

HP 81810S IC Design Verification System

**HP 8180A/B Data Generator
HP 8181A/B Data Generator Extender
HP 8182A/B Data Analyzer**

Operating and Programming Manual

This Manual applies to all Instruments



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PREFACE

PURPOSE OF THIS MANUAL

This manual deals with front panel operation and remote programming of the HP 8180A/B, 8181A/B and HP 8182A/B instruments. It can be used both as a training manual for new users, or as a reference work for experienced users.

AUDIENCE

This manual is intended for the user of any of the single instruments HP 8180A/B, HP 8181A/B and HP 8182A/B, or of the HP 81810S IC Design Verification System. If you require more information on any of the hardware or software of the HP 81810S system, refer to the additional manuals listed in the Related Publications.

RELATED PUBLICATIONS

Title	HP Part no.
HP 81810A System Software Manual	81810-90001
HP 81804A CAE Link Users Manual	81804-90001
HP 81810S System Configuration Manual	81810-90010
HP 8180A/B Data Generator HP 8181A/B Data Generator Extender HP 8182A/B Data Analyzer Operating and Programming Manual (This manual)	08180-90066
HP 15466A 256 Pin Testhead Operating and Programming Manual	15466-90001

CONTENTS

- Chapter 1, "General Information" contains general information on topics such as product overview, safety aspects, full specifications and a list of all options and accessories.
- Chapter 2, "Installation Procedures" describes the steps when inspecting the newly arrived equipment, and gives the procedure when claiming for damage. It then deals with the power requirements of the equipment and gives the procedures for its installation for use *on the bench*. Rack installations are covered in the System Configuration Manual. Finally, the chapter provides guidelines on storing and shipping the equipment.
- Chapter 3, "Generator Operation" gives tutorial and reference information on the front panel operation of the HP 8180A/B Generator, describing in sequence all of the Operating Pages of the instrument. It uses numerous examples to illustrate and clarify in step-by-step procedures the various operating procedures.
- Chapter 4, "Analyzer Operation" gives tutorial and reference information on the front panel operation of the HP 8182A/B Analyzer, describing in sequence all of the Operating Pages of the instrument. It uses numerous examples to illustrate and clarify in step-by-step procedures the various operating procedures.
- Chapter 5, "Increasing Generator and Analyzer Channel Count" shows how the stimulus channels can be increased with the use of up to two HP 8181A/B Generator Extenders per HP 8180A/B Generator or by using two generators in parallel. On the analysis side it shows how to increase the channel count by operating two analyzers in parallel.
- Chapter 6, "Device Measurements" describes several parametric tests on an AM 2909A Sequencer, which the user can himself perform, putting into practice what he has learned so far.
- Chapter 7, "Generator Programming" familiarizes the user with generator programming techniques. It uses HP BASIC as the computer programming language.
- Chapter 8, "Analyzer Programming" familiarizes the user with analyzer programming techniques. It uses HP BASIC as the computer programming language.
- Chapter 9, "Programming Examples" shows how to program the equipment to perform the tests done manually in Chapter 6.
- Chapter 10, "Syntax Diagrams" lists all HP-IB commands for programming the equipment, together with their correct syntax. The commands are listed in alphabetical, as well as Operating Page order.
- Chapter 11, "Generator Performance Verification" gives the procedures to verify in-spec performance of the HP 8180A/B Generator and the HP 8181A/B Generator Extender.
- Chapter 12, "Analyzer Performance Verification" gives the procedures to verify in-spec performance of the HP 8182A/B Analyzer.
- Appendix A, "Generator Standard Set" lists the standard (default) set of generator parameters.
- Appendix B, "Analyzer Standard Set" lists the standard (default) set of analyzer parameters.

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Appendix A Generator Standard Set

Appendix B Analyzer Standard Set

Glossary of Terms

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Chapter 1

General Information

1-1 Introduction

This Operating and Programming Manual contains information required to install, operate, program, and test the Hewlett-Packard Models 8180A/B, 8181A/B and 8182A/B, the Data Generator, the Data Generator Extender and the Data Analyzer respectively. The A-version of these instruments has memory depth of 1024 words, the B-version 16384 words.

Figures 1-1 and 1-2 show the generator (with extender) and the analyzer respectively, together with their accessories. Only the signal cables are supplied with each instrument. The number of cables supplied with each depends on the number of channels fitted. The cable accessories shown at the bottom of each figure must be ordered separately under their respective part numbers. The generator extender has a blank front panel with an on-off switch. The electrical and mechanical interconnecting accessories for the extender (shipped with the instrument) are shown in Figure 1-3.

A mains power cable correct for the country of destination and a spare fuse of the correct rating for the country of destination (both not shown) are included with each instrument.

This chapter covers instrument identification, description, specifications, options, accessories and other basic information.

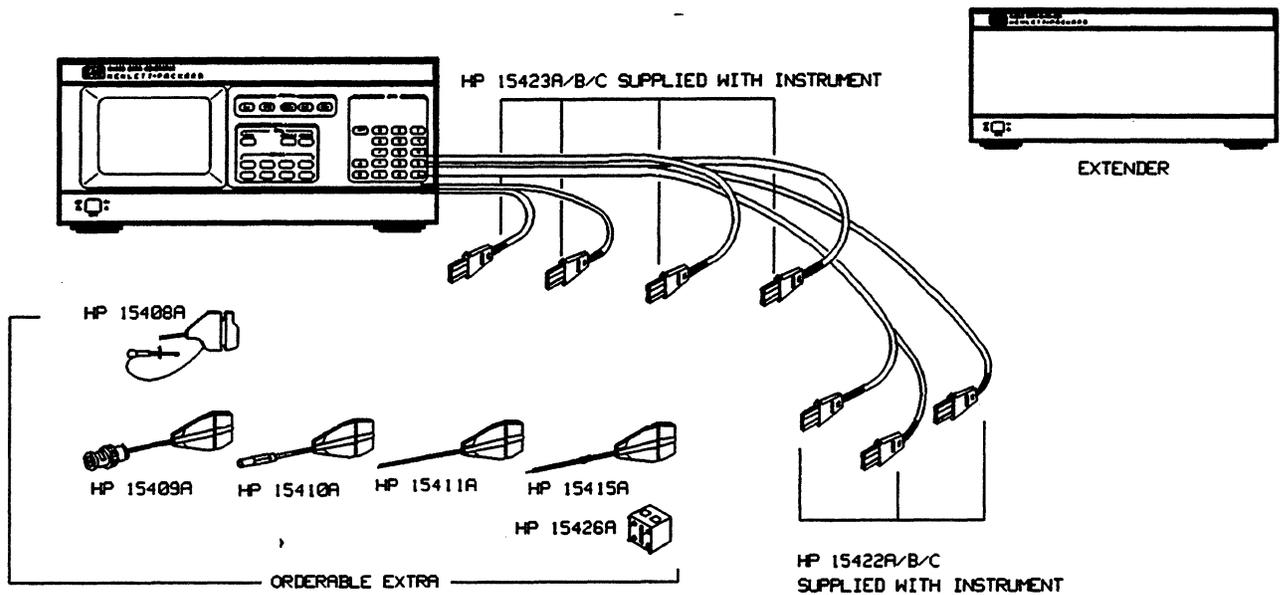


Figure 1-1. HP 8180A/B Data Generator (with HP 8181A/B Extender) and Accessories

Safety Considerations

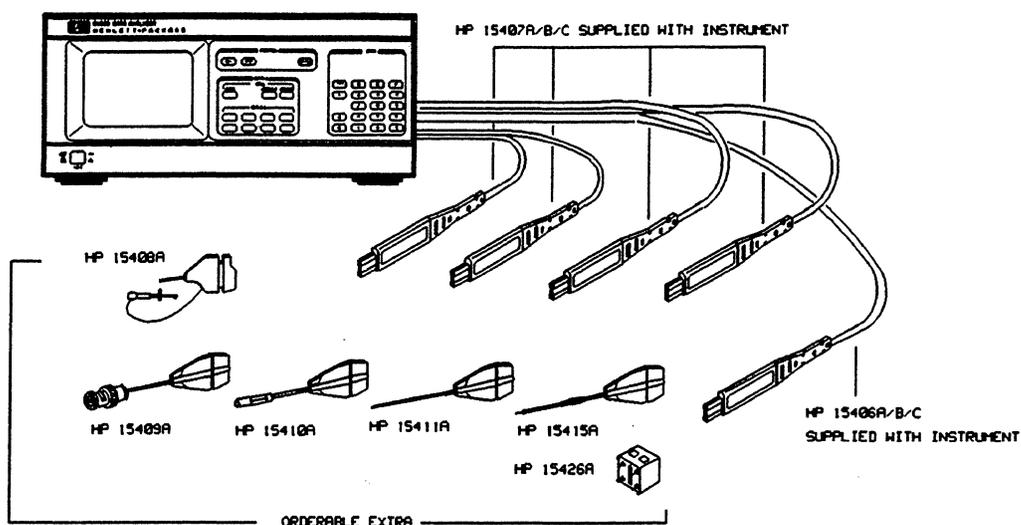


Figure 1-2. HP 8182A/B Data Analyzer and Accessories

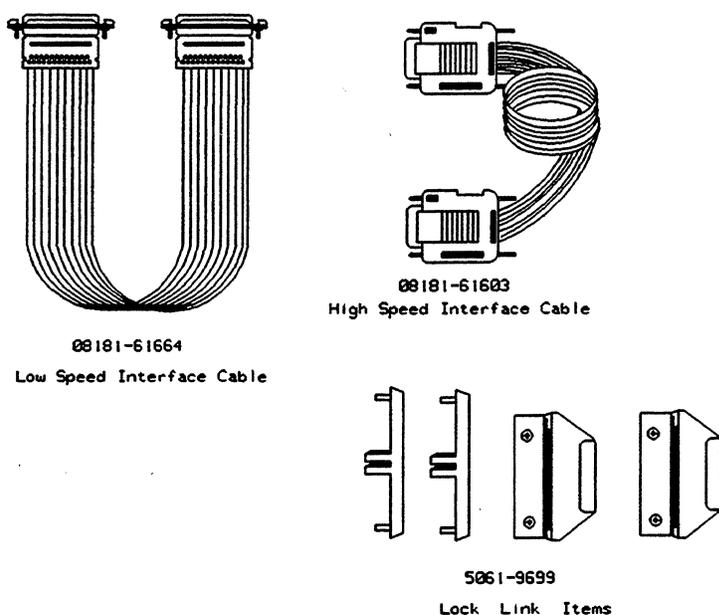


Figure 1-3. Mechanical and Electrical Interconnecting Accessories for the Extender

1-2 Safety Considerations

The Models 8180A/B, 8181A/B and 8182A/B are Safety Class 1 instruments (instruments with an exposed metal chassis that is directly connected to earth via the power supply cable).

Before operation, the instruments and manual, including the red safety page, should be reviewed for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instruments in a safe condition.

Brief Description of Instruments

1-3 Instruments Covered by the Manual

Attached to the rear of each instrument is a serial number plate (Figure 1-4). The first four digits of the serial number only change when there is a significant change to the instrument. The last five digits are assigned to instruments sequentially. The contents of this manual apply directly to the instrument serial number quoted on the title page (or to all instruments if stated). For instruments with higher serial numbers, refer to the Manual Change sheets supplied with this manual. In addition to change information, the Manual Change sheets may contain information for correcting any errors in the manual.

To keep this manual as up-to-date and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified by a print date and part number, both of which appear on the title page. Complimentary copies of the supplement are available from Hewlett-Packard.

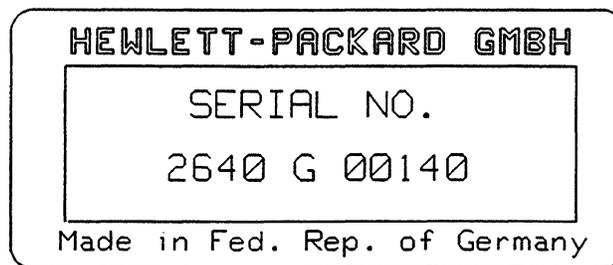


Figure 1-4. Serial Number Plate

1-4 Brief Description of Instruments

The 8180A/B is a modular, high speed (50MHz) programmable data generator for the stimulation of multi-channel digital circuits. It has the capability to control up to two 8181A/B Data Generator Extenders. By combining the 8180A/B (with or without the 8181A/B) and the 8182A/B Data Analyzer, a complete stimulus/response system for ac-parametric hardware analysis of digital ICs, boards and modules can be set up. Both the generator and the analyzer have an operating concept based around a CRT and softkeys. Remote program control over the HP-IB is straightforward since every parameter can be directly accessed. (HP-IB is the Hewlett-Packard Interface Bus, Hewlett-Packard's implementation of ANSI/IEEE Standard 488 - Standard Digital Interface for Programmable Instrumentation).

Possible 8180A/B and 8181A/B Configurations

The 8180A/B Data Generator contains up to 16 data channels. The data channel count can be extended by adding up to two 8181A/B Data Generator Extenders. Each extender contains up to 24 data channels. The complete data generator configuration is controlled via the 8180A/B and contains up to 64 parallel data channels in total. Also, two 8180A/B Data Generators can be synchronized, allowing the configuration to be expanded up to 128 channels.

Specifications Options, Accessories

Summary of the 8180A/B and 8181A/B Features

- 1Hz-50MHz data rate
- 8-64 NRZ-channels (non-return-to-zero)
- up to 8 RZ-channels (return-to-zero) with 100ps resolution for delay and width
- two clock channels with 100ps resolution for delay and width
- 1 kbit memory/channel, non-volatile for A-version
- 16 kbit memory/channel, non-volatile for B-version
- -2V to +17V into open (-2V to +5.5V into 50 Ohm with 10 mV resolution)
- 3.5 ns transition times for TTL, typically 1.5 ns for ECL
- comfortable data pattern editing; convenient softkey operation
- full HP-IB programmability

Possible 8182A/B Configurations

The 8182A/B Data Analyzer contains up to 32 data channels. The data channel count can be extended by connecting two or three 8182A/B Data Analyzers in parallel.

Summary of the 8182A/B Features

- 1Hz-50MHz data rate (synchronous and asynchronous)
- 8-32 channels
- 1 kbit memory/channel, non-volatile for A-version
- 16 kbit memory/channel, non-volatile for B-version
- delayable sampling point referenced to the active clock edge with 100ps resolution
- real time window compare with 100ps resolution for window width and placement
- glitch detection and storage
- -2V to +17V into open (-2V to +5.5V into 50 Ohm with 10 mV resolution)
- 3.5 ns transition times for TTL, typically 1.5 ns for ECL
- comfortable compare pattern editing; convenient softkey operation
- full HP-IB programmability

1-5 Specifications, Options, Accessories

Instrument specifications for the 8180A/B, 8181A/B and 8182A/B are listed below. These specifications are the performance standards or limits against which the instruments are tested.

Specifications Options, Accessories

If not otherwise mentioned, specifications are valid at the end of the supplied data cables (1.5m...4m length)

Vector Memory	HP 8180A/B Generator	HP 8181A/B Extender																				
vector depth (A/B version)	1k/16k words	1k/16k words																				
max. vector width	16 channels	24 channels																				
memory loading and editing																						
data code	BIN, OCT, HEX, DEC	The Extender has no display and no front panel. Data entry via the Generator's front panel or HP-IB. For data and address codes/editing see Generator.																				
address code	OCT, HEX, DEC																					
data entry	front panel or HP-IB																					
displayed channel order	user defined																					
line edit	insert, delete, copy, move, macro																					
channel edit	clear, set, copy, PRBS, counts, entry mask																					
Outputs																						
clock channels	2 (RZ-type)	The Extender has no clocks																				
strobe channels	1 (it can either be an NRZ data channel or the reference clock)	The Extender has no strobe channel																				
strobe levels	TTL settings: high $\geq 2.4V$, low $\leq 0.2V$ ECL settings: high $\geq -0.8V$, low $\leq -1.7V$ Levels are valid for operating into 50 Ohm (voltage doubles, if no load is connected).																					
strobe pulse width in clock mode	10ns \pm 3ns																					
data channels	8...16; expandable in modules of 4	8...24; expandable in modules of 4 (NRZ-types only)																				
NRZ	8...16; expandable in modules of 4																					
RZ	0...8; expandable in modules of 4																					
output impedance of data channels, clocks and strobe	50 Ohm Load condition is selectable in common for 50 Ohm or high impedance																					
output levels of Generator and Extender	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border-right: 1px dashed black; padding: 5px;">output driver from 50 Ohm into 50 Ohm (voltage doubles, if no load is connected)</td> <td style="width: 50%; padding: 5px;">output driver from 50 Ohm into high impedance ($\geq 10k\Omega$)</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">-1.5V to +5.5V</td> <td style="padding: 5px;">-1.0V to +17.0V</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">-2.0V to +5.0V</td> <td style="padding: 5px;">-2.0V to +16.0V</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">10 mV</td> <td style="padding: 5px;">20mV; (for V out $> 10V$: 100mV)</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">0.5V to 5.5V</td> <td style="padding: 5px;">1.0V to 17.0V</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">...20 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 30mV$ For 4m cable length : high level: -0.5%/-1.5% of [high level] $+2\%$/-4% of amplitude $\pm 30mV$ low level: -0.5%/-1.5% of [high level] $+4\%$/-2% of amplitude $\pm 30mV$ (add $\pm 30mV$ for amplitudes $< 0.7V$)</td> <td style="padding: 5px;">...40 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 60mV$ (add $\pm 60mV$ for amplitudes $< 1.5V$)</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">...1 ms settling time: $\pm 0.5\%$ of level $\pm 30mV$ (add $\pm 30mV$ for amplitudes $< 0.7V$)</td> <td style="padding: 5px;">...1 ms settling time: $\pm 0.5\%$ of level $\pm 60mV$ (add $\pm 60mV$ for amplitudes $< 1.5V$)</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">$< 3ns + amplitude \times 0.2ns/V$ (add 0.2ns for cable length $> 1.5m$)</td> <td style="padding: 5px;">$< 3ns + amplitude \times 0.5ns/V$ (add 0.2ns for cable length $> 1.5m$)</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">1.5ns (1.7ns for cable length $> 1.5m$)</td> <td style="padding: 5px;">---</td> </tr> <tr> <td style="border-right: 1px dashed black; padding: 5px;">max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)</td> <td style="padding: 5px;">max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)</td> </tr> </table>		output driver from 50 Ohm into 50 Ohm (voltage doubles, if no load is connected)	output driver from 50 Ohm into high impedance ($\geq 10k\Omega$)	-1.5V to +5.5V	-1.0V to +17.0V	-2.0V to +5.0V	-2.0V to +16.0V	10 mV	20mV; (for V out $> 10V$: 100mV)	0.5V to 5.5V	1.0V to 17.0V	...20 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 30mV$ For 4m cable length : high level: -0.5% / -1.5% of [high level] $+2\%$ / -4% of amplitude $\pm 30mV$ low level: -0.5% / -1.5% of [high level] $+4\%$ / -2% of amplitude $\pm 30mV$ (add $\pm 30mV$ for amplitudes $< 0.7V$)	...40 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 60mV$ (add $\pm 60mV$ for amplitudes $< 1.5V$)	...1 ms settling time: $\pm 0.5\%$ of level $\pm 30mV$ (add $\pm 30mV$ for amplitudes $< 0.7V$)	...1 ms settling time: $\pm 0.5\%$ of level $\pm 60mV$ (add $\pm 60mV$ for amplitudes $< 1.5V$)	$< 3ns + amplitude \times 0.2ns/V$ (add 0.2ns for cable length $> 1.5m$)	$< 3ns + amplitude \times 0.5ns/V$ (add 0.2ns for cable length $> 1.5m$)	1.5ns (1.7ns for cable length $> 1.5m$)	---	max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)	max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)
output driver from 50 Ohm into 50 Ohm (voltage doubles, if no load is connected)	output driver from 50 Ohm into high impedance ($\geq 10k\Omega$)																					
-1.5V to +5.5V	-1.0V to +17.0V																					
-2.0V to +5.0V	-2.0V to +16.0V																					
10 mV	20mV; (for V out $> 10V$: 100mV)																					
0.5V to 5.5V	1.0V to 17.0V																					
...20 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 30mV$ For 4m cable length : high level: -0.5% / -1.5% of [high level] $+2\%$ / -4% of amplitude $\pm 30mV$ low level: -0.5% / -1.5% of [high level] $+4\%$ / -2% of amplitude $\pm 30mV$ (add $\pm 30mV$ for amplitudes $< 0.7V$)	...40 ns settling time: $\pm 0.5\%$ of level $\pm 3\%$ of amplitude $\pm 60mV$ (add $\pm 60mV$ for amplitudes $< 1.5V$)																					
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$< 3ns + amplitude \times 0.2ns/V$ (add 0.2ns for cable length $> 1.5m$)	$< 3ns + amplitude \times 0.5ns/V$ (add 0.2ns for cable length $> 1.5m$)																					
1.5ns (1.7ns for cable length $> 1.5m$)	---																					
max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)	max. $\pm 10\%$ of amplitude (max. $+8\%$ / -12% of amplitude for cable length $> 1.5m$)																					
high level range																						
low level range																						
resolution																						
amplitude range																						
level accuracy after....																						
level accuracy after....																						
transition times (10%...90%)																						
typ. transition times for ECL levels (20%...80%)																						
preshoot, overshoot, ringing																						

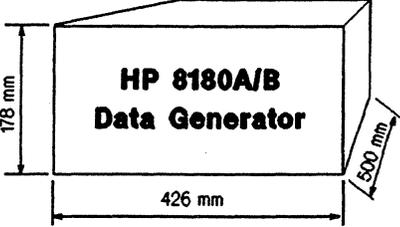
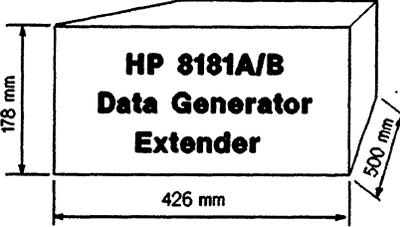
Specifications Options, Accessories

Outputs (continued)	HP 8180A/B Generator	HP 8181A/B Extender
video output	composite video signal, negative SYNC 1.0 Vpp into 75 Ohm typ. (recommended monitor HP 82913A)	not applicable
Timing		
<p>general</p> <p>clock and data frequency (the Extender contains no clock channels)</p> <p>range</p> <p>resolution</p> <p>accuracy</p> <p>repeatability</p> <p>jitter (max)</p> <p>channel skew (A version in brackets)</p>	<p>Timing specs are valid for operation into 50 Ohm. Skew and delay specs are valid for the 50% points of a signal with 2.5V amplitude. For different amplitudes:</p> $\text{delay changes with } \frac{0.2\text{ns} \times (\text{amplitude} - 2.5\text{V})}{V}$ $\text{and skew changes with } \frac{0.2\text{ns} \times \text{amplitude} - 2.5\text{V} }{V}$ <p>Delay is measured with respect to the strobe output (clock mode), TTL setting, 50% point of amplitude.</p> <p>1.05Hz...50MHz</p> <p>3 digits</p> <p>± 5% of prog. value</p> <p>factor 4 better than accuracy</p> <p>± (0.2% of period setting + 100ps)</p> <p>±0.8 (±1.0)ns for a 64 channel system (1 Generator + 2 Extenders) ±1.5 (±2.0)ns for a 128 channel system (2 Generators + 4 Extenders) (RZ delays programmed to zero)</p>	
<p>delay (clocks & data channels except Generator's NRZ channels)</p> <p>range</p> <p>resolution</p> <p>accuracy</p> <p>repeatability</p> <p>max. jitter</p> <p>max. delay</p>	<p>0.0ns...950ms</p> <p>3 digits (exception: 90ns...100ns and 990ns...1.0us, 2 digits) best case 100ps</p> <p>± 5% of programmed value ± 1ns</p> <p>factor 4 better than accuracy</p> <p>± (0.2% of delay setting + 150ps)</p> <p>90% of period - 18ns</p>	<p>0.0ns...950ms</p> <p>3 digits (exception: 90ns...100ns and 990ns...1.0us, 2 digits) best case 100ps</p> <p>± 5% of programmed value ± 1ns</p> <p>factor 4 better than accuracy</p> <p>± (0.2% of delay setting + 150ps)</p> <p>90% of period - 18ns</p>
<p>width (clocks & RZ channels)</p> <p>range</p> <p>resolution</p> <p>accuracy</p> <p>repeatability</p> <p>max. jitter</p> <p>max. width</p>	<p>10.0ns...950ms</p> <p>3 digits (best case 100ps)</p> <p>± 5% of programmed value ± 1ns</p> <p>factor 4 better than accuracy</p> <p>±(0.2% of width setting + 150ps)</p> <p>90% of period - 8ns</p> <p style="text-align: right;">not applicable</p>	

Specifications Options, Accessories

Inputs	HP 8180A/B Generator	HP 8181A/B Extender										
<p>All inputs are edge triggered and can be enabled or disabled independently</p> <p>available control inputs</p> <p>input impedance</p> <p>threshold range</p> <p>threshold accuracy</p> <p>threshold overdrive</p> <p>min. pulse width at thresh</p> <p>active edge</p> <p>max. input voltage</p> <p>min. amplitude</p>	<p>ext. CLOCK STOP BREAK RUN (GATE)</p> <p>50 Ohm / 100K Ohm (selectable) -10V...+10V with 100mV resolution $\pm 3\%$ of programmed value $\pm 50\text{mV}$ $\geq 100\text{mV}$ 8 ns pos. or neg. (selectable)</p> <p>$\pm 10\text{V}$ into 50 Ohm, $\pm 20\text{V}$ into 100k Ohm 250mVpp</p>	<p>Extender is controlled via Generator's control inputs</p>										
HP-IB												
<p>general</p> <p>programming times (time to execute a message, typ.)</p> <p>period</p> <p>delay, width</p> <p>level</p> <p>transfer times (time to receive a message, typ.)</p> <p>transfer time for ≤ 255 characters</p> <p>number of characters per command</p> <p>vector memory load time, typ.</p> <p>formatted (HEX), 16 channels</p> <p>64 channels</p> <p>unformatted, 16 channels</p> <p>64 channels</p>	<p>All data, parameters and modes are programmable via HP-IB. With a specific command the display of the Generator may be used as a format free, general purpose alphanumeric display (monitor).</p> <p>45 ms</p> <p>10 ms</p> <p>12 ms</p> <p>$\leq 60\mu\text{s}$ per character</p> <p>4..6 for modes, 6..11 for levels and timings</p> <table border="1" data-bbox="587 1260 1057 1501"> <thead> <tr> <th>HP 8180A with 1k chan.depth</th> <th>HP 8180B with 16k chan.depth</th> </tr> </thead> <tbody> <tr> <td>10 sec</td> <td>180 sec</td> </tr> <tr> <td>30 sec</td> <td>500 sec</td> </tr> <tr> <td>400 msec</td> <td>120 msec *</td> </tr> <tr> <td>900 msec</td> <td>460 msec *</td> </tr> </tbody> </table> <p>* HP 9000 Series 300 controller with 98620-66502 DMA card</p>	HP 8180A with 1k chan.depth	HP 8180B with 16k chan.depth	10 sec	180 sec	30 sec	500 sec	400 msec	120 msec *	900 msec	460 msec *	<p>The HP 8181A/B programming is performed via the Generators HP-IB interface. The Extender is directly connected to the Generator's processor bus.</p>
HP 8180A with 1k chan.depth	HP 8180B with 16k chan.depth											
10 sec	180 sec											
30 sec	500 sec											
400 msec	120 msec *											
900 msec	460 msec *											
<p>vector, parameter and mode storage capability (non-volatile)</p>	<p>1 active operating vector/parameter/mode set 3 programmable parameter/mode sets 1 standard parameter/mode set 9 first/last address pair set</p>											

Specifications Options, Accessories

General	HP 8180A/B Generator	HP 8181A/B Extender
recalibration period warm-up time environmental (A/B version) storage temp. operating temp. max. operating humidity at 40°C	1 year 30 minutes - 40°C 75°C / - 40°C 75°C 0°C 50°C / 5°C 40°C 95% R.H. / 80% R.H.	
power weight dimensions	115/230V rms +10%, -22%; 48...66Hz; 800VA, 460W max. net 19.0 kg (42 lbs) shipping 26.0 kg (58 lbs)	115/230V rms +10%, -22%; 48...66Hz; 700VA, 410W max. net 18.5 kg (41 lbs) shipping 23.5 kg (52 lbs)
	 <p align="center">(7 x 16.8 x 19.7 inch)</p>	 <p align="center">(7 x 16.8 x 19.7 inch)</p>
Ordering Information		
the basic version contains options retrofit options	Data Generator: HP 8180A/B 2 clock channels 1 strobe channel 8 NRZ data channels accessories: one set of clock cables two sets of data cables 1 x 15426A receptacles operating & programming manual for HP 8180/81/82 A/B 001 4 additional NRZ data channels (incl. one set of data cables, 1 x 15426A) 002 4 additional RZ data channels (incl. one set of data cables, 1 x 15426A) 907 front handle kit (part no. 5061-9690) 908 rack flange kit (part no. 5061-9678) 909 rack flange and front handle com- bination (part no. 5061-9684) 916 additional operating & programming manual (HP 8180/81/82 A/B)	Generator Extender: HP 8181A/B 8 NRZ data channels accessories: two sets of data cables 1 x 15426A receptacles no separate manual, information is part of the HP 8180A/B manual 001 4 additional NRZ data channels (incl. one set of data cables, 1 x 15426A) 907 front handle kit (part no. 5061-9690) 908 rack flange kit (part no. 5061-9678) 909 rack flange and front handle com- bination (part no. 5061-9684)
	81801A/B retrofit of option 001 at HP office 81802A/B retrofit of option 002 at HP office	81801A/B retrofit of option 001 at HP office

Specifications Options, Accessories

If not otherwise mentioned, specifications are valid at the front-end of the active probes (1.5m....4m cable length)

Vector Memory	HP 8182A/B Data Analyzer
vector depth max. vector width expected data memory loading and editing data code address code data entry displayed channel order line edit channel edit	1k/16k words (A/B version) 32 channels BIN, OCT, HEX DEC Keyboard, HP-IB or read-in from DUT user defined insert, delete, word mask (don't care) clear, set, copy, exchange, mask (don't care)
Inputs	HP 8182A/B Data Analyzer
data channels input impedance input capacity overvoltage protection max. input amplitude threshold range threshold resolution threshold set single thresh. accuracy dual thresh. accuracy lower thresh. upper thresh. min. difference between upper and lower thresh. max. input signal devi- ation from any threshold threshold overdrive level detection accuracy 50ms after input signal transition clock input input impedance input capacity overvoltage protection max. input amplitude hysteresis symmetrical to threshold threshold overdrive min. clock pulse width at threshold min. clock slew rate	<p>The clock and data inputs are active probes. 8....32; expandable in modules of 8 1 MOhm \pm 5% typ. \leq 7pF typ. \pm 100V continuous 10Vpp (for amplitudes up to 10Vpp refer to operating manual) -10V....+10V 10mV 6 single and 6 dual threshold voltage sets can be programmed. Any of these sets can be assigned to any data input channel \pm 2% of prog. value \pm 10mV \pm 2% of prog. value \pm 10mV \pm 1% of prog. upper threshold \pm 1% of lower threshold \pm 1% of prog. (upper minus lower) threshold \pm 10mV 100mV 10V \geq 10(20*)% of amplitude or \geq 50(150*)mV, whichever is bigger actual threshold \pm 15mV (*) value for input cables >1.5m</p> <p>The clock input threshold voltage is individually programmable. The active clock slope is selectable to be positive, negative or both</p> <p>1 MOhm \pm 5% typ. \leq 7pF typ. \pm 100V continuous 10Vpp (for amplitudes up to 10Vpp refer to operating manual) 100mV max. \geq 10(20*)% of amplitude or \geq 100(200*)mV, whichever is bigger (*) value for input cables >1.5m 5 ns 10 V/us</p>

Specifications Options, Accessories

Inputs (continued)	HP 8182A/B Data Analyzer
control inputs	for each input an individual threshold can be set up
clock qualifier	1 (level triggered, active level: high, low or don't care)
trigger arm	1 (edge triggered, active slope: pos., neg. or don't care)
trigger qualifier	1 (level triggered, active level: high, low or don't care)
external stop	1 (edge triggered, active slope: pos., neg. or don't care)
input impedance	50 Ohm or 100k Ohm typ. (selectable for each input independently)
threshold range	-10 V +10 V
threshold resolution	10 mV
threshold accuracy	± 3% of prog. value ±50 mV
threshold overdrive	≥ 100 mV
max. input voltage	±10 V in to 50 Ohm, ±20 V in to 100k Ohm
min. amplitude	250 mVpp
min. pulse width at thresh.	8 ns
setup time	5 ns
hold time	0 ns
Timing	

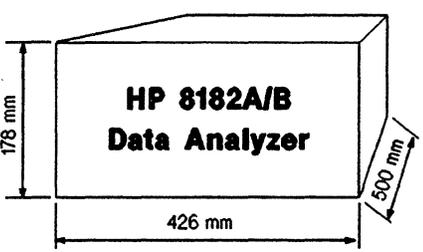
Timing specifications apply for equal amplitudes of clock and data inputs, ≥0.5 Vpp, with threshold programmed to the middle between high and low level of input signal.

... in standard analysis mode		... in real time compare mode	
external clock operation		max. clock frequency	50 MHz
max. clock frequency	50 MHz	prog. compare window delay range	0....1.0s
prog. clock delay range	0...1 sec.	compare window delay resolution	3 digits (best case 100ps)
clock delay resolution	3 digits (best case 100 ps)	max. compare window delay	95% of period - 1ns
sampl. point accuracy	± 5% of prog. clock delay ± 1 ns (clock input to data channels, including channel skew; this specification replaces setup and hold time specifications)	compare window delay accuracy	± 5% of prog. value ± 2ns
sampl. point repeatability	factor 4 better than accuracy	compare window delay repeatability	factor 4 better than accuracy
max. clock delay	95% of period - 1ns	prog. compare window width range	10.0ns....1.0s
min. detectable pulse and glitch width at threshold	5 ns (6 ns for 4m cable length)	compare window width resolution	3 digits (best case 100 ps)
channel skew	± 1ns around sampling point	max. compare window width	95% of period - 9ns
internal clock operation		compare window width accuracy	± 5% of prog. value ± 1ns
prog. clock period range	20ns....1.0s (1Hz...50MHz)	compare window width repeatability	factor 4 better then accuracy
clock period step	1-2-5 sequence	min. pulse width at threshold	5 ns (6 ns for 4m cable length)
clock period accuracy	0.01% of prog. period	min. error width	5ns
min. detectable pulse and glitch width at threshold	5 ns (6 ns for 4m cable length)	channel skew	± 1ns around window edges
channel skew	≤ 2ns		

Specifications Options, Accessories

Triggering	HP 8182A/B Data Analyzer													
trigger condition depends on...	<ul style="list-style-type: none"> - the two control inputs: "trigger arm" "trigger qualifier" - the trigger word across all channels - the trigger word counter (range: 1....16) - the digital trigger delay (range: 0....65535 clock periods) (The trigger condition can be selected to start or to stop the analysis)													
Outputs														
available indicator outputs	real time error output latched error output trigger word match output active state indicator clock output													
high level low level transition times propagation delay for pulsed and latched error output signal with respect to data probe input	2.5V typ. 0V typ. $\leq 4\text{ns}$ 60 ns typ.	levels apply when driving into 50 Ohm load (voltage doubles, if no load is connected)												
video output	composite video signal, negative SYNC 1.0V into 75 Ohm typ. (recommended monitor HP 82913A)													
HP-IB														
general	All data, parameters and modes are programmable via HP-IB. With a specific command the display of the Analyzer may be used as a format free, general purpose alphanumeric display (monitor). Times are measured by programming with the HP 9826A computer and remote message page of 8182A/B active.													
programming times (time to execute a message, typ.)														
int. clock period delay, width threshold run	7 ms 24 ms 70 ms													
transfer times (time to receive a message, typ.)														
transfer time for ≤ 255 characters number of characters per command	≤ 75 us per character 4...6 for modes, 6...11 for thresholds and timing													
expected vector memory load time, typ.														
formatted (HEX), 8 channels 32 channels unformatted, 8 channels 32 channels word mask	<table style="border-collapse: collapse; width: 100%;"> <thead> <tr> <th style="border-bottom: 1px dashed black; width: 50%; text-align: center;">HP 8182A with 1k chan.depth</th> <th style="border-bottom: 1px dashed black; width: 50%; text-align: center;">HP 8182B with 16k chan.depth</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">21 sec</td> <td style="text-align: center;">181 sec</td> </tr> <tr> <td style="text-align: center;">37 sec</td> <td style="text-align: center;">472 sec</td> </tr> <tr> <td style="text-align: center;">90 ms</td> <td style="text-align: center;">60 ms *</td> </tr> <tr> <td style="text-align: center;">320 ms</td> <td style="text-align: center;">230 ms *</td> </tr> <tr> <td></td> <td style="text-align: center;">170 ms *</td> </tr> </tbody> </table>	HP 8182A with 1k chan.depth	HP 8182B with 16k chan.depth	21 sec	181 sec	37 sec	472 sec	90 ms	60 ms *	320 ms	230 ms *		170 ms *	* HP 9000 series 300 controller with 98620- 66502 DMA card
HP 8182A with 1k chan.depth	HP 8182B with 16k chan.depth													
21 sec	181 sec													
37 sec	472 sec													
90 ms	60 ms *													
320 ms	230 ms *													
	170 ms *													

Specifications Options, Accessories

HP-IB (continued)	HP 8182A/B Data Analyzer	
captured vector memory load time, typ. formatted (HEX), 8 channels 32 channels unformatted, 8 channels 32 channels error map	HP 8182A with 1k chan.depth <hr style="border-top: 1px dashed black;"/> 9 sec 18 sec 90 ms 320 ms	HP 8182B with 16k chan.depth <hr style="border-top: 1px dashed black;"/> 152 sec 281 sec 100 ms * 360 ms * 260 ms * * HP 9000 series 300 controller with 98620-66502 DMA card
vector, parameter and mode storage capability (non-volatile)	1 active operating data/parameter/mode set 3 programmable parameter/mode sets 1 standard parameter/mode set	
General		
recalibration period warm-up time environmental (A/B version) storage temp. operating temp. max. operating humidity at 40°C power weight dimensions	1 year 30 minutes - 40°C 75°C / - 40°C 75°C 0°C 50°C / 5°C 40°C 95% R.H. / 80% R.H. 115/230V rms +10%, -22%; 48...66Hz 900VA max, 510W max. net 20.0 kg (44 lbs) shipping 27.0 kg (60 lbs)	
		
Ordering Information		
Analyzer the basic version contains options retrofit option	HP 8182A/B 8 data channels accessories: one set of clock probes two sets of data cables with probes 1 x 15426A receptacles, 2 x 15408A set of grabbers operating & programming manual 001 8 data channels (incl. data cables with probes, 1 x 15426A, 2 x 15408A) 907 front handle kit (part no. 5061-9690) 908 rack flange kit (part no. 5061-9678) 909 rack flange kit and front handle combination (part no. 5061-9684) 916 additional operating & programming manual (HP 8180/81/82 A/B) 81821A/B retrofit of option 001 at HP office	

Specifications Options, Accessories

Optional Accessories

HP Number	description	useful for:
15406A/B/C *	clock probe (cable length: A=1.5m B=2.4m C=4m)	HP 8182 A/B
15407A/B/C *	cable set with probes for 4 data channels (cable length: A=1.5m B=2.4m C=4m)	HP 8182 A/B
15408A	5 plug-on grabbers with ground leads	HP 8180/81/82 A/B
15409A	5 plug-on BNC adapters	HP 8180/81/82 A/B
15410A	5 plug-on SMB adapters	HP 8180/81/82 A/B
15411A	5 plug-on coax open-end adapters for fixed wiring or use with custom connector	HP 8180/81/82 A/B
15415A	5 plug-on mini-probes, which can be used in conjunction with the HP 10024A IC Test Clip for easy probing of dual in-line packages	HP 8180/81/82 A/B
15416A	cable for parallel operation of 2 instruments	HP 8182 A/B
15421A	cable for parallel operation of 2 instruments	HP 8180 A/B
15422A/B/C *	cable-set for clock 1, clock 2 and strobe (cable length: A=1.5m B=2.4m C=4m)	HP 8180 A/B
15423A/B/C *	cable-set for 4 data channels (cable length: A=1.5m B=2.4m C=4m)	HP 8180/81 A/B
15426A	20 solder-in receptacles	HP 8180/81/82 A/B
15429A	10 solder-in receptacles	HP 8180/81/82 A/B
15476A	System Rack 56" (please refer to Ordering & Configuration Guide P/N 5952-9615)	
15477A	System Rack 24" (please refer to Ordering & Configuration Guide P/N 5952-9615)	
15480A	cable for parallel operation of 3 instruments	HP 8180B

* If modules are installed in a system rack HP 15476A and when the Test Head HP 15466A is used cable length must be 4m (HP 154xxC).

For more information please refer to these publications, available from your HP sales office:

Technical Data Sheet Software (describes the HP 81810A System Software and HP 81804A CAE Link Software)	P/N 5952-9613
Product Brochure (provides an overview about the HP 81810S IC Design Verification System)	P/N 5952-9614
Ordering & Configuration Guide (includes ordering and configuration details)	P/N 5952-9615
Technical Data Sheet DC PMU HP 4141B (provides technical information and specification)	P/N 5950-2875
Technical Data Sheet Power Supply HP 6624A (provides technical information and specifications)	P/N 5952-4148

Chapter 2 Installation

WARNING

The 8180B, 8181B and 8182B instruments weigh 19.0 kg (42 lbs), 18.5 kg (41 lbs) and 20 kg (44 lbs) respectively. Care must be exercised when lifting to avoid personal injury.

2-1 Introduction

This chapter provides installation instructions for the 8180B, the 8181B and the 8182B, as well as their accessories. It also includes information about initial inspection and damage claims, preparation for use, packaging, storage and shipment.

2-2 Initial Inspection and Claims for Damage

Inspect the shipping container for damage. If the container or cushioning is damaged, it should be kept until the contents of the shipment have been checked for completeness, and the instrument has been verified mechanically and electrically. The contents of the shipment should be as shown in Figures 1-1, 1-2 or 1-3 depending on your order, plus any accessories that were ordered with the instrument(s). Procedures for checking the electrical operation are given in Chapter 3 onwards. If the contents are incomplete, mechanical damage or defect is apparent, or if an instrument does not pass the operator's checks or meet specification when received, notify the nearest Hewlett-Packard Sales/Service Office. Keep the shipping materials for carrier's inspection. The HP Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

2-3 Power Requirements

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any part of the outer enclosure (covers, panels, connectors and so on).

The instruments require a power source of 115/230 V rms (+10% -22%) at a frequency of 48 - 66 Hz single phase. The maximum power consumptions are: 8180A/B - 460 W (800 VA), 8181A/B - 410 W (700 VA), 8182A/B - 510 W (900 VA).

2-4 Line Voltage Selection

CAUTION

DO NOT SWITCH ON THE INSTRUMENTS before reading the following section.

1. Read the safety summary - red sheet - at the front of this manual.

Installation

2. Make sure the instruments are set to the local line voltage. If a change is made to the voltage selector switch setting, ensure you supply a fuse of the correct loading - see below.
3. Before changing the fuse switch off the instruments and disconnect the power cables.

Figure 2-1 provides information for line voltage and fuse selection.

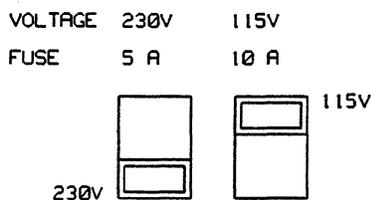


Figure 2-1. Switch Settings for Line Voltages and Correct Fuses

2-5 Power Cable

In accordance with international safety standards, the instruments are equipped with a three-wire power cable. When connected to an appropriate A.C. power receptacle, this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends upon the country of destination. Refer to Figure 2-2 for the part number of the power cable available.

WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on.

- If the instruments are to be powered via an autotransformer for voltage reduction, ensure that the common terminal of the autotransformer is connected to the grounded pole of the power source.
- The power cable plug shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.
- Make sure that the protective ground terminal of each instrument is connected to the protective conductor of the power cable. To verify this, check that the resistance between the instrument chassis and the front panel, and the ground pin of the power cable is zero Ohms.

The following work must be carried out by a qualified electrician. All local electrical codes must be strictly observed. If the plug on the cable does not fit the power outlet, or the cable is to be attached to a terminal block, cut the cable at the plug end and re-wire it. The color coding used in the cable will depend on the cable supplied. Figure 2-2 gives the plug identification for the available power cables.

Installation

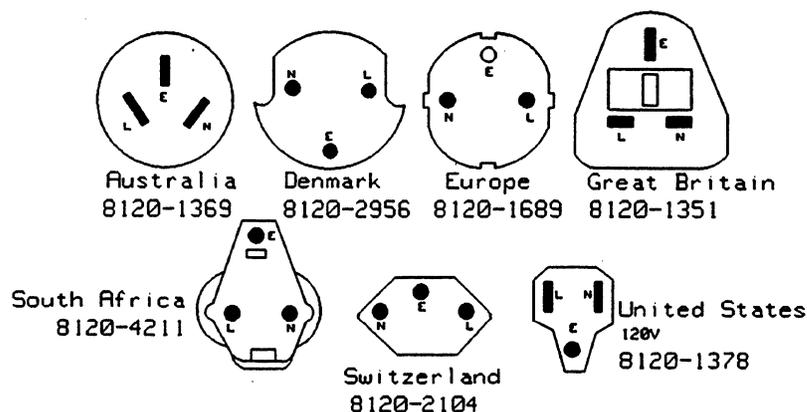


Figure 2-2. Power Cables Available - Plug Identification

If a new plug is to be connected, it must meet local safety requirements and include the following features:

- Adequate load-carrying capacity (see the specifications section in Chapter 1).
- Ground connection.
- Cable clamp.

2-6 Front Handle/Rack Mounting

If metal handles are to be fitted to the (front of the) instruments, the plastic trim, shown in Figure 2-3 must first be removed. To release the trim, place the blade of a small screwdriver under it and give a sharp tap onto the back of the screwdriver. The handles themselves have a similar plastic trim fitted. This has to be taken off when removing or mounting the handles. The procedure to do this is identical.

Rack mounting information (when using the instruments in a Test System) is given in the System Configuration Manual (see Related Publications at the front of this manual).

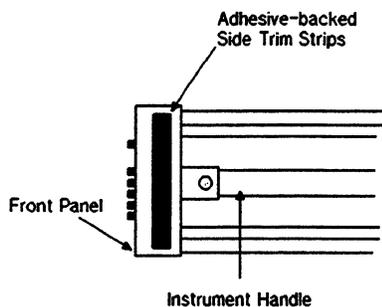


Figure 2-3. Removing Plastic Trim

2-7 Storage and Shipment

The instruments can be stored or shipped at temperatures between minus 40°C and plus 75°C. The instruments should be protected from temperature extremes which may cause condensation within them.

If an instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required. The original shipping carton and packing material may be re-usable, but the Hewlett-Packard Sales/Service Office will

Installation

provide information and recommendations on materials to be used if the original packing is no longer available or re-usable. General instructions for re-packing are as follows:

1. Wrap the instrument in heavy paper or plastic.
2. Use a strong shipping container. A double wall carton made of material with 350 pound (120 kg) burst test rating is adequate.
3. Use enough shock-absorbing material (3 to 4 inch layer - 10 cm) around all sides of the instrument to provide a firm cushion and prevent movement inside the container. Protect the control panel of the instrument with cardboard.
4. Seal the shipping container securely.
5. Mark the shipping container **FRAGILE** to encourage careful handling.
6. In any correspondence, refer to the instrument by its model number and its serial number.

Chapter 3

Generator Operation

3-1 Introduction

This chapter is divided into ten sections, of which Sections 3-4 to 3-10 are organized around the seven main Operating Pages of the 8180A/8180B Generator. Each main page is a starting point to other pages on which selections and entries can be made with the use of softkeys. The various softkeys are described using example settings.

Each section gives a full description of all the softkeys, allowed entries and setting ranges. Any restrictions and the likely error messages are also included.

3-2 Data Generator Block Diagram

In Figure 3-1 is the block diagram of a data generator. The generator can be driven by either an internal or external clock. The data memory provides a data depth of and 16384 bits for each channel in the case of the 8180B and 1024 bits for each channel in the case of the 8180A.

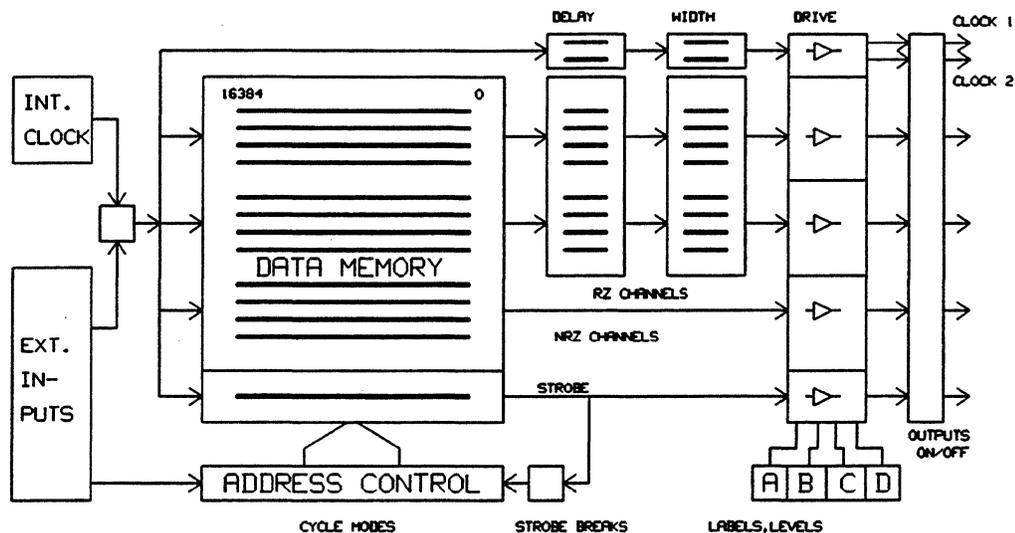


Figure 3-1. Block Diagram of the Data Generator

The block diagram shows a fully loaded generator containing eight non-return to zero (NRZ) channels and two blocks of four return to zero (RZ) channels, giving a maximum total of 16 channels. This particular configuration is obtained by adding two Options 002 (four RZ channels each) to the standard eight NRZ channels. A full description of the generator options is given in Chapter 1. Each RZ channel provides data with individually variable delay and width with respect to the strobe channel.

The block diagram also shows two clock channels Clock 1 and Clock 2 as well as a strobe channel. The clock outputs feature individual delay and width settings with respect to the strobe channel.

All channels (with the exception of the strobe channel) have variable output levels. Four different pairs of high and low levels can be set up and individually assigned to any of these channels.

3-3 Front Panel Controls and Operating Concept of User Interface

Before turning on the generator we should spend a moment on the instrument front panel layout and its operating concept. This section explains the main features of the generator front panel. Figure 3-2 shows the front panel controls.

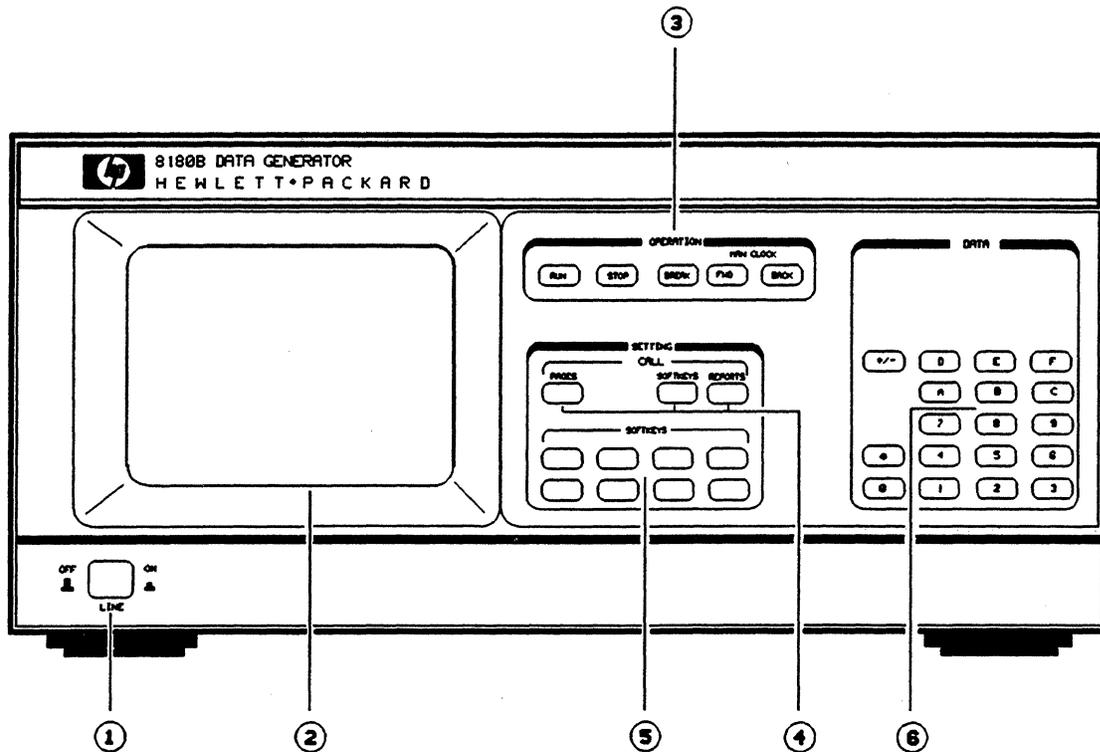


Figure 3-2. Data Generator Front Panel

1. Mains power ON/OFF pushbutton with ON indicator lamp.
2. CRT display. See below for Display Format.
3. OPERATION keys are used to run and stop the instrument and to step manually through the memory. They are explained in detail at the end of Section 3-4 'Control Page and Operating States'.
4. CALL keys are a sub-group consisting of the PAGES, SOFTKEYS and REPORTS keys. They are a part of a group called SETTING keys. The key PAGES permit a return to the main SELECT PAGE menu from any page or sub-page. The keys SOFTKEYS and REPORTS allow a mixed display as is explained later in chapters 3 and 4.
5. SOFTKEYS are a sub-group of eight keys used to set and modify all generator parameters. They are also part of a group called SETTING keys. The SOFTKEYS are discussed throughout this chapter.
6. DATA keys keys permit entry of front panel data in binary, octal, decimal or hexadecimal modes. They are also used for numeric value entry of measurement parameters such as frequency, delay, width, etc. Only those keys currently appropriate are enabled. This prevents making non-meaningful entries. The DATA keys are discussed throughout this chapter.

Front Panel Controls and Operating Concept of User Interface

Display Format

The display is divided into three areas. At the top is status information, at the bottom are the softkey labels (together with parameter entry information where appropriate), and the center part of the display, called the Report Area, is dedicated to generator settings or data. As an example, refer to Figure 3-3 showing the Control Page.

8180B		Status Address	STOP
CONTROL			
First Address	00000	Last Address	16383
Cycle Mode	AUTO	Strobe breaks	OFF
Clock Source	INTERNAL	Clock 1 in Break	OFF
Input Impedance	50 g	Run Input	OFF
Input Threshold	+0.0 V	Stop Input	OFF
		Break Input	OFF
Strobe Output	DATA	Outputs	ON
Select Further			
First Address	Last Address	Cycle Mode	Break Control
Clock Source	Inputs	Strobe Output	Outp on/off.

Figure 3-3. Example of the Display Format showing the Control Page

Page Concept

The operating concept of the generator is based on seven main menu pages accessible through softkeys. The main pages have other pages behind them which become available once a softkey selection is made, resulting in layered softkey menus. Figures 3-4 and 3-5 demonstrate this concept.

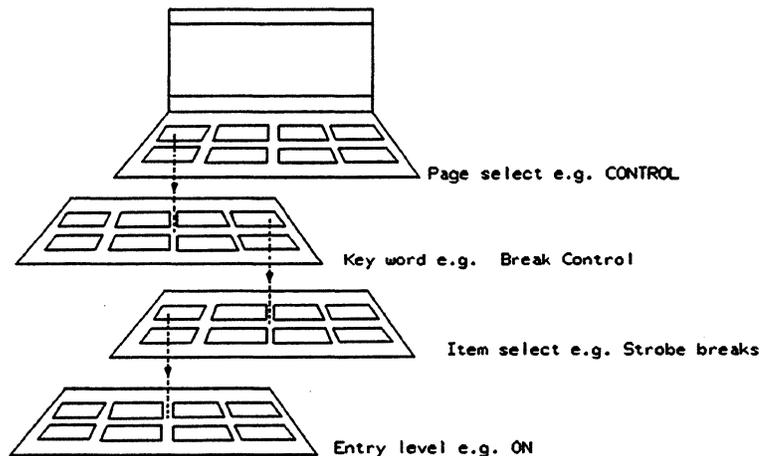


Figure 3-4. Softkey Operating Concept

Front Panel Controls and Operating Concept of User Interface

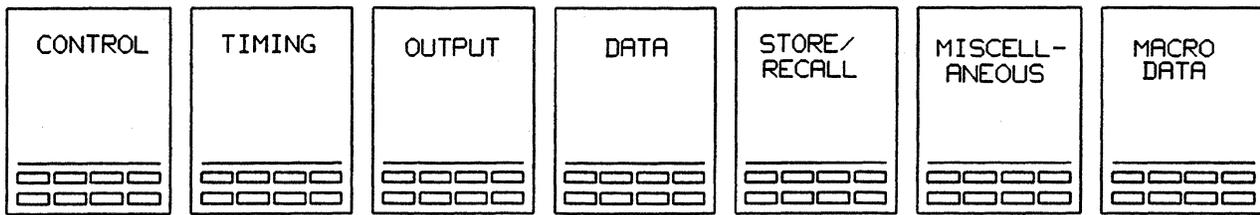


Figure 3-5. Generator Main Pages

The menu-driven operation is user oriented, and you will become familiar with it after a little practice. To get familiar with the operating concept, you should do the simple exercise on the operation of softkeys that follows in just a moment.

Switching On the Generator

Turn on the generator by pressing the ON/OFF button. The instrument always performs a power-up self test on switch-on lasting about five seconds, after which the main pages become available on the softkeys.

NOTE

If the power up self test detects a fault the generator displays the type of error on the screen and the softkeys remain blank except for the top left hand one - **CONTINUE**. If you press this key, operation of the generator resumes albeit with the fault present. The presence of a fault may or may not prevent you working with the generator. This depends on the nature of the fault. In any case you should refer to Section 2-2 of this manual.

On powering up the generator the outputs are always turned off. All other settings and data remain as they were prior to power down. Back-up batteries keep this information stored for approximately 1 week.

Exercise - Softkey Operation

- **STORE/RECALL**
- **Rcl Std Set**
- **EXECUTE**

The fastest way to bring the instrument to a known state is to call up the standard parameter set; this is what we will do next. Push the **STORE/RECALL** softkey. This brings up the corresponding display, and the softkeys now offer further selections. One option is **Rcl Std Set**. Once this softkey is pushed, the command must be confirmed by pressing **EXECUTE**. All parameters are now set to the values as listed in Table A-1 in Appendix A.

Front Panel Controls and Operating Concept of User Interface

NOTE

All screens in the subsequent sections showing main pages give values following the execution of the Recall Standard Set command.

Pushing the PAGES key returns you to the main PAGES menu.

Notice that softkeys which have additional level(s) of softkey menus behind them (not main page softkeys) are displayed in lower case letters. Softkeys which are at the lowest level, that is those performing actual functions are displayed in upper case letters. There are no additional softkey menus behind these keys.

Exercise

- PAGES
- **OUTPUT**
- **Outp on/off**
- **ON**

Next we will turn on the outputs. Call up the OUTPUT page (push the **OUTPUT** softkey). One of the softkey labels now says **Outp on/off**. Pushing the key displays the choice ON or OFF. If we push the **ON** key, the outputs will be turned on and the flashing message "OUTPUTS OFF" will disappear from the top of the screen.

These two examples which activate the standard settings and enable the outputs should show you how easy it is to operate the generator.

Next we'll go through all seven pages of the generator in detail. To start with, call up the highest decision level by pushing the PAGES key.

3-4 Control Page and Operating States

The first page is the Control Page. It provides access to the main control functions of the generator. Call up the Control Page by pressing **CONTROL**.

The softkey labels at the bottom of the display now indicate which parameters are accessible. Notice that the keywords in the report area, such as "First Address", also appear in the softkey area. The same principle operates on all menu pages.

Let us now go through the capabilities in detail. Figure 3-6 shows the functions of the generator which are accessible through the Control Page.

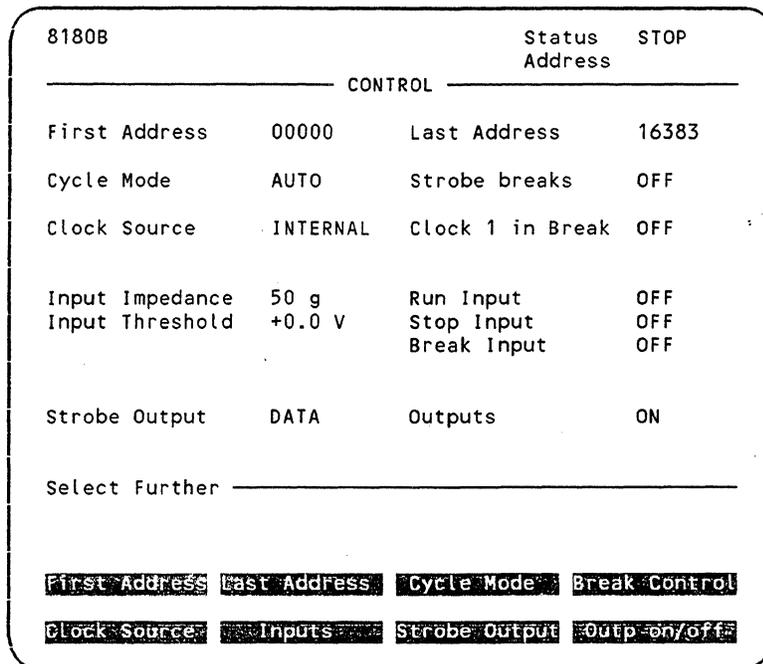


Figure 3-6. Control Page after Recall Standard Set

Address Control - First and Last Address

The first and last addresses determine which part of the generator's memory is to be output while the generator is running.

First Address allows entry of a desired first address value using either the DATA keys or the **INCREMENT** and **DECREMENT** softkeys. When using the DATA keys, you can either enter the full number (including leading zeros if applicable) or omit the leading zeros and terminate the entry by pressing **ENTER NUMBER**. The entry must be in the range as shown in the square brackets in line 22 of the display. If you've just recalled the Standard Set, then the address code will be decimal, the first address will be 00000 and the last address will be 16383 (1023). The address code can also be octal and hexadecimal. Changing the address code is discussed on the Data Page in Section 3-7.

Last Address allows entry of a desired last address value in the same way.

Later, when we get onto the DATA page, you will see that only the data between the first and the last addresses changes in response to data manipulation. A more detailed explanation will be given when we deal with this page.

Control Page and Operating States

Cycle Modes

The Cycle Mode determines the way the generator outputs data. Five different cycle modes are available. On pressing the **Cycle Mode** key the following choices are offered:



- AUTO

Data is repeatedly output from the first address (FAD) to the last address (LAD) until a STOP or BREAK signal is detected.
- SINGLE

Data is output once only, starting from the first and finishing with the last address. If started by an external signal (positive or negative edge - see Run Input) applied to the "RUN,GATED" input on the rear panel, the generator stops after it has reached the last address. In this mode the "RUN,GATED" input is edge sensitive. The generator outputs the next single sequence of data when triggered by the next edge, but only after the completion of the previous data sequence.
- GATED

Data output commences when a signal at the input "RUN,GATED" on the rear panel is true. Data is repeatedly output as in AUTO mode as long as the gating signal remains true. When this signal goes false, data is output through to the last address, and output ceases. The output can be programmed to sense a positive or a negative edge at a given threshold voltage. In this mode the RUN key is inoperative. Refer below to the softkey **Run Input** and also to 'Instrument Operating States' at the end of this section. There is an exercise at the end of this section to illustrate operation of the Gated Mode.
- INIT+AUTO

Causes the generator to output data from address 00000 to the first address once, and then cycle between the first and the last addresses.
- INIT+GATED

Similar to INIT+AUTO, except the cycle is triggered by a gating signal at the "RUN,GATED" input. The generator output will stop at the last address, after the gating signal goes false. In this mode the RUN key is inoperative. Refer below to the softkey **Run Input** and also to 'Instrument Operating States' at the end of this section.

The above cycle modes are illustrated in Figure 3-7.

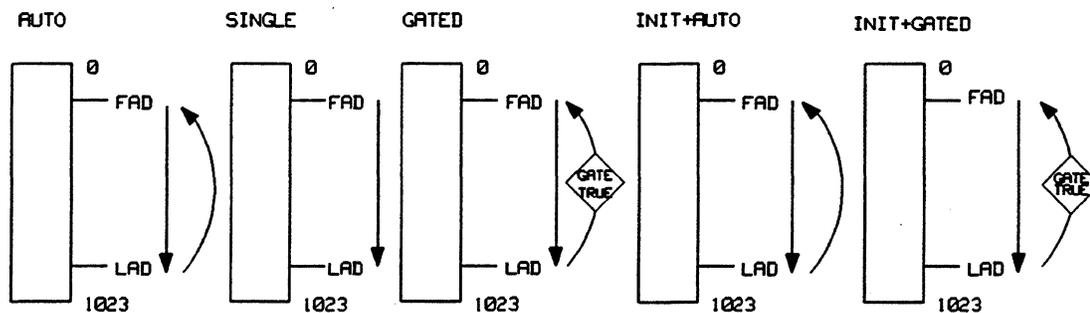


Figure 3-7. Available Cycle Modes

Control Page and Operating States

In cycle modes AUTO, SINGLE and INIT+AUTO the generator can be triggered into operation by pressing the RUN key or by a signal at the "RUN,GATED" input on the rear panel, provided this input is enabled. Refer below to the softkey **Run Input**.

Break Control

This facility allows you to specify how the generator will enter the BREAK state and what it will do once it is there. The **Break Control** softkey and the 'Strobe breaks' and 'Clock 1 in Break' entries in the Report area of the screen are not displayed and their functions cannot be used when the GATED or INIT+GATED cycle modes are selected. The **Break Control** key makes the following softkeys available:

Strobe breaks **Clk1 in Break** **EXIT** ↑

Strobe breaks **ON** indicates that a logic "1" in the strobe channel will put the generator into the BREAK state. The BREAK state can be entered from the front panel, programmed via the computer, or sent to the generator via the BREAK socket on the rear panel. Strobe breaks allows a simple way of causing the generator to enter the BREAK state *in synchronism* with the data stream.

There are a number of applications for this facility. For instance, when debugging in a particular section of the output data, you may wish to break its flow and use the manual clock keys to step through a certain address range in order to observe some logic sequences. Or you may be running a functional test on a device and want to perform a DC test at a certain address.

Note that when Strobe breaks is enabled, you cannot use the generator in AUTO or INIT+AUTO mode and use the strobe channel as a synchronizing or arming signal for the test device, the analyzer or some other piece of test equipment. The moment the generator accesses the address at which it finds a "1" in the strobe channel, it will enter the BREAK state.

Clk1 in Break **ON** indicates that the Clock 1 signal will keep running while the generator is in the BREAK state. Clock 2 remains unaffected. This feature is useful for some devices such as certain microprocessors which need to be kept clocked even when on hold.

Clock Source

The generator has its own internal clock, which can be set to any frequency between 1 Hz and 50 MHz. It can also accept an external clock at the "EXT CLK" input on the rear panel. The softkey **Clock Source** offers the following sources for the generator clock signal:

INTERNAL **EXTERNAL 1** **EXTERNAL 2** **MANUAL** **EXIT** ↑

INTERNAL Internal clock is used. The clock frequency is set on the Timing Page.

Control Page and Operating States

- EXTERNAL**  External clock is used. Generator triggers on the positive edge. The frequency range of the external clock may be 1 Hz to 50 MHz. Refer to the Section "Using External Clock" on the Timing Page.
- EXTERNAL**  External clock is used. Generator triggers on the negative edge. The frequency range of the external clock may be 1 Hz to 50 MHz. Refer to the Section "Using External Clock" on the Timing Page.
- MANUAL** Manual clocking is possible using the "MAN CLOCK" keys FWD and BACK on the front panel. These keys are operational only if selected as the Clock Source on this page. Then, each time the FWD or the BACK key is pressed, a clock pulse will be generated and the instrument will output the data at the next or the previous address respectively.

Inputs

The **Inputs** softkey allows you to set up the Clock input and to define the "BREAK", "RUN,GATED" and "STOP" inputs on the rear panel (refer to Figure 3-8). On pressing this key the following softkeys are made available to you:

Clock Source	Run Input	Stop Input	Break Input
Impedance	Threshold		EXIT 

Clock Source Identical to Clock Source above.

Run Input The generator can be remotely started (set to RUN mode) by an edge applied to the "RUN,GATED" input on its rear panel. You can disable this input by pressing the **OFF** key. You can enable this input and set it to sense a positive slope by pressing the **ON**  key, or a negative slope by pressing the **ON**  key. See 'Generator Operating States' at the end of this section. In absence of a signal applied to this input, the input level is zero volts. The exercise 'Gated Mode' at the end of this section illustrates the function of the Run Input.

Stop Input The generator can be remotely stopped (set to STOP mode) by an edge applied to the "STOP" input on its rear panel. You can disable this input by pressing the **OFF** key. You can enable this input and set it to sense a positive slope by pressing the **ON**  key, or a negative slope by pressing the **ON**  key. See 'Instrument Operating States' at the end of this section. In absence of a signal applied to this input, the input level is zero volts.

Break Input The generator can be remotely stopped (set to BREAK mode) by an edge applied to the "BREAK" input on its rear panel. You can disable this input by pressing the **OFF** key. You can enable this input and set it to sense a positive slope by pressing the **ON**  key, or a negative slope by pressing the **ON**  key. See 'Instrument Operating States' at the end of this Section. In absence of a signal applied to this input, the input level is zero volts. The **Break Input** softkey and the 'Break Input' entry in the Report area of the screen are not displayed and their functions cannot be used when the GATED or INIT+GATED cycle modes are selected. In these modes the 'RUN, GATED' input on the generator rear panel controls run state of the generator.

Control Page and Operating States

Impedance

Common to all inputs, this key permits setting their input impedance. You can select one of two impedances by pressing the **50 Ω** or the **100 kΩ** key.

Threshold

Common to all rear panel inputs, this key permits setting the input threshold voltage level. After entering the numerical value in volts in the range of +10 V to -10 V, you must press the **VOLET** key to terminate the entry. Alternatively you can use the **INCREMENT** or **DECREMENT** keys, which operate in 100 mV steps.

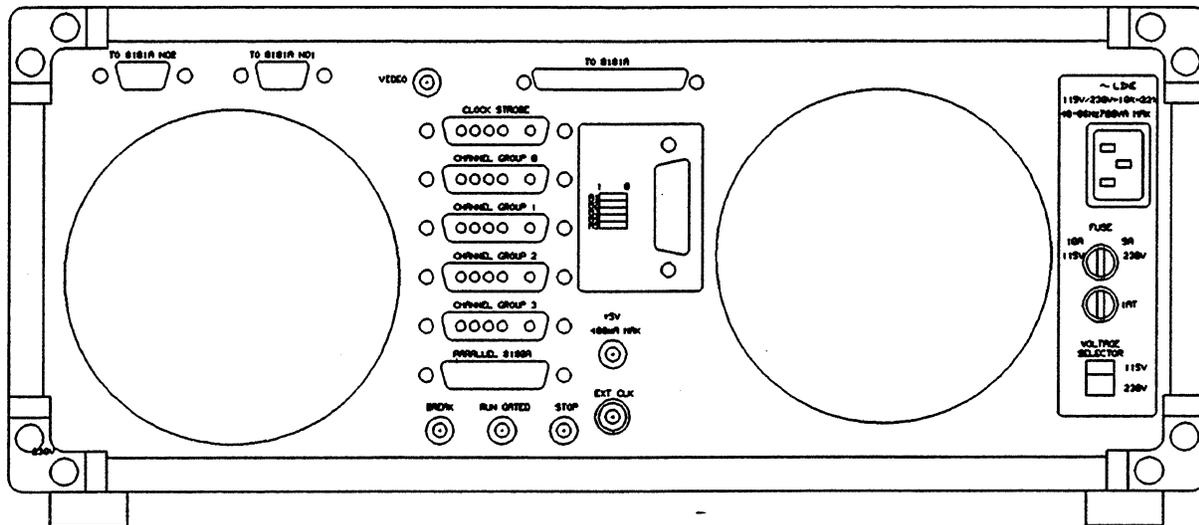


Figure 3-8. Generator Rear Panel

Strobe Output

The **Strobe Output** key offers the following choices:



DATA

When DATA mode is selected, the strobe output can be used as an additional NRZ channel - see Figure 3-9. This is the normal mode of operation, where the analyzer accepts this signal at its trigger input to synchronize with the generator. Setting the strobe channel in DATA mode is covered on the Data Page.

CLOCK

When CLOCK mode is selected, the strobe output becomes the reference clock output - see Figure 3-9. This extra clocking channel of narrow pulse width (approximately 8 ns) and at zero delay can be used to clock external devices such as scopes, counters etc. It is also useful for setting-up purposes, for example to measure channel timing skew.

Control Page and Operating States

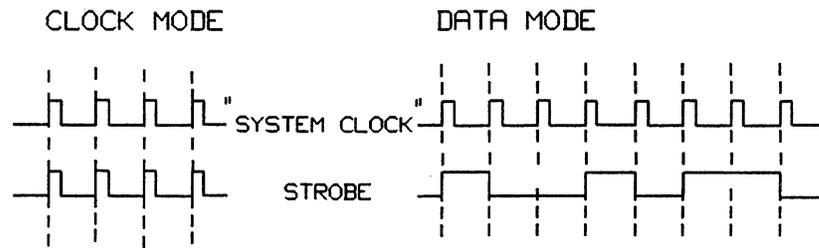


Figure 3-9. Strobe Channel Modes

Output Enable

Via the **Outp on/off** key you can switch all the generator outputs on or off. These are the CLK1, CLK2 and STROBE channels, as well as all called up DATA channels. (For a definition of called up data channels see the Data Page.) All outputs are off until enabled. The choices are as follows:

- OFF** All outputs are turned off (i.e. set to high impedance).
- ON** All outputs are turned on.

Generator Operating States

The 8180B has three operating states - RUN, STOP and BREAK. They can be initiated either via the corresponding front panel keys, external control inputs or remotely via the Hewlett-Packard Interface Bus (HP-IB). For a description of the instrument states when operating under program control via HP-IB refer to Chapter 7. The operating states are valid for all cycle modes except under the following GATED cycle mode conditions:

- In either of the GATED modes, irrespective of clock source, all BREAK related functions are disabled, disappearing from the screen. Also, the front panel RUN key is disabled. Only the STOP key is active.
- In either of the GATED modes, if the clock source is MANUAL, only the STOP and FWD keys are active. The MANUAL clock is enabled by the external RUN signal going true and disabled by the front panel STOP key or by the external RUN signal going false.

RUN: Data output (generation) active. When RUN is initiated after stop, data generation begins from the **First Address**. (If in the "INIT+GATED" or "INIT+AUTO" mode, it begins from **Address zero**.) In MANUAL clock mode only the FWD key is operative.

The RUN state occurs after:

- pressing the RUN key
- an external RUN signal is detected

STOP: data generation stops with the last word's NRZ data remaining at the outputs, and the RZ data returning to logic false after the programmed delay and width. Logic false is always zero as displayed on the Data Page, which normally means low at the generator outputs. This can however be inverted by using the Complement function. This function will be discussed later on when we get to Data Channel Labeling on the Output Page.

Control Page and Operating States

The STOP state is entered after:

- power on
- pressing the STOP key
- an external STOP signal
- at end of a SINGLE cycle
- at end of a GATED cycle

BREAK: as for STOP except that when RUN is initiated after BREAK, data generation begins from the current address, (this can have been changed via the MAN CLOCK FWD or BACK keys). If the FWD or BACK keys are operated in BREAK then data at the outputs will change.

The BREAK state occurs after:

- pressing the BREAK key
- an external BREAK signal is detected
- an internal BREAK from the STROBE channel. This happens if the Strobe breaks condition has been enabled and a "1" is encountered in the STROBE channel.

The operating states are graphically summarized in Figure 3-10.

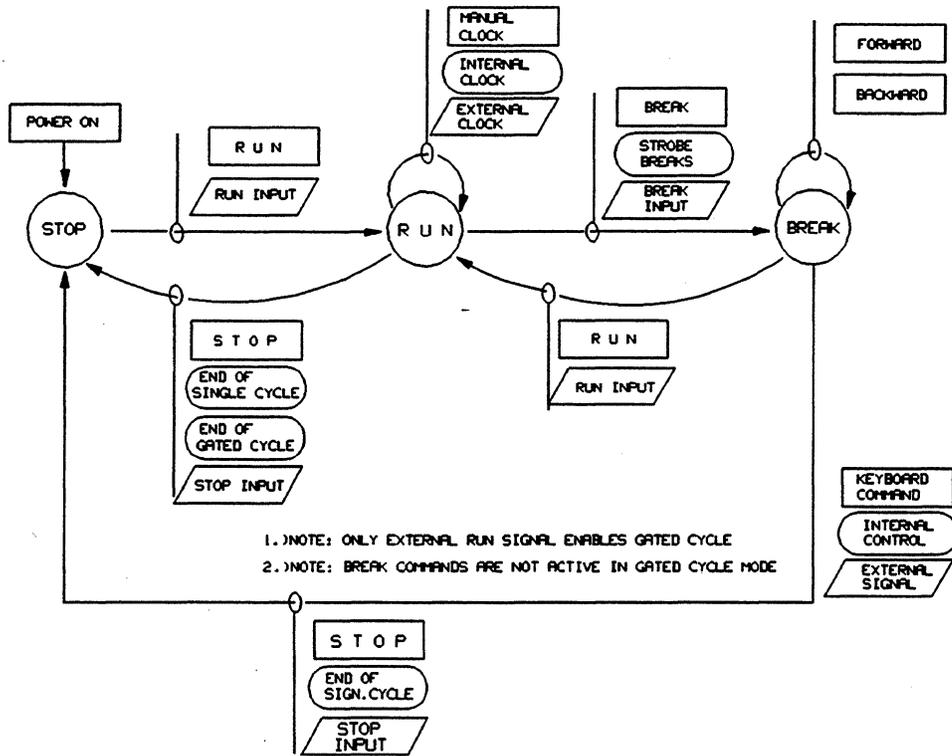


Figure 3-10. Generator Operating States

Exercise - Addresses, Cycle Mode

1. Set the generator, so that it outputs 128 words once and then stops at word address 256. The generator should run on its internal clock.
2. Next, set it to continuously output the data contents.
(Disregard other settings, e.g., clock rate and data, at this time.)

Required settings:

Control Page and Operating States

First address: 128
Last Address: 256
Cycle mode: A) Single
 B) Auto

Exercise - Gated Mode

Set the generator so that its Operating State is controlled by the "RUN,GATED" input on the rear panel.

Required settings for initial conditions:

First address: 00000
Last address: 16383 (1023)
Cycle mode: GATED
Run Input: ON ✓
Input Threshold: +0.0 V

In the absence of a signal at the "RUN,GATED" input, the input level remains at zero volts. To simulate an external signal at this input, we make use of the Input Threshold function. On the Threshold menu press the **DECREMENT** key to bring the threshold down to -0.1 V. Alternatively, you can directly enter some negative value into the Input Threshold inverse video field. The generator will go into the RUN state. In the top right hand corner of the display the Status is RUN. The Address is now sweeping through the entire address range of the generator, although this may be too fast to see, depending on the clock frequency.

There are two ways to stop the generator. One is to press the STOP key (second from left among the OPERATION keys). This is an asynchronous STOP. The generator stops at whatever address you happen to press the STOP key. The other way is to press the **INCREMENT** key on the Threshold menu to bring the threshold level to a positive value. You can also enter in a positive value for the threshold. This is a synchronized STOP. The generator will run to the Last Address, in our case 16383 (1023) and then stop.

Note that you cannot restart the generator with the RUN key. You can also not use the BREAK key. They are both disabled in the GATED mode.

Error Messages

The generator monitors the entries you make and will return an error message if any of them are incorrect. Here is a list of error messages that can be received as a result of incorrect entries on the Control Page.

VALUE OUT OF RANGE This flashing inverse video message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable to First Address, Last Address and Input Threshold entries. If you exit the page where you made such an entry, it will be ignored and the previous valid entry will be retained.

Run Input Off This flashing message appears if you have selected a Gated or Init+Gated cycle mode, but forgotten to enable one of the two Run Inputs. The message appears in the center of line 1 (top of the screen).

Outputs Off This flashing message is a warning rather than an error message. It tells you that generator outputs have not been switched on. This is the default

Control Page and Operating States

condition after instrument switch-on. The message appears in the same place as the previous message "Run Input Off". If the previous error condition is true, its message has priority and is shown.

Apart from incorrect entries which are flagged as such by the generator, it is possible to make other erroneous entries which, although syntactically correct, will not make the generator do what you want it to. If you experience such a problem the Control Page setup is usually the cause. Therefore always check that the settings on this page are correct.

3-5 Timing Page

The second page is the Timing Page. It provides access to Frequency, Period, Clock Timing and Channel Timing. It also allows the channels installed in HP 8181A/B extender units to be delayed in common (when present). Control of the extender units is covered separately in Chapter 5. Before we go on to the individual Timing Page functions it will be of benefit to mention the generator data formats.

Data Formats

Performing parametric digital hardware analysis requires RZ (Return to Zero), NRZ (Not Return to Zero) and DNRZ (Delayed Non Return to Zero) formats as shown in Figure 3-11. Let us briefly review these formats.

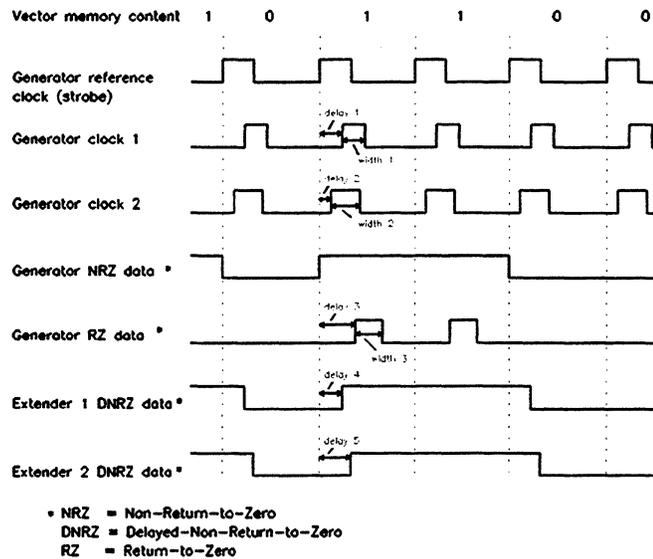


Figure 3-11. Supported Data Formats

NRZ channel data

The width of an NRZ data bit is identical to the clock period. The only timing information associated with NRZ data is the number of clock periods for which the data is true or false. Every HP 8180A/B Data Generator contains at least eight channels supporting this format.

RZ channel data

The width of an RZ data bit is shorter than the clock period and is variable. Therefore, a transitions always occurs between consecutive true bits. In addition, the RZ channels can be delayed individually or together with respect to the reference clock. Such channels are supplied under Option 002. An HP 8180B Data Generator can have a maximum of eight RZ channels installed (that is, 2 x Opt. 002).

DNRZ channel data

The width of a DNRZ data bit is identical to the clock period. However, its delay with respect to the reference clock is variable. There are two occasions when NRZ channels are strictly speaking DNRZ channels:

1. When installed RZ channels are set to NRZ. The delay can be varied individually for each channel, or for all channels in common.

Timing Page

- When the delay feature of NRZ data channels in each HP 8181A/B Data Generator Extender is used. The extender can contain only NRZ channels (ranging in number from 8 to 24) and all of them can be delayed in common. This is useful, for example, in simulating buses.

It is important to note that although the channels behave in both cases as DNRZ channels, they are still called up on the generator as NRZ channels.

Since delay and width are both timing variables, RZ channels are also known as timing channels. RZ channels are used when the logic state of a data line must change state at a specific point in time and remain in that state for a specific time interval. For example, consider waveform diagrams commonly used in IC data sheets. Address, data, and control lines all require specific data bit timing sequences relative to each other in order that the IC can function correctly.

8180B		TIMING		Status	STOP
				Address	
Clock Frequency	10.0 MHz	Clock Period	100. ns		
	Delay	Format	Width		
Clock 1	00.0 ns	RZ	40.0 ns		
Clock 2	50.0 ns	RZ	10.0 ns		
Channel 0-0	00.0 ns	NRZ			
Channel 0-1	00.0 ns	NRZ			
Channel 0-2	00.0 ns	NRZ			
Channel 0-3	00.0 ns	NRZ			
Select Further _____					
Frequency	Period	Clock Timing	Chnl Timing		

Figure 3-12. Timing Page

Call up the Timing Page now by pressing PAGES and **TIMING**. Figure 3-12 shows the Timing Page and the functions of the generator which are accessible via softkeys through this page. Let us now go through the functions in detail.

Frequency

The **Frequency** key allows you to set the rate of the internal master clock. On pressing this key a choice of **INCREMENT** or **DECREMENT** is offered. By means of these keys you can modify the current frequency displayed in the inverse video field in line 22 of the display, just above the softkeys. Alternatively, you can enter the frequency directly into this field, using the DATA keys. If you choose the second method, you must terminate your entry by pressing one of the **HERTZ**, **KILOHERTZ** or **MEGAHERTZ** keys which subsequently appear. The clock frequency range available (1 Hz - 50 MHz) is displayed in the square brackets just above the softkey labels, but refer to 'Error Messages' below for additional information. Changes to the Clock Frequency will also be displayed as corresponding changes in the Clock Period field in line 4 and vice

Timing Page

versa.

Period

If preferred, the period, rather than the frequency of the internal master clock can be set. The procedure is identical to that for frequency. The clock period range is 20.0 ns - 999 ms.

Clock Timing

There are two clock channels with RZ format capability. They can be used as required to clock the device under test as well as to clock the analyzer in a test set-up. There is nothing to stop you using one or more RZ data channels as additional clock channels. From the timing point of view they are identical. The advantage of the clock channels is, however, that their output levels can be set independently of the data channels. This is covered on the Output Page. Also, as detailed on the Control Page, Clock 1 can be set to run even when the instrument is in the Break state.

On pressing the key **Clock Timing** the following softkeys are presented for selection:

```
Clock 1 Delay  Clock1 Format  Clock 1 Width  [REDACTED]
Clock 2 Delay  Clock2 Format  Clock 2 Width  [EXIT] [↑]
```

Clock 1 Delay allows you to enter a delay for the Clock 1 channel by using the **INCREMENT** and **DECREMENT** keys, or directly, using the DATA keys. If you make a direct entry using the DATA keys, the additional scaling keys **MILLISEC**, **MICROSEC** and **NANOSEC** will appear. You must terminate your direct entry by pressing one of these keys. The delay range available (0.0 ns - 999 ms) is displayed in the square brackets in line 22 of the display, just above the softkey labels, but refer to 'Error Messages' at the end of this section for additional information.

Clock1 Format allows the selection of a variable width signal by pressing the **RZ** key, or a fixed 50% mark-space ratio signal by pressing the **RZ=50%** key.

Clock 1 Width allows the entry of a width for the Clock 1 channel by using the **INCREMENT** and **DECREMENT** keys, or directly, using the DATA keys. This is possible only when the selected format is RZ and the **Clock 1 Width** key is displayed. If you make a direct entry from the DATA keys, additional scaling keys **MILLISEC**, **MICROSEC** and **NANOSEC** will appear. You must terminate your direct entry by pressing one of these keys. The delay range available (10.0 ns - 999 ms) is displayed in the square brackets just above the softkey labels, but refer to 'Error Messages' at the end of this section for additional information.

Clock 2 Delay operates in the same way as for Clock 1 delay.

Clock2 Format operates in the same way as for Clock 1 format.

Clock 2 Width operates in the same way as for Clock 1 width.

Timing Page

Data Channel Timing

On pressing the key **Chnl. Timing**, the following softkeys are presented for selection:

Delay **Format** **Width** **EXIT**
All Ch Delay **All Ch Format** **All Ch Width** **EXIT** ↑

Note that if you have previously recalled Standard Set the softkeys **Width** and **All Ch Width** will not be displayed. See the explanation given with the softkey descriptions.

Delay

allows setting the delay of individual data channels by using the **INCREMENT** and **DECREMENT** keys, or directly, by using the DATA keys. If you make a direct entry from the DATA keys, additional scaling keys **MILLISEC**, **MICROSEC** and **NANOSEC** will appear. You must terminate your direct entry by pressing one of these keys. The delay range available (0.0 ns - 999 ms) is displayed in the square brackets just above the softkey labels, but refer to 'Error Messages' below for additional information. The **Prev Channel** and **Next Channel** keys take you through the installed RZ data channels, so you can modify the delay of any particular channel at will.

Format

allows the selection of a variable width signal by pressing the **RZ** key, a fixed 50% mark-space ratio signal by pressing the **RZ=50%** key or an NRZ format (strictly speaking DNRZ) by pressing the **NRZ** key. The **Prev Channel** and **Next Channel** keys take you through the installed RZ data channels, so you can modify the format of any particular data channel at will.

Width

allows setting of the width of individual data channels by using the **INCREMENT** and **DECREMENT** keys, or directly, using the DATA keys. This is possible only when the selected format is RZ and the **Width** key is displayed. If you make a direct entry from the DATA keys, additional scaling keys **MILLISEC**, **MICROSEC** and **NANOSEC** will appear. The delay range available (10.0 ns - 999 ms) is displayed in the square brackets just above the softkey labels, but refer to 'Error Messages' at the end of this section for additional information. The **Prev Channel** and **Next Channel** keys take you through those installed RZ data channels which are currently set to the RZ format, so you can modify the width of any of those channels at will.

All Ch Delay

operates in the same way as for individual channel delay, except that all installed RZ channels are affected. The **INCREMENT** and **DECREMENT** keys appear only after a direct entry has been made.

All Ch Format

operates in the same way as for individual channel format, except that all installed RZ channels are affected.

All Ch Width

operates in the same way as for individual channel width, except that all installed RZ channels which are currently set to the RZ format are affected. The **INCREMENT** and **DECREMENT** keys appear only after a direct entry has been made.

Timing Page

Use of External Clock

The generator can be driven by an external clock of desired. The selection of the external clock has been covered in Clock Source on the Control Page. When using external clock, bear the following points in mind:

1. The frequency of the external clock must lie in the range of 1 Hz - 50 MHz. Refer to Error Messages at the end of this section.
2. The displayed value for the generator clock frequency pertains always to the internal clock, regardless of whether it is selected or not.
3. Any programmed clock/data delays or widths act upon the external clock when this is selected. However, any timing incompatibilities between clock frequency and programmed delays or widths, and any error messages resulting thereof are based upon the internal clock.
4. The fixed 50% mark-space ratio format for Clock 1, Clock 2 and the RZ data channels is always derived from the internal clock, whether this is used or not. No warning is given if the external clock runs faster than the de-selected internal clock. If this happens, some clock pulses or data bits will be lost. It is up to you to monitor the two values, and set the internal clock value accordingly.

Exercise - Clock and Channel Timing

Set up the following conditions:

Clock Frequency 5 MHz

1. Clock 1 Delay: 15 ns
Clock 1 Format: RZ
Clock 1 Width: 10 ns
2. Clock 2 Delay: 0 ns
Clock 2 Format: RZ
Clock 2 Width: 80 ns
3. Channels 0-0 to 0-3 to RZ
All Channels Delay: 10 ns
All Channels Width: 60 ns

Exercise - Cycle Boundary Crossing

Using the generators variable delay and width capabilities, a data signal (bit) can be programmed into the next clock cycle. The limit value for the delay is 90% of set period - 18 ns, and for the width 90% of set period - 8 ns. Taking for example a clock period of 100 ns, the resulting output waveform from a channel set to these limit values would be as shown in Figure 3-13.

Timing Page

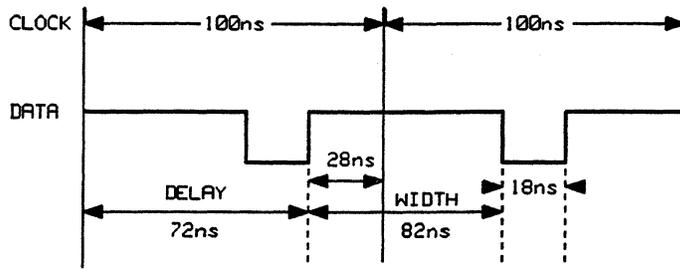


Figure 3-13. Cycle Boundary Crossing Example

Exercise - Increasing Relative Timing Resolution

The timing requirements on the diagram in Figure 3-14 appear to go beyond the capabilities of the generator. We only have three digits of resolution and we need four to set up a channel delay of 475.5 us.

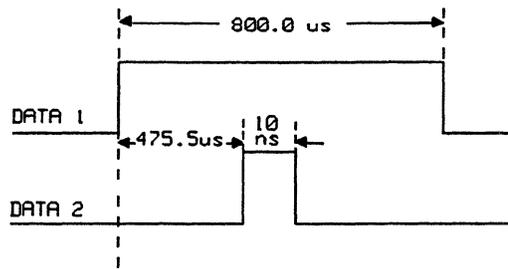
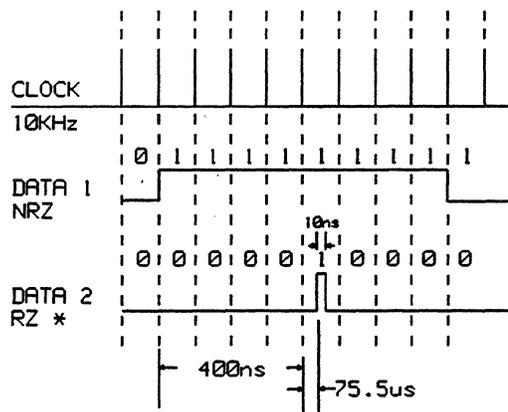


Figure 3-14. Required Timing Resolution

Additional resolution can be obtained at the expense of memory depth. We set the generator's clock to 10 kHz (period = 100 us) and set one channel to the NRZ format. Next, we use eight bits at the set clock period to generate a pulse 800 us wide. We have thus created the signal DATA 1, shown in the diagram in Figure 3-15.

For the signal DATA 2 we set another channel to the RZ format with a width of 10 ns and a delay of 75.5 us. We then set seven of the eight bits (bits 1 to 4 and 6 to 8) to zero and bit 5 to one, as shown in the diagram in Figure 3-15.



* DELAY 75.5us
WIDTH 10ns

Figure 3-15. Relative Timing Resolution versus Memory Depth

Timing Page

When considering an approach such as this one, it is important to bear in mind the overall accuracy of the generator, which is +/-5% of programmed value +/-1 ns.

Error Messages

The generator monitors the entries you make and will return an error message if any of them are incorrect. Here is a list of error messages that can be displayed as a result of incorrect entries on the Timing Page.

VALUE OUT OF RANGE This inverse video flashing message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable to Frequency, Period, any of the clock or data delays and any of the clock or data widths. After exiting the page where you made such an entry, the instrument will return to the previously set value.

E A flashing letter E will appear next to any variables whose settings have become incompatible with each other as a result of entering a false value. This applies to any (or all) of the channel delays or widths which become incompatible with the set period (or frequency), or vice versa. The error warning "E" appears when the delay exceeds (90% of the period - 18 ns), or when the width exceeds (90% of the period - 8 ns).

Assume for instance, that you have entered a clock period of 500 ns followed by a Clock 1 width of 443 ns. The error warning "E" appears by the settings for the frequency, period, Clock 1 width and the inverse video entry field for Clock 1 width.

TIMING This flashing message is triggered by an incompatible timing entry, which we have just covered previously, and appears in line 2 of the display on all pages and sub-pages, serving as a reminder of the error condition.

The generator cannot be seriously used when this error condition prevails, as channel timing can no longer be guaranteed.

CLOCK This inverse video flashing message is triggered by an external clock running faster than 50 MHz, and appears in line 2 of the display on all pages and sub-pages, serving as a reminder of the error condition.

The generator cannot be seriously used when this error condition prevails, as correct timing can no longer be guaranteed.

3-6 Output Page

The third page is the "Output Page". It provides access to functions such as output enable, output levels, output impedance, channel configuration, etc. Before we go on to the individual Output Page functions let us briefly discuss the relationship between output impedance and output level.

Output Impedance / Level Interaction

The generator can be programmed to drive a 50 Ohm load or a high impedance load (greater than 10 kOhm). To match the load impedance the generator does not switch its own output impedance. That remains fixed at 50 Ohm. Rather, it adjusts the output voltage level according to the output impedance selected in order to deliver the correct voltage to the load. Therefore, as long as the load impedance matches the programmed impedance, the actual level at the load will match the programmed level.

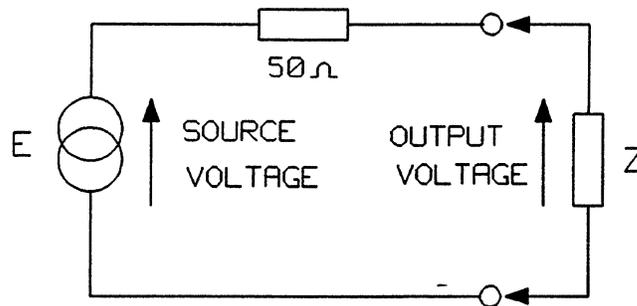


Figure 3-16. Equivalent of the Generator Output Stage

The output stage of the generator can be equated to a voltage source "E" in series with a 50 Ohm resistance, as shown in Figure 3-16. Across this is connected the actual output load "Z". Assuming that we have programmed an output level of 5 V, then the source and output voltages for the two programmed output impedances and the two load impedances are as in Table 3-1.

Table 3-1. Generator Output Voltages and Impedances (Set Voltage Level is 5V)

PROGRAMMED IMPEDANCE	LOAD IMPEDANCE	SOURCE VOLTAGE	OUTPUT VOLTAGE
50 Ohm	50 Ohm	10 V	5 V
50 Ohm	OPEN	10 V	10 V
OPEN	OPEN	5 V	5 V
OPEN	50 Ohm	5 V	2.5 V

Operation of the generator under conditions given by the last case in Table 3-1 is not recommended and the output level is not guaranteed.

Call up the Output Page now by pressing PAGES and **OUTPUT**.

Figure 3-17 shows the Output Page and the functions of the generator which are now accessible via softkeys through this page. Let us now go through the functions in detail.

COMMENT: this document is called DICESCRN.PUB.MKTPROM

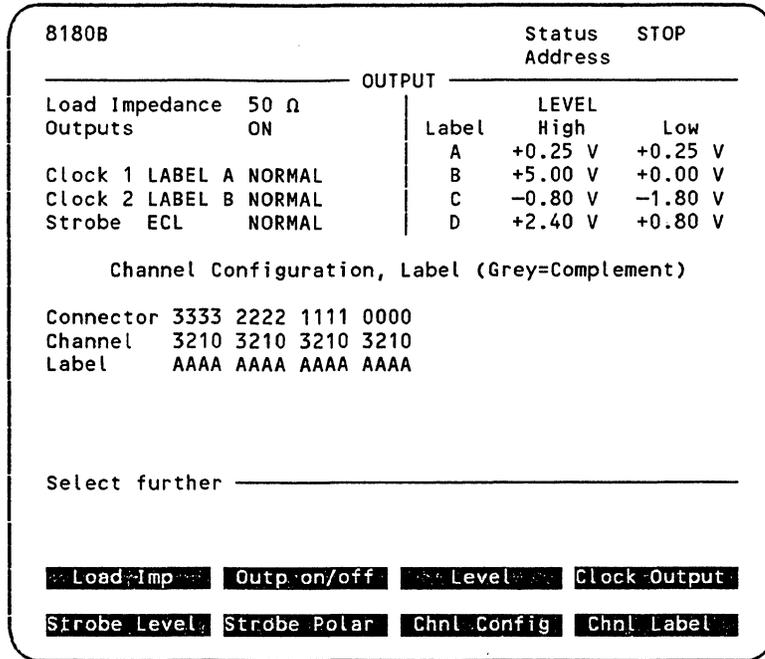


Figure 3-17. Output Page after Recall Standard Set

Load Impedance

The softkey offers two possibilities: 50 Ohms and a high impedance. Make your selection by pressing the softkey or .

Output Enable

Via the key you can switch all the outputs on or off. These are the CLK1, CLK2 and STROBE channels, as well as all called up DATA channels. (For a definition of called up data channels see the Data Page.) All outputs are off until enabled. The choices are as follows:

- All outputs are turned on.
- All outputs are turned off. The generator outputs will always be off after switch-on or after a reset. (Reset may occur while connecting an extender. Refer to the section on the generator extender.)

Output Level Capabilities

The generator can work simultaneously with up to four different high and low voltage level pairs. Each pair has a label in the form of a letter. Thus, there are four programmable voltage level pairs labeled A, B, C and D. Any of the labels can be associated with any of the installed data channels. The maximum and minimum voltage levels, the maximum and minimum voltage swing and the resolution depend on whether the generator is working into a 50 Ohm or an open (high impedance) load. These parameters are summarized in Table 3-2.

Table 3-2. Summary of generator output level capabilities

IMPEDANCE = 50 OHM					IMPEDANCE = OPEN				
Max. Level	Min. Level	Max. Swing	Min. Swing	Resolution	Max. Level	Min. Level	Max. Swing	Min. Swing	Resolution
5.5 V	-2 V	5.5 V	0.5 V	10 mV	17 V	-2 V	17 V	1 V	20 mV

On pressing the softkey **Level** the following softkey menu appears.

```

INCREMENT  Next Label  Low ↔ High  EXIT
DECREMENT TTL LEVELS  ECL LEVELS  EXIT ↑

```

Notice that you also get some additional information just above the softkeys in line 22 of the display. You get the label that you are currently accessing, the level of that label (high or low) and the allowed voltage range for that level. The allowed voltage range depends on whether you have set the output impedance to 50 Ohms or "open". In the inverse video field further to the right you get the actual voltage level value of the label you are currently accessing.

So, for instance after performing "Recall Standard Set" (we did that in Section 3-3) you will get the following information: Label A High Level [-1.5V +5.5V]. The current voltage for the label A high level, which in this case is +0.25 V is repeated in the inverse video field.

You can now directly enter the new value for the voltage level and label displayed using the data keys. You have to terminate your entry by pushing the **VOLT** key, which now appears.

- INCREMENT** allows incrementing the currently displayed value in the inverse video field.
- DECREMENT** allows decrementing the currently displayed value in the inverse video field.
- Next Label** allows you to step through the four labels A to D. You always step in the forward direction, going back to A after reaching D. Notice that the current label in line 22 changes as you press this softkey.
- Low ↔ High** toggles between the high and low level for the particular label you are currently accessing. The allowed voltage range also changes to correspond to the level you select.
- TTL LEVELS** allows you to set a label to TTL levels directly, without having to use the DATA keys. You step to the desired label with the **Next Label** key and press the **TTL LEVELS** key. The selected label appears in line 22 of the display, just above the softkeys - for example: Label B TTL. You then have to give an acknowledgment of your entry by pressing **EXECUTE**. If you've made a mistake, you can leave the menu by pressing **REFUSE** or **Exit** ↑. TTL levels are 2.40 V and 0.20 V for high and low level respectively.
- ECL LEVELS** allows you to set a label to ECL levels. The procedure is the same as for TTL levels. Note however, that ECL levels cannot be entered when load impedance is set to open. The **ECL LEVELS** softkey is not displayed. ECL levels are -0.80 V and -1.70 V for high and low level respectively.

Clock Output

The two clock channels also use the labels A to D in the same way as the data channels. The **Clock Output** key allows you to assign labels to the clock channels. On pressing this key the following softkey menu appears.

```

Clock 1 Label  Clock 1 Polar  [ ] [ ]
Clock 2 Label  Clock 2 Polar  [ ] [EXIT] [↑]
    
```

Clock 1 Label

allows you to assign a label to Clock 1. You get a choice of four keys:

```

[LABEL A] [LABEL B] [LABEL C] and [LABEL D]
    
```

Line 22 tells you which clock channel you are modifying and the label currently in use (in inverse video field). Having made your label selection you must use the **EXIT** **↑** key to get back to the previous menu.

Clock 2 Label

allows you to assign a label to Clock 2. Its operation is identical to that of Clock 1.

Clock 1 Polar

allows you to set the polarity of Clock 1. A choice of **NORMAL** or **COMPLEMENT** is offered. In the normal mode the low level means "false" and the high level means "true". In the complement mode it is the other way round. Line 22 tells you which clock channel you are modifying and the polarity currently in use (in inverse video field). Having made your polarity selection you must use the **EXIT** **↑** key to get back to the previous menu.

Clock 2 Polar

allows you to set the polarity of Clock 2. Its operation is identical to that of Clock 1 polarity.

Strobe Level

The strobe channel does not use labels to determine its high and low voltage levels. It can only be assigned TTL or ECL logic levels. The strobe channel is an additional channel that can be used for applications such as measuring equipment triggering or signal qualification. It is not a full clock or data channel. On pressing the softkey **Strobe Level** the softkey menu below appears.

```

[TTL] [ECL] [ ] [ ]
[ ] [ ] [ ] [EXIT] [↑]
    
```

Select the required logic level by pressing the appropriate softkey. Having made your selection use the **EXIT** **↑** key to return to the previous menu. Note that after a Recall Standard Set the default is ECL.

Strobe Polarity

You can set the polarity of the strobe channel in the same way you have set the polarity of the clock channels. The key **Strobe Polar** Calls the softkey menu below.

```

[NORMAL] [COMPLEMENT] [ ] [ ]
[ ] [ ] [ ] [EXIT] [↑]
    
```

A choice of **NORMAL** or **COMPLEMENT** is offered. In the normal mode the low level means "false" and the high level means "true". In the complement mode it is the other way round. Line

Output Page

22 shows you the polarity currently in use (in inverse video field). Having made your polarity selection use the **EXIT** **↑** key to get back to the previous menu.

Channel Configuration - Output Page

The lower part of the report area shows the current channel configuration. If you have just performed "Recall Standard Set", and assuming that you have the full complement of 16 data channels installed and no HP 8181B extender is connected, you will see sixteen channels arranged in four columns of four channels each. This configuration is shown in Figure 3-17. Each column represents one 4-bit word, or one 4-bit "segment". It is important to differentiate between segments and connectors. In our case it happens that a segment corresponds to a connector on the rear panel of the generator. This is because we have recalled Standard Set. However, a segment does not have to be associated with any particular connector, connectors, or even part/s of a connector, as we are just about to see. The choice is entirely up to you. The segments are numbered from left to right starting at 1, thus in our example the leftmost segment is the 1st segment and the rightmost one is the 4th segment.

The connectors are labeled from 0 upwards and after a Recall Standard Set are displayed on the screen from right to left. The channels within each connector are labeled 0 to 3 and after a Recall Standard Set are also displayed from right to left. The channel numbering tells you where a particular channel *physically* comes out at the generator rear panel. Thus in the current display for example, see Figure 3-17, the third channel from the right is called 0-2 and comes out on connector 0 cable 2, labeled yellow. The seventh channel from the left is called 2-1 and comes out on connector 2 cable 1, labeled red. The least significant channel is 0-0 and comes out on connector 0 cable 0, labeled black. And the most significant channel is 3-3 and comes out on connector 3 cable 3, labeled blue. The color labels are attached to the free ends of each split cable and are supplemented with cable numbers.

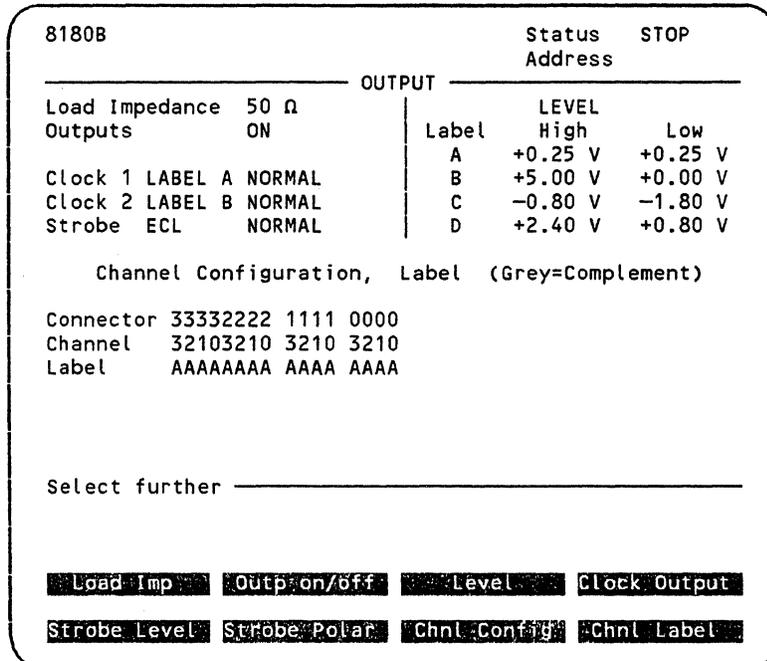


Figure 3-18. Output Page Displaying one 8-bit and two 4-bit segments

Using the **Chnl Config** key you can change the way the channels, or rather the parallel data bits on the screen are arranged. You may for instance be working with an 8-bit device. You will then want to have an 8-bit word on the screen, which also arranges your data in 8-bit words on the Data Page. In

Output Page

other words, you will want to see an 8-bit segment, as is shown in Figure 3-18. This does not change the connections at the rear panel of the generator, you will still most likely be using the same two 4-channel connectors as before. However, it does allow you to view and to work with the eight bits as a complete word. This is useful, for instance, when you want to set up an 8-bit up- or down-counter, as we shall see on the Data Page.

The **Chnl Config** function also allows you to mix the channels on the screen by selecting them from different connectors and arrange them into segments (data busses) of varying sizes. It is important to note, that in such a case the bus arrangement made up of physical channels at the rear panel of the generator must correspond to the bus arrangement on the screen.

The maximum segment size (maximum size a word can have on the screen) is 16. This maximum segment size by no means prevents you setting up a larger physical data bus, for instance one of 32 bits. The segment size of 16 bits ensures however that a reasonably clear overview of the channels within a segment is available. By connecting one or two extenders to the generator, it is possible to build up a physical bus of up to 64 channels. This figure can be further increased by stacking up several generators (with extenders), as is normally the case when operating large systems.

On pressing the **Chnl Config** key the following softkey menu appears.

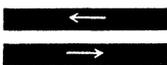
INSERT CHNL	DELETE CHNL	←	→
INSERT SEGMENT	Std Config	Code/Entry	EXIT ↑

Notice that several other changes also take place. Channel 3-3 is now displayed in inverse video. This inverse video field is the channel cursor that shows you which channel you are currently accessing. The segment which contains the channel currently being accessed is also repeated in the softkey label area in lines 22 and 23 together with the channel cursor.

The channel cursor allows you to make a **Direct Channel Entry** into the highlighted position. Simply use the DATA keys to enter the new connector number followed by the channel number. In effect you are making a substitution. Let's assume we want to replace the channel 3-3 with the channel 0-1. Simply type over the old entry using the DATA keys. The cursor moves automatically to the next channel on the right. The cursor remains stationary only when you have reached the rightmost channel, in our example channel 0-0.

All the displayed channels can be redefined in this way. Note however, that only DATA keys 0 to 3 are enabled. This is because we are not using an HP 8181B extender and have only connectors 0 to 3 fitted.

If you replace a channel such as 3-1 for example, that is part of a data segment made up of consecutive channels such as 3-3, 3-2, 3-1, 3-0, 2-3, 2-2, 2-1, 2-0 with another data channel such as 1-1, and you still wish to use the resulting segment as an 8-bit data bus, you must make a corresponding change to the physical wiring leading to the device under test.



are scanning softkeys, which allow you to position the inverse video cursor at the correct data channel before making a change to the configuration. If you move the cursor to the left past all the data channels, you access the strobe channel.

Channel Insertion

INSERT CHNL

enables you to add additional data channels to the display. Move the cursor to the desired position and press **INSERT CHNL**. The new channel will always appear to the right of the current channel and will always have a channel number one less than the current channel until you reduce the channel number to zero. Then the connector

Output Page

number is reduced by one, the channel number goes to three and the whole sequence is repeated. When you get to channel 0-0, the next inserted channel will be channel three of the highest installed connector, which in our case is three. (The maximum size of a segment is 16 channels.)

As an example to illustrate channel insertion, let us consider the case where we wish to insert channel 0-1 in between channels 2-2 and 2-1. As the first step we use the arrow keys to bring the cursor over channel 2-2 as shown in Figure 3-19.

```

8180B                                     Status  STOP
                                     Address
-----
Load Impedance 50 Ω                     LEVEL
Outputs         ON                       Label   High   Low
Clock 1 LABEL A NORMAL                   A      +0.25 V +0.25 V
Clock 2 LABEL B NORMAL                   B      +5.00 V +0.00 V
Strobe ECL     NORMAL                     C      -0.80 V -1.80 V
                                           D      +2.40 V +0.80 V

Channel Configuration , Label (Grey=Complement)

Connector 3333 2222 1111 0000
Channel   3210 3210 3210 3210
Label     AAAA AAAA AAAA AAAA

ENTER NEW VALUE _____
Configuration 2.Data Segment
Connector     2222           Code BIN  Entry YES(↑)
Channel       3210
INSERT CHNL  DELETE CHNL  ←      →
INSERT SEGMENT Std. Config  Code/Entry  EXIT
  
```

Figure 3-19. Channel Config Screen of the Output Page

We now push the **INSERT CHNL** key. The result of this step is shown in Figure 3-20. An extra channel is now displayed between channels 2-2 and 2-1. Its designation is 2-1 because it follows after channel 2-2. We also see a flashing error message in line 21 of the display: Dupl Chnl in Segment. This is because channel 2-1 now occurs twice in the same segment. For a more detailed explanation of this error message refer to "Error and Warning Messages" at the end of this section.

Output Page

8180B		Status	STOP
		Address	
----- OUTPUT -----			
Load Impedance	50 Ω	LEVEL	
Outputs	ON	Label	High Low
Clock 1 LABEL A	NORMAL	A	+0.25 V +0.25 V
Clock 2 LABEL B	NORMAL	B	+5.00 V +0.00 V
Strobe ECL	NORMAL	C	-0.80 V -1.80 V
		D	+2.40 V +0.80 V
Channel Configuration , Label (Grey=Complement)			
Connector	3333 22022 1111 0000		
Channel	3210 32110 3210 3210		
Label	AAAA AAAAA AAAA AAAA		
ENTER NEW VALUE -----			
Configuration	2.Data Segment	Dupl Chnl in Segment	
Connector	22022	Code BIN	Entry YES(↑)
Channel	32110		
INSERT CHNL DELETE CHNL ← →			
INSERT SEGMENT Std Config Code/Entry EXIT ↑			

Figure 3-20. Output Page after Channel Insertion

As the last step we type 01 over the cursor using the DATA keys. The error message disappears and we now have an extra channel 0-1 inserted in between channels 2-2 and 2-1 as is shown in Figure 3-21.

8180B		Status	STOP
		Address	
----- OUTPUT -----			
Load Impedance	50 Ω	LEVEL	
Outputs	ON	Label	High Low
Clock 1 LABEL A	NORMAL	A	+0.25 V +0.25 V
Clock 2 LABEL B	NORMAL	B	+5.00 V +0.00 V
Strobe ECL	NORMAL	C	-0.80 V -1.80 V
		D	+2.40 V +0.80 V
Channel Configuration , Label (Grey=Complement)			
Connector	3333 22022 1111 0000		
Channel	3210 32110 3210 3210		
Label	AAAA AAAAA AAAA AAAA		
ENTER NEW VALUE -----			
Configuration	2.Data Segment	Code BIN	Entry YES(↑)
Connector	22022		
Channel	32110		
INSERT CHNL DELETE CHNL ← →			
INSERT SEGMENT Std Config Code/Entry EXIT ↑			

Figure 3-21. Output Page after Channel Substitution

Output Page

Channel Deletion

DELETE CHNL enables you to delete unwanted channels from the display. The channel currently highlighted by the cursor is deleted.

Segment Insertion

INSERT SEGMENT enables you to add new data segments to the display. Move the cursor to the desired position and press **INSERT SEGMENT**. The new segment will always appear to the right of the current segment and will always have a channel number one less than the channel in the current segment until you reduce the channel number to zero. Then the connector number is reduced by one, the channel number goes to three and the whole sequence is repeated. When you get to channel 0-0, the next inserted segment will contain channel three of the highest installed connector, in our case three.

Calling Standard Channel Configuration

Std Config enables you to set the standard configuration, i.e. the one showing all the installed channels. Confirm your entry by pressing **EXECUTE**. Note that "Standard Config" is not the same as "Recall Standard Set", as only the channel configuration is changed. The other parameters, such as level and timing settings etc. are left undisturbed. However "Standard Config" is performed as part of "Recall Standard Set".

Data Encoding

Code/Entry enables you set up the method of data encoding and to allow or disable data editing on the Data Page. On pressing this key the following choices are presented:

BINARY codes the data contained in the currently accessed segment in the binary format on the Data Page. The Code field in inverse video (in line 22) echoes the selection by displaying **BIN**.

OCTAL codes the data contained in the currently accessed segment in the octal format on the Data Page. The Code field in inverse video (in line 22) echoes the selection by displaying **OCT**.

HEXADECIMAL codes the data contained in the currently accessed segment in the hexadecimal format on the Data Page. The Code field in inverse video (in line 22) echoes the selection by displaying **HEX**.

DECIMAL codes the data contained in the currently accessed segment in the decimal format on the Data Page. The Code field in inverse video (in line 22) echoes the selection by displaying **DEC**.

Note that the data format selected here affects the editing of data on the Data Page. For example, if a segment is coded for decimal entry but contains only two bits, then only DATA keys 0 to 3 will be active when editing it on the Data Page. Similarly, if a segment is coded for hexadecimal entry but contains only three channels, then only DATA keys 0 to 7 (not 0 to F) will be active.

← moves the cursor to the left (functions the same way as above).

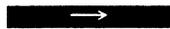
→ moves the cursor to the right (functions the same way as above).

Output Page

ENTRY YES/NO enables editing on the Data Page of data contained in the currently accessed segment. The key toggles between YES and NO as displayed in the inverse video field called "Entry" in line 22 of the display. If YES, an up arrow under the enabled segment on the Data Page signifies that data editing is possible.

Data Channel Labeling and Channel Polarity

The channel label feature enables you to assign one of the voltage level labels A,B,C or D to any of the data channels. You do this by pressing the **Chnl Label** key and then moving the inverse video cursor to the desired channel on the screen and selecting A,B,C or D on the DATA key pad. The cursor then automatically moves on to the next channel on the right. The **Chnl Label** key calls up the following softkeys.



moves the cursor to the right one channel at a time.



moves the cursor to the left one channel at a time. This softkey is blank if the cursor is located at the leftmost channel, or if you have just executed "Standard Config" or "Recall Standard Set". Notice that you cannot go further left past the leftmost channel to access the strobe, as strobe level and polarity are set by separate softkeys.



moves the cursor all the way to the left to the starting position at the leftmost channel. This softkey is blank if the cursor is located at the leftmost channel, or if you have just executed "Standard Config" or "Recall Standard Set".



inverts (complements) the channel polarity and moves on to the next channel on the right. Each inverted channel is marked by a grey field in the Label row in the Report Area (line 15). The inversions for the segment currently being accessed are also echoed in the Softkey Label Area on line 23.



returns a complemented channel to the default (normal) polarity.

Exercise - Level Setting

Set the following:

Clock 1:	TTL Levels, Normal Polarity
Clock 2:	TTL Levels, Complement Polarity
Strobe:	TTL Levels, Normal
Channel:	0-0, 0-1, 0-2: High Level 4.0 V, Low Level 0 V
Channel 0-3 :	TTL Levels
All Other Channels:	High Level 15 V Low Level -5 V

Note that in order to set a level of 15 V, load impedance must first be changed to "open". (The maximum level obtainable at the load impedance of 50 Ohms is 5.50 V. See Table 3-2, giving generator output level capabilities.)

Output Page

Error and Warning Messages

Dupl Chnl in Segment This flashing message appears on the **Chnl Config** screen in the Softkey Label area in line 21 if you have duplicated a channel in one segment (and the cursor lies in that segment). This happens also if you have inserted a new channel at the start of a segment (leftmost channel of a segment) or in the middle of a segment. Inserting a channel at the end of a segment (rightmost channel of a segment) does not trigger this warning message as the next channel always has a lower channel or segment number.

The generator cannot be seriously used when an error condition prevails, as certain data edit functions cannot be performed. If you need to insert extra channels in a segment and get this warning, you can change the channel and connector numbers via the DATA keys.

VALUE OUT OF RANGE This flashing inverse video message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable to the Level entry. If you exit the page where you made such an entry, it will be ignored and the previous entry will be retained.

Outputs Off This flashing message is strictly speaking a warning rather than an error message. It tells you that generator outputs have not been switched on. This is a normal condition after instrument switch-on.

E A flashing letter E will appear next to any variables whose settings have become incompatible with each other as a result of entering a false value. This applies to any (or all) of the individual voltage level labels. An error occurs if you enter a value that is incompatible with the maximum or minimum swing as given in Table 3-2, Summary of generator output level capabilities.

Suppose for instance, that you have entered "Recall Standard Set". This gives a high level on Label A of +0.25 V and a low level on Label A of -0.25 V. If you then decrement the Label A high value by 10 mV an error occurs. The error warning "E" appears next to the level settings for the affected label and next to the inverse video entry field for the currently accessed level.

SWING This flashing message is triggered by an incompatible level entry, which we have just covered above, and appears in line 2 of the display on all pages and sub-pages, serving as a reminder of the error condition.

The generator cannot be seriously used when an error condition prevails, as channel voltage levels can no longer be guaranteed.

3-7 Data Page

The fourth page is the Data Page. It gives you access to the generator memory and the data editing features. There are a number of ways of generating or bringing into generator's memory the data that will be used to stimulate a device under test. The simplest, and also the most tedious, is to type the data direct into the memory using the DATA keys. Other ways include the use of functions that set up up-counters, down-counters or a pseudo-random binary sequence, or set whole channels high or low (1 or 0). In addition, data can be edited (inserted, deleted or copied) or often used data sequences can be set up in a separate memory containing 16 words (macros) and then brought over to the main memory as required.

Data can also be brought in from an external device such as a computer system where it may be stored in the form of a disc file. The data transfer mechanism is the Fast Binary Transfer Mode, which is discussed in Chapter 7 of this manual. The CAE Link, which can convert and download large chunks of stimulus data in the form of device test vectors from a Computer Aided Engineering design station is yet another way of bringing data into the generator's memory. The CAE Link uses Fast Binary Transfer in the last stage of the conversion and transfer process. The link is covered in the CAE Link Manual.

Call up the Data Page now by pressing PAGES and **DATA**.

Figure 3-22 shows the Data Page and the functions of the generator which are now accessible via softkeys through this page. Let us now go through the functions in detail.

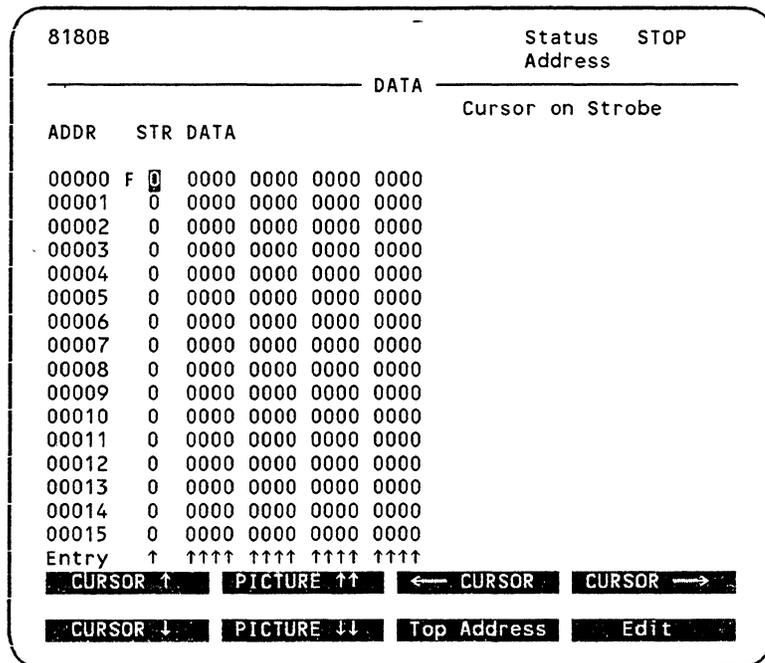


Figure 3-22. The Data Page

Notice that when the Data Page is called up, channel data is displayed as defined by the channel configuration keys on the Output Page, that is in binary, octal, decimal or hexadecimal format. These keys are also repeated on this page and their operation is identical. The data can now be entered and modified. Data entry is performed with the DATA keys at the current cursor location.

Which of the DATA keys are enabled for data entry depends on the data configuration currently in use. If you have just recalled Standard Set the data in all segments will be encoded in binary. Hence only the

Data Page

DATA keys 0 and 1 will be enabled. If you have selected octal format, DATA keys 0 to 7 will be enabled. For decimal format it will be keys 0 to 9 and for hexadecimal 0 to F.

The letter F in between the address and strobe columns on the screen indicates that this address is currently the First Address. Similarly, the letter L marks the Last Address. Setting the first and last addresses was covered on the Control Page.

Cursor and Screen Controls

There are several ways to move the cursor:

- CURSOR ↑** enable the cursor to be stepped vertically through the data stream.
- CURSOR ↓** Holding down the softkey causes repetitive cursor movement. When the cursor reaches the top (bottom) of the screen, further repetition causes the data and address display to scroll.
- PICTURE ↑↑** replace the current sixteen lines displayed by the next numerically higher (lower) sixteen lines. Single or repetitive operation is available.
- PICTURE ↓↓**
- ← CURSOR** enable horizontal movement of the cursor. When the cursor is at the limit of its travel, it jumps to the beginning of the next (end of the previous) line. When "Entry Allowed" arrows under a data segment/s are missing, the cursor jumps over the disabled segment/s to the next enabled segment. (Refer back to Channel Configuration menu on the Output Page.) If none of the segments are enabled, the cursor is not displayed.
- CURSOR →**
- Top Address** enables a new display of data to be called up quickly. It is activated either by entering a 4 digit number (including leading zeros) or via the **INCREMENT** or **DECREMENT** keys. If you enter a number of less than 4 digits, follow this by pressing the softkey **ENTER NUMBER**.

Exercise - Data Display

1. Set Top Address to some address, for instance 128.
 2. Recall Standard Set.
 3. Set Top Address to 16383 (1023)
- You should now see both the last and the first address on the screen.

Data Editing

The softkey **Edit** opens the way to the data editing capabilities of the generator. On pressing it, the following softkey menu appears.

Address Code **Clear & Set** **Channel Edit** **Line Edit**
CHECKSUM **Entry mode** **Chnl Config** **EXIT ↑**

Data Edit - Address Encoding

Address Code allows you to set the address format. After recalling the Standard Set the address is encoded in decimal. Additional options are octal and hexadecimal. The desired format is selected by pressing the appropriate key **OCTAL**, **HEXADECIMAL** or **DECIMAL**. The inverse video field in line 22 shows

Data Page

the current format. Leave the menu by pressing the **EXIT ↑↑** key. Note that the First and Last Addresses on the Control Page are displayed in the address format selected here.

Memory Clear and Set

Clear & Set allows you to clear or set all data memory locations. This softkey calls a subsequent softkey menu offering three functions.

Clear Data clears all data channel memory locations (except strobe) to zero. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**.

Set Data sets all data channel memory locations (except strobe) to one. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**.

Clear Strobe clears all strobe memory locations to zero. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**.

Channel Editing

Channel Edit enables you to carry out editing tasks on individual channels. It is important to note that Channel Edit operations function only between the currently valid First and Last Addresses.

Clear Channel clears all relevant memory locations in the accessed channel to zero. Use the arrow keys **←** and **→** to move the cursor to the required channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **EXIT ↑↑**. Note that if you have previously duplicated a channel in the same or a different segment, then changing one of these channels will result in a change in all the others.

Set Channel sets all relevant memory locations in the accessed channel to one. Use the arrow keys **←** and **→** to move the cursor to the required channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **EXIT ↑↑**. Note that if you have previously duplicated a channel in the same or a different segment, then changing one of these channels will result in a change in all the others.

Copy Channel allows you to perform a one-to-one channel copy. You can copy the contents of memory of one channel to that of another channel within the relevant address range. The information you need to perform the copy operation is given in lines 21 to 23 of the display. The source channel is contained within a grey field and its segment is shown on the left hand side of the display. The destination channel is contained within

Data Page

an inverse video field and its segment is shown on the right hand side of the display.

A similar distinction is used for the data segments in the Report Area. Two pairs of softkey arrows  and  move the cursors to the desired channels. The left hand arrows move the grey cursors (source channel/segment) and the right hand arrows move the inverse video cursors (destination channel/segment).

To carry out the actual copy operation press the key . If you've changed your mind, leave the menu by pressing .

(pseudo-random binary sequence) enables a different random binary pattern to be set on each channel within the relevant address range. The same pattern will always appear in a given channel when PRBS is enabled. Use the arrow keys  and  to move the cursor to the required channel. To enter PRBS on a particular channel press the key . If you've changed your mind, leave the menu by pressing . Note that if you have previously duplicated a channel in the same or a different segment, then changing one of these channels will result in a change in all the others.

enables you to set up an up-counter on individual segments within the relevant address range. Use the arrow keys  and  to move the cursor to the required segment. To enter an up-counter on a particular segment press the key . If you've changed your mind, leave the menu by pressing . Avoid setting an up-counter on a segment containing a duplicate channel as this gives unpredictable results.

enables you to set up a down-counter on individual segments within the relevant address range. Use the arrow keys  and  to move the cursor to the required segment. To enter a down-counter on a particular segment press the key . If you've changed your mind, leave the menu by pressing . Avoid setting a down-counter on a segment containing a duplicate channel as this gives unpredictable results.

Exercise - Setting a Data Pattern

Set the following:

- First Address: 128
- Last address: 136
- Clear entire memory
- Top Address: 126
- Chans. 2-3 to 2-0: Up-counter
- Channel 1-3: PRBS pattern

Data Page

Line Editing

Line Edit

enables you to carry out editing tasks on individual lines. This is especially useful if you are working with many data channels in parallel. The sort of tasks that can be performed includes inserting, deleting and copying lines, or bringing in line macros from the Macro Data Page, and so on.

Copy Macro

allows you to bring in a single predefined data line from the Macro Data Page. This is useful if there is a certain data line that you use frequently.

Using Copy Macro you can copy any one of the 16 data lines previously edited on the Macro Data Page to any data line on the Data Page. The small Macro Data Memory is totally independent of the main Data Memory. The Copy Macro feature performs only a memory transfer.

After pressing the **Copy Macro** key a new set of softkeys appears. You will see a softkey **PREV FIELD** and two softkeys **INCREMENT** and **DECREMENT**. These three keys always appear together. As well as these keys an inverse video field appears on the right hand side of the display in line 22 showing the destination address (the address to which the new data will be copied). You can increment or decrement the destination address or make a direct entry using the DATA keys and the **ENTER NUMBER** softkey.

The source address (the one from which data will be copied) is also shown in line 22 in a grey field. If you now press the softkey **PREV FIELD** the source address field switches to inverse video and the destination address switches to grey. You can now enter in hex notation the address on the Macro Data Page from which you want to copy the line of data. Use the **EXECUTE** key to perform the copy. The **NEXT FIELD** softkey gets you from the source address to the destination address. Leave the menu by pressing **EXIT: ↑↑↑**.

Copy Macro's

allows you to bring in several data lines from the Macro Data Page. This is useful if there are certain consecutive data lines that you use frequently.

Using Copy Macro's you can copy a block of up to 16 data lines previously edited on the Macro Data Page to any address on the Data Page including those causing data to be brought in over the 16384/00000 address boundary.

After pressing the **Copy Macro's** key a new set of softkeys appears. You will see a softkey **PREV FIELD** and two softkeys **INCREMENT** and **DECREMENT**. These three keys always appear together. As well as these keys an inverse video field appears on the right hand side of the display in line 22 showing the destination address (the address to which the new data will be copied). You can increment or decrement the destination address or make a direct entry using the DATA keys and the **ENTER NUMBER** softkey. The subsequent lines from the Macro Data page are automatically allocated to the Data Page addresses depending on the macro block size.

The source addresses (those from which data will be copied) are also shown in line 22 in a grey field. If you now press the softkey

Data Page

PREV FIELD the destination address switches to grey. The source address field contains the macro start and stop addresses. Only the stop address switches to inverse video. To get at the macro start address press **PREV FIELD** again. You can now enter in hex notation the start address followed by the stop address of the data on the Macro Data Page which you want to copy to the Data Page. Use the **EXECUTE** key to perform the copy. The **NEXT FIELD** softkey gets you from the source addresses to the destination address. Leave the menu by pressing **EXIT**.

Limit Address

is normally used in conjunction with the Insert Line and Delete Line functions to safeguard data at addresses greater than the Limit Address. This is particularly useful if you have allocated certain data sequences to certain parts of memory in order to carry out particular test tasks using different sets of first and last addresses. The actual mechanism of how Limit Address interacts with the Insert Line and Delete Line functions is described later, when we discuss these softkeys. After switching the generator on the Limit Address defaults to the end of the address range, i.e. 16383 (1023). Executing Recall Standard Set has no effect on the Limit Address setting.

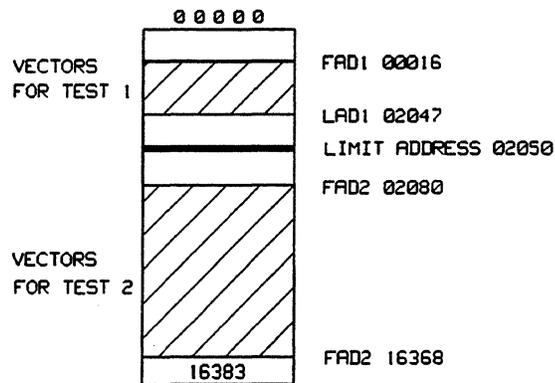


Figure 3-23. The Use of Limit Address

The example in Figure 3-23 demonstrates a case on the generator B version where two areas in memory are to be used at different times to output data to a test device. The first data set resides in the address range from 00016 to 02047, the second in the range between 02080 to 16368. In order to protect the second data set you could set the Limit Address to say 02050 and edit the first data set. Having finished, you could set the limit address to say 00000 in order to safeguard the first data set and then edit the second. This method is also valid for the A version, except that the memory range is 1024 words.

After pressing the **Limit Address** softkey you can enter the address directly into the inverse video field in line 22 of the display, or you can use the **INCREMENT** and **DECREMENT** softkeys. Leave the menu by pressing **EXIT**.

Insert Line

allows you to insert a line of data (containing zeros) at the selected address. Suppose we wish to insert a line at address 00004. In order to see what is happening we will now set up some initial conditions. You should have no

Data Page

problems with the steps suggested below, as we have already covered them all in this chapter.

- Recall Standard Set
- Set First Address to 00000
- Set Last Address to say 00010
- Set all channels to 1
- Set up-counter on first segment
- Set Limit Address to 00008

Enter 00004 into the inverse video field in line 22 of the display. Press **EXECUTE** to perform the insertion. Then use the **DECREMENT** key to bring the address 00000 to the top of the display. You will now have a screen as shown in Figure 3-24. The data lines between addresses 00004 and 00008 move down by one (to the next higher address) and the data at address 00008 is lost. Had we not set the Limit Address to 00008, the data at address 16383 would have been lost, as this is the default limit address. For each data line inserted, one data line is lost at the current Limit Address.

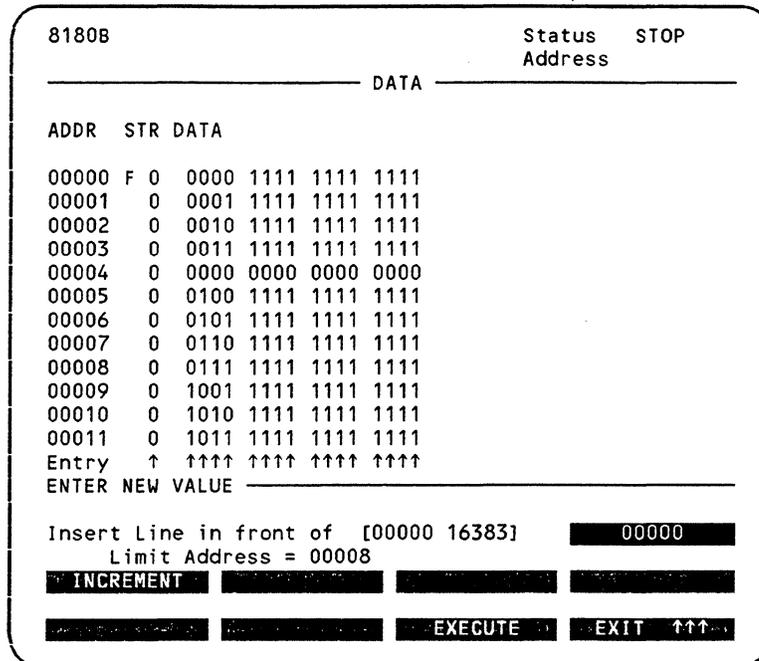


Figure 3-24. Inserting a Single Data Line

Let's say that we now want to insert extra lines at address 00006. We find it is possible to insert only three extra lines, because the limit address has been set to 00008. After rolling the data display back to show the first address, we should now see the screen as in Figure 3-25.

Data Page

8180B		Status	STOP
		Address	
DATA			
ADDR	STR	DATA	
00000	F 0	0000	1111 1111 1111
00001	0	0001	1111 1111 1111
00002	0	0010	1111 1111 1111
00003	0	0011	1111 1111 1111
00004	0	0000	0000 0000 0000
00005	0	0100	1111 1111 1111
00006	0	0000	0000 0000 0000
00007	0	0000	0000 0000 0000
00008	0	0000	0000 0000 0000
00009	0	1001	1111 1111 1111
00010	0	1010	1111 1111 1111
00011	0	1011	1111 1111 1111
Entry	↑	↑↑↑↑	↑↑↑↑ ↑↑↑↑
ENTER NEW VALUE			
Insert Line in front of [00000 16383]		00000	
Limit Address = 00008			
INCRMENT 			
 EXECUTE EXIT ↑↑↑↑			

Figure 3-25. Inserting Extra Lines up to the Limit Address

Leave the menu by pressing EXIT ↑↑↑↑.

Delete Line

allows you to delete a line of data from the selected address. Suppose we wish to delete a line at address 00004. In order to see what is happening we have to once again set up some initial conditions. These will be identical to those we just used for the Insert Line function.

- Recall Standard Set
- Set First Address to 00000
- Set Last Address to 16383
- Set all channels to 1
- Set up-counter on first segment
- Set Limit Address to 00008

Enter 00004 into the inverse video field in line 22 of the display. Press EXECUTE to perform the deletion. Then use the DECREMENT key to bring the address 00000 to the top of the display. You will now have a screen as shown in Figure 3-26.

Data Page

8180B		Status	STOP
	DATA	Address	
ADDR	STR	DATA	
00000	F 0	0000 1111 1111 1111	
00001	0	0001 1111 1111 1111	
00002	0	0010 1111 1111 1111	
00003	0	0011 1111 1111 1111	
00004	0	0101 1111 1111 1111	
00005	0	0110 1111 1111 1111	
00006	0	0111 1111 1111 1111	
00007	0	1000 1111 1111 1111	
00008	0	0000 0000 0000 0000	
00009	0	1001 1111 1111 1111	
00010	0	1010 1111 1111 1111	
00011	0	1011 1111 1111 1111	
Entry	↑	↑↑↑↑ ↑↑↑↑ ↑↑↑↑ ↑↑↑↑	
ENTER NEW VALUE			
Insert Line in front of		[00000 16383]	00000
Limit Address = 00008			
INCREMENT			
EXECUTE			
EXIT ↑↑↑			

Figure 3-26. Deleting a Single Data Line

Let's say that we now want to delete extra lines at address 00006. We find it is only possible to delete two more lines, because the limit address has been set to 00008. After rolling the data display back to show the first address, we should now see the screen as in Figure 3-27.

8180B		Status	STOP
	DATA	Address	
ADDR	STR	DATA	
00000	F 0	0000 1111 1111 1111	
00001	0	0001 1111 1111 1111	
00002	0	0010 1111 1111 1111	
00003	0	0011 1111 1111 1111	
00004	0	0101 1111 1111 1111	
00005	0	0100 1111 1111 1111	
00006	0	0000 0000 0000 0000	
00007	0	0000 0000 0000 0000	
00008	0	0000 0000 0000 0000	
00009	0	1001 1111 1111 1111	
00010	0	1010 1111 1111 1111	
00011	0	1011 1111 1111 1111	
Entry	↑	↑↑↑↑ ↑↑↑↑ ↑↑↑↑ ↑↑↑↑	
ENTER NEW VALUE			
Insert Line in front of		[00000 16383]	00000
Limit Address = 00008			
INCREMENT			
EXECUTE			
EXIT ↑↑↑			

Figure 3-27. Deleting Extra Lines up to the Limit Address

Leave the menu by pressing **EXIT ↑↑↑**.

Data Page

Copy Line

allows you to copy a line of data from one memory location to another by overwriting the data at the destination memory location. The source memory location remains undisturbed.

After pressing **Copy Line** a new set of softkeys appears together with two extra fields in in lines 22 and 23 of the display. The field in line 22 is highlighted in inverse video and gives the address data is copied from. You can type over the current address using the DATA keys and complete your entry by pressing the **ENTER NUMBER** softkey. Alternatively, use the **INCREMENT** and **DECREMENT** softkeys to reach the required address. The numbers in the square brackets also in line 22 give the address range.

The grey field in line 23 gives the address data is copied to. To access the "copy-to" address press the **NEXT FIELD** softkey. Notice that the "copy-to" address is now highlighted. Locate the required address the same way as previously. Press the **EXECUTE** softkey to copy the line.

To scroll the data on the screen you have to access the "copy-from" address again. To do that press the **PREV FIELD** softkey. To leave the menu press **EXIT**.

Move Line

allows you to move a line of data from one memory location to another. The data between the two addresses moves up or down one line, depending on whether the line is being moved to a higher or a lower address in memory. The following example illustrates this concept.

First, we have to set up some initial conditions. You should have no problems with the steps given below. We have already covered them in this chapter.

- Recall Standard Set
- (Set First Address to 00000)
- (Set Last Address to 16383 (1023))
- Set data in all channels to 0
- Set up-counter on first segment
- Set data in first segment to decimal mode

Let us suppose that we want to move a line of data at address 00006 to address 00002. After pressing **Move Line** a new set of softkeys appears together with two extra fields in in lines 22 and 23 of the display as shown in Figure 3-28. The field in line 22 is highlighted in inverse video and gives the address data is moved from. You can type over the current address using the DATA keys and complete your entry by pressing the **ENTER NUMBER** softkey. Alternatively, use the **INCREMENT** and **DECREMENT** softkeys to reach the required address. We will type in 00006. The numbers in the square brackets also in line 22 give the address range available for the move operation.

Data Page

8180B		Status	STOP
	DATA	Address	
ADDR	STR	DATA	
00006	0	06 0000 0000 0000	
00007	0	07 0000 0000 0000	
00008	0	08 0000 0000 0000	
00009	0	09 0000 0000 0000	
00010	0	10 0000 0000 0000	
00011	0	11 0000 0000 0000	
00012	0	12 0000 0000 0000	
00013	0	13 0000 0000 0000	
00014	0	14 0000 0000 0000	
00015	0	15 0000 0000 0000	
00016	0	16 0000 0000 0000	
00017	0	17 0000 0000 0000	
Entry	↑	↑↑ ↑↑↑↑ ↑↑↑↑ ↑↑↑↑	
ENTER NEW VALUE _____			
Move Line		[00000 16383]	00006
to Line		[00000 16383]	00002
INCREMENT	PREV FIELD		
DECREMENT		EXECUTE	EXIT ↑↑↑

Figure 3-28. Moving a Line - Initial Screen

The grey field in line 23 gives the address data is moved to. To access the "move-to" address press the **NEXT FIELD** softkey. Notice that the "move-to" address is now highlighted. Input the required address the same way as previously. We type in 00002. Press the **EXECUTE** softkey to copy the line. To access the "move-from" address again press the **PREV FIELD** softkey. Now depress the **DECREMENT** key until address 00000 appears. You should now see the screen as shown in Figure 3-29.

8180B		Status	STOP
	DATA	Address	
ADDR	STR	DATA	
00000	F 0	00 0000 0000 0000	
00001	0	01 0000 0000 0000	
00002	0	06 0000 0000 0000	
00003	0	02 0000 0000 0000	
00004	0	03 0000 0000 0000	
00005	0	04 0000 0000 0000	
00006	0	05 0000 0000 0000	
00007	0	07 0000 0000 0000	
00008	0	08 0000 0000 0000	
00009	0	09 0000 0000 0000	
00010	0	10 0000 0000 0000	
00011	0	11 0000 0000 0000	
Entry	↑	↑↑ ↑↑↑↑ ↑↑↑↑ ↑↑↑↑	
ENTER NEW VALUE _____			
Move Line		[00000 16383]	00000
to Line		[00000 16383]	00002
INCREMENT			
DECREMENT	NEXT FIELD	EXECUTE	EXIT ↑↑↑

Figure 3-29. Moving a Line - Final Screen

Data Page

Data at address 00006 has been moved to address 00002. The data lines at addresses 00002 to 00005 have been moved down by one address. To leave the menu press **EXIT** **↑↑↑**.

Exercise - Line Edit

- Set Limit Address to 150
- Copy line 130 into address 135
- Move line 140 to line 146
- Insert 2 lines at address 137
- Delete a line at address 148

Data Integrity - Checksum

CHECKSUM provides you with the means of checking the integrity of the data stored in the generator's memory. When you press this softkey, a message Data Checksum NNNNNNNN is displayed in line 22 of the screen, where NNNNNNNN is a eight digit number. If you change the data in memory in any way, the checksum number will change.

Auto Cursor Movement - Data Page

Entry mode selects the cursor movement when entering data from the DATA keys on the screen.

HOLD CURSOR holds the cursor at the current data bit after data entry - no cursor movement.

HORIZONTAL moves the cursor horizontally to the next data bit on the right. When the end of the line is reached the cursor wraps round to the beginning of the next line, i.e. the cursor.

VERTICAL moves the cursor vertically downwards to the same data bit in the word, but at a higher address.

Channel Configuration - Data Page

Chnl Config allows you to set the generator channel configuration. The softkey menus and functions behind this softkey are identical to those that can be accessed via the **Chnl Config** softkey on the Output Page. We have already covered these procedures in the Subsection entitled Channel Configuration. The only difference is that on the Output Page the Report Area of the screen shows the channels, whereas here on the Data Page it shows the data in the memory behind each channel.

Data Page

Exercise - Data Pattern Generation

0000	00000
0000	00001
0001	00010
0001	00011
0010	00100
0010	00101
0011	00110
0011	00111
0100	01000
0100	01001
0101	01010
0101	01011
0110	01100
0110	01101
0111	01110
0111	01111

Create the bit pattern shown in the left hand column between addresses 0000 and 00031. This is an up counter, with every digit listed twice. This might be required in a memory test, where you write to a specific memory cell, then immediately read back the same cell for test. The next memory cell will then be addressed.

The pattern is easy to generate if you appreciate that it represents an up counter in which the least significant bit is missing.

We configure a segment of five channels, then create an up counter, as shown in the right hand column, and finally delete the channel which carries the least significant bit.

We have now covered the most complex page of the data generator.

Error Messages

The generator monitors the entries you make and will return an error message if any of them are incorrect. Here is a list of error messages that can be displayed as a result of incorrect entries on the Data Page.

VALUE OUT OF RANGE This inverse video flashing message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable wherever you can make a direct address entry, that is in the following cases: Top Address, Copy Macro, Copy Macros, Insert Line, Delete Line, Copy Line, Move Line and Limit Address. After exiting the page where you made such an entry, the instrument will return to the previously set value.

Dupl Chnl in Segment This flashing message appears on the **Chnl Config** screen in the Softkey Label area in line 21 if you have duplicated a channel in one segment (and the cursor lies in that segment). This happens also if you have inserted a new channel at the start of a segment (leftmost channel of a segment) or in the middle of a segment. Inserting a channel at the end of a segment (rightmost channel of a segment) does not trigger this warning message as the next channel always has a lower channel or segment number.

The generator cannot be seriously used when an error condition prevails, as certain data edit functions cannot be performed. If you need to insert extra channels in a segment and get this warning, you can change the channel and connector numbers via the DATA keys.

Display incomplete This flashing message on the **Chnl Config** screen in the Report Area in line 5 of the display appears if you have inserted more channels or segments than can be displayed on the screen. You should delete some of the unwanted channels.

Data Page

The message can also appear if the physical number of channels installed (in one generator and two extenders) is greater than can be displayed on the screen. This problem arises if the displayed segments are encoded in binary. If you change to the hexadecimal mode, you can display all 64 channels on the screen.

You should avoid using the generator when this error message appears, as the channels which are not displayed cannot be edited.

3-8 Store/Recall Page

The fifth page is the Store/Recall Page. It allows you to store and recall up to three generator parameter sets and up to nine first and last address pairs. These facilities are useful if you are performing a number of different tests and need to switch between different parameters or first and last address values. This page also enables you to recall the Standard Set (default set) of generator parameters. A parameter set includes all generator parameter settings. It does not include the data stored in the main or the macro memory. A listing of these parameters is given in Table A-1, Appendix A at the back of this manual.

Call up the Store/Recall Page now by pressing PAGES and **STORE/RECALL**.

The Store/Recall Page is shown in Figure 3-30. Its contents are entirely dependent on what parameters or address pairs have been stored by the previous user. If your generator is new it will still have some entries on this page, as it will have gone through the factory final test.

8180B		Status	STOP
		Address	
STORE/RECALL			
	First Address	Last Address	Frequency
Parameter 1	0001	0011	1.00 MHz
Parameter 2	0002	0022	2.00 MHz
Parameter 3	0003	0033	3.00 MHz
Addresses 1	0001	0010	
Addresses 2	0002	0020	
Addresses 3	0003	0030	
Addresses 4	0004	0040	
Addresses 5	0005	0050	
Addresses 6			
Addresses 7			
Addresses 8	0008	0080	
Addresses 9			
Select Further			
Rcl Parameter	Rcl Addresses	Rcl Std Set	
Sto Parameter	Sto Addresses		

Figure 3-30. Store/Recall Page

In our version of the Store/Recall Page the values for the first and last addresses and the frequencies are not perhaps very realistic, but they offer a clear overview of what is going on. Notice also that Addresses 6, 7 and 9 are not present, as no values have been stored to these.

The generator is equipped with batteries which allow the internal memory to retain the stored parameters and address pairs for approximately one week. If you come to use the generator after longer than that, it is possible that the batteries will be discharged and the Store/Recall Page will be empty of any stored parameters or addresses. This can also be the case if the generator has been repaired. If this happens, a flashing inverse video message **PARAMETER DESTROYED - STANDARD SET RECALLED**, displayed on the main page after you switch the generator on will warn you of this condition. As you use the generator, the batteries will recharge again and the instrument's memory storage facilities will be enabled. As soon as you use the store functions, the corresponding memory locations will be filled.

NOTE

Whenever you recall a parameter, including the Standard Set, the generator will go into the STOP state.

Recalling Standard Set

When you call up the Standard Set you cause the generator to load a set of default parameters. These are preset values for the various timing settings such as frequency, width or delay, or input and output signal settings such as input threshold or output levels and so on. The Standard Set also recalls the standard channel configuration. This configuration depends on the number of data channels present in the data generator and the data generator extender/s (if connected). Table A-1 in Appendix A lists the full set of parameters (and their values) that are loaded when Recall Standard Set is executed.

NOTE

Whenever you recall the Standard Set the generator outputs will be turned off. This applies also to any extenders that may be connected. A flashing warning Outputs Off appears in line 1 of the display.

After pressing the **Rec Std Set** softkey you have to confirm your entry by pressing **EXECUTE** on the next menu. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Storing a Parameter

You can store up to three different parameter sets. As an aid to quick identification of the stored parameter sets, the First and Last Addresses and the Clock Frequency for each set are displayed in the Report Area of the screen. After pressing the **Sto Parameter** softkey you have to enter a single digit 1, 2 or 3, specifying a store location for the current parameter set. Confirm your selection by pressing **EXECUTE**. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Recalling a Parameter

You can recall up to three different parameter sets. After pressing the **Rec Parameter** softkey you have to enter a single digit 1, 2 or 3, specifying the store location of the parameter set you wish to recall. Confirm your selection by pressing **EXECUTE**. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Storing an Address

You can store up to nine different first and last address pairs. After pressing the **Sto Addresses** softkey you have to enter a single digit between 1 and 9, specifying a storage location for the current address pair. Confirm your selection by pressing **EXECUTE**. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Store/Recall Page

Recalling an Address

You can recall up to nine different first and last address pairs. After pressing the **Rcl. Addresses** softkey you have to enter a single digit between 1 and 9, specifying the storage location of the address pair you wish to recall. Confirm your selection by pressing **EXECUTE**. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT** ↑.

Exercise - Storing and Recalling a Parameter Set

- Recall Standard Set
- Change First and Last addresses
- Insert data segments and channels
- Change output voltage levels
- Store the current parameters
- Recall Standard Set
- Recall the previously stored parameter set
- Check on the Control, Output and Data Pages that the parameter set has been recalled

3-9 Miscellaneous Page

The Miscellaneous Page is basically an information page. It tells you what the generator HP-IB address settings are and gives you an overview of the installed channels. In addition, this page gives you access to the Autoexit facility and to the display brightness adjustment. The settings on this page do not affect the operating parameters of the generator. The Miscellaneous Page is shown in Figure 3-31.

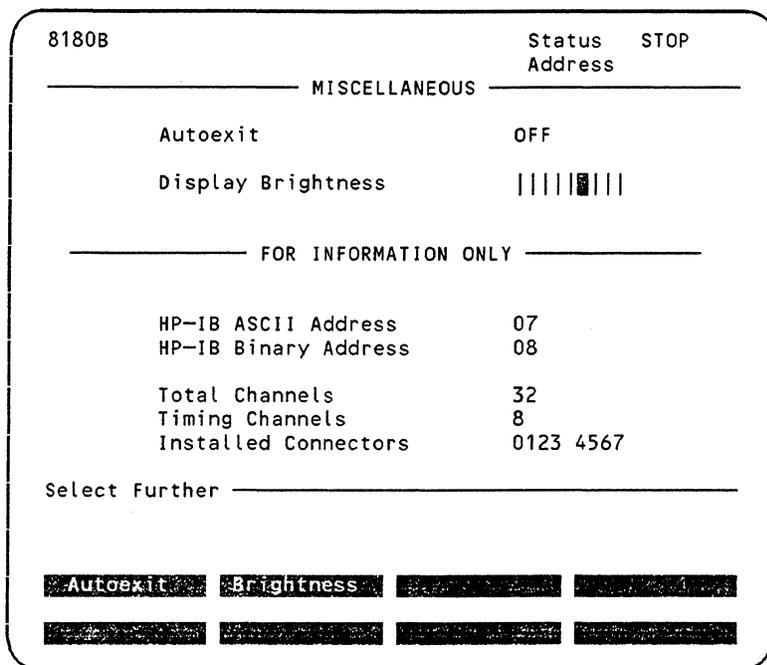


Figure 3-31. Miscellaneous Page

HP-IB ASCII Address

The generator has a Hewlett-Packard Interface Bus connection which enables it to be connected to a computer and operated under program control. The HP-IB ASCII address is used to set an address on this bus when the generator is operated from a computer. The address displayed is the address set on the address switches on the rear panel of the generator. For the information on setting the HP-IB ASCII address as well as for other details, refer to Chapter 7 of this manual, which deals with the generator programming procedures.

HP-IB Binary Address

The address displayed informs you of the setting of the binary address on the Hewlett-Packard Interface Bus. There are no switches on the generator to set this address. The binary address is always one higher than the ASCII address. For further details about the HP-IB binary address refer to Chapter 7 of this manual, which deals with the generator programming procedures.

Total (Installed) Channels

The number displayed tells you how many data channels (RZ and NRZ) are currently installed in your generator (and data generator extender/s when present). The number can range from 8 to 64 in steps of 4 or 8. For further details refer to the Specifications Section in Chapter 1. Figure 3-31 shows 32 channels, which could mean a generator fitted with 8, 12 or 16 channels and an extender unit fitted with 24, 20 or 16 channels. However, from the 'Installed Connectors' field we see that we have a generator with 16 channels and an extender also with 16 channels.

Timing Channels

The number displayed tells you how many RZ channels (variable delay and width) are currently installed in your generator. (The data generator extender/s accept only NRZ channels.) The figure displayed can be 0, 4 or 8. For further details refer to the Specifications Section in Chapter 1.

Installed Connectors

The numbers displayed tell you which connectors are installed. Each connector carries four channels. A fully loaded generator contains four connectors. Each data generator extender can contain up to six connectors. Thus the maximum number of channels accessible via a single data generator is 64. From Figure 3-31 we see that a single extender unit fitted with 16 channels has been added to the generator.

Autoexit

With Autoexit set to ON an Exit automatically occurs following each new entry of a parameter value or operating mode (except via the **INCREMENT** and **DECREMENT** softkeys), returning the display to the previous softkey level. Throughout the softkey menu descriptions in this chapter Autoexit is OFF. If you wish to enable it press **Autoexit** followed by **ON**. The display returns automatically to the previous softkey level. Autoexit is always off after switching on the generator.

Screen Brightness Adjustment

Via the **Brightness** softkey you can alter the brightness of the generator display. The actual adjustment is done by pressing the **INCREASE** or the **DECREASE** softkey as appropriate.

Macro Data Page

3-10 Macro Data Page

The Macro Data Page gives you access to an additional block of data memory consisting of 16 data lines. This memory is totally independent of the main generator memory as far as the data contents are concerned. Any data set up on this page does not effect the generator output until it is transferred to the Data Page using the Copy Macro or Copy Macros features on the Data Page. However, the data channel configuration follows the configuration set on the Output Page or the Data Page. Indeed, you can also modify the generator channel configuration from the Macro Data Page. Recall Standard Set does not affect the data stored on this page. The Macro Data Page is shown in Figure 3-32. Call it up now by pressing PAGES and **MACRO DATA**.

The screenshot shows the Macro Data Page interface. At the top left is the address '8180B'. At the top right are 'Status' and 'STOP Address'. The main area is titled 'MACRO DATA' and contains a table with 16 rows. The first column is 'MACRO' (0-F) and the second is 'STR DATA'. The data in the 'STR DATA' column consists of hexadecimal values: 'F 0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0', '0'. Below the table is an 'Entry' label with a cursor and four sets of arrows. At the bottom are four softkey buttons: 'CURSOR ↑', '← CURSOR', 'CURSOR →', and 'CURSOR ↓'. An 'Edit' softkey is also visible at the bottom right.

MACRO	STR DATA
0	F 0 0000 0000 0000 0000
1	0 0000 0000 0000 0000
2	0 0000 0000 0000 0000
3	0 0000 0000 0000 0000
4	0 0000 0000 0000 0000
5	0 0000 0000 0000 0000
6	0 0000 0000 0000 0000
7	0 0000 0000 0000 0000
8	0 0000 0000 0000 0000
9	0 0000 0000 0000 0000
A	0 0000 0000 0000 0000
B	0 0000 0000 0000 0000
C	0 0000 0000 0000 0000
D	0 0000 0000 0000 0000
E	0 0000 0000 0000 0000
F	0 0000 0000 0000 0000

Figure 3-32. Macro Data Page

Notice that this page has the same appearance as the Data Page except that the softkeys for the Picture up, Picture down and Top Address functions are missing. The missing softkeys are not necessary as the Macro Data memory has only 16 data lines and they are all displayed on the screen.

Cursor Control - Macro Data Page

The horizontal and vertical cursor keys are identical to those on the Data Page. For details refer to 'Cursor Control - Data Page.

Data Editing - Macro Data Page

The data editing facilities on the Macro Data Page are somewhat less comprehensive than those on the Data Page, but then the Macro memory is also very much smaller. Generation of any patterns or setting and clearing channels must be done manually with the help of the cursor control softkeys. Using the **Edit** softkey you can change the channel configuration of the generator using the **Chnl Config** softkey and access the automatic movement function using the **Entry mode** softkey.

Macro Data Page

Auto Cursor Movement - Macro Data Page

Entry Mode selects cursor movement when editing data on the Macro Data Page. Its operation is identical to the Entry Mode function on the Data Page.

Channel Configuration - Macro Data Page

Chnl Config sets the channel configuration of the generator. The configuration as displayed on this page as well as on the Output Page and the Data Page is affected. The Channel Config softkey menu is identical to those on the Data and Output Pages. The operation of all the functions is also identical.

Exercise - Macro Data Edit and Copy

- Recall Standard Set
- Set up an alternating one/zero pattern on segments 2 and 3 between addresses 2 and B
- Clear all data on the Data Page including strobe
- Copy Macros 2-B to line 30

You should have an alternating data pattern at addresses 30 to 39. The rest of the data memory should be filled with zeros.

Chapter 4

Analyzer Operation

4-1 Introduction

This chapter is divided into ten sections, of which Sections 4-4 to 4-10 are organized around the seven main Operating Pages of the 8182A/B Analyzer. Each main Page is a starting point to other Pages on which selections, entries etc. can be made with the use of softkeys. The various softkeys are described using example settings.

Each section gives a full description of all softkeys, allowed entries and setting ranges. Any restrictions and the likely error messages are also included.

The 8182A and 8182B Data Analyzers have been designed specifically to complement the 8180A and 8180B Data Generators respectively, for parametric evaluation of multi-channel hardware at clock rates up to 50 MHz. High resolution timing and level measurements are essential for such tests. The A version has a memory depth of 1024 words, the B version has a memory depth of 16384 words.

In addition to providing state diagrams and timing diagrams, the analyzer generates an error map for rapid verification of device functions and performance, and provides a real-time compare mode for detection of intermittent failures.

4-2 Data Analyzer Block Diagram and Internal Operating Concept

Figure 4-1 is the block diagram of the data analyzer. The analyzer contains the following parts:

- input comparators which determine an input level to be "1", "0", or "intermediate",
- triggering circuits which indicate the onset of data capture
- a high speed memory to store sampled data or to hold compare data for real time compare
- a low speed Received Data memory to hold recorded data
- a low speed Expected Data memory to hold reference data
- timing circuits which precisely control the duration of time windows in which data must be sampled or compared
- a CPU for software related control functions
- an HP-IB interface for communication with a controller
- a keyboard for data and parameter entry
- a display.

The analyzer can be driven by an internal or an external clock. The data memory provides a memory depth of 16384 (1024) bits for each channel.

The basic data analyzer contains 8 input data channels. A fully loaded analyzer contains 32 input data channels. That particular configuration is obtained by adding three options 001 (each with eight data channels). A full description of the analyzer options is given in Chapter 1.

Introduction

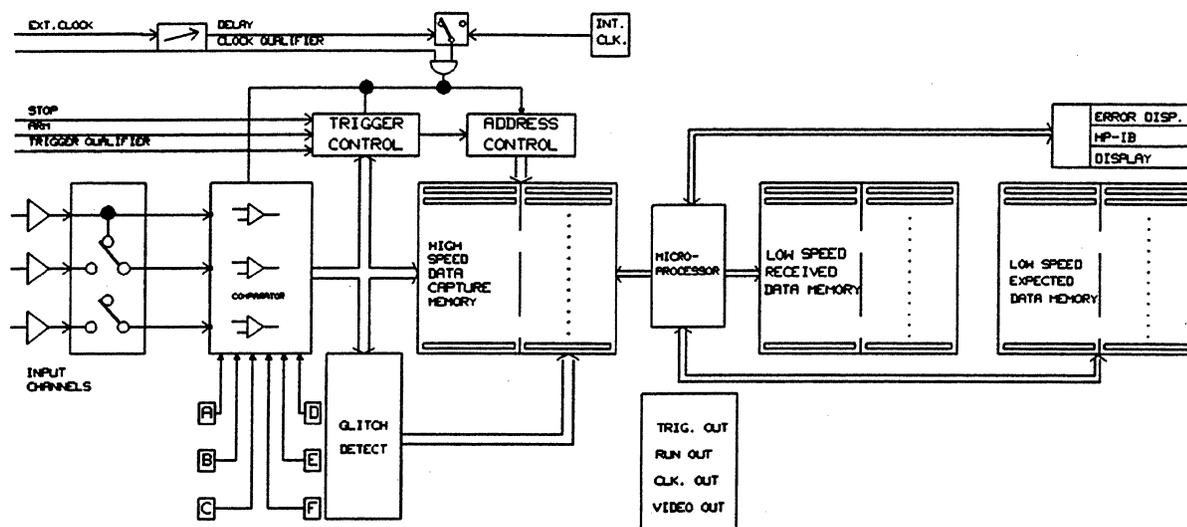


Figure 4-1. Block Diagram of the Data Analyzer

The analyzer has two basic modes of operation. The Standard Analysis Mode, in which data is sampled at programmable points in time within the clock period, and the Real Time Compare Mode, in which data is compared against a reference pattern during a programmable time window. The Standard Analysis Mode in turn splits up into the Trigger Start Analysis Mode and the Trigger Stop Analysis Mode. The two modes differ by the triggering conditions and can be individually called up, as we shall see a little later in Section 4-4, Control Page and Operating States. First we shall discuss the Standard Analysis Mode, followed later by the Real Time Compare Mode.

Let us use the analyzer block diagram to see what the instrument does in the Standard Analysis Mode. The instrument runs synchronously with the external clock when the trigger control conditions are true, and it samples data during the active slope of the clock (or after the active slope when the clock delay is not equal to zero).

The sampled data is read into a high speed (ECL) memory. After data has been captured, it is compared with data stored in a low speed (CMOS) reference memory. The reference data can be obtained from a known good device, or entered and edited manually, or up-loaded via HP-IB. The comparison is done in the internal microprocessor using a software compare routine.

Synchronous Sampling

At this stage we need to discuss the difference between *synchronous* and *asynchronous* analysis techniques.

If a data analyzer uses a clock running synchronously with the Device Under Test (DUT) to strobe data into its memory (analyzer clock signal), as shown in Figure 4-2, the measurement is said to be synchronous with the DUT. If a data analyzer uses a clock source which is not synchronized with the DUT, the measurement is said to be asynchronous with the DUT.

Introduction

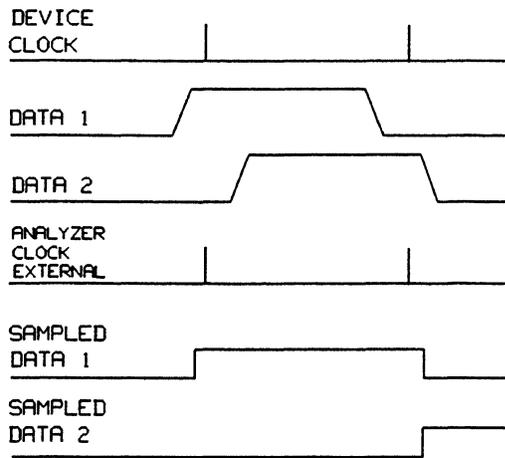


Figure 4-2. Synchronous Sampling of Data

Synchronous analysis is usually more closely associated with software (state analysis). This is because each clock cycle corresponds to a specific logic state and thus describes the functional behavior of the device. On the other hand, asynchronous analysis is more closely associated with hardware (timing analysis). With this technique, incoming data can be sampled at a clock rate several times faster than the device clock cycle time. This method provides the user with rudimentary parametric information (for example edge A occurred before edge B).

Asynchronous Sampling

When sampling asynchronously, the resolution is inversely proportional to the internal clock period. Although the resolution improves with higher sampling rates, the time window available for analysis becomes proportionally narrower (i.e. twice the sampling rate yields a time window half as long). Asynchronous sampling is shown in Figure 4-3.

High sampling rates necessitate stringent hardware requirements. For example, a resolution of 5 ns requires a sampling rate of 200 MHz.

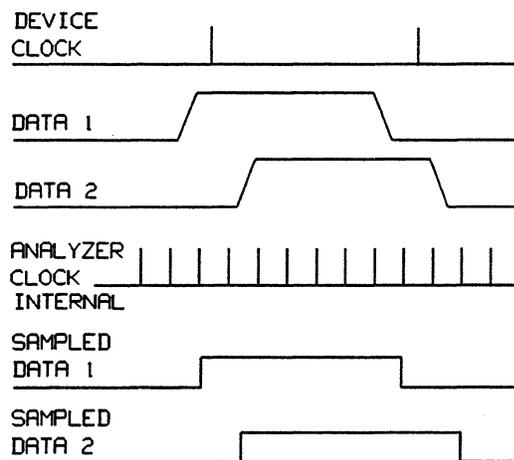


Figure 4-3. Asynchronous Sampling of Data

Introduction

Variable Sampling Point

The 8182A/B Data Analyzer, although designed for digital hardware analysis, will primarily be operated synchronously rather than asynchronously. Nevertheless, the analyzer offers excellent timing resolution, with a best case of 100 ps.

The key to achieving this resolution is the use of HP-designed custom IC's. These special integrated circuits permit precise determination of sampling or real time compare time windows. This is accomplished either by precisely delaying the sampling point of the analyzer after the external clock signal edge, see Figure 4-4, or by defining a precise compare window during which bit levels are monitored for stability. This method achieves high timing resolution, even while operating in synchronous mode.

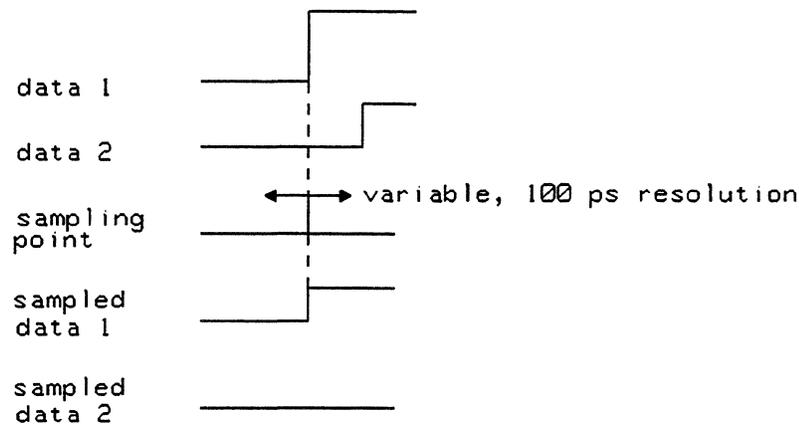


Figure 4-4. Variable Sampling Point Method

Synchronous sampling with adjustable Sampling Point Delay down to 100 ps permits high resolution timing measurements. Note that the resolution is not a function of the sampling rate. All channels are equally suited for high resolution measurements.

Wiring Diagram

In order for the test signals to reach the analyzer input, connect the generator outputs directly to the analyzer inputs using generator data interconnecting cables and analyzer data active probes, as shown in Figure 4-5. Then connect generator Clock 1 output directly to the analyzer Clock input using the generator clock interconnecting cable and analyzer clock active probe. Finally, connect the generator Strobe output directly to the analyzer BNC "ARM" input using a 15409A Pod to BNC adapter.

This setup allows us to study known generator signals without having to worry at this stage about signal changes produced by a test device. We use generator Clock 1 to clock the analyzer. The strobe signal from the generator arms the analyzer for the next analysis cycle. Analyzer arming is a rather complex subject which we will cover later on in this chapter.

Introduction

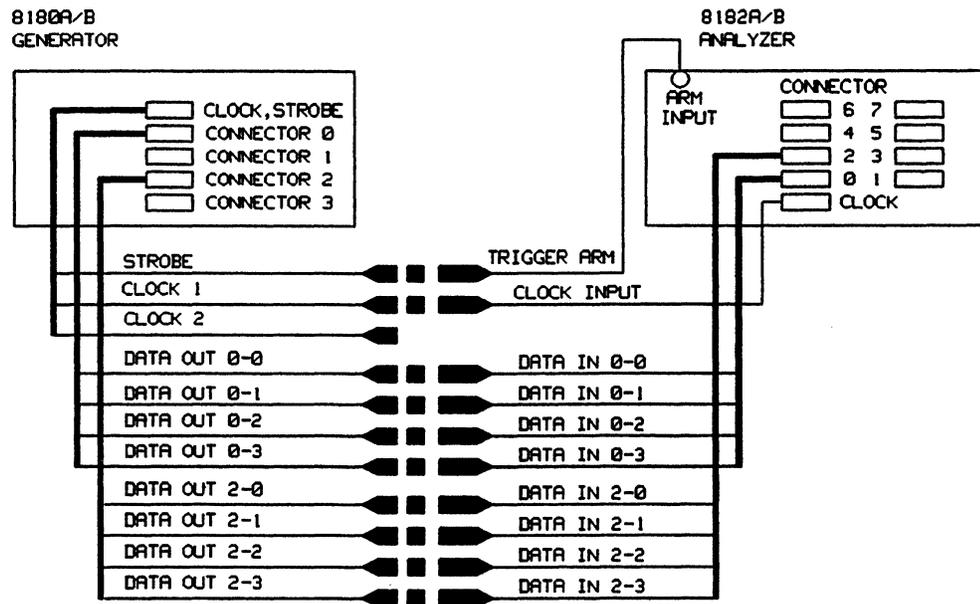


Figure 4-5. Connecting the Analyzer to the Generator

Setting up Initial Conditions at Generator

Before we begin a detailed discussion of the 8182B Data Analyzer, we should set up a specific set of conditions at the generator, so that we have clearly defined signals at the input to the analyzer.

Set the following on the generator:

- Recall Standard Set
- First Address: 00000
- Last Address: 00031
- Clock 1 Delay: 20 ns
- All output levels TTL (data, clock, strobe)
- Clear all data
- Up-counter on four channels of Connector 0
- Down-counter on four channels of Connector 1
- Strobe at address 00000 to 1

4-3 Front Panel Controls and Operating Concept

Before turning on the analyzer we should spend a moment on the instrument front panel layout and its operating concept. This section explains the main features of the analyzer front panel. Figure 4-6 shows the front panel controls.

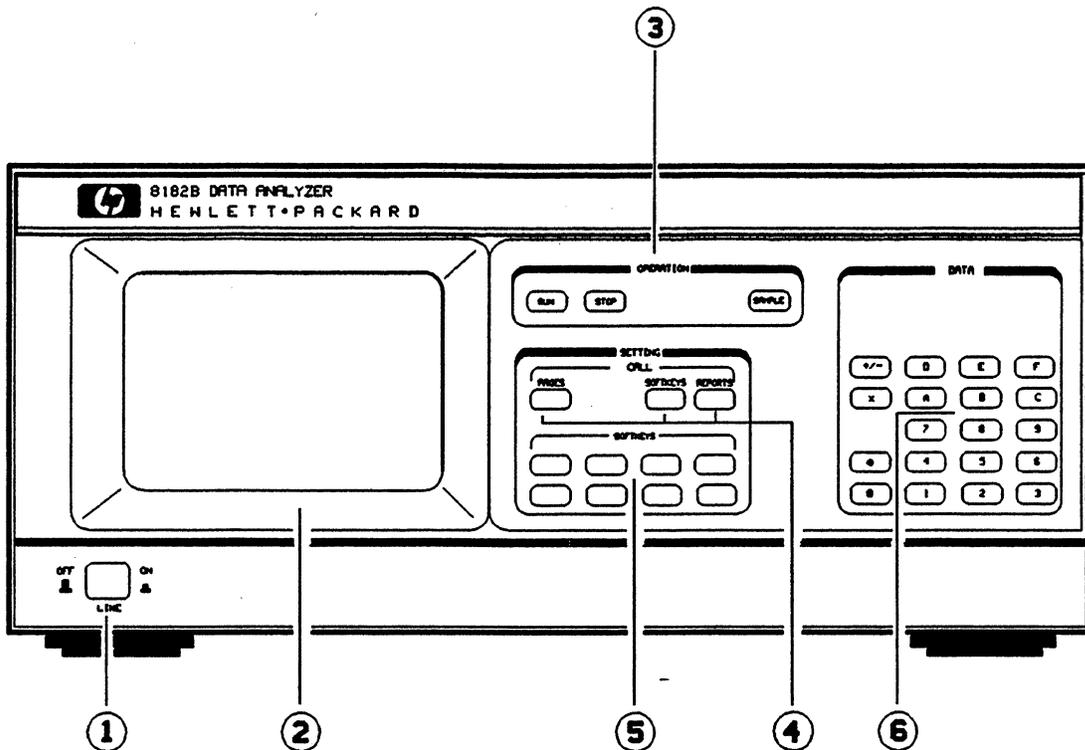


Figure 4-6. Data Analyzer Front Panel

1. Mains power ON/OFF pushbutton with ON indicator lamp.
2. CRT display. See below for Display Format.
3. **OPERATION** keys are used to run and stop the instrument and to manually sample the data word currently on the inputs. The keys are explained in detail at the end of Section 4-4 'Control Page and Operating States'.
4. **CALL** keys are a sub-group consisting of the **PAGES**, **SOFTKEYS** and **REPORTS** keys. They are a part of a group called **SETTING** keys. The **PAGES** key is discussed throughout this chapter. An explanation of the **SOFTKEYS** and **REPORTS** keys is given in an exercise on the State List Page.
5. **SOFTKEYS** are a sub-group of eight keys used to set and modify all analyzer parameters. They are also part of a group called **SETTING** keys. The **SOFTKEYS** are discussed throughout this chapter.
6. **DATA** keys permit entry of front panel data in binary, octal, decimal or hexadecimal modes. They are also used for numeric value entry of measurement parameters such as frequency, delay, width, and so on. Only those keys currently appropriate are enabled. This prevents making non-meaningful entries. The **DATA** keys are discussed throughout this chapter.

Front Panel Controls and Operating Concept

Display Format

The analyzer not only looks like the generator. It also features the same operating concept. This will be evident later when we turn the analyzer on.

The display is divided into three areas. At the top is status information, at the bottom are the softkey labels (together with parameter entry information where appropriate). The center part of the display, called the Report area, is dedicated to analyzer settings or data. As an example, refer to Figure 4-7 showing the Control Page.

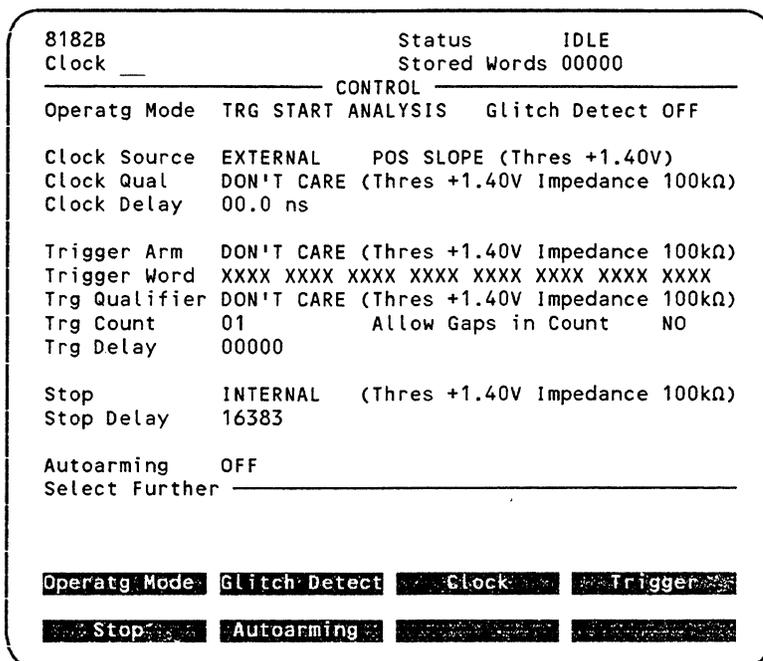


Figure 4-7. Example of the Display Format showing the Control Page

Page Concept

The operating concept of the analyzer is based on seven main menu pages accessible through softkeys. As we shall see later, under certain circumstances two of the main pages are not relevant and therefore not available. The main pages have other pages behind them which become available once a softkey selection is made, resulting in layered softkey menus. Figures 4-8 and 4-9 demonstrate this concept.

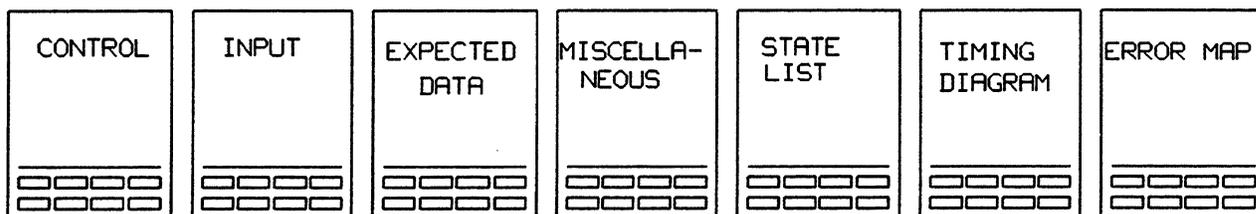


Figure 4-8. Analyzer Main Pages

Front Panel Controls and Operating Concept

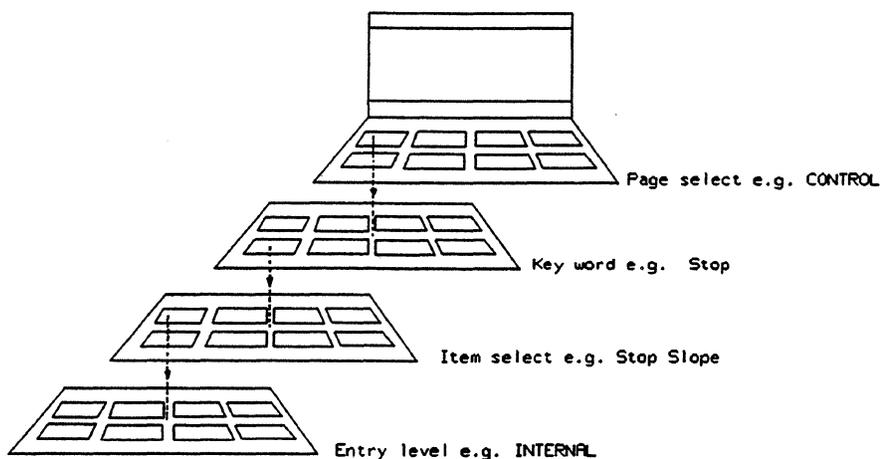


Figure 4-9. Softkey Operating Concept

The menu-driven operation is identical to that of the generator, so you will be already familiar with it. You should nevertheless do the simple exercise which follows in just a moment.

Switching On the Analyzer

Switch on the analyzer by pressing the ON/OFF button. The instrument always performs a power-up self test on switch-on lasting about nine seconds, after which the main pages become available on the softkeys. The Status is always IDLE. All settings and data remain as they were prior to switch off. Back-up batteries keep this information stored for approximately 1 week.

NOTE

If the power up self test detects a fault the analyzer displays the type of error on the screen and the softkeys remain blank except for the top left hand one - **CONTINUE**. If you press this key operation of the analyzer resumes, albeit with the fault present. The presence of a fault may or may not prevent you working with the analyzer. This depends on the nature of the fault. In any case you should refer to Section 2-2 of this manual.

Exercise - Softkey Operation

- **MISCELLANEOUS**
- **Recall**
- **Standard Set**
- **EXECUTE**

The fastest way to bring the instrument to a known state is to call up the standard parameter set; this is what we will do next. Push the **MISCELLANEOUS** softkey. This brings up the corresponding display, and the softkeys now offer further selections. One option is **RECALL**. This offers yet another set of options. One of these is **Standard Set**. Once this softkey is pushed, the command must be confirmed by pressing **EXECUTE**. All parameters are now set to the values as listed in Table B-1 in Appendix B.

Front Panel Controls and Operating Concept

NOTE

All screens in the subsequent sections showing main pages give values following the execution of the Recall Standard Set command.

Pushing the "PAGES" key returns you to the main PAGES menu.

Notice that softkeys which have additional level(s) of softkey menus behind them (not main page softkeys) are displayed in lower case letters. Softkeys which are at the lowest level, i.e. those performing actual functions are displayed in upper case letters. There are no additional softkey menus behind these keys.

This example which activates the standard settings should show you how easy it is to operate the analyzer.

Next we'll go through all seven pages of the analyzer in detail. To start with, call up the highest decision level by pushing the PAGES key.

Control Page and Operating States

4-4 Control Page and Operating States

The first page is the Control Page. It provides access to the main control and configuration functions of the analyzer. It is essential to review all the parameters on this page before attempting to make a measurement. If the parameters are not set correctly, the analyzer will not perform the measurements that you expect.

Call up the Control Page by pressing **CONTROL**.

The softkey labels at the bottom of the display now indicate which parameters are accessible. Let us now go through the capabilities in detail. Figure 4-10 shows the functions of the analyzer which are accessible through the Control Page.

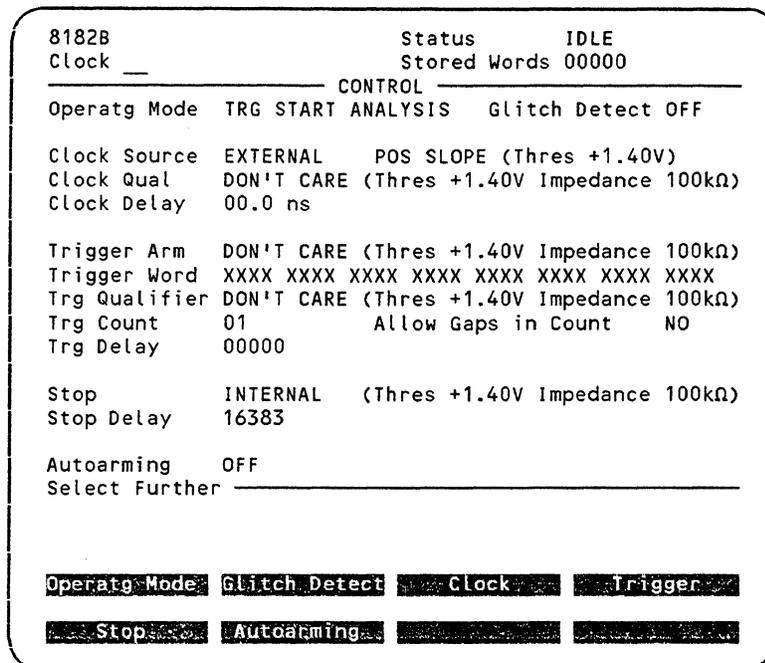


Figure 4-10. Analyzer Control Page

Operating Modes

To access the operating modes of the 8182A/B data analyzer press the softkey **Operatg Mode**. The analyzer offers three modes.

- Trigger Start Analysis for recording post-trigger data (trigger event start analysis).
- Trigger Stop Analysis for recording pre-trigger data (trigger event stop analysis) and post-trigger data with trigger delay.
- Trigger Start Compare for real time comparison of incoming data against previously stored 'expected' data (trigger event start compare).

The first key decision that must be made when configuring the analyzer is to choose either analysis or compare. If analysis is selected, then either trigger start or trigger stop analysis must be specified. Before we proceed to selecting an operating mode, we need to discuss each one in detail. If you have previously recalled the Standard Set, the selected operating mode will be Trigger Start Analysis.

Control Page and Operating States

Trigger Event Start Analysis

Trigger Start Analysis mode is used for post-trigger data capture and analysis. The mode is called by the **TRG STRT ANAL** softkey. In this mode the instrument will go to the ARMED state following entry of the RUN command. It will go active (i.e., sampling data) when the trigger conditions become true. When the stop conditions become true, the analyzer will go back to the IDLE state. This mode of operation is shown in the simplified timing diagram in Figure 4-11. The trigger and stop conditions will be discussed later under their respective headings.

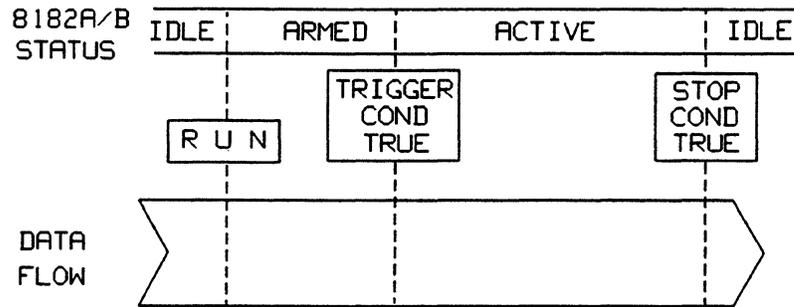


Figure 4-11. Timing Diagram for Trigger Event Start Analysis

A different representation of this is shown in the State Diagram in Figure 4-12.

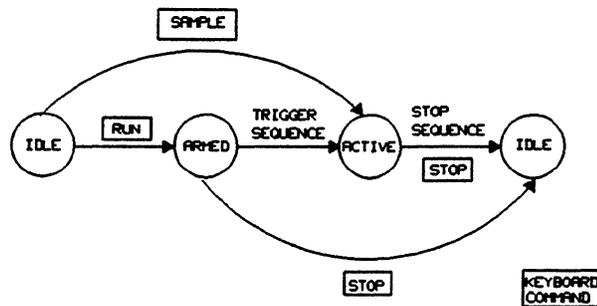


Figure 4-12. State Diagram for Trigger Event Start Analysis

A maximum of 16384 (1024) words can be stored in the analyzer memory. Memory addressing is arranged to suit the data capture requirements as can be seen from Figure 4-13. A real addressing system is used so that the data word stored at the trigger event (that is the first stored word) is stored at address 00000 and each successive sampled word is stored at an ascending address until the stop sequence is encountered, or until the capture memory is filled. Data streams longer than the memory size can also be handled, but require a controller to provide the data handling facilities. Refer to Chapter 8 of this manual, or to the System Software Manual if you are running under the HP System Software.

Control Page and Operating States

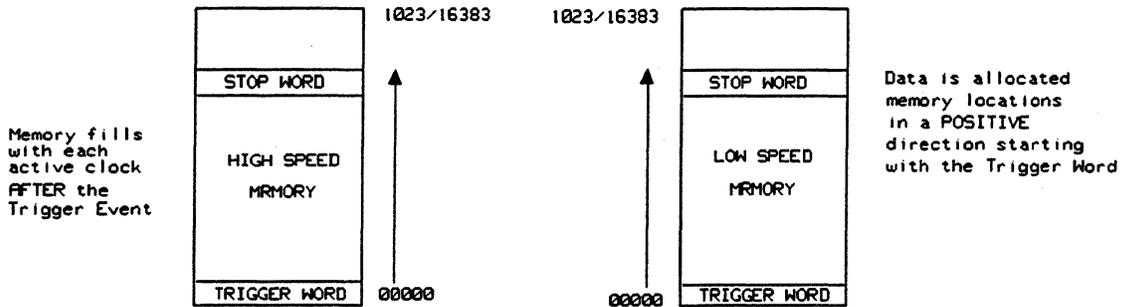


Figure 4-13. Memory Real Addressing System

The trigger start analysis mode is used mainly for logic analysis or for device characterization. In this mode the analyzer can be set up to look at certain parts of a data stream in order to debug some hardware or software. An example to illustrate such an application is included later, after we have covered other important parameters.

Trigger Event Stop Analysis

The Trigger Start Analysis mode is used for pre-trigger data capture and analysis. It is called by the **TRG STOP ANAL** softkey. In this mode the instrument will go to the ARMED state following entry of the RUN command. From the ARMED state, it will become ACTIVE at the first occurrence of an external clock pulse. The analyzer will remain ACTIVE, sampling data until the trigger conditions are met, after which it will go back to the IDLE state. This mode of operation is shown in the simplified timing diagram in Figure 4-14, which illustrates the cumulative effect of the various trigger stop conditions determining the size of the data capture window. The trigger conditions will be discussed later under their respective headings.

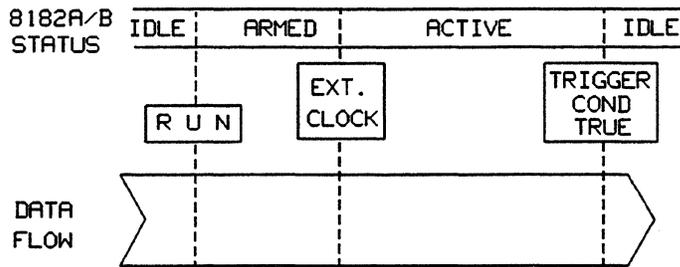


Figure 4-14. Timing Diagram for Trigger Event Stop Analysis

A different representation of this is shown in the State Diagram in Figure 4-15.

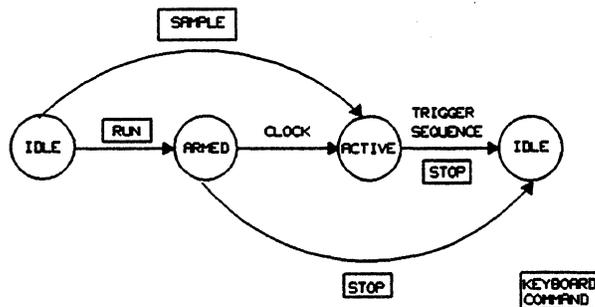


Figure 4-15. State Diagram for Trigger Event Stop Analysis

Control Page and Operating States

A maximum of 16384 (1024) words can be stored in the analyzer memory. Memory addressing is arranged to suit the data capture requirements as can be seen from Figure 4-16. A relative addressing system is used whereby the data word stored at the trigger event (that is the last stored word) is allocated address -00000 and each word stored prior to the trigger event is allocated an address accordingly. For example, the tenth word prior to the trigger event is located at address -00010. As we shall see later, the displayed address on the State List, Timing Diagrams and Error Map pages corresponds to its word's relative position to the trigger event.

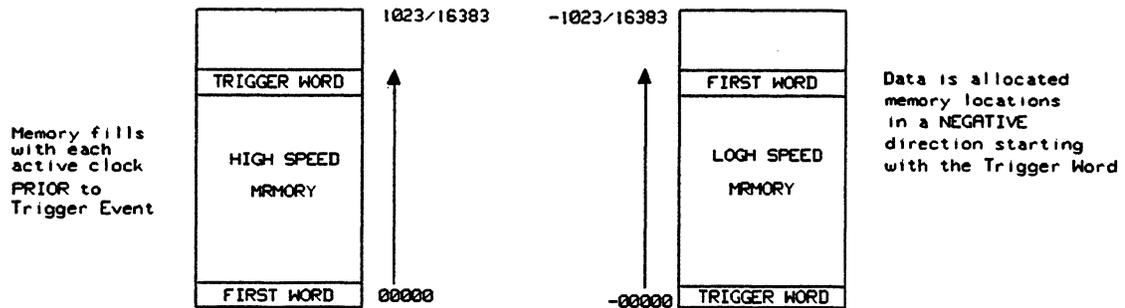


Figure 4-16. Memory Relative Addressing System

Trigger stop analysis mode is also used mainly for logic analysis. In this mode the analyzer can be set up to look at certain parts of a data stream in order to debug some hardware or software. An example to illustrate such an application is included later, after we have covered other important parameters. Of considerable importance in Trigger Stop Analysis is the role of Trigger Delay, which is explained later under its heading.

It is important to realize that when this operating mode is employed and no use of Trigger Delay is made (i.e. it is set to 00000), the generator cannot be set to its free-running mode AUTO. This is because the analyzer needs a certain amount of time to perform a software comparison of the captured data and update the display, which can occur only *after* the stop conditions have been received. During this time the analyzer ignores incoming data. Immediately after it completes these tasks the analyzer goes active again on the first clock pulse it sees, which could be anywhere in a cycle. The analyzer therefore cannot remain in synchronism with the generator and the displayed data is meaningless. The generator should be set to GATED, or SINGLE mode and started from an external source via the RUN,GATED input, or from a controller via HP-IB.

If however you wish to capture a block of data (16384 or 1024 words long, depending on analyzer version) from a long data stream, you can do so only if the generator is set to AUTO. For further explanation refer to the subsection Trigger Delay and to the last example on triggering entitled Capturing a 16384 (1024) Word Data Block with Trigger Delay.

Trigger Event Start Compare

Trigger Event Start Compare mode is called by the **TRG-START-COMP** softkey. In this mode the instrument is set to perform real time comparison of incoming data with data previously stored in memory. No data capture is performed. The Trigger Event Start Compare mode is used mainly for device testing because of its high speed (and throughput) and its ability to detect sporadic errors. The Trigger Event Start Compare mode is similar to the Trigger Start Analysis mode with respect to the triggering conditions. It is the active state which differentiates the two.

Control Page and Operating States

Trigger Start Compare is rather a complex subject and requires prior knowledge of certain other features of the analyzer. We are therefore going to deal with it later in a section entitled Real Time Compare Mode.

Glitch Detection

In either of the analysis modes glitch detection capability is provided on all channels. When enabled, two or more data signal transitions between two consecutive sampling points (that is one clock period) are interpreted as a glitch. Glitch detection operates in Single or Dual Threshold mode. Thus a glitch can occur on a single, upper or lower threshold. The threshold function is explained on the Input Page. A detected glitch is stored in memory and can be displayed on any of the three analysis pages State List, Timing Diagrams and Error Map. A glitch is shown at the next or just after the next sampling point (that is clock edge), depending on which analysis page you select. Figure 4-17 shows a waveform with a glitch occurring between the second and the third clock edge. When glitch detection is enabled the maximum data memory is halved to 8192 (512) words. Glitch detection is not available when in the Trigger Start Compare mode (see the section entitled Real Time Compare Mode at the end of this chapter).

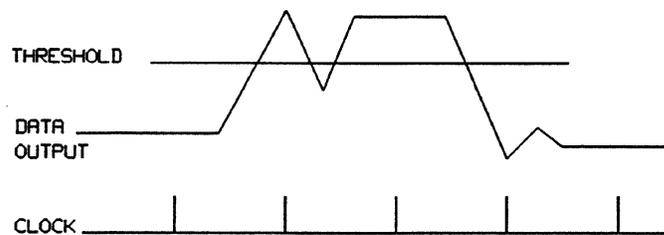


Figure 4-17. Glitch Detection

After a Recall Standard Set has been performed, glitch detection is set to OFF. To enable it press the softkey **Glitch Detect** and then **ON**. Exit the menu by pressing **EXIT**. Similarly, **OFF** disables glitch detection.

There are some examples on glitch detection and displaying glitches later on when we deal with the analysis pages.

Clock Control

The softkeys that can be called up via the **Clock** softkey deal with the various parameters affecting the main analyzer clock. If you have previously recalled the Standard Set, you will get the following softkey menu after pressing the **Clock** softkey:

```
Clock Source  Clock Slope  Clock Thres  Clock Qual
Clock Delay  EXIT
```

The clock softkey menu is dependent on the clock source and after a Recall Standard Set the clock source is external. If the internal clock source had previously been selected, the above softkey menu would appear as follows:

Control Page and Operating States

Clock Source Clock Qual
Clock Period EXIT ↑

Clock Source

Clock Source allows you to select the analyzer clock. The analyzer can use either an internal or an external clock. When set to internal clock, the analyzer samples generator data asynchronously, as its clock is independent of the generator clock. When using the internal clock to sample incoming data, it is important to sample at least at a minimum of twice the frequency of the incoming data, otherwise the results of the analysis will be meaningless. Refer to Section 4-2 which discusses both synchronous and asynchronous sampling. Displaying synchronously and asynchronously sampled data will be covered on the analysis pages State List, Timing Diagrams and Error Map.

EXTERNAL selects an external clock as the clock source for the analyzer. This will normally be one of the two generator clock channels and means that the analyzer samples synchronously with the generator (and any device that is being investigated). However, the clock can come from any accurate source, such as a pulse generator, in which case the analyzer will sample asynchronously.

INTERNAL selects the analyzer's own internal clock as the clock source, which means the analyzer will sample asynchronously.

Clock Slope

Clock Slope allows you to select the clock edge to be used as the sampling point. The softkey appears when the clock source is *external*.

POS. SLOPE selects the clock leading edge as the sampling point.

NEG. SLOPE selects the clock falling edge as the sampling point.

BOTH SLPS selects both the leading edge and the falling edge of the clock as sampling points. Note that in this case the sample rate is doubled, so ensure the time between slopes is greater than or equal to 20 ns.

Clock Threshold

Clock Thres permits setting the input threshold level for the external clock. The softkey appears when the clock source is *external*.

INCREMENT increments the current input threshold level for external clock in 10 mV steps.

DECREMENT decrements the current input threshold level for external clock in 10 mV steps.

TTL (+1.40V) enters a TTL level directly.

ECL (-1.29V) enters an ECL level directly.

Alternatively, you can enter the numerical value in volts in the range of +10 V to -10 V. You must then press the **VOLT** key to terminate the entry.

Control Page and Operating States

Clock Qualifier

Clock Qual allows you to qualify (gate) the clock signal with some other signal. The qualifier signal is applied to the rear panel CLOCK QUALIFIER input BNC connector. Active signal level, input threshold and input impedance can be all set via softkeys. The **Clock Qual** softkey appears whether the clock source is either *internal* or *external*.

Level selects the active level of the gating signal. The clock can be enabled when the level is high by pressing the softkey **HIGH LEVEL**, or when the level is low by pressing the softkey **LOW LEVEL**. When **DON'T CARE** is selected the clock is always enabled.

Threshold sets the threshold voltage level at the CLOCK QUALIFIER input BNC connector. After entering the numerical value in volts in the range of +10 V to -10 V, you must press the **VOLT** key to terminate the entry. Alternatively you can use the **INCREMENT** or **DECREMENT** keys, which operate in 10 mV steps. The **TTL (+1.40V)** or **ECL (-1.29V)** softkeys allow you to set the threshold level to a TTL or ECL level directly, without having to use the DATA keys.

Impedance sets the input impedance of the CLOCK QUALIFIER input. The available choices are **50Ω** and **100kΩ**. After a Recall Standard Set the input impedance is set to 100 kOhms.

Clock Delay

Clock Delay allows you to delay the analyzer sampling point with respect to the external clock. The softkey appears only when the clock source is external.

INCREMENT increments the clock delay.

DECREMENT decrements the clock delay.

Alternatively, you can enter a numerical value directly, using the DATA keys, in the range of 00.0 ns to 1.00 s. You must then press one of the additional scaling keys **SECONDS**, **MILLISEC**, **MICROSEC** or **NANOSEC** to terminate the entry. The delayed clock signal is available at the rear panel CLOCK output BNC connector.

The clock delay feature is a powerful tool for measuring timing parameters of devices and circuits. It will be used later in a measurement example to determine the propagation delay of a test device.

Clock Period

Clock Width allows you to set the period of the internal clock. The softkey appears when the clock source is *internal*.

INCREASE increases the clock period in a 1, 2, 5 sequence (e.g. 100 ns, 200 ns, 500 ns).

DECREASE decreases the clock period in a 1, 2, 5 sequence (e.g. 500 ns, 200 ns, 100 ns).

FAST INCREASE increases the clock period in a decade sequence (e.g. 1 ms, 10 ms, 100 ms).

FAST DECREASE decreases the clock period in a decade sequence (e.g. 100 ms, 10 ms, 1 ms).

It is not possible to make a direct entry via the DATA keys.

Control Page and Operating States

Trigger Control

The trigger condition determines the start or the stop of an analysis/compare sequence, thus ensuring the analyzer operates in synchronism with the generator as far as the data stream is concerned. The analyzer can still be clocked asynchronously (using the external clock). Synchronous clocking and synchronous analysis/compare are two different things.

A number of different trigger conditions can be employed and combined together to obtain the desired overall trigger condition. Setting up the trigger conditions is a very important part of the overall setup, since they influence to a large degree what the analyzer measures. The softkey **Trigger** accesses the trigger-related functions of the analyzer. On pressing it the following choices are offered:

Trigger Arm **Trigger Word** **Trg Qualifier** **EXIT**
Trg Count **Allow Gaps** **Trg Delay** **EXIT**

Trigger Arming

Trigger Arm provides an edge-active trigger condition using a signal applied to the rear panel TRG ARM input BNC connector. Active slope of the trigger signal, as well as voltage threshold at the TRG ARM input and its input impedance can be designated.

Slope selects the active slope (edge) of the trigger input signal. You can select the positive edge or negative edge by pressing the **POS SLOPE** or **NEG SLOPE** softkey respectively. If you press the **DON'T CARE** softkey, the analyzer will trigger on the first clock edge that comes along. This is not a very useful method of triggering the analyzer as it works only at extremely low frequencies. The analyzer will therefore lose synchronization unless some other trigger condition has been specified.

Threshold sets the threshold voltage level of the TRG ARM input BNC connector. After entering the numerical value in volts in the range of +10 V to -10 V, you must press the **VOLT** key to terminate the entry. Alternatively you can use the **INCREMENT** or **DECREMENT** keys, which operate in 10 mV steps. The **TTL (+1.40V)** or **ECL (-1.29V)** softkeys allow you to set the threshold level to a TTL or ECL level directly, without having to use the DATA keys.

Impedance sets the input impedance of the TRG ARM input. The available choices are **50 Ω** and **100k Ω** . After a Recall Standard Set the input impedance is set to 100 kOhms.

Trigger Word

Trigger Word provides a method of triggering the analyzer when a certain preset word is encountered in the data stream. In other words it provides a pattern recognition trigger condition. When this softkey is pressed the current trigger word and the current channel configuration are displayed in lines 21 to 23, just above the softkeys. The Trigger Word in line 11 in the Report Area moves to the left to line up with the channels and the Trigger Word in the lower part of the screen.

The trigger word can be encoded in binary, octal or hex, depending on the code setting on the Input, Expected Data, State List, Timing Diagrams or Error Map Pages. After a Recall Standard Set the Trigger Word is set to "don't care", that is all X's. You can change the Trigger Word with the DATA keys and the arrow softkeys. After

Control Page and Operating States

each entry from the Data keys the cursor moves one field to the right, unless you have reached the rightmost field or have pressed the **HOLD CURSOR** softkey.

-  Moves the cursor a single field to the right.
-  Moves the cursor a single field to the left.
-  Moves the cursor all the way to the left.
- HOLD CURSOR** Stops the cursor moving to the next field on the right after an entry has been made using the Data keys. To cancel the hold, exit from this menu.

If the logic polarity is changed via the **NORMAL** / **INVERSE** softkeys on the Input, Expected Data, State List, Timing Diagram or Error Map Pages, then this word is automatically changed to correspond to the new polarity. If you have duplicate channels in a segment and you change the setting of that channel in the Trigger Word, then the other channel/s will also get changed. The same follows for identical channels also used in other segments.

If you have such a set-up on the display and have also set some of the segments to codes other than binary, (for instance octal or hex), a small x appears in the Trigger Word in a place where some channels in a group of channels contained in an octal or a hex code are set to "don't care", while the others are given a certain level. As a general rule, duplicate channels in a segment, or multiple channel definitions should be avoided.

The small x can however appear as the result of a "legal" setting, where the Trigger Word displayed in binary code is defined a bit at a time and where some bits in a segment are set to a 1 or a 0, while others in the same segment are set to an X (don't care). The small x appears when this segment is later encoded in octal or hexadecimal.

As an example of this, let us assume that we have a channel configuration and a Trigger Word as shown in Figure 4-18. The first and second segments contain 12 channels each, the third and fourth segments contain 4 channels each. The code is binary.

```

8182B                               Status      IDLE
Clock  _                            Stored Words 00000
-----
Operatg Mode TRG START ANALYSIS  Glitch Detect OFF

Clock Source EXTERNAL  POS SLOPE (Thres +1.40V)
Clock Qual   DON'T CARE (Thres +1.40V Impedance 100kΩ)
Clock Delay  00.0 ns

Trigger Arm   DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trigger Word XXXX10XXXXX0 XX1XX011XX01 X00X XXXX
Trg Qualifier DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trg Count    01          Allow Gaps in Count  NO
Trg Delay    00000

Stop         INTERNAL  (Thres +1.40V Impedance 100kΩ)
Stop Delay   16383

Autoarming   OFF
ENTER NEW VALUE
Connector    777766665555 444433332222 1111 0000
Channel      321032103210 321032103210 3210 3210
Trg Word     XXXX10XXXXX0 XX1XX011XX01 X00X XXXX
HOLD CURSOR  
HOLD CURSOR  EXIT 

```

Figure 4-18. Trigger Word Before Change

Control Page and Operating States

If the code for the first segment is changed to say octal, the second segment to hex, the third to octal and the fourth to hex, we will get small x's appearing in the Trigger Word as shown in Figure 4.19. The change is done using the **Chnl Config** and **Code/Polarity** softkeys, which can be accessed on one of the following pages: Input, Expected Data, State List, Timing Diagrams and Error Map.

```

8182B                               Status      IDLE
Clock  ___                          Stored Words 00000
----- CONTROL -----
Operatg Mode TRG START ANALYSIS      Glitch Detect OFF

Clock Source  EXTERNAL      POS SLOPE (Thres +1.40V)
Clock Qual    DON'T CARE (Thres +1.40V Impedance 100kΩ)
Clock Delay   00.0 ns

Trigger Arm   DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trigger Word  XXXx          xxx  x  XX
Trg Qualifier DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trg Count     01            Allow Gaps in Count  NO
Trg Delay     00000

Stop          INTERNAL      (Thres +1.40V Impedance 100kΩ)
Stop Delay    16383

Autoarming    OFF
ENTER NEW VALUE -----
Connector     777766665555 66 5 5555 2222 1111 0000
Channel       321032103210 10 3 3210 3210 3210 3210
Trg Word      XxXx          xxx  x  xx
HOLD CURSOR  ←→
                ←→
                ←→  EXIT ↑↑
  
```

Figure 4-19. Trigger Word After Change

Trigger Qualifier

Trg Qualifier allows you to qualify (gate) the trigger signal with some other signal, thus providing extra control of the trigger condition. The qualifier signal is applied to the rear panel TRG QUAL input BNC connector. Active signal level, input threshold and input impedance can be all set via softkeys.

Level selects the active level of the gating signal. The trigger can be enabled when the level is high by pressing the softkey **HIGH LEVEL**, or when the level is low by pressing the softkey **LOW LEVEL**. When **DON'T CARE** is selected the trigger is *always qualified*.

Threshold sets the threshold voltage level of the TRG QUAL input BNC connector. After entering the numerical value in volts in the range of +10 V to -10 V, you must press the **VOLT** key to terminate the entry. Alternatively you can use the **INCREMENT** or **DECREMENT** keys, which operate in 10 mV steps. The **TTL (+1.40V)** or **ECL (-1.29V)** softkeys allow you to set the threshold level to a TTL or ECL level directly, without having to use the DATA keys.

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Impedance

sets the input impedance of the TRG QUAL input. The available choices are **50 Ω** and **100k Ω** . After a Recall Standard Set the input impedance is set to 100 kOhms.

Trigger Count

Trg Count

determines how many times the qualified Trigger Word must occur prior to triggering. Refer to a triggering example near the end of this section.

Trigger Count is set by incrementing or decrementing the current value using the **INCREMENT** or **DECREMENT** softkeys, or by entering an integer value in the range of 01 to 16 using the DATA keys.

Trigger Word Gaps

Allow Gaps

determines whether the qualified Trigger Word must occur on consecutive clock pulses. Refer to a triggering example near the end of this section. If **Allow Gaps** is set to **YES**, the Trigger Word has to occur the number of times defined by Trigger Count, but not necessarily consecutively. If it is set to **NO**, the Trigger Word has to occur the correct number of times consecutively.

Trigger Delay

Trg Delay

determines how many clock periods occur between the trigger event and the actual triggering. Refer to a triggering example near the end of this section.

In Trigger Stop Analysis mode, Trigger Delay can be set to capture a maximum of 16383 (1023) words before the selected trigger word by entering a value of 00000, or any 16384 (1024) segment after the trigger word by entering a value between 16384 (1024) and 65535.

Trigger Delay is set by incrementing or decrementing the current value using the **INCREMENT** or **DECREMENT** softkeys, or by entering an integer value in the range of 00000 to 65535 using the DATA keys.

Example - Triggering with the Trigger Arm Input

Figure 4-20 shows a set-up where the Trigger Arm input alone is used to trigger the analyzer. The signal at the ARM input BNC connector could be the generator strobe channel, or a data channel. Taking for example the "Trigger Start Analysis" operating mode, the strobe channel should be set to zero except for a one at the first address. The analyzer would then trigger on this pulse and would look at the data stream following the strobe pulse. All other trigger conditions must be set to don't care.

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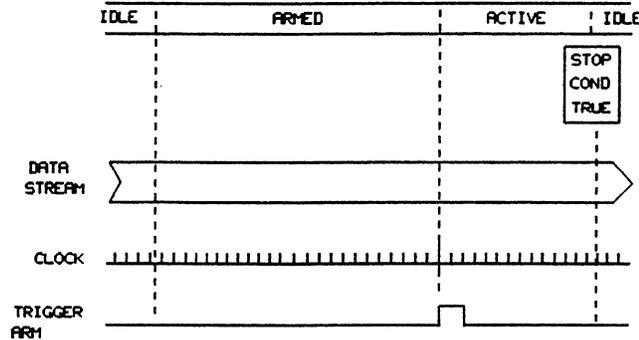


Figure 4-20. Triggering with the Trigger Arm Input

Example - Triggering with Trigger Word and Trigger Qualifier

Figure 4-21 shows a set-up where a Trigger Word is used to trigger the analyzer. In the "Trigger Start Analysis" operating mode, the analyzer goes into the active state when the received data matches the Trigger Word and at the same time the Trigger Qualifier Input receives a valid pulse. All other trigger conditions are set to "don't care".

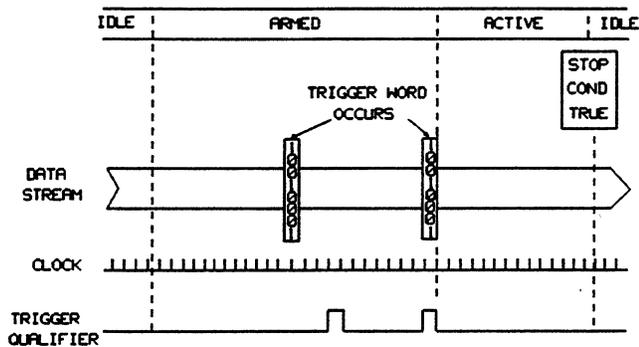


Figure 4-21. Triggering with a Trigger Word and Trigger Qualifier

Example - Triggering with Trigger Word, Trigger Count and Trigger Delay

Figure 4-22 shows a set-up where the selected Trigger Word must be encountered three times (trigger count=3) before the analyzer triggers. However, since trigger delay is set to 5 (clock pulses), the analyzer first goes active after this delay. Thus in the Trigger Start Analysis mode, the analyzer becomes active when all three conditions are met.

If the Allow Gaps setting had been ON, then the analyzer would trigger only if it encountered data words matching the Trigger Word *and occurring on three consecutive clock pulses*. All other trigger conditions are set to "don't care".

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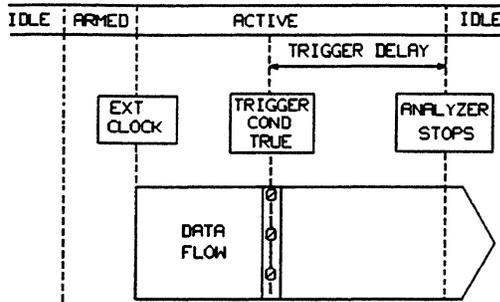


Figure 4-23. State Map for Delayed Trigger Stop Analysis

Stopping Analysis/Compare

The softkeys that can be called up via the **Stop** softkey deal with the various parameters affecting the end of the analyzer data capture cycle. If you have previously recalled the Standard Set, you will get the following softkey menu on pressing the **Stop** softkey:

Stop Slope	Stop Thres	Stop Imp	EXIT
Stop Delay			EXIT

The Stop softkey menu is dependent on the operating mode and after a Recall Standard Set the operating mode is Trigger Event Start Analysis. If Trigger Event Start Compare had previously been selected, the above softkey menu would appear as follows:

Stop Slope	Stop Thres	Stop Imp	EXIT
Stop Delay	Stop on Error		EXIT

Stop Slope

Stop Slope allows you to enable or disable the analyzer data capture stop and select the source of the stop. When using external stop, **Stop Slope** determines the active edge of the Stop signal applied to the rear panel STOP input BNC connector.

- POS SLOPE** selects the external stop signal leading edge as the data capture stop.
- NEG SLOPE** selects the external stop signal falling edge as the data capture stop.
- INTERNAL** selects an internal counter loaded on the Stop Delay menu, which counts the number of clock periods following the start of the analyzer data capture cycle.
- NOT ACTIVE** disables the analyzer data capture stop function. The analyzer will still stop when it has stored enough words to fill the entire memory. The effect is identical to setting the stop delay to 16383 (1023) and using internal stop.

Stop Threshold

Stop Thres permits setting the input threshold level for the external Stop signal. The softkey appears when the clock source is *external*.

- INCREMENT** increments the current input threshold level for external stop in 10 mV steps.
- DECREMENT** decrements the current input threshold level for external stop in 10 mV steps.

Control Page and Operating States

TTL (+1.40V) enters a TTL level directly.

ECL (-1.29V) enters an ECL level directly.

Alternatively, you can enter the numerical value in volts in the range of +10 V to -10 V. You must then press the **VOLT** key to terminate the entry.

Stop Impedance

Stop Imp sets the input impedance of the external STOP input. The available choices are **50.0** and **100k Ω** . After a Recall Standard Set the input impedance is set to 100 kOhms.

Stop Delay

Stop Delay allows you to set a delay on the analyzer internal stop, thus setting it to look at the required part of the received signal in absence of any external stop conditions. With internal Stop selected, the setting determines the number of clock periods between transition to the ACTIVE state and termination of data capture. Using external Stop, this setting determines the number of clock periods between the active edge of the stop signal and termination of data capture. This setting performs no function if Stop Slope is set to Not Active.

INCREMENT increments the stop delay.

DECREMENT decrements the stop delay.

Alternatively, you can enter a numerical value directly, using the DATA keys, in the range of 00000 to 16383 (1023). You must then press the softkey **ENTER:NUMBER** to terminate the entry.

Control Page and Operating States

Example - Stopping the Analysis with an External Stop Signal and Stop Delay

Figure 4-24 shows a set-up where the analysis/compare is stopped by an external stop signal applied to the STOP input BNC connector. Since stop delay has been set to 13, the analyzer carries on for another 13 clock pulses before it stops. The stop delay counter starts to decrement after the external stop signal has been received. Note that if no external stop signal is received, the analyzer will run on until it has stored 16384 (1024) words (full memory) and will be re-armed if autoarming has been enabled. If it has not, the analyzer will stop.

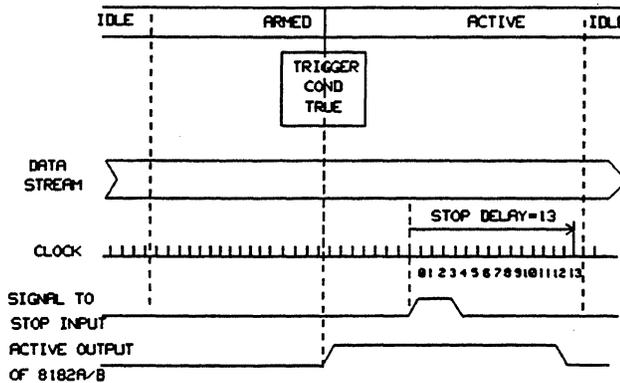


Figure 4-24. Stopping Analysis with External Stop Input and Stop Delay

Example - Stopping the Analysis with an Internal Stop Signal and Stop Delay

Figure 4-25 shows a set-up where the analysis/compare is stopped by the internal stop function. The stop delay counter starts to decrement after the analyzer has gone active (at the start of data capture/compare cycle). Since stop delay has been set to 13, the instrument analyzes/compares 13 data words before it stops.

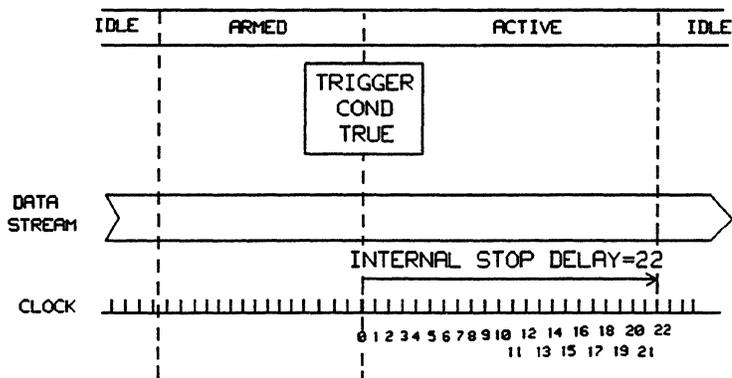


Figure 4-25. Stopping Analysis with Internal Stop Input and Stop Delay

Control Page and Operating States

Stop on Error

Stop on Error allows you to stop the analyzer compare cycle when an error is encountered. When enabled, comparison stops one clock period after an error occurs. This facility is available (and softkey appears) only when running in Real Time Compare Mode (Trigger Event Start Compare).

The softkeys **ON** and **OFF** enable and disable the Stop-on-error facility.

An example entitled Real Time Compare Mode later on in this chapter makes use of this facility.

Autoarming

The autoarming facility automatically re-arms the analyzer after it comes to the end of its data capture or compare cycle. This replaces repetitive RUN key operations. The **Autoarming** softkey gives access to the following autoarming options:

DELAY 0s	DELAY 1s	DELAY 3s	OFF
DELAY 0s *	DELAY 1s *	DELAY 3s *	EXIT ↑

DELAY 0s re-arms the analyzer on the clock cycle immediately following the end of its data capture or compare sequence (that is ACTIVE state). The analyzer does not enter the IDLE state.

DELAY 1s causes the analyzer to enter the IDLE state and re-arms it one second after the end of its data capture or compare cycle.

DELAY 3s causes the analyzer to enter the IDLE state and re-arms it three seconds after the end of its data capture or compare cycle.

DELAY 0s * re-arms the analyzer on the clock cycle immediately after the end of its data capture or compare cycle. Re-arming is disabled when an error is encountered.

DELAY 1s * causes the analyzer to enter the IDLE state and re-arms it one second after the end of its data capture or compare cycle. Rearming is disabled when an error is encountered.

DELAY 3s * causes the analyzer to enter the IDLE state and re-arms it three seconds after the end of its data capture or compare cycle. Rearming is disabled when an error is encountered.

OFF disables automatic re-arming.

If re-arming has been disabled for some reason, the analyzer remains in the IDLE state. To restart automatic re-arming you must press the softkey with the appropriate delay, followed by the RUN key. Refer below to Analyzer Operating States.

Control Page and Operating States

Analyzer Operating States

The 8182B has three operating states - IDLE, ARMED and ACTIVE. They can be initiated either by the front panel keys, external control inputs (when enabled), or remotely via the Hewlett-Packard Interface Bus (HP-IB). For a description of the instrument states when operating under program control via HP-IB refer to Chapter 8. The instrument states have to be looked at in the context of the selected operating mode, that is Trigger Event Start Analysis, Trigger Event Stop Analysis or Trigger Event Start Compare.

Trigger Event Start Analysis

After pressing the front panel RUN key, sampling is started by the trigger sequence and terminated by the stop sequence. A maximum of 16384 (1024) words can be stored in the analyzer memory. The diagram in Figure 4-26 illustrates the operation of the analyzer in Trigger Start Analysis.

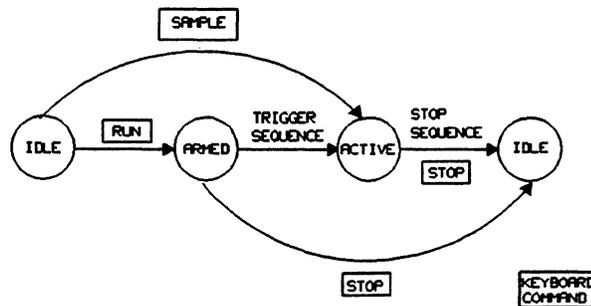


Figure 4-26. Analyzer Operating States in Trigger Start Analysis

The operating states are:

IDLE: The analyzer is waiting for the arming condition. The arming condition could be:

- RUN key pressed
- autoarming enabled
- arming signal at ARM input BNC connector (if input enabled)

ARMED: The analyzer is searching for trigger conditions. The trigger conditions could be:

- trigger arm signal at ARM input BNC connector itself (all other condition are "don't care")
- trigger word (words if trigger delay is not zero) valid
- trigger word and trigger qualifier valid

The start of the data capture sequence (data sampling) occurs only when the trigger delay counter has run to zero.

ACTIVE: Input data is sampled. The analyzer can enter the ACTIVE state from the ARMED state, or directly from the IDLE state by pressing the SAMPLE key on the front panel. In the absence of a clock signal, the analyzer generates one clock pulse every time the SAMPLE key is pressed.

When a stop condition is encountered (this includes also pressing the STOP key), the analyzer goes back to the IDLE state.

As a further aid to understanding data capture when Trigger Start Analysis is selected, a simplified timing diagram is shown in Figure 4-27. The diagram illustrates the cumulative effect of the various trigger and stop conditions in determining the data capture window. In Trigger Start Analysis, because data is stored in predetermined addresses (first word in address 00000, and so on) memory readout for

Control Page and Operating States

analysis and display can commence for lower addresses as data is still being written into the higher addresses. This interactive readout is especially useful at low clock frequencies, when stored data can be inspected for errors before the data capture cycle is completed.

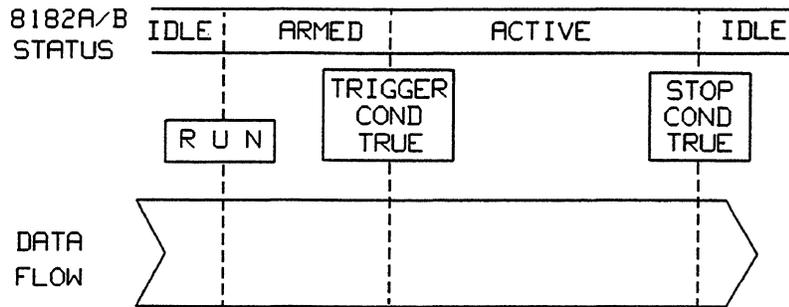


Figure 4-27. Timing Diagram for Trigger Start Analysis

Trigger Event Stop Analysis

After pressing the front panel RUN key, sampling starts on the first active clock pulse and is terminated by the trigger sequence. A maximum of 16384 words (address 00000 to 16383) can be stored in the analyzer memory. The diagram in Figure 4-28 illustrates the operation of the analyzer in Trigger Stop Analysis.

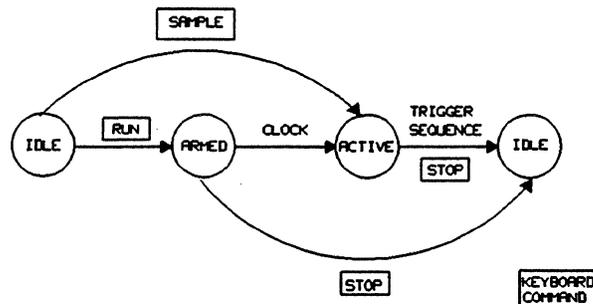


Figure 4-28. Analyzer Operating States in Trigger Stop Analysis

The operating states are:

IDLE: The analyzer is waiting for the arming condition. The arming condition can be:

- RUN key pressed
- autoarming enabled

ARMED: The analyzer is waiting for the first active clock edge.

ACTIVE: Input data is sampled. The analyzer can enter the ACTIVE state from the ARMED state, or directly from the IDLE state by pressing the SAMPLE key on the front panel. Subsequent presses of the SAMPLE key cause the analyzer to toggle between the IDLE and ACTIVE states.

When left in the IDLE state with an autoarming delay selected, the analyzer returns to the ARMED state after the delay is up.

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When a stop condition is encountered the analyzer goes back to the IDLE state. The stop conditions can be:

- trigger arm signal at ARM input BNC connector
- trigger word (words if trigger delay is not zero) valid
- trigger word and trigger qualifier valid

The end of the data capture sequence (data sampling) occurs only when the trigger delay counter has run to zero.

As a further aid to understanding data capture when Trigger Stop Analysis is selected, a simplified timing diagram is shown in Figure 4-29. The diagram illustrates the cumulative effect of the various stop conditions in determining the data capture window. The trigger delay can be set to capture a maximum of 16383 words before the selected trigger word by setting the trigger delay to 00000, or any 16384 segment after the trigger word by setting trigger delay to any value between 16384 and 65535.

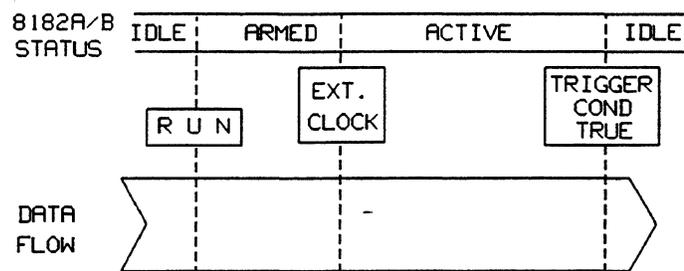


Figure 4-29. Timing Diagram for Trigger Stop Analysis

This mode cannot be used with the analyzer cycle mode AUTO, because the analyzer cannot see incoming data from the DUT (in our case directly from the generator) while it is writing to the display. Having completed the display (and waited if Autoarming Delay has been set), the analyzer starts sampling on the first clock pulse it receives. The analyzer cannot therefore remain in sync with the generator. Not only has the analyzer cycle mode to be set to SINGLE, but the generator must wait until the analyzer display is drawn. Since the analyzer waits for the trigger stop condition before it starts to display the results, sufficient time must be left between each single cycle to allow for this.

To obtain autocycling, use the analyzer TRIGGER output to gate the generator RUN,GATED input. This way the generator is restarted at the end of the analyzer compare and display cycle.

Trigger Event Start Compare

In synchronous Real Time Compare Mode the active slope of the external clock signal is used to generate a "time window" within each clock period for comparing incoming data with an expected data pattern. The positioning and width of this time window are set via the analyzer **Clock Delay** and **Clock Width** softkeys, located on the Control Page. Using the internal clock with the Real Time Compare Mode is possible, however it is not very beneficial, as the clock delay is always zero and the clock width is always 10 ns.

After pressing the front panel RUN key, comparison is started by the trigger sequence and terminated by the stop sequence. A maximum of 16384 words (address 00000 to 16383) can be stored in the analyzer memory. The diagram in Figure 4-30 illustrates the operation of the analyzer in Trigger Start Compare.

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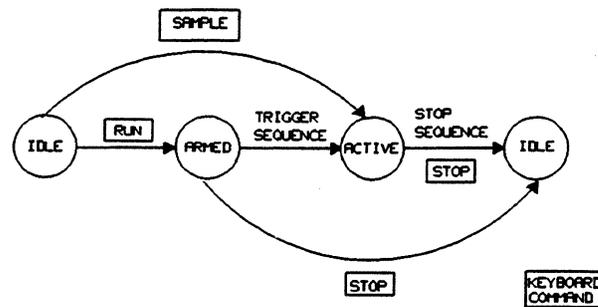


Figure 4-30. Analyzer Operating States in Trigger Start Compare

The operating states are:

- IDLE:** The analyzer is waiting for the arming condition. The arming condition could be:
- RUN key pressed
 - autoarming enabled
 - arming signal at ARM input BNC connector (if input enabled)
- ARMED:** The analyzer is searching for trigger conditions. The trigger conditions could be:
- trigger arm signal at ARM input BNC connector itself (all other condition are "don't care")
 - trigger word (words if trigger delay is not zero) valid
 - trigger word and trigger qualifier valid

The start of the data compare sequence occurs only when the trigger delay counter has run to zero.

- ACTIVE:** Input data is compared. The analyzer can enter the ACTIVE state from the ARMED state, or directly from the IDLE state by pressing the SAMPLE key on the front panel. In the absence of a clock signal, the analyzer generates one clock pulse every time the SAMPLE key is pressed.

When a stop condition is encountered the analyzer goes back to the IDLE state, unless autoarming has been enabled, in which case it goes directly to the ARMED state. The various parameters associated with the Real Time Compare Mode, such as trigger and stop conditions and a timing diagram will be discussed later in a separate section entitled "Real Time Compare Mode".

Exercise - Triggering with Trigger Arm, Stopping with Internal Delay

In this exercise the analyzer starts sampling 80 words as soon as the Arm Input becomes true.

Set the following:

Recall Standard Set

Operating Mode: Trigger Start Analysis

Glitch Detect: OFF

Clock Source: External Positive Slope (Thres + 1.40 V)

Clock Qualifier: Don't Care (Thres + 1.40 V Impedance 100 kOhm)

Clock Delay: 00.0 ns

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Trigger Arm:	Positive Slope	(Thres + 1.40 Impedance 100 kOhm)
Trigger Word:	XXXX XXXX XXXX XXXX	
Trig Qualifier:	Don't Care	(Thres + 1.40 V Impedance 100 kOhm)
Trigger Count:	01	
Allow Gaps:	NO	
Trigger Delay:	00000	
Stop:	Internal	(Thres + 1.40 V Impedance 100 kOhm)
Stop Delay:	79	
Autoarming:	1s	

Note that in order to obtain the above parameters, you only need to recall the Standard Set and then modify the settings for Trigger Arm, Stop Delay and Autoarming. The other parameters are set by recalling the Standard Set.

Exercise - Multiple Trigger Conditions

Consider Figure 4-31, showing the trigger and stop conditions. Assume the analyzer has been set to Trigger Start Analysis. A Trigger Word has been defined which must occur 3 times after the ARM input was true (each time concurrent with a Trigger Qualifier). A Trigger Delay of 5 clock cycles delays the onset of data capture. Finally, a Stop Delay of 7 has been designated.

This exercise can be set up by using a single extra data channel as trigger qualifier. The analyzer must be set to Allow Gaps = YES. Stop condition is internal and is generated by Stop Delay.

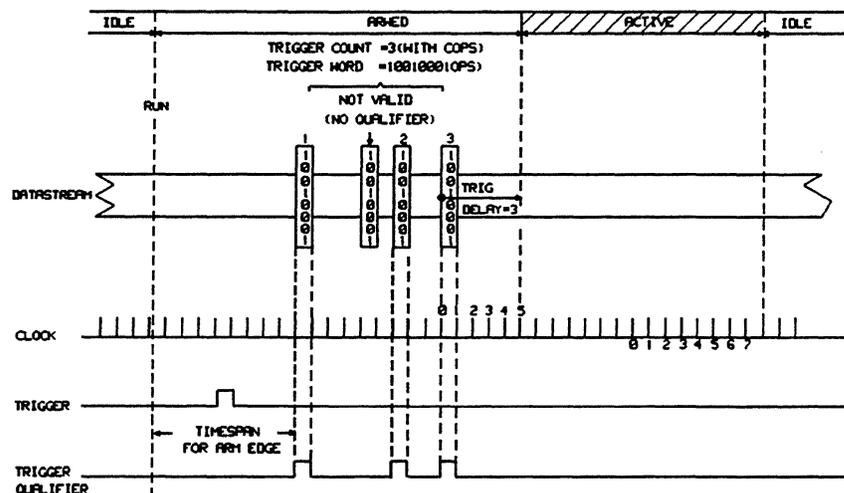


Figure 4-31. Exercise - Trigger and Stop Conditions

On pressing RUN the analyzer becomes armed. It now waits for the ARM input to become true (1), then waits for 3 trigger words to occur simultaneously with the trigger qualifier (2), (3) and (4). The analyzer proceeds to sample five clock cycles, after which it goes ACTIVE (5). The recognition of the STOP condition (i.e. STOP input is true), (6) causes the analyzer to take seven more samples (remember, Stop Delay = 7) and then go idle with the next clock cycle (7).

Control Page and Operating States

Error Messages

The analyzer monitors the entries you make and will return an error message if any of them are incorrect. Here is a list of error messages that can be received as a result of incorrect entries on the Control Page.

- VALUE OUT OF RANGE This flashing inverse video message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable to input threshold entries for clock, trigger and stop inputs, as well as to clock delay. If you exit the page where you made such an entry, it will be ignored and the previous valid entry will be retained.
- CLOCK IS TOO FAST This flashing message in line 2 of the display appears if the clock timing parameters are incompatible, e.g. clock delay or width setting with the external clock period.
- CLOCK WAS TOO FAST This flashing message in line 2 of the display appears if the clock timing parameters were at some time incompatible, e.g. clock delay or width setting with the external clock period. The message disappears when the analyzer enters the ARMED or ACTIVE state.

Apart from incorrect entries which are flagged as such by the analyzer, it is possible to make other erroneous entries which, although syntactically correct, will not make the analyzer do what you want it to. If you experience such a problem the Control Page setup is usually the cause. Therefore always check that the settings on this page are correct.

4-5 Input Page

The second page is the "Input Page". It provides access to functions such as single/dual threshold level selection, input threshold voltage level setting and input channel configuration.

Call up the Input Page now by pressing PAGES and **INPUT**.

Figure 4-32 shows the Input Page and the functions of the analyzer which are now accessible via softkeys on this page. The Input Page is somewhat similar to the Output Page of the generator. Let us now go through the functions in detail.

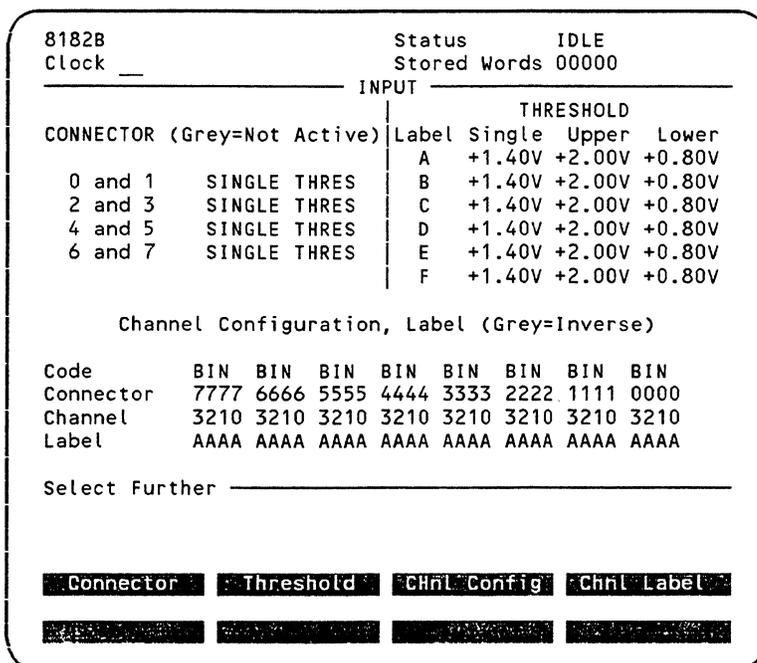


Figure 4-32. Analyzer Input Page

Single/Dual Threshold Selection

The analyzer can compare the incoming data against a single, variable threshold, or against variable upper and lower thresholds. The advantage of having dual threshold capability is that intermediate levels can be detected. The trade-off is that only half the input channels are available for this purpose. If you have a fully loaded analyzer, that is 32 channels (8 connectors), the Input Page main screen will appear as in Figure 4-32. If you switch to dual threshold mode for all channels, only the even-numbered connectors will remain on the screen. If you subsequently go back to single threshold mode, the odd-numbered connectors will not reappear, you have to call them back up, using the Channel Config facility. This will be covered later.

The softkey **Connector** provides access to the installed connectors:



0 and 1

accesses connectors 0 and 1. You can now select single or dual threshold by pressing the appropriate key - **SINGLE THRES** or **DUAL THRES**. On selecting dual threshold the odd numbered connector on the left hand side of the Report Area appears in a grey box, signifying that it is no longer available for use.

Input Page

2 and 3 as for the previous connector pair.

4 and 5 as for the previous connector pair.

6 and 7 as for the previous connector pair.

Note that if your analyzer does not have all of its channels installed, the uninstalled connectors, both odd and even appear in the Report Area in grey boxes, showing they are not available for use. The current threshold setting for these connectors is replaced with the message NOT INSTALLED. Only the installed connectors appear on the softkeys.

Input Threshold Voltage Level

The analyzer offers six labels A to F, for which different sets of input voltage level thresholds can be set. Later we will see how these labels are assigned to input channels. The analyzer offers a resolution of 10 mV and the thresholds can be set within the following ranges:

- Single threshold: -10.0 V to +10.0 V
- Upper threshold: -9.90 V to +10.0 V
- Lower threshold: -10.0 V to +9.90 V

The softkey **Threshold** allows you to set voltage levels for both the single and the dual upper and lower thresholds associated with each label. On pressing the softkey, the currently accessed label, threshold and voltage level appears in line 22 of the display, together with the following softkey menu:

```
INCREMENT  Next Label  Sing/Upp/Low  [ ]
DECREMENT  TTL (+1.40V)  ECL (-1.29V)  EXIT [ ]
```

INCREMENT increments the voltage level for the currently selected threshold and label. The voltage level is displayed in the inverse video field in line 22 of the display.

Next Label selects in turn the six labels A to F to which different threshold voltage levels can be assigned.

Sing/Upp/Low accesses in turn the three voltage thresholds for the selected label: Single, Upper and Lower.

DECREMENT decrements the voltage level for the currently selected threshold and label. The voltage level is displayed in the inverse video field in line 22 of the display.

TTL (+1.40V) allows the assignment of a TTL level directly to a label. The voltage level associated with this softkey depends on whether a single, upper or lower threshold has been selected by the **Sing/Upp/Low** softkey. The **Sing/Upp/Low** softkey therefore dictates which threshold will be assigned a TTL level.

ECL (-1.29V) allows the assignment of a ECL level directly to a label. The voltage level associated with this softkey depends on whether a single, upper or lower threshold has been selected by the **Sing/Upp/Low** softkey. The **Sing/Upp/Low** softkey therefore dictates which threshold will be assigned an ECL level.

Input Page

Channel Configuration - Input Page

The channel config facility on the analyzer is in part identical to that of the generator, and therefore only the differences will be discussed here. You should already be familiar with the channel configuration concept, as you will have read Chapter 3 of this manual, entitled "Generator Operation". If you need to update yourself, turn to the generator Output Page.

The lower part of the report area shows the current channel configuration. If you have just performed "Recall Standard Set", and assuming you have the full complement of 32 data channels installed, you will see 32 channels arranged in eight columns of four channels each. This configuration is shown in Figure 3-33.

8182B		Status		IDLE					
Clock		Stored Words		00000					
INPUT									
		THRESHOLD							
CONNECTOR (Grey=Not Active)	Label	Single	Upper	Lower					
	A	+1.40V	+2.00V	+0.80V					
0 and 1	SINGLE THRES	B	+1.40V	+2.00V	+0.80V				
2 and 3	SINGLE THRES	C	+1.40V	+2.00V	+0.80V				
4 and 5	SINGLE THRES	D	+1.40V	+2.00V	+0.80V				
6 and 7	SINGLE THRES	E	+1.40V	+2.00V	+0.80V				
		F	+1.40V	+2.00V	+0.80V				
Channel Configuration, Label (Grey=Inverse)									
Code	BIN	BIN	BIN	BIN	BIN	BIN	BIN	BIN	BIN
Connector	7777	6666	5555	4444	3333	2222	1111	0000	
Channel	3210	3210	3210	3210	3210	3210	3210	3210	
Label	AAAA	AAAA	AAAA	AAAA	AAAA	AAAA	AAAA	AAAA	
ENTER NEW VALUE									
Code	BIN	BIN	BIN	BIN	BIN	BIN	BIN	BIN	BIN
Connector	7777	6666	5555	4444	3333	2222	1111	0000	
Channel	3210	3210	3210	3210	3210	3210	3210	3210	
INSERT CHNL DELETE CHNL ← →									
INSRT SEGMENT Std Config Code/Polarity EXIT									

Figure 4-33. Analyzer Input Page Channel Config Menu

The analyzer data cables are a little different from those of the generator and have active probes on their ends. There are, however, still four cables per data connector and the cables are labeled the same way - 0 to 3. Channel numbering on the screen corresponds to the physical positions on the rear panel of the analyzer, the same way as on the generator.

The analyzer channels can be built into segments of up to 16 channels wide, and the channels mixed as required, or redefined via the DATA keys in the same way as with the generator. The connectors are labeled from 0 upwards and after a Recall Standard Set are displayed on the screen from right to left. The channels within each connector are labeled 0 to 3 and after a Recall Standard Set are also displayed from right to left.

As was the case with the generator, it is important to note when arranging the physical channels at the rear panel of the analyzer into input busses, that these must correspond to the bus arrangement on the screen.

Input Page

On pressing the **Chnl. Config** key the following softkey menu appears.

INSERT CHNL **DELETE CHNL** **←** **→**
INSERT SEGMENT **Std. Config** **Code/Polarity** **EXIT** ↑

The functions called up by the softkeys **INSERT CHNL**, **DELETE CHNL**, **←**, **→**, **INSERT SEGMENT** and **Std. Config** are identical to those of the generator. Their descriptions are therefore not repeated here.

Data Encoding

The arrangement for data encoding differs slightly from that of the generator. The relevant softkey is labeled **Code/Polarity**, rather than **Code/Entry** as on the generator, and the softkeys called up are also somewhat different.

NORMAL	displays the received data according to the positive logic convention.
INVERSE	displays the received data according to the negative logic convention, i.e. the data is displayed inverted.
←	moves the cursor to the left.
→	moves the cursor to the right.
BINARY	codes the data contained in the currently accessed segment in binary format on the Expected Data and State List Pages. The Code field in inverse video above the accessed segment echoes the selection by displaying BIN .
OCTAL	codes the data contained in the currently accessed segment in octal format on the Expected Data and State List Pages. The Code field in inverse video above the accessed segment echoes the selection by displaying OCT .
HEXADECIMAL	codes the data contained in the currently accessed segment in hexadecimal format on the Expected Data and State List Pages. The Code field in inverse video above the accessed segment echoes the selection by displaying HEX .

Data Channel Labeling

The channel label feature enables you to assign one of the voltage level labels A to F to any of the data channels. You do this by pressing the **Chnl. Label** key and then moving the inverse video cursor to the desired channel on the screen and selecting A to F on the DATA key pad. The cursor then automatically moves on to the next channel on the right. The **Chnl. Label** key calls up the following softkeys.

HOLD CURSOR **←** **→**
← **EXIT** ↑

→ moves the cursor to the right one channel at a time.

Input Page



moves the cursor to the left one channel at a time. This softkey is blank if the cursor is located at the leftmost channel, or if you have just executed "Standard Config" or "Recall Standard Set".



moves the cursor all the way to the left to the starting position at the leftmost channel. This softkey is blank if the cursor is located at the leftmost channel, or if you have just executed "Standard Config" or "Recall Standard Set".



prevents the cursor moving when assigning labels to data channels. To cancel, exit the menu.

Error and Warning Messages

VALUE OUT OF RANGE This flashing inverse video message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable to the Level entry. If you exit the page where you made such an entry, it will be ignored and the previous entry will be retained.

Upp-Low forced to +0.10 V This flashing message appears in line 23 if you make a value entry such that the difference between the upper and lower thresholds would have been less than +0.10 V, regardless of which threshold is being modified.

4-6 Expected Data Page

The third page is the Expected Data Page. It gives you access to the analyzer low speed (reference) memory and the data editing capabilities for this memory. The analyzer contains a high speed and a low speed memory, see Figure 4-34.

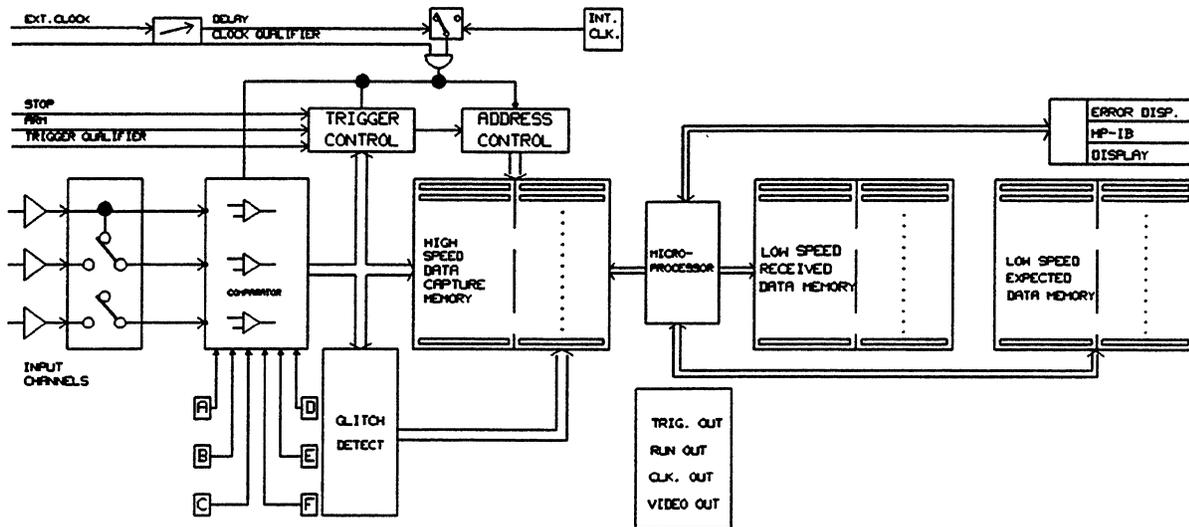


Figure 4-34. Analyzer Block Diagram

There are a number of ways of generating or bringing into analyzer's memory the data that will be used as reference for the incoming data. The simplest, and also the most tedious, is to type the data direct into the memory using the DATA keys. Other ways include using the data from a known device, which, having been received by the high speed memory, can be dumped into the low speed memory and later used as reference. In addition, data can be edited using the editing features on this page (inserted, deleted, copied or masked).

Data can also be brought in from an external device such as a computer system where it may be stored in the form of a disc file. The data transfer mechanism is the Fast Binary Transfer Mode, which is discussed in Chapter 8 of this manual. The CAE Link, which can convert and download large amounts of expected data in the form of device test vectors from a Computer Aided Engineering design station is yet another way of bringing data into the analyzer's memory. The CAE Link uses Fast Binary Transfer in the last stage of the conversion and transfer process. The link is covered in the CAE Link Manual.

Call up the Expected Data Page now by pressing PAGES and **EXPECTED DATA**.

Figure 4-35 shows the Expected Data Page and the functions of the analyzer which are now accessible via softkeys through this page. Let us now go through the functions in detail.

Expected Data Page

8182B		Status	STOP								
Clock	DATA	Address									
ADDR	MASK	DATA									
00000	.	0000 0000 0000 0000 0000 0000 0000 0000									
00001	.	0000 0000 0000 0000 0000 0000 0000 0000									
00002	.	0000 0000 0000 0000 0000 0000 0000 0000									
00003	.	0000 0000 0000 0000 0000 0000 0000 0000									
00004	.	0000 0000 0000 0000 0000 0000 0000 0000									
00005	.	0000 0000 0000 0000 0000 0000 0000 0000									
00006	.	0000 0000 0000 0000 0000 0000 0000 0000									
00007	.	0000 0000 0000 0000 0000 0000 0000 0000									
00008	.	0000 0000 0000 0000 0000 0000 0000 0000									
00009	.	0000 0000 0000 0000 0000 0000 0000 0000									
00010	.	0000 0000 0000 0000 0000 0000 0000 0000									
00011	.	0000 0000 0000 0000 0000 0000 0000 0000									
00012	.	0000 0000 0000 0000 0000 0000 0000 0000									
00013	.	0000 0000 0000 0000 0000 0000 0000 0000									
00014	.	0000 0000 0000 0000 0000 0000 0000 0000									
00015	.	0000 0000 0000 0000 0000 0000 0000 0000									
<table style="width: 100%; border: none;"> <tr> <td style="border: 1px solid black; padding: 2px;">CURSOR ↑</td> <td style="border: 1px solid black; padding: 2px;">PICTURE ↑↑</td> <td style="border: 1px solid black; padding: 2px;">← CURSOR</td> <td style="border: 1px solid black; padding: 2px;">CURSOR →</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">CURSOR ↓</td> <td style="border: 1px solid black; padding: 2px;">PICTURE ↓↓</td> <td style="border: 1px solid black; padding: 2px;">Top Address</td> <td style="border: 1px solid black; padding: 2px;">Edit</td> </tr> </table>				CURSOR ↑	PICTURE ↑↑	← CURSOR	CURSOR →	CURSOR ↓	PICTURE ↓↓	Top Address	Edit
CURSOR ↑	PICTURE ↑↑	← CURSOR	CURSOR →								
CURSOR ↓	PICTURE ↓↓	Top Address	Edit								

Figure 4-35. Expected Data Page

Notice that when the Expected Data Page is called up, channel data is displayed as defined by the channel configuration keys on the Input Page, that is in binary, octal, or hexadecimal format. These keys are also repeated on this page and their operation is identical. The data can now be entered and modified. Data entry is performed with the DATA keys at the current cursor location.

The DATA keys which are enabled for data entry depend on the data configuration currently in use. If you have just recalled Standard Set the data in all segments will be encoded in binary. Hence only the DATA keys 0 and 1 will be enabled. If you have selected octal format, DATA keys 0 to 7 will be enabled and for hexadecimal 0 to F will be enabled.

The reference data displayed on the Expected Data Page can also be masked. Any data bits or words which have been masked are not used for comparison with the incoming data from the test device and therefore do not generate any errors. Reference data can be masked individually, bit by bit, word by word, or completely by using the relevant functions accessed via the **Clear & Set** softkey.

To mask a single data bit/segment, use the cursor controls (described below) to bring the cursor to the required place and press the "X" DATA key. To cancel the mask, type in a value. To mask a whole word, bring the cursor to the relevant word mask marked by a "." (period) and press the "X" DATA key. To unmask the word press the "." DATA key.

Cursor and Screen Controls

There are several ways to move the cursor:

- CURSOR ↑
enable the cursor to be stepped vertically through the data stream.
- CURSOR ↓
Holding down the softkey causes repetitive cursor movement. When the cursor reaches the top (bottom) of the screen, further repetition causes the data and address display to scroll unless you have reached either end of memory.

Expected Data Page

PICTURE ↑↑	replaces the current sixteen lines displayed by the next numerically higher (lower) sixteen lines. Single or repetitive operation is available.
PICTURE ↓↓	
← CURSOR	enables horizontal movement of the cursor. When the cursor is at the limit of its travel, it jumps to the beginning of the next (end of the previous) line unless you have reached either end of memory.
CURSOR →	
Top Address	enables a new display of data to be called up quickly. It is activated either by entering a 5 digit number (including leading zeros) or via the INCREMENT or DECREMENT keys. If you enter a number of less than 4 digits, follow this by pressing the softkey ENTER NUMBER .

Data Editing

The softkey **Edit** opens the way to the data editing capabilities of the analyzer. On pressing it, the following softkey menu appears.

Dump Rec. Data **Clear & Set** **Channel Edit** **Line Edit**
CHECKSUM **Entry mode** **Chnl Config** **EXIT ↑**

Memory Loading

The memory load function is used in cases where the reference data comes from a known "golden" device. In order to perform subsequent tests on other devices, the known data has to be transferred from the low speed Received Data Memory to the low speed Expected Data (reference) Memory.

Dump Rec Data allows you to perform the data transfer from the Received Data Memory to the Expected Data Memory.

Memory Clear and Set

Clear & Set functions affect all locations of the reference memory. The data stored in this memory can be modified by setting all bits to a "1" or a "0", or by setting word or bit masks for the entire memory. This softkey calls a subsequent softkey menu offering the following functions.

Clr Word Mask clears all word masks. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**. After clearing, the word mask for each address (in MASK column) should contain a "." (period).

Set Word Mask sets all word masks. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**. After setting, the word mask for each address (in MASK column) should contain an "X".

Clr Bit Mask clears all bit/segment masks. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑**. After clearing, the data displayed will be the contents of the reference memory before the mask was applied.

Expected Data Page

- Set Bit Mask** sets all bit/segment masks. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you change your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑↑**. After setting, the bit/segment masks for the entire memory should contain "X's".
- Clr. Data** clears all reference data memory locations to zero. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑↑**.
- Set Data** sets all reference data channel memory locations to one. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you've changed your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑↑**.

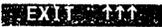
Channel Editing

- Channel Edit** enables you to carry out editing tasks on individual channels. Channel Edit operations function for all addresses.
- Clear Channel** clears all memory locations in the accessed channel to zero. Use the arrow keys **←** and **→** to move the cursor to the required channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you change your mind, leave the menu by pressing **EXIT ↑↑↑**. Note that if you have previously duplicated a channel in the same or a different segment, changing one of these channels will result in changes in all the others.
- Set Channel** sets all memory locations in the accessed channel to one. Use the arrow keys **←** and **→** to move the cursor to the required channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you change your mind, leave the menu by pressing **EXIT ↑↑↑**. Note that if you have previously duplicated a channel in the same or a different segment, changing one of these channels will result in changes in all the others.
- Clr Chnl Mask** clears channel masks in the selected channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you change your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑↑**. After clearing, the data displayed in that channel will be the contents of that part of the reference memory before the mask was applied.
- Set Chnl Mask** sets channel masks in the selected channel. You have to provide an acknowledgment by pressing the key **EXECUTE**. If you change your mind, leave the menu by pressing **REFUSE** or **EXIT ↑↑↑**. After setting, the selected channel should contain "X's" for the entire address range.
- Copy Channel** allows you to perform a one-to-one channel copy. You can copy the contents of memory of one channel to that of another channel. The information you need to perform the copy operation is given in lines 21 to 23 of the display. The source channel is contained within a grey field

Expected Data Page

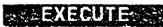
on the left hand side of the display. The destination channel is contained within an inverse video field on the right hand side of the display.

Two pairs of softkey arrows  and  move the cursors to the desired channels displayed in lines 22 and 23. The left hand arrows move the grey cursor (source channel/segment) and the right hand arrows move the inverse video cursor (destination channel/segment).

To carry out the actual copying operation press the key . If you change your mind, leave the menu by pressing .

allows you to exchange one channel with another. The information you need to perform the exchange operation is given in lines 21 to 23 of the display. The channels to exchange are contained within two inverse video fields in line 21 of the display.

Two pairs of softkey arrows  and  move the cursors to the desired channels displayed in lines 22 and 23. The left hand arrows move the cursor pertaining to the left hand field and the right hand arrows move the cursor pertaining to the right hand field.

To carry out the actual exchange operation press the key . If you change your mind, leave the menu by pressing . If you press  again, the channels move back to their original positions.

Line Editing

enables you to carry out editing tasks on individual lines. This is especially useful if you are working with many data channels in parallel. The tasks that can be performed are line inserting, deleting, and moving the memory contents with respect to the memory addresses.

allows you to insert a line of data (containing zeros) at the selected address. Suppose we wish to insert a line at address 00004. In order to see what is happening we will now set up some initial conditions. You should have no problems with the steps suggested below, as we have already covered them all in this chapter.

- Recall Standard Set
- Set all channels to 1

Enter 00004 into the inverse video field in line 22 of the display. Press  to perform the insertion. Then use the  key to bring the address 00000 to the top of the display. The word at address 00004 now contains all zeros. For each data line inserted, one data line at the end of the memory end (address 16383) is lost. Leave the menu by pressing .

allows you to delete a line of data from the selected address. Suppose we wish to delete a line at address 00004. In order to see what is happening we have to once again set up some initial conditions.

Expected Data Page

- Recall Standard Set
- Set all channels to 1
- Set the data at address 00004 to some random value

Enter 00004 into the inverse video field in line 22 of the display. Press **EXECUTE** to perform the deletion. Then use the **DECREMENT** key to bring the address 00000 to the top of the display. The word at address 00004 now contains all zeros, i.e. the random data at address 00004 has been deleted. For each data line deleted, one data line is added at the end of the memory end (address 16383/1023). The line contains all zeros. Leave the menu by pressing **EXIT**.

Roll Down Mem

allows you to move the contents of the memory with respect to the addresses. This feature is especially useful when for some reason the reference data, although correct, is not located at the right addresses. This can occur for example when tests using the real time compare mode are to be performed on some device/s and the reference data is obtained from a "golden" device. The reference data must be downloaded in Trigger Start Analysis mode, where trigger delay can be zero. However, in Trigger Start Compare mode (real time compare) minimum trigger delay is 00001. If identical triggering conditions have for some reason not been observed, the roll up memory / roll down memory feature can be used to bring the reference data into the correct address range.

After pressing **Roll Down Mem** a new set of softkeys appears together with an extra field highlighted in inverse video in line 22 which gives the number of memory locations by which the data will be rolled in the *downward* direction. This means physically downward on the screen, which translates to rolling the data at address 00000 to the entered address, that is the address contained in the highlighted field. The rest of the data follows suit. No data is lost as a result of a memory roll.

To enter the "roll address", use the DATA keys to type it into the highlighted field in line 22 and complete your entry by pressing the **ENTER NUMBER** softkey. Alternatively, use the **INCREMENT** and **DECREMENT** softkeys to reach the required address. The numbers in the square brackets also in line 22 give the allowed address range. Press the **EXECUTE** softkey to perform the roll.

Roll Up Mem

allows you to move the contents of the memory with respect to the addresses in the opposite direction.

After pressing **Roll Up Mem** a new set of softkeys appears together with an extra field highlighted in inverse video in line 22 which gives the number of memory locations by which the data will be rolled in the *upward* direction. This means physically upward on the screen, which translates to rolling the data at the entered address, that is the address contained in the highlighted field to address 00000. The rest of the data follows suit. No data is lost as a result of a memory roll.

To enter the "roll address", use the DATA keys to type it into the highlighted field in line 22 and complete your entry by pressing the **ENTER NUMBER** softkey. Alternatively, use the **INCREMENT** and **DECREMENT**

Expected Data Page

softkeys to reach the required address. The numbers in the square brackets also in line 22 give the allowed address range. Press the **EXECUTE** softkey to perform the roll.

Data Integrity - Checksum

CHECKSUM

provides you with the means of checking the integrity of the data stored in the analyzer's reference memory. When you press this softkey, a message Data Checksum NNNNNNNN is displayed in line 22 of the screen, where NNNNNNNN is a eight digit number (five digit on the A version). If you change the data in memory in any way, the checksum number will change.

Auto Cursor Movement - Expected Data Page

Entry Mode

selects the cursor movement when entering data from the DATA keys on the screen.

HOLD CURSOR

holds the cursor at the current data bit after data entry - no cursor movement.

HORIZONTAL

moves the cursor horizontally to the next data bit on the right. When the end of the line is reached the cursor wraps round to the beginning of the next line, i.e. the cursor.

VERTICAL

moves the cursor vertically downwards to the same data bit in the word, but at a higher address.

Channel Configuration - Data Page

Chnl Config

allows you to set the analyzer channel configuration. The softkey menus and functions behind this softkey are identical to those that can be accessed via the **Chnl Config** softkey on the Input Page. We have already covered these procedures in the subsection entitled Channel Configuration. The only difference is that on the Input Page the Report Area of the screen shows the channels, whereas here on the Expected Data Page it shows the data in the memory behind each channel.

Note that the channels displayed are those which we selected earlier during the channel configuration.

We have now covered the most complex page of the data analyzer.

Error Messages

The analyzer monitors the entries you make and will return an error message if any of them are incorrect. Here is a list of error messages that can be displayed as a result of incorrect entries on the Expected Data Page.

Expected Data Page

VALUE OUT OF RANGE This inverse video flashing message appears in line 20 if you make a value entry outside the range displayed in the square brackets in line 22 (just above the softkeys). This message is applicable wherever you can make a direct address entry, i.e. in the following cases: Top Address, Insert Line, Delete Line, Roll Down Memory and Roll Up Memory. After exiting the page where you made such an entry, the instrument will return to the previously set value.

4-7 Miscellaneous Page

The Miscellaneous Page is the fourth page and is basically an information page. It tells you what the analyzer HP-IB address settings are and gives you an overview of the installed channels. In addition, this page gives you access to the Autoexit facility, the display brightness adjustment, cursor and top address linking and to the store and recall facilities of the analyzer. The settings on this page, with the exception of the store and recall functions, in no way affect the operating parameters of the analyzer. The Miscellaneous Page is shown in Figure 4-36.

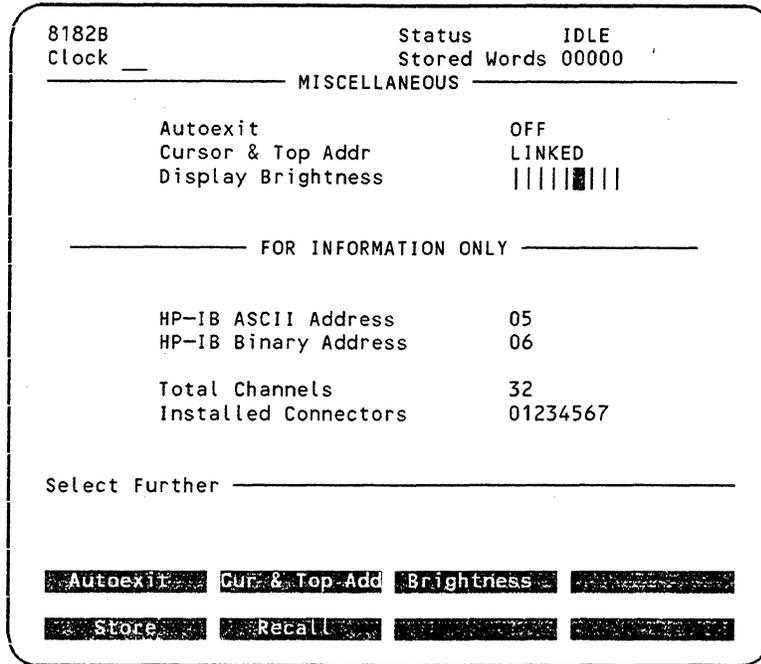


Figure 4-36. Miscellaneous Page

HP-IB ASCII Address

The analyzer has a Hewlett-Packard Interface Bus connector which enables it to be connected to a computer and operated under program control. The HP-IB ASCII address is used to set an address on this bus when the analyzer is operated from a computer. The address displayed is the address set on the address switches on the rear panel of the analyzer. For the information on setting the HP-IB ASCII address as well as for other details, refer to Chapter 7 of this manual, which deals with the analyzer programming procedures.

HP-IB Binary Address

The address displayed informs you of the setting of the binary address on the Hewlett-Packard Interface Bus. There are no switches on the analyzer to set this address. The binary address is always one higher than the ASCII address. For further details about the HP-IB binary address refer to Chapter 7 of this manual, which deals with the analyzer programming procedures.

Total (Installed) Channels

The number displayed tells you how many data channels are currently installed in your analyzer. The number can range from 8 to 32 in steps of 8. For further details refer to the Specifications Section in Chapter 1. Figure 4-36 shows 32 channels.

Installed Connectors

The numbers displayed tell you which connectors are installed. Each connector carries four channels. A fully loaded analyzer contains eight connectors.

Autoexit

With Autoexit set to ON an Exit automatically occurs following each new entry of a parameter value or operating mode (except via the **INCREMENT** and **DECREMENT** softkeys), returning the display to the previous softkey level. Throughout the softkey menu descriptions in this chapter Autoexit is OFF. If you wish to enable it press **Autoexit** followed by **ON**. The display returns automatically to the previous softkey level. Autoexit is always off after recalling the Standard Set.

Linking Cursor Position and Top Address

Via the **Cur. & Top. Add** softkey you can link the current position of the cursor on the Timing Diagrams and Error Map Pages to the top address of the displayed data on the State List and Expected Data Pages. You do this by pressing the softkey **LINKED**. This is also the default setting after recalling Standard Set. If you press **LOOSE**, the top address of the displayed data on the State List and Expected Data Pages is that which was active just before exiting one of those pages. The position of the cursor is nevertheless indicated on these pages by the letters "CUR" and a vertical line in column 8 of the display, joining it with the previous cursor setting. The length of the line is the difference between the two settings and is called "DELTA". This feature is covered on the Timing Diagram Page.

Screen Brightness Adjustment

Via the **Brightness** softkey you can alter the brightness of the analyzer display. The actual adjustment is done by pressing the **INCREASE** or the **DECREASE** softkey as appropriate. After a Recall Standard Set the brightness is set to about two thirds full setting.

Store/Recall Facility

The analyzer is equipped with batteries which allow the internal memory to retain the stored parameters and address pairs for approximately one week. If you use the analyzer after longer than that, it is possible that the batteries will be discharged and the stored parameters will be lost. This can also be the case if the analyzer has been repaired. If this happens, a flashing inverse video message PARAMETER DESTROYED - STANDARD SET RECALLED, displayed on the main page after you switch the analyzer on will warn you of this condition. As you use the analyzer, the batteries will recharge again and the instrument's memory storage facilities will be enabled. As soon as you use the store functions, the corresponding memory locations will be filled.

NOTE

Whenever you recall a parameter set, including the Standard Set, the analyzer will go into the IDLE state.

Recalling Standard Set

When you call up the Standard Set you cause the analyzer to load a set of default parameters. These are preset values for the various timing settings such as frequency, width or delay, or input signal settings such as input threshold etc. The Standard Set also recalls the standard channel configuration. This configuration depends on the number of data channels present in the data analyzer Table B-1 in Appendix B lists the full set of parameters that are loaded when Recall Standard Set is executed.

After pressing the **Recall** softkey you have to press the **Standard Set** softkey and confirm your entry by pressing **EXECUTE**. If you've changed your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Storing a Parameter

You can store up to three different parameter sets. After pressing the **Store** softkey you have to select the desired store location for the current parameter set by pressing the softkey **Set 1**, **Set 2** or **Set 3**. Confirm your selection by pressing **EXECUTE** on the next menu. If you change your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Recalling a Parameter

You can recall up to three different parameter sets. After pressing the **Recall** softkey you have to select the store location for the parameter set you wish to recall by pressing the softkey **Set 1**, **Set 2** or **Set 3**. Confirm your selection by pressing **EXECUTE** on the next menu. If you change your mind, you can leave the menu by pressing **REFUSE** or **EXIT**.

Exercise - Storing and Recalling a Parameter Set

- Recall Standard Set
- Change Stop Delay
- Insert data segments and channels
- Change input threshold voltage levels
- Store the current parameters
- Recall Standard Set
- Recall the previously stored parameter set
- Check on the Control, Input and Expected Data Pages that the parameter set has been recalled

State List Page

4-8 State List Page

The fifth page is the State List Page. The page shows the received data as it comes in from the tested device. In other words, it shows the contents of the high speed ECL memory. This is as opposed to the Expected Data Page, which shows the expected data residing in the low speed reference memory.

The State List Page is not available when the analyzer is operating in the Real Time Compare Mode (trigger start compare). This is because in this mode the incoming data from the tested device is not logged, but compared directly at the input comparators. A more detailed explanation is provided in the section entitled Real Time Compare Mode, later on in this chapter.

The State List Page does not show the whole of the high speed RAM range, only that part filled with received data. Therefore the received data is displayed only when the analyzer is ACTIVE, or if previously received data is still present in the memory.

The State List Page offers screen control keys for viewing the received data, channel configuration facility as on the Input Page and the display error and display glitches facility for displaying errors and glitches in the received data. In addition a Mask column is provided. This column serves only as a *reminder* that a word mask for a certain address or a block of addresses has been set on the Expected Data Page. The masks displayed in this column cannot be accessed from the State List Page, only from the Expected Data Page.

Call up the State List Page now by pressing PAGES and **STATE LIST...**

Figure 4-37 shows the State List Page and the functions of the analyzer which are now accessible via softkeys through this page. The display shows that all zero data has been received and that the reference data in the low speed memory also contains all zeros. Let us now go through the capabilities in detail.

ADDR	MASK	DATA	Display Errors	YES
00000	.	0000 0000 0000 0000 0000 0000 0000 0000		
00001	.	0000 0000 0000 0000 0000 0000 0000 0000		
00002	.	0000 0000 0000 0000 0000 0000 0000 0000		
00003	.	0000 0000 0000 0000 0000 0000 0000 0000		
00004	.	0000 0000 0000 0000 0000 0000 0000 0000		
00005	.	0000 0000 0000 0000 0000 0000 0000 0000		
00006	.	0000 0000 0000 0000 0000 0000 0000 0000		
00007	.	0000 0000 0000 0000 0000 0000 0000 0000		
00008	.	0000 0000 0000 0000 0000 0000 0000 0000		
00009	.	0000 0000 0000 0000 0000 0000 0000 0000		
00010	.	0000 0000 0000 0000 0000 0000 0000 0000		
00011	.	0000 0000 0000 0000 0000 0000 0000 0000		
00012	.	0000 0000 0000 0000 0000 0000 0000 0000		
00013	.	0000 0000 0000 0000 0000 0000 0000 0000		
00014	.	0000 0000 0000 0000 0000 0000 0000 0000		
00015	.	0000 0000 0000 0000 0000 0000 0000 0000		

8182B
Clock _____

Status IDLE
Stored Words 00032

STATE LIST

Display Errors YES

PICTURE ↑ PICTURE ↑↑ Disp Errors Disp Glitches
PICTURE ↓ PICTURE ↓↓ Top Address Chnl Config

Figure 4-37. State List Page

Screen Controls

There are several ways to move the screen:

- PICTURE ↑** enable the screen to be stepped upwards and downwards. Holding down the
- PICTURE ↓** softkey causes continuous screen movement. When the screen reaches the top (bottom) of the address range, the scrolling stops.
- PICTURE ↑↑** replace the current sixteen lines displayed by the next higher (lower) sixteen
- PICTURE ↓↓** lines. Single or repetitive operation is available.
- Top Address** enables a new display of data to be called up quickly. It is activated either by entering a 5 digit number (including leading zeros) or via the **INCREMENT** or **DECREMENT** keys. If you enter a number of less than 4 digits, follow this by pressing the softkey **ENTER NUMBER**.

Displaying Errors and Glitches

The State List Page, (as well as the Timing Diagrams and Error Map Pages) can display any detected errors or glitches. Data bits containing errors or glitches are displayed in an inverse video field or a grey field respectively. Data bits containing both errors and glitches are displayed in an inverse video field only. It is important, therefore, to make a separate test for errors only and then for glitches only. Glitch detection can be switched on and off on the Control Page. Glitch Display can be enabled on the State List Page, (as well as on the Timing Diagrams and Error Map Pages), but only if Glitch Detection has previously been enabled on the Control Page. Error Display can be switched on and off on the State List Page (and on the Error Map Page).

The display errors function enables you to see any detected errors on the screen. If you switch the function off, errors will still be detected, only they will not be displayed. The error capture facility works by comparing the received data arriving at the high speed memory with the data stored in the low speed Expected Data memory. An error means the bit pattern actually sampled is different from the bit pattern stored previously in the Expected Data reference memory. It is therefore important to make sure that correct data is indeed stored in the reference memory, otherwise any flagged errors on the State List Page (and Timing Diagrams and Error Map Pages) will be meaningless.

The **Disp Errors** softkey gives two choices in the next menu: **YES** and **NO**. If YES is selected, any errors will be displayed in inverse video.

The **Disp Glitches** softkey gives two choices in the next menu: **YES** and **NO**. If YES is selected, any glitches will be displayed in grey.

Exercise - Glitch Detection

For this exercise you need at least four data channels with RZ capability. For the first time we going to use the generator and the analyzer together. For this reason we need to set up some initial conditions on the generator. We shall take those described in the introduction section of this chapter. They are as follows:

- Recall Standard Set
- First Address: 00000
- Last Address: 00031
- Clock frequency: 1 MHz

State List Page

- Clock 1 Delay: 20 ns
- All output levels TTL (data, clock, strobe)
- Clear all data
- Up-counter on four channels of Connector 0
- Down-counter on four channels of Connector 1
- Strobe at address 00000 to 1

In addition perform the following steps:

- Enable outputs
- Start the generator by pressing the RUN key

Similarly, we have to set up initial conditions on the analyzer:

- Recall Standard Set
- Trigger Arm: Positive Slope
- Stop Delay: 00031
- Clock Delay: 05.0 ns
- Autoarming Delay: 0 s
- Display Errors: OFF

In addition perform the following steps:

- Start the analyzer by pressing the RUN key
- Dump Recorded Data to reference memory (on the Expected Data Page)

Figure 4-38 shows the resulting generator signals. Only channels 0-0 to 0-3 are shown. Remember that they contain a 4-bit up-counter.

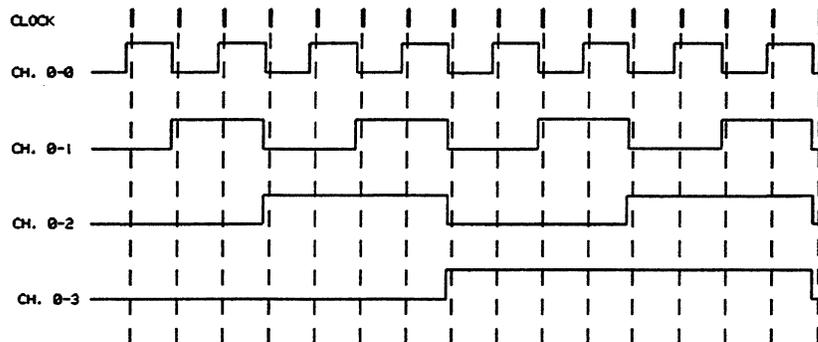


Figure 4-38. Single Transition Between Consecutive Sampling Points

A glitch is defined as two or more data signal transitions occurring between two consecutive sampling points. By changing the format on generator channels 0-0 to 0-3 to RZ=50%, we double the number of transitions between consecutive sampling points as is shown in Figure 4-39. These register as glitches on the analyzer.

The State List Page now shows the resulting glitches as grey fields around individual data bits. Notice that channel 0-0 shows no glitches. A careful study of Figure 4-39 and a glance at the total Clock Delay of 25 ns and data channel delay of 0 ns reveals that on this channel there is only *one* signal transition between consecutive analyzer sampling points. The signals on the other channels in

segment zero contain glitches, as is also shown in Figure 4-39.

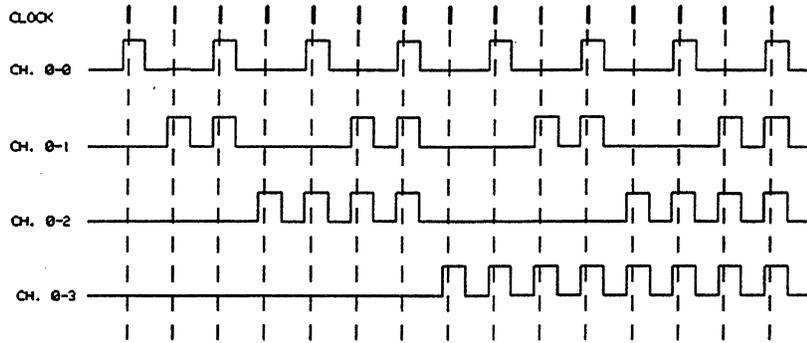


Figure 4-39. Dual Transitions Between Consecutive Sampling Points Registering as Glitches

If we were to force glitches on channel 0-0, we would have to change channel 0-0 data to all one's. This would result in two signal transitions between consecutive analyzer sampling points, as is shown in Figure 4-40. The resulting pattern contained in this segment is of course no longer an up-counter.

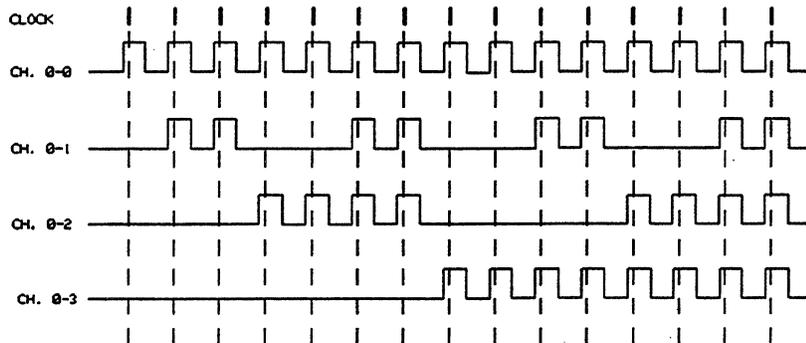


Figure 4-40. Forcing Glitches on the Least Significant Channel of a Segment Containing an Up-counter

Channel Configuration - State List Page

Chnl Config

allows you to set the analyzer channel configuration. The softkey menus and functions behind this softkey are identical to those that can be accessed via the **Chnl Config** softkey on the Input Page. We have already covered these procedures in the subsection entitled Channel Configuration. The only difference is that on the Input Page the Report Area of the screen shows the channels, whereas here on the State List Page it shows the received data in the memory behind each channel.

Note that the channels displayed are those which we selected earlier during the channel configuration.

State List Page

Use of SOFTKEYS and REPORTS Keys

The State List Page is the first of the three analysis display pages. Often a requirement arises to change some settings on other pages while viewing one of the display pages. It is therefore a good idea to look at a simple example illustrating this technique at this stage of our familiarization with the analyzer. The concept is completely flexible, i.e. you can view any page you want while changing the parameters on any of the other pages as long, of course, as the desired pages or softkeys are currently available. This is dependent on certain parameter selections such as Operating Mode.

The front panel key labeled SOFTKEYS enables you to access softkeys on other pages while observing the Report Area of the currently selected page. The front panel key labeled REPORTS enables you to access a Report Area on another page while changing parameters via softkeys on the currently selected page.

We can make use of the last exercise we have just done. It is possible that the grey fields on the State List Page signifying glitches are a little too dark to see properly. We can increase the brightness of the display while actually observing the State List Page data by performing the following:

- SOFTKEYS
- MISCELLANEOUS
- Brightness
- INCREASE
- SOFTKEYS
- STATE LIST

4-9 Timing Diagrams Page

The sixth page is the Timing Diagrams Page. It gives the same information as the State List Page, but in the form of a wave diagram similar to a display provided by an ordinary logic analyzer. Only the data actually captured by the high speed RAM can be displayed. The screen cannot possibly display all of the installed (maximum) channels, nor the full range of the capture memory. Instead, it works as a window which can be moved vertically and horizontally to display some of the channels and some of the memory respectively. This is achieved by means of picture control and window control keys.

The Timing Diagrams Page also offers a cursor for pinpointing individual data addresses, and facilities for making delta-time measurements, displaying errors, displaying glitches and for channel configuration.

Similarly to the State List Page, the Timing Diagrams Page is available during the Standard Analysis modes selected on the Control Page (Trigger Start Analysis and Trigger Stop Analysis), not during the Real Time Compare mode (Trigger Start Compare).

Call up the State List Page now by pressing PAGES and **TIMING DIAGR**. The Timing Diagrams Page is shown in Figure 4-41.

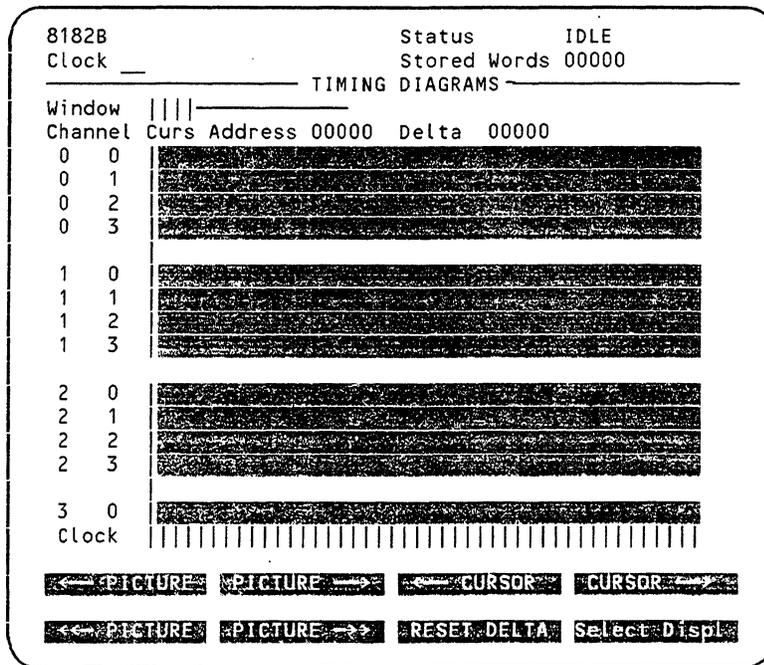


Figure 4-41. Timing Diagrams Page

When the analyzer is running, the capture memory gets filled by the incoming data at every analysis cycle. Regardless of the triggering conditions, the memory always starts filling at address +/-00000 and goes on filling until the stop conditions are fulfilled, or until all of its locations are filled. In Trigger Start Analysis mode the memory is filled in the positive direction to +16383, in Trigger Stop Analysis mode the memory is filled in the negative direction to -16383.

Picture Controls

The Picture Control keys allow you to select a part of the Received Data memory and display the contents on the screen. A window indicator in the top left hand corner of the Report Area shows you which part of the capture memory is being displayed. The direction of the Picture Control keys corresponds to the movement of the waveforms displayed on the screen, not to that of the window indicator. So, for example, in the Trigger Start Analysis mode the initial display starts at address +00000 and the window is at the extreme left of the indicator. If you move the waveforms to the left by pressing for instance the **←← PICTURE** softkey, the window indicator moves to the right, showing that you have moved further up the memory range. If on each analysis cycle you are filling only a part of the capture memory, you will eventually lose the display when you move the display window into an empty part of the memory. The Picture Control keys are explained below:

← PICTURE moves the display to the left one address at a time. Holding down the softkey causes continuous display movement. The window indicator moves to the right.

←← PICTURE moves the display to the left a block of addresses at a time. The size of the block is dependent on the current horizontal zoom factor (see later). Holding down the softkey causes continuous display movement. The window indicator moves to the right.

PICTURE → moves the display to the right one address at a time. Holding down the softkey causes continuous display movement. The window indicator moves to the left.

PICTURE →→ moves the display to the right a block of addresses at a time. The size of the block is dependent on the current horizontal zoom factor (see later). Holding down the softkey causes continuous display movement. The window indicator moves to the left.

Note that when Glitch Detection is enabled the capture memory is halved in size. This is regardless of whether Glitch Display is switched on or off.

Cursor Controls and Delta-time Measurement

A cursor is provided to aid in identifying or pinpointing particular data words or to make delta-time measurements. If you wish to pinpoint any part of the captured data you make use of both the Picture Control and Cursor Control keys, first to locate the correct memory window and then to identify the required address. You can also make a direct cursor address selection as we shall see in a moment.

As you move the cursor, the value contained in parameter Delta changes. You can reset Delta to zero at any position of the cursor. This becomes the new zero Delta position. Delta is defined as the difference between the current position of the cursor and its position the last time Delta was reset to zero. A horizontal line drawn by the moving cursor in the Clock row above the softkey labels gives a graphical representation of Delta. The units of Delta are addresses. Thus if you've moved the cursor by 10 words from say address 4305 to 4295 immediately after resetting it to zero, Delta will read -00010. Delta enables you to see at a glance any differences between cursor movements and is a useful general tool when working with address ranges.

← CURSOR moves the cursor to the right one step at a time. The step size is dependent on the horizontal zoom factor (see later), but is never greater than one address. Holding down the softkey causes continuous cursor movement. On reaching the right hand end of the window, the cursor stops and the softkey disappears.

Timing Diagrams Page

CURSOR ←

moves the cursor to the left one step at a time. The step size is dependent on the horizontal zoom factor (see later), but is never greater than one address. Holding down the softkey causes continuous cursor movement. On reaching the left hand end of the window, the cursor stops and the softkey disappears.

RESET DELTA

resets the value in Delta to 00000.

Cursor Address

By means of the **Curs Address** softkey you can select the cursor address you desire. To access the softkey you first have to get to its level by pressing **Select Displ**. The following softkey menu appears:

Curs Address **Disp Glitches** **Chnl Config**
Horiz Zoom **Vertical Zoom** **Vert Window** **EXIT**

Press **Curs Address**. You can now either enter the new cursor address directly into the inverse video field in line 22 using the DATA keys, or use the **INCREMENT** and **DECREMENT** keys. Press **EXIT** to leave the menu.

Displaying Errors and Glitches

The Timing Diagram Page, (as well as the State List and Error Map Pages) can display any detected errors and/or glitches. The right-most column on the Timing Diagrams Page is reserved for a binary representation of levels at the address currently occupied by the cursor. If the capture memory contains no data, or the cursor is positioned in an empty part of the memory, this column is empty. Any bits at the cursor address containing errors are highlighted in this column by inverse video fields, provided the Display Errors function has been enabled either on the State List Page or on the Error Map Page.

Data bits containing glitches are also highlighted in the right-most column by a grey field. Data bits containing both errors and glitches are highlighted by an inverse video field only. It is important, therefore, to make a separate test for errors only and then for glitches only. Glitch detection can be switched on and off on the Control Page. Glitch Display can be enabled on the Timing Diagrams Page, (as well as on the State List and Error Map Pages), but only if Glitch Detection has previously been enabled on the Control Page. As an additional help, glitches are also displayed on the timing diagrams themselves by means of short vertical lines in positions where they are occurring.

The display errors function enables you to see any detected errors on the screen. It can be switched on or off on the State List or the Error Map Pages. If you switch the function off, errors will still be detected, only they will not be displayed. The error capture facility works by comparing the received data arriving at the high speed memory with the data stored in the low speed reference memory. An error means the bit pattern actually sampled is different from the bit pattern stored previously in the Expected Data reference memory. It is therefore important to make sure that correct data is indeed stored in the reference memory, otherwise any flagged errors on the Timing Diagrams Page (and State List and Error Map Pages) will be meaningless.

The **Disp Glitches** softkey gives two choices in the next menu: **YES** and **NO**. If YES is selected, any glitches at cursor position will be highlighted in grey and any glitches contained in display window will be highlighted by short vertical lines. The **Disp Glitches** softkey is available on the Timing Diagrams Page only if Glitch Detection has previously been enabled on the Control Page.

Horizontal Zoom

Horizontal zoom controls the size of the display window relative to the size of the capture memory. Four zoom factors are available: x1, x2, x4 and x8. After a Recall Standard Set the display defaults to the x1 zoom factor, showing the biggest possible part of the capture memory, i.e. the biggest display window. This however makes the display too crowded for most purposes. By selecting a higher zoom factor the timing diagrams on the screen can be expanded by the corresponding amount, making the display window relatively smaller by the same amount.

To obtain access to the horizontal zoom menu, press **Select Displ.** on the Timing Diagrams Page main menu. The following softkey menu appears:

```

Curs Address  [ ]  Disp Glitches  Chnl Config
Horiz. Zoom   Vertical Zoom  Vert Window  EXIT [ ]
    
```

Horiz Zoom enables you to change the zoom factor of the horizontal display, i.e. of the amount of memory being displayed. Press one of the horizontal zoom keys **[]**, **[]**, **[]** or **[]** to select the desired zoom factor. Press **EXIT []** to leave the menu.

Vertical Zoom

Vertical zoom controls the size of the display window relative to the number of installed channels. Two zoom factors are available: x1 and x2. After a Recall Standard Set the display defaults to the x1 zoom factor, showing the biggest possible number of channels. This may however make the display too crowded for some purposes. By selecting the higher zoom factor the timing diagrams on the screen can be expanded by the corresponding amount, making the number of channels smaller by the same amount.

To obtain access to the vertical zoom menu, press **Select Displ.** on the Timing Diagrams Page main menu. The following softkey menu appears:

```

Curs Address  [ ]  Disp Glitches  Chnl Config
Horiz. Zoom   Vertical Zoom  Vert Window  EXIT [ ]
    
```

Vertical Zoom enables you to change the zoom factor of the vertical display, i.e. of the number of channels being displayed. Press one of the horizontal zoom keys **[]** or **[]** to select the desired zoom factor. Press **EXIT []** to leave the menu.

Vertical Window

The analyzer screen can display at most 13 channels at any one time. Selection of different sub-menus and/or the higher vertical zoom factor can limit this to 6. For this reason we need the vertical window facility. Vertical window controls the position of the display window relative to the called up channels.

As we know from the work done with some of the previously described pages, channels can be called up from the installed channels by means of the channel configuration facility. This is included on the Input, Expected Data, State List, Timing Diagrams and Error Map Pages. Vertical window control keys function rather like the cursor control keys, but in the vertical direction.

Timing Diagrams Page

To obtain access to the vertical window menu, press **Select Displ** on the Timing Diagrams Page main menu. The following softkey menu appears:

Curs:Address	Disp:Glitches	Chnl:Config
Horiz:Zoom	Vertical:Zoom	Vert:Window
		EXIT

Vert Window enables you to select the channels you wish to observe out of the called up channels. On pressing this key the current channel configuration appears in lines 22 and 23 of the display, together with an inverse video window, showing which channels are currently being displayed on the Timing Diagrams Page. Two arrow keys **←** and **→** allow you to move the window, thus selecting the desired channels for display. To leave the menu press **EXIT**.

Channel Configuration - Timing Diagrams Page

Chnl Config allows you to set the analyzer channel configuration. The softkey menus and functions behind this softkey are identical to those that can be accessed via the **Chnl:Config** softkey on the Input Page. We have already covered these procedures in the subsection entitled Channel Configuration.

Note that the channels displayed are those which we selected earlier during the channel configuration.

4-10 Error Map Page

The seventh page is the Error Map Page. In the Standard Analysis Mode this Page shows the received data as it comes in from the tested device. In other words, it shows the contents of the high speed ECL Data Capture memory (and the low speed Received Data memory). This is as opposed to the Expected Data Page, which shows the expected data residing in the low speed Expected Data reference memory. The data is displayed in a condensed form.

The Error Map Page is the only "analysis" display page available when the analyzer is operating in the Real Time Compare Mode (trigger start compare). In this mode the display is drawn at the end of a compare cycle. The incoming data from the tested device is not logged, but compared directly at the input comparators. A more detailed explanation is provided in Section 4-11, Real Time Compare Mode, later on in this chapter.

Unlike the State List and Timing Diagrams Pages, where errors are easy to identify only if they happen to occur on addresses which are actually displayed, the Error Map checks the entire sequence (up to 16384/1024 words) at once for errors. This is because the data is presented in a condensed form. The Error Map Page is the only page capable of giving an overview of any errors in the whole of the memory range of the analyzer. When only a part of the memory is filled with received data however, the Error Map Page shows only that part. The Error Map represents every word by a dot as long as it corresponds to its counterpart in the Expected Data reference memory. When one or more bits in a word are different, the word will be displayed as a square. This is a very powerful feature and we will use it frequently while making measurements.

The Error Map Page offers cursor control keys for viewing the received/error data, error and glitch display keys, and error search and count keys for error logging. In addition it offers the channel configuration facility as on the Input, Expected Data, State List and Timing Diagrams Pages.

Call up the Error Map Page now by pressing PAGES and **ERROR-MAP**.

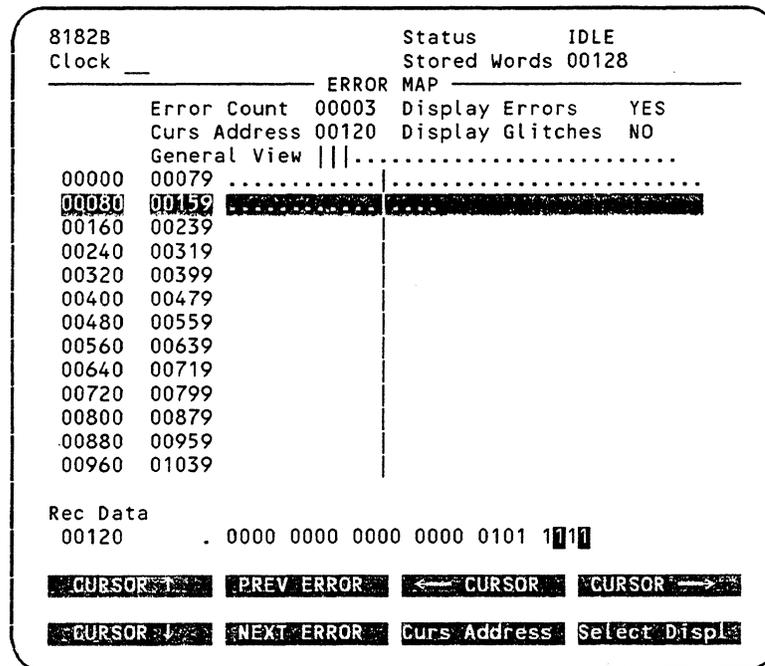


Figure 4-42. Error Map Page (B-version)

Error Map Page

The layout and some facilities of this page change depending on the selected operating mode. Figure 4-42 shows the Error Map Page for the Trigger Start Analysis mode, giving the functions of the analyzer which are accessible in this mode via softkeys through this page. We shall cover the other two operating modes a little later. The display shows that 128 words have been stored and three errors have been found. The cursor is at address 120. Let us now go through the capabilities in detail.

Screen Controls

The cursor consists of a wide grey line running in the horizontal direction and a thin line in the vertical direction. The grey line contains a block of 80 addresses. The cursor address is where the two lines meet. Note that if Cursor Address and Top Address are linked on the Miscellaneous Page, the cursor address on the Error Map Page corresponds the cursor address on the Timing Diagrams Page and to the Top Address on the State List Page.

The Error Map Page on the 8182A analyzer can display data for 1024 addresses at a time. Since its memory depth is 1024 words, the Error Map displays the whole of the memory at a time. Any errors are displayed in the form of small squares.

On the 8182B analyzer the Error Map Page can display data for 1040 addresses at a time. Since the 8182B analyzer has a memory depth of 16384 words, the page functions like a window that can be scrolled through memory with the cursor keys, always showing approximately 1K of data. The parameter General View in line 6 of the display shows the position of the display window on a row of dots representing the complete memory. Each dot in turn represents 256 words of received data. It is this row of dots that enables you to see at a glance if any errors have occurred anywhere within the full memory range of 16384 words. If an error or errors occur within a block of 256 words, the dot turns into a small square. You can then scroll the display to that area of memory and pinpoint the error (also appearing as a small square) with the cursor. Alternatively, you can use the error search facility to find the error. We shall discuss this in a little while.

There are several ways to move the cursor:

- | | |
|---------------------|---|
| CURSOR ↑ | step the wide grey line upwards and downwards. Holding down the softkey causes a continuous movement of the line. On reaching the top (or bottom) of the screen (not the address range), the display starts to scroll through memory. The window indicator moves along the dotted line giving the position of the window in the capture memory. On reaching either of the address range limits cursor movement stops. |
| CURSOR ↓ | |
| ← CURSOR | moves the thin vertical line left and right. Holding down the softkey causes a continuous movement of the line. On reaching an 80-word boundary, the cursor jumps to the next horizontal row, or scrolls the screen. On reaching either of the address range limits cursor movement stops. |
| CURSOR → | |
| Curs Address | enables a new display of data to be called up quickly. It is activated either by entering a 5 digit number (including leading zeros) or via the INCREMENT or DECREMENT keys. If you enter a number of less than 5 digits, follow this by pressing the softkey ENTER NUMBER . |

Error Map Page

Displaying Errors and Glitches

The Error Map Page, (as well as the State List and Timing Diagrams Pages) can display any detected errors or glitches. Both glitches and errors are represented by small squares on the Error Map Page. It is therefore important to make separate tests for glitches and for errors in order to distinguish the two. Assuming that either glitches or errors have been selected for display, you can use the **NEXT ERROR** and **PREV. ERROR** softkeys to quickly locate any glitches or errors that have been received.

Glitch detection can be switched on and off on the Control Page. Glitch Display can be enabled on the Error Map Page, (as well as on the State List and Timing Diagrams Pages) but only if Glitch Detection has previously been enabled on the Control Page (see Glitch Detection in Section 4-4, Control Page and Operating States). Error Display can be switched on and off on the Error Map Page (and on the State List Page).

The display errors function enables you to see any detected errors on the screen. If you switch the function off, errors will still be detected, only they will not be displayed. The error capture facility works by comparing the received data arriving at the low speed Received Data memory with the data stored in the low speed Expected Data reference memory. An error means the bit pattern actually sampled is different from the bit pattern stored previously in the reference memory. It is therefore important to make sure that correct data is indeed stored in the reference memory, otherwise any flagged errors on the State List Page (and Timing Diagrams and Error Map Pages) will be meaningless.

To obtain access to the additional error logging keys, press **Select Displ.** on the Error Map Page main menu. The following softkey menu appears:

```

Error Count  Displ Errors  Disp Glitches  Chnl Config
EXIT

```

Disp Errors gives two choices in the next menu: **YES** and **NO**. If YES is selected, any errors will be displayed as small squares on the Error Map.

Disp Glitches gives two choices in the next menu: **YES** and **NO**. If YES is selected, any glitches will be displayed as small squares on the Error Map.

Error Count gives two choices in the next menu: **ON** and **OFF**. When switched on, the error counter logs all errors or glitches or both, provided they have been enabled for logging by the **Displ Errors** or **Disp Glitches** softkeys.

Channel Configuration - Error Map Page

Chnl Config allows you to set the analyzer channel configuration. The softkey menus and functions behind this softkey are identical to those that can be accessed via the **Chnl Config** softkey on the Input Page. We have already covered these procedures in the subsection entitled Channel Configuration.

Note that the channels displayed are those which we selected earlier during the channel configuration.

4-11 Real Time Compare Mode

Concepts of Real Time Compare

In this section we are going to discuss all aspects of data comparison in real time as offered by the Trigger Start Compare Mode of the 8182A/B Data Analyzer. The block diagram of the analyzer in Figure 4-43 will help you understand the operation of the instrument in this mode. The real time compare mode permits complex functional testing at speed in which timing and level parameters of a tested device are checked simultaneously.

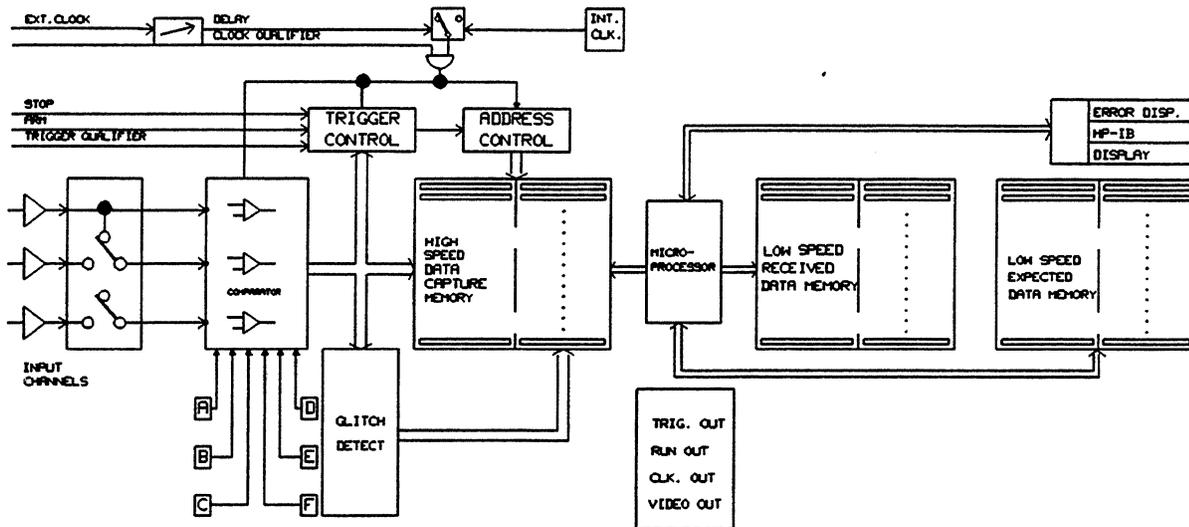


Figure 4-43. Analyzer Block Diagram

We already know that the two analysis modes work by storing the incoming data during each cycle in the fast (ECL) Data Capture memory and at the end of the data capture cycle downloading it into the low speed (CMOS) Received Data memory. At the end of each cycle a software compare with the reference data stored in the low speed (CMOS) Expected Data memory is performed via the microprocessor.

From the Received Data memory the data is passed to the screen and displayed on the State List, Timing Diagram or Error Map Pages. The data remains there until the start of the next cycle. This method has the disadvantage of missing a large amount of data in the time that the microprocessor performs the data comparison and updates the display, as can be seen in Figure 4-44. The percentage amount of lost data is of course proportional to the generator clocking frequency and the size of the capture cycle.

The Trigger Start Compare Mode performs comparison in real time using hardware comparators. Software compare via the microprocessor is not possible due to speed limitations. Glitch detection, which too is a software operation is therefore not available. The incoming data is not stored because the Data Capture memory is now used as a reference memory to hold the reference data for the hardware compare. The fast memory is needed for this task in order that "at speed" comparison can be achieved. For this reason are the State List and Timing Diagrams Pages not available in the Real Time Compare Mode.

Real Time Compare Mode

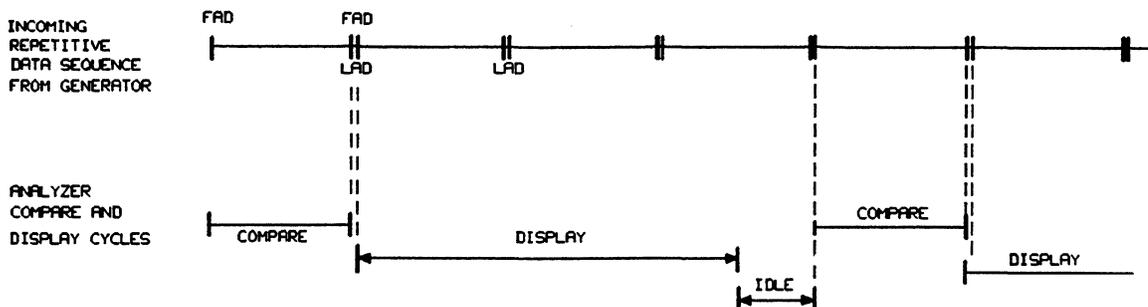


Figure 4-44. Synchronized Analyzer Operation in Standard Analysis Mode

The hardware comparators require a reference memory with a short access time. The CMOS memory which normally holds the reference data does not satisfy this requirement. Therefore, the reference data is transferred into the fast ECL memory, and from there, applied to the comparators. As soon as a comparison fails, channel and address flags are set, displaying the errors on the Error Map.

In addition, signals indicating errors in real time are available at two rear panel BNC outputs. The output labeled PULSED delivers a pulse every time a comparison fails. The output labeled LATCHED is set with the first compare failure and cleared when a new compare cycle starts. These outputs can be used, for example, to stop the analyzer, or to trigger an oscilloscope on an error pulse.

In the synchronous Real Time Compare Mode the active slope of the external clock signal is used to generate a "time window" within each clock period, in which incoming data is compared with an expected data pattern. Incoming data is tested for stability during each discrete time interval so created. The position and width of this time window (see the timing diagram in Figure 4-45) are set via the **Clock Delay** and **Clock Width** softkeys respectively. Both softkeys are located on the analyzer Control Page menu.

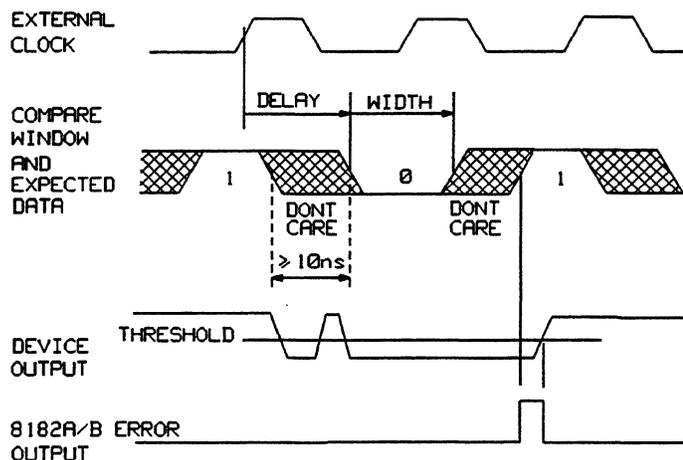


Figure 4-45. Time Windows in Real Time Compare Mode

Comparison is started by the trigger sequence and terminated by the selected stop conditions (e.g. Stop on Error, external stop signal, pressing the STOP key and so on). Analyzer operating states listed below and the state diagram in Figure 4-46 illustrates analyzer operation in this mode.

- IDLE: Waiting for the arm condition (RUN command)
- ARMED: Searching for the trigger conditions
- ACTIVE: Comparing incoming data with expected data

Real Time Compare Mode

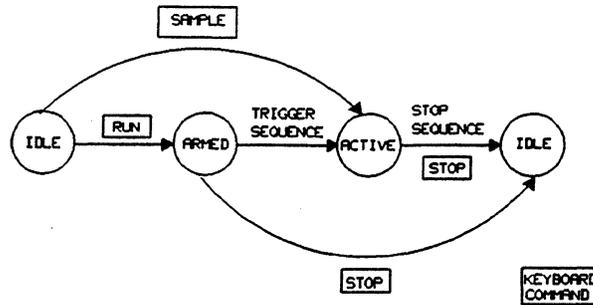


Figure 4-46. State Diagram for the Real Time Compare Mode

In the ARMED state, the analyzer searches for the selected trigger word by momentarily sampling the incoming data as in the Trigger Start Analysis mode. The sampling point is determined by the active edge of the external clock and analyzer Clock Delay setting. For valid trigger word recognition, therefore, the trigger word must be true when sampling occurs. The Clock Width setting has no effect on data sampling in the ARMED state. In the ACTIVE state, the analyzer compares incoming data with the expected data for the duration of the "compare window", as determined by the Clock Width setting, see Figure 4-45. At the end of each compare window, the next word of expected data is made available for comparison. To accomplish this, the analyzer requires a gap between successive "compare windows" of at least 10 ns, as can be seen in Figure 4-45.

On pressing the RUN key in the Trigger Start Compare Mode, the contents of the low speed Expected Data memory are transferred to the high speed Data Capture (ECL) memory prior to the real time comparison. During the active compare operation, the current input word is compared directly (i.e. without any microprocessor involvement) with the reference word stored at the appropriate address in the high speed memory. It is therefore essential to have a data sequence stored in the high speed memory, which is identical to the sequence arriving at the inputs of the analyzer.

To see more clearly why the two sequences must be of identical length, consider the cycling diagram in Figure 4-47. If the cycling period of the analyzer was set to $(N+1)$ words, where the sequence length of incoming data is N words, we would begin to see errors as soon as the second sequence is compared. At this point, the first word of the incoming second sequence would be compared with the last word from the reference data memory (which generally won't match), and a steady string of errors would result.

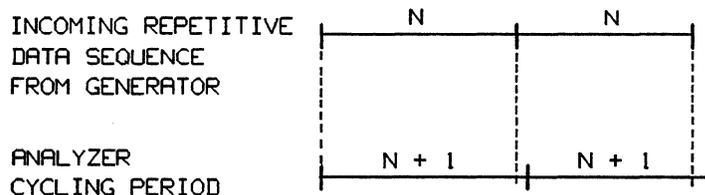


Figure 4-47. Effect of Unequal Lengths of Incoming and Stored Data Sequences

Rear Panel Error Outputs

The analyzer has two BNC error output sockets labeled PULSED and LATCHED, which can be used by external devices such as scopes, counters and so on. The PULSED Output delivers a high-going pulse whenever an error within the current compare "time window" occurs. The LATCHED Output goes high with the first error and remains high until the analyzer is re-armed.

Real Time Compare Mode

The message "Compare PASSED" or "Compare FAILED" at the top of the report area of the Error Map Page indicates the signal status of the rear panel LATCHED output.

Note that the LATCHED and PULSED Outputs also function in Logic Analyzer mode to indicate comparison errors.

At the end of a compare cycle, any change to the word mask settings on the Expected Data page will not affect error indications of the outputs until the next compare cycle begins. (This applies also to the display of the Error Map Page.)

Memory Loading

Before selecting Real Time Compare Mode, the expected data pattern must be loaded into the Expected Data low speed memory. This can be done by:

1. Entering and editing the data manually via the front panel DATA keys.
2. Downloading the data from a computer via HP-IB (see Chapter 8, Analyzer Programming).
3. Executing a memory dump of data recorded in Trigger Start Analysis (Standard Analysis Mode).

Before executing a memory dump, it is recommended that data is recorded under triggering conditions identical to those required for the Real Time Compare mode. Therefore remember to set the Trigger Delay value to not less than 1 when recording data in preparation for real time comparison, because in Real Time Compare mode the comparison starts a minimum 1 clock period after the Trigger Word.

If the Trigger conditions have not been observed, the Roll Up Memory/Roll Down Memory feature of the Expected Data Page enables cyclic rolling of the Expected Data Memory contents. This has already been covered on the Expected Data Page.

The following provides a general memory dump procedure prior to real time comparison.

1. With synchronous Trigger Start Analysis selected, define the data capture cycle using the **Trigger** and **Stop** softkeys on the Control Page. Ensure the Trigger Delay setting is greater than or equal to 1.
2. Press the front panel RUN key to record data.
3. Press the front panel PAGES key and select the Expected Data Page.
4. Dump received data from the low speed Received Data Memory into the low speed Expected Data Memory by using the following keystroke sequence:

```
EDIT
Dump Rec Data
EXECUTE
```

Look at the Data Page of the generator and visually compare its display with that of the Expected Data Page of the analyzer, i.e. Second Word of the generator = First Word of the analyzer, Third Word of the generator = Second Word of the analyzer, and so on. The First Word of the generator is not recorded by the analyzer because Trigger Delay has been set to 1.

We can now return to the Control Page and select Real Time Compare Mode. The content of the Expected Data Memory is automatically transferred back to the high speed memory the first time the RUN key is pressed, or if the analyzer is already running, at the beginning of each new data compare cycle.

Real Time Compare Mode

Autocycling

For data streams comprising long repetitive data sequences, you can use the autocycling feature of Real Time Compare mode to provide continuous monitoring of the data stream until an error occurs. When you call up autocycling, all data applied to the analyzer inputs is compared. During error-free comparison no display is made and therefore no incoming data is missed. Select autocycling via the **Cycling Per** softkey on the Control Page menu (when in Trigger Start Compare operating mode). When set to **ON**, the entered value must correspond exactly to the repeated sequence length.

For Cycling Period = N, therefore, the analyzer compares each consecutive sequence of N words with the first N words of expected data, starting with memory address 00000. This is illustrated in the cycling diagram in Figure 4-48. Note that if expected data has been loaded using the Dump Recorded Data feature described under Memory Loading, the content of memory address 00000 is determined by the Trigger Delay setting; e.g. if Trigger Delay = 00006, memory address 00000 contains the sixth word following the Trigger Word.

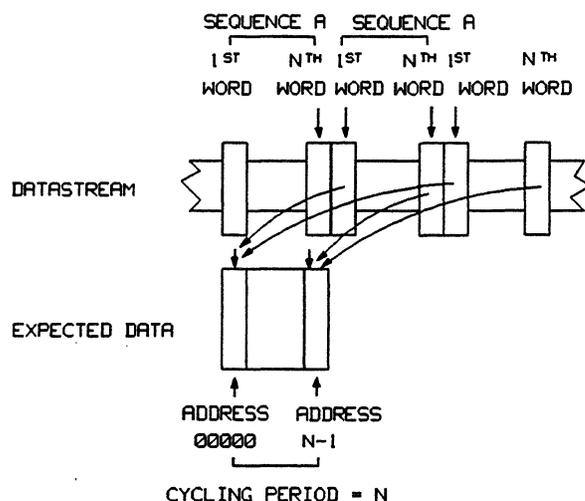


Figure 4-48. Analyzer Autocycling Diagram

During autocycle operation, the user can select either of the following error-related stop conditions:

1. Set Stop on Error to **ON** via the **Stop on Error** softkey on the Control Page. Real time comparison then stops one clock period after an error occurs. The Error Map will display the compare result for all words up to and including the word immediately after the error word. There is no display during error-free cycling.
2. If you also wish to trap errors that may be occurring after the first error, you have to connect the rear panel PULSED output to the STOP input, and make the following Control Page settings via softkeys:

Stop on Error:	OFF
Stop Slope:	Positive
Stop Delay	e.g. 15
(Set other parameters as required)	

Real Time Compare Mode

Real time comparison then stops after the 16th clock period (could be 17th or 18th, depending on clock frequency and propagation delay arising from the rear panel connection) following the occurrence of the error. The Error Map will display the compare result for at least 16 words following the error word. This is a useful method for determining if the error is sporadic or if a sequence of errors has occurred. Also in this case there is no display during error-free cycling.

Note that Stop Delay must be such that the analyzer stops within the cycle period. In other words, Stop Delay cannot be greater than the difference between the last address and the error address. Since errors can occur anywhere within the cycle period, i.e. on any address, it is better to start with a short delay first and then extend it according to the emerging pattern of errors.

Exercise - Stop on End (of Test)

An alternative to the techniques just described above is to let the Error Map display all errors occurring within a cycle period (i.e. within the address range between the First and Last Addresses). This means that you have to use the analyzer Stop Delay to determine the length of the compare cycle. Set **Stop Slope** to **INTERNAL** and set **Stop Delay** according to the formula:

$$\text{Stop Delay} = (\text{LAD} - \text{FAD}) - 1.$$

(You need to subtract 1 to compensate for the minimum Trigger delay.) In addition, make the following settings:

Stop Slope: Internal
(Set other parameters as required)

Start the generator in Auto Cycle. The analyzer is now receiving a continually repetitive stream of data without any time gaps between the Last Address and the First Address. Once again, record the compare reference data in the Trigger Start Analysis mode under identical triggering conditions to those about to be used in the Trigger Start Compare mode. You do not need to stop the analyzer after recording the reference data. Select Trigger Start Compare mode and make the following settings:

Stop on Error: OFF
Cycling Period: OFF

The analyzer now compares the incoming stream of data starting at the first address plus 1 with the data set stored in the high speed memory starting at address 00000. When it has reached the end of the cycle (i.e. compared the number of words entered in Stop Delay plus 1), it stops and displays the results on the Error Map. While the analyzer is updating the display, the generator carries on running. Therefore, one or more cycles from the generator may be lost, depending on the clock frequency and the number of words per cycle. The cycling diagram for such a set-up is shown in Figure 4-49.

Real Time Compare Mode

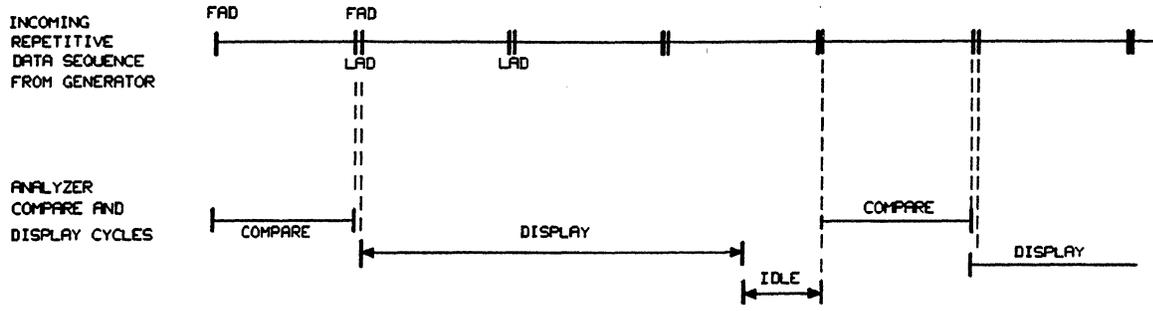


Figure 4-49. Cycling Diagram for Stop on End (of Test)

Chapter 5

Increasing Generator and Analyzer Channel Count

5-1 Introduction

A single generator can be fitted with a maximum of 16 channels, a single analyzer with 32 channels. This may not be enough for larger bench setups or for system operation. There are a number of ways you can increase the channel count on both the stimulus and analysis sides. This chapter deals with the channel expansion methods available to non-system users.

On the stimulus side there are two methods, and you can use one, the other, or both in combination. The first one is to add one or two Data Generator Extenders. This gives a maximum of 64 channels. The second one is to add a second Data Generator in a master/slave arrangement. This gives a maximum of 32 channels. However, a combination of these two methods enlarges the channel count to 128 channels.

On the analysis side there is only one way to increase the channel count and that is to add a second analyzer in a parallel master/master configuration. This boosts the channel count to 64.

Even larger channel counts are possible by running more than two generators with their associated extenders in parallel on the stimulus side and more than two analyzers in parallel on the analysis side, but such installations are beyond the scope of this manual. These are no longer bench setups but system installations, which require housing in rack/s and are driven by System Software. Note however, that the modular design of the system components (i.e. individual instruments) allows systems to be made up of any number of generators (with or without extender/s) and analyzers. A minimum system can consist of one generator and one analyzer. The information necessary for the installation and operation of systems is published in the System Configuration Manual and the System Software Manual.

5-2 Adding One or Two Extenders

Either one or two 8181A/B extenders may be interfaced to an 8180A/B Data Generator. The A-version extender has a memory depth of 1024 words, the B-version has a depth of 16384 words. Therefore, A-version extenders must always be connected to A-version generators, B-version extenders to B-version generators.

Before proceeding to add your extender/s, let us briefly discuss the new data channel arrangement. Figure 5-1 shows the input and output connectors of an extender. Notice that the data output connectors are labeled 4 to 9 and in brackets A to F. The first extender provides channels 4-0 to 9-3 (24 channels if fully loaded), the second extender (if present) provides channels A-0 to F-3 (also 24 channels if fully loaded). The alpha-numeric connector identifiers appear as Installed Connector numbers on the Miscellaneous Page. The identifiers are "fixed" to their respective connectors, therefore if certain channels are not installed, their connector numbers are not displayed on the Miscellaneous Page, but *space for them is still reserved*. Connector numbers are always reserved for their respective connectors. The output cables used with the extenders are standard generator output cables and are connected to the extender in the same way as to the generator.

Adding One or Two Data Generator Extenders

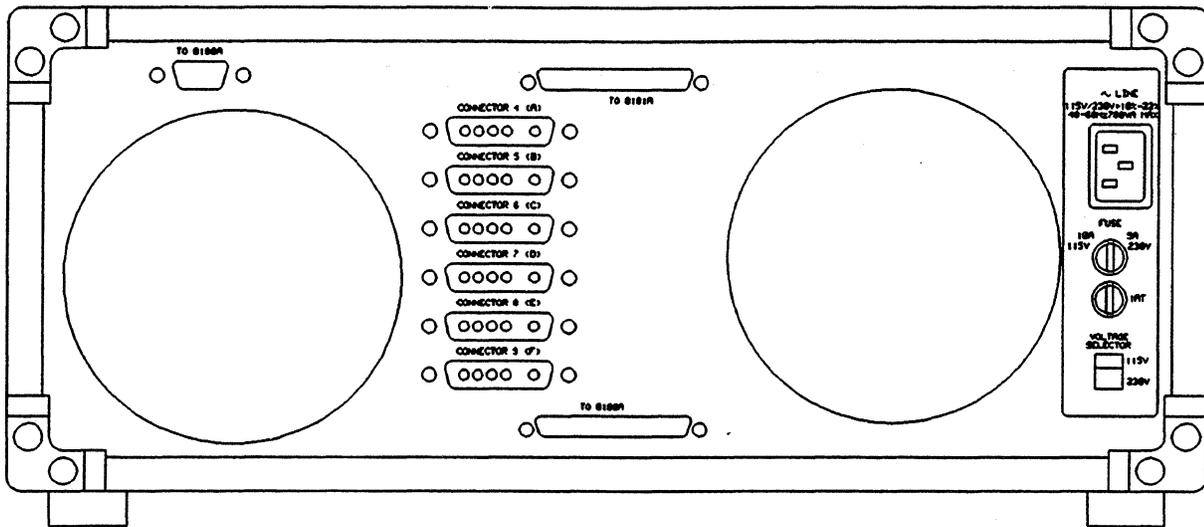


Figure 5-1. Extender Input and Output Connectors

Interconnecting Procedure



Always switch off any instruments before commencing work on electrical interconnections.

Installation of an extender unit involves electrical and mechanical interfacing to its controlling generator. The accessories making up the electrical and mechanical interconnecting kits are shown in Figure 5-2.

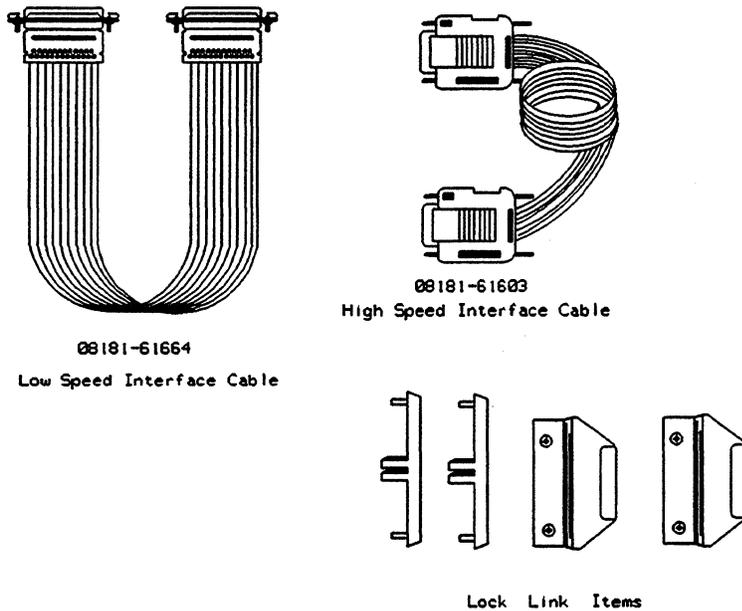


Figure 5-2. Parts of the Electrical and Mechanical Interconnecting Kits

Adding One or Two Data Generator Extenders

When mounting the extender/s to a generator using the short low speed interface cable 08181-61604, the instruments must be arranged such that extender 2 is always positioned on top of extender 1, which is itself positioned on top of the controlling generator, as is illustrated in Figure 5-3. A long low speed interface cable 08181-61664 is also available, and can be used in setups where space limitations do not allow the use of the short cable.

A mechanical mounting kit (supplied with extender) should be used to attach the instruments to each other. This reduces conducted RFI (radio frequency interference), as well as making the instrument stack more stable. Alternatively, a mechanical mounting kit HP 5061-9699 can be used to mount two instruments at a time together. These can be found in the Hewlett-Packard Catalog under Cabinet Accessories.

Each extender needs a High Speed Interface Cable and a Low Speed Interface Cable. Extender 2 obtains its low speed signals via extender 1. Connect these cables as shown in Figure 5-3. If only one extender is to be fitted then ignore the references to extender 2. For rack installations (described in the System Configuration Manual) use the longer Low Speed Interface Cable 0818161603.

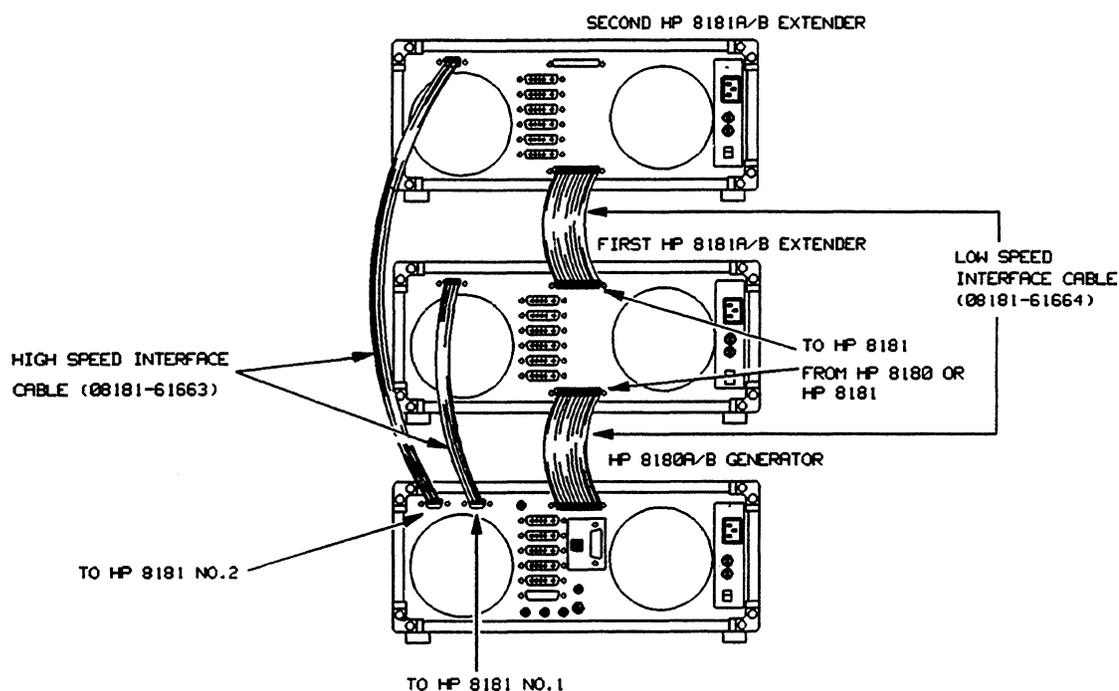


Figure 5-3. Generator and Extender Interconnections

Operation

The following functions of the resulting system will be exactly as set for the generator and will automatically apply to the extender/s without the need for additional settings.

1. Status
2. Cycle Mode
3. Clock Frequency
4. Clock Source
5. Output State
6. First and Last Addresses

Parallel Operation of Two Generators

All other settings for the extender/s are also made via the generator but with their own values set as required. The operating procedure for a generator with extender/s attached is very similar to that for a generator alone.

Switch on the generator and the extender/s. The system is now ready for use. Whenever an extender is switched off (or on) during parallel operation, a reset cycle is initiated and the generator display reverts to the power up status. This is necessary, as the generator takes the presence or absence of an extender into account only during the power-up/reset cycle.

If an extender has been switched off, a flashing message **HARDWARE**, displayed in line 2 warns of this condition. At the same time an inverse video flashing error message **EXTENDER POWER DOWN** is also displayed. If you wish to continue without the extender, press the softkey **CONTINUE** to re-enable page selection. The warning message **HARDWARE** is retained as a reminder. If two extenders are connected to a generator, then a reset cycle is initiated whenever *either* of them is switched on. However, only when *both* of them have been switched off is a further reset cycle initiated.

The extender channels are all of the DNRZ format (delayed non-return to zero), refer to discussion of formats in Chapter 3, Timing Page. All channels in one extender can be delayed in common, by accessing the extender delay menu. Press softkey **Extender 1** or **Extender 2** (if you have two extenders fitted) on the generator Timing Page and enter a value in the range 0 to 999 ms or use the **INCREMENT** or **DECREMENT** softkeys.

If the Standard Parameter Set is recalled with both extenders connected, the extender data channels are coded in hexadecimal format to enable all channels to be displayed on the screen.

As mentioned above, there are no significant differences for extender operation. In effect you now have a generator with an increased channel count.

5-3 Parallel Operation of Two Generators

A maximum of two 8180A generators can be connected together using the 15421A cable, giving synchronous parallel operation with a maximum of 32 channels. With this cable you can also connect two 8180B generators together, giving the same maximum channel count. To increase the channel count even further, you can connect three 8180B generators for parallel operation using the 15480A cable, giving a maximum channel count of 48. This requires an internal change in the master 8180B generator. The procedure is fully described in Chapter 5 of the System Configuration Manual. (You can of course add two extenders to each generator also in this setup, to obtain 192 stimulus channels.)

Interconnecting Procedure



Always switch off any instruments before commencing work on electrical interconnections.

To connect two generators for synchronous parallel operation, use the 15421A cable, plugging each end in the D-type connector marked **PARALLEL 8180A/B**. You can connect together generators of either version, but a mixed setup of one 8180A and one 8180B does not make much sense, unless you wish to work with only a 1K of memory.

The two instruments will be operated in a master-slave configuration. The slave generator is determined by the 15421A cable. One of the connectors has an identifying mark and whichever generator is

Parallel Operation of Two Generators

connected to this end is designated the slave. The diagram in Figure 5-4 illustrates the setup and shows how the external operating commands for both generators are given via the master.

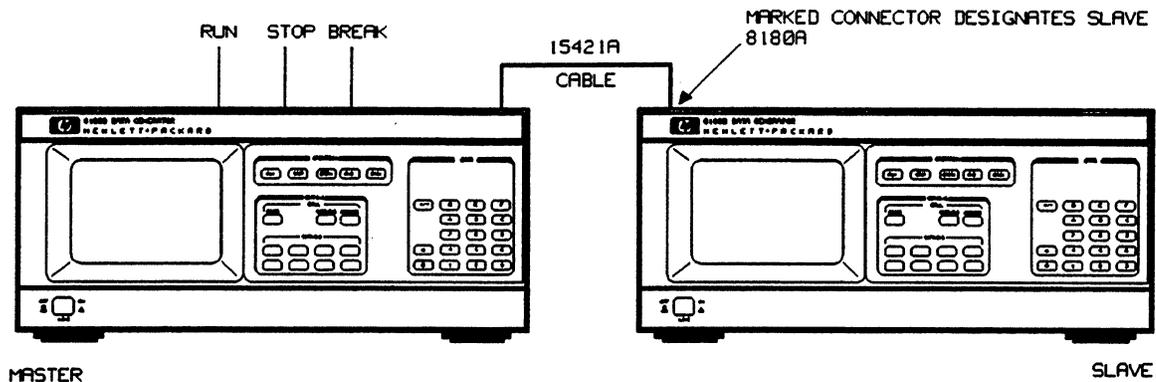


Figure 5-4. Parallel Synchronous Operation of two Generators

Modifications to Specifications

As mentioned in the specifications, the skew measured across both generators increases by 1ns. All other output and timing specifications remain as described for a single generator (and extender/s if connected).

Restrictions Concerning Both Master and Slave Generators

1. Back-stepping (BACK after a BREAK initiation) is not allowed.
2. Initialization cycle modes (INIT+AUTO, INIT+GATED) are not allowed.
3. Operating commands RUN, STOP and BREAK can only be made via the master, irrespective of command source (front panel, external input or HP-IB). The current state for both instruments is displayed only by the master.
4. The "Strobe breaks" function, if required, can only be set via the master.
5. Operating frequency (or period) and clock source can only be set at the master. Note however, if data timing format RZ=50% is set at the slave, the resulting width value will be determined by its own frequency setting which is not necessarily the same as the master's (unless set independently by operator).
6. For the following three settings: First Address, Last Address and Cycle Mode, the instruments should be stopped prior to making the required change to avoid any non-defined output status. These settings must be made separately on each 8180A/B and must be set the same for each instrument.

Restrictions Concerning only the Slave Generator

1. During timing parameter changes involving a range change, the clock signal is not interrupted (as it is in the master), which means that temporary non-defined conditions will occur.
2. Data changes cannot be made "on the fly" and the master must be stopped before changing slave data.

Parallel Operation of Two Analyzers

3. Error detection of frequency related settings e.g. delay exceeds value allowed by current period, can only be practically achieved via HP-IB programming (since the operative frequency is derived via the master 8180B). It is possible to manually enter the required frequency into the slave 8180B, for reference purposes etc. if wished.

The connection of extender/s to either the master or the slave generator does not cause any additional limitations to either instruments' operation.

5-4 Parallel Operation of Two Analyzers

General

Using the HP15416A accessory cable, the trigger conditions of two analyzers can be synchronized, thus increasing the number of data channels to a maximum of 64. The following section provides information on setup requirements as well as functional and parametric restrictions in parallel operation. A summary of the restrictions is given at the end of this section.

Setup Requirements

The setup in Figure 5-5 and Table 5-1 illustrates the basic connections and settings for parallel operation. To function correctly, both analyzers must be set to the same operating mode, connected to a common external clock (only synchronous data sampling is possible), and must have identical clock slope and threshold settings. Use two Solder-in Receptacles HP 15412A to connect the clock probe cables 15406A/B/C to a common clock source.

If a clock qualifier signal is applied for selective sampling purposes, then it must be connected as shown, although this signal is not mandatory for parallel operation. If not, set the Clock Qualifier Level to DON'T CARE on the Control Pages of both analyzers.

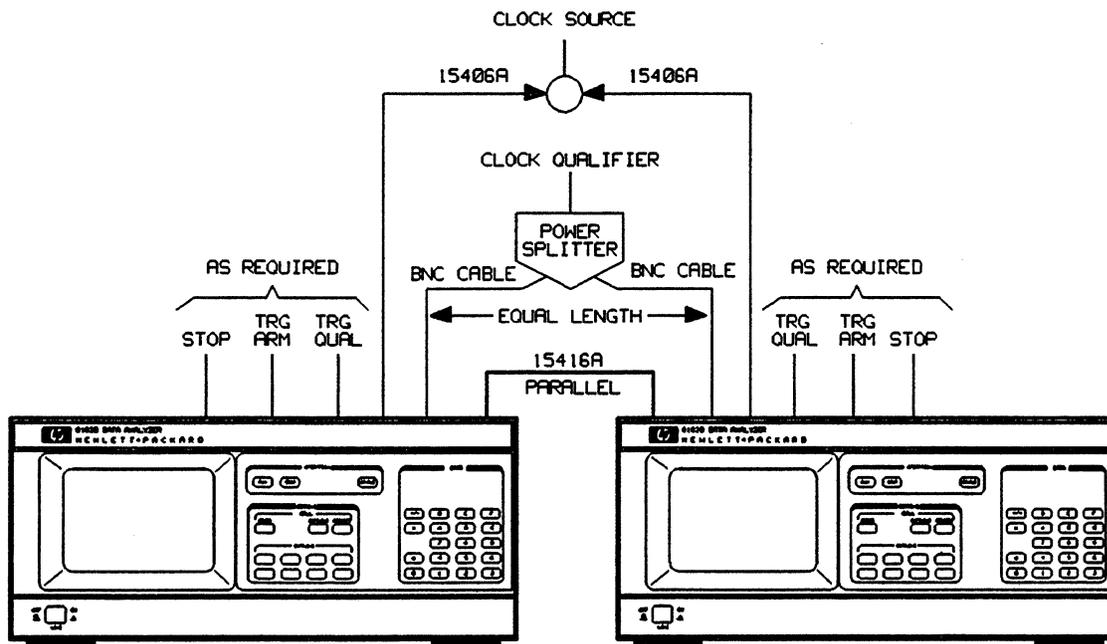


Figure 5-5. Parallel Operation of Two Analyzers

Parallel Operation of Two Analyzers

In order to reduce reflections in the Clock Qualifier feeder cables, you will have to use a 50 Ohm Power Splitter HP 11667A and three 50 Ohm N-BNC adapters HP 1250-0780.

Note that if you wish to use the Strobe signal (from the master generator in a multi-generator system) to trigger both analyzers, you will need the same splitting network as used for the Clock Qualifier signal (a Power Splitter, three N-BNC adapters and three BNC cables, two of which are of identical length). In this case, connect the two identical BNC cables to the TRG ARM inputs of the analyzers.

Table 5-1. Settings Required for Parallel Analyzer Operation

ANALYZER	1	2
Operating Mode	same as 2	same as 1
Clock Source	External	External
Clock Slope	same as 2	same as 1
Clock Threshold	same as 2	same as 1
Clock Qual. Level	same as 2	same as 1
Clock Qual. Thres.	same as 2	same as 1
Clock Qual. Imp.	50 Ohms	50 Ohms

Although both instruments are connected to the same clock source, the clock delay (and clock width in Real Time Compare mode) settings are independently programmable within the following range specifications:

Maximum Clock Delay:

95% of Period - 11ns

Maximum Delta Delay between analyzer 1 and analyzer 2:

95% of Period - 19ns

Note that in the event of different clock delays, the channel skew time is equal to the delay difference.

Data Capture

The data capture cycle is determined by the front panel OPERATION keys (RUN, SAMPLE, STOP) and the following Control Page settings:

- trigger conditions
- stop conditions
- autoarming

With reference to the OPERATION keys, a brief description of their role in parallel operation is given as follows:

RUN: Pressing either RUN key arms both instruments.

STOP: If the autoarming function is switched off for both instruments, pressing either STOP key stops both instruments. With autoarming switched on for one instrument (only one instrument should have autoarming enabled) then only the STOP key for this instrument can abort autoarming. Pressing this key stops both instruments.

SAMPLE: These keys function independently and their use is not recommended in parallel operation.

Regarding the Control Page settings, certain functions in parallel operation are dependent on the selected operating mode. They are therefore detailed according to mode below.

Parallel Operation of Two Analyzers

Analysis Modes (Trigger Start/Stop Analysis)

Whereas in single operation the trigger delay is immediately active at the end of the trigger count, in parallel operation the trigger delay counters of both instruments are synchronously started only when both trigger count conditions are satisfied, and the combined trigger word is true (see settings in Table 5-2). This is illustrated in the simplified timing diagram in Figure 5-6.

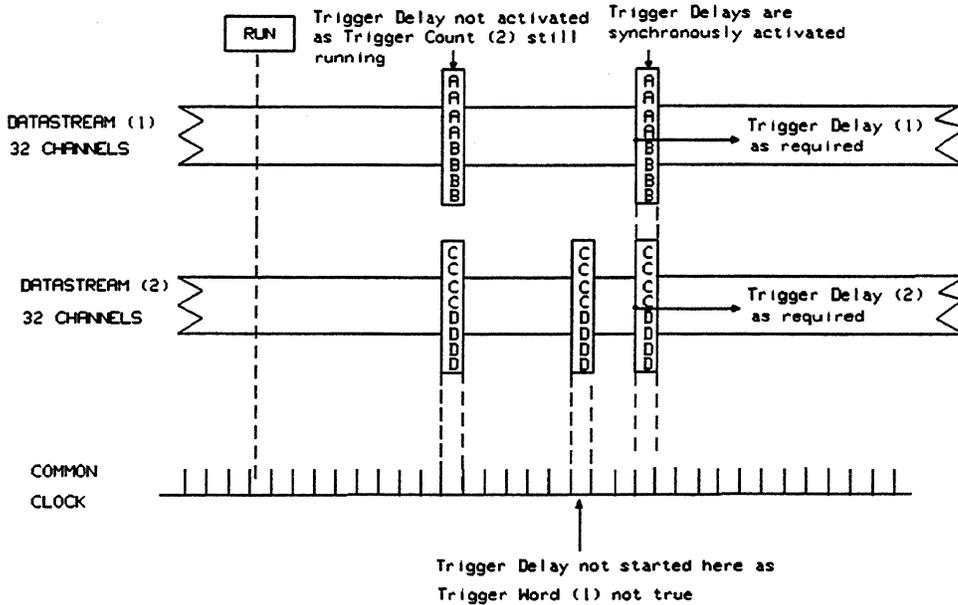


Figure 5-6. Parallel Triggering in Analysis Modes

For termination of the data capture cycle, all stop parameters on the Control Page of each instrument are independently programmable. Also, for repetitive data capture cycles, the autoarming feature should only be set on one analyzer. Both analyzers are then re-armed at the end of a capture cycle. Regarding the 'Abort on Compare Error' feature of autoarming, neither instrument is re-armed if the error occurs in an instrument set to autoarming.

Table 5-2. Settings for Parallel Triggering

ANALYZER	1	2
Trigger Arm Slope	Don't care	Don't care
Trigger Word	AAAABBBB(hex)	CCCCDDDD(hex)
Trigger Qualifier	Don't care	Don't care
Trigger Count	01	02
Trigger Delay	as required	as required
Allow Gaps	YES	YES

Real Time Compare Mode

The trigger sequence in this mode functions as already described for the Analysis modes, with the additional consideration that the Trigger Delay of both instruments must be set to a minimum of 2. The Stop on Error feature of this mode functions independently for both instruments, although a combined Stop on Error can be simulated using the setup shown in Figure 5-7 and Table 5-3.

Parallel Operation of Two Analyzers

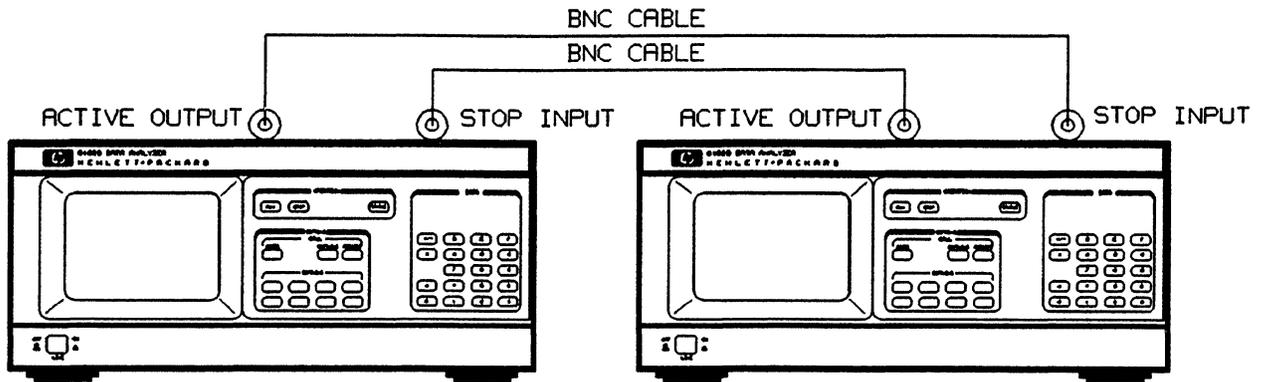


Figure 5-7. Setup for Combined Stop-on-error

Table 5-3. Settings for Parallel Stop-on-error

ANALYZER	1	2
Stop Slope	Neg. Slope	Neg. Slope
Stop Threshold	TTL	TTL
Stop Impedance	50 Ohm	50 Ohm

If the above setup is used, there may be a stop difference of a few words depending on the clock period and internal propagation delays. During data comparison, the Error Maps of both analyzers must be inspected to ensure error-free compare results (there is no combined error display). The rear panel error outputs (PULSED and LATCHED) of both instruments are also independent of each other. In the event of a combined output being required, the output signals can be added via a power splitter.

Summary

The following provides a summary of restrictions, parametric and operating, which apply to parallel operation.

Parametric

The only parametric restrictions refer to the Clock Delay settings and are listed as follows:

Maximum Clock Delay:

95% of Period - 11ns

Maximum Delta (Clock) Delay between both analyzers

95% of Period - 19ns

Operating

The operating restrictions are:

1. Only synchronous data analysis possible.
2. The minimum Trigger Delay in Real Time Compare mode is 2.
3. In Real Time Compare mode, there is no combined Stop-on-error.
4. All displays are instrument specific and cannot be combined on one screen.
5. The error outputs are instrument specific, but can be added via a power splitter.



Chapter 6

Device Measurements

6-1 Introduction

In this chapter we are going to perform actual device measurements. The device we shall use is the AM2902 sequencer, which is employed in bit-sliced CPU's. The measurements to be carried out are typical of those for which the 8180/1B and 8182B instruments are normally used:

- Propagation Delay
- Set-up Time
- Hold Time
- Output Level
- Data Stability

6-2 DUT Block Diagram

First of all, we are going to look at our device under test (DUT). Its block diagram is shown in Figure 6-1.

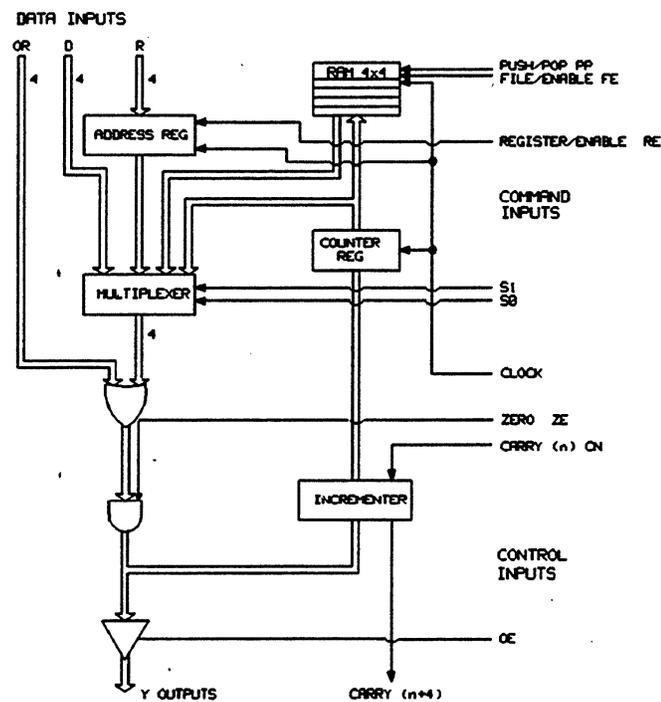


Figure 6-1. Block Diagram of the AM2909 Sequencer

In the upper left corner we see the input lines (OR, D and R inputs). The status of the lines S1 and S0 (on the right) determine which one of the data sources is switched through to the output of the sequencer. ZE sets the outputs to zero, and CN is the carry bit for the incrementing internal up-counter. For our measurements, we will use only one mode: R inputs will be switched to the output.

We shall drive the R inputs and the control lines (S1, S0, ZE, CN) with the generator and monitor the Y outputs and the control lines with the analyzer. The generator clock will be used to drive the sequencer and synchronize the analyzer to the generator. The strobe output will trigger the analyzer to start sampling data.

DUT Connection

6-3 DUT Connection

Before proceeding, we have to connect the device under test to the generator and to the analyzer. A number of methods exist and their use depends on the DUT interface hardware ordered with your test instruments or system. You may be using one of the following units:

- HP 15466A 256 channel testhead
- HP 15425A 84 channel testhead
- HP 15424A 84 channel performance board

All three are clean interface solutions providing 50 Ohm matching right up to the pins of the DUT. The two testheads are designed for IC test applications and are remotely controlled from a computer via the HP-IB. The performance board is designed for engineering applications and has a fixed configuration. The connection diagram in Figure 6-2 tells you which generator and analyzer channels are to be connected to which device pins. However, for the physical wiring connections and subsequent testhead configuration refer to the Testhead Manual and the System Configuration Manual.

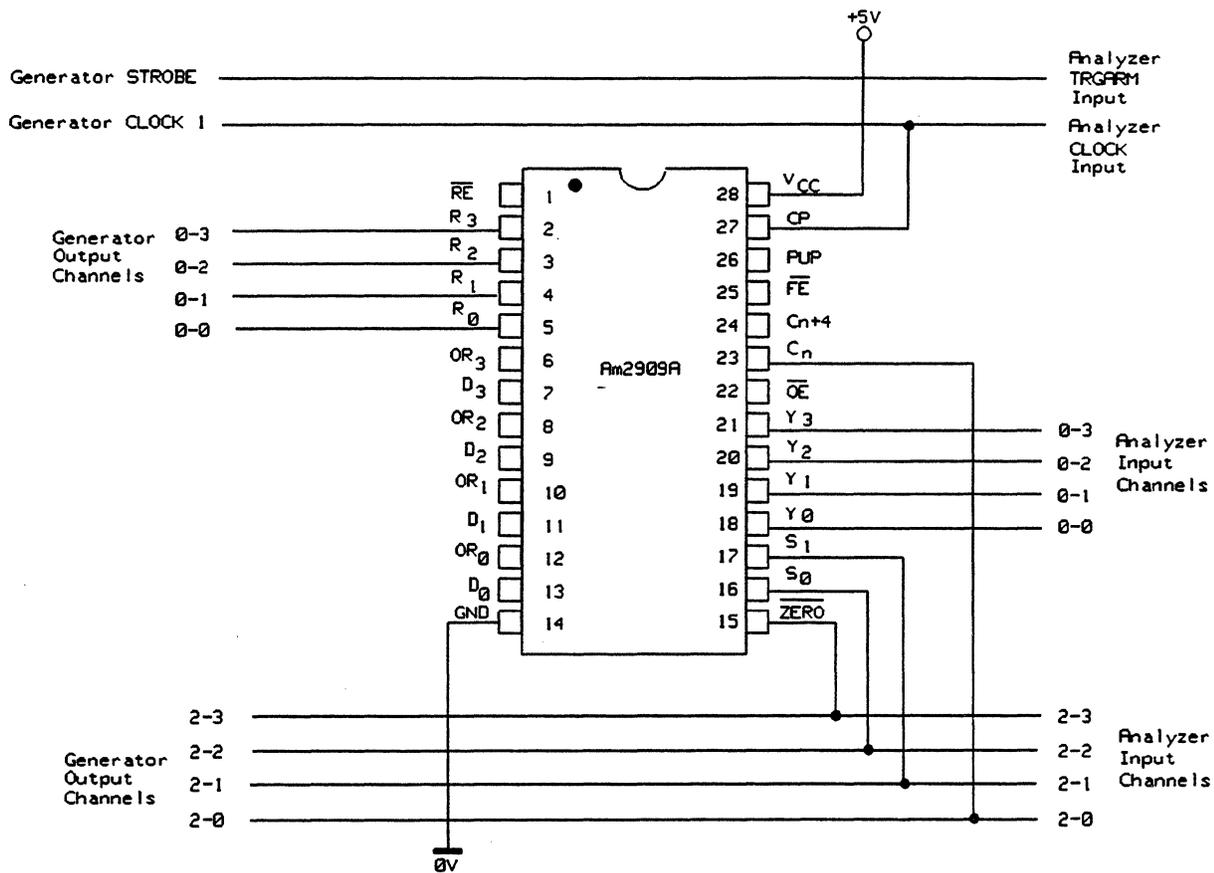


Figure 6-2. Connection Diagram for the AM2909 Sequencer

Generator Settings - General

6-4 Generator Settings - General

When the connections are made, we can set up the generator so that it will provide the signals required by the sequencer to run. In order to establish a known starting point for the generator settings, it is good practice to recall Standard Set and then modify where necessary. Let's do this. (Generator settings after Recall Standard Set are listed in Appendix A, Table A-1.)

Recall Standard Set

Now call up the Control Page. All we need to change here is the Last Address which we set to 79.

Control Page Last Address: 0079

On the Timing Page change the Frequency, Clock 1 Delay and Channel Format as shown below.

Timing Page Frequency: 2 MHz
 Clock 1 Delay: 15 ns
 Channel Timing: All channel format RZ

Next, call up the Output page. For this specific test we need eight channels to drive the sequencer. Let us therefore configure the generator to display only eight channels, even if it is equipped with more. Use the Channel Configuration feature to do this. In addition, set label A and the strobe channel to TTL levels, and turn on generator outputs.

Output Page Channel Configuration
 Connector 2222 0000
 Channel 3210 3210
 Label AAAA AAAA

 Set Label A to TTL levels
 Set Strobe to TTL levels
 Set Outputs to ON

To set up the bit pattern, call the Data Page. The data we need to set up is shown below. We set a 1 in the strobe channel at the first address, i.e. address zero, since we want to synchronize the analyzer with this bit. The analyzer accepts the strobe signal at the TRIG input on its rear panel and uses it to trigger each analysis cycle.

The next four bits on the display represent the channels in connector 2 which we have connected to the control inputs of the sequencer. From its data sheet we know that it needs the bit pattern shown below in order to read the R inputs, which is where we have connected the data lines. (If, for example, all lines of the connector 2 were high, the sequencer would ignore the R inputs and read the D inputs instead.) The data pattern on the channels of connector 0 is simply an up-counter.

Data Page	ADDR		STR	DATA
	0000	F	1	1101 0000
	0001		0	1101 0001
	0002		0	1101 0010
	0003		0	1101 0011
	0004		0	1101 0100
	.		.	Conn 2 Conn 0
	.		.	.
	.		.	.
	.		.	.
	0079		0	1101 1111

Analyzer Settings - General

6-5 Analyzer Settings - General

As on the generator, we begin by Recalling the Standard Set of parameters which we find on the Miscellaneous Page. (Analyzer settings after Recall Standard Set are listed in Appendix B, Table B-1.)

Recall Standard Set

Next, call up the Control Page. Set the clock delay to 40 ns (high enough to be on the safe side with respect to the propagation delay of the device). Set Trigger Arm to Positive Slope and Stop Delay to 79. Set Autoarming (the pause time between measurements) to a delay of 1 second.

Control Page	Clock Delay:	40 ns
	Trigger Arm:	Positive Slope
	Stop Delay:	79
	Autoarming:	Delay 1s

On the Input Page, use the Channel Configuration facility to display only those channels where there is relevant information, i.e. connectors 0 and 2. Set both of these connectors to Dual Threshold.

Input Page	Channel Configuration	
	Code	BIN BIN
	Connector	2222 0000
	Channel	3210 3210
	Label	AAAA AAAA
	Connector 0 and 1 to Dual Threshold	
	Connector 2 and 3 to Dual Threshold	

On the State List Page disable Error Display

State List Page	Display Errors:	NO
------------------------	-----------------	----

Pressing the RUN key on both the generator and analyzer, we now get one reading per second.

The State List Page displays data contained in the Received Data memory. If we now stop the analyzer (by pressing its STOP key) and make a visual comparison of the data displays of the generator and the analyzer, we will find that they are identical, telling us that the device is functioning properly under the given conditions (levels, frequency, and so on).

We now want to download the received data into the Reference memory and then command the analyzer to display errors. We do the downloading by using the Dump Recorded Data function on the Expected Data Page. After this, any errors that are received by the analyzer will be compared against the correct data in the Reference memory and highlighted on one of the Analysis Display Pages (State List, Timing Diagrams or Error Map). But first we restart the analyzer.

Press RUN

Expected Data Page	Dump Recorded Data
State List Page	Display Errors: YES

The analyzer now runs again, displaying the incoming data from the sequencer. But now, any errors that come along will be easily recognizable. To observe this, disconnect connector 0 (channel 0 of the analyzer) from the testhead/performance board and watch the effect on the analyzer.

Analyzer Settings - General

Reconnect it, and alter one bit in the up-count sequence of the generator in addresses 00005 and 00025. Clearly, both words cannot be displayed simultaneously on the State List Page. At a glance, the Error Map gives us all the information we need for a functional test. The cursor gives access to error details.

Before going on to the next section, correct the errors introduced at addresses 00005 and 00025.

Propagation Delay Measurement

6-6 Propagation Delay Measurement

Before making the measurement, let us briefly review propagation delay. It is simply the time elapsed from clocking the data into a device to its output changing, as is shown in Figure 6-3. It is, therefore, a very significant factor affecting the overall speed of a device.

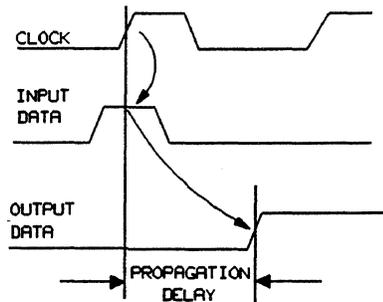


Figure 6-3. Principle of Propagation Delay

Figure 6-4 shows the signals provided to the sequencer. The data is present at the input before the active (positive) clock edge occurs. This clock edge triggers both the sequencer and the analyzer.

We have set up the analyzer so that it samples the output of the sequencer 40 ns after triggering, giving the output more than enough time to change. We now want to determine the precise position of the output edge. This is achieved by moving the sampling point to earlier values (reducing the analyzer clock delay) until different data is read. This will happen when the clock delay becomes shorter than the propagation delay.

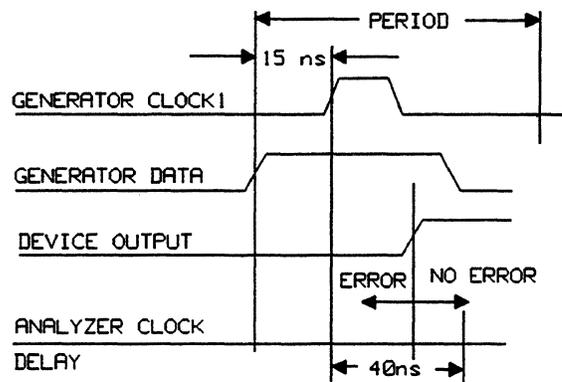


Figure 6-4. Measuring the Propagation Delay of the AM2909 Sequencer

A simple way of determining when readings change is by monitoring the Error Map while changing the analyzer Clock Delay. To do this we make use of the key SOFTKEYS and create a mixed display consisting of Error Map Page report area and Control Page softkeys (where Clock Delay is available).

When the Error Map Page is called up, it appears with its own softkeys. However, the instrument permits us to maintain a current report while calling up softkeys from a different page. We have already done a similar exercise in the previous chapter. Now we are going to press the SOFTKEYS button to access all softkeys. Since we know that Clock Delay is on the Control Page, we shall call it up, this time getting only the softkeys. Then we'll select Clock Delay and once on the display, decrement it until errors show up on the Error Map.

Propagation Delay Measurement

Call up: Error Map Page

Press: SOFTKEYS

CONTROL

Clock

Clock Delay

DECREMENT

Adjust the analyzer Clock Delay so that the errors have just disappeared, and read the numerical value off the screen. This is the propagation delay of the sequencer. Refer also to Figure 6-4.

Set the Clock Delay back to 40 ns before proceeding to the next measurement, which involves set-up time.

Set-up Time Measurement

6-7 Set-Up Time Measurement

Set-up time is the time interval during which data must be present and stable (unchanging) at the data input before it can be clocked in. Some devices can tolerate the appearance of data at the input after the clock edge has occurred. In these cases, the set-up time is negative.

To measure set-up time, we need to vary the delay between the clock and data outputs of the generator, as is illustrated in Figure 6-5.

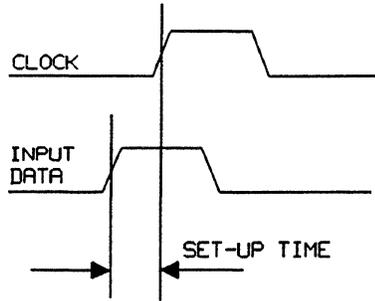


Figure 6-5. Principles of Set-up Time

We do this by setting the generator clock delay to say 15 ns and increasing the delay of all data channels from zero until errors begin appearing on the Error Map - see Figure 6-6. This indicates that the data has not been present long enough prior to the clock edge, causing the device to incorrectly read the data. We now decrease the delay of all channels until the errors just disappear. The minimum set-up time is the difference between the clock delay and the delay of the data channels. A typical range for the AM 2909A sequencer is 0.3 to -0.3 ns, while a typical value for the AM 2909 is 3 ns.

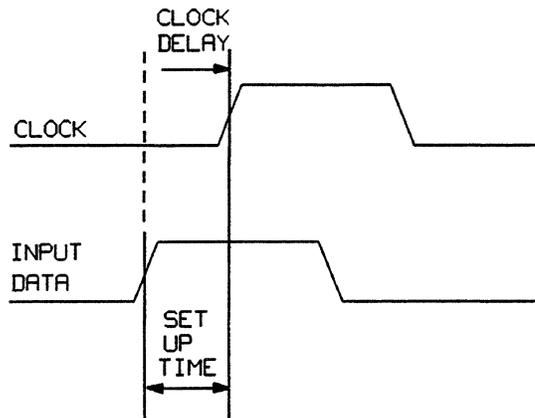


Figure 6-6. Measuring the Set-up Time for the AM2909 Sequencer

Set the delay of all channels back to 0 before going on, so that we can be sure we are seeing the effects of only one parameter at a time.

Hold Time Measurement

6-8 Hold Time Measurement

Hold time is the time interval over which the input signal must be present *after* the active clock edge has occurred. This is shown in Figure 6-7.

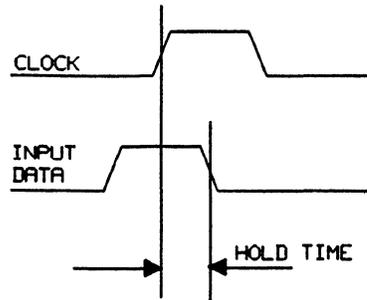


Figure 6-7. Principles of Hold Time

Some devices can tolerate the occurrence of the trailing edge of the data before the clock edge. In these cases the hold time is negative. In order to determine the minimum hold time required by the sequencer, we need to move the trailing edge of the data input towards the active clock edge. We do this by reducing the width of the data outputs of the generator until errors occur on the analyzer's display. This indicates that the data has not been present long enough at the input of the sequencer to be read in properly. Then we increase the width until the errors just disappear. This is then the hold time requirement for the sequencer.

In order to calculate the minimum hold time, we have to subtract the clock delay (set for instance to 15 ns) from the current data width, as you can see in Figure 6-8. A typical hold time for this sequencer is 1.5 ns (AM2909A) or -1.0 ns (AM2909).

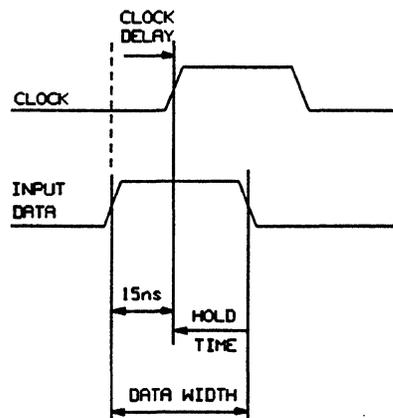


Figure 6-8. Measuring the Hold Time for the AM2909 Sequencer

Set the data width back to 50 ns before proceeding. Minimum set-up time and minimum hold time cannot be measured simultaneously, because the minimum data/clock width is 10 ns. In any case, manufacturers specify that set-up time be measured with a long hold time, and hold time be measured with a long set-up time.

The measurements we have just made demonstrate the importance of the Error Map. At a glance, it provides information about whether or not a test sequence has been received correctly. In addition, we can see the usefulness of the timing resolution of 100 ps for parametric measurements.

Level Measurement

6-9 Level Measurement

The 8182B analyzer can perform dual threshold measurements, comparing an input signal against two threshold levels which can be set independently. With the analyzer configured in this way, a signal must exceed the upper threshold to be recognized as high, or fall below the lower threshold to be recognized as low, as shown in Figure 6-9. If neither condition is satisfied, the level is interpreted as intermediate.

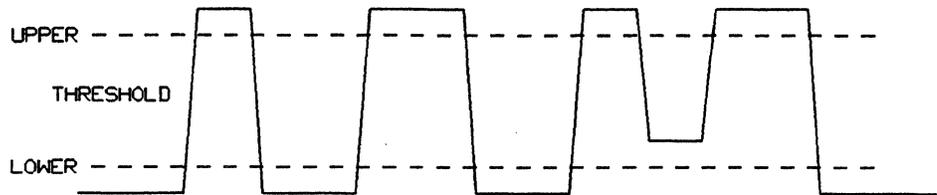


Figure 6-9. Level Measurement Using Dual Threshold

We shall now measure the high level voltage of the sequencer output. By recalling Standard Set, we have set all input channels of the analyzer to label A, with an upper and lower threshold of 2.0 V and 0.8 V respectively. As no errors appear on the Error Map, the conditions are being satisfied.

Raise the upper level of label A to 2.45 V and monitor the Error Map. There should be errors in nearly every word now. A closer look (using the cursor) reveals that intermediate levels occur only in the first four bits. Those are the control lines, the high level of which we have set to 2.4 V at the generator. If you now switch to the State List Page you will see that these errors are actually intermediate levels, displayed as dashes in inverse video fields. These same errors are displayed on the Timing Diagrams Page as half height pulses.

To ignore the control lines, which we don't wish to measure at this time, we can do one of two things:

1. Mask them off in the Expected Data Memory.
2. Apply different level criteria to the control lines (connector 2) and the data lines (connector 0).

We shall use method 2. Call up the following:

Input Page	Channel Label		
Assign the following:	Code	BIN	BIN
	Connector	2222	0000
	Channel	3210	3210
	Label	BBBB	AAAA

This method has the advantage that we can now check the high level of the data lines alone and disregard the levels of the control lines. Raise the upper threshold of label A until errors occur, then lower it until they just disappear. The numerical value which can now be read from the analyzer's display is the high level which is safely exceeded by the output of the sequencer.

Glitch Detection

6-10 Glitch Detection

The DUT output signal may look something like the waveform in Figure 6-10. We can check for any glitches or multiple level crossings within a single period by enabling the Glitch Detect facility on the Control Page and monitoring the result on the Timing Diagrams Page.

We can use the setup and technique from Section 6-10. When raising the level of upper threshold Label A from the original setting of 2V, glitches will appear before errors (intermediate levels) because of slight overshoot on the input lines to the analyzer. As we drive the level even higher, the glitches disappear and errors appear instead. Then we have the case already discussed in Section 6-9.

We can observe glitches on the State List, Timing Diagrams and Error Map Pages. For this exercise we are going to use a mixed display of a Timing Diagrams Page report and the softkeys from the Input Page.

Control Page	Glitch Detect
	ON
Timing Diagrams Page	Select Displ
	Disp Glitches
	YES

Now, while still in the Timing Diagrams Page call up the softkeys of the Input Page by pressing SOFTKEYS and **INPUT**. Select **Threshold** and increase the level of the upper threshold of Label A until glitches occur. This should be around 3.3V, as we are measuring the output of the sequencer.

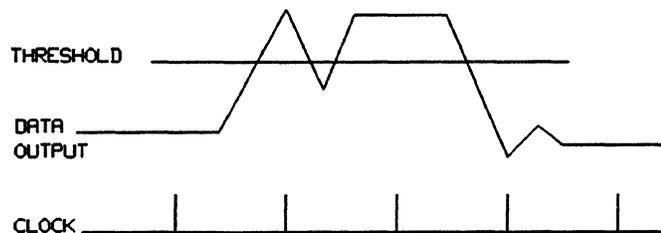


Figure 6-10. Detecting Glitches at Outputs of the MA2909 Sequencer

Before proceeding to the next test, set the upper level of label A on the analyzer to 2.0 V.

Real Time Compare Measurement

6-11 Real Time Compare Measurement

In this section we are going to perform a timing measurement on the sequencer using the real time window comparison available on the analyzer. We shall set the size of the time window with the **Clock Delay** and **Clock Width** softkeys.

Setting Trigger and Stop Conditions

Before selecting Real Time Compare mode, we need to record the data pattern to be used later for comparison (i.e. the reference data) and load it into the Expected Data memory. We have to set the size of the data capture block using the **Trigger** and **Stop** softkeys on the Control Page. It is important that we record the data under the same triggering conditions as those that will be used in Real Time Compare mode. Therefore, while still in Trigger Start Analysis mode, we shall set Trigger Delay to 00001, since this is the minimum Trigger Delay in Real Time Compare mode.

The end of the data capture block will be determined by the Stop Delay (Internal Stop). Stop Delay must be equal to or greater than the difference between generator Last Address and First Address. In our test exercise, First address (FAD) is set to 00000 and Last Address (LAD) is set to 00079. Therefore we are going to set Stop Delay to 00079. Having done this, we shall start the analyzer in order to record reference data. Finally, we'll dump the recorded data into the Expected Data memory.

Control Page Trigger Delay: 1
 Stop Delay: 00079

Start analyzer (press RUN)

Expected Data Page **Edit**
 Dump Rec. Data
 EXECUTE

If you now compare the analyzer Expected Data Page with the generator Data Page, you will see that generator second word equates to analyzer first word, generator third word equates to analyzer second word, and so on. Generator first word is registered on the analyzer as the last word. Address 00000 on the analyzer therefore contains the word 1011 0001.

Having recorded the reference data, we can switch to the Real Time Compare mode and start the analyzer. The Error Map Page should show no errors.

Control Page Operating Mode: Trigger Event Start Compare

Start Analyzer

Select Error Map Page

Checking Data Stability Using Window Compare

Now determine how long the data at the output of the sequencer is stable while the analyzer is running at 2 MHz. Do this by monitoring the Error Map on the analyzer while increasing the clock width (use softkeys from the Control Page while displaying the Error Map). Typical values should be around 480 ns.

Set Clock Width to 500ns
Monitor Error Map
Decrement Clock Width until errors disappear

Real Time Compare Measurement

Note that although this comparison is performed in real time, it is being interrupted. The analyzer is set up to stop after every cycle of 80 words and display the result. This means that the analyzer ignores the inputs during the display period, and failures occurring during this interval will go unnoticed.

Set Clock Width to 100 ns before proceeding further.

Continuous Comparison Using Autocycling

Next, we are going to set up the analyzer to continuously (without interruption) monitor the incoming signals and stop only when an error occurs. Incoming data will be compared with the reference data in the high speed RAM, and in the absence of errors the analyzer display will not be updated. The cycling period must be identical to (or a multiple of) the data repetition length. No other period makes sense, as the Cycling Period = $(LAD-FAD+1)*N$, where $N=1,2,\dots$

Control Page	Stop Slope:	Not Active
	Stop on Error:	ON
	Cycling Period:	00080

There is now no display on the Error Map. The analyzer status is ACTIVE and the Error Count shows 00000.

Note that if a bit is changed in the first word of the generator, the message Compare FAILED appears on the screen, but no square signifying an error is displayed. To display this error, select a cycling period twice the length of the data stream ($N=2$ in the above equation).

Set the Cycling Period back to 00080.

To see the effect of an error at some other address, change one bit of the generator's data output. (Change any bit of connector 0, so as not to alter the function of the sequencer.) Display is drawn only when a stop condition is true e.g. Stop On Error. Stop On Error = OFF permits longer term continuous counting of the error pulse using an external counter hooked up to the PULSED error output.

Chapter 7

Generator Programming

7-1 Introduction

In this chapter we are going to discuss generator remote programming using the HP-IB (Hewlett-Packard Interface Bus). HP-IB is Hewlett-Packard's implementation of the ANSI/IEEE-488 interface, "Digital Interface for Programmable Instrumentation". The generator has an HP-IB connector, and supports the IEEE Standard 488-1978 and the ANSI Standard MC 1.1. It can be remotely programmed from any controller or personal computer (PC) equipped with a suitable interface and supporting this standard.

The generator is programmed by means of HP-IB commands, sent to it from the controller. In this way every operating parameter can be accessed. Generator programming is therefore independent of the controller or the programming language used.

The generator is supported by the HP 9000 Series 200 and 300 family of technical computers. In this manual HP BASIC is used as the programming language. You can use HP BASIC and instrument HP-IB commands to write your own test routines and programs. It is the task of this and the next chapter to introduce you to HP-IB programming of the generator and the analyzer, and to show you how you can put together complete test programs to test various device parameters.

If you do not wish to write your own test programs, you can use the HP 81810S System Software, which supports systems ranging from a single generator and analyzer, right up to large installations of multiple generators and analyzers. The System Software allows interactive or "batch" testing of devices and can be used by people with little programming experience. It is written in HP BASIC and is therefore an open system. For further information refer to the System Software Manual.

HP-IB Cable Connection

The available HP-IB cables are the following:

- HP 10833A - 1.0 m (3.3 ft) cable
- HP 10833B - 2.0 m (6.6 ft) cable
- HP 10833C - 4.0 m (13.2 ft) cable
- HP 10833D - 0.5 m (1.6 ft) cable

To connect the generator to the computer, simply plug either end of one of the above cables into the HP-IB connector of the computer and the generator and tighten the retaining screws using your fingers. At the computer end you will probably already have a connection to the disc. So plug the new cable into the one already present.

The devices making up your system (generators, analyzers, computer, disc and so on) can be connected together in any configuration (star, linear or both) as long as the following rules are observed:

- The total number of devices connected to one computer HP-IB interface is not greater than 15.
- The total length of all cables used is not greater than two meters times the number of devices connected together, up to a maximum of 20 meters.

If your individual cable lengths exceed 4 meters, refer to operating guidelines in the IEEE Standard 488-1978. Do not stack more than three cable connector blocks together on any HP-IB connector. The resultant leverage can exert excessive force on the mounting panels. Make sure that all connectors are fully seated and that the lock screws are firmly finger tightened. *Do not use a screwdriver to tighten the lock screws.* You may use a screwdriver to release the screws.

7-2 Generator HP-IB Addresses

The generator is connected to a computer by means of the HP-IB. The generator will not be the only piece of equipment connected. There will most probably be an analyzer and a disc drive, and there may also be a testhead, other generators and/or analyzers, a printer and so on. Each device must have its own address which the computer can select in order to communicate with that device.

The generator has two HP-IB addresses, and 2 modes of remote operation based on the two addresses.

HP-IB ASCII Address

The ASCII address is used by the computer to communicate with the generator in the ASCII mode in which data, and parameter and mode settings are transferred over the bus as a series of ASCII bytes. The ASCII message is then interpreted by the instrument and executed.

The HP-IB ASCII address can be set directly on the HP-IB address switches on the back panel of the generator. If you wish to find out the current setting of this address, you can either look at the address switches (shown in Figure 7-1), or read it on the Miscellaneous Page of the instrument, which is shown in Figure 7-2. To access the Miscellaneous Page, switch on the instrument and press the PAGES key followed by the **MISCELLANEOUS** softkey.

There are five binary HP-IB address switches, giving an address range of 00000 to 11101 binary, or 0 to 29 decimal. Settings of 11110 and 11111 binary or 30 and 31 decimal are illegal. The switches are marked "1" and "0". To change the HP-IB ASCII address, slide the switches to the appropriate position using a pointed object, such as a small screwdriver.

NOTE

You can change the setting of the address switches with power on. Any changes will take effect immediately, unless the generator is currently communicating via the HP-IB, in which case they will take effect when the HP-IB is no longer busy.

NOTE

The address immediately following a generator ASCII address may not be assigned to any device on the bus.

NOTE

When changing the switch setting or connecting a number of instruments to one computer, make sure that every device on the bus has a unique address. This includes also the address of the HP-IB interface card of the active controller (the computer), which has a factory setting of 21. Therefore avoid setting the ASCII address switches to either 21 or 20 (see HP-IB Binary Address later), otherwise bus contention problems will occur.

Generator HP-IB Addresses

If you suspect that the address of the HP-IB interface card has been changed, you can find out the new address with the command:

```
STATUS SC,3;N_v  
PRINT N_v
```

where SC is the HP-IB interface select code, currently set to 7, and 3 is the HP-IB Status Register 3 which contains the HP-IB address. N_v is any valid name for a numeric variable.

For more details on the command and the Status Register refer to the BASIC 4.0 Language Reference. Select codes are covered in the next section.

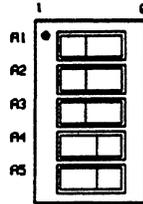


Figure 7-1. Generator HP-IB Address Switches

8180B	Status	STOP
Address		
----- MISCELLANEOUS -----		
Autoexit	OFF	
Display Brightness	█	
----- FOR INFORMATION ONLY -----		
HP-IB ASCII Address	07	
HP-IB Binary Address	08	
Total Channels	16	
Timing Channels	8	
Installed Connectors	0123	
Select Further	-----	
Autoexit	Brightness	

Figure 7-2. Miscellaneous Page

HP-IB Binary Address

The binary address is used to transfer blocks of binary data at high speed between the computer and the generator. This is covered later in Section 7-8, Generator Fast Binary Transfer.

There are no switches on the generator to set the binary address. Whatever the setting of the ASCII address, the binary address is always one higher than the ASCII address. This is why you cannot allocate the address immediately following the generator's ASCII address to any other device on the bus. The binary address is also displayed on the Miscellaneous Page.

7-3 Concept of HP-IB Programming - Generator

The instrument is programmed by sending the appropriate listen address plus an HP-IB command which can be followed by numerical values and units. We shall illustrate this technique with some exercises using the ASCII mode in just a moment. But first, we have to look at one additional aspect of HP-IB programming.

Select Code

When you send an HP-IB command to the generator, it is not enough to specify just the two-digit address of the required instrument. You have to precede this with another single or double digit number specifying the *Select Code* of the computer plug-in HP-IB interface to which your generator is connected. You may have two HP-IB interfaces in your computer, a high speed one linking the disc drive/s to the computer, and a low speed one for the instruments making up your test system and any other slow peripherals such as a printer. In some larger systems there may be a third HP-IB interface for further instruments.

To find out the Select Code, look at the adhesive label attached to the HP-IB Interface Card plugged into rear of the computer, or (better still) look at the Boot ROM Message which appears on the computer screen when booting the BASIC Operating System. This message lists all the interface and other cards installed in the computer, together with their select codes. Note that you have to press the space bar on the computer keyboard several times after the Boot ROM Message appears in order to pause the Auto-loader program. You will then be able to study the entries on the screen without them disappearing again. (To restart the Auto-loader type in the code for the operating system required, exactly as displayed on the computer screen.)

The normal select codes for HP-IB interface cards are:

- 7 - First HP-IB Interface
- 8 - Second HP-IB Interface
- 14 - Fast HP-IB Interface for Discs

Let us assume that your HP-IB interface card has a Select Code of 7 and the generator connected to this card via the HP-IB cable has an address of 07. To send a command to this generator, the full address has to be specified. Thus to recall the Standard Set on this generator, you would type in the following:

```
OUTPUT 707; "RSS" 
```

Exercise - Setting Generator Last Address

Set the last address of the generator to 800.

The HP-IB programming command for the last address is LAD and it has to be followed by a *number*, in our case 800. Type in the following:

```
OUTPUT 707; "LAD 800" 
```

Note that you have just programmed a parameter interactively, without actually writing a program. Note also that it is not necessary to call up a specific page prior to programming a parameter. Every parameter is directly accessible.

Concept of HP-IB Programming - Generator

20 Puts the generator in the remote listen mode and instructs it to display the Output Page. It then instructs it to recall the Standard Parameter Set.

30/50 Ramps up label D low level from -2V to +1V in 10mV steps.

While the program is running, you can observe the low level of label D stepping from -2V to +1V in steps of 10mV.

NOTE

The generator accepts a new programming line only after it has settled at the values of the previous one (but see subsection "Synchronizing Character" below). Therefore, the programmer need not worry about settling times of the instrument.

From these two examples we have seen how to program generator parameters. We will discuss more commands as we go along. A complete listing of the HP-IB commands together with the syntax for each is given in Chapter 10, HP-IB Syntax Diagrams.

HP-IB Command Syntax

All HP-IB commands always start with three letters (upper or lower case, but upper case is preferred for readability). The letters may be the whole command, or may be followed by a digit (number), letter, several digits or several letters. The precise syntax for each HP-IB command is explained individually in Chapter 10, HP-IB Syntax Diagrams.

HP-IB Command Delimiters

You can place one or more HP-IB commands on a single BASIC program line. For instance, in line 20 of the above exercise we have two HP-IB commands on a program line. You can place even more commands on a single BASIC program line as long as there is space on that line.

If you wish to place multiple commands on a program line, you have to separate them by delimiters. Valid delimiters can be the following characters:

- a blank (space) " "
- a comma ","
- a semicolon ";"

In line 20 we have used a blank. As you are about to see, blanks are used a great deal in the example programs in this chapter because it is easy to see the individual HP-IB commands. As you will also see, semicolons are used on certain occasions. A semicolon (or a comma) must be used when a programming command does not have a fixed length such as in the case of the CAS or ADS command. The length of these commands depends on the size of the segment to be set up (refer to Section 7-6, Output Page Programming). If you always want to be sure use a comma or a semicolon for a delimiter.

Synchronizing Character

The synchronizing character (sent to the generator) has the effect of locking up the HP-IB until the programming command or commands preceding it have been processed by the generator. The processing times of HP-IB commands vary considerably from command to command, with some being processed in

Concept of HP-IB Programming - Generator

several milliseconds, while others, notably the up- and down-counter commands, may require times of the order of tens of seconds, depending on the segment size and memory depth.

The synchronizing character for the generator is the carriage return. In applications where high processing speed is not required, you can send the synchronizing character after each HP-IB programming command, resulting in one command per line. The generator will then process the commands sequentially, not accepting the next one until the previous one has been processed.

This practice may be fine for simple programs such as those given in this chapter, where only one generator is being controlled. However, in large systems with several generators and analyzers on the HP-IB, such an approach may result in unacceptably slow response times for the system as a whole. To illustrate this, consider the following example.

Let us assume that we are running three generators in parallel and each generator is configured to contain one 16-channel segment. We wish to set up an up-counter on each of these three segments. We could use the following program lines to set up the up-counters:

```
o                                     o
o                                     o
o      1000  Gen1=700                  o
o      1010  Gen2=702                  o
o      1020  Gen3=704                  o
o      1030  OUTPUT Gen1;"UPC1"        o
o      1040  OUTPUT Gen2;"UPC1"        o
o      1050  OUTPUT Gen3;"UPC1"        o
o      1060  END                       o
o                                     o
o                                     o
o                                     o
```

The BASIC system automatically supplies a carriage return and a line feed to the HP-IB programming commands (in lines 1030 to 1050) and sends them to the bus. Generator 1 will therefore lock up the HP-IB until its up-counter has been set up. For the full memory range of 16384 bytes this takes almost 30 seconds. Only when the up-counter is completed can the next up-counter command be sent. Thus loading all three generators with up-counters can take almost a minute and a half.

To save an appreciable amount of time, the program lines can be modified as follows:

```
o                                     o
o                                     o
o      1000  Gen1=700                  o
o      1010  Gen2=702                  o
o      1020  Gen3=704                  o
o      1030  OUTPUT Gen1;"UPC1";      o
o      1040  OUTPUT Gen2;"UPC1";      o
o      1050  OUTPUT Gen3;"UPC1";      o
o      1060  ASSIGN @Gen TO Gen1,Gen2,Gen3  o
o      1070  OUTPUT @Gen               o
o      1080  ASSIGN @Gen TO *          o
o      1090  END                       o
o                                     o
o                                     o
o                                     o
```

Because of the semicolons at the ends of lines 1030 to 1050 the carriage returns and line feeds which would normally be sent to the HP-IB are suppressed. An I/O path name is assigned to the three generators in line 1060 and a carriage return (and line feed) are sent to all three in line 1070. The up-counters will now be set-up in parallel by the three generators bringing the total time down to just over a third. Line 1080 closes the assigned I/O path.

Generator Control Page Programming

7-4 Generator Control Page Programming

The following example program shows how to call up the Control Page, recall the Standard Set, and then change the settings for the following parameters:

- First Address
- Last Address
- Cycle Mode
- Clock Source
- Outputs Enable
- Input Threshold

Type this program into your computer and save it to your disc. You can now run it, or better still, step through it line by line, so that you can observe the effect of the individual lines on the settings on the Control Page. In practice a proper (debugged) program would not call up the display of the various Operating Pages, as it is not necessary for parameter programming and it wastes processing time.

```
o
o
o      10  Gen = 707
o      20  OUTPUT Gen; "PAG1"
o      30  OUTPUT Gen; "RSS"
o      40  OUTPUT Gen; "FAD 0002 LAD 10"
o      50  OUTPUT Gen; "CYM2 CLK2 OUT2"
o      60  OUTPUT Gen; "THR +0.98V"
o      70  END
o
o
o
o
```

NOTE

If you have typed in any of the lines incorrectly, the generator will on running your program display a warning SRQ (service request) in line 1 of the display. Don't worry about it at this stage. Type into your computer `SPOLL(GEN)` to clear the warning.

The function of the program lines is explained below:

- 40 Sets the First and Last Address values to 0002 and 0010 respectively.
- 50 CYM2 sets Cycle Mode to Single Cycle, CLK2 sets Clock Source to External and Positive Slope, and OUT2 sets the Outputs ON. Note that **SINGLE**, the second softkey in manual operation, corresponds to the 2 in CYM2 for the selection of Cycle Mode. Similarly, PAG1 refers to the Control Page because it is the first softkey in manual front panel operation.
- 60 Sets input Threshold to +0.9 V (only two significant digits are retained).

The above program by no means uses all of the Control Page HP-IB commands. It is meant to give you a feel for the type of commands used to program Control Page Parameters. The complete list of the commands for the Control Page is given in Section 10-4. From there you can cross-reference to Section 10-2 which gives a full explanation and the correct syntax.

Generator Data Page Programming

data entry to this segment, which contains channels 1-0 to 1-3. Note also that you cannot enter data to channels that you have not called up, even if those channels are physically installed in the generator.

- 90 Load Channel Data (i.e. load data in vertical direction) into channel 2-2, starting at the Transfer Start Address of 9. The channel data to be loaded is 1 1 0 1.
- 100 Load FORmatted data (i.e. load data in horizontal direction) into data word at Transfer Start Address of 14. FOR is a formatted entry and the data entered must correspond exactly to the actual channel configuration, including Entry Yes/No and data encoding for each segment. Thus in this case the first 1 sets the Strobe channel at address 14 to 1. The following 1111 group sets the data bits of the *first* segment at address 14 to 1111 (because this segment containing channels 2-0 to 2-3 has been coded in binary in line 50 of the program). The following B sets the third segment containing channels 0-1 to 0-3 to hex B, because this segment has been coded in hex in line 50 of the program. No attempt has been made to load data into the third segment containing channels 1-0 to 1-3, because data entry to this segment has been disabled with N in line 50 of the program. If you had tried it anyway, the generator would only send a Service Request to the computer without implementing the command.

Generator Fast Binary Transfer

7-8 Generator Fast Binary Transfer

The Fast Binary Transfer, also called the "fast data reload mode", enables data to be transferred rapidly to or from an 8180A/B (and 8181A/B) and a suitable high speed I/O controller, such as an HP 9000 Series 200 or 300 Computer. The figures show how much faster this mode can be, compared to the normal ASCII transfer mode:

Normal ASCII mode:	Formatted HEX data (16 channels x 1024 bits) 10 s.
Fast Binary:	Unformatted data (16 channels x 1024 bits) 400 ms.

Before transferring data in the fast binary mode, we must transmit instructions indicating where the data that will follow is supposed to be loaded into or read from the generator's memory. This information must include the first and the last connector (e.g. BSC 0/1 would send data to or read it from connectors 0 and 1) and the address at which the first data word is to be stored or read from (e.g. BSA 100 would send the first word to address 100 or would start reading at address 100). The command BTR1 is used for channel data transfer and BTR2 for strobe data transfer.

Whether data is written to or read from the generator depends on the BASIC Language command used to perform the transfer. With OUTPUT the computer writes data to the generator, with ENTER it reads data back.

The generator memory is cyclic. This means that if more data is sent to the generator than its memory can hold, the top end of the data will be overwritten by the bottom end.

NOTE

The first connector must be an even HEX digit (0 to E) and the last connector must be an odd hex digit (1 to F). Correct examples include BSC 0/1 or BSC A/F, whereas BSC 1/2 is illegal.

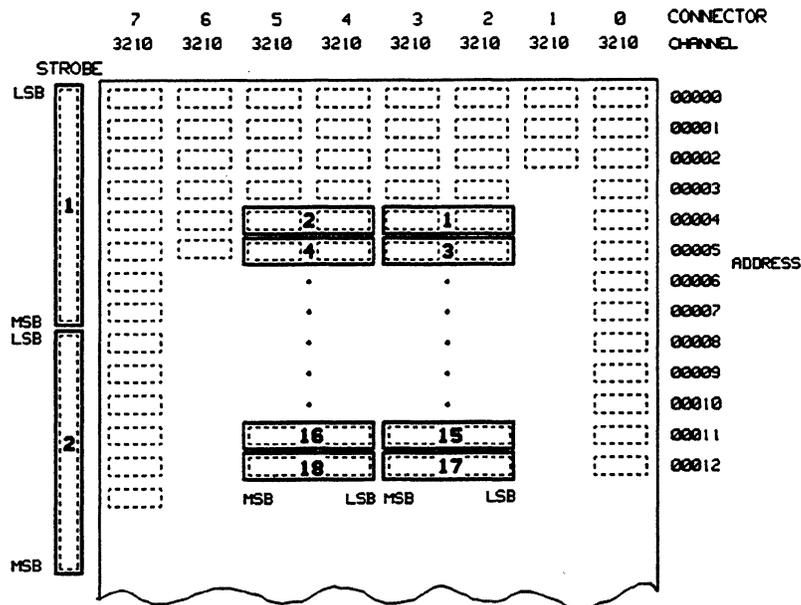


Figure 7-3. Storing Binary Data in Generator Memory

Generator Fast Binary Transfer

Figure 7-3 shows how binary data is stored in the generator memory. The memory map is for a generator containing the full complement of 16 channels and an extender fitted with 16 channels.

Let us suppose that we wish to send channel data to connectors 2, 3, 4 and 5. To address these connectors we need the command BSC 2/5. The data should start at address 00004. To do this we need the command BSA 4. Finally, we want to fill memory locations from the starting address through to address 00012. To satisfy this requirement we have to send 18 bytes of channel data. The BTR 1 command specifies the transfer of channel binary data.

We also wish to send strobe data to the same address range. To specify the transfer of strobe binary data, we need the command BTR 2. Since the strobe data segment contains only one channel and binary data is transferred in bytes (of eight bits), a single byte covers a range of eight memory addresses. This is also shown in Figure 7-1. The least significant bit of each byte of strobe data always falls on a data address that is a multiple of 8.

There is no command to define a starting address for the transfer of strobe data. The transfer must always start at address zero. Therefore we need to send enough bytes of strobe data to cover the address range of interest, even though the data sent to locations preceding this address range is not used for anything. To satisfy the requirements in our case we have to send two bytes of strobe data, of which we only need the bits at address 00004 through to address 00012.

The program to perform such a transfer is shown below. To run it you need an extender fitted with 16 channels (if your generator also contains 16 channels). If you do not have an extender you need to modify the program so that it will run:

- Delete lines 30 and 40.
- Change the first ADS in line 50 to CAS.
- Change BSC 2/5 in line 80 to BSC 2/3.
- Change line 130 to read FOR I=1 TO 9.-

```
o
o
o 10 Gen_ascii=707
o 20 Gen_binary=Gen_ascii+1
o 30 OUTPUT Gen_ascii;"CAS BY 73 72 71 70; ADS BY 63 62 61 60"
o 40 OUTPUT Gen_ascii;"ADS BY 53 52 51 50; ADS BY 43 42 41 40"
o 50 OUTPUT Gen_ascii;"ADS BY 33 32 31 30; ADS BY 23 22 21 20"
o 60 OUTPUT Gen_ascii;"ADS BY 13 12 11 10; ADS BY 03 02 01 00"
o 70 OUTPUT Gen_ascii;"PAG4 CLD"
o 80 OUTPUT Gen_ascii;"BSC 2/5"
o 90 OUTPUT Gen_ascii;"BSA 4"
o 100 OUTPUT Gen_ascii;"BTR 1"
o 110 DIM D$(18)
o 120 D$=""
o 130 FOR I=1 TO 18
o 140   D$=D$&CHR$(255)
o 150 NEXT I
o 160 OUTPUT Gen_binary USING "#,K";D$;END
o 170 OUTPUT Gen_ascii;"CLS"
o 180 OUTPUT Gen_ascii;"BTR 2"
o 190 DIM S$(2)
o 200 S$=""
o 210 FOR J=1 TO 2
o 220   S$=S$&CHR$(255)
o 230 NEXT J
o 240 OUTPUT Gen_binary USING "#,K";S$;END
o 250 OUTPUT Gen_ascii;"TAD 2"
o 260 END
o
o
o
o
```

Generator Fast Binary Transfer

The function of the program lines is explained below:

- 10 Assign generator ASCII address.
- 20 Assign generator binary address.
- 30/60 Set up eight segments of four channels each.
- 70 Call up the Data Page, clear all data.
- 80 Define the connectors for data transfer. Since each byte has 8 bits, at least 2 connectors have to be defined. Here the transfer channels are those contained in connectors 2 to 5, i.e. 16 channels.
- 90 Set address 00004 as the starting address for the data transfer.
- 100 Select the type of transfer. BTR 1 specifies the transfer of channel binary data.
- 110 Define a string D\$ of size 18 characters. We are going to send 18 bytes of channel data to the generator.
- 120 Initialize D\$ to a string of zero length. (This is good programming practice, although in this case not necessary, since D\$ has not previously been used and therefore defaults to zero length.)
- 130/150 Convert numeric values 1 to 18 into binary equivalents and store them in the string D\$. D\$ starts off with a length of zero. The first time round the loop the variable I equals 1 and this is added to the string. The string D\$ then has a length of 1 and contains a binary 11111111. Second time round the loop it has a length of two and contains 11111111 11111111, and so on. This way the complete string is built up which is later in the program sent to the generator.
- 160 Send binary data contained in D\$ to the generator HP-IB binary address, beginning at the data transfer start address (defined in line 90 of the program). Length of the data string is given in D\$ and comes from line 130.
END: Indicates to the analyzer the end of the data transfer.
- 170 Clear all strobe data.
- 180 Select the type of transfer. BTR 2 specifies the transfer of strobe binary data.
- 190 Define a string S\$ of size 2 characters. We are going to send 2 bytes of strobe data to the generator.
- 200 Initialize S\$ to a string of zero length. (This is good programming practice, although in this case not necessary, since S\$ has not previously not been used and therefore defaults to zero length.)
- 210/230 Convert numeric values 1 to 2 into binary equivalents and store them in the string S\$. S\$ starts off with a length of zero. The first time round the loop the variable J equals 1 and this is added to the string. The string S\$ then has a length of 1 and contains a binary 11111111. Second time round the loop it has a length of two and contains 11111111 11111111.
- 240 Send binary data contained in S\$ to the generator HP-IB binary address, beginning at address zero (by default). The length of the data string is given in S\$ and comes from line 210.
END: Indicates to the analyzer the end of the data transfer.
- 250 Scroll the data to Top Address of 00002.

Generator Fast Binary Transfer

- 110 Sets up data connectors for data transfer, sets the starting address for the data transfer, and then selects the type of transfer. All these commands are sent to the ASCII address.
BSC 0/1: Defines the connectors into which the data will be stored. Since each byte has 8 bits, at least 2 connectors have to be defined. Here the data is stored to channels contained in connectors 0 and 1.
BSA 0: Specifies the start address for binary transfer as 0.
BTR 1: Specifies the transfer of Binary Data (not strobe data - that is sent with the command BTR2).
- 120 Send binary data contained in Buffer\$ to the generator HP-IB binary address, beginning at the data transfer start address (defined in the previous program line). Length of the data string is given in Buffer\$ and comes from line 80.
END: Indicates to the generator the end of the data transfer.
- 130 Commands the controller to read from the generator HP-IB binary address into the Buffer2\$ string.
USING: Declares the format
-K = free field (CR/LF do not terminate the entry)
= EOI (End or Identify) and LF are item terminators
% = as for #, except that an END indication is an immediate statement terminator.
- 140 Sets up connectors 2 and 3 to receive channel data (not strobe data) starting at data transfer address 0. The line is the same as line 110, except that now the data is to be sent to generator connectors 2 and 3.
- 150 Send binary data contained in Buffer2\$ (brought back from the generator in line 130) to the generator HP-IB binary address, beginning at the data transfer start address (defined in the previous program line). Length of the data string is given in Buffer2\$ and is the same as that of Buffer\$.
END: Indicates to the generator the end of the data transfer.
- 160 Program pauses for 5 seconds, giving you time to study the changes on the Data Page of the generator. You can change this to PAUSE, in which case you must then restart the program with CONTINUE.
- 170/190 These lines have nothing to do with the binary transfer itself, but they allow you to see a part of the data transferred to the generator. The loop increases the value for the top address, thus scanning through the generator data memory.
- 200 Wait 3 seconds. You should see the current First and Last Addresses come up, which we set up in our previous example. Remember, we have not called up the Standard Set in this program.
- 210 The Top Address is set back to address 245, allowing you to see the end of the transferred data pattern (an up-counter ending with 255, at address 254).

You could also use the TRANSFER command to send the binary data to the generator. With this command, unformatted data can be transferred even faster than with the OUTPUT command used in this example. However, the use of the TRANSFER command requires extra programming overhead, and to realize its potential fully, also extra hardware.

Generator Fast Binary Transfer

Local, Remote, Local Lockout and Remote Lockout

To return the generator to local control (from remote), several possibilities exist. You can press the **LOCAL** softkey, or you can do it remotely from the computer. You can either send the BASIC command:

```
LOCAL 707,
```

where 707 is the HP-IB ASCII address, or you can send the low level GTL (Go To Local) HP-IB command:

```
SEND 7;LISTEN 7 CMD 1.
```

Power-up reset also returns the generator to local control.

To avoid the possibility of data transmissions being interrupted, which can happen if the generator is returned to local control via the front panel **LOCAL** softkey, it is recommended that local lockout be set to disable the softkey. You can do this by sending the BASIC command:

```
LOCAL LOCKOUT 7.
```

This locks out local operation of all listeners on the HP-IB select code 7 currently in remote mode. If you do not wish to perform a blanket lockout, you can do a selective one by sending the low level LLO (Local Lockout) HP-IB command:

```
SEND 7;LISTEN 7 CMD 17
```

The **LOCAL** softkey disappears and its function is disabled. The affected device does not have to be in remote mode to accept this command. The device can now be brought back into the local mode only remotely by sending one of the commands forcing the device into local, described above. Power-up reset also returns the generator to local control (and enables the **LOCAL** softkey).

To enable the **LOCAL** softkey, you have to send the BASIC command:

```
LOCAL 7.
```

This returns all devices on the HP-IB select code 7 to local mode and cancels any existing LOCAL LOCKOUTS. The generator can now be operated from the front panel, but will not accept any remote commands. To enable remote programming, send the BASIC command:

```
REMOTE 707.
```

The generator is back to its original state, that is remote programming and front panel operation are possible, and the **LOCAL** softkey is available.

For further details on the commands discussed here refer to the BASIC 4.0 Language Reference.

Summary

So far in this chapter we have learned how to set up HP-IB addresses, how to program the generator from a computer via HP-IB, and how to send data to the generator and read it back to the computer.

The task of this chapter is not to make you familiar with all of the HP-IB commands but to give you an overview of the most important programming techniques. A full listing of all the HP-IB programming commands for the generator is given in Chapter 10. Chapter 10 gives an alphabetical listing of all the generator HP-IB commands, and also groups the commands into functional sections.

Generator Fast Binary Transfer

The generator Pages not covered in this chapter are the following:

- Store Recall Page
- Miscellaneous Page
- Macro Data Page
- Remote Message Page

The number of HP-IB commands for these Pages is small and the parameters they relate to are not of primary importance to the operation of the generator. The Store Recall Page has commands dealing purely with the storing and recalling of parameter and address sets. An example of such a command is RSS, which has been used extensively in the example programs. The Miscellaneous Page is for information only and thus has only one command (to call up the Page). The Macro Data Page provides a small amount of extra memory, which is useful when operating the generator from the front panel, but becomes relatively unimportant when programming the generator from a computer (equipped with a comparatively large memory). The Remote Message Page is the eighth Page and corresponds to the blank softkey on the generator SELECT PAGE menu. This Page can be accessed only via the HP-IB.

Additional HP-IB command groups that have not been covered here are the Operation Commands group and the Universal Commands group. The commands are covered in Chapter 10, HP-IB Syntax Diagrams.

If you want to find the syntax of a command not covered here, look it up in the relevant section in Chapter 10. For example, to find out the correct syntax for the command to start the generator, turn to the Operation Commands Section.

Our next topic is the generator talker modes, with which the generator can send various information to the computer.

Generator Talker Modes

7-9 Generator Talker Modes

When addressed as a *talker*, the generator can send messages of various types to the computer. There are six different talker modes:

- TLK1 - Generator Status information
- TLK2 - Current Parameter Set (Learn Mode)
- TLK3 - Display Information
- TLK4 - Formatted Data
- TLK5 - Data Page Format
- TLK6 - String Error Identification

We will now discuss these and consider some examples.

TLK1 Output Status Information

When addressed and given the TLK1 command, the generator returns a character string which can be read into the controller. The format of the string is W,XXXXX,Y,Z, where:

- W status: 0=STOP, 1=RUN, 2=BREAK
- XXXXX actual memory address (4-bit in the case of 8180A, 5-bit in the case of 8180B when address code is decimal; can also be octal and hexadecimal, in which case the number of digits displayed alters accordingly)
- Y a hex number indicating the highest installed connector number
- Z the number of timing channel connectors installed

The simple program below performs this task. Type it into your computer and run it.

```
o                                     o
o                                     o
o      10  Gen=707                      o
o      20  OUTPUT Gen;"TLK1"            o
o      30  ENTER Gen; A$                o
o      40  PRINT A$                     o
o      50  END                          o
o                                     o
o                                     o
o                                     o
o                                     o
```

The function of the program lines is explained below:

- 10 Assign generator (ASCII) address.
- 20 Instruct the generator to function as a talker in mode 2.
- 30 Read the data string from the generator.
- 40 Display the data string on the computer screen.

Suppose for example, that you had a generator fitted with four timing channels (capable of RZ format) and 12 non-timing (NRZ) channels, and that you had programmed it to stop at address 255. Assuming the address code was set to decimal, the character string returned by the generator would then be 0,00255,3,1.

Note that after switching on the generator, the current address is undefined, as the RUN mode has not been engaged. In this case the ADDRESS field in line 2 of the generator display is empty and the string

Generator Talker Modes

The second part of the program (which would normally be executed later) reads the disc file and writes the data to another array in the computer's memory. It then sends the data to the generator, where it is immediately available for use in the current parameter set. Note that on restoring the parameters to the generator, Parameter Set 3 is overwritten with the new parameters (old information is lost).

Type up the following program and run it.

```
o
o
o 1000 Gen=707
o 1010 DIM A$(1:8)[68]
o 1020 DIM B$(1:8)[68]
o 1030 OUTPUT Gen;"PAG3 CAS BY 33 32 31 30 23 22 21 20 13 12 11 10 03 02 01 00"
o 1040 OUTPUT Gen;"TLK2"
o 1050 FOR I=1 TO 8
o 1060     ENTER Gen;A$(I)
o 1070 NEXT I
o 1080 ASSIGN @File TO "PARSET_GEN"
o 1090 OUTPUT @File;A$(*);END
o 1100 ASSIGN @File TO *
o 1110     !
o 1120     !
o 2000 WAIT 1
o 2010 OUTPUT Gen;"RSS"
o 2020 WAIT 1
o 2030     !
o 2040     !
o 3000 ASSIGN @File TO "PARSET_GEN"
o 3010 ENTER @File;B$(*)
o 3020 ASSIGN @File TO *
o 3030 FOR J=1 TO 8
o 3040     OUTPUT Gen;B$(J)
o 3050 NEXT J
o 3060 END
o
o
o
o
```

The function of the program is as follows:

- 1000 Assign generator (ASCII) address.
- 1010 Dimension a string array A\$ having 8 lines of 70 characters each, starting with line 1 and ending with line 8. This array will hold generator parameter set data to be sent to disc.
- 1020 Dimension a string array B\$ having 8 lines of 70 characters each, starting with line 1 and ending with line 8. This array will hold generator parameter set data to be retrieved from disc.
- 1030 Call up the Output Page and set up a single segment containing 16 channels.
- 1040 Instruct the generator to function as a talker in mode 2.
- 1050/1070 Read the parameter set from the generator, one line at a time and store it to a string array B\$.
- 1080 Assign an I/O path name to the disc file PARSET_GEN.
- 1090 Output the contents of array A\$ to the above defined I/O path.
END: specifies end of data transfer.

Generator Talker Modes

- 80 **HEX:** The address field is coded in hex.
 SNE: Strobe Entry N - not allowed. (SYE would mean Strobe Entry Yes - allowed.)
- 90 Calls up the Data Page. Instructs the generator to function as a talker in mode 5.
- 100/130 Read the format data one string at a time and display it on the computer screen. The upper bound in the FOR/NEXT loop is the number of data segments +1. We have set up six data segments, thus we shall need to output seven strings to the screen. In other words, we always have to read in one more string than there are data segments.
- Each string, except the last one, gives the full details of a data segment. Note that even the strings of those segments not shown (or not completely shown) on the generator screen and causing the warning `Display incomplete` are sent to the computer and displayed there. We could do that for instance by adding one more channel to the sixth segment.
- The last string gives details of the address code (in this case HEX, but can also be DEC or OCT), and Strobe Entry (in this case entry is not allowed - N, but entry can also be allowed - Y).

TLK 6 Output String Error Identification

TLK 6 mode instruct the generator to transmit an error code, in case an illegal message string was sent to the generator. The value of the number returned following a TKL 6 instruction identifies the position of the erroneous character in the message string.

In the example below, the number returned will be 19. This means that the 19th character was illegal; specifically the 6 indicating "Cycle Mode 6" is an error because that mode does not exist.

```
o          o
o          o
o          10  GEN=707          o
o          20  OUTPUT GEN;"FAD 10 LAD 100 CYM6"  o
o          30  OUTPUT GEN;"TLK6"                o
o          40  ENTER GEN;I                      o
o          50  PRINT I                          o
o          60  END                            o
o          o
o          o
o          o
```

The function of the program lines is explained below:

- 20 Create an error by sending a non-existent command (CYM6).
- 30 Instruct the generator to function as a talker in mode 6.
- 40 Read the number that has been output by the generator.
- 50 Display the number on the computer screen.

You can also dimension a string `B$` of 7 characters at the beginning of the program and then read the complete string from the generator. The result printed out would in this case then be `SRQ 019`.

This mode would normally be used when debugging a program to control the generator. The simple program above has only one parameter programming line, so it is easy to see where the error has occurred. In a larger program, talker mode 6 alone would not help much to identify the error.

Generator Talker Modes

Therefore it would be part of an interrupt service routine, called by the generator Service Request. (The Service Request is covered in the next section.)

Note that the error indication remains inside the generator even if the error is no longer present, until it is replaced by another error indication. If you perform TLK 6 immediately after switch-on, the mode returns a value of zero.

Generator Service Request Messages - Status Byte

7-10 Generator Service Request Messages - Status Byte

When the generator detects an error condition, it responds by requesting service. Conditions causing service requests include syntax errors, incorrectly formatted statements, addressing hardware which is not installed, and operator action via the SRQ softkey. Any of these will result in the SRQ line of the HP-IB being set true, and SRQ will be displayed at the top of the generator's display area in line 1.

The generator can then be "serial polled". For HP 9000 Series 200 and 300 computers, the command is SPOLL (HP-IB address). In response the generator outputs an 8 bit Status Byte onto the HP-IB. The byte can then be decoded and interpreted by the computer.

The Status Byte is encoded as follows. The upper nibble is made up of the four most significant bits DIO 5 to DIO 8 (Data I/O lines when referring to HP-IB). These bits are encoded singly and each represents an error condition or a warning. The bits come up independently of each other, therefore several of them can come up at the same time. The lower nibble is made up of the four least significant bits DIO 1 to DIO 4. These bits form a 4-bit code, giving 16 different error messages. The complete list of error and warning messages is given in Table 7-1.

Table 7-1. Status Byte Messages

STATUS BYTE	ERROR OR WARNING MESSAGE
Upper Nibble	
DIO 8	Status is BREAK (updating every 50 ms or at UPD-Update Screen)
DIO 7	Request Service
DIO 6	Hardware or Compatibility Error
DIO 5	Status is RUN (updating every 50 ms or at UPD - Update Screen)
Lower Nibble	
DIOs 4 3 2 1	
(0) 0 0 0 0	User Service Request from SRQ softkey
(1) 0 0 0 1	Syntax Error
(2) 0 0 1 0	Unexpected Unit
(3) 0 0 1 1	Statement not complete (missed number or unit)
(4) 0 1 0 0	String not terminated
(5) 0 1 0 1	Range overflow
(6) 0 1 1 0	Illegal Sign
(7) 0 1 1 1	Illegal Unit
(8) 1 0 0 0	Hardware not installed
(9) 1 0 0 1	Illegal Channel Number
(10) 1 0 1 0	Entry not allowed
(11) 1 0 1 1	Formatter Error
(12) 1 1 0 0	Parameter Set Destroyed
(13) 1 1 0 1	Timing Incompatibility Error
(14) 1 1 1 0	Level Incompatibility Error
(15) 1 1 1 1	GET either not at all, or not immediately executed *

(*) GET is an HP-IB programming command. For details see Chapter 10, HP-IB Syntax Diagrams.

Additional details concerning the Status Byte are as follows:

- The generator provides a single level of error reporting. A serial poll of the generator returns the *last* error detected. The previous errors, if any, are lost. It is therefore up to the programmer to structure his software in such a way as not to lose any of the error messages. This may for instance take the form of a subroutine call to a Status Byte interpreting code after each generator programming line or after a group of programming lines. Another approach may be an interrupt service routine to catch the errors as they occur.

Generator Service Request Messages - Status Byte

- A timing error or a swing error is flagged by the *Hardware or Compatibility Error* bit (DIO 6) in addition to the *Timing Incompatibility Error* code (1101) or the *Level Incompatibility Error* code (1110). As long as one of these errors is present, DIO 6 remains set even if another error subsequently occurs, resulting in a different error code being returned.

Note however that, if you use a service routine which executes immediately in response to an interrupt on the SRQ control line on the HP-IB, you need to include a small delay (of say 0.1 s) before you serial poll the generator. Otherwise it is possible that the SPOLL will execute before DIO 6 gets set and the Hardware or Compatibility Error message will be lost.

- The Status Byte buffer is not "emptied" when read by the serial poll. In absence of a change in status, the old status is returned in response to a serial poll. A change in status is signaled by the *Request Service* bit (DIO 7). When this bit is set the returned error is new.
- You can disable the SRQ interrupt and the Service Request bit (DIO 7) relating to the Timing Incompatibility Error (value 13 decimal) and the Level Incompatibility Error (value 14 decimal) by sending the ISR 2 command before you send any timing or level commands. The Hardware or Compatibility Error bit (DIO 6) is not affected. To restore error reporting on these parameters, send the ISR 1 command.

The following program can be used to decode the individual messages from the Status Byte. Some of the program's features have not been used (certain lines have been deactivated - turned into comments) so as not to make the error printout too cluttered. However, you can activate them to see their effect on the error message printout.

The program uses an interrupt service routine which is executed on receipt of an interrupt sent by the generator whenever it detects a problem of some sort. The program masks off all the bits of the Interrupt Enable Mask Register except bit 1, the SRQ bit. When a programming error is detected by the generator (or any other addressed device on the bus), the HP-IB SRQ control line is activated until an SPOLL is sent to the relevant device. The device then replies by sending the Status Byte onto the bus.

The program consists of three main parts. The first part is the parameter programming part, where various HP-IB commands are sent to the generator. The second part is the interrupt service routine, which decodes the Status Byte sent by the generator. The third part is the data for the service routine, which contains the error and warning messages.

If there are more devices on the HP-IB, which is normally the case in a test setup, then the program must poll each device on the bus to find out which one has requested service. It is the device that has Bit 6 (DIO 7) of the Status Byte set. Only then can the correct Status Byte be read and decoded. The program below polls only the generator, as there are no other instruments in our setup.

Generator Service Request Messages - Status Byte

The function of the program lines is explained below:

- 10 Read error messages stored under DATA in lines 500 to 650.
- 20 Assign generator (ASCII) address.
- 30 Trap interrupt at HP-IB interface select code 7 (that means an interrupt from any device connected to that HP-IB, including the generator) and execute subroutine Srq.
- 40 Enable the SRQ Bit in the Interrupt Enable Mask Register of HP-IB interface with select code 7 as the only source of interrupt to the computer.
- 80/150 Program the generator.
- 170 Stop the program. The program is now effectively at its end.
- 210 Start of interrupt service routine Srq. The routine reads the status byte and decodes it into individual warning and status messages.
- 220 Introduce a wait statement of 100ms to give the generator enough time to set the relevant Status Byte bits (according to error).
- 230 Perform serial poll on the generator and read the status byte into variable C.
- 240 Print the Status Byte encoded in binary (prints also eight leading zeros). This line is not needed for printing out error messages and is therefore not activated.
- 260/280 Mask off all bits except for DIO 8. If this bit is true, print out the message.
- 300/320 Mask off all bits except for DIO 7. If this bit is true, print out the message. These lines cause the "Request Service" message to come up every time any of the other messages are output. Therefore the lines have been disabled.
- 340/360 Mask off all bits except for DIO 6. If this bit is true, print out the message.
- 380/400 Mask off all bits except for DIO 5. If this bit is true, print out the message.
- 440 Dimension a string array of 16 lines, each 60 characters long (the length of the longest warning message). The array must start at 0 and finish at 15, and the messages listed in lines 500 to 650 must remain in the order shown, so that the correct message is output in response to an interrupt.
- 450 Mask off all bits of the status byte except for the low nibble (the least significant four bits) by performing a binary AND of the status byte with 00000000 00001111 (variable C contains 16 bit data). Index the string array by the resulting value and print out the accessed string - the warning message.
- 460 Attract attention to each warning message with a beep.
- 470 Enable interrupts so that the service routine can be executed next time the generator issues an interrupt.
- 480 Return to the main program (lines above the Interrupt service routine).
- 500/650 Sixteen messages which can result from the least significant four bits of the status byte.

As the program stands, the interrupt service routine will not be executed because there are no errors in the parameter programming part. All that will happen is that the parameters contained in the program

Generator Service Request Messages - Status Byte

will be downloaded to the generator and the program will stop. You can activate the service routine by introducing errors into the parameter programming part.

Experiment on your own, or try out the following changes and additions to obtain a selection of error and warning messages on the computer screen.

```
80  OUTPUT Gen;"PAG4 CYM6"  
90  OUTPUT Gen;"HES FAD 0 LAD F TAD 0"  
100 OUTPUT Gen;"CAS HY 33 32 31 30 23 22 21 20 1 12 11 10 03 02 0100"  
110 OUTPUT Gen;"ADS DY 33 32 31 30 23 22 21 20;ADS DY"  
130 OUTPUT Gen;"ADS BY 33 32 31 30 23 22 21 20 13 12 11 10 03 02 01 50"  
140 OUTPUT Gen;"ADS BY 33 32 31 30 23 22 21 24"  
151 OUTPUT Gen;"LOLA 1MS"  
152 OUTPUT Gen;"PAG2 FRQ 5MHZ WID 2C 200NS"  
153 OUTPUT Gen;"HILA 0.2V LOLA -0.25V"
```

The following error messages appear as a result of the errors in the above program lines.

```
WARNING: Range Overflow  
WARNING: Syntax Error  
WARNING: Statement not complete (missing number or unit)  
WARNING: Hardware not installed  
WARNING: Illegal Channel Number  
WARNING: Illegal Unit  
WARNING: Hardware or Compatibility Error  
WARNING: Timing Incompatibility Error  
WARNING: Level Incompatibility Error (Swing Error)
```

The last two messages can be suppressed by including the following line in the program:

```
75  OUTPUT Gen;"ISR 2"
```

Restore the error reporting by sending the ISR 1 command.

If you are writing a large test program, it is reasonable to assume that there will be a few bugs in it. An interrupt routine such as the one in this program will trap the bugs, but will not help much in locating them quickly. It is therefore of benefit to include a serial poll command with the Status Byte interpreting code and a position pointer after each parameter programming section until the test program has been debugged.

Note that the generator issues a service request when it detects an erroneous HP-IB programming command on a line. When there are more than one of these per programming line, the generator does not flag the second and subsequent errors. However, as long as there is at least one erroneous command on a program line, the generator flags up an error, and you can then check the line for correctness.

Chapter 8

Analyzer Programming

8-1 Introduction

In this chapter we are going to discuss analyzer remote programming using the HP-IB (Hewlett-Packard Interface Bus). For a more detailed overview of the HP-IB refer to Section 7-1.

The analyzer is programmed by means of HP-IB commands, sent to it from the controller. In this way every operating parameter can be accessed. Analyzer programming is therefore independent of the controller or the programming language used. Programming the analyzer is very similar to programming the generator. Thus, if you have read the previous chapter, Generator Programming, then the concepts of analyzer programming will be clear to you.

The analyzer is supported by the HP 9000 Series 200 and 300 Family of Technical Computers. HP BASIC is used as the programming language. You can use HP BASIC and instrument HP-IB commands to write your own test routines and programs.

If you do not wish to write your own test programs, you can turn to the HP 81810S System Software, which supports systems ranging from a single generator and analyzer, right up to large installations of multiple generators and analyzers. The System Software allows interactive or "batch" testing of devices and can be used by people with little programming experience. It is written in HP BASIC and is therefore an open system. For further information refer to the System Software User Manual.

HP-IB Cable Connection

The available HP-IB cables are the following:

- HP 10833A - 1.0 m (3.3 ft) cable
- HP 10833B - 2.0 m (6.6 ft) cable
- HP 10833C - 4.0 m (13.2 ft) cable
- HP 10833D - 0.5 m (1.6 ft) cable

To connect the analyzer to the computer, simply plug either end of one of the above cables into the HP-IB connector of the computer and the analyzer and tighten the retaining screws using your fingers. At the computer end you will probably already have a connection to the disc. So plug the new cable into the one already present.

The devices making up your system (generators, analyzers, computer, disc and so on) can be connected together in any configuration (star, linear or both) as long as the following rules are observed:

- The total number of devices connected to one computer HP-IB interface is not greater than 15.
- The total length of all cables used is not greater than two meters times the number of devices connected together, up to a maximum of 20 meters.

If your individual cable lengths exceed 4 meters, refer to operating guidelines in the IEEE Standard 488-1978. Do not stack more than three cable connector blocks together on any HP-IB connector. The resultant leverage can exert excessive force on the mounting panels. Make sure that all connectors are fully seated and that the lock screws are firmly finger tightened. *Do not use a screwdriver to tighten the lock screws.* You may use a screwdriver to release the screws.

8-2 Analyzer HP-IB Addresses

The analyzer is connected to a controlling computer by means of the HP-IB. The analyzer will not be the only piece of equipment connected. There will most probably be a generator and a disc drive, and there may also be a testhead, other generators or analyzers, a printer and so on. Each device must therefore have its own address, which the computer can select in order to communicate with that device.

Similarly to the generator, the analyzer has two HP-IB addresses, and 2 modes of remote operation based on the two addresses.

HP-IB ASCII Address

The ASCII address is used by the computer to communicate with the analyzer in the ASCII mode in which data, and parameter and mode settings are transferred over the bus as a series of ASCII bytes. The ASCII message is then interpreted by the instrument and executed.

The HP-IB ASCII address can be set directly on the HP-IB address switches on the back panel of the analyzer. If you wish to find out the current setting of this address, you can either look at the address switches (shown in Figure 8-1), or read it on the Miscellaneous Page of the instrument, which is shown in Figure 8-2. To access the Miscellaneous Page, switch on the instrument and press the PAGES key followed by the **MISCELLANEOUS** softkey.

There are five binary HP-IB address switches, giving an address range of 00000 to 11101 binary, or 0 to 29 decimal. Settings of 11110 and 11111 binary or 30 and 31 decimal are illegal. The switches are marked "1" and "0". To change the HP-IB ASCII address, slide the switches to the appropriate position using a pointed object, such as a small screwdriver.

NOTE

You can change the setting of the address switches with power on. Any changes will take effect within two seconds, unless the analyzer is currently communicating via the HP-IB, in which case they will take effect when the HP-IB is no longer busy. If for any reason (bus contention for instance) the HP-IB is blocking an address change, press the RESET key on the computer keyboard to release the bus.

NOTE

The address immediately following an analyzer ASCII address may not be assigned to any device on the bus.

NOTE

When changing the switch setting or connecting a number of instruments to one computer, make sure that every device on the bus has a unique address. This includes also the address of the HP-IB interface card of the active controller (the computer), which has a factory setting of 21. Therefore avoid setting the ASCII address switches to either 21 or 20 (see HP-IB Binary Address later), otherwise bus contention problems will occur.

Analyzer HP-IB Addresses

If you suspect that the address of the HP-IB interface card has been changed, you can find out the new address with the command:

```
STATUS SC,3;N_v
PRINT N_v
```

where SC is the HP-IB interface select code, currently set to 7, and 3 is the HP-IB Status Register 3 which contains the HP-IB address. N_v is any valid name for a numeric variable.

For more details on the command and the Status Register refer to the BASIC 4.0 Language Reference. Select codes are covered in the next section.

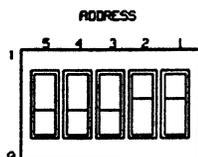


Figure 8-1. Analyzer HP-IB Address Switches

8182B Clock	Status Stored Words	IDLE 00000
----- MISCELLANEOUS -----		
Autoexit		OFF
Cursor & Top Addr		LINKED
Display Brightness		█
----- FOR INFORMATION ONLY -----		
HP-IB ASCII Address		03
HP-IB Binary Address		04
Total Channels		32
Installed Connectors		01234567
Select Further -----		
Autoexit	Cur. & Top Addr	Brightness
Store	Recall	

Figure 8-2. Miscellaneous Page

HP-IB Binary Address

The binary address is used to transfer blocks of binary data at high speed between the computer and the analyzer. This is covered later in Section 8-7, Analyzer Fast Binary Transfer.

There are no switches on the analyzer to set the binary address. Whatever the setting of the ASCII address, the binary address is always one higher than the ASCII address. This is why you cannot allocate the address immediately following the instrument's ASCII address to any other device on the bus. The binary address is also displayed on the Miscellaneous Page.

8-3 Concept of HP-IB Programming - Analyzer

The instrument is programmed by sending the appropriate listen address plus an HP-IB program command which might be followed by numerical values and units. The technique is identical to that used by the generator. If you are not familiar with it, read Section 7-3 of this manual first.

Select Code

The Select Code considerations are the same for the analyzer as for the generator. They are explained in Section 7-3 of this manual.

Since the analyzer is connected to the same bus as the generator, its HP-IB address prefix (the Select Code) will be the same as for the generator. In our case it will therefore be 7. Since the analyzer has the HP-IB ASCII address set to 03, then in order to recall the analyzer Standard Set, for instance, we need to type into the computer the following:

```
OUTPUT 703; "RSS" 
```

Exercise - Setting Analyzer Operating Mode

Set the Operating Mode of the analyzer to Trigger Start Compare.

The HP-IB programming command for the Operating Mode is OPR and it has to be followed by a *number*, in this case 3. Type in the following:

```
OUTPUT 703; "OPR 3" 
```

Note that you have just programmed a parameter interactively, without actually writing a program. Note also that it is not necessary to call up a specific page prior to programming a parameter. Every parameter is directly accessible.

As was the case with the generator, the normal operating softkeys have disappeared and the following softkeys have appeared in their place:



This happens whenever an HP-IB command has been sent to the instrument, and means that the instrument is now in the remote mode. The instrument does not respond to any front panel controls. To bring it back to the local mode, press the softkey . The operating softkeys return and you can operate the instrument from the front panel.

The softkey sends a Service Request to the computer. We shall cover the Service Request later in this chapter.

You can now check by pressing the softkey and selecting the Control Page, that the Operating Mode has been set as programmed.

NOTE

Similarly to the generator, the analyzer accepts a new programming line only after it has settled at the values of the previous one. Therefore, the programmer need not worry about settling times of the instrument.

We will discuss more analyzer programming commands as we go along. A complete listing of the HP-IB commands together with the syntax for each is given in Chapter 10, HP-IB Syntax Diagrams.

HP-IB Command Syntax

The syntax is the same as for the generator commands. It is explained in Section 7-3 of this manual.

HP-IB Command Delimiters

The delimiters used are the same as for the generator. This topic is discussed in Section 7-3 of this manual.

Synchronizing Character

The function of the synchronizing character is the same as in the generator. The details are available in Section 7-3 of this manual. There is however one important difference. Whereas the generator synchronizing character is fixed, the analyzer allows its synchronizing character to be programmed. The range of characters available is ASCII 0 to 255. Default setting is ASCII 13 - Carriage Return. You can program a new character (for instance a "!") with the following program line:

```
Output Ana;"SYN 33"
```

33 is the decimal equivalent of ASCII "!". Note that the default character is forced at power-up and at an HP-IB address switch change.

Analyzer Control Page Programming

8-4 Analyzer Control Page Programming

The following example program shows how to call up the Control Page, recall the Standard Set, and then change the settings for the following parameters:

- Clock Delay
- Clock Width
- Clock Threshold
- Trigger Arm Slope
- Trigger Arm Threshold
- Trigger Word
- Trigger Qualifier Level
- Trigger Qualifier Impedance
- Trigger Count
- Trigger Delay

Type this program into your computer and save it to your disc. You can now run it, or better still, step through it line by line, so that you can observe the effect of the individual lines on the settings on the Control Page. In practice a proper (debugged) program would not call up the display of the various Operating Pages, as it is not necessary for parameter programming and it wastes processing time.

```
o
o
o 10 Ana=703
o 20 OUTPUT Ana;"PAG1"
o 30 OUTPUT Ana;"RSS"
o 40 OUTPUT Ana;"CKD 10NS"
o 50 OUTPUT Ana;"CKW 1US"
o 60 OUTPUT Ana;"CKT 2.05V"
o 70 OUTPUT Ana;"TAS2"
o 80 OUTPUT Ana;"TAT 1V"
o 90 OUTPUT Ana;"TWD 1111 0000 XXXX 1010 0011 1001"
o 100 OUTPUT Ana;"TQL3 TQ12 TRC4 TRD16"
o 110 END
o
o
o
o
```

NOTE

If you have typed in any of the lines incorrectly, the analyzer will on running your program display a warning SRQ (service request) in line 1 of the display. Type into your computer SPOLL (HP-IB address) **ENTER** to clear the warning.

The function of the program lines is explained below:

- 10 This declares the variable Ana=703, to be used throughout the program in place of the literal 703. (703 can always be used, however.)
- 20 Puts the analyzer in the remote listen mode and instructs it to display the Control Page.
- 30 Recalls the Standard Parameter Set.

Analyzer Control Page Programming

- 40 Sets Clock Delay to 10ns.
- 50 Sets Clock Width to 1 μ s. Notice that you cannot see a Clock Width entry on the Control Page. This is because the analyzer has entered the Trigger Start Analysis operating mode on recalling the Standard Set. The Clock Width command is nevertheless executed and the value is entered in the analyzer's memory. You can check this by calling up the Trigger Start Compare mode, where the Clock Width parameter is used.
- 60 Sets Clock Threshold to 2.05V. Numbers containing more than two decimal places are accepted by the generator, but are ignored.
- 70 Sets Trigger Arm Slope to negative slope.
- 80 Sets Trigger Arm Threshold to 1V.
- 90 Sets the Trigger Word to 1111 0000 XXXX 1010 0011 1001 1XX0 X01X. The Trigger Word must be of the same format as the current channel configuration. This example assumes that your analyzer contains the full complement of 32 channels. As we have recalled the Standard Set in line 30 and have since not changed the channel configuration, then the Trigger Word configuration fits. It is important to remember that the Trigger Word format and range must always match the current channel configuration.

If your analyzer is fitted with less channels, you need to reduce the range of the Trigger Word to match. If you forget this, the analyzer will send out a service request and will fail to execute the command.

- 100 TQL3: Trigger Qualifier Level set to Don't care.
- TQI2: Trigger Qualifier Impedance set to 100 kOhms
- TRC4: Trigger Count set to 04. (The Trigger Word must occur four times before the analyzer triggers.)
- TRD16: Trigger Delay set to 16. (After triggering, the analyzer goes active when 16 clock pulses have been counted.)

The above program by no means uses all of the Control Page HP-IB commands. It is meant to give you a feel for the type of commands used to program Control Page Parameters. The complete list of the commands for the Control Page is given in Section 10-5. From there you can cross-reference to Section 10-3 which gives a full explanation and the correct syntax.

Analyzer Input Page Programming

- 70 LBL CCCC DDDD BBBB ABBB: assigns threshold labels to *individual* channels. The configuration of the labels must match the channel configuration with respect to segment size. The number of label "segments" must be equal to or smaller than the number of channel segments.
- 80 POL I-- NIII II-N N-I: sets the polarity of the analyzer inputs. N sets normal polarity, I sets inverse polarity. Dash skips to the next channel without changing the polarity. The resulting polarity is therefore determined by the previous setting. The configuration of the polarity identifiers must match the channel configuration with respect to segment size. The number of polarity identifier "segments" must equal to or be smaller than the number of channel segments.

Analyzer Expected Data Page Programming

- 50/70 Transfer five words of Expected Data *with word mask* to the Expected Data Memory of the analyzer. This is an ASCII data transfer. The transferred data must correspond exactly to the current channel format of the analyzer.

In effect, it does not matter what the transferred data is (as long as the condition in the previous sentence is met), since the word mask is set (an X appears in the MASK column of data at addresses 00000 to 00004).

The data transfer can also be made without the mask, using the DAT command. In that case the mask is determined by the previous setting, which in this case may not give the results we require, as we do not know what the previous setting was.

- 80 Set Transfer Start Address for data transfer to 00005.

- 90/110 Transfer 9 words of Expected Data *with word mask* to the Expected Data Memory of the analyzer. This is an ASCII data transfer. Here the word mask is not set, thus a period (.) appears in the MASK column of data at addresses 00000 to 00004. The transferred data must again correspond exactly to the current channel format of the analyzer.

The data itself is identical to that sent to the previous five addresses. It contains bit masks on all channels in segments 5 and 6. The Expected Data in these memory locations will also be masked.

- 120 Call up the State List Page and select analyzer internal clock. In absence of a generator clock we could not otherwise clock in any data under program control.

- 130 Start the analyzer. The analyzer now starts to clock in data at the internal clock frequency of 1 MHz. This frequency is the default setting brought in by recalling the Standard Set in line 20 (even though RCL4 actually selects external clock). The Standard Set also selects a maximum Stop Delay of 16383 (1023 for the A version). The generator therefore runs to that address and stops, sending a service request to the computer. The Standard Set also sets the Display Errors parameter to ON, which will enable us to see any errors on the State List Page.

Notice that the State List Page displays all zeros, some in inverse video and some in normal video. This is indeed correct because the analyzer has sampled zero data on all its input channels. All data displayed in normal video is analyzed as correct, and that in inverse video is analyzed as erroneous. The Received Data at addresses 00000 to 00004 is displayed as correct, because we have enabled the word mask at these addresses.

The following 9 words at addresses 00005 to 00013 show errors on all channels in segments 2 and 4 (counted from left to right). This is because we have set the data in those memory locations to '1'. Segments 5 and 6 show no errors due to the bit masks on these memory locations.

Thereafter, all memory locations right up to the last word display errors, since the Expected Data at these locations has been set to '1' in line 30 of the program.

- 140 Read the Status Byte from the analyzer. Similarly to the generator, the analyzer also outputs a Status Byte on the HP-IB when serial polled, although this is rather differently encoded. This subject will be covered in detail in Section 8-10. For the moment it is important to know that, when no errors are registered by the analyzer the Status Byte gets cleared to zero by a serial poll, and when the analyzer stops (goes in the IDLE state) it notifies this by sending a service request and sets bits 6 (Service Request Bit, value 64) and 4 (Ready Bit - Stop Routine Executed, value 16) to '1'.

Analyzer Expected Data Page Programming

Notice however that the number returned by the analyzer is zero. This is because the SPOLL command came before the analyzer had stopped.

- 150 The delay introduced in this line enables the analyzer to run to the end of its memory range and stop, before the next SPOLL is sent to it.
- 160 This time the analyzer is already in the IDLE state and replies to the serial poll with 80 decimal (bits 6 and 4 are set).
- 170 Dump Received Data from Received Data Memory to the Expected Data (reference) Memory. Notice that the inverse video fields disappear. The content of the Expected Data Memory and the Received Data Memory is now the same and the error indication is no longer there.
- 180 Return back to the Expected Data Page.
- 190 Set Channel Data on segments 1 and 3. A one sets the data. Zeros cannot be used. Dash skips to the next channel without changing the channel content. The resulting content is therefore determined by the previous setting. The configuration of the channel setting identifiers must match the channel configuration with respect to segment size. The number of channel setting identifier "segments" must equal to or be smaller than the number of channel segments.
- 200 Set Channel Mask on segment 4 (counted from left to right). A one sets the mask. Zeros cannot be used. Dash skips to the next channel without changing the channel mask. The resulting channel mask is therefore determined by the previous setting. The configuration of the channel mask setting identifiers must match the channel configuration with respect to segment size. The number of channel mask setting identifier "segments" must equal to or be smaller than the number of channel segments.

Note that if you step through the program, the computer displays a Status Byte of 80 decimal followed by 0 decimal. The analyzer reaches the IDLE state before you can manually execute line 60 of the program. In line 80 the Status Byte is already cleared to zero.

Analyzer Fast Binary Transfer

8-7 Analyzer Fast Binary Transfer

The analyzer also features Fast Binary Transfer. It functions in a very similar manner to that of the generator and enables data to be transferred rapidly to or from an 8182A/B and a suitable high speed I/O controller, such as an HP 9000 Series 200 or 300 Computer. As with the generator, the binary transfer of data is very much faster than normal ASCII transfer.

To set up a binary data transfer between the computer and the analyzer is a little more complex than it was with the generator as there are more types of transfer the analyzer supports. There are two binary listen commands and three binary talk commands for initiating binary transfers. The commands and their functions are as follows:

BLI1 - transfers expected data from the computer to the analyzer.

BLI2 - transfers bit mask data from the computer to the analyzer.

BTK1 - transfers received data from the analyzer to the computer

BTK2 - transfers expected data from the analyzer to the computer

BTK3 - transfers bit mask data from the analyzer to the computer

In addition to these commands supported by both the A- and B-version, the 8182B analyzer also supports an extra binary listener transfer and two more binary talker transfers:

BLI3 - transfers word mask data from the computer to the analyzer.

BTK4 - transfers word mask data from the analyzer to the computer

BTK5 - transfers error map data from the analyzer to the computer

As well as providing the analyzer with one of the above commands, we must also transmit instructions indicating where the data that will follow is supposed to be loaded into or read from the analyzer's memory. This information must include the first and the last connector (e.g. BSC 01 sends data to or reads it from connectors 0 and 1) and the address at which the first data word is to be stored or read from (e.g. BSA 100 sends the first word to or reads it from address 100).

The analyzer memory is cyclic. This means that if more data is sent to the analyzer than its memory can hold, the top end of the data will be overwritten by the bottom end.

NOTE

The first connector must be an even HEX digit (0 to 6) and the last connector must be an odd hex digit (1 to 7). Correct examples include BSC 01 or BSC 67, whereas BSC 12 is illegal.

Figure 8-3 shows how binary data is stored in the analyzer Expected Data memory. The memory map is for an analyzer containing the full complement of 32 channels.

Let us suppose that we wish to transfer bit mask data to connectors 2, 3, 4 and 5. To address these connectors we need the command BSC 25. The data should start at address 00004. To set the Binary Start Address we need the command BSA 4. Finally, we want to fill memory locations from the starting address through to address 00012. To satisfy this requirement we have to send 18 bytes of bit mask data. The BLI 2 command specifies the transfer of bit mask data from the computer to the analyzer. The program to perform such a transfer is shown below.

Analyzer Fast Binary Transfer

start connector is 2 and the stop connector is 5. We are therefore making a transfer to 16 channels.

- 50 Set address 00004 as the starting address for the data transfer.
- 60 Select the type of transfer. BLI 2 specifies the transfer of bit mask data from the computer to the analyzer.
- 70 Define a string S\$ of size 18 characters. We are going to send 18 bytes of bit mask data to the analyzer.
- 80 Initialize S\$ to a string of zero length. (This is good programming practice, although in this case not necessary, since S\$ has previously not been used and therefore defaults to zero length.)
- 90/110 Convert numeric values 1 to 18 into binary equivalents and store them in the string S\$. S\$ starts off with a length of zero. The first time round the loop the variable I equals 1 and this is added to the string. The string Buffer\$ then has a length of 1 and contains a binary 11111111. Second time round the loop it has a length of two and contains 11111111 11111111, and so on. This way the complete string is built up which is later in the program sent to the analyzer.
- 120 Send binary data contained in S\$ to the analyzer HP-IB binary address, beginning at the data transfer start address (defined in line 50 of the program). Length of the data string is given in S\$ and comes from line 90.
- END: Indicates to the analyzer the end of the data transfer.

Note that a service request will be forced if you attempt to program a start connector of a number higher than the stop connector, or a stop connector of a number higher than highest installed connector.

The actual transfer address is reset to BSA (Binary Start Address) whenever any of the following conditions occur:

- Last data bit of the last memory address in the analyzer has been reached.
- HP-IB address (Listen, Talk, Unlisten and so on) sent by controller changed - a different device on the HP-IB is addressed.
- Serial Poll complete.
- BSA (Binary Start Address) or BSC (Binary Start Connector) changed.
- EOI (End or Identify) received by analyzer.
- BLI (Binary Listener) or BTK (Binary Talker) changed.

If you are in the process of transferring a binary data string between the analyzer and the computer, you have to avoid causing any of the above conditions to occur. Otherwise the transfer address (in the process of incrementing) will be reset to the programmed Binary Start Address.

Analyzer Fast Binary Transfer

With the second program we execute a fast binary transfer from the computer to the analyzer, then read it back into the computer. Finally, we send the data out to the analyzer again, but to different memory locations (different connectors) in the analyzer.

```
o
o
o 10  DIM Buffera$(11)
o 20  DIM Bufferb$(11)
o 30  Ana_ascii=703
o 40  Ana_binary=Ana_ascii+1
o 50  L=SPOLL(Ana_ascii)
o 60  L=SPOLL(Ana_ascii)
o 70  OUTPUT Ana_ascii;"RCL4 PAG3 CLD"
o 80  OUTPUT Ana_ascii;"CAS B 33 32 31 30 23 22 21 20"
o 90  OUTPUT Ana_ascii;"ADS B 13 12 11 10 03 02 01 00"
o 100 OUTPUT Ana_ascii;"BSC 01 BSA 0 BLI1"
o 110 Buffera$=""
o 120 FOR N=255 TO 245 STEP -1
o 130   Buffera$=Buffera$&CHR$(N)
o 140 NEXT N
o 150 OUTPUT Ana_binary;Buffera$;END
o 160 OUTPUT Ana_ascii;"BTK2"
o 170 ENTER Ana_binary USING "-K,%,#";Bufferb$
o 180 OUTPUT Ana_ascii;"BSC 23 BSA 3 BLI1"
o 190 OUTPUT Ana_binary USING "K,#";Bufferb$;END
o 200 END
o
o
o
o
```

The function of the program lines is explained below:

- 10 Define a string Buffera\$ of size 255 characters.
- 20 Define a string Bufferb\$ of size 255 characters.
- 30 Assign analyzer ASCII address.
- 40 Assign analyzer binary address. You can assign the binary address directly, but the way we have done it here is more convenient as it is always tied to the ASCII address if that should change.
- 50 Serial poll the analyzer. It is always a good idea to do this before any HP-IB commands are sent to the analyzer in case the Status Register contains any status data.
- 60 Serial poll the analyzer. The analyzer has two levels of error reporting, thus the Status Byte has to be read twice. More about this in Section 8-9, Service Request Messages - Status Byte.
- 70 Recall Standard Set, call up the Expected Data Page, clear all data, set Top Address to 0.
- 80 CAS: Clear All Segments and set up a new eight channel segment containing channels 2-0 to 3-3, coded in binary (B).
- 90 ADS: Add Data Segment containing eight channels 0-0 to 1-3, coded in binary (B).
- 100 Set up data connectors for data transfer, then set the starting address for the data transfer, then select the type of transfer. All these commands are sent to the ASCII address.
 - BSC 01: Binary Select Connector 0 and 1. We wish to send data to segment 2 made up of channels in connectors 0 and 1.
 - BSA 0: Binary Start Address is 00000. The first transferred byte will be stored to this address.
 - BLI 1: Transfer expected data from computer to analyzer.

Analyzer Fast Binary Transfer

- 110 Initialize Buffera\$ to a string of zero length. (This is good programming practice, although in this case not necessary, since Buffera\$ has previously not been used and therefore defaults to zero length.)
- 120/140 Converts numeric values 255 to 245 into binary equivalents and stores them in the string Buffera\$. Buffera\$ starts off with a length of zero. The first time round the loop the variable N equals 255 and this is added to the string. The string Buffera\$ then has a length of 1 and contains a binary 1111111. Second time round the loop it has a length of two and contains 1111111 11111110, and so on. This way a binary down-counter is created, which later in the program is sent to the analyzer.
- 150 Send binary data contained in Buffera\$ to the analyzer HP-IB binary address, beginning at the data transfer start address (defined in line 100). Length of the data string is given in Buffera\$ and comes from line 120.
END: Indicates to the analyzer the end of the data transfer.
- 160 Select a new type of transfer.
BTK 2: Transfer expected data from analyzer to computer.
The other setting up commands are still valid from line 100.
- 170 Commands the controller to read from the analyzer HP-IB binary address into the Bufferb\$ string.
USING: Declares the format
-K = free field
% = terminate on EOI (End or Identify)
= suppress all statement terminators (such as CR, LF; these would be entered as normal data in this situation)
- 180 Sets up connectors 2 and 3 to receive channel data (not strobe data) starting at data transfer address 00003. The line is the same as line 100, except that now the data is to be sent to analyzer connectors 2 and 3, and the transfer start address has been changed to 00003.
- 190 Send binary data contained in Bufferb\$ (brought back from the analyzer in line 170) to the analyzer HP-IB binary address, beginning at the data transfer start address (defined in the previous program line). Length of the data string is given in Bufferb\$ and is the same as that of Buffera\$.
END: Indicates to the generator the end of the data transfer.

You could also use the TRANSFER command to send the binary data to the generator. With this command unformatted data can be transferred even faster than with the OUTPUT command used in this example. However the use of the TRANSFER command requires extra programming overhead, and to realize its potential fully, also extra hardware.

Analyzer Memory Arrangements

The contents of the Expected Data and Received Data Memories and the Bit Mask Memory depend on the operating mode selected and the state of the Glitch Detector. It is obviously important to know the current arrangement of these memories when transferring data with the Fast Binary Transfer Mode or when using the analyzer talker modes (discussed later) to obtain received data, error information and so on, from the analyzer. The following memory maps indicate the memory content of various Binary Start Addresses during the two analysis modes, and for the Received Data Memory map also with Glitch Detection switched on or off. The maps cover both the A- and the B-version of the analyzer.

Analyzer Fast Binary Transfer

Figure 8-4 shows a map of the Expected Data Memory. The first column gives the Binary Start Addresses (BSA), which are the physical addresses selected. The second and third columns give the logical addresses for the Trigger Start Analysis (OPR1) and Trigger Stop Analysis (OPR2) operating modes. The logical address is always the same as that displayed on the Expected Data Page when either Trigger Start Analysis or Trigger Stop Analysis is selected.

BSA	OPR1	OPR2
0000/00000	+0000/+00000	-1023/-16383
.	.	.
.	.	.
.	.	.
0511/08191	+0511/+08191	-0512/-08192
0512/08192	+0512/+08192	-0511/-08191
.	.	.
.	.	.
.	.	.
1023/16383	+1023/+16383	-0000/-00000

Figure 8-4. Map of Expected Data Memory

Figure 8-5 shows a map of the Received Data Memory. The first column gives the Binary Start Addresses (BSA), that is, the physical addresses selected. The second and third columns give the logical addresses for the Trigger Start Analysis (OPR1) and Trigger Stop Analysis (OPR2) operating modes with Glitch Detection switched off (GLD2). The third and fourth columns give the logical addresses for the Trigger Start Analysis (OPR1) and Trigger Stop Analysis (OPR2) operating modes with Glitch Detection switched on (GLD1). The logical address is always the same as that displayed on the State List Page for all four conditions in Figure 8-5.

BSA	OPR1 GLD2	OPR2 GLD2	OPR1 GLD1	OPR2 GLD2
0000/00000	+0000/+00000	-1023/-16383	+0000/+00000	-0511/-08191
.
.	.	.	Get Data	Get Glitch Information
.
0511/08191	+0511/+08191	-0512/-08192	+0511/+08191	-0000/-00000
0512/08192	+0512/+08192	-0511/-08191	+0000/+00000	-0511/-08191
.
.	.	.	Get Glitch Information	Get Data
.
1023/16383	+1023/+16383	-0000/-00000	+0511/+08191	-0000/-00000

Figure 8-5. Map of Received Data Memory

The 8182B analyzer has three additional binary transfer modes, as we have seen at the beginning of this section. An extra binary listener transfer BLI3 and two more binary talker transfers BTK4 and BTK5.

BLI3 - transfers word mask data from the computer to the analyzer.

BTK4 - transfers word mask data from the analyzer to the computer

BTK5 - transfers error map data from the analyzer to the computer

Analyzer Fast Binary Transfer

These binary transfer modes differ from the other modes (supported by both the A- and B-version) in that each byte contains information for 8 consecutive vectors, whereas the other modes transfer bytes contain information for 8 consecutive bits. Figure 8-6 shows how the word mask data and error map data is stored in the analyzer.

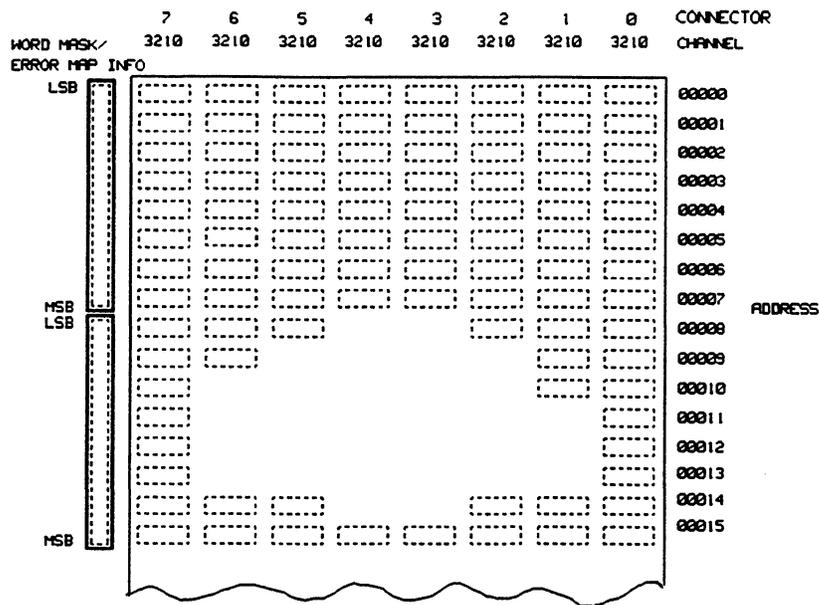


Figure 8-6. Storing Binary Word Mask and Error Map Data in the Analyzer

This is somewhat similar to the way strobe channel data is stored in the generator. However, there is one important difference. The starting address for the binary transfer (BSA) can be specified. You can specify any address without regard for byte boundaries. The analyzer calculates the correct starting address for the transfer. It is up to you to make sure however that the preceding bits are also transferred if the BSA does not lie on an address that is a multiple of 8. For this reason it is strongly recommended to perform binary transfers of word mask and error map data with BSA dividable by 8 without remainder. If we call this new address EBSA (Effective Binary Start Address), then we can calculate it using the following formula:

$$\text{EBSA} = \text{BSA} - (\text{BSA} \text{ MOD } 8)$$

Assume for example, that we want to obtain error map information from a vector at address 00012 (see Figure 8-6). Then:

$$\begin{aligned} \text{EBSA} &= 12 - (12 \text{ MOD } 8) \\ \text{EBSA} &= 12 - (4) \\ \text{EBSA} &= 8 \end{aligned}$$

The calculated Binary Start Address is 00008 and from the transferred byte we need bit 4. A safe method of changing the word mask is to read the old word mask from the analyzer, change it, and write it back to the analyzer.

The memory map for word mask and error map data is shown in Figure 8-7. The first column gives the Effective Binary Start Addresses (EBSA), that is, the physical addresses calculated. The second and third columns give the logical addresses for the Trigger Start Analysis (OPR1) and Trigger Stop Analysis (OPR2) operating modes with Glitch Detection switched off (GLD2). The third and fourth columns give the logical addresses for the Trigger Start Analysis (OPR1) and Trigger Stop Analysis (OPR2)

Analyzer Fast Binary Transfer

operating modes with Glitch Detection switched on (GLD1). The logical address is always the same as that displayed on the State List Page for all four conditions in Figure 8-7.

In BTK4 and BLI3 a "1" means word mask in that vector is set, a "0" means word mask is not set. In BTK5 a bit set to "1" means that an error has occurred somewhere in one or more bits in that vector.

BSA	OPR1 GLD2	OPR2 GLD2	OPR1 GLD1	OPR2 GLD2
00000	+00000	-16383	+00000	XXXXXX
.	.	.	.	(Not used)
.	.	.	.	
08191	+08191	-08192	+08191	XXXXXX
08192	+08192	-08191	XXXXX	-08191
.	.	.	(Not used)	.
.
16383	+16383	-00000	XXXXX	-00000

Figure 8-7. Memory Map for Word Mask and Error Map Data

Local, Remote, Local Lockout and Remote Lockout

To return the analyzer to local control (from remote), several possibilities exist. You can press the **LOCAL** softkey, or you can do it remotely from the computer. You can either send the BASIC command:

LOCAL 703,

where 703 is the HP-IB ASCII address, or you can send the low level GTL (Go To Local) HP-IB command:

SEND 7;LISTEN 3 CMD 1.

Power-up reset also returns the analyzer to local control.

To avoid the possibility of data transmissions being interrupted, which can happen if the analyzer is returned to local control via the front panel **LOCAL** softkey, it is recommended that local lockout be set to disable the softkey. You can do this by sending the BASIC command:

LOCAL LOCKOUT 7.

This locks out local operation of all listeners on the HP-IB select code 7 currently in remote mode. If you do not wish to perform a blanket lockout, you can do a selective one by sending the low level LLO (Local Lockout) HP-IB command:

SEND 7;LISTEN 3 CMD 17

The **LOCAL** softkey disappears and its function is disabled. The affected device does not have to be in remote mode to accept this command. The device can now be brought back into the local mode only remotely by sending one of the commands forcing the device into local, described above. Power-up reset also returns the analyzer to local control (and enables the **LOCAL** softkey).

Analyzer Fast Binary Transfer

To enable the **LOCAL** softkey, you have to send the BASIC command:

LOCAL 7.

This returns all devices on the HP-IB select code 7 to local mode and cancels any existing LOCAL LOCKOUTs. The analyzer can now be operated from the front panel, but will not accept any remote commands. To enable remote programming, send the BASIC command:

REMOTE 703.

The analyzer is back to its original state, that is remote programming and front panel operation are possible, and the **LOCAL** softkey is available.

For further details on the commands discussed here refer to the BASIC 4.0 Language Reference.

Summary

So far in this chapter we have learned how to set up HP-IB addresses, how to program the analyzer from a computer via HP-IB, and how to send data to the analyzer and read it back to the computer.

The task of this chapter is not to make you familiar with all of the HP-IB commands for the analyzer but to give you an overview of the most important programming techniques. A full listing of all the HP-IB programming commands for the analyzer is given in Chapter 10. Chapter 10 gives an alphabetical listing of all the analyzer HP-IB commands, and also groups the commands into functional sections.

The analyzer Pages not covered in this chapter are the following:

- Miscellaneous Page
- State List Page
- Timing Diagram Page
- Error Map Page
- Remote Message Page

The number of HP-IB commands for these Pages is small and the parameters they relate to are not of primary importance to the operation of the analyzer. The Miscellaneous Page is an information page. It also has commands dealing with the storing and recalling of parameter sets. An example of such a command is RCL4, which has been used extensively in the example programs. The State List Page displays the received data as it comes in and can display any errors that may occur. Its only command pertains to error display. The Timing Diagrams Page commands are used for error display and display scaling factors. The Error Map Page commands are used for highlighting errors, enabling the Error Count and displaying glitches. The Remote Message Page is the eighth Page and corresponds to the blank softkey on the analyzer SELECT PAGE menu. This Page can be accessed only via the HP-IB with the command REP8.

Additional HP-IB command groups that have not been covered here are the Operation Commands group and the Universal Commands group. The commands are covered in Chapter 10, HP-IB Syntax Diagrams.

If you want to find the syntax of a command not covered here, look it up in the relevant section in Chapter 10. For example, to find out the correct syntax for the command to start the analyzer, turn to the Operation Commands Section.

Our next topic is the analyzer talker modes, with which the analyzer can send various information to the computer.

Analyzer Talker Modes

it to one of the three parameter set storage locations first, using the command SEx (Transfer Parameter SET x, where x is 1, 2 or 3) and then recall this parameter set with the command RCL x, where x has the same value as before. The analyzer can now make use of the parameter set. We are going to take Parameter Set 1 for this exercise.

```
o
o
o 10 DIM A$(6)[74]
o 20 Ana=703
o 30 OUTPUT Ana;"PAG3 CAS B 33 32 31 30 20 22 21 20 13 12 11 10 03 02 0"
o 40 OUTPUT Ana;"TLK2"
o 50 FOR I=1 TO 6
o 60 ENTER Ana;A$(I)
o 70 NEXT I
o 80 OUTPUT Ana;"RCL4"
o 90 WAIT .5
o 100 OUTPUT Ana;"SE1";A$(1);A$(2);A$(3);A$(4);A$(5);A$(6)
o 110 OUTPUT Ana;"RCL1"
o 120 END
o
o
o
o
```

The function of the program lines is explained below:

- 10 Define a string array of 6 strings, each containing 76 characters.
- 30 Display the Expected Data Page. Set up a single segment containing 16 channels.
- 40 Instruct the analyzer to function as a talker in mode 2.
- 50/70 Read the data from the analyzer one string at a time (and store it in the string array A\$).
- 80 Modify the current parameter set by recalling the Standard Set.
- 100 Download the original set of parameters to Parameter Set 1, (overwriting the previously held parameter set).
- 110 Recall Parameter Set 1.

Exercise - Storing Analyzer Parameters to Disc

The analyzer allows you to store up to three different parameter sets in its memory. If you have a lot of different tests to perform, you may need to hold more than this number. Using discs as a storage media allows you to store as many parameter sets as you need.

We are going to use a short program to do this. The technique is similar to that of the previous example, except that now we are going a stage further and storing the received parameter set to disc. But first, we need to create an empty file on our disc, into which we are going to store the parameter set. For each parameter set a new disc file is needed.

The disc file where we shall store the parameter set is a binary data (bdat) file. To create a binary data file on the current disc (the one that would be accessed without changing the Mass Storage Identifier - for details see the BASIC 4.0 Language Reference Manual), type into your computer:

```
CREATE BDAT "PARSET_ANA", 2 
```

where PARSET_ANA is the name we have just given to the new disc file that is going to hold the analyzer parameter set, and 2 specifies the file size as two sectors. We do not need more than two sectors to store the six strings.

Analyzer Talker Modes

- 30 **PAG1:** Select the Control Page.
 LIN1: Set line 1 of the analyzer display as the first line to be transferred.
 TLK3: instruct the analyzer to function as a talker in mode 3.

- 40/70 Read the data from the analyzer display one line at a time and send it to the computer screen. Note that in order to prevent the display on the computer from scrolling upwards, "T" cannot be greater than 18.

TLK 4 Expected Data

The TLK 4 mode outputs the contents of the specified word of the analyzer Expected Data memory, formatted according to the actual channel configuration and coding settings of the analyzer.

Expected Data obtained with this mode cannot later be directly downloaded back to the analyzer. For this purpose there is the Fast Binary Transfer Mode and the ASCII transfer commands TSA, DAT and DAM which have been discussed in Section 8-6, Expected Data Page Programming.

The following example program displays the Expected Data Page on the analyzer screen and repeats it on the computer screen. Type it into your computer and run it.

```
o                                     o
o                                     o
o  10   DIM A$(50)                    o
o  20   Ana=703                        o
o  30   OUTPUT Ana;"PAG3 TSA0 TLK4"    o
o  40   FOR I=1 TO 22                  o
o  50     ENTER Ana;A$                 o
o  60     PRINT A$(1,50)               o
o  70   NEXT I                         o
o  80   END                            o
o                                     o
o                                     o
o                                     o
o                                     o
```

The function of the program lines is explained below:

- 10 Define a string containing 50 characters.

- 30 Select the Expected Data Page. Transfer Start Address is 00000. The first word will be transferred from address zero. Instruct the analyzer to function as a talker in mode 4.

- 40/70 Read the data from the analyzer Expected Data memory one word at a time and display it on the computer screen. The seventh character in the case of a 8182A and eighth in the case of an 8182B is the word mask. This can be an X when the mask is set or a period (.) when the mask is not set.

TLK 5 Received (Captured) Data

The TLK 5 mode outputs the contents of the specified word of the analyzer Received Data memory, formatted according to the actual channel configuration and coding settings of the analyzer. In effect, in this mode the analyzer outputs the contents of the State List Page.

The following example program displays the State List Page on the analyzer screen and repeats it on the computer screen. Type it into your computer and run it.

Analyzer Talker Modes

The function of the program lines is explained below:

- 10 Define a string containing 50 characters.
- 30 Select the Error Map Page. Instruct the analyzer to function as a talker in mode 8.
- 40 Read the channel marking string from the analyzer.
- 50 Display the string on the computer screen.

TLK 9 Servicing of Analyzer

TLK 9 mode is for the use of qualified service personnel only. Its use by other people is to be avoided as it can corrupt the analyzer internal memory.

TLK A Error Map (Errors and Data)

TLK A mode is supported only on the 8182B analyzer. It outputs the contents of the specified word of the Received Data memory formatted according to the actual channel configuration and coding settings of the analyzer. On this data is superimposed error and glitch information. TLK A is effectively a combination of TLK 5 and TLK 6, but it returns the full data and error/glitch information, no matter what the current segment code is (binary, octal or hex). The information returned is encoded according to Table 8-1.

Table 8-1. TLK A Mode Data Coding

DATA	NO ERROR NO GLITCH	ERROR NO GLITCH	NO ERROR GLITCH	ERROR GLITCH
0	0	.	G	!
1	1	/	H	"
2	2	i	I	#
3	3	j	J	\$
4	4	k	K	%
5	5	l	L	&
6	6	m	M	'
7	7	n	N	(
8	8	o	O)
9	9	p	P	*
A	A	q	Q	+
B	B	r	R	,
C	C	s	S	<
D	D	t	T	=
E	E	u	U	>
F	F	v	V	?
-	-	w	W	@

The last entry in the table is a hyphen (-), which means the data received has an intermediate level (only in dual threshold mode).

The following example program displays the State List Page on the analyzer screen and repeats it on the computer screen with error and glitch data superimposed. Type it into your computer and run it.

8-9 Analyzer Service Request Messages - Status Byte

When the analyzer detects an error condition, it responds by requesting service. Conditions causing service requests include the stop routine executed, fast clock detected, incorrect programming commands such as syntax errors, incorrectly formatted statements and addressing hardware which is not installed, and operator action via the SRQ softkey. Any of these will result in the SRQ control line of the HP-IB being set true, and SRQ will be displayed at the top of the analyzer's display area in line 1.

The analyzer can then be "serial polled". For HP 9000 Series 200 and 300 computers, the command is SPOLL (HP-IB address). In response the analyzer outputs an 8 bit Status Byte onto the HP-IB. The byte can then be decoded and interpreted by the computer.

The Status Byte is encoded as eight individual bits DIO 1 to DIO 8 (Data I/O lines when referring to HP-IB). Each represents an error condition or a warning. The bits come up independently of each other, therefore several of them can come up at the same time.

The complete list of error and warning messages is given in Table 8-2.

Table 8-2. Status Byte Messages

STATUS BYTE	ERROR OR WARNING MESSAGE
DIO 8	Power-on Test failed
DIO 7	Request Service
DIO 6	Fast Clock detected
DIO 5	Stop Routine executed
DIO 4	User Service Request from SRQ softkey
DIO 3	Autocorrection done *
DIO 2	Wrong Value programmed
DIO 1	Statement not recognized by interpreter or not allowed

(*) Autocorrection occurs when the analyzer itself changes a parameter setting. For example, if Trigger Delay has been set to 00000 and then the Real Time Compare mode is selected, Trigger Delay is automatically set to 00001 and DIO 3 is set to '1'.

Additional details concerning the Status Byte are as follows:

- The analyzer provides two levels of error reporting. Two registers are employed for the Status Byte: the Service Request Register and the Accumulation Register. When an error occurs the appropriate error bit and the Service Request bit are set in the Service Request Register. Sending a serial poll to the analyzer reads the bits out and clears the register.

If other errors occur before a serial poll is sent, they get diverted into the Accumulation Register. Thus all errors except the first get ORed into this register. Sending a Service Request to the analyzer now reads out the contents of the Service Request Register and copies the contents of the Accumulation Register into the Service Request Register. A second serial poll reads out the Service Request Register again and clears it. A copy operation between the registers still takes place, but the Accumulation Register is now empty. This way errors of all types are detected. If there are several errors of the same type, they will register as one error. It is therefore up to the programmer to structure his software in such a way as not to lose any of the error messages. This may for instance take the form of a subroutine call to a Status Byte interpreting code after each analyzer programming line or after a group of programming lines. Another approach may be an interrupt service routine to catch the errors as they occur.

Analyzer Service Request Messages - Status Byte

- DIO 8 (*Power-on Self Test Failed*) bit does not cause a Service Request, but disables remote operation of the analyzer until the softkey **CONTINUE** is pressed. (The analyzer then continues operation, albeit with the fault present - refer to Switching On the Analyzer, at the end of Section 4-3.)
- The Service Request Register is always "emptied" when read by two serial polls, except when the Power-on Self Test fails.
- DIO 5 (*Stop Routine Executed*) bit can be used to indicate to the computer that a measurement cycle is completed (IDLE state entered) and that data transfer (for instance of captured data) can commence.
- DIO 7 (*Request Service*) bit is always set whenever any of the DIO 1 to DIO 6 bits are set.

Bits DIO 1 to DIO 6 can be masked using the MSK command. For example, the program line: `Output Ana_ascii;"MSK 16"`, masks all of the maskable bits except for DIO 5, by sending a binary mask 010000 (decimal 16). This can be used to sense the end of a measurement cycle, ignoring the other status bits. The decimal value 63 is the default forced at power-on and at an HP-IB address switch change. If you mask bit DIO4 user Service Request from the SRQ softkey with `Output Ana_ascii;"MSK 55"`, the SRQ softkey will not be displayed in the remote mode and is disabled.

The following program can be used to decode the individual messages from the Status Byte. Some of the program's features have not been used (certain lines have been deactivated - turned into comments) so as not to make the error printout too cluttered. However, you can activate them to see their effect on the error message printout.

The program uses an interrupt service routine which is activated by an interrupt sent by the analyzer whenever it detects a problem of some sort. The program masks off all the bits of the Interrupt Enable Mask Register except bit 1, the SRQ bit. When a programming error is detected by the analyzer (or any other addressed device on the bus), the HP-IB SRQ control line is activated until an SPOLL is sent to the relevant device. The device then replies by sending the Status Byte onto the bus.

The program consists of two main parts. The first part is the parameter programming part, where various HP-IB commands are sent to the analyzer. The second part is the interrupt service routine, which decodes the Status Byte sent by the analyzer.

Not all of the Status Byte bits represent errors. DIO 5 (value 16 decimal) is set whenever the STOP routine is executed. In order that the DIO 5 bit can be trapped by the same interrupt service routine that also traps errors, the main parameter programming part contains a loop which causes the program to "wait" for the analyzer STOP routine to be executed. When DIO 5 (and DIO 7) are set true, the program does not return to the main parameter programming part as is the case with the other Status bits, but stops inside the interrupt service routine.

If there are more devices on the HP-IB, which is normally the case in a test setup, then the program must poll each device on the bus to find out which one has requested service. It is the device that has Bit 6 (DIO 7) of the Status Byte set. Only then can the correct Status Byte be read and decoded. The program below polls only the analyzer, as there are no other instruments in our setup.

Analyzer Service Request Messages - Status Byte

```

o
o
o 10 Ana=703
o 20 ON INTR 7 GOSUB Srq_ana
o 30 ENABLE INTR 7;2
o 40 !
o 50 !=====
o 60 !
o 70 OUTPUT Ana;"PAG2 RCL4"
o 80 OUTPUT Ana;"CLK2 CKP 2MS"
o 90 OUTPUT Ana;"CAS B 53 52 51 50 43 42 41 40"
o 100 OUTPUT Ana;"ADS H 33 32 31 30;ADS B 23 22 21 20"
o 110 OUTPUT Ana;"ADS O 33 32 31 30 23 22 21 20 13 12 11 10 03 02 01 00"
o 120 OUTPUT Ana;"ADS B 33 32 31 30 20"
o 130 OUTPUT Ana;"RUN"
o 140 PRINT
o 150 Loop: GOTO Loop
o 160 STOP
o 170 !
o 180 !=====
o 190 !
o 200 Srq_ana: !
o 210 PRINT
o 220 WAIT .1
o 230 D=SPOLL(Ana)
o 240 !PRINT "Status Word is ";D,IVAL$(D,2)
o 250 !
o 260 IF BINAND(D,128) THEN
o 270 PRINT "WARNING: Power On Test Failed"
o 280 END IF
o 290 !
o 300 !IF BINAND(D,64) THEN
o 310 ! PRINT "WARNING: Request Service"
o 320 !END IF
o 330 !
o 340 IF BINAND(D,32) THEN
o 350 PRINT "WARNING: Fast Clock Detected"
o 360 END IF
o 370 !
o 380 IF BINAND(D,16) THEN
o 390 PRINT "WARNING: STOP Routine Executed"
o 400 BEEP
o 410 STOP
o 420 END IF
o 430 !
o 440 IF BINAND(D,8) THEN
o 450 PRINT "User Service Request from SRQ softkey"
o 460 END IF
o 470 !
o 480 IF BINAND(D,4) THEN
o 490 PRINT "WARNING: Autocorrection done"
o 500 END IF
o 510 !
o 520 IF BINAND(D,2) THEN
o 530 PRINT "WARNING: Wrong Value Programmed"
o 540 END IF
o 550 !
o 560 IF BINAND(D,1) THEN
o 570 PRINT "WARNING: Statement not recognized by Interpreter or not
o 580 END IF
o 590 !
o 600 !=====
o 610 !
o 620 BEEP
o 630 ENABLE INTR 7;2
o 640 RETURN
o 650 END
o
o
o
o

```

The function of the program lines is explained below:

10 Assign analyzer (ASCII) address.

Analyzer Service Request Messages - Status Byte

- 20 Trap interrupt at HP-IB interface select code 7 (that means an interrupt from any device connected to that HP-IB, including the analyzer) and execute subroutine Srq.
- 30 Enable the SRQ Bit in the Interrupt Enable Mask Register of HP-IB interface with select code 7 as the only source of interrupt to the computer.
- 70/120 Program the analyzer. In line 80 the internal clock is selected together with a relatively long clock period (2ms), to introduce an appreciable delay between starting the analyzer and the receipt of the Stop Routine Executed interrupt. If you wish to change the clock period, remember that only values in the 2,5,10 sequence are allowed.
- 130 Start the analyzer. The analyzer runs until its memory is full, at which point it stops and sends an interrupt Stop Routine Executed.
- 150 Drop into an endless loop. The program "waits" for an interrupt from the analyzer.
- 160 Stop the program. The program is now effectively at its end.
- 200 Start of interrupt service routine Srq_ana. The routine reads the status byte and decodes it into individual warning and status messages.
- 220 Introduce a wait statement of 100ms to give the analyzer time to respond with all the relevant bits of the Status Byte.
- 230 Perform serial poll on the analyzer and read the Status Byte into variable D.
- 240 Print the Status Byte encoded in binary (prints also eight leading zeros). This line is not needed for printing out error messages and is therefore not activated.
- 260/280 Mask off all bits except for DIO 8. If this bit is true, print out the message.
- 300/320 Mask off all bits except for DIO 7. If this bit is true, print out the message. These lines cause the "Request Service" message to come up every time any of the other messages are output. Therefore the lines have been disabled.
- 340/360 Mask off all bits except for DIO 6. If this bit is true, print out the message.
- 380/420 Mask off all bits except for DIO 5. If this bit is true, print out the message and attract attention to the warning message with a beep. Stop the program as this was the Stop Routine Executed bit.
- 440/460 Mask off all bits except for DIO 4. If this bit is true, print out the message.
- 480/500 Mask off all bits except for DIO 3. If this bit is true, print out the message.
- 520/540 Mask off all bits except for DIO 2. If this bit is true, print out the message.
- 560/580 Mask off all bits except for DIO 1. If this bit is true, print out the message.
- 620 Attract attention to each warning message with a beep.
- 630 Enable interrupts so that the service routine can be executed next time the analyzer issues an interrupt.
- 640 Return to the main program (lines above the Interrupt service routine).

As the program stands, the interrupt service routine will be executed once, when the analyzer Stop Routine executes. There are no errors in the parameter programming part. You can activate the service routine several times by introducing errors into the parameter programming part.

Analyzer Service Request Messages - Status Byte

Experiment on your own, or press the SRQ softkey and try out the following changes and additions to obtain a selection of error and warning messages on the computer screen.

```
70  OUTPUT Ana;"PAG2 RCL4 OPR3"  
110 OUTPUT Ana;"QDS O 33 32 31 30 23 22 21 20 13 12 11 10 03 02 01 00"  
120 OUTPUT Ana;"ADS B 33 32 31 30 29"
```

The following error messages appear as a result of the errors in the above program lines.

```
User Service Request from SRQ softkey  
WARNING: Autocorrection done  
WARNING: Statement not recognized by Interpreter or not allowed  
WARNING: Wrong Value Programmed  
  
WARNING: Stop Routine Executed
```

Note that the analyzer issues a service request when it detects an erroneous HP-IB programming command on a line. When there are more than one of these on a programming line, the analyzer does not flag the second and subsequent errors. However, as long as there is at least one erroneous command on a program line, the analyzer flags up an error, and you can then check the line for correctness.

If you are writing a large test program, it is reasonable to assume that there will be a few bugs in it. An interrupt routine such as the one in this program will trap the bugs, but will not help much in locating them quickly. It is therefore of benefit to include a serial poll command with the Status Byte interpreting code and a position pointer after each parameter programming section until the test program has been debugged.

Chapter 9

Programming Examples

9-1 Introduction

In this chapter we are going to put into practice what we have learned in Chapters 7 and 8, by running actual test programs. The programs are based on the tests carried out manually on the AM2909 sequencer in Chapter 6. They test the following device parameters:

- Propagation Delay
- Set-up Time
- Hold Time
- Output Level

We are going to use the generator to provide a data pattern at the R-inputs (channels 0-0 to 0-3) and to set the input control lines to a state in which the sequencer reads its R-inputs (channels 2-0 to 2-3).

The analyzer will be used to monitor the Y-outputs of the sequencer (channels 0-0 to 0-3) and the input control lines (channels 2-0 to 2-3). Refer to the block diagram of the sequencer in Figure 6-1. The DUT connection is the same as that described in Section 6-3. The connection diagram is shown in Figure 6-2.

9-2 Propagation Delay Test

Propagation Delay is defined as the time between data being clocked into a tested device (with the generator clock) and appearing at the output lines (monitored by the analyzer) without error.

To find out the Propagation Delay of the sequencer chip, we need to set up some data at its input lines and clock it in with the generator clock. The data must be steady before it can be clocked in. This means we can clock the data in *after* the specified Set-up Time for the device. We are going to use generator Clock 1 for this and select a clock delay of 15 ns - long enough for the input lines to stabilize.

The output lines of the device will be sampled after a time determined by the analyzer clock delay, the initial value of which we set to 40 ns. Again, a long enough time for the device to switch properly. We then reduce the analyzer clock delay in large steps until errors occur. The delay is now smaller than the Propagation Delay of the device. By increasing the analyzer clock delay in small steps, the errors will eventually be made to disappear.

The program will measure the Propagation delay as the time from clocking the data into the sequencer with the generator clock to the time it can be read out by the analyzer without errors. In other words, it is the value of the analyzer clock delay at the end of the test. If you need more clarification on the measurement principle used in this test refer back to Section 6-6 and Figures 6-3 and 6-4.

The flowchart in Figure 9-1 shows the major blocks of the program to measure the Propagation Delay of the device.

Initialization Block

Generator and analyzer parameters are programmed. The parameters must be well within the specifications of the tested device. Generator data is programmed. The analyzer and generator are started and a single measurement cycle is made. The analyzer loads the received data into its Expected Data Memory. This data is then used as a reference for subsequent measurements.

Propagation Delay Test

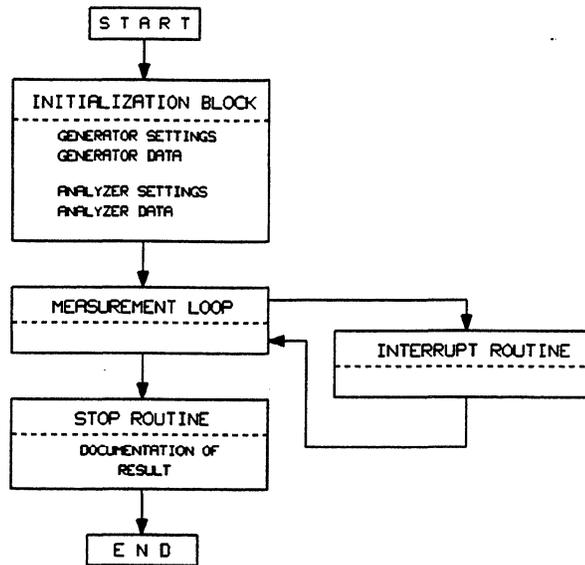


Figure 9-1. Program Flowchart for Propagation Delay Measurement

Measurement Loop

The sampling point delay of the analyzer clock is reduced by a fixed step and a *single* measurement cycle is initiated. In the meantime, the program goes into a wait loop. The computer is set to react to a service request from the analyzer, which occurs when the measurement cycle comes to its end (analyzer stop routine executed).

Interrupt Routine

The service request interrupts the (looping) program and diverts it to an interrupt routine. The routine programs the analyzer to send status information, from which it can be determined whether or not errors occurred in the (last) measurement cycle.

If no errors occurred, the sampling point delay of the analyzer clock is reduced by a further fixed step and another measurement cycle is started. This procedure repeats itself until errors are registered.

When errors occur, the sampling point delay of the analyzer clock is increased by a much smaller step and the procedure is repeated until no errors are again registered by the analyzer. The clock delay has now reached a value for which all outputs of the device under test switched properly. This value therefore represents the Propagation Delay of the tested device.

Stop Routine

In this block the measured value for Propagation Delay is written to the computer screen.

Propagation Delay Test

- 60 Force the analyzer into the IDLE state.
- 70/90 Clear Status Byte registers of generator and analyzer.
- 100 Trap interrupt at HP-IB interface select code 7 and go to label Status_pd (to read the analyzer Status Byte).
- 130 Recall generator Standard Set and call up the Timing Page.
- 140 Clear all generator segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 150 Set generator First Address to 0 and Last Address to 239. Set output high level of label A to 3.4 V.
- 160 Set generator output low level of label A to 0.2 V. Set strobe level to TTL. Set clock frequency to 1 MHz.
- 170 Set generator timing format on channels 0-0 to 0-3 to return-to-zero.
- 180 Set generator Clock 1 delay to 15 ns and width to 40 ns.
- 190 Set generator data to all "1's". Set an up-counter on segment 2 (second segment - channels 0-0 to 0-3). Clear channel data on channel 2-1. Clear strobe channel to zero. Set the Transfer Start Address to 0 and transfer a "1" to the strobe channel. This bit will be used to trigger the analyzer via the TRGARM input.
- 200 Select generator Cycle Mode SINGLE, enable outputs.
- 230 Recall analyzer Standard Set, clear all segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 240 Call up the analyzer Error Map Page. Set analyzer clock (Clock 1 from generator) delay to 40 ns. Switch autoarming off. Select positive slope as the Trigger Arm Input active slope.
- 250 Set analyzer stop delay to 239, switch Error Count on, mask off all bits of the analyzer Status Byte except bit 4 (Stop Routine executed).
- 270 Start analyzer.
- 280 Start Generator.
- 290 Include a wait statement to allow a single measurement cycle to take place.
- 300 Dump recorded data from the Received Data Memory to the Expected Data Memory. The analyzer now contains the data which will be used as a reference for comparison with the incoming data from the tested device during the test cycles that are to follow.
- 310 Clear the Service Request Register of the analyzer containing the status Stop Routine executed.
- 340 Define the analyzer clock delay increment as -1 (ns).
- 350 Define the starting value for the analyzer clock delay as 40 (ns).
- 360 Start of the REPEAT UNTIL loop.

Set-up Time Test

- 370/380 Analyzer clock delay will be incremented by -1 ns until errors are detected by the analyzer.
- 400 Enable the SRQ Bit in the Interrupt Enable Mask Register of HP-IB interface with select code 7 as the only source of interrupt to the computer.
- 410/420 Start analyzer and generator.
- 430 Remain in the wait loop until an interrupt from the analyzer comes. Note that if for some reason no interrupt occurs, the program will be stuck at this line.
- 460 Clear the Service Request register by serial polling the analyzer.
- 470 Instruct the analyzer to function as a talker in mode 1. In this mode the analyzer outputs current status information.
- 480 Read the status information into the character string Status\$.
- 490 Extract from the character string the error count E-count. On the B-version this is contained in characters 10 to 14. On the A-version is contained in characters 9 to 12. If you are using an 8182A analyzer, this line must read:
490 E_count=VAL(Status\$[9,12]).
- 500 Print out the error count in the current measurement cycle.
- 510 When errors occur while the analyzer clock delay is incrementing with a step of -1 ns, set the step to +100 ps. The clock delay will now increase after every measurement cycle until errors disappear (see the next line).
- 520 End of the REPEAT UNTIL loop. The loop repeats itself until error count is zero and the increment step is positive.
- 550 Restore the Status Byte mask to its default (power-up) setting.
- 570 The Propagation Delay of the device under test is the last value of analyzer clock delay.

9-3 Set-up Time Test

Set-up Time is defined as the time between data being placed on the data input lines of a tested device and the data being clocked into the device (with the generator clock) without any errors (monitored for by the analyzer) occurring.

To find out the Set-up Time of the sequencer chip, we need to set up some data on its input lines and clock it in with the generator clock. The data must be steady before it can be clocked in. This means we can clock the data in *after* the specified Set-up Time for the device. We shall select a channel data delay of 15 ns (after generator system clock). We therefore need to set the delay of generator Clock 1 to 30 ns - long enough for the input lines to stabilize. The output lines of the device will be sampled at a time after the Propagation Delay of the device to ensure that no errors occur due to this parameter being violated. We will set the analyzer clock delay to 40 ns, a time long enough for the device to switch properly.

We then reduce the delay of generator Clock 1 in large steps until errors occur, indicating that data has not been present on the input lines long enough prior to the clock edge. The delay is now smaller than the Set-up Time of the device. By increasing the generator clock delay in small steps, the errors will eventually be made to disappear.

Set-up Time Test

Set-up Time is measured as the time from setting data up on the device's input lines to clocking the data into the device without any errors occurring on the device's output lines. In other words, it is the value of the generator Clock 1 delay at the end of the test minus the generator channel data delay. Some devices can tolerate a clock edge occurring before data is placed on the input lines. In these cases the Set-up Time is negative. If you need more clarification on the measurement principle used in this test refer back to Section 6-7 and Figures 6-5 and 6-6.

The flowchart in Figure 9-1 can again be used, as the structure of the program to measure the Set-up Time of the sequencer is the same as that of the previous program.

```
o
o
o 10 Setup_time: !
o 20 DIM Status$(40)
o 30 Gen=707
o 40 Ana=703
o 50 OUTPUT Gen;"STP"
o 60 OUTPUT Ana;"STP"
o 70 Sg=SPOLL(Gen)
o 80 Sa1=SPOLL(Ana)
o 90 Sa2=SPOLL(Ana)
o 100 ON INTR 7 GOTO Status_st
o 110 !
o 120 ! Generator Settings -----
o 130 OUTPUT Gen;"RSS PAG2"
o 140 OUTPUT Gen;"CAS BY 23 22 21 20; ADS BY 03 02 01 00"
o 150 OUTPUT Gen;"FAD 0 LAD 239 HILA 3.4V"
o 160 OUTPUT Gen;"LOLA .2V STL1 FRQ 1.0 MHZ"
o 170 OUTPUT Gen;"FMT 00 1 FMT 01 1 FMT 02 1 FMT 03 1"
o 180 OUTPUT Gen;"DEL 03 15NS DEL 02 15NS DEL 01 15NS DEL 00 15NS"
o 190 OUTPUT Gen;"DEL 1C 30NS WID 1C 40NS"
o 200 OUTPUT Gen;"SED UPC 2 CCD 21 CLS TSA 0 FOR 1"
o 210 OUTPUT Gen;"CYM2 OUT2"
o 220 !
o 230 ! Analyzer Settings -----
o 240 OUTPUT Ana;"RCL4 CAS B 23 22 21 20; ADS B 03 02 01 00"
o 250 OUTPUT Ana;"PAG7 CKD 40NS AAD4 TAS1"
o 260 OUTPUT Ana;"SPD 239 CTE 1 MSK 16"
o 270 !
o 280 OUTPUT Ana;"RUN"
o 290 OUTPUT Gen;"RUN"
o 300 WAIT 1
o 310 OUTPUT Ana;"DRD"
o 320 Sa3=SPOLL(Ana)
o 330 !
o 340 Loop: ! Measurement Loop -----
o 350 Inc_gen_clk=-1
o 360 I=30
o 370 REPEAT
o 380 I=I+Inc_gen_clk
o 390 OUTPUT Gen;"DEL 1C";I;"NS"
o 400 !
o 410 ENABLE INTR 7;2
o 420 OUTPUT Ana;"RUN"
o 430 OUTPUT Gen;"RUN"
o 440 Wait_loop: GOTO Wait_loop
o 450 !
o 460 Status_st: !
o 470 Sr=SPOLL(Ana)
o 480 OUTPUT Ana;"TLK1"
o 490 ENTER Ana;Status$
o 500 E_count=VAL(Status$(10,14))
o 510 PRINT "Current Number of Errors is";E_count
o 520 IF E_count>0 AND Inc_gen_clk=-1 THEN Inc_gen_clk=.1
o 530 UNTIL E_count=0 AND Inc_gen_clk>0
o 540 !
o 550 Result: !
o 560 OUTPUT Ana;"MSK 63"
o 570 PRINT
o 580 PRINT "SET_UP TIME (NS) = ";I-15
o 590 END
o
o
o
```

Set-up Time Test

The function of the program lines is explained below:

- 20 Dimension a string Status\$ to hold the analyzer Status Byte.
- 30/40 Assign generator and analyzer (ASCII) addresses.
- 50/60 Force the generator into the STOP state and the analyzer into the IDLE state.
- 70/90 Clear generator and analyzer Status Byte registers.
- 100 Trap interrupt at HP-IB interface select code 7 and go to label Status_st (to read the analyzer Status Byte).
- 130 Recall generator Standard Set and call up the Timing page.
- 140 Clear all generator segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 150 Set generator First Address to 0 and Last Address to 239. Set output high level of label A to 3.4 V.
- 160 Set generator output low level of label A to 0.2 V. Set strobe level to TTL. Set clock frequency to 1 MHz.
- 170 Set generator timing format on channels 0-0 to 0-3 to return-to-zero.
- 180 Set the delay of generator channels 0-0 to 0-3 to 15 ns.
- 190 Set generator Clock 1 delay to 15 ns and width to 40 ns.
- 200 Set generator data to all "1's". Set an up-counter on segment 2 (second segment - channels 0-0 to 0-3). Clear channel data on channel 2-1. Clear strobe channel to zero. Set the Transfer Start Address to 0 and transfer a "1" to the strobe channel. This bit will be used to trigger the analyzer via the TRGARM input.
- 210 Select generator Cycle Mode SINGLE, enable outputs.
- 240 Recall analyzer Standard Set, clear all segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 250 Call up the analyzer Error Map Page. Set analyzer clock (Clock 1 from generator) delay to 40 ns. Switch autoarming off. Select positive slope as the Trigger Arm Input active slope.
- 260 Set analyzer stop delay to 239, switch Error Count on, mask off all bits of the analyzer Status Byte except bit 4 (Stop Routine executed).
- 280/290 Start analyzer and generator.
- 300 Include a wait statement to allow a single measurement cycle to take place.
- 310 Dump recorded data from the Received Data Memory to the Expected Data Memory. The analyzer now contains the data which will be used as a reference for comparison with the incoming data from the tested device during the test cycles that are to follow.
- 320 Clear the Service Request Register of the analyzer containing the status Stop Routine executed.
- 350 Define the generator Clock 1 delay increment as -1 (ns).

Hold Time Test

- 360 Define the starting value for the generator Clock 1 delay as 30 (ns).
- 370 Start of the REPEAT UNTIL loop.
- 380/390 Generator Clock 1 delay will be incremented by -1 ns until errors are detected by the analyzer.
- 410 Enable the SRQ Bit in the Interrupt Enable Mask Register of HP-IB interface with select code 7 as the only source of interrupt to the computer.
- 420/430 Start analyzer and generator.
- 440 Remain in the wait loop until an interrupt from the analyzer comes. Note that if for some reason no interrupt occurs, the program will be stuck at this line.
- 470 Clear the Service Request register to zero by serial polling the analyzer.
- 480 Instruct the analyzer to function as a talker in mode 1. In this mode the analyzer outputs current status information.
- 490 Read the status information into the character string Status\$.
- 500 Extract from the character string the error count E-count. On the B-version this is contained in characters 10 to 14. On the A-version is contained in characters 9 to 12. If you are using an 8182A analyzer, this line must read:
500 E_count=VAL(Status\$[9,12]).
- 510 Print out the error count in the current measurement cycle.
- 520 When errors occur while the generator clock delay is incrementing with a step of -1 ns, set the step to +100 ps. The clock delay will now increase after every measurement cycle until errors disappear (see the next line).
- 530 End of the REPEAT UNTIL loop. The loop repeats itself until error count is zero and the increment step is positive.
- 560 Restore the Status Byte mask to its default (power-up) setting.
- 580 The Set-up Time of the device is the last value of generator Clock 1 delay minus 15 ns.

9-4 Hold Time Test

Hold Time is defined as the time interval over which the input data signal must be present *after* the active clock edge (from the generator) occurs without any errors (monitored by the analyzer) occurring.

To find out the Hold Time of the sequencer chip, we need to set up some data on its input lines and clock it in with the generator clock. The data must be steady before it can be clocked in. This means we can clock the data in *after* the specified Set-up Time for the device. We shall select a channel data delay of 0 ns. We can then set the delay of generator Clock 1 to 30 ns - long enough for the input lines to stabilize. The output lines of the device will be sampled at a time after the Propagation Delay of the device to ensure that no errors occur due to this parameter being violated. We will set the analyzer clock delay to 40 ns, a time long enough for the device to switch properly.

We then increase the delay of generator Clock 1 in large steps until errors occur, indicating that data has not been present on the input lines long enough after the clock edge. The delay is now smaller than the

Hold Time Test

The function of the program lines is explained below:

- 20 Dimension a string Status\$ to hold the analyzer Status Byte.
- 30 Assign generator (ASCII) address.
- 40 Assign analyzer (ASCII) address.
- 50 Force the generator into the STOP state.
- 60 Force the analyzer into the IDLE state.
- 70/90 Clear Status Byte registers of generator and analyzer.
- 100 Trap interrupt at HP-IB interface select code 7 and go to label Status_ht (to read the analyzer Status Byte).
- 130 Recall generator Standard Set and call up the Timing page.
- 140 Clear all generator segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 150 Set generator First Address to 0 and Last Address to 239. Set output high level of label A to 3.4 V.
- 160 Set generator output low level of label A to 0.2 V. Set strobe level to TTL. Set clock frequency to 1 MHz.
- 170 Set generator timing format on channels 0-0 to 0-3 to return-to-zero.
- 180 Set generator Clock 1 delay to 30 ns and width to 40 ns.
- 190 Set generator data to all "1's". Set an up-counter on segment 2 (second segment - channels 0-0 to 0-3). Clear strobe channel to zero. Set the Transfer Start Address to 0 and transfer a "1" to the strobe channel. This bit will be used to trigger the analyzer via the TRGARM input.
- 200 Select generator Cycle Mode SINGLE, enable outputs.
- 230 Recall analyzer Standard Set, clear all segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 240 Call up the analyzer Error Map Page. Set analyzer clock (Clock 1 from generator) delay to 40 ns. Switch autoarming off. Select positive slope as the Trigger Arm Input active slope.
- 250 Set analyzer stop delay to 239, switch Error Count on, mask off all bits of the analyzer Status Byte except bit 4 (Stop Routine executed).
- 270 Start analyzer.
- 280 Start generator.
- 290 Include a wait statement to allow a single measurement cycle to take place.
- 300 Dump recorded data from the Received Data Memory to the Expected Data Memory. The analyzer now contains the data which will be used as a reference for comparison with incoming data from the tested device during the test that is to follow.

Level Measurement Test

- 310 Clear the Service Request Register of the analyzer containing the status Stop Routine executed.
- 340 Define the generator Clock 1 delay increment as -1 (ns).
- 350 Define the starting value for the generator Clock 1 delay as 30 (ns).
- 360 Start of the REPEAT UNTIL loop.
- 370/380 Generator Clock 1 delay will be incremented by -1 ns until errors are detected by the analyzer.
- 400 Enable the SRQ Bit in the Interrupt Enable Mask Register of HP-IB interface with select code 7 as the only source of interrupt to the computer.
- 410/420 Start analyzer and generator.
- 440 Remain in the wait loop until an interrupt from the analyzer comes. Note that if for some reason no interrupt occurs, the program will be stuck at this line.
- 460 Serial poll the analyzer, clear the Service Request register to zero.
- 470 Instruct the analyzer to function as a talker in mode 1. In this mode the analyzer outputs current status information.
- 480 Read the status information into the character string Status\$.
- 490 Extract from the character string the error count E-count. On the B-version this is contained in characters 10 to 14. On the A-version is is contained in characters 9 to 12. If you are using an 8182A analyzer, this line must read:
490 E_count=VAL(Status\$[9,12]).
- 500 Print out the error count in the current measurement cycle.
- 510 When errors occur while the generator clock delay is incrementing with a step of -1 ns, set the step to +100 ps. The clock delay will now increase after every measurement cycle until errors disappear (see the next line).
- 520 End of the REPEAT UNTIL loop. The loop repeats itself until error count is zero and the increment step is positive.
- 550 Restore the Status Byte mask to its default (power-up) setting.
- 570 The Set-up Time of the device under test is the last value of generator Clock 1 delay minus 15 ns.

9-5 Level Measurement Test

The high and low output voltage levels of a device are defined as follows: Output high is the minimum output voltage high level below which the output should not drop. Output low is the maximum output voltage low level above which the output should not rise. For a TTL device such as the AM2909 sequencer these are 2.4 V and 0.8V respectively.

To find out the output levels of the sequencer chip, we need to set up some data at its input lines and clock it in with the generator clock. The data must be steady before it can be clocked in. This means we can clock the data in *after* the specified Set-up Time for the device. We are going to use generator

Level Measurement Test

Clock 1 for this and select a clock delay of 15 ns - long enough for the input lines to stabilize. The output lines of the device will be sampled at a time after the Propagation Delay of the device. Analyzer clock delay of 40 ns is long enough to enable the device to switch properly. We must also set the analyzer inputs to the dual threshold mode and set the upper threshold below the expected voltage level when the output is high. Similarly, we need to set the lower threshold above the expected voltage level when the output is low.

We then increase the analyzer upper threshold in large steps until errors occur. The high level of the device's output is now not high enough to cross the upper threshold of the analyzer inputs. By lowering the threshold in small steps, the errors will eventually disappear.

A similar sequence is carried out to determine the low level of the device's output. However, first we have to return the upper threshold of the analyzer input channels back to the starting value to make sure that no errors can occur as a result of spurious variations in the output high level of the device. We increase the analyzer lower threshold in large steps until errors occur. The low level of the device's output is now not low enough to cross the lower threshold of the analyzer inputs. By raising the threshold in small steps, the errors will eventually disappear.

The program will measure the high and low output levels by comparing them to the analyzer input thresholds. Thus the levels will be the threshold levels of the analyzer inputs when no more errors are registered. If you need more clarification on the measurement principle used in this test refer back to Section 6-9 and Figure 6-9.

The flowchart in Figure 9-2 shows the major blocks of the program to measure the output level of the device. No interrupt service routine is used this time (although the program would function just as well with one). Instead, the analyzer is continuously serial polled after the start of each measurement cycle.

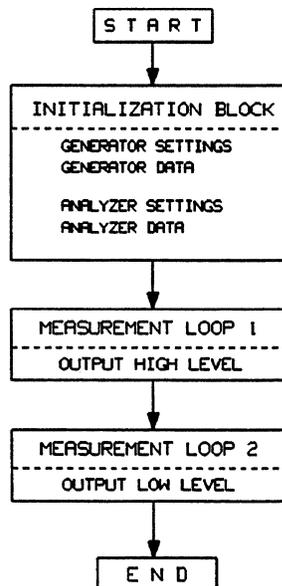


Figure 9-2. Program Flowchart for Level Measurement

Level Measurement Test

Initialization Block

Generator and analyzer parameters are programmed. The parameters must be well within the specifications of the tested device. Generator data is programmed. The analyzer and generator are started and a single measurement cycle is made. The analyzer loads the received data into its Expected Data Memory. The data is now used as a reference for the measurements that are to follow.

Measurement Loop 1

The upper threshold of the analyzer input is increased by a fixed step and a *single* measurement cycle is initiated. The program then goes round a loop waiting for the Stop Sequence Executed bit of the analyzer Status Byte to be set true. When this happens the analyzer is requested to send status information, from which it can be determined whether or not errors occurred in the (last) measurement cycle.

If no errors occurred, the upper threshold of the analyzer input is increased by a further fixed step and another measurement cycle is started. This procedure repeats itself until errors are registered.

When errors occur, the upper threshold of the analyzer input is lowered by a much smaller step and the procedure is repeated until no errors are again registered by the analyzer. The upper threshold has now reached a value which can safely be reached by the output stages of the tested device. This value therefore represents the high output level of the tested device.

Measurement Loop 2

The lower threshold of the analyzer input is lowered by a fixed step and a *single* measurement cycle is initiated. The program then goes round a loop waiting for the Stop Sequence Executed bit of the analyzer Status Byte to be set true. When this happens the analyzer is requested to send status information, from which it can be determined whether or not errors occurred in the (last) measurement cycle.

If no errors occurred, the lower threshold of the analyzer input is lowered by a further fixed step and another measurement cycle is started. This procedure repeats itself until errors are registered.

When errors occur, the lower threshold of the analyzer input is increased by a much smaller step and the procedure is repeated until no errors are again registered by the analyzer. The lower threshold has now reached a value which can safely be reached by the output stages of the tested device. This value therefore represents the low output level of the tested device.

Level Measurement Test

```
o
o
o 710 REPEAT
o 720 UNTIL BINAND(SPOLL(Ana),16)
o 730 OUTPUT Ana;"TLK1"
o 740 ENTER Ana;Status$
o 750 E_count=VAL(Status$[10,14])
o 760 DISP "Current Number of Errors is";E_count
o 770 IF E_count>0 AND Inc_ana_loa=-.1 THEN Inc_ana_loa=.01
o 780 UNTIL E_count=0 AND Inc_ana_loa>0
o 790 !
o 800 PRINT
o 810 PRINT "DEVICE OUTPUT LOW LEVEL (V) =";J
o 820 DISP ""
o 830 END
o
o
o
o
```

The function of the program lines is explained below:

- 20 Dimension a string Status\$ to hold the analyzer Status Byte.
- 30 Assign generator (ASCII) address.
- 40 Assign analyzer (ASCII) address.
- 50 Force the generator into the STOP state.
- 60 Force the analyzer into the IDLE state.
- 70/90 Clear Status Byte registers of generator and analyzer.
- 120 Recall generator Standard Set and call up the Output Page.
- 130 Clear all generator segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 140 Set generator First Address to 0 and Last Address to 239. Set output high level of label A to 3.4 V.
- 150 Set generator output low level of label A to 0 V. Set strobe level to TTL. Set clock frequency to 1 MHz.
- 160 Set generator timing format on channels 0-0 to 0-3 to return-to-zero.
- 170 Set generator Clock 1 delay to 30 ns and width to 40 ns.
- 180 Set generator data to all "1's". Set an up-counter on segment 2 (second segment - channels 0-0 to 0-3). Clear data on channel 2-1 to zero. Clear strobe channel to zero. Set the Transfer Start Address to 0 and transfer a "1" to the strobe channel. This bit will be used to trigger the analyzer via the TRGARM input.
- 190 Select generator Cycle Mode SINGLE, enable outputs.
- 220 Recall analyzer Standard Set, clear all segments and set up two binary coded segments containing channels 2-0 to 2-3 and 0-0 to 0-3.
- 230 Set analyzer connectors 0 and 1 to dual threshold mode. Set connectors 2 and 3 to dual threshold mode.

Level Measurement Test

- 240 Set the upper threshold of label A of analyzer data channels to 2 V. Set the lower threshold of label A to 1 V.
- 250 Set the upper threshold of label B of analyzer data channels to 2 V. Set the lower threshold of label B to 1 V.
- 260 Assign level labels to analyzer data channels. Device data lines are assigned the label A, the clock lines are assigned the label B. This way we can vary the threshold levels on the data lines without having to worry about the effect of the clock lines.
- 270 Call up the analyzer Error Map Page. Set analyzer clock (Clock 1 from generator) delay to 20 ns. Switch autoarming off. Select positive slope as the Trigger Arm Input active slope.
- 280 Set analyzer stop delay to 239, switch Error Count on.
- 300 Start analyzer.
- 310 Start Generator.
- 320 Include a wait statement to allow a single measurement cycle to take place.
- 330 Dump recorded data from the Received Data Memory to the Expected Data Memory. The analyzer now contains the data which will be used as a reference for comparison with incoming data from the tested device during the test that will follow.
- 340 Clear the Service Request Register of the analyzer containing the status Stop Routine executed.
- 380 Define the analyzer voltage increment of label A as 100 (mV).
- 390 Define the starting value for the analyzer label A voltage level as 2 (V).
- 400 Start of first outer REPEAT UNTIL loop.
- 410/420 Analyzer upper threshold level of label A will be incremented by 100 mV (until the analyzer detects errors).
- 440/450 Start analyzer and generator.
- 470/480 Go round this first inner REPEAT UNTIL loop serial polling the analyzer, until the Stop Routine Executed bit of the Status Byte is set true. (The bit is extracted with a binary AND.) Note that if for some reason this bit is not set, the program will be stuck in this loop.
- 490 Instruct the analyzer to function as a talker in mode 1. In this mode the analyzer outputs current status information.
- 500 Read the status information into the character string Status\$.
- 510 Extract from the character string the error count E-count. On the B-version this is contained in characters 10 to 14. On the A-version is contained in characters 9 to 12. If you are using an 8182A analyzer, this line must read:
510 E_count=VAL(Status\$[9,12]).
- 520 Display the error count in the current measurement cycle.

Level Measurement Test

- 530 When errors occur while the analyzer upper threshold voltage level of label A is incrementing with a step of 100 mV, set the step to -10 mV. The upper threshold voltage level of label A will now decrease after every measurement cycle until errors disappear (see the next line).
- 540 End of the first outer REPEAT UNTIL loop. The loop repeats itself until error count is zero and the increment step is negative.
- 550 Set the analyzer voltage level of label A back to its starting value of 2V.
- 580 The high output level of the device under test is the last value of the analyzer upper threshold of label A.
- 620 Define the analyzer voltage increment of label A as -100 (mV).
- 630 Define the starting value for the analyzer label A voltage level as 1 (V).
- 640 Start of second outer REPEAT UNTIL loop.
- 650/660 Analyzer lower threshold level of label A will be decremented by 100 mV (until the analyzer detects errors).
- 680/690 Start analyzer and generator.
- 710/720 Go round this second inner REPEAT UNTIL loop serial polling the analyzer, until the Stop Routine Executed bit of the Status Byte is set true. (The bit is extracted with a binary AND.) Note that if for some reason this bit is not set, the program will be stuck in this loop.
- 730 Instruct the analyzer to function as a talker in mode 1. In this mode the analyzer outputs current status information.
- 740 Read the status information into the character string Status\$.
- 750 Extract from the character string the error count E-count. On the B-version this is contained in characters 10 to 14. On the A-version is is contained in characters 9 to 12. If you are using an 8182A analyzer, this line must read:
750 E_count=VAL(Status\$[9,12]).
- 760 Display the error count in the current measurement cycle.
- 770 When errors occur while the analyzer lower threshold voltage level of label A is incrementing with a step of -100 mV, set the step to 10 mV. The lower threshold voltage level of label A will now increase after every measurement cycle until errors disappear (see the next line).
- 780 End of the second outer REPEAT UNTIL loop. The loop repeats itself until error count is zero and the increment step is positive.
- 810 The low output level of the device under test is the last value of the analyzer lower threshold of label A.
- 820 Remove error count reporting.

Conclusion

9-6 Conclusion

The test programs given in this chapter are very simple and a lot could be done to improve them. It has been the aim of this manual among other things to make you familiar with generator and analyzer programming and to show you how a device can be tested in practice. Its task is not to lay down guidelines on device testing techniques and good programming practices. Nevertheless, a few points could be mentioned.

Binary Search

Binary search considerably decreases the time required to test a device. This is especially apparent when the parameters of the tested device are known only approximately or not at all. The program tests for a range of given values, but it does not do so sequentially. It uses the binary search method instead. Thus if the program is given the high and low limit values for the current test, it tries for the middle value and checks for errors. Depending on whether errors occurred or not, the program carries on in the same direction or reverses the direction and again tries for a new half way value (which is now a quarter or three quarters of the way between the original limit values).

This sequence repeats itself until the program reaches the entered step size. The program can now switch to a new step size and repeat the sequence until the minimum entered step size or the maximum resolution of the system is reached.

The binary search represents a significant programming overhead and is beyond the scope of this manual.

Provision for Spurious Errors

Coupled to the binary search, a good test program would also make provisions for spurious errors. A program that does that, does not accept the first error-free result as the correct result. It makes repeated measurements at this value, typically five times, to see if any errors appear as a result of jitter, level variations and so on. If an error occurs, it backs off another step and tries again. Only when no errors appear, is the value accepted as the correct one.

None of the programs have this feature. That is why in the level measurement program in the previous section we have had to return the upper threshold of the analyzer inputs to the starting value. This is anyway a good thing to do when writing large programs that test several parameters of a device one after another. For example, Set-up Time should be measured with a long Hold Time and vice versa. A test program normally enters the spurious error code when the step has reached the minimum step size or the maximum resolution of the system.

Techniques such as these are used in the HP 81810A System software and are described in the System Software User Manual.

Chapter 10

HP-IB Syntax Diagrams

10-1 Introduction

This section contains a description of all HP-IB commands that are applicable for the HP 8180A/B Data Generator and HP 8182A/B Data Analyzer. The commands are listed in three different sections.

Section 10-4 lists all generator commands in separate groups in functional order. All the Control Page commands are listed, followed by the Timing Page commands, Output Page commands, and so on. If you need a command relating to for instance Fast Binary Transfer, then refer to the relevant group. Section 10-5 performs the same task, but for the analyzer commands. Having found the command(s) you need in these sections, turn to Section 10-6, listing all the commands alphabetically. Each command is supported by a syntax diagram and a brief description.

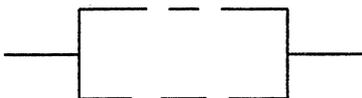
Each command is a mnemonic followed by one or more parameters or variables. The syntax for each command is shown by a syntax diagram, and each parameter and variable is explained. An expanded version of each mnemonic is also provided.

10-2 Syntax Drawings Explained

In this section, the syntax of each command is represented pictorially. Each keyboard entry is enclosed by an envelope. The type of envelope tells you whether the symbols inside it represent a constant value, an item, or a variable. The different types of envelope and their meanings are listed below:



A rounded envelope means that the characters inside must be typed in exactly as they appear. Be careful if the characters appear in upper case, that you also enter them in upper case.



A square envelope contains the name of a list of values, or of a variable. The list or range of the variable is shown underneath or alongside the diagram.

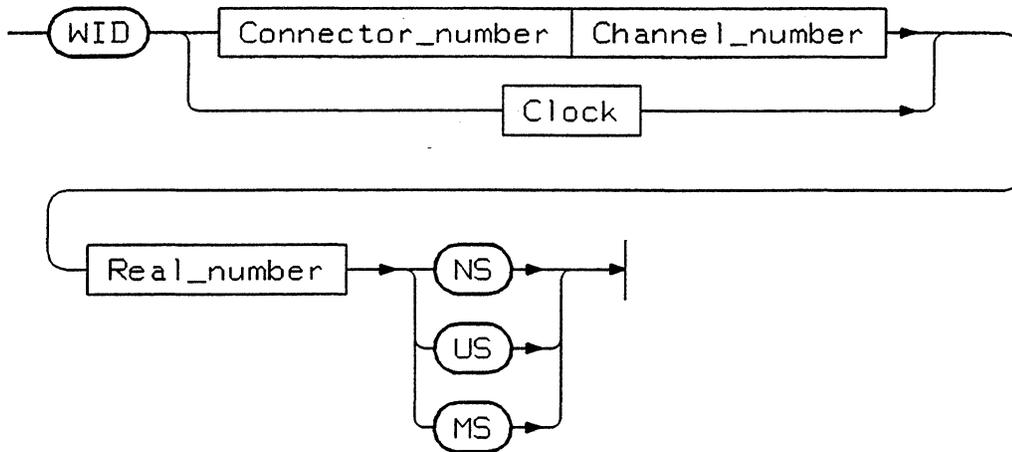


Lines and arrows indicate the valid paths and are used to show the correct sequence of symbols in the diagram. Lines diverging indicate options in the command. An example of such a command is given below.

When envelopes are connected by lines, this indicates that they are delimited by one or more blanks. Where envelopes are not separated by lines, the parameters or variables must be entered sequentially without delimiting blanks.

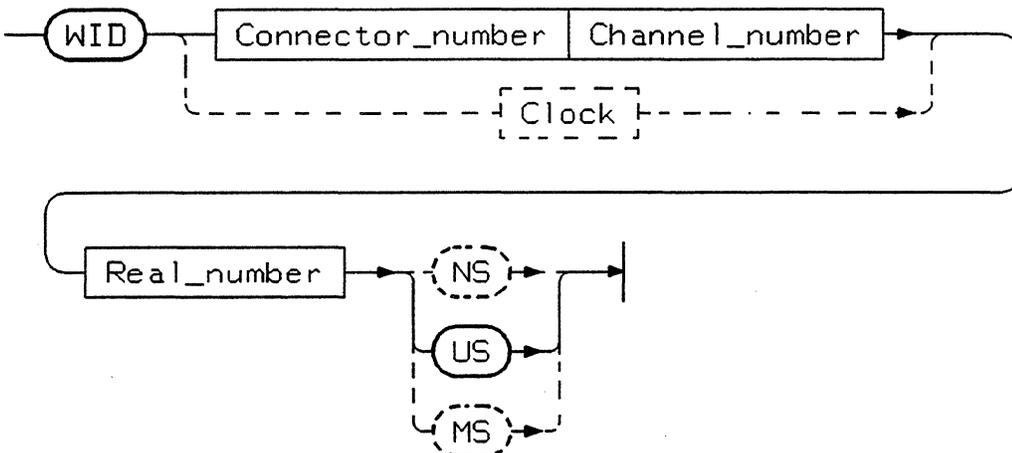
Example:

The diagram below shows the syntax for the **WID** command. This command enables you to set the width of a clock or channel pulse to a period ranging from 10 nanoseconds to 999 milliseconds.



- Clock** ≡: The identity of the generator clock, C1 or C2.
- Connector_number** ≡: Hexadecimal value representing the generator connector number, 0 to F (including extenders).
- Channel_number** ≡: Integer representing the channel number of the connector defined, 0 to 3.
- Real_number** ≡: Any positive real number between 0 and 99. Two places of decimal are allowed.

If you want to define a pulse delay of five microseconds for a particular channel, then the options you choose from the diagram are shown below.

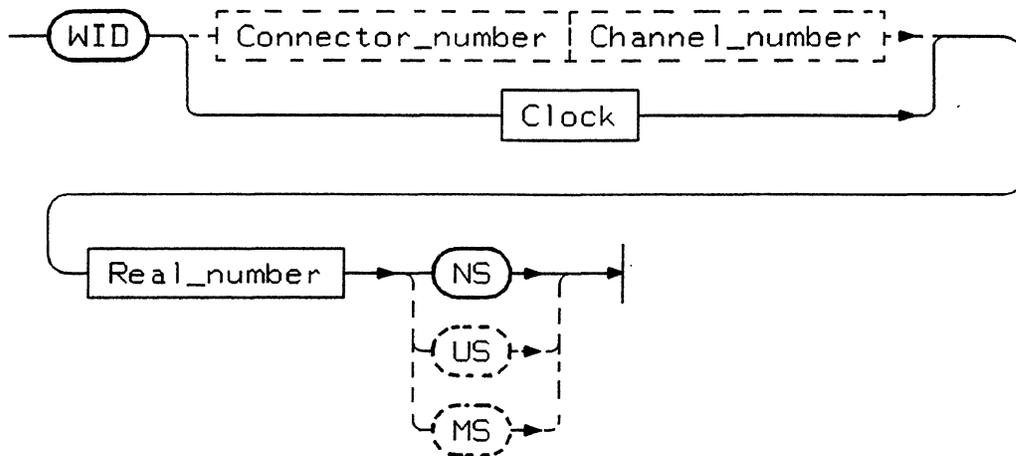


To define a five microsecond delay for connector 2 channel 0, the input line would look like this:

WID 20 5 US

Note that the connector number 2 and the channel number 0 have no delimiting blank between them. This is indicated in the diagram by the envelopes for connector and channel number, touching each other.

If however, you want to define a clock delay of 15 nanoseconds for Clock 2 of the generator, the options you choose from the diagram are shown below:



The input line would look like this:

```
WID C2 15 NS
```

10-3 Addressing the Instruments

When you issue a command to an instrument, you must first address the instrument using the BASIC OUTPUT command. The HP-IB commands are then enclosed in double quotes. You can issue as many HP-IB commands as can fit on one line and each command must be delimited from its neighbour by commas, semicolons, or blanks. Exceptions are the ADS and CAS commands, where the delimiters must be either commas or semicolons.

You can set integer variables to the different HP-IB addresses in the system and choose the variable names to resemble the instrument names. For example:

```
Gen1=707
Output Gen1;"FAD 10 LAD 100 CYM 6 CLK1"
```

When requesting data from an instrument, you use the ENTER command, for example:

```
OUTPUT Gen1;"TLK6"
ENTER Gen1;F$
PRINT F$
```

This example requests any error information from generator 1 about the last command string received. F\$ gives the position in the string of any character causing an error. If these commands were issued following the previous example, then F\$ would have the value 20 because CYM 6 is not a valid command.

These techniques and others are described in Chapters 7 and 8, Generator and Analyzer Programming, respectively.

10-4 HP-IB Commands

The following sections list each of the generator and analyzer pages and functions and the HP-IB commands that relate to each page or function. All the HP-IB commands for the generator and analyzer are listed in the remainder of this chapter.

To find a particular command, refer to the relevant instrument Page or function in this list and then to the alphabetical list of all HP-IB commands.

10-5 Generator

Control Page

BRI	Break Input Slope
CAB	Clock 1 in Break
CLK	Clock Source
FAD	First Address
IMP	Input Impedance
LAD	Last Address
OUT	Outputs On/Off
RUI	Run Input
SPI	Stop Input Slope
STB	Strobe Breaks
STO	Strobe Output
THR	Input Threshold - rear panel inputs

Timing Page

DEL	Channel or Extender Delay
FMT	Format
FRQ	Frequency
PER	Clock Period
WID	Width

Output Page

ADS	Add Data Segment
CAS	Clear and Add Data Segment
COM	Complementary Output
HIL_	High Level
LB_	Channel Label
LIM	Load (Output) Impedance
LOL_	Low Level
NOR_	Normal Polarity
SPO	Strobe Polarity
SSC	Set Standard Configuration
STL	Strobe Level

Data Page

CCD	Clear Channel Data
CLD	Clear Data
CLS	Clear Strobe
COC	Copy Channel
COL	Copy Line
DEC	Address Coding Decimal
DLI	Delete Line
DNC	Down Counter
FOR	Formatted Data
HEX	Address Coding Hexadecimal
ILI	Insert Line
LMA	Limit Address
MOV	Move Line
OCT	Address Coding Octal
PRB	PRBS on Channel
SCD	Set Channel Data
SED	Set All Data
SNE	Strobe No Entry
SSC	Set Standard Configuration
SYE	Strobe Yes Entry
TAD	Top Address
UPC	Up Counter

Store/Recall Page

ASR	Address Set Recall
ASS	Address Set Store
PSR	Parameter Set Recall
PSS	Parameter Set Store
RSS	Recall Standard Set

Macro Data Page

CMA	Copy Macro
CMS	Copy Macros
MAC	Macro Data
SSC	Set Standard Configuration

Remote Message Page

DSP	Display
LIN	Select Line to Display

Menu Select

KEY	Select Page Softkeys
PAG	Select Page
REP	Select Report

Operation Commands

BCK	Manual Clock Back
BRK	Break
FWD	Manual Clock Forward
RUN	Run
SRU	Stop and Run
STP	Stop

Fast Binary Transfer

BSA	Binary Start Address
BSC	Binary Select Connectors
BTR	Binary Transfer

Talker Modes

TLK	Talker Mode
-----	-------------

Special Commands

FSR	Front Panel SRQ
ISR	Incompatibility SRQ Control
MSK	Mask Status Byte
TSA	Transfer Start Address
UPD	Update Status and Address Information

10-6 Analyzer

Control Page

AAD	Autoarming Delay
AGC	Allow Gaps in Count
CKD	Clock Delay
CKP	Clock Period
CKS	Clock Slope
CKT	Clock Threshold
CKW	Clock Width
CQI	Clock Qualifier Input Impedance
CQL	Clock Qualifier Level
CQT	Clock Qualifier Threshold
CYM	Cycle Mode
CYP	Cycling Period
DSG	Display Glitches
OPR	Operating Mode
SPD	Stop Delay
SPE	Stop On Error
SPI	Stop Input Impedance
SPS	Stop Input Active Slope
SPT	Stop Input Threshold
TAI	Trigger Arm Impedance
TAS	Trigger Arm Active Slope
TAT	Trigger Arm Threshold
TQI	Trigger Qualifier Impedance
TQL	Trigger Qualifier Level
TQT	Trigger Qualifier Threshold
TRC	Trigger Count
TRD	Trigger Delay
TWD	Trigger Word

Input Page

ADS	Add Data Segment
C	Connector Threshold Mode
CAS	Clear and Add Data Segment
LBL	Channel Labeling
LO	Low Level
POL	Polarity
SI	Set Analyzer Label - Single Threshold
SSC	Set Standard Configuration
UP	Upper Level

Expected Data Page

CAD	Cursor Address
CBM	Clear Bit Mask
CCD	Clear Channel Data
CCM	Clear Channel Mask
CHD	Channel Data
CLD	Clear Data
COC	Copy Channel
CWM	Clear Word Mask
DAM	Expected Data with Word Mask
DAT	Expected Data without Word Mask
DLI	Delete Line
DRD	Dump Received Data
ILI	Insert Line
RDO	Roll Down Memory
RUP	Roll Up Memory
SBM	Set Bit Mask
SCD	Set Channel Data
SCM	Set Channel Mask
SED	Set Data
SSC	Set Standard Configuration
SWM	Set Word Mask
TAD	Top Address
XCH	Exchange Channels

Miscellaneous Page

RCL	Recall Settings
STO	Store Parameters

State List Page

CAD	Cursor Address
NXE	Next Error
PRE	Previous Error
SSC	Set Standard Configuration
TAD	Top Address

Timing Diagrams Page

CAD	Cursor Address
DSW	Display Window Vertical
HOZ	Horizontal Zoom Factor
NXE	Next Error
PRE	Previous Error
TAD	Top Address
VEZ	Vertical Zoom Factor

Error Map Page

CAD	Cursor Address
CTE	Error Count
DSE	Display Errors
NXE	Next Error
PRE	Previous Error
TAD	Top Address

Remote Message Page

DSP	Display (Messgae)
LIN	Select Line for Display

Menu Select

KEY	Select Page Softkeys
PAG	Select Page
REP	Select Report

Operation Commands

RUN	Run
SPL	Sample
STP	Stop

Fast Binary Transfer

BLI	Binary Listen
BTK	Binary Talk

Talker Modes

SE	Transfer Parameter Set
TLK	Talker Mode
LIN	Select Line to Display

Special Commands

MSK	Mask Status Byte
SYN	Set Synchronizing Character
TSA	Transfer Start Address

10-7 Universal HP-IB Commands

DCL	Device Clear
GET	Group Execute Trigger
GTL	Go to Local
LLO	Local Lockout
SDC	Selected Device Clear
SPD	Serial Poll Disable
SPE	Serial Poll Enable



AAD

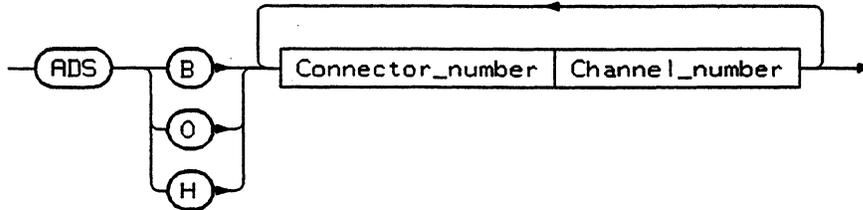
Used to replace analyzer manual RUN key operations. At the end of a data capture cycle, the analyzer is automatically re-armed for the next data capture cycle. If set to either 5, 6, or 7, re-arming is disabled if an error is detected.

- Autoarm_delay** ::= Integer 1 to 7
- | | |
|---------------|---------------------------------|
| 1 = Delay 0s | 5 = Delay 0s (abort on compare) |
| 2 = Delay 1s | 6 = Delay 1s (abort on compare) |
| 3 = Delay 3s | 7 = Delay 3s (abort on compare) |
| 4 = Delay OFF | |

Autoarming Delay

ADS

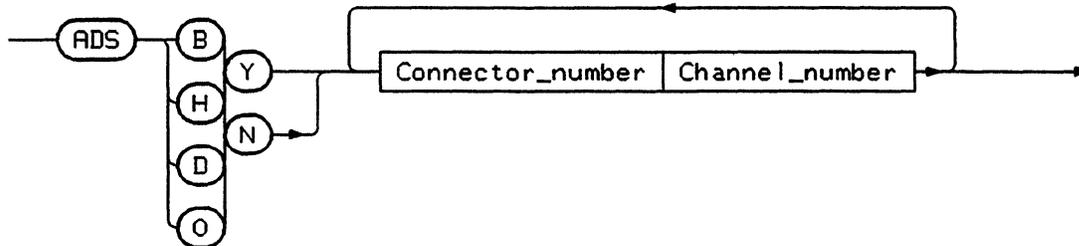
Analyzer



Adds a data segment to the analyzer configuration. Data can be in Binary, Hexadecimal, or Octal form. An ADS statement must be preceded by a CAS statement.

- Connector_number** ::= Hex integer representing the connector number.
Channel_number ::= Integer 0 to 3 representing the channel number for the connector specified.

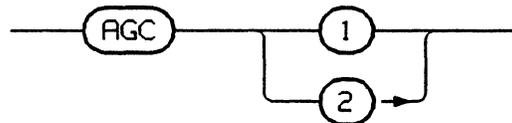
Generator



Adds a data segment to the generator configuration. Data can be in Binary, Hexadecimal, Decimal or Octal form. Entry must be specified (Y or N). An ADS statement must be preceded by a CAS statement.

- Connector_number** ::= Hex integer representing the connector number.
Channel_number ::= Integer 0 to 3 representing the channel number for the connector specified.

Add Data Segment



AGC

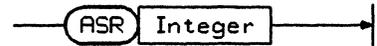
Allows gaps in the trigger word counter.

When set to NO (2) the qualified Trigger Word must occur on consecutive clock pulses, the number of pulses being defined by the Trigger Count Setting. When set to YES (1), the analyzer will be triggered as soon as the Trigger Word has been detected the number of times defined by the Trigger Count Setting.

- 1 = Gaps in count
 2 = No gaps count

Allow Gaps in Count

ASR

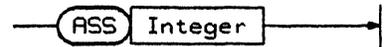


Recalls one of the 9 sets of addresses stored in a generator (see Store/Recall Page).

Integer ≡: An integer value 1 to 9. This corresponds to the nine address sets that can be stored on the Store/Recall page.

Address Set Recall

ASS



Stores the current address settings in one of nine locations in a Generator (see Store/Recall Page)

Integer ≡: An integer value 1 to 9. This corresponds to the nine address locations on the Store/Recall page.

Address Set Store

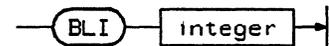
BCK



This command reverses the operation of the generator in manual clocking mode, and feeds the contents of the next lower memory address to the outputs. This has the same function of the BACK key on the front panel.

Manual Clock Back

BLI

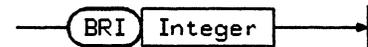


Performs Binary Data Transfer from computer to analyzer. You must define the connectors for data transfer with BSC and the Binary Start Address (BSA) where data is to be downloaded before attempting binary transfer. (This is the inverse of the analyzer binary talk function BTK.) For more details see Section 8-7.

Integer ≡: An integer value 1 to 3.
 1 - Transfers Expected Data (versions A and B)
 2 - Transfers Bit Mask Data (versions A and B)
 3 - Transfers Word Mask Data (version B only)

Binary Listen

BRI



Sets active slope of generator rear panel break input.

Integer ≡: Integer value 1 to 3
 1 - Off - break input has no effect
 2 - On positive slope
 3 - On negative slope

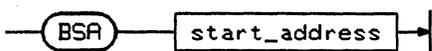
Break Input

BRK



Halts the Generator and sets it in the BREAK state. This command has the same function as the BREAK key on the front panel.

Break



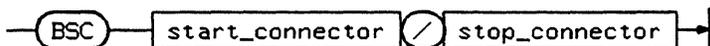
BSA

Sets the start address in the Generator's and Analyzer's memory where the binary data is to be loaded using the Binary Transfer method. You must define the connectors (BSC) where the data is to be loaded before attempting a binary transfer.

Start_address ≡: Integer representing the start address in the generator memory where the data is to be loaded. This is in the range 1 to 1K for A type instruments, and 1 to 16K for B type.

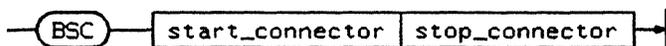
Binary Start Address

Generator



BSC

Analyzer



Sets the channels which the binary data applies to for a Fast Binary Transfer to the generator. You must define the binary start address (BSA) where the data is to be loaded before attempting a binary transfer. For more details see Sections 7-8 and 8-7.

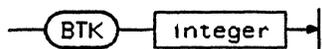
Start_connector ≡: The connector number to which the first binary digits apply.

Stop_connector ≡: The connector number that represents the end of a binary sector. Must be greater than Start_connector.

Example

BSC 0/3 selects connectors 0 to 3. Data to be sent consists of two bytes where byte 1 contains the data for connectors 0 and 1 and byte 2 the data for connectors 3 and 3.

Binary Select Connectors

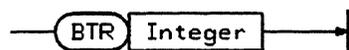


BTK

Performs Binary Data Transfer from analyzer to computer. You must define the connectors for data transfer with BSC and the Binary Start Address (BSA) where data is to be read from before attempting binary transfer. (This is the inverse of the analyzer binary listen function BLL.) For more details see Section 8-7.

Integer ≡: An integer value 1 to 3.
 1 - Transfers Received Data (versions A and B)
 2 - Transfers Expected Data (versions A and B)
 3 - Transfers Bit Mask Data (versions A and B)
 4 - Transfers Word Mask Data (version B only)
 5 - Transfers Error Map Data (version B only)

Binary Talk



BTR

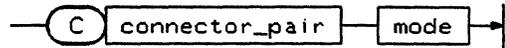
Sets the generator in binary talk mode for the transfer of stimulus or strobe data in binary format. This is the inverse of the binary listen function TLK4. BSA, BTR and BSC must be set before using this command.

Integer ≡: An integer value 1 to 2.
 1 - Fast binary transfer of stimulus data
 2 - Fast binary transfer of strobe data

Binary Transfer

Syntax Diagrams

C



This command is used to set the channel threshold mode configuration of the analyzer. Since dual threshold mode requires two channels for each signal, the connectors are always selected in pairs.

connector_pair := 01 - selects connector pair 0 and 1
 23 - selects connector pair 2 and 3
 45 - selects connector pair 4 and 5
 67 - selects connector pair 6 and 7

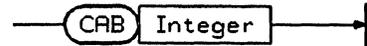
mode := 1 - single threshold mode
 2 - double threshold mode

Example

C01 1 sets connectors 0 and 1 to single threshold mode - eight inputs
C67 2 sets connectors 6 and 7 to double threshold mode - four inputs only

Connector Threshold Mode

CAB

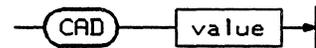


Allows the Clock 1 to remain active during break (while the generators are halted). This is equivalent to the manual operating mode Clock 1 in Break.

Integer := Integer value 1 to 2.
 1 - No clock during break
 2 - Clock during break

Clock 1 in Break

CAD



Used to set the position of the cursor in the Timing Diagram Page of the Analyzer. The maximum values depend on the analyzer operating modes as listed below.

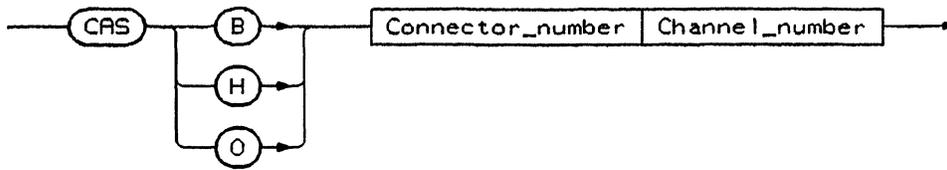
Operating Mode	Range
Trigger Start Analysis with Glitch Detect OFF (OPR1 GLD2)	0000 to +1008 (16368)
Trigger Start Compare (OPR3)	0000 to +1008 (16368)
Trigger Start Analysis with Glitch Detect ON (OPR1 GLD1)	0000 to +0496 (08175)
Trigger Stop Analysis with Glitch Detect OFF (OPR2 GLD2)	-1023 (16383) to -0015
Trigger Stop Analysis with Glitch Detect ON (OPR2 GLD1)	-511 (-8191) to -0015

value := integer

Cursor Address

CAS

Analyzer



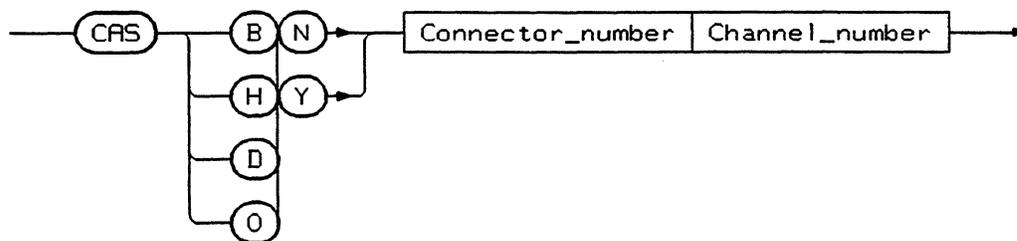
Clears all existing data segments and adds one new segment. Data can be in Binary, Hexadecimal, or Octal form. A CAS statements after an ADS statement clears all the segments programmed in the ADS statement. The command must be delimited with a comma or semi-colon. A maximum of 16 channels can be defined in one segment.

Connector_number := Hex integer representing the connector number.
Channel_number := Integer 0 to 3 representing the channel number for the connector specified.

Example

CAS B 13 12 11 10 33 32 31 30; creates a new segment comprising all the channels of connectors 1 and 3. Data entry to this segment will be in binary.

Generator



Clears all existing data segments and adds one new segment. Data can be in Binary, Hexadecimal, Decimal or Octal form. Entry must be specified (Y or N). A CAS statements after an ADS statement clears all the segments programmed in the ADS statement. The command must be delimited with a comma or semi-colon. A maximum of 16 channels can be defined in one segment.

Connector_number := Hex integer representing the connector number.
Channel_number := Integer 0 to 3 representing the channel number for the connector specified.

Example

CAS BY C3 C2 C1 C0 B3 B2 B1 B0; creates a new segment comprising all the channels of connectors B and C. Data entry to this segment will be in binary.

Clear and Add Data Segment



CBM

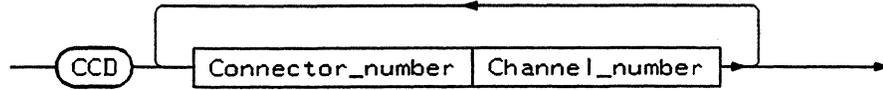
Clears all bit masks in the expected data memory of the Analyzer.

Clear Bit Mask

CCD

Clears the data (set to zero) from the specified connector and channel.

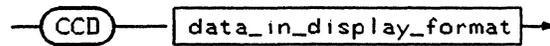
Generator



Data is cleared only between the first and last addresses.

Connector_number := Hex integer representing the connector number.
Channel_number := Integer 0 to 3 representing the channel number for the connector specified.

Analyzer



Clears the data in all addresses of the Analyzer. Data must be entered in the same format as the current channel configuration, that is, the number of channels in each segment and the number of segments. For more information refer to Section 8-6 of the Operating and Programming Manual.

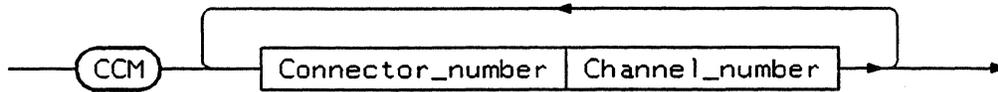
Data 1 := Set data to 1
 - := Retain current value

Example

CCD 11-- 1-1- ---- 1111 sets the data in channels 1, 2, 5, 7, 13 to 16 (as displayed in the Expected Data Page) to 1.

Clear Channel Data

CCM



Clears the channel mask at all addresses of the Analyzer. Data must be entered in the same format as the current channel configuration, that is, the number of channels in each segment and the number of segments. For more information refer to Section 8-6 of the Operating and Programming Manual.

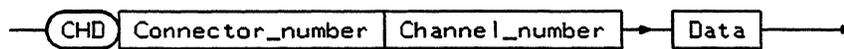
Data := 1 Clear Mask
 - Retain current value

Example

CCD 11-- 1-1- ---- 1111 clears the mask in channels 1, 2, 5, 7, 13 to 16 (as displayed in the Expected Data Page) to 1.

Clear Channel Mask

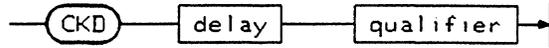
CHD



Sets one bit of data in the generator at the current address set by TSA. Data can be either 1 or 0. If more data is present TSA will be incremented after each bit of data so that data will be set at further addresses.

Channel Data

Syntax Diagrams



CKD

Sets the analyzer clock delay. This must be set between 0 nanosecond and 1 second.

delay ::= a real value

Qualifier ::= one of S, MS, US, or NS

Analyzer Clock Delay

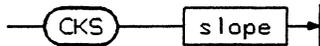


CKP

Sets the internal clock period of the analyzer.

Period ::= an integer 1, 2 or 5 followed by one of MS, US, or NS

Clock Period

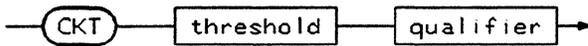


CKS

Sets the analyzer clock slope.

slope ::= 1 - Positive
2 - Negative
3 - Both

Analyzer Clock Slope



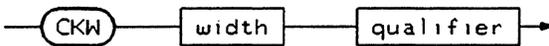
CKT

Sets the analyzer clock threshold level in the range -10 V to +10 V.

threshold ::= real number

qualifier ::= one of V or MV

Analyzer Clock Threshold



CKW

Sets the analyzer clock width. This must be set between 10 nanosecond and 1 second.

width ::= real number

qualifier ::= one of NS, US, MS

Analyzer Clock Width

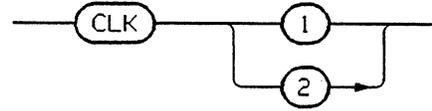
CLD



Sets all the data of a Generator and the expected data of an Analyzer to 0 and clears any bit masks previously set.

Clear Data

CLK

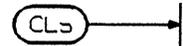


Sets the clock source for the generator and analyzer.

Digit	Generator Setting	Analyzer Setting
1	Internal	External
2	External - rising edge	Internal
3	External - falling edge	
4	Manual	

Clock Source

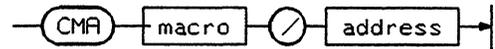
CLS



Sets all the data in the strobe channel of the Generator to zero.

Clear Strobe

CMA



Copies a single macro from the Macro Data Page to the specified address in the generator data memory.

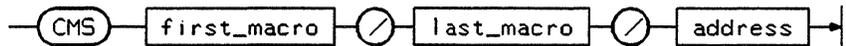
macro := Hex number of macro
address := Address (0 to 16383 (1023))

Example

CMA D/257 copies the macro in line D to address 257.

Copy Macro

CMS



Copies a group of macros from the Macro Data Page to the generator data memory. The address specified address is taken as the start address of the group and any existing data at those addresses will be overwritten by the macro data.

macro := Hex number of macro
address := Address (0 to 16383 (1023)) in current address format (hex, octal, binary, decimal)

Example

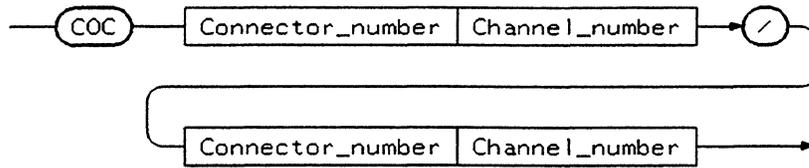
CMA 1/7/257 copies the macros in lines 1 to 7 to addresses 257 to 265 decimal if decimal addressing has already been specified.

Copy Macros

COC

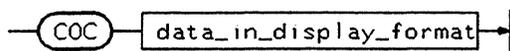
Copies a single channel of data in the Generator and Analyzer. The format used is different for each instrument.

Generator



The command COC 32 22 copies the complete data set of channel 32 to channel 22.

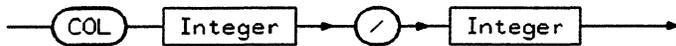
Analyzer



- 1 := Source channel
- 2 := Target channel
- := Unchanged channels

The data input must be in the same format as displayed on the expected data page (channel configuration and organization). The command COC --- 1--- ---2- --- --- copies the complete data set in the channel displayed fifth from the left to the 15th displayed channel.

Copy Channel

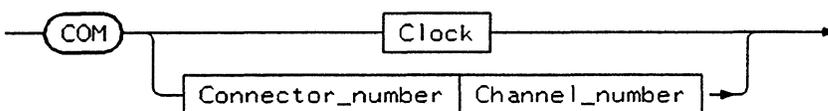


COL

Copies the vector of generator data at one address to another (second) address and overwrites the previous values at the second address.

For 'A' type instruments, integer must be between 0 and 1023 and, for 'B' type instruments 0 and 16383

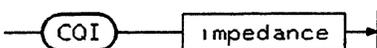
Copy Line



COM

Sets the output of the channel specified to complementary polarity. For clocks, the inputs 1C and 2C refer to Clock 1 and Clock 2 respectively.

Complementary Polarity



CQI

Sets the input impedance for the analyzer clock qualifier input.

- impedance := 1 - 50 Ohm
- := 2 - 100 kOhm

Clock Qualifier Input Impedance

CQL

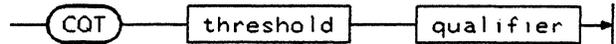


Sets the active level for the analyzer clock qualifier.

level := 1 - High
 2 - Low
 3 - Don't care

Clock Qualifier Level

CQT

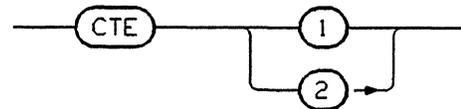


Sets the voltage threshold for the analyzer clock qualifier in the range between +10 V and -10 V.

range := real number
qualifier := One of V or MV

Clock Qualifier Threshold

CTE

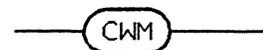


This analyzer command switches the Error count feature on and off.

1 := Error counter on and current value of error count displayed
2 := Error counter off

Error Count

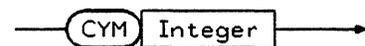
CWM



This Analyzer command clears the word mask for all vectors.

Clear Word Mask

CYM

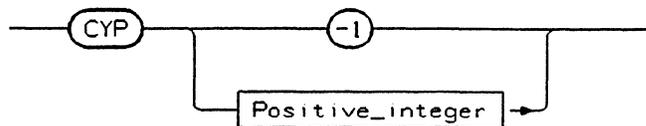


Sets the cycle mode of the generator.

Integer := Integer value between 1 and 5.
 1 - Auto
 2 - Single
 3 - Gated
 4 - Initialized and Gated
 5 - Initialized and Auto

Cycle Mode

Syntax Diagrams

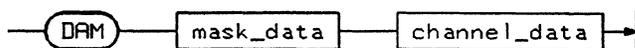


CYP

Sets the cycling period of the Analyzer when it is being used in real-time compare mode. Refer to Section 4-11 of the Operating and Programming Manual for more information.

-1 := Switches cycling period off.
Positive_integer := Integer between 2 and 1024 (A' type) or 2 and 16384 (B' type) to set the cycling period.

Cycling Period



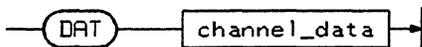
DAM

Used to input data at the current address defined by TSA in the Expected Data Page of the Analyzer. Data input must be in the same format as the Expected Data display (channel configuration and number). This command has the same effect as DAT with mask data inputs.

Mask_data := . - word mask not set
 X - word mask set

Channel_data := 0 - set data to 0
 1 - set data to 1
 X - mask data

Expected Data with Word Mask



DAT

Used to input data at the current address defined by TSA in the Expected Data Page of the Analyzer. Data input must be in the same format as the Expected Data display (channel configuration and number). This command has the same effect as DAM without mask data inputs.

Channel_data := 0 - set data to 0
 1 - set data to 1
 X - mask data

Expected Data without Word Mask

DCL

Universal HP-IB command used with the BASIC 'SEND' command to stop instruments connected to the same interface on the bus. It has the same effect as pressing the STOP key. Refer to the BASIC Language Reference Manual for more information.

Device Clear

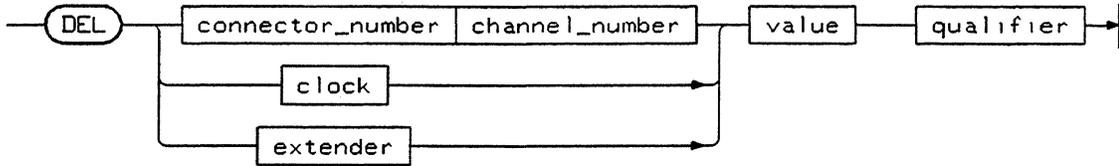
DEC



Sets the address display of the generator to decimal. See also HEX and OCT which are used to set the address format to hexadecimal and octal respectively.

Address Coding Decimal

DEL

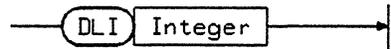


Sets the delay of a clock, channel or extender with respect to the generator internal clock.

- connector_number** := the connector number of the signal to be delayed
- channel** := the channel in connector to be delayed
- clock** := 1C, 2C - Clock 1 and Clock 2 respectively
- extender** := X1, X2 - Extender 1 and Extender 2 respectively

Channel or Extender Delay

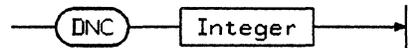
DLI



Deletes one line of data in the Generator and Analyzer. All lines below the deleted line move up one position and the last line is filled with zeros.

Delete Line

DNC



Sets the generator data in the segment specified to a down counter. The displayed segments (data page) are numbered from the left, the first segment having segment number 1.

Down Counter

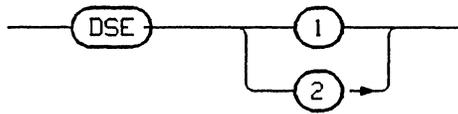
DRD



This analyzer command copies the data stored in the received data memory into the expected data memory.

Dump Received Data

Syntax Diagrams

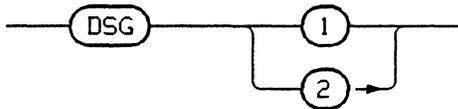


DSE

This command specifies whether the analyzer is to display errors or not.

- 1 ::= Errors displayed
- 2 ::= Errors not displayed

Display Errors

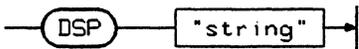


DSG

This command switches the Analyzer Display Glitches feature on and off. The Glitch Detect feature must be enabled (see GLD) before this command can be used.

- 1 ::= Display Glitches on
- 2 ::= Display Glitches off

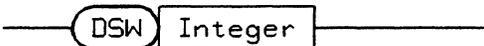
Display Glitches



DSP

This command displays text in the Remote Message Page of the generators and analyzers at the current line defined by the LIN command. After each DSP command, LIN will be incremented.

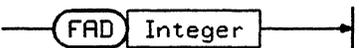
Display



DSW

This analyzer command vertically scrolls the Timing Diagrams Page. The integer number following DSW marks the right bottom of the vertical window and must be greater than zero and less 40.

Display Window Vertical



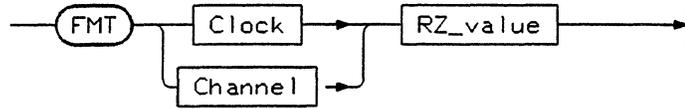
FAD

Sets the generator first address for cycling.

- integer ::= for 'A' type instruments 0 to 1022
- for 'B' type instruments 0 to 16382

Set First Address

FMT

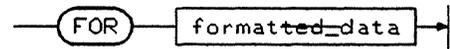


Sets the format of generator clock and channel data for signals with RZ capability.

- Clock** := 1C or 2C for Clock 1 and Clock 2 respectively
- channel** := the hex connector number followed by the channel number (0 to 3) to be set
- rz_value** := 1 - RZ format
 2 - RZ=50% format
 3 - NRZ format (not for clocks)

Format

FOR



Sends a formatted vector with strobe to the generator. The data must be in the same format as the current channel configuration and segment code with no NO ENTRY segments. The FOR statement must be delimited by a comma, period or CR/LF. After the delimiter is read, TSA will be incremented ready for the next FOR statement.

- data** := 0 - sets the bit to zero
 1 - sets the bit to one
 - - leaves the bit in its previous state

Example

FOR 0 0000 1111 -1-1 1010 sets the strobe to 0 and the four defined segments to the states shown at the current address set by TSA.

Formatted Data

FRQ

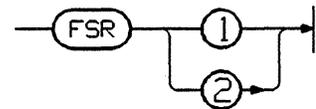


Sets the Generator clock frequency and will also change the period setting (PER).

- value** := real number
- qualifier** := one of HZ, KHZ, or MHZ

Frequency

FSR



Enables and disables operation of the generator front panel SRQ control.

- 1 := Enabled
- 2 := Disabled

Front Panel SRQ

Syntax Diagrams



FWD

When the generator is in manual clock mode, it is clocked one cycle each time this command is received. This command has the same effect as the FWD key on the front panel.

Manual Clock Forward

GET

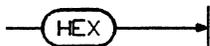
This is a universal HP-IB command used with the BASIC SEND command. It has the effect of starting the instruments on the bus. Refer to the BASIC Language Reference Manual for more information.

Group Execute Trigger

GTL

This is a universal HP-IB command used with the BASIC SEND command. It has the effect of setting the selected device to LOCAL mode. Refer to the BASIC Language Reference Manual for more information.

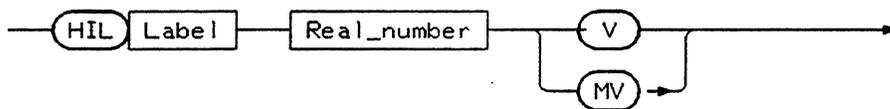
Go to Local



HEX

Sets the address display of the generator to hexadecimal. See also DEC and OCT which are used to set the address format to decimal and octal respectively.

Hexadecimal Address Coding



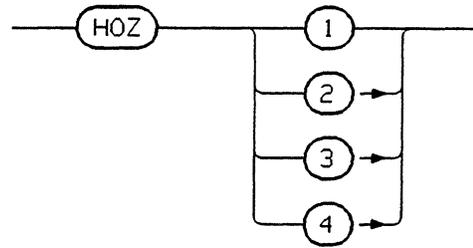
HIL

Sets a value for each of the generator output high level labels.

label := A, B, C, or D

High Level

HOZ

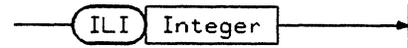


Sets the zoom factor of the analyzer timing diagram page. It has the same effect as the relevant softkeys in this page.

Number Input	Zoom Factor
1	1
2	2
3	4
4	8

Horizontal Zoom Factor

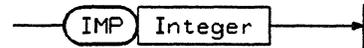
ILI



Inserts a new line of data at the position specified in the generator data page and analyzer expected data page. All lines following the inserted line will be moved downwards and the last line 1023 or 16383 will be deleted.

Insert Line

IMP

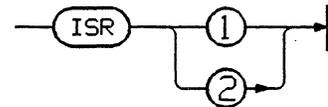


Sets the input impedance of the generator rear panel inputs. The input impedance can be set to 50 Ohm or 100 kOhm

1	:=	50 Ohm
2	:=	100 kOhm

Input Impedance

ISR

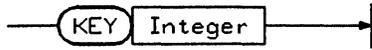


Enables and disables generation of an SRQ by the generator in the case of incompatibility of timing or level settings.

1	:=	Enable SRQ 13 and 14 and set SRQ if error detected
2	:=	Disable SRQ 13 and 14

Incompatibility SRQ Control

Syntax Diagrams

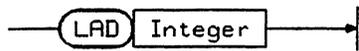


KEY

Selects the softkeys corresponding to the page specified by integer without changing the report display after returning to local control.

			Analyzer	Generator
integer	:=	1	Control Page	Control Page
		2	Input Page	Timing Page
		3	Expected Data Page	Output Page
		4	Miscellaneous Page	Data Page
		5	State List Page	Store/Recall Page
		6	Timing Diagrams Page	Miscellaneous Page
		7	Error Map Page	Macro Data Page

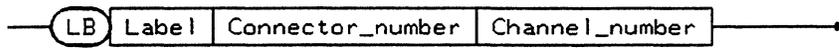
Select Page Softkeys



LAD

Sets the last address of the generator to be used in the various cycle modes. The last address set must be higher than the first address. For 'A' types last address must be between 2 and 1024 and for 'B' types between 2 and 16384.

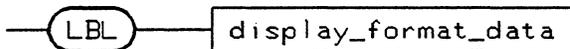
Last Address



LB

Used to set the voltage levels of the generator output channel specified to the levels defined by labels A to D. For clock signals you should use 1C and 2C for Clock 1 and Clock 2 instead of connector and channel number.

Channel Label



LBL

Used to set the voltage levels of the analyzer data input channels. The data must be input in the same format as the current channel configuration.

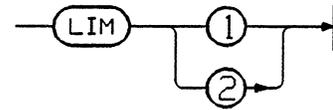
level := A, B, C, D, E or F to set the channel to these levels respectively.
 - to leave the channel in its previous state

Example

LBL AAAA BBCC ---A BBBB

Channel Labeling

LIM

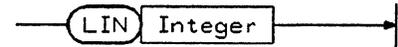


Sets the load (output) impedance of the generator data outputs. Refer to Chapter 3 of the Operating and Programming Manual for more information on output impedance.

integer := 1 - 50 Ohm
 2 - Open (high impedance)

Load Impedance

LIN



Selects the line (1 to 26) in which the string entered by a DSP command will be displayed on the Remote Message Page of the generator and analyzer and selects the line to be output by the instrument in talker mode 3 - display dump. The line number is incremented after every DSP or TLK3 command entered. LIN is set to 1 at power-up.

Select Line to Display

LLO

This is a universal HP-IB command used with the BASIC SEND command. It has the effect of setting the selected device to REMOTE mode and disabling front panel key operation. Refer to the BASIC Language Reference Manual for more information.

Local Lockout

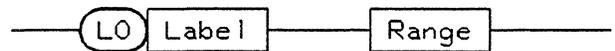
LMA



Sets a limit address in the generator above which existing data is safeguarded for insert and copy line functions. Any insert and copy procedures will affect data up to the limit address but will be ignored if they try to modify data after the limit address.

Limit Address

LO

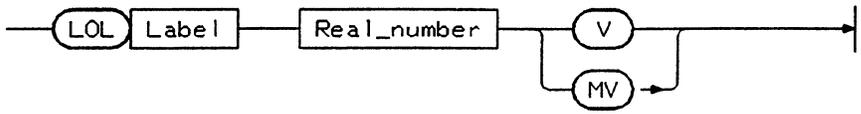


Sets the analyzer lower voltage threshold for the label specified (A to F) in dual threshold compare mode. This value must be in the range -10.0 V to +9.90 V.

value := real number
qualifier := One of V or MV

Low Level

Syntax Diagrams

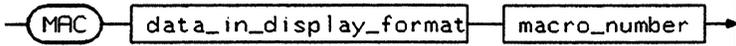


LOL

Sets the voltage of the generator low level output for the specified label.

Label ::= A, B, C, or D

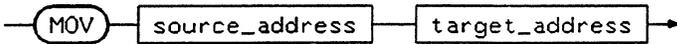
Low Level



MAC

Used to input macro data in the generator Macro Data Page. Data must be input in the same format and configuration as the display. The MAC command must be followed by a hex digit indicating the address of the data to be input.

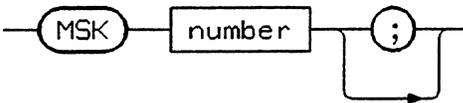
Macro Data



MOV

Moves the vector of data from one address to another address in the generator.

Move Line



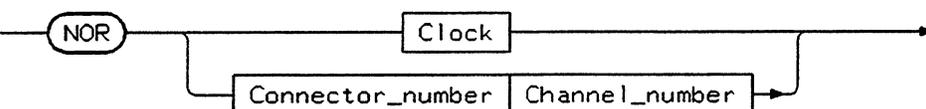
MSK

This analyzer command allows you to set the mask register of the specified output so that bits 0 to 5 in the status byte are masked (do not cause SRQ to be sent). The number output is the sum of the values of the bits which are to be used to set the mask register. The default at power up or after changes to the IIP-IB address is 63. The values are listed below:

Bit Position	Bit Weight	Meaning
6	64	Request Bit - set if any other bits set
5	32	Error Bit - set if fast clock detected
4	16	Ready Bit - set if STOP routine detected
3	8	Front Panel SRQ Bit - set if the SRQ key has been set
2	4	Autocorrect Bit - set if an autocorrection has been performed
1	2	Wrong Value Bit - set if an illegal value setting has been attempted
0	1	Wrong Statement Bit - set if an unrecognized or unallowed statement has been interpreted

number ::= integer between 0 and 63

Mask Status Byte



NOR

Sets the output of the generator channel specified to normal polarity. For clocks, the inputs 1C and 2C refer to Clock 1 and Clock 2 respectively.

Normal Polarity

NXE



Moves the cursor (top address) on the analysis display pages (State List, Timing Diagram, and Error Map) and the expected data page to the next address where an error has been detected. When the last error has been displayed, the cursor moves to the last address.

Next Error

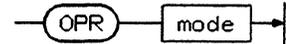
OCT



Sets generator address coding to octal. This can also be set to decimal or hexa-decimal by using the DEC and HEX commands respectively.

Octal Address Coding

OPR

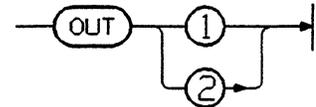


Sets the analyzer operating mode.

mode := 1 - Trigger start analysis
 2 - Trigger stop analysis
 3 - Trigger start compare

Analyzer Operating Mode

OUT

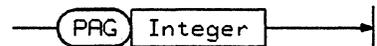


Used to switch the generator outputs on and off.

1 := Outputs off
 2 := Outputs on

Outputs

PAG

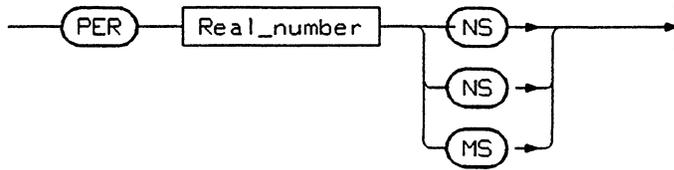


Selects the pages of the analyzer and generator.

		Analyzer	Generator
value	:=	1 Control Page	Control Page
		2 Input Page	Timing Page
		3 Expected Data Page	Output Page
		4 Miscellaneous Page	Data Page
		5 State List Page	Store/Recall Page
		6 Timing Diagrams Page	Miscellaneous Page
		7 Error Map Page	Macro Data Page

Select Page

Syntax Diagrams

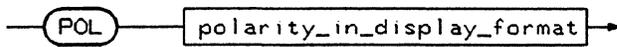


PER

Sets the Generator clock period and will also change the frequency setting (FRQ). The setting must be in the range 20.0 ns to 999 ms.

Number := real number
qualifier := one of NS, US, or MS

Clock Period

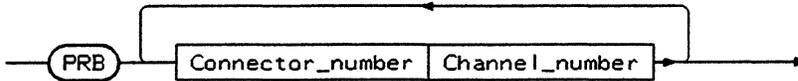


POL

Sets the polarity of the analyzer expected data inputs. The polarity data must be in the same order and format as that displayed in the expected data page, that is, the number of segments and number of channels in each segment must agree with the current channel configuration.

polarity := N sets input to normal polarity
 I sets input to inverse polarity
 - leave channel in current polarity

Polarity



PRB

Sets the generator data in the channel specified to a pseudo-random binary sequence.

PRBS on Channel



PRE

Moves the cursor (top address) on the analysis display pages (State List, Timing Diagrams, and Error Map) and the expected data page to the previous address where an error has been detected. When the first error has been displayed, the cursor moves to the first address.

Previous Error

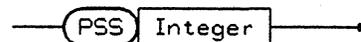


PSR

Recalls the generator parameter set specified (1 to 3) and makes it the current setting. These settings should have been previously stored using the PSS command.

Parameter Set Recall

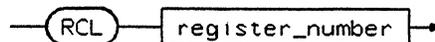
PSS



Stores the current generator settings into one of the three parameter sets (1 to 3) for later use by the PSR command.

Parameter Set Store

RCL



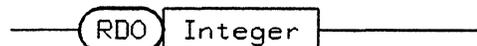
Analyzer

This command recalls the settings previously stored using the STO command. When no settings have been previously stored, RCL causes a service request.

register_number	1 2 3	:=	recall the settings in registers 1,2, or 3 respectively
	4	:=	recalls the standard set. Refer to the Operating and Programming Manual for a complete list of these settings.

Recall Settings

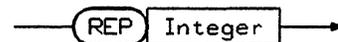
RDO



Rolls the contents of the analyzer memory downwards with respect to the address.

Roll Down Memory

REP



Selects the specified Report Page of the generator or analyzer. This is similar to the command PAG except that the softkeys from the previous page will remain active returning to local.

		Generator	Analyzer
integer	:=	1 Control Page	Control Page
		2 Timing Page	Input Page
		3 Output Page	Expected Data Page
		4 Data Page	Miscellaneous Page
		5 Store/Recall Page	State List Page
		6 Miscellaneous Page	Timing Diagrams Page
		7 Macro Data Page	Error Map Page
		8 Remote Message Page	Remote Message Page

Select Page

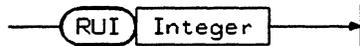
RSS



Recalls the generator standard set. For more details of the settings refer to the Operating and Programming Manual.

Recall Standard Set

Syntax Diagrams



RUI

Sets the generator rear panel RUN INPUT active edge.

1	:=	Off
2	:=	Positive Slope
3	:=	Negative Slope

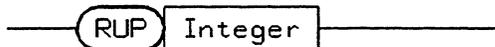
Run Input



RUN

Has the same effect as pressing the RUN key on the generator or analyzer front panel.

Run



RUP

Rolls the contents of the analyzer memory upwards with respect to the addresses.

Roll Up Memory



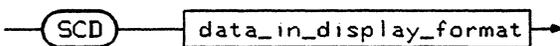
SBM

Sets all bit masks in the expected data memory of the Analyzer. This is only possible in Trigger Start and Trigger Stop Analysis Modes.

Set Bit Mask

SCD

Analyzer



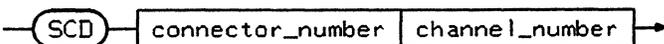
Sets the data at all addresses of the Analyzer to 1. Data must be entered in the same format as the current channel configuration, that is, the number of channels in each segment and the number of segments. For more information refer to Section 8-6 of the Operating and Programming Manual. See also CCD to set data to 0.

Data	:=	1	Set data to 1
		-	Retain current value

Example

SCD 11-- 1-1- ---- 1111 Sets the data mask in channels 1, 2, 5, 7, 13 to 16 (as displayed in the Expected Data Page) to 1.

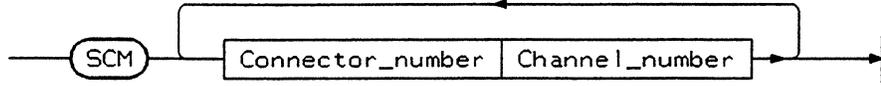
Generator



Sets the data of the specified connector and channel to one. Data is only changed between the first and last addresses.

Set Channel Data

SCM



Sets the channel mask at all addresses of the Analyzer. Data must be entered in the same format as the current channel configuration, that is, the number of channels in each segment and the number of segments. For more information refer to Section 8-6 of the Operating and Programming Manual.

Data := 1 Set Mask
 - Retain current value

Example

SCM 11-- 1-1- ---- 1111 sets the mask in channels 1, 2, 5, 7, 13 to 16 (as displayed in the Expected Data Page) to 1.

Set Channel Mask

SDC

This is a universal IIP-IB command used with the BASIC SEND command. Refer to the BASIC Language Reference Manual for more information. This has the same effect as the STOP command on the addressed instrument but makes use of the synchronize buffer.

Selected Device Clear

SE_



This command is used to restore an analyzer parameter set previously saved to a mass storage device with the TLK 2 command. The data read by the analyzer using the BASIC ENTER command can be stored in locations 1 to 3. See Chapter 8 of the Operating and Programming Manual for more information.

Transfer Parameter Set

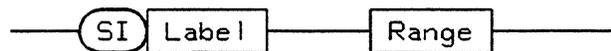
SED



Sets all the data of a Generator and the expected data of an Analyzer to 1.

Set Data

SI_



Sets the single threshold voltage input level for the analyzer voltage labels A to F. This must be in the range +10 V to -10 V.

label := One of A, B, C, D, E, or F
 value := real number followed by one of V or MV

Set Analyzer Label - single threshold

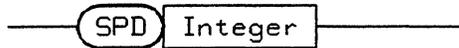
Syntax Diagrams



SNE

Used to disable data entry in the strobe channel of the generator.

Strobe No Entry



SPD

Sets the internal stop delay of the analyzer which causes the analyzer to stop and terminate data capture (go into idle state) after the number of clock periods specified by integer. This feature must be enabled with the SPS command.

integer ≡ 0 to 16383 (1023)

Stop Delay

SPD

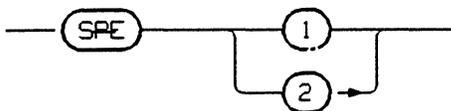
HP-IB Universal command used with the SEND command. Refer to the BASIC Language Reference Manual for more information.

Serial Poll Disable

SPE

HP-IB Universal command used with the SEND command. Refer to the BASIC Language Reference Manual for more information.

Serial Poll Enable

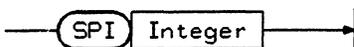


SPE

Enables or disables the stop-on-error feature of the analyzer when it is being used in Trigger Start Compare Mode. This command has no effect when the the analyzer is in other operating modes.

1 ≡ On
2 ≡ Off

Stop On Error



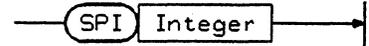
SPI

This command sets the impedance of the analyzer stop input.

1 ≡ 50 Ohm
2 ≡ 100 kOhm

Stop Input Impedance

SPI

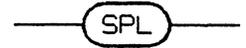


Sets the active slope of the generator rear panel STOP input.

- | | | |
|---|---|----------------|
| 1 | ≡ | Off |
| 2 | ≡ | Positive Slope |
| 3 | ≡ | Negative Slope |

Stop Input Slope

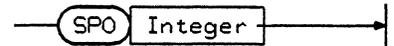
SPL



Has the same effect as pressing the SAMPLE key on the analyzer.

Sample

SPO

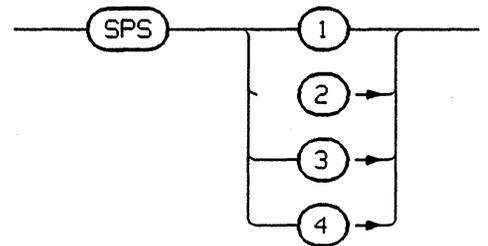


Sets the generator strobe output polarity to normal or complement.

- | | | |
|---|---|-------------------|
| 1 | ≡ | Normal output |
| 2 | ≡ | Complement output |

Strobe Polarity

SPS

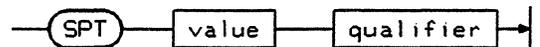


Sets the active slope of the analyzer rear panel stop input.

- | | | |
|---|---|------------|
| 1 | ≡ | Positive |
| 2 | ≡ | Negative |
| 3 | ≡ | Internal |
| 4 | ≡ | Not active |

Stop Active Slope

SPT



Sets the voltage threshold of the analyzer stop input. This must be in the range +10 V to -10 V.

value ≡ real number

qualifier ≡ one of V or MV

Stop Threshold

Syntax Diagrams



SRU

Stops the generator, sets the address to FAD and restarts the generator. In INIT PLUS AUTO mode the address is set to 00000 before restarting.

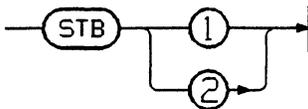
Stop and Run



SSC

Sets the generator and analyzer to a default standard condition. Refer to the Operating and Programming manual for more information.

Set Standard Configuration

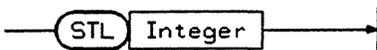


STB

Used to switch the generator Strobe Break feature on and off.

1	≡	Off
2	≡	On

Strobe Breaks

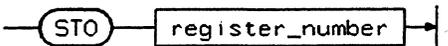


STL

Sets the generator strobe output level to either ECL or TTL levels.

1	≡	TTL
2	≡	ECL

Strobe Level



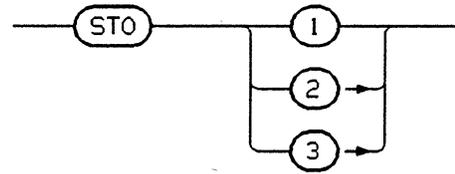
STO

Analyzer

This command stores the active settings of all outputs in one of the analyzer setting registers (1 to 3).

Store Parameters

STO



Used to set the format of the generator strobe output signal to either clock (pulse output) or data (NRZ format).

- 1 := Data
- 2 := Clock

Strobe Output

STP



Has the same effect as pressing the STOP key on the generator and analyzer.

Stop

SWM



Sets the word mask in the analyzer.

Set Word Mask

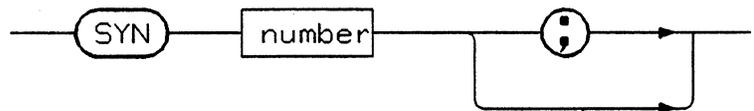
SYE



Enables data entry in the generator strobe channel.

Strobe Yes Entry

SYN



Used to set a new analyzer synchronizing character on the HP-IB. The default synchronizing character 13 (CR) is set at power on and after changing the HP-IB switch settings.

- number := ASCII character number of the new synchronize character. This can be any ASCII character except 'A..Z', 'a..z', '0..9', '-', '@', '*', or '?.

Set Synchronizing Character



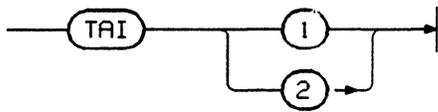
TAD

Sets the top address for data. For the generator this can be between 0 and 16383 (1023). For the analyzer, the maximum value depends on the operating mode as listed below.

Operating Mode	Range
Trigger Start Analysis with Glitch Detect OFF (OPR1 GLD2)	0000 to +1023 (16383)
Trigger Start Compare (OPR3)	0000 to +1023 (16383)
Trigger Start Analysis with Glitch Detect ON (OPR1 GLD1)	0000 to +0511 (08191)
Trigger Stop Analysis with Glitch Detect OFF (OPR2 GLD2)	-1023 (16383) to 0
Trigger Stop Analysis with Glitch Detect ON (OPR2 GLD1)	-511 (-8191) to 0

address ::= integer

Top Address

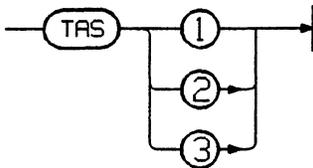


TAI

Sets the impedance of the analyzer trigger arm input.

1 ::= 50 Ohm
2 ::= 100 kOhm

Trigger Arm Impedance

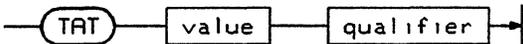


TAS

Used to set the slope of the signal appearing at the TRG ARM input that sets the analyzer to the ARMED state.

1 ::= POSITIVE
2 ::= NEGATIVE
3 ::= DON'T CARE

Trigger Arm Active Slope



TAT

Sets the threshold of the analyzer trigger arm input. This value must be in the range +10 V to -10 V.

range ::= real number

qualifier ::= V or MV

Trigger Arm Threshold

THR

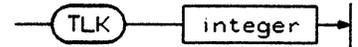


Sets the input voltage threshold of the generator rear panel inputs. The value must be in the range -10 V to +10 V.

- value** :=: real number
- qualifier** :=: One of V or MV

Input Threshold

TLK



Analyzer

Used to set one of the analyzer talker modes (1 to 8). Data output in each talker mode is listed below. For more information on the different talker modes, refer to Chapter 8 of the Operating and Programming Manual. For talker modes 4 to 7, TSA should be set before this command is used.

- value** :=: 1 Returns status information
- 2 Learn Mode - Outputs the current parameter settings for storage on a mass storage device. This data cannot be read by the user but can be reloaded to the analyzer using the SE_ command.
- 3 Display Dump
- 4 Expected Data
- 5 Captured Data
- 6 Errors/Glitches from State List
- 7 Error Map
- 8 Channel Marking
- 9 Analyzer Servicing (8182B only)
- A Combination of TLK5 and TLK6 (8182B only)
- B As TLKA, but only vectors containing errors (8182B only)

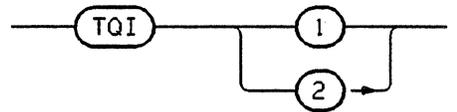
Generator

Used to set one of the generator talker modes (1 to 6). Data input/output in each talker mode is listed below. For more information on the different talker modes, refer to Chapter 7 of the Operating and Programming Manual.

- value** :=: 1 Returns status information
- 2 Learn Mode - as above, reloading the data is performed using the BASIC OUTPUT command.
- 3 Display Information - line to be output can be set with the LIN command
- 4 Formatted Data
- 5 Data Page Format
- 6 Error String

Talker Modes

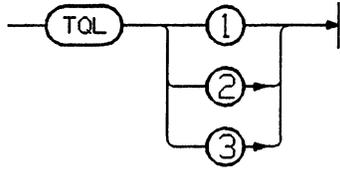
TQI



Sets the input impedance of the analyzer trigger qualifier input.

- 1 :=: 50 Ohm
- 2 :=: 100 kOhm

Trigger Qualifier Impedance

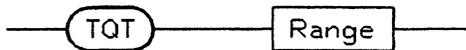


TQL

Sets the active level of the analyzer trigger qualifier input.

level := 1 - Active level high
 2 - Active level low
 3 - Don't care

Trigger Qualifier Level

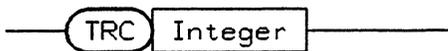


TQT

Sets the voltage threshold of the analyzer trigger qualifier input. This value must be between +10 V and -10 V.

value := real number followed by one of V or MV

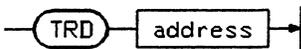
Trigger Qualifier Threshold



TRC

Sets the number of times (1 to 16) the analyzer must be triggered before it goes into the active state. Whether the analyzer goes directly into the active state is determined by the TRD setting. See TRD.

Trigger Count



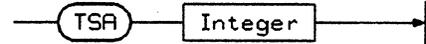
TRD

Sets the delay (in addresses) between the analyzer being triggered and entering the active state. The range of addresses that can be programmed is 0 to 66535 (1023). See TRC.

Note: When in Trigger Start Compare Mode, the range is 00001 to 66535. Attempting to program TRD 0 will cause a service request.

Trigger Delay

TSA



Analyzer

Sets the start address for data transfers to and from the analyzer. The default value is TSA DISABLED, so this command must be used to set TSA the first time the analyzer is addressed to talk in talker modes 4, 5, 6, or 7 or if the Expected Data has been modified using DAT or DAM. The default is set after power on, altering the HP-IB address switch setting, RCL, OPR or GLD settings. The allowable range for TSA depends on the operating mode as listed below.

If TSA is disabled, TLK 4, 5, 6, and 7 return empty strings.

If TSA is enabled, it will be incremented within its allowed range each time a string is entered in talker modes 4, 5, 6, or DAT or DAM are used.

After a talker mode 7 command, it will be incremented to the next multiple of 64 minus 1 ($TSA \rightarrow (TSA - (TSA \text{ modulo } 64) + 63)$). Refer to Chapter 8 of the Operating and Programming Manual.

Operating Mode	Range
Trigger Start Analysis with Glitch Detect OFF (OPR1 GLD2)	0000 to +1023 (16383)
Trigger Start Compare (OPR3)	0000 to +1023 (16383)
Trigger Start Analysis with Glitch Detect ON (OPR1 GLD1)	0000 to +0511 (08191)
Trigger Stop Analysis with Glitch Detect OFF (OPR2 GLD2)	-1023 (-16383) to 0
Trigger Stop Analysis with Glitch Detect ON (OPR2 GLD1)	-511 (-8191) to 0

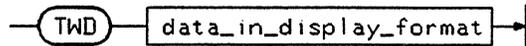
Generator

Sets the start address for data transfers to and from the generator. The default value is TSA DISABLED, so this command must be used to set TSA the first time the generator is addressed for a data transfer. The set address must be in the range 0 to 1023 (16383).

value := integer (for the generator the entry must correspond to the selected address format (DEC, HEX, or OCT))

Transfer Start Address

TWD

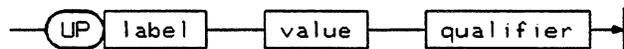


Sets the trigger word that is to be used to trigger the analyzer. The format of the data must be agree with the current channel configuration, that is, the number of segments and the organization of the segments.

Data can be set to 0, 1 and X, where X is a don't care condition. If the trigger consists of all X's, the trigger word is not used to trigger the analyzer - it triggers on every word in the absence of any other trigger conditions.

Trigger Word

UP



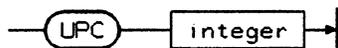
Sets the analyzer upper voltage threshold for the label specified (A to F) in dual threshold compare mode. This value must be in the range -9.90 V to +10.0 V.

value := real number

qualifier := One of V or MV

Upper Level

Syntax Diagrams



UPC

Sets the generator data in the segment specified to an up counter. The displayed segments (data page) are numbered from the left, the first segment having segment number 1.

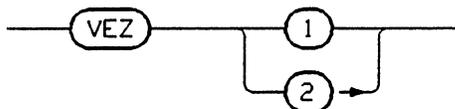
Up Counter



UPD

Causes the generator to update current status and run address information. This is done automatically every 50 milliseconds if the processor is not busy. UPD can be sent directly before executing the TLK 1 command to obtain the current run address and status.

Update Status and Address Information

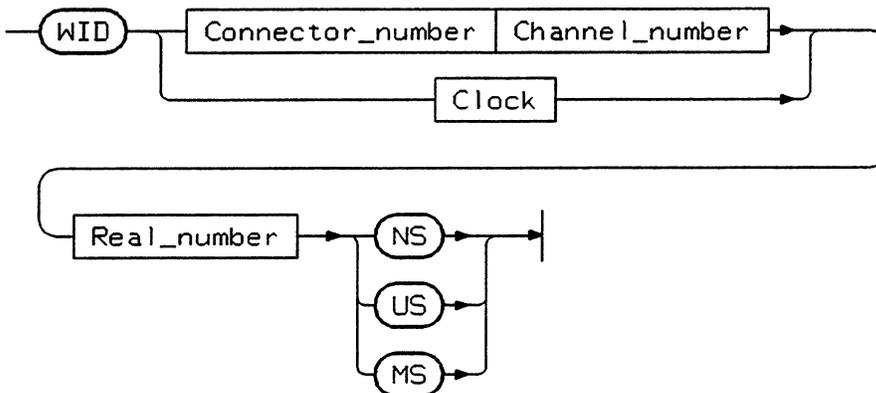


VEZ

Sets the vertical zoom factor of the analyzer Timing Diagram Page. The Timing Diagram Page does not have to be displayed for the command to function.

1	≡	Zoom factor X1
2	≡	Zoom factor X2

Vertical Zoom Factor



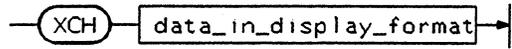
WID

Sets the width of the generator clock or RZ channel output signal.

connector_number	≡	hex number of connector
channel_number	≡	channel number to be set
clock	≡	1C, 2C for Clock 1 and Clock 2 respectively

Width

XCH



Switches the positions of two channels of data in the analyzer.

- 1 := First channel
- 2 := Second channel
- := Unchanged channels

The data input must be in the same format as displayed on the expected data page (channel configuration and organization). The command XCH --- 1--- ---2- --- exchanges the complete data set in the channel displayed fifth from the left with that of the 15th displayed channel.

Exchange Channels

Chapter 11

Generator Performance Verification

11-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications for the HP 8180A/B Data Generator and the HP 8181A/B Data Generator Extender given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place. The tests must be performed in the order given.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

11-2 Cycle Modes / Run / Stop / Break / Forward / Back Tests

For testing the different cycle modes, a low frequency (10Hz) is used in order to be able to follow the address changes on the 8180A/B display. The external gate signal is simulated by changing the threshold level of the RUN/GATED input. First and last address detection at maximum speed is tested separately.

1. Program 8180A/B Standard Set.
(PAGES, **STORE/RECALL** , **Rcl Std Set** , **EXECUTE**)
2. Clock Frequency 10 Hz.
(PAGES, **TIMING** , **Frequency** , 10, **HERTZ**)
3. Last Address 100.
(PAGES, **CONTROL** , **Last Address** , 100, **ENTER NUMBER**)

Auto Cycle Test

4. Press RUN and check that the 8180A/B starts with address 00000 (upper right hand corner of the display), counts up to address 00100 and continues with address 00000.

Break; Forward; Back; Stop Test

5. Press **BREAK**. The 8180A/B should switch to **BREAK**.
6. Increment and decrement addresses by pressing **FWD** and **BACK**. Note that addresses can be decremented down to the First Address.

Cycle Modes / Run / Stop / Break / Forward / Back Test

7. Press **RUN**. The 8180A/B should start one address after the Break Address.
8. Press **STOP** and **RUN**. The 8180A/B should start with the First Address.

Single Cycle Test

9. Program the 8180A/B to Single Cycle.
(PAGES, **CONTROL**, **Cycle Mode**, **SINGLE**)
10. Press **RUN** and check that the 8180A/B starts at address 00000 and stops at address 00100.

Gated Cycle Test

11. Program the following: Gated Cycle; Run (Gate) Input ON; Threshold +5V.
(PAGES, **CONTROL**, **Cycle Mode**, **Gated**, **EXIT** ↑
Inputs, **Run Input**, **ON**, **EXIT** ↑
Threshold, 5, **VOLT**)
12. Set threshold voltage to -5V (-, 5, **VOLT**). The 8180A/B should run between address 00000 and 00100 as in Auto Cycle.
13. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Gated Cycle Test

14. Program Init+Gated.
(PAGES, **CONTROL**, **Cycle Mode**, **INIT+GATED**)
15. First Address 30.
(PAGES, **CONTROL**, **First Address**, 30, **ENTER NUMBER**)
16. Input Threshold +5V.
(PAGES, **CONTROL**, **Inputs**, **Threshold**, 5, **VOLT**)
17. Program the threshold voltage to -5V (-, 5, **VOLT**) and check that the 8180A/B starts with address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.
18. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Auto Cycle Test

19. Program Init+Auto.
(PAGES, **CONTROL**, **Cycle Mode**, **Init+Auto**)
20. Run Input OFF.
(PAGES, **CONTROL**, **Inputs**, **Run Input**, **OFF**)
21. Press **RUN** and check that the 8180A/B starts at address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.

To repeat the whole sequence press **STOP** and **RUN** again.

Last Address (Address Difference Counter) Test

11-3 Last Address (Address Difference Counter) Test

This test ensures correct programmability of the address difference counters and proper operation up to 50 MHz.

1. Program 8180A/B Standard Set.
(PAGES, **Store/Recal**, **Rcl Std Set**, **EXECUTE**)
2. Clock Frequency 50 MHz.
(PAGES, **TIMING**, **Frequency**, 50, **MEGAHERTZ**)
3. Single Cycle.
(PAGES, **CONTROL**, **Cycle Mode**, **SINGLE**)
4. Last Address 00001.
(PAGES, **CONTROL**, **Last Address**, 1, **ENTER NUMBER**)
5. Press RUN and check that the 8180A/B stops at address 00001.
6. Change Last Address to 2 (2, **ENTER NUMBER**) press RUN and check cycle length.
7. Repeat Single Cycle test with the following Last Address settings:
8; 16; 32; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.

Strobe Break (Strobe Difference Counter) Test

11-4 Strobe Break (Strobe Difference Counter) Test

Correct programmability and proper strobe difference counter function at 50 MHz is verified with this test. After setting the Strobe Breaks, the instrument is stepped from Break to Break.

1. Program 8180A/B Standard Set.
(PAGES, **STORE/RECALL**, **Rcl Std Set**, **EXECUTE**)
2. Clock Frequency 50 MHz.
(PAGES, **TUNING**, **Frequency**, 50, **MEGAHERTZ**)
3. Clear Strobe.
(PAGES, **DATA**, **Edit**, **Clear & Set**, **Clear Strobe**, **EXECUTE**)
4. Strobe Breaks ON.
(PAGES, **CONTROL**, **Break Control**, **Strobe Breaks**, **ON**)
5. Entry Mode Vertical.
(PAGES, **DATA**, **Edit**, **Entry Mode**, **VERTICAL**, **EXIT** ↑↑, **EXIT** ↑↑)
6. Top Address 00000; Strobe Bit to 1.
(**Top Address**, 0, **ENTER NUMBER**, **EXIT** ↑↑, 1)
7. Using the Cursor softkey move cursor to address ⁰⁰⁰¹00001 and set strobe bit high by pressing the 1 key on the data entry key pad.
8. Set strobe bits to high in following addresses as described in step 7:
1; 2; 4; 8; 16; 32; 64; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.
9. Press **STOP** and **RUN**. The 8180A/B should be in **BREAK** at address 00000.
10. Press **RUN** again and the 8180A/B should break at address 00001.
11. Check that the 8180A/B breaks at addresses 2; 4; 8; 16; 32; 64; 128; 256, 512, 1024, 2048, 4096, 8192 and 0 each time after pressing **RUN** again. On the 8180A check up to 512.

11-5 Internal Clock Frequency Test

Specification

Accuracy: $\pm 5\%$ of programmed value.

Description

The Strobe output signal programmed as clock is used to measure the internal clock generator accuracy. Clock timing errors flagged up on the screen with Standard Set and 50 MHz programmed have no influence on the Strobe output.

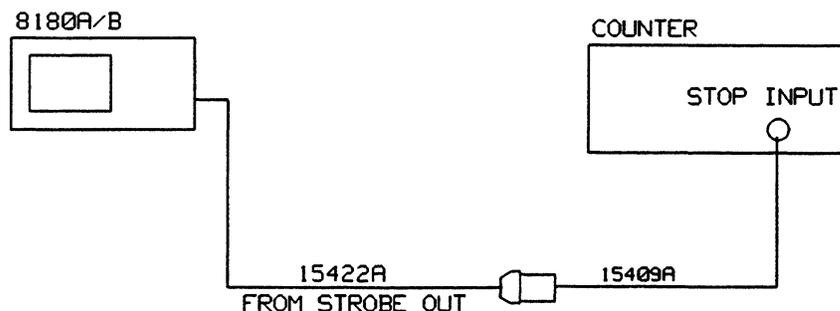


Figure 11-1. Test Setup for the Internal Clock Frequency Test

Equipment

Universal Counter	HP 5370B
Plug-on BNC Adapter	HP 15409A
Clock and Strobe Cable Set	HP 15422A

Procedure

- Set counter as follows.

Trig Level:	+0.14V
FUNCTION:	FREQUENCY
GATE:	0.01s
STOP IMP:	50 Ohm
START COM switch:	SEParate
- Program 8180A/B Standard Set
(PAGES, **STORE/RECALL**, **Rcl Std Set**, **EXECUTE**)
- Strobe Level TTL
(PAGES, **OUTPUT**, **Strobe Level**, **TTL**)
- Strobe Output Clock; Outputs ON
(PAGES, **CONTROL**, **Strobe Output**, **CLOCK**, **EXIT** ↑, **Outp on/off**, **ON**)
- Frequency 50 MHz
(PAGES, **TIMING**, **Frequency**, 50, **MEGAHERTZ**)
- Connect equipment as shown in Figure 11-1 and press RUN.

Internal Clock Frequency Test

7. Check 8180A/B internal clock generator at the set frequencies as detailed in Table 11-1.

Table 11-1. Internal Clock Frequency Test Values - Tested Frequencies

Set Frequency	Min. Frequency	Max. Frequency
50.00 MHz	47.50 MHz	52.50 MHz
25.00 MHz	23.75 MHz	26.25 MHz
10.00 MHz	9.50 MHz	10.50 MHz
9.99 MHz	9.49 MHz	10.49 MHz
3.00 MHz	2.85 MHz	3.15 MHz
1.00 MHz	0.95 MHz	1.05 MHz
1.05 Hz	1.00 Hz	1.10 Hz

11-6 Clock and Data Skew Test

Specification

Skew: ≤ 1.6 ns for Clock and Data channels.

Description

A Square Wave pattern is used to test the Clock channels and all installed Data channels. The Strobe clock signal is used as a reference, the maximum deviation from positive going Strobe transition should be $\leq \pm 0.8$ ns. TTL levels are used for all outputs, the test is valid also for the 8181A/B NRZ Data channels.

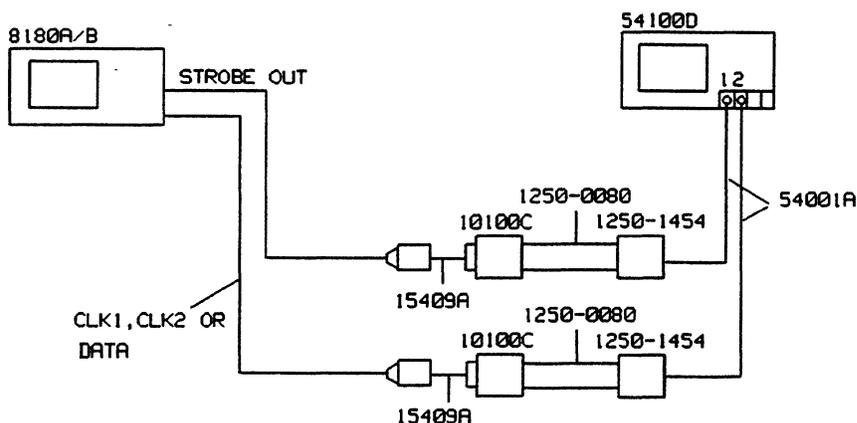


Figure 11-2. Test Setup for the Clock and Data Skew Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Scope Probe Adapter	1250-1454
BNC Adapter female/female	1250-0080
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Strobe/Clock Cable Assy	HP 15422A
Data Cable	HP 15423A

Procedure

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL, Rcl Std Set, EXECUTE)
2. Label A TTL, Strobe TTL, Strobe to Clock.
(PAGES, OUTPUT, Level, TTL Levels, EXECUTE, EXIT, ↑, Strobe Level, TTL, PAGES, CONTROL, Strobe Output, CLOCK)
3. Clock 1 Format RZ=50%; Clock 2 Format RZ=50%; Clock 1 Delay 0 ns; Clock 2 Delay 0 ns.
(PAGES, TIMING, Clock Timing, Clock1 Format, RZ=50%, EXIT, ↑↑)

Clock and Data Skew Test

Clock2 Format , RZ=50% , EXIT ↑↑ ,
Clock 1 Delay , 0 , NANOSEC , EXIT ↑↑ ,
Clock 2 Delay , 0 , NANOSEC)

4. First address 00000; Last Address 00001.
(PAGES , CONTROL , First Address , 0 , ENTER NUMBER , EXIT ↑ ,
Last Address , 1 , ENTER NUMBER)
5. Set Data.
(PAGES , Data [fill Data pattern at first address with 1's, and Data pattern at last address with 0's])
6. Connect the equipment as shown in Figure 11-2. Switch outputs ON and start the generator
(PAGES , OUTPUT , Outp on/off , ON)
Press RUN.

Cancel out interchannel delay between scope channel 1 and scope channel 2.
7. Set scope as follows:
(Autoscale > Display > Split Screen to OFF > Trigger > TRG Mode to State > TRG on Pos Edge > On Chan 2 > When Pattern L-XX > Timebase > Sec/Div > 500ps > More > Wfmsave > Memory 1 to ON > Clear Memory 1 > Store to Memory 1).
8. Connect in turn all Clock and Data channels to scope input 1 and store each displayed transition to Memory 1.
9. Set Start Marker to the 50% point of the displayed strobe transition and measure with the Stop Marker the maximum \pm deviation of the stored channel transitions (Delta t > T Markers to ON > Start Marker > Knob > Stop Marker > Knob)
10. The maximum deviation should be $\leq \pm 0.8$ ns.

Clock 1, Clock 2 Delay Test

11-7 Clock 1, Clock 2 Delay Test

Specification

Accuracy: $\pm 5\%$ of programmed value ± 1 ns

Description

The clock delays are referenced to the Strobe clock output signal. Delays longer than 300ns are measured with a time interval counter.

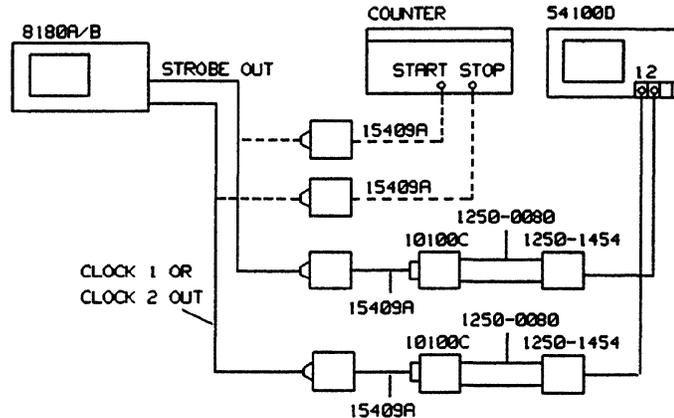


Figure 11-3. Test Setup for the Clock 1 and Clock 2 Delay Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Clock, Strobe Cable Assembly	HP 15422A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454
Counter	HP 5370B

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL, Rcl Std Set, EXECUTE)
2. Period 1 μ s.
(PAGES, TIMING, Period, 1, MICROSEC)
3. Label A TTL; Strobe TTL; Strobe output to Clock.
(PAGES, OUTPUT, Level, TTL Levels, EXECUTE, EXIT \uparrow , Strobe Level, TTL, PAGES, CONTROL, Strobe Output, CLOCK)
4. Clock 1 and Clock 2 Format RZ = 50%; Clock 1 and Clock 2 Delay = 0.00 ns.
(PAGES, TIMING, Clock Timing, Clock1 Format, RZ=50%, EXIT \uparrow , Clock2 Format, RZ=50%, EXIT \uparrow , Clock 1 Delay, 0, NANOSEC, EXIT \uparrow , Clock 2 Delay, 0, NANOSEC)

Clock 1, Clock 2 Delay Test

5. Outputs ON.
(PAGES, **OUTPUT**, **Outp.on/off**, **ON**)
6. Clock 1 (2) Delay in Softkey Area and start the generator.
(PAGES, **TIMING**, **Clock Timing**, **Clock 1 Delay**, (**Clock 2 Delay**))
Connect the equipment as shown in Figure 11-3 and start the generator (press RUN).

Cancel out scope trigger delay of channel 2 and interchannel delay between scope channel 1 and channel 2.
7. Connect equipment as shown in the measurement setup and set the scope as follows:
(Autoscale > Trigger > Trig Src to Chan2 > Slope to pos > Timebase > Ins > Display > Split Screen to OFF > Delta > T Markers to ON > Start Marker to 0.00ns (50% point of the positive going transition of the Strobe clock signal))

Note: The position of the start marker is used as reference for this test and should therefore not be moved during the measurement.
8. Set clock delay to 30 ns (30, **NANOSEC**).
9. Set the scope as follows:
(Timebase > Delay > 30ns > Delta t > Stop Marker > 30ns > Knob)
10. Position the Stop Marker at the 50% point of the displayed transition and read Delta t. Delta t must be in the following range:
Delta t minimum = 27.5 ns
Delta t maximum = 32.5 ns
11. Check also the clock delay for the settings detailed in Table 11-2.

Table 11-2. Clock 1, Clock 2 Delay Test Values - Clock Delay at 1 μ s Period

Set Delay	Min. Delay	Max. Delay
89.9 ns	84.4 ns	95.4 ns
90.0 ns	84.5 ns	95.5 ns
300 ns	284 ns	316 ns

12. Disconnect the Strobe and Clock connections from the scope (between 15409A and 10100C) and connect Strobe cable to Start Input of the counter and the Clock 1 (2) cable to the Stop Input of the counter.
13. Set the counter as follows:

Function:	Time Interval
Sample Size:	1
Start/Stop input:	Level to Preset
Start/Stop slopes:	J
Start/Stop input impedance:	50 Ohm
AC/DC switches to:	AC
Start COM/SEP switch:	SEP

Clock 1, Clock 2 Delay Test

14. Change 8180A/B Clock Period to 200 ms and check delay at Clock 1 and 2 at settings given in Table 11-3:

(PAGES, TIMING, Period, 200, MILLISEC, EXIT ↑,
Clock Timing, Clock 1 Delay [Clock 2 Delay])

Table 11-3. Clock 1, Clock 2 Delay Test Values - Clock Delay at 200 ms Period

Set Delay	Min. Delay	Max. Delay
989 ns	938.5 ns	1039.5 ns
100 ms	95.0 ms	105.0 ms

Clock 1, Clock 2 Width Test

11-8 Clock 1 , Clock 2 Width Test

Specification

Accuracy: $\pm 5\%$ of programmed value ± 1 ns

Description

The clock width is measured at 50% amplitude. Width ranges greater than 300 ns are measured with the counter.

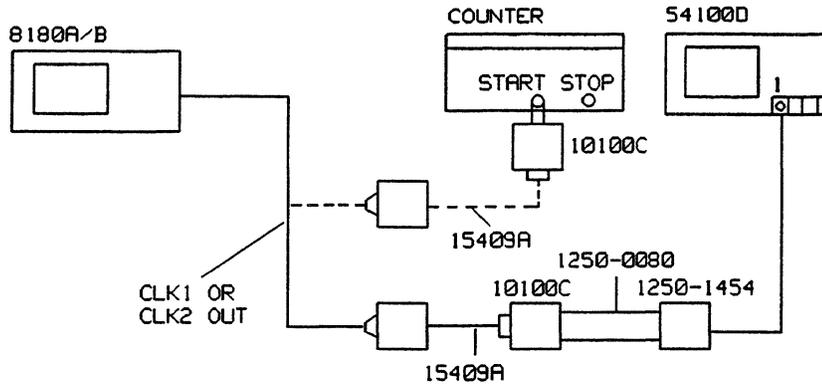


Figure 11-4. Test Setup for the Clock 1 and Clock 2 Width Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Clock, Strobe Cable Assembly	HP 15422A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Scope Probe Adapter	1250-1454
Counter	HP 5370B
BNC Adapter female/female	1250-0080

Procedure

1. Program 8180A/B Standard Set
(PAGES, **STORE/RECALL**, **Rcl. Std. Set**, **EXECUTE**)
2. Clock Period 1 μ s
(PAGES, **TIMING**, **Period**, 1, **MICROSEC**)
3. Label A TTL
(PAGES, **OUTPUT**, **Level**, **TTL Level**, **EXECUTE**)
4. Outputs ON
(PAGES, **OUTPUT**, **Outp. on/off**, **ON**)
5. Connect the equipment as shown in Figure 11-4 and press RUN.
6. Set the scope as follows:
(Autoscale > Timebase > Sec/DIV > 500 ps)

Clock 1, Clock 2 Width Test

7. Set the Start Marker to the 50% point of the displayed positive going transition.
(Delta t > T Markers to ON > Start Marker > Knob)
 8. Set Clock 1 Width to 10 ns.
(PAGES, **TIMING**, **Clock Timing**, **Clock 1 Width**, 10, **NANOSEC**, **EXIT** ↑)
 9. Set the scope as follows:
(Timebase > Delay > 10 ns > Delta t > Stop Marker > Knob)
 10. Adjust the Stop Marker to the 50% point of the negative going transition of the Clock 1 signal and read Delta t.
Delta t minimum = 8.5 ns
Delta t maximum = 11.5 ns
- Note: The position of the Start Marker is used as reference for the following measurements and should therefore not be moved.
11. Check step linearity when incrementing the width in 100 ps steps up to 20 ns.
 12. Check clock width using the procedure described in steps 8 to 10 for the width settings given in Table 11-4.

Table 11-4. Clock 1, Clock 2 Width Test Values - Clock Width at 1 μs Period

Set Width	Min. Width	Max. Width
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns
300.0 ns	284.0 ns	316.0 ns

13. Disconnect the clock connection between the 10100C and 1250-0080 and connect the 10100C to the Start Input of the counter.
14. Set the counter as follows:

Function:	Time Interval
Sample Size:	1
Start/Stop Input Levels:	Preset
Start slope to:	1
Stop slope to:	1
Start & Stop Input Imp.:	1 MΩ
AC/DC switches to:	AC
START COM/SEP switch:	START COM
Divider:	divide by 10
15. Change 8180A/B Clock Period to 200 ms and check Clock 1 width at the settings given in Table 11-5.
(PAGES, **TIMING**, **Period**, 200, **MILLISEC**, **EXIT** ↑, **Clock Timing**, **Clock 1 Width**)

Clock 1, Clock 2 Width Test

Table 11-5. Clock 1, Clock 2 Width Test Values - Clock Width at 200 ms Period

Set Width	Min. Width	Max. Width
999 ns	948 ns	1050 ns
100 ms	95.0 ns	105 ns

16. Perform the above procedures for Clock 2.

Timing Channel Delay Test

11-9 Option 002 Timing Channel Delay Test

Specification

Accuracy: $\pm 5\%$ of programmed value ± 1 ns

Description

Data channel delays are referenced to the Strobe Clock output signal. Delays greater than 300 ns are measured with a time interval counter.

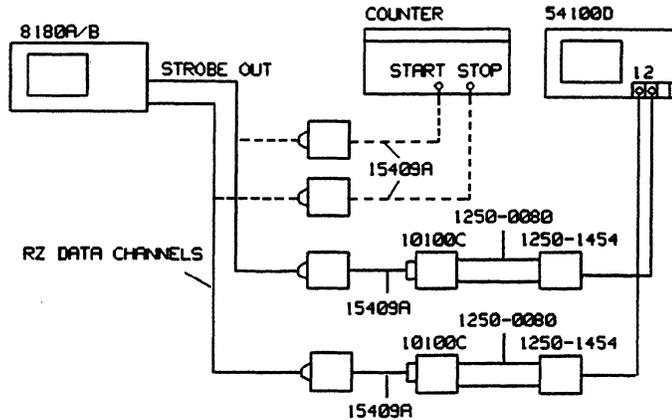


Figure 11-5. Test Setup for the Timing Channel Delay Test

Equipment

Scope	HP 54100D
Active Pads	HP 54001A
Counter	HP 5370B
Clock, Strobe Cable Assembly	HP 15422A
Data Cable set	HP 15423A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL, Rcl Std Set, EXECUTE)
2. Set Clock Period to 1 μ s.
(PAGES, TIMING, Period, 1, MICROSEC)
3. Label A TTL; Strobe TTL; Strobe Output to Clock.
(PAGES, OUTPUT, Level, TTL Levels, EXECUTE, EXIT, Strobe Level, TTL, PAGES, CONTROL, Strobe Output, CLOCK)
4. Outputs ON.
(PAGES, OUTPUT, Outp on/off, ON)

Timing Channel Delay Test

5. Set Data.
(PAGES, **Data**, **Edit**, **Clear & Set**, **Set DATA**, **EXECUTE**)
6. Connect the equipment as shown in Figure 11-5 and press RUN.

NRZ Function Test

7. Check all installed RZ channels listed on the Timing Page for a static TTL high level (greater than +2V).
8. Set All Channel Format to RZ.
(PAGES, **TIMING**, **Channel Timing**, **All Ch. Format**, **RZ**)

Cancel out interchannel skew between scope channel 1 and channel 2 and the trigger delay of channel 2.

9. Set the scope as follows:
(Autoscale > Timebase > Sec/DIV > 500 ps > Trigger > Trg Src to Channel 2 > slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)
10. Position the Start Marker to the 50% point of the positive going Strobe transition (0.00 ns).

Note: The position of the Start Marker is used as reference for this test and should therefore not be moved during the measurement.

Delay Test

11. Set All Channel Delay to 10 ns.
(PAGES, **TIMING**, **Chnl Timing**, **All Ch Delay**, 10, **NANOSEC**)
12. Set the scope as follows:
(Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Timebase > Delay > 10 ns > Delta t > Stop Marker > 10ns > Knob)
13. Place the Stop Marker at the 50% point of the displayed positive going transition and read Delta t.
Delta t minimum = 8.5 ns
Delta t maximum = 11.5 ns
14. Check in turn all RZ Data channels.
15. Repeat steps 11 to 14 for the settings given in Table 11-6.

Table 11-6. Timing Channel Delay Test Values - Clock Period at 1 μ s

Set Delay	Min. Delay	Max. Delay
10.0 ns	8.5 ns	11.5 ns
30.0 ns	27.5 ns	32.5 ns
89.9 ns	84.4 ns	95.4 ns
90.0 ns	84.5 ns	95.5 ns
300 ns	284 ns	316 ns

16. Change the Clock Period to 200 ms.
(PAGES, **TIMING**, **Period**, 200, **MILLISEC**, **EXIT** \uparrow , **Chnl Timing**, **All Ch Delay**)
17. Disconnect the Strobe and Data cable from the scope (between 15409A and 10100C) and connect the cables to the counter inputs as shown in the measurement setup.

Timing Channel Delay Test

18. Set the counter as follows:

Function:	Time Interval
Sample size:	1
Start/Stop levels:	Preset
Start/Stop slope:	J
Input impedances:	50 Ω
AC/DC switches:	AC
Start CAM/SEP switch:	SEP
Input Divider:	divide by 1

19. Check in turn all RZ Data channels for the delay settings given in Table 11-7.

Table 11-7. Timing Channel Delay Test Values - Clock Period at 200 ms

Set Delay	Min. Delay	Max. Delay
989.0 ns	938.5 ns	1039.5 ns
100.0 ms	95.0 ms	105.0 ms

Option 002 Timing Channel Width Test

11-10 Option 002 Timing Channel Width Test

Specification

Accuracy: $\pm 5\%$ of programmed value ± 1 ns

Description

The Data channel width is measured at 50% of amplitude. Width ranges greater than 300 ns are checked with the counter.

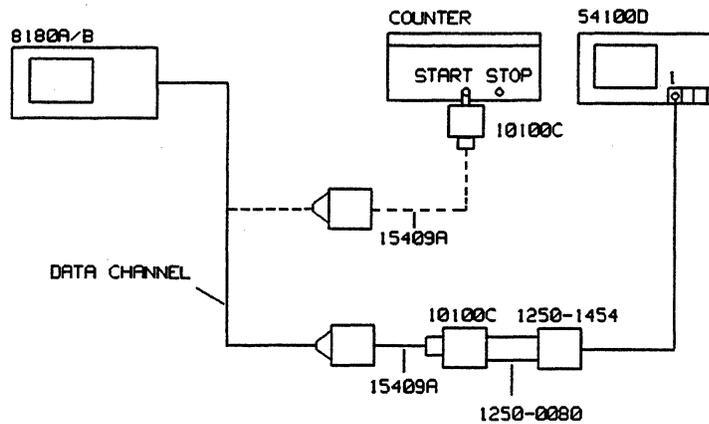


Figure 11-6. Test Setup for the Timing Channel Width Test

Equipment

Scope	HP 54100D
Active Pods	HP 54001A
Counter	HP 5370B
Data cable set	HP 15423A
BNC Adapter	HP 15409A
50 Ω Feedthrough	HP 10100C
BNC Adapter female/female	1250-0080
Scope Probe Adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
(PAGES, **Store/Recall**, **Rcl:Std:Set**, **EXECUTE**)
2. Period 1 μ s (PAGES, **Timing**, **Period**, 1, **MICROSEC**)
3. Label A TTL; Outputs ON.
(PAGES, **Output**, **Level**, **TTL LEVELS**, **EXECUTE**,
EXIT \uparrow ,
Outp on/off, **ON**)
4. Set Data.
(PAGES, **DATA**,
Edit, **Clear & Set**, **Set Data**, **EXECUTE**)

Option 002 Timing Channel Width Test

5. All Channel Width 10 ns.
(PAGES, **TIMING**, **Chnl Timing**, **All Ch Format**, **RZ**, **EXIT** ↑↑
, **All Ch Width**, 10, **NANOSEC**)
6. Connect the equipment as shown in Figure 11-6 and press RUN.

Cancel out the trigger delay of scope channel 1.
7. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 500 ps > Trigger > Trigger Src to Chan 1 > Slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)
8. Position the Start Marker at the 50% point of the positive going Data transition.

Note: The position of the Start Marker is used as reference and should therefore not be moved during the measurements.
9. Set the scope as follows:
(Timebase > Delay > 10 ns > Delta t > Stop Marker > 10 ns > Knob)
10. Position the Stop Marker at the 50% point of the negative going transition of the Data pulse and read Delta t.
Delta t min. = 8.5 ns
Delta t max. = 11.5 ns
11. Check in turn all RZ Data channels for the width settings given in Table 11-8.

Table 11-8. Timing Channel Width Test Values - Clock Period at 1 μs

Set Width	Min. Width	Max. Width
10.0 ns	8.5 ns	11.5 ns
30.0 ns	27.5 ns	32.5 ns
99.0 ns	83.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns
300.0 ns	284.0 ns	316.0 ns

12. Change 8180A/B clock period to 200 ms.
(PAGES, **TIMING**, **Period**, 200, **MILLISEC**, **EXIT** ↑↑
, **Chnl Timing**, **All Ch Width**)
13. Disconnect the Data probe from the scope (between 10100C and 1250-0080) and connect the open end of the 10100C to the counter Start input.
14. Set the counter as follows:

Function:	Time Interval
Sample size:	1
Start/Stop input levels:	Preset
Start slope:	↓
Stop slope:	↑
Input impedances:	1 MΩ
AC/DC switches:	AC
Start COM/SEP switch:	Start COM
Input Divider:	divide by 10

Option 002 Timing Channel Width Test

15. Check in turn all RZ Data channels for the delay settings given in Table 11-9.

Table 11-9. Timing Channel Width Test Values - Clock Period at 200 ns

Set Width	Min. Width	Max. Width
999.0 ns 100.0 ms	948.0 ns 95.0 ms	1050.0 ns 105.0 ms

Data High / Low Level Accuracy Test

11-11 Data High / Low Level Accuracy Test

Specification

Level accuracy: $\pm 0.5\%$ of level $\pm 60\text{mV}$ (add $\pm 60\text{mV}$ for amplitudes smaller than 1.5V); only valid with standard cable length of 1.5m.

Description

High and low level accuracy is measured with a digital voltmeter. All data channels are set to the NRZ format. To measure the high level all data is set to high. Low level is measured with data cleared (low).

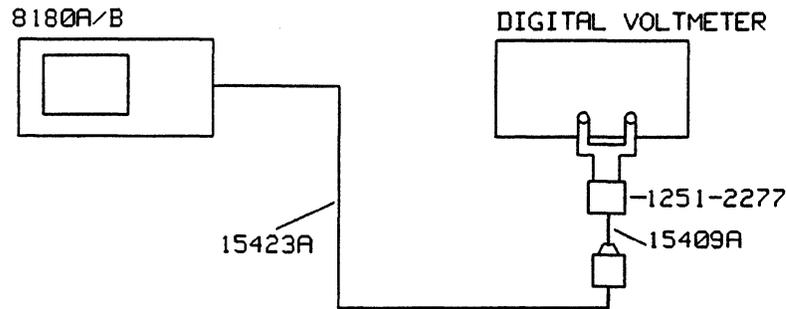


Figure 11-7. Test Setup for the Level Accuracy Test

Equipment

Digital Voltmeter	HP 3456A
BNC (f) to dual banana Plug	1251-2277
Plug-on BNC Adapter	HP 15409A
Data Cable Set	HP 15423A

High Level Accuracy Test

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL , Rcl Std Set , EXECUTE)
2. Set Data.
(PAGES, DATA , Edit , Clear & Set , Set Data , EXECUTE)
3. Load Impedance to Open.
(PAGES, OUTPUT , Load Imp , Open)
4. Outputs ON.
(PAGES, OUTPUT , Outp on/off , ON)
5. Label A Low Level to -2V, High Level to -1V.
(PAGES, OUTPUT , Level , Low ↔ High [to low], -, 2, Volt , Low ↔ High [to high], -, 1, Volt)
6. Connect the equipment as shown in Figure 11-7 and press RUN.
7. Measure the output voltage at the high level settings given in Table 11-10.

Data High / Low Level Accuracy Test

Table 11-10. Data High Level Accuracy Test Values

Set Level	Min. Level	Max. Level
-1.00 V	-0.875 V	-1.125 V
0.00 V	-0.060 V	+0.060 V
+1.00 V	+0.875 V	+1.125 V
+5.00 V	+4.375 V	+5.085 V
+17.00 V	+16.860 V	+17.150 V

8. Repeat step 7 for all Data channels.

Low Level Accuracy Test

9. Clear Data.
(PAGES, **DATA**, **Edit**, **Clear & Set**, **Clear Data**, **EXECUTE**)
10. Set Label A High Level to +17V, Low Level to -2V.
(PAGES, **OUTPUT**, **Level**, **Low ↔ High** [to high], 17, **Volt**, **Low ↔ High** [to low], -, 2, **Volt**)
11. Measure the output voltage at the low level settings given in Table 11-11.

Table 11-11. Data Low Level Accuracy Test Values

Set Level	Min. Level	Max. Level
-2.00 V	-1.930 V	-2.070 V
-1.00 V	-0.935 V	+1.065 V
0.00 V	+0.060 V	+0.060 V
+1.00 V	+0.875 V	+1.125 V
+16.00 V	+15.860 V	+16.140 V

12. Repeat step 11 for all data channels.

11-12 20 MHz Memory Test

Description

The 8180A/B memory can be tested with a Signature Multimeter up to 20 MHz. Start/Stop conditions for the Signature Multimeter are established with a high bit in the strobe channel. A pseudo-random binary sequence which can be generated on all channels is used as the test pattern.

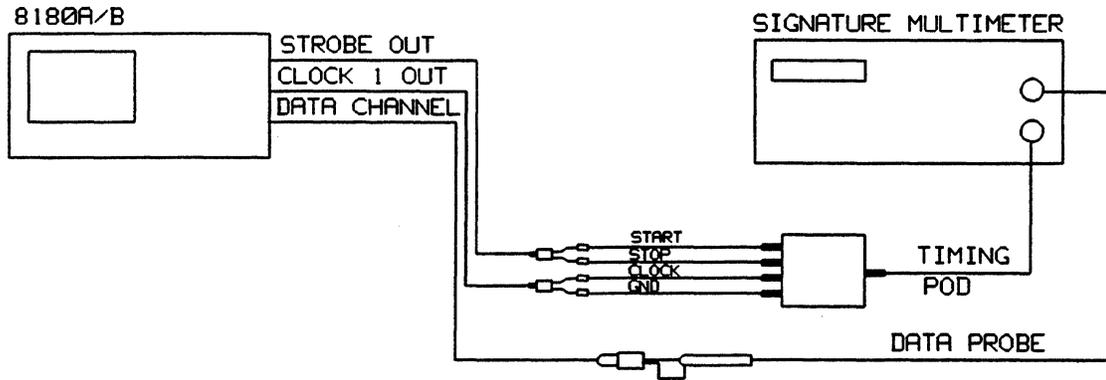


Figure 11-8. Test Setup for the 20 MHz Memory Test

Equipment

Signature Multimeter	HP 5005A
Data Cable Set	HP 15423A
Clock Strobe Cable Set	HP 15422A
Solder-in Receptacle	HP 15412A

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL, Rcl Std Set, EXECUTE)
2. Clock 1 Format to RZ 50%; Clock 1 Delay to 25 ns; Clock 2 Delay to 0 ns.
(PAGES, TIMING, Clock Timing, Clock1 Format, RZ = 50%, EXIT ↑, Clock 1 Delay, 25, NANOSEC, EXIT ↑, Clock 2 Delay, 0, NANOSEC)
3. Clock Period to 50 ns.
(PAGES, TIMING, Period, 50, NANOSEC)
4. Load Impedance Open; Label A TTL.
(PAGES, OUTPUT, Load Imp, Open, EXIT ↑, Level, TTL Levels, EXECUTE)
5. Strobe Level TTL; Outputs ON.
(PAGES, OUTPUT, Strobe Level, TTL, EXIT ↑, Outp on/off, ON)
6. Clear Strobe.
(PAGES, DATA, Edit, Clear & Set, Clear Strobe, EXECUTE)

20 MHz Memory Test

7. PRBS on Channel 0-0.
(PAGES, **DATA**, **Edit**, **Channel Edit**, **Channel PRBS**, **→**)
[until PRBS channel 00 is displayed], **EXECUTE**, **EXIT** (↑↑))
8. Copy Channel.
Press Copy Channel and using the **→** softkey in the right hand half of the display move the inverse video cursor until Copy Channel **0-0** to **0-0** is displayed.
9. Copy Channel 0-0 to all other channels.
Press alternately (**←** [on the right hand half of the display] and **EXECUTE**) until all Data channels contain the pattern in channel 0-0.
10. Set the Strobe Bit to High at address 00000.
(PAGES, **DATA**, **Top Address**, 0, **ENTER NUMBER**, **EXIT** (↑), 1)
11. Connect the equipment as shown in Figure 11-8 and press RUN.
12. Check all data channels for the following signature:
On the 8180A - 46F9
On the 8180B - H150

11-13 Ext. Clock; RUN; BREAK and STOP Hysteresis/Threshold Test

Specification

Threshold Accuracy: $\pm 3\%$ of programmed value ± 50 mV

Description

A low frequency triangular wave signal is used to stimulate the 8180A/B external inputs. When the current threshold level of the 8180A/B inputs is reached, the 8180A/B starts or stops generating a signal at its Clock 1 output. Both signals, the triangular wave signal and the Clock 1 output signal are displayed on the scope. The level of the triangular wave signal where Clock 1 generation commences or stops is the actual input threshold.

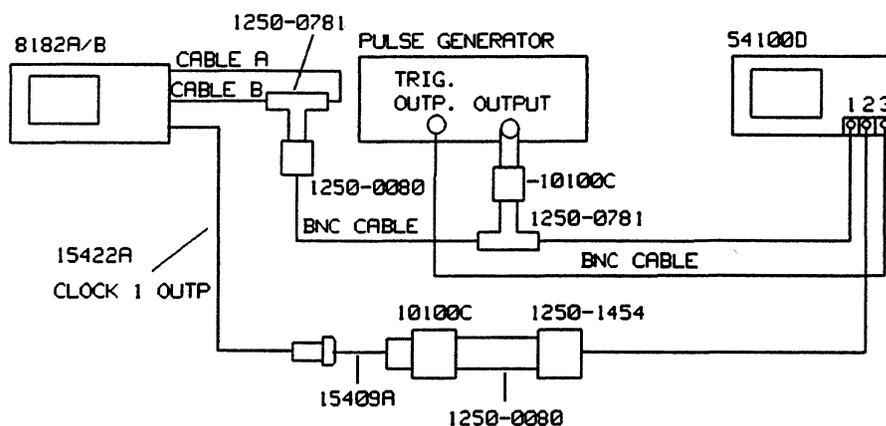


Figure 11-9. Test Setup for the External Input Test

Equipment

Pulse/Function Generator	HP 8007B/HP8116A
Scope	HP 54100D
Active Pods	HP 54001A
50 Ohm Pod	HP 54002A
50 Ohm Feedthrough	HP 10100C
BNC Tee Adapter	1250-0781
BNC female/female	1250-0080
Scope Probe Adapter	1250-1454
BNC Adapter	HP 15409A
Clock/Strobe cable set	HP 15422A
BNC Cable	

Procedure

1. Program 8180A/B Standard Set.
(PAGES, STORE/RECALL, Rcl Std Set, EXECUTE)
2. Clock 1 Width 20 ns; Clock 2 Delay 0 ns.
(PAGES, TIMING, Clock Timing, Clock 1 Width, 20, NANOSEC, EXIT, Clock 2 Delay, 0, NANOSEC)

Ext. Clock; RUN; BREAK; and Stop Hysteresis/Threshold Test

3. Label A TTL; Outputs ON.
(PAGES, **OUTPUT**, **Level**, **TTL Levels**, **EXECUTE**,
EXIT ↑,
Outp on/off, **ON**)
4. Input Impedance 100 K Ω
(PAGES, **CONTROL**, **Inputs**, **Impedance**, **100 k Ω**)
5. Clock Source External Positive Edge
(PAGES, **CONTROL**, **Clock Source**, **EXTERNAL J**)
6. Set the Pulse Generator as follows:

Period approx.	1 ms
Width	0.5 ms
Transition	5 μ s to 250 μ s
Amplitude	250 mVpp (into open)
Offset	ON
7. Adjust leading edge and trailing edge for a triangle waveform on the scope.

External Clock Test

8. Connect the equipment as shown in Figure 11-9 and press RUN. (BNC Cable A connected to External Clock Input.)
9. Adjust the triangular waveform such that it is symmetrical about 0V using the pulse generator's offset vernier.
10. Set the scope as follows:
(Autoscale > Chan 2 > Volts/Div > 1 Volt > Trigger > Trig Src to Chan 2 > Trigger Level > 1 Volt > Chan 1 > Chan 1 Mode to Magnify > Magnify to ON > Volts/Div > 20mV/Div > Offset > 0V > Timebase > Sec/Div > 50 μ s)
11. The displayed transition should cross the vertical graticule line between ± 50 mV.
12. Change External Clock Slope (active edge) to negative. (**EXTERNAL L**)
13. The displayed transition should cross the vertical graticule line between ± 50 mV.

External RUN and BREAK Test

14. Connect cable A to the Break Input (cable B to the Run Input).
15. Set the 8180A/B to Clock Source INTERNAL; RUN Input to ON, active edge positive; BREAK Input to ON, active edge negative.
(PAGES, **CONTROL**, **Inputs**, **Clock Source**, **INTERNAL**,
EXIT ↑↑,
Run Input, **ON J**, **EXIT** ↑↑,
Break Input **ON L**)
16. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 200 microsec/Div > Trigger > Trigger Source to Channel 3 > Trigger Level > 1 Volt > Delta t > T Markers to ON > Start Marker > Knob > Stop Marker > Knob)
Set the Start Marker to the positive going edge of displayed pulse on channel 2. Set the Stop Marker to the negative going edge of displayed pulse on channel 2.

Ext. Clock; RUN; BREAK; and Stop Hysteresis/Threshold Test

17. Set the scope as follows:
(Timebase > Delay > Knob)
Adjust Start Marker to the vertical center graticule line.
18. Set the scope as follows:
Timebase to 50 μ s; Chan 2 to OFF; Split Screen to OFF
(Sec/Div > 50 μ s > Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Channel 1 > Channel 1 Mode to Magnify > Magnify ON > Volts/Div > 20 mV/Div.
19. The displayed transition should cross the vertical graticule line within the limits of ± 50 mV.
20. Repeat the measurement at the position where the Stop Marker is located. The displayed transition should cross the vertical graticule line within the limits of ± 50 mV.
21. Set the Run Input to ON, active edge negative; Break Input to ON, active edge positive.
(EXIT $\uparrow\uparrow$, Run Input , ON \downarrow , EXIT $\uparrow\uparrow$,
Break Input , ON \downarrow)
22. Repeat step 15 through 20 with reversed slopes for Run and Break Inputs. Threshold Limit is ± 50 mV.

External STOP Test

23. Connect cable A to the Stop Input (cable B to the Run Input).
24. Check threshold levels of the Stop Input for both slopes as described above for the Break Input.
25. Check Clock, Run, Break and Stop inputs at +2 Volt and -2 Volt threshold settings.
(PAGES , CONTROL , Inputs , Threshold , 2 [-2], VOLT) .

For this test set the pulse generator to triangular waveform with an amplitude of 8V pp symmetrical about 0V.

Limits: Voltage Threshold minimum = 1.85 V
Voltage Threshold maximum = 2.15 V

Check inputs only at one slope setting.

11-14 Transition Time / Overshoot Test

Specification

Transition Time: less than $3.0 \text{ ns} + |\text{amplitude}| \times 0.2 \text{ ns}$.
 Preshoot, Overshoot, Ringing: less than $\pm 10\%$ of amplitude.
 Specifications are valid for a cable length of 1.5 m.

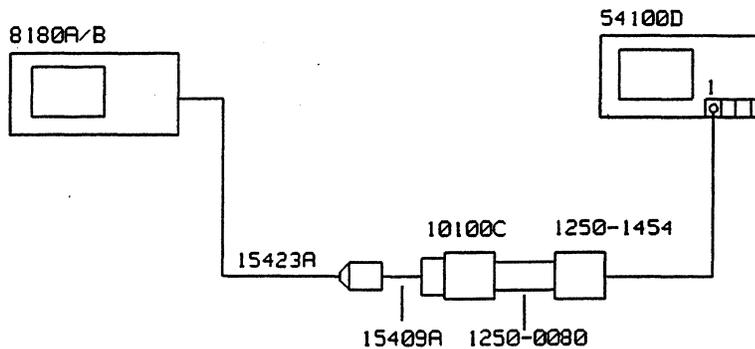


Figure 11-10. Test Setup for the Transition Time / Overshoot Test

Equipment

Scope	HP 54100D
Active Pod	HP 54001A
Data Cable	HP 15423A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
BNC female/female	1250-0080
BNC scope probe adapter	1250-1454

Procedure

1. Program 8180A/B Standard Set.
 (PAGES, **STORE/RECALL**, **Rcl Std Set**, **EXECUTE**)
2. Set all bits at address 00000 High; Set all bits at address 00001 Low.
 (PAGES, **DATA**, **Top Address** 0 **ENTER NUMBER**, **EXIT**, **↑**)
 Press 1 until the strobe channel and all data channels at address 00000 are set to high.
 Press 0 until the strobe channel and all data channels at address 00001 are set to low.
3. Last Address 00001.
 (PAGES, **CONTROL**, **Last Address**, 1, **ENTER NUMBER**)
4. Outputs ON.
 (PAGES, **OUTPUT**, **Outp on/off**, **ON**)
5. Set Label A High Level to -1 V; Low Level -2 V.
 (PAGES, **OUTPUT**, **Level**, **Low ↔ High** [to High], -1, **Volt**, **Low ↔ High** [to Low], -2, **VOLT**)
6. Connect the equipment as shown in Figure 11-10 and press RUN.
7. Set the scope as follows:
 (Autoscale > Delta V > Vmarkers to ON > Marker 1 Position > Knob [set Marker 1 to 0% of pulse])

Transition Time / Overshoot Test

> Marker 2 Position > Knob [set Marker 2 to 100% of pulse] > 10-90% > Timebase > Sec/Div > 500 ps > Delta t > T Markers to ON > Start Marker > Knob [set the Start Marker to the crossing point at the 10% Level and displayed transition] > Stop Marker > Knob [Set the Stop Marker to the crossing point at the 90% Level and displayed transition]).

8. Measure the transition time (Delta t) from 10 % to 90 % of amplitude for all data channels.
Specification: Transition Time = less than 3 ns.

9. Change Label A High Level to + 2 V; Low Level to 0 V.
(PAGES, OUTPUT, Level, Low ↔ High [to High], 2, VOLT, Low ↔ High [to Low], 0, VOLT)

10. Measure preshoot, overshoot and ringing at all data channels.
Specification: less than ±10% of amplitude.

Chapter 12

Analyzer Performance Verification

12-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications of the HP 8182A/B Data Analyzer given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

12-2 Trigger Word and Operating Modes Tests

Description

The Data Generator HP-Model 8180A/B is used to generate the Trigger Word (bit) for two 8182A/B data channels. The error display indicates the Trigger Word position. Because of the cleared memory, the Trigger Word appears as an error. When selecting Trigger Event Start Compare Mode, the Trigger Delay is set to 00001. This causes the Trigger Word to be displayed in address 1023/16383.

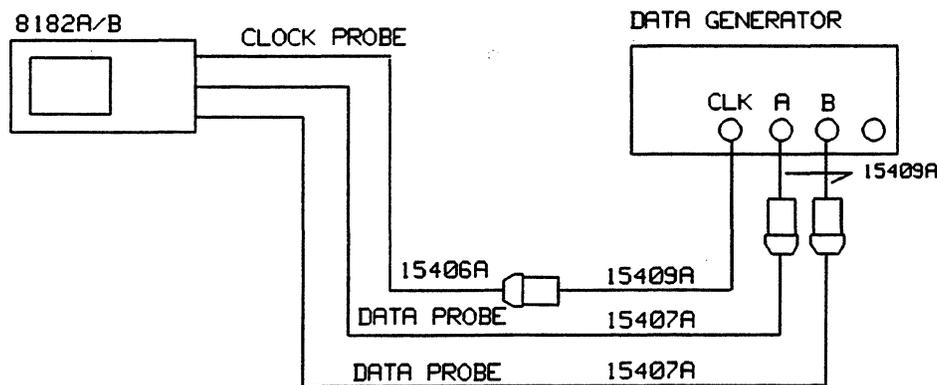


Figure 12-1. Test Setup for the Trigger Word and Operating Mode Test

Trigger Word and Operating Modes Tests

Equipment Required

Data generator	HP 8018A
Plug-on BNC Adapter (3 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A

Procedure

Set the 8018A as follows:

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int.Clock	Amplitude	2.5V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm

1. Clear both 8018A Data Channels by selecting the channel and pressing the toggle switch to Channel Clear.
2. Select Word Address 01 and load bit 1 to high in channel A and channel B.
3. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, **Rec. Std. Set**, **EXECUTE**)
4. Clear Word Mask; Clear Data.
(PAGES, EXPECTED DATA, **Edit**, **Clear & Set**, **Clr Word Mask**, **EXECUTE**, **Clr Data**, **EXECUTE**)
5. Clock Delay 5 ns.
(PAGES, CONTROL, **Clock**, **Clock Delay**, 5, **NANOSEC**)
6. Autoarming Delay 1s.
(PAGES, CONTROL, **Autoarming**, **DELAY 1s**)
Set Stop Delay to 1023.
(PAGES, CONTROL, **Stop**, **Stop Delay**, 1023, **ENTER**)
7. Error Map; Trigger Word in Softkey Area.
(PAGES, Error Map, SOFTKEYS, CONTROL, **Trigger**, **Trigger Word**)
8. Connect the equipment as shown in Figure 12-1 and press RUN.

Trigger Start Analysis Test

With Trigger Word set to X (don't care) a single sporadic error should be displayed on the Error Map.

9. Set the Trigger Word for both connected data channels to 1.
The Error Map should display only the Trigger Word in address 00000 as an error.
10. Set Trigger Word for one data channel to 0.
The 8182A/B should switch to ARMED (no trigger recognition).
11. Set the Trigger Word back to 1 and the 8182A/B should trigger again.
12. Set the Trigger Word for the second channel to 0 and 1 and check Trigger Word recognition as described in steps 8 to 10.

Trigger Word and Operating Modes Tests

Trigger Stop Analysis Test

13. Program 8182A/B to Trigger Stop Analysis.
(PAGES, **CONTROL** , **Operatg Mode** , **Trg Stop Anal**)
14. Error Map; Trigger Word in the Softkey Area.
(PAGES, **Error Map** , SOFTKEYS, **CONTROL** , **Trigger** , **Trigger Word**)

With Trigger Word 1 for both connected data channels, the error display should stop always at address -00000 (the Trigger Word at address -00000 is indicated as error).
15. Set the Trigger Word for one connected channel to 0.
The 8182A/B should stay in ACTIVE (no trigger).
16. Set the Trigger Word back to 1.
The 8182A/B should trigger again.
17. Set the Trigger Word for the second connected data channel to 0 and 1 and check Trigger Word recognition as described in steps 14 to 16.

Trigger Event Start Compare Test

18. Program 8182A/B to Trigger Event Start Compare.
(PAGES, **CONTROL** , **Operatg Mode** , **Trg Strt Comp** , **EXECUTE**)
19. Select Error Map.
(PAGES, **Error Map**)

The error display should show the Trigger Word indicated as error at address 1023 (caused by Trigger Delay 00001) and errors in the channel marking display for both connected data channels.
20. Program Trigger Start Analysis and Trigger Delay 0.
(PAGES, **CONTROL** , **Operatg Mode** , **Trg Strt Anal** , **EXIT** ↑ , **Trigger** , **Trg Delay** , 0, **ENTER NUMBER**)
21. Repeat the procedure starting with step 5 for the remaining data channel pairs.

Trigger Delay and Stop Delay Tests

12-3 Trigger Delay and Stop Delay Tests

Description

This test is to be performed with any one of the available channels to check the Trigger Delay and Stop Delay Functions. A data generator is used to generate the Trigger Word. The Trigger Word for unused data channels must be set to don't care (X).

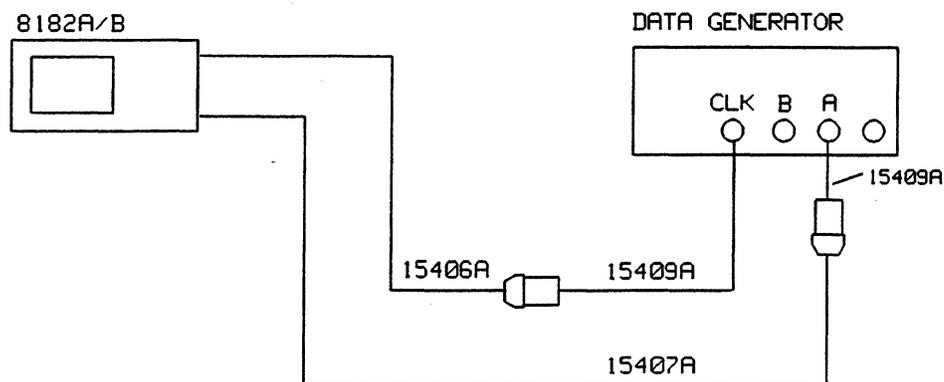


Figure 12-2. Test Setup for the Trigger Delay and Stop Delay Test

Equipment

Data Generator	HP 8018A
Plug-on BNC Adapter (2 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A

Procedure

Set the 8018A as follows:

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int. Clock	Amplitude (A)	2.5 V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm

1. Clear 8018A channel A data by selecting channel A and pressing the toggle switch to Channel Clear position.
2. Select Word Address 01 and load bit 1 to high.
3. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
4. Clear Word Mask; Clear Data.
(PAGES, EXPECTED DATA, Edit, Clear & Set, Clr Word Mask, EXECUTE, Clr Data, EXECUTE)
5. Set Clock Delay to 5ns.
(PAGES, CONTROL, Clock, Clock Delay, 5, NANOSEC)

Trigger Delay and Stop Delay Tests

6. Set Autoarming Delay to 1s; Set Stop Delay to 1023
(PAGES, **CONTROL** , **Autoarming** , **Delay 1 s**)
(PAGES, **CONTROL** , **Stop** , **Stop Delay** , 1023, **ENTER**)
7. Connect the equipment as shown in Figure 12-2 and press RUN.
8. Set the Trigger Word to I for the connected data probe (all other channels to X, don't care)
(PAGES, **CONTROL** , **Trigger** , **Trigger Word** , I)
9. Error Map; Trigger Delay in Softkey Area.
(PAGES, **Error Map** , SOFTKEYS, **CONTROL** , **Trigger** , **Trig Delay**)

Trigger Delay Test

10. Increase Trigger Delay by pressing **INCREMENT** , and check that the displayed error moves backwards from address 1023 (for Trg Delay 1) with increasing delay setting.
11. Set Trigger Delay back to 00000.

Stop Delay Test

12. Select Stop Delay in the Softkey Area and set Stop Delay to 1023/16383.
(SOFTKEYS, **CONTROL** , **Stop** , **Stop Delay** , 16383, **ENTER NUMBER**)
13. Check that the Stored Words displayed in the upper right hand corner of the 8182A/B display indicates 1024/16384. Vary the Stop Delay and check that the Stop Delay setting + 1 is displayed as Stored Words in the upper right hand corner of the 8182A/B display.

Sampling Point Accuracy and Skew Tests

12-4 Sampling Point Accuracy and Skew Tests

Specification

Sampling point accuracy: $\pm 5\%$ of set Clock Delay ± 1 ns.

Channel skew: ≤ 2 ns.

Description

The test setup uses a pulse generator as clock and data source for the 8182A/B Data Analyzer. The data is delayed by a fixed 3 ns delay line. Setting the 8182A/B Clock Delay to 3 ns then corresponds to zero delay between clock and data. The clock can now be advanced by 3 ns and delayed with respect to the data to check when the incoming data signal is recognized as a high or a low level.

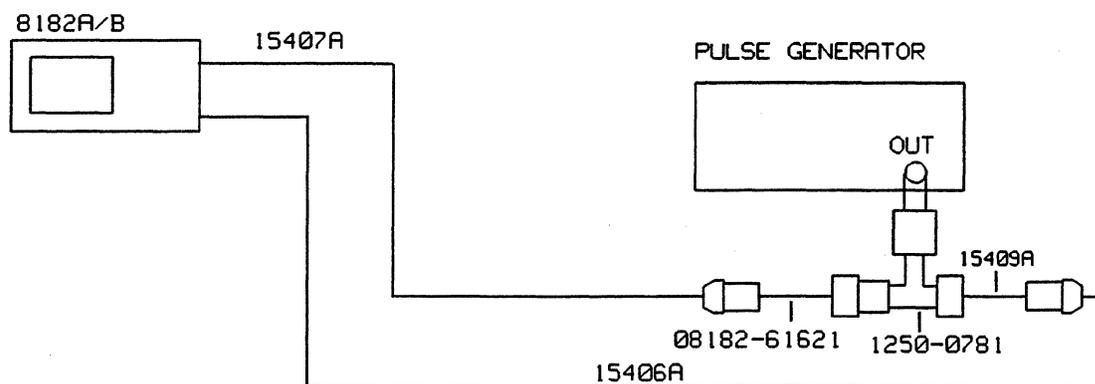


Figure 12-3. Test Setup for the Sampling Point Accuracy and Skew Test

Equipment

Pulse Generator	HP 8007B
BNC Tee	1250-0781
Plug-on BNC Adapter (2 off)	HP 15409A
Clock Probe Assembly	HP 15406A
Data Probe Assembly	HP 15407A
Delay Line (including 50 Ω) 3 ns	08182-61621

Procedure

1. Set Pulse Generator as follows:

Period:	1 μ s
Pulse Width:	0.5 μ s
Leading Edge:	< 3 ns
Trailing Edge:	< 3 ns
Amplitude High Level:	+2V into 50 Ω
Low Level:	0V

2. Program 8182A/B Standard Set.

(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)

3. Set Clock Threshold to +1V.

(PAGES, CONTROL, Clock, Clock Thres, 1, VOLT)

4. Set Threshold Label A to +1 V.

(PAGES, Input, Threshold, 1, VOLT)

Sampling Point Accuracy and Skew Tests

5. Set Stop Delay to 40.
(PAGES, **CONTROL** , **Stop** , **Stop Delay** , 40, **ENTER NUMBER**)
6. Set Autoarming Delay to 0 s.
(PAGES, **CONTROL** , **Autoarming** , **DELAY 0s**)
7. Select the Timing Diagrams Page.
(PAGES, **TIMING-DIAGR**)
8. Press SOFTKEYS, **CONTROL** , **Clock** , **Clock Delay** , 3, **NANOSEC**)
9. Connect the equipment as shown in Figure 12-3 and press **RUN**. (Start with Connector 0 Channel 0.)
10. Using **INCREMENT** , check that the displayed timing signal switches from low to high within 2 to 4 ns of the Clock Delay setting.
11. Set the Clock Slope to Negative.
(PAGES, **CONTROL** , **Clock** , **Clock Slope** , **NEG.SLOPE** , **EXIT** , **↑↑** , **Clock Delay**)
12. Increment the Clock Delay starting from 2 ns and check that the timing signal switches from high to low within 2 to 4 ns of the Clock Delay setting.
13. Repeat the Skew Test for Positive Clock Slope and Negative Clock Slope for the remaining channels as described in steps 10 to 12.

When checking skew from connector 3 channel 0 upwards, move the vertical display window.
(PAGES, **TIMING-DIAGR** , **Select Displ** , **Vertical Window** , **←** [until the required channels are displayed])

Clock Delay Test

12-5 Clock Delay Test

Specification

$\pm 5\%$ of set Clock Delay $\pm 1\text{ns}$.

Description

The test setup uses a pulse generator as an external clock source. The Clock Delay is measured at the 8182A/B clock output referenced to 0.00ns programmed Clock Delay.

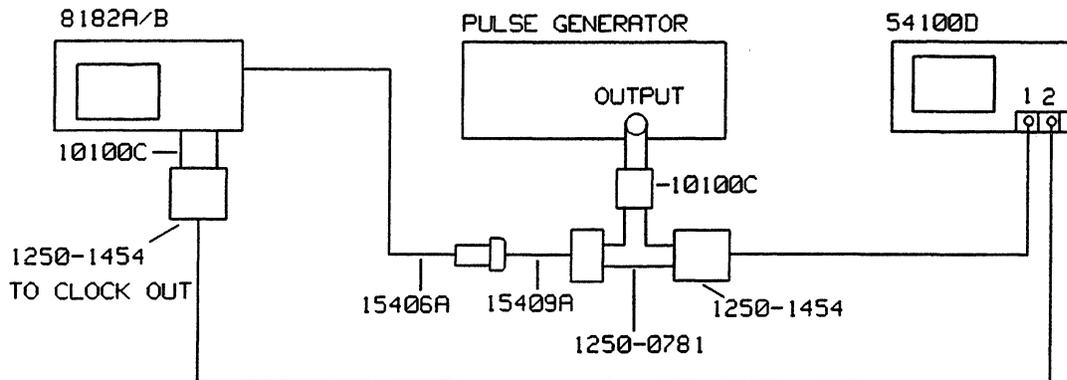


Figure 12-4. Test Setup for the Clock Delay Test

Equipment

Pulse Generator	HP 8007B
Scope	HP 54100D
Active scope Pods	HP 54001A
BNC Tee Adapter	1250-0781
50 Ohm Feedthrough	HP 10100C
BNC scope Probe Adapter	1250-1454
BNC Adapter	HP 15409A
Clock Probe	HP 15406A

Procedure

1. Cancel out channel to channel skew and the Trigger Delay of channel 2.
Set the Pulse Generator as follows:

Period:	110 μs
Pulse Width:	1.5 μs
Transition Time:	2 ns
Amplitude LOL:	0 V
(into 50 Ohm) HIL:	2.5 V
Offset:	OFF
2. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
3. Set Clock Threshold to +1.2V; Set Clock Delay to 0.00ns.
(PAGES, CONTROL, Clock, Clock Thres, 1.2, VOLT, EXIT, Clock Delay, 0, NANOSEC)

Clock Delay Test

4. Connect the equipment as shown in Figure 12-4.
5. Set the scope as follows:
(Autoscale > Trigger > Trigger Src to Chan 2 > Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF)
6. Center the 50% point of the positive going transition of the displayed clock pulse on the center graticule.
(Timebase > Sec/Div > Ins > Delay > Knob)
7. Set the Start Marker to the 50% point of the displayed transition.
(Delta > Tmarkers to ON > Start Marker > Knob)
8. Using **INCREMENT**, step through the delay range of 0.00ns to 10.00 ns in 100 ps steps and check the accuracy.

The position of the Start Marker is the reference for the following measurements and must therefore not be moved.

9. Program 8182A/B Clock Delay as listed in Table 12-1 and check that accuracy is in the range $\pm 5\%$ ± 1 ns.

Example: Zero delay between scope input Channel 1 and Channel 2 = 38 ns
Programmed Clock Delay = 21.9 ns

Set scope Timebase delay to 60 ns and position the Stop Marker to the 50% point of the displayed transition. Perform a delta t reading; the reading should be in the following range:

Delta t min = 19.8 ns
Delta t max = 24.0 ns

Table 12-1. Clock Delay Test Values

Set Delay	Delta t min.	Delta t max.
21.9 ns	19.8 ns	24.0 ns
22.0 ns	19.9 ns	24.1 ns
70.0 ns	65.5 ns	74.5 ns
117.0 ns	110.2 ns	123.9 ns
118.0 ns	111.1 ns	124.9 ns
500.0 ns	474.0 ns	526.0 ns
1.01 us	0.96 us	1.06 us
1.02 us	0.97 us	1.07 us
5.00 us	4.75 us	5.25 us
9.99 us	9.49 us	10.49 us
10.0 us	9.50 us	10.5 us
50.0 us	47.5 us	52.5 us
99.9 us	94.9 us	104.9 us

Compare Window Width Test

12-6 Compare Window Width Test

Specification

Compare window width accuracy $\pm 5\%$ of set value ± 1 ns.

Description

The test setup uses a pulse generator as an external clock source. Analyzer Clock Delay is measured at the 8182A/B Clock Output referenced to 0.00 ns programmed Clock Delay. Ranges up to 10 ns are measured with an oscilloscope. A time interval counter is used for higher ranges. A time offset is programmed on the counter in order to compensate for internal and cable delays, instead of adding these delays manually.

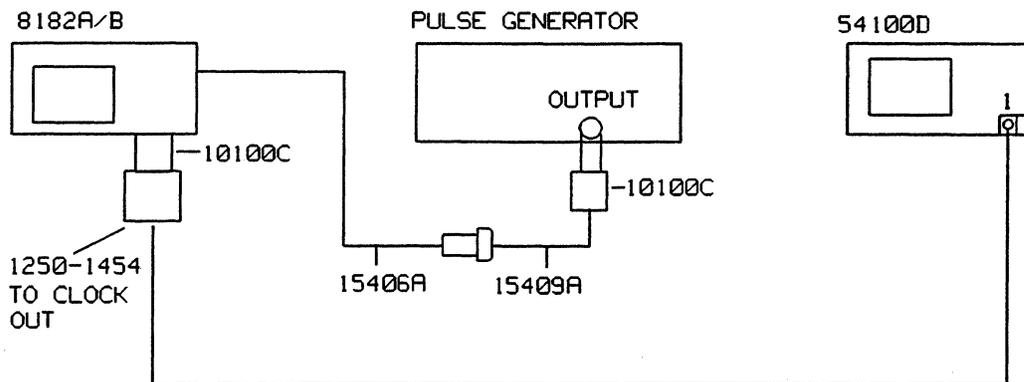


Figure 12-5. Test Setup for the Compare Window Width Test

Equipment

Scope	HP 54100D
Active scope Pods	HP 54001A
Pulse Generator	HP 8007B
Clock Probe Assy	HP 15406A
BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 10100C
Scope Probe Adapter	1250-1454

Procedure

Before performing this measurement cancel out the Trigger Delay of scope channel 1.

- Set the Pulse Generator as follows:
Period: 1 μ s
Pulse Width: 0.5 ns
Transition Time: 2 ns
HIL: 2.5 V
LOL: 0.0V
- Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
- Select Trigger Event Start Compare.
(PAGES, CONTROL, Operatg Mode, Trg-Strt-Comp, EXECUTE)

Compare Window Width Test

4. Set the Clock Width to 10ns.
(PAGES, **CONTROL**, **Clock**, **Clock Width**, 10, **NANOSEC**)
5. Connect the equipment as shown in Figure 12-5.
6. Set the scope as follows:
(Autoscale > Timebase > Sec/Div > 500ps > Trigger > Trigger Src to Chan 1 > slope to pos)
7. Adjust the 50% point of the positive going transition to lie on the center horizontal graticule line.
(Chan 1 > Offset > Knob)
8. Move the Start Marker to the 50% point of the displayed transition.
(Delta t > Tmarkers to ON > Start Marker > Knob)

Note: The Start Marker is the reference for the following measurements and must therefore not be moved.

9. Set the scope timebase delay to 10ns.
(Timebase > Delay > 10ns)
10. Set the Stop Marker to the 50% point of the negative going transition and read delta t (Delta t > Stop Marker > Knob)

Delta t must be in the following range:

Delta t min: 8.5 ns
Delta t max: 11.5 ns

11. Check linearity by incrementing the clock width in 100 ps steps up to 20 ns.
12. Check the Clock Width at the settings given in Table 12-2.

Table 12-2. Clock Width Test Values - Clock Period at 1 μ s

Set Width	Max. Width	Min. Width
29.9 ns	27.4 ns	32.4 ns
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105.0 ns
100.0 ns	94.0 ns	106.0 ns

13. Change pulse generator period to 120 ms and repeat step 12 using the values in Table 12-3.

Table 12-3. Clock Width Test Values - Clock Period at 120 ms

Set Width	Max. Width	Min. Width
300.0 ns	284.0 ns	316.0 ns
999.0 ns	948.0 ns	1050.0 ns

Compare Window Width Test

14. Increase the number of averages to 256 and repeat step 12 using the values in Table 12-4.
(Display > Number of Averages > to 256)

Table 12-4. Clock Width Test Values - Averaging at 256

Set Width	Max. Width	Min. Width
100.0 ms	95.0 ms	105.0 ms

12-7 Clock Threshold and Hysteresis Tests

Specification

Threshold accuracy: $\pm 2\%$ of set value $\pm 10\text{mV}$.

Hysteresis: $< \pm 50\text{mV}$.

Description

The pulse generator is adjusted to generate a triangular waveform with a period of 1 ms. This signal is fed into the CLOCK input of the 8182A/B. When the 8182A/B clock threshold is reached the 8182A/B generates a clock pulse, which is available at its Clock Output. This clock pulse triggers a trace on the oscilloscope. The vertical offset from zero volts corresponds exactly to the level where the 8182A/B recognises a clock signal.

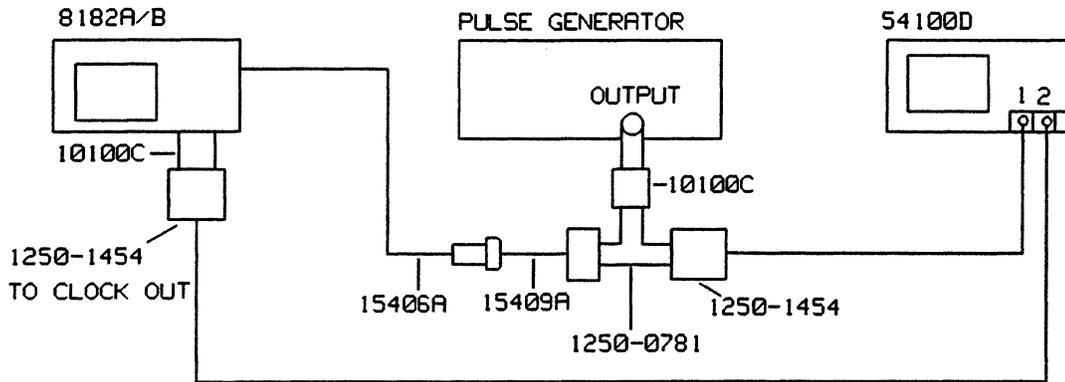


Figure 12-6. Test Setup for the Clock Threshold Hysteresis Test

Equipment

Scope	HP 54100D
Active scope Pods	HP 54001A
Pulse Generator	HP 8007B
BNC Tee Adapter	1250-0781
Scope Probe Adapter	1250-1454
50 Ohm Feedthrough	HP 10100C
Clock Probe	HP 15406A
BNC Adapter	HP 15409A

Procedure

1. Set the pulse generator as follows:

Period:	1 ms
Width:	0.5 ms
Transition Time:	5 μs to 250 μs
Amplitude:	4V pp into 50 Ω
Offset:	ON
2. Adjust the leading and trailing edges for a triangle waveform on the scope.
3. Using the pulse generator offset vernier, set the waveform symmetrical to 0V graticule line.

Clock Threshold and Hysteresis Tests

Hysteresis Test

4. Program 8182A/B to Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
5. Clock Slope Positive; Threshold 0.00V.
(PAGES, CONTROL, Clock, Clock Slope, POS SLOPE, EXIT ↑↑, Clk Threshold, 0, VOLT)
6. Connect the equipment as shown in Figure 12-6.
7. Set the scope as follows:
(Autoscale > Trigger> Trig Src to Chan 2 > Display > Split Screen to OFF > Chan 2 > Chan 2 Display to OFF > Timebase > Sec/Div > 500ns > Chan 1 > Volts/DIV > 100mV > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV > Delta V > V Markers to ON > Marker 1 Position > Knob)
8. Position the Marker to the point where the transition crosses the vertical graticule line and read V(1).
 $V(1) \leq +50\text{mV}$.
9. Change to negative Clock Slope.
(EXIT ↑↑, Clock Slope, NEG SLOPE)
Move V Marker 1 to the crossing point and read V(1)
 $V(1) \leq -50\text{mV}$

Threshold Test

10. Set the threshold to -1.4V.
(EXIT ↑↑, Clock Thres, 1.4, VOLT)
11. Set the scope as follows.
(Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > -1.2 V > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV/DIV > Offset > -1.400V > Delta V > V markers to ON > Marker 1 Position > Knob)
12. Move Marker 1 to the crossing point where the displayed transition meets the vertical graticule line and read V(1)
 $V(1) \text{ min: } -1.49 \text{ V}$
 $V(1) \text{ max: } -1.31 \text{ V}$
13. Set Clock Slope to positive; Set Clock Threshold to +1.4V.
(EXIT ↑↑, Clock Slope, POS SLOPE, EXIT ↑↑, Clock Thres, 1.4, VOLT)
14. Set the scope as follows:
(Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > 1.200 V > Chan 1 Mode to Magnify > Magnify to ON > Volts/DIV > 20mV > Offset > 1.400V)
15. Move V Marker 1 to the point where the transition crosses the vertical graticule line
(Delta V > Vmarker to ON > Marker 1 Position > Knob)
16. Read V(1). V(1) must be in the range of:
 $V(1) \text{ min: } 1.31\text{V}$
 $V(1) \text{ max: } 1.49\text{V}$

12-8 Data Threshold Level Accuracy and Linearity Tests

Specification

Single threshold accuracy: $\pm 2\%$ of set value ± 10 mV.
 Level detection accuracy 50 ms
 after input signal transition: actual threshold = ± 15 mV.

Description

This test is used to measure the high and low level detection voltage to determine the actual threshold voltage. The check-sequence is selected to ensure that all data lines used for level programming are working properly. To get a better resolution when adjusting the power supply, two 20 dB attenuators are used to reduce the output voltage. 20 W attenuators are recommended to avoid damage to the rest of the equipment. The capacitor across the DVM input suppresses spikes generated by the DVM.

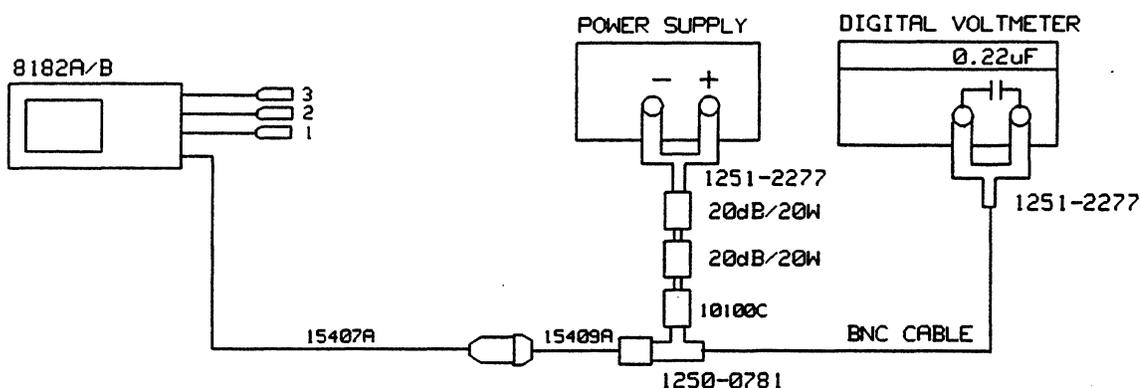


Figure 12-7. Test Setup for the Data Threshold Level Accuracy and Linearity Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
Plug-on BNC Adapter	HP 15409A
Data Probe Assy.	HP 15407A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
50 Ohm Feedthrough	HP 10100C
Capacitor	0.22 uF
2 x Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
Cable Assembly BNC to BNC	HP 11170C

Procedure

1. Program 8182A/B Standard Set.
 (PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Clock Source Internal.
 (PAGES, CONTROL, Clock, Clock Source, INTERNAL)
3. Select Autoarming Delay of 0s.
 (PAGES, CONTROL, Autoarming, DELAY 0s)

Data Threshold Level Accuracy and Linearity Tests

4. Set Stop Delay to 40.
(PAGES, **CONTROL**, **Stop**, **Stop Delay**, 40, **ENTER NUMBER**)
5. Set Channel Configuration to Connector 0 Channel 0.
(PAGES, **Input**, **Chnl. Config**, **DELETE CHNL** [until only connector 0 channel 0 is displayed])
6. Select Timing Diagrams; Select Single Threshold Label A in the Softkey Area.
(PAGES, **TIMING DIAGR**, **SOFTKEYS**, **Input**, **Threshold**, [**Next Label** if necessary])
7. Set Single Threshold of Label A to +0.01 V.
(.01, **VOLT**)



Set power supply voltage to minimum. Do not overload attenuators.

8. Connect the equipment as shown in Figure 12-7 and press RUN.
9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).
10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).
Level Detection Accuracy (Va - Vb) must be better than 30 mV.
Actual Threshold (Va + Vb)/2 must be within ±2% of the set value ±10 mV.

Example: Programmed Threshold = +0.01 V
 High Level Voltage (measured in step 9) = +0.012 V
 Low Level Voltage (measured in step 10) = +0.009 V
 Level detection accuracy = (0.012 V - 0.009 V) = 0.003 V
 Limit = <0.03 V
 Single threshold accuracy = (0.012V + 0.009 V)/2 = 0.011 V
 Limit = 0.00 V to 0.02 V

13. Program the thresholds given in Tables 12-5, 12-6 and 12-7, and check for specifications as described in step 10.

Table 12-5. Threshold Level Accuracy and Linearity Test - All Attenuators in Place

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy		
				Min.	Actual	Max.
0.01 VVVV	0.000V	0.020V
0.02 VVVV	0.010V	0.030V
0.04 VVVV	0.020V	0.050V
0.08 VVVV	0.068V	0.092V
0.16 VVVV	0.147V	0.173V

Data Threshold Level Accuracy and Linearity Tests

Table 12-6. Threshold Level Accuracy and Linearity Test - One 20 dB Attenuator Removed

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy		
				Min.	Actual	Max.
0.32 VVVV	0.304V	0.336V
0.64 VVVV	0.617V	0.663V
1.28 VVVV	1.244V	1.316V
2.56 VVVV	2.499V	2.621V

Table 12-7. Threshold Level Accuracy and Linearity Test - Both Attenuators and 50 Ω Feedthrough Removed

Set Thres.	Hi Level Va	Lo Level Vb	Delta V	Threshold Accuracy		
				Min.	Actual	Max.
5.12 VVVV	5.008V	5.232V

12-9 Data Offset and Gain Tests

Specification

Single threshold accuracy: $\pm 2\%$ of set value ± 10 mV.
 Level detection accuracy 50 ms
 after input signal transition: actual threshold = ± 15 mV.

Description

To determine the actual threshold and to check the threshold accuracy, the hysteresis between high and low level detection voltages must be measured first. The actual threshold is midway between high and low level detection voltages. This value must be within the specifications for single threshold.

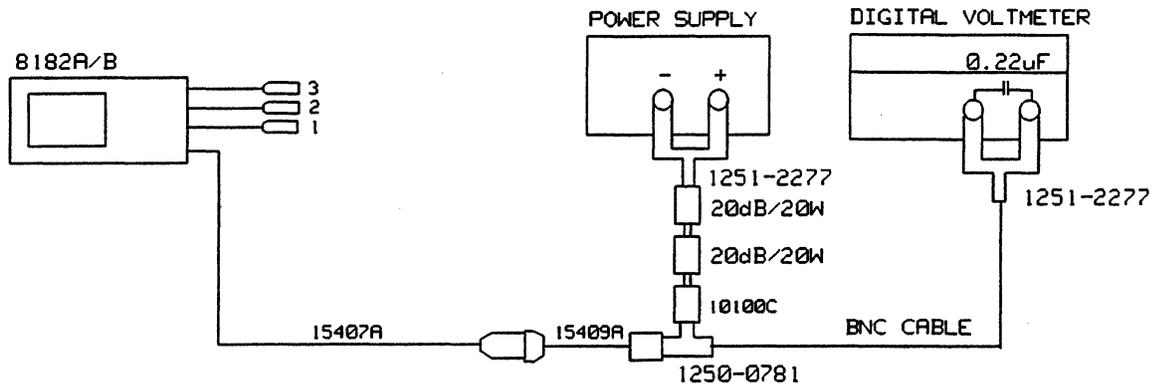


Figure 12-8. Test Setup for the Data Offset and Gain Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
Plug-on BNC Adapter	HP 15409A
Data Probe Assy.	HP 15407A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
50 Ohm Feedthrough	HP 10100C
Capacitor	0.22 uF
2 x Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
Cable Assembly BNC to BNC	HP 11170C

Positive Offset Test

1. Program 8182A/B Standard Set.
 (PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Set Clock Source to Internal.
 (PAGES, CONTROL, Clock, Clock Source, INTERNAL)
3. Set Autoarming Delay to 0s.
 (PAGES, CONTROL, Autoarming, DELAY 0s)
4. Set Stop Delay to 40.
 (PAGES, CONTROL, Stop, Stop Delay, 40, ENTER NUMBER)

Data Offset and Gain Tests

- Set Channel Configuration to Connector 0 Channel 0.
(PAGES, **Input** , **Chnl Config** , **DELETE CHNL** [until only connector 0 channel 0 is displayed])



Set power supply voltage to minimum. Do not overload attenuators.

- Set Single Threshold Label A to +0.05 V.
(PAGES, **Input** , **Threshold** , **Next Label** [if necessary] .05, **VOLT**)
- Select Timing Diagrams Report; Channel Configuration in Softkey Area.
(PAGES, **TIMING DIAGR** , **SOFTKEYS**, **Input** , **Chnl Config**)
- Connect the equipment as shown in Figure 12-8 and press RUN.
- Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).
- Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).

Level Detection Accuracy ($V_a - V_b$) must be less than 30 mV.
Actual Threshold $(V_a + V_b)/2$ must be within $\pm 2\%$ of set value $\pm 10\text{mV}$.

Example: Programmed Threshold = 0.05 V
 High Level Voltage (measured in step 9) = 0.056 V
 Low Level Voltage (measured in step 10) = 0.043 V
 Level detection accuracy = $0.056\text{ V} - 0.043\text{ V} = 0.013\text{ V}$
 Limit: < 0.03 V
 Single thresh. accuracy = $(0.056\text{ V} + 0.043\text{ V})/2 = 0.050\text{ V}$
 Limit: 0.039V to 0.061V

- Select the connector and channel to be tested by pressing first the connector number and then the channel number on the data entry key pad. Connect in turn all data probes to the test setup and check for $+50\text{ mV} \pm 10\text{ mV}$ threshold accuracy.

Negative Offset Test

- Change power supply polarity to negative and program the 8182A/B as follows:
- Set Label A Single Threshold to -0.05 V.
(SOFTKEYS, **Input** , **Threshold** , -.05, **VOLT**)
- Select Channel Configuration.
(SOFTKEYS, **Input** , **Chnl Config**)
- Proceed as described for the Positive Offset Test and check all channels for $-50\text{ mV} \pm 10\text{ mV}$ threshold accuracy.

Gain Test (Negative)

- Remove both 40 dB attenuators and the 50 Ohm feedthrough from the test setup and set the power supply voltage to -9.00 V (reading on DVM).

Data Offset and Gain Tests

19. Program Standard Channel Configuration.
(PAGES, **Input**, **Chnl Config**, **Std Config**, **EXECUTE**)
20. Select Timing Diagrams; Select Single Threshold Label A in the Softkey Area.
(PAGES, **TIMING DIAGR**, SOFTKEYS, **Input**, **Threshold**, [**Next Label** if necessary])
21. Set the threshold to -8.81 V and check that the corresponding timing display is low. (-8.81, **VOLT**)
22. Set the threshold to -9.19 and on pressing **VOLT**, the timing display should jump to high.
23. Repeat step 21 and 22 for all data channels.

Gain Test (Positive)

24. Change power supply voltage to +9.00 V.
25. Set the threshold to +8.81 V and check that the corresponding timing display is high. (8.81, **VOLT**)
26. Set the threshold to +9.19 and on pressing **VOLT**, the timing display should jump to low.
27. Repeat step 25 and 26 for all data channels.

Note: When testing channels at connectors 3 to 7, move the timing diagrams display up:
(PAGES, **TIMING DIAGR**, **Select Displ**, **Vert Window**, **←** or **→** [until required connectors are displayed], SOFTKEYS, **Input**, **Threshold**)

Qualifier Threshold and Impedance Tests

12-10 Qualifier Threshold and Impedance Tests

Specification

Threshold accuracy: $\pm 3\%$ of set value $\pm 50\text{mV}$.

Description

This test is used to measure the high and low level detection voltage (hysteresis) to determine the actual threshold voltage of the Qualifier Inputs (TTL setting). By measuring the voltage drop across the 20dB attenuator when switching the input to 50Ω , proper input impedance selection can be verified.

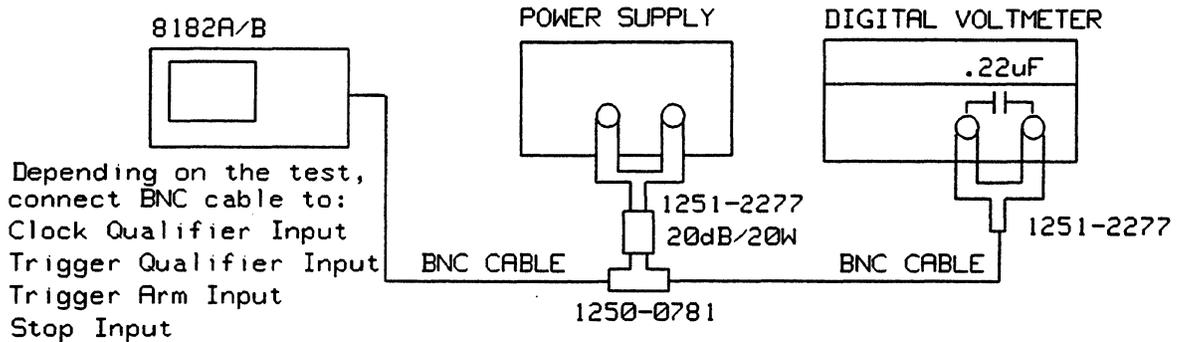


Figure 12-9. Test Setup for the Qualifier Threshold and Impedance Test

Equipment

DC Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
BNC - Tee	1250-0781
BNC (f) to dual banana Plug (2 off)	1251-2277
Capacitor	0.22 uF
Attenuator 20 dB (20W)	(e.g. Texscan HFP 50/20)
2x Cable Assembly BNC to BNC	HP 11170C

Clock Qualifier Threshold Accuracy Test

1. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Set Clock Source to Internal.
(PAGES, CONTROL, Clock, Clock Source, INTERNAL)
3. Set Autoarming Delay to 0s.
(PAGES, CONTROL, Autoarming, DELAY 0s)
4. Set Clock Qualifier to High Level; Set Threshold to +1.4V.
(PAGES, CONTROL, Clock, Clock-Qual, Level, HIGH LEVEL, EXIT, Threshold, 1.4, VOLT)
5. Connect the equipment as shown in Figure 12-9 and press RUN.
6. Increase power supply voltage slowly until a clock signal is just indicated in the upper left hand corner of the display and note the DVM reading.

Qualifier Threshold and Impedance Tests

7. Decrease the power supply voltage slowly until the clock indication just disappears and note the DVM reading.
Result: The mean value should be between +1.31V and +1.49V.
8. Change power supply polarity and set 8182A/B threshold to -1.40V.
9. Increase power supply voltage slowly until the clock indication just disappears and note the DVM reading.
10. Decrease power supply voltage slowly until a clock signal is just indicated and note the DVM reading.
Result: The mean value should be between -1.31V and -1.49V.

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.40V reading on the DVM.
12. Set the Clock Qualifier Input Impedance to 50Ω.
(EXIT , Impedance , 50 Ω)

The DVM should show approximately -0.7 V.

12-11 Trigger Qualifier Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Clock Source Internal.
(PAGES, CONTROL, Clock, Clock Source, INTERNAL)
3. Set Autoarming Delay to 0s.
(PAGES, CONTROL, Autoarming, DELAY 0s)
4. Trigger Qualifier High Level; Threshold +1.4V.
(PAGES, CONTROL, Trigger, Trg Qualifier, Level, HIGH LEVEL, EXIT ↑↑↑, Threshold)
5. Connect the equipment as shown in Figure 12-9 and press RUN.
6. Increase power supply voltage slowly until the status display in the upper right hand corner of the display jumps just from ARMED to IDLE (IDLE toggles) and note the DVM reading.
7. Decrease power supply voltage slowly until the display just jumps to ARMED and note the DVM reading.
Result: The mean value should be between +1.31V and +1.49V
8. Change power supply polarity and set 8182A/B threshold to -1.40V.
9. Increase power supply voltage slowly until the display just jumps from IDLE to ARMED and note the DVM reading.
10. Decrease power supply voltage slowly until the display just jumps back to IDLE and note the DVM reading.
Result: The mean value should be between -1.31V and -1.49V

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.4 V reading on the DVM.
12. Program Triger Qualifier Input Impedance to 50Ω.
(EXIT ↑↑↑, Impedance, 50 Ω)

The DVM should show approximately - 0.7V.

Trigger Arm Threshold Accuracy Tests

12-12 Trigger Arm Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Set Clock Source to Internal; Set Clock Period to 1s.
(PAGES, CONTROL, Clock, Clock Source, INTERNAL, EXIT ↑↑, Clock Period Increase [until 1 s is displayed])
3. Set Stop Delay (Internal) to 0.
(PAGES, CONTROL, Stop, Stop Delay, 0, ENTER NUMBER)
4. Set Autoarming Delay to 0s.
(PAGES, CONTROL, Autoarming, DELAY 0s)
5. Set Trigger Arm Slope to Positive (Threshold is +1.40).
(PAGES, CONTROL, Trigger, Trigger Arm, Slope, POS SLOPE)
6. Connect the equipment as shown in Figure 12-9 and press RUN.
7. Increase power supply voltage slowly until the 8182A/B switches from ARMED to ACTIVE (upper right hand corner of display).

NOTE

Continuous toggling may be caused by noise when the threshold level has just been reached.

The DVM reading should be between +1.31 V and +1.49 V.

8. Set Trigger Arm Slope to Negative; Set Threshold to -1.4 V.
(POS SLOPE, EXIT ↑↑↑, Threshold, -1.4, VOLT)
9. Change power supply polarity, press RUN and increase power supply voltage slowly again until the 8182A/B switches from ARMED to ACTIVE. (See Note above.)

The DVM reading should be between -1.31 V and -1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40 V reading on the DVM.
11. Set Trigger Arm Input Impedance to 50Ω.
(EXIT ↑↑↑, Impedance, 50 Ω)

The DVM should show approximately -0.7 V.

External Stop Threshold Accuracy Tests

12-13 External Stop Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
(PAGES, MISCELLANEOUS, Recall, Standard Set, EXECUTE)
2. Set Clock Source to Internal; Set Clock Period to 100ms.
(PAGES, CONTROL, Clock, Clock Source, INTERNAL, EXIT ↑↑, Clock Period. Increase [until 100ms is displayed])
3. Set Stop Delay (Internal) to 0.
(PAGES, CONTROL, Stop, Stop Delay, 0, ENTER NUMBER)
4. Set Autoarming Delay to 1s.
(PAGES, CONTROL, Autoarming, DELAY: 1s)
5. Set External Stop to Positive Slope (Threshold is +1.40).
(PAGES, CONTROL, Stop, Stop Slope, POS SLOPE)
6. Connect the equipment as shown in Figure 12-9 and press RUN.
7. Increase power supply voltage slowly until the 8182A/B switches from ACTIVE to IDLE (upper right hand corner of display).

NOTE

Continuous toggling may be caused by noise when the threshold level has just been reached.

The DVM reading should be between +1.31V and 1.49V.

8. Program Negative Slope; Threshold -1.4 V.
(NEG SLOPE, EXIT ↑↑, Stop Thres, -1.4, VOLT)
9. Change power supply polarity, press RUN and increase power supply voltage again until the 8182A/B switches from ACTIVE to IDLE. (See the Note above.)

The DVM reading should be between -1.31V and 1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40V reading on the DVM.
11. Set External Stop Input Impedance to 50Ω.
(Stop Imp, 50 Ω)

The DVM should show approximately -0.7V.

Appendix A

Generator Parameters After Recall Standard Set

Control Page

First Address:	00000	Last Address:	1023/16383
Cycle Mode:	AUTO	Strobe Breaks:	OFF
Clock Source:	INTERNAL	Clock 1 in Break:	OFF
Input Impedance:	50 g	Input Threshold:	+0.0 V
Run Input:	OFF	Stop Input:	OFF
Break Input:	OFF	Strobe Output:	DATA
Outputs:	OFF		

Timing Page

Clock Frequency:	10.0 MHz	Clock Period:	100 ns
Clock 1 Delay:	0.00 ns	Clock 1 Format:	RZ
Clock 1 Width:	40.0 ns	Clock 2 Delay:	50.0 ns
Clock 2 Format:	RZ	Clock 2 Width:	10.0 ns
Timing Channels Format:	NRZ	Timing Channels Delay:	00.0 ns

Output Page

Load Impedance:	50 Ohms	Outputs:	OFF
Clock 1 Assigned Label:	A	Clock 1 Polarity:	NORMAL
Clock 2 Assigned Label:	A	Clock 2 Polarity:	NORMAL
Strobe Levels:	ECL	Strobe Polarity:	NORMAL
Label A High Level:	+0.25 V	Label A Low Level:	-0.25 V
Label B High Level:	+5.00 V	Label B Low Level:	+0.00 V
Label C High Level:	-0.80 V	Label C Low Level:	-1.80 V
Label D High Level:	+2.40 V	Label D Low Level:	+0.80 V
Channel Configuration:			
Polarity of all Channels is NORMAL.		All Fitted Connectors are displayed.	
Label A Assigned to all Channels.		Each Segment contains a Single Connector.	

Data Page

Segment Code Entry:	BINARY	Data Entry:	YES
Memory Contents not Affected.			

Appendix A

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Appendix B

Analyzer Parameters After Recall Standard Set

Control Page

Glitch Detect:	OFF	Operating Mode:	TRIG. STRT. ANAL.
Clock Source Input Slope:	POSITIVE	Clock Source:	EXTERNAL
Clock Source Input Threshold:	+1.40 V	Clock Qualif. Input Level:	DON'T CARE
Clock Qualif. Input Threshold:	+1.40 V	Clock Qualifier Input Imp:	100 kOhm
Trigger Arm Input Threshold:	+1.40 V	Trigger Arm Input Slope:	DON'T CARE
Trigger Arm Input Impedance:	100 kOhm	Trigger Word:	DON'T CARE (X's)
Trigger Qualif. Input Slope:	DON'T CARE	Trig. Qual. Input Thres.:	+1.40 V
Trigger Qualif. Input Imp.:	100 kOhm	Trigger Count:	01
Trigger Delay:	00000	Allow Gaps in Count:	NO
Stop Input Threshold:	+1.40 V	Stop:	INTERNAL
Stop Input Impedance:	100 kOhm	Stop Delay:	1023/16383
Autoarming:	OFF		

Input Page

All Installed Connectors:	SINGLE THRESHOLD	All Labels Single Threshold:	+1.40V
All Labels Upper Threshold:	+2.00 V	All Labels Lower Threshold:	+0.80V
Channel Configuration:			
All Fitted Connectors are Displayed		Each Segment Contains a Single Connector.	
Polarity of all Channels is NORMAL.		Label A assigned to all Channels	

Expected Data Page

Memory Contents not Affected.

Miscellaneous Page

Screen Brightness Setting: 2/3 MAXIMUM

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GLOSSARY

This section contains a list of abbreviations used in this, as well as the other books, which make up the manual set for the HP 81810S Device Verification System, and gives an explanation of some of the technical vocabulary that relates to IC testing. The terms are listed in alphabetical order and a short explanation of each term is provided.

ASIC	Application Specific Integrated Circuit. A generic term encompassing all forms of custom and semicustom IC's designed specifically for a particular application. Sometimes called USICs, for User Specified Integrated Circuits.
Bonding	The joining of metal bonding pads on an integrated circuit to a metal leadframe, using fine wires, usually of aluminum or gold.
Break	When in Break, the generator has ceases to output data. This facility can be used for instance for debugging with the manual. The generator restarts at the Break Address.
CAE	Computer Aided Engineering. The technique of using a computer to aid an engineer in the design of electrical circuits, integrated circuits, gate arrays and other complex engineering designs in a reasonable time frame.
CCD	Charge Coupled Devices. A device utilizing a technique in which information is stored and transported by means of packages of minute electrical charges.
Cell	Circuit performing a digital or linear function that is repeatedly used in the design of an LSI/VLSI chip.
Cell library	Collection of predefined cell functions stored in a computer aided design database. Custom devices can be designed by choosing appropriate cells from the library and locating them on a chip.
Channel Config	The channel configuration is the current arrangement of generator or analyzer channels on the CRT.
Characterization	An IC can be characterized in terms of timing and level measurements. Timing measurements can be set-up and hold-time, propagation delay and minimum cycle time. Level measurements can be minimum input level and maximum fan-out.
Checksum	A number displayed by the generator and the analyzer, which changes every time a change to stored data is made. The checksum number thus provides a means of checking the integrity of the data stored in memory.
Chip	(or die) A single square or rectangular piece of semiconductor material on which a specific electrical circuit has been fabricated.
Chip carrier	A square or rectangular IC package with I/O connections on four sides; connections may be leadless or may not be leadless.
CMOS	Complementary Metal Oxide Semiconductor. A logic family made by combining N-channel and P-channel MOS transistors. This fast, low-power chip fabrication technology has become the leading process for advanced designs.

Continuity test	This DC test checks for proper connection of the DUT by monitoring leakage current at every pin.
Cross leakage	Cross leakage is the leakage current through the power supply pin, with a inputs held at a constant voltage level and all outputs disconnected.
CRT	Cathode Ray Tube. The type of display on the generator and the analyzer.
Cycle Boundary	The ability to program a data signal from one clock period into the on following,
Crossing	using the delay facility. The generator has this capability on the RZ an DNRZ channels.
Cycle Modes	Data output modes of the generator. They determine the data output sequences.
Density	Number of gates (gate count) and/or elements on the circuit. A characteristic largely limited by the size (as measured in microns) of the smallest component element on the device.
Design rules	Collection of rules that define minimum dimension of device-topological structures. Design rules also express process-parameter design limits such as gain factor, threshold level, oxide thickness and capacitance.
Design verification	DV enables the design engineer to decide whether the design should be committed to manufacturing or not. It checks all the aspects of device performance, such as functional operation, DC-parametric and timing characteristics DV is performed in two steps. The first is a verification using CAE simulation tools. The second phase is the hardware verification process.
DC tests	A device has to go through several DC tests, such as: <ul style="list-style-type: none"> - Continuity test - Supply current test - Cross leakage test - Drive level test
Die	(or chip, plural is dice) A single square or rectangular piece of semiconductor material on which a specific electrical circuit has been fabricated.
DNRZ	Delayed Non-Return-to-Zero timing format. Same as NRZ, but delayed with respect to the reference clock (System Clock). The width of a DNRZ data signal equal the System Clock period.
DUT	Device under Test. The tested device or circuit.
ECL	Emitter Coupled Logic. A family of bipolar devices using differential transistor parts that run extremely fast, but which tend to consume much more power than CMOS technologies, especially while inactive.
Foundry	A company that provides IC manufacturing services, usually in the area of wafer fabrication.
Functional test	A functional test ensures some minimal level of function. It conveys little or no information about how the device will respond to changes in timing, drive levels, loads or environmental conditions.

GaAs	Gallium Arsenide. A compound semiconducting material (compound of Group III and Group V elements) in which active devices are fabricated. GaAs has higher carrier mobility than silicon, thus can be used to produce higher speed devices.
Gate	The basic logical element, where the binary value of the output depends on the values of the inputs. In CMOS, gates can be built from two n-channel and two p-channel transistors.
Gate array	An IC consisting of a regular arrangement of gates that are interconnected through one or more layers of metal interconnections. This IC may provide custom functions and is then called an ASIC.
Gate equivalent	The basic unit of measurement for digital circuit complexity, based on the number of individual logic gates that would have to be interconnected to perform the same circuit function.
Glitch	A glitch is defined as two or more transitions of an analyzer voltage threshold between two consecutive analyzer sampling points, i.e. within one cycle. Glitches are unwanted pulses.
Hold time	This is the minimum time data has to be valid at the input lines of a device after the active clock edge for proper operation of the device.
HP-IB	Hewlett-Packard Interface Bus. Hewlett-Packard's implementation of the IEEE Standard 488-1978 and ANSI Standard MC 1.1 "Digital Interface for Programmable Instrumentation".
HP-IB Address	The address assigned to individual instruments linked by the HP-IB. There are two addresses, the ASCII address and the binary address. The former can be set by switches on the rear panel of each instrument, the latter is automatically one higher. The ASCII address is used to send programming commands to the instruments, the binary address is used to send high speed data.
Labels	Letters A-D on the generator and A-F on the analyzer used to assign input or output voltage levels to instrument channels, thus <i>labeling</i> the channels.
LCC	Leadless Chip Carrier. The IC is usually mounted on a ceramic material, which also carries the contact pads. This type of package requires a special test fixture.
Limit Address	An address specifiable by the user, after which no movement of data with respect to the memory addresses in the generator takes place, which would otherwise result from data editing operations such as data inserting, copying, moving or deleting.
LSI	Large-Scale Integration. Device design integration from 100 up to thousands of gate equivalents on a chip.
Macro	A data word edited on the Macro Data Page and then transferred to the data on the Data Page.
Macrocells	The physical gate-level elements and I/O buffers that form the basic building blocks for logic-array design. Macrocells are predefined and characterized metal interconnections of transistors on the array-base masterslice. They correspond to unique logic functions (NAND, NOR, flip-flops, buffers, etc.).

Mask	A feature on the analyzer, which allows the user to mask off bits or whole words of the stored reference data pattern, in order to avoid errors in the incoming data being flagged up.
Mask	A transparent plate covered with an array of patterns used in making integrated circuits. Each pattern consists of opaque areas that prevent the passage of light. The mask is used to expose photoresist which defines areas to be later etched on a wafer.
Megacell	A very large custom-optimized cell that performs a specific function. Megacells include ROMs, RAMs and bit-slice microprocessors.
MSI	Medium-Scale Integration. Device design integrating from 10 to 100 gate equivalents on a chip.
NRZ	Non-Return-to-Zero timing format. A one is represented by the logical high level for one cycle, since the width of a NRZ signal is identical to the System Clock period. The leading edge of this signal and the strobe are identical.
Pad	Comparatively large metallization areas usually placed around the perimeter of the die which provide the areas to which wires or other interconnections are made.
Page	Instrument (generator or analyzer) display menu. The Main Page is the uppermost Page of either instrument and is selected by pressing the PAGES key on the front panel.
Pin Name	A logical name allocated to a DUT pin signal. The name represents a definition, which contains the total path from the instruments to the DUT.
PRBS	Pseudo-Random Binary Sequence. The generator has the ability to generate such a data sequence in a data segment.
Probing	A term used to describe the testing of individual dice on a wafer by using a prober to temporarily connect each die through needles to a tester. A bad die will usually be marked with a spot of ink.
Propagation Delay	The time it takes for a change in the input state of a gate to result in a change in the output state.
Routing	The process of designing interconnections between components in an integrated circuit.
RC	Return to Complement. A logic state in one cycle is followed by its complement in the next cycle.
ROM	Read only memory. A type of memory that cannot be written to, only read from.
RZ	Return-to-Zero timing format. The RZ format starts with a logical zero, pulses to the logical one and returns to logical zero, all within one cycle. The timing information consists of a delay referenced to the System Clock and pulse width.
Sampling	Sampling of data by the analyzer can be <i>synchronous</i> and <i>asynchronous</i> . In synchronous sampling the analyzer clock is synchronized with the DUT clock, in asynchronous sampling it is not. Synchronous sampling with the <i>variable</i>

sampling point allows positioning of the sampling edge with a very high resolution, in the case of the analyzer it is 100 ps.

Segment	A block of generator or analyzer channels arranged in a group on the instrument's CRT. A data segment is <i>not</i> a data bus, unless the positions of the physical data channels in a physical bus correspond exactly to the positions of individual data channels in the data segment on the CRT.
Semicustom	A technique for building ASICs using pre-defined or pre-built building blocks.
Set-up time	This is the minimum time the data has to be valid before the active clock edge for proper processing in the circuit.
Softkeys	Keys on the front panel of the generator and the analyzer, which can be assigned different parameters, depending on the currently accessed screen menu (instrument Page).
SSI	Small-Scale Integration. ICs containing fewer than 10 logic gate equivalents.
Standard cell	A technology allowing designers to use precharacterized gate-level cells in building-block fashion. These "fixed height, variable width" cells are placed in columns and then routed.
Standard Set	A set of standard (default) parameters for the generator and analyzer, which are stored in instrument ROM.
State Diagram	A diagram giving the overview of the analyzer operating states.
Strobe	The Strobe channel, when set to DATA, is another NRZ data channel. When set to CLOCK, it is identical to the system clock. The Strobe can be used as a synchronizing signal for the analyzer.
Supply current	This is the current through the supply pin under different conditions such as stand-by, active, inputs high or low, outputs high or low and all combinations.
System Clock	Internal generator clock (in multi-generator installations the master-generator clock) from which all timing relationships in a test system are derived. The System Clock is normally not available external to the generator, except as the Strobe set to CLOCK.
Test vector	A row of 0's and 1's representing the logical state at the inputs and outputs of a digital device.
Trigger Arm	Triggers the analyzer into the ARMED state when programmed to do so. The analyzer accepts the arming signal at its TRG ARM input.
Trigger Word	A data word on which the analyzer is set to trigger (and go into the ACTIVE state).
USIC	See ASIC.
VLSI	Very Large-Scale Integration. Device design integrating thousands of gate equivalents on a chip.
Wafer	A thin disk of semiconductor material (usually silicon) on which many separate chips can be fabricated. This is then sliced so that the individual chips can be packaged.

Workstation

A user terminal that has local processing capabilities and that is connected to a computer.

BIBLIOGRAPHY

This section contains a list of all publications related to installation, operation, and maintenance of the IC Design Verification System. The publications can be ordered by quoting the part number, which is provided alongside the publication title.

Title	Part no.
HP 81810S IC Design Verification System System Software Manual	HP 81810-90001
HP 81810S IC Design Verification System CAE Link Users Manual	HP 81804-90001
HP 81810S IC Design Verification System System Configuration Manual	HP 15476-90001
HP 81810S IC Design Verification System Data Generator Data Generator Extender Data Analyzer Operating and Programming Manual	HP 08180-90001
HP 81810S IC Design Verification System 256 Pin Testhead Operating and Programming Manual	HP 15466-90001

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