SQUARE-LOOP FERRITE CIRCUITRY

C. J. QUARTLY

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Storage and Logic Techniques

by C. J. QUARTLY

INITIALLY the development of high speed computers was seriously handicapped by the lack of a suitable method of storing information, but this situation was changed by the discovery of a ferrite with a rectangular hysteresis loop, which fulfilled the main requirements of reliability, cheapness and speed of obtaining information. Since transistors of the required characteristics have become available the associated circuits have advanced rapidly.

The author describes in a concise and simple manner the principles of operation of coincident drive stores and the more elaborate systems which have been proposed to increase speed of operation. Though primarily intended for matrix stores, square-loop ferrite cores have found other uses in computers and other digital equipment and brief descriptions are given here.

Early chapters describe the historical developments and then discuss the properties of square-loop materials in general. Various systems—coincident drive storage, word address storage and faster storage—are then described in detail.

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Further chapters explain fully non-destructive read out, the construction of stores, special purpose stores, circuits in storage systems, logical circuits, multi-apertured logical elements and counting circuits using more than two flux levels. Throughout the book the fully transistorized associated circuitry is clearly explained and illustrated.

SQUARE-LOOP FERRITE CIRCUITRY will serve as an introduction for engineers who are beginning work on square-loop ferrite circuits as well as to non-specialists who are incorporating ferrites in a digital system, and also as a source of information for anyone concerned with the development, maintenance and use of such systems.

Mr. Quartly is a senior engineer in the Electronic Components Division of The Mullard Radio Valve Company Limited. In writing this book, he has drawn widely on the experience gained during his ten years with the Mullard organization, many of which have been spent on research into computer storage systems, particularly those using ferrite materials.

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STORAGE AND LOGIC TECHNIQUES

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PREFACE

A few years ago progress in the development of high speed digital computers was seriously handicapped by the lack of a convenient method for storing information. The main requirements for such a store are reliability, cheapness and that the information should be available within a few microseconds. Storage systems which made use of the properties of ferrite materials with a rectangular hysteresis loop appeared to offer the most likely solution to the problem, and since then a large amount of effort has been devoted to the development of this type of store. The original proposal of a coincident drive selection scheme operating upon a matrix of ferrite cores has remained the most widely used, so that most of the development work has been directed towards improving the ferrite materials and circuits which are necessarily associated with the matrix for the purpose of inserting and extracting the information. These circuits advanced rapidly when transistors with the required characteristics became available and, at the present time, reliable square-loop ferrite stores are being manufactured on a large scale.

This book describes the principles of operation of coincident drive stores and other more elaborate systems which have been proposed from time to time usually to obtain an increase in speed. Although primarily intended for matrix stores, square-loop ferrite cores have also found uses in circuits for performing logical operations in computers and other digital equipment and a brief description is given of some of these circuits.

An attempt has been made to cover the field of application of square-loop ferrites in a simple and concise manner. A list of references is included at the end of each chapter to indicate where more detailed information on any particular topic may be found.

It is hoped that the book will provide an introduction to the subject for engineers who are beginning work on square-loop ferrite circuits. It is also intended for non-specialists in the field who are contemplating the incorporation of square-loop ferrites in a digital system, and as a source of information for anyone concerned with the development, maintenance or use of such systems.

The author wishes to thank the directors of Mullard Limited for permission to publish in this book the results of work done on their behalf. He also acknowledges with gratitude the co-operation of many colleagues.

London, 1962

C. J. QUARTLY

Chapter 1

INTRODUCTION

The ability to store large amounts of information is an essential feature of most digital computers. The functions of a computer store include the storage of numbers and instructions fed into the machine, the storage of intermediate results arising during computation and the storage of final results before they are transferred to the output equipment.

In most digital computers information is represented by a binary code—i.e. a code which uses only two symbols, 1 and 0. All numbers and instructions are therefore built up from these two binary digits. For example, the number 13 is represented by 1101 in binary code, while letters of the alphabet can be rendered into similar patterns just as they are rendered into dots and dashes by the Morse code.

By the very nature of the binary code it needs a large number of binary digits to represent a single number—usually between ten and a hundred. A complete number or instruction in binary form is called a " word " in computer terminology. The storage capacity needed by a computer may be many thousands of these " words ", depending on the type of work for which the machine is employed.

A practical storage system for a computer must be reliable in operation and small in size. It must have a low power consumption and be reasonably inexpensive to manufacture (the cost being usually reckoned in so much per binary digit stored). The practical store must also be capable of handling information at a speed compatible with the operating speed of the computer's arithmetic circuits.

Some of the early computers used cathode-ray tubes for storage —the information being retained by electrostatic charges on the screen—but these devices were somewhat bulky and unreliable. Acoustic delay lines and magnetic drums are used quite extensively

nowadays, but these have the drawback that their " access time "* is too long for the high speed operation required in fast computers. The development of square-loop ferrite materials was undertaken to provide storage devices which would overcome all these disadvantages.

Storage elements made of square-loop ferrite material can store binary digits, without consuming electrical power, by virtue of the

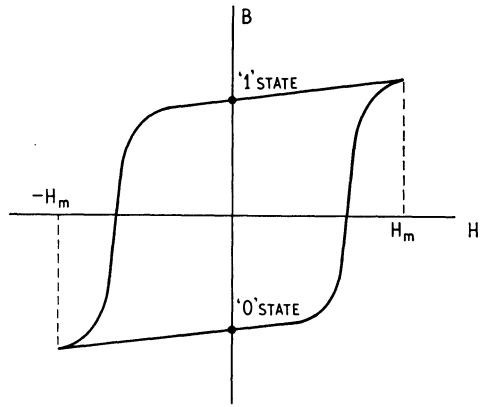

Fig. 1.1—Storage of digital information in an element with a rectangular hysteresis loop

fact that they can be put into two different states of remanent magnetization. These two states of remanence are produced by applying magnetic fields of opposite polarities with sufficient strength to saturate, or nearly saturate, the material.

Fig. 1.1 shows the hysteresis loop of a typical square-loop material. The flat top and bottom of the loop indicate the two states of saturation, where increasing the strength of the applied magnetic field (H) produces little change of magnetic flux (B) in the material.

The magnetic fields are applied electromagnetically by passing electric currents through windings surrounding the material. The two different polarities of magnetic fields are obtained by passing the currents in opposite directions and in practice this is usually done by applying positive-going or negative-going pulses.

* Access time is the average time interval between a request for information from the store and its arrival at the store output.

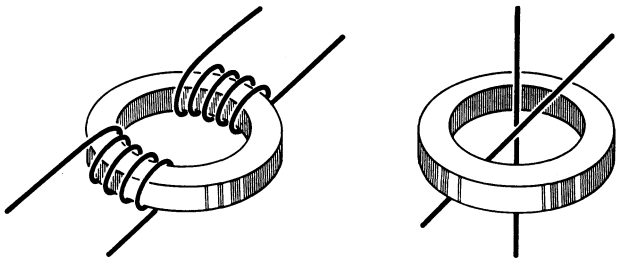

Fig. 1.2—Windings magnetically coupled to toroidal cores to apply and detect magnetic fields: (a) multiple-turn windings, (b) single-" turn " windings consisting of wires threading the core

A low permeability in the ferrite material is desirable at the remanent state, since the simplest method of detecting what digit is stored is by applying a saturating magnetic field in a given direction and observing the resultant change of flux in the material. If the saturation permeability is low there will be a much larger flux change in an element which is changed from one state to the other than in an element which is only driven further into saturation.

Thus, in Fig. 1.1, a much larger flux change will result from the action of a negative field, $-Hm$, on an element in the " 1 " state than on one in the " 0 " state. If a winding is coupled with the magnetic path, the information which was stored can be determined from the form of the e.m.f. generated by the flux change.

This method of storage was first realized in practice about ten years ago. At that time the only magnetic materials available with the desired properties were certain ferromagnetic alloys. These alloys can be rolled into a thin tape which can be wrapped around a bobbin to make a toroidal core possessing an approximately rectangular hysteresis loop. A thin tape is used in order to reduce eddy currents which would slow down the rate of flux change and lead to loss of energy.

The windings needed to apply the magnetic fields are put on these toroidal cores as shown diagramatically in Fig. 1.2. They may consist of several turns of wire, or just be a single wire threaded through the core to give in effect a single-turn " winding ".

One of the first applications described for these alloy toroidal cores was a serial store or shifting register.[1] The principle is

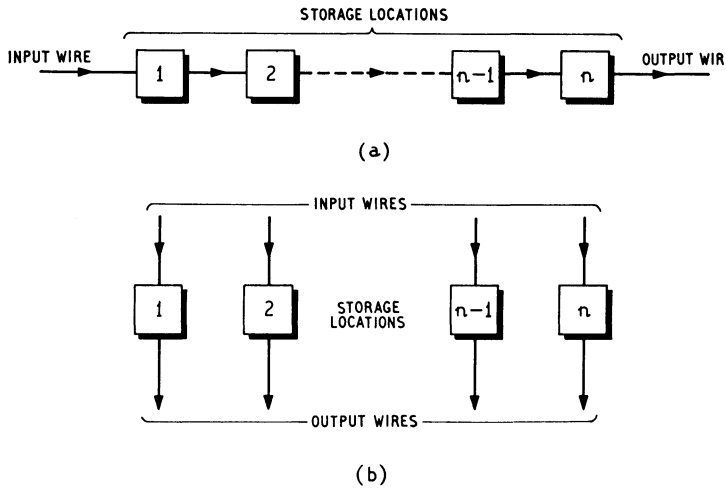

Fig. 1.3—(a) serial access store, (b) parallel access store

shown in Fig. 1.3(a). The device stores binary numbers represented by sequences of electrical impulses which arrive on the single input wire. Each impulse, as it arrives, sets the first magnetic-core storage element to the digit it represents, " 1 " or "0 ", then passes on to the second magnetic-core element and sets that, and so on—the complete pattern of digits moving step-by-step along the length of the register until the whole number is stored.

The maximum rate of transfer of information from one magnetic-core element to the next is limited by the characteristics of the magnetic material, and, since each digit must pass through every storage element when being put into or taken out of the register, this type of store is rather slow in operation. Also the circuits required for shifting the information from one storage element to the next are complex and make the cost per digit stored unduly high. Nevertheless a store using this principle is convenient for holding a small amount of information, provided that the digit input rate does not exceed a few hundred thousand per second.

A much higher speed of " writing " into and " reading " out of a magnetic-core store can be attained if the information is inserted and extracted in parallel, instead of in serial, form. This process

is illustrated in Fig. 1.3 (b). Since all the impulses representing the number arrive on several wires simultaneously, a whole "word " can be handled in the same time as a single digit in the serial store.

In order to prevent the parallel store from becoming prohibitively expensive some simple method for writing-in and reading-out the digits must be provided. A solution to this problem is to wire the magnetic cores in a matrix arrangement[2] in which each core is threaded by two energizing wires, as shown in Fig. 1.4. The rectangular hysteresis loop can now be used for selecting any

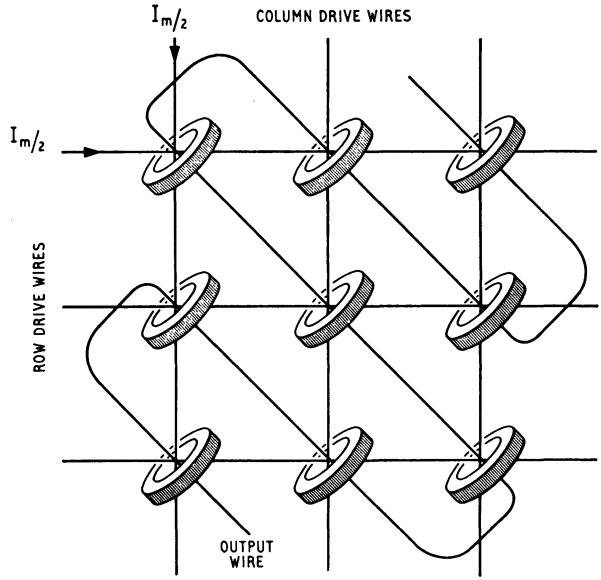

Fig. 1.4—Principle of a coincident drive matrix store

individual core in the matrix for storing binary digits. It is arranged that equal energizing currents applied simultaneously to the two wires passing through one core produce sufficient magnetic field strength to change this core from one remanent state to the other. The other cores, which are only threaded by one energized wire, receive only half this magnetic field strength and are substantially unaffected although they are said to be disturbed. A

third wire through each core is used to carry the output signal arising from the selected core, as shown.

To make a parallel store capable of handling several digits simultaneously it is necessary to provide a separate matrix for each digit, since only one core in a matrix can be used at any one time. This type of store is easy to manufacture as it is only necessary to use single-turn windings.

When this principle of selecting cores was first devised it became theoretically possible to construct a large parallel store with metal tape cores, but in practice these cores proved to be slow in switching from one remanent state to the other and were rather expensive to manufacture—among several other disadvantages. It was not long, however, before a suitable ferrite material was found with the desired square-loop characteristic, and toroidal cores made of this material soon came on the market.[3,4]

These early ferrite cores were somewhat inferior to those in use today, but they were adequate for the purpose and in a very short time the first stores using them were under construction.[5,6] Since then the coincident-current selection scheme has continued to be used in nearly all stores in which it is necessary to have high speed access to the storage elements in a random manner. Improved materials have allowed very large stores to be manufactured. Some idea of how the capacity of these stores has increased over the years can be gained from Table 1.1, which lists a few of the more notable examples.

The improvements which have taken place in ferrite stores have been mainly in increased reliability, lower cost of manufacture and higher speed of operation. Rather elaborate electronic circuits are required to transfer information between the storage elements and the other sections of an electronic computer. In the early ferrite stores these circuits used a large number of thermionic valves, which required far more space than was occupied by the cores themselves. Since then, however, suitable transistors have been developed to replace the valves, and these, together with the use of printed circuit techniques, have resulted in much more compact and reliable equipments.

Such techniques, and others under development, are leading to a considerable reduction in the cost of manufacture per digit stored. If this trend continues a square-loop ferrite store with a capacity of millions of digits—already shown to be possible technically—will become an economic proposition. Many digital

computers at present use two " levels " of storage, in that a high speed ferrite-core store is backed up by a store of much larger capacity but slower speed of operation, such as a magnetic drum. A reduction in the cost of ferrite-core storage might make it possible to replace this system with a single high speed store. This would mean that the programming of computers would be simplified,

TABLE 1.1. DEVELOPMENT OF COINCIDENT CURRENT MATRIX STORE

Computer	*Store size* *Words* × *Digits*	*Cycle time* (*μsec*)
Myriabit Store (R.C.A. 1953)	10,000 × 1 (10,000)	12·5
Whirlwind (M.I.T. 1953)	1,024 × 17 (17,000)	10
Bizmac I (R.C.A. 1956)	4,096 × 7 (28,000)	20
Mercury (Ferranti, 1956)	4,096 × 11 (45,000)	10
Johnniac (Int. Telemeter, 1956)	4,096 × 40 (160,000)	15
TX–2 (M.I.T. 1957)	63,536 × 38 (2,500,000)	6
7302 Store (I.B.M. 1961)	16,384 × 72 (1,200,000)	2·2

and the electronic circuits and time needed for transferring information between the two " levels " would be eliminated.

In recent years there has been an increasing demand for large capacity stores with extremely high speeds of operation. The speeds required are higher than those which can be obtained by using the available ferrite materials in coincident-current stores. Faster switching speeds have been achieved by new systems in which the amplitude of the drive currents is higher than can be used in coincident-current selection. These systems, however, tend to cost more than similar sized coincident-current stores

because the selection circuits or the storage elements themselves are more complicated.

As a result of this increased cost it seems that square-loop ferrites will have to compete in this range of speed with other types of storage elements, such as thin magnetic films or superconductivity devices, unless a faster ferrite material can be found. However, these new types of devices have not been fully developed yet, and in the immediate future the majority of stores will still be using ferrite cores.

Ferrite stores are also being used to an increasing extent in digital data handling equipment. In some cases the storage requirements are similar to those in a computer, but in others they may allow the use of less complex circuit techniques or wiring configurations. For example, a store may be required to hold information temporarily while it is being transferred between units operating at different speeds. Even in applications where the storage capacity may be only a few hundred digits, or where the operating speed required may be very low, ferrite stores are still often preferred to other storage methods because of their compactness, reliability and robustness.

Other applications for ferrite stores include permanent and semi-permanent storage, where the information has to be changed infrequently if at all, and storage systems where a high " reading " repetition rate is required but a much slower " writing " rate.

The characteristics of square-loop ferrites can also be used in logical circuit elements for the arithmetic or control sections of computers. Devices based on these characteristics have only been used to a limited extent, however, since they do not offer any outstanding advantages over alternative elements constructed from transistors and diodes. The main reason is that in order to provide a reliable system a large number of other electronic components is required in addition to the cores. Moreover the complexity of the function which can be obtained from each core is rather limited. On the other hand ferrite cores have been used fairly extensively in certain switching systems where the ratio of cores to other electronic components is much higher.

Many of the objections to logical circuits using ferrite cores do not apply to a recently introduced class of devices constructed from plates of ferrite with multiple apertures. It is probably in this direction that ferrite devices for logical purposes will be developed in the future.

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Chapter 2

PROPERTIES OF SQUARE-LOOP FERRITES

2.1. Material

Square-loop properties are exhibited by many ferrite materials but practically the only material in use at the present time is that with a cubic crystal structure of the spinel type and the general composition MFe_2O_4 where M is a divalent metal or mixture of metals such as magnesium and manganese. The raw materials are pressed into the required shape and after firing the resulting ferrite takes a homogeneous polycrystalline form. Toroidal cores are most commonly used but other shapes, some of which are described later, are made for special purposes. The two main properties which render such ferrites suitable for high speed storage and switching elements are their rectangular hysteresis loops and their high resistivity. The value of the latter is greater than 10^5 Ω/cm which means that eddy current losses are negligible.

2.2. Low frequency hysteresis loop

Typical low frequency hysteresis loops of a square-loop ferrite toroidal core are shown in Fig. 2.1. In the majority of switching and logical circuits which use these cores driving fields very much larger than the coercive force are used, so that the two remanent states which result are those on the outer or saturation loop of Fig. 2.1. It is desirable in these applications that the ratio of the flux change produced, for example, by the action of a negative field on a core in the positive remanent state to that produced by a similar field on a core in the negative state should be as large as possible. To achieve this the gradient of the loop, i.e. the permeability, at remanence should be low.

Magnetic matrix stores usually use a coincident current drive selection system where the main property required from the core

is that, while a field, H_m, is sufficient to switch the core from one remanent state to the other, a field $H_m/2$ is insufficient to cause any significant change of flux. Thus, if B_m and B_α are the flux density levels produced by the fields H_m and $H_m/2$ in Fig. 2.2, a figure of merit for the core when used in a coincidence system

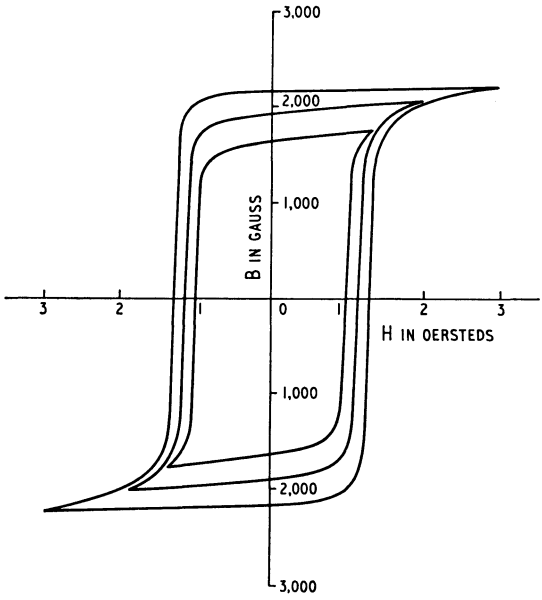

Fig. 2.1—Typical hysteresis loops of a square-loop ferrite core

is the squareness ratio B_α/B_m. The maximum squareness ratio which usually exceeds 0·9 is achieved when a loop rather smaller than the saturation loop is employed such as the inside loop of Fig. 2.1. Thus the requirements for the core differ slightly in the two types of application.

Flux changes in the core may either be reversible, i.e. the core returns to its original state after the applied field is removed, or irreversible. A field which is not large enough to take the state of the core beyond the knee of the hysteresis loop produces mainly reversible charges. Larger applied fields result in permanent changes of flux and the core is said to switch. Changes of flux are

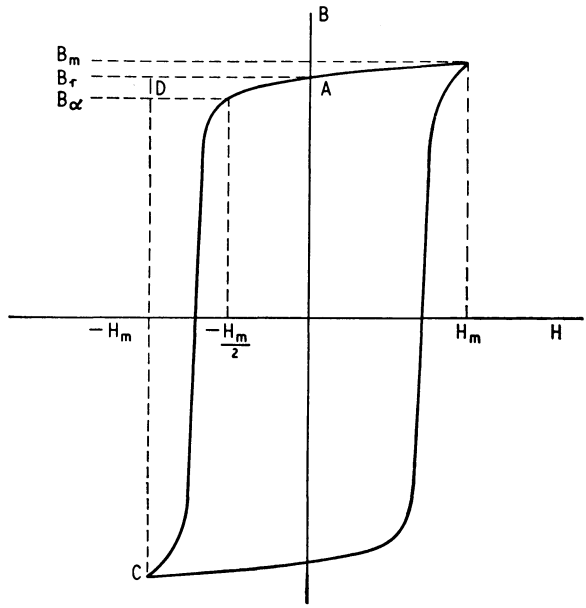

Fig. 2.2—Coincidence selection on a square-loop ferrite core

not instantaneous. If the field $-H_m$ in Fig. 2.2 is applied as a step function the state of the core will follow the path *ADC* rather than the path *AC* along the loop and the e.m.f. waveform generated in a wire linking the core will show two peaks. The first of these is due to the reversible flux changes and the second to the irreversible ones which are much slower. This difference in speed arises from the difference in the mechanism by which flux changes take place within the material. Reversible changes are usually attributed to reversible domain growth and rotation of the direction of magnetization of a domain and the irreversible changes to domain nucleation and domain wall movement.[1,2]

In practice the applied field must have a finite rise time and while there is little difficulty in making this faster than the rise time of the output signal resulting from irreversible flux changes, this is not so for reversible ones and consequently the amplitude and duration of the outputs from the latter are normally dependent upon the rise time of the drive pulse.

2.3. Switching speeds

Over a limited range of applied fields the switching time of a core and the field are related by the formula $T(H - H_0) = S$ where H_0 is a field approximately equal to the coercive force and S is the switching coefficient for the material. Fig. 2.3(a) shows 1/T plotted against H. Switching time can be defined in a number of ways. A common definition when the physics of the switching mechanisms are under discussion is " the time elapsing between 10% and 90% of the flux change ". This is not easy to measure quickly and a more useful method from the user's standpoint is the period from the time when the drive pulse reaches 10% of its maximum amplitude until the output e.m.f. of the core has fallen to 10% of its peak value, as in Fig. 2.3(b). This definition assumes

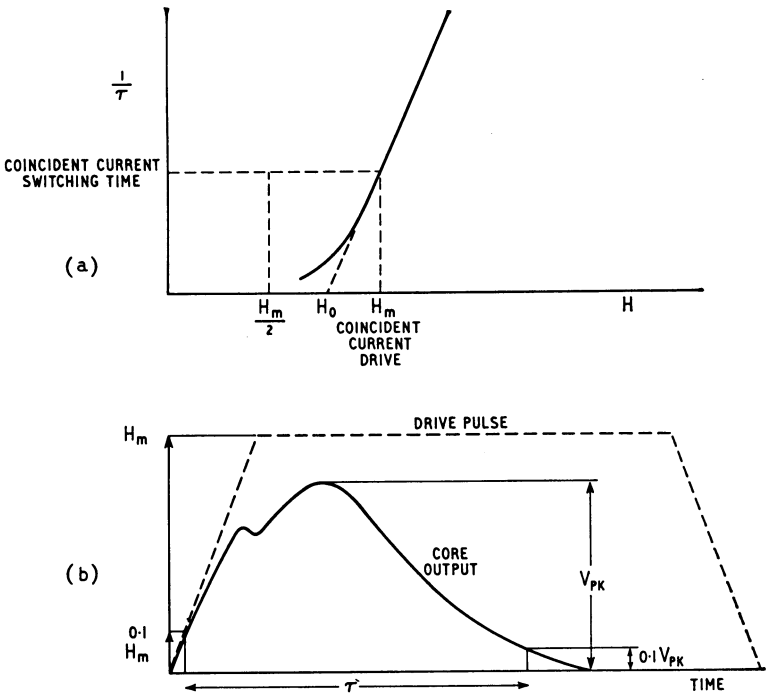

Fig. 2.3—Relation between switching time and applied field

that the rise time of the drive pulse is considerably faster than the time taken for the output to reach its peak value, otherwise the switching time will be increased.

Owing to the common use of coincidence systems, the switching times of cores are often quoted without specifying the drive current. In this case, a driving field, H_m, of about 1·3 H_c, is assumed, since

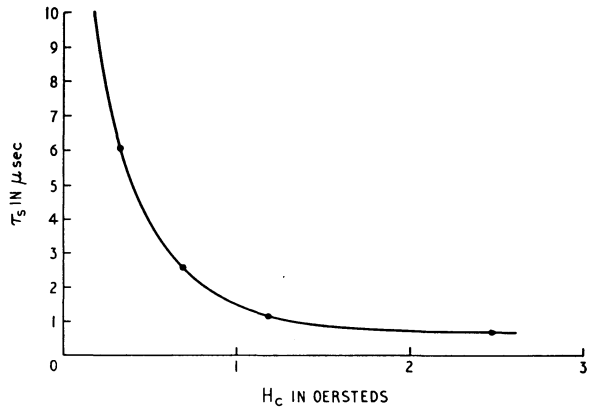

Fig. 2.4—Coincident current switching time and H_c for typical ferrites

to yield maximum squareness, this is the optimum field for such a system (Fig. 2.3(a)).

The switching coefficients of available materials are approximately the same and have a value of about 0·7 to 0·8 μsec Oe, although some newer materials may have a lower value than this.[3] H_o ranges from 0·6 to 3 Oe in different materials. Since the ratio of H_m to H_o is fixed in a coincident drive system, it is obvious that a core with a higher H_o will switch more rapidly in this case though it will require a larger drive to do so. Other cores with a low H_o are available for occasions when ease of driving is of more importance than high speed or where higher speeds for a given drive are required in non-coincidence systems.

Coincident current switching times are plotted against coercive force for some available square loop ferrites in Fig. 2.4 and the results lie on a general curve for this type of material. It has been shown[4] that the formula $T(H - H_o) = S$ only holds up to a value of applied field from two to five times the coercive force. Above

this point S falls to a value of about 0·3 μsec Oe and at a still higher drive to less than 0·2 μsec Oe though the actual values depend on the material. These variations in S have been explained by assuming that the mode of switching changes as the drive increases, the first fall being attributed to a change from domain wall movement to domain rotation and the second by a change over to coherent rotation of the total magnetization within the toroid.

Owing to this effect, switching constants substantially lower than the 0·7 μsec Oe mentioned above are often quoted for drive pulses several times the coercive force but these conditions do not arise in a coincident current store where the maximum drive is limited.

2.4. Temperature effects

The Curie point of most square-loop ferrites lies in the region 150–300°C. As the temperature of a core increases both the saturation flux B_s and the coercive force H_c decrease, finally reaching zero at the curie point.

Temperature problems arise in two ways, firstly from changes in ambient temperature and secondly from self heating due to switching losses in the cores. Coincidence storage systems used at 100 kc/s switching rate or less are more concerned with the former. Self heating is unlikely to be a problem in these systems since the core dissipation would not normally exceed about 0·02 W in a 2 mm core. At room temperature H_c falls off at rates from 0·3% to 3% per °C depending upon the type of material. A 10–20°C rise is often sufficient to impair the discrimination in a large store owing to the consequent reduction in coercive force which increases the flux change in cores subjected to half drive pulses. Any further increase might cause irreversible flux changes under the action of these pulses so that serious loss of information would result. The solution to this problem is either to use a thermostatically controlled enclosure for the matrix or to allow the drive pulse amplitude to vary according to the ambient temperature. The latter is possible since below 100°C squareness varies little with temperature.

Faster storage systems described later have been devised in which cores are subjected to a much heavier drive than 1·3 times the coercive force, in order to obtain faster switching. In these systems changes in H_c are less important since coincident switching

with half pulses is not used. Changes in B_s may however cause trouble.

If a field H_m is applied with a rise time sufficiently fast so that the field is established before the core begins to switch appreciably, the energy used in switching the core is proportional to $H_m B_s$. This energy is dissipated as heat and might be much greater than that dissipated if the low frequency loop path were followed.

In addition, the frequency of switching might be higher in such a system. For example if a 2 mm core intended for use in a 100 kc/s

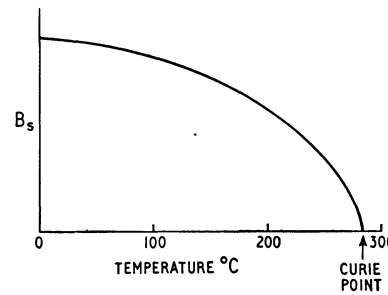

Fig. 2.5—Variation of saturation flux density with temperature for typical core

coincidence store were switched in 0·2 μsec at a 1 Mc/s rate the core might dissipate up to 0·5 W. This does not mean that the curie temperature would be exceeded, since B_s falls off with temperature as in Fig. 2.5 but it does mean that the available flux swing would be reduced. The effect of this is discussed further in Chapter 5 with reference to specific systems.

Faster coincident drive stores are now being made in which cycle times of 2μsec or less are obtained. If the same address in these is allowed to be repeatedly selected at the maximum repetition rate for more than a few tenths of a second then self heating can present a problem owing to its effect on H_c. Control of the ambient temperature or drive current is not a solution in this case since the temperature rise is taking place in one address only. However the temperature rise may be minimized by using the smallest available cores which will provide the most favourable ratio of volume to surface area and the shortest distance for the heat to travel from the interior of the core to its surface. The surface temperature

may be maintained near ambient by surrounding the cores with oil or fast moving air. The use of a material exhibiting a low rate of change of H_c with temperature will also be an advantage.

2.5. Core sizes

Since the early days of core storage fairly standard sizes of toroidal core have emerged. These have external diameters of 0·75, 1·25, 2, 3, 5, 8, 13 and 25 mm. The ratio of the internal to external diameters is around 0·6 to 0·7 and the depth about the same as the difference between these diameters. This shape is important for smaller cores since it enables two straight wires at right angles to pass through the core as required in matrix wiring. The three smaller sizes are intended mainly for use in matrix stores while the larger sizes find their main uses in switching circuits and are consequently produced in much smaller quantities.

Other shapes are also made. An alternative storage element is a hole through a block of square-loop ferrite material. Plates containing many holes made for this purpose are described in Chapter 6. Also the use of elements with two or more apertures for logical circuits is described in Chapter 11 and for faster storage in Chapter 5.

All shapes are made with continuous flux paths. Small air gaps tend to make the hysteresis loop skew so that the squareness deteriorates, although for applications using large drive pulses this effect is less important.[5]

2.6. Comparison with metal tape cores

The early work on magnetic logical circuits was performed with cores consisting of wrapped metal alloy tapes. These have continued to be used for switching purposes, such as the switch matrices used for driving ferrite stores. Iron nickel alloys have been most popular and materials have been developed with hysteresis loops at least as square as any which have yet been attained with ferrites. Owing to its high conductivity the material must be rolled to less than 0·00025 in. in order to reduce eddy currents to an acceptable level. Several turns of this are wrapped on a bobbin. These processes tend to make the cores much more expensive than the corresponding ferrite ones.

The switching constants of metal alloys can be better than those of ferrites, about 0·2 to 0·5 μsec Oe but the coercive forces are

usually very much lower, about 0·05 Oe and this combined with the higher price makes tham a poor competitor for coincident drive matrices. However, the low coercive force would be an advantage in stores not using coincident drive since, for cores of the same size, considerably faster switching would result from a given drive. Metal alloys have also a saturation flux density of about 8000 G and it is this property combined with the lower coercive force which has led to their use in switching matrices.

If very high speed switching is being considered, one advantage of tape cores is their better heat conductivity which allows more efficient cooling to be achieved.

2.7. Core testing

Two types of testing procedure are applied to cores. The first of these, a low frequency loop test, measures the parameters of the saturation loop and is generally applied to the larger sizes of core intended for switching purposes. The second is used to determine their suitability for incorporation in a store using coincident drive selection and in this case drive pulses of rather smaller amplitude than that required to saturate the material are used, since these provide the condition for maximum squareness as defined in Section 2.2 above.

2.7.1. LOW FREQUENCY LOOP TEST

The main requirements here are that the ratio of the permeability at saturation, μ_s, to the permeability as B passes through zero, μ_c, is as small as possible. Some limits may also be required on the spread of B_s and H_c. These parameters may all be determined by applying to the core a sinusoidal current, I, of sufficient amplitude to take the core well into saturation in both directions.[6,7] The core output and integrated core output shown in Fig. 2.6 may then be used as follows:—

μ_c is derived directly from the peak value of the core output e.m.f. or its value when the value of the integrated output e.m.f. passes through zero.

H_c may be determined by measuring I either when the core output e.m.f. reaches its peak or when the integrated output e.m.f. passes through zero.

μ_s follows from the value of the core output e.m.f. when I passes through zero.

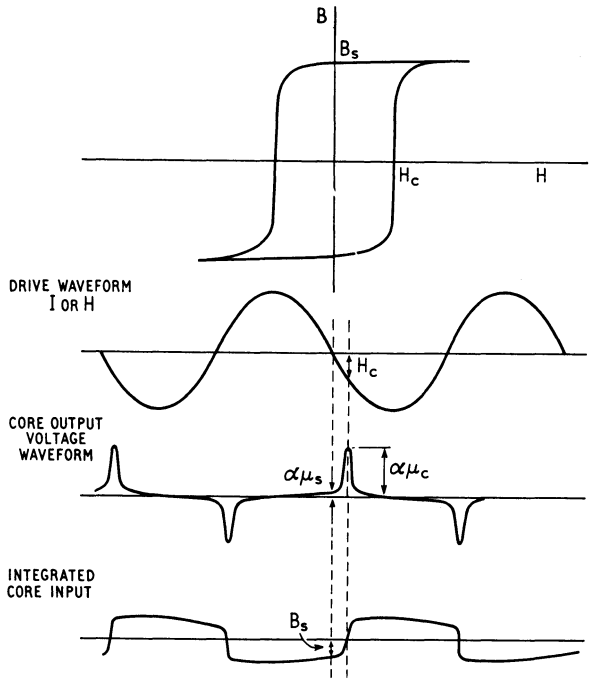

Fig. 2.6—Low frequency loop test

B_s is the value of the integrated output e.m.f. when I passes through zero.

Thus, in theory, it is a simple matter to obtain strobing pulses from the drive and integrated output and use these to sample the appropriate waveforms at the required times. In practice the problem is to obtain a high enough signal-to-noise ratio with the gain and bandwidth required for integration since it is desirable from the point of view of core handling to restrict the output winding to one turn. This is one reason why this type of test is normally used only for larger cores. However, the pulse tests applied to smaller cores for matrix use also provide an indication of their behaviour on the saturation loop as far as μ_s, μ_c and H_c are concerned, though B_s may vary considerably.

An alternative method of performing the above tests is to use a sinusoidal flux change rather than a sinusoidal driving field.

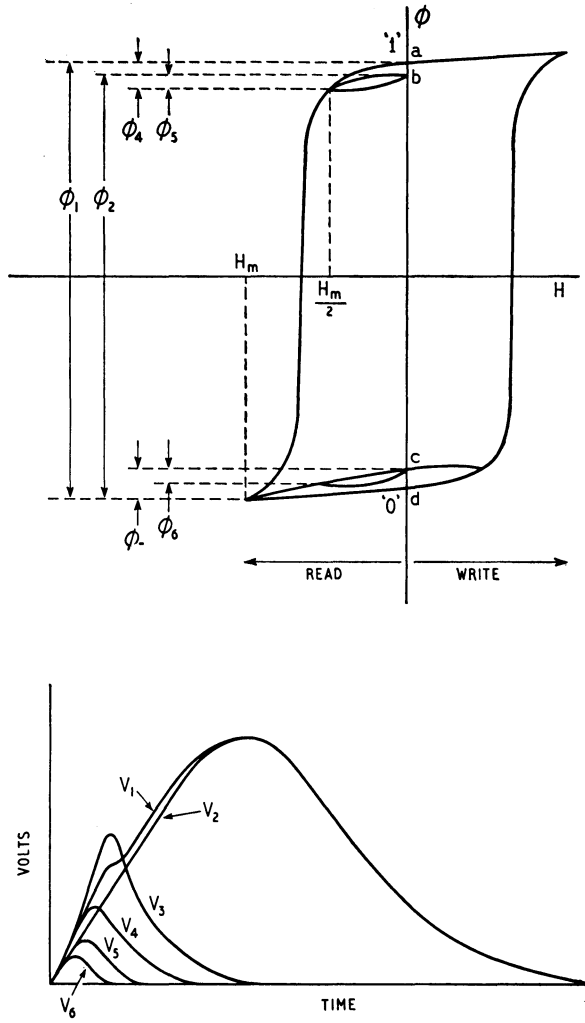

Fig. 2.7—Flux changes and outputs of core in coincident drive storage system

This may necessitate some form of feedback from the output winding to the sinusoidal voltage drive source if high accuracy is required but it eliminates the integration difficulties since integration of a sine wave only amounts to a phase change. A small series resistor in the drive winding can be used to obtain the driving current waveform.

2.7.2. PULSE TEST

The loop test described above does not provide enough information about the core to make it possible to assess its value as a storage element in a coincident drive matrix store. Pulse drives similar to these encountered in the store are used.

Before describing the test procedure the flux changes normally found in such a store will be considered with reference to the hysteresis loop (Fig. 2.7). When the core is in the upper remanent state it is assumed to be storing a " 1 " and when in the lower remanent state a " 0 ". In this case a full pulse to determine the state of the core will be applied in the negative direction. Also appearing on the output wire in a store will be the outputs from a number of cores which only receive a half drive pulse and the effect of this pulse on a core is required to be known. All outputs likely to arise in a coincident current store are set out in Table 2.1 which refers to Fig. 2.7.

TABLE 2.1. OUTPUTS FROM CORES IN A COINCIDENT DRIVE MATRIX STORE

Output	*Symbol*	*Drive*	*Information stored*	*Flux change (Fig. 2.7)*	*Output Voltage (Fig. 2.7)*
Undisturbed " 1 "	uV_1	Hm	" 1 "	ϕ_1	V_1
Disturbed " 1 "	rV_1	Hm	" 1 "	ϕ_2	V_2
Disturbed " 0 "	dV_z	Hm	" 0 "	ϕ_3	V_3
First " 1 " Disturb		$Hm/_2$	" 1 "	ϕ_4	V_4
" 1 " Disturb	rVh_1	$Hm/_2$	" 1 "	ϕ_5	V_5
" 0 " Disturb	rVh_z	$Hm/_2$	" 0 "	ϕ_6	V_6

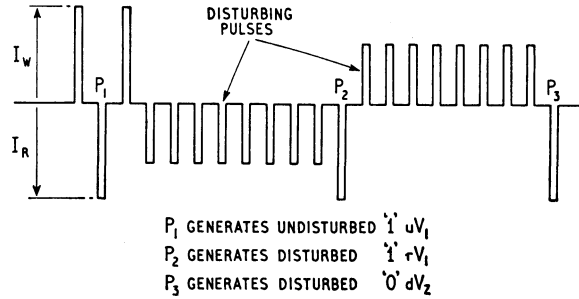

Fig. 2.8—Pulse train used for core testing

It will be noticed that the first half read pulse after a " 1 " has been written produces some irreversible change of flux (from *a* to *b*) and hence the output from this pulse is somewhat larger in amplitude and longer than those from subsequent half pulses in the same direction which produce only reversible changes. Read pulses will not normally be applied to a core in the lower remanent state, *d*, since in a computer a read process is usually followed by a write process in which the core experiences at least a half write pulse which would return it to point *c* in the figure. Thus the " 0 " outputs are assumed to arise from a core at *c* and not *d*. The first three outputs in Table 2.1 are due to full pulses acting on the selected core. The remainder arise from any other core which receives a half pulse and since one problem in a store is to distinguish between a " 1 " and " 0 " output in the presence of many disturb outputs it is evident that V_1 and V_2 should be as large as possible compared with the others.

It is unnecessary to obtain and examine all these outputs in order to test the core.

A pulse train such as that shown in Fig. 2.8 may be used, where the pulses P_2, P_5 and P_7 generate an undisturbed " 1 ", a disturbed " 1 " and a " 0 " respectively, all three of which are examined. Any loss of information due to the half pulses will be exposed by the appearance of a large " 0 " output. A typical drive pulse specification for a core which switches in 1·5 μsec as as follows:—

duration: 2 μsec.

rise time: 0·15 μsec $\pm$0·01 μsec.

overshoot: $<2\%$

droop: $<2\%$.

The ratio of a full to a half pulse used for testing is usually made about 1·6:1 in order to provide a safety margin.

Testing is usually accomplished by choosing a suitable standard reference core which is driven by the same pulse train and backing off the outputs from this core against those from the core under test. By sampling the difference between the outputs of the two cores at appropriate times, acceptance limits may be placed upon the minimum value of the " 1 " output, the maximum value of a " 0 " output, the switching time and the time for the " 1 " output to reach its peak value. As stated previously, the reversible signals are dependent on the pulse rise time but this method of comparing the outputs with a standard core means that the rise time of the drive pulse may have a reasonable tolerance. Cores with a coercive force which differs substantially from the standard will be rejected by this test, since they will switch at a different rate The test is thus not only a test for squareness in individual cores, but also ensures a degree of uniformity which is essential in most systems. Cores of small size are handled easily, automatically and with the aid of a probe which carries the drive and output signals, they may be tested at high speed. Tests are carried out at a fixed temperature.

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Chapter 3

COINCIDENT DRIVE STORAGE SYSTEMS

3.1. Core requirements

Proposals for using square-loop magnetic materials in a coincident drive storage system were made before square-loop ferrite materials had been developed.[1,2,3] Stores using metal tape cores were investigated and a system emerged but the long switching time and high cost of these cores did not make this system attractive. To overcome these difficulties suitable ferrites were produced[4,5] and only a short period elapsed before the first stores were constructed.[6,7]

In coincident drive systems the main requirement of a core is a high squareness ratio as defined in Chapter 2. The necessity for squareness in this sense arises from the fact that in this system the core is used for address selection as well as storage of information. The digit stored in a core is determined by applying a magnetic field in a given direction and observing the e.m.f. induced in a winding linking the core. Thus, for ease of discrimination it is desirable only that the ratio of the flux change due to this field from a core initially in one remanent state to that from a core in the other remanent state should be as high as possible. In terms of the loop shown in Fig. 2.2 B_r/B_m should approach unity. However, the selection function provided by a core in a coincident drive store places a further requirement on the hysteresis loop characteristics in that it is essential that the action of a half amplitude drive pulse should produce a minimum of flux change, both to prevent loss of information in cores to which only a half pulse is applied and to reduce noise on the output wire during reading as described below. This means that B_α/B_m (Fig. 2.2) should also approach unity. These requirements are met sufficiently well in square-loop ferrites for coincident drive selection to be successful.

Fig. 3·1 shows how the amplitudes of the disturbed " 1 " output, rV_1, and the disturbed " 0 " output, dVz, vary with drive current for a typical core when it is subjected to the test pulse train of Fig. 2.8. A value of drive current approximately equal to that indicated by the dotted line will provide the optimum ratio of " 1 " output to " 0 " output over the temperature range 25°C to 40°C when allowance is made for the fact that the ratio of the drive to the

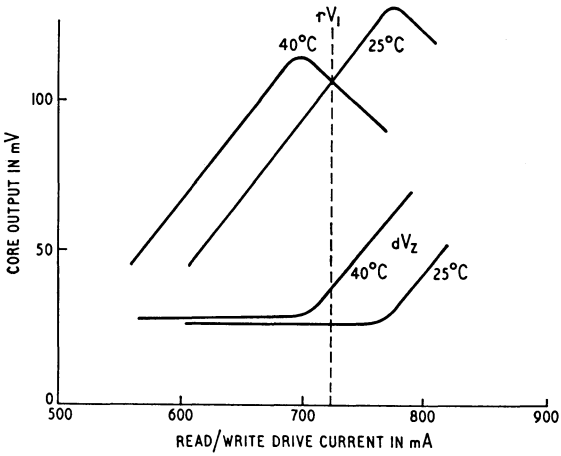

Fig. 3.1—Variation of disturbed " 1 " and " 0 " with drive for test pulse train

disturbing pulse is 2:1 in the store rather than about 1·6:1 as used in the test pulse train from which the curves were derived.

Switching times of cores used in coincident drive stores are usually about 1 μsec which allows a complete operation involving reading, writing and switching the drive pulses to another storage location, to be accomplished in less than 10 μsec, although faster materials are now available which switch in less than 0·5 μsec and hence enable cycle times down to 2 μsec to be achieved. In a random access parallel store these cycle times are short enough to operate with the type of serial logical circuit being used in the majority of commercial computers. They are, however, still too long for some newer computers which achieve much faster operating speeds by the use of parallel logic.

3.2. Matrix wiring

In the coincident drive system the cores are arranged in the form of a matrix. A common method of wiring this matrix is shown in Fig. 3.2 for a plane containing 64 cores.

Every core is linked by four single turn windings. The selected X drive winding carries a half amplitude drive pulse to all the cores in one row of the matrix and simultaneously the selected Y drive winding carries a second half amplitude drive pulse to the cores in one column. Thus the core linked by both of these windings receives a full amplitude pulse. Pulses used for reading are of the opposite polarity to those used for writing. With the cores arranged as shown it is evident that the polarity of a read or write pulse will

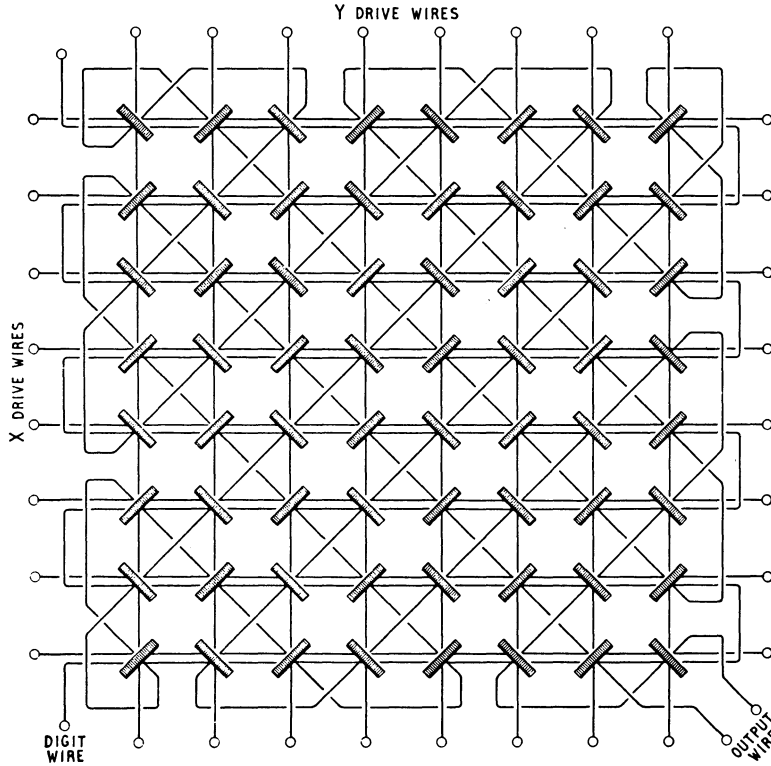

Fig. 3.2—Matrix plane wiring

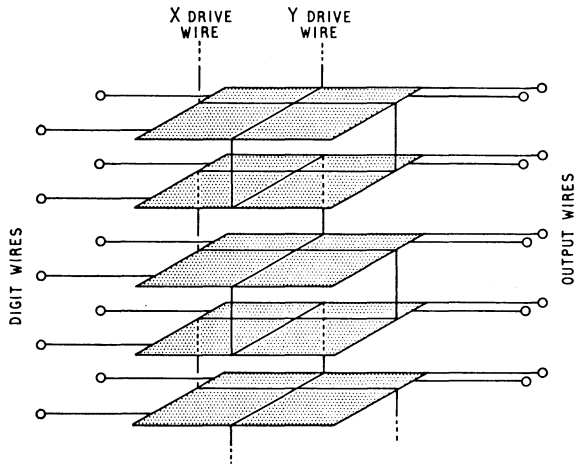

Fig. 3.3—Connection of planes in matrix stack

alternate from one row or column to the next in order that any selected core should receive the sum rather than the difference of the two half pulses.

A core which is driven by a full pulse during the writing operation will be switched from one remanent state to the other and is then said to be storing a " 1 ". Since a core is driven to the " 0 " state during a read operation, no switching is required during writing when it is desired to store a " 0 ". This could be accomplished by withholding one of the half write pulses. However, a word of several digits is stored in parallel and since one plane is required for each digit it is desirable from the point of view of economy that all planes should use the same driving circuits by connecting them in series as in Fig. 3.3. Another winding is then required in each plane and is energized only in the planes where a " 0 " is required to be written. This winding is the digit wire of Fig. 3.2. It threads all cores in one plane, and a half pulse in the appropriate direction on this wire opposes the write pulse in the selected core and reduces the total pulse received by the core to one half pulse which is insufficient to cause switching. Information in other cores in the plane will be unaffected by the digit pulse since it will reduce the drive experienced by cores on the selected row and column to zero while the remainder of the cores in the

plane will experience a half pulse in the read direction. In systems such as this where the digit pulse opposes the write pulse it is often called an inhibit pulse.

Also threading the cores in each plane is the output wire. There are various reasons for inserting this winding in a manner such as the one shown. Firstly, to a first approximation the inductive coupling between the output wire and any two selected drive wires is zero and in addition its terminations are close together so that any loop external to the plane may also be small. Thus large signals due to direct pick up from the high current read pulses are avoided. Secondly, and more important, owing to their lack of perfect squareness the remainder of the cores on the selected row and column produce small disturb outputs, and the method of wiring shown provides a first order cancellation of these outputs. In a matrix plane with an even number of rows and columns there remain two uncancelled cores. With an odd number of rows and columns there may be 0, 2 or 4, depending upon the position of the selected core in the plane.

3.3. Matrix plane output

During a read process the problem is to determine from the e.m.f. produced at the output terminals of the matrix plane whether the selected core produced a " 1 " or a " 0 " output. The output of this core is masked by " noise " which is generated by the disturbed cores on the selected row and column and by direct pick up from the drive windings. Various methods have been devised to ease the problem of discrimination but before describing these the origin and form of the unwanted signals will be considered more closely.

The disturbed cores may be storing either a " 1 " or a " 0 ". Of the states *a*, *b*, *c* and *d* in Fig. 2.7, it is impossible for any core to be in state *d* in a store in which a read/write cycle is used for each address selection since in this case each core will have received at least one half write pulse immediately after a full read pulse. Thus all cores storing a " 0 " will be in state *c*. It can also easily be shown that with the same cycle it is impossible for more than two half selected cores to be in state *a*, even though there may be many in this state present in the whole plane. Thus the vast majority of half selected cores will be either in state *b* or state *c* and will generate an e.m.f. in the output wire of the form V_5 or V_6 in Fig. 2.7 upon the application of the read drive pulses. Owing to the spread in core properties and the fact that different cores

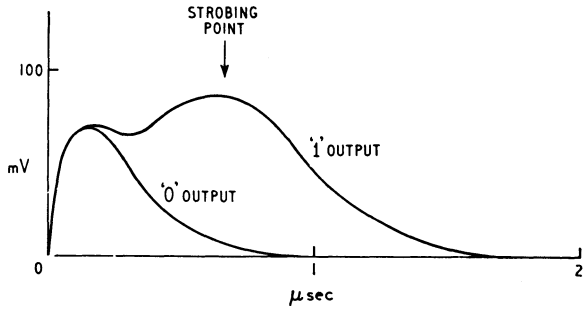

Fig. 3.4—Output waveforms of matrix plane after rectification

have received different pulse patterns, the amplitude of these outputs vary from core to core and for a given core V_5 will be larger than V_6. As mentioned in Section 3.2, the arrangement of the output wire provides a first order cancellation of these outputs in that approximately the same number of each polarity will occur. But since V_5 and V_6 are not equal, the total output will depend upon the pattern of " 1 "s and " 0 "s stored in the plane and allowance must be made for the worst pattern which can occur. This pattern arises when all cores providing a disturb output of one polarity are in state *b* and all those providing the opposite polarity are in state *c*. A measure of the performance of a core in a given size of plane can therefore be determined from the difference between V_5 and V_6 (i.e. $rVh_1 - rVh_2$) which is often called the delta noise and can be measured by taking the average value over a number of cores.

Both wanted and unwanted outputs may be of either polarity at the output terminals of the plane and for this reason the waveform is usually rectified before any operation other than amplification is performed on it in the output amplifier. After rectification the outputs for a " worst " pattern might be of the form shown in Fig. 3.4 and it is necessary to be able to distinguish between these outputs and generate a signal to denote which output has occurred. In the past several methods have been used to solve this problem of discrimination between a " 1 " and " 0 " output and some of these are described below.

3.3.1. AMPLITUDE DISCRIMINATION

For a small matrix plane, the " 1 " signal may be distinguished from the " 0 " by simple amplitude discrimination, especially if

the rise time of the drive pulse is slow in which case the outputs from half selected cores become much smaller relative to the " 1 " output.

3.3.2. STROBING

By far the most common method of aiding the discrimination between a " 1 " and " 0 " output is by means of a strobe pulse which samples the output at the point where the ratio of a " 1 " to " 0 " output is a maximum. This point is near the peak time of the " 1 " output by which time the noise amplitude has fallen to a low value and, provided that the plane is not too large, will be well below the " 1 " output as in Fig. 3.4. The strobe pulse must be over before the end of the drive pulse at which point there is a further large noise pulse on the output wire when the drive pulse returns to zero.

The absence of a strobe signal during a writing operation means that a further gating operation to prevent the outputs during writing from passing through the output amplifier is not necessary.

3.3.3. INTEGRATION

During the application of a half read pulse to cores in state *b* or *c* (Fig. 2.7), these cores will undergo reversible flux changes and return to their original state when the pulse terminates so that the total flux change is zero. This means that the total voltage/time integral over the whole pulse is zero. Thus if integration is carried out over this period and amplitude discrimination applied to the integrated waveform it should be comparatively easy to detect the presence of a " 1 " output which arises mainly from an irreversible change of flux.

In one early store[6] the read/write cycle was more complicated than usual and a read operation consisted of a drive pulse in each direction. Integration was then performed over both pulses to determine whether the core had switched in one or both directions and had hence undergone either a change of flux or no change respectively.

The integration technique has been used much less than the strobing technique, partly because the output circuits required are more complicated and partly because a longer access time is involved. When strobing is used the information is available at the strobing time, whereas with integration it will not appear until after the drive pulse has ended.

However, integration may be advantageous in some cases where time is less important since it enables drive pulses of slower rise time to be used.

3·3·4. NON-SQUARE MATRICES

Another method of eliminating much of the disturbed output is achieved by commencing the read drive pulse in one co-ordinate before the other. The disturb outputs from the first pulse may then be allowed to die away completely before the second pulse arrives and there remain only those arising from the second pulse to be encountered at the strobe time. This method may be improved somewhat by making the matrix rectangular rather than square and arranging that the pulse which begins first is applied to the longer dimension.

For example a 64×64 matric plane normally provides the output wire with disturb signals from 126 cores, whereas a 32×128 plane containing the same number of cores and used as described above will yield only 31 disturb outputs.

The disadvantages of this system are again that the access time is longer owing to the extra time elapsing between the beginning of the first half read pulse and the strobe time and also that the driving circuits are less economical owing to the non-square matrix. Against these a simpler form of matrix wiring may be employed with the output wire parallel to the long dimension.

At least one large store has been built using this system.[8]

3·3·5. POST-WRITE-DISTURB

In some stores[7] a post-write-disturb pulse is incorporated. The pulse consisted of a short duration half pulse on the digit wire and occurs after the write operation and in the same direction as the inhibit pulse, i.e. the read direction as far as the cores are concerned. The object of this pulse is to ensure that all disturbed cores last received a half drive in the read direction and are thus more likely to provide similar outputs.

In stores where writing does not follow reading in the same address a post-write-disturb pulse may be essential in order to eliminate the first disturb outputs.

Extra time is not usually necessary for such a pulse since it may be inserted during the time allowed for address changing.

3·4. Matrix drive requirements

One disadvantage of coincident current systems is that the amplitude of the current pulses required for core driving is rather critical. Variations of more than a few per cent relative to one another in the half pulses, including the digit pulse, cannot be

tolerated although a rather larger variation from the nominal can be permitted, provided it occurs in the same direction for all pulses. In the latter case a slightly different hysteresis loop will be followed without much change in squareness. Since the load presented by a drive wire is very non-linear a current source is used.

To illustrate the nature of this load a typical store consisting of

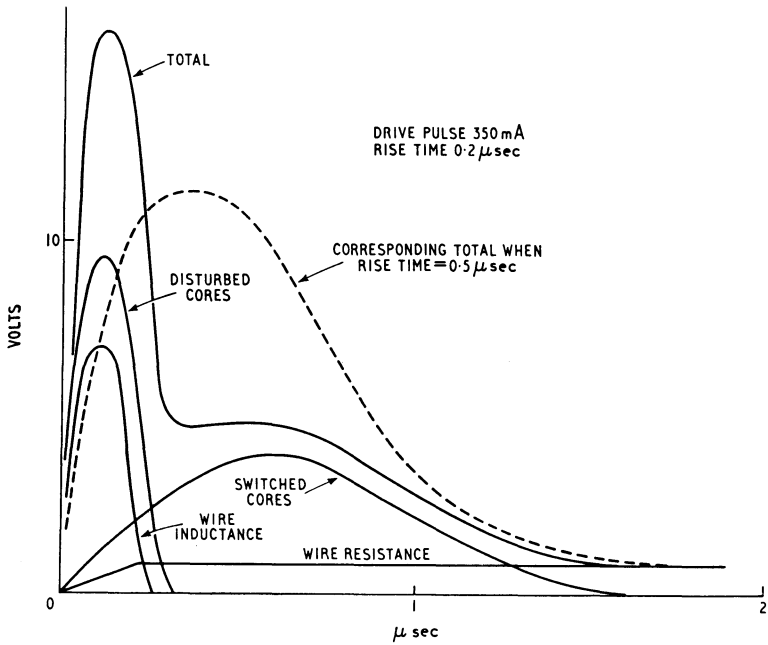

Fig. 3.5—Voltage developed across drive winding of typical matrix stack

40 planes each containing 32 × 32 cores will be taken. A switching time of 1·5 μsec and a peak " 1 " output of 100 mV is assumed for the cores. As shown in Fig. 3.5, the back e.m.f. appearing across the stack on one drive wire arises from four sources. These are the e.m.f.s from half selected cores (in this case 1240 cores), the inductance of the wire, the resistance of the wire and the e.m.f. from the 40 selected cores. The last of these will be a maximum if all 40 selected cores are storing " 1 "s and this is assumed to be

the case. Typical values for inductance and resistance of a drive wire in one plane are 0·1 μH and 0·05 Ω.

It can be seen that the back e.m.f. consists of a large initial spike followed by a long tail. The former is mainly due to the wire inductance and the disturbed cores both of which produce back e.m.f.s which are dependent upon the rise time of the current pulse. The dotted line in Fig. 3.5 shows the same total back e.m.f. when the current pulse rise time has been extended to 0·5 μsec. The peak is then lower and this may be an advantage from the point of view of drive circuit design, particularly if transistors are being used, but it is only obtained at the expense of some loss in switching time and in the ratio of wanted to unwanted output signal at the strobing time. Thus the rise time chosen will depend upon the particular requirements.

Digit pulse shape and amplitude are similar to those of a half drive pulse except that they must inhibit the action of the write pulse over its complete length and should hence begin earlier and finish later than the latter. In the store described above the impedance presented to the digit drive circuit arises from the digit wire and the disturb voltages from 1024 cores in one plane.

3.5. Large coincidence stores

Up to the present time the largest stores to be constructed have used a straightforward coincident current system. The largest so far described contains thirty-eight 256 × 256 planes or a total of about two and a half million bits of fast access storage. A cycle time of 6 μsec has been achieved for this store.[9,10]

On account of the large plane size, one or two variations on the simple scheme are incorporated. The windings in a plane behave as delay lines and a pulse on these is delayed by approximately 0·1 μsec for each 4000 cores.[9] To reduce this delay and prevent distortion of the digit pulse, the digit wire in each plane is divided into four sections, each threading about 16,000 cores. This also reduces the large transients which would otherwise occur on the output wire when the digit pulse is applied.

In order to reduce the disturb output the output wire is divided into 16 sub-assemblies each threading 64 × 64 cores. Four of these are connected to each output amplifier and are arranged in such a way that not more than one assembly on each amplifier is disturbed by the selected drive windings. By this means the total disturb output is no larger than that from a 64 × 64 plane.

However, delay also occurs in the output windings and a series parallel arrangement of the outputs of the four sub-assemblies is used to alleviate this problem.

3.6. Multiple coincidence systems

Selection ratios greater than 2:1 have been proposed[11] for two reasons. Firstly, a multiple coincidence store places less stringent requirements on the core's squareness and hence might be used to improve the reliability of a store using normal materials, to make drive currents less critical or to allow inferior materials to be employed. Secondly it might be used to increase the speed of the store.

The extra selection wires are threaded obliquely in such a manner that no core other than the selected one is situated on more than one energized winding. For example, in the first case, if four selection wires thread each core and a current $\frac{Im}{4}$ is applied to each selected wire no disturbed core in the matrix will experience a drive larger than $\frac{Im}{4}$. This means either that the cores are much less likely to lose information or that the material may be much less square. It was pointed out later[12] that by passing a negative current of value $\frac{Im}{p(2p-1)}$ simultaneously through every unselected wire the maximum disturbing current to any core could be further reduced to $\frac{Im}{(2p-1)}$ where p is the selection ratio.

The disadvantages of multiple coincidence systems are that the matrix plane would be difficult to construct, more complicated selection circuits are needed, many more disturb outputs will appear on the output wire and lastly it is difficult to see how a digit wire could be used to allow planes to be driven in series. In view of these and the fact that satisfactory material for 2:1 selection is available, these systems have not been used for the purpose of improving upon 2:1 systems at normal speed.

Multiple coincidence drive systems can also provide a faster store if $\frac{Im}{2}$ is applied to the drive wires. In this case the selected core will receive a total drive of $\frac{pIm}{2}$ and will switch faster than

in the normal 2:1 system. The problems mentioned above remain except that the " 1 " output might be more easily distinguished from the noise and it is doubtful whether this system is a serious contender for faster storage when compared with other systems described in Chapter 5

3.7. Matrix construction

The fabrication of matrix planes from toroidal cores is still mainly a manual operation. Threading of the output wire in particular would be a very difficult problem to overcome by automatic methods. Various mechanical aids are employed to make the task of wiring less arduous. Among these is the suction jig[13] which serves to hold the cores in position while some or all of the windings are inserted. The tendency to use smaller cores increases the difficulties since apart from the smaller apertures a thinner, and hence less robust, gauge of wire must be used.

Each core assembly is usually mounted in a frame carrying terminals to which the wires are soldered. The use of flux coated wire and dip soldering techniques can simplify this operation as well as the connection of the drive wires in one plane to those of the next when the planes are built up into a complete stack. Storage core life is probably unlimited so that the source of any unreliability will lie in the wiring and in particular in the soldered joints of which there are a large number. Possible damage to wire insulation from core vibration can be prevented by applying a plastic coating to the whole plane. Thus if care is taken to ensure that no faults exist in the wiring, including the joints, the matrix stack can be one of the most reliable components in a computer. Physical damage can be avoided by enclosing the stack in a protective container. There remains the possibility of failure due to the application of excessive voltage or current to the various windings and adequate precautions should be taken in the design of the associated circuits to ensure that faults in these circuits cannot lead to these conditions.

In order to reduce or eliminate the time spent in wiring the matrix planes various alternative forms of construction have been tried. Among these, apertured plates have been by far the most successful and a more detailed description of this type of element is given in Chapter 6.

Another proposal concerns the use of printed wiring with toroidal cores.[14] In the arrangement described the cores were mounted

in holes in a supporting plate with the axis of the core perpendicular to the plate. Cores and plate were then covered with a plastic material which bridged the gaps between them and served as a base for the copper coating. Four collimated light beams with suitable masks were required in order to print a wiring pattern which included four windings through each core aperture and interconnections on each side of the plate. One of the main problems in this method is the accuracy required in the positioning of the cores, masks, and light sources during the photographic process. It might be easier to achieve a partially printed system in which two wires are printed and the other threaded through all planes at the same time in a similar manner to that described for apertured plates in Chapter 6.

It has also been suggested that the ferrite storage elements should be fired in position on a wire matrix which is relatively easy to construct beforehand.[15] The ferrite " beads " so formed have square-loop properties. For this method to be successful the wires would need to be very thin and, although this means a low drive current, the ratio of the outer to inner diameter of the bead is high so that the loop is not as square as that of a toroidal core.

Although the above methods certainly lead to a reduced wiring time, it is unlikely that the operations involved would lead to a cheaper store than the conventional type.

3.8. Advantages and disadvantages of coincidence systems

The vast majority of ferrite matrix stores in use today containing anything from a few hundred to millions of cores employ for selection the 2:1 coincidence principle as described in this chapter. The popularity of this method suggests that it must have considerable advantages over other possible systems such as the one described in the next chapter.

Its main advantage probably lies in the driving circuit requirements. These circuits account for a major part of the cost of any store and also any unreliability will probably be found here. By combining the storage and selection function in the core the complexity and therefore cost of the driving circuits is reduced to a minimum and the reliability is a maximum.

The disadvantages of the system are as follows:—

(a) Since the output wire links many disturbed cores there is considerable noise masking the selected core output.

(b) A high degree of uniformity is required in the core characteristics in order that the cancellation of disturbed outputs should be effective.

(c) The amplitude of the drive pulses must be closely controlled.

(d) The insertion of the diagonal output wire during plane manufacture is not a simple operation. The problem is alleviated by the use of apertured plates as described in Chapter 6.

(e) The speed of operation of the store is limited since although faster cores can be produced the problem of driving them becomes difficult.

The first three of these are influenced by the extent to which the hysteresis loop of the material departs from the ideal and as better materials become available these problems are reduced. The last is more fundamental and although it can be partly overcome by using a material with a higher coercive force, the difficulties of obtaining the higher drive current necessary may be considerable. However, the speed attainable with the system is fast enough for present day commercial computers where its relative cheapness is of more importance. It seems likely that this system will continue to be the most widely used where information is to be stored in square-loop ferrite toroidal cores.

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Chapter 4

WORD ACCESS STORAGE SYSTEMS

4.1. General system

The coincidence system described in Chapter 3 places rather stringent requirements on the squareness of the cores and on the drive pulses in order that information should not be partially erased or inserted by the half current pulses used for reading and writing. In addition a large number of unwanted signals from partially selected cores appear on the output wire and render the discrimination between " 1 " and a " 0 " a more difficult operation than if these noise signals were absent. These problems arise because the storage core performs a selection function as well as the storage function.

A storage system which overcomes these difficulties to a large extent has been devised and used for high speed storage in at least one large computer, namely EDSAC II at Cambridge University.[1,2] In this system, which is commonly known as a word access or direct selection system, the gating or selection function is entirely removed from the storage matrix for reading. It is retained for writing but less exacting requirements are placed on the cores' performance than in the coincident drive system. Thus, apart from the reduced noise on the output wire, this type of store will allow less well defined drive pulses to be used, will provide higher speeds of operation than a coincident drive store, and will permit the use of materials with lower switching constants which can be obtained at the expense of a reduction in squareness.

4.2. Read operation

Cores are arranged in a matrix as illustrated in Fig. 4.1. Each word address location has its own read drive wire so that a pulse on one of these wires is applied only to the cores in the address from which information is to be extracted. The cores are driven to saturation in the " 0 " state by the read pulse so that any core

which was storing a " 1 " will provide a larger output than one which was storing a " 0 ". Since no other cores are disturbed by the read pulse there are no unwanted disturb outputs on the output wire and discrimination between " 1 " and a " 0 " should be a simple matter. In practice imperfections in the selection circuits discussed in Section 4.4 and direct pick up will lead to the presence

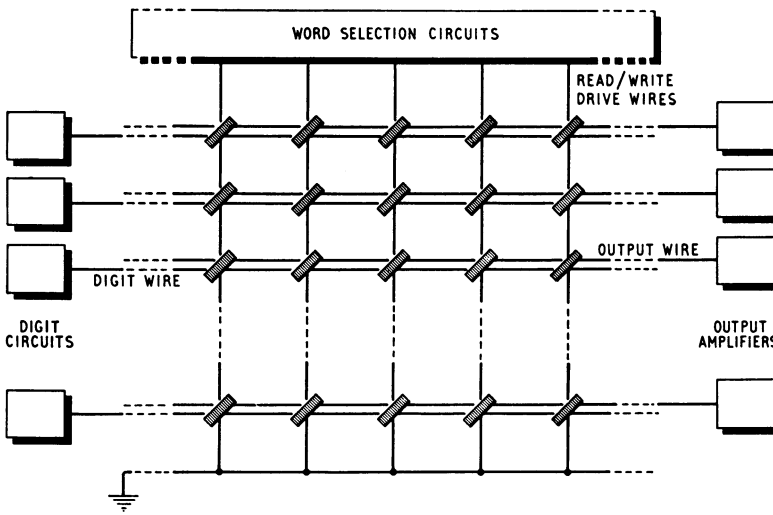

Fig. 4.1—Word access storage system

of some noise. Owing to the configuration of the cores and windings, the " 1 " and " 0 " signals will always be of the same polarity regardless of the storage location and it is possible to back off the " 0 " output with a similar pulse derived, for example, from a compensating core on each output wire. In this way a higher " 1 " to " 0 " ratio may be achieved.

The fact that the read wire only threads the selected word means that there is no limit on the amplitude of the read pulse and by using a larger drive than can be applied in coincidence stores a higher amplitude " 1 " output may be produced. A faster output is also obtained by this means and leads to a shorter access time for the store.

4.3. Write operation

After reading, all cores in the selected word are left in the " 0 " state so that during the writing process they are required to be either left in this state or switched to the " 1 " state depending upon the information which is to be stored. Thus, unlike the reading process, the writing process cannot be performed by applying the same total pulse to every core in the address and for this operation a coincidence drive is employed. One component pulse may be carried by the same wire used to provide the read pulse but in the opposite direction to the latter. The other is carried by the digit wire which threads cores in the same position in every word as in Fig. 4.1. The digit pulse, the presence or absence of which determines the information stored, may take the form of an inhibiting or an augmenting pulse or a combination of both may be used. The relative merits of these are discussed below.

If the read pulse is larger than the full write pulse an asymmetrical hysteresis loop will result as shown in Fig. 4.2, since complete saturation cannot be achieved by the coincident pulses used for writing, if these pulses must not produce loss of information in other cores.

Any preference for an augment or inhibit system depends partly on the result of disturbances caused by the digit pulse on the unselected cores and by the write pulse on the selected core when a " 0 " is written, and partly on the design of the selection circuit.

In the augment system, Fig. 4.2(a), a half write pulse on the read/write drive wire is added to a half pulse on the digit wire when a " 1 " is to be written. A core into which a " 0 " is written receives no digit pulse. Disturbing pulses are all in the write direction and hence can only affect a stored " 0 " adversely. They consist of a single half pulse on the read/write drive wire when the " 0 " is written and then a number of half pulses on the digit wire when " 1 "s are written into the corresponding digit position of other word locations.

In the inhibit system, Fig. 4.2(b), a full write pulse is carried by the read/write drive pulse and this is opposed by a half pulse on the digit wire when a " 0 " is to be stored. In this case the disturb pulses which could cause trouble are the single half pulse in the write direction when a " 0 " is written which might lead to a larger " 0 " output and the digit pulses in the read direction for other addresses which might tend to destroy a stored " 1 ".

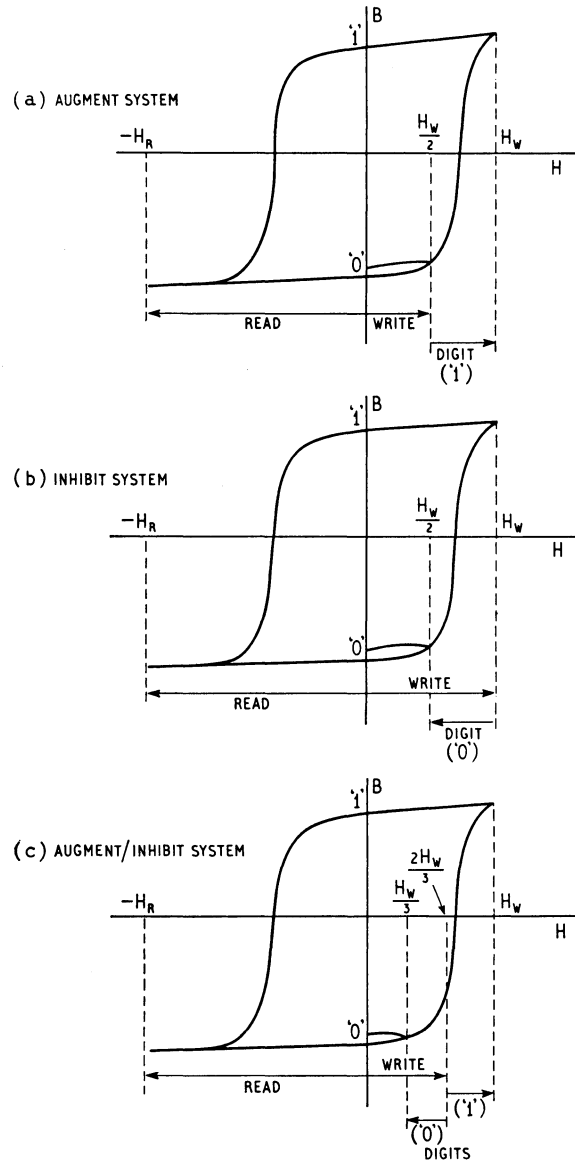

Fig. 4.2—Comparison of writing methods in word access system

In both systems, therefore, a core storing a " 0 " receives one disturbing pulse in the write direction from the read/write wire during the writing process but stored " 0 "s are affected by the digit pulses in the augment system and stored " 1 "s are affected in the inhibit system. On this basis the inhibit system might be considered to be preferable since a slight reduction in a " 1 " output following these disturbances affects the " 1 " to " 0 " output ratio less than an equal increase in the " 0 " output.

However, since in both systems there is only one disturb pulse from the read/write drive wire, this pulse can be allowed to be somewhat larger than half the full write current, I_W, without causing very much additional irreversible flux change in a stored " 0 ". As a result the digit pulses become smaller than half the full write current and are thus less likely to cause significant loss of stored information by their repeated application.

Another advantage of the augment system is that the two pulses need only overlap for long enough for the core to switch. With the inhibit system the inhibit pulse must exist for the whole duration of the write pulse. This can be difficult to achieve with large direct selection systems working at high speeds.

A combination of augment and inhibit currents may also be used. In this case a digit current adds to the write current when a " 1 " is to be written and a digit current of the opposite polarity subtracts from the write current for a " 0 ". It can be shown[1] that from the point of view of disturbances the optimum conditions occur if $2/3I_W$ is derived from the write drive wire and $\pm 1/3I_W$ from the digit wire as shown in Fig. 4.2(c). Disturbing currents are now only $1/3I_W$ in amplitude and will have less effect on the stored information.

As mentioned previously fast reading may be achieved in a direct selection store, since the amplitude of the read pulse is not limited. The writing methods described above involve coincidence selection and the writing speed is similar to that in a coincident current store using the same cores. Two methods for decreasing the writing time to a limited extent are illustrated in Fig. 4.3. The first of these, Fig. 4.3(a), uses an augment/inhibit system of digit pulses which can be of the same amplitude as those in the normal augment or inhibit system, i.e., $I_{W/2}$, and a full write current pulse, I_W, on the write drive wire. The second, Fig. 4.3(b) uses a standing negative bias of $-I_{W/2}$ on all cores so that with an augment system both the digit pulse and the write pulse may be as large as I_w.

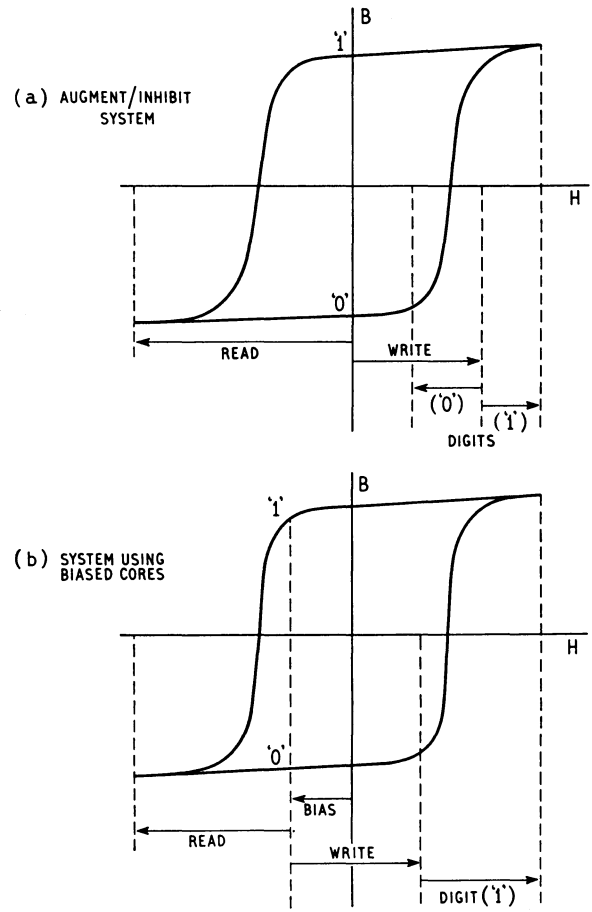

Fig. 4.3—Methods for increasing writing speed of word access store

The presence of a steady bias current, which can be carried by the digit wire, means that a given read drive requires a smaller amplitude read pulse. This read pulse can then be similar to the write pulse in amplitude which may simplify drive circuit design.

In both cases the total write current to store a " 1 " can be up to 50% larger than in the previously described systems so that the switching time for writing may be reduced by a factor approaching 3.

4.4. Drive circuits

Since the selection function has been removed from the matrix cores, more complex selection circuits are required for this system when compared with a coincident drive store. A switch matrix containing square-loop cores forms a convenient method of performing this operation. These matrices are discussed in detail in Chapter 8 and are only considered here with regard to their effect on the performance of the store.

Firstly, owing to imperfections in the switch cores, those lying on a selected row and column in the switch matrix will produce small outputs at the same time as the read pulse. These small currents in turn induce small changes of flux in the storage cores to which they are coupled and the corresponding voltages in the output wire are all in the same direction. In addition there will be a certain amount of direct pick up from the drive wire. Cross-talk may also take place between adjacent output wires. Hence if a matrix switch is used for selection the store output will be far from noise-free and although various schemes may be employed to reduce this noise it may well set a limit to the size of the store.

Secondly, the choice of inhibit or augment digit pulses may be influenced by the switch matrix. Writing is normally carried out as the switch core resets so that if an inhibiting system is used, when a larger amplitude write current is needed, this core may be allowed to reset more quickly and hence speed up the write operation. Against this the extra voltage developed across the switch core means that extra voltage and hence power dissipation is needed for the switch core driver. The latter was one of the main reasons for using an augment system in EDSAC II.[2]

The load presented to the switch core depends on the number of " 1 "s and " 0 "s stored in the address and is not constant. The lack of a constant load is an embarrassment in the design of a switch core matrix but may be overcome by inserting an extra resistive load which outweighs the effect of different stored information. Another method uses two cores per bit, the storage of a " 1 " or " 0 " depending upon which core is switched. This method also leads to easier output discrimination[3] and is discussed further in Chapter 6.

If a diode matrix selection circuit of the type described in Section 8.2. is used instead of a switch core matrix, small unwanted signals will again appear on drive wires as a result of the fact that the diodes are not perfect.

4.5. Comparison with coincidence system

The advantages of the word access system when compared with a coincidence system are listed below.

1. Only the selected core output is present on the output wire. This is a theoretical advantage which may be considerably modified in practice as described above.
2. The read current is not critical and has no upper limit on amplitude so that the access time may be short. The write current is also less critical than in a coincident drive system.
3. Matrix plane wiring is simpler. If a common output and digit wire is used, then only two windings are required in each core. This is a particular advantage with apertured plates (see Chapter 6).
4. By using the inhibit-augment system, inferior materials, less critical amplitude control of drive currents or higher writing speed may be used.

The main disadvantage of the system is that although the selection function had been removed from the cores it still remains a problem. The cost of the selection circuits is higher than those in a coincident current store of the same size and they are more difficult to design satisfactorily.

The fact that the word access system has not been much used suggests that it is not an attractive proposition for a large store using toroidal cores at normal speed. However, the system is used occasionally for larger stores when somewhat higher speeds are required or when apertured plates are to be used. The system is often preferred for small stores, particularly if each word contains a large number of digits since the output amplifiers can be less complicated than those of a coincident drive store.

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Chapter 5

FASTER STORAGE SYSTEMS

5.1. Introduction

During recent years an increasing number of mathematical problems have arisen requiring the use of much faster computers than are generally available in order that the computations involved might be completed within a reasonable length of time. The advent of newer types of transistor has led to the possibility of increasing the speed of logical circuits by at least a factor of 10 and there is consequently a growing need for stores which operate at speeds correspondingly higher than the 5–10 μsec cycle rates which have been common with coincident current systems. A small fast store with a large slower backing store is not a completely satisfactory solution to the problem and efforts are being made to construct large fast stores without vastly increasing the cost per bit.

In practice ferrites have provided the most suitable storage elements for a parallel access store operating with cycle rates up to 500 kc/s but at higher rates possible methods of using these tend to be more complex so that other techniques, notably the use of thin magnetic films and superconducting devices, have been investigated as an alternative. However, these also produce their own problems and are still in the development stage so that it is likely that ferrites will satisfy faster storage requirements in the near future.

Before describing various arrangements which have been proposed, the limitations in speed of the two systems already described will be discussed briefly.

Coincident drive systems using a pair of drive pulses as described in Chapter 3 are severely limited in speed by the materials available. Since $T(H - H_o) = S$ (see Fig. 2.3(a)), and in this system H_m is approximately $1{\cdot}3\ H_o$, then the switching time, T, is given by $S/0{\cdot}3\ H_o$. It has not yet proved possible to reduce S significantly. The coercive force has however been raised and

cores are now available which switch in 0·5 μsec and enable a cycle time of 2–3 μsec to be achieved. Because of their high drive pulse requirements these are made in the smallest possible sizes but full switching currents of about 700 mA are still required. For this reason it would appear that any further increase of speed by this means will be difficult. A further complication arises from the self heating of cores switched at these speeds which might render their use in coincidence systems unreliable owing to the consequent change of coercive force. The heating problem can be overcome to some extent by more efficient cooling.

A word access store of the type described in Chapter 4 may be made to operate faster than a coincident drive store when using cores of the same material. The maximum speed is then controlled by the writing operation but by using the augment-inhibit method or an augment system in conjunction with a standing bias a considerable increase in speed may be achieved. The same objections regarding high drive currents apply since a high coercive force material is required and the amplitude of the write current must be fairly well controlled. For these reasons it is doubtful whether a cycle time of much less than 2 μsec is possible with available materials in this system.

5.2. Multiple coincidence systems

The idea of using multiple coincidence driving as a means of increasing speed has been referred to in Chapter 3. As mentioned there this form of storage suffers from several disadvantages including the elaborate selection circuits required and above all the complicated matrix plane wiring. In view of these the system is not an attractive proposition.

5.3. Two core per bit system using one storage and one switch core

Switching speed limitation caused by the limitation of drive in coincidence systems has been eliminated during reading in the direct selection system already described, but remains during writing. The next step is to consider the possibility of removing this restriction during writing also by performing selection external to the storage core. Since a core forms a convenient switch as well as storage element the use of more than one core per digit stored would appear to provide a solution to the problem.

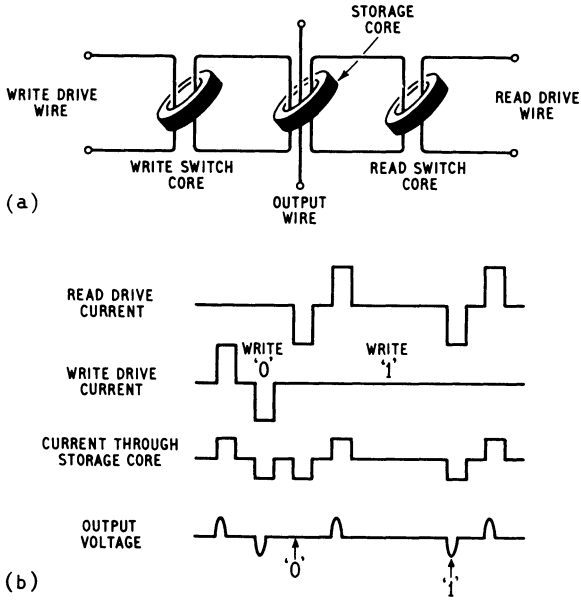

Fig. 5.1—Principle of storage system using separate storage and selection cores

A method of connecting and driving the cores has been described[1,2] and is illustrated in Fig. 5.1(a) where separate switch cores are used for reading and writing. Writing is accomplished by applying consecutive drive pulses of each polarity to the write switch core to store a " 0 " and applying no drive pulses to store a " 1 ". Reading is accomplished by applying consecutive drive pulses of each polarity to the read switch core. These pulses together with the corresponding current pulses induced in the small coupling loops and the storage core outputs are shown in Fig. 5.1(b). It is assumed here that a " 1 " is stored when no write drive pulses have been applied since by convention a " 1 " output is usually considered to arise when the storage core switches during reading.

It can be seen that a read/write cycle consists of four successive periods in which a drive pulse may occur. These may in fact be compressed to three since the second read pulse drives the storage

core in the same direction as the first write pulse and may therefore coincide with it.

In a practical store, to enable selection to be performed easily, it is convenient to arrange the read and write switch cores in separate coincidence driven biased switch matrices. The second pulse of

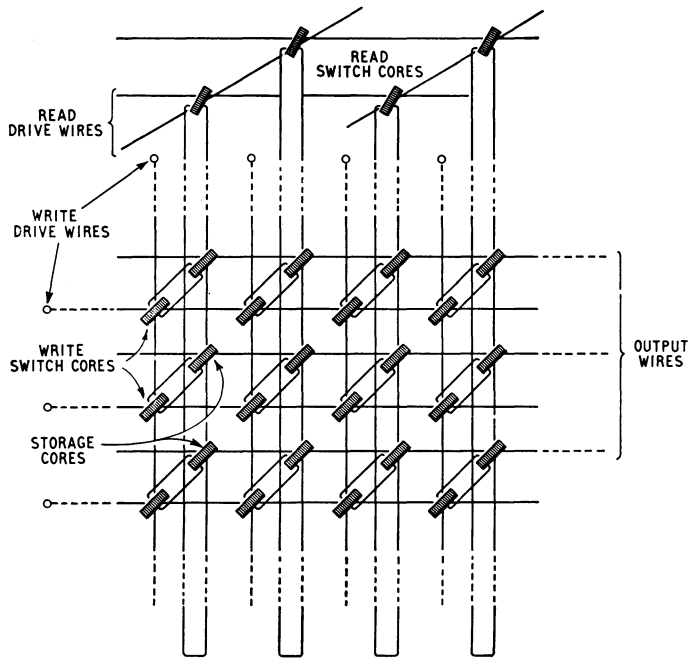

Fig. 5.2—Complete system using separate storage and selection cores (bias wires in read and write switch core matrices are not shown)

the read or write cycle will then be derived by the resetting of these cores under the influence of the bias current when the drive pulses are removed. A common read switch core can be used for all digits in one word since the same operation is needed at the same time. Thus the reading method is identical with that of the word access store of Chapter 4. This means that the system reduces in practice from three to a little over two cores per bit as shown in Fig. 5.2.

For writing into the store the drive wire carrying a half drive pulse to the same digit position in each word becomes the digit

wire. Alternatively this wire may be used to carry the bias current in which case the bias will be removed when a " 0 " is to be written. A separate bias wire is then unnecessary.

A greater flux change should occur in the switch core than is required to switch the storage core in order to allow for losses in the coupling loop. Furthermore during a read/write cycle there may be occasions when a change in flux in the switch core drives the storage core further into saturation so that only a low impedance is presented by the latter. To allow the switch core to change state in a reasonable time under these conditions it is essential that the coupling loop contains some resistance and it may well be constructed of resistance wire. This again leads to losses and it has been stated[2] that for best operation the switch core should contain at least six times as much flux as the storage core.

Drive currents for this system although large, are not as critical as in coincidence systems. A ferrite of low coercive force is now an advantage if the lowest possible drive current for a given speed is required.

The main disadvantages of the system lie in the difficulty of inserting the coupling loops and the large amplitude of drive current required. Temperature rise may also be a problem at high speeds although a less troublesome one than may be encountered in a coincidence system. In this case a reduction of coercive force through a rise in temperature is not important but the reduction in the saturation flux might be more serious since a core written into when hot and read from later when cold will tend to generate a large " 0 " or a small " 1 " output.

As far as is known, no large store has been contemplated which makes use of this system but it is of interest in that it forms a logical extension of the idea of separating gating and selection which has been partly achieved in the system of Chapter 4. Now that higher speed storage is required it seems worthy of consideration if the practical difficulties of wiring and driving can be solved.

5.4. Two core per bit system using two storage cores

Increasing speed by applying to the core a considerably higher field than in a coincidence store, as for example in the direct selection and two core per bit systems described above, gives rise to three problems as a result of this extra drive. Firstly more power is required to switch the core, secondly the ratio of the flux changes between a " 1 " and a " 0 " output is less, and thirdly more heat is

produced in the core and may further decrease this ratio. A system which partly overcomes these problems will now be described.

In Chapter 4 it was mentioned that two storage cores per bit have been suggested as a method of presenting a constant impedance to the drive circuit regardless of the information stored and also as a means for easing discrimination between a " 1 " and a " 0 " output. An extension of this idea can be used to provide a much faster storage system. This system differs in that short current pulses are used which only partially switch the cores during the write process.

A word access system is used. For each digit stored two cores are arranged in the manner shown in Fig. 5.3. They both receive a digit pulse, but in opposite directions in each core with respect

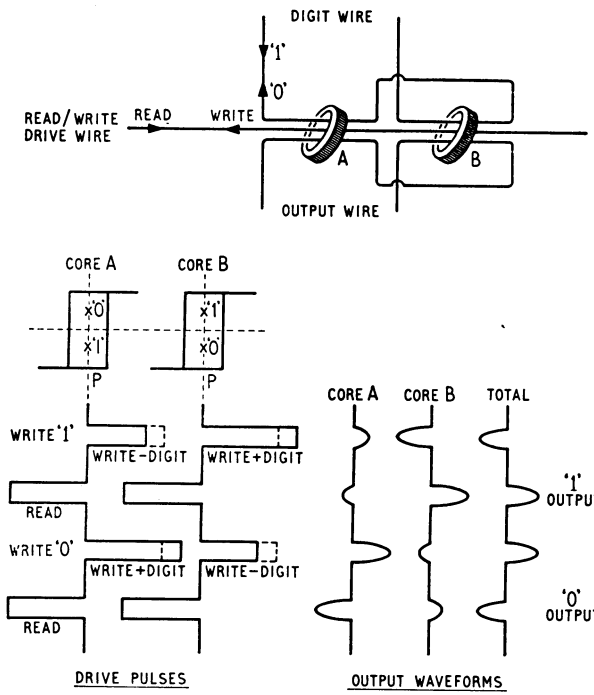

Fig. 5.3—Principle of storage system using two storage cores per bit

to the write pulse. The digit pulse which is applied coincidently with the write pulse is of one polarity if a " 1 " is to be written and of the opposite polarity for a zero. The net result of this operation is that one core, in which the digit pulse adds to the write pulse, experiences a larger drive than the other, in which the two pulses

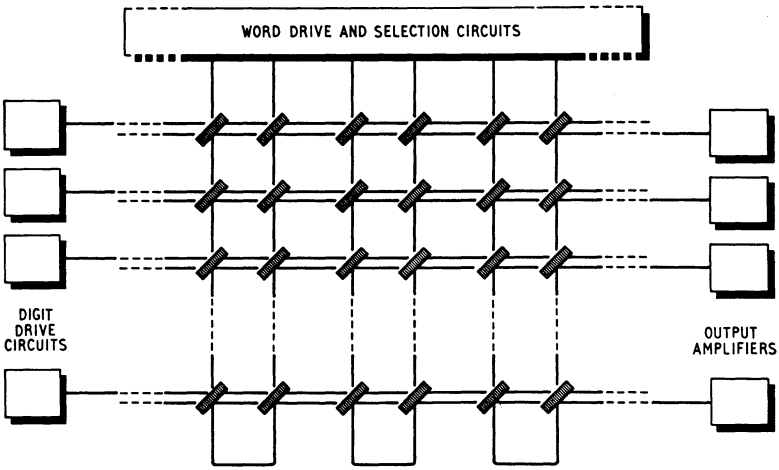

Fig. 5.4—Matrix wiring or two storage cores per bit system

are in opposition, and will consequently switch further from state P during the writing period as illustrated in the figure. When reading takes place both cores are returned to P and the output of the core which was switched further will be greater than the output from the other. Since these outputs are in opposition on the output wire, the polarity of the combined output indicates which digit was stored.

In this system two core effects are met which do not arise in conventional matrix stores used at lower speeds. Both of these are advantageous though not essential for the basic storage principle as described above.

The first concerns the switching time of cores when they are driven into saturation from various values of remanent magnetization. Fig. 5.5(b) shows the outputs obtained by applying a constant amplitude read pulse to a core which has been previously set to

remanent states *A* to *D* in Fig. 5.5(a). It can be seen that considerably lower switching times are obtained from a partially switched core than from a core which is switched from one saturation state to the other, although the exact switching time from a given state depends to some extent on the setting pulse used.

The second property is concerned with the viscosity effect which has also been found in metal tape cores.[3] Pulses very much larger

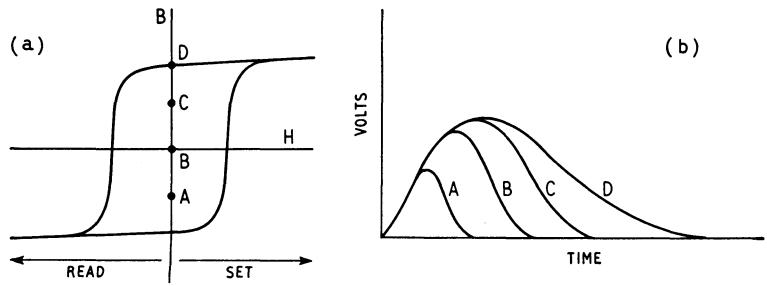

Fig. 5.5—Outputs from a partially switched core

in amplitude than the d.c. coercive force may be repeatedly applied to a saturated core without causing any appreciable irreversible change of flux, provided that the pulses are shorter than a certain length which varies inversely as the amplitude. The curves of Fig. 5.6 show the amount of switched flux plotted against driving field for various drive pulse lengths. It can be seen that the viscosity effect which is only significant for drive pulses shorter than 0·1 μsec leads to a higher rate of change of Φ with H than would result if the effect did not exist as indicated by the dotted lines. This means that even with a fast write pulse of large amplitude the two cores can be set to significantly different states of flux without using a large digit pulse.

The apparent advantages of this system are as follows:—

5.4.1. HEATING

Problems caused by self-heating of the cores only arise at a much higher repetition rate than in the system described previously. In the first place, since only partial switching occurs the amount of heat generated is less. In addition and more important, although the quantity of flux stored may change with temperature,

it is a flux difference which is used to determine the stored digit and the sign of this difference will not change.

However, temperature changes are of some importance if really high speeds are contemplated since at higher temperatures both cores will switch too far during writing and the resulting output amplitude will fall. In the limit both cores might switch completely and provide zero output. Some simple form of cooling helps to reduce this effect considerably.

5.4.2. PLANE WIRING

Storage plane wiring is simple in principle, Fig. 5.4. Only co-ordinate wires are required and no diagonal wires or small coupling loops are involved. In practice it may be a problem to reduce the direct pick up between drive and output wires to an acceptable level. A common wire can be used for digit pulse

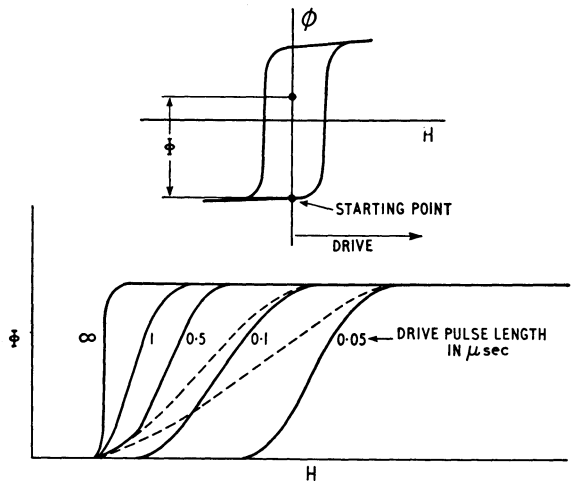

Fig. 5.6—Flux setting by pulses of restricted length

and output, in which case only two wires need thread each core. This might be particularly advantageous if very small storage cores are used, though simplification of associated circuits may be of more importance and make two wires preferable, including separate wires, for the read and write pulses.

5·4·3. OUTPUT DISCRIMINATION

Discrimination between a " 1 " and a " 0 " output should be much easier than in systems where they are of the same polarity but of different amplitudes.

5·4·4. DRIVE CURRENTS

None of the drive pulses are critical in amplitude. In order to ensure that both storage cores are always returned to remanence the read pulse should be larger than the sum of the write and digit pulse. Alternatively the same result may be achieved by making it slightly longer since under these conditions the total flux change is approximately proportional to the product of the drive ampere turns and the time for which they are applied.

Digit pulses for " 1 " and " 0 " should be similar in magnitude.

5·4·5. DRIVE PULSE GENERATORS

Regardless of the information stored, the same impedance is always presented to the drive pulse generators by the storage cores. This may be an advantage when considering the design of these circuits.

The variation of output amplitude with write and digit drive is shown in Fig. 5.7 for a pair of 1·25 mm storage cores typical of the type used in coincidence systems. The peak of these curves occurs where the write pulse is of sufficient magnitude to half switch the cores if the digit pulse is absent. They fall to zero at low values of write drive where neither core switches appreciably and at high values where both are completely switched. In practice, at high drives a small constant value of output will result since there is likely to be difference in saturation flux in the two cores. The output for any given write pulse is larger for a higher value of digit pulse since the flux difference stored is then larger. However, the digit pulse cannot be increased indefinitely without changing the state of cores in other addresses through which the digit wire passes, but provided that the digit current amplitude does not exceed about one third of the value equivalent to the coercive force, there will be no significant loss of information.

Drive pulses from 0·1 to 0·5 μsec duration cover the useful range for this system so that a read/write cycle time as short as 0·5 μsec may be obtained. As an example of the drive currents required and the outputs to be expected, 1·25 mm cores with a coercive force of 1 Oe need from about 1 A for 0·1 μsec falling to

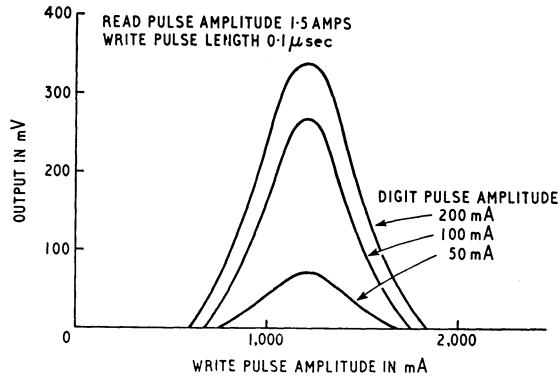

Fig. 5.7—Variation of output amplitude with write and digit drive for a pair of typical 1·25 mm storage cores

0·4 A for 0·5 μsec as the write pulse. Outputs will in these cases be 300 mV and 70 mV respectively for a digit pulse of 75 mA assuming that the read pulse is similar in magnitude to the write pulse.

It is obvious that here again a low coercive force material is advantageous in order to reduce drive requirements. Smaller cores also help in this direction and will provide an output of reasonable amplitude when subjected to the drive pulses necessary for the operation of the system.

There appears to be no reason why the function of the two cores could not be combined in a single storage element as for example in Fig. 5.8 where two possibilities are shown. In this case the write pulse will partly switch the whole core, the majority of the flux change being along the path where it is assisted rather than opposed by the digit pulse. Saturation in the opposite direction will be caused by the read pulse and the difference in flux change in paths *A* and *B* will generate the output. These devices would only be useful if flux path lengths and hence drives could be made comparable with those in a small core. Another alternatve element might be the apertured plates described in Chapter 6.

This general storage method would appear to be a strong contender for higher speeds. A store of about 75,000 bits which uses a similar principle has been described[7] in which a cycle time of 0·7 μsec is achieved.

In Chapter 7 a modification of this system to provide non-destructive read-out is described.

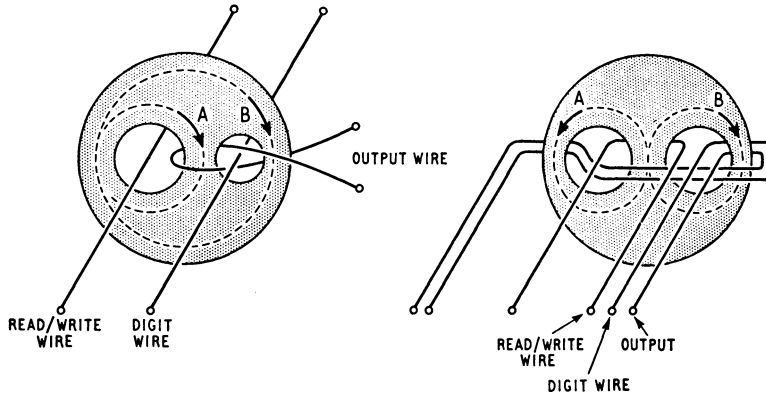

Fig. 5.8—Alternative methods of using a flux difference for high speed storage

5.5. Coincident Flux System

In the coincident flux system as originally described[4] a core shape is used such that there is no flux change in the flux path linked by the output wire when a single drive is applied, however large this drive may be. Only the presence of two coincident drives can switch the flux in this path, and, since there is no amplitude limitation on these, very fast switching may be achieved.

The system uses a three holed device as shown in Fig. 5.9(a). If X and Y are energized simultaneously with equal current pulses of the correct polarity, the effect is the same as a drive pulse coupling the whole core through hole B since the total current through hole A is zero. This means that coincident pulses on X and Y can be used to switch the total flux round hole B to saturation in either direction depending upon the polarities of X and Y. These operations may be considered as writing and reading a "1" which is stored in leg 4 which is linked by the output wire.

In order that the element may be selected by coincident current pulses a drive on X or Y alone should not affect the flux stored in leg 4. When only one pulse is applied, several types of flux change are possible depending upon the flux state present as a result of previously applied pulses. Of these, some may involve a flux change around hole B, but none affect the flux stored in leg 4. Two examples of the flux patterns occurring before and after a half drive are illustrated in Fig. 5·9(b). The principle upon which

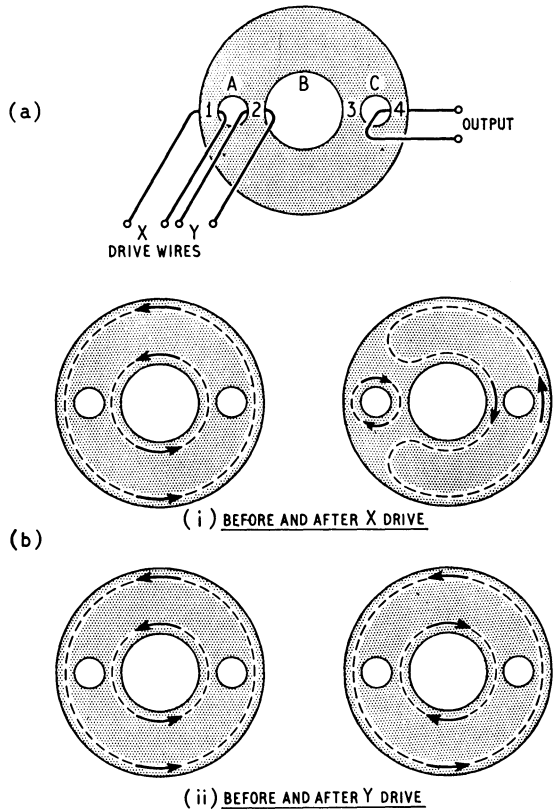

Fig. 5.9—(a) Coincident flux device (1), (b) examples of flux pattern changes produced by half drives

satisfactory operation depends is that the reluctance of a flux path round hole *B* and through leg 3 is substantially less than that of a similar path through leg 4 in order that leg 3 switches preferentially when only one drive is applied. Thus the presence of both drives is essential if leg 4 is to change state. This is a different principle from the coincidence systems hitherto described in which only a required drive amplitude is obtained by coincident pulses.

A digit wire may be threaded through hole *A* and carry a current to oppose the *X* drive when necessary and so enables a parallel

access store with X and Y windings common to all digits to be built.

A more practical development of this idea has been described[5] and is shown in Fig. 5.10. A rectangular core is used with rectangular holes arranged so that the difference in length between the flux paths around the centre leg and through the inner and outer legs on the output side is considerably larger than in the core described previously. Another difference is that a bias winding is used in conjunction with the drive which is applied through the centre hole. X and Y drives are in this case applied coincidently

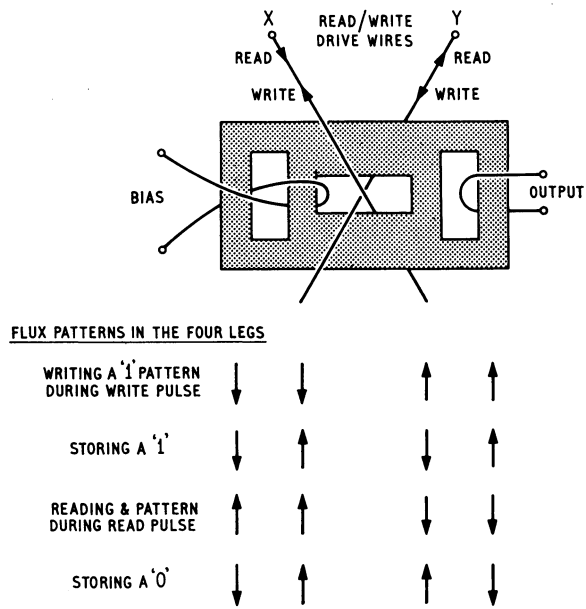

Fig. 5.10—Coincident flux device (II)

in order to obtain a required amplitude, one drive pulse being insufficient to overcome the bias and cause switching. An advantage of this scheme over the former are that no back voltages arise from half selected cores so that the drive power required is reduced. Only two static states exist for the whole element since the bias

winding returns the two legs coupled with it to the same state every time a full drive is removed. The operations of reading and writing are shown in the figure.

Output pulse widths of 0·1 μsec are claimed for this device together with an adequate " 1 " to " 0 " output ratio. The main

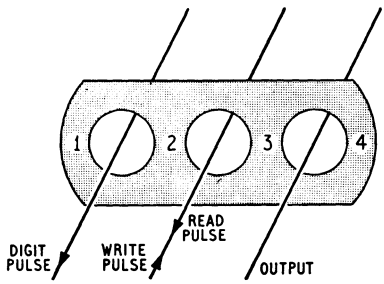

Fig. 5.11—Alternative method of storage in three hole device

disadvantages would appear to be that the complex core shapes would be expensive on the basis of cost per bit of storage and inevitably somewhat larger than the smallest toroidal memory cores. Apart from making the store bulky, this large size means that large driving currents are involved. Multi-turn windings allow smaller currents to be used but increase the constructional problems and introduce delays due to the extra inductance in the drive wires. For these reasons the system in the form described does not appear to offer a solution for a large fast store. It does, however, form a useful technique for a smaller store.

A variation of this principle[6] which can be used in a word access system is shown in Fig. 5.11. Here a single drive wire which carries the read and write pulses passes through the centre hole and a digit wire passes through the left hand hole. To write a " 1 " the digit wire is not energized so that the complete flux around the centre hole is switched in a clockwise direction. This is returned to an anti-clockwise direction by the read pulse so that an output is generated in the output wire. To write a " 0 " a digit pulse is applied coincidently with the write pulse and is used to prevent any flux change in leg 1. This in turn prevents a flux change in leg 4 so that when a read pulse is applied there will be no flux change in this leg and no output in the output wire.

The storage methods described in this section are special cases of a general system of logic which makes use of multi-apertured devices. This is discussed further in Section 11.2.

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Chapter 6

APERTURED PLATES

6.1. Properties of a hole in a block of ferrite

Large matrix stores containing perhaps millions of cores are expensive to construct. A major part of the cost is due to the time involved in wiring so that any system which reduces this time significantly would be attractive. One method which has been developed[1,2] towards this end makes use of a different type of storage element consisting of a hole in a block of material. The material adjacent to the hole is used in a similar manner to the material in a toroid but its properties are slightly different and are described below. Since one block may contain a large number of elements the number of separate components to be handled during assembly may be drastically reduced and, provided that dimensional tolerances are small, wiring is correspondingly simplified. In addition there is the possibility of printed wiring in the form of a conductor coated on the block. Another advantage is that the hole diameter may be small so that lower drive currents are required and are more easily provided.

One main difference between a core and a hole in a block is that in the latter the amount of flux which can be switched by a drive pulse on a wire threading the element is not determined by the cross-sectional area of material but by the amplitude and duration of the pulse. The field, H, experienced by a toroidal section of material at radius r from the hole centre is proportional to $1/r$ so that for a step function of drive current the switching time t which is proportional to $1/(H - H_0)$ will increase with t becoming infinite at a radius r_0 where $H = H_0$. No irreversible switching takes place outside this limit. Thus upon the application of a step function drive pulse a boundary can be envisaged radiating from the hole, inside which switching is completed. It can be shown[2] that the penetration of this boundary with time follows an approximately exponential rise to the limit r_0 and since the output

amplitude is proportional to the rate of change of flux this amplitude will fall quite rapidly as r increases. The output waveform does in fact look rather similar to that of a toroidal core except for a slightly longer " tail ". However, one important difference is that an increasing drive only produces an increase in amplitude and does not reduce the switching time which remains fairly constant after a certain value is reached.[3,4] This effect is due to the larger volume of material which contributes to the output from a larger drive pulse and may easily be shown by considering the block to be composed of a series of concentric toroidal elements and summing the outputs from these.

Coincident current switching time is not very different from that of a toroid. In practice, switching in the outer regions of the switching area where r approaches r_o will be stopped by the arrival of the rear edge of the drive pulse which need not extend beyond the point where the output amplitude has fallen to 10% of its peak value.

The main disadvantage of the element is that a larger volume of material contributes to the unwanted outputs due to reversible flux changes. These extend well beyond r_o and are fast. As a result the disturb outputs are expected to be about three times as large as those from a toroid of similar material[2] and make this type of element less suitable for a straight-forward coincidence system using one core per bit. They are however very useful for direct selection or coincidence systems using two cores per bit as described in Section 6.3.

By placing the holes near an edge of the block their properties may be improved[2] since the reversible flux change is then limited. This is not practicable if a large number of holes is required in a small piece of ferrite but adjacent holes may also serve a similar purpose. It has been suggested that an optimum spacing occurs when the distance between centres is twice their diameter.[1] This distance is a compromise between discrimination improvement and interaction between holes.

6.2. Characteristics of Rajchman Plate

Plates containing holes which have been pressed[1] and drilled[2] have been described. The former technique would seem to be more suitable for mass production. As far as is known the only successful pressed plate made so far is that described by Rajchman, with which the remainder of this chapter is concerned.

This plate, a portion of which is shown in Fig. 6.1, contains 256 holes arranged in a 16 × 16 array. The whole plate is only 0·83 in. square with hole diameters of 0·025 in. separated by 0·05 in. between centres and with a thickness of about 0·007 in. One method for printing a winding which links every hole in series is

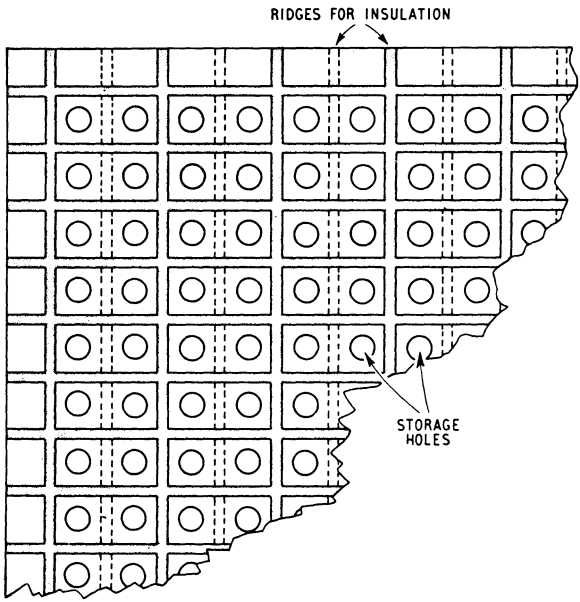

Fig. 6.1—Section of Rajchman plate

accomplished by covering the whole plate with a metal conducting layer and then removing this layer from the top of the appropriate ridges. This winding can then be used as a combined digit and output wire.

The accuracy obtained in the positioning of the holes is such that it is possible to thread a wire through corresponding holes in a stack of several plates. Thus, the amount of wire threading to be carried out in the construction of a complete store has been reduced to a small fraction of that required for a core assembly.

The nominal drive current necessary for coincident current

operation is 330 mA which provides an output of about 30 mV with a switching time of 1·5 μsec.

Testing can be performed by a multiple probe core handler and, by selecting the holes sequentially, the outputs can be shown superimposed and their envelope used to measure the properties and uniformity of the holes simultaneously.

6.3. Storage systems using Rajchman Plate

A complete stack of Rajchman Plates may be operated in either a coincidence or direct selection system.[1] Holes in plates have characteristics somewhat inferior to carefully selected toroids but perform sufficiently well to permit their use in a 32 × 32 plane when driven coincidently.[5] In order to provide cancellation of unwanted outputs in a 16 × 16 array it is necessary to use a pair of holes for each digit stored. Two holes per bit are also an advantage in direct selection systems but this is a less serious complication than it would be in a core store since virtually no extra wiring

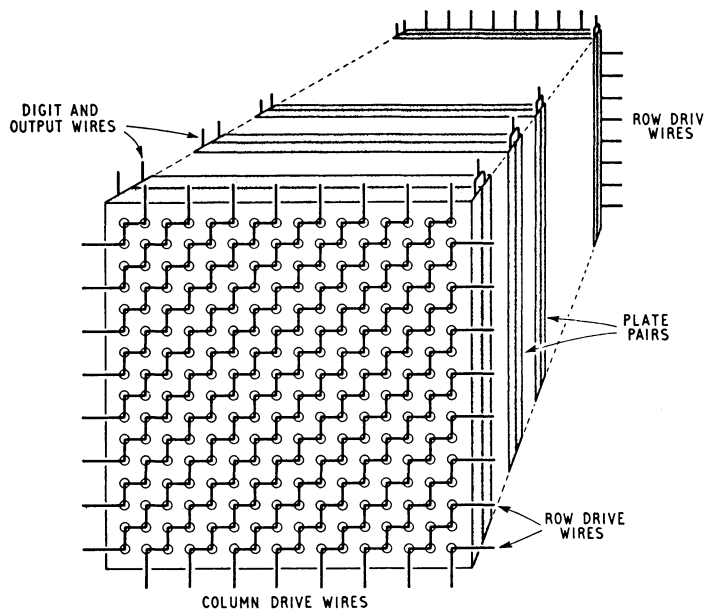

Fig. 6.2—Arrangement of Rajchman plates in coincidence system

is required, the only additional cost being the extra plates. Corresponding positions on two adjacent plates are used for the pair of holes and only one of these holes is switched during writing, the choice depending upon the digit to be stored.

6.3.1. COINCIDENCE SYSTEM

A coincidence method is achieved by wiring the plates as shown in Fig. 6.2. In one plate the wiring is such that the disturb outputs from the half selected holes in the energized row and column do not cancel out in the manner described in Chapter 3. This is the reason for using the two plates with their output wires connected in series opposition. Thus, on reading, the disturb outputs from one plate tend to cancel those from the other. The digit pulse is applied to only one of the plates to inhibit switching during writing and as the output windings are in opposition the polarity of the output signal will indicate which plate contained the switched hole and hence the stored digit.

An alternative method[5] for reducing the disturbed output and at the same time only using one hole per bit uses four plates in each plane arranged as a 32×32 matrix. In this case the output wires of the four 1×16 plates are connected in series in such a way that the disturb outputs from the plate containing the selected core are cancelled by the disturb outputs from the other two plates through which the selected row and column wires pass.

However the success of the coincidence method will depend very much on the uniformity of holes in one plate and between plates although the usual aids for discrimination, such as strobing the output, may be applied in the same way with this device as with coincident drive core stores.

6.3.2. DIRECT SELECTION SYSTEM

Less stringent requirements are placed on the properties of the holes and also on the drive pulses if a direct selection system similar to that described in Chapter 4 is used. In this case the main purpose of the two holes per bit is to provide a fixed load impedance which is independent of the stored information. To provide drive pulses similar plates may now be stacked on the end of the store and used as a biased matrix switch of the type described in Chapter 8. Straight wires are threaded through both store and switch plates in the same wiring operation which is an advantage over a core

switch. Row and column drive windings are also required in the switch plates but the printed winding can be left out.

The common digit and output wires of pairs of plates in the store are again connected in series opposition but in this case the digit pulse may be applied to both plates in one direction for a " 1 " and in the other for a " 0 ". The polarity of the output indicates the stored digit and is here free from disturb outputs from other holes.

The flux change in the storage plates is limited to that taking place in the switch. This allows the drive currents to be particularly non-critical[6] since it is no longer necessary for switching to be entirely confined to one hole of a pair but a flux difference between the holes may be used instead. This method is very similar to that described in Section 5.4 for a fast store and may also be used here to obtain considerably faster speeds than those resulting from coincidence driving.

A transistorized store using this technique has been described[3,4] in which a cycle time of 10 μsec was achieved. Current pulses of about 500 mA were required for the switch drive windings and were obtained from 10:1 step-up transformers driven by transistors. Digit currents of about 100 mA were used.

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Chapter 7

NON-DESTRUCTIVE READ-OUT

7.1. Introduction

In the storage systems already described the reading process destroys the information which was stored in the element. Re-writing is thus necessary even when the stored information is to be unchanged. This is not a serious disadvantage since practically no extra equipment is involved. In addition the information already present must be destroyed before new information can be written since a writing operation, at least in the systems described in Chapters 3 and 4, will not change a stored " 1 " to a " 0 ". This means that three types of drive operation, read, write, and clear, would be required for a non-destructive read system as against two for the usual method. For these reasons little effort has been applied to the investigation of non-destructive read-out systems in the past.

The desirability of higher speeds has led to a renewed interest in non-destructive reading for two reasons. Firstly, time will be saved if there is no necessity for a rewrite operation and, secondly, if the reading operation does not involve switching the core from one remanent state to another, less power will be required from the drive circuits and less self-heating will occur in the core. The latter is particularly important if very high reading speeds are contemplated.

This chapter is only concerned with methods for determining the state of a core without causing irreversible changes of flux. Other methods such as those described in Chapter 9 for permanent and semi-permanent stores are also non-destructive but involve core switching and are not applicable to a temporary store where the information is to be changed frequently.

Non-destructive read-out in a store using multiholed devices is described in Chapter 11.

Although no large store using non-destructive reading has been

built two general methods have been published and the principles of both are described below.

7.2. Perpendicular field method

One method for determining the state of the core involves the application of a magnetic field parallel to the axis of the core,

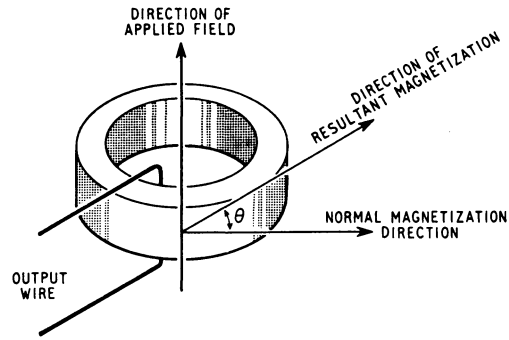

Fig. 7.1—Principle of non-destructive read out by means of perpendicular field

i.e. at right angles to the preferred directions of magnetization.[1,2] A field of this nature will cause a change in the direction of magnetization as shown in Fig. 7.1 without switching the core irreversibly. As a result the tangential flux linked by the output wire will be reduced from Φ_M to $\Phi_M \cos \theta$ and an output proportional to the rate of flux change will appear. The polarity of the output signal will indicate the digit stored. Since these flux changes do not involve domain wall movement they may be extremely fast and will follow the rise time of any field which is practicable. Thus for fast rise times the outputs may be quite large in amplitude. The main problem here is to devise a suitable method for generating the interrogating field. Suggested methods[2,3] include a hollow toroid, inside which lies an interrogation winding, and a block of ferrite containing holes at right angles, which is described below. For a magnetic tape core, the tape itself may be used as the winding for providing the non-destructive read.

The presence of a perpendicular field during writing enables a core to be switched with a lower drive[3] so that writing and

clearing might be performed by coincident application of this field with a normal drive of insufficient amplitude to switch the core by itself. Thus the same circuit may be used for writing, clearing and non-destructive reading with a consequent saving in cost. Faster switching may also be accomplished by this means.

Of these suggestions the block containing two holes at right angles, Fig. 7.2(a), would appear to be the most practical. The material surrounding one hole is used as the storage element. Information can be written into this element by the normal methods

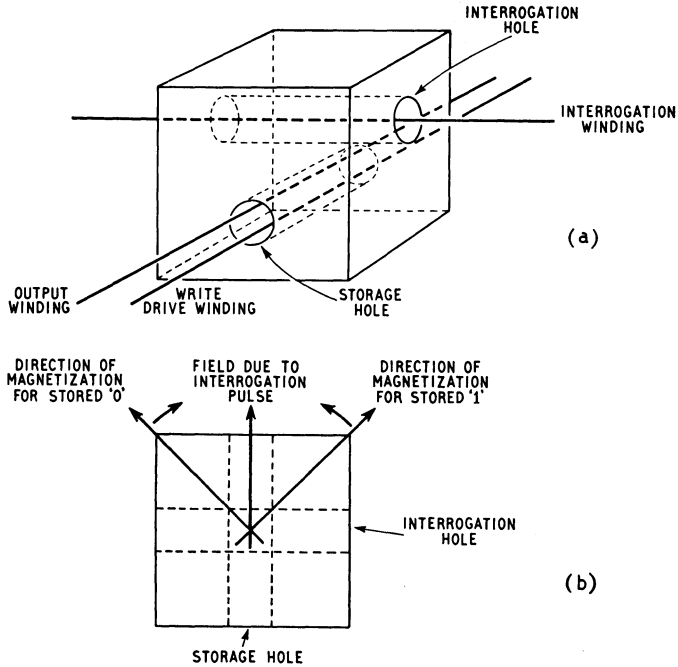

Fig. 7.2—Non-destructive read in ferrite block

employed for writing into a toroidal core but a direct selection system enables faster writing to be achieved. After the write pulse has terminated the material in the region between the two holes remains saturated but the flux is shared between the paths

around the two holes so that the resultant direction of this flux is midway between the directions of the applied fields when the drive wire through either hole is energized. This is illustrated by the vector diagram in Fig. 7.2(b). When the read pulse is applied this vector will rotate and the flux linking an output wire through the storage hole will be reduced. The polarity of the output waveform indicates from which direction the flux vector moved so that a stored " 1 " and a stored " 0 " provide outputs of opposite polarity. Removal of the read pulse allows the flux vector to return to its original direction which means that the reading operation is non-destructive.

7.3. Permeability difference methods

As can be seen from Fig. 2.1 the slope of the hysteresis loop in the region of saturation is not constant but decreases gradually from the knee of the loop towards saturation. This fact can be used to determine the state of the core without using drive pulses large enough to cause irreversible switching. Since the flux changes caused by small fields in these regions are reversible they are also fast so that a fast non-destructive read system should be possible.

However, the flux changes are small and a direct comparison between the outputs resulting from drives towards saturation and towards the knee would not form a satisfactory method for discrimination between a " 1 " and a " 0 ".

One possible method described[5] uses the non-linearity of the loop to perform a mixing operation on two sine wave drives applied coincidently along the selected co-ordinate wires of a matrix plane. Among the frequencies appearing on the output wire will be the difference frequency which may be easily isolated if the drive frequencies are sufficiently close together. The phase of the difference frequency depends upon the sign of the change of slope of the hysteresis loop over the range used so that the state of the core can be deduced. In order to increase the output amplitude the drive waveforms may exceed the d.c. coercive force if their frequency is high enough since any irreversible change resulting from one half cycle appears to be cancelled by the next.

The above system is not very practical owing to the need for elaborate drive and output circuits in addition to the normal pulse drive circuits. It is also doubtful whether the read operation could be made fast enough to provide any useful gain in speed over destructive reading and rewriting.

Another method using pulse drives rather than sine waves appears to be more promising.[9] Although, as mentioned above, a direct determination of the core state by comparison of outputs resulting from small drives towards saturation and towards the knee of the loop is not feasible, an extension of this principle using

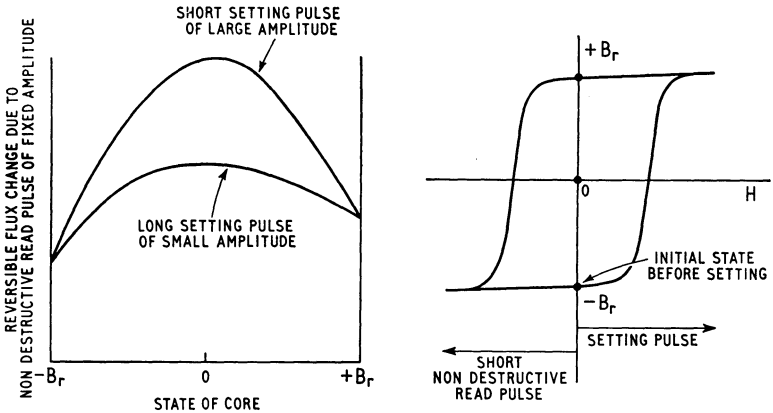

Fig. 7.3—Variation of reversible flux change with the average magnetization in a core

a pair of cores for each digit stored offers a considerable improvement. A wiring arrangement for the two cores is the same as that described in Section 5.4 and illustrated in Fig. 5.3 for a high speed destructive reading system. A similar writing method may be employed here in which a digit pulse, I_D, is added to a write pulse, I_W, in one core and subtracted from it in the other so that the two cores may be switched to different flux states. When reading non-destructively, a read pulse of insufficient amplitude to cause significant irreversible flux change is applied in the same direction as the read pulse in the fast destructive reading system. In this case, however, the difference of the reversible flux changes in the two cores will appear on the output wire. These flux changes are comparatively small but an output voltage of a few millivolts can be obtained from a read pulse with a fast rise time. The variation of reversible flux change for a fixed read pulse with the state of magnetization of the core is shown in Fig. 7.3 for different setting drives.[6] It can be seen from this that the two saturation states

do not provide the maximum difference in output. It is preferable in the system that one core should be set to approximately the zero magnetization state by the drive $I_W + I_D$ and the other should be unaffected by $I_W - I_D$ so that it remains in the saturated state. It can also be seen that a much larger difference in outputs between the saturated state and the state of zero magnetization results when a short, large amplitude pulse is used for setting rather than a longer pulse of smaller amplitude.

If very short (about 50 mμsec or less) read pulses are used, the amplitude of these pulses may exceed the value equivalent to the coercive force by a large amount without switching the core irreversibly. The use of this effect, which is similar to that described for metal tape cores,[7] and which has already been mentioned in Chapter 5 enables larger output signals of some tens of millivolts to be obtained. Low coercive force materials are advantageous in order to reduce drive currents.

One problem with the system might be the generation and propagation of the fast drive pulses required. With the writing system described above both cores must be switched back to the same saturated state by a clear pulse before information can be inserted, although the circuit which produces the read pulse might also be used to provide the clear pulse.

It is also possible to determine the state of the core by applying a drive pulse which tends to reduce the total flux to zero. The polarity of the signal on an output wire threading the core will then indicate the direction of remanent saturation. One method[8] for driving a core in this way involves the use of a core containing three apertures as shown in Fig. 7.4(a). A current pulse on the wire threading the two smaller holes will tend to drive the core towards the state shown in the diagram in which the flux in the top half of the core is equal and opposite to that in the bottom half and the total across any radial section is zero. If the drive is not large enough to cause irreversible changes, one of the minor loops A in Fig. 7.4(b) will be followed depending upon the initial state. Even if the drive is large enough to reduce the total flux to zero, the elastic properties of the core will ensure that a residual flux returns when the drive is removed and the minimum change after a large number of read pulses will result from one of the minor loops marked B. Thus, there is no limit on the amplitude of the read pulse and comparatively large outputs can be obtained. Normal coincidence methods can be used for writing but here again

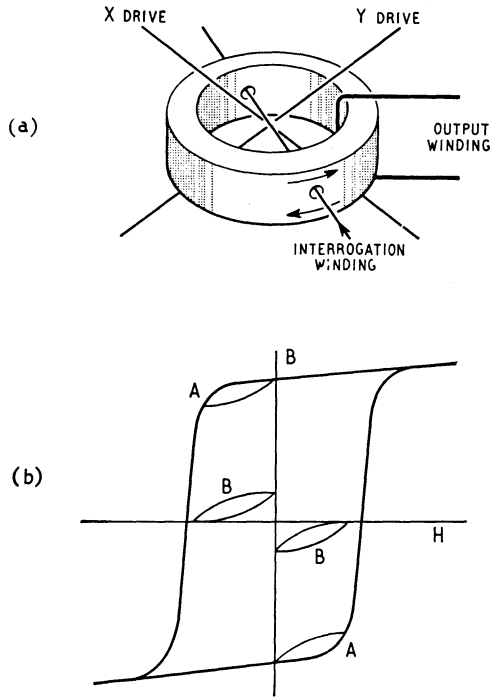

Fig. 7.4—Non-destructive read using multi-apertured core

the core must be cleared to the " o " state before the write pulses are applied.

All the systems described above suffer from the defect that the writing operation is not very fast and the time needed for changing information is very much longer than that required for a reading operation. They are, thus, not particularly useful from a speed point of view unless the ratio of the number of read operations to the number of times the stored information is required to be changed is higher than about 4:1 but even above this they may not be economically desirable. This ratio is approximately the average ratio required in most present day computers.

However, they are capable of an extremely fast access time and the information may be extracted repeatedly at rates approaching 10 mc/s. Thus their main use unless fast writing can be achieved

will lie in stores for special applications where the information is to be changed relatively infrequently.

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Chapter 8

MATRIX STORE DRIVE AND OUTPUT CIRCUITS

8.1. Introduction

In order to insert and extract the information in the storage elements of a magnetic matrix store fairly elaborate electronic circuits are required. These circuits, which must be regarded as part of the store when assessing the merits of a system, account for a large fraction of the total cost and are also the most likely source of any unreliability. Thus, since the possible practical arrangements of the storage elements themselves are limited and well known, the success of a store depends mainly upon efficient design of the input and output circuits.

The block diagram of Fig. 8.1 shows the general arrangements of the major circuits essential for the operation of a typical random access coincident current store. The greatest design problems are undoubtedly connected with the drive and selection circuits for the matrix rows and columns and it is with these that this chapter is mainly concerned. The problem is basically one of partly decoding outputs from the address registers and using the result to direct a suitable drive pulse to the selected row and column. In a direct selection system of the type described in Chapter 4 the corresponding circuits are similar but are relatively more complex owing to the absence in the matrix stack of the final decoding operation, which takes place in the coincident current arrangement.

Several methods for performing row and column selection have been proposed. During the early years of matrix store development all systems relied upon valves for drive pulse generation and effort was directed towards reducing the number of valves in order to increase reliability and reduce size and power consumption. More recently, improved types of transistor have become available together with smaller cores and cores made from materials with

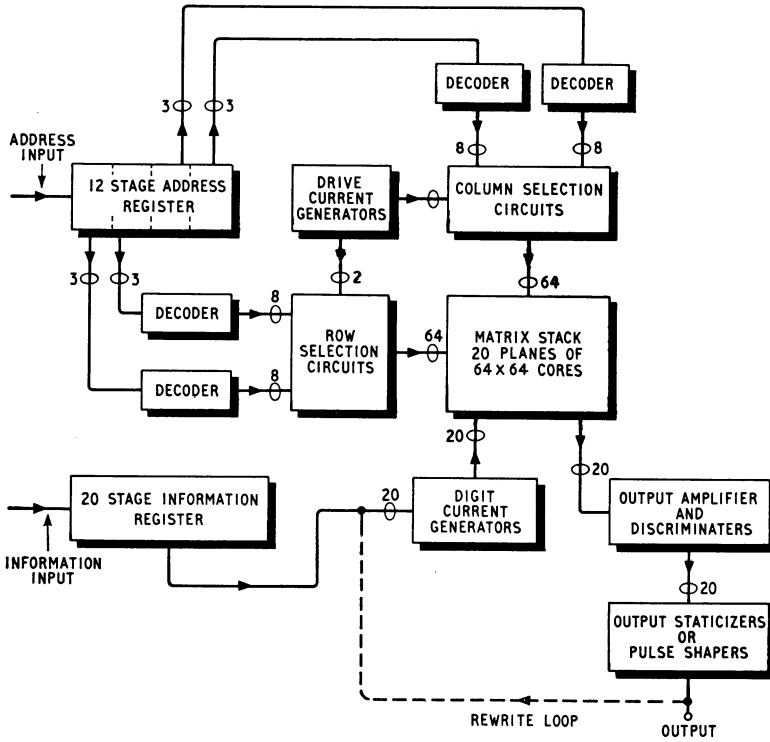

Fig. 8.1—Typical circuit arrangement for a coincident current store (control circuits not shown)

lower coercive forces. As a result it is now possible to construct complete stores without using any valves although a combination of valves and transistors is sometimes used for convenience.

Half drive pulses for coincidence systems range from about 200 mA to 600 mA depending upon the type of core. A rise time of less than about a quarter of the switching time of the core is required for this pulse, i.e. from about 0·1 to 0·5 μsec. During the application of the pulse the impedance of the stack varies considerably, Fig. 3.4, so that a current source is necessary. The magnitude of the back e.m.f. arising from the matrix stack depends upon the number of half selected cores, the pulse rise time, etc., and is of particular importance to transistor drive circuits where maximum permissible inverse voltages and power dissipation will set a limit

to the size of stack which can be driven. In this connection it must be remembered that, since most of the back e.m.f. arises from half selected cores and wire inductance, a voltage will arise at the rear edge of the drive pulse of opposite polarity to that generated on the leading edge. However, in order to avoid some of the problems which may arise from the changing load it is sometimes possible to insert terminating impedances which match the impedance of the drive wires. These wires are delay lines and have a characteristic impedance which usually lies between 100Ω and 250Ω depending upon the type of core and the wiring configuration. Provided that the wires are correctly matched the inverse e.m.f. will be of the same form as the current drive pulse so that the voltage drop across the line and terminating resistor will be constant during most of the pulse. This often enables drive circuits to be designed more easily and also allows a voltage drive to be employed if desired.

8.2. Direct gating systems

The simplest arrangement for row and column selection consists of a separate valve or transistor connected to each matrix drive wire, the other end of the wires being joined together. The valves or transistors may be current amplifiers but more often will be gates which, when open, allow the passage of a drive pulse derived from a common drive circuit. Similar sets of gates are required to select rows and columns and since read and write pulses of opposite polarities are necessary either a pair of gates or a bi-directional gate is attached to each drive wire. Some early stores used a pair of valves for this purpose but for a larger matrix such a system becomes bulky and relatively unreliable. These objections apply much less to transistor circuits and in this case there may be advantages in this type of system from the point of view of fault finding and the fact that efficient gates can reduce break-through on unselected wires to a very low level.

A few possible gating methods using transistors are shown in Fig. 8.2. The simple scheme using two PNP transistors for each wire, Fig. 8.2(a), would probably not be used in practice since it possesses several undesirable features. These are liable to arise in any transistor selection circuit and this circuit has been included to examine them in more detail. The circuit includes read and write current pulse generators which are common to all drive wires. On each drive wire an emitter follower is used to gate the

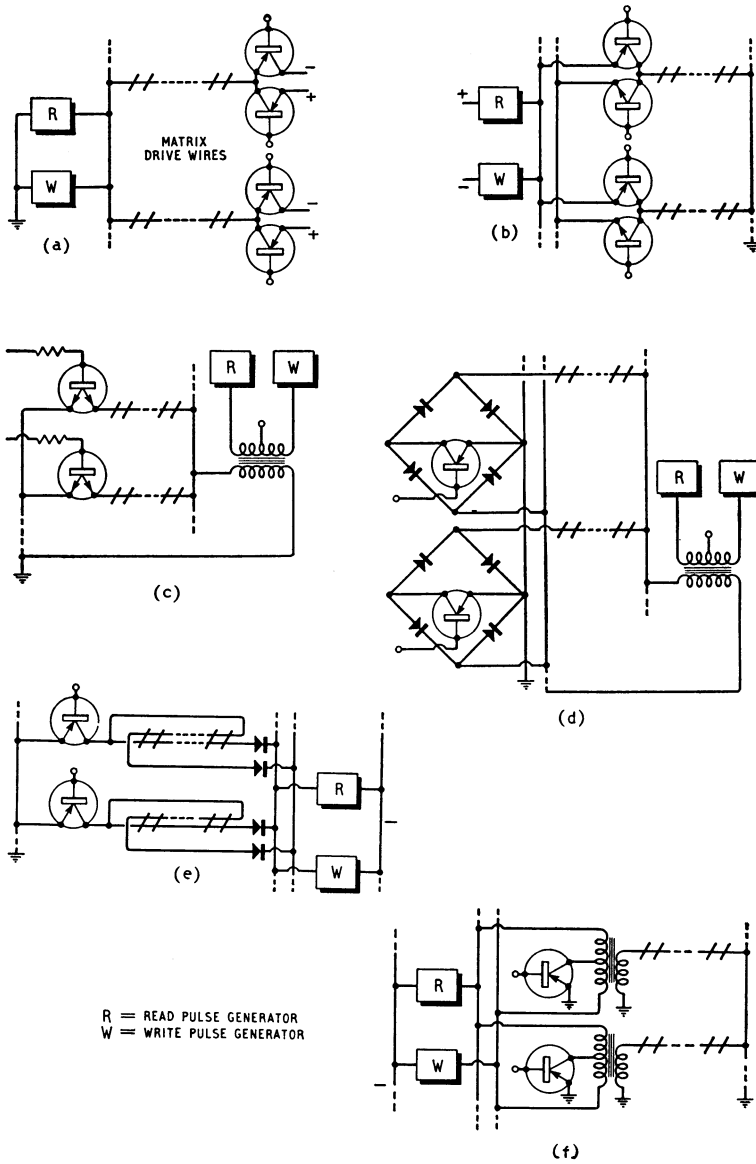

Fig. 8.2—Drive wire selection methods using direct gating

pulse in one direction and a grounded emitter circuit to gate the pulse in the opposite direction. The major disadvantages of this circuit are as follows:—

(a) The base voltage difference between a selected and an unselected emitter follower must be greater than the back e.m.f. developed across the drive wire. This may lead to difficulties in the decoding circuits both from the amplitude and speed aspect since it may be difficult to provide a fast, large voltage swing from the decoding circuits to drive the emitter followers.

(b) When any wire is driven, the potential of all unselected drive wires will change by an amount equivalent to the back e.m.f. across the selected wire. This means that current will be drawn from the drive pulse to charge the stray capacities associated with these wires and, in addition, a large voltage may be picked up in the output wire during reading and increase the difficulty of discriminating between "1" and "0"

(c) The pair of gates being used for a read/write cycle cannot be selected simultaneously otherwise a current path will exist through these transistors from the positive to the negative supply rail. Hence input levels must be changed between the two operations. This will lead to loss of speed and/or a more complicated addressing system.

These three problems can be overcome by using the circuit of Fig 8.2(b) which employs grounded base gates of NPN and PNP transistors. In this case only small differences in the base voltages of selected and unselected transistors are required, the unselected transistors isolate the unselected drive wires from the pulse generators and both gates may be selected together. A disadvantage in this case is that the transistors cannot be bottomed and considerable power dissipation must be allowed for in consequence.

A bidirectional gate may also be used and may take the form of a symmetrical transistor[1] as shown in Fig. 8.2(c). The problems (a) and (b) mentioned above apply to this circuit but in addition to the economy in transistors it has the advantage that since no d.c. source need be present the pulse current can be applied through a transformer as shown. This in turn means that the transistor may be bottomed during the whole of the drive pulse and a low power transistor may be used. All transistors except the one

attached to the selected drive wire are cut off by a negative voltage applied to the base. The base of the selected transistor is at a positive potential so that current flows from the base to the other electrodes. Upon the application of a positive drive pulse to the common termination of the drive wires the transistors become grounded emitter gates and current will flow only through the selected transistor. On the other hand a negative drive pulse from the transformer will cause more base current to flow towards this point and the base will become negative with respect to the earthed electrode which then becomes the collector. The gate is now behaving as an emitter follower and in this case the bases of the unselected transistors must be more negative than the back voltage expected from the drive wire if they are not to be brought into conduction.

As an alternative to a symmetrical transistor a bi-directional gate consisting of a transistor in a diode bridge, Fig. 8.2(d), can be used.[2]

Economy in transistors may also be achieved by threading two wires through each row and column. An example is shown in Fig. 8(e), though other types of gate may have advantages. The diodes are necessary to block alternative current paths.

Transformer coupling to the drive wires has been used[3,4] with either one or two gating transistors per wire. Current transformation is now possible and similar types of gate are used for read and write pulses so that design problems are simplified. In Fig. 8.2(f) one transistor at the centre tap of the transformer primary gates both read and write pulses. A transistor on each end of the winding may equally well be used and at the same time will serve to isolate the unselected transformer capacities from the drive pulse, though in this case the transistor must withstand twice the inverse collector voltage.

In all circuits described above the selection is assumed to be performed before the arrival of a drive pulse by means of a voltage change on the base of a transistor relative to a d.c. level. In most cases the base/emitter current may be established in the gates by a current drive through a transformer. This then allows the selected gates to be bottomed during the passage of the drive pulse so that lower power dissipation results but the system is dynamic and difficulty may arise in the derivation of the required currents from the decoders.

Gates working as grounded base or emitter follower circuits are unlikely to cause distortion of drive pulses through lack of frequency

response provided that suitable transistors are used. Grounded emitter gates will usually require the necessary base current to be established before the arrival of the drive pulse in order to pass the leading edge without too much distortion.

8.3. Selection circuits using a diode matrix

By introducing the drive pulses at an earlier stage in the decoding the number of valves or transistors used for gating purposes may be

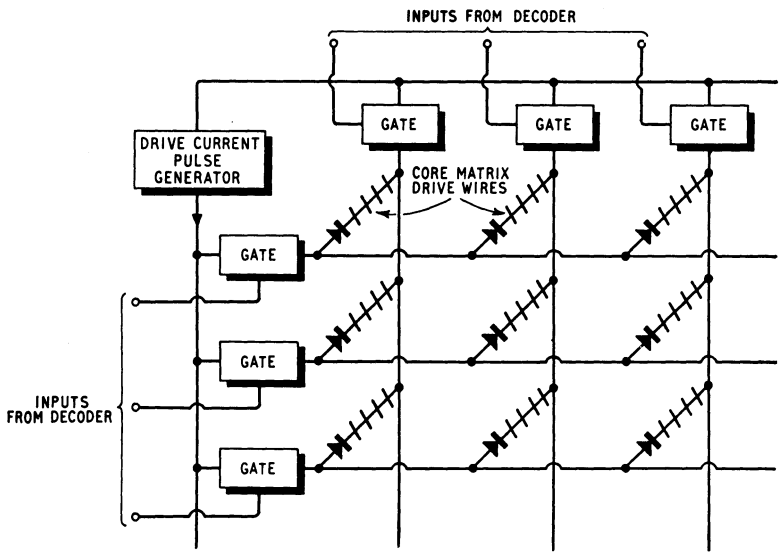

Fig. 8.3—Basic circuit of diode matrix selection scheme

reduced significantly. This reduction is greater than is apparent by just considering schematic circuits since each gate in the circuits described in this section and Section 8.2 may involve the use of two or three transistors or valves to provide an adequate drive to the element through which the drive pulse passes. One method of routing drive pulses is by means of a diode matrix. Other methods using square-loop magnetic materials are described in Section 8.4. The basic circuit of the diode matrix selection scheme is shown in Fig. 8.3. One of each set of gates is selected to allow the passage of a drive pulse. This circuit is straightforward but

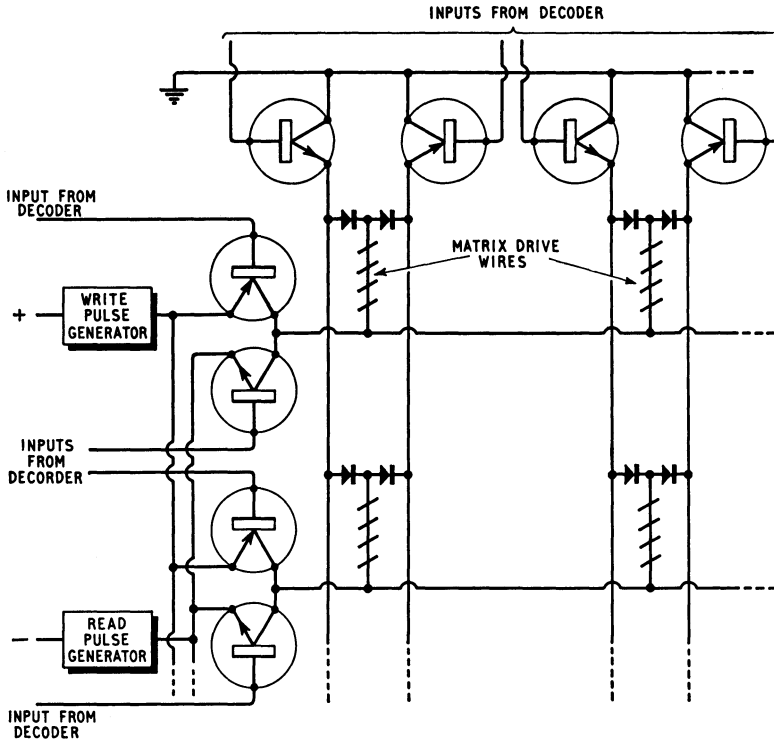

Fig. 8.4—Diode matrix selection circuit using transistor gates

provides drive currents in one direction only. Most of the design problems arise when the same principle is used to provide currents in both directions on a single drive wire. The diodes are necessary to prevent current from flowing through paths other than the selected drive wire but also serve to isolate the stray capacity of unselected lines from the drive pulse. Any of the circuits described in Section 8.2 for direct gating of the drive wires may equally well be used in combination with the diode matrix and the same considerations regarding their relative advantages apply here. One of several possible systems using transistors is shown in Fig. 8.4. The gates on the left side of the matrix are grounded base transistor circuits which require small changes in base voltage for selection but fairly high power dissipation since the peak voltage across the

stack must be taken up without bottoming. The upper gates are emitter followers which require a large base voltage swing for selection but comparatively low power dissipation since they may be almost bottomed when selected. In the latter case the high voltage swing may be overcome by replacing the emitter followers by grounded emitter transistors of the opposite type which are bottomed when in use. The gates for the read and write pulse cannot be selected simultaneously so that some selection voltage changes must take place between the two operations. The combination of gating circuits used here is not necessarily the best and the choice of the many possibilities will be dictated by particular requirements and the available transistors. As in the case of direct gating, economy in transistors can be achieved by threading two wires for each row and column.[2]

Transformers may also be used with the diode matrix scheme. These are often found with valve gates[5,6] when impedance matching may be more important than the slight reduction in gating elements which results. A typical valve driven circuit is shown in Fig. 8.5. The capacity isolating function of the diodes is of rather greater importance here than in transistor circuits since the valve current may be from five to ten times less than the current through the matrix wires.

Transistor circuits sometimes require transformers for impedance transformation especially when the matrix drive wires are terminated by matching resistors. Under these conditions the e.m.f.s generated across the drive wires are too high to be accommodated by the collector turnover voltage of many germanium power transistors but these transistors may easily be able to supply a higher current than is required for a half drive pulse in most coincidence drive stores.

A diode matrix selection scheme provides one answer to the problem of driving faster stores, as for example the stores described in Chapter 5, whether or not these stores use ferrites as the storage elements. However, transistors and diodes capable of handling the currents and voltages at the speeds required to take full advantage of these stores are not yet in quantity production.

8.4. Selection circuits using square-loop magnetic materials

Systems which make use of the properties of square-loop magnetic cores have often been used. These cores may be made of a ferrite similar to that used in the storage cores or of thin metal tape.

The basic principle employed is illustrated in Fig. 8.7(b) where a core in remanent state, *A*, on the saturation hysteresis loop is subjected to a driving field H_1. If H_1 is considerably larger than H_c the core will be completely switched by a positive pulse and will return to state *B* after removal of the pulse. A negative pulse will only drive the core further into saturation and return it to state *A* when removed. The ratio of the two flux changes depends upon the gradient of the *BH* loop from remanence towards saturation and it is important that this saturation permeability should be low. If a core of this type is used to make a current transformer to supply each matrix drive wire the non-linear property outlined above can be used for selection purposes by arranging the transformers in a suitable matrix. Various arrangements have been proposed

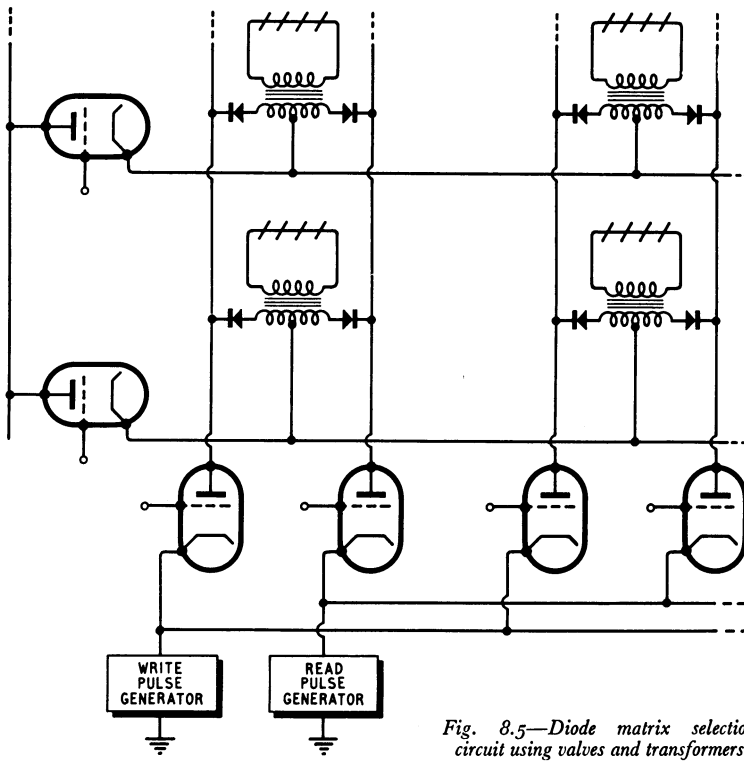

Fig. 8.5—Diode matrix selection circuit using valves and transformers

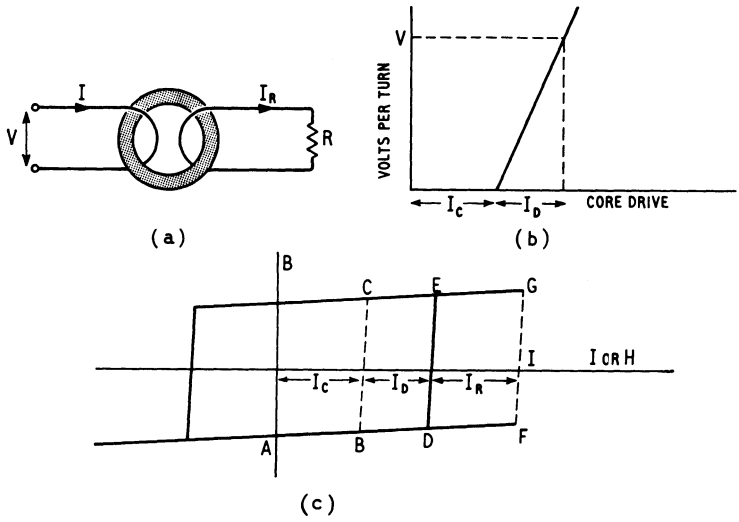

Fig. 8.6—Operation of a loaded core

for accomplishing this but before describing these the operation of a current driven loaded core will be briefly described.

In the circuit shown in Fig. 8.6(a) a square-loop core, loaded by the resistance R, is driven by a rectangular current pulse of amplitude I. It is assumed that the voltage pulse across the core is also rectangular and is related to the net driving current by the curve shown in Fig. 8.6(b). This is a sufficiently good approximation for a qualitative description of the operation. I_c is equivalent to the coercive force and ID is the excess magnetizing current necessary for the core to switch at the desired rate since V is proportional to dB/dt. This curve may be expressed by $V = I_D R_o$ where R_o is an impedance which depends upon the shape, size and material of the core. A somewhat idealized hysteresis loop is shown in Fig. 8.6(c). When I is applied the state of the core will follow the path $ADEG$ and a current I_R will be induced to flow in the resistor. From Fig. 8.6(c) it is evident that

$$I = I_c + I_D + I_R$$

or

$$I = I_c + \frac{V}{R_o} + \frac{V}{R}$$

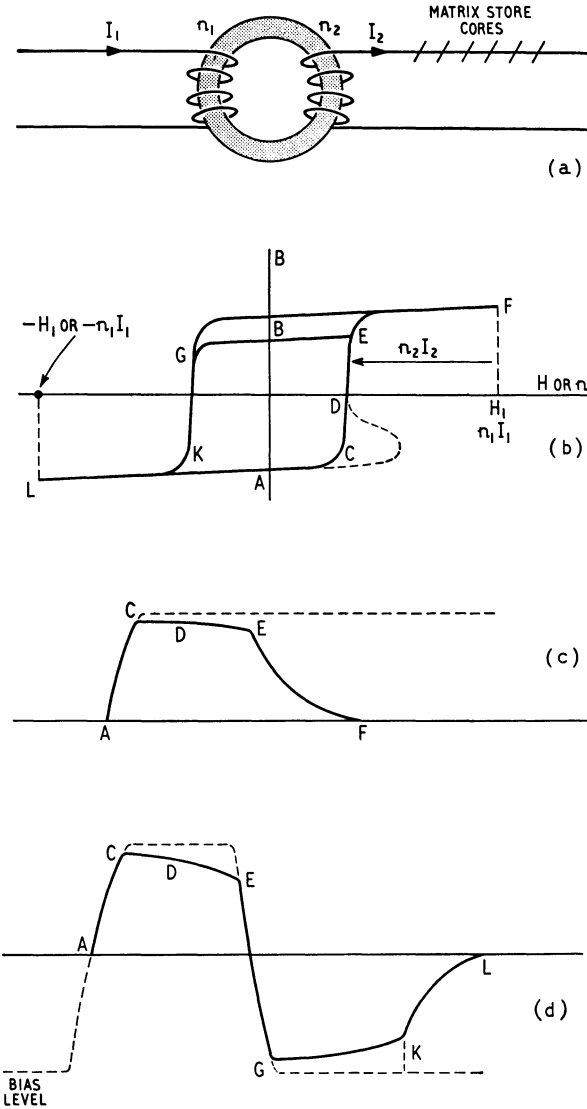

Fig. 8.7—Hysteresis loop and output waveforms of a switch core driving a matrix store

Thus if R is small compared with R_o, i.e. the load resistance is small compared with the core impedance

$$I_R = I - I_c$$

and the path followed will approach *ABCG*. In this case the voltage across the core, V, and hence the speed of switching will be almost entirely controlled by R and I. On the other hand if R is large compared with R_o the path followed will approach *AFG* in which case the speed is controlled by I and the core characteristics as in the case of an unloaded core. Intermediate paths such as *ADEG* will be taken when R and R_o are comparable in value. A primary and secondary winding of only one turn has been considered but the argument may easily be extended to include multiple turn windings.

Similar results are obtained if the core is voltage driven except that in this case I_R is given by V/R where V is the applied voltage and is independent of the core characteristics. During switching I is still given by the sum of I_c, I_D and I_R but will rise rapidly as soon as switching is completed unless the voltage is removed.

In practice the switch core is loaded by a matrix drive wire, Fig. 8.7(a). It can be seen from Fig. 3.5 that the voltage waveform across a matrix stack consists of a short high amplitude portion followed by a longer period of low amplitude which continues until the end of the drive pulse. The former arises mainly from disturbed cores and wire inductance and the latter from switch cores and wire resistance. The switch core and its windings are usually chosen so that its impedance, R_o, is high compared with the drive wire impedance for the following reasons:—

(a) The ratio of the power transferred by the core to the load, to the power absorbed by the switch core is then high.

(b) I_2 then depends less upon the switch core characteristics which might vary from core to core.

(c) In most selection systems, see below, current I passes through unselected switch cores and if I is kept to a minimum the bias required on these cores is also a minimum.

The state of the switch core is assumed to follow the path *ACDEF* in Fig. 8.7(b) when a current pulse, I_1, is applied to the primary which has n_1 turns. The secondary ampere turns are then a function of time and at any given time are equal to the difference

between n_1I_1 and the ampere turns corresponding to the point on the curve which has been reached. As stated above the conditions are such that the speed of switching is controlled mainly by the load and during the first part of the pulse when the output voltage is high the path AD is traversed fairly rapidly when compared with the path DE which is followed when the output voltage is low. The slope of the top of the output current pulse Fig. 8.7(c) depends upon the slope of the hysteresis loop between C and E so that the percentage droop over this region depends upon this slope and the value of n_1I_1. This means that the minimum value of n_1I_1 is determined by the droop required, the difference in coercive force likely to be encountered between switch cores, and the effect of temperature on the coercive force. From E to F the output current falls off slowly since as I_2 falls the rate of flux dissipation also falls and apart from the flux in the switch core there is also a certain amount of flux stored in the load to be dissipated. This fall can be speeded up by inserting extra resistance in the secondary though more flux, i.e. a core with a larger cross-section or with a larger number of secondary turns, is then required in order to maintain the output current for sufficient time. In either case extra power is necessary to provide for the power lost in the resistor. The pulse can be terminated more rapidly by removing the drive pulse but, in some systems, where a standing bias is used this is not possible and the slow trailing edge is still present after the writing operation, Fig. 8.7(d). There is however usually more time available for this to occur after writing so that the slow fall is then less troublesome than if it occurred after reading.

It has been assumed that the drive pulse rise time has been slow enough for flux change in the switch core to follow. If a fast rise time is used the path followed will be one such as the dotted line AD shown in Fig. 8.7(b) and the secondary current rise time will be slower than that of the primary. This situation is unlikely to occur owing to the large power requirements of the drive pulse and in any case it does not affect the operation significantly.

Thin metal tape has some advantages over a square-loop ferrite as the material used for a switch core and has been preferred in many cases. Its lower saturation permeability means that less signal is produced by half selected cores and the lower coercive force leads to less power loss in the core. In addition its higher saturation flux means that fewer turns are required for the same

area of cross-section. Against these, metal tape cores are less uniform, more easily damaged, and cost considerably more than the corresponding ferrite cores.

8.4.1. COINCIDENCE MATRIX SWITCHES

Selection circuits using square-loop cores most commonly take the form of a coincident current matrix switch.[7,8,9] Various methods, some of which are shown in Fig. 8.8, can be used for driving a switch of this type. The first circuit shown uses coincident

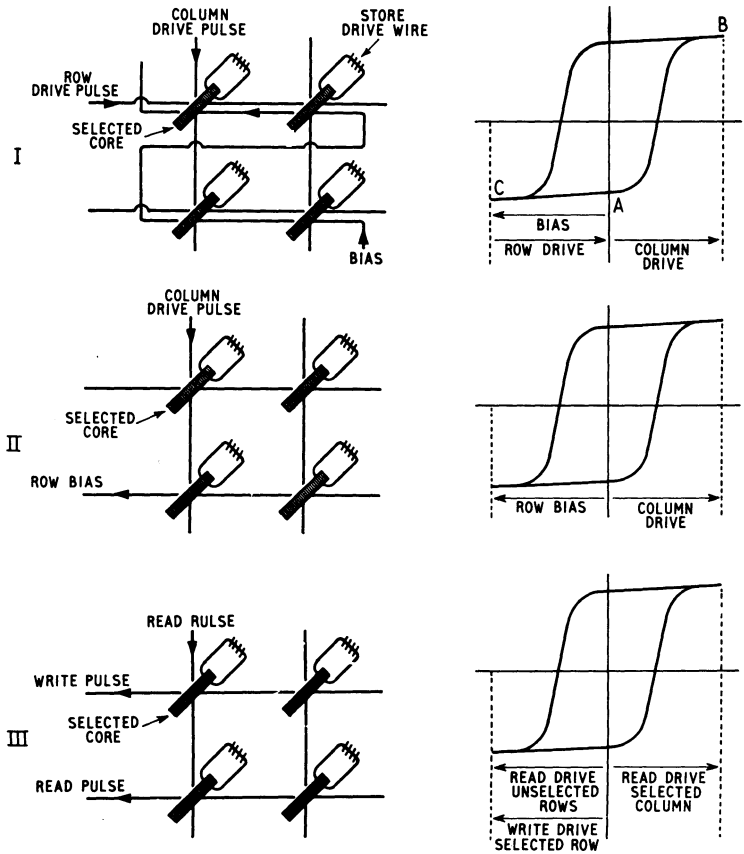

Fig. 8.8—Coincident drive matrix switch circuits

half drives in the same manner as a coincidence store except that all cores are normally biased well into saturation. The presence of one drive is sufficient to change the state of the core from *C* to *A* and the core at the intersection of the selected row and column receives a drive which takes it to *B* and causes an output to be produced in the selected drive wire of the store. Upon removal of the drive pulses the core returns to C under the influence of the bias current and in doing so provides a second output of opposite polarity to the first. The first pulse is normally used for reading and the second for writing. As mentioned above a small resistor is often inserted in the store winding in order to speed up the fall of current in this winding.

A slight variation on this is shown in circuit II. Here a separate bias current is provided for each row from a current source which can be controlled. The bias is then removed from the selected row and a drive pulse is applied coincidently on the selected column. The operation is thus very similar to that in circuit I but the switch cores only possess three windings. A disadvantage is that the current generators attached to the rows must pass a higher average current.

Circuit III uses anticoincidence rather than coincidence. During reading all rows other than the selected one are driven towards saturation so that only the core on the selected row provides an output when the drive pulse is applied to the selected column. Writing is performed by subjecting the selected row to a negative pulse which will switch the core back to its original state.

A time delay between reading and writing can be achieved in all three circuits if desired. In the first one this is accomplished by continuing the row pulse until the write operation is required and in the second by not reapplying the row bias until this time.

More important differences between the three circuits emerge if one output is required to be more than two or three times larger than the other in amplitude. For instance in a direct selection store it is often an advantage for the read pulse to be much larger than the write pulse since the latter may be used coincidently with a digit pulse and is therefore limited in amplitude. In circuit I use may be made of the square-loop as shown in Fig. 8.9(a). The read drive, H_R, can be made larger than the write drive H_W without disturbing half selected cores unduly but the ratio is limited by the actual value of H_W since as H_W is reduced the output current corresponding to this drive becomes more dependent

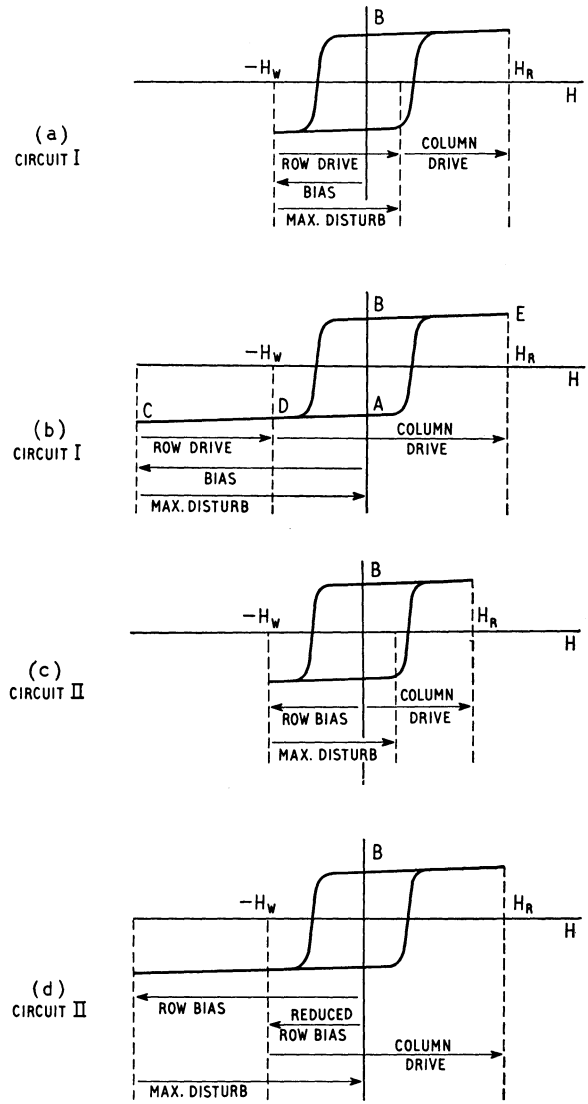

Fig. 8.9—Methods for supplying unequal read and write drives from a coincidence switch

upon H_C and is therefore less accurate owing to differences in core characteristics.

Another approach for the same circuit is shown in Fig. 8.9(b). The row drive moves the core from C to D and the column drive from D to E on the selected core or from C to A on unselected cores. When the column drive is removed the selected core returns to D and provides a write output. The row drive is not removed until switching is complete and then only a small output will arise from the change DC. In this case the row and column drive may be unequal and AD is adjusted for the correct write output. The only limitation is that the column drive must not be larger than the bias to prevent switching of unselected cores.

In circuit II similar methods may be employed though in the first case, Fig. 8.9(c), a slightly lower ratio of read to write current is obtainable for a given value of H_W and in the second case, Fig. 8.9(d), the row bias is reduced to a lower level rather than removing it completely.

In circuit III any ratio of read to write may be obtained since the amplitude of the row pulses applied during reading need bear no relation to the write pulse amplitude.

Voltage drive has been used for the column pulses in circuits I and II.[10,11] In order to do this a resistor must be connected in series with the matrix store drive wires. Since this resistor is used to define the output current the voltage across it during the drive pulse should be considerably larger than that obtained from the drive wire of the store. Extra power is then required, but since a constant voltage is applied to the switch, the drive pulse generator can be bottomed and may not need to dissipate more power than the corresponding current driver.

A three dimensional switch matrix using the principle shown in Fig. 8.9(a) has also been described.[11] In this case coincident pulses on three lines are used to overcome the bias on the selected core.

The large drive power requirements of the switches described above are not easily obtained from currently available transistors. To overcome this difficulty another type of switch, known as a load sharing switch[12] has been proposed. The principle of operation is illustrated in Fig. 8.10 by a switch which delivers four outputs. The polarities of the windings on the cores, which are not necessarily made of square-loop material, are indicated by the position of the dots. The switch drivers are arranged in pairs and one of each pair provides a drive pulse for the selection of any

core. It can be seen, for example, that core 2 will receive a pulse drive four times as large as that derived from a single driver if drivers 1*a*, 2*b*, 3*a*, 4*b* are used. A similar pulse in the opposite direction is received if 1*b*, 2*a*, 3*b*, 4*a* are used so that a read and write pulse may be delivered to the selected store drive wire. No

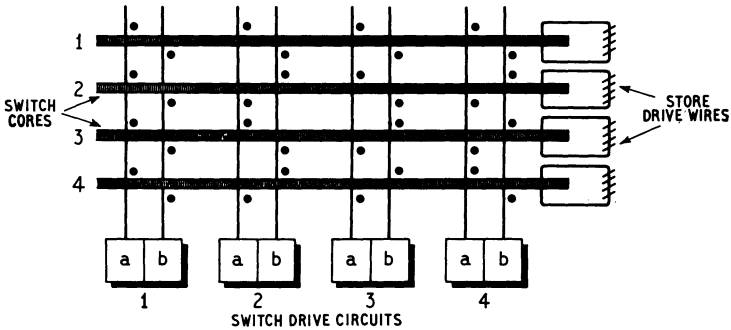

Fig. 8.10—Load sharing matrix switch

other core will receive any net drive provided that the current pulses from all drivers are identical in amplitude and length. Other combinations of selected drivers switch other cores. Since the number of outputs is equal to the number of driver pairs there is no economy in numbers of transistors over the straightforward system described in Section 8.2 where two transistors are attached directly to each matrix drive wire. In this case, however, each transistor can be a lower power device. Thus the advantage which the load sharing matrix offers depends upon the relative cost, size, and availability of the transistors which are necessary in the two cases. Slightly modified forms of load sharing switch can be constructed which use fewer drivers though at the expense of a small drive to some unselected cores so that small spurious outputs result. The possibility of single turn windings for the inputs means that the construction of a load sharing matrix should be relatively simple.

8.4.2 DECODING SWITCHES

Although a certain amount of decoding occurs in the matrix switches described above this process can be taken much further by using cores with many windings and in the limit the decoders

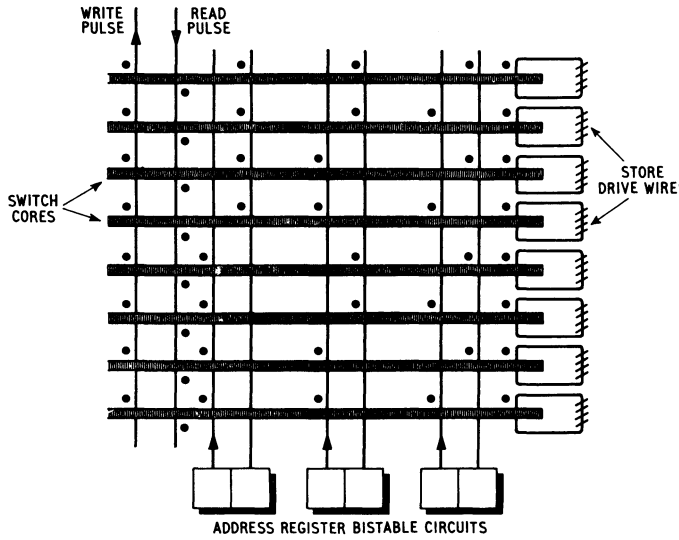

Fig. 8.11—Switch matrix decoder

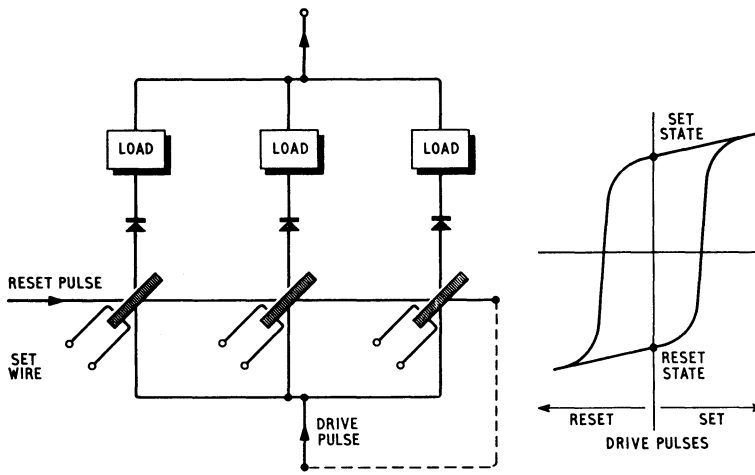

Fig. 8.12—Principle of current routing system using square loop cores and diodes

shown in Fig. 8.1 can be eliminated by transferring their function to the switch matrix.

Circuits of this type have been suggested[13] but as far as is known have not been incorporated in a large store.

Many arrangements of windings are possible but as an example the circuit shown in Fig. 8.11 will be taken. Currents obtained from the address register are used to bias the switch cores represented by the horizontal thick lines, and it is assumed that current is only derived from one side of each binary circuit. For example when the binary is storing a " 1 " a current is fed to the right hand line and when storing a " 0 " to the left hand line. The bias lines are only coupled with a core where a dot is shown. It is obvious that for any pattern of information in the address register only one core is left unbiased assuming that all bias currents are equal. If now a read drive pulse is applied to all cores with an amplitude less than that of a bias current then only the unbiased core will switch and provide a read output for the store. A write pulse following this will return the selected core to its original state and produce a write output.

The disadvantage of this type of circuit is the large number of multi-turn windings required on each core if 32 or 64 outputs are needed for the store. These are not only difficult to wind and terminate but each winding loads the switch core when switching takes place so that the large number of windings involved will distort the output.

8.4.3. CURRENT ROUTING SWITCHES

In the switches described above the outputs, which are fed to the matrix store drive wires, are all derived from a switch core by transformer action. This means that the output waveform is dependent upon the characteristics of the core. A better principle from this point of view would be to use gates which when opened allow the passage of a well defined drive pulse to a selected row or column. Unfortunately the ratio of unsaturated to saturated impedance is not nearly high enough for the core to make an effective gate for this purpose but when combined with a diode a satisfactory gate can be achieved. The core is now used merely as a voltage source to cut off or turn on the diode through which the drive current may pass. This type of circuit is commonly known as a current routing or current steering circuit.[14,15]

The basic principle employed is illustrated in Fig. 8.12. Before

the drive pulse is applied the core associated with the selected load is set by switching it to the upper remanent state. This setting operation will not cause any current to flow since all possible current paths are either open circuit or blocked by diodes. The drive and reset pulse are then applied coincidently. During this operation the core resets and in so doing provides on the output wire a voltage with a polarity such that the diode on its own wire is turned on and those on the other wires are biased in the reverse direction. The drive pulse will thus pass through the forward biased diode to the selected load. A back voltage is generated across the load in opposition to that from the core so that the core output voltage must exceed that across the load and diode. In addition the drive current opposes the action of the reset current in the core and excess reset current must be supplied to allow for this reduction.

The same current pulse may be used for resetting and driving as indicated by the dotted line in Fig. 8.12. By a suitable choice of core and the number of turns on each winding any load may be accommodated. The main requirements are that the flux linkage on the output wire is sufficient to furnish the voltage/time integral demanded by the load and that the drive, equal to the difference between the reset and drive ampere turns, switches the core at about the correct rate.

The circuit so far described is not particularly economical since one switch core and one diode are needed on each store drive wire. By using cores in series the number of cores may be drastically reduced and at the same time extra decoding may be achieved. An example is shown in Fig. 8.13. One of the pair of set wires from each binary on the address register is energized depending upon the information stored. This means that only one of each pair is set. The setting current may remain throughout the operation provided that the reset current is adjusted to take it into account.

Each output wire passes through one core of each pair so that 4 outputs are possible in the case shown and 2^n can be obtained from n pairs of cores.

When the combined reset and drive pulse arrives a voltage nE will be developed in only one wire if E is the voltage from one core. The maximum in any other wire is $(n - 1)E$ so that a voltage equal to the difference E can arise across the stack before other diodes begin to conduct.

The limitations of this method are likely to be due firstly to the ratio of back to forward impedance of the diodes, secondly to lack

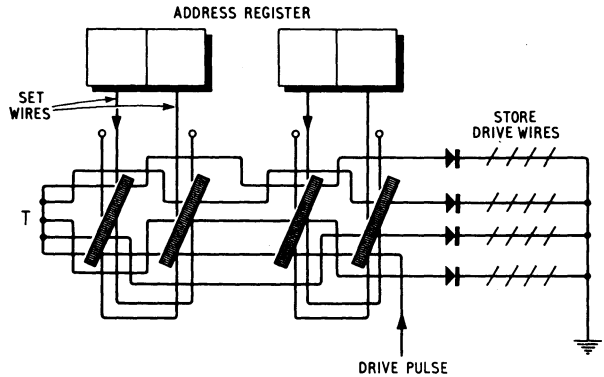

Fig. 8.13—Current routing circuit using cores in series

of uniformity of the output voltage E from each core, and thirdly to the wiring complexity.

The wiring problem is not too formidable if the output wires consist of a single turn. A rather large cross-sectional area of material may then be required and to keep the drive small a tube or several small cores wired together may be preferable to a large core of conventional shape. The higher flux density of metal tape cores may also be advantageous.

The number of wires through each core can be reduced if junctions are allowed since a group of wires following the same path after leaving the common termination, T in Fig. 8.13, may be replaced by a single wire up to the point where their paths diverge. By choosing correctly the groups of wires to be combined and by making use of the fact that the cores on a wire may be threaded in any order, it can be arranged that the number of wires through each core is approximately the same.

A considerably relaxed specification may be placed on the cores in these circuits, when compared with a normal matrix switch, since disturb outputs cannot pass through the biased diodes to the store.

8.5. Drive current pulse generators

In most of the selection systems described above, high impedance current generators are required for supplying the read and write pulses for the store. Similar circuits are also needed to provide suitable digit pulses, and the large number involved for this

purpose means that economy of components is of some importance. It is desirable that transistors should be used and a possible circuit[2] for the final stage of a current pulse generator is shown in Fig. 8.14. In view of the variable impedance of the load presented by a matrix drive wire, and the high accuracy necessary for the amplitude of a drive pulse in a coincident current store, an emitter

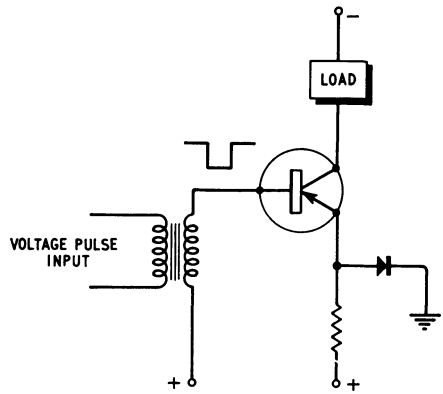

Fig. 8.14—Transistor drive pulse generator for a matrix store

stabilized circuit is preferable to a bottomed transistor as the method of defining current. In the circuit shown, current normally flows through the emitter resistance and the diode to earth and the transistor is cut off. An input voltage pulse is used to take the base a few volts negative with respect to earth. While current continues to flow through the diode it acts as a clamp on the emitter so that a voltage can be maintained across the base emitter junction until all the current is passing through the transistor. This means that a fast rise time can be achieved for the collector current. By making the emitter supply voltage high, the accuracy of the current pulse obtained can be made less dependent upon the input voltage. The transistor power requirements depend to some extent on the type of selection circuit used. In some of the circuits described in Sections 8.2 and 8.3 the gating transistors may be bottomed in which case the drive transistor must accommodate the peak matrix stack voltage without bottoming and a considerable power dissipation must be allowed. In other cases the gates take

up this voltage and the drive transistor may be almost bottomed during the drive pulse so that a lower power device may be used. If drive wires are terminated by a matching resistor some of the difficulties of providing a satisfactory current pulse for both the drive and digit circuits in a large store may be overcome. Matching of these wires prevents large e.m.f. variations across the load which tend to distort the current pulse by causing current flow to collector and other stray capacities. Power dissipation can also be kept to a minimum in drive transistors if the load e.m.f. rises to a constant value during the pulse.

8.6. Output amplifiers

In a parallel access matrix store the number of output amplifiers is determined by the word length since one amplifier is needed for each digit position. These circuits are used to amplify the output signal, distinguish between a " 1 " and a " 0 " output, and, depending upon the logical system used, either feed the result to a temporary store such as a bi-stable circuit or transform it into a suitable pulse for use in the computer. These operations are well within the capabilities of modern high frequency low power transistors. The most difficult problems are likely to be encountered in a coincident current store and amplifiers for this type of store will be described.

A schematic diagram of the basic elements in a typical amplifier is shown in Fig. 8.15(a) although these elements need not necessarily occur in the order shown. The output winding of a matrix plane behaves as a transmission line with a characteristic impedance of about 150 Ω to 250 Ω and should be matched at the output terminals. Advantage may be taken of this low impedance to insert a transformer at the amplifier input to provide voltage gain if the transformer is followed by a stage with a high input impedance such as an emitter follower as shown.

Further gain may be achieved by means of the second transistor, before the signal is rectified. Rectification, which is necessary because the signals from the plane may be of either polarity, may be performed by means of a diode bridge or similar circuit. A strobe pulse may then be introduced through an '*AND*' gate, which here uses diodes, and the output of this gate is sampled by the final transistor biased to an optimum level for discriminating between " 1 "s and " 0 "s. The output from this stage may then be used to trigger a storage circuit or pulse shaper.

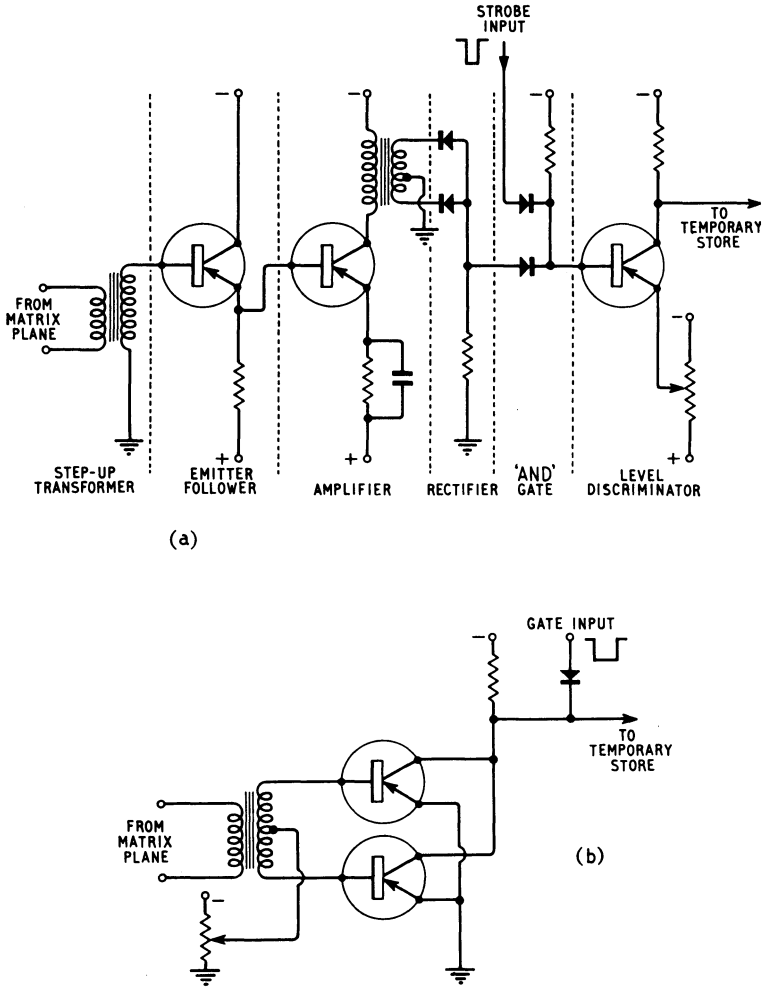

Fig. 8.15—Schematic diagrams of output amplifiers

Since the determination of the digit being read from the store depends upon the amplitude, at strobing time, of the output signal with reference to a fixed d.c. level, a problem arises in a.c. coupled amplifiers, especially when the read/write repetition rate is high. Under these conditions insufficient time may elapse for the inductive or capacitive coupling elements to recover to their quiescent state between successive inputs. As a result the level from which the latter commences will vary with the pattern of pulses preceding it from the store. For example, in a coincident drive store of the type described in Chapter 3, if the operation is such that a sequence of " 1 " outputs occur with the same polarity and if " 0 "s are being written between these outputs, then the level at the strobing position in the amplifier corresponding to no input will drift and reduce the tolerance available for the level used to discriminate between a " 0 " and a " 1 ". Input signals derived from the digit pulse during write time may produce a similar effect if these signals, which are usually much larger than a " 1 " output, cause the amplifier to leave its region of linear amplification. Thus, although at the amplifier input the voltage/time integral of this signal is zero, this is no longer true after non-linear amplification has taken place and a shift of the reference level will again follow. In extreme cases the amplifier might be completely blocked by these signals so that a considerable time is necessary for recovery before the next read output can be accepted.

These problems do not arise in direct-coupled amplifiers but, although these are sometimes used, it is often impossible to achieve the required gain with adequate stability with regard to drifts arising from component and temperature changes. In an a.c. coupled amplifier the effect can be minimized in a number of ways. It is impossible to continue to read " 1 "s and write " 0 "s indefinitely so that the maximum shift of level due to this cause takes place in a limited period. Thus if the initial stages of the amplifier are designed so that the time constants associated with the coupling or decoupling components are considerably longer than this period then drift will not be significant. In addition, if the inputs due to the digit pulse are not too large the initial stages may be a.c. connected and a transfer made to direct coupling when they have attained an amplitude sufficient for non-linear amplification to result. Alternatively, a switch may be introduced to suppress these large signals so that a.c. amplification may be extended to further stages.

A small condenser followed by a low impedance clamp such as the collector of a bottomed transistor is sometimes inserted immediately before the strobing circuit. Impedances are arranged so that the voltage across this condenser follows the signal arriving while the clamp is in action. The clamp is released for reading just before the arrival of the core output to be sampled so that the condenser charging time then rises to a much higher value and its output follows the input but starts from a known level defined by the clamp. Drift of the reference level is thus eliminated.

A much less elaborate circuit, such as that shown in Fig. 8.15(b), may be used with a small matrix plane. Impedance matching on the output wire is less important and a larger step up ratio may be used in the transformer. Since strobing may be unnecessary this ratio may be increased at the expense of bandwidth. In the circuit shown, rectification, amplification, gating and amplitude discrimination are all performed with only two transistors.

The remainder of the circuits associated with the store, such as the timing circuits address registers, diode decoders, etc., may be of conventional types as used in numerous other applications and will not be discussed here.

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Chapter 9

SPECIAL PURPOSE STORES

The preceding chapters have been primarily concerned with the use of square-loop ferrites as a storage element in fast parallel access stores with the properties required for a general purpose digital computer. Although in the past these stores have absorbed most of the cores produced, there exists in the digital data handling field a large variety of storage problems which may also conveniently be solved by the use of ferrites. In some cases the nature of the requirement allows the use of techniques which are not applicable to the normal computer store. A few examples of special purpose stores have been chosen to illustrate the possibilities.

9.1. Permanent stores

In digital computers and elsewhere there is often a need for a random access store to contain permanently stored information such as fixed programmes, function tables or numerical constants. The short access time which is often required makes ferrites an attractive proposition for this type of store.

A simple permanent storage method can be achieved by constructing a store in the same manner as a normal coincidence or direct selection store but only inserting a core where a " 1 " is required. Reading may then be accomplished by applying drive pulses to the selected word and then resetting the cores to their original state by a pulse in the opposite direction. Outputs will only arise from those positions in which a core is situated.

An improvement over this may be obtained by means of a standing bias on all storage cores. The bias will reset the cores without the necessity for a second drive pulse, and in the coincidence case the drive pulse amplitude may be increased to provide faster access.

These arrangements would be simple to wire but there is considerable redundancy since one core could be used to store several

bits. If a direct selection system is used two possibilities arise for reducing the number of storage cores. In theory, a single core is sufficient for each word of storage as shown in Fig. 9.1(a) for a store containing four words of four digits. The output wires pass through the core only when a " 1 " is required. Alternatively[1] a single set of cores may be used for several words, Fig. 9.1(b), in which case the drive wires thread cores in the digit positions corresponding to a stored " 1 ". In each case biased cores may be used.

Apart from the wiring complexity the main problem arises from the possibility of induced currents by transformer action in the selected cores. This is particularly important, if a switch matrix is used for word selection, since the impedance of a saturated drive core is low. These induced currents tend to drive the other cores

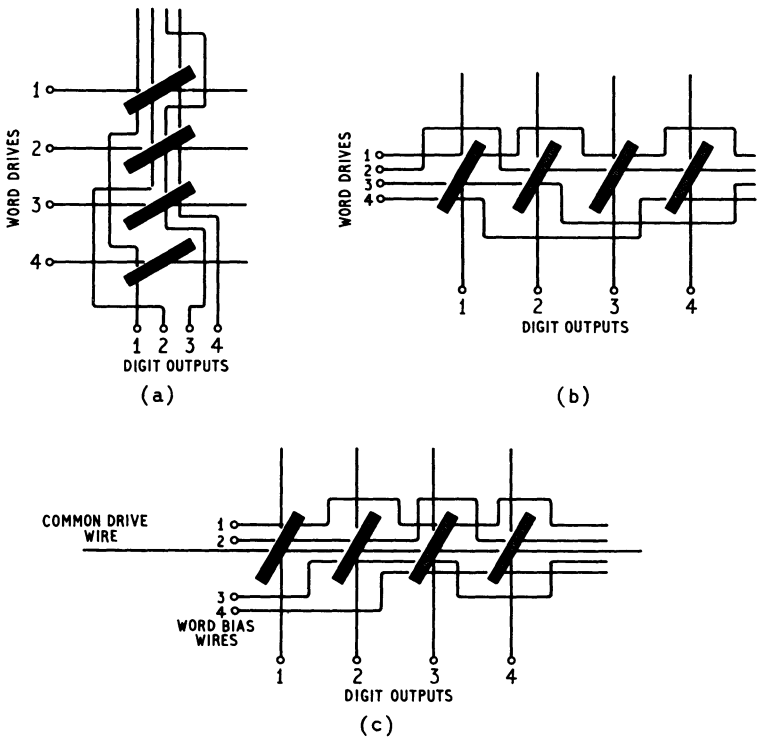

Fig. 9.1—Permanent storage wiring methods

to which they are coupled towards saturation. The outputs thus produced in unselected cores are of the opposite polarity to those from selected cores so that discrimination is not impaired. However in unfavourable wiring configurations the total drive current received by a selected core might be very much reduced or even reversed. By including a series resistor in each drive wire it has been shown[1] that the problem may be largely overcome although extra power will be necessary in the drive pulse.

A slightly different wiring method[2] has also been described, Fig. 9.1(c), in which a common drive wire is used for a set of cores storing several words, and word selection within the set is performed by applying bias current to a winding which threads cores in which a " 0 " is needed. It might be feasible to extend this idea so that each bias wire threads several sets of cores serially, each set being driven by one switch core. By this means the total number of bias wires may be kept small and by driving them from a high impedance source the induced current problem mentioned above would be less severe.

9.2. Semi-permanent stores

It would be impracticable to change the stored information in the systems described in Section 9.1 since re-routing of most of the windings would be involved. Several applications arise when the contents may need to be changed occasionally. From the point of view of economy and speed it is desirable that this should be possible without the necessity for building a new store. In addition, if a large number of permanent stores are being manufactured it is sometimes preferable for a system to be avoided in which wiring mistakes are not easily rectified. For these reasons several semi-permanent storage systems have been devised, into which any pattern of " 1 "s and " 0 "s can readily be inserted after the core wiring is complete.

In this type of store cores must be present in all digit positions since they may be needed at some time for the storage of a " 1 ". Economies cannot be realized by using one core to represent several digits. As far as drive and output windings are concerned the store will in fact be identical with the equivalent size temporary store. The problem is now to render inoperative cores in which a stored " 0 " is required.

If the patterns to be stored are random each core must be accessible separately. Electrical methods of pattern insertion thus

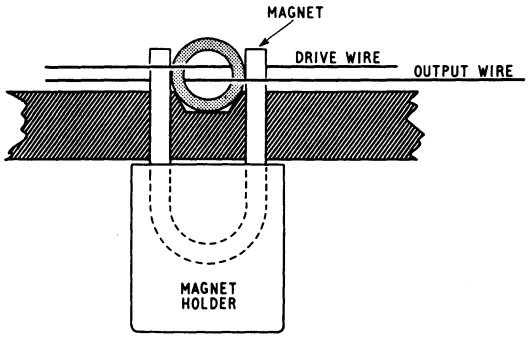

Fig. 9.2—Prevention of switching by means of a permanent magnet

need an additional winding on each core to which a connection can be made. This may be achieved, for example, by mounting the cores on a plate of insulating material. A single turn winding through each core may then be taken to terminating pins pushed through the plate and the pattern wiring carried out on the face of the plate remote from the cores.

One method for preventing cores from switching when subjected to a drive pulse is by means of a short circuited turn. The currents induced in this winding will reduce the flux swing to a low value during the pulse. In practice some switching will occur owing to the difficulty of providing a winding of sufficiently low impedance with a wire thickness which will pass through the core.

A second method relies upon a standing bias with an amplitude larger than that of the drive pulse so that the " o " cores remain in a saturated condition. This method produces a smaller " o " output than the first and has the additional advantage that long wires may be inserted between the cores and the connection board.

A core can also be prevented from switching by means of a magnetic field and a method based on this principle does not require a separate winding for each core. A practical arrangement employs a small length of permanently magnetized wire in the shape of a horseshoe, Fig. 9.2. The core lies between the poles of this magnet in a field of adequate intensity to over-ride the driving field. Accurate location of the core and magnet is achieved by using the plate on which the cores are mounted as a support for the magnets, as shown. The required information pattern can thus easily be inserted, corrected or changed by the insertion or removal of the appropriate magnets.

9.3. Cyclic stores

Digital systems often need a store in which the storage locations are used in rotation. Applications for these are most commonly encountered where data is being transferred between two devices which operate at different speeds. For example, a large number of measurements may require a temporary store before being used for computation, or before being stored in a more permanent form. Stores used for this type of operation are commonly called buffer stores. A ferrite store is especially suitable for this purpose since the insertion and extraction of information may be quite random in time apart from being subject to a limiting frequency and the fact that reading and writing may not coincide. The latter may be overcome by using a register to hold incoming digits while a read operation is being completed although, in the case of a small direct selection system, it is possible for both operations to take place simultaneously in different addresses if the read drive pulse is much larger than the write drive pulse.

The cores in a cyclically addressed store will normally be wired in the same manner as in a random access store. The main

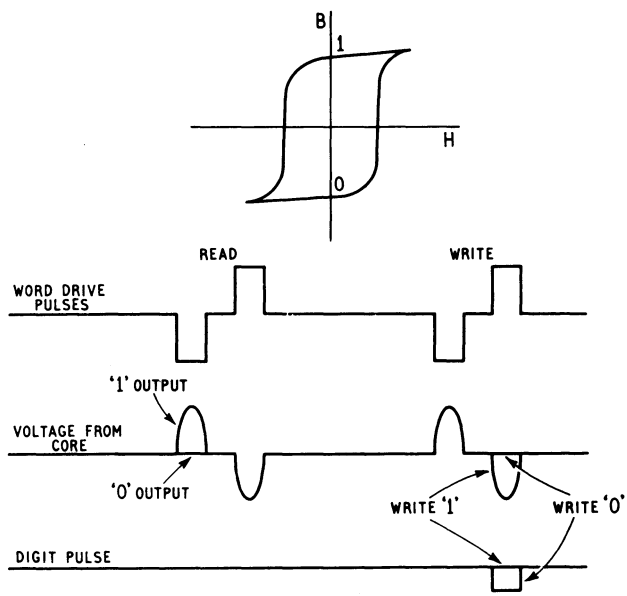

Fig. 9.3—Driving method using identical read and write drive pulses

differences, if any, will lie in the drive and selection circuits. Since reading and writing no longer take place consecutively in a selected address it may be more convenient to use completely separate read and write circuits. If transformer coupling is used on the drive wire of the matrix it may then be necessary to insert a series diode to provide d.c. restoration at high repetition rates.[3]

One method[4] which uses a common read and write drive circuit generates two pulses in succession of opposite polarity for both the reading and writing process, Fig. 9.3. For reading only the first pulse is used and for writing only the last. Thus economy of driving circuits can be achieved, though at the expense of time. This method is more applicable to a store driven by a ferrite switch matrix when the production of the two pulses is inevitable.

Since the storage locations are usually selected sequentially in a buffer store a ring counter, such as a multi-cathode valve, is an alternative to an address register and decoder but more important than these differences is the possibility of reduced power dissipation in some of the selection circuit elements. This is particularly true of transistor driven stores where a low power transistor capable of supplying an adequate drive current is often excluded from a random access store, where this current may be demanded from it repeatedly, owing to its power limitations.

9.4. Stores for delaying information

In digital data handling systems the necessity sometimes arises for delaying information for periods which are long compared with the time between digits or between words if a parallel transfer is in use. Various devices may be used for this purpose but in some cases a magnetic matrix store has some advantages. It provides a reasonably economical method where very long delays are required either for serial or parallel information provided that the transfer rate is less than 100 kc/s. It also has the advantage that the delay is precisely tied to the clock period.

The magnetic matrix delay can be considerably simpler than a matrix store as used in a computer. A read/write cycle is used in each address and the addresses are selected in succession. Further economy can be achieved by using a storage plane in which the number of rows and the number of columns have no common factor and then using ring counters as address selectors. Each time the address is changed the ring counters controlling the row and column selection are stepped on and by this means the complete

plane is scanned before an address selection is repeated. Suitable ring counters will provide the drive pulses directly without any further need for amplification. For example the current pulses from the transistor collectors in a core/transistor ring counter or the advance pulse in a current routing counter may be designed to be of the right amplitude for the store. These counters are described in Chapter 12.

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Chapter 10

LOGICAL CIRCUITS USING TOROIDAL CORES

10.1. Introduction

Although the vast majority of the square-loop ferrite elements in use today are to be found in matrix stores, a large number are also being employed in digital computers and other data handling equipment as logical circuit components. This chapter is concerned with the use of toroidal cores in these circuits. Recently, multi-apertured devices have been developed as an alternative form of logical element and a description of these is given in the next chapter.

As random access storage elements, the advantages of square-loop ferrites over other known devices are fairly obvious, but as logical elements in the form of toroidal cores they are less easy to define in general terms and are usually only evident when the particular application is considered. They do, however, offer the advantages of small size, low weight and robustness when these qualities are at a premium and at low frequencies of operation their power requirements may be very small indeed. In addition the circuits can be designed to be relatively insensitive to ambient temperature variations. The extreme reliability of the core itself is to some extent offset by the multiple turn windings usually employed and by other less reliable components included in the circuits. The cost of core logic is not significantly lower than some other types although in some cases considerably fewer components may be needed.

The electrical characteristics required for cores in logical circuits are similar to those required for a core in a matrix store. Although coincidence driving is seldom used, a square-loop with a high ratio of switching to saturation permeability is desirable. Uniformity of coercive force is less important than in a coincidence store since higher drives are usually employed, but in some circuits cores

with closely controlled values of saturation flux would be advantageous.

10.2. Transfer circuits and shifting registers

Since it is not practicable to use a core as a control element without changing its magnetic state, core logical circuits are essentially dynamic, the logical operations being carried out as information is transferred between cores which act as temporary

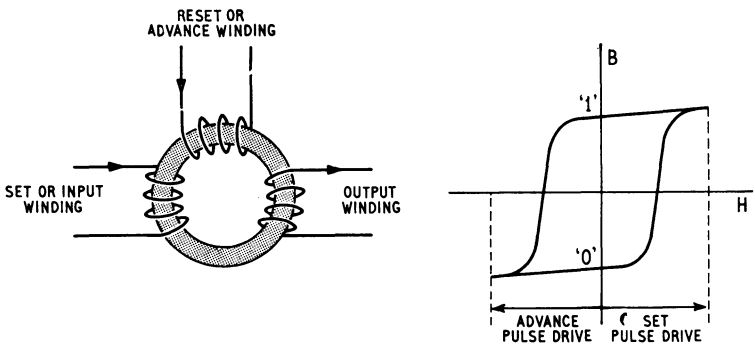

Fig. 10.1—General principle used in core logical circuits

stores. The repetition frequency of such transfers may be from zero up to a few hundred kilocycles per second. Higher frequencies of operation are possible but are not often used owing to the high power consumption and the difficulties arising from core heating. Various methods for effecting this transfer of information from one core to another have been suggested and these will be described before their capabilities for performing logical operations are considered in the next section.

The basic principle used in most core logical circuits is illustrated in Fig. 10.1. When no information is being transferred the core will remain in the lower remanent state. Upon the arrival of an input pulse, which is normally used to represent a " 1 " in the binary scale, the core will be switched to the upper remanent state. At a later time the application of an advance pulse resets the core to its initial state and the voltage appearing across the output winding during this operation is used to determine whether or not an input pulse is applied to another core. If no input pulse is received then no output voltage will arise when the advance pulse is applied.

A succession of cores operated in this fashion may be used as a serial shifting register.

10.2.1. CORE/DIODE CIRCUIT USING TWO CORES PER BIT

The first large group of circuits to be considered uses the output of one core directly as the source of energy for setting the next core. In this case the core must act as an amplifier if the magnitude of the flux change representing a " 1 " is to be maintained over a large number of cores in series since losses must inevitably occur in the coupling circuits. The gain characteristic of a core with its coupling network, i.e. from the input of one core to the input

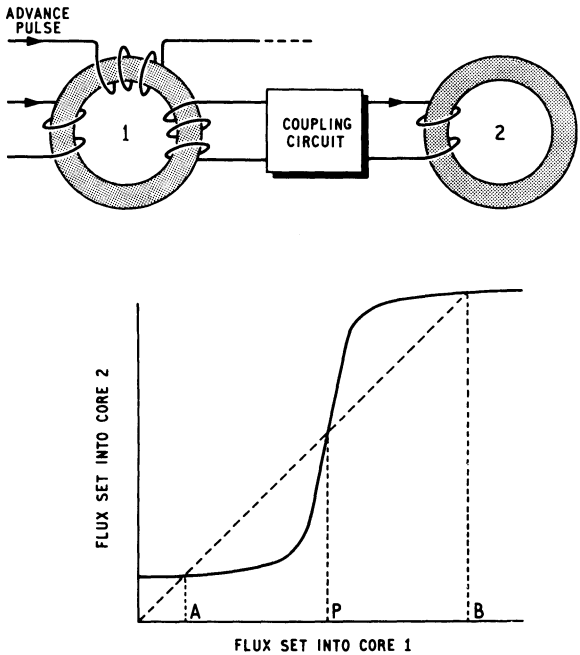

Fig. 10.2—Gain characteristic of core transfer circuit

of the next can be represented by the curve shown in Fig. 10.2 where the flux set into one core is plotted against that set into the next.[1] Unity gain is represented by the dotted line at 45°. Provided that the curve crosses this line in the manner shown it can be seen that over a number of stages any input less than the value

represented by P will tend to approach the value A and similarly any input greater than P will approach the value B. This shape of gain characteristic is essential if " 0 "s are to remain " 0 "s and " 1 "s are to remain " 1 "s and the areas between the curve and the unity gain line are an indication of the stability of the circuit since they represent its ability to withstand tolerances in components, etc.

A direct connection between the output winding of one core and the input winding of the next is not possible for two reasons. Firstly, a voltage will appear across the output winding when the

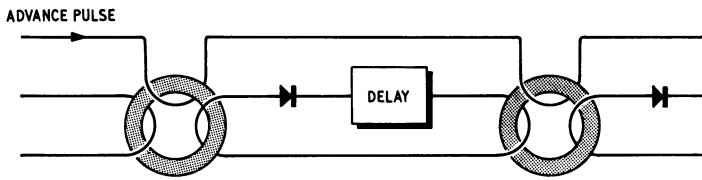

Fig. 10.3—Basic transfer circuit

input arrives and would affect the next core. The simplest way to overcome this is by the insertion of a diode in the output winding to block any current flow during the setting operation. Secondly, the input pulse cannot arrive at the same time as the advance pulse so that some form of delay is required between cores as shown in Fig. 10.3. Although, for simplicity only, one turn is shown for each winding in the diagram several turns are used in practice and it is essential that more turns are used on the output winding than on the input winding in order to allow for voltage drop in the coupling loop.

One of the earliest proposals[2] was the use of a similar core circuit as the delaying device as shown in Fig. 10.4. This arrangement, commonly called a two core per bit circuit since it requires two cores for each binary digit in the register, needs two phases of advance pulse. During the application of the first pulse, A, the information is transferred from the main register, composed of cores 1 and 3, to cores 2 and 4, which form a subsidiary register and when the second pulse, B, arrives the information is transferred back to the main register. The circuit shown possesses an additional refinement in that a shunt diode is used in the coupling network. The purpose of this component is the prevention

of flux transfer between one core and the previous one when the advance pulse is applied by providing a lower impedance path than that through the output winding of the latter. The resistance is necessary in order that the core being driven may be allowed to switch since it would otherwise be short circuited by the shunt diode on its input winding.

For a detailed analysis of the operation of the two core per bit register the reader is referred to the literature[3] but some of the important conclusions will be briefly mentioned. Assume that core 2 in Fig. 10.4 is being reset and a " 1 " is being transferred to core 3. It can be shown that, if both cores switch at the same speed, the minimum drive is required when the resistance in the coupling loop, i.e., the sum of the series resistance and the forward resistance

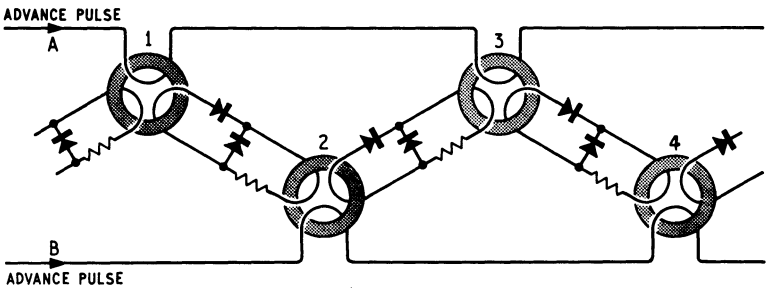

Fig. 10.4—Two core per bit circuit using shunt diodes

of the diode, is equal to the average equivalent input resistance of core 3 and, in addition, the turns ratio of the output winding of core 2 to the input winding of core 3 is 2:1. In this case the minimum drive is equivalent to four times that required to switch an unloaded core in the same time. The value of the series resistance and hence the number of turns in the input and output winding are determined from the permissible transfer of flux to the previous core (core 1) and the forward voltage drop across the shunt diode since the latter is applied across the output winding of core 3. In practice the circuit values will be arranged so that core 3 switches slightly faster than core 2 to ensure that the former switches completely but for this to occur an increased drive will be required and energy will be wasted in the resistor if core 3 is switched faster than is necessary. The small amplitude output of short duration from a stored " 0 " is prevented from building

up to a " 1 " by several factors including the forward voltage drop across the series diode, the square hysteresis loop of the core, and the leakage inductance of the windings. The leakage inductance cannot however be too high otherwise a " 1 " will not be transferred reliably, and this consideration places a lower limit on the area of cross section of the core. A small area of cross section is otherwise desirable from the point of view of economy in driving energy requirements.

The most suitable diode for use in these circuits is a germanium junction diode since its forward resistance is low and it provides an adequate frequency response.

10.2.2. CORE/DIODE CIRCUITS USING ONE CORE PER BIT

The fact that two cores and their associated components are used for each binary digit stored and the necessity for two phases of drive pulse may be considered to be disadvantages of the two core per bit circuit described above when employed in a shifting register. The first of these is less important in logical circuits since logical operations may be performed during shifts both to and from the subsidiary register. However, circuits have been devised and used which only required one core for each digit present. The best known of these[4,5] uses a capacitor to delay the energy transfer between cores as shown in Fig. 10.5.

The advance pulse, the amplitude of which is equivalent to several times the coercive force of the core, drives all cores to the " 0 " state. As a result, if core 1 contains a " 1 " it switches and current induced in its output winding flows through the diode to charge the condenser, C_1, more or less linearly. As the condenser voltage builds up a corresponding voltage will appear across the core input winding and cause current to flow through the resistance R_0 into the output winding of the previous core. Owing to the presence of R_0 this current will be small and will not affect this core since it is also being driven towards the " 0 " state by the advance pulse. During this time also, a certain amount of current will flow from C_1 through R_1 and the input winding of the following core but this current is again ineffective in causing flux change owing to the presence of the advance pulse. After the cessation of the advance pulse, C_1 continues to discharge through R_1 and will set core 2 to the " 1 " state. Zeros are prevented from building up in amplitude since the charge from the short duration "0" pulse which has not leaked away by the end of the advance pulse

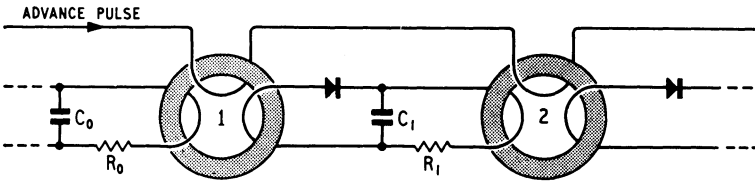

Fig. 10.5—One core per bit circuit using a condenser for temporary storage

will be insufficient to exceed the coercive force of the following core.

At high frequencies the condenser may not become completely discharged between advance pulses if a " 1 " has been transferred. This only means that a slightly larger charge is available for setting the core when successive " 1 "s are passing. If a " 0 " is following a " 1 " the action of clearing the " 1 " tends to discharge the preceding condenser so that " 0 "s are again prevented from increasing in size.

For this circuit the amplitude of the advance pulse is not critical provided that a certain level is exceeded. Its length, for a given amplitude, is fairly critical since if it is shorter than the cores' switching time incomplete clearing will result and if longer too much charge may leak away from the condenser before the next core is

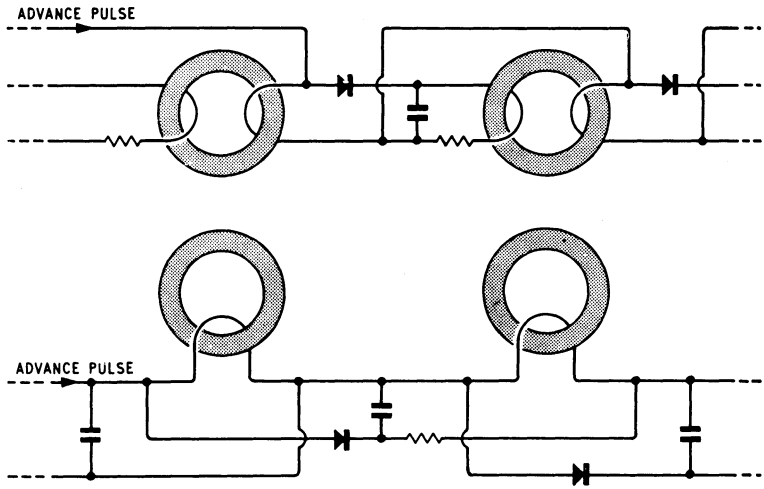

Fig. 10.6—Modified one core per bit circuits using fewer windings per core

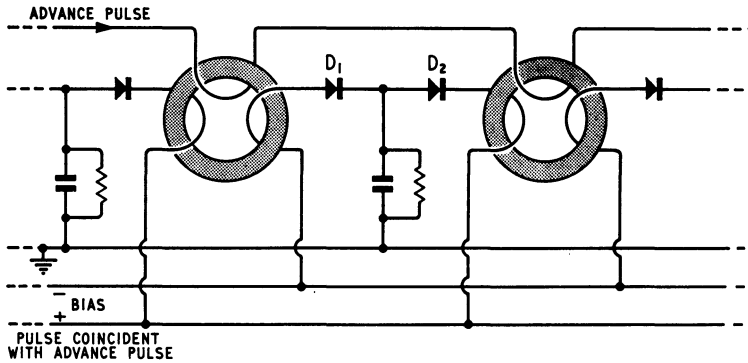

Fig. 10.7—Improved version of one core per bit circuit

ready for setting. The latter is more important if the register has been designed for operation at high frequencies when a small time constant for the *CR* network is required.

It is not necessary for the one core per bit shifting register described above to use cores with three separate windings. These may be reduced to two or even one as shown in Fig. 10.6. Although these modifications lead to a cheaper wound core, the facility of arranging winding impedances to suit other circuit components has been lost and difficulties arise if the combination of such circuits to perform logical operations is considered.

A diode may be used with advantage to replace the series resistor[6] as shown in Fig. 10.7. A bias voltage coincident with and derived from the advance pulse is applied across D_2 and does not allow the condenser to begin to discharge through the succeeding core until the advance pulse has terminated. By this means backward current flow is also eliminated and the length of the advance pulse becomes less critical. An additional refinement shown here is the standing bias across D_1. This helps to block " o " outputs and in addition allows the voltage across the output winding to rise to this level before current flows into the condenser so that faster switching and hence a higher repetition frequency may be achieved. Alternatively, the " o " output may be eliminated by biasing D_1 with the output of a compensating core which is driven by the advance pulse to provide a " o " output.

Reversible operation is also possible in a register using this transfer mechanism.

10.2.3. CORE/DIODE CIRCUITS USING MORE COMPLEX ADVANCE PULSE SEQUENCES

The circuit shown in Fig. 10.8(a) contains only a diode in the coupling loop. Outputs which arise when cores are being set to the " 1 " state are prevented from affecting succeeding cores by means of this diode. Conflicting requirements make this simple circuit rather difficult to design for successful operation. A high ratio of output to input turns is needed to prevent backward transfer of flux when a " 1 " is being advanced but a low ratio is desirable to prevent " 0 " increasing in amplitude since in the absence of resistance in the coupling loop most of the voltage across the output appears across the input of the next core. Various schemes involving more elaborate advance pulse arrangements have been suggested in order to overcome this difficulty.

Initially the " 0 " outputs are small and of short duration so that their effect on the following core during transfer can be greatly minimized by overlapping the advance pulses. Thus, for example, the *A* phase cores are held in the " 0 " state when " 0 "s produced from the *B* phase cores arrive. It has been shown[1] that more reliable operation is obtained during this overlap period if the advance pulse which is terminating is of larger amplitude than the one which is beginning.

When a " 1 " is being transferred, say from core 1 to core 2, it is clear that the switching time of core 2 must be shorter than that of core 1 if core 2 is to be completely switched. This means that core 1 is left with a low impedance on its output winding after core 2 has finished switching and in order to remove the remaining flux from core 1 in a reasonable time a large drive may be necessary. This can conveniently be applied during the overlap period so that the advance pulses now take the form which is shown in Fig. 10.8(b).

To enable a higher operating speed to be obtained an inverse d.c. voltage can be applied across the coupling diode. This voltage allows a core which contained a " 1 " to reset more rapidly after the following core has finished switching.

Another method described[7] involves the use of three phases of advance pulse as shown in Figs. 10.8(c) and (d). In addition to the pulse used for shifting the information a second pulse, shown dotted, is also applied to hold in the " 0 " state the cores preceding those being driven. Thus backward flux transfer is prevented and

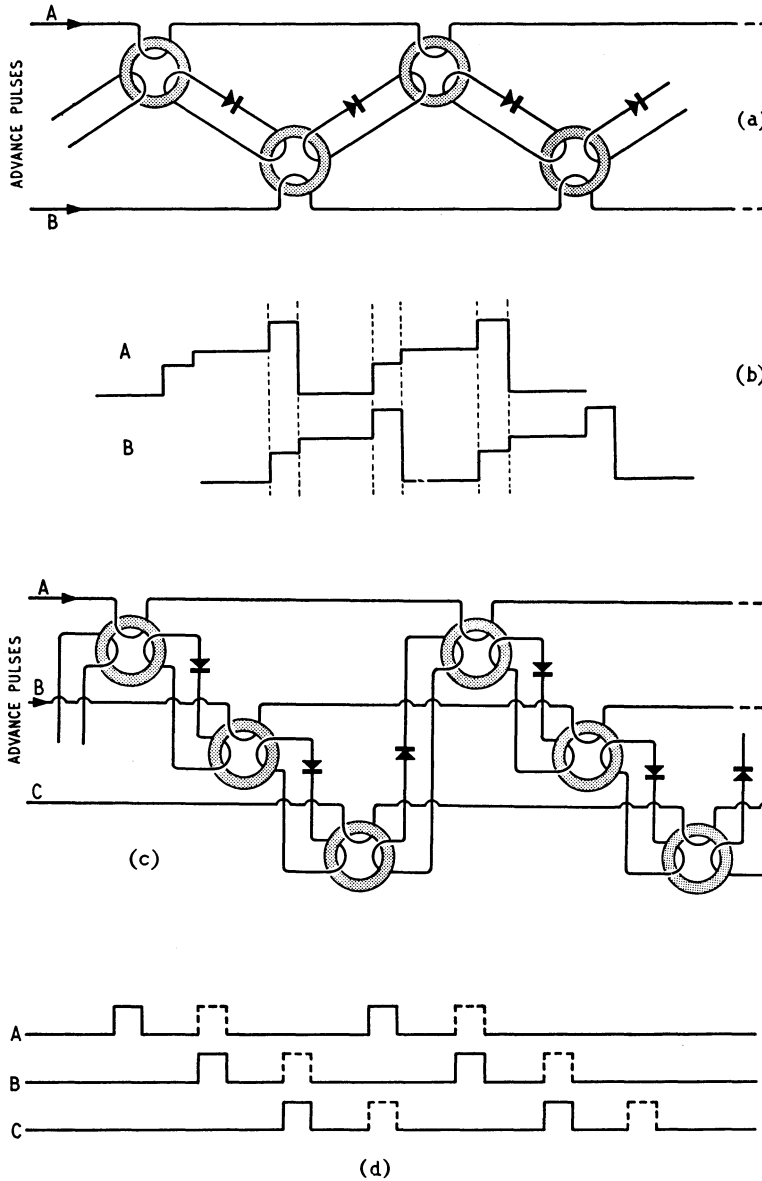

Fig. 10.8—Circuits using more complicated advance pulses

the turns ratio may be adjusted to reduce the possibility of " 0 " s increasing in amplitude.

Although the above circuits use few components more complicated advance pulse generators are needed so that any economic advantage will depend mainly upon the number of cores which can be switched from one pulse generator.

10.2.4. CIRCUITS USING CORES AND RESISTORS

A circuit which uses only wound cores and resistors may offer a slight advantage with regard to component reliability especially where extreme conditions such as a high ambient temperature are met. In general these circuits[8,9] require more than two pulse sources in order to perform a transfer operation and more than two cores per bit are usually necessary. Also, since the reverse to forward impedance ratio obtainable from a crystal diode is considerably better than any impedance ratio which can be provided by a square-loop core, the circuits without diodes tend to require small tolerances on components and drive pulse characteristics for reliable operation.

As an example the circuit[9] shown in Fig. 10.9 will be considered. If core 2 initially contains a " 1 " the advance pulse *A* will reset this core to " 0 " and its output will cause cores 3 and 4 to switch

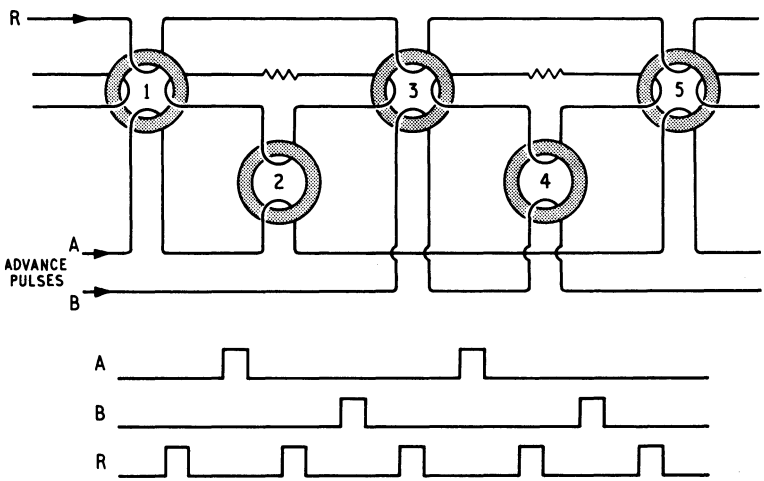

Fig. 10.9—Diodeless transfer circuit

to the " 1 " state. During this time core 5 is held in the " 0 " state by pulse A. When pulse A has terminated, core 3 is reset to " 0 " by the application of pulse R, the resistance in the coupling loop being sufficient to prevent the current flowing in this loop from exceeding a value equivalent to the coercive force of cores 2 and 4. In the next operation pulses B and R are used to transfer the information from core 4 to core 6 in a similar fashion. Thus, in this case four cores per bit and three drive pulse sources are needed. Owing to the fact that the drive R must be limited in amplitude, circuits of this type tend to be slow in operation.

10.2.5. SPLIT WINDING CIRCUIT

In all of the circuits described above the transfer of a " 1 " from one core to another involves using one core as a power transformer since the energy needed to switch one of the cores is derived from the output winding of the other which is in turn driven by the advance pulse. This leads to two problems. Firstly, in most cases a large amount of energy must be delivered by the advance pulse for each " 1 " being transferred since, apart from the switching requirements of the two cores, in many cases an equal or even greater amount of energy is dissipated in other circuit elements. Secondly, the output current waveform depends upon the core characteristics and also upon the elements loading the core. Thus the setting current pulse received by the input winding of the next core is not very well defined.

Various types of transfer circuit will now be described in which these problems are largely overcome. The first of these[10] uses two diodes and a split input winding in the coupling loop as illustrated in Fig. 10.10. If cores 1 and 2 both contain zeros no change of state occurs when the advance pulse, A, arrives since the current will divide equally between the two paths and core 1 will be driven further into saturation while core 2 receives no net drive. If, on the other hand core 1 is already set to the " 1 " state then the current through its output winding will tend to switch it to a " 0 " and the impedance presented by this winding, which possesses a large number of turns, causes the current to divide unequally betweeen the two paths so that core 2 is switched to the " 1 " state.

At low frequencies a core which contained a " 1 " can be completely reset by using a long advance pulse. If a high frequency is required the pulses R_1 and R_2 can be used to reset cores quickly

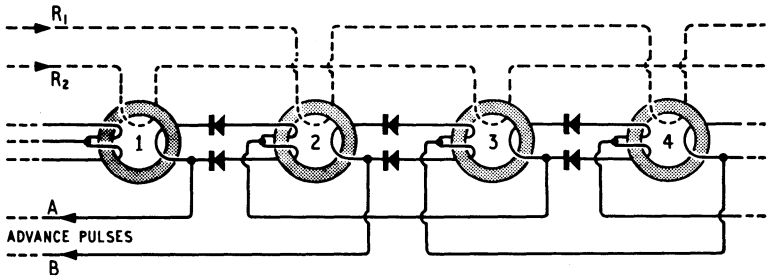

Fig. 10.10—Split winding transfer circuit

after the advance pulse has terminated. During this operation no current can flow in the output windings owing to the presence of the diodes. This diode arrangement also completely blocks any backward flux transfer during both the advance and the reset drives. In order to ensure that the advance current divides equally when a " 0 " is transferred it may be beneficial to insert a small resistance in series with each diode. This circuit has a good gain characteristic and furthermore, by means of additional windings, information can be inserted into or extracted from the main register in parallel without affecting the cores of the subsidiary register.

10.2.6. CURRENT ROUTING CIRCUITS

An important group of transfer circuits uses the current routing technique[11] which has been briefly discussed in Section 8.4. Here the cores are unloaded and are used only as voltage sources which in conjunction with diodes determine the path to be followed by a combined advance and setting pulse. Although the more attractive features of this transfer system only become apparent when its use is considered for more complicated logical operations it may be connected as a shifting register in the manner shown in Fig. 10.11.

In both circuits if a " 1 " is present in core 1 the advance pulse A will switch this core to the " 0 " state and cause a voltage to appear across its output winding with a polarity such that the diode D_2 is biased in the reverse direction. The advance current will then flow through the path containing D_1 and set core 2 to the " 1 " state. If core 1 initially contains a " 0 " then no output will result and the advance pulse divides between the two paths but as soon as a small amount of current flows through D_1 a small

voltage is generated across the input winding of core 2 and will be sufficient to cause most of the advance current to pass through D_2. Provided that the advance pulse is only present for a sufficient time to transfer a " 1 " then an insignificant amount of flux will be set into core 2 during a " 0 " transfer. By choosing a suitable number of turns on each winding it can easily be arranged that the output voltage of core 1 is always larger than the voltage appearing

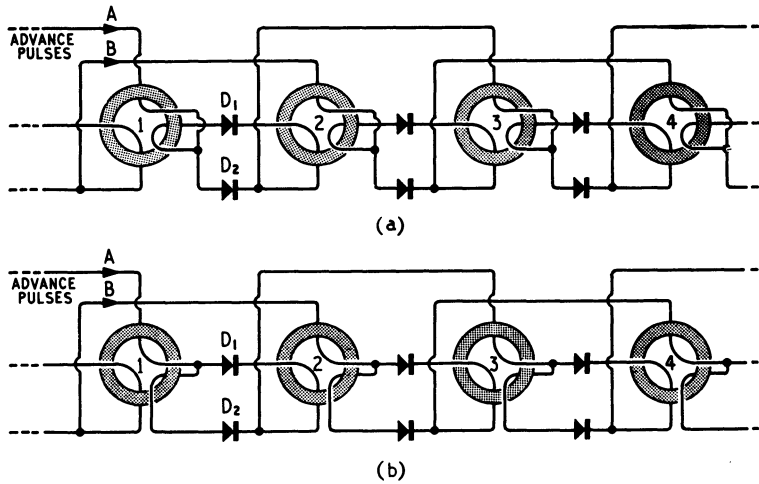

Fig. 10.11—Current routing transfer circuits

across D_1 and the input winding of core 2 in order to ensure that the latter is completely switched during a " 1 " transfer. The advantage of the first circuit, Fig. 10.12(a), is that there is a lower impedance in the path containing D_2 so that this path forms a more effective short circuit when a " 0 " is transferred. The second circuit, Fig. 10.12(b), has the advantage that the current flowing in the output winding does not oppose that in the advance winding so that in this case fewer turns are necessary on the advance winding.

Here again the blocking action of the diodes allows information to be inserted or extracted in parallel.

10.2.7. CORE/TRANSISTOR TRANSFER CIRCUITS

Another method for reducing the advance pulse power requirements is realized by inserting an active element, such as a transistor,

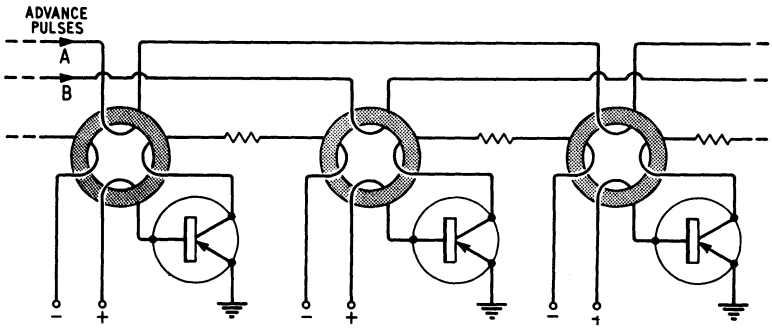

Fig. 10.12—Core/transistor transfer circuit

in the coupling loop to act as a power amplifier. The transistor also provides a standardized pulse to the input winding and by its unidirectional properties prevents any backward flux transfer. Core/transistor combinations provide excellent transfer gain characteristics and as a result a shifting register composed of these elements is relatively easy to design and is capable of accepting large tolerances in component characteristics and drive pulses. Against these the cost of the transistor makes the circuits more expensive than most of those previously described.

The transistor can be operated with either its emitter, collector or base grounded. A grounded emitter configuration[12,13] is shown in Fig. 10.12. In this circuit a feedback winding from the collector is included. An advance pulse of short duration drives a core towards the " 0 " state and thereby induces a voltage in its output winding such that the transistor is driven into conduction. If the core is in the " 1 " state, regeneration occurs owing to the presence of feedback and the transistor will continue to conduct until the core is completely switched. During the same period the next core is set to the " 1 " state since its input winding is also driven from the transistor collector. A core in the " 0 " state will be driven further into saturation by the advance pulse and its low permeability in this region does not allow sufficient gain for regeneration to occur so that the " 0 " output from the transistor does not significantly affect the flux state of the succeeding core. In addition, by using a transistor with a suitable frequency response, it may be arranged for the short duration " 0 " output to be over before the transistor has been brought into conduction. The duration of the " 1 " output depends upon the saturation

flux of the core and the voltage which is allowed to develop across the output winding, i.e. the bias voltage plus the transistor emitter/base voltage. More elaborate circuits which ensure that the output pulse is of fixed duration are considered in the next section but these are not necessary for a shifting register. Stabilization of amplitude may be achieved by using a series resistor in the collector so that the transistor is bottomed and most of the load voltage is developed across it.

Owing to the small power requirements of the advance pulse it is possible to supply a very large number of cores from a drive circuit which uses only low power high frequency transistors.

10.3. Logical circuits

In the previous section several transfer circuits have been described and a comparison was made of their ability to transfer information reliably from one core to another as normally required in a shifting register. This involves only the simplest of logical operations in that an output must arise when an input has been presented. In this case the choice of transfer circuit is probably determined mainly by the cost of components and the extent of design and component tolerances that the circuit will withstand.

The general principle used in core logical circuits is that one or more words are presented serially to one core or set of cores and at a later time the result of the logical operation, which has been performed during transfers, will appear in another core or set of cores. A number of transfers may be necessary to achieve the required function. Any core in the circuit may be required to accept inputs from and deliver outputs to more than one other core. Thus another important factor now arises to govern the choice of transfer circuit in that if in one circuit a core can cope with more inputs and outputs than in another then a system using the former is likely to need fewer components and also fewer transfers to complete an operation. A decrease in the required number of transfers probably means an increase in speed although the minimum transfer times are not the same for all types of circuit.

For the purpose of discussion it is convenient to classify the transfer circuits into three general types as follows:—

(a) " Loaded core " circuits in which the core output, which is derived by transformer action from the advance pulse, is used directly to set information into succeeding cores.

(b) Transistor-core circuits in which the output of a core is amplified by a transistor before being used to set other cores.

(c) Current routing circuits in which the advance pulse is used to set cores, its path being determined by core outputs.

10.3.1. " LOADED CORE " LOGICAL TECHNIQUES

The general principle employed in this type of circuit is illustrated in Fig. 10.13. A positive input applied to the dotted terminal

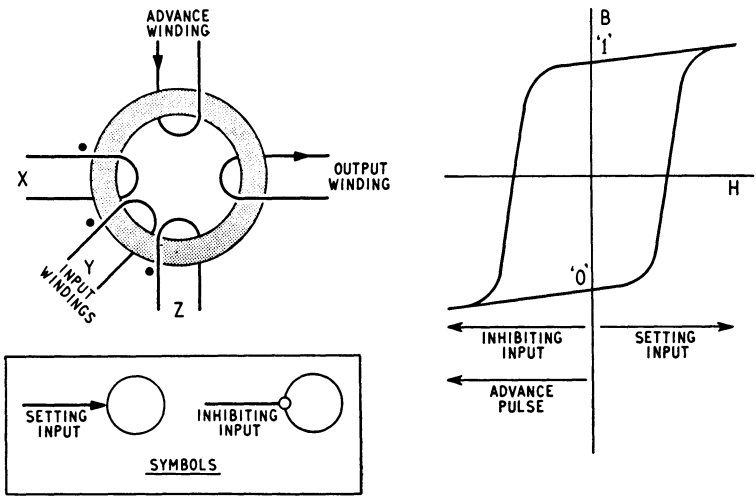

Fig. 10.13—Operation of a core in serial logic circuits

of one, two or three of the input windings X, Y and Z will set a core to the " 1 " state so that a " 1 " output suitable for setting other cores is produced by the application of the advance pulse at a later time. Similar inputs applied to the other terminals will drive a core further into saturation in the " 0 " state so that no output results. Assuming that the current input waveforms are identical the action of an input to the dotted terminal may be inhibited by an input to an undotted terminal of another winding. The symbols to be used for these two types of input are shown in the lower part of the diagram. Thus, with three input windings, two set inputs must be present to override one inhibit, while if two inhibit inputs are present it is impossible to set the core to the " 1 " state. Extra input windings may, of course, be used to

generate more complex functions on one core and it is also possible to use half currents as discussed later.

With " loaded core " circuits the inputs received from other cores are liable to exhibit large variations, both in amplitude and length, so that if inhibiting signals are being used the number of input windings which are energized simultaneously is severely limited and in general is restricted to two. The reason for this is that where an inhibit input is to be overridden by the presence of two set inputs, as might be the case in a simple *AND* gate, a short inhibit signal will allow the core to begin switching under the influence of one set input after the inhibit signal has terminated, while a long inhibit signal will tend to return the core to the " o " state after the set signals have finished. It is evident that pulse length is more critical than pulse amplitude since variations in the latter may be accommodated to a large extent by making use of the square-loop characteristics of the core.

Although variations in component characteristics contribute partly to the nonuniformity of input waveforms, most of the differences arise from the type of load which is attached to the core output circuit. For ease of logical design it is preferable that a core should be able to feed its output to at least as many cores as its number of input windings. For example a core with two input windings should be able to feed an output to two other cores. In this case the two cores being fed may be either set or inhibited so that the back voltage from these, seen by the previous core, may be either $2V$, V, or zero where V is the back voltage from one core being set. This means that if a current drive is used for the advance pulse the output current amplitude will be fairly well defined but its length, which depends on the load voltage, will be variable. In the two core per bit core/diode circuit this undesirable feature may be offset to some extent by using a large output to input turns ratio and a high value of series resistance so that most of the load voltage appears across this resistor. In the one core per bit circuit using a condenser for temporary storage the mechanism is slightly different in that the condenser acts as the source of energy for setting other cores but the effects are similar.

In view of these difficulties " loaded core " circuits usually use two input windings on each core and if one winding is used for inhibiting, this winding may have extra turns to ensure that it overrides a nominally equal amplitude set pulse on the other winding. If one core only feeds two others, as shown in Fig.

10.14, then pulse length problems are not troublesome since the duration of the longest set pulse, t_2, results from feeding a set and an inhibit winding but this is also the condition for the shortest inhibit pulse.

Using these restrictions a number of elementary logical circuits obtainable are shown in Fig. 10.15. In the case of the *OR* function

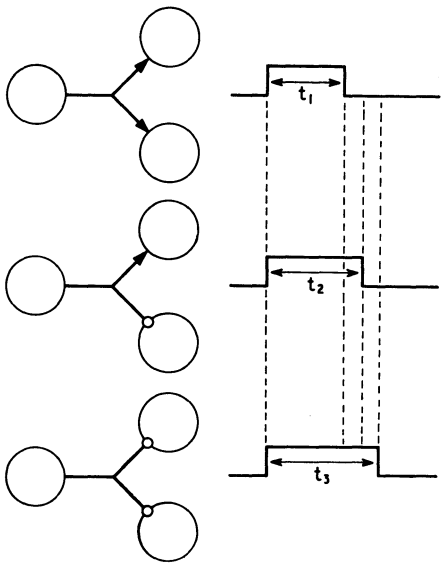

Fig. 10.14—Output current waveforms from a core loaded by two others

an alternative circuit may be used where the output windings of two cores are connected in parallel through diodes but this would not be used in a system constructed of standard building blocks consisting of one core with its coupling network. The " 1 " generator in the complementing circuit consists of a core which is always set to the " 1 " state between the arrivals of its advance pulse so that a " 1 " output always results.

The construction of circuits to derive more complex logical functions using these basic elements can be accomplished without difficulty but a relatively large number of cores and transfer times may be required.

As stated before a close control of the output current duration would enable more input windings to be used on each core. This

then leads to the possibility of using half currents so that a smaller advance drive will suffice and some of the basic operations may be performed in a simpler manner. For example the *AND* function may now be formed by the coincidence of two half inputs neither

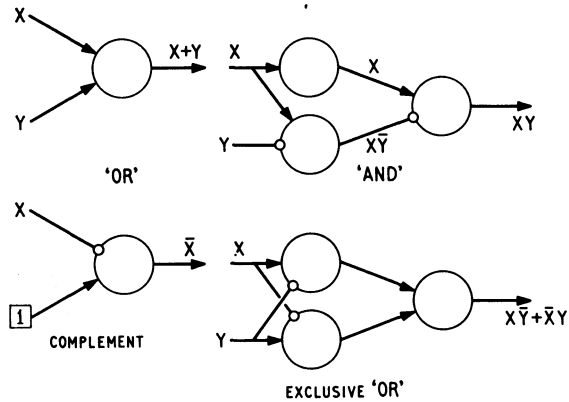

Fig. 10.15—Basic functions obtainable from loaded core circuit

of which is, by itself, sufficient to set a core. One circuit which is claimed to achieve the uniformity of output pulse necessary for this type of operation is the circuit described in the previous section where overlapping stepped advance pulses are employed.[1]

10.3.2. CORE/TRANSISTOR LOGICAL TECHNIQUES

Core/transistor techniques enable many more inputs and outputs to be attached to one core plus its coupling network than are possible with the " loaded core " circuits. Fewer cores are thus required for a given function generator so that in spite of the extra cost of each transfer circuit the total cost may be less.

In Section 10.2 the use of a core/transistor circuit for a shifting register has been considered in which the output current amplitude is stabilized by means of a collector resistance. This circuit and a circuit in which the current is controlled by an emitter resistance[14] are shown in Fig. 10.16. The main advantage of the first circuit is low power dissipation in the bottomed transistor but the second circuit will provide a closely controlled output to more cores since nearly the whole of the supply voltage may be taken up across the load. Although not shown, a feedback winding may be used in both cases in order to reduce the advance pulse power requirements.

In Fig. 10.16(b) the voltage developed across the output winding during the advance pulse period is defined by means of the diode D_1 so that this voltage in conjunction with the emitter resistance will control the collector current fairly accurately. In both circuits the duration of the output current pulse depends upon the switching time of the core. This switching time is determined by the volts

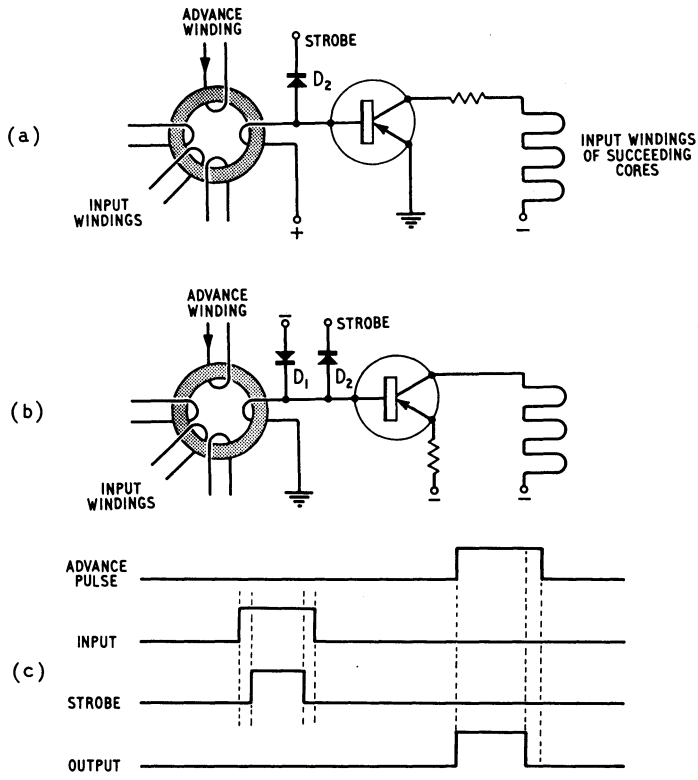

Fig. 10.16—Core transistor logical circuits

per turn allowed across the output winding and the flux swing in the core if it is assumed that the advance pulse is applied for a period long enough to completely switch the core. Since cores are not normally selected on the basis of close tolerance of saturation flux the outputs are liable to vary in length from one circuit to another. It is possible to gate the output so that current only flows to other

cores during a specified period but a more economical method allows the whole of the pulse to pass to succeeding cores but prevents any change of flux in these cores except during a strobe period. This is achieved by providing a short circuit on a winding on these cores and using a strobe pulse to remove the short circuit as illustrated in Fig. 10.16(c). The output winding can be used for this purpose since during the setting period the base of the transistor is driven

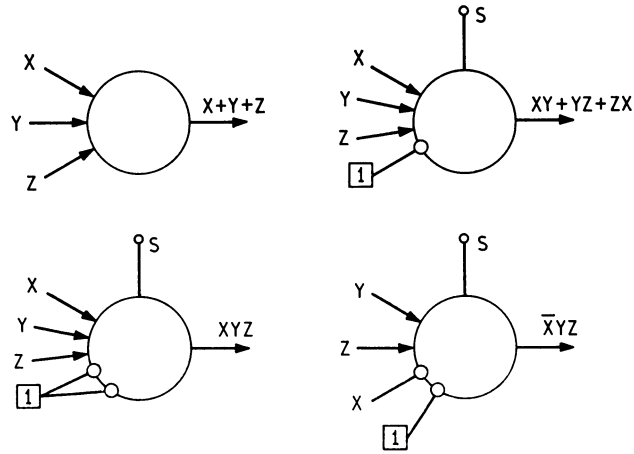

Fig. 10.17—Examples of functions obtainable from a core/transistor combination using a strobe pulse(s)

positively. Normally the cathode of D_2 is held near earth by a low impedance source. During the strobe period the cathode is taken positively thus allowing a voltage to be generated across the output winding so that the core may switch if required. A secondary purpose of the strobe pulse is the limitation of voltage swing during setting so that the reflected voltage across each input winding is well defined. This enables the number of cores which can be fed from a transistor to be determined more exactly and by suitable adjustment of the strobe pulse amplitude this number may be increased though at the expense of speed.

Examples of logical functions which may be produced by using building blocks consisting of one core and one transistor, as shown in Fig. 10.17, using the same symbols which were employed for the "loaded core" logic. There remains one fundamental restriction to the operations which can be performed using this circuit. A long inhibiting pulse cannot be overridden by shorter

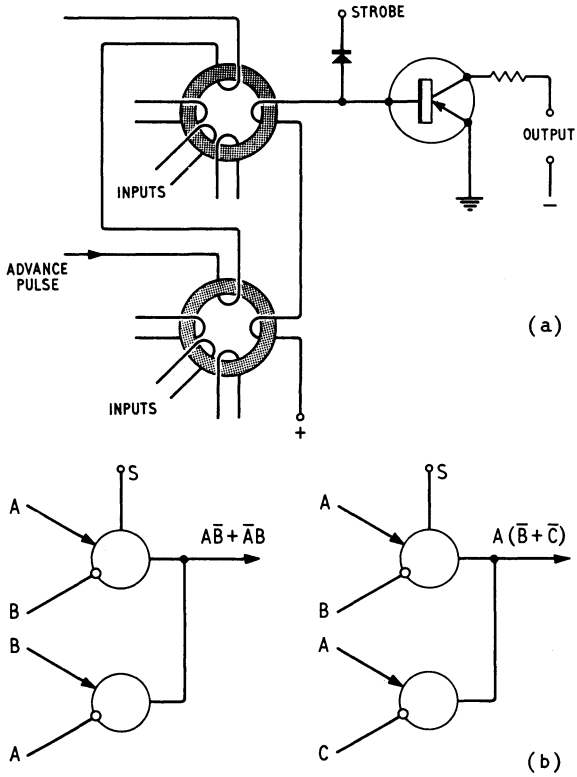

Fig. 10.18—Circuit using two cores with one transistor and examples of functions obtainable

setting pulses otherwise the core will switch back towards the zero state during the last part of the inhibiting pulse. Switching in this direction is not prevented by the absence of a strobe pulse. Thus, for example, the function $(Y + Z)\bar{X} + YZ$ cannot be obtained from one core by inhibiting Y or Z with X since X may be longer than either Y or Z. This restriction does not necessarily apply to inhibition by a " 1 " generator since the duration of an input from this may easily be arranged to be shorter than any information pulse likely to be developed.

The use of half current pulses is also possible since the amplitude tolerances, particularly from the circuit of Fig. 10.16(b), allow this mode of operation.

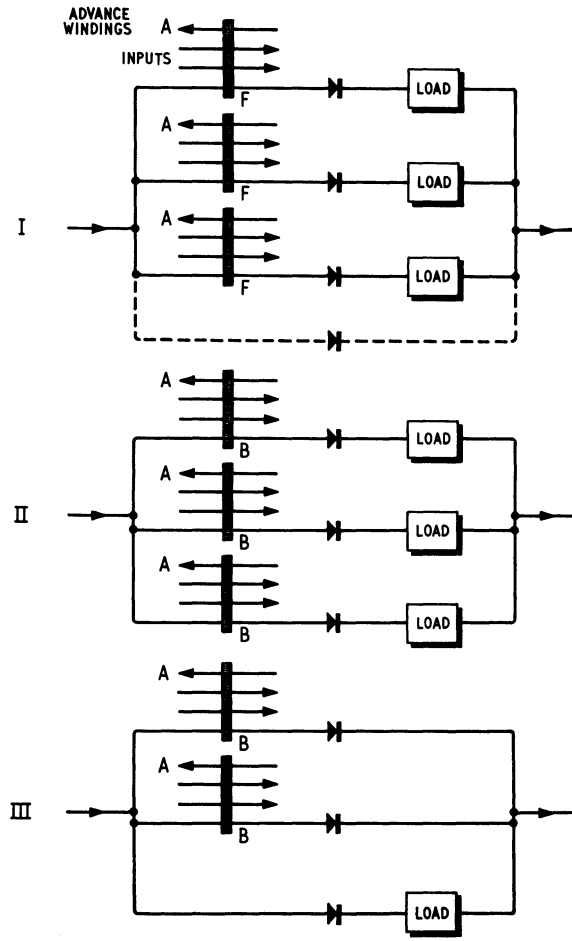

Fig. 10.19—Circuits using current routing techniques

An *OR* function can be provided by series connection of output windings as shown in Fig. 10.18(a). This allows fewer transistors to be used and some functions which can be obtained by this means are shown in Fig. 18(b). A standard building block consisting of two cores and one transistor can be used more economically than a one core block in most cases.

Other variations of core/transistor circuits may have advantages. For example a circuit has been described[15] in which the core is both set and reset by clock pulses and setting is permitted or inhibited according to the information received from previous cores. The inhibition is accomplished by providing a short circuit across a winding.

10.3.3. CURRENT ROUTING LOGICAL TECHNIQUES

Three basic logical circuits[11] using the current routing transfer technique are shown in Fig. 10.19. In circuit I the polarity of the voltage induced in the output windings when the core is reset by the advance pulse is such that its associated diode is forward biased (*F*) and the output voltage is developed across the remainder of the diodes in the reverse direction. Thus the advance pulse passes through the branch on which a core is switched. Before branching the advance pulse flows through advance windings, *A*, on the three cores in series. It is assumed in the diagrams that a pulse shown from left to right on the input windings is in the direction to set a core and one from right to left in the direction to inhibit setting. All inputs provide identical driving fields and may be considered to be advance pulses of the opposite phase which have been routed to these cores by a previous set of cores. In turn the loads shown may be the input windings of succeeding cores. Since the inputs are well defined in amplitude and duration almost perfect cancellation will result from an input in each direction provided that they arrive simultaneously. In circuit I the inputs must be arranged so that one and only one of the cores is set during the input phase but if desired the shunt diode shown in the dotted path may be inserted to allow the condition that no core need be set by providing an alternative route for the advance pulse. The outputs may be fed to separate loads as shown or some or all may be connected together to feed a common load.

A different principle is used in circuit II. Here the output from a switched core during resetting is of a polarity such that the diode in the same branch is biased in the reverse direction (*B*) and blocks the advance pulse. In this case all cores except one must be set by the inputs so that only one core is unswitched by the advance pulse and provides the path of this pulse to the load. This circuit has the disadvantage that more cores are switched than in circuit I. However, the circuit is more easily adapted for complex functions since more than one output winding can be used on a core so that fewer cores can be used for a given number of outputs. A shunt

diode cannot be used but if only one output is required the modification shown in circuit III may be advantageous. In this circuit the load is shunted by a logic core network similar to that of circuit II and the advance pulse is routed through the load for any input combination which sets cores to block all alternative paths.

The input connections for deriving the basic *OR* and *AND* functions with these three circuits are shown in Fig. 10.20. The " 1 " inputs can be the advance pulse of the opposite phase to that used in resetting the cores but the use of double-sided logic in which both a function and its complement are available leads to simpler circuits in that no " 1 " pulses need be used and fewer windings are necessary.

If the outputs from one set of cores are used as inputs to further cores the turns ratio can be adjusted so that the latter are switched more rapidly and are thus completely switched before the inputs

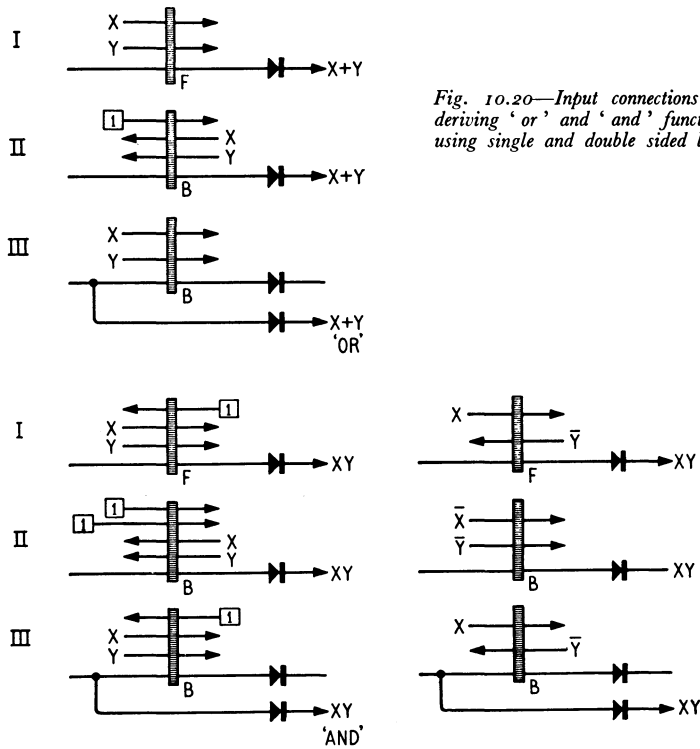

Fig. 10.20—Input connections for deriving ' or ' and ' and ' functions using single and double sided logic

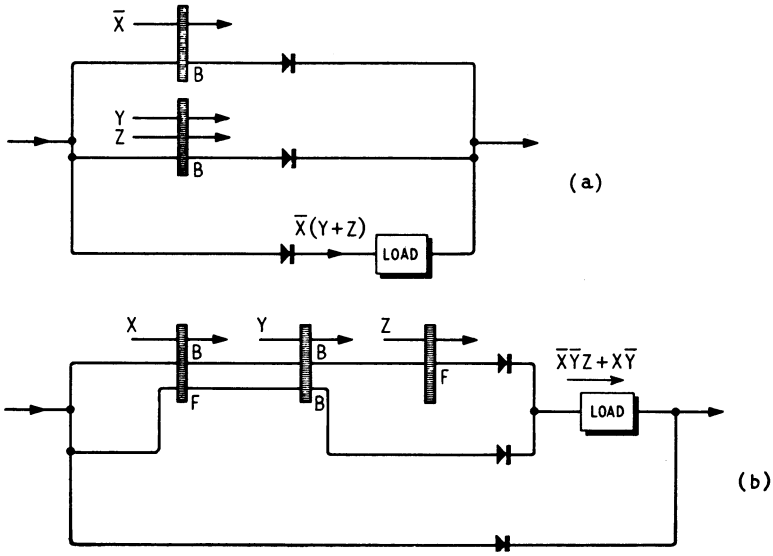

Fig. 10.21—Current routing circuits using only setting inputs

are terminated. In circuit I allowance must be made for the fact that current in the output winding opposes the field produced by current in the advance winding.

Cores which have not been set give rise to " 0 " outputs which cause a spurious pulse to appear on output lines which should otherwise carry no signal. This effect is particularly troublesome in circuit III but may be reduced by inserting an *LC* network in the load path. By this means the amplitude of the short duration unwanted signal can be decreased to a level which is insufficient to switch succeeding cores without seriously affecting a " 1 " output.

If inhibition is being employed on input windings another source of error may be due to inputs not arriving simultaneously. This problem can be solved by rearranging the circuit so that the input windings only receive setting pulses to drive cores towards the " 1 " state and then performing further operations in the output network. Circuit III lends itself to this method of operation as shown by the simple example in Fig. 10.21(a) but may use a comparatively large number of cores in the process. A more elegant solution has been suggested[16] in which outputs of both polarities are used in a circuit similar to circuit I. It is arranged that there

is only one forward biasing output winding on each output line and a minimum of one backward biasing output winding. By this means an additional advantage is obtained in that a forward "o" output is always cancelled by at least a backward "o" output so that practically no spurious outputs result. An example of this circuit is shown in Fig. 10.21(b).

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Chapter 11

MULTI-APERTURED LOGICAL ELEMENTS

11.1. The transfluxor

Blocks of square-loop ferrite material containing a number of apertures have been developed for use as logical circuit elements. As an alternative to the toroidal core circuits discussed in the previous chapter, circuits containing these elements can offer some important advantages including increased reliability, smaller size and lower cost. These qualities arise from the fact that comparatively complex logical functions can be derived from a single block so that most applications require only a small number of such blocks. Some of these devices are also capable of high speed operation but the large energy requirement for this purpose probably means that their main contribution will lie towards reducing the cost and increasing the reliability of digital computers working at digital rates not exceeding a few hundred kc/s.

The basic principle used in the operation of a multi-apertured device involves the establishment of one of a number of various possible flux patterns by means of input signals on windings linking different parts of the element and producing an output which corresponds to the pattern inserted. Two general methods of operation have been described. The first of these has been used in elements known as transfluxors and is described in this section.

A two hole transfluxor[1] is shown in Fig. 11.1. This element is only capable of performing fairly simple operations but it illustrates the principles used in all transfluxors. Windings can be arranged to link the element as shown in Fig. 11.1(a). If the cross sectional area of leg 1 equals the sum of the areas of legs 2 and 3 then a blocking pulse applied to a winding linking leg 1 can be used to saturate the material in a given direction around hole *A*, Fig. 11.1(b). Under these conditions a drive current applied

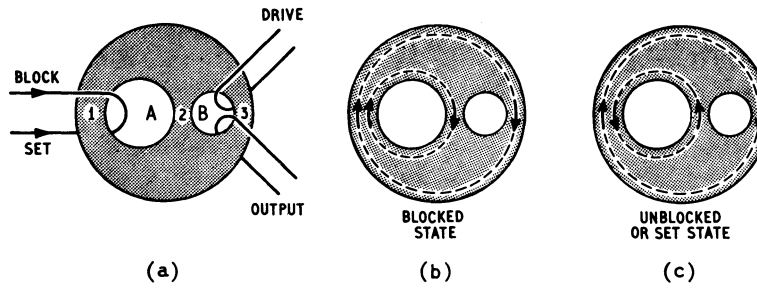

Fig. 11.1—Two hole transfluxor

later to the drive winding linking leg 3 will be unable to induce an output in the output winding since a flux change around hole *B* is not possible, provided that the drive current is not large enough to reverse flux along the path encircling both holes.

A setting pulse applied to the same winding as the blocking pulse, but in the opposite direction to the latter, can be used to unblock the element. The setting pulse amplitude is arranged to produce a field exceeding the coercive force of the material in the flux path through legs 1 and 2 but less than the coercive force in the path through legs 1 and 3. Thus the direction of saturation immediately surrounding hole *A* can be reversed and the pattern shown in Fig. 11.1(c) is established. A drive current of sufficient amplitude can now switch flux around hole *B* and provide an output. The drive current may take the form of a single pulse but is more commonly an alternating current.

The two hole transfluxor provides both a memory and gating function and as a result forms a useful type of switch for many applications. Among these are channel selection and a non-destructive read-out store.[1] For channel selection one transfluxor is connected to each output channel. Selection is accomplished by applying blocking pulses to all transfluxors except the one on the desired output. A setting pulse on a separate winding common to all transfluxors is applied coincidently with the blocking pulses and causes the unblocked transfluxor to be set. Drive pulses applied later to a common drive winding will then provide an output only on the selected channel. Combined decoding and selection can be achieved by arranging blocking windings in a similar manner to the setting windings in the decoding switch described in Chapter 8.

A non-destructive read-out store may be obtained by using the set and blocked states of the transfluxor to represent stored binary digits. A coincident current matrix wired through hole *A* is used for writing and a separate matrix wired through hole *B* for reading. If all transfluxors are initially blocked a " 1 " may be written by coincident half pulses through hole *A* which set the selected transfluxor, the presence of one half pulse being insufficient to cause

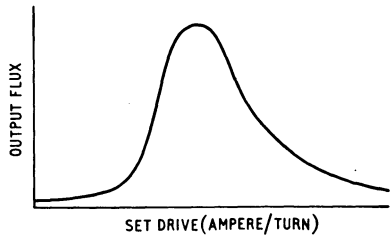

Fig. 11.2—Variation of output with set current for a constant drive

any change of flux. A " 0 " may be written in by similar pulses in the opposite direction which return the transfluxor to the blocked state. Read pulses consist of a pulse in one direction followed by a pulse in the other so that the net effect of a read operation on the flux state of a core is zero. Set cores provide output pulses to a common read wire during the read operation. A half read pulse must be insufficient to cause any change of flux round hole *B*. A store of this type can be used as a " semi-permanent " store and provides an alternative to those described in Chapter 9.

Various difficulties arise with the two hole transfluxor and a number of methods[1,2] have been developed to overcome these. Fig. 11.2 shows the general form of curve relating the setting pulse amplitude to the output obtained for a given drive. There is a fairly sharp peak in this curve where approximately half the total flux around hole *A* has been reversed by the setting pulse. The actual output obtained is thus rather critically dependent upon the setting pulse in this region which is the region for maximum ratio of unblocked to blocked output. Furthermore, since coercive force varies with temperature, the setting drive corresponding to this peak will change with ambient temperature.[3] In some cases leg 2 can be used for setting, in which case the setting pulse is not critical, provided that the maximum output is desired since a winding on leg 2 cannot do more than reverse half of the

total flux around hole *A*. A disadvantage is that the output circuit is now loaded by the impedance on the setting winding.

The drive current amplitude is also fairly critical since it must be sufficient to exceed the coercive force of the material in the path around hole *B* but not around both holes. This is again adversely affected by temperature changes.

If a linear voltage relationship is required between drive and output winding the changing impedance of the transfluxor between blocked and unblocked states presents another problem and finally the output obtained in the blocked state is not zero owing to the fact that the permeability of the material at saturation is not zero. Two forms of transfluxor which are designed to reduce the problems mentioned above are shown in Figs. 11.3 and 11.4. The first of these, Fig. 11.3(a), is a three hole element in which setting can be accomplished by applying a pulse to leg 1. Optimum setting will now result with a setting pulse of sufficient amplitude without the output circuit being loaded by the setting winding. This element may be used for other purposes such as a shifting register[4,5] and for a few simple logical operations. One method[4] of transferring

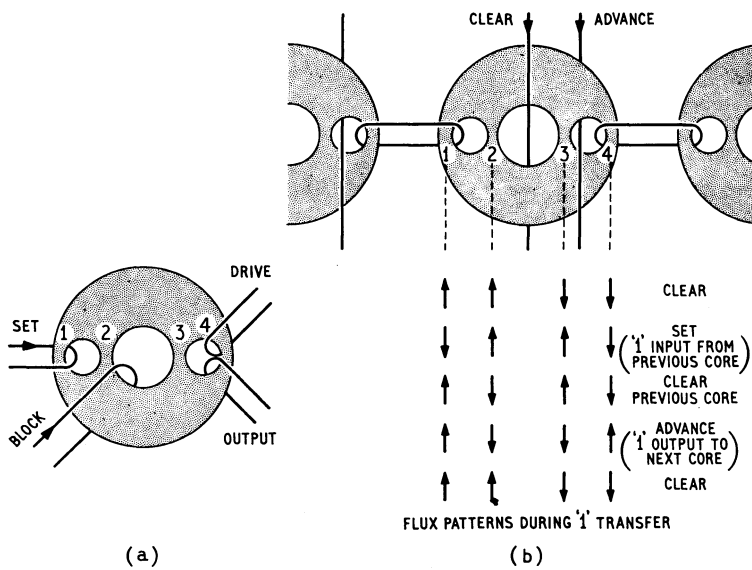

Fig. 11.3—Three hole transfluxor and its use in a shifting register

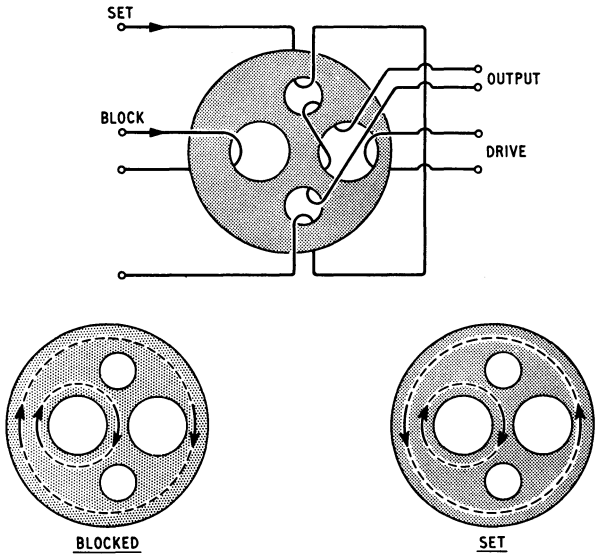

Fig. 11.4—Four hole transfluxor

information from one transfluxor to another as in a shifting register is illustrated in Fig. 11.3(b) where the flux patterns in the transfluxor during the transfer of a " 1 " are shown. Since inputs and outputs cannot take place simultaneously a " two-transfluxors-per-bit " system employing two phases of clearing and advance pulses are necessary. A " 1 " input switches flux in legs 1 and 3 so that advance pulse following this can switch flux around legs 3 and 4, and provide a " 1 " output to set a subsequent core. Outputs resulting from clearing pulses are not transmitted further than the input aperture of the next core since, as shown by diagram, flux change around legs 1 and 2 is possible after a " 1 " has been inserted. No flux changes take place during a " 0 " transfer. In practice it may be advantageous to use leg 2 for the input winding to reduce the ampere turns required for setting and to wind the advance winding around leg 3 to reduce direct pickup in the output winding. Various methods for cancellation of the " 0 " output may be incorporated to prevent " 0 "s from building up to become " 1 "s.

The second type of improved transfluxor[2] also removes the maximum amplitude restriction on the setting pulse when wired

as shown in Fig. 11.4 and has the additional advantage that no output arises during either the blocking or the setting pulse since flux changes due to these do not link the output winding.

Simple logical functions can be derived from the transfluxors described above so that more complicated functions may be

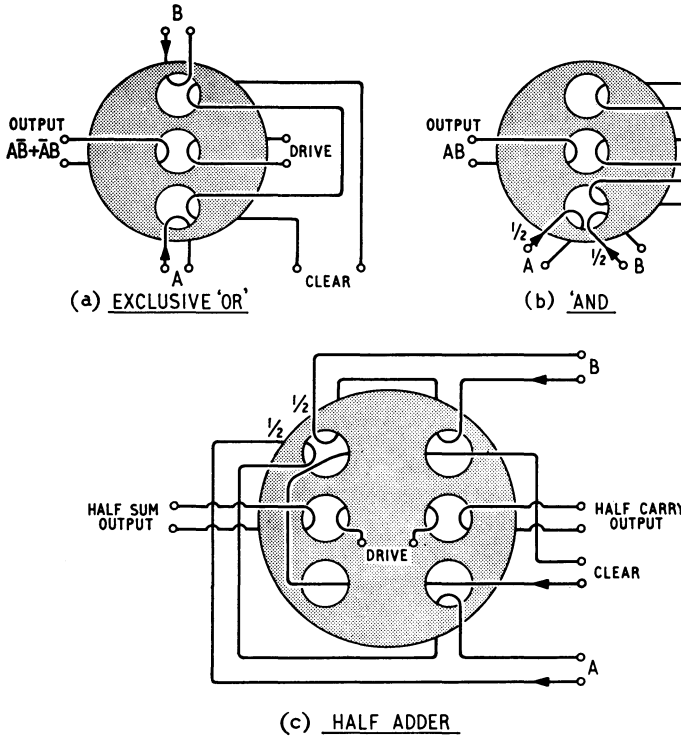

Fig. 11.5—Logical functions from transfluxors

achieved by connecting a number of these together. However, the latter can be obtained in a more economical and straightforward manner by means of elements containing a larger number of apertures. One system[2] uses the principle illustrated in Fig. 11.5(a) in which an exclusive *OR* output is provided from windings through three holes. The presence of either input alone unblocks the flux path immediately surrounding the centre hole but if both inputs are present this path is again blocked since the flux in both

legs has been reversed. An *AND* function can be obtained if coincident half set pulses are used as in Fig. 11.5(b). One pulse is arranged to be insufficient to overcome the coercive force of the material around the input aperture by limiting the number of turns on the input windings so that both pulses are necessary in order to switch the flux around this aperture and unblock the path around the output aperture. The two operations illustrated in Figs. 11.5(a) and (b) can be combined in the six hole transfluxor shown in Fig. 11.5(c) to form a half adder. A six hole transfluxor of this type can be used to perform other logical operations by using different winding arrangements.

11.2. The Laddic and similar devices

The transfluxors described in the previous section are capable of providing an output function, corresponding to a given set of inputs, for an indefinite number of times if a pulse drive is used or for an indefinite length of time if an alternating current drive is used. This property is the result of the fact that the drive current does not destroy the flux pattern which has been inserted by pulses on the input windings so that the pattern can be used repeatedly until the element receives a reset pulse. It is in applications where this property is required that the main use of the transfluxor lies. In most logical systems the output function is required only once and in this case other devices such as the Laddic,[6] described below, have definite advantages.

For these devices a property of the material additional to those required from a simple toroid is commonly used and is illustrated in Fig. 11.6. If leg 1 of the element shown is switched by means of a drive pulse on winding *D* then a flux change equal to that in leg 1 must occur in legs 2 and 3 since flux paths are continuous within the material. It is found that the ratio of flux change in leg 2 to that in leg 3 is very much larger (about 20:1 for the dimensions shown) than would be expected from consideration of the path lengths and switching speeds for the two legs and is independent of the drive provided that the drive pulse amplitude is sufficient to cause complete reversal of flux in leg 1.[6] Thus for a qualitative description of logical operations in this element it can be assumed that flux change will take place along the shortest possible path and leave other paths unaffected. An explanation of this behaviour which involves the dynamic reluctance of the material has not yet been given. This method of flux setting may be compared

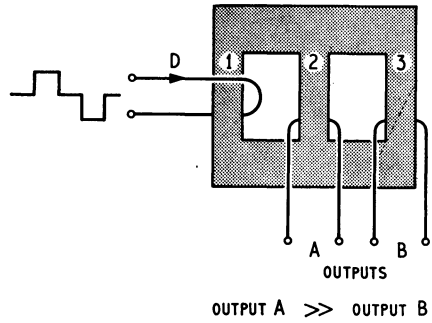

Fig. 11.6—Principle used in multi-apertured logical devices

with that in the transfluxor where, with less favourable geometry, unwanted flux changes in various paths are prevented by limiting the amplitude of the setting pulse so that the field experienced by these paths does not exceed the coercive force.

An application of this principle for high speed storage has already been discussed in the coincident flux store of Chapter 5. When used in logical applications a variety of methods using different shapes of element and different wiring arrangements may be used. One of the most straight-forward methods[7] is illustrated in Fig. 11.7(a). After a clear pulse the direction of saturation flux is as shown in Fig. 11.7(b). If an input is applied to either the winding on leg 1 or the winding on leg 2 in such a direction to reverse the flux in these legs then the flux in leg 3 will be reversed and an output winding on leg 3 will provide a signal for the *OR* function, Fig. 11.7(c). If both inputs are present then both legs 3 and 4 will switch so that an output winding on leg 4 will provide the *AND* function Fig. 11.7(d). By connecting these windings in opposition the EXCLUSIVE *OR* function may be obtained.

Thus outputs arise simultaneously with the inputs and this combined with the possibility of using large amplitude inputs to cause fast switching means that this type of device is inherently very much faster than a transfluxor in which the inputs are limited in amplitude and the outputs are the result of a drive pulse being applied at a later time than the input pulses.

The principles described above are capable of extension to more complicated structures and winding arrangements. The adder of Fig. 11.8 may be taken as an example. Here a six legged device

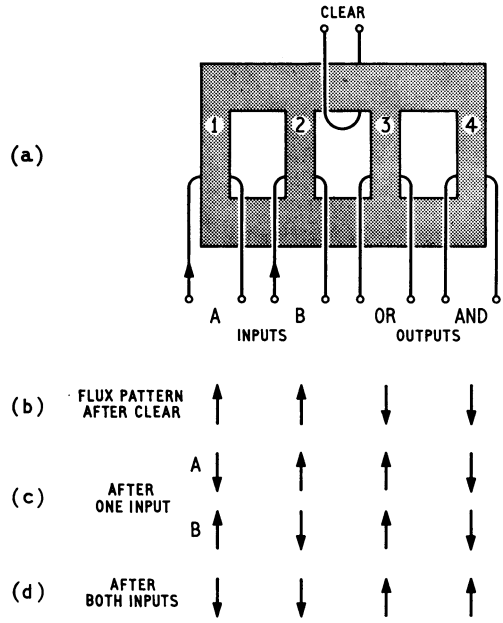

Fig. 11.7—Logical functions from four legged device

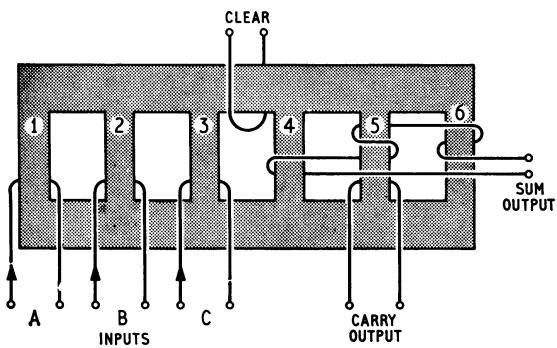

Fig. 11.8—Full adder using six legged device

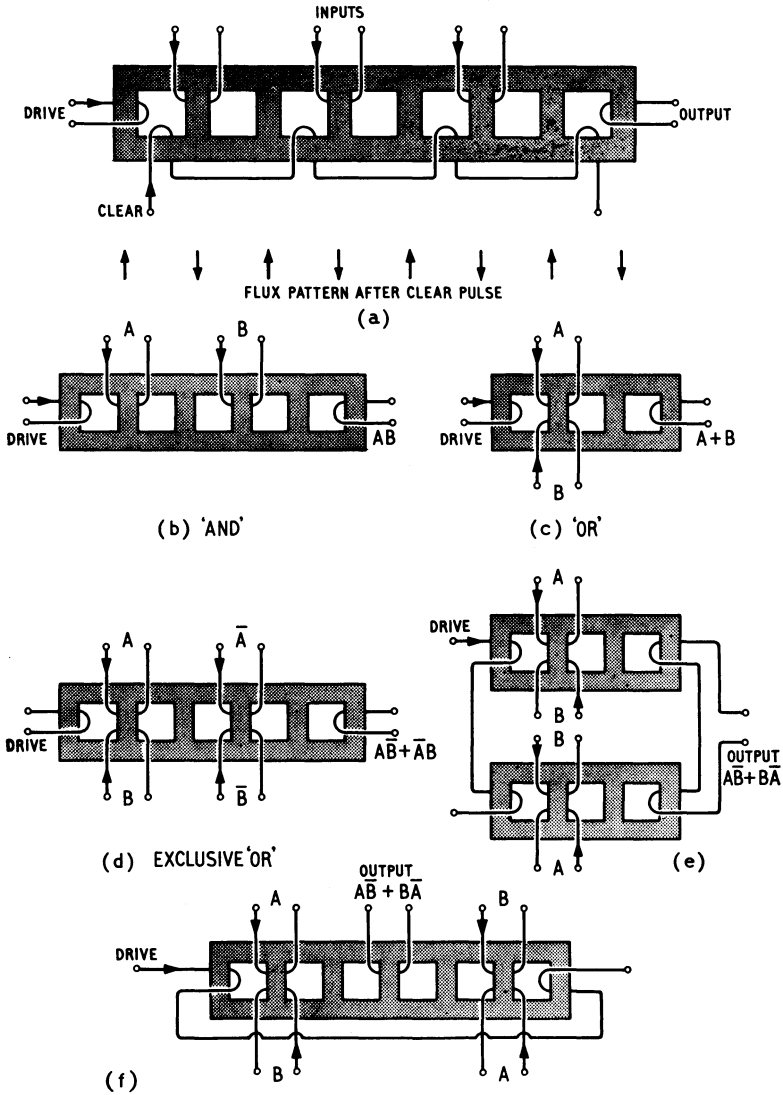

Fig. 11.9—The Laddic and some methods of operation

is used. If any two inputs are present the outputs in legs 4 and 5 oppose each other in the sum output winding but one or three inputs will cause an output to appear. If at least two inputs are present an output will result in the carry output winding which links leg 5.

One or two difficulties arise with this type of device. Firstly, the switching speed for a given input drive depends upon the length of the path in which the flux change takes place. Thus cancellation of outputs by connecting output windings in opposition is only partially effective. However, outputs can equally well be obtained during the reset operation when the element is returned to its original state and by using a distributed clear winding the switching speed of all paths can be arranged to be approximately equal. It may also be advantageous to make use of the reset outputs if several elements are connected together in order to synchronize input pulses arriving from other elements although the delay between setting and resetting adds to the time taken for the results to appear.

The second problem is the requirement that if more than one input pulse is present these pulses must overlap for a sufficient period for any switching which results to be completed otherwise input legs might act as return paths for other input legs. It is not, however, necessary for the beginning and end of different input pulses to be coincident.

The energy requirements for setting a core may be quite high but in the device shown in Fig. 11.9(a), which has been named the Laddic,[6] the input pulses are no longer used to set the core so that very little energy is required from these. Instead a separate clock pulse is used for setting and the function of an input is to hold a path leg in the saturated state so that the switched flux path is diverted to another leg. In the device shown the clear pulse sets the flux in odd numbered legs in an upward direction and that in even numbered legs in a downward direction. At a later time a drive pulse of sufficient amplitude applied to leg 1 will reverse the direction of saturation flux in this leg and, to complete the path, will also reverse the flux in the nearest leg in which a change is possible, i.e. the nearest even numbered leg which is receiving no input to hold it in saturation. If all inputs are energized the only other leg in which a flux change can take place is the leg furthest from leg 1 and around which is the output winding. Thus an output voltage on this winding provides the *AND* function for the

input signals, Fig. 11.9(b). An *OR* function can be derived by using more than one winding on each input leg as in Fig. 11.9(c). Functions involving negations can be obtained either by using double-sided logic where variables and their complements are available or by applying inputs in the opposite direction to that necessary for maintaining a leg in its saturated state so that the effect of other inputs on this leg is cancelled. Examples of these are shown in Figs. 11.9(d), (e), (f) for the EXCLUSIVE *OR* function. Fig. 11.9(e) also illustrates how an *OR* function may be derived by connecting the outputs of two elements in series and Fig. 11.9(f) makes use of an output winding on a leg other than one at the end. Many other winding arrangements may be used, if desired, including the connection of the output winding of one unit to an input winding of another.

For the basic arrangement shown in Fig. 11.9(a) the minimum input current needed to hold a leg in saturation decreases as the distance of the leg from leg 1 increases owing to the increase in switching path length. Also since the material is not perfectly square the application of an input will cause a small flux change in the output leg. This flux change will be larger for legs nearer to the output leg. Thus for optimum conditions the hold current for the input legs should decrease from left to right. However, if only single turn windings are employed for ease of manufacture, this is not always convenient although, even with all input currents equal to the minimum required for leg 2, an adequate signal to noise ratio can usually be obtained.[6]

Short, large amplitude drive pulses may be used in order to obtain fast operation. This, combined with the fact that the input and drive pulses are simultaneous, enables logical operations to be performed in a fraction of the time required in a transfluxor. In addition, this type of device appears to lend itself to the manufacture of a standard building block containing perhaps ten legs, each leg being provided with two windings apart from the reset winding. A block of this type could be used for a very large variety of operations by making external corrections as required. These advantages, combined with those mentioned at the beginning of the chapter, suggest that the Laddic or some similar element may well be a valuable component for use in the production of cheaper, more reliable computers.

Perhaps the most attractive feature of logic which uses these elements is the relatively small volume it occupies. This advantage,

combined with those mentioned at the beginning of the chapter, suggest that the Laddic or some similar element may well be a valuable component to use when a reliable system is needed for equipment in a restricted space.

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Chapter 12

COUNTERS AND PULSE DISTRIBUTERS

Circuits containing square-loop ferrite elements often provide a convenient method for various applications involving counting. As with the logical circuits described in Chapters 10 and 11 these circuits can offer the advantages of robustness, small size and weight, and low power consumption at low frequencies when compared with other methods. It is sometimes a serious disadvantage that, with a few exceptions using multi-apertured devices, no simple method exists for displaying the number held in such a counter. However, in many applications a dynamic indication that a certain count has been reached is all that is required.

12.1. Binary counters

A simple type of binary counter can be constructed by using transfer circuits similar to those described in Section 10.2. The general form of a single binary stage of this type is shown in Fig. 12.1. The two transfer circuits *A* and *B* are connected so that the output of one feeds the input of another. Provided that initially one core contains a " 1 " and the other a " 0 " then an input, which leads to the generation of an advance pulse, will cause the core which contains the " 1 " to be switched to the " 0 " state and by so doing inserts a " 1 " into the other core. By this means a " 1 " is transferred backwards and forwards between the two cores and an output from one core occurs for alternate inputs. The setting drive for one circuit must overlap the advance drive and exceed it in magnitude by an amount sufficient to switch the core. For this reason, and also the fact that energy would need to be provided from the first stage to switch succeeding stages, " loaded core " transfer circuits using only passive elements are not suitable for this type of counter. Transfer circuits of the

current routing type can be used but are rather complicated so that the best practical circuits are those using core-transistor combinations.

A typical binary counting stage using transistors and cores is shown in Fig. 12.2. Since regeneration is used for core switching only a short trigger pulse is required as the advance pulse to a stage and there is no difficulty in ensuring that a transistor output over-rides the effect of the advance pulse. Otherwise the circuit

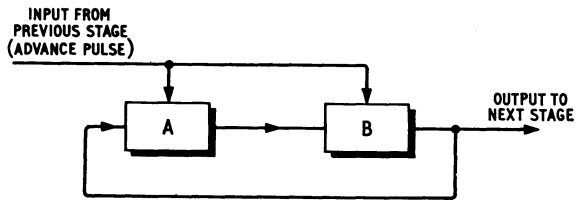

Fig. 12.1—General form of symmetrical binary stage

is similar to the core-transistor transfer circuit of Section 10.2. Four static states of which only two are used, are possible in a single binary stage of this type. A reset pulse of adequate length and amplitude is thus necessary to ensure that one and only one core contains a " 1 " before counting begins. This is not necessarily a disadvantage since most counters need to be set to a known initial state before use. Nevertheless, to avoid the possibility of a

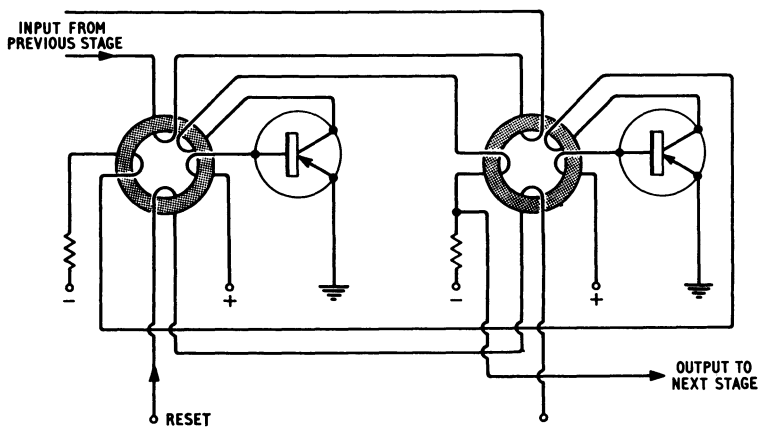

Fig. 12.2—Symmetrical core-transistor binary counter

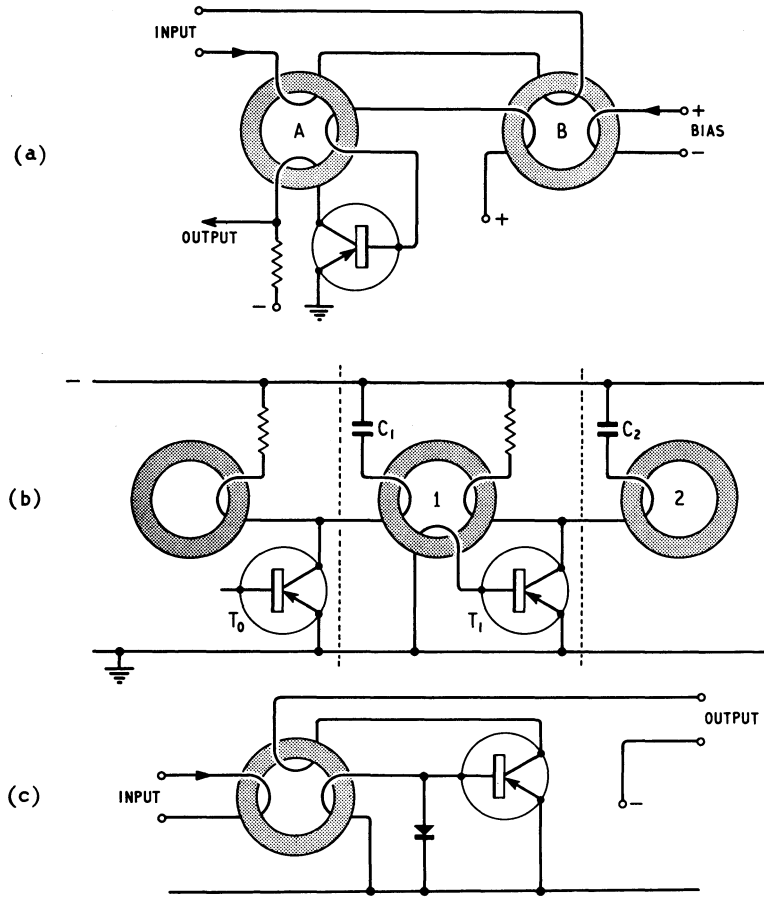

Fig. 12.3—Transistor-core binary counters

state arising which prevents any further counting action until a reset pulse arrives, various other circuits have been devised which are either only capable of existing in two states or are quickly returned to a usable state should an unusable state arise due to spurious pulses etc. These circuits are usually asymmetrical, i.e. not composed of two identical transfer circuits, and are often more economical in the use of components. Examples are shown in Figs. 12.3(a), (b) and (c). In the circuit[1] of Fig. 12.3(a) an input

pulse always switches core B and if A is already in the " 1 " state an output from core B turns on the transistor which drives core A to the " 0 " state over-riding the effect of the input on this core. The next input pulse will switch both cores but the output of core A is made larger than that of core B by using more turns on the output winding so that the transistor is not turned on and core A is left in the " 1 " state. Thus an output is obtained from the transistor for every other input pulse which is the requirement for a binary counting stage. The bias current on core B returns this core to the " 0 " state after every input.

The circuit[2] shown in Fig. 12.3(b) uses, in series with the input winding of a core, a condenser which is charged when the transistor conducts and discharges after the transistor has ceased to conduct. The current flowing during both operations is sufficient to switch a core. When an input arrives to transistor T_0 core 1 is switched to the " 1 " state if it was already in the " 0 " state. By this means C_1 is charged and transistor T_1 is brought into conduction to charge C_2 also. After core 1 has switched C_1 and C_2 discharge and the net effect on core 1 is zero since the discharging currents produce equal and opposite drives to this core. The next input again charges C_1 but does not switch core 1 since it is already in the " 1 " state so that C_2 is not charged. C_1 now switches core 1 back to the " 0 " state as it discharges and the cycle can be repeated. A filter can be incorporated in the output winding to minimize the effect of a " 0 " output on the following transistor.

Another approach[3] is illustrated in Fig. 12.3(c). Here use is made of the permeability at saturation to trigger the transistor sufficiently for regeneration to occur. If the core is already in the " 0 " state the input pulse drives it further into saturation and at the trailing edge provides a small output of the correct polarity to cause the transistor to conduct. Regeneration then produces further current so that the core is switched to the " 1 " state. The next input switches the core back to " 0 " and generates a positive voltage on the diode terminal attached to the base of the transistor. Hole storage in this diode then prevents a negative voltage from being applied to the transistor base at the trailing edge of the trigger pulse.

12.2. Ring counters

Counting in a scale other than binary, e.g. the scale of ten, can sometimes be accomplished by incorporating suitable feedback

loops in a counter composed of binary stages. It is usually more economical to use a ring counter, in which for example a " 1 " is circulated around ten cores, to provide a decade counter. These are also somewhat easier to design than the equivalent counter composed of binary stages with feedback.

Since only one core in each ring is being switched at any one time almost any of the transfer circuits described in Section 10.2

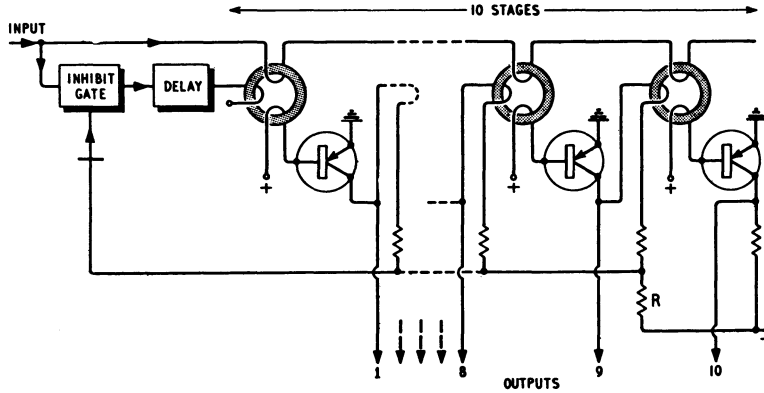

Fig. 12.4—Ten stage core-transistor pulse distributer

could be used as the basic circuit of the counter. If a " loaded core " type of circuit is used it is preferable to insert an amplifying stage between each ring to avoid the loading of one ring by another. This is an economical procedure in the case of a decade ring counter since the amount of equipment needed for the amplifiers would be small compared with the remainder of the circuits.

A core-transistor decade ring counter is relatively easy to design using the transfer circuit of Fig. 10.12. Since each ring contains only a single " 1 ", a " 1 " will not be written into a core from which a " 1 " is being read out so that, if the advance pulse is short, there is no necessity for two phases of advance pulse. A variation of this type of counter is shown in Fig. 12.4. Here the ring is not closed but consists of a succession of ten cores. Each input advances a " 1 " held in the counter and after a delay can produce a set pulse for the first core. This set pulse is inhibited by an output voltage from any of the first nine stages developed across the small resistor R if a " 1 " is being transferred in these stages. The circuit shown has the advantage over a ring that if an extra " 1 " should

accidentally be inserted it is quickly eliminated and if a " 1 " is lost it is immediately replaced. This feature is probably more important if the circuit is being used as a pulse distributer for supplying pulses sequentially to a number of output lines since it may then avoid the need for a reset pulse. One application for a pulse distributer of this type is the drive circuit for a cyclic store such as that described in Section 9.3. A two phase drive makes the delay in Fig. 12.4 unnecessary if only the opposite phase to that driving core 1 is used to produce the setting pulse for this core.

Another type of ring counter[4,5] uses the current routing technique described in Section 10.2 and is shown in Fig. 12.5. One phase of advance pulse links the odd numbered cores and the other

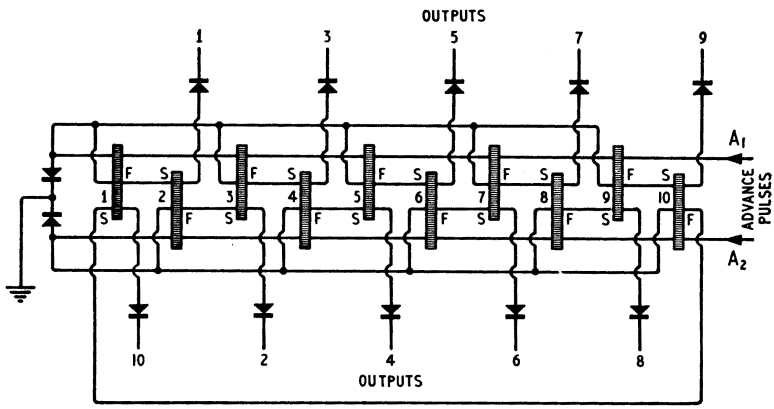

Fig. 12.5—Decade ring counter using current routing principle

the even numbered ones. A reset pulse on a separate winding, not shown in the diagram, initially sets core 1 to the " 1 " state and the remainder to the " 0 " state. The first advance pulse switches core 1 to " 0 " and the resultant output from the output winding, *F*, of core 1 causes the diode in this winding to be biased in a forward direction so that the advance current passes through this diode. The current also passes through the set winding, *S*, of core 2 to switch this core to the " 1 " state. Core 2 is reset and core 3 is set by the next advance pulse and so on until core 10 sets core 1 and the cycle is repeated. The outputs from the diodes may be taken to separate loads if required or the output lines may be taken to a common return lead. The output from the line

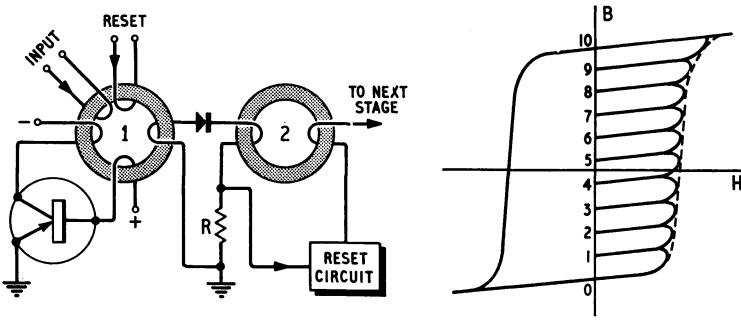

Fig. 12.6—Multi-level flux counter

linking the output winding of core 10 may be taken directly to another counter although some form of alternating switch is necessary in order to provide the two phases of advance pulse.

Multihole devices such as the transfluxor can also be used as ring counter elements. The use of transfluxors presents the possibility of displaying the contents of a counter. An extra hole can be used for deriving a non-destructive-output alternating current from a core containing a " 1 ". This current can then be used to light an indicating lamp.

12.3. Multi-level flux counters

In most of the applications previously described use has been made of only two of the remanent states of a toroidal core, namely the positive and negative saturation states, in order to store the binary digits " 1 " and " 0 ". There is no fundamental reason why intermediate remanent states should not be used to represent numbers so that a scale higher than binary can be handled but, in practice, the difficulties of inserting these states and discriminating between outputs would make such a system unreliable.

However, for counting purposes these objections are less valid since only one value of flux is inserted and an output is only required when one value of flux has been reached. The basic circuit[6,7] of such a counter is shown in Fig. 12.6. Core 2 is used to accumulate the count as illustrated by the hysteresis loops shown. For each input a fixed quantity of flux is switched in this core so that, after ten inputs in the case shown, the core is completely switched from negative to positive saturation. The remainder of the circuit is concerned with providing a reasonably constant flux change for each input, determining when the positive saturation state has been

reached, and resetting the core for the next cycle. The simplest method for causing a fixed amount of flux change for each input is achieved by applying across the input winding of core 2 a fixed voltage time integral. This can be obtained conveniently by completely switching another core, core 1, and using the output voltage of this core as the input voltage to core 2. In order to cope with a wide variety of trigger pulses it is preferable to make the drive to core 1 in the form of a regenerative circuit so that the output of this core is not substantially dependent on the trigger pulse. A reset pulse or a standing bias can be used to return core 1 to negative saturation. The number of outputs from core 1 needed to switch core 2 is determined mainly by the turns ratio of the windings on the coupling loop. Extra turns are required on the output winding of core 1 to allow for voltage drops in the diode and the resistor and for the reversible flux change in core 2 which may be a large fraction of the irreversible change if the flux steps are small. The resistor R is chosen so that its resistance is small compared with the input impedance of core 2 when flux is available for switching but large compared with the input impedance when saturation is reached. Thus the voltage across R indicates when saturation occurs and may be used as a trigger pulse for the reset drive circuit which returns core 2 to negative saturation. This reset pulse may also be used to trigger the next stage if two or more stages are in cascade.

The circuit is not particularly susceptible to ambient temperature changes since the rate of change of B_S with temperature is small at normal room temperature and in any case both cores are affected similarly. Temperature rises due to self generated heat are more serious since core 1 is switched more often than core 2 and will place an upper limit on the frequency. Storage cores are not normally selected for close tolerance on B_S so that for standard blocks cores must either be specially selected or some means must be incorporated for adjusting the quantity of flux transferred. The latter may be accomplished, for example, by a variable resistance in the coupling loop. A decade counter of this type is claimed to provide reliable operation.

A similar principle[8] may be used with the two holed device shown in Fig. 12.7. Windings through the small hole enable non-destructive read-out of the intermediate storage states to be obtained so that a continuous display of the state of the counter is possible. If the flux state of the core around the large hole is

progressively switched from saturation in one direction to saturation in the other by a similar method to that described above, then the transferable flux between legs *A* and *B* will increase from zero to a maximum when the core is half switched and fall again to zero when switching is complete. A constant voltage source may be used to transfer flux between the two legs so that the time for transfer indicates the quantity of transferable flux. By using a transfer circuit, such as a magnetically coupled multivibrator, it may be arranged that as soon as flux transfer has ceased in one direction it immediately begins again in the other direction and

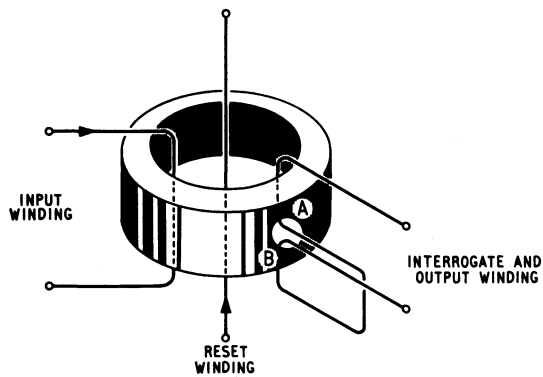

Fig. 12.7—Multi-level flux counter to provide count indication

under these conditions the frequency of the multi-vibrator will indicate the amount of transferable flux. Ambiguity will arise since the transferable flux rises to a maximum when the core is half switched. This might be overcome by using a three holed device similar to that shown in Fig. 7.4 and resetting the core to zero average flux by means of a wire through both small holes and then using only half of the total available flux swing for counting.

12.4. A multi-apertured pulse distributer

The multi-apertured device shown in Fig. 12.8 can be used to distribute a pulse sequentially to a number of output lines. The geometry is arranged so that a resetting pulse with a linear rise of current switches the legs in succession with constant time intervals between the peaks of the outputs. This time interval depends upon the rate of rise of current. For fast rise times the outputs

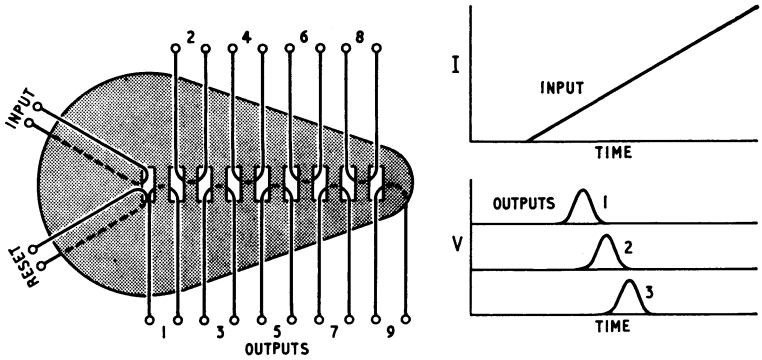

Fig. 12.8—Multi-apertured pulse distributer

overlap considerably owing to the switching time of the material but with a rise time of about 20 μsec in a twenty holed device a pulse has almost terminated before the next one begins if a fast switching material is used. All output pulses are approximately equal in amplitude. Although the outputs cannot be locked to clock pulses this element provides an economical and compact method for sequential pulse distribution when exact timing is not required.

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