PCLV11-J

MULTIFUNCTION UNIT

TECHNICAL MANUAL

WEBSTER
COMPUTER
CORPORATION

PCLV11-J MULTIFUNCTION UNIT

TECHNICAL MANUAL

Version 1.0

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CHAPTER 1
PCLV11-J General Description

GENERAL DESCRIPTION

The Webster PCLV11-J is a multifunctional unit, combining on one DEC-dual-sized board the following components :

(1) 4 enhanced serial lines
(2) a 16 Kbyte comprehensive bootstrap ROM
(3) a 45 Mbyte cartridge tape interface.

Qbus Interface

The PCLV11-J plugs directly into the Qbus. Originally introduced in 1975 by Digital Equipment Corporation to support the LSI-11 Qbus range, the Qbus architecture has evolved in speed and functionality to the point where it now outperforms most small computer bus systems. The PCLV11-J supports many current DEC Qbus enhancements, including 22-bit addressing and 4-level interrupt structure.

Programmable Configuration

The PCLV11 features per-line programmable baud rate, character length, parity, and stop bits. Many of the baud rates available with the DLV11 are rarely or never used, and so the PCLV11 provides options for these codes to permit access to newer, faster rates (19200 and 38400 baud).

Component Compatibility

The PCLV11-J bootstrap is functionally compatible with DEC's KDF11-B bootstrap, and the four serial lines with DEC's DLVJ1 (DLV11-J) type serial lines. The Cartridge Tape Interface is hardware and software compatible with the Cartridge Tape used in Webster SPECTRUM and PRISM computers, and is supported by an RT-11 handler (SC.SYS) which is program compatible with the DEC standard MM, MS and MT handlers.

Controls and Indicators

At the rear edge of the circuit board is a red LED indicator to signal board failure and a green LED to signal "Access in Progress". An output is provided for off-board indication of Access, and inputs are provided for optional "Write Protect" and "Online Control" switches.

COMPONENT FEATURES

1. Serial Lines

The unit provides four independent, full duplex, asynchronous RS232C serial line interfaces to the LSI-11 Qbus. Each line is separately programmable for baud rate (see Chapter 4), and variable character format. For the latter, the following options exist :

No. of data bits	: 7 or 8
No. of stop bits	: 1 or 2
Parity	: ODD, EVEN or NO PARITY

One serial line (line zero) is configurable as the computer console device interface, including halt or boot on received break.

2. Bootstrap

The PCLV11-J bootstrap features an EPROM with a large 16 Kbyte capacity, accessible by means of two banks of thirty-two 256-byte pages. These are made sequentially available via a Page Control Register through octal addresses 773000 to 773776 (standard DEC addresses for the boot) or, optionally, through addresses 771000 to 771776. This large capacity also accommodates diagnostic software (see appendix A) inherent in the design of PRISM and future SPECTRUM computers.

3. Cartridge Tape Interface

The PCLV11 provides a Cartridge tape interface which connects to cartridge drives conforming to the QIC-02 Industry Interface Standard. It is hardware and software compatible with the 450 foot, quarter-inch ANSI standard tape cartridges used in the SPECTRUM and PRISM computer series. These have a 45 Mbyte capacity and a 5 Mbyte per minute transfer rate.

CHAPTER 2
PCLV11-J Specifications

General Specifications

Bus Interface:	DEC Qbus
Qbus Loads:	1 DC, 1AC
Power Requirement:	5 Volt at 2.5amp; 12 Volt at 0.25amp
Physical Specifications:	132mm. x 219 mm.
On-board LED Indicators:	Green: Cartridge Tape Access in progress Red: Board Failure
TTL output:	Cartridge Tape Access in progress
TTL input:	Write Protect switch Online switch

Specifications - Serial Lines

Emulation:	DEC DLVJ1 4 Independent serial lines
CSR Base Address:	776500 or 776540 (Plug-selectable) Serial line zero selectable as console at 777560
Interrupt Vector:	300 or 340 (Address plug-selectable) Console: 60
Baud Rates:	50 to 38400 (Software programmable)
Data Format:	7 or 8 bits 1 or 2 stop bits Odd, even or no parity (Software programmable)
Terminal Interface:	RS232 Data Leads Only
Connector:	40-way Berg-style
Character Buffer:	Each receiver has a 4 character FIFO buffer, to reduce the risk of lost data

Specifications - Bootstrap

Hardware Compatibility:	KDF11-B (11-23+) Emulation
Bootstrap Address - PROM 1575W W0 option:	
	Low : 773000 - 773376
	High : 773400 - 773776
- PROM 1575W W1 option:	
	Low : 771000 - 771376
	High : 771400 - 771776
Page Control Register Address: 777520	
Capacity:	16 Kbyte 27128 PROM comprising two banks of:-
	16 pages of 256 bytes in low address range
	16 pages of 256 bytes in high address range
Software:	Self-test, Auto-bootstrap and Interactive modes

Specifications - Cartridge Tape Interface

CSR Base Address:	777340
Interrupt Vector:	214
Interface:	QIC-02
Front Panel Interface:	Inputs: Online, Write Protect switches
	Output: Access line
Connectors:	50-way Berg-style to Tape Drive
	10-way front panel connector
Data Transfer Mode:	22-bit address DMA transfer

CHAPTER 3
PCLV11-J Installation

3.1 Configuration Options

Miniature movable configuration plugs permit easy selection of base address, vector, break option and interrupt priority.

3.1.1 **Tape Cartridge** - No configuration possible; fixed addresses.

3.1.2 **Serial Lines**

Serial Line Address and Vector Assignments

Two option links on the MFU (N1 and N2) provide the following serial line addressing options :

	N2=0		N2=1		
LINE	ADDRESS	VECTOR	ADDRESS	VECTOR	
1	776500	300	776540	340	
2	776510	310	776550	350	
3	776520	320	776560	360	
0(N1=1)	776530	330	776570	370	
0(N1=0)	777560	60	777560	60	*Console option selected by N1

N.B. : See section 4.2 and Appendix A for information on programming the Baud Rate and other serial line parameters.

3.1.3 Bootstrap

The Bootstrap address is selected by PROM 1575W. Three different PROMs are available :-

PROM Option	Address
W0	773000 - 773776
W1	771000 - 771776
W2	No Bootstrap

3.1.4 Break Option
Configuration Plug (L1-L3)

Position: L1 Break received on console causes CPU halt
L2 No effect
L3 Break received on console causes CPU reboot

3.1.5 Interrupt Priority
Configuration Plugs (P1-P3)

P3,P2,P1:	Priority level:
000	4
001	5
010	6
110	7

3.2 Connector Pinouts

3.2.1 Tape Cartridge Interface

Connector Pinouts - Tape Cartridge (J1)

PIN	FUNCTION
2,4,6,8	Reserved
10	Reserved for host odd parity
12	Host bus bit 7
14	Host bus bit 6
16	Host bus bit 5
18	Host bus bit 4
20	Host bus bit 3
22	Host bus bit 2
24	Host bus bit 1
26	Host bus bit 0
28	Online
30	Request
32	Reset
34	Transfer
36	Acknowledge
38	Ready
40	Exception
42	Direction
44,46,48,50	Reserved

3.2.2 Serial Lines

Connector Pinouts - Serial Lines (J2)

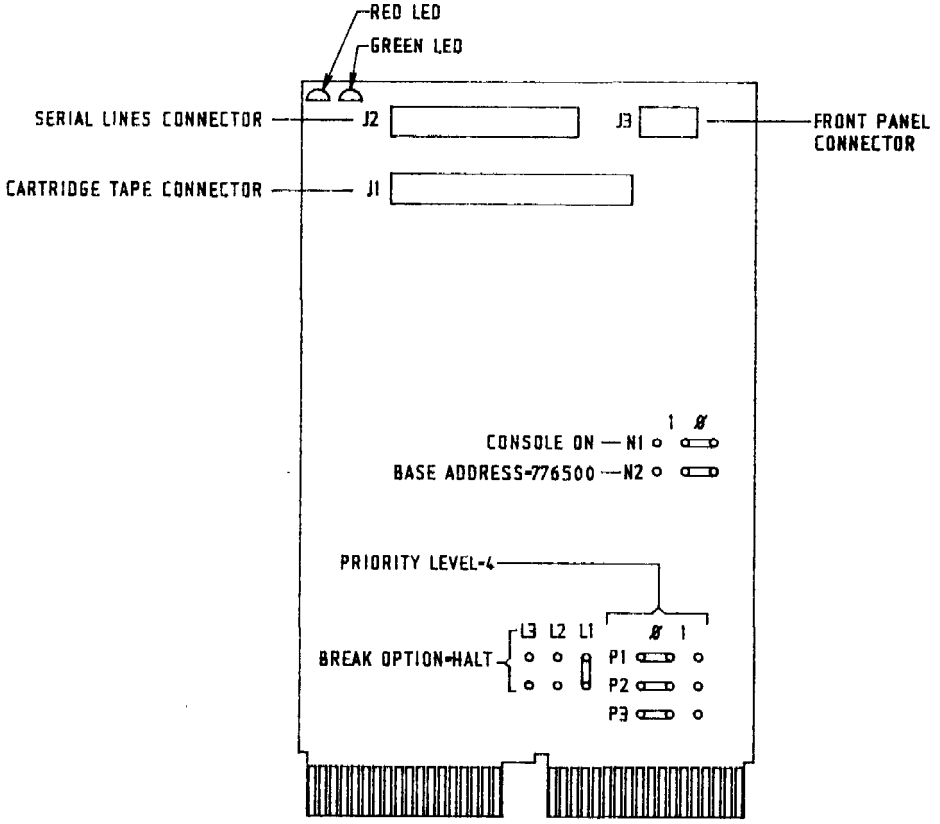
PIN	FUNCTION
2,5,8	Ground
3	Line 0 Transmit data
8	Line 0 Receive data
10	+12V.
12,15,19	Ground
13	Line 3 Transmit data
18	Line 3 Receive data
20	+12V.
22,25,29	Ground
23	Line 2 Transmit data
28	Line 2 Receive data
30	+12V.
32,35,39	Ground
33	Line 1 Transmit data
38	Line 1 Receive data
40	+12V.

3.2.3 Front Panel

Connector Pinouts - Front Panel (J3)

PIN	FUNCTION
1	Write Protect Input - Connect to Ground for Write Protect
2	Offline Input - Connect to Ground for Offline
3	ACCESS Output - Low TTL Signal indicates Drive Access

3.3 Jumper Plug Settings



3.4 Optional Accessories

The available accessories comprise :

LSPCLV/C Cartridge Control Cable
LSPCLV/L Serial Cable
SDBPCL RS232 Distribution Panel
SDKPCLV/F Support Software on RX01/RX02 single density diskette
SDKPCLV/C Support Software on Bootable QIC-02 Cartridge

3.4.1 Cartridge Control Cable

The Control Cable consists of a flat or twisted pair cable joining a 50-way displacement-type flat cable socket at the controller end, and a 50-way displacement-type flat cable PC edge connector at the drive end. The cable has a maximum length of 6 metres.

3.4.2 Serial Cable

The Serial Cable consists of a flat cable joining a 40-way displacement-type flat cable socket at the controller end, and four 10-way displacement-type flat cable sockets at the other end. These plug in to the 1574E/01 (or equivalent) RS232 distribution panel.

3.4.3 RS232 Distribution Panel

This consists of 4 DB25 male connectors on a board physically compatible with MICRO/PDP-11 I/O panel cutouts.

3.4.4 Software

Distribution Media :

a) Diskette, RX01/RX02 single density.

b) Cartridge tape (QJV13/U/S/MDC300XL - QIC-02), bootable.

For cartridge tape, an RT-11 run-time system is required and will be charged for, as the tape is distributed as a bootable RT-11 system.

Software modules distributed to support the PCLV11-J are :

* - CUTIL.SAV the cartridge diagnostic utility
** - SCINIT.SAV the cartridge tape initialization program
- SC.MAC driver handler for RT-11/TSX+ operating systems
- SC.RSX driver handler for RSX-11M+ operation systems
- SBRU.TSK the modified RSX-11M+ BRU utility
- SAVRES.SAV the Webster save/restore image mode utility
*** - SCBOOT.SAV the bootable tape generator
- SB.SYS the bootable device handler

*** CUTIL - Cartridge utility**

CUTIL is a diagnostic program for the cartridge tape drive. The following commands are supported:

A - Set transfer count. Default is one block (256 words).
B - Rewind cartridge to beginning of tape.
E - Write file mark.
F - Search forward and find next file mark.
G - Compare read and write buffers.
L - List, in ASCII, the number of bytes specified from the read buffer. (Defaults to forty bytes unless number length supplied.)
M - Move data from read to write buffer.
N - Select drive.
P - Position. Space forward one block.
R - Read a block.
S - Read status information.
U - Issue a reset.
W - Write a block.
X - Examine the specified register:
C1 command and status
WC transfer count
BA base address
BX base address extension
Y - Retension cartridge.
Z - Erase cartridge.

**** SCINIT - Cartridge Initializer**

This program initializes a cartridge, erasing the entire tape and writing a dummy file as the first file. An initialized cartridge has the format:

VOL1 HDR1 * dummy record * EOF1 * blank tape

with the dummy file having the name 'ZEROED.FIL' and a zero sequence number. This file will not appear on any directory of the cartridge. A cartridge must be initialized by SCINIT before it is first used otherwise errors will occur during read or write operations.

Note :

VOL1 :	ANSI volume label
HDR1 :	ANSI file header label
* :	File mark
EOF1 :	ANSI end of file label
blank tape:	Erased tape

***** SCBOOT - Bootable Cartridge Creator**

A bootable cartridge has the same format as a bootable magtape:

VOL1 SCBOOT HDR1 * disc image * EOF1 *

where SCBOOT is the soft boot handler. This bootstrap is created from the SB handler, which treats the cartridge as a file-structured device. The disc image is a file which contains a runnable RT-11 image, the SB.SYS special handler, and a bootstrap. The image is best created as a logical disc.

Device Handlers

SC:
The SC: device handler which emulates the DEC MT handler. SC.MAC is the device handler for RT-11/TSX+ operating systems and SC:RSX is the device handler for RSX-11M+ operating systems.

SB:
The SB: device handler allows the cartridge to be used as a read only random access device and enables RT-11 to be booted and run from a cartridge tape.

3.4.5 Creation of a Bootable Cartridge

An additional device handler (SB) has been provided to allow RT-11 to be booted and run from cartridge tape. A bootable cartridge tape is created as follows :
(NB assume master distribution RT-11 on device DK:)

First create a logical disc image of the required RT-11 system , including the SB.SYS handler.
a) create rt2.dsk/allocate:3000.
b) mount ld0 rt2
c) init/noq ld0:
d) copy/sys dk: ld0:

Put the SB handler's bootstrap in block zero on the logical disc as the primary boot.
e) copy/boot:SB ld0:rt11sj.sys ld0:

Load the cartridge tape into the drive and initialize it.
f) r scinit

Create the cartridge tape boot file SCBOOT.BOT. When SCBOOT.SAV executes, it requires the boot file (SCBOOT.BOT) be on device DK:. The SCBOOT.BOT file is created as follows:

Copy the RT-11 disc image to a file
g) copy dk:rt2.dsk dk:scboot.bot

Find the boot file's starting block number
h) dir/block scboot.bot

Delete the boot file. (You may have to unprotect it first.)
i) unpro scboot.bot
j) del scboot.bot

Recreate the boot file as a one block file containing the SB handler's bootstrap.
k) create scboot.bot/start:n./allocate:1
where n is the starting block number from step h.

Now create the bootable cartridge.
l) r scboot.sav and respond to the prompt with rt2.dsk

The system image file will be written to the cartridge, with the bootstrap file SCBOOT.BOT written as the second block. When the program finishes successfully, the following message will be displayed:

```
** The SC: Cartridge is now Hardware Bootable **
** The system image file is SC:SYSTEM.FIL     **
```

A bootable cartridge tape now exists.

CHAPTER 4
PCLV11-J Programming

The components of the PCLV11-J comprise the Cartridge tape interface, four serial lines, and the bootstrap.

This chapter discusses the internal registers of these components, and the function of each register bit.

4.1 Cartridge Tape Programming

The MFU controller contains four usable 16-bit device registers used to interface with the Cartridge Tape drive and Qbus. These registers are loaded and/or read under program control to initiate selected commands, and monitor subsystem status and error conditions. Device register bits are generally cleared by a Qbus Initialise (INIT).

With the exception of CTBAX, all registers must be written as words.

CARTRIDGE TAPE REGISTER ADDRESSES

REGISTER NAME	ADDRESS
CTCSR	777340
CTWC	777342
CTBA	777344
CTBAX	777346

Control Status Register (CTCSR)

BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				CON					RDY	IE	0	0	EXC	PE	WLE	NED
	F8	F7	F6	F5	F4	F3	F2	F1								
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W			R	R	R	R

CTCSR<00> - Non Existent Drive (NED)

Set when the front panel access button has been depressed, forcing the drive into an off-line condition.

CTCSR<01> - Write Lock Error (WLE)

When set, indicates that a Write data, Write File Mark, or Erase Tape command was issued while the front panel write protect button was depressed.

CTCSR<02> - Parity/Timeout Error (PE)

When set indicates that a Qbus parity or timeout error occurred during a DMA transfer.

CTCSR<03> - Exception (EXC)

Alerts the controller to a condition which has terminated the execution of a command. The only legal response to EXC being set is for the controller to issue a Read Status command and transfer all six status bytes.

EXC is set for an error condition or for two other conditions; whenever the drive reads a file mark or as the result of a power-up.

CTCSR<06> - Interrupt Enable (IE)

When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor under any of the following conditions:

(a) normal completion of any drive command.
(b) termination of a command due to an exception condition.
(c) termination of a command due to a parity error, writelock error, or non-existent drive error.

CTCSR<07> - Controller Ready (RDY)

Resets when a drive command is issued; sets when it is completed.

CTCSR<12> - Continue (CON)

When set, indicates that a further read or write is desired at the completion of a given Read Data or Write Data command. (Refer to explanations of "Read Data" and "Write Data" on the following pages.) It also indicates, when set, that the Drive's Select light is on.

CTCSR<08-15> - Drive Command Function Code (F1-F8)

All commands to the drive are single byte commands. The command byte has two fields. The three most significant bits (15, 14, 13) define the type of command; the five least significant bits (12, 11, 10, 09, 08) contain the command data.

The configuration of the command type field (Function bits F6-F8), allows the drive to respond to the following commands:

Command	F8	F7	F6	F5	F4	F3	F2	F1	Octal
Drive Select	0	0	0	*L	0	0	0	1	001
Position:									
Retension	0	0	1	0	0	1	0	0	044
Erase Tape	0	0	1	0	0	0	1	0	042
Rewind to BOT	0	0	1	0	0	0	0	1	041
Write Data	0	1	0	0	0	0	0	0	100
Write File Mark	0	1	1	0	0	0	0	0	140
Read Data	1	0	0	0	0	0	0	0	200
Read File Mark	1	0	1	0	0	0	0	0	240
Read Status	1	1	0	0	0	0	0	0	300

* Note : If L=0, the Drive's Select light will be off at BOT, and on otherwise.
L=1 is an "optional" command which causes the Drive's select light always to be on. (Select Drive, Lock Cartridge).

The drive will accept a command when RDY CTCSR<07> is set. If EXC is set, Read Status is the only command that will be accepted.

Select (001)

The Select command will have 000 in bits 15 through 13, and bits 12 through 08 set to 00001 to identify the drive as Drive 0. (Exception - see * note above). If a Select command is not issued after power-up/reset (following Read Status), the drive defaults to Drive 0.

Position (044, 042, 041)

The position command is used to perform one of the three following functions. This command will have 001 in bits 15 through 13, and either bit 08, 09 or 10 set to identify the function.

Retension (044)

The Retension command is used to re-tighten the tape. The drive will first bring the cartridge to BOT and then move the tape from BOT to EOT and back to BOT. Best results are obtained if a retensioning pass is used prior to writing, when excessive read errors are encountered, or prior to reading for hard tape errors.

Erase Tape (042)

The Erase Tape command is used to completely erase the cartridge. This command will cause the drive to rewind the tape to BOT, erase from BOT to EOT and then rewind the tape to BOT. During a normal write operation, the erase head is activated, erasing ahead of the write head for the full width of the tape. However if new data is written to a cartridge and that file is less than the length of track 0, old data may remain on the tape.

Rewind to BOT (041)

The Rewind to Beginning of Tape command permits the controller to position the tape prior to executing a Read or Write function. When a Rewind command is received, the drive will check if a cartridge is inserted. If a cartridge is not fully inserted, the command is aborted and EXC CTCSR<03> is set. At the completion of the Rewind command, if no abnormal condition exists, the controller will set RDY CTCSR<07>.

The drive will position the tape to BOT if the controller does not issue a Position command (Tension, Erase, Rewind) before a Read, Write, Read Filemark or Write Filemark command.

Write Data (100)

The Write Data command will have 010 in bits 15 through 13 and all zeros in bits 12 through 08. This command is used to write user data blocks to the tape. If a write operation is not preceded by a Select or Position command, the drive defaults to Drive 0 and BOT, Track 0. When a Write Data command is received and a tape is not inserted or WRITE PROTECT is activated, EXC CTCSR<03> or WLE CTCSR<01> are set.

If, at the end of a Write Data command, it is desired to write more data to tape, another write command should be issued with the continue bit set. (Ref. F5, CTCSR<12>.)

The controller can terminate a write operation by issuing a Write File Mark command after transmitting the last data block. The drive will stop accepting new data from the controller and then finish writing and read-checking the remaining data in its buffers before writing and read-checking a file mark.

Having issued a WFM command, the controller can resume writing and either issue another Write command, another WFM command, or return to BOT by issuing a Position command.

When the Early Warning Hole of the last track is detected, the drive will stop accepting new data from the controller on a 512 byte block boundary. The drive will then write and read-check the remaining data in its buffers, stop tape motion, and set EXC CTCSR<03>. The controller must respond with a Read Status command. The Status bytes inform the controller of the End of Media status.

When End of Media is reached, the controller may issue a Write command or WFM command. If a Write command is issued, two blocks of data will be accepted by the drive and the End of Tape procedure will be repeated. The controller should use these blocks to note that the file, if it is not complete, is continued on another cartridge. A file mark should be written after these blocks so that when the cartridge is read, the file mark will indicate that all the data was recovered.

Write File Mark (140)

The Write File Mark command will have 011 in bits 15 through 13, and all zeros in bits 12 through 08.
File marks can be used to separate data into smaller segments. When a drive is in a write mode, a Write File Mark command will terminate the write operation and the tape will not rewind to BOT.

A file mark is a full block of data consisting of a unique code that cannot appear in a user data field. The controller issues a WFM command but the drive creates the pattern.

Read Data (200)

The Read Data command will have 100 in bits 15 through 13 and all zeros in bits 12 through 08.
The Read Data command is used to read user data from tape. If no Position command was issued prior to a read operation, the drive will move the tape to BOT.
When a Read data command is issued and a cartridge is not completely inserted, the drive will assert EXC CTCSR<03> and abort the read operation.

If, at the end of a Read Data command, it is desired to read more data from tape, another Read Data command should be issued with the Continue bit set. (Ref. F5, CTCSR <12>.)

The drive terminates a read operation after reading a file mark, or after transferring a Block-In-Error (B.I.E.) when an irrecoverable read error occurs, or upon detecting erased tape. If the controller wishes to continue reading the next file after a file mark or the next data block after a B.I.E., it must issue another read command. If the B.I.E. was a file mark, the next block of data will be the first block of the next file.

During a read operation, the controller may issue a Read File Mark command. If the first few blocks of a file have been read during a read operation, and a user has determined that the required data is not in that file, a Read File Mark command will cause the tape drive to read to the next file mark without transferring data. Until a read operation is terminated, an RFM command is the only legal command that may be issued.

Read File Mark (240)

The Read File Mark (RFM) command will have 101 in bits 15 through 13, and all zeros in bits 12 through 08.

The RFM command is the same as a Read command except that no data is transferred. At each file mark, the drive sets EXC CTCSR<03> and informs the controller that a file mark has been found. If the controller is looking for a particular file, it must count the number of file marks found and re-issue RFM after each file mark.

Read Status Command (300)

The Read Status command will have 110 in bits 15 through 13, and all zeros in bits 12 through 08.

This command is used by the controller to request a status report from the drive. The controller must read status anytime the drive sets EXC CTCSR<03>, and should read status at the completion of a read or write operation to receive the error report for the operation and clear the error count in the drive.

The Word Count (CTWC) and Bus Address (CTBA) registers must be set up before the Read Status command is issued as the six drive status bytes are transferred in the same way as a normal data transfer. Each byte is copied to both the low and high byte of the word it occupies in memory.

CTWC Must be set to -6 (octal) prior to issuing the Read Status command.

CTBA Must be set to desired memory address where the 6 status bytes are to be transferred.

Status Bytes

Byte 0	Bit 7	Exception Byte 0
	Bit 6	Cartridge Not In Place
	Bit 5	Drive Not Online
	Bit 4	Write Protected
	Bit 3	End of Media
	Bit 2	Irrecoverable Data Error
	Bit 1	B.I.E. Not Located
	Bit 0	File Mark Detected

Byte 1	Bit 7	Exception Byte 1
	Bit 6	Illegal Command
	Bit 5	No Data Detected
	Bit 4	8 or More Read Retries
	Bit 3	Beginning of Media
	Bit 2	Reserved
	Bit 1	Reserved
	Bit 0	Reset/Power-up Occurred

Bytes 2 and 3	Write Operations	: Number of Blocks re-written
	Read Operations	: Number of Soft Read errors

Bytes 4 and 5	Write Operations	: Number of Write Underruns
	Read Operations	: Number of Read Underruns

The first two bytes (0 and 1) will define the condition that causes EXC (CTCSR Bit 03) to be set. In both bytes, the most significant bit will be set if any other bit in the byte is set. If bit 7 is not set, no other bit should be set.

Status Byte 0

Bit 7 - Exception byte 0, set if any other bit in the byte is set.

Bit 6*- Cartridge Not in Place, set if cartridge is not fully inserted into the drive.

Bit 5*- Drive Not Online, set if drive not physically connected to controller or not receiving power.

Bit 4*- Write Protect, set if the cartridge WRITE PROTECT is in file protect position.

Bit 3 - End of Media, set when logical Early Warning Hole of Track 3 is detected during a write operation and remains set as long as the drive is at logical End of Media. Will not be reset by a Read Status command, nor will it be set during a normal Read operation.

Bit 2 - Irrecoverable Data Error, set when drive experiences a hard error during read or write operations. After 16 retries to write/read block of data, bit is set and tape rewinds to BOT. Resets after the Read Status command.

Bit 1 - Block In Error Not Located, set when an Irrecoverable Data Error occurs and the drive cannot confirm that the last block transmitted was the Block In Error. Resets after the Read Status command.

Bit 0 - File Mark Detected, set when a file mark is detected during a read or RFM command. Read Status will cause this bit to reset.

* This error condition must be corrected before bit will reset.

Status Byte 1

Bit 7 - Exception Byte 1, set if any other bit in the byte is set.

Bit 6 - Illegal Command, set if any of the following occurs:

Select Command is issued with no drives or more than one drive selected.

Position Command is issued with no qualifier bits.

The drive is not online and a Write, Write File Mark, Read or Read File Mark command is issued.

A command other than Write or Write File Mark is issued during the execution of a Write command.

A command other than a Read File Mark is issued during the execution of a Read command.

De-selecting a drive when the tape cartridge is not at BOT, Track 0.

A Read Status command causes this bit (6) to reset.

Bit 5 - No Data Detected, set when an Irrecoverable Data Error occurred due to lack of recorded data. Absence of recorded data is the failure to detect a data block within a drive time out period (32 block times). Resets after a Read Status command.

Bit 4 - Eight or more Read Retries, set when 8 or more read retries required to recover a data block. (Indicates tape cartridge nearing end of life).

Bit 3 - Beginning of Media, set whenever tape is logically at the BOT, Track 0. As the tape moves away from beginning of tape, bit resets.

Bit 2 - Reserved

Bit 1 - Reserved

Bit 0 - Reset/Power-up Occurred, set after the controller receives signal from controller or drive is powered up. Reset by Read Status command.

Status Bytes 2 and 3

These two bytes will contain a 16 bit binary count of tape data errors. For write operations, this count increments for each data block that is rewritten due to read after write error. Byte 2 contains the MSB (most significant byte) and Byte 3 the LSB (least significant byte). The counter will increment twice for each error as the rewrite sequence rewrites two data blocks for each error.

Status Bytes 4 and 5

These two bytes will contain a 16 bit binary count of buffer underruns. Byte 4 contains the MSB and Byte 5 contains the LSB. For write operations this count increments each time the controller is unable to keep data flowing to the drive. If the drive is ready to write the next block, but a buffer is not full and ready to write, the drive will stop tape motion and wait for the controller.

During a read operation, the count increments when the controller is unable to empty the drive buffers fast enough. If an empty buffer is not available for the next block of data to be read from the tape, tape motion will stop.

Word Count Register (CTWC)

WORD COUNT															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Loaded with the 16-bit twos complement of the desired count of data words to be transferred to or from main memory. The register is incremented by 1 after each bus cycle and accommodates a maximum transfer of 65,536 words.

Bus Address Register (CTBA)

BUS ADDRESS															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Initially loaded with the low order 16 bits of the transfer address.

Bus Address Extension Register (CTBAX)

		BIT													
15		08	07	06	05										00
UNUSED			0	0	BUS ADDRESS										
					21	20	19	18	17	16					
					R/W	R/W	R/W	R/W	R/W	R/W					

Contains the memory address extension bits, which in conjunction with the low order address bits from CTBA, forms a 22-bit starting address for tape transfers.
In the above diagram, bits 0 through 5 represent the high-order 6 bits of the DMA address.
Bits 8 through 15 are unused, but a high-byte deposit to this register will invoke a hardware reset on the tape drive.

4.2 Serial Line Programming

SERIAL LINE REGISTERS (Four per line)

* See Section 3.1.2 for base address for each line.

RCSR	base address
RBUF	b.a.+2
TCSR	b.a.+4
TBUF	b.a.+6

Control and Status Registers (RCSR and TCSR)

These two registers contain ready status and interrupt control bits associated with their respective data buffers. The high bytes of both these registers are used for the programmable Communications Characteristics function.

Data Buffers (RBUF and TBUF)

The receive register provides quadruple-buffering in that three bytes of data can be held while another byte is entering or exitting. Data is handled in the low byte of the register. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF.

Receiver Control and Status Register (RCSR)

BIT 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BD RTE TBL	STP BIT	0	PTY INH	0	PTY	CHAR LENGTH		RDY	RCVR INT ENB	0	0	0	0	0	0
W	W		W		W	W		R	R/W						

RCSR<06> - Receiver Interrupt Enable (RCVR INT ENB)

When set, allows an interrupt sequence to start when RDY (RCSR<07>) sets. Cleared by INIT.

RCSR<07> - Ready (RDY)

Set when an entire character has been received and is ready for transfer to the processor. When set initiates an interrupt sequence provided RCVR INT ENB (RCSR<06>) is also set.

RCSR<09-08> - Character Length (CHAR LENGTH)

Bit Conformation :	00	01	10	11
Char Length :	5	6	7	8

RCSR<10> - Parity (PTY)

Set to 0 for even parity. Set to 1 for odd parity.

RCSR<12> - Parity inhibitor (PTY INH)

Set to 1 for no parity.

RCSR<14> - Number of Stop Bits (STP BIT)

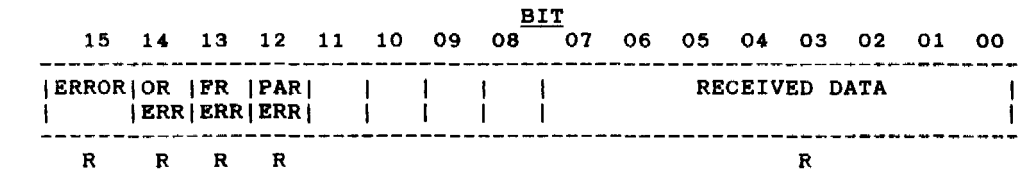
Set to 0 for 1 stop bit. Set to 1 for 2 stop bits.

RCSR<15> - Baud Rate Table Select (BD RTE TBL)
(Refer also to following section on Register TCSR bits 12-15).

This is implemented in RCSRs for serial lines 0 and 3 only.
This bit selects which of the DUART Baud Rate Tables is used.
The baud rate table bit in the RCSR for serial line 0 selects the table used for serial lines 0 and 2, and the baud rate table bit in the RCSE for serial line 3 selects the table used for serial lines 3 and 1.

NB : This register responds only to a high-byte (bits 15-08) write to the RCSR. It is all zeroes on read.

Receiver Data Buffer Register (RBUF)



RBUF<00-07> - RECEIVED DATA

These bits hold the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher or unused bits are read as zeros. Not cleared by INIT.

RBUF<12> - Parity Error (PAR ERR)

When set, indicates that parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Cleared by INIT.

RBUF<13> - Framing Error (FR ERR)

When set indicates that the character read had no valid stop bit. Cleared by INIT.

RBUF<14> - Overrun Error (OR ERR)

When set, indicates that the reading of the previously received character was not complemented (RCVR DONE RCSR<07> not cleared) prior to receiving a new character. Cleared by INIT.

RBUF<15> - Error Condition (ERROR)

Used to indicate that an error condition is present. This bit is the logical OR of RBUF<14>, <13> and <12>. Whenever one of these bits is set it causes RBUF<15> to set. This bit is not connected to the interrupt logic. Cleared by removing the error-producing condition.

Error indications are cleared by reading RBUF. INIT clears error bits.

Transmit Control and Status Register (TCSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PBR SEL 3	PBR SEL 2	PBR SEL 1	PBR SEL 0	PBR SEL ENB				XMIT RDY	XMIT INT ENB						XMIT BREAK
W	W	W	W	W				R	R/W						R/W

TCSR<00> - Transmit Break (XMIT BREAK)

When set, this bit transmits a continuous space to the external device. Cleared by INIT. When not set, normal character transmission can occur. This bit is not implemented for line 0, which is usually configured as the console.

TCSR<06> - Transmitter Interrupt Enable (XMIT INT ENB)

When set, allows an interrupt sequence to start when XMIT RDY TCSR<07> is set. Cleared by INIT.

TCSR<07> - Transmitter Ready (XMIT RDY)

This bit is set when the transmitter buffer XBUF can accept another character. When set it initiates an interrupt sequence provided XMIT INT ENB TCSR<06> is also set.

TCSR<11> - Programmable Baud Rate Enable (PBR SEL ENB)

This bit must be set to select a new baud rate indicated by TCSR<12-15>.

TCSR<12-15> - Programmable Baud Rate Select (PBR SEL)

When set, these bits choose a baud rate from 50-38400 as shown in the baud rate table on the following page. (Note that bit 15 in RCSR selects which table is to be used). Serial lines 0 and 2 use the same table, as do serial lines 3 and 1.

BAUD RATE SELECTION TABLE

PBR Bit 15	14	13	12	DLV11/E/F	PCLV11 ucode V.1 RCSR15=0	RCSR15=1	PCLV11 ucode >=V.2 RCSR15=0	RCSR15=1
0	0	0	0	50	50	75	50	75
0	0	0	1	75	110	110	50	75
0	0	1	0	110	134.5	134.5	110	110
0	0	1	1	134.5	200	150	134.5	134.5
0	1	0	0	150	300	300	200	150
0	1	0	1	300	600	600	300	300
0	1	1	0	600	1200	1200	600	600
0	1	1	1	1200	1050	2000	1200	1200
1	0	0	0	1800	2400	2400	1200	1200
1	0	0	1	2000	4800	4800	1050	2000
1	0	1	0	2400	7200	1800	2400	2400
1	0	1	1	3600	9600	9600	2400	2400
1	1	0	0	4800	38400	19200	4800	4800
1	1	0	1	7200	N/U	N/U	7200	1800
1	1	1	0	9600	N/U	N/U	9600	9600
1	1	1	1	19200	N/U	N/U	38400	19200

0 = program bit cleared
1 = program bit set
N/U = Not Used

Transmit Data Buffer Register (TBUF)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	TRANSMITTER DATA BUFFER							
								W							

TBUF<00-07> - TRANSMITTER DATA BUFFER

Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded right-justified.

Serial Line Configuration

The PCLV11-J module provides four RS232 DLVJ1-compatible serial line ports, one of which may be configured as the console. The programming requirements are identical for each port. Thus there is a total of 16 device registers (four per line) within this component of the MFU. Of these, the 4 pairs of control and status registers (RCSR and TCSR) are used to configure the ports. The high bytes of both these registers are used for the programmable Communications Characteristics function. The actual bit values were detailed in the previous pages. To illustrate this, consider the following examples : (Note that we will use the convention of programming the Receive CSR with a high-byte write (as it won't respond to a word write), and the transmit CSR with a word-write).

a) Required: Line 0- 9600 Baud, 8 data-bits, No parity, 1 Stop bit (format: 9600 8N1)
Assuming a Version 2 or greater MFU, the high-byte value for the TCSR is 11101000. This gives a word value of 160000. The value for the RCSR is 00010011, or 23 octal. Combining these two words gives a "configuration word" of 160023.

b) Required: Line 1- 300 7E2. 0101100001000011 = 054103

c) Required: Line 2- 19200 8N1 1111100010010011 = 174223.
Note that in this case, the required baud rate is in the RCSR15=1 column of the table, and thus the high (200) bit of the lower byte must be set.

d) Required: Line 3- 9600 8N1 1110100000010011 = 160023

The lower byte of each "configuration word" is then written into the high byte of each RCSR, and the higher byte is written into the high byte of each TCSR.

Configuration Hierarchy

1. The bootstrap PROM contains a table of default serial line configuration parameters in the last 4 words (8 bytes). These are in the exact format detailed in the previous examples, i.e. for 300 7E2 the word 054103 would be stored.

2. The bootstrap program in the EPROM also has the capability of using the console's Answerback Message for the line configuration function. See Appendix A for details on this.

3. After booting, a program can be run to change the settings. We provide the program "SETLIN.SAV" for this purpose under RT-11. Accessing the computer I/O page under RT11-XM, TSX+, RSX or RSTS/E is difficult and not supported (hence the provision of (2) above).

4. TSX+ V5.1 supports DLV11/E/F-compatible serial ports, and attempts to set up the baud rates during initialization. If this is not specified during the installation procedure, TSX+ programs all the lines to 50 Baud on a default of zero (see baud rate selection table). Therefore TSX+ V5.1 or greater must be generated with the SPEED parameter included in the line definitions.

4.3 Bootstrap Programming

Page Control Register (PCR)

PCR Address = 177520

BIT 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DIAG LED& BANK SEL				PSH 3	PSH 2	PSH 1	PSH 0	0	0	0	0	PSL 3	PSL 2	PSL 1	PSL 0
R/W				R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W

This register comprises two 8-bit bytes, is word- or byte-addressable and can be read from or written to. The Bank Select bit determines which one of the two 8K banks of the PROM is currently selected.
The low 4 bits of each byte are used to select a page between 0 and 15 (depending on the bit value) in one of two different places in the boot PROM (depending on the bus address). As each page comprises 256 bytes, this gives a total boot capacity of :

2 x 256 x 16 x 2 = 16384 bytes.

PCR<00-03> - Page Select Low (PSL0 to PSL3)

These bits select one of 16 256-byte pages in the boot PROM. The selected page is then accessible through boot locations 173000 - 173377.

PCR<08-11> - Page Select High (PSH0 to PSH3)

These bits also select one of 16 256-byte pages in the boot PROM. However, the selected page is then accessible through the higher boot locations 173400 - 173777.

PCR<15> - Diagnostic LED (DIAG LED)
- Bank Select <BANK SEL)

Setting this bit causes the diagnostic LED to light.
This bit is also used to select one of the two 8K banks of the EPROM. Setting the bit zero selects the lower 8K bank and setting the bit to one selects the high 8K bank.

CHAPTER 5
PCLV11-J Functional Description

This section describes the general operation of each principal section of the PCLV11.

5.1 System Clock Generator

Two clock signals SYSCLK (7.3728 MHz) and BCLK (3.6846 MHz)are generated by the 74LS321 oscillator chip at D2. BCLK is used by the two dual uarts (DUARTS) to generate the various transmit and receive baud rates. SYSCLK is used by the microprogrammed sequencer to step through the instructions in sequence.

5.2 Microprogrammed Sequencer

The heart of the sequencer is the Next Address PROM at G5. This PROM, like all the others in the sequencer, is a 512 x 8 fusible link PROM with an output register. The function of this PROM is to produce, at each positive edge of SYSCLK, the address of the next step of the routine currently being executed. The output from this PROM is the next address bus uA1 - uA8, which, combined with uA0, connects back to the inputs of the same PROM, so that at all times the PROM is using the current value of the next address bus to look up the next value to be placed on this bus.

The least significant bit of this bus, uA0, can be made to assume the state of any one of the 22 system signals which are connected to the inputs of the 8 input multiplexers K3, K4 and J4. These multiplexers are under the control of the sequencer, so that at any step of a sequence, any one of the 22 inputs to these chips can be connected to uA0, causing the next address to be conditionally odd or even, based on the selected input. This mechanism allows the sequencer to make decisions based on various system states, including Tape Data Alarm and ALU = zero, and then take the appropriate action. A permanently high input and a permanently low input to K4 allow for the more common situation where no conditional test is required.

Six other PROMs are connected to the next address bus, each producing eight output signals which control the rest of the logic on the board. The final PROM in the Sequencer, the P PROM at H5, has the task of determining which microprogram routine or sequence is executed next. It does this by decoding the 9 signals at its inputs into a starting address, which, under the control of the TRAP/ signal, is placed onto the next address bus. Once this starting address is recognised by the sequencer, i.e., one clock cycle later, the P PROM is switched off by the TRAP/ signal and the next address

PROM takes control and steps through to the end of the sequence. At this point the P PROM is re-enabled by the TRAP/ signal so that a new routine may be initiated.

5.3 Data Flow

Eight of the P PROM inputs are derived from Qbus signals so that the P PROM can recognise data transfer requests from the Qbus and initiate the appropriate microcode sequence to handle the request.

As an example, assume that the LSI-11 reads the Console Receiver Status Register in the PCLV11. First, the address of the Console RCSR appears on the Qbus data and address lines BDAL0L - BDAL15L. The W PROM at C6 decodes DAL3 - DAL12 and RBS7, and produces a four - bit output corresponding to the device being addressed. In the case of an access to the Console RCSR, the output is the number 11 Octal. This number, together with DAL0 - DAL2 is clocked into the 74LS374 at J5 by RSYNC. On receipt of BDINL, J5 will be enabled to drive the P PROM by the RDIN signal synchronized with the system clock by K5. The P PROM determines from these signals that either the Console CSR (device 11) or the Boot Prom (device 10) is being accessed, and prompts a microcode routine to handle the request. The ambiguity is resolved by the microcode routine, which examines the LSB of the device number, using the ID input to J4, and branches accordingly. This routine first loads register E2 from the data bus using the PAGE/ signal. The signals LINAD0 and LINAD1 select the appropriate half of the appropriate DUART for the Console operation. It then falls into a common routine (used by all 4 RCSRs) and has to choose between the options of DIN, DOUT, DOUTB lo-byte and DOUTB hi-byte. For this case (DIN) the routine extracts the RIE bit from bit 6 of register 10 in the RALU, and then reads the selected DUART using the RDN/! signal to get the RRDY bit. This data, after appropriate manipulation, is loaded into the Qbus transceivers D7 and C7 by the signal LDBRL/. Zero is loaded into B7 and A7 by LDBRM/ to complete the RCSR image.

The sequencer then asserts the TRPLY signal from the addressable latch at E6, which in turn drives the BRPLYL signal on the Qbus. When the LSI-11 sees BRPLYL active, it reads the data from the Qbus and then removes BDINL. When the RDIN signal goes off in the PCLV11 at Pin 3 of K4, the microcode routine deasserts TRPLY, completing the handshake.

A similar sequence of events occurs for a DOUT cycle from the LSI-11, but this time data is written from the Qbus into a PCLV11 register. The 16-bit Qbus data enters via the bus transceivers A7, B7, C7 and D7. The received data, DAL0 - DAL15 is multiplexed onto the internal data bus, D0 - D7, by the two tristate buffers A6 and B6 under the control of the sequencer outputs DAL/ and HILO/. Depending on the function being performed, the data can now be loaded into a DUART or into the ALU for further processing.

5.4 Arithmetic Logic Unit (ALU)

The 8-bit ALU, consisting of the two 2901C bit slice chips A4 and B4, is used primarily for emulating the register sets of the PCLV11 - in particular 4 sets of RSCR, RBUF, TCSR and TBUF registers for each of the serial lines, as well as registers MTCSR, MTWC, MTBA and MTBAX for the Cartridge controller, and the Boot PROM PCR. An image of all of these is maintained in internal storage in the ALU. It is updated when written to by the LSI-11 or by other events such as the Magtape or Duarts becoming ready.

5.5 Line Addressing

The ALU also maintains a pointer which is used by a microcode routine to scan each DUART in succession, looking for a change in status. The contents of this pointer are loaded by the PAGE/ signal into the 8-bit latch at E2. The two low order outputs of this latch, LINAD0 and LINAD1 determine which channel of which DUART is to be accessed.

5.6 Interrupt Logic

When the sequencer is not servicing a Qbus request it runs a number of background 'housekeeping' routines. One of these monitors the state of some bits in the Magtape and eight serial line CSRs, looking for the conditions necessary to generate an interrupt request to the LSI-11. If these conditions are found, eg. if TRDY and TIE are both set, the sequencer will store the appropriate interrupt vector (there are 19 possible) in an internal register and set the DEVIRQ/ signal from the addressable latch at E6. This will assert BIRQ4L, and, depending on the priority level configured by the P1 to P3 jumpers, may also assert BIRQ5L, BIRQ6L and/or BIRQ7L. The LSI-11 acknowledges this request by first asserting BDINL. Provided that there is no higher priority device requesting an interrupt, as determined by the I-PROM at J7, Pin 9 of J6 will go low. A short time later the LSI-11 sends the daisy-chained acknowledge signal BIACKOL. If Pin 9 of J6 is low the acknowledge signal is blocked by G7 Pin 13. The on-board signal IACKI at pin 4 on J6 allows it to be clocked on next SYSCLK edge, asserting the INTR! signal at J6 Pin 6. This INTR! signal is an input to the P PROM which starts up a microcode routine to handle the vector transfer phase of the interrupt cycle. This routine reads the interrupt vector from the internal register and loads it into the Qbus transmit register. The TRPLY signal is then set, and the Qbus handshake proceeds (as described earlier in paragraph 3, section 5.3) to complete the vector transfer.

5.7 RS232 Interface

The four RS232 serial data inputs, RX0 - RX3, are received by the RS232 receive chip A2. The outputs of this chip are connected directly to the receive inputs of the DUARTS R0 - R3. Within each DUART there are two separate channels operating entirely independently. Each channel converts incoming serial data into 8-bit bytes, which are then referred to an internal 4-character SILO. When requested by the LSI-11 reading one of the four receive buffer addresses, the output of the appropriate one of these 4 SILOs is enabled onto the Data bus D0 - D7. From here the characters, along with a status byte containing the Data Valid, Overrun, Framing and Parity Error bits, are transferred to the Qbus.

Serial transmit data from the DUARTs is buffered by the RS232 driver chip A1 to become TX0 - TX3. These RS232 drivers consist of NAND gates which are selectively enabled/disabled by the outputs of the upper half of latch E2. Under sequencer control, this latch reflects the state of the Break Control bits as written into the Transmit Control and Status Register (TCSR).

5.8 Cartridge Tape Interface

An 8-bit, bi-directional bus, HB0- to HB7-, is used to transfer all cartridge data, commands and status information.

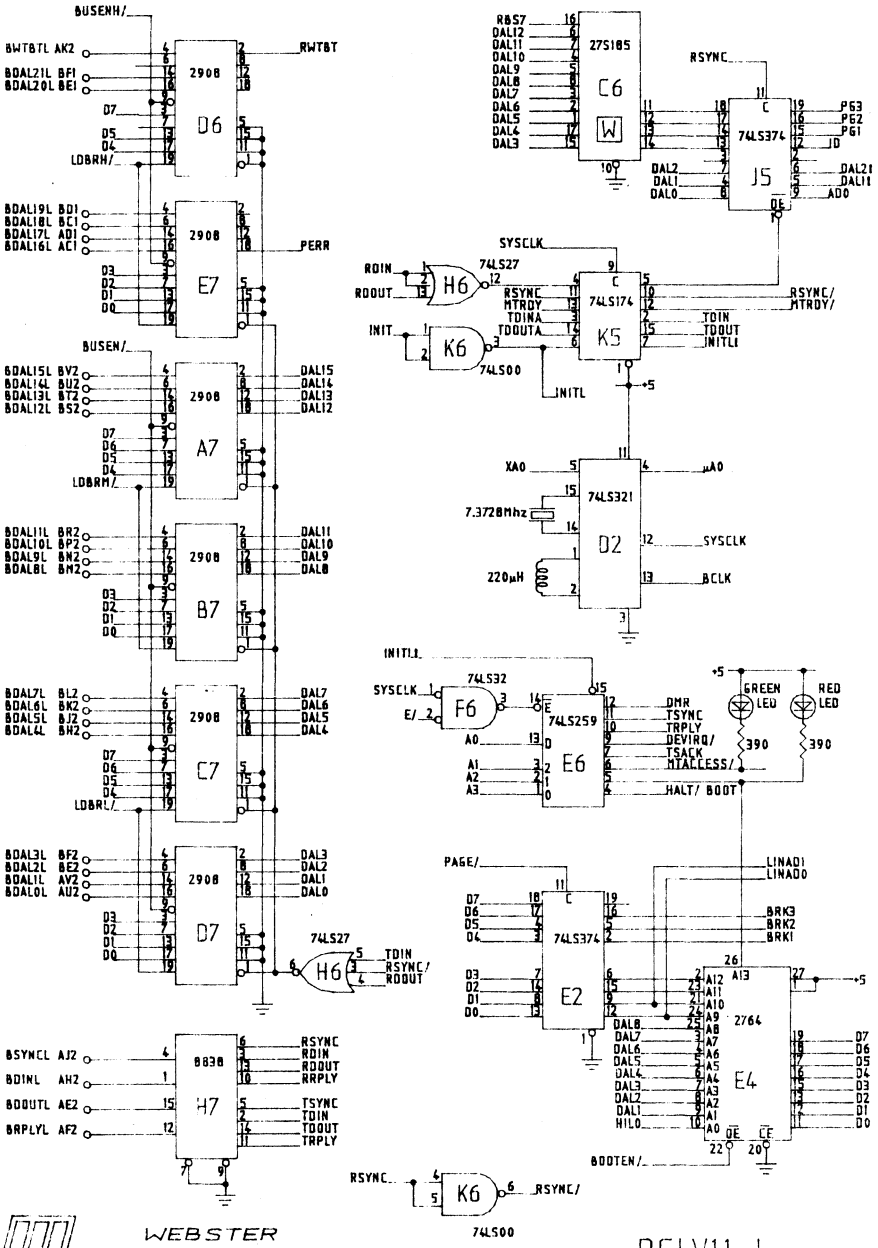
When the control signal DIR- is high, data flows from the PCLV11-J to the cartridge drive via the octal latch at F2. When DIR- is low, data flow is in the opposite direction via the octal buffer at G2.

Data transfer is controlled by a handshake protocol implemented by the signals XFER- and ACK-.
In the case of a Write operation, the PCLV11-J asserts the XFER- signal when it has loaded a byte of data into the latch at F2. When the drive detects the asserted state of the XFER- signal, it reads the data byte into its own buffer, then asserts the ACK- signal to inform the PCLV11-J that it can load the next byte. This sequence continues for each byte of data transferred. A similar protocol is observed in a read operation. The ACK- signal is used to clear the XFER- signal and to assert the MTDALARM signal which causes the microsequencer to execute its portion of the handshake protocol.

Commands are transferred to the drive using the same bus, but are strobed by the REQ- signal. This signal is derived from pin 9 of K2, and is cleared by the RDY- signal from the drive indicating that the command has been transferred.
The RDY- signal is also used to indicate completion of a command. It causes the MTRDY signal to be asserted and the microsequencer to act accordingly. MTRDY can also be asserted by the EXC- signal from the drive, indicating that a command has terminated unexpectedly.

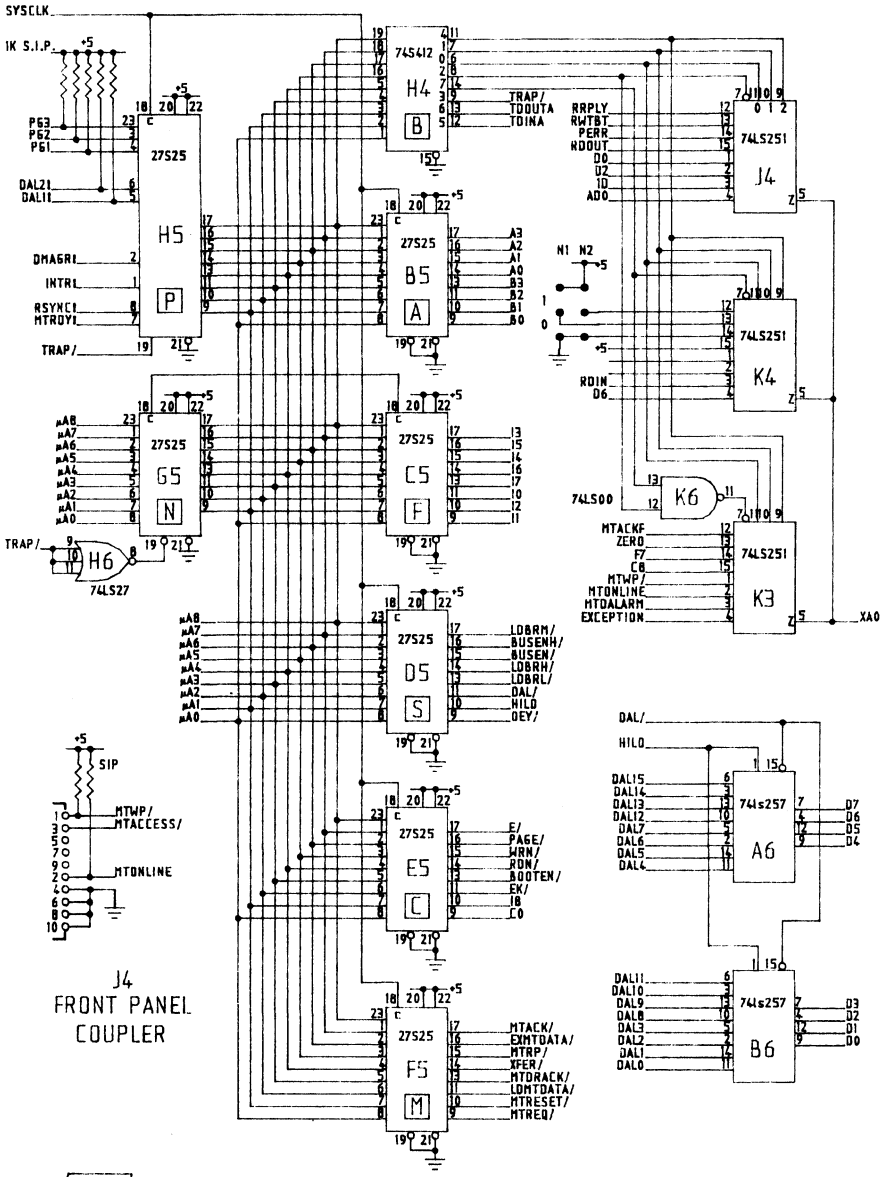
An alternate form of the REQ- signal is generated by pin 10 of J3, and is used in the transfer of status bytes from the drive to the PCLV11-J during a Read Status command.

Pin 6 of J3 generates the RST- signal which causes a power-up reset to occur in the drive.



WEBSTER COMPUTER CORPORATION

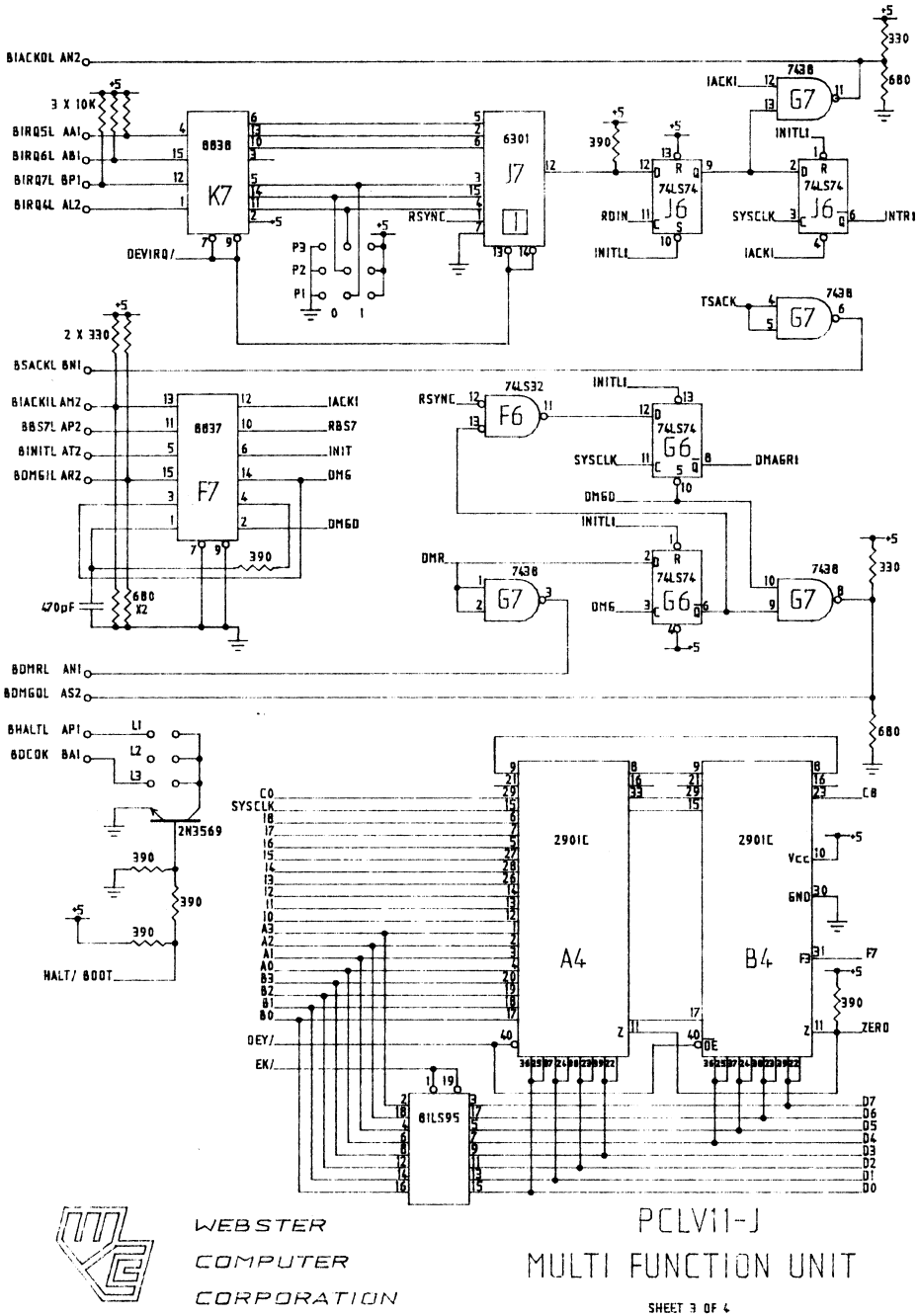
PCLV11-J
MULTI FUNCTION UNIT
SHEET 1 OF 4



WEBSTER COMPUTER CORPORATION

PCLV11-J
MULTI FUNCTION UNIT

SHEET 2 OF 4

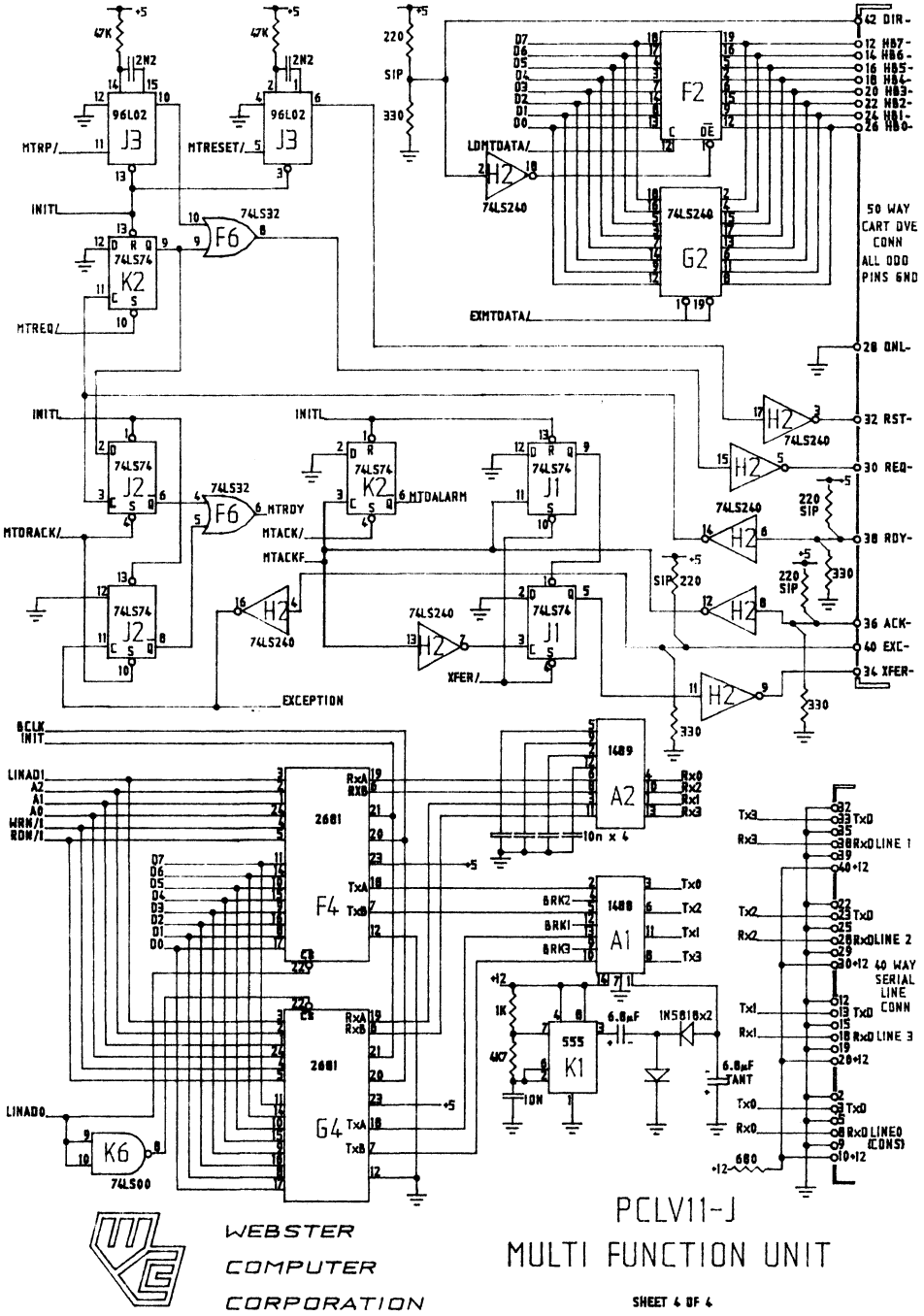


WEBSTER COMPUTER CORPORATION

PCLV11-J

MULTI FUNCTION UNIT

SHEET 3 OF 4


WEBSTER
COMPUTER
CORPORATION
PCLV11-J
MULTI FUNCTION UNIT
SHEET 4 OF 4
50 WAY
CART DVE
CONN
ALL ODD
PINS GND
40 WAY
SERIAL
LINE
CONN
LINE 1
LINE 2
LINE 3
LINE0
(CONS)

Appendix A
Bootstrap Information

Bootstrap Program Description

The bootstrap program dialogue normally consists of progress and error messages. It can run in one of 2 modes - Reports On or Reports Off. If reporting is enabled, many of the tests print informative messages advising details of system configuration, testing and errors. The normal mode is Reporting Off - (no news is good news). If a test produces a serious error, it enables reporting and then restarts the whole program; all reports will then be printed including the one that gave the error.
The functions of the V2.1. bootstrap are executed in the following sequence:-

1. Tests bank switching hardware.

2. Soft-senses V.1 or V.2 uCode and sets appropriate 9608N1 default.

3. Programs MFU lines at 777560, 776500-776520 from the PROM default serial line configuration table. If the table is unblown, uses 9608N1 default.

4. Executes quick memory test below 100000, then sets SP = 100000.

5. Prints "MFBoot V2.1.".

6. Tests the lower 64Kb of memory. Reports and halts if error.

7. Copies a loader into RAM at 600 and runs it.

8. Copies the 16Kb bootstrap into RAM starting at 1000, performs checksum function, and runs it.

9. Sets up all of vector memory (0-776) to point to a trap-table so as to report any unexpected or wrong interrupts.

10. Redetermines uCode level and sets appropriate table pointers.
There are 4 current versions of MFU microcode. The bootstrap senses the differences and prints :-
    ".1" for V.1 ucode with non-DLV11/E/F-compatible Baud Rate Table.
    ".2" for V.2 ucode with DLV11/E/F-compatible Baud Rate Table.
    ".4" for V.4 ucode with speed-improved cartridge code.
    ".6" for V.6 ucode with bug fixes to V.4

11. Enables interrupt on console. In the event of a Control/C being entered the Control/C Menu will display. See next section.

12. If checksum test failed (function 8), reports it and halts. (Type P to continue the boot).

13. Tests page control register (PCR), reports if failure.

14. Initializes and tests all memory management registers (only if memory management enabled).

15. Determines and prints processor type, options, memory size, and parity.

*16. Solicits an answerback from the console. (see section on Serial Line Configuration for details on valid formats). If not valid, then uses PROM default serial line configuration table. The PROM defaults are checked, and if invalid a message is printed to that effect. If the PROM is unblown or invalid, uses 9608N1.

*17. Checks for DY:, SC:, MS: and DU: controllers. Prints status (online or offline), and in the case of the DU: unit, the size of the disc in blocks and Mbytes, and sets the 1st. online device as the boot-device. (Note that the MS: test will not run if an MT controller is detected).

*18. Scans for all DLV type serial lines from 776500 and tests the CSR, interrupt vector and level. Scans and tests addresses 760000-760200 for SDZV11 muxs. If any duplication of interrupt vectors found, reports an error.

19. Tests all of memory above the bootstrap in RAM, up to 4Mb. If processor has parity support, then turns parity trapping on. If an error is detected, the address and data are printed and the CPU halts.

20. Tests line time clock, reports if not enabled.

21. Proceeds to boot device selected in step 17. If unable to boot from selected device (device not online or cleared by Control/C Menu), goes to the Bootstrap Menu.

* Any of the tests may be bypassed if bit set in exclusion word.

Control/C Menu

Entry to this menu clears the bootstrap program's selected boot device, allowing automatic entry to the bootstrap menu when all tests have been completed.

Option 1 : Reboot

Restarts the bootstrap program with full reporting enabled.

Option 2 : Diagnostic Menu

a) Serial Loopback Test. Loops all discovered DL and DZ lines to themselves and to the console to allow field maintenance testing. Upon exit, restarts bootstrap program. If section 16 (above) has been run, then the PCLV11 serial lines will be set up as per that section, and the SDZV11 lines will be set to 8 bits, no parity, 1 stop bit, with the baud rate being that assigned to PCLV11 serial line no. 3. (This allows this test to be run at other than 9600 baud).

b) Memory Test. Continuously run memory test. Upon exit, restarts bootstrap program.

c) Halt. Halts the CPU. This is useful for maintenance in machined which have the halt-on-break option disabled.

d) WOMBAT Disc Test. Calls a Webster field maintenance Utility resident within the disc controller. You must re-boot system to exit. Refer to the SRQD11 manual for instructions.

e) Computer I/O Map. Prints out a list of all responding addresses in the I/O page area, together with a "best guess" of what each range is. Note however, certain disc controllers with on-board "imitation" Bootstraps assume a read of their bootstrap addresses means a request to boot. They will thus read the 1st sector on the disc into memory at location zero, and will totally wreck the running program (this one). If this test crashes on your system, then don't run it.

Option 3 - Bootstrap Menu

Allows manual selection of device from which to boot. The menu prompts with a list of possible devices, together with their default CSRs, and an indication as to whether any device is responding to that address. The format of a legal response is :-

ddn<CR> or ddn@XXXXXX<CR>

where "dd" is a legal device name (selected from the list), "n" is the unit number, "@" is the "@" symbol and "XXXXXX" is an optional, alternate CSR address specified in octal.

Option 4 - Bootstrap Test Exclusion

The operator may exclude any bootstrap tests (see section below). Upon exit bootstrap program recommences.

Note: Entry of any character to the ^C Menu prompt other than 1 to 4 will exit from the menu and resume the interrupted operation.

Exclusion Byte

Because of the (remote) possibility of particular tests in the bootstrap interfering with particular hardware configurations, the Exclusion option in the Control C Menu may be implemented. This allows particular tests to be bypassed if they are found to cause trouble. As a slightly more permanent solution, the Exclusion Byte is implemented on the EPROM at address 37760 (20 octal addresses from the end). A bit value of 1 enables the test, while 0 disables it. Thus the PROM is overblowable.
The currently assigned bit values are :

1	AN	Exclude serial line configuration from Answerback Message
2	DL	Exclude DL serial line tests
4	DZ	Exclude DZ serial line tests
10	SC	Exclude cartridge tape check
20	MS	Exclude MS magtape check
40	DY	Exclude RX02 floppy disc check
100	DU	Exclude SRQD11 Winchester disc check

N.B. : Bit assignments in this byte are equivalent to those in Option 4 of the Control C Menu.

Serial Line Configuration

The bootstrap EPROM contains a table of default serial line configuration parameters in the last 4 words (8 bytes). These are in the exact format detailed in the examples in "Serial Line Configuration" in section 4.2., i.e. for 300 7E2 the word 054103 would be stored.

The bootstrap program in the EPROM also contains the capability of using the console's Answerback Message for the line configuration function. The Bootstrap program copies the values from this default serial line configuration table into the appropriate registers to initialize the ports. If the above table is not entered in the PROM, (normal state as supplied by Websters), then the bootstrap program recognizes the unburnt content (all ones) and supplies the appropriate registers with the bootstrap default values for 9600 8N1. If the values in the table are determined invalid by the bootstrap program an error message is displayed and the appropriate registers are supplied with the bootstrap default values for 9600 8N1.

For example, to set up the values specified in the previous example, the following bytes would be burnt into the PROM:

Address Octal	Address Hex	Line (Log)	Function	Example	Value Octal	Value Hex
37770	3FF8	0 (Con)	MODE	8N1	23	13
37771	3FF9	0 (Con)	BAUD	9600	350	E8
37772	3FFA	1	MODE	7N1	22	12
37773	3FFB	1	BAUD	300	130	58
37774	3FFC	2	MODE	8N1	23	13
37775	3FFD	2	BAUD	192	50	28
37776	3FFE	3	MODE	8N1	23	13
37777	3FFF	3	BAUD	9600	350	E8

Since most customers will not be able to burn a set of values into the PROM's default serial line configuration table, the bootstrap program supports setting up the ports by using the Answerback Message of the console terminal. The Bootstrap solicits the Answerback Message from the console, and then waits for a response. It will get a null, invalid or valid Answerback Message. Only in the case of the latter will it change the settings of the ports. The definition of a legal answerback message is <bbbnpsbbbnpsbbbnps>, where "bbb" refers to a baud rate description, "n" the number of data bits, "p" the parity, and "s" the number of stop bits. "n" can be 7 or 8, "s" can be 1 or 2, "p" can be O, E, N, o, e or n and the "bbb" is the first three letters of the required baud rate EXCEPT in the case of 50 and 75 baud where a leading zero is added. Valid examples are "050","075","300","120","960" and "192" for 50, 75, 300, 1200,9600 and 19200 baud respectively. Only 3 lines can be changed (the console cannot), and the descriptions for these are

butted up against each other to make the message. For example, setting lines 1, 2, and 3 to 1200 8N1, 19200 7E1 and 300 7O2 respectively would cause the Answerback Message to appear as <1208N11927E1300702>.

Note that there are four possible addressing configurations for the serial lines. Base address at 777600 or 777640 and console either enabled or disabled. The physical lines will be programmed as follows:

Address	Physical	Logical bbbnps Group
777560	Console	always 9600 8N1
776500	1	1
776510	2	2
776520	3	3
776530	4	3
776540	5	1
776550	6	2
776560	7	3
776570	8	3