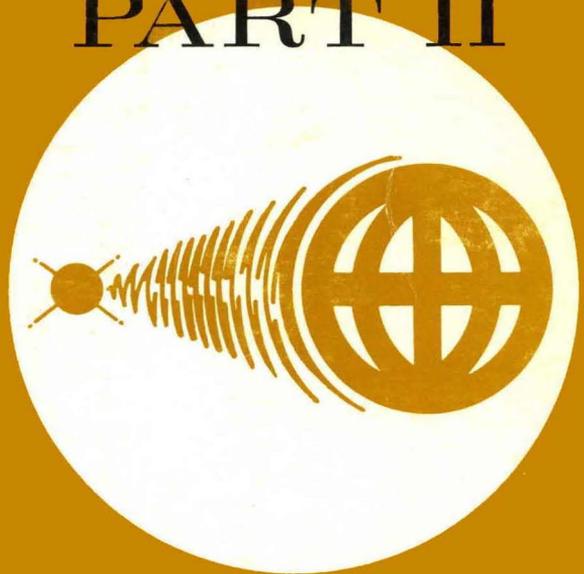


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# Communications HANDBOOK PART II



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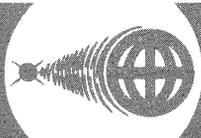
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# Communications Handbook

## PART II

Prepared by the Engineering Staff of  
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## Preface

Communications Handbook, Parts I and II, are the first two paperback volumes in the Texas Instruments Microlibrary. The objective of the Handbook is to give the communications circuit designer as much useful and current information as can be supplied in a work of 400 pages. Obviously, we cannot hope to present comprehensive coverage of the vast communications field; instead, we have tried to include material that has proved to be of current interest, as evidenced by reactions to papers delivered at Texas Instruments technical seminars, acceptance of our monthly Technical Newsletter, and requests from customers for special information.

New editions of the Handbook will be published periodically, to reflect improvements in design techniques and devices.

Please send any queries regarding material in this Handbook to the individual author, in care of Texas Instruments Incorporated, Post Office Box 5012, Dallas, Texas 75222.

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**AN/VRC-12 field radio, using TI transistors and diodes, was developed and is being produced by AVCO Electronics Division, Cincinnati, Ohio. (U.S. Army photograph)**

# Noise Characterization

by Bob Crawford

## INTRODUCTION

This chapter covers some of the general considerations involved in the design of low-noise linear amplifiers. The  $e_n$ ,  $i_n$  method and the direct NF method of characterizing or presenting noise performance are covered. A method of noise characterization for the  $1/f$  region is covered. The effect that correlation between generators has on NF is explained.

## NOISE CHARACTERIZATION

**$e_n$ ,  $i_n$  Method.** For noise considerations, any linear two-port network or amplifier may be characterized by a series noise-voltage generator and by a parallel noise-current generator at the input. Figure 1 shows a noisy amplifier together with its representation by a noiseless amplifier with  $e_n$  and  $i_n$  brought out front. The term  $\gamma$  indicates the amount of correlation between the two generators.  $R_{in}$  is the input resistance of the amplifier.

Measurement of  $e_n$  and  $i_n$  is straightforward. For measurement of  $e_n$ , the input terminals of the network must be short circuited with a resistor value ( $R_{short}$ ) that meets these two inequalities:

$$R_{short} \ll R_{in}$$

and

$$\frac{i_n R_{short}}{R_{in} + R_{short}} \ll \frac{e_n}{R_{in} + R_{short}}$$

The first condition assures that all of the generator voltage  $e_n$  will appear across the amplifier input. The second requirement limits the amount of signal current contributed by  $i_n$ . The output of the amplifier, as measured with a true-reading rms voltmeter, is divided by the gain of the amplifier to give the input series noise-voltage generator.

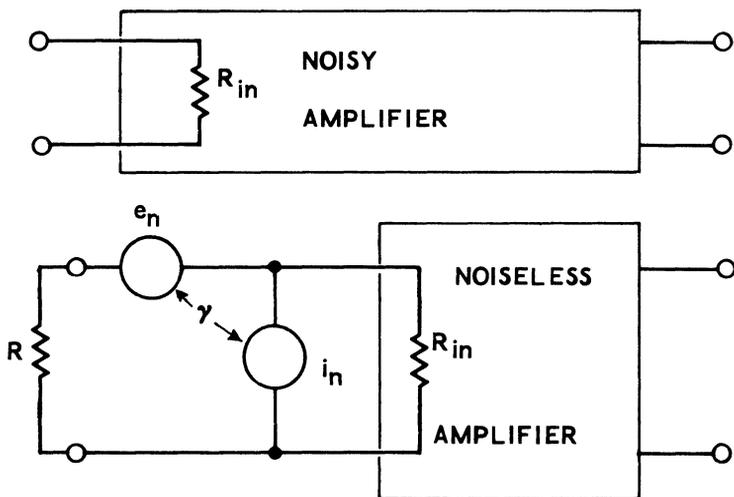


Figure 1

In the measurement of  $i_n$ , it is necessary to open-circuit the input of the amplifier with a resistor ( $R_{open}$ ) so the two following inequalities are met:

$$R_{open} \gg R_{in}$$

and

$$\frac{i_n R_{open}}{R_{in} + R_{open}} \gg \frac{e_n}{R_{in} + R_{open}}$$

It is necessary that the gain of the amplifier be high so that any noise introduced in the following stages will be small compared to the input noise.

Now, assuming  $e_n$  and  $i_n$  are known, the noise factor of the amplifier can be calculated. Defining noise factor as

$$F = \frac{\text{Total noise power output}}{\text{Power out due to the thermal noise generated by } R_g} \quad (1)$$

then by substituting  $e_n$  and  $i_n$  into Eq. (1), an expression for noise factor is derived:

$$F = 1 + \frac{1}{4kT\Delta F} \left( i_n^2 R_g + \frac{e_n^2}{R_g} + 2\gamma e_n i_n \right) \quad (2)$$

where

$k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  Joules/ $^\circ K$

$T$  = temperature in degrees Kelvin =  $273 + ^\circ C$

$\Delta F$  = noise power bandwidth

$\gamma$  = correlation coefficient

$4kT = 1.66 \times 10^{-20}$  watt-seconds at  $25^\circ C$

Note that Eq. (2) is independent of  $R_{in}$  because it is a noiseless resistor. The input resistance for a common-emitter stage is approximately  $h_{fe} r_e$ . Because  $r_e$  is not a real resistance it generates no thermal noise. Any noise generator within the emitter junction has already been taken into account by the two noise generators.

Since  $F$  is a function of the generator resistance,  $R_g$  may be varied to find the minimum (or optimum) noise factor. This may be done in one of two ways:

(1)  $F$  may be differentiated with respect to  $R_g$ . The result is then set equal to zero. Solving for  $R_g$  will yield an optimum value of source resistance,  $R_{(opt)}$ . Substituting  $R_{(opt)}$  into the general equation for noise factor yields the minimum noise factor (for a given bias level).

(2) The minimum noise factor occurs when each generator contributes equally to the total noise power. Looking at the first two terms within the parentheses of Eq. (2), it is noted these have the dimensions of power. Setting these two terms equal and solving for  $R_g$  yields the optimum generator resistance:

$$R_{(opt)} = \frac{e_n}{i_n} \tag{3}$$

Substituting Eq. (3) into Eq. (2) yields the minimum or optimum noise factor obtainable,  $F_{(opt)}$ .

$$F_{(opt)} = 1 + (1 + \gamma) \frac{e_n i_n}{2kT\Delta F} \tag{4}$$

Note that  $F_{(opt)}$  depends upon the product of  $e_n$  and  $i_n$ , while  $R_{(opt)}$  depends upon the ratio of  $e_n$  and  $i_n$ . The dependency of NF upon  $R_g$  can be seen in Fig. 2. Figure 2a is for a conventional transistor while Fig. 2b is for a field-effect transistor. Notice the lower current levels at which the 2N930 is run and the higher optimum source resistance for the 2N2500. Figure 2a also gives typical values for the  $e_n$  and  $i_n$  generators for the 2N930.

The quantities  $e_n$  and  $i_n$  are functions of  $I_E$  and therefore  $F$  is valid only at the bias condition at which  $e_n$  and  $i_n$  are measured. These two generators are fairly independent of collector voltage for voltages below six to ten volts.

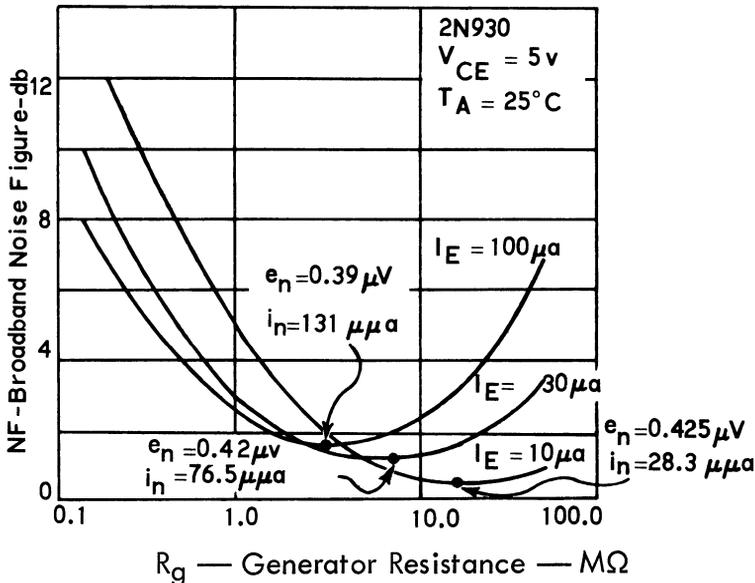


Figure 2a

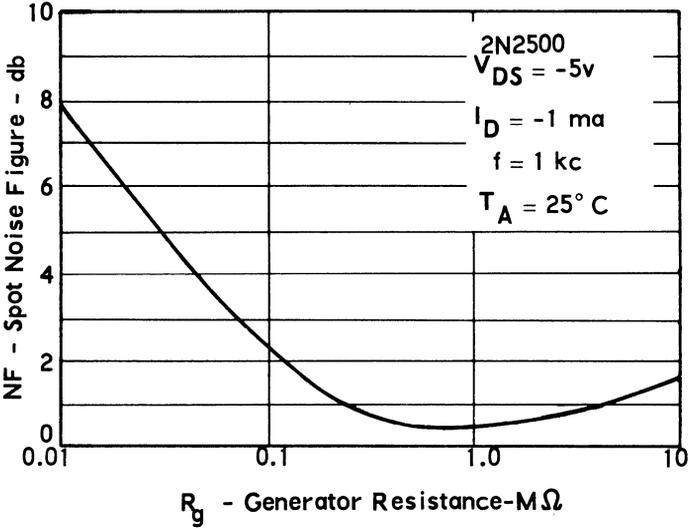


Figure 2b

Equation (4) states that, for a low noise factor,  $\gamma$  should be as small as possible. The significance of the correlation factor and its effect in a circuit can best be explained by an example where two generators are in series across a load (Fig. 3), each with an rms amplitude of  $a$ . The two extreme cases of  $\gamma$  will be examined. In the first case, let the two generators be of differing and randomly related frequencies, i.e., no correlation ( $\gamma = 0$ ); while in the second case,  $\gamma =$  unity, i.e., the generators have identical frequencies and phase. With  $\gamma = 0$ , the two voltage vectors add in quadrature, so that power into  $R$  is proportional to  $a^2 + a^2 = 2a^2$ . When  $\gamma = 1$ , the two generators are of the same frequency and exactly in phase. Their amplitudes can be added directly, that is, power into  $R$  is proportional to the quantity  $(a + a)^2 = 4a^2$ . Taking the ratio of the two cases where  $\gamma = 1$  and 0, the power output in the first case is twice that of the second case.

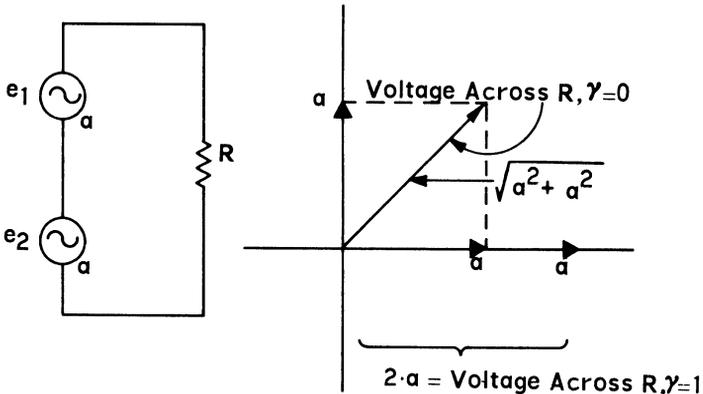


Figure 3

**Considerations<sup>1\*</sup> of  $\gamma$ .** Since  $F$  depends upon  $\gamma$ , it will be interesting to investigate the dependency of the correlation coefficient upon transistor parameters. Noise factor as a function of  $\gamma$ ,  $e_n$  and  $i_n$  has already been described in Eq. (2). Noise factor in terms of transistor parameters has been given in the literature by Nielson<sup>2</sup>, and is presented below:

$$F = 1 + \frac{r'_b}{R_g} + \frac{r_e}{2R_g} + \frac{(r'_b + r_e + R_G)^2}{2\alpha_o^2 R_g r_e h_{FE}} \tag{5}$$

Equating Eq. (5) to Eq. (2) and letting  $R_g \rightarrow 0$ , and  $R_g \rightarrow \infty$ , yields values for  $e_n$  and  $i_n$ , respectively. These values are given in the following two equations:

$$e_n^2 = 4kT\Delta f \left[ r'_b + \frac{r_e}{2} + \frac{(r_e + r'_b)^2}{2\alpha_o^2 r_e h_{FE}} \right] \tag{6}$$

$$i_n^2 = \frac{2kT\Delta f}{\alpha_o^2 r_e h_{FE}} \tag{7}$$

Substituting these values into Eq. (2) and solving for  $\gamma$ :

$$\gamma = \frac{\frac{r'_b}{r_e} + 1}{\sqrt{\left(\frac{r'_b}{r_e} + \frac{1}{2}\right) (2\alpha_o^2 h_{FE}) + \left(\frac{r'_b}{r_e} + 1\right)^2}} \tag{8}$$

In Fig. 4,  $\gamma$  is plotted as a function of  $h_{FE}$  with  $r'_b/r_e$  as a running parameter to describe a family of curves. At low emitter currents,  $r_e \gg r'_b$ , and  $\gamma$  reduces to:

$$\gamma \cong \frac{1}{\sqrt{h_{FE}}}$$

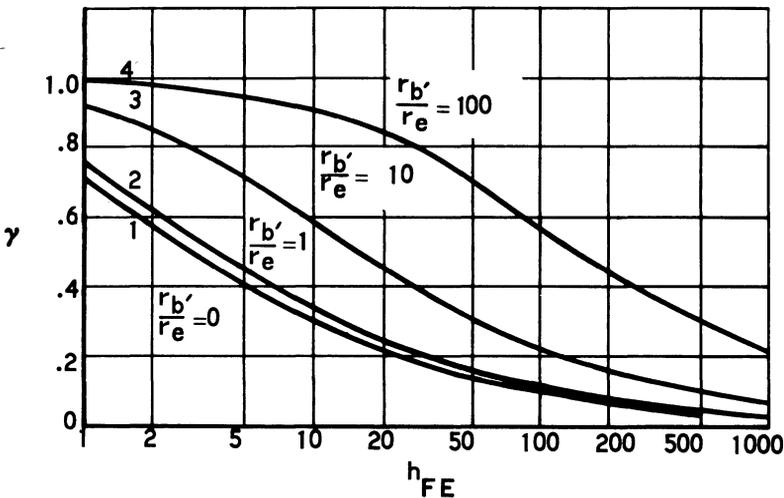


Figure 4

\*Superscript numbers refer to bibliography entries at end of chapter.

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Thus for large values of current gain,  $\gamma$  can be very small. Curves 1 and 2 of Fig. 4 would apply to most of the situations where a transistor is biased for low-noise operation. For current gain  $> 100$ ,  $\gamma < 0.1$ . The following table will serve to illustrate the effect that  $\gamma$  has upon NF.

**Table 1**

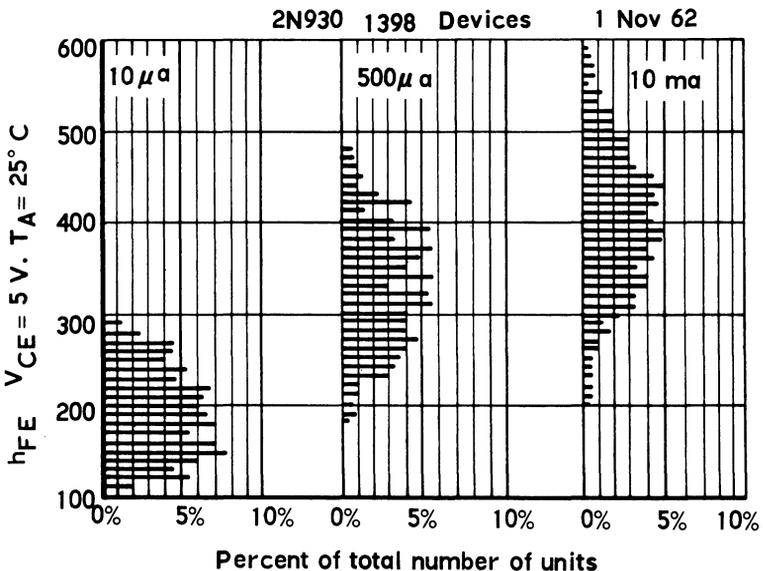
	NF	F
$\gamma = 0$	1.5 db	1.41
$\gamma = 0.1$	1.62 db	1.45
$\gamma = 1.0$	2.64 db	1.82

It is obvious from the curve of Fig. 4 that a high current gain device is desirable for low-noise operation. Figure 5 shows the distribution of 1398 2N930's at three different current levels. Notice the very high  $h_{FE}$ , averaging around 200 (even at  $10 \mu a$ ).

**NF Measurement.** The following measurement in the audio range is one of the easiest noise measurements to make. It lends itself to the testing of large quantities of transistors. Once the measurement system has been set up, no calculations are necessary and NF is read directly.

The fundamental principle of this method lies with the basic definition of noise figure in Eq. (9):

$$NF = 10 \log_{10} \frac{\frac{S_{p \text{ in}}}{N_{p \text{ in}}}}{\frac{S_{p \text{ out}}}{N_{p \text{ out}}}} \quad (9)$$



**Figure 5**

where  $S_{p \text{ in}}$  = Signal power in  
 $N_{p \text{ in}}$  = Noise power in  
 $S_{p \text{ out}}$  = Signal power out  
 $N_{p \text{ out}}$  = Noise power out

Since each signal and its associated noise work into the same load, the expression for NF can be written in terms of voltage rather than absolute power.

$$NF = 20 \log_{10} \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}} \tag{10}$$

where  $S_i$  = Signal voltage in  
 $N_i$  = Noise voltage in  
 $S_o$  = Signal voltage out  
 $N_o$  = Noise voltage out

Equation (10) can be written in the following form:

$$NF = 20 \log \frac{S_{in}}{N_{in}} - 20 \log \frac{S_o}{N_o} \tag{11}$$

If the source resistance  $R_g$  is known, then the input noise to the amplifier can be calculated by the relationship  $N_i = \sqrt{4kT\Delta fR_g}$ . By setting the input signal 10 times greater than the input noise, the first term on the right side of the equation reduces to 20 db.

$$NF = 20 \text{ db} - 20 \log \frac{S_o}{N_o} \tag{12}$$

With a noiseless amplifier, the second term would also be 20 db, indicating that the noise figure of the amplifier is zero. In an actual amplifier, the second term will be something less than 20 db — say, 19 db — making the amplifier NF = 1 db.

Figure 6 shows a test set-up for the described noise measurement. The audio oscillator at the input supplies a signal ten times greater than the input noise produced by  $R_g$ . Depending upon the amount of available power gain or the output signal level of the network *under test*, the low-noise amplifier may or may not be needed. The bandwidth is set by the filter. Potentiometer  $R_1$  allows the VTVM to be adjusted to a convenient zero point (or varies the system gain). Output levels are observed with an oscilloscope to be sure that no clipping or stray 60-cycle pickup occurs within the circuit.

A step-by-step procedure for measuring noise figure is as follows:

1. Calculate input-noise voltage.  $N_i = \sqrt{4kT\Delta fR_g}$ .
2. Set signal level equal to ten times (20 db) the noise level.
3. Adjust  $R_1$  so that the VTVM reads 10 db on some convenient scale.
4. Reduce the input signal to zero and note how many db the meter falls.
5. Subtract the meter drop (in db) from 20 db to obtain the NF of the amplifier.

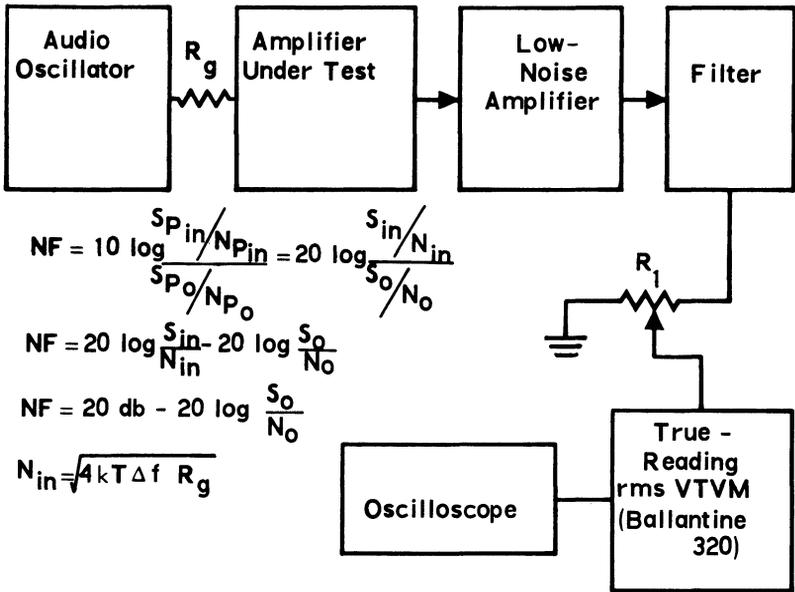


Figure 6

Referring to Eq. (12), steps number 1 and 2 set the 20-db term. Steps 3 and 4 determine the output signal-to-noise ratio ( $20 \log S_o - 20 \log N_o$ ). Step 5 subtracts the last term from the 20-db term, thus yielding NF.

In making noise measurements, a true-reading rms voltmeter (such as a Ballantine model 320) must be used. An average, or peak-reading, rms calibrated meter will give erroneous readings (unless suitable correction factors are used).

Some comment should be made on the accuracy of this method of measurement. This method is based upon the assumption that the output signal and noise can be measured separately (Eq. 12). This is not exactly true. The signal can be removed while reading the output noise; however, the noise cannot be turned off while measuring the output signal. In effect, the measured value of the output signal will also include the output noise. The last term in Eq. (12) is therefore changed to

$$20 \log \sqrt{S_o^2 + N_o^2} / N_o$$

(The numerator is written in this form because "The rms value of the total wave is the square root of the sum of the squares of the rms values of the components.") The error in this measurement may be figured by first calculating the measured noise figure ( $NF_m$ ) and subtracting this from the true noise figure ( $NF_T$ ).

$$\text{Error db} = NF_T - NF_m = 20 \log \sqrt{\left(\frac{S_o}{N_o}\right)^2 + 1} - 20 \log \frac{S_o}{N_o} \quad (13)$$

To keep the error to a minimum, the signal-to-noise ratio should be as large as possible. The larger the  $S_o/N_o$  is, the less difference there is between the two terms in Eq. (13).

Equation (13) is plotted as a function of  $NF_m$  (Fig. 7). From this curve, the true noise figure may be obtained by adding the error (in db) to the measured noise figure. Two curves are shown in Fig. 7. The first curve is for the case where the input signal-to-noise ratio is selected to be 20 db while the second curve represents an input signal-to-noise ratio of 30 db. Each 10-db increase in the input signal-to-noise ratio transposes the curve 10 db to the right along the abscissa. For a 20-db input signal-to-noise ratio, transistor noise figures may be measured up to 10 db with less than 0.5-db error. This may be acceptable since the overall error of the equipment may be greater than 0.5 db anyway. Convenient levels for the input signal-to-noise ratio are 20 db and 40 db because they set the signal an even 10 times and 100 times greater than the noise.

The above method can be used for the broadband noise measurement (3 db down at 10 cps and 10 kc) or the spot noise measurement (narrow bandwidth). Because of the limited bandwidth in the spot noise method, the input signal and noise powers are greatly reduced as compared to the broadband measurement. Thus more gain will have to be supplied to increase the output to measurable levels. As bandwidths narrow, the time required to average the output readings increases. If the bandwidth is sufficiently small, an integrating circuit with a fairly long time constant may be required on the rms meter monitoring the output.

**1/f Region.** As operation in the audio range is pushed to lower frequencies the observed noise figure is seen to increase. The noise increase approaches a  $-3$  db/octave slope asymptotically as frequency decreases. The  $1/f$  noise curve in effect gives an indication of the relative amount of power that each noise generator at each frequency is capable of delivering. Thus, the noise power at 50 cps is twice the noise power at 100 cps (assuming these points are well within the  $1/f$  region). The characteristic dependence of noise on frequency in this area labels this noise as  $1/f$  noise. Since it is difficult to relate  $1/f$  noise analytically to specific transistor parameters, empirical methods must be relied upon to furnish the desired information necessary to characterize this region.

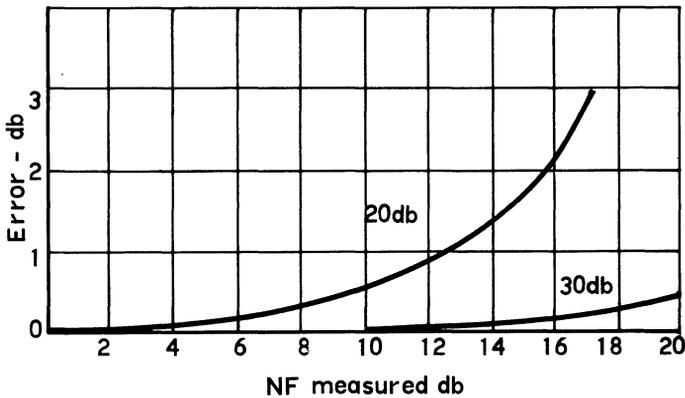


Figure 7

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Of the various methods of noise characterization for the  $1/f$  region, the most complete would be a spot noise check at a number of frequencies from well within the  $1/f$  region to well within the plateau region. This method would plot out the actual NF curve and give detailed information at any frequency. This is not a practical method because of the time and cost involved in making a large number of noise measurements. (It is routinely done, however, on limited sample quantities for typical curves for the data sheet.)

Specifying the NF by the above method, but restricting the number of specified points to three yields a practical and very useful characterization. Of the three points selected:

1. One should be well within the  $1/f$  region
2. One should lie on the "knee" of the curve
3. One should lie well within the plateau region

From these three points a fairly accurate picture of the low and middle frequency regions of the NF curve can be drawn. Figure 8 shows a typical curve drawn from three known points. A fourth point is actually also known. Considering the two asymptotes ( $1/f$  and plateau), the actual NF will be approximately 3 db higher than the cross point. Figure 9 shows a portion of the 2N2586 data sheet with the three selected frequencies are 100 cps, 1 kc and 10 kc. A wideband NF is also given.

Specifying the noise corner frequency (the frequency where the NF is up 3 db from the plateau region) of transistors is not as useful a method as it might seem.

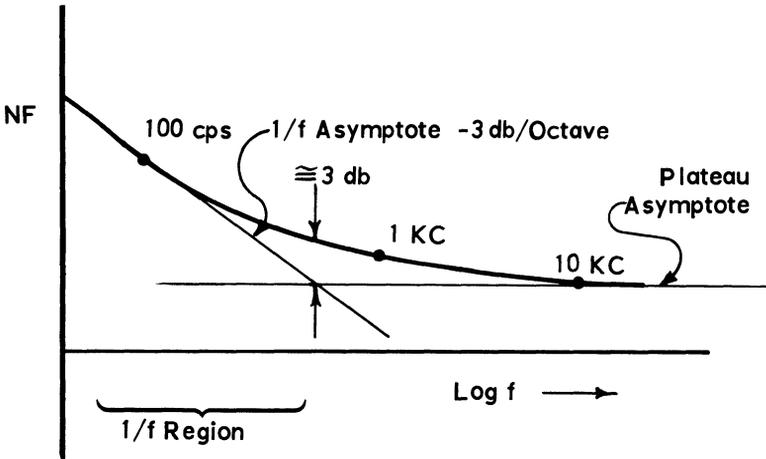


Figure 8

TENTATIVE DATA SHEET

**TYPE 2N2586**  
**N-P-N DOUBLE-DIFFUSED PLANAR SILICON TRANSISTOR**



**FOR EXTREMELY-LOW-LEVEL,  
LOW-NOISE, AMPLIFIER APPLICATIONS**

- Guaranteed Very-Low-Current  $h_{FE} - 80$  min at  $1\mu a$
- Guaranteed Low-Temperature  $h_{FE} - 40$  min at  $10\mu a, -55^{\circ}C$
- Complete Noise Characterization at  $1\mu a$  and  $10\mu a$
- Optional Package Available †

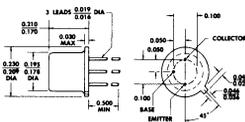


TYPE 2N2586  
MILITARY FORM DCS-62287, AUGUST 1968

**environmental tests**

To ensure maximum integrity, stability, and long life, all finished transistors are subjected to sustained acceleration at a minimum of 35,000 G and verification of hermetic seal by the use of both helium leak and bubble testing.

**mechanical data**



\* THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE.

\* ALL JEDEC TO-18 DIMENSIONS AND NOTES ARE APPLICABLE.

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

**\* absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Collector-Base Voltage . . . . .	60 v
Collector-Emitter Voltage (See Note 1) . . . . .	45 v
Emitter-Base Voltage . . . . .	6 v
Collector Current . . . . .	30 ma
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . .	0.3 w
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 3) . . . . .	0.6 w
Operating Collector Junction Temperature . . . . .	175°C
Storage Temperature Range . . . . .	-65°C to + 300°C

- NOTES: 1. This value applies when the emitter-base diode is open circuited.  
 2. Derate linearly to 175°C free-air temperature at the rate of 2.0 mw/°C.  
 3. Derate linearly to 175°C case temperature at the rate of 4.0 mw/°C.  
 4. These parameters must be measured using pulse techniques. PW = 300  $\mu$ sec, Duty Cycle  $\leq$  2%.

†Electrically identical transistors are also available upon request in TO-5 packages with the active elements insulated from the case.

\*Indicates JEDEC registered data.



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Figure 9

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Two noise figure curves are shown in Fig. 10; one is for a high current gain device and the other is for a low current gain device. Both devices have the same  $1/f$  characteristics and differ only in the plateau region. The figure shows that the higher current gain device will have a higher corner frequency ( $f_c$ ) even though its noise performance is better than the low current gain device at all frequencies. The point where the  $-3$  db/octave asymptote crosses the 0 db NF line is labeled  $f_n$  and is a function of only the  $1/f$  noise. The point  $f_n$  would be independent of the plateau NF.

It should be noted that all of the curves in the  $1/f$  noise region have assumed a constant bias point and  $R_g$ . This condition will not necessarily give optimum NF performance in the  $1/f$  region. Consider for a moment a field-effect transistor. Since the  $1/f$  noise comes from essentially one source, its representation can take the form of a single noise voltage generator in series with the input. This generator is considered in series with the  $e_n$  generator already mentioned. As operation is moved lower in frequency, the total voltage in series with the input increases. As  $e_n$  increases, the optimum source resistance will also increase to yield the optimum value for NF. (Alternatively,  $R_g$  may be held constant while bias current is decreased).

To illustrate this point, a curve (Fig. 11) of  $e_n$  and  $i_n$  as a function of frequency is given for the 2N2500 field-effect transistor. Notice the marked increase in  $e_n$  at low frequencies. Figure 12 illustrates the two cases where: first,  $1/f$  curve was derived for a constant  $R_g$ , and second,  $R_g$  was selected for  $R_{g(opt)}$  for each frequency.

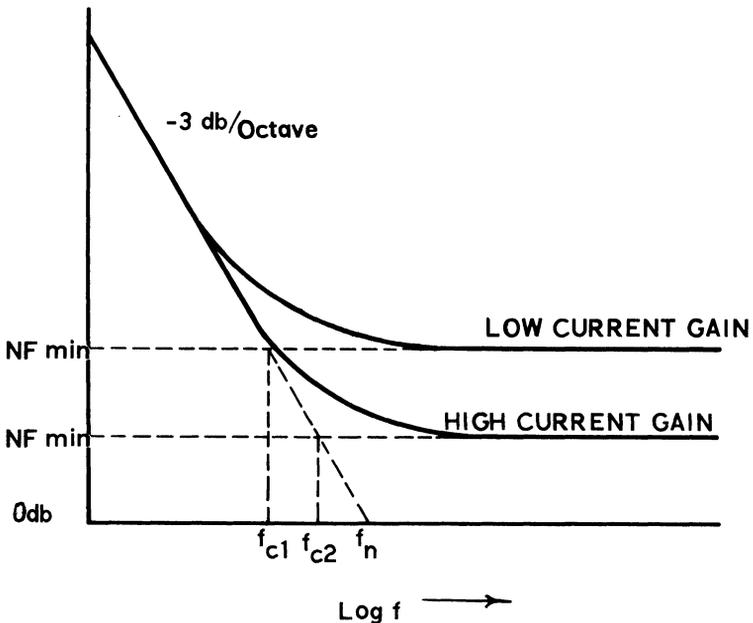


Figure 10

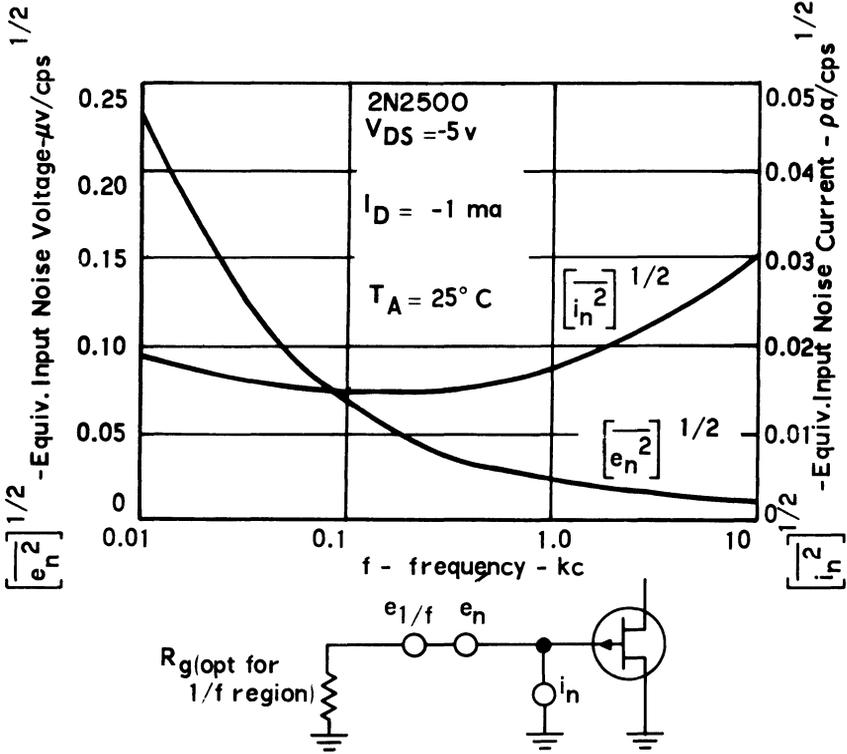


Figure 11

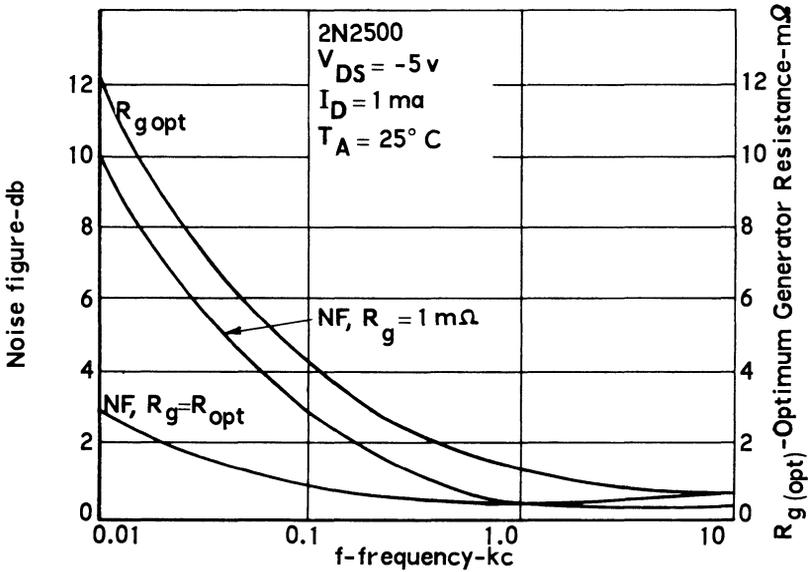


Figure 12

GENERAL CONSIDERATIONS IN LOW-NOISE DESIGN

**Bias Point.** Since NF is a function of  $I_E$ , care must be taken to bias the transistors for low-noise operation. In general, the bias current for best low-noise operation will lie somewhere between  $10 \mu a$  and  $200 \mu a$ . A specific bias point will call for a specific  $R_g$  to give minimum NF. As  $I_E$  decreases, this value of  $R_g$  usually increases.

In designing low-noise stages certain conditions are usually fixed so the designer does not have complete freedom in his design. If  $R_g$  is specified, the designer must select the device and bias current that will give the best low-noise results; however, the device and bias point may not be compatible with other circuit features such as stability and frequency response. When this occurs, compromises must be made. If the design calls for  $I_E = 10 \mu a$  for low-noise considerations, and the leakage current becomes  $10 \mu a$  at elevated operating temperatures, it is obvious that a higher bias current must be used (sacrificing noise performance). See Fig. 13.

**Devices.** Figure 14 shows the noise figure of several TI devices as a function of frequency. The right device for any application will depend upon a compromise between circuit performance and cost.

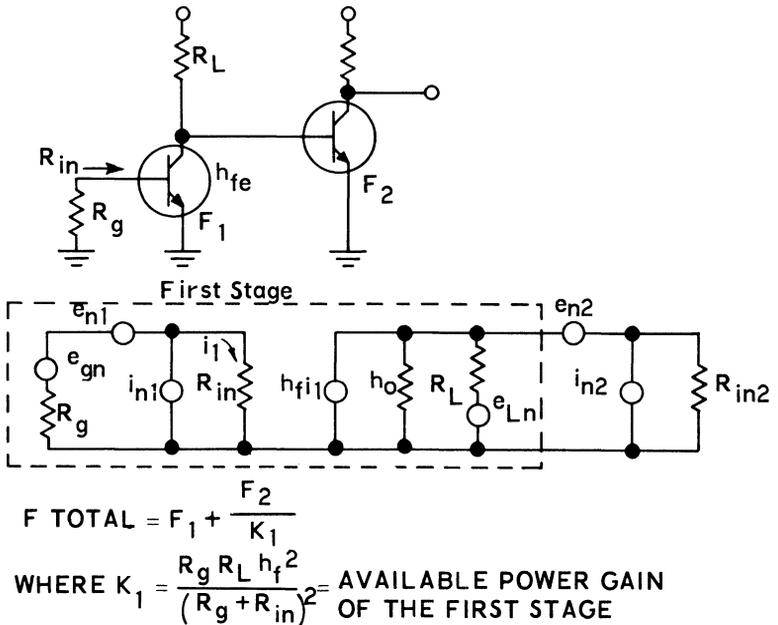


Figure 13

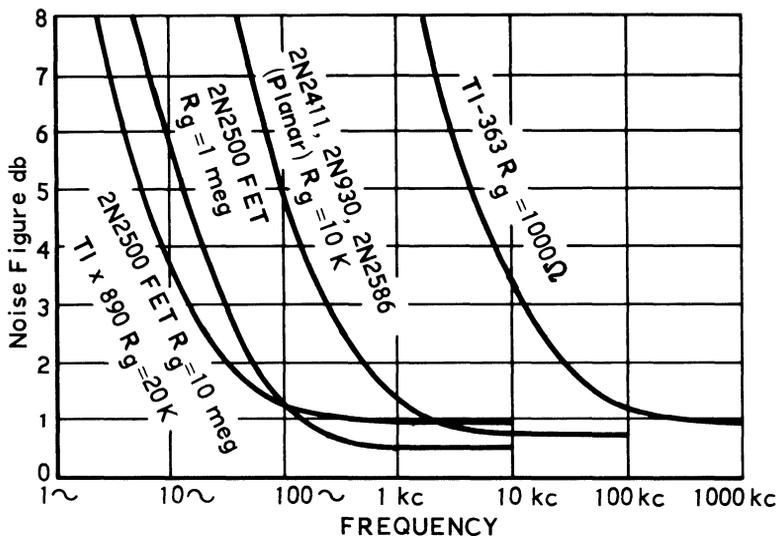


Figure 14

**TERMS DEFINED**

- a — constant
- $\alpha_o$  — low-frequency, common-base, a-c, current gain
- $\Delta f$  — effective noise bandwidth
- $e_{Ln}$  — thermal noise generator associated with the load resistor
- $e_n$  — noise voltage generator
- F — noise factor
- $f_c$  — corner frequency, NF curve has increased 3 db from the plateau region
- $f_n$  — frequency at which the  $1/f$  asymptote crosses the zero-db axis
- $F_{opt}$  — optimum or minimum noise factor
- $e_{gn}$  — thermal noise generator associated with the generator resistor
- $\gamma$  — correlation factor
- $h_{fe}$  — a-c current gain, common-emitter
- $h_{FE}$  — d-c current gain, common-emitter
- $h_o$  — output admittance of a transistor
- $i_n$  — noise current generator
- k — Boltzmann's constant
- NF — noise figure,  $NF = 10 \log F$
- $NF_m$  — measured noise figure
- $NF_T$  — true noise figure
- $N_i$  — noise voltage in
- $N_o$  — noise voltage out
- $N_{p in}$  — noise power in
- $N_{p out}$  — noise power out
- $R_g$  — generator resistance
- $R_{in}$  — input resistance
- $R_{open}$  — resistance that simulates an open circuit
- $R_{opt}$  — optimum generator resistance that gives minimum noise figure
- $R_{short}$  — resistance that simulates a short circuit

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$r'_b$	— ohmic base resistance in transistor equivalent circuit
$r_e$	— incremental emitter resistance in transistor equivalent circuit
$S_i$	— signal voltage in
$S_o$	— signal voltage out
$S_{p\ in}$	— signal power in
$S_{p\ out}$	— signal power out
$T$	— temperature in degrees Kelvin $T = 273 + ^\circ\text{C}$

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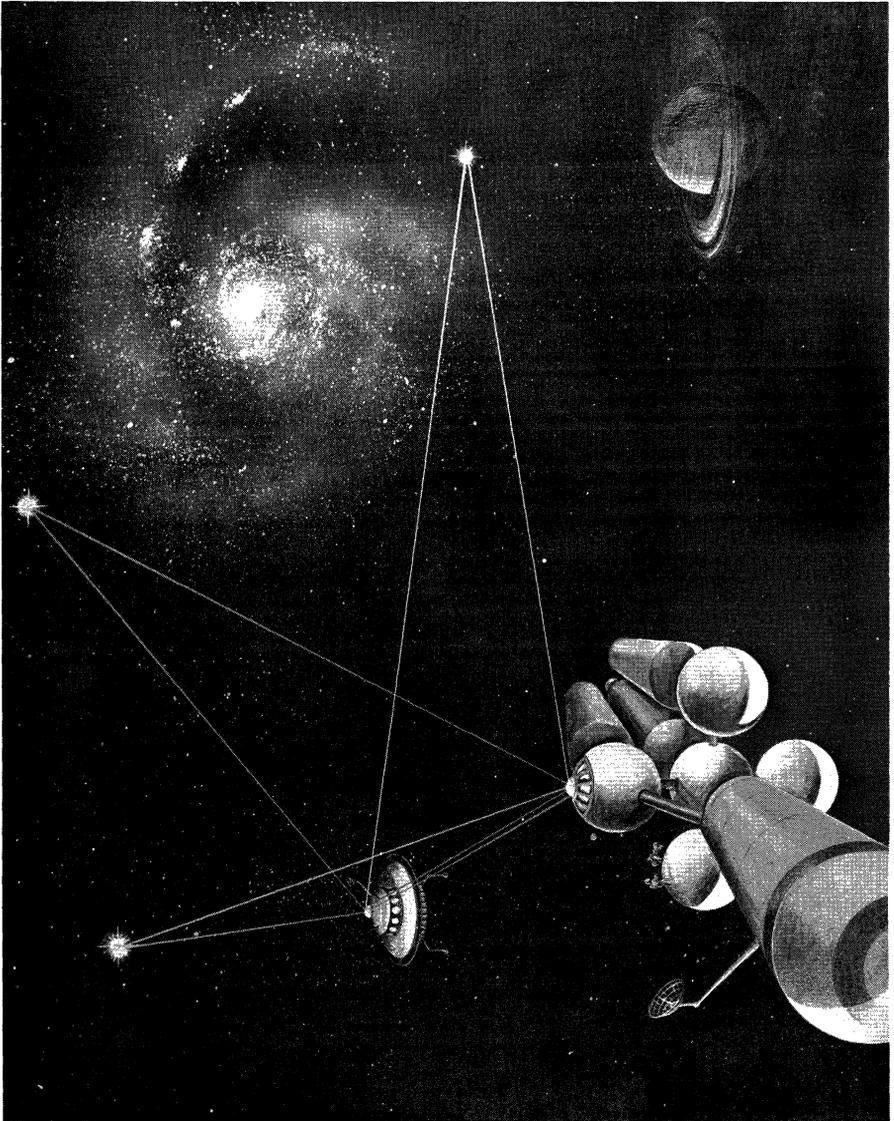
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## Transistor Gain Control

by Bill Tulloch

### INTRODUCTION

Amplifiers are usually designed to meet predetermined gain, pass-band, and noise requirements. Additional requirements are created when these amplifiers are used as integral parts of a system. The requirement discussed here is the ability of a system to handle input signals that have wide dynamic ranges. A receiver that is capable of receiving input signals from several microvolts to several hundred millivolts without distorting the intelligence is an example of such a system.

To meet this requirement the designer provides a means of controlling the gain of the individual amplifier stages. This is accomplished by the use of feedback to automatically control the bias of the amplifier. The gain of a transistor amplifier can be controlled by three methods: external gain control, internal gain control, or a combination of external and internal control called hybrid gain control.

### EXTERNAL GAIN CONTROL

External gain control is accomplished by reducing the signal available to either the input or the output of the amplifier. Three examples of external gain control are presented in Fig. 1. Figure 1a is of the input shunt type, in which the control element reduces the signal available to the input of the transistor, thereby reducing the effective gain of the stage. The output shunt type is shown in Fig. 1b; in this type, the gain is reduced by decreasing the collector a-c impedance. In Fig. 1c the control element is used to provide emitter degeneration to reduce the gain of the stage.

The major disadvantage of external gain control is the additional components needed for the separate biasing of the control elements. Since the characteristics of an external-gain-controlled amplifier are only slightly dependent on the characteristics of the transistor, the balance of this discussion deals with internal and hybrid gain control methods.

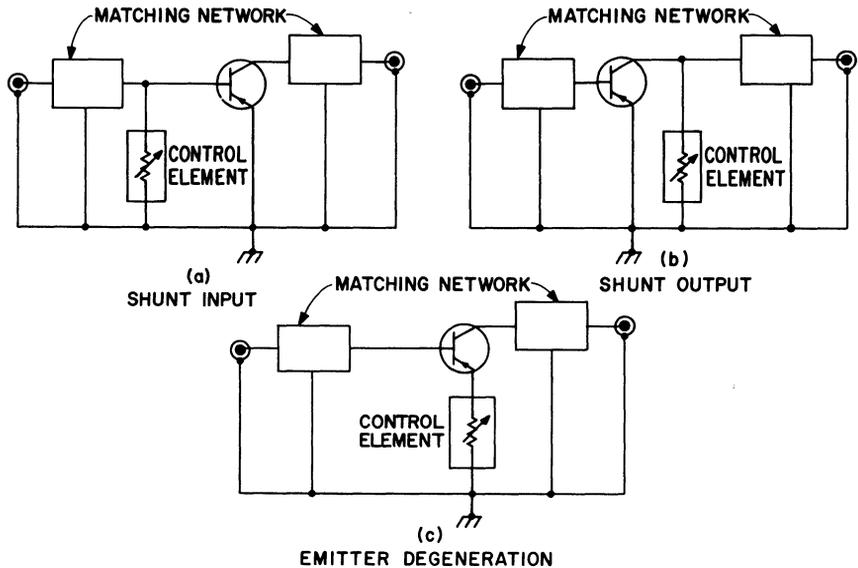


Fig. 1. Types of external gain control.

**INTERNAL GAIN CONTROL**

The internal gain control characteristics of a transistor amplifier may be predicted, given sufficient knowledge of the parameter variations versus bias. To obtain this information it is necessary to measure parameters of a number of transistors at various operating conditions for the frequencies of interest. The amplifier gain is then calculated at each bias point using conventional design techniques. It is enormously time-consuming to evaluate each amplifier to be designed for gain control.

Another method of evaluation is to design the amplifier for the desired gain, pass-band, and noise requirements using the manufacturer's recommended bias conditions. Once the amplifier has been constructed, the gain control characteristics may then be measured rapidly. This is the technique used in obtaining the curves presented later. There are three types of transistor internal gain control: forward, reverse, and tetrode.

Forward gain control is accomplished by varying the collector-base (or collector-emitter) voltage in accordance with the collector current. Figure 2 is a diagram of a forward-gain-controlled amplifier. The collector current increases as the AGC voltage is increased and  $V_{CB}$  is reduced due to the additional voltage developed across  $R_c$ . The output impedance of the transistor is considerably reduced at the high-current low-voltage conditions, so an increase in bandwidth is to be expected. The other transistor parameter variations are dependent on the type of transistor, frequency of operation, and circuit components. Forward gain control usually accepts larger input signals as the gain is reduced.

Figure 3 is a diagram of a reverse-gain-controlled amplifier. The gain of such an amplifier is reduced by decreasing the collector current with the collector voltage remaining relatively constant. There is no collector dropping resistor ( $R_c$ )

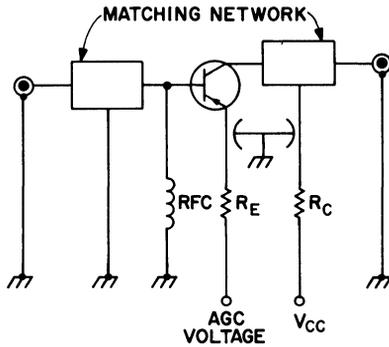


Fig. 2. Forward gain control.

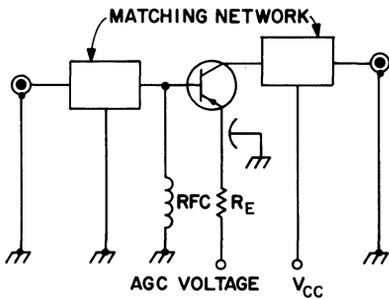


Fig. 3. Reverse gain control.

for this type of control. The bandwidth change is less with reverse gain control than with forward gain control; however, reverse gain control amplifiers have a decreasing input signal capability as the gain is reduced.

Figure 4 is an example of a tetrode gain-controlled amplifier. Tetrode gain control is obtained by varying the base-2 current. The base-2 current for gain control ranges approximately from  $-100$  to  $+100 \mu a$  depending on the frequency of operation and the desired gain range. A tetrode gain control amplifier uses less AGC power than the other two types and will handle increasingly larger input signals as the gain is reduced.

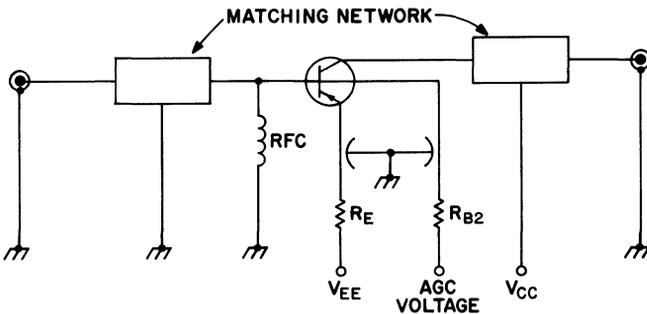


Fig. 4. Tetrode gain control.

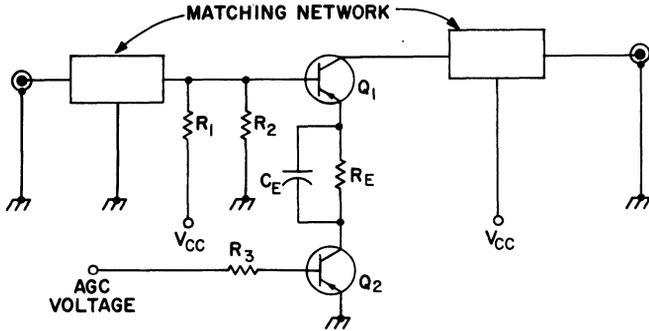


Fig. 5. Hybrid gain control.

**HYBRID GAIN CONTROL**

There are systems that demand the acceptance of maximum input signals of one to ten volts. None of the internal gain control types will perform this function. By using a transistor for the control element as shown in Fig. 5, it is possible to control the gain by two methods simultaneously. For maximum gain conditions,  $Q_2$  is in saturation and  $Q_1$  is biased for the desired gain and noise requirements. For gain control, the AGC voltage is changed so that  $Q_2$  is brought out of saturation. The output impedance of  $Q_2$  is increased as the collector current is decreased, providing emitter degeneration. At the same time, the collector current of  $Q_1$  is also being reduced, giving reverse gain control action. This type of gain control has two advantages: a greater reduction in gain is possible in this type than with the reverse gain control only. Second, the capability of handling input signals of a large magnitude is available due to the increasing emitter impedance. The noise figure of this method of gain control usually is no more than 1 db greater than that of the basic amplifier at the same bias conditions.

**GAIN-CONTROLLED AMPLIFIER STAGES**

Six transistor amplifiers are presented to demonstrate the different methods of gain control. The gain, bandwidth, and center frequency characteristic curves are shown so that comparisons may be made. Maximum gain in the forward and reverse gain control curves are at the same bias point. The noise figures discussed are measured at this bias condition. Noise figure is of primary interest only at this point since at the reduced gain levels the signal-to-noise ratio is larger. Insertion gain is defined as the ratio of the output power to the generator power into the same load. Maximum input signal capability is defined as the RMS signal measured at the input of the amplifier that will result in a 0.75-db change in the output power with a 1-db input power change.

Figure 6 is a schematic of a 30-mc amplifier. This amplifier is used to evaluate both reverse and forward gain control characteristics.  $R_c$  is zero ohms for reverse gain control and 1000 ohms for forward gain control. The gain is 15 db with a typical noise figure of 5 db. Figure 7 shows that the reverse gain control range is 25 db from a collector current of 1.5 milliamps to 20 microamps. Figure 8 shows the pass-band characteristics with  $f_1$  and  $f_2$  being the lower- and upper-half power frequencies, respectively. Center frequency is indicated as  $f_0$ . Bandwidth change is less than 2:1 over the range shown.



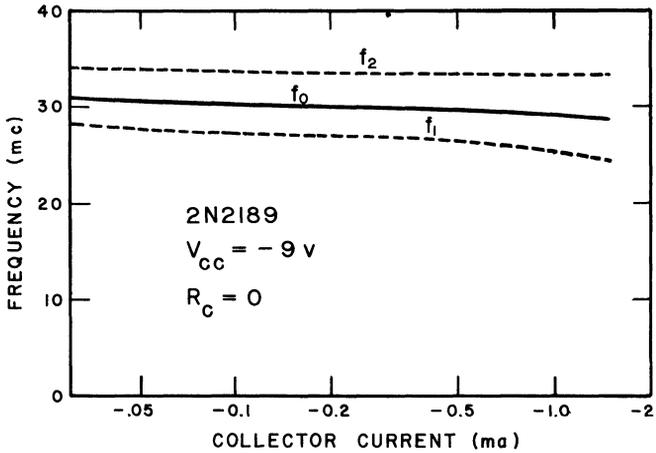


Fig. 8. Reverse gain control pass-band characteristics.

Figure 9 is the forward gain control characteristic. This circuit provides 20 db of forward gain control, but essentially all of the change is in the 8- to 10-milliamp region of collector current. The flatness of this curve can be used as a form of delayed AGC. Figure 10 presents the forward gain control pass-band characteristics. This curve is limited to 8 milliamps due to the large change in bandwidth and center frequency at higher currents. This change is caused by the transistor approaching saturation. Input signal capability is 35 millivolts at maximum gain, 3 millivolts at minimum reverse gain, and only 10 millivolts at minimum forward

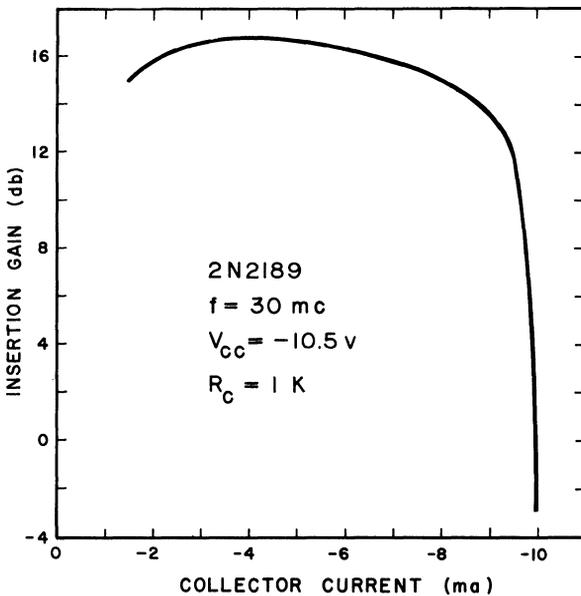


Fig. 9. Forward gain control characteristic.

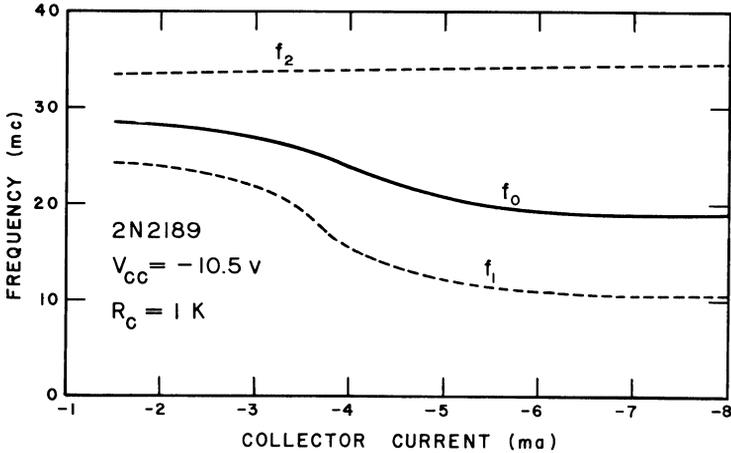


Fig. 10. Forward gain control pass-band characteristics.

gain. Lower signal capability at minimum forward gain is another indication that the transistor is almost in saturation.

Figure 11 is a 30-mc tetrode amplifier. Collector voltage and current are kept constant and the gain is changed in accordance with the base-2 current. The collector-base voltage is + 20 volts and the collector current is 1.3 milliamps. The gain is 21 db with a typical noise figure of 6 db at the base-2 current of -100 microamps. Tetrode gain control characteristics also show a delay (Fig. 12). Figure 13 gives the pass-band characteristics. The increase in bandwidth is caused by a decrease in output impedance of the tetrode as the gain is reduced. The input signal capability of this circuit is 25 millivolts at -100 microamps of base-2 current and 300 millivolts at + 20 microamps of base-2 current.

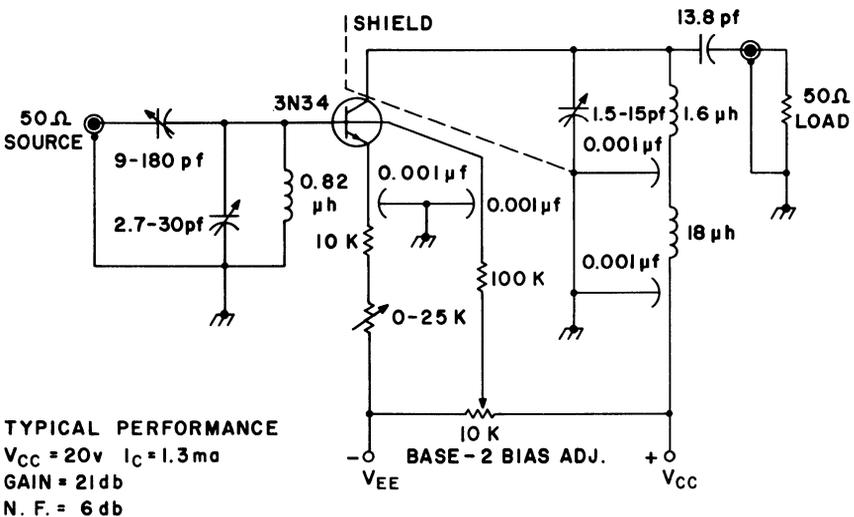


Fig. 11. 3N34 30-mc amplifier.

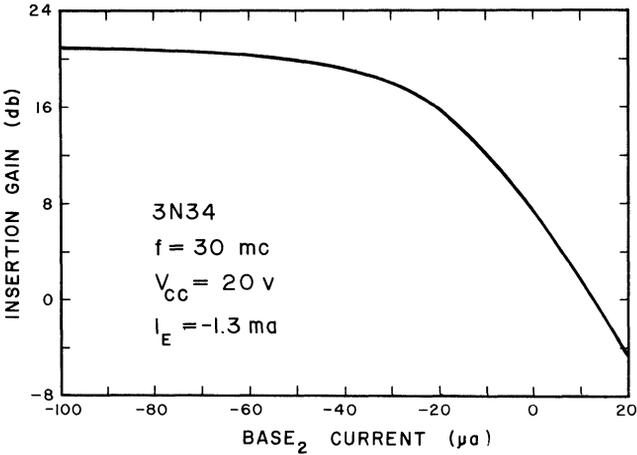


Fig. 12. Tetrode gain control characteristic.

Figure 14 is a 70-mc neutralized amplifier. At a collector voltage of  $-6$  volts and a collector current of 2 milliamps, the gain is 27 db with a typical noise figure of less than 3 db.  $R_C$  for reverse gain control is 0 ohms and for forward gain control is 1000 ohms. Figure 15 shows a reverse control range of 35 db. The slope of this curve is approximately 20 db of gain for a decade of current change. Figure 16 presents the reverse gain control pass-band characteristics. The bandwidth is increasing at the lower current levels with this circuit. Figure 17 is the forward gain control characteristic. Forward gain control of 47 db is made available by increasing the collector current to approximately 7 ma. Again we notice a delay in the characteristic before the gain begins to fall. In Fig. 18 the bandwidth has greater than 4:1 change as the current is increased to 6 milliamps. The input signal capability is 40 millivolts at maximum gain, 5 millivolts at minimum reverse gain, and 200 millivolts at minimum forward gain.

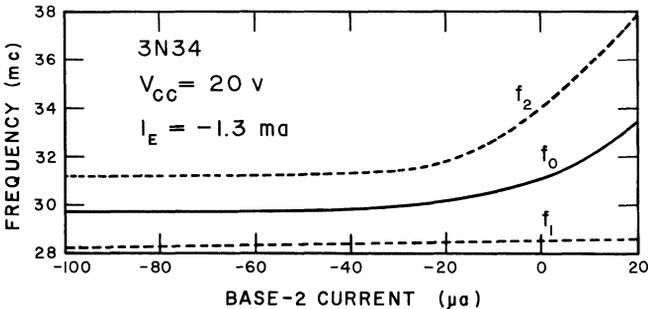
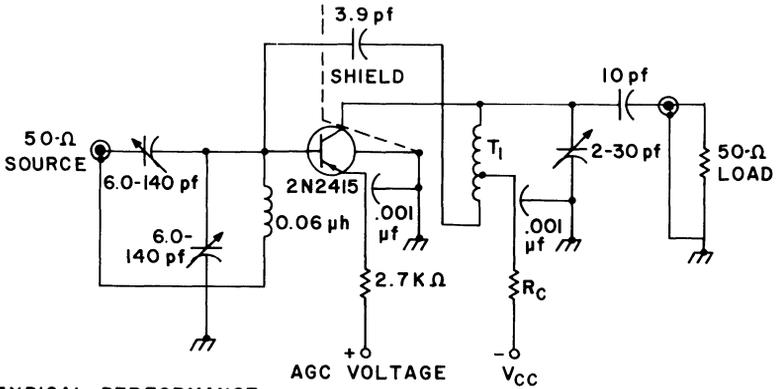


Fig. 13. Tetrode gain control pass-band characteristics.



TYPICAL PERFORMANCE  
 $V_{CB} = -6\text{ v}$   $I_C = -2\text{ ma}$   
 GAIN = 27 db  
 N. F. < 3 db

$T_1$  - 5t AIR DUX #516  
 TAPPED 4t FROM THE  
 COLLECTOR

Fig. 14. 2N2415 70-mc neutralized amplifier.

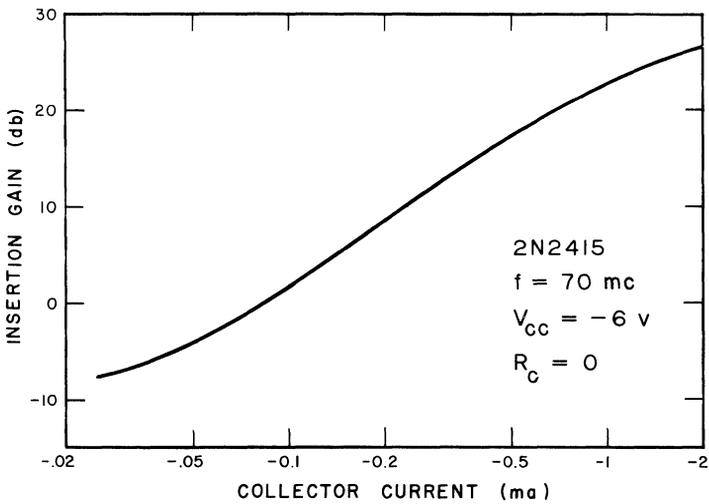


Fig. 15. Reverse gain control characteristic.

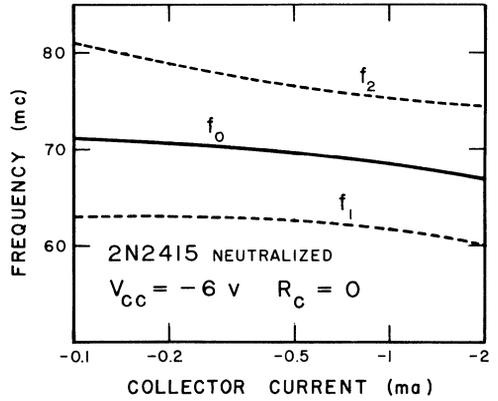


Fig. 16. Reverse gain control pass-band characteristics.

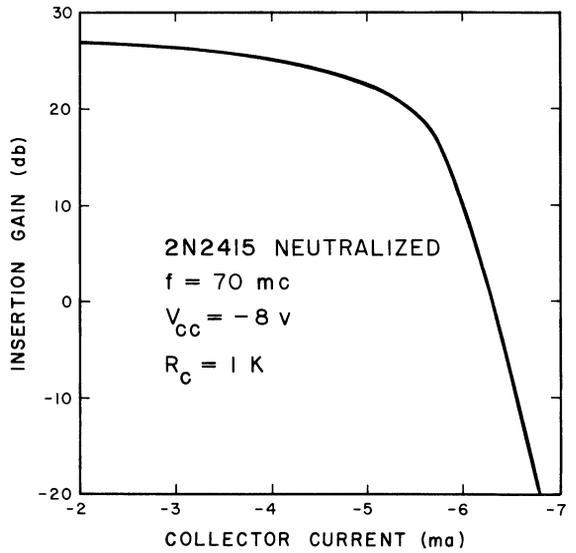
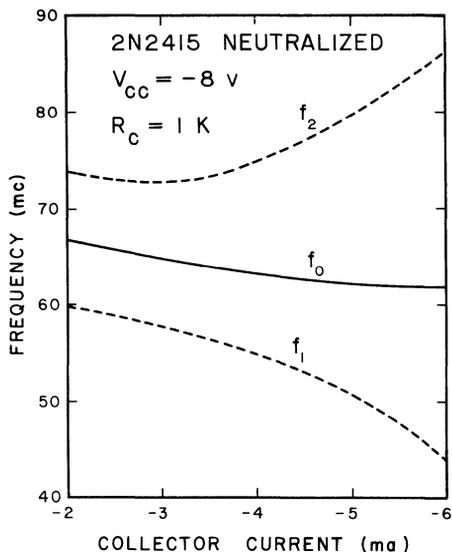


Fig. 17. Forward gain control characteristic.



**Fig. 18. Forward gain control pass-band characteristics.**

Figure 19 is a 200-mc amplifier. At a collector voltage of  $-6$  volts and a collector current of 1.5 milliamps, this circuit has a gain of 17 db with a typical noise figure of 3 db. Figure 20 presents the reverse gain control characteristic. There is a 32-db reduction in gain with a change in collector current from 1.5 milliamps to 20 microamps. This curve also has approximately 20-db change in gain per decade change of collector current. Figure 21 shows the reverse gain control pass-band characteristics. There is a 2:1 increase in bandwidth as the current is reduced, with a 24-mc change in the center frequency. Figure 22 indicates 24 db of forward gain control with the collector current increased to 9.5 milliamps. The top portion of this curve is not as flat as in some of the other amplifiers. Figure 23 is the forward gain control pass-band characteristic. This circuit has a 4:1 change in bandwidth with a 24-mc change in the center frequency as the gain is reduced for forward gain control. The input signal capability is approximately the same as for the 70-mc amplifier.

Figure 24 is a 450-mc amplifier that has a gain of 8 db with a typical noise figure of 4 db when biased with a collector voltage of  $-6$  volts and a collector current of 2 milliamps. Figure 25 is the reverse gain control characteristic. Gain control of 21 db is available by decreasing the collector current to 20 microamps. The gain change is beginning to level off at 40 microamps of collector current for this amplifier. Figure 26 indicates only small changes in the pass-band characteristics for the full range of reverse gain control. This curve indicates that the pass-band characteristics for the 2N2415 at 450 mc are very stable with gain control. Figure 27 shows a 26-db range of forward gain control by increasing the collector current to 7 milliamps. Again we notice a delay region in the forward gain control characteristic before the gain begins to fall. Figure 28 indicates less than 1.5:1 increase in bandwidth with a collector current of 6.5 milliamps. There is practically no change in center frequency. The input signal capability is 50 mv at maximum gain, 20 mv at minimum reverse gain, and 500 mv at minimum forward gain. This indicates that the 2N2415 also performs very well as a forward-gain-controlled amplifier at 450 mc.

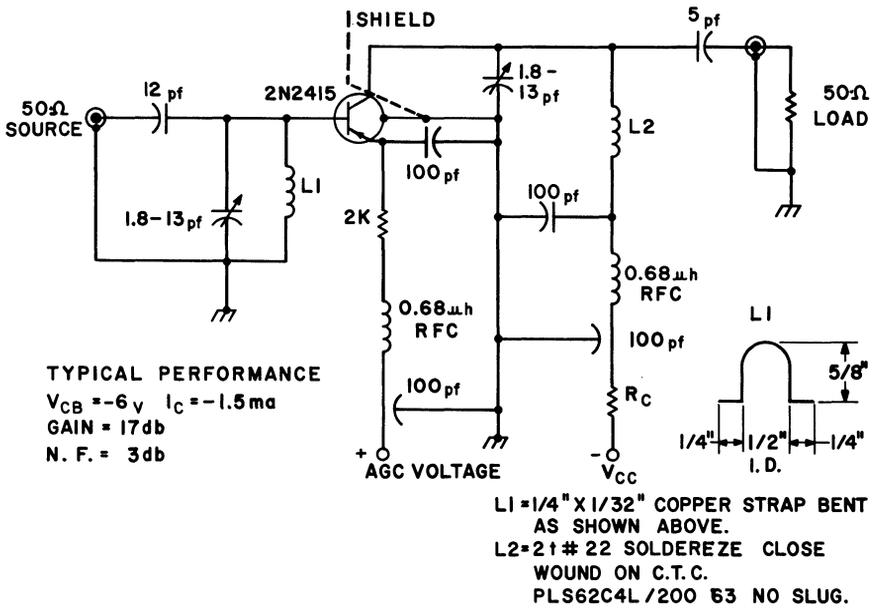


Fig. 19. 2N2415 200-mc amplifier.

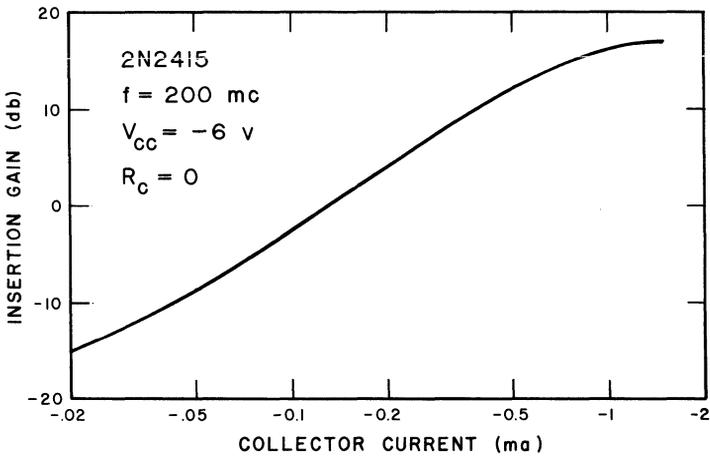


Fig. 20. Reverse gain control characteristic.

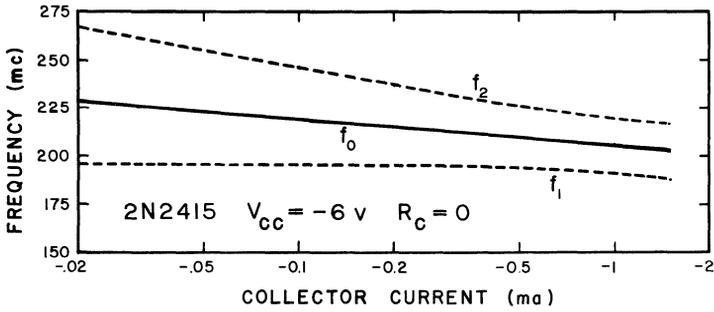


Fig. 21. Reverse gain control pass-band characteristics.

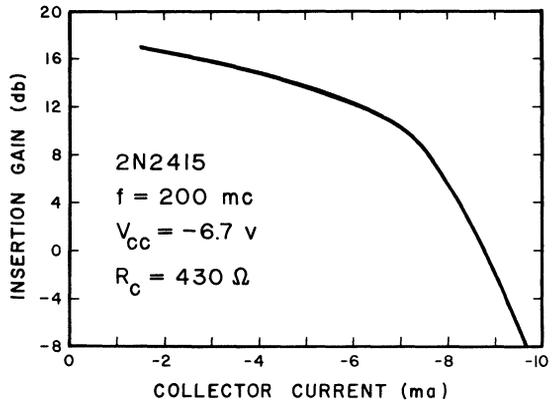


Fig. 22. Forward gain control characteristic.

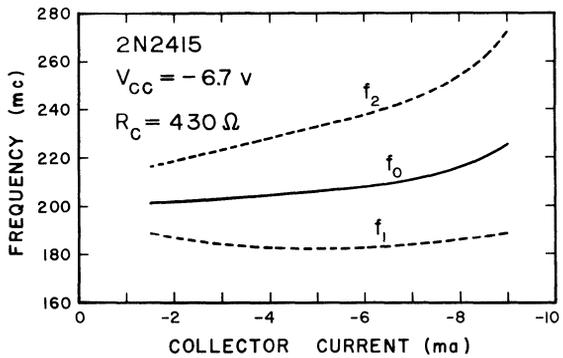
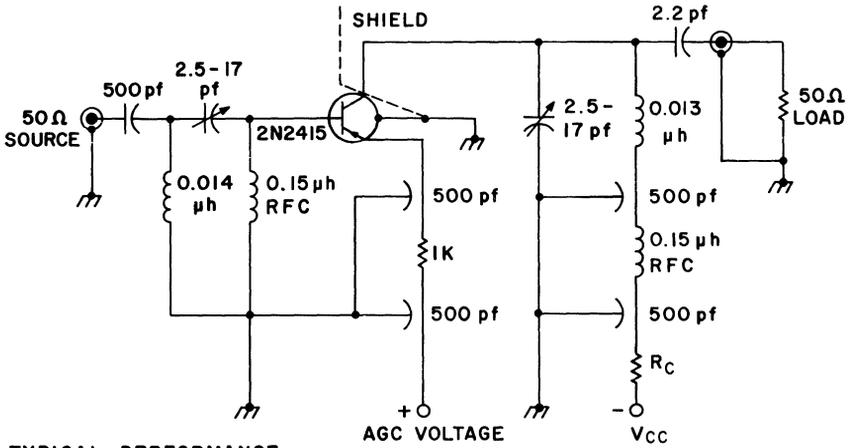


Fig. 23. Forward gain control pass-band characteristics.



**TYPICAL PERFORMANCE**  
 $V_{CB} = -6v$   $I_C = -2ma$   
**GAIN = 8 db**  
**N. F. = 4 db**

Fig. 24. 2N2415 450-mc amplifier.

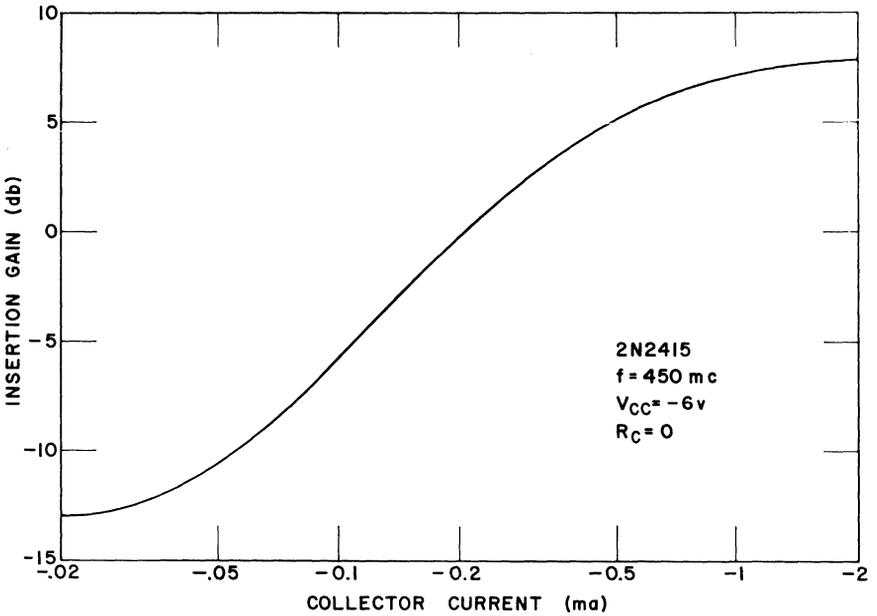


Fig. 25. Reverse gain control characteristic.

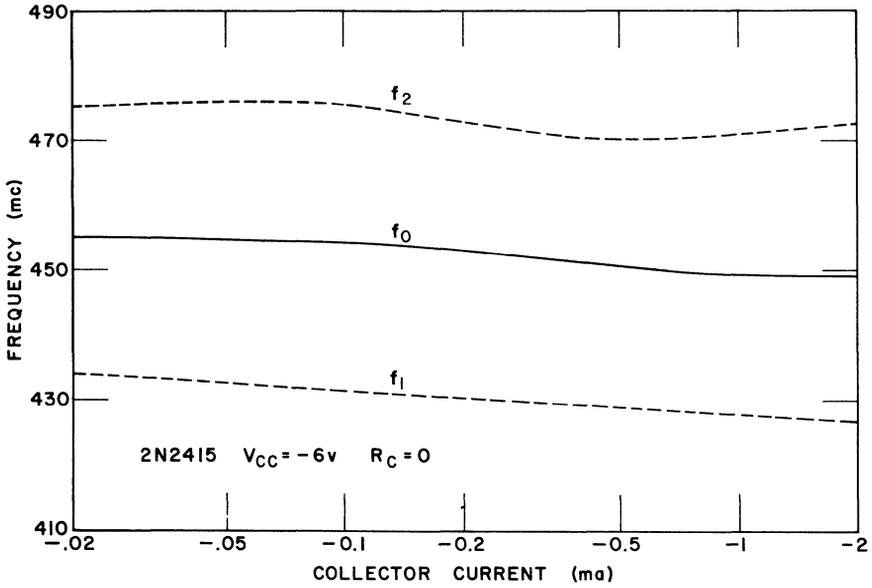


Fig. 26. Reverse gain control pass-band characteristics.

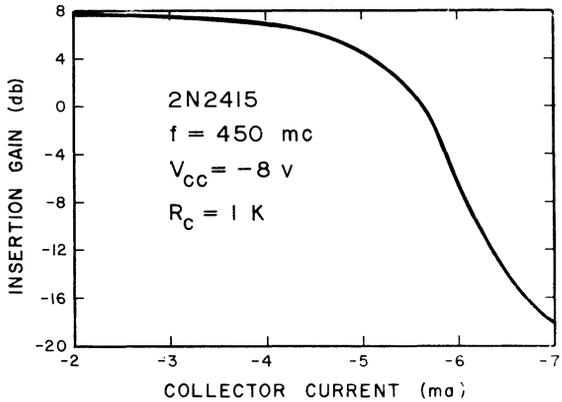


Fig. 27. Forward gain control characteristic.

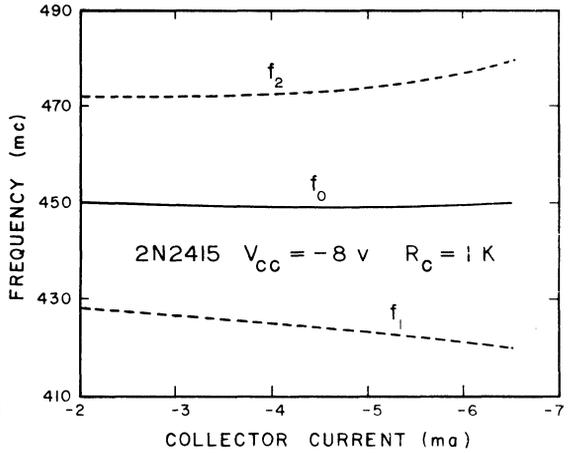


Fig. 28. Forward gain control pass-band characteristics.

Figure 29 is the 30-mc amplifier shown in Fig. 6, modified to demonstrate the hybrid gain control method. Q<sub>2</sub> acts as a variable impedance to give emitter degeneration, which is a form of external gain control. Q<sub>2</sub> also controls the collector current of Q<sub>1</sub> to give reverse gain control action, an internal gain control method. Figure 30 is the gain control characteristic for this circuit. The gain control range is 33 db (6 db more than for Fig. 6). There is a sharp change in gain as the collector current is reduced due to the increase in impedance of Q<sub>2</sub> as it is brought out of saturation. Figure 31 presents the pass-band characteristic of the hybrid circuit. There is a 2:1 change in bandwidth over the gain control range with most of the change from 1.0 to 1.5 ma of collector current. The center frequency shift is less than 1.5 mc. This circuit has a typical noise figure of 5.5 db (only 0.5 db more than that of Fig. 6). The input signal capability is 35 mv at maximum gain, but it is 11.5 volts at minimum gain. This is possible because of the high emitter impedance that Q<sub>2</sub> provides.

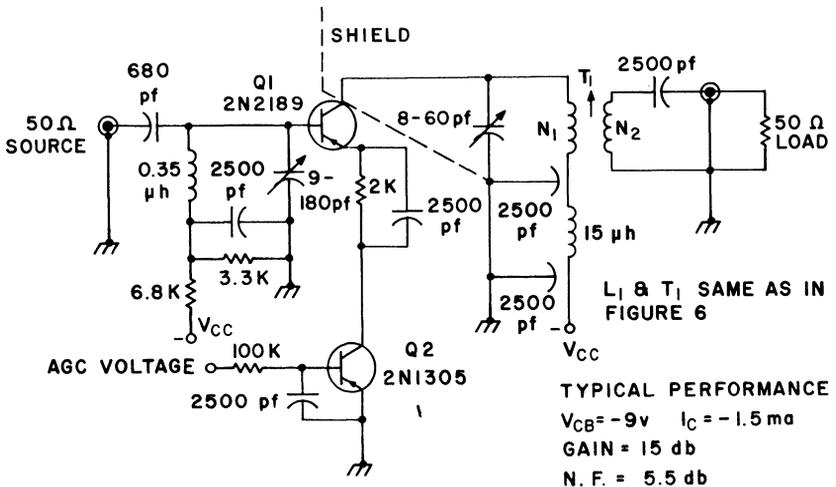


Fig. 29. 2N2189 30-mc amplifier (hybrid gain control).

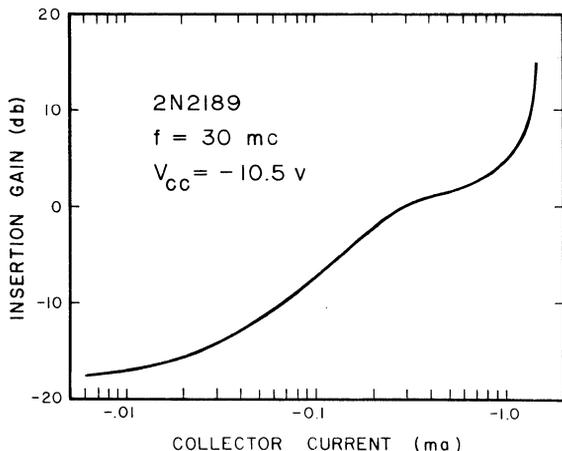


Fig. 30. Hybrid gain control characteristic.

COMMENTS

Comparisons of the different gain control methods may be made; however, the gain control characteristics of an amplifier depend not only on the transistor characteristics but are also influenced by the matching networks. Therefore, these comments are generalized only and may vary with individual circuits.

Reverse gain control circuits usually have a fairly predictable gain variation. The signal-handling capability decreases as the gain is reduced, and the changes in pass-band characteristics are reasonable. The AGC power required is relatively low.

Forward gain control characteristics vary more widely and depend upon the type of transistor, frequency, value of collector d-c resistance ( $R_C$ ), and matching networks. Forward gain control will normally handle increasingly larger input signals as the gain is reduced unless transistor "saturation" is approached. The bandwidth will increase with reduced gain due to the decrease in transistor impedance with the increase in collector current. Higher AGC power is necessary to give the high collector currents for forward gain control.

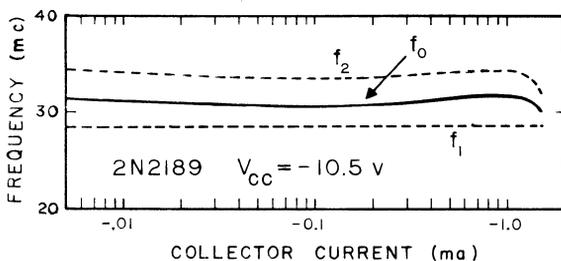


Fig. 31. Hybrid gain control pass-band characteristics.

Tetrode gain control requires the least amount of AGC power, and is able to accept increasing input signals as the gain is reduced. Receivers, using tetrodes, have been built that have greater than 100 db of linear gain control with close tolerances on the gain and phase characteristics.

The hybrid gain control circuit has the advantage of reverse gain control but also has the ability to handle input signals of much larger amplitudes with little degradation of available gain or noise figure. This method requires only an additional transistor, resistor, and capacitor.

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## RF Harmonic Oscillators

by George Johnson

This chapter discusses some of the fundamentals of RF harmonic oscillator design. The characteristic equation for the various oscillator configurations is used to develop expressions for the natural frequency of oscillation and the necessary conditions for buildup of oscillation. Causes of frequency instability and methods of improving stability are discussed. The effects of changing load, changing passive parameters, and changing active parameters are analyzed. A brief treatment of crystal oscillators is presented along with a discussion of the crystal itself. Finally, a design procedure is proposed, and circuit examples are presented.

The general treatment of oscillators in this chapter is on a linear basis. However, the conditions of self-sustained oscillation must necessarily be nonlinear. Because of this linear analysis restriction, certain interesting topics such as limiting output voltage and current amplitude will be treated on a very approximate basis. To analyze these aspects more accurately would require limit-case solutions of the nonlinear differential equation describing the oscillator current or voltage in the phase plane, which are beyond the scope of this treatment.

### OSCILLATOR CONFIGURATIONS

**Necessary Conditions for Oscillation.** The first necessary condition for self-sustained oscillation in a circuit is that the active device permit power gain at the frequency of oscillation. Furthermore, the device must have sufficient gain to overcome circuit losses and establish exactly unity gain around the feedback loop. The second necessary condition is that the phase shifts introduced by the active device and the feedback network result in exactly zero phase shift around the overall circuit.

These conditions will permit sustained oscillations, but they do not guarantee that oscillations will occur. In other words, it is not enough that unity loop gain can exist. There must be more than unity loop gain at first to cause buildup of oscillations. These, then, are the necessary and sufficient conditions for the buildup and maintenance of self-sustained oscillation in a circuit.

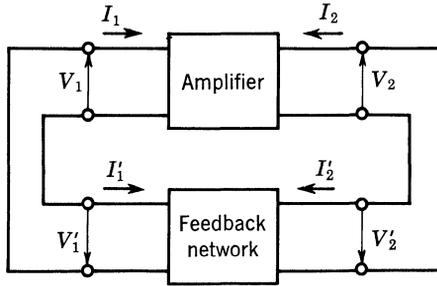


Fig. 1. Feedback oscillator configuration.

**Basic Configurations.** Most oscillator circuits can be regarded as having two basic components: the amplifier and the frequency-selective feedback circuit. This arrangement is known as a *feedback oscillator*, and is shown in Fig. 1. The frequency-selective circuit can be further reduced to the network arrangement shown in Fig. 2. This configuration allows a clear visualization of each of the basic oscillator types. If  $K_2$  and  $K_1$  are capacitors and  $K_3$  is an inductor, the circuit is a Colpitts type. Figure 3 shows this configuration. If  $K_1$  and  $K_2$  are inductors and  $K_3$  is a capacitor, the configuration is called a Hartley oscillator and is shown in Fig. 4. Figure 5 shows the Hartley configuration realized with a two-winding transformer. The choice between a two-winding transformer and a tapped coil depends partly on the frequency of operation, since the expressions for the natural frequency of oscillation are slightly different. Also, the tapped coil requires an extra d-c isolation capacitor, which is not necessary with the two-winding transformer. Because of the possibility of obtaining phase reversal with the two-winding transformer, the transistor can be changed from common base to common emitter.

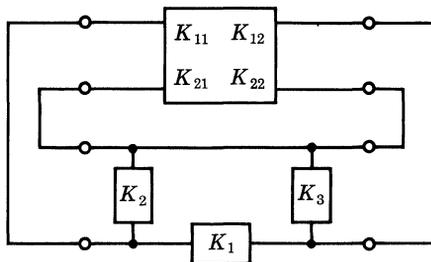


Fig. 2.  $\pi$ -type feedback oscillator.

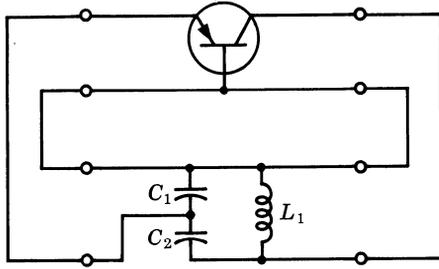


Fig. 3. The Colpitts type circuit.

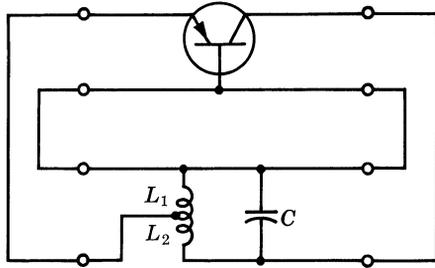


Fig. 4. The tapped Hartley circuit.

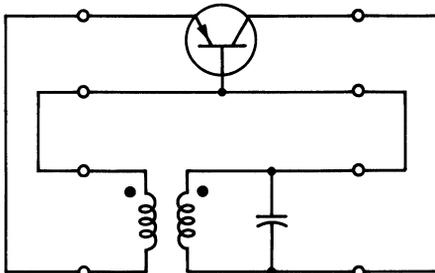
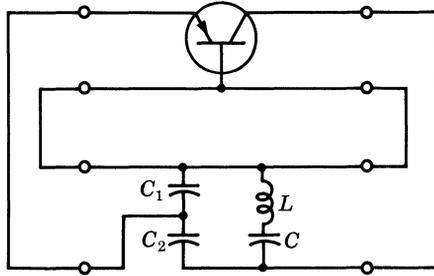


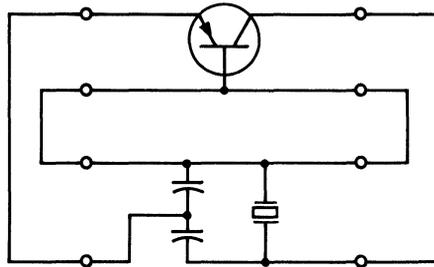
Fig. 5. Two-winding Hartley oscillator.

A modification to the Colpitts circuit results in the Clapp oscillator. In this circuit, the resonant frequency is determined primarily by the series combination of L and C. Figure 6 shows the arrangement. Where there is a requirement for high stability, crystals may be used for the frequency-determining element. A configuration using a crystal is shown in Fig. 7.

Some of the many possible modifications to the above basic configurations are shown in the circuit performance section. These arrangements of the active device and passive structure have been made so that it will be easy to combine the two-terminal pair parameters of each *black box* into one equation characterizing the composite network. The set of equations characterizing the active device in h parameters is shown in Eqs. (1) and (2).



**Fig. 6. The Clapp oscillator.**



**Fig. 7. Crystal oscillator.**

$$V_1 = h_{ib}I_1 + h_{rb}V_2 \tag{1}$$

$$I_2 = h_{fb}I_1 + h_{ob}V_2 \tag{2}$$

Equations (3) and (4) characterize the passive structure.

$$V_1' = h_{11}I_1' + h_{12}V_2' \tag{3}$$

$$I_2' = h_{21}I_1' + h_{22}V_2' \tag{4}$$

The combination of these black boxes results in a set of equations which completely characterize the composite network. For the networks of the type shown in Fig. 2, the combination must be accomplished as indicated in Eqs. (5) and (6).\*

$$V_1'' = (h_{ib} + h_{11})I_1'' + (h_{rb} - h_{12})V_2'' \tag{5}$$

$$I_2'' = (h_{fb} - h_{21})I_1'' + (h_{ob} + h_{22})V_2'' \tag{6}$$

Oscillator connections are special cases, however, since  $V_1'' = 0$  and  $I_2'' = 0$ . These restrictions create the set of simultaneous homogeneous linear equations shown in Eqs. (7) and (8).

$$0 = (h_{ib} + h_{11})I_1'' + (h_{rb} - h_{12})V_2'' \tag{7}$$

$$0 = (h_{fb} - h_{21})I_1'' + (h_{ob} + h_{22})V_2'' \tag{8}$$

This set is, by definition, the characteristic equation of the combined network; and its solution for the imaginary part will yield the natural frequency of the system. This may be done by inserting actual circuit values into Eq. (9) and solving for the imaginary part equated to zero.

$$(h_{ib} + h_{11})(h_{ob} + h_{22}) - (h_{rb} - h_{12})(h_{fb} - h_{21}) = 0 \tag{9}$$

Evaluation of the real part of the expression is done in a similar way to yield the unity gain and, hence, starting conditions. Table 1 lists the natural frequencies and starting conditions for various configurations.

## TANK CIRCUIT

**Considerations for the Tank Circuit.** Tuned LC circuits can be made to store energy. Used for this purpose, they have acquired the nickname of "tank" circuits. The frequency-determining LC circuit of an oscillator is such an example. The three essential parameters of the oscillator tank circuit are natural frequency of oscillation, selectivity, and characteristic impedance. The tank performs the following functions:

1. It determines the frequency of oscillation.
2. It is the feedback network.
3. It determines the stability of the oscillator.
4. It is a part of the coupling network to the load.
5. It affects the noise energy output of the oscillator.
6. It is a principal factor determining the circuit efficiency.

For a well-designed oscillator, the reactive components surrounding the tank are negligible in their effect on the resonant frequency set by the L and C of the tank.

\*See Ref. 3, p. 553, for further discussion.

It is easily seen in Figs. 1 to 3 that the tank can be treated as a feedback network connected across the active device. Even in the Clapp connection of Fig. 6 this is still true, but now the feedback is primarily determined by divider action of  $C_1$  and  $C_2$ , and the frequency is determined by  $L$  and  $C$  in series.

Frequency stability is primarily determined by the  $Q_L$  of the tank. The reason for this is that the frequency deviation required to develop a given phase correction to establish exactly  $360^\circ$  phase shift around the feedback loop is inversely proportional to the loaded  $Q$ . Frequency stability is usually the most difficult specification to meet, and meeting it will usually more than satisfy the other requirements of constant  $Q$  and constant characteristic impedance. In other words, the environment of the tank tends to change not only for  $f_0$ , but also  $Q$  and  $Z_0$ :\* By satisfying the requirement for stability of  $f_0$ , one usually satisfies the requirements of stability of  $Q$  and  $Z_0$  also.

The load on a transistor oscillator is usually magnetically or capacitively coupled into the tank circuit. The load determines both the power drawn from the oscillator and the loaded  $Q$  of the tank circuit. The ratio of loaded  $Q$  to unloaded  $Q$  for the tank circuit should be low for good circuit efficiency.

**Components of the Tank.** *Capacitors.* One of the most desirable types of capacitors for use in RF oscillators is the silvered-mica type. Since the silver plates are applied on the mica by vacuum evaporation, the silvered-mica capacitor is much more stable than ordinary mica capacitors with plates of foil pressed against the mica insulation. Mica has high secular<sup>†</sup> stability, a low temperature coefficient of capacity, and a low power factor. Typical values are  $+20$  ppm/ $^\circ\text{C}$  temperature coefficient and  $0.015\%$  power factor at 1 mc, over a range of  $-60^\circ\text{C}$  to  $+80^\circ\text{C}$ . Dielectric constants of 6 are typical. Very low parasitic inductance and d-c leakage (the leakage is principally over the surface of the plastic jacket) are features of the silvered-mica capacitor.

Ceramic capacitors offer two interesting advantages. Ceramic has, when mixed with titanium, negative temperature coefficients as high as  $750$  ppm/ $^\circ\text{C}$  and about 10 times greater dielectric constant than mica. These advantages lead to the following possibilities: First, owing to the negative temperature coefficient, some compensation can be made for the positive coefficient of most inductance coils. Second, since such high dielectrics are available, it is possible to obtain large capacitance in small noninductive structures. Secular stability is very good, and power factors range from  $0.02$  to  $0.05\%$  at 1 mc to  $0.04$  to  $0.1\%$  at 100 mc. The temperature coefficient with frequency is about constant between 1 and 100 mc.

*Inductance.* Normally, the capacitors used in LC tank circuits of RF oscillators have very low losses compared to the losses in the coil. For this reason, the unloaded  $Q$  of a resonator depends almost entirely on the  $Q$  of the coil. The exact design of a coil is quite complicated because of the many factors which must be considered. The coil must have the correct inductance and be stable with time and temperature. It must have low parasitic capacitance and a high, reasonably stable unloaded  $Q$ .

The form of inductance coil most frequently used in RF circuitry is the single-layer solenoid, although powdered iron cores are sometimes used for better  $Q$  or for a variable inductance. The inductance is determined by the number of turns

\* $Z_0$  is the antiresonant tank resistance.

<sup>†</sup>Secular stability is the property of a material which enables it to retrace its path when one of its parameters is cycled with respect to temperature.

and the geometry of the coil. The self-inductance and the resistivity will vary with the frequency because of proximity and skin effects. Since the resistivity of a conductor varies rapidly with temperature changes, the inductance of a coil may be very sensitive to temperature changes, even though no appreciable change occurs in its dimensions. The problem, therefore, is to design the coil so that its dimensions are independent of time, temperature, and atmospheric conditions. The current distribution through the wire cross section must also be independent of temperature over the range specified.

If severe vibration is not expected, a coil may be self-supported at one end and connected at the other end by flexible braid. This results in reasonably stable coils having low losses. If both ends are rigidly attached, temperature-expansion coefficients may become a problem.

As stated before, the self-inductance of a coil is a function of skin effect. Skin effect is, in turn, a function of conductivity. At high frequencies the penetration of current into the conductor is very shallow, while at low frequencies it may cover the entire cross section. The inductance is a function of both frequency and resistivity. Since this resistivity increases rapidly with temperature, the inductance also increases. The temperature coefficient of copper is about 4,000 ppm/°C, and the inductance coefficient due to this effect alone may be as high as 100 ppm/°C. At higher frequencies, where small inductance values are needed, sheet-copper strap is used to form the coil. This provides a large surface area and reduces skin effect for a given inductance.

Because it is expensive as well as difficult to build coils with low positive temperature coefficients of inductance, negative-temperature-coefficient capacitors are often used for compensation. This method is sometimes impractical, however, since the elements must track each other and must be reproducible in large-scale production.

Typically, a poorly built LC resonator may be affected by temperature so that its self-resonant frequency drifts by about 40 ppm/°C. The drift of a GT cut crystal will usually be 1/10,000 as great.

**Crystal Discussion.** When extreme frequency stability is required of an oscillator, a crystal is usually used as a substitute for the tank circuit or in the feedback loop to stabilize the frequency. The tolerance on most commercial crystals is about 0.002% from -55 to +90°C. An example of a Colpitts-Pierce crystal-oscillator configuration is shown in Fig. 7. Here the crystal is operated at a frequency just slightly below its parallel resonant frequency so that it will appear as an inductance.

The equivalent circuit for a crystal is shown in Fig. 8.

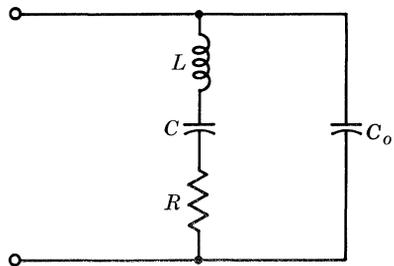


Fig. 8. Equivalent circuit of a quartz crystal.

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The L is analogous to the mass of the crystal structure, C is analogous to the crystal elasticity, and R is analogous to mechanical friction, accounting for energy lost as heat in the crystal.  $C_o$  is the total effective shunt capacitance contributed by the distributed capacitance of the leads and terminals of the mounting structure, the nonvibrating electrostatic capacitance across the quartz-crystal faces with the quartz serving as the dielectric, and any capacitance added by the crystal holder.

Crystals may also be operated at certain overtones of the fundamental, but even though the overtone Q is approximately the same as the fundamental Q, the activity or piezoelectric effect will be progressively smaller, the higher the overtone. Also, since in the parallel mode the activity is inversely proportional to the square of the terminal capacitance, care should be taken to minimize external capacitance so as to preserve crystal activity.

In RF circuits, the dissipation must often be held to a few milliwatts. Temperature coefficients are normally specified in the form of Eq. (10):

$$\text{Drift} = \frac{\Delta f/f_o}{\Delta T} \quad (10)$$

In other words, the specification is in parts per million per degree or in per cent per degree. This coefficient can be positive, negative, or zero over small temperature ranges, depending on the crystal cut. Crystal-oscillator design will not be elaborated here, in view of the wide range of crystal types and possible circuits.

### ACTIVE DEVICE

**Requirements.** The primary function of the active device is to develop enough output power at the frequency of operation to supply the required load power, the tank losses, and the drive power for itself. It should also generate as little noise voltage as possible. The active device should have a maximum frequency of oscillation well above the design frequency. Because these requirements are rather loose, many transistor types will function properly as oscillators. However, certain types of manufacturing processes result in device parameters which yield better oscillator performance. Paramount among these is the epitaxial mesa technique which allows a relatively lower value of effective collector bulk resistance, permitting higher operating efficiency.

**Parameter Variation.** At low frequencies the transistor parameters in the characteristic equation do not have large imaginary components, but at RF frequencies these parameters must be inserted in the characteristic equation in complex form. Solution of the real and imaginary parts, therefore, will include the effects of input, output, and transfer immittances. The sensitivity of frequency and starting conditions to changes in any of these immittances with the temperature, age, or bias point can be evaluated. Examination of Table 1 and the design example shows the form of these equations and the specific parameters involved.

### FREQUENCY STABILITY

**Causes of Frequency Instability.** Oscillator frequency stability is a measure of the amount of drift in frequency away from the design center value. There are two causes of drift. First, the active parameters may change. The equations for  $\omega^2$  in Table 1 indicate the particular active parameters involved. Inserting actual

Table 1.

Circuit	Natural frequency ( $\omega^2$ )	Starting condition
Colpitts .....	$= \frac{1}{LC} + \frac{r}{L} \frac{1}{C_1 h_{ie}} + \frac{\Delta h_e^*}{C_1 h_{ie}} + \frac{h_{oe}}{C_1 C_2 h_{ie}}$ $\cong \frac{1}{LC} \left( 1 + \frac{L C h_{oe}}{C_1 C_2 h_{ie}} \right)$ <p>where <math>C = \frac{C_1 C_2}{C_1 + C_2}</math></p> <p>and <math>r =</math> a-c series resistance of coil <math>L</math></p>	$h_{fe} > \frac{r(C_1 + C_2) h_{ie}}{L} + \frac{C_2}{C_1} + \frac{C_1}{C_2} \Delta h_e \cong \frac{C_2}{C_1}$
Colpitts .....	$= \frac{1}{LC} + \frac{h_{ob}}{h_{ib} C_1 C_2} \cong \frac{1}{LC}$	$h_{fb} > \frac{-C_2}{C_1 + C_2}$
Hartley (tapped) .....	$= \frac{h_{ie}}{C(L h_{ie}) + (L_1 r_2 + L_2 r_1) h_{fe} + (L_1 L_2 - M^2) h_{oe}}$ $\cong \frac{1}{LC + (L_1 L_2 - M^2) \frac{h_{oe}}{h_{ie}}}$ <p>where <math>L = L_1 + L_2 + 2M</math></p> <p><math>r_1 =</math> a-c series resistance of coil <math>L_1</math></p> <p><math>r_2 =</math> a-c series resistance of coil <math>L_2</math></p>	$h_{fe} > \frac{r L C h_{ie} + (M + L_1)^2 + (L_1 r_2 + L_2 r_1) \frac{\Delta h_e^*}{h_{ie}}}{(L_1 + M)(L_2 + M)}$ $\cong \frac{L_1 + M}{L_2 + M} \cong \frac{1 + KN}{1/N^2 + KN}$ <p>where <math>K = \frac{M}{\sqrt{L_1 L_2}}</math></p> $N = \sqrt{\frac{L_2}{L_1}}$
Hartley (tapped) .....	$= \frac{1}{LC + (h_{ob}/h_{ib})(L_2 L_1 - M^2)} \cong \frac{1}{LC}$ <p>where <math>L = L_1 + L_2 + 2M</math></p>	$h_{fb} > \frac{L_1 + M}{L_1 + L_2 + 2M} \cong -\frac{N_1}{N_2}$ <p>where <math>N_1 =</math> number of turns of <math>L_1</math></p> <p><math>N_2 =</math> number of turns of <math>L_2</math></p>
Clapp .....	$\cong \frac{1}{LC} + \frac{1}{L} \frac{C_1 + C_2}{C_1 C_2}$ <p>where <math>C =</math> series capacity with <math>L</math></p>	$h_{fb} > -\frac{C_2}{C_1 + C_2} \quad h_{fe} > \frac{C_2}{C_1}$

\* $\Delta h_e =$  common-emitter determinant  $= h_{ie} h_{oe} - h_{re} h_{fe}$ .

values gives an indication of their influence. Second, the passive parameters may change. Both active and passive parameters generally change for two reasons: temperature and age.

**Specification of Frequency Stability.** An explicit expression for frequency variation with temperature is given in Eq. (11).

$$\text{Drift} = \frac{\Delta f/f_o}{\Delta T/T_o} \quad (11)$$

This expression gives the sensitivity of center frequency,  $f_o$ , to temperature change at a particular center frequency and operating temperature. Another expression that can be used is given in Eq. (12),

$$\text{Drift} = \frac{\Delta f/f_o}{\Delta T} \quad (12)$$

usually expressed as parts per million per centigrade degree.

**Techniques for Improving Frequency Stability.** As mentioned earlier, minimization of active device influence will improve stability. For the Colpitts connection, this is satisfied by the following inequality:

$$\frac{h_{ob}}{h_{ib}C_1C_2} < \frac{C_1 + C_2}{LC_1C_2} \quad (13)$$

Similar inequalities for other oscillator connections may be found from Table 1. Selection of an active device which satisfies this inequality is therefore the first technique.

The second technique is to *swamp out* part of the particular active parameter which enters the frequency expression by putting appropriately sized resistances in series with  $h_{ib}$  and in parallel with  $h_{ob}$ . The characteristic equation below shows the effect of this approach.

$$(h_{ib} + R_1 + h_{11p})(h_{ob} + \frac{1}{R_2} + h_{22p}) - (h_{rb} - h_{12p})(h_{fb} - h_{21p}) = 0 \quad (14)$$

Now if  $h_{ib} < R_1$  and  $h_{ob} < 1/R_2$ , the equation becomes

$$(R_1 + h_{11p})(G_2 + h_{22p}) - (h_{rb} - h_{12p})(h_{fb} - h_{21p}) = 0 \quad (15)$$

The resonant frequency is solved for in the same way, except that now  $R_1$  and  $G_2$  are the terms in the expression instead of  $h_{ob}$  and  $h_{ib}$ .

The effect of load change on frequency may be shown by inserting  $Y_L$  into the characteristic equation. This is shown in Eq. (16).

$$(h_{ib} + h_{11p})(h_{ob} + h_{22p} + Y_L) - (h_{rb} - h_{12p})(h_{fb} - h_{21p}) = 0 \quad (16)$$

If  $Y_L < (h_{ob} + h_{22p})$ , its change will be minimized in the expression for frequency. This condition is generally established by a buffer stage. On the other hand, the solution of Eq. (16) for  $Y_L$  will yield the maximum load conductance which will still satisfy the conditions for oscillation. This load is important if the oscillator is intended as a power source rather than as a frequency source.

## OSCILLATOR DESIGN PROCEDURE

**Discussion.** The design procedure for transistor oscillators is usually treated on a linear basis even though self-sustained oscillation indicates nonlinear operation. Therefore, the preliminary design calculations provide only approximate values for components, and these components must be adjusted experimentally in the final design.

Since a design procedure must be tailored to the individual oscillator specification no exact procedure can be given other than the general steps involved. The following is a listing of these design steps:

### Design Steps

1. Select a transistor capable of providing sufficient gain and desired power output at the operating frequency, based on data sheet specifications.
2. Select the oscillator configuration to be used, based on the application. For example, the oscillator will probably be used either as a frequency-determining element or as a source of power at a given frequency.
3. Design the d-c bias network to establish the bias point and provide the necessary stability.
4. Design the tank or frequency-determining network using the formulas for operating frequency and starting conditions given in "Oscillator Configurations" and in Table 1. The table gives natural frequency ( $\omega^2$ ) and starting conditions in terms of h parameters.
5. Make necessary adjustments in the feedback and bias networks to optimize efficiency. Be sure not to sacrifice ease of starting when adjusting the bias network for possible class B or C operation.
6. Use a trimming capacitor to make final adjustments, if necessary, to oscillator frequency.

### DESIGN EXAMPLE

Specifications for the low-power oscillator design example are as follows:

$$\begin{aligned} f_o &= 90 \text{ mc} \\ V_o &= 2V_{(\text{rms})} \text{ across a 1,000-ohm load} \\ V_{CC} &= 10 \text{ volts} \end{aligned}$$

The design procedure is as follows:

1. Select the 2N743 to provide this specified output power and voltage. It has an  $f_t$  which is, at the normal bias point of 5 volts and 5 ma, about three times  $f_o$ .
2. The Colpitts connection is selected for this frequency range because it yields values of tank inductance and capacitance which should be fairly insensitive to transistor parameter variation. The circuit configuration is shown in Fig. 9.
3. The d-c values for the network are as follows:  
Let the drop across  $R_3$  be 2.5 volts.

$$R_3 = \frac{2.5 \text{ volts}}{5 \text{ ma}} = 500 \text{ ohms}$$

Let the current through  $R_1$  and  $R_2$  be 5 ma, so that the value of  $R_2$  will be

$$R_2 = \frac{3.1 \text{ volts}}{5 \text{ ma}} = 620 \text{ ohms}$$

This leaves  $V_{R1} = 10 - 3.1 = 6.9$  volts; if  $I_B$  is about 0.4 ma,

$$R_1 = \frac{6.9 \text{ volts}}{5.4 \text{ ma}} = 1.3 \text{ kilohms}$$

$R_4$  will have about 2.5 volts across it; therefore,

$$R_4 = \frac{2.5 \text{ volts}}{4.5 \text{ ma}} = 550 \text{ ohms}$$

4. The a-c circuit design is carried out as follows: Since  $R_2$  is 620 ohms, adequate bypass is about 5 ohms. This gives  $C_1 = 300$  pf; to avoid a self-resonant frequency at or around 90 mc,  $C_1$  must have a total lead length less than 0.4 ma.  $C_4$  and  $C_5$  are 500-pf feed-through capacitors.

At 5 volts, 5 ma, and about 90 mc, the  $h_b$  parameters for the 2N743 are:

$$h_{ib} = 21.3 \angle 45.6^\circ = (15.2 + j15) \text{ ohms} \tag{17}$$

$$h_{rb} = 0.069 \angle 77^\circ = 0.0672 + j0.0154 \tag{18}$$

$$h_{fb} = 0.97 \angle 182.3^\circ = -0.969 - j0.039 \tag{19}$$

$$h_{ob} = 2.76 \times 10^{-3} \angle 15.3^\circ = (2.66 + j0.73) \times 10^{-3} \text{ mho} \tag{20}$$

The expression for  $\omega^2$  is

$$\begin{aligned} \omega^2 &= \left( \frac{h_{ib}}{L} + \frac{h_{ob}}{C_1 + C_2} \right) \frac{C_1 + C_2}{C_1 C_2} \frac{1}{h_{ib}} \\ &= \frac{1}{L} \frac{C_1 + C_2}{C_1 C_2} + \frac{h_{ob}}{h_{ib} (C_1 C_2)} \\ &= \frac{1}{L C_1 C_2 / C_1 + C_2} + \frac{1}{h_{ibr} / h_{obr} (C_1 C_2)} \end{aligned} \tag{21}$$

By experimentally adjusting the capacitance ratio of the tank, we found that the following ratio gave the desired signal across the 1-kilohm load:

$$\frac{C_2}{C_3} = \frac{43}{91} = 0.47 \quad \frac{C_2 C_3}{C_2 + C_3} = \frac{(43)(91)}{134} = 29 \text{ pf}$$

The inductance is  $0.11 \mu\text{h}$  ( $\cong 2$  turns no. 18 wire on  $\frac{1}{2}$  in. diameter.)  $V_o = 2$  volts across the 1-kilohm load.

In order to determine the effect of the transistor parameters on the frequency of oscillation, we will compare the values obtained from the following expressions.

Frequency determined by considering only the tank:

$$\omega^2 = \frac{1}{L[C_1C_2/(C_1 + C_2)]}$$

$$\omega_o^2 = \frac{1}{(0.11 \times 10^{-6})(29 \times 10^{-12})}$$

$$f_o = \frac{1}{(6.28)(3.2 \times 10^{-18})^{1/2}} = \frac{1}{(6.28)(1.79)10^{-9}} = 90 \text{ mc}$$

Using  $h_{ibr}$  and  $h_{obr}$  equal to 15.2 ohms and  $2.66 \times 10^{-3}$  mho, respectively,

$$\omega_o^2 = \frac{1}{L[C_1C_2/(C_1 + C_2)]} + \frac{1}{(h_{ibr}/h_{obr})(C_1C_2)}$$

$$= \frac{1}{(0.11 \times 10^{-6})(29 \times 10^{-12})} + \frac{1}{(15.2/2.66) 3.94 \times 10^{-18}}$$

$$= 0.313 \times 10^{18} + 0.044 \times 10^{18}$$

$$\omega_o^2 = 0.359 \times 10^{18} \quad f_o = 95.4 \text{ mc}$$

Evaluation of the operating frequency, using the full set of complex values for the  $h$  parameters, indicates that the frequency is still almost completely determined by the tank components. Experimental measurements of frequency agreed very well with the predicted value. Figure 9 shows the circuit.

**ADDITIONAL CIRCUITS AND PERFORMANCE**

**23-mc Oscillator.** The 23-mc push-pull oscillator of Fig. 10 was designed to deliver 75 mw to a 50-ohm load. A  $\pi$ -matching network is used to optimize the output to a 50-ohm load with a noncritical design for the output transformer. Transistor type used is the Dalmesa 2N2188.

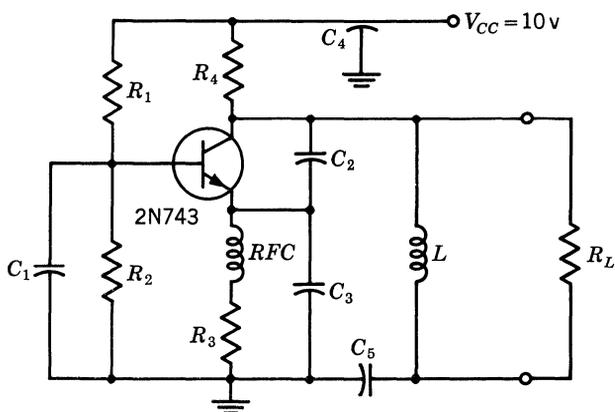


Fig. 9. 95-mc oscillator. Circuit uses a silicon epitaxial mesa to deliver about 2 volts (rms) across a 1-kilohm load at 95 mc. Typical circuit efficiency  $\cong$  3%.

## 50 Communications Handbook

**24-mc Oscillator.** Figure 11 shows a 24-mc Clapp oscillator designed to deliver 300 mw into a 50-ohm load. Typical collector efficiency is 35%. The transistor type used is the 2N696.

**30-mc Oscillator.** Figure 12 shows a 30-mc oscillator designed to operate over a temperature range of  $-40$  to  $+60^{\circ}\text{C}$ . Typical power out is 23 mw at  $-40^{\circ}\text{C}$  and 20 mw at  $+60^{\circ}\text{C}$ . Typical collector efficiency is 30%. Transistor type used is the Dalmesa 2N2188.

**60-mc Oscillator.** The common-base circuit in Fig. 13 is a 60-mc oscillator designed to deliver approximately 10 mw to a 50-ohm load at  $25^{\circ}\text{C}$ . Collector efficiency is typically 8 to 10%. Transistor type used is the Dalmesa 2N2188.

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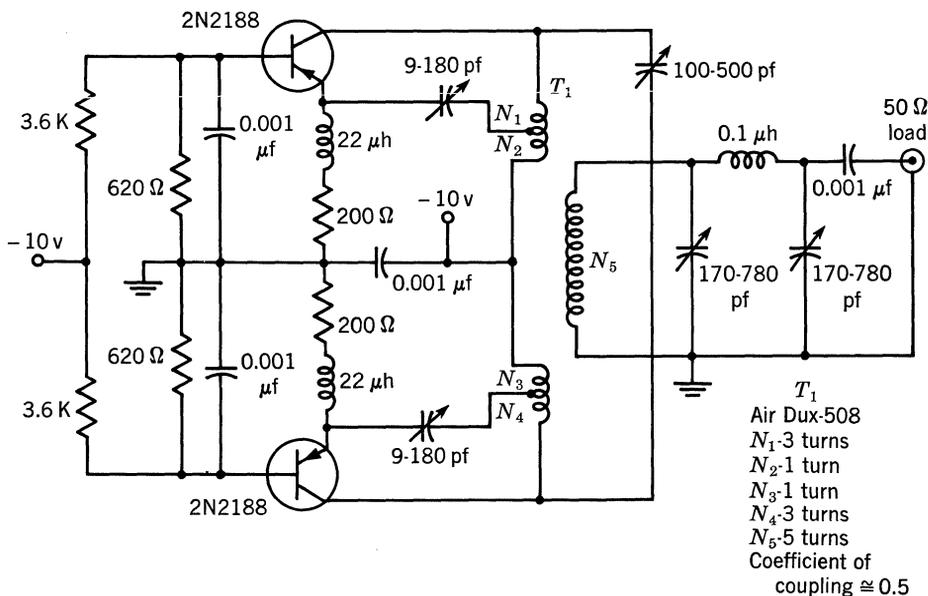


Fig. 10. 23-mc push-pull oscillator.

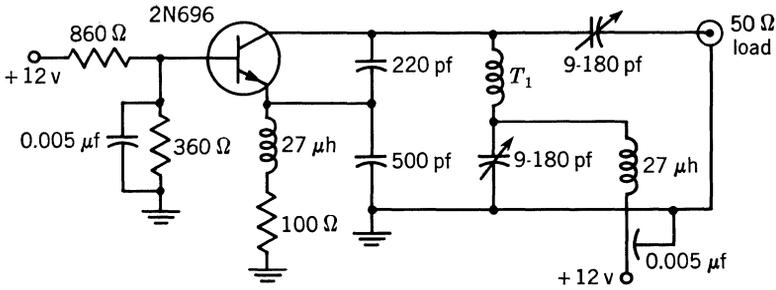


Fig. 11. 24-mc oscillator.

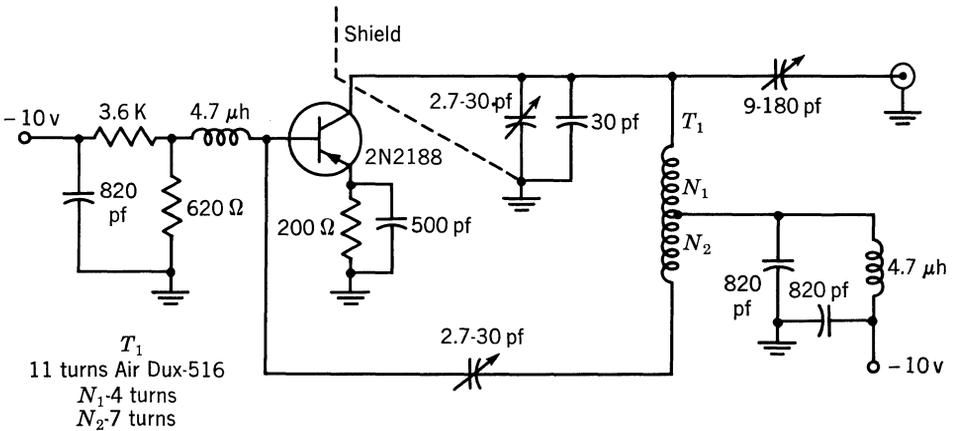


Fig. 12. 30-mc oscillator.

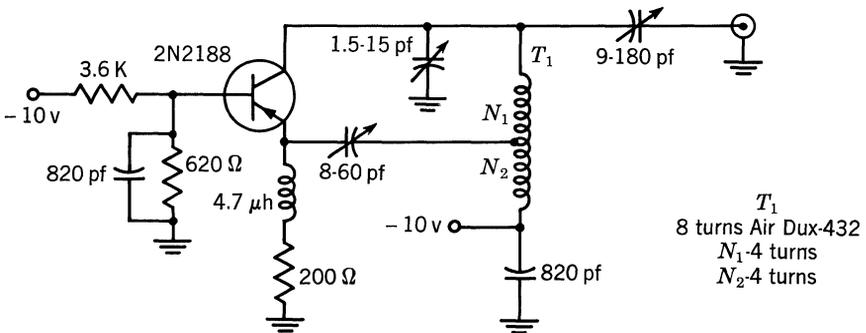


Fig. 13. 60-mc oscillator.

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**A bank of diffusion furnaces, one of several such installations that give TI unparalleled diffusion capacity.**

# Transistors in Wide-band Low-distortion Amplifiers

by Roger Webster

## INTRODUCTION

Line amplifiers used for repeaters or multicouplers are characterized by:

1. Wide bandwidths
2. Very low distortion and intermodulation products
3. Modest output power level
4. Modest power gain
5. Wide dynamic range

The frequency spectrum of the amplifiers to be discussed extends from a few hundred Kc to 30 Mc or higher. Intermodulation products should be down 60 db or more at maximum signal levels. The output power level is in the order of 10 to 50 mw and the gain is in the order of 10 to 15 db.

The dynamic range is a function of the difference between system noise and the maximum signal handling capability. For a given maximum signal level, dynamic range will be maximum for a system with lowest noise figure.

## GENERAL CONSIDERATIONS

**Type of Transistor.** Linear operation over a wide range of frequencies is a prime consideration. Operating the transistor at fairly high currents and voltages serves to restrict current and voltage swings to a small percentage of the operating point, and generally enhances linearity. For these and other reasons to be discussed later, the desirable transistor characteristics may be summarized as follows:

1. Fairly substantial dissipation capability
2. Fairly high current and voltage rating
3. High cutoff frequency relative to operating frequency
4. Fairly low capacitance
5. The following parameters should be as independent of operating point (i.e., current and voltage) as possible:

- a. current gain
  - b. base resistance
  - c. cutoff frequency
  - d. capacitance
  - e. emitter and collector body (parasitic) resistance.
- 6. Low collector-base leakage current
  - 7. High d-c current gain
  - 8. Low base resistance

Although either silicon or germanium might be used, requirements 1 and 2 can more easily be met with silicon in a small-area, low-capacitance device. Low capacitance is important because of the requirement that the device operate at reasonably high frequencies. Characteristics 6, 7, and 8 are included because transistor applications require low-noise devices.

**Configuration.** The common-base connection is clearly superior for greatest linearity and smallest gain variation with frequency. A comparison of the common-emitter and common-base transfer characteristics will demonstrate the inherent advantage of common-base operation. Figure 1 shows such a comparison.

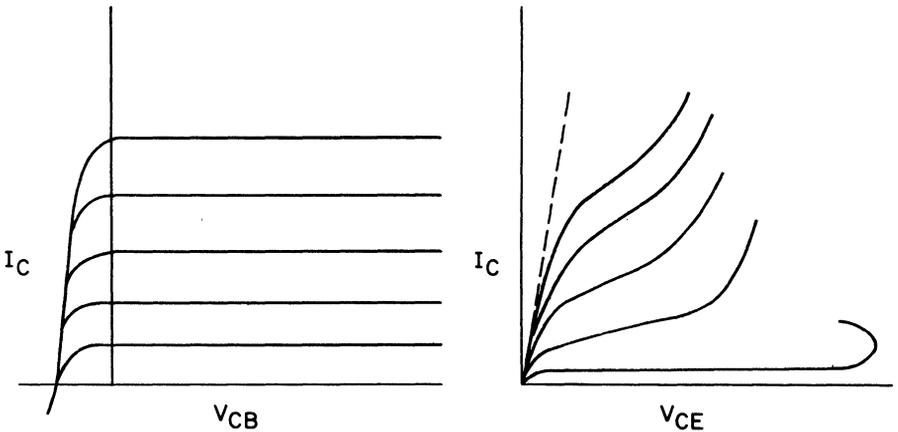
Fortunately, gain requirements are usually modest and, thus, common-base operation is satisfactory. A further advantage of common-base operation is that gain is primarily determined by an impedance transformation ratio, which is determined by the external circuit rather than the device. A still further advantage is that the output impedance of the common-base stage is both much higher and more independent of operating point than is the common-emitter output impedance.

**DISTORTION ANALYSIS**

**Generation of Harmonics and Intermodulation Products.**

Harmonics, cross modulation and intermodulation products are produced by non-linearity in the input-output characteristics. The three principle effects ordinarily considered are:<sup>1</sup>

*First order:* Output is strictly proportional to input. No intermodulation or cross modulation products exists.



**Fig. 1. Common-base and common-emitter characteristics.**

*Second order:* Output is proportional to the square of the input signal, and to curvature of the transfer characteristics. It generates a d-c component, second harmonics, and sum and difference frequencies if two input signals are present.

*Third order:* Output is proportional to the cube of the input signal, and to rate of change of curvature of the transfer characteristics. It generates third harmonics and odd-order combination frequencies if two input signals are present (e.g.,  $2\omega_a \pm \omega_b$  or  $2\omega_b \pm \omega_a$ ).

Since there is a fundamental component proportional to the cube of the input signal, the total output at the fundamental is not proportional to the input. Moreover, when two signals are present, the amplitude of the first is dependent upon the amplitude of the second, giving rise to cross-modulation.

Higher-order components cause similar effects. Even orders generate even harmonics, d-c components, and even-order combination frequencies, while odd orders generate odd harmonics, odd-order combination frequencies, lack of proportionality between input and output, and cross-modulation.

As a practical matter, second-order and all higher even-order effects may be substantially reduced by a balanced push-pull circuit. Thus the third-order effect is ordinarily the dominant effect in the class of amplifiers described here.

**Sources of Distortion in Transistors.**

1. *Nonlinear input characteristics:*

a. Emitter-base diode characteristics:

The emitter-base diode has the usual semiconductor diode exponential current-voltage relationship. Ideally, this relationship is:

$$I = I_0 \left( e^{\frac{qV}{kT}} - 1 \right) \tag{1}$$

A series expansion of this relationship shows that all harmonics are present in the current flow for a sinusoidal applied voltage. The relative magnitude of the harmonics is proportional to the applied voltage. When two sinusoidal voltages are applied, intermodulation and cross modulation products are also generated.

When  $e^{\frac{qV}{kT}} \gg 1$ , the rate of change of current in the ideal diode is:

$$\frac{dI}{I} = \frac{q}{kT} dv \tag{2}$$

Thus, in the ideal diode, the curvature of the diode characteristic for a given change in voltage is independent of the current. As a result, the relative magnitudes of the distortion components are functions only of the applied signal voltages, and are independent of the operating current.

In any practical structure, the foregoing statements must be modified considerably. This will be discussed further in a following section on the influence of the operating point.

b. Non-constant base resistance:

Any variation in base resistance will cause a corresponding variation in the input impedance. Variations in base resistance result primarily from (1) modulation of resistivity by heavy injection of minority carriers, and (2) base-width modulation. There are at least two different causes of base-width modulation. A variation in base width results because the collector-base junction depletion layer width is dependent on applied voltage. As voltage changes, the location of the edges of the junction depletion layer moves. This is known as the "Early" effect<sup>2</sup> and is shown in Fig. 2. Base-width modulation is also caused by the inability of the collector depletion region or the collector body, or both, to support more than some finite current density without radical changes in internal parameters. The depletion layer contracts and tends to move into the collector body, thus in effect widening the base.<sup>3</sup>

2. *Non-constant transfer characteristics:*

Not all of the emitter current is injected into the base, nor does all of the injected current reach the collector, nor is the collector current all injected current. This may be expressed as follows:

$$\alpha = \alpha^* \beta \gamma \tag{3}$$

where  $\alpha$  = emitter-collector current gain

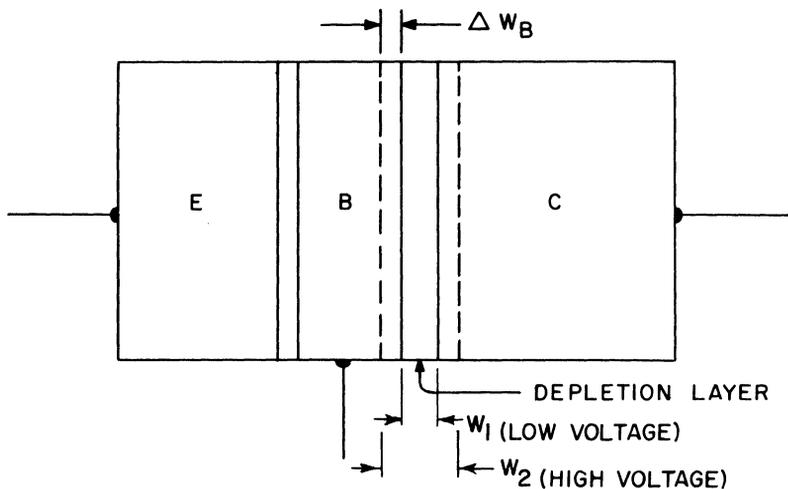
$\alpha^*$  = collector multiplication factor

$\beta$  = base transport efficiency

$\gamma$  = emitter injection efficiency

The fact that none of these factors is unity is not a problem in itself. However, these factors are not constant and depend on terminal currents and voltages. This results in non-constant transfer characteristics and nonlinear distortion. Some of the factors influencing each of these will be discussed in the following paragraphs.

Variation of emitter injection efficiency results from a variation in the total number of base impurities as seen by the emitter. This is caused by base-width



**Fig. 2. Early effect — base width modulation.**

modulation and base-conductivity modulation. Both of these were discussed in the previous section.

The variation of base transport efficiency also results in a corresponding change in current gain and, thus, a nonlinear transfer characteristic. This variation is primarily caused by base-width modulation. Since high-frequency current gain (common emitter) is inversely proportional<sup>2</sup> to base width, current gain may vary considerably. In common base, this may be manifested largely as a phase-angle modulation.

Collector multiplication may result from a number of factors. The most significant of these in modern transistors is collector junction avalanche multiplication. Collector avalanche multiplication occurs in the collector-base junction; thus it is out of the input-signal path. The multiplication factor is voltage dependent. For these two reasons, avalanche multiplication generates unwanted distortion components.

3. *Non-constant output characteristics:*

It may be shown analytically and experimentally that many of the previous variations will also influence the output impedance. This, in turn, introduces distortion components into the signal.

**Influence of the Operating Point.**

1. *Reduction of distortion components:*

Earlier, in discussing nonlinear input characteristics, it was shown that in the ideal diode the relative magnitudes of the distortion components are independent of the operating point. This is not true of practical structures because series impedances in the structure (notably base resistance) considerably modify the terminal characteristics. Consider the simple equivalent transistor input circuit shown in Fig. 3.<sup>4</sup>

$$I = I_0(\exp \frac{qV}{kT} - 1)$$

WHEN  $V \gg \frac{q}{kT}$

$$\frac{dI}{I} = \frac{q}{kT} dV$$

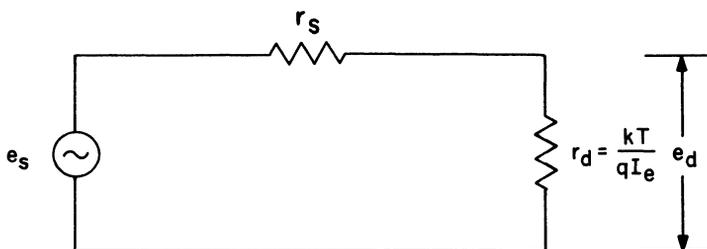


Fig. 3. Simple transistor input equivalent circuit.

In Fig. 3,  $e_s$  is an applied signal voltage,  $r_s$  is an equivalent series resistance,  $r_d$  is the emitter diode impedance, and  $e_d$  is the signal voltage appearing across the diode.

At large emitter currents,  $r_d \ll r_s$ , and in the simple voltage divider circuit shown:

$$e_d \propto \frac{1}{I_e} \tag{4}$$

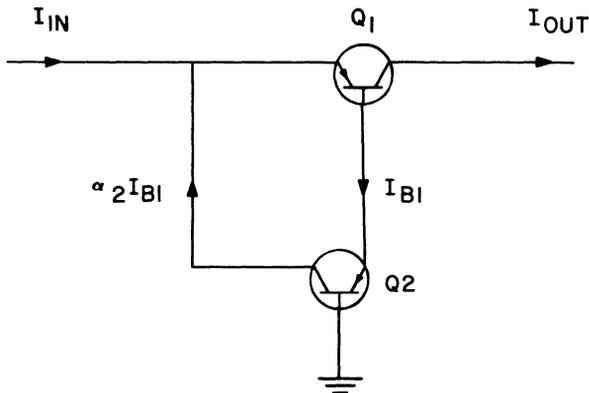
Therefore, operation at high emitter current reduces distortion by virtue of the fact that the applied signal voltage across the diode proper is reduced. Two factors oppose increasing operating current indefinitely. Shot noise generated in the emitter-base and collector-base diodes is directly proportional to current, so that noise figure is degraded by increasing the operating current. Moreover, nonlinearities eventually appear in the transfer characteristics as current is increased. This leads to increased distortion components.

2. *Cancellation or reduction of certain distortion products:*

D. R. Fewer was the first to show that the second-order distortion products may be reduced substantially by proper selection of source impedance and emitter current.<sup>5</sup> However, the exact point at which this occurs is dependent on the individual transistor. Moreover, the third-order components do not show such a minimum, but in general tend to decrease as emitter current is increased. It therefore appears more practical to use balanced push-pull pairs to cancel second-order products, and to operate the transistors in a region of low third-order distortion.

**CIRCUIT ARRANGEMENTS FOR DISTORTION REDUCTION**

Boxall described a method for distortion reduction in which the base current of a common-base output stage is fed back into the input.<sup>6</sup> The base current is an exact measure of how far the collector current departs from the input current. If the input current represents exactly what is to be reproduced, then reinserting the base current at the input will give an output current which is an exact reproduction of the input current. Figure 4 shows how the reinsertion may be accomplished. The d-c circuitry is omitted for clarity.



**Fig. 4. Base current feedback.**

If the current gain of  $Q_2$  is close to unity, the desired effects are accomplished. The results of such a feedback arrangement are to:

1. make the effective overall current gain close to unity. If  $\alpha_T$  is the overall current gain, then:

$$\alpha_T = \frac{\alpha_1}{1 - \alpha_2(1 - \alpha_1)} \quad (5)$$

2. raise the effective output impedance:

$$Z_T = Z_1 \frac{1 - \alpha_2(1 - \alpha_1)}{1 - \alpha_2} \cong Z_1 \frac{\alpha_1}{1 - \alpha_2} \quad (6)$$

where  $Z_1$  is the open-circuit output impedance of  $Q_1$  without feedback.

3. lower the distortion current flowing in the output:

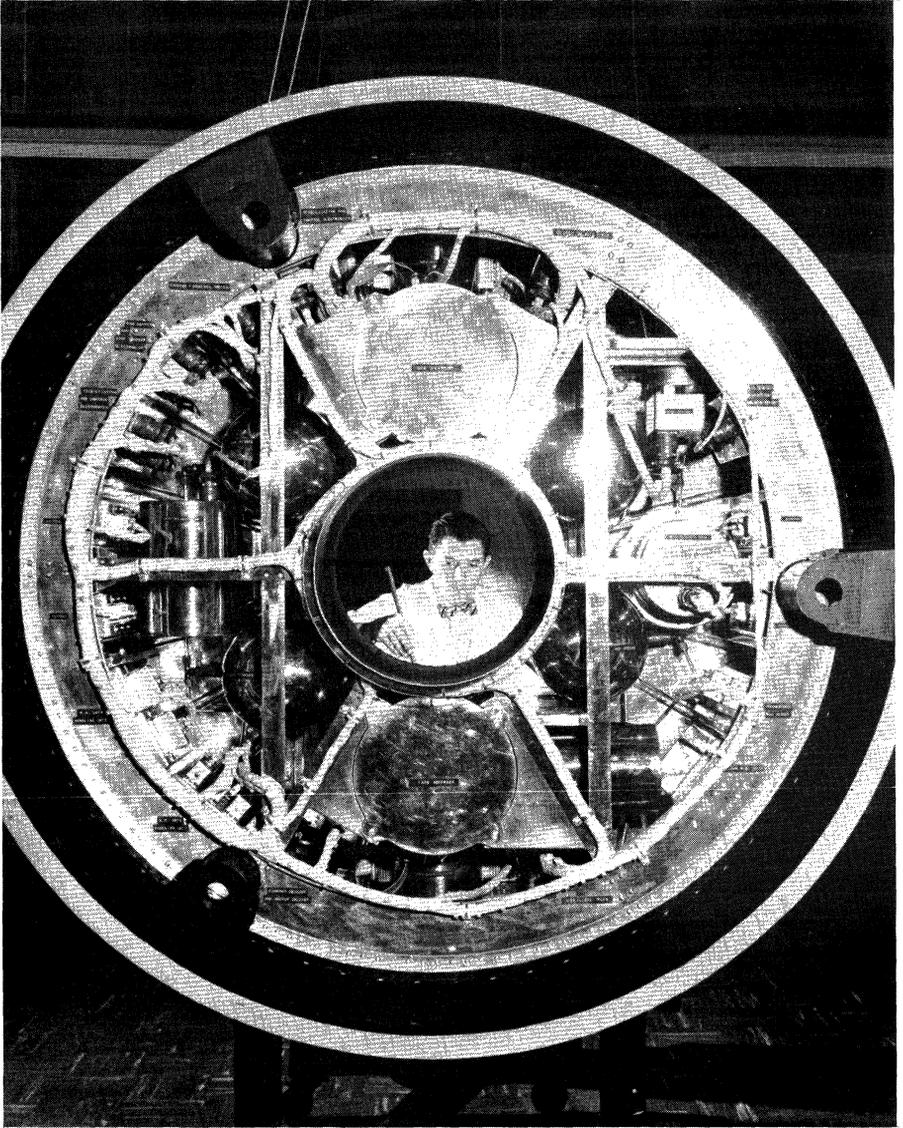
$$D_T \cong (1 - \alpha_2)D_1 \quad (7)$$

where  $D_1$  is the per-unit distortion current flowing in the output without feedback.

Aldridge has shown a variation of this arrangement which he calls a "cascade" circuit.<sup>7</sup> Distortion reduction of 15 db of third-harmonic components at high frequencies is realized.

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## VHF and UHF Amplifiers and Oscillators Using Silicon Transistors

by Harry F. Cooke

### INTRODUCTION

The amplifiers, oscillators, and signal sources to be discussed in this chapter cover a variety of applications at frequencies from 500 Mc through X band. These include wide-band, low-noise amplifiers, oscillators delivering 50 mw at 2 Gc, harmonic power up to 25 mw at 4 Gc and (with a varactor multiplier) up to 25 mw at 9.2 Gc.

The transistors used in these applications are a new generation of UHF silicon devices.

### THE TI 3016A AND 2N3570

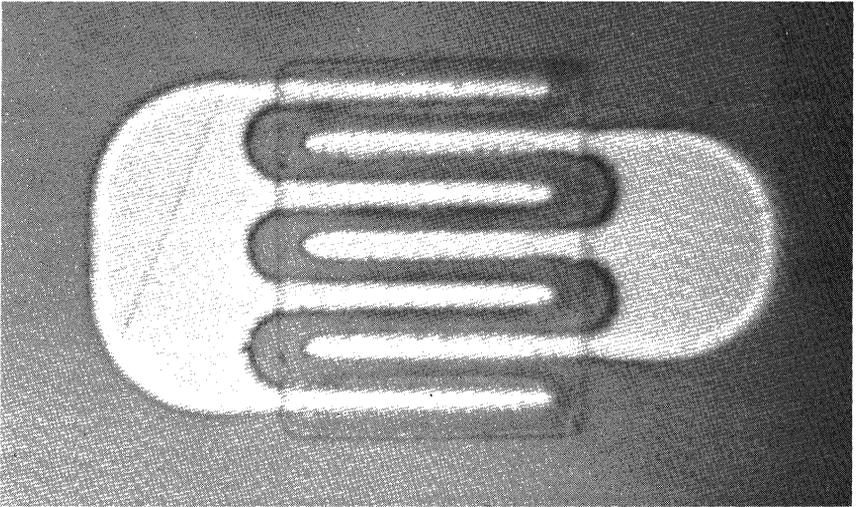
The TI3016A and 2N3570 are identical electrically, but are supplied in different packages (TI-line\* and TO-18, respectively). These devices are planar-epitaxial silicon transistors that feature very small dimensions made possible by advanced photomasking techniques. Interdigitated base and emitter contacts result in very low base resistance. Figure 1 is a photograph of the completed silicon chip. Four base fingers and three emitter fingers are clearly seen, as well as the expanded areas for making external contacts. The total area of the base diffusion window is 7.2 sq mils.

The outstanding performance of this unit results from the following high-frequency parameters:

1. very high cutoff frequency:  $f_T \cong 1.8$  Gc
2. very low base resistance:  $r_b' \cong 10$  to 20 ohms
3. low capacitance:  $C_C \cong 0.5$  pf

These parameters are the result of the very narrow base (base width is in the order of 0.01 mils) and the other very small dimensions. The electrical charac-

\*Trademark of Texas Instruments



**Fig. 1. 2N3570, TI3016A geometry showing the four base fingers and three emitter fingers.**

teristics of this unit are summarized in Table 1.

Some of the design considerations involved in the TI3016A are of interest:

1. *High cutoff frequency:* Several structure-determined time constants are involved in cutoff frequency. The most important of these is the base width. An important phase of the development of this transistor was the development of suitable base and emitter diffusions so that a base width of about 0.01 mil could be consistently realized.

**Table 1. Characteristics of 2N3570 and TI3016A**

	2N3570 (TO-18 package) (Useful to 1.5 Gc and then package limited)			TI3016A (TI-line package)		
	Min.	Typical	Max.	Min.	Typical	Max.
$BV_{CBO}$	30 v (10 $\mu a$ )			30 v (10 $\mu a$ )		
$h_{FE}$ (6 v, 5 ma)	20		200	20		200
$r_b'C_c$ (6 v, 5 ma)	5 psec		8 psec	5 psec		
$f_T$ (6 v, 5 ma)	1.5 Gc	1.7 Gc		1.7 Gc		
NF 1 Gc (6 v, 2 ma)	6.0 db		7.0 db	6.0 db		
$F_{max}$	4 Gc			4 Gc		
$P_o$ (1 Gc, 20 v, 15 ma)	60 mw			30 mw (2 Gc)		

2. *Low base resistance:* For convenience, the base resistance may be separated into two components: that part underneath the emitter and that part between the emitter and base contacts. The first part may be minimized by using very narrow emitters. The emitter width is about 0.1 mil in the TI3016A. The second part is minimized by close spacing between emitter and base contacts and by paralleling many paths. The spacing between emitter and base contacts is 0.2 mils in these units, and the interdigitated geometry provides six parallel paths.

Base resistance may also be lowered by proper diffusion profile, although other factors must be considered. The TI3016A has a very heavy concentration of impurities in the base and a very shallow diffusion front. These lower the resistivity of the base, particularly under the emitter where an appreciable portion of the base resistance usually exists.

By combining an optimum diffusion profile with interdigitated geometry, a small-signal silicon transistor with  $r_b'$  in the order of 15 ohms has been realized.

3. *Low capacitance:* Low capacitance is a desirable feature in any high-frequency device. The most effective way to reduce capacitance is to reduce the junction areas. The junctions of the TI3106A and 2N3570 are quite small; the actual areas are:

Collector-base junction area  $\cong 7.2$  sq mil

Emitter-base junction area  $\cong 0.9$  sq mil

It is possible to reduce collector capacitance by raising collector resistivity, or by increasing the collector-base voltage. There are practical limits to these changes, however, and other factors must be considered. Among these are collector series resistance, and behavior of the device at various voltages and currents (which is influenced by the width resistivity of the collector epitaxial region).

## LARGE-SIGNAL BEHAVIOR OF TI3016A

These devices work well as large-signal oscillators and amplifiers. The factors that influence large-signal behavior are discussed here, along with some modifications to the basic structure which will permit even higher outputs.

**Variation of Parameters.** Under large-signal conditions, the a-c signal is of sufficient magnitude to influence the d-c operating point of the amplifier or oscillator. It is important, therefore, that the parameters be as nearly independent of current and voltage as possible. For example, the high-frequency current gain is always current and voltage dependent to some degree, but proper use of epitaxial techniques will tend to minimize this dependence.

At large-signal levels and high emitter currents, the input impedance of a transistor is essentially  $r_b'$ . Since this is a loss resistance, it is important to keep  $r_b'$  low — even more important than in the small-signal case. The collector capacitance  $C_c$  is voltage dependent and may vary considerably as the collector voltage swings with large signals. This effect is generally secondary compared to other effects, but may be useful to enhance harmonic generation.

**Dissipation.** Although the TI3016A and 2N3570 are relatively efficient devices and will deliver appreciable power at microwave frequencies, it is of interest to consider methods for increasing power handling capability.

Obviously, the package must provide adequate thermal properties, as well as the proper high-frequency characteristics.

A unique problem is associated with the silicon chip itself. The active area of the transistor is so small that it acts as a point source of heat. When the wafer or chip is mounted on an adequate header, the bulk of the thermal impedance is in the silicon wafer. Under these conditions, increasing the size of the active transistor area is an inefficient way to increase dissipation. It is more efficient thermally to provide two or more small units dispersed over the chip. If these units are separated by at least the thickness of the wafer, the thermal impedance is nearly inversely proportional to the number of units. The actual spacing between such multiple devices on a single chip is a compromise between dissipation and the parasitic inductance and capacitance added by interconnecting leads. Paralleling devices with evaporated lead patterns can significantly alter performance because of the additional capacitance of the leads.

Such multiple-unit-chip devices as the TIXS12 (four TI3016's in parallel) can offer greatly increased power capability. The TIXS12 produces a minimum of 0.25 watts at 1.5 Gc.

**APPLICATION OF THE TI3016A AND 2N3570**

A description of these devices, with some of their performance characteristics, has been presented earlier. This section provides more specific information on performance and circuit design using these devices.

**Admittance Parameters.** The admittance parameters provide probably the most useful source of information on gain, matching, and stability.\* A complete set of the common-emitter admittance parameters is given in Figs. 2 through 5.

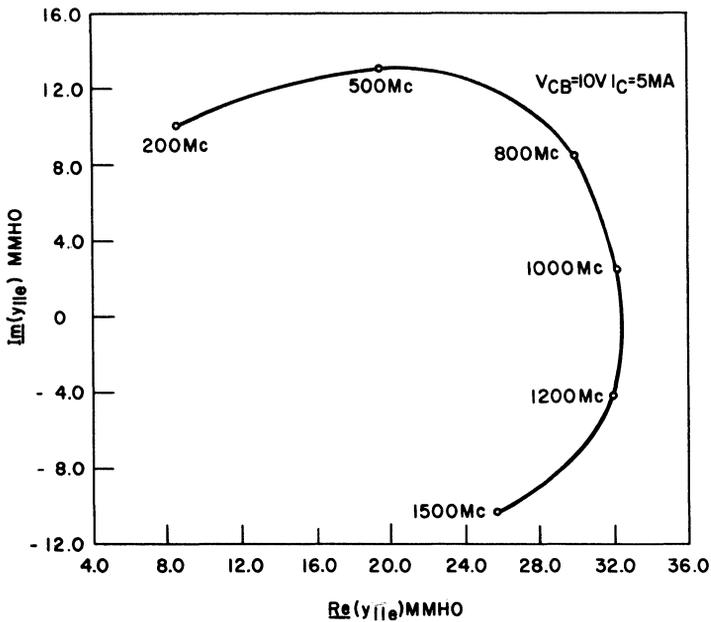


Fig. 2. 2N3570  $y_{11e}$  vs. frequency.

\*One of the more helpful considerations of admittance parameters is presented in Rollett, J. M.: Stability and Power Gain Invariants of Linear Twoports, *IRE Trans.*, vol. CT-9, no. 1, pp. 29-32, March, 1962.

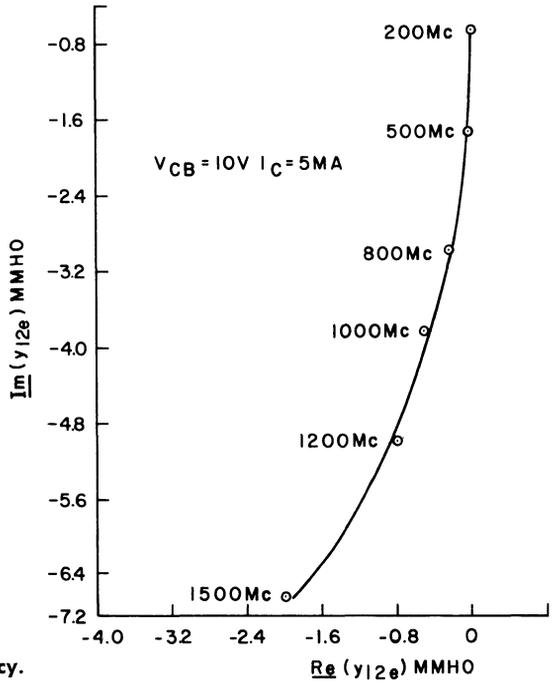


Fig. 3. 2N3570  $y_{12e}$  vs. frequency.

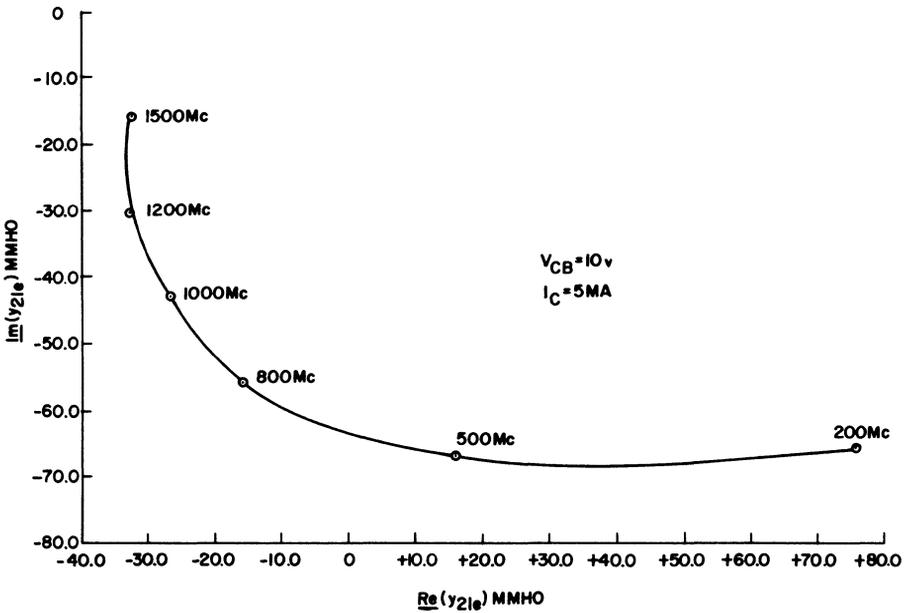


Fig. 4. 2N3570  $y_{21e}$  vs. frequency.

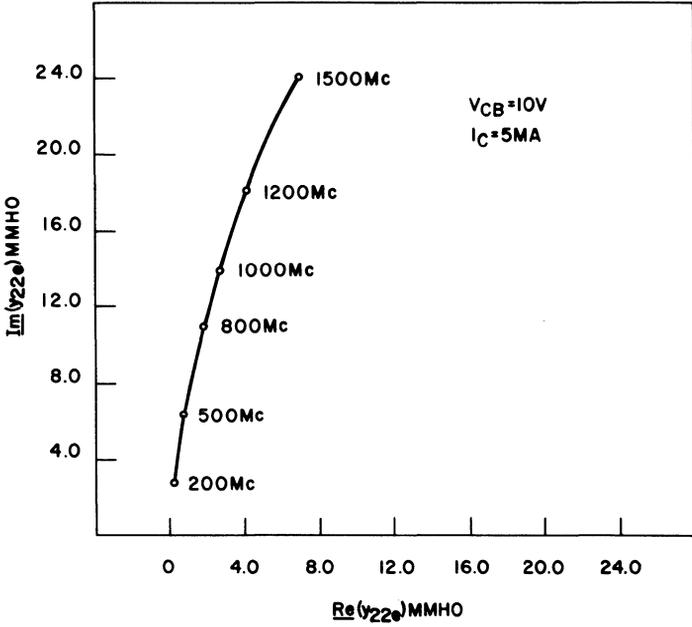


Fig. 5. 2N3570  $y_{22e}$  vs. frequency.

These are plotted with frequency as a parameter from 200 to 1500 Mc, the upper limit of the General Radio 1607A Transfer Function and Immittance Bridge. These parameters are also plotted vs current at 500 Mc in Figs. 6 through 9.

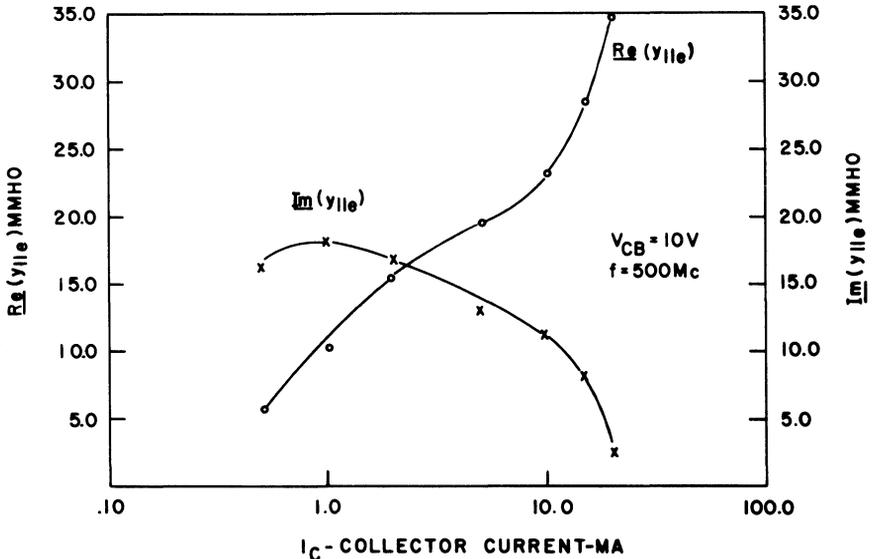


Fig. 6. 2N3570  $y_{11e}$  vs.  $I_C$ .

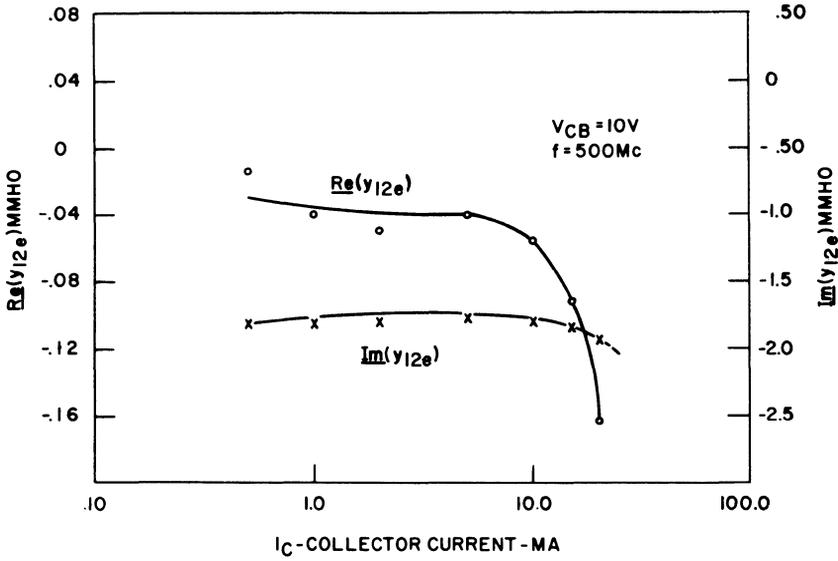


Fig. 7. 2N3570  $y_{12e}$  vs.  $I_C$ .

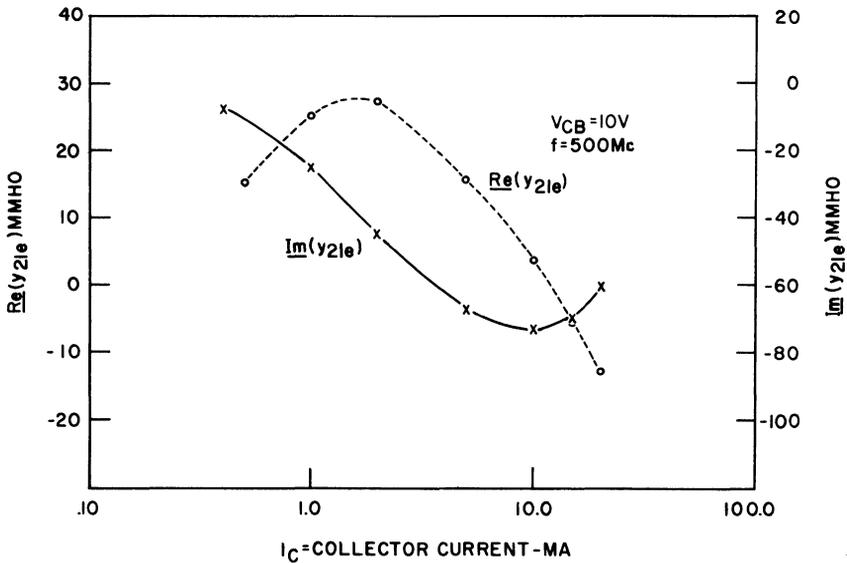


Fig. 8. 2N3570  $y_{21e}$  vs.  $I_C$ .

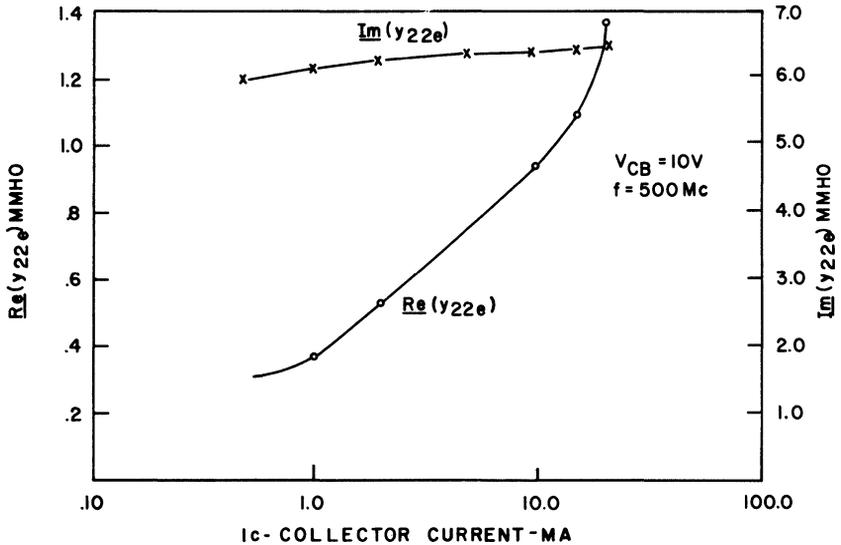


Fig. 9. 2N3570  $y_{22e}$  vs.  $I_C$ .

**Noise Figure.** Plots of noise figure vs frequency for an average 2N3570 are shown in Figs. 10 and 11. Two currents and source impedances are indicated.

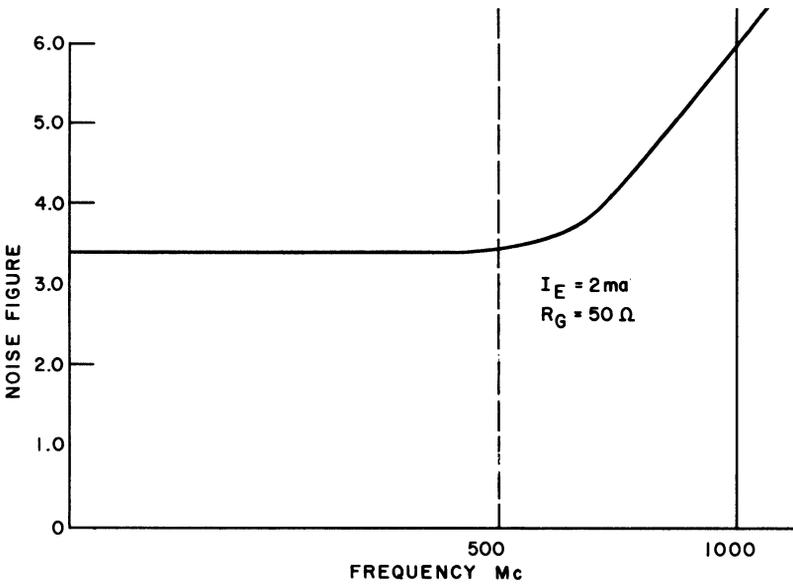
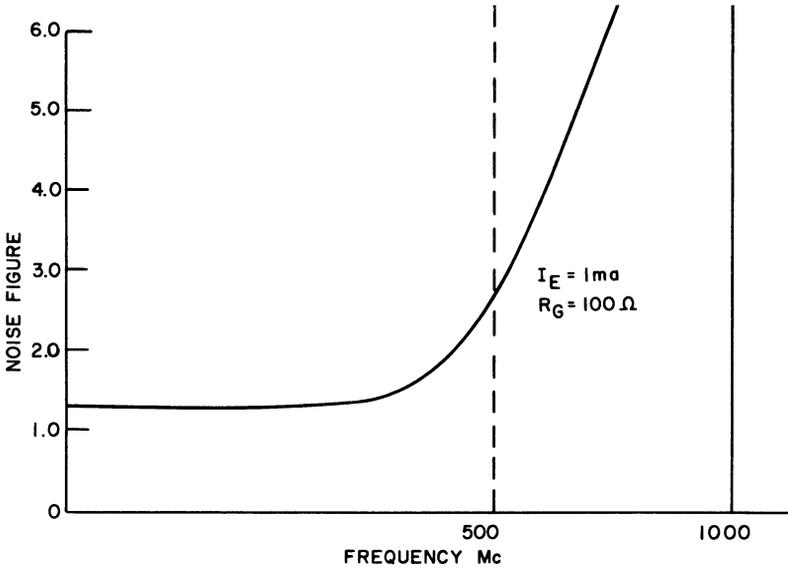
**Selecting Operating Points.** The primary requirements of an amplifier are usually a minimum acceptable gain and a maximum acceptable noise figure. Other requirements, such as bandwidth, linearity, or stability in an environment, may be nearly as important, and in some cases may force a compromise in other characteristics. For the present, however, let gain and noise figure be the primary considerations.

If gain were the only criterion, selection of an operating point would be straightforward. The operating point giving maximum (or near maximum) gain is selected. When noise figure also must be considered, selecting the operating point may not be so simple, since the noise figure of the amplifier may be a function of both gain and noise figure of the devices in the first two (or possibly three) stages.

Power gain usually increases with increasing emitter current and then becomes flat for an appreciable range of current. Gain will also increase slowly with increasing collector voltage up to breakdown. The power gain of the TI 2N3570 is essentially constant with emitter current from 3 to 15 ma, and collector voltage from 4 to 20 volts.

Noise figure, on the other hand, is relatively independent of collector voltage, although there may be a broad minimum. Noise figure is at a minimum at a fairly well-defined emitter current. The noise figure of the 2N3570 tends to a minimum value at emitter currents between 1 and 3 ma, and collector voltages between 3 and 10 volts. The minimum noise figure tends to occur at higher currents as frequency is increased.

**500-Mc Amplifier.** The first design example to be considered is a 500-Mc linear amplifier using the 2N3570. Assume that the requirement is for an amplifier with a noise figure of 4 db or better and an average gain of about 16 db. From



**Figs. 10 and 11. Effect of  $R_G$  and operating point on noise figure.**

Fig. 11, the average noise figure is 3 db for a transistor operated at 5 ma and with an  $R_G$  of 50 ohms. The amplifier could be operated at a lower current to obtain a better noise figure, but at lower gain.

The next step is to obtain the 500-Mc y-parameters from Figs. 6 through 9. These are listed in Table 2. The calculated unilateral gain is only slightly greater than 16 db, the design objective. Therefore, the amplifier must be neutralized. Neglecting the effects of the neutralizing network, the input resistance of the transistor is  $1/0.0195$  or 51 ohms; the output resistance is  $1/0.00076$  or 1300

**Table 2. Typical Common-emitter  $y$  Parameters of the 2N3570 at 500 mc**

$$\begin{aligned}
 y_{11} &= + 19.5 + j13.5 \text{ millimhos} \\
 y_{21} &= + 15.7 - j66.8 \text{ millimhos} \\
 y_{22} &= + 0.76 + j 6.36 \text{ millimhos} \\
 y_{12} &= - 0.04 - j 1.76 \text{ millimhos}
 \end{aligned}$$

Unilateral Gain,  $U = 18.6$  db, from  $y$  parameters

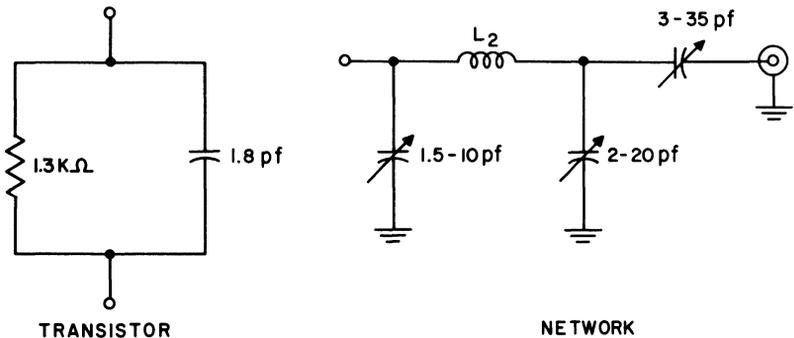
ohms, in parallel with 1.8 pf. The input can be connected directly to the 50-ohm source with a negligible mismatch loss. The output will be matched by a modified pi network.

Figure 12 shows the pi network with an additional series capacitor to increase the flexibility of the system. A piece of 1/4" silverplated brass rod serves as the inductor. The design of the pi network will not be covered here as it has been thoroughly described in the literature.<sup>1,2</sup>

Figure 13 shows the complete schematic of a one-stage amplifier. The input network contains an additional element  $C_3$  so that the source can be connected alternately at point A. This would be desirable, for example, when minimum noise figure is desired. Neutralizing voltage is obtained from a coupling loop  $L_3$  which is a silverplated strip of beryllium copper running parallel to  $L_2$ . Figure 14 is a photograph of the complete amplifier. The placement of  $L_3$  can be critical.

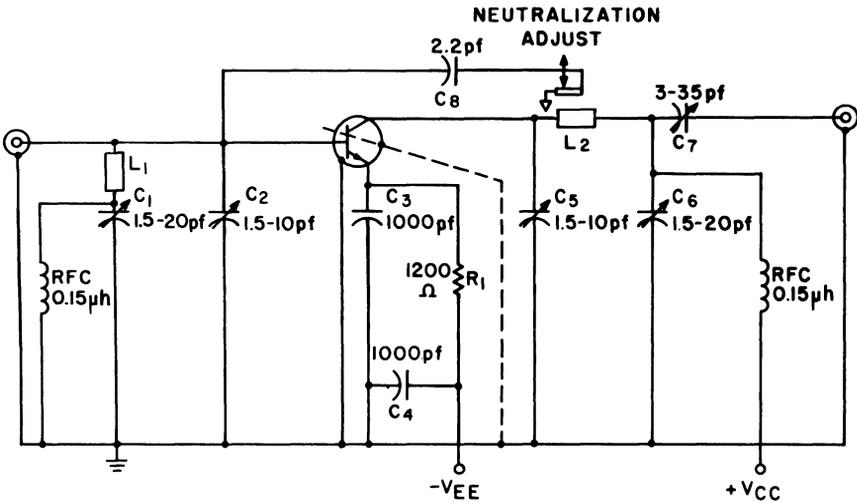
Table 3 shows a comparison of measured and calculated gains made on this amplifier. The agreement is fairly good, the difference in measured gain being attributable to circuit losses.

If the prime requirement had been for minimum noise figure, the design procedure would have varied somewhat. The best combination of emitter current and source resistance can be found by using an automatic noise figure meter in combination with a stub tuner and a suitable test fixture.\* At high frequencies, the correlation factor between input and output noise of a transistor has the dimensions of capacitance. As a result, the optimum noise source is slightly inductive. In general, the optimum noise source resistance decreases with increasing frequency. The



**Fig. 12. Output network for 500-mc amplifier.**

\*A suitable fixture is described in a later chapter, "Noise Figure Measurement."



L<sub>1</sub>: SILVER-PLATED BRASS ROD—1 9/16" LENGTH, 1/4" DIA.  
 L<sub>2</sub>: SILVER-PLATED BRASS ROD—2 1/8" LENGTH, 1/4" DIA.

Fig. 13. 500-mc small-signal common-emitter amplifier.

optimum emitter current, however, increases with increasing frequency, reaching a maximum near the upper useful frequency. The maximum value of  $I_e$  is approximately the value at which  $f_\alpha$  peaks. Figure 11 shows this effect; the 1-ma, 100-ohm curve is about optimum for 500 Mc, and the 5-ma, 50-ohm curve is best for 1 Gc.

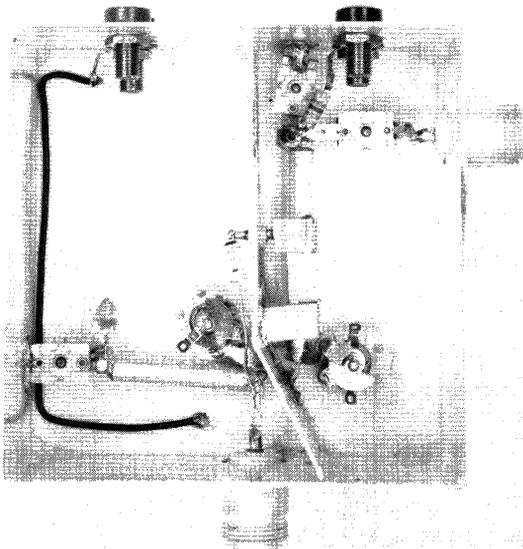


Fig. 14. 500-mc amplifier.

**Table 3. Comparison of Calculated and Measured Gains of 2N3570 at 500 mc**

	Calculated		Measured	Test fixture loss (approx.)
	From $f_T$ & $r_b/C_c$	From y parameters		
1.	18.5 db	18.7 db	16.2 db	2 db
2.	18.9 db	18.9 db	16.5 db	2 db
3.	18.5 db	19.7 db	16.7 db	2 db
4.	18.5 db	19.9 db	17.0 db	2 db

If linearity had been a factor in the design, this would have complicated the selection of an operating point still further. When low distortion is important, it is desirable to operate at a higher emitter current.

**500-Mc Power Amplifier-oscillator.** Power amplifiers or oscillators cannot be designed as simply as linear amplifiers because most of the transistor parameters vary widely with signal level. Thus, this design will be started with a few simple calculations, and then will proceed to a description of the hardware. Assume that a power of 200 mw is desired. Approximate values for the maximum collector voltage and load impedance may be calculated as follows:

$$\begin{aligned}
 V_{CB} &\cong \frac{BV_{CBO}}{2} \\
 &= \frac{40}{2} = 20 \text{ volts} \\
 R_L &\cong \frac{(V_{CB})^2}{2P_o} = \frac{20^2}{2(0.2)} = 1000 \text{ ohms}
 \end{aligned}$$

Since  $R_L$  is greater than 50 ohms, a simple capacitance probe can be used for matching.  $R_L$  is, however, high enough that care should be exercised to see that element Q's are high. A tunable cavity will assure this and will give the additional flexibility of wide-range tuning.

The design shown in Fig. 15 will accommodate either TO-5 or TO-18 transistors, if the collector is tied to the case internally. If the collector is isolated, a connection must be made between collector lead and cavity. Alternately, the collector lead may be soldered to the case. The center conductor of the cavity is a copper rod, and the transistor is inserted into the end to make electrical connection. The copper rod is a very efficient heat sink.

The top of the cavity is made of two plates, the upper one being insulated from the body of the cavity by 0.001-inch Mylar\*. The upper plate is the base connection, and is at RF ground, but is isolated for biasing. Lastly, the emitter is connected to a modified N-type receptacle. An outside d-c block gives the necessary isolation to the emitter line for biasing the emitter. The movable piston makes contact with the cavity walls and the center rod, through beryllium-copper helical springs set into 0.05-inch lands in the piston.

When used as an oscillator, a sliding short is connected to the emitter via the outside d-c block. By adjusting the sliding short, the optimum susceptance for oscillation can be presented to the emitter. Frequency is adjusted by sliding the

\*Reg. Trademark, E. I. DuPont.

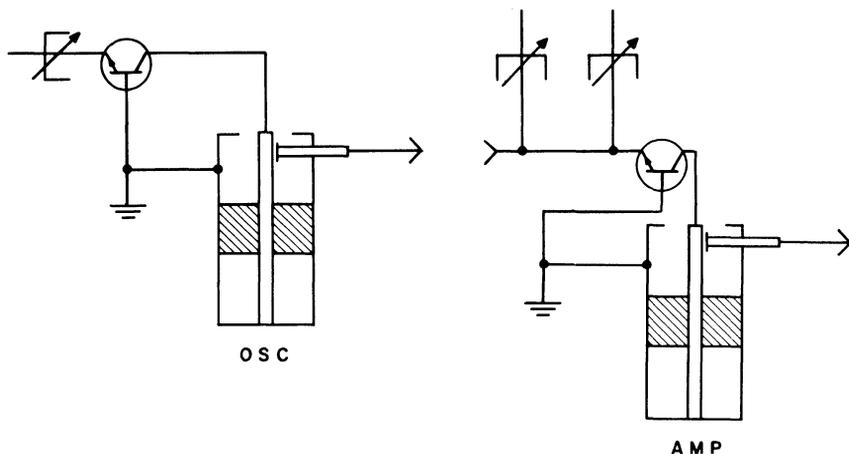


Fig. 15. Tunable high-power fixture for TO-5 and TO-18 transistors.

piston to the appropriate length. The 2N3570 will tune from about 400 to 1000 Mc in this cavity.

The cavity also can be used as a common-base power amplifier by simply replacing the sliding short with a sub tuner to match the input to a generator.

**Wideband Amplifier, 0.5 to 1.45 Gc.** Wideband amplification with transistors at L band was first described by Hamasaki<sup>3</sup> in a design using germanium mesa transistors. The amplifier described here uses TI3016A silicon transistors in a somewhat different circuit configuration. The interstage coupling in this design is a simple LC combination with peaking designed to compensate for the high-frequency gain falloff of the transistor. A single stage of the amplifier is shown in Fig. 16.

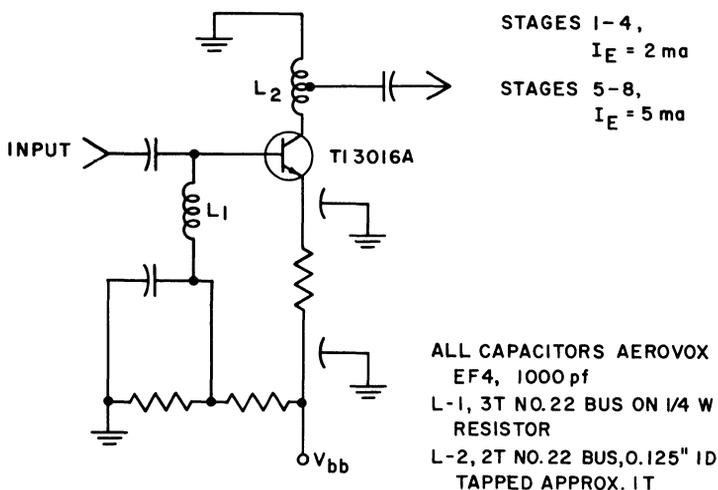


Fig. 16. L-band amplifier single stage.

An unneutralized common-emitter stage was chosen because, of several connections, this gives the greatest bandwidth and is unconditionally stable. However, the stage gain is low, averaging less than 4 db per stage. The low stage gain means that the overall noise figure is strongly influenced by the noise in the second and third stages, as well as the first. A new design using a common-base first stage has been built. It also may be possible to alternate common-base and common-emitter stages to obtain better gain and lower noise figure in fewer stages, while still maintaining the absolute stability of the present design.

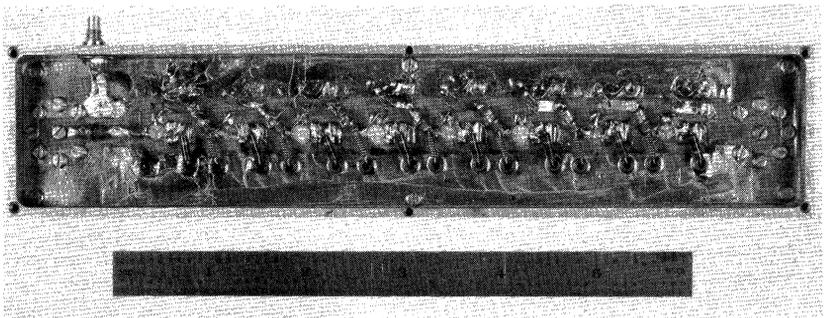
The operating current for optimum noise is a compromise necessitated by the low stage gain and large bandwidth of the amplifier. Since the intrinsic transistor noise figure is rising rapidly at the upper end of the amplifier response, it is best to make a design that favors the higher frequencies.

In selecting the stage current, the early stages need to have a minimum noise measure, i.e., both gain and noise must be considered in the overall noise figure. The later stages are biased for maximum gain. For this amplifier, a 2-ma operating point is used in the first stage, increasing to 5 ma in the last four stages. A photo of the complete amplifier is shown in Fig. 17. Figure 18 shows the performance of the amplifier in graphic form. The gain is flat within  $\pm 1$  db across the specified passband. The noise figure is good but not as low as that of a similar amplifier that was built using the 2N2999 germanium mesa transistor. Phase response is also very good, although this was not a design criterion.

**General-purpose Fixed Tuned Oscillator Amplifier.** A transistor mounted in a TO-18 package can be used to about 1.5 Gc before losses become excessive, although package resonances in some units may set a lower limit. In the fixture described next, the 2N3570 will give 50 to 100 mw as a self-excited oscillator at 1 Gc. The design is similar to the 500-Mc cavity except that frequency is trimmed with a capacitive probe. Figure 19 is a drawing of the fixture.

One of the unique features of this cavity is the method of introducing the collector bias. A discoidal capacitor is soldered to the top of the tubular center conductor of the cavity. The bias lead enters the cavity through the bottom and terminates in the discoidal capacitor which, in turn, is connected to the collector of the transistor.

Note that the transistor socket is mounted horizontally and that the transistor is plugged into the open end of the socket. This arrangement allows a minimum of lead length for all elements. The base grounds directly to the cavity cover, while the emitter is connected to the N-type receptacle. An outside d-c block connects



**Fig. 17. Wide-band amplifier.**

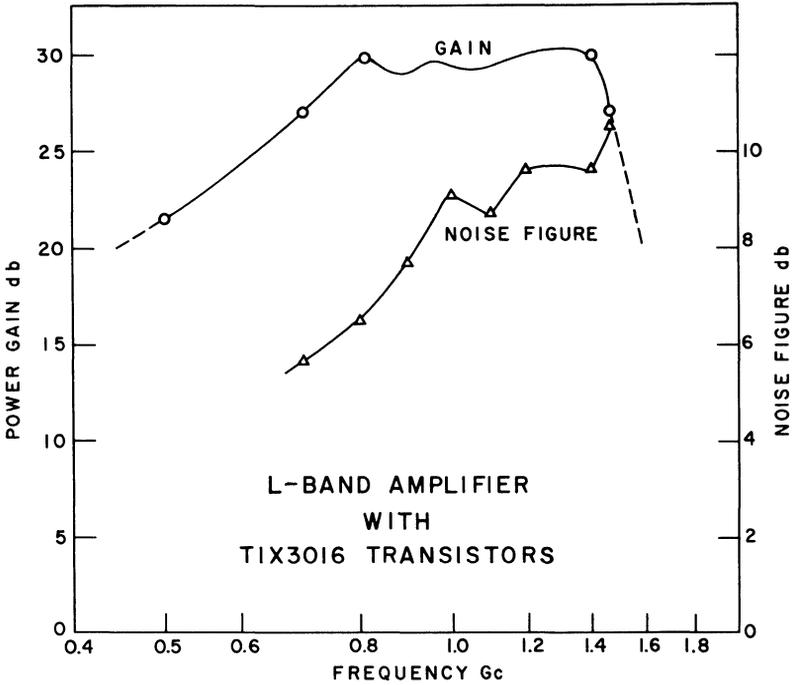


Fig. 18. L-band amplifier with T13016A transistors.

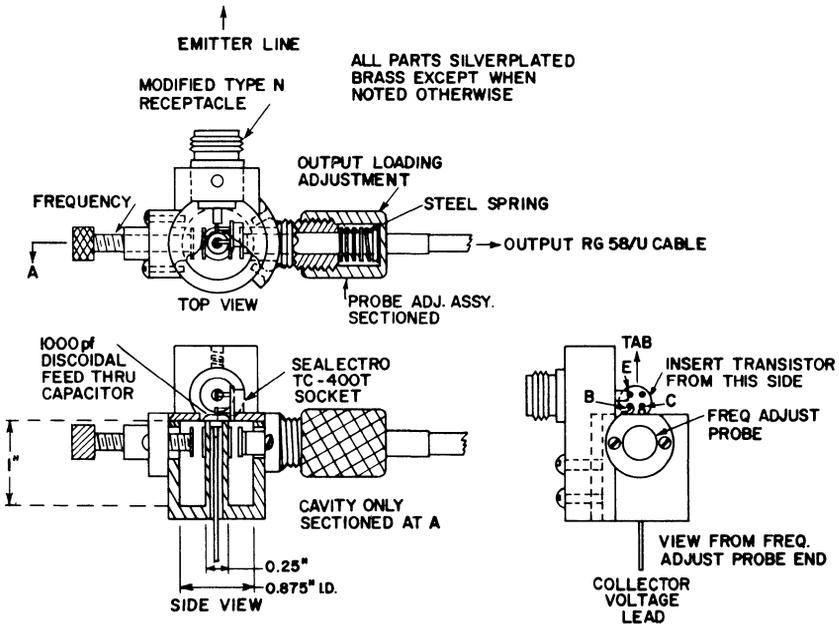


Fig. 19. 1-Gc coaxial cavity for TO-5 or TO-18 transistors.

to the receptacle and thus makes it possible to bias the emitter via the line joined to the d-c block.

Another way to bias the emitter is to feed bias through a shunt choke or resistor. This method results in a much more compact system and can be used where either the absolute maximum output power is not needed, or the transistor is being operated so far below  $f_{\max}$  that emitter immittance is not critical.

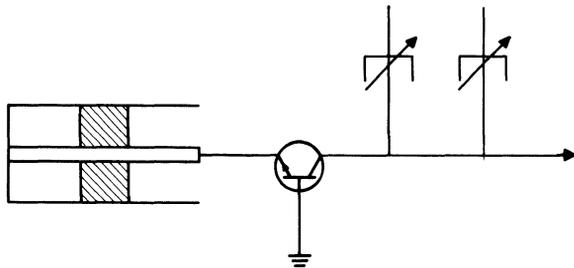
Since the cavity does not have the case connected to a heat sink, it is limited to modest input power — e.g., less than 1 watt. For most measurements, the can is left floating, although it can be grounded when testing transistors such as the 2N3570 with an isolated collector. At 1 Gc it is not necessary to add additional feedback capacitance external to the transistor if the can is left floating.

It also appears that transistors in some types of encapsulation require external capacitance to maintain oscillation. A capacitive "gimmick" which will do this can be made by sliding a piece of Teflon\*-insulated wire inside a small eyelet and soldering these between the collector and emitter. Moving the wire in and out of the eyelet will usually give sufficient range of adjustment. This cavity, like the one described previously, can also be used as an amplifier by connecting a stub tuner to the input.

**2-Gc Oscillator.** The TI-line†-packaged TI3016A can be used as a 2-Gc power source with an average output of 50 mw. Efficiency is about 16 per cent. The base is the common terminal in the TI-line package. The oscillator circuit is shown in Fig. 20. Note that a double-stub tuner in the collector line acts both as a tuning and a matching element. As in the other oscillators previously discussed, the internal capacitance of the transistor is the feedback element.

Both the double-stub tuner and the tunable emitter cavity are isolated from the V-shaped center piece by 0.001-inch Mylar\* film for biasing purposes. The capacitance across these connections is greater than 100 pf, which is adequate for the range of frequencies covered by the fixture. The emitter cavity is tuned by a movable piston using beryllium-copper springs for contacts. The latter are wound from 0.005-inch wire with an outside diameter of 0.05 inch, and are inserted into 0.045-inch lands in the piston. This type of contact appears to be very efficient and lends itself better to small assemblies than bigger stock.

An interesting characteristic of the TI3016A in this kind of oscillator is its second harmonic efficiency. If, for example, a 3-Gc high-pass filter is inserted in the



**Fig. 20. 2-Gc transistor test cavity.**

\*Reg. Trademark, E. I. DuPont

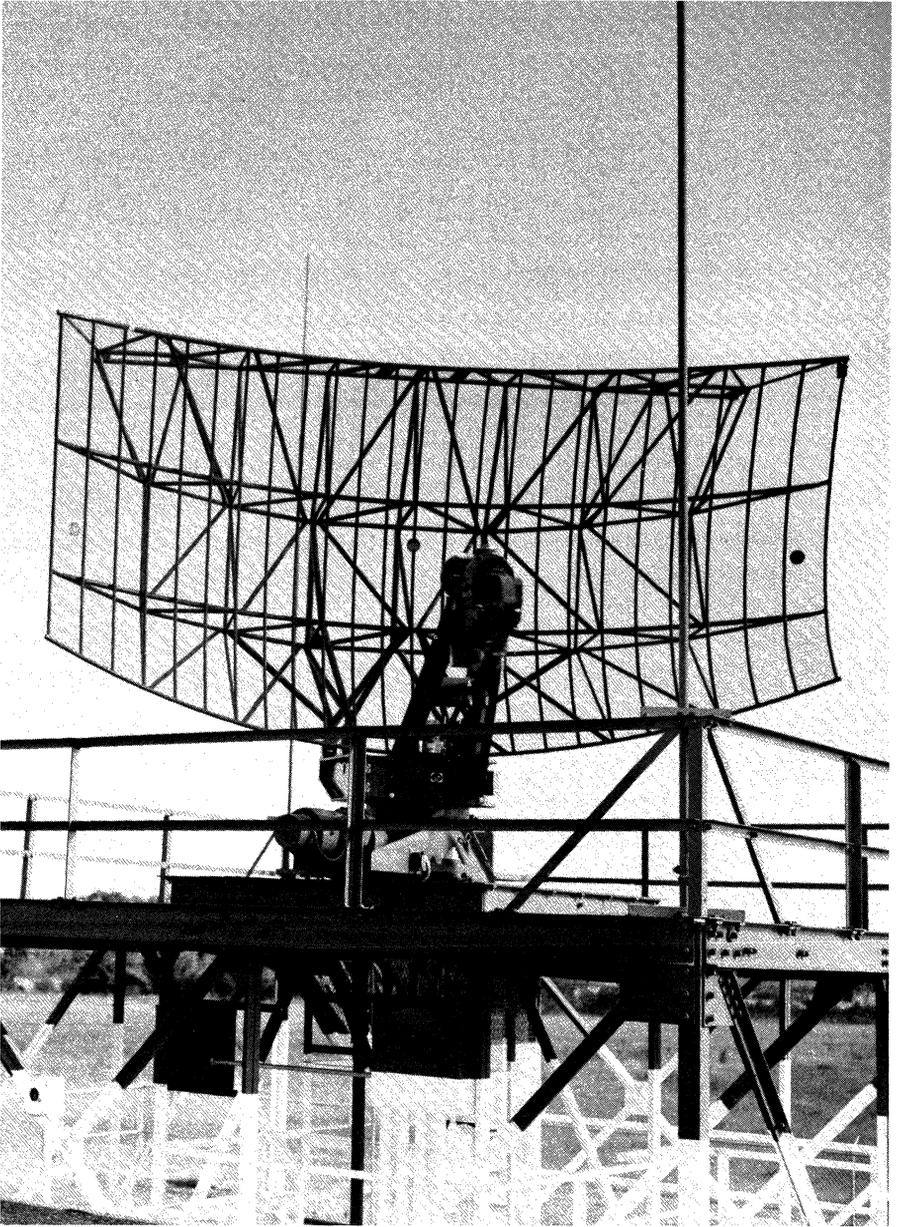
†Trademark of Texas Instruments

output, and the output is retuned slightly, the harmonic power will be only 3 to 6 db below the fundamental, and up to 25 mw may be obtained at 4 Gc. Possibly one of the reasons for the good harmonic efficiency of the TI3016A is that, with proper tuning, the collector capacitance operates as a varactor multiplier.

This oscillator has been used to drive a single 4X gallium varactor frequency multiplier to obtain 25 mw at 9.2 Gc. Another design uses a TIXS13 with two varactor triplers to obtain 30 mw at 16.5 Gc. The simplicity of such systems makes them attractive for applications requiring wideband tuning.

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**The ASR-4 Airport Surveillance Radar is one of many complex radar systems built by TI using TI components.**

## Causes of Noise

by Harry F. Cooke

### INTRODUCTION

The process of low-noise amplification is now almost exclusively dominated by solid-state devices. Recently, we have seen many refinements in the technology of device fabrication, rather than the discovery of new types of devices using new principles. These refinements are in large part responsible for the rather spectacular noise performance of today's semiconductors.

Throughout this chapter we shall use the term "noise figure" to describe noisiness of a device. It is the most common term in use today and means simply the degradation in signal-to-noise ratio caused by an amplifier, expressed as a ratio or in db. As an example of device improvement, we may cite Shockley's early audio transistor noise figure of 70 db, compared with 0.2 db obtainable today. One of the reasons our technology has been so successful in improving semiconductor devices is that our understanding of the noise mechanism in semiconductors is now fairly complete. Even those types of noise which are not completely understood can be controlled to a degree.

In Fig. 1, the noise characteristics of a number of types of semiconductor amplifiers from sub-audio to microwave frequencies are shown. Note that the parametric amplifier provides the lowest noise figure at both ends of the spectrum. The great complexity of the parametric amplifier, however, makes it uneconomical to use where other devices are available. Silicon FET's or planar devices are most used at low frequencies, while both mesa and planar devices are useful in the microwave region.

### TYPES OF NOISE

We will now describe briefly some of the types of noise found in semiconductor amplifiers. For some of the types of noise there are simple circuit equivalents, which are shown.

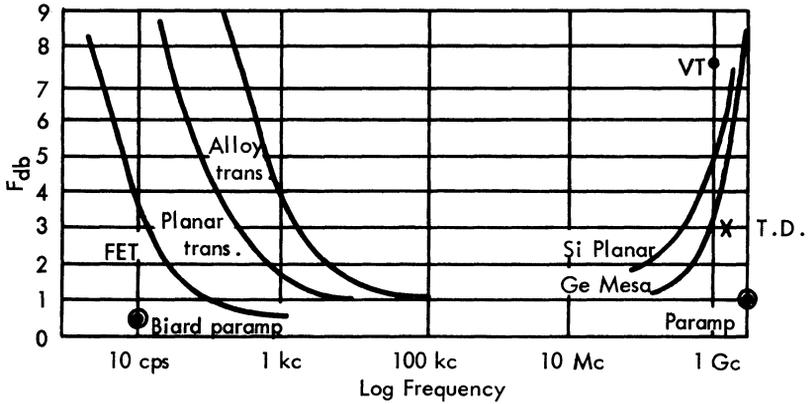
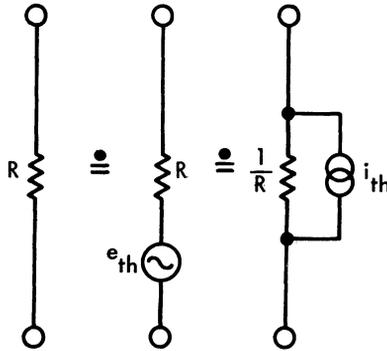


Figure 1

**Thermal Noise.** Thermal noise power is generated by all solids not at absolute zero; it arises from the fact that the thermal agitation of carriers gives rise to electrical energy. The thermal power generated depends only on the temperature (and the bandwidth over which it is measured). This agitation is so completely random that when we attach terminals to the medium, we find that the voltage at the terminals covers all frequencies. In fact, the mean-squared value of the voltage is proportional only to resistance, temperature, bandwidth, and a constant called "Boltzmann's Constant." Figure 2 shows how we can represent this voltage from a circuit point of view.



$$G = \frac{1}{R}$$

where

$$\overline{i_{th}^2} = 4kT\Delta fG$$

$$\overline{e_{th}^2} = 4kT\Delta fR$$

$k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  joules/°K

$T$  = temperature in degrees Kelvin =  $300^\circ$  at room temperature

$\Delta f$  = bandwidth in cps

$R$  = resistance in ohms

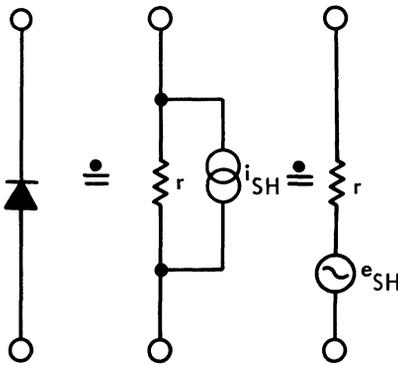
Figure 2

Here we equate a noisy resistor with a noiseless resistor plus a voltage generator. In semiconductors, thermal noise voltage is found wherever there is an appreciable bulk resistance, as in the base resistance of a transistor. Note that the noise power is proportional to bandwidth, but not frequency; the voltage is the same regardless of where we take our slice of bandwidth in the frequency spectrum.

**Shot Noise.** The second type of noise with which we will be concerned is shot noise. Shot noise occurs whenever a current flows, as from the influence of a field in vacuum tubes, or a concentration gradient in transistors and diodes. Although there is some degree of organization in the motion of carriers (their average motion is in one direction), their final arrival is completely random. This randomness gives rise to a uniform frequency spectrum of noise, as in the thermal case. The mean-squared noise current is proportional to the charge on an electron, the d-c current flowing, and the bandwidth.

Figure 3 gives the circuit representation of shot noise in a diode.

The noisy diode is here equated with a resistance equal to the dynamic resistance



$$\overline{i_{SH}^2} = 2qI_{dc} \Delta f$$

$$r = \frac{nkT}{qI_{dc}} \approx \frac{25}{I_{dc}} \text{ ohms}$$

$$\overline{e_{SH}^2} = \overline{i_{SH}^2} r^2$$

$$= 2 q I_{dc} \Delta f \left( \frac{nkT}{qI_{dc}} \right)^2$$

$$= 2 k T \Delta f r$$

$q$  = charge of an electron =  $1.59 \times 10^{-19}$  coulombs

$n$  = a constant  $\cong 1$  for transistor

$\Delta f$  = bandwidth in cps

Figure 3

of the diode in parallel with a noise-current generator. The dynamic resistance of a diode at average carrier injection levels has been shown to be equal to  $nkT/qI_{dc}$ , where the symbols have the meaning shown in Fig. 3. In many circuits it is more convenient to have a voltage generator than a current generator. Since the dynamic resistance of the diode has been defined in terms similar to the noise current, we find that a simple arithmetical manipulation transforms the shot-noise current generator into a resistance in series with a voltage generator as shown. Note that the form of the shot-noise voltage generator is almost identical to the thermal-noise generator, but is  $\sqrt{2/2}$  times as large. At very high frequencies, where the transit time of carriers across the diode becomes appreciable, the diode resistance decreases. In other words, the diode behaves as if we had paralleled another resistor with it. It has been found that this resistance shows full thermal noise.

**Other Types of Noise.** The two types of noise just mentioned are the only kinds that affect high-frequency transistors and other RF devices to any degree. The remaining types of noise which we will now discuss do not affect semiconductor operation except under special conditions.

The first and most important of these is  $1/f$  noise, sometimes called flicker, or scintillation noise. It is called  $1/f$  noise because the noise power per unit bandwidth increases inversely with frequency. It usually occurs only at the lower audio frequency, but can manifest itself up into the UHF region. The exact causes of  $1/f$  noise are not known at present, although many theories have been set forth in explanation of the phenomenon. It is even difficult mathematically to write a simple expression for  $1/f$  noise. Most  $1/f$  noise in transistors has been localized to what are called slow states within the emitter depletion layer. These slow states, or traps, capture and release carriers at different rates, but with energy levels varying inversely with frequency.

Figure 4 shows a plot of the low-frequency noise figure of a transistor vs. log frequency. The noise figure increases at a 3 db per octave rate for frequencies

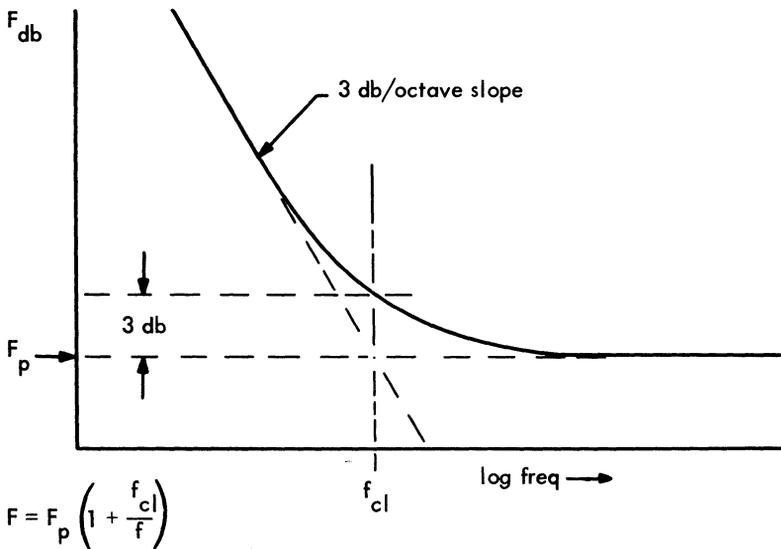


Figure 4

below the point called the corner frequency  $f_{CL}$ . The corner frequency is defined as that frequency at which the  $1/f$  noise power equals the mid-frequency noise power. At this frequency the noise figure has increased 3 db over the mid-frequency figure. Once the corner frequency has been determined, we may write the noise factor in the  $1/f$  region as:

$$F = F_p \left( 1 + \frac{f_c}{f} \right)$$

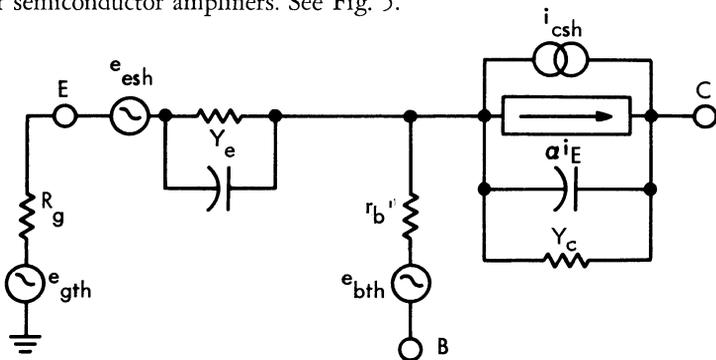
Admittedly, we have used a mathematical convenience to define a type of noise that we cannot designate by other means. However, once we have found the corner frequency for a given type of transistor, this frequency will remain fairly constant for a given set of operating conditions with other transistors of this type. Excessive  $1/f$  noise may be an indication of defects in transistor fabrication. In general, planar and FET transistors have lower  $1/f$  corner frequencies than other types.

Another type of noise commonly found in transistors is generation-recombination noise. G-R noise is basically a thermal effect. The noise is generated when carriers recombine or separate after crossing a junction causing a net change in charge. G-R noise is generally negligible in good transistors. It appears most often in transistors having very low current gain, and falls off rapidly at high frequencies.

Avalanche noise is present in Zener diodes and transistors operated in the breakdown region. Its presence is due to the fact that carriers under the influence of very large fields may collide with and release other carriers within the crystal lattice. This multiplication of carriers during breakdown can produce very large noise voltages. Fortunately, the effect occurs in a region where transistors are normally never operated for other reasons, and is of no importance in amplifying devices. It has been used as a noise source for test purposes.

### NOISE SOURCES AND EQUIVALENT CIRCUITS

We will next show how noise sources fit into the equivalent circuits for four types of semiconductor amplifiers. See Fig. 5.



$$F_{HF} = 1 + \frac{r_{b'}'}{R_g} + \frac{r_e}{2R_g} + \frac{(r_e + r_{b'}' + R_g)^2}{2\alpha_o R_g r_E} \left[ \left( \frac{f}{f_\alpha} \right)^2 + \frac{I_{co}}{I_E} + \frac{1}{h_{FE}} \right]$$

$$F_{1/f} = F_{HF} \left( 1 + \frac{f_{CL}}{f} \right)$$

Figure 5

The transistor, except in the  $1/f$  region, has two types of noise sources; thermal and shot. The thermal noise comes from the base spreading resistance, or more simply  $r'_b$ . The emitter-base diode develops full shot noise as does the collector-base diode. When we calculate the noise figure of the transistor, we must recognize that the shot noise in the two diodes comes about from almost exactly the same carriers. Therefore, we must subtract from one diode that noise which we have already accounted for in the other. If we sum the noise voltages in the output of the transistor, only the uncorrelated part of the collector noise is added. In the simplest case, the collector and emitter shot-noise generators are correlated by the alpha of the transistor. The noise figure expressions for the common-base and common-emitter connections are the same. The three terms shown in the noise figure equation represent the contributions of the base resistance, emitter, and uncorrelated collector noise, respectively. If we examine the noise figure equation, we can immediately make some observations as to the most desirable features of a low-noise transistor. First of all, the base resistance should be low. Next,  $f_\alpha$  and  $h_{FE}$  should be high.  $I_{co}$  should be as low as possible. The term  $\alpha_o$  approaches 1 when  $h_{FE}$  is high. At low frequencies the frequency-dependent part  $f/f_\alpha$  vanishes, and the last term of the noise figure depends primarily on the common-emitter current gain  $h_{FE}$ . At low frequencies and high source impedances, the entire equation degenerates to:

$$F = 1 + \frac{R_g}{2r_e h_{FE}} \tag{1}$$

$$R_{g(opt)} = \left[ (r_e + r'_b)^2 + \frac{\alpha_o r_e (2r'_b + r_e)}{\frac{1}{h_{FE}} + \left(\frac{f}{f_\alpha}\right)^2 + \frac{I_{co}}{I_E}} \right]^{1/2} \tag{2}$$

$= r_e \sqrt{h_{FE}}$       if  $r_b \ll r_e$ , at low frequencies  
 $= r_e + r'_b$       at very high frequencies

The next most obvious question is "What  $R_g$  will give the best noise figure?" This is found by differentiating the noise equation with respect to  $R_g$ . The result is then set equal to 0, and  $R_g$  is solved for. The result is shown in Eqs. (1) and (2). At high frequencies  $R_{g(opt)}$  simplifies to  $r'_b + r_e$ . This value of  $R_{g(opt)}$  may be substituted in the original noise figure equation to get the expression for the minimum noise figure  $F_{min}$ .

**Noise in Other Solid-state Amplifying Devices.** *The field-effect transistor (FET) in the present state of the art is used most at low frequencies, but it is becoming a UHF device. It is subject to the same types of noise that are found in a conventional transistor, including  $1/f$  noise. Most FET's are planar in design, and the  $1/f$  noise does not become significant until a very low frequency is reached.*

The noise mechanisms in the FET are quite similar to those in the diffusion transistor except for the part which capacitance plays. Gate-to-source capacitance can couple output noise back to the input since input impedance is high. Since this capacitance is distributed in nature, not all the capacitance acts as a feedback element. To properly divide the channel resistance, Bechtel\* has suggested a constant,  $\lambda$ . The significance of  $\lambda$  is shown in Fig. 6. A more conventional schematic of an FET and the equation for noise figure are shown in Fig. 7.

\*Bechtel, N. G.: A Circuit and Noise Model of the Field-effect Transistor, Proc. of the International Solid State Circuits Conf., February, 1963.

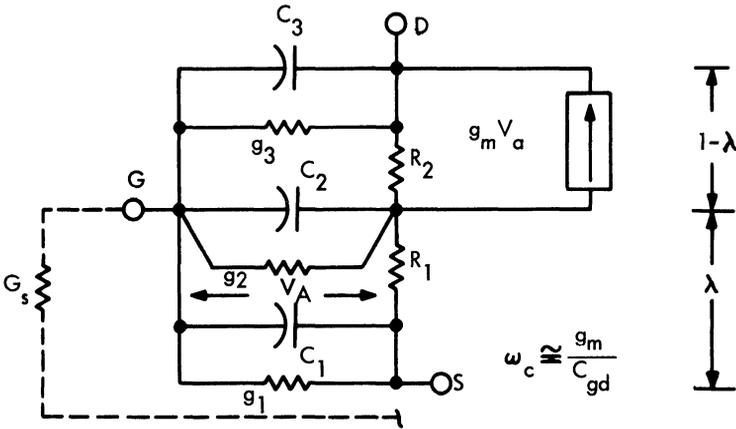
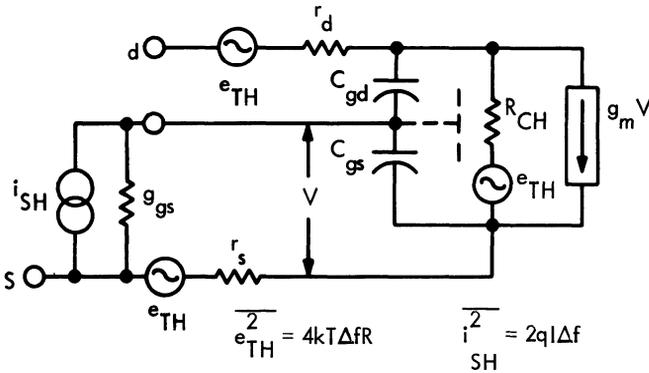


Figure 6



For all frequencies except 1/f region:

$$F = 1 + \frac{2\lambda\omega}{g_m} (C_{gs} + C_{gd}) + \frac{\lambda}{g_m} \left[ \frac{G_s - \omega (C_{gs} + C_{gd})}{G_s} \right]^2$$

For low frequencies except 1/f region:

$$F_{low} = 1 + \frac{\lambda G}{g_m}$$

$$G_{opt} \approx \omega (C_{gs} + C_{gd})$$

where

$G_s$  = source conductance

$g_m$  = low-frequency transconductance

$\omega$  = frequency of operation

Figure 7

The main sources of noise in a field-effect transistor are: thermal noise in the channel, shot noise in the gate-to-channel leakage, thermal noise in the bulk resistances, and capacitance-coupled thermal noise at the input. Note that the low-frequency noise figure depends on  $\lambda$ , which is about 0.5. For the vacuum tube,  $\lambda = 2.5$ . Thus, for the same  $g_m$ , the FET is less noisy than the vacuum tube.

The tunnel diode is a relative newcomer to the field of low-noise amplification. It is a very-low-noise device, but since it has only two terminals, its application differs radically from the transistors discussed previously. As with all two-terminal amplifiers, its performance is affected by the noise in the load as well as the source.

See Fig. 8; the noise figure of the tunnel diode is: (3)

$$F = 1 + \frac{R_g}{R_L} \frac{R_g}{R - r_s} \frac{1 + \omega^2 R^2 C^2}{\left(\frac{\omega}{\omega_c}\right)^2 + \omega_c^2 R^2 C^2} + \frac{q(I_{eq}) R}{2kT} \frac{R_g}{r_s} \frac{R}{R - r_s} \frac{1}{\left(\frac{\omega}{\omega_c}\right)^2 + \omega_c^2 R^2 C^2}$$

The first term in the noise expression is the thermal noise in the load resistance  $r_L$ . The second term is the thermal noise from  $r_s$ . The third term is the equivalent shot noise term. This last term needs some explanation since it actually accounts for two separate currents. In some regions of operation, both of these currents show full shot noise. Since these currents flow in opposition, the net terminal d-c current may be much less than either one of the two internal currents that make it up. Thus we use the term, "equivalent current" which can be larger than the actual external d-c current flowing at the point of operation. The term  $\omega_c$ , the angular cutoff frequency, is the highest frequency at which the device terminals still show negative resistance. A good noise figure of merit for a tunnel diode is the reciprocal of the negative resistance times the equivalent shot-noise current at the point where this is maximum. It is beyond the scope of this work to discuss the many circuit variations that are possible with a tunnel diode.

The varactor, or variable capacitance diode, is the active element in most so-called parametric amplifiers. The capacitance of a reverse-biased diode varies with volt-

age and according to the law of  $C = \frac{k}{V \frac{1}{n}}$ , where n usually lies between 2 and

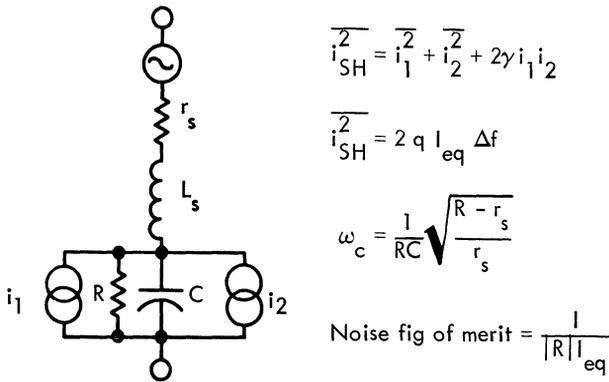


Figure 8

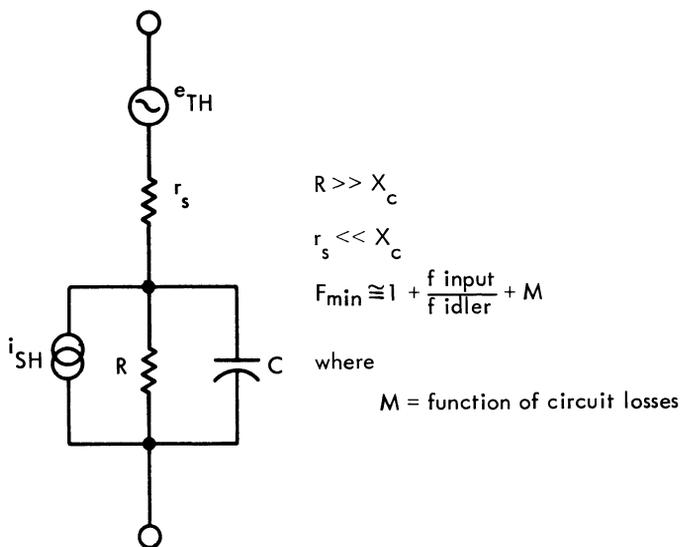


Figure 9

3. The parametric amplifier utilizes the variable capacitance effect to obtain power gain by translating (pumping) energy at one frequency to a higher frequency. See Fig. 9.

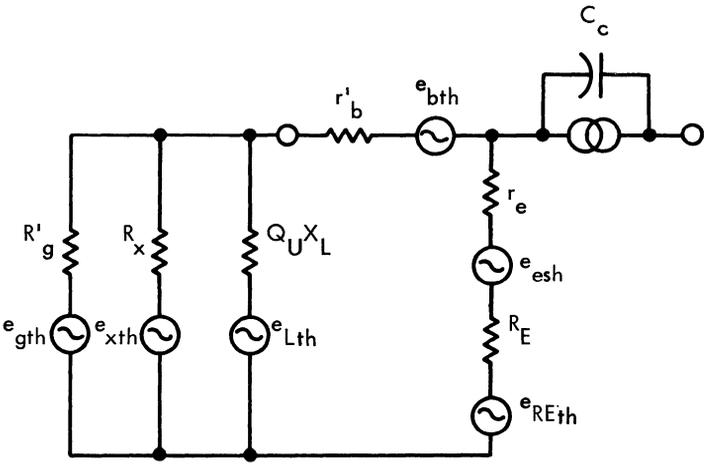
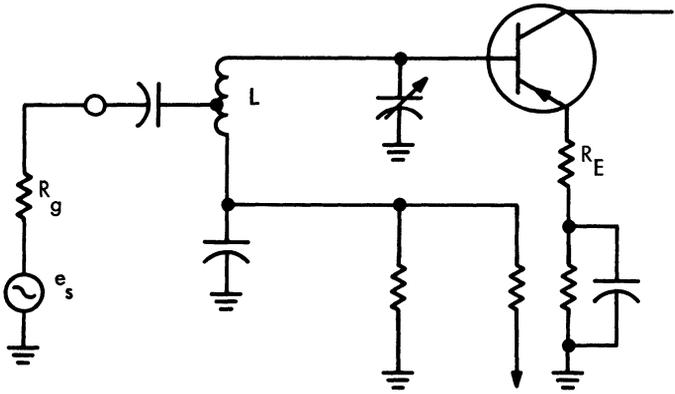
The sources of noise in the parametric amplifier are thermal noise in the series resistance, shot noise from the leakage current, and thermal noise, in the load, idler, and input circuits respectively. The first two are characteristics of the diode alone, the last terms are functions of the circuit. Both of the noise sources in the diode can be made negligible by proper fabrication and design. With careful attention to circuit details, overall noise figures of less than 1 db are attainable. Note that we have talked about only one type of parametric amplifier. Readers interested in the details of other types are referred to the many papers that have been written on the subject.

**Design Precautions.** The following discussion will illustrate some of the precautions to be used in designing a low-noise transistor amplifier. Consider the circuit shown in Fig. 10 and the noise equivalent. The following points are to be noted:

1. Bias resistors when they appear across an input circuit always attenuate the desired signal to some extent. At higher frequencies their value may be much less than that indicated by d-c measurements. It is always best to bias through the ground end of the input tank circuit if at all possible.

2. The unloaded Q of the input tank should be as high as possible or the loaded Q should be as low as possible, or both. This ensures that input losses from the tuning circuits will be low. It usually also implies that input selectivity will be quite broad.

3. Since  $R_g$  is seldom the same as  $R_{g(opt)}$ , some transformation is usually necessary. This can be done with tapped transformers (as shown), LC networks, baluns, or distributed type transformers. The losses in these networks should also be low.



$R'_g$  = transformed  $R_g$   
 $R_x$  = equivalent loss resistance, miscellaneous losses  
 $Q_U X_L$  = coil loss resistance

Figure 10

4. In the UHF and microwave range all component losses can be important, e.g., those from socket leads and coupling capacitors.

One final word of caution. Under certain circumstances it is possible that a transistor, when operated to give best noise figure in the input stage, will not give the minimum overall noise figure which includes the second and following stages.

The overall noise figure for several stages is shown in Fig. 11. If the point of operation chosen to minimize  $F_1$  is such that  $G_1$  is low or  $F_2$  is high, or both, then the overall noise figure may be improved by choosing a value for  $R_g$  which increases the gain. This will deteriorate the noise figure of the first stage, but the overall noise figure will be lower.

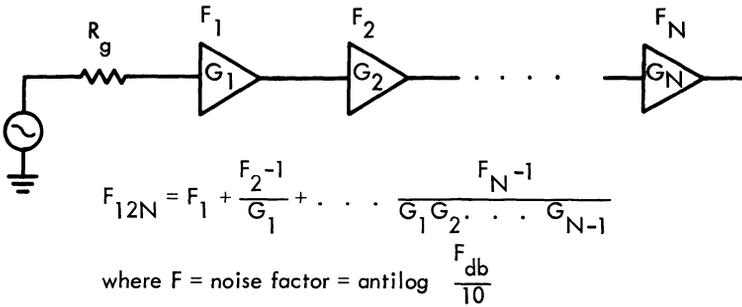
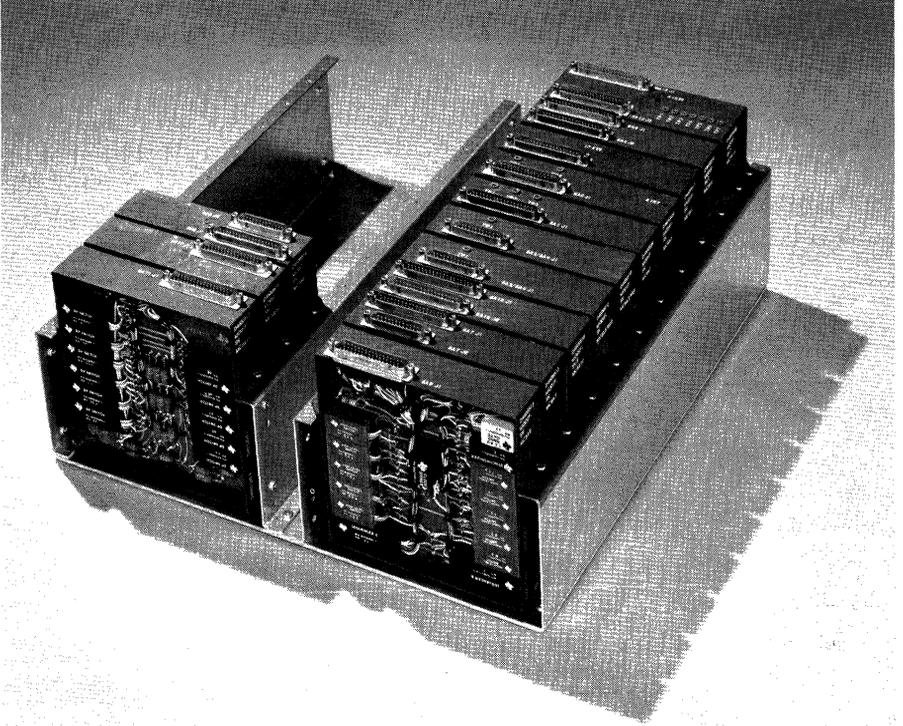


Figure 11



**TI telemetry equipment in the Mariner probe. Mariner voyages into deep space are the farthest explorations ever made by man.**

## Transistor Noise Figure

by Harry F. Cooke

### INTRODUCTION

The noise figure of junction transistors has been treated by several authors (particularly Nielsen<sup>1</sup>, van der Ziel<sup>2-4</sup>, and Strutt<sup>5</sup>) in great detail and with mathematical rigor. However, a development of the noise-figure expression using a somewhat simplified approach is useful to many engineers, particularly those engaged in circuit design. A great deal of noise theory is statistical in nature and quite complex. The actual derivation of the thermal and shot-noise generators is avoided in this chapter for this reason. The development of the noise-figure expression and following remarks attempt to use circuit concepts more familiar to the average engineer.

There are three broad classifications of noise sources usually found in a transistor — flicker (or  $1/f$ ) noise, thermal noise, and shot noise. Flicker noise begins to influence noise figure at some relatively low frequency ( $f_{CL}$ , the low-frequency noise corner, Fig. 1) and increases as frequency decreases at a 3 db/octave rate. As yet, flicker noise is not completely mathematically predictable. Fortunately, the

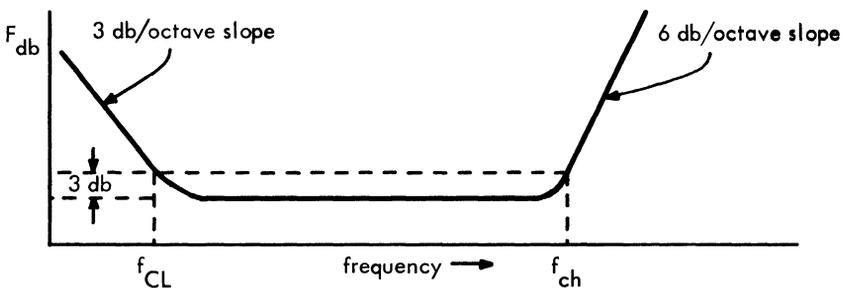


Figure 1

flicker noise corner can be lowered to some extent by transistor fabrication techniques, and usually is not important to high-frequency operation.

Neither thermal noise nor shot noise is frequency dependent, and both exhibit uniform noise output through the entire useful frequency range of the transistor. The internal gain of the transistor does vary with frequency, however, and falls off as frequency increases. The noise figure begins to rise when the loss in gain becomes appreciable. The frequency at which this occurs is called  $f_{CH}$ , the upper- or high-frequency noise corner. Since the power gain falls inversely as frequency squared, the noise figure rises as frequency squared, or 6 db per octave. This is shown graphically in Fig. 1.

**THERMAL NOISE**

Thermal noise is due to the disorganized nature of the motion of charges within a device. This motion gives rise to an electrical power that is proportional to the absolute temperature and the bandwidth. The noise voltage across the terminals of a device is a function of the power and the resistance of the device. The mean-squared noise voltage,  $\overline{e_{nth}^2}$ , which appears at the terminals is:

$$\overline{e_{nth}^2} = 4kTR\Delta f, (\text{volts})^2, \tag{1}$$

$$\text{or } e_{nth} = 126 \sqrt{R\Delta f} \times 10^{-12} \text{ volts at } 290^\circ\text{K}$$

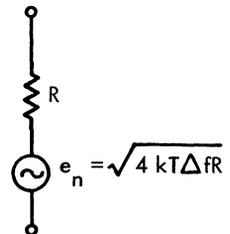
- where
- $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  joules/ $K^\circ$
  - $T$  = temperature in degrees Kelvin
  - $R$  = resistance of the device in ohms at its terminals
  - $f$  = bandwidth in cycles/sec.

Because of the random character of the motion of the charges, the thermal noise spectrum is uniform throughout the useful range of present transistors as long as  $R$  is a pure resistance.

From a circuit viewpoint, thermal noise may be represented as a voltage generator in series with a noiseless resistor, as shown in Fig. 2.

**SHOT NOISE**

Shot noise occurs under certain conditions when a current flows. The current flow may be caused by a field as in vacuum tubes or by a concentration gradient (i.e., diffusion) as in transistors. In both cases, it is caused by the random nature of the arrival of the charges. If the charges arrived uniformly, a single frequency would be generated which would be about  $10^{16}$  cycles/ma of d-c current. However, the process is completely random and, like thermal noise, the shot noise spectrum is uniform.



**Figure 2**

The shot-noise energy associated with a stream of carriers (or charges) — i.e., a d-c current — is proportional to the charge of an electron, the d-c current flowing, and the bandwidth. This can be represented by a constant-current generator,  $i_n^2$ , where:

$$\overline{i_n^2} = 2qI_{dc}\Delta f \tag{2}$$

where  $q$  = charge of an electron =  $1.6 \times 10^{-19}$  coulombs  
 $I_{dc}$  = d-c current flow in amperes  
 $\Delta f$  = bandwidth in cps

The equivalent circuit is that of a current generator in parallel with a noiseless conductance,  $g_o$ , where  $g_o$  is the effective conductance of the region through which the current stream flows (Fig. 3).

For transistors and semiconductor diodes at low carrier injection levels, the conductance  $g_o$  is the incremental conductance of the P-N junction and is given by the following expression:

$$g_o = \frac{qI_{dc}}{kT} \tag{3}$$

$$= \frac{I_{dc} \text{ ma}}{25} \text{ mhos} \tag{3a}$$

where  $q$ ,  $I_{dc}$ ,  $k$ , and  $T$  have the same meaning as used previously.

Since we now have an expression for the conductance of the diode, it is possible to convert the mean-squared shot-noise current generator to an equivalent voltage generator.

$$\begin{aligned} \overline{e_n^2} &= \frac{\overline{i_n^2}}{g_o^2} \\ &= \frac{2qI_{dc}\Delta f}{qI_{dc}} kT \frac{1}{g_o} \\ &= \frac{2kT\Delta f}{g_o} \\ &= 2kTr_o\Delta f \end{aligned} \tag{4}$$

where  $r_o = \frac{1}{g_o}$

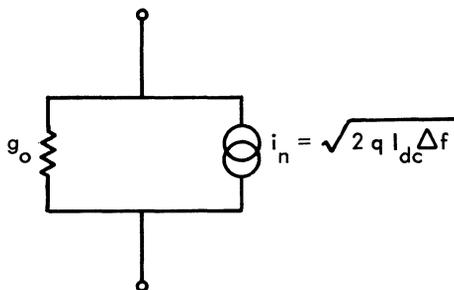


Figure 3

Note that the shot-noise voltage is exactly the same in form as the thermal-noise voltage, but is  $\sqrt{2}/2$  times as large. The alternate equivalent circuit is then as shown in Fig. 4. The equivalent circuit again is that of a voltage generator in series with a noiseless resistance.

At very high frequencies, usually beyond the useful range of present transistors, the transit time of the carriers across the diode becomes appreciable. This introduces a conductance in addition to  $g_o$  shunting the diode which will show full thermal noise. The total shot-noise current under these conditions will be:

$$\overline{i_n^2} = 2qI_{dc}\Delta f + 4kT(g - g_o)\Delta f \quad (5)$$

where  $g$  is the high-frequency diode conductance.

This additional noise in transistors is attributed by van der Ziel to carriers that cross the emitter-base junction to the base but return and recombine in the emitter region where they originated.

**TRANSISTOR NOISE-FIGURE EQUATION, HIGH FREQUENCY**

The development that follows is based on the common-base configuration, but Nielsen<sup>1</sup> has shown it to be valid for both common-base and common-emitter. The common-collector stage, because of its larger noise figure, is usually of little interest in high-frequency applications.

The transistor itself has three main internal noise generators:

1. shot noise in the emitter-base junction,
2. thermal noise in the base resistance, and
3. shot noise in the collector-base junction.

These noise sources can best be shown in the high-frequency T-equivalent circuit of Fig. 5.

In Fig. 5:  $e_{esh}$  = emitter shot noise equivalent voltage generator =  $\sqrt{2kT r_e \Delta f}$

$i_{esh}$  = emitter shot noise equivalent current generator =  $\sqrt{2qI_E \Delta f}$

$i_{csh}$  = collector shot noise current generator (includes noise from  $I_{CO}$ )

$e_{gth}$  = thermal noise from the generator resistance

$i_c$  = collector current at frequency of test

$I_E$  = d-c emitter current

$I_C$  = d-c collector current due to d-c emitter current (does not include  $I_{CO}$ )

$I_{CO}$  = d-c collector cutoff current

$e_{bth}$  = thermal noise from the base resistance,  $r_b'$

$\alpha$  = common-base current gain at frequency of test

$$z_e = \text{emitter diode impedance} = \frac{1}{y_e} = \frac{1}{g_e + j\omega C_e}$$

$r_e = 25/I_{Ema}$  ohms, the real part of the emitter impedance at low frequencies

$R_g$  = source resistance

Both the emitter and collector junctions have shot-noise generators, but some of the noise is due to the flow of the same charges and is, therefore, the same noise.

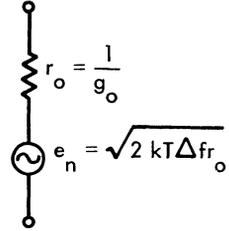


Figure 4

In other words, these two generators are strongly correlated. When we add the total noise in the output we must make an allowance for this by *subtracting* from the collector noise that part of the noise which came directly from the emitter. If the emitter shot-noise current generator is  $i_{esh}$ , the part of the noise that reaches the collector is  $\alpha i_{esh}$ . The total shot noise at the collector junction is then:

$$i_{esh(\text{total})} = i_{esh} - \alpha i_{esh}$$

To get the mean-squared value, both sides are squared and the correlation factor is taken according to van der Ziel.<sup>6</sup> The result is:

$$i_{esh(\text{total})}^2 = 2q\Delta f \left( I_C + I_{C0} + |\alpha|^2 I_E - 2|\alpha|^2 I_E \frac{\alpha_{dc}}{\alpha_o} \right) \tag{6}$$

Before we proceed with the noise-figure derivation from Fig. 5, two assumptions will be made:

1. All of the noise and signal transfer from the input of the transistor to the output will be made through transistor action via the collector current generator,  $|\alpha| i_e$ . The signal transfer through  $r_c'$  and  $z_c$  is negligible, provided  $r_c' \omega C_e \ll 1$  or  $r_b' \ll |z_c|$ .
2. The emitter impedance  $z_e$  can be approximated by its real part  $r_e$ . Again, this is true for most regions of usefulness of the transistor.

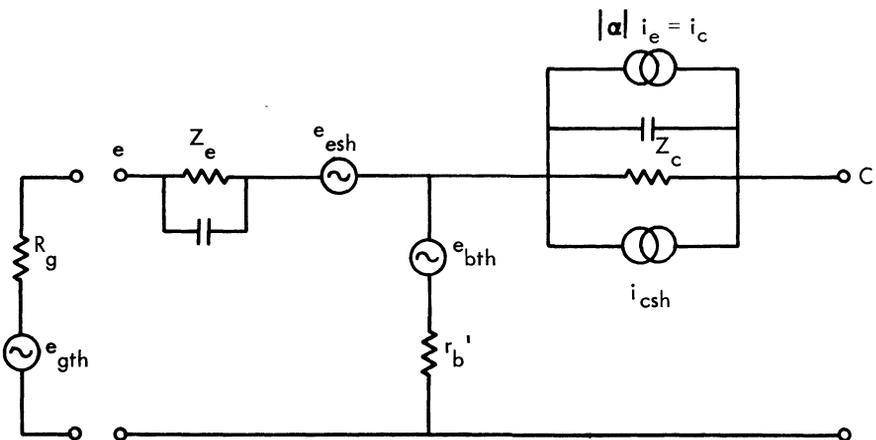


Figure 5

**NOISE FIGURE CALCULATION**

A conventional definition of noise figure is:

$$F = \frac{\text{Total mean-squared open-circuit noise voltage at transistor output}}{\text{Total mean-squared open-circuit noise voltage at transistor output from } R_g \text{ alone}} \quad (7)$$

The total noise current flowing in the emitter,  $i_{en}$ , can be found by adding the input loop noise voltages and dividing by the loop impedance.

$$i_{en} = \frac{e_{gth} + e_{esh} + e_{bth}}{(R_g + r_e + r_b')}$$

This current will appear in the output as  $|\alpha| i_{en}$ , or as an open-circuit noise voltage,  $|\alpha| i_{en} z_c$ . The three noise voltages are squared separately since they are uncorrelated. Hence, the mean-squared open-circuit noise voltage is:

$$|\alpha|^2 i_{en}^2 z_c^2 = \frac{|\alpha|^2 |z_c|^2 (e_{gth}^2 + e_{esh}^2 + e_{bth}^2)}{(R_g + r_e + r_b')^2} \quad (8)$$

The mean-squared open-circuit noise voltage from the collector is:

$$\overline{e_{oc}^2} = i_{csh}^2 |z_c|^2 \quad (9)$$

Equations (8) and (9) may now be combined to yield the numerator of Eq. (7). The denominator

$$\frac{|\alpha|^2 |z_c|^2 e_{gth}^2}{(R_g + r_e + r_b')^2}$$

is the thermal noise from the source as it appears in the output. Hence, from Eq. (7)

$$F = \frac{\frac{|\alpha|^2 z_c^2 (e_{gth}^2 + e_{esh}^2 + e_{bth}^2)}{(R_g + r_e + r_b')^2} + i_{csh}^2 |z_c|^2}{\frac{|\alpha|^2 |z_c|^2 e_{gth}^2}{(R_g + r_e + r_b')^2}}$$

Rearranging terms:

$$F = 1 + \frac{e_{esh}^2}{e_{gth}^2} + \frac{e_{bth}^2}{e_{gth}^2} + \frac{i_{csh}^2 (R_g + r_e + r_b')^2}{e_{gth}^2 |\alpha|^2}$$

The voltage and current generator now are replaced by their equivalents from Eqs. (1), (4), and (6).

$$F = 1 + \frac{r_e}{2R_g} + \frac{r_b'}{R_g} + \frac{q}{kT} \left( \frac{I_{CO} + I_C}{|\alpha|^2} + I_E - 2I_E \frac{\alpha_{dc}}{\alpha_o} \right) \frac{(R_g + r_e + r_b')^2}{2R_g} \quad (10)$$

This is not yet in a very useful form and, therefore, several more substitutions will be made. The amplitude of alpha of a transistor frequency can be assumed to behave like an RC network, thus:

$$\alpha = \frac{\alpha_o}{1 + j \frac{f}{f_\alpha}} \quad (11)$$

where  $\alpha_0$  is the low-frequency alpha (*not* the d-c  $\alpha$ ),  $f$  is the frequency of measurement, and  $f_\alpha$  is the frequency at which alpha has decreased to  $\frac{\sqrt{2}}{2} \alpha_0$  (i.e.,  $0.707 \alpha_0$ ).

From Eq. (11) we obtain:

$$|\alpha|^2 = \frac{\alpha_0^2}{1 + \left(\frac{f}{f_\alpha}\right)^2} \tag{12}$$

From Eq. (3):

$$\frac{q}{kT} = \frac{g_e}{I_E} = \frac{1}{r_e I_E} \tag{3a}$$

Also, we know that:

$$I_C = \alpha_{dc} I_E \tag{13}$$

Combining Eqs. (10), (12), (3a), and (13):

$$F = 1 + \frac{r_e}{2R_g} + \frac{r_b'}{R_g} + \frac{(R_g + r_e + r_b')^2}{2R_g r_e} \left\{ \left( \frac{I_{CO}}{I_E} + \alpha_{dc} \right) \left[ 1 + \left( \frac{f}{f_\alpha} \right)^2 \right] \frac{1}{\alpha_0^2} + 1 - \frac{2\alpha_{dc}}{\alpha_0} \right\} \tag{14}$$

Making the following assumptions:

- (a)  $\alpha_{dc} + \frac{I_{CO}}{I_E} \cong 1 + \frac{I_{CO}}{I_E}$
- (b)  $\alpha_{dc} \cong \alpha_0$
- (c)  $\frac{I_{CO}}{I_E} \ll 1$
- (d)  $\frac{\alpha_{dc}^2}{h_{FE}} \cong \frac{1}{h_{FE}}$

Eq. (14) can be manipulated to give:

$$F = 1 + \frac{r_e}{2R_g} + \frac{r_b'}{R_g} + \frac{(R_g + r_e + r_b')^2}{2\alpha_0 R_g r_e} \left[ \frac{1}{h_{FE}} + \frac{I_{CO}}{I_E} + \left( \frac{f}{f_\alpha} \right)^2 \right] \tag{14a}$$

where  $h_{FE}$  is the common-emitter d-c current gain.

The noise-figure expression of Eq. (14a) can be used for frequencies above the low-frequency corner in the plateau region and in the 6 db/octave region of Fig. 1. The accuracy with which  $F$  can be predicted from other measured parameters is approximately 0.5 db at higher frequencies due principally to difficulties in measuring  $f_\alpha$ . Parasitics such as lead inductance, header capacitance, etc., can cause large errors in measurement of  $f_\alpha$  above 500 mc. The noise figure itself may be the most accurate index of  $f_\alpha$ . At low frequencies, generator-recombination noise may cause errors in noise measurement when  $h_{FE} < 10$ . Figure 6 shows a normalized noise figure plot with the contributions of the various noise sources.

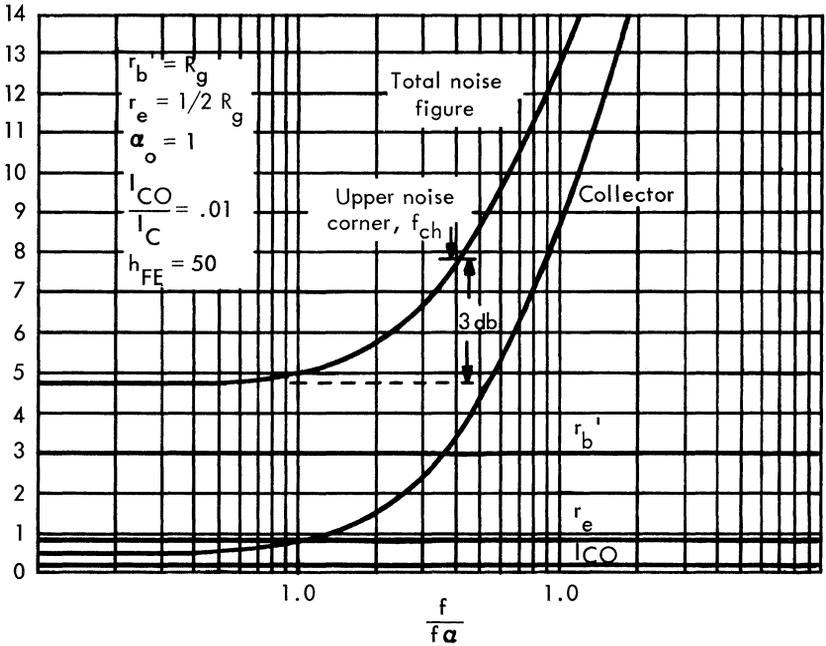


Fig. 6. Normalized transistor noise figure vs. frequency.

**OPTIMUM NOISE SOURCE**

If Eq. (14a) is examined, it will be noted that the collector term contains  $R_g$  in both the numerator and denominator, while  $R_g$  appears in the denominator only in the base and emitter terms. From this we conclude that by proper selection of  $R_g$  the noise figure can be minimized. To determine this value, we differentiate Eq. (14a), set the result equal to zero, and solve for  $R_g$ . The result  $R_{g(opt)}$  is:

$$R_{g(opt)} = \left[ (r_e + r_b')^2 + \frac{\alpha_o r_e (2r_b' + r_e)}{\frac{1}{h_{FE}} + \left(\frac{f}{f_\alpha}\right)^2 + \frac{I_{CO}}{I_E}} \right]^{1/2} \tag{15}$$

As the frequency  $f$  approaches  $f_\alpha$ , the second term becomes small and the optimum source approaches  $(r_b' + r_e)$ . At low frequencies where  $(f/f_\alpha)^2$  is small, a transistor having a high d-c current gain will require a high source resistance  $R_g$  for best noise performance.

The optimum noise source in the  $1/f$  region cannot be determined from the type of calculation described above.

**TRANSISTOR NOISE FIGURE, MEDIUM AND LOW FREQUENCIES**

In the low-frequency region, near and below the low-frequency noise corner, the  $1/f$  noise begins to dominate the noise figure. Unfortunately, there is no accurate way to predict noise in this region from known accessible parameters, and we must rely on empirical means for deriving a noise-figure expression. If the noise figure is measured carefully from the plateau region where it begins to increase, and well into the  $1/f$  region, a curve like Fig. 7 will result.

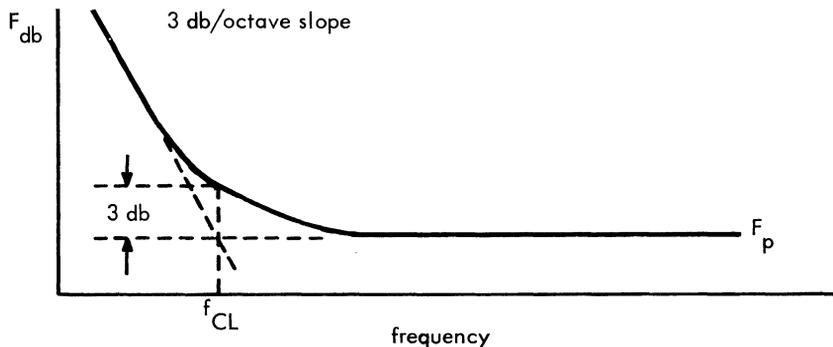


Figure 7

A tangent drawn to the low-frequency part of the curve will intersect the extension of the plateau noise figure at a point 3 db below the actual curve. The frequency at this point is called the low-frequency noise corner  $f_{CL}$ . The noise figure now can be defined for this region, using  $F_p$ , the plateau noise figure, and  $f_{CL}$ .

$$F_{low\ freq} = F_p \left( 1 + \frac{f_{CL}}{f} \right) \tag{16}$$

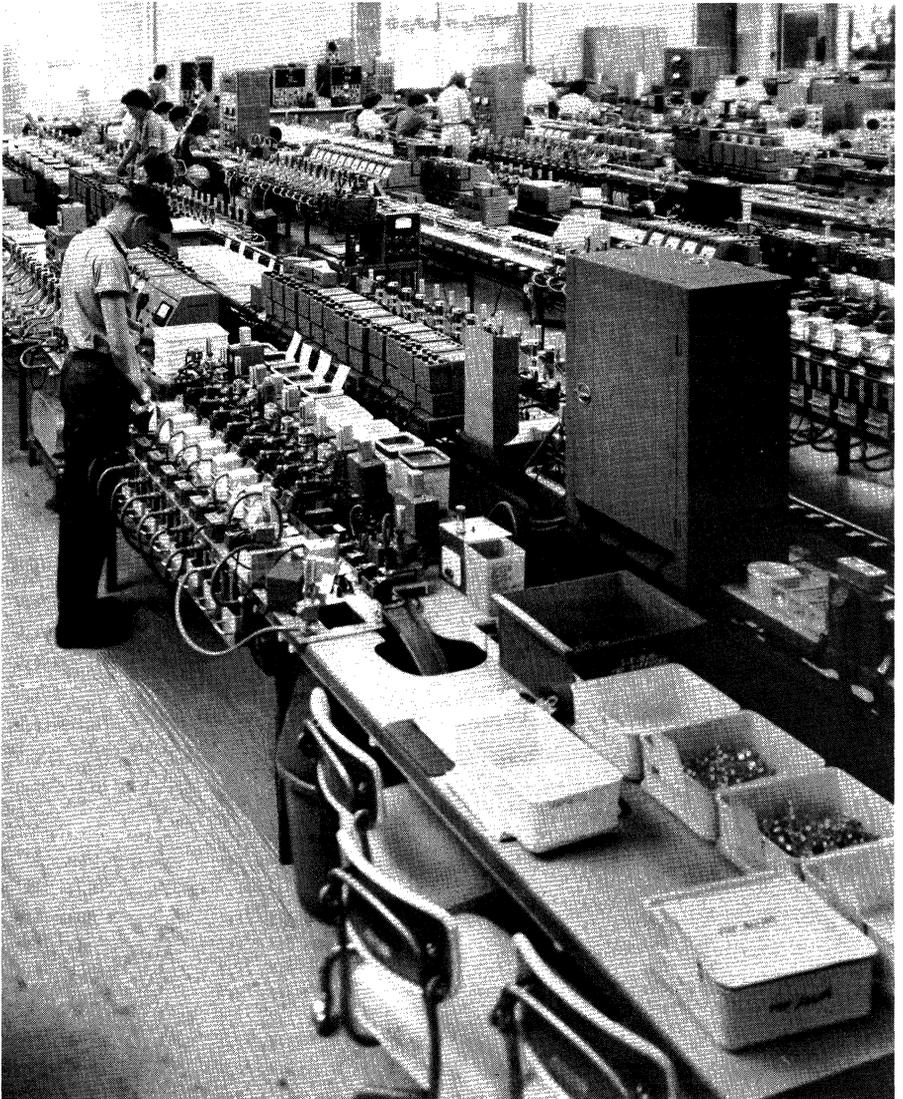
The plateau noise figure  $F_p$  is the same as Eq. (14a) except that the  $(f/f_\alpha)^2$  term is so small that it can be dropped. The low-frequency noise figure is then:

$$F_{low\ freq} = \left( 1 + \frac{f_{CL}}{f} \right) \left[ 1 + \frac{r_b'}{R_g} + \frac{r_e}{2R_g} + \frac{(R_g + r_e + r_b')^2}{2\alpha_0 R_g r_e} \left( \frac{1}{h_{FE}} + \frac{I_{CO}}{I_E} \right) \right] \tag{17}$$

Equation (17) is not as useful as Eq. (14a) since  $f_{CL}$  must be obtained by experiment. However, once the value for  $f_{CL}$  is obtained, it is usually fairly constant for a given value of transistor when operated with a given generator resistance and emitter current. Exceptions to this rule, interestingly enough, are sometimes excessive noise figures from defective transistors. The defects may not be apparent from any other measurement, but may show up after many hours of operation.

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**Centralized Automatic Testers (CATs) automatically test quantities and parameters, and categorize thousands of transistors every hour without danger of human error.**

## Communications Circuit Applications

This chapter offers forty tested circuit designs, categorized in the following order:

- Low-level Low-frequency Amplifiers
- RF Amplifiers
- Oscillators, Mixers, and Converters
- IF Amplifiers
- Power Amplifiers
- Transmitters

Although sufficient circuit information is presented to enable an experienced engineer to reproduce the circuits, these designs are presented to stimulate creative engineering, and not to serve as construction exercises.

### LOW-LEVEL LOW-FREQUENCY AMPLIFIERS

**High-impedance Low-noise Wideband Amplifier.** This broadband amplifier (Fig. 1) offers input impedances greater than 30 megohms with a noise figure of less than 3 db over a wide range of generator resistances. Bootstrapping of the input stage enhances the high input impedance of the TI 2N2498 field-effect transistor. Miller capacitance effects are reduced, permitting an extremely wide bandwidth with the use of a TI 2N930 in a grounded-base configuration following the input stage. This amplifier will operate at very low frequencies without the need for large-dimension capacitors.

*Characteristics:*

High input impedance  $> 30$  megohms

Low noise figure  $< 3$  db, 50 kilohms  $\leq R_g \leq 5$  megohms

Wide frequency response = average 1 db BW, 1 cps to 500 kc at  $R_g = 100$  kilohms

Stable voltage gain =  $40 \pm 0.5$  db from  $-55$  to  $+125^\circ\text{C}$

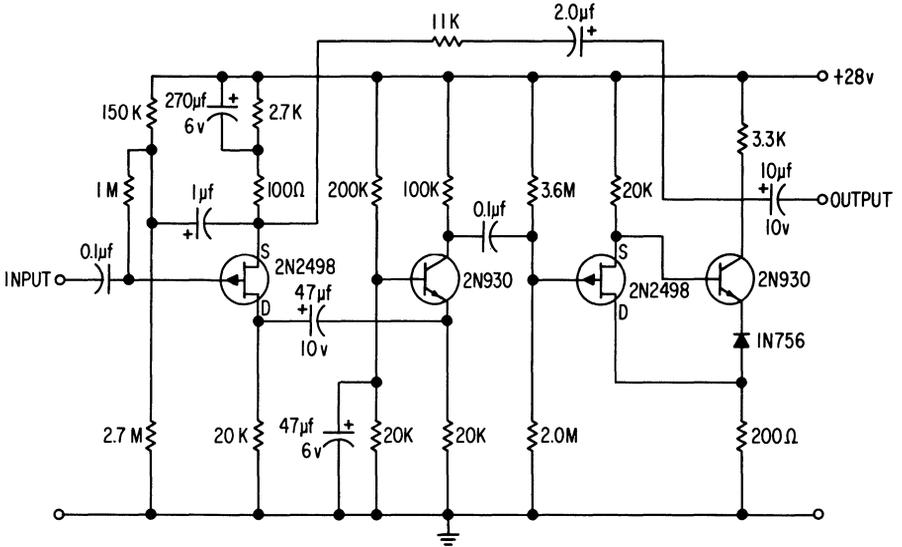


Fig. 1. High-impedance low-noise wideband amplifier.

**Two-stage Low-level D-C Amplifier Using Complementary Pair.** Both PNP and NPN dual transistors in six-lead TO-5 cases (from the 2N2802-07 and 2N2639-44 series) are used in this circuit (Fig. 2). They provide extremely high gain for greater stability and fewer stages. The circuit shown provides both low drift and high common-mode rejection for either differential or single-ended outputs.

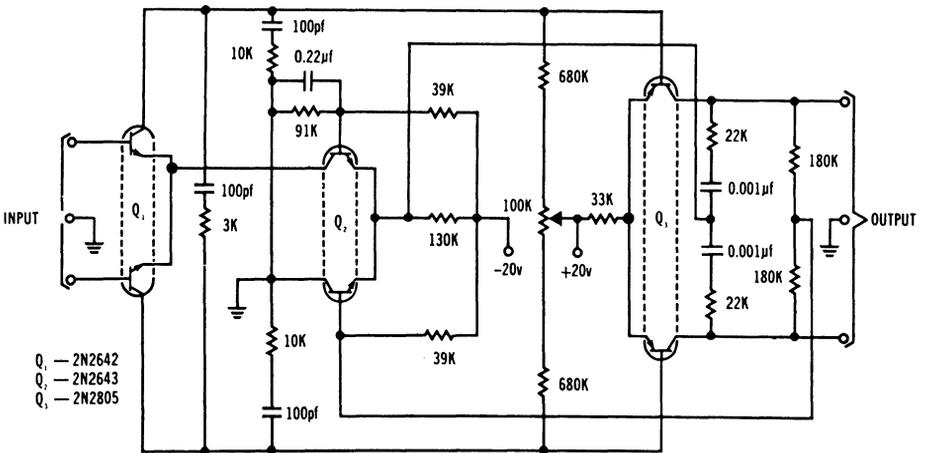


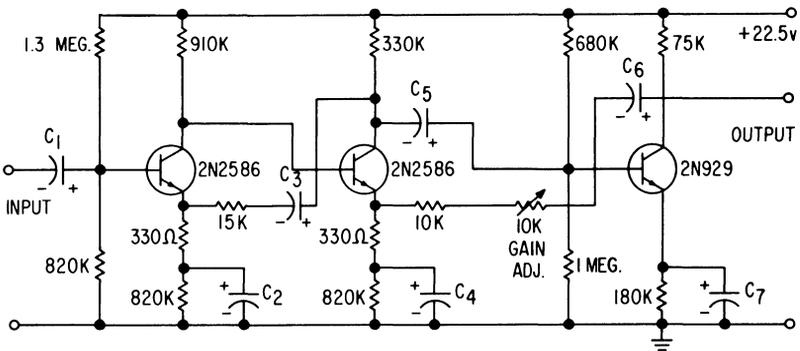
Fig. 2. Two-stage low-level d-c amplifier using complementary pair.

*Characteristics:*

- Common mode rejection ratio = 120 db
- Equivalent input current drift = 0.1 na/°C
- Equivalent input voltage drift = 3 μv/°C
- Differential input impedance = 500 kilohms min
- Low-frequency voltage gain = 68 db
- Gain-bandwidth product = 5 mc

**Low-level Low-noise Amplifier.** This low-level high-gain amplifier (Fig. 3) has a typical noise figure as low as 1 db. Advanced low-level planar technology of Texas Instruments 2N929 and 2N2586 transistors makes possible high gain at low current levels, plus the extremely low leakage currents necessary for true low-noise performance.

For high-impedance transducer applications, TI 2N930 and 2N2586 devices permit typical 1-db noise figure at emitter currents below 1 microampere and generator resistance over 1 megohm. These special characteristics allow direct coupling of low-level high-impedance sources . . . advantages previously available only with vacuum tubes and field-effect transistors. High gain at low levels plus very thin regions in these units combine to offer low power consumption and high radiation resistance, making the 2N930 and 2N2586 ideal for space applications.



- RESISTORS—ALL 1/2 watt, T1 type CD1/2 MR
- CAPACITORS
- C<sub>1</sub>, C<sub>3</sub>, C<sub>5</sub>, C<sub>6</sub> — 2μf, T1 type SCM 225FP020C4
  - C<sub>2</sub>, C<sub>4</sub> — 20μf, T1 type SCM 226BP015C4
  - C<sub>7</sub> — 20μf, T1 type SCM 226GP035C4

**Fig. 3. Typical low-level high-gain amplifier.**

*Characteristics:*

Amplifier gain = 1000 = 60 db

Feedback = 4 db at  $R_g = 1$  kilohm

NF = 0.4 db at  $R_g = 10$  kilohms

BW ( $R_g = 50$  kilohm) = 1.7 db at  $R_g = 100$  kilohms

Input impedance = 340 kilohms at 1 kc

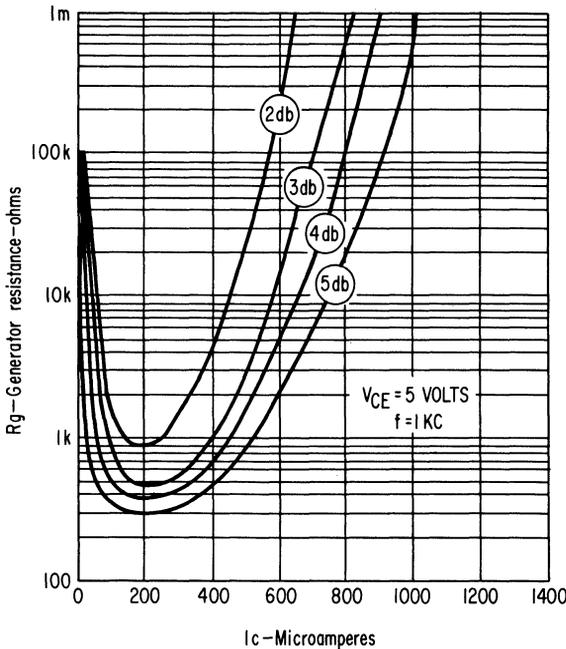
Output impedance = 12 kilohms at 1 kc

First stage biased at  $10 \mu a$

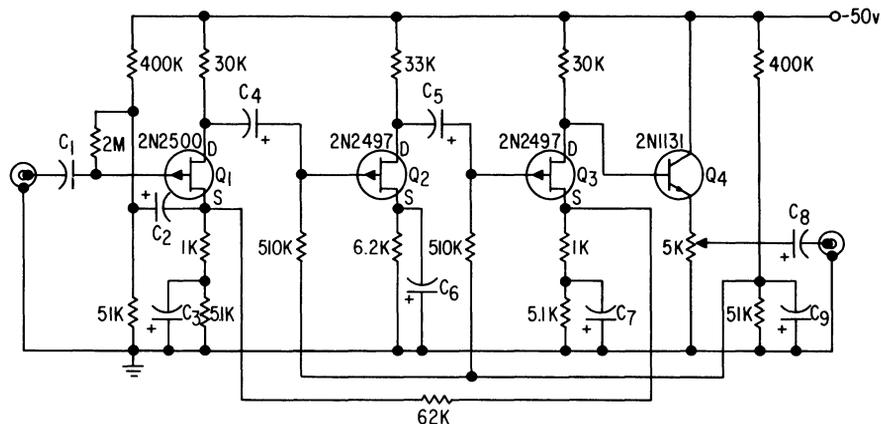
The 2N2586 is ideal for critical low-level low-noise applications such as the input stage of amplifiers taking signals from high-impedance low-level transducers. Previously, such applications required either complex transistor circuitry or vacuum tubes.

Guaranteed minimum  $h_{FE}$  at  $1 \mu a$  is 80. The guaranteed minimum low-temperature  $h_{FE}$  is 40 at  $10 \mu a$  and  $-55^\circ C$ . Because of this high available gain, simple amplifiers employing a minimum number of stages may be used.

The constant-noise contour curves for 2N2586 transistors (Fig. 4) enable you to select bias currents ( $I_C$ ) for different source resistances. Noise figures of less than 2 db are easy to obtain for high-impedance transducers such as piezoelectric strain gauges.



**Fig. 4. Constant noise contour curves, 2N2586.**



RESISTORS: All 1/2 watt, T1 Type CDI1/2MR

CAPACITORS:

C<sub>1</sub>—0.1μf

C<sub>2</sub>—5.6μf—TI Type SCM 565BP035C4

C<sub>3</sub>, C<sub>6</sub>, C<sub>7</sub>—220μf—TI Type SCM 227HP010C4

C<sub>4</sub>, C<sub>5</sub>—1.0μf—TI Type SCM 105FP035C4

C<sub>8</sub>—10μf—TI Type SCM 106BP020C4

C<sub>9</sub>—68μf—TI Type SCM 686GP015C4

Fig. 5. 60-db low-noise amplifier.

**60-db Low-noise Amplifier.** The circuit of Fig. 5 illustrates how Texas Instruments 2N2500 silicon field-effect transistors are used to achieve low-noise low-frequency operation. The 2N2497-2500 series field-effect transistors give you extremely low noise characteristics—as low as 5 db at 10 cycles. They are ideal for such low-frequency equipment as null-detection apparatus, medical research equipment, oscillographic and magnetic tape recorders, oscilloscopes, and all types of low-level transducers.

This circuit gives you a maximum voltage gain of 60 db  $\pm$  0.5 db from  $-55$  to  $125^{\circ}\text{C}$  with built-in gain adjustment. You also get good low-frequency response and stable circuit operation.

*Characteristics:*

NF = 1.5 db at  $R_g = 10$  kilohms

1.2 db at  $R_g = 50$  kilohms

1 db at  $R_g = 100$  kilohms

1 db at  $R_g = 1$  megohm

**High Input Impedance Amplifier.** You can get input impedances greater than 1 megohm for your high-impedance transducer applications (Fig. 6) by using the TI 2N930 and 2N2411. Complementary TI 2N930 (NPN) and 2N2411 (PNP) transistors, both in the TO-18 case, also allow you single power supply design for direct coupling of low-level high-impedance sources. You get greater stability, reliability, and economy because you need fewer power supplies and fewer circuit elements.

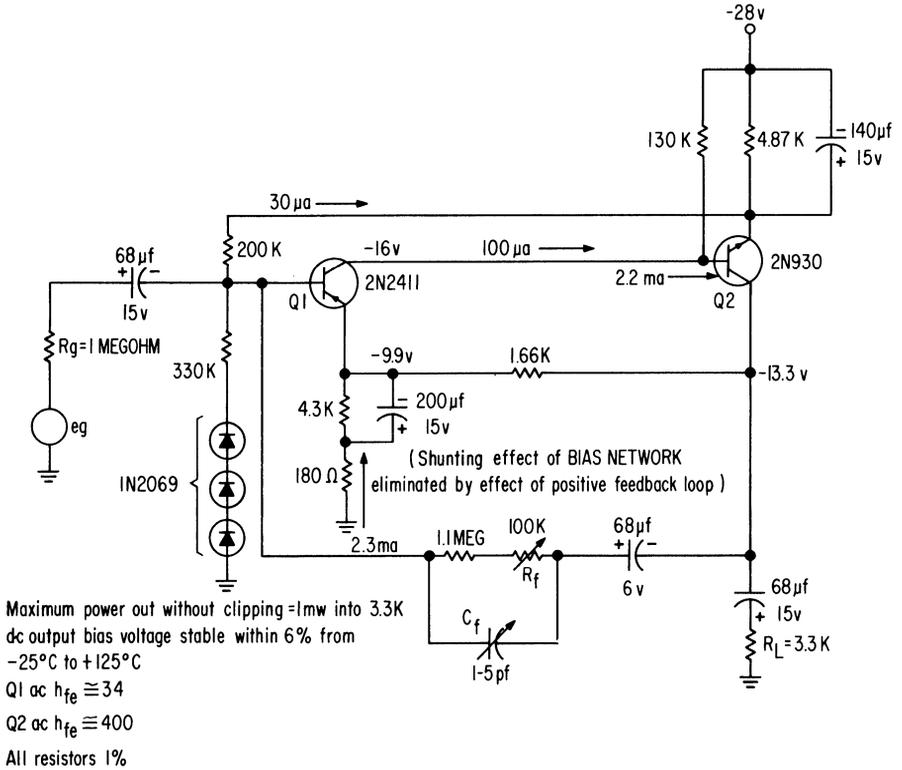


Fig. 6. High input impedance amplifier.

*Characteristics:*

Input impedance > 1 megohm

Wide frequency response =  $A_v$  1 db Bandwidth 100 cps to 230 kc at  $R_g = 1$  megohm

Low noise voltage = 1.2  $\mu v$  (rms),  $R_g = 0$

Stable voltage gain = 20 db  $\pm 0.05$  db from -25 to +125°C

Low power consumption = 65.5 mw

Small loads possible = down to 3.3 kilohms

Power gain = 46 db

(Also see Figs. 7 and 8)

**Wideband Unity-gain Amplifier.** This circuit employs a 2N2386 silicon field-effect transistor in a broadband unity-gain amplifier having an input impedance of about 100 megohms (Fig. 9). Frequency responses for various values of generator resistance are shown in Fig. 10.

Other designs may be used to extend response to d-c and give an input impedance in the order of 1000 megohms.

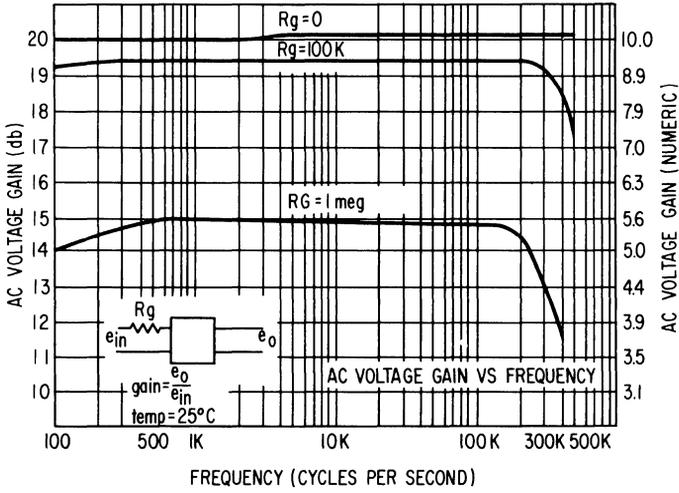


Fig. 7. A-C voltage gain vs. frequency.

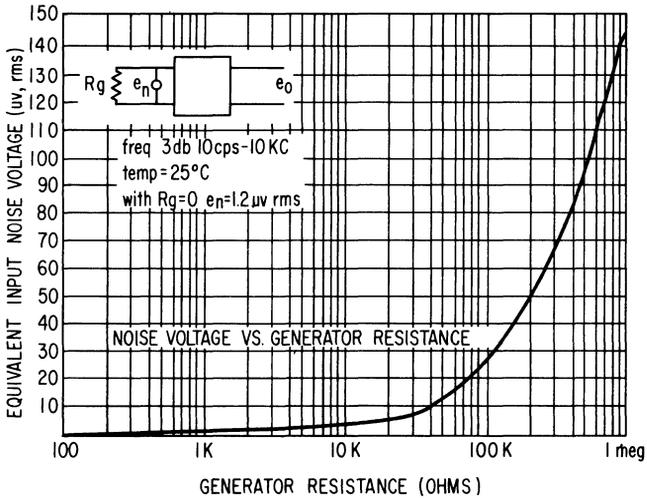


Fig. 8. Noise voltage vs. generator resistance.

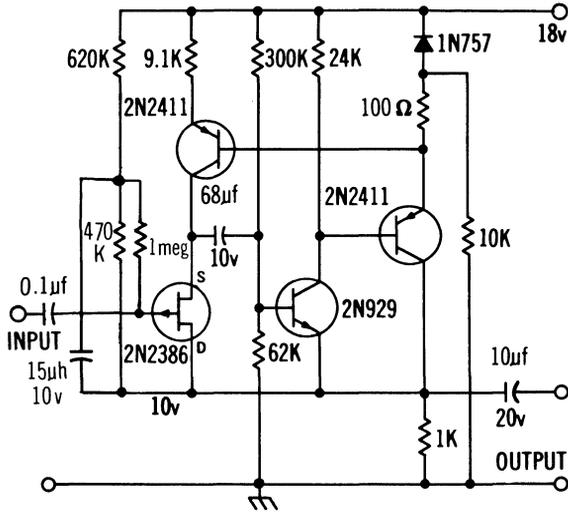


Fig. 9. High input impedance unity-gain amplifier employing 2N2386 FET.

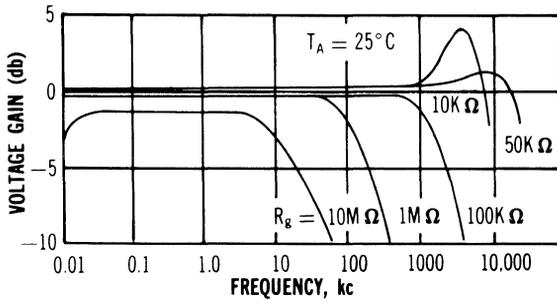


Fig. 10. Amplifier voltage gain vs. frequency for circuit of Fig. 9.

**RF AMPLIFIERS**

**60- to 90-mc Voltage-tuned Amplifier.** The close tolerance of TI's silicon XA585 voltage-variable capacitance diodes, together with a uniform slope and high Q, make the circuit shown in Fig. 11 extremely stable and give excellent tracking.

The ten new diodes from TI, typed XA580 through XA589, give capacitance ranges from 22 pf through 47 pf (at -4v), ±15% capacitance range, Q of 100 for five of the ten types, and guaranteed minimum capacitance ratios of 3.5 and 4.5 to 1.

Used in this two-stage voltage-tuned amplifier, the circuit gives more than 40-db gain from 60 to 90 mc with a 50-ohm source and 50-ohm load. The untuned input allows constant source impedance over the tunable frequency range.



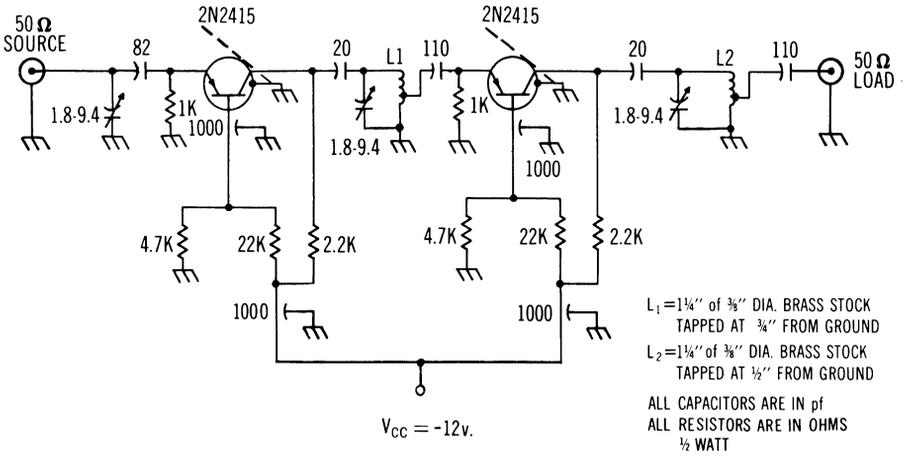


Fig. 13. 450-mc RF amplifier.

**450-mc RF Amplifier.** Figure 13 is a two-stage synchronously-tuned 450-mc RF amplifier using 2N2415 high-frequency low-noise transistors. This frequency is in the band allocated to aeronautical-navigational equipment (420-450 mc), and is also used for some telemetry systems. Tank circuits are contained in sections 1" deep by 1" wide by 2" long. Inductors are brass rods 3/8" in diameter tapped as indicated. All brass parts are silver-plated to a thickness greater than 0.5 mils to minimize losses.

The common-base configuration is used because it allows slightly more power gain than a common-emitter orientation at this frequency. The 2N2415, a diffused-base mesa transistor, is unconditionally stable at 450 mc, so that no source or load termination can be found that will cause oscillation.

*Characteristics:*

- Two-stage performance: PG = 20 db
- NF = 4.5 db
- BW = 10 mc

**UHF TV Tuner.** Figure 14 shows a low-noise highly efficient UHF tuner using 2N2415 transistors. Full design data is available to interested manufacturers.

The circuit was designed for use as a UHF television tuner, but is adaptable to other uses. Input is tunable from 470 to 890 mc. Output is 45 mc. Power requirement is only 18 ma at 12 volts. Mixer-emitter current is 0.1 ma.

On test, the tuner indicated a typical noise figure of 7 to 9 db, compared with 10 or 12 db for comparable vacuum-tube circuits. Gain was 3 to 9 db—a substantial increase over the 6-db loss usually obtained from tube circuits in the 470- to 890-mc band.

Stability was excellent. At 935 mc, temperature fluctuations from 25 to 50°C caused the local oscillator frequency to vary only 600 kc, and supply-voltage changes of 10% caused frequency variances of only 400 kc.

L<sub>1</sub> = 1 1/4" of 3/8" DIA. BRASS STOCK TAPPED AT 3/4" FROM GROUND  
 L<sub>2</sub> = 1 1/4" of 3/8" DIA. BRASS STOCK TAPPED AT 1/2" FROM GROUND  
 ALL CAPACITORS ARE IN pf  
 ALL RESISTORS ARE IN OHMS  
 1/2 WATT

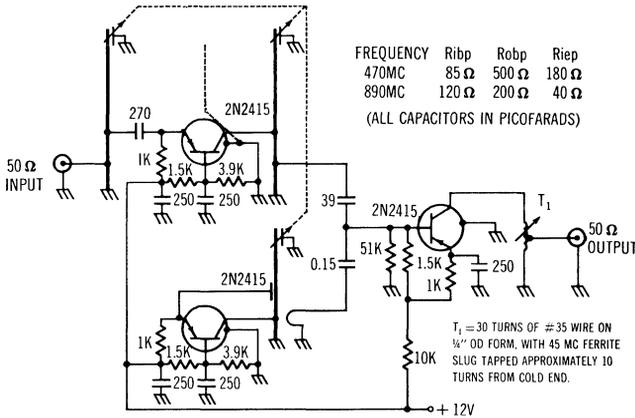
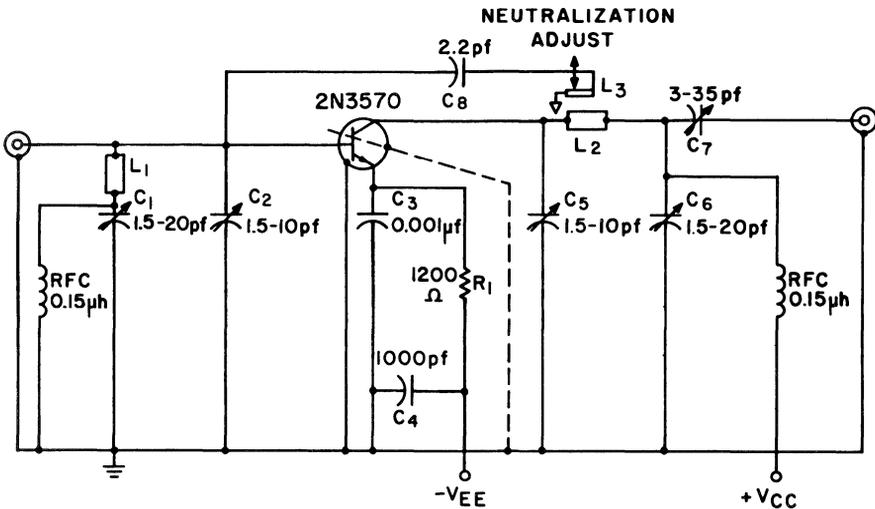


Fig. 14. UHF TV tuner.

The TI 2N2415 transistors in this circuit have an  $f_{max}$  of 3 Gc, the highest in the industry. Transistor noise figures through the UHF range are the lowest available today. A typical noise figure at 200 mc is 2.4 db. Collector-base time constant is unusually low—three picoseconds. Ruggedness of construction is confirmed by 100-percent centrifuge testing.

**500-mc Amplifier.** The TI 2N3570 provides high gain at 500 mc. Figure 15 shows how it may be used in a common-emitter single-stage amplifier. The small-signal circuit provides 17-db gain at a low 3-db noise figure (with  $R_g = 50$  ohms). It has an input impedance of 51 ohms and an output impedance of 1300 ohms in parallel with 1.8 pf. Neutralizing voltage is obtained from the coupling loop  $L_3$  which is a silver-plated strip of beryllium copper running parallel to  $L_2$ .



L<sub>1</sub>=SILVER-PLATED BRASS ROD—1 9/16" LENGTH, 1/4" DIA.  
 L<sub>2</sub>=SILVER-PLATED BRASS ROD—2 1/8" LENGTH, 1/4" DIA.

Fig. 15. 500-mc amplifier.

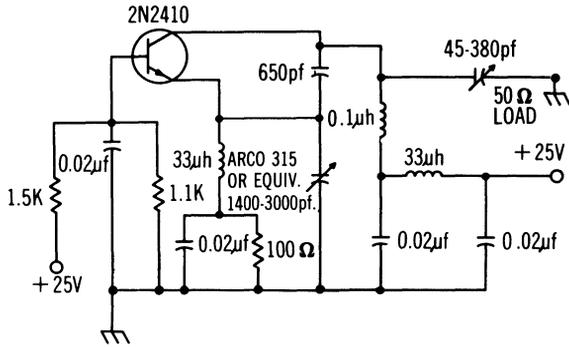


Fig. 16. 20-mc power oscillator using 2N2410.

OSCILLATORS, MIXERS, AND CONVERTERS

**20-mc Power Oscillator.** Figure 16 shows a 2N2410 in a Colpitts-type common-base oscillator circuit. Power output is about 500 mw to a 50-ohm load. The transistor dissipates about 750 mw at this output.

**30- to 5.5-mc Mixer.** This circuit mixes a 30-mc input and a 35.5-mc oscillator output to give a 5.5-mc IF signal (Fig. 17). The following shows the IF voltage output vs. the 30-mc input voltage, with an oscillator signal of 630 mv:

$V_1$	$V_{OUT}$	$(V_2 = 630 \text{ mv})$
100 $\mu\text{v}$	3.5 mv	$T_A = 25^\circ\text{C}$
1 mv	11.5 mv	
10 mv	100 mv	
100 mw	880 mv	

The 1000-pf capacitor eliminates most of the 30- and 35.5-mc signals from the output.

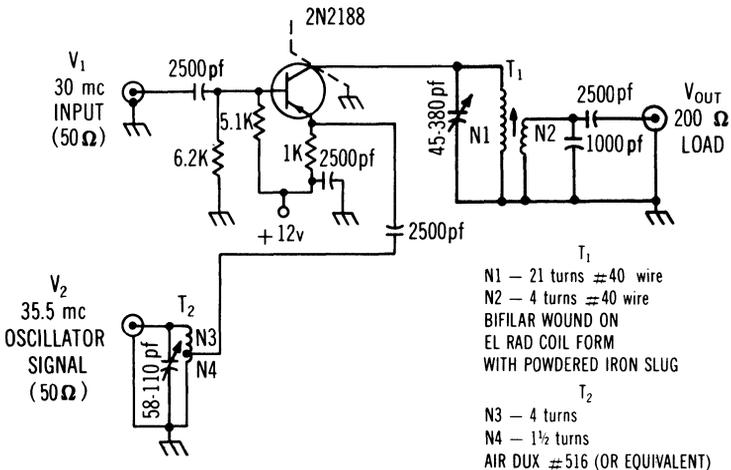


Fig. 17. 30- to 5.5-mc mixer.

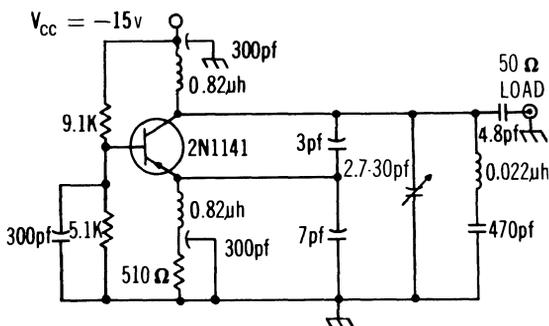


Fig. 18. 200-mc oscillator employing 2N1141.

**200-mc Oscillator.** This exceptionally stable oscillator (Fig. 18) varies less than 2 mc in frequency and 1.5 mw in power output over a temperature range of +25 to +80°C. Nominal power output is 22.5 mw at 25°C.

**500-mc Oscillator.** The Colpitts-type oscillator of Fig. 19 employs the high-frequency low-noise 2N2415 transistor. T<sub>1</sub> is a 1½" length of ⅜" brass rod with the output tap ¼" from the bottom. Frequency variation is less than 1.5 mc as bias is varied from 6 to 9 volts. Frequency varies less than 3.0 mc with temperature variations from +25 to +75°C. Typical output to the 50-ohm load is 10 mw.

**450- to 30-mc Mixer.** This straightforward design (Fig. 20) employs the low-noise high-frequency 2N2415 transistor. Figure 21 shows power gain and noise figure of the 2N2415 at various levels of emitter current.

With a local oscillator feeding one milliwatt, conversion gain was about 15 db and noise figure was about 10 db. When an RF amplifier using a 2N2415 preceded the mixer, combined power gain was 25 db and noise figure was about 6 db.

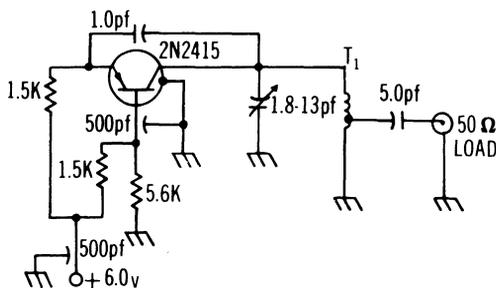
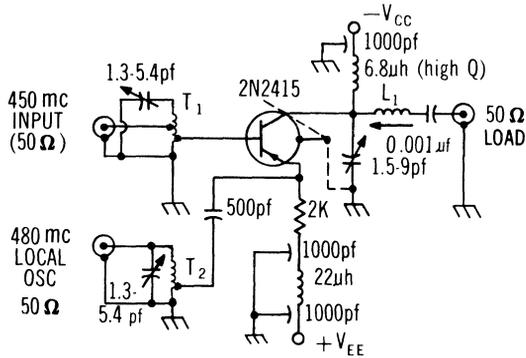


Fig. 19. 500-mc oscillator using 2N2415.



$T_1$  -  $\frac{3}{8}$ " DIA. x  $1\frac{1}{2}$ " BRASS ROD  
TAPPED AT 0.75" and 0.375"  
FROM GROUND

$T_2$  -  $\frac{3}{8}$ " DIA. x  $1\frac{1}{2}$ " BRASS ROD  
TAPPED 0.375" FROM BOTTOM

$L_1$  = 18 TURNS #30 WIRE ON CTL COIL  
FORM # PL562C4L/20063-O CLOSE  
WOUND FROM BOTTOM. SLUG GROUNDED

Fig. 20. 450- to 30-mc mixer using 2N2415.

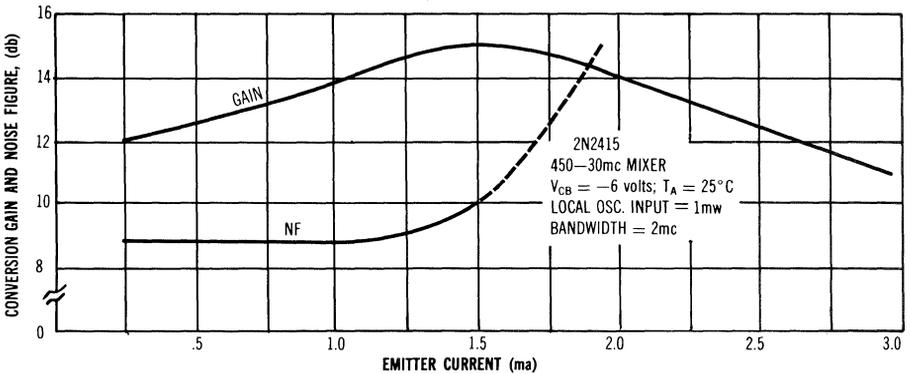


Fig. 21. Power gain and noise figure vs. emitter current, 2N2415.

**250- to 60-mc Converter.** The circuit of Fig. 22 consists of an RF amplifier, a mixer, a separate buffered local oscillator, and a two-stage IF amplifier—all using the 2N2865 transistor. Separate chassis were used to provide flexibility and utility. There is no tendency to oscillate with the RF amplifier disconnected.

The RF amplifier uses single-tuned input and output networks and provides a power gain of approximately 12 db, NF of 4.5 db ( $R_g = 50$  ohms), and a bandwidth of 13 mc.

The mixer employs separate injection with the local oscillator injected into the emitter. A single-tuned network matches the 50-ohm cable to the base. A double-tuned network is used at the output to transform down to the 50-ohm cable

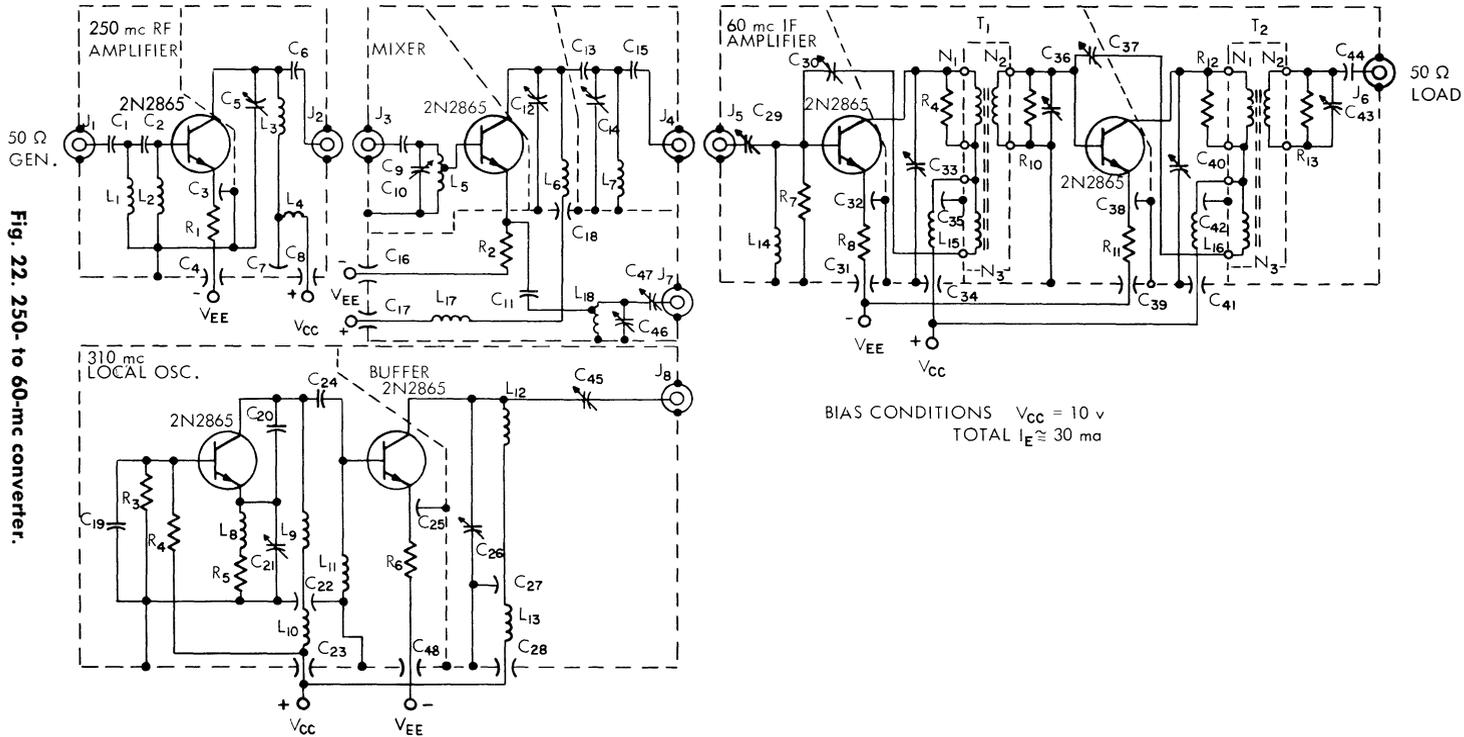


Fig. 22. 250- to 60-mc converter.

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connecting the mixer and the IF amplifier. Local oscillator injection was set at approximately 60 mv. Conversion power gain was approximately 11 db.

The 310-mc local oscillator is a Colpitts-type which feeds a common-emitter buffer. Output is connected through a matching network to the emitter of the mixer stage.

The 60-mc IF amplifier consists of two neutralized double-tuned stages with approximately 45-db power gain and an effective bandwidth of 10 mc.

### Typical Performance:

Power gain = 69 db

Bandwidth = 5 mc (-3 db)

Noise figure = 7 db ( $R_g = 50$  ohms)

Sensitivity = 3.5  $\mu$ v

Image rejection > 40 db

**450- to 105-mc Converter Using 2N2996.** The RF amplifier in the converter circuit of Fig. 23 is designed for low-noise operation at 450 mc. The 2N2996 in the common-base configuration has a typical power gain at 450 mc of 13 db, with a 5.9-db noise figure. Input is matched to the 50-ohm source and the output is coupled from a tap on  $T_1$  to the mixer input.  $R_3$  is used to obtain the desired stability factors for  $Q_1$  and  $Q_2$  for interchangeability considerations.

$Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 - 2N2996$			
$C_1$	- 10 pf	$R_1$	- 1.5 k
$C_2$	- 1.8 - 13 pf	$R_2$	- 3.0 k
$C_3$	- 1.8 - 13 pf	$R_3$	- 3.0 k
$C_4$	- 1000 pf (See $C^1$ below)	$R_4$	- 51 $\Omega$
$C_5$	- 9 - 35 pf	$R_5$	- 1.5 k
$C_6$	- 3 pf	$R_6$	- 3.0 k
$C_7$	- 9 - 35 pf	$R_7$	- 3.0 k
$C_8$	- 10 pf	$R_8$	- 3.0 k
$C_9$	- 9 - 35 pf	$R_9$	- 3.0 k
$C_{10}$	- 3.0 pf	$R_{10}$	- 1.5 k
$C_{11}$	- 9 - 35 pf	$R_{11}$	- 3.0 k
$C_{12}$	- 10 pf	$R_{12}$	- 3.0 k
$C_{13}$	- 9 - 35 pf	$R_{13}$	- 1.5 k
$C_{14}$	- 3 pf	$R_{14}$	- 1.5 k
$C_{15}$	- 9 - 35 pf	$R_{15}$	- 3.0 k
$C_{16}$	- 10 pf	$R_{16}$	- 3.0 k
$C_{17}$	- 2.5 pf	$R_{17}$	- 1.5 k
$C_{18}$	- 0.9 - 7 pf	$R_{18}$	- 3.0 k
$C_{19}$	- 0.9 - 7 pf	$R_{19}$	- 3.0 k
$C_{20}$	- 220 pf	$R_{20}$	- 510 $\Omega$
$C_{21}$	- 110 pf		
$C_{22}^1$	- 3 pf		
$C^1$	- 1000 pf (Aerovox Hi-Q EF4 by-pass cap.)		

$T_1$	- 1/2 turn of 1/4" x 1/32" copper strip, tapped approx. 1/3 up from ground
$L_1$	- 2 turns # 20 Buss wire on 1/2 watt-1 megohm resistor
$L_2$	- 0.15 $\mu$ h RFC
$L_3$	- 0.33 $\mu$ h RFC
$L_{4,5,7,8,10,11}$	- 2 1/2 turns #30 wire on Cambion LS 9 coil form (adjusted to resonate with 31 pf at 105 mc)
$L_6$	- 3.3 $\mu$ h RFC
$L_9$	- 3.3 $\mu$ h RFC
$L_{12}$	- 0.15 $\mu$ h RFC
$L_{13}$	- 2 turns #20 Buss wire on 1/2-watt - 1 megohm resistor
$L_{14}$	- 0.33 $\mu$ h RFC

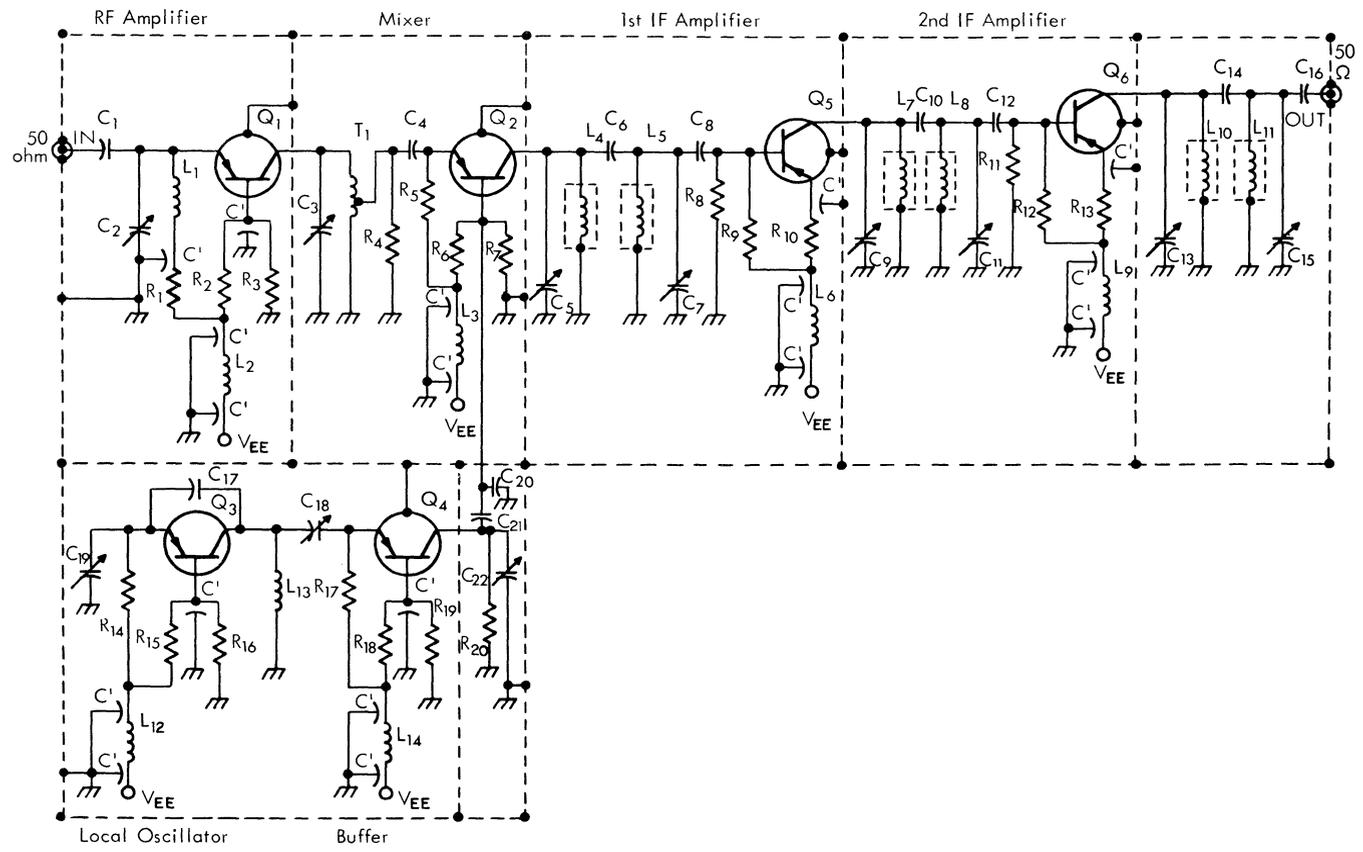


Fig. 23. 450- to 105-mc converter using 2N2996.

The 450-mc RF signal is mixed with a 345-mc oscillator signal to produce the 105-mc IF signal. Impedance at the base of the mixer is made as low as possible for maximum performance. A double-tuned network in the output attenuates all undesired signals. The 2N2996 is an excellent low-noise VHF/UHF mixer.

The stable 345-mc Colpitts oscillator is capable of 5-mw output power; however, less than 1 mw is required by the buffer stage for good mixing action. The buffer helps stabilize the oscillator by providing a relatively constant load, plus isolation from the RF signals. Buffer output is divided down for injection to the mixer with the proper signal level at a low impedance.

The 105-mc IF signal produced by the mixer is coupled to the first IF amplifier. This is a common-emitter amplifier with a stable power gain of 20 db and a noise figure of 2.5 db at 105 mc. The output circuit is another double-tuned network to further attenuate undesired signals. The second IF amplifier is identical to the first with the output coupled to a 50-ohm load.

*Typical Performance:*

Power gain = 63 db

Noise figure = 7 db

3-db bandwidth = 6.5 mc

30-db bandwidth = 20 mc

Power = +12 v at 42 ma

There are no signals above the noise level at the output with the absence of an input signal.

The 2N2998 transistor can replace the 2N2996 in the RF amplifier to provide a 3-db increase in power gain with an overall noise figure of only 3 db.

**450- to 105-mc Converter Using 2N2415.** This converter (Fig. 24) consists of a two-stage amplifier, a 450- to 105-mc mixer stage, and a 345-mc local oscillator. The two-stage RF amplifier uses the TI 2N2415, and has a typical power gain of 20 db, NF of 4.5 db, and a bandwidth of 10 mc. The mixer uses a TI 2N2415 and has a conversion gain of approximately 12 db. The local oscillator in this circuit uses a TI 2N1407.

The overall noise figure of this frequency converter is 5.0 db, and the circuit delivers a conversion gain from antenna terminals to IF strip terminals of 32 db.

## IF AMPLIFIERS

**5.5-mc IF Amplifier.** Three 2N2189 germanium Dalmesa transistors are used in this high-gain low-noise 5.5-mc IF strip (Fig. 25).

*Typical Performance:*

Power gain = 62 db

Noise figure = 4 db

Bandwidth = 0.18 mc

Response curve is shown in Fig. 26.



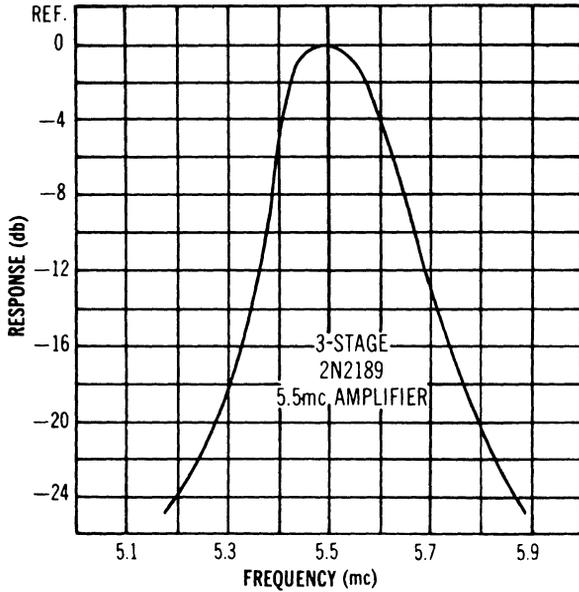


Fig. 26. Response curve for 5.5-mc IF strip.

**30-mc IF Amplifier Using 2N2410.** This circuit (Fig. 27) employs a 2N2410 epitaxial planar silicon transistor. Because of its large signal handling capability it may be used as the final stage of IF strips. Typical power gain at the indicated bias point is 16 db.

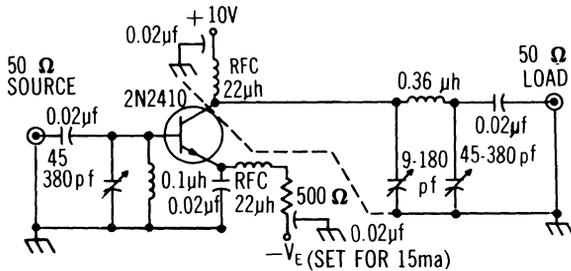


Fig. 27. 30-mc amplifier using 2N2410.

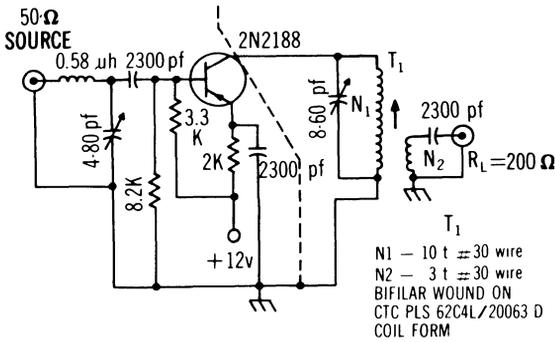


Fig. 28. 30-mc IF amplifier using 2N2188.

**30-mc IF Amplifier Using 2N2188.** The 2N2188 Dalmesa transistor is used in this circuit (Fig. 28), which includes an L-section to give an  $R_g$  of 350 ohms from a 50-ohm source. Typical performance is 13-db power gain, 4-db noise figure, and 5-mc bandwidth. Noise characteristics of the 2N2188 are shown in Fig. 29.

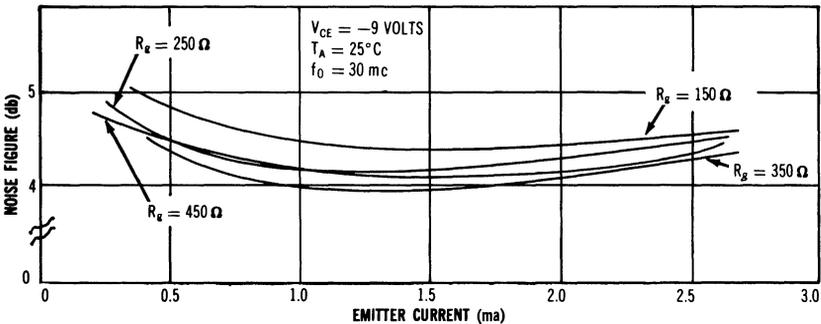


Fig. 29. Noise figure vs. emitter current, 2N2188 series.

**30-mc Double-tuned Amplifier.** The amplifier of Fig. 30 demonstrates the gain and noise capabilities of the 2N2996 at 30 mc. Good stability is achieved through proper loading, even though the 2N2996 is potentially unstable at this

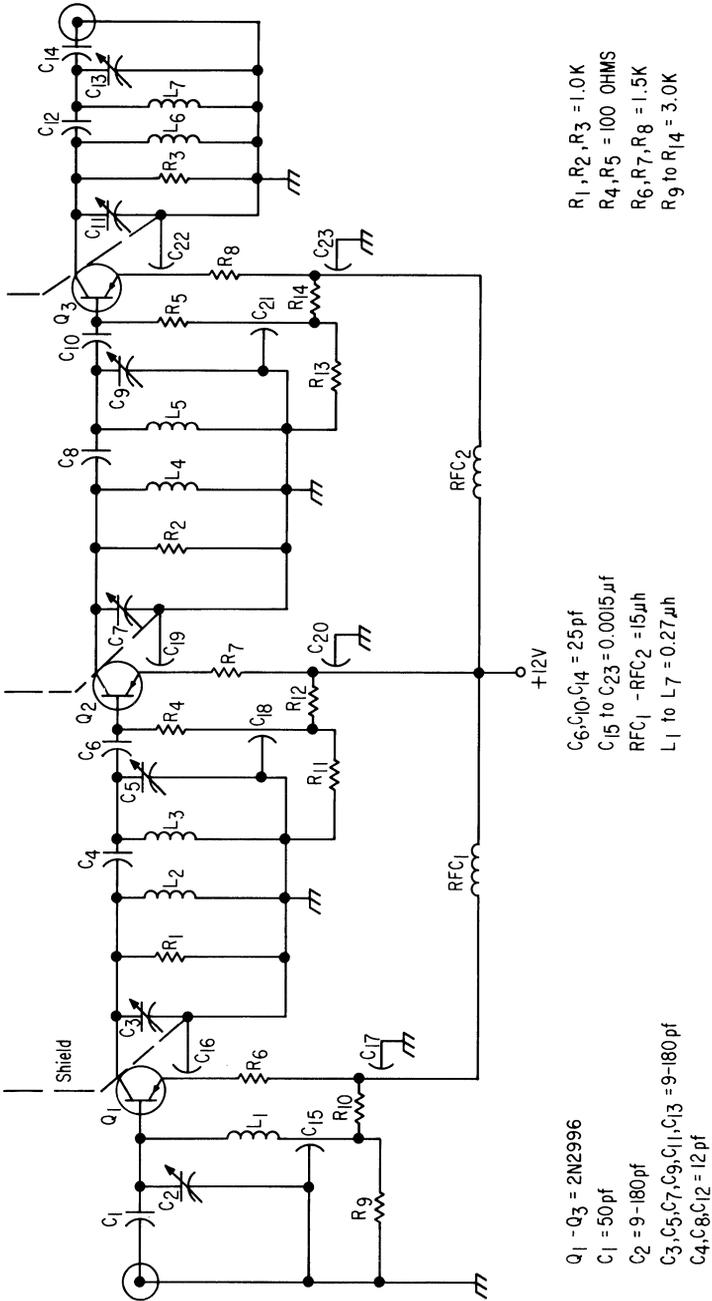


Fig. 30. 30-mc double-tuned amplifier.

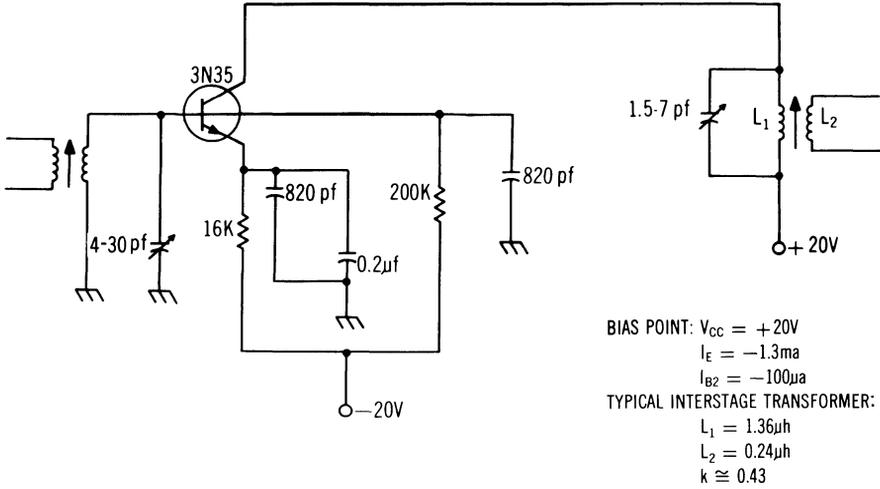


Fig. 31. 60-mc tetrode IF amplifier.

frequency. Even with the necessary loading, the amplifier has a good gain figure of 21-db gain per stage.

*Typical Performance:*

Power gain  $\approx 63$  db

Bandwidth = 3 mc

Noise figure = 2.3 db

**60-mc Tetrode IF Amplifier.** The 3N35 grown-junction tetrode transistor offers several advantages for 60-mc use (see Fig. 31). AGC characteristics are excellent and power requirements are much lower than for other silicon transistors at this frequency. Typical stage gains of 12 db are obtainable.

**60-mc IF Amplifier Using 2N743.** This circuit (Fig. 32) takes advantage of the excellent gain and noise figure capabilities of 2N743 silicon epitaxial transistors. Alignment is simplified because of the unconditional stability of the 2N743 at this frequency, and the heavy mismatch. Higher gains—up to 16 db per stage—are possible with a conjugate match at the output.

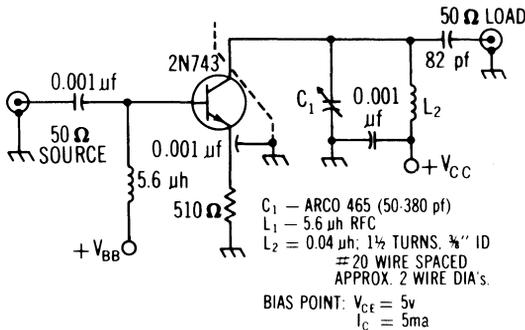
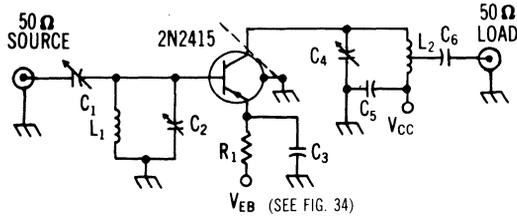


Fig. 32. 60-mc IF amplifier using 2N743.



- $C_1=5.3 - 102$  pf
- $C_2=3.7 - 52$  pf
- $C_3=0.01$  uf
- $C_4=3.7 - 52$  pf
- $C_5=0.01$  uf
- $C_6=0.01$  uf
- $L_1$  3T #14 WIRE  $\frac{1}{2}$ " DIA; = 0.25 uh
- $L_2$  4T #610 AIR DUX (OR EQUIV.); = 0.35 uh TAPPED APPROX. 1 TURN UP FROM BOTTOM
- $C_1$  IS ADJUSTED TO GIVE DESIRED VALUE OF  $R_g$
- \*4th LEAD GROUNDED.  $R_1 = 1K \frac{1}{2} W$
- BIAS POINT:  $-6V$ .  $I_E$  (SEE FIG. 34)

Fig. 33. 70-mc low-noise amplifier.

Typical Performance:

Power gain = 13 db

Bandwidth = 20 mc

Noise figure = 5.5 db

**70-mc Low-noise IF Amplifier.** Dalcom 2N2415 transistors make possible extremely low noise IF strip circuitry in the 70-mc region. A typical amplifier stage design is shown in Fig. 33; Fig. 34 displays the noise figures available at various emitter currents and generator resistances.

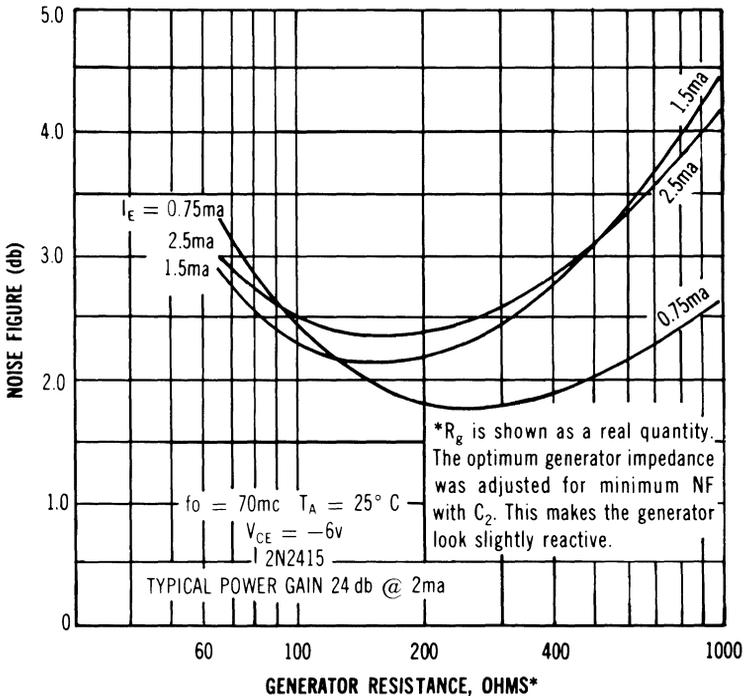


Fig. 34. Noise figure vs. generator resistance, 2N2415 at 70 mc.

**70-mc Neutralized Amplifier.** Chief design objective for the circuit in Fig. 35 was to achieve as much power gain as possible using only a single stage and maintaining good circuit stability.

*Typical Performance:*

(Conditions:  $V_{CB} = -6v$ ,  $I_C = -2\text{ ma}$ )

Power gain = 27 db

Noise figure < 3 db

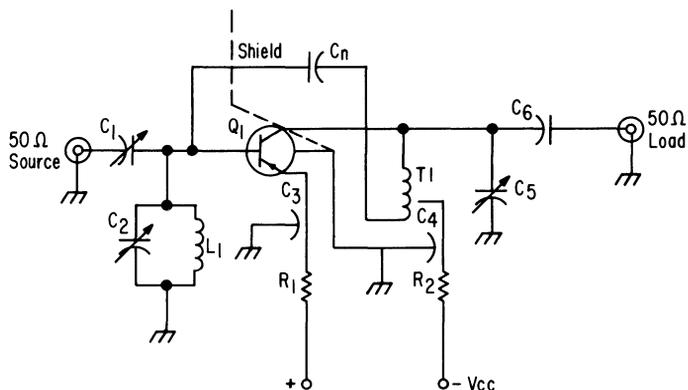
**105-mc IF Amplifier.** The circuit in Fig. 36 demonstrates that the 2N2996 still has excellent gain and noise capabilities at 105 mc. Although the 2N2996 is potentially unstable at 105 mc, proper loading yields good stability and still permits the circuit to achieve 19 db of gain per stage.

*Typical Performance:*

Power gain = 38 db

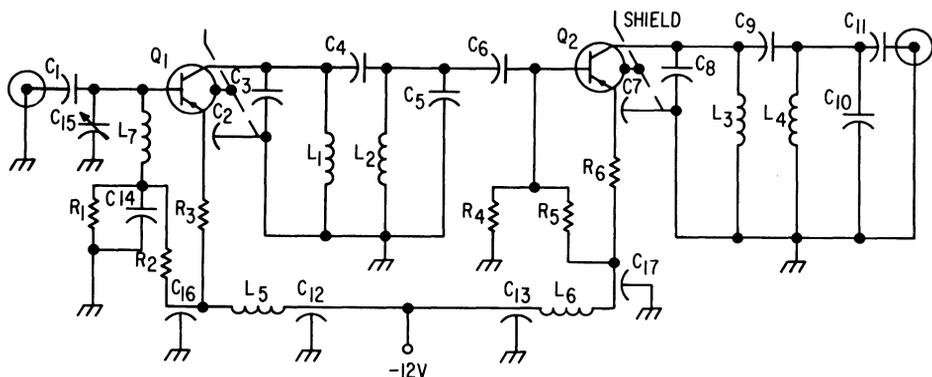
Bandwidth = 8 mc

Noise figure = 2.5 db



- |  |  |
|--|--|
| $Q_1 = 2N2996$                         | $C_n = 3.9\text{ pf}$                                  |
| $C_1, C_2 = 6.0\text{--}140\text{ pf}$ | $R_1 = 2.7\text{ k}$                                   |
| $C_3, C_4 = .001\text{ }\mu\text{f}$   | $R_2 = 1.0\text{ k}$                                   |
| $C_5 = 2\text{--}30\text{ pf}$         | $L_1 = 0.06\text{ }\mu\text{h}$                        |
| $C_6 = 10\text{ pf}$                   | $T_1$ 5 Turns No. 516 air dux tapped 4T from collector |

**Fig. 35. 70-mc neutralized amplifier.**



Q1,2 = 2N2996

L<sub>1</sub>, L<sub>2</sub>, L<sub>3</sub>, L<sub>4</sub> = 2 1/2 TURNS # 30 WIRE ON CAMBION

LS9 COIL FORM (ADJUSTED TO RESONATE WITH 31pf AT 105mc)

L<sub>5</sub>, L<sub>6</sub> = 3.3μh

L<sub>7</sub> = 0.07μh

R<sub>1</sub>, R<sub>2</sub>, R<sub>4</sub>, R<sub>5</sub> = 3K

R<sub>3</sub>, R<sub>6</sub> = 1.5K

C<sub>1</sub> = 250pf

C<sub>2</sub>, C<sub>7</sub>, C<sub>12</sub>, C<sub>13</sub>, C<sub>14</sub> = 1000pf

C<sub>3</sub>, C<sub>5</sub>, C<sub>8</sub>, C<sub>10</sub> = 9-35 pf

C<sub>4</sub>, C<sub>9</sub> = 1.3-5.4pf

C<sub>6</sub> = 1.5-20pf

C<sub>11</sub> = 10pf

C<sub>15</sub> = 9-180pf

C<sub>16</sub>, C<sub>17</sub> = 1000pf

Fig. 36. 105-mc IF amplifier.

**500-mc Staggered-tuned Amplifier.** The amplifier of Fig. 37 is a two-stage slightly staggered type that offers excellent stability. This circuit will not oscillate with either an open circuit load or source. Midband gain is 21 db, and power requirement is 7 ma at 15 v.

## POWER AMPLIFIERS

**70-watt Audio Amplifier.** Figure 38 shows a 70-watt audio amplifier output stage using the advanced TI3031 germanium alloy power transistor, which gives you the industry's highest power-to-cost ratio in a JEDEC TO-3 package. The output is capacitor coupled and does not require transformer coupling to the speaker coil. Thus, there is a significant cost reduction in output coupling to complement the low cost of the TI3031 transistors.

Characteristics: 90 watts at 55°C case temperature, 7-amp collector current, 45-120 volts  $BV_{CBO}$ , minimum  $h_{FE}$  of 40 at 3 amps.

Other consumer and industrial applications include electronic organs, d-c converters, series regulators for power supplies, light flashers, and tape recorder bias oscillators.

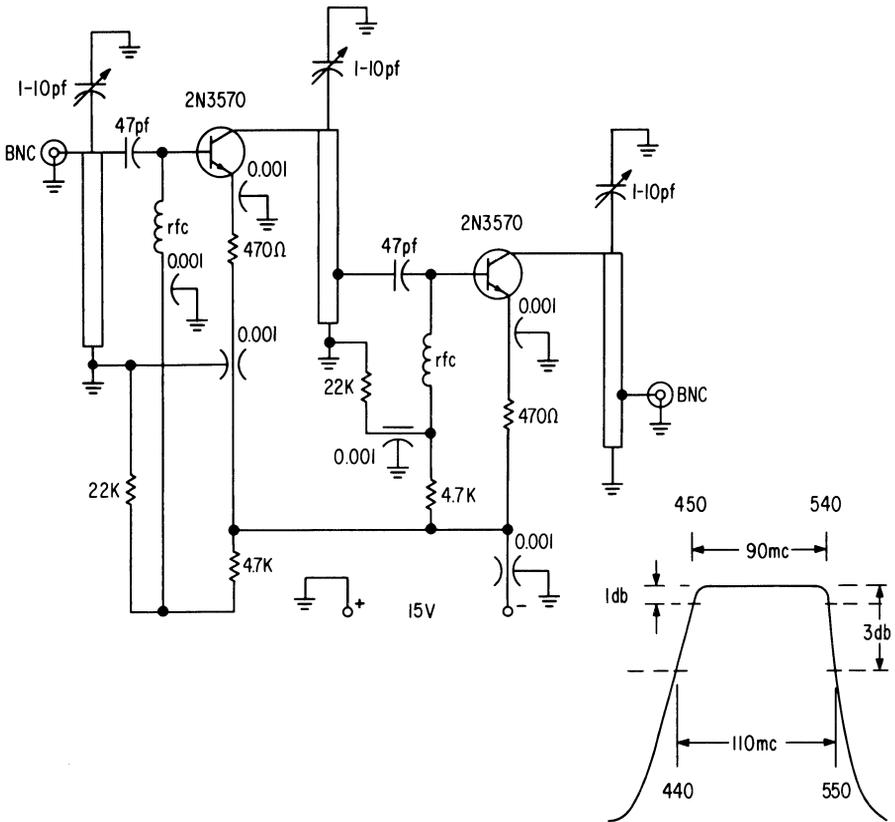


Fig. 37. 500-mc staggered-tuned amplifier.

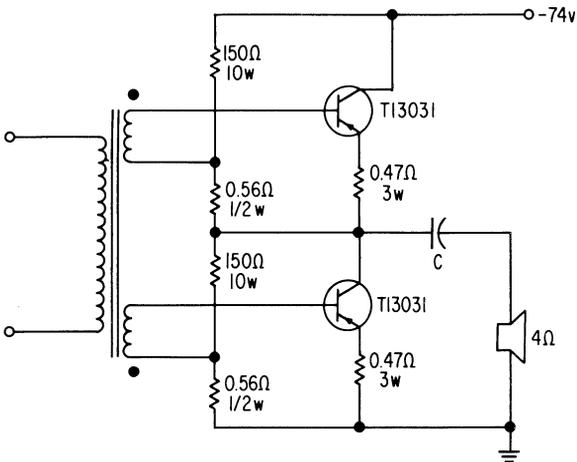


Fig. 38. 70-watt audio amplifier stage using TI3031.

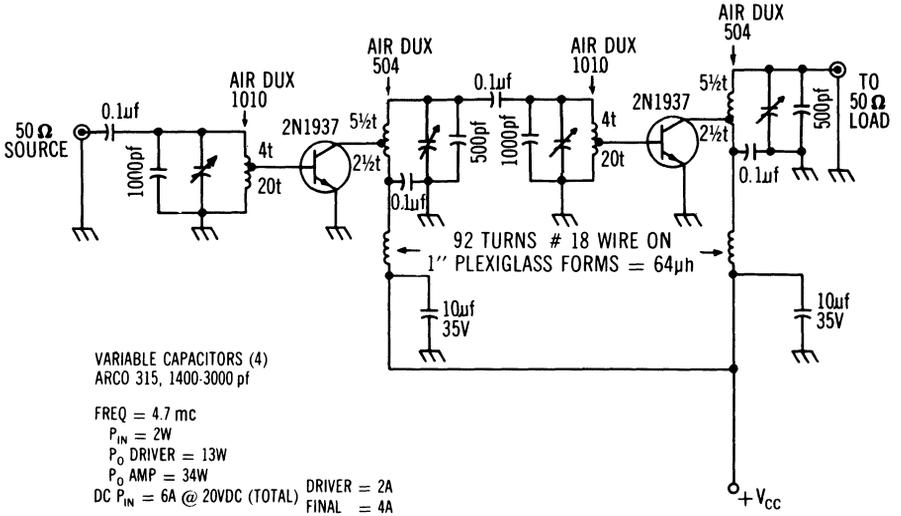


Fig. 39. 4.7-mc two-stage drive and amplifier.

**4.7-mc Driver and Amplifier.** This two-stage driver and amplifier (Fig. 39) employs two 2N1937's in a common-emitter circuit. Figure 40 shows characteristics of the 2N1937 with  $V_{CE}$  of 20 volts.

**50-mc Power Amplifier.** Figure 41 is the schematic of an amplifier stage used to test the characteristics of the 2N2410 for power amplifier service. Values shown are for 50-mc common-base operation.

Operating characteristics of the 2N2410 transistor are shown in Figs. 42 through 45.

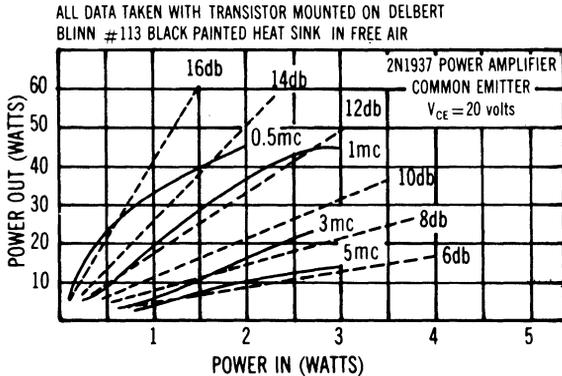


Fig. 40. Common-emitter amplifier characteristics, 2N1937.

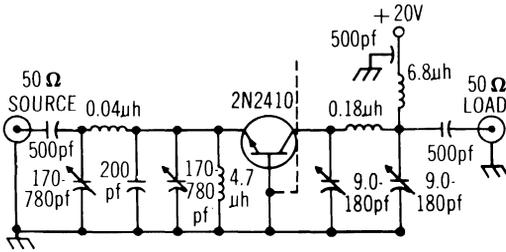


Fig. 41. 50-mc power amplifier using 2N2410.

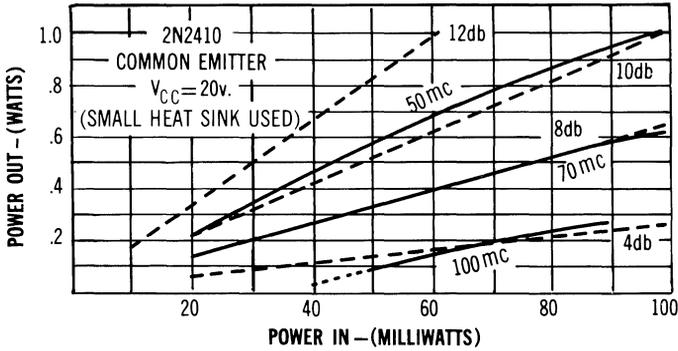


Fig. 42. Common-emitter amplifier characteristics, 2N2410.

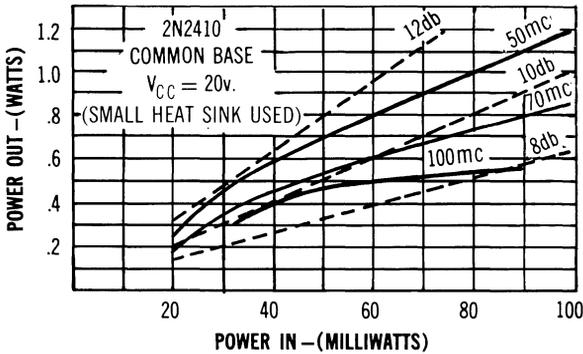


Fig. 43. Common-base amplifier characteristics, 2N2410.

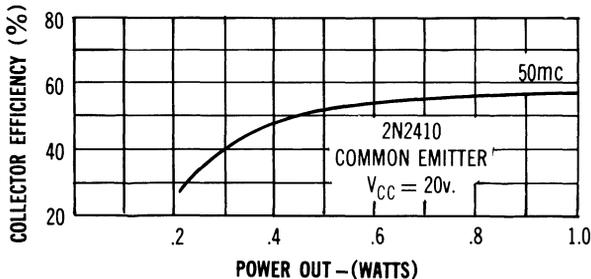


Fig. 44. Collector efficiency, 2N2410 as common-emitter amplifier at 50 mc.

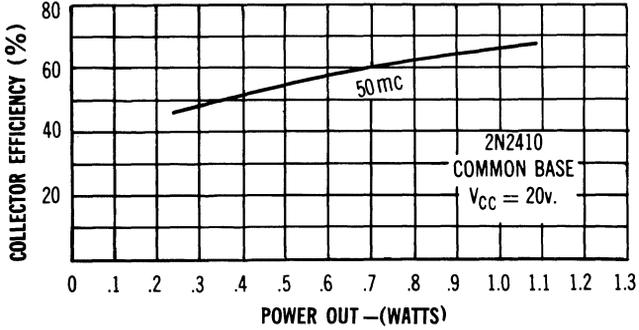


Fig. 45. Collector efficiency, 2N2410 as common-base amplifier at 50 mc.

**160-mc Power Amplifier.** This circuit (Fig. 46) is designed to operate as a Class C power amplifier at 160 mc with a power output of approximately 750 mw.

Since the minimum  $BV_{CBO}$  rating is 60 v, the collector supply is limited to 30 v. The  $BV_{CEO}$  rating is only 40 v; however, the common-emitter circuit is essentially in a  $BV_{CES}$  condition and the breakdown characteristic is the same as  $BV_{CBO}$ .

Pi matching networks are used at the input and output to reflect the proper impedance to the transistor for maximum performance. The transistor was measured with a 2" x 2" x 1/2" aluminum plate attached.

The circuit was constructed on a 0.032" brass chassis with a metal shield passing between the collector and emitter pins of the transistor socket. The output coil has an unloaded Q of 220 and the loaded Q is designed for a value of 10.

Power output was measured with a 50-ohm Hewlett-Packard Bolometer Mount, Model 476A. Power gain is the ratio of this power to the power measured out of the signal source into the same bolometer mount. See Figs. 47 and 48.

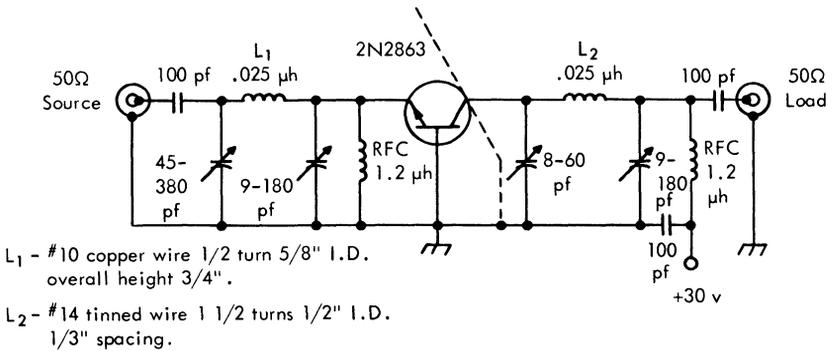


Fig. 46. 160-mc power amplifier.

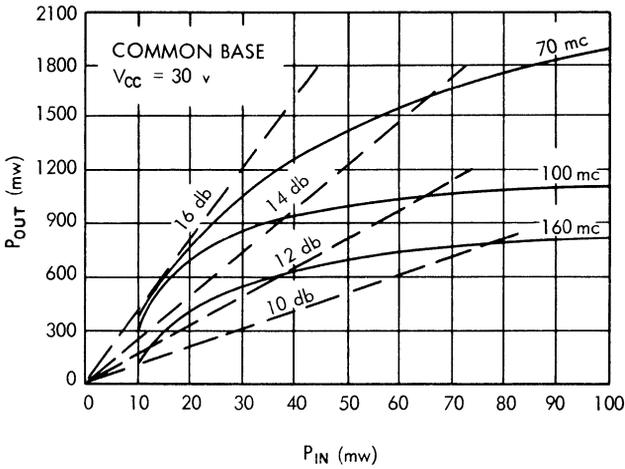


Fig. 47. Power out vs. power in, 2N2863 in common-base configuration.

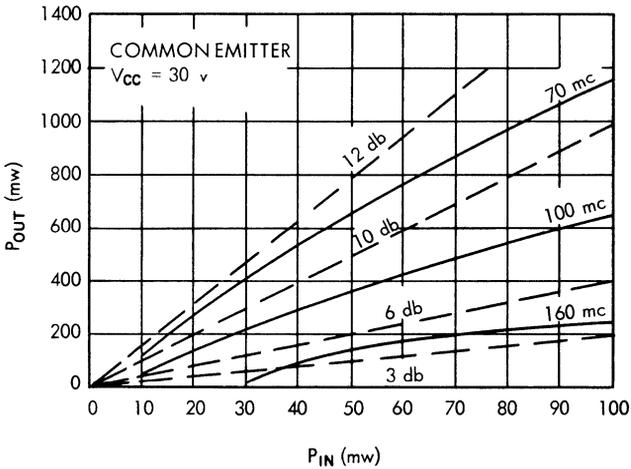


Fig. 48. Power out vs. power in, 2N2863 in common-emitter configuration.

*Typical Performance:*

- Supply voltage = 30 v
- Power output = 750 mw
- Efficiency = 25%
- 3-db bandwidth = 15 mc

**173-mc Power Amplifier.** The 2N1141 transistor is useful to 500 mc and delivers excellent large-signal performance at 173 mc in the power amplifier cir-

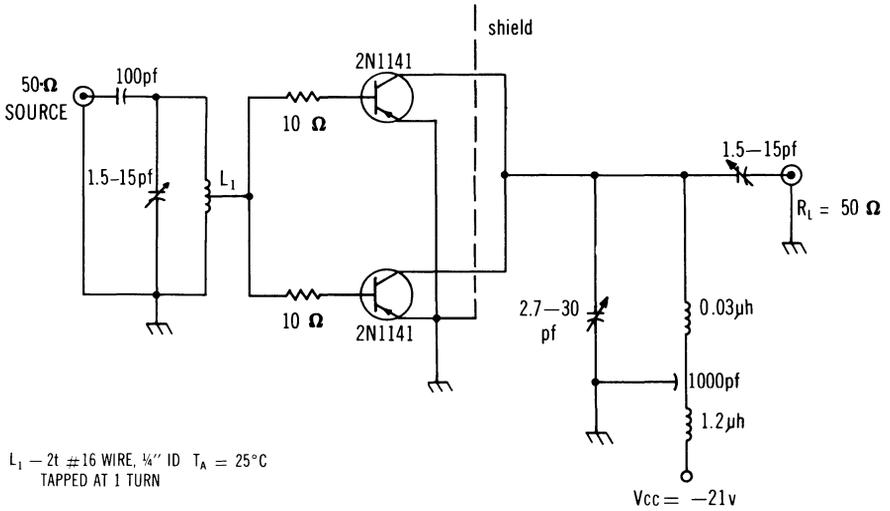


Fig. 49. 173-mc amplifier.

cuit of Fig. 49. Two 2N1141's are connected in parallel to deliver an average of 400 mw to a 50-ohm load. Base resistors equalize input signal power to the transistors. Small heat sinks (JADERO #1101 or equivalent) are used.

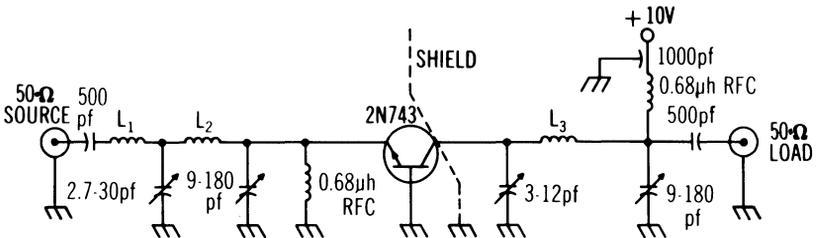
*Typical Performance:*

Power output = 400 mw

Power gain = 11.5 db

Collector efficiency = 41.8%

**250-mc Power Amplifier.** The 2N743 gives good large-signal performance as well as good small-signal performance. Figure 50 shows a common-base power amplifier test circuit with component values selected for 250-mc operation.



INDUCTANCE DATA

COIL NO.	AIR DUX NO.	NO. TURNS
$L_1$	404	5
$L_2$	408	2
$L_3$	404	3

Fig. 50. 250-mc common-base power amplifier.

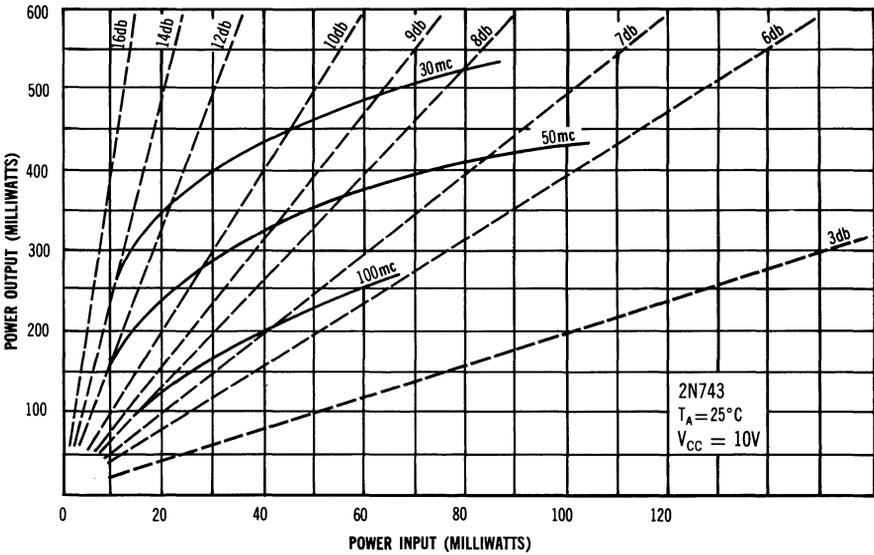


Fig. 51. Common-emitter amplifier characteristics, 2N743.

Figure 51 gives common-emitter amplifier performance, Fig. 52 gives common-base performance, and Fig. 53 indicates the desirable frequency at which to switch from common-emitter to common-base for two fixed drive levels.

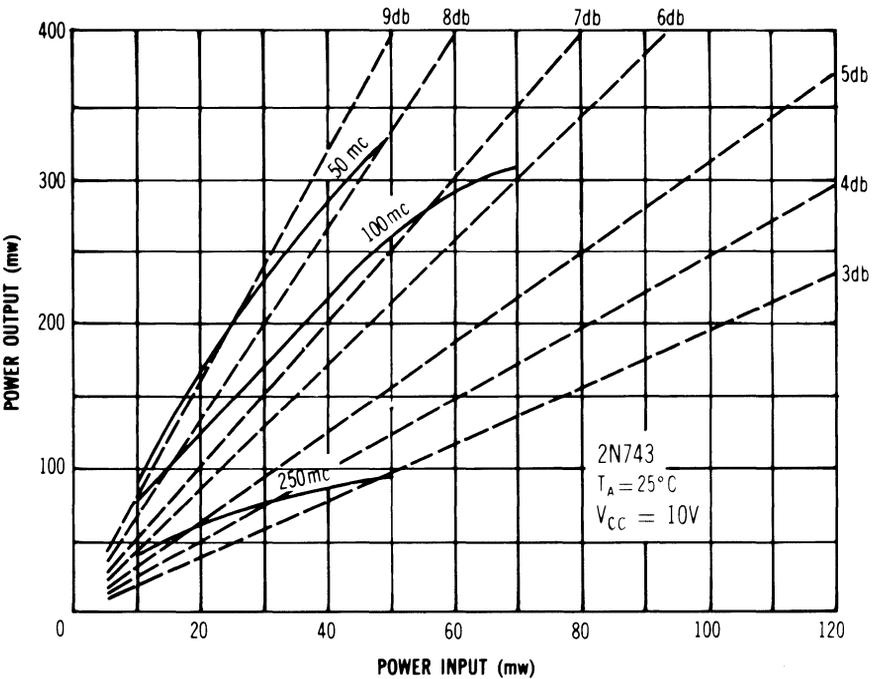


Fig. 52. Common-base amplifier characteristics, 2N743.

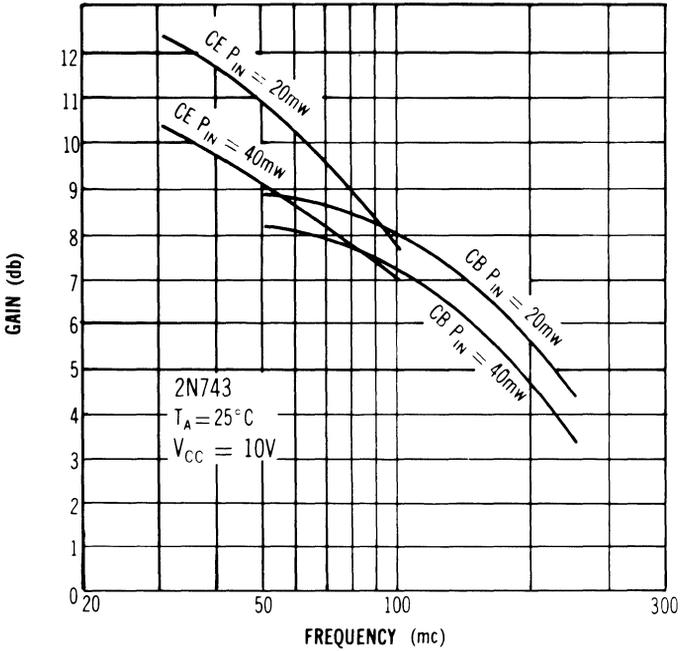
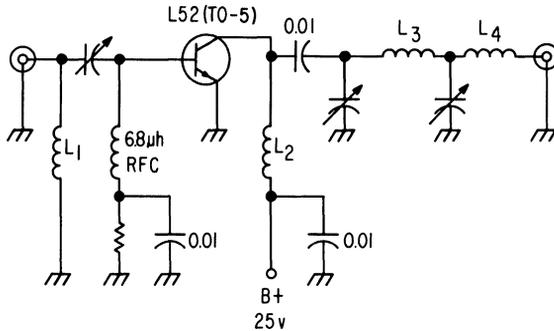


Fig. 53. Combined power amplifier characteristics, 2N743.

TRANSMITTERS

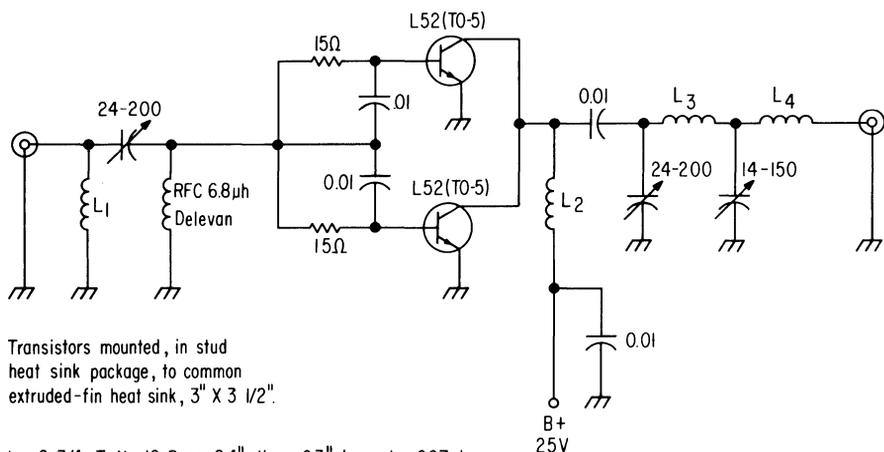
**1-watt 50-mc Transmitter.** TI's new L-52 makes 1 watt at 50 mc easily obtainable. The circuit of Fig. 54 is a common-emitter Class C amplifier with a  $\pi$ -L output circuit matching to a 50-ohm antenna. The input impedance matching network is designed to make the input impedance 50 ohms.



- $L_1 = 3\text{T NO. 16 Buss, } 0.4 \text{ diam, } 0.3'' \text{ long, } L = 0.085\mu\text{h}$
- $L_2 = 4\text{T NO. 16 Buss, } 0.4 \text{ diam, } 0.4'' \text{ long, } L = 0.12\mu\text{h}$
- $L_3 = 8\text{T NO. 16 Solderize, } 0.5 \text{ diam, } 0.5'' \text{ long, } L = 0.5\mu\text{h}$
- $L_4 = 10\text{T NO. 16 Solderize, } 0.4 \text{ diam, } 0.6'' \text{ long, } L = 0.34\mu\text{h}$

Power out = 1w  
 Power gain = 10 db

Fig. 54. 1-watt 50-mc transmitter.



Transistors mounted, in stud heat sink package, to common extruded-fin heat sink, 3" X 3 1/2".

- $L_1 = 2 \frac{3}{4}$  T No. 16 Buss, 0.4" diam, 0.3" long,  $L = .067 \mu h$
- $L_2 = 5$  T No. 16 Buss, 0.4" diam, 0.4" long,  $L = .14 \mu h$
- $L_3 = 5$  T No. Solderize, 0.5" diam, 0.4" long,  $L = .22 \mu h$
- $L_4 = 6$  T No. Solderize, 0.5" diam, 0.5" long,  $L = .34 \mu h$

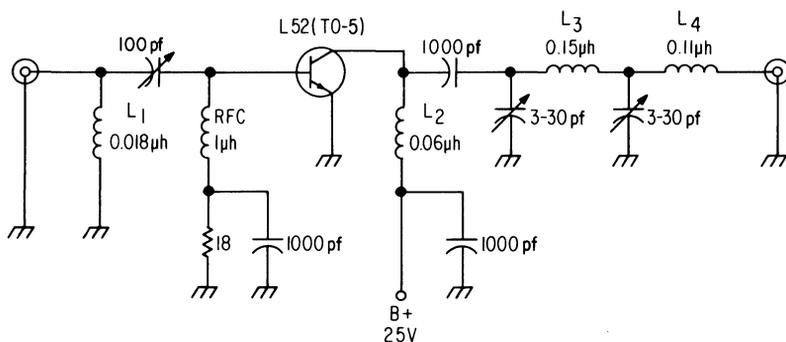
Power out = 10w  
 Power gain = 10 db  
 DC Power in = 600 ma at 25 v = 15 w

Fig. 55. 10-watt 50-mc transmitter.

The relatively high breakdown voltage of this device allows the amplifier to be amplitude modulated. The overall efficiency of the amplifier is approximately 65%.

**10-watt 50-mc Transmitter.** Two TI L-52's in parallel will produce 10 watts of output power with 10-db gain. Figure 55 is basically a common-emitter circuit with a  $\pi$ -L output matching network to match a 50-ohm antenna. Separate biasing resistors are used in the base circuits to balance the operating currents of the two transistors. The input circuit is designed to produce a 50-ohm input impedance. Overall efficiency of this circuit is approximately 65%.

**1-watt 170-mc Transmitter.** This circuit (Fig. 56) is a single common-emitter Class C amplifier utilizing TI's new L-52 to produce 1-watt output power



$P_o = 1$  watt power gain = 4 db average  
 $V_{cc} = 25$  v  
 $I_c = 125$  ma

- $L_1 = 1$  T No. 14 Buss, 0.5" diam
- $L_2 = 3$  T No. 14 Buss, 0.4" diam, 0.3" long
- $L_3 = 5$  T No. 14 Buss, 0.4" diam, 0.5" long
- $L_4 = 4$  T No. 14 Buss, 0.4" diam, 0.4" long

Fig. 56. 1-watt 170-mc transmitter.

at 170 mc. The output circuit is a  $\pi$ -L network designed to match the output of the transistor to a 50-ohm input impedance. The overall efficiency of this circuit is approximately 30%, with 1-watt output and 4-db power gain.

**162- to 180-mc Transmitter.** Figure 57 shows a narrowband transmitter capable of being tuned over a frequency range of 162 to 180 mc. The first stage acts as a buffer for an oscillator. Second and third stages provide frequency multiplication. The fourth stage isolates changes that might appear in the load, to prevent their being reflected across the tripler stage, which would cause frequency instability. The final stage is a Class C power amplifier; the two devices in parallel can deliver 300 mw to a 50-ohm load.

**223-mc Transmitter.** The 223-mc transmitter shown in Fig. 58 is satisfactory for many telemetry applications.

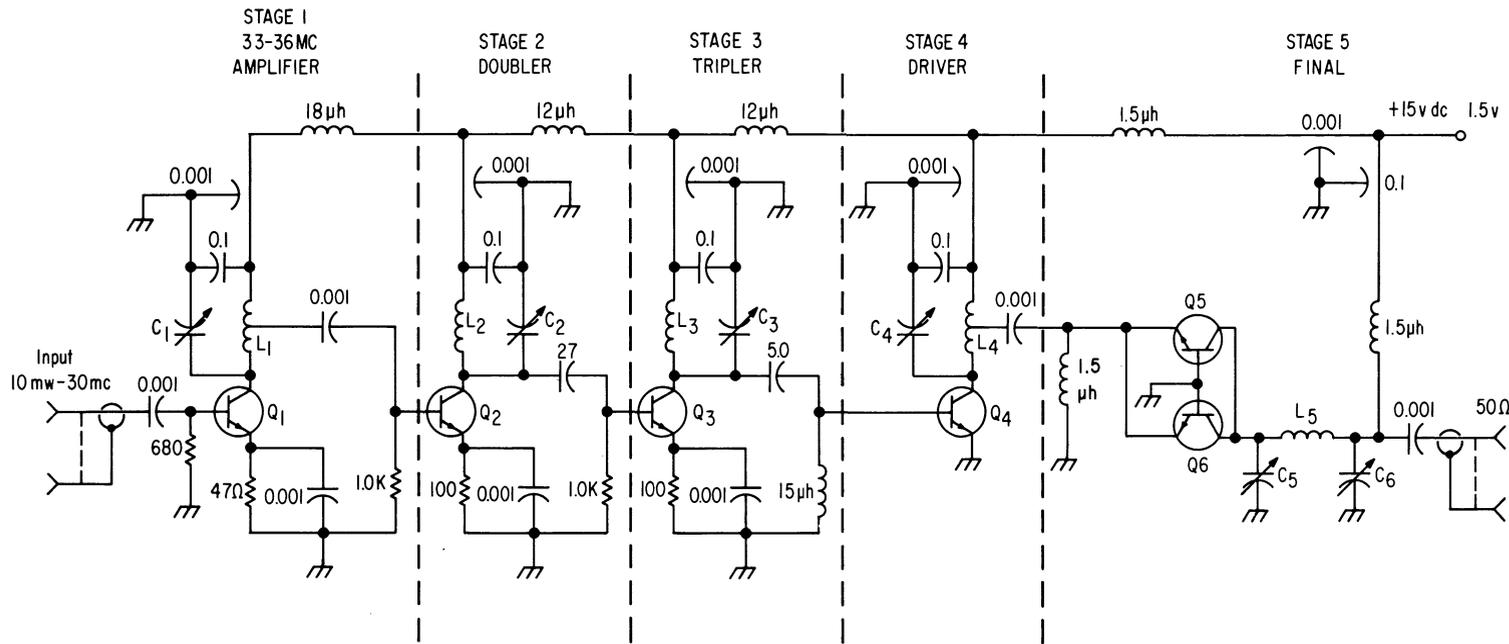
The crystal-controlled Colpitts-type oscillator employs a 2N743 transistor working in the common-base configuration. The oscillator delivers about 10 mw into a 50-ohm load.

The first doubler is a common-emitter amplifier with a pi-type circuit in the output tuned to the second harmonic and employing a trap network at the collector to eliminate the fundamental in the output. Power gain of this circuit is about 6 db and the power output to the second doubler is about 40 mw at 111.5 mc.

The second doubler is a common-base amplifier with a pi-filter in the output tuned to the second harmonic. The trap eliminates the 11.5-mc fundamental. Power output to the final is about 45 mw at 223 mc.

The final stage is a common-base Class C amplifier employing another pi-network in the 223-mc output. The final will deliver 80 to 100 mw to a 50-ohm load.

Fig. 57. 162- to 180-mc transmitter.



$C_1, C_2, C_6 = 8-60 \text{ pf}$   
 $C_3, C_4, C_5 = 1.5-20 \text{ pf}$   
 All other capacitor values in  $\mu\text{f}$

$L_1 = 8\text{T}, 1/4''$  Form with core, tap center  
 $L_2 = 6\text{T}, 1/4''$  Form  
 $L_3 = 2\text{T}, 1/4''$  Form

$L_4 = 2\text{T}, 1/4''$  Form, tap center  
 $L_5 = 3\text{T}, 1/4''$  Form  
 $Q_1$  Thru  $Q_6 = \text{SM2498}$

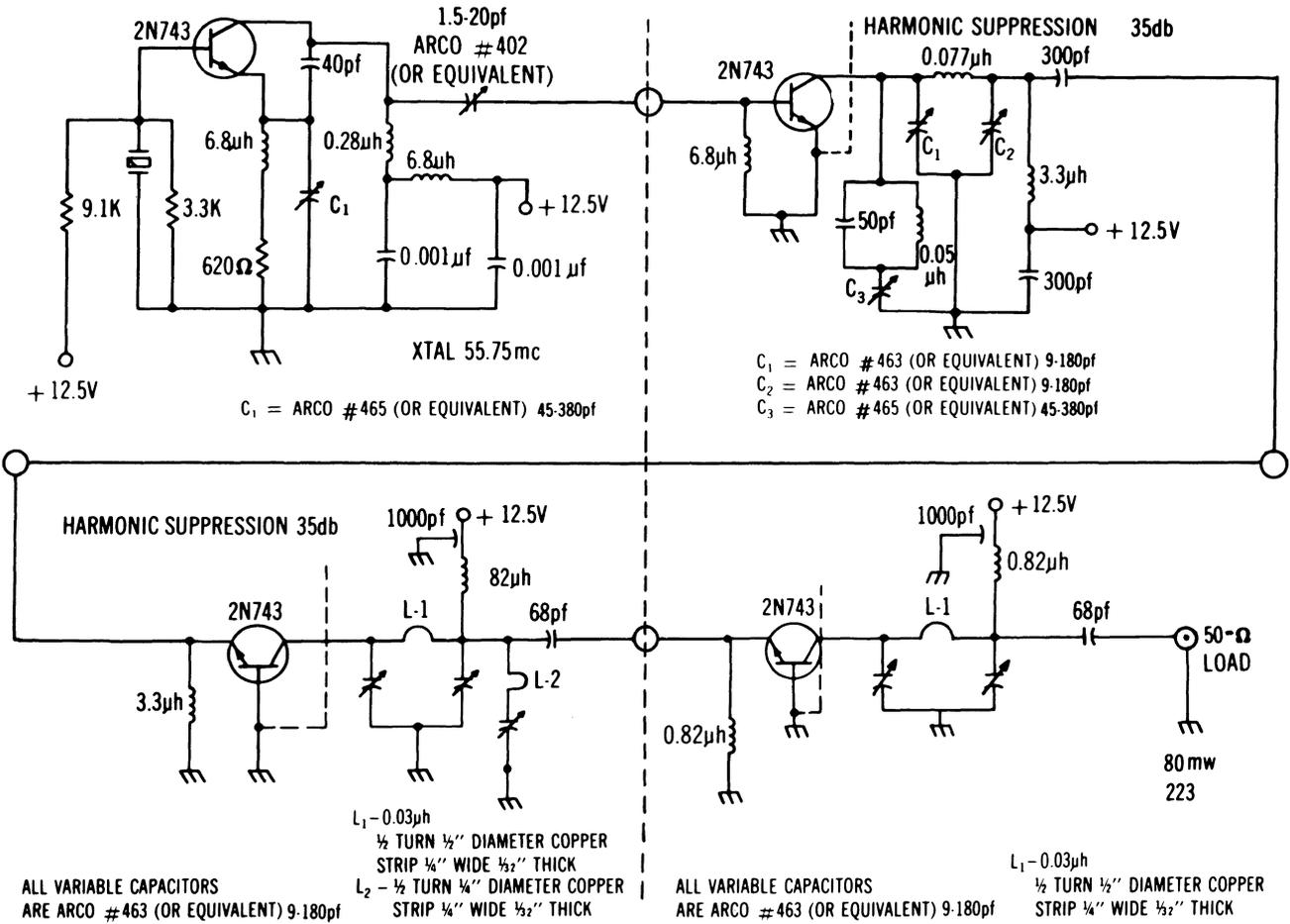


Fig. 58. 223-mc transmitter.

## Device Nomenclature and Standard Test Circuits

### GENERAL PRINCIPLES OF LETTER SYMBOL STANDARDIZATION

**Electrical Quantities and Electrical Parameters.** Electrical quantities deal primarily with voltage, current, and time quantities. Electrical parameters deal with the relationship between specific electrical quantities.

In studying the operation of a transistor, we assume it to be a black box with two input leads and two output leads. See Fig. 1.

In describing this black box, we write equations relating the input current, input voltage, output current, and output voltage. An example of this is the equation:

$$v_i = h_i i_i + h_r v_o$$

This equation states that the input voltage  $v_i$  equals the input current multiplied by a certain number  $h_i$  plus the output voltage  $v_o$  multiplied by a certain number  $h_r$ . The numbers  $h_i$  and  $h_r$  are parameters.

Although many electrical quantities ( $I_{co}$ , Zener voltage, etc.) are called parameters, they are not parameters in the true sense of the word.

**Electrical Quantities and Associated Subscripts.** The following is a list of accepted symbols for electrical quantities:

$$\begin{aligned} V &= \text{voltage (d-c volts)} \\ v &= \text{voltage (a-c volts)} \end{aligned}$$

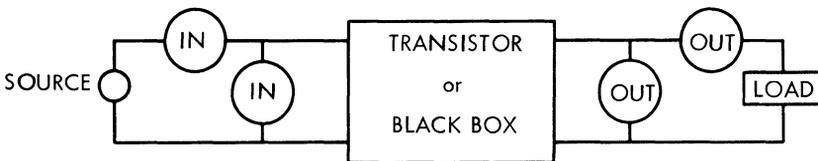


Figure 1

$I$  = current (d-c amperes)  
 $i$  = current (a-c amperes)  
 $R$  = resistance (ohms)  
 $Z$  = impedance (ohms)  
 $Y$  = admittance (mhos)  
 $P$  = power (watts)  
 $f$  = frequency (cycles per second)  
 $B$  = breakdown

The following subscripts are associated with these symbols for electrical quantities:

$E$  or  $e$  = emitter electrode  
 $B$  or  $b$  = base electrode  
 $C$  or  $c$  = collector electrode  
 $O$  or  $o$  = open electrode  
 $X$  or  $x$  = other electrode not opened

An upper-case subscript designates a d-c quantity while a lower-case subscript designates an a-c quantity.

Examples:

$I_B$  = d-c current in circuit  $B$   
 $i_b$  = a-c current in circuit  $B$

*First subscript:* designates the electrode at which current or voltage is measured with respect to the reference electrode.

*Second subscript:* designates the reference electrode. (If understood, this subscript may be omitted.)

*Third subscript:* designates circuit conditions at the instant the current or voltage is measured. (If the second subscript is omitted, this becomes the second subscript.)

Examples:

$I_{CBO}$  = collector-to-base d-c current with emitter circuit open.  
 $I_{CO}$  = collector-to-base d-c current with emitter circuit open.  
 $V_{BE}$  = d-c voltage between base and emitter.  
 $i_c$  = a-c collector current in the collector circuit.

**Electrical Parameters and Associated Subscripts.** The following is a list of the most commonly used subscripts. Formerly, double numbers were used instead of letter subscripts but these have fallen into disuse because they are not sufficiently informative. In all cases, the double number is considered as one subscript.

$22$  or  $O$  or  $o$  = output  
 $11$  or  $I$  or  $i$  = input  
 $21$  or  $F$  or  $f$  = forward transfer ratio  
 $12$  or  $R$  or  $r$  = reverse transfer ratio  
 $E$  or  $e$  = emitter electrode  
 $B$  or  $b$  = base electrode  
 $C$  or  $c$  = collector electrode  
 $O$  or  $o$  = open (depending on relative position)  
 $S$  or  $s$  = short

In most cases parameters have one, two, or three subscripts.

*First subscript:* designates input, output, or ratio function

*Second subscript:* designates circuit configuration

*Third subscript:* gives additional information

Examples:

$h_{22}$  or  $h_{ob}$  = output admittance with the input open (this is assumed) and using a common-base circuit.

$H_{OB}$  = output conductance (1/resistance) with the input open (this is assumed) and using a common-base circuit.

$h_{11}$  or  $h_{ib}$  = input impedance with the output shorted (this is assumed) and using a common-base circuit.

**Bias Voltage Symbols.** Bias voltages are supplied from a d-c source and are designated by repeating the electrode subscript. The reference electrode may be designated by the third subscript.

Examples:

$V_{EE}$  = d-c bias voltage applied to emitter circuit

$V_{CC}$  = d-c bias voltage applied to collector circuit

## DEFINITIONS AND TEST CIRCUITS

### Schematic Nomenclature.

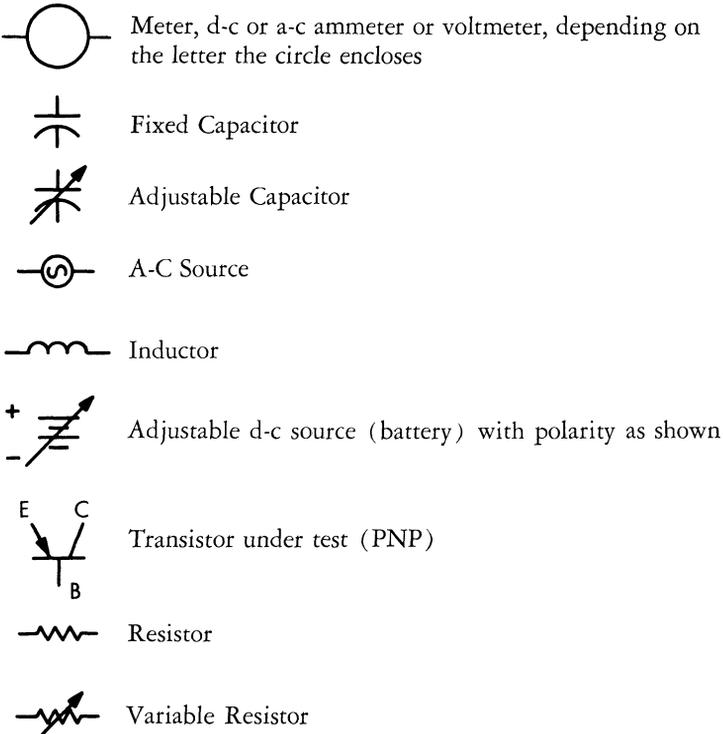


Figure 2

D-C Measurements and Test Circuits.

See Fig. 3:

$I_{CBO}$  = the current that flows when the collector-base junction is reverse biased to a specified d-c voltage with the emitter open-circuited.

$BV_{CBO}$  = breakdown voltage. A d-c voltage, applied in the reverse direction of the collector-base junction with the emitter open-circuited, which gives a specified reverse current.

See Fig. 4:

$I_{EBO}$  = the current that flows when the emitter-base junction is reverse biased to a specified d-c voltage with the collector open-circuited.

$BV_{EBO}$  = breakdown voltage. A d-c voltage, applied in the reverse direction of the emitter-base junction with the collector open-circuited, which gives a specified reverse current.

See Fig. 5:

$I_{CEO}$  = the current that flows when the collector-emitter junction is reverse biased to a specified d-c voltage with the base open-circuited.

$BV_{CEO}$  = breakdown voltage. A d-c voltage, applied in the reverse direction of the collector-emitter junction with the base open-circuited, which gives a specified reverse current.

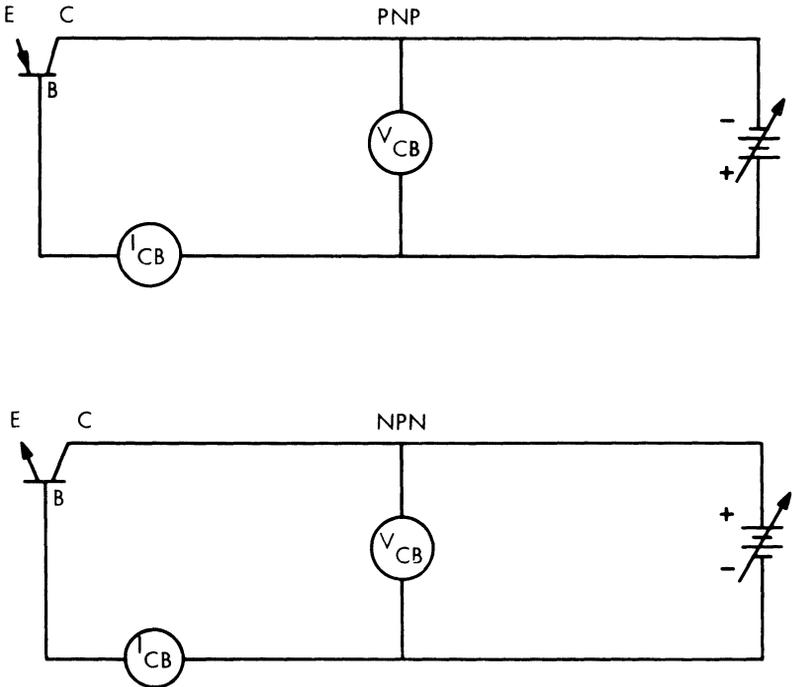


Figure 3

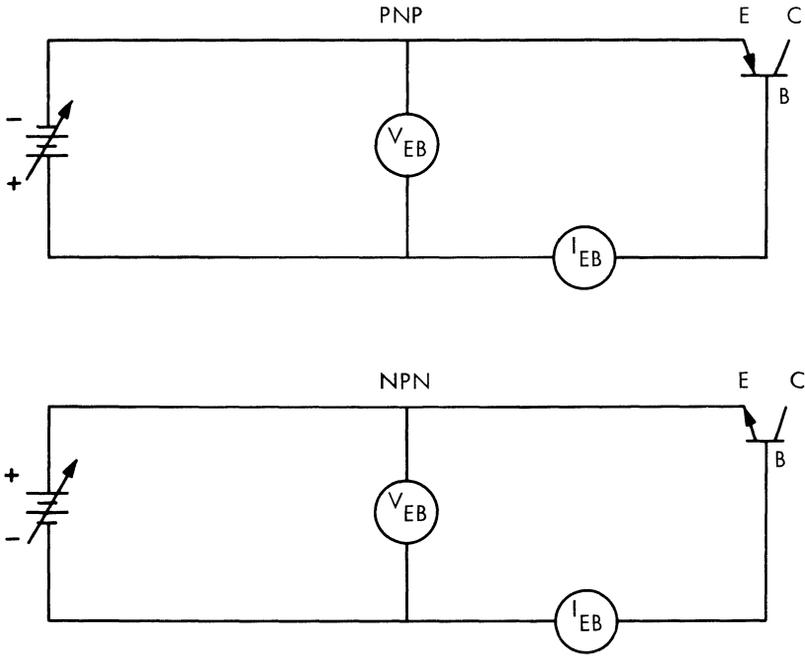


Figure 4

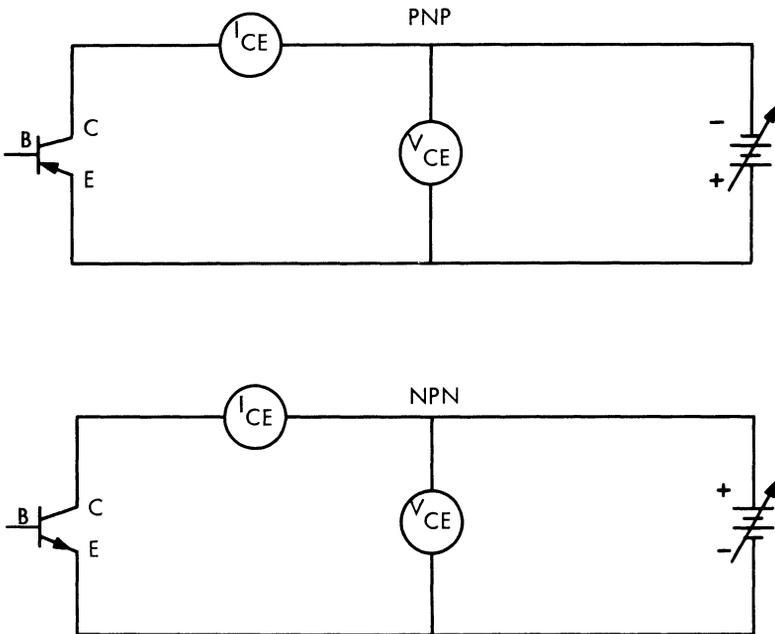


Figure 5

See Fig. 6:

$I_{CER}$  = the current that flows in the collector with a specified voltage applied to the collector, and a resistor connected from the base to emitter.

$BV_{CER}$  = the voltage measured between the collector and emitter with a specified current flowing in the collector, with a resistor connected from the base to emitter.

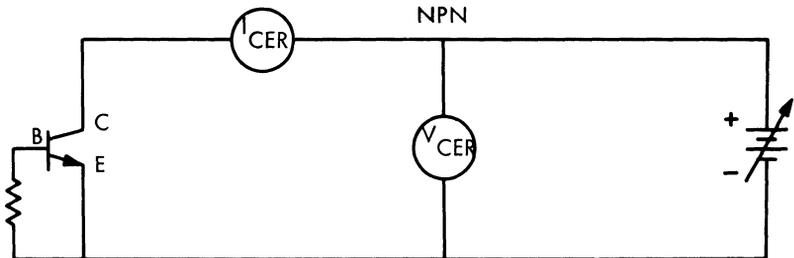
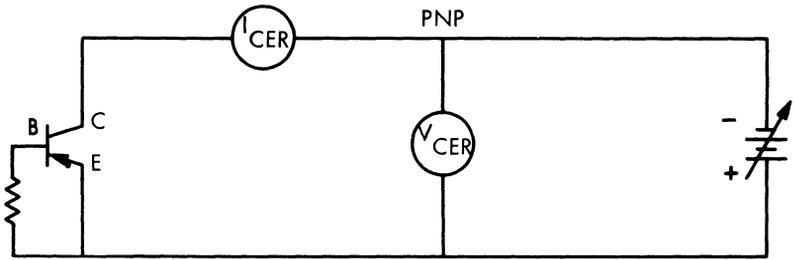
See Fig. 7:

$I_L$  = Leakage current between the can of a transistor and all electrodes (emitter, base, and collector) at a specified voltage. This is a measure of insulation resistance. This test is omitted if one of the transistor leads is connected to the can.

See Fig. 8:

$h_{FE}$  = d-c beta ( $\beta$ ). Current transfer ratio of a common-emitter transistor circuit.

$$h_{FE} = \frac{I_C}{I_B}$$



**Figure 6**

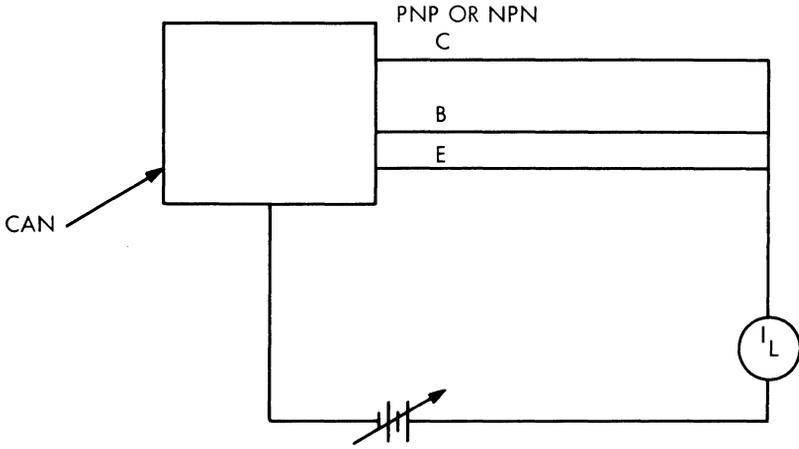


Figure 7

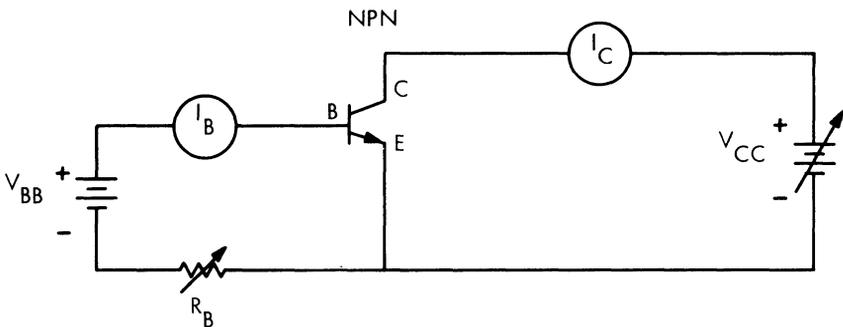
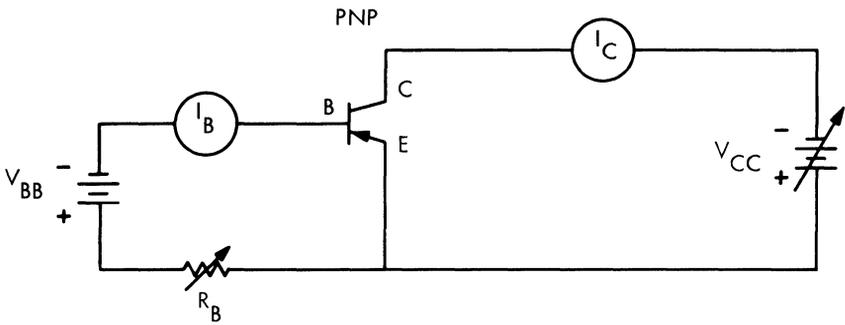


Figure 8

Operation:

1. With  $V_{CC}$  set at a specified value, adjust  $R_B$  until  $I_B$  or  $I_C$  reads a specified value, then read  $I_B$  and  $I_C$ .

See Fig. 9:

$R_{CS}$  = saturation resistance. Ratio of collector-to-emitter voltage  $V_{CE}$ , which at times is referred to as the saturation voltage  $V_{CS}$ , to the collector current  $I_C$  at a specified base current  $I_B$  in a common-emitter transistor circuit.

$$R_{CS} = \frac{V_{CE}}{I_C} = \frac{V_{CS}}{I_C}$$

Operation:

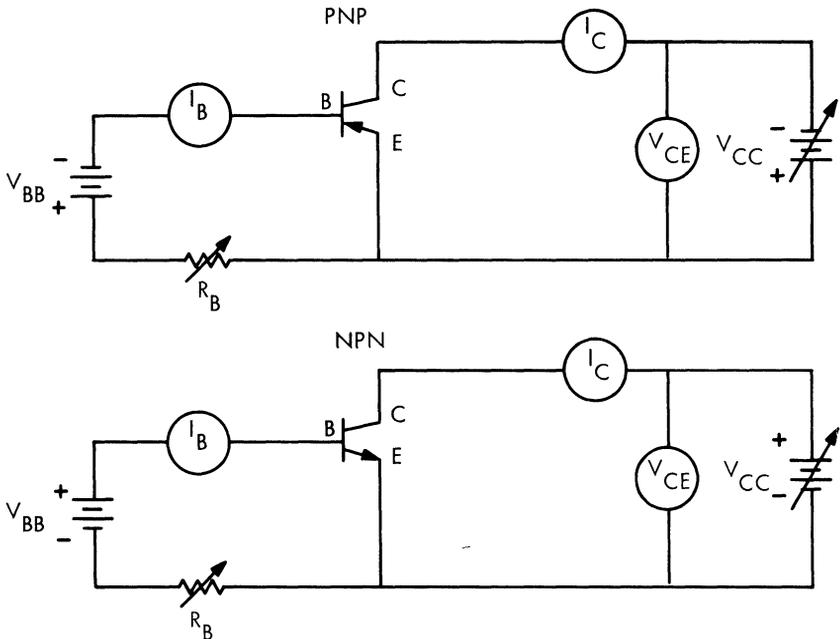
1. Set  $I_B$  at a specified value by varying  $R_B$ .
2. Vary  $V_{CC}$  until  $I_C$  reads a specified value and read  $V_{CE}$  which equals  $V_{CS}$ .
3. Or, vary  $V_{CC}$  until  $V_{CE}$  reads a specified value and read  $I_C$ .

*Pulse testing.* Any of the d-c parameters may be measured under pulse conditions. This method is particularly useful for power transistors, for it allows testing of the units without the necessity of heat sinking. TI uses a 2% or less duty cycle, which means that the power pulse to the transistor is applied for 2% (or less) of the time during a 16.7-millisecond period.

**A-C Measurements and Test Circuits.**

See Fig. 10:

$h_{fe}$  = a-c beta. Small-signal a-c current transfer ratio of a common-emitter transistor circuit with the collector and emitter short-circuited to a-c current.



**Figure 9**

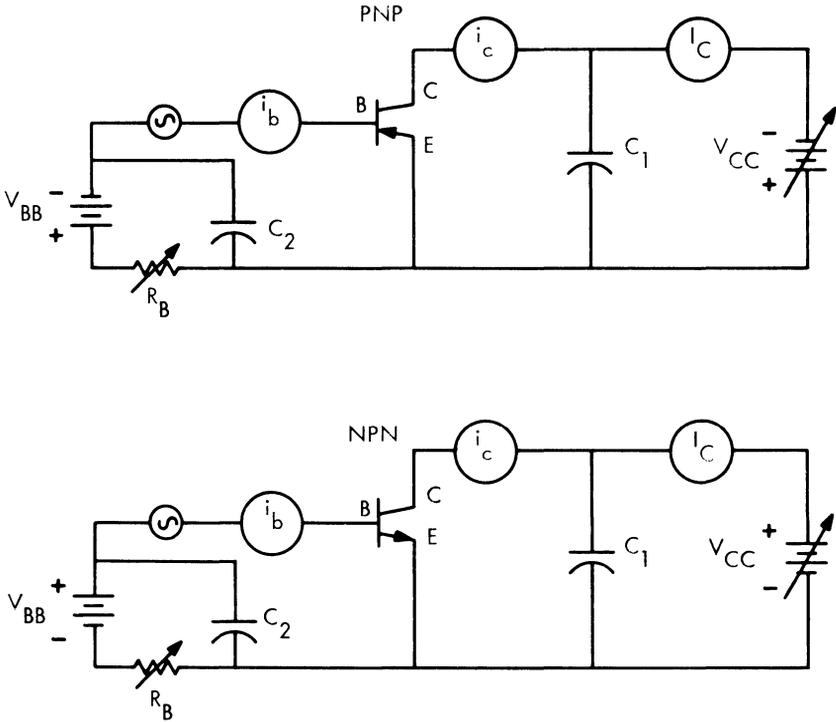


Figure 10

Operation:

1.  $C_1$  shorts a-c current between emitter and collector.
2.  $C_2$  allows a-c current to bypass bias battery  $V_{BB}$  and  $R_B$ .
3. With  $V_{CC}$  set a certain value,  $R_B$  is varied until  $I_C$  reaches a specified value.
4. Small a-c signal is applied and  $i_c$  and  $i_b$  are read.

$$5. h_{fe} = \frac{i_c}{i_b}$$

See Fig. 11:

$h_{oe}$  = small-signal a-c output admittance of a common-emitter transistor circuit with the base open-circuited to the a-c current.

Operation:

1. Capacitor  $C_1$  allows a-c current to bypass  $V_{CC}$ .
2. Resonant circuit  $R$  constitutes infinite resistance (open) to a-c current, but zero resistance to d-c current.
3. With  $V_{CC}$  set at a specified value,  $R_B$  is varied until either  $I_C$  or  $I_E$ , as required, reaches a specified value. This is called the bias condition.
4. Small a-c signal is applied and  $v_{ce}$  and  $i_c$  are read.

$$5. h_{oe} = \frac{i_c}{v_{ce}}$$

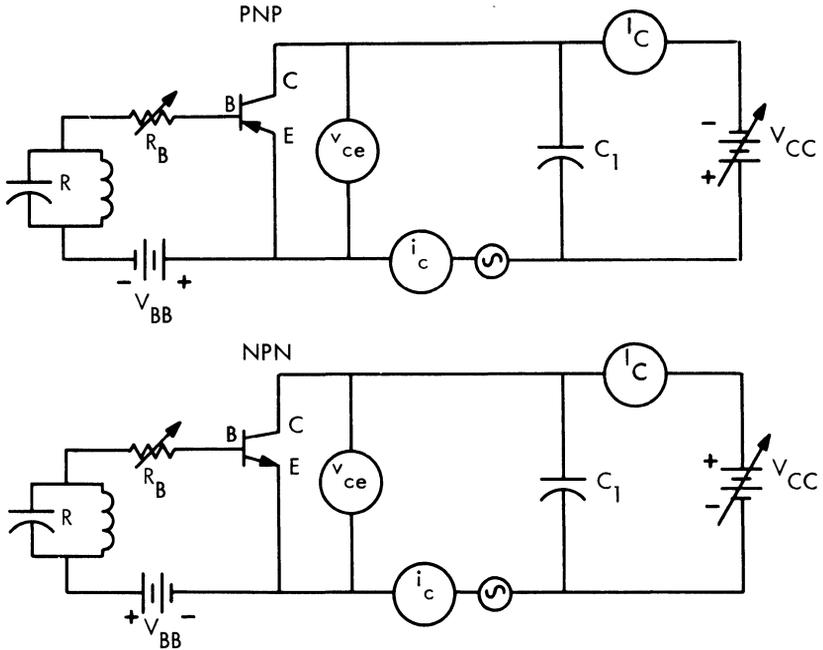


Figure 11

See Fig. 12:

$h_{re}$  = small-signal a-c reverse voltage ratio of common-emitter transistor circuit with the base open-circuited to the a-c current.

Operation:

1. Capacitor  $C_1$  allows a-c current to bypass  $V_{CC}$ .
2. Resonant circuit  $R$  constitutes infinite resistance (open) to a-c current, but zero resistance to d-c current.
3. With  $V_{CC}$  set at a specified value,  $R_B$  is varied until either  $I_C$  or  $I_E$ , as required, reaches a specified value. This is called the bias condition.
4. Small a-c signal is applied and  $v_{ce}$  and  $v_{be}$  are read.

$$5. h_{re} = \frac{v_{be}}{v_{ce}}$$

See Fig. 13:

$h_{ie}$  = small-signal a-c input impedance of a common-emitter transistor circuit with the collector short-circuited to the a-c current.

Operation:

1. Capacitor  $C_1$  shorts the a-c current in the collector circuit.
2. Capacitor  $C_2$  allows the a-c signal to bypass the base d-c bias.
3. With  $V_{CC}$  set at a specified value,  $R_B$  is varied until either  $I_C$  or  $I_E$ , as required, reaches a specified value. This is called the bias condition.
4. Small a-c signal is applied and  $i_e$  and  $v_{be}$  are read.

$$5. h_{ie} = \frac{v_{be}}{i_b}$$

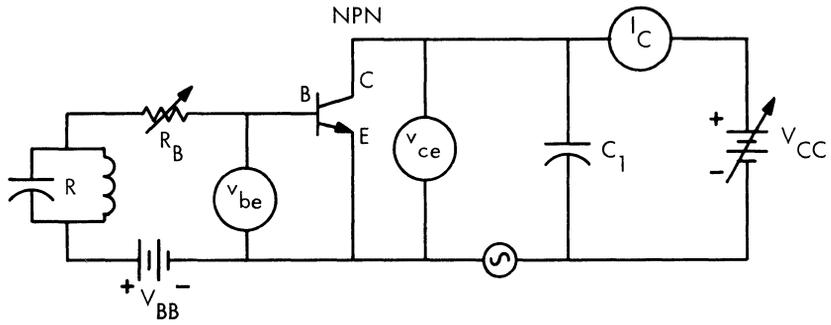
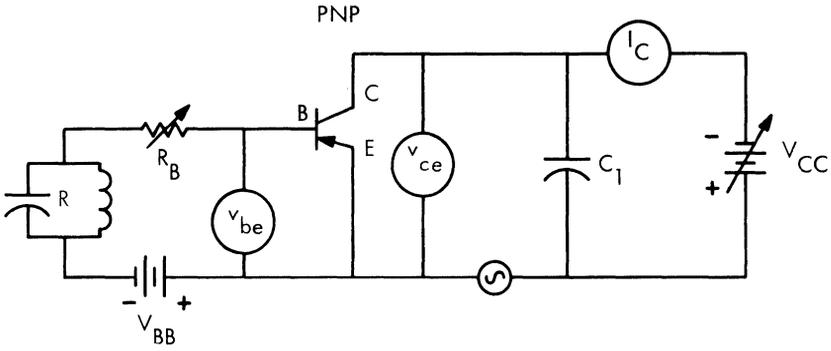


Figure 12

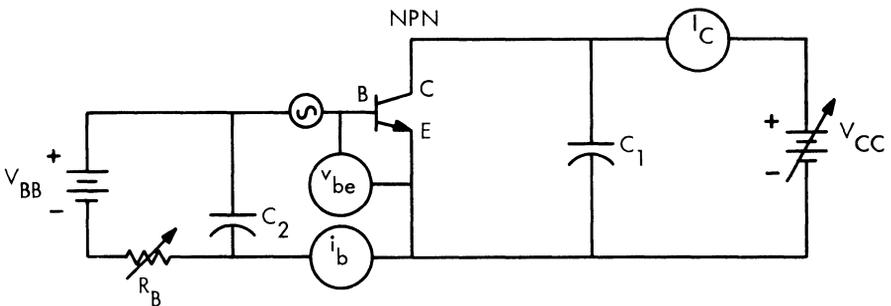
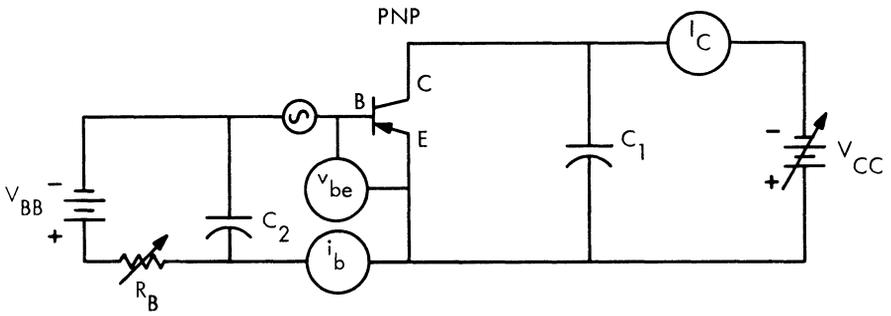


Figure 13

See Fig. 14:

$h_{ob}(h_{22})$  = small-signal a-c output admittance of a common-base transistor circuit with the emitter circuit open-circuited to the a-c current.

Operation:

1. Capacitor  $C_1$  allows a-c current to bypass bias battery  $V_{CC}$ .
2. Resonant circuit  $R$  constitutes infinite resistance, but zero resistance to d-c current.
3. With  $V_{CC}$  set at a specified value,  $R_E$  is varied until  $I_E$  reaches a specified value. This is called the bias condition.
4. Small a-c signal is applied and  $v_{eb}$  and  $i_c$  are read.

5.  $h_{ob} = \frac{i_c}{v_{eb}}$

See Fig. 15:

$h_{ib}(h_{11})$  = small-signal a-c input impedance of a common-base transistor circuit with the collector circuit short-circuited to the a-c current.

Operation:

1. Capacitor  $C_1$  shorts the a-c current in the collector circuit.
2. Capacitor  $C_2$  allows a-c current to bypass bias battery  $V_{EE}$ .
3. With  $V_{CC}$  set at a specified value,  $R_E$  is varied until  $I_E$  reaches a specified value. This is called the bias condition.
4. Small a-c signal is applied and  $i_e$  and  $v_{eb}$  are read.

5.  $h_{ib} = \frac{v_{eb}}{i_e}$

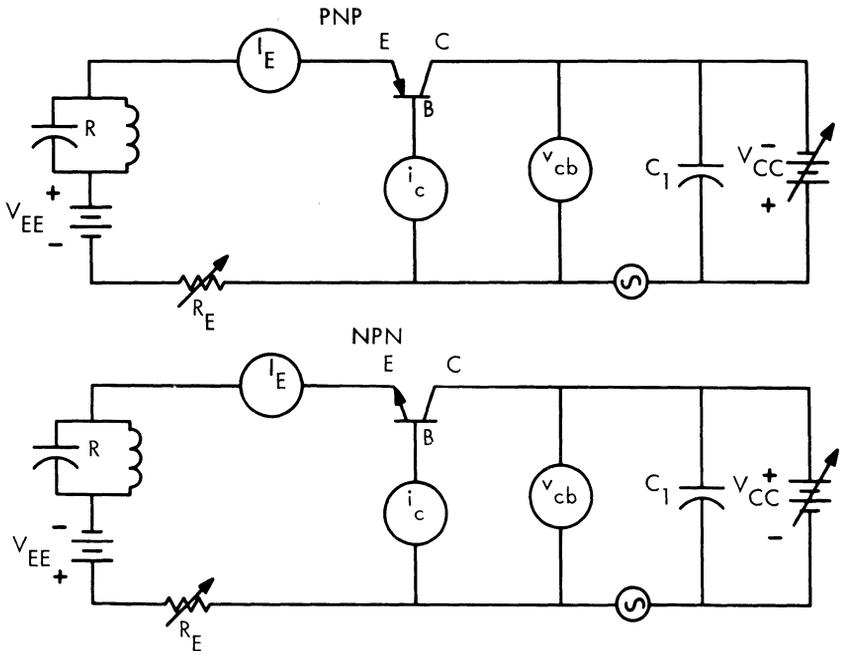


Figure 14

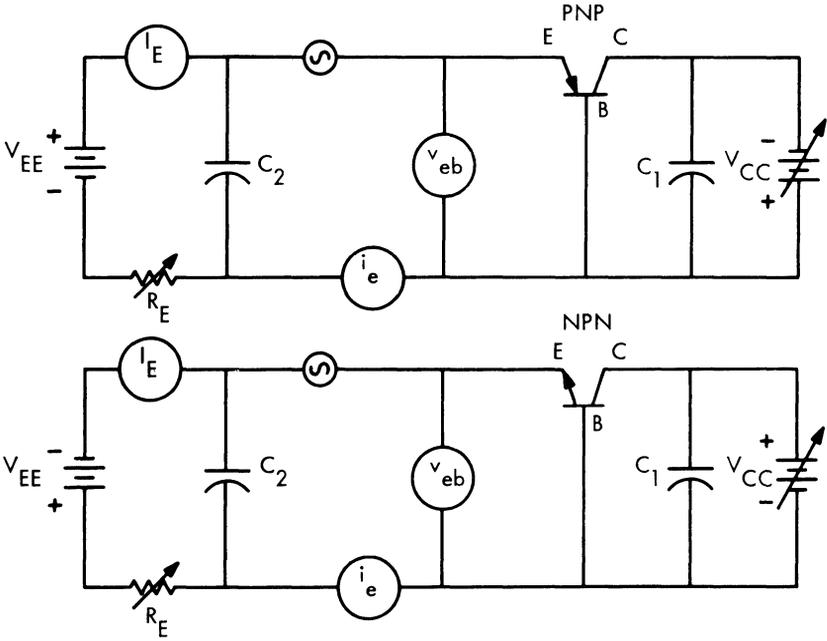


Figure 15

See Fig. 16:

$h_{fb}(h_{21})$  = small-signal a-c current transfer ratio of a common-base transistor circuit with the collector short-circuited to the a-c current.

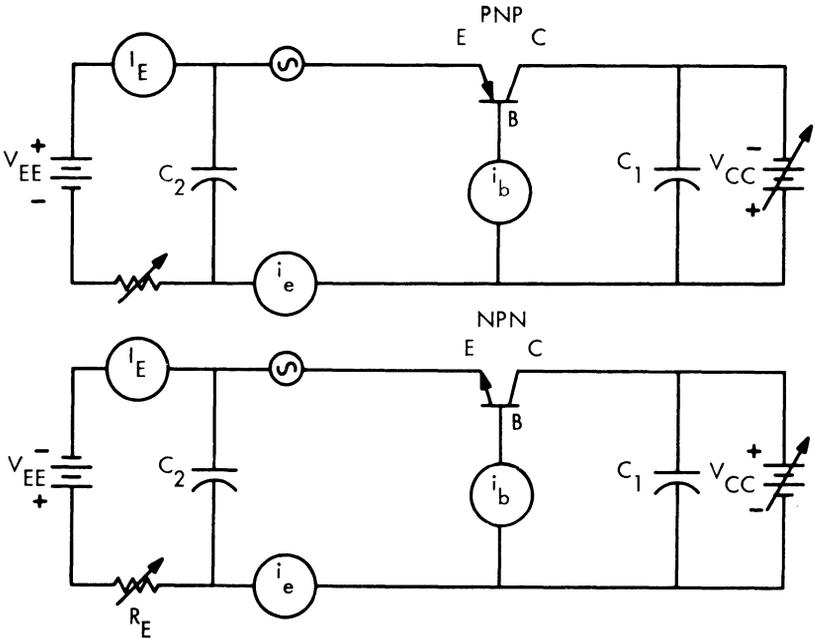


Figure 16

$$h_{rb} = \frac{i_c}{i_e} = -\alpha \text{ (Sometimes referred to as a-c alpha)}$$

For greater readability accuracy,  $1 + h_{rb}$  is measured at TI:

$$1 + h_{rb} = \frac{i_b}{i_e}$$

Operation:

1. Capacitor  $C_1$  shorts a-c current in the collector circuit.
2. Capacitor  $C_2$  allows a-c current to bypass bias battery  $V_{EE}$  and  $R_E$ .
3. With  $V_{CC}$  set at a certain value,  $R_E$  is varied until  $I_E$  reaches a specified value.
4. Small a-c signal is applied and  $i_e$  and  $i_b$  are read.

See Fig. 17:

$h_{rb}$  = small-signal a-c reverse voltage ratio of a common-base transistor circuit with the emitter open-circuited to the a-c current.

Operation:

1.  $C_1$  allows a-c current to bypass  $V_{CC}$ .
2. Resonant circuit  $R$  constitutes infinite resistance (open) to a-c current, but zero resistance to d-c current.
3. With  $V_{CC}$  set to a specified value,  $R_E$  is adjusted until  $I_E$  reaches a specified value.
4. Small a-c signal is applied and  $v_{cb}$  and  $v_{be}$  are read.
5.  $h_{rb} = \frac{v_{be}}{v_{cb}}$

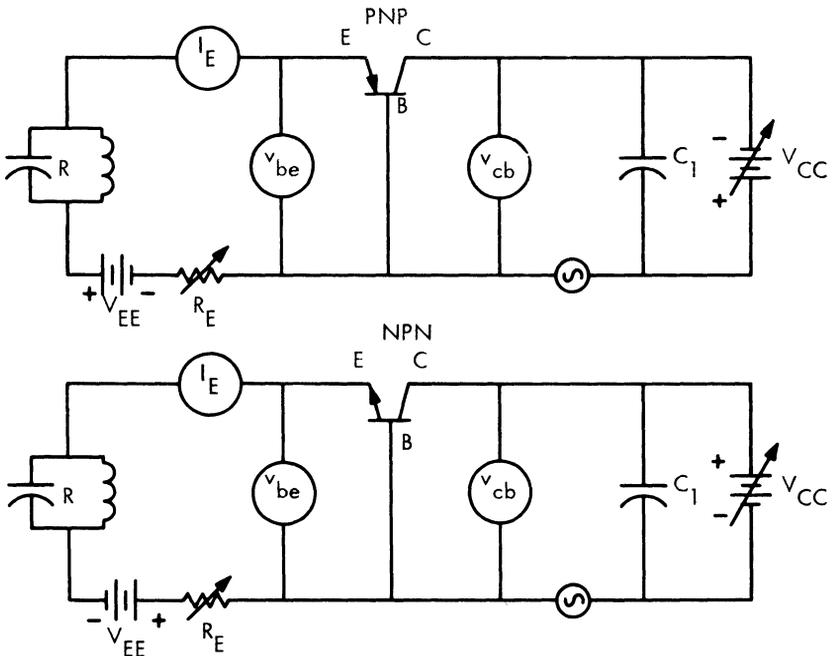


Figure 17

See Fig. 18:

$C_{ob}(C_o)$  = capacitance measured from the collector-to-base in a common-base transistor circuit with the emitter open-circuited to a-c current.

Operation:

1.  $C_1$  allows a-c current to bypass bias battery  $V_{CC}$ .
2. Resonant circuit R presents open circuit to a-c current.
3. With  $V_{CC}$  set at certain value adjust  $R_E$  until  $I_E$  reads a specified value.
4.  $C_X$  is a calibrated adjustable capacitor. With the transistor removed, adjust  $C_X$  until a null on V is reached, then place transistor in test and again null V. The difference between the two  $C_X$  readings is  $C_{ob}$ .

$P_g$  = a-c power gain. Ratio of output voltage multiplied by output current to input voltage multiplied by input current. Sometimes referred to as  $A_p$ .

$$P_g = A_p = \frac{i_o v_o}{i_i v_i}$$

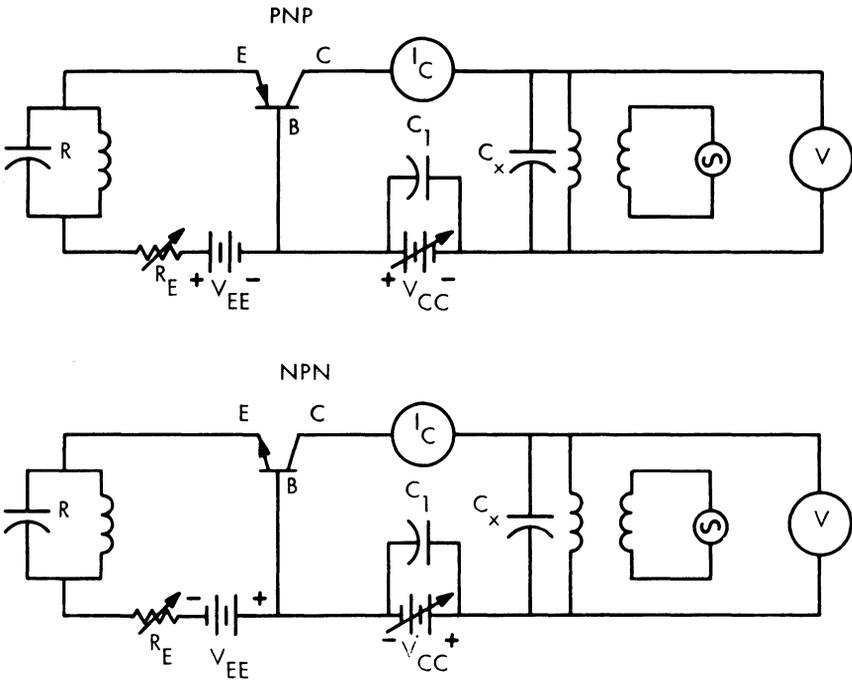
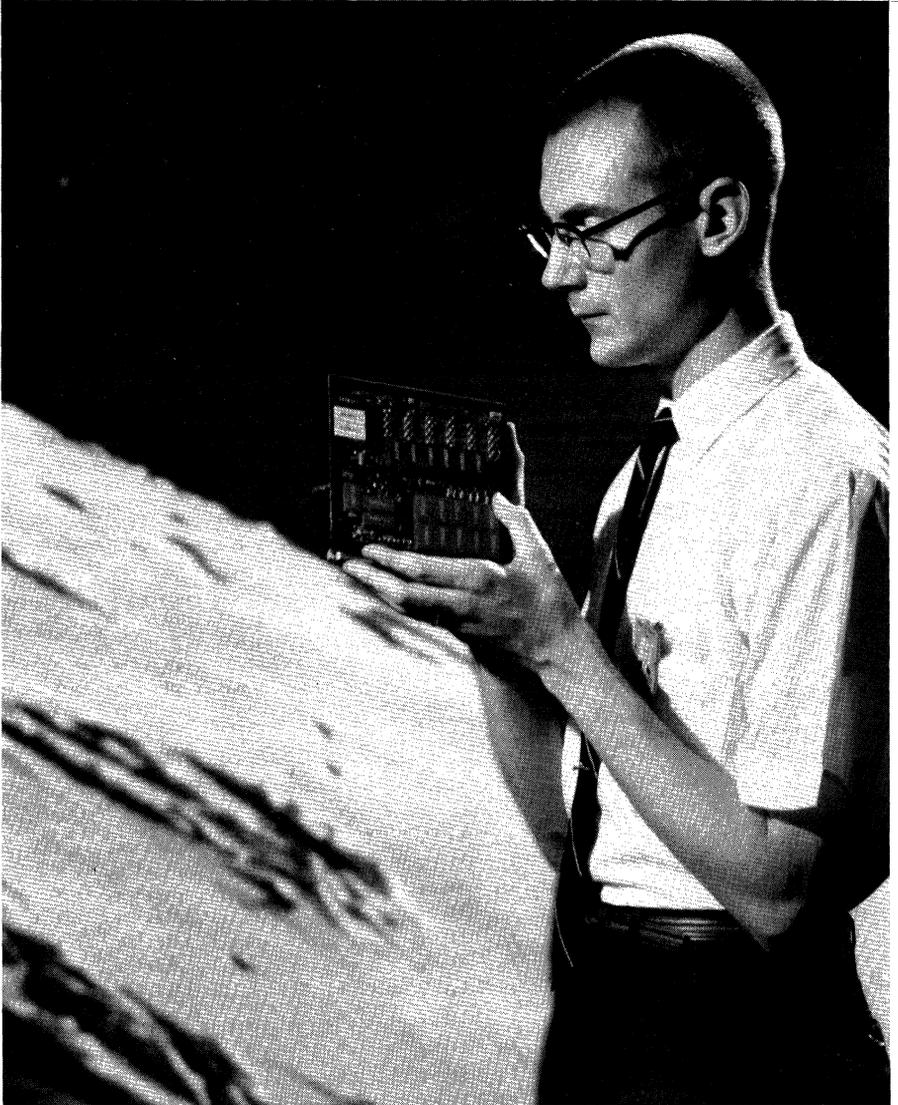


Figure 18



**TI's Apparatus division designed and built this detector and decoder, using TI components, for the Ranger VII spacecraft. Ranger VII obtained the most detailed photographs ever made of the lunar surface.**

## Noise Figure Measurement

by Harry F. Cooke

### 200-MC NF MEASUREMENT

Texas Instruments now includes 100% testing of 200-mc noise figure on several of its high-frequency transistors. The method of testing is semi-automatic and is based on the Hewlett-Packard 342A Noise Figure Meter. A block diagram of the test layout is shown in Fig. 1.

**Description of Test Set-up.** The noise source is a Hewlett-Packard type 343A temperature-limited diode which has a useful range of 10 to 600 mc. It is powered by the Hewlett-Packard 342A Noise Figure Meter and run at a constant current of 3.31 ma.

The test jig is a common-base amplifier with input and output tunable. Common-base operation is used since it avoids the problem of neutralization, which is sometimes necessary in the common-emitter connection operation to achieve sufficient

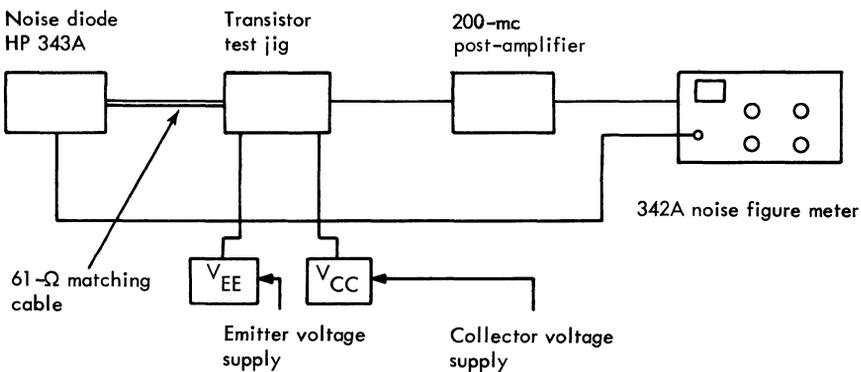


Fig. 1. Noise figure test set-up.

gain. The noise figure of common-emitter and common-base transistor amplifiers is essentially the same. The test jig circuit is shown in Fig. 2.

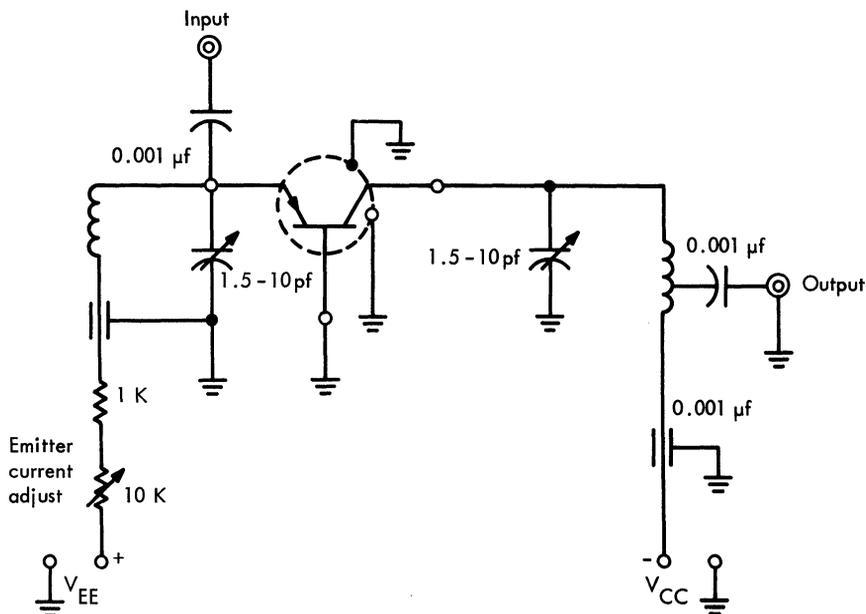
The post-amplifier is a three-stage transistor amplifier with a power gain of 40 db and a noise figure of 3.0 db. It uses three type 2N2415 germanium mesa transistors in a cascaded common-base connection. The circuit is shown in Fig. 3.

The Hewlett-Packard 342A Noise Figure Meter is the heart of the automatic noise figure measurement. It operates by pulsing the noise diode on and off while comparing the noise outputs of the amplifier with the diode on and off. It is self-contained and self-calibrating.

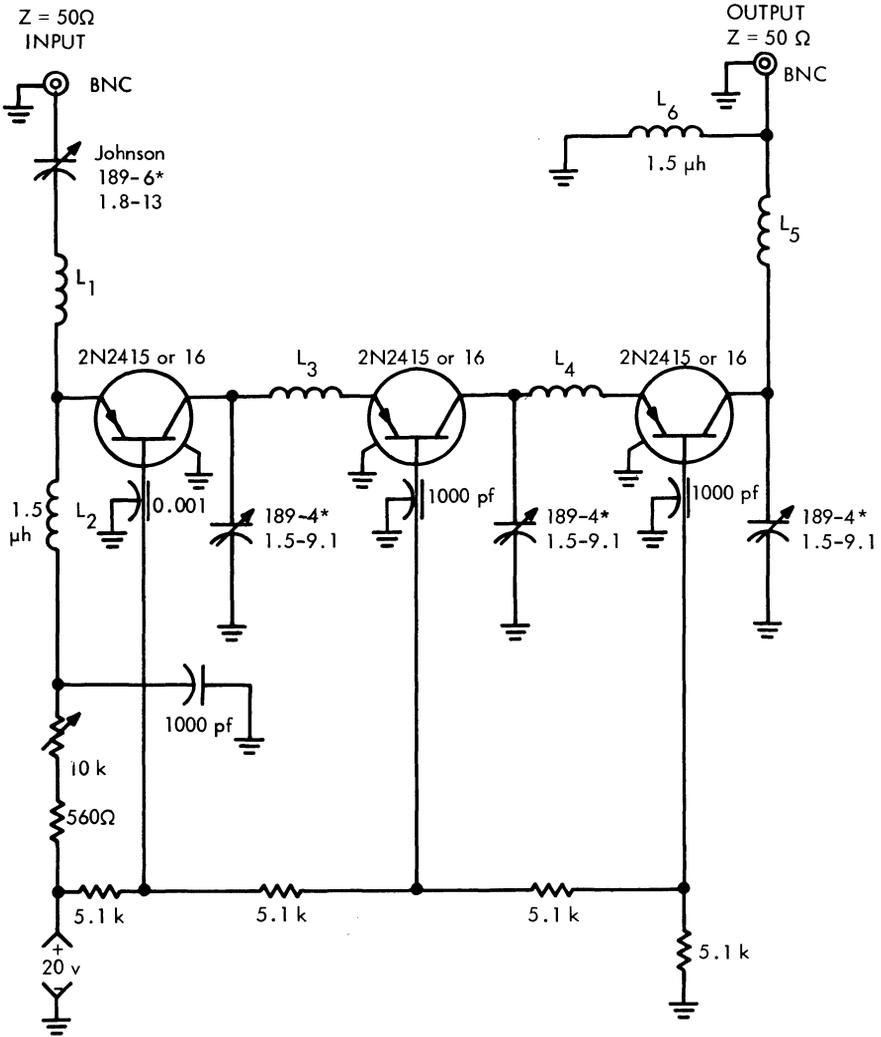
A majority of TI's customers are most interested in a noise test using a 75-ohm source resistance. The 343A noise diode has a 50-ohm output and thus it is necessary to transform the 50-ohm diode to 75 ohms with minimum losses. This is done by using a 200-mc quarter-wavelength 61-ohm cable. This cable is made by removing the #20 center conductor from a 7.5" length of RG-58/U and substituting a #21 center conductor. The ends of the cable are fitted with standard UG-88/U BNC connectors.

**Test Procedure.** After making the set-up shown in Fig. 1:

1. Turn on supply voltages and the post-amplifier
2. Adjust the 342A according to the manufacturer's instructions
3. Insert transistor into the test jig and set the emitter current to the correct value
4. Adjust input and output jig tuning for best noise figure. The input adjustment is usually adjusted only once for a given transistor type



**Fig. 2. 200-mc test jig.**



\* or equivalent

$L_1 = 3T \text{ \#18 bus } 1/2 \text{ diam}$

$L_2, L_6 = \text{Delavan } 1537-16 \text{ or Equiv.}$

$L_{3,4} = 3T \text{ \#18 bus, } 3/8 \text{ diam}$

$L_5 = 2T \text{ \#18 bus, } 3/8 \text{ diam}$

Gain = 40 db

Bandwidth = 25 Mc

Noise figure = 3 db

Note: Transistors on 3/4-inch centers

Fig. 3. 200-mc amplifier.

**1-GC NF MEASUREMENT**

**Description of Test Set-up.** In Fig. 4, the test layout is given in block form. The Hewlett-Packard 349A coaxial gas-tube noise source can be used to approximately 4 Gc. It has an excess noise of  $15.7 \pm 0.5$  db, according to the manufacturer's specification. The HP 342A is an automatic noise figure indicator and provides the necessary power for the 349A. Noise figure is read directly in db with this system.

A 10-db attenuator is used between the noise source and the test jig to reduce the excess noise to 5.7 db. This gives a more accurate measurement of noise figures below 10 db.

The test jig is designed for TO-5 or TO-18 devices. It is essentially a four-port coaxially tuned common-base amplifier. By crossing the emitter and base leads, it can be used as a common-emitter amplifier, provided the biasing network is suitably modified. The common-base and common-emitter noise figures are the same if the transistor is operated at the same gain level. Figure 5 shows the construction details of the test jig.

Figure 6 shows in detail the elements of the tuning network which are part of the test jig. The tunable shorted lines  $L_1$ ,  $L_2$ , and  $L_3$  are used as follows:

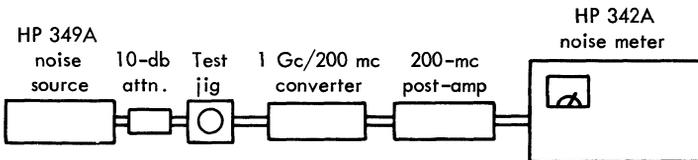
$L_1$  tunes the source *susceptance only*. The source resistance is 50 ohms fixed, unless otherwise specified.  $L_2$  tunes the collector circuit.  $L_3$ , in conjunction with  $L_2$ , comprises a double-stub tuner to tune and match the transistor output circuit to the converter.

A 200-mc post-amplifier with 40-db gain and a 3.0-db noise figure is used. The post-amplifier shown earlier in Fig. 3 is suitable.

The 1-Gc signal is converted down to 200 mc in the converter as shown in Fig. 4. The converter oscillator is operated at 1.2 Gc. Image response, which is thus at 1.4 Gc, is 30 db below the 1-Gc response. The converter has a 5.0-db noise figure and 10-db gain. A schematic of the converter is given in Fig. 7.

**Test Procedure.** To make a noise-figure measurement:

1. Insert transistor into the jig
2. Adjust bias according to manufacturer's specification
3. Adjust  $L_1$ ,  $L_2$ , and  $L_3$  for minimum noise figure. Once an appropriate setting has been made,  $L_2$  usually will not require further adjustment for other transistors of a given type



**Figure 4**

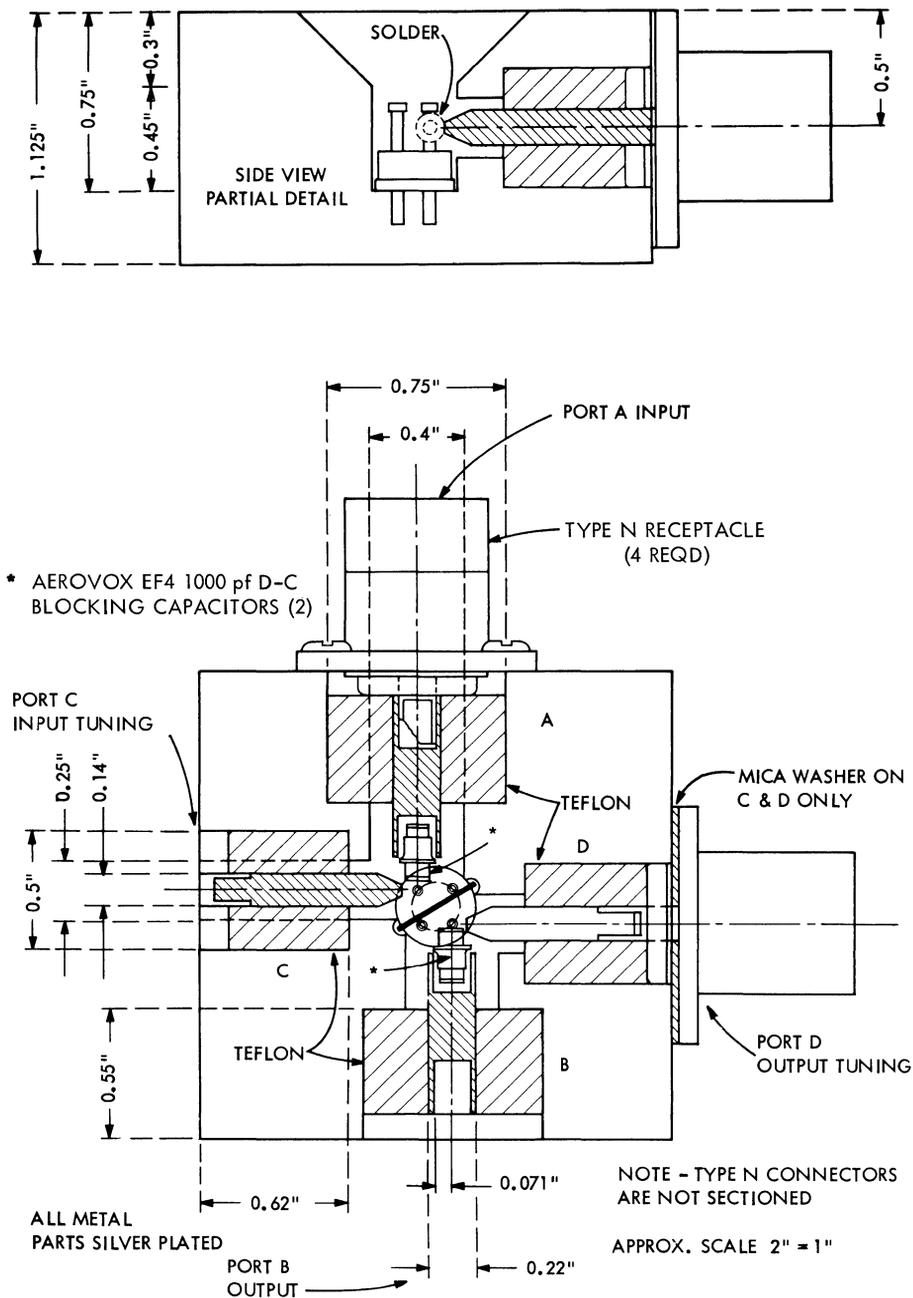


Fig. 5. TO-18, TO-5 common-base UHF amplifier module.

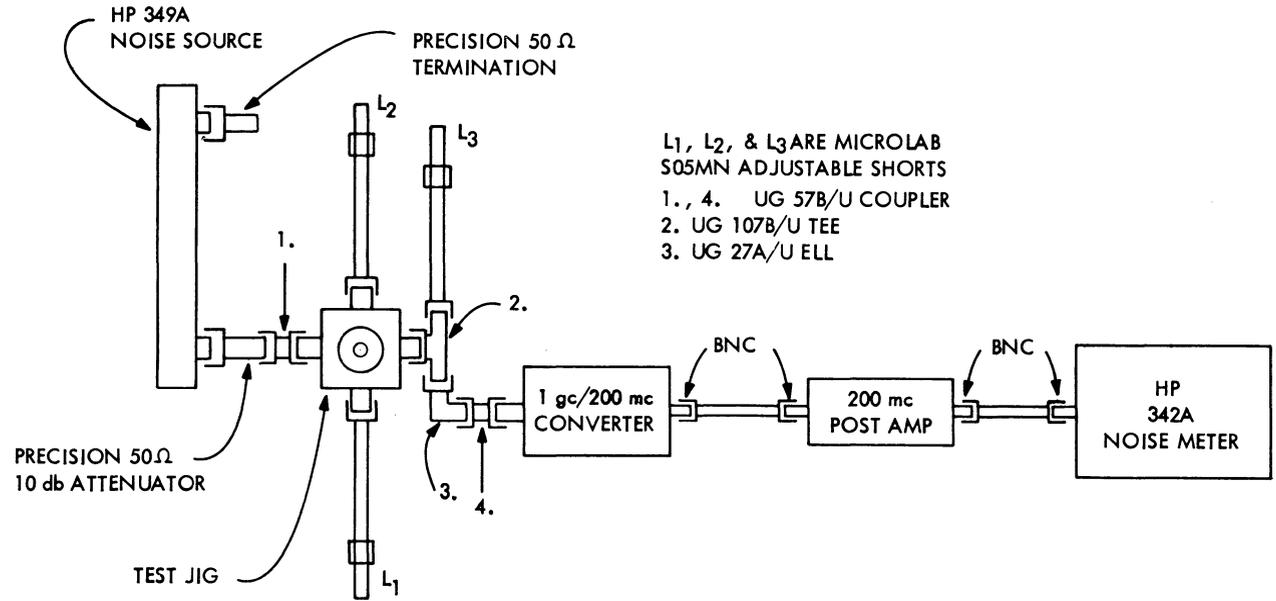


Fig. 6. 1-Gc noise figure test layout.

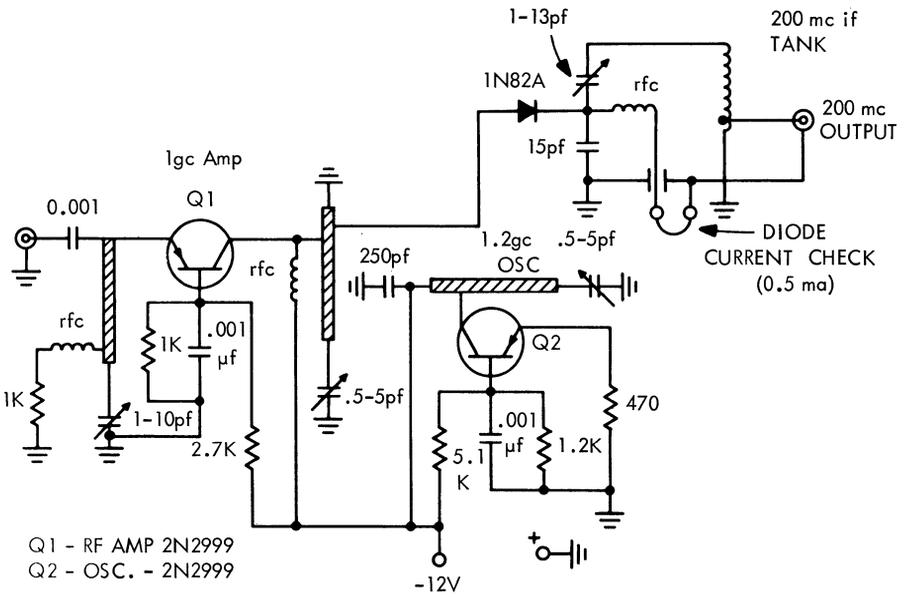
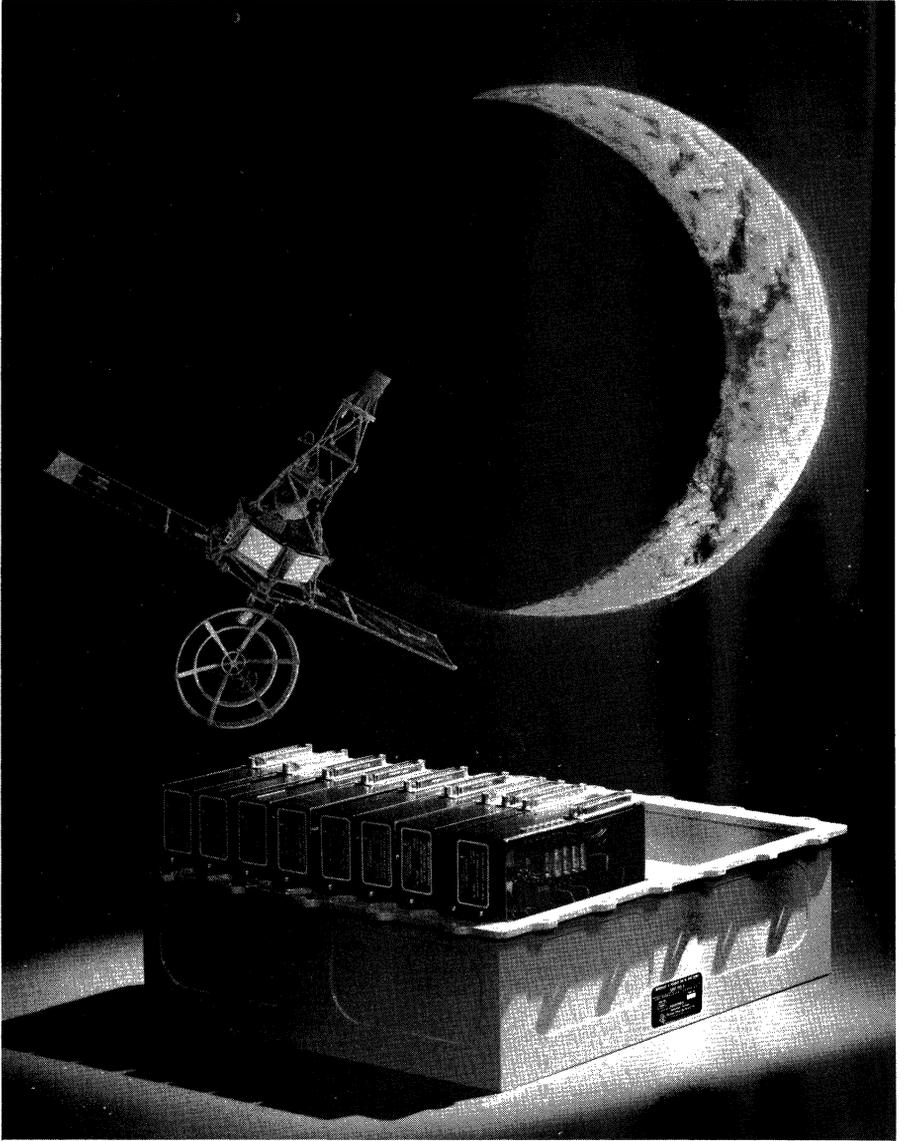


Fig. 7. 1-Gc 200-mc converter.



**Mariner Flight Data Encoder, designed and built by TI Apparatus division for the Mariner spacecraft.**

# Power Oscillator Test Procedure

by Harry F. Cooke

## 1-GC POWER OSCILLATOR TEST

**Fixture Description.** Some devices are functionally tested for output power as self-excited oscillators at 1 Gc. The test fixture is a common-base tuned-collector tuned-emitter oscillator. Feedback is provided by the internal capacitance of the transistor itself and the incidental capacitance of the transistor socket. Figure 1 shows the test fixture. Since the length of the collector cavity is fixed, frequency is adjusted with the capacitive probe as shown. Collector loading is varied by the coaxial capacitive probe. Bias for the collector is brought in through the center conductor of the collector cavity by way of a 1000-pf feedthrough capacitor. Emit-

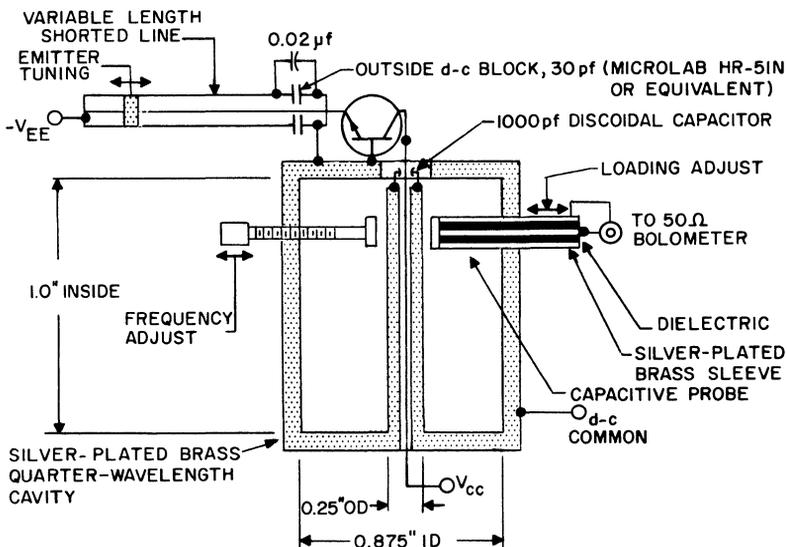


Fig. 1. 1-Gc oscillator power output test circuit.

ter bias is connected to the transistor via the emitter line through an outside d-c block (See Fig. 1).

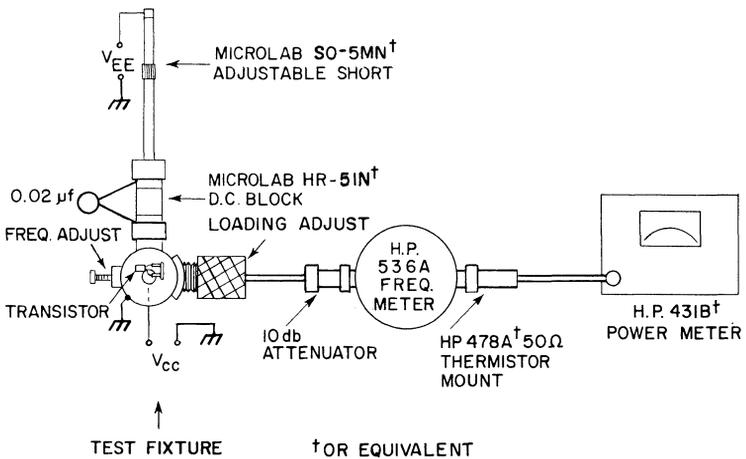
**Test Procedure.** Figure 2 is the test layout. An outside d-c block and adjustable short are connected to the emitter via the type-N receptacle. Emitter bias is applied between the lead coming out through the bottom of the cavity, and ground. The output line is connected to the 10-db attenuator as shown. When the set-up is completed as in Fig. 2, the transistor is plugged into the socket from the *open* end (refer to Fig. 2) and the biases are set according to specifications. To tune the oscillator, use the following procedure:

1. Maximize output by adjusting the emitter line
2. Maximize output by adjusting the output probe
3. Maximize output by retuning the emitter line
4. Check frequency for 1.0 Gc
5. (a) Turn frequency adjust probe *in* (clockwise) to lower frequency, or  
(b) Turn frequency adjust probe *out* (counter clockwise) to raise frequency
6. Repeat steps 1 through 4

It may be necessary during the tuning procedure to reset the emitter bias since this is affected by strong oscillations. The correct power output is that obtained at 1 Gc with rated collector voltage and current.

**1- TO 4-GC POWER OSCILLATOR TEST**

**Fixture Description.** Figure 3 is a detailed drawing of the test fixture itself. It is basically a two-cavity oscillator with the internal capacitance of the transistor itself providing the necessary feedback. The tunable cavity between the base and emitter presents the proper susceptance to the emitter to give oscillation. In the collector-base circuit a double-stub tuner is used both as the collector tuning element and as an output matching device. To bias the transistor, the outside conductors of the emitter and collector lines are isolated from the V-shaped center piece by 0.001" Mylar\* film.



**Fig. 2. 1-Gc oscillator power output test layout.**

\*Trademark of DuPont Corporation.

**Test Procedure.** After the test layout has been completed as shown in Fig. 4, the transistor is inserted into the test fixture so that the collector connects to the double-stub tuner. The biases are then adjusted to the specified values.

Next, adjust the tuning stub nearest the transistor to about midway in its travel. The remaining stub and the emitter line are both adjusted for maximum power output as indicated on the power meter. It may be necessary to repeat the adjustment of these two elements several times to get the maximum power. At this point, the frequency should be checked with the frequency meter. If the frequency is low, shorten the stub nearer the transistor and then readjust the other stub and emitter line. If the frequency is high, lengthen the stub nearer the transistor. Once the correct frequency has been obtained, only minor adjustments will be necessary for other transistors of the same type. The correct power output is that which is obtained at the desired test frequency.

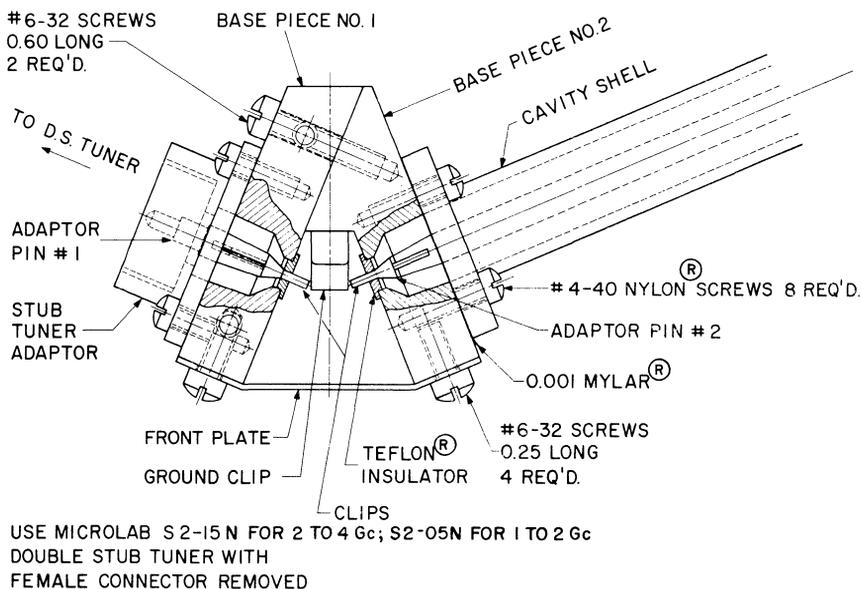


Fig. 3. Top view, 2-Gc cavity.

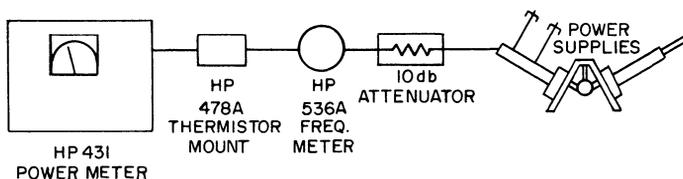


Figure 4

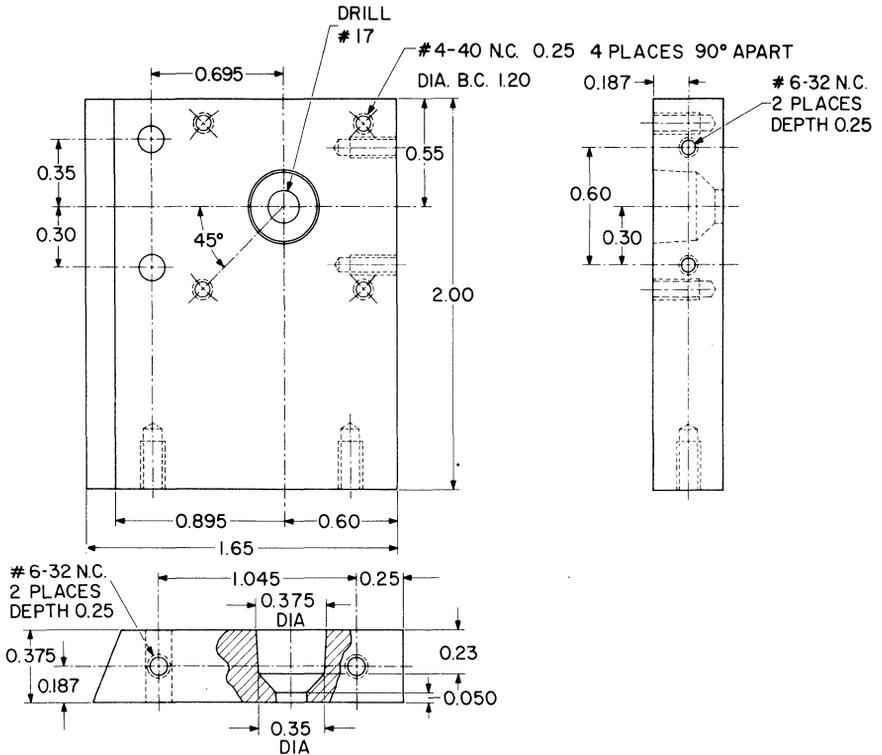


Fig. 5. Base piece No. 1, 2-Gc cavity.

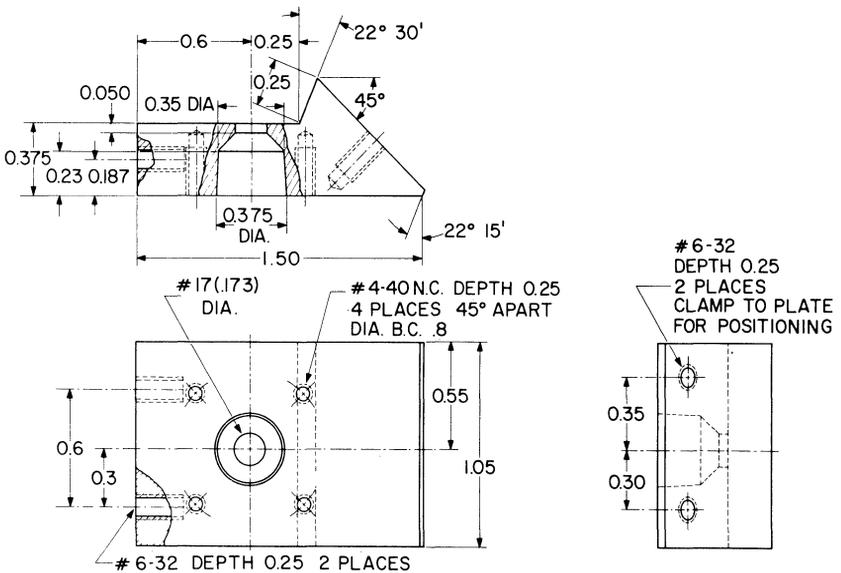


Fig. 6. Base piece No. 2, 2-Gc cavity.

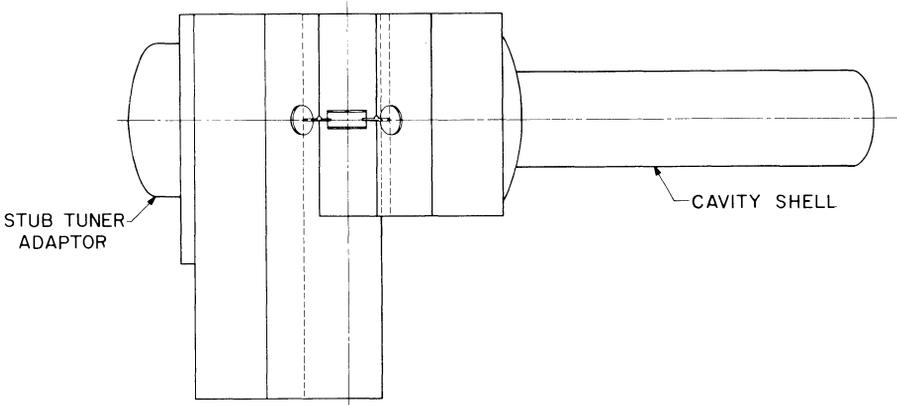


Fig. 7. Front view (without front plate), 2-Gc cavity.

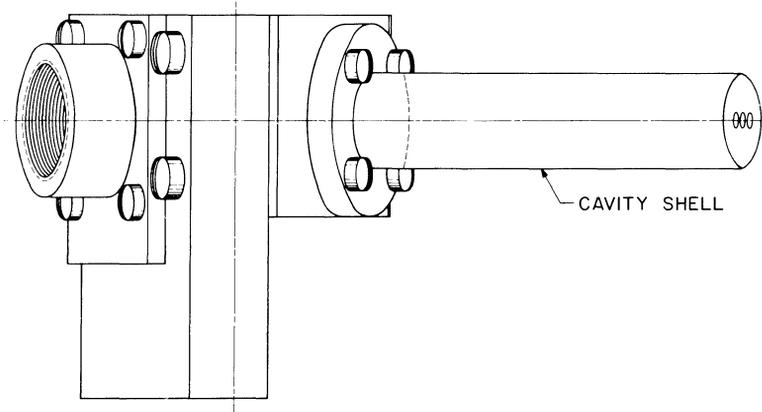


Fig. 8. Back view, 2-Gc cavity.

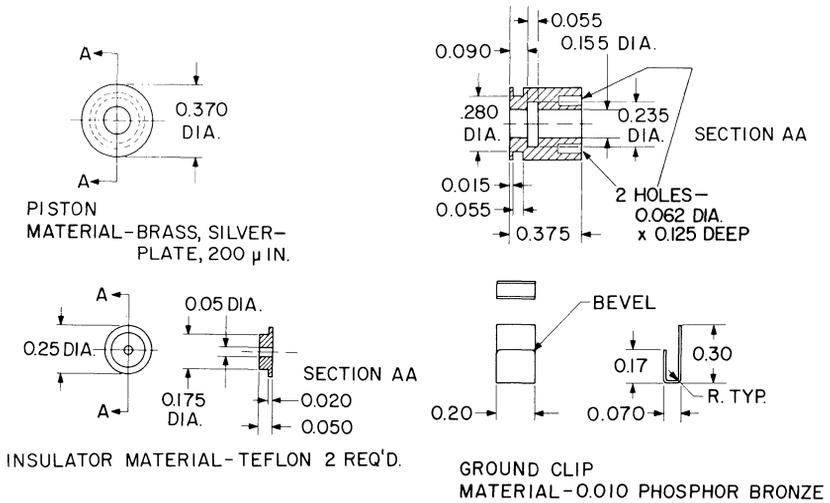


Fig. 9. Piston, ground clip, and Teflon insulator, 2-Gc cavity.

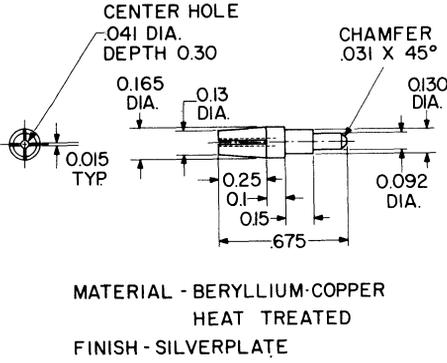


Fig. 10. Adapter pin No. 1, 2-Gc cavity.

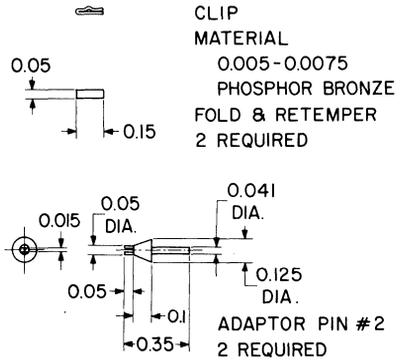


Fig. 11. Clip and adaptor pin No. 2, 2-Gc cavity.

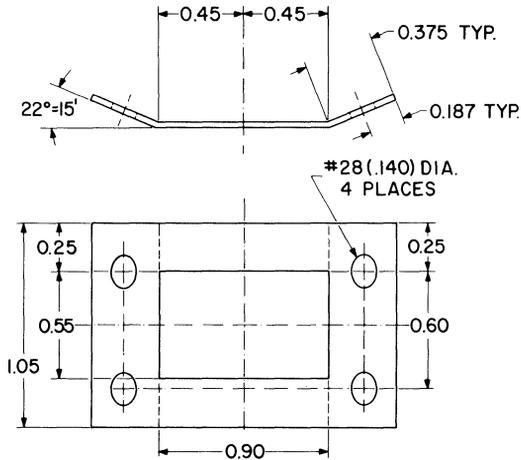


Fig. 12. Front plate, 2-Gc cavity.

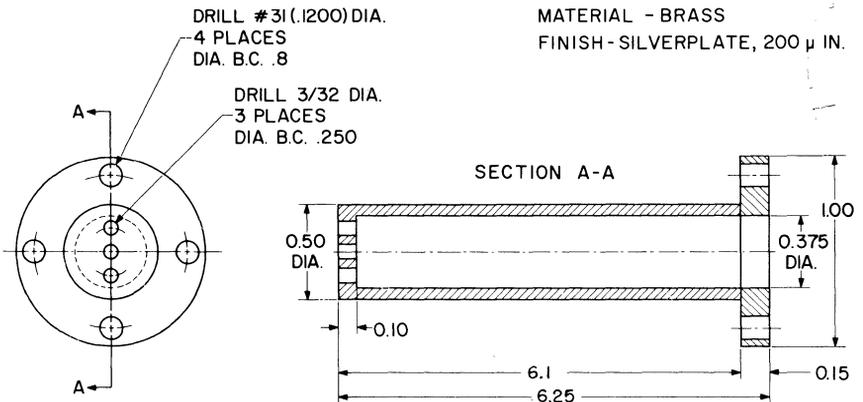
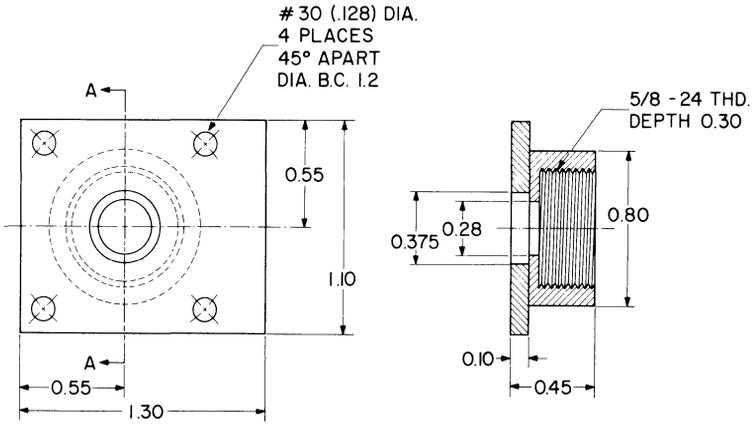
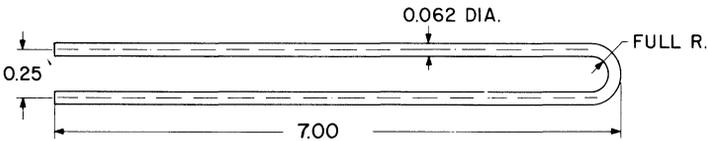
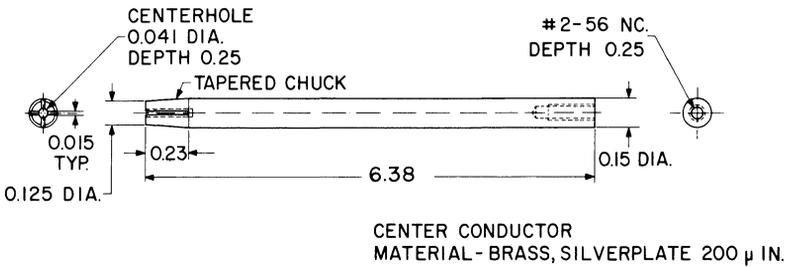


Fig. 13. Cavity shell, 2-Gc cavity.



MATERIAL - BRASS  
FINISH - SILVERPLATE, 200  $\mu$  IN.

Fig. 14. Stub tuner adaptor piece No. 1, 2-Gc cavity.



PULL BAR  
MATERIAL - BRASS, SILVERPLATE

Fig. 15. Inner conductor and pull bar, 2-Gc cavity.



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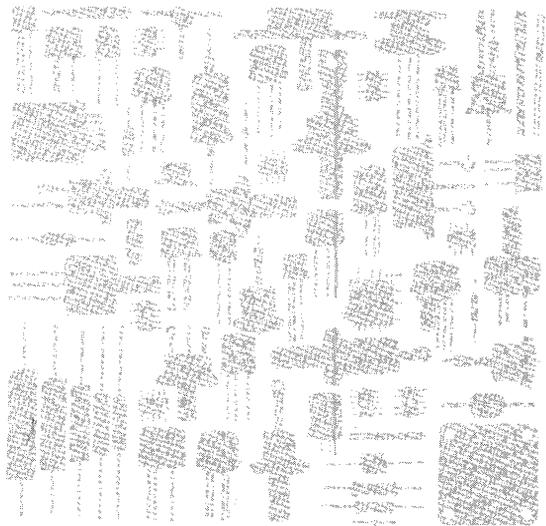
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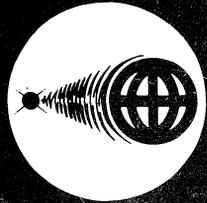


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