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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

This manual supports the following TEKTRONIX products:

8550 Option	8540 Option	Products
2P	2P	8300E26
3U	3U	8300P26
		8300P26 option 01

8500
MODULAR MDL SERIES
68000
EMULATOR PROCESSOR
AND
PROTOTYPE CONTROL PROBE
SERVICE

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

070-3770-00
Product Group 61

First Printing SEPT 1982

Printed in U.S.A.

PREFACE

ABOUT THIS MANUAL

This manual contains servicing information for the 68000 Emulator Processor module and its associated Prototype Control Probe. The manual applies to use of this equipment in the TEKTRONIX 8550 Microcomputer Development Lab or 8540 Integration Unit.

Throughout this manual, the term "microcomputer development system" (or simply "development system") refers to the TEKTRONIX 8550 Microcomputer Development Lab or 8540 Integration Unit.

The TEKTRONIX 68000 Emulator Processor module utilizes a Motorola MC68000L microprocessor to perform the emulation function. All references in this manual to the 68000 microprocessor pertain to the Motorola MC68000L microprocessor.

MANUAL ORGANIZATION

This manual is divided into 13 sections:

Section 1	contains general information about the Emulator Processor module and the Prototype Control Probe.
Section 2	contains information about electrical and environmental characteristics.
Section 3	discusses configuration jumpers and their functions.
Section 4	describes in detail the operation of the Emulator Processor module and Prototype Control Probe.
Section 5	contains functional check procedures for the development system.
Section 6	contains power supply adjustment procedures.
Section 7	contains Emulator Processor module and Prototype Control Probe performance check procedures and diagnostic information.
Section 8	describes general maintenance procedures.
Section 9	provides detailed installation procedures for the Emulator Processor module and the Prototype Control Probe.
Sections 10–13	contain technical reference material, electrical parts list, schematic diagrams, and mechanical parts list with accessories information, respectively.

GENERAL INFORMATION

Intended Use

This manual is designed to be used by trained service technicians; it is not designed for use as a training guide. The intent is to provide a sufficiently detailed theory of operation and accompanying reference material to enable a technician to locate a problem to a particular component on a circuit board.

Revision History

As this manual is revised and reprinted, revision history information is included on the text and diagrams. Existing manual pages that have been revised, are indicated by a REV and date (REV SEP 1982) at the bottom inside corner of the page. New pages added to an existing section (whether they contain old, new, or revised information) contain the word "ADD" alongside the revision date (Example: ADD SEP 1982).

Change Information

Change notices are issued by Tektronix, Inc., to document changes to the manual after it has been published. Change information is located at the back of this manual, following the yellow tab marked "CHANGE INFORMATION & TEST EQUIPMENT". When you receive the manual, you should enter any change information into the body of the manual, according to the instructions on the change notice.

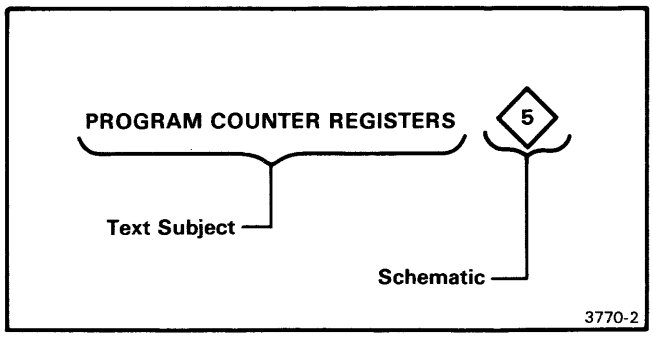
Notational Conventions

Hexadecimal

All addresses are in hexadecimal notation, unless otherwise noted. Where necessary for clarity, hexadecimal numbers are defined by an H following the number (i.e., 43ACH). Other hexadecimal identifiers, such as the prefix or suffix "hex" or subscripts denoting base 16, are not used.

Schematics

The schematics included in this manual have been drawn with grey overlays to highlight functional blocks of circuitry. The text is coordinated with these block overlays. Headings in the text indicate the schematic(s) that depict the circuit under discussion. The following example illustrates a text heading:



This example shows that:

- The subject of the text is the program counter registers.
- These registers appear on schematic 5.

Signal Lines

In this manual, signal line names followed by the symbol (L) are active in the low state. Lines that are active in the high state may have no symbol following their names, or an (H) following the name if an ambiguity might exist. For example:

PPDOUT(L)
CS16
IO(H)/M(L)

DOCUMENTATION OVERVIEW

Support documentation for TEKTRONIX development systems consists of service manuals, installation manuals, and user's manuals. To derive the greatest benefit from this manual, you should be familiar with your TEKTRONIX development system, as described in the appropriate manuals listed here. You should also be familiar with the 68000 microprocessor, described in The Complete Motorola Microprocessor Data Library, published by Motorola, Inc.

Service Manuals

Service manuals provide the information necessary to perform system testing, to isolate hardware problems, and to repair system components. Service manuals may be purchased from Tektronix as optional accessories.

The following manuals provide service information for the various host systems that support the 68000 Emulator Processor:

- 8301 Microprocessor Development Unit Service Manual
- 8540 Integration Unit Service Manual

Also available are service manuals for Emulator Processor modules, for peripheral equipment, and for optional features such as the PROM Programmer and the Trigger Trace Analyzer.

Installation Manuals

Installation manuals or guides tell how to unpack the equipment, and how to install it and verify its proper operation. Installation manuals may be separate manuals, or may be provided as supplements to existing publications. Installation manuals are provided with the equipment as a standard accessory.

The following installation manuals are available for the 68000 Emulator Processor and its host systems:

- 8500 MDL Series 68000 Emulator Processor and Prototype Control Probe Installation Service Manual
- 8550 Microcomputer Development Lab Installation Guide
- 8540 Integration Unit Installation Guide

The 68000 Emulator Processor and Prototype Control Probe Installation Service Manual is provided with the 68000 Prototype Control Probe as a standard accessory.

User's Manuals

User's manuals describe procedures required to operate the development system and its peripheral devices. User's manuals are provided as a standard accessory to the product.

For an overview of your development system and its capabilities, the following manuals may be of interest:

- 8550 Microcomputer Development Lab System Users Manual (with the 68000 Emulator Processor Specifics supplement)
- 8540 Integration Unit System Users Manual (with the 68000 Emulator Processor Specifics Supplement)

CONTENTS

ILLUSTRATIONS

TABLES

TABLE (Cont.)

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

As Marked on Equipment

DANGER high voltage.

Protective ground (earth) terminal.

ATTENTION - Refer to manual.

SAFETY PRECAUTIONS

Grounding the Product

This product is grounded through grounding conductors in the interconnecting cables. To avoid electrical shock, plug the supporting system's power cord into a properly wired receptacle. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product. Be sure the fuse is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

(Refer also to the preceding Operators Safety Summary)

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

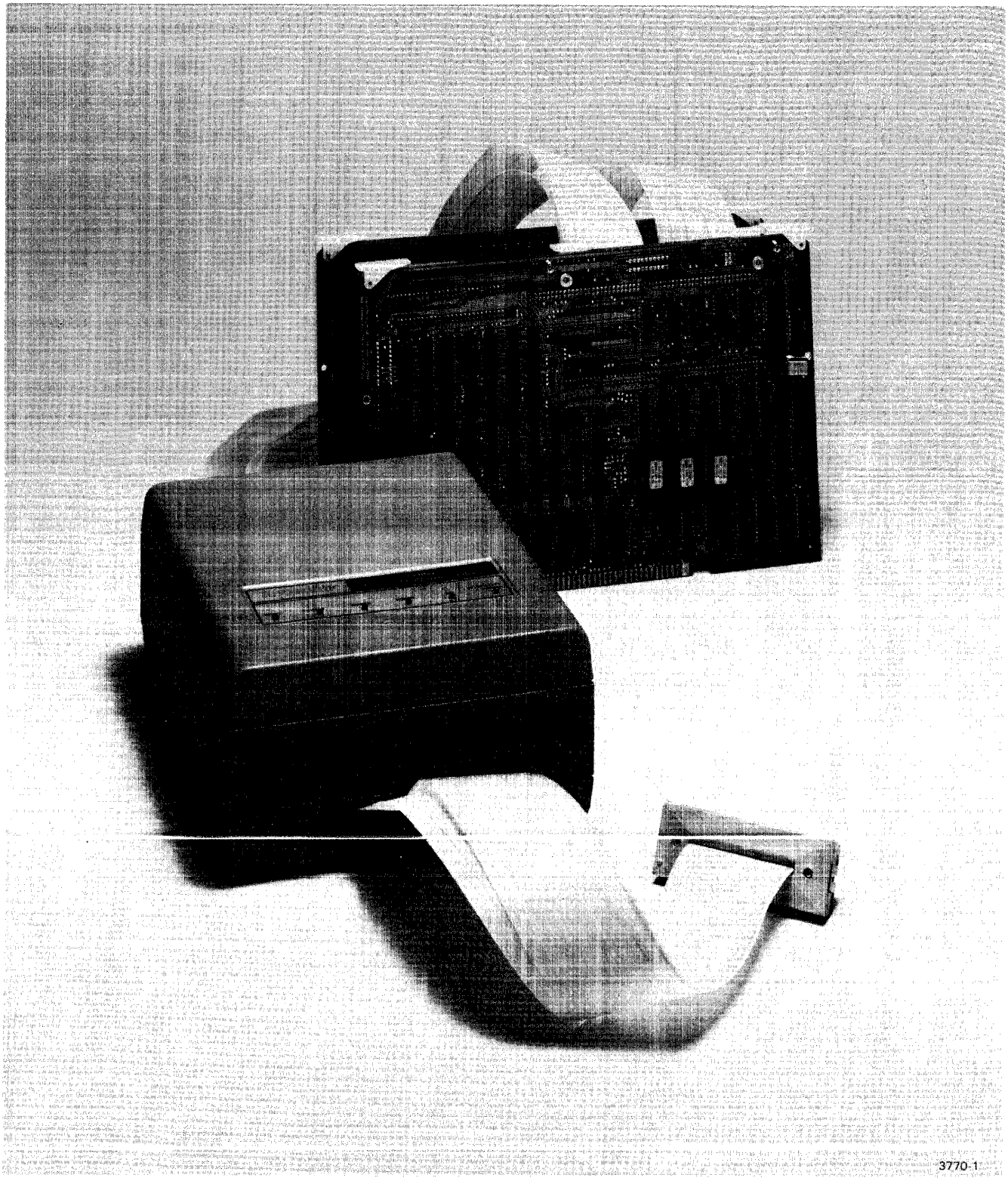
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

The system that supports this product is intended to operate from a power source that will not apply more than 250 volts between the supply conductors or between either supply conductor and ground. A protective ground by way of the grounding conductor in the supporting system's power cord is essential for safe operation of this product.



68000 Emulator Processor and Prototype Control Probe.

Section 1

GENERAL INFORMATION

INTRODUCTION

The 68000 Emulator Processor is a microprocessor design aid that emulates a 68000 microprocessor. The 68000 Emulator Processor is operated in conjunction with the 68000 Prototype Control Probe and a TEKTRONIX microcomputer development system. In this arrangement, the 68000 Emulator Processor and Prototype Control Probe effectively replace the 68000 microprocessor in a prototype circuit.

This section contains general information about the 68000 Emulator Processor and Prototype Control Probe.

Modes of Operation

The 68000 Emulator Processor module, with its Prototype Control Probe, may be operated in any one of three emulation modes. The mode is determined and set by the user. The emulator is controlled by the System Controller module in the microcomputer development system. The three emulation modes are:

MODE 0 — "System" mode. Mode 0 is used to develop software for a prototype 68000 microprocessor-based circuit. Mode 0 operation uses the development system's program memory, I/O facilities, and clock to execute a software program. In Emulation Mode 0, the development system acts as an independent 68000-based microcomputer. Prototype circuitry is not involved. Figure 1-1(a) illustrates Mode 0 operation.

MODE 1 — "Partial emulation" mode. Mode 1 is used to develop the hardware functions of the prototype circuit. The Prototype Control Probe is used as the interface between the prototype circuit and the Emulator Processor module. Clock and control signals for Emulation Mode 1 are provided by the prototype circuit.

Another function available in Emulation Mode 1 is memory mapping. Execution memory may be mapped (in 4 K blocks) into program memory or to the user prototype. Figure 1-1(b) illustrates Mode 1 operation.

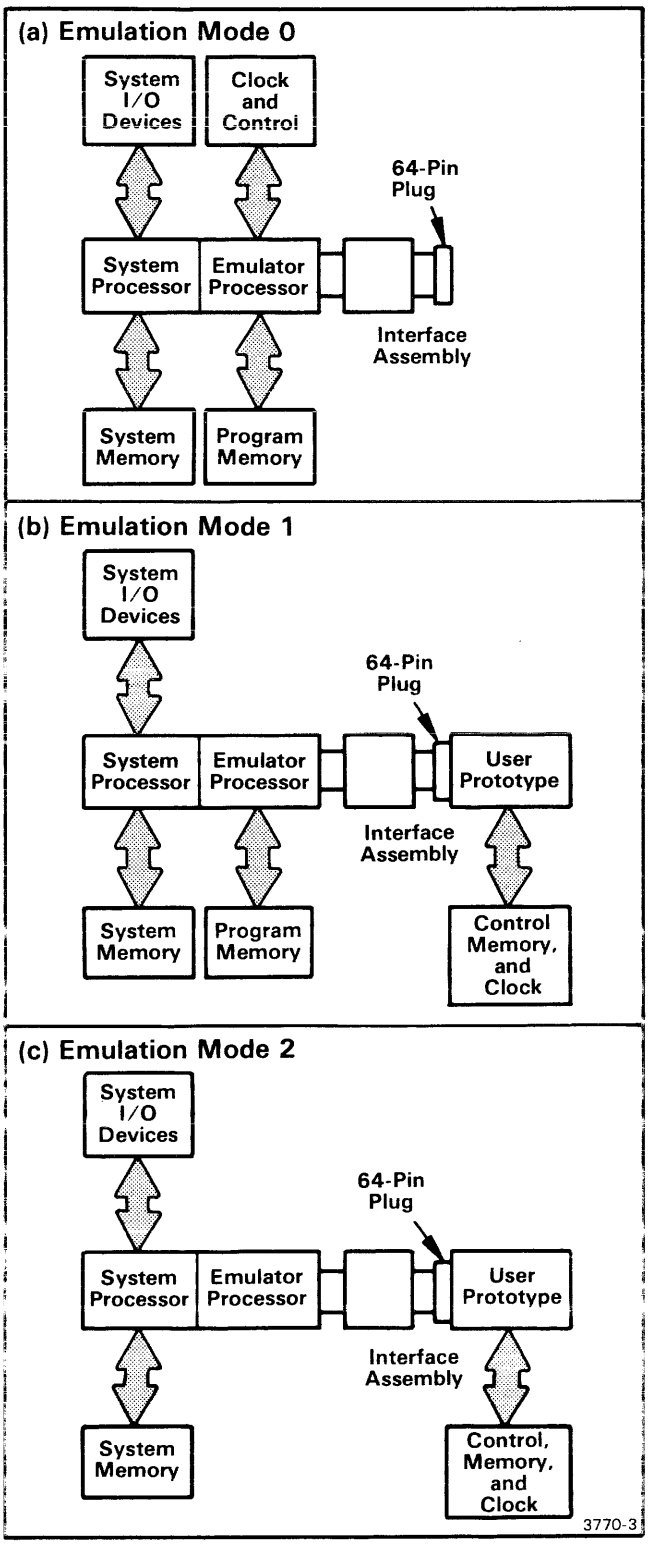


Fig. 1-1. Emulation Modes 0, 1, and 2.

MODE 2 "Full emulation" mode. Mode 2 is used for the final development stages of hardware and software integration in the prototype circuit. The only difference between Mode 1 and Mode 2 operation is that in Mode 2, prototype memory is the single source of operation code. Program memory cannot be accessed. Figure 1-1(c) illustrates Mode 2 operation.

EMULATOR PROCESSOR

The 68000 Emulator Processor and Prototype Control Probe are illustrated in Fig. 1-2. The Emulator Processor consists of:

- Two emulator circuit boards that plug into the Main Interconnect board in the development system mainframe. Throughout this manual, these circuit boards are referred to as EMU 1 and EMU 2.
- Two short ribbon cables that interconnect EMU 1 and EMU 2.

The Emulator Processor serves two purposes in the development system. First, the Emulator Processor has the ability to run a program written specifically for a 68000 microprocessor. With the help of other modules in the development system, the Emulator Processor can check the program for run-time errors or program logic errors. Second, when the Prototype Control Probe's 64-pin plug is used, a prototype circuit can be debugged and stepped through the final stages to design completion.

The 68000 Emulator Processor emulates the operation of a target 68000 microprocessor device that will be used in the final version of a prototype system. The Emulator Processor responds to software in the same way as the target microprocessor, and also allows software debugging.

PROTOTYPE CONTROL PROBE

As illustrated in Fig. 1-2, the 68000 Prototype Control Probe consists of:

- The Cable Termination board that plugs into EMU 1.
- The Interface Assembly, containing the Buffer, Control, Power Supply, and Mobile Microprocessor boards.
- Three six-foot ribbon cables that attach the Interface Assembly to the Cable Termination board.
- A 64-pin plug with two 1.5-foot ribbon cables that connect the Interface Assembly to the prototype circuit's 68000 microprocessor socket.

Five strain relief cable clamps are also shipped with the Prototype Control Probe to replace the original system cable clamps.

The Prototype Control Probe Interface Assembly contains the emulating microprocessor device, and thus is required for operation in all three emulation modes. In Mode 0 operation, the 64-pin plug may be connected to the prototype circuit, but will not use or drive any signals to or from the prototype. However, in Modes 1 and 2, the Prototype Control Probe acts as the interface between the Emulator Processor and the prototype circuit. Therefore, in Modes 1 and 2, the 64-pin plug must be connected to a prototype circuit.

Prototype Control Probe LEDs

Six indicator LEDs are visible on the Prototype Control Probe's Interface Assembly. When the Emulator Processor is operating in Emulation Mode 1 or 2, these LEDs indicate the following conditions:

- RESET: the Emulator Processor's RESET line has been driven low.
- HALT: the Emulator Processor's HALT line has been driven low.
- DTACK: the 68000 microprocessor has not received a DTACK (Data Transfer Acknowledge) within 1 ms of having requested one. This condition is referred to as a DTACK Timeout in this manual.
- BGACK: a Bus Grant Acknowledge has occurred (i.e., the 68000 microprocessor has acknowledged a prototype Bus Request).
- BG: a Bus Grant has occurred (i.e., the 68000 microprocessor has granted the bus following a Bus Request).
- Prototype Power: the prototype power supply is functioning.

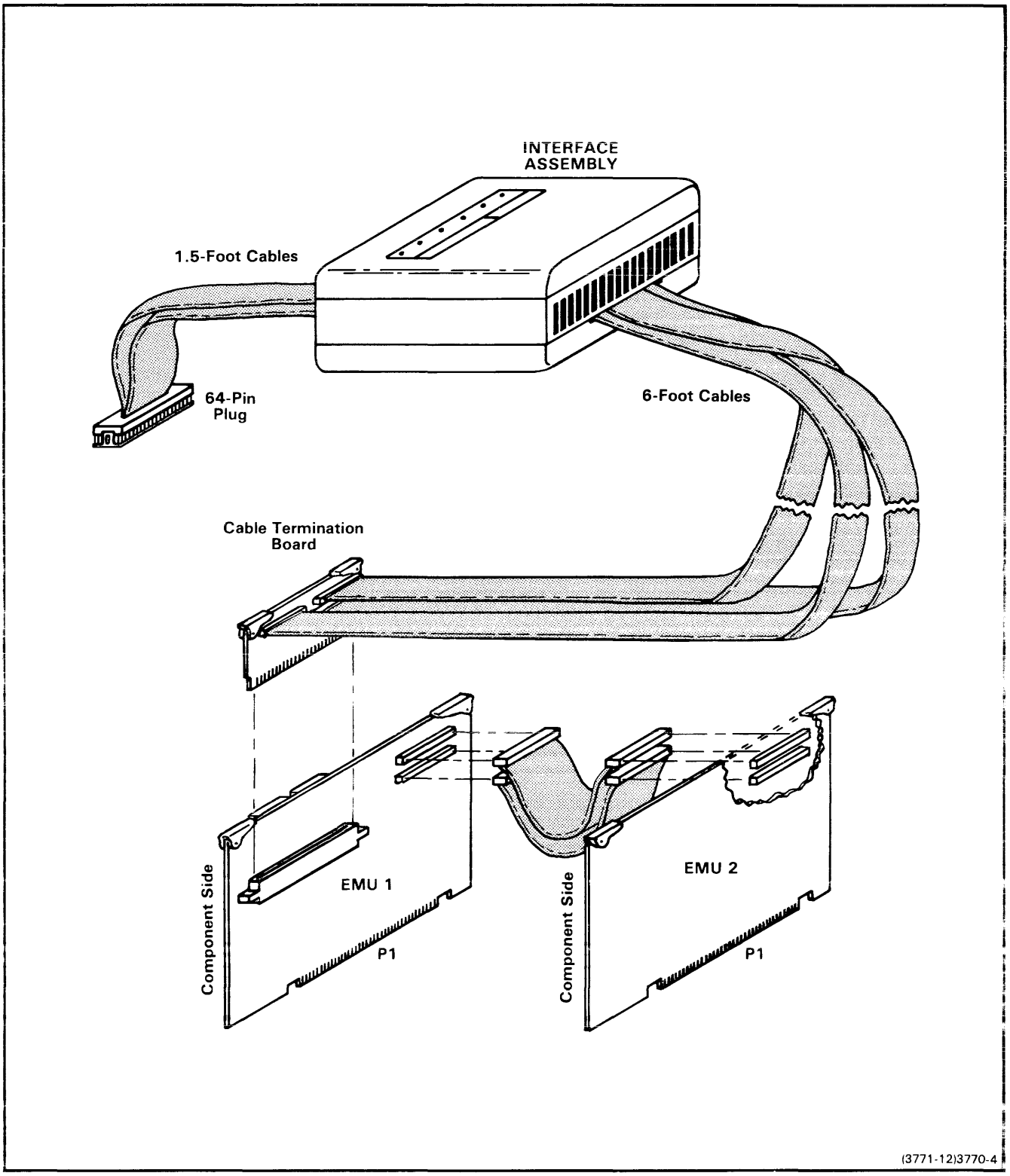


Fig. 1-2. 68000 Emulator Processor and Prototype Control Probe.

Section 2

SPECIFICATIONS

INTRODUCTION

The electrical and environmental characteristics listed here are general. For detailed environmental test procedures, including failure criteria, contact your local Tektronix Field Office or representative.

Electrical Characteristics

Five supply voltages are used by the 68000 Emulator Processor and Prototype Control Probe. Three of these (+5.2 Vdc, +12 Vdc, and –12 Vdc) are generated by the development system and are taken directly from its Main Interconnect board. The remaining two supply voltages (+4.9 Vdc and +5.2 Probe Vdc) are generated on the Power Supply board located in the Interface Assembly. The Emulator Processor and its Prototype Control Probe use the supply voltages as follows:

- Emulator Processor

  +5.2 Vdc—Primary supply voltage.

- Prototype Control Probe

  +5.2 Vdc—Used by the Buffer, Control, and Mobile Microprocessor boards.

  –12 Vdc—Used to power the fan in the Interface Assembly when the Emulator Processor is active.

  +12 Vdc—Used by the Power Supply board to generate the +4.9 Vdc and +5.2 Probe Vdc supply voltages when the Emulator Processor is active.

  +4.9 Vdc—Supplies power for the Buffer and Control boards. This is a regulated supply and is active only when the Emulator Processor is selected (active).

  +5.2 Probe Vdc—Used only by the 64-pin plug when the Emulator Processor is selected (active).

Each of the three supply voltages generated by the development system is protected at the Cable Termination board with a 3AG, 250 Volt, 2 Ampere fuse.

The supply voltages generated on the Power Supply board located in the Interface Assembly are not fused.

Table 2-1
Electrical Characteristics

Characteristic	Performance Requirements	Supplemental Information
Supply Voltages	+5.2 Vdc +1%/-2% +12 Vdc ±5% -12 Vdc ±5% +4.9 Vdc ±20 mV +5.2 Probe Vdc +50 mV/-.2 V	 Adjustable (See Section 6.) Adjustable (See Section 6.)
Current		Emulator not selected 6.8 A (max) @ +5.2 Vdc 150 mA (max) @ +12 Vdc Emulator selected 6.8 A (max) @ +5.2 Vdc 1.65 A (max) @ +12 Vdc 300 mA (max) @ -12 Vdc 3.4 A (max) @ +4.9 Vdc 15.3 mA (max) @ +5.2 Probe Vdc

Environmental Characteristics

Table 2-2
Environmental Characteristics

Characteristic	Description
Air Temperature Operating Storage	 0°C to +50°C (+32°F to +122°F) –55°C to +75°C (–67°F to +167°F)
Humidity	90% relative non–condensing (maximum)
Altitude Operating Storage	 4 500 m (15,000 ft) maximum 15 000 m (50,000 ft) maximum

Section 3

OPERATING INFORMATION

INTRODUCTION

The 68000 Emulator Processor and Prototype Control Probe have user-selectable configuration jumpers. This section describes the functional characteristics for the individual jumpers. Only user-selectable jumpers are discussed here. All other jumpers are for factory use only and are not user-selectable. Section 8 of this manual tells how to disassemble and reassemble the Prototype Control Probe to gain access to the jumpers.

This section also contains a brief description of development system jumpers and straps that directly influence the 68000 Emulator Processor.

CONFIGURATION JUMPERS

The following pages describe each jumper used to select specific operations of the 68000 Emulator Processor. All jumpers are in their 'normal' position (1—2) when shipped from the factory. These jumpers affect the operation of all three emulation modes unless otherwise indicated within the text. Some jumper configurations available may cause the system to hang (not respond) and are noted accordingly.

NOTE

EMU 1 and EMU 2 must be removed from your microcomputer development system, to allow access to jumpers located on these boards. Section 9 of this manual tells how to remove the circuit boards from the development system.

EMU 1

EMU 1 of the 68000 Emulator Processor contains one configuration jumper: P1080. Figure 3-1 shows the location of P1080 on EMU 1.

P1080 determines whether control returns to the development system or remains with the prototype circuit after an Emulator Processor halt condition has occurred, that is, when a double bus error or double address error has occurred.

Normal (1–2)	When an Emulator Processor halt condition occurs, control is returned to the development system.
Option (2–3)	When an Emulator Processor halt condition occurs during Mode 0 operation, control is returned to the development system. In Mode 1 or 2 operation, control remains in the prototype circuit.

NOTE

When P1080 is in its option (2–3) configuration and the Emulator Processor is operating in Emulation Mode 1 or 2, the system will hang until the prototype circuit resets the 68000 microprocessor. (The 68000 must exit the halt condition.)

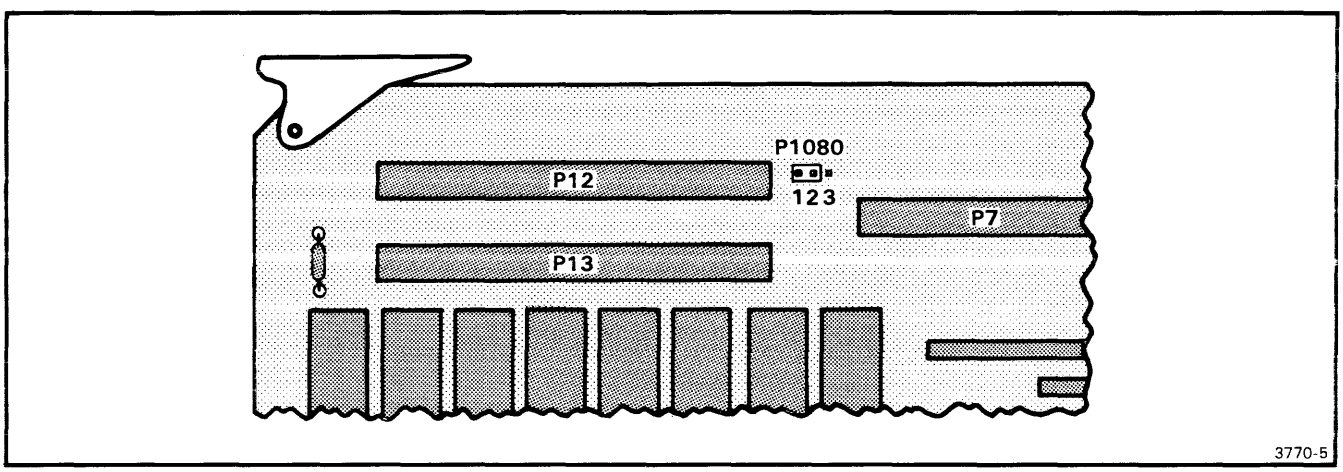


Fig. 3-1. EMU 1 jumper location.

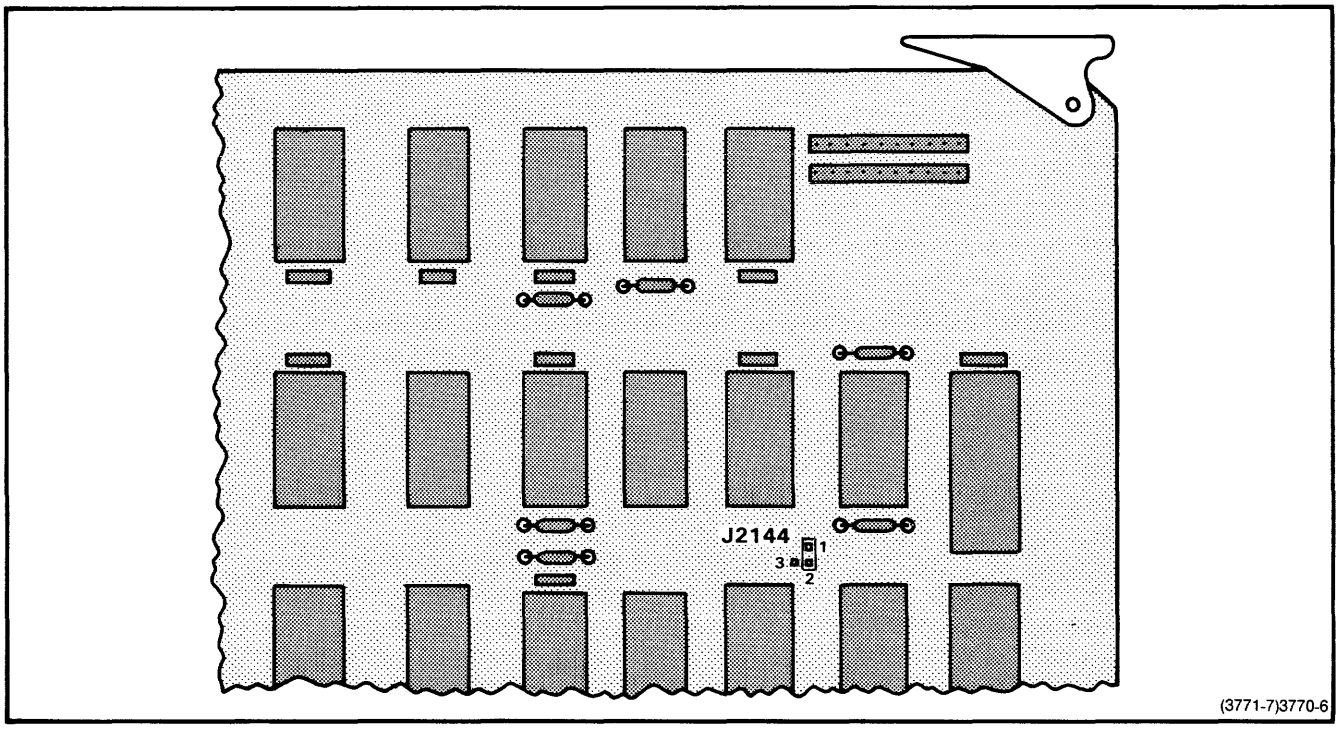


Fig. 3-2. EMU 2 jumper location.

EMU 2

EMU 2 contains one configuration jumper: J2144. Figure 3-2 shows the location of J2144 on EMU 2.

J2144 controls the break cycle of the Emulator Processor after the emulator has executed a stop instruction.

Normal (1–2) — When a stop instruction is executed, the Emulator Processor breaks and returns control to the operating system only while the emulator is operating in Emulation Mode 0.

Option (2–3) — When a stop instruction is executed, the Emulator Processor breaks regardless of the emulation mode, and returns control to the operating system.

NOTE

If the Emulator Processor is being operated in Emulation Mode 1 or 2 and J2144 is in its normal (1–2) configuration, the emulator will appear to hang (not respond) when a stop instruction is encountered. To return control to the operating system, you must request that the Emulator Processor break (for example, by typing CTRL-C) or issue a prototype interrupt. For more information on how to request the Emulator Processor to break, refer to your System Users Manual and its 68000 Emulator Specifics supplement.

Buffer Board

The Buffer board contains six configuration jumpers: P1, P2, P3, P6, P7, and P8. Figure 3-3 shows the location of these jumpers on the Buffer board. To gain access to these jumpers, perform steps 1–7 of the Prototype Control Probe Disassembly/Assembly procedure located in Section 8 of this manual.

P1 inserts or removes a delay between the prototype circuit's Data Transfer ACKnowledge (DTACK) and the 68000 microprocessor while the emulator is operating in Emulation Mode 1.

NOTE

The configuration of jumper P1 depends on the configuration of Mobile Microprocessor board jumpers J1045 and J2045. For more information, see the discussion of the Mobile Microprocessor board jumpers later in this section.

Normal (1–2) — The prototype's DTACK is delayed at the rate determined by J1045 and J2045. This prevents overdriving the Program Memory's access time.

Option (2–3) — This configuration bypasses J1045 and J2045, allowing the prototype to return DTACK without delay.

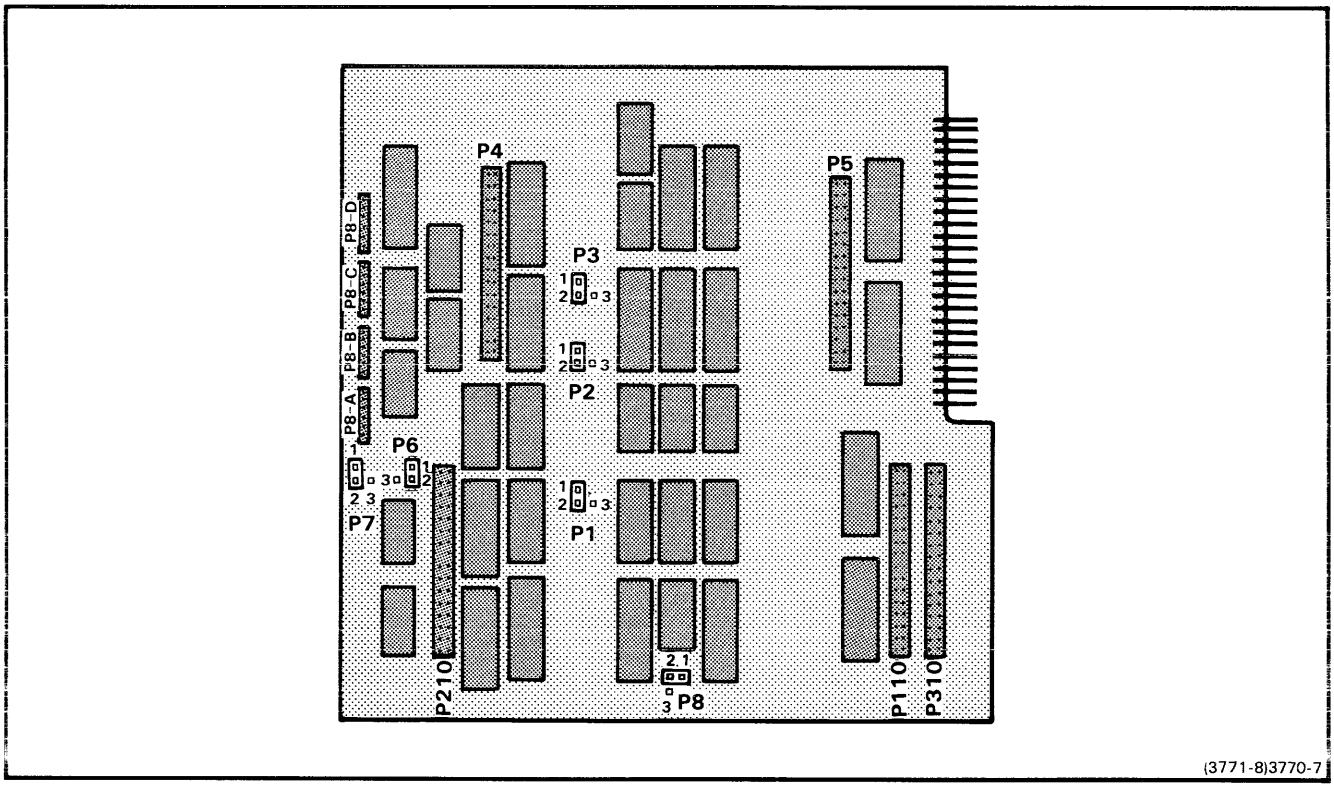


Fig. 3-3. Buffer board jumper locations.

NOTE

When P1 is in its optional (2–3) configuration, data may be invalid or lost if Program Memory is accessed beyond its limitations. However, no component damage will result.

P2 and P3 control prototype bus arbitration during an Emulator Processor Dump and Restore routine.

Normal (both jumpers 1–2)	The prototype's Bus Request and Bus Grant Acknowledge signals to the 68000 microprocessor are disabled when the Emulator Processor has returned control to the operating system.
Option (both jumpers 2–3)	The prototype's Bus Request and Bus Grant Acknowledge signals are allowed to request and hold the 68000 microprocessor bus. This is valid even while the Emulator Processor has entered Dump and Restore and has returned control to the operating system.

NOTE

In the optional (2–3) configuration for P2 and P3, the emulator may hang (not respond). To return to normal operation, you must release the bus (for example, by typing CTRL-C). Refer to your System Users Manual and its 68000 Emulator Specifics supplement for more information on how to release the bus.

P6 determines when the 68000 microprocessor address strobe is driven to the prototype circuit.

Normal (1–2)	The 68000 microprocessor address strobe is driven in all cycles except during an Emulator Processor Dump and Restore, or during an interrupt acknowledge of a non-maskable interrupt (NMI) issued by the Emulator Processor.
Option (2–3)	The 68000 microprocessor address strobe is driven in all cycles except during an interrupt acknowledge of an NMI issued by the Emulator Processor.

P7 controls how the Emulator Processor reacts to a DTACK timeout (no prototype DTACK within 1 ms). This jumper is used when any of the following conditions exist:

- P8 is in its normal position and no prototype DTACK is generated when memory is mapped to the prototype.
- P8 is in its optional position and no DTACK is generated by the prototype circuitry.
- The development system is operating in Emulation Mode 2 and no prototype DTACK is generated.

Normal (1–2)	The emulator will hang (not respond) until a DTACK is received from the prototype or a break condition occurs.

Option (2–3) The emulator will hang until a DTACK is received from the prototype, at which time the system will continue normal operation. A break condition will not clear the system.

P8 controls the internal generation of a Data Transfer AC-Knowledge (DTACK) signal by the 68000 Emulator Processor while operating in Emulation Mode 1.

Normal (1–2) If memory is mapped to the development system's Program Memory, then an internal DTACK is generated. If memory is mapped to the prototype, then DTACK must be generated by the prototype circuitry.

Option (2–3) Internal generation of a DTACK signal is not allowed, regardless of mapping. All DTACK signals must originate from the prototype circuitry.

NOTE

When P8 requires a prototype DTACK, the prototype circuit must generate a DTACK within 1 ms. If a prototype DTACK is required by P8 but is not generated within 1 ms, then a DTACK timeout occurs. For more information regarding when a DTACK timeout may occur, see the discussion of jumper P7, earlier in this section.

Control Board

The Interface Control board contains two configuration jumpers: J4011 and J6021. Figure 3-4 shows the location of these jumpers on the Control board. To gain access to these jumpers, perform steps 1–7 of the Prototype Control Probe Disassembly/Assembly procedure located in Section 8 of this manual.

J4011 controls whether non-maskable interrupts (NMIs) are saved during Dump and Restore (D/R) routines.

Normal (1–2) NMIs are saved during D/R routines (such as when the development system has control and the emulator is not running).

Option (2–3) NMIs are not saved.

NOTE

Saved NMIs are issued to the 68000 microprocessor when the development system relinquishes control and the Emulator Processor begins program execution.

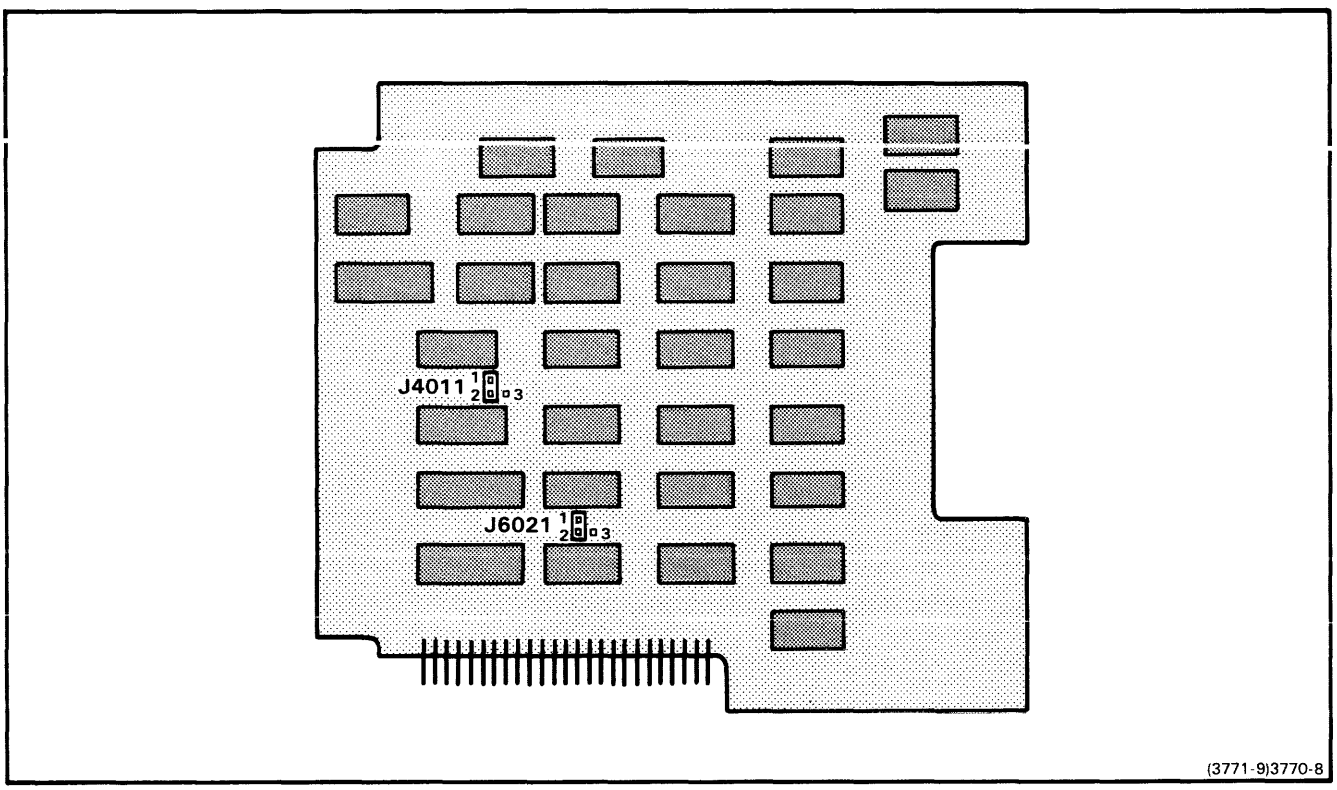


Fig. 3-4. Control board jumper locations.

J6021 controls whether prototype circuit interrupts (interrupt levels 1–6) are saved during Dump and Restore (D/R) routines.

Normal (1–2)	Prototype circuit interrupts (if held until acknowledged) are saved during D/R routines (such as when the development system has control and the emulator is not running).
Option (2–3)	Prototype circuit interrupts are not saved.

NOTE

Saved interrupts are issued to the 68000 microprocessor when the development system relinquishes control and the Emulator Processor begins program execution.

J1045 and J2045. In their option positions, these jumpers delay assertion of Data Transfer ACKnowledge (DTACK) signals to the Emulator Processor, to prevent Program Memory from being accessed faster than its limitations will allow. Two different DTACK signals may be issued to the Emulator Processor: the 68000 microprocessor's DTACK and the prototype's DTACK. With J1045 and J2045 in their 'option' positions:

- Assertion of the 68000 microprocessor DTACK signal is delayed to the Emulator Processor.
- Assertion of the prototype's DTACK signal is delayed to the Emulator Processor only when jumper P1 is in its 'normal' position during Mode 1 emulation. (See the discussion of Interface Buffer board jumper P1, earlier in this section.)

The jumper positioning, as shown in Table 3-1, is based on which Program Memory configuration is installed in your development system.

NOTE

When J1045 and J2045 are in their normal configuration and Program Memory is accessed beyond its limitations, data may be invalid or lost. However, no component damage will result.

Mobile Microprocessor Board

The Mobile Microprocessor board contains two configuration jumpers: J1045 and J2045. Figure 3-5 shows the location of these jumpers on the Mobile Microprocessor board. To gain access to these jumpers, perform steps 1–9 of the Prototype Control Probe Disassembly/Assembly procedure located in Section 8 of this manual.

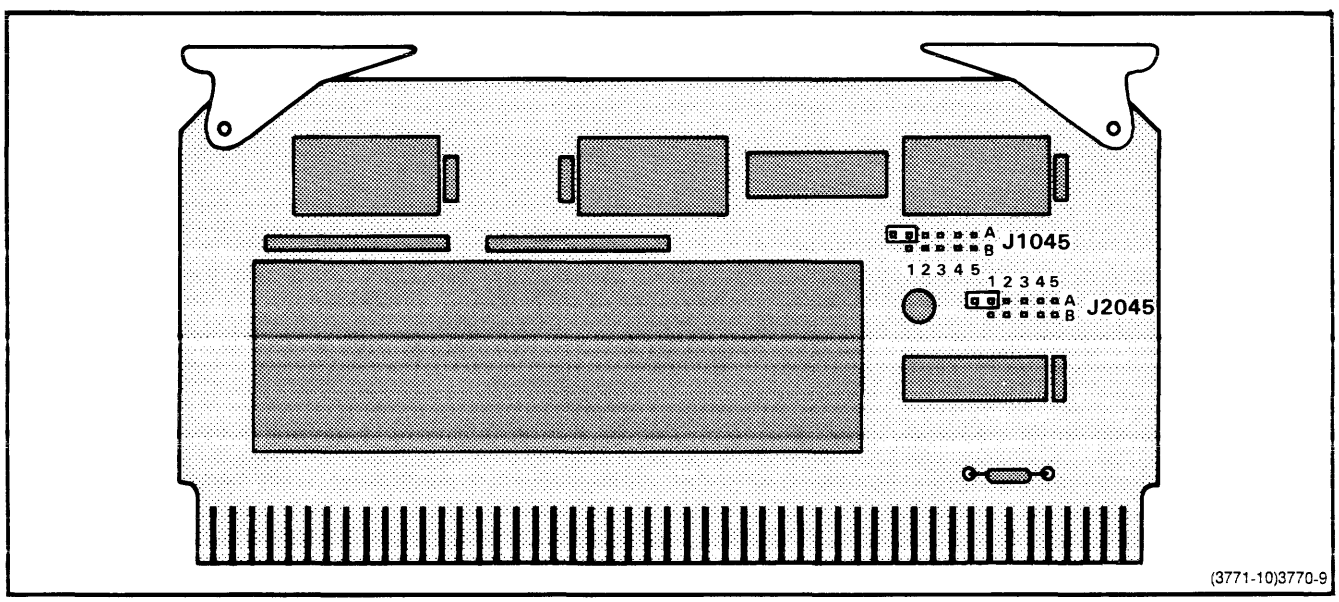


Fig. 3-5. Mobile Microprocessor board jumper locations.

As shown, the Mobile Microprocessor's jumpers (J1045 and J2045) are in their A1 to A configuration.

Table 3-1
J1045 and J2045 Configurations[a]

Memory Configuration	Jumper Configuration[b]		
	J1045	J2045	Characteristic
32K Program Memory board	A1 to A	A1 to A	Normal (no delay)
64K or 128K Static Program Memory board	A1 to A	A1 to A	Normal (no delay)
64K or 128K Static Program Memory board and Memory Allocation Control	A1 to A	A1 to A	Normal (no delay)
32K Program Memory board and Memory Allocation Control	A5 to B	A1 to A	Option (one wait state delay at ≥6.4 MHz)[c]

[a] **Jumper configurations listed are for ≤8 MHz operation.**

[b] **Jumper configurations not listed for J1045 and J2045 are for future use.**

[c] **One wait state is equivalent to one extra clock cycle per memory cycle.**

EMULATOR PROCESSOR JUMPER DEFAULT POSITIONS

The 68000 Emulator Processor has 12 user-selectable jumpers (discussed in detail, earlier in this section). Table 3-2 lists the default position and board location for each of these jumpers.

Table 3-2
Emulator Processor Jumper Default Positions

Jumpers	Default Positions	Board	Fig. No.
P1080	1–2	EMU 1	3-1
J2144	1–2	EMU 2	3-2
P1 P2 and P3 P6 P7 P8	1–2 Both 1–2 1–2 1–2 1–2	Buffer board	3-3
J4011 J6021	1–2 1–2	Control board	3-4
J1045 and J2045	Both A1–A	Mobile Microprocessor board	3-5

SYSTEM JUMPERS AND STRAPS

For proper operation with the 68000 Emulator Processor, the development system jumpers and straps listed in Tables 3-3, 3-4, and 3-5 must be in the indicated positions. For more information about these jumpers and straps, refer to your development system's installation guide.

Table 3-3
32K Program Memory Board
Normal Operating Configuration

Jumper/ Switch	Designation	Setting
W5011	Delayed Read Enable strap	2–3 Disable
J5175	Memory Relocation Enable/Disable jumper	2–3 Disable
J6175	Low/High Board jumper (1st board)	2–3 Low
J6175	Low/High Board jumper (2nd board, segment 00, if used)	1–2 High
J6175	Low/High Board jumper (2nd board, segment 01–7F, if used)	2–3 Low
J6179	System/Program Memory jumper	1–2 Program
J7171	Extended Bank Enable jumper	1–2 Enable
SW7170	Extended Memory DIP switch (1st board)	OFF (all)
SW7170	Extended Memory DIP switch (2nd board)	[a]

[a] For the 68000 Emulator Processor, the Extended Memory DIP switch, SW7170, selects which 64K page the memory will respond to. Switches A16–A23 correspond to the 68000 address lines, A16–A23. One Program Memory low board must always be set for segment 00 operation (all the SW7170 switches to the OFF position).

Table 3-4
Emulator Controller Board
Normal Operating Configuration

Jumper/ Switch	Designation	Setting
W1111	Extended Address Enable strap	1–2 Enable
J1183	Front Panel Hold Enable/Disable jumper	2–3 Disable
J3073	Interrupt Direct/Indirect jumper	2–3 Indirect
W4153	Immediate Interrupt Option strap	1–2 Single
W4163	Forced Jump Option strap	1–2 Int 29
W4165	Forced Jump Option strap	1–2 Disable
J5177	SVC Detection jumper	1–2 SLV OPREQ

Table 3-5
64K/128K Static Program Memory
Normal Operating Configuration

Jumper/ Switch	Designation	Setting
J7090	Read Delay jumper	0 Delay
J7191	System/Program Select strap	No Strap
J7192	System/Program Select strap	No Strap
J7193	System/Program Select strap	No Strap
J7194	System/Program Select strap	No Strap
J7193	Address Select jumpers	[a]

[a] Refer to the 64K/128K Static Program Memory Service Manual for proper jumper selection.

Section 4

THEORY OF OPERATION

INTRODUCTION

This section provides the following information:

- Information Flow. A general description of information flow through the 68000 Emulator Processor.
- Emulator Processor Overview. A block diagram overview of the Emulator Processor.
- Circuit Descriptions. A detailed description of the Emulator Processor and Prototype Control Probe circuitry.
- Typical Emulation Cycle. An example of a typical emulation cycle using the command "G 100".

INFORMATION FLOW

The following text describes information flow between the 68000 Emulator Processor, the development system, and the prototype circuit (via the Prototype Control Probe). Figure 4-1 illustrates the connections between the Emulator Processor and the Prototype Control Probe. Figure 4-2 is a simplified block diagram of the Emulator Processor, and further illustrates the information flow. Refer to these illustrations as you read the following descriptions.

Refer to Section 9 of this manual for the 68000 Emulator Processor and Prototype Control Probe installation procedure.

Edge Connectors P1

The 68000 Emulator Processor has two circuit boards: EMU 1 and EMU 2. Each board has a connector labeled P1 that plugs into the development system's motherboard. EMU 1 and EMU 2 are functionally one board, and their connections to the development system are treated as one connection.

The development system data and address buses, and certain control lines, are connected to the Emulator Processor at P1. The data and address flow through P1 is bidirectional, and buffered in both directions.

Edge Connector Socket J2

The receptacle for the Cable Termination board is J2 on EMU 1. Data and control flow are bidirectional and buffered in both directions. Address flow and buffering are from the Prototype Control Probe only.

P6 and P7

Connections P6 and P7 are referred to as the Top Plane Interconnect Bus. The optional Trigger Trace Analyzer (TTA) and Memory Allocation Controller (MAC) boards are connected to the Emulator Processor through the Top Plane Interconnect Bus. Address, data, and control signals flow over this bus and are not buffered

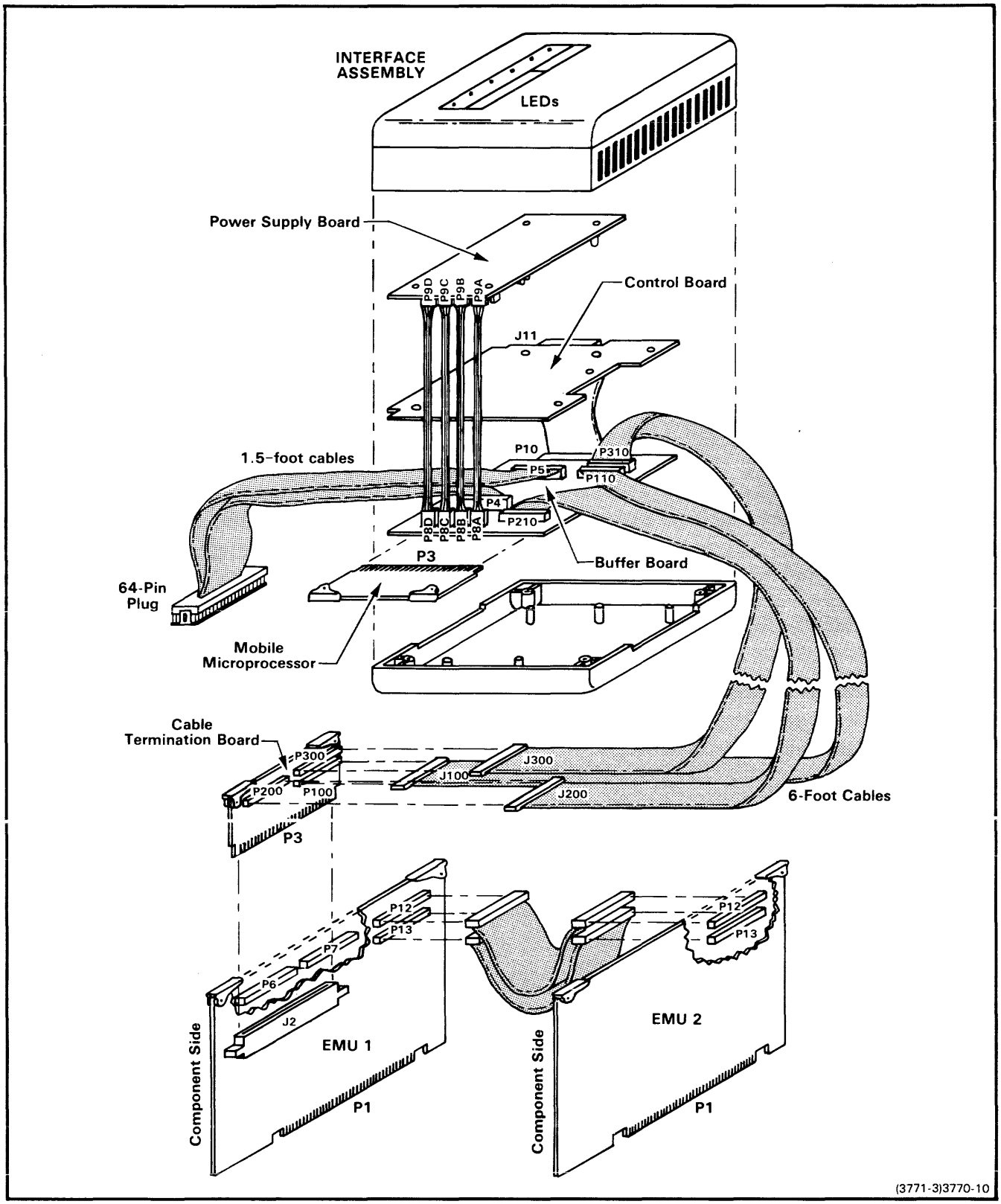


Fig. 4-1. 68000 Emulator Processor interconnections.

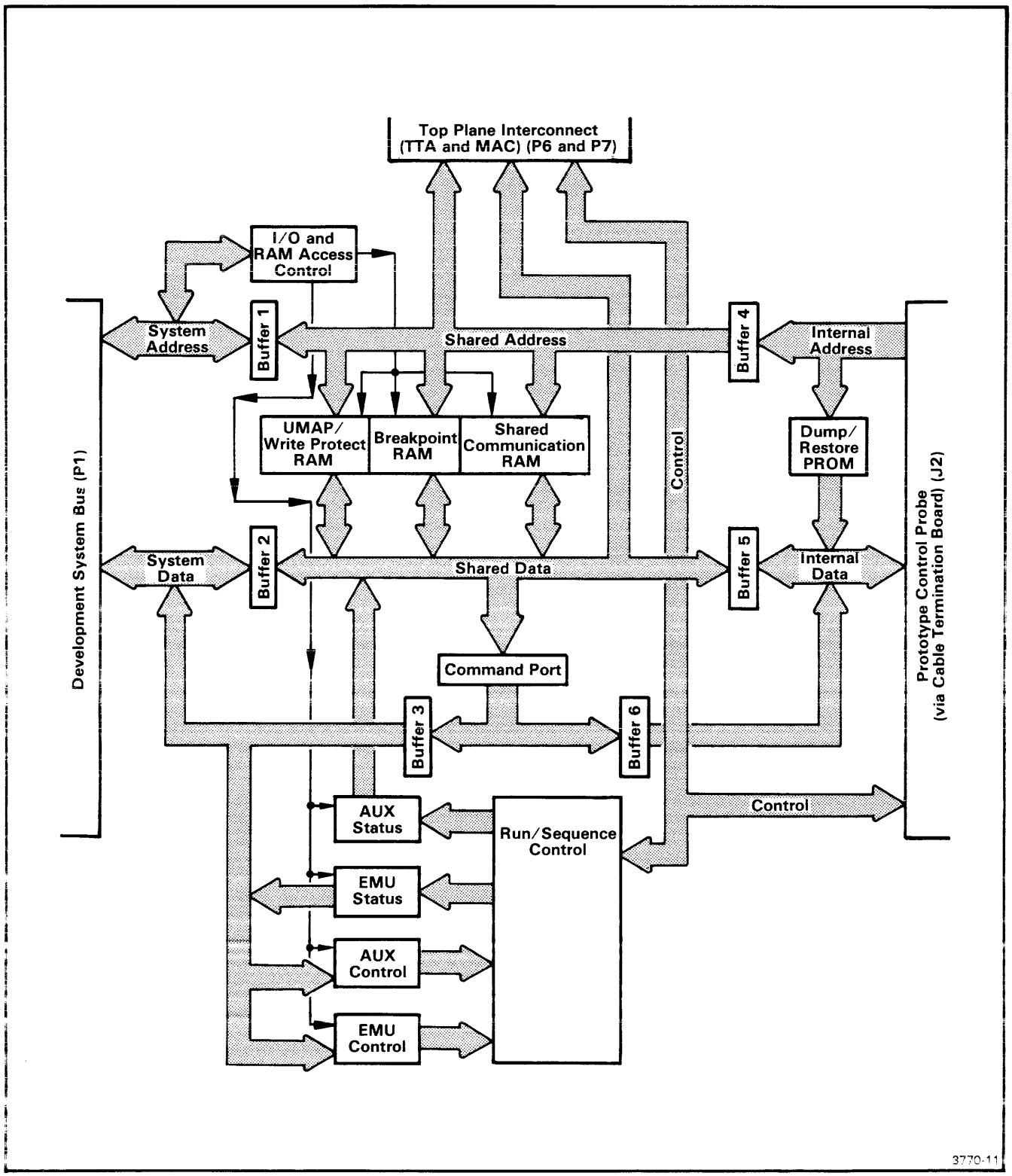


Fig. 4-2. 68000 Emulator Processor simplified block diagram.

Prototype Control Probe

The 68000 Prototype Control Probe contains address, data, and control line buffers, the microprocessor device, and driver/receiver devices. A 64-pin plug at the end of the Prototype Control Probe plugs into the 68000 microprocessor socket in the prototype circuit. When the Prototype Control Probe is plugged into the prototype circuit, the prototype sees the 68000 Emulator Processor as a 68000 microprocessor device.

Mobile Microprocessor Board

The Mobile Microprocessor board, located in the Prototype Control Probe's Interface Assembly, contains the key element to emulation: a 68000 microprocessor device. The microprocessor device communicates with the rest of the system by way of edge connector P3.

EMULATOR PROCESSOR OVERVIEW

The 68000 Emulator Processor is used in the development of prototype hardware and software. Interface and multiplexing circuitry connect the 68000 microprocessor device, located on the Mobile Microprocessor board, to either the development system bus or the Prototype Control Probe. Control for the 68000 Emulator Processor is provided by the System Processor (2650) located in your development system. For more information about the interaction of the various modules in the development system, refer to your development system's service manual.

Figure 4-2 is a simplified block diagram of the 68000 Emulator Processor. Although the Emulator Processor consists of two circuit boards (EMU 1 and EMU 2), functionally it is a single board. The following pages provide a functional-level description of the individual blocks of circuitry shown in Fig. 4-2. Later in this section, we'll describe the circuitry in more detail.

EMU Status Port (AD)

The EMU Status Port is read by the development system and written to by the Run/Sequence Control logic. The information contained in this port is shown in Fig. 4-3, and is concerned with the 68000 microprocessor's running status. The most important function of this port is to inform the development system when the 68000 has halted and cannot be started by the normal sequence. (The Emulator's normal starting sequence is discussed under the heading "A Typical Emulation Cycle," later in this section.)

AUX Status Port (8E)

The AUX Status Port contains information about the running status of the 68000 microprocessor (see Fig. 4-4). The AUX Status Port is read by the development system and written to by the Run/Sequence Control logic. When this port is read, its contents are automatically reset.

EMU Control Port (AD)

The EMU Control Port is written to by the the development system and read by the Run/Sequence Control logic, discussed later in this section. This write/read function provides a path through which the development system controls the Emulator Processor. As shown in Fig. 4-5, the EMU Control Port contains the following information:

- D1—RAMEN. This bit is asserted high to enable the Emulator Processor's on-board RAM for development system access.
- D2—EMU ACTIVE. This bit is asserted high to activate the Emulator Processor.
- D5, D6—Emulation Mode. These bits are used to select Emulation Mode 0, 1, or 2, as shown in Table 4-1.
- D7—PROBEPWR. This bit is asserted high when the Emulator Processor is selected (activates the Prototype Control Probe's Power Supply board).

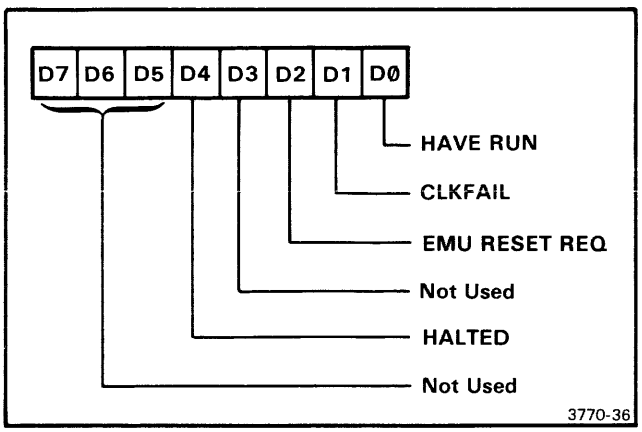


Fig. 4-3. EMU Status Port

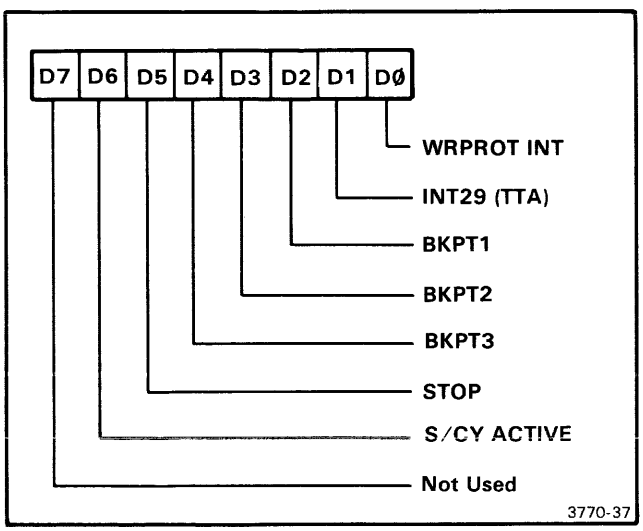


Fig. 4-4. AUX Status Port.

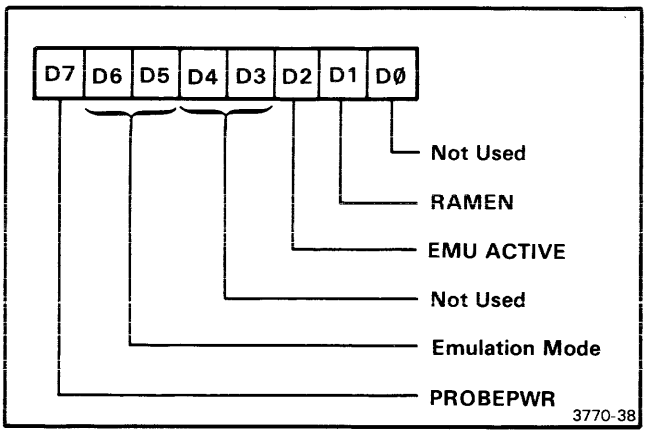


Fig. 4-5. EMU Control Port.

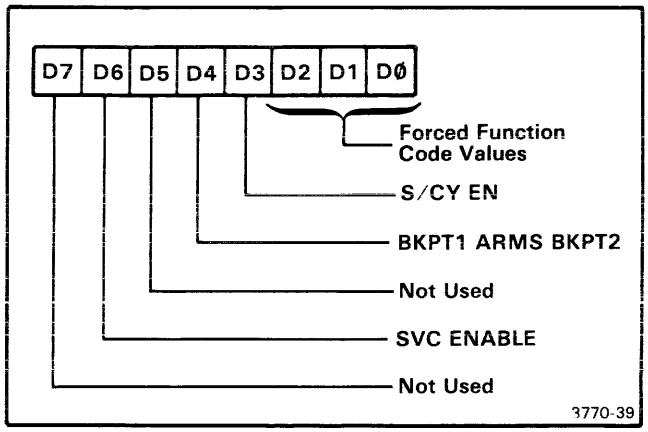


Fig. 4-6. AUX Control Port.

Table 4-1
Emulation Mode Encoding

D6	D5	Function
L	L	Mode 0
L	H	Mode 1
H	H	Mode 2

Table 4-2
Forced Function Code Encoding

Forced Function Codes			Memory Space Accessed
FFC2(D2)	FFC1(D1)	FFC0(D0)	
L	L	L	Not Used
L	L	H	User Data
L	H	L	User Code
L	H	H	Not Used
H	L	L	Not Used
H	L	H	Supervisor Data
H	H	L	Supervisor Code
H	H	H	Interrupt Acknowledge

AUX Control Port (8E)

The AUX Control Port is essentially an extension of the EMU Control Port. As shown in Fig. 4-6, the AUX Control Port contains the following information:

- D0–D2—Forced Function Code values. These bits are selected, as shown in Table 4-2, to be used by the probe during UGET and UPUT operations. This allows the prototype to access the separate memory spaces of the 68000.
- D3—S/CY EN. This bit is asserted high to single-step the 68000.
- D4—BKPT1 ARMS BKPT2. When this bit is asserted high, breakpoint 1 must occur before breakpoint 2 can be asserted.
- D6—SVC ENABLE. This bit is asserted high to enable the 68000 microprocessor to detect SVCs (service calls).

Command Port

The development system loads the Command Port with a command that tells the 68000 microprocessor to perform one subroutine located in the Dump and Restore PROM. Figure 4-7 illustrates the contents of the Command Port. Table 4-3 lists the Command encoding of bits D1–D5.

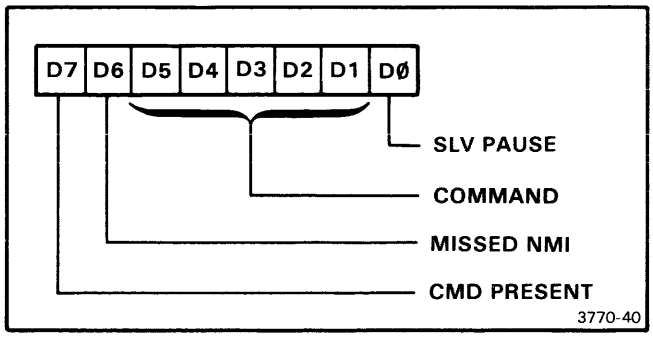


Fig. 4-7. Command Port.

NOTE

The CMD PRESENT bit (D7) is also written to by the 68000. After completing execution of a command, the 68000 clears the CMD PRESENT bit.

Refer to the circuit description of the Command Port, later in this section, for more information.

Table 4-3
Command Encoding

D5	D4	D3	D2	D1	Command
L	L	L	L	L	RUNUSER (Return to user program)
L	L	L	L	H	Register Dump
L	L	L	H	L	Register Restore
L	L	L	H	H	UPUT
L	L	H	L	L	UGET
L	L	H	L	H	Readback check
L	L	H	H	L	Execute from Dump and Restore RAM
L	L	H	H	H	Reserved for future use
X	H	X	X	X	Reserved for future use[a]
H	X	X	X	X	Reserved for future use[a]

[a] **X = Don't care.**

Run/Sequence Control

The Run/Sequence Control logic is the interpreter between the Emulator Processor and the Status Ports (EMU Status and AUX Status). Several control lines bring 68000 microprocessor status information to Run/Sequence Control from various parts of the Emulator Processor. The Run/Sequence Control circuitry converts the control signals into status signals, which are then fed to the Status Ports.

Run/Sequence Control logic is also the interpreter between the Control Ports (EMU Control and AUX Control) and the Emulator Processor. Run/Sequence Control receives control signals from the Control Ports. Run/Sequence Control logic processes these signals into different control signals needed to operate the Emulator Processor. The processed signals are then driven to the various sections of the Emulator Processor to provide proper timing and control.

Run/Sequence Control logic also determines whether the Emulator Processor is to execute a user program or a Dump and Restore subroutine.

I/O And RAM Access Control

The I/O and RAM Access Control logic decodes the development system's address information into control signals that allow the development system to access the following:

- Breakpoint RAM.
- Shared Communication RAM.
- UMAP/Write Protect RAMs.
- EMU Status Port.
- AUX Status Port.
- EMU Control Port.
- AUX Control Port.

RAM

The 68000 Emulator Processor uses three different blocks of RAM: Breakpoint, Shared Communication, and UMAP/Write Protect. The I/O and RAM Access Control logic determine which RAM is accessed by the 2650. The following paragraphs describe the general nature of these RAM. For more information on how the RAMs are accessed and utilized, refer to the "Development System/Emulator Processor Communication" and "Microprocessor/Emulator Processor Communication" discussions, later in this section.

Breakpoint RAM

The 68000 Emulator Processor cannot use the breakpoint circuitry on the development system's Emulator Controller board. Therefore, a RAM-based breakpoint comparator is incorporated into the Emulator Processor's circuitry. This breakpoint comparator consists of four 256 x 4-bit RAMs located on EMU 2.

As shown in Table 4-4, a portion of the 2650's address range (8000–83FF) is designated for use by the four Breakpoint RAMs. Table 4-5 lists the addresses used by each RAM device. When the 68000 microprocessor is not running your programs, the 2650 can program the breakpoint RAMs with an address at which a breakpoint (BKPT) or Service Call (SVC) is to occur and the breakpoint type (BKPT 1, BKPT 2, or BKPT 3).

Table 4-4
Emulator Processor RAM Partitioning

2650 Address Space Allocation	68000 Emulator Processor RAM
8000–82FF	Breakpoint RAM
8300–83DF	Not Used
83E0–83FF	Breakpoint RAM
8400–9FFF	Not Used[a]
A000–A7FF	Shared Communication RAM
A800–BFFF	Not Used[b]
C000–FFFF	UMAP/Write Protect RAM

[a] **Contains Breakpoint RAM images.**

[b] **Contains Shared Communication RAM images.**

The 68000 microprocessor's address lines and some control lines are also divided into four parts, one for each BKPT RAM (see Table 4-6). While your programs are running, the 68000 microprocessor's address and control lines are presented to and monitored by the BKPT RAMs. When an address presented to the BKPT RAMs equals the address previously loaded by the 2650, the appropriate BKPT or SVC occurs by way of the BKPT RAM data output lines. Table 4-7 show the BKPT associated with each data line.

Table 4-6
Breakpoint RAM Partitioning

2650 Address Space	Breakpoint RAM Circuit Number	68000 Microprocessor Address and Control Lines
8000–80FF	U3050	A7–A0
8100–81FF	U3070	A15–A8
8200–82FF	U3080	A23–A16
83E0–83FF	U3090	R/W, B/W, FC2, FC1, and FC0

Table 4-5
2650 RAM Access Bit Encoding

2650 Address Lines[a]									
A15	A14	A13	A12	A11	A10	A9	A8	A7–A0	Emulator Processor RAM Accessed
1	0	0	0	0	0	0	0	[b]	BKPT RAM (U3050)
1	0	0	0	0	0	0	1	[b]	BKPT RAM (U3070)
1	0	0	0	0	0	1	0	[b]	BKPT RAM (U3080)
1	0	0	0	0	0	1	1	[b]	BKPT RAM (U3090)
1	0	1	0	0	[b]				Shared Communication RAM
1	1	0	0	[b]					UMAP/Write Protect RAM (User Code)
1	1	0	1	[b]					UMAP/Write Protect RAM (User Data)
1	1	1	0	[b]					UMAP/Write Protect RAM (Supervisor Code)
1	1	1	1	[b]					UMAP/Write Protect RAM (Supervisor Data)

[a] **A "1" indicates that the address line is asserted. A "0" indicates that the address line is deasserted.**

[b] **Binary address that is presented directly to the RAMs.**

Table 4-7
Breakpoint RAM Data Out

Data Lines	Description
D0(L)	BKPT 1
D1(L)	BKPT 2
D2(L)	BKPT 3
D3(L)	SVC

Shared Communication RAM

The Shared Communication RAM serves as a buffer memory for data transfers between the 2650 and the 68000 microprocessor. A portion of the 2650's address space (A000–A7FF) and a portion of the 68000 microprocessor's address space (0800–0FFF) are used to access the Shared Communication RAM.

Table 4-8 is a memory map of the Shared Communication RAM. Refer to Table 4-8 as you read the following discussion.

Table 4-8
Shared Communication RAM Memory Map

		68000 Microprocessor	
2650 Address Space	Shared Communication RAM Contents	Address Space	Registers
A000–A003	Register Save Area	0800–0803	D0
A004–A007		0804–0807	D1
A008–A00B		0808–080B	D2
A00C–A00F		080C–080F	D3
A010–A013		0810–0813	D4
A014–A017		0814–0817	D5
A018–A01B		0818–081B	D6
A01C–A01F		081C–081F	D7
A020–A023		0920–0823	A0
A024–A027		0924–0827	A1
A028–A02B		0928–082B	A2
A02C–A02F		092C–082F	A3
A030–A033		0930–0833	A4
A034–A037		0934–0837	A5
A038–A03B		0938–083B	A6
A03C–A03F	Supervisor Stack Pointer	083C–083F	
A040–A043	User Stack Pointer	0840–0843	
A044–A045	Status Register	0844–0845	
A046–A047	PC Next (High)	0846–0847	
A048–A049	PC Next (Low)	0848–0849	
A04A–A04B	NMI Missed (Flag)	084A–084B	
A04C–A04F	Prototype Address	084C–084F	
A050–A051	Byte Count	0850–0851	
A052–A053	Byte/Word	0852–0853	
A054–A055	Command Completion Status	0854–0855	
A056–A059	Error Address	0856–0859	
A05A–A7F5	Buffer Block	085A–0FF5	
A7F6–A7F7	PROM Stack	0FF6–0FF7	
A7F8–A7FF	Interrupt Trapstack	0FF8–0FFF	

The Shared Communication RAM is used for the following major data transfer operations:

Register Dump. The 68000 microprocessor loads its register values into the Shared Communication RAM's Register Save, Supervisor Stack Pointer, User Stack Pointer, Status Register, and PC Next areas. The 2650 then copies these registers to A000–A049 at the system memory's RSAVE area. The register values are then displayed on your development system terminal. When the command finishes executing, the 68000 loads the Command Completion Status area and clears the Command Port.

Register Restore. The inverse of Register Dump: the 2650 loads the Shared Communication RAM with register values to be used by the 68000. The 68000 copies these values into its registers for use when running user programs. When the command finishes executing, the 68000 loads the Command Completion Status area and clears the Command Port.

UGET. The 68000 transfers a block of data from the prototype memory to the Shared Communication RAM's Buffer Block area. The block of data to be transferred is defined within the Shared Communication RAM's Prototype Address, Byte Count, and Byte/Word areas. The Prototype Address area contains the transferring block's starting address. The Byte Count area contains the number of bytes to be transferred. The Byte/Word area determines whether the transferring block is byte- or word-oriented. Using these parameters, the 2650 then transfers the block of data from the Buffer Block area into the development system's memory. When the command finishes executing, the 68000 loads the Command Completion Status area and clears the Command Port.

UPUT. The inverse of UGET: a block of memory from the development system is transferred to prototype memory.

Starting the Emulator Processor. The 68000 builds a stack in the Shared Communication RAM's Interrupt Trapstack. The Trapstack consists of PC Next and Status Register values based on the Supervisor Stack Pointer value. Upon executing an RTE instruction, the 68000 unstacks from the Trapstack and begins executing a user program at the unstacked PC Next with the correct Status Register. For more information on starting the Emulator Processor, refer to the discussion "A Typical Emulation Cycle," later in this section.

Stopping the Emulator Processor. The hardware on the Emulator Processor catches the PC Next and Status Register values and loads them into the Shared Communication RAM's Trapstack area. The 68000 microprocessor then moves values from the Trapstack area to the PC Next and Status Register areas, respectively. The 68000 then loads the Command Completion Status area (to indicate that command execution has completed) and clears the Command Port.

UMAP And Write Protect RAM

The 2650 controls memory mapping between Program Memory and prototype memory, through a RAM-based map/write protect comparator incorporated into the Emulator Processor's circuitry.

The UMAP/Write Protect comparator consists of eight 4K x 1-bit RAMs located on EMU 2. Table 4-9 shows how the eight RAMs are used. A portion of the 2650's address range, C000–FFFF, is divided into four parts. Each part is designated for use by two of the eight UMAP/Write Protect RAMs. When the 68000 microprocessor is not running a user program, the 2650 can program the UMAP/Write Protect RAMs.

The UMAP/Write Protect RAMs are programmed and used in the same way as the Breakpoint RAMs (discussed earlier in this section), except for the use of different parameters. The parameters used by the UMAP/Write Protect RAMs are listed in Tables 4-10 and 4-11.

For more information, refer to the circuit description entitled 'UMAP/Write Protect RAM' later in this section.

Dump and Restore PROM

The Dump and Restore (D/R) PROM contains 68000 microprocessor subroutines. When an Emulator Processor command is present in the Command Port, the 68000 jumps to the address of the appropriate subroutine in the D/R PROM. Each subroutine provides the means by which the 68000 can execute the command contained in the Command Port.

Table 4-9
UMAP/Write Protect RAM Partitioning

2650 Address Space	Memory Space Accessed	Circuit Numbers	RAM Function
C000–CFFF	User Data	U3010	Mapping
		U4010	Write Protect
D000–DFFF	User Code	U3020	Mapping
		U4020	Write Protect
E000–EFFF	Supervisor Data	U3030	Mapping
		U4030	Write Protect
F000–FFFF	Supervisor Code	U3040	Mapping
		U4040	Write Protect

Table 4-10
UMAP/Write Protect RAM Data Out

Data Lines[a]		Description	
D1	D0	Write Protect	Map to:
0	0	Yes	Prototype Memory
0	1	Yes	Program Memory
1	0	No	Prototype Memory
1	1	No	Program Memory

[a] A "1" indicates that the data line is asserted.
A "0" indicates that the data line is deasserted.

Table 4-11
Addresses Presented to the UMAP/Write Protect RAMs

2650 Address Lines	68000 Microprocessor Address Lines
A13	FC2
A12	FC1
A11	A23
A10	A22
A9	A21
A8	A20
A7	A15
A6	A14
A5	A13
A4	A12
A3	A19
A2	A18
A1	A17
A0	A16

Emulator Processor Operation Support

The following paragraphs describe the four main operations supported by the 68000 Emulator Processor:

- Communications between the development system and the Emulator Processor.
- Communications between the 68000 microprocessor and the Emulator Processor.
- Communications between the 68000 microprocessor and the development system.
- Communications between the Emulator Processor and the Top Plane Interconnect Bus.

Development System/Emulator Processor Communication

When the development system communicates with the Emulator Processor, buffers 1 and 2 (illustrated in Fig. 4-2) are switched on. and all other buffers are switched off. This allows the development system to access the RAMs (via the Shared Address bus and Shared Data bus). After the development system has accessed the RAMs, it writes a command to the Command Port. Buffers 1 and 2 are switched off; buffers 4 and 5 are switched on. This gives control of the Emulator Processor's Shared Address and Shared Data Buses to the 68000 microprocessor.

While the 68000 is communicating with the Emulator Processor, the development system monitors the Status Ports and Command Port to see if the 68000 has stopped running or finished executing a command. Buffers 3 and 6 are switched on; the development system and 68000 monitor the Command Port at the same time. This lets the development system know when the 68000 has finished executing the command, and also lets the 68000 know when a command has been issued by the development system.

The development system also provides control information to the 68000 microprocessor via the Control Ports.

Microprocessor/Emulator Processor Communication

The development system selects the 68000 via Run/Sequence Control. When the 68000 has been instructed to run, buffers 3 and 6 are the only buffers switched on. The 68000 reads a command from the Command Port via buffer 6; the development system monitors the Command Port via buffer 3. With a command to execute (and the D/R PROM providing the instructions), buffers 4 and 5 are switched on, qualified by a read or write. This allows the 68000 to access the RAMs and to read and/or write address/data according to the command received. When the 68000 has completed the instructions necessary to execute the command, it writes data to the Command Port, indicating that command execution is complete. This allows the development system to take control.

Microprocessor/Development System Communication

The 68000 and the development system communicate with each other directly when the Emulator Processor is instructed to execute your program. To accomplish this, buffers 1 and 4 are switched on in the direction of the development system, and buffers 2 and 5 are switched on, qualified by a read or write. Buffers 3 and 6 are switched off.

Emulator Processor/Top Plane Communication

The Top Plane Interconnect Bus has access to all information presented to the Shared Address, Shared Data, and Control lines.

CIRCUIT DESCRIPTIONS

The following circuit descriptions are divided into function blocks that correspond to the grey-tint overlays on the schematics. A block diagram of the 68000 Emulator Processor is illustrated in Fig. 4-2, earlier in this section. Refer to Fig. 4-2 and the schematic diagrams as you read the following text.

Emulator Board 1 (EMU 1)

Data Buffers 

The Data buffers isolate the System Data Bus and the Shared Data Bus. When D TO SD(L) is asserted, System Data Bus information (D0(L)–D15(L)) is enabled to the Shared Data Bus lines (SD0(L)–SD15(L)) via U6100 and U6120. When SD TO D(L) is asserted, Shared Data Bus information is enabled to the System Data Bus lines, via U6090 and U6110.

Address Buffers 

The Address buffers isolate the System Address Bus and the Shared Address Bus. U6060 and U6080 are enabled by A TO SA(L) low and allow System Address Bus information (A0(L)–A15(L)) to the Shared Address Bus lines (SA0–SA15(L)). The remaining address buffers (U6050, U6070A, U6070B, and U6130) control the information flow of the Shared Address Bus to the System Address Bus. U6050 and U6070B control address lines 0–11 and are enabled when RUNNING(L) is low (the 68000 microprocessor is executing code). U6070A and U6130 control address lines 12–23 and are enabled by a low output from U5120C.

Upper Address Enable 

The output of U5120C enables or disables U6070A and U6130, which are the buffer devices for SA12(H)–SA23(H) and A12(H)–A23(H).

When RUNNING(L) is low (68000 is executing a program) and MACAVAL(L) is high (the MAC board is not installed or not operating), U5120C's output is low, enabling U6070A and U6130.

When MACAVAL(L) is low, the output of U5120C is high, disabling U6070A and U6130. When MACAVAL(L) is asserted, the MAC board is installed in your development system and is operating. When the MAC board is operating it will relocate and drive address lines A12(H)–A23(H). When the 68000 is not executing a program (RUNNING(L) high), U5120C's output is also driven high, disabling U6070A and U6130.

Internal Address Latches 

The Internal Address Latches consist of U4180, U4190, and U4200. Notice that the latch enable lines of these devices (pin 11) are all connected to the output of U2180. When J-K flip-flop U2180 is low, U4180, U4190, and U4200 are latched. When the output of U2180 is high, the Internal Address Latches function as buffers. Refer to Fig. 4-8 for the timing required at U2180 to open and close these latches.

The output enable line of U4200 (pin 1) is always asserted. The output enable lines of U4180 and U4190 are only asserted when IA TO SA(L) is low.

Internal Data Bus Latches 

The Internal Data Bus Latches (U4140 and U4170) latch data from the 68000 (ID0(H)–ID15(H)) to the Shared Data Bus.

ID TO SD(L) and DATA LAT EN(H) determine when the Internal Data Bus is driven to the Shared Data Bus. ID TO SD(L) low enables U4140 and U4170's output to the Shared Data Bus. When DATA LAT EN(H) is deasserted, the Internal Data Bus information is latched by U4140 and U4170. For information on when ID TO SD(L) and DATA LAT EN(H) are asserted or deasserted, refer to the Internal Bus Latch Control function block description later in this section.

68000 Read Buffers 

During the 68000's read cycles, U4150 and U4160 buffer SD0(H)–SD15(H) (from the Shared Data Bus) to ID0(H)–ID15(H) (the Internal Data Bus). When SD TO ID(L) is low, these buffers are enabled. For more information on the SD TO ID(L) signal, see the heading Internal Bus Latch Control later in this section.

Internal Bus Latch Control 

There are five internal bus latch control signals generated here. Let's look at the generation and function of each of these signals.

DATA LAT EN(H). The DATA LAT EN(H) signal determines whether Internal Data Bus information is latched to the Shared Data Bus. DATA LAT EN(H) is asserted via U5050D, which is controlled by BB CPUCLK(H) and the $\overline{S}$-$\overline{R}$ Latch configuration, (U6040C and U6040D). $\overline{R}$ is represented by pin 9 of U6040C, $\overline{S}$ by pin 12 of U6040D, and Q by pin 11 of U6040D. Refer to Fig. 4-9 for R-S Latch configuration and DATA LAT EN(H) assertion.

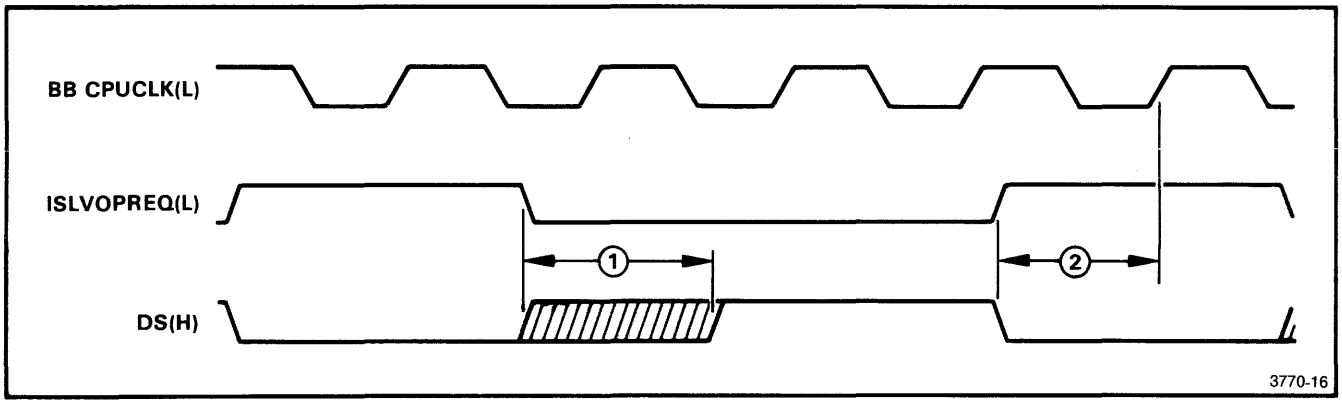


Fig. 4-8. Internal Address Latches enable timing.

1. ISLVOPREQ(L), low, and DS(H), high, set U2180's output low (latches are closed).
2. When DS(H) goes low, the next rising clock edge of BB CPUCLK(L) will reset 2180's output high (latches are open).

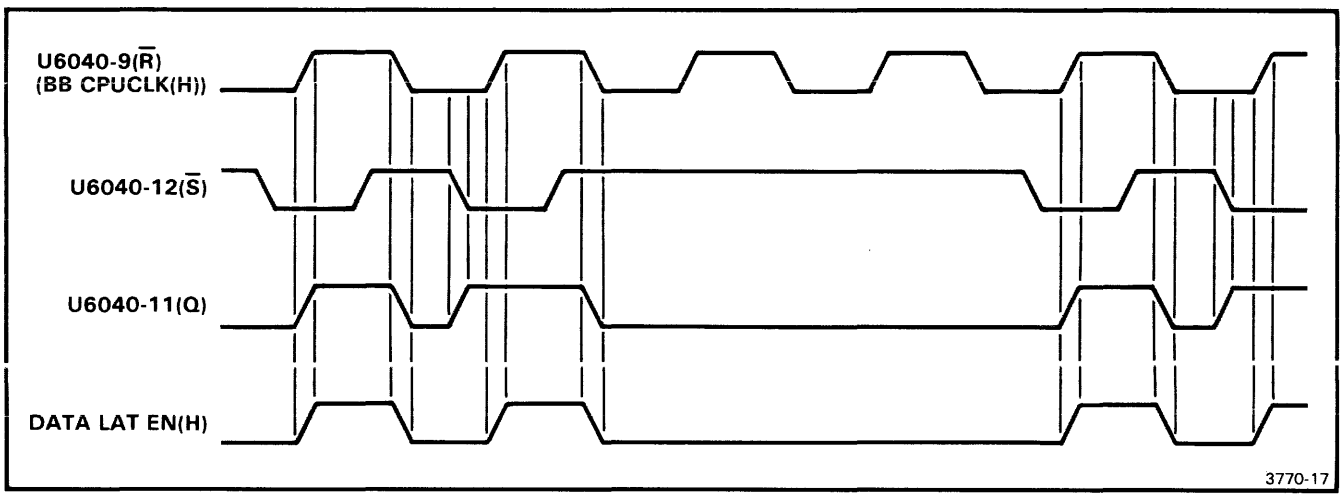


Fig. 4-9. DATA LAT EN(H) timing.

ID TO(L)/FROM(H). ID TO(L)/FROM(H) is driven to the Buffer board's function block, Probe To EMU A/D Buffers (discussed later in this section).

First, let's look at how ID TO(L)/FROM(H) is driven low to indicate that data is enabled to the 68000 microprocessor. At U5050A, a read is requested when BB R(H)/W(L) and U4050B's output are both high. U4050B's output is high when UG/UP+RUNNING(H) is deasserted or U5080A's output is low. U5080A's output is low when the 68000 is executing a program (RUNNING(L) low). This program execution will not be out of the prototype memory as indicated by U4090B's low output (discussed later in this section under the heading, Isolation Buffer Control).

Now let's look at how ID TO(L)/FROM(H) is driven high to indicate that data is enabled from the 68000 or the prototype circuit. At U5050A a write is requested when BB R(H)/W(L) is low or when U4050B's output is low. For U4050B's output to be low, UG/UP+RUNNING(H) and the output of U5080A must be high. U5080A's output is high when memory is mapped to or from the prototype circuit, as indicated by a high from U4090B (discussed later in this section).

IA TO SA(L). IA TO SA(L) controls the Internal Address Latch's output-enable lines.

IA TO SA(L) is asserted when the output of U5030D is low. U5030D becomes low when the 68000 microprocessor is

executing a program (RUNNING(H) high), or U5030A's output is high. U5030A's output is high when all the following signals are low:

- UG/UP+RUNNING(H) (from the Buffer board)
- output of U5120B
- output of U5060D

U5120B's and U5060D's outputs are low when all the following signals are deasserted:

- BA CMD=0(H) (There is no command present.)
- PROM(L) (The 68000 is not accessing the D/R PROM.)
- D/R CMDRD(L) (The 68000 is not reading the Command Port.)

ID TO SD(L). ID TO SD(L) is the output-enable signal for the Internal Data Bus Latches. When ID TO(L)/FROM(H) is high and IA TO SA(L) is low, U5040D asserts ID TO SD(L).

SD TO ID(L). SD TO ID(L) is the output-enable signal for the 68000 Read Buffers. When both ID TO(L)/FROM(H) and IA TO SA(L) are low, U5040A drives SD TO ID(L) low.

Isolation Buffer Control 

Control signals for the Isolation Buffers are generated here.

When A TO SA(L) is asserted, A0(L)–A15(L) are enabled to SA0(H)–SA15(H). A TO SA(L) is asserted by U5100B when there is no command in the Command Port (BA CMD=0(H) high) and the 68000 is not executing any programs (RUNNING(L) high).

When D TO SD(L) and SD TO D(L) are asserted, they enable the System Data bus to the Shared Data bus and the Shared Data bus to the System Data bus, respectively. U4110 and U4120 decode running and read/write status lines to assert D TO SD(L) or SD TO D(L). The only other signal decoding performed to generate these two data control lines is by U4090B and U4090C. U4090B's high output indicates that the Emulator Processor is operating in Mode 0 (MODE)(H) high) or in Mode 1 with memory mapped to Program Memory (MODE1(H) asserted and UMAP(H) deasserted at U4090C).

Function Code Buffer 

The Function Code Buffer consists of U2040. U2040 is always enabled via pins 1 and 19. Therefore, BA FC0(H)–BA FC2(H) are passed from the Buffer board to EMU 1 and EMU 2 (via BC FC0(H)–BC FC2(H)).

UMAP Valid Generator 

The UMAP Valid Generator issues UMAP EN(H) to the UMAP/Write Protect RAM circuit block, discussed later in this section.

UMAP EN(H) is asserted to indicate that the UMAP/Write Protect RAM outputs are valid. UMAP EN(H) becomes high when U6020B is presented with (1) a high from U5100C's output and (2) a positive clock edge from BB CPUCLK(H). U5100C's output is high when the 68000 is executing a program (RUNNING(L) asserted), and a write operation has been requested, or when DS(H) is asserted (U3030A's output is low).

NOTE

During a write DS(H) is asserted late. Therefore, U5100C's output is high only when RUNNING(L) is asserted and a write request has been issued.

UMAP EN(H) is reset low when U5040C's output is low. This low output at U5040C is present when BA R(L)/W(H) is low (indicating a read) and IOPREQ(H) is deasserted (indicating that no operation is requested).

TTA Strobe Generator 

TOPSTRBDATA(L) is a strobe that is sent to the TTA option to strobe in data from the Shared Data Bus. The TTA requires that TOPSTRBDATA(L) be asserted to clock in valid data before the trailing edge of SLVOPREQ(L). Notice that TOPSTRBDATA(L) is generated at U4090D using SLVOPREQ(L) and BB CLK+25(H). (Refer to foldout sheet 26, located in the Diagrams section of this manual.) For more information on the TTA's use of TOPSTRBDATA(L), refer to the TTA Service Manual.

System Interface And Control 

The System Interface and Control block consists of control signals for your development system and TTA option. Because so many of these signals act upon one another, we'll look at just a few of the more important signals individually. As you read the following signal descriptions, refer to the timing diagrams on foldout sheet 26, located in the rear of the Diagrams section of this manual.

WRP(L) is the write pulse signal to the development system. This signal is a delayed data strobe from the 68000. The delay allows IA0(H) to be generated, setting up Prograr Memory before the write pulse is issued. (The 68000 does not have an A0 signal, so A0 is generated by the Emulator Processor using the 68000 data strobes.)

U2030 decodes the data strobes (UDS(L) and LDS(L)) to assert WD ACCESS(L), IBYTE(H)/WORD(L), and SWAP(L). Notice that if the cycle is a read cycle, then the Emulator Processor defaults to a word read (16-bits). This default condition allows a longer read access time. (For example, during a read, WD ACCESS, IBYTE(H)/WORD(L), and SWAP(L) are generated by BB R(H)/W(L) and BA R(L)/W(H), not by the data strobes.)

SLV OPREQ(L) is asserted at U6020A on the first positive clock edge of BB CPUCLK(H) after DS(H) has been assert-

ed. SLV OPREQ(L) is deasserted on the first positive clock edge of BB CLK+25(H) after DS(H) has been deasserted. In this way, ISLVOPREQ(L)'s timing to the TTA is assured.

MODE0 Clock 

This circuit block generates 8MHZ and MODE0CLK(H). A 16 MHz crystal (Y3228) and associated oscillator circuitry generate a 16 MHz clock pulse to pin 4 of U2180A. U2180A divides the 16 MHz pulse by two, thereby generating 8MHZ. The 8MHZ clock signal is qualified at U2060C by MODE0(L) low. MODE0CLK(H) is then driven to the Buffer board's Clock Select circuitry.

Break Interrupt Control 

INTMACHEN(H) enables the Interrupt Machine circuitry, which is located on the Control board. Let's look at when INTMACHEN(H) is asserted.

U4020C, U4050D, and U5030C will drive U2140B's pin 11 high at the first Supervisor or User Code memory space access after the 68000 starts executing out of Program Memory or prototype memory. This is done when BC FC0(H) is low, BC FC1(H) is high, and RUNNING(L) is low. U2140B is then clocked by the next falling edge of BA AS(L), driving pin 9 high (INTMACHEN(H) asserted). This assures that at least one instruction has been executed by the 68000 before the Emulator Processor issues an interrupt (via the State Machine circuit on the Control board).

INTMACHEN(H) is deasserted when U2140B is cleared by RUNNING(H) low (indicating that the 68000 has stopped executing a program).

NOTE

MODE0 BKEN(H) is for factory use only and does not effect the operation of the 68000 Emulator Processor.

RUN Control 

The RUN Control block generates two control signals: SLV PAUSE(H) and RUN(L). SLV PAUSE(H) is asserted to the Command Port, indicating that the development system is accessing the Shared Bus. SLV PAUSE(H) low indicates to the Command Port that the 68000 microprocessor can access the Shared Bus. RUN(L) is driven low to the development system to indicate that the 68000 is executing out of Program Memory or prototype memory. Because these two signals work together, we need to look at how both of them are asserted and deasserted.

U6030B's clock (pin 12) and pin 9 of U5090C monitor SLVPSE(L) from the development system for a high condition. When SLVPSE(L) goes high, U5090C deasserts SLV PAUSE(H) and clocks U6030B, presenting a low to pin 2 of U3040A. This low at pin 2 of U3040A drives pin 1 of U2060B low, thereby asserting RUN(L). Notice that RUNNING(L) is presented to pin 13 of U3040A also.

Before the 68000 actually starts executing a program (RUNNING(L) high), it must first execute a RTE instruction. Therefore, U6030B ensures that RUN(L) is asserted via U3040A before the development system can issue a HALT (absence of RUN(L) longer then 26 us after SLVPSE(L) is deasserted).

When RUNNING(L) and RUNNING(H) are asserted, two transitions occur to maintain RUN(L)'s low state. RUNNING(H) is presented to U3030, causing U6030B to clear. This drives pin 2 of U3040A high, which would deassert RUN(L). However, at the same time, RUNNING(L) low is presented to pin 13 of U3040A, thus maintaining the assertion of RUN(L).

NOTE

If CMD PRESENT(L) is deasserted (indicating that there is no command in the Command Port) U6030B will remain cleared, keeping a high at pin 2 of U3040A. Also, because RUNNING(L) cannot be asserted to pin 13 of U3040A while there is no command, RUN(L) is held deasserted. A HALT is issued 26 us after SLV PAUSE(H) is deasserted. This indicates a major error, and the Command Port (along with the development system's access to the Command Port) should be checked closely for proper operation.

Factory Test NMI Control 

This block of circuitry is for factory use only.

RESET/HALT Control 

U2160A and U2160B hold BRDHALT(L) and RESET(L) low, respectively, as long as DLYD ACTIVE(H) is asserted.

HALTED(H) is asserted by U5090B to indicate that BRDHALT(L) is asserted and that DLYD ACTIVE(H) is deasserted.

RESET SEQ EN(H) is asserted when U6030A is clocked by DLYD ACTIVE(H)'s rising edge. RESET SEQ EN(H) is deasserted when U6030A is cleared by UNSTACKING(L) low (indicating that the first program instruction has been executed by the 68000 microprocessor).

User RUN Control 

User RUN Control issues control signals that indicate whether the 68000 is executing out of Program Memory or prototype memory. The control signals RUNNING(H) and RUNNING(L) are referred to in this discussion as RUNNING.

RUNNING is asserted by 6160D whenever SETRUN(L) is low. (For SETRUN(L) information, refer to the Transfer Out Of D/R Control discussion later in this section.) RUNNING remains asserted until RESET RUN(L) is asserted.

Let's look at what conditions will drive U1220B's output:

U1220B's output is high when all three inputs are low, that is, when all of the following conditions are true:

- DLYD ACTIVE(H) is asserted.
- U5090A's output is low. This is achieved when RESET RUN(L) is deasserted (from the Transfer Into D/R Control circuit block, discussed later in this section) or IOPREQ(H) is asserted.
- U1220A's output is high. This requires that CLKFAIL(H) be deasserted and that input pin 11 of U1220A be low (see the following note).

NOTE

The state of U1220A's pin 11 depends on the position selected for P1080. If P1080 is in its normal (1—2) position, HALTED(H) controls the state of pin 11 directly. However, if P1080 is in its optional (2–3) position, HALTED(H) will control the state of U1220A's pin 11 only during Mode 0 operation (MODE0(L) low). In Mode 1 or 2 (MODE0(L) high), U2060B is disabled, and RP6182-10 holds pin 11 low regardless of HALTED(H)'s state.

U1220B's output is low when any of its three inputs are high (indicating that the Emulator Processor has stopped executing a program). U1220B's inputs are high (and its output is therefore low) when any of the following conditions are true:

- DLYD ACTIVE(H) is deasserted.
- U5090A's output is high. This is true when RESET RUN(L) is asserted and IOPREQ(H) is deasserted.
- U1220A's output is low. This requires that CLKFAIL(H) be asserted, or that input pin 11 of U1220A be high (see the previous note).

F.P. HOLD Interface 

This circuit is for factory use only.

AUTO Vector Request 

An auto vector is requested of the 68000 via the assertion of VPA(L). When BC AS(L) is asserted and BKINTA(L) is asserted (indicating that the Emulator Processor has issued and acknowledged a break interrupt), U5090D asserts VPA(L).

D/R PROM 

The two Dump/Restore PROM devices are enabled when BA R(H)/W(L) is high and the output of U3090A is high (output signal PROM(L) is asserted).

Internal Address lines IA1(H)–IA10(H) are presented to the D/R PROM devices from the 68000 microprocessor. ID0(H)–ID15(H) are the lines used to carry D/R instruction code to the 68000. For more information about the D/R PROM, refer to the Dump And Restore PROM discussion, earlier in this section.

UGET/UPUT Decode 

UGET(H) and UPUT(H) indicate that the D/R PROM is issuing UGET or UPUT instruction code, respectively, to the 68000. Let's look at the process involved to assert UGET(H) or UPUT(H).

U5170 is enabled for operation in the same way as the D/R PROM devices (discussed earlier in this section). The enable occurs when BA R(H)/W(L) is asserted and the output of U3090A is high. U3090A's output is high when all of the following are true:

- UG/UP+RUNNING(H) is asserted.
- IA11(H) and IA12(H) are deasserted (see Table 4-12).
- D/R EN(L) is asserted.
- BC AS(L) is asserted.

While U5170 is enabled, it monitors the same Internal Address lines as do the D/R PROM devices. When these address lines are equal to the address of a UGET or UPUT routine, U5170's pin 9 or 10 is driven low (indicating that a UGET or UPUT routine is being executed by the 68000). Pin 11 of U5170 is low when the Internal Address lines are equal to any D/R routine except UGET or UPUT. These three output lines are driven to U6170.

BC AS(L)'s rising edge clocks U6170's inputs to S-R Latch U6160, asserting UGET(H) during a UGET operation and UPUT(H) during a UPUT operation. (Both UGET(H) and UPUT(H) are reset low when neither operation occurs.) Note that U6170 is cleared (all outputs high) when DLYD ACTIVE(H) is deasserted.

Table 4-12
68000 Memory Address Map

IA12(H)	IA11(H)	Memory Addressed
L	L	D/R PROM
X	H	Shared RAM[a]
H	L	Command Port

[a] **X = Don't care.**

Transfer Out Of D/R Control ◇7◇

The main function of the Transfer Out of D/R Control circuitry is to assert SETRUN(L) when the 68000 has completed executing the RUNUSER set of instructions from the D/R PROM (that is, when the RTE instruction is issued). SETRUN(L) low is used to assert RUNNING(H) in the User RUN Control circuit block.

When the RTE instruction is issued, END D/R(L) is asserted by U5170's Q4 output. END D/R(L) low is presented to U6170F.

U6170F is the first of five D-type flip-flops that are configured as a stack register. The stack register is clocked by BC AS(L), and delays the assertion of SETRUN(L) until the Trapstack in the Shared RAM is unstacked to the 68000. Each of the following steps represent one rising edge of BC AS(L):

1. With END D/R(L) asserted, U6170D is clocked, forcing Q0 high. (A NOP is pre-fetched from the D/R PROM.)
2. U2220C clocks the high, presented by U6170D, changing Q1 to a high. This asserts STUSREGPUL(L), indicating that the Status Register in the Shared Communication RAM is being accessed. Also, UNSTACKING(L) is asserted via U1220C. (The 68000 unstacks the Status Register.)
3. U2220D clocks a high to Q2, maintaining the assertion of UNSTACKING(L). Due to this clocking though, STUSREGPUL(L) is deasserted. (The 68000 unstacks PC Low.)
4. U2220A clocks a high to U2220B, also maintaining UNSTACKING(L) low. (The 68000 unstacks PC High.)
5. U2220B is clocked by BC AS(L)'s rising edge, driving a low to pin 1 of U5120A. When IOPREQ(H) is deasserted at pin 2 of U5120A, SETRUN(L) is asserted. (The RTE routine (unstacking the Trapstack) is complete, with the 68000 ready to read an instruction at the new PC and assert RUNNING.)

Transfer Into D/R Control ◇7◇

The main function of the Transfer Into D/R Control circuitry is to catch the stacking operations performed by the 68000 in response to an Emulator Processor level 7 interrupt (NMI).

NOTE

Recall that RESET RUN(L) low deasserts RUNNING(H) in the User RUN Control circuit block.

To allow the Shared RAM Trapstack Area time to catch the stacking operations, this circuit contains a stack register (U4220) that functions in much the same way as the stack register discussed in the Transfer Out Of D/R Control. The main difference is that RESET RUN(L) deasserts RUNNING(H) first and then enables the D/R PROM.

To start the D/R enable sequence, stack register U4220 is presented a high at D1 and clocked by BC AS(L). The high at D1 is provided by U4050C when PODBKINTA(L) is asserted from the Control board. U3020's output to U4050C is the same as PODBKINTA(L) and is of no concern here unless the device is faulty (U3020 is for factory use).

With U4220's D1 high, pin 11 of U4220 goes low at the next clock pulse, asserting RESET RUN(L). Pin 10 of U4220 goes high causing the stack register to step with each clock pulse from BC AS(L) until Q3 goes high, asserting D/R EN(L) via U3050B. U4220 is cleared when UNSTACKING(L) is asserted at the end of the D/R PROM access.

Notice that U3050B also asserts D/R EN(L) when RESET SEQ EN(H) is asserted from the RESET/HALT Control function block, discussed earlier in this section.

Shared RAM ◇8◇

The Shared RAM circuitry consists of Shared Communication RAM devices (U5190, U5200, U5220, and U5210) and Shared RAM buffers (U6200, U6210, and U6220). First, let's look at the Shared RAM buffers.

The direction control input (pin 1) of these buffers is tied to SHARED R(H)/W(L). While SHARED R(H)/W(L) is high, the buffers, when enabled, read D/R Data lines to the Shared Data lines. While SHARED R(H)/W(L) is low, the buffers, when enabled, write the Shared Data lines to the D/R Data lines. Each of these buffers is enabled differently, depending on whether the 68000 or the development system's 2650 is accessing the Shared Communication RAM. The buffers are enabled as follows:

U6220 is enabled when either the 68000 or the 2650 access the Shared RAM (LCS(L) asserted).

U6210 is enabled when the 2650 accesses the Shared RAM (2650 HCS(L) asserted).

U6200 is enabled when the 68000 accesses the Shared RAM (68000 HCS(L) asserted).

Now let's look at the Shared RAM devices. These RAM devices are all write-enabled at pin 10 by SHARED R(H)/W(L) low. Note that the Shared RAM can be written to by either the 68000 or the 2650. The chip-select signals (HCS(L) and LCS(L)) are provided by the Shared RAM Select function block. HCS(L) low selects U5190 and U5200 (high-order data bits) and LCS(L) low selects U5220 and U5210 (low-order data bits).

Shared RAM Select ◇8◇

The Shared RAM pair is selected by HCS(L) and LCS(L). Also, 68000 HCS is generated to enable Shared RAM buffer, U6200. The way in which these chip-select signals are generated depends on whether the 68000 or the 2650 is accessing Shared RAM. Let's examine both possibilities.

2650 Access. U4080B or U4080C are presented with 2650 LCS(L) or 2650 HCS(L), respectively. As explained later, under the heading EMU RAM Access Decode, only one of these signals can be present at a time.

LCS(L) is driven low when 2650 LCS(L) is asserted. While LCS(L) is low, Shared RAM pair U5220 and U5210 are selected, along with buffer U6220. This gives the 2650 access to the low-order data bits.

HCS(L) functions similarly to LCS(L), except that HCS(L) enables U5190 and U5200, giving the 2650 access to the high-order data bits. Note that buffer U6210 is enabled by 2650 HCS(L) low.

68000 Access. U4080B and U4080C are presented with 68000 LCS(L) and 68000 HCS(L), respectively. These signals are asserted via U4010D and U4010A.

When U5010C's output is high, U4010D and U4010A are ready to assert 68000 LCS(L) and 68000 HCS(L) waiting only for BA LDS(H) and/or BA UDS(H) to be asserted. Notice that when U5010C's output is high, the 68000 has access to the Shared RAM and that BA LDS(H) and BA UDS(H) indicate whether the access is to the low-order bits, high-order bits, or both.

U5010C is driven high when any one of the following conditions are true:

- U5010A's inputs are all high (driving the out low). This indicates that the Trapstack is to be stacked by the 68000.
- UNSTACKING(L) is asserted, indicating that the 68000 is unstacking from the Trapstack.
- U3060C's inputs are all high (driving the output low). This indicates that the 68000 is accessing the Shared RAM, due to D/R PROM instructions.

D/R Interrupt Trapstack Control 

U6190 and U6040A assure that only the Trapstack portion of Shared RAM is accessed during stacking or unstacking operations.

Asynchronous Break Control 

U3010C and U6160B decode BKSTOP(L), BKINTA(H), and DLYD ACTIVE(L) to asynchronously interrupt the 68000 by deasserting ASYNCBK(L). ASYNCBK(L) low is driven to the Control board when the 68000 executes a STOP instruction (BKSTOP(L) asserted). ASYNCBK(L) is reset high when BKINTA(H) and DLYD ACTIVE(L) are high, indicating an interrupt acknowledge.

MAC Board Address Generator 

The MAC Board Address Generator issues A24(H) and A25(H) to the Memory Allocation Controller (MAC) in your development system. These two address lines indicate which memory space the 68000 is accessing. Table 4-13 lists the decoding of these address lines. The exclusive-OR gate U4040A ensures that BC FC1 and BC FC2 indicate a valid memory space and not one of the unused spaces shown back in Table 4-2.

Table 4-13
MAC Board Relocation Decode

A24(H)	A25(H)	Memory Space Allocated
L	L	User Data
L	H	User Code
H	L	Supervisor Data
H	H	Supervisor Code

Command Port 

The Command Port Latch U2080 is accessed for a read or write by either the development system or the 68000 microprocessor.

U2080 is written to via the Shared Data Bus, SD1(H)–SD7(H). While DLYD ACTIVE(H) is asserted, the data written to U2080 is latched to the Q outputs upon a high at pin 11. Notice that when pin 11 is low, the Shared Data lines can change without effecting the Q output lines.

U2050 is an inverting buffer used when the development system reads the Command Port (via D0(L)–D7(L)). U2050 is enabled by 8F RD(L) low from the 2650 I/O Access Decode circuit located on EMU 2.

When D/R CMDRD(L) is low, U2090 is enabled for the 68000 to read the Command Port via ID0(H)–ID7(H).

U3060A and U6010A detect missed NMIs. When an NMI is detected by U3060A and issued to U6010A, U6010A asserts NMI MISSED(H) to the Command Port Buffers. After one of these buffers is read and acknowledged, the Command Port (U2080) is written to, asserting MISSED NMI(H). MISSED NMI(H) high then clears U6010A, and the NMI MISSED(H) signal is deasserted.

Command Port R/W Control 

This circuit determines whether the Command Port is to be accessed by the development system or the 68000 for a read or write operation.

Let's look at how the 68000 accesses the Command Port. When 3080B's inputs are all low, its output is driven high, indicating that the 68000 is not executing a program or performing a UGET or UPUT operation and is requesting a

Command Port access (via IA11(H) and IA12(H)). U3080B's high output is ANDed with BB R(H)/W(L) at U5100A to generate D/R CMDRD(L). The assertion of D/R CMDRD(L) to U2090 enables a 68000 read of the Command Port. U3080B's high output is also ANDed with BA R(L)/W(H) and CMD=0(L) at U3040C. When U3040C's inputs are all high, it outputs a high to U3010A, which clocks the Command Port U2080 for a 68000 write.

A development system write to the Command Port is issued by U3010D and U3010A when 8F WR(L) (from the 2650 I/O Access Decode function block) and CMD=0(L) are asserted.

CMD=0(L) low is issued by U3080A and U4020A when CMD PRESENT(H) and NMI MISSED(H) are deasserted and D/R EN(L) is asserted from the Transfer Into D/R Control circuit, discussed earlier in this section.

Emulator Board 2 (EMU 2)

2650 I/O Access Decode 

The development system's address lines A0–A7 are decoded to produce the port access control signals shown in Table 4-14. These port control signals are qualified by OPREQ(L), MSTRRUN(L), M(L)/IO(H), DLYD ACTIVE(H), and R(H)/W(L).

Address lines A0–A7 represent the binary equivalent of the port that is to be addressed, and are qualified by a read or write operation (see Table 4-15).

EMU RAM Access Decode 

The Emulator Processor's three RAMs (Breakpoint, UMAP/Write Protect, and Shared Communication) each have their own read/write control signals. The EMU RAM Access Decode circuit decodes the development system's control and address lines, to generate these read/write signals.

Table 4-14
Emulator Processor Port Access Control Signals

Control Signals	State	Port Accessed
ADREAD(L)	Low	EMU Status Port (0AD)
ADWRITE(L)	Low	EMU Control Port (0AD)
8E RD(H)	High	AUX Status Port (08E)
8E WR(L)	Low	AUX Control Port (08E)
8F RD(H)	High	Command Port (08F)
8F WR(L)	Low	

This logic also generates 2650 RAMAC(H) and RAMINH(L), which enable the Emulator Processor's RAM and disable the Program Memory in your development system. Lets look at these two memory control signals first.

RAMINH(L) becomes low whenever any one of the following conditions exist:

- 2650 RAMAC(H) becomes asserted. 2650 RAMAC(H) is asserted when U4150A's output is low.
- The 68000 microprocessor is running while the emulator is in Emulation Mode 2.
- The 68000 microprocessor is running while the emulator is in Emulation Mode 1 and memory is mapped to the prototype circuit.

Now let's look at the Emulator Processor RAM read/write control signals. To qualify the individual RAM read/write lines, U3110B is presented with OPREQ(L) low from the development system when all the address and control lines used to generate 2650 RAMAC(H) are valid. While U3110B's output is low, the individual RAM control lines output from this block are selected, as described in the following paragraphs.

The 2650 LCS(L) and 2650 HCS(L) signals are selected by SA0(H) via U3100D and U3100A, respectively. U5160A's high output indicates that the Shared Communication RAM is to be accessed.

Table 4-15
Emulator Processor Port Address

Port Address	Address Lines 7	6	5	4	3	2	1	0	R(H)/ W(L)	Port Accessed
AD	L	H	L	H	L	L	H	L	H L	EMU Status Port EMU Control Port
8E	L	H	H	H	L	L	L	H	H L	EMU Control Port AUX Control Port
8F	L	H	H	H	L	L	L	L	H L	Command Port

The Breakpoint RAM's read and write signals are selected by SA13(H) and SA14(H) at U5160B. BKPT RD(L) is selected when U5160B's output is high and the development system requests a read (BA SYS R(H)/W(L) is high). BKPTW0(L)–BKPTW3(L) are selected by SA8(H) and SA9(H) (see Table 4-16) when U4100D's output is low. U4100D's output becomes low by way of a write (SYS R(H)/W(L) low) and a write pulse (WRP(L) low) from the development system, plus U5160B's high output.

MAPRAMRD(L) or MAPRAMWR(L) is selected when a UMAP/Write Protect RAM access has been requested (U5040C's output is low). MAPRAMRD(L) is asserted when the development system requests a read (BA SYS R(H)/W(L) high). MAPRAMWR(L) is selected when U5120B receives two low inputs.

SHARED R(H)/W(L) is equal to the 68000's read/write signal BB R(H)/W(L) when CMD=0(H) is low. CMD=0(H) low indicates a command is present for the 68000 microprocessor to execute. SHARED R(H)/W(L) is equal to the development system's read/write signal SYS R(H)/W(L) when CMD=0(H) is high. U2080B will output a low for a write cycle when pins 1 and 13 are low, or pin 1 is high and pin 14 is low. A read will be output by U2080B when pin 1 is low and pin 13 is high, or pins 1 and 14 are high.

Table 4-16
Breakpoint RAM Write Decode

SA8(H)	SA9(H)	Signal Asserted
L	L	BKPTW0(L)
L	H	BKPTW1(L)
H	L	BKPTW2(L)
H	H	BKPTW3(L)

STOP Instruction Decode 

The stop instruction signal STOP(L) causes the 68000 to stop (no Address Strobes) until an interrupt occurs.

To assert STOP(L) to the AUX Status Port (U2060, center page), U1120C looks for BC AS(L) to be absent for 100 μs while the Emulator Processor is not RESET, HALTED, or bus-requested (BG(L) or BGACK(L)). This 100 μs delay is derived by the clocking of U2140A, U2140B, and U2130B. If U1120C's output is not driven high to reset the clocking sequence, then U2120B is clocked, asserting STOP(L). When BKCOND(H) is asserted, U3150E is clocked, setting BKSTOP(L) low. At the next address strobe this whole block is reset to start clocking all over again.

NOTE

The Address Strobe (BC AS(L)) is also absent while the 68000 is executing D/R PROM instructions, and the longest instruction that may be executed (Multiply/Divide at 2 MHz) can take as long as 100 μs. Therefore, the 100 μs delay is needed to limit confusion between a stop instruction and D/R PROM instruction execution.

Emulator Break Generator 

U2050 decodes any break condition that occurs, and asserts BKCOND(H). BKCOND(H) is presented to the AUX Status Port.

TTA Break Decode 

When the TTA option requests a break (DBG INT29(L) low), U2150A latches the INT29 to the AUX Status Port.

Jump Acknowledge Generator 

U5030 and U5130A ensure that a JMPACK(L) low will be clocked back to the development system if a Jump Command is issued by the development system (JMPCMD(H) high) while the Emulator Processor is active (DLYD ACTIVE(H) high).

Write Protect Interrupt Generator 

U1130B latches a write protect violation from U1140B to create the write protect interrupt signal, WRPROT INT(L).

Auxiliary Status Latch 

U2060 latches the AUX Status Port's contents until the information is read by the development system. Reading the AUX Status Port resets (clears) all break conditions contained within the port.

U2150B clocks the HAVERUN(H) signal to the EMU Status Port.

BKPT RAM Multiplexers 

The BKPT RAM Multiplexer block contains the Breakpoint RAM multiplexers, U2030 and U1070, which are used by the UMAP/Write Protect RAM. These multiplexers determine whether the development system address lines A0–A7 or the 68000 microprocessor address lines PA0–PA23 are to be presented to the Breakpoint RAM devices. Both sets of address lines are presented to the multiplexers by way of the Shared Address Bus.

The control signal CMD=0(H) selects either the "A" bank or the "B" bank of shared address lines. When CMD=0(H) is asserted, the "A" bank is selected and the development system's address information is presented to the Breakpoint RAM. When CMD=0(H) is deasserted, the "B" bank is selected, and the 68000's address information is presented to the Breakpoint RAM.

Breakpoint RAM 

The Breakpoint RAM devices (U3050, U3070, U3080, and U3090) may be written to or read by the development system.

The development system writes breakpoint data information to each RAM device (one at a time), using BKPTW0(L)–BKPTW3(L) as write-enable signals. The development system, via the BKPT RAM Multiplexers, always presents A0–A7 to these RAM devices.

When BKPT RD(L) is asserted, the development system is requesting to read the existing data in the BKPT RAM. Therefore, U4070 and U4090 are enabled and the data read on SD0(H)–SD3(H) is qualified by SA8(H) and SA9(H), as shown in Table 4-17.

After the development system has loaded the BKPT RAM, the 68000 address lines are presented to the BKPT RAM (via the BKPT RAM Multiplexers). The 68000 address lines are monitored for a True condition (address being monitored equals address previously loaded by the development system), at which time the data information is driven to the BKPT1/0(L)–BKPT3/3(L) and SVC0(L)–SVC3(L) buses.

UMAP/Write Protect RAM 

The UMAP/Write Protect RAM consists of UMAP RAM devices (U3010, U3020, U3030, and U3040) and Write Protect RAM devices (U4010, U4020, U4030, and U4040).

MA0(H)–MA11(H) represent either development system address lines or 68000 microprocessor address lines. Notice that multiplexer U2070 controls MA8(H)–MA11(H) in the same way that MA0(H)–MA7(H) are controlled by the Breakpoint RAM Multiplexers.

The UMAP RAM and Write Protect RAM are selected in pairs. For example, pins 10 of U3040 and U4040 are selected at the same time. U3040 and U4040 address the Supervisor Code memory space. U3030 and U4030 address Supervisor Data, U3020 and 4020 address User Code, and U3010 and U4010 address User Data.

The RAM pair selection is decoded by U2080A and U4050A. U2080A uses CMD=0(H) to select either SA12(H) and SA13(H), or BC FC1(H) and BC FC2(H). When CMD=0(H) is high, the development system has control of the bus, using SA12(H) and SA13(H). When CMD=0(H) is low, the 68000 is running, and BC FC1(H) and BC FC2(H) are being used. For decoding of RAM pair selection, see Table 4-18.

The UMAP/Write Protect RAM devices are write-enabled at pin 8 when MAPRAMWR(L) from the 2650 RAM Access Decode function block is asserted. This allows SD0(H) and SD1(H) to be written to pin 11 of the RAM devices selected. As shown in Table 4-19, SD0(H) and SD1(H) indicate where the 4K block, represented by MA0(H)–MA11(H), is to be mapped and whether the block is write-protected.

Table 4-17
BKPT Read Decode

RAM Select		RAM Contents				
SA8(H)	SA9(H)	SD0	SD1	SD2	SD3	RAM Device
L	L	BKPT1/0	BKPT2/0	BKPT3/0	SVC0	U3050
H	L	BKPT1/1	BKPT2/1	BKPT3/1	SVC1	U3070
L	H	BKPT1/2	BKPT2/2	BKPT3/2	SVC2	U3080
H	H	BKPT1/3	BKPT2/3	BKPT3/3	SVC3	U3090

Table 4-18
UMAP/Write Protect RAM Selection

BC FC1(H)	BC FC2(H)	U2080A			
SA12(H)	SA13(H)	1Y	2Y	Memory Accessed	RAM Devices
L	L	L	L	U.D. ACCESS(L)	U3010 U4010
L	H	H	L	S.D. ACCESS(L)	U3030 U4030
H	L	L	H	U.C. ACCESS(L)	U3020 U4020
H	H	H	H	S.C. ACCESS(L)	U3040 U4040

Table 4-19
UMAP/Write Protect Data Lines

SD0(H)	SD1(H)	WRPROTECT (L)	Mapping
L	L	Yes	Prototype
L	H	No	Memory
H	L	Yes	Program
H	H	No	Memory

When MAPRAMWR(L) is deasserted, the RAM devices selected will monitor MA0(H)–MA11(H) and output the PROTOMAP(L) and WRPROTECT(L) data previously loaded by the development system.

Notice that U5060B and U5060C are enabled by MAPRAMRD(L), indicating that the development system has requested to read the UMAP/Write Protect RAM's data information (via SD0(H) and SD1(H)).

Breakpoint Interrupts 

The Breakpoint Interrupt logic qualifies BKPT1(L), BKPT2(L), and BKPT3(L) and presents them to the AUX Status Port. Let's look at each of these Breakpoint signals individually.

NOTE

In this discussion, we'll assume that BKPT1 ARMS BKPT2(H), from the AUX Control Port, is deasserted. BKPT1 ARMS BKPT2(H) is discussed later in this section.

BKPT1 data, along with RUNNING(H) is presented to U4060B. When these inputs are all asserted, J-K flip-flop U2120A sees a high at 'J'. When U2120A is clocked with a breakpoint valid by U1130A, 'Q' presents a low to U3110D. U3110D then asserts BKPT1(L).

BKPT2(L) is qualified and clocked in the same manner as BKPT1, with the exception of an added qualifier at pin 3 of U4060A. Pin 3 goes low while the 68000 microprocessor is running (RUNNING(H) high) and BKPT1 ARMS BKPT2(H) is deasserted.

BKPT3(L) is qualified and clocked to the AUX Status Port in the same manner as BKPT1(L).

Note that the J-K flip-flops used for BKPT1(L)–BKPT3(L) are reset when the AUX Status Port is read (BA 8E RD(L) asserted).

BKPT1 ARMS BKPT2 

When BKPT1 ARMS BKPT2(H) (from the AUX Control Port shown at the bottom of the schematic) becomes asserted, a BKPT2(L) (high) cannot be issued until a BKPT1 has occurred. When BKPT1 does occur, BKPT1(L) is not asserted due to U3110D.

SVC 

SVC-M(H)/IO(L) low indicates that a Service Call is to be performed by the development system. This low requires that SVC0(L)–SVC3(L) and U2040A's output all be low. For U2040A to output a low, it must be presented with SVC ENABLE(H) high (from the AUX Control Port) and a Breakpoint/SVC valid (pin 5 of U1130A high).

Clock Fail Detect 

This circuit monitors BB CPUCLK(L) to make sure that the clock signal is greater than 2 MHz and less than 8 MHz.

U5150 is a counter that counts the number of positive clock edges presented by BB CPUCLK(L). The number of clocks are represented in binary by output lines A–D (where A =

low-order bit and D = high-order bit). The duration of the count is approximately 600ns (at pin 1 of U5150) and is controlled by SYS CLK(H) divided by 10 (U2130).

The gates from U5150 to U5040D decode the output of U5150. If A–D are low (indicating a count of zero) or if D is high (indicating a count of eight or more), then pin 2 of U3150A is driven low. When U5150 is reset, the count is terminated and U3150A is clocked, forcing CLK FAIL(H) high.

The feedback loop from U3150A to U5040D assures that when CLK FAIL(H) has been asserted, it will remain asserted until the Emulator Processor has been reset. Note that the emulator reset sequence will deassert, then assert DLYD ACTIVE(H) on pin 4 of U3150A.

AUX Status Latch 

For information about this latch, refer to the AUX Status Port discussion earlier in this section.

AUX Control Latch 

For information about this latch, refer to the AUX Control Port discussion earlier in this section.

EMU Control Latch 

For information about this latch, refer to the EMU Control Port discussion earlier in this section.

Buffer Board

The Mobile Microprocessor board, which houses the 68000 microprocessor, connects directly to the Buffer board. The Buffer board's major function is to buffer signals to and from the 68000 microprocessor.

User Function Code Buffers 

When the 68000 Emulator Processor is running in your prototype circuit (RUNNING(H) asserted), the 68000 microprocessor's Function Code lines (FC0(H)–FC2(H)) are buffered to the prototype via U6020B. When the 68000 is running out of the Dump/Restore PROM (RUNNING(L) high), the Forced Function Code lines (FFC0(H)–FFC2(H)) from the AUX Control Port on EMU 2 are driven to the prototype. This allows the Emulator Processor to read or write to any memory space while doing a UGET or UPUT operation. When A/DTRIST(L) is low, U6020 and U6050 are tri-stated.

Probe to EMU Control Signal Buffer 

U2050 buffers the 68000 microprocessor control signals to EMU 1.

Probe Control Signal Generation 

The Probe Control Signal Generation logic consists of eight output signals. Let's look at each of these signals in turn.

VPA(L). When asserted, VPA(L) indicates to the 68000 microprocessor that either an autovectored interrupt or an M6800-type cycle (E and VMA) has been requested.

U9030D will assert VPA(L) only when an address strobe is present (AS(L) is low) and a VPA cycle is requested. A VPA cycle is requested when any one of the following conditions exist:

- The prototype circuit is accessed (UACCESS(H) is high) and the prototype circuit requests a VPA cycle (UVPA(L) is low).
- The prototype circuit is not being accessed, UACCESS(H) is low, and U5050B has issued an interrupt acknowledge (FC1(H), FC2(H), and BB FFC0(H) are all high). This is to make sure that any interrupts being issued while the 68000 microprocessor is executing out of the Dump/Restore PROM will be autovectored.
- A probe break interrupt acknowledge is issued (POD BKINTA(L) is low). This is the interrupt acknowledge associated with an Emulator Processor-issued NMI, and requires the autovectored request (refer to the Control board description for more details).

QBG(L). The qualified bus grant signal, QBG(L), is used on the Power Supply board to turn on the BG (bus grant) indicator LED. U9030C asserts QBG(L) when the Emulator Processor is active, BA DLYD ACTIVE(H) is high, and the 68000 microprocessor issues a bus grant (BG(L) is low).

DTACK T.O.(H). A data transfer acknowledge time-out (DTACK T.O.(H) high) is issued by U4030B when the prototype circuit is accessed (UACCESS(H) is high), a user data transfer acknowledge (UDTACK(L) low) has not been issued by the prototype circuit, and a data strobe is present (UDS/LDS(H) is high). UDS/LDS(H) is asserted via U7040A when UDS(L) or LDS(L) is low. The assertion of DTACK T.O.(H) is delayed approximately 200 us due to an R-C network made up of R7034 and C7031.

QUINTA(H). A qualified user interrupt acknowledge (QUINTA(H) high) indicates that an interrupt acknowledge in the prototype has occurred. QUINTA(H) is asserted by U8010B when UAS(L) is low and U5050B has issued an interrupt acknowledge (FC1(H), FC2(H), and BB FC0(H) are all high).

QINTA7(H). A qualified level-seven interrupt acknowledge from the 68000 (QINTA7(H) high) indicates a level-seven interrupt to the prototype circuit. U9090B asserts QINTA7(H) when an address strobe is present (AS(L) is low) and U7030 issues a level-seven interrupt acknowledge (U7030 pin 8 is low). A level-seven interrupt acknowledge is true when PA1(H)–PA3(H), ST0/BKINTEN(H), BB FC0(H), FC1(H), and FC2(H) are all asserted.

BA MODE0(L) and BC MODE0(H). BA MODE0(L) and BC MODE0(H) both originate from U7040B, which is used as an inverting buffer. BA MODE0(L) is buffered further by U5030C, to produce BC MODE0(H). When asserted, these signals indicate that Emulation Mode 0 has been selected.

BG(H). BG(H) is BG(L) inverted by U9050F, and BB AS(L) is the equivalent of AS(L) buffered through U5020C.

User Strobe Enable/Disable 

68000 microprocessor control signals AS(L), LDS(L), UDS(L), R(H)/W(L), and VMA(L) are qualified by Emulator Processor control lines at U8020. These signals are buffered to the prototype circuit at U9010, which is controlled by the state of CTRIST(H). Refer to the Halt/Bus Request Tri-State function block description later in this section for more information on CTRIST(H).

The following text describes how U8020 qualifies the 68000 microprocessor's signals.

UAS(L). The address strobe signal (UAS(L)) is driven to the prototype circuit by one of two means:

- Jumper P6 is in its normal (1–2) position and both of the following are true:
  1. The 68000 microprocessor is running or performing a UGET or UPUT operation (UG/UP+RUNNING(H) is high).
  2. The 68000 microprocessor operation cycle being executed is not an Emulator Processor-caused NMI acknowledge (output of U7030 is high).
- Jumper P6 is in its optional (2–3) position and the 68000 microprocessor operation cycle being executed is not an Emulator Processor-caused NMI acknowledge (output of U7030 is high).

UR(H)/W(L). UR(H)/W(L) is driven to the prototype circuit when both of the following are true:

- The 68000 microprocessor is running a program or executing a UGET or UPUT operation (UG/UP+RUNNING(H) is high).
- The 68000 microprocessor operation cycle being executed is not an Emulator Processor-caused NMI acknowledge (output of U7030 is high).

ULDS(L), UUDS(L), and UVMA(L). The upper and lower data strobes (UUDS(L) and ULDS(L)) and valid memory address (UVMA(L)) signals are all qualified in the same manner. U5050A enables these signals to the prototype circuit when all of the following conditions are true:

- The 68000 microprocessor is running a program or executing a UGET or UPUT operation (UG/UP+RUNNING(H) is high).
- The 68000 microprocessor is not attempting a write to a write protected block of memory (U7040D).
- The 68000 microprocessor operation cycle being executed is not an Emulator Processor-caused NMI acknowledge (output of U7030 is high).

UGET/UPUT Or RUNNING Decode 

A UGET or UPUT cycle is a read from or a write to the prototype circuit that occurs while the Emulator Processor is executing from Dump/Restore PROM. For more information on UGET(H) and UPUT(H), refer to the UGET/UPUT Decode function block description earlier in this section.

The 68000 microprocessor communicates with the prototype circuit when any of the following conditions occur:

- The Emulator Processor is running in Mode 2, or in Mode 1 with memory mapped to the prototype.
- The current cycle is a UGET.
- The current cycle is a UPUT.

While the UGET or UPUT routine is being executed, the respective signal is high. Using UPUT(H) for example, let's look at the sequence required to assert UGET/UPUT+RUNNING(H) via U6040 and U5030B.

During the UPUT routine, the 68000 microprocessor is reading its instructions from the Supervisor Program memory space. For one bus cycle, however, the 68000 microprocessor will write a byte or word (depending on whether the UPUT is byte or word oriented) to Supervisor Data space. It is this write to Supervisor Data space that is enabled to the prototype circuit. U6040 decodes 68000 microprocessor Function Code lines FC0(H) and FC1(H), to ensure that the current access is to the Supervisor Data space. (The state of FC2(H) is irrelevant because we know that the 68000 microprocessor is in Supervisor space when executing Dump/Restore code.) U6040 also assures that UPUT(H) is asserted and that the current cycle is a write, R(H)/W(L) is low. If these conditions are met, U6040 will drive its output low, forcing U5030B's output high.

UACCESS(H) is asserted when UG/UP+RUNNING, MODE1, or MODE2 are asserted.

Clock Select <17>

The Emulator Processor accepts two possible clock sources: UCLK(L) or MODE0 CLK(H). The UCLK(L) signal from the prototype can not exceed 8 MHz.

In Emulation Mode 0, U5010A is enabled by MODE0(L). This allows MODE0 CLK(H) to drive output lines CPUCLK(L), BA CPUCLK(L), and BA CPUCLK(H).

In Emulation Mode 1 or 2, however, the prototype's clock (UCLK(L)) is used, via analog switch Q9011. Because UCLK(H) is buffered with an F04 in the 64-Pin Plug, U7010A inverts UCLK(L) before it is passed to Q9011. Q8011, via MODE0(H), controls the biasing of Q9011.

User Bus Request Control <17>

The prototype circuit's UBR(L), UBERR(L), and UBGACK(L) signals are received by two 74S241s. U5010 is enabled while operating in Mode 1 or 2 (MODE0(L) is high). U6020 is enabled only while operating in Mode 1 or 2 and the 68000 microprocessor is running (decoded by U4030A, located in the UGET/UPUT OR RUNNING Decode function block). Depending on the position of jumpers P2 and P3, output signals BR(L) and BGACK(L) are passed through either U5010 or U6020 to the 68000 microprocessor. These jumpers affect when the prototype is able to request the 68000 bus. Refer to Section 3 of this manual for more information on jumpers P2 and P3.

Processor DTACK Generation/Select <17>

The 68000 microprocessor requires that memory devices respond with a Data Transfer Acknowledge (DTACK(L)) to indicate that the data either has been written, or is on the bus ready for the 68000 to read.

DTACK EN(H) is a delayed data strobe signal created on the Mobile Microprocessor board. DTACK EN(H) (when low) prevents a DTACK from being asserted to the 68000 microprocessor too soon. For more information regarding DTACK EN(H), refer to the Mobile Microprocessor board circuit descriptions later in this section.

DTACK(L) is generated differently in each emulation mode. Let's look at the generation and use of DTACK(L) for each mode.

NOTE

When the 68000 microprocessor is running Dump/Restore (not doing a prototype access, UACCESS(H) is low), the Emulator Processor must assert its own DTACK regardless of the emulation mode selected.

MODE 0. In Emulation Mode 0, all memory references are to Program Memory. Therefore, all memory cycles must rely on DTACK EN(H) to insure that the 68000 microprocessor does not override the Program Memory's access time. In Emulation Mode 0, there is no prototype DTACK, so the Emulator Processor must create its own DTACK.

U5040's pins 1, 11, 12, and 13 are used by the Emulator Processor to internally-generate a DTACK. Pin 1 indicates whether the Emulator is accessing the prototype circuit. U6010C pulls pin 1 of U5040 high when UACCESS(H) is low or when U9030A's output is low. The output of U9030A can be low only when a break condition exists (BKCOND(H) is high) and a DTACK time-out occurs (DTACK T.O.(H) is high) with jumper P7 in its normal (1–2) position. (For more information regarding jumper P7, refer to Section 3 of this manual.)

U5040's pins 11, 12, and 13 determine when during the cycle DTACK(L) is to be asserted. Pin 11 is tied high by R7045 and is not dependent on the position of jumper P1. Pin 12 becomes high when DTACK EN(H) is asserted. Finally, pin 13 of U5040 becomes high when a data strobe is present (DS(H) is high).

MODE 1. In Emulation Mode 1, DTACK(H) is synthesized with two AND functions.

The first AND function is the prototype's data transfer acknowledge, UDTACK(H) (lower left), qualified with DTACK EN(H) and Mode 1 operation (see pins 4, 5, and 6 of U5040). Pin 5 is asserted by U6030 when both MODE0(H) and MODE2(H) are low, and DTACK EN(H), BKCOND(L), and UG/UP+RUNNING(H) are high. The qualification by DTACK EN(H) at pin 4 is controlled by jumper P1. If P1 is in its optional (2–3) position, UDTACK(H) at pin 6 of U5040 will cause a 68000 microprocessor DTACK with no further qualification. This may result in the loss of data transferred if Program Memory cannot run at full speed. Refer to Section 3 of this manual for more information on jumper P1.

The second AND function is performed using pins 9 and 10 of U5040. The same qualifications stated in the previous AND function description for pin 5 are also true for pin 9.

However, UDTACK is not factored in, because it is used for creation of DTACK(L) only while memory is mapped to the prototype's memory. Therefore, when memory is mapped to Program Memory (SMAP(H) high), and jumper P8 is in its normal (1–2) position, DTACK will be asserted regardless of the state of UDTACK(H).

MODE 2. In Emulation Mode 2, DTACK(L) is asserted using MODE2(H) and UDTACK(H) as qualifiers (see pins 2 and 3 of U5040). Pin 2 is driven high by U6030 when the Emulator Processor is in Mode 2 (MODE2(H) high) and is performing a UGET/UPUT OR RUNNING operation. If the Emulator Processor trys to stop program execution, DTACK EN(H) will qualify DTACK(L) through U8010B.

Probe To Prototype A/D Buffers 18

The Probe To Prototype A/D Buffers circuit block contains the address and data line buffers to your prototype circuit. The address buffers are enabled when A/DTRIST(L), from the Control board, is high. A/DTRIST(L) indicates that the 68000 microprocessor has tri-stated its address and data buses, and that the Emulator Processor must tri-state its buses also. The deassertion of A/DTRIST(L) also qualifies the data buffer's enable line through U6010A.

When the output from U6010A is low, the data buffers are enabled to or from the prototype. For U6010A's output to be low, A/DTRIST(L) and ID TO(L)/FROM(H) must be high. This allows data transfers between the 68000 microprocessor and the prototype circuit.

The R(H)/W(L) line controls the data buffer direction. When R(H)/W(L) is high, data is read from the prototype. When R(H)/W(L) is low, data is written to the prototype.

Probe To EMU A/D Buffers 18

The Probe To EMU A/D Buffer devices buffer address and data lines to EMU 1 and EMU 2. The address buffer's enable lines are tied high (always enabled). However, the data buffer's direction is controlled by ID TO(L)/FROM(H). Data is enabled to the 68000 microprocessor when ID TO(L)/FROM(H) is low, and from the Interface Assembly (68000 microprocessor or prototype circuit) when ID TO(L)/FROM(H) is high. While data is enabled to the 68000, U6010A disables the buffers that access the prototype so that bus contention does not occur The data is enabled from the Interface Assembly so that the 68000 can transfer data to the main boards, and the TTA option can monitor data transfers between the 68000 and the prototype circuit.

Buffer Board Feedthroughs 19

This schematic shows the buffered lines to and from the Buffer board.

Mobile Microprocessor Board

The Mobile Microprocessor board contains the MC68000-8 emulation device and memory access wait state generator.

DTACK EN/Wait State Generator 20

DTACK EN(H) is essentially a data strobe (LDS(L) or UDS(L)), qualified by HOLD(L) and wait state jumpers J1045 and J2045. The jumper positions are based on the speed of the 68000 microprocessor. If the memory access time of the 68000 is faster than that of Program Memory, a delay is inserted in the 68000 memory cycle. Table 4-20 lists the delays. For more information on J1045 and J2045, refer to Section 3 of this manual.

HOLD(L) is a buffered signal from the development system and is for factory use only.

Table 4-20
Memory Access Delays

J1045[a]	Delay	J2045[a]	Delay
A1 to A	None	A1 to A	None
A1 to B	40ns	A1 to B	20ns
A2 to B	80ns	A2 to B	40ns
A3 to B	120ns	A3 to B	60ns
A4 to B	160ns	A4 to B	80ns
A5 to B	200ns	A5 to B	100ns

[a] **The delays imposed by J1045 and J2045 are cumulative (For example: When J1045 and J2045 are in their A2 to B positions, J1045 imposes an 80 ns delay and J2045 imposes a 40 ns delay. The total delay is 120ns.)**

Control Board

The Control board's major function is to handle interrupts, which are used by the Emulator Processor to cause control transfers. The Control board also buffers the HALT and RESET lines, and samples the bus arbitration signals and HALT line to determine when the 68000's address, data, and control lines are tri-stated. (If the 68000 uses tri-state lines, the Emulator Processor will also use tri-state lines.)

Probe NMI Decode 21

U7010B buffers the interrupt lines from the prototype (UIPL0(L)–UIPL2(L)) and is enabled by MODE1+2(H) high. U4010B asserts LEVEL7(H) indicating an NMI (level 7) interrupt when UIPL0(L)–UIPL(L) are all asserted. Notice that in its optional (2–3) position, jumper J4011 will inhibit the assertion of LEVEL7(H). For more information on jumper J4011, refer to Section 3 of this manual.

EMU-Issued Interrupt Buffers 21

The EMU-Issued Interrupt Buffers (U7010A, U6010A, U6010B, and U3000) drive various interrupts to the 68000 and are discussed later in this section under the heading Emulator Issued Interrupt Enable Control.

Probe Interrupt Decode 21

The Probe Interrupt Decode circuitry decodes the prototype interrupt lines for interrupt levels 1–6. While the 68000 is executing a D/R routine, the Emulator Processor samples the prototype interrupt lines, to ensure that a prototype interrupt is not missed. In the case of an interrupt other than an level 7, the Emulator Processor expects that the prototype will hold the interrupt asserted until acknowledged.

When the 68000 begins executing user instructions after exiting a D/R routine, the prototype interrupt lines are sampled by clocking them into U5010 on the rising edge of INTMACHEN(H) from the Break Interrupt Control. This prototype interrupt sample at U5010 is presented to comparator U6020. U6020 is also presented the interrupt mask level (located in the Status Register) from U7020. U7020 is loaded with the current state of the interrupt mask level (D8, D9, and D10) when clocked due to the unstacking that occurs just after an RTE instruction. U6020 compares these two interrupt levels, with the result of the comparison output as LEVELINT(H). LEVELINT(H) will only be asserted if the prototype interrupt level is greater than the masked interrupt level. In its optional (2–3), jumper J6021 inhibits the assertion of LEVELINT(H) For more information on J6021, refer to Section 3 of this manual.

EMU-Issued Interrupt Enable Control 

The function of the EMU-Issued Interrupt Control block is to enable one of four different interrupt paths to the 68000 at different times. Before we discuss this circuit in detail, let's look each of the four interrupt paths.

Path one (U7010A enabled) allows prototype interrupt lines to the 68000. U7010A is enabled when both of the following are true:

- A break interrupt is not pending.
- The Interrupt State Machine (discussed later in this section) is in State 2 (open prototype interrupt buffers).

NOTE

In order for Path one to become valid, the 68000 must run more than one user instruction without breaking. Thus, U7010A is never enabled while the Emulator Processor is in Trace All mode.

Path two (U6010B enabled) allows prototype interrupts (other than level 7) to the 68000. Upon beginning execution of user instructions, U6010B is enabled when the Interrupt State Machine recognizes that a prototype interrupt is pending. This path is used during Trace All if the prototype interrupt lines are a level higher than the interrupt mask in the 68000 Status Register.

Path three (U6010A enabled) allows a break interrupt (NMI) to the 68000. U6010A is enabled when the Emulator Processor encounters a break condition, and remains enabled until a new Status Register is unstacked.

NOTE

U6010A holds the 68000 interrupt lines at level 7 (NMI) the entire time that the 68000 is executing out of the D/R PROM.

Path four (U3000A enabled) allows a mask level interrupt to the 68000. This path assures that the Emulator Processor does not cause an intermittent interrupt if you use the SET command to change the Status Register to an interrupt level less than 7.

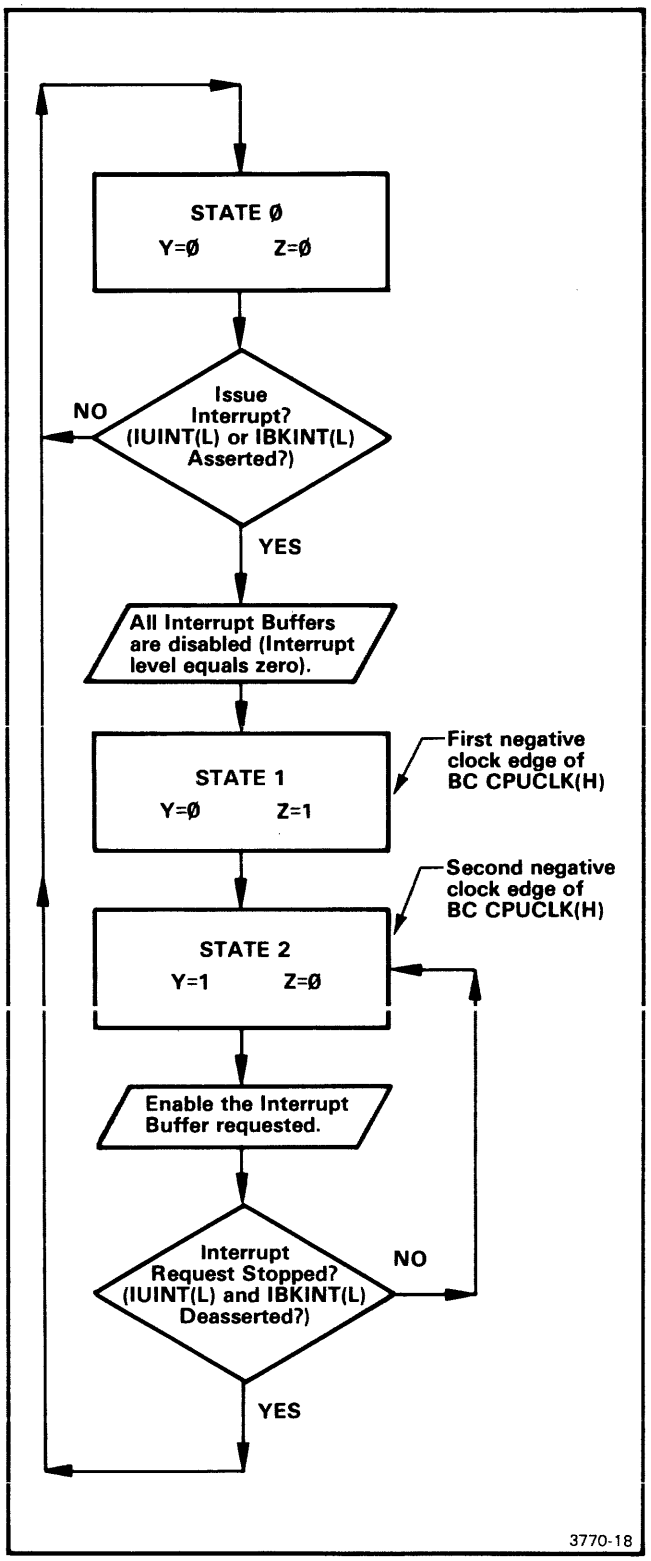


Fig. 4-10. Interrupt Buffer Control State Machine.
U2050A is referred to as Y and U2050B is referred to as Z. To assure that two negative edges occur, there is no decision between State 1 and State 2.

NOTE

To assure that an extraneous interrupt is not issued, U3000A is enabled only if an NMI is being asserted (see U2000A). Path four continues to be enabled until path one, two, or three become enabled.

Figure 4-10 is a flow chart of the Interrupt Buffer Control State Machine. Figure 4-11 is a timing diagram of the buffer control circuitry. Refer to these figures as you read the following discussion.

The 68000 samples the interrupt lines on the falling edge of BC CPUCLK(H). To create an interrupt, the 68000 samples the interrupt lines on two consecutive edges and finds the level higher than the two previous consecutive edges. The Interrupt Buffer Control State Machine accomplishes this in the following manner:

1. When an interrupt request (IUINT(L) or IBKINT(L) asserted) arrives from the Interrupt State Machine, all four buffer paths are disabled (using U1040A, U7030C, and U2040C). Pull-up resistors R2030, R2031, and R7032 (iocated on the Buffer board) will bring the interrupt lines to a level zero state.
2. The Buffer Control State Machine counts two negative clock edges (BC CPUCLK(H)), then enables the interrupt buffer requested.

NOTE

When OPEN USER(L) is deasserted, path one (U7010A) is disabled. When RESET SAMPLE(H) is asserted, path four (U3000) is disabled. OPEN USER(L) and RESET SAMPLE(H) are both generated from the Interrupt State Machine.

RESET/HALT Buffers 

The main function of the RESET/HALT Buffer block is to buffer bi-directional signal lines RESET(L), URESET(L), HALT(L), and UHALT(L) in the same direction as the 68000 microprocessor. The direction in which HALT(L) and UHALT(L) are buffered is controlled in the same way as RESET(L) and URESET(L). For this reason, we will look only at RESET(L) and URESET(L).

Buffers U4020C and U4020D are enabled or disabled by U5020B and U4010C, respectively (only one of these buffers may be enabled at a time). Notice that U5020B and U4010C monitor each other's outputs (U5020B's pin 11 and U4010C's pin 9), and also monitor both URESET(L) and RESET(L) (U5020B's pin 10 and U4010C's pin 10).

Let's look at an example that shows how these buffers are to be enabled or disabled.

1. U5020B's pin 10 is driven low before U4010C's pin 10. (This indicates that the direction of the buffers is to be from URESET(L) to RESET(L)).
2. U5020B's output goes high, enabling buffer U4020C and driving U4010C's input pin 9.
3. With U4020C enabled URESET(L) low is buffered and becomes RESET(L) low.
4. With U4010C's pin 9 held high by the output of U5020B, U4010C's output must remain low (disabling buffer U4020D).

When EN WINDOW(L) is deasserted, the buffer enable circuitry s overridden and all four buffers used by RESET(L), URESET(L), HALT(L), and UHALT(L) are disabled.

BRDHALT(L) is asserted to EMU 1 to indicate a double bus or address error. (The 68000 is driving the HALT(L) line indicating a reset is required.)

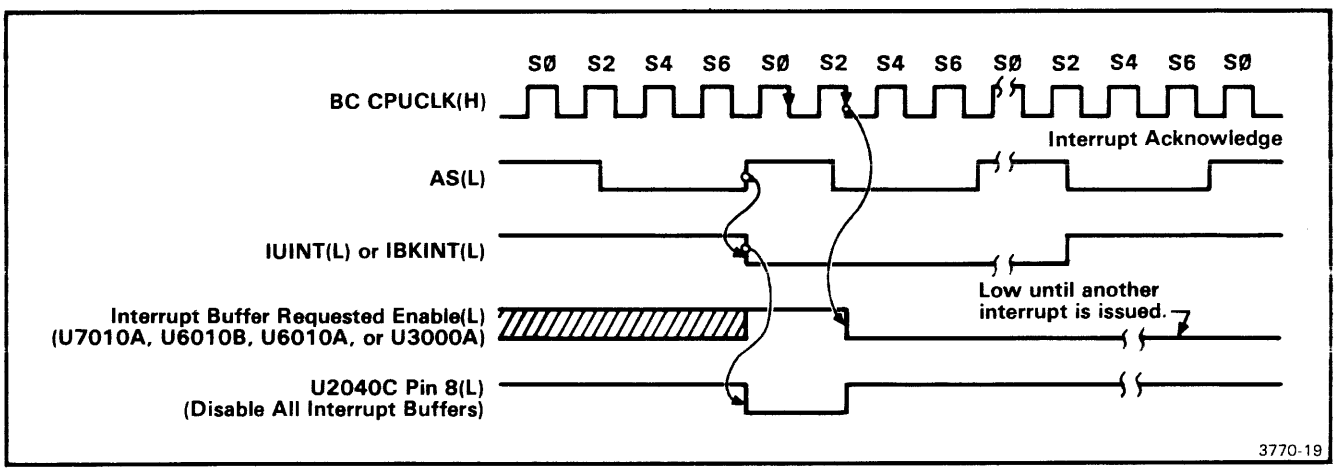


Fig. 4-11. Timing of the Buffer Control State Machine.

IUINT(L) and IBKINT(L) are from the Interrupt State Machine, discussed later in this section.

HALT/BR Tri-state Control (22)

A/D TRIST(L) and CTRIST(H) are generated here. When the 68000 microprocessor tri-states its address, data, or control lines, the Emulator Processor must also tri-state its buffers. The 68000 tri-states under either of the following conditions:

- The prototype requests a halt by asserting UHALT(L). In this case cnly the address and data are tri-stated.
- The prototype requests the bus using the normal bus arbitration sequence. Address, data, and control lines are tri-stated.

U3030A, U2040D, and U3030B assert A/D TRIST(L) when CTRIST(H) is asserted, or when the QHALT line has been asserted for two negative clock edges and AS(H) is deasserted.

CTRIST(H) is asserted when operating in Emulation Mode 0 (BD MODE0(H) asserted) or BG(H) is asserted with BBAS(L) deasserted (U7030A and U6040A). CTRIST(H) is deasserted when both BR(L) and BGACK(L) are deasserted (U7030B, U6030A, and U6040A).

Probe NMI Pending Decode (23)

The Probe NMI Pending Decode circuitry asserts NMI PENDING(L) only when LEVEL7(H) is deasserted for at least two consecutive negative clock edges and then asserted for two consecutive negative clock edges. (LEVEL7(H) indicates an interrupt level-seven when asserted or an interrupt level less than seven (1–6) when deasserted.) Shift register U1050 and AND gate U1040B monitor LEVEL7(H) for the LEVEL7 shift sequence, using CPUCLK(L) as the clock.

R-S flip flop U6040D is set, asserting NMI PENDING(L), when U1040B's output is low. When either an emulator reset or a probe interrupt acknowledge occurs, U6040D is reset, deasserting NMI PENDING(L) and driving U2040B's output low.

Interrupt State Machine (23)

While the 68000 microprocessor is running user instructions, the Interrupt State Machine transfers control from the user program to the D/R PROM routines. Let's approach this function block by discussing the high-level information flow rather then describing the representation.

Refer to the Interrupt State Machine flow chart in Fig. 4-12 as you read the following paragraphs.

The Interrupt State Machine starts in STATE 0 and remains in that state until BA INTMACHEN(H) is asserted (that is, when the 68000 begins program execution). Then Interrupt State Machine starts to shift states as follows:

- STATE 1—If a probe interrupt has been generated (NMI PENDING(H) or LEVEL INT(H) asserted at U3010A), the interrupt needs to be presented to the 68000.
- STATE 3—A break interrupt is pending (BA BKCOND(H) from the Emulator Break Generator is asserted).
- STATE 2—If no interrupts pending, probe signals need to be enabled to the 68000 (assert OPEN USER(L) until BA BKCOND(H) is asserted).

Power Supply Board

The Power Supply board converts the development system's +12 Vdc line into two auxiliary voltage lines, and thus reduces the current required of the development system's +5.2 Vdc power supply. These two auxiliary voltages are +5.2V PROBE and +4.9V, both of which are used exclusively by the Prototype Control Probe.

LED displays are located on the Power Supply board and are visible on the Prototype Control Probe's Interface Assembly.

+4.9V Regulator (24)

The +4.9 Vdc supply is produced by a switching power supply on the Power Supply board. A small current from the +12 Vdc line passes through input filter L3021 and resistor R4031 to the input of voltage regulator U3040. This current turns on the switching transistor (Q4021) and allows a much larger current to pass to the power supply's coils (L4041 and C6041). At this point, the following steps occur to complete the power supply's switching cycle:

1. When the voltage at the output node (between R4042 and L4033) reaches a predetermined level, U3040 begins to draw less current. This predetermined voltage level varies, because it is determined by adjusting R1051 until TP1061 is +4.9 Vdc.
2. When U3040 begins to draw less current, Q4021 begins to turn off. This causes current to flow from L4041 through the flyback diode (CR3021).
3. CR3021 is reverse-biased, shutting off switching transistor Q4021 completely and causing positive feedback through VR3022, C3032 and R4031. This transition turns the voltage regulator off.
4. When the voltage at the R4042/L4033 junction drops, the voltage regulator again turns on and this cycle is repeated.

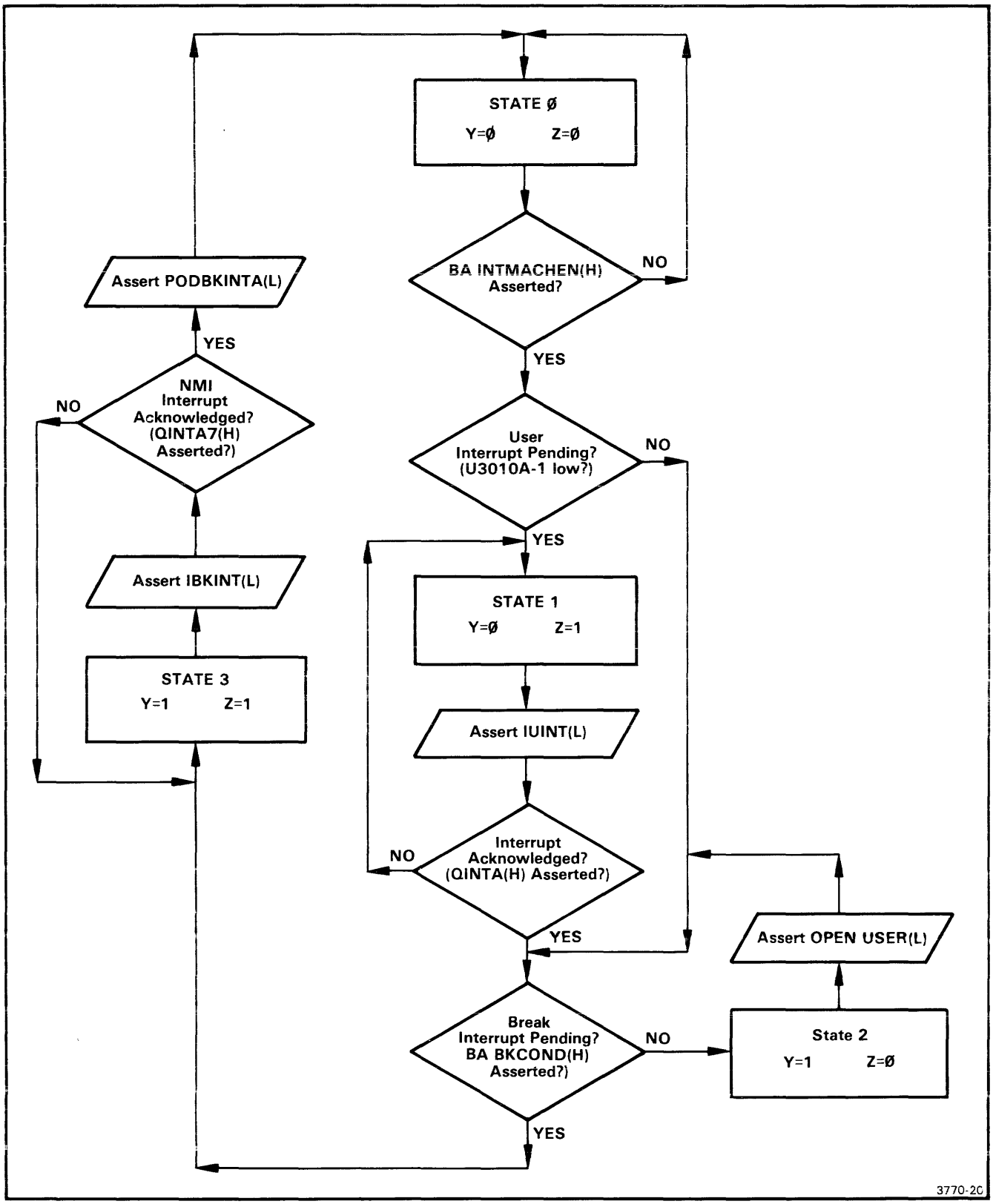


Fig. 4-12. Interrupt State Machine.

Y and Z represent the state of U3040A's and U3040B's Q outputs, respectively. The clock for the Interrupt State Machine is provided by the falling edge of AS(H).

Although voltage would be available at the output node during each cycle, the +4.9 Vdc is not available to the probe until the switching power supply is enabled. Since the +12 Vdc supply is current-limited, the power supply will not be enabled until C1041 is fully charged.

The switching power supply is enabled by the ACTIVE O.C.(H) signal. This signal is asserted when bit 7 of the emulator's EMU Control Port is set. Essentially, the power supply is turned on when the 68000 Emulator Processor is selected.

Once asserted, the ACTIVE O.C.(H) signal enables the switching power supply in the following manner:

1. ACTIVE O.C.(H) is high at the base of Q5012. This signal turns on the transistor and causes its collector to go low.
2. The low at the collector of Q5012 biases both Q5011 and Q3011.
3. When Q5011 is turned on, current passes through Q5011 to bias Q6021 and operate the probe's fan.
4. When Q3011 is turned on, the power supply is enabled. Current passes through the output filter (L4033 and C5031) and through Q3011 to other circuitry in the Prototype Control Probe.

+5.2V PROBE Regulator <24>

The +5.2V PROBE supply is produced by a single voltage regulator on the Power Supply board. This voltage regulator (U2010) converts +12 Vdc into +5.2V PROBE. The voltage is adjusted by turning potentiometer R1011 until TP1011 is +5.2 Vdc.

Fan Control <24>

Refer to the +4.9V Regulator function block description.

LED Control <24>

Refer to Section 1 of this manual for more information on the Prototype Control Probe's LEDs.

A TYPICAL EMULATION CYCLE

To complete a typical emulation cycle, the 68000 Emulator Processor performs four basic operations: resetting the emulator or microprocessor, starting the emulator, running the emulator, and stopping the emulator. The following paragraphs discuss each of these operations, using a "G 100" command as an example.

In this discussion, we'll assume that the Emulator Processor is being used in an 8550 Microcomputer Development Lab running under DOS/50 Version 2. We'll also assume that the Emulator Processor is selected and operating in Emulation Mode 0.

Resetting the Emulator or Microprocessor

There are two different reset levels for the 68000 Emulator Processor: the Emulator reset (which resets the 68000 Emulator Processor) and the Microprocessor reset (which resets only the 68000 microprocessor).

Emulator Reset

If the PROBEPWR bit (D7) of the EMU Control Port (refer to Fig. 4-13) is cleared, the Emulator Processor turns off the power to the Interface Assembly. The Emulator reset is required whenever the PROBEPWR bit has been cleared (for example, by the SEL, EDIT, or ASM commands).

The 68000 microprocessor requires approximately 0.1 second, to perform an Emulator reset. The sequence of events for an Emulator reset is as follows:

1. The 2650 writes to the EMU Control Port, setting the emulation mode (bits D6 and D5), and clearing the PROBEPWR bit (D7) and EMU ACTIVE bit (D2).
2. The 2650 writes to the EMU Control Port, asserting the PROBEPWR bit (D7). The Emulator Processor turns on the power to the Interface Assembly.
3. The 2650 waits for 0.1 second, then asserts the EMU ACTIVE bit (D2).

This completes the Emulator reset.

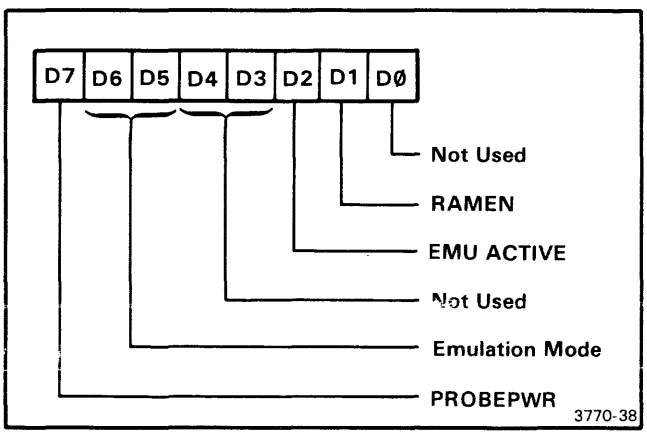


Fig. 4-13. EMU Control Port.

Microprocessor Reset

The Microprocessor reset is required whenever the emulation mode changes or the 68000 microprocessor halts. The EMU Status Port bit D2 (refer to Fig. 4-14) indicates whether an Emulator reset (D2=1) or a Microprocessor reset (D2=0) is required. When a Microprocessor reset is performed:

1. The EMU ACTIVE bit (D2) in the EMU Control Port is cleared.
2. The EMU ACTIVE bit (D2) in the EMU Control Port is asserted.

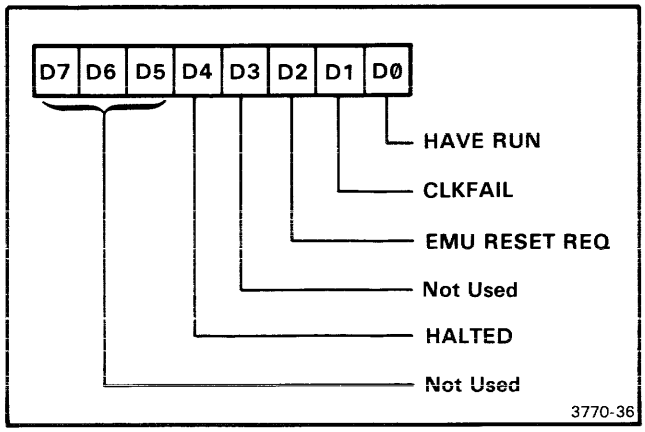


Fig. 4-14. EMU Status Port.

Starting The Emulator

Let's assume that you've entered the following commands at the system terminal:

```
S SSP=67FE SR=2700  <CR>  (These values become the register image)
G 100  <CR>
```

No action is taken until you enter "G 100" (followed by a carriage return). The System Processor then restores the 68000 microprocessor's registers, as follows:

1. The 2650 enables its access to the Shared Communication RAM by asserting D1 at the EMU Control Port.
2. The 2650 then loads the Shared Communication RAM with the register image (SSP=67FE and SR=2700).
3. The 2650 writes a Register Restore command to D1–D5 in the Command Port (see Fig.4-15). The 2650 then polls the Command Port until the 68000 microprocessor has finished executing the Register Restore command. Bits D1 and D4 in the EMU Status Port (Fig. 4-14) are checked to see if there has been an Emulator Processor fault.
4. The 68000 responds to the Register Restore command by building a new control stack in the Trapstack (the upper four words in the Shared Communication RAM; refer back to Table 4-8). The 68000 builds the Trapstack by using the desired Supervisor Stack Pointer (SSP) 67FE, and by stacking the Program Counter (PC) to equal 100 and the Status Register (SR) to 2700 in the Trapstack.
5. After a Return from Exception (RTE), the 68000 loads the remaining registers from the Register Save Area of the Shared Communication RAM. When the Register Restore command has been executed, the 68000 then clears the Command Port (D7–D1).

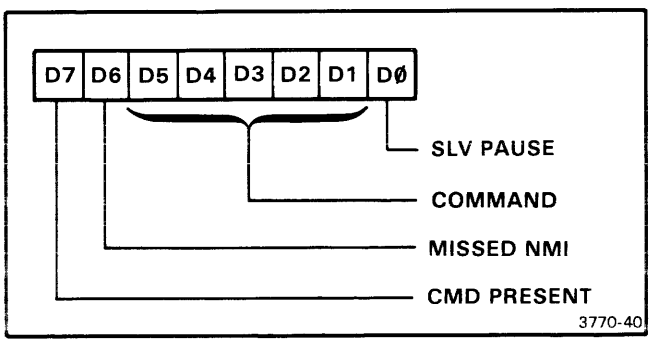


Fig.4-15. Command Port.

Running the Emulator

The 68000 Emulator Processor executes a user program in the following manner:

1. The 2650 issues the RUNUSER command by writing the appropriate command to D1–D5 in the Command Port (see Table 4-3 earlier in this section). The Emulator Processor responds by switching the buffers so that the 68000 microprocessor has access to the Shared Communication RAM. At this time, the 68000 drops from the Command Present polling loop into a Wait for Deassertion of SLV PAUSE (Command Port D0) polling loop.
2. The 2650 executes a HALT instruction and the emulator controller clears SLV PAUSE. The Emulator Processor "sees" this in the polling loop, and branches to the RTE instruction in the special area of the Dump and Restore (D/R) PROM. This enables the RUNUSER sequence.

3. The 68000 then executes an RTE instruction, which retrieves the PC and Status Register from the Trapstack. This transfers control to the user program at PC=100 and SR=2700.

Stopping the Emulator

When a system interrupt occurs, the Emulator Processor stops executing your program and returns control to the 2650. The interrupt may come from a number of sources: the Emulator Processor itself, a keyboard interrupt, timer interrupt, I/O interrupt, or any other system interrupt.

There are two major types of interrupts: non-debug interrupts and debug interrupts.

Non-Debug Interrupts

A non-debug interrupt asserts SLV PAUSE (bit D0 in the Command Port). This has no effect on the emulation process, since the emulator control software just resumes emulation by calling the halt routine. A non-debug interrupt may be generated by the keyboard (other than by typing CTRL-C), the timer, or I/O.

Debug Interrupts

A debug interrupt requires service by the emulator control software or firmware. These interrupts indicate that some change of control is required. The following sources may generate debug interrupts:

- Emulator Processor: breakpoint, service call, write protection violation, or any Emulator Processor fault (such as clock, power, and halt)
- Memory Allocation Controller (by attempting to access non-existent memory)
- Trigger Trace Analyzer (encounters a breakpoint)
- CTRL-C (CTRL and C keys pressed simultaneously)

When the 2650 is activated, it first executes the appropriate interrupt service routine, then resumes execution of the emulator control software immediately after the halt instruction.

NOTE

It is possible that more than one interrupt may cause the Emulator Processor to stop (such as a BKPT and CTRL-C). The emulator control software checks all possible conditions to determine priority of action.

When the Emulator Processor receives an interrupt (non-debug or debug), a Non-Maskable Interrupt (NMI) to the 68000 microprocessor is asserted.

When the interrupt is acknowledged, the Emulator Processor blocks the 68000 from running the user program, and requires the 68000 to run out of the Dump and Restore (D/R) PROM. This is done by requiring a vector to the D/R PROM routine after the NMI acknowledge. The D/R PROM routine then clears the RUNUSER command from the Command Port and begins polling the Command Port for further commands from the 2650.

The 2650 reads the Status Port on the Emulator Processor to determine the cause(s) of the break (Emulator Processor Halted).

With a non-debug interrupt, the 2650 issues a Register Dump command to the Command Port. The 68000 executes the Register Dump routine out of the D/R PROM. (The 68000 dumps its register values into the Shared Communication RAM, and moves SP and SR from the Trapstack into the Register Save Area of the Shared Communication RAM.) When the Register Dump routine is completed, the 68000 clears the Command Port. The 2650 then reads the register values in the Shared Communication RAM, and displays these values on the system terminal.

Section 5

FUNCTIONAL CHECK PROCEDURES

INTRODUCTION

This section tells how to verify the operation of the 68000 Emulator Processor installed in an 8550 Microcomputer Development Lab or an 8540 Integration Unit. To perform verification with the 8550, you'll need a system terminal (connected to the 8301) and the 8550 system diagnostics disk. To perform verification with the 8540, you'll need a system terminal (connected to the 8540), and the 68000 Diagnostics PROM.

This section is not intended to give you a detailed description of the 8550 disk-resident diagnostics or the 8540 ROM-resident diagnostics. The information provided here gives you a procedure to verify the operation of the 68000 Emulator Processor in the quickest way possible.

For more information about your system's disk-resident or ROM-resident diagnostics, refer to the following manuals:

- 8550 Microcomputer Development Lab Installation Guide
- 8540 Integration Unit Installation Guide

For detailed information on development system diagnostics, refer to the following optional manuals:

- 8301 Microprocessor Development Unit Service Manual
- 8540 Integration Unit Service Manual

8550 MICROCOMPUTER DEVELOPMENT LAB VERIFICATION

When both the 8501 and 8301 have displayed "boot" messages on the system terminal, you're ready to run the 8550 disk-resident diagnostics.

Procedure

To verify 68000 Emulator Processor operation, perform the following procedure:

1. Insert the 8550 system diagnostics disk (label side up) into drive 0 (top drive) of the 8501.
2. Close the disk-drive door.
3. Within 6 seconds, the 8501 will begin a preliminary read of the disk.
4. The system terminal will display the following information:

```
8301 BOOT V x.x
8501 V x.x
8301 BOOT V x.x
```

5. The 8501 will begin reading the disk again.
6. Approximately 12 seconds later, the diagnostic greeting message and first menu will appear on the system terminal. The message and menu are shown in Display 5-1.

```
*******************************************************
*         TEKTRONIX INC.                              *
*         8550 DISK-RESIDENT DIAGNOSTIC SYSTEM        *
*         VERSION X.X                                 *
*         Copyright (C) 1981 Tektronix, Inc.          *
*******************************************************


                    RUN MODE MENU
                    -------------

1 - AUTOMATIC MODE    *** default ***
2 - SELECT MODE
H - HELP

Type in desired mode    {<CR> or 1, 2, or H and <CR>}
```

Display 5-1

As soon as the system terminal displays the diagnostic greeting message and RUN MODE MENU, press the RETURN key to select the AUTOMATIC MODE (System Verification). Immediately, another menu is displayed: AUTOMATIC MODE MENU. Press the RETURN key again to select the DISPLAY OPTION menu. Press the RETURN key a third time, to start execution of the AUTOMATIC SYSTEM VERIFICATION tests. No further intervention is required.

Various "test running" messages for both the 8301 and 8501 are displayed while the verification tests are executing. The 8301 (including the 68000 Emulator Processor) is tested first, followed by the 8501. The diagnostic tests take a total of approximately ten minutes to execute. At the end of that time, the system terminal will display either of two messages:

```
SYSTEM VERIFICATION PASSED

        or

SYSTEM VERIFICATION FAILED
```

If the SYSTEM VERIFICATION FAILED message is displayed, refer to the 8301 Microprocessor Development Unit Service Manual and 8501 Data Management Unit Service Manual for information on performing exhaustive diagnostic troubleshooting.

This completes the functional test procedure for the 68000 Emulator Processor.

8540 INTEGRATION UNIT VERIFICATION

Procedure

1. If the 68000 Emulator Processor was factory-installed in your 8540, the 68000 Diagnostics PROM is already installed. If not, you'll have to insert the 68000 Diagnostics PROM into the 8540 Integration Unit. Refer to the 8540 Integration Unit Installation Manual for this procedure.
2. Make sure that the Mode Selector switch on the System Controller board is in its normal operating configuration: switch positions 0–2 and 4–7 set to 0, switch position 3 set to 1.
3. Power up the 8540.
4. After the 8540 has displayed its boot message on the system terminal, you're ready to run the 8540 ROM-Based Diagnostics.
5. At the system terminal, enter:

   ```
   > SEL DIAGS <CR>
   ```

   The system terminal will display the diagnostic greeting and the Run Mode Menu, as shown in Display 5-2.

As soon as the system terminal displays the diagnostic greeting message and RUN MODE MENU, press the RETURN key to select the AUTOMATIC MODE (System Verification). Immediately, another menu is displayed: AUTOMATIC MODE MENU. Press the RETURN key again to select the DISPLAY OPTION menu. Press the RETURN key a third time, to start execution of the AUTOMATIC SYSTEM VERIFICATION tests. No further intervention is required.

Various "test running" messages are displayed while the verification tests are executing. The diagnostic tests take a total of approximately ten minutes to execute. At the end of that time, the system terminal will display either of two messages:

```
SYSTEM VERIFICATION PASSED

        or

SYSTEM VERIFICATION FAILED
```

If the SYSTEM VERIFICATION FAILED message is displayed, refer to the 8540 Integration Unit Service Manual for information on performing exhaustive diagnostic troubleshooting.

This completes the functional test procedure for the 68000 Emulator Processor.

```
*********************************************
*   TEKTRONIX INC.                          *
*   8540 ROM-RESIDENT DIAGNOSTIC SYSTEM     *
*   VERSION X.X                             *
*   Copyright (C) 1981 Tektronix, Inc.      *
*********************************************

                RUN MODE MENU
                -------------

1 - AUTOMATIC MODE     *** default ***
2 - SELECT MODE
H - HELP

Type in desired mode    {<CR> or 1, 2, or H and <CR>}
```

Display 5-2

Section 6

ADJUSTMENT PROCEDURES

INTRODUCTION

This section tells how to adjust the 68000 Prototype Control Probe's Power Supply board.

PROTOTYPE CONTROL PROBE POWER SUPPLY CALIBRATION

The 68000 Prototype Control Probe's Power Supply board generates two regulated supply voltages: +4.9 Vdc and +5.2 Probe Vdc. The +4.9 Vdc supplies voltage for much of the Interface Assembly circuitry. The +5.2 Probe Vdc is used only by the 64-Pin Plug. Both of these voltages are adjustable and may require occasional calibration.

Equipment Required

- TEKTRONIX microcomputer development system, with the 68000 Emulator Processor and Prototype Control Probe installed.
- DVM with 100 μV resolution and $\pm$0.1% accuracy (TEKTRONIX DM501 or equivalent).

Procedure

1. Make sure that primary power (115 Vac or 230 Vac) to the development system is OFF.
2. Remove the four screws at the corners on the bottom of the Interface Assembly housing.

CAUTION

The Power Supply board is mounted to the top cover of the Interface Assembly. The Power Supply board is connected to the main housing by four ribbon cables. Be careful not to damage these cables when you remove the top cover.

3. Remove the top cover of the Interface Assembly and set it beside the main housing (see Fig. 6-1).

NOTE

Do not disconnect any of the interconnecting ribbon cables.

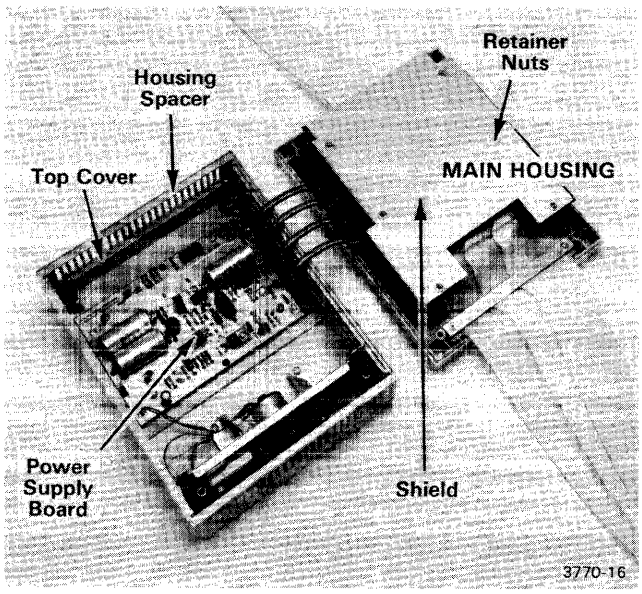


Fig. 6-1. Access to Power Supply board.

NOTE

For the remainder of this procedure, refer to Fig. 6-2.

4. Connect the negative (–) test probe of the DVM to GROUND (any one of the four Power Supply board mounting screws).
5. Connect the positive (+) test probe of the DVM to TP1061 on the Power Supply board (see Fig. 6-2).
6. Turn on the DVM and the microcomputer development system.
7. At the system terminal, enter the following command:

   >SEL 68000 <CR>

8. Observe the voltage measured by the DVM.
9. Adjust R1051 on the Power Supply board, until the DVM reads +4.9 Vdc, ±20 mV (+4.88 Vdc to +4.92 Vdc).
10. Disconnect the positive (+) test probe of the DVM from TP1061.
11. Connect the positive (+) test probe of the DVM to TP1011 on the Power Supply board (see Fig. 6-2).
12. Observe the voltage measured by the DVM.
13. Adjust R1011 on the Power Supply board, until the DVM reads +5.2 Vdc, +50 mV/–.2V (+5 Vdc to +5.25 Vdc).
14. Turn off power to all equipment.
15. Disconnect the DVM from the Power Supply board.
16. Reassemble the Prototype Control Probe Interface Assembly in reverse order of disassembly.

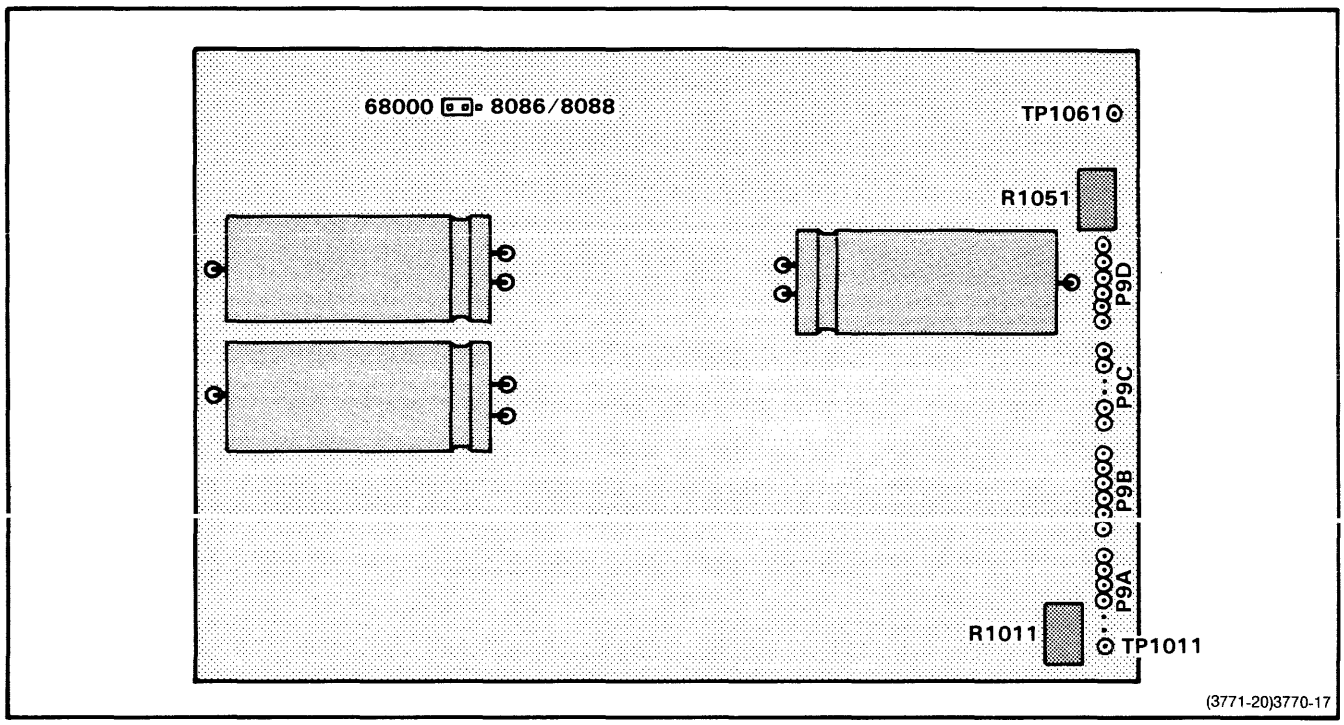


Fig. 6-2. Power Supply board.

Section 7

PERFORMANCE CHECK PROCEDURES

INTRODUCTION

After you have installed the 68000 Emulator Processor and Prototype Control Probe in your microcomputer development system, the Emulator Processor should be tested for proper operation. The first part of this section discusses equipment necessary to verify functional operation of the 68000 Emulator Processor and its associated Prototype Control Probe. The second part of this section discusses equipment necessary to verify timing relationships of signals available at the Prototype Control Probe pins. And the third part of this section contains diagnostic information specific to the 68000 Emulator Processor and Prototype Control Probe.

PERFORMANCE VERIFICATION

Equipment Required

To verify functional performance of the installed 68000 Emulator Processor, the following equipment is required:

- TEKTRONIX MicroLab I (067-0892-xx)
- 68000 Personality Card (018-0181-xx)

The MicroLab I checks the 68000 Emulator Processor and Prototype Control Probe by providing a circuit with known characteristics. This circuit is monitored by MicroLab I circuitry, and test results are indicated on the MicroLab I's LED display. The MicroLab I operating system also contains tests that functionally exercise the Emulator Processor and its probe.

The information presented in this section assumes that you are familiar with the MicroLab I and its characteristics. For more information about this equipment, refer to the MicroLab I Instruction Manual (with the 68000 Personality Card supplement).

Test Procedures

Equipment Setup

1. Ensure that primary power (115 or 230 Vac) to the microcomputer development system and to the MicroLab I is OFF.
2. Verify that jumpers P4 and P5 are correctly installed on the 68000 Personality Card (see Fig. 7-1). For more information on 68000 Personality Card jumpers, refer to the Jumpers discussion in the 68000 Personality Card supplement.
3. Install the 68000 Personality Card in the MicroLab I.

NOTE

To ensure a secure mechanical and electrical connection between the Prototype Control Probe's DIP plug and the zero-insertion-force (ZIF) socket on the personality card, you should attach a standard low-profile DIP circuit board socket (64-pin) to the probe plug.

4. Plug the 68000 Prototype Control Probe's DIP plug into the ZIF socket on the 68000 Personality Card.

Functional Test Procedure

1. If you have not already done so, perform the Equipment Setup procedure described earlier in this section.
2. Turn on primary power to the microcomputer development system.
3. Turn on power to the MicroLab I test fixture.

NOTE

For detailed information on operating procedures for your microcomputer development system, refer to your System User's Manual.

4. Start up (boot if necessary) the operating system of your development system.
5. At the system terminal, when the prompt character (>) is displayed, enter:

```
>SEL 68000 <CR>
```

   This identifies the Emulator Processor and Prototype Control Probe to be tested.

6. Enter the desired emulation mode:

```
>EM 1 <CR>
```

7. To verify memory mapping capability, enter:

```
>MAP U 0000 0FFFF <CR>
>MAP UR0 SP:SD:0000 1FFF <CR>
```

8. To verify breakpoint capability, enter:

```
>BK 1 02F8 <CR>
```

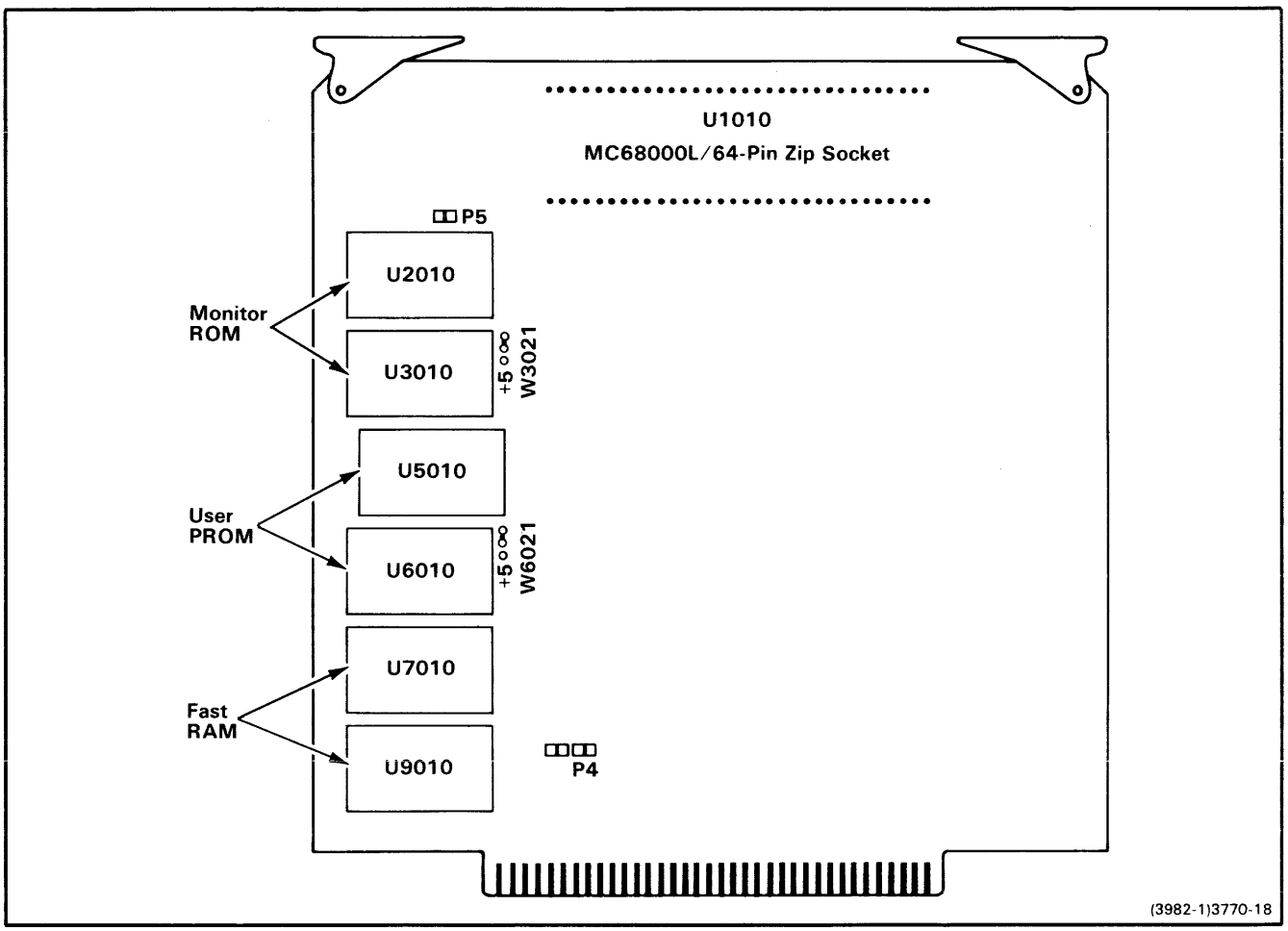


Fig. 7-1. 68000 Personality Card jumper and strap locations.

9. Initialize the MicroLab I by entering:

```
>RESET <CR>
```

10. To begin program execution in the Emulator Processor, enter:

```
>G <CR>
```

If the 68000 Emulator Processor and Prototype Control Probe are operating properly, the MicroLab I will display "HELLO".

11. Press the MicroLab I INC key twice to trigger the breakpoint.

The Emulator Processor displays the breakpoint information on the system terminal. Program Counter will contain 0002FC with A2 equal to 000002F8.

The "HELLO" display on the MicroLab I, and the breakpoint information on the terminal indicate that most of the 68000 Emulator Processor logic is functioning properly. However, several control lines are not checked during initialization and should be verified with the Processor Test, described later in this section.

No "HELLO" Display

If the MicroLab I LEDs do not display "HELLO", a problem is indicated in the 68000 Emulator Processor module, the Prototype Control Probe, or the MicroLab I. You can use the following procedure to determine which unit is malfunctioning:

1. Turn off power to the MicroLab I and to the microcomputer development system.
2. Disconnect the Prototype Control Probe from the ZIF socket on the 68000 Personality Card.

NOTE

The 68000 microprocessor device is subject to damage by static discharge when not installed in its socket. Be careful when handling this device; hold it by its ends only and do not touch the pins. When the device is not in use, it should be stored in its conductive foam packing.

3. Obtain a 68000 microprocessor device that is known to be operating properly. Install the device in the ZIF socket on the 68000 Personality Card.
4. Turn on power to the MicroLab I test fixture.

If the MicroLab I now displays "HELLO", the problem is in either the Emulator Processor module or the Prototype Control Probe. Refer to the Diagnostics discussion, later in this section, for corrective maintenance information.

If "HELLO" is not displayed, a malfunction is indicated in the MicroLab I. Refer to the MicroLab I Instruction Manual for corrective maintenance information.

Processor Test Procedure

1. If you have not already done so, perform steps 1–5 of the Functional Test Procedure, described earlier in this section.
2. At the system terminal, enter:

   ```
   >EM 2 <CR>
   ```

3. To initialize the MicroLab I, enter:

   ```
   >RESET <CR>
   ```

4. To initiate program execution in the Emulator Processor, enter:

   ```
   >G <CR>
   ```

5. Press the RESET key on the MicroLab I keypad. This initializes the processor test hardware in the MicroLab I.
6. Press the Shift key, then the 1 key (PROC TEST), to start the Processor Test function. The display will show "Pn".
7. Press the 0 key. The MicroLab I begins the Processor Test sequence at PROC 0 and performs each of the Processor Tests in order. While each test is being performed, the display shows "Proc x" (where x is the number of the test being performed).

Three Processor Tests (PROC 0–PROC 2) are used for testing the 68000 Emulator Processor with its Prototype Control Probe installed.

PROC 0 checks the BERR line. When the test begins, "PROC 0" will be displayed. If the test is completed successfully, then PROC 1 is executed next. If the line is open or tied high, then 'Error P0' is displayed.

PROC 1 tests Bus Arbitration (Bus Request (BR), Bus Grant (BG), and Bus Grant Acknowledge (BGACK)). When the test begins, "PROC 1" is displayed. If the BR(L) line is open or tied high, then "Error P1" is displayed. If the BR(L) test is competed successfully, then "PRES ANY" is displayed, and you must check the 68000 Prototype Control Probe's Interface Assembly LEDs as follows:

If the BG(L) LED **is not** lit, then the BG(L) line is open or tied high. Note that the BGACK(L) LED has not been tested yet and is also **not** lit.

If the BGACK(L) LED **is not** lit and the BG(L) LED **is** lit, then the BGACK(L) line is open or tied high.

If both the BG(L) and BGACK(L) LEDs are lit, then press one of the hexadecimal keys (0–F) located on the MicroLab I.

PROC 2 is executed next.

PROC 2 tests the Autolevel Interrupt levels (3–7). When the test begins, "PROC 2" is displayed, followed by "IN= 7". You must then press the SPECIAL key. If the test is executed successfully, then the next level interrupt is displayed and you must press the SPECIAL key again. If any of the interrupt lines (IPL0–IPL2) are not functioning properly, then the monitor will hang or "Error P2" will be displayed. Note that this test requires you to press the SPECIAL key a total of five times, decrementing from interrupt levels seven to three.

If all the PROC tests are successfully completed, the LED display indicates "rEAdY".

Successful completion of both the Functional Test and the Processor Test procedures verifies that the 68000 Emulator Processor and Prototype Control Probe are operational.

EMULATOR TIMING VERIFICATION

You may occasionally want to verify timing relationships between the signals available at the pins of the Prototype Control Probe. The following paragraphs discuss equipment necessary to perform these timing verifications.

Details of these timing relationships are provided in the 68000 Emulator Specifics section of your System Users Manual.

Measurement Considerations

Verifying the timing relationships of Emulator Processor signals involves the measurement of very small time increments. Test equipment used for these measurements should be able to resolve timing differences between two signals of 5 ns or less. A resolution of 1 ns is preferred for verification of the most critical timings.

Be careful that errors are not introduced with the test equipment being used. Test equipment calibration should be checked carefully. If you are using a dual trace oscilloscope, rather than a dual beam model, be sure to account for any possible skew between the two input channels. In general, good laboratory measurement practices should be followed to ensure accurate measurement of these timing relationships.

Equipment Required

To measure timing relationships with the preferred accuracy and resolution, the following equipment may be used:

- TEKTRONIX 7844 Dual Beam Oscilloscope, or equivalent
- Two TEKTRONIX 7A26 Vertical Amplifiers, or equivalent
- TEKTRONIX 7B85 Delaying Time Base; or equivalent

Controlling the Signal Lines Under Test

Some processor signal lines, such as interrupt lines, are normally connected to asynchronous circuits. Timing relationships of these asynchronous signals may be difficult to measure with an oscilloscope. To exercise these signal lines in a periodic manner, you may find it necessary to develop software routines, or use an external test fixture such as the TEKTRONIX MicroLab I.

DIAGNOSTIC TESTING

Each time you install the 68000 Emulator Processor in your microcomputer development system, system verification checks should be performed. Emulator Processor diagnostics are run automatically as a part of the system diagnostic test program. Procedures for running this diagnostic test program are included in your microcomputer development system's Installation Guide.

The diagnostics allow you to verify operation of the 68000 Emulator Processor and the 8500-Series Emulator Controller board. The following text describes the 68000 Emulator Processor diagnostics in detail. Note that the descriptions are divided into the following two major headings:

Test Descriptions include general functional descriptions and error displays for the individual 68000 diagnostic test modules.

Test Module Specifics describe in detail the operation of the individual 68000 diagnostic test modules.

The 68000 Emulator Processor diagnostics function as a sub-set of the 8550 disk-resident diagnostics or 8540 ROM-resident diagnostics. (For the 8540, the 68000 diagnostics ROM must be installed.) That is, the 68000 diagnostics are selected and run from within the operating system's executive diagnostics. This text will not describe how these executive diagnostics are loaded and executed. For a complete description of the applicable diagnostics, see the service manual for your development system.

If the diagnostics are run in Automatic Mode, the software will determine which emulator processor is installed, and run the appropriate diagnostics.

If the 68000 Emulator Processor diagnostic program is selected, but a 68000 Emulator Processor is not installed, error code 0E/0000 will be displayed. If the diagnostics display this error code, verify that you selected the correct diagnostic program.

Diagnostics Overview

The 68000 Emulator Processor diagnostics are menu-driven. You select test, error loop, and display options prior to running a specific test group, and the options remain in effect until you abort the test by entering ESC, CTRL-C, or BREAK. The following paragraphs describe the test option selection sequence.

When the 68000 diagnostics are selected, you are presented with a test option menu, as shown in Display 7-1.

```
                        OPTION MENU
                        -----------

0 - RUN ALL                              *** default ***
1 - I/O PORT & RAM TESTS
2 - DUMP/RESTORE LOGIC TESTS
3 - EMULATION MODE 0 TESTS
4 - BREAKPOINT TESTS
5 - SVC TESTS
6 - WRITE PROTECT/MEMORY MAP TESTS
7 - 68000 CPU TEST
8 - TTA INTERFACE TEST
9 - MAC INTERFACE TEST
T - SPECIFIC TEST
H - HELP

Type in desired option number, H or T with <CR>
```

Display 7-1

NOTE

Test options 8 and 9 are executed only if the TTA and MAC options are installed in your development system.

Test Option Selection

Each test option is made up of one or more "test modules" (individual tests) which are described later. When you select a test option, the 68000 diagnostics run all of the test modules within that option.

For example, if you select option 0 (the RUN ALL option), all test modules are executed. If the 68000 Emulator Processor passes a module, the diagnostics go on to the next module. If an error is detected, the diagnostics may loop on that module, or go on to the next, depending on the looping option you select.

if you type H, the diagnostic program will display a help message that lists all the individual test modules and their test numbers (see Display 7-2).

Test Module Selection

If you type T, the diagnostic program will prompt you to enter a two-digit module number and <CR>, to select a SPECIFIC TEST module to run. The test modules are listed in the Help Option Menu.

It is recommended that you use the RUN ALL option in order to gain the broadest overview of the faulty boards, and then employ the SPECIFIC TEST option to repeat the test program(s) most useful in troubleshooting your system.

```
                HELP OPTION MENU
                ----------------

OPTION--TEST MODULE
-----------------------------------
0       All Modules 00-90        *** default ***
        00 - EMU Detection Test
1       10 - EMU Activation Sequence Test
        11 - Clock Fail Detection Test
        12 - Auxiliary Port Test
        13 - Command Port Test
        14 - RAM INHIBIT Test
        15 - UMAP/Write Protect RAM Test
        16 - BKPT/SVC RAM Test
        17 - Shared Communication RAM Test
2       20 - Invalid Command Test
        21 - Shared RAM Access Test
        22 - UMAP/BKPT RAM Access Test
        23 - Register Restore/Dump Test
        24 - D/R ROM Routines Completion Test
3       30 - SLVPAUSE/RUN Line Test
        31 - RUNUSER Test
        32 - Single Cycle Test
        33 - AO Write Test
        34 - STOP Instruction Test
        35 - Address Fault Test
        36 - Halt Condition Test
4       40 - BKPT1 Test
        41 - BKPT2 Test
        42 - BKPT3 Test
        43 - BKPT1 Arms 2 Test
5       50 - JMP ACK/SVC INHIBIT Test
        51 - SVC Operational Test
6       60 - Write Protect Test
        61 - Memory Map Test
7       70 - 68000 CPU Test
8       80 - TTA Interface Test
9       90 - MAC Interface Test
T - Run 1 TEST MODULE from this list instead of OPTION test group

Type in desired option number, H or T with <CR>
```

Display 7-2

```
                    ERROR LOOP CONTROL MENU
                    -----------------------

1 - LOOP ON ERROR / CONTINUE IF PASS     *** default ***
2 - LOOP ON ERROR UNTIL RESET
3 - DO NOT LOOP ON ERROR - CONTINUE

Type in looping selection {<CR> or 1 - 3 and <CR>}
```

Display 7-3

```
                        DISPLAY MENU
                        ------------

  1 - DISPLAY ON TERMINAL              *** default ***
  2 - DISPLAY ON TERMINAL & J103 AUX PORT PRINTER
  3 - NO DISPLAY

  Type in display option {<CR> or 1 - 3 and <CR>}
```

Display 7-4

```
OPTION 01  MODULE RUNNING=12  ITERATION # 000D  ERRORS=0000
```

Display 7-5

Error Loop Option Selection

Each test option prompts you to select an error loop option. Display 7-3 shows the Error Loop Control Menu.

Each test module is broken down into loops, so that the entire test need not be repeated to isolate an error.

Error loop option 1. The default option. The test being run loops only as long as an error condition exists.

Error loop option 2. If an error is detected, the test being run loops until you enter ESC or CTRL-C.

Error loop option 3. Continues on to the next test, even if an error is detected. Error loop option 3 is useful in order to gain an overview of the failure states.

Display Option Selection

You will also be prompted to select from three display options, as shown in Display 7-4.

Display option 1. The default option. All messages are displayed on the terminal only.

Display option 2. Messages are displayed on the terminal and are sent to a line printer connected to Auxiliary Port, J103.

Display option 3. No messages are displayed. This display option decreases scope loop delays.

As the diagnostics are running, a display showing the test module number, the iteration number, and the number of errors is shown on the system terminal. Display 7-5 is an example of the display caused by the Auxiliary Port test execution. The RUN ALL option will be executed as option 00.

The **Module Running entry** contains the number of the test module currently executing. If SELECT MODE has been utilized to run the 68000 diagnostic test program, the Module Running message will sequence through the tests in the option list selected, then repeat the sequence until interrupted by a keyboard ESC or BREAK character.

The **Iteration count** represents the number of times that the selected test sequence has been completed. The **Error count** is incremented whenever an error is detected during test execution and is cumulative. Both the Iteration and Error counts are displayed as hexadecimal numbers.

The error display formats are unique to the type of testing being performed. These error displays are described in the individual test module descriptions. Table 7-1 is a list of System Interrupt codes which may appear in the error display.

Table 7-1
System Interrupt Definitions

INTRPT	Definition
01	System Memory Error
02	Write Protect Violation
03	Program Parity Error
04	HSI Interface Input
05	HSI Interface Output
06	Remote Port ACIA
07	Auxiliary Port ACIA
10	System Port ACIA
11	Interval Timer
12	DMA Interrupt
13	Flexible Disc Interrupt <manufacturing test>
14	(not assigned)
15	PROM Programmer Data Interrupt
16	PROM Programmer Status Interrupt
17	(not assigned)
20-27	SVC1-SVC8
30	BKPT1 (Emulator Controller)
31	BKPT2 (Emulator Controller)
32	Single Cycle (Emulator Controller)
33	SLV HLT Interrupt
34	Diagnostics Interrupt <diagnostic front panel>
35	<INT29 (TTA)>
36	<INT30>
37	<INT31(MAC)>

The 68000 Emulator Processor contains on-board breakpoints (1, 2, and 3). The breakpoint values given in the error displays represent the Emulator Processor's breakpoint values and not those of the System Controller.

Diagnostic Program Overview

The following text provides a program overview of the 68000 Emulator Processor diagnostics. Each test group name is preceded by the option number (1–9) that you use to select that test group. (Option number 0, however, selects the RUN ALL option, rather than selecting only the Emulator Detection Routine to run as an individual option.) Each test module within a test group is listed by its test number.

The 68000 diagnostic program consists of nine test groups that are broken down into four separate areas.

In **Test Group 1,** the 68000 Emulator Processor is activated and its reset is cleared. However, no commands are issued to the 68000 microprocessor and no operational tests are performed. Test Group 1 concentrates on the I/O Port, memory, and control line verification.

In **Test Group 2,** the 68000 Emulator Processor executes various Dump and Restore (D/R) ROM utilities without executing the Run User utility. Test Group 2 functionally tests the Emulator Processor without allowing the 68000 microprocessor to access the system bus.

In **Test Groups 3–7,** the 68000 microprocessor executes the RUNUSER command and gains access to the system's resources.

In **Test Groups 8 and 9,** the Trigger Trace Analyzer (TTA) and Memory Allocation Controller (MAC) board interfaces are verified. Test Groups 8 and 9 are executed only if the TTA and MAC are installed in your development system.

NOTE

Breakpoint RAM, Write Protect RAM, and Program Memory are initialized before Test Groups 3–9 are run. The 68000 microprocessor's exception/interrupt vector space (0–03FF) is loaded with 0000 04FE (which points to a Branch to Self instruction). The remainder of Program Memory is filled with Branch to Self instructions.

The test sequencer has been designed to deactivate and reactivate the Emulator Processor between each test. Power is left turned on to the Interface Assembly, unless the reset sequence is specifically being tested. The reactivation sequence ensures that each test is being started from a common base (that is, the microprocessor will be in the Supervisor state).

Test Descriptions

The following text gives a general description of the test modules and error displays used by the 68000 Emulator Processor diagnostics. The Test Module Specifics discussion, later in this section, describes in detail the operation of each test module.

In the following test module descriptions, some sample error displays contain data in the EXPECTED column that is not used as a test criteria for successful completion. Consult the Test Module Specifics to determine what is required for successful test completion.

Some test modules are run several times for a particular test option. In this case, expected values may change with each test pass, and are displayed as "**" or "****". Consult the individual test descriptions to determine the individual test pass's expected values.

Test Group 0 Emulator Detection

0E/0000—EMU Detection Test. This test verifies that the 68000 Emulator Processor has been properly installed. This is the first test executed only when RUN ALL is selected.

Description. The EMU Status Port (AD) has four defined bits:

- D4—HALTED
- D2—EMU RESET REQ
- D1—CLKFAIL
- D0—HAVE RUN

The Emulator Processor is powered down, and the EMU RESET REQ bit should be reset high, indicating that the Emulator Reset sequence must be performed. When the EMU Status Port is read, the unused bits are masked off, and a non-zero condition indicates that the 68000 Emulator Processor is installed. In particular, the EMU RESET REQ bit is relied upon to indicate that the Emulator Processors is present. However, any other defined bit that is asserted also allows the test to pass.

Error Message. See Display 7-6.

Test Group 1 I/O Port And RAM Tests

Test Group 1 tests the 68000 Emulator Processor without requiring the 68000 microprocessor to be operational. It therefore represents the smallest emulator kernel that can be tested by the system processor. This test group exercises the Emulator Processor's I/O ports, on-board memory, and selected control lines.

Only the Command Port allows (partial) direct read-back verification, so the EMU Control and AUX Control Ports are tested through specific control line verification tests. Because some control line verification tests require that the Emulator Processor be operational, these tests are executed in each test group that includes operational testing. Only a select group are included in Test Group 1. The following is a list of status lines that are **not** tested (while asserted) in Test Group 1:

EMU Status Port (AD)

- HAVE RUN (see RUNUSER Test, 0E/0031)
- HALTED (see HALT Condition Test, 0E/0036)

AUX Status Port (8E)

- STOP (see STOP Instruction Test, 0E/0034)
- BKPT1 (see BKPT1 Test, 0E/0040)
- BKPT2 (see BKPT2 Test, 0E/0041)
- BKPT3 (see BKPT3 Test, 0E/0042)
- INT29 (see TTA Interface Test, 0E/0080)
- WRPROT INT (see Write Protect Test, 0E/0060)

Command Port (8F or 1001)

- MISSED NMI (not tested in asserted state)

In addition, the AUX Control Port's (8E) Forced Function Code lines FFC0–FFC2 are not used in Emulation Mode 0, and therefore, are not tested in this diagnostic program.

```
>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<

                                        Error Code = 0E/0000

EMU Detection Test

68000 EMULATOR NOT DETECTED

----------------------------------------
PRIMARY SUSPECT  = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-6

Test Group 1 is designed to initialize a port prior to individual control line testing of that port. The initialization tests have been included to test for port accessibility and to detect stuck status bits that could cause misleading error displays in subsequent tests. Consult the test description sections for specific initialization procedures, because different initialization procedures are required for various status bits. Specific control line tests contain provisions to both assert and deassert the control lines being tested. In this way, port initialization is effectively tested twice; after the power-up sequence and in simulation of normal Emulator Processor operation.

Many port functions, such as a Command Port read-back, cannot be tested until the 68000 microprocessor has been released from a reset condition (EMU ACTIVE bit asserted in the EMU Control Port). Therefore, the Emulator Processor's basic hardware kernel must also include the 68000 microprocessor, the shared resource arbitration logic, and supporting buffer circuitry. In the Test Module Specifics discussion, later in this section, the Key ICs lists include those components identified as primary sources of failure, The shared bus arbitration logic can also be the source of error for many of the tests in Test Group 1; however, those IC's are not specifically listed.

Test Group 1 concludes with a 2650 test of the 68000 Emulator Processor's on-board RAM. The memory tests make multiple passes through the memory array, reading and writing dissimilar test patterns. With each pass through memory, a new test pattern is loaded into the entire memory array. The existence of the old test pattern is verified before the next pattern is written. Thus both the data and address integrity of the RAM are tested. (Shorted address lines will be detected in the read before write phase.)

The LOOP ON ERROR and LOOP UNTIL RESET options produce the tightest scope loops, with the test repeating after the first occurrence of an error. The DO NOT LOOP, CONTINUE option displays all errors detected within any given pass, with the first occurrence listed in the primary error display, and subsequent errors listed in a secondary display. The DO NOT LOOP, CONTINUE option can thus be used to obtain failure pattern information, which is helpful during shorted address line troubleshooting. If errors are listed in the secondary display, a random memory failure has probably occurred (rather than the pattern failure expected with a buffer or memory chip failure).

Test Group 2 continues to test the Emulator Processor by executing "non RUNUSER" commands to the 68000 microprocessor kernel. Both Test Group 1 and 2 perform tests that do not halt the System Processor (2650).

0E/0010—EMU Activation Sequence Test. The Activation Sequence test verifies that the Emulator Reset sequence logic is operational. The Emulator Processor is powered up and activated, and the EMU Status Port checked for a low in the EMU RESET REQ bit (D2). Therefore, two bits are tested in the EMU Control Port, PROBEPWR (D7) and EMU ACTIVE (D2), and one bit is tested in the EMU Status Port, EMU RESET REQ (D2).

Description. Successful completion of the reset sequence determines whether the Emulator Processor's DLYD ACTIVE signal is asserted or deasserted. Therefore, if this test fails, all of the other tests in the 68000 diagnostic program might be invalidated (unless the problem is specifically with the EMU Status Port, U2060).

The Emulator Processor asserts the EMU Status Port's EMU RESET REQ bit high whenever the Emulator Processor's Interface Assembly is powered down. The EMU RESET REQ bit should be cleared after EMU Control Port's EMU ACTIVE bit is asserted. Note that Test Group 3 contains tests for the EMU Status Port bits HALTED (D4) and HAVE RUN (D0) (in their asserted state).

Error Message. See Display 7-7.

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0010

EMU Activation Sequence Test

EMU STATUS PORT (AD)
ACTUAL   = **
EXPECTED = **

----------------------------------------
PRIMARY SUSPECT  = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-7

0E/0011—Clock Fail Detection Test. The Clock Fail Detection test verifies that the Emulator Processor's clock fail detection circuitry is operational. The EMU Status Port's CLKFAIL bit (D1) is also tested.

Description. This test assumes that the 64-Pin Plug does not have a clock source connected to it. The Emulator Processor is forced into Emulation Mode 2, where it would normally expect a prototype circuit clock source to be available. However, since no clock source is connected, the CLKFAIL bit (D1) should be asserted in the EMU Status Port. To complete the test, Emulation Mode 0 is reselected, which should clear the CLKFAIL bit.

Error Message. See Display 7-8.

0E/0012 - Auxiliary Port Test. The Auxiliary Port test verifies that the AUX Status Port (8E) can be initialized properly, and that the S/CY EN bit (Single Cycle Enable) can be set in the AUX Control Port (8E). This test also verifies that the status of the AUX Control Port's S/CY EN bit can be read back through the AUX Status Port's S/CY ACTIVE bit.

Description. The AUX Status Port can only be accessed via the Shared Data Bus. Therefore, this test must fully activate the Emulator Processor to guarantee that the Shared Data Bus arbitration logic is active. Bits D0–D5, of the AUX Status Port, are reset high when this port is read. (Note that the AUX Status Port is inverted.) This means that the port is read twice—once to reset and once to test.

Note that the EMU Status Port's bit D7 is pulled high. This is so that a port access failure can be detected by a low in D7.

The S/CY EN bit is the only AUX Control Port bit with direct read-back capabilities through the AUX Status Port. Three read-backs must be performed to verify that the S/CY EN (in the AUX Control Port) and S/CY ACTIVE (in the AUX Status Port) can be asserted and deasserted.

Error Message. See Display 7-9.

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0011

Clock Fail Detection Test

EMU STATUS PORT (AD)
ACTUAL    = **
EXPECTED  = **

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
SECOND  SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-8

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0012

Auxiliary Port Test

AUX STATUS PORT (8E)
ACTUAL    = **
EXPECTED  = **

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-9

0E/0013—Command Port Test. The Command Port test verifies that the Emulator Processor's Command Port (8F) is initialized properly after the Emulator Processor has been activated, and that bits D1–D5 can be written to and read back.

Description. The Command Port has three parts that are inspected during this test.

The first part tests the SLV PAUSE (read-back) bit, D0. This bit is essential for the RUNUSER command synchronization between the development system and 68000 microprocessor. Only the assertion state can be directly tested by the 2650, since SLV PAUSE is always asserted while the 2650 is running. The RUNUSER test (Test Group 3) tests the deassertion state.

The second part tests the MISSED NMI bit, D6. This bit can be asserted only when the Emulator Processor is operating in Emulation Mode 1 or 2 and the prototype circuit asserts a specific interrupt sequence during an Emulator Processor break or trace operations. The MISSED NMI assertion state is not tested in this diagnostic program. However, this test does verify that the Missed NMI latch can be reset through the deactivation of the Emulator Processor or by writing a 1 to bit D6.

The third part concerns command transfer (data bits D1–D5 and D7). Although writing to the Command Port involves access via the Shared Data Bus, the Command Port can be read by the 2650 through only one dedicated buffer (U2050). The Emulator Processor must be "Active" (Selected) and MSTRRUN(L) asserted to get access to the Command Port (8F), however the port can be read by the 2650 even though the 68000 microprocessor has control of the Shared Data Bus. This test verifies that the CMD PRESENT bit (D7) has been cleared in the Command Port immediately after a power-up sequence. The COMMAND (code) bits, D1–D5, are tested using write/read test patterns (see Test Module Specifics, later in this section).

The third part continues with a write function, which requires the Shared Data Bus Arbitration logic to be functioning properly. CMD PRESENT(H) is the key signal employed by the arbitration logic and remains deasserted for the duration of this test. The asserted state of CMD PRESENT (D7) is not verified in this test, since the test is not intended as an operational check (refer to Test Group 2).

Error Message. See Display 7-10.

0E/0014—RAM INHIBIT Test. The RAM INHIBIT test verifies that the 68000 Emulator Processor's RAMINH(L) line is operational.

Description. The Emulator Processor's RAMINH(L) line is used as a Program Memory de-select line. When the Emulator Processor's Shared Communication RAM is mapped into the Program Memory space and the 2650 accesses the Emulator Processor's memory, RAMINH(L) low, prevents Program Memory from responding. RAMINH(L) is activated via the RAMEN (RAM Enable) bit in the Emulator Processor's EMU Control Port (D1), since RAMINH(L) is active only when the RAMEN bit is asserted.

This test verifies the operation of RAMINH(L) both within and outside of the Emulator Processor's RAM address range. Data integrity of the Emulator Processor's RAM is not verified in this test, so the value written to the Emulator Processor is not read back. (See tests 0E/0015, 0E/0016, and 0E/0017 for Emulator Processor RAM verification.) Note that since address line A15(L) and CMEM(H) are factored into the access equation, the RAMINH(L) signal should be asserted by the Emulator Processor only during access of Program Memory, 8000–FFFF. Note also that CMD=0(H) has also been factored into the equation. Thus RAMINH(L) is asserted only when no commands are present in the Command Port.

NOTE

Program Memory operation is assumed to have been verified by the general system tests, prior to execution of the 68000 diagnostic program.

Error Message. See Display 7-11

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0013

Command Port Test

COMMAND PORT (8F)
ACTUAL   = **
EXPECTED = **

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-10

0E/0015—UMAP/Write Protect RAM Test. The UMAP/Write Protect RAM test verifies the integrity of the 68000 Emulator Processor's UMAP/Write Protect RAM.

Description. The UMAP/Write Protect RAM are implemented in separate memory chips, but share a common selection logic and are tested together.

This is a 2650 access test of the UMAP/Write Protect RAM, and should be used with Test Group 2 (verifying that the 68000 microprocessor cannot corrupt the UMAP/Write Protect memory) and Test Group 6 (testing for complete verification of the RAM, including operational functioning).

This RAM is implemented as 2 bits wide, with SD0 for the Write Protect function and SD1 for the UMAP function. RAM is mapped into the Program Memory space from C000-FFFF after the RAMEN bit (D1) in the EMU Control Port has been set. Since access to the memory is via the Shared Buses only, the CMD=0 signal is significant in allowing the 2650 access. During the second memory pass, this test performs a read verify prior to a write at each location. Thus both address and data integrity are tested. You can specify the DO NOT LOOP, CONTINUE option, to read all errors detected within each memory pass.

Error Message. See Display 7-12

0E/0016—BKPT/SVC RAM Test. The BKPT/SVC RAM test verifies that the Emulator Processor's Breakpoint RAM is operational.

Description. The Breakpoint (BKPT) and Service Call (SVC) functions share common memory and selection logic. Therefore, their RAM circuitry is tested together. This is a memory test only. (See Test Groups 4 and 5 for operational testing.)

The BKPT/SVC RAM is mapped from 8000–83FF and is four bits wide. D3 is used for SVC's and D0–D2 for BKPTs. Since this memory is accessed via the Shared Data Bus, CMD=0 is significant in allowing the 2650 access. The DO NOT LOOP, CONTINUE option should be used to display all of the errors that occur during one memory pass.

The memory passes were chosen to ensure that both the data and address integrity of the memory is adequately tested (see Test Module Specifics, later in this section). Since the data read-back from the memory is via multiplexers (U4070, U4090), the memory test has been broken down into four groups, to ensure that multiplexer failures can be detected. This test performs three passes through memory: one write only, one read then write, and one read only.

Error Message. See Display 7-13.

```
>>>>>>>>>>>>>>>> DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                    Error Code = 0E/0014

RAM INHIBIT Test


----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-11

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                    Error Code = 0E/0015

UMAP/Write Protect RAM Test

FAILURE LOC= C000 EXPECTED DATA= 01 ACTUAL (MASKED) DATA= 00

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-12

0E/0017—Shared Communication RAM Test. The Shared Communication RAM test verifies that the Emulator Processor's Shared Communication RAM is operational. This is a memory test from the 2650 side only (see Test Group 2 for a write test originating from the 68000 microprocessor).

Description. The Shared Communication RAM is mapped into the Program Memory space from A000-A7FF. The Shared Communication RAM consists of two banks of 4-bit wide memory. This test accesses the memory from the Shared Data Bus, and is therefore affected by the condition of the CMD=0(L) signal.

This test makes four passes through memory, each pass consisting of one write and one read verify. Both the data and address integrity of the RAM are tested. Refer to Test Module Specifics, later in this section, for test pattern information.

The 2650 accesses the Shared Communication RAM eight bits at a time. The 68000 microprocessor performs a word access. Therefore, this test can be used to verify memory, but Test Group 2 must be run to verify the high order data byte buffer (U6200) from the Shared Data Bus.

Error Message. See Display 7-14.

Test Group 2 Dump/Restore Logic Verification

Test Group 2 exercises the 68000 Dump/Restore (D/R) PROM routines and associated logic, with the exception of the RUNUSER command. The RUNUSER command has been excluded in an effort to confine testing to the shared resources of the Emulator Processor, without allowing the 68000 microprocessor to access the Program Memory space. Since the 68000 microprocessor executes the D/R routines (except RUNUSER) in parallel with 2650 execution, the 2650 is not halted during these tests.

Communication between the two processors is arbitrated through the Emulator Processor's EMU Command Port. Writes to this port are arbitrated between the two processors primarily through the state of CMD PRESENT. However, either processor is allowed to read the EMU Command Port (with a few 68000 exceptions) while the other has control of the Shared Bus area. Because the CMD PRESENT bit (D7) can be accessed by both processors at the same time, the software convention of requiring two successive reads before the deciding state is used.

The software access convention is especially important in light of the fact that mutual hardware exclusion to the Shared Data Bus is not guaranteed. Specifically, a read of the AUX Control Port (8E) or a write to the Command Port (8F) by the 2650 while the 68000 microprocessor has control of the Shared Buses (CMD=0 asserted with a com-

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0016

BKPT/SVC RAM Test

FAILURE LOC= 8000 EXPECTED DATA= 05 ACTUAL (MASKED) DATA= 00

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-13

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0017

Shared Communication RAM Test

FAILURE LOC= A000 EXPECTED DATA= AA ACTUAL (MASKED) DATA= 00

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-14

mand present) results in bus contention on the Shared Data Bus. (Refer to the D TO SD(L) signal and the 8F RD(L) signal on EMU 1 for details.) The 2650, therefore, accesses the Shared Buses only after it has determined that D7 in the Command Port is equal to zero on two successive reads. The system processor asserts D7 when it passes a command to the 68000 Emulator Processor, and the 68000 microprocessor clears the bit when it completes execution of the command. Each test in Test Group 2 uses a timeout wait loop when the 2650 polls the Command Port for deassertion of bit D7.

This test group does not contain a D/R PROM checksum test, because the Emulator Processor hardware design requires that an external hardware jumper be placed on the D/R address decoder PROM (in order to prevent a RUNUSER detection during the checksum verification process). The D/R PROM are therefore tested via a functional test of its routines.

NOTE

Even a hardware jumpered checksum test would require use of the EXECRAM routine of the D/R PROM, so the PROM must be at least partially operational before its checksum can be calculated by the 68000 microprocessor. The 2650 cannot gain direct access to the D/R PROM.

0E/0020—Invalid Command Test. The Invalid Command test verifies that the 68000 Emulator Processor's recognizes an invalid command from the 2650. Since the 68000 microprocessor need only read the Command Port and compare that value to the commands listed in the Dump/Restore PROM, this test represents a minimal test of the D/R PROM and the shared bus arbitration logic.

Description. The 68000 Emulator Processor begins polling the Command Port as soon as the port's reset is cleared during the Activation sequence. While the 68000 microprocessor is in a program loop (location 0434–043E) in the D/R PROM, bit D7 of the Command Port is tested for the presence of a valid command (CMD PRESENT, D7 = 1).

The test begins when the 2650 writes an invalid command to the Command Port and begins polling the Command Port for D7 to be cleared by the 68000 microprocessor. The 68000 senses that CMD PRESENT has been asserted after two consecutive reads, and compares the command to a list of reference commands in its D/R PROM. After determining that the command does not exist, the 68000 microprocessor should write 02 to the CMDSTAT in the Shared Communication RAM (location A054, as accessed by the 2650) and clear the Command Port. The 68000 then returns to its polling state. The 2650 detects the cleared command status and checks the CMDSTAT location for the proper value.

The basic hardware kernel being tested is of significant size. It includes the 68000 microprocessor and buffer circuitry in the Interface Assembly, the D/R PROM on the Emulator Processor, cable buffers, and the shared bus arbitration logic during the write to the CMDSTAT location in the Shared Communication RAM. (Consult the Test Group 2 introduction earlier in this section for more details on arbitration logic.)

The write operation to the CMDSTAT location tests the Emulator Processor's data bus buffer latch operation, via the DATA LAT EN(H) and ID TO SD(L) signals on EMU 1. The 68000 microprocessor generates a Data Strobe (DS) whenever writing to the Shared Data Bus or the System Data Bus (via the Shared Data Bus). Note the delay line included in the circuit on the Mobile Microprocessor board.

Error Message. See Displays 7-15 and 7-16. A timeout wait loop is used when the 2650 polls the Command Port, so that if CMD PRESENT (D7) never clears, Display 7-15 is displayed. The selected test sequence then continues. If an error is detected, Display 7-16 is displayed. Note that only one of these messages will be displayed.

0E/0021—Shared RAM Access Test. The Shared RAM Access test verifies that the 2650 is not allowed access to the Shared Communication RAM while the 68000 microprocessor is executing a command and has been granted control of the Shared Buses.

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0020

Invalid Command Test

68000 DID NOT RUN TO COMPLETION

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-15

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = OE/0020

Invalid Command Test

COMMAND STATUS BYTE
ACTUAL   = **
EXPECTED = 02

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-16

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = OE/0021

Shared RAM Access Test

68000 DID NOT RUN TO COMPLETION

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-17

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = OE/0021

Shared RAM Access Test

2650-RAM-ACCESS LOGIC FAILURE

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-18

Description. Both the Shared Bus arbitration logic, and the D/R PROM's diagnostic Execute from RAM command (EXECRAM) are tested. The 2650 attempts a write to the Shared Communication RAM while the 68000 is executing a Decrement and Branch to Self instruction. The 68000 should loop 256 times and then clear the Command Port. This effectively tests the Shared Data Bus arbitration logic (U4120).

The 2650 should see the deassertion of the Command Port's bit D7 and then attempt to regain the control of the Shared Bus by writing to a second location in the Shared Communication RAM. The 2650 checks that the second test location was modified, but that the first test location still contains its original reference value.

Error Message. See Displays 7-17 and 7-18. Display 7-17 is displayed if the 68000 did not clear the Command Port. Display 7-18 is displayed if the test locations did not compare correctly.

0E/0022—UMAP/BKPT RAM Access Test. The UMAP/BKPT RAM Access test ensures that the 68000 microprocessor cannot inadvertently modify its UMAP or BKPT RAM while executing code.

Description. Test patterns are loaded into the UMAP and BKPT RAM and the 68000 writes to both RAM areas. The D/R PROM utility EXECRAM executes the write test program located in the Shared Communication RAM space. The 2650 then checks that the RAM areas remain unmodified.

Error Message. See Displays 7-19 and 7-20. Display 7-19 indicates that the UMAP RAM was modified. Display 7-20 indicates that the BKPT RAM was modified. Note that only one of these messages will be displayed at a time.

0E/0023—Register Restore/Dump Test. The Register Restore/Dump test verifies that the register dump and restore routines in the D/R PROM are operational.

Description. The 68000 microprocessor restores its registers from the values stored in the Shared Communication RAM space. Since the registers are dumped back into the same RAM space, the RAM space is cleared between operations to ensure that the registers have been restored and dumped correctly.

The register test pattern is generated by filling the Register Save Area (A000–A046) with 01, 02, 03, etc. for the 68000 registers D0–D7, A0–A6, System Stack Pointer (SSP), User Stack Pointer (USP), and Status Register (SR). These values fill an area from A000 to A045 (2650 addressing). Note that each register is 32 bits wide and that the pattern used leaves the SSP with an even value. Any odd value would abort the register restore routine.

Error Message. See Displays 7-21 and 7-22. Display 7-21 indicates that a register was modified. Display 7-22 indicates that the SSP was modified to an odd value. Note that only one of these messages will be displayed at a time.

0E/0024—D/R ROM Routines Completion Test. The D/R ROM Routines Completion test verifies that the UGET, UPUT, and Readback routines in the Dump and Restore (D/R) PROM terminate properly and return control to the 2650. The functionality of the routines are not checked (the UGET routine cannot be verified while the Emulator Processor is operating in Emulation Mode 0).

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                      Error Code = 0E/0022

UMAP/BKPT RAM Access Test

MAP-RAM-WRITE LOGIC FAILURE

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-19

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                      Error Code = 0E/0022

UMAP/BKPT RAM Access Test

BKPT-WRITE LOGIC FAILURE

----------------------------------------
PRIMARY SUSPECT  =68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-20

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0023

Register Restore/Dump Test

ACTUAL    = **
EXPECTED  = **

----------------------------------------
PRIMARY SUSPECT  = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-21

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code  = 0E/0023

Register Restore/Dump Test

D/R ROM ROUTINE DID NOT RUN TO COMPLETION

----------------------------------------
PRIMARY SUSPECT  = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-22

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0024

D/R ROM Routines Completion Test

D/R ROM ROUTINE DID NOT RUN TO COMPLETION

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-23

Description. The D/R PROM (located on EMU 2) can be accessed only by the 68000 microprocessor. Therefore, a checksum test of the D/R PROM must be made by the 68000. However, the 68000 cannot perform a checksum test without causing the D/R PROM address decoder to detect a RUNUSER condition. D/R PROM can be verified only by executing the actual PROM routines.

Error Message. See Display 7-23.

Test Group 3 Emulation Mode 0 Verification

Test Group 3 is the first of four groups of tests that exercises the RUNUSER option in the Dump/Restore PROM. The RUNUSER command allows the Emulator Processor to execute code in the Program Memory or prototype memory space. However, Test Group 3 is confined to Program Memory execution only.

The RUNUSER command should produce the Emulator Processor's RUNNING(H) signal, which is instrumental in circuits utilizing the RUN(L) signal, bus drivers, activation of BKPT, SVC and Write Protect. The BKPT and Write Protect functions are active during all of Test Group 3's tests, even though they are not being tested directly.

The SVC's can be separately disabled via bit D6 in the Aux Control Port. The appropriate RAM elements for these functions are programmed for the don't-care state, and should therefore not affect the tests. However, since the detection logic is active once RUNUSER is executed, the RAM elements must be fully operational to guarantee that the BKPT and Write Protect Interrupts do not take place. Test Group 1 can be used to verify the RAM integrity. The BKPT circuitry IC's are not specifically listed in Test Group 3's Key ICs lists, but should be assumed if an error display indicates that they are the source of halting the Emulator Processor.

Test Group 3 utilizes a standard error display format that includes complete port status and interrupt information. Consult the individual test descriptions to determine which ports are actually being compared against reference values.

Note that jumpers P1 on the Buffer board, and J1045 and J2045 on the Mobile Microprocessor board can affect the Emulator Processor's access of Program Memory. These jumpers are assumed to be in their normal position during Test Group 3. For more information on jumpers, refer to Section 3 of this manual.

Consult Test Groups 4 and 5 for information on how the Emulator Processor's BKPT, Write Protect and SVC operations are verified.

0E/0030—SLVPAUSE/RUN Line Test. The SLVPAUSE/RUN Line test verifies that the 68000 Emulator Processor's SLVPSE/RUN logic allows the 2650 to regain control when the 68000 microprocessor is not running.

Description. Although the Emulator Processor's DLYD ACTIVE signal is asserted during this test, the RUNNING signal should not be asserted, since no RUNUSER command is issued to the Command Port. Without the RUNUSER command:

- the UGET/UPUT PROM decoder (U5170) does not assert END D/R(H).
- SETRUN(L) is not asserted at U5120A.
- RUNNING is deasserted at U6160D.

At this point, the Emulator Processor is activated and the 2650 is halted. Because the Emulator Processor was not given a command to start running a program, the 2650 should be restarted by a SLV HALT interrupt.

Error Display. See Display 7-24.

0E/0031—RUNUSER Test. The RUNUSER test verifies the Emulator Processor's RUNUSER and SLV PAUSE circuitry. The SLV PAUSE circuitry is the RUNUSER command's effect on the Emulator Processor's RUN(L) signal.

Description. The RUNUSER test is the first test in which the Emulator Processor's RUNNING(H) signal is asserted and Program Memory space is accessed. RUNNING(H) is asserted via the D/R PROM address decoder (U5170 on EMU 1) and the SETRUN logic (U6170 and U2220 on EMU 1). The RUNNING signal activates the Emulator Processor's BKPT and Write Protect circuitry. Thus, these interrupts may affect this test even though they are set to their don't-care state.

This test loads a Branch to Self instruction into Program Memory, directs the Emulator Processor to execute a RUNUSER command to the Branch to Self instruction, then halts the Emulator Processor operation via a system timer interrupt. The timer interrupt should cause the Emulator Controller to assert SLVPSE(L) on the bus. The Emulator

```
>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<   <<<<<<<

                                          Error Code   0E/0030

SLVPAUSE/RUN Line Test


----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-24

Processor detects SLVPSE(L) low and produces an internal Break Condition. This should force a Non Maskable Interrupt (NMI) to the 68000 microprocessor, causing an exit from the Branch to Self loop. The Emulator Processor then deasserts its RUN(L) signal and allows the Emulator Controller's master/slave flip-flop to toggle. When the flip-flop is toggled, the 2650 starts up and completes the test verification. The 2650 should find the Emulator Processor's Command Port cleared and a HAVE RUN status in the EMU Status Port.

Error Message. See Display 7-25.

0E/0032—Single Cycle Test. The Single Cycle test verifies the Emulator Processor's Single Cycle operation.

Description. The 68000 Emulator Processor implements all interrupt requests through the use of the 68000's NMI line. Since the 68000 does not output a fetch signal and the Emulator Processor does not contain a fetch predictor, the 68000 can be synchronously stopped at the end of a given instruction only through the use of a control signal that performs the synchronization automatically. The Non Maskable Interrupt (NMI) feature performs this task.

The Single Cycle operation is performed by the Emulator Processor whenever the S/CY EN bit, D3, is set high in the AUX Control Port. Bit D3 asserts BKCOND(H), which turns into BA BKCOND(H). BA BKCOND(H) produces IBKINT(L) and, finally, the BKINTEN(L) signal on the Control board. The BKINTEN(L) signal will force an NMI to the 68000. Note that the 68000 should not detect the pending NMI until the RUNUSER command has finished executing and RUNNING is asserted. RUNNING produces INTMACHEN(H) (U2140 on EMU 1), which gates the NMI to the 68000. (Gating is performed on the Control board.)

Note that the Interface Assembly drives pins 29–33 of J2, providing an output to the TTA board via the top plane connectors P6 and P7. Note also that the S/CY ACTIVE read-back function has already been tested in Test Group 1.

Error Message. See Display 7-26.

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0031

RUNUSER Test

EXPECTED: CMD 01  EMU/AUX STATUS 01FF  INTRPT 11  PCNEXT 0404
ACTUAL:   CMD **  EMU/AUX STATUS ****  INTRPT **  PCNEXT ****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
SECOND  SUSPECT = POD CONTROL BOARD
----------------------------------------
```

Display 7-25

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0032

Single Cycle Test

EXPECTED: CMD=01  EMU/AUX STATUS=01BF  INTRPT=33  PCNEXT=0402
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
SECOND  SUSPECT = POD CONTROL BOARD
----------------------------------------
```

Display 7-26

0E/0033—A0 Write Test. The A0 Write test verifies the Emulator Processor's write logic and generation of address line A0.

Description. The Invalid Command test in Test Group 2 tested the data bus latching mechanism by writing to the Shared Communication RAM. The A0 Write test completes the sequence by testing a write operation to Program Memory.

A0 is generated from the 68000's Upper and Lower Data Strobes (UDS and LDS). Therefore, A0 is high only when the 68000 is accessing an odd memory boundary. Since the 68000's R/W signal is factored into the WD ACCESS(L) signal (which controls the memory board access widths), word accesses are the default mode during all Program Memory read cycles. Therefore, the odd address memory situation is a factor only during Program Memory write operations.

In this test, the 68000 attempts to write to an odd address boundary. Single Cycle (verified earlier, 0E/0032) interrupts the Emulator Processor after the write instruction.

Error Message. See Display 7-27.

0E/0034—STOP Instruction Test. The STOP Instruction test verifies that the Emulator Processor will halt after executing a Stop Instruction in Emulation Mode 0.

Description. The Stop Instruction suspends 68000 operation until an external interrupt synchronization signal allows the 68000 to continue. Since prototype interrupt sources are not allowed in Emulation Mode 0, the Emulator Processor deasserts its RUN(L) line after executing a Stop Instruction in Emulation Mode 0. This causes the Emulator Controller to detect an Emulator Processor fault condition and interrupt the 2650 with a SLV HLT INTRP.

The STOP Instruction test checks for a SLV HLT INTRP from the Emulator Controller and for the assertion of the STOP bit, D5, in the AUX Status Port. The AUX Status Port is read again to verify that it was reset high on the first read. Jumper option J2144 on EMU 2 must be installed for this test. The jumper may be in either position.

Following execution of a Stop Instruction the BC AS(L) signal is halted. This produces STOP(L) via U2120 (on EMU 2), which produces BKCOND(H). BKCOND(H) in turn produces STOPPED BK(L), which generates ASYNCBK(L) (U6160 on EMU 1). ASYNCBK(L) immediately causes an NMI to be issued to the 68000 via IBKINT(L) and the interrupt machine on the Control board (U3040 or U5030). After the 68000 indicates an interrupt acknowledge, the following sequence will progress from the Interface Assembly to EMU 1 and deassert the Emulator Processor RUN(L) line: PODBKINTA(L), RESET RUN(L), RUNNING(L), and RUN(L).

Notice that the Single Cycle Test (0E/0032) produces a break condition that issues an NMI to the 68000 only after being synchronized by INTMACHEN(H) on the Control board. However, the Stop Instruction results in an ASYNCBK(L), which interrupts the 68000 immediately.

Error Message. See Display 7-28.

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0033

A0 Write Test

LOC 040D
ACTUAL   = **
EXPECTED = AA

EXPECTED: CMD=01  EMU/AUX STATUS=01BF  INTRPT=33  PCNEXT=0406
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-27

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0034

STOP Instruction Test

EXPECTED: CMD=01  EMU/AUX STATUS=01DF  INTRPT=33  PCNEXT=0404
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
SECOND  SUSPECT = 68000 EMULATOR BOARD 1
----------------------------------------
```

Display 7-28

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0035

Address Fault Test

EXPECTED: CMD=01  EMU/AUX STATUS=01DF  INTRPT=33  PCNEXT=0408
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT =  MOBILE PROCESSOR BOARD
----------------------------------------
```

Display 7-29

0E/0035—Address Fault Test. The Address Fault test checks the Emulator Processor's ability to detect and service an address fault condition. The Halt Condition Test (0E/0036) then creates a double address fault condition and tests the Emulator Processor's halt processor logic.

Description. The 68000 enters its exception-processing sequence whenever it detects a bus error, address error, illegal instruction, zero divide condition, or when the CHK instruction detects a boundary violation. The Halt Condition Test that follows requires a validated exception, therefore, the address error trap is tested here by forcing the 68000 to branch to an odd address.

The bus error condition cannot be tested in Emulation Mode 0. Therefore, the bus error condition is not tested in this diagnostic program.

The remaining exception processing conditions are tested in the 68000 CPU Test (0E/0070).

Note that this test is primarily a test of the 68000 microprocessor, and that the Stop Instruction verified in test 0E/0034 is used as a successful completion qualifier.

Error Message. See Display 7-29.

0E/0036—Halt Condition Test. The 68000 has been designed to halt itself whenever a double fault condition has been detected. The address error exception processing The HALT Condition test verifies that the 68000 can process a double fault condition and that the Emulator Processor can detect the halted 68000 state.

Description. The address error exception processing verified in the Address Fault test (0E/0035) is used in this test to create a double fault condition. The fault is created by force-jumping the 68000 to an odd boundary, with an odd vector pointer located in the address error vector at location 000C.

This test also verifies that the 68000 Emulator Processor samples the 68000 microprocessor's HALT signal and deasserts the RUN(L) signal whenever the HALT signal assertion is detected. The RUN(L) line is deasserted via the RUNNING flip-flop (U6160 on EMU 1). The Emulator Controller board detects that the Emulator Processor's RUN line has been deasserted and toggles its master/slave flip-flop (allowing the 2650 to run again).

Note that the 68000 can only be cleared from the halted state via a microprocessor reset.

Error Message. See Display 7-30.

Test Group 4 BKPT Tests

Test Group 4 tests the Emulator Processor's three breakpoints (BKPT 1, BKPT 2, and BKPT 3) in Emulation Mode 0. It is assumed that Test Groups 1–3 have been run at this point, so the Key ICs lists included in the Test Module Specifics discussion lists only the additional devices being tested.

0E/0040—BKPT1 Test. The BKPT1 test verifies the Emulator Processor's BKPT 1 function.

Description. This test loads a routine into Program Memory, and sets BKPT1 on a User Program word-read of an address within the routine. The Emulator Processor then jumps to the start of the routine, and a BKPT should occur. An interval timer interrupt will occur in the event of a test failure. Note that PCNEXT is also tested here (PCNEXT was first verified in the Single Cycle test, 0E/0031).

Error Message. See Display 7-31.

0E/0041—BKPT2 Test. The BKPT2 test verifies the Emulator Processor's BKPT2 function.

Description. See the description of the BKPT1 test (0E/0040) substituting BKPT2 for BKPT1 in the description.

Error Message. See Display 7-32.

0E/0042—BKPT3 Test. The BKPT3 test verifies the Emulator Processor's BKPT3 function.

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0036

Halt Condition Test

EXPECTED: CMD=81  EMU/AUX STATUS=11FF  INTRPT=33  PCNEXT=0000
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT =  68000 EMULATOR BOARD 1
SECOND  SUSPECT =  POD CONTROL BOARD
----------------------------------------
```

Display 7-30

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0040

BKPT1 Test

EXPECTED: CMD=01  EMU/AUX STATUS=01FB  INTRPT=33  PCNEXT=5558
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-31

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0041

BKPT2 Test

EXPECTED: CMD=01  EMU/AUX STATUS=01F7  INTRPT=33  PCNEXT=5558
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-32

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0042

BKPT3 Test

EXPECTED: CMD=01  EMU/AUX STATUS=01EF  INTRPT=33  PCNEXT=5558
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-33

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0043

BKPT1 Arms 2 Test

EXPECTED: CMD=01  EMU/AUX STATUS=01F7  INTRPT=33  PCNEXT=555A
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-34

Description. See the description of the BKPT1 Test (0E/0040) substituting BKPT3 for BKPT1 in the descriptions.

Error Message. See Display 7-33.

0E/0043—BKPT1 Arms 2 Test. The BKPT1 Arms 2 test verifies the Emulator Processor's BKPT1 ARMS BKPT2 function.

Description. The Emulator Processor's logic implements this function through the normal BKPT1 and BKPT2 functions, with additional random logic qualification logic. The qualification logic factors BKPT1 into the BKPT2 equation and prevents the BKPT1 from being detected by the Emulator Processor's BKCOND summing gate (U2050 on EMU 2). The combined breakpoint condition appears as a breakpoint status of BKPT2 only.

Error Message. See Display 7-34.

Test Group 5 SVC Tests

Test Group 5 verifies the Service Call (SVC) function that is implemented by both the 68000 Emulator Processor and your development system's Emulator Controller board. SVC's 1–8 are checked to verify that the Emulator Controller's SVC ID latch is operating correctly.

0E/0050—JMP ACK/SVC INHIBIT Test. The JMP ACK/SVC INHIBIT test verifies the Emulator Processor's JMPACK and SVC circuitry. The test also partially verifies the Emulator Controller's SVC detection circuitry.

Description. The Emulator Controller uses the Emulator Processor's JMPACK(L) signal to enable its SVC mechanism after the SVCs have been inhibited by a forced jump. This test enables SVCs and sends a forced-jump command to the Emulator Processor. The Emulator Processor should generate a JMPACK signal that completes the SVC enable sequence on the Emulator Controller.

In this test, the 68000 microprocessor is set up to execute an SVC (I/O) instruction when allowed to run. Therefore, this test verifies both the JMPACK and SVC mechanisms. The Emulator Processor is designed to process SVCs in the same way that it processes breakpoints, that is, both (SVC's and BKPT's) are set up through Emulator Processor RAMs that look at bus conditions. The difference lies in the fact that the SVC does not cause an Emulator Processor BKCOND; instead it causes the Emulator Processor's M(H)/IO(L) signal, at the System Bus, to indicate that an I/O operation is taking place. The Emulator Controller detects the I/O operation as an SVC, asserts SLVPSE(L) to the Emulator Processor, and interrupts the 2650 with an SVC interrupt acknowledge code.

Only SVC1 is verified during this test. Thus, the Supervisor Data byte-write instruction that generates the SVC will have an operand of 0007.

Error Message. See Display 7-35.

0E/0051—SVC Operational Test. The SVC Operational test extends the Emulator Controller testing that began in the JMP ACK/SVC INHIBIT Test (0E/0050).

Description. The JMP ACK/SVC INHIBIT Test was used to verify that the Emulator Processor could produce the JMPACK(L) and M(H)/I/O(L) signals on your development system bus. The Emulator Controller's SVC circuitry was also partially evaluated in the process. The SVC Operational test completes the Emulator Controller's SVC circuitry verification by completely checking the bits of the SVC page register, comparator, and ID latch. The setup procedure employed by the JMP ACK Test (0E/0050) is also used by this test; however, different pass parameters are used. Refer to the Test Module Specifics discussion later in this section, for these test parameters.

Error Message. See Display 7-36.

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0050

JMP ACK/SVC INHIBIT Test

EXPECTED: CMD=01  EMU/AUX STATUS=01FF  INTRPT=20  PCNEXT=040A
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BD
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-35

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0051

SVC Operational Test

EXPECTED: CMD=01  EMU/AUX STATUS=01FF  INTRPT=**  PCNEXT=040A
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BD
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-36

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0060

Write Protect Test

LOC 1000
ACTUAL     **
EXPECTED   AA

EXPECTED: CMD=01  EMU/AUX STATUS=01FE  INTRPT=33  PCNEXT=0408
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-37

Test Group 6 Write Protect/Memory Map Verification

Test Group 6 checks the 68000 Emulator Processor's write protect and memory map functions in Emulation Mode 0. Since the memory map function should be nonoperational in Emulation Mode 0, the actual mapping operation of the memory map function is not tested.

0E/0060—Write Protect Test. The Write Protect test verifies the Emulator Processor's write protect function. Both the write protect break condition and write pulse inhibit are tested.

Description. The UMAP/Write Protect RAM was tested in Test Group 1 (0E/0019). This test confines itself to operational testing of the write protect function.

In this test, the UMAP/Write Protect RAM is set up to prevent the 68000 microprocessor from writing to locations 1000–1FFF. The write protect logic disables the Emulator Processor's WRP(L) signal and cause the Emulator Processor to process an internal BKCOND.

Error Message. See Display 7-37.

0E/0061—Memory Map Test. The Memory Map test verifies that the Emulator Processor's memory map function is not operational in Emulation Mode 0. Since this diagnostic test is executed in Emulation Mode 0, a functional test of the Emulator Processor's memory map function is not performed.

Description. This test maps Emulator Processor memory locations 1000-1FFF to the prototype, and then writes a value to location 1000. If the map function in Emulation Mode 0 operates properly, the memory write should be allowed. Single cycle (verified earlier, 0E/0032) is used to interrupt the Emulator Processor after the write instruction.

Error Message. See Display 7-38.

```
>>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0061

Memory Map Test

LOC 1000
ACTUAL   = **
EXPECTED = AA

EXPECTED: CMD=01  EMU/AUX STATUS=01BF  INTRPT=33  PCNEXT=0406
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=**  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-38

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                        Error Code = 0E/0070

68000 CPU Test

EXPECTED: CMD=01  EMU/AUX STATUS=01DE  INTRPT=33  PCNEXT=056C
ACTUAL:   CMD=**  EMU/AUX STATUS=****  INTRPT=11  PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = MOBILE PROCESSOR BOARD
----------------------------------------
```

Display 7-39

Test Group 7 68000 CPU Test

Test Group 7 consists of one test that activates the Emulator Processor and directs it to execute a series of 68000 instructions loaded into Program Memory.

0E/0070—68000 CPU Test. The 68000 CPU test is a two part test that verifies the 68000's exception-processing abilities and then runs a number of 68000 instructions.

Description. This test first verifies that the 68000 can properly handle instructions that cause exception processing to occur. These conditions include illegal instructions, Chk, TRAP and TRAPV instructions, supervisor instructions executed in user mode, and division by zero. The address error condition was verified previously.

If no errors occur in the first part, the second part verifies that a representative set of 68000 instructions can be properly executed. The instructions execute data movement, integer arithmetic, logical, bit manipulation, BCD, and program control instructions. All addressing modes are used. The Stop Instruction (verified earlier, 0E/0034) is employed as a successful completion qualifier.

Error Message. See Display 7-39. The PCNEXT value in the error message will indicate which group of instructions failed. Refer to Test Module Specifics, later in this section, for failure information.

NOTE

If an error occurs during any part of the 68000 CPU test, the 68000 will loop on a Branch to Self instruction until a system timer interrupt occurs (11). The PCNEXT value in the error display will then indicate which group of instructions failed. (Refer to the Specifics discussion on 0E/0070, later in this section.)

Test Group 8 TTA Interface Test

0E/0080—TTA Interface Test. The TTA Interface test verifies that the interface between the TTA and Emulator Processor is operational. Since the 68000 Emulator Processor is a 16-bit emulator, this test verifies the upper address and data lines, as well as much of the Top Plane Interface. It also provides a parametric test of the Emulator Processor.

Description. This test first checks for the presence of a TTA in the system. If a TTA is not found, the message "TTA NOT DETECTED" is displayed on the first iteration.

If a TTA is detected in the system, a TTA setup procedure is performed. The 68000 test routine is then loaded into Program Memory. The 68000 repeats this instruction sequence until it is interrupted by the TTA after 10 passes through the routine. If the TTA interrupt does not operate properly, the 2650's interval timer will provide a failsafe test exit.

When the 2650 regains control, it checks the AUX Status Port to verify that the TTA interrupt caused the Emulator Processor to pause. The 2650 then checks the TTA's acquisition RAM against a reference list. For more on the TTA's acquisition list, refer to the Test Module Specifics later in this section).

NOTE

This test assumes that the TTA and 68000 Emulator Processor are properly connected with the two Top Plane Connectors (P6 and P7). The Activity and Bus/ID columns represent the status of these Top Plane signals. Likewise, the PROBE comparison is based on having the TTA probe interface board properly connected to the TTA board, with the probe test clips left disconnected. Disconnecting the probe assembly from the TTA board produces a FF value in the Probe column and result in an error display.

Error Message. See Display 7-40 or 7-41. Display 7-40 is displayed if the interrupt did not occur. Display 7-41 is displayed if the acquisitions did not compare to the reference list.

NOTE

The TTA acquires one additional instruction after it issues a TTA interrupt to the Emulator Processor. This instruction is acquired and counted, but is not compared against the reference buffer.

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0080

TTA Interface Test

EXPECTED: CMD=01   EMU/AUX STATUS=01FD   INTRPT=33   PCNEXT=0410
ACTUAL:   CMD=**   EMU/AUX STATUS=****   INTRPT=**   PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = TTA BOARD 1
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-40

```
>>>>>>>>>>>>>>>>    DIAGNOSTIC FAILURE    <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0081

TTA Interface Test

EXPECTED NUMBER OF ACQUISITIONS = 78H
COMPARISON FAILED AT ACQUISITION yyH

ACQ #    ADDRESS    DATA   PROBE  ACTIVITY  BUS/ID
 xx      xxxxxx     xxxx    xx       xx       xx
 yy      xxxxxx     xxxx    xx       xx       xx
 xx      xxxxxx     xxxx    xx       xx       xx
 xx      xxxxxx     xxxx    xx       xx       xx
 xx      xxxxxx     xxxx    xx       xx       xx
 xx      xxxxxx     xxxx    xx       xx       xx
 xx      xxxxxx     xxxx    xx       xx       xx

----------------------------------------
PRIMARY SUSPECT = TTA BOARD 1
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-41

NOTE

The first line of the acquisition dump is normally the last correct acquisition, followed by all subsequent acquisitions (or until 7 lines have been displayed). If the first acquisition was incorrect, it is displayed as the first line. If no acquisitions occurred, none are displayed.

Test Group 9 MAC Interface Test

0E/0090—MAC Interface Test. The MAC Interface test verifies the portion of the MAC board that is not accessible to the 2650 without the aid of a 16-bit emulator. All MAC functions that can be initiated and examined without physical access to the MAC board are exercised.

This test also verifies the ability of the MAC board to generate an interrupt when the 68000 Emulator Processor attempts to access non-allocated Program Memory.

Description. This test first checks for the presence of a MAC board in the system. If a MAC board is not found, the message "MAC NOT DETECTED" is displayed on the first iteration.

If the MAC board is detected in the system, two 4K blocks of memory are mapped at 02AA A000 and 0055 5000. A 68000 routine is loaded into the Program Memory causing the 68000 to write to a location in each of the two 4K blocks and to write a third time to an area where memory is non-existent. This third write should generate a MAC interrupt and cause the write address to be latched on the MAC board.

When the 2650 regains control, it verifies that a MAC interrupt caused the Emulator Processor to pause at the proper time (PCNEXT check). The 2650 then verifies that the test locations were written to by the 68000 and that the address in the MAC interrupt latch is correct.

NOTE

This test assumes that the MAC and 68000 Emulator Processor are properly connected with with Top Plane connector P6.

Error Message. See Displays 7-42, 7-43, and 7-44. Display 7-42 is displayed if the MAC interrupt did not occur or occurred at the wrong time. Display 7-43 or 7-44 is displayed if the test locations did not compare to the reference.

NOTE

If Display 7-42 is displayed, the DO NOT LOOP option can be used to gain additional information with a second display.

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0090

MAC Interface Test

EXPECTED: CMD=01   EMU/AUX STATUS=01FF   INTRPT=37   PCNEXT=0426
ACTUAL:   CMD=**   EMU/AUX STATUS=****   INTRPT=**   PCNEXT=****

----------------------------------------
PRIMARY SUSPECT = MAC BOARD
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-42

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0091

MAC Interface Test

MAC FAILED TO MAP 4K MEMORY BLOCK AT 2AAA000 (or 0555000)

----------------------------------------
PRIMARY SUSPECT = MAC BOARD
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-43

```
>>>>>>>>>>>>>>>>     DIAGNOSTIC FAILURE     <<<<<<<<<<<<<<<<

                                          Error Code = 0E/0091

MAC Interface Test

MAC INTERRUPT ADDRESS LATCH FAILURE

----------------------------------------
PRIMARY SUSPECT = MAC BOARD
SECOND  SUSPECT = 68000 EMULATOR BOARD 2
----------------------------------------
```

Display 7-44

Test Module Specifics

The following text describes in detail the operation of the test modules used by the 68000 Emulator Processor diagnostics. This information includes each step of the testing process and a brief explanation of the expected results. Where possible, a list of key ICs affected by the test is also provided. For a general description of the test modules, including error displays, refer to the Test Module Descriptions earlier in this section.

0E/0000

Group
0—RUN ALL

Module
0—EMU Detection Test

Process

1. Write 00 to EMU Control Port AD (powers down the Interface Assembly).
2. Read EMU Status Port AD.
3. Mask unused bits.

Expected
The EMU Status Port should not equai zero when read, indicating that the 68000 Emulator Processor is installed.

Key ICs
EMU 2: U3100, U4160, U5060, U5070, U5090.

0E/0010

Group
1—I/O Port and RAM Test

Module
10—EMU Activation Sequence Test

Process

1. Write 00H to EMU Control Port AD (powers down the Interface Assembly).
2. Write 80H to the EMU Control Port (powers up the Interface Assembly).
3. Wait 0.1 second.
4. Check EMU Status Port AD for EMU RESET REQ (D2), and mask all other bits.
5. Write 84H to the EMU Control Port (asserts the EMU ACTIVE bit).
6. Read AUX Status Port 8E (resets HAVE RUN).
7. Read the EMU Status Port.
8. Mask off CLKFAIL and unused bits.

Expected
The EMU Status Port should equal 04H on its first read, and 00H its second (EMU RESET REQ, HALTED, and HAVE RUN should be cleared, low).

Key ICs
EMU 2: (EMU RESET REQ) U4160, U5060, U5070, U5090; (HAVE RUN) U2150, U3130, U5060; (HALTED) U5060, Mobile Microprocessor board.

0E/0011

Group
1—I/O Port and RAM Test

Module
11—Clock Fail Detection Test

Process

1. Activate the Emulator Processor.
2. Write E4H to EMU Control Port AD (selects Emulation Mode 2).
3. Check EMU Status Port AD for a clock failure indication (CLKFAIL bit, D1, asserted).
4. Write 80H to the EMU Control Port (reselects Mode 0).
5. Write 84H to the EMU Control Port (releases the microprocessor reset).
6. Check the EMU Status Port. All assigned bits should be cleared.

Expected
With no prototype circuit clock source in Emulation Mode 2, the EMU Status Port's CLKFAIL bit should be asserted high (D1 = 1) on the first read. On the second read, the CLKFAIL bit should be deasserted (D1 = 0).

Key ICs
EMU 1: U2180, Y3228.
EMU 2: U3150, U5060, U5150, U5160.
Buffer board: U5010, U7010, Q8011, Q9011.

0E/0012

Group
1—I/O Port and RAM Tests

Module
12—Auxiliary Port Test

Process

1. Activate the Emulator Processor.
2. Read the AUX Status Port (bits D0-D5 are reset high)
3. Write 00H to AUX Control Port 8E (deasserts S/CY EN).
4. Read the AUX Status Port (expecting FFH, indicating that S/CY ACTIVE is deasserted and the port has been reset).
5. Write 08H to the AUX Control Port (asserts S/CY EN).
6. Read the AUX Status Port (expecting BFH, indicating that S/CY ACTIVE is asserted).
7. Write 00 to the AUX Control Port (deasserts S/CY EN).
8. Read the AUX Status Port (expecting FFH, indicating that S/CY ACTIVE is deasserted).

Expected
The AUX Status Port should equal the values expected as listed in the previous Process list.

Key ICs
EMU 1: (bit D7) U4110, U6090.
EMU 2: (bit D7) U2060; (bit D6) U2110, U5080; (bits D0-D5) U1130, U2120, U2150, U3120.

0E/0013

Group
1—I/O Port and RAM Tests

Module
13—Command Port Test

Process

1. Deactivate the Emulator Processor.
2. Activate the Emulator Processor.
3. Read Command Port 8F (expecting 01H).
4. Write the first test pattern shown in Table 7-2 to the Command Port.
5. Read the Command Port and compare to the first test pattern shown in Table 7-2.
6. Repeat steps 4 and 5 for test patterns 2-6.

Table 7-2
Command Port Test Patterns

Pattern	Write	Read
1	40	01
2	42	03
3	44	05
4	48	09
5	50	11
6	60	21

Expected
The first read should equal 01, indicating the port has been reset. The other read values should equal those listed in Table 7-2.

Key ICs
EMU 1: U2050, U2060, U2080, U2090, U4120, U6100; (bit D6 only) U6010.
EMU 2: U3130, U4160; (bit D0 only) U5090, U6030.

0E/0014

Group
1—I/O Port and RAM Tests

Module
14—RAM INHIBIT Test

Process

1. Activate the Emulator Processor.
2. Write 55H to system memory address space A000, and to Program Memory A000 and 2000.
3. Read Program Memory location A000.

NOTE

If Program Memory equals 55H, then continue to step 4. However, if Program Memory does not equal 55H, then execute the following:

3a. Relocate a 4K block of Program Memory to A000.
3b. Write 55H to A000 of Program Memory.
3c. Read Program Memory, A000.

If Program Memory equals 55H, then continue to step 4. If Program Memory still does not equal 55H, then assume that RAMINH(L) is stuck low and generate an error.

4. Write 86H to EMU Control Port AD (enables the Emulator Processor's RAM, RAMEN bit).

5. Write AAH to Program Memory locations A000 and 2000, and to system memory location A000.
6. Write 84H to the EMU Control Port (disables the Emulator Processor's RAM).
7. Read system memory location A000, and Program Memory locations A000 and 2000.

Expected
Location A000 in system memory should contain AAH. However, A000 and 2000 in Program Memory should contain 55H and AAH, respectively. (RAMINH(L) should prevent the second write to Program Memory location A000, but should not affect the writes to system memory location A000 or to Program Memory location 2000.)

Key ICs
EMU 2: U4130, U4150, U5050, U5070, U5090.

0E/0015

Group
1—I/O Port and RAM Tests

Module
15—UMAP/Write Protect RAM Test

Process
1. Activate the Emulator Processor.
2. Assert the RAMEN bit, D1, (by writing 86H to the EMU Control Port, AD).
3. Write 01H to the UMAP/Write Protect RAM at locations C000-FFFF.
4. Read, verify, and write 02H to the UMAP/Write Protect RAM at each location from C000-FFFF.
5. Read, verify, the UMAP/Write Protect RAM at locations C000-FFFF.

Expected
Mask the UMAP/Write Protect RAM read with a 03H for both passes, then verify that the first read returns 01H and the second returns 02H. Note that the second pass through memory performs a read, verify, then writes the second test pattern at the same location before advancing to the next location.

Key ICs
Common Components—
EMU 1: U4110, U4120, U6060, U6080, U6100.
EMU 2: U1070, U2030, U2070, U2080, U4050, U5060.
Individual Components—See Table 7-3.

Table 7-3
Suspected Bad Devices For Test 0E/0015

Faulty Address Line		Probable Cause	
A13	A12	Write Protect (D1)	UMAP (D0)
0	0	U4010	U3010
0	1	U4030	U3030
1	0	U4020	U3020
1	1	U4040	U3040

0E/0016

Group
1—I/O Port and RAM Tests

Module
16—BKPT/SVC RAM Test

Process
1. Activate the Emulator Processor.
2. Enable the Emulator Processor's RAM for 2650 access (by writing 86H to EMU Control Port AD).
3. Write the first memory pass shown in Table 7-4.
4. Read the first memory pass and write the second memory pass shown in Table 7-4.
5. Read the second memory pass.
6. Mask the read operation with 0FH (memory is only 4 bits wide) after each read.

Table 7-4
Breakpoint RAM Test Passes

Memory Pass	8000–80FF	8100–81FF	8200–82FF	8300–83FF
1.	05H	05H	0AH	0AH
2.	0AH	0FH	0FH	05H

Expected
The memory reads should equal the memory writes, respectively. Note that the second pass through memory (step 4) performs a read, then writes the second test pattern at the same location before advancing to the next location.

Key ICs
EMU 1: U4110, U4120, U6060, U6080, U6100.
EMU 2: U3050 (8000-80FF), U3070 (8100-81FF), U3080 (8200-82FF), U3090 (8300-83FF), U1070, U1080, U1090, U2010, U2020, U2030, U4050, U4070, U4090.

0E/0017

Group
1—I/O Port and RAM Tests

Module
17—Shared Communication RAM Test

Process

1. Activate the Emulator Processor.
2. Enable the Emulator Processor's RAM for 2650 access (by writing 86H to the EMU Control Port, AD).
3. Write the first test pattern shown in Table 7-5 to the Shared Communication RAM locations, A000-A7FF.
4. Read the first test pattern, and write the second pattern to each location from A000-A7FF.
5. Repeat step 4 for test passes 2-5 listed in Table 7-5.

Table 7-5
Shared Communication RAM Test Patterns

Test Pass	Read	Write
1	None	AA
2	AA	CC
3	CC	F0
4	F0	0F
5	0F	None

Expected
For each test pass the memory read back should correspond to the test pattern last written to memory. Note that in step 4 a read (for verification), then a write is executed at the same location before advancing to the next location.

Key ICs
EMU 1: Low bank (A000-A3FF); U5210, U5220, U4080, U6220.
High bank (A400-A7FF); U4080, U5190, U5200, U6210.
Common; U4110, U4120, U6060, U6080, U6100, U6190.
EMU 2: U3100

0E/0020

Group
2—Dump/Restore Logic Tests

Module
20—Invalid Command Test

Process

1. Activate the Emulator Processor.
2. Write 86H to EMU Control Port AD (enables the Emulator Processor's RAM).
3. Clear the CMDSTAT location in the Shared Communication RAM (location A054).
4. Write the illegal command, B0H, to Command Port 8F.
5. Poll the Command Port for bit D7 clear.
6. Read the CMDSTAT location in the Shared Communication RAM.

Expected
The 68000 microprocessor should set CMDSTAT to 02 (indicating an invalid command), then clear the Command Port before the poll loop timeout.

Key ICs
EMU 1: U2080, U3080, U4110, U4120, U4140, U4150, U4160, U4170, U4180, U4190, U5040, U5060, U5140, U5160, U6040, U6200.
Buffer board: U2040, U4050, U7050, U8050.
Mobile Microprocessor board: U1010, the 68000 microprocessor.

NOTE

Devices U1010, U4140, U4170, U5040, U5060, and U6040 may specifically affect writes to the CMNDSTAT.

0E/0021

Group
2—Dump/Restore Logic Tests

Module
21—Shared RAM Access Test

Process

1. Activate the Emulator Processor.
2. Load the following into the Shared Communication RAM starting at location A05A:

```
4E71              NOP (reference pattern)
70FF, 51C8, 00FC  Branch to Self (FF times)
4238, 1001        Clear Command Port
4E75              Return from subroutine
```

3. Load 085C into PCNEXT location (A046-A047) in the Shared Communication RAM (points to Branch to Self instruction).
4. Write EXECRAM command (8CH) to Command Port 8F.
5. Write 55H to test location A05A (attempts to gain access to Shared Communication RAM while 68000 is running).
6. Poll Command Port for D7 clear.
7. Write FFH to the Shared Communication RAM (location A05B) and read-back to verify that memory can be accessed.
8. Read test location A05A.

Expected
The Emulator Processor should prevent the write to A05A. After the Command Port has been cleared, the write to A05B should be allowed.

Key ICs
EMU 1: U2080, U3080, U4110, U4120.

0E/0022

Group
2—Dump/Restore Logic Tests

Module
22—UMAP/BKPT RAM Access Test

Process

1. Activate the Emulator Processor.
2. Write 55H to the UMAP and BKPT RAM (8000 and C000).
3. Load the following into the Shared Communication RAM starting at location A05C:

```
11FC, 00AA, 8000    Write AA to 8000
11FC, 00AA, C000    Write AA to C000
4238, 1001          Clear Command Port
4E75                Return from subroutine
```

4. Load 085C into PCNEXT location, A046 (points to start of routine).
5. Write EXECRAM command (8CH) to Command Ports 8F.
6. Poll the Command Port for bit D7 clear.
7. Read the test locations in the UMAP and BKPT RAMs.

Expected
The test locations in the UMAP and BKPT RAMs should not be modified.

Key ICs
EMU 2: (UMAP problem) U4100B, U5040, U5120; (BKPT problem) U4100D or U4050B.

0E/0023

Group
2—Dump/Restore Logic Tests

Module
23—Register Restore/Dump Test

Process

1. Activate the Emulator Processor.
2. Load the register test values into the Shared Communication RAM.
3. Write the Register Restore command (84H) to Command Port 8F.
4. Poll the Command Port for clear status.
5. Write 00H to the Register Save Area in the Shared Communication RAM, and read-back to verify that 00H has been written.
6. Write the Register Dump command (82H) to the Command Port.
7. Poll the Command Port for bit D7 clear.
8. Read the registers dumped to the Shared Communication RAM.

Expected
The values returned in Shared Communication RAM should match those originally loaded.

Key ICs
Refer to Test Group 2 (0E/0020, 0E/0021, and 0E/0022)

0E/0024

Group
2—Dump/Restore Logic Tests

Module
24—D/R ROM Routines Completion Test

Process

1. Activate the Emulator Processor.
2. Write the first D/R Routine command listed in Table 7-6 to the Command Port.
3. Poll the Command Port for bit D7 clear.
4. If the Command Port is cleared by the 68000 microprocessor before the poll loop timeout, repeat steps 2 and 3 for test passes 2 and 3, listed in Table 7-6.

Table 7-6
D/R ROM Routines Completion Test Passes

Test Pass	D/R Routine	Command
1	UGET	86H
2	UPUT	88H
3	Readback	8AH

Expected
The execution of each of the three commands listed in Table 7-6 should cause the 68000 microprocessor to clear the Command Port before the poll loop timeout occurs.

Key ICs
EMU 1: U5160, U5170

0E/0030

Group
3—Emulation Mode 0 Verification

Module
30—SLVPAUSE/Run Line Test

Process

1. Activate the Emulator Processor.
2. Enable the system interval timer (failsafe use).
3. Halt the 2650.

Expected
Slave Halt Interrupt (interrupt 33), indicating the 68000 did not run. A timer interrupt (interrupt 11) will occur in the event of a test failure, such as if the RUN(L) line is permanently stuck low (because Emulator Controller will not toggle the Master/Slave FF and SLV PAUSE(H) will remain asserted). However, the development system will appear to hang if the Emulator Processor fails to deassert the RUN(L) line after SLV PAUSE(H) is asserted following the timer interrupt. The latter condition results because the RUN(L) signal prevents the Master/Slave FF from toggling and allowing the 2650 to once again run and complete the test.

Key ICs
EMU 1: U2060, U2220, U5120, U5170, U6030, U6160, U6170.

0E/0031

Group
3—Emulation Mode 0 Verification

Module
31—RUNUSER Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
4E71, 4E71      NOP, NOP
60FE            Branch to Self
```

3. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Write the RUNUSER command (80H) to Command Port 8F.
5. Activate the system timer.
6. Halt the 2650 (allows the Emulator Processor to access Program Memory).

Expected
Command Port should equal 01H (SLV PAUSE). The EMU Status Port should equal 01H (HAVE RUN). Interrupt should equal 11 (Timer).

Key ICs
EMU 1: U2140, U2170, U2215, U2220, U4220, U5170, U6160, U6170F.
EMU 2: U2050, U2150B.
Control board: U1020, U3040, U5030, U6010, U6030, U6040.

0E/0032

Group
3—Emulation Mode 0 Verification

Module
32—Single Cycle Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
4E71, 4E71      NOP, NOP
60FE            Branch to Self
```

3. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Write 08H to AUX Control Port 8E (asserts the S/CY EN bit).
5. Write the RUNUSER command (80) to Command Port 8F.
6. Halt the 2650.

Expected
The Command Port should equal 01H. The EMU Status Port should equal 01H. The AUX Status Port should equal BF (S/CY ACTIVE). Interrupt should equal 33. PCNEXT should equal 0402H.

Key ICs
EMU 1: U2140, U2170 (MODE0 BKEN(H)).
EMU 2: U2050.
Control board: U3040, U6030, U6040.
Mobile Microprocessor board: 68000 microprocessor.

0E/0033

Group
3—Emulation Mode 0 Verification

Module
33—A0 Write Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
11FC, 00AA, 040D    Write AA to 040D
4E71, 4E71          NOP, NOP
60FE                Branch to Self
```

3. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Load S/CY EN into the AUX Control Port.
5. Write the RUNUSER command (80H) to the Command Port.
6. Halt the 2650.

Expected
Program Memory location 040D should equal AAH.

Key ICs
EMU 1: (WRP(L)) DL4030, U3090; (A0) U3050, U4180, U4190, U6050, U6070; (WD ACCESS(L)) U2030, U5030.

0E/0034

Group
3—Emulation Mode 0 Verification

Module
34—STOP Instruction Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
4E72, 2000  Stop and load Status Register
            with 2000
```

3. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Write the RUNUSER command (80H) to the Command Port.
5. Halt the 2650.

Expected
The Command Port should equal 01H. The AUX Status Port should equal DFH (STOP). Interrupt should equal 33. On the second read, the AUX Status should equal FFH. The AUX Status Port is read a second time to verify that the STOP status can be cleared.

Key ICs
EMU 1: U4220, U5120, U6160.
EMU 2: U1120, U2120, U2130, U2140, U3140, U3150.
Control board: U3040, U4030.

0E/0035

Group
3—Emulation Mode 0 Verification

Module
35—Address Fault Test

Process

1. Activate the Emulator Processor.
2. Load 0404 into Program Memory location 0000 (address error vector).
3. Load the following into Program Memory starting at location 0400:

```
60FF          Branch to 0401
60FE          Branch to Self
4E72, 2700    Stop and load Status Register
              with 2700
```

4. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
5. Write the RUNUSER command (80H) to the Command Port.
6. Start the system timer.
7. Halt the 2650.

Expected
The 68000 should execute a Jump instruction at location 0400, vector to 000C for address error exception processing. This should result in the execution of a Stop instruction at location 0404. The Command Port should equal 01H. The EMU Status Port should equal 01H. The AUX Status Port should equal DFH. Interrupt should equal 33.

Key ICs
Mobile Microprocessor board: 68000 microprocessor.

0E/0036

Group
3—Emulation Mode 0 Verification

Module
36—Halt Condition Test

Process

1. Activate the Emulator Processor.
2. Load 0403 into Program Memory location 000C (address error vector).
3. Load the following into Program Memory starting at location 0400:

```
60FF          Branch to 0401
60FE          Branch to Self
4E72, 2000    Stop and load Status Register
              with 2000
```

4. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
5. Write the RUNUSER command (80H) to the Command Port.
6. Start the system interrupt timer.
7. Halt the 2650.

Expected
The odd address error vector at 000C should cause the 68000 to halt. The Command Port should equal 81H. The EMU Status Port should equal 11H. The AUX Status Port should equal FFH. Interrupt should equal 33.

Key ICs
EMU 1: U1220, U5090, U6160.
Mobile Microprocessor board: 68000 microprocessor.
Control board: U3010, 8040A.

0E/0040

Group
4—Breakpoint Tests

Module
40—BKPT1 Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 5552:

```
46FC, 0700    Change to user mode
4E71, 4E71    NOP, NOP
60FE          Branch to Self
```

3. Load 5552 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Load the Breakpoint RAM with BKPT1 set on a User Program word-read from location 5556.
5. Write the RUNUSER command (80H) to Command Port 8F.
6. Activate the interval timer.
7. Halt the 2650.

Expected
The AUX Status Port should equal FBH (BKPT1). Interrupt should equal 33. PCNEXT should equal 5558. The AUX Status Port is read a second time to verify that the BKPT status can be cleared.

Key ICs
EMU 2: U2060, U2120, U3110, U3140, U4060, U5120.

0E/0041

Group
4—Breakpoint Tests

Module
41—BKPT2 Test

Process

1. Consult the BKPT1 Test (0E/0040) setup procedure for details, substituting BKPT2 for BKPT1.

Expected
Consult the BKPT1 Test (0E/0040) for details, substituting BKPT2 for BKPT1.

Key ICs
EMU 2: U2060, U3120, U4060, U4140.

0E/0042

Group
4—Breakpoint Tests

Module
42—BKPT3 Test

Process

1. Consult the BKPT1 Test (0E/0040) setup procedure for details, substituting BKPT3 for BKPT1.

Expected
Consult the BKPT1 Test (0E/0040) for details, substituting BKPT3 for BKPT1.

Key ICs
EMU 2: U2060, U3120, U4080.

0E/0043

Group
4—Breakpoint Tests

Module
43—BKPT1 Arms 2 Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 5552:

```
46FC, 0700     Change to user mode
4E71, 4E71     NOP, NOP
60FE           Branch to Self
```

3. Load 5552 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Load the Breakpoint RAM with BKPT1 and BKPT2 set on a word-read from location 5556.
5. Load Breakpoint RAM with BKPT2 set on a User Program word-read from location 5558.
6. Write 10H to AUX Control Port 8E (asserts the BKPT1 ARMS BKPT2 bit).
7. Write the RUNUSER command (80H) to Command Port 8F.
8. Activate the interval timer.
9. Halt the 2650.

Expected
The AUX Status Port should equal F7H (BKPT2). Interrupt should equal 33. PCNEXT should equal 555A. The AUX Status Port is read a second time to verify that the BKPT status can be cleared.

Key ICs
EMU 2: U2060, U3110, U3140, U4140, U5080.

0E/0050

Group
5—SVC Tests

Module
50—JMP ACK/SVC INHIBIT Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
13C0, 00FF, AA07  Write a byte to FFAA07
4E71, 4E71        NOP, NOP
60FE              Branch to Self
```

3. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
4. Load the Breakpoint RAM (SVC RAM) to detect an SVC on a Supervisor Data byte-write to location FFAA00-FF.
5. Write 40H to AUX Control Port 8E (asserts the SVC ENABLE bit).
6. Enable SVCs on the Emulator Controller by writing FBH to port F9.
7. Load the Emulator Controller's SVC map register (by writing 0 to port F3).
8. Write the RUNUSER command (80H) to Command Port 8F.
9. Activate the interval timer.
10. Halt the 2650.

Expected
The SVC1 interrupt (interrupt 20) should be received from Emulator Controller.

Key ICs
EMU 1: U2190.
EMU 2: U1130, U4080, U4130B, U5080, U5130.
Emulator Controller Board: U4110, U5040, U5050, U5070, U5160, U5180.

0E/0051

Group
5—SVC Tests

Module
51—SVC Operational Test

Process

1. Consult the JMP ACK Test (0E/0050) setup procedure and Table 7-7 for details.

Expected
Consult the JMP ACK Test (0E/0050) and the test parameters listed in Table 7-7.

Table 7-7
SVC Operational Test Pass Parameters

Test Pass	MOVE.B Operand	SVC MAP Register[a]	Interrupt Expected	SVC Expected
1	FFAA01	10	26	7
2	FFAA02	20	25	6
3	FFAA04	40	23	4
4	FFAA08	80	11	None
5	FFAA10	01	27	8
6	FFAA20	02	27	8
7	FFAA40	04	27	8
8	FFAA80	08	27	8

[a] **Write value to port F3.**

Key ICs
Emulator Controller Board: U4070, U5040, U5050, U5070.

0E/0060

Group
6—Write Protect/Memory Map Tests

Module
60—Write Protect Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
11FC, 00AA, 1000    Write AA to 1000
60FE                Branch to Self
```

3. Load UMAP/Write Protect RAM to write protect Program Memory at 1000-1FFF.
4. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
5. Write the RUNUSER command (80H) to Command Port 8F.
6. Activate the interval timer.
7. Halt the 2650.

Expected
Program Memory location 1000 should not be modified. The AUX Status Port should equal FEH (WR PROTECT INT). Interrupt should equal 33. The AUX Status Port should be read a second time to verify that the interrupt latch can be cleared.

Key ICs
EMU 1: U2190, U3090.
EMU 2: U1110, U1130, U2050, U2060.

0E/0061

Group
6—Write Protect/Memory Map Tests

Module
61—Memory Map Test

Process

1. Activate the Emulator Processor.
2. Load the following into Program Memory starting at location 0400:

```
11FC, 00AA, 1000    Write AA to 1000
60FE                Branch to Self
```

3. Load UMAP/Write Protect RAM to map 1000-1FFF to prototype (non-operational in Mode 0).
4. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
5. Write the RUNUSER command (80H) to Command Port 8F.
6. Write 08H to EMU Control Port 8E (enables S/CY).
7. Activate the interval timer.
8. Halt the 2650.

Expected
Program Memory location 1000 should contain the new write value (AAH). The AUX Status Port should equal BFH. Interrupt should equal 33. PCNEXT should equal 0406.

Key ICs
EMU 2: U1110, U4130, U4140.

0E/0070

Group
7—68000 CPU Test

Module
70—68000 CPU Tests

Process

1. Activate the Emulator Processor.
2. Load the test program into Program Memory and initialize the microprocessor's vectors.
3. Write the RUNUSER command (80H) to the Command Port.
4. Enable the interval timer.
5. Halt the 2650.

Expected
The 68000 should execute each exception processing instruction, and vector to the respective service routine. The 68000 should then execute each sequence of representative instructions and pass each checkpoint, until it reaches the Stop instruction. The AUX Status Port should equal DFH (STOP). Interrupt should equal 33. PCNEXT should equal 056C.

If an error occurs, the 68000 will loop on a Branch to Self until a system timer interrupt (11) occurs. As shown in Table 7-8, the PCNEXT value will indicate which group of instructions failed.

Key ICs
Mobile Microprocessor board: 68000 microprocessor.

Table 7-8
68000 CPU Test Instruction Failures

PCNEXT	Failing Instruction Type
0422	Illegal Instruction (Trap Vector 10H)
042C	Divide by Zero (Trap Vector 14H)
0436	Check Instruction (Trap Vector 18H)
0442	TRAP V Instruction (Vector ICH)
0458	Privilege Violation (Trap Vector 20H)
0468	Trace (Trap Vector 24H)
0472	Unimplemented Instruction (Trap Vector 28H)
047C	Unimplemented Instruction (Trap Vector 2CH)
048E	Trap Instruction (Trap Vector 9CH)
04A2	Logical Instruction
04C0 or 04C4	Data Movement Instruction
04EE or 04F2	Integer Arithmetic Instruction
04F8 or 04FC	Program Control Instruction
04FE	Incorrect Vector Taken in Trap Test
0532	Shift/Rotate Instruction
0550	Test and Set Instruction
0564	Binary Coded Decimal Instruction

0E/0080

Group
8—TTA Interface Test

Module
80—TTA Interface Test

Process

1. Attach the Data Acquisition Interface board and probe to the TTA (leave the probe test clips disconnected).
2. Position the Data Acquisition Interface's control panel switches as follows:
   - EXT CLK PLRT—Center position (the constant sample position).
   - TTL VAR—Up position (the TTL reference position).
3. Initialize the TTA's I/O ports:
   - 74=FD Top plane for address, data, activity
   - 73=00 Clear Triggers
   - 72=91 Ignore WRP, break on Trigger1
   - 71=02 Acquire all
   - 70=02 2650 access to TTA RAM, SLVOP as auxiliary count source
   - 77 and 76 Reset control chip, load CTR1 with number of SLVOPs, set CTR1 to count SLVOPs, down, TC toggled output, other CTRs inactive; Set CTR outputs (54321)=10101
4. Load the TTA comparison RAM to generate Evt1 on STATUS=10101.
5. Read and save the initial Acquisition Pointer value.
6. Arm CTR1.
7. Disable the 2650's access to the TTA RAM, then arm the TTA.
8. Enable the interval timer.
9. Activate the Emulator Processor.
10. Load the following into Program Memory starting at location 0400:

```
13FC, 5555, 0055, 5555   Write 55 (byte)
                         to 555555
33FC, AAAA, 00AA, AAAA   Write AAAA (word)
                         AAAAAA
4EF8, 0400               Jump back to 0400
                         (start)
```

11. Load 0400 into the Trapstack's PCNEXT location in the Shared Communication RAM.
12. Write the RUNUSER command (80H) to Command Port 8E.
13. Halt the 2650.

Expected
The AUX Status Port should equal FDH (TTA INT29), with no differences between the Acquisition RAM, shown in Table 7-9, and the reference buffer. The number of acquisitions should be 78H. The AUX Status Port is read a second time to verify that the TTA Interrupt latch can be cleared.

Key ICs
TTA Board 1: U3100 (A16-A23); U3030 (A8-A15); U3020 (A0-A7); U3080 (D8-D15); U3070 (D0-D7); U1020 (Probe); U3150 (Activity); U3110 (Bus/IO); U1130 (no TTA interrupt).
EMU 2: U5100, U2150.

0E/0090

Group
9—MAC Interface Test

Module
90—MAC Interface Test

Process

1. Initialize the MAC board for test.
   a. Initialize the MAC State and Relocation RAM with FF.
   b. Write 01H to C000, D000, E000, F000, EAAA, and C555 in the Relocation RAM.
   c. Write FDH to C000, D000, E000, F000, EAAA, and C555 in the State RAM.
   d. Activate the MAC.

Table 7-9
TTA Interface Reference List

Program Comparison	TTA Acquisition RAM					
Instruction	ACQ#	Address	Data	Probe	Activity	Bus/ID
START:						
MOVE.B #5555,555555H	00	000400	13FC	00	CF	FD
	01	000402	5555	00	CF	FD
	02	000404	0055	00	CF	FD
	03	000406	5555	00	CF	FD
MOVE.W #AAAA,AAAAAAH	04	000408	33FC	00	CF	FD
	05	555555	5555	00	BF	BD
	06	00040A	AAAA	00	CF	FD
	07	00040C	00AA	00	CF	FD
	08	00040E	AAAA	00	CF	FD
	09	000410	4EF8	00	CF	FD
JMP START	0A	AAAAAA	AAAA	00	AF	BD
	0B	000412	0400	00	CF	FD

2. Activate the Emulator Processor.
3. Load the following into Program Memory starting at location 0400:

```
13F9, 00AA, AAAA, 00AA, AAAB Move data from
                             AAAAAA to
                             AAAAAB
46FC, 0700                   Change to user
                             mode
13F9, 0055, 5555, 0055, 5556 Move data from
                             555555 to
                             555556
13C0, 0066, 6666             Write to 666666
                             (666666 is
                             non-existent
                             memory)
60FE                         Branch to Self
```

4. Enable the interval timer.
5. Halt the 2650.

Expected
Interrupt should equal 37 (MAC INT31). PCNEXT should equal 041E. Program Memory locations 0AAB and 0556 should equal 60H and FEH, respectively. The MAC interrupt address latch should be 00666666H.

Key ICs
MAC Board: U1530, U2530, U2540 (no MAC interrupt); U2110, U2120, U2150 (no memory map).

Section 8

MAINTENANCE AND TROUBLESHOOTING

INTRODUCTION

This section describes preventive maintenance procedures that will help to improve equipment reliability. Techniques and aids for troubleshooting, including diagnostic testing routines, are also included in this section. If the equipment fails to operate properly, corrective measures should be taken immediately; an equipment malfunction may cause additional problems to develop.

STATIC-SENSITIVE PARTS

Many components can be damaged by static discharge. Static-caused damage may be catastrophic, or it may only cause degradation in component performance. Either type of damage is costly: destroyed devices must be replaced, and unnoticed marginal devices can cause intermittent equipment malfunction.

To minimize static problems during maintenance or troubleshooting, follow these procedures:

1. Minimize the handling of static-sensitive parts.
2. Transport and store static-sensitive parts in their original containers, on a metal rail, or on conductive foam. Label any container having a static-sensitive assembly or device.
3. Before handling static-sensitive parts, discharge the static charge on yourself by using a grounded metal wrist strap. Static-sensitive assemblies or devices should be serviced only at a static-free work station, and only by qualified personnel.
4. Do not allow anything capable of generating or holding a static charge onto the work station surface.
5. Pick up a part by the body, never by the leads.
6. Keep the device leads shorted together whenever possible.
7. Do not subject a device to sliding movements over any surface.
8. Avoid handling parts in areas having a floor or work surface covering that contributes to the generation of a static charge.
9. Use a soldering iron that has a connection to earth ground.
10. For desoldering, use a special anti-static suction-type tool, such as the Silverstat Soldapullt, or a wick-type desoldering tool.

REDUCING SUSCEPTIBILITY TO STATIC DISCHARGE

This equipment and its supporting system incorporate a number of safeguards to reduce the chance of static discharge damage.

CAUTION

Violation or modification of the following safeguards can result in ground loops and/or static discharge problems.

1. The ground (earth) wire of the primary power cable is connected to the chassis where the cable enters the unit.
2. Shields of interconnecting cables are grounded to the chassis at the point of connection to each unit.
3. Ground loops have been avoided by installing a common ground between all units.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, and performance checks. The preventive maintenance schedule established for the equipment should be based on the amount of use, and on the environment in which the equipment is operated.

Cleaning

Clean the equipment often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulator and prevents efficient heat dissipation. It also provides high-resistance electrical leakage paths between conductors or components in a humid environment.

CAUTION

Do not allow water to get inside any enclosed assembly or components, such as switch assemblies, potentiometers, etc. Do not clean any plastic materials with organic cleaning solvents (such as benzene, toluene, xylene, acetone, or similar compounds); such solvents may damage the plastic.

Exterior

Clean dust from the outside of the equipment by cleaning the surface with a soft cloth or brush. The brush will remove dust from around the front panel controls. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

Interior

Clean the interior by loosening accumulated dust with a soft, dry brush, then blow the loosened dirt away with low-pressure air. To clean a circuit board, remove the circuit board and clean it with a soft, dry brush. Hardened dirt or grease may be removed with a cotton-tipped applicator dampened with a solution of mild detergent and water. Abrasive cleaners should not be used.

After cleaning, allow the interior to dry thoroughly before applying power to the equipment.

Visual Inspection

After cleaning, carefully check the equipment for such defects as poor connections and damaged parts. For most visible defects, the remedy is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before replacing the damaged part; otherwise, the damage may be repeated.

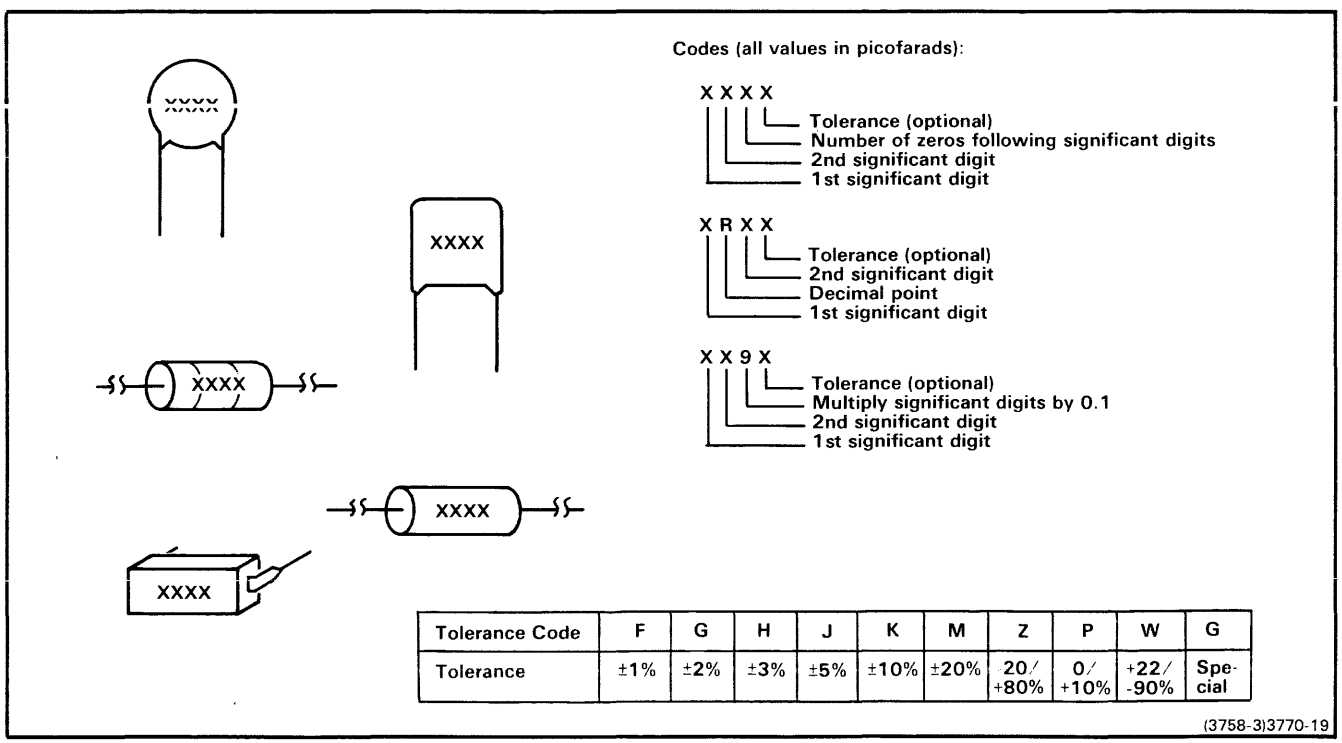
SERVICING AIDS

Diagrams

Circuit diagrams appear on foldout pages in the Diagrams section of the manual. The circuit number and electrical value of each component are shown on the diagram. (See the first tab page for an explanation of the symbols used to identify components in each circuit.) Components on circuit boards are assigned vertical and horizontal grid numbers, which correspond to the location of the component on the circuit board. Refer to the Replaceable Electrical Parts section for a complete description of each component and assembly. Those portions of the circuit that are on circuit boards are enclosed with a black border line, with the name and assembly number shown on the border.

Circuit Board Illustrations

Electrical components, connectors, and test points are identified on circuit board illustrations located on the inside fold of the corresponding circuit diagram, or on the back of the preceding diagram. This allows cross-referencing between the diagram and the circuit board, and shows the physical location of components.



Tolerance Code	F	G	H	J	K	M	Z	P	W	G
Tolerance	±1%	±2%	±3%	±5%	±10%	±20%	20/ +80%	0/ +10%	+22/ -90%	Special

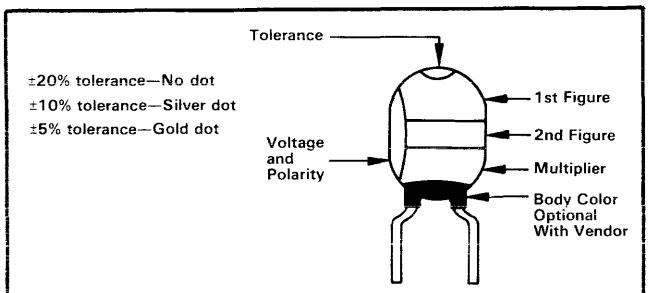
Fig. 8-1. Ceramic and film capacitor code.

Capacitor Marking

The capacitance (in microfarads or picofarads) and voltage ratings of many ceramic, mica, plastic film, and electrolytic capacitors are marked on the component body. The values of other ceramic disc and plastic film capacitors, as well as monolithic ceramic capacitors (such as DIP and glass encapsulated types), are marked according to the code shown in Fig. 8-1. Tantalum capacitors are marked in microfarads or according to the color code shown in Fig. 8-2.

Resistor Marking

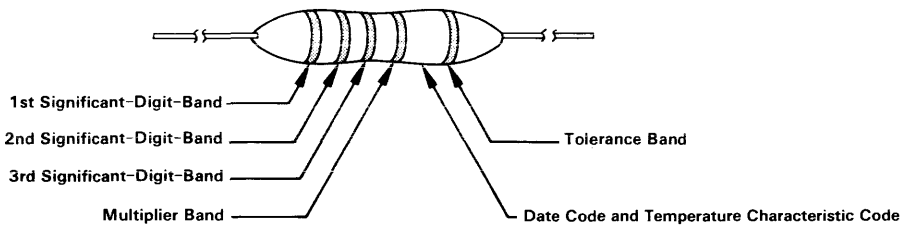
Carbon resistors are marked according to the standard 4-band resistor color code. The fifth band, if present, indicates the device's failure rate. Metal film resistors are marked according to either the standard 4-band resistor color code or to the 5-band color code shown in Fig. 8-3.



Color	+85 C Voltage	Capacitance in Picofarads 1st Figure	2nd Figure	Multiplier
Black	4	0	0	—
Brown	6	1	1	—
Red	10	2	2	—
Orange	15	3	3	—
Yellow	20	4	4	$x10^4$
Green	25	5	5	$x10^5$
Blue	35	6	6	$x10^6$
Violet	50	7	7	$x10^7$
Gray	—	8	8	—
White	—	9	9	—

(3758-4)3770-20

Fig. 8-2. Tantalum capacitor color code.



DATE CODE INFORMATION

YYWW

Week of the year (may be from 01-52).

Last two digits of the year.

COLOR BAND INFORMATION

Color	1st Sig. Digit	2nd Sig. Digit	3rd Sig. Digit	Multiplier	Tolerance ± %	
Black	0	0	0	1	—	
Brown	1	1	1	10	1.	F
Red	2	2	2	100	2.	G
Orange	3	3	3	1,000	3.	H
Yellow	4	4	4	10,000	—	
Green	5	5	5	100,000	.5	D
Blue	6	6	6	1,000,000	.25	C
Violet	7	7	7	10,000,000	.1	B
Grey	8	8	8	100,000,000	.05	A
White	9	9	9	1,000,000,000	—	
Gold				.1	5.	J
Silver				.01	10.	K
No Color					15.	L
No Color					20.	M

TEMPERATURE CHARACTERISTIC INFORMATION

Temperature Characteristic Code	Temperature Coefficient (PPM/°C)	Temperature Range (°C)
T-0 D (C-0)	0 to ±150	-55 to +175
T-00	0 to ±200	-55 to +175
T-1 D (C-1)	0 to ±100	-55 to +175
T-2 C (C-2)	0 to ± 50	-55 to +175
T-9 E (C-3)	0 to ± 25	-55 to +175
T-10	0 to ± 15	-20 to + 85
T-13	0 to ± 10	-20 to + 85
T-14	0 to ± 20	-20 to + 85
T-15	0 to ± 25	-20 to + 85
T-16	0 to ± 5	-20 to + 85
T-18	0 to ± 2	0 to + 60
T-18	0 to ± 5	-55 to +125
T-B	0 to ± 10	25 to -125
T-E	0 to +100 -500	-55 to +175
T-R	0 to +100 -250	-55 to +175

(3758-5)3770-21

Fig. 8-3. Metal film resistor color code.

Diode Code

Diode cathodes are marked by a stripe, a series of stripes, or a dot on the diode body. Some diodes have a diode symbol printed on one side. Figure 8-4 illustrates some common diode types and polarity markings.

Coil and Transformer Identification

Coils and transformers used in this product are identified by Tektronix part numbers. If the number appearing on the part consists of only four digits, a prefix number must be added to obtain the complete part number:

Classification	Part No. Prefix
Fixed coils	108-XXXX-XX
Variable coils	114-XXXX-XX
Transformers	120-XXXX-XX

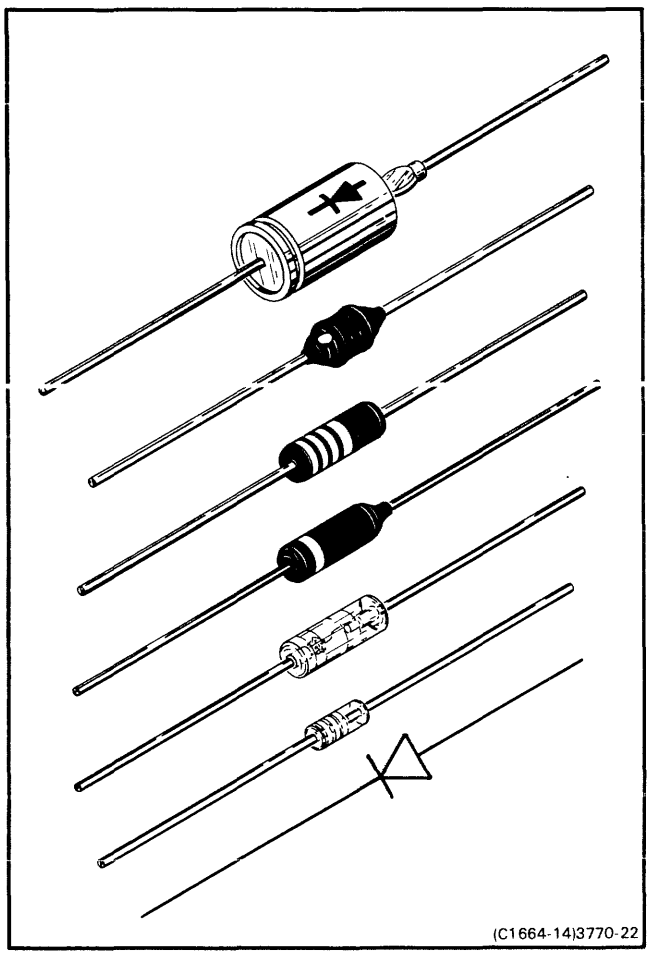


Fig. 8-4. Diode polarity markings.

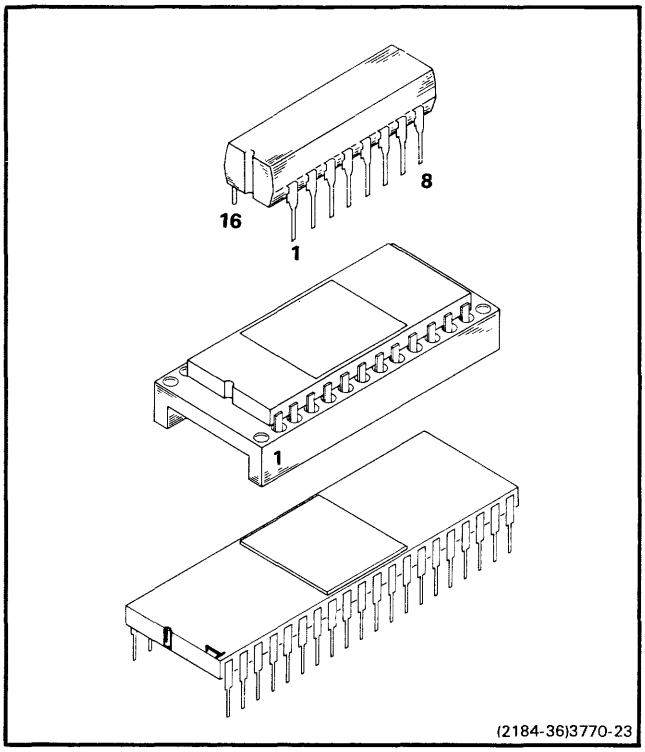


Fig. 8-5. Integrated circuit pin 1 identification.

Transistor and Integrated Circuit Pin Configuration

Lead identification drawings for transistors and 3-lead integrated circuits are included with the schematic diagrams. Pin 1 identification for typical DIP integrated circuits is illustrated in Fig. 8-5.

Obtaining Replacement Parts

Most electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Electrical and Mechanical Parts sections contain information on how to order these replacement parts. Many standard electronic components can be obtained locally in less time than required to order from Tektronix, Inc. It is best to duplicate the original component as closely as possible. Parts orientation and lead dress should be duplicated, since orientation may affect circuit interaction.

If a component you have ordered has been replaced with a new or improved part, your local Field Office or representative will contact you concerning the change in the part number.

ASSEMBLY REPAIR AND EXCHANGE PROGRAM

Tektronix service centers provide replacement or repair of TEKTRONIX equipment and major assemblies. Contact your local service center for this service.

Prototype Control Probe Disassembly/Assembly

Some configuration options are selected by positioning jumper blocks in the Prototype Control Probe's Interface Assembly. The jumpers discussed in Section 3 of this manual are located on the Control, Buffer, and Mobile Microprocessor boards. To gain access to these boards, perform the following procedure:

1. Ensure that primary power (115 Vac or 230 Vac) to the microcomputer development system is OFF.
2. Remove the four screws at the corners on the bottom of the Interface Assembly housing.

CAUTION

The Power Supply board is mounted to the top cover of the Interface Assembly. The Power Supply board is connected to the main housing by four ribbon cables. Take care not to damage these cables when removing the top cover and housing spacer.

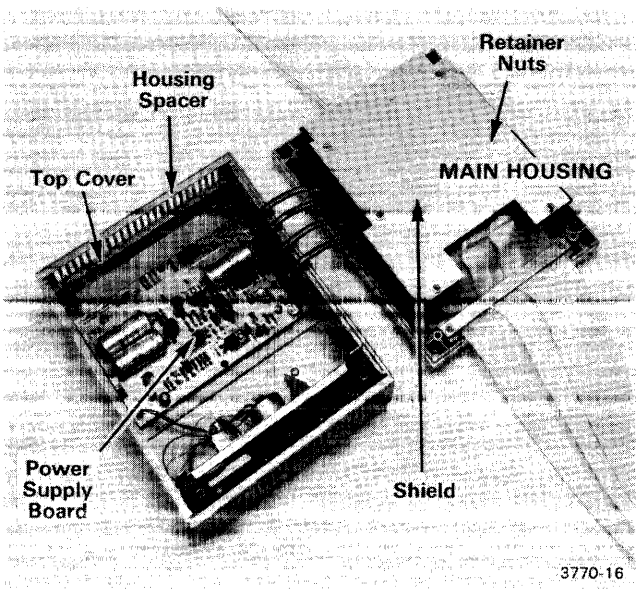


Fig. 8-6. Access to Power Supply board.

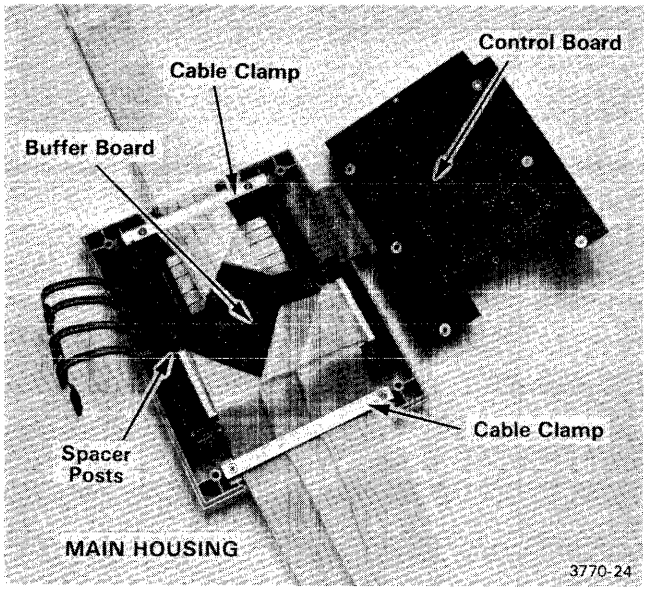


Fig. 8-7. Access to Control board and Buffer board.

3. Remove the top cover of the Interface Assembly and set it beside the main housing (see Fig. 8-6).
4. Lift the housing spacer and rotate it to set on the top cover (see Fig. 8-6).
5. Disconnect the four ribbon cables (J1010, J1020, J1030, and J1040) from the Power Supply board. Then set the top cover and housing spacer aside.
6. Remove the six retaining nuts from the metal shield on top of the main housing. Then remove the shield by lifting straight up, and set it aside.
7. Lift the Control board away from the main housing and drape it to one side, as shown in Fig. 8-7. Take care not to damage the interconnecting ribbon cable.

NOTE

Now you may select configuration jumpers on either the Buffer board or the Control board. Refer to the Configuration Jumpers discussed in Section 3, for more specific information.

8. Remove the six spacer posts. Note that the shorter threads are used to retain the Buffer board in place.
9. Remove the two cable clamps located at each end of the main housing.

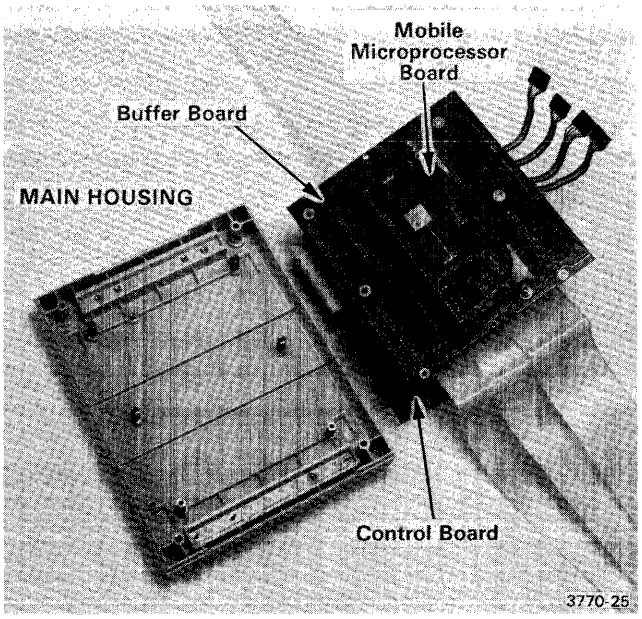


Fig. 8-8. Access to Mobile Microprocessor board.

10. Lift the Buffer board and turn it over to expose the Mobile Microprocessor board (refer to Fig. 8-8).

NOTE

Now you may select configuration jumpers on the Mobile Microprocessor board. Refer to the Configuration Jumpers discussed in Section 3, for more specific information.

11. After you have selected the configuration jumpers, reassemble the Interface Assembly in reverse order of disassembly.

TROUBLESHOOTING

Before you begin any troubleshooting work, check your warranty or service agreement. For your warranty to remain in effect, all service must be performed by Tektronix, Inc., for the first 90 days following delivery.

Your Tektronix Service Support Center is best suited to perform repairs on this unit. However, the following general troubleshooting procedures may aid you in tracing a problem to its source.

Initial Equipment Checks

Before you start any detailed troubleshooting of the equipment, perform the following basic equipment checks:

- Verify that all system equipment is operating correctly.
- Check all mainframe power supply levels.
- Check that all cabling is installed properly.
- Shut off primary power to the development system, and remove the appropriate circuit boards. Clean the circuit board's edge connectors, and put the board back in the development system's card cage.
- Check all power supply levels (these levels are accessible at test points on each board).
- If a duplicate set of boards is available, try swapping the boards, one by one, to find the defective board.

Will Not Boot Up (Disk-Resident Systems Only)

- Try using another operating system disk.
- If, after boot-up, the front panel SYSTEM LED does not come on, check the SYSTEM LED and/or replace the Emulator Controller board.

Emulation Problems

If the system does not function properly in Emulation Mode 1, check the following:

- Check that the Prototype Control Probe is properly installed.
- Check for broken pins on the DIP plug, or a broken socket on the prototype.
- Check the clock input to the Emulator Processor to verify the presence and level of the prototype clock.
- Check the prototype power supplies.
- If mapped memory is being used, check that the System Controller board is plugged into the Main Interconnect board.

If the system fails in Emulation Modes 1 or 2, check that the signals that exist on the emulating microprocessor also exist at the prototype socket. If they do not, check the Prototype Control Probe. If the signals do exist at the prototype socket, refer to the Theory of Operation section of this manual and check the operation of the Emulator Processor.

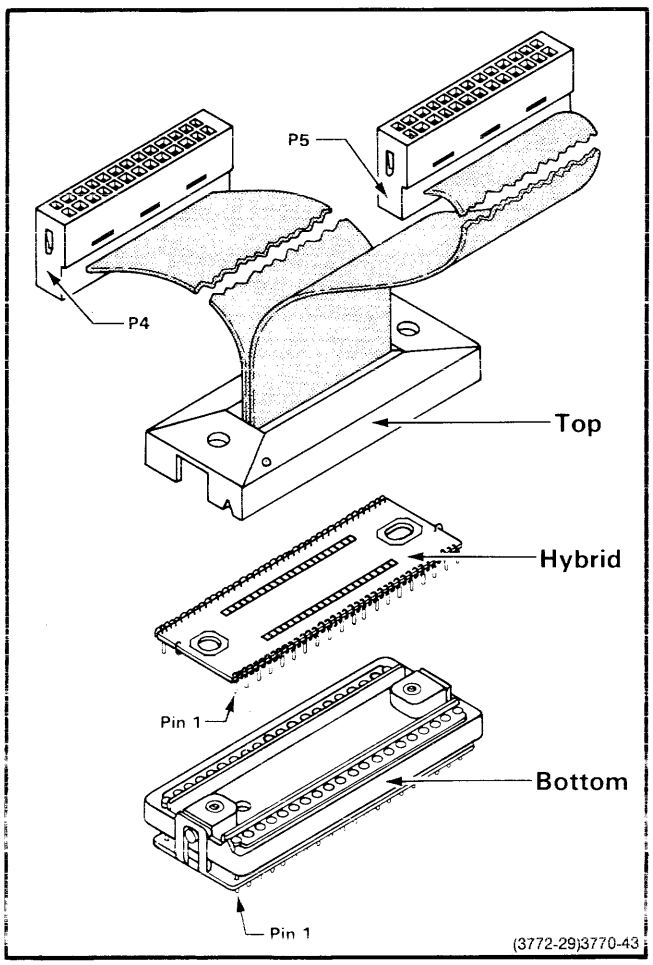


Fig. 8-9. 68000 Prototype Control Probe plug.

Servicing the Prototype Control Probe Plug

The 68000 Prototype Control Probe plug contains interface circuitry in the form of a hybrid device. (See Fig. 8-9.) For access and general maintenance of this hybrid device, perform the following procedure:

1. Ensure that primary power (115 Vac or 230 Vac) to the microcomputer development system is OFF.

CAUTION

The Prototype Control Probe's 64-pin plug is extremely sensitive. Do not attempt to service the plug. Refer any servicing or parts replacement to a qualified Tektronix service representative.

2. Remove the two screws at the top of the plug housing, and open the Prototype Control Probe plug housing.
3. Use magnification to inspect the top of the plug housing (wire side). Check for wire alignment and for cleanliness.
4. Clean the top of the plug housing (wire side) by spraying briefly with freon spray. (No part of the plug housing or hybrid should be sprayed for longer than ten seconds.)
5. If the hybrid must be removed, proceed to step 5. If you aren't going to remove the hybrid, skip to step 8.
6. Using a fiber alignment tool (such as a "spudger"), or your fingernails, gently pry up along the long sides of the hybrid. Take care that you don't bend any of the pins.

CAUTION

Do not use any metal tools to remove the hybrid from the bottom of the Prototype Control Probe plug housing. The hybrid is extremely susceptible to physical damage.

7. Clean the pin side of the hybrid with freon spray. (Recall the 10 sec. warning in step 3.)
8. To replace the hybrid, first align the hybrid's pins with the sockets in the bottom of the plug housing. (Pin 1 is marked with a "1" on both sides of the hybrid. Pin 1 of the plug housing is marked with a notch.) Then press down on the hybrid with your fingers, distributing pressure evenly on the hybrid.
9. Clean the exposed part of the hybrid with freon spray. (Recall the 10 sec. warning in step 3.)
10. Carefully mate the top and bottom of the plug housing; the wires in the top of the plug housing must remain in the correct position.
11. Replace the two screws removed in step 1; maintain equal pressure on the two screws. Do not overtighten the screws—the plug housing or hybrid may crack if the screws are torqued to a pressure greater than 2.0 inch-lbs (.23 N-m).

Section 9

INSTALLATION PROCEDURES

INTRODUCTION

This section tells how to install the 68000 Emulator Processor and its Prototype Control Probe in your TEKTRONIX microcomputer development system. This section also contains information on how to connect the 68000 Emulator Processor to the TTA and MAC options, and how to connect the 64-pin probe plug to your prototype circuit.

CAUTION

Before you insert or remove any module, ensure that primary power to the microcomputer development system is OFF. Inserting or removing a module (or board) while the power is ON may result in component damage.

CAUTION

Under no circumstances can any other Emulator Processor be installed in any TEKTRONIX microcomputer development system while the 68000 Emulator Processor is installed. Excessive power supply loading will result.

INSTALLING THE EMULATOR PROCESSOR AND PROTOTYPE CONTROL PROBE

The 68000 Prototype Control Probe, with its Cable Termination board, is attached to EMU 1 of the 68000 Emulator Processor. The 68000 Emulator Processor, with the Prototype Control Probe attached, is then installed in your development system. To install the 68000 Emulator Processor, perform the following procedure:

1. Verify that primary power (115 Vac or 230 Vac) to the microcomputer development system is OFF.
2. Remove the cover retainers at the upper corners on the rear of the mainframe (Fig. 9-1).
3. Remove the top cover by sliding it straight back, then set it aside.

NOTE

If you are installing the 68000 Emulator Processor in an 8540 Integration Unit, take the time now to install the ROM packages provided. Refer to your 8540 Integration Unit Installation Guide for the installation procedure.

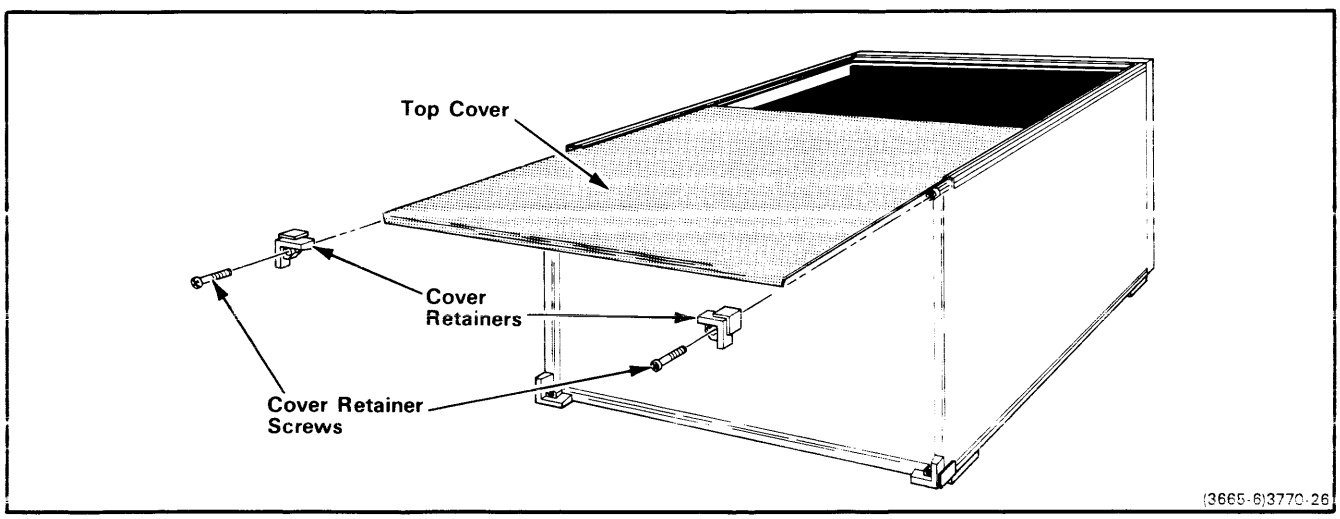


Fig. 9-1. Removal/installation of top cover.

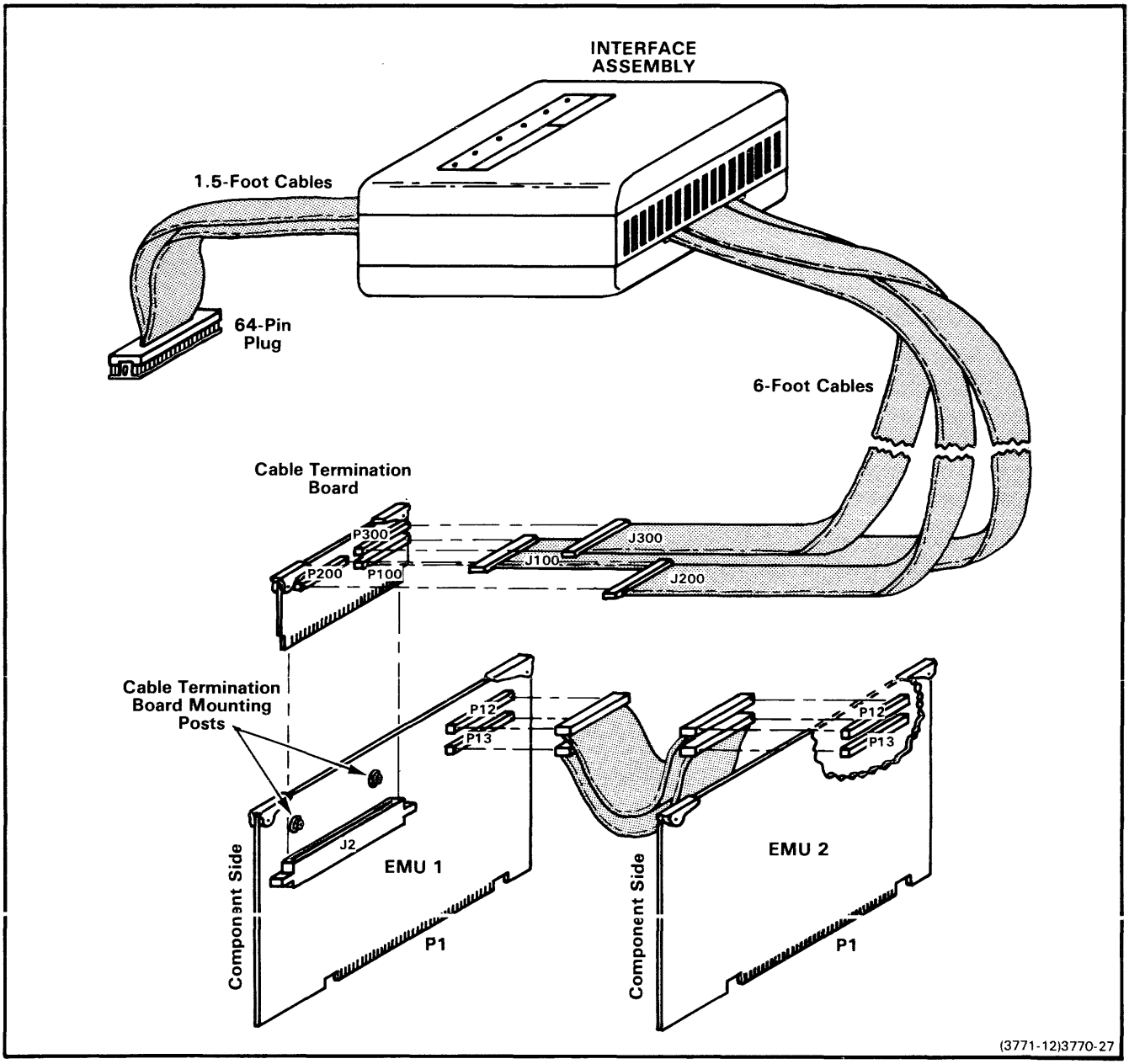


Fig. 9-2. 68000 Emulator Processor with Prototype Control Probe.

4. Remove the two retaining screws from the Cable Termination board mounting posts located on EMU 1 (see Fig. 9-2).

5. Hold the Cable Termination board above J2 on EMU 1. Make sure the component side of the Cable Termination board faces away from EMU 1.

6. Guide edge connector P2 of the Cable Termination board into socket J2 on EMU 1.

7. Install the two retaining screws, removed in step 4, at the upper corners of the Cable Termination board. Tighten the screws securely.

8. Connect EMU 1 (with Cable Termination board) to EMU 2, using the two short ribbon cables provided. Dress the cables as illustrated in Fig. 9-3.

9. Facing the front of the mainframe, hold EMU 1 and EMU 2 by their upper edges. With the component sides facing left, align the boards with other modules in the mainframe.

10. Guide EMU 1 and EMU 2 down the vertical channels to J15 and J16, respectively, on the Main Interconnect board (refer to Fig. 9-4).

NOTE

Don't snap EMU 1 and EMU 2 into place yet. You may need to lift the boards slightly when performing later steps in this procedure.

11. Remove the two mounting screws at the top and bottom of the strain relief plate, as shown in Fig. 9-5. Then remove the strain relief/cable clamp assembly from the rear panel.

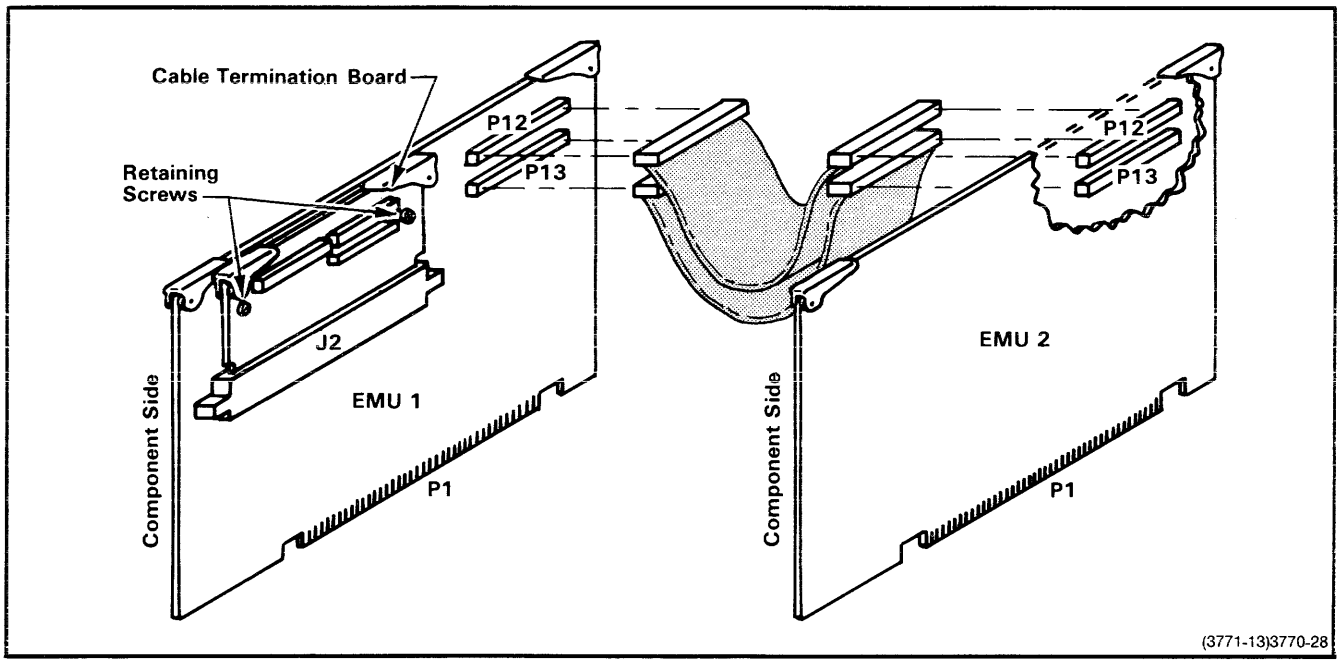


Fig. 9-3. EMU 1/EMU 2 interconnection with Cable Termination board.

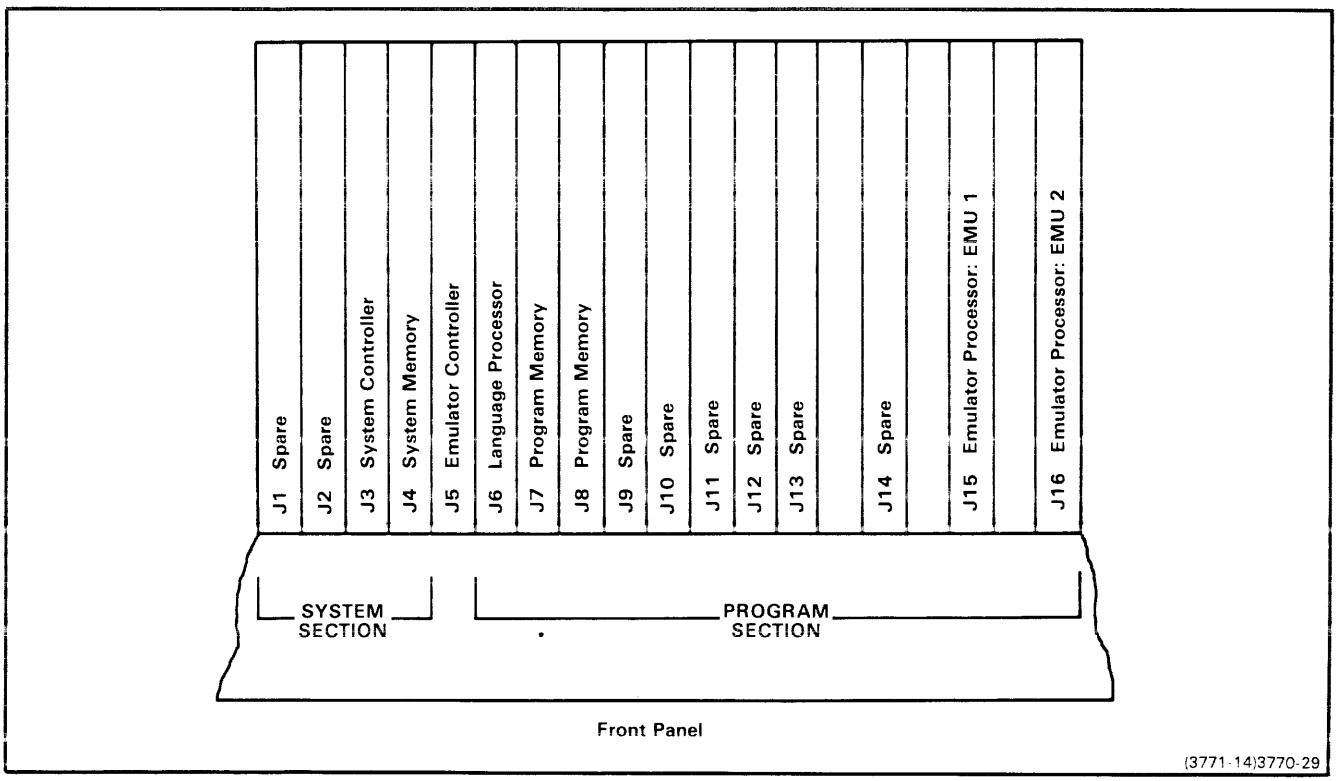


Fig. 9-4. Recommended module arrangement.

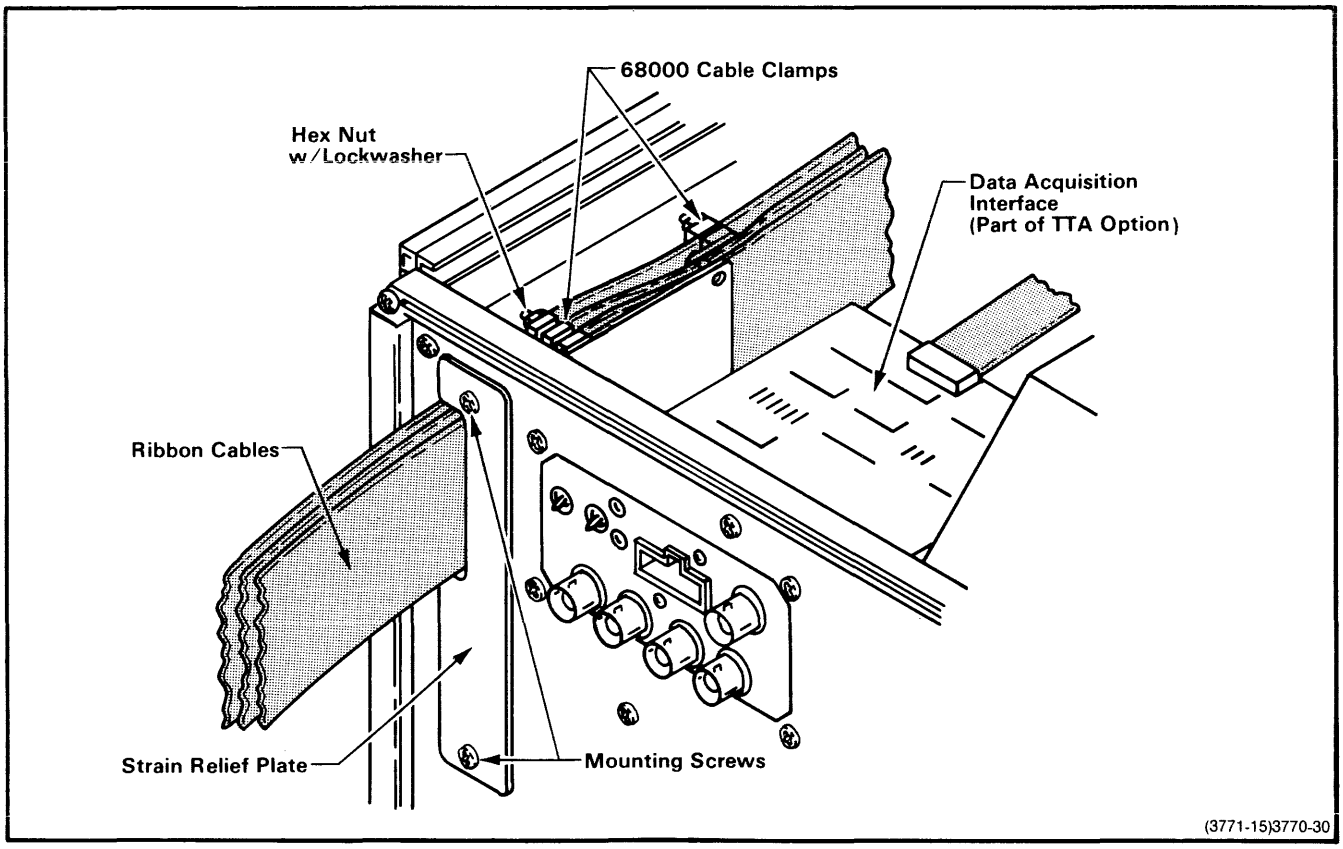


Fig. 9-5. Strain relief plate installation/removal.

NOTE

The standard cable clamps provided with your development system are not compatible with the ribbon cables used with the 68000 Prototype Control Probe. The standard clamps must be replaced with the clamps provided with your 68000 Prototype Control Probe.

12. Make sure you have allowed enough ribbon cable to reach the Cable Termination board (already attached to EMU 1), which is now located in the development system's card cage. Then mount the long Prototype Control Probe ribbon cables to the cable clamp assembly, using the new clamps provided. Secure the cable clamps with hex nuts and lock washers. Refer to Fig. 9-6.

13. Feed the Prototype Control Probe connectors (J100, J200, and J300) through the cableway opening. Then guide the strain relief/cable clamp assembly into the cableway opening. Attach the strain relief plate to the rear panel, using the two screws removed in step 11.

14. Attach the ribbon cable connector labeled J300 to P300 on the Cable Termination board (refer back to Fig. 9-2). Be sure that pin 1 of the cable connector (blue stripe) and pin 1 of the module socket align and are to the left when viewed from the component side of the module.

15. Following the procedure of step 14, attach ribbon cable connector J200 to P200 on the Cable Termination board.

16. Following the procedure of step 14 again, attach ribbon cable connector J100 to P100 on the Cable Termination board.

17. Now slide EMU 1 and EMU 2 down until they reach their respective connectors on the Main Interconnect board in your development system's mainframe. Then press down firmly and evenly on the top edges (one board at a time), until each board snaps into place.

18. Dress the cables along the cableway at the side of the mainframe and over the side of the card cage. Make sure the cables are dressed to lie flat, to allow clearance for the top cover.

19. Slide the top cover back into the guide tracks at the top of the mainframe. Be sure the cover is properly seated in the slot at the front of the mainframe.

20. Install the cover retainers at the upper corners on the rear of the mainframe (see Fig. 9-1). Tighten the cover retainer screws securely.

CONNECTING TO OPTIONS

The following procedures describe how to connect the 68000 Emulator Processor to the Trigger Trace Analyzer (TTA) option and Memory Allocation Controller (MAC) option. The first procedure describes connecting the Emulator Processor to both options. The second procedure describes connecting the Emulator Processor to the TTA only. The third procedure describes connecting the Emulator Processor to the MAC only.

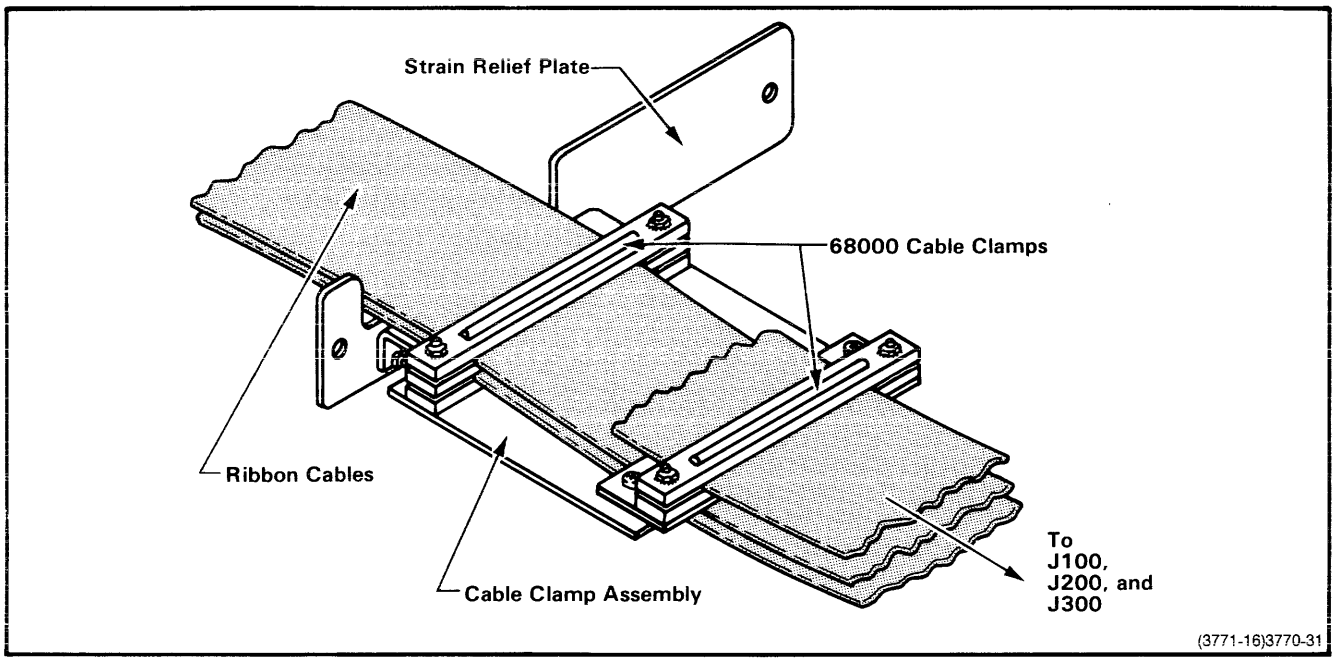


Fig. 9-6. Ribbon cable installation.

Connecting to the TTA and MAC Boards (Optional)

When the TTA and MAC boards are used with the 68000 Emulator Processor, they must be installed as shown in Fig. 9-7. Refer to the Memory Allocation Controller and Trigger Trace Analyzer Installation Service Manuals for information specific to each option.

To install the TTA, MAC, and Emulator Processor, perform the following procedure:

1. Attach connector J1 of the TTA/Emulator Interconnect cable to P1, on the etched side of TTA Circuit Board no. 1.
2. Attach connector J2 of the TTA/Emulator Interconnect cable to P2, on the etched side of TTA Circuit Board no. 1.
3. Install the TTA, using the procedures described in the Trigger Trace Analyzer Installation Service Manual. (Don't replace the cover of the microcomputer development system until this entire procedure is completed.)
4. Set the jumpers and switch on the MAC board as shown in Table 9-1.
5. Install the MAC board in position J14 of your development system, using the procedures described in the Memory Allocation Controller Installation Service Manual.
6. Attach the middle connector of the TTA/Emulator Interconnect cable to P6 on the MAC board.
7. Install the 68000 Emulator Processor in positions J15 and J16 of your development system, using the procedures described earlier in this section.

Table 9-1
MAC Jumper and Switch Settings

Jumper/ Switch	Designation	Setting
J2101	Address Range jumper	12–25[a]
J3151	Block Size jumper	A12
J5140	Block Size jumper	A12
SW2180	Address Feedthrough switches	All OPEN (OFF)

[a] **The most significant address line generated by the 68000 Emulator Processor is A25.**

8. Attach connector J6 of the TTA/Emulator Interconnect cable to P6 on EMU 1 of the 68000 Emulator Processor.
9. Attach connector J7 of the TTA/Emulator Interconnect cable to P7 on EMU 1.
10. Replace the top cover of the development system, using the procedures described earlier in this section.

CAUTION

When removing either the 68000 Emulator Processor or the MAC board from this configuration, be sure to first remove the TTA/Emulator Interconnect cables from the appropriate board(s). Failure to do so may result in damage to the connector pins.

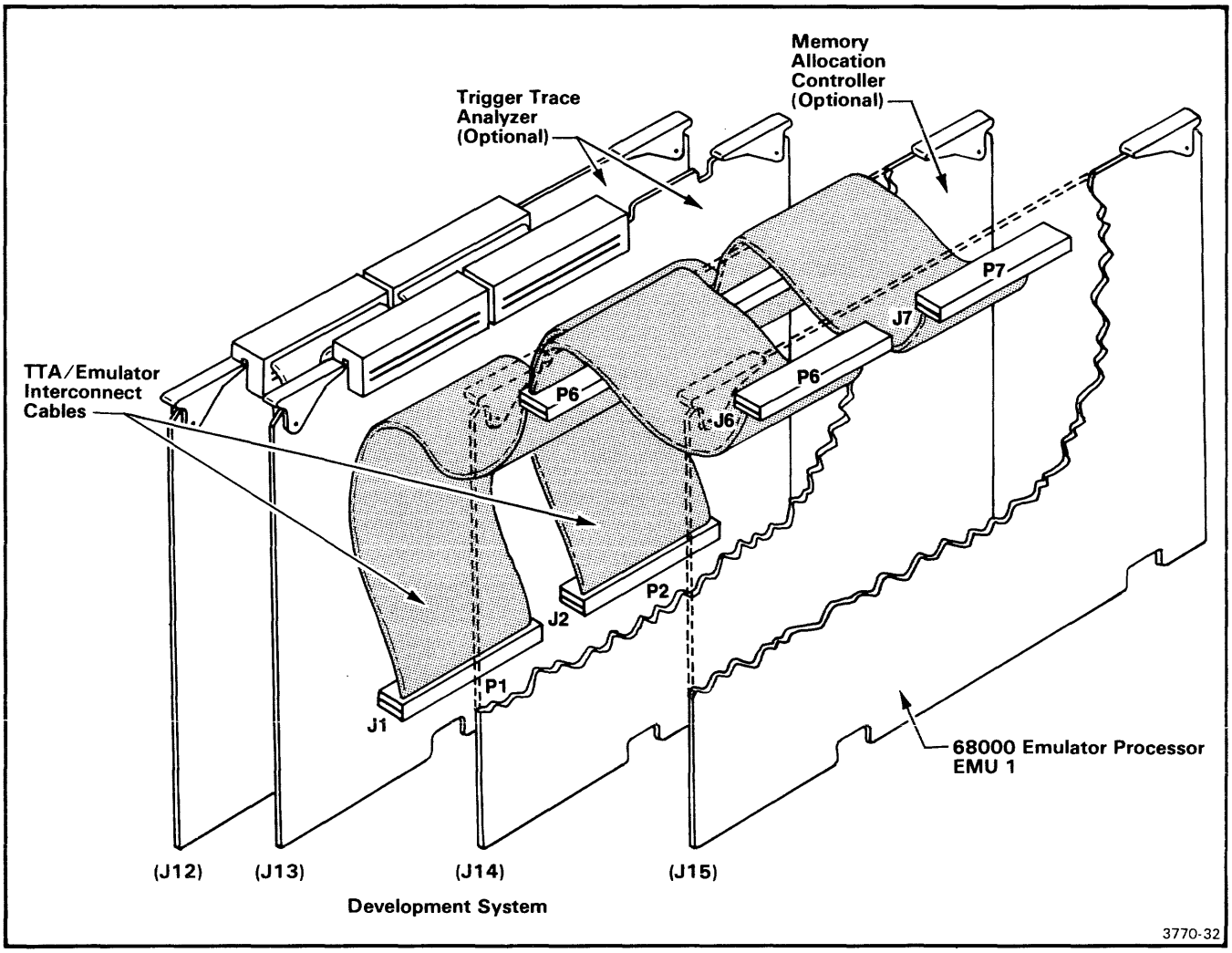


Fig. 9-7. Connecting the 68000 Emulator Processor to the optional Memory Allocation Controller Board.

Connecting to the TTA Only (Optional)

The following procedure tells how to connect the 68000 Emulator Processor to the optional Trigger Trace Analyzer (TTA). If you are planning to use both a TTA and a MAC board in your development system, refer to the TTA/MAC board installation procedure, earlier in this section.

Figure 9-8 shows the connection between the TTA and the Emulator Processor. To install the TTA with the 68000 Emulator Processor, perform the following procedure:

1. Install the Emulator Processor in your development system, using the procedures described earlier in this section. (Don't replace the cover of the microcomputer development system until this entire procedure is completed.)
2. Attach connector J1 of the TTA/Emulator Interconnect cable to P1, on the etched side of TTA Circuit Board no. 1.
3. Attach connector J2 of the TTA/Emulator Interconnect cable to P2, on the etched side of TTA Circuit Board no. 1.
4. Install the TTA, using the procedures described in the Trigger Trace Analyzer Installation Manual.
5. Attach connector J6 of the TTA/Emulator Interconnect cable to P6 on EMU 1 of the 68000 Emulator Processor.
6. Attach connector J7 of the TTA/Emulator Interconnect cable to P7 on EMU 1.
7. Install the top cover on the development system mainframe, using the procedures described earlier in this section.

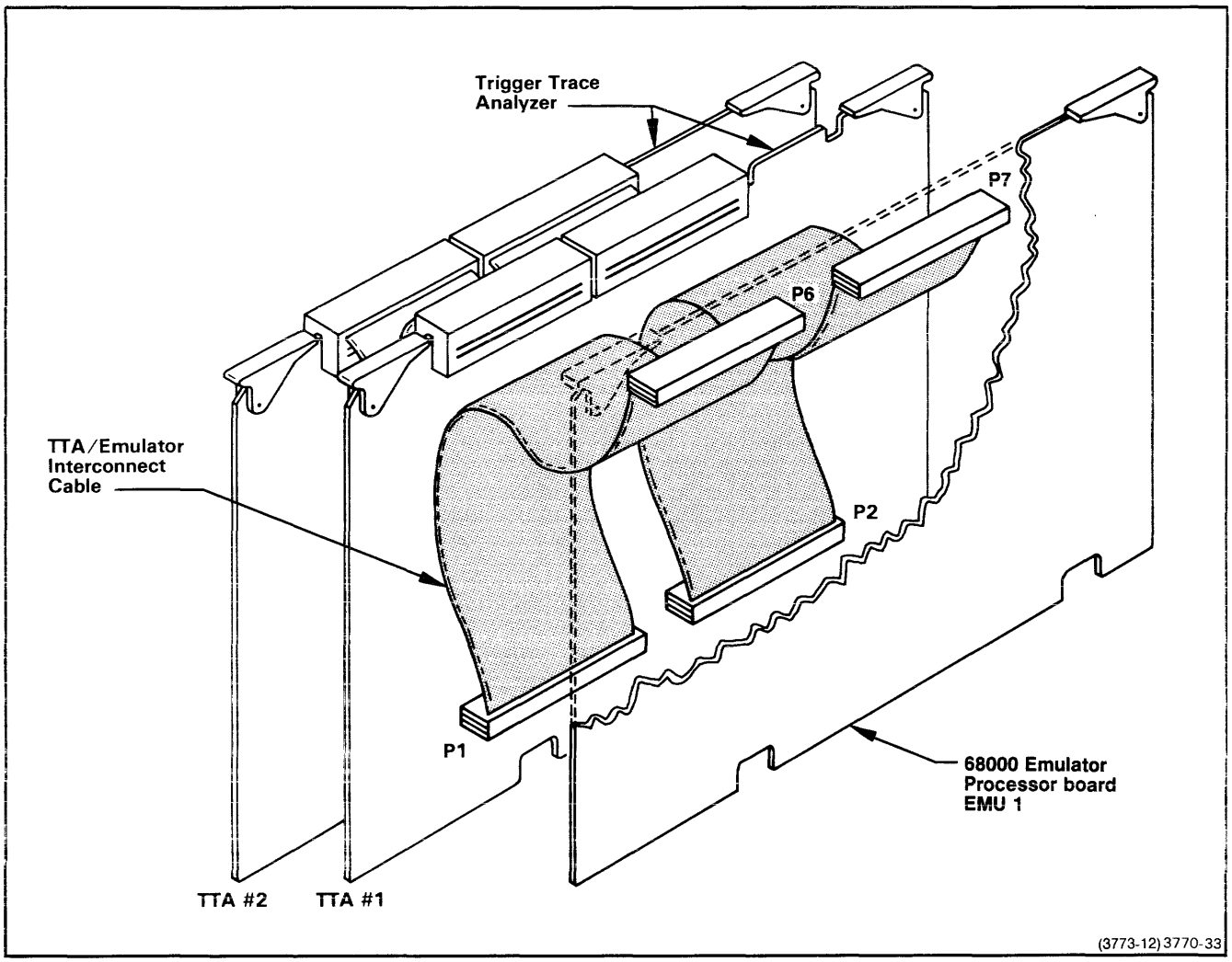


Fig. 9-8. Connecting the 68000 Emulator Processor to the optional Trigger Trace Analyzer.

Connecting to the MAC Board Only (Optional)

The following procedure tells how to connect the 68000 Emulator Processor to the optional Memory Allocation Controller (MAC) board. If you are planning to use both a TTA and a MAC board in your development system, refer to the TTA/MAC board installation procedure, earlier in this section.

To install the MAC board with the 68000 Emulator Processor, perform the following procedure:

1. Install the Emulator Processor in positions J15 and J16 of your development system, using the procedures described earlier in this section. (Don't replace the cover of the microcomputer development system until this entire procedure is completed.)
2. Set the jumpers and switch on the MAC board as shown earlier in Table 9-1.
3. Install the MAC board in position J14 of your development system, using the procedures described in the Memory Allocation Controller Board Installation Manual.
4. Attach the middle connector of the TTA/Emulator Interconnect cable to P6 on the MAC board.
5. Attach connector J6 of the TTA/Emulator Interconnect cable to P6 on EMU 1 of the 68000 Emulator Processor.

NOTE

Connectors J1 and J2 are not connected. Arrange the excess cable so as not to interfere with replacing the development system's top cover.

6. Replace the top cover of the development system, using procedures described earlier in this section.

CONNECTING TO THE PROTOTYPE

The 64-pin plug at the end of the 1.5-foot ribbon cables fits into the 68000 microprocessor socket on the prototype. Pin 1 on the plug must be mated with receptacle 1 on the socket. A notch is located near pin 1 on both the protective spring-loaded plate and the body of the plug, to aid in pin identification (see Fig. 9-9).

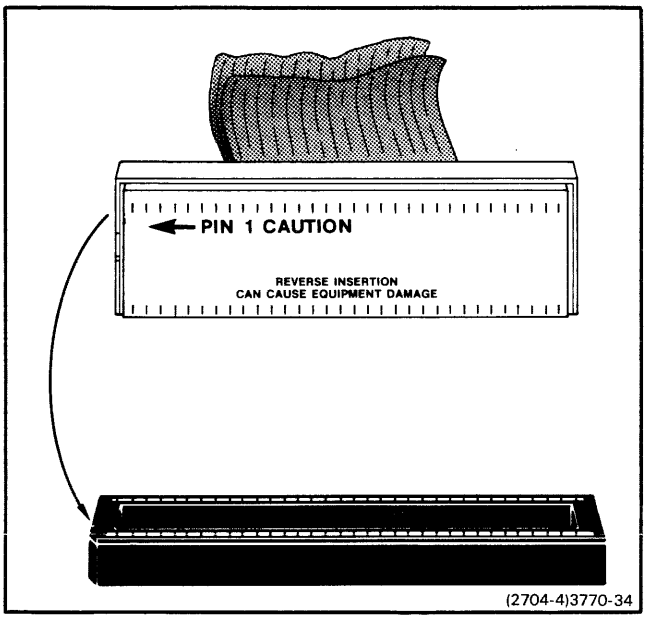


Fig. 9-9. Pin identification and proper plug insertion.

CAUTION

If the Prototype Control Probe plug is incorrectly inserted in the prototype socket, damage to the Prototype Control Probe will result. Figure 9-9 shows the proper method of plug insertion.

If you are using a zero-insertion-force (ZIF) socket for the 68000 microprocessor on your prototype, you should insert a standard low-profile 64-pin DIP socket between the probe plug and the prototype's ZIF socket, to ensure a secure mechanical and electrical connection (see Fig. 9-10).

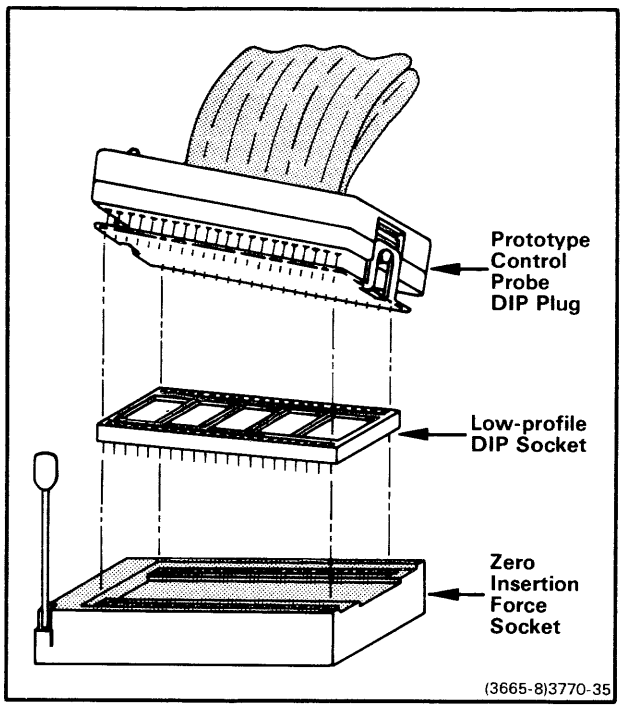


Fig. 9-10. Using a zero-insertion-force socket.

GROUNDING

A proper ground system is mandatory for satisfactory operation of your microcomputer development system. The 68000 Emulator Processor module and its Prototype Control Probe, as well as any other optional and peripheral equipment, must be properly grounded to eliminate ground loops and to reduce susceptibility to static discharge. The following grounding procedures are recommended:

- Ensure that primary power cords of all units (including your prototype system) are connected to outlets that are on the same ground system.
- Attach all grounding strap lugs to the chassis of any unit being grounded. Ensure that the lugs make good contact with bare metal; remove any paint or protective coating from the metal before attaching the ground lug.

Section 10

TECHNICAL REFERENCE MATERIAL

INTRODUCTION

This section contains technical reference material on the 68000 Emulator Processor. The technical reference material includes a circuit block locator, signal summary, test point information, pin connection locators, I/O port configurations, RAM partitioning, memory restrictions, and timing relationships.

CIRCUIT BLOCK LOCATOR

Table 10-1 is a summary of 68000 Emulator Processor circuit blocks and the schematics on which they are located.

Table 10-1
Circuit Block Locator

Circuit Block	Schematic
+4.9V Regulator	24
+5.2V PROBE Regulator	24
2650 I/O Access Decode	10
68000 Read Buffers	2
Address Buffers	1
Asynchronous Break Control	9
Auto Vector Request	6
AUX Control Latch	13
AUX Status Latch	11
BKPT RAM	12
BKPT RAM Multiplexers	12
Breakpoint Interrupt Control	5
Breakpoint Interrupts	13
Buffer Board Feedthroughs	19
Clock Fail Detect	13
Clock Select	17
Command Port	9
Command Port R/W Control	9
D/R Interrupt Trapstack Control	8

Table 10-1 (cont)

Circuit Block	Schematic
D/R PROM	7
Data Buffers	1
DTACK EN/Wait State Generator	20
EMU Control Latch	13
EMU Issued Interrupt Enable Control	21
EMU RAM Access Decode	10
EMU Status Latch	13
Emulator Break Generator	11
F.P. HOLD Interface	6
Factory Test NMI Control	6
Fan Control	24
Function Code Buffer	3
HALT/BR Tri-state Control	22
Internal Address Latches	2
Internal Bus Latch Control	3
Internal Data Bus Latches	2
Interrupt Control Buffers	21
Interrupt State Machine	23
Isolation Buffer Control	3
Jump Acknowledge Generator	11
LED Control	24
MAC Board Address Generator	9
MODE0 Clock	5
Probe Control Signal Generation	16
Probe Interrupt Decode	21
Probe NMI Decode	21
Probe NMI Pending Decode	23
Probe To EMU A/D Buffers	18
Probe To EMU Control Signal Buffer	16

Table 10-1 (cont)

Circuit Block	Schematic
Probe To Prototype A/D Buffers	18
Processor DTACK Generation/Select	17
RESET/HALT Buffers	22
RESET/HALT Control	6
RUN Control	5
Shared RAM	8
Shared RAM Select	8
STOP Instruction Decode	11
SVC	13
System Interface And Control	4
Transfer Into D/R Control	7
Transfer Out Of D/R Control	7
TTA Break Decode	11
TTA Strobe Generator	4
UGET/UPUT Decode	7

Table 10-1 (cont)

Circuit Block	Schematic
UGET/UPUT Or Running Decode	17
UMAP Valid Generator	4
UMAP/Write Protect RAM	14
Upper Address Enable	1
User Bus Request Control	17
User Function Code Buffers	16
User RUN Control	6
User Strobe Enable/Disable	16
Write Protect Interrupt Generator	11

SIGNAL SUMMARY

Table 10-2 is a summary of signals used by the 68000 Emulator Processor.

Table 10-2
Signal Summary

Signal Name	Schematic	Description
2650 HCS	10	2650 High Chip Select. Selects the Shared Communication RAM's high-order byte. Source: U3100A-3
2650 LCS	10	2650 Low Chip Select. Selects the Shared Communication RAM's low-order byte. Source: U3100D-11
2650 RAMAC	10	2650 RAM Access. Indicates that the 2650 is accessing the Emulator Processor's RAM. Source: U4150A-6
8E RD	10	8EH Read. 2650 requests a read of the AUX Status Port (8E). Source: U3130-10
8E WR	10	8EH Write. 2650 requests a write to the AUX Control Port (8E). Source: U3130-14
8F RD	10	8FH Read. 2650 requests a read of the Command Port (8F). Source: U3130-11
8F WR	10	8FH Write. 2650 requests a write to the Command Port (8F). Source: U3130-15
8MHZ	5	8 MHz clock signal. Source: U2180A-6
A0-A23	[a]	Address lines 0-23.
A24	9	Address line 24 (synthetic). Source: U5050B-6
A25	9	Address line 25 (synthetic). Source: U5050C-8
A TO SA	3	Address lines enabled to the Shared Address lines. Source: U5100B-6
A/DTRIST	22	Address/Data Tri-State. Tri-states address and data lines. Source: U3010D-13
ADDR LAT EN	2	Address Latch Enable line. Latches 68000 address lines to shared address lines. Source: U2180-9
ADREAD	10	ADH Read. 2650 requests a read from the EMU Status Port (AD). Source: U3100B-6
ADWRITE	10	ADH Write. 2650 requests a write to the EMU Control Port (AD). Source: U3100B-8
AS	20	Address Strobe line. Source: On-board 68000 microprocessor.
ASYNCBK	9	Asyncronous Break. Generated if a break occurs after a stop instruction has been executed. Source: U2020-9
BA 8E RD	10	Single-buffered 8EH Read (see 8E RD). Source: U2100E-10
BA AS	16	Single-buffered Address Strobe (see AS). Source: U1040-14
BA BERR	17	Single-buffered Bus Error (see BERR). Source: U6020G-5
BA BG	16	Single-buffered Bus Grant (see BG). Source: U1040-18
BA BKCOND	15	Single-buffered Break Condition line (see BKCOND). Source: U1010A-5
BA CLK+25	19	Single-buffered Clock Plus 25 ns line (see CLK+25). Source: U5020B-9
BA CMD=0	9	Single-buffered Command Equal Zero (see CMD=0). Source: U2040-9
BA CPUCLK	17	Single-buffered microprocessor Clock (see CPUCLK). Source: U5020E-7
BA DISABLE WR	15	Single-buffered Disable Write (see DISABLE WR). Source: U2040-3
BA DLYD ACTIVE	15	Single-buffered Delayed Active (see DLYD ACTIVE). Source: U2040-7
BA FC0	16	Single-buffered Function Code 0 (see FC0). Source: U1040-7
BA FC1	16	Single-buffered Function Code 1 (see FC1). Source: U1040-12
BA FC2	16	Single-buffered Function Code 2 (see FC2). Source: U1040-9

[a] **Shown throughout the schematics section.**

Table 10-2 (cont)

Signal Name	Schematic	Description
BA HALT	19	Single-buffered Halt (see HALT). Source: U8040E-9
BA HOLD	15	Single-buffered Hold (see HOLD). Source: U2040-12
BA ID TO/FROM	15	Single-buffered Internal Data To or From the Probe (see ID TO/FROM). Source: U2040-18
BA INTMACHEN	15	Single-buffered Interrupt Machine Enable (see INTMACHEN). Source: U2040-14
BA IPL0	15	Single-buffered Interrupt Line 0 (see IPL0). Source: U1010C-16
BA IPL1	15	Single-buffered Interrupt Line 1 (see IPL1). Source: U1010C-3
BA IPL2	15	Single-buffered Interrupt Line 2 (see IPL2). Source: U1010C-18
BA LDS	16	Single-buffered Lower Data Strobe (see LDS). Source: U1040-16
BA MODE0	15	Single-buffered Mode0 line. (see MODE0). Source: U2040-16
BA MODE2	15	Single-buffered Mode2 line. (see MODE2). Source: U1010A-7
BA PODBKINTA	19	Single-buffered Pod Break Interrupt Acknowledge (see PODBKINTA). Source: U6050F-7
BA R/W	16	Single-buffered Read or Write (see R/W). Source: U1040-3
BA RUNNING	15	Single-buffered Running line (see RUNNING). Source: U1010B-9
BA SLVPSE	11	Single-buffered Slave Pause (see SLVPSE). Source: U2110A-2
BA SMAP	15	Single-buffered System Map (see SMAP). Source: U1010B-14
BA STUSREGPUL	15	Single-buffered Status Register Pull (see STUSREGPUL). Source: U2040-5
BA SYS R/W	10	Single-buffered System Read or Write (see SYS R/W). Source: U4120A-6
BA UDS	16	Single-buffered Upper Data Strobe (see UDS). Source: U1040-5
BA UG/UP+RUNNING	17	Single-buffered UGET, UPUT, or Running (see UG/UP+RUNNING). Source: U5020D-12
BB AS	16	Double-buffered Address Strobe (see AS). Source: U5020C-16
BB DLYD ACTIVE	6	Double-buffered Delaved Active line (see DLYD ACTIVE). Source: U4020F-12
BB CPUCLK	15	Double-buffered Microprocessor Clock (see CPUCLK). Source: U1010D-12
BB CLK+25	15	Double-buffered Clock Plus 25ns (see CLK+25) Source: U2040E-9
BB FC0	17	Double-buffered Function Code 0 line (see FC0). Source: U5020A-18
BB LDS	4	Double-buffered Lower Data Strobe line (see LDS). Source: U2040C-14
BB MODE0	3	Double-buffered Mode0 line (see Mode0). Source: U4100F-12
BB R/W	7	Double-buffered Read or Write line (see R/W). Source: U2040-18
BB RUNNING	13	Double-buffered Running line (see RUNNING). Source: U2110B-4
BC AS	5	Triple-buffered Address Strobe (see AS). Source: U2040C-12
BC CPUCLK	22	Triple-buffered Microprocessor Clock (see CPUCLK). Source: U4040E-10
BC DLYD ACTIVE	22	Triple-buffered Delayed Active line (see DLYD ACTIVE). Source: U4040C-6
BC FC0	3	Triple-buffered Function Code Line 0 (see FC0). Source: U2040-16
BC FC1	3	Triple-buffered Function Code Line 1 (see FC1). Source: U2040-5
BC FC2	3	Triple-buffered Function Code Line 2 (see FC2). Source: U2040-3
BC MODE0	16	Triple-buffered Mode0 line (see MODE0). Source: U5030C-6
BD0-BD7	13	Buffered Data lines 0-7. Source: U5070 or U5080 or U5090

Table 10-2 (cont)

Signal Name	Schematic	Description
BD AS	5	Quadruple-buffered Address Strobe line (see AS). Source: U4040D-11
BD MODE0	22	Quadruple-buffered Mode0 line (see MODE0). Source: U2010B-4
BERR	17	Bus Error line. Source: U6020-7
BG	20	Bus Grant line. Source: On-board 68000 microprocessor.
BGACK	17	Bus Grant Acknowledge line. Source: P3 (normal) U6020-9 or P3 (option) U5010-7
BKCOND	11	Break Condition line. Source: U2050-8
BKINT	6	Break Interrupt line. Source: U2170A-5
BKINTA	7	Break Interrupt Acknowledge line. Source: U4050C-8
BKINTEN	21	Break Interrupt Enable line. Source: U6040C-9
BKPT RD	10	Breakpoint RAM Read enable line. Source: U4100A-3
BKPT1 ARMS BKPT2	13	Breakpoint 1 arms Breakpoint 2 line. Source: U5080-6
BKPT1	13	Breakpoint 1 line. Source: U3110D-11
BKPT2	13	Breakpoint 2 line. Source: U3120A-7
BKPT3	13	Breakpoint 3 line. Source: U3120B-9
BKPT1/0	12	Breakpoint 1's subset 0 line. Source: U3050-10
BKPT2/0	12	Breakpoint 2's subset 0 line. Source: U3050-12
BKPT3/0	12	Breakpoint 3's subset 0 line. Source: U3050-14
BKPT1/1	12	Breakpoint 1's subset 1 line. Source: U3070-10
BKPT2/1	12	Breakpoint 2's subset 1 line. Source: U3070-12
BKPT3/1	12	Breakpoint 3's subset 1 line. Source: U3070-14
BKPT1/2	12	Breakpoint 1's subset 2 line. Source: U3080-10
BKPT2/2	12	Breakpoint 2's subset 2 line. Source: U3080-12
BKPT3/2	12	Breakpoint 3's subset 2 line. Source: U3080-14
BKPT1/3	12	Breakpoint 1's subset 3 line. Source: U3090-10
BKPT2/3	12	Breakpoint 2's subset 3 line. Source: U3090-12
BKPT3/3	12	Breakpoint 3's subset 3 line. Source: U3090-14
BKPTW0	10	Breakpoint 0 Write enable line. Source: U4050B-12
BKPTW1	10	Breakpoint 1 Write enable line. Source: U4050B-11
BKPTW2	10	Breakpoint 2 Write enable line. Source: U4050B-10
BKPTW3	10	Breakpoint 3 Write enable line. Source: U4050B-9
BKSTOP	11	Stop Break line. Asserted when a break is caused by a STOP Instruction when asserted. Source: U3150B-8
BR	17	Bus Request line. Source: P2 (normal) U6020-9 or P2 (option) U5010-7
BRDDTACK	6	Main Board (EMU 1 and EMU 2) Data Transfer Acknowledge line. Source: U4010B-6
BRDHALT	22	Main Board (EMU 1 and EMU 2) Halt line. Asserted when a double bus or address error occurs. Source: U8040A-2
BYTE ADDR	4	Byte Address access line. Asserted when Program Memory is byte-oriented. Source: U2190-7
BYTE/WORD	4	Byte or Word access line. Indicates that access is byte- or word-oriented. Source: U2030-6

Table 10-2 (cont)

Signal Name	Schematic	Description
CLK+25	20	Clock Plus 25 ns. Source: DL1010-8
CLKFAIL	13	Clock Failed line. Source: U3150A-6
CMD=0	9	Command Equals 0. Asserted when there is no command in the Command Port. Source: U3080A-5
CMD PRESENT	9	Command is Present line. Asserted when there is a command in the Command Port. Source: U3030D-13
CMEM	10	Common Memory line. Source: P1-33 (development system)
CPUCLK	17	68000 microprocessor Clock. Source: U5010A-18 OR Q9011
CTRIST	22	Control Tri-State line. Source: U2010C-6
D0-D15	[a]	Data lines 0-15.
D TO SD	3	Data lines are enabled to the Shared Data lines. Source: U4120-8
D/R A2-D/R A9	8	Dump and Restore Address lines 2-9.
D/R D0-D/R D7	8	Dump and Restore Data lines 0-7.
D/R EN	7	Dump and Restore PROM Enable line. Source: U3050B-4
D/R CMDRD	9	Dump and Retore Command Read enable line. Asserted to enable the 68000 to read the Command Port. Source: U5100A-3
DBG INT29	11	Debug Interrupt 29 line. Source: P1-77 (development system)
DATA LAT EN	3	Data Latch Enable line. Enables data to be latched from the 68000. Source: U5050D-11
DISABLE WR	4	Disable Write line. Source: U5080D-11
DLYD ACTIVE	11	Delayed Active line. Indicates that the Emulator Processor is selected (active). Source: U4120C-8
DS	4	Data Strobe line. Source: U5060C-8
DTACK	17	Data Transfer Acknowledge line. Source: U7010-14
DTACKEN	20	Data Transfer Acknowledge Enable line. Source: U2040B-8
DTACK T.O.	16	Data Transfer Acknowledge Time Out line. Asserted when a DTACK has not been received within 1 ms. Source: U4030B-8
E	20	Enable line. Source: On-board 68000 microprocessor
EMU ACTIVE	13	Emulator Active line. Source: U5090-5
EMU RESET REQ	11	Emulator Processor requires reseting. Source: U4160A-6
EN WINDOW	23	Enable Window line. A time frame where the prototype lines are allowed access to the 68000. Source: U5040A-1
FC0	20	Function Code 0 line. Source: On-board 68000 microprocessor
FC1	20	Function Code 1 line. Source: On-board 68000 microprocessor
FC2	20	Function Code 2 line. Source: On-board 68000 microprocessor
FETCH	5	Fetch line. Not Used. Source: U2060H-12
FFC0	13	Forced Function Code 0 line. Source: U5080-2
FFC1	13	Forced Function Code 1 line. Source: U5080-19
FFC2	13	Forced Function Code 2 line. Source: U5080-5
F.P.HOLD	6	Front Panel Hold line. Source: P1-87 (development system)
HALT	20, 22	Halt line. Source: On-board 68000 microprocessor or U8040-4 or U4020B-6

[a] Shown throughout the schematics section.

Table 10-2 (cont)

Signal Name	Schematic	Description
HALTED	6	Halted line. Source: U5090B-4
HAVERUN	11	Has Run line. Asserted after the 68000 has executed one user instruction. Source: U2150B-9
HOLD	6	Hold line. Factory use only. Source: U3040B-6
IA0-IA23	[a]	Internal Address lines 0-23.
IA TO SA	3	Internal Address lines are enabled to the Shared Address lines. Source: U5030D-13
IBKINT	23	Internal Break Interrupt line. Source: U5030A-6
IBYTE/WORD	4	Internal Byte or Word line. Source: U5110C-6
ID0-ID15	[a]	Internal Data lines 0-15.
ID TO SD	3	Internal Data lines are enabled to the Shared Data lines. Source: U5040D-11
ID TO/FROM	3	Internal Data To or From the Interface Assembly. Source: U4060C-6
INTMACHEN	5	Interrupt Machine Enable line. Asserted when user instructions begin running. Source: U2140B-9
IOPREQ	4	Internal Operation Request line. Source: U5040B-6
IPL0	21	Interrupt Line 0. Source: U7010A-14 or U6010A-14 or U6010B-7 or U3000-12
IPL1	21	Interrupt Line 1. Source: U7010A-16 or U6010A-16 or U6010B-5 or U3000-16
IPL2	21	Interrupt Line 2. Source: U7010A-18 or U6010A-18 or U6010B-3 or U3000-14
ISLVOPREQ	4	Internal Slave Operation Request line. Source: U6020A-6
IUINT	23	Internal User Interrupt line. Source: U2020A-6
JMPACK	11	Jump Acknowledge line. Source: U4130B-6
JMPCMD	11	Jump Command line. Source: U4130B-6
LEVEL7	20, 21	Interrupt Level 7 line. Source: On board 68000 microprocessor or J4011 (normal) U4010B-6 or (option) Ground.
LEVEL INT	21	Interrupt Level other than Level 7 line. Source: J6021 (normal) U6020-5 or (option) Ground.
M/IO	4, 10	Memory or I/O operation indicator line. Source: U2190-18 or P1-52 (development system)
MA0-MA3	12	Memory Address lines 0-3. Source: U2030-7, -4, -9, -12
MA4-MA7	12	Memory Address lines 4-7. Source: U1070-4, -7, -9, -12
MA8-MA11	14	Memory Address lines 8-11. Source: U2070-7, -4, -9, -12
MACAVAL	1	Asserted when the MAC board is available and operating. Source: P6-5 (MAC board)
MAPRAMRD	10	UMAP RAM Read line. Source: U4100C-8
MAPRAMWR	10	UMAP RAM Write line. Source: U4100B-6
MSTRRUN	10	Master Run line. Source: P1-84 (development system)
MODE0	13	Mode0 line. Asserted during Mode 0 emulation. Source: U5090-15
MODE0 BKEN	5	Mode0 Break Enable line. Source: U2140A-5
MODE0CLK	5	Mode0 Clock line. Source: U2060C-7
MODE1	13	Mode1 line. Asserted during Mode 1 emulation. Source: U5120C-10

[a] **Shown throughout the schematics section.**

Table 10-2 (cont)

Signal Name	Schematic	Description
MODE2	13	Mode2 line. Asserted during Mode 2 emulation. Source: U4140C-8
NMI PENDING	23	Non Maskable Interrupt Pending line. Asserted when the prototype requests an NMI. Source: U3000E-9
OPEN USER	23	Open for User access line. Source: U4030-8
OPREQ	4, 10	Operation Request line. Source: U2190-9 or P1-54 (development system)
OPREQ EN	9	Operation Request Enable line. Source: U4040A-3
PA1-PA23	[a]	68000 Address lines 1-23.
PD	[a]	68000 Data line.
P.O. RESET	13	Power On Reset line. Source: P1-59 (development system)
PODBKINTA	23	Pod Break Interrupt Acknowledge line. Asserted when a Break Interrupt Acknowledge occurs. Source: U4030-12
PROBEPWR	13	Activates the Probe's Power Supply board. Source: U5090-12
PROBEPWR O.C.	13	Probe Power Open Collector. Source: U5110B-4
PROM	7	D/R PROM select line. Source: U4060F-12
QBG	16	Qualified Bus Grant line. When asserted, turns on Probe LED. Source: U9030C-8
QHALT	22	Qualified Halt line. When asserted, turns on Probe LED. Source: U3020A-12
QINTA7	16	Qualified Interrupt Level 7 Acknowledge line. (Qualified by AS). Source: U9040B-4
QRESET	22	Qualified Reset line. When asserted, turns on Probe LED. Source: U3020B-6
QUINTA	16	Qualified User Interrupt Acknowledge line. (Qualified by AS). Source: U8010B-10
R/W	20	Read or Write line. Source: On-board 68000 microprocessor
RAMEN	13	RAM Enable line. Source: U5090-19
RAMINH	10	RAM Inhibit line. Turns off Program Memory when asserted. Source: U4130A-3, -8, and -11
RESET	20, 6, 22	Reset line. Source: On-board 68000 microprocessor or U2160B-4 or U8040C-6 or U4020C-8
RESET RUN	7	Reset the RUNNING line. Source: U4220-11
RESET SAMPLE	22	Reset Sample line. Resets the prototype interrupt sampling circuit. Source: U2040A-3
RESET SEQ EN	6	Reset Sequence Enable line. Source: U6030A-6
RUN	5	Run line. Source: U2060B-18
RUNNING	6	Running line. Asserted when user instructions are executed. Source: U4060E-10
SA0-SA23	[a]	Shared Address lines 0-23.
SD0-SD15	[a]	Shared Data lines 0-15.
SD TO D	3	Shared Data lines are enabled to the Data lines. Source: U4110-8
SD TO ID	3	Shared Data lines are enabled to the Internal Data lines. Source: U5040A-3
SETRUN	7	Set the RUNNING line. Source: U5120-3
SHARED R/W	10	Shared Read or Write line. Is equal to either the 2650's R/W line or the 68000's R/W line. Source: U2080B-12

[a] Shown throughout the schematics section.

Table 10-2 (cont)

Signal Name	Schematic	Description
SLV CLK	4	Slave Clock line. Source: U2190-14
SLV OPREQ	4	Slave Operation Request line. Source: U2190-5
SLVPSE	5	Slave Pause line. Source: P1-77 (development system)
SMAP	14	System Map line. Asserted when memory is mapped to Program Memory. Source: U1110D-13
SLV PAUSE	5, 11	Slave Pause line. (Synchronized). Source: U5090C-10
ST0/BKINTEN	23	State 0 or Break Interrupt Enable line. Asserted when prototype interrupt acknowledges are to be suppressed. Source: U7030D-11
STUSREGPUL	7	Status Register Pull line. Asserted when the Status Register is unstacked after an RTE instruction has been executed. Source: U2020A-18
SVC0	12	Service Call 0 line. Source: U3050-16
SVC1	12	Service Call 1 line. Source: U3070-16
SVC2	12	Service Call 2 line. Source: U3080-16
SVC3	12	Service Call 3 line. Source: U3090-16
SVC-M/IO	13	Service Call and Memory or I/O line. Source: U4040A-5
SVC ENABLE	13	Service Call Enable line. Source: U5080-9
SWAP	4	Swap line. Used with 32K Program Memory. Source: U2030-12
SYSCLK	11	System Clock line. Source: P1-96 (development system)
SYS R/W	4, 10	System Read or Write line. Source: U2190-12 or P1-55 (development system)
TOPSTRBDATA	4	Top Plane Data Strobe line. Source: U4090D-11
S/CY EN	13	Single Cycle Enable line. Source: U5080-16
UA1-UA23	[a]	Prototype Address lines 1-23.
UACCESS	17	Prototype Access line. Source: U9040C-10
UAS	16	Prototype Address Strobe line (see AS). Source: U9010-18
UBERR	25	Prototype Bus Error line (see BERR). Source: 64-Pin Plug (prototype circuit)
UBG	25	Prototype Bus Grant line (see BG). Source: 64-Pin Plug (prototype circuit)
UBGACK	25	Prototype Bus Grant Acknowledge line (see BGACK). Source: 64-Pin Plug (prototype circuit)
UBR	25	Prototype Bus Request line (see BR). Source: 64-Pin Plug (prototype circuit)
UCLK	25	Prototype Clock line. Source: 64-Pin Plug (prototype circuit)
UD0-UD15	[a]	Prototype Data lines 0-15.
UDS	20	Upper Data Strobe line. Source: On-board 68000 microprocessor
UDS/LDS	16	Upper Data Strobe or Lower Data Strobe line. Source: U7040A-3
UDTACK	25	Prototype Data Transfer Acknowledge line. Source: 64-Pin Plug (prototype circuit)
UE	19	Prototype Enable line. Source: U7010B-6
UFC0	16	Prototype Function Code line 0. Source: U6050-18 or U6020B-18
UFC1	16	Prototype Function Code line 1. Source: U6050-14 or U6020B-14
UFC2	16	Prototype Function Code line 2. Source: U6050-12 or U6020B-12
UG/UP+RUNNING	17	UGET, UPUT, or RUNNING line. Source: U5030B-4

[a] **Shown throughout the schematics section.**

Table 10-2 (cont)

Signal Name	Schematic	Description
UGET	7	UGET line. Source: U6160-7
UHALT	25, 22	Prototype Halt line. Source: 64-Pin Plug (prototype circuit) or U4020A-3
UIPL0	25	Prototype Interrupt Line 0. Source: 64-Pin Plug (prototype circuit)
UIPL1	25	Prototype Interrupt Line 1. Source: 64-Pin Plug (prototype circuit)
UIPL2	25	Prototype Interrupt Line 2. Source: 64-Pin Plug (prototype circuit)
ULDS	16	Prototype Lower Data Strobe line. Source: U9010-7
UMAP	14	User Map line. Asserted when memory is mapped to the prototype. Source: U3110C-8
UMAP EN	4	UMAP RAM Enable line. Asserted when data out of the UMAP/Write Protect RAMs is valid. Source: U6020B-9
UNSTACKING	7	Un-Stack line. Asserted during unstacking process caused by the RTE instruction. Source: U1220C-8
UPUT	7	UPUT line. Source: U6160-4
UR/W	16	Prototype Read or Write line. Source: U9010-3
URESET	25, 22	Prototype Reset line. Source: 64-Pin Plug (prototype circuit) or U4020D-11
UUDS	16	Prototype Upper Data Strobe line. Source: U9010-5
UVMA	16	Prototype VMA line. Source: U9010-9
UVPA	25	Prototype VPA line. Source: 64-Pin Plug (prototype circuit)
VMA	20	VMA line. Source: On-board 68000 microprocessor
VPA	6, 16	VPA line. Source: U2160D-8 or U9030D-11
WD ACCESS	4	Word Access line. Asserted when access is word-oriented. Source: U2030-9
WRP	4, 10	Write Pulse line. Source: U2190-16 or P1-53 (development system)
WRPROT	14	Write Protect line. Source: U1110B-4

TEST POINTS

Test points are available on three 68000 Emulator Processor boards: EMU 1, EMU 2, and Power Supply (located in the Interface Assembly).

EMU 1 has two sets of test points: TP1141 and TP1143. Tables 10-3 and 10-4, summarize these test points and the schematics on which they appear.

Table 10-3
EMU 1 TP1141

Pin	Signal	Schematic
1	SSLVPSE(H)	5
2	A TO SA(L)	3
3	IOPREQ(H)	4
4	ISLVOPREQ(L)	4
5	RESET SEQ EN(H)	7
6	ASYNCBK(L)	9
7	UNSTACKING(L)	7
8	STUSREGPUL(H)	7
9	RESET(L)	7
10	IA TO SA(L)	3

Table 10-4
EMU 1 TP1143

Pin	Signal	Schematic
1	SD TO D(L)	3
2	D TO SD(L)	3
3	BKINTAL(L)	6
4	MODE0 BKEN(H)	5
5	MODE0CLK(H)	5
6	D/R EN(L)	6
7	ID TO SD(L)	3
8	DATA LAT EN(H)	3
9	SETRUN(L)	6
10	SD TO ID(L)	3

EMU 2 has 20 test points available. Table 10-5 is a summary of these test points and the schematics on which they appear.

Table 10-5
EMU 2 Test Points

TP	Signal Name	Schematic
1	BKPT1(L)	13
2	(Not Used)	a
3	BKPT3(L)	13
4	(Not Used)	10
5	(Not Used)	10
6	MAPRAMRD(L)	10
7	MAPRAMWR(L)	10
8	(Not Used)	a
9	BKPT RD(L)	10
10	(Not Used)	a
11	ADREAD(L)	10
12	ADWRITE(L)	10
13	(Not Used)	10
14	8F WR(L)	10
15	(Not Used)	10
16	BKPT2(L)	13
17	BKPTW0(L)	10
18	BKPTW1(L)	10
19	BKPTW2(L)	10
20	BKPTW3(L)	10

[a] **Not shown in schematic section.**

The Power Supply board has two test points available: TP1011 and TP1061. Table 10-6 is a summary of these test points and the schematics on which they appear. TP1011 and TP1061 are used in the adjustment of the power supply output voltages. (Refer to the Prototype Control Probe Power Supply Calibration procedure located in Section 6 of this manual for more information.)

Table 10-6
Power Supply Board Test Points

TP	Signal	Schematic
1011	+5.2V	24
1061	+4.9V	24

PIN LOCATORS

The pin connections associated with the 68000 Emulator Processor are divided into three categories: Main Interconnect Bus, Top Plane, and the 68000 Emulator Processor Interconnections.

Main Interconnect Bus

The Main Interconnect Bus consists of P1 located both on EMU 1 and EMU 2. P1 connects the 68000 Emulator Processor with your development systems' bus on the program side of the mainframe. Table 10-7 is a summary of P1s' pins and the schematics on which they appear.

Table 10-7
Main Interconnect Bus P1

Pin	Signal Name	Schematic	Pin	Signal Name	Schematic
1	+5.2V	5, 14	2	+5.2V	5, 14
3	+5.2V	5, 14	4	+5.2V	5, 14
5	(Not Used)	[a]	6	(Not Used)	[a]
7	(Not Used)	[a]	8	(Not Used)	[a]
9	GND	5, 14	10	GND	5, 14
11	+12V	5	12	+12V	5
13	-12V	5	14	-12V	5
15	GND	5, 14	16	GND	5, 14
17	A0(H)	1, 10	18	A1(H)	1, 10
19	A2(H)	1, 10	20	A3(H)	1, 10
21	A4(H)	1, 10	22	A5(H)	1, 10
23	A6(H)	1, 10	24	A7(H)	1, 10
25	A8(H)	1	26	A9(H)	1
27	A10(H)	1	28	A11(H)	1
29	A12(H)	1	30	A13(H)	1, 10
31	A14(H)	1, 10	32	A15(H)	1, 10
33	CMEM(H)	10	34	RAMINH(L)	10
35	WD ACCESS(L)	4	36	D0(L)	1, 13
37	D1(L)	1, 13	38	D2(L)	1, 13
39	D3(L)	1, 13	40	D4(L)	1, 13
41	D5(L)	1, 13	42	D6(L)	1, 13
43	D7(L)	1, 13	44	D8(L)	1
45	D9(L)	1	46	D10(L)	1
47	D11(L)	1	48	D12(L)	1
49	D13(L)	1	50	D14(L)	1
51	D15(L)	1	52	M(L)/IO(H)	4, 10
53	WRP(L)	4, 10	54	OPREQ(L)	4, 10
55	SYS R(H)/W(L)	4, 10	56	GND	5, 14
57	JMPCMD(L)	11	58	RUN(L)	5
59	P.O. RESET(L)	13	60	JMPACK(L)	11
61	(Not Used)	[a]	62	(Not Used)	[a]
63	A16(L)	1	64	A17(L)	1
65	A18(L)	1	66	A19(L)	1
67	A20(L)	1	68	A21(L)	1
69	A22(L)	1	70	A23(L)	1

[a] Not shown in schematic section.

Table 10-7 (cont)

Pin	Signal Name	Schematic	Pin	Signal Name	Schematic
71	DBG INT29(L)	11	72	(Not Used)	a
73	(Not Used)	a	74	(Not Used)	a
75	SLV OPREQ(L)	4	76	(Not Used)	a
77	SLVPSE(L)	5, 11	78	(Not Used)	a
79	(Not Used)	a	80	SWAP(L)	4
81	(Spare)	a	82	FETCH(L)	5
83	(Not Used)	a	84	MSTRRUN(L)	10
85	GND	5, 14	86	BYTE ADDR(L)	4
87	F.P.HOLD(L)	6	88	(Not Used)	a
89	(Not Used)	a	90	(Not Used)	a
91	(Not Used)	a	92	(Not Used)	a
93	SLV CLK(L)	4	94	(Not Used)	a
95	(Not Used)	a	96	SYSCLK(L)	11
97	GND	5, 14	98	GND	5, 14
99	GND	5, 14	100	GND	5, 14

[a] **Not shown in schematic section.**

Top Plane Connectors

The Top Plane connectors, located on EMU 1, consist of: P6 and P7. These Top Plane connectors are the interface between the 68000 Emulator Processor, Memory Allocation Controller (MAC), and Trigger Trace Analyzer (TTA). (However, P7 does not connect to the MAC.)

Tables 10-8 and 10-9 summarize the pins of P6 and P7, respectively, and the schematic on which each pin appears.

Table 10-8
Top Plane Connector P6

Pin	Signal Name	Schematic
1	A24(H)	9
2	A25(H)	9
3	(Not Used)	a
4	(spare)	a
5	MACAVAL(L)	1
6	(Not Used)	a
7	RUNNING(L)	3
8	GND	5
9	ISLVOPREQ(L)	4
10	GND	5
11	(Not Used)	a
12	GND	5
13	TOPSTRBDATA(L)	4
14	GND	5
15	SA12(H)	1
16	SA13(H)	1
17	SA14(H)	1
18	SA15(H)	1
19	GND	5
20	SA16(H)	1
21	SA17(H)	1
22	SA18(H)	1
23	SA19(H)	1
24	GND	5
25	SA20(H)	1
26	SA21(H)	1
27	SA22(H)	1
28	SA23(H)	1
29	GND	5

Table 10-8 (cont)

Pin	Signal Name	Schematic
30	(Not Used)	a
31	(Not Used)	a
32	BA BG(L)	4
33	(Not Used)	6
34	GND	5
35	(Not Used)	7
36	(Not Used)	4
37	BA HALT(L)	6
38	BB R(H)/W(L)	7
39	GND	5
40	BA BERR(L)	4
41	BA IPL2(H)	6
42	BA IPL1(H)	6
43	BA IPL0(H)	6
44	GND	5
45	VPA(L)	6
46	BYTE(H)/WORD(L)	4
47	BA FC0(H)	7
48	BA FC1(H)	7
49	BA FC2(H)	7
50	GND	5

[a] **Not shown in schematic section.**

Table 10-9
Top Plane Connector P7

Pin	Signal Name	Schematic
1	GND	5
2	SA0(H)	8
3	SA1(H)	8
4	SA2(H)	8
5	SA3(H)	8
6	GND	5
7	SA4(H)	8
8	SA5(H)	8
9	SA6(H)	8
10	SA7(H)	8
11	GND	5
12	SA8(H)	8
13	SA9(H)	8
14	SA10(H)	8

Table 10-9 (cont)

Pin	Signal Name	Schematic
15	SA11(H)	2
16	GND	5
17	SD0(H)	8
18	SD1(H)	8
19	SD2(H)	8
20	SD3(H)	8
21	GND	5
22	SD4(H)	8
23	SD5(H)	8
24	SD6(H)	8
25	SD7(H)	8
26	GND	5
27	SD8(H)	8
28	SD9(H)	8
29	SD10(H)	8
30	SD11(H)	8
31	GND	5
32	SD12(H)	8
33	SD13(H)	8
34	SD14(H)	8
35	SD15(H)	8
36	GND	5
37	(Not Used)	a
38	(Not Used)	a
39	(Not Used)	a
40	(Not Used)	a
41	(Not Used)	a
42	(Not Used)	a
43	(Not Used)	a
44	(Not Used)	a
45	GND	5
46	(Not Used)	a
47	(Not Used)	a
48	(Not Used)	a
49	(Not Used)	a
50	GND	5

[a] **Not shown in schematic section.**

68000 Emulator Processor Interconnections

The 68000 Emulator Processor's interconnections consist of 13 cables that interconnect various parts of the Emulator Processor. Table 10-10 lists these connectors and their functions in the order in which they appear in this section. Tables 10-11 through 10-23 summarize the pins associated with each connector listed in Table 10-10.

Table 10-10
68000 Emulator Processor Connectors

Connectors	Description
P12 P13	Connects EMU 1 with EMU 2
J2 and P2	Connects EMU 1 and the Cable Termination board
P100 and P110 P200 and P210 P300 and P310	Connects the Cable Termination board with the Buffer board [a]
P10 and J11	Connects the Buffer board[a] with the Control board [a]
P8A and P9A P8B and P9B P8C and P9C P8D and P9D	Connects the Power Supply board[a] with the Buffer board[a]
P4 P5	Connects the Buffer board[a] with the 64-Pin Plug

[a] **Board is located in the Interface Assembly.**

Table 10-11
P12 Interconnect

Pin	Signal Name	Schematic	
		EMU 1	EMU 2
1	MODE2(H)	4	13
2	GND	5	12
3	MODE0(H)	3	13
4	MODE1(H)	3	13
5	TRACE(L)	[a]	11
6	GND	5	12
7	FFC1(H)	4	13
8	FFC0(H)	4	13
9	FFC2(H)	4	13
10	GND	5	12
11	BA BG(L)	4	11
12	DLYD ACTIVE(H)	6	11
13	BGACK(L)	4	11
14	GND	5	12
15	BRDHALT(L)	6	11
16	RESET(L)	6	11
17	BKCOND(H)	6	11
18	GND	5	12
19	BC AS(L)	5	11
20	BB CPUCLK(L)	4	13
21	UMAP EN(H)	4	14
22	UMAP(H)	3	14
23	2650 LCS(L)	8	10
24	2650 HCS(L)	8	10
25	2650 RAMAC(H)	3	10
26	GND	5	12
27	8E RD(H)	3	10
28	SHARED R(H)/W(L)	8	10
29	GND	5	12
30	8F WR(L)	9	10
31	BA CMD=0(H)	9	14
32	8F RD(L)	9	10
33	WRPROT(H)	4	14
34	RUNNING(H)	6	13
35	ISLVOPREQ(L)	4	13
36	GND	5	12
37	IBYTE(H)/WORD(L)	4	12
38	BB R(H)/W(L)	7	11
39	GND	5	12
40	ACTIVE O.C.(H)	4	13
41	BA SLVPSE(L)	[a]	11
42	8MHZ	5	11
43	BA SYS R(H)/W(L)	3	10
44	SVC-M(H)/IO(L)	4	13
45	SYS R(L)/W(H)	3	10
46	GND	5	12
47	BA HALT(L)	6	11
48	BKSTOP(L)	9	11
49	GND	5	12
50	(Not Used)	[b]	[b]

Table 10-12
P13 Interconnect

Pin	Signal Name	Schematic	
		EMU 1	EMU 2
1	BC FC0(H)	3	14
2	GND	5	13
3	BC FC2(H)	3	14
4	BC FC1(H)	3	14
5	SA0(H)	2	12
6	GND	5	13
7	SA2(H)	2	12
8	SA1(H)	2	12
9	SA3(H)	2	12
10	GND	5	13
11	SA5(H)	2	12
12	SA4(H)	2	12
13	SA6(H)	2	12
14	GND	5	13
15	SA8(H)	2	12
16	SA7(H)	2	12
17	SA9(H)	2	12
18	GND	5	13
19	SA11(H)	2	12
20	SA10(H)	2	12
21	SA12(H)	2	12
22	GND	5	13
23	SA14(H)	2	12
24	SA13(H)	2	12
25	SA15(H)	2	12
26	GND	5	13
27	SA17(H)	2	12
28	SA16(H)	2	12
29	GND	5	13
30	SA18(H)	2	12
31	SA20(H)	2	12
32	SA19(H)	2	12
33	SA22(H)	2	12
34	SA21(H)	2	12
35	SA23(H)	2	12
36	GND	5	13
37	SD1(H)	8	11
38	SD0(H)	8	11
39	GND	5	13
40	SD2(H)	8	11
41	SD4(H)	8	11
42	SD3(H)	8	11
43	SD6(H)	8	11
44	SD5(H)	8	11
45	SD7(H)	8	11
46	GND	5	13
47	CLKFAIL(H)	6	13
48	SMAP(H)	6	14
49	GND	5	13
50	HALTED(H)	6	13

[a] **Not connected.**

[b] **Not shown in schematic section.**

Table 10-13
J2 And P2 Interconnect

Pin	Signal Name	Schematic		Pin	Signal Name	Schematic	
		J2	P2			J2	P2
1	GND	5	15	2	GND	5	15
3	IA4(H)	2	15	4	IA5(H)	2	15
5	IA3(H)	2	15	6	IA6(H)	2	15
7	IA2(H)	2	15	8	IA7(H)	2	15
9	IA1(H)	2	15	10	IA8(H)	2	15
11	IA10(H)	2	15	12	IA9(H)	2	15
13	IA12(H)	2	15	14	IA11(H)	2	15
15	IA14(H)	2	15	16	IA13(H)	2	15
17	IA16(H)	2	15	18	IA15(H)	2	15
19	IA18(H)	2	15	20	IA17(H)	2	15
21	+5.2V	5	15	22	+5.2V	2	15
23	IA20(H)	2	15	24	IA19(H)	2	15
25	IA22(H)	2	15	26	IA21(H)	2	15
27	GND	5	15	28	IA23(H)	2	15
29	BA IPL0(H)	6	15	30	GND	5	15
31	BA IPL1(H)	6	15	32	UGET(H)	7	15
33	BA IPL2(H)	6	15	34	UPUT(H)	7	15
35	BA BERR(L)	4	15	36	RUNNING(H)	6	15
37	VPA(L)	6	15	38	SMAP(H)	6	15
39	-12V	5	15	40	-12V	5	15
41	BB CPUCLK(H)	3	15	42	MODE0CLK(H)	5	15
43	+5.2V	5	15	44	BA HALT(L)	6	15
45	ID12(H)	2	15	46	ID15(H)	2	15
47	ID11(H)	2	15	48	ID14(H)	2	15
49	ID10(H)	2	15	50	ID13(H)	2	15
51	ID9(H)	2	15	52	ID8(H)	2	15
53	ID7(H)	2	15	54	ID6(H)	2	15
55	ID5(H)	2	15	56	ID0(H)	2	15
57	ID1(H)	2	15	58	FFC0(H)	4	15
59	ID2(H)	2	15	60	FFC1(H)	4	15
61	ID3(H)	2	15	62	FFC2(H)	4	15
63	ID4(H)	2	15	64	+12V	5	15
65	+12V	5	15	66	BB CLK+25(H)	4	15

Table 10-13 (cont)

Pin	Signal Name	Schematic		Pin	Signal Name	Schematic	
		J2	P2			J2	P2
67	ASYNCBK(L)	9	15	68	GND	5	15
69	BRDDTACK(L)	6	[a]	70	HOLD(L)	6	15
71	BA BG(L)	4	15	72	DTACKEN(H)	6	[a]
73	BGACK(L)	4	15	74	DLYD ACTIVE(H)	6	15
75	(Not Used)	[b]	[b]	76	INTMACHEN(H)	5	15
77	BRDHALT(L)	6	15	78	BA R(H)/W(L)	7	15
79	RESET(L)	6	15	80	BA LDS(L)	4	15
81	+12V	5	15	82	+12V	5	15
83	E(H)	[a]	15	84	BA UDS(L)	4	15
85	BA PODBKINTA(L)	7	15	86	BA AS(L)	5	15
87	STUSREGPUL(L)	7	15	88	BA FC0(H)	3	15
89	MODE0(H)	3	15	90	BA FC1(H)	3	15
91	MODE2(H)	4	15	92	BA FC2(H)	3	15
93	ACTIVE O.C.(H)	4	15	94	VMA(L)	[a]	15
95	DISABLE WR(H)	4	15	96	ID TO(L)/FROM(H)	3	15
97	BKCOND(H)	6	15	98	BA UG/UP(H)+RUNNING(H)	3	15
99	GND	5	15	100	GND	5	15

[a] **Not connected.**

[b] **Not shown in schematics section.**

Table 10-14
P100 And P110 Interconnect

Pin	Signal Name	Schematic	
		P100	P110
1	ASYNCBK(L)	15	19
2	+12V	15	19
3	+12V	15	19
4	+12V	15	19
5	+12V	15	19
6	BA CLK+25(H)	15	19
7	GND	15	17
8	+12V	15	19
9	ID4(H)	15	18
10	FFC2(H)	15	16
11	ID3(H)	15	18
12	FFC1(H)	15	16
13	ID2(H)	15	18
14	FFC0(H)	15	16
15	GND	15	17
16	ID0(H)	15	18
17	ID1(H)	15	18
18	ID6(H)	15	18
19	ID5(H)	15	18
20	ID8(H)	15	18
21	ID7(H)	15	18
22	ID13(H)	15	18
23	ID9(H)	15	18
24	ID14(H)	15	18
25	ID10(H)	15	18
26	GND	15	17
27	ID11(H)	15	18
28	ID15(H)	15	18
29	ID12(H)	15	18
30	-12V	15	17
31	MODE0CLK(H)	15	17
32	-12V	15	17
33	+5.2V	[a]	17
34	GND	15	17
35	BA CPUCLK(H)	15	17
36	BA SMAP(H)	15	17
37	VPA(L)	15	16
38	BA RUNNING(H)	15	17
39	BA BERR(L)	15	17
40	GND	15	17

[a] Not connected.

Table 10-15
P200 And P210 Interconnect

Pin	Signal Name	Schematic	
		P200	P210
1	GND	15	16
2	BA HALT(L)	15	[a]
3	+5.2V	15	16
4	+5.2V	15	16
5	+5.2V	15	16
6	UPUT(H)	15	17
7	GND	15	16
8	UGET(H)	15	17
9	IPL2(H)	15	19
10	+5.2V	15	16
11	IPL1(H)	15	19
12	IA23(H)	15	18
13	IPL0(H)	15	19
14	IA21(H)	15	18
15	GND	15	16
16	IA19(H)	15	18
17	+5.2V	15	16
18	IA17(H)	15	18
19	IA22(H)	15	18
20	IA15(H)	15	18
21	IA20(H)	15	18
22	IA13(H)	15	18
23	IA18(H)	15	18
24	IA11(H)	15	18
25	IA16(H)	15	18
26	GND	15	16
27	IA14(H)	15	18
28	IA9(H)	15	18
29	IA12(H)	15	18
30	IA8(H)	15	18
31	IA10(H)	15	18
32	IA7(H)	15	18
33	IA1(H)	15	18
34	GND	15	16
35	IA2(H)	15	18
36	IA6(H)	15	18
37	IA3(H)	15	18
38	IA5(H)	15	18
39	IA4(H)	15	18
40	GND	15	16

[a] Not connected.

Table 10-16
P300 And P310 Interconnect

Pin	Signal Name	Schematic	
		P300	P310
1	GND	15	16
2	+5.2V	[a]	16
3	+5.2V	15	16
4	+5.2V	15	16
5	+5.2V	15	16
6	+5.2V	15	16
7	GND	15	16
8	ACTIVE O.C.(H)	15	19
9	BA MODE2(H)	15	17
10	BA UG/UP(H)+RUNNING(H)	15	17
11	BA BKCOND(H)	15	19
12	ID TO(L)/FROM(H)	15	18
13	BA DISABLE WR(H)	15	16
14	VMA(L)	15	[a]
15	GND	15	16
16	BA FC2(H)	15	16
17	BA MODE0(H)	15	16
18	BA FC1(H)	15	16
19	BA STUSREGPUL(L)	15	19
20	BA FC0(H)	15	16
21	BA PODBKINTA(L)	15	19
22	BA AS(L)	15	16
23	E(H)	15	[a]
24	BA UDS(L)	15	16
25	+12V	15	19
26	GND	15	16
27	+12V	15	19
28	BA LDS(L)	15	16
29	+12V	15	19
30	BA R(H)/W(L)	15	16
31	+12V	15	19
32	BA INTMACHEN(H)	15	19
33	RESET(L)	15	19
34	GND	15	16
35	BRDHALT(L)	15	19
36	BA DLYD ACTIVE(H)	15	19
37	BGACK(L)	15	17
38	BA BG(L)	15	16
39	BA HOLD(L)	15	19
40	GND	15	16

[a] **Not connected.**

Table 10-17
P10 And J11 Interconnect

Pin	Signal Name	Schematic	
		EMU 1	EMU 2
1	GND	19	22
2	GND	19	22
3	IPL2(L)	19	21
4	UIPL2(L)	19	21
5	IPL1(L)	19	21
6	UIPL1(L)	19	21
7	(Not Used)	[a]	[a]
8	+4.9V	19	22
9	IPL0(L)	19	21
10	UIPL0(L)	19	21
11	HALT(L)	19	22
12	RESET(L)	19	22
13	BA MODE0(L)	16	22
14	QRESET(H)	19	22
15	GND	19	22
16	AS(H)	16	22
17	A/DTRIST(L)	16	22
18	BA STUSREGPUL(L)	19	21
19	EN WINDOW(L)	17	23
20	+5.2V	19	22
21	UHALT(L)	19	22
22	+4.9V	19	22
23	PD10(H)	18	21
24	+4.9V	19	22
25	PD9(H)	18	21
26	GND	19	22
27	PD8(H)	18	21
28	ST0/BKINTEN(H)	16	23
29	(Not Used)	[a]	[a]
30	(Not Used)	[a]	[a]
31	URESET(L)	19	22
32	QINTA7(H)	16	23
33	(Not Used)	[a]	[a]
34	+4.92V	19	22
35	QINTA(H)	16	23
36	ASYNCBK(L)	19	23
37	PODBKINTA(L)	19	23
38	BA BKCOND(H)	19	23
39	CTRIST(H)	16	22
40	BG(H)	16	22

Table 10-17 (cont)

Pin	Signal Name	Schematic P10	Schematic J11
41	BA INTMACHEN(H)	19	23
42	BB AS(L)	16	22
43	BR(L)	17	22
44	BGACK(L)	17	22
45	CPUCLK(L)	17	22
46	QHALT(H)	19	22
47	BRDHALT(L)	19	22
48	BA DLYD ACTIVE(L)	19	22
49	GND	19	22
50	GND	19	22

[a] Not shown in schematics section.

Table 10-18
P8A And P9A Interconnect

Pin	Signal Name	Schematic P8A	Schematic P9A
1	-12V	17	24
2	ACTIVE O.C.(H)	19	24
3	+5.2V PROBE	17	24
4	UVDD(H)	19	24
5	GND	17	24
6	GND	17	24

Table 10-19
P8B And P9B Interconnect

Pin	Signal Name	Schematic P8B	Schematic P9B
1	+4.9V	17	24
2	BGACK(H)	17	24
3	QRESET(L)	19	24
4	QHALT(H)	19	24
5	DTACK T.O.(H)	16	24
6	QBG(H)	16	24

Table 10-20
P8C And P9C Interconnect

Pin	Signal Name	Schematic P8C	Schematic P9C
1	+12V	19	24
2	+12V	19	24
3	GND	19	24
4	GND	19	24
5	+12V	19	24
6	+12V	19	24

Table 10-21
P8D And P9D Interconnect

Pin	Signal Name	Schematic P8D	Schematic P9D
1	+4.9V	17	24
2	+4.9V	17	24
3	+4.9V	17	24
4	+4.9V	17	24
5	+4.9V	17	24
6	+4.9V	17	24

Table 10-22
P4 Interconnect

Pin	Signal	Schematic
1	(Not Used)	[a]
2	(Not Used)	[a]
3	UD4(H)	18
4	UD3(H)	18
5	UD2(H)	18
6	UD1(H)	18
7	GND	16
8	UD0(H)	18
9	UAS(L)	16
10	UUDS(L)	16
11	ULDS(L)	16
12	UR(H)/W(L)	16
13	UDTACK(H)	17
14	BG(H)	14
15	GND	16
16	UBGACK(L)	17
17	UBR(L)	17
18	UVDD(H)	19
19	UCLK(H)	17
20	UHALT(L)	19
21	GND	16
22	URESET(L)	19
23	UVMA(L)	16
24	UE(L)	19
25	UVPA(L)	16
26	GND	16
27	UBERR(L)	17
28	UIPL2(L)	19
29	UIPL1(L)	19
30	UIPL0(L)	19
31	UFC2(H)	16
32	UFC1(H)	16
33	UFC0(H)	16
34	GND	16
35	UA1(H)	18
36	UA2(H)	18
37	UA3(H)	18
38	UA4(H)	18
39	+5.2V PROBE	19
40	+5.2V PROBE	19

[a] **Not shown in schematic section.**

Table 10-23
P5 Interconnect

Pin	Signal	Schematic
1	(Not Used)	[a]
2	(Not Used)	[a]
3	UD5(H)	18
4	UD6(H)	18
5	UD7(H)	18
6	UD8(H)	18
7	GND	19
8	UD9(H)	18
9	UD10(H)	18
10	UD11(H)	18
11	UD12(H)	18
12	UD13(H)	18
13	UD14(H)	18
14	UD15(H)	18
15	GND	19
16	GND	19
17	UA23(H)	18
18	UA22(H)	18
19	UA21(H)	18
20	UVDD(H)	19
21	UA20(H)	18
22	UA19(H)	18
23	UA18(H)	18
24	UA17(H)	18
25	UA16(H)	18
26	GND	19
27	UA15(H)	18
28	UA14(H)	18
29	UA13(H)	18
30	UA12(H)	18
31	UA11(H)	18
32	UA10(H)	18
33	UA9(H)	18
34	GND	19
35	UA8(H)	18
36	UA7(H)	18
37	UA6(H)	18
38	UA5(H)	18
39	+5.2V PROBE	[b]
40	+5.2V PROBE	[b]

[a] **Not shown in schematic section.**

[b] **Not connected.**

I/O PORT CONFIGURATIONS

There are five 68000 Emulator Processor I/O Ports: Status, AUX Status, Control, AUX Control, and Command. (See Figs. 10-1 through 10-5, respectively.) Each port consists of one byte of binary information. For more information on the I/O Ports, refer back to Section 4 of this manual.

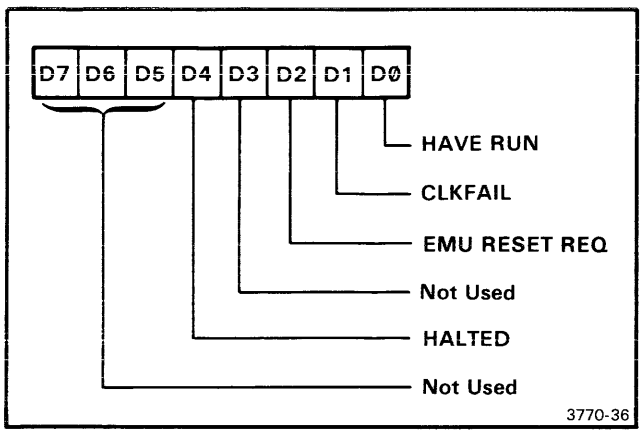


Fig. 10-1. EMU Status Port.

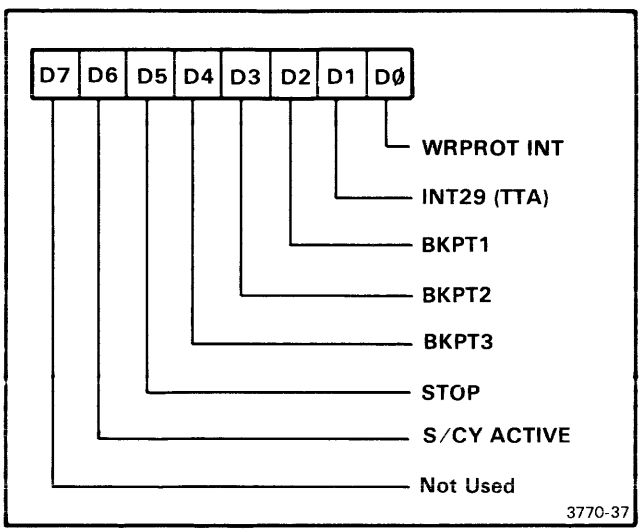


Fig. 10-2. AUX Status Port.

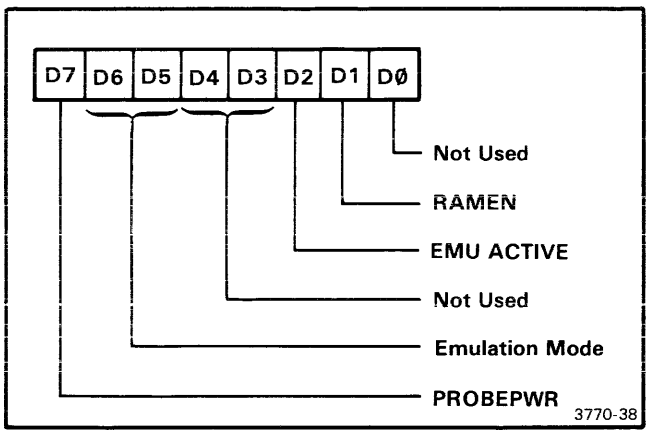


Fig. 10-3. EMU Control Port.

For encoding of the Emulation Mode bits, refer to Table 10-24.

Table 10-24
Emulation Mode Encoding

D6	D5	Function
L	L	Mode 0
L	H	Mode 1
H	H	Mode 2

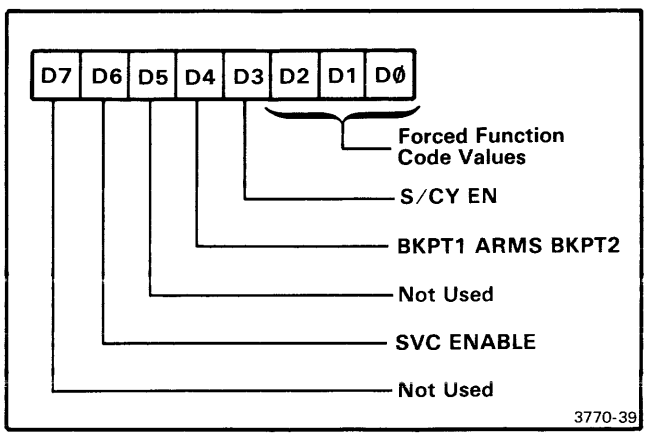


Fig. 10-4. AUX Control Port.

For encoding of the Forced Function Code bits, refer to Table 10-25.

Table 10-25
Forced Function Code Encoding

Forced Function Codes			
FFC2	**FFC1**	**FFC0**	**Accessed**
L	L	L	Not Used
L	L	H	User Data
L	H	L	User Code
L	H	H	Not Used
H	L	L	Not Used
H	L	H	Supervisor Data
H	H	L	Supervisor Code
H	H	H	Interrupt

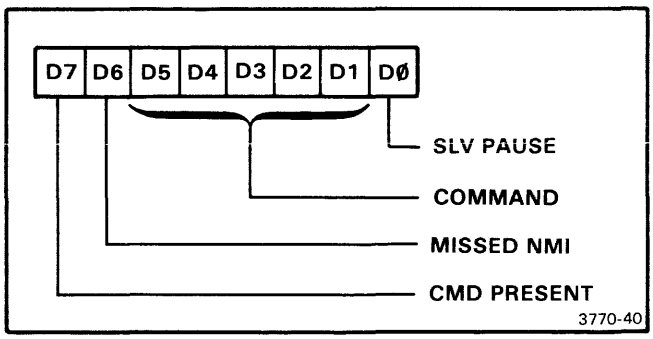


Fig. 10-5. Command Port.

For encoding of the Command bits, refer to Table 10-26.

Table 10-26
Command Encoding

D5	D4	D3	D2	D1	Command
L	L	L	L	L	Return to user program
L	L	L	L	H	Register Dump
L	L	L	H	L	Register Restore
L	L	L	H	H	UPUT
L	L	H	L	L	UGET
L	L	H	L	H	Readback check
L	L	H	H	L	Execute from Dump and Restore RAM
L	L	H	H	H	Reserved for future use
H	X	X	X	X	Reserved for future use[a]
X	H	X	X	X	Reserved for future use[a]

[a] **X = Don't care.**

RAM PARTITIONING

The 68000 Emulator Processor utilizes three different RAM circuits: Breakpoint, Shared Communication, and UMAP/Write Protect. Tables 10-27 and 10-28 show the 2650's access to these RAM circuits. For more information regarding the 68000 Emulator Processors' RAM circuits, refer to Section 4 of this manual.

Table 10-27
Emulator Processor RAM Partitioning

2650 Address Space Allocation	68000 Emulator Processor RAM
8000-82FF	Breakpoint RAM
8300-83DF	Not Used
83E0-83FF	Breakpoint RAM
8400-9FFF	Not Used[a]
A000-A7FF	Shared Communication RAM
A800-BFFF	Not Used[b]
C000-FFFF	UMAP/Write Protect RAM

[a] **Contains Breakpoint RAM images.**

[b] **Contains Shared Communication RAM images.**

Table 10-28
2650 RAM Access Bit Encoding

2650 Address Lines[a]									
A15	A14	A13	A12	A11	A10	A9	A8	A7–A0	Emulator Processor RAM Accessed
1	0	0	0	0	0	0	0	[b]	BKPT RAM (U3050)
1	0	0	0	0	0	0	1	[b]	BKPT RAM (U3070)
1	0	0	0	0	0	1	0	[b]	BKPT RAM (U3080)
1	0	0	0	0	0	1	1	[b]	BKPT RAM (U3090)
1	0	1	0	0	[b]				Shared Communication RAM
1	1	0	0	[b]					UMAP/Write Protect RAM (User Code)
1	1	0	1	[b]					UMAP/ Write Protect RAM (User Data)
1	1	1	0	[b]					UMAP/Write Protect RAM (Supervisor Code)
1	1	1	1	[b]					UMAP/Write Protect RAM (Supervisor Data)

[a] **A "1" indicates that the address line is asserted. A "0" indicates that the address line is deasserted.**

[b] **Binary address that is presented directly to the RAMs.**

MEMORY RESTRICTIONS

Because of the Emulator Processor's operating power levels, two memory restrictions must be observed. (1.) The 68000 Emulator Processor and the development system's PROM Programmer cannot be selected at the same time. (2.) A limited memory arrangement is available. The 68000 Emulator Processor can be operated within the configurations listed in Table 10-29.

Table 10-29
Memory Arrangement Restrictions

Configuration	Memory Arrangements
TTA and PROM Programmer Installed	(1) LAS + (1) MAC (1) LAS + (1) 32K (2) LAS (2) 32K
TTA Installed, No PROM Programmer	(2) LAS + (1) MAC (2) LAS + (1) 32K (1) LAS + (2) 32K (4) 32K

Memory Configurations

Table 10-30 shows the memory configurations you may use in your development system with the 68000 Emulator Processor. Also included in the table are the recommended jumper positions for each memory configuration.

NOTE

J1045 and J2045 are located on the Mobile Microprocessor board. Refer to Section 3 of this document for more specific information.

TIMING RELATIONSHIPS

Table 10-31 lists a comparison of timing relations between the MC68000L8 microprocessor and the 68000 Emulator Processor at the 64-Pin Plug. These timing relationships listed in Table 10-31 are illustrated by Figures 10-6 and 10-7.

NOTE

Table 10-31 applies only to the 8 MHz operation of both the 68000 microprocessor and the 68000 Emulator Processor.

Table 10-30
J1045 and J2045 Configurations[a]

Memory Configuration	Jumper Configuration[b]		Characteristic
	J1045	J2045	
32K Program Memory board	A1 to A	A1 to A	Normal (no delay)
64K or 128K Static Program Memory board	A1 to A	A1 to A	Normal (no delay)
64K or 128K Static Program Memory board and Memory Allocation Control	A1 to A	A1 to A	Normal (no delay)
32K Program Memory board and Memory Allocation Control	A5 to B	A1 to A	Option (one wait state delay at $\leq$ 6.4MHz)[c]

[a] **Jumper configurations listed are for $\geq$8 MHz operation.**

[b] **Jumper configurations not listed for J1045 and J2045 are for future use.**

[c] **One wait state is equivalent to one extra clock cycle per memory cycle.**

Table 10-31
Timing Comparison

Number	Characteristic	Symbol	Processor		Emulator		Unit
			Min	Max	Min	Max	
1	Clock Period	'cyc	125	500	125	500	ns
2	Clock Width Low	'CL	55	250	55	250	ns
3	Clock Width High	'CH	55	250	55	250	ns
4	Clock Fall Time	'Cf	—	10	—	10	ns
5	Clock Rise Time	'Cr	—	10	—	10	ns
6	Clock Low to Address	'CLAV	—	70	—	92	ns
6A	Clock High to FC(H) Valid	'CHFCV	—	70	—	92	ns
7A	Clock High to Address High Impedance (Max.)	'CHAZx	—	80	—	114	ns
7B	Clock High to Data High Impedance (Max.)	'CHDZx	—	80	—	130	ns
8	Clock High to Address/FC(H) Invalid (Min.)	'CHAZn	0	—	14	—	ns
9[1]	Clock High to AS(L), DS(L) Low (Max.)	'CHSLx	—	60	—	86	ns
10	Clock High to AS(L), DS(L) Low (Min.)	'CHSLn	0	—	14	—	ns
11[2]	Address to AS(L), DS(L) (Read) Low/AS(L) Write	'AVSL	30	—	24	—	ns
11A[2]	FC(H) Valid to AS(L), DS(L) (Read) Low/AS(L) Write	'FCVSL	60	—	44	—	ns
12[1]	Clock Low to AS(L), DS(L) High	'CLSH	—	70	—	96	ns
13[2]	AS(L), DS(L) High to Address/FC(H) Invalid	'SHAZ	30	—	20	—	ns
14[2,5]	AS(L), DS(L) Width Low (Read)/AS(L) Write	'SL	240	—	240	—	ns
14A[2]	DS(L) Width Low (Write)	—	115	—	115	—	ns
15[2]	AS(L), DS(L) Width High	'SH	150	—	150	—	ns
16	Clock High to AS(L), DS(L) High Impedance	'CHSZ	—	80	—	93	ns
17[2]	AS(L), DS(L) High to R(H)/W(L) High	'SHRH	40	—	40	—	ns
18[1]	Clock High to R(H)/W(L) High (Max.)	'CHRHx	—	70	—	96	ns
19	Clock High to R(H)/W(L) High (Min.)	'CHRHn	0	—	14	—	ns
20[1]	Clock High to R(H)/W(L) Low	'CHRL	—	70	—	96	ns
21[2]	Address Valid to R(H)/W(L) Low	'AVRL	20	—	14	—	ns
21A[2]	FC(H) Valid to R(H)/W(L) Low	'FCVRL	60	—	54	—	ns
22[2]	R(H)/W(L) Low to DS(L) Low (Write)	'RLSL	80	—	80	—	ns
23	Clock Low to Data Out(H) Valid	'CLDO	—	70	—	95	ns
25[2]	DS(L) High to Data Out(H) Invalid	'SHDO	30	—	20	—	ns
26[2]	Data Out(H) Valid to DS(L) Low (Write)	'DOSL	30	—	20	—	ns
27[6]	Data In to Clock Low (Setup Time)	'DICL	15	—	17	—	ns
28[2]	AS(L), DS(L) High to DTACK(L) High	'SHDAH	0	120	0	94	ns
29	DS(L) High to Data Invalid (Hold Time)	'SHDI	0	—	0	—	ns
30	AS(L), DS(L) High to BERR(L) High	'SHBEH	0	—	0	—	ns
31[2,6]	DTACK(L) Low to Data In (Setup Time)	'DALDI	—	90	—	88	ns
32	HALT(L) and RESET(L) Input Transition Time	'RHrf	0	200	0	200	ns
33	Clock High to BG(L) Low	'CHGL	—	70	—	93	ns
34	Clock High to BG(H) High	'CHGH	—	70	—	93	ns
35[7]	BR(L) Low to BG(L) Low	'BRLGL	1.5	3	1.5	3	Clk Per
36[7]	BR(L) High to BG(L) High	'BRHGH	1.5	3	1.5	3	Clk Per
37	BGACK(L) Low to BG(L) High	'GALGH	1.5	3	1.5	3	Clk Per
38	BG(L) Low to Bus High Impedance (With AS(L) High)	'GLZ	—	80	—	148	ns
39	BG(L) Width High	'GH	1.5	—	1.5	—	Clk Per
46	BGACK(L) Width	'BGL	1.5	—	1.5	—	Clk Per
47[6,8]	Asynchronous Input Setup Time	'ASI	20	—	20	—	ns
48	BERR(L) Low to DTACK(L) Low[3]	'BELDAL	50	—	50	—	ns
53	Data Hold from Clock High	'CHDO	0	—	0	—	ns
55	R(H)/W(L) to Data Bus Impedance Change	'RLDO	30	—	20	—	ns
56	HALT(H)/RESET(L) Pulse Width[4]	HRPW	10		10		Clk Per

[1] For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.

[2] Actual value depends on clock period.

[3] If #47 is satisfied for both DTACK(L) and BERR(L), #48 may be 0 ns.

[4] After Vcc has been applied for 100 ms.

[5] For T6E, BF4, and R9M mask sets #14 and #14A are one clock period less than the given number.

[6] If the asynchronous setup time (#47) requirements are satisfied, the DTACK(L) low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following cycle.

[7] For the Probe-tip add 20 nanoseconds to the clock periods listed.

[8] VPA = 50 nanoseconds for the Probe-tip.

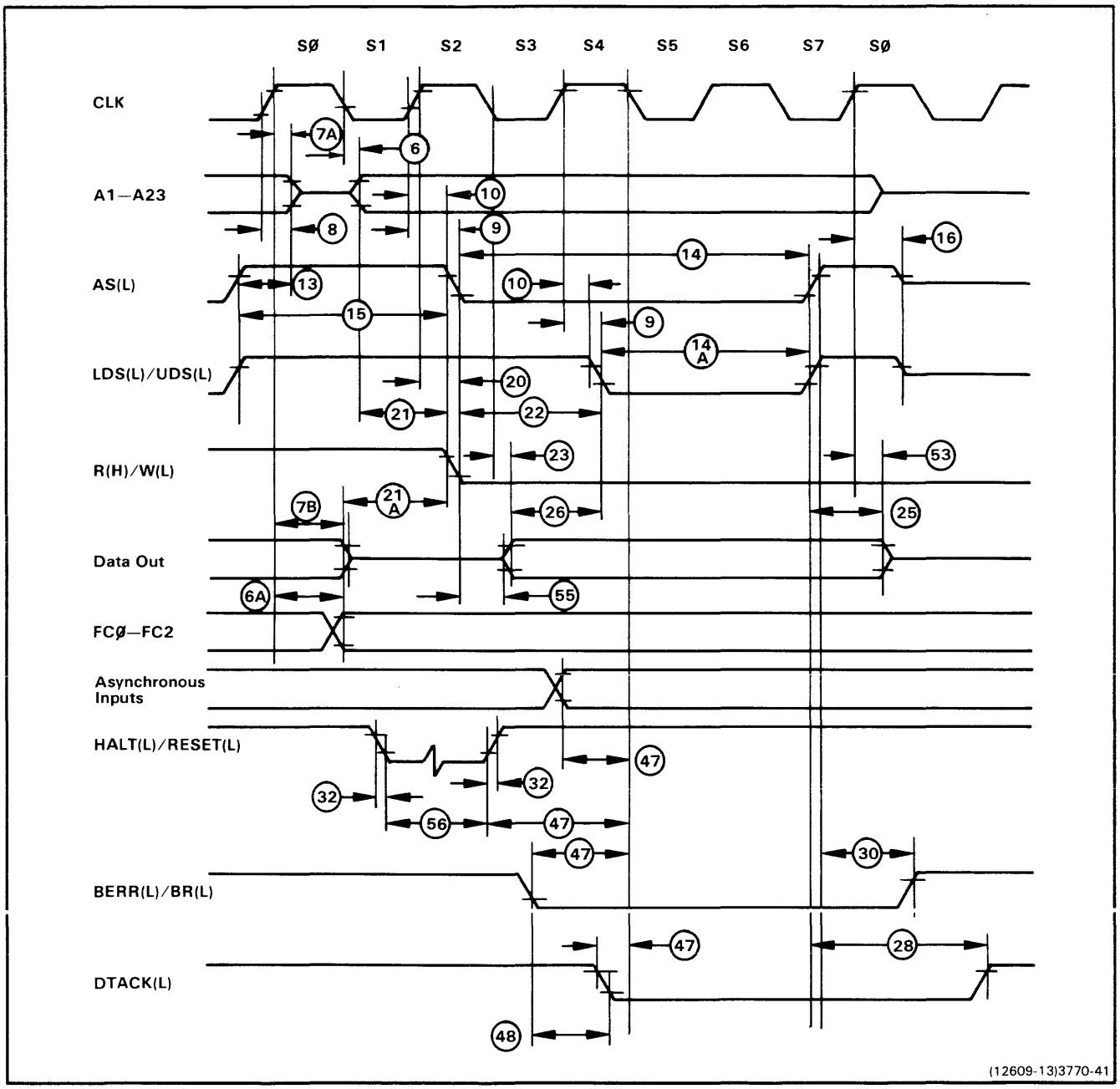


Fig. 10-6. Control signal timing during write cycle.

All numbers circled are in reference to Table 10-31.

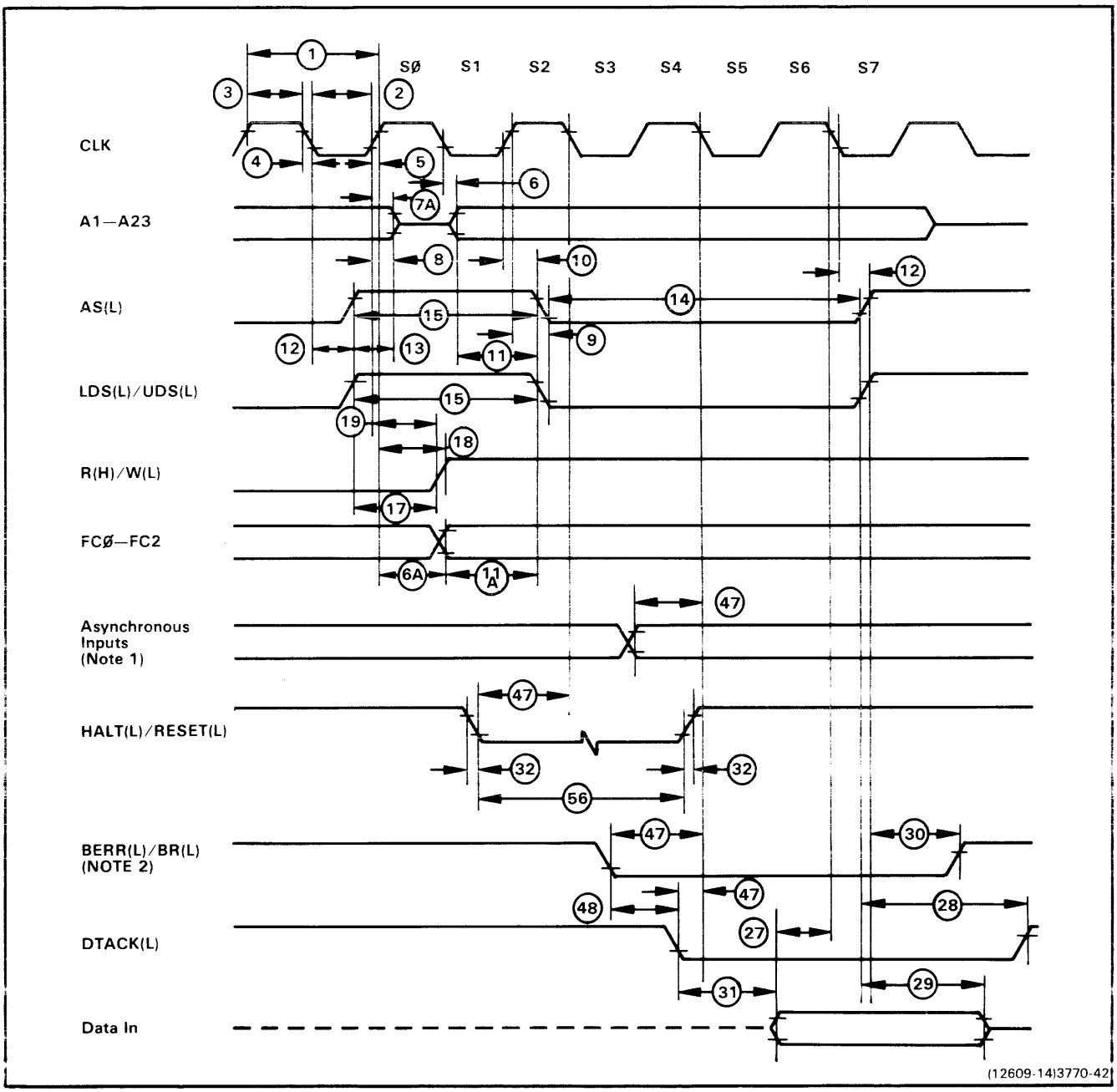


Fig. 10-7. Control signal timing during read cycle.

All numbers circled are in reference to Table 10-31.

SECTION 11

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

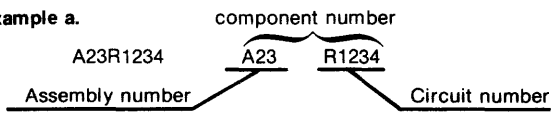
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

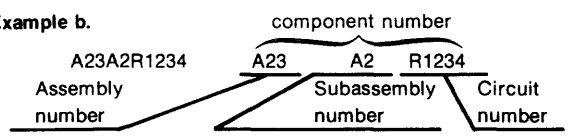
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01807	PETERSEN RADIO COMPANY, INC.	2800 WEST BROADWAY	COUNCIL BLUFFS, IN 51501
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32440	ENGINEERED COMPONENTS CO.	3580 SACRAMENTO DR.	SAN LUIS OBISPO, CA 93406
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
58361	GENERAL INSTRUMENT CORP. OPTO ELECTRONICS DIV.	3400 HILLVIEW AVE	PALO ALTO, CA 94304
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC , HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
90095	TECHNITROL INC.	1952 ALLEGHENY AVE.	PHILADELPHIA, PA 19134
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-7301-00	B010100	B010191	CKT BOARD ASSY:EMULATOR I	80009	670-7301-00
	----- -----			(8300E26-8540/8550 OPTION 2P ONLY)		
A10	670-7301-01	B010192		CKT BOARD ASSY:EMULATOR I	80009	670-7301-01
	----- -----			(8300E26-8540/8550 OPTION 2P ONLY)		
A15	670-7302-00			CKT BOARD ASSY:EMULATOR II	80009	670-7302-00
	----- -----			(8300E26-8540/8550 OPTION 2P ONLY)		
A20	670-7304-00			CKT BOARD ASSY:CABLE TERMINATION	80009	670-7304-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A30	670-7303-00	B010100	B010182	CKT BOARD ASSY:BUFFER	80009	670-7303-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A30	670-7303-01	B010182		CKT BOARD ASSY:BUFFER	80009	670-7303-01
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A35	670-7305-00			CKT BOARD ASSY:68000 MOBILE	80009	670-7305-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A40	670-7300-00	B010100	B010191	CKT BOARD ASSY:68000 CONTROL	80009	670-7300-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A40	670-7300-01	B010192		CKT BOARD ASSY:68000 CONTROL	80009	670-7300-01
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A50	670-7235-00			CKT BOARD ASSY:POD POWER SUPPLY	80009	670-7235-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A60	----- -----			PROBE ASSY:68000		
	----- -----			(REPLACEABLE AS 175-4575-00)		
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A10	670-7301-00	B010100	B010191	CKT BOARD ASSY:EMULATOR I	80009	670-7301-00
	----- -----			(8300E26-8540/8550 OPTION 2P ONLY)		
A10	670-7301-01	B010192		CKT BOARD ASSY:EMULATOR I	80009	670-7301-01
	----- -----			(8300E26-8540/8550 OPTION 2P ONLY)		
A10C2012	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2042	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2052	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2062	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2162	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2172	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2182	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2218	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C2219	283-0115-00			CAP.,FXD,CER DI:47PF,5%,200V	59660	805-519-C0G0470J
A10C2221	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3042	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3052	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3062	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C3223	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4012	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4042	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10C4052	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4062	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4102	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4112	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4122	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4142	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4152	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4162	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4172	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4182	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4192	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4202	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C4222	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5012	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5042	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5052	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5062	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5102	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5112	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5122	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5192	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5202	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5212	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C5222	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6012	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6042	283-0421-00			CAP..FXD.CER DI:0.1UF.+80-20%.50V	04222	DG015E104Z
A10C6044	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	55680	16U-47V-T
A10C6052	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6062	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6072	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6102	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6112	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6122	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6132	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6142	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6159	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6162	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6172	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6192	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6202	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6212	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10C6222	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A10DL4030	119-1407-00			DELAY LINE,ELEC:100NS,TAPPED,14 PIN	32440	TTLDM100
A10R1012	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R2014	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R2161	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10R2181	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R2212	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A10R2214	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R2216	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A10R2217	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R6024	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10RP2111	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A10RP2121	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A10RP3111	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A10RP6151	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A10RP6182	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A10U1220	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A10U2020	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U2030	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U2040	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3STATE OUT	01295	SN74S241 JP3
A10U2050	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U2060	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U2080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A10U2090	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A10U2140	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A10U2160	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05
A10U2170	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A10U2180	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A10U2190	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U2210	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A10U2220	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A10U3010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A10U3020	156-0418-01			MICROCIRCUIT,DI:8 INPUT NAND GATE,SCRN	01295	SN74S30
A10U3030	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A10U3040	156-0320-03			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S11NP3
A10U3050	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A10U3060	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A10U3080	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A10U3090	156-0966-01			MICROCIRCUIT,DI:DUAL 5 INP NOR GATES	80009	156-0966-01
A10U4010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A10U4020	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A10U4040	156-0707-03			MICROCIRCUIT,DI:QUAD 2 INP EXCL OR GATE	07263	74S86
A10U4050	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A10U4060	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A10U4080	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A10U4090	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A10U4100	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A10U4110	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A10U4120	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A10U4140	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U4150	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A10U4160	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A10U4170	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U4180	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U4190	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U4200	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A10U4220	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A10U5010	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10
A10U5030	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A10U5040	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A10U5050	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A10U5060	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10U5080	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A10U5090	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A10U5100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A10U5110	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A10U5120	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A10U5140	160-1308-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	160-1308-00
A10U5160	160-1309-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	160-1309-00
A10U5170	160-1310-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	160-1310-00
A10U5190	156-1614-00			MICROCIRCUIT,DI:SRAM,1024 X 4,W/3 STATE	34649	D2114AL-3
A10U5200	156-1614-00			MICROCIRCUIT,DI:SRAM,1024 X 4,W/3 STATE	34649	D2114AL-3
A10U5210	156-1614-00			MICROCIRCUIT,DI:SRAM,1024 X 4,W/3 STATE	34649	D2114AL-3
A10U5220	156-1614-00			MICROCIRCUIT,DI:SRAM,1024 X 4,W/3 STATE	34649	D2114AL-3
A10U6010	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A10U6020	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POSITIVE EDGE	80009	156-0331-03
A10U6030	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A10U6040	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A10U6050	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U6060	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A10U6070	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U6080	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A10U6090	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U6100	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A10U6110	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U6120	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A10U6130	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A10U6160	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-RLATCH,SCRN	01295	SN74LS279NP3
A10U6170	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A10U6190	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A10U6200	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A10U6210	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A10U6220	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A10Y3228	158-0115-00			XTAL UNIT,QTZ:16MHZ,0.01%,SERIES	01807	7-13P

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15	670-7302-00			CKT BOARD ASSY:EMULATOR II	80009	670-7302-00
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A15C1071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C1072	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A15C1081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C1101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C1111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C1121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C1141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2102	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C2161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C3161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4142	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C4161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5022	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A15C5041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5072	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5112	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15C5161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A15R1091	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A15R1092	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A15R1093	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A15R1122	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R1131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R2041	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R2122	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R2123	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15R2151	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R2152	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R3042	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R3151	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R4042	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R4091	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R4162	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R5071	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R5091	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R5111	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R5131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R5151	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15U1070	156-0522-02			MICROCIRCUIT,DI:QUAD 2-INP MUX W/3 STATE	07263	74S257
A15U1080	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A15U1090	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A15U1110	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A15U1120	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A15U1130	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POSITIVE EDGE	80009	156-0331-03
A15U1140	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A15U2100	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A15U2010	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A15U2020	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A15U2030	156-0522-02			MICROCIRCUIT,DI:QUAD 2-INP MUX W/3 STATE	07263	74S257
A15U2040	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A15U2050	156-0418-01			MICROCIRCUIT,DI:8 INPUT NAND GATE,SCRN	01295	SN74S30
A15U2060	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A15U2070	156-0522-02			MICROCIRCUIT,DI:QUAD 2-INP MUX W/3 STATE	07263	74S257
A15U2080	156-0522-02			MICROCIRCUIT,DI:QUAD 2-INP MUX W/3 STATE	07263	74S257
A15U2090	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A15U2110	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A15U2120	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A15U2130	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A15U2140	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A15U2150	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A15U3100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A15U3010	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U3020	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U3030	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U3040	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U3050	156-1293-00	B010100	B010266	MICROCIRCUIT,DI:256 X 4 STATIC RAM	07263	93L422SUPRIILB
A15U3050	156-1293-01	B010267		MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A15U3070	156-1293-00	B010100	B010266	MICROCIRCUIT,DI:256 X 4 STATIC RAM	07263	93L422SUPRIILB
A15U3070	156-1293-01	B010267		MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A15U3080	156-1293-00	B010100	B010266	MICROCIRCUIT,DI:256 X 4 STATIC RAM	07263	93L422SUPRIILB
A15U3080	156-1293-01	B010267		MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A15U3090	156-1293-00	B010100	B010266	MICROCIRCUIT,DI:256 X 4 STATIC RAM	07263	93L422SUPRIILB
A15U3090	156-1293-01	B010267		MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A15U3110	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A15U3120	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A15U3130	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A15U3140	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A15U3150	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A15U4100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A15U4010	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U4020	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U4030	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3
A15U4040	156-1613-00			MICROCIRCUIT,DI:SRAM,4096 X 1,W/3 STATE	34649	D2147HL-3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15U4050	156-0693-02			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74S139
A15U4060	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A15U4070	156-0471-02			MICROCIRCUIT,DI:DUAL 4/1 LINEDATA SEL	01295	SN74LS253NP3
A15U4080	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A15U4090	156-0471-02			MICROCIRCUIT,DI:DUAL 4/1 LINEDATA SEL	01295	SN74LS253NP3
A15U4110	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14NP3
A15U4120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A15U4130	156-1393-01			MICROCIRCUIT,DI:QUAD 2 INPUT NAND BFR,SCRN	01295	SN74S38N3/J4
A15U4140	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A15U4150	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A15U4160	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A15U5100	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14NP3
A15U5020	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A15U5030	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10
A15U5040	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A15U5050	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A15U5060	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A15U5070	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A15U5080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A15U5090	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A15U5110	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A15U5120	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A15U5130	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A15U5140	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A15U5150	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A15U5160	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20	670-7304-00			CKT BOARD ASSY:CABLE TERMINATION	80009	670-7304-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A20C1009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C2039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20F2010	159-0021-00			FUSE,CARTRIDGE:3AG,2A,250V,FAST-BLOW	71400	AGC 2
A20F2020	159-0021-00			FUSE,CARTRIDGE:3AG,2A,250V,FAST-BLOW	71400	AGC 2
A20F3010	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
A20R1041	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A20R1043	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A20RP2030	307-0658-00			RES NTWK,FXD,FI:14,220 OHM,14,330 OHM,2%	01121	316E221331
A20U1010	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A20U2040	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30	670-7303-00	B010100	B010182	CKT BOARD ASSY:BUFFER	80009	670-7303-00
A30	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A30	670-7303-01	B010182		CKT BOARD ASSY:BUFFER	80009	670-7303-01
A30	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A30C1011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7032	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C8021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C8031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C8041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C9013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C9041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C9051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C9052	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A30C9091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30CR7031	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A30Q8011	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A30Q9011	151-1103-00			TRANSISTOR:SILICON,FE,N-CHANNEL	18324	SD210EE
A30R1031	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A30R1032	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R1033	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R2031	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A30R2032	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A30R2033	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A30R2051	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R2052	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R4051	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R4052	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R7011	308-0620-00			RES.,FXD,WW:27.0 OHM,1%,3W	80009	308-0620-00
A30R7012	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A30R7013	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A30R7021	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R7022	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30R7023	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R7031	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A30R7032	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A30R7033	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A30R7034	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A30R7041	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R7042	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R7043	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R7044	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R7045	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A30R8011	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A30R8013	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R8014	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R8015	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R8016	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R8017	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A30R8018	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A30R8019	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A30R9011	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A30R9012	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A30R9013	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A30R9031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A30R9041	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A30R9042	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A30U1010	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U1020	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U2040	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A30U2050	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U4010	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A30U4020	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A30U4030	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A30U4040	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14NP3
A30U4050	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A30U5010	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U5020	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U5030	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A30U5040	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A30U5050	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A30U6010	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A30U6020	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U6030	156-0966-01			MICROCIRCUIT,DI:DUAL 5 INP NOR GATES	80009	156-0966-01
A30U6040	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A30U6050	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U7010	156-1617-00			MICROCIRCUIT,DI:HEX 2-INP NORDRVR,SCRN	01295	SN74AS804J1N
A30U7020	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U7030	156-0418-01			MICROCIRCUIT,DI:8 INPUT NAND GATE,SCRN	01295	SN74S30
A30U7040	156-0413-02			MICROCIRCUIT,DI:QUAD 2-INP SCHMITT TRIG	80009	156-0413-02
A30U7050	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U8010	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A30U8020	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A30U8030	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A30U8040	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U8050	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A30U9010	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A30U9020	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A30U9030	156-0303-01			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S03NP3
A30U9040	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A30U9050	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A35	670-7305-00			CKT BOARD ASSY:68000 MOBILE	80009	670-7305-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A35C1011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C1019	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C1041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C2040	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A35C2041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35DL1010	119-1446-00			DELAY LINE,ELEC:25NS,TAPPED,8PIN	90095	TTLDL025
A35DL1020	119-1448-00			DELAY LINE,ELEC:200NS,TAPPED,14 PIN	90095	TTLDL200
A35DL1040	119-1407-00			DELAY LINE,ELEC:100NS,TAPPED,14 PIN	32440	TTLDM100
A35R1016	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A35R2042	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A35RP1009	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A35RP1019	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A35U1030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A35U2020	156-1445-00			MICROCIRCUIT,DI:16-BIT MICROPROCESSOR	04713	MC680001
A35U2040	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40	670-7300-00	B010100	B010191	CKT BOARD ASSY:68000 CONTROL (8300P26-8540/8550 OPTION 3U ONLY)	80009	670-7300-00
A40	670-7300-01	B010192		CKT BOARD ASSY:68000 CONTROL (8300P26-8540/8550 OPTION 3U ONLY)	80009	670-7300-01
A40C1009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C1033	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C1049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C1056	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C2009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C2029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C2039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C2049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C2056	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C3009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C3029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C3039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C3049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C4009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C4029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C4039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C4049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C5009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C5029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C5039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C5049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C6009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C6029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C6039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C6049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C7009	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C7029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C7039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C7049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C8009	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A40C8041	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	72982	0831085Z5E00471J
A40C8049	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40C9059	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A40R1001	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R2031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R2057	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R2058	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R2059	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R3031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R5002	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A40R5003	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A40R5004	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A40R6031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R6038	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R6047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7001	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7002	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7003	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7004	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R7038	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R8024	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A40R8025	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A40R8027	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40R8041	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A40U1010	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A40U1020	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A40U1040	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A40U1050	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A40U2000	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A40U2010	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A40U2020	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A40U2030	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A40U2040	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A40U2050	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A40U3000	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U3010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A40U3020	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A40U3030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A40U3040	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A40U4010	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A40U4020	156-1619-00			MICROCIRCUIT,DI:QUAD BUS BUFFER,W/3 STATE	04713	SN74LS126
A40U4030	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A40U4040	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A40U5010	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A40U5020	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A40U5030	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A40U5040	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A40U6010	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U6020	156-1041-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE COMPARATOR	01295	SN74S85JP4
A40U6030	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POSITIVE EDGE	80009	156-0331-03
A40U6040	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-RLATCH,SCRN	01295	SN74LS279NP3
A40U7010	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP3
A40U7020	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A40U7030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U7040	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A40U8040	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05
A40U8050	156-0955-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	04713	SN74LS241

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50	670-7235-00			CKT BOARD ASSY:POWER SUPPLY	80009	670-7235-00
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A50C1031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1033	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1041	290-0965-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,20VDC	90201	VPR122N020J1L1J
A50C2012	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A50C2015	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A50C2032	283-0005-00			CAP.,FXD,CER DI:0.01UF,+100-0%,250V	72982	8131N300Z5U0103P
A50C3032	283-0197-00			CAP.,FXD,CER DI:470PF,5%,100V	72982	8121N075C0G0471J
A50C5031	290-0965-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,20VDC	90201	VPR122N020J1L1J
A50C6011	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	55680	16U-47V-T
A50C6041	290-0965-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,20VDC	90201	VPR122N020J1L1J
A50CR2014	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A50CR2034	152-0638-00			SEMICOND DEVICE:ZENER,0.4W,7V,5%	80009	152-0638-00
A50CR3021	152-0582-00			SEMICOND DEVICE:SILICON,20V,3A	80009	152-0582-00
A50DS1021	150-1014-00			LAMP,LED:RED,50MA	58361	MV5054-1
A50DS2051	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50DS3051	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50DS3052	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50DS4051	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50DS5051	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50DS6051	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
A50L3021	108-0336-00			COIL,RF:100UH	80009	108-0336-00
A50L4033	108-0554-00			COIL,RF:5UH	80009	108-0554-00
A50L4041	108-0574-00			COIL,RF:30UH	80009	108-0574-00
A50Q2021	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A50Q3011	151-0625-01			TRANSISTOR:D45H11,SCREENED	80009	151-0625-01
A50Q4021	151-0625-01			TRANSISTOR:D45H11,SCREENED	80009	151-0625-01
A50Q5011	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A50Q5012	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A50Q6021	151-0655-00			MICROCIRCUIT,DI:SILICON,NPN	01295	2N3725
A50R1011	311-1936-00			RES.,VAR,NONWIR:CKT BD,50 OHM,20%,0.5W	73138	MODEL 72X
A50R1012	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1022	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A50R1032	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A50R1051	311-1236-00			RES.,VAR,NONWIR:250 OHM,10%,0.50W	73138	72-22-0
A50R1052	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R2011	315-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.25W	01121	CB1505
A50R2012	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	MFF1816G249R0F
A50R2021	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A50R2022	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A50R2033	321-0816-03			RES.,FXD,FILM:5K OHM,0.25%,0.125W	91637	MFF1816D50000C
A50R2034	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A50R3062	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A50R4011	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A50R4012	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A50R4013	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R4014	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A50R4015	303-0470-00			RES.,FXD,CMPSN:47 OHM,5%,1W	01121	GB4705
A50R4031	321-0034-00			RES.,FXD,FILM:22.1 OHM,1%,0.125W	91637	MFF1816G22R10F
A50R4032	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A50R4033	321-0123-00			RES.,FXD,FILM:187 OHM,1%,0.125W	91637	MFF1816G187R0F
A50R4041	321-0097-00			RES.,FXD,FILM:100 OHM,1%,0.125W	91637	MFF1816G100R0F
A50R4042	308-0710-00			RES.,FXD,WW:0.27 OHM,10%,1W	75042	BW20-R2700J
A50R4061	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R4062	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R4063	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50R4064	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R5012	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A50R5013	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A50R5014	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A50TP1011	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A50TP1061	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A50U2010	156-0991-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC78L05ACP
A50U2030	156-1266-00			MICROCIRCUIT,LI:OVER VOLTAGE SENSING CKT	04713	SC77113LH
A50U3040	156-1161-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM317T
A50U3060	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	27014	DM8016
A50VR3022	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A60	----- -----			PROBE ASSY:68000		
	----- -----			(REPLACEABLE AS 175-4575-00)		
	----- -----			(8300P26-8540/8550 OPTION 3U ONLY)		
A60U10	155-0258-00			MICROCIRCUIT,DI:68000 EMULATOR PROBE	80009	155-0258-00
A60U10	----- -----			(REFER TO MAINTENANCE SECTION)		

Section 12
DIAGRAMS

Standards

The following American National Standard Institute standards are used in the preparation of Tektronix, Inc. diagrams.

Graphic Symbols	ANSI Y32.2–1975
Logic Symbols	ANSI Y32.14–1973 (Positive logic. Logic symbols depict the logical function performed and may differ from the manufacturer's data.)
Abbreviations	ANSI Y1.1–1972
Drafting Practices	ANSI Y14.15–1966
Line Conventions And Lettering	ANSI Y14.2–1973
Letter Symbols	ANSI Y10.5–1968

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

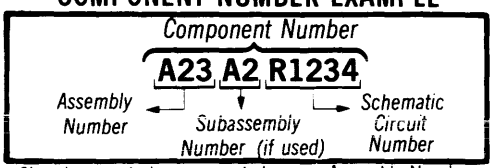
Resistors = Ohms (Ω)

The following special symbols may appear on the diagrams:

Assembly Numbers and Grid Coordinates

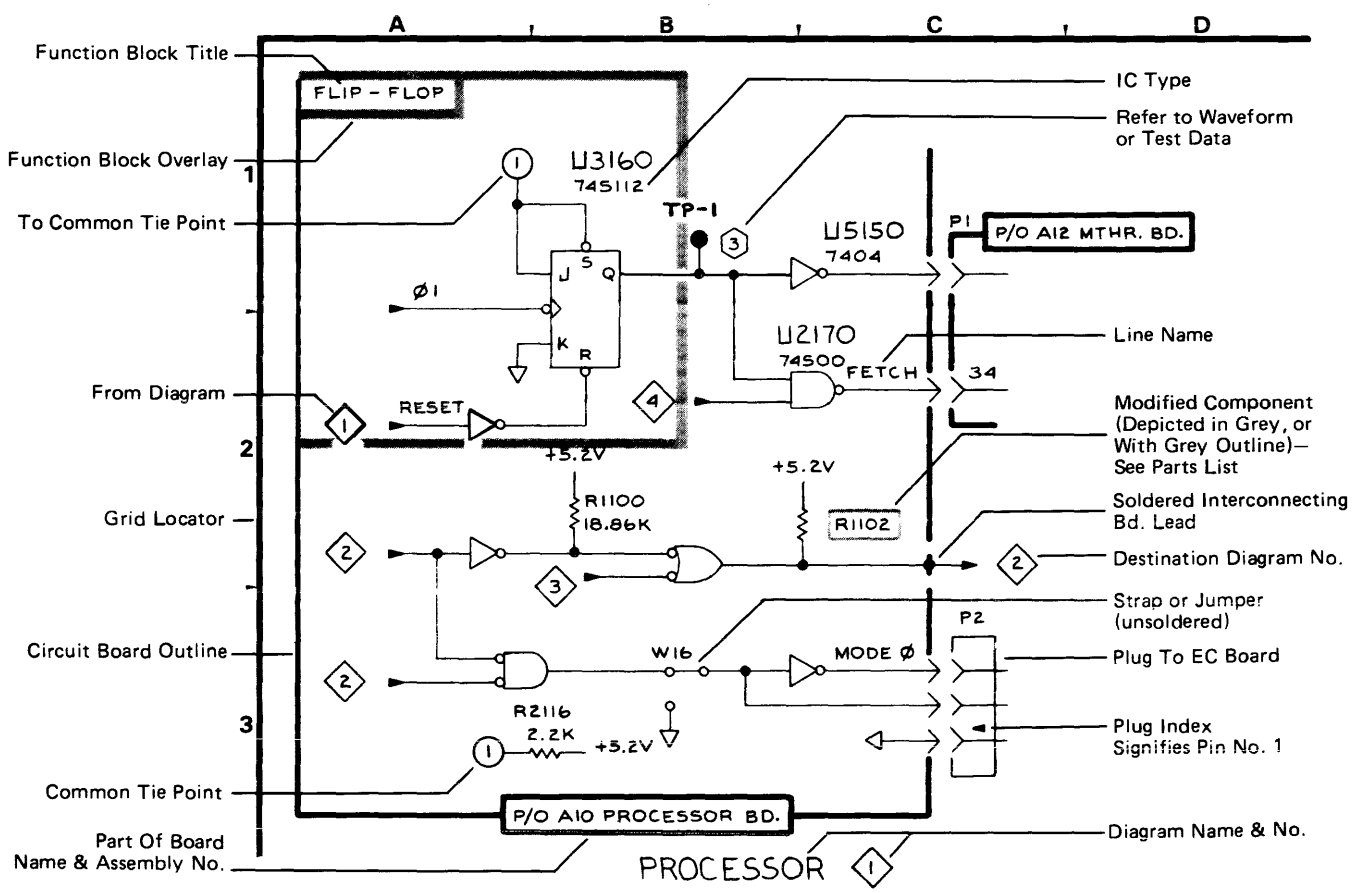
Each circuit board in the instrument is assigned an assembly number (e.g. A20). This number appears on the component location illustration, the schematics, and the component lookup table. The Replaceable Electrical Parts list also uses the number to list components by assembly. The following illustration shows an example of a component number in the Electrical Parts list.

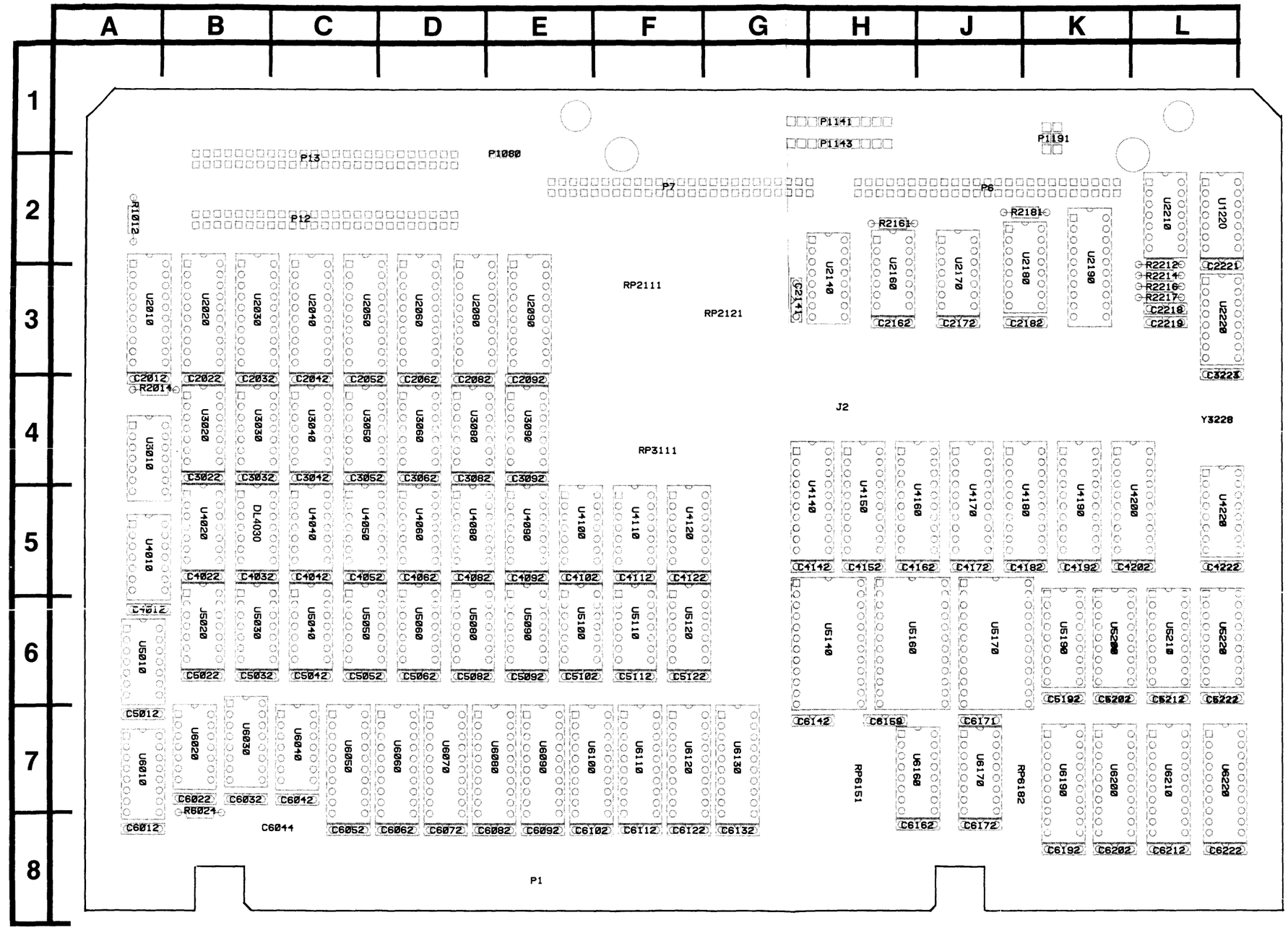
COMPONENT NUMBER EXAMPLE



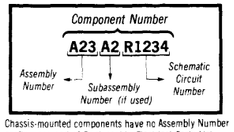
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Both the schematics and the component locator illustration have locating grids. A lookup table is assigned to each schematic. The lookup table gives the component location in both the associated schematic, and on the component locator illustration.





COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-1. A10 68000 EMU 1 Component Locations.

Static Sensitive Devices
See Maintenance Section

Table 12-1
EMU 1 IC Pin Information

DEVICE	GND	VCC[a]	DEVICE	GND	VCC[a]
74S00-LS	7	14	74LS109	8	16
74S02-LS	7	14	74S112	8	16
74S04-LS	7	14	74LS175	8	16
74LS05	7	14	74S240-LS	10	20
74S08	7	14	74S241	10	20
74LS10	7	14	74LS244	10	20
74S11	7	14	74LS245	10	20
74LS20	7	14	74S248	8	16
74LS27	7	14	74S260-LS	7	14
74S30	7	14	74LS273	10	20
74S32-LS	7	14	74LS279	8	16
74S64	7	14	74LS373	10	20
74S74-LS	7	14	82LS181	8	16
74S86	7	14	2114AL-3	9	18

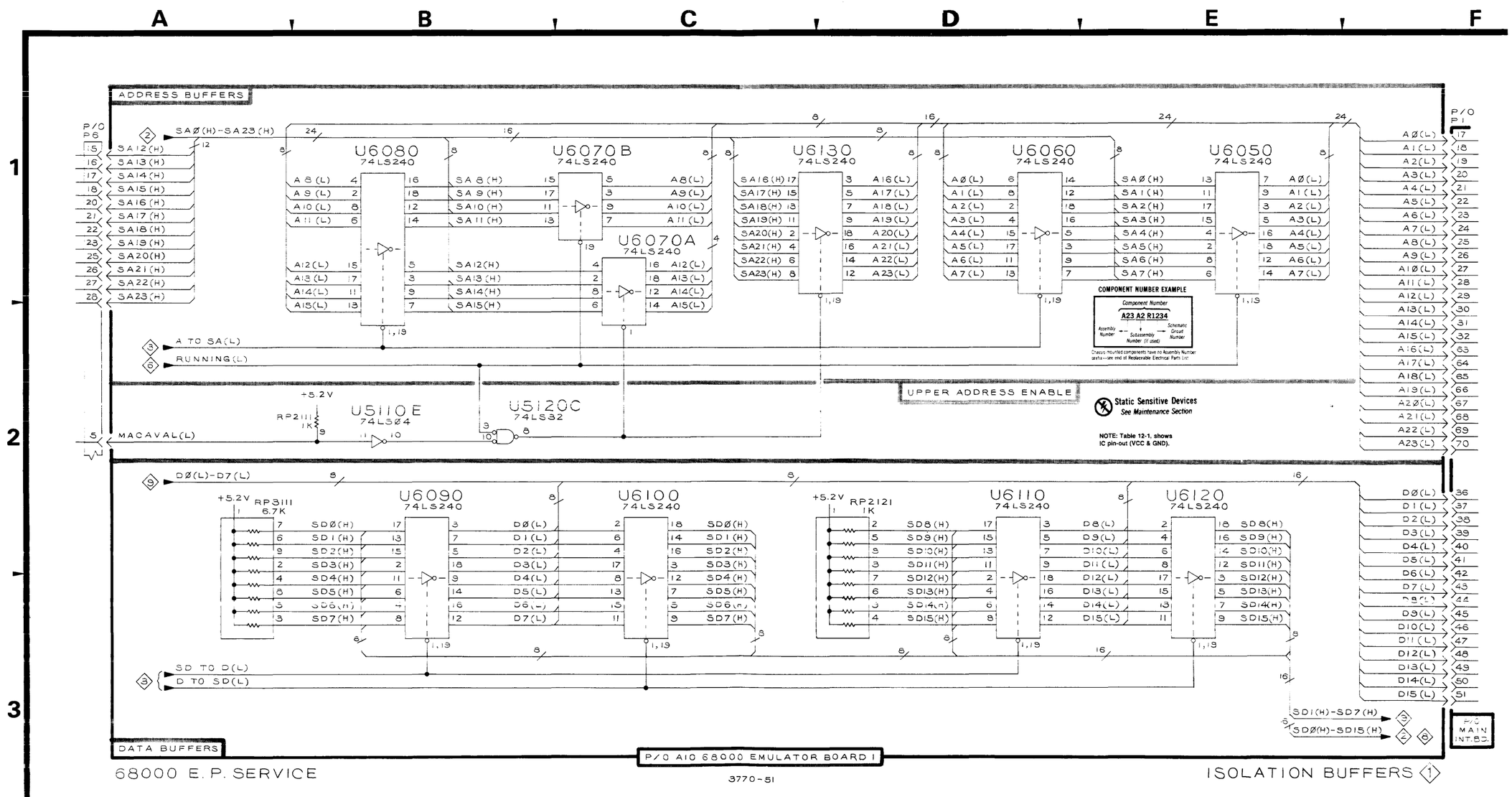
[a] **All VCC supplies are +5.2 Vdc from the development system's Main Interconnect board.**

Table 12-2
Isolation Buffers Diagram 

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	F1	E8	U6060	D1	D7
P6	A1	J2	U6070A	C1	D7
			U6070B	C1	D7
RP2111	B2	F3	U6080	B1	E7
RP2121	D2	G3	U6090	B2	E7
RP3111	A2	F4	U6100	C2	F7
			U6110	D2	F7
U5110E	B2	F6	U6120	E2	G7
U5120C	B2	G6	U6130	C1	G7
U6050	E1	D7			

Partial A10 also shown on diagrams 2, 3, 4, 5, 6, 7, 8 and 9.



68000 E.P. SERVICE

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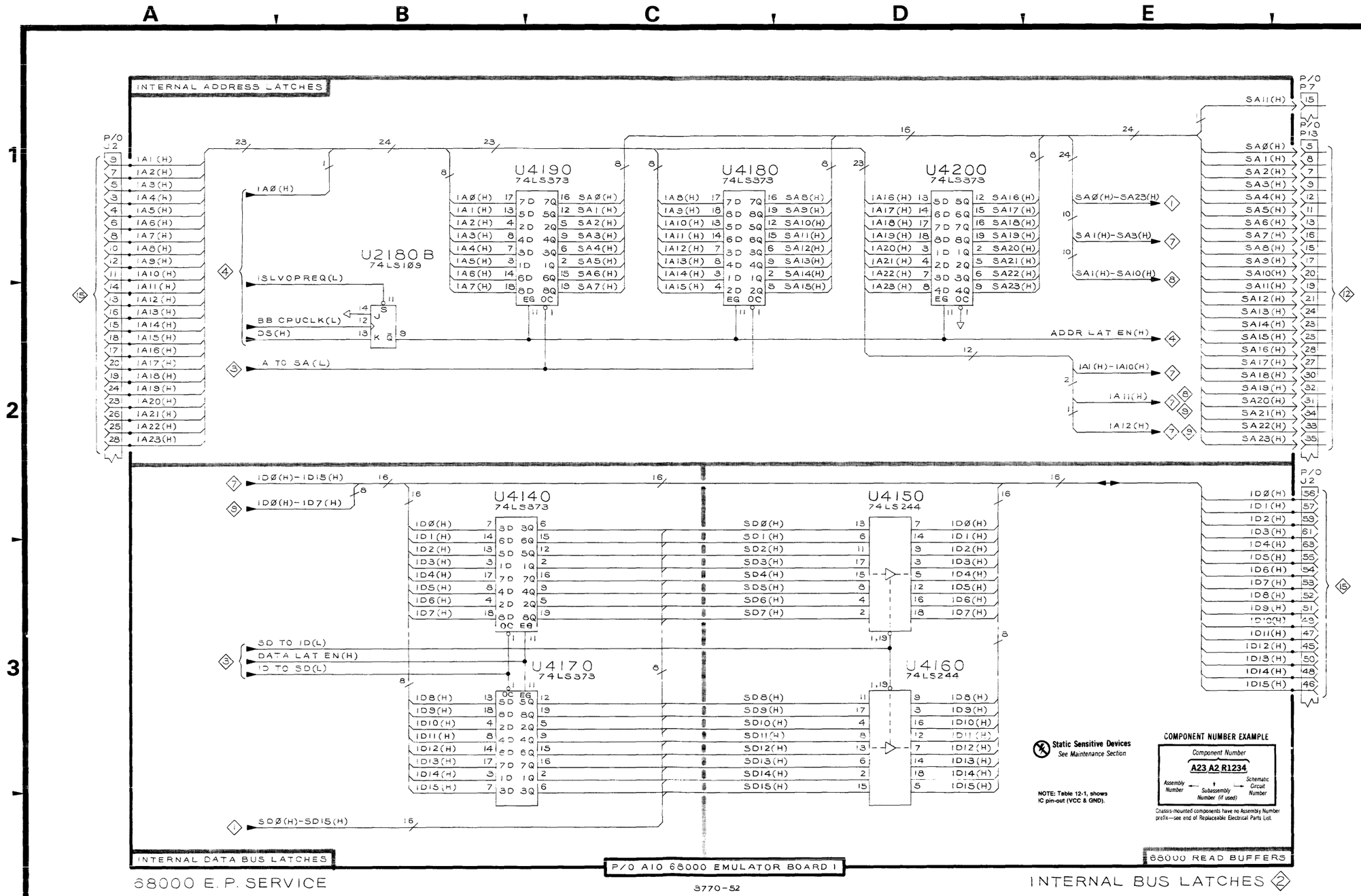
Table 12-3
Internal Bus Latches Diagram 2

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	A1	H4
J2	F2	H4
P7	F1	F2
P13	F1	C2
U2180B	B2	K3
U4140	B2	H5
U4150	D2	H5
U4160	D3	J5
U4170	B3	J5
U4180	C1	K5
U4190	C1	K5
U4200	D1	L5

Partial A10 also shown on diagrams 1, 3, 4, 5, 6, 7, 8 and 9.



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INTERNAL BUS LATCHES ◇2

Table 12-4
Internal Bus Latch/Latch Control Diagram 3

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	A1	H4	U4060C	D2	D5
J2	F2	H4	U4090B	C3	E5
			U4090C	B3	E5
P6	F3	J2	U4100C	E2	F5
P12	A2	C2	U4100D	B3	F5
P13	F1	C2	U4100F	B2	F5
			U4110	E3	F5
RP2111	D3	F3	U4120	D3	G5
RP2111	D4	F3	U5030A	C2	C6
			U5030D	C2	C6
TP1141	D2	H1	U5040A	E2	C6
TP1141-2	E3	H1	U5040D	E2	C6
TP1143	E3	H2	U5050A	D2	D6
TP1143-1	E4	H2	U5050D	D2	D6
TP1143-2	E3	H2	U5060A	B2	D6
TP1143-7	E2	H2	U5060D	B2	D6
TP1143-8	E2	H2	U5080A	C2	E6
			U5100B	D3	F6
U2040	C1	C3	U5120B	B2	G6
U4020D	B3	B5	U6040C	C1	C7
U4050B	C2	D5	U6040D	C2	C7
U4060B	C2	D5			

Partial A10 also shown on diagrams 1, 2, 4, 5, 6, 7, 8 and 9.

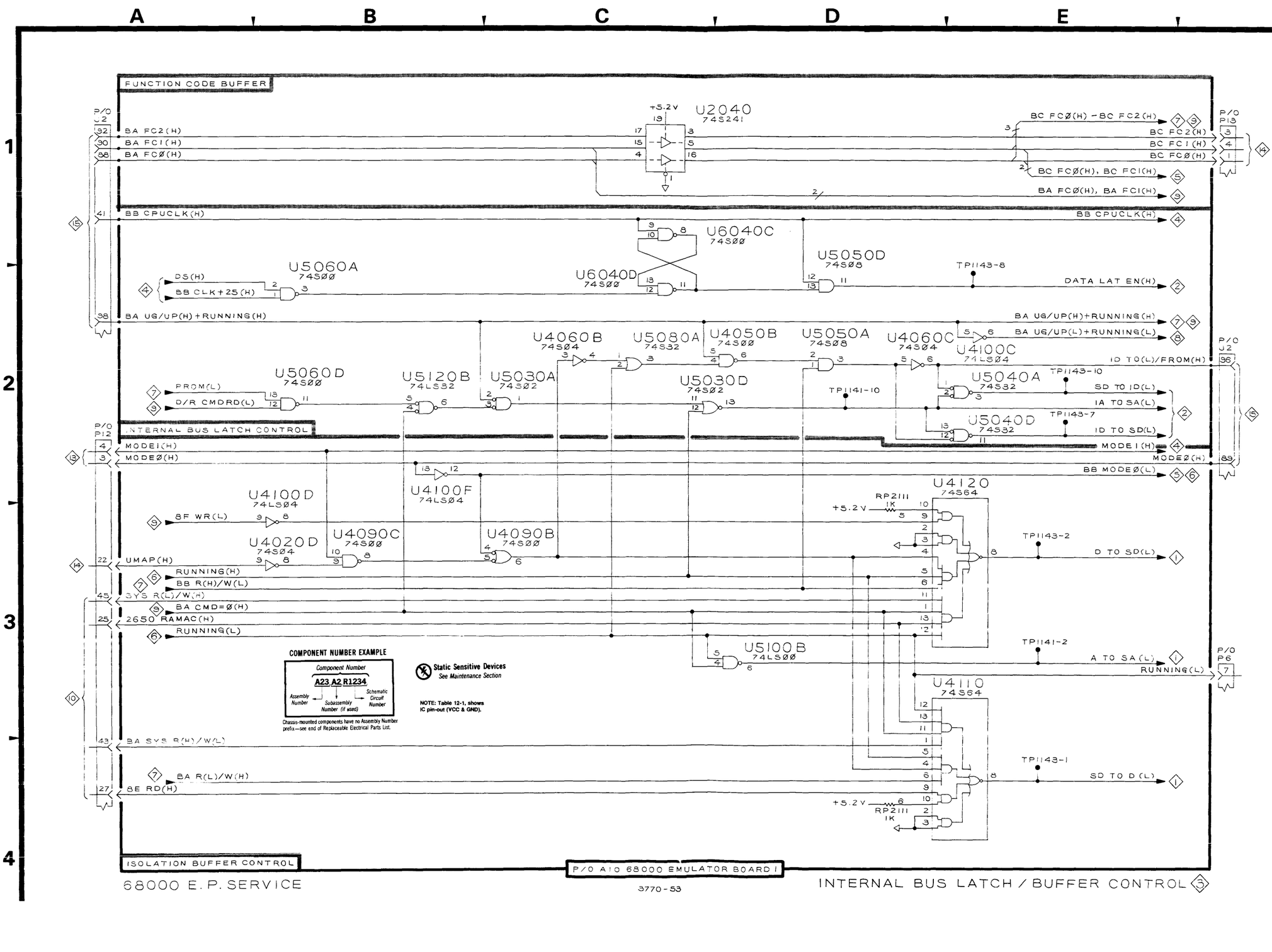

FUNCTION CODE BUFFER
P/O J2
BA FC2(H)
BA FC1(H)
BA FCØ(H)
+5.2V
U2040
74S241
BC FCØ(H) - BC FC2(H)
BC FC2(H)
BC FC1(H)
BC FCØ(H)
BC FCØ(H), BC FC1(H)
BA FCØ(H), BA FC1(H)
P/O P15
BB CPUCLK(H)
U6040C
74SØØ
U5050D
74S08
TP1143-8
DATA LAT EN(H)
U5060A
74SØØ
DS(H)
BB CLK+25(H)
U6040D
74SØØ
BA UG/UP(H)+RUNNING(H)
BA UG/UP(L)+RUNNING(L)
U4060B
74S04
U5080A
74S32
U4050B
74SØØ
U5050A
74S08
U4060C
74S04
U4100C
74LS04
ID TO(L)/FROM(H)
P/O J2
U5060D
74SØØ
PROM(L)
D/R CMDRD(L)
U5120B
74LS32
U5030A
74S02
U5030D
74S02
TP1141-10
U5040A
74S32
TP1143-10
SD TO ID(L)
IA TO SA(L)
U5040D
74S32
TP1143-7
ID TO SD(L)
INTERNAL BUS LATCH CONTROL
P/O P12
MODE1(H)
MODEØ(H)
BB MODEØ(L)
U4100D
74LSØ4
8F WR(L)
U4100F
74LSØ4
U4020D
74SØ4
U4090C
74SØØ
U4090B
74SØØ
U4120
74S64
RP2111
1K
+5.2V
TP1143-2
D TO SD(L)
UMAP(H)
RUNNING(H)
BB R(H)/W(L)
SYS R(L)/W(H)
BA CMD=Ø(H)
2650 RAMAC(H)
RUNNING(L)
U5100B
74LSØØ
TP1141-2
A TO SA(L)
RUNNING(L)
P/O P6
U4110
74S64
BA SYS R(H)/W(L)
BA R(L)/W(H)
8E RD(H)
TP1143-1
SD TO D(L)
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTE: Table 12-1, shows IC pin-out (VCC & GND).
ISOLATION BUFFER CONTROL
P/O A10 68000 EMULATOR BOARD 1
68000 E.P. SERVICE
3770-53
INTERNAL BUS LATCH / BUFFER CONTROL 3

Table 12-5
System Interface Control Diagram

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DL04030	C3	C5	U2040F	B1	C3
			U2190	E3	K3
J2	A1	H4	U2210C	D3	L2
J2	F4	H4	U3030A	D2	C4
			U3050A	E1	D4
P1	F1	E8	U3050C	B1	D4
P1	F3	E8	U3090B	C3	E4
P6	F1	J2	U4010C	C3	B5
P6	F2	J2	U4020B	C2	B5
P7	F2	F2	U4020E	B4	B5
P12	F1	C2	U4050A	B3	D5
P12	F2	C2	U4080A	B3	E5
P12	F3	C2	U4080D	D3	E5
P13	F1	C2	U4090D	D2	E5
			U5030B	D1	C6
R2181	D3	K2	U5040B	D3	C6
R6024	A3	B8	U5040C	D2	C6
			U5060B	D1	D6
RP6151	C3	H7	U5060C	B2	D6
			U5080D	C4	E6
TP1141-4	E2	H1	U5100C	E2	F6
			U5100D	B4	F6
U2020B	C1	B3	U5110C	D1	F6
U2020C	D1	B3	U6020A	C3	B7
U2030	D1	C3	U6020B	E2	B7
U2040'	B2	C3	U6040D	B3	C7

Partial A10 also shown on diagrams 1, 2, 3, 5, 6, 7, 8 and 9.

A B C D E F

1 2 3 4

P/O U2

BA BERR(L) 35
BA BG(L) 71
BA LDS(L) 80
BA UDS(L) 84

U2040F 74S241
U3050C 74S02
U2020B 74240
U2020C 74S240
U5110C 74LS04
U2030 74LS373
U3050A 74S02
U5030B 74S02
U2040C 74S241
U5060B 74S00
U5060C 74S00
U3030A 74S02
U5100C 74LS00
U6020B 74S74
U5040C 74S32
U4020B 74S224
U4090D 74S00
U5040B 74S32
U2210C 74S04
U2190 74S240
U4050A 74S00
U4010C 74LS00
U6040D 74S00
U6020A 74S74
U4080D 74S08
U4080A 74S08
DL4030 DM-100
U3090B 74S260
U5100D 74LS00
U4020E 74S04
U5080D 74S32

ADDR LAT EN(H) 2
BB R(H)/W(L) 7
RUNNING(L) 5
BA R(L)/W(H) 7
BB CPU CLK(H) 3
BB CLK+25(H) 5 66

SYSTEM INTERFACE AND CONTROL
UMAP VALID GENERATOR
TTA STROBE GENERATION

R6024 1K +5.2V 1

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234
Assembly Number · Subassemoly Number (if used) · Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

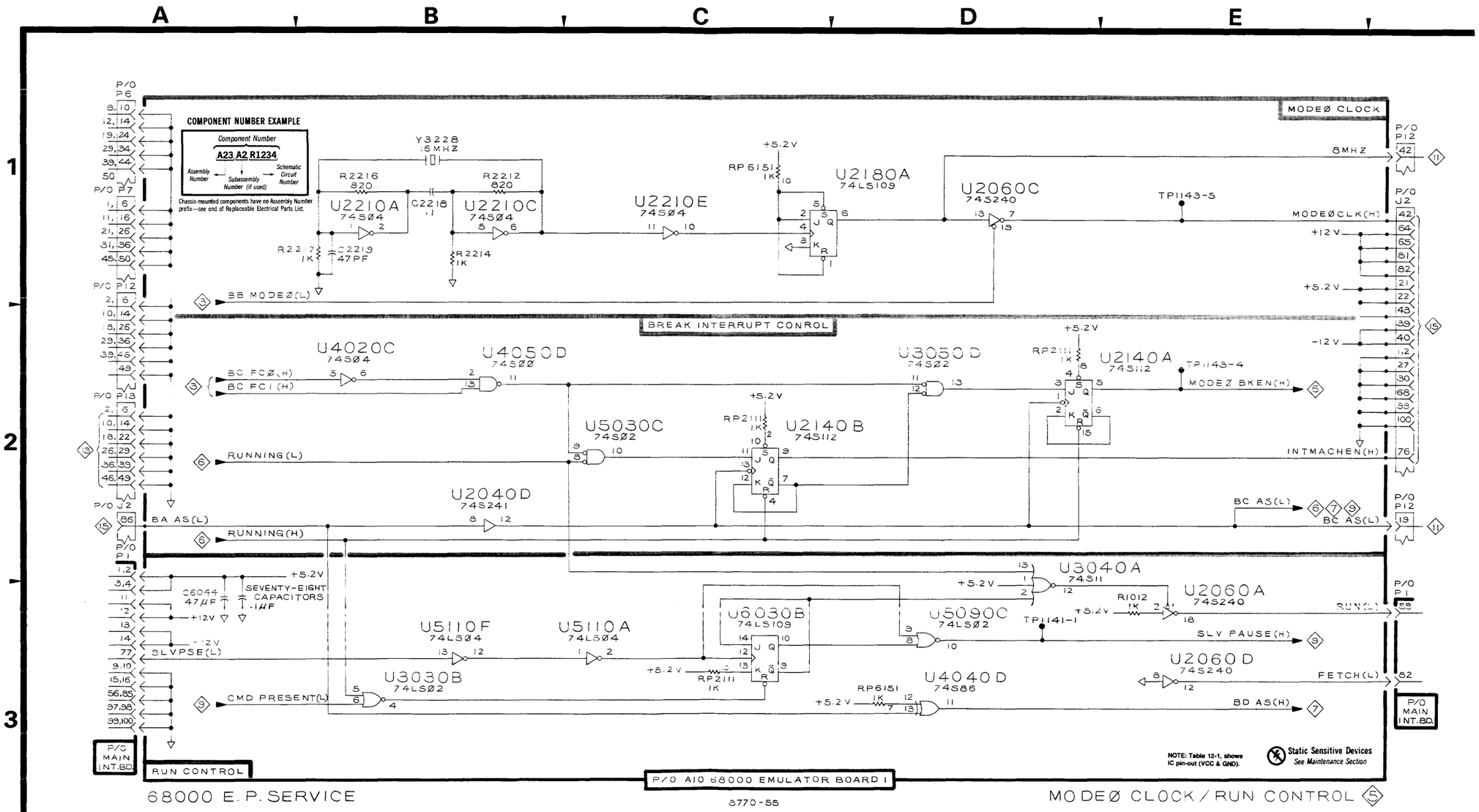
NOTE: Table 12-1, shows IC pin-out (VCC & GND).

BKINTA(L) 7 8
OPREQ EN(H)
SVC-M(H)/IO(L) 44
WRPROT(H) 33 14
MODE1(H) 3
SMAP(H) 6
ACTIVE O.C.(H) 40 13
BSACK(L) 13 11
MODE2(H) 1
FFC0(H) 8
FFC1(H) 7 13
FFC2(H) 9

P/O P6
BA BERR(L) 36,40
BA BG(L) 32
IBYTE(H)/WORD(L) 46
BB LDS(H)
BA UDS(H) 8
BA BG(L) 11
IBYTE(H)/WORD(L) 37 12
P/O P13
IAØ(H) 5
P/O P1
IAØ(H) 2
WD ACCESS(L) 35
SWAP(L) 80
P/O MAIN INT.BD.
BB LDS(L) 9
DS(H) 2 3
P/O P7
IAØ(H) 2
P/O P12
UMAP EN(H) 21 14
TP1141-4
ISLVOPREQ(L) 35
ISLVOPREQ(L) 2
BB CLK+25(H) 3
P/O P6
TOPSTRBDATA(L) 3
ISLVOPREQ(L) 9
P/O P12
IOPREQ(H) 6 7
BB CPUCLK(L) 20 13
BB CPUCLK(L) 2
P/O P1
SLV CLK(L) 53
SYS R(H)/W(L) 55
SLV OPREQ(L) 75
BYTE ADDR(L) 86
OPREQ(L) 54
M(L)/IO(H) 52
WRP(L) 53
P/O MAIN INT. BD.
P/O U2
DISABLE WR(H) 95
ACTIVE O.C.(H) 33
BGACK(L) 73
MODE2(H) 91 15
FFC0(H) 58
FFC1(H) 60
FFC2(H) 62

TP1141-3
R2181 1K +5.2V

P/O A10 68000 EMULATOR BOARD 1



68000 E. P. SERVICE

3770-55

MODEØ CLOCK / RUN CONTROL

Table 12-7
NMI/Reset/Halt/User Run Control Diagram 6

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	A1	H4	TP1143-3	B1	H2
J2	A2	H4	TP1143-6	C2	H2
J2	F1	H4			
J2	F2	H4	U1220A	C3	M2
J2	F3	H4	U1220B	D3	M2
			U2060H	B3	D3
P1	A3	E8	U2160A	B3	J3
P6	F2	J2	U2160D	C1	J3
P12	A1	C2	U2160F	C3	J3
P12	A3	C2	U2170A	D2	J3
P12	F1	C2	U3040B	C3	C4
P12	F2	C2	U4010B	C1	B5
P12	F3	C2	U4020F	B3	B5
P13	A1	C2	U4060D	E3	D5
P13	A3	C2	U4060E	D3	D5
P13	F3	C2	U4090A	B2	E5
P1080	C3	E2	U4100A	C2	F5
P1191	D2	K2	U5090A	B3	E6
			U5090B	B3	E6
R2014	C3	L3	U5090D	B1	E6
R2161	D3	J2	U5110B	C3	F6
R6024	B2	B8	U6030A	C2	C7
			U6160B	B2	J7
RP2111	C2	F3	U6160D	D3	J7
RP2111	D1	F3			
RP6182	B3	K7			

Partial A10 also shown on diagrams 1, 2, 3, 4, 5, 7, 8 and 9.

A B C D E

1 2 3

AUTO VECTOR REQUEST

P/O P13 48 SMAP(H) ← SMAP(H) → P/O J2 38 SMAP(H) ◇4

P/O J2 44 BA HALT(L) ◇15 → P/O P12 47 BA HALT(L) ◇11

TP1143-3

◇7 BIKINTA(L)

◇5 BC AS(L)

U5090D 74LS02

U2160D 74LS05

+5.2V RP2111 1K

P/O J2 37 VPA(L)

NMI CONTROL

U4010B 74LS00

P/O P12 17 BKCOND(H) ◇11 → BRDDTACK(L) 69 / BKCOND(H) 97

U4090A 74S00

U4100A 74LS04

RP2111 1K +5.2V

U2170A 74LS74

◇5 MODE0 BKEN(H)

P/O J2 72 DTACKEN(H)

TP1143-6

P1131

BKINT(H) ◇8

P/O P6 45 VPA(L)

◇7 D/R EN(L)

29 BA IPL0(H) → BA HALT(L) 33,37

31 BA IPL1(H) → BA IPL0(H) 43

33 BA IPL2(H) → BA IPL1(H) 42

BA IPL2(H) 41

RESET/HALT CONTROL

Static Sensitive Devices
See Maintenance Section

NOTE: Table 12-1, shows IC pin-out (VCC & GND).

COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234 (Assembly Number / Subassembly Number (if used) / Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

R6024 1K +5.2V

U6030A 74LS109

RESET SEQ EN(H) ◇7

P/O J2 74 DLYD ACTIVE(H) / 79 RESET(L) ◇15

DLYD ACTIVE(H) ◇7 ◇9

P/O P12 16 RESET(L) / 15 BRDHALT(L) ◇11

U2160B 74LS05

U2160A 74LS05

◇7 UNSTACKING(L)

77 BRDHALT(L)

U5090B 74LS02

P/O P13 50 HALTED(H) ◇13

P/O P12 12 DLYD ACTIVE(H) ◇11

U4020E 74S04

U2060H 74S240 RP6182 1K

U5110B 74LS04

P1080

U1220A 74LS27

U2160F 74LS05

R2161 1K +5.2V

U1220B 74LS27

U6160D 74LS279

U4060D 74S04

USER RUN CONTROL

BB DLYD ACTIVE(L) ◇3

RUNNING(L) ◇1 ◇3 ◇4 ◇5

◇3 BB MODE0(L)

P/O P13 47 CLKFAIL(H) ◇3

P/O P12 34 RUNNING(H) ◇13

◇4 IOPREQ(H)

◇7 RESET RUN(L)

SETRUN(L)

U5090A 74LS02

U4060E 74S04

RUNNING(H) ◇3 ◇5

P/O J2 36 RUNNING(H) ◇15

F.P. HOLD INTERFACE

R2014 1K +5.2V

U3040B 74S11

P/O P1 87 F.P.HOLD(L)

HOLD(L) 70

P/O MAIN INT. BD.

P/O A10 68000 EMULATOR BOARD 1

68000 E.P. SERVICE

3770-56

NMI / RESET / HALT / USER RUN CONTROL ◇6

Table 12-8
D/R Restore Proms Diagram 

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	A1	H4	U2220B	D3	L3
J2	A3	H4	U2220C	C3	L3
J2	F2	H4	U2220D	D3	L3
			U3020	B4	B4
P6	F1	J2	U3050B	D4	D4
P6	F4	J2	U3090A	B2	E4
P12	F2	C2	U4050C	B4	D5
			U4060A	D4	D5
RP6151	C2	H7	U4060F	B2	D5
RP6151	D2	H7	U4100E	D4	F5
			U4220	C4	L5
TP1141-5	D4	H1	U5080C	D4	E6
TP1141-7	E3	H1	U5110D	C3	F6
TP1141-8	D3	H1	U5120A	E3	G6
TP1141-9	D4	H1	U5140	B1	H6
			U5160	D1	J6
U1220C	E3	M2	U5170	B2	K6
U2020A	E3	B3	U6160	E2	J7
U2020D	B2	B3	U6170D	C3	J7
U2040A	B2	C3	U6170	C2	J7
U2220A	D3	L3			

Partial A10 also shown on diagrams 1, 2, 3, 4, 5, 6, 8 and 9.

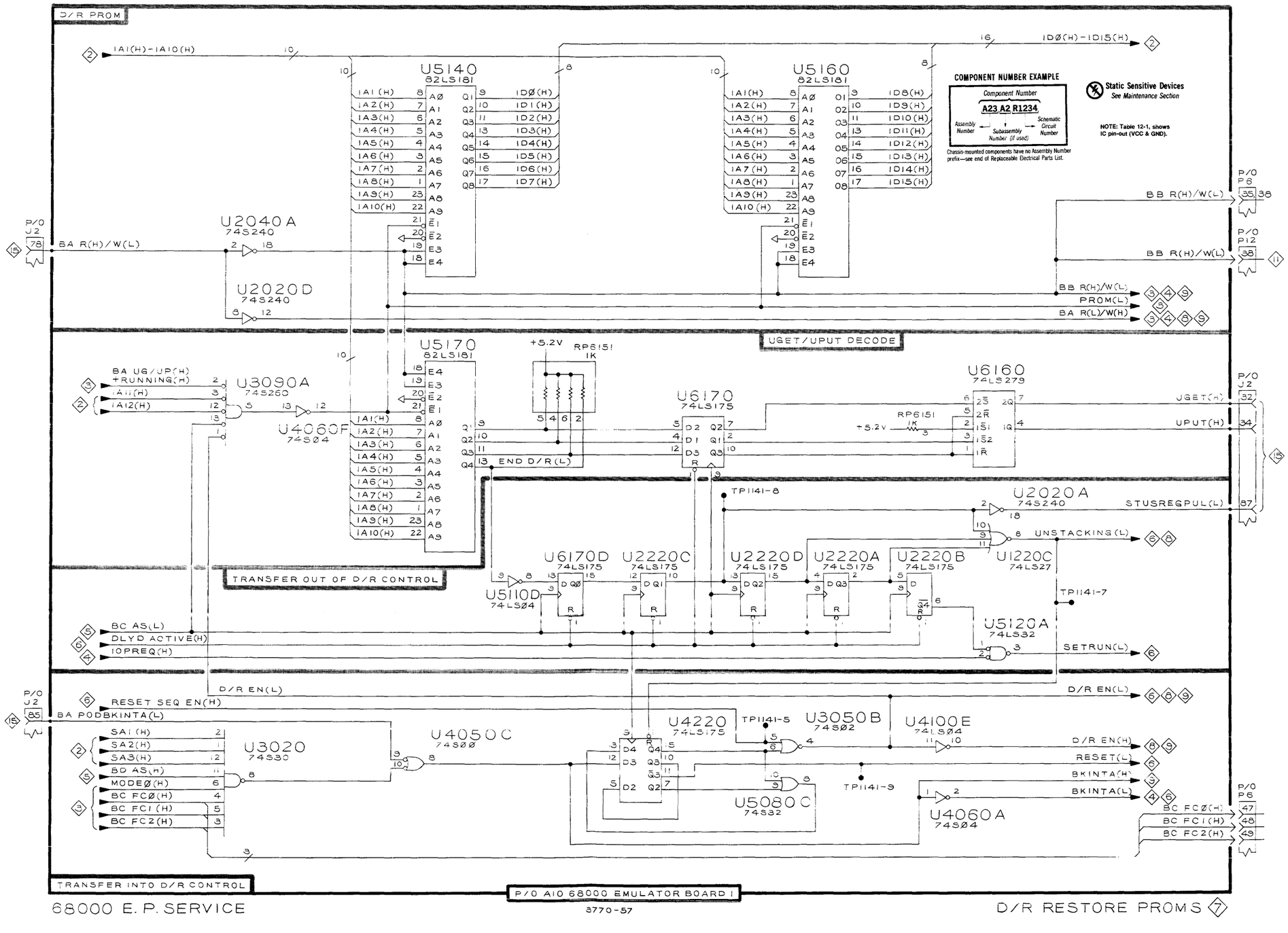

D/R PROM
U5140
82LS181
U5160
82LS181
U2040A
74S240
U2020D
74S240
U5170
82LS181
U3090A
74S260
U4060F
74S04
+5.2V
RP6151
1K
U6170
74LS175
U6160
74LS279
U2020A
74S240
U6170D
74LS175
U2220C
74LS175
U2220D
74LS175
U2220A
74LS175
U2220B
74LS175
U1220C
74LS27
U5110D
74LS04
U5120A
74LS32
U4050C
74S00
U3020
74S30
U4220
74LS175
U3050B
74S02
U4100E
74LS04
U5080C
74S32
U4060A
74S04
UGET/UPUT DECODE
TRANSFER OUT OF D/R CONTROL
TRANSFER INTO D/R CONTROL
P/O A10 68000 EMULATOR BOARD 1
3770-57
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTE: Table 12-1, shows IC pin-out (VCC & GND).
BA R(H)/W(L)
BB R(H)/W(L)
PROM(L)
BA R(L)/W(H)
D/R EN(L)
RESET SEQ EN(H)
BA PODBKINTA(L)
BC AS(L)
DLYD ACTIVE(H)
IOPREQ(H)
END D/R(L)
UNSTACKING(L)
SETRUN(L)
STUSREGPUL(L)
RESET(L)
BKINTA(H)
BKINTA(L)
UGET(H)
UPUT(H)
BC FC0(H)
BC FC1(H)
BC FC2(H)
68000 E.P. SERVICE
D/R RESTORE PROMS 7

Table 12-9
Shared Ram Diagram 8

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P7	F1	F2
P12	A2	C2
P13	F3	C2
RP6182	C1	K7
U3060C	B2	D4
U4010A	B2	B5
U4010D	B2	B5
U4080B	B2	E5
U4080C	B2	E5
U5010A	A2	B6
U5010C	B2	B6
U5190	C2	K6
U5200	D2	L6
U5210	E2	L6
U5220	D2	L6
U6040A	B1	C7
U6190	B1	K7
U6200	C3	L7
U6210	D3	L7
U6220	E3	L7

Partial A10 also shown on diagrams 1, 2, 3, 4, 5, 6, 7 and 9.

D/R INTERRUPT TRAPSTACK CONTROL

U6190 74LS244

SA1(H)-SA10(H)

SA3(H) SA4(H) SA5(H) SA6(H) SA7(H) SA8(H) SA9(H) SA10(H)

D/R A2(H) D/R A3(H) D/R A4(H) D/R A5(H) D/R A6(H) D/R A7(H) D/R A8(H) D/R A9(H)

+5.2V

RP6182 1K

U6040A 74S00

UNSTACKING(L)

U5010A 74LS10

U5010C 74LS10

U4080B 74S08

U4010D 74LS00

U3060C 74LS20

BKINT(H)
D/R EN(L)
BA R(L)/W(H)
BA UB/UP(L)+ RUNNING(L)
D/R EN(H)
BA1(H)
CMD=0(L)
BA LDS(H)
2650 LCS(L)

P/O P12

SHARED RAM SELECT

U4010A 74LS00

U4080C 74S08

BA UDS(H)
SHARED R(H)/W(L)
2650 HCS(L)

HCS(L)
LCS(L)

U5190 2114AL-3
U5200 2114AL-3
U5220 2114AL-3
U5210 2114AL-3

SA1(H) SA2(H) D/R A2(H) D/R A3(H) D/R A4(H) D/R A5(H) D/R A6(H) D/R A7(H) D/R A8(H) D/R A9(H)

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 I/O0 I/O1 I/O2 I/O3 CS WE

D/R D12(H) D/R D13(H) D/R D14(H) D/R D15(H)
D/R D8(H) D/R D9(H) D/R D10(H) D/R D11(H)
D/R D4(H) D/R D5(H) D/R D6(H) D/R D7(H)
D/R D0(H) D/R D1(H) D/R D2(H) D/R D3(H)

U6200 74LS245
U6210 74LS245
U6220 74LS245

68000 HCS(L)

DR E

SD8(H) SD9(H) SD10(H) SD11(H) SD12(H) SD13(H) SD14(H) SD15(H)

D/R D8(H) D/R D9(H) D/R D10(H) D/R D11(H) D/R D12(H) D/R D13(H) D/R D14(H) D/R D15(H)

SD0(H) SD1(H) SD2(H) SD3(H) SD4(H) SD5(H) SD6(H) SD7(H)

D/R D0(H) D/R D1(H) D/R D2(H) D/R D3(H) D/R D4(H) D/R D5(H) D/R D6(H) D/R D7(H)

SD0(H)-SD15(H)

P/O P7

SA1(H) SA2(H) SA3(H) SA4(H) SA5(H) SA6(H) SA7(H) SA8(H) SA9(H) SA10(H)

SD0(H) SD1(H) SD2(H) SD3(H) SD4(H) SD5(H) SD6(H) SD7(H) SD8(H) SD9(H) SD10(H) SD11(H) SD12(H) SD13(H) SD14(H) SD15(H)

P/O P13

SD0(H) SD1(H) SD2(H) SD3(H) SD4(H) SD5(H) SD6(H) SD7(H)

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 12-1, shows IC pin-out (VCC & GND).

SHARED RAM

P/O A10 68000 EMULATOR BOARD 1

68000 E. P. SERVICE

SHARED RAM

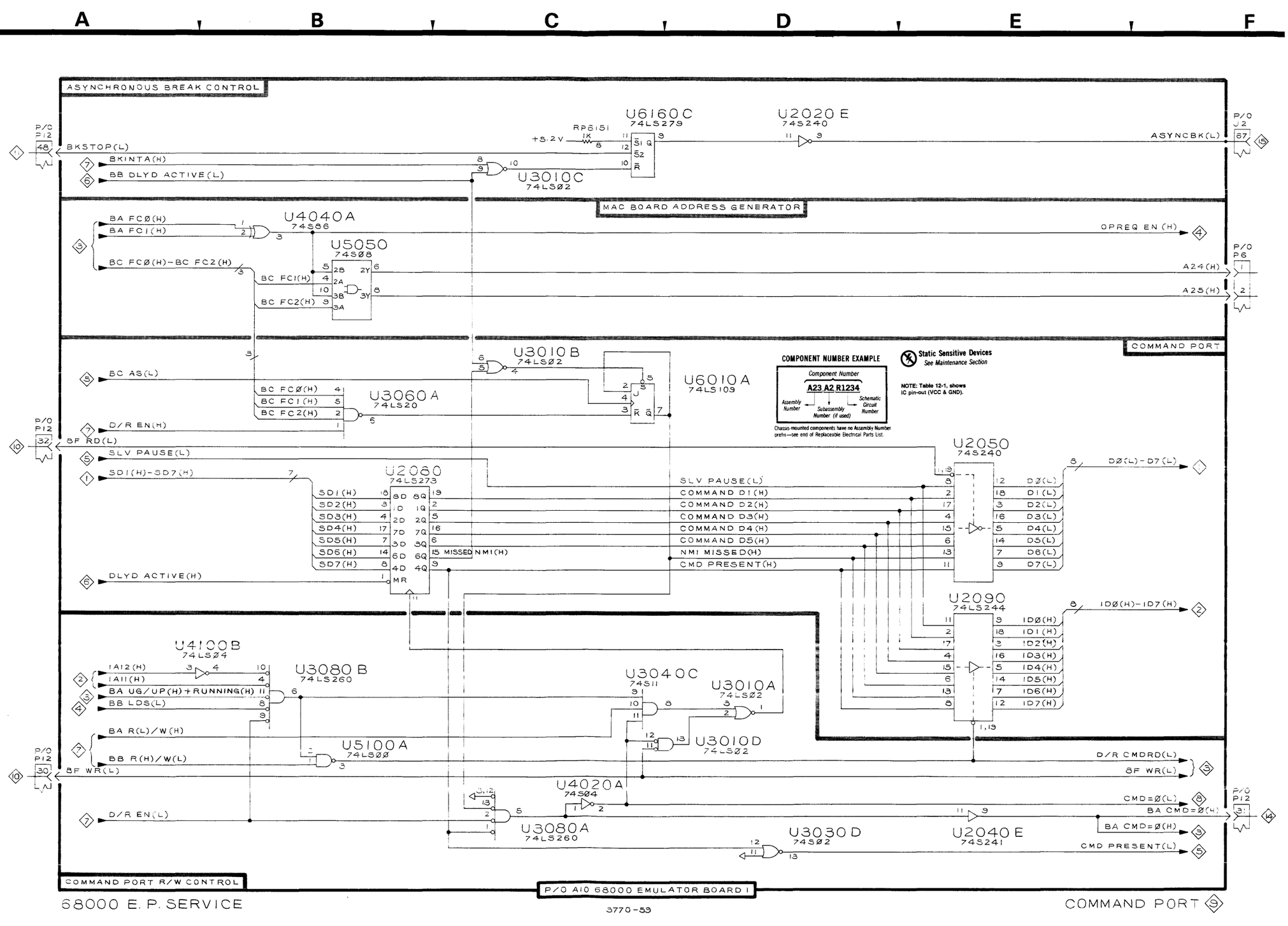
3770-58

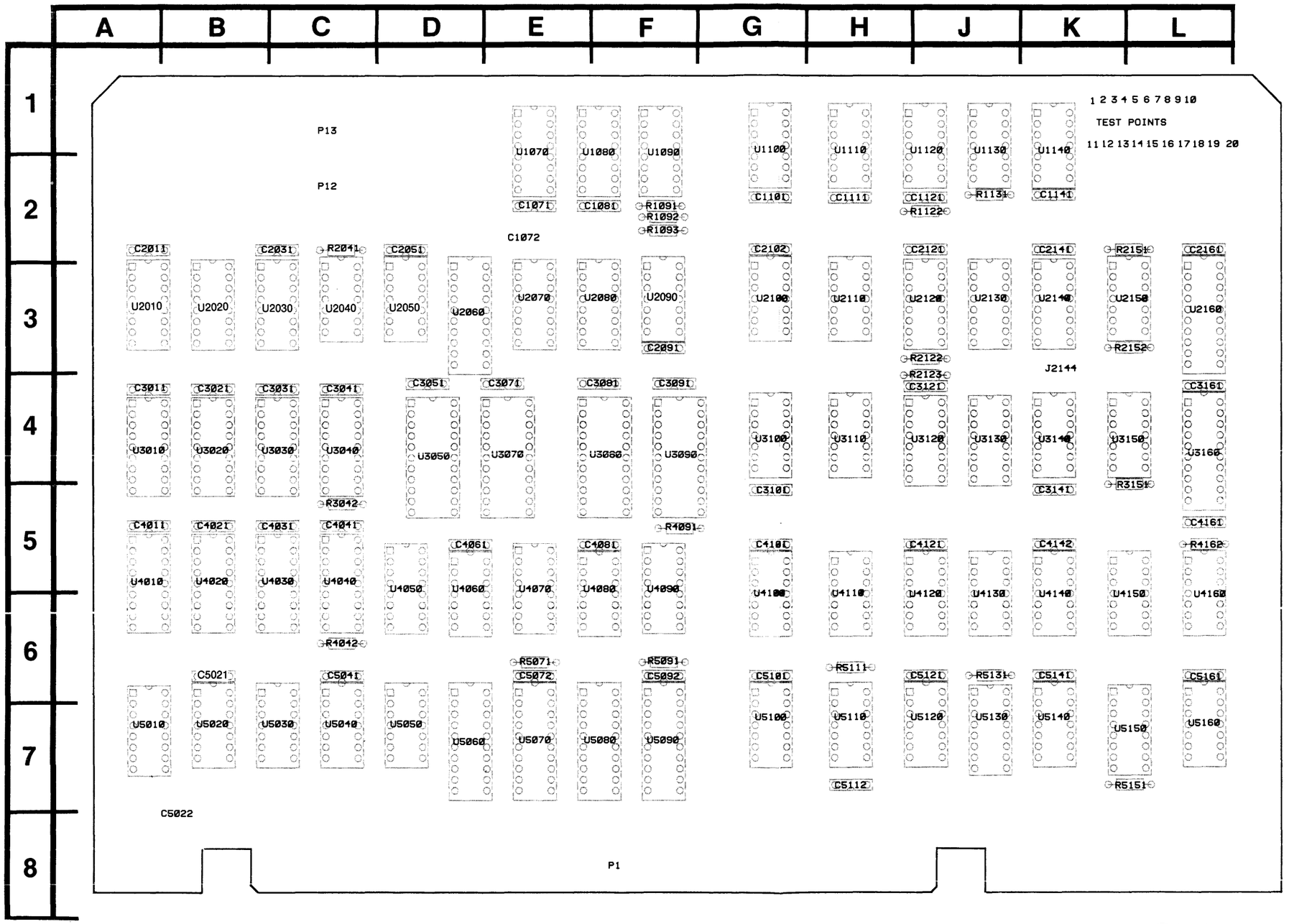
Table 12-10
Command Port Diagram 

ASSEMBLY A10

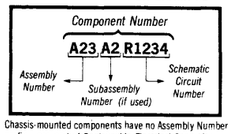
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	F1	H4	U3010B	C2	B4
			U3010C	C1	B4
P6	F1	J2	U3010D	C3	B4
P12	A1	C2	U3030D	D4	C4
P12	A2	C2	U3040C	C3	C4
P12	A4	C2	U3060A	B2	D4
P12	F4	C2	U3080A	C4	E4
			U3080B	B3	E4
RP6151	C1	H7	U4020A	C4	B5
			U4040A	B1	C5
U2020E	D1	B3	U4100B	A3	F5
U2040E	E4	C3	U5050	B1	D6
U2050	E2	D3	U5100A	B4	F6
U2080	B2	E3	U6010A	D2	B7
U2090	E3	E3	U6160C	C1	J7
U3010A	D3	B4			

Partial A10 also shown on diagrams 1, 2, 3, 4, 5, 6, 7 and 8.


ASYNCHRONOUS BREAK CONTROL
MAC BOARD ADDRESS GENERATOR
COMMAND PORT
COMMAND PORT R/W CONTROL
P/O A10 68000 EMULATOR BOARD 1
68000 E. P. SERVICE
COMMAND PORT
3770-53
U6160C 74LS279
U2020E 74S240
RP5151 1K
+5.2V
BKSTOP(L)
BKINTA(H)
BB DLYD ACTIVE(L)
ASYNCBK(L)
U3010C 74LS02
U4040A 74S86
U5050 74S08
BA FC0(H)
BA FC1(H)
BC FC0(H)-BC FC2(H)
OPREQ EN(H)
A24(H)
A25(H)
U3010B 74LS02
U6010A 74LS109
U3060A 74LS20
BC AS(L)
BC FC0(H)
BC FC1(H)
BC FC2(H)
D/R EN(H)
BF RD(L)
SLV PAUSE(L)
SD1(H)-SD7(H)
U2080 74LS273
DLYD ACTIVE(H)
MISSED NMI(H)
U2050 74S240
U2090 74LS244
COMMAND D1(H)
COMMAND D2(H)
COMMAND D3(H)
COMMAND D4(H)
COMMAND D5(H)
NMI MISSED(H)
CMD PRESENT(H)
D0(L)-D7(L)
ID0(H)-ID7(H)
U4100B 74LS24
U3080B 74LS260
U3040C 74S11
U3010A 74LS02
U3010D 74LS02
U5100A 74LS00
BA R(L)/W(H)
BB R(H)/W(L)
BF WR(L)
D/R CMDRD(L)
U4020A 74S04
U3080A 74LS260
U3030D 74S02
U2040E 74S241
CMD=0(L)
BA CMD=0(H)
CMD PRESENT(L)
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTE: Table 12-1, shows IC pin-out (VCC & GND).



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-2. A15 68000 EMU 2 Component Locations.

Static Sensitive Devices
See Maintenance Section

3770-44

Table 12-11
EMU 2 IC Pin Information

DEVICE	GND	VCC[a]	DEVICE	GND	VCC[a]
74LS00	7	14	74LS86	7	14
74S02-LS	7	14	74LS109	8	16
74S04-LS	7	14	74LS138	8	16
74S05	7	14	74S139	8	16
74LS08	7	14	74LS240	10	20
74S10-LS	7	14	74LS253	8	16
74LS14	7	14	74S257-LS	8	16
74LS20	7	14	74LS260	7	14
74LS27	7	14	74LS273	10	20
74S30-LS	7	14	74LS374	10	20
74LS32	7	14	74LS390	8	16
74S38	7	14	93L422	8	22
74S74-LS	7	14	2147H	9	18

[a] **All VCC supplies are +5.2 Vdc from the development system's Main Interconnect board.**

Table 12-12
I/O and Ram Access Control Diagram 

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	A1	F8	U3110B	C3	H4
P1	F3	F8	U3130	D1	J4
P12	F1	C2	U4050B	E3	D6
			U4100A	D3	G6
R5071	E3	E6	U4100B	E2	G6
			U4100C	E2	G6
TP4	E1	L1	U4100D	D3	G6
TP5	D1	L1	U4110E	A3	H6
TP6	E2	L1	U4120A	B2	J6
TP7	E2	L1	U4130A	D3	J6
TP9	E3	L1	U4140B	C4	K6
TP11	D1	K2	U4150A	C3	L6
TP12	D1	K2	U5020A	B1	B7
TP13	E1	L2	U5020B	B1	B7
TP14	E1	L2	U5030A	C1	C7
TP15	E1	L2	U5030B	B1	C7
TP17	E3	L2	U5030C	C1	C7
TP18	E3	L2	U5040C	C2	C7
TP19	E3	L2	U5050B	B3	D7
TP20	E3	L2	U5100A	D2	G7
			U5100D	B2	G7
U2080D	E2	F3	U5100F	C1	G7
U2100B	E2	G3	U5120B	C2	J7
U2100D	E2	G3	U5120D	D2	J7
U2100E	E2	G3	U5140A	D3	K7
U3100A	E3	G4	U5140E	D3	K7
U3100B	D1	G4	U5160A	D3	L7
U3100C	D1	G4	U5160B	C3	L7
U3100D	D3	G4			

Partial A15 also shown on diagrams 11, 12, 13 and 14.

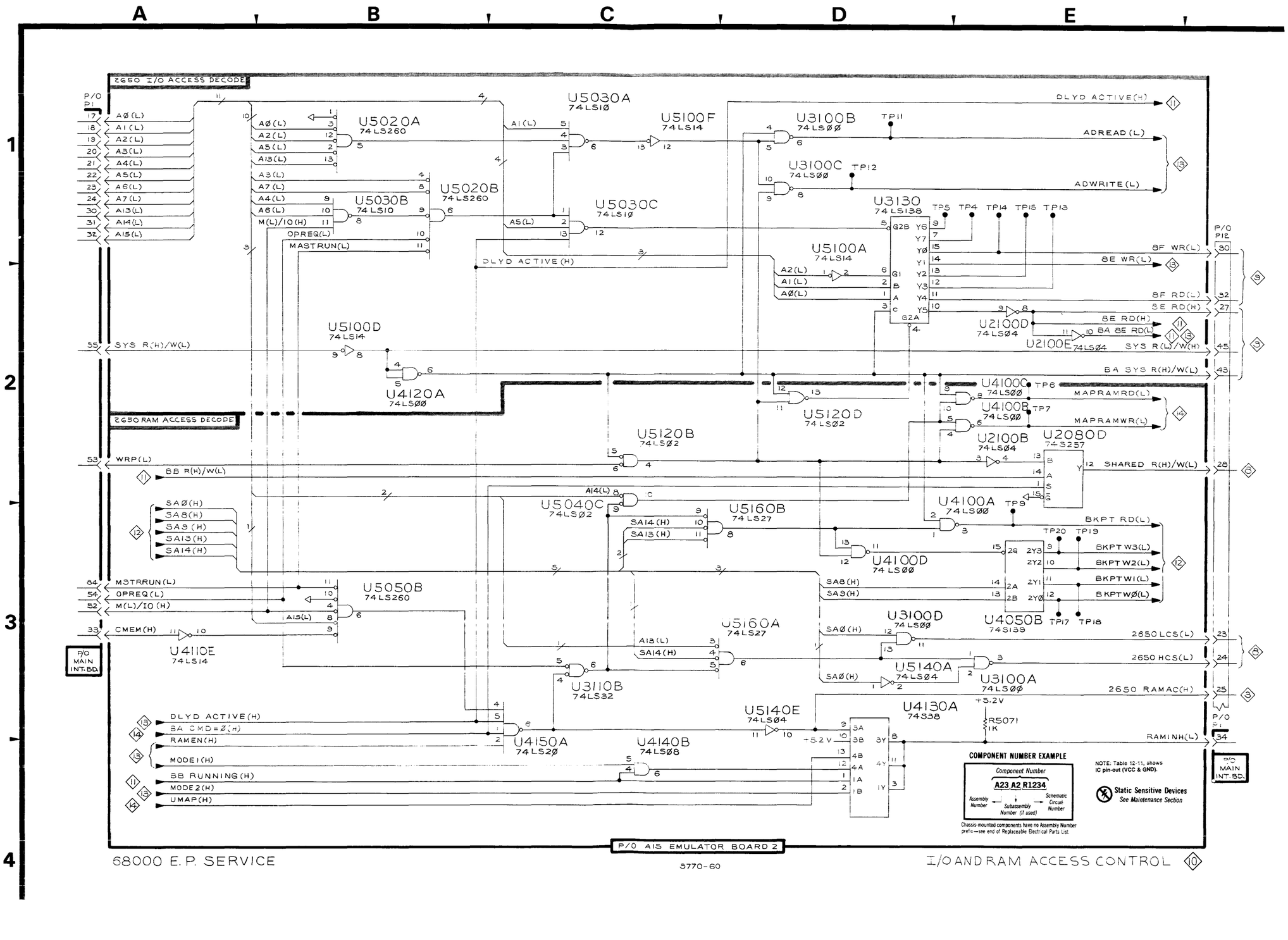

2650 I/O ACCESS DECODE
2650 RAM ACCESS DECODE
P/O P1
A0(L)
A1(L)
A2(L)
A3(L)
A4(L)
A5(L)
A6(L)
A7(L)
A13(L)
A14(L)
A15(L)
U5020A 74LS260
U5030A 74LS10
U5100F 74LS14
U5020B 74LS260
U5030B 74LS10
U5030C 74LS10
M(L)/IO(H)
OPREQ(L)
MASTRUN(L)
DLYD ACTIVE(H)
U3100B 74LS00
TP11
ADREAD(L)
U3100C 74LS00
TP12
ADWRITE(L)
U3130 74LS138
TP5 TP4 TP14 TP15 TP13
U5100A 74LS14
8F WR(L)
8E WR(L)
8F RD(L)
8E RD(L)
U2100D 74LS04
8A 8E RD(L)
U2100E 74LS04
SYS R(L)/W(H)
U5100D 74LS14
SYS R(H)/W(L)
8A SYS R(H)/W(L)
U4120A 74LS00
U5120D 74LS02
U4100C 74LS00
TP6
MAPRAMRD(L)
U4100B 74LS00
TP7
MAPRAMWR(L)
U2100B 74LS04
U2080D 74S257
SHARED R(H)/W(L)
U5120B 74LS02
WRP(L)
8B R(H)/W(L)
U4100A 74LS00
TP9
BKPT RD(L)
U5040C 74LS02
U5160B 74LS27
SA14(H)
SA13(H)
SA0(H)
SA8(H)
SA9(H)
SA13(H)
SA14(H)
U4100D 74LS00
TP20 TP19
BKPT W3(L)
BKPT W2(L)
BKPT W1(L)
BKPT W0(L)
U5050B 74LS260
MSTRRUN(L)
OPREQ(L)
M(L)/IO(H)
CMEM(H)
U4110E 74LS14
P/O MAIN INT. BD.
U5160A 74LS27
U3100D 74LS00
U4050B 74S139
TP17 TP18
2650 LCS(L)
2650 HCS(L)
2650 RAMAC(H)
U5140A 74LS04
U3100A 74LS00
U3110B 74LS32
DLYD ACTIVE(H)
8A CMD=0(H)
RAMEN(H)
MODE1(H)
8B RUNNING(H)
MODE2(H)
UMAP(H)
U4150A 74LS20
U4140B 74LS08
U5140E 74LS04
+5.2V
U4130A 74S38
R5071 1K
RAMINH(L)
P/O P12
P/O P11
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 12-11, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
P/O A15 EMULATOR BOARD 2
68000 E.P. SERVICE
I/O AND RAM ACCESS CONTROL
5770-60

Table 12-13
Aux Status Port Diagram 11

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2144	B2	K4	U2050	C2	D3
			U2060	D2	E3
P1	A1	F8	U2100C	A3	G3
P1	A2	F8	U2100F	C3	G3
P1	A4	F8	U2110A	B2	H3
P1	F3	F8	U2110D	B2	H3
P12	A1	C2	U2110E	C3	H3
P12	A3	C2	U2120B	D1	J3
P12	F1	C2	U2130B	D1	J3
P12	F4	C2	U2140A	B1	K3
P13	F2	C1	U2140B	C1	K3
			U2150A	B3	L3
R1122	A1	J2	U2150B	E3	L3
R1131	C3	J2	U3140A	D2	K4
R2041	C3	C3	U3140D	B2	K4
R2122	C3	J4	U3150B	E1	L4
R2151	B3	L3	U4120C	C3	J6
R2152	D3	L3	U4130B	E3	J6
R3151	E1	L5	U4140D	D2	K6
R4162	B3	L5	U4160	B3	L6
R5091	E3	F6	U5100C	A3	G7
R5131	D3	J6	U5100E	A2	G7
			U5130A	D3	J3
U1120C	B1	J2	U5130B	D3	J3
U1130B	C3	J2	U5140C	B1	K7
U1140B	B3	K2			

Partial A15 also shown on diagrams 10, 12, 13 and 14.

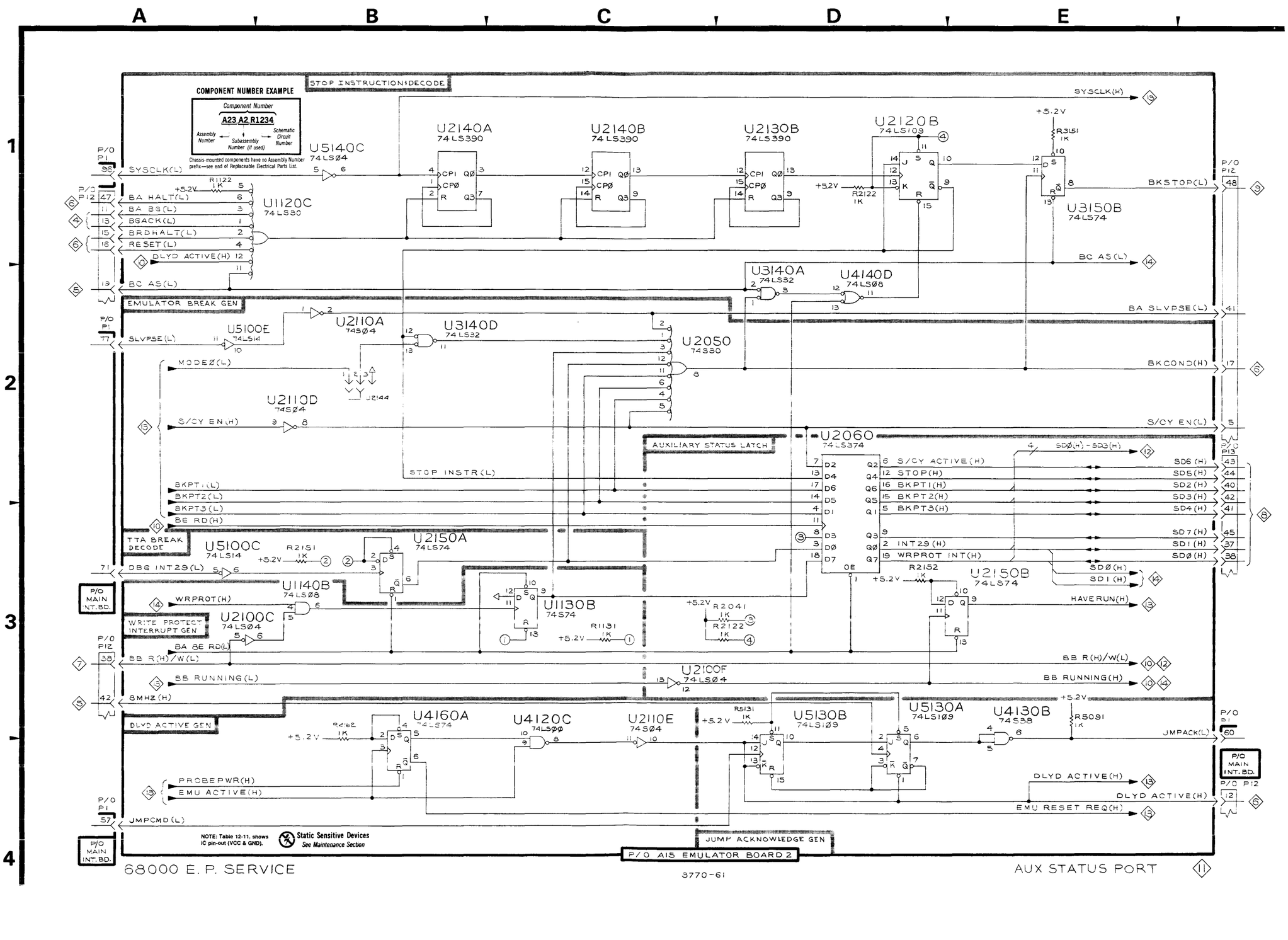

COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
STOP INSTRUCTION DECODE
SYSCLK(H)
SYSCLK(L)
U5140C 74LS04
U2140A 74LS390
U2140B 74LS390
U2130B 74LS390
U2120B 74LS109
U3150B 74LS74
+5.2V
R3151 1K
R1122 1K
R2122 1K
U1120C 74LS30
BA HALT(L)
BA BG(L)
BGACK(L)
BRDHALT(L)
RESET(L)
DLYD ACTIVE(H)
BC AS(L)
BKSTOP(L)
U3140A 74LS32
U4140D 74LS08
EMULATOR BREAK GEN
U5100E 74LS14
U2110A 74S04
U3140D 74LS32
U2050 74S30
SLVPSE(L)
BA SLVPSE(L)
MODE0(L)
BKCOND(H)
U2144
U2110D 74S04
S/CY EN(H)
S/CY EN(L)
AUXILIARY STATUS LATCH
U2060 74LS374
STOP INSTR(L)
S/CY ACTIVE(H)
STOP(H)
BKPT1(H)
BKPT2(H)
BKPT3(H)
INT29(H)
WRPROT INT(H)
SD0(H)-SD3(H)
SD6(H)
SD5(H)
SD2(H)
SD3(H)
SD4(H)
SD7(H)
SD1(H)
SD0(H)
BKPT1(L)
BKPT2(L)
BKPT3(L)
BE RD(H)
TTA BREAK DECODE
U5100C 74LS14
R2151 1K
U2150A 74LS74
DBG INT29(L)
P/O MAIN INT. BD.
U1140B 74LS08
WRPROT(H)
WRITE PROTECT INTERRUPT GEN
U2100C 74LS04
U1130B 74S74
R1131 1K
R2041 1K
R2122 1K
R2152 1K
U2150B 74LS74
HAVE RUN(H)
BA BE RD(L)
BB R(H)/W(L)
BB RUNNING(H)
8MHZ(H)
U2100F 74LS04
DLYD ACTIVE GEN
U4160A 74LS74
R2162 1K
U4120C 74LS00
U2110E 74S04
R5131 1K
U5130B 74LS109
U5130A 74LS109
U4130B 74S38
R5091 1K
JMPACK(L)
DLYD ACTIVE(H)
PROBEPWR(H)
EMU ACTIVE(H)
EMU RESET REQ(H)
JMPCMD(L)
JUMP ACKNOWLEDGE GEN
NOTE: Table 12-11, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
P/O A15 EMULATOR BOARD 2
68000 E. P. SERVICE
3770-61
AUX STATUS PORT

Table 12-14
Break Point Ram Diagram 12

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P12	A2	C2
P13	A1	C1
R1091	C1	F2
R1092	C1	F2
R1093	C1	F2
R4091	D1	G5
U1070	C3	E2
U1080	C2	F2
U1090	C1	F2
U2010	B1	B3
U2020	B3	B3
U2030	B2	C3
U2110C	B4	H3
U3050	D3	D4
U3070	D3	E4
U3080	D2	F4
U3090	D1	G4
U4070	E3	E6
U4090	E1	F6

Partial A15 also shown on diagrams 10, 11, 13 and 14.

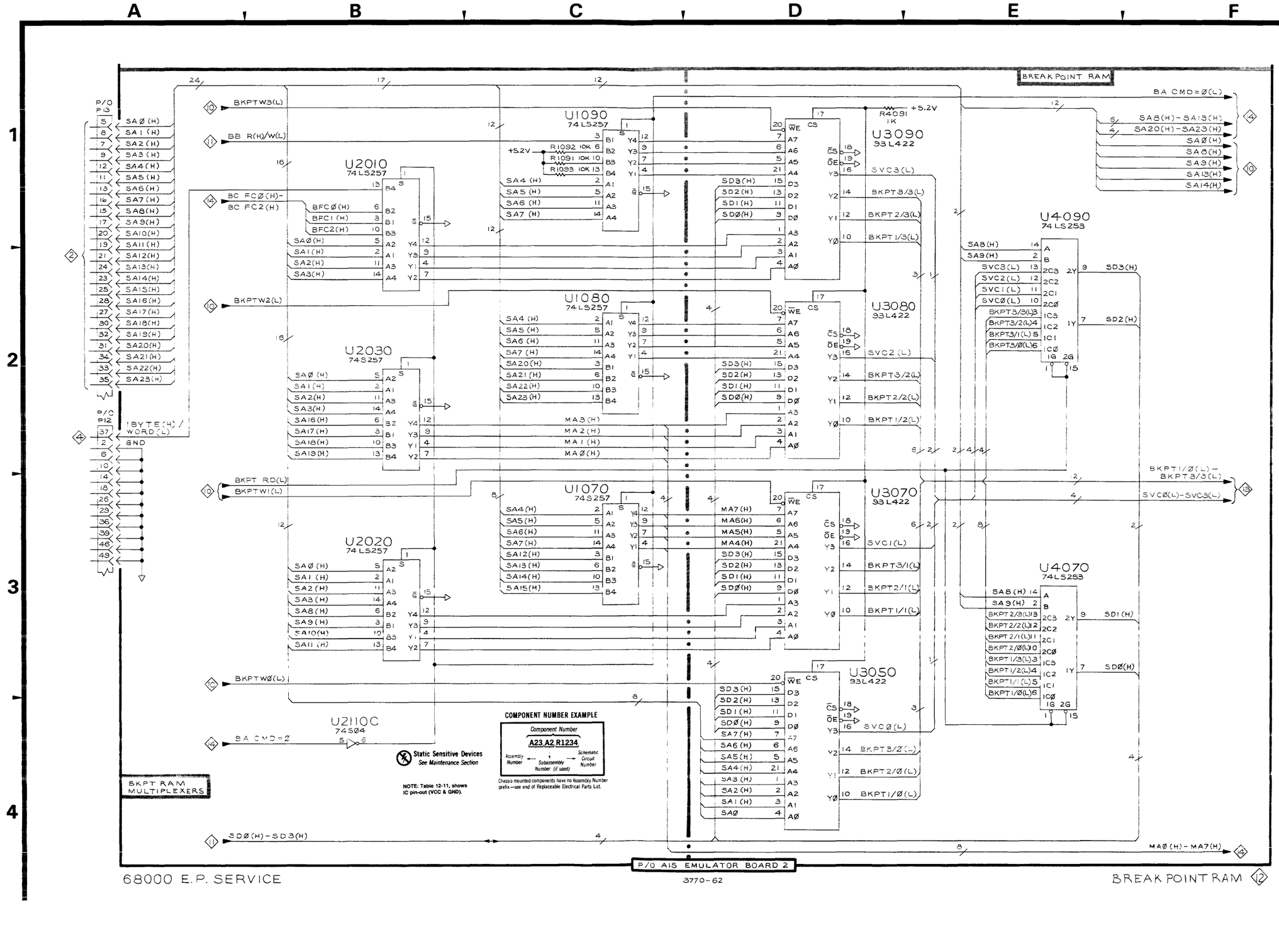

BREAK POINT RAM
BKPTW3(L)
BB R(H)/W(L)
BC FCØ(H)-BC FC2(H)
BKPTW2(L)
BKPT RD(L)
BKPTW1(L)
BKPTWØ(L)
BA CMD=2
SDØ(H)-SD3(H)
BA CMD=Ø(L)
SA8(H)-SA15(H)
SA20(H)-SA23(H)
SAØ(H)
SA8(H)
SA9(H)
SA13(H)
SA14(H)
MAØ(H)-MA7(H)
BKPT1/Ø(L)-BKPT3/3(L)
SVCØ(L)-SVC3(L)
P/O P6
P/O P12
!BYTE(H)/WORD(L)
GND
U1090 74LS257
U2010 74LS257
U1080 74LS257
U2030 74S257
U1070 74S257
U2020 74LS257
U2110C 74S04
U3090 93L422
U3080 93L422
U3070 93L422
U3050 93L422
U4090 74LS253
U4070 74LS253
R4091 1K
+5.2V
R1092 10K
R1091 10K
R1093 10K
SVC3(L)
SVC2(L)
SVC1(L)
SVCØ(L)
BKPT3/3(L)
BKPT2/3(L)
BKPT1/3(L)
BKPT3/2(L)
BKPT2/2(L)
BKPT1/2(L)
BKPT3/1(L)
BKPT2/1(L)
BKPT1/1(L)
BKPT3/Ø(L)
BKPT2/Ø(L)
BKPT1/Ø(L)
SD3(H)
SD2(H)
SD1(H)
SDØ(H)
MA3(H)
MA2(H)
MA1(H)
MAØ(H)
MA7(H)
MA6(H)
MA5(H)
MA4(H)
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Static Sensitive Devices
See Maintenance Section
NOTE: Table 12-11, shows IC pin-out (VCC & GND).
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
BKPT RAM MULTIPLEXERS
P/O AIS EMULATOR BOARD 2
3770-62
68000 E.P. SERVICE
BREAK POINT RAM

Table 12-15
EMU Status Port and Control Port Diagram

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	A3	F8	U3140B	D1	K4
P12	A1	C2	U3140C	E1	K4
P12	E2	C2	U3150A	E3	L4
P12	F3	C2	U4060A	D1	E6
P13	A3	C1	U4060B	B1	E6
P13	F2	C1	U4080A	C2	F6
			U4080B	D2	F6
R1131	D4	J2	U4110B	B3	H6
R2041	E4	C3	U4120D	C1	J6
R2122	E4	J4	U4140A	C1	K6
R2123	E1	J4	U4140C	D3	K6
R2151	D4	L3	U5040A	D2	C7
R5111	E3	H6	U5040D	D2	C7
R5151	B2	L7	U5060	B3	E7
			U5070	B3	E7
TP1	C1	K1	U5080	C4	F7
TP3	E2	L1	U5090	C3	F7
TP16	E1	L2	U5100B	D3	G7
			U5110B	E3	H7
U1130A	B2	J2	U5110C	D3	H7
U2040A	C2	C3	U5120A	E1	J7
U2110A	A2	H3	U5120C	E3	J7
U2110B	A1	H3	U5140B	D3	K7
U2120A	C1	J3	U5140D	D2	K7
U2130	B3	J3	U5140F	D2	K7
U3110D	C1	H4	U5150	B2	L7
U3120A	E1	J4	U5160C	C3	L7
U3120B	E2	J4			

Partial A15 also shown on diagrams 10, 11, 12 and 14.

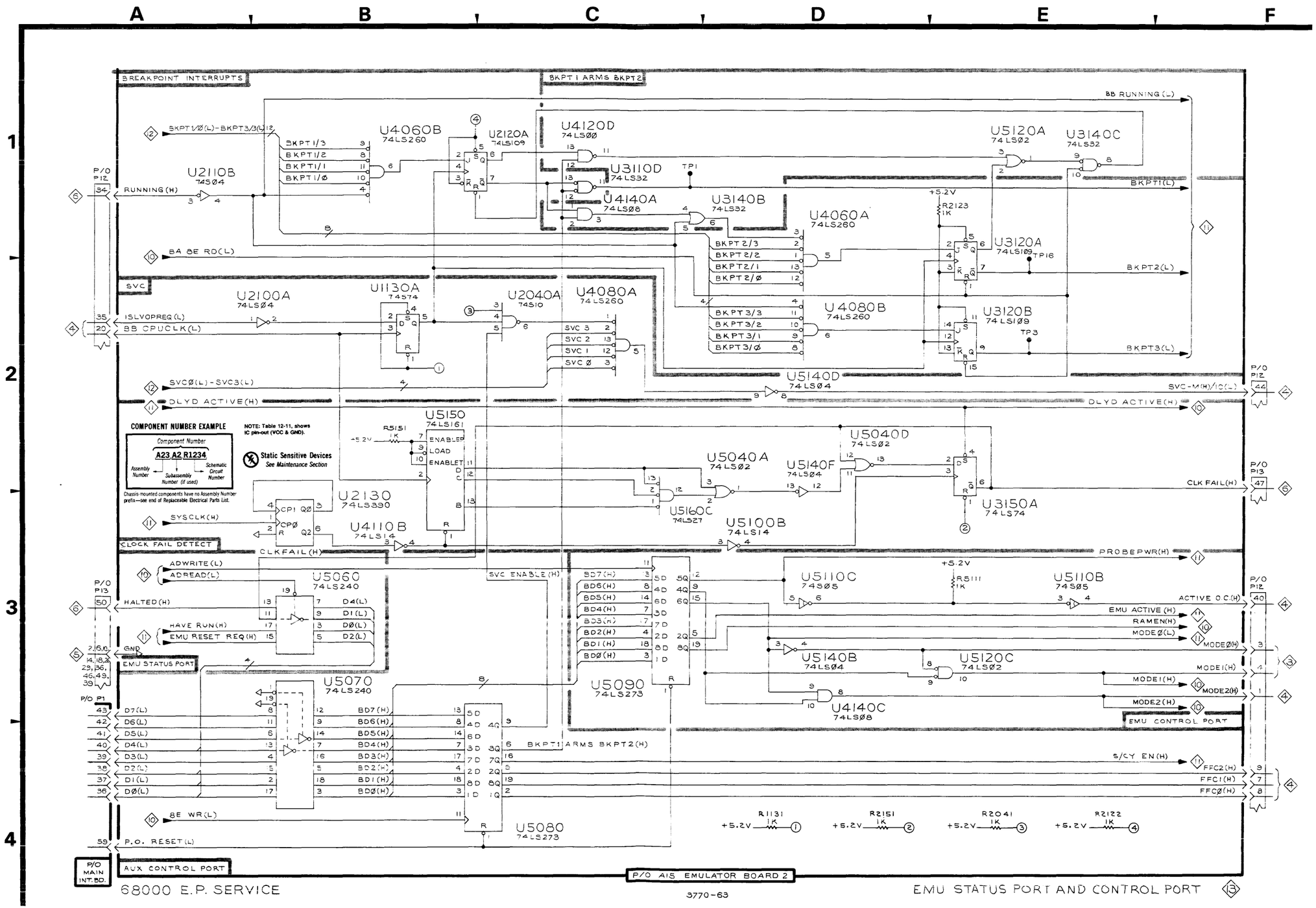
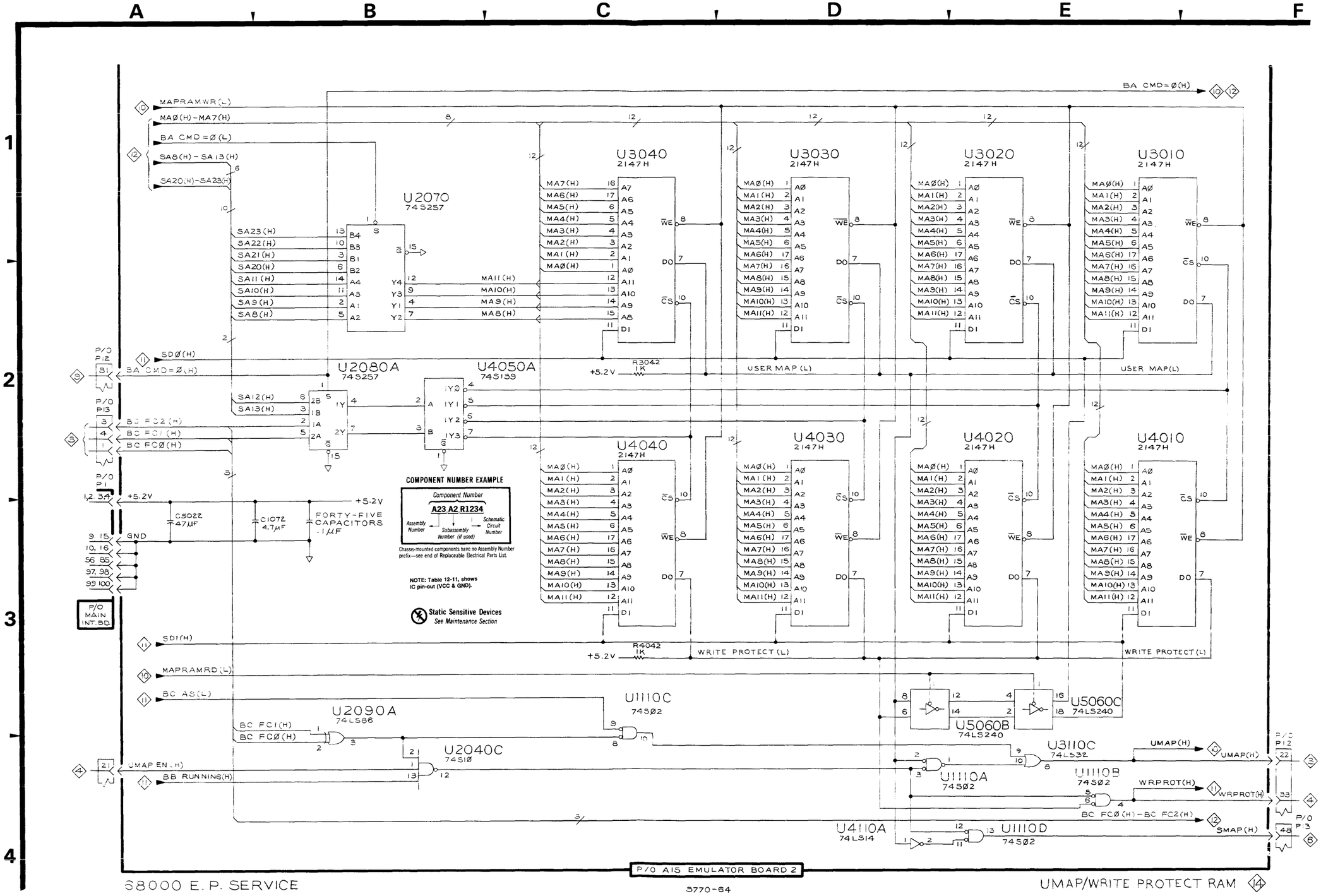

BREAKPOINT INTERRUPTS
BKPT1 ARMS BKPT2
BB RUNNING(L)
SKPT1Ø(L)-BKPT3/3(L)
BKPT1/3
BKPT1/2
BKPT1/1
BKPT1/Ø
U4060B
74LS260
U2120A
74LS109
U4120D
74LSØØ
U5120A
74LSØ2
U3140C
74LS32
U2110B
74SØ4
P/O P12
RUNNING(H)
U3110D
74LS32
TP1
U4140A
74LSØ8
U3140B
74LS32
BKPT1(L)
+5.2V
R2123
1K
U4060A
74LS260
BKPT2/3
BKPT2/2
BKPT2/1
BKPT2/Ø
U3120A
74LS109
TP16
BKPT2(L)
BA BE RD(L)
SVC
U2100A
74LS04
U1130A
74S74
U2040A
74S10
U4080A
74LS260
ISLVOPREQ(L)
BB CPUCLK(L)
SVC 3
SVC 2
SVC 1
SVC Ø
BKPT3/3
BKPT3/2
BKPT3/1
BKPT3/Ø
U4080B
74LS260
U3120B
74LS109
TP3
BKPT3(L)
SVCØ(L)-SVC3(L)
U5140D
74LS04
SVC-M(H)/IO(L)
DLYD ACTIVE(H)
U5150
74LS161
R5151
1K
ENABLEP
LOAD
ENABLET
U50040D
74LSØ2
U5040A
74LSØ2
U5140F
74LS04
U5160C
74LS27
U3150A
74LS74
CLK FAIL(H)
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 12-11, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
U2130
74LS390
SYSCLK(H)
U4110B
74LS14
U5100B
74LS14
CLOCK FAIL DETECT
CLKFAIL(H)
PROBEPWR(H)
ADWRITE(L)
ADREAD(L)
U5060
74LS240
SVC ENABLE(H)
BD7(H)
BD6(H)
BD5(H)
BD4(H)
BD3(H)
BD2(H)
BD1(H)
BDØ(H)
U5110C
74SØ5
R5111
1K
U5110B
74SØ5
ACTIVE O.C(H)
EMU ACTIVE(H)
RAMEN(H)
MODEØ(L)
MODEØ(H)
HALTED(H)
HAVE RUN(H)
EMU RESET REQ(H)
GND
EMU STATUS PORT
U5090
74LS273
U5140B
74LS04
U5120C
74LS02
MODE1(H)
MODE2(H)
U4140C
74LSØ8
EMU CONTROL PORT
D7(L)
D6(L)
D5(L)
D4(L)
D3(L)
D2(L)
D1(L)
DØ(L)
U5070
74LS240
BKPT1 ARMS BKPT2(H)
S/CY EN(H)
FFC2(H)
FFC1(H)
FFCØ(H)
8E WR(L)
U5080
74LS273
R1131
R2151
R2041
R2122
P.O. RESET(L)
P/O MAIN INT.BD.
AUX CONTROL PORT
P/O AIS EMULATOR BOARD 2
68000 E.P. SERVICE
3770-63
EMU STATUS PORT AND CONTROL PORT

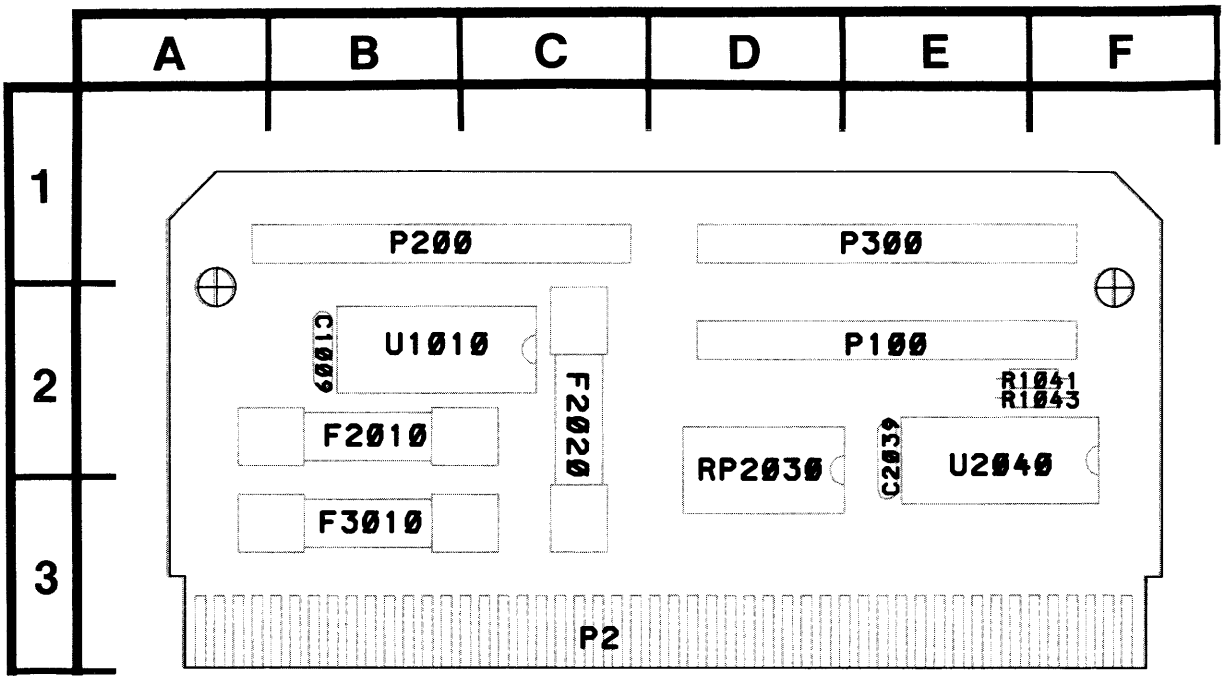
Table 12-16
UMAP/Write Protect Ram Diagram 14

ASSEMBLY A15

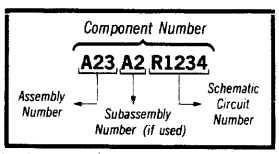
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1071	B3*	E2	C3161	B3*	L4	P13	F4	C1
C1072	A3	E2	C4011	B3*	B5			
C1081	B3*	F2	C4021	B3*	B5	R3042	C2	C5
C1101	B3*	G2	C4031	B3*	C5	R4042	C3	C6
C1111	B3*	H2	C4041	B3*	C5			
C1121	B3*	J2	C4061	B3*	E5	U1110A	D4	H2
C1141	B3*	K2	C4081	B3*	F5	U1110B	E4	H2
C2011	B3*	B3	C4101	B3*	G5	U1110C	C3	H2
C2031	B3*	C3	C4121	B3*	J5	U1110D	E4	H2
C2051	B3*	D3	C4142	B3*	K5	U2040C	B4	C3
C2091	B3*	F3	C4161	B3*	L5	U2070	B1	E3
C2102	B3*	G3	C5021	B3*	B6	U2080A	B2	F3
C2121	B3*	J3	C5022	A3	B8	U2090A	B3	F3
C2141	B3*	K3	C5041	B3*	C6	U3010	E1	B4
C2161	B3*	L3	C5072	B3*	E6	U3020	E1	B4
C3011	B3*	B4	C5092	B3*	F6	U3030	D1	C4
C3021	B3*	B4	C5101	B3*	G6	U3040	C1	C4
C3031	B3*	C4	C5112	B3*	H7	U3110C	E4	H4
C3041	B3*	C4	C5121	B3*	J6	U4010	E2	B6
C3051	B3*	D4	C5141	B3*	K6	U4020	E2	B6
C3071	B3*	E4	C5161	B3*	L6	U4030	D2	C6
C3081	B3*	F4				U4040	C2	C6
C3091	B3*	G4	P1	A2	F8	U4050A	B2	D6
C3101	B3*	G5	P12	A2	C2	U4110A	D4	H6
C3121	B3*	J4	P12	F4	C2	U5060B	E3	E7
C3141	B3*	K5	P13	A2	C1	U5060C	E3	E7

Partial A15 also shown on diagrams 10, 11, 12 and 13.


BA CMD=Ø(H)
MAPRAMWR(L)
MAØ(H)-MA7(H)
BA CMD=Ø(L)
SA8(H)-SA13(H)
SA20(H)-SA23(H)
U2070
74S257
U3040
2147H
U3030
2147H
U3020
2147H
U3010
2147H
SA23(H)
SA22(H)
SA21(H)
SA20(H)
SA11(H)
SA10(H)
SA9(H)
SA8(H)
MA11(H)
MA10(H)
MA9(H)
MA8(H)
MA7(H)
MA6(H)
MA5(H)
MA4(H)
MA3(H)
MA2(H)
MA1(H)
MAØ(H)
SDØ(H)
BA CMD=Ø(H)
U2080A
74S257
U4050A
74S139
SA12(H)
SA13(H)
BC FC2(H)
BC FC1(H)
BC FCØ(H)
P/O P12
P/O P13
P/O P11
+5.2V
C5022 47µF
C1072 4.7µF
FORTY-FIVE CAPACITORS .1µF
GND
P/O MAIN INT.BD.
R3042 1K
USER MAP(L)
U4040
2147H
U4030
2147H
U4020
2147H
U4010
2147H
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 12-11, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
SD1(H)
R4042 1K
WRITE PROTECT(L)
MAPRAMRD(L)
BC AS(L)
U1110C
74S02
U2090A
74LS86
U2040C
74S10
UMAP EN.(H)
BB RUNNING(H)
U5060C
74LS240
U5060B
74LS240
U3110C
74LS32
U1110A
74S02
U1110B
74S02
U1110D
74S02
U4110A
74LS14
UMAP(H)
WRPROT(H)
BC FCØ(H)-BC FC2(H)
SMAP(H)
P/O P12
P/O P13
P/O A15 EMULATOR BOARD 2
38000 E.P. SERVICE
3770-64
UMAP/WRITE PROTECT RAM



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-3. A20 68000 Cable Terminal Board Component Locations.

Static Sensitive Devices
See Maintenance Section

3770-45

Table 12-17
Cable Termination IC Pin Information

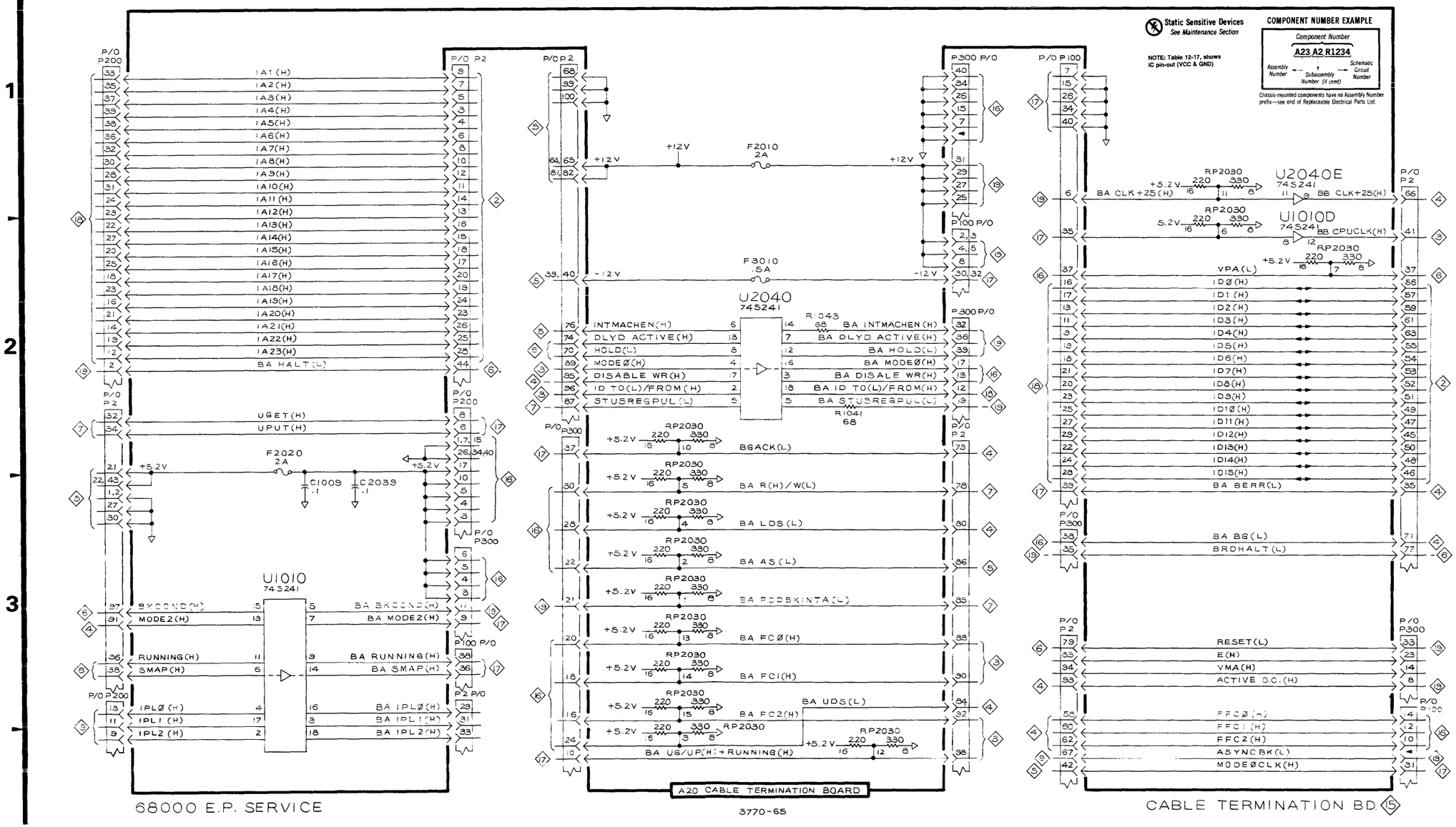
DEVICE	GND	VCC[a]
74S241	10	20

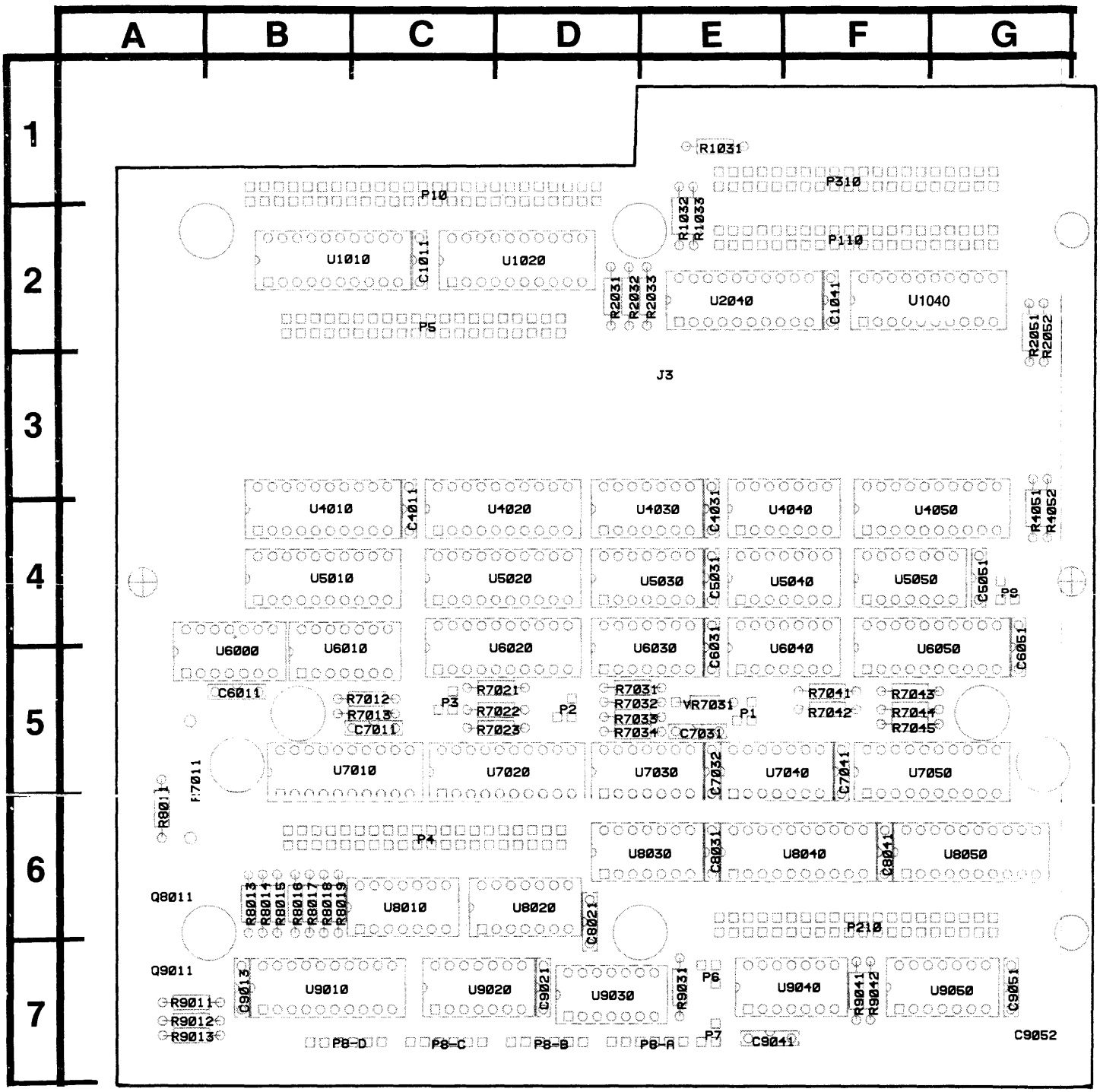
[a] **All VCC supplies are +5.2 Vdc from the development system's Main Interconnect board.**

Table 12-18
Cable Termination Bd. Diagram

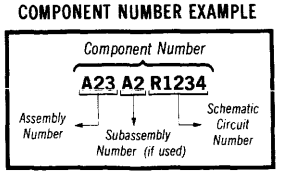
ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1009	B3	B2	P300	C2	E1
C2039	B3	E2	P300	D1	E1
			P300	D2	E1
F2010	C1	B2	P300	E3	E1
F2020	A2	C2	P300	F3	E1
F3010	C2	B3			
			R1041	D2	E2
P2	A2	C3	R1043	D2	E2
P2	B1	C3			
P2	B3	C3	RP2030	C2	D2
P2	C1	C3	RP2030	C3	D2
P2	D2	C3	RP2030	C4	D2
P2	E3	C3	RP2030	D4	D2
P2	F1	C3	RP2030	E1	D2
P100	B3	E2	RP2030	E2	D2
P100	D2	E2	RP2030	F2	D2
P100	E1	E2			
P100	F3	E2	U1010D	F2	B2
P200	A1	B1	U1010	A3	B2
P200	A3	B1	U2040E	F1	E2
P200	B2	B1	U2040	C2	E2
P300	B3	E1			


Static Sensitive Devices
See Maintenance Section
NOTE: Table 12-17, shows IC pin-out (VCC & GND)
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
68000 E.P. SERVICE
A20 CABLE TERMINATION BOARD
CABLE TERMINATION BD.
3770-65



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-4. A30 68000 Buffer Board Component Locations.

Static Sensitive Devices
See Maintenance Section

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Table 12-19
Buffer Board IC Pin Information

DEVICE	GND	VCC[a]
74S00	7	14
74S02	7	14
74S03	7	14
74S04	7	14
74S10	7	14
74LS14	7	14
74LS27	7	14
74S64	7	14
74S132	7	14
74S240	10	20
74S241	10	20
74LS245	10	20
74S260	7	14
AS804		

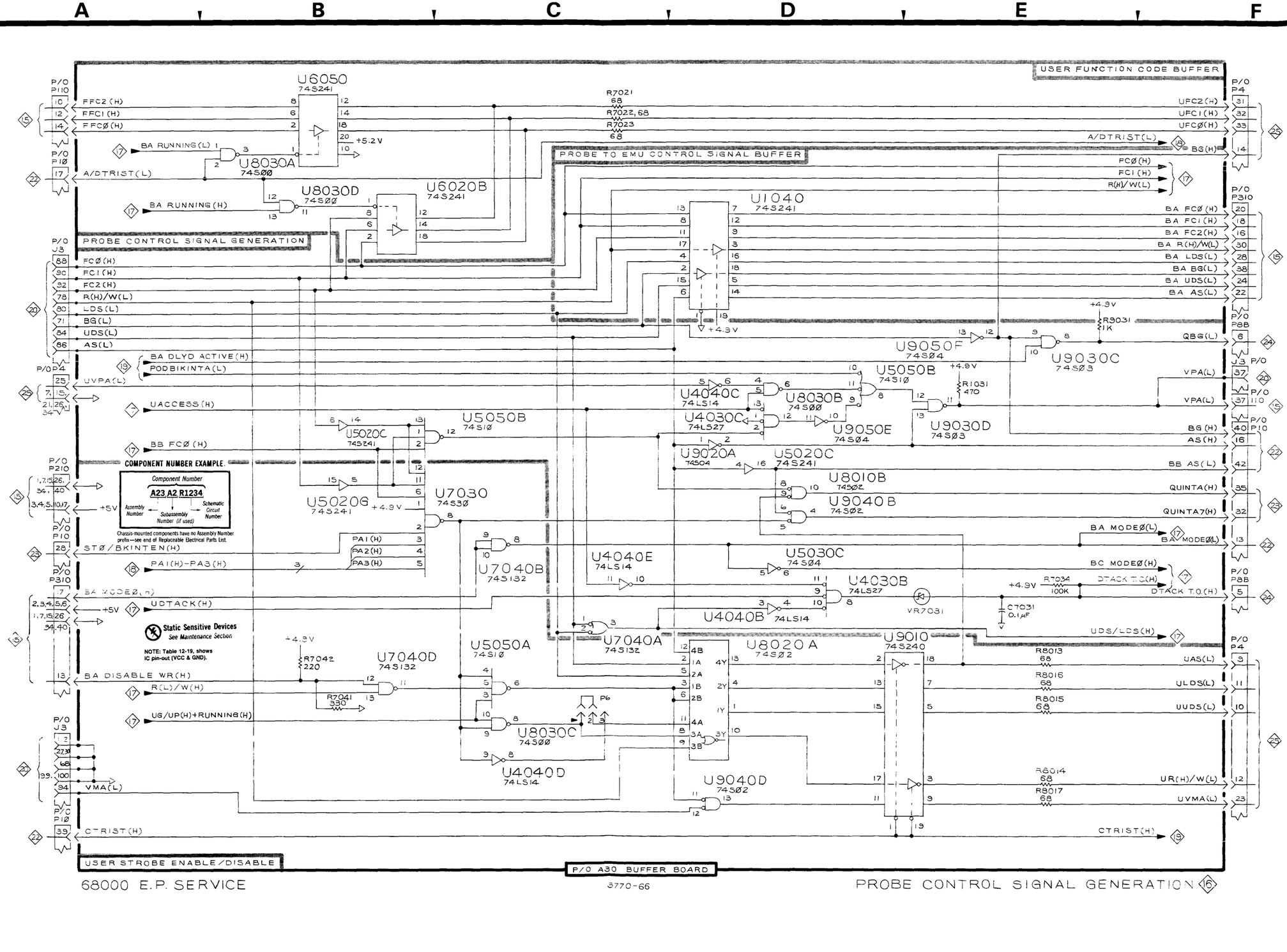
[a] **All VCC supplies are +4.9 Vdc from the 68000 Power Supply Board uniess otherwise noted.**

Table 12-20
Probe Control Signal Generation Diagram 16

ASSEMBLY A30

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C7031	E3	E5	R7022	C1	C5	U5050B	C2	F4
			R7023	C1	C5	U5050B	D2	F4
J3	A1	E3	R7034	E3	D5	U6020B	B1	D4
J3	A3	E3	R7041	B3	F5	U6050	B1	G5
J3	F2	E3	R7042	B3	F5	U7030	C2	E5
			R8013	E3	B6	U7040A	C3	E5
P4	A2	C6	R8014	E4	B6	U7040B	C3	E5
P4	F1	C6	R8015	E3	B6	U7040D	B3	E5
P4	F3	C6	R8016	E3	B6	U8010B	D2	C6
P6	C3	E7	R8017	E4	B6	U8020A	D3	D6
P8B	F2	D7	R903	E2	E7	U8030A	B1	E6
P8B	F3	D7				U8030B	D2	E6
P10	A1	C1	U1040	D1	F2	U8030C	C3	E6
P10	A3	C1	U4030B	D3	E4	U8030D	B1	E6
P10	A4	C1	U4030C	D2	E4	U9010	D3	B7
P10	F2	C1	U4040B	D3	E4	U9020A	D2	C7
P110	A1	F2	U4040C	D2	E4	U9030C	E2	D7
P110	F2	F2	U4040D	C4	E4	U9030D	E2	D7
P210	A2	F6	U4040E	C3	E4	U9040B	D3	F7
P310	A3	F1	U5020C	B2	C4	U9040D	D4	F7
P310	F1	F1	U5020C	D2	C4	U9050E	D2	G7
			U5020G	B2	C4	U9050F	E2	G7
R1031	E2	E1	U5030C	D3	E4			
R7021	C1	C5	U5050A	C3	F4	VR7031	E3	E5

Partial A30 also shown on diagrams 17, 18 and 19.



68000 E.P. SERVICE

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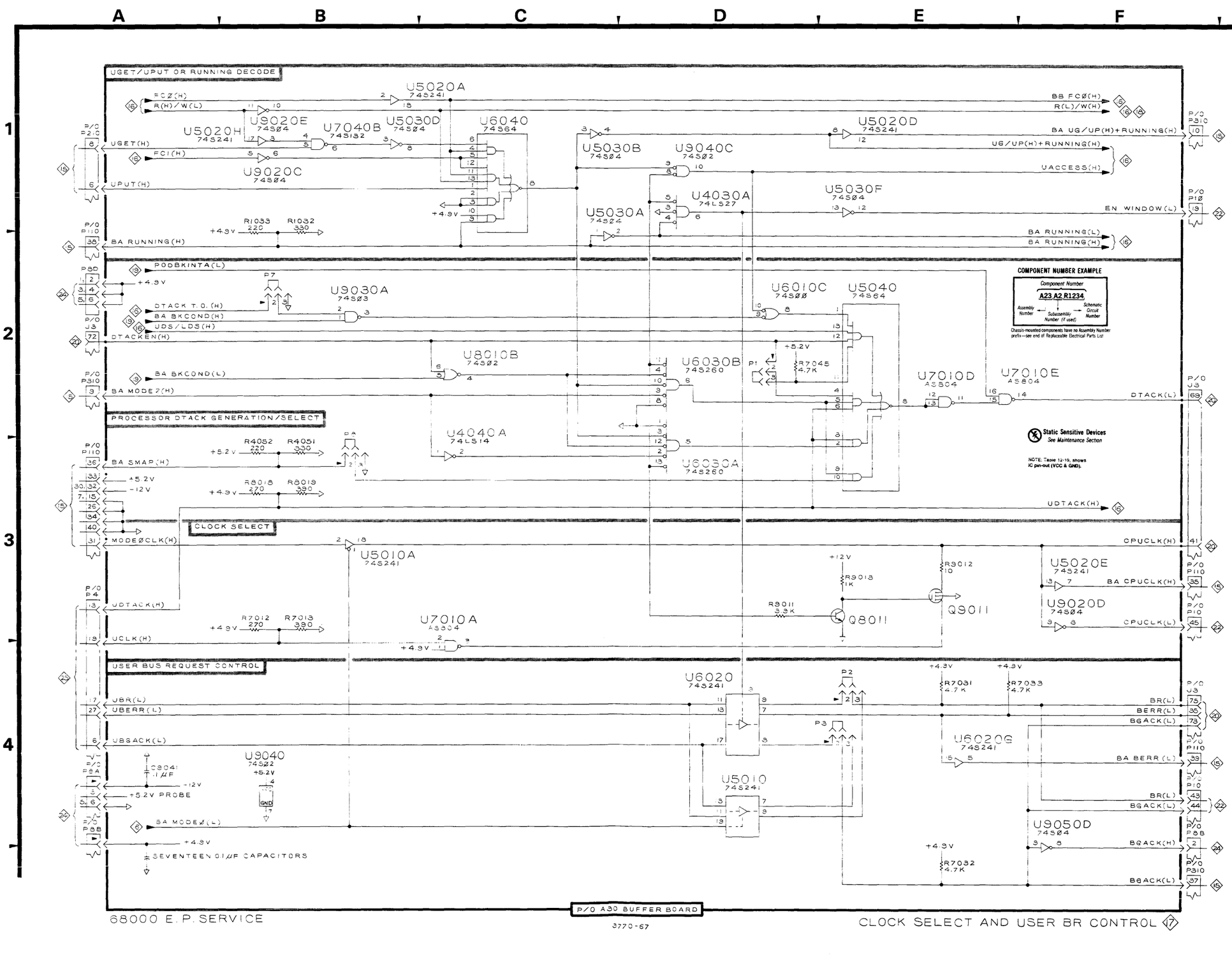
PROBE CONTROL SIGNAL GENERATION 6

Table 12-21
Clock Select and User BR Control Diagram 17

ASSEMBLY A30

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1011	A5*	C2	P10	F1	C1	U4030A	D1	E4
C1041	A5*	F2	P10	F3	C1	U4040A	C3	E4
C4011	A5*	C4	P10	F4	C1	U5010A	B3	B4
C4031	A5*	E4	P110	A2	F2	U5010	D4	B4
C5031	A5*	E4	P110	A3	F2	U5020A	B1	C4
C5051	A5*	G4	P110	F3	F2	U5020D	E1	C4
C6011	A5*	B5	P110	F4	F2	U5020E	F3	C4
C6031	A5*	E5	P210	A1	F6	U5020H	B1	C4
C6051	A5*	G5	P310	A2	F1	U5030A	C1	E4
C7011	A5*	C5	P310	F1	F1	U5030B	C1	E4
C7032	A5*	E5	P310	F5	F1	U5030D	B1	E4
C7041	A5*	F5				U5030F	E1	E4
C8021	A5*	D6	Q8011	E3	A6	U5040	E2	F4
C8031	A5*	E6	Q9011	E3	A7	U6010C	D2	B5
C8041	A5*	F6				U6020G	E4	D4
C9013	A5*	B7	R1032	B2	E2	U6020	D4	D4
C9041	A4	E7	R1033	B2	E2	U6030A	D3	D5
C9051	A5*	G7	R4051	B3	G4	U6030B	D2	D5
			R4052	B3	G4	U6040	C1	E5
J3	A2	E3	R7012	B3	C5	U7010A	C3	B5
J3	F2	E3	R7013	B3	C5	U7010D	E3	B5
J3	F4	E3	R7031	E4	D5	U7010E	E2	B5
			R7032	E5	D5	U7040B	B1	E5
P1	D2	E5	R7033	E4	D5	U8010B	C2	C6
P2	E4	D5	R7045	D2	E5	U9020C	B1	C7
P3	E4	C5	R8018	B3	B6	U9020D	F3	C7
P4	A3	C6	R8019	B3	B6	U9020E	B1	C7
P7	B2	E7	R9011	D3	A7	U9030A	B2	D7
P8A	A4	E7	R9012	E3	A7	U9040C	D1	F7
P8B	F4	D7	R9013	E3	A7	U9050D	F4	G7
P8D	A2	B7	R9041	C2	F7			
P8	B3	G4						

Partial A30 also shown on diagrams 16, 18 and 19.



68000 E.P. SERVICE

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CLOCK SELECT AND USER BR CONTROL 17

Table 12-22
Probe A/D Buffers Diagram

ASSEMBLY A30

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J3	A1	E3
P4	F1	C6
P5	F2	C2
P10	A4	C1
P110	D3	F2
P210	D1	F6
P310	A3	F1
R7043	A3	F5
R7044	A3	F5
R9042	C1	F7
U1010	E2	B2
U1020	E3	D2
U1030	B3	E2
U4010	B1	B4
U4020	B2	D4
U4050	B3	F4
U6010A	B1	B5
U7020	E1	C5
U7050	C2	F5
U8040	C2	F6
U8050	C1	G6
U9020F	E1	C7

Partial A30 also shown on diagrams 16, 17 and 19.

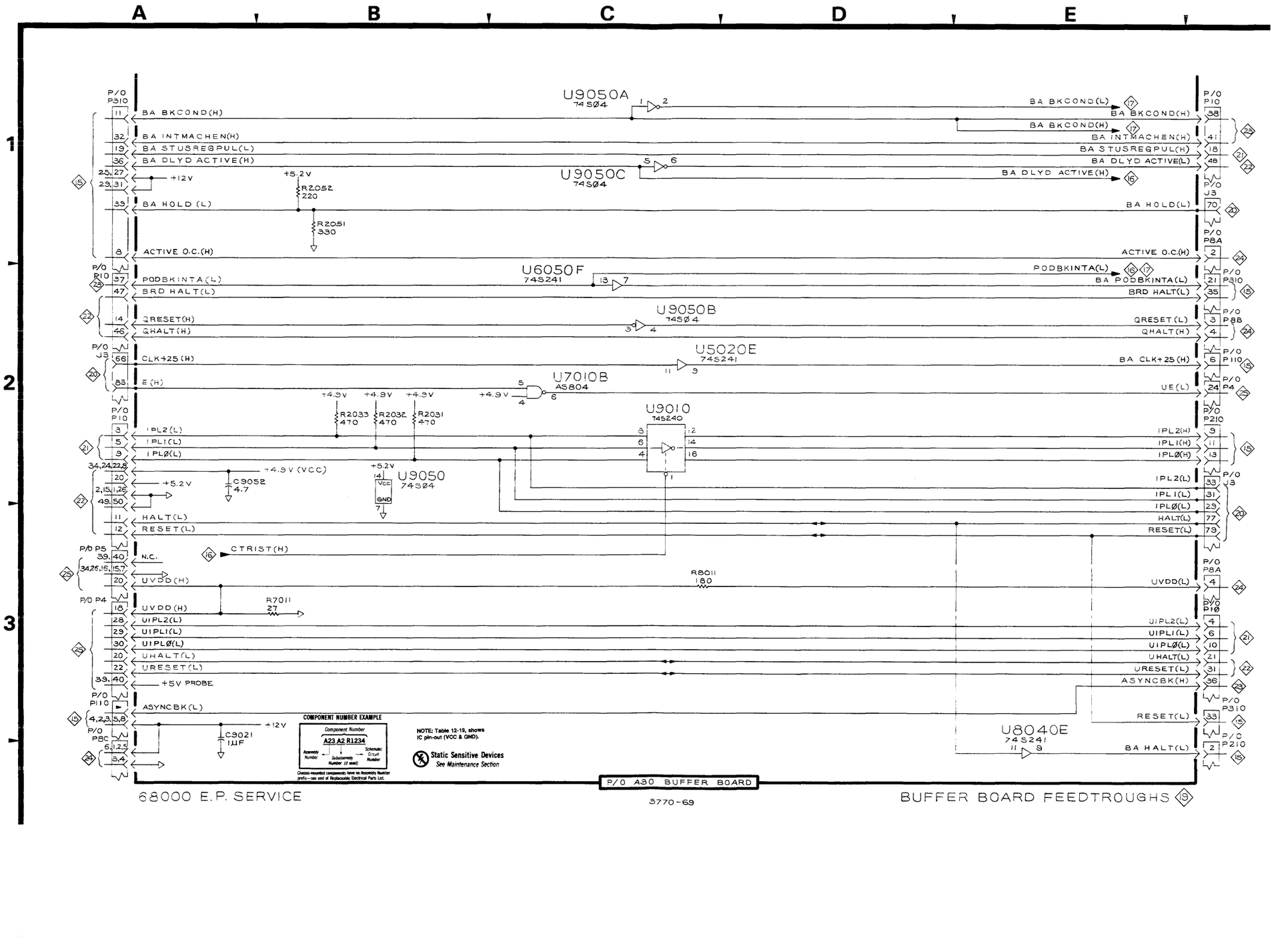
PROBE TO PROTOTYPE A/D BUFFERS
P/O P310
PA1(H)
PA2(H)
PA3(H)
PA4(H)
PA5(H)
PA6(H)
PA7(H)
PA8(H)
PA9(H)
PA10(H)
PA11(H)
PA12(H)
PA13(H)
PA14(H)
PA15(H)
PA16(H)
PA17(H)
PA18(H)
PA19(H)
PA20(H)
PA21(H)
PA22(H)
PA23(H)
PD0(H)
PD1(H)
PD2(H)
PD3(H)
PD4(H)
PD5(H)
PD6(H)
PD7(H)
PD8(H)
PD9(H)
PD10(H)
PD11(H)
PD12(H)
PD13(H)
PD14(H)
PD15(H)
A/DTRIST(L)
U6010A
74S00
R(L)/W(H)
U4010
74LS245
U4020
74LS245
68 BR/W(H)
U4050
74LS245
U1030
74LS245
BA ID TO(L) /FROM(L)
+5.2V
R7044 220
R7043 330
U8050
74S241
U7050
74S241
U8040
74S241
U4050, U7050, U8050
+5.2V
+4.9V
R9042 1K
P/O P210
P/O P110
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 12-19, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
PROBE TO EMU A/D BUFFERS
68000 E.P. SERVICE
PA1(H)-PA3(H)
U9020F
74S04
U7020
74S241
U1010
74S241
U1020
74S241
P/O P4
P/O P5
A/D TRIST(H)
A/D TRIST(L)
UD0(H)
UD1(H)
UD2(H)
UD3(H)
UD4(H)
UA1(H)
UA2(H)
UA3(H)
UA4(H)
UA5(H)
UA6(H)
UA7(H)
UA8(H)
UA9(H)
UA10(H)
UA11(H)
UA12(H)
UA13(H)
UA14(H)
UA15(H)
UA16(H)
UA17(H)
UA18(H)
UA19(H)
UA20(H)
UA21(H)
UA22(H)
UA23(H)
UD5(H)
UD6(H)
UD7(H)
UD8(H)
UD9(H)
UD10(H)
UD11(H)
UD12(H)
UD13(H)
UD14(H)
UD15(H)
P/O A30 BUFFER BOARD
3770-68
PROBE A/D BUFFERS

Table 12-23
Buffer Board Feedthroughs Diagram 

ASSEMBLY A30

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C9021	A3	D7	P310	A1	F1
C9052	A2	G7	P310	F2	F1
			P310	F3	F1
J3	A2	E3			
J3	F1	E3	R2031	B2	D2
J3	F2	E3	R2032	B2	D2
			R2033	B2	E2
P4	A3	C6	R2051	B1	G2
P4	F2	C6	R2052	B1	G2
P5	A3	C2	R7011	B3	A5
P8A	F1	C7	R8011	C3	A6
P8A	F3	C7			
P8B	F2	C7	U5020E	C2	C4
P8C	A3	C7	U6050F	C2	G5
P10	A2	C1	U7010B	C2	B5
P10	F1	C1	U8040E	E3	F6
P10	F3	C1	U9010	C2	B7
P110	A3	F2	U9050A	C1	G7
P110	F2	F2	U9050B	C2	G7
P210	F2	F6	U9050C	C1	G7
P210	F3	F6			

Partial A30 also shown on diagrams 16, 17 and 18.


A
B
C
D
E
1
2
3
U9050A
74S04
U9050C
74S04
U6050F
74S241
U9050B
74S04
U5020E
74S241
U7010B
AS804
U9010
74S240
U9050
74S04
U8040E
74S241
P/O P310
BA BKCOND(H)
BA INTMACHEN(H)
BA STUSREGPUL(L)
BA DLYD ACTIVE(H)
+12V
+5.2V
R2052 220
R2051 330
BA HOLD (L)
ACTIVE O.C.(H)
P/O P10
PODBKINTA(L)
BRD HALT(L)
QRESET(H)
QHALT(H)
P/O J8
CLK+25(H)
E(H)
+4.9V
R2033 470
R2032 470
R2031 470
IPL2(L)
IPLI(L)
IPLØ(L)
+4.9V (VCC)
C9052 4.7
+5.2V
HALT(L)
RESET(L)
P/O P5
N.C.
CTRIST(H)
UVDD(H)
P/O P4
R7011 27
UIPL2(L)
UIPLI(L)
UIPLØ(L)
UHALT(L)
URESET(L)
+5V PROBE
P/O P110
ASYNCBK(L)
P/O P8C
C9021 1µF
BA BKCOND(L)
BA BKCOND(H)
BA INTMACHEN(H)
BA STUSREGPUL(H)
BA DLYD ACTIVE(L)
BA DLYD ACTIVE(H)
BA HOLD(L)
ACTIVE O.C.(H)
PODBKINTA(L)
BA PODBKINTA(L)
BRD HALT(L)
QRESET(L)
QHALT(H)
BA CLK+25(H)
UE(L)
IPL2(H)
IPLI(H)
IPLØ(H)
IPL2(L)
IPLI(L)
IPLØ(L)
HALT(L)
RESET(L)
R8011 180
UVDD(L)
UIPL2(L)
UIPLI(L)
UIPLØ(L)
UHALT(L)
URESET(L)
ASYNCBK(H)
RESET(L)
BA HALT(L)
P/O P10
P/O P8A
P/O P310
P/O P8B
P/O P110
P/O P4
P/O P210
P/O J3
P/O P8A
P/O P10
P/O P310
P/O P210
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 12-19, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
P/O A30 BUFFER BOARD
68000 E.P. SERVICE
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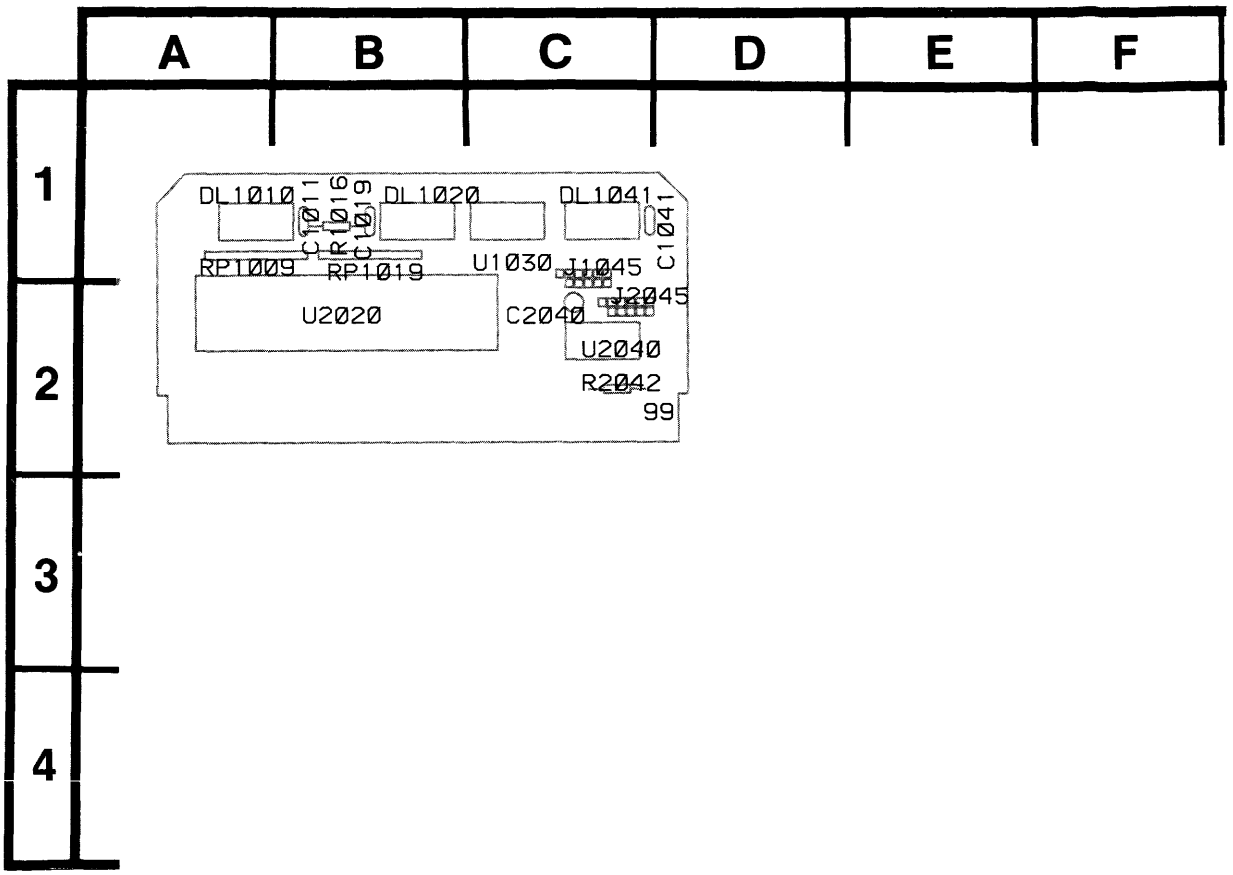
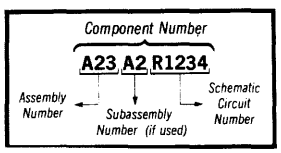
BUFFER BOARD FEEDTROUGHS



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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Fig. 12-5. A35 68000 Mobile Microprocessor Board Component Locations.

Table 12-24
Mobile μProcessor Board IC Pin Information

DEVICE	GND	VCC[a]
74LS00	7	14
74LS27	7	14

[a] **All VCC supplies are +4.9 Vdc from the 68000 Power Supply Board unless otherwise noted.**

Table 12-25
Mobile Microprocessor Bd. Diagram 20

ASSEMBLY A35

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1011	A2	B1
C1019	A2	B1
C1041	A2	C1
C2040	A2	C2
C2041	A2	D2
DL1010	A1	A1
DL1020	C1	B1
DL1040	D2	C1
J1045	C1	C1
J2045	D1	C2
P3	A1	B2
P3	E1	B2
R1016	D2	B1
R2042	D3	C2
RP1009	B1	A1
RP1019	C2	B1
U1030B	C2	C1
U1030C	C2	C1
U2020	C2	B2
U2040A	D1	C2
U2040B	D1	C2
U2040C	D1	C2

A B C D E

1 2 3

P/O P3 70 BA HOLD(L) (9)

DL1010 8

RP1009 4.7K +4.9V 9 10 5 8 7 6 4 3

U2020 MC68000-8

41	CPUCLK(H)	15	CLK
29	IPLØ(L)	25	$\overline{IPL0}$
31	IPL1(L)	24	$\overline{IPL1}$
33	IPL2(L)	23	$\overline{IPL2}$
35	BERR(L)	22	$\overline{BERR}$
73	BGACK(L)	12	$\overline{BGACK}$
75	BR(L)	13	$\overline{BR}$
37	VPA(L)	21	$\overline{VPA}$
69	DTACK(L)	10	$\overline{DTACK}$
21,22,43	+4.9V	14	VDD
		49	VDD
		16	VSS
1,2,27,30,65,99,100	GND	53	VSS

C2040 4.7µF; C1011, C1013, C1041, C2041 .1µF

9	PA1(H)	29	A1
7	PA2(H)	30	A2
5	PA3(H)	31	A3
3	PA4(H)	32	A4
4	PA5(H)	33	A5
6	PA6(H)	34	A6
8	PA7(H)	35	A7
10	PA8(H)	36	A8
12	PA9(H)	37	A9
11	PA10(H)	38	A10
14	PA11(H)	39	A11
13	PA12(H)	40	A12
16	PA13(H)	41	A13
15	PA14(H)	42	A14
18	PA15(H)	43	A15
17	PA16(H)	44	A16
20	PA17(H)	45	A17
19	PA18(H)	46	A18
24	PA19(H)	47	A19
23	PA20(H)	48	A20
26	PA21(H)	50	A21
25	PA22(H)	51	A22
28	PA23(H)	52	A23

23

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234 (Assembly Number; Subassembly Number (if used); Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: Table 12-24, shows IC pin-out (VCC & GND)

Static Sensitive Devices *See Maintenance Section*

U2040A 74LS27 (4, 5, 3, 6)

U2040C 74LS27 (2, 13, 12, 1)

U2040B 74LS27 (9, 11, 10, 8) DTACKEN(H) 72 (17)

U1045 A

DL1020

U2045 A B

DL1040

U1030C 74LSØØ (9, 10, 8)

U1030B 74LSØØ (4, 5, 6)

LDS	6	LDS(L)	80
UDS	7	UDS(L)	84
AS	6	AS(L)	86
R/W	9	R(H)/W(L)	78
FC2	26	FC2(H)	92
FC1	27	FC1(H)	90
FCØ	28	FCØ(H)	88
HALT	17	HALT(L)	77

6 3 2 4 7 10 9 8 RP1019 10K +4.9V

+4.9V R1016 2.7K

RESET	18	RESET(L)	79
E	20	E(H)	83
VMA	19	VMA(L)	94
BG	11	BG(L)	71

16

DØ	5	PDØ(H)	56
D1	4	PD1(H)	57
D2	3	PD2(H)	59
D3	2	PD3(H)	61
D4	1	PD4(H)	63
D5	64	PD5(H)	55
D6	63	PD6(H)	54
D7	62	PD7(H)	53
D8	61	PD8(H)	52
D9	60	PD9(H)	51
D10	59	PD10(H)	49
D11	58	PD11(H)	47
D12	57	PD12(H)	45
D13	56	PD13(H)	50
D14	55	PD14(H)	48
D15	54	PD15(H)	46

+4.9V R2042 4.7K

36		85	
		38	

P/O P3 CPUCLK(H) 42 (17); CLK+25(H) 66 (17, 19)

P/O A35 MOBILE MICROPROCESSOR BOARD

68000 E. P. SERVICE

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MOBILE MICROPROCESSOR BD. (20)

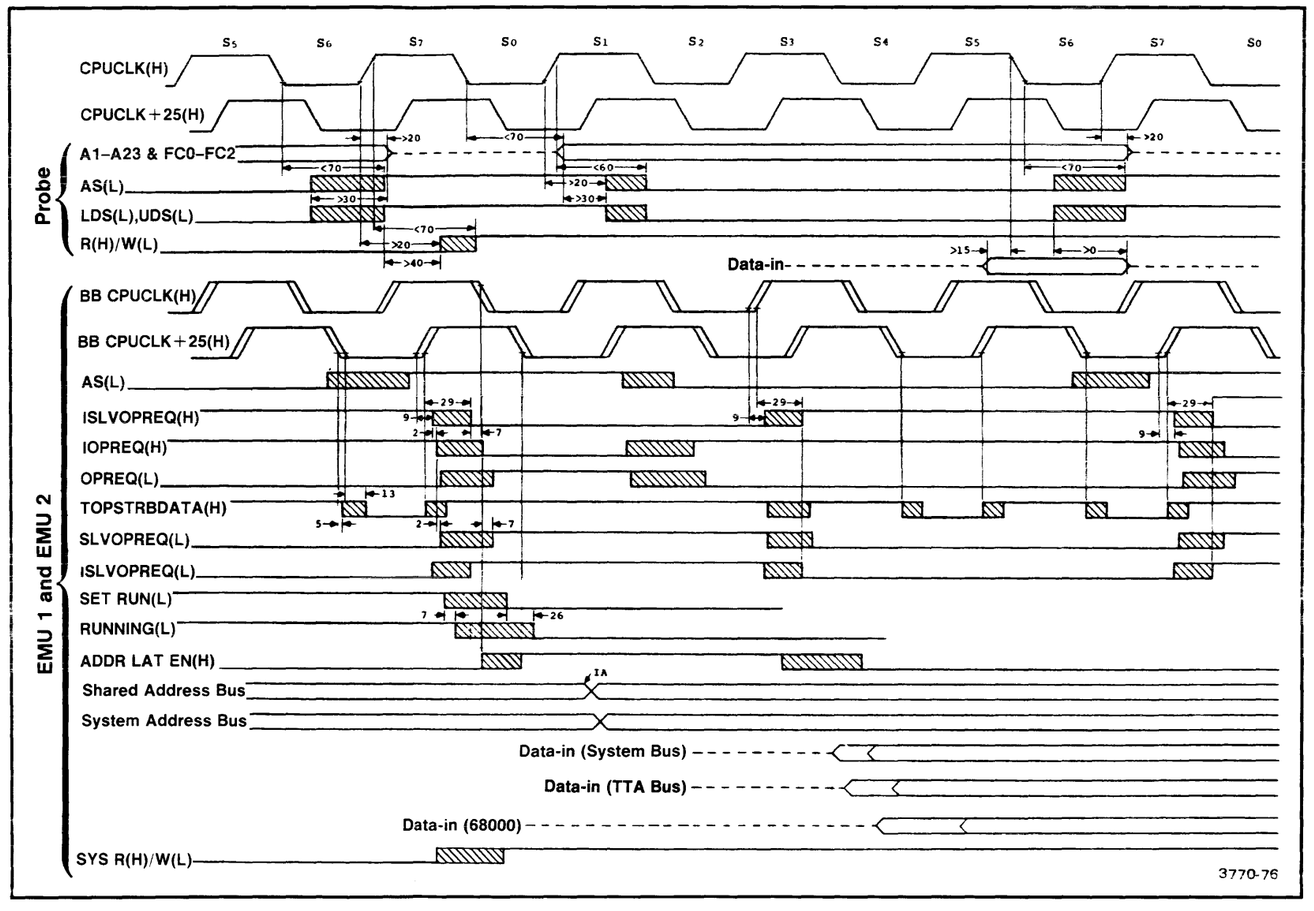


Fig. 12-8. 68000 Read cycle.

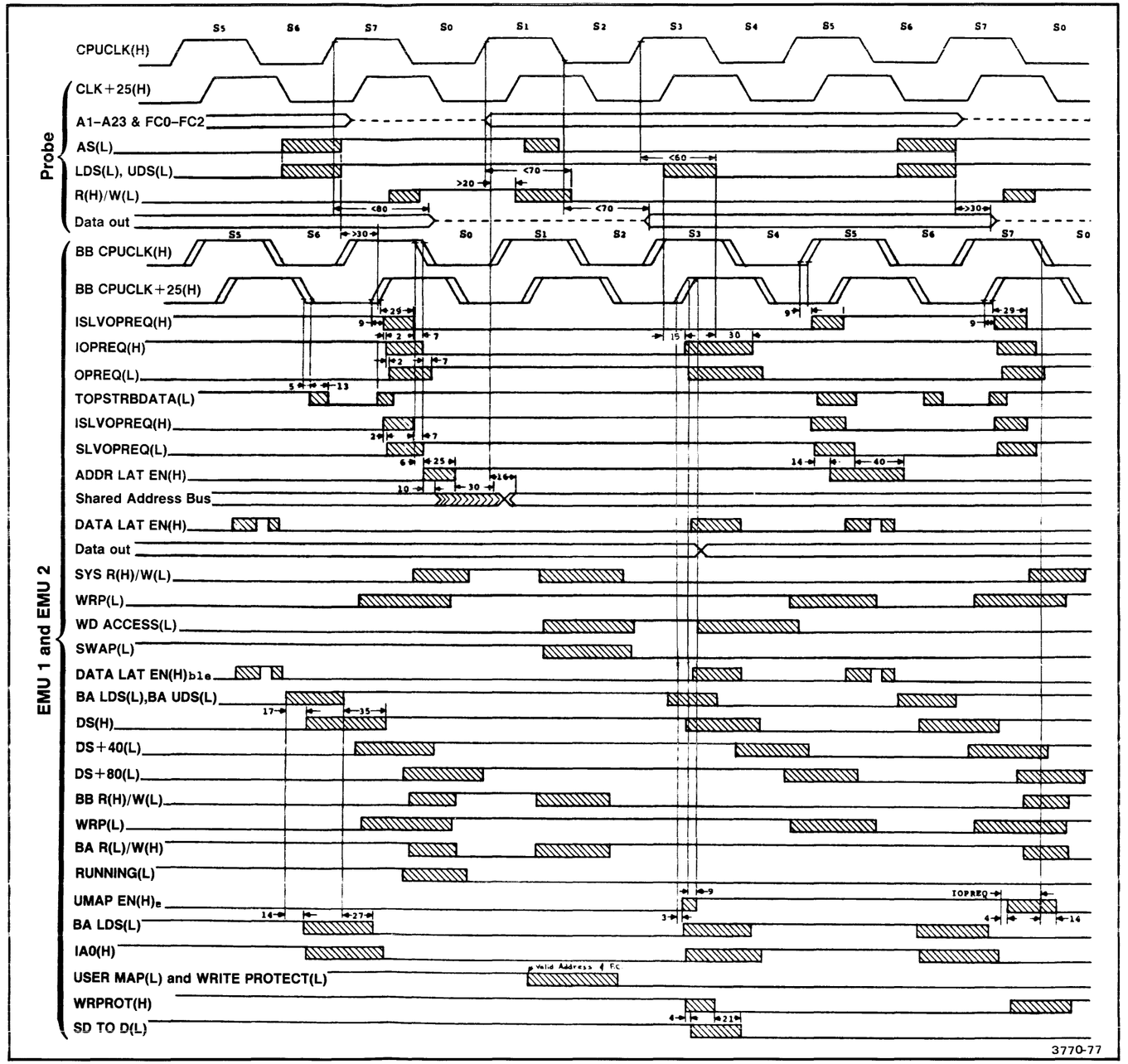
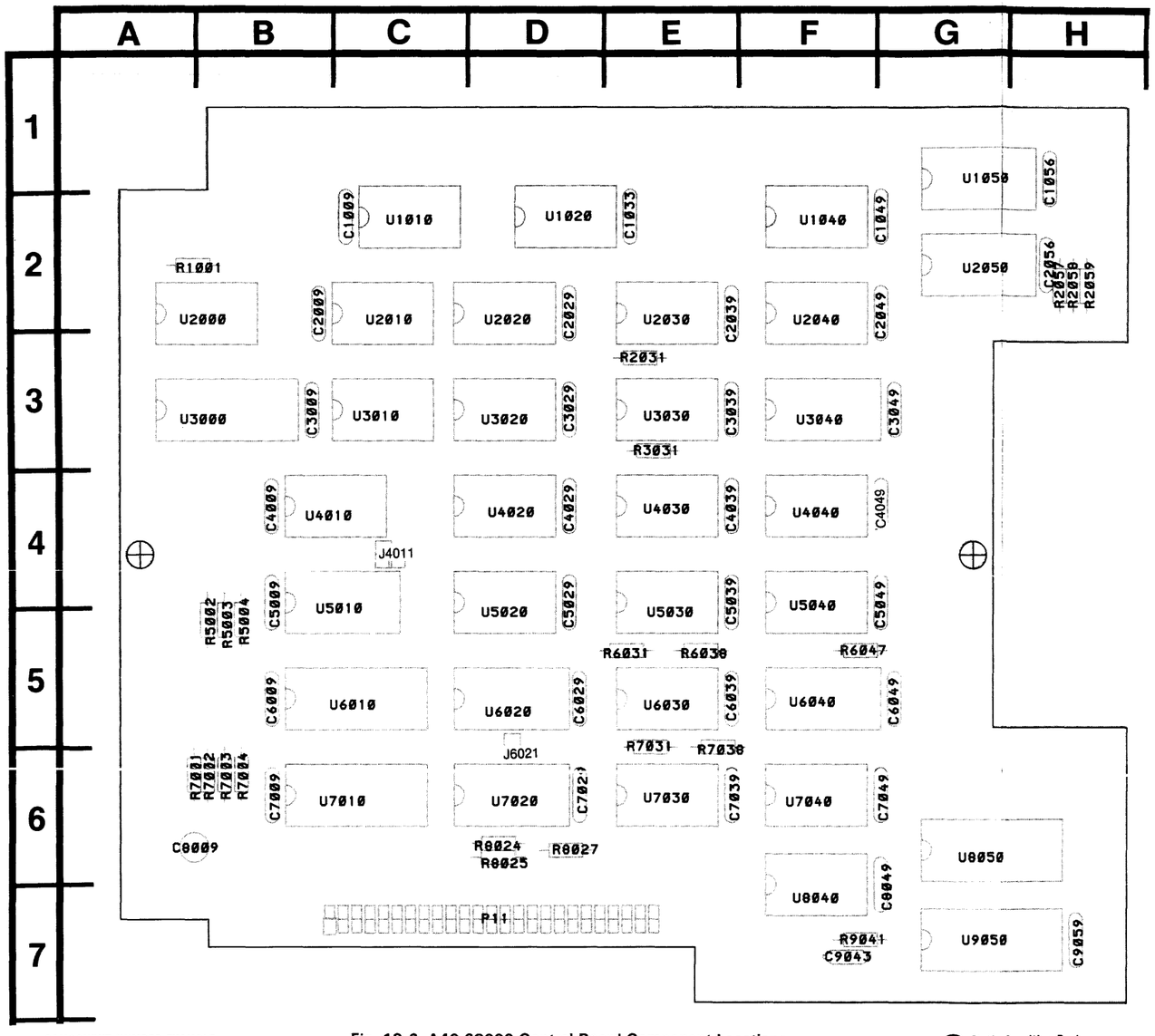
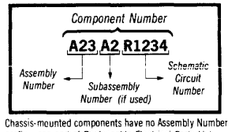


Fig. 12-9. 68000 Write cycle.



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-6. A40 68000 Control Board Component Locations.

Static Sensitive Devices
See Maintenance Section

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Table 12-26
Control Board IC Pin Information

DEVICE	GND	VCC[a]
74S00-LS	7	14
74S02-LS	7	14
74S04-LS	7	14
74LS05	7	14
74LS08	7	14
74S10-LS	7	14
74LS20	7	14
74LS27	7	14
74LS32	7	14
74S74-LS	7	14
74S85	8	16
74S112	8	16
74LS126	7	14
74LS175	8	16
74LS240	10	20
74S241	10	20
74LS279	8	16

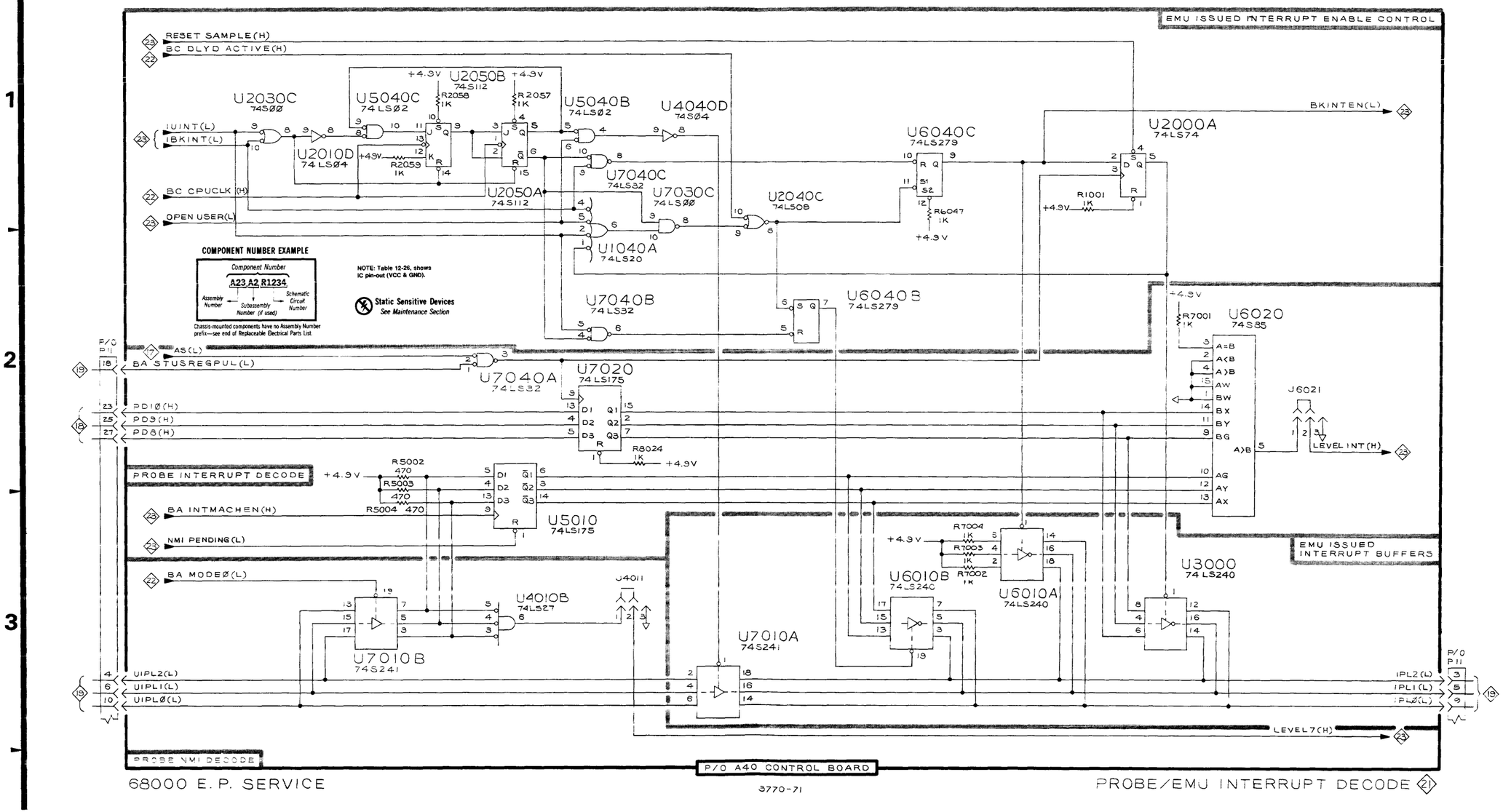
[a] **All VCC supplies are +4.9 Vdc from the 68000 Power Supply Board unless otherwise noted.**

Table 12-27
Probe/EMU Interrupt Decode Diagram

ASSEMBLY A40

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J4011	C3	C4	U2030C	A1	E2
J6021	F1	D6	U2040C	C1	F2
			U2050A	B1	G2
P11	A2	D7	U2050B	B1	G2
P11	F3	D7	U3000	E3	B3
			U4010B	B3	B4
R1001	E1	A2	U4040D	C1	F4
R2057	B1	H2	U5010	C3	C5
R2058	B1	H2	U5040B	C1	F5
R2059	B1	H2	U5040C	B1	F5
R5002	B2	B5	U6010A	D3	C5
R5003	B2	B5	U6010B	D3	C5
R6047	D1	F5	U6020	E2	D5
R7001	E2	A6	U6040B	D2	F5
R7002	D3	B6	U6040C	D1	F5
R7003	D3	B6	U7010A	C3	C6
R7004	D3	B6	U7010B	B3	C6
R8024	C2	D6	U7020	C2	D6
			U7030C	C1	E6
U1040A	C2	F2	U7040A	B2	F6
U2000A	E1	B2	U7040B	C2	F6
U2010D	B1	C2	U7040C	C1	F6

Partial A40 also shown on diagrams 22 and 23.



68000 E. P. SERVICE

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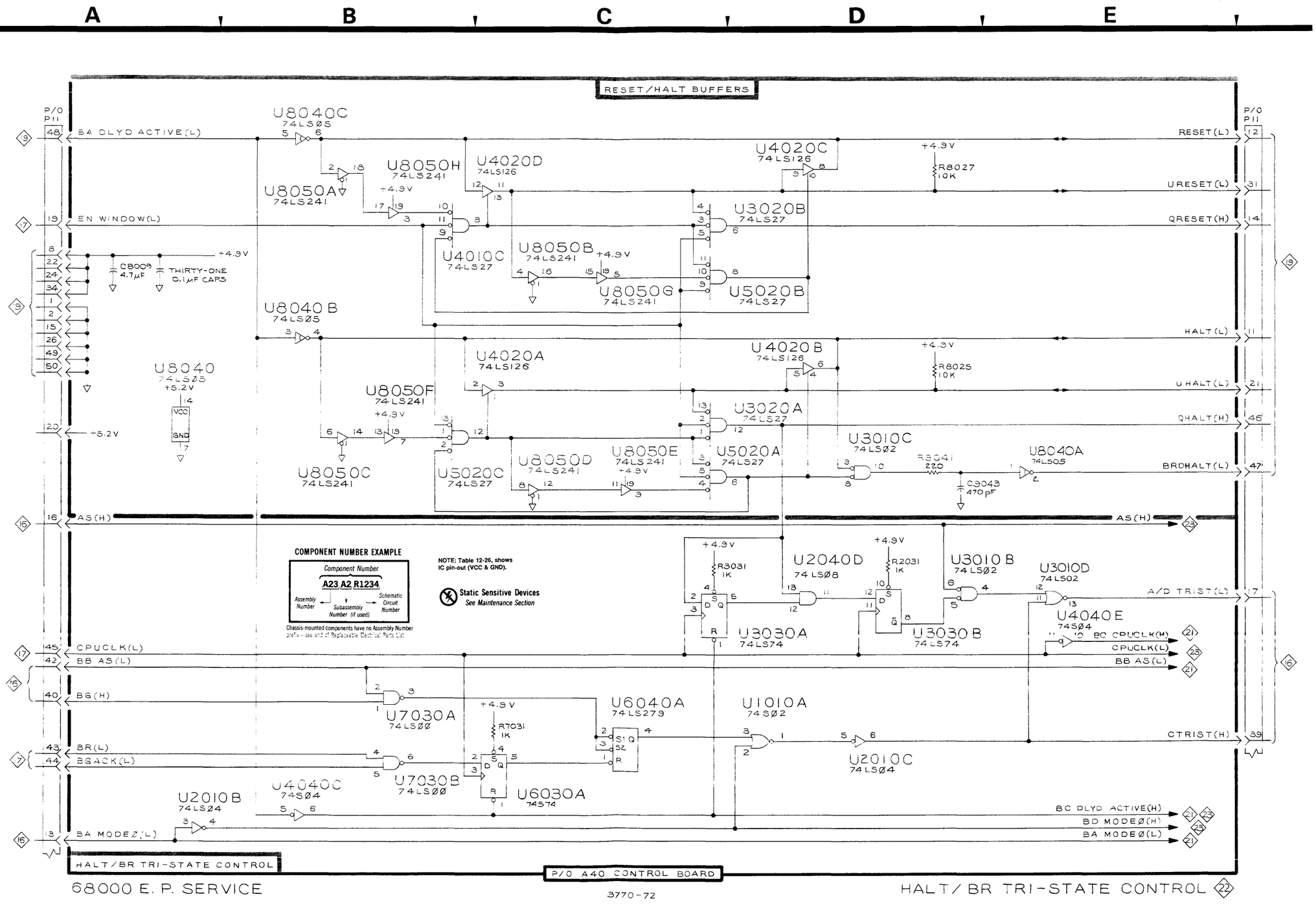
PROBE/EMU INTERRUPT DECODE 21

Table 12-28
Halt/BR Tri-state Control Diagram 

ASSEMBLY A40

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1009	A1*	C2	C7039	A1*	E6	U3030B	D3	E3
C1033	A1*	E2	C7049	A1*	F6	U4010C	B1	B4
C1049	A1*	F2	C8009	A1	A6	U4020A	C2	D4
C1056	A1*	H1	C8049	A1*	F7	U4020B	D2	D4
C2009	A1*	B2	C9043	D2	F7	U4020C	D1	D4
C2029	A1*	D2	C9059	A1*	H7	U4020D	C1	D4
C2039	A1*	E2				U4040C	B3	F4
C2049	A1*	F2	P11	A1	D7	U4040E	E3	F4
C2056	A1*	H2	P11	F1	D7	U5020A	C2	D5
C3009	A1*	B2				U5020B	C1	D5
C3029	A1*	D3	R2031	D3	E3	U5020C	B2	D5
C3039	A1*	E3	R3031	C3	E3	U6030A	C3	E5
C3049	A1*	G3	R7031	C3	E6	U6040A	C3	F5
C4009	A1*	B4	R8025	D2	D6	U7030A	B3	E6
C4029	A1*	D4	R8027	D1	D6	U7030B	B3	E6
C4039	A1*	E4	R9041	D2	F7	U8040A	E2	F7
C4049	A1*	F4				U8040B	B2	F7
C5009	A1*	B5	U1010A	D3	C2	U8040C	B1	F7
C5029	A1*	D5	U2010B	A4	C2	U8040	A2	F7
C5039	A1*	E5	U2010C	D3	C2	U8050A	B1	G6
C5049	A1*	F5	U2040D	D3	F2	U8050B	C1	G6
C6009	A1*	B5	U3010B	D3	C3	U8050C	B2	G6
C6029	A1*	D5	U3010C	D2	C3	U8050D	C2	G6
C6039	A1*	E5	U3010D	E3	C3	U8050E	C2	G6
C6049	A1*	G5	U3020A	C2	D3	U8050F	B2	G6
C7009	A1*	B6	U3020B	C1	D3	U8050G	C1	G6
C7029	A1*	D6	U3030A	D3	E3	U8050H	B1	G6

Partial A40 also shown on diagrams 21 and 23.



68000 E. P. SERVICE

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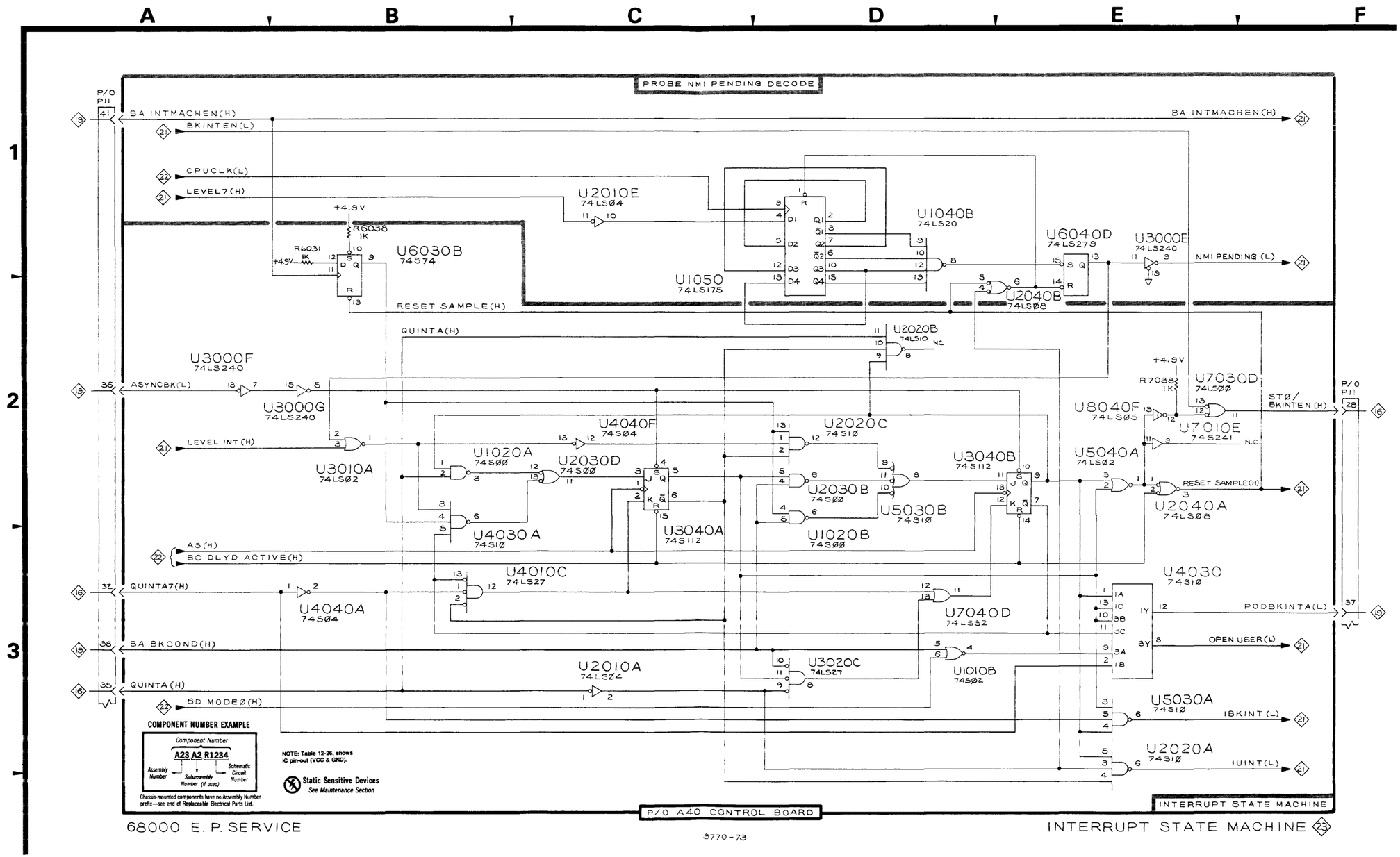
HALT/BR TRI-STATE CONTROL 22

Table 12-29
Interrupt State Machine Diagram

ASSEMBLY A40

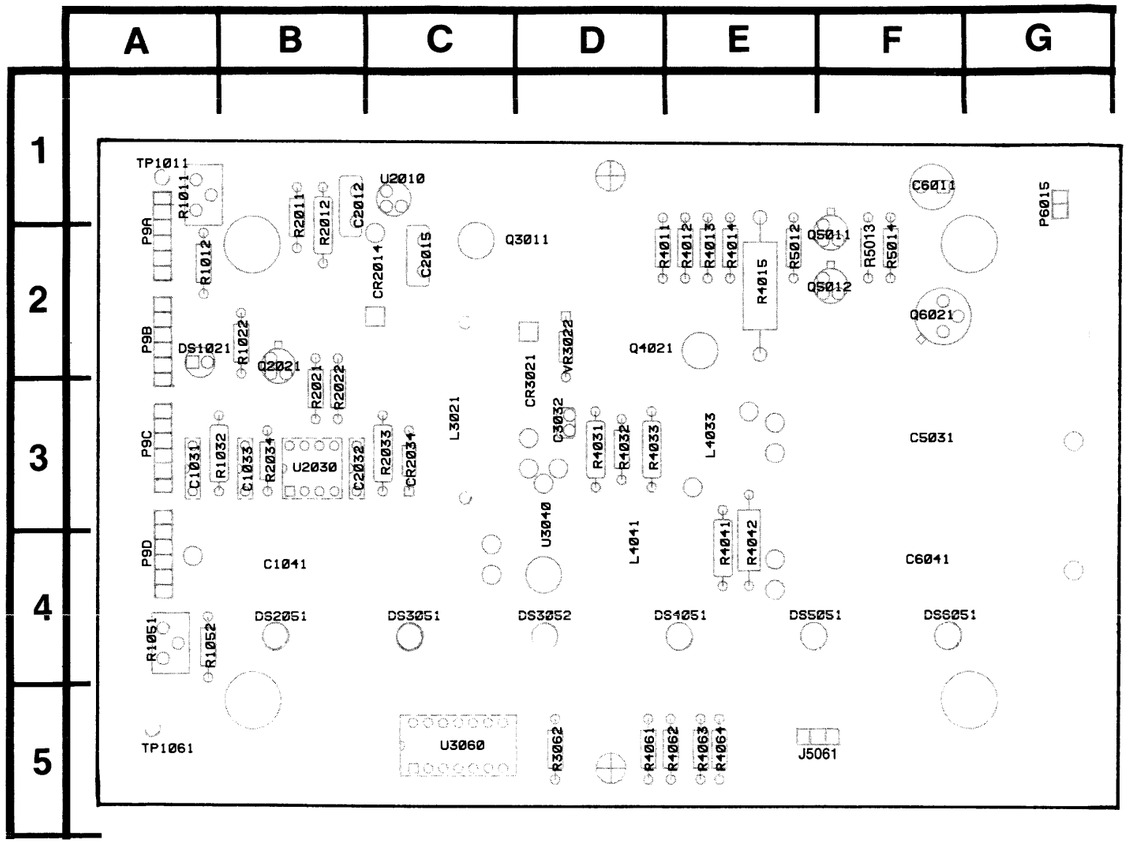
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P11	A1	D7	U3000E	E1	B3
P11	F2	D7	U3000F	A2	B3
			U3000G	B2	B3
R6031	B1	E5	U3010A	B2	C3
R6038	B1	E5	U3020C	D3	D3
R7038	E2	E6	U3040A	C2	F3
			U3040B	E2	F3
U1010B	D3	C2	U4010C	B3	B4
U1020A	B2	D2	U4030A	B3	E4
U1020B	D3	D2	U4030	E3	E4
U1040B	D1	F2	U4040A	B3	F4
U1050	D1	G1	U4040F	C2	F4
U2010A	C3	C2	U5030A	E3	E5
U2010E	C1	C2	U5030B	D2	E5
U2020A	E3	D2	U5040A	E2	F5
U2020B	D2	D2	U6030B	B1	E5
U2020C	D2	D2	U6040D	E1	F5
U2030B	D2	E2	U7010E	E2	C6
U2030D	C2	E2	U7030D	E2	E6
U2040A	E2	F2	U7040D	D3	F6
U2040B	E2	F2	U8040F	E2	F7

Partial A40 also shown on diagrams 21 and 22.

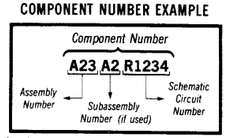


68000 E. P. SERVICE

INTERRUPT STATE MACHINE 23



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 12-7. A50 68000 Power Supply Board Component Locations.

Static Sensitive Devices
See Maintenance Section

Table 12-30
Power Supply IC Pin Information

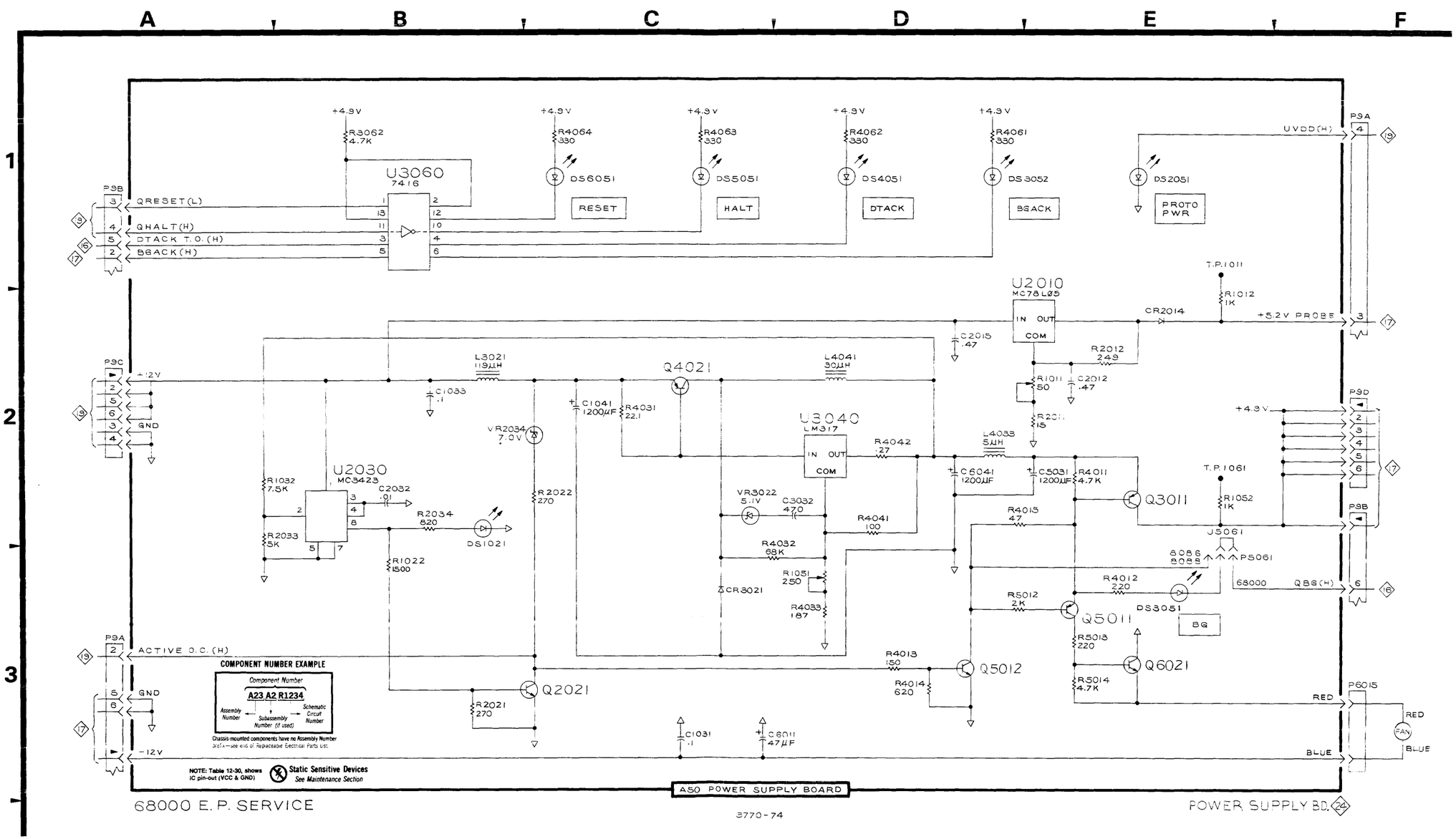
DEVICE	GND	VCC[a]
7416 MC3423	7	14

[a] **All VCC supplies are +4.9 Vdc from the Power Supply board.**

Table 12-31
Power Supply Bd. Diagram

ASSEMBLY A50

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1031	C3	A3	P9A	F1	A2	R4011	E2	D2
C1033	B2	B3	P9B	A1	A2	R4012	E3	E2
C1041	C2	B4	P9B	F2	A2	R4013	D3	E2
C2012	E2	B1	P9C	A2	A3	R4014	D3	E2
C2015	D2	C2	P9D	F2	A4	R4015	D2	E2
C2032	B2	B3	P5061	E3	G1	R4031	C2	D3
C3032	D2	D3	P6015	F3	G1	R4032	C3	D3
C5031	E2	F3				R4033	D3	D3
C6011	C3	F1	Q2021	C3	B2	R4041	D2	E4
C6041	D2	F4	Q3011	E2	C2	R4042	D2	E4
			Q4021	C2	E2	R4061	D1	D5
CR2014	E2	C2	Q5011	E3	F2	R4062	D1	E5
CR3021	C3	D2	Q5012	D3	F2	R4063	C1	E5
			Q6021	E3	F2	R4064	C1	E5
DS1021	B2	A2				R5012	D3	E2
DS2051	E1	B4	R1011	E2	A1	R5013	E3	F2
DS3051	E3	C4	R1012	E2	A2	R5014	E3	F2
DS3052	D1	D4	R1022	B3	B2			
DS4051	D1	E4	R1032	A2	A3	TP1011	E1	A1
DS5051	C1	E4	R1051	D3	A4	TP1061	E2	A5
DS6051	C1	F4	R1051	D3	A4			
			R1052	E2	A4	U2010	E2	C1
J5061	E2	F5	R2011	E2	B1	U2030	B2	B3
			R2012	E2	B1	U3040	D2	D3
L3021	B2	C3	R2021	B3	B3	U3060	B1	C5
L4033	D2	E3	R2022	C2	B3			
L4041	D2	D4	R2033	A2	C3	VR2034	B2	C3
			R2034	B2	B3	VR3022	C2	D2
P9A	A3	A2	R3062	B1	D5			



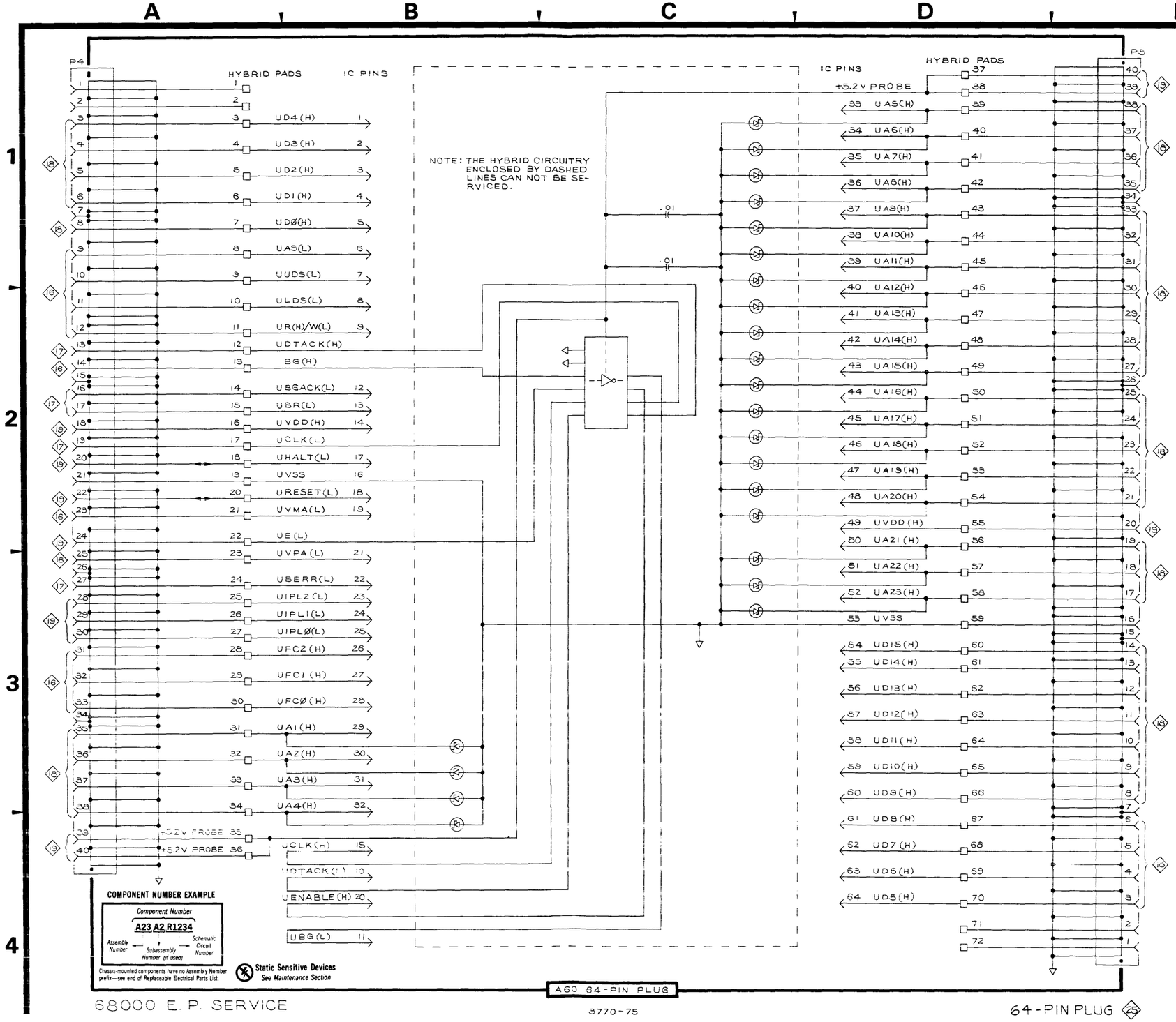
NOTE: Table 12-30, shows IC pin-out (VCC & GND)

Chassis-mounted components have no Assembly Number
Add A—see end of Replaceable Electrical Parts List.

68000 E.P. SERVICE

3770-74

POWER SUPPLY BD.


A
B
C
D
E
1
2
3
4
P4
P5
HYBRID PADS
IC PINS
NOTE: THE HYBRID CIRCUITRY ENCLOSED BY DASHED LINES CAN NOT BE SERVICED.
UD4(H) 1
UD3(H) 2
UD2(H) 3
UD1(H) 4
UDØ(H) 5
UAS(L) 6
UUDS(L) 7
ULDS(L) 8
UR(H)/W(L) 9
UDTACK(H) 12
BG(H) 13
UBGACK(L) 14
UBR(L) 15
UVDD(H) 16
UCLK(-) 17
UHALT(L) 18
UVSS 19
URESET(L) 20
UVMA(L) 21
UE(L) 22
UVPA(L) 23
UBERR(L) 24
UIPL2(L) 25
UIPL1(L) 26
UIPLØ(L) 27
UFC2(H) 28
UFC1(H) 29
UFCØ(H) 30
UA1(H) 31
UA2(H) 32
UA3(H) 33
UA4(H) 34
+5.2V PROBE 35
+5.2V PROBE 36
UCLK(-) 15
UDTACK(-) 12
UENABLE(H) 20
UBG(L) 11
.01
.01
IC PINS
HYBRID PADS
+5.2V PROBE 37 38
UA5(H) 33 39
UA6(H) 34 40
UA7(H) 35 41
UA8(H) 36 42
UA9(H) 37 43
UA10(H) 38 44
UA11(H) 39 45
UA12(H) 40 46
UA13(H) 41 47
UA14(H) 42 48
UA15(H) 43 49
UA16(H) 44 50
UA17(H) 45 51
UA18(H) 46 52
UA19(H) 47 53
UA20(H) 48 54
UVDD(H) 49 55
UA21(H) 50 56
UA22(H) 51 57
UA23(H) 52 58
UVSS 53 59
UD15(H) 54 60
UD14(H) 55 61
UD13(H) 56 62
UD12(H) 57 63
UD11(H) 58 64
UD10(H) 59 65
UD9(H) 60 66
UD8(H) 61 67
UD7(H) 62 68
UD6(H) 63 69
UD5(H) 64 70
71
72
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
A60 64-PIN PLUG
64-PIN PLUG
68000 E. P. SERVICE
3770-75

SECTION 13

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

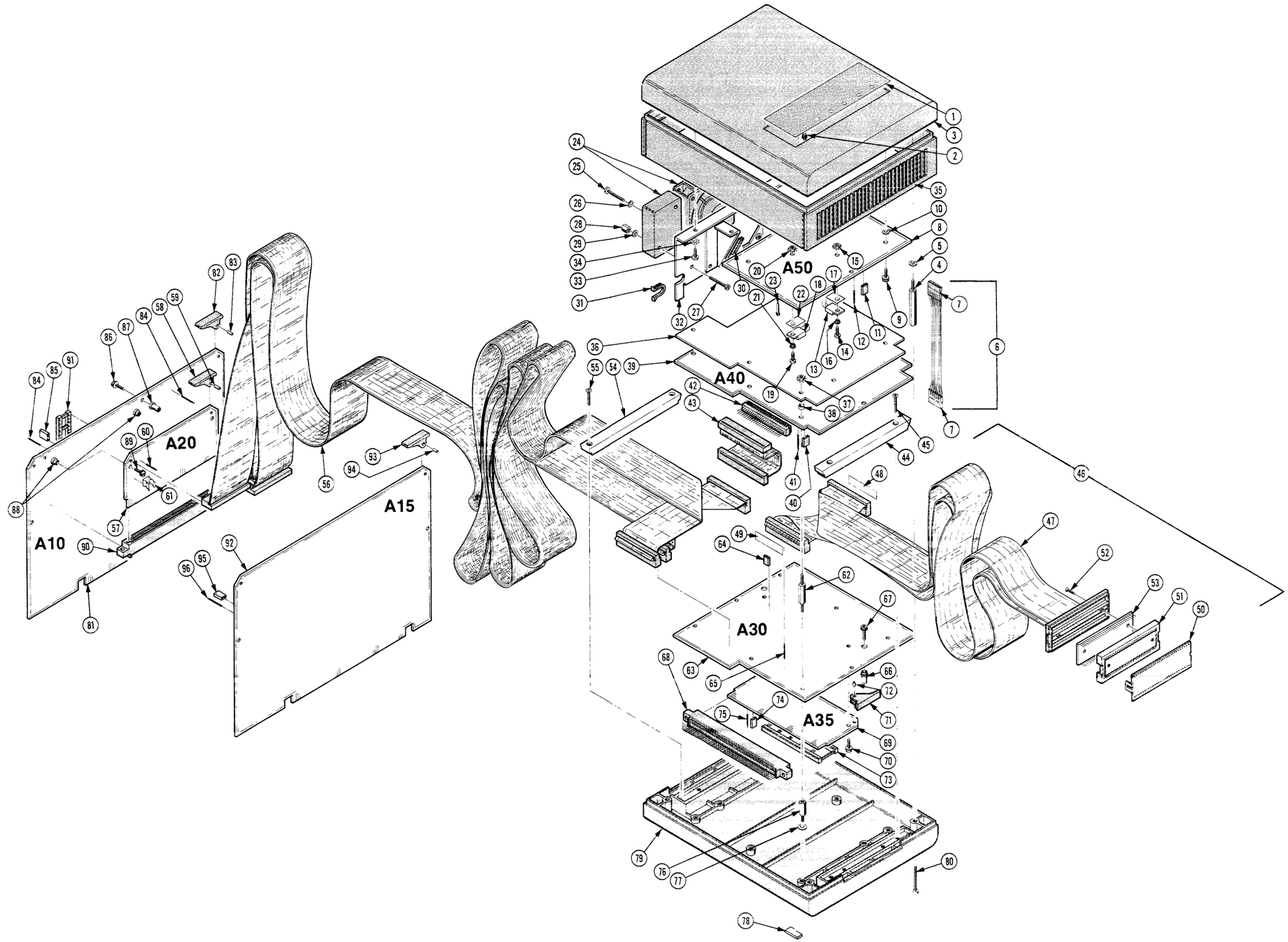
CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
000EO	ZEPHER ELECTRONIC SALES CORP.	647 INDUSTRY DRIVE	SEATTLE, WA 98188
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
06776	ROBINSON NUGENT INC.	800 E. 8TH ST., BOX 470	NEW ALBANY, IN 47150
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
31514	STANFORD APPLIED ENGINEERING, INC. ADVANCED PACKAGING DIV.	3080 AIRWAY DRIVE	COSTA MESA, CA 92626
49671	RCA CORPORATION	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
74921	ITEN FIBRE CO.,	4001 BENEFIT AVE., P O BOX 9	ASHTABULA, OH 44004
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83294	ARROW FASTENER CO., INC.	271 MAYHILL ST.	SADDLE BROOK, NJ 07662
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						8540/8550 OPTION 3U-3300P26		
1-1	334-4291-00			1		MARKER,IDENT:68000 PROTOTYPE CONTROL	80009	334-4291-00
-2	378-0602-01			6		LENS,LIGHT:AMBER	80009	378-0602-01
-3	380-0687-01			1		HSG HALF,PROBE:TOP,DRIVER/RECEIVER,PLASTIC	80009	380-0687-01
-4	129-0935-00			4		SPACER,POST:2.01 L,W/6-32INT THD ONE END	80009	129-0935-00
-5	210-1345-00			4		WASHER,FLAT:0.162 ID X 0.048 THK,STL	86928	5702-64-48-C2
-6	175-2876-00			4		CA ASSY,SP,ELEC:6,26 AWG,6.0 L	80009	175-2876-00
-7	352-0164-00			2		. CONN BODY,PL,EL:6 WIRE BLACK	80009	352-0164-00
-8	----- -----			1		CKT BOARD ASSY:POWER SUPPLY(SEE A50 REPL)		
						(ATTACHING PARTS)		
-9	211-0601-00			4		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	OBD
-10	210-0823-00			4		WASHER,FLAT:0.14 ID X 0.031 THK,RED FBR	74921	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-11	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-12	131-0608-00			29		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-13	----- -----			1		. MICROCIRCUIT,DI:(SEE A50U3040 REPL)		
						(ATTACHING PARTS)		
-14	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-15	210-0586-00			1		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-16	210-1178-00			1		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
-17	342-0322-00			1		. INSULATOR,FILM:TRANSISTOR	80009	342-0322-00
-18	----- -----			2		. TRANSISTOR:(SEE A50Q3011 & Q4021 REPL)		
						(ATTACHING PARTS)		
-19	211-0008-00			2		. SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-20	210-0586-00			2		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-21	210-1178-00			2		. WASHER,SHLDR:U/W TO-220 TRANSISTOR	49671	DF137A
						- - - * - - -		
-22	342-0322-00			2		. INSULATOR,FILM:TRANSISTOR	80009	342-0322-00
-23	----- -----			2		. TEST POINT:(SEE A50TP1010 & TP1060 REPL)		
-24	119-0830-03			1		FAN,TUBEAXIAL:12VDC,2.4W	80009	119-0830-03
						(ATTACHING PARTS)		
-25	211-0019-00			4		SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	OBD
-26	210-0004-00			4		WASHER,LOCK:#4 INTL,0.015THK,STL CD PL	000BK	OBD
-27	211-0018-00			2		SCREW,MACHINE:4-40 X 0.875 PNH,STL	83385	OBD
-28	129-0517-00			2		POST,ELEC-MECH:0.25 L X 0.25 HEX,AL	80009	129-0517-00
-29	210-0801-00			2		WASHER,FLAT:0.14 ID X 0.025 THK,BRS NI PL	12327	OBD
						- - - * - - -		
-30	252-0571-00			AR		NEOPRENE EXTR:CHAN,0.234 X 0.156	85471	DIE#1353
-31	348-0171-00			1		GROMMET,PLASTIC:U-SHAPED	80009	348-0171-00
-32	386-4740-01			1		PLATE,FAN MTG:W/BRACKET,ALUMINUM	80009	386-4740-01
						(ATTACHING PARTS)		
-33	211-0504-00			4		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-34	210-0005-00			4		WASHER,LOCK:#6 EXT,0.02 THK,STL	78189	1106-00
						- - - * - - -		
-35	361-1149-00			1		SPACER,HOUSING:	80009	361-1149-00
-36	337-2953-00			1		SHIELD,ELEC:CKT BOARD	80009	337-2953-00
						(ATTACHING PARTS)		
-37	210-0586-00			6		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-38	361-0762-00			6		SPACER,SLEEVE:0.128 ID X 0.15" L,BRASS	80009	361-0762-00
-39	----- -----			1		CKT BOARD ASSY:CONTROL(SEE A40 REPL)		
-40	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-41	131-0608-00			6		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-42	131-2221-00			1		. CONN,RCPT,ELEC:CKT BD,50 CONT,MALE	00779	2-86479-9
-43	175-3881-00			1		CA ASSY,SP,ELEC:50,28 AWG,3.75 L	000E0	2CA-08215
-44	343-1007-00			1		CLAMP,CABLE:4.9 L,ALUMINUM	80009	343-1007-00
						(ATTACHING PARTS)		
-45	211-0687-00			2		SCREW,MACHINE:6-32 X 0.75,FLH,STL,CD PL	83294	OBD
						- - - * - - -		
-46	175-4575-00			1		CA ASSY,SP,ELEC:64 PIN,19.5 L	80009	175-4575-00
	----- -----			-		(REFER TO MAINTENANCE SECTION)		
-47	175-4576-00			1		. CA ASSY,SP,ELEC:48 PIN,19.5 L	80009	175-4576-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-48	334-3281-00			1		. . MARKER,IDENT:MARKED DRIVER/RECEIVER	80009	334-3281-00
-49	334-3280-00			1		. . MARKER,IDENT:MARKED DRIVER/RECEIVER	80009	334-3280-00
-50	386-4689-00			1		. PLATE,PIN PROT:64 PIN,NYLON	80009	386-4689-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-51	204-0913-00			1		. BODY HALF,PROBE:64 PIN,BOTTOM,NYLON	80009	204-0913-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
						(ATTACHING PARTS)		
-52	211-0112-00			2		. SCREW,MACHINE:2-56 X 0.375,FLH,100 DEG	83385	OBD
						- - - * - - -		
-53	----- -----			1		. MICROCIRCUIT,DI:(SEE A60U10 REPL)		
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-54	343-1026-00			1		CLAMP,CABLE:5.33 L,ALUMINUM	80009	343-1026-00
						(ATTACHING PARTS)		
-55	211-0687-00			2		SCREW,MACHINE:6-32 X 0.75,FLH,STL,CD PL	83294	OBD
						- - - * - - -		
-56	175-4066-00			3		CA ASSY,SP,ELEC:108,33AWG,72.0 L,RIBBON	80009	175-4066-00
	334-4329-00			1		MARKER,IDENT:J100	80009	334-4329-00
	334-4330-00			1		MARKER,IDENT:J110	80009	334-4330-00
	334-4331-00			1		MARKER,IDENT:J200	80009	334-4331-00
	334-4332-00			1		MARKER,IDENT:J210	80009	334-4332-00
	334-4333-00			1		MARKER,IDENT:MRK J300	80009	334-4333-00
	334-4334-00			1		MARKER,IDENT:MRK J310	80009	334-4334-00
-57	----- -----			1		CKT BOARD ASSY:CABLE TERMINATION(SEE A20 REPL)		
-58	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-59	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-60	131-0608-00			120		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-61	344-0326-00			6		. CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-62	129-0936-00			6		SPACER,POST:1.0 L,W/6-32 EXT THD EA END	80009	129-0936-00
-63	----- -----			1		CKT BOARD ASSY:BUFFER(SEE A30 REPL)		
-64	131-0993-00			6		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-65	131-0608-00			292		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	129-0320-00			2		. POST,ELEC-MECH:0.187 OD X 0.15 INCH LONG	80009	129-0120-00
-66	129-0209-00			2		. SPACER,POST:0.375 L,W/32 THD THRU	80009	129-0209-00
						(ATTACHING PARTS)		
-67	211-0602-00			2		. SCR,ASSEM WSHR:6-32 X 0.438 INCH,PNH BRS	80009	211-0602-00
-68	131-2719-00			1		. CONN,RCPT,ELEC:EDGECARD,RTANG,2 X 50	31514	MPH7000-100R33
-69	----- -----			1		CKT BOARD ASSY:MOBILE(SEE A35 REPL)		
						(ATTACHING PARTS)		
-70	211-0116-00			2		SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-71	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-72	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-73	136-0716-00			1		. SKT,PL-IN ELEK:MICROCKT,64 CONT	06776	ICN649-S5-G30
-74	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-75	131-0608-00			22		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-76	129-0918-00			6		SPACER,POST:0.812 L,W/6-32 THD INT ONE END	80009	129-0918-00
-77	210-1345-00			6		WASHER,FLAT:0.162 ID X 0.048 THK,STL	86928	5702-64-48-C2
-78	348-0596-00			4		PAD,CAB.FOOT:0.69 X 0.255 X 0.06,PU	80009	348-0596-00
-79	380-0688-00			1		HSG HALF,PROBE:BOTTOM,DRVR/RECEIVER,PLSTC IC	80009	380-0688-00
						(ATTACHING PARTS)		
-80	211-0529-00			4		SCREW,MACHINE:6-32 X 1.25 INCHES,PNH STL	83385	OBD
						- - - * - - -		
						8540/8550 OPTION 2P-8300E26		
-81	----- -----			1		CKT BOARD ASSY:EMULATOR I(SEE A10 REPL)		
-82	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-83	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-84	131-0608-00	B010100	B010191	226		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	131-0608-00	B010192		229		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-85	131-0993-00	XB010192		1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-86	129-0209-00			2	. SPACER,POST:0.375 L,W/32 THD THRU	80009	129-0209-00
					(ATTACHING PARTS)		
-87	211-0602-00			2	. SCR,ASSEM WSHR:6-32 X 0.438 INCH,PNH BRS	80009	211-0602-00
					- - - * - - -		
-88	129-0320-00			2	. POST,ELEC-MECH:0.187 OD X 0.15 INCH LONG	80009	129-0120-00
-89	211-0116-00			2	. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
-90	131-2719-00			1	. CONN,RCPT,ELEC:EDGECARD,RTANG,2 X 50	31514	MPH7000-100R33
-91	136-0751-00			3	. SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
	253-0176-00			1	. TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	OBD
-92	----- -----			1	CKT BOARD ASSY:EMULATOR II(SEE A15 REPL)		
-93	105-0792-00			2	. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-94	214-1337-00			2	. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-95	131-0993-00			1	. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-96	131-0608-00			123	. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357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A30
A35

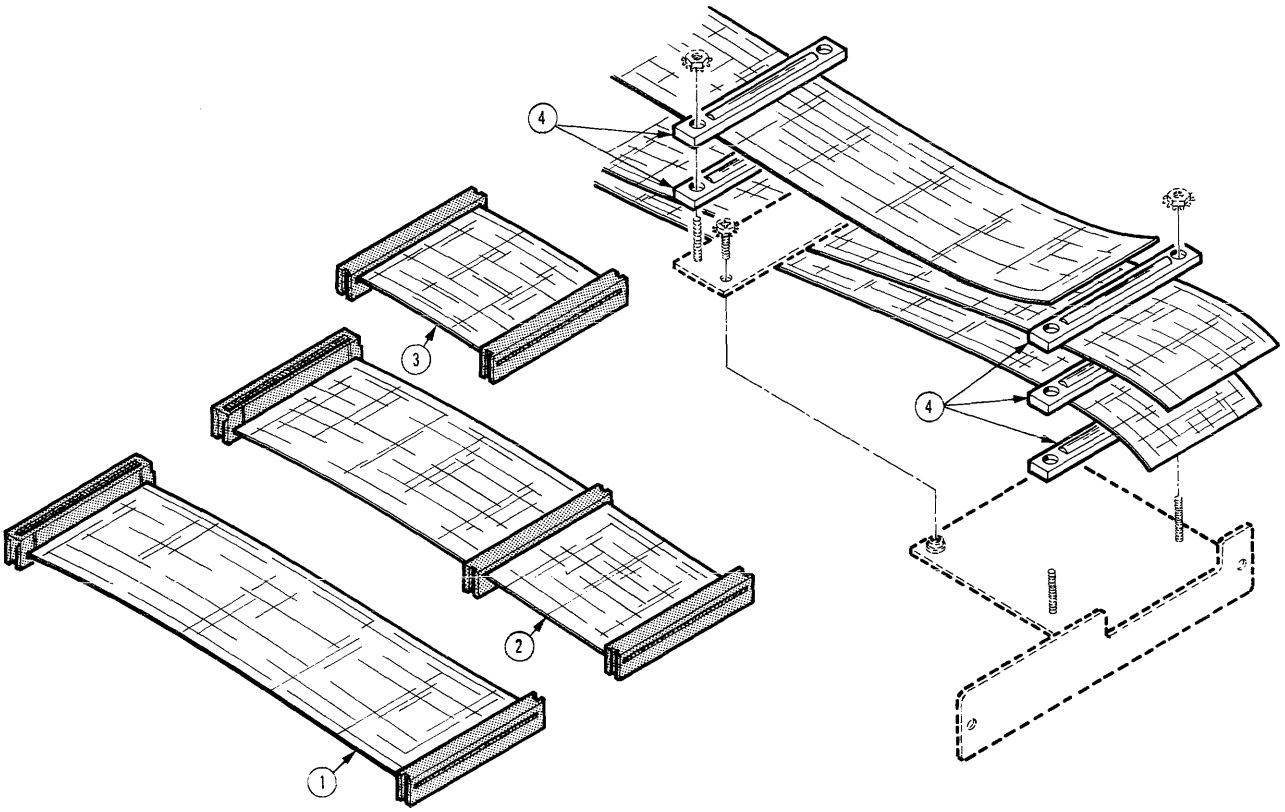

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
2-1	175-3882-00			1		CA ASSY,SP,ELEC:50,28 AWG,8.0L	000EO	2CA-08218
	----- -----			-		(8540/8550 OPTION 2P/8300E26 ONLY)		
-2	175-3883-00			1		CA ASSY,SP,ELEC:50,28 AWG,9.0L	000EO	OBD
	----- -----			-		(8540/8550 OPTION 2P/8300E26 ONLY)		
-3	175-6671-00			2		CA ASSY,SP,ELEC:50,28 AWG,10.0 L RIBBON	80009	175-6671-00
	----- -----			-		(8550 OPTION 2P/8300E26 ONLY)		
	175-3881-00			1		CA ASSY,SP,ELEC:50,28 AWG,3.75 L	000EO	2CA-08215
	----- -----			-		(8540 OPTION 2P ONLY)		
	062-5956-00			1		SOFTWARE PKG:DBL SIDED FLOPPY DISC	80009	062-5956-00
	----- -----			-		(8550 OPTION 3U/8300P26/P26 OPT 01 ONLY)		
	070-2552-00			1		CARD,INFO:DISC HANDLING	80009	070-2552-00
	----- -----			-		(8550 OPTION 3U/8300P26 ONLY)		
	070-3771-00			1		MANUAL,TECH:INSTALLATION	80009	070-3771-00
	----- -----			-		(8540/8550 OPTION 3U/8300P26 ONLY)		
	070-3969-00			1		MANUAL,TECH:USERS	80009	070-3969-00
	----- -----			-		(8550 OPT 3U ONLY)		
	070-3970-00			1		MANUAL,TECH:USERS	80009	070-3970-00
	----- -----			-		(8540 OPTION 3U/8300P26 ONLY)		
-4	343-1011-00			5		CLAMP,CABLE:2.95 L	80009	343-1011-00
	----- -----			-		(8540/8550 OPTION 3U-8300P26 ONLY)		
	160-1353-00			1		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1353-00
	----- -----			-		(8540 OPT 3U-8300 P26 OPT 01)		
	160-1364-00			1		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1364-00
	----- -----			-		(8540 OPT 3U-8300 P26 OPT 01)		
	160-1399-00			1		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1399-00
	----- -----			-		(8540 OPT 3U-8300 P26 OPT 01)		
	160-1400-00			1		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1400-00
	----- -----			-		(8540 OPT 3U-8300 P26 OPT 01)		
	160-1606-00			1		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1606-00
	----- -----			-		(8540 OPT 3U-8300 P26 OPT 01)		
						OPTIONAL ACCESSORIES		
	070-3770-00			1		MANUAL,TECH:SERVICE	80009	070-3770-00

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MANUAL CHANGE INFORMATION

Date: 9-14-82 Change Reference: C1/982

Product: 68000 E. P. and Probe Service Manual Part No.: 070-3770-00

DESCRIPTION Product Group 61

TEXT CHANGES

Page 4-18 Replace Table 4-15 with the following:

Table 4-15
Emulator Processor Port Addresses

Port Address	Address Lines 7	6	5	4	3	2	1	0	R(H)/ W(L)	Port Accessed
AD	L	H	L	H	L	L	H	L	H	EMU Status Port
									L	EMU Control Port
8E	L	H	H	H	L	L	L	H	H	AUX Status Port
									L	AUX Control Port
8F	L	H	H	H	L	L	L	L	H	Command Port
									L	

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MANUAL CHANGE INFORMATION

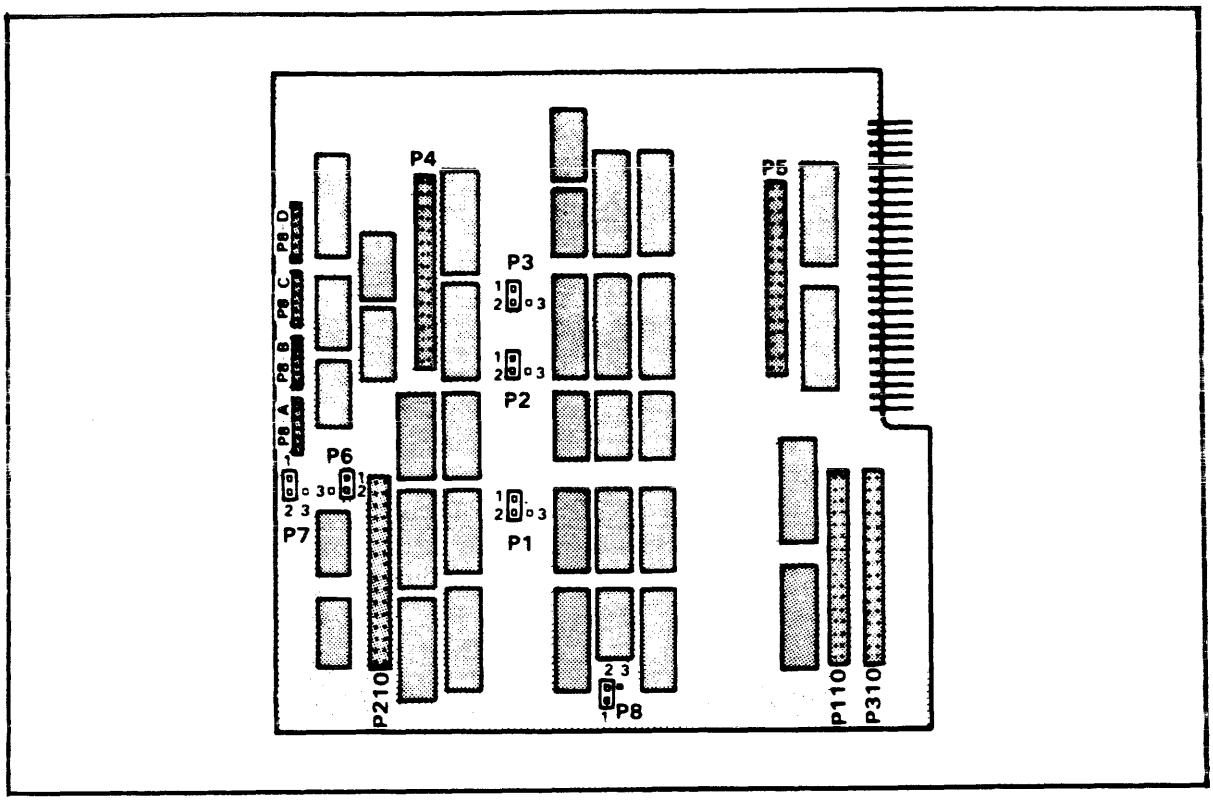
Date: 11-1-82 Change Reference: C2/1182

Product: 68000 E. P. and Probe Service Manual Part No.: 070-3770-00

DESCRIPTION Product Group 61

TEXT AND SCHEMATIC CORRECTIONS

Page 3-3 In Fig. 3-3, the pin configuration of P8 is shown incorrectly. Change Fig. 3-3 to the following:



Schematic 1 Isolation Buffers

Change U6050, U6070A, U6070B, U6090, U6110, and U6130 from 74LS240s to 74S240s.

Schematic 4 System Interface Control

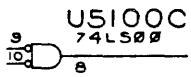
In the upper right corner, change signal name BB LDS(H) (shown going to sheet 8) to signal name BA LDS(H).

DESCRIPTION

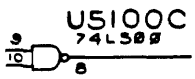
Schematic 4 System Interface Control (cont)

In the upper right corner, signal line IA0(H) is not connected to P13-5; therefore, remove the IA0(H) connection to P13-5.

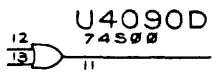
In the UMAP Valid Generator circuitry, change U5100C from



to the following:

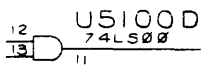


In the TTA Strobe Generation circuitry, change U4090D from

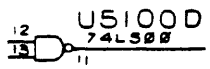


to the following:

In the lower left corner, change U5100D from



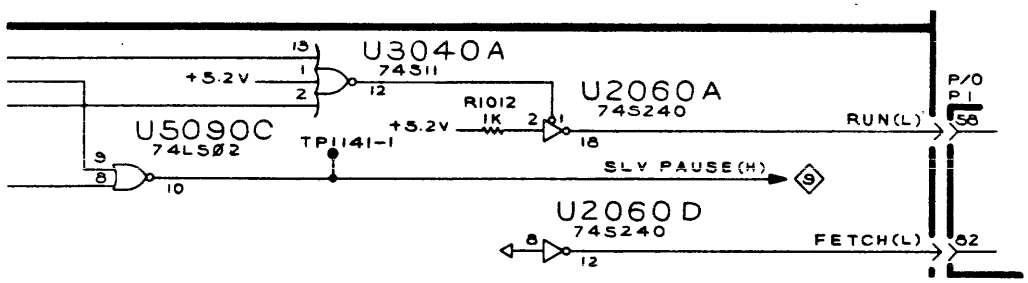
to the following:



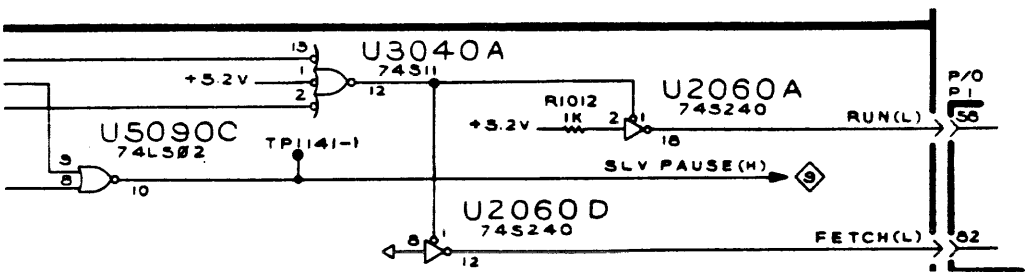
DESCRIPTION

Schematic 5 MODE0 Clock/RUN Control

Change the lower right corner from



to the following:

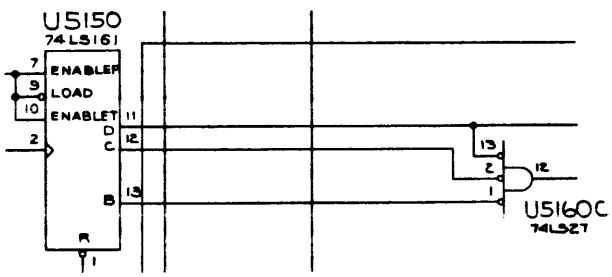


Schematic 7 D/R Restore PROMS

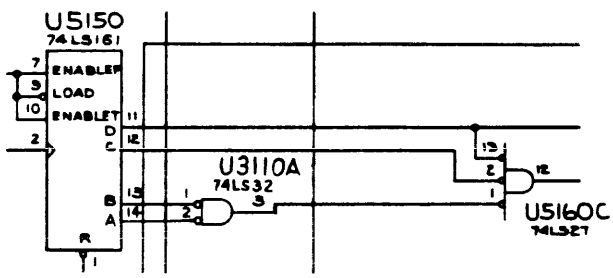
In the lower right corner, change signal line name RESET(L) to RESET RUN(L).

Schematic 13 EMU Status & Control Ports

Change the connection between U5150 and U5160C from



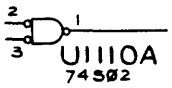
to the following:



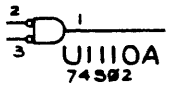
DESCRIPTION

Schematic 14 UMAP/Write Protect RAM

In the lower right corner, change U1110A from

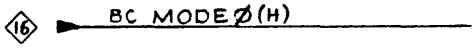


to the following:



Schematic 17 Clock Select

Near the center of the schematic, add source line



to U6030A-13, U6030B-11, U4030A-5, U9040C-8, and R9011.

Schematic 18 Probe A/D Buffers

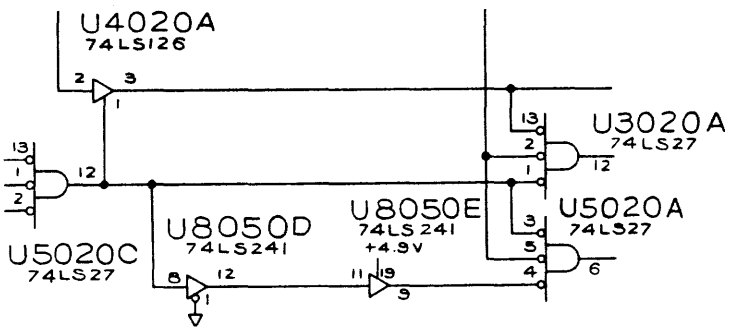
In the lower left, change signal line name
BA ID TO(L)/FROM(L) to BA ID TO(L)/FROM(H).

Schematic 21 Interrupt Decode

In the left center portion of the schematic, U7040A pin 2 is shown connected to AS(L) from sheet 17. Change this to read BB AS(L) from sheet 22.

Schematic 22 HALT/BR Tri-State

At the center of the schematic change



to the following: