

PDP-5 INTERRUPT SYSTEM  
PROGRAMMER'S GUIDE

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1.0 Introduction

The PDP-5 Interrupt System has been modified to provide automatic encoding of the device flags which cause interrupts. Upon receiving an interrupt, reading one word into the Accumulator, and executing that word as an instruction, a branch to one of 16 trap routines located anywhere in PDP-5 memory occurs.

In addition, there are instructions for independently arming and disarming individual interrupts.

At present, interrupts exist for the following:

- |      |           |               |
|------|-----------|---------------|
| (1)  | 930/PDP-5 | Link Receive  |
| (2)  | 930/PDP-5 | Link Transmit |
| (3)  | PDP-5     | Teleprinter   |
| (4)  | PDP-5     | Keyboard      |
| (5)  | Tablet    | Pen-down      |
| (6)  | Tablet    | Pen-up        |
| (7)  | Tablet    | Match         |
| (8)  | Display   | ∅             |
| [(9) | Display   | Keyboard]*    |

\* To be added soon.

## 2.0 General Operation

Each interrupt (except GO) has two memory elements associated with it: (a) a flag which when true causes the interrupt and which must be reset by program control, and (b) an arm/disarm bit which must be true (armed) in order for the interrupt to occur regardless of the state of the flag bit. In some cases (teleprinter, keyboard, 930 Link) the flag bit may be sensed with skip instructions.

Whenever an interrupt flag comes true for an armed flag, and provided an  $I\bar{O}N$  has been executed since the previous interrupt or since the machine was last halted, the contents of the P-counter are stored in memory location 1 and the instruction in location 2 is executed. Normally the contents of the Interrupt Counter are then read into the AC, stored in memory, and then executed to provide an indirect jump through a transfer vector to the particular interrupt processing routine involved. Within the interrupt routine the flag is turned off and the state of the arm bit changed if necessary. A general "return" routine would next execute an  $I\bar{O}N$  and continue processing the interrupted task.

3.0 Interrupt Counter, IC

The IC is derived from a scanner (See Figure 1.) which scans the interrupt flags, one every microsecond; the current set of flags is scanned every 10 usec. When an armed interrupt occurs, the scanner stops when the count representing the interrupt is reached. The scanner is then released whenever the interrupt flag is turned off or the counter reset. Since execution of IRC resets the counter, some "hardware priority" control is provided by executing IRC just prior to enabling interrupts. If an interrupt with higher C ("higher priority") has occurred, it will be serviced next.

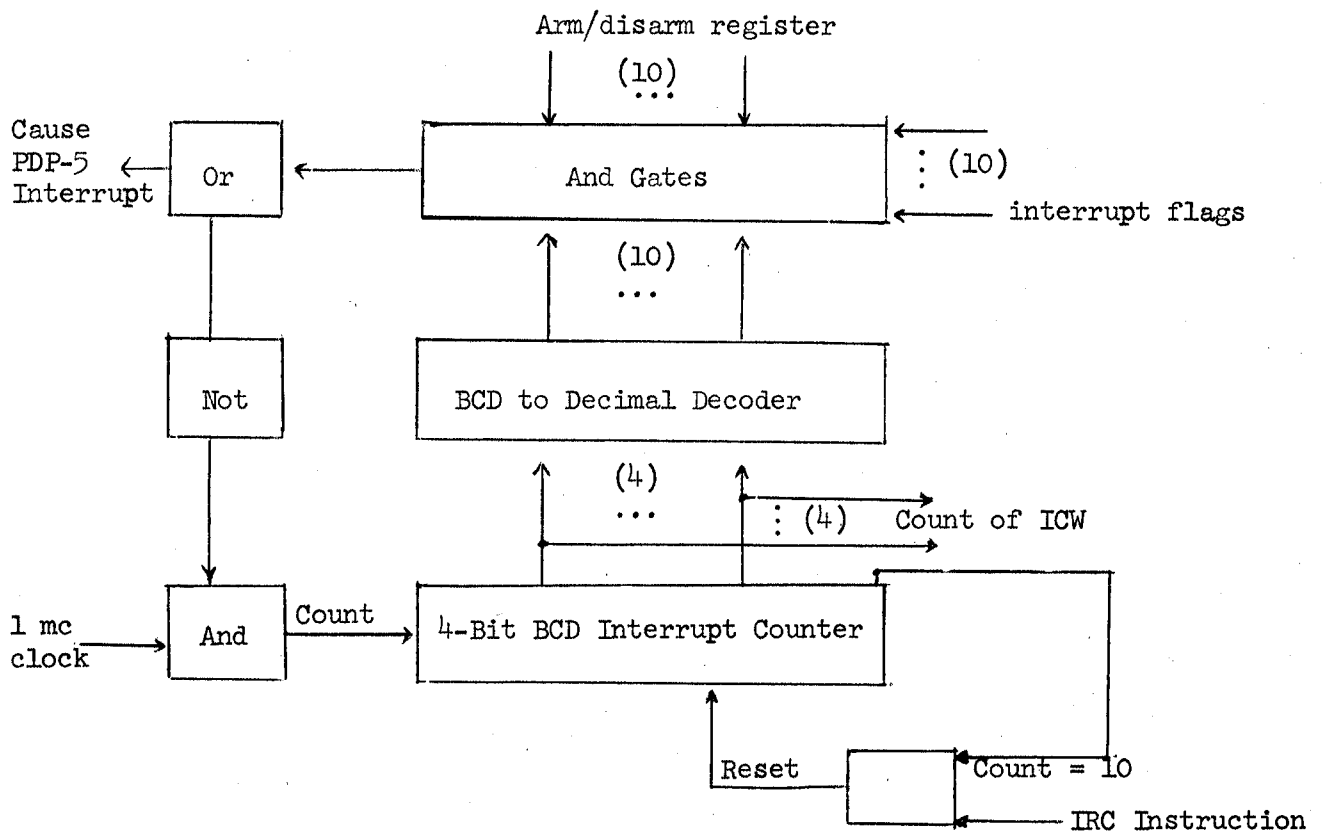
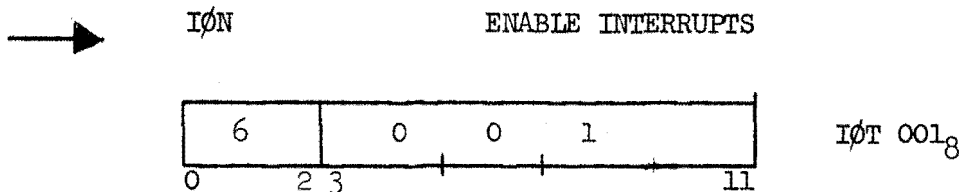


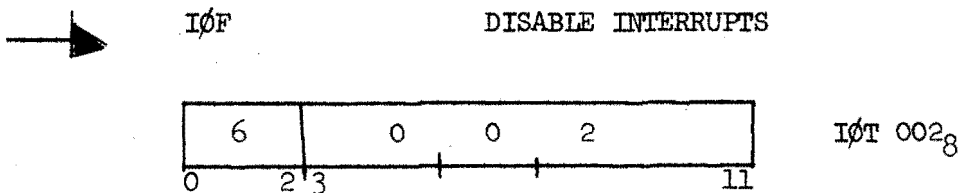
Figure 1: PDP-5 Interrupt Scanner Logic

#### 4.0 Enable/Disable Interrupts

The standard PDP-5 facility for controlling all interrupts simultaneously has not been modified. The following IØT's are for this purpose.



Turn interrupt control on. The instruction following IØN is privileged; i.e., it will be executed before the next interrupt occurs.



Turn interrupt control off. The equivalent of this instruction is executed at the time each interrupt occurs to prevent multiple interrupts.

#### 4.1. Arm/Disarm Interrupts

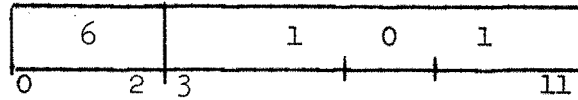
Two instructions are provided to prevent (disarm) or allow (arm) the occurrence of each interrupt individually.

At the time of execution, certain bits of the accumulator are associated with each interrupt. See Part 7.0.



ARM

ARM INTERRUPTS



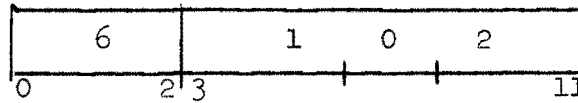
IOT 101<sub>8</sub>

Arm those interrupts whose associated accumulator bit is ON. Other interrupts are unaffected.



DARM

DISARM INTERRUPTS



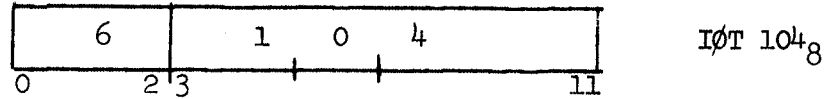
IOT 102<sub>8</sub>

Disarm those interrupts whose associated accumulator bit is ON. Other interrupts are unaffected.

5.0. Interrupt Counter Word, ICW

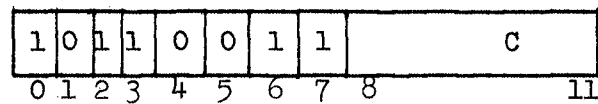
The word read into the accumulator is called the Interrupt Counter Word and is read with the following IOT instruction:

→ IRC READ INTERRUPT COUNTER WORD → AC



The contents of the accumulator will be OR'd with the contents of the Interrupt Counter Word which has the following bit pattern:

→ JMP\* 60<sub>8</sub>+C INTERRUPT COUNTER WORD (ICW)



where C represents which of 16 interrupts occurred. If the IC is executed, a branch will occur to one of 16 locations whose address is specified by the contents of locations 60-77 of page 0. The current assignments are given in part 7.0.

6.0

The following table contains all the detailed information necessary for operation of the PDP-5 interrupt system.

<u>Interrupt</u>	<u>ARM Accumulator Contents Bit</u>	<u>IC Contents</u>	<u>Page 0 Location</u>	<u>Flag Reset Instruction</u>	<u>Flag Sense Skip if True</u>	
930 Link Transmit	1 <sub>8</sub>	11	17	77	6212 6211	6211**
930 Link Receive	2 <sub>8</sub>	10	16	76	6201 6212	6201
Tablet/Display Match	4 <sub>8</sub>	9	15	75	6114 (GØ button)	--
Tablet Pen-down	10 <sub>8</sub>	8	14	74	6111 6112 6212	--
Tablet Pen-up	20 <sub>8</sub>	7	13	73	6202 6212	--
PDP-5 Keyboard	40 <sub>8</sub>	6	12	72	6032	6031
PDP-5 Teleprinter	100 <sub>8</sub>	5	11	71	6042	6041
Display GØ	Go is always armed		10	70	6212	--
Display Keyboard*	200 <sub>8</sub>	4	07	67***	6222 6212	

Special Instructions

IØT 001 Enable  
IØT 002 Disable  
IØT 101 Arm\*\*  
IØT 102 Disarm\*\*  
IØT 104 Read IC

\* To be added soon.

\*\* Also clears accumulator

\*\*\* Locations 60-66 are currently unassigned and won't occur



7.0. PDP-5 System Program - Interrupt Control

A sample PDP-5 interrupt control program is given below. The individual interrupt routines are responsible for preserving the state of the machine, turning off the flag, and enabling traps when they have reached a state in which they themselves can be reentered.

<u>Location (Octal)</u>	<u>Instruction</u>	<u>Comments</u>
0	----	Program Counter
1	----	Interrupt Store Location
2	DCA ACC	Start of Interrupt Control Routine, Save AC
3	IRC	Read Interrupt Counter Word
4	DCA .+1	Execute It
5	JMP* 60+C	
ACC	----	Accumulator Saved
Return --	RET	CLA
		For Return From Interrupt Routines
	TAD ACC	Restore AC
	IØN	Re-Enable Interrupts
	JMP* 1	Return to Last Routine in Control
67	DKBD	Display Keyboard
70	GØ	Display GØ
71	TPR	PDP-5 Teleprinter
72	KBD	PDP-5 Keyboard
73	FU	Tablet Pen-up
74	PD	Tablet Pen-down
75	LT	930 Link Transmit

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<u>Location (Octal)</u>	<u>Instruction</u>	<u>Comments</u>
76	LR	930 Link Receive
77	MAT	Locations of Interrupt Routines

The preceding program costs 66 usec. to get to an Interrupt Routine, and 60 usec. to return to the interrupted task, or 126 usec. overhead.