3301
CONTROL MODULES

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ELECTRONIC DATA PROCESSING SERVICE

3301 CONTROL MODULES

3301 CONTROL MODULES

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CONTROL MODULE

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3301 TYPEWRITER CONTROL MODULE

1.0 Introduction

The purpose of the Typewriter Control Module is to provide control and buffering between 3301 processor and the console typewriter. The control module also has provisions for a digital clock, which is an optional device. The typewriter functions both as an input or an output device, while the clock is an input device only.

The control module provides decoding from 3301 code to typewriter code for both reads and writes. It also provides HSM strobe control and status level request for the processor and case shift control, carriage return, and space functions for the typewriter.

1.1 General Description of Typewriter

The typewriter is an IBM, series 721, modified by the INVAC Corporation to be compatible with the 3301 processor. The typewriter will perform a receiving function (writing to typewriter) and sending function (reading from typewriter). The typewriter is capable of printing 15.5 characters per second when operating at maximum speed. Printing of a character requires a 180 degree (64.4 msec) rotation of the main cycle shaft which is released mechanically when sending, or by the clutch magnet when receiving (controlled by control module). Attached to the cycle shaft is a photo-diode timing disc which provides a sequence of timing pulses for syncronization with the control module. When sending, the character code is derived from 7 photo diode switches which transmit the character code to the control module (in typewriter code - 6 bits plus parity). These switches are mechanically operated within the typewriter. Signals leaving the typewriter are OV for a "1" and -12V for an "O". The signals are converted into compatible levels in the control module (O to 6.5V).

When receiving, the typewriter receives a 6 bit code (typewriter code) from the control module. Each "1" bit energizes one of 6 bit magnets which mechanically select the proper character to be printed.

The typewriter performs certain operations known as machine functions which are performed by single current pulses from the control module which energize the particular function solenoid. The cycle shaft does not rotate during a machine function. The machine functions

are: carriage return, upper case shift, lower case shift, and space function.

The typewriter returns signals, in addition to data, to the control module to indicate what case (upper or lower) it is in, when the carriage has completely returned, when the right hand margin has been reached, and when a machine function has completed.

2.0 Applicable Instructions

3301 instructions for the typewriter consists of reads, writes, and sense device. The reads or writes may be performed either in the SIMO 1 or SIMO 2 modes but never in the SIMO 3. The sense instruction is a normal mode instruction only. The read and write instructions terminate with an SCOM (16 or 17) interrupt if no errors are detected, or an SRA (13 or 14) interrupt if an error is detected. If the control module or typewriter is busy, the instruction will not perform and will enter the interrupt routine with INT·11 set (Busy or Inoperable). The carriage automatically returns at the completion of each read or write instruction and will cause INT 9 (device available) to take place upon completely returning to the left hand margin, indicating the typewriter is available for use.

2.1 Read Instructions

Read instructions are a means to allow data to be entered into the memory from the typewriter. The instructions terminate upon address equality or depression of the CANCEL or RELEASE buttons on the console. CANCEL terminates the instruction with an SRA interrupt to allow the programmer to re-staticize the original instruction through the interrupt routine. This is performed by programming and not by hardware. RELEASE terminates the instruction normally (SCOM) to allow the processor to proceed. Detection of an error or address equality during a read instruction terminates the instruction immediately with an SRA interrupt.

Input/output instructions are performed in the simultaneous modes only. Consequently, the S (SIMO 1) or C (SIMO 2) registers replaces the function of the A register; and the T (SIMO 1) or E (SIMO 2) assume the function of the B register. The addresses are transferred during the SIO 1 and SIO 2 status levels.

OPERATION	N	A	B
RF1	4	=	HSM Location	* HSM to receive
RF2	5	(EQUAL)	to receive the first character	the last character

* If RELEASE or CANCEL is depressed, the instruction will terminate regardless of the B address.

FINAL SETTINGS

Sf or Cf = HSM last character read +1
Tf or Ef = B i

The characters will be transferred into the memory one at a time for each key depressed, working from left to right.

If the read instruction was initiated by depressing the LOAD CONSOLE button, address equality is ignored and termination will take place only upon depressing of RELEASE or CANCEL. Depression of RELEASE terminates the instruction without the SCOM interrupt to allow the processor to perform the instruction located in location 0000. CANCEL will terminate the instruction with the SRA interrupt. Depressing LOAD CONSOLE generates the following conditions:

NOR	N	A	B	
4	=	0000	IGNORED	P Register set to 0000

2.2 Write Instructions

The write instructions provide a means of printing information from the memory to the typewriter. The instructions terminate on address equality. Either INT 16 or 17 is set if no errors are detected, or INT 13 or 14 if an error is detected.

OPERATION		N	A	B
WR 1	8	=	HSM location	HSM location
WR 2	9	(EQUAL)	of first char. to be written	of last char. to be written

FINAL SETTINGS

Sf or Cf = HSM location of last character written + 1
Tf or Ef = B i

2.3 Test Device Instruction

The test device provides a method of testing the typewriter or conditions in the control module and take a path accordingly. The test device is a normal mode instruction only.

OPERATION	N	A	B
S	=	Function to be tested (see chart)	Address of next instruction if any one condition being tested is present

Next instruction if condition(s) is not present.

Character	Bit Position	Symbol	Test Function
A_0	2^0	1	Is the Typewriter inoperable?
A_0	2^1	2	Is the Typewriter operating?
A_0	2^2	4	Has a Console Request been received?
A_0	2^3	8	Is there a parity error on read or write? (Has a RE or WE occurred?)
A_0	2^4	&	Has a message Cancel been received?
A_1	2^0	1	Carriage return complete?
A_1	2^2	4	Has A/B equality been received?

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

3.0 Control Module Operation

3.1 SIO 1 and SIO 2 Status Levels

The N character of the instruction is inspected by gate 27D8B which recognizes $76_{(8)}$ (equal sign), and that the instruction is not in the SIM 3 mode, to produce TNC (typewriter N count). If the simultaneous mode in the processor is not busy ($\overline{MB}$) and the instruction is a read forward (RF), the READ flip-flop is set to indicate a read instruction is in progress. READ, being reset, produces the level TYPE which indicates a write is in progress to the typewriter. The A ODD (27B3F) flip-flop is initially set at HK1 and if the A address of the instruction is an odd address (0B10), the flip-flop is RESET during SIO 1. The flip-flop will be triggered prior to executing the first character transfer to choose the appropriate character of a diad. A-ODD also provides HSM strobe control during read instructions.

The Operable Not Busy check is performed in the control module by gate 28C2H. If the typewriter is operable (TOP), the processor mode is free ($\overline{MB}$), the control module is free ($\overline{BUSY}$), and the Data Delay (DD) flip-flop is reset (indicating the carriage on the typewriter is not in the process of returning), the ONB return is sent to the processor to prevent INT 11 from being set.

The B-ODD (27B3H) flip-flop is set during SIO 2 to conform to the 2^0 bit of the B address. This will be used to terminate the instruction on the proper character of the last diad.

3.2 READS (Figure 3-1)

Following the SIO 2 status level, the control module remains in the static condition until a key lever on the typewriter is depressed. The code for the particular character is sent to the control module into the ENCODER (Figure 3-1) which translates the typewriter code into 3301 code (Chart 3-1). The character is then stored in the typewriter buffer and a status level requested to transfer the character into the memory. The status level gates the character from the buffer to either input Bus 0 or 1, depending upon the condition of the A-ODD flip-flop and is stored into the memory as addressed by either the S or the C registers. This process is repeated each time a key lever is depressed until a reason to terminate has been found.

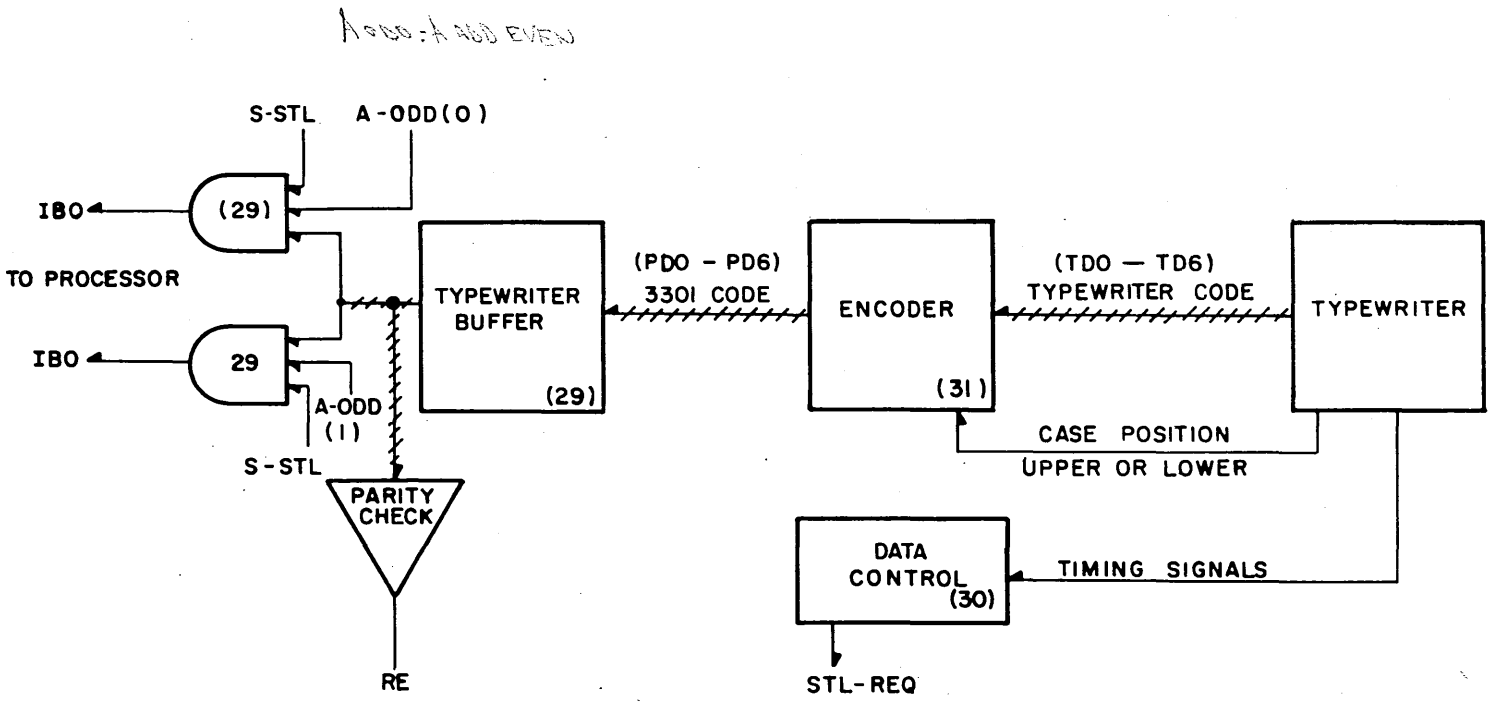

Figure 3-1 READS FROM TYPEWRITER

CHART 3-1 3301 and TYPEWRITER CODES

Character	Case	3301 Code (Octal)	Typewriter Code (Octal)	Character	Case	3301 Code (Octal)	Typewriter Code (Octal)
A	L	21	17	7	L	07	71
B	L	22	12	8	L	10	65
C	L	23	13	9	L	11	64
D	L	24	14	Ø	L	00	61
E	L	25	15	.	L	33	40
F	L	26	10	”	L	60	01
G	L	27	11	&	L	20	41
H	L	30	05	$	L	53	20
I	L	31	04	/	L	61	57
J	L	41	37	#	L	13	60
K	L	42	32	,	L	73	00
L	L	43	33	-	L	40	21
M	L	44	34	¬	U	12	71
N	L	45	35	@	U	14	65
O	L	46	30	(	U	15	64
P	L	47	31	)	U	16	61
Q	L	50	25	CR	U	37	40
R	L	51	24	=	U	76	01
S	L	62	52	'	U	36	41
T	L	63	53	(SUB) 10	U	57	20
U	L	64	54	e	U	17	60
V	L	65	55	¤	U	77	00
W	L	66	50	<	U	56	21
X	L	67	51	:	U	35	44
Y	L	70	45	;	U	36	45
Z	L	71	44	+	U	32	51
1	L	01	77	>	U	55	24
2	L	02	72	*	U	54	25
3	L	03	73	⌐	U	52	31
4	L	04	74	↑	U	75	04
5	L	05	75	%	U	74	05
6	L	06	70	÷	U	72	11

The control module is actually controlled by two signals from the timing disc on the typewriter (Figure 3-2). The figure is marked in degrees of rotation of the cycle shaft which requires 180 degrees to print one character (1/2 revolution). The character bits (DATA) begin at approximately 17 degrees and last until approximately 160 degrees. The typewriter data strobe (TRDS) is produced at 43 degrees of rotation and ends at 107 degrees. The typewriter data gate, (TDG) is always present until 43 degrees of rotation, at which time it goes negative and stays negative until 167 degrees of rotation. The signals from the typewriter are considered present when at 0 volts and not present at -12 volts. The typewriter levels are converted to control module levels by the receivers in the control module.

	INPUT	OUTPUT
3P143 & 3P141 Receivers	0 V	0 V
	-12 V	+6.5 V

The data bits are received on print 31 by the 3P141 receives in areas D, -2, 3, 4, 5, 6, 7, and are labeled as Typewriter data (TD 0, 1, 2, 3, 4, 5, 6) signals. The encoder then converts the character into 3301 code and produces the Processor Data signals (PD 0, 1, 2, 3, 5, & 6). The PD 4 signal does not exist, since it is necessary only to invert the 2^4 bit before it goes into the typewriter buffer ($\overline{TD4}$ = TB 2^4). The encoder must know whether the typewriter is sending a code in the upper case or lower case shift position in order to produce the correct 3301 code. This is indicated by the level UC being present for upper case and not present for lower case characters. By inspecting the code chart (Chart 3-1) it can be seen that the typewriter sends identical codes for a pair of characters, however, one is in upper case and the other in lower case. For example, the typewriter code for an H is 05_8 in lower case and the code for a % is 05_8 in upper case. The encoder would decode an 05_8 in lower case to a 30_8 (3301-H) and an 05_8 in upper case to a 74_8 (3301 - %).

The outputs of the encoder (PD signals) are sent to a set of control gates leading into the typewriter buffer (29C2A, C3A, C4A, C5A, C6A & C8C) which are controlled by gate 29D2A. To determine the time at which the character is gated to the buffer, Figure 3-2 must be discussed.

Control of the data within the control module is performed by the DC (Data Control 35C7B) and DDC (Delayed Data Control 35B7A) flip-flops. When a key lever is depressed, the cycle shaft starts to rotate. The data signals are sent to the encoder at approximately 17 degrees

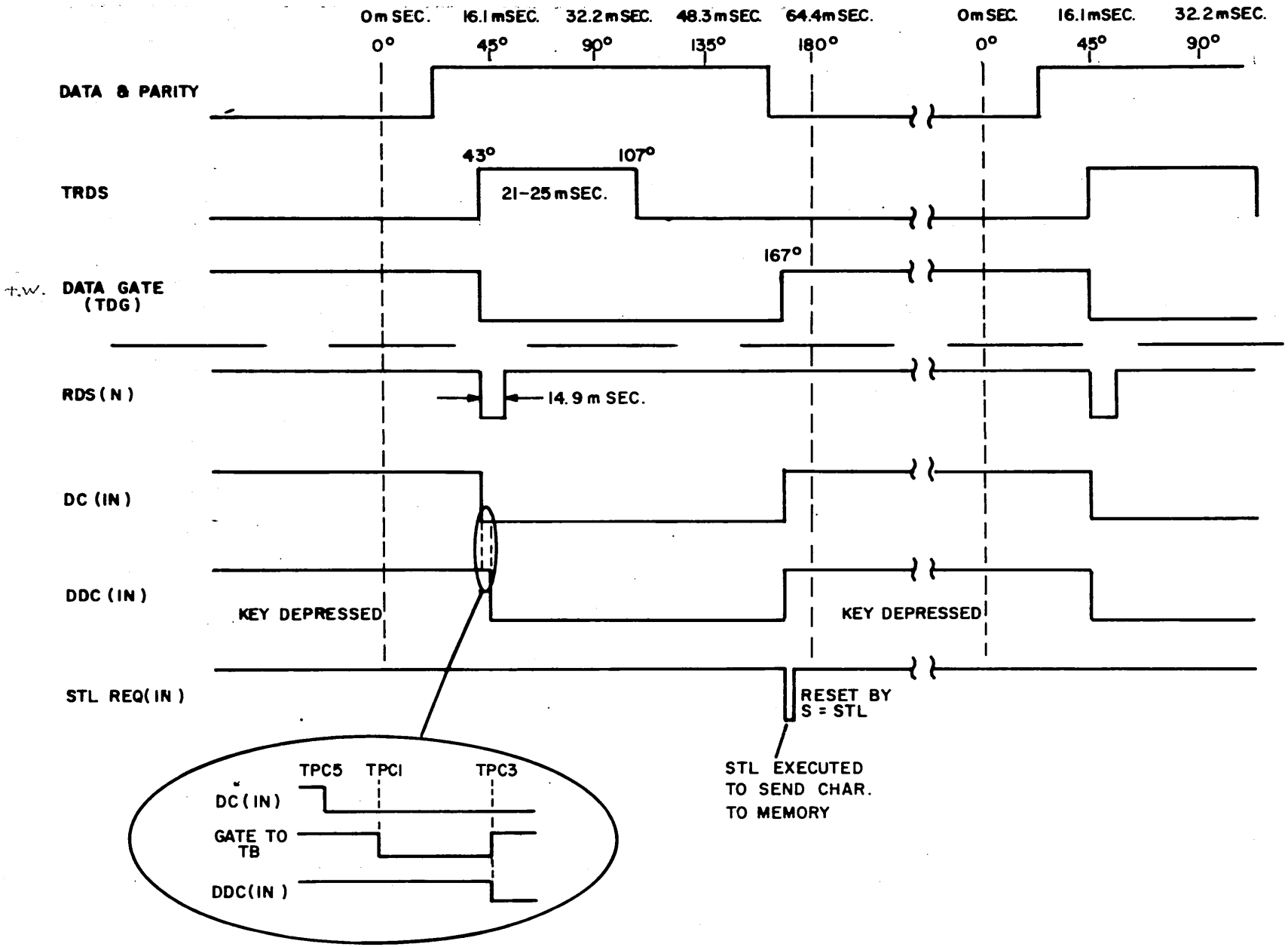

Figure 3-2 Read Timing

of rotation and the PD signals are immediately produced. The TRDS (Typewriter Read Data Strobe) is sent at 43 degrees of rotation and is received by 30D1A to trigger a 14.9 msec "one shot" to produce RDS (Read Data Strobe) in the control module. Also, at 43 degrees the TDG (Typewriter Data Gate) goes negative (always present until 43 degrees). Receiver 30D7A provides a path to set the DC flip-flop at the next TPC 5. With DC set, DDC reset, and RDS present, the outputs of the encoder (PD signals) are gated to the typewriter buffer (29D2A). DDC is set at the next TPC 3 (30C7C) to remove the gating signal. The 3301 code for the particular character is stored in the buffer until a status level is requested to insert the character into the memory.

The status level is requested by resetting the DC flip-flop when TDG appears (167 degrees of rotation) and TPC 5 (30D7J). With DC reset and DDC set, the status level request flip-flop (30A7B) is set to send either an S1 or an S2 request to the processor (28A7B or A6A).

The signal READY (30B7C) is produced which triggers the A-ODD flip-flop (27B3F) to the opposite state and clocks a parity checker (30D5A) which is inspecting the character in the TB for odd parity. If even parity exists, the RE flip-flop is set, indicating a Read Error. RE prevents the status level from being requested by setting the PRE-STOP (28C7D) flip-flop.

When the status level is produced by the processor, the contents of the TB are gated to either Input Bus 0 or 1, depending upon the condition of the A-ODD flip-flop (29 area B). A-ODD, being set, sends the character to IB 1 or if reset, to IB 0. The character is then sent to memory as addressed by the S or C register. This cycle is repeated for each character printed until a reason to terminate is found.

3.2.1 Space Function During Reads

Depressing the space bar on the typewriter advances the type head one position without printing. The cycle shaft does not rotate during this function, consequently, the TDG pulse is not generated to set the DC flip-flop. The typewriter code for a space (67_8) is sent to the control module and is recognized by 30B6E to set the DC flip-flop (30D7B) and allow a status level to be requested. The 67_8 is decoded to a 3301 space (12_8) and sent to the typewriter buffer. The status level will take the character from the buffer into the memory. Each depression of the space bar inserts a 12_8 into the memory.

3.2.2 Read Termination (Figure 3-3)

Termination of reads may occur due to one of four conditions; (1) Address equality, (2) RELEASE depressed, (3) CANCEL depressed, (4) An error occurs.

RELEASE terminates the instruction on a SCOM interrupt while address equality, CANCEL or an error, terminates with a SRA interrupt.

Depressing the RELEASE button sets the TERM flip-flop (28C5F) which allows the Pre-stop flip-flop (28C7D) to be set at a TPC 5 following the return of the RELEASE button to its normal condition ($\overline{\text{RELEASE (P)}}$). With TERM set, P-STOP set, and ERROR reset, the next TPC 3 sends the SCOM 1 or SCOM 2 return to the processor (28B5C). TPC 3 also sets the STOP flip-flop and resets the BUSY flip-flop to terminate the instruction in the control module.

Depression of the CANCEL button sets the CANCEL flip-flop (2802B) and at TPC 5 the P-SRA (28C5E) flip-flop is set. TPC 1 then sets the ERROR flip-flop (28C4C) to allow the SRA 1/2 return to be sent to the processor at the next TPC 3 (28B5A). Release of the CANCEL switch allows P-STOP and STOP to be set to terminate the instruction.

Detection of an error (RE or DNF) terminates the instruction in the same manner as CANCEL, except the CANCEL flip-flop is not set.

3.3 WRITES (Figure 3-4)

During a write instruction a character is sent into the control module from the processor. The character is inspected by the case shift logic to determine whether the character is an upper case or a lower case character. The typewriter is instructed to shift to the appropriate case, if necessary. The character is decoded into typewriter code (Chart 3-1) and placed into the typewriter buffer. The character is delayed until the typewriter has shifted to the appropriate position then is sent to the typewriter to energize the bit magnets. The typewriter mechanically prints the character and sends back the code for the character actually being printed. This code is compared against the code in the buffer. If the codes do not agree, a write error is indicated, the SRA interrupt is sent to the processor, and the instruction continues to address equality. If no errors are detected, the instruction continues until AE is detected and the instruction terminates with a SCOM interrupt.

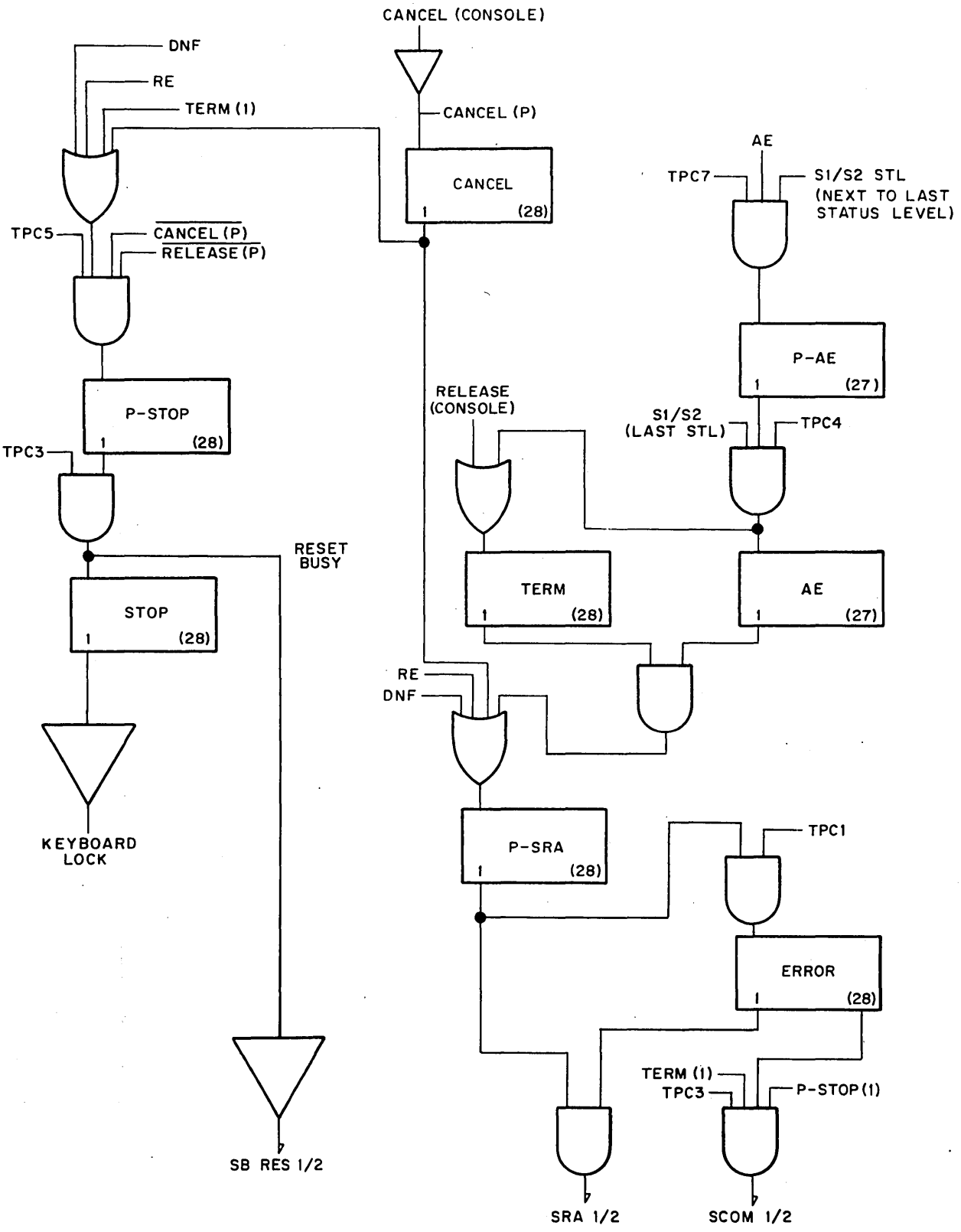

Figure 3.3 Read Termination

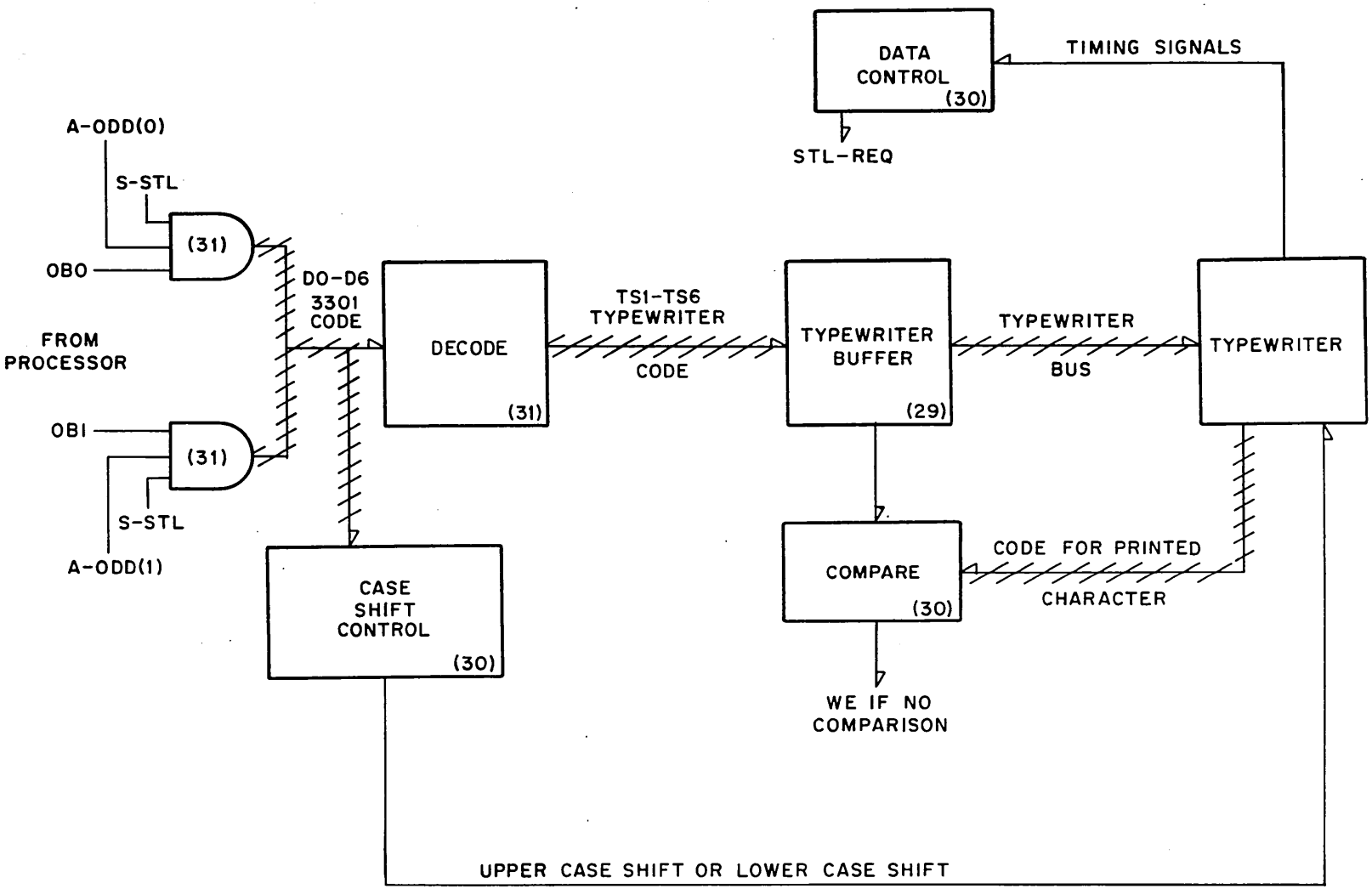

Figure 3.4 Writes to Typewriter

Typewriter and control module timing is shown on Figure 3-5. The CLUTCH GATE signal is always present until the cycle shaft has rotated 43 degrees, at which time the signal is negative until 107 degrees of rotation. CLUTCH GATE is used to control status level requests and data control within the control module through the DC and DDC flip-flops. the COMP (complete) signal is transmitted to the control module at 43 degrees to indicate that the character sent by the control module is in the process of being printed and the control module may begin the sequence for the next character coming up.

To actually print a character, the cycle shaft must be released by the PRINT TRIGGER from the control module. To allow the typewriter to operate at maximum speed, the print trigger must be sent no later than 107 degrees of rotation in order to prevent the cycle shaft from latching at 180 degrees. This is due to the "pull in" time of the clutch magnet in the typewriter. If the PRINT TRIGGER is missing, the cycle shaft will stop and cannot be released until the next PRINT TRIGGER is sent. The cycle shaft does not rotate during machine functions (case shift, space and carriage return).

Following the SIO 2 status level, an S status level is requested to bring the first character from memory. This is performed by setting the DC flip-flop at TPC 5 through gate 30D8D. Clutch gate is present, COMP is not, and SPACE is reset to provide the primes. With DC set and DDC reset, the STL REQ flip-flop is set (30B7E) to request a status level. The status level brings a diad of data into the control module over OB 0 and OB 1 (print 31 area D). The A-ODD flip-flop chooses the appropriate character to go into the decoder (31D3D or 31D8A). The "bit" signals at this point are labeled D0 through D6 (Data 2^0 to 2^6). The D signals are sent to the decoder to be transformed into the typewriter code. At TPC 7 of the S status level the output gates of the decoder are clocked by the GTR (Gate to Register) pulse (31C1C). The clocked outputs of the decoder are called Typewriter Signals TS 1 to TS 6 which go directly into the typewriter buffer (TS 1 is 2^0, TS 2 is 2^1, etc.). The TB now contains the typewriter code for the particular character to be printed. TPC 8 of the status level sets the PDG (Print Data Gate 30B5D) flip-flop which produces the print trigger, provided the Data Delay (DD) flip-flop is reset. DD delays the data if a case shift or a carriage return is in progress. The print trigger is sent to the typewriter to release the clutch for the cycle shaft. The signal CDG (Control Module Data Gate 30A5A) gates the contents of the TB to the typewriter through gate 29C1A. TDG is present from the typewriter at this time (Figure 3-5). The typewriter now has a character to print and the cycle shaft has been released. The actual printing is

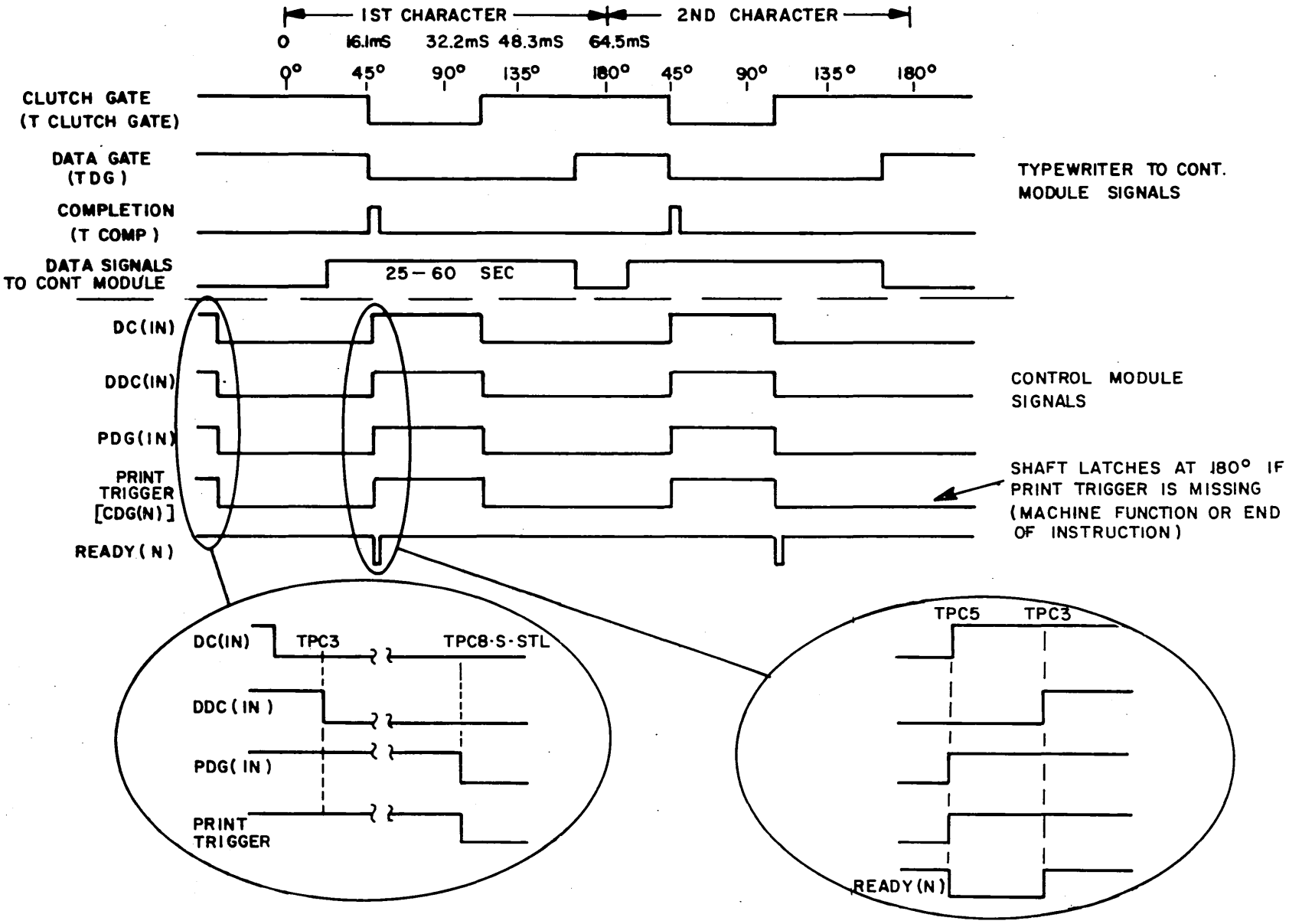

FIGURE 3-5 WRITE TIMING

now a mechanical function of the typewriter. When the shaft has rotated 43 degrees the CLUTCH GATE from the typewriter disappears and the typewriter sends the COMP signal to the control module. The DC flip-flop is reset at TPC 5 (30D6C) which allows gate 30B7B to create the READY pulse. READY resets the PDG flip-flop (30B5A) and gates the output of the compare circuit (30C4B). If the character in the buffer does not compare with the actual character being printed, the WE flip-flop is set.

The shaft continues to revolve and at 107 degrees, CLUTCH GATE appears, to allow DC to be set and a status level is requested which brings the next character to the control module. The character is decoded and placed into the TB and a print trigger is developed to energize the clutch magnet before the cycle shaft latches. The shaft continues to revolve and the character is printed provided a case shift is not required. If a case shift is required, the cycle shaft will latch and the print trigger and character will be delayed until the case shift is complete.

3.3.1 Case Shift

Each character entering the control module during a write is inspected to see if it is to be printed in the upper or lower case. Gates 30D2E, C2B, and C3E perform this function by inspecting the 3301 code for each character as it arrives from the Output Bus. The conditions for an upper case character are $2^3 \cdot \left[2^2 / \overline{(2^0 \cdot 2^1)}\right]$. The output of 30C3E is compared to the actual case position of the typewriter and if a lower case shift is required, SL (Shift Lower) is produced or if an upper case shift is required, SU (Shift Upper) is produced. The case shift indicator (CSI) flip-flop is either set or reset, depending upon the two signals. The case shift required (CSR) flip-flop is set which allows a 35 msec "one shot" to send either UCS or LCS to the typewriter, depending upon the CSI flip-flop. The data delay (DD) flip-flop (30A4B) is also set, which prevents the print trigger and character from being sent to the typewriter (inhibits 30B6H). When the case shift is complete, the typewriter returns the COMP signal to reset DD and CSR and allow the character to be printed. The typewriter requires approximately 30 milliseconds to perform a shift.

3.3.2 Write Termination (Figure 3-6)

Write instructions normally terminate when address equality has been detected by the processor. If a WE occurs, the instruction continues to completion and terminates with the SRA

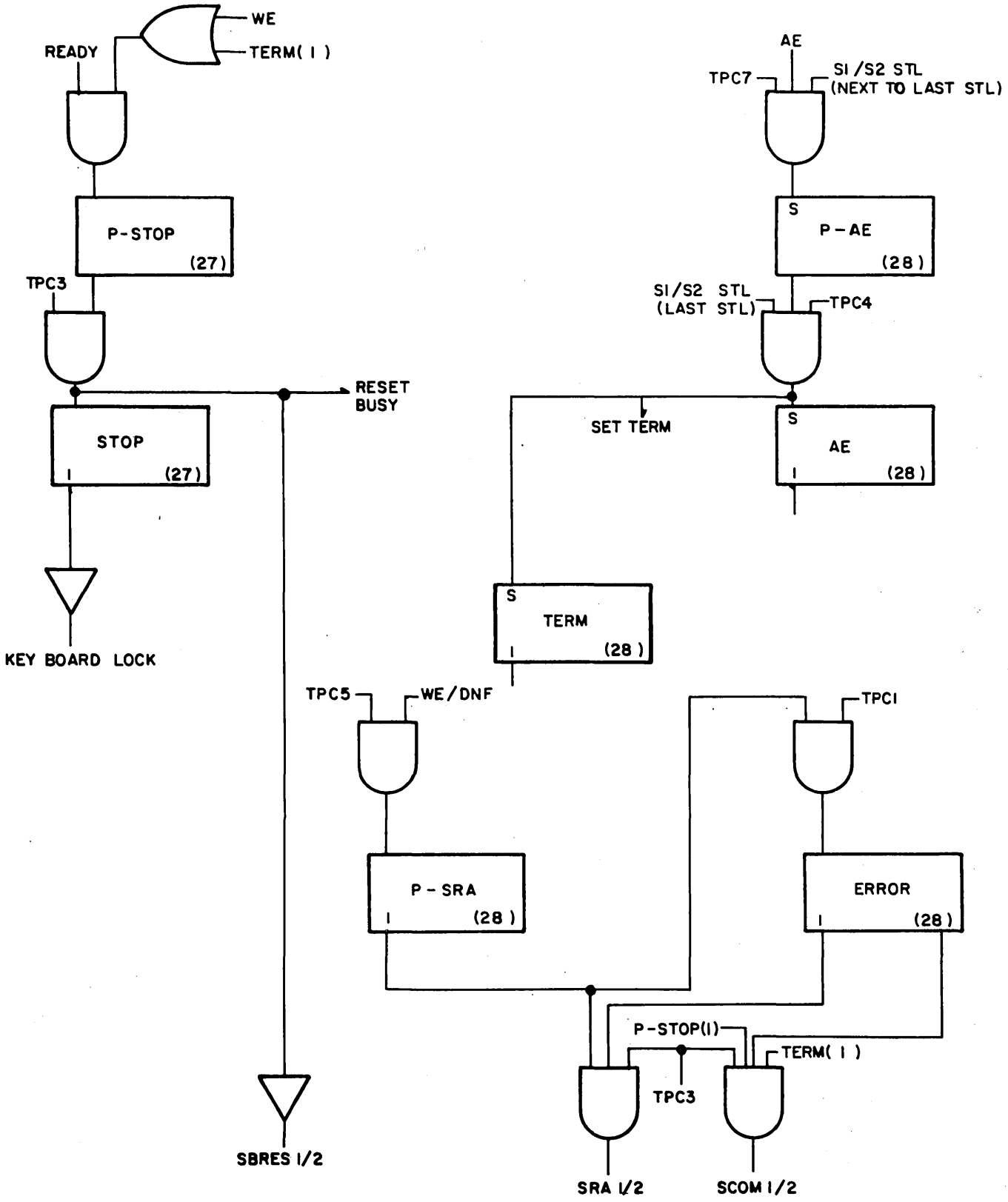

Figure 3.6 Write Termination

interrupt set. The SRA interrupt is set immediately upon detection of the WE, however, the instruction cannot terminate until AE is detected.

Address equality is detected by the processor during the next to last status level (addresses are compared in the processor after the bus adder modification). TPC 7 of this status level the P-AE (27B4A) flip-flop is set and at TPC 4 of the next (last) status level, the AE flip-flop is set. When the READY signal occurs indicating the typewriter is in the process of printing the last character, the P-STOP (28C7D) flip-flop is set to send the SCOM 1/2 return to the processor if an error has not occurred (28B5D). The STOP flip-flop is set at TPC 3 to terminate the instruction in the control module.

The DNF error will terminate the instruction immediately by setting P-STOP and P-SRA. A WE being detected sets the P-SRA flip-flop and sends the SRA return to the processor but the instruction continues until AE has been detected in the normal manner except the SCOM return is inhibited by the ERROR flip-flop (28B5D).

3.3.3 Space Function

If the character to be printed is a space (3301 - 12_8) the typewriter is to advance one position without printing. Gate 30C2A recognizes the 3301 space code and sets the space flip-flop (30B2C). With PDG set (S status level), a 35 msec pulse is sent to the typewriter to perform the space function. SPACE being set prevents the print trigger and character from being sent to the typewriter (inhibits 30B6H). When the typewriter completes the space function, the complete signal is returned to trigger a 1 msec "one shot" (30C2D) to reset the DC flip-flop and 1 msec later to reset SPACE. Resetting space allows DC to be set to start the next character cycle.

The case shift function is inhibited during a space function since a shift operation would be wasted time. The space will be recognized as an upper case character but gate 30A3C prevents the shift command from being generated.

3.4 Carriage Return (Figure 3-7)

The typewriter will be instructed to do a carriage return when either of two conditions exist:

during a write instruction when the right-hand margin is reached, and at the completion of every Read or Write instruction. When the carriage return is due to the completion of an instruction, INT 9 occurs in the processor as soon as the carriage is completely returned. If an instruction is attempted while the carriage is in the process of returning, the instruction will terminate on INT 11 and will not be performed, therefore, the INT 9 condition indicates the typewriter is available for use. The typewriter requires approximately one second for a full carriage return.

The typewriter indicates when the right-hand margin has been reached by setting the RHM flip-flop (30C3D) in the control module. When the READY signal occurs, indicating the last character of the line has been typed, a 35 milli sec. pulse is sent to the typewriter (30A3B) and energizes the carriage return solenoid. The DATA DELAY (30A4B) flip-flop is set to delay all data until the carriage has completely returned (inhibits 30B6H). When the carriage has returned to the leftmost margin, the complete signal is sent to the control module to reset the DD flip-flop and allow the Write instruction to continue.

To perform a carriage return at the completion of an instruction, the setting of the STOP flip-flop initiates the 35 milli sec. carriage return pulse (30B3D). The COMP signal indicates when the carriage has returned and sets the P-IR9 (27C3J) flip-flop to send a signal called DDFC to the processor to set IR 9 in the interrupt register. (The signal is labeled DDFC only to maintain standard signal nomenclature with the processor.) The IR 9 (27C3H) flip-flop in the control module is also set to provide a sense condition for the TEST DEVICE instruction and allows P-IR9 to be reset. This prevents sending a second IR-9 condition to the processor. The control module IR9 remains set until the next instruction is performed or a TEST DEVICE (sense) instruction is executed sensing for carriage return complete ($A^1\ 2^0$). The resetting of IR 9 is performed by the SENSE - IR-9 flip-flop in the case of the TEST DEVICE.

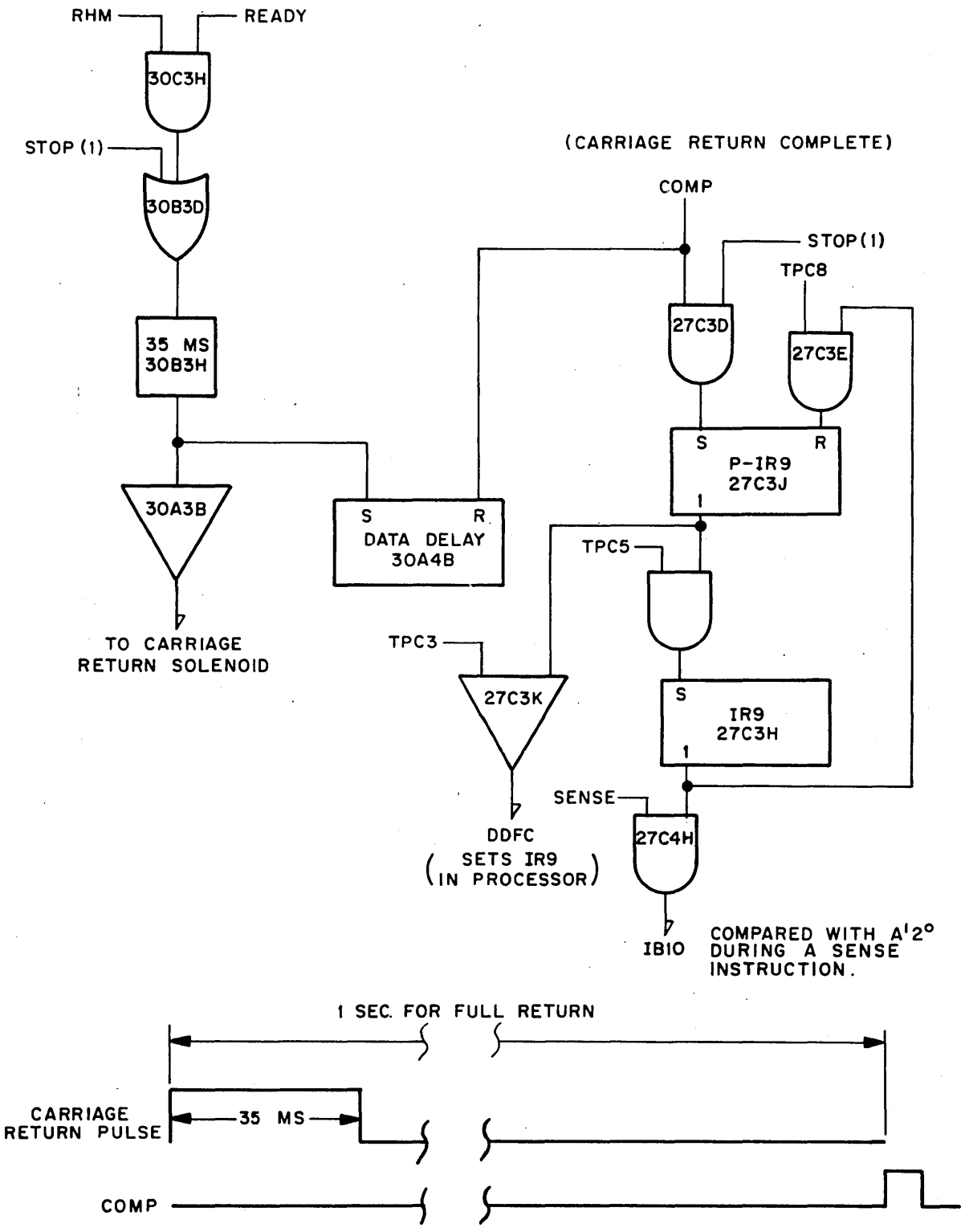

Figure 3.7 Carriage Return

3303 - 005 CONTROL MODULE

SIO 1

SIO 1 Level	Set SIO
	$\overline{MB}$ • TOP • TNC • DD(0) • (RF/WR) • $\overline{BUSY}$ - ONB TO PROCESSOR
	$\overline{MB}$ • COP • $\overline{BUSY}$ • CNC - ONB TO PROCESSOR
	IOS - ONB TO PROCESSOR
TPC 1	Set TPC 13
	$\overline{IOS}$ • $\overline{BUSY}$ • TNC - Generate HK 1
	HK 1 - Set A-ODD, Reset STOP , Reset READ
TPC 13	$\overline{IOS}$ • $\overline{BUSY}$ • TNC • $\overline{SIO\ 2}$ - Generate HK/GR
	$\overline{BUSY}$ - Reset STROBE COUNTER (clock only)
TPC 2	TNC • $\overline{BUSY}$ • RF • $\overline{MB}$ - Set READ
	IOS • TNC • OB 10 - Set SENSE IR 9
	TNC • $\overline{BUSY}$ • OB 10 - Reset A-ODD
	$\overline{SOP\ 3}$ • CNC (N = 71) $\overline{MB}$ • RF • $\overline{BUSY}$ - Set C/T & READ
TPC 4	Reset TPC 13

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SIO 2

TPC 1	Set TPC 13
TPC 2	SOP2 • $\overline{\text{BUSY}}$ • (TNC/CNC) - Set SIM 2
	TNC • OB 10 • $\overline{\text{BUSY}}$ - Set B-ODD
TPC 3	AE • $\overline{\text{BUSY}}$ • TNC - Set P-AE
TPC 4	(RF/WR) • TNC • DD(0) • TOP • $\overline{\text{MB}}$ - Set BUSY
	CNC • C/T(1) • COP - Set BUSY
	Reset TPC 13
TPC 5	SENSE•IR 9 (1) - Reset C-IR 9 & IR 9
TPC 8	Reset SENSE IR 9
	Reset SIO

3305-005 SOURCE & ABBREVIATIONS

AE (1N)	Address Equality	27A5B
AL1	Alarm Inhibit	27D6C
A-ODD (1N - ON)	A Address Odd	27B3F
AR	Alarm Reset	27D6B
B-ODD	B Address Odd	27B3H
BUSY (1N-ON)	Control Module Busy	27C7H
BUSY (1P)	Control Module Busy	27B7B
BUSY (OP)	Control Module Busy	27B7C
CANCEL (1N)	Cancel Flip-flop	28D2B
CANCEL (P)	From Console	28D2A
Carriage Return SOL	Carriage Return Command	30A3B
CDG	Control Data Gate	30A5A
C-IR9	Control Interrupt 9	27C2F
CLUTCH GATE		30D7E
CNC	Clock N Character	30C8D
COMP	Complete	30D8A/D6A
CON INT	Console Request Interrupt	27A4B
CON REQ (NO)	Console Request Normally Open	27D4B
CON REQ (NC)	Console Request Normally Closed	27D4A
CON REQ (1N)	Console Request Flip-flop	27B4B
COP	Clock Operable	28D3A
CR	Carriage Return	30B3H
CSR (FF)	Case Shift Required	30A2A
CSR (P)	Case Shift Required	30A2A
C-STROBE-1	Clock Strobe 1	28A3C
C-STROBE-2	Clock Strobe 2	28A3B
C-STROBE-3	Clock Strobe 3	28A3A
C-S1/S2	S1 or S2 Status Level in Control Module	27A6D
C/T	Clock or Typewriter Flip-flop	30B8D

DC	Data Control Flip-flop	30C7B
DD	Data Delay Flip-flop	30A4B
DDC	Delayed Data Control	30B7A
DDFC	(Data Disc File Complete) Sets Processor IR9 on a Carriage Return	27C3K
DNF	Device Not Following	30B5E
D0	Data from Output Bus 2^0	31C3C/C3E
D1	Data from Output Bus 2^1	31C4C/C4E
D2	Data from Output Bus 2^2	31C5D
D3	Data from Output Bus 2^3	31C5A/C5F
D4	Data from Output Bus 2^4	31C6A/C6F
D5	Data from Output Bus 2^5	31C7B/C7H
D6	Data from Output Bus 2^6	31C8A
ERROR	Error F. F.	28C4C
ETW	Sense Condition for Console Request	28C2A
GR	General Reset	27D6A
GTR	Gate to Register	31C1C
HK	Housekeeping	27B2D
HK/AR	Housekeeping or Alarm Reset	30C6B
HK/GR	Housekeeping or General Reset	27A2A
HK1	Housekeeping #1	27B6A
I-O INST	Input/output Instruction	27C7A
IOS	Input/output Sense Instruction	28D3D
IR 9	Interrupt 9	27C3H
LCS	Lower Case Shift	30A2B
LOCK SOL	Keyboard Lock	28A7D
MB	Mode Busy	28C7A
MOTION	Sense Condition for Busy	28C2C

N0	N Register 2^0	27D5A/D5C
N1	N Register 2^1	27D5B/D5D
N2	N Register 2^2	27D4A/D4E
N3	N Register 2^3	27D4B
N4	N Register 2^4	27D4C
N5	N Register 2^5	27D4D
N6	N Register 2^6	27D3A
ONB	Operable Not Busy	28B1B
P-CON REQ	Pre Console Request	28C4D
PDG	Print Data Gate	30B5D
PD0	Processor Data 2^0	31B2D/B2H
PD1	Processor Data 2^1	31A2D
PD2	Processor Data 2^2	31B3A/B3E
PD3	Processor Data 2^3	31B5D/B5F
PD5	Processor Data 2^5	31A6D/A6F
PD6	Processor Data 2^6	31A4H
P-IR9	Pre Interrupt 9	27C3J
PRINT TRIGGER	Clutch Pulse for Cycle Shaft	30A6A
P-SRA	Pre Simultaneous Requires Attention	28C5E
P-STOP	Pre-Stop	28C7D
RB	Reset Buffer	27C4F
RDS	Read Data Strobe	30D1C
RE (P)	Read Error	30D5C
RE (1N)	Read Error FF	30C5A
READ (1N)	Read Instruction	27C8F
READ A (N)	Read Instruction	27B8C
READ B (N)	Read Instruction	27B8B
READ T (N)	Read from Typewriter	27A8B
READ S1/S2	S1 or S2 Status Level During Read	27A1A
READY		30B7C

REL (P)	Release	28C5D
RESET BUSY		28B3B
RESET DC	Reset Data Control	30C2D
RESET PDG	Reset Print Data Gate	30B1C
RESET P-STOP	Reset Pre Stop	28A8A
RES RHM	Reset Right Hand Margin	30C1B
REV	Sense Condition for Cancel	28C2B
RF	Read Forward	27D7A
RHM	Right Hand Margin	30C1B
RHM (ON)	Right Hand Margin F. F.	30C3D
SB RES 1	Simultaneous Busy Reset SIMO 1	28A6B
SB RES 2	Simultaneous Busy Reset SIMO 2	28A6C
SCOM 1	Simultaneous Complete SIMO 1	28A5C
SCOM 2	Simultaneous Complete SIMO 2	28A4A
SENSE (N)	Input/output Sense to Typewriter	28D3F
SENSE (P)	Input/output Sense to Typewriter or Clock	28B3A
SENSE IR9	Resets IR 9 During a Sense	27C1B
SET BUSY	Set Busy FF	27C7D
SET DC	Set Data Control F F	30B6D
SET READ (P)	Set Read FF for Clock	30B8C
SET TERM	Set Terminate FF	27B5D
SIMO 2	SIMO 2 Instruction	27B5A
SIO (1N)	SIO 1 & SIO 2 Status Levels	27A6C
SIO 1	SIO 1 Status Level	27B6E
SIO 2	SIO 2 Status Level	27B7E/A7A
SL	Shift Lower	30B3B
SOP 2	SIMO 2 Operation	27C6A
SOP 3	SIMO 3 Operation	27D8A
SPACE (1N)	Space FF	30B2B
SPACE SOL	Pulse for Space Solenoid	30A1A
SRA 1	Simultaneous Requires Attention SIMO1	28A5A
SRA 2	Simultaneous Requires Attention SIMO2	28A5B

SRE	Sense Condition for Read Error	30C5C
STL REQ	Status Level Request	30A7B
STOP	Stop FF	28B7C
STRA	Shift Typewriter A Character	31C2C
STRB	Shift Typewriter B Character	31C1B
STROBE A	Inhibit Even # Strobe	27A4C
STROBE B	Inhibit Odd # Strobe	27A4D
SU	Shift Upper	30B3C
SWE	Sense Condition for Write Error	30C4D
S1	SIMO 1 Status Level	28D7D
S2	SIMO 2 Status Level	28D6D
S1 REQ	Request for SIMO 1 Status Level	28A6A
S2 REQ	Request for SIMO 2 Status Level	28A7B
TB0	Typewriter Buffer 2^0	29B2A
TB1	Typewriter Buffer 2^1	29B3A
TB2	Typewriter Buffer 2^2	29B4A
TB3	Typewriter Buffer 2^3	29B5A
TB4	Typewriter Buffer 2^4	29B6A
TB5	Typewriter Buffer 2^5	29B7B
TB6	Typewriter Buffer 2^6	29B7A
TDG	Typewriter Data Gate	30D7D
TD0	Typewriter Data 2^0	31C2A/C2D
TD1	Typewriter Data 2^1	31C3A/C3D
TD2	Typewriter Data 2^2	31C4A/C4D
TD3A	Typewriter Data 2^3	31C5B
TD3	Typewriter Data 2^3	31C5E/C5J
TD4	Typewriter Data 2^4	31C6C/C6E
TD5	Typewriter Data 2^5	31C7D/C7F
TD6	Typewriter Data 2^6	31C7A/C7E
TNC	Typewriter N Character	27D8C
TNC/CNC	Typewriter N Character or Clock N Character	27C6E
TERM (P)	Termination for Clock	28B6B

TERM (1N)	Terminate Flip-flop	28C5F
TOP	Typewriter Operable	30D2A/D2D
TOPS	Sense Condition for Typewriter Operable	28C3B
TPOST	TPCO & STOP from Processor	28C8A
TPC 1	Time Pulse Clock 1	27D3D
TPC 13	Time Pulse C1 to C3 FF	27C3F
TPC 2	Time Pulse Clock 2	27C2L
TPC 3	Time Pulse Clock 3	27C4B/B4A
TPC 4	Time Pulse Clock 4	27D2A
TPC 5	Time Pulse Clock 5	27D2B
TPC 6	Time Pulse Clock 6	27D2C
TPC 7	Time Pulse Clock 7	27C5A
TPC 8	Time Pulse Clock 8	27D1A
TS 1	Typewriter Signals 2^0	31A3A
TS 2	Typewriter Signals 2^1	31B4D
TS 3	Typewriter Signals 2^2	31B4A
TS 4	Typewriter Signals 2^3	31A6E
TS 5	Typewriter Signals 2^4	31B6A
TS 6	Typewriter Signals 2^5	31A7A
TYPE-A (N)	Write Instruction to Typewriter	27B8D
TYPE-B N	Write Instruction to Typewriter	27B7D
UC	Upper Case	30D5E/C5B
UCS	Upper Case Shift Command	30A2B
WE (ON)	Write Error F. F.	30C4C

3329

CONTROL MODULE

3329
CONTROL MODULE

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3329 CONTROL MODULE

1.0 Introduction

There are two types of card readers available with the 3301 System; both use the 3329 Control Module. The Model 329 (Uptime) reads up to 1470 CPM and the Model 324 (ICT) reads up to 900 CPM. Both readers use electronic reading. Cards are picked on a demand basis (one instruction, one card) and are read serially column by column. Either 80 or 51 column cards can be read in the Binary or Translate Mode. Both readers have facilities for rejecting cards. The Control Module determines when a Pick command is to be issued, whether the information read from the card is to be translated or accepted in binary form, and whether the card is to be rejected.

1.1 Model 324 Card Reader

The Model 324 Card Reader has a 2000-card capacity input hopper, a 500-card capacity reject stacker, and a 2400-card capacity main stacker. When the "Load" button on the Operator's Display Panel is depressed, two cards are picked by a picker knife and are fed broadside into a waiting station. The cards will remain in the waiting station until a Read instruction is executed. One Pick command is generated when the Read instruction is executed. The Pick command will cause one card to be extracted from the wait station and sent to the read station. Another Read instruction must be executed to cause the second card to be removed from the wait station. The wait station is refilled whenever it is empty. If, after the card is read and a Photo Diode Error or a Data Error has been detected, the card will be placed in the reject stacker. If no errors are detected, the card will be sent to the main stacker. For ease of handling, cards are stacked in the main stacker in groups of approximately 400 cards. Cards may be put in the input hopper and removed from the stackers while the reader is operating.

1.2 Model 329 Card Reader

The Model 329 Card Reader has a 3000-card capacity input hopper and two (2) 2000-card capacity output hoppers. The stacker nearest the input hopper is the normal stacker; the other is the reject stacker. Stackers cannot be selected by program. A card will be put in the reject stacker only if a Data Error or Photo Diode Error is detected.

A single card is picked by the Pick Roller and fed into the read station. The read station has a two column read head. Each column of the read head has 12 photo diodes. Forty photo diodes are used for timing. As the leading edge of the card covers up a timing diode, two consecutive columns on the card are over the read station. Two columns at a time will be strobed from the card and placed in the registers. After the card is read, action must be taken if the card is to be rejected. A metal vane must be positioned so that the card will either go into the normal or the reject stacker.

2.0 General Operation of Model 329 Card Reader

2.1 Picking the Card

When the Control Module wishes to pick a card, it sends a 3 microsecond Pick command to the Card Reader. If the "Clear" button is not depressed, if the "Hold" is not on, if no "Errors" are detected, and a card is not now present ($\overline{PDO}$), the Pick flip-flop will be set. As long as the Pick flip-flop is set, the pick multivibrator will be allowed to oscillate. The 16 MS output from the multivibrator actuates the pick solenoid which jams the rotating pick roller up against the bottom card in the input hopper. If the card is picked and reaches PDO (Card Presence), the AND gate used to set the Pick flip-flop will be inhibited and the Pick flip-flop will be reset. If a card is not picked in three attempts (three oscillations of the multivibrator), a timer will terminate and a Non-pick Error will be generated. This error will inhibit the AND gate and will reset the Pick flip-flop. An operator will have to determine the cause of the "Non-pick", remove the cause, and depress the "Clear" button before the reader can pick more cards.

2.2 Reading the Card

After the card has been picked, it will enter the read area where data will be extracted from the card and gated to the data registers and then to the Control Module. As each timing diode is covered, a set of timing pulses are generated and two columns are read from the card. The outputs of the diodes for the Odd columns on the card are connected directly to the inputs of the Data Register #1. The outputs of the diodes for the Even columns are gated into Data Register #2 by the Read In #2 signal. The Enable Read Out signals apply the outputs of the registers (Data Register #1, then #2) to the AND gates on the bus. When Gate Data Required (GDR) is generated, the data is gated one column at a time to the Control Module.

2.3 Card Reader Errors (Inoperable)

Non-picks, jams, input hoppers empty, or output hoppers full, will render the Card Reader inoperable and will generate "Error." A Non-pick Error will be generated if a card is not picked after three attempts. It indicats that the cards are damaged, warped or that the

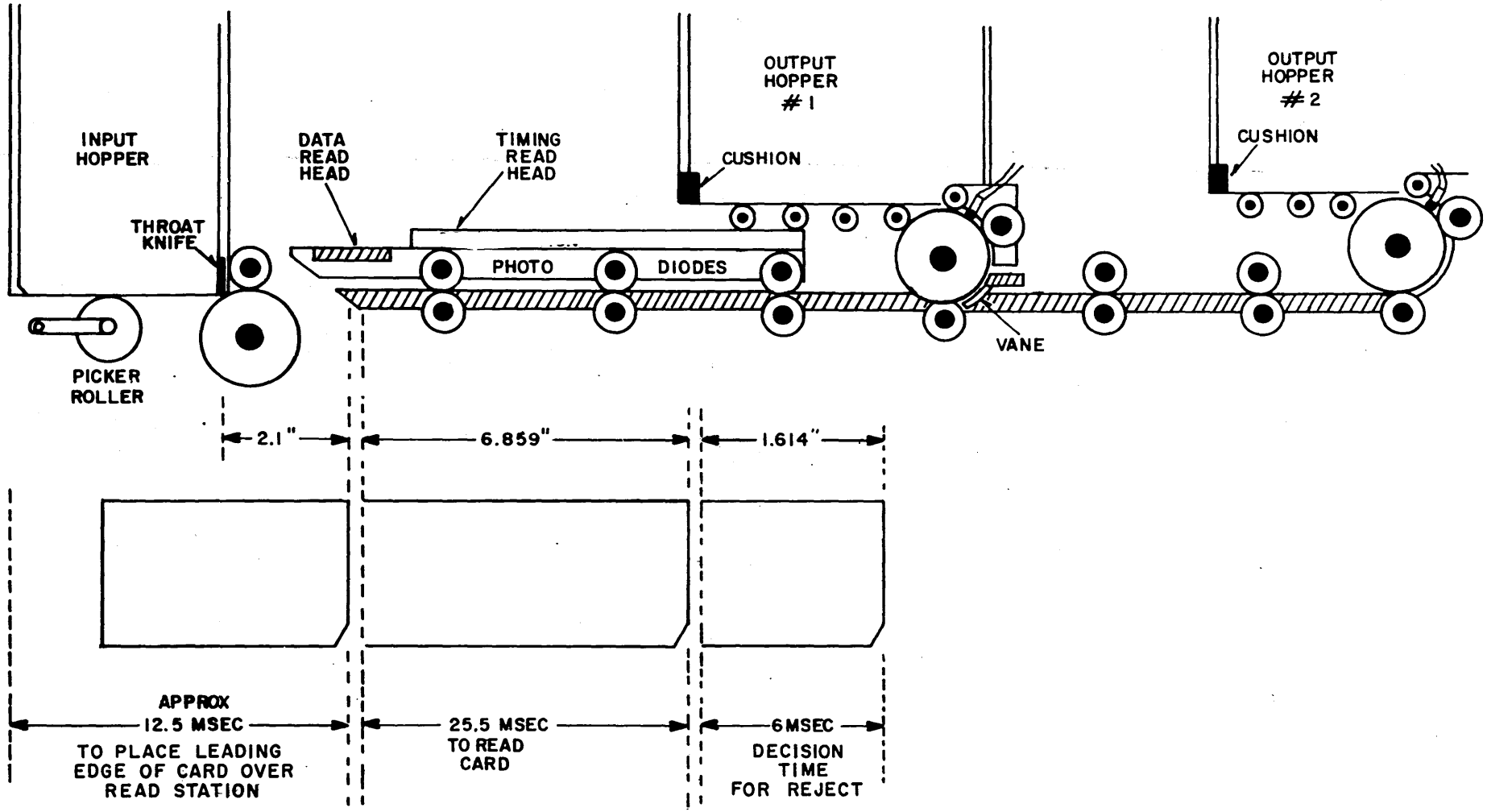


Figure 2-1 329 Card Reader Transport

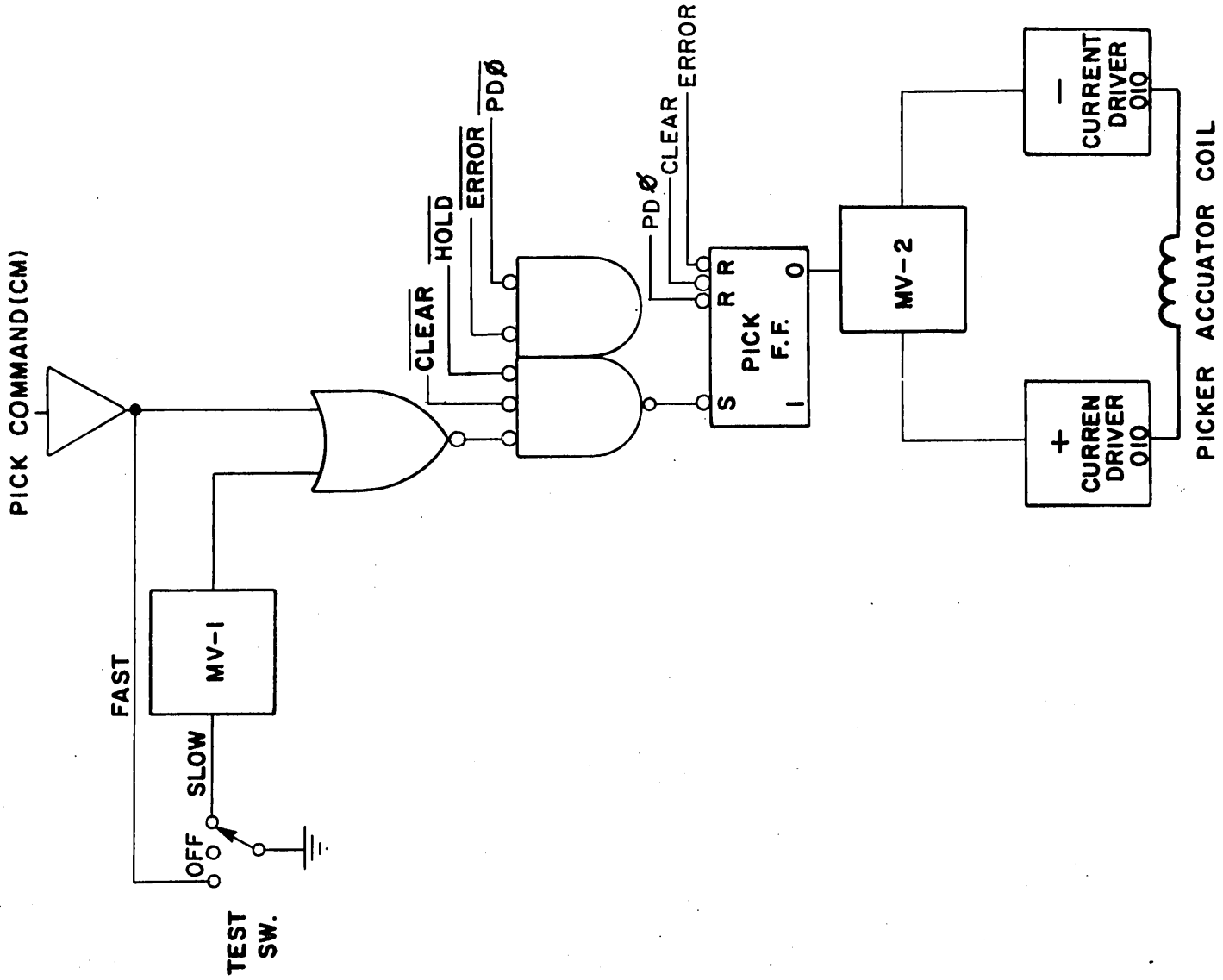


Figure 2-2 Pick Circuitry

picker is improperly adjusted. In all cases, it will take manual intervention to correct the trouble.

For detection of transport jams, cards are timed from the instant Card Presence is generated until they are placed in one of the stackers. Ninety MS is allowed for the card if it is being placed in the normal hopper; 130 MS, if it is being placed in the reject hopper.

Stacker jams are determined by the time it takes to place a card in the stacker. The diode at the input of the normal stacker must not be dark for more than 35 MS or a stacker jam will be detected. The circuitry for the reject stacker allows the diode to be dark for 41 MS before a stacker jam is detected. If either output hopper is full or if the input hopper is empty, the card reader is also inoperable.

2.4 Photo Diode Errors

The data read head photo diodes are tested for proper operation when each card is read. At the beginning of each card a dark check (all diodes should be dark) is made; after the trailing edge of the card, a light check (all diodes should be light) is made. If an error occurs, the PDE signal is sent to the Control Module. The Control Module will respond with a Reject signal and the card will be placed in the reject hopper.

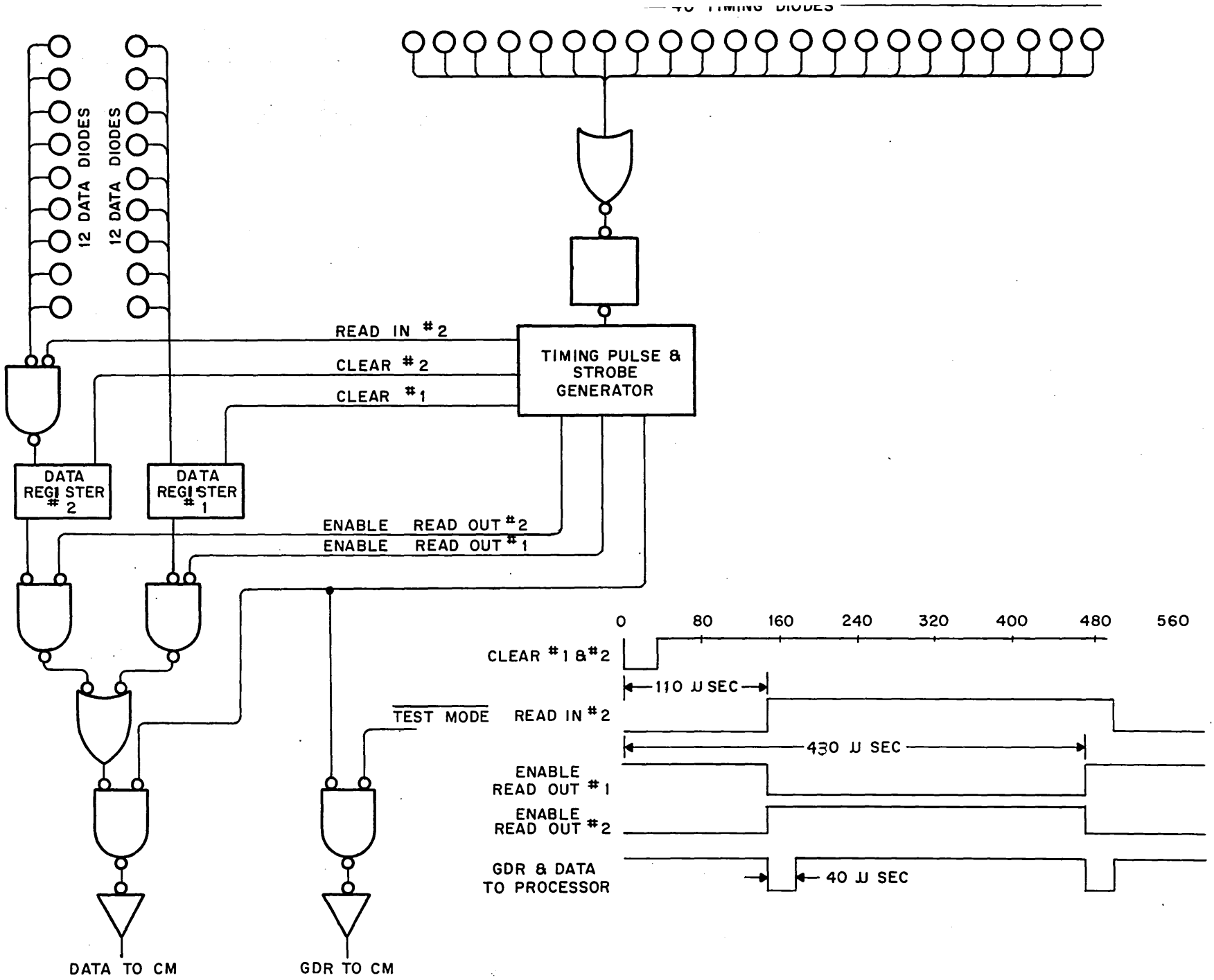


Figure 2-3 Read Circuitry

3.0 Applicable Instructions

The Control Module contains the necessary logic to control the card reader for the following instructions:

Read Forward Simo 1	Read Forward Simo 2
Control Device Simo 1	Control Device Simo 2
Test Device	

3.1 Control Device Instruction (Refer to Fig. 3-1)

The Control Device Simo 1 or Simo 2 instruction prepares the Control Module to read cards in either the Binary or the Translate Mode. When the Control Module is set up for the Translate Mode, each card will be translated character by character from the 12 row EAM card code to RCA 3301 seven bit code. When the Control Module is set up for the Binary Mode, each card column is split into two characters. Parity will be generated for these characters and the result will be placed into memory. When a card is read in the Binary Mode, no converting is necessary. The Control Module will stay in a selected mode until another control device instruction changes it.

FORMAT

Operation = 2 (CD1) or 3 (CD2)

N = - (Minus) if first card reader; J if second card reader

A Address= Must be all zeros (0000)

B Address= B0, B1, and B2 must be zeros (000). If B3 = 0, the Translate Mode will be selected. If B3 = 1, the Binary Mode will be selected.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = (A)i

$(T)_f$ or $(E)_f$ = (B)i

3.2 Read Forward Instruction

A Read Forward Simo 1 or Simo 2 instruction must be executed for each card read. Cards are read in the Binary or Translate Mode as specified by a previous control device instruction. If the Translate Mode was specified, the card columns are automatically translated to RCA

3301 code. If the Binary Mode had been specified, each card column would be split into two characters. Rows 9 thru 4 represent one character with 2^0 bit in row 4. Rows 3 thru 12 represent another character with 2^0 bit in row 12. One hundred-sixty (160) HSM locations must be available if a card is read in the Binary Mode. Refer to Figure 3.1 for an example of how the binary characters are placed in the HSM.

FORMAT

Operation = 4 (RF1) or 5 (RF2)

N = - (Minus) if first card reader; J if second card reader

A Address = HSM location to receive first character. Location must be even.

B Address = Must be all zeros (0000)

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = (A) i + 80 if the Translate Mode had been previously selected OR
(A) i + 160 if the Binary Mode had been previously selected.

$(T)_f$ or $(E)_f$ = (B) i

3.3 Test Device Instruction

The Test Device instruction allows specific conditions of the Card Reader and various indicators in the Control Module to be sensed. This instruction is performed in the normal mode only. If the listed condition(s) is present, a transfer of control to the B Address is performed. If not, the next instruction in the sequence is selected.

FORMAT

Operation = S

N = - (Minus) if first card reader; J if second card reader

A Address = Specifies the test to be performed as follows:

Character	Bit Position	Symbol	Test
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (busy)?
A_0	$2^2 = 1$	4	Is there a Photo Diode Error (PDE)?
A_0	$2^3 = 1$	8	Is there a Multi-Punch Error (MPE)?
A_1	$2^3 = 1$	8	Is the EF Indicator set?

B Address = HSM location of the next instruction to be executed if the condition (s) being tested is (are) present.

FINAL SETTINGS

$(A)_f = (A)\ i$

$(B)_f = (B)\ i$

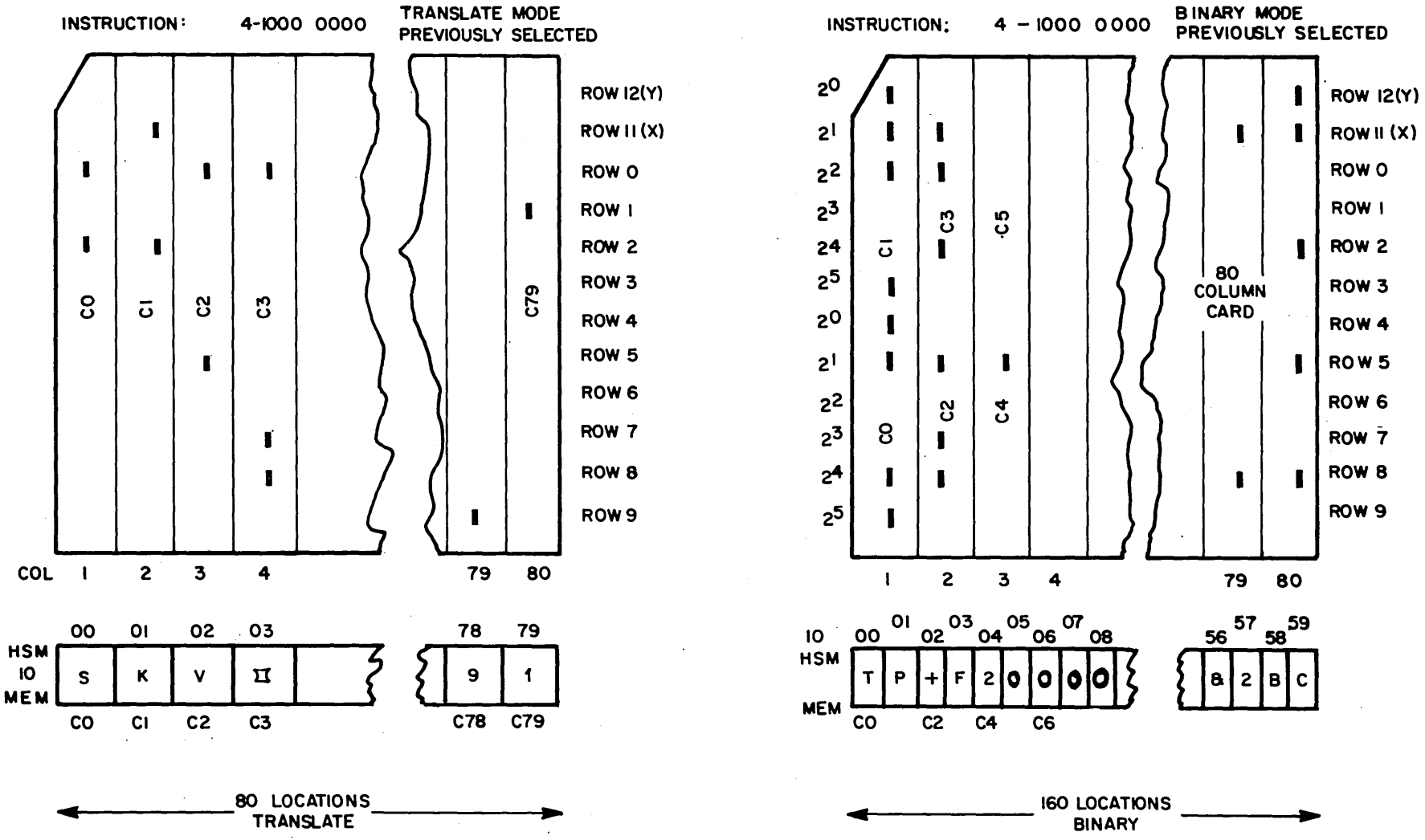


Figure 3-1 Card Formats

4.0 Control Module Operation

4.1 Control Device Instruction

The Control Device instruction will either set or reset the Binary Mode (BM) flip-flop, depending on whether the instruction specifies binary or translate mode.

On print 32 when an N count of - (minus) or J is received by the Control Module and an SIO status level is selected, the Reader N Count (RNC) signal will be generated (32C7E). Note, the Reader N Count signal will not be generated if a Simo 3 instruction is being executed. A Simo 3 instruction cannot be used on the Card Reader. The RNC signal and the IOC (Control Device) signal from the processor are ANDed together and generate a signal, IOC • RNC (32B8A). The IOC • RNC signal will reset the Binary Mode FF (32B6H) and the Simo 2 FF (32B5E).

When the RNC signal is generated, the ONB signal (33C7B) will be gated to the processor. The Operable and Not Busy (ONB) signal will be generated if the Card Reader is Not Busy (CRB) (ON), the Mode is Not Busy (MB), and there are no (inoperable) errors at the Card Reader.

If the instruction being executed is a Simo 2 instruction at TPC2 of the SIO 2 status level, the Sim 2 flip-flop will be set. If the instruction specifies the Binary Mode, OB 10 will be present and the BM flip-flop will be set. If the Translate Mode had been specified, the BM flip-flop would remain reset. The BM flip-flop will remain set until the next Control Device instruction or until General Reset is pressed.

The IOC flip-flop (32B2D) is set at TPC7 of the SIO 2 status level. At the next TPC3 timing pulse, Simo Complete (SCOM 33A6C) and Simo Busy Reset (SBRES 33A6A) will be generated. At the following TPC5 the IOC flip-flop will be reset and the instruction completed.

4.2 Read Forward Operation

4.2.1 Read Forward Initiation

The Reader N Count (RNC) and the Read Forward (RF) signal from the processor are ANDed

together on print 32 and generate RF • RNC. The ONB signal on print 33 is generated and sent to the processor. And if it is a Simo 2 instruction, the Sim 2 flip-flop will set at TPC2 of the SIO 2 status level.

The Card Reader Busy (CRB) flip-flop (32B3E) will be set if the mode is not busy and the Card Reader is not generating (Inoperable) Error. Setting the CRB flip-flop will cause the 3 microsecond Pick (33C6C) command to be generated. After the Card Reader picks the card and it enters the read data area, the Card Presence (CP 33D3B) signal will be generated. The signal is inverted twice in the Control Module and renamed Card Is Present (CIP 33D3C). This signal will be used when the instruction terminates.

When the Card Reader places a character on the bus, it sends a signal, Gate Data Required (GDR), to the Control Module (33D5B). This signal will be used to set the First Character Present (FCP 36D3A) flip-flop and the Pre-Request (P-REQ 33C5C) flip-flop. The Request (REQ 33C2A) flip-flop will be set at the next TPC8. A Simo Request (S REQ 33C3D or C2B) is generated and sent to the processor. The processor will respond with an S1 or S2 (Service) status level. When S1 or S2 is received from the processor, [C-S1/S2] (33D2C or 33D1A) is generated and is used to gate the data from the Control Module to the processor.

The processor must know whether the character is going to be placed in an Even or an Odd memory location. The Strobe A (33B2B) signal indicates that the character will be placed in an Even memory location; the Strobe B (33B1B) signal, an Odd location. The A-ODD flip-flop on print 32 determines whether the character will be placed in an Even or Odd location. Since the initial A Address must be even, the first character read from the card will be placed in an Even location. The Housekeeping or General Reset (HK/GR) signal causes the A-ODD flip-flop to be set. When the P-REQ and REQ flip-flops are set, the A-ODD flip-flop will be triggered to the reset state. When [C-S1/S2] occurs, Strobe A will be generated and the character will be placed in an Even memory location.

If the Control Module is reading binary information, each column on the card will be split into two characters. This means that two characters will be gated to the processor at the same time. Strobe A and Strobe B will both be generated when the Binary Mode (BM) flip-flop is set.

4.2.2 Translate Mode Gating and Accuracy Control

If the Translate Mode has previously been selected, the 12 row character from the Card Reader will be converted to the RCA 7 bit 3301 code before it is sent to the processor. The 12 row character from the Card Reader is received on print 35, area B3 to B7, and is then applied to the translator on print 35. There are two 12 row card codes, Card Code A and Card Code B (see Figure 4-1 for differences). Card Code A is the normal code and is the one that the Control Module is normally set up to receive. That is, on print 34, a jumper from D6A to D6E and D5B to D5C. If Card Code B is being used, there will be jumpers from D6C to D6E and from D5A to D5C.

When an "A" is punched on a card, row 1 and row 4 will be punched. The translator will convert this to D0, D4, and D6 (the 3301 Processor Code for an "A"). To accomplish the conversion, R1 is applied to OR gate D3B and produces D0. The signal RY is applied to OR gate D6E and produces D4. AND gate B7C must be enabled to produce D6. The absence of R8 will make pin 6 low; the presence of RY on OR gate B7A will make pin 7 low; and the presence of R1 on OR gate B6A will make pin 17 low. The output of AND gate B7C feeds OR gate A4A which produces D6.

The output of the translator is applied to two different areas of the data logic on print 35, the section feeding IB0 and the section feeding IB1. If the character is to be placed in an Even location in memory, it will be gated by AND gate D8B into the section of logic feeding IB0. If the character is to be placed into an Odd memory location, it will be gated by AND gate D4A into the section of logic feeding IB1.

The signals applied to AND gates D8B and D4A are INHD, BM, SENSE, and A-ODD. The Inhibit Data (INHD) signal is generated only when an error is detected. The Binary Mode flip-flop will be reset. The SENSE signal will be absent. And if the character is going into an Even location in memory, the A-ODD flip-flop will be reset. The output of AND gate D8A is inverted and causes the translated character to be applied to the inputs of the line drivers going to the processor. When [C-S1/S2] is generated, the character will be gated to IB0.

If a Multi-punch Error or Parity Error is detected, an octal 17 (e) will be sent to the processor in the place of the character received from the Card Reader. When the instruction

RCA 3301 CODES

Printed Symbol	Machine Code	Card Code A
0	00	0
1	01	1
2	02	2
3	03	3
4	04	4
5	05	5
6	06	6
7	07	7
8	08	8
9	09	9
]	12	Space
#	13	3, 8
@	14	4, 8
(	15	5, 8
)	16	6, 8
e	17	7, 8
&	20	Y
A	21	Y, 1
B	22	Y, 2
C	23	Y, 3
D	24	Y, 4
E	25	Y, 5
F	26	Y, 6
G	27	Y, 7
H	30	Y, 8
I	31	Y, 9
+	32	Y, 2, 8
.	33	Y, 3, 8
;	34	Y, 4, 8
:	35	Y, 5, 8
'	36	Y, 6, 8
C_R	37	Y, 0
-	40	X
J	41	X, 1
K	42	X, 2
L	43	X, 3
M	44	X, 4
N	45	X, 5
O	46	X, 6
P	47	X, 7
Q	50	X, 8
R	51	X, 9
[	52	X, 2, 8
$	53	X, 3, 8
*	54	X, 4, 8
>	55	X, 5, 8
<	56	X, 6, 8
10	57	X, 7, 8
"	60	X, 0
/	61	0, 1
S	62	0, 2
T	63	0, 3
U	64	0, 4
V	65	0, 5
W	66	0, 6
X	67	0, 7
Y	70	0, 8
Z	71	0, 9
÷	72	0, 2, 8
,	73	0, 3, 8
%	74	0, 4, 8
↑	75	0, 5, 8
=	76	0, 6, 8
¤	77	0, 7, 8

Differences Between Card Code A and Card Code B

Printed Symbol	Machine Code	Card Code A	Card Code B
&	20	Y	Y, 0
-	40	X	X, 0
C_R	37	Y, 0	Y
"	60	X, 0	X

Figure 4-1

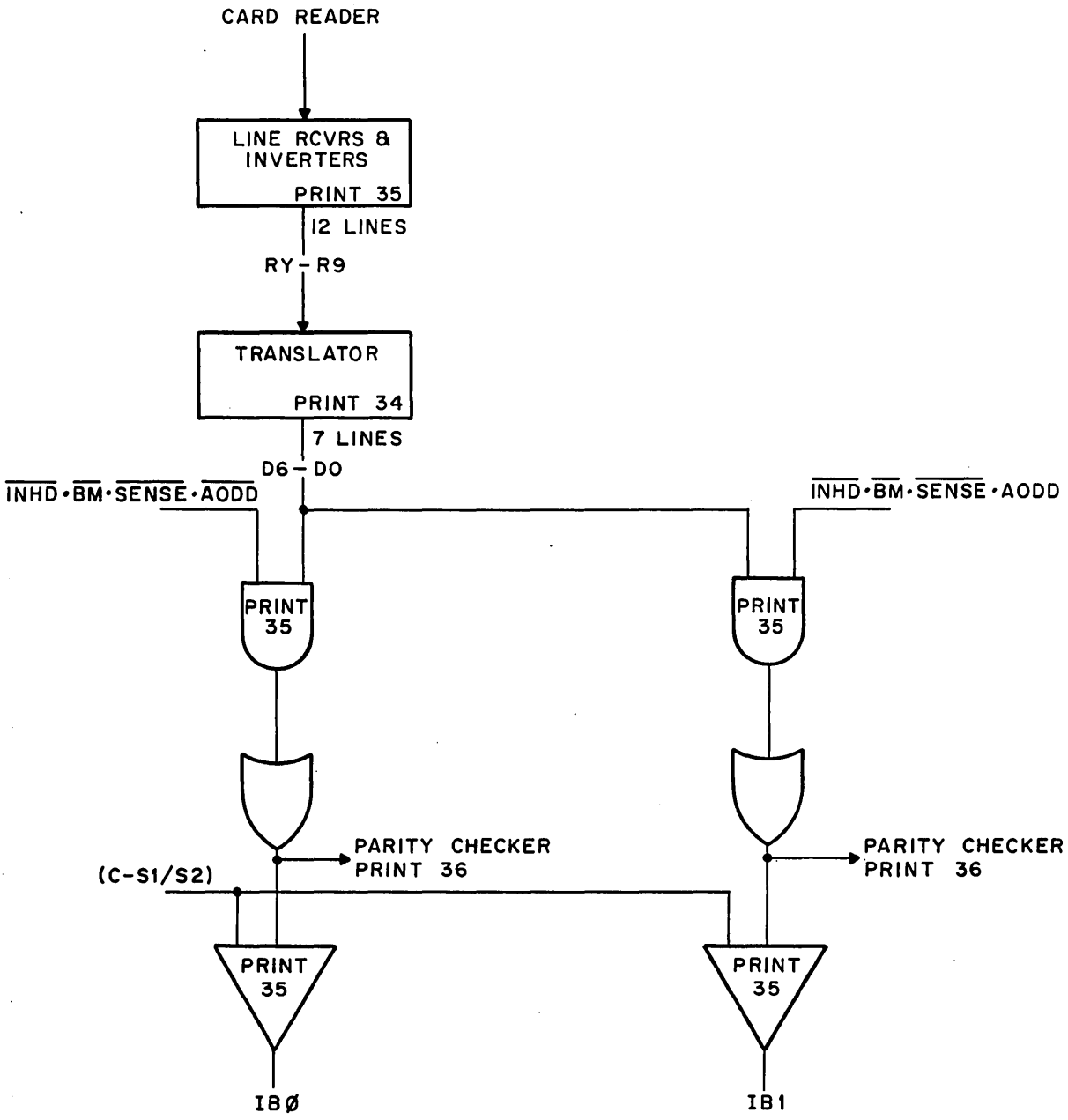


Figure 4-2 Data Logic Translate Mode

terminates, a Reject command is sent to the Card Reader.

A Multi-punch error is generated on print 34 when an illegal code character is received from the Card Reader. As an example, if only row 2 and row 8 are received from the Card Reader, AND gate 34C3C will be enabled and an MPE will be generated. The MPE signal will set PE0 and PE1 on print 36.

If the data being applied to the inputs of the bus drivers for IB0 and IB1 on print 35 contains bad parity, the PE0 or PE1 flip-flop will be set. The PE0 flip-flop would be set if there is a parity error on the data waiting to be gated to IB0.

When either PE0 or PE1 is set, AND gate 36C7E generates INHD which prevents the output of the translator from being gated (gates 35D8B and 35D4A) to the bus drivers for IB0 or IB1. The Data Error (DE) flip-flop will be set and the Card Error Lamp on the console will light. The Reject flip-flop will be set when the Card Read instruction terminates. Whenever PE0/1 is generated in the Translate Mode, AND gates 35C8C or 35C2E will be enabled and an octal 17 will be generated for IB0 or IB1.

4.2.3 Binary Mode Gating and Accuracy Control

In the Binary Mode each column read from the card is split into two characters. Row 9 thru 4 is one character; row 3 thru Y is the other. These two characters are then gated simultaneously to the processor.

The outputs of the line receivers from the Card Reader, rows 9 thru 4, are fed to the top of print 35 as six bits of a character. The seventh bit of the character is supplied by the parity generator 34D8A. Rows 3 thru Y are handled similarly and generate a character for IB1. If Inhibit A Character (INH AC) and INH BC are not present, the two characters will be supplied to the inputs of the bus drivers. When $\overline{C}$-S1/S2 is generated, the two characters will be gated to the bus.

If the characters being applied to the inputs of the bus drivers contain bad parity, either PE0 or PE1 will be set. Whenever PE0 or PE1 is set, INH AC (Inhibit A Character) or INH BC will be generated. This will prevent the defective character from being sent to the processor. An octal 17 (e) will be sent in its place (AND gate 35C8A or 35C2E). The Data Error (DE)

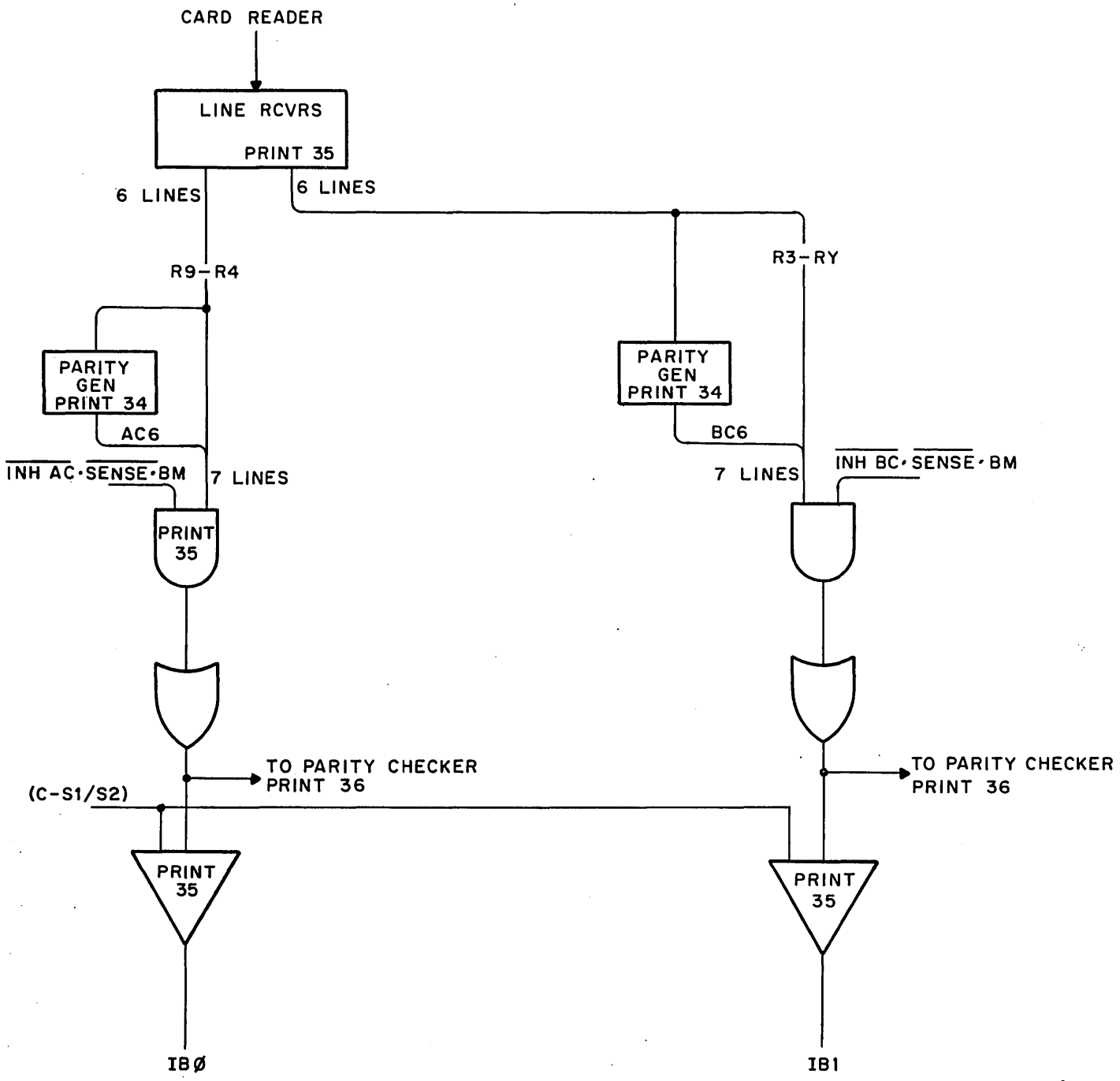


Figure 4-3 Data Logic Binary Mode

flip-flop will be set and the Card Error (CE) lamp on the console will light. At the termination of the Read instruction, the Reject flip-flop will be set and the card will be rejected.

4.2.4 PDE Logic

The data read head photo diodes in the Card Reader are tested for proper operation when each card is read. At the beginning of each card, the diodes are tested to insure that they are all dark. After the trailing edge of the card, all of the diodes are checked to see that they indicate light. If an error occurs, the Photo Diode Error (PDE) signal is sent to the Control Module. When the PDE flip-flop (33C5B) is set, the ME1 indicator on the console will light. When the Read instruction terminates, the Reject flip-flop (36C5D) will be set and the card will be placed in the reject stacker.

4.2.5 DNF Logic

If, while reading a card, the Card Reader becomes inoperable (transport jam, stacker jam, non-pick, etc.), it will send an Error signal to the Control Module. The Error signal sets the DNF flip-flop (33C7C). The DNF flip-flop causes the DNF indicator on the console to light and the Read instruction to terminate abnormally.

4.2.6 Detecting End File

The Control Module contains the necessary logic to detect an EF card. An EF card contains the "<" symbol in the first character position, and the remainder of the card is blank. In the Translate Mode, the card contains X-6-8 punches in column 1 and no punches in columns 2 thru 80. In the Binary Mode, the card contains 9-7-6-5 punches in column 1 and no punches in columns 2 thru 80.

The EF flip-flop (33A4B) will be set when the Character Counter (CC1) flip-flop is reset, the "<" symbol is detected, and PC10 to PC15 contains zeros. The CC1 flip-flop (36C2A) will remain reset until after the first character is read in. Then it is set and remains set until the next Read instruction is initiated. It cannot be triggered to the reset state because the "O" output will hold the trigger input high. In the Translate Mode, PC10 thru PC15 will always be zeros when the first character is read in. In the Binary Mode, each column on

the card contains two characters. If the second character, rows 3 thru Y, contain no punches, PC10 to PC15 will be zeros. The EF flip-flop must remain set until after the Read instruction terminates and a Sense instruction has been performed. If any punch is detected on the remainder of the card, the EF flip-flop will be reset and the card will be handled as normal data. If no additional punches are detected, the Read instruction will terminate abnormally. A Sense instruction is then executed to determine that an EF card was read.

4.2.7 Read Forward Termination

A Read instruction will terminate either normally or abnormally. If the instruction terminates normally, Simo Busy Reset (SBRES) and Simo Complete (SCOM) will be generated. If the instruction terminates abnormally, a PDE, DNF, DE, or EF has occurred; Simo Busy Reset (SBRES) and Simo Requires Attention (SRA) will be generated.

When a card has been completely read, the Card Is Present (CIP-P) signal on AND gate 36C3B will go negative and enable the gate. The FCP flip-flop was set when the first character was gated to the Control Module. After 250 microseconds, the Pre-End (P-END) flip flop will be set. And at the next TPC1, the End flip-flop will be set. The 250 microsecond delay is provided so that the Card Reader's photo diode "light check" can be made before the Read instruction terminates.

The presence of P-END and END on AND gate 33B7B will generate the signal, Terminate (TERM). Terminate will cause the Simo Busy Reset (SBRES) signal to be generated and will cause the SRA signal or the SCOM signal to be generated. If a PDE, DNF, DE, or EF is present at termination, the signal ALARM, output of AND gate 33B7C, will set the SRA flip-flop and will inhibit the generation of SCOM. If no conditions requiring the generation of SRA are present, AND gate 33B6A will be enabled and SCOM will be generated. At TPC4 while the End flip-flop is set, the Card Read Busy (CRB 32B3E) flip-flop will be reset.

4.3 Test Device Instruction Operation

The Test Device instruction is performed only in the normal mode. It is used to test the EF, CRB, DE, and PDE flip-flops and the (Inoperable) Error from the Card Reader.

The Input/Output Sense (IOS) signal from the processor and the RNC signal are ANDed together at gate 33D4A and produce SENSE. The SENSE signal gates the EF, CRB, DE, and PDE flip-flops and the (Inoperable) Error signal to the inputs of the bus drivers on print 35. The appropriate bus drivers on print 35 will be enabled by AND gate 35C8E. The processor, using this information, determines what instruction should be performed next.

4.4 Status Flow

CONTROL DEVICE

INSTRUCTION: NOR = 2 or 3 N = - or J A = Must be zeros
B = B0, B1, B2 must be zeros. If B3 = 1 Binary Mode will be selected; if B3 = 0 Translate Mode will be selected.

SIO 1

Following events occur during this status level:

Set SIO flip-flop
Generate RNC if (Processor N Count is a - or J) $\cdot \overline{SOP3}$
Generate ONB if RNC $\cdot$ (IOS + $\overline{CRB} \cdot \overline{MB} \cdot \overline{ERROR}$)
Reset BM and SIM 2 if $[IOC \cdot RNC] \cdot \overline{CRB}$

SIO 2

TPC 2 - Set SIM 2 flip-flop if $[IOC \cdot RNC] \cdot \overline{CRB} \cdot SOP2$
Set BM flip-flop if $[IOC \cdot RNC] \cdot \overline{CRB} \cdot OB10$

TPC 7 - Set IOC flip-flop if $[IOC \cdot RNC] \cdot \overline{MB} \cdot \overline{ERROR} \cdot \overline{CRB}$

TPC 8 - Reset SIO flip-flop

After SIO 2

TPC 3 - Generate SBRES 1 if IOC $\cdot \overline{SIM\ 2}$
Generate SBRES 2 if IOC $\cdot$ SIM 2
Generate SCOM 1 if IOC $\cdot \overline{SIM\ 2}$
Generate SCOM 2 if IOC $\cdot$ SIM 2

TPC 5 - Reset IOC

READ FORWARD

INSTRUCTION: NOR = 4 or 5 N = - or J A = Location for first character. Must be even. B = Must be all zeros (0000).

SIO 1

Following events occur during this status level:

Set SIO flip-flop
Generate RNC if (Processor N Count is a - or J) • $\overline{\text{SOP3}}$
Generate ONB if RNC (IOS + $\overline{\text{CRB}}$ • $\overline{\text{MB}}$ • $\overline{\text{ERROR}}$)
Generate HK/GR

SIO 2

TPC 2 - Set SIM 2 flip-flop if [RF • RNC] • $\overline{\text{CRB}}$ • SOP2

TPC 4 - Set CRB flip-flop if [RF • RNC] • $\overline{\text{MB}}$ • $\overline{\text{ERROR}}$

TPC 8 - Reset SIO flip-flop

First Column Read From Card

Set P-REQ and FCP flip-flop if CRB • GDR

TPC 8 - Set REQ flip-flop if P-REQ
Generate SREQ

TPC 1 - Trigger A-ODD if P-REQ • REQ

TPC 4 - Generate GATE PE if REQ
Reset P-REQ

Pg 25

S - STL

Generate [C-S1/S2] if CRB • (S1 • $\overline{\text{SIM2}}$ + S2 • SIM2)
Generate STROBE A if [C-S1/S2] • ($\overline{\text{A-ODD}}$ + BM)
Generate STROBE B if [C-S1/S2] • BM
Strobe Data to Bus if [C-S1/S2]
Reset REQ if [C-S1/S2]

Last Column Read from Card

Set P-REQ if CRB • GDR

TPC8 - Set REQ flip-flop if P-REQ
Generate SREQ

TPC1 - Trigger A-ODD if P-REQ • REQ

TPC4 - Generate GATE PE if REQ
Reset P-REQ

S - STL

Generate [C-S1/S2] if CRB (S1 • $\overline{\text{SIM2}}$ + S2 • SIM2)
Generate STROBE A if [C-S1/S2] • BM
Generate STROBE B if [C-S1/S2] • (A-ODD + BM)
Strobe Data to Bus if [C-S1/S2]
Reset REQ if [C-S1/S2]

Card No Longer Present

Trigger P-END after 250 microseconds if FCP (IN) • $\overline{\text{CIP}}$ • CRB

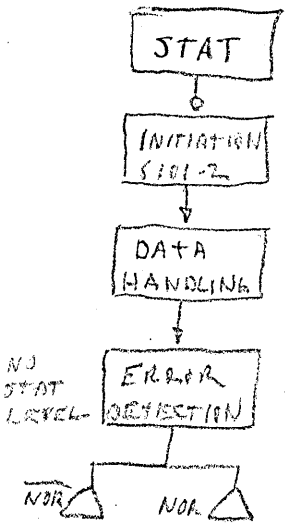
TPC 1 - Set END if P-END
Generate TERM if P-END • END
Generate ALARM if TERM •[PDE + DNF + DE + (TERM • EF • $\overline{\text{IOC}}$)]
Set SRA if ALARM

TPC 3 - Generate SBRES1/2 if TERM • (SIM2 + $\overline{\text{SIM2}}$)
Generate SRA1/2 if SRA • (SIM2 + $\overline{\text{SIM2}}$)
Generate SCOM1/2 if TERM • ALARM • (SIM2 + $\overline{\text{SIM2}}$)

TPC 4 - Reset CRB if END • $\overline{\text{SIO}}$

TPC 5 - Set REJECT if (DE + PDE) • $\overline{\text{IOC}}$ • TERM

TPC 8 - Reset P-END



PROC

S101

SET INH REQ

(A) → S,C,F REG A3,A5R

NOR+N S3R,S4R,S5R

N → ALL CONTROL MODULES

FUNCTION → ALL CM

SB1,SB2 → ALL CM

SOP → ALL CM

S102

(B) → T, E,G REG, B3,A5R

CHK ADD EQ

$\overline{\text{ONB}}$ INT 11

SET MODE BUSY

RESET INHIB REQ

SET SRF/SRR/SW/SER

CM

S101

SETS101 READ/IOC/IOS

GEN RNC +.

GEN HK (SET A ODD)

RAISE ONB

S102

SET SIM2 IF SOP2

SET BUSY

" PICK

RESET S10

SOP1 = NORO NOR+

SOP 2 = NORO

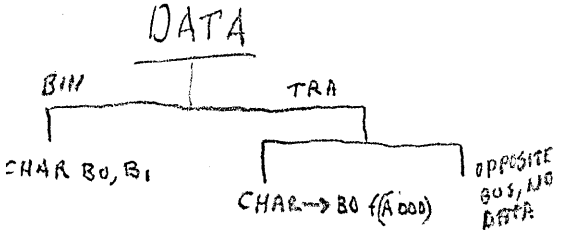
P 4-18

4.5 Control Module Source & Abbreviation List

AC6	Parity bit for Binary Character A	3506834 D8A
ALARM	Abnormal condition requiring computer action	33B7C
ALI	Alarm Inhibit	32D1A
A ODD	Address Odd location in memory	32B7F
AR	Alarm Reset	32D2B
BC6	Parity bit for Binary Character B	34C8A
BM	Binary Mode	32B6H
CC1	Character Counter One	36C2A
CE	Card Error	36B7A
CIP	Card Is Present	33D3C
CLEAR	Clear CR of errors (not used on 329 CR)	33C6D
CRB	Card Reader Busy	32B3E
C-S1/S2	An S1 or S2 status level has been generated	33D2D
DE	Data Error	36C7H
DE/PDE	Data Error/Photo Diode Error	36D5A
DNF	Device does not follow	34D7B
D0		34D3A
D1		34D4D
D2		34D5E
D3	Data bits from Translator	34D5C
D4		34D6E
D5		34D7B
D6		34A4A
EF	End File	33A4B
END	End of a Read Instruction	36A3A
ERROR	An inoperable error from CR	33D7B
GATE PE	Gate Parity Error	34B1A
GDR	Gate Data Required	33D5B
GR	General Reset	32D2A
HK/GR	House Keeping or General Reset	33C8A

HK/AR	House Keeping or Alarm Reset	33C8B
INHAC	Inhibit A Character	36B8A
INHBC	Inhibit B Character	36B6A
INHD	Inhibit Data	36C7E
IOC	Input/Output Control	32B2D
IOC • RNC	Input/Output Control & Reader N Count	32B8A
IOS	Input/Output Sense	32D3B
IPABO		35D4A
IPAB1		35D8B
MB	Mode Busy	32B4D
ME1	Miscellaneous Error #1	33C5D
MPE	Multi-punch Error	34B2B
NO PUNCH	No Punch on Card	34D4A
NUM	Number	34D2B
OB 10	Output Bus 10	32D4B
ONB	Operable & Not Busy	33C7B
PC00 to PC06	Even Character Bits	35C5 to C7
PC10 to PC16	Odd Character Bits	35C1 to C4
PDE	Photo Diode Error	33C5B
PE0	Parity Error for Even Character	36C7F
PE0/1	Parity Error for Even or Odd Characters	36D7A
PE1	Parity Error for Odd Character	36C6D
PICK	Command sent to Card Reader	33C6C
P-REQ	Pre-Request	33C5C
REJECT	Command sent to Card Reader	36C5D
RES SIM2	Reset Sim 2 flip-flop	32B6D
REQ	Request	33C2A
RF • RNC	Read Forward & Reader N Count	32B7A
RNC	Reader N Count	32C7E
RX/RY	X or Y Punch on Card	34B7A
RO to RY	Rows from Card Reader	35A3-A7
R1/R2/R4/R7	Row 1 or Row 2 or Row 4 or Row 7 punched on card	34BCA

SBRES-1	Simo Busy Reset-1	33A6A
SBRES-2	Simo Busy Reset-2	33A6B
SCRB	Sensed Card Reader Busy	33C3A
SCOM-1	Simo Complete-1	33A6C
SCOM-2	Simo Complete-2	33A5A
SDE	Sensed Data Error	33C3B
SEF	Sensed EF	33C4B
SENSE	Sense	33D4C
SER	Sensed Error	33C4B
SET FCP	Set First Character Present Flip-flop	33D5C
SIM 2	Simultaneous Mode 2	32B5E
SIO	Start Input/Output	33B3C
SIO 1	Start Input/Output status level 1	32D5C
SIO 2	Start Input/Output status level 2	32D4A
SOP 2	Simultaneous Operation	32D3A
SPDE	Sensed Photo Diode Error	33C3C
SRA-1	Simult. Requires Action-1	33A8A
SRA-2	Simult. Requires Action-2	33A7A
SREQ 1	Simo 1 Request	33C3D
SREQ 2	Simo 2 Request	33C2B
STROBE A	Used in memory storage	33B2B
STROBE B	Used in memory storage	33B1B
S1	Simo 1 service status level	32C2C
S2	Simo 2 service status level	32C1A
TERM	Terminate a Read Instruction	33B7J
TPC0 to TPC8	Timing pulses	32C2 to C5



GDR

PRE REQ

REQ → SET S1/S2 REQ
INH NG
@ TPCO SET S1/S2

S1/S2

C.M.

RECOGNIZE SCRFICE STL
STROBE A/B/(AB)
CHAR B0/B1/(B0 B1)
RESET REQ

S1/S2 PROC

S,C, F Reg → MAR

GEN CM

INH 1/2 char.
Bus → MPR 1/2 char
Bus adder → Bus
T,E,G → SPMR
F BUS = SPMR SETAE
Bus adder → SCF

SENSE TERM COND:

ABNORM NORM
DNF AE
BLOCK
EF, EO
CAL B0

SET PRE END → END → TERM
RESET SB1/SB2 / SCOM1/SCOM2
RA1.2
4-18 RESET CBUSY

3333 - 3335
CONTROL MODULE

3333/3335
CONTROL MODULE-BUFFER

3333/3335 CONTROL MODULE-BUFFER

TABLE OF CONTENTS

1.0 Introduction

The Model 3333/3335 Control Module-Buffer permits the 3301 Processor to be connected to the 333/335 On-Line Printer. The Control Module works with the buffer logic and BPU, whereas the buffer logic works in conjunction with the Printer and CM.

1.1 Printer

The Printer may operate at a nominal printing speed of 1000 lines per minute in the synchronous mode and 800 lines per minute in the asynchronous mode. A line may contain either 120 or 160 characters, depending on the printer type.

In asynchronous printing, all 64 symbols on the print drum may be printed in one drum revolution with paper advance occuppying a portion of the next revolution. In synchronous mode, only 47 symbols on the drum may be printed since a complete line of print and a single line paper advance are accomplished during one drum revolution. Those symbols excluded from print during synchronous mode are positions 16 thru 32 of the Standard Print Table. (Table 1.1) A paper tape loop is provided so that paper advancing may be controlled directly by instruction or in conjunction with the paper tape loop. Paper advancing includes advancing a specified number of lines, vertical tabbing, or page changing.

In addition to working with the BPU, the Buffered Printer has the capability (via a maintenance panel) to print off line a prestored line of print data.

1.2 Control Module-Buffer

The Control Module-Buffer contains the necessary logic to effect the data transfer from the BPU to the Buffer core memory; to effect the scan of the data in core and print the appropriate character on the On-Line Printer; to initiate Paper Advance; and to sense for errors and inoperable conditions.

1.2.1 Control Module

The Control Module consists of 3 rows of logic mounted in the 3301 standard I/O rack with power supplied by the BPU. A maximum of two buffered printers may be used with any

Table 1.1

Table* Position	Character	Printed Symbol	Table* Position	Character	Printed Symbol
1	Minus	-	33	A	A
2	Plus	+	34	B	B
3	Space		35	C	C
4	Zero	0	36	D	D
5	One	1	37	E	E
6	Two	2	38	F	F
7	Three	3	39	G	G
8	Four	4	40	H	H
9	Five	5	41	I	I
10	Six	6	42	J	J
11	Seven	7	43	K	K
12	Eight	8	44	L	L
13	Nine	9	45	M	M
14	Comma	,	46	N	N
15	Period	.	47	O	O
16	At the Rate of	@	48	P	P
17	Percent	%	49	Q	Q
18	Colon	:	50	R	R
19	Number	#	51	S	S
20	Dollar Sign	$	52	T	T
21	Close Parenthesis	)	53	U	U
22	Quotation Mark	"	54	V	V
23	Subscript$_{10}$	10	55	W	W
24	Open Parenthesis	(	56	X	X
25	Close Bracket	]	57	Y	Y
26	Semicolon	;	58	Z	Z
27	Greater	>	59	Credit	C_R
28	Divide	÷	60	Apostrophe	'
29	Up Arrow	↑	61	Asterisk	*
30	Open Bracket	[	62	Ampersand	&
31	Less	<	63	Virgule	/
32	Equal	=	64	Lozenge	✧

*Table positions correspond to print positions on the Drum.

3301 system. However, each requires a separate Control Module and at no time is it permissible to pair a Buffered Printer with an Unbuffered Printer. Each Control Module is activated during a WRITE instruction upon recognizing its assigned N count similar to all control modules in the system.

1.2.2 Buffer

The Buffer consists of a separate rack of logic containing seven rows of plug-ins, a 184 or 224 character core memory, and an independent power supply. The Buffer memory contains a 64 character table area and a 120 or 160 character data (field) area. Memory access time is 8 microseconds and is diad oriented, i.e., each memory cycle stores or extracts two characters.

The Buffer logic is activated by the Control Module. Once initiated, data transfer from the BPU is upon request by the Buffer via the Control Module until either the table area is loaded or the data area is loaded, depending upon the instruction being performed. Immediately upon filling the data area of the Buffer memory, the Processor is released and the Buffer performs the necessary scan, print and paper advance.

2.0 Applicable Instructions

Two instructions are used with the Buffered Printer. They are WRITE and TEST DEVICE. A Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction in conjunction with the "B" Address is used to transfer the table from BPU HSM to the Buffer memory, to transfer a line of print characters from BPU HSM to the Buffer memory for print and Paper Advance or Paper Advance Only without print. Error Free Operation causes termination of each instruction with SCOM, whereas, Errors causes an SRA termination.

	SCOM	SRA
SIMO 1	INT 17	INT 14
SIMO 2	" 16	" 13
SIMO 3	Not used with On-Line Printer	

The Test Device Instruction (TDV) tests the status of the Printer and transfers control if the condition (s) being tested is (are) present.

2.1 Write Instructions

2.1.1 Load Buffer Table

A Write instruction in SIMO 1 or 2 (NOR = 8 or 9) with B_1 2^0 and B_3 2^2 present signify no print and transfer to table respectively. The "A" Address indicates the location of the first character in the BPU HSM to be transferred. A_3 must always be even. The print table in the BPU may be located in any 64 contiquous HSM locations provided the first table character is in the first position of a diad.

The instruction terminates after 64 characters have been transferred.

2.1.2 Paper Advance (Only)

The Write instruction may specify Paper Advance Only without printing by placing paper advance information in the B portion of the address, making B_1 2^0 a One, signifying no printing; and B_3 all Zeros, indicating no HSM to Buffer transfer.

2.1.3 Print and Paper Advance

The Write instruction transfers 120 or 160 characters from BPU HSM to the Buffer memory, prints one line and advances paper. Synchronous or asynchronous mode and line size 120 or 160 characters must be specified by the B_1 and B_3 characters of the address. Paper advancing is controlled by the line count contained in B_2 or by paper tape loop.

Table 2.1 shows the significance of the "A" and "B" Addresses used with the Write instruction.

Table 2.1 Write Instructions 3301 OLP

WRITE INSTRUCTIONS

1. Print & Paper Advance Instruction
2. Paper Advance Only Instruction
3. Table to Buffer Instruction

FORMAT

		A_0 A_1 A_2 A_3	B_0 B_1 B_2 B_3
NOR	N		
8/9	Q/R	X X X X	X X X X

NOR	8	Simo 1
	9	Simo 2
N	Q	Printer #1
	R	Printer #2

INSTRUCTIONS

	Print & Paper Advance	Paper Advance Only	Load Buffer Table
A_0 - A_3	First CHAR to be printed A_3 must be even	Must be zeros	First CHAR of BPU HSM Print Table A_3 must be even
B_0 - $1(2^0)$	Paper Advance as specified by count in B_2	Paper Advance as specified by count in B_2	B_0 must be zero
$2(2^1)$	Loop controlled Vertical Tab	Loop controlled Vertical Tab	
$4(2^2)$	Loop controlled Page Change	Loop controlled Page Change	

B_1 - 0	Asynchronous Mode	——	——
$1(2^0)$	——	No Printing	No Printing
$2(2^1)$	Synchronous Mode	——	——
B_2 (0 - 15)	Number of lines to advance paper	Number of lines to advance paper	B_2 must be zero
B_3 - 0	——	No HSM —— Buf. Trans.	——
$1(2^0)$	Print 120 Char.	——	——
$2(2^1)$	Print 160 Char.	——	——
$4(2^2)$	——	——	Specifies Print Table

2.2 Testing the Device

FORMAT

OPERATION - S
N - Q if first Printer, R if second Printer.
A Address - Specifies function to be performed as follows:

Character	Bit Position	Symbol	Test or Reset Function
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a low paper supply?
A_0	$2^3 = 1$	8	Is there a parity error (PE)?
A_0	$2^4 = 1$	&	Is the paper advancing?
A_1	$2^0 = 1$	1	Is Buffer available?
A_2	$2^3 = 1$	8	Resets PE Indicator.
A_3	$2^0 = 1$	1	Resets Buffer Available Indicator.

Unused characters must be zeros and are not to be used by programming.

B Address - HSM location of the next instruction to be executed if the condition (s) being tested is (are) present.

3.0 Operation

The operation of the 3333/3335 Control Module-Buffer will be explained by instruction, i.e., Load Table, Print and Paper Advance, and Paper Advance Only. Figure 3.1 indicates the relationship between BPU, CM, Buffer and Printer and indicates the associated logic print numbers.

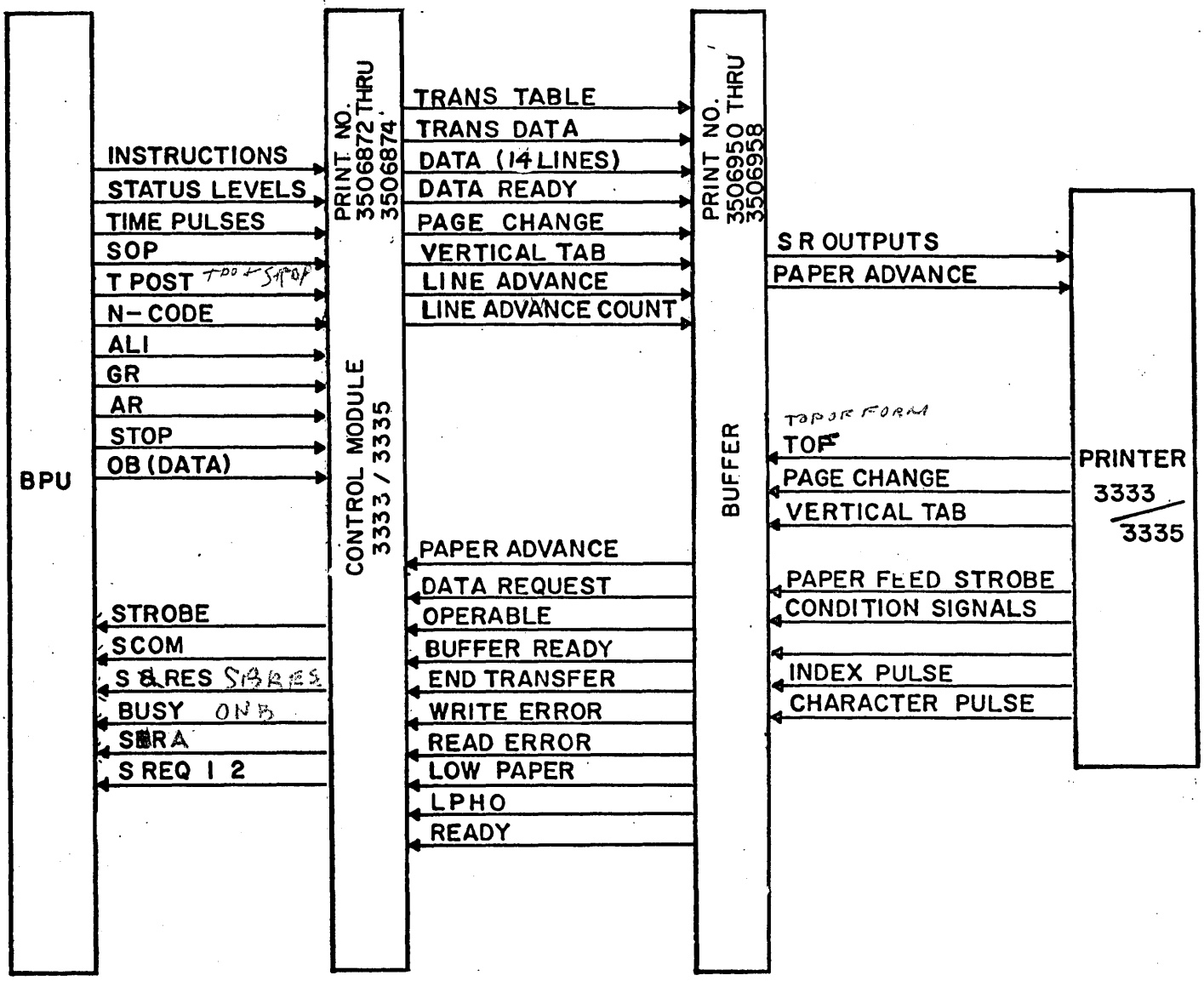


Figure 3.1 Block Relationship

3.1 Control Module - Reference Print Nos. 3506872 thru 3506874

The Control Module is activated during the SIO1 and SIO2 status levels which follow an I/O instruction. During these two status levels, the significant addresses (A and B), the OP code, and the N-count are stored in reserved scratch pad locations if the addressed Control Module is not busy. In addition, a copy of NOR is transferred to the appropriate SOR, Hardware Register, and the OP level and N-count are transmitted to all control modules.

3.1.1 SIO1

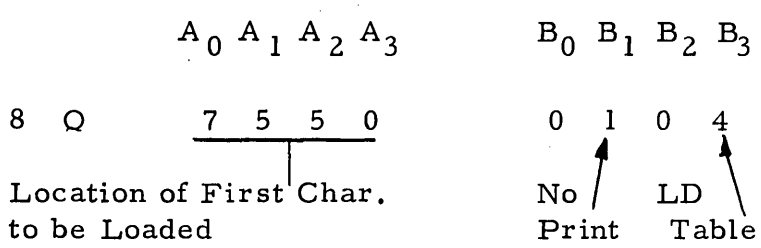
During SIO1 of a Printer instruction, N is a Q or R (Printer 1 or 2) and recognized by gates on print 3506873, area D3 (73/D3). Pin 9 of D4D is low from TPC1 time of SIO1, provided the CM is operable and not busy. Refer to gate 73/C4D. The receivers for the N-lines are on 72/C7. Notice that N0 and N6 may be altered by jumpers to satisfy the Q or R designation and permit gate 73/D3, which in turn generates N-COUNT-N from 73/D3E. N-COUNT-N and WRITE at 73/D8A produces P-ADD-N and enables 73/D7A to generate HOUSECLEANING and GENERAL RESET. Had the Control Module been busy or inoperable when its N-count was recognized, transmitter 73/C5F would be inhibited due to 73/C5E being enabled (assuming this was a Write instruction and not an I/O Sense) and the signal ONB (73/C5F), a low, would set the INTERRUPT 11 flip-flop in the BPU.

3.1.2 SIO2

TPC 1 - During the SIO2 status level, the P-BUSY flip-flop (73/B8B) is Set (73/C8). Pin 17 of 73/D6B, LPHO-0N (Line Printer Hold Off) from flip-flop 73/A6B only goes Set if the Buffer rack has been placed in the LOCAL mode.

TPC 2 - At TPC2 time of SIO2, the B^2 and B^3 characters of the address are sensed to Set the control flip-flops at the bottom of print 74. The Scratch Pad Memory Register is gated to the Bus via 05/C2B (BPU) at TPL1 time. This places SPMR2 and SPMR3 on the I/O BUS0 and 1 respectively for the duration of TPL1 (leading edge of TPC1 time until the trailing edge of TPD2).

Assume the following instruction has been staticized.



From Table 2.1, it is determined that this is a Load Buffer Table instruction with the first character to be loaded from location 7 5 5 0 in BPU HSM.

The signal, SIO2 · TPC2-N from driver 74/B4C strobes the lower right-hand gates used to detect the B_2 character (OB00-OB03) and the B_3 character (OB10-OB12). The B_2 character is used to determine the number of lines to advance paper (0-15) and is stored in the LAC (Line Advance Counter) flip-flops. Since B_2 is now equal to 0, none of the LAC flip-flops are Set with SIO2 · TPC2-N. Gate 74/B4D is enabled if $B_3 2^0$ is present (B3=1) to Set the PRINT 120 flip-flop, indicating PRINT 120 Characters instead of 160 Characters. Gate 74/B4E is enabled if B3=2 and Resets PRINT 120. Gate 74/B4F Sets the TRANSFER TABLE flip-flop if B3=4 (our example). Gate 74/B3B Sets TRANSFER DATA flip-flop if B3=1 or 2. Transfer Table Set (74/A4B) primes gate 73/B5D via 73/B6E.

TPC 3 - At TPC3, 73/B5D is enabled to Set D-REQ (73/A5B). Pin 3 of 73/B5D is a low as a result of Housecleaning (SIO1) Setting the PRINT flip-flop, 74/A8A. The D-REQ flip-flop Set and a Simo 1 instruction staticized generates S-REQ1 which is sent back to the BPU to request a diad.

NOTE: This first S-REQ1 is a function of the SIO2 status level; all future requests must be initiated by the Buffer transmitting the signal D-REQ-N to element 73/B5A and Setting the D-REQ flip-flop via gate 73/B5F.

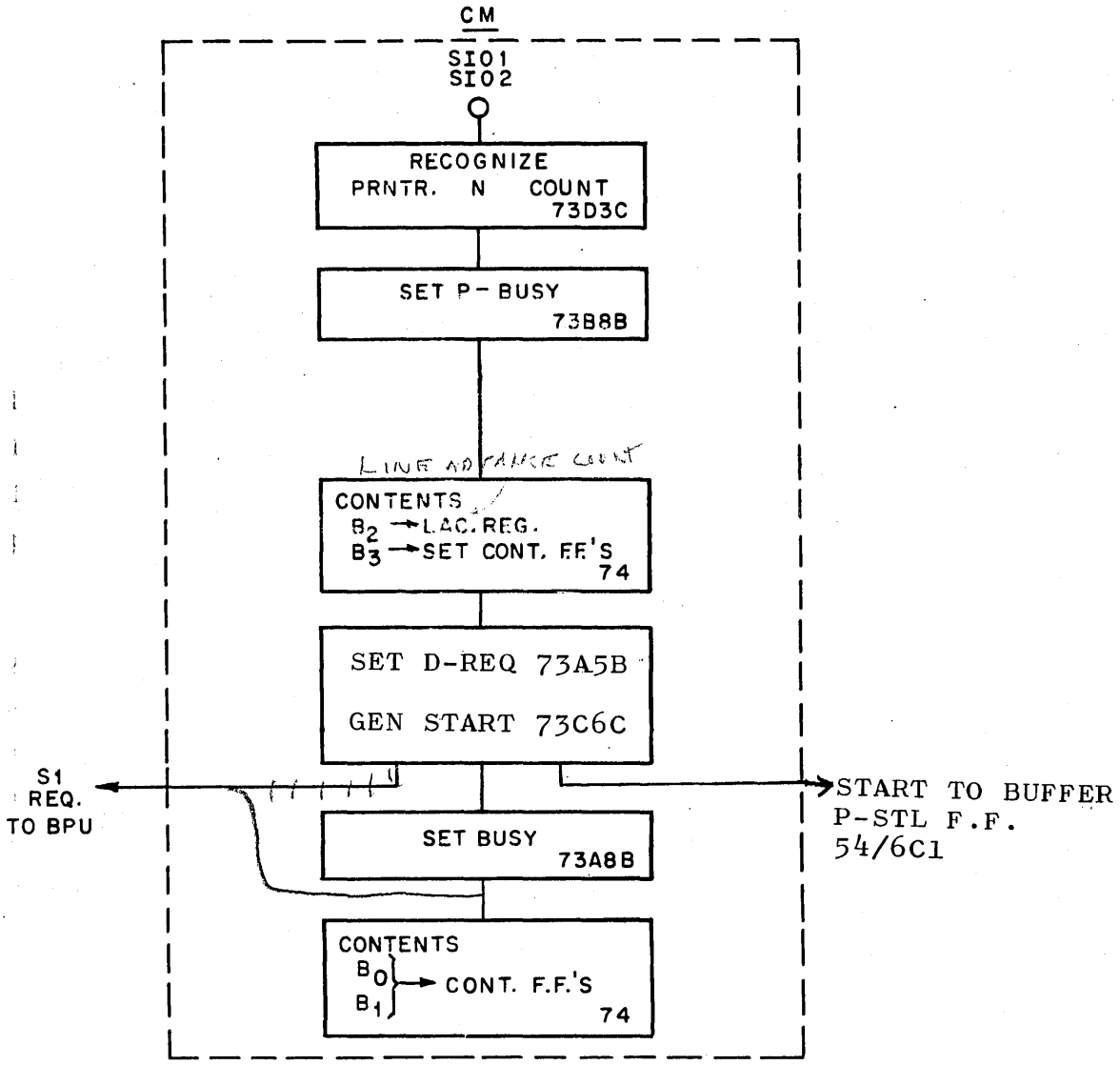
The START-P (73/C6C) signal is sent to the Buffer and used to Set or Reset (depending on whether the B portion of the Write instruction dictates a Transfer Table or a Print Operation) a PRE-STATUS LEVEL flip-flop.

TPC 4 - During TPC4 of SIO2, the BUSY flip-flop, 73/A8B, is Set.

TPC 5 - At TPC5 time, 74/B8B is enabled to strobe the left-hand series of gates on print 74. The inputs to these gates are labeled similar to those on the right; however, at this time, OB00 thru OB02 is actually the B_0 character and OB10 and OB11 is the B_1 character of the

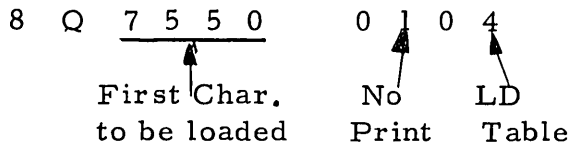
instruction word. These were gated onto the bus by the BPU at TPL4 via 05/B3B (BPU logic). If $B_0 = 1$, gate 74/B7C Sets Line Advance; if $B_0 = 2$, 74/B7D Sets Vertical Tab; and if $B_0 = 4$, 74/B6D Sets Page Change. The B_1 character is examined by 74/B8D and B8F. If $B_1 = 1$, the Print flip-flop is Reset. If $B_1 = 2$, the Synch flip-flop is Set, indicating synchronous mode.

At the completion of SIO2, nothing of significance happens until the BPU services the S_1 Request. Figure 3.2 summarizes the SIO1 and SIO2 functions in the Control Module. Figure 3.3 is a detailed account of SIO1 and SIO2 referenced to the logic drawing for the example selected.



SIO1-SIO2 CONTROL MODULE FUNCTIONS

Figure 3.2



SIO1

TPC1 - Set SIO (73B4A)
HK/GR (73C7A) and LP-HK/GR (73C6D)
Generate N-COUNT-N (73D3E)
Set PRT SEL (73A7B)
IF LPHO - Set LPHO (73A6B)

SIO2

TPO -

TPC1 - IF $\overline{(\text{BUSY HO (P)})}$ (P-ADD-N) - Set P-BUSY (73B8B)

TPC2 - Contents B2 → LAC (74)
B3 = 1 Set PRINT 120 (74B4D) - Set TRANSFER DATA (74A3A)
B3 = 2 Reset PRINT 120 - Set TRANSFER DATA (74A5A)
B3 = 4 Set TRANSFER TABLE (74A4B)

TPC3 - IF $\overline{(\text{TRA TA} + \text{TRA DT})}$ $\overline{(\text{BUSY})}$ (P-BUSY)(PRINT): Set D-REQ (73A5B)
IF $\overline{\text{LPHO}} \cdot \text{P}$ - BUSY · P - ADD - Start (73D6A)

TPC4 - IF ~~BP~~ PRE - BUSY - Set BUSY (73A8B)

TPC5 - B1 = $\overline{2^0}$ Reset P START (73B2D)
B1 = 1 $\overline{(\text{TRA-TA})}$ Reset PRINT (74A8A
B1 = 2 Set SYNCH (74A8B)
B0 = 1 Set LINE ADVANCE (74A7A)
B0 = 2 Set VERTICAL TAB (74A7B)
B0 = 4 Set PAGE CHANGE (74A6A)
IF LA + VT + PC: Set PA (73C3E)

TPC7 - Reset LPHO (73A6B)

TPC8 - Reset SIO (73B4A)

Figure 3.3 - SIO1-SIO2 Status Flow

When the BPU honors the S-REQ1, it sends S1 to 72/D5A. The output of 72/D5A is applied to 73/D4A and produces C-S1/S2, STROBE A and STROBE B. The Strobe A and B signals are returned to the Processor for control. C-S1/S2 Resets D-REQ, 73/A5B, via 73/B5C and also primes 74/D8B. At TPC7, 74/D8B is enabled to strobe the diad on the bus onto Data Register 1 and 2 with the GATE DATA (P) signal. Gate Data (P) also Sets DATA READY, 73/A4B, to send the DATA RDY (DR) signal to the Buffer. The Buffer transfers the diad into the Buffer Memory Register to be later stored in core and sends back to the Control Module D-REQ-N, 73/B5A, requesting another diad. This process continues until the Buffer is full.

3.1.3 Termination

Termination is controlled by the Buffer Setting its TERMINATE flip-flop which sends BR-P (Buffer Ready) to 72/B5B in the CM. BR(N) is applied to 73/B3D and 73/B2B. 73/B2B Sets END TRA, 73/A3D, for a Load Table instruction (TRA-TAB) and 73/B3D Sets END TRA for a Print instruction (TR-DT). END TRA and PRT SEL 73/A7B (Set since SIO1), at gate 73/D2C permits the generation of INS TERM-N 73/D2F at TPC3 time. Gate 73/C2B is enabled provided Low Paper was not detected (LP-INT), there was no Write Parity Error (WE), no Read Parity Error (RE), and the Device Not Follow Alarm was not detected. The signal SIMO COMPLETE ONE (SCOM 1 or SCOM 2, depending on mode) is sent from 73/C2E to the BPU logic to Set Interrupt 17 (16 for SCOM 2).

The signal INS TERM, 73/D2F, generates Simo Busy Reset 1 or 2 via 72/C3A, C3B, which Resets the appropriate BUSY flip-flop in the BPU. Error termination is detected by 72/D3A and 73/D2A to generate Simo Requires Attention, SRA1 or SRA2, which causes an Interrupt 14 (13) in the BPU.

Upon receiving the S_1 REQ, the BPU will grant service in accordance with the established priority system, i.e., Communications Mode Requests, Simo 3 Requests (S_3), S_2 Requests, S_1 Requests, and Normal Mode. Refer to Figure 3.4. When the Processor services the S_1 Requests, the status level that is generated is an $S_1 \cdot WR_1$ (Status Flow Manual, Page E11). When $S_1 \cdot WR_1$ is selected, the signal S_1 is sent to the Control Module to inform it that its request is now being honored. The CM responds with Strobe A, Strobe B, indicating that it

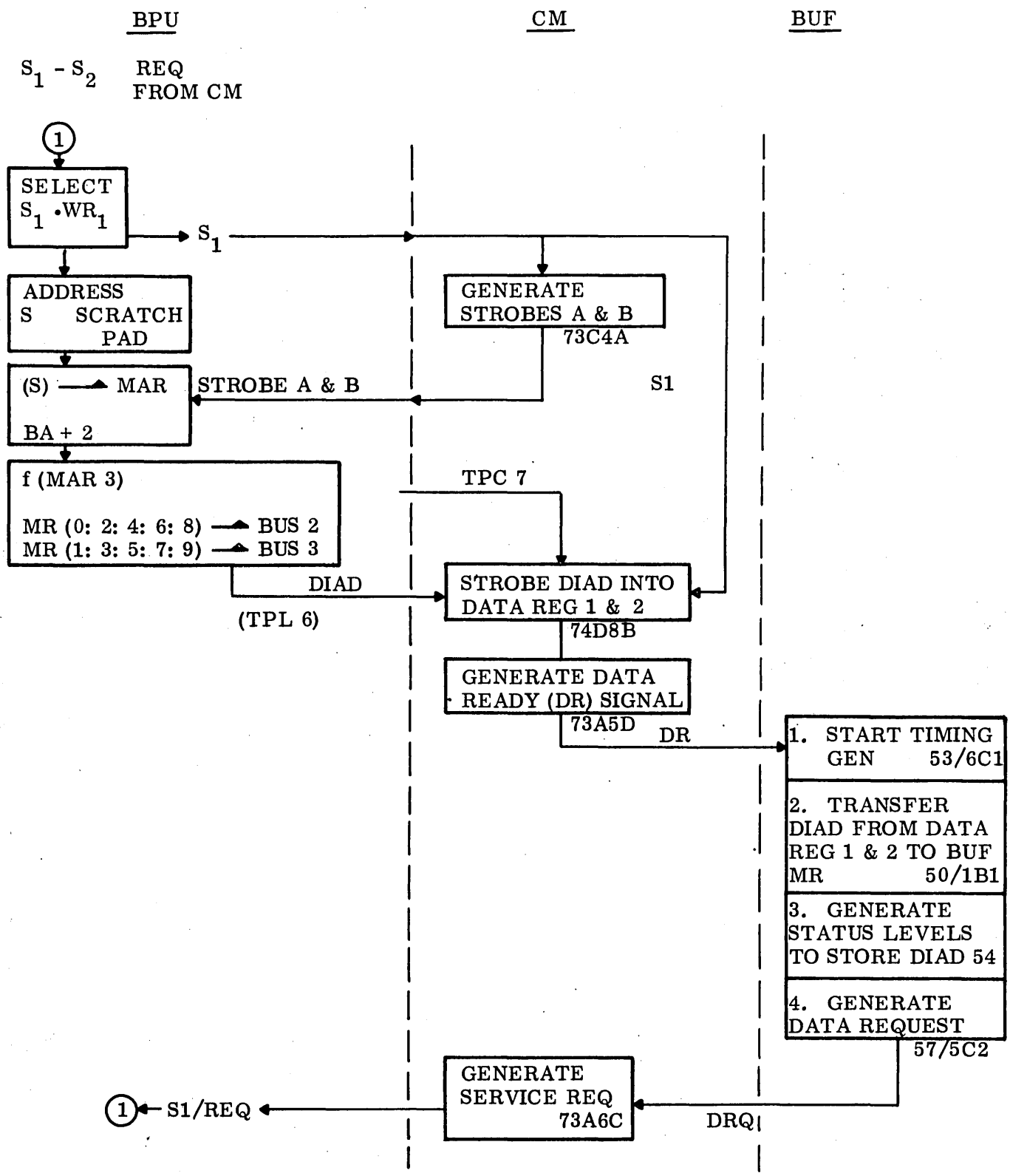


Figure 3.4 Transfer of Data - BPU → Buffer

accepts data by diad which informs the BPU to increment "S" by plus 2 prior to placing "S" back in SP. The contents of "S" addresses the main memory placing a decade in the MR. MAR3 determines which two characters of the decade are to be gated to the bus at TPL6 time.

At TPC7 the diad is strobed into Data Register 1 and 2 in the CM and a Data Ready (DR) signal is sent to the Buffer.

Reception of DR activates the Buffer timing, transfers the diad from the Control Module Data Register to the Memory Register in the Buffer, initiates a status level to store the diad, and generates a request for another diad.

The Data Request (DRQ) is sent to the Control Module, which in turn generates an S_1 REQ to the BPU after a fixed delay which insures the Buffer will have stored the first diad before the BPU sends the second. The S_1 REQ causes the BPU to select an $S_1 \cdot WR_1$ status level (again, in accordance with priority) and the process continues until the Buffer has filled the 64 character table area of his core memory, at which time, the instruction terminates.

NOTE: In the case of a Print Instruction, termination takes place after the data area of the Buffer is filled. All characters will be compared and printed after the mode is free. An Interrupt 9 signifies that the line has been printed.

Figure 3.5 is a flow chart of the BPU functions after reception of the S1 REQ.

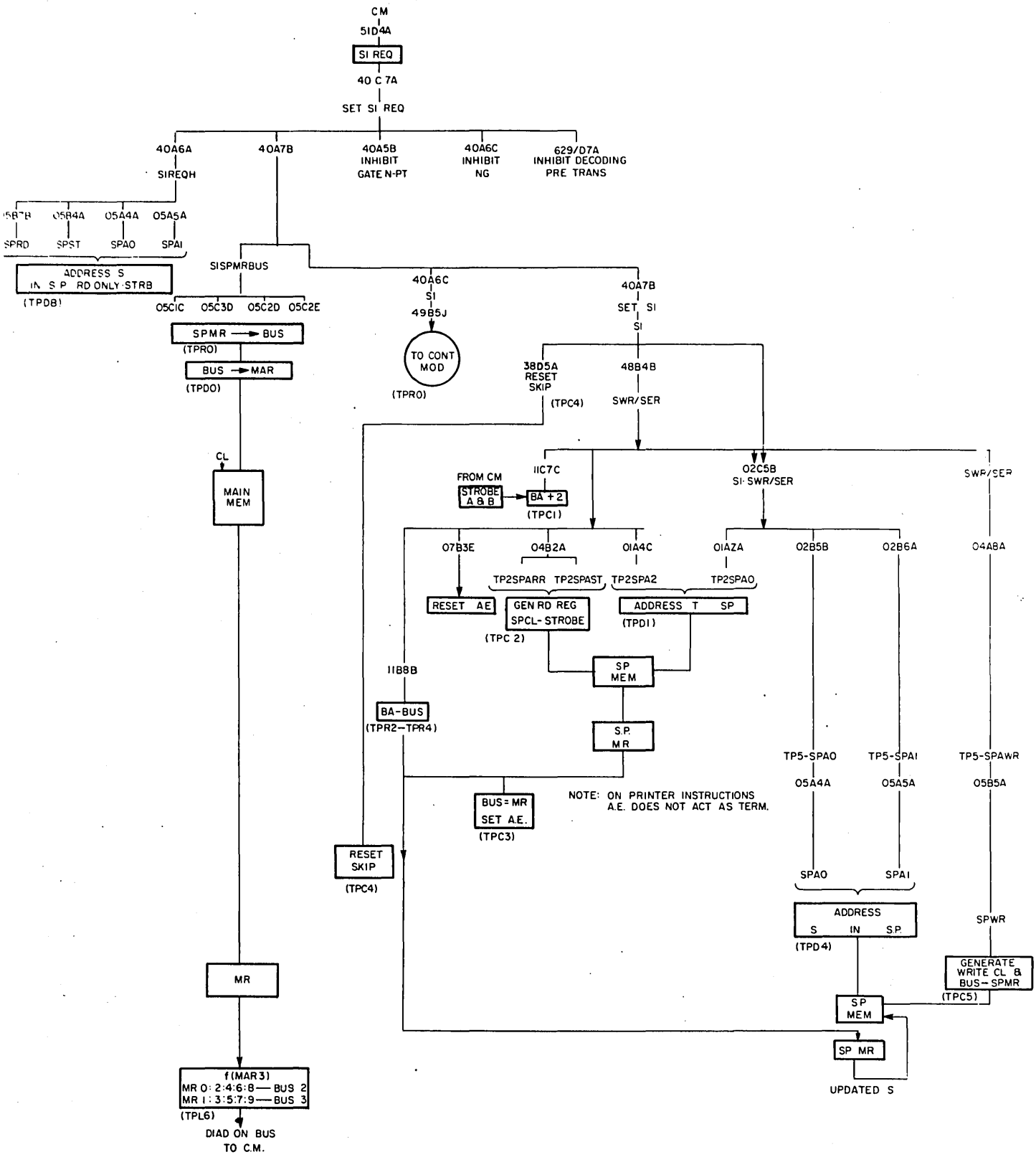


Figure 3.5 Flow Chart SI Request

3.2 Buffer - Reference Logic Prints Nos. 3506950 thru 3506958

The Buffer logic is activated by two signals from the Control Module. The first, START (Refer to Figure 3.2), is received during the SIO2 status level following staticizing and is used in conjunction with the Transfer Table or Transfer Data flip-flops in the CM to condition pre-status level flip-flop. Two status levels are used in the Buffer logic, i.e., "E" or "F." An "E" status level is selected any time the TABLE area of the memory is to be addressed. An "F" status level is selected any time the data area of memory which holds the line of print data (sometimes referred to as the FIELD area) is to be accessed.

The second signal, DR (DATA READY), is received from the CM when it has a diad available. The DR signal starts the Buffer timing, permits strobing of the diad into the Buffer MR, and selects the "E" or "F" status level.

Operation of the Buffer is classified into three cycles. They are:

1. Fill Cycle - used when loading the Buffer memory.
2. Print Cycle - used when comparing each character of the Table to every character of the field and firing the appropriate printer hammer.
3. Paper Advance Cycle - used when moving paper.

It is important to note that an "E" and "F" status level may be used during the Fill and Print (also referred to as Compare) cycles. For example:

1. E-STL·FILL (cycle) - indicates the Buffer Table is being loaded.
2. F-STL·FILL - indicates the Buffer Field is being loaded.
3. E-STL·COMP (print cycle) - indicates the Table is being accessed to determine the next character on the Print Drum.
4. F-STL·COMP - indicates the Field is being accessed to compare it against the next character to be printed.

Figure 3.6 illustrates the status level combinations and their associated functions. During the Load Table Instruction, an "E" status level and Fill cycle is repeatedly used (32 times) to store each diad coming from the Control Module. When the table is completely loaded, the signal, TBL COMPLETE permits termination.

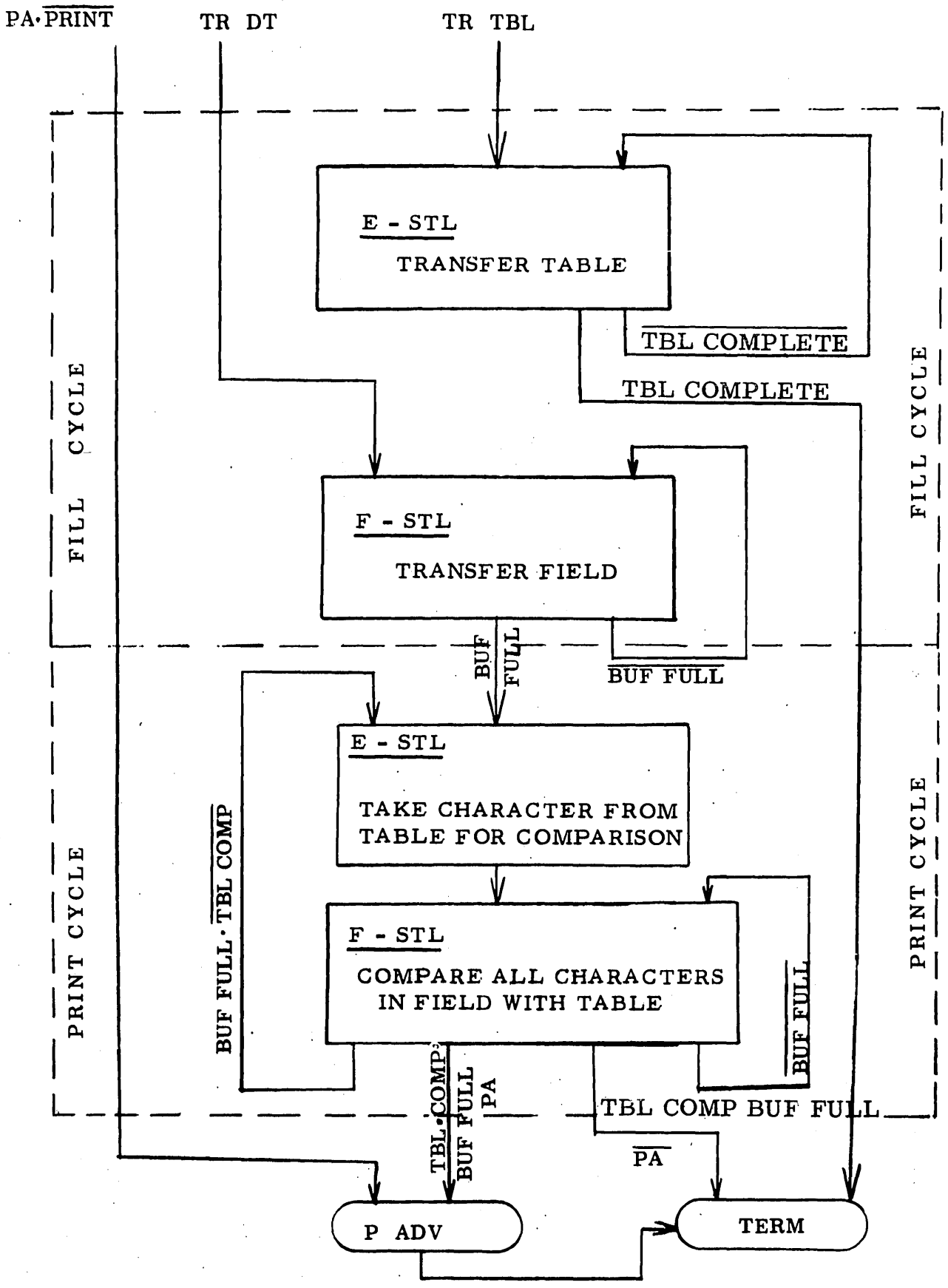


Figure 3.6 Status Level Combinations

On a Print instruction, an "F" status level and FILL cycle is repeated (60 times for 120 col. PTR, 80, for 160 col. PTR) until the Field is loaded. The Signal, BUF FULL, then selects an "E" status level and PRINT cycle which extracts that character from the Print Table next to be printed. After the "E" status level, 60 (or 80) "F" status levels are performed to compare the entire Field to the Table character. After this is done, those characters which compared are printed, another E-STL is selected which brings out the next character to be printed. Sixty "F" status levels are then performed to again compare every character in the Field to the new Table character. The signal, TBL COMP • BUF FULL, indicates that all Table characters have been compared to the Field and Paper Advance or Termination is permitted.

3.2.1 Load Table Instruction

When the START signal is received (57/8D1) from the CM, it Sets the P-STL flip-flop 54/6C1 via 54/6D5 and AND gate 54/7D2. The TR-TA (N) signal (Transfer Table) and PRINT (N) signal at 54/7D2 also come from the CM and are both low for this instruction. When the CM strobes the diad from the BPU in its Data Register, it also sends DATA READY to the Buffer on 57/7D3. Through the receiver and inverters, the signal becomes DR(N) and DR(P). DR(P) Sets FILL 54/8A3 and PRINT GATE 54/7C9. DR(N) strobes the diad present in the CM Data Register into the Buffer Memory Register on print 50 via gates 50/1B1, 2B6, 2B4, etc. DR(N) also Sets the RUN flip-flop 53/8C4 via 53/6C1. The OSC "B" signal is always present and is derived from the 500KC oscillator 53/8D1.

With RUN Set, the timing generator, consisting of C_0 thru C_5 in conjunction with decoder gates 53/8A5 thru 53/5A7, produces timing pulses CP0 thru CP7. Figure 3.7 depicts the propagation of 1's from C_0 to C_2 to C_4 with OSC "B" pulses and the propagation of 1's from C_1 to C_3 to C_5 with OSC "A" pulses. Note the generation of CPO • STP from 53/8A1 at the completion of CP7. CPO • STP Resets PRINT GATE 54/7C9 via 54/6C3 which removes the E-STL(N) level 54/6B1, causing the Buffer to stop until the CM again sends DATA READY (DR), indicating another diad is available for the Buffer. The RUN flip-flop, once Reset, must also wait until DR is received before being Set for this instruction.

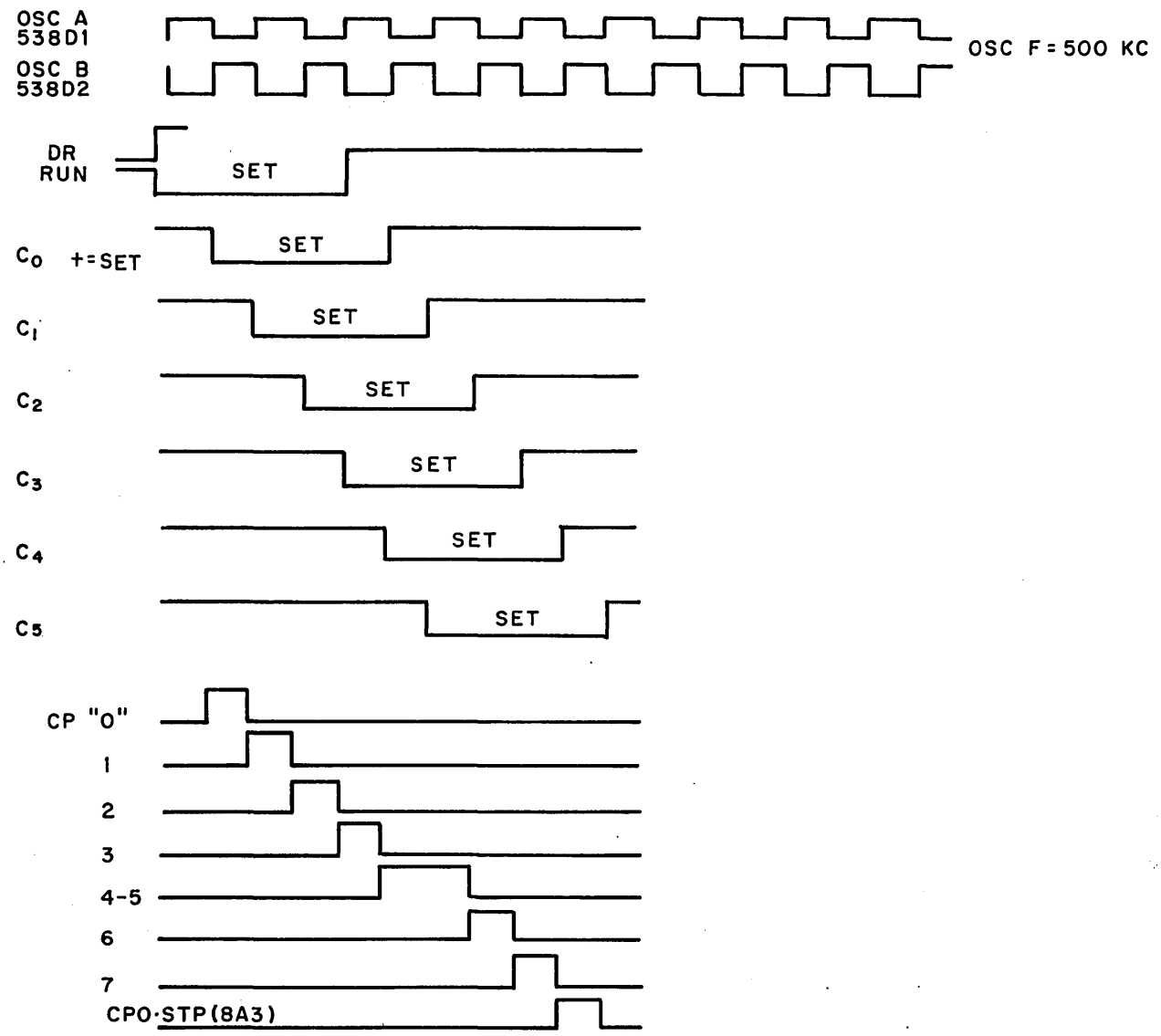


Figure 3.7 Printer Buffer Timing

CP0 - With the generation of the CP pulses, an E-STL is selected. CP0 Sets E/F-STL, 54/6C7 via 54/6C5 and E-STL(N) is generated from 54/6B1. E-STL(N) is combined with the FILL flip-flop to generate E-STL · FILL(N) 53/5B5.

CP1 - Addressing of the Buffer memory is controlled by the X and Y counters and decoders on print 56. Gate 56/7D1 triggers $YT2^0$ at CP1 time, changing it from its Set to Reset state, which also causes $YT2^1$ to go Reset. Notice that initially both were Set (assuming a Buffer Reset prior to the Load Table instruction). The YT counter is used for Y address line selection of the table area of memory only when loading the Table. The memory is addressed by selecting one of ten X lines and one of twelve Y lines. The table area is addressed by selecting Y8, 9, 10, or 11 and any X line from X_0 thru X_7. Four Y lines and eight X lines provide 32 discreet addresses with a diad at each for a total of 64

characters. The right-hand side of print 55 shows the assignment just described.

The decoding of YT 2^0 and YT 2^1 provide the four possible combinations for the table Y lines. Y8 is decoded from 56/5B2 when both are Reset; Y9, 10, and 11 are decoded for the remaining three combinations. Notice that YT 2^2, 56/8D4, is not decoded. It is simply a control flip-flop which determines when the X counter 2^0 stage, 56/4D6, may be triggered. Initially, $X2^0$ thru $X2^3$ are Reset; gates 56/8C1 thru 56/6C3 decode the X counter. At this time, gate 56/6C3 is enabled and the signal X00(N) generated. X00(N) primes pin 15 of 56/5B8 with pin 16 low due to FILL (ON) and $X2^3$ (ON), the signal X0(P) is generated from 56/5A1. Lines X_0 and Y8 have now been selected.

Each CP1 time of a Load Table instruction YT 2^0, 56/7D5, is triggered and a new Y line selected. The X line, however, only changes when the selected X line has been used with each Y line, since the $X2^0$ stage can only be triggered when YT 2^2 is Set. The following example shows the X and Y relationships and may be related to the core layout drawing on print 55.

1st Diad	X_0	Y_8
2nd "	X_0	Y_9
3rd "	X_0	Y_{10}
4th "	X_0	Y_{11}
5th "	X_1	Y_8

CP1 - In addition to selecting the X and Y address line at CP1 time, a request for a second diad is requested even though the first diad still has not been stored in the Buffer core. The signal DRQ, 53/7B6, is present during the Transfer Table instruction until it is determined that the table is completely filled, at which time, TAB COMP (ON) goes high. DRQ (N) is ANDED with CP123 on 57/5C2 to send DRQ (P) back to the CM. The CM, in turn, delays this to permit time to store the first diad and then generates the S_1 REQ to the BPU.

CP1 - CP1 also Sets flip-flop CP 17, 56/1C1, which remains Set until the leading edge of CP0 (trailing edge of CP7). CP 17 (IN) at 54/5B3 produces STR INH (P) (Strobe Inhibit). STR INH (P) to 50/6D2 inhibits its output for the duration of the status level which prevents the strobing of the Sense Amplifier gates 50/8B1 thru 50/2B3 during the Read portion of the memory cycle.

CP2 - At CP2 time, the X line counter and YT line counter are checked on 54/2B2 to determine if the present diad to be loaded is the last. In effect, 54/2B2 recognizes when lines X7 and Y11 are going to be accessed, which is the last table address of core (refer to core layout on 55). When this condition is detected, the TABLE COMPLETE flip-flop, 54/2B6, is Set.

CP2 - Starting with CP2 and lasting until the completion of CP3, the READ COMMAND is generated by 54/6A4, 6A5, 5A3, and 5A4. READ (N) applied to 51/5D1 and 51/3D2 provides the current source for the selected X and Y switches on 52, which receive their inputs from the decoders on print 56. Refer to Figure 3.8.

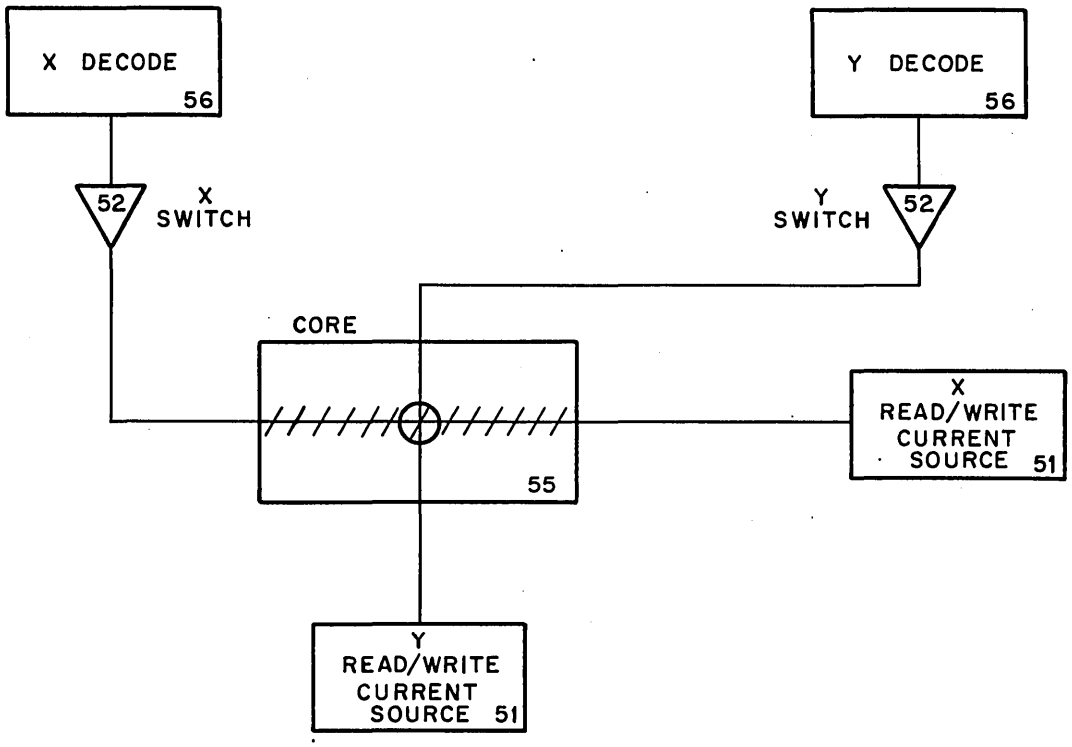


Figure 3.8 Address Line Selection

CP5, 6 - Starting at CP5 and lasting until the end of CP6, the WRITE (P) signal is generated (54/5B4 and applied to 51/5C1 and 51/3C1 to permit writing the diad now in the Buffer MR

(print 50) into the cleared memory location under the control of the digit drivers, 51/8C1 thru 51/2C1.

CP5, 6 - During the time the Write pulse is present to memory, parity is checked on the MR on print 55/7C1, 7C2. Bad parity, when loading, constitutes a Write Error (WE) and causes SRA termination rather than SCOM termination in the CM.

CP7- If the Table is not completely loaded, 54/7D3 Sets P-STL, 54/6C1, to insure selection of another "E" status level when the CM contains another diad as a result of the DRQ (Data Request) sent at CP 123 time.

CP7- The Buffer MR is Reset via 54/3B7, 54/3A2 and 50/6D5, 6D4, making it available for the next diad transfer.

The preceding CP sequence is repeated each time the CM sends the Data Ready signal (DR) to the Buffer until the Table is finally filled. Figure 3.9 is a block analysis of the Transfer Table instruction,with each block keyed to the logic drawing.

Termination- Assume the Data Ready (DR) signal is received indicating a diad available in the CM and it is the 63rd and 64th character of the Table. FILL, 54/8A3, PRINT GATE, 54/7C9, RUN, 53/8C4, and the BUFFER MR flip-flops, 50, are Set as before. E-STL •FILL and CP pulses are produced.

CP1 - $YT2^0$ is triggered via 56/7D1. $YT2^0$ and $YT2^1$ are now Set and Y11 (P) is generated by 56/2B2. The X counter at this time is 0111 with LSB on right. Decoder 56/8C1 produces X70 (N). X70 (N) enables 56/2B9 to produce X7 (P). Y11 (P) and X7 (P) are applied to their respective switches, 52/2C2 and 52/2B2.

CP 123 - DRQ (N), 53/7B6, is sent to driver 57/5C2 and causes a DRQ (P) signal to be sent to the CM. Even though the diad placed in the BUFFER MR with DR is the last, the Buffer logic as yet, still does not recognize it and asks for another diad. Remember that the CM delays this request prior to setting its own D-REQ flip-flop. Before the CM's delay expires, the Buffer logic will send a signal to the CM to prevent it from acting on this last request.

CP 17 - A strobe inhibit is again produced by 54/5B3.

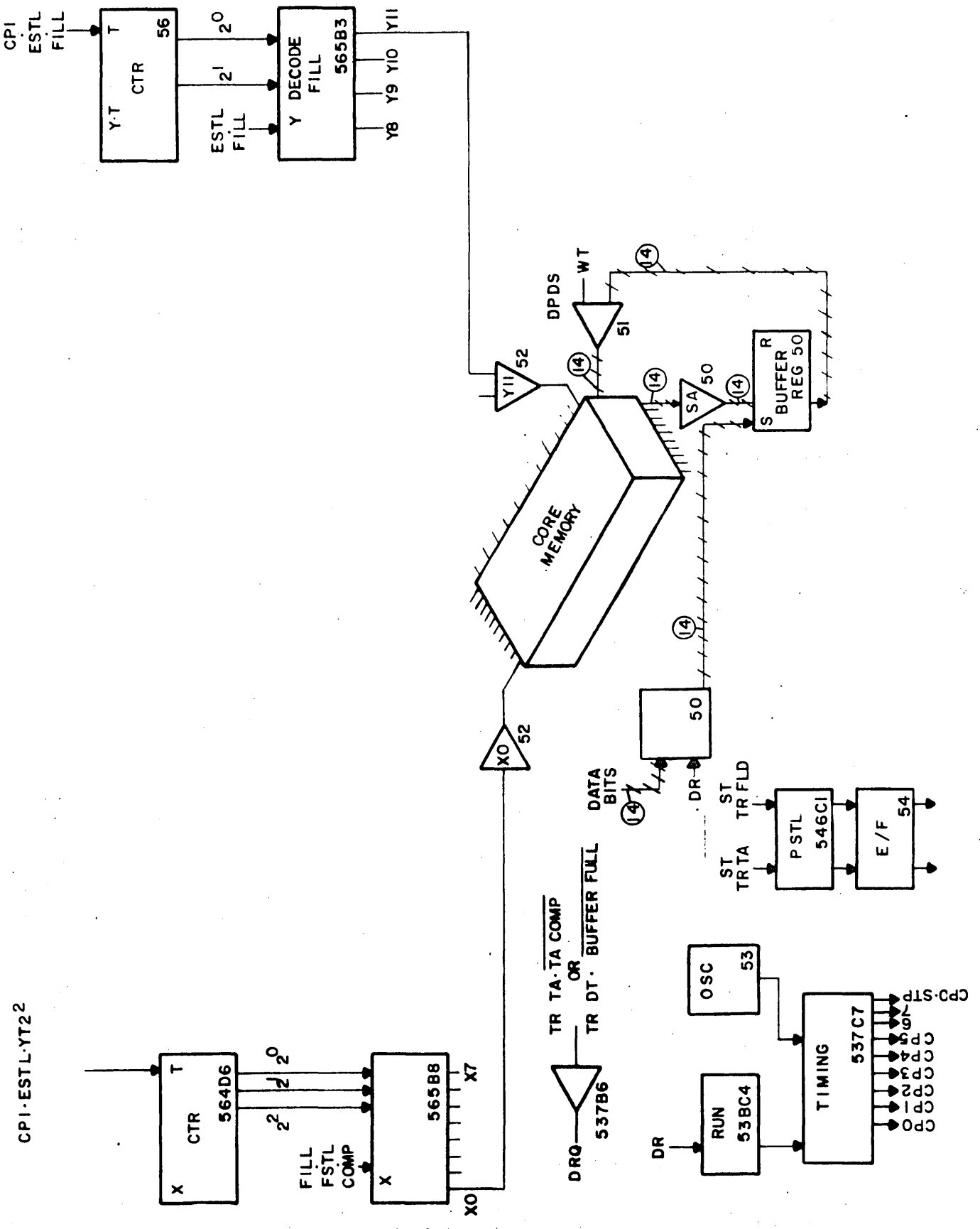


Figure 3.9 Transfer Table 32 E Status Levels

CP2 - The X and YT counters are decoded by 54/2B2 which finds the Y11 and X7 condition present and Sets TABLE COMPLETE, 54/2B6.

CP23 - Read Pulse to Memory is generated 54/5A4.

CP4 - With TABLE COMPLETE Set, and TR DT (P) a low, gate 54/4C5 Sets TERMINATE, 54/4B1.

NOTE: TR DT (P) is high when transferring the data (Field), not when transferring the Table (TR TA).

CP56 - The Write pulse is generated on 54/5B4. Write parity is checked on 55/7C1, 7C2. The Setting of TERMINATE at CP4 primes transmitter 57/5C4 and $BR_{(P)}$ (Buffer Ready) is sent to the CM. This BR signal, when received by the CM, Sets an END OF TRANSFER flip-flop which informs the CM to disregard the last DRQ sent by the Buffer and permits the CM to terminate the instruction with SCOM1 or 2 and SBRES1 or 2.

CP7 - The Buffer MR is Reset as before via 54/3B7, 54/3A2, and 50/6D4, 6D5.

Since TABLE COMPLETE is now Set, 56/5D1 Sets the address counters back to their first location. Figure 3.10 is the status flow for the Load Table Instruction.

E-STL • FILL

CP1 - TRIGGER YT ADDRESS 56/7D1

IF $YT2^2$(1) TRIGGER X ADDRESS 56/4D2

CP123 - IF TR TA •TAB COM(0) —— GENERATE DRQ 53/7B4

CP17 - GENERATE STROBE INHIBIT 54/5B3

CP2 - IF X7 •Y11 —— SET TAB COMP 54/2B4

CP23 - GENERATE READ PULSE TO MEMORY 54/6A4

CP3 - RESET $YT2^2$ 56/8D3

CP4 - IF $\overline{\text{TR DT}}$ • TAB COMP(1) —— SET TERMINATE 54/4C5

CP45 -

CP56 - GENERATE WRITE PULSE TO MEMORY 54/5B4

IF EVEN PARITY —— SET WRITE ERROR 55/7C1

IF TERM —— GENERATE BUFFER READY 57/5C4

CP6 -

CP7 - IF $YT2^0$(1) AND $YT2^1$(1) SET $YT2^2$ 56/8D2

IF TAB COMP(0) —— SELECT E-STL 54/ 7D3

RESET BUFFER REGISTER 54/3A2

IF TAB COMP(1) —— SET ADDRESS TO FIRST LOCATION 56/3D2

CP0•STP• RESET PRINT GATE 54/6C3

- -

NOTES:

TPC8 •TRA TBL •BR —— SET END TRA 73/B2B

Figure 3.10 Transfer Table Status Flow

3.2.2 Print Instruction

A Print instruction uses two cycles. The Fill cycle is used to load the data characters (120 or 160) from the BPU via the CM and the Compare cycle is used to compare table to data (field) and print. A third cycle is required if the instruction also specifies Paper Advance.

Fill Cycle- The Fill Cycle is initiated by the START and DATA READY signals from the CM. The START signal is received during the SIO2 status level following staticizing and enables 54/6D4, Resetting P-STL, 54/6C1. TR DT(N) (Transfer Data) and PRINT(N) are both low during this instruction at 54/5D1.

Data Ready (DR) is sent to the Buffer each time the CM has a diad available and performs the following functions:

1. Set PRINT GATE on 54/7C9.
2. Set FILL on 54/8A3.
3. Set RUN on 53/6C1.
4. Transfer diad from CM to Buffer MR 50/1B1, 2B6, etc.

Figure 3.11 is the block diagram of Buffer operation during the data transfer. This diagram differs from that of the load table block in that:

1. The P-STL flip-flop is Reset and an "F" status level selected.
2. A YF counter is used to select the Y address line of the field portion of memory.
3. The Y decoder gates decode only Y0 thru Y7. Lines Y8 thru Y11 are not addressed since they represent the table area of core.
4. The X counter is the same, but it is now possible to decode X8 and X9 lines in addition to X0 thru X7.
5. The applicable equation to generate DRQ (Data Request) is now TR DT • $\overline{\text{BUFFER FULL}}$.

Receipt of DR starts the timing generator, as previously discussed for the Load Table instruction, and CP0 thru CP7 are generated.

CP0 - CP0 (N) at 54/6C6 Resets E/F-STL, 54/6C7, and produces F-STL(N), 54/6B2. This is combined with the FILL flip-flop to produce F-STL • FILL(N) on 53/5B4.

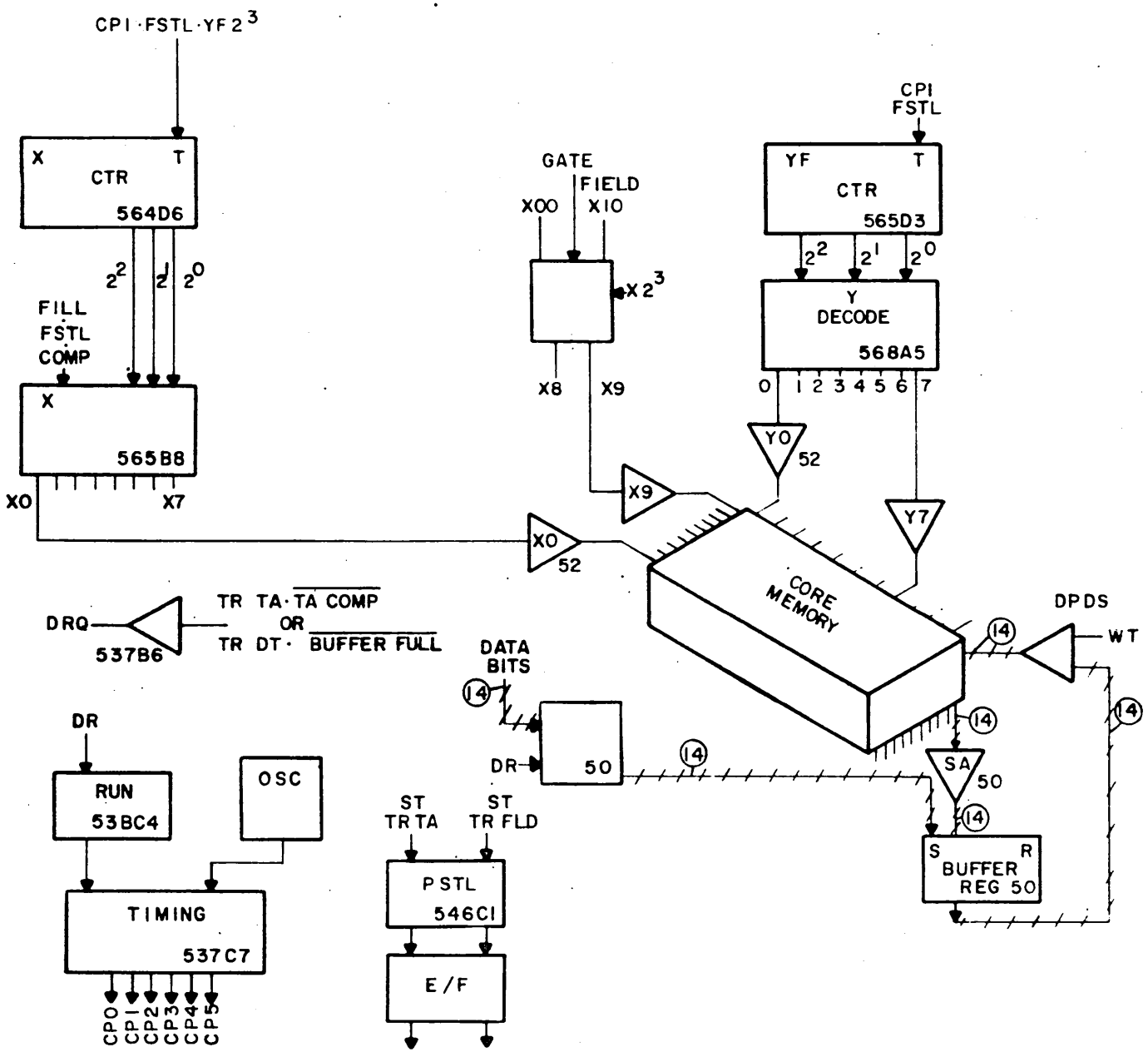


Figure 3.11 Print Instruction - Fill Cycle

CP1 - 56/5D2 triggers $YF2^0$, causing $YF2^0$, 2^1, and 2^2 to go Reset. $YF2^3$ is not used for address decoding, but controls the triggering of $X2^0$ via 56/4D1. A given X line is combined with each possible Y line before the X line can be changed. The X counter is decoded as before, but since a different Y counter is used during the Print Instruction, the decoder gates on the lower left of print 56 decode the selected Y line and enable the corresponding Y switch on print 56.

CP 123 - Gate 53/7B5 generates DRQ(N) as long as the BUFFER FULL flip-flop is not Set, indicating that the data area is not yet fully loaded. 57/5C2 sends DRQ to the CM to request another diad.

CP 17 - Strobe Inhibit (STR INH (P)) from 54/5B3 inhibits strobing of the Sense Amplifiers on print 50 via 50/6D2.

CP 23 - Read Pulse is generated to start the memory cycle on 54/6A4.

CP3 - A check is made each CP3 time to determine if the diad being stored is the final diad. Gate 54/2D4 recognizes when the last address in memory has been decoded. The last address of core for a 120 column printer is Y3 and X7; for a 160 column printer, it is Y7 and X9 (refer to core layout on print 55). When this is detected, BUFFER FULL is Set 54/3C1.

CP4 - If BUFFER FULL is set, set TERMINATE.

CP 56 - The Write pulse is generated on 54/5B4 to turn ON the Write Current Source on print 51. Also, Write Parity is checked on 55. If the TERMINATE flip-flop is set, BR on print 57 is generated. The BR signal causes the Control Module to terminate the instruction and free the mode. When the Buffer has completed printing the line, it will again generate BR. This time it will cause the CM to generate Interrupt 9.

CP7 - Gate 54/5D5 Resets P-STL, 54/6C1, to ensure selection of another F-STL as long as the Buffer is not full.

When the last diad is received, the same sequence is repeated, except that at CP3 time, BUFFER FULL is Set 54/3C1; at CP 45 time, P-COMP, 54/8C1, is Set via 8D4 and the X and Y counters on print 56 are Set to the first location via 56/3D3. Figure 3.12 is the complete status flow for the Fill Cycle of the Print Instruction.

F-STL • FILL

CP1 - TRIGGER YF ADDRESS 56/5D2
IF $YF2^3$ (1) —TRIGGER X ADDRESS 56/5D1

CP123 - IF TR DT • BUFF FULL(0) — GEN DRQ 53/7B5

CP17 - GENERATE STROBE INHIBIT 54/5B3

CP23 - GENERATE READ PULSE TO MEMORY 54/6A4

CP3 - RESET $YF2^3$ 56/6D1
IF X9 • Y7/X7 • Y3 — SET BUFF FULL 54/2D4

CP4 - IF TRDT(N) • BUFF FULL • FILL — SET TERMINATE 54 3C3

CP45 - IF BUFF FULL(1) — SET P-COMP 54/8D4

CP56 - GENERATE WRITE PULSE TO MEMORY 54/5B4
IF EVEN PARITY SET WRITE ERROR 55/7C1, 7C2
IF TERMINATE — BR 57 5C4

CP7 - IF $YF2^0$ (1) • $YF2^1$ (1) • $YF2^2$ (1) — SET $YF2^3$ 56/7D3
IF BUFF FULL(0) — SELECT F-STL 54/5D5
IF BUFF FULL(1) — SET ADDRESS TO FIRST LOCATION 56/3D3
RESET BUFFER REGISTERS 54/3B7

CP0 • STP • RESET PRINT GATE 54/6C3

NOTES:

First location of address — (X=0000, YT=011, YF=0111)

Figure 3.12 - Fill Cycle - Print Instruction

Compare Cycle - The Compare Cycle is started as soon as it is determined that the last diad of the print line has been stored in the Buffer memory. Both "E" and "F" status levels are used during the Compare.

An "E" status level is performed to identify the character next to be printed. This is accomplished by having the character pulses coming from the Printer Drum control a memory address counter. The count contained in the counter then becomes the address of the table area of Buffer memory where that character may be found. A memory cycle is started and the character extracted and placed in a One Character Compare Register. Figure 3.13.

Sixty (80, for 160 col. prt.) "F" status levels are then performed to compare each diad in the data (field) area of core to the character in the Compare Register. Each true comparison is remembered by Setting a flip-flop in a Shift Register so that its associated printer hammer may be fired to print the character. Figure 3.14.

Another "E" status level is performed to identify the next character to be printed and is put in the Compare Register. Sixty "F" status levels then compare each diad in the data area to that character in the One Character Compare Register and the process continues.

If synchronous mode has been specified by the instruction, only 47 characters of the drum are compared and printed. If asynchronous mode is specified, the sequence just explained is repeated until all 64 characters of the table have been compared to every character in the field and printed, at which time termination may take place.

Identify Character Next to be Printed - The Setting of the PRE-COMPARE flip-flop, P-COM, 54/8C1, at the conclusion of filling the data area of Buffer core permits the selection of the E-STL • COMP sequence. P-COM primes 54/4D5 and 54/3D1. Gate 54/3D1 is enabled with the next character pulse from the Print Drum if asynchronous mode is specified. Gate 54/4D5 is enabled if in synchronous mode, but not until the signal CC40 (54/1C4) is detected. The reason for this is that in asynchronous mode, since all 64 table characters are compared, no specific drum reference is needed to start. In synchronous mode, however, a reference is needed to the Print Drum to insure those characters not to be printed are not compared. CC40 represents table location 32 which, when ANDED with character pulse at 54/4D5, provides the reference needed for the first character to be compared.

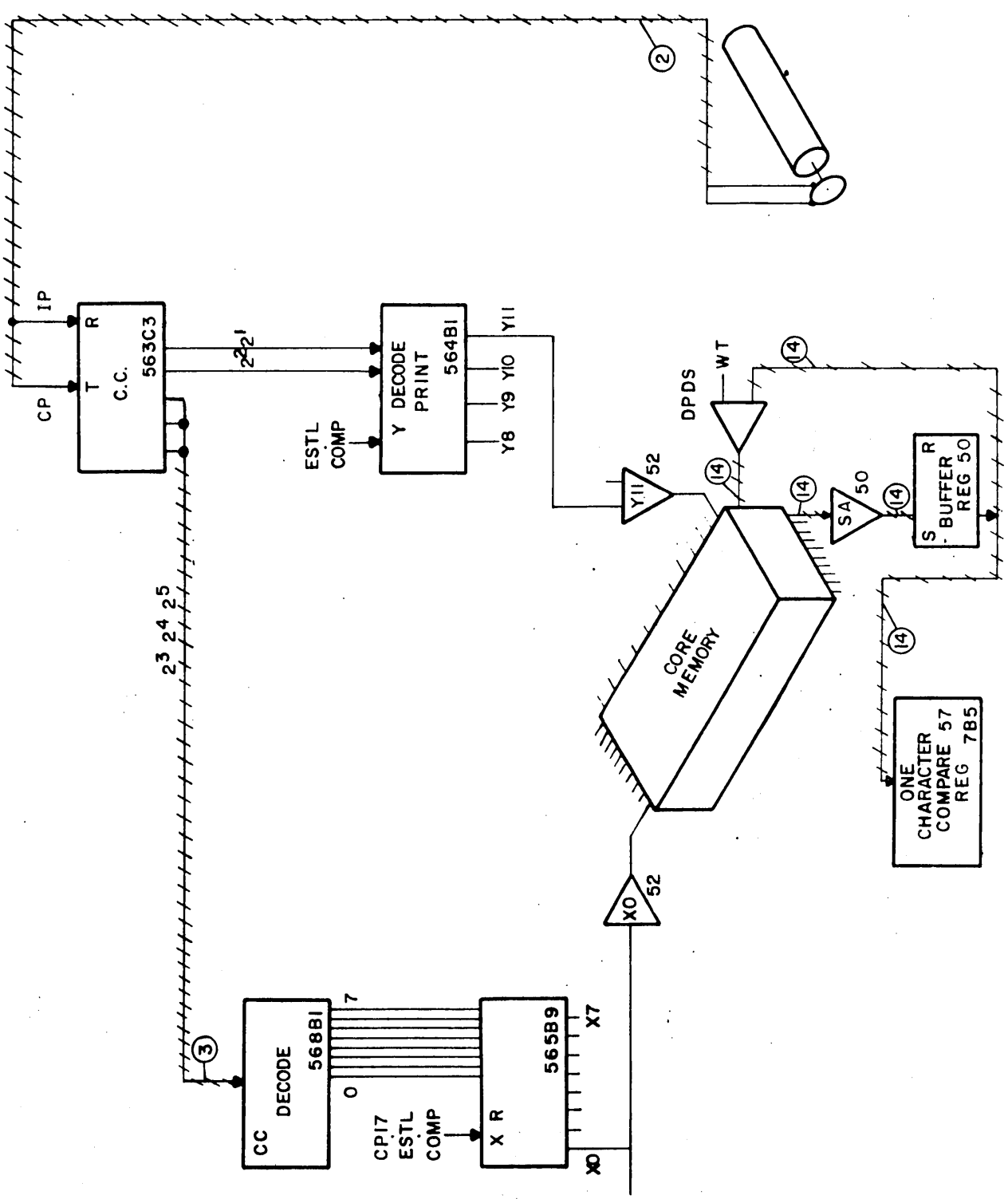


Figure 3.13 E Status Level - Compare Cycle

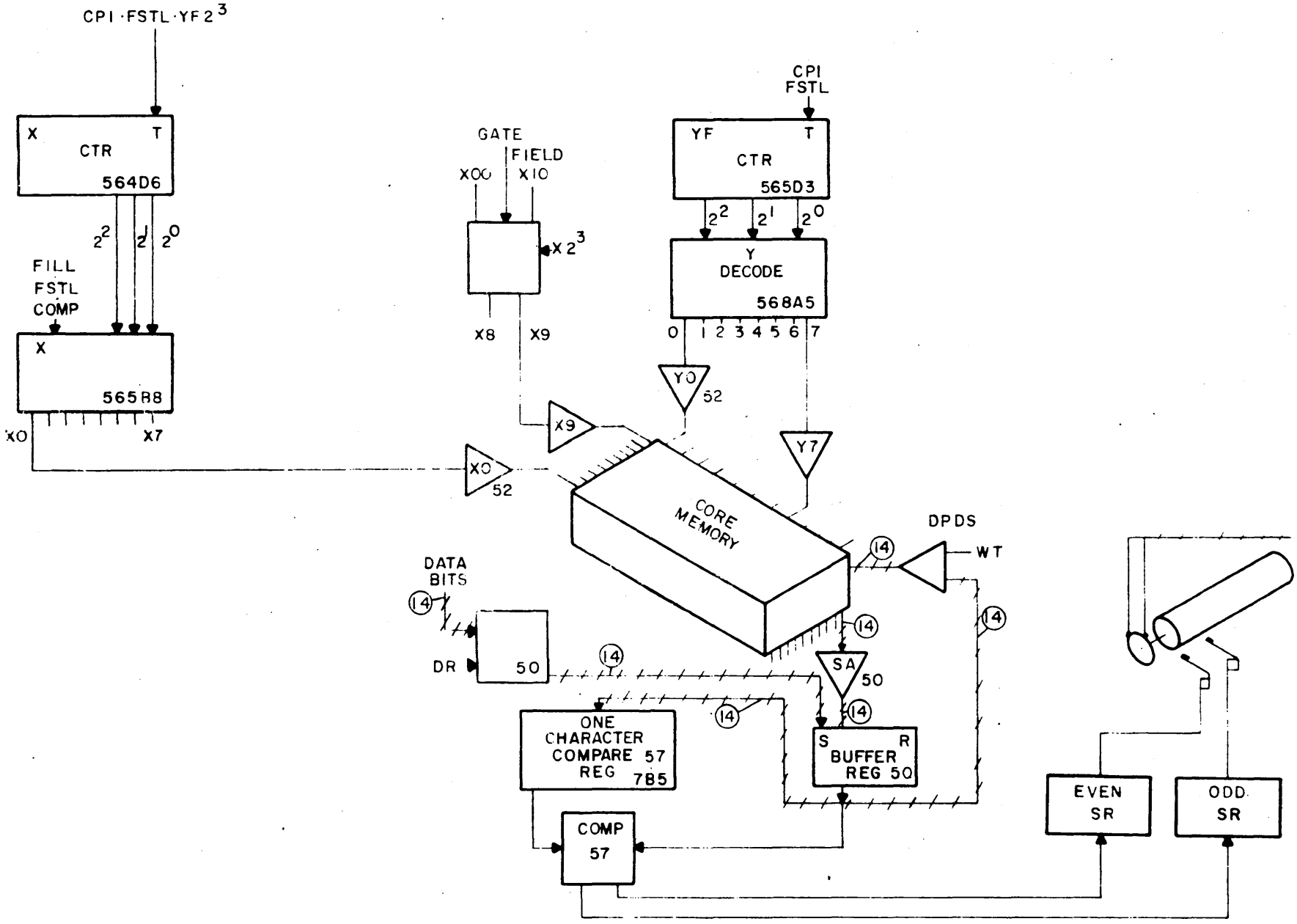


Figure 3.14 F Status Level - Compare Cycle

Either of these gates enabled, generates SET 1st COMP (P) and Sets 1st COMP, 54/4C1, which in turn causes the following to go Set:

1. PRT GATE 54/7C2
2. FCCP 54/3A3
3. P-STL 54/6C1
4. RUN via 53/6C3
5. COMPARE 54/7A4

With RUN Set, the CP pulses are generated as before.

CP0 - Select "E" status level 54/6C5, 6C7, 6C8, 6B1, and combine with COMP to produce E-STL • COMP 53/6B2.

CP 17 - A table address is generated from the CC counter 56/3C. The three most significant stages are decoded by 56/8B1 thru 56/6B4, which in turn prime 56/5B9 thru 56/2B10 to select a table X line. Gates 56/4B1 thru 56/2B3 decode the least significant stages of CC for Y line selection.

CP 23 - A Read pulse to memory is generated by 54/5A4. Note that the STROBE INHIBIT signal is not generated for these memory cycles.

CP3 - P-COMP, 54/8C1, is Reset.

CP 45 - 1st COMP, 54/4C1, is Reset.

CP 56 - The Write pulse, 54/5B4, is generated and a Read parity error check performed 55/6C1. At this time the MR contains a diad. However, only one character may be placed in the Compare Register. The 2^0 stage of the CC counter determines whether it should be BR1 or BR2. Refer to 57/8C2, 8C4.

CP6 - BUFFER FULL Reset 54/1D1.

CP7 - Select F-STL by Resetting P-STL via 54/4D1.

A series of 60 (80) F-STL's are performed to compare Field to Table. Those characters which compare are printed and another E-STL • COMP is selected. Each time a table

character has been compared when in asynchronous mode, a special CC counter is triggered 54/4A1. CCC 2^6 is sensed to tell when 64 table characters have been compared. In synchronous mode, 54/2C4, decodes CC17 which indicates the selected 47 table characters have been compared. When either of these two conditions exist, gates 54/2B1 or 3B1 cause TABLE COMPLETE, 54/2B6, to Set and FCCP, 54/3A3, to Reset. Figure 3.15 contains detailed status flow for the E-STL • COMP sequence.

E-STL • COMP

External Preliminary Timing

IF CHAR PUL • P-COM(1) • $\overline{PA}$ • SYNCH(0) • FILL(0)/SYNCH(1) • CC40
— SET 1st COMP 54/4C1 • SET PRT GATE 54/7C2 • SET FCCP 54/3A3 •
SELECT E-STL 54/7D4

IF (CCC 2^6(N) • SYNCH(0) 54/3B2/SYNCH(1) • CC17) 54/3B1 — RESET FCCP —
SET TABLE COMPLETE

IF COMP(1) • SYNCH(0) — SET CCC 2^0, RESET CCC 2^1 THRU CCC 2^6

IF 1st COMP(0) • FCCP(1) • SYNCH(0) • CHAR PUL — TRIGGER CCC 54/4A1

IF 1st COMP(1) • $\overline{\text{INH COMP}}$ — SET COMP 54/7A1

INDEX PULSE — RESET CHAR COUNTER 56/3C3
CHAR PULSE — TRIGGER CHAR COUNTER 54/4B3

IF CHAR PUL • FCCP(1) • COMP(1) • OSC "B" — SET RUN 53/6C4
IF CHAR PUL • FCCP(1) — SET PRINT GATE 54/7C1

CP 17 - GENERATE TABLE ADDRESS (CC 2^1 - 2^5)

CP 23 - GENERATE READ PULSE TO MEMORY 54/6A4

CP 3 - RESET P-COMP 54/8C1

CP 45 - RESET 1st COMP 54/3D3

CP 56 - GENERATE WRITE PULSE TO MEMORY 54/5B4
IF EVEN PARITY SET READ ERROR 55/6C1, 6C2
IF CC 2^0(0) BUFF FULL(1) GATE BR1 TO COMP REG 57/8C3
IF CC 2^0(1) BUFF FULL(1) GATE BR2 TO COMP REG 57/8C4

CP 6 - RESET BUFFER FULL 54/1D1

CP 7 - RESET BUFF REG 54/3B7
SELECT F-STL 54/4D1

- -

NOTES:

Figure 3.15 Identify Character Over Hammers

Compare Field to Table Character - At CP7 of E-STL • COMP, the P-STL flip-flop was Reset via 54/4D1. The RUN flip-flop, 53/8C4, was also Set via 53/5C1 to insure the generation of continuous CP pulses.

CP0 - The status of P-STL is transferred to E/F-STL via 54/6C6 selecting an "F" status level. This, combined with the COMPARE flip-flop, produces F-STL • COMP on 53/5B3.

CP1 - Trigger the YF counter to 1000 via 56/5D2 and decode Y0 line from 56/6A12. The X counter is decoded as before.

CP2 - The shift register used to remember the valid comparisons is shown on print 53. 53/2D3 and 2C2 each contain 60 flip-flops. If a 160 column printer is used, 53/2C5 and 2B4 (20 flip-flops each) are added. The table character present in the One Character Register is compared to each diad extracted from the data area of core. In order to distinguish between comparisons of the odd-numbered character of the diad versus the even-numbered ones, the shift register is divided into EVEN and ODD flip-flops interleaved. Each CP2 pulse of an F-STL • COMP advances both the Odd and Even Shift Register stages via 53/2B1.

CP23 - The Read pulse is generated to start the memory cycle on print 54/5A4. Note that the Strobe Inhibit Level is not generated during this status flow.

CP3 - Each CP3 time, a check is made to determine if the diad presently being addressed is the last diad of the data area to be compared to the table character in the One Character Register. Gate 54/2D1 is used for 120 column printers, and 54/2D2 for 160 column printers. If the condition being tested is true, BUFFER FULL, 54/3C1, is Set.

CP56 - The Write pulse to memory, 54/5B4, is generated to restore the diad and a Read parity error checked performed on the MR. If Even parity is detected, the READ ERROR flip-flop, 55/6C4, is Set. The contents of the MR is compared to the One Character Register on 57/8A1 thru 57/2A4 and provided "e" is not detected, 57/5A1, 5A4 produces SET SR-ODD(P), 57/6A6, and/or SET SR-EV(P), 57/4A5, when comparison is true.

The timing pulses do not stop at this time, but continually recycle, causing successive data diads to be compared and Setting of the appropriate ODD or EVEN flip-flops. When

the last data diad is compared with the table character, the BUFFER FULL flip-flop, 54/3C1, is Set at CP3 time. CP6 and Buffer Full Resets the Compare Register via 57/2B2. The signal, RES COMP REG(P), 57/3B3, is used to Set FSD (Fire Solenoid Drivers), 53/6D1. FSD and FIRE HAM (from 54/4B3 when next character pulse is received from Printer Drum) enables 53/4C1 to generate the GATE 1 thru GATE 14 signals applied to 53/1D1, 1C1, 1B1, and 1B2, which are those transmitters which have a shift register flip-flop Set and fire the printer drivers to print the first character. CP0 • ST Resets PRINT GATE 54/7C9.

Reception of the next character pulse from the Printer Drum Sets:

1. PRINT GATE 54/7C9
2. P-STL 54/6C1
3. RUN 53/8C4

With the above flip-flops Set, an E-STL • COMP is selected and the next table character is read out of core and placed in the Compare Register. An F-STL • COMP is then selected 60 (or 80) consecutive times to again compare the entire data area with the new table character.

When ALL table characters have been compared to the data characters, BUFFER FULL and TABLE COMPLETE are both Set, causing TERMINATE, 54/4B1, to Set at CP4 of the F-STL • COMP that compares the last data diad to the last table character. Also, at this time, SET P-PAD, 54/5C3, Sets PRE-PAPER ADVANCE flip-flop, 58/8C5, if paper advance information was contained in the Print Instruction.

CP56 • TERM generates BR(P) 57/5C4 to the CM to permit the generation of Interrupt 9. When the field was loaded, the Buffer generated BR which caused the Control Module to terminate the instruction. The TRANSFER DATA flip-flop (74A3A) was Reset after the END TRA flip-flop was Set and the BR signal was completed.
The BR signal, generated now, will Set the BUFFER READY flip-flop (73A3C). AND gate 73C8C causes the P-BUSY(73B8B) flip-flop to be Reset and the P-INT9 (74C2A) flip-flop to be set. At the next TPC0, INT9 will be set. At the following TPC3, the signal INT9-P is sent to the processor.

F-STL • COMP

CP 1 - Trigger YF Address 56/5D2
If YF 2^3(1) —— Trigger X Address 56/5D1

CP2 - Advance Shift Register 53/2B1

CP23 - Generate Read Pulse to Memory 54/6A4

CP3 - Reset YF 2^3 56/6D1
If (PRT 120(0) • X9 • Y7) / (PRT 120(1) • X7 • Y3) —— Set Buff Full 54/2D

CP4 - If BUFFER FULL(1) • Tab Comp(1) —— Set TERMINATE 54/4C2
If BUFFER FULL(1) • Tab Comp(1) • (LA/VT/PC) ——Set P-PAD 58/7D3

CP56 - Generate Write Pulse to Memory 54/5B4
If Even Parity —— Generate Read Error 55/6C1, 6C2
If Term(1) —— Generate Buffer Ready 57/5C4
Set Shift Registers Odd or/and Even 57/6A6, 4A6

CP6 - If BUFF FULL(1) —— Reset Comp Reg 57/2B1
If BUFF FULL(1) —— Set FSD 53/6D1

CP7 - If Buff Full(1) —— Set Address to First Location 56/3D3
If YF 2^2(1) • YF 2^1(1) • YF 2^0(1) —— Set YF 2^3 56/7D3
Reset Buffer Register 54/3A2

CP0 ST - If Buff Full(1) —— Reset Print Gate 54/7C4
If Synch(1) • Buff Full(1) • CC17 —— Reset Comp 54/7B5
If CCC 2^6(1) • Synch(0) —— Reset Comp 54/7B3

EXTERNAL TIMING

If Buff Full(1) • Tab Comp(0) • FCCP(1) • Char Pul —— Select E-STL 54/6D1
If Fire Ham —— Reset Tab Comp 54/1B1
If FSD(1) • Fire Ham —— Gate Print Information to Printer 53/4C1

NOTES:

Figure 3.16 Compare Data to Table

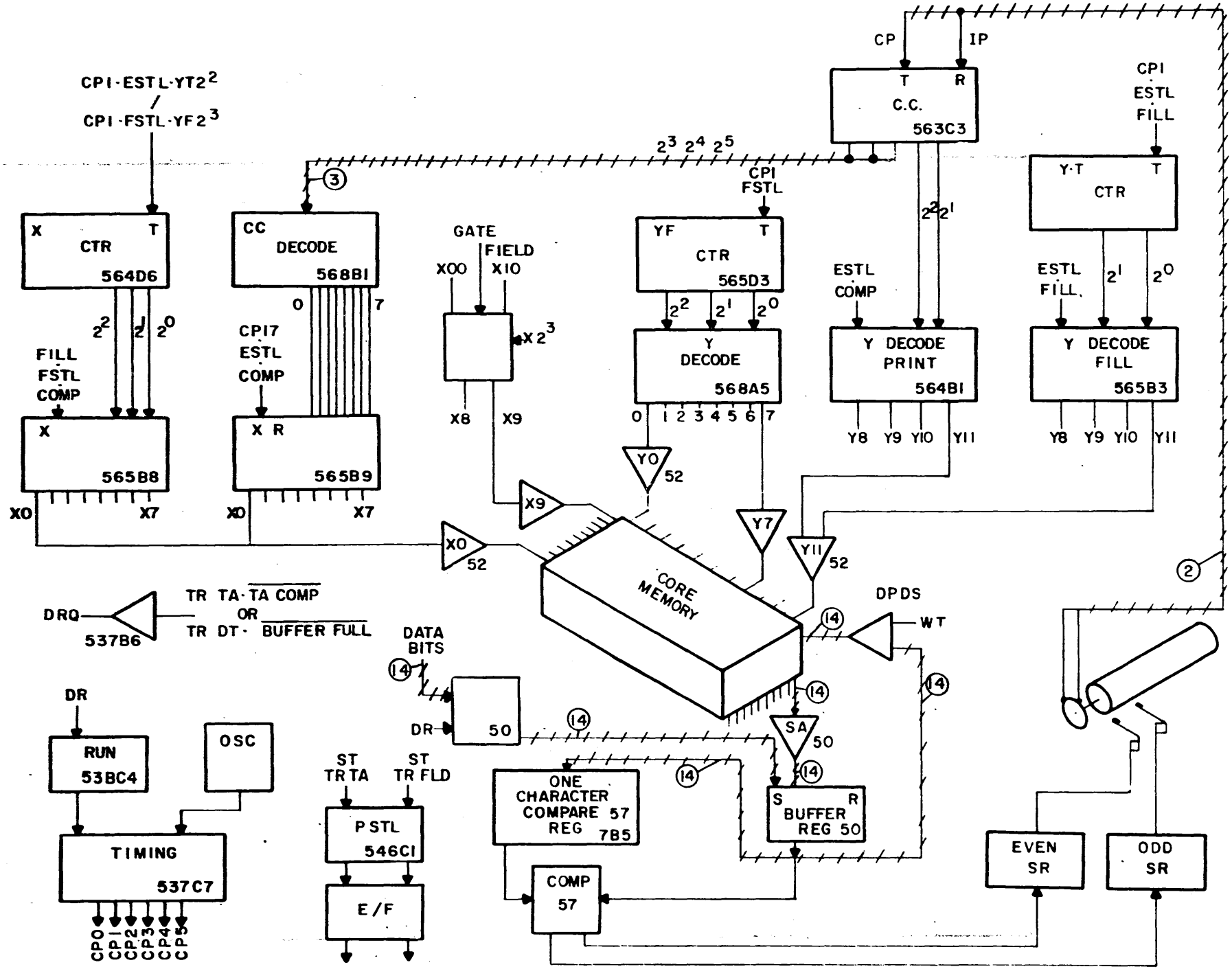


Figure 3.17 Composite Block

3.2.3 Paper Advance Cycle

The CM flip-flops Set by the "B" Address information indicate whether the instruction calls for Print and Paper Advance or Paper Advance Only. Also, they determine whether to advance the paper a specific number of lines, by vertical tab, or by a complete page change. The START signal (73C6C) will cause the API signal (58/8C4) to be generated. The signal API(N), 58/8C4, (Advance Paper Information) Sets VT 58/7D6, LA 58/6D6, or PC 58/5D4, dependent on the control flip-flops Set in the CM. For a Paper Advance Only instruction, API(N) is generated during the SIO2 status level, provided Paper Advance is not already in progress.

If a Paper Advance is in progress and another Paper Advance instruction is received, the P-START (73/B2D) flip-flop will be set. When the Buffer is no longer advancing paper, the signal B-PA-P from the Buffer will be low and flip-flop 73A2A will be set. This will cause the signal RESTART to be generated which will cause START (73D6C) to be generated. The paper will now advance for the second Paper Advance Instruction.

A Print and Paper Advance Instruction does not generate API until the E-STL COMP sequence 58/8C2. If API Sets LA, the signal SET LA 58/6D5 transfers the count, specifying the number of lines to advance paper from the CM into the four stage LAC counter via 58/5C2. The Setting of VT, LA, or PC generates LA/VT/PC(N) via 58/6C1 and primes gates 58/7C3 and 58/7D3.

SET P-PAD at 7D1 is generated during the last F-STL COMP and is used to Set PRE-PAPER ADVANCE 58/8C5. Gate 58/7C3 is enabled and Sets PAD 58/7B4. PAD (0N) generates the Printer Advance (PA) command 57/2D7 which is sent to the Printer.

Each time the Printer advances paper 1 line, PFS (Paper Feed Strobe) at 58/3D1 is returned and triggers the LAC counter. When LAC0(N) 58/4A1 is generated, it enables 58/6C4. The signal D-LA(N) at pin 8 is generated by the LA flip-flop via 58/4D2. The output from 58/7B2 indicates paper has been advanced as directed, either by LA, VT, or PC, and Resets PAD 58/7B4; Resets P-PAD 58/8C5; and Sets COUNT FF 58/6B1.

COUNT FF Zero side output maintains the PA signal so that PA(P) inhibits 58/8C1 and 8C3 from accepting further paper advance information prior to braking of the Printer. The one side output of COUNT FF permits gate 58/6B2 to trigger a four stage counter with each character pulse from the Printer Drum. When CT8 is produced, 58/7A1, COUNT FF is Reset which removes the PA levels. The four stage counter is used to provide the required delay need for braking by the Printer.

4.0 APPENDICES

PRINTER BUFFER MEMORY ADDRESSING PRINT TABLE LOCATIONS

TABLE POSITION	SYMBOL PRINTED		X	Y
1, 2	-	+	X_0	Y_8
3, 4		0		9
5, 6	1	2		10
7, 8	3	4		11
9, 10	5	6	X_1	Y_8
11, 12	7	8		9
13, 14	9	,		10
15, 16	.	@		11
17, 18	%	:	X_2	Y_8
19, 20	#	$		9
21, 22	)	"		10
23, 24	10	(		11
25, 26	?	;	X_3	Y_8
27, 28	>	!		9
29, 30	↑	[		10
31, 32	<	=		11
33, 34	A	B	X_4	Y_8
35, 36	C	D		9
37, 38	E	F		10
39, 40	G	H		11
41, 42	I	J	X_5	Y_8
43, 44	K	L		9
45, 46	M	N		10
47, 48	O	P		11
49, 50	Q	R	X_6	Y_8
51, 52	S	T		9
53, 54	U	V		10
55, 56	W	X		11
57, 58	Y	Z	X_7	Y_8
59, 60	C_r	'		9
61, 62	*	&		10
63, 64	/	¤		11

*standard print table DATA 0000-0079 TABLE 0080-0119

NOTE: Table addressing is explained in the 3333-3335 Control Module Buffer Training Manual pages 3-12 to 3-19

PRINTER BUFFER MEMORY ADDRESSING
DATA LOCATIONS

PRINT POSITION	X	Y	PRINT POSITION	X	Y
1, 2	X_0	Y_0	81, 82	X_5	Y_0
3, 4		1	83, 84		1
5, 6		2	85, 86		2
7, 8		3	87, 88		3
9, 10		4	89, 90		4
11, 12		5	91, 92		5
13, 14		6	93, 94		6
15, 16		7	95, 96		7
17, 18	X_1	Y_0	97, 98	X_6	Y_0
19, 20		1	99, 100		1
21, 22		2	101, 102		2
23, 24		3	103, 104		3
25, 26		4	105, 106		4
27, 28		5	107, 108		5
29, 30		6	109, 110		6
31, 32		7	111, 112		7
33, 34	X_2	Y_0	113, 114	X_7	Y_0
35, 36		1	115, 116		1
37, 38		2	117, 118		2
39, 40		3	119, 120		3
41, 42		4	121, 122		4
43, 44		5	123, 124		5
45, 46		6	125, 126		6
47, 48		7	127, 128		7
49, 50	X_3	Y_0	129, 130	X_8	Y_0
51, 52		1	131, 132		1
53, 54		2	133, 134		2
55, 56		3	135, 136		3
57, 58		4	137, 138		4
59, 60		5	139, 140		5
61, 62		6	141, 142		6
63, 64		7	143, 144		7
65, 66	X_4	Y_0	145, 146	X_9	Y_0
67, 68		1	147, 148		1
69, 70		2	149, 150		2
71, 72		3	151, 152		3
73, 74		4	153, 154		4
75, 76		5	155, 156		5
77, 78		6	157, 158		6
79, 80		7	159, 160		7

NOTE: Field addressing is explained in the 3333/3335 control module buffer training manual, pages 3-20 to 3-23, 3-27 to 3-29 and 3-31.

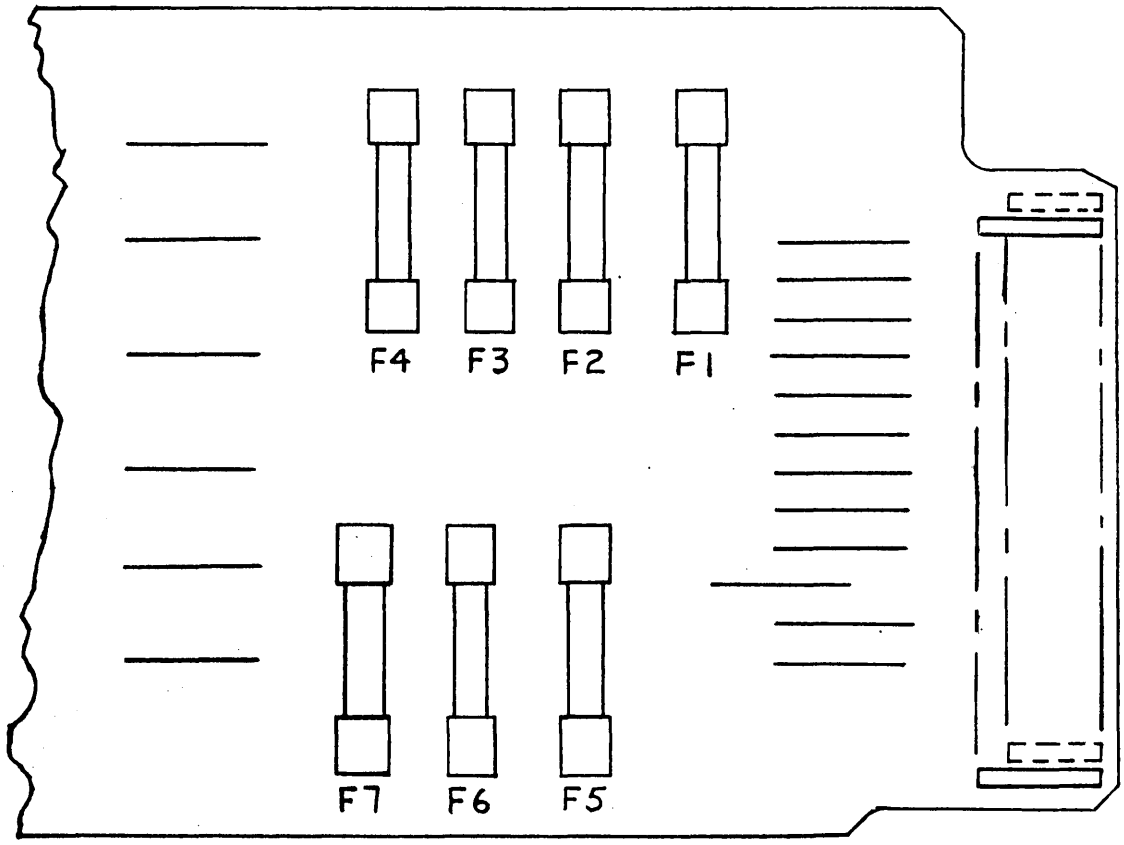
ODD NUMBER COLUMNS

3R031					GATE	3I011 GATE INVERTER	ADVANCE INVERTER 3I011
SR LOC.	COLUMN NUMBER						
7-6	1	3	5	7	12	7-11-5	7-11-22
7-7	9	11	13	15	↓	↓	↓
7-8	17	19	21	23	↓	↓	7-11-23
7-9	25	27	29	31	11	7-11-4	↓
7-10	33	35	37	39	↓	↓	↓
5-15	41	43	45	47	5	5-16-2	7-16-25
5-14	49	51	53	55	↓	↓	↓
5-13	57	59	61	63	↓	↓	↓
5-12	65	67	69	71	4	5-16-3	7-16-24
5-11	73	75	77	79	↓	↓	↓
5-10	81	83	85	87	↓	↓	↓
5-9	89	91	93	95	3	5-16-6	7-16-21
5-8	97	99	101	103	↓	↓	↓
5-7	105	107	109	111	↓	↓	↓
5-6	113	115	117	119	2	5-16-5	7-16-22
5-5	121	123	125	127	↓	↓	↓
5-4	129	131	133	135	↓	↓	↓
5-3	137	139	141	143	1	5-16-4	7-16-23
5-2	145	147	149	151	↓	↓	↓
5-1	153	155	157	159	↓	↓	↓
OUTPUT PIN NUMBER	23	22	7	3			

EVEN NUMBER COLUMNS

3R031 SR LOC.	3R031 COLUMN NUMBER				GATE	3I011 GATE INVERTER	ADVANCE INVERTER 3I011
7-5	2	4	6	8	14	7-11-3	7-11-24
7-4	10	12	14	16	↓	↓	↓
7-3	18	20	22	24	13	7-11-6	7-11-21
7-2	26	28	30	32	↓	↓	↓
7-1	34	36	38	40	↓	↓	↓
6-1	42	44	46	48	10	6-16-2	6-16-23
6-2	50	52	54	56	↓	↓	↓
6-3	58	60	62	64	↓	↓	↓
6-4	66	68	70	72	9	6-16-3	6-16-22
6-5	74	76	78	80	↓	↓	↓
6-6	82	84	86	88	↓	↓	↓
6-7	90	92	94	96	8	6-16-6	6-16-21
6-8	98	100	102	104	↓	↓	↓
6-9	106	108	110	112	↓	↓	↓
6-10	114	116	118	120	7	6-16-5	6-16-24
6-11	122	124	126	128	↓	↓	↓
6-12	130	132	134	136	↓	↓	↓
6-13	138	140	142	144	6	6-16-4	6-16-25
6-14	146	148	150	152	↓	↓	↓
6-15	154	156	158	160	↓	↓	↓
OUTPUT PIN NUMBER	23	22	7	3			

REFER TO THE BELOW CHART AND MARK THE 3M063 BUFFER MEMORY BOARD FOR EASIER TROUBLESHOOTING



3M063/20

Plug-in Location; 1-15

FUSE	BITS	BUFFER REGISTER	BUFFER MEMORY CHAR.
F-1	2^0, 2^2	BR1	odd colm.
F-2	2^1, 2^3	BR1	odd colm.
F-3	2^4, 2^6	BR1	odd colm.
F-4	2^5	BR1	odd colm.
F-4	2^0	BR2	even colm.
F-5	2^1, 2^3	BR2	even colm.
F-6	2^2, 2^4	BR2	even colm.
F-7	2^5, 2^6	BR2	even colm.

LOAD TABLES

Place TEST, LDTBL, and OCSP to the up position. Insert 2 characters into BR using switches labeled BR-1 and BR-2. Depress START. Load 2 more characters and depress START. Continue until 64 characters have been loaded.

NOTE: If an error is made in loading the tables, depress RESET and start over. When table is loaded, place TEST, LDTBL, and OCSP in the down position.

LOAD FIELD

THREE OR MORE DIFFERENT CHARACTERS.

Place TEST, LDFLD and OCSP to the up position. Insert 2 characters into BR using switches labeled BR-1 and BR-2. Depress START. Repeat until 120 characters have been loaded. Then place TEST, LDFLD and OSCP switches to the down position.

LESS THAN THREE DIFFERENT CHARACTERS.

Place TEST and LDFLD to the up position. Insert 2 characters into BR using switches labeled BR-1 and BR-2. Depress START. Place TEST and LDFLD switches to the down position.

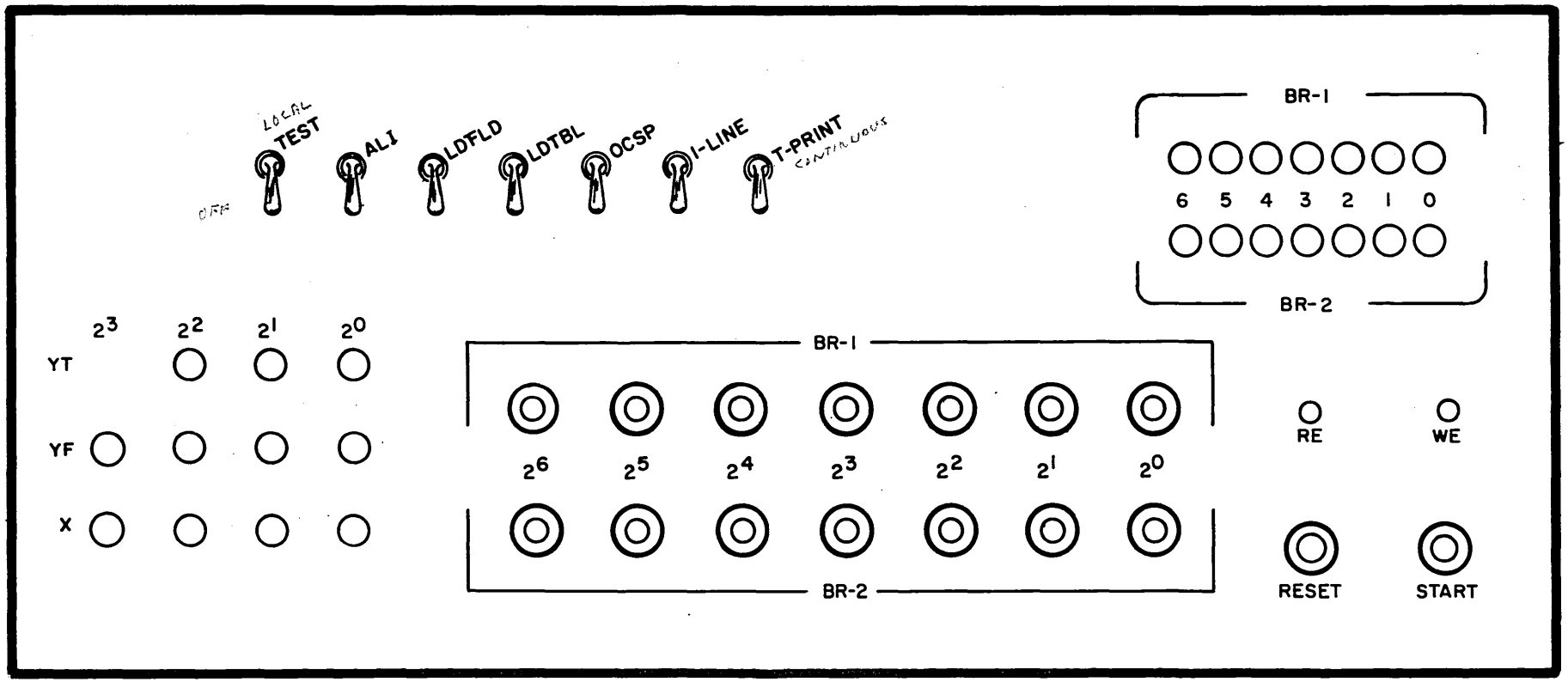
PRINT

1-LINE

Load Tables and Field. Note: Tables may be loaded using T&Ms. Place TEST, 1-LINE, and T-PRINT to up position. Depress START for each line to be printed. When completed, return switches to the down position.

CONTINUOUS

Load Tables and Field. Note: Tables may be loaded using T&Ms. Place TEST to "UP" position. To start printing, place T-PRINT in up position to stop place T-PRINT in the down position. When completed, return switches to the down position.



MAINTENANCE TEST PANEL

PRINTER CONTROL MODULE

SOURCE AND ABBREVIATION LIST

ALI-P	Alarm Inhibit (from BPU)	72D8A
ALRES-P	Alarm Reset (from BPU)	72D8B
BE-P	Buffer Error (to BPU)	72B5E
BR-N	Buffer Ready (from Buffer)	72B5B
BR-P	Buffer Ready (from Buffer)	72B5E
BUF RDY-1N	Buffer Ready	73A3C
BUSY-1N	Busy	73A2B
BUSY HO-P	Busy Hold Off	73C6E
B-PA-N	Paper Advancing (from Buffer)	72D4A
B-PA-P	Paper Advancing	73C2D
COMP-SEL-P	(Will always be low)	72C8C
C-S1/S2-P	S1 or S2 Status Level Present	73C5D
DATA RDY-P	Data Ready (to Buffer)	73A5D
DNF-P	Device Does Not Follow	72A3B
DNF-1N	Device Does Not Follow	72B3D
DRQ-N	Data Request (from Buffer)	72D5C
D1-2^0-P to D1-2^6-P	Data Register One (to Buffer)	74D
D2-2^0-P to D2-2^6-P	Data Register Two (to Buffer)	74B

END TRA-N	End Transfer (from Buffer)	72B5C
END TRA-1N	End Transfer	73A3D
GATE DATA-P	Gate Data	74D8B
GATE DATA A	Gate Data A	74D8A
GATE DATA B	Gate Data B	74C8A
GEN RES-P	General Reset (from BPU)	72D7A
HK/GR "A"-P	HouseKeeping or General Reset "A"	72C6B
HK/GR "B"-P	HouseKeeping or General Reset "B"	72C7B
HK/GR "C"-P	HouseKeeping or General Reset "C"	72C7A
IB00-P to IB04-P	Input Bus "0" (to BPU)	72C
IB10	Input Bus "1" (to BPU)	74B3C
INS TERM-N	Instruction Termination	73D2F
INT 9-P	Interrupt 9 (to BPU)	74B2C
INT 9-1N	Interrupt 9	74C2E
IOS-N	Input/Output Sense	72A4B
IOS-P	Input/Output Sense	72A4C
LA-P	Line Advance (to Buffer)	74A7C
LA-1N	Line Advance	74A7A
LAC-2^0-P to LAC-2^3-P	Line Advance Count (to Buffer)	74A
LACO-N	Line Advance Count Zero	74B7E

LP-N	Low Paper (from Buffer)	72B4C
LP-P	Low Paper	72B4F
LPHO-N	Line Printer Hold Off (from Buffer)	72D5D
LPHO-0N	Line Printer Hold Off	73A6B
LP-HK/GR-P	Line Printer HouseKeeping or General Reset (to Buffer)	73C6D
LP INT-1N	Low Paper Interrupt	72C2F
MODE BUSY-P	Mode Busy	73D5B
N0-P	"N" Count from BPU	72C6B
N1-P		72C7H
N2-P		72C7F
N3-N		72C7B
N4-P		72C7E
N5-N		72C8B
N6-N		72C8C
N-COUNT-N	"N" Count	73D3E
[N-COUNT • IOS] -N	"N" Count and Input/Output Sense	72D4D
OB00-N to OB06-N	Output Bus "0" (from BPU)	72A
OB03-1N	Output Bus "0" Bit "3"	72C2D
OB10-N to OB16-N	Output Bus "1" (from BPU)	72A
OB10-P	Output Bus "1" Bit "0" (from BPU)	72A6D

OB10-1N	Output Bus "1" Bit "0"	74C2B
OB11-P	Output Bus "1" Bit "1" (from BPU)	72A6E
ONB	Operable and Not Busy (to BPU)	73C5F
OP-N	Operable (from Buffer)	72B5A
OP-P	Operable	72B5D
PA-N	Paper Advance	73C3F
PA-1N	Paper Advance	73C3E
PC-P	Page Change (to Buffer)	74A6C
PC-0N	Page Change	74A6A
PRINT-P	Print (to Buffer)	74A8C
PRINT-1N	Print	74A8A
PRT SEL-N	Printer Select	73A7C
PRT SEL-1N	Printer Selected	73A7B
PRT 120-P	Print 120 Col. (to Buffer)	74A4C
P-ADD-N	Printer Address	73D8B
P-BUSY-1N	Pre-Busy	73B8B
P-INT 9-1N	Pre-Interrupt 9	74C2A
P-START-0N	Pre-Start	73B1D
RDR1-P	Reset Data Register One	74D4A
RDR2-P	Reset Data Register Two	74C4A
RE-N	Read Error (from Buffer)	72B4B

RE-P	Read Error	72B4E
RE-1N	Read Error	72B2H
READY-N	Printer Ready	72B3E
RESTART-P	Restart (used for Paper Advance Only)	73A2B
RES P-BUSY-P	Reset Pre-Busy	73C8C
SBRES1-P	Simo Busy Reset One (to BPU)	72C3A
SBRES2-P	Simo Busy Reset Two (to BPU)	72C3B
SB1-N	Simo One Busy (from BPU)	72D7C
SB2-N	Simo Two Busy (from BPU)	72D7D
SCOM1-P	Simo One Complete (to BPU)	73C2E
SCOM2-P	Simo Two Complete (to BPU)	73C2F
SIM2-1N	Simo Two Mode	73A4C
SIM3-P	Simo Three Mode	72C5B
SIO-1N	Start Input/Output	73B4A
SIO1-N	Start Input/Output Status Level One (from BPU)	72D6B
SIO1-P	Start Input/Output Status Level One (from BPU)	72D6D
SIO2-N	Start Input/Output Status Level Two (from BPU)	72D6C
SIO·TPC2-N	TPC2 Timing Pulse During SIO2 Status Level	74B4C
SOP2-N	Simultaneous Operation Two	72A3C
SOP2-P	Simultaneous Operation Two (from BPU)	72A3A

SRA1-P	Simo One Requires Attention (to BPU)	72C3C
SRA2-P	Simo Two Requires Attention (to BPU)	72C3D
START-P	Start Command (to Buffer)	73C6C
STROBE-A	Strobe Control Used in Memory Storage (to BPU)	73C4A
STROBE-B	Strobe Control Used in Memory Storage (to BPU)	73C4B
SYNCH-P	Synchronous Mode (to Buffer)	74A8D
S1-N	Simo One Service Status Level (from BPU)	72D5A
S2-N	Simo Two Service Status Level (from BPU)	72D5B
S-REQ1	Simo 1 Request (to BPU)	73A6C
S-REQ2	Simo 2 Request (to BPU)	73A5C
TPC0-N to TPC8-N	Timing Pulses (from BPU)	72B
TPC0-P to TPC8-P	Timing Pulses	72B
TPCOST-N	TPCO and Stop (from BPU)	72D6A
TPC1/8-N	TPC1 or TPC8	73B2A
TPC30-0N	Flip-Flop Set at TPC3 and Used at TPC1	73D6D
TRANSFER-N	Transfer Data or Tables	73B6E
TR DT-P	Transfer Data (to Buffer)	74A3B
TR TA-P	Transfer Table (to Buffer)	74A3C
TR TA-1N	Transfer Table	74A4B

VT-P	Vertical Tab (to Buffer)	74A7D
VT-0N	Vertical Tab	74A7B
WE-N	Write Error (from Buffer)	72B4A
WE-P	Write Error	72B4D
WE-P	Write Error (to BPU)	72A1A
WE-1N	Write Error	72B1E
WRITE-N	Write Command (from BPU)	72D7B

PRINTER BUFFER

SOURCE AND ABBREVIATION LIST

API (N)	Advance Paper Information	58/8C4
BR (P)	Buffer Ready (To CM)	57/5C4
BR1 RES	Buffer Register One Reset	50/6D4
BR1 - 2^0 (1N)	Buffer Register Number One	50/4A2
BR1 - 2^1 (1N)	Buffer Register Number One	50/4A4
BR1 - 2^2 (1N)	Buffer Register Number One	50/3A3
BR1 - 2^3 (1N)	Buffer Register Number One	50/3A1
BR1 - 2^4 (1N)	Buffer Register Number One	50/2A2
BR1 - 2^5 (1N)	Buffer Register Number One	50/2A4
BR1 - 2^6 (1N)	Buffer Register Number One	50/1B3
BR1 - 2^0 LT	Buffer Register Number One Lights	55/5C1
BR1 - 2^1 LT	Buffer Register Number One Lights	55/4C1
BR1 - 2^2 LT	Buffer Register Number One Lights	55/4C2
BR1 - 2^3 LT	Buffer Register Number One Lights	55/4C3
BR1 - 2^4 LT	Buffer Register Number One Lights	55/3C1
BR1 - 2^5 LT	Buffer Register Number One Lights	55/3C2
BR1 - 2^6 LT	Buffer Register Number One Lights	55/3C3
BR2 RES	Buffer Register Two Reset	50/6D5

BR2 - 2^0 (1N)	Buffer Register Number Two	50/8A2
BR2 - 2^1 (1N)	Buffer Register Number Two	50/7A1
BR2 - 2^2 (1N)	Buffer Register Number Two	50/7A3
BR2 - 2^3 (1N)	Buffer Register Number Two	50/7A4
BR2 - 2^4 (1N)	Buffer Register Number Two	50/6A2
BR2 - 2^5	Buffer Register Number Two	50/6A4
BR2 - 2^6	Buffer Register Number Two	50/5B5
BR2 - 2^0 LT	Buffer Register Two Light	55/5B1
BR2 - 2^1 LT	Buffer Register Two Light	55/4B1
BR2 - 2^2 LT	Buffer Register Two Light	55/4B2
BR2 - 2^3 LT	Buffer Register Two Light	55/4B3
BR2 - 2^4 LT	Buffer Register Two Light	55/3B1
BR2 - 2^5 LT	Buffer Register Two Light	55/3B2
BR2 - 2^6 LT	Buffer Register Two Light	55/3B3
BR-RES (N)	Buffer Register Reset	54/3A2
BUF FULL (1N)	Buffer Full	54/3C1
BUF RES (N)	Buffer Reset	53/7B2
BUF RES (P)	Buffer Reset	53/7B3
B-LA (N)	Line Advance (from CM)	57/5D1
B-PC (N)	Page Advance (from CM)	57/6D1
B-VT (N)	Vertical Tab (from CM)	57/6D2

CCC2^{6} (1N)	Continuous Character Counter	54/7A5
CC2^{0} (1N)	Character Counter	56/3C3
CC2^{1} (1N)	Character Counter	56/3C2
CC2^{2} (1N)	Character Counter	56/3C1
CC2^{3} (1N)	Character Counter	56/4C3
CC2^{4} (1N)	Character Counter	56/4C2
CC2^{5} (1N)	Character Counter	56/4C1
CC17 (N)	Character Count 17_8	54/2C1
CC40 (N)	Character Count 40_8	54/1C1
CHAR PUL (N)	Character Pulse	54/4A6
CHAR PUL (P)	Character Pulse	54/4A4
COMP (1N)	Compare Cycle	54/7A4
CONT PRINT (N)	Continuous Printing	53/8C5
COUNT FF (0N)	Count Flip-Flop	58/6B1
CO - 2^{0} (1N)	Compare Register	57/7B5
CO - 2^{1} (1N)	Compare Register	57/7B6
CO - 2^{2} (1N)	Compare Register	57/6B5
CO - 2^{3} (1N)	Compare Register	57/5B5
CO - 2^{4} (1N)	Compare Register	57/4B5
CO - 2^{5} (1N)	Compare Register	57/4B6
CP0 (P)	Clock Pulse	53/8A2
CP0 (N)	Clock Pulse	53/8A4

CP0 STP	Clock Pulse Zero and Stop	53/8A3
CP1 (N)	Clock Pulse	53/7A5
CP1, 2, 3 (N)	Clock Pulse	53/5A6
CP 17	Clock Pulse	56/1C1
CP2 (N)	Clock Pulse	53/7A6
CP3 (N)	Clock Pulse	53/7A7
CP4 (N)	Clock Pulse	53/5A8
CP4 (P)	Clock Pulse	53/5A7
CP45 (N)	Clock Pulse	53/7A8
CP5 (N)	Clock Pulse	57/4A8
CP56 (N)	Clock Pulse	53/5A5
CT2 (1N)	Count 2	58/7A1
CT8 (1N)	Count 8	58/6B1
C0 (1N)	Clock	53/7C7
C1 (1N)	Clock	53/7B1
C2 (1N)	Clock	53/7C8
C3 (1N)	Clock	53/6B1
C4 (1N)	Clock	53/6C5
C5 (1N)	Clock	53/5B1
DR (N)	Data Ready (from CM)	57/6C1
DR (P)	Data Ready (from CM)	57/6D3

DRQ (N)	Data Request	53/7B6
DRQ (P)	Data Request (to CM)	57/5C2
D1 - 2^0 (1N)	Data (from CM)	57/5D2
D1 - 2^1 (1N)	Data (from CM)	57/5D3
D1 - 2^2 (1N)	Data (from CM)	57/4D1
D1 - 2^3 (1N)	Data (from CM)	57/4D2
D1 - 2^4 (1N)	Data (from CM)	57/4D3
D1 - 2^5 (1N)	Data (from CM)	57/3D1
D1 - 2^6 (1N)	Data (from CM)	57/3D2
D2 - 2^0 (1N)	Data (from CM)	57/2D1
D2 - 2^1 (1N)	Data (from CM)	57/2D2
D2 - 2^2 (1N)	Data (from CM)	57/2D3
D2 - 2^3 (1N)	Data (from CM)	57/8D3
D2 - 2^4 (1N)	Data (from CM)	57/7D4
D2 - 2^5 (1N)	Data (from CM)	57/7D5
D2 - 2^6 (1N)	Data (from CM)	57/7D6
D-LA (N)	Delayed Line Advance	58/4D2
END TRANS (P)	End Transfer	57/2B5
E - STL (N)	TABLE Status Level	54/6B1
E-STL·COMP (N)	"E" Status Level and Compare Cycle	53/6B3
E-STL-CP3 (P)	Clock Pulse 3 During E Status Level	56/8D3

E-STL·FILL(N)	"E" Status Level and Fill Cycle	53/5B5
FCCP (1N)		54/3A3
FILL (1N)	Fill Cycle	54/8A3
FILL/COMP (N)	Fill or Compare Cycle	54/8C2
FIRE HAM (N)	Fire Hammers	54/4B3
FSD (1N)	Fire Solenoid Drivers	53/6D1
F-STL (N)	FIELD Status Level	54/6B2
F-STL·COMP (N)	"F" Status Level and Compare Cycle	53/5B3
F-STL·COMP (P)	"F" Status Level and Compare Cycle	53/5B6
F-STL·FILL (N)	"F" Status Level and Fill Cycle	53/5B7
GATE 1 (N)	Gate Signal	53/4C3
GATE 2 (N)	Gate Signal	53/4C7
GATE 3 (N)	Gate Signal	53/4B1
GATE 4 (N)	Gate Signal	53/4B5
GATE 5 (N)	Gate Signal	53/4A1
GATE 6 (N)	Gate Signal	53/4C4
GATE 7 (N)	Gate Signal	53/4C8
GATE 8 (N)	Gate Signal	53/4B2
GATE 9 (N)	Gate Signal	53/4B6
GATE 10 (N)	Gate Signal	53/4A2
GATE 11 (N)	Gate Signal	53/3C1

GATE 12 (N)	Gate Signal	53/3C3
GATE 13 (N)	Gate Signal	53/3B1
GATE 14 (N)	Gate Signal	53/3B3
GATE FIELD (N)	Gate Field	56/5B1
INH COMP (P)	Inhibit Compare Cycle	54/8B4
INOP (N)	Inoperable	53/8B3
INOP (P)	Inoperable	53/8B5
LA (1N)	Line Advance	58/6D6
LACO (N)	Line Advance Count Zero	58/4A1
[LA/VT/PC] (N)	Line Advance, or Vertical Tab, or Page Change	58/6C1
LD TBL/FLD (N)	Load Table or Field	54/8B1
LOCAL - LT	Local Light	55/7B7
LP (P)	Low Paper (from printer to CM)	57/3C1
LPHK/GR (N)	Line Printer HouseKeeping or General Reset (from CM)	57/8D4
LPHO (P)	Line Printer Hold Off	55/7B6
OP (P)	Operable (to CM)	57/5C3
OSC "A"	Oscillator "A" Signal	53/8D1
OSC "B"	Oscillator "B" Signal	53/8D2

PA (N)	Paper Advance	58/5B3
PA (P)	Paper Advance	58/5A1
PA (P)	Paper Advance (to CM)	57/5C1
PAD (N)	Paper Advance (to Printer)	57/2D7
PAD (0N)	Paper Advance Flip-Flop	58/7B4
PAD RES (P)	Paper Advance Reset	58/7B2
PAD RES A (P)	Paper Advance Reset A	58/8B3
PC (1N)	Page Change	58/5D4
PFS (P)	Paper Feed Strobe (from Printer)	57/2D6
PRINT (N)	Print (from CM)	57/7C1
PRT 120 (1N)	Print 120 Col.	57/1B1
P-CHAR PUL (P)	Character Pulse (from Printer)	57/3D3
P-COM (1N)	PreCompare Flip-Flop	54/8C1
P-INDEX (P)	Index Pulse (from Printer)	57/3D4
P-OP (N)	Operable Signal (from Printer)	57/1C5
P-PAD (1N)	Pre-Paper Advance	58/8C5
P-PC (P)	Page Change (from Printer)	57/2D5
P-START (N)	Start (from CM)	57/8D1
P-VT (P)	Vertical Tab (from Printer)	57/2D4
RE (1N)	Read Error	55/6C4
RE (P)	Read Error (to CM)	57/4C3
READ (N)	Read Memory	54/5A4

READY (N)	(from Printer)	57/8C6
READY (P)	(to CM)	57/7C2
RELT	Read Error Light	55/6B1
RES COMP REG (P)	Reset Compare Register	57/3B3
RES PRINT (P)	Reset Print Gate	54/8A1
REMOTE-LT	Remote Light	55/7B8
SET LA (P)	Set Line Advance	58/6D5
SET P-PAD (P)	Set Pre-Paper Advance	54/5C3
SET SR EV (P)	Set Shift Register Even	57/4A5
SET SR ODD (P)	Set Shift Register Odd	57/6A6
SET 1ST COMP (P)	Set First Compare	54/4D6
START (P)	(from CM)	57/8D2
STR INH (P)	Strobe Inhibit	54/5B3
SYNC (N)	(from CM)	57/8C1
SYNC (P)	(from CM)	57/8C1
SYNC (1N)	Synchronous Mode	53/8B6
TAB COMP (1N)	Table Complete	54/2B6
TERM (1N)	Terminate	54/4B1
TEST (P)	(from Test Panel)	53/5D1
TOF (1N)	Top Of Form	58/7B3
T-START (N)	(from Test Panel)	53/7D1

[T-STOP · TEST](P)	(from Test Panel)	58/2C3
VT (1N)	Vertical Tab	58/7D6
WE (1N)	Write Error	55/7C4
WE (P)	Write Error (to CM)	57/4C2
WELT	Write Error Light	55/6B2
WRITE	Write Command	54/5B4
XR/W	X Read or Write	51/4D1
XR00 (N) to XR70 (N)	X Addresses from Character Counter	56
X0 to X9	X Address Lines	52
X7 (N)		52/3B1
X9 (N)		52/2B1
X0 (P) to X9 (P)	X Addresses	56
X00 (N) to X70 (N)	X Addresses from X Counter	56
$X2^0$ (1N) to $X2^3$ (1N)	X Counter	56
$X\text{-}2^0$ LT to $X\text{-}2^3$ LT	X Address Light	55
$YF2^0$ (1N) to $YF2^3$ (1N)	Y Field Counter	56
$YF\text{-}2^0$-LT to $YF\text{-}2^3$-LT	Y Field Counter Light	55
YR/W	Y Read or Write	51/3D1
$YT2^0$ (1N) to $YT2^2$ (1N)	Y Table Counter	56
$YT\text{-}2^0$-LT to $YT\text{-}2^2$-LT	Y Table Counter Light	55

Y0 to Y11	Y Address Lines	52
Y3 (N)		52/6D2
Y7 (N)		52/4D2
Y0 (P) to Y11 (P)	Y Address	56
1ST COMP	First Compare	54/4C1
120 CHAR PRT	120 Character Printer	57/1C2

3383

CONTROL MODULE

3383
CONTROL MODULE

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LIST OF ILLUSTRATIONS

3383 Control Module

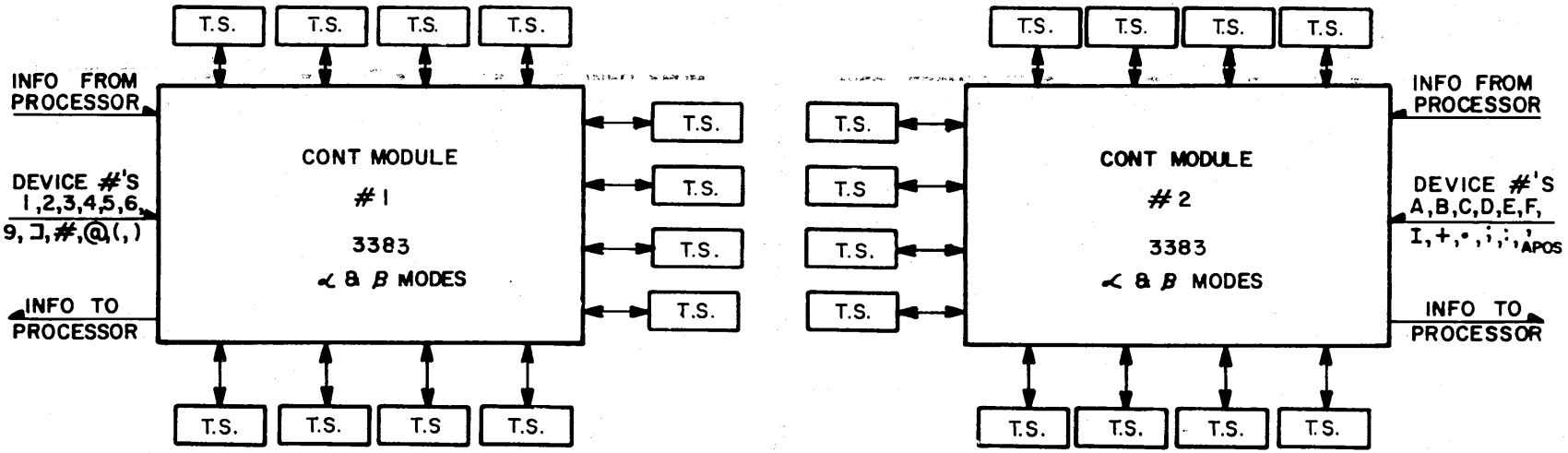
1.0 Introduction

The 3383 control module allows the 3301 processor to function with the model 581, 582 or 681 tape stations. Two models of the control module are available, the 3383-6 has capabilities for 6 tape stations while the 3383-12 provides for 12 tape stations. Either model may have any mixture of 581, 582 or 681 tape stations attached. A maximum of two 3383-12 control modules may be attached to the 3301 processor allowing up to 24 tape stations to be used. The address assignments for the control modules and tape stations attached are as given in figure 1-1.

Internally the control module has two separate modes called α (alpha) and β (Beta) which provides capabilities to function with any two of the attached tape stations simultaneously. That is the control module can execute two reads, two writes, a read and write or any combination of operations as long as the same tape station is not being used.

The α mode will be used for all instructions performed in the SIMO-1 mode of the processor. The β mode will be used for all instructions performed in the SIMO-2 mode. If the processor is equipped with a SIMO-3 mode a SIMO-3 instruction may use either α or β. The first preference being the α mode, if α is busy the β mode will be selected.

In any case if the α & β modes or device is not available for use the instruction will terminate on a busy or inoperable interrupt in the processor. (figure 1-2)



First 2 x 12				Second 2 x 12			
First 2 x 6		Second 2 x 6		Third 2 x 6		Fourth 2 x 6	
Address Symbol	Station Number	Address Symbol	Station Number	Address Symbol	Station Number	Address Symbol	Station Number
1	01	9	11	A	21	I	31
2	02	⌐	12	B	22	+	32
3	03	#	13	C	23	.	33
4	04	@	14	D	24	;	34
5	05	(	15	E	25	:	35
6	06	)	16	F	26	'	36

FIGURE 1-1. 3383 α & β MODES

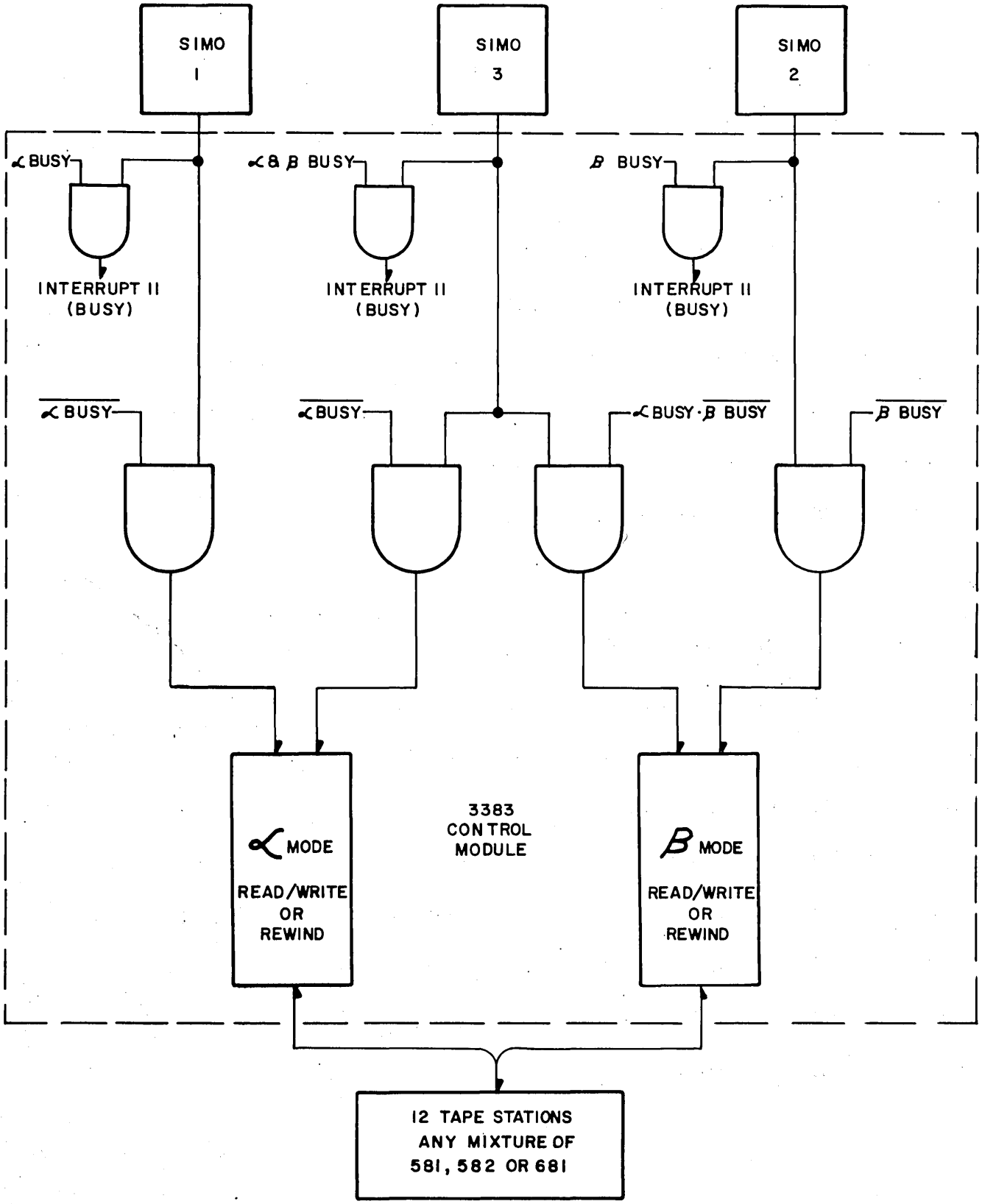


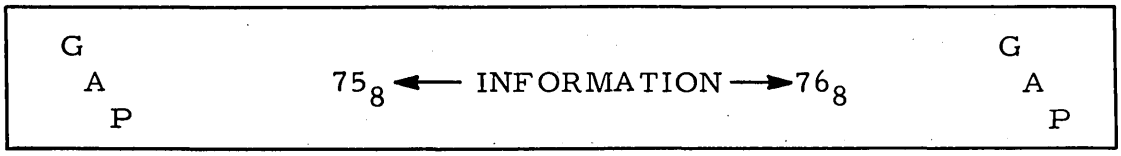
FIGURE 1-2. 3383 MODE SELECTION

The control module contains all logic necessary for the transfer of data to and from the processor, accuracy control, tape station selection and control. Logic is also incorporated to determine the type of tape station to be used in an instruction (581, 582 or 681).

1.1 Related Devices

The 581 tape station records information at a 33.3 KC rate with a tape speed of 100 in/sec giving a packing density of 333 characters for each inch of tape. Rewind speed is also 100 in/sec. Accuracy control during a write consists of a parity check of the bits sent to the write head for each character. If the character has correct parity a write verify pulse is returned to the control module for each character. The tapes prepared on a 581 are not compatible with a 582 or 681 tape station.

The 582 tape station records information at 66.6 KC at a tape speed of 100 in/sec giving a packing density of 666 characters per inch of tape. Rewind speed is 150 in/sec. Accuracy control during a write consists of reading each character approximately 2 millisec after it is written and checking for proper parity. If correct parity is not found the signal R/WPE is sent to the control module as a negative signal. Tapes prepared on a 582 with the LONG GAP switch set may be used on the 681 tape station. The foremat of the information recorded on the 582 consists of a first guard character (75_8) followed by the block of information and then a last guard character (76_8).



582 TAPE FOREMAT

The writing of the guard characters is a function the control module and the characters do not appear in memory during reading or writing. Accuracy checks are performed to insure that the guard characters are present.

The 681 tape station records information at 120 KC with a tape speed of 150 in/se giving a packing density of 800 characters per inch of tape. A 100 KC switch may be set to change the recording density to 100 KC which gives a packing density of approximately 666 characters per inch. Tapes prepared on a 681 with the 100 KC switch set may be used on the 582 tape station. The function of changing the recording rate is a control module responsibility. The rewind speed of a 681 is 225 inches per second. The tape will either rewind to BTC or to the load point depending upon the programmed instruction. Each character written to a 681 tap station is read approximately 1.4 millisecs later and checked for parity. If incorrect parity is found the signal R/WPE is transmitted to the control module as a negative signal. Tape foremat on the 681 is identical to the 582 tape station.

The returns from the tape stations are inspected in the control module to determi which type of tape station is to be used in a particular instruction. Two returns are used to determine this, R/WPE (called WR VER from the 581) and R/WCHK. The following chart indicates the status of the returns when the tape station is in the static condition:

TAPE STATION	[R/WPE] /WR VER	R/WCHK
581	Negative - Goes Positive for each Character written with Good Parity	NON EXISTENT
582	Positive - Goes Negative on Error only	Negative - Goes Positive when 1st Character is read. Goes Negative 120 us after la Character is read.
681	Positive - Goes Negative on Error only	Positive - Goes Negative when 1st Character is read and positive again 41 usec after the last character is read

2.0 Applicable Instructions

2.1 Read Instructions

Read instructions are a means to transfer data from a selected tape station into the main memory of the processor. The instructions terminate upon detection of a gap on magnetic tape. If address equality is found before the gap no further information is inserted into the memory and the tape proceeds to run to the gap. If address equality is found before the gap or a error occurs the instructions terminate with the SRA interrupt indicator set. If no errors occur and address equality is not detected the instructions terminate with the SCOM interrupt indicator set. The interrupt indicators for the three simultaneous modes are:

	SCOM	SRA
SIMO-1	17	14
SIMO-2	16	13
SIMO-3	15	12

Guard Characters if present are not stored in the memory.

OPERATION	N	A	B
RF 1 4 RF 2 5 RF 3 D	Device #	HSM Location To Receive The First Character	HSM Location To Receive The Last Character (Limit Address)

Since all read instructions are performed in the simultaneous modes the A and B registers are not used in the actual transfer of data into the memory. The SP memory provides two additional registers for each simultaneous mode to replace

the function of A and B. The contents of A&B are transferred into the appropriate registers during the SI01 & SI02 status levels which preceed the actual execution of the instruction.

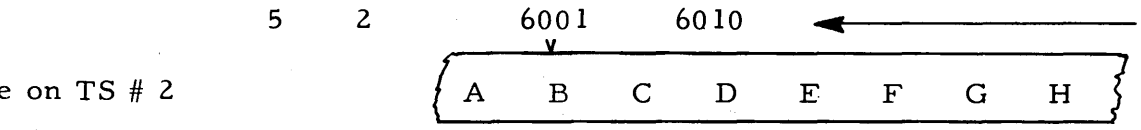
	A - ADDRESS	B - ADDRESS
SIMO-1	S-Register	T-Register
SIMO-2	C-Register	E-Register
SIMO-3	F-Register	G-Register

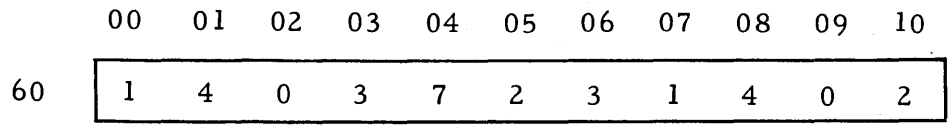
FINAL SETTINGS:

S_f, C_f or F_f = HSM location of the last character inserted into the memory +1.

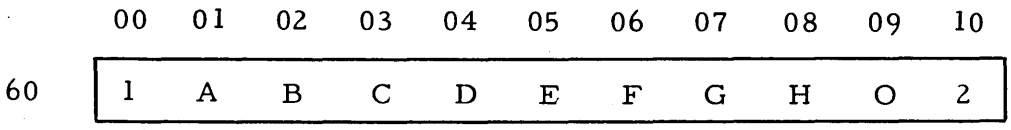
T_f, E_f or G_f = Same as B initial

EXAMPLE:





HSM BEFORE



HSM AFTER

FINAL SETTINGS: C_f - 6009 E_f - 6010

INT 16 set if no errors

Reading in reverse is also permitted by utilizing the following operation codes. The sequence is the same as forward reads except the characters are inserted into the

memory right to left and the tape runs in reverse.

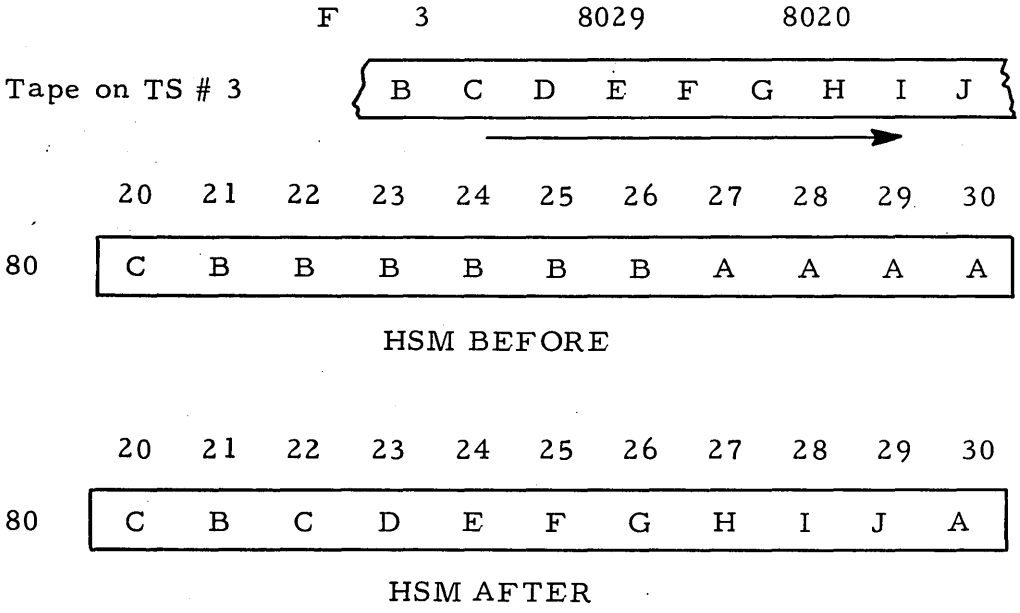
OPERATION	N	A	B
RR 1 / RR 2 / RR 3 — 6 / 7 / F	Device #	HSM Location To Receive The First Character	HSM Location To Receive The Last Character (Limit Address)

FINAL SETTINGS:

S_f, C_f or E_f = HSM location of the last character inserted into memory minus 1

E_f, T_f or G_f = B initial

EXAMPLE:



F_f - 8020 G_f - 8020

INT 15 set if no errors

2.2 Write Instructions

Write instructions provide a means of transferring information from the HSM to a designated tape station. The instructions terminate on address equality. In the case of writing to a 582 or 681 tape station guard characters are automatically generated before and after the block of information. Guard characters do not appear in the memory write out area. Termination of a write instruction is signified by setting the appropriate interrupt indicator. If no errors occur either INT 15, 16 or 17 is set (SCOM). An error will allow INT 12, 13 or 14 to be set (SRA).

OPERATION		N	A	B
WR-1	8	Device #	HSM Location Of First Character To be Written	HSM Location Of Last Character To Be Written
WR-2	9			
WR-3	H			

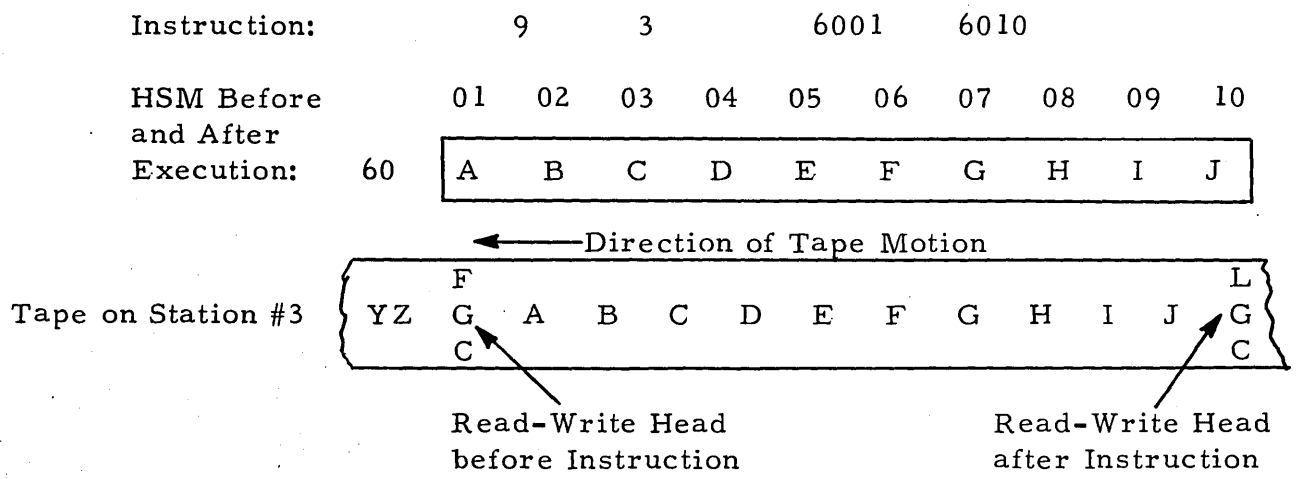
Writes are performed in the simultaneous modes consequently the S, C or F register replaces the A register functions and the T, E or G register replaces the B register functions.

FINAL SETTINGS:

S_f, C_f or F_f - HSM last character written +1

T_f, E_f or G_f - B initial

EXAMPLE:



Final Settings: $(C)_f$ - 6011 $(E)_f$ - 6010

(Guard Characters on 582/681 only)

2.3 Erase Instructions

The erase instructions allow a specified length of tape to be erased on a designated tape station. The instructions are identical to the write instructions except no information is written on the tape. The amount of tape erased depends upon the A&B addresses. For example if 666 characters are specified to a 582 tape station approximately 1 inch of tape is erased. (Plus UTS time)

OPERATION		N	A	B
ER-1 ER-2 ER-3	* > %	Device #	HSM Address Of Left Most Character*	HSM Address Of Right Most Character*

* The number of characters between the A&B address determine the amount of tape to be erased.

FINAL SETTINGS:

S_f, C_f or F_f - HSM location of rightmost character +1

T_f, E_f or G_f - B initial

2.4 Control Device Instructions

The control device instructions provide a means to rewind a tape station to BTC, rewind a 681 to the load point or to rewind one gap on a designated tape station.

OPERATION		N	A	B
CD-1	2	Device #	0000	B^0, B^1 & B^2 = 000
CD-2	3			B^3 - 1-Rewind to BTC
CD-3	B			B^3 - 2-Rewind 681 to load point
				B^3 - 4-Rewind one gap

2.5 Test Device Instruction

The test device instruction provides a means to test specific conditions of a designated tapes station or test the condition of various indicators in the control module. If the control module indicators are specified the mode α or β , must also be indicated. This instruction is performed in the normal mode only. If the tested condition(s) is present a transfer of control to B is performed if not the next instruction in sequence is performed.

FORMAT

OPERATION - S

N - Specifies Magnetic Tape Station

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	By Mode	Test Function
A_0	$2^0 = 1$	1		Is device inoperable?
A_0	$2^1 = 1$	2		Is tape in motion?
A_0	$2^2 = 1$	4		Has ETW been sensed?
A_0	$2^3 = 1$	8		Is tape positioned on BTC?
A_0	$2^4 = 1$	&		Is tape moving in reverse?
A_0	$2^5 = 1$	-		Is splice detected?
A_1	$2^0 = 1$	1	✓	Is there a Parity Error (PE) on read or write?
A_1	$2^1 = 1$	2	✓	Is there a Magnetic Tape Alarm (MTA)?
A_1	$2^2 = 1$	4	✓	Has address equality been detected before a gap? (Long Block)
A_1	$2^3 = 1$	8	✓	Is the EF/ED Indicator Set?
A_1	$2^4 = 1$	&	✓	Is switch (α or β) busy?
A_3	$2^0 = 1$	1		Simo 1 Mode or α switch
A_3	$2^1 = 1$	2		Simo 2 Mode or β switch
A_3	$2^2 = 1$	4		Simo 3 Mode

Unused characters must be zeros and are not to be used by programming.

A_3 must be specified for those functions with a check (✓) in the "By Mode" column.

B Address - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

3.0 Control Module Operation

3.1 Tape Selection

Following staticizing an input output instruction performs the SI01 and SI02 status levels during which the N character is present in the control module. The N character is recognized by the logic in the control module and if the N character is the address of a tape station connected to the particular control module the signal TNC is produced (35 C7B). The 3Z051 plug ins (35D7D & 35D6C) are connected in such a manner that only tape numbers for the particular control modules are recognized. TNC is combined with $\overline{IOS}$ to produce TI (Tape Instruction). A decision is made at this time as to which mode, α or β is to be used. If the instruction is not a SIMO-2 instruction (SOP-2) or not a SIMO-3 instruction with the α mode busy the signal αTI is produced by gate 35A7B indicating α is to be used. If either of the conditions above are present βTI is produced to select the β mode (35A7A).

A check is now made to determine if the tape station being requested to already in use. The control module contains two registers to store tape numbers while the instructions are actually being performed. One functions for the α mode (α N print 45) and the other for the β mode (β N print 46). If either mode is busy the new tape number is compared against the respective register by the compare networks or print 45 & 46 area D-2. A comparison produces an address compare signal (α or β ADC) which will prevent the operable not busy return from being sent to the processor (35 B2A/B2B). The ONB return not being sent allows the INT 11 indicator to be sent in the processor and interrupt occurs.

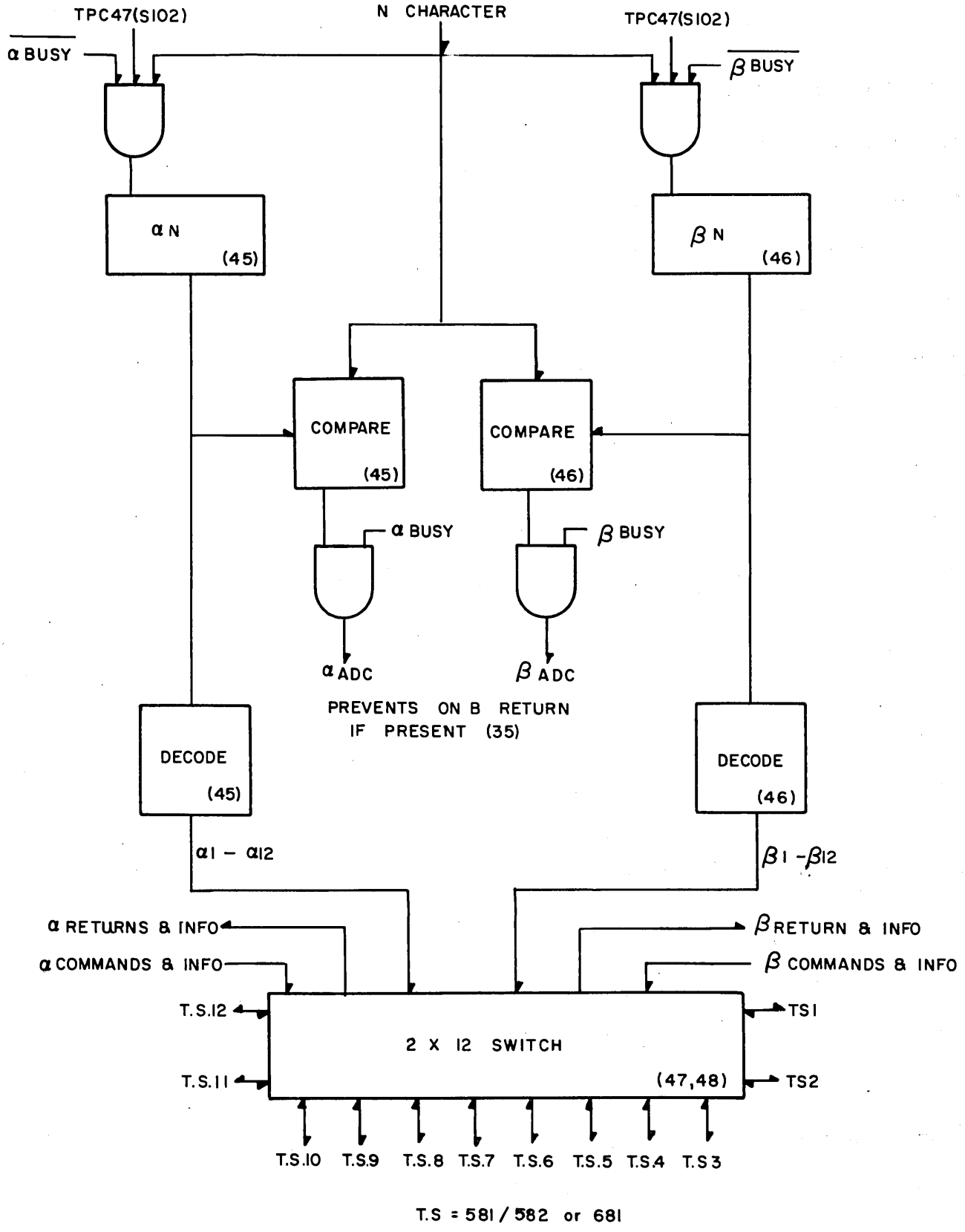


FIGURE 3-1. TAPE STATION SELECTION

If a comparison is not found the tape number is gated to the α or β N registers for decoding (45D7A or 46D7A). The signals α busy or β busy are not produced until the end of SI02 unless they are already present from a previous instruction. The 2^0, 2^1 and 2^2 bits are decoded by a binary to octal decoder (3G061 plug in). The decoder produces 6 outputs to correspond with the configurations 1 through 6. The outputs of the decoder are combined with the 2^3 stage to choose one out of a possible 12 tape stations by producing the appropriate α or β signal. (α 1 to α 12 or β 1 to β12). These signals are sent to a 2 x 12 switch to allow commands to be sent out to the selected tape station (Print 47) and returns to be receive from the selected tape station (Print 48). The switch logic is duplicated to allow a tape station to be connected for both α & β modes simultaneously. The control module is now in communication with the desired tape station and the instruction may be executed.

3.2 Read Operation

The general operation of a read consist of selecting the desired tape station and sending the proper commands. The information for the selected tape station enters the control module through the 2 x 12 switch and is gated into either the A or B buffer depending upon the condition of the write read data control (WRDC) flip flop. WRDC determines whether the character is to be eventually placed into the C0 or C1 position of a diad in the main memory. The flip flop is initially set to the configuration of the $A^3 2^0$ bit and will change state for each character received from the tape station. The characters are placed into the A&B buffers alternately. When the A&B buffers are full a gate signal "dumps" the characters into the C&D

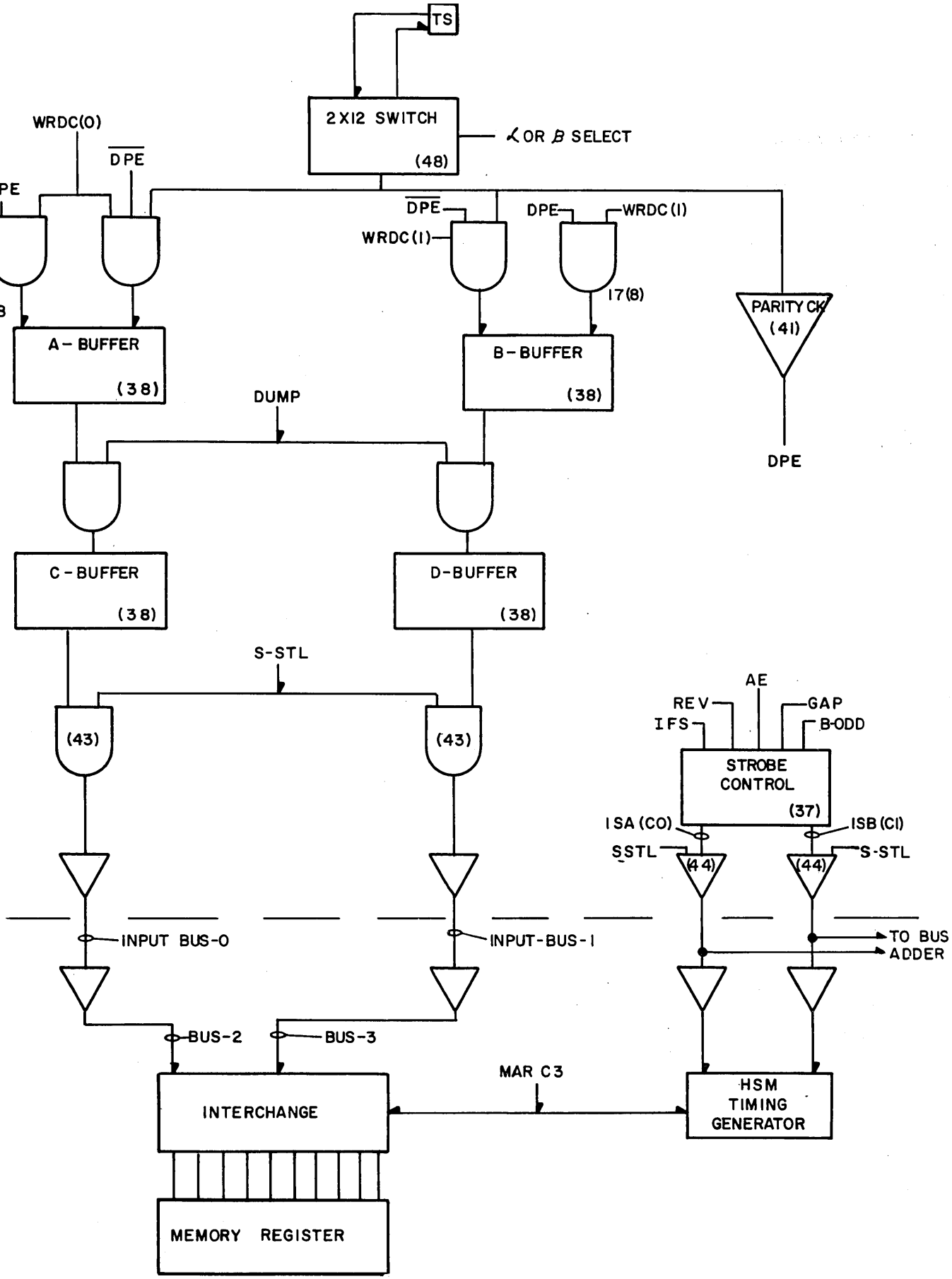


FIGURE 3-2. READ INFORMATION FLOW

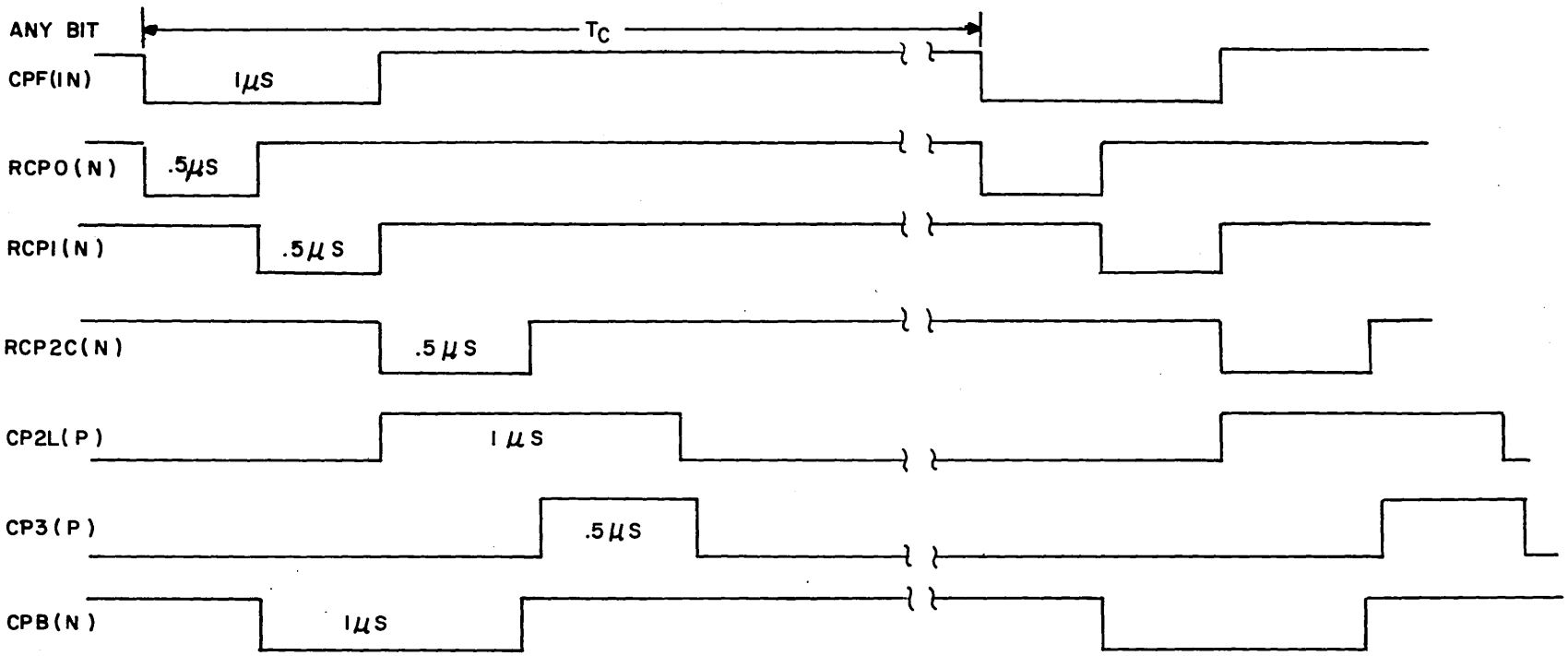
buffers and a status level is requested to transfer the diad into the main memory. The A&B buffers are reset to await the arrival of the next pair of characters from the tape station. The cycle continues until terminating conditions are detected. The last character(s) is transferred and either the SCOM return sent to the processor or the SRA return sent if an error occurred during the read. Each characte is checked for parity as it enters the control module. A $17_{(8)}$ is substituted for the character if even parity is found unless ALI is set which allows the actual character to be sent to the processor. The instruction continues to completion and the SRA return is sent to the processor.

3.2.1 Read Logic

During SI01 the $A^3 2^0$ bit is inspected to set the WRDC flip flop to the set state if 2^0 is present (39D2B) indicating the first character is to be placed into the C^1 position of the first diad. The IFS (initiate first strobe) flip flop is also set if 2^0 is present and a forward read is to be performed (42B4A) or if 2^0 is not present and a reverse read is to be performed (42B5B). IFS controls the strobes in the HSM for the first transfer of information from the control module. In a forward read with IFS set the C^0 strobe for the first diad will be generated but not the C^1 strobe since the character being read is to be inserted the C^1 location. The situation for a reverse read is opposite in that if the IFS flip flop is set the C^1 strobe is generated but not C^0. The signals ISA and ISB (37C4D & 37C4E) if present allow the strobes to be generated by controlling the signals STROBE A (44C8A) and STROBE B (44C7A) which are sent to the processor. The situation of controlling the strobes will also

arise when the last character(s) are transferred which is determined by inspecting the B-ODD flip flop (42 A5A/42 A2B). This flip flop is set according to the $B^3 2^0$ bit during SI02.

As the characters arrive from the tape station a set of timing pulses are created for each character to control the gating of buffers, resetting of buffers etc. Any one bit being received triggers the CPF flip flop (39C3B) to the set state and starts the train of pulses as shown in figure 3-3. The characters are gated into either the A or B buffers at RCP2C by the signals RDA or RDB (39B4F & 39B3K). In order to generate RDA or RDB the PMT RW (Permit Read or Write 39A5C) flip flop must be set. If the read is from a 581 tape station the flip flop is already set (TPC4 · SI02). If the read is from a 582 or 681 the flip flop is not set until the first character has been recognized as a guard character. The FGC flip flop (41B4A) is set if the proper character is recognized at RCP2C of the first character. The PMT RW flip flop is not set until RCPO of the next character consequently the first guard character was not placed into the buffers. The second character would be placed into the appropriate buffer by its RCP2C. The WRDC flip flop is triggered to the opposite state at the end of CP2L (39D2D) in preparation for the next character. The sequence continues until conditions are found to transfer the A&B buffers to the C&D buffers. Gate 39D7D normally recognizes this condition and creates the signal DUMP at the RCPO of the next character after the gate conditions are recognized. RCP1 now resets the A&B buffers (39B6A) and RCP2C inserts the next character into A or B.



T_C DEPENDS UPON THE RATE AT WHICH CHARACTERS ARE RECEIVED

120KC -	APPROX	8.3μSEC.
66KC -	"	15μSEC
33KC -	"	30μSEC

FIGURE 3-3. READ TIMING

The character(s) in C&D must be inserted into the processor memory by a status level. The signal DUMP sets the REQ flip flop (37B3B) and a request is sent the processor (figure 3-4) for a status level (44C6A, B7B or B6C). The status level is produced and gates the contents of the C&D buffers to input busses 0 & 1 (43B4A & 43B5A). The processor would have addressed the memory with the appropriate register and placed the character(s) into the proper position of the MR. The C&D buffers are reset (39B5B) at TPC5 of the S-status level and are ready for the next set of characters. This sequence continues until terminating conditions are found.

The read instructions terminate when a gap has been detected after at least one character has been read in. The first CP3 sets the control counter (CTC) flip flop (40C2C) and allows the counter to be triggered every 10 us (100 KC osc). The counter is reset for each character from the tape by CPF/CPB. If no characters are received the counter triggers to a count of 12 and gate 35D6C recognizes that approximately 120 us have passed without a character being received to set the PRE GAP flip flop (35D5A). The GAP flip flop is set at TPC3 if a guard character has been detected or a 581 tape station is being used. The signal SGAP generates the DUMP signal (39B8A/39B8B) to send the last character(s) to the processor. The B-ODD flip flop is inspected to determine which strobes are to be generated for the last diad (37D4A/37D3A).

GAP being set allows P-term (37B6B) to set which in turn sets TERM (37B6F) by

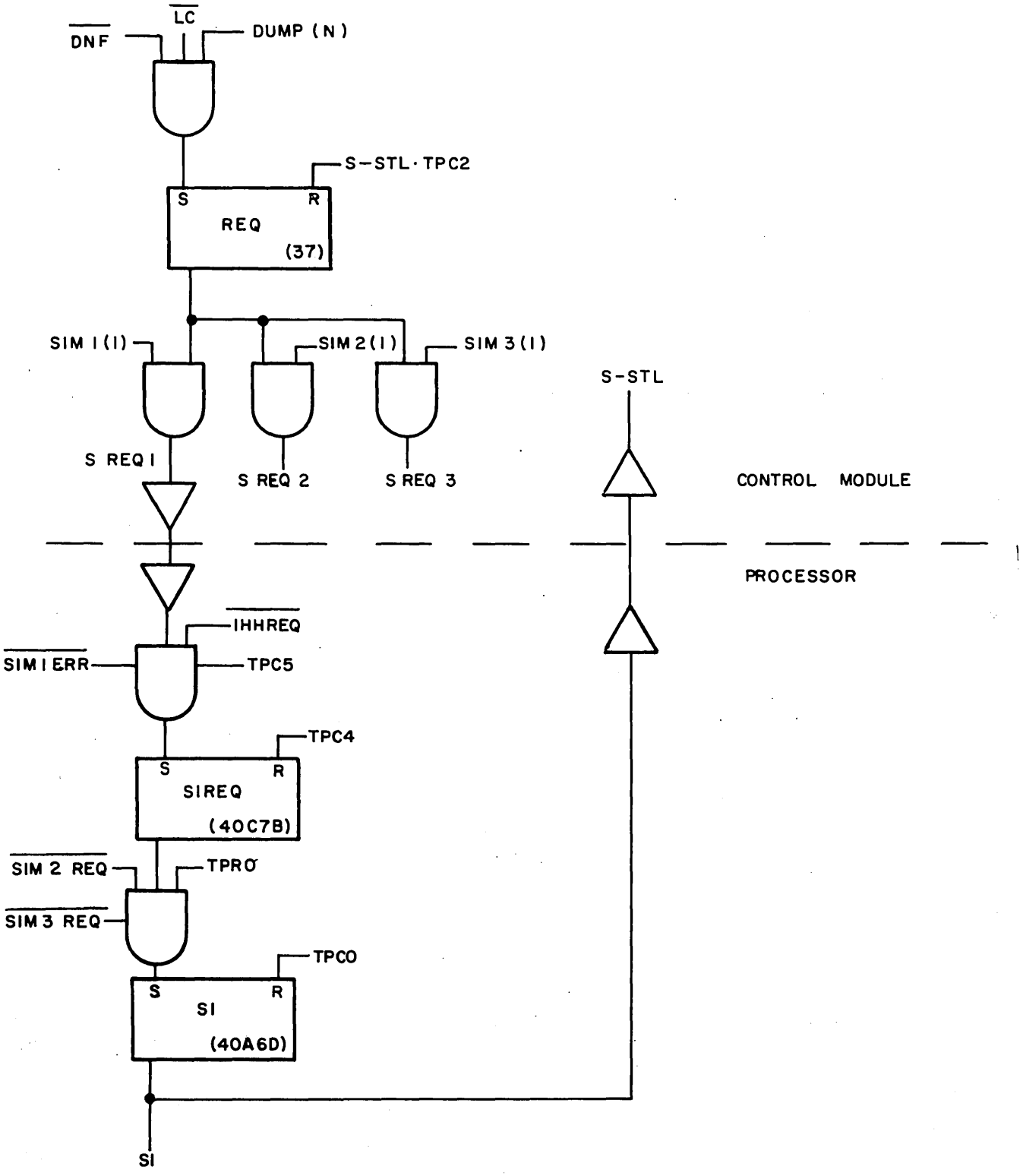


FIGURE 3-4. READ STL REQUEST

the signal S-TERM(P). S-TERM(P) sends either the SCOM or SRA return to the processor depending upon the SRA flip flop (Print 44). The return will be for SIMO-1, SIMO-2 or SIMO-3 depending upon the mode flip flops in the control module.

3.2.2 Read Accuracy

Several checks are made in the control module to insure the accuracy of the data received from the tape station. A check is also made to determine if the tape station is following the commands from the control module.

When the read is from a 582 or 681 tape station a check is made for the guard characters. No information is transferred to the processor until a FGC has been detected. If the FGC and EGC are missing the block is ignored and the read continues until a valid block is actually read in. If the FGC is present and the EGC is not the block is read in and the instruction terminates with SRA set and a RE indicated. Gate 41B6C detects this condition. If the FGC is missing but the EGC is present the block is not read in and the instruction terminates with SRA set with a RE indicated. Gate 41B5D detects this condition due the character counter containing zero's.

When a parity error is detected on the data being read an octal 17 is sent to the processor in place of each character which has improper parity. The instruction terminates upon the detection of a gap with SRA set and a RE indicated. The A17 and B17 flip flops (41B5A & 41B5B) remember that at least one parity error has occurred during the instruction. If AL1 is set the actual character is transferred

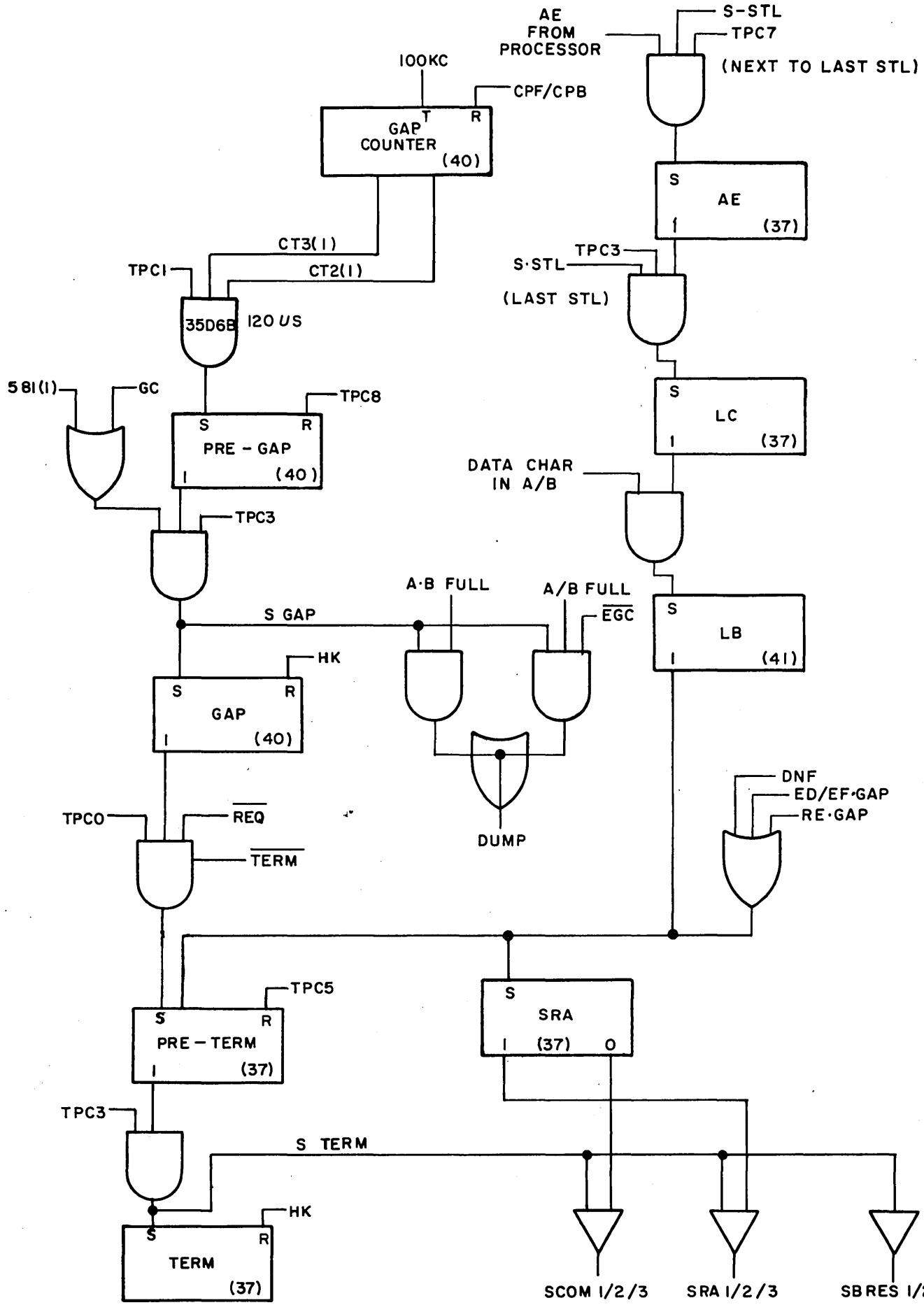


FIGURE 3-5. READ TERMINATION

and the instruction terminates with SRA and RE set.

RE is also set during a read from a 582 or 681 if less than four characters have been read in and a ED/EF has not been found (41B5D). (Including EGC but not FGC).

The ME1 (miscellaneous error 1) flip flop is used only with a 581 tape station to indicate a MCP (41B8B) or less than three characters being read (41B8C).

An error condition allows the SRA flip flop (37B2D) to be set which prevents a SCOM return and sends the SRA return to the processor:

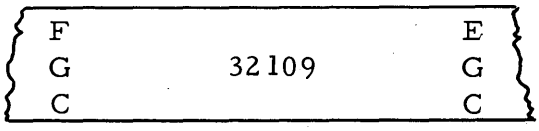
The detection of an ED or EF (55_8 or 56_8) sets the ED/EF indicator (41B2A) along with the SRA flip flop. The 501 system ED/EF (72_8 or 73_8) also set the ED/EF indicator.

READ EXAMPLE

Instruction: 4 6 0741 0750

Tape on TS # 6 (582/681

Tape



Memory Before Instruction

	40	41	42	43	44	45	46	47	48	49	50
07	A	A	A	A	A	A	A	A	A	A	A

SI01 (A address to S reg in the processor)

TPC1 - Generate HK

TPC2 - Set WRDC

Set IFS

TPC4 - 6 to N register

SI02 (B address to T register in the processor)

TPC2 - Set B-ODD

TPC4 - Set 582

Set CUTS-6

TPC8 - Set SIM-1

TPC5 - After SI02 - Set RUN

1st Character (FGC)

CPF/CPB - Reset GAP counter

RCP2C - Set FGC

CP3 - Set CTC

2nd Character

CPF/CPB - Reset GAP counter

RCPO - Set PMTRW

RCP1 - Advance "one" into CC1

RCP2C - "3" to B Buffer

CP2L - Trigger WRDC to reset state (after CP2L)

3rd Character

CPF/CPB - Reset GAP counter

RCPO - Gate "3" to D buffer - (DUMP)

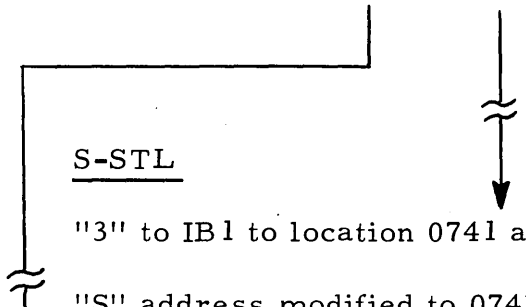
Set REQ (SREQ1 to processor)

RCP1 - Advance "one" to CC2

Reset A&B buffers

RCP2C - "2" to A Buffer

CP2L - Trigger WRDC to set state (after CP2L)



S-STL

"3" to IB1 to location 0741 allow C^0 strobe but not C^1.

"S" address modified to 0742

TPC2 - Reset REQ

TPC5 - Reset C&D buffers (Check for address equality in processor)

4th Character

CPF/CPB - Reset GAP counter

RCP1 - Advance "one" to CC3

RCP2C - "1" to A Buffer

CP2L - Trigger WRDC to reset state

5th Character

CPF/CPB - Reset GAP counter

RCPO - Gate "2" & "1" to C&D buffers

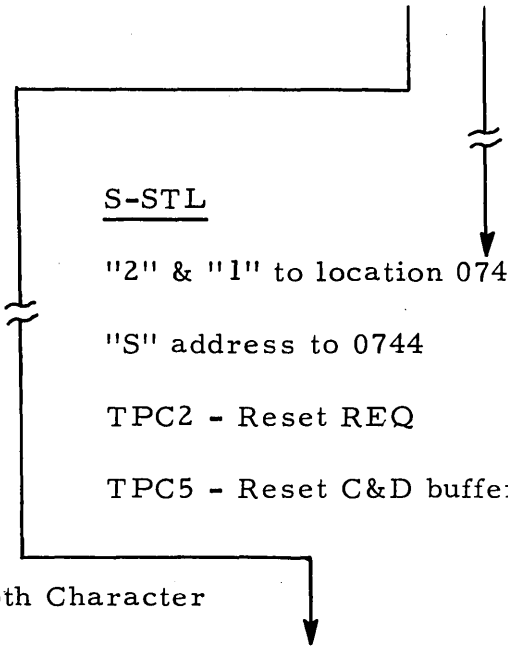
Set REQ (SREQ1 to processor)

RCP1 - Advance "one" to CC4

Reset A & B buffers

RCP2C - "O" to A buffer

CP2L - Trigger WRDC to set state



S-STL

"2" & "1" to location 0742 (inhibit both strobes)

"S" address to 0744

TPC2 - Reset REQ

TPC5 - Reset C&D buffers (Check for Address Equality in Processor)

6th Character

CPF/CPB - Reset GAP counter

RCP1 - Advance CC

RCP2C - "9" to B buffer

CP2L - Trigger WRDC to reset state

7th Character (EGC)

CPF/CPB - Reset GAP counter

RCPO - Gate "O" & "9" to C&D buffers

Set REQ

RCP1 - Reset A&B buffers

RCP2C - EGC (75_8) to A buffer

Set EGC

CP2L - Trigger WRDC to set state

S-STL "O" & "9" to 0744 (inhibit both strobes)

"S" address to 0746

TPC2 - Reset REQ

TPC5 - Reset C&D buffers (Check for Address Equality in Processor)

GAP counter = 12

TPC1 - Set P-GAP

TPC3 - Set GAP

Reset RUN

TPC8 - Reset P-GAP

TPC0 - Set P-TERM

TPC3 - Set TERM

Send SCOM 1 to processor

Send SBRES1 to processor

TPC5 - Reset P-TERM

		40	41	42	43	44	45	46	47	48	49	50
Memory After Instruction	07	A	3	2	1	0	9	A	A	A	A	A

S_f = 0746 T_f = 0750

3.3 Write Operation

The write instructions begin by selecting the desired tape station and sending the run command. The tape is allowed to move and erase for a specified distance before the first character is written. The UTS times for the tape stations and various conditions are as follows.

T.S.	UTS TIME
581	3.6 M sec
582	3.6 M sec
582 & LONG GAP	9.12 M sec
681	6.0 M sec

If the write is following a read to the same tape station the UTS time is increased to 15.36 M sec to insure a proper gap on the tape. This applies to all tape station models. If the tape is at BTC an additional 35 M sec is added to the UTS time in all cases.

While the UTS time is taking place a status level is requested and the first diad to be written is inserted into the A&B buffers. A gate signal "dumps" the A&B buffers into the C&D buffers and another status level is executed to fill the A&B

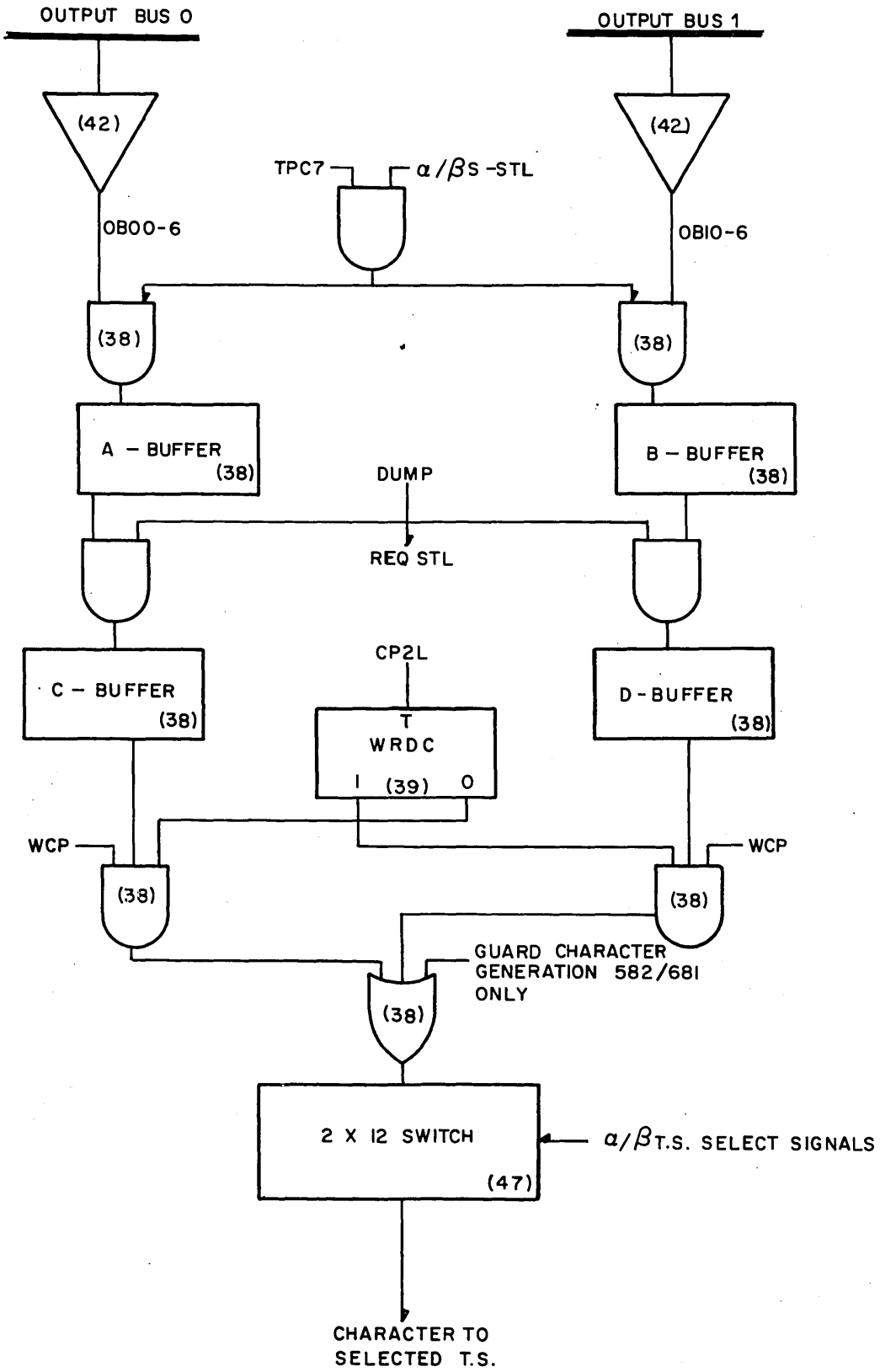


FIGURE 3-6. WRITE DATA FLOW

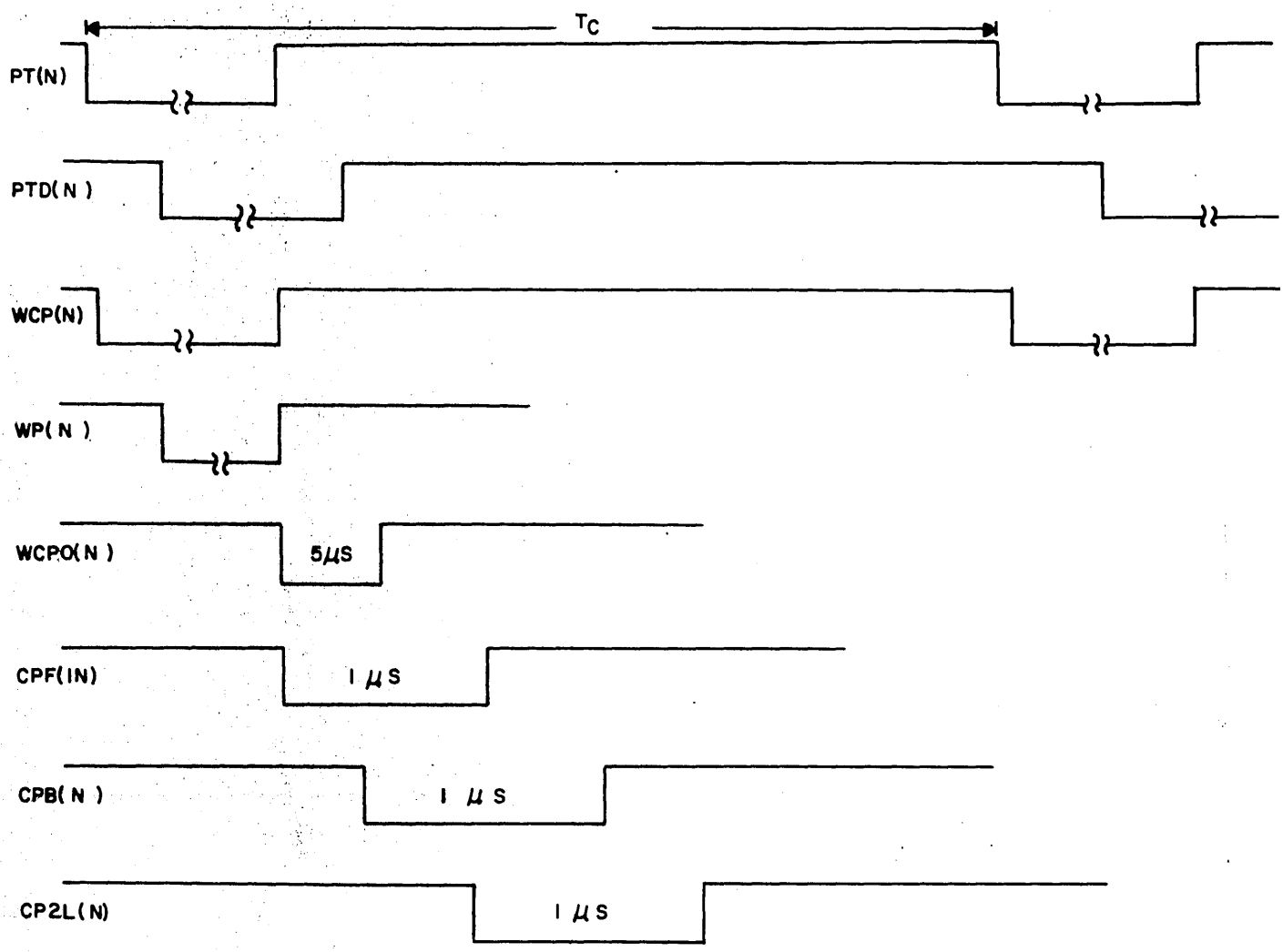
buffers. Both buffers are now full and waiting to be written to the tape when the UTS time has elapsed.

After the UTS Count the FGC is generated and written to the tape in the case of a 582/681 tape station followed by the character from either the C or D buffer. If a 581 tape station is being used the character from either C or D is written to tape without the guard character. The character from the C or D buffer is chosen by the WRDC flip flop which is initially set to the configuration of the $A^3 2^0$ bit during SI01. The WRDC flip flop changes state each time a character is written to gate the contents of the C and D buffers alternately to tape. When the character from the D buffer has been written the A & B buffers are "dumped" to C&D and another status level requested to fill A&B. This cycle continues until terminating conditions are found. After address equality has been found the remaining characters are written out of the buffers and one more status level is performed to bring the last diad to the control module. This is necessary since address equality is detected, during a STL, <u>after</u> the address has been modified by the bus adder. After the last data character has been written the run command is removed from the tape station in the case of a 581 and the instruction terminates. If a 582/681 is being used the EGC is generated and written and the tape continues to move until all characters have been checked by the read after write logic. This is indicated by the change in status of the R/WCHK level from the tape stations.

3.3.1 Write Logic

During SI01 the WRDC flip flop is set to the configuration of the A32^{o} bit to allow the correct first data character to be written. The FGC flip flop is set during SI02 if a 581 is not being used. The RUN command is sent and the counter is triggered every 30 us (40B1A - 33KC). The proper UTS count will eventually be recognized and the UTS flip flop set (40B7B) depending upon the type of tape station selected. If the signal CUTS is present a read has been performed to the tape station prior to the write and UTS will not be set until 15.36 M sec. have passed (40C7D). This insures that a proper gap is made on the tape before writing begins. Setting of the UTS flip flop allows a set of pulses to be generated for each character written to the tape. The frequency of the "sets" of pulses determine the write out rate (figure 3-7). For a 681 tape station the pulse rates are controlled by a 120 KC oscillator (45C3A) or a 100 KC oscillator (45C3B) with the 100 KC return present. A 66 KC oscillator (45C3C) is used for the 582 tape station. The 66 KC oscillator triggers the 33 KC flip flop (40B6B) to provide the write out rate for a 581 tape station. The WCP will gate the character to the tape station and the WP actually clocks the character onto the tape. The remaining pulses are used to control the logic in the control module.

While the UTS count is taking place the processor has executed two status levels to fill the buffers. The REQ flip flop (37B3H) was set during SI02 to request the first status level. The processor grants the STL which extracts the diad from memory and sends it to the control module over output busses 0 & 1. TPC7 of the



	PT	PTD	WCP	WP	T_c
120 KC	4.1 μs	4.1 μs	4.1 μs	3.35 μs	8.2 μs
100 KC	5 μs	5 μs	5 μs	4.25 μs	10 μs
66 KC	7.5 μs	7.5 μs	7.5 μs	6.75 μs	15 μs
33 KC	7.5 μs	7.5 μs	7.5 μs	6.75 μs	15 μs

(30 us between Chars

FIGURE 3-7. WRITE TIMING

status level gates the diad into the A&B buffers (39B3L). FF-1 is set approximately 120 us later to allow TPC8 to "dump" the diad into the C&D buffers (39B8C) and request the second status level to fill the A&B buffers again. The control module remains in this condition until the UTS time has elapsed.

The first WCP is generated and if FGC is set an octal 75 is generated and written to the Tape (582/681 only 38A8A & 38B3D). Only the WCP & WP are generated if FGC is set consequently the buffers and WRDC are not affected. FGC is triggered to the reset state at the end of the WCP. The second WCP gates the first data character to the tape and WRDC is triggered to the opposite state after CP2L has occurred. After the character is gated from the D buffer to tape (WRDC set) the "DUMP" signal is generated (39D7C) to gate the next diad into C&D and request the next status level. This process continues until address equality is detected by the processor which will be in the status level that sends the next to last diad to the control module. The AE flip flop (37B8A) is set in the control module and the LC last character flip flop (37A8B) is set during the last status level. At the WCPO of the last character to be written, as determined by the B-ODD flip flop, the UTS flip flop is reset if a 581 is being used (40C6B) or the EGC flip flop is set if a 581 is not being used (41C3E). In the latter case one more WCP is generated to write a octal 76 to the tape and then the UTS flip flop is reset (40C7H). UTS being reset prevents write timing pulse generation and if 581 is being used the P-TERM flip flop is set (35D5B). TERM is set and RUN is reset to send the SCOM or SRA return sent to the processor to end the instruction. P-TERM is not set for a 582/

681 until the END CHK (37A7B) flip flop is triggered to the set state by the signal R/WCHK from the tape station changing polarity indicating all characters have been read and checked. This time will be approximately 2 M sec for 582 or 1.4 M sec for a 681 from the time the last character was written.

3.3.2 Write Accuracy Control

The characters written to a 581 tape station are checked for parity in the tape station and if the character is correct the WR VER pulse is returned to the control module. The pulse is normally returned within 6.5 u sec after the character is written on tape by the WP. If the WR VER pulse is not returned within 14.25 u sec after the WP the MEI flip flop is set (41B7B) to indicate a write error. The LC flip flop is set (37B8B) at the next WCPO to terminate the instruction with SRA set.

A read after write parity error during a write to a 582/681 will set the R/WE flip flop (41A4A) due to the signal R-WPE/WVER being transmitted from the tape station to the control module as a negative signal. The LC flip flop is set at the next WCPO. The EGC is written to the tape and the instruction terminates with SRA set after the guard character has passed over the read head of the tape station. This is signified by the triggering of the END CHK flip flop due to the change in status of the R/WCHK return from the tape station.

3.4 Erase Operation

The erase instructions perform in the same manner as the write instructions with the exception that no characters are actually written on the tape. The ER flip flop

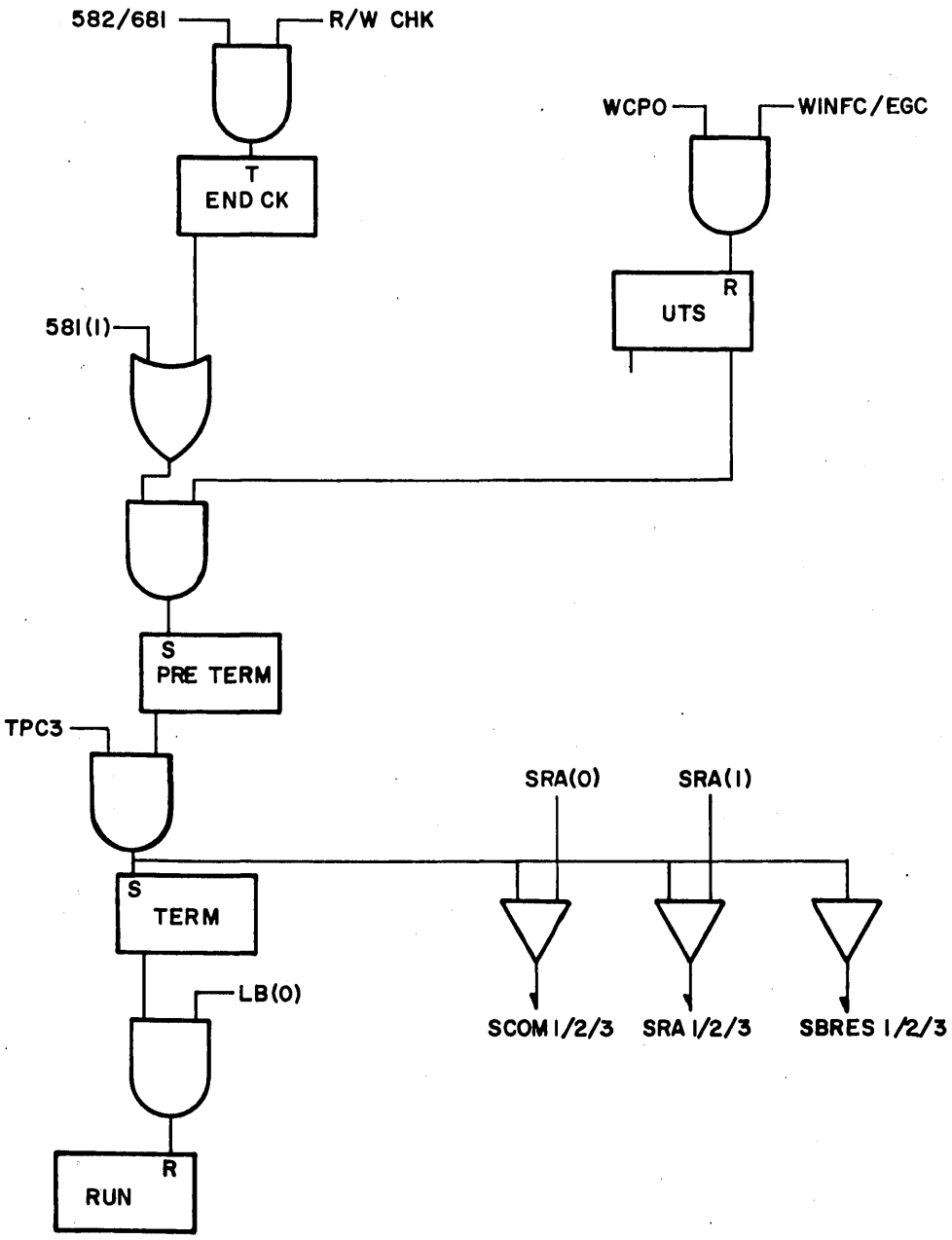


FIGURE 3-8. WRITE TERMINATION

(37B4F) is set during SI02 along with the WR flip flop. The UTS count is recognized but the WP is not generated due to ER being set (40A7A) consequently the characters are not written on the tape. The instruction continues until AE is detected and the instruction terminates immediately. No accuracy checks are performed during the ERASE other than the DNF check.

If a "splice" is detected during the erase the instruction terminates with a SRA condition. If the "splice" condition exists before the erase instruction is performed it is ignored (37D3C).

3.5 Rewind Operation

The IOC instruction provides 3 options in regard to the tape station depending upon the 2^0 2^1 & 2^2 bits of the B address. If only 2^0 is present a rewind to BTC is performed, a 2^1 bit instructs a 681 to rewind to the load point and a 2^2 bit rewinds one gap. The condition of the bits are stored in the control module by the B-ODD, B31 and B32 flip flops. If a rewind to BTC is specified the control module sends a 330 us rewind pulse to the selected tape station. After 320 u sec a check is made to insure the tape station is either running in reverse or is at BTL. If not the instruction terminates at the end of the rewind pulse with a SRA & DNF indication. A rewind to load point with a 681 station selected will send a 960 u sec rewind pulse. The station logic recognizes the longer length of the command and initiates a rewind to load point. The DNF check is made and the instruction terminates. The tape station continues to rewind off-line in both situations.

In the case of a rewind one gap the RUN & REVERSE commands are given and the instruction terminates when a 2 M sec gap has been detected.

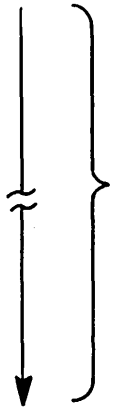
3.5.1 Rewind Logic

The condition of B-ODD, B31, B32, and RWD flip-flops are determined during SIO2. The rewind command is started at this point. The counter (Print 40) is triggered every 10 us by the 100 KC oscillator (40B2A). A count of 330 usec is recognized (37D6D) unless a rewind to load point is specified (B31 (1) & 681 (1) in which case a 960 us count is recognized by 37D5D. Recognition of the proper count sets P-TERM and then TERM. Setting of P-TERM checks for a DNF (41C6D). Setting of TERM resets the RWD flip-flop and ends the rewind command. The instruction terminates with either the SRA or SCOM return to the processor, depending upon the DNF and SRA flip-flops.

If B32 is set during SIO2, indicating a rewind "one" gap, the RUN & REV flip-flops are set to run the tape in reverse. The tape continues to run until a 2 M sec gap is recognized by gate 40C5B to set the GAP flip-flop. The longer gap is necessary to insure that all information is to the right of the write head when the tape stops due to the spacing of the read and write heads on the 582/681 sation. The instruction terminates by setting P-TERM and TERM in the normal sequence. No accuracy checks are performed other than the DNF check.

IOC · SI02 · $\overline{B32}$

SET RWD



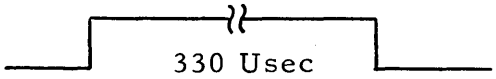
960 us if 681 · B31

330 us if $\overline{681 \cdot B31}$

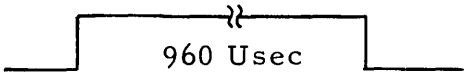
SET P TERM & CHECK DNF
SET TERM
RESET RWD

RWD COMMANDS

$\overline{681 \cdot B31}$



681 · B31



TPC1 - Set TPC13

if $\overline{\alpha \text{ BUSY}}$ generate α HK

if $\overline{\beta \text{ BUSY}}$ generate β HK

TPC2 - if $\overline{\alpha \text{ BUSY}}$ · α TI · OB10 - set α WRDC

if $\overline{\beta \text{ BUSY}}$ · β TI · OB10 - set β WRDC

if $\overline{\alpha \text{ BUSY}}$ · α TI · (RR · $\overline{\text{OB10}}$) / ($\overline{\text{RR}}$ · OB10) - set α IFS

if $\overline{\beta \text{ BUSY}}$ · β TI · (RR · $\overline{\text{OB10}}$) / ($\overline{\text{RR}}$ · OB10) - set β IFS

TPC3

TPC4 - Set TPC47

Reset TPC13

if $\overline{\alpha \text{ BUSY}}$ - N to α N REG

if $\overline{\beta \text{ BUSY}}$ - N to β N REG

TPC8 - Reset TPC47

(SI02 LEVEL)

if α TI · $\overline{\beta \text{ ADC}}$ · $\overline{\alpha \text{ BUSY}}$ · $\overline{\alpha \text{ REV RUN RET}}$ · α TOP set ONB

if β TI · $\overline{\alpha \text{ ADC}}$ · $\overline{\beta \text{ BUSY}}$ · $\overline{\beta \text{ REV RUN RET}}$ · β TOP set ONB

if $\overline{\text{IOS}}$ · [SOP3 · SB3] inhibit setting ONB

if SOP2 · SB2 inhibit setting ONB

if $\overline{\text{SOP2}}$ · SB1 · $\overline{\text{SOP3}}$ inhibit setting ONB

TPC1 - Set TPC13

TPC2 - if α TI · $\overline{\alpha \text{ BUSY}}$ · OB10 - set α B-ODD

if β TI · $\overline{\beta \text{ BUSY}}$ · OB10 - set β B-ODD

if α TI · $\overline{\alpha \text{ BUSY}}$ · IOC · OB11 - set α B31

if β TI · $\overline{\beta \text{ BUSY}}$ · IOC · OB11 - set β B31

if α TI · $\overline{\alpha \text{ BUSY}}$ · IOC · OB12 - set α B32 and α REV

if β TI · $\overline{\beta \text{ BUSY}}$ · IOC · OB12 - set β B32 and β REV

TPC4 - Reset TPC13

Set TPC47

if $\overline{\alpha \text{ BUSY}}$ · ONB(1) · α TI - GENERATE α set OP

if $\overline{\beta \text{ BUSY}}$ · ONB(1) · β TI - GENERATE β set OP

if α SETOP · RR - set α REV

if β SETOP · RR - set β REV

if α SETOP · ER - set α ER and α WR

if β SETOP · ER - set β ER and β WR

if α SETOP · WR - set α WR and α REQ

if β SETOP · WR - set β WR and β REQ

if α SETOP · $\overline{(R/WPE) / WR\ VER}$ - set α 581 and α PMT RW

if β SETOP · $\overline{(R/WPE) / WR\ VER}$ - set β 581 and β PMT RW

if α SETOP · $\overline{R/W\ CHK}$ · (R/WPE)/WR VER - set α 582

if β SETOP · $\overline{R/W\ CHK}$ · (R/WPE)/WR VER - set β 582

if α SETOP · R/W CHK · (R/WPE)/WR VER - set α 681

if β SETOP · R/W CHK · (R/WPE)/WR VER - set β 681

if α SETOP · IOC · α B32(0) - set α RWD

if β SETOP · IOC · β B32(0) - set β RWD

if (α SETOP / β SET OP) · (RR/RF) - set CUTS according to TS select signal.

ᵖC7 - if α WR(1) · α 581(0) - set α FGC

if β WR(1) · β 581(0) - set β FGC

if α SET OP · AE - set α AE

if β SET OP · AE - set β AE

ᵖC8 - Reset TPC47

if α TI · ONB(1) · $\overline{SOP3}$ set SIM1

if α TI · ONB(1) · SOP3 set α SIM3

if β TI · ONB(1) · $\overline{SOP3}$ set SIM2

if β TI · ONB(1) · SOP3 set β SIM3

3383 Source and Abbreviation List

Signal Abbr.	Description	Source
AA-1N	Character in "A" Buffer	38D5C
AA-0N	Character in "A" Buffer	38D5C
AB Full-N	"A" and "B" Buffers full	39C8B
A/B Full-N	"A" or "B" Buffers full	39C7A
AE-1N	Address Equality	37B8A
AE-0N	Address Equality	37B8A
AE-N	Address Equality	36C5A
ALI-P	Alarm Inhibit	36D4E
ALR-P	Alarm Reset	36D3A
ALR-PA	Alarm Reset	36D3B
ANY BIT-P	Any Bit Present	39D3F
A-17-P	Load octal 17 into "A" Buffer	38D5C
A30-0N	A_3 character 2^0 bit	42A7B
A30-1N	A_3 character 2^0 bit	42A7B
A31-0N	A_3 character 2^1 bit	42A7A
A31-1N	A_3 character 2^1 bit	42A7A
A32-0N	A_3 character 2^2 bit	42A8A
A32-1N	A_3 character 2^2 bit	42A8A

Signal Abbr.	Description	Source
ALPHA ADC-N	Alpha Address Compare	45D2C
ALPHA ADC-P	Alpha Address Compare	45C2A
ALPHA BODD-1N	Alpha B Address is odd	42A5A
ALPHA BODD-0N	Alpha B Address is odd	
ALPHA BUSY-N	Alpha Mode Busy	35C5H
ALPHA BUSY-P	Alpha Mode Busy	35B5A
ALPHA B31-1N	Alpha B_3 character 2^1 bit	42A6A
ALPHA B31-0N	Alpha B_3 character 2^1 bit	42A6A
ALPHA B32-1N	Alpha B_3 character 2^2 bit	42A6B
ALPHA B32-0N	Alpha B_3 character 2^2 bit	42A6B
ALPHA CUTS-P	Alpha Control up to Speed	49A3B
ALPHA DS-N	Alpha Device Sense	35A6A
ALPHA EDEF-N	Alpha ED or EF	44B2A
ALPHA HK/ALR-P	Alpha Housekeeping or Alarm Reset	35A5C
ALPHA HK1-P	Alpha Housekeeping	42B4C
ALPHA HK/GR-P	Alpha Housekeeping or General Reset	35A5D
ALPHA HK/GR-N	Alpha Housekeeping or General Reset	35A5B
ALPHA HK/GR-PC	Alpha Housekeeping or General Reset	45D4B

Signal Abbr.	Description	Source
ALPHA IFS	Alpha Inhibit First Strobe	42A4A
ALPHA N0-1N	Alpha "N" Register	45C4A
ALPHA N0-0N	Alpha "N" Register	45C4A
ALPHA N1-1N	Alpha "N" Register	45C4A
ALPHA N1-0N	Alpha "N" Register	45C5A
ALPHA N2-1N	Alpha "N" Register	45C6A
ALPHA N2-0N	Alpha "N" Register	45C6A
ALPHA N3-1N	Alpha "N" Register	45C7A
ALPHA N3-0N	Alpha "N" Register	45C7A
ALPHA S-P	Alpha "S" Status Level	36A8D
ALPHA S-N	Alpha "S" Status Level	36A7D
ALPHA SCB-N	Load Strobe Control Bits of A and B Addresses	42C6C
ALPHA SET0P-P	Alpha Set Operation Codes	35C6B
ALPHA SIM0.3-1N	Alpha Simo 3 Mode	35C5F
ALPHA SIM03-0N	Alpha Simo 3 Mode	35C5F
ALPHA T1-N	Alpha Tape Instruction	35A7D
ALPHA T1-P	Alpha Tape Instruction	35A7B
ALPHA SWITCH OUTPUT-P	Alpha Switch Output	48C3E
ALPHA SWITCH INVERTED OUTPUT	Alpha Switch Inverted Output	48B3A

Signal Abbr.	Description	Source
ALPHA 1-NA	Alpha Tape Station Trunk Number	45A8A
ALPHA 1-NB	Alpha Tape Station Trunk Number	45A8A
ALPHA 2-NA	Alpha Tape Station Trunk Number	45A8C
ALPHA 2-NB	Alpha Tape Station Trunk Number	45A7A
ALPHA 3-NA	Alpha Tape Station Trunk Number	45A7B
ALPHA 3-NB	Alpha Tape Station Trunk Number	45A7C
ALPHA 4-NA	Alpha Tape Station Trunk Number	45A6A
ALPHA 4-NB	Alpha Tape Station Trunk Number	45A6B
ALPHA 5-NA	Alpha Tape Station Trunk Number	45A6C
ALPHA 5-NB	Alpha Tape Station Trunk Number	45A6D
ALPHA 6-NA	Alpha Tape Station Trunk Number	45A5A
ALPHA 6-NB	Alpha Tape Station Trunk Number	45A5B
ALPHA 7-NA	Alpha Tape Station Trunk Number	45A5C
ALPHA 7-NB	Alpha Tape Station Trunk Number	45A4A
ALPHA 8-NA	Alpha Tape Station Trunk Number	45A4B
ALPHA 8-NB	Alpha Tape Station Trunk Number	45A4C
ALPHA 9-NA	Alpha Tape Station Trunk Number	45A3A
ALPHA 9-NB	Alpha Tape Station Trunk Number	45A3B
ALPHA 10-NA	Alpha Tape Station Trunk Number	45A3C
ALPHA 10-NB	Alpha Tape Station Trunk Number	45A3D

Signal Abbr.	Description	Source
ALPHA 11-NA	Alpha Tape Station Trunk Number	45A2A
ALPHA 11-NB	Alpha Tape Station Trunk Number	45A2B
ALPHA 12-NA	Alpha Tape Station Trunk Number	45A2C
ALPHA 12-NB	Alpha Tape Station Trunk Number	45A1A
	"B"	
BB-1N	Character in "B" Buffer	38C1A
BB-0N	Character in "B" Buffer	38C1A
BTL RET-P	BTL Return	48B3A
B ODD-1N	B Address is odd	42A2A
B ODD-0N	B Address is odd	42A2A
B17-P	Load Octal 17 into "B" Buffer	38D1A
B31-1N	B_3 character 2^1 bit	42A3A
B31-0N	B_3 character 2^1 bit	42A3A
B32-1N	B_3 character 2^2 bit	42A3B
B32-0N	B_3 character 2^2 bit	42A3B
BETA ADC-P	Beta Address Compare	46C2A
BETA BUSY-P	Beta Mode Busy	35B4A
BETA BUSY-N	Beta Mode Busy	35C4F
BETA CUTS-P	Beta Control Up To Speed	49A3A
BETA DS-N	Beta Device Sense	35A6B
BETA EDEF-N	Beta ED or EF	44B3A

Signal Abbr.	Description	Source
BETA HK/ALR-P	Beta Housekeeping or Alarm Reset	35A4D
BETA HK1-P	Beta Housekeeping	42B1A
BETA HK/GR-P	Beta Housekeeping or General Reset	35A4E
BETA HK/GR-N	Beta Housekeeping or General Reset	35A4B
BETA HK/GR-PC	Beta Housekeeping or General Reset	46D4B
BETA IFS	Beta Inhibit First Strobe	42A2B
BETA INVERTED OUTPUT	Beta Inverted Output	48B3B
BETA N0-0N	Beta "N" Register	46C4A
BETA N0-1N	Beta "N" Register	46C5A
BETA N1-0N	Beta "N" Register	46C5A
BETA N1-1N	Beta "N" Register	46C6A
BETA N2-0N	Beta "N" Register	46C6A
BETA N2-1N	Beta "N" Register	46C6A
BETA N3-0N	Beta "N" Register	46C7A
BETA N3-1N	Beta "N" Register	46C7A
BETA S-P	Beta "S" Status level	36A8C
BETA S-N	Beta "S" Status level	36A8E
BETA SCB-N	Load Strobe Control Bits of A and B Addresses	42C4D
BETA SET0P-P	Beta Set Operation Codes	35C6E
BETA SIM03-1N	Beta Simo 3 Mode	35C3E

Signal Abbr.	Description	Source
BETA SIM03-0N	Beta Simo 3 Mode	35C3E
BETA SWITCH OUTPUT	Beta Switch Output	48C3F
BETA TI-P	Beta Tape Instruction	35A7A
BETA TI-N	Beta Tape Instruction	35A7C
BETA 1-NA	Beta Tape Station Trunk Number	46A8A
BETA 1-NB	Beta Tape Station Trunk Number	46A8A
BETA 2-NA	Beta Tape Station Trunk Number	46A8A
BETA 2-NB	Beta Tape Station Trunk Number	46A8A
BETA 3-NA	Beta Tape Station Trunk Number	46A8A
BETA 3-NB	Beta Tape Station Trunk Number	46A8A
BETA 4-NA	Beta Tape Station Trunk Number	46A8A
BETA 4-NB	Beta Tape Station Trunk Number	46A8A
BETA 5-NA	Beta Tape Station Trunk Number	46A8A
BETA 5-NB	Beta Tape Station Trunk Number	46A8A
BETA 6-NA	Beta Tape Station Trunk Number	46A8A
BETA 6-NB	Beta Tape Station Trunk Number	46A8A
BETA 7-NA	Beta Tape Station Trunk Number	46A8A
BETA 7-NB	Beta Tape Station Trunk Number	46A8A
BETA 8-NA	Beta Tape Station Trunk Number	46A8A
BETA 8-NB	Beta Tape Station Trunk Number	46A8A

Signal Abbr.	Description	Source
BETA 9-NA	Beta Tape Station Trunk Number	46A8A
BETA 9-NB	Beta Tape Station Trunk Number	46A8A
BETA 10-NA	Beta Tape Station Trunk Number	46A8A
BETA 10-NB	Beta Tape Station Trunk Number	46A8A
BETA 11-NA	Beta Tape Station Trunk Number	46A8A
BETA 11-NB	Beta Tape Station Trunk Number	46A8A
BETA 12-NA	Beta Tape Station Trunk Number	46A8A
BETA 12-NB	Beta Tape Station Trunk Number	46A8A
	"C"	
CC2-1N-0N	Character Counter	41C8B
CC3-0N	Character Counter	41C7A
CC4-0N	Character Counter	41C7B
COMPATIBLE	Compatable	48(Table)
CPB-N	Clock Pulse B	39C3A
CPB-P	Clock Pulse B	39C3C
CPF-1N	Character Present Flip-flop	39C3B
CPF-0N	Character Present Flip-flop	39C3B
CP2L-N	Clock Pulse 2L	39B3E
CP2L-P	Clock Pulse 2L	39B2D
CP3-P	Clock Pulse 3	39B3J
CTC EDF1-P	Conditional transfer of control (ED or EF)	44A5B

Signal Abbr.	Description	Source
CTC EDF-2P	Conditional Transfer of Control (ED or EF)	44A5B
CTC-1N	Counter Control	40C2C
CTC-0N	Counter Control	40C2C
CT0-1N	Counter	40B2N
CT1-1N	Counter	40B2N
CT2-1N	Counter	40B2N
CT3-1N	Counter	40B2N
CT4-1N	Counter	40B2N
CT5-1N	Counter	40B2N
CT5-0P	Counter	40B2N
CT6-1N	Counter	40B2N
CT7-1N	Counter	40B2N
CT8-1N	Counter	40B2N
CT9-1N	Counter	40B6C
CT0-1N	Counter	38B5A
C1-1N	"C" Buffer Outputs	38B5A
C2-1N	"C" Buffer Outputs	38B5A
C3-1N	"C" Buffer Outputs	38B5A
C4-1N	"C" Buffer Outputs	38B5A
C5-1N	"C" Buffer Outputs	38B5A
C6-1N	"C" Buffer Outputs	38B8C

Signal Abbr.	Description	Source
	"D"	
DNF-0N	Device does not follow	41B6A
DNF-P	Device does not follow	44A8B
DPE-P	Data Parity Error	41C5C
DUMP-N	Dump "A" and "B" Buffers to "C" and "D" Buffers	39A7B
D0-1N	"D" Register	38B2B
D1-1N	"D" Register	38B2B
D2-1N	"D" Register	38B2B
D3-1N	"D" Register	38B2B
D4-1N	"D" Register	38B2B
D5-1N	"D" Register	38B2B
D6-1N	"D" Register	38B4A
	"E"	
EDEF-0N	ED or EF Flip-flop	41B2A
EDEF-P	ED or EF Level	41B2B
EGC-1N	End Guard Character	41B3A
EGC-0N	End Guard Character	41B3A
END CHK-1N	End Check Flip-flop	37A7B
END CHK-0N	End Check flip-flop	47A7B

Signal Abbr.	Description	Source
ER-N	Erase Command	36C7B
ERl/ALR 3-P	Error Indicators or Alarm Reset	35A8D
ERl/ALR 2-P	Error Indicators or Alarm Reset	35A8E
ERl/ALR 1-P	Error Indicators or Alarm Reset	35A8F
ETW RET	End Tape Warning Return	48
FFl-lN	First Fill Flip-flop one	39C5A
FF2-0N	First Fill Flip-flop two	39A5B
FGC-lN	First Guard Character	41B4A
FGC-0N	First Guard Character	41B4A
	"G"	
GAP-lN	Gap	40C5E
GAP-0N	Gap	40C5E
GC-N	Guard Character	41B5B
GC-P	Guard Character	41A3A
GR-PA	General Reset	36D5B
GR-PB	General Reset	36D4A
	"I"	
IB 00-P	Input Bus	43B1B
IB 01-P	Input Bus	43B1B
IB 02-P	Input Bus	43B1B

Signal Abbr.	Description	Source
IB 03-P	Input Bus	43B1B
IB 04-P	Input Bus	43B1B
IB 05-P	Input Bus	43B1B
IB 06-P	Input Bus	43B1B
IB 10-P	Input Bus	43B1B
IB 11-P	Input Bus	43B1B
IB 12-P	Input Bus	43B1B
IB 13-P	Input Bus	43B1B
IB 14-P	Input Bus	43B1B
IB 15-P	Input Bus	43B1B
IB 16-P	Input Bus	43B8C
INHST-P	Inhibit Start	37C7A
IOC-N	Input Output Control Instruction	36C6A
IOS-N	Input Output Sense Instruction	36C7A
IOS-P	Input Output Sense Instruction	36C7A
ISA-P	Inhibit STROBE A	37C4D
ISB-P	Inhibit STROBE B	37C4E
	"L"	
LB-1N	Long Block	41B1A
LB-0N	Long Block	41B1A
LB1-1N	Long Block Simo 1	44B2H

Signal Abbr.	Description	Source
LB2-1N	Long Block Simo 2	44B3H
LB3-1N	Long Block Simo 3	44C3B
LC-1N	Last Character	37A8B
LC-0N	Last Character	37A8B
	"M"	
MCP-1N	Missing Clock Pulse	41B8A
MCP-0N	Missing Clock Pulse	41B8A
ME1-1N	Miscellaneous Error 1	41A7A
ME1-P	Miscellaneous Error 1	44A8C
ME2-P	Miscellaneous Error 2	44A6C
MTA1-1N	Magnetic Tape Alarm 1	44B2E
MTA2-1N	Magnetic Tape Alarm 2	44B4E
MTA3-1N	Magnetic Tape Alarm 3	44C4A
	"N"	
NO SPLICE	No Splice	48 (Table)
N0-N	"N" Character From Processor	36D5A
N0-P	"N" Character From Processor	36D5C
N1-N	"N" Character From Processor	36D6D
N1-P	"N" Character From Processor	36D6B
N2-N	"N" Character From Processor	36D6A
N2-P	"N" Character From Processor	36D6C

Signal Abbr.	Description	Source
N3-N	"N" Character From Processor	36D7B
N3-P	"N" Character From Processor	35D6D
N4-N	"N" Character From Processor	36D7A
N5-P	"N" Character From Processor	36D8B
	"O"	
OB 00-N	Output Bus	42D2B
OB 01-N	Output Bus	42D2B
OB 02-N	Output Bus	42D2B
OB 03-N	Output Bus	42D2B
OB 04-N	Output Bus	42D2B
OB 05-N	Output Bus	42D2B
OB 06-N	Output Bus	42D2B
OB 10-N	Output Bus	42D2B
OB 10-P	Output Bus	42D2B
OB 11-N	Output Bus	42D2B
OB 12-N	Output Bus	42D2B
OB 13-N	Output Bus	42D2B
OB 14-N	Output Bus	42D2B
OB 15-N	Output Bus	42D2B
OB 16-N	Output Bus	42D8A
ONB-1N	Operable and Not Busy	35A3A
ONB-P	Operable and Not Busy	35A3C

Signal Abbr.	Description	Source
	"P"	
P-GAP	Pre-Gap	40D5A
P-TERM-1N	Pre-Termination	37B6B
P-TERM-0N	Pre-Termination	37B6B
PE1-1N	Parity Error Simo 1	44B1A
PE2-1N	Parity Error Simo 2	44B3J
PE3-1N	Parity Error Simo 3	44C2A
PMT RW-1N	Permit Read or Write	39A5C
PMT RW-0N	Permit Read or Write	39A5C
PT-P	Pulse Timer	40D4A
PT-N	Pulse Timer	40C3B
PTD-N	Pulse Timer Delayed	40B3A
	"R"	
RCP	Read Clock Pulse	48
RCP0-N	Read Clock Pulse 0	39B3B
RCP1-P	Read Clock Pulse 1	39B3B
RCP1-N	Read Clock Pulse 1	39B3F
RCP2-N	Read Clock Pulse 2	39B2C
RD-1N	Read	37B4F
RD-0N	Read	37B4F
RD-N	Read	47A4C
RDA-N	Load "A" Buffer During Read	39A4B
RDB-N	Load "B" Buffer During Read	39A3A

Signal Abbr.	Description	Source
RE-1N	Read Error	41A5A
RE-0N	Read Error	41A5A
RE-P	Read Error	41A4A
RE-P	Read Error	44A7D
RECHK-P	Read Error Check	37B3B
RESAB-P	Reset "A" and "B" Buffers	39A6A
RESCD-P	Reset "C" and "D" Buffers	39A4A
REV-1N	Reverse	37B4E
REV-0N	Reverse	37B4E
REV-N	Reverse	37A4A
REV RETURN	Reverse Return	48
REV RUN RET-P	Reverse Run Return	41C6A
RF-P	Read Forward	36C8D
RF/RR-N	Read Forward or Read Reverse	36B8A
RR-N	Read Reverse	36C8A
RR-P	Read Reverse	36C8C
RUN-1N	Run	37B6A
RUN-0N	Run	37B6A
RUN-N	Run	37B6E
RUN-RET	Run Return	48
RWD-1N	Rewind	37B5F
RWD-0N	Rewind	37B5F
R/WCK	Read After Write Check	48
R/WE-1N	Read After Write Error	41A4A

Signal Abbr.	Description	Source
R/WPE/WVER-P	Read After Write Parity Error or Write Verify	48
R0-P	Read Data From Tape Stations	48
R1-P	Read Data From Tape Stations	48
R2-P	Read Data From Tape Stations	48
R3-P	Read Data From Tape Stations	48
R4-P	Read Data From Tape Stations	48
R5-P	Read Data From Tape Stations	48
R6-P	Read Data From Tape Stations	48

"S"

S-NA	"S" Status Level	37C8D
SB1-N	Simo Busy 1	36C4A
SB2-N	Simo Busy 2	36C4B
SB3-N	Simo Busy 3	36C5B
SBRES1-P	Simo Busy Reset 1	44B6B
SBRES2-P	Simo Busy Reset 2	44B7A
SBRES3-P	Simo Busy Reset 3	44C5A
SCOM1-P	Simo Complete 1	44B6A
SCOM2-P	Simo Complete 2	44B8B
SCOM3-P	Simo Complete 3	44C4B
SEDF1-1N	Sense EDEF Simo 1	44B2F
SEDF2-1N	Sense EDEF Simo 2	44B3F
SEDF3-1N	Sense EDEF Simo 3	44C3A

Signal Abbr.	Description	Source
SET OP-N	Set Operation Code	37C5C
SET SIMO1-P	Set Simo 1 Flip-flop	35C5B
SET SIMO2-P	Set Simo 2 Flip-flop	35C4C
SET SIMO3-P	Set Simo 3 Flip-flop	35C5D
SET SIMO3-P	Set Simo 3 Flip-flop	35C3B
SGAP-N	Set Gap Flip-flop	40B6A
SIMO1-1N	Simo Mode 1	35C5E
SIMO1-0N	Simo Mode 1	35C5E
SIMO2-1N	Simo Mode 2	35C4E
SIMO3-0N	Simo Mode 3	35C4E
SIO-N	Start Input Output Status Levels	35C7A
SIO1-N	Start Input Output Status Level 1	36C2B
SIO1-P	Start Input Output Status Level 1	36C2D
SIO2-N	Start Input Output Status Level 2	36C2A
SIO2-P	Start Input Output Status Level 2	36C2C
SOP2-N	Simo Op Code 2 (2^0 bit of NOR Register Set)	36C3D
SOP2-P	Simo Op Code 2 (2^0 bit of NOR Register Set)	36C3B
SOP3-N	Simo Op Code 3 (2^4 bit of NOR Register Set)	36C3C
SOP3-P	Simo Op Code 3 (2^4 bit of NOR Register Set)	36C3A
SP-TERM-P	Set Pre-Terminate Flip-flop	37B1A
SRA-1N	Simo Requires Attention	37B2D

Signal Abbr.	Description	Source
SRA-0N	Simo Requires Attention	37B2D
SRA1-P	Simo Requires Attention Mode 1	44B7C
SRA2-P	Simo Requires Attention Mode 2	44B8A
SRA3-P	Simo Requires Attention Mode 3	44C6C
SREQ1-P	Simo Request Mode 1	44B6C
SREQ2-P	Simo Request Mode 2	44B7B
SREQ3-P	Simo Request Mode 3	44C7C
STERM-P	Set Terminate	37B6D
STERM-N	Set Terminate	37C6A
STROBE A-P	STROBE A	44C8A
STROBE B-P	STROBE B	44C7A

"T"

TERM-1N	Terminate	37B6F
TERM-0N	Terminate	37B6F
TI-N	Tape Instruction	35B7C
TNC-P	Tape "N" Count	35C7B
TNCD-0N	Tape "N" Count Delayed	42C4C
TPCO-ST-P	TPCO and Stop	36A1A
TPC0-N	Processor Timing Pulses	36B2A
TPC1-N	Processor Timing Pulses	36B3B
TPC1-P	Processor Timing Pulses	36A3A
TPC13-1N	Processor Timing Pulses	36D2B

Signal Abbr.	Description	Source
TPC2-N	Processor Timing Pulses	36B4C
TPC3-N	Processor Timing Pulses	36B4A
TPC3-P	Processor Timing Pulses	36A4A
TPC4-N	Processor Timing Pulses	36B5A
TPC4-P	Processor Timing Pulses	36A5A
TPC47-1N	Processor Timing Pulses	36D2A
TPC5-N	Processor Timing Pulses	36B6B
TPC5-P	Processor Timing Pulses	36A6A
TPC6	Processor Timing Pulses	
TPC7-N	Processor Timing Pulses	36B6A
TPC8-N	Processor Timing Pulses	36B7B
TPC8-P	Processor Timing Pulses	36A7C
TRICT-P	Trigger Counter	40B2D
	"U"	
UTS-P	Up To Speed	40A7D
	"W"	
WCP-N	Write Clock Pulse	40A8D
WCP	Write Clock Pulse	47C4B
WCPD-N	Write Clock Pulse Delayed	40A8C
WCP0-N	Write Clock Pulse 0	39C4B
WE-P	Write Error	44A7E

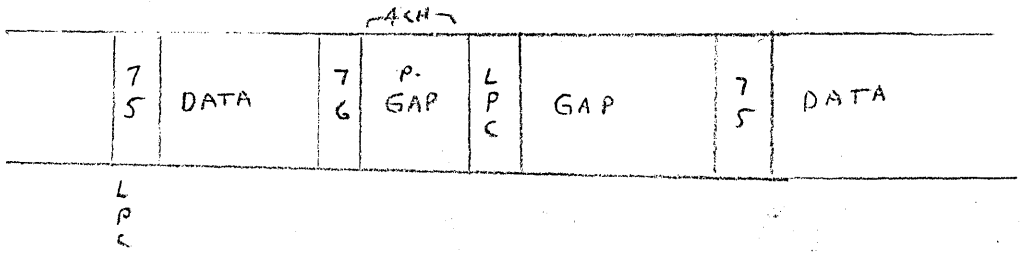
Signal Abbr.	Description	Source
WINFC-N	Write Information Complete	40C6C
WINT-N	Write Interrupt	37C3E
WP-P	Write Pulse	40A7B
WP-N	Write Pulse	40A7C
WR-N	Write	36C6B
WR-N	Write	37A3B
WR-1N	Write	37B4H
WR-0N	Write	37B4H
WR-P	Write	47C3C
WRA-N	Loads "A" Buffer During Write Instruction	39A3B
WRB-N	Loads "B" Buffer During Write Instruction	39A3C
WRDC-1N	Write Or Read Data Control	39C2A
WRDC-0N	Write Or Read Data Control	39C2A
WRDC-1P	Write Or Read Data Control	39C2B
WRDC-0P	Write or Read Data Control	39C2C
W0-N	Write Information	38A4B
W1-N	Write Information	38A4B
W2-N	Write Information	38A4B
W3-N	Write Information	38A4B
W4-N	Write Information	38A4B
W5-N	Write Information	38A4B
W6-N	Write Information	38A8B
WRITE INFO 2^0-2^6	Write Information to Tape Stations	47C8B-C5D

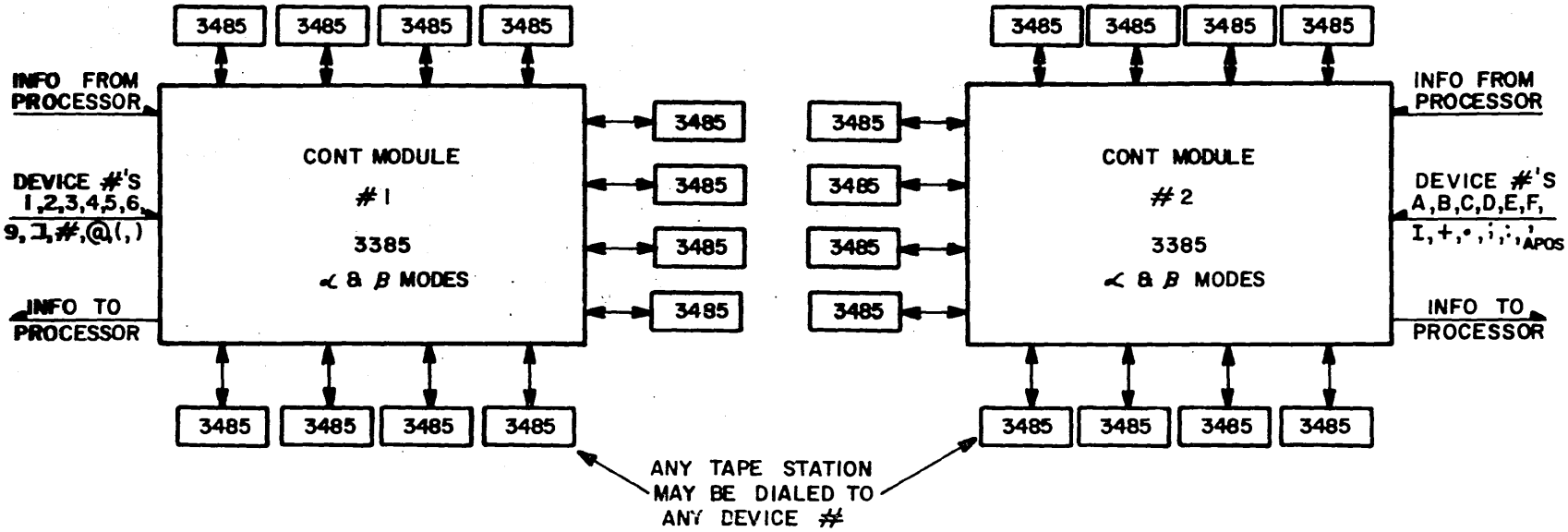
Signal Abbr.	Description	Source
33KC-1N	33 KC Flip-flop	40B6B
33KC-0N	33 KC Flip-flop	40B6B
66KC/S-N	66 KC Oscillator	45C3C
66KC/S-P	66 KC Oscillator	45C3C
100KC/S-N	100 KC Oscillator	45C3D
100KC/S-P	100 KC Oscillator	45C3B
120KC/S-P	120 KC Oscillator	45C3A
581-0N	581 Tape Station	40C5F
581-1N	581 Tape Station	40C5F
582-0N	582 Tape Station	40C4C
582-1N	582 Tape Station	40C4C
681-0N	681 Tape Station	40C4D
681-1N	681 Tape Station	40C4D
681-N	681 Tape Station	40B4A

3385

CONTROL MODULE

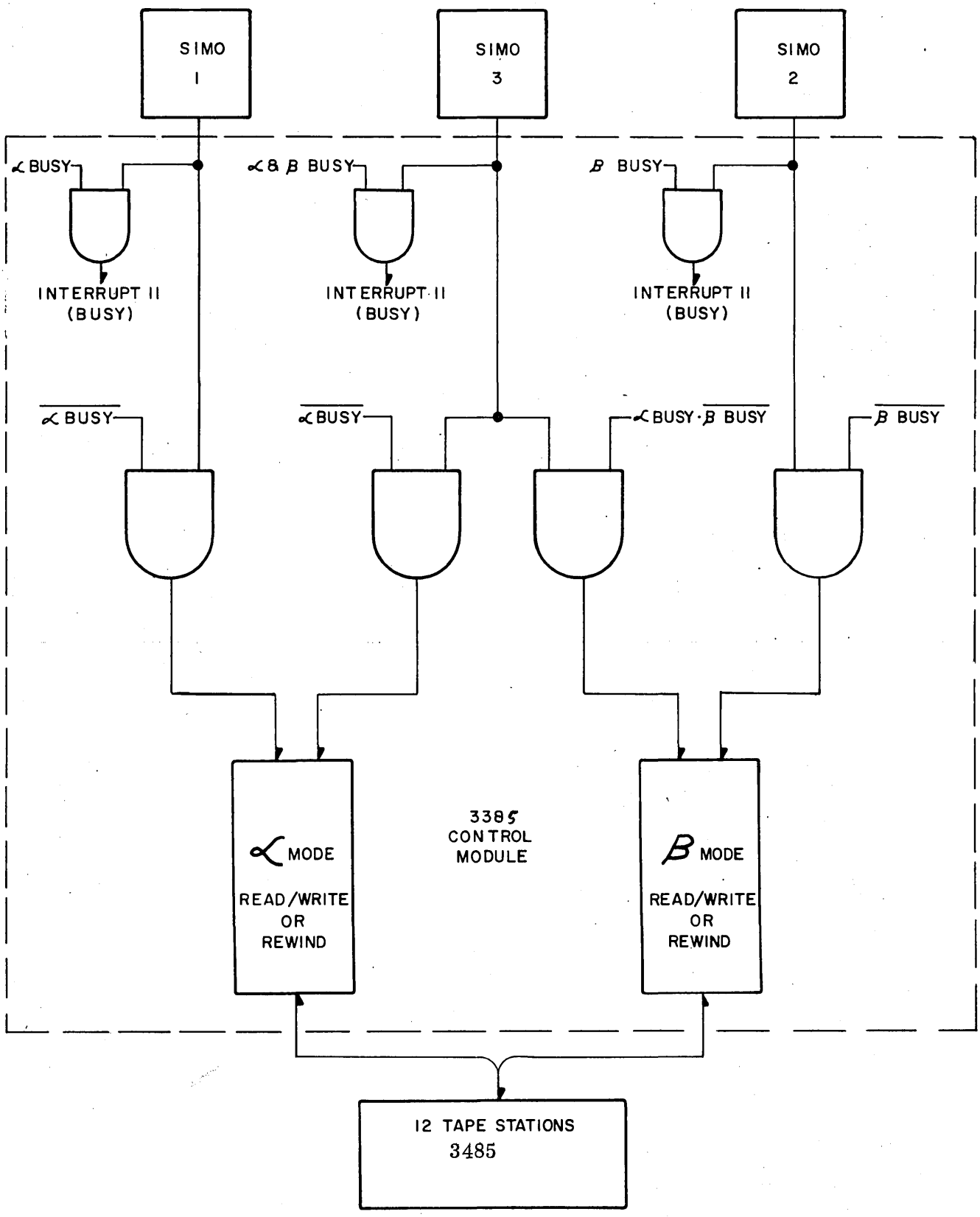
3385
CONTROL MODULE


4CH
75
DATA
76
P. GAP
LPC
GAP
75
DATA
LPC



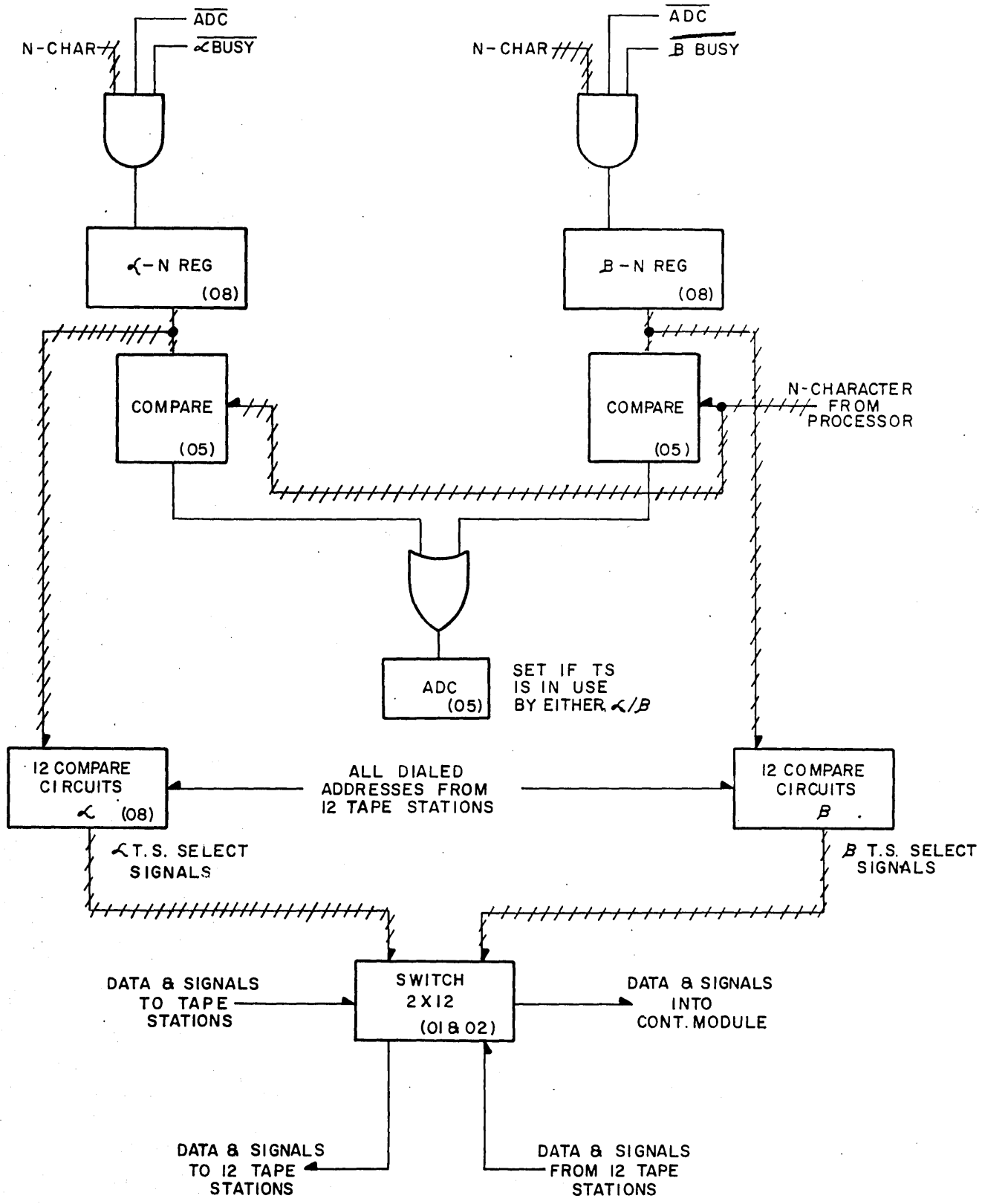
First 2 x 12				Second 2 x 12			
First 2 x 6		Second 2 x 6		Third 2 x 6		Fourth 2 x 6	
Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number
1	01	9	11	A	21	I	31
2	02	□	12	B	22	+	32
3	03	#	13	C	23	.	33
4	04	@	14	D	24	;	34
5	05	(	15	E	25	:	35
6	06	)	16	F	26	' (Apos)	36

3385 TAPE STATION ADDRESSES

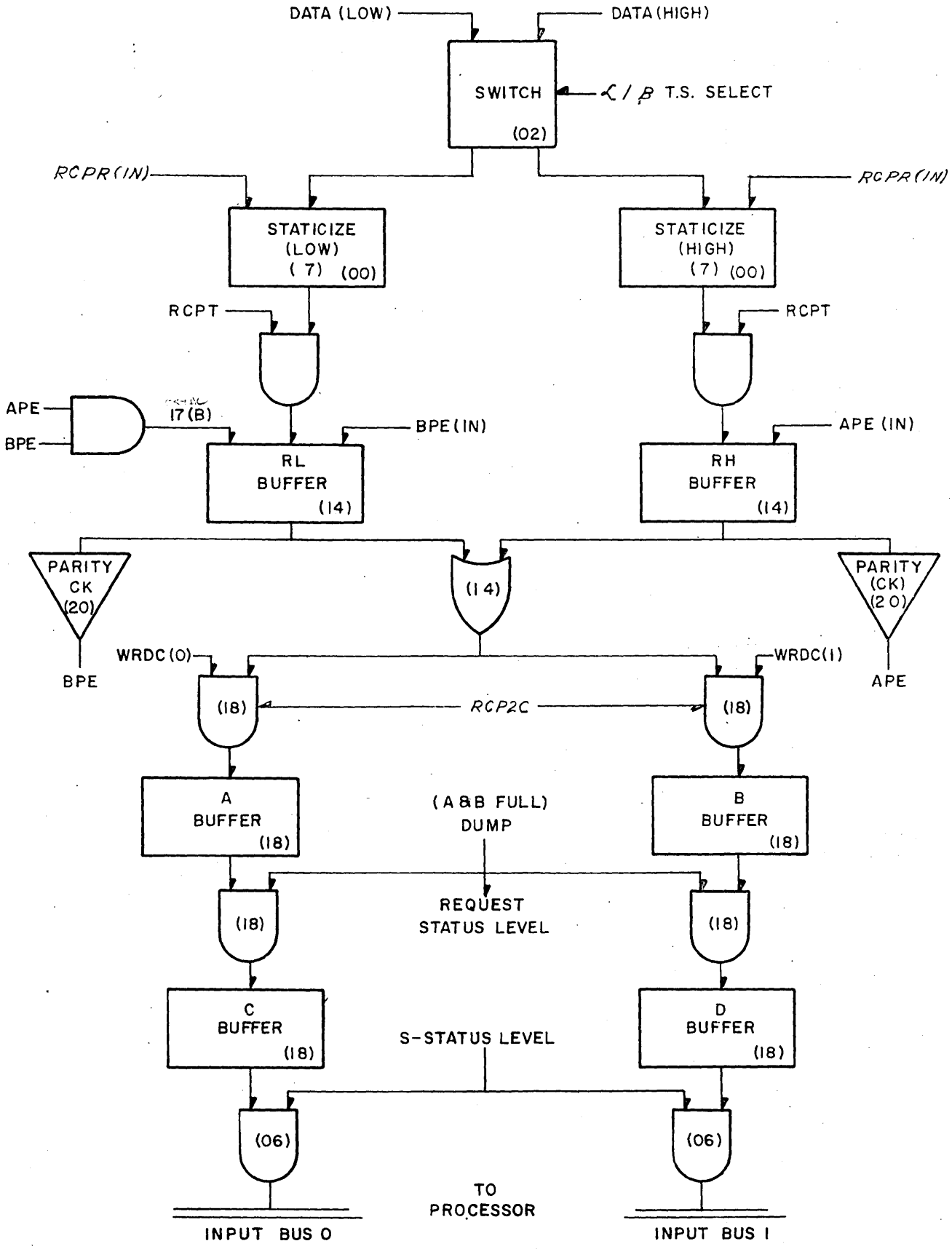


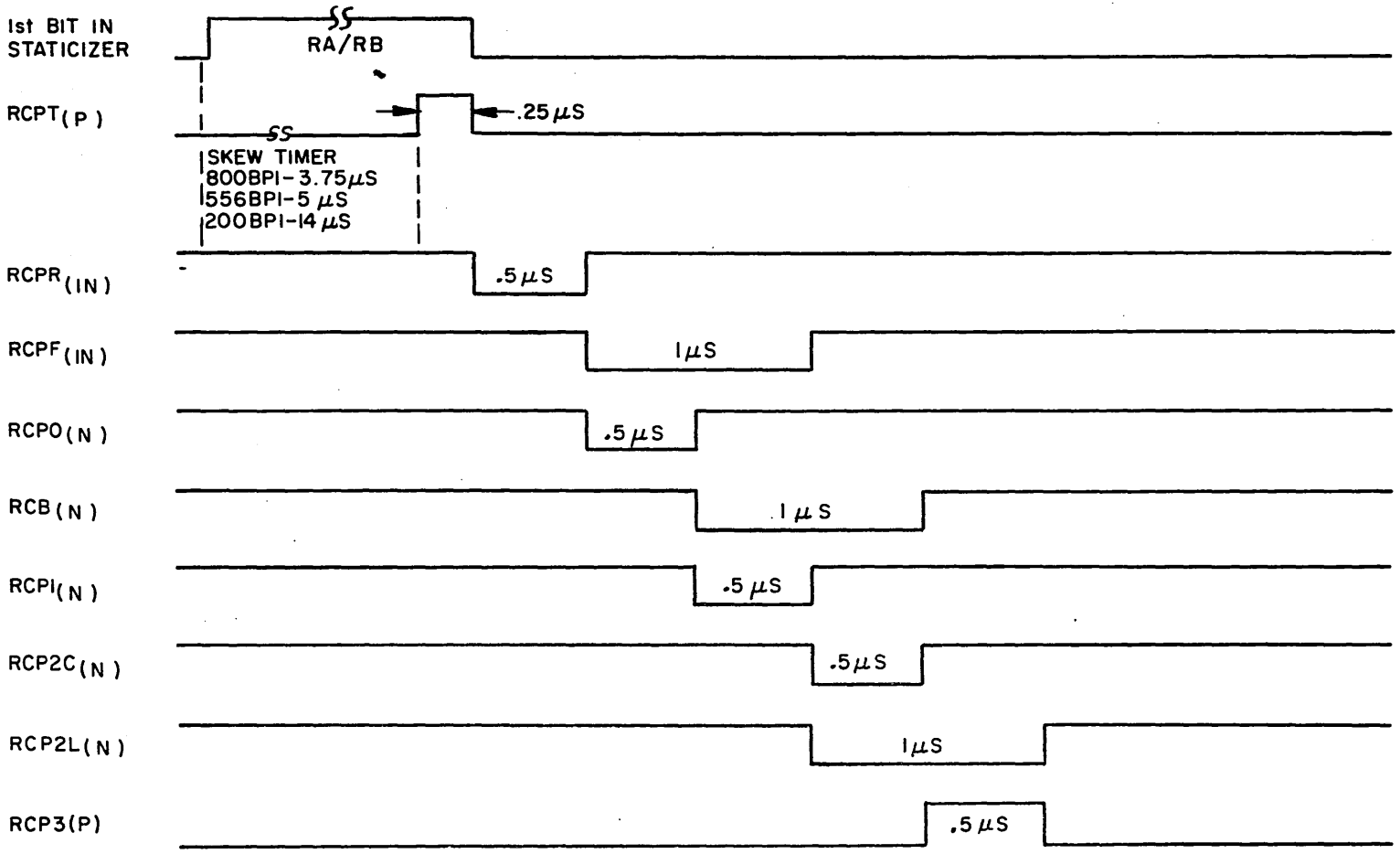
3385 MODE ASSIGNMENTS

— TAPE STATION COMPARE & SELECTION —

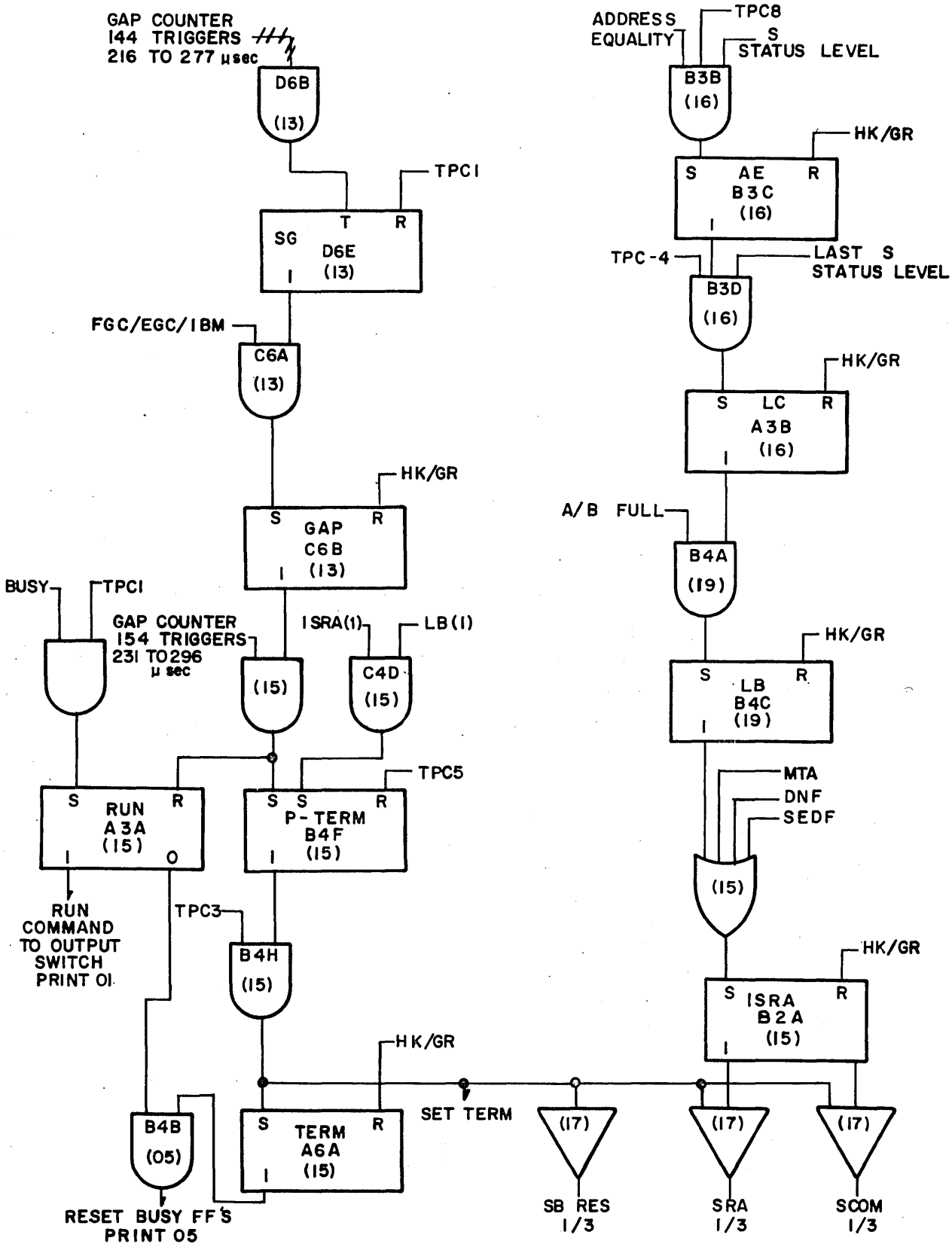


3385 - READ DATA FLOW

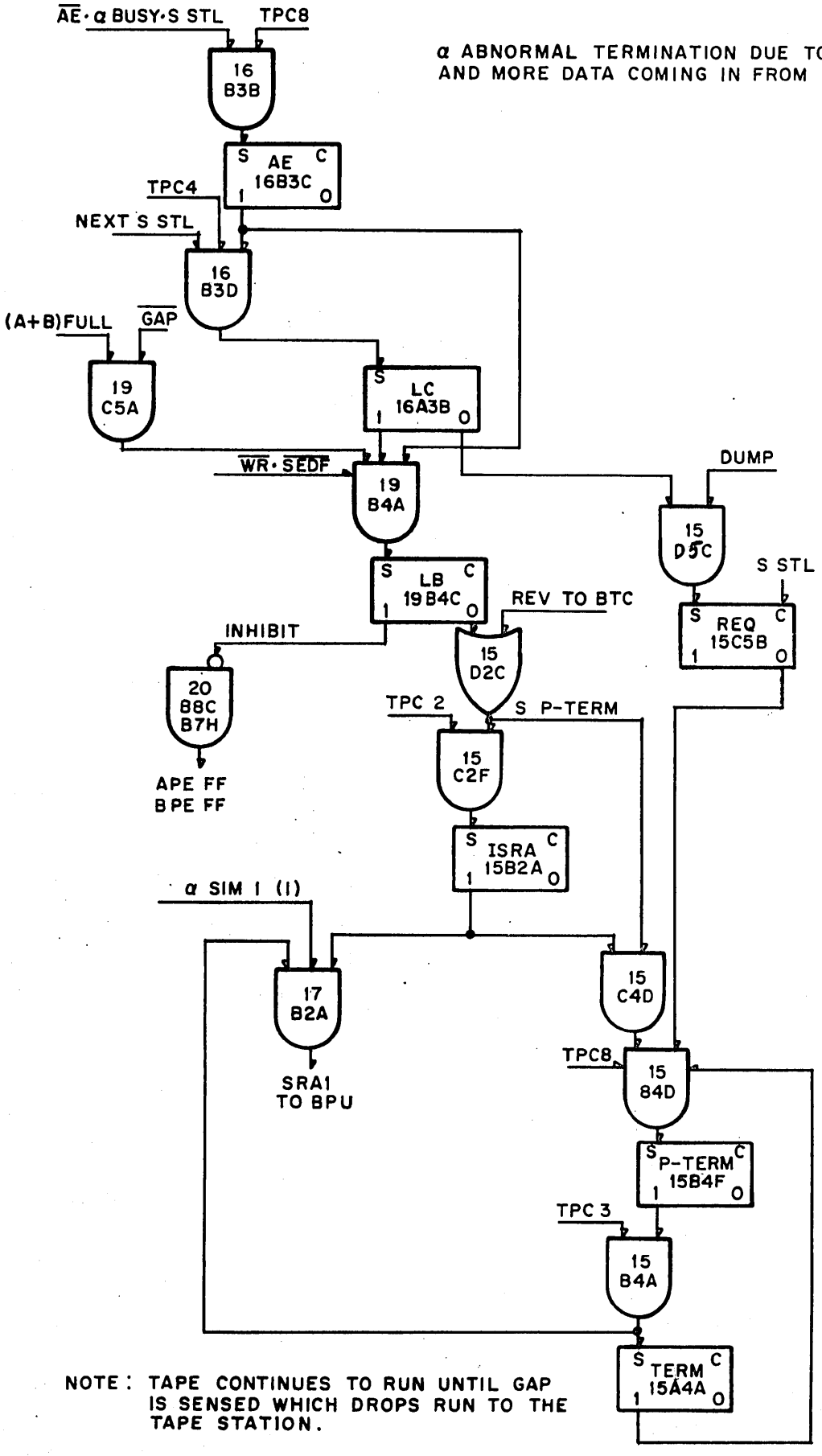




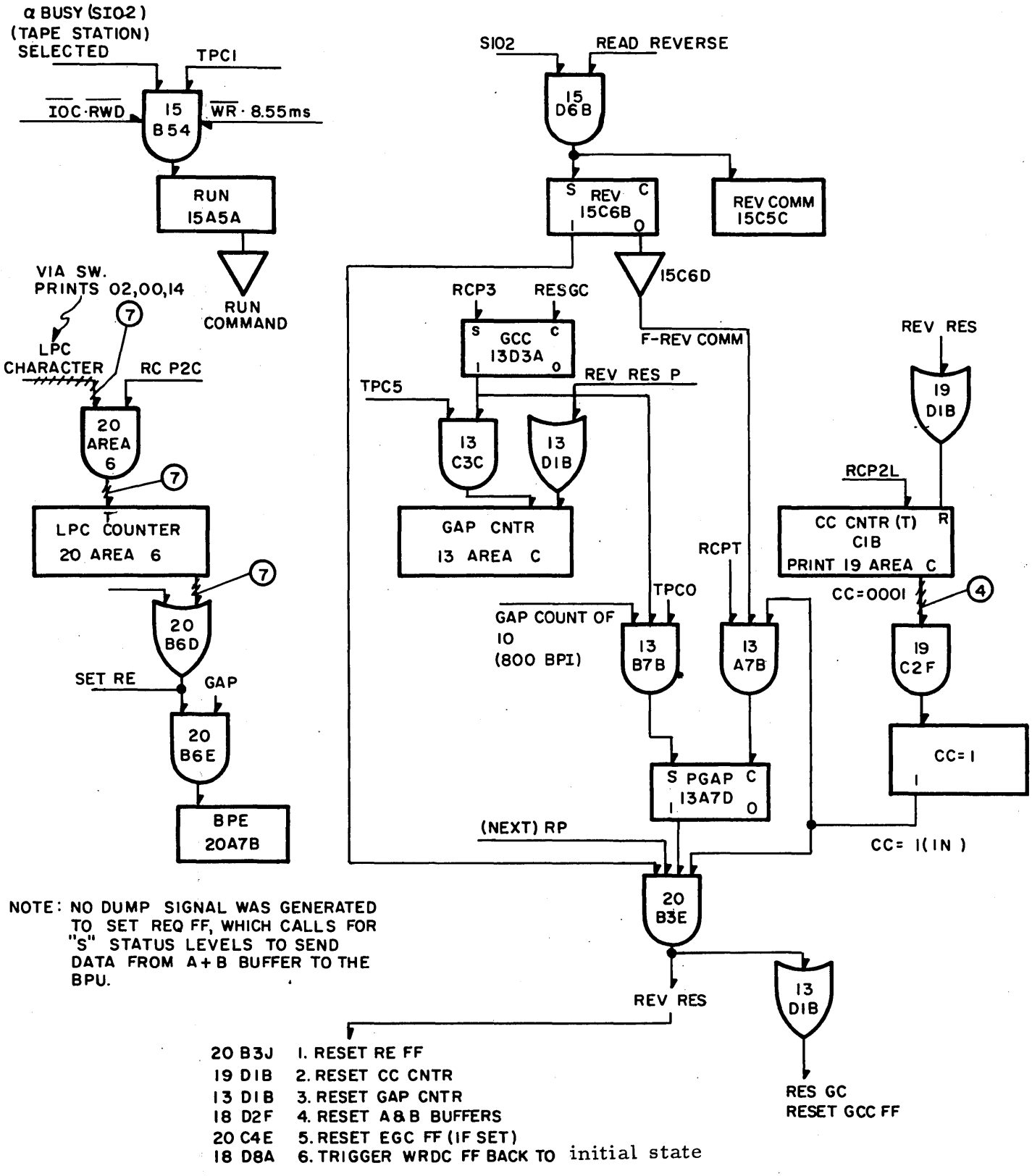
3385 READ CHARACTER TIMING



3385 READ TERMINATION



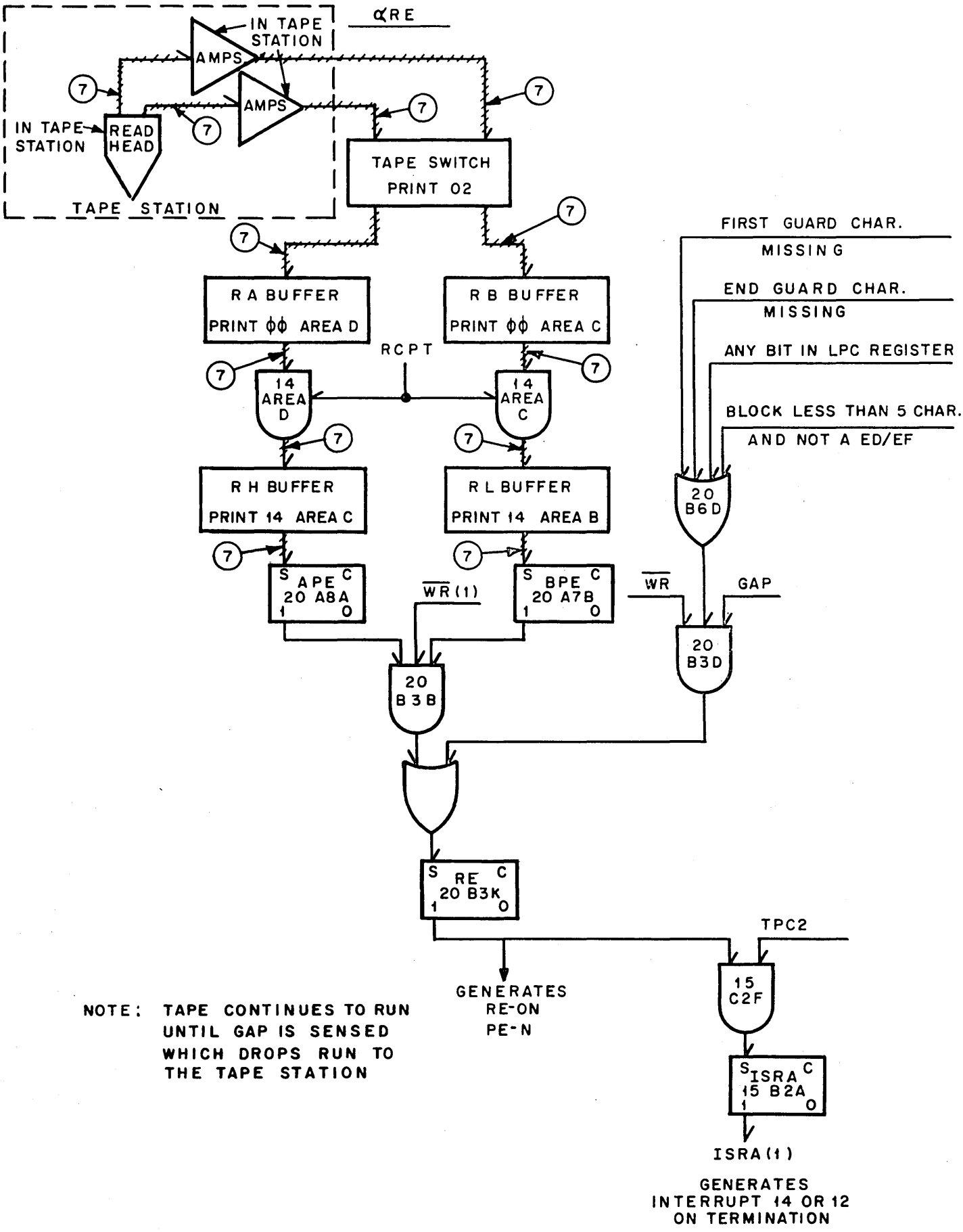
3385 READ TERMINATION ON ADDRESS EQUALITY



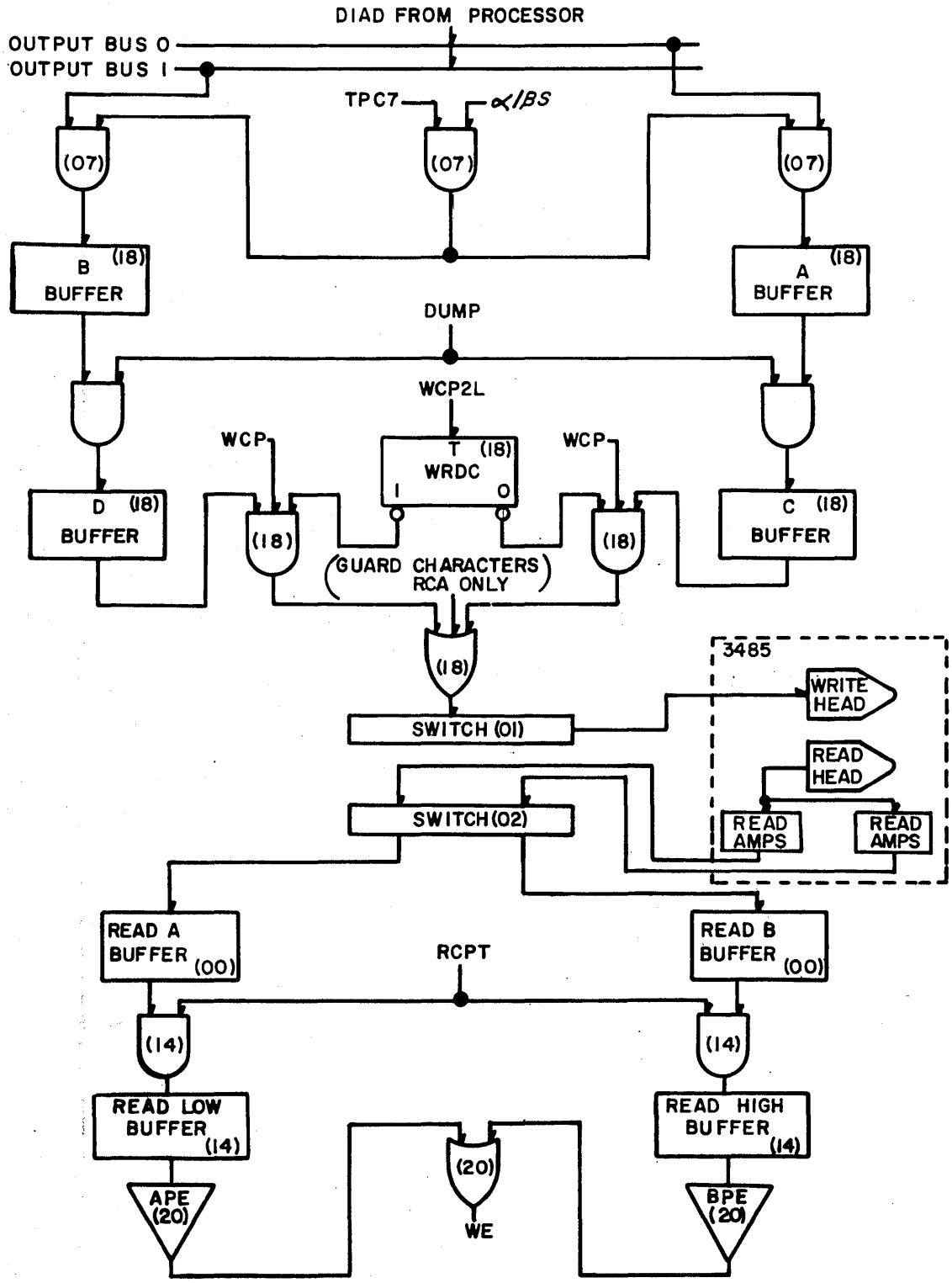
NOTE: NO DUMP SIGNAL WAS GENERATED TO SET REQ FF, WHICH CALLS FOR "S" STATUS LEVELS TO SEND DATA FROM A+B BUFFER TO THE BPU.

20 B3J	1. RESET RE FF
19 D1B	2. RESET CC CNTR
13 D1B	3. RESET GAP CNTR
18 D2F	4. RESET A&B BUFFERS
20 C4E	5. RESET EGC FF (IF SET)
18 D8A	6. TRIGGER WRDC FF BACK TO initial state

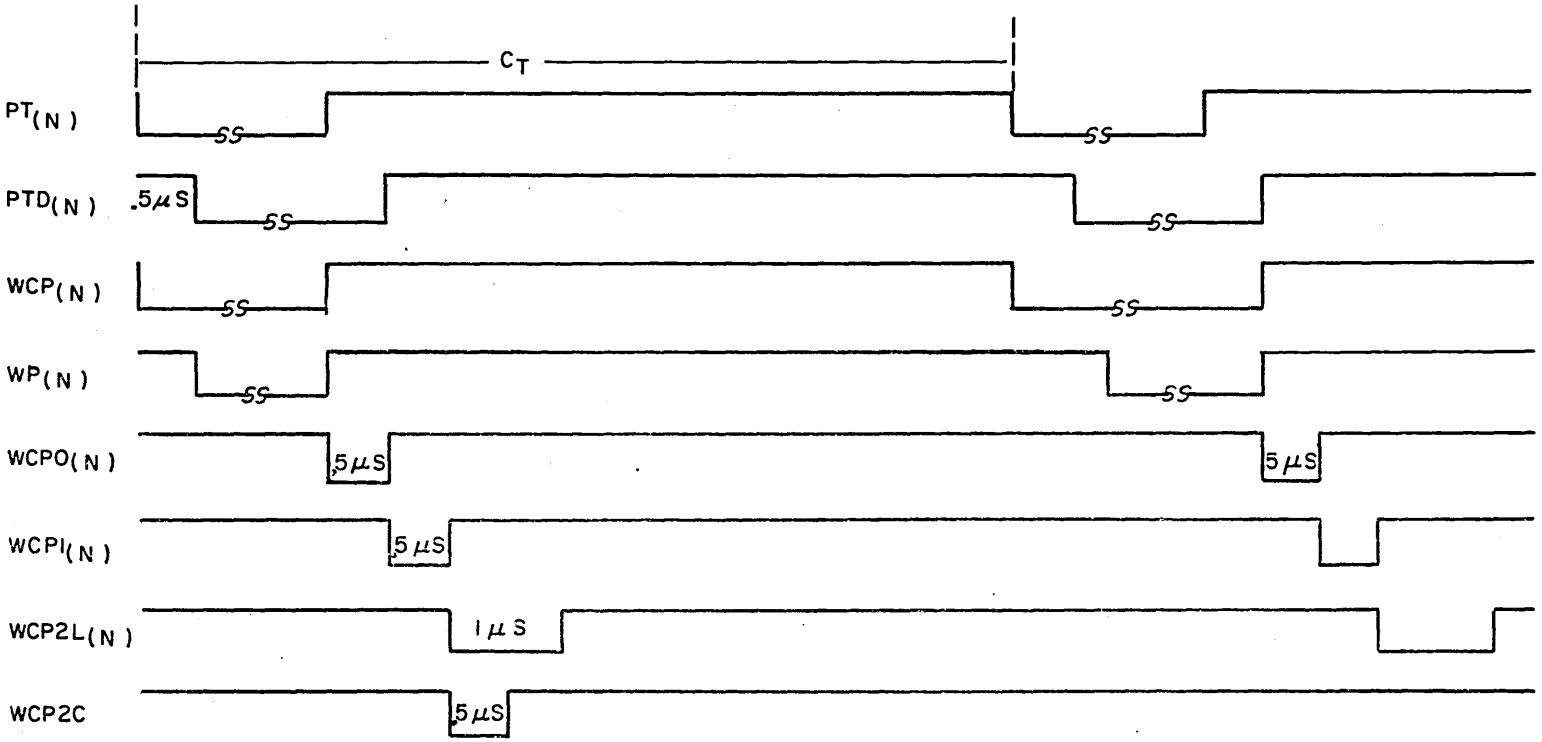
3385 LPC DETECTION IN READ REVERSE



3385 READ ERROR DETECTION



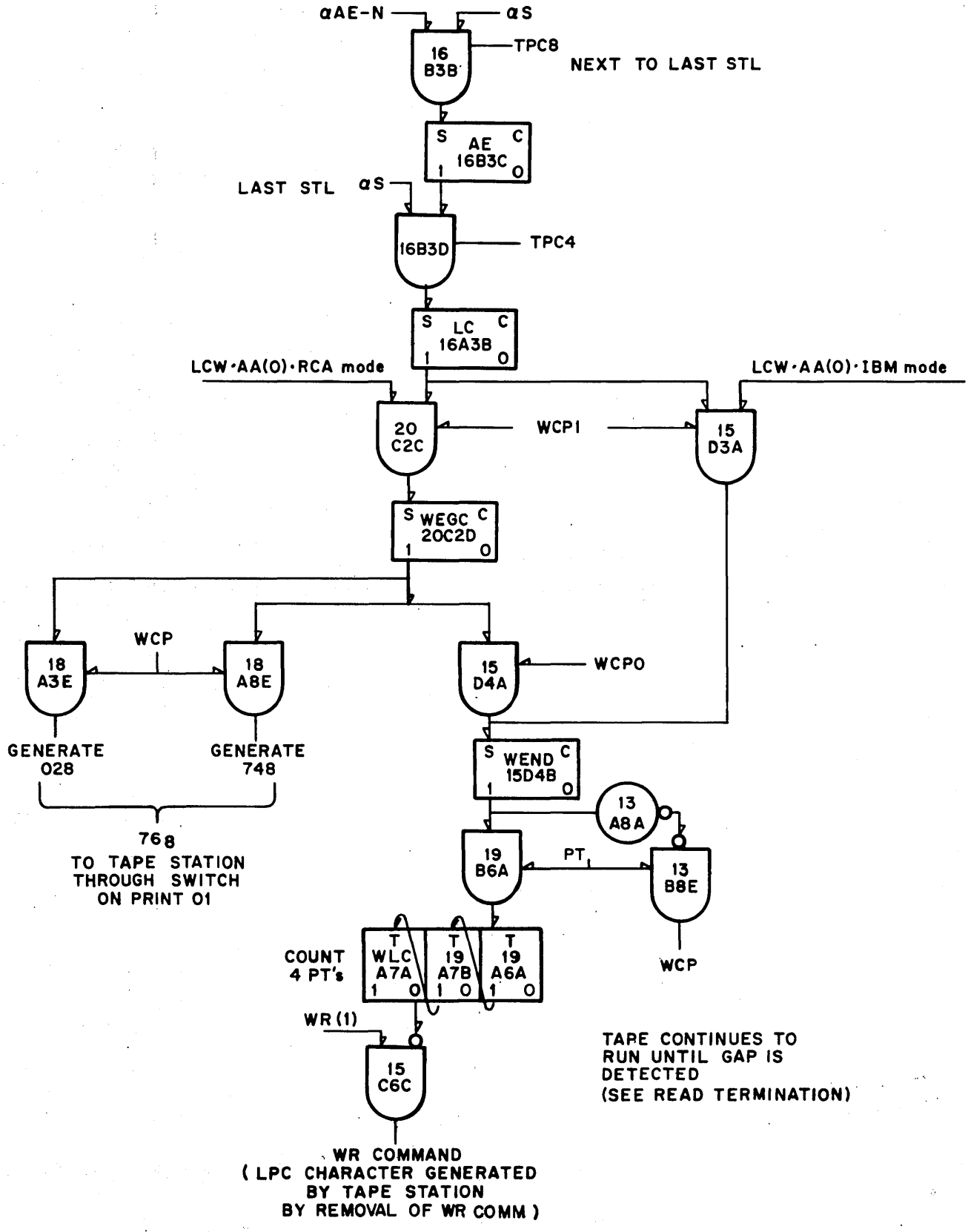
3385 WRITE INFORMATION FLOW



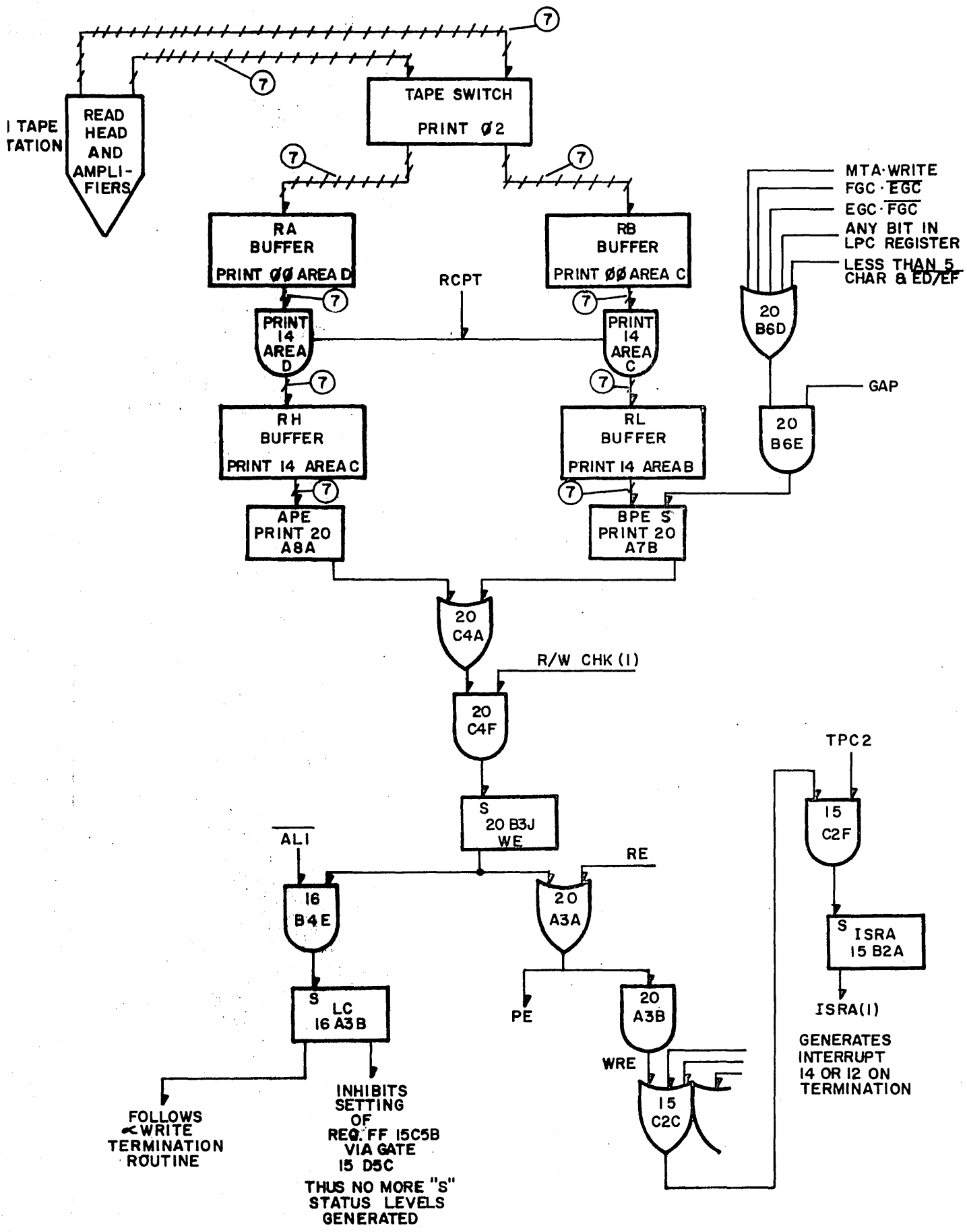
	PT	PTD	WCP	WP	CT
(800BPI) 120 KC	4.2	4.2	4.2	3.7	8.4
(556 BPI) 83.4 KC	5.9	5.9	5.9	5.4	11.8
(200 BPI) 30 KC	16.8	16.8	16.8	16.3	33.6

NOTE: ALL VALUES IN μS

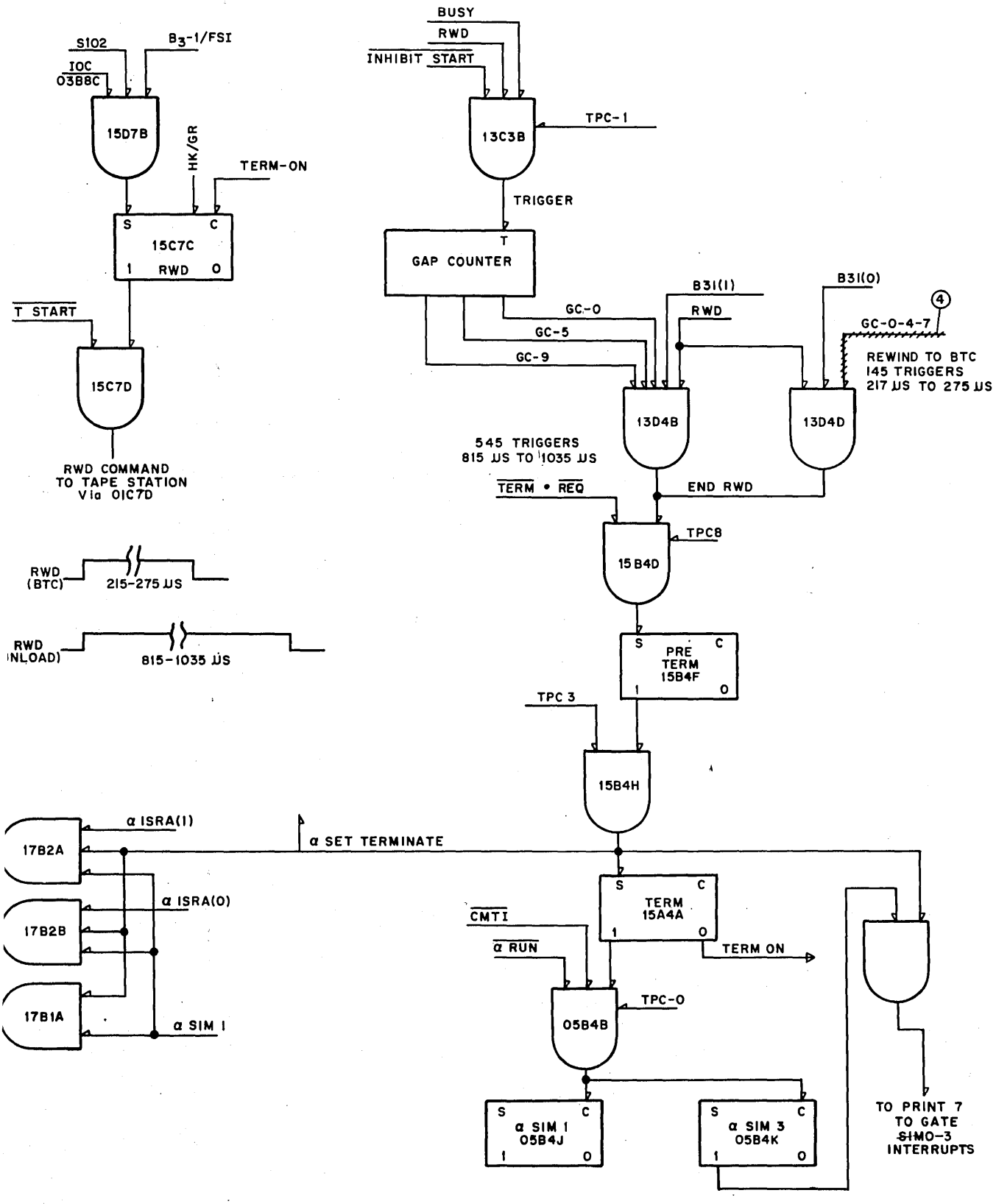
3385 WRITE CHARACTER TIMING



3385 GUARD CHARACTER & LPC GENERATION



3385 WRITE ERROR DETECTION


S102
B_3-1/FSI
IOC
03B8C
15D7B
HK/GR
TERM-ON
S
C
15C7C
1
RWD
0
T START
15C7D
RWD COMMAND
TO TAPE STATION
Via 01C7D
RWD
(BTC)
215-275 µS
RWD
(UNLOAD)
815-1035 µS
BUSY
RWD
INHIBIT START
13C3B
TPC-1
TRIGGER
T
GAP COUNTER
GC-0
GC-5
GC-9
B3I(1)
RWD
B3I(0)
GC-0-4-7
4
REWIND TO BTC
145 TRIGGERS
217 µS TO 275 µS
13D4B
13D4D
545 TRIGGERS
815 µS TO 1035 µS
TERM • REQ
END RWD
TPC8
15B4D
S
C
PRE
TERM
15B4F
1
0
TPC 3
15B4H
α ISRA(1)
α SET TERMINATE
17B2A
α ISRA(0)
17B2B
17B1A
α SIM 1
S
C
TERM
15A4A
1
0
CMTI
α RUN
TERM ON
TPC-0
05B4B
S
C
α SIM 1
05B4J
1
0
S
C
α SIM 3
05B4K
1
0
TO PRINT 7
TO GATE
SIMO-3
INTERRUPTS

ERROR CONDITIONS

ERROR	RECOGNITION GATE	TIMING
RE Indicated Error		
First Guard Character Missing	20B6B	Gap
End Guard Character Missing	20B6C	Gap
LPC Register Contains a Bit	20B6D	Gap
Less than 5 Characters and Not an ED/EF	20B5B	Gap
APE and BPE	20B3B	RCPO
WE Indicated Error		
APE or BPE	20C4A	RCPO
All RE Conditions	20B6D	Gap
Both Guard Characters Missing and RCA Mode	19B6E	Gap
Less than 8 Char. Written and $\overline{\text{ED/EF}}$ and IBM Mode	19B5B	Gap
DNF Indicated Error		
Run Command, Not LB +60us		
After Run Generated and:		
Write and No WR Return	19C4C	TPC47
No Run Return	19C3D	
Tape Not Operable	19C3E	
Write Return and Read	19C4D	
Reverse and No Rev. Return	19C3A	
Forward and Rev. Return	19C3B	
No BTL Return on a Rewind and Run Return/ Reverse Return Missing	19B3A	Gap Count 144

ERROR CONDITIONS - Continued

ERROR	RECOGNITION GATE	TIMING
MTA (Sensible Error in Read Only)		
RCA Mode, 16 Characters Read and Missing Both Guard Characters	19B6E	P-Gap
IBM Mode Less Than 9 Characters and $\overline{EOF}$ (17_8)	19B5D	GC-7
ISRA Interrupt 12, 13, or 14 with no Other Alarms		
SED/EF	15C2E	TPC2
Write End and ETW	15D2D	
Long Block Set	15D2C	
BTL Return and a Reverse Instruction	15D2B	

SIO 1 - 3385 CONTROL MODULE

SIO 1 Level - Set SIO H

If N Character for Control Module Generate CMSIO
If CMSIO • IOS Generate TS
Reset ONB and ADC F. F. 's
If CMSIO • $\overline{\text{IOS}}$ • ADC(0) • $\left[\overline{(\text{SOP2})}/\overline{(\text{SOP3} \cdot \alpha\ \text{BUSY})}\right]$ Generate α TI
If CMSIO • $\overline{\text{IOS}}$ • ADC(0) • $\left[(\text{SOP2})/(\text{SOP3} \cdot \alpha\ \text{BUSY})\right]$ Generate β TI

TPC 1 - Set TPC 13

If CMT1 • $\overline{\alpha\ \text{SIM1}} \cdot \overline{\text{SOP2}} \cdot \overline{\text{SOP3}}$ Generate SIM1 ER/ALR
If CMT1 • SOP2 • $\overline{\beta\ \text{SIM2}}$ Generate SIM2 ER/ALR
If CMT1 • $\overline{\text{SB3}}$ • SOP3 Generate SIM3 ER/ALR
If CMSIO • $\overline{\alpha\ \text{BUSY}}$ Generate α HK
If CMSIO • $\overline{\beta\ \text{BUSY}}$ Generate β HK

TPC 2
If $\overline{\beta\ \text{BUSY}}$ • β TI Generate β SISI
If $\overline{\alpha\ \text{BUSY}}$ • α TI Generate α SISI
If α SISI $(\overline{\text{RR}} \cdot \text{OB10}/\text{RR} \cdot \overline{\text{OB10}})$ Set α ISI
If β SISI $\overline{\beta\ \text{BUSY}} \cdot \beta\ \text{TI} \cdot (\overline{\text{RR}} \cdot \text{OB10}/\text{RR} \cdot \overline{\text{OB10}})$ Set β ISI
If α SISI • OB10 Set α WRDC
If α SISI • $\overline{\text{OB10}}$ Reset α WRDC
If β SISI • OB10 Set β WRDC
If β SISI • $\overline{\text{OB10}}$ Reset β WRDC
If N = αN/βN Set ADC
If TS • OB10 Set A30
If TS • OB11 Set A31
If TS • OB12 Set A32

TPC 4 - Set TPC 47

Reset TPC 13

If ($\overline{\alpha\,\text{BUSY}}$ • TS • $\overline{\text{ADC}}$)/($\overline{\alpha\,\text{BUSY}}$ • α TI) Gate N to α N Register

If ($\overline{\beta\,\text{BUSY}}$ • TS • α BUSY • $\overline{\text{ADC}}$)/ (βTI • $\overline{\beta\,\text{BUSY}}$) Gate N to β N Register

TPC 7

TPC 8 - Reset TPC 47

SIO 2 - 3385 CONTROL MODULE

SIO 2 Level

If A30(1)/A31(1)/A32(1) Gate Control Module Sense Indicators to IB1 (0-4)

If TS • N ≠ α N Generate αDS

If TS • N ≠ βN Generate βDS

If α DS Gate Tape Station Returns to IB0(0-4)

If βDS Gate Tape Station Returns to IB0 (0-4)

If $\overline{N5}$ • (RR/RF) • $\overline{SOP3}$ • $\overline{SOP2}$ Reset SEDF1 (CTC)

If $\overline{N5}$ • (RR/RF) • SOP2 Reset SEDF2 (CTC)

Reset OB0 thru OB5

If TS • α BUSY • β BUSY • A30(0) • A31(0) • A32(0) • ADC(0)
Inhibit Setting ONB

If (α TI • $\overline{IOS}$ • α NST • $\overline{\alpha \text{ BUSY}}$)/(CMTI • ADC(1))/($\beta$TI • βBUSY)/
(α TI • α BUSY)/(SOP3 • $\overline{IOS}$ • SB3)/(SOP2 • SB2)/(SB1 • $\overline{SOP2}$ •
$\overline{SOP3}$ • $\overline{IOS}$)/(β TI • β NST • $\overline{\beta BUSY}$ • $\overline{IOS}$)
Inhibit Setting ONB

TPC 1 - Set TPC 13
Reset SIO H

TPC 2 If IOC Gate Output Bus to OB (0 - 5)

If αTI • $\overline{\alpha ER}$ • $\overline{\alpha BUSY}$ Gate Selected Tape Station Conditions to
α800, α200, αEVEN/ODD, αIBM/RCA

If βTI • $\overline{\beta ER}$ • $\overline{\beta BUSY}$ Gate Selected Tape Station Conditions to
β800, β200, βEVEN/ODD and βIBM/RCA

If αTI • $\overline{\alpha ER}$ • $\overline{\alpha BUSY}$ • OB10 Set αFSI

If βTI • $\overline{\beta ER}$ • $\overline{\beta BUSY}$ • OB10 Set βFSI

If IOC • αTI • $\overline{\alpha ER}$ • $\overline{\alpha BUSY}$ • OB11 Set αB31

If IOC • βTI • $\overline{\beta ER}$ • $\overline{\beta BUSY}$ • OB11 Set βB31

If IOC • αTI • $\overline{\alpha ER}$ • $\overline{\alpha BUSY}$ • OB12 Set αB32

If IOC • βTI • $\overline{\beta ER}$ • $\overline{\beta BUSY}$ • OB12 Set βB32

TPC 3 If P-TERM(1) Set TERM

TPC 4 - Set TPC 47
Reset TPC 13

If αTI • $\overline{\alpha BUSY}$ Generate αSIO 2 Set

If βTI • $\overline{\beta BUSY}$ Generate βSIO 2 Set

If α SIO2 Set • ER Set α ER

If β SIO2 Set • ER Set β ER

If α SIO2 Set • WR Set α WR

If β SIO2 Set • WR Set β WR

If α SIO2 Set • RR Set α REV and α REV COMM

If β SIO2 Set • RR Set β REV and β REV COMM

If α SIO2 Set • IOC • [αB31(1)/ αFSI(1)] Set αRWD

If β SIO2 Set • IOC • [βB31(1)/ βFSI(1)] Set βRWD

If α SIO2 Set • $\overline{\alpha NST}$ • WR Set αREQ

If β SIO2 Set • $\overline{\beta NST}$ • WR Set βREQ

If α SIO2 Set • α WNE • α IBM(0) Set α WFGC

If β SIO2 Set • β WNE • β IBM(0) Set β WFGC

If α WR(1) • α ER(0) Generate α WNE

If β WR(1) • β ER(0) Generate β WNE

TPC 5

TPC 6

TPC 7 If α TI • ONB(1) • $\overline{\text{SOP2}}$ $\overline{\text{SOP3}}$ α SIM3(0) $\overline{\alpha \text{ NST}}$ Set α SIM 1

If α TI • ONB(1) • α SIM1(0) • SOP3 • $\overline{\alpha \text{ NST}}$ Set α SIM 3

If β TI • ONB(1) • β SIM3(0) • SOP2 • $\overline{\text{SOP3}}$ • $\overline{\beta \text{ NST}}$ Set β SIM2

If β TI • ONB(1) • SOP3 • β SIM2(0) • α SIM3(0) • $\overline{\text{SOP2}}$ • $\overline{\beta \text{ NST}}$
Set β SIM3

If α SIM1(1)/ α SIM3(1) Generate α BUSY

If β SIM2(1)/ β SIM3(1) Generate β BUSY

If α SIO2 Set • α B32(0) • α RWD(0) • α TERM(0) • α REQ(0) • IOC
Set α P-TERM

If β SIO2 Set • β B32(0) • β RWD(0) • β TERM(0) • β REQ(0) • IOC
Set β P-TERM

TPC 8 - Reset TPC 47

If α AE • α BUSY • $\overline{\text{RUN}}$ Set AE

If β AE • β BUSY • $\overline{\text{RUN}}$ Set AE

S and READ

General — Entire Status Level

If $\overline{\text{ISA}}$ - Gate C to IB0

If $\overline{\text{ISB}}$ - Gate D to IB1

TPC 0 -

TPC 1 -

TPC 4 - Set LC If AE (1)

Reset C and D Registers

TPC 5 -

TPC 8 - Set AE If Busy • AE

Reset ISI F. F.

S and WRITE

General

TPC 0 -

TPC 1 -

TPC 3 -

TPC 4 - Set LC If AE (1)

TPC 5 -

TPC 7 - If WNE Gate OB0 to A Buffer

If WNE Gate OB1 to B Buffer

TPC 8 - Set AE If Busy • AE

Reset ISI F. F.

3385 ABBREVIATION AND SOURCE LIST

Abbreviation	Name	General Print Element	α Print Element	β Print Element
AA-1N	Character in "A" Buffer		18B5A	18B5A
A thru M-N	(Tape Station Trunk Designations)		08B6D	08B4E
(A • B)Full-N	"A" and "B" Buffers Full		18B2H	18B2H
(A /B)Full-N	Character in "A" or "B" Buffer		18B2E	18B2E
ADC-1N	Address Compare	05C4D		
AE-1N	Address Equality		16B3C	21B3C
APE-1N	A Buffer Parity Error		20A8B	20A8B
A30-1N	A_3 Character 2^0 Bit	07A6B		
A31-1N	A_3 Character 2^1 Bit	07A7B		
A32-1N	A_3 Character 2^2 Bit	07A8B		
BB-1N	Character in "B" Buffer		18B2B	18B2B
BPE-1N	B Buffer Parity Error		20A7B	20A7B
B31-1N	B_3 Character 2^1 Bit		16C3B	21C3B
B32-1N	B_3 Character 2^2 Bit Negative		16C3A	21C3A
B32-1P	B_3 Character 2^2 Bit Positive		16C3C	21C3C
BUSY-N	_____Mode Busy Negative		05A4A	05A2A
BUSY-P	_____Mode Busy Positive		05A4C	05A2B
BUSY-A-N	_____Mode Busy ("A" Inverter) Negative		05B3A	05C1A

Abbreviation	Name	General Print Element	α Print Element	β Print Element
C-HK/GR-N	Mode Controlled Housekeeping or General Reset		13A6B	13A6B
CC0 thru CC3-1N	Character Counter (Stage 0, 1, 2, 3)		19C1B-C2C	C1B-C2C
CC=1-N	Character Counter Count = 0		19A2C	19A2C
CC=1-1N	Character Counter Count = 1		19B2B	19B2B
CC=5-1N	Character Counter Count = 5		19A2B	19A2B
CC=16-1N	Character Counter Count = 16		19A2A	19A2A
CMSIO-N	Control Module Recognized SIO (Negative)	05C8C		
CMTI-N	Control Module Tape Instruction (Negative)	05B7B		
CMTI-P	Control Module Tape Instruction (Positive)	05B7A		
CUTS-P	Control Up to Speed (Write Following a Read)		09B2D	09A2A
C0 thru C6-1N	Bits in "C" Buffer		18 Area B	18 Area B
DNF-1N	Tape Station Not Following Commands		19A3A	19A3A
DNF-P	Not Following α or β Mode	17A6D		
DS-N	_____ Device Sense		05C3B	05C2C
DUMP-N	Dump ("A" Buffer to "C" Buffer and "B" to "D")		18D4J	18D4J
D0 thru D6-N	Bits in "D" Buffer		18 Area B	18 Area B
EGCP-N	End Guard CharacterPresent (Negative)		20B4E	20B4E
EGCP-P	End Guard Character Present (Positive)		20A4A	20A4A
END RWD-P	End Rewind (Positive)		13D4B	13D4B

Abbreviation	Name	General Print Element	α Print Element	β Print Element
ER-1N	Erase		15C8A	15C8A
ER-N	Erase (Negative) Operation Code	03C8C		
ER-P	Erase (Positive) Operation Code	03B8A		
EVEN-1N	Even or Odd Parity Mode Control		16C5B	21C5B
FHK/GR-P	First Housekeeping or General Reset		05A5E	05A3E
FSI-1N	Final Strobe Inhibit		16C2A	21C2A
F-REV-N	"F" Driver - Reverse FF		15C6D	15C6D
FGCP-N	First Guard Character Present (Negative)		20B5B	20B5B
FGCP-P	First Guard Character Present (Positive)		20A5A	20A5A
FF1-1N	First Fill #1		18C6A	18C6A
FRES-P	Fill Reset		18D6A	18D6A
GAP-N	Gap		13C6D	13C6D
GAP-1N	Gap		13C6B	13C6B
GC1 thru GC9-N	Gap Counter (Stages)		13 Area C	13 Area C
GR4A-P	General Reset (Driver #4)	10D5F		
HK/ALR-P	Housekeeping or Alarm Reset		05B5A	05B3B
HK/GR-P	Housekeeping or General Reset		05A5F	05A3F

Abbreviation	Name	General Print Element	α Print Element	β Print Element
IBM-OP	IBM Mode		16C4D	21C4D
IBM-IP	IBM Mode		16C4C	21C4C
IB00 thru 06	Input Bus 0 Bits 2^0 thru 2^6	06 Area A		
IB10 thru 16	Input Bus 1 Bits 2^0 thru 2^6	06 Area A		
ICC-P	Inhibit Character Counter (Count of 15)		19D2B	19D2B
IS-P	Inhibit Start		15B5B	15B5B
ISA-P	Inhibit Strobe "A"		15A8A	15A8A
ISB-P	Inhibit Strobe "B"		15A7C	15A7C
ISG-N	Inhibit Sense Gap		13C7B	13C7B
ISI-1N	Initial Strobe Inhibit		16A2B	21A2B
ISRA-1N	Initiate Simultaneous Requires Attention		15B2A	15B2A
LB-1N	Long Block		19B4C	19B4C
LB1-1N	Long Block Simo 1			17C2A
LB2-1N	Long Block Simo 2		17C5B	
LB3-1N	Long Block Simo 3		17C7A	17C7A
LC-1N	Last Character		16A3B	21A3B
LCW	Last Character Write		20D2B	20D2B

Abbreviation	Name	General Print Element	α Print Element	β Print Element
MTA-1N	Magnetic Tape Alarm		19A5A	19A5A
MTA1-1N	Magnetic Tape Alarm Simo 1		17C2B	
MTA2-1N	Magnetic Tape Alarm Simo 2			17C4A
MTA3-1N	Magnetic Tape Alarm Simo 3		17C7B	17C7B
NC-0N	Nine Count (Character Counter = 9)		19B2A	19B2A
NST-N	No Start (Tape Station Rewinding or Inoperable)		05B5H	05B3F
NST-P	No Start (Tape Station Rewinding or Inoperable)		05B5C	05B2A
OB0-N	Output Bus 0 2^0 Bit	07A1A		
OB0+OB1-N	Output Bus 0 2^0 or 2^1 Bit	07B1B		
OB1+OB2-N	Output Bus 0 2^1 or 2^2 Bit	07B2F		
OB2-N	Output Bus 0 2^2 Bit	07A2A		
OB3-N	Output Bus 0 2^3 Bit	07A3B		
OB3+OB4N	Output Bus 0 2^3 or 2^4 Bit	07B3N		
OB4+OB5N	Output Bus 0 2^4 or 2^5 Bit	07B3F		
OB5 N	Output Bus 0 2^5 Bit	07A3A		
OB10-N	Output Bus 1 2^0 Bit	07D6C		
OB10-P	Output Bus 1 2^0 Bit	07B6A		
OB10A-N	Output Bus 1 2^0 Bit (A Driver)	07B6B		
OB11-N	Output Bus 1 2^1 Bit	07D6B		

Abbreviation	Name	General Print Element	α Print Element	β Print Element
OB12-N	Output Bus 1 2^2 Bit	07D6A		
ONB(1N)	Operable and Not Busy	05		
ONB-P	Operable and Not Busy	05 C4E		
P-GAP-1N	Pre Gap		13A7D	13A7D
P-GAP-1P	Pre Gap		13A8B	13A8B
P-TERM-1N	Pre Terminate		15B4F	15B4F
PE-N	Parity Error		20A3A	20A3A
PE1-1N	Parity Error Simo 1		17C2C	
PE2-1N	Parity Error Simo 2			17C4B
PE3-1N	Parity Error Simo 3		17C6A	17C6A
PT-N	Pulse Timer		13B4A	13B4A
PTD-N	Pulse Timer Delayed		13A5B	13A5B
RCB-N	Read Clock Pulse (B Designation)		16C4B	21C4B
RCP0-N	Read Clock Pulse (0 Designation)		16A5B	21A5B
RCP1-N	Read Clock Pulse (1 Designation)		16A5A	21A5A
RCP2C-N	Read Clock Pulse (2C Designation)		16A5C	21A5C
RCP2L-N	Read Clock Pulse (2L Designation)		16A4A	21A4A
RCP3	Read Clock Pulse (3 Designation)		16B6B	21B6B
RCPR-1N	Read Clocking Pulse Register		16A8A	21A8A

Abbreviation	Name	General Print Element	α Print Element	β Print Element
RCPT-N	Read Clocking Pulse Trigger		16B8E	21B8E
RDD-1N	Read Data Delay		18C5A	18C5A
RE-1N	Read Error		20B3K	20B3K
RE-P	Read Error	17A7E		
REQ-1N	Request Status Level		15C5B	15C5B
RES-CC-P	Reset Character Counter		19C1A	19C1A
RES-GC-P	Reset Gap Counter		13C1A	13C1A
REV-1N	Reverse		15C6B	15C6B
REV COMM-1N	Reverse Command		15C5C	15C5C
REV RES-N	Reverse Reset		20B2B	20B2B
REV to BTC-P	Reverse to Beginning of Tape Control		15D2B	15D2B
RH0 thru 6-1N	Read "Hi" Buffer 2^0 thru 2^6 Bits		14 Area C	14 Area C
RI0 thru 6-N	Read Information 2^0 thru 2^6 Bits		14 Area B	14 Area B
RL0 thru 6 -1N	Read "Lo" Buffer 2^0 thru 2^6 Bits		14 Area B	14 Area B
RP P	Read "Bit" Present		16C8A	21C8A
RR/RF-N	Read Forward or Read Reverse	03C8A		
RUN-1N	Run		15A5A	15A5A
RUN COMM-N	Run Command		15A5B	15A5B
RWD-N	Rewind		15B7A	15B7A
RWD-1N	Rewind		15C7C	15C7C

Abbreviation	Name	General Print Element	α Print Element	β Print Element
R0A thru R6A-1N	Read Staticizer (To Read "Hi" Buffer)		00 Area D	00 Area C
R0B thru R6B-1N	Read Staticizer (To Read "Lo" Buffer)		00 Area C	00 Area B
S-N	"S" Status Level		03B2C	03B2B
SA-N	"S" Status Level (A Driver)		15D5D	15D5D
S REQ1-P	S1 Status Level Request		17A3A	
S REQ2-P	S2 Status Level Request			17A2A
S REQ3-P	S3 Status Level Request		17A7D	17A7D
SB RES1-P	Simo 1 Busy Reset		17B1A	
SБ RES2-P	Simo 2 Busy Reset			17B3A
SB RES3-P	Simo 3 Busy Reset		17B7C	17B7C
SCA-N	Station Connected Trunk A	10C8A		
SCB-N	Station Connected Trunk B	10C5B		
SCC-N	Station Connected Trunk C	10B8F		
SCD-N	Station Connected Trunk D	10B5F		
SCE-N	Station Connected Trunk E	11C8A		
SCF-N	Station Connected Trunk F	11C5B		
SCG-N	Station Connected Trunk G	11B8F		
SCH-N	Station Connected Trunk H	11B5F		
SCJ-N	Station Connected Trunk J	12C8A		
SCK-N	Station Connected Trunk K	12C5B		

Abbreviation	Name	General Print Element	α Print Element	β Print Element
SCL-N	Station Connected Trunk L	12B8F		
SCM-N	Station Connected Trunk M	12B5F		
SCOM1-P	Simo 1 Completed Normally		17B2B	
SCOM2-P	Simo 2 Completed Normally			17B4B
SCOM3-P	Simo 3 Completed Normally		17B7B	17B7B
SEDF-N	Sense ED or EF		19B7A	19B7A
SEDF-1N	Sense ED or EF		19C7F	19C7F
SEDF1-P	Simo 1 Sense ED or EF(CTC)		17B6B	
SEDF1-1N	Simo 1 Sense ED or EF		17C3A	
SEDF2-P	Simo 2 Sense ED or EF (CTC)			17B5B
SEDF2-1N	Simo 2 Sense ED or EF			17C5A
SEDF3-1N	Simo 3 Sense ED or EF		17C8A	17C8A
SET EVEN-N	Set Even Parity Mode	16D5A		
SET EVEN-P	Set Even Parity Mode	10,11,12C6B		
SET IBM-N	Set IBM Mode	16D4A		
SET IBM-P	Set IBM Mode	10,11,12C6C		
SET 200-N	Set 200 Bits Per Inch Mode	16D6B		
SET 200-P	Set 200 Bits Per Inch Mode	10,11,12C7D		
SET 800-N	Set 800 Bits Per Inch Mode	16D6A		
SET 800-P	Set 800 Bits Per Inch Mode	10,11,12C8B		

Abbreviation	Name	General Print Element	α Print Element	β Print Element
SG-1N	Sense Gap		13D6E	13D6E
SIM1-1P	Simo 1 (Busy)		05A4B	
SIM1-0P	Simo 1 (Busy)		17D6B	
SIM2-1P	Simo 2 (Busy			05B2N
SIM2-0P	Simo 2 (Busy)			17D6D
SIM3-1P	Simo 3 (Busy)		05A4D	05A1B
SIM3-0P	Simo 3 (Busy)		17D6E	17D6E
SIM1 ER/ALR-N	Simo 1 Error or Alarm Reset		05A6A	
SIM2 ER/ALR-N	Simo 2 Error or Alarm Reset			05A6B
SIM3 BUSY-P	Simo 3 Busy		05A3D	05A3D
SIM3 ER/ALR-N	Simo 3 Error or Alarm Reset		05A6C	05A6C
SIOH-0N	SIO 1 Hold Register	05D8B		
SIO2 SET-N	SIO 2 Set	10A5A	05B6A	05B6B
SISI-N	Set Initial Strobe Inhibit		16C2D	21C2D
SRA1-P	Simo 1 Mode Requires Attention		17B2A	
SRA2-P	Simo 2 Mode Requires Attention			17B4A
SRA3-P	Simo 3 Mode Requires Attention		17B8B	17B8B
STERM-N	Set Terminate		15A4B	15A4B
STROBE A-P	Strobe "A" of Processor (Inhibit)	17A4A		
STROBE B-P	Strobe "B" of Processor (Inhibit)	17A3B		

Abbreviation	Name	General Print Element	α Print Element	β Print Element
TERM-1N	Terminate		15A4A	15A4A
TI-N	Tape Instruction		05A7D	05A8B
TPC13-1N	Time Pulse 1 and 2 and 3	03A7A		
TPC47-1N	Time Pulse 4 and 5 and 6	03A8A		
TS-N	Tape Sense	05B8B		
UTS-1N	Up to Speed		13B8A	13B8A
WCP-N	Write Clock Pulse		13A8A	13A8A
WCP0-N	Write Clocking Pulse 0		13B1A	13B1A
WCP1-N	Write Clocking Pulse 1		13A3A	13A3A
WCP2C-N	Write Clocking Pulse 2C		13A3B	13A3B
WCP2L-P	Write Clocking Pulse 2L		13B2H	13B2H
WE-P	Write Error	17A6C		
WE-1N	Write Error		20B3J	20B3J
WEGC-1N	Write End Guard Character		20C2D	20C2D
WEND-1N	Write End		15D4B	15D4B
WFGC-1N	Write First Guard Character		20C2A	20C2A
WGC-N	Write Guard Character		20C2E	20C2E
WGC-P	Write Guard Character		20B2A	20B2A
WI0 thru 6-N	Write Information Bits		18 Area A	18 Area A

Abbreviation	Name	General Print Element	α Print Element	β Print Element
WLC-0N	Write Last Character		19A7A	19A7A
WNE-N	Write and Not Erase		15B76	15B7C
WP-N	Write Pulse		13B8F	13B8F
WPE-P	Write Parity Error		20A3B	20A3B
WR-1N	Write		15C6A	15C6A
WR-1P	Write		15B7B	15B7B
WR COMM-N	Write Command		15B6A	15B6A
WRDC-1N	Write/Read Data Control		18C8B	18C8B
WSA0 thru 6-P	Write Signals from Bus 0 to "A" Buffer		07 Area C	07 Area C
WSB0 thru 6-P	Write Signals from Bus 1 to "B" Buffer		07 Area C	07 Area C
30KC/S-1N	30KC/S Generator	07A5A		
83.4KC/S-N	83.4KC/S Generator	07B4B		
120KC/S-N	120KC/S Generator	07A4C		
200-1N	200 BPI Mode		16C5A	21C5A
556-N	556 BPI Mode		16C6E	21C6E
800-1N	800 BPI Mode		16C6A	21C6A