



DATA PROCESSING SYSTEM

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*TIME*  
**REFERENCE**  
**MANUAL**



RADIO CORPORATION OF AMERICA

Electronic Data  
Processing,  
Camden 8, N. J.

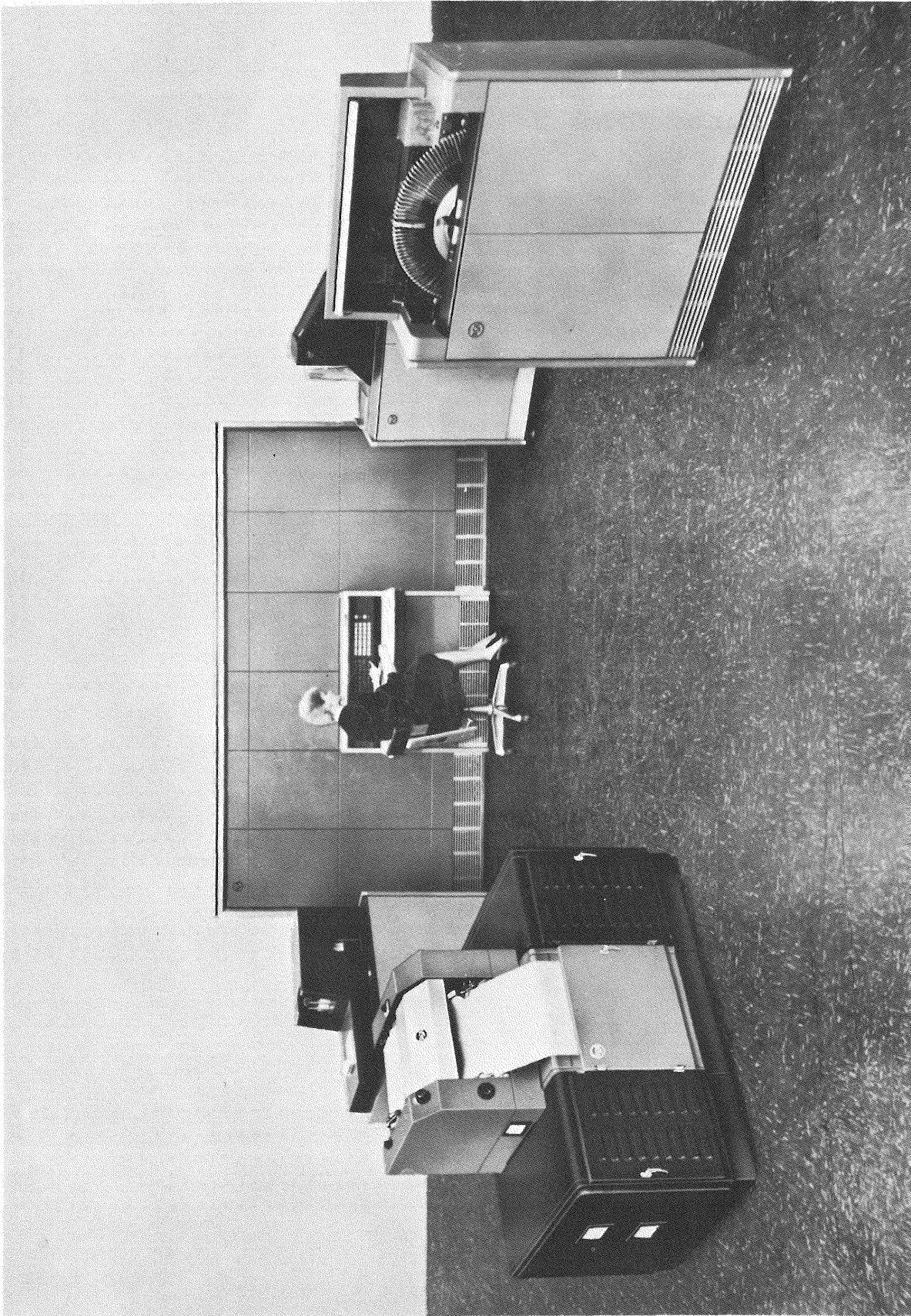
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# CONTENTS

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	<i>Page</i>
<b>THE RCA 301 SYSTEM – GENERAL DESCRIPTION</b>	
Introduction . . . . .	1
System Elements Description . . . . .	1
The RCA 301 Code . . . . .	5
Organization of Data . . . . .	6
<b>PERIPHERAL EQUIPMENT – FUNCTIONAL DESCRIPTION</b>	
Card Equipment . . . . .	10
Paper Tape Equipment . . . . .	10
On-Line Printer . . . . .	11
Monitor Printer . . . . .	12
MICR Sorter-Reader . . . . .	12
Data Record File . . . . .	12
Data Disc File . . . . .	13
Hi-Data Tape Group . . . . .	13
33KC Magnetic Tape Stations . . . . .	14
66KC Magnetic Tape Stations . . . . .	14
<b>THE COMPUTER – FUNCTIONAL DESCRIPTION</b>	
High Speed Memory . . . . .	15
The Basic Instruction . . . . .	15
Program Control . . . . .	17
The Console . . . . .	23
<b>THE RCA 301 INSTRUCTIONS – INTRODUCTION</b>	
Detailed individual instructions are listed on page . . . . .	30
<b>APPENDICES</b>	
I. RCA 301 Codes . . . . .	118
II. List of Instructions . . . . .	120
III. Summary of Instructions . . . . .	122
IV. Instruction Timing . . . . .	138
V. Standard High Speed Memory Locations . . . . .	144
VI-A. Symbols Used for N Character Counts Except in Repeat and Paper Advance Instructions . . . . .	145
VI-B. Symbols Used for N Character Counts in Repeat and Paper Advance Instructions . . . . .	145
VII. Device Identification for Input/Output and IOS Instructions . . . . .	146
VIII. Print Table . . . . .	147
IX. Glossary of Terms . . . . .	148
<b>ILLUSTRATIONS</b>	
<i>Figure #</i>	
1. Recording on Data Disc File . . . . .	8
2. Recording on Magnetic Record . . . . .	8
3. Recording on Hi-Data Tape . . . . .	8
4. Recording on Paper Tape . . . . .	8
5. Block Diagram of Basic RCA 301 Computer . . . . .	18
6. RCA 301 Console Display . . . . .	27



AN RCA 301 ELECTRIC DATA PROCESSING SYSTEM

# THE RCA 301 SYSTEM

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## GENERAL DESCRIPTION

### INTRODUCTION

The RCA 301 Electronic Data Processing System is a general purpose, stored program, digital processor employing solid-state electronic circuitry. Highly flexible RCA 301 Systems are integrated from a diversified array of input/output devices, a range of memory sizes, and other special features. Each System is tailored to meet the data processing requirements of a specific organization. While each RCA 301 System is complete within itself, a high degree of compatibility has been attained with the medium-scale RCA 501 and the large-scale RCA 601.

System efficiency is enhanced by:

- . Rapid memory access time
- . Character addressability providing completely variable data organization
- . Decimally addressed memory
- . Built-in and programmed accuracy controls
- . Machine code covering full range of numerics, alphabets, and special symbols
- . Automatic and programmed storage in High-Speed Memory of the contents of various Program Control Registers
- . Direct and Indirect Addressing
- . A powerful programming instruction repertoire including the following:
  - . A Translate by Table instruction permitting efficient internal processing of various code structures
  - . Locate Symbol instructions permitting an internal search within High-Speed Memory for any character designated
  - . Transfer instructions permitting transfer of data to left or right within High-Speed Memory
  - . Arithmetic instructions permitting Logical "OR", Logical "AND" and Exclusive "OR"
  - . A Repeat instruction permitting the next instruction to be repeated a specified number of times
  - . Automatic programming aids include RCA 301 COBOL, Assembly Systems, and a Scientific Interpreter. An extensive library of service and maintenance routines is also available.

The System processes information prepared by a variety of input media for distribution to the appropriate output. The complete compatibility of System elements provides for ease of expansion at a later date, which is part of the System philosophy.

### SYSTEM ELEMENTS DESCRIPTION

The RCA 301 Computer comprises a Processor and appropriate Input/Output Control Modules. The latter operate the peripheral devices connected in the system. The Processor is a general purpose, stored program, digital machine which includes the following sub-units: High-Speed Memory, Program Control, Console Panel, and Power Supply. The Simultaneous Mode Control may be included in the system to provide concurrent operation of two input/output devices, or an input/output instruction with a compute instruction.

The **High-Speed Memory** is a random access, magnetic core device which provides storage and work area for programs and data. The memory capacity is 10,000, 20,000 or 40,000 alphanumeric characters. Each location is decimally addressable and can store one of the RCA 301 characters. The RCA 301 code includes all the letters of the alphabet, the ten decimal digits, control and special symbols. (Refer to 301 Code Chart, Appendix I). The memory cycle time to address, bring into register, and regenerate a diad in its original memory location is 7 microseconds.

The **Program Control** executes the instructions of the program stored in the High-Speed Memory and performs the automatic accuracy checks. The classes of instructions are : Data Handling, Arithmetic, Decision and Control, and Input Output. Both direct and indirect addressing can be employed.

The **Console Panel** provides for complete monitoring of operation of the Computer. Adequate indicators and controls are provided on the panel to initiate normal computer operation and to facilitate program check-out and maintenance.

The **Power Supply** distributes power to the Processor and to certain Peripheral Equipment which require d-c or regulated a-c power. Other Peripheral Equipment, not requiring d-c or regulated a-c, are supplied from the power mains individually.

The **Simultaneous Mode Control** permits the operation of one input/output device simultaneously with another operation being performed by the Computer. This other operation being performed by the Computer can be a second input-output instruction or a compute instruction.

The **Record File Mode Control** provides an additional degree of simultaneity so that reading from or writing to one of four Data Record Files can be time-shared with other operations.

The **Input/Output Control Modules** control the peripheral equipment, generally one for each device used in a system. The modules are installed only when their associated input/output devices, described in succeeding paragraphs of this section, are added to the system.

The **Card Reader** reads information punched in 80-column cards for transfer through the Card Reader Control to the Processor. Hollerith card code may be automatically translated to RCA 301 code. It is possible, through the use of the Translate Bypass Switch on the Console, to bypass automatic translation and to read cards binarily. Cards are read at the rate of approximately 600 cards per minute. Two card readers can be operated simultaneously at a rate of approximately 1200 cards per minute. Reading and editing is under complete control of the stored program. Two reading stations are provided for automatic accuracy checks.

The **Card Punch** automatically translates RCA 301 characters from memory to 80-column card code and punches the information into cards. Two models of the card punch are available, one with an output rate of 100 cards per minute and one with an output rate of 200 cards per minute. The card punching unit includes an automatic card-handling mechanism, a card-punching station, and a card reading station for automatic accuracy checks. Information is edited and rearranged under program control.

Paper tape input and output is provided by three optional paper tape devices. The **Paper Tape Reader and Punch** is a single unit which permits on-line reading from and writing to either 5- or 7-channel paper tape at a rate of 100 characters per second. The **Paper Tape Reader** is a single unit which permits on-line reading from 5-, 6-, or 7-channel odd or even parity paper tape at either 500 or 1000 characters per second. The **Paper Tape Punch** is a single unit which permits writing to 5 or 7-channel paper tape at 100 characters per second. The accuracy of data read from paper tape is assured by an echo check.

Two models of the **On-Line Printer** are available, one printing 120 characters per line and the other printing 160 characters per line. The 120 characters per line model has a printing rate up to approximately 1000 lines per minute during synchronous printing with the ability to print 47 selected characters and up to approximately 800 lines per minute with the ability to print 64 characters. Two printer units can be operated simultaneously for an effective printing rate of up to approximately 2000 lines per minute. The 160 characters per line model has a rate up to approximately 1070 lines per minute with the ability to print from 47 selected characters and up to approximately 835 lines per minute with the ability to print 64 characters. Two printer units can be operated simultaneously at a rate up to approximately 715 lines per minute each for an effective printing rate of up to approximately 1430 lines per minute. Paper can be advanced at the rate of 150 lines a second on both models of the On-Line Printer, independently of the normal data processing activity. The printer operation, variations in format, and complete editing are under the control of the stored program.

The **Monitor Printer** accepts information from memory and prints it at a rate of up to 10 characters per second. Information is checked for correct parity in the Processor. Operation is under control of the stored program.

The **MICR Sorter/Reader** sorts magnetically encoded documents under control of the stored program. Data is also verified and accumulated for further processing by the Computer. Six-inch documents can be read at a rate of up to 1560 per minute. A separate Reference Manual is available for use in programming this equipment.

The **Data Record File** provides mass storage of over 4.6 million characters per file. Each file contains 128 magnetic records. Each side of a record is divided into two bands with each band containing ten cells. Each cell has a storage capacity of 900 characters. The contents of as many as ten cells can be transferred between High-Speed Memory and the Data Record File, with one instruction, at a transfer rate of 2500 characters per second. As many as six Data Record Files can be used in the system with as many as three of the files being written to or read from simultaneously.

The **Data Disc File** provides rapid random access in modules of 22 million alphanumeric characters up to a total of 176 million. Each module contains 6 magnetic discs. Each side of a disc is divided into 1152 tracks of 10 sectors each. Each sector contains 160 characters. The contents of a complete track, 1600 characters, can be transferred between High-Speed Memory and the Data Disc File, with one instruction, at a transfer rate of 32,000 characters per second.

The **Hi-Data Tape Group** is composed of a cluster of six tape decks with a common set of control, power supply, and switching circuits. Reading is performed in either the forward or reverse direction. Data is recorded in seven channels, with a density of 333 1/3 characters per inch. Tape speed is 30 inches per second. Tape rewind at 90 inches per second is independent of the normal data processing ability. Two Hi-Data Tape Groups may be utilized in a system for a total of 12 tape decks. In this case, two tape decks, one from each group, may be operating simultaneously. A parity check is performed during reading and writing.

**33KC Magnetic Tape Stations** are operated through either 33KC Tape adapters or 33KC Dual Tape Channels. Reading is performed in either the forward or reverse direction. Data is recorded in seven channels with each channel dually recorded. Recording density is 333 1/3 characters per inch. Tape speed is 100 inches per second. Tape rewind is independent of the normal data processing ability. A parity check is performed during reading and writing.

**66KC Magnetic Tape Stations** are operated through either 66KC Tape Adapters or 66KC Dual Tape Channels. Reading is performed in either the forward or reverse direction. Data is recorded in seven channels with each channel dually recorded. Recording density is 666.6 characters per inch. Tape speed is 100 inches per second. Tape rewind at 150 inches per second is independent of the normal data processing ability. A parity check is performed during reading. A read-after-write accuracy check is effected when writing.

**SUMMARY OF PERIPHERAL EQUIPMENT PERFORMANCE**

- Card Reader . . . . . up to approximately 600 cards per minute. Two units can be utilized to operate simultaneously for an effective rate of up to approximately 1200 cards per minute.
- Card Punch . . . . . Approximately 100 cards per minute or approximately 200 cards per minute.
- Paper Tape Reader and Punch . . . . . Reads and punches at approximately 100 characters per second.
- Paper Tape Reader . . . . . Approximately 1000 characters per second with the ability to stop in a position to read a character three sprocket holes from the last character read.  
 . . . . . Approximately 500 characters per second with the ability to stop in a position to read the next character.
- Paper Tape Punch . . . . . 100 characters per second.
- On-Line Printer . . . . . 120 characters per line: up to approximately 1000 lines per minute (47 characters); up to approximately 800 lines per minute (64 characters).  
 . . . . . 160 characters per line: up to approximately 1070 lines per minute (47 characters); up to approximately 835 lines per minute (64 characters).
- Monitor Printer . . . . . Up to 10 characters per second.
- MICR Sorter Reader . . . . . Up to 1,560 documents per minute.
- Data Record File . . . . . Storage of over 4.6 million alphanumeric characters per file. Up to 6 files may be utilized. Transfer rate is 2,500 characters per second.
- Data Disc File . . . . . Storage of over 22 million alphanumeric characters per module. Up to 8 modules may be utilized. Transfer rate is 32,000 characters per second.
- Hi-Data Tape Group (magnetic tape) . . . . . 10,000 characters per second.
- High-Speed Magnetic Tape Stations . . . . . 33,333 and 66,667 characters per second.

## Accuracy Control

Adequate accuracy checking techniques are used in the System to assure correct data processing. Correct parity is ascertained on read-in, during data flow in the Computer, and on write-outs. If a parity error occurs in one of the Computer modes (Normal, Simultaneous or Data Record File) the mode in which the error occurs is stopped immediately. The other modes complete their function.

Accuracy of information from the Card Reader and to the Card Punch is assured by use of two separate reading stations in the Card Reader, and a reading station following the punch unit in the Card Punch. When reading cards in the Translate Mode of operation, any non-RCA 301 Card Code combination (excluding Y/O) is detected, transferred into memory as an octal 57 ( $57_8$ ), and both the Computer and Card Reader halt after the complete card image has been transferred to memory.

A parity check is made of paper tape characters (odd or even input parity) when transferred to the Computer, and an echo check is made of those characters punched into paper tape.

A read error condition (RE) is indicated when the printer table character stored in the control module for scanning the print field has a parity error.

A write error condition (WE) is indicated when either of the characters in the diad sent to the Printer Control module for comparison has a parity error.

A DDF occurs if the device is inoperable or a page change (PC) is required with a low paper supply.

The Data Record File possesses a lock-out feature to prevent writing on a "master" record. An accuracy check also warns of malfunctioning Block or Character Counter.

The Data Disc File checks if the positioner is in the correct track, and it has a bit counter to assure that the bit serial to character serial conversion is functioning properly.

Magnetic Tape accuracy features include end of reel stops, both beginning of tape and end of tape warning, dual recording, write lockouts, correct parity of data read and read after write accuracy check.

## Application of Accuracy Checking Techniques

*Program Control* - The following controls are typical of conditions causing the computer to stop:

1. Incorrect parity in Memory Address Register.
2. Incorrect parity in Memory Register.
3. Incorrect parity in Operation Register.
4. Incorrect parity in N Register.
5. Incorrect parity in Repeat ( $N_r$ ) Register.

*Input-Output* - The following are input/output conditions which may cause the Computer to stop:

1. Incorrect parity of data being transferred.
2. Input-Output device inoperable or not following command.
3. Record not on turntable of Data Record File.
4. Attempting to write to record or magnetic tape when lockout device applied.
5. Card equipment input hopper empty or output hopper full.
6. Non-RCA 301 card character read by the Card Reader, when BCT button on Computer Console not depressed.
7. Tape Station reading extra bits in interblock gap.
8. On-Line Printer paper supply low.

## THE RCA 301 CODE

The RCA 301 System employs a binary code using seven binary digits, or bits to represent each RCA 301 character. Of the seven bits which make up each of the characters, the highest order bit ( $2^6$ ) is the parity bit. The remaining six bits are the information bits, with a specific configuration of bits representing each RCA 301 character.

Bit Position	P	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$
Bits	X	X	X	X	X	X	X

(X = 0 or 1)

For ease in presentation, the bit configurations of the RCA 301 Code are divided into four groups with the zone bits ( $2^5$  and  $2^4$ ) designating the group, as follows:

### RCA 301 GROUP CODE

	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$
Group I	0	0	X	X	X	X
Group II	0	1	X	X	X	X
Group III	1	0	X	X	X	X
Group IV	1	1	X	X	X	X

The following table shows the bit configuration for each RCA 301 character. The parity bit ( $2^6$ ) is not shown in this table but is inserted in each configuration to indicate an odd parity count.

### RCA 301 CODE

Group I	Group II		Group III		Group IV		$2^3$	$2^2$	$2^1$	$2^0$
$2^5$ $2^4$	$2^5$	$2^4$	$2^5$	$2^4$	$2^5$	$2^4$				
0 0	0	1	1	0	1	1				
0	&		- (minus)		"		0	0	0	0
1	A		J		/		0	0	0	1
2	B		K		S		0	0	1	0
3	C		L		T		0	0	1	1
4	D		M		U		0	1	0	0
5	E		N		V		0	1	0	1
6	F		O		W		0	1	1	0
7	G		P		X		0	1	1	1
8	H		Q		Y		1	0	0	0
9	I		R		Z		1	0	0	1
(space)	+		EI		EB		1	0	1	0
#	. (period)		\$		, (comma)		1	0	1	1
@	;		*		%		1	1	0	0
(	:		ED		● (ISS)		1	1	0	1
)	' (apostrophe)		EF		=		1	1	1	0

On 80 column cards, the groups are designated by the presence or absence of zone punches. Group I has no zone punch. Group II has a Y zone punch, Group III has an X zone punch, and Group IV has a O zone punch.

RCA 301 programs are written using alphanumeric characters. Memory Locations are addressed as follows:

Memory Locations	Addresses
0000 to 9999	0000 to 9999
10000 to 10999	&000 to &999
11000 to 11999	A000 to A999
12000 to 12999	B000 to B999
13000 to 13999	C000 to C999
14000 to 14999	D000 to D999
15000 to 15999	E999 to E999
16000 to 16999	F000 to F999
17000 to 17999	G000 to G999
18000 to 18999	H000 to H999
19000 to 19999	I000 to I999
20000 to 20999	-000 to -999
	(minus) (minus)
21000 to 21999	J000 to J999
22000 to 22999	K000 to K999
23000 to 23999	L000 to L999
24000 to 24999	M000 to M999
25000 to 25999	N000 to N999
26000 to 26999	O000 to O999
27000 to 27999	P000 to P999
28000 to 28999	Q000 to Q999
29000 to 29999	R000 to R999
30000 to 30999	''000 to ''999
31000 to 31999	/000 to /999
32000 to 32999	S000 to S999
33000 to 33999	T000 to T999
34000 to 34999	U000 to U999
35000 to 35999	V000 to V999
36000 to 36999	W000 to W999
37000 to 37999	X000 to X999
38000 to 38999	Y000 to Y999
39000 to 39999	Z000 to Z999

## ORGANIZATION OF DATA

### Definitions

*Bit:* A bit is a single binary digit, having a value of either zero or one.

*Character:* An RCA 301 character consists of six information bits and one parity bit combined to represent a decimal digit, a letter of the alphabet, a punctuation or other special mark, or a control symbol.

*Item:* An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.) In many cases an item is preceded by a symbol to define the beginning of each item.

*Record:* A record consists of one or more related items with the amount of information in a record being completely variable.

*Line:* A line is composed of the characters that are to be printed on a single line on the On-Line Printer. One model of the On-Line Printer permits 120 characters to be printed per line. A second model permits 160 characters to be printed per line.

*Block:* On magnetic and paper tape a block is a group of at least three characters preceded and followed by a blank space called an "interblock gap."

On the Data Record File record a block is defined as the information contained in one cell. From one through 900 characters of information may be recorded in a cell. If the block is composed of less than 900 characters, the last character will be an EB symbol (End of Block). If the block is composed of 900 characters, the last character may or may not be an EB symbol. On the Data Disc File disc a block is defined as the information contained in 1 to 10 sectors. Each sector contains 160 characters.

*File:* A file consists of any number of related information records and may consist of only a part of a Data Record File record or Data Disc File disc, or several records or discs. On magnetic tape it may consist of several tapes or any part of one tape.

### **Organization of Data on Paper Tape**

In the RCA 301 system, characters are represented on paper tape by combinations of holes punched in rows across the tape. A hole represents a zero bit; the absence of a hole represents a one bit. (See Figure 4)

### **Organization of Data on Data Record File**

Bits are recorded as magnetic spots on the face of each Data Record File record. Characters are written and read out in bit-serial fashion, the seven bits of each character following each other in a spiral around the disc, as shown in Figure 2.

Each side of the record is divided into two bands; each band is composed of ten cells; each cell has the capacity to store 900 characters. The cells on a record are addressable individually or in groups of consecutive cells up to a total of 10.

### **Organization of Data on Data Disc File**

Bits are recorded as magnetic spots on the face of each Data Disc File disc. Characters are written and read out in bit-serial fashion. The seven bits of each character following each other in concentric tracks around the discs as shown in Figure 1.

Each side of the disc is divided into nine zones of 128 tracks each. Each track contains 10 sectors of 160 characters each. The sectors are addressable individually or in groups of consecutive sectors up to a total of 10.

### **Organization of Data on Magnetic Tape**

In the RCA 301 system, characters are recorded on magnetic tape as magnetic spots in rows across the tape. On Hi-Data Tape, a magnetized spot represents a zero bit; the absence of a spot represents a one bit. All characters are recorded on tape serially so that the characters making up an item follow one another in sequence from most to least significant. Minimum interblock gaps on Hi-Data tape are approximately .34 inch (see Figure 3). All data on 33 KC and 66 KC magnetic tape is dually recorded. Minimum interblock gaps on 33 KC tape and 66 KC tape are approximately .4 inches and .55 inches, respectively.

### **Variable Item and Record Length**

Data storage in the RCA 301 system incorporates true variable item length. This concept may be more fully appreciated if prefaced with a definition of fixed and fixed variable word and block lengths.

"Word" is generally defined as a fixed number of consecutive characters or character locations, and "block" as a fixed number of consecutive words. These terms, word and block, are more aptly used with respect to fixed and fixed variable systems.

In a computer system using fixed word length, the number of characters for each word, or the number of words for each block, cannot be changed. In order to store data of a varying nature, redundant zeros or spaces are used to fill out the incomplete words, with uneconomical use of space.

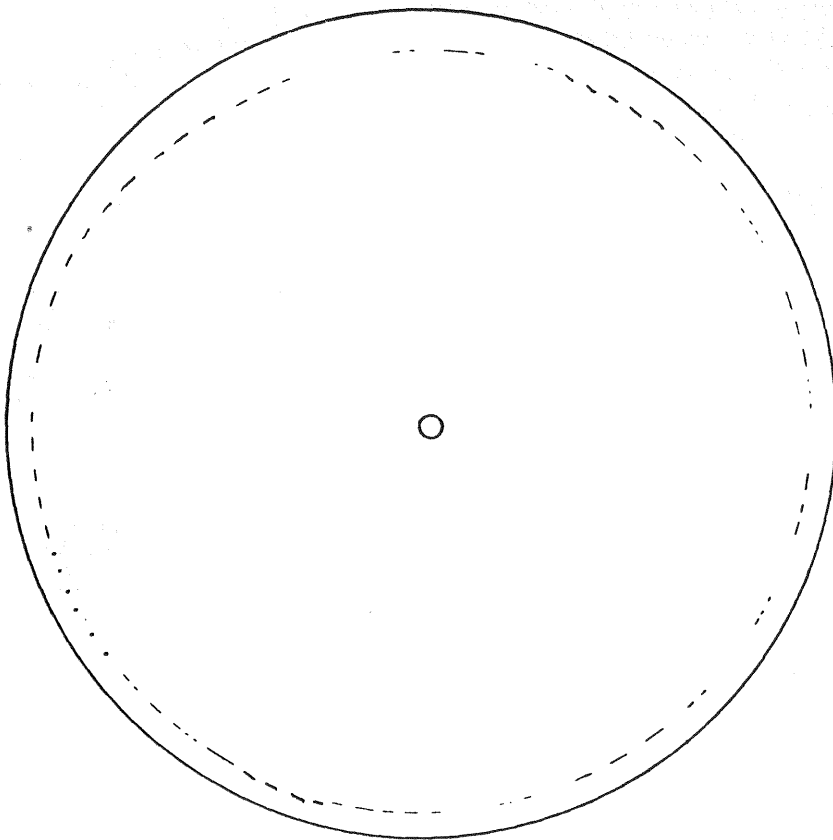


Figure 1—Recording on Magnetic Disc

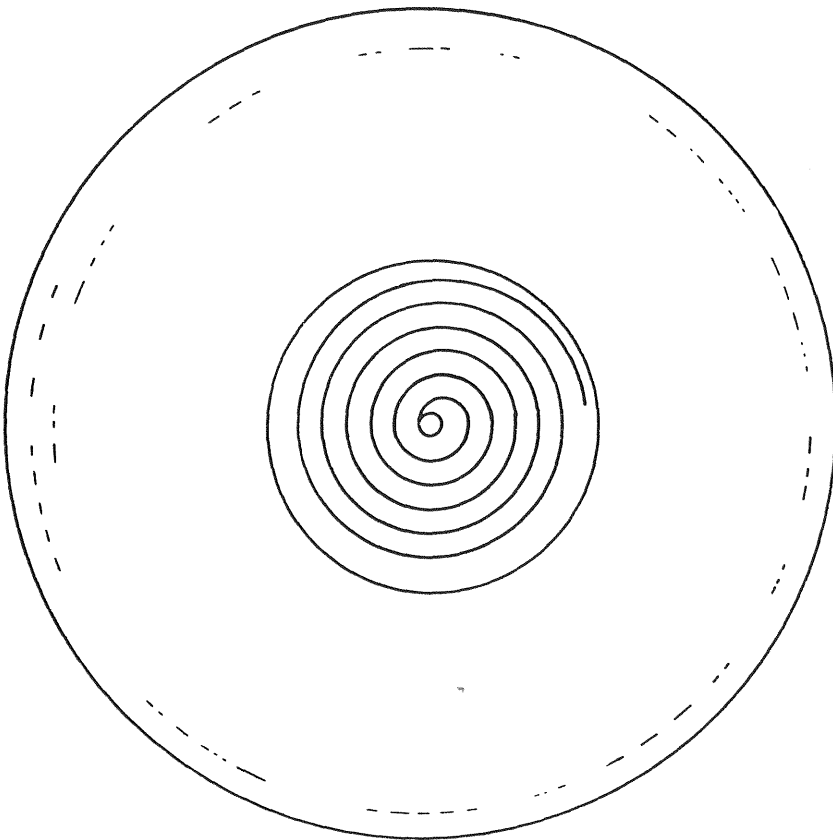


Figure 2—Recording on Magnetic Record

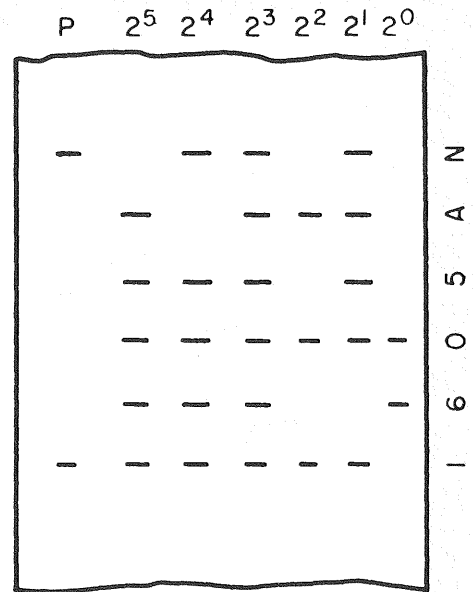


Figure 3—Recording on Hi-Data Tape

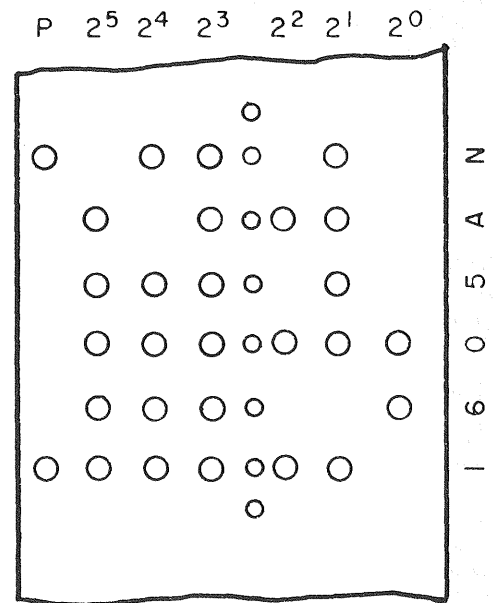


Figure 4—Recording on Paper Tape

In a fixed variable system, the number of character positions for each item in a record is assigned in accordance with the anticipated maximum length for that item. These lengths may be individually predetermined for each file, but remain constant for each item within the file. Fixed variable word length does provide greater flexibility than does fixed word length.

Data storage in a true variable length system does not have the limitations imposed by fixed or fixed variable systems. In the RCA 301, the use of control symbols and the ability to address each character location individually permits the length of any item in any record to be in strict accordance with that item's actual character count. This allows for total variability of item and record length but does not preclude the use of fixed or fixed variable lengths when the programmer finds this expedient.

In each of these categories – fixed, fixed variable, and variable, the method of internal storage is extended to the external storage. Therefore, if redundant zeros of the fixed and fixed variable systems are used in the computer, they would also appear on magnetic tape or other storage devices. By utilization of true variable length in the RCA 301 system, a characteristic business file requires less space in the Record File and less tape footage, and can be read and written out in less time than a fixed or fixed variable system would permit.

# PERIPHERAL EQUIPMENT

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## FUNCTIONAL DESCRIPTION

### CARD EQUIPMENT

The Card equipment includes a Card Reader and two models of Card Punches.

The Card Reader will either: 1. automatically convert 80-column Hollerith card code to RCA 301 characters for transfer to the HSM or 2. read a punch card image into HSM binary where it can be processed, in any desired manner, under program control. The Card Reader reads by row at a rate up to approximately 600 cards per minute with 20 milliseconds of free computing time between cards. Two Card Readers can be employed in a system, and operating simultaneously, they can read at an effective rate of up to approximately 1,200 cards per minute. The Card Reader can be instructed to maintain a 300 card-per-minute rate, resulting in 120 milliseconds of free computing time between cards.

The Card Reader feed hopper can hold up to 2,000 cards. Two card reading stations within the Card Reader provide an automatic hole count check. Capacity of the reject stacker is approximately 100 cards. Cards may be loaded and unloaded for continuous operation. The Card Reader has facilities for sensing empty input hopper, full output stacker, full reject stacker and card jams, and will stop the computer if any of these conditions exist.

One model Card Punch punches by row at a rate of 100 cards per minute. The input and output hoppers have a capacity of approximately 800 cards each. The cards are read after punching to permit an accuracy check of the punched data. The punch stops upon sensing an empty input or full output hopper.

The second model Card Punch punches by row at a rate of 200 cards per minute. The input and output hoppers have a capacity of approximately 2,000 cards each. The capacity of the reject stacker is approximately 100 cards. Cards may be loaded or unloaded for continuous machine operation.

### PAPER TAPE EQUIPMENT

The paper tape equipment includes the Paper Tape Reader/Punch, the Paper Tape Reader, and the Paper Tape Punch.

The Paper Tape Reader/Punch are mounted on the same base. The Reader and the Punch both operate at a rate of 100 characters per second. The unit writes to or reads from 5-channel or 7-channel paper tape. Gapless tape can be read. The seven channels across the width of the tape correspond to the seven bit positions (six information and a parity bit) of an RCA 301 character. When a character position on paper tape contains a punch in all seven channels, it is interpreted as "delete character", it is not an RCA 301 character and no attempt is made to read it into the Computer. When 5-channel tape is being read, the  $2^5$  position is interpreted as a zero bit and correct parity is placed in the  $2^6$  position to result in a 7-bit character being placed in HSM. When punching 5-channel tape, the  $2^6$  and the  $2^5$  bits of each character are stripped off after the character is called from HSM resulting in a 5-bit character being punched on tape. Both reading and punching can progress simultaneously if the System has a Simultaneous Control Unit. Parity is checked on all information read and on all information received at the Punch. Packing density is 10 characters per inch. Tape speed is approximately 10 inches per second. The Reader stops on a character and in a position ready to read the next character. The Stop-Start Distance of the punch is 0.3 inch, or 3 sprocket holes, from the last character punched.

The Paper Tape Reader reads 5, 6, or 7-level paper tape at speeds of approximately 500 or 1,000 characters per second. When 5 or 6-level tapes are read, additional bits are added in the most significant bit locations to produce 7-level characters of correct parity to be stored in HSM. At the 500 characters per second rate, the Reader stops on a character and in a position to read the next character. At the 1,000 characters per second rate, the Reader stops in a position to read a character at a maximum of 0.3 inch (three sprocket holes) from the last character read. Packing density on tape is 10 characters per inch, and tape moves at 50 or 100 inches per second. An adjustable guide is provided to handle tape in widths from 11/16 inch to one inch. Unwind and take-up reels may be used for reading tape lengths up to 1,000 feet. All Characters are checked for correct parity.

The Paper Tape Punch punches 5, or 7-level paper tape at speeds of approximately 100 characters per second. When 5-level tape is punched, the two most significant bits of each 7-bit character received from HSM are ignored resulting in a 5-bit character to be punched. The Punch stops in a position to punch a character a maximum of 0.3 inch (three sprocket holes) from the last character punched. Packing density on tape is 10 characters per inch, and tape moves at approximately 10 inches per second. All information received at the Punch is checked for parity.

## ON-LINE PRINTER

Two versions of the On-Line Printer are available in the RCA 301 System. The important differences between the two are 1.) the number of characters that can be printed per line, and 2.) the number of lines that can be printed per minute.

One model prints a maximum of 120 characters per line. The printing rate is up to approximately 1000 lines per minute in the Synchronous Mode which permits the printing of 47 selected characters. The printing rate is up to approximately 800 lines per minute in the Asynchronous Mode which permits the printing of 64 characters.

The second model prints a maximum of 160 characters per line. The printing rate is up to approximately 1070 lines per minute in the Synchronous Mode and up to approximately 835 lines per minute in the Asynchronous Mode.

The two printers can be operated in the following combinations at the indicated speeds:

No. of Printers	Model	Synchronous speed (lpm)	Asynchronous speed (lpm)	Normal Mode (N) or Simultaneous Mode (S)
1	120 Column	1,000	800	N or S
1	160 Column	1,070*	835*	N
1	160 Column	715	600	N or S
2	120 Column #1	1,000	800	N or S
	#2	1,000	800	N or S
2	160 Column #1	715	600	N or S
	#2	715	600	N or S

\* If a card read or punch operation is performed in the "S" Mode concurrently with a print instruction in the "N" Mode the rates are reduced to 715 and 600 l.p.m. respectively.

The following characteristics are common to both printers:

The Printer is a transistorized device which prepares output documents, printing data directly from the High Speed Memory of the Computer. Data editing is accomplished in the Computer under the direction of the stored program. Paper advance is controlled by the Computer program, either directly or through a paper tape loop in the Printer. Paper advance is independent of the Computer activity at a rate of 150 lines a second.

Two Computer instructions are directly associated with the On-Line Printer. One controls the On-Line Printer in the Normal Mode, the other in the Simultaneous Mode. Variations in these basic instructions permit printing, paper advance for a specified number of lines, vertical tabbing, or page change. Certain combinations of these functions are also possible with these instructions.

Ten characters are printed per horizontal inch and six lines per vertical inch.

Paper stock may be single or multiple sheet fanfold, from 4 to 19 inches in width and up to 17 inches in sheet length, provided length is a multiple of the standard sprocket distance of 1/2 inch. One original, plus 5 carbon copies (10-12 pound paper and 7-9 pound carbon) may be used. Hechto and multilith master stock may also be used.

In the Synchronous Mode, the Printer will print 26 letters of the English alphabet, the numerals (0 to 9), and the following 11 punctuation marks and symbols for a total of 47 available characters.

CR	credit	/	virgule	(SP)	space
'	apostrophe	⌘	lozenge	,	comma
*	asterisk	-	minus	.	period
&	ampersand	+	plus		

An automatic accuracy control prevents the tape from running off the feed reel. A write lockout prevents writing of information except on specifically designated reels of magnetic tape. Parity is checked on the information delivered to the write-head and on the tape station address received from the computer. Parity is also checked on information read.

### **33 KC MAGNETIC TAPE STATIONS**

The 33 KC magnetic tape station is used for reading and writing binary coded characters on 3/4 inch magnetic tape at a rate of 33,333 characters per second. Data is recorded at a density of 333 1/3 characters per inch. The tape speed is 100 inches per second, forward or reverse. Reading is possible in the forward or reverse direction; writing is performed in the forward direction. All characters are dually recorded on tape, and parity is checked on all data read or written. The tape station is designed to facilitate manual interchange of tape reels, which can be accomplished in less than one minute.

The gap between blocks is a minimum of 0.4 inches. Tape-start time is a minimum of 3.5 milliseconds.

33 KC Tape Stations may be operated in the system through Tape Adapters, Dual Tape Channels or a combination of both. The Tape Adapter connects a single Tape Station to the Computer. Two models of the Dual Tape Channel (2 x 6 switch or 2 x 12 switch) are available which operate up to six, and up to 12 Tape Stations, respectively. One 33 KC Dual Tape Channel and up to two 33 KC Tape Adapters may be connected to the Computer for operation of up to 14 Tape Stations. When the Computer is equipped with the Simultaneous Mode Control two Tape Stations can be operated concurrently.

### **66 KC MAGNETIC TAPE STATION**

The 66 KC Magnetic Tape Station is used for reading and writing binary coded characters on 3/4 inch magnetic tape at a rate up to 66,667 characters per second. Data is recorded at a density of 667 characters per inch nominally. The tape speed for reading and writing is 100 inches per second. Tape rewind speed is 150 inches per second. Reading is possible in the forward or reverse direction; writing (and erasing) are performed in the forward direction. All characters are dually recorded on tape, and each character is read and checked for parity after it is written. There is also a parity check on all characters read. The Tape Station is designed to facilitate manual interchange of tape reels, which can be accomplished in less than one minute.

The gap between blocks is nominally 0.55 inch. Tape-start time is approximately 3.5 milliseconds.

66 KC Tape Stations may be operated in the system through Tape Adapters, Dual Tape Channels, or a combination of both. The Tape Adapter connects a single Tape Station to the Computer. Two models of the Dual Tape Channel (2 x 6 switch or 2 x 12 switch) are available which operate up to six, and up to 12 Tape Stations, respectively. One 66 KC Dual Tape Channel and up to two 66 KC Tape Adapters may be connected to the Computer for operation of up to 14 Tape Stations. When the Computer is equipped with the Simultaneous Mode Control two Tape Stations can be operated concurrently.

# THE COMPUTER

## FUNCTIONAL DESCRIPTION

### HIGH SPEED MEMORY

The High-Speed Memory (HSM) in the RCA 301 System consists of 10,000, 20,000 or 40,000 characters. Each 10,000 characters consists of fourteen 50 x 100 matrices of magnetic cores. As each core represents one bit, a matrix of cores represents 5,000 bits and a memory unit represents 70,000 bits. As each 301 character is made up of seven bits, each memory unit can store 10,000 characters in 10,000 individual character locations.

Each location in memory has a unique address, consisting of four RCA 301 characters. Though oversimplified, the HSM may be pictured as a rectangular array of locations, with the smallest address in the upper left-hand corner and the largest address in the lower right-hand corner. The lowest address in the HSM is always 0000. The highest address in a system with a 10,000 character memory is 9999. In the case of a 20,000 character memory the second 10,000 characters are addressed from &000 to I999. In the case of a 40,000 character memory, the third 10,000 characters are addressed from -000 to R999, and the fourth 10,000 characters are addressed from /000 to Z999. If an address greater than the processor's maximum memory location is specified, a Memory Register Parity Error alarm will occur and stop the Computer.

The HSM is constructed so that two characters (14 bits) in consecutive memory locations are accessed in a single memory cycle. The computer cycle is 7 microseconds; this means that characters may be addressed, brought into the memory register, and regenerated in their original locations every 7 microseconds. Each of these groups of two locations, or the contents thereof, is called a "diad". Each diad begins with an "even" decimal address, and ends with the next consecutive "odd" address (such as the diad with addresses 1134 to 1135). Diagrammatic representations of portions of the HSM used throughout this manual are shown below.

5234	5235	5236	5237	5238	5239
D	E	F	G	2	J

The HSM address of each location is shown in the upper portion of the diagram, with the characters stored in each location shown in the lower portion.

The primary purpose of the HSM is the storage of programs and data. These may be stored in any area of the memory except for those locations reserved as Standard HSM Locations (see Appendix V).

### THE BASIC INSTRUCTION

#### Instruction Format

Each of the RCA 301 instructions consists of four parts:

1. Operation Code (one character)
2. N Character (one character)
3. A Address (four characters)
4. B Address (four characters)

An instruction, then, is made up of ten RCA 301 characters with the format:

O	N	AAAA	BBBB
Operation Code	N Character	A Address	B Address

In most cases, the entire A address refers to a HSM location, and the entire B address refers to another HSM location. In some instructions, however, only a portion of the A address or B address is used, or one part of the address may designate one value and the other part another value. The components of the A address are referred to as  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$ , and the components of the B address as  $B_0$ ,  $B_1$ ,  $B_2$ ,  $B_3$ .

In instructions where the N character is used as a count, the number of the count may be from 0 to 44. As the N character can only contain one character, the following symbols are used to designate the N character for counts from 0 to 44:

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	11	A	22	K	33	T
1	1	12	B	23	L	34	U
2	2	13	C	24	M	35	V
3	3	14	D	25	N	36	W
4	4	15	E	26	O	37	X
5	5	16	F	27	P	38	Y
6	6	17	G	28	Q	39	Z
7	7	18	H	29	R	40	EB
8	8	19	I	30	”	41	, (comma)
9	9	20	- (minus)	31	/	42	%
10	&	21	J	32	S	43	o (ISS)
						44	=

### Storage of Instructions

Instructions are stored sequentially in the High Speed Memory. Each instruction is stored in ten consecutive memory locations (5 diads) so that the Operation Code is placed in the first character of a diad.

### Staticizing

An instruction can be interpreted and executed by Program Control only after it has been brought out of the High Speed Memory locations in which it has been stored, and its components placed in the proper registers. This process is called “staticizing” and is accomplished in five status levels.

A status level lasts for seven microseconds and is a term applied to a series of pulses which open certain paths over which information can travel. Each status level has a specific function. In staticizing each instruction, the first status level brings the first diad (two characters) of the ten character instruction (ONAAAABBBB) into the Memory Register and automatically regenerates the characters in their original location in the HSM.

The O character is then sent to the NOR Register, and the N is sent to the N Register. This completes the first status level. The second status level brings the next diad ( $A_2, A_1$ ) into the memory register, regenerates the characters, and sends the  $A_0, A_1$  characters to the A Register. During the third status level the  $A_2, A_3$  characters are transferred in a similar manner, and the fourth and fifth status levels transfer  $B_0, B_1$  and  $B_2, B_3$  to the B Address Register.

The total staticizing time is 35 microseconds, and is constant for every instruction, even when the N count is zero. The number of status levels involved, and their sequence for execution (after staticizing) of a given instruction, depends upon what must be accomplished by that instruction.

### Direct and Indirect Addressing

When the least significant character of an address is written as a number, i.e., the zone bits are 00, the address is a direct address. Direct addresses establish the initial register settings for instructions in which they are employed.

When the least significant character of an address has zone bits 01, thus forming one of the following characters:

- |         |         |
|---------|---------|
| & for 0 | E for 5 |
| A for 1 | F for 6 |
| B for 2 | G for 7 |
| C for 3 | H for 8 |
| D for 4 | I for 9 |

the address is an indirect address. When an indirect address is staticized, the contents of the HSM location addressed by that indirect address replace it in the register. If the replacing address is also an indirect address, it too will be replaced in the register by the contents of the memory locations it addresses. The initial register settings for any instruction, are therefore, not established until both the A and B registers have been supplied with direct addresses. An indirect address must address the least significant diad of another address. Indirect addressing has proven valuable in reducing programmer effort, processing time, and instruction storage. Each indirect address requires two additional status levels (14 microseconds).

## PROGRAM CONTROL

Program Control is the control unit of the system. It interprets and executes the instructions stored in the High Speed Memory, directs the sequence of operations within the system, controls operation of the input-output devices, and performs automatic accuracy checks.

Program Control includes a number of specialized devices. Those which are of interest to the programmer are diagrammed in Figure 5, and are briefly discussed below, along with certain automatic Program Control functions.

### Registers

The *Memory Addressing Register* stores the address of the HSM location to be processed. The capacity of this register is four RCA 301 characters.

The *Memory Register* has a capacity of two RCA 301 characters. It receives the diad contents that emerge from or are to be placed in the HSM. A Series of Memory Output Gates permit or inhibit entrance into the Memory Register of either or both of the characters that emerge from the HSM.

The *Interchange* links the Memory Register with the Memory Address Bus. It selects the proper bus or busses to which characters are transferred from the Memory Register according to the operation being performed. For example, during staticizing operations, it selects the proper busses for the transfer of two instruction characters (diad) at a time into the proper registers. During an Input-output operation, it selects the correct bus for single character transfer of information into and out of the HSM.

The *A Register* has a capacity of four RCA 301 characters. It receives the A address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The *B Register* has a capacity of four RCA 301 characters. It receives the B address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The *P Register* has a capacity of four characters and holds the HSM address of the next instruction in sequence.

The *NOR (Normal Operation) Register* has a capacity of one RCA 301 Character. It holds the Operation code of the instruction currently being executed in the Normal Mode.

The *N Register* has a capacity of one character. It holds the N character of the currently processed instruction.

The *N<sub>R</sub> (Repeat) Register* is used by the Repeat instruction to store the count.

When an operation is executed in the Simultaneous Mode, four Registers are utilized:

- Simultaneous Operation Register (SOR) (receives OP Code)
- M Register (receives N character)
- S Register (receives A address)
- T Register (receives B address)

These registers assume the function of the NOR, N, A and B Registers respectively.

If an operation is executed in the Record File Mode, the following registers are utilized:

- Record File Operation Register (FOR) (receives OP Code)
- L Register (receives N character)
- U Register (receives A address)
- V Register (receives B address)

These registers also assume the function of the NOR, N, A, and B Registers.

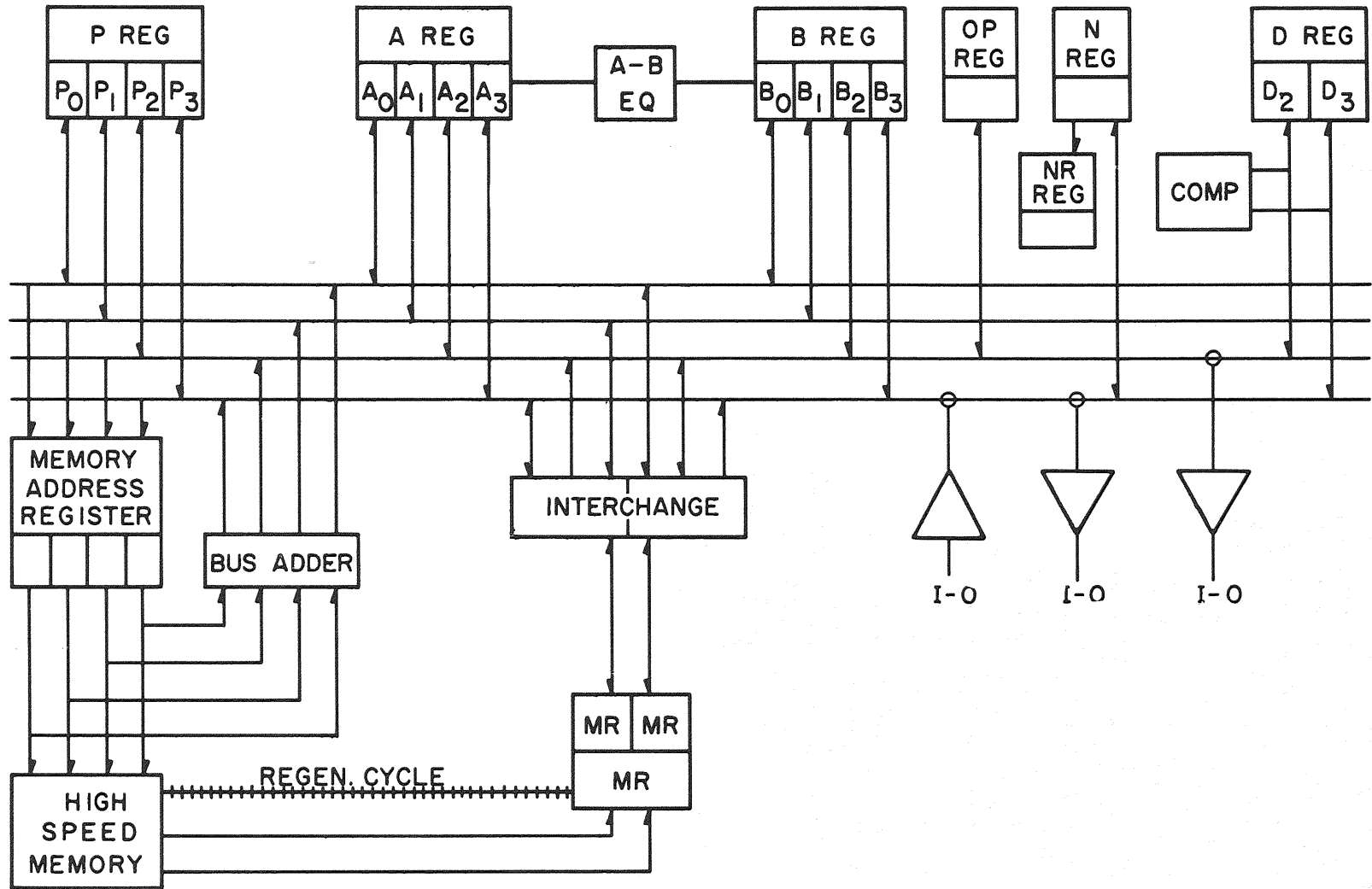


Figure 5—Block Diagram of Basic RCA 301 Computer

The *D Register* has a capacity of two RCA 301 Characters. Comparisons and arithmetic instructions utilize this register.

The *Bus Adder* is used to modify the contents of the various address registers. The Bus Adder can increment or decrement the contents of these registers by either 1 or 2, or leave them unchanged, thus permitting register contents to be directly related to the currently processed characters or diads.

The *A-B Equality Circuit* is located between the A and B Registers and is used to compare their contents. When they are equal, a flip-flop is set indicating to the Computer that the instruction-defined sector has been processed and the instruction can be terminated. In instructions that specify the left and right boundaries of the HSM sector to be processed, the contents of the A Register are always increased toward A-B equality and the contents of the B Register remain unchanged.

The *Memory Address Bus* is a four character pathway between the Interchange, Computer Registers, and Input-Output buffers. The particular pathways used are determined primarily by the Interchange.

The *Previous Result Indicators*, or PRI's are a set of flip-flops which preserve the sign of the result (or the zero result) of an arithmetic operation for automatic reference by a subsequent decision instruction. If the result is positive, the Previous Result Positive (PRP) flip-flop is set; if negative, the Previous Result Negative (PRN) flip-flop is set; if zero, the Previous Result Zero (PRZ) flip-flop is set. The PRI's are set in most of the arithmetic and logical instructions, and in certain search and transfer operations.

The PRI's may be sensed by use of the Conditional Transfer of Control Instruction.

### **Arithmetic Functions**

The arithmetic function of addition and subtraction in the RCA 301 System is performed by the use of arithmetic tables permanently stored in the High Speed Memory (Standard Memory Locations 0000-0199). These locations can be written into only if a special button on the console is depressed, thereby preventing the accidental destruction of these tables. The add and subtract instructions perform arithmetic operations utilizing a table lookup technique where the arguments are the specified operands.

### **Automatic Storage of Final Contents of the A Register (STA)**

STA is an automatic operation which occurs at the conclusion of selected RCA 301 instructions. In STA, the final contents of the A Register are automatically stored in the High Speed Memory locations 0212-0215. This permits the subsequent use of the final A Register contents. It is also a highly convenient programming technique which can be utilized to eliminate memory searching time.

STA is performed in the following list of instructions:

- Locate Symbol Left
- Locate Symbol Right
- Transfer Data by Symbol Left
- Transfer Data by Symbol Right
- Tape Read Forward Normal
- Tape Read Reverse Normal
- Block Read Record Normal
- Sector Read Disc Normal

To preserve the final A Register contents of all other instructions, the Store Register instruction can be used.

### **Automatic Storage of Contents of P Register (STP)**

STP is an operation which occurs whenever control is to be transferred; that is, whenever the next instruction to be performed is not the one stored immediately following the current instruction. STP automatically stores the contents of the P Register in standard High Speed Memory locations 0216-0219. The stored address is the address of the instruction that would have been executed if the transfer of control had not taken place. STP is performed in the following instructions, but only when control is actually transferred:

Condition Transfer of Control

Tally

Input-Output Sense

### Repeat Instruction

The Repeat Instruction (RPT) will cause the next one of the following instructions to be performed to be repeated a specified number of times:

Tape Read Forward Normal

Tape Read Reverse Normal

Add

Transfer Data Left

Transfer Data Right

Subtract

Translate by Table

Transfer Data by Symbol Left

Transfer Data by Symbol Right

Logical "OR"

Exclusive "OR"

Logical "AND"

The number of times a repeatable instruction following an RPT is to be repeated is specified in the N character of the RPT. If the N character of the RPT is zero, the instruction will be executed but not repeated. If the N character of the RPT is one, then the instruction will be performed twice. For proper operation the RPT instruction must be followed immediately by a repeatable instruction. Each repeatable instruction, when repeated, requires three additional status levels (21 microseconds) when the contents of the  $N_R$  (Repeat) Register exceed zero, and requires one additional status level (7 microseconds) when the contents of the  $N_R$  (Repeat) Register equal zero.

### Simultaneity in the RCA 301 System

Simultaneity in the RCA 301 Computer is defined as the coincident execution of two or three instructions. Simultaneity is accomplished through the optional control units: the Simultaneous Mode Control Unit and the Record File Mode Control Unit. When an instruction utilizes the circuitry of the Simultaneous Mode Control Unit it is progressing in the "Simultaneous Mode". When an instruction utilizes the circuitry of the Record File Mode Control Unit it is progressing in the "Record File Mode". When an instruction utilizes the Program Control circuitry of the basic computer it is progressing in the "Normal Mode".

Each of the RCA 301 instructions are designed to operate in one of the three modes. Those instructions designed to operate in the Normal Mode will operate in that mode only. If a button, called SMDI (Simultaneous Mode Inhibit), on the Console Panel is not on, those instructions designed to operate in the Simultaneous Mode will operate in that Mode only. If, however, SMDI is on, simultaneous instructions will operate in the Normal Mode as if they were Normal instructions and the Store S Register instruction will store the contents of the A Register in STA locations. Those instructions designed to operate in the Record File Mode will operate in that mode only.

### Operation of the Simultaneous Mode

The following instructions are designed to operate in the Simultaneous Mode:

Card Read Simultaneous

Card Punch Simultaneous

Tape Read Forward Simultaneous

Tape Read Reverse Simultaneous

Tape Write Simultaneous  
Print and Paper Advance Simultaneous  
Block Read Record Simultaneous  
Block Write Record Simultaneous  
Sector Read Disc Simultaneous  
Sector Write Disc Simultaneous

All instructions in the RCA 301 System are staticized in the Normal Mode. When any one of the above instructions are staticized, if:

1. SMDI is not on,
2. The system is equipped with a Simultaneous Mode Control Unit,
3. The Simultaneous Mode Control Unit is free; i.e., some other instruction is not now progressing in the Simultaneous Mode,

then the simultaneous instruction is transferred to the Simultaneous Mode; i.e., the contents of the NOR Register are transferred to SOR, the contents of the N Register are transferred to the M Register, the contents of the A Register are transferred to the S Register and the contents of the B Register are transferred to the T Register. The instruction is then executed in the Simultaneous Mode with SOR, M, S and T Registers acting as the NOR, N, A and B Registers respectively. The instruction is then processed similarly to a normal instruction. Immediately upon the transfer of an instruction from the Normal to the Simultaneous Mode, the Normal Mode is free to accept the next instruction.

If a simultaneous instruction is staticized and SMDI is on, the instruction is not transferred to the Simultaneous Mode, but is executed in the Normal Mode.

If a simultaneous instruction is staticized and SMDI is not on, but the system is not equipped with a Simultaneous Mode Control Unit, the instruction will be skipped.

If a simultaneous instruction is staticized and SMDI is not on, but the Simultaneous Mode is occupied, the simultaneous instruction will hold off in the Normal Mode until the Simultaneous Mode is free; i.e., the simultaneous instruction will occupy the Normal Mode, but will not be executed therein. When the Simultaneous Mode becomes free, the instruction will be transferred to the Simultaneous Mode to be executed there, freeing the Normal Mode for the next instruction.

All instructions will be executed serially and will take place in the mode desired when,

1. A System is equipped with a Simultaneous Mode Control Unit.
2. SMDI is not on.
3. ISIM (Inhibit Simultaneity) button on the Console Panel is on.

If a parity error occurs while a Simultaneous Mode input-output instruction is being executed, the mode in which the error occurred is stopped immediately and the instructions presently being executed in the other modes are completed before the computer halts. If the error occurs in the Simultaneous Mode, the SAL (Simultaneous Alarm) light will be on as well as another error light which will indicate the type of error.

#### **Operation of the Data Record File Mode**

The following instructions are designed to operate in the Record File Mode:

Record File Mode Read  
Record File Mode Write

All instructions are staticized in the Normal Mode. When any one of the above instructions are staticized, if:

1. The system is equipped with a Record File Mode Control Unit,
2. The Record File Mode Control Unit is free; i.e., some other instruction is not progressing in the Record File Mode, then

the Record File Mode instruction is transferred to the Record File Mode; i.e., the contents of the NOR Register are transferred to FOR, the contents of the N Register are transferred to the L Register, the contents of the A Register

are transferred to the U Register and the contents of the B Register are transferred to the V Register. The instruction is then executed in the Record File Mode with FOR, L, U and V Registers acting as the NOR, N, A and B Registers respectively. The instruction is then processed similarly to a normal instruction.

Immediately upon the transfer of an instruction from the Normal to the Record File Mode, the Normal Mode is free to accept the next instruction.

If a Record File Mode instruction is staticized and the system is not equipped with a Record File Mode Control Unit, the instruction will be skipped.

If a Record File Mode instruction is staticized and the Record File Mode is occupied, the Record File Mode instruction will hold off in the Normal Mode until the Record File Mode is free; i.e., the Record File Mode Instruction will occupy the Normal Mode, but will not be executed therein. When the Record File Mode becomes free, the instruction will be transferred to the Record File Mode for execution, freeing the Normal Mode for the next instruction.

### **Device Busy Hold-Off**

As soon as an input/output instruction is staticized regardless of the mode in which it is to be executed, it senses the input output device it must use. If the device is busy, the instruction holds off in the Normal Mode until the device is free.

### **Independent Operations**

The following operations are independent operations:

- Band selection
- Track selection
- Rewinding tapes
- Paper advancing

Regardless of the mode in which the instructions causing these functions are executed, once any one of these functions is initiated, they continue independent of the Computer. The instruction, then, is considered by the Computer circuitry to have completed itself upon the initiation of the function, and the mode which the instruction occupied is thereby freed for immediate use.

In a system equipped with both the Simultaneous Mode Control Unit and the Record File Mode Control Unit, it is possible to have one instruction progressing in the Simultaneous Mode, another instruction progressing in the Record File Mode, and still another instruction progressing in the Normal Mode and any number of independent operations in progress, all simultaneously.

If a parity error occurs while a Record File Mode instruction is being executed the mode in which the error occurred is stopped immediately and the instructions presently being executed in the other modes are completed before the computer halts. If the error occurs in the Record File Mode, the FAL (Record File Alarm) light will be on as will another error light which will indicate the type of error.

### **Time Sharing**

Simultaneity in the RCA 301 System is accomplished through a technique known as "time sharing". All input/output instructions need to access the High-Speed Memory for only a fraction of the time they are in progress. For most of their execution times, input/output instructions must wait for some mechanical action in the input/output device to occur (e.g., card movement, tape movement, print drum revolution, etc.)

The nominal time ratios that each input-output instruction must access memory is given in the following table:

DEVICE	Instructions Must Access Memory For	Out of Every
Card Reader	13.44 ms	100 ms
Card Punch (100 cpm)	6.72 ms	600 ms
(200 cpm)	13.44 ms	300 ms
Paper Tape-Read or Punch (100 cps)	7 $\mu$ s	10 ms
(1000 cps)	7 $\mu$ s	1 ms
Printer - 120 Column: Synchronous Mode	20.069 ms	60 ms
Asynchronous Mode	27.328 ms	76 ms
160 Column:		
Synchronous Mode, full speed	26.649 ms	55.8 ms
Asynchronous Mode, full speed	36.288 ms	71.8 ms
Synchronous Mode, reduced speed	26.649 ms	83.9 ms
Asynchronous Mode, reduced speed	36.288 ms	100 ms
Monitor Printer	7 $\mu$ s	100 ms
Data Record File	7 $\mu$ s	400 $\mu$ s
Data Disc File	7 $\mu$ s	62.5 $\mu$ s
Hi-Data Magnetic Tape-Read Write	7 $\mu$ s	100 $\mu$ s
33.3 KC Magnetic Tape-Read Write	7 $\mu$ s	30 $\mu$ s
66.7 KC Magnetic Tape-Read Write	7 $\mu$ s	30 $\mu$ s

In the RCA 301 System, then, the HSM is time shared; i.e., during the time that an input-output instruction is in progress, but is not using memory, another input/output instruction and/or compute instruction can use the memory.

## THE CONSOLE

### Register Display

When the computer is not running, no register is displayed. To display a register, it must be selected. To change the contents of a register, it must be selected and then the proper bits (buttons) depressed. These buttons which display the contents of a selected register are the rightmost bank in Figure 6 illustrating the layout of the buttons on the console.

### REGISTER SELECTION

Depressing one of the select buttons will cause the display of a register. The registers that can be selected are:

P, A, B, S, T, U, V - four characters in length.

NOR/N, SOR/M, FOR/L - two characters displayed; one is the operation code, the other the N Register or its corresponding registers in the other modes.

MR - Memory Register - two characters.

### SPECIAL PURPOSE SWITCHES

These are alternate action switches.

1. OCSP – (One Cycle Stop)  
This switch permits "one status level at a time" operation by stopping the computer at the end of every status level.
2. ICSP – (Instruction Complete Stop)  
Permits "one instruction at a time" operation by stopping the computer prior to the staticizing of the next instruction.
3. FPLS – (First Processing Level Stop)  
Stops the computer after staticizing an instruction.
4. RDM – (Read Memory)  
Allows the displaying of any diad in HSM.
5. WRM – (Write Memory)  
Allows the placing of a diad into two locations in HSM.
6. HSMI – (HSM Inhibit)  
Inhibits information from going to or coming from HSM.
7. BAI – (Bus Adder Inhibit)  
Adding or subtracting ability of the Bus Adder is inhibited. Output of the Bus Adder is the same as the input.
8. STLR – (Status Level Repeat)  
Inhibits changing the current status level.
9. ISIM – (inhibit Simultaneity)  
Causes all instructions to be executed serially although they take place in the mode desired.
10. BCT – (Bypass Card Translation)  
Bypasses the automatic card translation in the card read instruction. Two characters for each column read will be placed in HSM.
11. INT – (Interrupt)  
This button can be sensed by the CTC instruction when N = &.
12. WTAB – (Write to Table)  
When set, this switch allows the arithmetic tables (HSM locations 0000-0199) to be written into HSM. When reset, any attempt to write to the tables will cause an alarm.
13. SMDI – (Simultaneous Mode Inhibit)  
When set, causes all Simultaneous Instructions to be performed in the Normal Mode. It also will store the A Register when the S Register is indicated in the Store Register instruction.
14. ALI – (Alarm Inhibit)  
When this switch is depressed the Computer will not stop on any error condition. The alarm indicator, however will light.

#### STATUS LEVEL SELECTION (STL)

To select a status level its proper bit configuration must be placed in the buttons  $2^6$  to  $2^0$  in the second bank.

#### Alarm Indicators

##### PARITY ERRORS

The following errors indicate incorrect parity in the associated register(s):

1. SORM – (Simultaneous Operation or M Registers)
2. NORN – (Normal Operation of N Registers)
3. FORL – (V or L Registers)
4. NRPE – (Repeat Register)
5. MAPE – (Memory Address Register)
6. MRPE – (Memory Register)

- 7. DPE – (D Register)
- 8. STLE – (Status Level)

#### OTHER ERRORS

- 1. COME – Error in the Comparator.
- 2. ARIE – Arithmetic Error caused by one of the following:
  - Processor with 10,000 or 20,000 character memory:
    - a.  $2^4$  bit is a "one" in MSD of both operands in an Add instruction.
    - b.  $2^4$  bit is a "one" in other than MSD or LSD of either operand.
    - c.  $2^4$  bit is a "one" in the MSD of one of the operands and there is a carry.
  - Processor with 40,000 character memory:
    - a. An address ADD or address SUBTRACT instruction with a resultant negative address whenever an operand is distinguishable from data by having a zone bit in the MSD position.
    - b.  $2^4$  bit is a "one" in other than the MSD or LSD of either operand.
    - c.  $2^5$  bit is a "one" in the MSD of one of the operands and there is a carry.
- 3. WTT – attempted to write to arithmetic table (HSM location -- 0000-0199) with WTAB reset.
- 4. DDF – (Device doesn't Follow)
  - The device addressed is inoperable.
- 5. RE – (Read Error)
  - An error has occurred during a "read" instruction or when data is transferred from HSM to the printer output buffer.
- 6. TAE – (Tape Address Error)
  - Parity error in the tape address.
- 7. CCE – (Card Compare Error)
  - The second read station does not compare with the first read station on the Card Reader; or the read station does not compare with the punch on the Card Punch.
- 8. WE – (Write Error)
  - An error has occurred during a "write" instruction or when data is transferred between the Memory Register and an input or output buffer.
- 9. MCP – (Missing Clock Pulse)
  - This is an error on the 33.3 or 66.7 KC tape stations.
- 10. SAL – (Simultaneous Alarm)
  - An input-output alarm has occurred and the instruction was in the Simultaneous Mode. When this light is on, another one will also light to indicate the type of error.
- 11. MPE – (Multipunch Error)
  - A non-301 character has been recognized on a card read with the BCT switch off.
- 12. CIG – (Character in the Gap)
  - A block of less than 3 characters has been read.
- 13. RAE – (Record File Address Error)
  - Parity error in the Record File Address Register.
- 14. FAL – (Record File Alarm)
  - An error has occurred in an instruction in the Record File Mode.

#### MISCELLANEOUS

- 1. SB – Indicates Simultaneous Mode Busy.
- 2. FB – Indicates Record File Mode Busy.

3. Power Off – Will turn off power. It is not possible to turn power on from the console. This must be done at the Power Supply.
4. GEN RES – General Reset – Resets all registers and counters and the majority of flip-flops. It sets up the first status level (P1).
5. START – Used to execute status level displayed.
6. All buttons having diamond configurations are reset buttons.

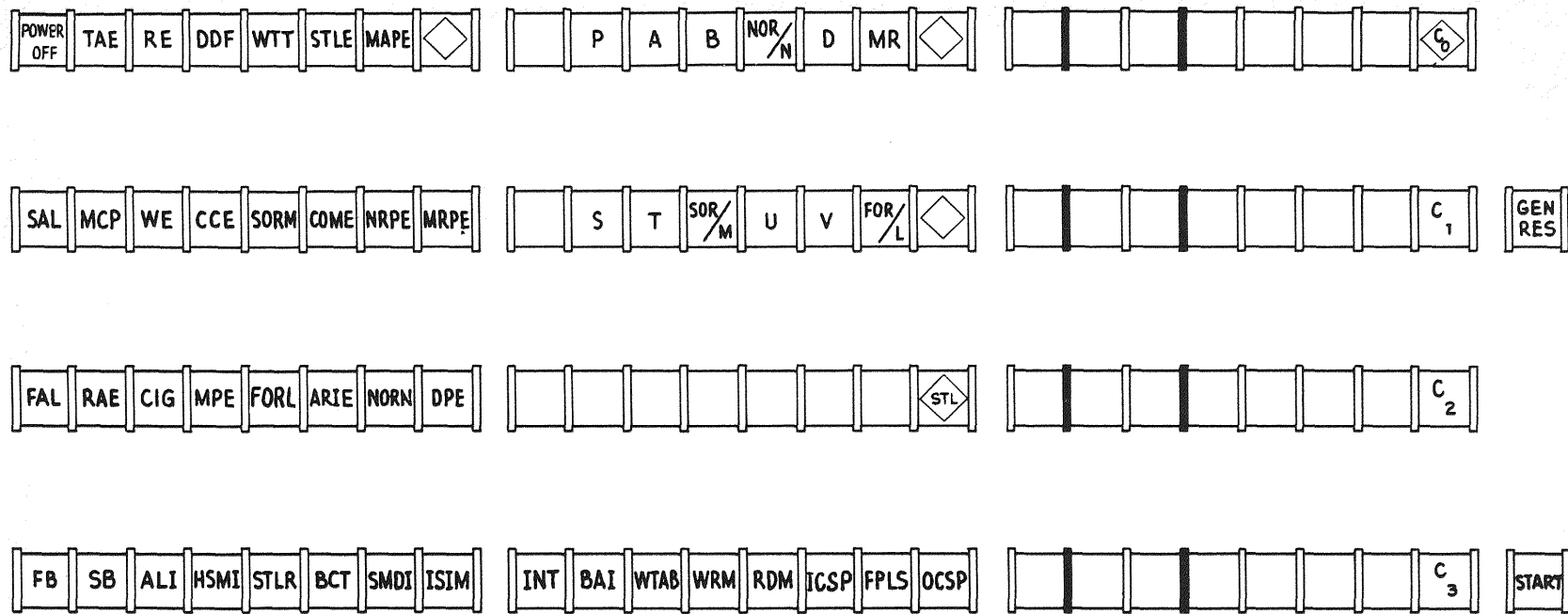


Figure 6—RCA 301 Console Display

# THE RCA 301 INSTRUCTIONS

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## GENERAL DESCRIPTION

### INTRODUCTION

The RCA 301 Computer operates under the direction of two-address instructions. For descriptive purposes, these instructions may be classified into four general categories: (1) Input/Output, (2) Data Handling, (3) Arithmetic and (4) Decision and Control.

#### Input-Output Instructions

These instructions enable the Computer to communicate with the peripheral devices. They perform the functions of positioning or searching tapes or disc files, bringing data from an input medium into the computer or sending data from the computer to an output medium.

In the group, certain operations can be executed in the Simultaneous Mode as well as in the Normal Mode, so that operational time for these instructions can overlap that of other instructions. In addition, several instructions can be executed in the Record File Mode.

Rewind to BTC, Band Select and Track Select instructions as well as the paper advance function are initiated by the Computer, but once underway, operate completely independent of the Computer. Any number of tapes may be rewinding while three instructions (unrelated to the rewinding tapes) are being simultaneously executed.

#### Data Handling Instructions

These are non-arithmetic instructions for manipulation of data stored in the High-Speed Memory. The instructions included in this group permit operational control by symbol, address, or count. The major data handling functions operate from right to left or left to right according to the specific instruction involved.

#### Arithmetic Instructions

Of the instructions in this group, two are decimal, and three are used to alter the bit configuration of an operand through the use of logical operations.

The decimal instructions operate in accordance with arithmetic rules and are designed to handle operands of equal length.

Three instructions, Logical "OR", Logical "AND" and Exclusive "OR" constitute what may be considered as a separate arithmetic category. They are used to alter the bit configuration of an operand by the employment of a second operand to "mask-out" or to insert "1" bits.

The Previous Result Indicators (PRI's) preserve the sign of the result of an arithmetic instruction for reference by a subsequent decision instruction.

#### Decision and Control Instructions

These instructions influence the sequence of operation. Three instructions enable the programmer to address registers directly and one instruction is conditional; that is, it chooses a path according to selected conditions. One instruction stops the Computer operation. The "Repeat" instruction enables the Computer to execute the same instruction a designated number of times. The compare instruction enables the Computer to determine the relative magnitude of two operands of equal length.

#### Description of Instructions

Information pertaining to each instruction is described under the headings as given below. Special explanation for some of these is also included.

Instructive Symbol (OP Code)  
Name and Abbreviation of Instruction  
Repeatable, if applicable  
General Description  
Format of Instruction  
Direction of operation  
Standard Location, if used  
Outline of operation  
Final Registers Contents  
PRI settings, where applicable  
Timing  
Example

#### DIRECTION OF OPERATION

A Direction of Operation subsection appears in all applicable instructions and defines the direction of operation in HSM.

#### OPERATION

An Outline of Operation subsection supplements the General Description prefacing the instruction. Internal logic is described not in every detail, but only to the extent that it contributes to the attainment of the objectives of a programmers reference manual: (1) to help the programmer gain a better understanding of Computer operation, (2) to permit the programmer to modify the instructions and their application for individual problem solution and (3) to enable the programmer to develop advanced programming techniques.

#### TIMING

Due to the variable item length concept in the RCA 301 System, instruction times can be expressed only as a function of the number of characters involved in a given operation. For example, the time required to write out to tape depends on the number of characters to be written, and the time required to add two numbers together depends on the number of digits in the operands.

The time, or timing formula, listed for each instruction includes staticizing time, and STA or STP where applicable. Indirect addressing requires an additional 14 microseconds per indirect address.

Each time a repeatable instruction is repeated there are three additional status levels (21 microseconds) required when the contents of the  $N_R$  (REPEAT) Register exceed zero, and one additional status level (7 microseconds) when the  $N_R$  (Repeat) Register contents are zero.

#### EXAMPLES

Wherever possible, the examples that accompany the instruction include representation of the affected portion or portions of the High-Speed Memory. The content of the HSM locations are shown by bit values in some of the instructions and as alphanumeric characters in other instructions.

In each example, the subheading "HSM before Instruction is Executed" is to be interpreted as before execution but after staticizing. The contents of the memory locations are not affected by staticizing. The initial register settings of  $A_i$ ,  $B_i$ ,  $T_i$ ,  $S_i$  however, reflect register contents after staticizing.

# THE RCA 301 INSTRUCTIONS

	<i>Page</i>
<b>DATA HANDLING INSTRUCTIONS</b>	
Translate by Table (A) . . . . .	TRA-31
Locate Symbol Left (K) . . . . .	LSL-33
Locate Symbol Right (L) . . . . .	LSR-36
Transfer Data Left (M) . . . . .	DL-38
Transfer Data Right (N) . . . . .	DR-40
Transfer Data by Symbol Left (#) . . . . .	DSL-42
Transfer Data by Symbol Right (P) . . . . .	DSR-43
Transfer Symbol to Fill (J) . . . . .	SF-44
<b>ARITHMETIC INSTRUCTIONS</b>	
Add (+) . . . . .	ADD-45
Subtract (-) . . . . .	SUB-48
Logical "OR" (Q) . . . . .	OR-50
Logical "AND" (T) . . . . .	AND-52
Exclusive "OR" (U) . . . . .	EXO-54
<b>DECISION AND CONTROL INSTRUCTIONS</b>	
Store Register (V) . . . . .	REG-56
Conditional Transfer of Control (W) . . . . .	CTC-58
Compare Left (Y) . . . . .	COM-60
Tally (X) . . . . .	TA-62
Halt (.) . . . . .	HLT-63
Repeat (R) . . . . .	RPT-64
Input/Output Sense (S) . . . . .	IOS-65
<b>INPUT/OUTPUT INSTRUCTIONS</b>	
Card Read Normal (0) . . . . .	CRN-67
Card Read Simultaneous (1) . . . . .	CRS-70
Card Punch Normal (2) (Model 334 Card Punch) . . . . .	CPN-72
Card Punch Normal (2) (Model 336 Card Punch) . . . . .	CPN-74
Card Punch Simultaneous (3) (Model 334 Card Punch) . . . . .	CPS-75
Card Punch Simultaneous (3) (Model 336 Card Punch) . . . . .	CPS-76
Tape Read Forward Normal (4) . . . . .	RFN-77
Tape Read Forward Simultaneous (5) . . . . .	RFS-80
Tape Read Reverse Normal (6) . . . . .	RRN-81
Tape Read Reverse Simultaneous (7) . . . . .	RRS-83
Tape Write Normal (8) . . . . .	TWN-84
Tape Write Simultaneous (9) . . . . .	TWS-86
Rewind to BTC (;) . . . . .	RWD-87
Print & Paper Advance Normal (B) . . . . .	PAN-88
Print & Paper Advance Simultaneous (C) . . . . .	PAS-91
Band Select Normal (D) . . . . .	BSN-93
Band Select Record File Mode (E) . . . . .	BSM-94
Block Read Record Normal (F) . . . . .	BRN-95
Block Read Record Simultaneous (G) . . . . .	BRS-97
Block Write Record Normal (H) . . . . .	BWN-99
Block Write Record Simultaneous (I) . . . . .	BWS-101
Record File Mode Read (*) . . . . .	RMR-103
Record File Mode Write (%) . . . . .	RMW-105
Track Select (D) . . . . .	TS-107
Sector Read Disc Normal (F) . . . . .	SRN-108
Sector Read Disc Simultaneous (G) . . . . .	SRS-110
Sector Write Disc Normal (H) . . . . .	SWN-112
Sector Write Disc Simultaneous (I) . . . . .	SWS-114

# A Translate By Table (TRA)

Repeatable

## General Description

This instruction translates a specified number of characters in an area from one code to another by the use of a translate table. It may be used to translate from one to forty-four characters in memory.

## Format

- Operation — A
- N — number (0-44) of characters to be translated. (See Appendix VI A).
- A Address — HSM location of leftmost character to be translated and result area.
- B Address — HSM location of first character of translate table (must end in 00).

## Direction of Operation

Left to right.

## Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the contents of the A Register is transferred to the D Register as follows:  $2^2$ ,  $2^1$ , and  $2^0$  bits are transferred to corresponding positions in  $D^3$ ;  $2^5$ ,  $2^4$ , and  $2^3$  bits are transferred to the  $2^2$ ,  $2^1$ , and  $2^0$  positions, respectively, of  $D_2$ ; the remaining bits in the D Register are zeros, except parity bits, which are generated properly. The contents of  $B_0$ ,  $B_1$ ,  $D_2$ , and  $D_3$  are used to address the translate table. The character is read out of the translate table and transferred to the HSM location specified by the contents of the A Register. The contents of the A Register are incremented by one. N is decremented by one and the cycle is repeated.

## Final Register Contents

- $(A)_f$  = HSM character location one to the right of the last character translated.
- $(B)_f = (B)_i$

## Timing

Total time in microseconds  
 $= 21n + 35$  where  $n$  = number of characters to be translated.

## Example:

*Instruction:*

Operation	N	A Address	B Address
A	5	4053	6300

*HSM before the Instruction is Executed*

4050	4051	4052	4053	4054	4055	4056	4057	4058
1	2	5	7	3	6	4	8	9

*Table: (Partial)*

	0	1	2	3	4	5	6	7	8	9
630	Z	A	B	C	D	E	F	G		
631	H	I	J	K	L	M	N	O		

*HSM after the Instruction*

4050	4051	4052	4053	4054	4055	4056	4057	4058
1	2	5	G	C	F	D	H	9

*Final Register Contents:*

$$A_f = 4058$$

$$B_f = 6300$$

*Time:*

$$21(5) + 35 = 140 \mu s.$$

## K Locate Symbol Left (LSL)

### General Description

This instruction searches through the contents of successive HSM locations between and including, two specified addresses. The operation ceases when the rightmost location is reached or upon detecting a non-selected symbol.

### Format

Operation — K.  
N — Selected symbol.  
A Address — Leftmost HSM location to be searched.  
B Address — Rightmost HSM location to be searched.

### Direction of Operation

Left to right.

### Standard Location

STA (0212-0215)

### Outline of Operation

This instruction initially sets PRZ, and operates in the following cycle:

The contents of the A Register are placed in the Memory Address Register. The contents of the A Register are compared with the contents of the B Register and if this comparison proves equal ABE (A-B Equality) is set; if the comparison proves unequal ABE is not set. The contents of the A Register are incremented by one.

The contents of the HSM location specified by the Memory Address Register is compared with the contents of the N Register.

- (1) If this comparison proves unequal, and the contents of the Memory Address Register are equal to  $A_i$ , PRN is set, the contents of the A Register is decremented by two, and the instruction terminates.
- (2) If this comparison proves unequal, and the contents of the Memory Address Register are not equal to  $A_i$ , PRP is set, the contents of the A Register is decremented by two, and the instruction terminates.
- (3) If this comparison proves equal and ABE is set the contents of the A Register is decremented by one and the instruction terminates.
- (4) If this comparison proves equal and ABE is not set the cycle is repeated.

### Final Register Contents

If a character is found not equal to N

$(A)_f = \text{One HSM address to the left of that character.}$   
 $(B)_f = (B)_i$

If all characters searched are equal to the contents of N

$(A)_f = (B)_i$   
 $(B)_f = (B)_i$

### PRI

PRN is set when the first character searched is not equal to the contents of N.

PRZ is set when all characters searched are equal to the contents of N.

PRP is set if a non selected symbol is found in the specified HSM area after a character equal to the contents of N has been found.

### Timing

Total time in microseconds

=  $14n + 70$  if a character is found not equal to the contents of N.

=  $14n + 56$  if all characters searched are equal to the contents of N.

n = number of selected symbols searched.

### Example #1

Instruction:

Operation	N	A Address	B Address
K	O	1000	1009

HSM before and after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
0	0	0	0	0	1	0	3	0	9

Final Register Contents:

$(A)_f = 1004$

$(B)_f = 1009$

PRI

PRP is set

Time:

$14(5) + 70 = 140 \mu s.$

### Example #2

Instruction:

Operation	N	A Address	B Address
K	sp	2010	2019

HSM before and after Instruction is Executed:

2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
sp	sp	sf	sp	sp	sp	sp	sp	sp	sp

Final Register Contents:

$A_f = 2019$

$B_f = 2019$

PRI

PRZ is set

Time:

$14(10) + 56 = 196 \mu s.$

**Example #3**

*Instruction:*

Operation	N	A Address	B Address
K	O	3278	3284

*HSM Before and After Instruction is Executed:*

<b>3278</b>	<b>3279</b>	<b>3280</b>	<b>3281</b>	<b>3282</b>	<b>3283</b>	<b>3284</b>
3	2	7	9	0	0	0

*Final Register Contents:*

$$A_f = 3277$$

$$B_f = 3284$$

*PRI*

PRN is set

*Time:*

$$14(1) + 70 = 84 \mu s.$$

## L Locate Symbol Right (LSR)

### General Description

This instruction searches through the contents of successive HSM locations between, and including, two specified addresses. The operation ceases when the leftmost location is reached or upon detecting a non-selected symbol.

### Format

- Operation — L.  
N — Selected Symbol.  
A Address — Rightmost HSM location to be searched.  
B Address — Leftmost HSM location to be searched.

### Direction of Operation

Right to left.

### Standard Location

STA (0212-0215)

### Outline of Operation

This instruction initially sets PRZ, and operates in the following cycle.

The contents of the A Register are placed in the Memory Address Register. The contents of the A Register are compared with the contents of the B Register and if this comparison proves equal ABE (A-B Equality) is set; if the comparison proves unequal, ABE is not set. The contents of the A Register are decremented by one.

The contents of the HSM location specified by the Memory Address Register is compared with the contents of the N Register.

- (1) If this comparison proves unequal, and the contents of the Memory Address Register are equal to  $A_i$ , PRN is set, the contents of the A Register is incremented by two, and the instruction terminates.
- (2) If this comparison proves unequal, and the contents of the Memory Address Register are not equal to  $A_i$ , PRP is set, the contents of the A Register is incremented by two, and the instruction terminates.
- (3) If this comparison proves equal and ABE is set the contents of the A Register is incremented by one and the instruction terminates.
- (4) If this comparison proves equal and ABE is not set the cycle is repeated.

### Final Register Content

If a character is found not equal to N

$$(A)_f = \text{One HSM address to the right of that character}$$
$$(B)_f = (B)_i$$

If all characters searched are equal to the contents of N

$$(A)_f = (B)_i$$
$$(B)_f = (B)_i$$

### PRI

PRN is set if the first character searched is not equal to the contents of N.

PRZ is set when all characters searched are equal to the contents of N.

PRP is set when a non symbol is found in the specified HSM area after a character equal to the contents of N has been found.

### Timing

Total time in microseconds

$$= 14n + 70 \text{ if a character is found not equal to the contents of N.}$$

$= 14n + 56$  if all characters searched are equal to the contents of N.  
 N = number of selected symbols searched.

**Example**

*Instruction:*

Operation	N	A Address	B Address
L	—	1009	1000

*HSM before and after Instruction is Executed:*

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
1	0	3	0	9	—	—	—	—	—

*Final Register Content:*

$(A)_f = 1005$

$(B)_f = 1000$

*PRI*

PRP is set

*Time*

$14(5) + 70 = 140 \mu s.$

## M Transfer Data Left (DL)

Repeatable

### General Description

This instruction transfers a specified number of consecutive characters from one HSM area to another HSM area. It may be used to transfer from one to forty-four characters in memory.

### Format

- Operation — M
- N — 0-44 characters to be transferred (See Appendix VI A),
- A Address — HSM location of leftmost character to be transferred.
- B Address — Destination address of first character.

### Direction of Operation

Left to right.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The contents of the A and B Registers are incremented by one, the contents of the N Register are decremented by one, and the cycle is repeated.

### Final Register Contents

(A)<sub>f</sub> = Address location one to the right of the last character transferred.

(B)<sub>f</sub> = Address location one to the right of the last destination address.

### Timing

Total time in microseconds

$$= 14n + 35, \text{ where } n \text{ equals the number of characters transferred.}$$

### Example

*Instruction:*

Operation	N	A Address	B Address
M	5	1000	1006

*HSM before Instruction is Executed:*

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011
A	B	A	T	E	—	—	—	—	—	—	—

*HSM after Instruction is Executed:*

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011
A	B	A	T	E	—	A	B	A	T	E	—

***Final Register Setting:***

$$(A)_f = 1005$$

$$(B)_f = 1011$$

***Time:***

$$(14 \times 5) + 35 = 105 \mu\text{s}.$$

## N Transfer Data Right (DR)

Repeatable

### General Description

This instruction transfers a specified number of consecutive characters from one HSM area to another. It may be used to transfer from one to forty-four characters in memory.

### Format

- Operation — N
- N — 0-44 characters to be transferred (See Appendix VI A).
- A Address — HSM location of rightmost character to be transferred.
- B Address — Destination address of first character.

### Direction of Operation

Right to left.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The contents of the A and B Registers are decremented by one, the contents of the N Register are decremented by one, and the cycle is repeated. The A Address and the B Address will be staticized although N may equal zero.

### Final Register Contents

(A)<sub>f</sub> = Address of location one to the left of the last character transferred.

(B)<sub>f</sub> = Address of location one to the left of the last destination location.

### Timing

Total time in microseconds.

=  $14n + 35$ , where n equals the number of characters transferred.

### Example

Instruction:

Operation	N	A Address	B Address
N	4	1003	1009

HSM before Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
B	0	0	K	—	—	—	—	—	—

HSM after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
B	0	0	K	—	—	B	0	0	K

***Final Register Settings:***

$$(A)_f = 0999$$

$$(B)_f = 1005$$

***Time:***

$$(4 \times 14) + 35 = 91 \mu\text{s}.$$

# # Transfer Data By Symbol Left (DSL)

Repeatable

## General Description

This instruction transfers data terminated by a selected symbol from one HSM location to another.

## Format

- Operation — #
- N — Selected symbol on which to stop transferring.
- A Address — HSM location of leftmost character to be transferred.
- B Address — Destination address of first character.

## Direction of Operation

Left to right

## Standard Location

STA (0212-0215)

## Outline of Operation

This instruction operates in the following cycle:

The contents of the HSM location specified by the A Register are compared with the contents of the N Register. The character specified by the A Register is transferred to the HSM location specified by the B Register and the contents of the A and B Registers are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

## Final Register Contents

- (A)<sub>f</sub> = HSM address location one to the right of the specified symbol in the original area.
- (B)<sub>f</sub> = HSM address location one to the right of the symbol in the destination area.

## Timing:

Total time in microseconds.

$$= 14n + 49, \text{ where } n \text{ equals the number of characters being transferred.}$$

## Example

Instruction:

Operation	N	A Address	B Address
#	"	2000	2007

HSM before Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
\$	4	3	2	"	—	—	—	—	—	—	—	—

HSM after Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
\$	4	3	2	"	—	—	\$	4	3	2	"	—

Final Register Contents:

- (A)<sub>f</sub> = 2005
- (B)<sub>f</sub> = 2012

Time:

$$(5 \times 14) + 49 = 119 \mu s.$$

# P Transfer Data By Symbol Right (DSR)

Repeatable

## General Description

This instruction transfers data terminated by a selected symbol from one HSM location to another.

## Format

- Operation — P
- N — Selected symbol on which to stop transferring.
- A Address — HSM location of rightmost character to be transferred.
- B Address — Destination address of first character.

## Direction of Operation

Right to left.

## Standard Location

STA (0212-0215)

## Outline of Operation

This instruction operates in the following cycle:

The contents of the HSM location specified by the A Register are compared with the contents of the N Register. The character specified by the A Register is transferred to the HSM location specified by the B Register and the contents of the A and B Registers are decremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

## Final Register Contents

- (A)<sub>f</sub> = HSM address of location one to the left of the specified symbol in the original area.
- (B)<sub>f</sub> = HSM address of location one to the left of the symbol in the destination area.

## Timing

Total time in microseconds

$$= 14n + 49, \text{ where } n \text{ equals the number of characters being transferred.}$$

## Example

Instruction:

Operation	N	A Address	B Address
P	"	3008	3003

HSM before Instruction is Executed:

2999	3000	3001	3002	3003	3004	3005	3006	3007	3008
-	-	-	-	-	"	\$	4	3	2

HSM after Instruction is Executed:

2999	3000	3001	3002	3003	3004	3005	3006	3007	3008
"	\$	4	3	2	"	\$	4	3	2

Final Register Contents:

- (A)<sub>f</sub> = 3003
- (B)<sub>f</sub> = 2998

Time:

$$(5 \times 14) + 49 = 119 \mu s.$$

## J Transfer Symbol To Fill (SF)

### General Description

This instruction inserts a selected symbol into each HSM location between and including the two given addresses.

### Format

Operation — J  
 N — Selected Symbol  
 A Address — Leftmost location in memory to be filled.  
 B Address — Rightmost location in memory to be filled.

### Direction of Operation

Left to right.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. If this comparison proves equal, the contents of the A Register are incremented by one and the instruction terminates. If the operation proves unequal, the contents of the A Register are incremented by one, and the cycle is repeated.

### Final Register Contents

$(A)_f = (B)_i + 1$   
 $(B)_f = (B)_i$

### Timing

Total time in microseconds

=  $7n + 35$ , where n equals the number of locations filled.

### Example

Instruction:

Operation	N	A Address	B Address
J	0	3001	3009

HSM before Instruction is Executed:

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009	3010
J	-	S	M	I	T	H	-	-	I	I

HSM after Instruction is Executed:

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009	3010
J	0	0	0	0	0	0	0	0	0	I

Final Register Contents:

$(A)_f = 3010$   
 $(B)_f = 3009$

Time:

$(9 \times 7) + 35 = 98 \mu s.$

## + Add (ADD)

Repeatable

### General Description

This instruction performs decimal addition in accordance with algebraic rules, providing a non-zero suppressed sum, which is stored in the memory location originally occupied by the augend. The two operands must be equal in length, but may be of any length up to forty-four characters per each operand.

### Format

Operation — +

N — Number of characters (0-44) in each operand. (See Appendix VI A).

A Address — HSM location of least significant digit of augend and sum.

B Address — HSM location of least significant digit of addend.

### Direction of Operation

Right to left.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are transferred to the  $D_2$  portion of the D Register; the contents of the HSM location specified by the B Register are transferred to the  $D_3$  portion of the D Register. The contents of the D Register are used to generate an address in the Sum or Difference Table located in HSM depending on the sign in each operand. If the signs of the operands are alike, the Sum Table is addressed; if unlike, the Difference Table is addressed. The character thus addressed is transferred to the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the cycle is repeated.

The sign of each operand does not require a separate character location, but is indicated by the  $2^5$  bit of the least significant digit (LSD) of each operand. When a one bit is present in the  $2^5$  position, the sign is negative. Otherwise it is assumed positive.

In the event there is a carry beyond the most significant digit (MSD) of the sum, a one bit is placed in the  $2^4$  bit position of the MSD of the sum and the first Overflow Indicator, which is present in all Processors, is set. In a Processor with a 40,000 character memory there may be an additional overflow carry from the  $2^4$  to the  $2^5$  position of the MSD of the sum and a second Overflow Indicator set. The  $2^4$  and  $2^5$  bit positions of the MSD of the sum then act as a two bit binary counter. Each Overflow Indicator can be sensed by the Conditional Transfer of Control instruction

\*When there is a carry beyond the MSD of the sum, and the first Overflow Indicator has already been set in a Computer containing only one Overflow Indicator, the Computer stops on an alarm. When there is a carry beyond the MSD of the sum in a Computer with a second Overflow Indicator and this indicator has already been set, the Computer stops on an alarm.

The only allowable one zone bits in the operands of an addition for a processor with up to 20,000 characters are in the  $2^4$  bit position of the MSD and the  $2^4$  and  $2^5$  positions in the LSD. The only allowable one zone bits in the operands of an addition for a processor with 40,000 characters are the  $2^4$  and  $2^5$  bit positions in the MSD and the LSD.

In single character operands, however, a one bit in the  $2^4$  position of either operand causes an alarm stop.

If the operands have unlike signs and the larger, in absolute value, is the addend, then this causes the "end around condition" when N equals zero. By the use of the Difference Table, the sum is complemented to give the correct result.

When the ADD instruction is used for address modification, the following special conditions apply:

1. If an indirect address is indicated by a one in the  $2^4$  bit position of the LSD of either operand, a one is generated in the  $2^4$  position of the LSD of the sum.

2. Addresses must always be positive. If it is desired to decrease an address, use the subtract instruction.
3. If the result of address addition is greater than 20,000 in a processor containing up to a 20,000 character memory, an alarm stop occurs.
4. If the result of address addition is greater than 40,000 in a processor with a 40,000 character memory, an alarm stop occurs.

**Final Register Contents**

- (A)<sub>f</sub> = HSM address of location one to the left of the MSD of the sum.
- (B)<sub>f</sub> = HSM address of location one to the left of the MSD of the addend.

**PRI**

- PRP is set if the sum is positive.
- PRZ is set if the sum is zero.
- PRN is set if the sum is negative.

**Timing**

Total time in microseconds

$$= 28n + 49, \text{ where } n \text{ is the number of characters in either operand (operands must be of equal lengths).}$$

If an "end around condition" exists,  $21n + 14$  microseconds must be added to the above.

**Example**

*Instruction:*

Operation	N	A Address	B Address
+	5	1006	1012

*HSM before Instruction is Executed:*

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
A	0	1	1	8	2	B	5	4	3	2	1

*HSM after Instruction is Executed:*

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
A	5	5	5	0	3	B	5	4	3	2	1

*Final Register Contents:*

- (A)<sub>f</sub> = 1001
- (B)<sub>f</sub> = 1007

**PRI**

PRP is set.

*Time:*

$$28(5) + 49 = 189 \mu s.$$

**Example #2**

*Instruction:*

Operation	N	A Address	B Address
+	4	2018	2023

*HSM before the Instruction is Executed:*

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
—	2	4	5	7	—	3	2	6	K	—

*HSM after Instruction is Executed:*

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
—	0	8	0	N	—	3	2	6	K	—

*Final Register Contents:*

$$(A)_f = 2014$$

$$(B)_f = 2019$$

*PRI*

PRN is set.

*Time: (End around condition)*

$$28(4) + 49 + 21(4) + 14 = 259 \mu s.$$

**Example #3**

*Instruction:*

Operation	N	A Address	B Address
+	3	3356	3352

*HSM before Instruction is Executed:*

3349	3350	3351	3352	3353	3354	3355	3356	3357
—	3	2	6	—	8	5	1	—

*HSM after the Instruction is Executed:*

3349	3350	3351	3352	3353	3354	3355	3356	3357
—	3	2	6	—	A	7	7	—

First Overflow Indicator is set

*Final Register Contents:*

$$(A)_f = 3353$$

$$(B)_f = 3349$$

*PRI*

PRP is set.

*Time:*

$$28(3) + 49 = 133 \mu s.$$

**General Description**

This instruction performs decimal subtraction in accordance with algebraic rules producing a non-zero suppressed difference which is stored in the memory location originally occupied by the minuend. The two operands must be equal in length, but of any length up to forty-four characters for each operand.

**Format**

- Operation — (minus)
- N — Number (0-44) of characters in each operand. (See Appendix VI-A),
- A Address — HSM location of least significant digit of the minuend and the difference.
- B Address — HSM location of least significant digit of the subtrahend.

**Direction of Operation**

Right to left.

**Outline of Operation**

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are transferred to the  $D_2$  portion of the D Register; the contents of the HSM location specified by the B Register are transferred to the  $D_3$  portion of the D Register. The contents of the D Register are used to generate an address in the Sum or Difference Table located in HSM depending on the sign in each operand. If the signs of the operands are alike, the Difference Table is addressed; if unlike the Sum Table is addressed. The character thus addressed is transferred to the HSM location specified by the A Register. The contents of the A, B, and N Register are decremented by one and the cycle is repeated.

The sign of each operand does not require a separate character location, but is indicated by the  $2^5$  bit of the least significant digit (LSD) of each operand. When a one bit is present in the  $2^5$  position, the sign is negative. Otherwise it is assumed positive.

In the event there is a carry beyond the most significant digit (MSD) of the result, a one bit is placed in the  $2^4$  bit position of the MSD of the result, and the first Overflow Indicator, which is present in all Processors, is set. In a processor with a 40,000 character memory, there may be an additional overflow carry from the  $2^4$  to the  $2^5$  bit position of the MSD of the result, and a second Overflow Indicator set. The  $2^4$  and  $2^5$  bit positions of the MSD of the result then act as a two bit binary counter. Each Overflow Indicator can be sensed by the Conditional Transfer of Control instruction.

When there is a carry beyond the MSD of the result, and the first Overflow Indicator has already been set in a computer containing only one Overflow Indicator, the computer stops on an alarm. When there is a carry beyond the MSD of the result in a computer with a second Overflow Indicator and this indicator has already been set, the computer stops on an alarm.

The only allowable one zone bits in the operands of a subtraction for a processor with up to 20,000 characters, are in the  $2^4$  bit position of the MSD and the  $2^4$  and the  $2^5$  bit positions of the LSD. The only allowable one zone bits in the operands of a subtraction, for a processor with 40,000 characters, are the  $2^4$  and  $2^5$  bit positions in the MSD and the LSD.

In single character operands, however, a one bit in the  $2^4$  position of either operand causes an alarm stop.

If the operands have like signs, and the larger, in absolute value, is the subtrahend, then this causes the "end around condition" when N equals zero. By the use of the Difference Table, the difference is complemented to give the correct result.

When the SUBTRACT instruction is used for address modification, the following special conditions apply:

1. If an indirect address is indicated by a one in the  $2^4$  bit position of the LSD of either operand, a one is generated in the  $2^4$  position of the LSD of the difference.

2. Both addresses entering the subtraction must be positive.
3. The result must be positive.

**Final Register Contents**

(A)<sub>f</sub> = Address of location one to the left of the MSD of the difference.  
 (B)<sub>f</sub> = Address of location one to the left of the MSD of the subtrahend.

**PRI**

PRP is set if the result is positive.  
 PRZ is set if the result is zero.  
 PRN is set if the result is negative.

**Timing**

Total time in microseconds  
 = 28n + 49, where n is the number of characters in either operand (operands must be of equal lengths),  
 If an "end around condition" exists, 21n + 14 microseconds must be added to the above.

**Example**

*Instruction*

Operation	N	A Address	B Address
—	3	2006	2010

*HSM before Instruction is Executed:*

2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
A	E	R	9	9	9	3	1	2	3

*HSM after Instruction is Executed:*

2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
A	E	R	8	7	6	3	1	2	3

*Final Register Contents:*

(A)<sub>f</sub> = 2003  
 (B)<sub>f</sub> = 2007

**PRI**

PRP is set

*Time:*

28 (3) + 49 = 133 μs.

## Q Logical "OR" (OR)

Repeatable

### General Description

This instruction is one of three instructions which provides the 301 system with bit manipulation abilities. It operates on equal length operands according to the rules outlined under "Outline of Operation" below.

### Format

- Operation — Q
- N — Number (0-44) of characters in each operand. (See Appendix VI-A).
- A Address — HSM location of least significant digit of first operand and result.
- B Address — HSM location of least significant digit of second operand.

### Direction of Operation

Right to left.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

<i>Bit in First Operand</i>	<i>Bit in Second Operand</i>	<i>Bit in Result</i>
0	0	0
0	1	1
1	0	1
1	1	1

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

### Example of Rules

(a) 1 00 1001	(b) 0 11 0001
1 01 0001	0 10 0011
<hr/>	<hr/>
0 01 1001	1 11 0011

### Final Register Contents

(A)<sub>t</sub> = Address of location one to the left of the most significant digit of the result.

(B)<sub>t</sub> = Address of location one to the left of the most significant digit of second operand.

### Timing

Total time in microseconds

=  $21n + 35$ , where  $n$  is the number of characters in either operand (operands must be of equal lengths).

### Example

#### Instruction:

Operation	N	A Address	B Address
Q	2	1003	1005

*HSM before Instruction is Executed:*

Memory Location	1002	1003	1004	1005
Bits within Each Location	1 00 0000	0 00 0111	0 00 0001	0 01 0101

*HSM after Instruction is Executed:*

Memory Location	1002	1003	1004	1005
Bits within Each Location	0 00 0001	1 01 0111	0 00 0001	0 01 0101

*Final Register Contents:*

(A)<sub>r</sub> = 1001

(B)<sub>r</sub> = 1003

*Time:*

$$21(2) + 35 = 77 \mu\text{s.}$$

## T Logical "And" (AND)

Repeatable

### General Description

This instruction is one of three instructions which provides the 301 system with bit manipulation abilities. It operates on operands of equal length according to the rules outlined under "Outline of Operation" below.

### Format

- Operation — T  
N — Number (0-44) of characters in each operand. (See Appendix VI-A).  
A Address — HSM location of least significant digit of the first operand and the result.  
B Address — HSM location of least significant digit of the second operand.

### Direction of Operation

Right to left.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

<i>Bit in First Operand</i>	<i>Bit in Second Operand</i>	<i>Bit in Result</i>
0	0	0
0	1	0
1	0	0
1	1	1

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

### Example of Rules

(a) 1 00 1001	(b) 0 11 0001
1 01 0001	0 10 0011
<hr/>	<hr/>
0 00 0001	1 10 0001

### Final Register Contents

- (A)<sub>f</sub> = Address of location one to left of the most significant digit of the result.  
(B)<sub>f</sub> = Address of location one to the left of the most significant digit of second operand.

### PRI

- PRP is set, if at least one of the information bits in the result is a one.  
PRN is set, if all the information bits in the results are zero.

### Timing

- Total time in microseconds  
= 21n + 35, where n is the number of characters in either operand (operands must be of equal length).

**Example****Instruction:**

Operation	N	A Address	B Address
T	2	1001	1006

**HSM before Instruction is Executed:**

HSM Location	1000	1001	1002	1003	1004	1005	1006
Bits within Each Location	1 00 0000	1 00 1111	—	—	—	0 00 0111	1 11 0101

**HSM after Instruction is Executed:**

HSM Location	1000	1001	1002	1003	1004	1005	1006
Bits within Each Location	1 00 0000	1 00 0101	—	—	—	0 00 0111	1 11 0101

**Final Register Contents:**(A)<sub>f</sub> = 0999(B)<sub>f</sub> = 1004**PRI**

PRP is set.

**Time:**

21 (2) + 35 = 77 μs.

## U Exclusive "OR" (EXO)

Repeatable

### General Description

This instruction is one of three instructions which provides the 301 System with bit manipulation abilities. It is executed on operands of equal length according to the rules outlined under "Outline of Operation" below.

### Format

- Operation — U  
N — Number of characters (0-44) in each operand. (See Appendix VI-A).  
A Address — HSM location of least significant digit of first operand and result.  
B Address — HSM location of least significant digit of second operand.

### Direction of Operation

Right to left.

### Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

<i>Bit in First Operand</i>	<i>Bit in Second Operand</i>	<i>Bit in Result</i>
0	0	0
0	1	1
1	0	1
1	1	0

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

### Examples of Rules

(a) 1 10 0111	(b) 0 01 0101
1 11 1001	0 10 1010
<hr/>	<hr/>
1 01 1110	1 11 1111

### Final Register Contents

(A)<sub>f</sub> = Address of location one to the left of the most significant digit of the result.

(B)<sub>f</sub> = Address of location one to the left of the most significant digit of the operand specified by the B address.

### Timing

Total time in microseconds

=  $21n + 35$ , where  $n$  is the number of characters in either operand (operands must be of equal length).

### Example

#### Instruction:

Operation	N	A Address	B Address
U	2	1003	1005

*HSM before Instruction is Executed:*

Memory Location	1002	1003	1004	1005
Bits within Each Location	1 00 0000	0 00 0111	0 11 0010	0 01 0101

*HSM after Instruction is Executed:*

Memory Location	1002	1003	1004	1005
Bits within Each Location	0 11 0010	1 01 0010	0 11 0010	0 01 0101

*Final Register Contents:*

$(A)_f = 1001$

$(B)_f = 1003$

*Time:*

$$(21 \times 2) + 35 = 77 \mu\text{s.}$$

## V Store Register (REG)

### General Description

This instruction places the contents of a specified register P, A, B, S, or U into a HSM location.

### Format

Operation — V

N — Register to be stored P, A, B, S, or U. The desired register is specified by the following chart.

Register to be Stored	None	P	A	B	S	U
N	0	1	2	4	8	&

**A Address** — Address of right hand diad of a two diad pair which is to receive the contents of the register specified by N if B, P, S, or U are to be stored. If A is to be stored, the contents of the A Register left by the previous instruction are stored in STA and the A address of this instruction is ignored.

**B Address** — HSM address of next instruction to be executed if P is being stored. If not P, the B address is zero (0000).

### Outline of Operation

The N character is examined in the N Register. If zero the instruction terminates. Otherwise the contents of the designated register are stored appropriately. If the N character selects the P Register, the P Register is stored in the location specified by the A Register and the contents of the B Register are sent to the P Register.

In the event the register selected is B, S, or U, the results are stored in the location designated by the A Register contents. When the B Register is stored, the B Address of the instruction is not staticized and the contents of the B Register resulting from the previous instruction are stored. In the case when the A Register is stored, the A address is not staticized and the contents of the A Register resulting from the previous instruction are stored in the STA standard memory location.

When the S Register is stored, the least significant diad of the S Register is placed in the location specified by the A Register. If a Simultaneous Instruction is being concurrently executed, the contents of the S Register may vary before the most significant diad is stored. The contents of the U Register may also change before being completely stored if a Record File Mode instruction is being concurrently executed.

### Final Register Contents

$(A)_f = (A)_i - 2$  if B, P, S, or U is stored; if A Register is stored or N equals zero,  $(A)_f$  of previous instruction.

$(B)_f = (B)_i$  if P, S, or U is stored; if A or B Register is stored or N equals zero,  $(B)_f$  of previous instruction.

### Timing

49  $\mu$ s

### Example

#### Instruction:

Operation	N	A Address	B Address
V	4	1005	0000

Assumption — Register B contains 2116 as a result of a prior operation.

#### HSM before Instruction is Executed:

1001	1002	1003	1004	1005
A	B	C	D	E

*HSM after Instruction is Executed:*

1001	1002	1003	1004	1005
A	2	1	1	6

*Final Register Contents:*

$(A)_f = 1003$

$(B)_f = 2116$

*Time:*

49  $\mu$ s.

## W Conditional Transfer of Control (CTC)

### General Description

This instruction senses the PRI's, the EF/ED, Overflow, and Interrupt Indicators, and the Simultaneous Mode. It can choose alternate sets of sequences of instructions.

### Format

Operation — W

N — Indicates element to be sensed according to the following chart:

N	Indicator Sensed
0	None
1	PRI's
2	Overflow Indicators
4	Simultaneous Indicator
8	EF/ED Normal Indicator
&	Interrupt Indicator
– (minus)	EF/ED Simultaneous Indicator

A Address — Contains the address of the next instruction if one of the following sets of conditions is true:

N = 1 and PRP set,

N = 2 and the First Overflow Indicator is set,

N = 4 and a "read" is in the simultaneous mode,

N = 8 and the EF/ED Normal Indicator is set,

N = & and the Interrupt Indicator is set (INT button on Console Panel is on), or

N = – and the EF/ED Simultaneous Indicator is set.

B Address — Contains the address of the next instruction if one of the following sets of conditions is true:

N = 1 and PRN is set,

N = 2 and neither Overflow Indicator is set,

N = 4 and a "write" is in the Simultaneous Mode,

N = 8 and the EF/ED Normal Indicator is not set,

N = & and the Interrupt Indicator is not set, or

N = – and the EF/ED Simultaneous Indicator is not set.

### Standard Location

STP (on Transfer only)

### Outline of Operation

The N character is examined in the N Register. The condition is sensed and either the contents of the A or B Register, as indicated above, are transferred to the P Register after the contents of the P Register are transferred to STP. The next instruction in sequence is performed if:

1.  $N = 0$ , a register is not being sensed.
2.  $N = 1$ , the PRI's are being sensed and PRZ is set.
3.  $N = 2$ , the Second Overflow Indicator is being sensed and is set.
4.  $N = 4$ , the Simultaneous Mode is being sensed and is found to be unoccupied.

The first Overflow Indicator is set when a one is in the  $2^4$  bit position of the MSD of the sum. The Second Overflow Indicator (present only in a 40,000 HSM) is set when a one is in the  $2^5$  bit position of the MSD of the sum.

### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f = (B)_i$$

### Time

49  $\mu\text{s}$  if a transfer of control takes place.

35  $\mu\text{s}$  if no transfer of control takes place.

## Y Compare Left (COM)

### General Description

This instruction is used to determine the relative magnitude of two operands of equal length. The resulting PRI settings permit alternate sequence of action.

### Format

Operation — Y  
N — Number (0-44) characters to be compared. (See Appendix VI-A)  
A Address — HSM address of leftmost character of first operand.  
B Address — HSM address of leftmost character of second operand.

### Description of Operation

Left to right.

### Outline of Operation

This instruction initially sets PRZ and operates in the following cycles:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM locations specified by the A and B Registers are transferred to the D<sub>2</sub> and D<sub>3</sub> positions of the D Register respectively. The contents of the A and B Registers are incremented by one. The contents of D<sub>2</sub> and D<sub>3</sub> are compared. If the contents of D<sub>2</sub> are greater than the contents of D<sub>3</sub>, PRP is set, and the instruction terminates. If the contents of D<sub>3</sub> are greater than the contents of D<sub>2</sub>, PRN is set, and the instruction terminates. If the contents of D<sub>2</sub> equal the contents of D<sub>3</sub>, the contents of the N Register are decremented by one, and the cycle is repeated.

### Final Register Contents

(A)<sub>f</sub> = Address of location one to the right of the last character compared in first operand.  
(B)<sub>f</sub> = Address of location one to the right of the last character compared in second operand.

### PRI

PRI set according to outline of operation.

### Timing

Total time in microseconds  
= 21n + 35, where n equals the number of characters compared.

### Example #1

#### Instruction:

Operation	N	A Address	B Address
Y	5	1001	1007

#### HSM before and after Instruction is Executed:

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
S	M	I	T	H	—	S	M	I	T	H	—

#### Final Register Contents:

(A)<sub>f</sub> = 1006  
(B)<sub>f</sub> = 1012

**PRI**

PRZ is set.

**Time:**

$$21(5) + 35 = 140 \mu\text{s}.$$

**Example #2**

**Instruction:**

Operation	N	A Address	B Address
Y	4	2000	2006

**HSM before and after Instruction is Executed:**

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011
1	2	4	5	6	-	1	2	3	6	9	-

**Final Register Contents:**

$$(A)_f = 2003$$

$$(B)_f = 2009$$

**PRI**

PRP is set.

**Time:**

$$(21) 3 + 35 \mu\text{s} = 98 \mu\text{s}.$$

**Example #3**

**Instruction:**

Operation	N	A Address	B Address
Y	4	3000	3005

**HSM before and after Instruction is Executed:**

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009
4	5	7	8	-	5	5	7	2	-

**Final Register Contents:**

$$(A)_f = 3001$$

$$(B)_f = 3006$$

**PRI**

PRN is set.

**Time:**

$$(21) 1 + 35 = 56 \mu\text{s}.$$

## **X Tally (TA)**

### **General Description**

This instruction permits looping through a sequence of operations by automatically reducing a pre-stored quantity each time control is transferred to the beginning of the sequence. When the quantity (always a positive numeric) has been exhausted, the Tally ends and the instruction following it is performed. The maximum value of the Tally quantity is 99.

### **Format**

Operation — X

N — 0 (Zero)

A Address — HSM address of the diad containing the quantity to be tested.

B Address — HSM location of next instruction to be performed if quantity being tested has not been exhausted.

### **Standard Location**

STP (on transfer only)

### **Outline of Operation**

The contents of the HSM diad specified by the A Register are transferred to the D Register. If the quantity is 00, the Tally ends and the next instruction in sequence is executed. If the quantity is other than 00, the contents of the D Register are decremented by one and stored in the HSM diad location specified by the A Register. The contents of the P Register are stored in STP, and the contents of the B Register are transferred to the P Register.

### **Final Register Contents**

$(A)_f = (A)_i$

$(B)_f = (B)_i$

### **Timing**

70  $\mu$ s — When Tally quantity is greater than zero upon starting.

49  $\mu$ s — When Tally quantity is equal to zero upon starting.

## ● Halt (HLT)

### General Description

This instruction inhibits the staticizing of any further instructions, halting the computer after completion of any instruction in the Simultaneous or Record File Modes.

### Format

Operation — . (period).

N            0 (Zero), may be used to designate type of stop.

A Address— 0000, may be used for numeric constants (0-9).

B Address— 0000, may be used for numeric constants (0-9).

### Outline of Operation

If the Simultaneous or Record File Mode is unoccupied the Computer stops immediately. If either of these two modes are occupied the instruction in these modes will be executed before stopping.

### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f = (B)_i$$

### Timing

35  $\mu$ s

## R REPEAT (RPT)

### General Description

This instruction causes all the instructions in sequence which precede a repeatable instruction to be repeated a specified number of times.

### Format

Operation – R

N – Number (0-14) of times to repeat the next repeatable instruction in sequence (See Appendix VI B).

A address – If zero (0000) or even, do not staticize A address when repeating the instruction. If one (0001) or odd, always staticize A address of the instruction.

B address – If zero (0000) or even, do not staticize B address when repeating the instruction. If one (0001) or odd, always staticize B address of the instruction.

### Standard Location

0222–0225

### Outline of Operation

The contents of the N Register are transferred to the  $N_R$  (Repeat) Register. The contents of the P Register are transferred to HSM locations 0222–0225. Indicators are set specifying whether or not the A and B addresses of the repeated instruction are to be staticized as denoted in the Repeat instruction's A and B addresses. The next instruction is then staticized and executed disregarding the settings of the indicators.

If the instruction following the Repeat instruction is a non-repeatable instruction, all successive non-repeatable instructions and the next repeatable instruction are staticized as specified by the indicators and executed.

If the instruction following the Repeat instruction is a repeatable instruction or when a repeatable instruction is encountered following a non-repeatable instruction, the sequence of instruction execution occurs in the following cycle.

The contents of the  $N_R$  Register are examined. If zero, the indicators are reset and the next instruction is executed. If other than zero, the contents of the  $N_R$  Register are decremented by one and the contents of the HSM locations 0222–0225 are transferred to the P Register. The instruction immediately following the RPT instruction is staticized as specified by the indicators and is executed. Henceforth, all successive non-repeatable instructions and the next repeatable instruction are staticized as specified by the indicators and executed. When the next repeatable instruction is again encountered, the cycle is repeated.

### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f = (B)_i$$

### Timing

49  $\mu$ s.

## S Input-Output Sense (IOS)

### General Description

This instruction tests the desired status of the selected input-output device, and chooses one of two sequences of instructions.

### Format

Operation – S

N – Selects the input-output device to be tested according to the following:

Device	N	
	Unit #1	Unit #2
Card Reader	(	:
Card Punch	)	
Paper Tape Reader	8	
Paper Tape Punch	9	
On-Line Printer	7	G
Data Disc File	R	Z
Data Record File (under control of DRFC Unit) <sup>1</sup>	R	Z
Data Record File (under DRFM Control Unit)	# \$ . ,	
Hi-Data Tape Group	1 2 3 4 5 6	A B C D E F
Dual Tape Channel (2x6 switch 33 or 66KC model) <sup>2</sup>	1 2 3 4 5 6	
Dual Tape Channel (2x12 switch 33 or 66KC model) <sup>3</sup>	123456 ABCDEF	
33KC Tape Adapter	J	N
66KC Tape Adapter	L	P

Note #1: Data Disc File #1 precludes the inclusion of Data Record File #1 operated through the DRFC. Data Disc File #2 precludes the inclusion of Data Record File #2 operated through the DRFC.

Note #2: The 2x6 Switch Dual Tape Channel precludes the inclusion of Hi-Data Tape Group #1.

Note #3: The 2x12 Switch Dual Tape Channel precludes the inclusion of both Hi-Data Tape Groups.

A Address – A<sub>0</sub> specifies the tests to be performed as follows:

Device	"1" bit in	Numeric Equival.	Tests
Card Reader or Punch	2 <sup>0</sup>	1	Is the selected device inoperable?
	2 <sup>1</sup>	2	Is the selected device operating?
Paper Tape Reader or Paper Tape Punch	2 <sup>0</sup>	1	Is the selected device inoperable?
	2 <sup>1</sup>	2	Is the selected device operating?

Device	"1" bit in	Numeric Equival.	Tests
On-Line Printer	2 <sup>0</sup>	1	Is the selected printer inoperable?
	2 <sup>1</sup>	2	Is a line being printed?
	2 <sup>4</sup>	&	Is the paper advancing?
Data Disc File	2 <sup>0</sup>	1	Is the selected device inoperable?
	2 <sup>1</sup>	2	Is the selected device operating?
	2 <sup>2</sup>	4	Is the track select complete?
Data Record File	2 <sup>0</sup>	1	Is the selected device inoperable?
	2 <sup>1</sup>	2	Is the selected device reading or writing?
	2 <sup>2</sup>	4	Is a record on the turntable of the selected Data Record File?
Magnetic Tape Station	2 <sup>0</sup>	1	Is the tape station inoperable?
	2 <sup>1</sup>	2	Is the tape in motion?
	2 <sup>2</sup>	4	Has ETW been sensed?
	2 <sup>3</sup>	8	Is the tape positioned on BTC?
	2 <sup>4</sup>	&	Is the tape moving in a reverse direction?

Depicts A<sub>0</sub> character when only one condition is being sensed. When the A<sub>0</sub> character contains the appropriate bits more than one condition may be sensed by a single IOS instruction.

A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub> – 000 (Zero)

B Address – HSM location of the next instruction to be executed if the condition or conditions being tested are present.

#### Standard Location

STP (on transfer only)

#### Outline of Operation

The test (or tests) called for by the one bits in A<sub>0</sub> are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

#### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f = (B)_i$$

#### Timing

49 μs if a transfer is executed.

35 μs if no transfer takes place.

## ○ Card Read Normal (CRN)

### General Description

This instruction reads information from punched cards in the Card Reader into the HSM. Facilities are provided for reading cards at 600, 300, or 200 cards per minute, or for single card feed on demand.

### Format

Operation – 0 (zero)

N – Selects the proper Card Reader and either determines the rate at which cards are to be read or is used in a card cycle ending routine, according to the following:

First Card Reader	Second Card Reader	Result
1	A	Reads single card or terminates continuous card reading cycle (600 cpm)
2	B	Used in continuous card ending routine (600 cpm)
4	D	Used in continuous card reading cycle (600 cpm)
M	U	Used in alternate card reading cycle (300 cpm)
8	H	Terminates alternate card reading cycle (300 cpm)

A Address – Address of HSM location to receive the first character read from punched cards. This address must be an even number (left hand end of a diad).

B Address – 0000 (zero).

### Direction of Operation

Left to right

### Outline of Operation

Initially and thereafter, as the need arises, the instruction automatically directs the Card Reader to place one or more cards in the read station and operates on successive characters in the following cycle:

The character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 code and is placed in HSM in the location specified by the A Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at  $(A)_i + 79$ .

In order to maintain a 600 card per minute rate, a Card Read instruction in which the N character is 4 or D (to denote the first or second card reader) must be executed for each card read. The successive card read instructions must be staticized before 100 milliseconds have elapsed. Approximately 80 milliseconds are required to read one card leaving 20 milliseconds of compute time between cards.

Continuous card reading is initiated when  $N=4$  (or D). Since only the first of the three cards in the card reader transport mechanism are read by this instruction, the continuous card reading cycle, must be terminated by two card read instructions in which the N characters are 2 and 1 (or B and A) respectively to avoid a "Feed" error.

The card feed rate may be accomplished at 300 cards per minute by staticizing successive card read instructions every 200 milliseconds for each card read. The N character in the card read instructions must be either M or U, depending upon whether the first or second card reader is addressed. Of this 200 millisecond card cycle, approximately 120 milliseconds are free for computing after the card has been read.

This Alternate Card Reading cycle must be terminated by a Card Read instruction in which the N=8 (or N=H).

When Card Read instructions are staticized in which the N character is 1, cards may be read at any rate up to 200 cards per minute. No terminating instruction is necessary since only one card has been fed into the Card Reader transport mechanism by this instruction.

Automatic card translation does not take place if the BCT button on the Computer Console Panel is in the "on" position. Each card column is then split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in columns 1 (row 9 = 2<sup>5</sup>, row 4 = 2<sup>0</sup>) is read into HSM at the location specified by the A Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at (A)<sub>i</sub> + 79. The character represented by column 1, rows 3 through Y (row 3 = 2<sup>5</sup>, row Y = 2<sup>0</sup>) is read into HSM at (A)<sub>i</sub> + 80. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at (A)<sub>i</sub> + 159. The final A Register setting is (A)<sub>i</sub> + 160.

**Final Register Contents**

- (A)<sub>f</sub> = One location to the right of the last character read into HSM.
- (B)<sub>f</sub> = (A)<sub>i</sub> with BCT off.
- (B)<sub>f</sub> = (A)<sub>i</sub> + 80 with BCT on.

**Timing**

*Bush!*

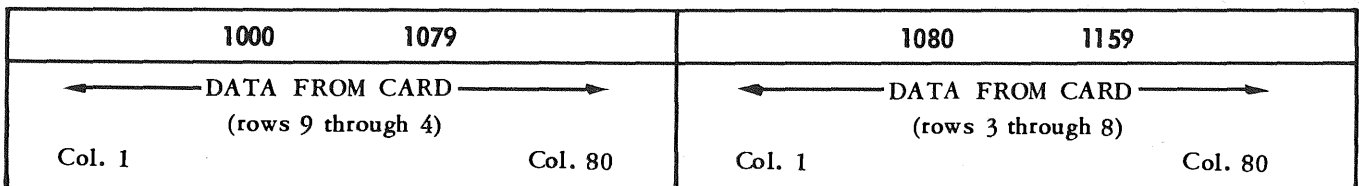
Card Feed Rate Per Minute	Time in Milliseconds	Time Free For Computing
600	100	20
300	200	120
up to 200	Min. 300	Min. 20

**Example**

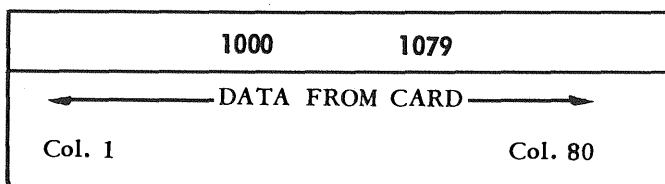
*Instruction:*

Operation	N	A Address	B Address
0	4	1000	0000

*HSM After Instruction is Executed (with BTC on):*



*HSM After Instruction is Executed (with BCT off):*



***Final Register Contents:***

(A)<sub>f</sub> = 1160 (BCT on)

(A)<sub>f</sub> = 1080 (BCT off)

(B)<sub>f</sub> = 1080 with BCT on

(B)<sub>f</sub> = 1000 with BCT off

***Time:***

100 milliseconds (20 milliseconds free for computing).

# 1 Card Read Simultaneous (CRS)

## General Description

This instruction reads information from punched cards in the card reader into the HSM in the Simultaneous Mode. Facilities are provided for reading cards at 600, 300 or 200 cards per minute, or for single card feed on demand.

## Format

Operation – 1

N – Selects the proper card reader and either determines the rate at which cards are to be read or is used in a card cycle ending routine, according to the following:

First Card Reader	Second Card Reader	Result
1	A	Reads single card or terminates continuous card reading cycle (600 cpm)
2	B	Used in continuous card ending routine (600 cpm)
4	D	Used in continuous card reading cycle (600 cpm)
M	U	Used in alternate card reading cycle (300 cpm)
8	H	Used in alternate card ending routine (300 cpm)

A Address – Address of HSM location to receive the first character read from punched cards. This address must be an even number (left-hand end of a diad).

B Address – 0000 (zeros)

## Direction of Operation

Left to right

## Outline of Operation

This instruction is initially staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to the SOR Register and the contents of the A and B Register are transferred to the S and T Registers, respectively.

This instruction operates in the Simultaneous Mode. Initially and therefore, as the need arises, this instruction automatically directs the Card Reader to place one or more cards in the read station and operates on successive characters in the following cycle:

The character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 code and is placed in the location specified by the S Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at (S)  $i + 79$ .

In order to maintain the 600 card per minute rate, a card read instruction in which the N character is 4 or D (to denote the first or second Card Reader) must be executed for each card read. The successive Card Read instructions must be staticized before 100 milliseconds have elapsed. Approximately 80 milliseconds are required to read one card leaving 20 milliseconds of compute time between cards.

Continuous card feeding is initiated when N=4 (or D). Since only the first of the three cards in the Card Reader transport mechanism are read by this instruction, the Continuous Card Reading cycle must be terminated by two Card Read instructions in which the N characters are 2 and 1 (or B and A) respectively to avoid a "feed" error.

The card feed rate may be accomplished at 300 cards per minute by staticizing successive Card Read instructions every 200 milliseconds for each card read. The N character in the Card Read instructions must be either M or U, depending upon whether the first or second card reader is addressed. Of this 200 millisecond card cycle, approximately 120 milliseconds are free for computing after the card has been read. This Alternate Card Reading cycle must be terminated by a Card Read instruction in which the N = 8 (or N = H).

When Card Read instructions are staticized in which the N character is 1, cards may be read at any rate up to 200 cards per minute. No terminating instruction is necessary since only one card has been fed into the Card Reader transport mechanism by this instruction.

Automatic card translation does not take place if the BCT button on the Computer Console Panel is in the "on" position. Each card column is then split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2<sup>5</sup>, row 4 = 2<sup>0</sup>) is read into HSM at the location specified by the S Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at (S)i + 79. The character represented by column 1, rows 3 through Y (row 3 = 2<sup>5</sup>, row Y = 2<sup>0</sup>), is read into HSM at (S)i + 80. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at (S)i + 159. The final S Register setting is (S)i + 160.

**Final Register Contents**

(S)<sub>f</sub> = One location to the right of the last character read into HSM.

(T)<sub>f</sub> = (A)<sub>i</sub> with BCT off.

(T)<sub>f</sub> = (A)<sub>i</sub> + 80 with BCT on.

**Timing**

Card Feed Rate Per Minute	Time in Milliseconds	Time Free For Computing
600	100	20
300	200	120
up to 200	Min. 300	Min. 20

## 2 Card Punch Normal (CPN)

### General Description

This instruction enables the Model 334 Card Punch to punch 80-column cards from information contained in the HSM. (See subsequent instruction for programming the Model 336 Card Punch).

### Format

- Operation – 2
- N – 0 (zero)
- A Address – HSM address of first character to be punched.
- B Address – HSM address of last character to be punched.

### Direction of Operation

Left to right

### Standard Location

0202–0205

### Outline of Operation

A start signal is sent to the Card Punch. The Card Punch punches the information from HSM between and including the locations addressed by the contents of the A and B Registers, punching 80 columns to a card. When the A and B Registers are equal, the last card is punched and the contents of the A Register are incremented by one.

The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of punching.

### Final Register Contents

(A)<sub>f</sub> = Address of location one to the right of the last character in HSM punched.

(B)<sub>f</sub> = B<sub>i</sub>

### Timing

Cards are punched at the rate of 100 cards per minute.

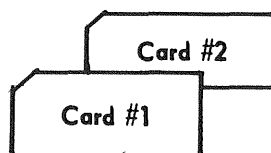
### Example

#### Instruction:

Operation	N	A Address	B Address
2	0	1000	1159

1000		1079		1080		1159
-	Card	-	Card	-	Card	-
	#1		#2			

Punched



***Final Register Contents:***

$$(A)_f = 1160$$

$$(B)_f = 1159$$

***Time:***

**1.2 seconds**

## 2 Card Punch Normal (CPN)

### General Description

This instruction enables the Model 336 Card Punch to punch 80-column cards from information contained in the HSM. (See preceding instruction for programming the Model 334 Card Punch.)

### Format

Operation – 2

N – Determines the rate at which cards are to be punched, or is used in a card cycle ending routine.

N	PURPOSE
1	Demand card punching, or to terminate continuous card punching
2	Used in continuous card punching ending routine
4	Continuous card punching

A Address – HSM address of first character to be punched.

B Address – 0000 (Zeros)

### Direction of Operation

Left to right

### Standard Location

0202–0205

### Outline of Operation

A start signal is sent to the Card Punch. Initially and thereafter, as the need arises, this instruction automatically directs the Card Punch to place one or more cards in the punch station and operates on successive characters in the following cycle.

The Card Punch punches all the information from the HSM location addressed by the A Register through the next 79 HSM locations. 80 characters are punched in each card. After the card is punched, it is immediately read to verify punching accuracy and placed in the output stacker.

### Final Register Contents

$$(A)_f = (A)_i + 80$$

$$(B)_f = (B)_i$$

### Timing

Cards are punched at a rate of up to 200 cards per minute.

### 3 Card Punch Simultaneous (CPS)

#### General Description

The instruction enables the Card Punch Model 334 to punch 80-column cards from information contained in the HSM, using the Simultaneous Mode. (See subsequent instruction for programming the Model 336 Card Punch).

#### Format

Operation – 3

N – 0 (zero)

A Address – HSM address of first character to be punched.

B Address – HSM address of last character to be punched.

#### Direction of Operation

Left to right.

#### Standard Location

0202–0205

#### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to SOR Register, and the contents of the A and B Registers are transferred to the S and T Registers respectively, and this instruction is executed in the Simultaneous Mode. The operation of the instruction is as follows:

A start signal is sent to the Card Punch. Punching by the Card Punch is initiated and continues until all the characters between and including the HSM locations specified by the S and T Registers are punched. When the contents of the S and T Registers are equal, the last card is punched and the contents of the S Register are incremented by one. The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of the punching.

#### Final Register Contents

$(S)_f = \text{HSM address of location one to the right of the last character in HSM punched.}$

$(T)_f = (B)_i$

#### Timing

Cards are punched at the rate of 100 cards per minute.

### 3 Card Punch Simultaneous (CPS)

#### General Description

This instruction enables the Model 336 Card Punch to punch 80-column cards from information contained in the HSM, using the Simultaneous Mode. (See preceding instruction for programming the Model 334 Card Punch).

#### Format

Operation – 3

N – Determines the rate at which cards are to be punched, or is used in card cycle ending routine.

N	PURPOSE
1	Demand card punching, or to terminate continuous card punching
2	Used in continuous card punching ending routine
4	Continuous card punching

A Address – HSM address of first character to be punched.

B Address – 0000 (zeros)

#### Direction of Operation

Left to right

#### Standard Location

0202–0205

#### Outline of Operation

A start signal is sent to the Card Punch. Initially and thereafter, as the need arises, this instruction automatically directs the Card Punch to place one or more cards in the punch station and operates on successive characters in the following cycle.

The Card Punch punches all the information from the HSM location addressed by the S Register through the next 79 HSM locations. 80 characters are punched in each card. After the card is punched, it is immediately read to verify punching accuracy and placed in the output stacker.

#### Final Register Contents

$$(S)_f = (A)_i + 80$$

$$(T)_f = (B)_i$$

#### Timing

Cards are punched at a rate of up to 200 cards per minute.

## 4 Tape Read Forward Normal (RFN)

Repeatable

### General Description

This instruction brings a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. When reading gapless paper tape, transfer begins with the first character and ends when a gap is sensed or the specified HSM area is filled.

### Format

Operation - 4

N - Identification character of tape station or Paper Tape Reader. (See Appendix VII).

A Address - Address of HSM location which is to receive the first character of the block.

B Address - Address of HSM location which is to receive the last character read.

### Direction of Operation

Left to right

### Standard Location

STA (0212-0215)

### Direction of Tape Motion

Forward

### Outline of Operation

Initially this instruction sends a start signal to the input unit specified by the contents of the N Register. When this input unit is a tape station or the Paper Tape Reader the first character following a gap, or the next character of gapless paper tape, is then placed in the input buffer and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the input buffer is transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are incremented by one. If the comparison proved equal and a gap is passed in sequence, PRZ is set, and the instruction terminates. If the comparison proved equal and a gap is not passed, PRP is set, and the instruction terminates. However, the tape movement continues to gap unless gapless paper tape is being read. If the comparison proved not equal and a gap is passed in sequence, PRN is set, and the instruction terminates. If the comparison proved not equal and a gap is not passed the cycle is repeated.

When reading 66 KC magnetic tape two characters are transferred from tape to the input buffer and then to HSM, and the A Register is incremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from magnetic tape, the EF/ED Normal Indicator is set.

### Final Register Contents

(A)<sub>f</sub> = One location to the right of the last character read into HSM.

(B)<sub>f</sub> = (B)<sub>i</sub>

### PRi (TAPE)

PRP: The A and B Registers are equal before a gap has been found on tape.

PRN: A gap has been found on tape and the A and B Registers are unequal.

PRZ: At the time a gap has been found on tape the A and B Registers are equal.



*HSM before Instruction is Executed:*

2000	2001	2002	2003	2004	2005	2006	2007	2008
2	5	7	9	1	-	J	1	M

*HSM after Instruction is Executed:*

2000	2001	2002	2003	2004	2005	2006	2007	2008
1	3	4	6	2	-	J	1	M

*Final Register Contents:*

(A)<sub>f</sub> = 2005

(B)<sub>f</sub> = 2004

*PRI*

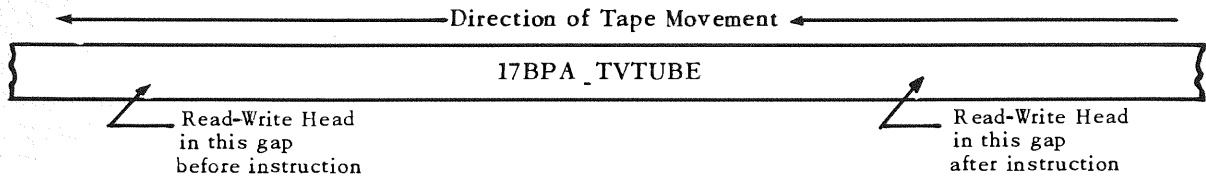
PRP is set

**Example #3**

*Instruction:*

Operation	N	A Address	B Address
4	P	4000	4050

*Tape on Station P*



*HSM before the Instruction is Executed:*

4000 - 4050 is filled with spaces

*HSM after the Instruction is Executed:*

4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012 -- 4050
1	7	B	P	A	-	T	V	T	U	B	E	-----

*Final Register Contents:*

(A)<sub>f</sub> = 4012

(B)<sub>f</sub> = 4050

*PRI*

PRN is set

## 5 Tape Read Forward Simultaneous (RFS)

### General Description

This instruction brings a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specific HSM area is filled. When reading gapless paper tape, transfer begins with the first character and ends when a gap is sensed or the specified HSM area is filled. This instruction is performed in the Simultaneous Mode.

### Format

Operation – 5

N – Identification character of tape station or Paper Tape Reader. (See Appendix VII).

A Address – Address of location in HSM which is to receive the first character on tape.

B Address – Address of location in HSM which is to receive the last character read from tape.

### Direction of Operation

Left to right.

### Direction of Tape Motion

Forward

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the input unit specified by the contents of the M Register. The first character following a gap on tape or the next character on gapless paper tape is placed in the tape buffer, and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the input buffer is transferred to the HSM location specified by the S Register. The contents of the S Register are compared with the contents of the T Register. The contents of the S Register are incremented by one. If a gap is passed in sequence, the instruction terminates. If the comparison proved equal and a gap is not passed, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

When reading 66 KC magnetic tape two characters are transferred from tape to the input buffer and then to HSM, and the S Register is incremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from tape, the EF/ED Simultaneous Indicator is set.

When a character is in the tape buffer, the instruction in the Normal Mode will be interrupted at the earliest possible moment.

### Final Register Contents

$(S)_f =$  One location to the right of the last character read into HSM.

$(T)_f = (B)_i$

### Timing

Hi-data tapes are read at the rate of 10 KC.

Paper tape is read at the rate of up to 1000 characters per second.

The tape station attached to the Tape Adaptor or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

**General Description**

This instruction transfers a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. Though the tape moves in reverse, the characters will be placed in their proper relative position within HSM.

**Format**

Operation – 6

N – Identification character of tape station or Paper Tape Reader. (See Appendix VII).

A Address – Address of HSM location to receive the first character from tape.

B Address – Address of HSM location to receive the last character read from tape.

**Direction of Operation**

Right to left

**Standard Location**

STA (0212-0215)

**Direction of Tape Motion**

Magnetic tape moves in a reverse direction. Paper Tape will be moved in a forward direction, but the characters read from paper tape will be placed in memory from right to left.

**Outline of Operation**

Initially this instruction sends a start signal to the input unit specified by the contents of the N Register. After a gap is passed on magnetic tape, the first character is placed in the tape buffer, and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the tape buffer is transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are decremented by one. If the comparison proved equal and a gap is passed in sequence, PRZ is set, the instruction terminates. If the comparison proved equal and a gap is not passed, PRP is set, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is passed in sequence, PRN is set, the instruction terminates. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

When reading 66 KC magnetic tape, two characters are transferred from tape to the input buffer and then to HSM, and the A Register is decremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from magnetic tape, the EF/ED Normal Indicator is set.

If ETW is passed the ETW flip-flop is reset.

**Final Register Contents**

$(A)_f =$  Address of location one to the left of the last characters read.

$(B)_f = (B)_i$

**PRI**

PRP: The A and B Registers are equal before a gap has been found on tape.

PRN: A gap has been found on tape and the A and B Registers are unequal.

PRZ: The A and B Registers are equal at the time a gap has been found on tape.

**Timing**

Hi-Data tapes are read at the rate of 10 KC.

Paper tape is read at the rate of up to 1000 characters per second.

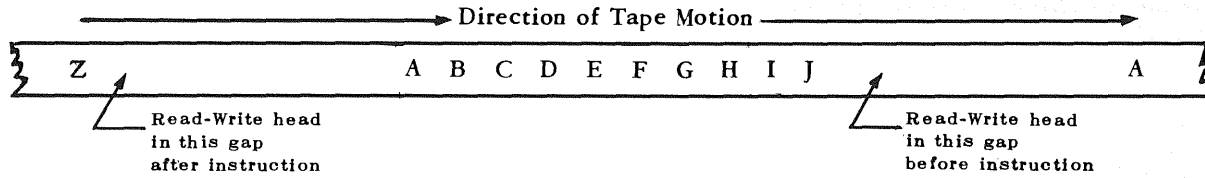
The tape station connected to the Tape Adaptor or Dual Tape Channel is read at the rate of 33.3KC if it is a Model 581 Tape Station, or 66.7 KC if it is a Model 582 Tape Station.

**Example**

*Instruction:*

Operation	N	A Address	B Address
6	3	2030	2021

*Tape on Station # 3:*



*HSM before Instruction is Executed:*

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
-	-	-	-	-	-	-	-	-	-

*HSM after Instruction is Executed:*

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
A	B	C	D	E	F	G	H	I	J

*Final Register Contents:*

$(A)_f = 2020$

$(B)_f = 2021$

*PRI*

PRZ is set

## 7 Tape Read Reverse Simultaneous (RRS)

### General Description

This instruction transfers a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. Though the tape moves in reverse, the characters will be placed in their proper relative position within HSM. This instruction operates in the Simultaneous Mode.

### Format

Operation – 7

N – Identification character of tape station or Paper Tape Reader. (See Appendix VII).

A Address – Address of HSM location to receive the first character from tape.

B Address – Address of HSM location to receive the last character read from tape.

### Direction of Operation

Right to left.

### Direction of Tape Motion

Magnetic tape moves in a reverse direction. Paper tape will move in the forward direction but characters read from paper tape are placed in memory from right to left.

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the input unit specified by the contents of the M Register. After a gap is passed on magnetic tape, the first character is placed in the input buffer, and this instruction operates in the following cycle:

The character in the input buffer is transferred to the HSM location specified by the S Register. The contents of the S Register are decremented by one. If a gap is passed in sequence, the instruction terminates. If the comparison proves equal and a gap is not passed, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

If an EF or ED alone is read from magnetic tape, the EF/ED Simultaneous Indicator is set.

If ETW is passed the ETW flip-flop is reset.

When an instruction is processing in the Normal Mode, it will be interrupted at the earliest possible moment.

### Final Register Contents

$(S)_f$  = Address of location one to the left of the last character read.

$(T)_f = (B)_i$

### Timing

Hi-data tapes are read at the rate of 10 KC.

Paper tape is read at the rate of up to 1000 characters per second.

The tape station attached to the Tape Adaptor or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

## 8 Tape Write Normal (TWN)

### General Description

This instruction transfers a specified series of consecutive characters in HSM to a designated Tape Station, the Paper Tape Punch, or Monitor Printer.

### Format

Operation – 8

N – Identification character of tape station, Paper Tape Punch, or Monitor Printer.  
(See Appendix VII).

A Address – Address of the first location in HSM to be written, punched, or typed.

B Address – Address of the last character in HSM to be written, punched, or typed.

### Direction of Operation

Left to right

### Tape Motion

Forward

### Outline of Operation

Initially this instruction sends a start signal to the output unit specified by the contents of the N Register and operates in the following cycle:

The contents of the HSM location specified by the A Register are transferred to the output unit specified by the N Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

### Final Register Contents

$(A)_f =$  Address of location one to the right of the last character written, punched or typed.

$(B)_f = (B)_i$

### Timing

Hi-data tapes are written at the rate of 10 KC. Paper tape is punched at the rate of up to 100 characters per second.

The tape station attached to the Tape Adaptor or Dual Tape Channel is written at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

The Monitor Printer types at the rate of 10 characters per second.

### Example

*Instruction:*

Operation	N	A Address	B Address
8	1	4001	4005

*HSM before and after instruction is Executed:*

4000	4001	4002	4003	4004	4005	4006
–	A	B	C	D	E	–



## 9 Tape Write Simultaneous (TWS)

### General Description

This instruction transfers a specified series of consecutive characters in HSM to a designated tape station, the Paper Tape Punch, or Monitor Printer. This instruction operates in the Simultaneous Mode.

### Format

Operation – 9

N – Identification character of tape station, Paper Tape Punch, or Monitor Printer.  
(See Appendix VII).

A Address – HSM location of the first character to be written, punched, or typed.

B Address – HSM location of the last character to be written, punched, or typed.

### Direction of Operation

Left to right

### Direction of Tape Motion

Forward

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the output unit specified by the contents of the M Register and operates in the following cycle:

The contents of the HSM location specified by the S Register are transferred to the output unit specified by the M Register. The contents of the S Register are compared with the contents of the T Register. The contents of the S Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

When an instruction is processing in the Normal Mode, it will be interrupted at the earliest possible moment.

### Final Register Contents

$(S)_f =$  Address of location one to the right of the last character written, punched, or typed.

$(T)_f = (B)_i$

### Timing

Hi-data tapes are written at the rate of 10 KC.

Paper tape is punched at the rate of up to 100 characters per second.

The tape station attached to the Tape Adaptor or Dual Tape Channel is written at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

The Monitor Printer types at the rate of 10 characters per second.

## **; Rewind to BTC (RWD)**

### **General Description**

This instruction causes a designated magnetic tape unit to be completely rewound. Once the operation has been initiated the rewind proceeds totally independent of the Computer, not occupying the Normal, Simultaneous, nor Record File Mode. The Computer, after initiating the rewind, is free to execute other instructions.

### **Format**

Operation – ;

N – Identification character of tape station. (See Appendix VII).

A Address – 0000 (Zero)

B Address – 0000 (Zero)

### **Direction of Tape Motion**

Reverse

### **Final Register Contents**

After rewind is initiated, the registers are available for use by the next instruction.

## B Print & Paper Advance Normal (PAN)

### General Description

This instruction can cause the contents of 120 or 160 consecutive HSM locations to be transferred to the On-Line Printer, initiating the printing of one line. It can advance paper a specified number of lines according to the contents of N, or by the punches in the paper tape loop of the printer.

### Format

Operation – B

N – Number of lines (0-14) to advance paper if  $B_3$  equals 1:

	Asynchronous Mode														Synchronous Mode*	
Number of lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1
First Printer	0	1	2	3	4	5	6	7	8	9	space	#	@	(	)	J
Second Printer	&	A	B	C	D	E	F	G	H	I	+	.	;	:	'	/

\* $B_3$  must equal 1

A Address – 0000 (Zero)

B Address – Address of data to be printed from HSM excluding  $B_3$ .

$B_0$  – MSD of address.

$B_1$  – When this digit is even, printing will occur. If odd, the line will not be printed.

$B_2$  – Always zero.

$B_3$  – Has the function of indicating the type of paper advance as follows:

Type of Paper Advance	$B_3$
No Paper Advance	0
Paper Advance Using N Register as count	1
Vertical Tab (using tape loop)	2
Page change (using tape loop)	3

### Direction of Operation

Left to right.

### Outline of Operation

The paper advance information given by  $B_3$  is stored in indicators. The  $B_3$  character is set to zero. If printing is to take place the contents of the B Register are transferred to the A Register. As the print drum revolves, the printer sends signals to the Computer indicating which character on the print drum will next be in the print position. These printer signals are used to develop an address for an automatic table lookup operation.

This operation extracts from the Print Table (see Appendix VIII) the RCA 301 character which is to be printed next. This character is stored in the Print Register. The diad addressed by the A Register is read out of HSM and checked for the character stored in the Print Register. The contents of the A Register are increased by two and the cycle is repeated. Modification of the contents of the A Register and checking of the addressed diad continue until 120 or 160 consecutive memory locations have been checked. This checking for one character is known as a "scan".

As each character is checked a one bit is sent to the printer shift register for an equality, a zero bit is sent for each non-equality. At the completion of a scan the shift register contains a one bit in every position on the line in which this character is to be printed. The one bits are then used to trigger the corresponding print hammers. The contents of the B Register are again transferred to the A Register, a new character is read from the Print Table, and another scan is begun.

There are two modes of operation, Synchronous and Asynchronous. The Synchronous Mode permits only 47 characters to be printed since a complete line of print and paper advance to the next print line is accomplished during each revolution of the print drum. The letter "A" is always the first character for which HSM is scanned, and the period is the last.

The Asynchronous Mode permits all 64 characters on the print drum to be printed (120 or 160 characters per line) in one full revolution, and paper advance occurs in a portion of the next print drum revolution. Scanning can proceed with the next character in sequence on the print drum at the conclusion of the paper advance function.

Appendix VIII shows print table containing RCA 301 characters. The code  $(17)_8$  is used to inhibit printing of certain characters on the print drum. An inhibited character may be used to specify a non-represented RCA 301 character by substituting the RCA 301 character's bit configuration into the proper print table position. For example, the EB symbol may be printed as "+" by inserting  $(72)_8$  in the thirty-third position of the print table.

#### Final Register Contents

$(A)_f$  = Address of location one to the right of the last character printed if printing is done, otherwise it is

$(A)_i$ .

$(B)_f = (B)_i$  with  $B_3$  set to zero.

#### Timing

Print and paper advance of one line takes 60 ms. in the Synchronous Mode or 76 ms. in the Asynchronous Mode. When more than one line is to be advanced, paper advancing is done at the rate of 150 lines per second after the first line.

#### Example:

##### Instruction:

Operation	N	A Address	B Address
B	1	0000	1201

##### HSM before and after Instruction is Executed:

(First Character Printed)		(Last Character Printed)	
1200	1201	1318	1319
1	2	8	9

Paper is advanced one line after the printing of the line.

*Final Register Contents:*

(A)<sub>f</sub> = 1320

(B)<sub>f</sub> = 1200

*Time:*

76 ms.

## C Print and Paper Advance Simultaneous (PAS)

### General Description

This instruction can cause the contents of 120 or 160 consecutive HSM locations to be transferred to the On-Line Printer, initiating the printing of one line. It can advance the paper a specified number of lines designated by N or by the punches of the paper tape loop of the printer. This instruction is executed in the Simultaneous Mode.

### Format

Operation – C

N – Number of lines (0-14) to advance paper if  $B_3$  equals 1:

	Asynchronous Mode															Synchronous Mode*
Number of lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1
First Printer	0	1	2	3	4	5	6	7	8	9	space	#	@	(	)	J
Second Printer	&	A	B	C	D	E	F	G	H	I	+	-	;	:	'	/

\* $B_3$  must equal 1

A Address – 0000 (zero)

B Address – Address of the data to be printed from HSM except for  $B_3$ .

$B_0$  – MSD of address.

$B_1$  – When this digit is even, printing will occur. If odd, the line will not be printed.

$B_2$  – Always zero.

$B_3$  – Has the function of indicating the type of paper advance as follows:

Type of Paper Advance	$B_3$
No paper advance	0
Paper advance using N Register as count	1
Vertical Tab (using tape loop)	2
Page Change (using tape loop)	3

### Direction of Operation

Left to right

### Outline of Operation

The paper advance information given by  $T_3$  is stored in indicators. The  $T_3$  character is set to zero. If printing is to take place the contents of the T Register are transferred to the S Register. As the print drum revolves, the printer sends signals to the Computer indicating which character on the print drum will next be in the print position.

These printer signals are used to develop an address for an automatic table look-up operation. This operation extracts from the Print Table (see Appendix VIII) the RCA 301 character which is to be printed next. This character is stored in the Print Register. The diad addressed by the S Register is read out of HSM and checked for the character stored in the Print Register. The contents of the S Register are increased by two and the cycle is repeated. Modification of the contents of the S Register and checking of the addressed diad continue until 120 or 160 consecutive memory locations have been checked. This checking for one character is known as a "scan".

As each character is checked a one bit is sent to the printer shift register for an equality, a zero bit is sent for each non-equality. At the completion of a scan the shift register contains a one bit in every position on the line in which this character is to be printed. The one bits are then used to trigger the corresponding print hammers. The contents of the T Register are again transferred to the S Register, a new character is read from the translate table, and another scan is begun.

There are two modes of operation, Synchronous and Asynchronous. The Synchronous Mode permits only 47 characters to be printed since a complete line of print and paper advance to the next print line is accomplished during each revolution of the print drum. The letter "A" is always the first character for which HSM is scanned, and the period is the last.

The Asynchronous Mode permits all 64 characters on the print drum to be printed (120 or 160 characters per line) in one full revolution, and paper advance occurs in a portion of the next print drum revolution. Scanning can proceed with the next character in sequence on the print drum at the conclusion of the paper advance function.

Appendix VIII shows a print table containing RCA 301 characters. The code  $(17)_8$  is used to inhibit printing of certain characters on the print drum. An inhibited character may be used to specify a non-represented RCA 301 character by substituting the RCA 301 character's bit configuration into the proper print table position. For example, the EB symbol may be printed as "÷" by inserting  $(72)_8$  in the thirty-third position of the print table.

#### Final Register Contents

$(S)_f$  = Address of location one to the right of the last character printed if printing is done; otherwise, it is  $(A)_i$ .

$(T)_f = (B)_i$  with  $B_3$  set to zero.

#### Timing

Print and paper advance of one line takes 61.5 ms. in the Synchronous Mode or 77.4 ms. in the Asynchronous Mode. When more than one line is to be advanced, paper advancing is done at the rate of 150 lines per second after the first line.

## D Band Select Normal (BSN)

### General Description

This instruction initiates a search of the Data Record File under the control of the Processor for the record containing the selected band, puts the record on the turntable, and positions the arm over the correct band. Once initiated, the record and band will be selected independent of Computer operation.

### Format

Operation - D

N - Selects the Data Record File Unit and Band as indicated below:

1st File	2nd File	
0	&	The record on the turntable, if any, will be returned to the cage. The desired record is then placed on the turntable and the indicated band selected.
1	A	The band selected is one of the two on the upside of the record on the turntable. If the B address is even, the first band will be selected; if odd, the second band will be selected.

A Address - 0000 (zero)

B Address - B<sub>0</sub> 0 (zero); B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub> designate band (000 to 511).

### Outline of Operation

Band addresses are numbered from 000 through 511 and are specified by the last three digits of the B address. The contents of the N Register designate the proper Data Record File and specify whether the record on the turntable, if any, is to be returned to the cage or not.

### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f = (B)_i$$

### Timing

To initiate selection (in microseconds):  $21(B_1) + 14(B_2) + 42$ .

To perform Band Selection, 2.25 seconds (average).

## E Band Select Record File Mode (BSM)

### General Description

This instruction selects a band from one of the four Data Record File Units controlled by the Record File Mode Control Unit. Once initiated, the band will be selected independently of the Computer operation.

### Format

Operation – E

N – Selects the Data Record File Unit and Band as indicated below:

Data Record File Unit				Effect
1	2	3	4	
0	&	–	”	The record on the turntable, if any, will be returned to the cage. The desired record is then placed on the turntable and the indicated band selected.
1	A	J	/	The band selected is one of the two on the upside of the disc on the turntable. If the B address is even, the first band will be selected; if odd, the second band will be selected.

A Address – 0000 (zero)

B Address – B<sub>0</sub> 0 (zero) B<sub>1</sub>, B<sub>2</sub>, and B<sub>3</sub> designate band (000 to 511).

### Outline of Operation

Band addresses are numbered from 000 through 511, and are specified by the last three digits of the B address. The contents of the N Register designate the proper Record File and specify whether the record on the turntable, if any, is to be returned to the cage or not.

### Final Register Contents

$$(A)_f = (A)_i$$

$$(B)_f \neq (B)_i$$

### Timing

To initiate selection (in microseconds):  $21(B_1) + 14(B_2) + 42$ .

To perform Band Selection, 2.25 seconds (average).

## F Block Read Record Normal (BRN)

### General Description

This instruction reads from a selected cell of the Data Record File to a designated HSM location. From one to ten blocks of information may be transferred from the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information to be transferred. In reading, the end of the block of information is designated by an EB symbol, or a count of 900 characters in the cell.

### Format

Operation – F

N – Selects the Data Record File Unit and number of blocks to be read as indicated below:

<b>Number of Blocks to be Read</b>	1	2	3	4	5	6	7	8	9	10
<b>First File</b>	1	2	3	4	5	6	7	8	9	0
<b>Second File</b>	A	B	C	D	E	F	G	H	I	&

A Address – HSM address where first character is to be placed.

B Address – B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd—record returned to cage.

B<sub>1</sub> = even—record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB is sensed or not.

B<sub>2</sub> = 1 – block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 – count or EB recognition.

If EB sensed before 900 characters have been read stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

### Direction of Operation

Left to right in HSM.

### Standard Location

STA (0212-0215)

### Outline of Operation

A start signal is sent to the Data Record File and the read-write head is placed on the record on the turntable. The contents of the cell specified in B<sub>3</sub> are transferred to the Record File Buffer and from the buffer to the HSM location designated by the A Register. Transfer is accomplished one character at a time, with the contents of the A Register being incremented by one after each character transferred. When the end of a block is reached, determined by B<sub>2</sub>, N is decreased by one. When N is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional read or write instructions from the same surface.

**Final Register Contents**

$(A)_f$  = Address of HSM location one to the right of the last character put in memory.

$(B)_f = (B)_i$

**Timing**

Characters are read at the rate of 2.5 KC. The average time to get to and read one selected cell is 2.6 seconds. It takes 1.5 seconds to return the record to the cage.

## G Block Read Record Simultaneous (BRS)

### General Description

This instruction reads from the Data Record File controlled by the Record File Control Unit to a designated HSM location. From one to ten blocks of information may be transferred from the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information to be transferred. In reading, the end of the block of information is designated by an EB symbol, or a count of 900 characters in the cell. This instruction is performed in the Simultaneous Mode.

### Format

Operation – G

N – Selects the Data Record File Unit and number of blocks to be read as indicated below:

Number of Blocks to be Read	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address – HSM location where first character is to be placed.

B Address – B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd—record returned to cage.

B<sub>1</sub> = even—record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB sensed or not.

B<sub>2</sub> = 1 — block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 — count or EB recognition.

If EB sensed before 900 characters have been read stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

### Direction of Operation

Left to right

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B registers are transferred to the SOR, M, S, T registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Record File. The contents of the cell specified in T<sub>3</sub> are transferred to the Record File Buffer and when the Normal Mode is interruptable, from the buffer to the HSM location designated by the S Register. Transfer is accomplished one character at a time, with the contents of the S Register being incremented by one after each character transferred. When the end of a block is reached, determined by T<sub>2</sub>, M is decreased by 1. When M is decreased to zero, the operation is terminated. The record does not have to be returned to the cage to perform additional read or write instructions on the same surface.

**Final Register Contents**

$(S)_f$  = Address of HSM location one to the right of the last character put in memory.

$(T)_f = (B)_i$

**Timing**

Characters are read at the rate of 2.5 KC. The average time to get to and read a selected cell is 2.6 seconds. The time to return the record to the cage is 1.5 seconds.

## H Block Write Record Normal (BWN)

### General Description

This instruction writes from a selected HSM location to designated cells of the Data Record File under control of the Record File Control Unit. From one to ten blocks of information may be transferred to the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information. In writing, a block is terminated by an End of Block (EB) Symbol or a cell count of 900 characters.

### Format

Operation – H

N – Selects the Data Record File Unit and number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address – HSM address of first character to be written to the Record File.

B Address – B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd – record returned to cage.

B<sub>1</sub> = even – record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB sensed or not.

B<sub>2</sub> = 1 — block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 count or EB recognition.

If EB sensed before 900 characters have been written stop transfer into this cell. If 900 count reached before an EB sensed, stop transfer into this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

### Direction of Operation

Left to right.

### Outline of Operation

A start signal is sent to the Data Record File and the arm is placed on the previously selected record on the turntable. The contents of the HSM location specified by the A address are transferred to the Data Record File Buffer and from the buffer to the specified cell. The contents of the A Register are incremented by one, and the contents of the next memory location are then transferred. When the end of a block is reached, determined by B<sub>2</sub>, N is decreased by one. When N is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional read or write instructions to the same surface.

**Final Register Contents**

$(A)_f$  = Address of HSM location one to the right of the last character written.

$(B)_f = (B)_i$

**Timing**

Characters are written at the rate of 2.5 KC. The average time to get to and write to a selected cell is 2.6 seconds. The time to return a record to the cage is 1.5 seconds.

# I Block Write Record Simultaneous (BWS)

## General Description

This instruction writes from a designated HSM location to selected Data Record File cells. From one to ten blocks of information may be transferred to the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information. In writing, a block is terminated by an End of Block (EB) Symbol or a cell count of 900 characters. This instruction is performed in the Simultaneous Mode.

## Format

Operation – I

N – Selects the Data Record File Unit and the number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address – HSM address of first character to be written.

B Address – B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd—record returned to cage.

B<sub>1</sub> = even—record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB sensed or not.

B<sub>2</sub> = 1 — block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer to this cell. If 900 count reached before an EB sensed, stop transfer to this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

## Direction of Operation

Left to right.

## Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B registers are transferred to the SOR, M, S, T registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Data Record File and the arm is placed on the previously selected record on the turntable. As soon as the normal mode is interruptable, the contents of the HSM location specified by the S Register are transferred to the Record File Buffer and from the buffer to the specified cell. The contents of the S Register are increased by one and the contents of the HSM location now addressed by the S Register are transferred in a like manner. When the end of a block is reached, determined by T<sub>2</sub>, M is decreased by one. When M is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional reads or writes to the same surface.

**Final Register Contents**

(S)<sub>f</sub> = HSM address of location one to the right of the last character written.

(T)<sub>f</sub> = (B)<sub>i</sub>

**Timing**

Characters are written at the rate of 2.5 KC. The average time to get to and write to a cell is 2.6 seconds. The time to return a record to the cage is 1.5 seconds.

## \* Record File Mode Read (RMR)

### General Description

This instruction reads from selected cells located in one of the four Data Record Files connected to the Data Record File Mode Control Unit. From one to ten blocks of information may be transferred from a Data Record File and placed in HSM with one instruction. Each cell may contain a block of information consisting of from one to 900 characters. In reading, the end of the block is designated by an EB symbol or a count of 900 characters in the cell.

### Format

Operation — \*

N — Selects the Data Record File Unit and the number of blocks to be read as indicated below:

Number of Blocks to be Read	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&
Third File	J	K	L	M	N	O	P	Q	R	- minus
Fourth File	V	S	T	U	V	W	X	Y	Z	"

A Address — HSM location where first character is to be placed.

B Address — B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd—record returned to cage.

B<sub>1</sub> = even—record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB sensed or not.

B<sub>2</sub> = 1 — block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

### Direction of Operation

Left to right in HSM.

### Outline of Operation

A start signal is sent to the selected Data Record File and the arm is placed on the previously selected record on the turntable. The contents of the cell specified in V<sub>3</sub> are transferred to the Data Record File Mode Buffer, and when the Normal Mode is interruptable, from the buffer to the HSM location specified by the U Register. Transfer is accomplished one character at a time with the contents of the U Register being incremented by one after each character transferred. When the end of a block is reached, determined by V<sub>2</sub>, L is decreased

by one. When L is decreased to zero, the operation terminates. This record does not have to be returned to the cage to perform other read or writes on the same surface.

#### **Final Register Contents**

$(U)_f = \text{HSM address of location one to the right of the last character placed in memory}$

$(V)_f = (B)_i$

#### **Timing**

Characters are written at the rate of 2.5 KC. The average time to get to and read a selected cell is 2.6 seconds. The time to return a record to the cage is 1.5 seconds.

## % Record File Mode Write (RMW)

### General Description

This instruction writes from a selected HSM location to designated cells in one of the four Data Record Files connected to the Data Record File Mode Control Unit. From one to ten blocks of information may be transferred to the Record File with one instruction. A cell can contain a block of information of from one to 900 characters. In writing, a block is terminated by an End of Block (EB) Symbol, or a cell count of 900 characters.

### Format

Operation — %

N — Selects the Data Record File Unit and the number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&
Third File	J	K	L	M	N	O	P	Q	R	— minus
Fourth File	/	S	T	U	V	W	X	Y	Z	”

A Address — HSM address of first character to be written to the Record File

B Address — B<sub>0</sub> 0 (zero)

B<sub>1</sub> determines if record stays on turntable after operation.

B<sub>1</sub> = odd—record returned to cage.

B<sub>1</sub> = even—record stays on turntable and arm is placed at beginning of previously selected band.

B<sub>2</sub> specifies whether EB sensed or not.

B<sub>2</sub> = 1 — block is terminated on counting of 900 characters.

B<sub>2</sub> = 0 — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer to this cell. If 900 count reached before an EB sensed, stop transfer into this cell.

B<sub>3</sub> addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

### Direction of Operation

Left to right in HSM.

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Record File Mode is free, the contents of the NOR, N, A, and B Registers are transferred to the FOR, L, U, and V Registers respectively, and this instruction is executed in the Record File Mode. A start signal is sent to the selected Data Record File and the arm is placed on the previously selected disc on the turntable. As soon as the normal mode is interruptable, the contents of the HSM location specified by the U Register are transferred to the Record File Mode Buffer and from the buffer to the specified cell. The contents of the U Register are increased by one and the contents of the HSM location now addressed by the U Register are transferred in a like manner. When the end of a block is reached,

determined by  $V_2$ ,  $L$  is decreased by one. When  $L$  is decreased to zero, the operation terminates. The record does not have to be returned to the cage to perform other read or writes to the same surface.

#### **Final Register Contents**

$(U)_f$  = Address of location one to the right of the last character written on the record.

$(V)_f = (B)_i$

#### **Timing**

Characters are written at the rate of 2.5 KC. The average time to get to and write to a selected cell is 2.6 seconds. The time to return a record to the cage is 1.5 seconds.

## D Track Select (TS)

### General Description

This instruction positions the read-write heads over 1 of 128 tracks. Once initiated the track selection is performed independently of computer operation.

### Format

Operation - D

N           - R (First Data Disc File)  
              - Z (Second Data Disc File)

A Address - 0000 (zeroes)

B Address -  $B_0 = 0$  (zero), will not override a DDF Simultaneous Instruction.  
              -  $B_0 = \&$ , will override any DDF Simultaneous Instruction.

### Outline of Operation

The contents of the N Register specify the proper Data Disc File.  $B_1, B_2, B_3$  designate the track address which can range from 000 to 127. All read-write heads within a Data Disc File are positioned concurrently so that 108 zones per module are accessible by the execution of one Track Select instruction.

If this instruction contains a bit in the  $B_0 2^4$  position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

### Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

### Timing

To initiate selection, 42  $\mu s$ .

To perform Track Selection:

Minimum - 40 milliseconds

Average - 75 milliseconds

Maximum - 100 milliseconds

## F Sector Read Disc Normal (SRN)

### General Description

This instruction reads from a selected sector of the Data Disc File to a designated HSM location. From one to ten sectors of information may be transferred from the Data Disc File with one instruction. 160 characters are transferred for each sector designated.

### Format

Operation - F

N - Specifies additional number of sectors to be read as follows:

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address - Address of HSM location to receive the first character read from the Data Disc File. This address must be an even number (left-hand end of a diad).

B Address - B<sub>0</sub> - designates first sector to be read:

First Sector to be read	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub> - specify the zone from which data is to be read:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

### Direction of Operation

Left to right in HSM

### Standard Location

STA (0212-0215)

### Outline of Operation

A start signal is sent to the Data Disc File and the contents of the sector specified by the B address are transferred to the Data Disc File Buffer and from the buffer to the HSM location, designated by the A Register. Transfer is effected two characters at a time, with the contents of the A Register being incremented by two after each pair of characters is transferred. When the additional number of sectors have been read, according to the N character, the operation terminates.

If this instruction contains a bit in the B<sub>0</sub> 2<sup>4</sup> position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

**Final Register Contents**

(A)<sub>f</sub> = Address of HSM location one to the right of the last character put in memory.

(B)<sub>f</sub> = (B)<sub>i</sub>

**Timing**

Characters are read at the rate of 32KC.

Five milliseconds are required to read one sector.

The average time to get to the designated sector is 25 milliseconds (file latency).

## G Sector Read Disc Simultaneous (SRS)

### General Description

This instruction reads from a selected sector of the Data Disc File to a designated HSM location. From one to ten sectors of information may be transferred from the Data Disc File with one instruction. 160 characters are transferred for each sector designated. However, this instruction may be terminated by any other Data Disc File instruction to the same file when the terminating instruction has the proper B<sub>0</sub> override character.

### Format

Operation - G

N - Specifies additional number of sectors to be read as follows:

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address - Address of HSM location to receive the first character read from the Data Disc File. This address must be an even number (left-hand end of a diad).

B Address - B<sub>0</sub> designates first sector to be read:

First Sector To Be Read	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub> - specify zone from which data is to be read:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

### Direction of Operation

Left to right in HSM.

### Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B registers are transferred to the SOR, M, S, T registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Data Disc File. The contents of the sector, as specified by the T Register are transferred to the Data Disc File Buffer, and when the Normal Mode is interruptable, from the buffer to the HSM location designated by the S Register. Transfer is accomplished two characters at a time, with the contents of the S Register being increased by two after each pair of characters is transferred. When the additional number of sectors have been read, according to the N character, the operation terminates.

The operation may also be terminated by another Data Disc File instruction to the same file when the B<sub>0</sub> character of the overriding instruction ranges from "&" to "I" as specified above.

If this instruction contains a bit in the B<sub>0</sub> 2<sup>4</sup> position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

**Final Register Contents**

(S)<sub>f</sub> - Address of HSM location one to the right of the last character transferred into memory.

(T)<sub>f</sub> - (B)<sub>i</sub>

**Timing**

Characters are read at the rate of 32KC.

Five milliseconds are required to read one sector into HSM.

The average time to get to the sector designated is 25 milliseconds (file latency).

## H Sector Write Disc Normal (SWN)

### General Description

This instruction writes from a selected HSM location to designated sectors of the Data Disc File. From one to ten sectors of information may be transferred to the Data Disc File with one instruction. 160 characters are transferred for each sector written.

### Format

Operation - H

N - Specified additional number of sectors to be written.

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address - HSM address of the first character to be written. This address must be an even number (left-hand end of a diad).

B Address -  $B_0$  - designates the first sector to be written:

First Sector to be Written	0	1	2	3	4	5	6	7	8	9
Will not override any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will override any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

$B_1, B_2, B_3$  - specify zone to which data is to be written:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

### Direction of Operation

Left to right in HSM

### Standard Location

STA (0212-0215)

### Outline of Operation

The contents of the HSM diad specified by the A Address are transferred to the Data Disc File Buffer and from the buffer to the specified sector. The contents of the A Register are incremented by two, and the contents of the next diad are then transferred. When the additional number of sectors have been written, according to the N character the operation terminates.

If this instruction contains a bit in the  $B_0 2^4$  position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

### Final Register Contents

$(A)_f$  = Address of HSM location one to the right of the last character written.

$(B)_f = (B)_i$

**Timing**

Characters are written at the rate of 32KC.

Five milliseconds are required to write one sector.

The average time to get to the sector designated is 25 milliseconds (file latency).

# I Sector Write Disc Simultaneous (SWS)

## General Description

This instruction writes from a selected HSM location to designated sectors of the Data Disc File. From one to ten sectors of information may be transferred to the Data Disc File with one instruction. 160 characters are transferred for each sector written; however, this instruction may be terminated by any other Data Disc File instruction to the same File when the terminating instruction has the proper  $B_0$  override character.

## Format

Operation - I

N - Specified additional number of sectors to be written.

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address - HSM Address of the first character to be written. This address must be an even number (left-hand end of a diad).

B Address -  $B_0$  - designates the first sector to be written

First Sector To Be Written	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

$B_1, B_2, B_3$  - specifies zone to which data is to be written:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

## Direction of Operation:

Left to right in HSM.

## Outline of Operation:

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B registers are transferred to the SOR, M, S and T registers, respectively; and this instruction is executed in the Simultaneous Mode. As soon as the Normal Mode is interruptible, the contents of the HSM diad specified by the S Register are transferred to the Data Disc File Buffer and from the buffer to the specified sector. The contents of the S Register are increased by two, and the contents of the diad specified transferred in a like manner. When the additional number of sectors have been written, according to the N character, the operation terminates.

The operation may also be terminated by another Data Disc File instruction to the same file when the  $B_0$  character of the overriding instruction ranges from "&" to "I" as specified above.

If this instruction contains a bit in the  $B_0 2^4$  position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

**Final Register Contents**

(S)<sub>f</sub> - Address of HSM location one to the right of the last character transferred from memory.

(T)<sub>f</sub> - B<sub>1</sub>

**Timing**

Characters are read at the rate of 32KC.

Five milliseconds are required to write one sector.

The average time to get to the sector is 25 milliseconds (file latency).



# **APPENDICES**

## APPENDIX I. RCA 301 CODES

Character Description	Printed Symbol	MACHINE CODE								TAPE CODE*								CARD CODE													
		P	ZONE			NUMERIC				P	ZONE			NUMERIC				PUNCHED ROWS													
		2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	Y	X	0	1	2	3	4	5	6	7	8	9
Zero	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1			1										
One	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0						1										
Two	2	0	0	0	0	0	1	0	1	1	1	1	1	0	1							1									
Three	3	1	0	0	0	0	1	1	0	1	1	1	1	0	0								1								
Four	4	0	0	0	0	1	0	0	1	1	1	1	0	1	1									1							
Five	5	1	0	0	0	1	0	1	0	1	1	1	0	1	0										1						
Six	6	1	0	0	0	1	1	0	0	1	1	1	0	0	1											1					
Seven	7	0	0	0	0	1	1	1	1	1	1	1	0	0	0												1				
Eight	8	0	0	0	1	0	0	0	1	1	1	0	1	1	1													1			
Nine	9	1	0	0	1	0	0	1	0	1	1	0	1	1	0														1		
Space		1	0	0	1	0	1	0	0	1	1	0	1	0	1																
Number	#	0	0	0	1	0	1	1	1	1	1	0	1	0	0								1						1		
At the rate of	@	1	0	0	1	1	0	0	0	1	1	0	0	1	1									1					1		
Open Parenthesis	(	0	0	0	1	1	0	1	1	1	1	0	0	1	0										1				1		
Close Parenthesis	)	0	0	0	1	1	1	0	1	1	1	0	0	0	1											1			1		
Ampersand	&	1	0	0	1	1	1	1	0	1	1	0	0	0	0				Not used												
A	A	1	0	1	0	0	0	1	0	1	0	1	1	1	0				1		1										
B	B	1	0	1	0	0	1	0	0	1	0	1	1	0	1				1			1									
C	C	0	0	1	0	0	1	1	1	1	0	1	1	0	0				1				1								
D	D	1	0	1	0	1	0	0	0	1	0	1	0	1	1				1					1							
E	E	0	0	1	0	1	0	1	1	1	0	1	0	1	0				1						1						
F	F	0	0	1	0	1	1	0	1	1	0	1	0	0	1				1							1					
G	G	1	0	1	0	1	1	1	0	1	0	1	0	0	0				1								1				
H	H	1	0	1	1	0	0	0	0	1	0	0	1	1	1				1									1			
I	I	0	0	1	1	0	0	1	1	1	0	0	1	1	0				1										1		
Plus	+	0	0	1	1	0	1	0	1	1	0	0	1	0	1				1										1		
Period	.	1	0	1	1	0	1	1	0	1	0	0	1	0	0				1				1						1		
Semicolon	;	0	0	1	1	1	0	0	1	1	0	0	0	1	1				1					1					1		
Colon	:	1	0	1	1	1	0	1	0	1	0	0	0	1	0				1						1				1		
Apostrophe	'	1	0	1	1	1	1	0	0	1	0	0	0	0	1				1							1			1		
Plus zero	+0	0	0	1	1	1	1	1	1	1	0	0	0	0	0				1	1											

\*Hi-Data Tape Group and Paper Tape

**APPENDIX I. RCA 301 CODES (Continued)**

Character Description	Printed Symbol	MACHINE CODE								TAPE CODE*								CARD CODE									
		P		ZONE			NUMERIC			P		ZONE			NUMERIC			PUNCHED ROWS									
		2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	Y	X	0	1	2	3	4	5	6	7	8	9
Minus	-	0	1	0	0	0	0	0	1	0	1	1	1	1	1												
J	J	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1											
K	K	1	1	0	0	0	1	0	0	0	1	1	1	0	1		1										
L	L	0	1	0	0	0	1	1	1	0	1	1	1	0	1			1									
M	M	1	1	0	0	1	0	0	0	0	1	1	0	1	1							1					
N	N	0	1	0	0	1	0	1	1	0	1	1	0	1	1							1					
O	O	0	1	0	0	1	1	0	1	0	1	1	0	0	1								1				
P	P	1	1	0	0	1	1	1	0	0	1	1	0	0	1									1			
Q	Q	1	1	0	1	0	0	0	0	0	1	0	1	1	1										1		
R	R	0	1	0	1	0	0	1	1	0	1	0	1	1	1										1		
End Information (EI)		0	1	0	1	0	1	0	1	0	1	0	1	0	1		1								1		
Dollars	\$	1	1	0	1	0	1	1	0	0	1	0	1	0	1			1							1		
Asterisk	*	0	1	0	1	1	0	0	1	0	1	0	0	1	1				1						1		
End Data (ED)		1	1	0	1	1	0	1	0	0	1	0	0	1	1							1			1		
End File (EF)		1	1	0	1	1	1	0	0	0	1	0	0	0	1								1		1		
Quotation Mark	”	0	1	0	1	1	1	1	1	0	1	0	0	0	Not used												
Virgule	/	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1											
S	S	0	1	1	0	0	1	0	1	0	0	1	1	0	1		1										
T	T	1	1	1	0	0	1	1	0	0	0	1	1	0	1			1									
U	U	0	1	1	0	1	0	0	1	0	0	1	0	1	1							1					
V	V	1	1	1	0	1	0	1	0	0	0	1	0	1	1							1					
W	W	1	1	1	0	1	1	0	0	0	0	1	0	0	1								1				
X	X	0	1	1	0	1	1	1	1	0	0	1	0	0	1										1		
Y	Y	0	1	1	1	0	0	0	1	0	0	0	1	1	1										1		
Z	Z	1	1	1	1	0	0	1	0	0	0	0	1	1	1										1		
End Block (EB)		1	1	1	1	0	1	0	0	0	0	0	1	0	1		1								1		
Comma	,	0	1	1	1	0	1	1	1	0	0	0	1	0	1			1							1		
Percent	%	1	1	1	1	1	0	0	0	0	0	0	0	1	1				1						1		
Item Separator (ISS)		0	1	1	1	1	0	1	1	0	0	0	0	1	1								1		1		
Equals	=	0	1	1	1	1	1	0	1	0	0	0	0	0	1									1	1		
Delete (paper tape only)		1	1	1	1	1	1	1							Indicates Gap												
									1	1	1	1	1	1	Not used												

\*Hi-Data Tape Group and Paper Tape

*Handwritten notes:*  
 60 ✓  
 70 ✓  
 80 ✓  
 90 ✓

## APPENDIX II. LIST OF INSTRUCTIONS

### Input-Output Instructions

<i>Op. Code</i>	<i>Abbreviation</i>	<i>Instruction Name</i>
0	CRN	Card Read Normal
1	CRS	Card Read Simultaneous
2	CPN	Card Punch Normal (Model 334 Punch)
2	CPN	Card Punch Normal (Model 336 Punch)
3	CPS	Card Punch Simultaneous (Model 334 Punch)
3	CPS	Card Punch Simultaneous (Model 336 Punch)
4	RFN	Tape Read Forward Normal
5	RFS	Tape Read Forward Simultaneous
6	RRN	Tape Read Reverse Normal
7	RRS	Tape Read Reverse Simultaneous
8	TWN	Tape Write Normal
9	TWS	Tape Write Simultaneous
B	PAN	Print and Paper Advance Normal
C	PAS	Print and Paper Advance Simultaneous
D	BSN	Band Select Normal
D	TS	Track Select
E	BSM	Band Select Record File Mode
F	BRN	Block Read Record Normal
F	SRN	Sector Read Disc Normal
G	BRS	Block Read Record Simultaneous
G	SRS	Sector Read Disc Simultaneous
H	BWN	Block Write Record Normal
H	SWN	Sector Write Disc Normal
I	BWS	Block Write Record Simultaneous
I	SWS	Sector Write Disc Simultaneous
*	RMR	Record File Mode Read
%	RMW	Record File Mode Write
;	RWD	Rewind to BTC

## APPENDIX II. LIST OF INSTRUCTIONS (Continued)

### Data Handling Instructions

<i>Op. Code</i>	<i>Abbreviation</i>	<i>Instruction Name</i>
A	TRA	Translate by Table
J	SF	Transfer Symbol to Fill
K	LSL	Locate Symbol Left
L	LSR	Locate Symbol Right
M	DL	Transfer Data Left
N	DR	Transfer Data Right
#	DSL	Transfer Data by Symbol Left
P	DSR	Transfer Data by Symbol Right

### Arithmetic Instructions

+	ADD	Add
Q	OR	Logical "OR"
- (minus)	SUB	Subtract
T	AND	Logical "AND"
U	EXO	Exclusive "OR"

### Decision and Control Instructions

R	RPT	Repeat
V	REG	Store Register
W	CTC	Conditional Transfer of Control
X	TA	Tally
Y	COM	Compare Left
S	IOS	Input-Output Sense
. (period)	HLT	Halt

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
A	Translate by Table	Number (0-44) of characters to be translated	HSM location of left-most character to be translated	HSM location of first character of translate table (must end in 00)
B	Print & Paper Advance Normal	Number (0-14) of lines to advance paper if $B_3 = 1$ . Also selects Printer unit and mode	0000 (zero)	Address of data to be printed from HSM excluding $B_3$ : $B_0$ = MSD of address $B_1$ = even - print, odd-do not print $B_2 = 0$ $B_3 = 0$ , no paper advance $B_3 = 1$ , paper advanced indicated by N $B_3 = 2$ vertical tab (using tape loop) $B_3 = 3$ , page change (using tape loop)
C	Print & Paper Advance Simultaneous	Number (0-14) of lines to advance paper if $B_3 = 1$ . Also selects Printer unit and mode	0000 (zero)	Address of data to be printed from HSM excluding $B_3$ : $B_0$ = MSD of address $B_1$ = even - print, odd-do not print $B_2 = 0$ $B_3 = 0$ , no paper advance $B_3 = 1$ , paper advanced indicated by N $B_3 = 2$ , vertical tab (using tape loop) $B_3 = 3$ , page change (using tape loop)
D	Band Select Normal	$2^0 = 0$ , selects first file; record returned to cage before selection. $2^0 = \&$ , selects second file; record returned to cage before selection. $2^0 = 1$ , selects first file; band selected is on turntable. $2^0 = A$ , selects second file; band selected is on turntable.	0000 (zero)	$B_0 = (\text{zero})$ $B_1, B_2, B_3$ designate band (000-511)
D	Track Select	Specifies Data Disc File to select R (First Data Disc File) Z (Second Data Disc File)	0000 (zero)	$B_0 = (\text{zero})$ $B_1, B_2, B_3$ selects track (000-127)

## OF INSTRUCTIONS

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
			Yes	Operation left to right. Translation in place	$(A)_f = \text{HSM address of location one to the right of the last character translated}$	$(B)_f = (B)_i$
				120 or 160 characters printed if $B_1$ is even. Print is done first when applicable. Paper Advance is completely independent of computing. Operation left to right	$(A)_f = \text{HSM address of location one to the right of last character printed.}$ $(A)_f = (A)_i$ when printing is not indicated	$(B)_f = (B)_i$ with $B_3$ set to zero
				120 or 160 characters printed if $B_1$ is even. Print is done first if applicable. Paper Advance is completely independent of computing. Operation left to right	$(S)_f = \text{HSM address of location one to the right of last character printed.}$ $(S)_f = (A)_i$ when printing is not indicated	$(T)_f = (B)_i$ with $B_3$ set to zero
				The record will be selected independent of computer operation	$(A)_f = (A)_i$	$(B)_f = (B)_i$
				Track will be selected independently of computer operation	$(A)_f = (A)_i$	$(B)_f = (B)_i$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
E	Band Select Record File Mode	$2^0 = 0$ , returns record to cage before selection. $2^0 = 1$ , band selected is on turntable. Bits $2^4 - 2^5 =$ Record File from which band is to be selected.	0000 (zero)	$B_0 = 0$ (zero) $B_1, B_2, B_3$ designates band (000-511)
F	Block Read Record Normal	$2^3, 2^2, 2^1, 2^0$ selects number of blocks to be read. $2^4 = 0$ , selects first file. $2^4 = 1$ , selects second file.	HSM address where first character is to be placed.	$B_0 = 0$ (zero) $B_1 = \text{odd}$ - record returned to cage after operation $B_1 = \text{even}$ - record stays on turntable and arm is placed at beginning of selected band after operation. $B_2 = 1$ - block terminated on counting 900 characters. $B_2 = 0$ - count or EB recognition. $B_3 =$ addresses cells 1-10.
F	Sector Read Disc Normal	Specifies additional number of sectors to be read and file selected.	Address of HSM location to receive first character read	$B_0$ = designates first sector to be read. $B_1, B_2, B_3$ specifies zone to be read from. $2^4$ of $B_0 = 0$ , prevents override of SRS instruction $2^4$ of $B_0 = 1$ , permits override of any Data Disc File Simultaneous instruction. $B_1, B_2, B_3$ , specifies zone to be read from.
G	Block Read Record Simultaneous	$2^3, 2^2, 2^1, 2^0$ selects number of blocks to be read. $2^4 = 0$ , selects first file. $2^4 = 1$ , selects second file.	HSM address where first character is to be placed	$B_0 = 0$ (zero) $B_1 = \text{odd}$ - record returned to cage after operation. $B_1 = \text{even}$ - record stays on turntable and arm is placed at beginning of selected band after operation. $B_2 = 1$ - block terminated on counting 900 characters. $B_2 = 0$ - count or EB recognition. $B_3 =$ addresses cells 1-10.
G	Sector Read Disc Simultaneous	Specifies Additional Number of sectors to be read and file selected	Address of HSM location to receive first character read	$2^3, 2^2, 2^1, 2^0$ bits of $B_0$ designates first sector to be read. $2^4$ of $B_0 = 0$ , prevents override of SRS instruction $2^4$ of $B_0 = 1$ , permits override of any Data Disc File Simultaneous instruction. $B_1, B_2, B_3$ , specifies zone to be read from.

**OF INSTRUCTIONS (Continued)**

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
				Record will be selected independent of computer operation. This instruction used with files under control of record file mode only	$(A)_f = (A)_i$	$(B)_f = (B)_i$
Yes				Operation left to right	$(A)_f =$ HSM address one to the right of last character read	$(B)_f = (B)_i$
Yes				Operation left to right	$(A)_f =$ HSM address one to the right of last character read.	$(B)_f = (B)_i$
				Operation left to right	$(S)_f =$ HSM address one to the right of last character read	$(T)_f = (B)_i$
				Operation left to right	$(S)_f =$ HSM address one to the right of last character	$(T)_f = (B)_i$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
H	Block Write Record Normal	$2^3, 2^2, 2^1, 2^0$ selects number of blocks to be written. $2^4 = 0$ , selects first file. $2^4 = 1$ , selects second file.	HSM address where first character is to be written	$B_0 = 0$ (zero) $B_1 =$ odd-record returned after operation $B_1 =$ even-record stays on turntable and arm is placed at beginning of selected band after operation $B_2 = 1$ - block terminates on counting 900 characters $B_2 = 0$ - count or EB recognition $B_3 =$ addresses cells 1-10
H	Sector Write Disc Normal	Specifies additional number of sectors to be written and file selected	HSM address of first character to be written	$B_0$ designates first sector to be written to $2^4$ of $B_0 = 0$ , prevents override of Data Disc Simultaneous instruction $2^4$ of $B_0 = 1$ , permits override of Data Disc Simultaneous instruction $B_1, B_2, B_3$ specifies zone to be written to
I	Block Write Record Simultaneous	$2^3, 2^2, 2^1, 2^0$ selects number of blocks to be written $2^4 = 0$ , selects first file $2^4 = 1$ , selects second file	HSM address where first character is to be written	$B_0 = 0$ (zero) $B_1 =$ odd-record returned after operation $B_1 =$ even-record stays on turntable and arm is placed at beginning of selected band after operation $B_2 = 1$ - block terminates on counting 900 characters $B_2 = 0$ - count or EB recognition $B_3 =$ addresses cells 1-10
I	Sector Write Disc Simultaneous	Specifies additional number of sectors to be written and file selected	HSM address of first character to be written	$2^3, 2^2, 2^1, 2^0$ bit of $B_0$ designate 1st sector to be written $2^4$ of $B_0 \neq 0$ , prevents override of Data Disc Simultaneous instruction $2^4$ of $B_0 = 1$ , permits override of Data Disc Simultaneous instruction $B_1, B_2, B_3$ specifies zone to be written to
J	Transfer Symbol to Fill	Selected Symbol	Leftmost HSM address to be filled	Rightmost HSM address to be filled
K	Locate Symbol Left	Selected Symbol	Leftmost HSM address to be searched	Rightmost HSM address to be searched

**OF INSTRUCTIONS (Continued)**

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
				Operation left to right	$(A)_f = \text{HSM address one to the right of last character written}$	$(B)_f = (B)_i$
Yes				Operation left to right	$(A)_f = \text{HSM address one to the right of last character written}$	$(B)_f = (B)_i$
				Operation left to right	$(S)_f = \text{HSM address one to the right of last character written}$	$(T)_f = (B)_i$
				Operation left to right	$(S)_f = \text{HSM address one to the right of last character written}$	$(T)_f = (B)_i$
				Operation left to right	$(A)_f = (B)_i + \text{one character location}$	$(B)_f = (B)_i$
Yes		Yes		Operation left to right. PRI's set as follows: PRN if first character not equal to N. PRZ if all characters are equal to N. PRP if non-symbol is located after a character equal to N is found	If a character is found not equal to N $(A)_f = \text{HSM address one to left of that character.}$ If all characters searched are equal to N $(A)_f = (B)_i$	$(B)_f = (B)_i$

0001

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
L	Locate Symbol Right	Selected Symbol	Rightmost HSM address to be searched	Leftmost HSM address to be searched
M	Transfer Data Left	Number (0-44) of characters to be transferred	HSM location of leftmost character to be transferred	Destination HSM address of first character
N	Transfer Data Right	Number (0-44) of characters to be transferred	HSM location of rightmost character to be transferred	Destination HSM address of first character
P	Transfer Data by Symbol Right	Selected symbol on which to stop transferring	HSM location of rightmost character to be transferred	Destination HSM address of first character
Q	Logical "OR"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand
R	Repeat	Number (0-14) of times to repeat next instruction in sequence	A = 0000-do not staticize when repeating instruction A = 0001-staticize when repeating instruction	B = 0000-do not staticize when repeating instruction B = 0001-staticize when repeating instruction
S	Input-Output Sense	Indicates the input-output device to be sensed	A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> = 000 (zero) A <sub>0</sub> = specifies tests to be performed	HSM address of the next instruction to be executed if the condition (s) being tested are present
T	Logical "AND"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand
U	Exclusive "OR"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand

**OF INSTRUCTIONS (Continued)**

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
Yes		Yes		Operation right to left PRI's set as follows: PRN if first character not equal to N PRZ if all characters are equal to N PRP if non-symbol is located after a character equal to N is found	If a character is found not equal to N $(A)_f = \text{HSM address one to right of that character.}$ If all characters searched are equal to N $(A)_f = (B)_i$	$(B)_f = (B)_i$
			Yes	Operation left to right	$(A)_f = \text{HSM address one to the right of last character transferred}$	$(B)_f = \text{HSM address one to the right of last destination address}$
			Yes	Operation right to left	$(A)_f = \text{HSM address one to the left of last character transferred}$	$(B)_f = \text{HSM address one to the left of last destination address}$
Yes			Yes	Operation right to left	$(A)_f = \text{HSM address one to the left of specified symbol in the original area}$	$(B)_f = \text{HSM address one to the left of symbol in destination area}$
			Yes	Operation right to left	$(A)_f = \text{HSM address one to the left of MSD of result}$	$(B)_f = \text{HSM address one to the left of MSD of second operand}$
					$(A)_f = (A)_i$	$(B)_f = (B)_i$
	Yes				$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes	Yes	Operation right to left. PRN is set if the result is all zeros, otherwise PRP is set	$(A)_f = \text{HSM address one to the left of the MSD in result}$	$(B)_f = \text{HSM address one to the left of MSD in second operand}$
			Yes	Operation right to left	$(A)_f = \text{HSM address one to the left of MSD in result}$	$(B)_f = \text{HSM address one to the left of MSD in second operand}$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
V	Store Register	Specifies Register to be stored: N = 0—None N = 1—P Register N = 2—A Register N = 4—B Register N = 8—S Register N = &—U Register	HSM address of rightmost diad to receive contents of register, excluding A Register, specified by N. If A is stored, contents of A Register of previous instruction are stored in STA. The contents of A of this instruction is ignored.	HSM address of next instruction if P Register is stored. Otherwise, B address is zero.
W	Conditional Transfer of Control	Specifies element to be sensed: N = 0, None N = 1, PRP's N = 2, Overflow Indicators N = 4, Simultaneous Mode Indicator N = 8, EF/ED Normal Indicator N = &, Interrupt Indicator N = -, EF/ED Simultaneous Indicator	HSM address of next instruction if one of the following conditions is true: N = 1 and PRP is set N = 2 and first overflow indicator is set N = 4 and a read is in Simultaneous Mode N = 8 and EF/ED Normal Indicator is set N = & and Interrupt Indicator is set (INT button is on) N = - and EF/ED Simultaneous Indicator is set	HSM address of next instruction if one of the following conditions is true: N = 1 and PRN is set N = 2 and neither overflow indicator is set N = 4 and a "write" is in the Simultaneous Mode N = 8 and the EF/ED Normal Indicator is not set N = & and the Interrupt Indicator is not set N = - (minus) and the EF/ED Simultaneous Indicator is not set
X	Tally	0 (zero)	HSM address of diad containing the quantity to be tested	HSM address of next instruction if quantity has not been exhausted
Y	Compare Left	Number (0-44) of characters to be compared	HSM address of leftmost character of first operand	HSM address leftmost character of second operand

## OF INSTRUCTIONS (Continued)

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
Yes (Store A only)					$(A)_f = (A)_i - 2$ , if B, P, S, or $\bar{U}$ are stored. $(A)_f = (A)_f$ of previous instruction if A is stored or if N equals zero	$(B)_f = (B)_i$ , if P, S, or U are stored. $(B)_f = (B)_f$ of previous instruction if A or B Register are stored or if N equals zero
	Yes			The next instruction in sequence is performed if: 1. N = 0 2. N = 1 and PRZ is set. 3. N = 2 and Second Overflow indicator is set 4. N = 4 and Simultaneous Mode is unoccupied.	$(A)_f = (A)_i$	$(B)_f = (B)_i$
	Yes			Maximum value of tally quantity is 99	$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes		Operation left to right. PRZ set when contents of N decreases to zero. PRP set when value of character addressed by (A) > than that of (B). PRN set when value of character addressed by (A) < than that of (B).	$(A)_f = \text{HSM address one to the right of last character compared in first operand}$	$(B)_f = \text{HSM address one to the right of last character compared in second operand}$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
0	Card Read Normal	Selects proper card reader and reading rate	HSM address of first character read from punched cards	0000 (zero)
1	Card Read Simultaneous	Selects proper card reader and reading rate	HSM address of first character read from punched cards	0000 (zero)
2	Card Punch Normal (Model 334 Card Punch)	0 (zero)	HSM address of first character to be punched	HSM address of last character to be punched
2	Card Punch Normal (Model 336 Card Punch)	Determines rate at which cards are to be punched	HSM address of first character to be punched	0000 (zero)
3	Card Punch Simultaneous (Model 334 Card Punch)	0 (zero)	HSM address of first character to be punched	HSM address of last character to be punched
3	Card Punch Simultaneous (Model 336 Card Punch)	Determines rate at which cards are to be punched	HSM address of first character to be punched	0000 (zero)
4	Tape Read Forward Normal	Specifies tape station or Paper Tape Reader.	HSM address of first character to be read	HSM address of last character to be read
5	Tape Read Forward Simultaneous	Specifies tape station or Paper Tape Reader	HSM address of first character to be read	HSM address of last character to be read
6	Tape Read Reverse Normal	Specifies tape station or Paper Tape Reader	HSM address of first character to be read	HSM address of last character to be read

**OF INSTRUCTIONS (Continued)**

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
				Operation left to right	$(A)_f = \text{HSM address one to the right of last character read into HSM}$	$(B)_f = (A)_i$ BCT off $(B)_f = A_i + 80$ BCT on
				Operation left to right	$(S)_f = \text{HSM address one to right of last character read from cards}$	$(T)_f = A_i$ BCT off $(T)_f = A_i + 80$ BCT on
				Operation left to right	$(A)_f = \text{HSM address one to right of last character punched}$	$(B)_f = (B)_i$
				Operation left to right	$(A)_f = (A)_i + 80$	$(B)_f = (B)_i$
				Operation left to right	$(S)_f = \text{HSM address one to the right of last character punched}$	$(T)_f = (B)_i$
				Operation left to right	$(S)_f = (A)_i + 80$	$(T)_f = (B)_i$
Yes		Yes	Yes	Operation left to right. PRP set when $(A) = (B)$ before gap occurs on tape. PRN set when $(A) \neq (B)$ and gap occurs. PRZ set when $(A) = (B)$ and gap occurs on tape. EF/ED Normal Indicator set if ED or EF alone is read from mag. tape.	$(A)_f = \text{HSM address one to the right of last character read}$	$(B)_f = (B)_i$
				Operation left to right. ED/EF Simultaneous Indicator set if an ED or EF alone is read from mag. tape.	$(S)_f \neq \text{HSM address one to the right of last character read}$	$(T)_f = (B)_i$
Yes		Yes	Yes	Operation right to left. PRP set when $(A) = (B)$ before gap occurs on tape. PRN set when $(A) \neq (B)$ and a gap occurs. PRZ set when $(A) = (B)$ and a gap occurs. EF/ED Normal Indicator is set if an EF or ED is read from mag. tape.	$(A)_f = \text{HSM address one to the left of last character read}$	$(B)_f = (B)_i$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
7	Tape Read Reverse Simultaneous	Specifies tape station or Paper Tape Reader	HSM address of first character to be read	HSM address of last character to be read
8	Tape Write Normal	Specifies tape station, Paper Tape Punch, or Monitor Printer.	HSM address of first character to be written, punched or typed	HSM address of last character to be written, punched or typed
9	Tape Write Simultaneous	Specifies tape station, Paper Tape Punch, or Monitor Printer.	HSM Address of first character to be written, Punched, or typed	HSM address of last character to be written, punched or typed
*	Record File Mode Read	2 <sup>3</sup> , 2 <sup>2</sup> , 2 <sup>1</sup> , 2 <sup>0</sup> selects number of blocks to be read 2 <sup>5</sup> , 2 <sup>4</sup> selects File Unit	HSM address where first character is to be placed	B <sub>0</sub> = 0 (zero) B <sub>1</sub> = odd—record returned to cage after instruction B <sub>1</sub> = even—record remains on turntable and arm placed at beginning of selected band after instruction. B <sub>2</sub> = 1—block terminates on count of 900 characters B <sub>2</sub> = 0—count or EB recognition B <sub>3</sub> = addresses cells 1-10
%	Record File Mode Write	2 <sup>3</sup> , 2 <sup>2</sup> , 2 <sup>1</sup> , 2 <sup>0</sup> selects number of blocks to be written 2 <sup>5</sup> , 2 <sup>4</sup> selects File Unit	HSM address of first character to be written	B <sub>0</sub> = 0 (zero) B <sub>1</sub> = odd—record returned to cage after instruction. B <sub>1</sub> = even—record remains on turntable and arm placed at beginning of selected band after instruction. B <sub>2</sub> = 1—block terminates on count of 900 characters B <sub>2</sub> = 0—count or EB recognition B <sub>3</sub> = addresses cells 1-10
;	Rewind to BTC	Specifies tape station	0000 (zero)	0000 (zero)
#	Transfer Data by Symbol Left	Selected symbol on which to stop transferring	HSM address of leftmost character to be transferred	HSM address of destination of first character
+	Add	Number (0-44) of characters in each operand	HSM address of LSD of augend and sum	HSM address of LSD of addend

## OF INSTRUCTIONS (Continued)

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
				Operation right to left. ED/ EF Simultaneous Indicator set if an ED or EF is read from mag. tape.	$(S)_f = \text{HSM address one tothe left of last characterread}$	$(T)_f = (B)_i$
				Operation left to right. Tape motion forward	$(A)_f = \text{HSM address one tothe right of last characterwritten, punched, or typed}$	$(B)_f = (B)_i$
				Operation left to right. Tape motion forward.	$(S)_f = \text{HSM address one tothe right of last characterwritten, punched, or typed}$	$(T)_f = (B)_i$
				Operation left to right	$(U)_f = \text{HSM address one tothe right of last characterplaced}$	$(V)_f = (B)_i$
				Operation left to right	$(U)_f = \text{HSM address one tothe right of last char-acter written}$	$(V)_f = (B)_i$
				Direction of tape motion is reverse and independent of computing	$(A)_f = (A)_i$	$(B)_f = (B)_i$
Yes			Yes	Operation left to right	$(A)_f = \text{HSM address one tothe right of specified sym-bol in origin area}$	$(B)_f = \text{HSM address one to theright of symbol in destinationarea}$
		Yes	Yes	Operation right to left with the sign in the zone bit $2^5$ of LSD. PRI's set as follows: PRP if sum is + PRZ if sum is 0 PRN if sum is -	$(A)_f = \text{HSM address one toleft of MSD of sum}$	$(B)_f = \text{HSM address one to theleft of MSD of addend}$

### APPENDIX III. SUMMARY

Op. Code	Instruction	N	A Address	B Address
-	Subtract	Number (0-44) of characters in each operand	HSM address of LSD of minuend and difference	HSM address of LSD subtrahend
•	Halt	0 (zero), may be used to designate type of stop	0000 (zero), may be used for numeric constants (0-9)	0000 (zero), may be used for numeric constants (0-9)

**OF INSTRUCTIONS (Continued)**

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
		Yes	Yes	Operation right to left with the sign in the zone bit $2^5$ of LSD: PRI's set as follows: PRP if result is + PRZ if result is 0 PRN if result is -	$(A)_f = \text{HSM address one to left of MSD of difference}$	$(B)_f = \text{HSM address one to left of MSD of subtrahand}$
				Stops the computer after completion of any instruction in the Simultaneous Mode.	$(A)_f = (A)_i$	$(B)_f = (B)_i$

## APPENDIX IV. INSTRUCTION TIMING\*

Op. Code	Instruction	Timing in $\mu$ s	Expository Notes
A	Translate by Table	$21n + 35$	$n$ = no. of characters to be translated
B	Print and Paper Advance Normal	a. $60 \dagger$ b. $76 \dagger$ c. 150 lines per second	a. Print and paper advance of one line in Synchronous Mode b. Print and paper advance of one line in Asynchronous Mode c. Paper advance rate after first line
C	Print and Paper Advance Simultaneous	a. $60 \dagger$ b. $76 \dagger$ c. 150 lines per second	a. Print and paper advance of one line in Synchronous Mode b. Print and paper advance of one line in Asynchronous Mode c. Paper advance rate after first line
D	Band Select Normal	a. $21(B_1) + 14(B_2) + 42$ b. $2.25 \ddagger$	a. To initiate selection b. Average time to perform Band Selection
D	Track Select	a. 42 b. $40 \dagger$ c. $75 \dagger$ d. $100 \dagger$	a. To initiate selection b. Minimum selection time c. Average selection time d. Maximum selection time
E	Band Select Record File Mode	a. $21(B_1) + 14(B_2) + 42$ b. $2.25 \ddagger$	a. To initiate selection b. Average time to perform Band Selection

\* STA or STP where applicable, and staticizing time included in formulas.

$\dagger$  Time here in milliseconds.

$\ddagger$  Time here in seconds

$\S$  Does not include staticizing time, stop-start, or switching time.

**APPENDIX IV. INSTRUCTION TIMING\* (Continued)**

Op. Code	Instruction	Timing in $\mu$ s	Expository Notes
F	Block Read Record Normal	a. 2.6‡ b. 1.5‡ c. 2.5 KC	a. Average time to get to and read one cell b. Return record to cage c. Character transfer rate
F	Sector Read Disc Normal	a. 25+ b. 32 KC	a. Average File Latency b. Character transfer rate
G	Block Read Record Simultaneous	a. 2.6‡ b. 1.5‡ c. 2.5 KC	a. Average time to get to and read one cell b. Return record to cage c. Character transfer rate
G	Sector Read Disc Simultaneous	a. 25+ b. 32 KC	a. Average File Latency b. Character transfer rate
H	Block Write Record Normal	a. 2.6‡ b. 1.5‡ c. 2.5 KC	a. Average time to get to and write one cell b. Return record to cage c. Character transfer rate
H	Sector Write Disc Normal	a. 25 b. 32 KC	a. Average File Latency b. Character transfer rate
I	Block Write Record Simultaneous	a. 2.6‡ b. 1.5‡ c. 2.5 KC	a. Average time to get to and write one cell b. Return record to cage c. Character transfer rate
I	Sector Write Disc Simultaneous	a. 25+ b. 32 KC	a. Average File Latency b. Character transfer rate
J	Transfer Symbol to Fill	a. $7n + 35$	n = no. of locations filled

\*See Footnotes on page 138.

**APPENDIX IV. INSTRUCTION TIMING\* (Continued)**

<b>Op. Code</b>	<b>Instruction</b>	<b>Timing in <math>\mu</math>s</b>	<b>Expository Notes</b>
K	Locate Symbol Left	a. $14n + 70$ b. $14n + 56$	a. If a character is found not equal to contents of N b. If all characters searched are equal to contents of N  $n = \text{no. of selected symbols searched}$
L	Locate Symbol Right	a. $14n + 70$ b. $14n + 56$	a. If a character is found not equal to contents of N b. If all characters searched are equal to contents of N  $n = \text{no. of selected symbols searched}$
M	Transfer Data Left	$14n + 35$	$n = \text{no. of characters transferred}$
N	Transfer Data Right	$14n + 35$	$n = \text{no. of characters transferred}$
P	Transfer Data by Symbol Right	$14n + 49$	$n = \text{no. of characters transferred}$
Q	Logical "OR"	$21n + 35$	$n = \text{no. of characters in each operand}$
R	Repeat	49	
S	Input-Output Sense	a. 49 b. 35	a. If a transfer is executed b. If no transfer takes place
T	Logical "AND"	$21n + 35$	$n = \text{no. of character in each operand}$
U	Exclusive "OR"	$21n + 35$	$n = \text{no. of characters in each operand}$
V	Store Register	49	
W	Conditional Transfer of Control	a. 49 b. 35	a. If a transfer of control takes place b. If no transfer of control takes place

\*See Footnotes on page 138.

**APPENDIX IV. INSTRUCTION TIMING\*** (Continued)

Op. Code	Instruction	Timing in $\mu$ s	Expository Notes
X	Tally	a. 70 b. 49	a. When tally quantity is greater than zero upon starting b. When tally quantity is equal to zero upon starting
Y	Compare	$21n + 35$	n = no. of character compared
0	Card Read Normal	a. 600 cards/min§ b. 300 cards/min§	a. If N = 4 or D b. If N = M or U
1	Card Read Simultaneous	a. 600 cards/min§ b. 300 cards/min§	a. If N = 4 or D b. If N = M or U
2	Card Punch Normal	a. 100 cards/min§ b. 200 cards/min§	a. Model 334 Punch b. Model 336 Punch
3	Card Punch Simultaneous	a. 100 cards/min§ b. 200 cards/min§	a. Model 334 Punch b. Model 336 Punch
4	Tape Read Forward Normal§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7 KC	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station
5	Tape Read Forward Simultaneous§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7 KC	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station

\*See Footnotes on page 138.

**APPENDIX IV. INSTRUCTION TIMING\*** (Continued)

Op. Code	Instruction	Timing in $\mu$ s	Expository Notes
6	Tape Read Reverse Normal§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station
7	Tape Read Reverse Simultaneous§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7 KC	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station
8	Tape Write Normal§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7 KC	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station
9	Tape Write Simultaneous§	a. 10 KC b. Up to 1000 char/sec c. 33.3 KC d. 66.7 KC	a. Rate of Hi-Data Tapes b. Rate of reading Paper Tape c. Rate of model 581 station d. Rate of model 582 station
*	Record File Mode Read§	a. 2.5 KC b. 2.6‡ c. 1.5‡	a. Rate of reading characters b. Average time to get to and read a cell c. Time to return record to cage
%	Record File Mode Write§	a. 2.5 KC b. 2.6‡ c. 1.5‡	a. Rate of reading characters b. Average time to get to and read a cell c. Time to return record to cage

\*See Footnotes on page 138.

**APPENDIX IV. INSTRUCTION TIMING\*** (Continued)

Op. Code	Instruction	Timing in $\mu$ s	Expository Notes
;	Rewind to BTC	Less than 180‡	Time to rewind full tape
#	Transfer Data by Symbol Left	$14n + 49$	n = no. of characters to be transferred
+	Add	a. $28n + 49$  b. $21n + 14$	a. Time when an "end around condition" does not exist  b. Time that must be added to "a" when an "end around condition" exists  n = no. of characters in each operand
-	Subtract	a. $28n + 49$  b. $21n + 14$	a. Time when an "end around condition" does not exist  b. Time that must be added to "a" when an "end around condition" exists  n = no. of characters in each operand
•	Halt	35	

\*See Footnotes on page 138.

**APPENDIX V. STANDARD HIGH SPEED MEMORY LOCATIONS**

<b>HSM Locations</b>	<b>Use</b>
0000-0099	Sum Table
0100-0199	Difference Table
0202-0205	Card Punch - Temporary storage of address
0206-0209	Arithmetic - Temporary storage of address
0212-0215	STA
0216-0219	STP
0222-0225	Standard Location for Storing P in a Repeat Instruction
	<b>Model 303 Processor:</b>
9900-9977	Print Table
9978-9999	Reserved
	<b>Model 304 Processor:</b>
I900-I977	Print Table
I978-I999	Reserved
	<b>Model 305 Processor:</b>
Z900-Z977	Print Table
Z978-Z999	Reserved

**APPENDIX VI-A. SYMBOLS USED FOR N CHARACTER COUNTS  
EXCEPT IN REPEAT AND PAPER ADVANCE INSTRUCTIONS**

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	11	A	22	K	33	T
1	1	12	B	23	L	34	U
2	2	13	C	24	M	35	V
3	3	14	D	25	N	36	W
4	4	15	E	26	O	37	X
5	5	16	F	27	P	38	Y
6	6	17	G	28	Q	39	Z
7	7	18	H	29	R	40	EB
8	8	19	I	30	"	41	, (comma)
9	9	20	- (minus)	31	/	42	%
10	&	21	J	32	S	43	● (ISS)
						44	=

**APPENDIX VI-B. SYMBOLS USED FOR N CHARACTER COUNTS  
IN REPEAT AND PAPER ADVANCE INSTRUCTIONS**

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	4	4	8	8	12	@
1	1	5	5	9	9	13	(
2	2	6	6	10	(space)	14	)
3	3	7	7	11	#		

## APPENDIX VII. DEVICE IDENTIFICATION FOR INPUT-OUTPUT AND IOS INSTRUCTIONS

### IOS Instructions

Device	First Unit	Second Unit
Card Reader	(	:
Card Punch	)	
Paper Tape Reader	8	
Paper Tape Punch	9	
On Line Printer	7	G
Data Disc File	R	Z
Data Record File (under control of RFC Unit)	R	Z
Data Record File (under control of RFM Unit)	# \$ . ,	
Hi-Data Tape Group	123456	ABCDEF
Dual Tape Channel (Model 341,351)	123456	
Dual Tape Channel (Model 342,352)	123456 ABCDEF	
Tape Adapter, 33KC	J	N
66KC	L	P

### Input/Output Instructions

Device	First Unit	Second Unit
Card Reader	$2^4 \text{ bit} = 0$	$2^4 \text{ bit} = 1$
Card Punch (Model 334)	0 (zero)	
Card Punch (Model 336)*	1, 2, 4	
Paper Tape Reader	8	
Paper Tape Punch	9	
On Line Printer	$2^4 \text{ bit} = 0$	$2^4 \text{ bit} = 1$
Monitor Printer	7	
Data Disc File:		
Track Select	R	Z
Read-Write	$2^4 \text{ bit} = 0$	$2^4 \text{ bit} = 1$
Data Record File:		
Record File Control		
Band Select	R	Z
Read-Write	$2^4 \text{ bit} = 0$	$2^4 \text{ bit} = 1$
Record File Mode		
Band Select**	$2^4 2^5 = 00$	$2^4 2^5 = 01$
Read-Write	$2^4 2^5 = 00$	$2^4 2^5 = 01$
Hi-Data Tape Group	123456	ABCDEF
Dual Tape Channel (Model 341, or 351)	123456	
Dual Tape Channel (Model 342, or 352)	123456	ABCDEF
Tape Adapter		
33KC	J	N
66KC	L	P

\*Also Indicates Speed and Ending Routine

\*\*Third Unit -  $2^4 2^5 = 10$ ; Fourth Unit -  $2^4 2^5 = 11$

**APPENDIX VIII. PRINT TABLE\***

Character	Table Location			Character	Table Location		
	Memory Size				Memory Size		
	10,000	20,000	40,000		10,000	20,000	40,000
- Minus	9900	1900	Z900	A Letter	9940	I940	Z940
+ Plus	9901	1901	Z901	B "	9941	I941	Z941
Space	9902	1902	Z902	C "	9942	I942	Z942
0 Zero	9903	1903	Z903	D "	9943	I943	Z943
1 One	9904	1904	Z904	E "	9944	I944	Z944
2 Two	9905	1905	Z905	F "	9945	I945	Z945
3 Three	9906	1906	Z906	G "	9946	I946	Z946
4 Four	9907	1907	Z907	H "	9947	I947	Z947
5 Five	9910	1910	Z910	I "	9950	I950	Z950
6 Six	9911	1911	Z911	J "	9951	I951	Z951
7 Seven	9912	1912	Z912	K "	9952	I952	Z952
8 Eight	9913	1913	Z913	L "	9953	I953	Z953
9 Nine	9914	1914	Z914	M "	9954	I954	Z954
, Comma	9915	1915	Z915	N "	9955	I955	Z955
. Period	9916	1916	Z916	O "	9956	I956	Z956
@ At	9917	1917	Z917	P "	9957	I957	Z957
% Percent	9920	1920	Z920	Q "	9960	I960	Z960
: Colon	9921	1921	Z921	R "	9961	I961	Z961
# Number	9922	1922	Z922	S "	9962	I962	Z962
\$ Dollar Sign	9923	1923	Z923	T "	9963	I963	Z963
) Close Parenthesis	9924	1924	Z924	U "	9964	I964	Z964
" Quote	9925	1925	Z925	V "	9965	I965	Z965
<sub>10</sub> Sub 10	9926	1926	Z926	W "	9966	I966	Z966
( Open Parenthesis	9927	1927	Z927	X "	9967	I967	Z967
] Close Bracket	9930	1930	Z930	Y "	9970	I970	Z970
; Semicolon	9931	1931	Z931	Z "	9971	I971	Z971
> Greater Than	9932	1932	Z932	CR Credit Symbol	9972	I972	Z972
÷ Divide	9933	1933	Z933	' Apostrophe	9973	I973	Z973
↑ Arrow Up	9934	1934	Z934	* Asterisk	9974	I974	Z974
[ Open Bracket	9935	1935	Z935	& Ampersand	9975	I975	Z975
< Less Than	9936	1936	Z936	/ Virgule	9976	I976	Z976
= Equal Sign	9937	1937	Z937	⊠ Lozenge	9977	I977	Z977

\* Four of the 64 code configurations will not be available as standard 301 codes but can be generated by computer programming. Also, some of the 301 symbols do not appear in this list so that other symbols may be chosen to represent the 301 symbols. It is advisable to prevent energizing the hammers for spaces by placing the code (17)<sub>8</sub> in location 9902, 1902, or Z902. In fact, the code (17)<sub>8</sub> can be placed in any location in the table when it is desired to prevent printing of the associated character. For this reason, too, any (17)<sub>8</sub> codes appearing in the print area will never cause printing of any character.

## APPENDIX IX: GLOSSARY OF TERMS

- Access Time.* A time interval which is characteristic of a storage device, and is essentially a measure of the time required to communicate with that device. The time interval between (1) the instant at which information is called for from storage and the instant at which it is delivered or (2) the instant at which information is ready for storage and the instant at which it is stored.
- Address (noun).* An expression, which designates a particular location in a storage or memory device or other source or destination of information.
- Absolute Address (Direct Address).* The specific label assigned by the machine designer to a particular storage location. To code in absolute means to write a sequence of instructions in a computer code.
- Indirect Address.* The address of a memory location whose contents contain the address of another memory location to be accessed.
- Instruction Address. (Line Number, Location).* An expression used in coding to denote the address of a stored instruction. NOT a part of the instruction itself.
- Symbolic Address.* A label expressed in a pseudo-code. To code using symbolic addresses implies that the sequence of instructions must be translated into absolute before being executed by a computer. Relative addresses are those symbolic addresses which are translated into absolute by sequencing from some specific "reference" address.
- Band.* An addressable area on the Data Record File. A band is a spiral groove around the record with a storage capacity of 9000 characters. Each band contains 10 cells of 900 characters each.
- Batch.* Several groups of items in sequence, each separated by a sentinel and the entire grouping terminated by an EF. (This is contrasted to a single group of related items for a message.)
- Beginning of Tape Control (BTC).* A "window" placed at the beginning of a magnetic tape, where recording of data is not possible and which can be sensed photo-electrically.
- Binary Code.* A code composed of a combination of entities each of which can assume one of two possible states. Each entity must be identifiable in time or space.
- Binary Digit.* A digit (0 or 1) in binary notation. See Digit.
- Binary Notation.* A system of positional notation in which the digits are coefficients of powers of the base two. Synonymous with Binary Representation. See Positional Notation.
- Binary Representation.* Synonymous with Binary Notation. See Positional Notation.
- Binary-to-Decimal Conversion.* The mathematical process of converting a binary number to the equivalent quantity in decimal notation. For example: 001-1, 010-2, 011-3, 100-4, 101-5, etc.
- Bit.* A single binary digit having a value of either zero or one. The word is a contraction of "Binary Digit."
- Block.* A group of consecutive data considered or transferred as a unit, particularly with reference to input and output. On magnetic and paper tape a block is a group of at least three characters preceded and followed by a space called an "inter-block gap". On the Data Record File Disc a Block is the information contained in one cell. From one through 900 characters of information may be recorded in a cell.
- Buffer.* A storage device used to compensate for a difference in rate of flow of information or in time of occurrence of events when transmitting information from one device to another, as from an input device to the High-Speed Memory, or from the High-Speed Memory to an output device.
- Bus.* A main circuit, channel, or path for the transfer of information.
- Card.* Any card adapted for being punched in an intelligent array of holes for the storage of information.
- Card Column.* One of a number of columns in a card into which information is entered.
- Card Feed.* A mechanism which moves cards one by one into a processing device.
- Card Punch.* A mechanism which punches cards. An automatic card punch punches cards according to a stored program.
- Card Reader.* A mechanism that reproduces the information on cards in another form, usually electrical signals.

## APPENDIX IX: GLOSSARY OF TERMS (Continued)

*Card Stacker.* A mechanism that stacks cards after they have passed through a machine.

*Carry.* (1) A condition occurring during addition when the sum of two digits in the same column equals or exceeds the base number. (2) The digit to be added to the next higher column.

*Cell.* An addressable area on the Data Record File. A cell may contain from one to 900 characters.

*Character.* One of a set of elementary symbols which may be arranged in ordered aggregates to express information. These symbols, typewrite symbols, and any other symbols which a computer may read, store, or write.

*Code (noun).* A system of symbols and rules for their use in representing information. A language.

*Pulse Code.* The binary representation of characters.

*Operation Code.* The code representing an operation (add, subtract, transfer, etc.) built into the hardware of the computer.

*Complement (noun).* A quantity which is derived from a given computer quantity by the following rules:

a. Complement on  $n$  (as in tens complement). Subtract each digit of the given quantity from  $n-1$ , add unity to the least significant digit, and perform all resultant carries.

b. Complement on  $n-1$  (as in nines complement). Subtract each digit of the given quantity from  $n-1$ .

*Constant.* A number is said to be a constant if it has the same value under all conditions. For example, in the formula (area of a circle) =  $\text{Pi} \times (\text{radius})^2$ ,  $\text{Pi}$  is a constant, equal to 3.14159 - - -, which applies to all circles.

*Control Symbol.* A character used to indicate the beginning or the end of unit of data (item, record, file, etc.).

*Counter.* A device (register or storage location) for storing integers, permitting these integers to be increased or decreased by units or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer.

*Criterion (Key).* A group of characters, usually comprising an item, used to identify a record.

*CTC.* Conditional transfer of control.

*Decimal Number System.* See Positional Notation.

*Diad.* A unit consisting of two consecutive HSM locations. Each diad begins with an "even" decimal address and ends with the next consecutive "odd" address.

*Digit.* One of the  $n$  symbols of integral value ranging from 0 to  $n-1$ , inclusive, in a scale numbering of base  $n$ . Examples of various types of digits are:

Binary Digits are 0 to 1

Octal Digits are 0 through 7

Decimal Digits are 0 through 9

*Direct Address.* The specific label assigned by the machine designer to a particular storage location. Synonymous with *Absolute Address*.

*EB.* End of Block Symbol.

*ED.* End of Data Symbol.

*Edit.* To rearrange information. Editing may involve the deletion of unwanted data, the selection of pertinent data, the insertion of invariant symbols such as page numbers and typewriter characters, and the application of standard processes such as zero suppression.

*EF.* End of File Symbol.

*EI.* End of Information Symbol.

*End Data Symbol.* A symbol which the computer interprets as meaning there is no data following the symbol. For example, the last character on a magnetic tape is the End Data Symbol.

## APPENDIX IX: GLOSSARY OF TERMS (Continued)

*End-Around-Carry.* A carry in which the overflow from the column of highest order is added to the column of lowest order.

*End of Tape Warning (ETW).* A warning generated by a metal strip on the tape indicating that approximately 5 feet of usable tape is available.

*End File Symbol.* A symbol which the computer interprets as meaning all Data pertaining to a file precedes the symbol. For example, the last character in a file is the End File Symbol.

*Erase.* 1. To expunge, wipe out, or destroy stored information, usually without destroying the storage media.  
2. To replace all the binary *digits* in a storage cell by binary zeros.

*f.* Used as subscript to denote final.

*Field.* A set of one or more characters which is treated as a whole; a unit of information.

*File.* The complete group of records to be processed. For example, the data relative to one employee in a payroll application is a record; the total records for all employees constitute a file.

*Flip-Flop.* A device having two stable states and two input terminals (or types of input signals), each of which corresponds to one of the two states. (The two states may be considered as corresponding to "off" and "on" or to binary 0 and 1. The circuit remains in either state until it is caused to change to the other state by application of the corresponding signal.

*Gap.* A blank space on magnetic or paper tape. The gap is used to separate blocks or other units of data.

*High-Speed Memory.* Magnetic core storage in the Computer in the RCA 301 System. See also Storage.

*High-Speed Memory (HSM) Location.* A unit of magnetic core storage (High-Speed Memory) which can store (hold, remember) one RCA character. See Address.

*HSM.* High-Speed Memory.

*i.* Used as subscript to denote initial.

*Indirect Address.* The address of a memory location whose contents contain the address of another memory location to be accessed.

*Input.* (1) Information transferred into the computer. (2) The device by means of which information is fed into the computer.

*Instruction.* Information which conveys to a machine where the operands are obtained, what operations to perform, what to do with the result, and sometimes, where to obtain the next instruction.

*Instruction Code.* An artificial language for expressing the instruction to be carried out by a machine.

*Item.* An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.). In many cases an item is preceded by a symbol to define the beginning of each item.

*Item Separator Symbol (ISS).* Control symbol which may be used to designate the beginning of an item.

*Jump Table.* Record indicating executed transfers out of program sequence.

*Justify.* Shift an operand to effect right or left columnar alignment.

*KC.* Thousand characters per second.

*Key.* See Criterion.

*Line.* A line is composed of the characters that are to be printed on a single line on the On-Line Printer or Monitor Printer. Each character space to appear in the printed line decreases the maximum line capacity by one.

*Line Printer.* A printing device capable of printing an entire line of characters at one time.

## APPENDIX IX. GLOSSARY OF TERMS (Continued)

*Location.* A storage position in the High-Speed Memory. Each location has a specific address and can hold one RCA character.

*LSC.* Least Significant (rightmost) character.

*LSD.* Least Significant (rightmost) Digit.

*L to R.* Left to Right.

*Machine Language.* A language occurring within a machine, ordinarily not perceptible or intelligible to persons without special equipment or training.

*Magnetic Storage.* Any device which makes use of the magnetic properties of materials for the storage of information.

*Magnetic Tape.* A ribbon of paper, metal, or plastic, coated or impregnated with magnetic material on which information may be stored in the form of magnetically polarized areas.

*Mask.* A pattern consisting of 0 and/or 1 bits, used to alter the bit configuration of an operand.

*Memory.* See Storage.

*Message.* The data relative to a single item to be processed. For example, all data relative to a single inventory item is a message. See Record.

*Microsecond.* A millionth of a second.

*Millisecond.* A thousandth of a second.

*Mnemonic Code.* A pseudo-code in which information, usually instructions, is represented by symbols or characters which are readily identified with the information.

*MSC.* Most Significant (leftmost) character.

*MSD.* Most Significant (leftmost) Digit.

*N.* Number of characters (used in timing).

*Number System.* See Positional Notation.

*Octal.* See Positional Notation.

*Octal Digit.* One of the symbols 0, 1, 2, 3, 4, 5, 6, or 7 when used as a digit in octal notation.

*Octal Notation.* Notation of numbers in the scale of eight. The octal digits can be represented by the eight possible combinations of three binary digits.

*Octonary.* See Positional Notation.

*Operand.* Any one of the quantities entering into an operation.

*Output (noun).* (1) Information transferred from the computer to external storage. (2) The device to which the computer delivers information.

*PA.* Paper Advance.

*PC.* Page Change.

*Positional Notation.* One of the schemes for representing numbers, characterized by the arrangement in sequence of digits which are to be interpreted as co-efficients of successive powers of an integer called the base of the number system.

In the *binary* number system the successive digits are interpreted as co-efficients of the successive powers of the base 2, just as in the *decimal* number system they relate to successive powers of the base 10.

In the ordinary number systems the digits are symbols which stand for zero and for the positive integers smaller than the base.

*PRI's.* Previous Result Indicators.

## APPENDIX IX. GLOSSARY OF TERMS (Continued)

*PRN.* Previous Result Negative Indicator.

*PRP.* Previous Result Positive Indicator.

*PRZ.* Previous Result Zero Indicator.

*Random Access.* Access to storage under conditions in which the next position from which information is obtained, or to which it is delivered, is in no way dependent on the previous one.

*RCA Character.* See the RCA 301 Code, Appendix.

*Record.* A record consists of one or more related items with the amount of information in a record being completely variable.

*Register.* A storage device with a specifically assigned function and a given unit capacity. Registers in the computer in the RCA 301 System are of one, two, or four character capacity.

*Relative Address.* An address which specifies a location sequentially relative to a group of addresses but not a specific storage location.

*Rewind.* Move a tape in a backward direction to BTC.

*Routine.* A set of instructions arranged in proper sequence to cause a machine to perform a desired operation.

*R to L.* Right to Left.

*RWD.* Rewind.

*Sector.* An addressable unit of information on the Data Disc File. One sector contains 160 characters. Ten sectors are contained in one track.

*Sign Position.* The sign of each operand is indicated by the  $2^5$  bit of the least significant digit (LSD) of each operand. When a "one" bit is present in the  $2^5$  position, the sign is negative, otherwise it is assumed positive.

*Simultaneity.* The ability of the computer to execute more than one instruction at the same time.

*STA.* Store A Register (automatic storage of final contents of A Register).

*Standard Memory Locations.* Designated locations in the HSM which are used for Arithmetic Tables, automatic storage of the final contents of certain Registers, etc. (See Appendix.)

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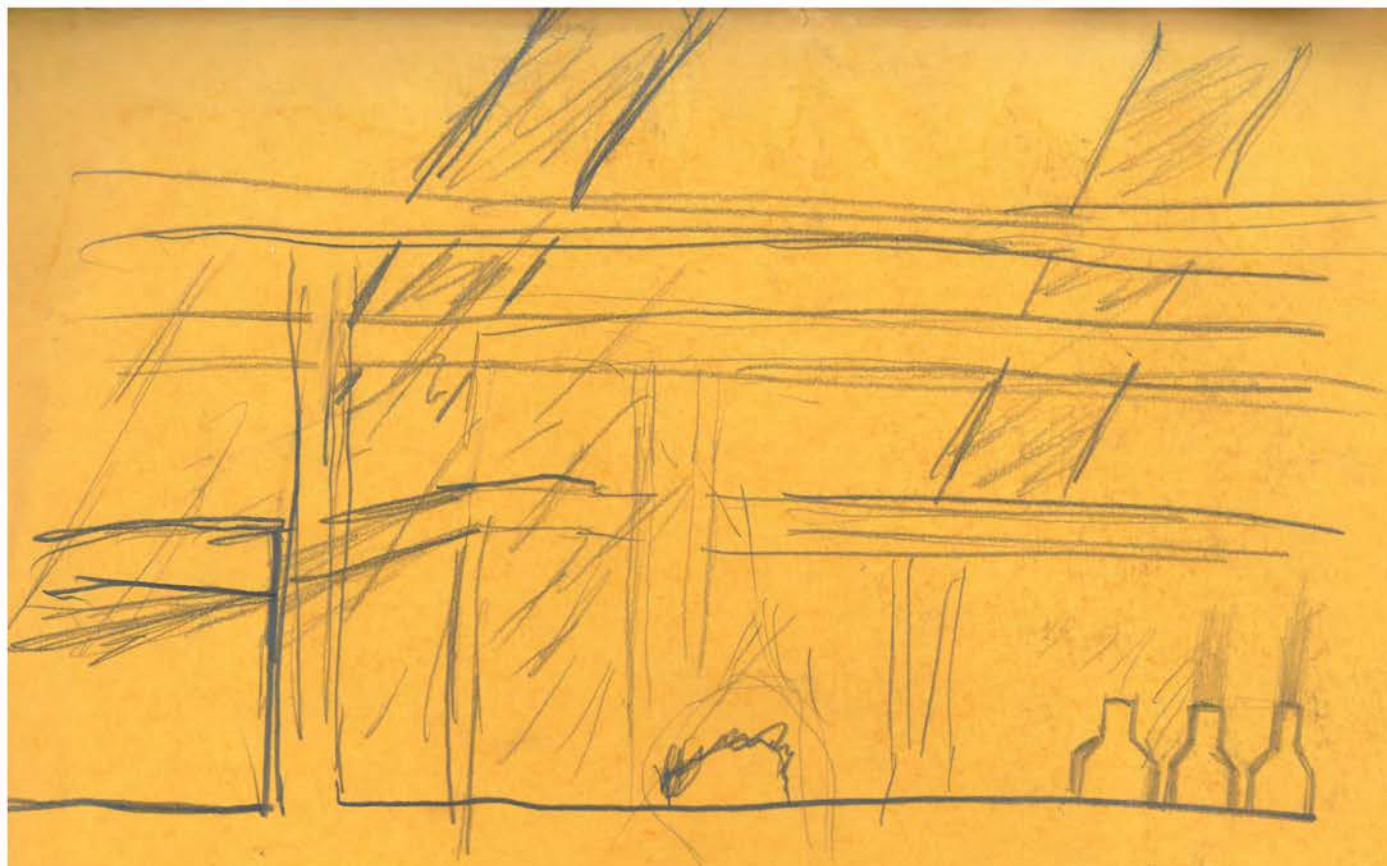
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