

DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION

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Gordon D. Goldstein, Editor
Jean S. Campbell, Asst. Editor

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Approved by
The Under Secretary of the Navy
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COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

MANIAC III - UNIVERSITY OF CHICAGO - CHICAGO, ILLINOIS

The arithmetic unit of Maniac III has two separate and distinct modes of operation. The first is the familiar floating point system with the exception that the usual normalization step at the end of each operation is omitted. Instead, the treatment of results corresponds to one of several possible significant digit arithmetics. A complete discussion is in press. The second mode is an unconventional fixed point scheme that permits wider application with greater ease. Indeed double, or multiple precision floating point arithmetic can be handled in a rather straight-forward manner with this approach.

Construction of the arithmetic unit of Maniac III is approximately one-half completed. All arithmetic registers and the adder are finished, and are under test operation with a minimum section of the control. Surface-barrier and micro-alloy transistors are used throughout. All circuits are assembled on etched circuit cards (double-sided) which are inserted into multiple contact connectors. A novel form of gating circuit is employed which relies principally on diodes for logical elements, and minimizes the need for transistors. All circuits are direct coupled, and the control is asynchronous. About 4,000 transistors and 16,000 diodes are needed for the complete arithmetic unit.

AUTOMATIC ERROR-CORRECTION - DATAMATIC - NEWTON HIGHLANDS, MASSACHUSETTS

DATAMatic Division of Minneapolis-Honeywell has developed ORTHOTRONIC CONTROL, an automatic error correction technique which almost entirely overcomes tape errors.

The DATAMatic tape is divided into 36 tracks or channels which extend longitudinally along the tape. 31 of these channels are used to store information words, of which 62 can be recorded in a unit block on tape. Of the remaining 5 channels, one is a spare, three are allocated for control purposes and one is the Monitor Channel (Orthochannel). The words are recorded in a staggered fashion on every other block with the tape moving in a forward direction. At the physical end of the tape the motion is reversed and the alternate blocks are recorded. It is in this manner that the interlace recording system of the DATAMatic 1000 omits the usual "dead" spaces required for tape acceleration and deceleration.

Each DATAMatic word is composed of a collection of 52 binary zeroes and ones numbered from 1 through 52 when read from right to left. The four bit (binary digit) positions on the extreme right of each word (positions 1 through 4) are employed as the Weight Count digit, a checking device. This 4-bit digit is automatically generated and appended to each 48 bits of information introduced or generated with the computer. It provides a verification of the accuracy of all word transfers and arithmetic and logical manipulations. It is important to note that every word, be it numeric, alphanumeric, or instruction, is treated as numeric (4-bit) for the computation of its weight count.

Associated with each of the 48 information bits in a word is a number 1, 2, 4, or 8 called the weight for the related bit position. For example, bit positions 5, 6, 7, and 8 have the weights of 1, 2, 4, and 8 respectively. The weight count of each word is determined as follows and appears in bit positions 1 through 4.

1. Calculate the decimal sum of the weights where binary ones occur in bit positions 5 through 52.
2. Divide this sum by nine and obtain a remainder digit having a value of from zero to eight.
3. If the remainder digit is zero, the weight count appears as a nine.

4. If the remainder digit has a value of from 1 to 8, the weight count digit is precisely this value.

Whenever a word is transferred from the Input Buffer to memory, the weight count is recomputed and checked against the original. If an incorrect count is detected indicating that the word is incorrect, the DATAmatic 1000 utilizes ORTHOTRONIC CONTROL to regenerate the original information. It is important to note that this procedure is initiated only when an error is evident.

To simplify the explanation of the development of the Orthochannel, only three data channels will be considered although the same reasoning will apply when using up to 31 channels. If the sum of the "1" bits in position 52 of words 1, 3, and 5 is an odd number, then Orthobit 52 of the word in the Orthochannel is a "1." However, if there is an even number of "1" bits in those information positions, bit 52 of the Orthochannel is a "0". This Orthoaddition method of construction is repeated for all information and weight count bits of the odd-numbered words. This produces the first 52 bits of the Orthochannel, and constitutes the first Orthoword. Furthermore, this process is repeated for the even-numbered words within that block to obtain the second set of 52 bits to complete the construction of the Orthochannel. It should be pointed out that all 52 Orthobits are summed simultaneously.

The procedure described above occurs in circuitry which is located between the memory and the Output Buffer section of the computer. This Output Buffer is a temporary storage location for 62 words prior to their transfer to magnetic tape. By the time all 62 of the data words that are to be written as a block of information on the tape have been assembled in the Output Buffer, the two words of the Orthochannel have been constructed and are ready for the actual recording operation. This process, therefore, requires no additional machines or programming time. When the appropriate instruction is given by the Control Unit of the system for writing on tape, 32 channels are recorded simultaneously—31 channels of information and the Orthochannel. This then completes the first phase of the operation.

When, at some subsequent time, the information on this tape is read back into the Central Processor, it is at this point that the actual corrective procedure will be initiated, if necessary. When the instruction is given via the Control Unit to read the tape, all 32 channels are read simultaneously into the Input Buffer section. The next step in the normal sequence of operation is to transmit the information from the Input Buffer to the Memory section of the machine. It is at this stage that data is verified for accuracy by applying the normal weight count check. If the information content (the first 48 bits) of a word does not agree with its weight count, it is known that this word has certain inaccuracies within the body of its information. Previously when this was determined, certain alternatives were open to the programmer. He could stop the machine or could attempt to re-read the information in the hope that upon the second reading the information would be found to be correct. With Orthotronic Control, however, an entirely different and completely constructive action is taken. If the word is found to be inconsistent with its weight count, the operation is directed to memory register 1987. The instruction stored in 1987 leads to a subroutine, devised by the programmer, which used the Orthochannel to correct the error. Before initiating the correction procedure, the subroutine may, as one of many alternatives, cause the entire block of data to be re-read from tape into the buffer. A new Orthomonitor Transfer In instruction, one which includes the transfer of the Orthotronic Monitor Channel, is then used to bring into memory the entire block. When all 64 words have been entered into memory a special Add instruction, which has been included in the repertoire of instructions, then enables the machine to regenerate the original data. If, for example, an error exists in an odd-numbered word, all other odd-numbered words in that block (including the Orthoword) are specially summed by this newly-developed instruction and the result obtained is the authentic, original and correct version of the inaccurate word. The table shows how this is accomplished. Assume that word 1 (which would be located directly above word 3) became garbled or lost, word 3, word 5, and the Orthoword are added by the Orthotronic Add instruction. As a result of the uniqueness of binary mathematics, this simple addition enables the machine to reconstruct the erroneous word into its original form. The same reasoning may be applied regardless of the number of channels involved.

| | | | | | | | | | |
|-----------|--------|--------|--------|--------|--------|--------|--------|--------|------|
| Word 3 | 000001 | 001000 | 000111 | 010000 | 100111 | 010001 | 101001 | 100010 | 0100 |
| Word 5 | 100101 | 010101 | 110110 | 010000 | 111000 | 100110 | 101001 | 100010 | 1001 |
| Orthoword | 000101 | 001100 | 010101 | 010101 | 101101 | 100111 | 010011 | 011011 | 1011 |
| <hr/> | | | | | | | | | |
| Total | 100001 | 010001 | 100100 | 010101 | 110010 | 010000 | 010011 | 011011 | 0110 |
| | J | A | M | E | S | space | C | | |

Errors in any two words within the same block, even though in different channels, are correctable if one occurs in an odd-numbered word and the other in an even-numbered word. Oxide flaking and dust particles on the magnetic tape contribute to the greatest percentage of errors in data processing equipment. Of the few which do crop up, the majority affect only one channel and can, therefore, be corrected automatically by the machine. In relatively infrequent instances, particles of dust or foreign matter may be large enough to affect two adjacent channels. The majority of these errors are correctable, since the words are arranged on the tape in a unique staggered fashion. In most cases, therefore, these particles will influence an odd and an even word within the same block or two odd or two even words in adjacent blocks. All of these situations are correctable. The correction procedure outlined above is initiated by the machine only when an error is detected. If the information is correct, the machine follows its regular routine since the Orthotronic Add instruction is not required. The weight count digit appended to the Orthoword is not the actual weight count of that word but rather the Orthosum of the weight of all companion words. Therefore if an information word is reconstructed using a defective Orthoword, its Orthocorrected weight count will not agree with its originally computed weight count. In practice, this may be checked by the Orthotronic Add instruction. This provides a means for double checking each correction. If the Orthocorrected information does not have a valid weight count, it obviously was regenerated using a defective Orthoword.

There are a few instances where the machine alters the procedure outlined above. If, by some remote possibility, errors occur in two odd-numbered words or in two even-numbered words within the same block, the programmer may select any of several alternatives. In many of these cases it will be found that after the alternatives have been tried, the error will have been eliminated. In those rare instances where none of these methods is effective, the computer will begin the regular detection subroutine. This eliminates any possibility of an inaccurate word being carried through the system.

Orthochannels are also generated within the Input Converter. The DATAmatic 1200 Card Input System is used to read punched card information and to convert it to a binary representation for writing on magnetic tape. Each punched card is converted to one 16-word record or blockette on tape: 14 words derived from the card, one word of identification and one control word. Two such records are written on each tape block. In addition, circuitry is now being added to the Input converter to include two Orthochannels, one for each blockette. Each blockette carries its Orthochannel until the card data is transferred into Central Machine memory and is confirmed. The contents of the blockettes may then be processed, and conveyed to the Output Buffer where the data is assembled for writing onto magnetic tape. When a Write instruction is given, a new Orthochannel is generated for each block.

DOCUMENT DATA PROCESSING SET, AN/GSQ-13(XW-1) -
U.S. AIR FORCE - WASHINGTON, D.C.

The Document Data Processing Set is a general purpose computer especially designed for problems requiring a high degree of correlating ability. Specialized commands have been designed for data entry, data reorganization, and data look-up so as to facilitate decision making. The set is being used to control the dissemination of documents to organizations and individuals interested in specified subject areas. The internal memory file contains the set of customer requests against which the document coverage is compared.

The main memory is a magnetic drum, 16" in diameter, rotating at 1800 rpm. It has been designed for capacity up to 22,000 words of storage, each word consisting of ten alphanumeric characters. Information is recorded in channels each divided into 100 sectors. A word of information can be stored in any sector in any channel. Provision has been made for up to 220 channels for the total capacity of 22,000 words of storage.

Information is represented as fixed length words, each containing 60 bits. A single such word may be used to represent 10 characters of alphanumeric data, 15 characters of numeric data, or a command. The command word consists of: three decimal digits, which specify the operation, five which specify the address of the operand, and five which specify the address from which the next command is to be taken. Such a structure is frequently called a "one-and-one" address command.

Checking features are: Storage of an additional bit with each word to serve as a parity check. Checks to verify the reliability of the internal logical elements by checking the consistency of the counters, the timing circuitry, the instruction execution, and the state of decision elements. The operation of the input device is checked by a parity bit for each character input.

Programs have been prepared for controlling the Document Data Processing Set in the determination of groups or individuals interested in particular documents. Requests for information form the basic file against which incoming documents must be compared. These requests specify subject and area of interest together with other qualifying data (such as evaluation, type of copy desired, etc.) and the identification of the customer making the request. The requests are stored internally on the magnetic drum, one to each word. The capacity has been designed for storage of up to 20,000 requests.

A dissemination operation involves the following steps. The subject and area coverage of a document, which were previously punched into punched paper tape, form the input. The individual words must be grouped by the Document Data Processing Set into phrases of the same structure as the stored requests. Since several combinations of subjects and areas may be covered by the document, the phrases describing the coverage given by the document must be analyzed and all valid combinations searched against the file.

The file search commands have been designed so that generically coded requests will pick up all relevant documents concerned with sub-categories. Each valid subject-area coverage of the document is searched against the file of requests. The result will be the output of a list of requestors for the document and, if desired, the area of interest for each requestor.

The file handling commands have been designed to facilitate the addition of new requests to the file and the deletion of out-moded requests. Programs have been prepared for complete listings of the file of requests, in order by requestor identification. These can thus be screened for need to know, etc.

A library of sub-routines for other operations has been prepared. This can be expanded, and the machine applied to a number of other tasks such as: file indexing, item coding and translation, pattern recognition, etc.

The system has been in operation since July 1958 at the Headquarters, U. S. Air Force, and was manufactured by the Magnavox Research Laboratory, Los Angeles, California.

COMPUTING CENTERS

DATA REDUCTION LABORATORY - AIR PROVING GROUND CENTER - ELGIN AFB, FLORIDA

An IBM type 738 Magnetic Core Storage Unit with 32,768 words, was installed in the 704 system replacing the two 737's.

Elgin Air Force Base's Civilian Payroll accounting was mechanized for the 704. Now being used for confidence checking against the previous methods, the payroll program will start independent operation and actual check preparation with the last quarter of this year. This program is believed to be a first for payroll preparation in the Air Force on a 704 computer.

Bendix Computer Division has delivered a Telemetry reception, digital conversion and Univac Scientific Computer input system which is being acceptance tested. The equipment will permit quick, or even real time telemetry data reduction.

Further telemetry and magnetic tape data reduction facilities have been assembled into the system called TELEMAC, of which the Bendix equipment is a subsystem. This facility provides a broad and general capability for analog and digital data processing (see Digital Computer Newsletter, January 1958).

SWAC - UNIVERSITY OF CALIFORNIA - LOS ANGELES, CALIFORNIA

A magnetic core memory, utilizing RCA ferrite core plates, is under construction. A revision in assembly procedure as well as in internal arrangement of the plates allows modules of 16 words, each of 48 bits, to be constructed. Each module contains its own driving and sensing circuitry. Amplifiers and coding network are separately mounted. All circuitry is transistorized and on printed circuit boards. The modular method of assembly permits replacement of an individual plate if defects or malfunctions make this necessary.

The core memory will have a capacity of 256 words of 48 bits each. It is now planned to operate this memory in conjunction with the 256 word electrostatic memory to provide enhanced storage. Two logical control methods are being considered. Either the internal logic of the computer will be altered to permit independent addressing of either memory without increase of word length, or the word length will be increased and the four address logic left unchanged. No decision has been reached on this as yet.

Preliminary plans have been made for moving SWAC to new quarters in October 1959. Most of the wiring between the main sections of the computer will be replaced with modern cabling, and multi-prong plug and receptacle connections will replace the present soldered terminal boards. The core memory will be installed and tested before the move. The computer will be "off the air" for approximately 3 months. It is planned to install a new console at the new location, and design work on this project has begun.

The computer has been operated at somewhat lowered efficiency during the last few months. Some time has been assigned to wire tracing in preparation for the removal, and considerable time has been spent on a study of the arithmetic organ. Some experiments to determine faults in the design of the adder have led to circuit alterations which have improved the operation for this portion of SWAC. Further studies of undesirable side effects of the alterations are going on. It is expected that the arithmetic organ can be improved further.

The work on SWAC continues to be done by graduate research assistants and undergraduate technicians, all working part-time. The magnetic core memory is being constructed completely in our laboratories at Numerical Analysis Research. Techniques in printed circuitry construction and dip soldering are being developed. Valuable training in the field of practical shop work, as well as in logical design and theoretical research is being provided to these students.

AERODYNAMICS LABORATORY - DAVID TAYLOR MODEL BASIN - WASHINGTON 7, D. C.

The Aerodynamics Laboratory of the Navy's David Taylor Model Basin has added an Alwac III-E digital computer to its data processing systems. For several years an Alwac II has been used to process data from the Laboratory's Transonic Wind Tunnel. Now the output of data from two Subsonic Wind Tunnels is automatically put on punched paper tape. Either 6 or 12 channels of information can be accommodated, together with several channels of semi-automatic identification data. The tapes are then fed to the Alwac III-E computer, which furnishes tabulated corrected data, ready for analysis and reporting.

AEC COMPUTING AND APPLIED MATHEMATICS CENTER -
NEW YORK UNIVERSITY - NEW YORK, N. Y.

UNIVAC I System. Recent machine modifications include the following:

1. The installation of a manually operated system to facilitate the assignment of any computer number to any servo. Positioning of an eleven-position switch located at the servo which simultaneously selects one of ten computer numbers, indicates the one selected by lighting an enditron, and provides a warning if another servo has been assigned the same computer number.

2. An addition to the N.Y.U. instruction code based upon a previously reported modification (Digital Computer Newsletter, October 1957) of the Univac Control Counter. This instruction, known as R1, may be either programmed or manually selected. Although of restricted usefulness, its effectiveness in aiding debugging of new codes will save much computing time.

3. A "Last Read Indicator" has been installed. The last read indicator performs the function of indicating, at supervisory control, the last servo which was moved in a read operation. The device is useful for the following reasons:

- a. Allows operator to rock a tape without identifying the servo.
- b. Records the last servo read in case of bad I tank to memory transfer, which allows the saving of the program in many cases.
- c. The indicator allows a programmer to follow his tape movements in debugging.

Since the indicator is separate from the machine operation, no machine down time is necessary during the installation other than the connections to the backboards.

Machine time is readily available at present on the UNIVAC I. There is no charge to AEC contractors, and contractors of other government agencies can be allotted time at established hourly rates.

Inquiries should be addressed to Professor R. D. Richtmyer, Director, AEC Computing and Applied Mathematics Center, 4 Washington Place, New York 3, New York.

MATHEMATICS DEPARTMENT - U.S. NAVAL ORDNANCE LABORATORY,
WHITE OAK - SILVER SPRING, MARYLAND

NOL expects to take delivery of an IBM 704 in January 1959. This computer will replace the two IBM 650's presently in operation at the Laboratory.

The former Applied Mathematics Division at the Naval Ordnance Laboratory has recently been elevated to departmental status. It is now known as the Mathematics Department and contains two new Divisions, the Mathematical Analysis Division and the Mechanized Computations Division.

NAVAL ORDNANCE COMPUTATION CENTER -
U. S. NAVAL PROVING GROUND -
DAHLGREN, VIRGINIA

Hardware is now being assembled for the Universal Data Transcriber (UDT), scheduled for completion early in 1959. Logical design of the UDT is being tested by a simulation routine on the NORC. Another NORC routine is being used to select, among several wiring layouts, the one resulting in minimum wire lengths and absence of excessive loading on individual logic circuits. Input-output media initially provided for will be NORC tape, punched cards, and punched tape; others will be added as needed.

Another conversion device has been completed and tested, its use being needed earlier than the expected completion of the UDT. This special purpose device accepts three-decimal-digit-and-sign samples from an analog-to-digital converter at the rate of 6,000 samples per second, and writes the samples on NORC tape.

A contract has been awarded to Daystrom Instrument for a 20,000 word ferrite core memory with eight microsecond cycle, to replace the present 2,000 word Williams tube memory of the NORC. Delivery is due in mid-1959.

The Aiken Dahlgren Electronic Calculator (ADEC) has been dismantled after being idle for some months. Completed in early 1950 by the Harvard University Computation Laboratory under Professor Howard Aiken, the ADEC was the pioneer among large magnetic drum calculators.

DIGITAL COMPUTATION BRANCH (WCLJU) - WRIGHT AIR
DEVELOPMENT CENTER - WRIGHT-PATTERSON
AIR FORCE BASE, OHIO

The Scientific Computation Facility of the Wright Air Development Center now uses two Univac Scientifics to solve the engineering problems that arise in the Center. The first Model 1103 with magnetic core storage was installed January 1956 and has been in three shift operation since July 1956. For the first seven months of 1958, average power-on time (excluding two hours of preventive maintenance per day) was 468.9 hours per month. For the same period emergency maintenance averaged 3.9 hours per month and reruns, due to computer malfunction, averaged 4.1 hours per month. Thus the computer was available 460.9 hours per month, an efficiency of 98.3% of power-on time.

The newer Model 1103A was installed May 1958. One shift operation has been used since 2 June 1958 with a second shift scheduled for January 1959. The average efficiency was 97.9% of power-on time for June and July. The equipment includes 12,288 words of core storage, floating point feature, 8 Uniservos, high speed printer (on or off-line), Bull Reproducer, etc.

The OARAC Computer, built in 1952 by the General Electric Company, is presently undergoing extensive modifications, including a 10,000 word core storage. It will be used in the future as a research computer under an "open-shop" operation by the Aeronautical Research Laboratory.

COMPUTERS, OVERSEAS

GAMMA 60 - COMPAGNIE DES MACHINES BULL - PARIS, FRANCE

Note.—The following informal review of the GAMMA 60 characteristics was contributed by Mr. Harry Hayman, U. S. Navy Bureau of Ships (Code 687E), Washington 25, D. C. Additional information concerning the machine may be obtained from the Compagnie des Machines Bull, 94, Avenue Gambetta, Paris, France.

The GAMMA 60 computer manufactured by the Bull Company, Paris, France is a high-speed solid state computer designed for data processing. It is based on the concept that the memory is the most expensive portion of the computer and therefore should be kept busy all the time. The memory is used as a buffer between all units.

Before proceeding, a discussion of the basic word length is necessary. The basic word is 24 bits, however, this is not a true word, but called a CATENA. The various units can operate on variable CATENA lengths, with the exception of the arithmetic unit which always operates on two CATENAs. To conserve memory space the arithmetic unit operates on a four bit binary

coded decimal digit; the program word, which may be one, two, or three CATENAs long is in binary; and the input-output and other units can operate on a six bit binary coded alphanumeric.

The individual units within the system are:

- | | |
|--------------------|-----------------------|
| 1. Arithmetic Unit | 6. Card Reader Unit |
| 2. Logical Unit | 7. Paper Tape Unit |
| 3. Compare Unit | 8. Magnetic Tape Unit |
| 4. Translate Unit | 9. Magnetic Drum Unit |
| 5. Printer Unit | 10. Card Punch Unit |

All of the individual units communicate directly with the core storage. They cannot communicate with each other except through the program distributor. Each unit is a little computer within itself. Each unit besides performing its basic function consists of a simple adder (to add or subtract one from its current address register), three current address registers (instruction counters), programming register, and one CATENA input and output buffer.

To provide the central control for these various units there is a program distributor, which receives from all units requests for instructions; and a transfer distributor which receives, from all units, requests for data. The magnetic core memory has an 11 microsecond access time for each CATENA. Therefore not all units can refer to the memory simultaneously and the program distributor has priority circuits to control the access to memory. Because the slowest units are mechanical in nature and difficult to stop they have the highest priority to memory, and the fastest units, which are electronic and can easily be stopped, have the lowest priority to memory. Priority is as follows:

- | | |
|----------------|------------------|
| 1. Card Reader | 5. Magnetic Tape |
| 2. Card Punch | 6. Arithmetic |
| 3. Printer | 7. Logical |
| 4. Drums | 8. Compare |

Thus if we consider the arithmetic unit, it will start with a C type instruction which will cut it into operation. If the program it is working on is in location 101 it will start at location 101 and continue on until it reaches the next C or cut type instruction. The arithmetic unit then looks at its next current address register, which tells it where the next series of instructions for the arithmetic unit begins. This information has previously been supplied by the program distributor. After each operation every unit sends one CATENA of information back to the program distributor, which supplies error, transfer, and other information to the program distributor.

In order to operate units simultaneously, there is a conditional transfer instruction which is an "and" type operation and can call for cut instructions to two different units. As many of these transfers as are necessary to put the desired units into operation may be used. There is also a regrouping conditional transfer which will prevent the transfer until each of the units have reported that their work has been completed.

Other features of the computer are:

1. Transistor, diode, and magnetic core logic.
2. No off-line equipment.
3. Variable CATENA operation.
4. One, two, and three address instructions.
5. Each CATENA individually addressed. 4096 to 32,768 CATENA memory.
6. 4 alphanumerics or 6 numerics per CATENA.
7. Indirect addressing may continue indefinitely.

8. Two and three address compare instructions in many forms and in variable CATENA word length.

9. 11 millisecond average access time for the drum. 44 microseconds transfer time per CATENA for drum. 32,768 CATENA on each drum.

10. 11 microseconds for a comparison.

11. Arithmetic speeds (decimal, floating point):

| | |
|----------------|----------------------|
| Addition | 100 microseconds av. |
| Multiplication | 300 " " |
| Division | 600 " " |

All arithmetic operations 2 CATENAs in length.

12. \$1.5 million purchase price for basic system with 4096 CATENA memory.

13. Engineering prototype now in production to be completed by April 1959. 1st delivery of commercial model scheduled for October 1959.

14. No plugboards provided on input-output unit. All editing done by translate unit with special instructions using three address instruction.

- A. Address of information to be edited
- B. Format address
- C. Address to store result

15. Logical operations 20 microseconds plus access time.

16. Uses about 15,000 U.S. transistors for the entire computer, General Ceramic cores, and Electrodata or Ampex tape units.

17. 120 character line printer, 300 lines/minute.

18. Checking:

A. Three extra bits per CATENA which give a remainder when divided by seven. During addition divides the addend, augend, and total by seven, and compares the sum of the remainders with the remainder of the sum.

| | |
|-----|------------|
| | Remainders |
| 31 | 3 |
| +43 | +1 |
| 74 | 4 |

B. Card reader reads two or three times. Compares first and second reading. If necessary makes third reading and selects correct reading of first two.

- C. Card punch reads after punch.
- D. Echo check on print.
- E. Reads paper tape after punch.
- F. Reads paper tape twice.
- G. Compares memory address with that actually requested.

19. Reads 300 cards/minute.

Comparison of GAMMA 60 with IBM 705

| | GAMMA 60 | IBM 705 |
|---------------------------------------|----------------------|--------------------|
| Add | 100 microseconds | 119 |
| Multiply | 300 " | 1819 |
| Input (120 digits - Memory time only) | 242 " | 1141 |
| High speed memory access | 11 (4 alphanumerics) | 9 (1 alphanumeric) |
| Arithmetic | Fixed and floating | Fixed |

Memory Access Time (Microseconds)

| | GAMMA 60 | IBM 705 |
|----------------------------|----------|---------|
| 6 Decimals | 11 | 54 |
| 4 Alphanumerics | 11 | 36 |
| Single address instruction | 11 | 45 |

In comparing the two computers it should be remembered that if memory is kept busy on the 60, several operations may be performed simultaneously, whereas on the 705 only input-output and one computer operation may be performed simultaneously. Also one memory reference in the 60 is the equivalent of 4 alphanumeric or 6 decimal references in the 705.

MERCURY - FERRANTI, LTD. - MANCHESTER, ENGLAND

Ferranti Mercury High Speed Electronic Computers are now in use at:

U. K. Atomic Energy Authority, Harwell.
French Atomic Energy Authority, Paris.
Norwegian Defence Research Establishment, Oslo.

A fourth machine for the Council of European Nuclear Research recently completed its performance tests and was installed at the Council's headquarters in Geneva before the September Exhibition.

Altogether seven Mercury Computers will be used in the Nuclear Field. The major part of the computing work on Atomic Physics in Europe during the next few years will be done on these machines. A system has been set up for exchanging information among all users so that each user benefits by the accumulated experience of all the others.

An autocode has also been written for the machine which simplifies the preparation of problems and shortens the total time necessary to solve them. This makes it possible for Nuclear engineers to carry out their own calculations on it. These are essentially smaller than those met with by the Nuclear Physicists and more akin to those encountered in general engineering.

Mercury was introduced in August 1957, and can solve problems up to fifty times faster than any computer made in Western Europe. For three years Ferranti employed the largest team of Electronic Computer Research Personnel in the United Kingdom developing the machine. In the U.S.A. the Ferranti Electric, Inc., 30 Rockefeller Plaza, New York 25, New York, represents Ferranti, Ltd.

HIGH SPEED PRINTER - POWERS-SAMAS ACCOUNTING MACHINES, LTD. -
LONDON, ENGLAND

The Samastronic Output Printer, for use with Electronic Computers, Magnetic Tape Control Units, and such like devices, employs a unique method of printing. Each individual character is formed by traversing a single stylus some 15 times across the width of one character above the printing paper. As the paper moves forward at a uniform speed, 140 styluses are continuously oscillated thus each stylus produces a scanning effect in much the same manner as the spot on a television screen scans the picture area.

The actual print is produced by pulsing the styluses on to an inked ribbon or carbon paper at appropriate times during the scanning cycle. The dots caused by pulsing the styluses can be produced at any point on the scan to form solid, distinct printed characters.

The machine has a total printing capacity of up to 42,000 characters a minute. This is achieved by mounting the 140 styluses, side by side in a single oscillating bar, thus enabling up to 140 characters to be printed in one line at a speed of 5 lines per second. Printing can be accommodated on most existing forms, eliminating the need for designing special stationery in many instances.

Fifty different pulse trains contained on a Character Disc Assembly in the Printer provide a repertoire of 50 characters. Printing format is determined by interchangeable connection units. Different formats may be selected by control signals for each line of print.

Two stationery feeding carriages are provided permitting two webs of continuous marginally-punched forms to be fed independently. Wide flexibility in stationery feeding programs is provided by automatically-compensated long-feeding facilities which are built into the machine.

A model has been displayed by Ferranti Electric, Inc., 95 Madison Ave., Hempstead, N. Y.

COMPONENTS

AUTOMATIC MULTIPLE PROGRAMMER - BUREAU OF THE CENSUS - WASHINGTON, D. C.

The Maintenance and Development Branch, Machine Tabulation Division, Bureau of the Census, has developed and is experimenting with an Automatic Multiple Programmer attached to an IBM 027 Key punch Machine. This device permits the punching of six different card forms and changes the card form automatically on ejection of a card by the punch machine. A counter is provided which will accumulate a tally of the number of cards punched, and punch the total into the last card of the record automatically.

The console of the Programmer provides for manual overriding of the automatic advance feature to allow selection and repetition of any program. The card count is displayed on the console at all times, and there are indicator lights showing which program is in use at any time.

Programs are stored in printed circuit boards. Each program requires two circuit boards. The process on which the Programmer is being tested requires six programs. This number can easily be expanded. The device can also be connected to the standard Type 024 or 026 Key punch machines.

The key punching of a complete record at one time has many advantages. The problem of work flow and accompanying controls is reduced drastically. More of the data common to all cards for a record can be automatically duplicated. The cards produced from the record are together at the time of their creation, thus eliminating merging operations on more expensive punch card equipment.

Optimum use of punch cards as an initial recording media makes mandatory the use of variable length fields. Therefore different card formats are required for different portions of the record. The Automatic Multiple Programmer provides the facility to punch six different formats consecutively and makes possible the punching of a complete record at one time by one operator.

In the past the processing, by an electronic computer, of multiple card records, where the number of cards varies, has been complicated by the inability to determine completeness of the data. There was no positive assurance that all cards for the record had been recorded consecutively on magnetic tape. Yet the capabilities of a computer can be employed to a much greater extent if a complete record is processed as a unit. The automatic recording, of the number of cards punched for a record, in the last card of the record, provides a control medium for determination of its completeness when processing on a computer. In fact, with this attachment, punch cards can now assume some of the advantages of paper tape in the continuous recording of related data.

METALLIC TAPE CLEANER - DIGITRONICS CORP. - ALBERTSON, N.Y.

The Dykor Metallic Tape Cleaner has been designed to solve the problem of dirt and grime accumulation on metallic tape. Presence of foreign matter results in reading gaps as well as excessive machine wear. The operation of the cleaner is semi-automatic and results in completely cleaning and relubricating an entire reel of tape in a matter of minutes. At the completion of the process, the tape is rewound and ready for immediate use. No data is destroyed.

The Dykor Cleaner is a compact portable floor model mounted on casters. It is 21" x 18" and approximately desk height. Construction is rugged and designed for continuous use. This completely self-contained unit could add years to the life of both the metallic tape and the tape handler.

ALWAC UNIVERSAL TESTER - EL-TRONICS, INC. - HAWTHORNE, CALIFORNIA

To further increase the high reliability of the ALWAC III-E Electronic Data Processing System (national average: above 90% uptime), the ALWAC Computer Division has announced a new plug-in unit tester. It is designed to be universal in scope and will accommodate all possible circuit configurations currently employed or proposed for the ALWAC Computer System. The heart of the unit is a printed circuit grid card which permits 32^{33} combinations. The mode variation increases the number of combinations by 2^5 , load combinations by a factor of 2^4 , and power supply connections by 2^7 . Other parameters such as signal rise-fall-time extensions, special tests, power supply ranges, and test signal levels increase the number of combinations almost infinitely.

A grid card is required for each circuit type to be tested and this card, when inserted, will determine the mode of test. A major advantage of the Universal Tester is the simplicity of operation. Instructions as to the set-up for only six manually operated switches are made available on each grid card.

It is anticipated that the Tester will enable more efficient computer operations considering the decrease in training costs of maintenance personnel, as well as a decrease in time for maintenance sessions.

HIGH SPEED TAPEREADER - ELECTRODATA DIV. - PASADENA, CALIF.

A perforated paper tape reader which operates at 1,000 characters/second has been announced by the Burroughs Corporation's ElectroData Division. The photoreader will stop on a single stop-character in a little more than a microsecond and will read the next character within five milliseconds of re-initiation of the read operation.

Although the unit is designed for use with their 220 electronic data processing system, it may be adapted to any equipment. Delivery is currently quoted as four months.

Some features are: Automatic rewind and end-of-tape sensing. Rapid, simple "straight-line" tape loading. Automatic reel braking and servo shutoff system to prevent tape damage and consequent loss of data in the event of power failure, tape breakage, or other malfunction.

NEURON COUNTER - DATA INSTRUMENTS DIV., TELECOMPUTING CORP. - NORTH HOLLYWOOD, CALIFORNIA

Telecomputing's Data Instruments Division has a new bi-directional counter which is a rapid-follow function digital indicator. Known as the NEURON counter it can be used to indicate the position of almost any discrete variable such as valve opening, shaft position, angle of magnetic tape position. It can also be used to store in-out information which is necessary for inventory control bi-directional flow, liquid quantity and flow indication, or batch tabulation. Special units, for example, digital clocks are available.

The standard counting rate of the counter is 0 to 40 counts per second. Separate add and subtract motors allow random input pulses. Reset can be manual by a single-stroke push bar or electrical by a remote switch pulse. The unique drive prevents double-indexing arising from shock vibration and over-voltage. The digital readout to five decades can be both electrical and visual.

The electrical readout feature consists of an etched 10-point switch and circuit combination which makes each point on the switch externally available. A 10-point epoxy-glass etched switch deck is mounted adjacent to each counter wheel and projects through the bottom of the counter case for electrical connection. An insulated rotor attaches to each counter wheel position. Each rotor connection is brought out through a slip ring on its mating switch deck. The life of a counter is in excess of 300 million counts.

CORE STORAGE - TELEMETER MAGNETICS, INC. -
LOS ANGELES, CALIF.

Telemeter Magnetics new magnetic core storage buffer, type 1092-BQ8A, operates at 100-kc rate and stores up to 1092 eight-bit characters. The prime application area for this unit is in synchronizing two digital data systems which operate at different speeds. For example: communication between a tape unit and a telemetering system; between an analog-to-digital converter and a computer tape unit; or between two units of different design. The buffer is also a necessary element in systems for converting from one format to another as from IBM magnetic tape code to UNIVAC code. The unit is available from stock. Functional features include:

The buffer is supplied as an integral unit in a standard 19 inch relay rack. All connections are made by means of plug connectors. Adequate cooling is provided by ambient air.

A conveniently located "manual clear" control clears information stored in the buffer unit and resets it to an initial fixed address. Connections are incorporated for easy installation of a remote clear push-button or switch. The complete clear and reset operation is executed in approximately 50 milliseconds.

Interlaced load and unload permits any random pattern of load and unload signals at rates up to 100,000 signals per second.

The buffer incorporates signal generating circuits for checking the operation independent of external equipment. In addition, manual controls permit marginal operation to locate weak or intermittent signals.

SPEEDREADER 2000 - UPTIME CORP. - RAWLINGS, WYOMING

The prototype model of the SPEEDREADER 2000 punch card input system has been in full operation at the factory for more than six months, following an extensive period of thorough testing.

The unit handles and senses cards reliably at a rate of 2000 cards per minute. The prototype reads 80-column cards; production models will be available to read 80- or 90-column cards.

Card sensing and timing is done photoelectronically. No mechanical elements are used in timing. A card is sensed row by row at an 80- or 90-column sensing station by 80 or 90 photodiodes. Row read-time is established by the leading edge of the card striking each of 12 photodiodes mounted vertically in the center of the card path.

Card-sensing registration is completely reliable, and the angular deviation from the horizontal encountered during card travel does not cause reading of an adjacent column rather than the correct one.

With this new equipment, high-speed data processing systems can use card data at speeds more nearly compatible with that of the central computer. The reading rate can increase the capabilities of conventional tabulating installations, and the operation of card-to-magnetic-tape conversion units can be speeded up.

The 2000 is available with or without electronic circuitry (vacuum-tube or transistorized) for large-scale or medium-sized data processing systems or for electro-mechanical accounting systems.

MISCELLANEOUS

INTERDISCIPLINARY CONFERENCE ON SELF-ORGANIZING SYSTEMS - CHICAGO, ILLINOIS

An Interdisciplinary Conference on Self-Organizing Systems will be held on May 5 and 6, 1959, in Chicago, Illinois. The conference is being sponsored by the Office of Naval Research, Information Systems Branch, with the assistance of the Armour Research Foundation of the Illinois Institute of Technology. The major function of this conference is to bring together research workers in the fields of the Biological, Mathematical, Physical, Psychological, and Social Sciences who have actively considered the development and growth of Systems capable of spontaneous classification of their environments. Emphasis will be placed primarily on non-biological mechanisms which exhibit characteristics of organization and growth, of thought and learning, of information and communication—those characteristics which are normally attributed to intelligent organisms.

Interested individuals may obtain further information and a preliminary program, when available, by writing to Mr. Scott Cameron, ICSOS Conference Secretary, Armour Research Foundation, 10 West 35th Street, Chicago, Illinois.

CONTRIBUTIONS FOR DIGITAL COMPUTER NEWSLETTER

The Office of Naval Research welcomes contributions to the NEWSLETTER. Your contributions will assist in improving the contents of this newsletter, and in making it an even better medium of exchange of information, between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to this Office for future issues. Because of limited time and personnel, it is often impossible for the editor to acknowledge individually all material which has been sent to this Office for publication.

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Communications should be addressed to:

GORDON D. GOLDSTEIN, Editor
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