L2 2.2μH
Y1 16MHZ
C1 68pf
7404 U1
R2 390
C2 150pf
16MHZ
+5V
LS163 U15
16 MHZ
1MHZ
2MHZ
4 MHZ
8 MHZ
+12V
R1 4.7K
Q1 2N3904
7404 U1
+5V
3 - WAIT
NC
NC
+5V
BUSRQ
6,7,8 - INT
NMI
6 - RESET
Z80A U2
4MHZ
TIMER ENA
RD
WR
A1
AØ
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA Ø
8253 U6
BAUD2
BAUD 1
BAUD Ø
READ
WRITE
LS132 U73
STB
IORQ
MI
LSØ2 U91
INTA
A6
A5
A4
LS138 U17
SIO ENA
DART ENA
TIMER ENA
LPORTS ENA
IO 3Ø
IO 2Ø
IO 1Ø
IO ØØ
A7
A1
AØ
LS138 U84
STB
IO
LPORTS ENBL
SR ENA
CLRINT
CEN STAT
DRV STAT
CEN DATA
BANK STB
DRV STB
M1
IORQ
RD
WR
RFSH
A15
A14
A13
A12
A11
AIØ
A9
A8
A7
A6
A5
A4
READ
IORQ
LS32 U99
LS244 U5
LS04 U72
RD
WR
WRITE
RFSH
INTA
7-EOQ
LSØØ U102
+5V
LS244 U100
2-CINT
2- AUTO ENA
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA Ø
4-MATCH
LS74 U101
CLRINT
A3
A2
A1
AØ
LS244 U18
G2
DO 7
DO 6
DO 5
DO 4
DO 3
DO 2
DO 1
DO Ø
LS244 U3
3 - AUTO
A12
JP1
10K R
LS151 U104
+5
HIGH -3
A13
A14
A15
M1
IORQ
LSØ2 U91
LSØ4 U72
IO
A3
A2
LS139 U54
CTL STB
MODE STB
SYNC ENA

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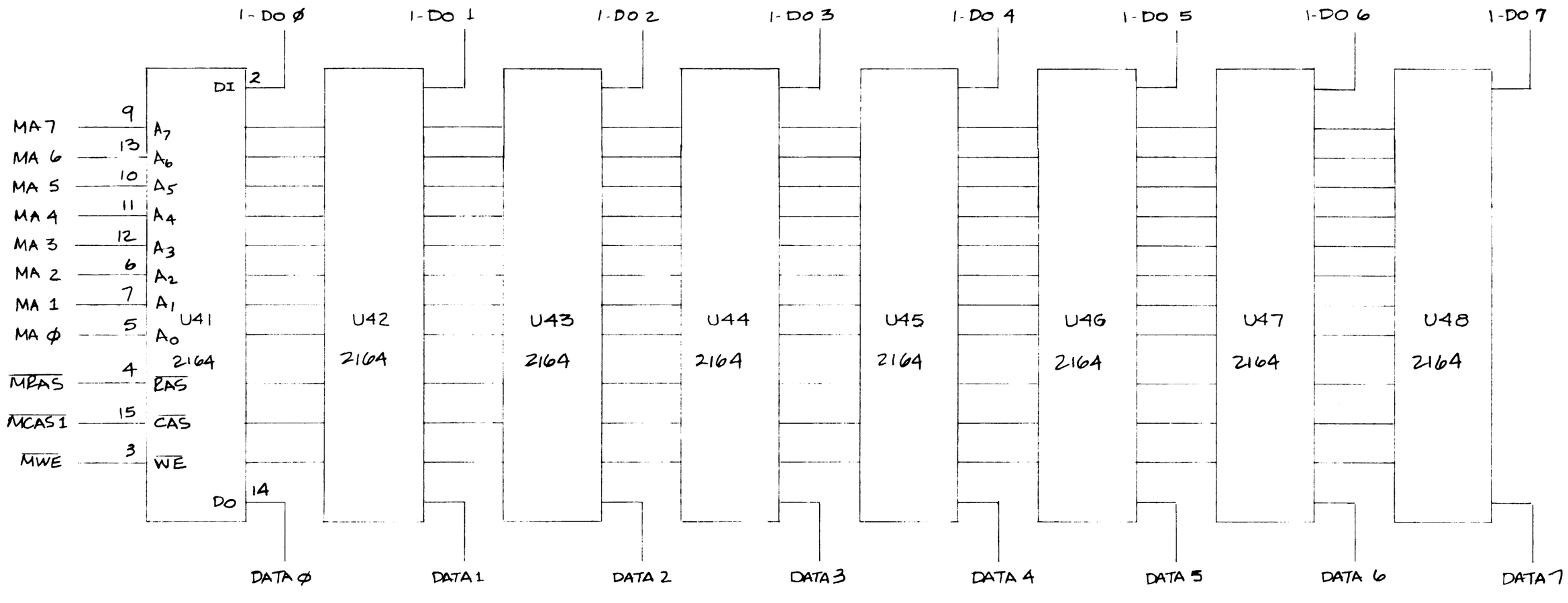
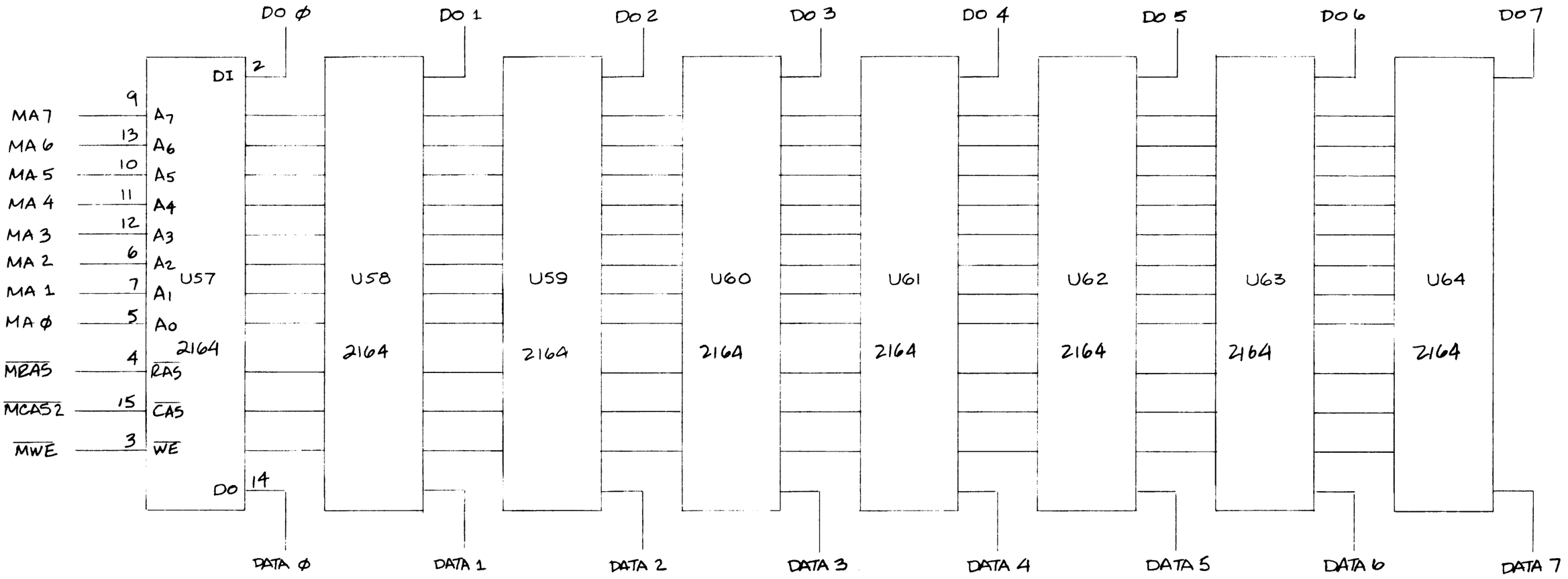
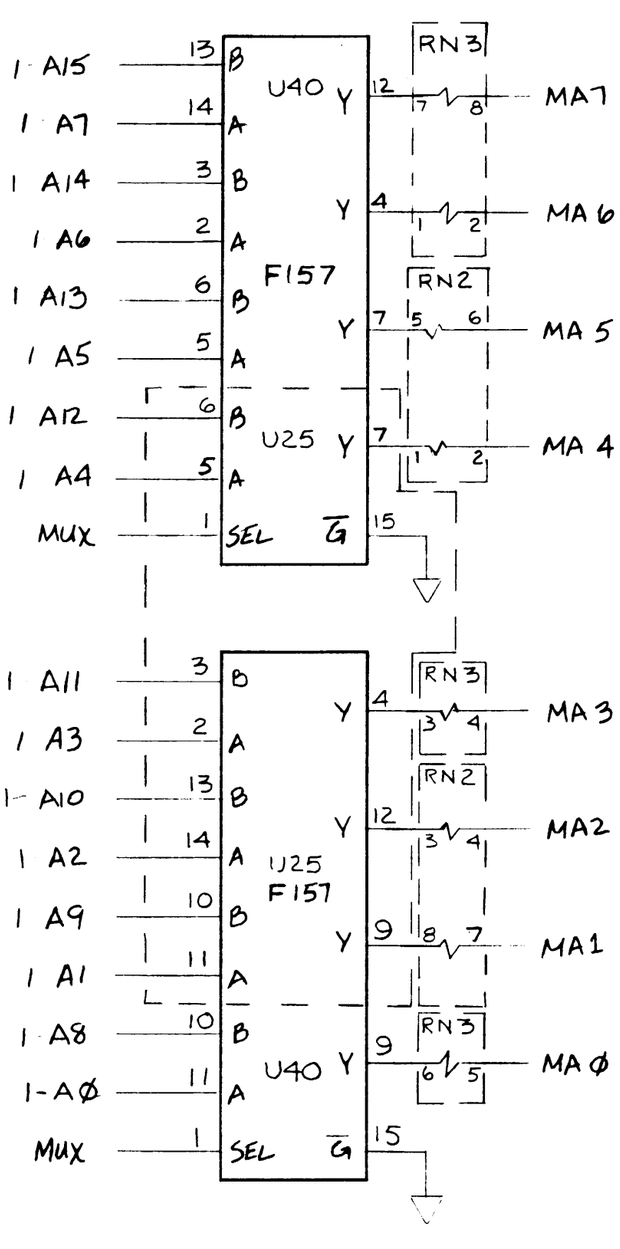
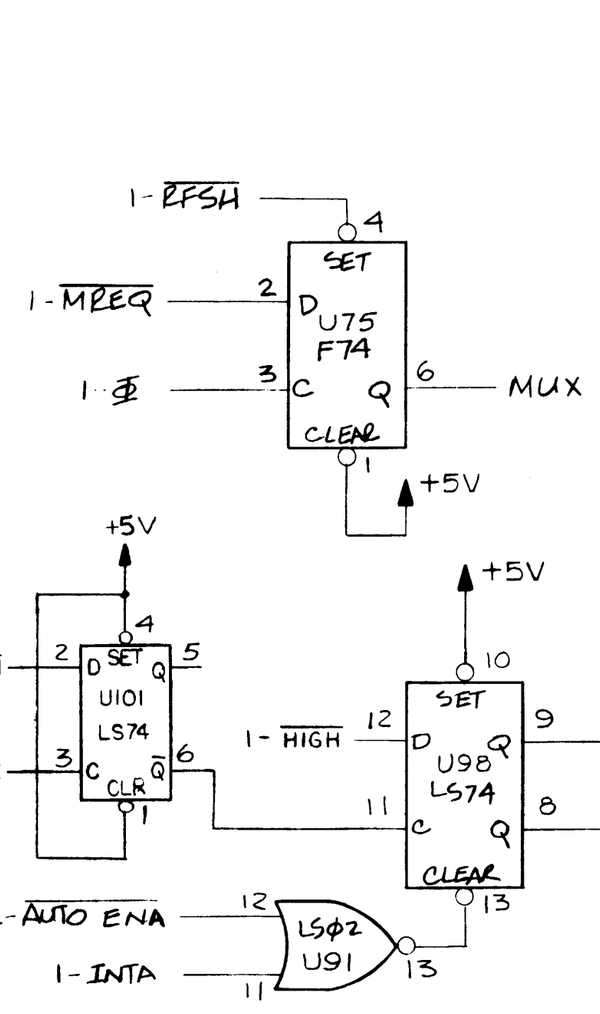
CPU, TIMER, & IO DECODING LOGIC ©1983

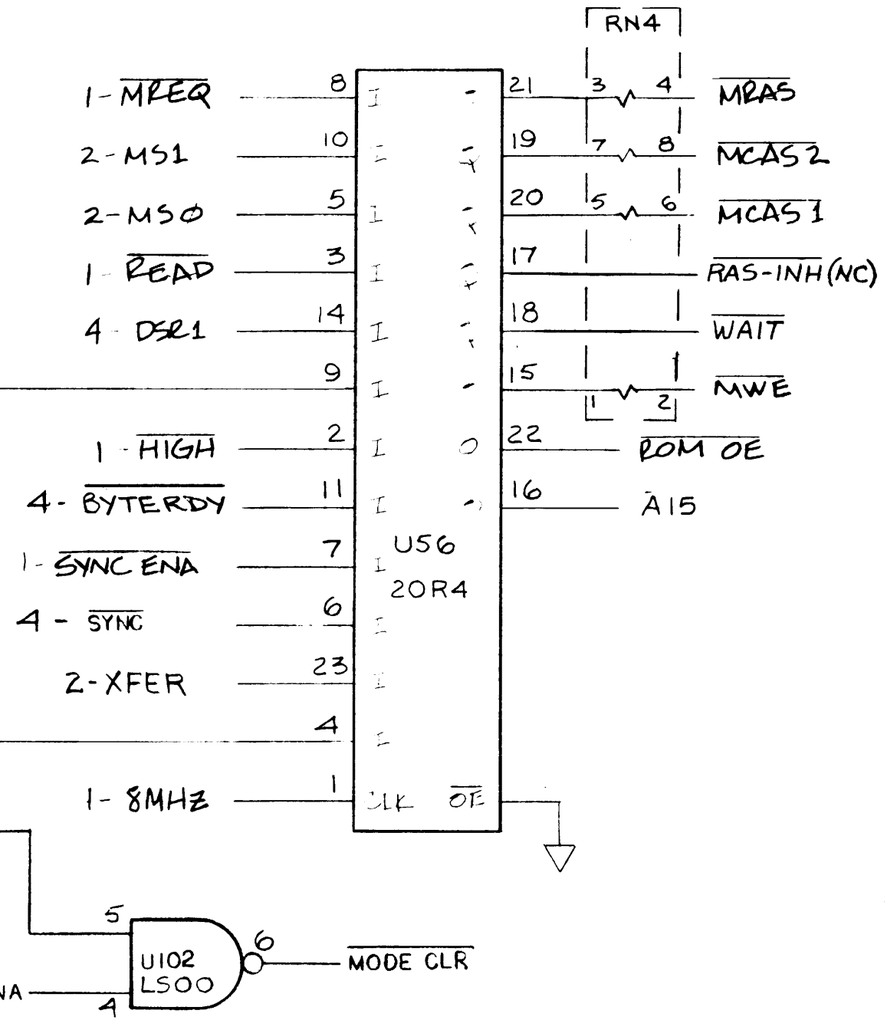
4-LATE
4-EARLY
LS132 U73
WACTV
+5V
DELAY U95
2D
3D
1D
LS153 U96
4-LATE
4-EARLY
FWDATA
HWDATA
+5V
SET
U98 LS74
4-CELL CLK
CLEAR
WACTV
4MHz
U97 LS175
CLEAR
3D
2D
1D
J4
+5V
R44 1K
R49 330Ω
J4
C FAULT
27
6-MTR
1-CEN STAT
U5 LS244
DATA 3
DATA 2
DATA 1
DATA Ø
+5V
R48 330Ω
READY
22
U107
+5V
U108 LS74
U109 LSØ8
CINT
1-CENSTAT
AUTO ENA
U22 LSØ4
AUTO ENA
MTR ON
U22 LSØ4
MTR ON
STROBE
U22 LSØ2
STROBE
1-DO7
1-DO6
1-DO5
1-DO4
1-DO3
1-DO2
1-DO1
1-DOØ
1-BANK STB
6 RESET
U21 LS273
CINTENB
XFER
MTR ON
AUTO ENA
STROBE
RSTOR
MS1
MSØ
CLEAR
1-DO7
1-DO6
1-DO5
1-DO4
1-DO3
1-DO2
1-DO1
1-DOØ
1-CEN DATA
U4 LS374
J4
RSTOR
U5 LS244
RESTORE
STROBE
U5 LS244
PSTB
EVEN 2-24 ⅁ PIN 34
PINS ARE GROUNDED
RN1 1K
+5V
1-A12
1-A11
1-A10
1-A9
3-AUTO
LS244 U18
A12
A11
A13
A9
U29
2764
2732
2716
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA Ø
4-OP1
1-A8
4-OPØ
1-A7
1-A10
1-A6
1-A11
1-A5
3-AUTO
U34 LS157
CA8
CA7
CA6
CA5
1-A4
1-A3
1-A2
1-A1
4-LADDR
1-MREQ
3-ROM OE
+5V
MD 11 REV 2
PAGE 2 OF 8
DISK WRITE LOGIC ⅁ ROM LOGIC





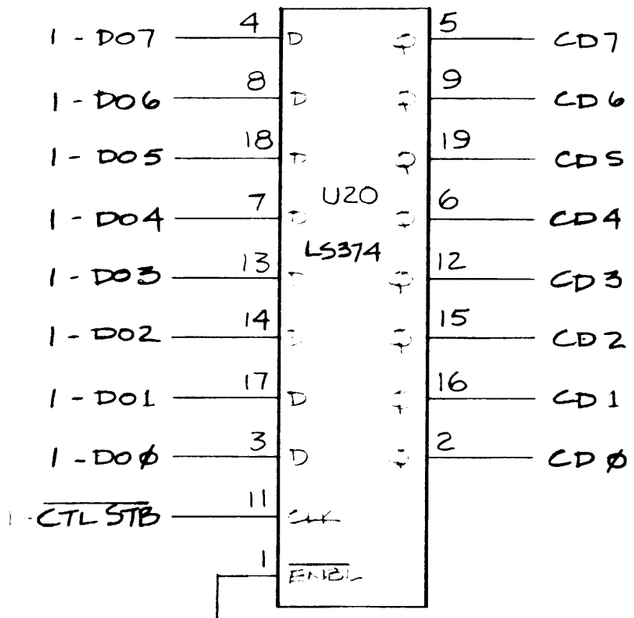


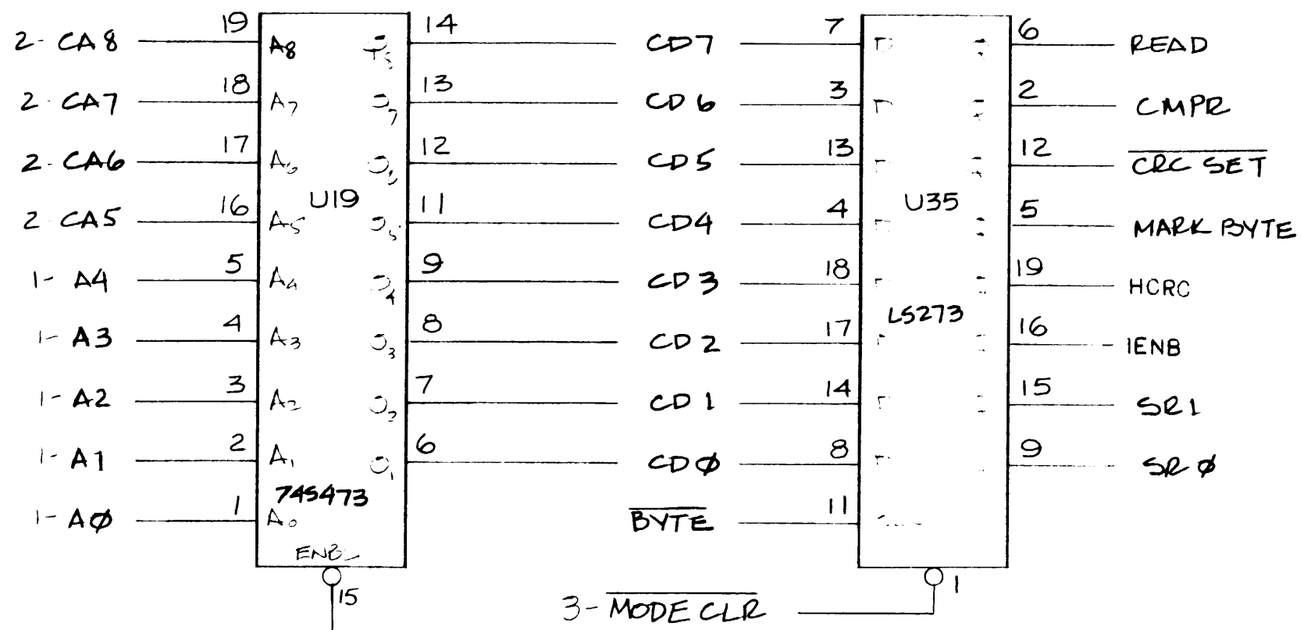


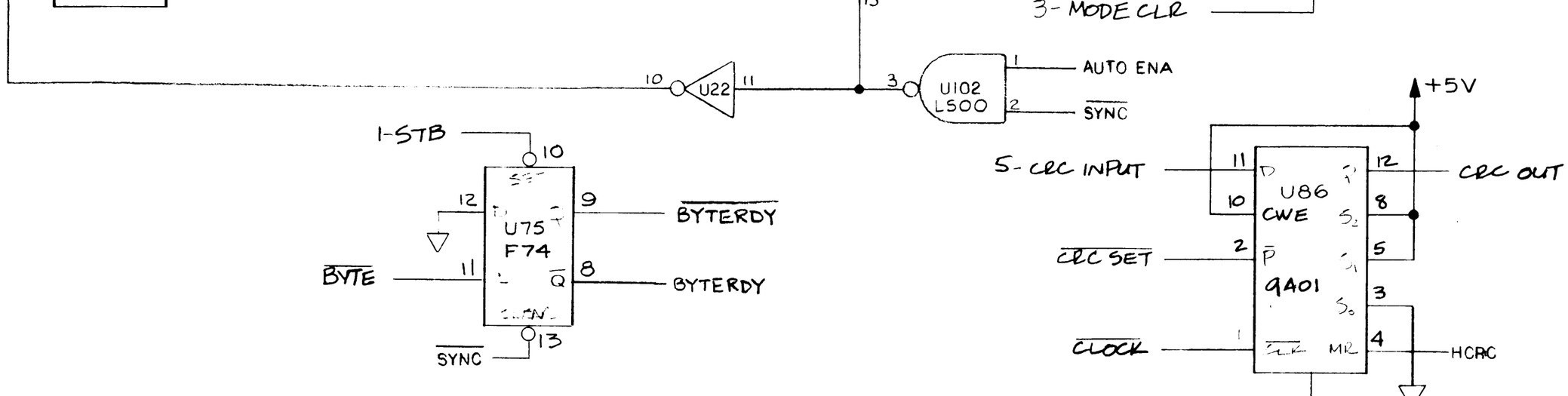


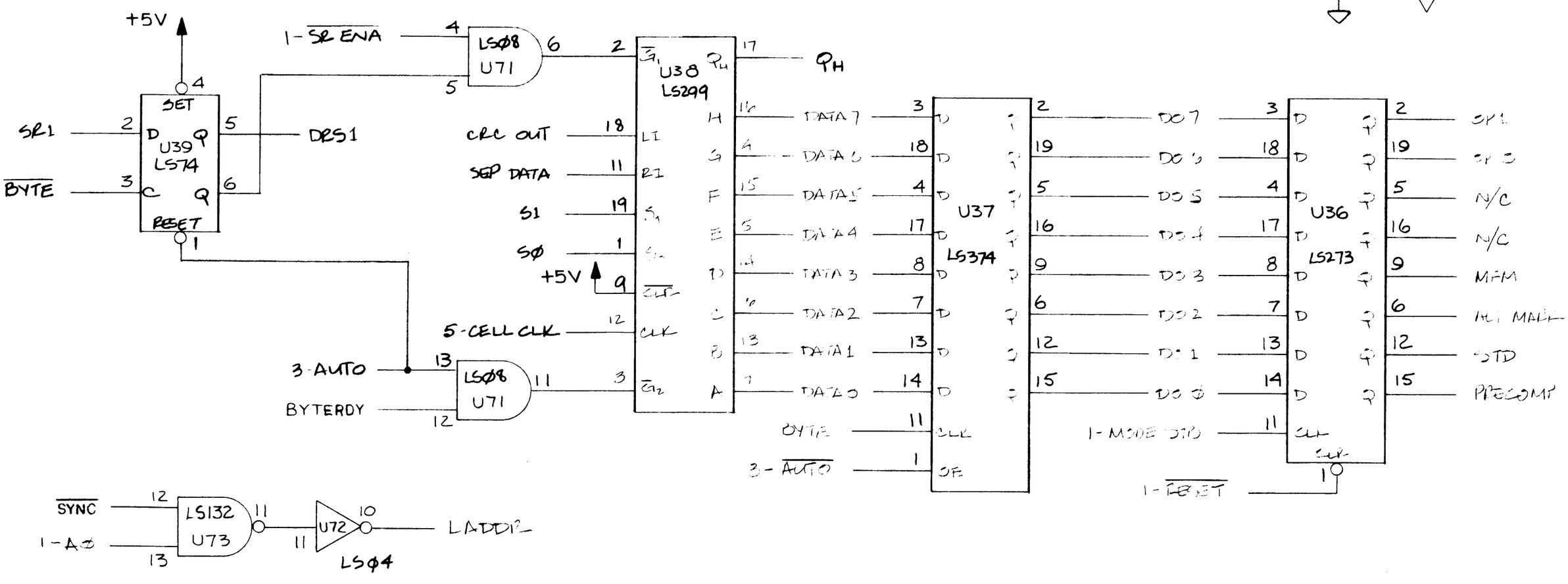
MD 11 REV 2

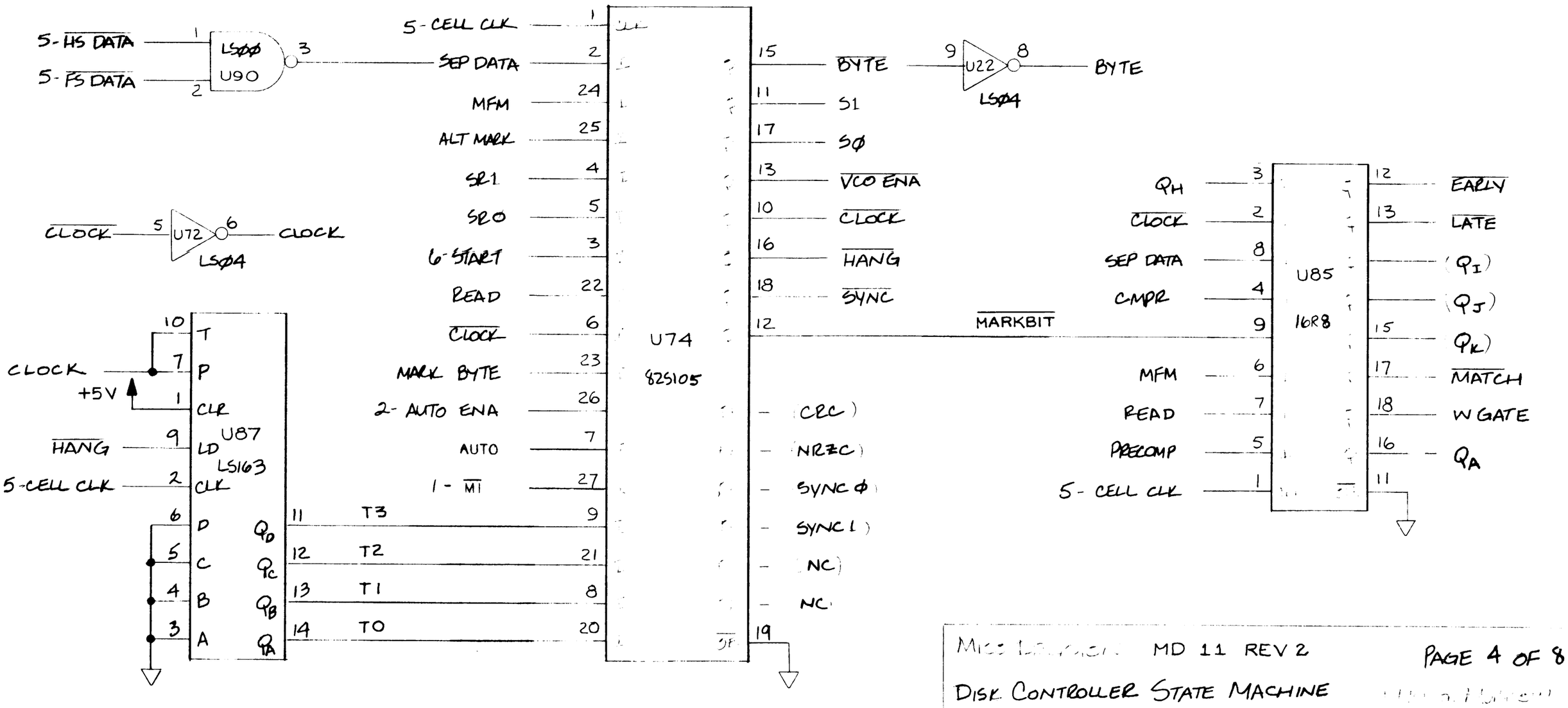
MEMORY ARRAY & LOGIC











MD 11 REV 2

DISK CONTROLLER STATE MACHINE

TRAN
FDAT
LS279 U89
FVCO
U76 LS04
TRAN
FVCO
LS279 U89
TRANEX
+5V
"A" Q LS74 U79
FVCO
FTENB
FS DATA
C24 112pf
DLY Ø
LS175 U88
DLY 1
DLY 2
DL CLK
CLK
RESET
DLY Ø
DLY 1
DLY2
TRAN
TRAN
+5V
+5V
"B" U81 LS74
TRAN
FVCO
"A" Q LS74 U81
FVCO
+5V
R27 511Ω 1%
CR4
CR3
R26 1K 1%
CR2
U90 LS00
C21 .05μ
C20 .001μ
R25 270Ω
R32 33K
R31 330K
C22 .1μF
U82 "A"
R30 2.2K
R24 3.3K
C23 .1μF
R29 3.3K
R28 3.3K
+5V
+5V
+5V
ENA
U83
FRQ
Y
LS629
VV
VG
RNG
FPVCO
+5V
15
1
C29 25pf
VCO DATA
"B" U80 74F74
LLEAR
HVCO
"B" U93 74F74
LLEAR
+5V
+5V
+5V
R39 3.3K
R40 3.3K
R36 3.3K
U82 "B"
C27 .1μF
R41 2.2K
R43 3.3K
C30 .1μF
RNG
FRQ
ENA
U94 74S124
Y
VV
VG
LHVCO
+5V
15
9
JAM
R38 33K
3.3K
Q5
CR5
R37 330
C28 330pf
R34 330 1%
R33 330 1%
CR6
R35 3.3K
C26 .0068μ
C25 150 pf
R42 680
+5V
+5V
+5V
"A" U80 74F74
"A" U93 74F74
"A" U77 74F74
"A" U78 LS74
"B" U78 LS74
VCO DATA
4-VCOENA
VCO DATA
VCO DATA
JAM X
JAM Y
U92 50ns DELAY
LS00 U90
R22 220
R23 220
HVCO
U76 LS04
HVCO
HS DATA
6-DS1
L3 3.3μH
Y2
10MHz
C19 150pf
C18 150pf
R20 390
LS04 U76
HD XTAL
U31 LS393
HALF XTAL
+5V
U39 LS74
1MV
1-8 MHZ
1-4 MHZ
1-2 MHZ
U30
4-STD
4-MFM
1MF
.5MF
.25MF
LS153
DLC
FPVCO
VCO
FDIV
U31 LS393
1MF
.5MF
.25MF
HD XTAL
VCO
HVCO
FVCO
HALF XTAL
6-HRDATA
6-DS1
U32 LS157
4-Q_H
Q_A
U33 LS157
CELL CLK
CRC INPUT
VCO DATA
JAM
4-VCOENA
6-DS1
U91
FTENB
FPVCO
1-2MHZ
DLC
1-8MHZ
VCO
1MV
6-FRDATA
1-1MHZ
U105 LS157
FDIV
DLCLK
FVCO
FDAT

MICRO DECISION MD 11 REV 2 PAGE 5 OF 8

DATA SEPARATION LOGIC

7437 OR 7406 & 7407 TYP

J1

SEL Ø — U49 — DRIVE 1
SEL 1 — U49 — DRIVE 2
MTR — U50 — MOTOR ON
DIR — U50 — DIRECTION
STEP — U67 — STEP
HDØ — U67 — SIDE SELECT
2-FWDATA — U67 — WRITE DATA
4-WGATE, LOWVCC — 7437 U68 — WRITE GATE

7437 OR 7406 & 7407 TYP

SEL 2 — U49 — DRIVE Ø
SEL 3 — U49 — DRIVE 1
STEP — U50 — STEP
DIR — U50 — DIRECTION
HDØ — U50 — HEAD Ø
HD 1 — U50 — HEAD 1
HD 2 — U67 — HEAD 2
LOW CURRENT — U67 — LOW CURRENT
4-WGATE, LOWVCC — 7437 U68 — WRITE GATE

+5V
R12 330
C15 33
555 U70
C16 .1µF
9 U49 8 — 7407
2-MTR ON
3 U107 4 — MTR
RESET

+5V
R17 510Ω
LOWVCC — LS132 U73 — 7406 U67 — RESET
R15 4.7K
R18 4.7K
VR1
R16 4.7K
R11 150
Q2
Q3
J10
R19 47K
C17 33µF
CR7

J1
R10 150
RN5 150
WRITE PROT 28 — WPROT
TRACK Ø 26 — FTRK Ø
INDEX 8 — FINDEX
R21 150
READ DATA 30 — FRDATA

J2
TRACK Ø 10 — HTRK Ø
SEEK CMPL 8 — SEEK COMPLETE
READY 22 — DRV RDY
INDEX 20 — HINDEX
FAULT 12 — FAULT

MATCH
4-IENB
"B" Q U79 LS74
1-CLRINT
2-CINT
U106 LS32
U107
R5 4.7KΩ
7407 U49
INT

LS20 U103
MTR
4-MATCH

FINDEX, HINDEX — LSØ8 U71
FTRKØ, HTRKØ — LSØ8 U71
JP5
4 - CRC SET
WPROT
FAULT
SEEK COMPLETE
DRVRDY
R47 1K
U53 LS240
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA Ø

1-DRV STAT
R8 4.7K
C13 100pf
HRDATA
U51 96LS02
R9 10K, 1%
C14 .001µF
U51 96LS02
LSØ2 U69
START -4

J3A
110Ω R14
9637 U65
SEL 2
LSØ2 U69
HRDATA
J3B
R13 110Ω
9637 U65
SEL 3
LSØ2 U69

PINS 2,4,6,8,12,16,20,11,19 NEED SEPARATED ON BOTH J3A AND J3B

1-DØ7
1-DØ6
1-DØ5
1-DØ4
1-DØ3
1-DØ2
1-DØ1
1-DØØ
1-DRV STB
RESET
U52 LS273
STEP
DIR
LOW CURRENT
HD2
HD 1
HDØ

DS1
MTR
U54 LS139
SEL3
SEL2
SEL 1
SEL Ø

J3A
2-HWDATA — 9638 U66
J3B
2-HWDATA — 9638 U66

ODD NUMBERED PINS ON J1 AND J2 ARE GROUNDED

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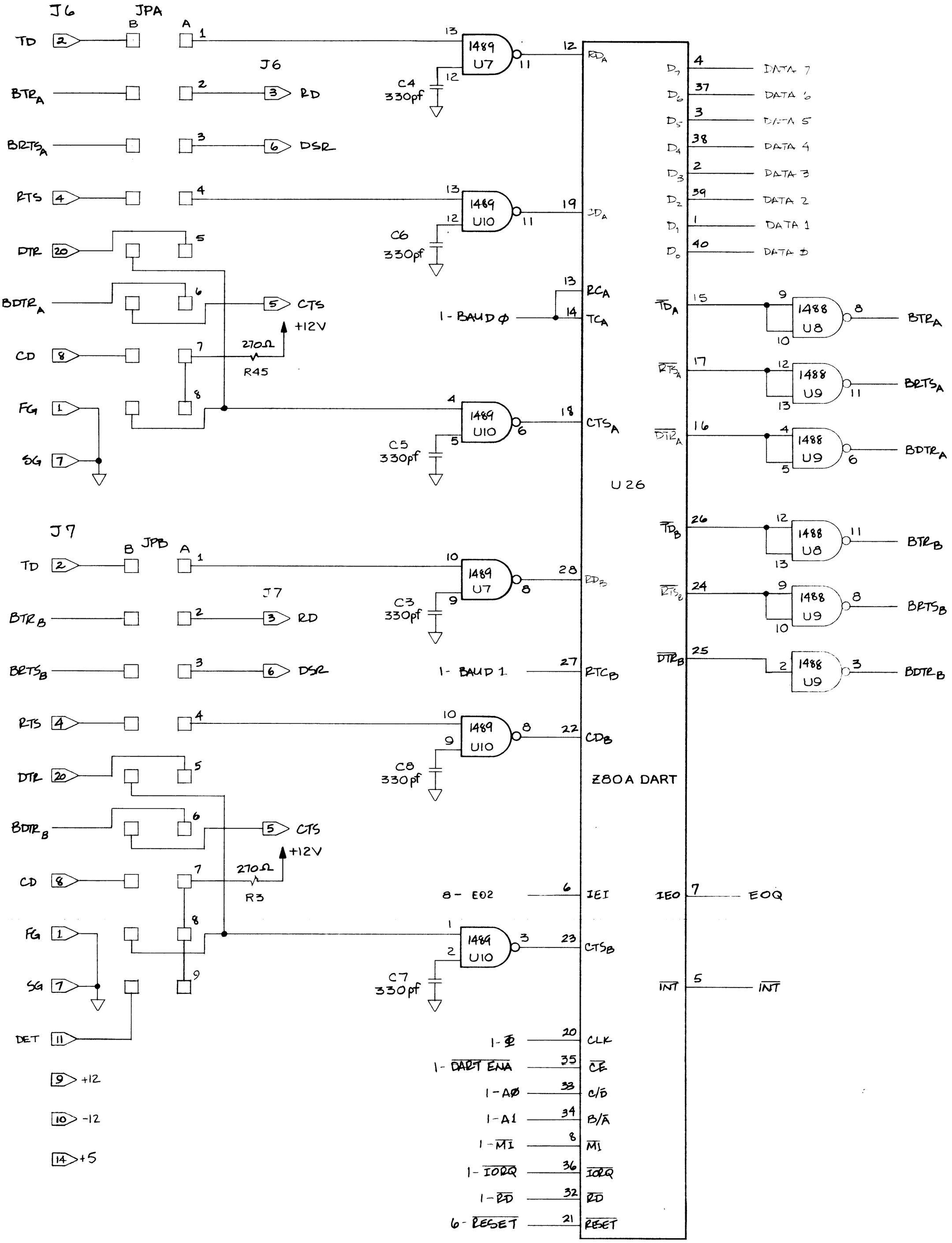
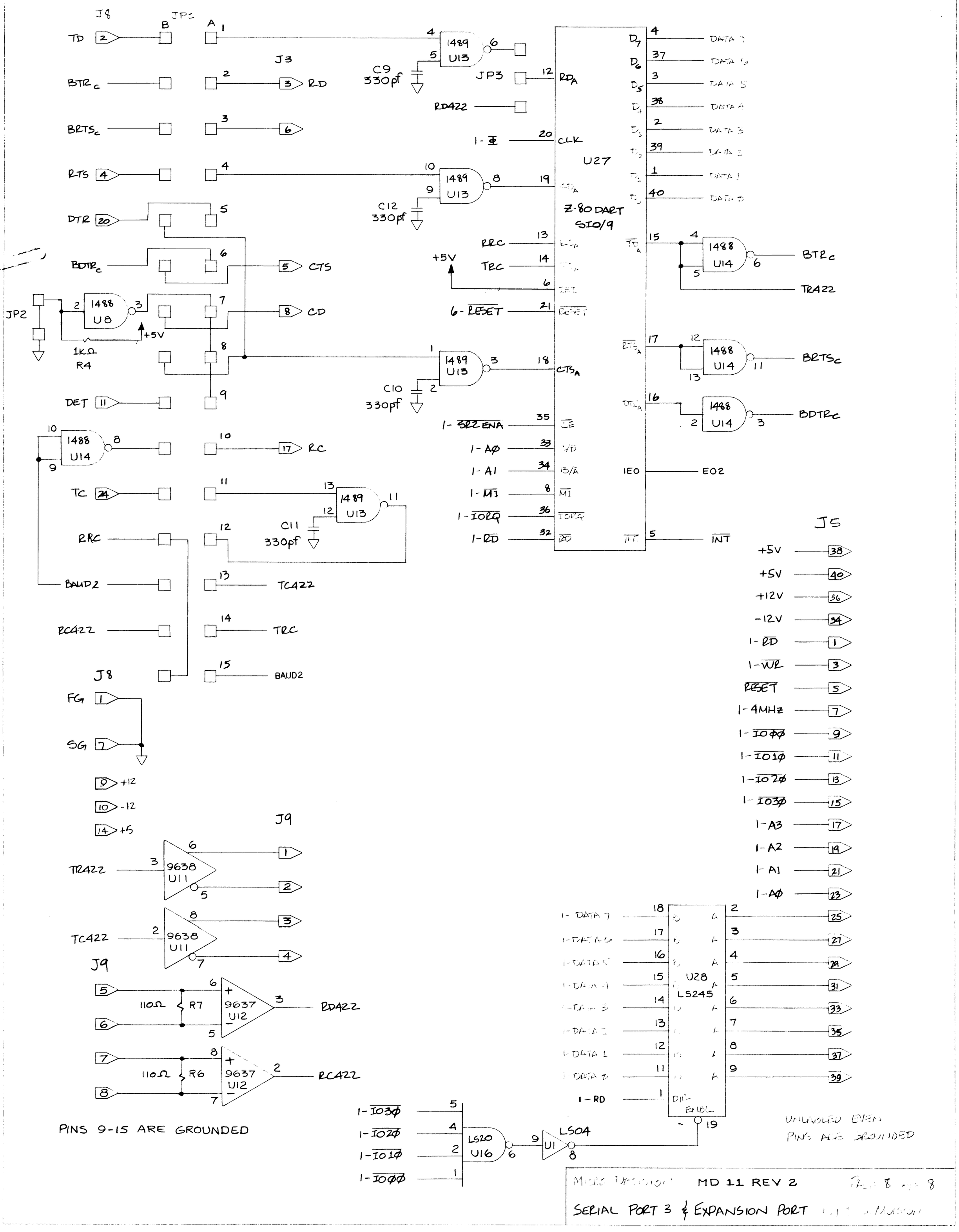
DISK INTERFACE LOGIC



SERIAL PORTS 1 & 2


J8
JP2
TD
BTR_C
BRTS_C
RTS
DTR
BDTR_C
JP2
1488 U8
+5V
1KΩ R4
DET
J3
RD
CTS
CD
1489 U13
C9 330pf
C12 330pf
C10 330pf
C11 330pf
JP3
RD422
1-Φ
RRC
TRC
+5V
6-RESET
1-SEL ENA
1-AØ
1-A1
1-M1
1-IORQ
1-RD
U27
Z-80 DART SIO/9
CLK
RD_A
CTS_A
CE
IEO
INT
D7
D6
D5
D4
D3
D2
D1
D0
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA 0
1488 U14
BTR_C
TRA22
BRTS_C
BDTR_C
J8
FG
SG
+12
-12
+5
RC
TC
RRC
BAUD2
TC422
TRC
BAUD2
J9
TRA22
TC422
9638 U11
RDA22
RCA22
110Ω R7
110Ω R6
9637 U12
J5
+5V
+5V
+12V
-12V
1-RD
1-WR
RESET
1-4MHz
1-IOØØ
1-IO1Ø
1-IO2Ø
1-IO3Ø
1-A3
1-A2
1-A1
1-AØ
1-DATA 7
1-DATA 6
1-DATA 5
1-DATA 4
1-DATA 3
1-DATA 2
1-DATA 1
1-DATA 0
U28 LS245
DIR
ENBL
LS20 U16
LS04 U1
UNUSED GATES PINS ARE GROUNDED
PINS 9-15 ARE GROUNDED
MD 11 REV 2
SERIAL PORT 3 & EXPANSION PORT