MicroSystems Inc.

Maintenance Manual

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

1.1.1 Purpose of the Manual

The purpose of this manual is to provide the user of the computer with the necessary fundamental knowledge to enable him to maintain, analyze and isolate faults, and repair the computer. The manual is a self-sufficient document in that it provides operational theory, functional and operational characteristics and procedures which stand alone. The manual will provide the user with in-depth procedures and analytical tools to maintain, troubleshoot and repair the computer.

1.1.2 Organization of Manual

The document is divided into six sections. Section 1 presents general information with respect to machine operation, physical characteristics, available options, and general expansion capability, a glossary of terms for signals used within the machine and a description showing the relationship of documentation notes to physical hardware.

Section 2, Programming and Operation, describes the commands, formats and their mnemonic codes, used in the computer.

Section 3, Theory of Operation, describes in general the operation of the machine from the block diagram viewpoint, explaining each block, its function, its inputs and outputs and its use. Details of each logic element are given. The section provides detailed theory of operation for each functional unit utilized in the machine, presenting timing diagrams, circuit analyses, command timing and flow charts, plus truth tables. This section also includes a description of the input/output facilities of the computer.

Section 4, Installation and Maintenance, is comprised of three subsections:

Checkout and Installation - provides the procedures used to prepare the computer for operation from unpackaging to test and operation and to repackage for trans shipment.

Field Maintenance - provides preventive maintenance procedures, maintenance schedules, quick fault isolation, and parts list.

Depot Maintenance - provides procedure for fault isolation within the computer using maintenance panel procedures.

Section 5 contains the expansion capabilities of the computer.

Section 6 contains the schematic diagram necessary to define the computer.

1.1.3 Introduction to the Computer

The computer is a small byte-oriented microprogrammable digital processor designed for dedicated applications. The computer establishes a hardware base upon which is formed a series of computers. It incorporates advanced features and operating characteristics resulting in a high speed, microprogrammable digital computer. It provides a medium where the user can define his own instructions, input/output and interrupt capabilities to suit his particular needs. The computer can be used to create higher level computers whose architecture and instruction sets are tailored to the users' applications.

A microprogram consists of sequences or command steps commonly referred to as "firmware." The name firmware results from the commands being placed into a Read Only Storage (ROS) consisting of a matrix of discrete diodes. The microprogram firmware can be used without a core memory as a system controller or data concentrator or with a core memory when storage of data, tables, variable parameters, etc., is required. Core memory is added as a functional module and is a prime example of the computer's high degree of flexibility and modularity. The microprogram is changed by replacing the read only storage plug-in boards. In addition, software programming can be stored in core memory and used to extend the capabilities of the firmware.

The functional modularity of the computer permits expandable core memory from 0 to 32,768 bytes (8 or 9 bits) in 4096 byte increments.

Read only storage, is constructed in modules of 256 words and can be expanded to 1,024 words. The read only storage uses discrete diodes mounted on printed circuit board as plug-in modules.

The processor is organized around an 8-bit arithmetic/logic unit which performs all arithmetic logic and shifting functions. Inputs to the arithmetic/logic unit may be from:

a. A file of registers.

b. A bus which derives its input from the output of a temporary buffer register, the input bus or an eight-bit literal contained in the command.

The processor uses eight registers and 16 file registers. Each register has a specific purpose in the processor while the file registers are used for general storage and flags.

The computer utilizes 16 basic commands and offers many unique variations of the commands. All instructions are executed in 220 nanoseconds (except for the jump and skip commands).

1.2 PHYSICAL DESCRIPTION

1.2.1 General Characteristics

Figure 1, showing an external overall view of the computer, includes the control panel (1), which contains those switches and indicators required to operate and control the computer and observe its operation. Also seen in Figure 1 is the housing (2) for the components of the machine. Figures 2 and 4 show the alternative rear view panel (1)(inside of which the power supply is mounted) (2) a cooling fan (3) the connector for the power line cord (4) terminal board (TB1) where power supply voltages may be monitored without opening the computer, (5) a toggle switch, which makes power available to the control panel power ON switch, and two fuses (F1 and F2) (6). F1 is a 10 amp fuse used in the input power circuit and F2 is a 15 amp fuse used in the +5V d.c. power circuit.

WARNING

115V power is exposed at terminal board TB1. Do not attempt removal of the power supply panel when power is on. Disconnect the line cord before handling the power supply assembly.

The power supply configurations for the two rear panel alternatives of Figures 2 and 4 are shown in Figures 3 and 5 respectively.

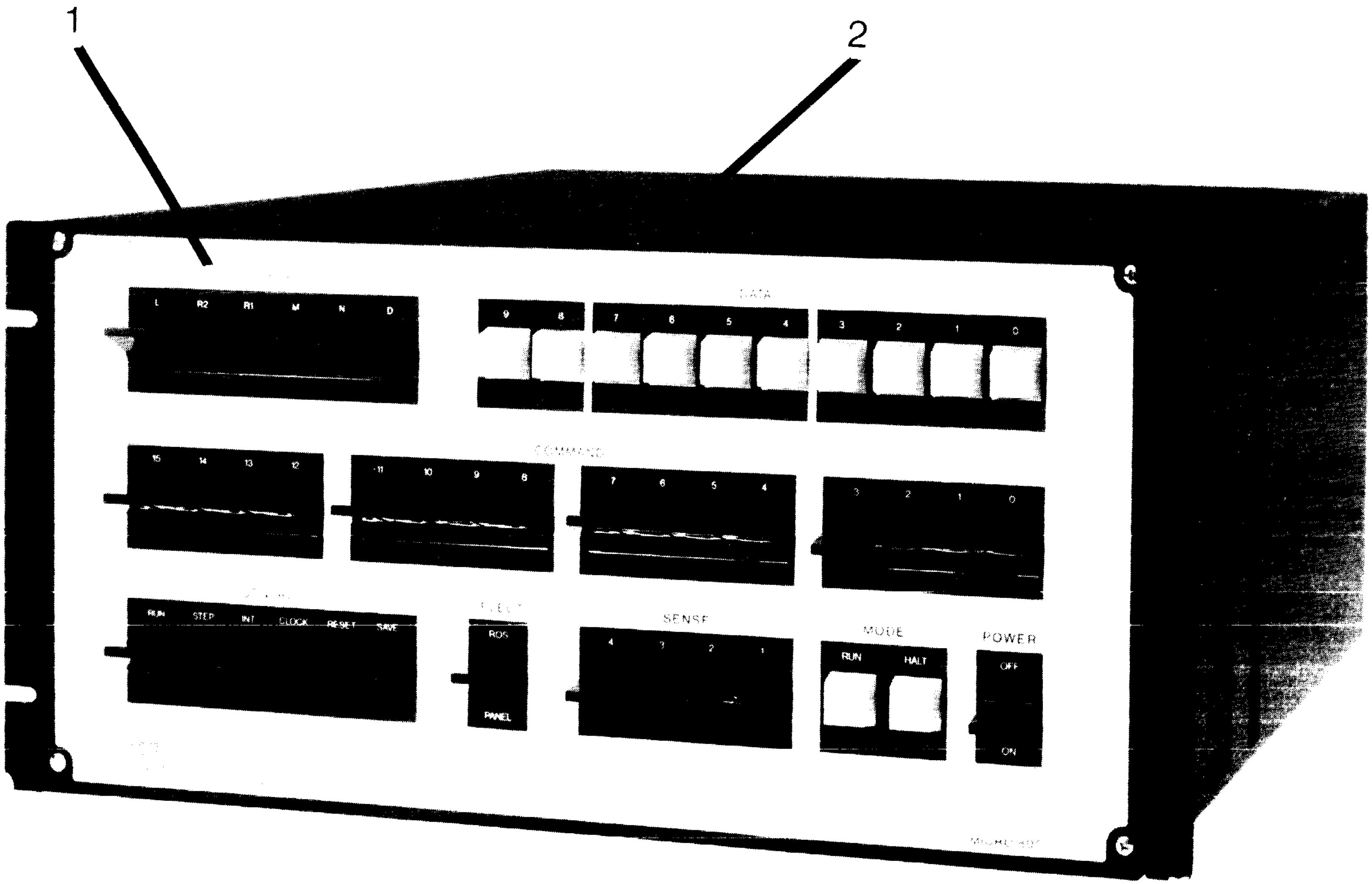

1
2
L R2 R1 M N D
RUN STEP INT CLOCK RESET SAVE
ROS
PANEL
SENSE
MODE
RUN HALT
POWER
OFF
ON

FIG 1

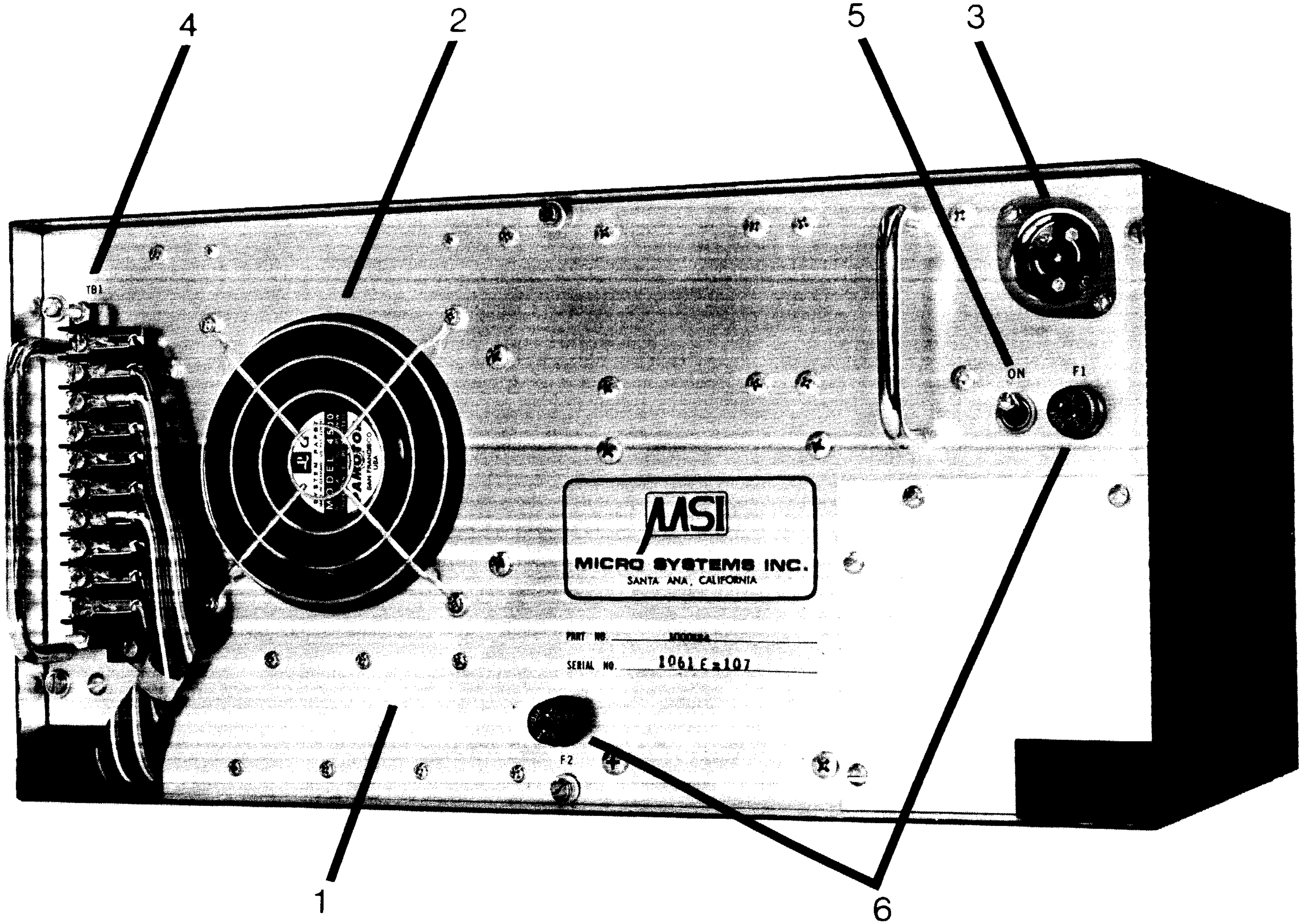

4
2
5
3
TB1
ON
F1
MSI
MICRO SYSTEMS INC.
SANTA ANA, CALIFORNIA
PART NO.
SERIAL NO.
F2
1
6

FIG 2

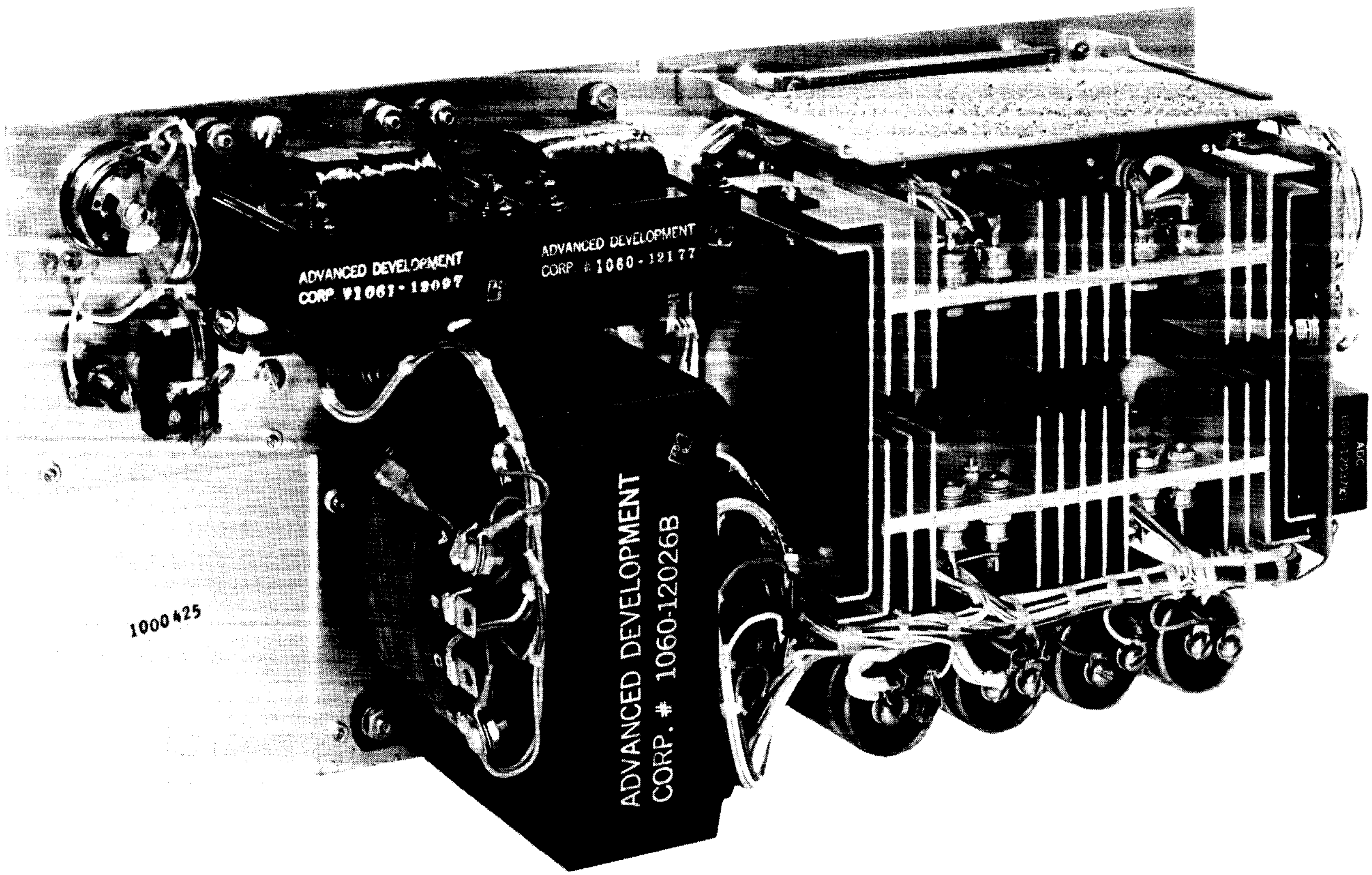

ADVANCED DEVELOPMENT
CORP #1061-12097
ADVANCED DEVELOPMENT
CORP #1060-12177
ADVANCED DEVELOPMENT
CORP. # 1060-12026B
1000425
2

FIG 3

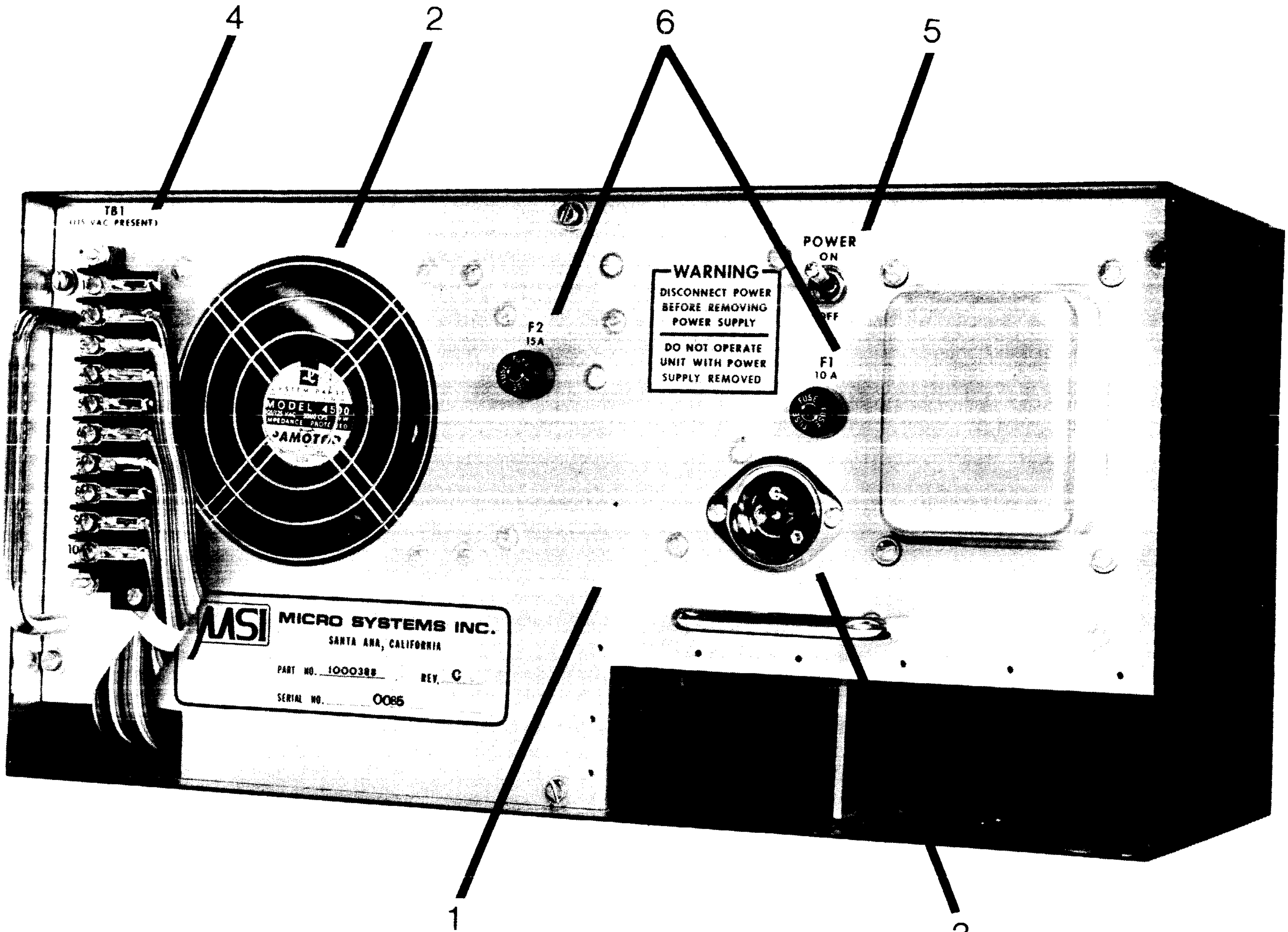

4
2
6
5
TB1
POWER
ON
OFF
F2
15A
WARNING
DISCONNECT POWER
BEFORE REMOVING
POWER SUPPLY
DO NOT OPERATE
UNIT WITH POWER
SUPPLY REMOVED
F1
10 A
MSI
MICRO SYSTEMS INC.
SANTA ANA, CALIFORNIA
PART NO. 1000388
REV. C
SERIAL NO. 0085
1
3

FIG 4

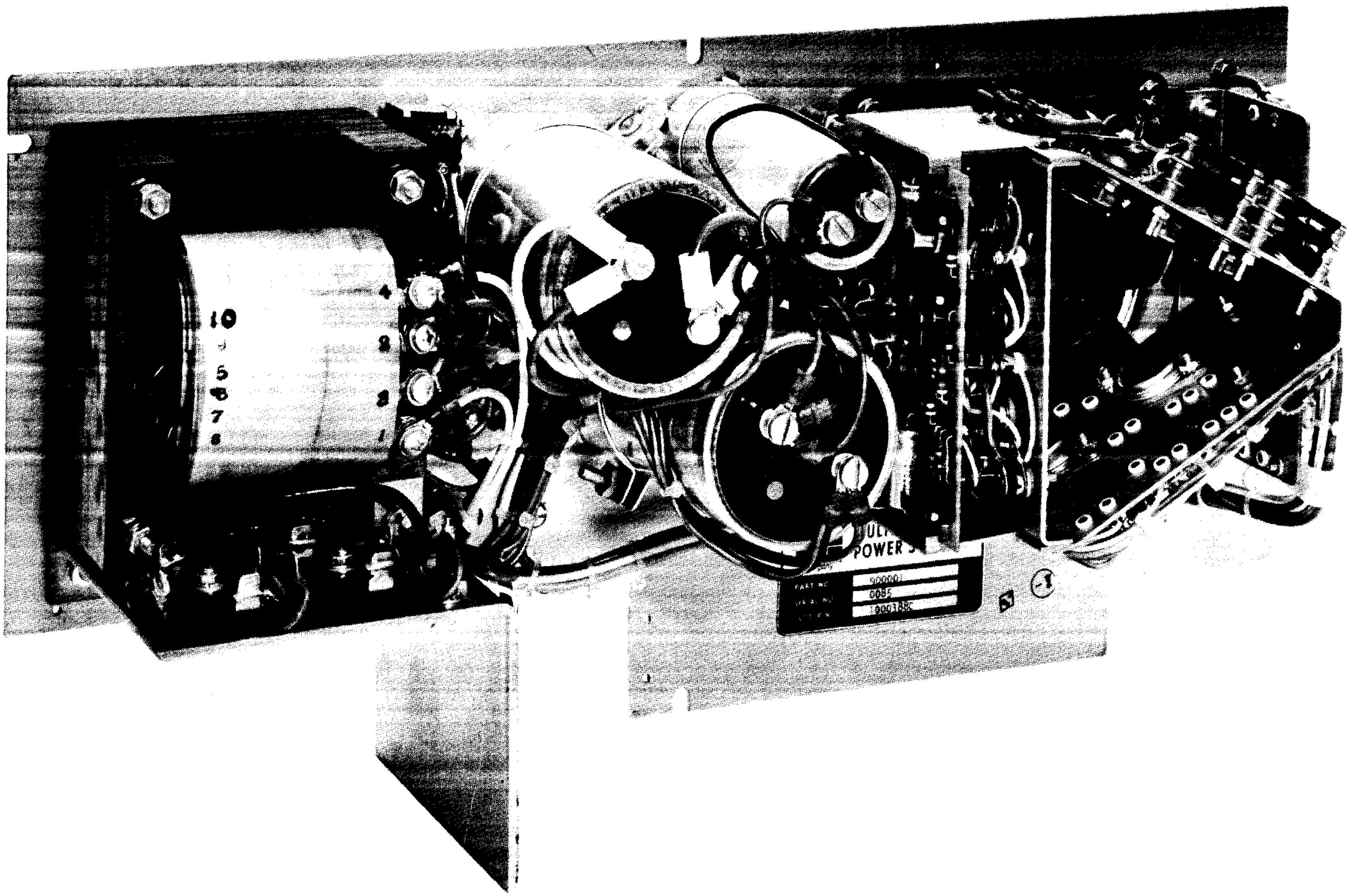


FIG 5

The overall dimensions of the computer are 8 3/4 inches high, 19 inches wide, and 23 inches deep. The voltage required for operation is 115/230VAC ±10% at 47-63 Hertz. The machine power is rated at 340 watts. The operational environment ranges from 10-90% humidity (without condensation). Fully expanded, the computer weighs 75 pounds, including the power supply.

When the power supply panel is removed from the rear of the enclosure, all circuit board sub-assemblies are accessible for removal. The layout of the sub-assemblies (rear view) is shown in Figure 6.

J1 J2	MEMORY (0-4095)	J10	DATA
		J11	CONTROL
		J12	DATA
J3 J4	MEMORY (4095-8191)	J13	PROCESSOR OPTIONS
		J14	ROS (0-255)
		J15	ROS (256-511)
J5 J6	MEMORY (8192-12,287)	J16	ROS (512-767)
		J17	ROS (768-1023)
		J18	I/O OPTION
J7 J8	MEMORY (12,288-16,383)	J19	I/O OPTION
		J20	I/O OPTION
J9	DMA OR MEMORY EXPANSION	J21	I/O OPTION

FIGURE 6

SUB-ASSEMBLY CIRCUIT BOARD LOCATION
(REAR VIEW OF CABINET)

The ROS connector slots, J14-J17, are wired on the backplane with the byte I/O bus as are the I/O Option connectors, J18-J21. Therefore, any vacant ROS connectors may be used to contain additional I/O option boards.

A DMA board normally plugs into connector J9. However, when memory is expanded beyond 16,384 bytes by means of an expansion cabinet, this connector is used for a memory expander board which contains drivers, receivers, and the cable connector for wiring the memory and DMA busses to the expansion cabinet. In such a case, DMA boards may be plugged into any odd numbered memory connector (J1, J3, J5, or J7), at the expense of a memory module. A maximum of two DMA boards may be contained in any system in which case the maximum core memory capacity would be 24,576 bytes. DMA boards may be mounted only in the main cabinet. When memory locations in the main cabinet are occupied by DMA boards, the vacated memory addresses can be addressed in the expansion cabinet so that memory locations are continuous. Proper location of expanded memory in combinations with DMA is detailed in the section on the expansion cabinet.

When the sub-assembly circuit boards are removed from the computer, the rear portion of the backplane and Front Panel PC Board Assembly can be seen. Figure 7 illustrates the mechanical assembly and interface between the backplane and some sub-assembly circuit boards.

1.2.2 Major Assemblies

A. Control Panel

The control panel provides computer control, mode indication, display of registers and manual command execution. There are two variations of the control panel, as shown in Figure 8, which provide all or some of the aforementioned functions:

i. Basic Control Panel - provides only computer control operation switches.

ii. System Control Panel - permits display of registers, manual command execution and computer control switches.

GENERAL NOTE REGARDING SWITCHES: Many of the switches on the control panel are alternate action type. That is, to set the switch it is depressed and to disable the switch it is depressed. Do not force the switch upward to disable it. Excessive upward force in an attempt to disable this type of switch will damage the switch. Depress to set and depress to disable all alternate action switches.

POWER SWITCH

The ON position of this switch enables excitation to the power supply for the generation of all voltages required for computer operation.

Mode Indicator Lamps

RUN lamp - when illuminated, indicates that the processor is running.

HALT lamp - when illuminated indicates that the power is on and the processor is not running.

SENSE SWITCHES

Four alternate action switches, the state of which may be transferred to a file register or machine register by the control micro command. These switches may be used to provide manual control of the program.

SELECT SWITCH

An alternate action switch used to select the source for the next command to be executed. The next command to be executed may be selected from the panel command switches or the read only storage.

CONTROL SWITCHES

The six control switches are used to establish and control the operational mode of the computer.

a. RUN - This momentary contact swtich places the processor in a run mode causing it to execute micro commands obtained from the read only storage.

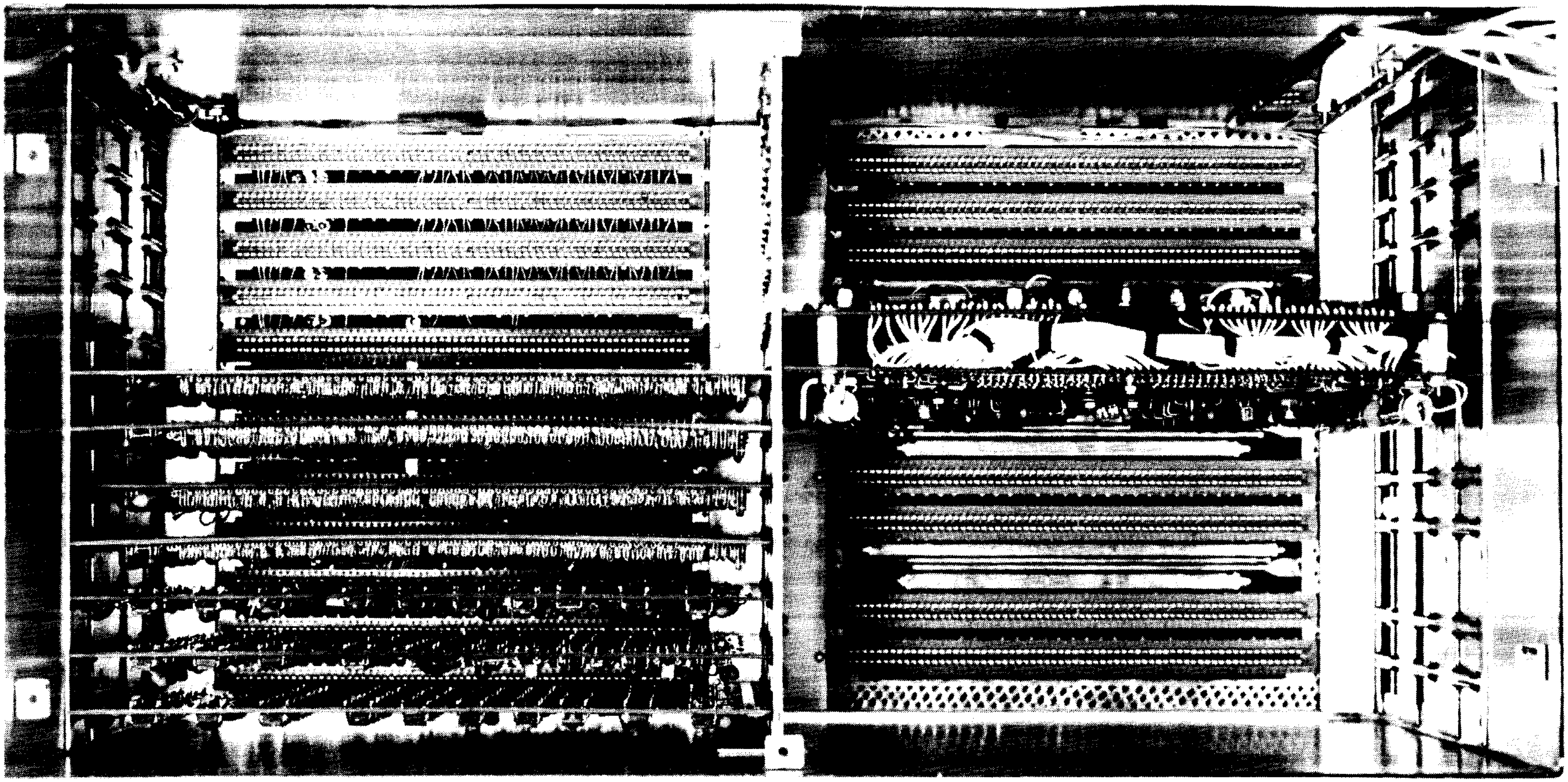
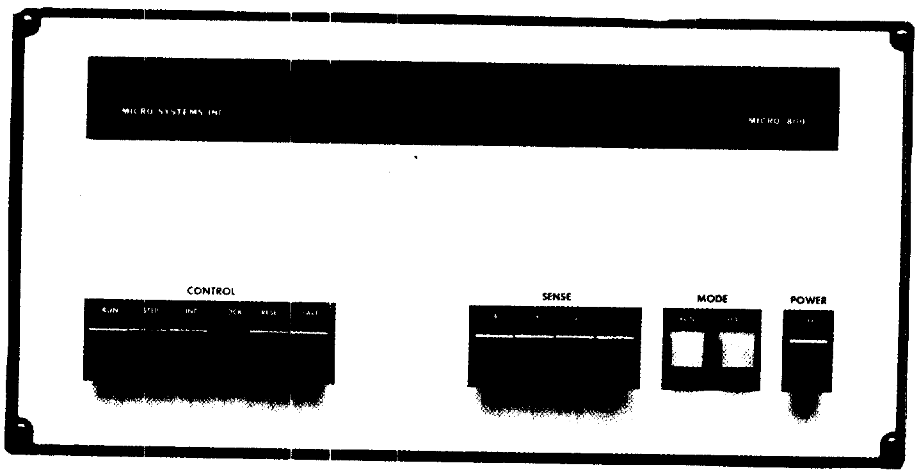
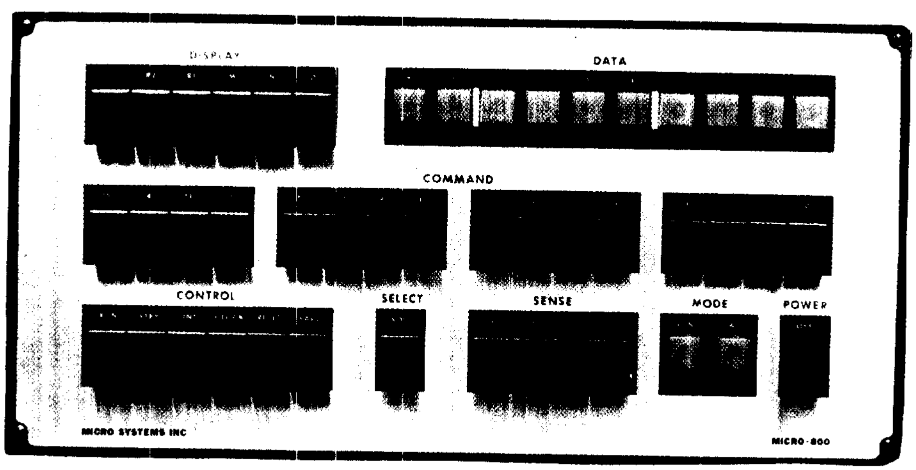


FIG 7



BASIC CONTROL PANEL



SYSTEM CONTROL PANEL

FIGURE 8

b. STEP - This momentary contact switch places the processor in the run mode and as long as the switch is depressed causes an internal interrupt. The switch is normally programmed to cause the processor to halt. Since the processor is forced to run when the switch is depressed, the machine can be programmed to cause a single instruction to be executed.

c. INT (INTERRUPT) - This momentary contact switch places the processor in the run mode and causes an internal interrupt. Normally, the switch is programmed to cause a console interrupt.

d. CLOCK - This momentary contact switch causes the processor to execute a single microcommand. If the processor is running at the time the switch is depressed the processor will come to a forced halt.

e. RESET - This momentary contact swtich halts the processor and clears the L register, I/O control register and other control circuits. The reset is made available to I/O devices.

f. SAVE - This alternate action switch is similar to the RESET switch but can be set on providing a continuous reset. If this switch is on at the time the power is turned on or off, the contents of the memory will not be lost or altered.

COMMAND SWITCHES (0-15)

These 16 alternate action switches are substituted for the read only storage when the SELECT switch is in the PANEL position. Depressing the CLOCK switch causes the command set on the switches to be executed The command may be repeatedly executed by depressing the RUN switch. These switches are used to gate registers to the A bus display and for entering data into the file and registers.

DATA LAMPS (0-9)

The eight data display lamps on the operator control panel display the data which is on the A bus of the processor. When the processor is halted the contents of a file or T register can be displayed be setting the proper command in the 16 COMMAND switches and enabling these switches by setting the SELECT switch in the PANEL position. The hexadecimal commands used for display are:

File Register F	CF00
T Register	B020
Link Register	B080

The 10 data display lamps on the system control panel display data which is selected as a function of one of the DISPLAY selector switches.

DISPLAY SELECTOR SWITCHES

These six interlocked switches select the register or bus to be displayed on the control panel data display. Displays which can be selected are:

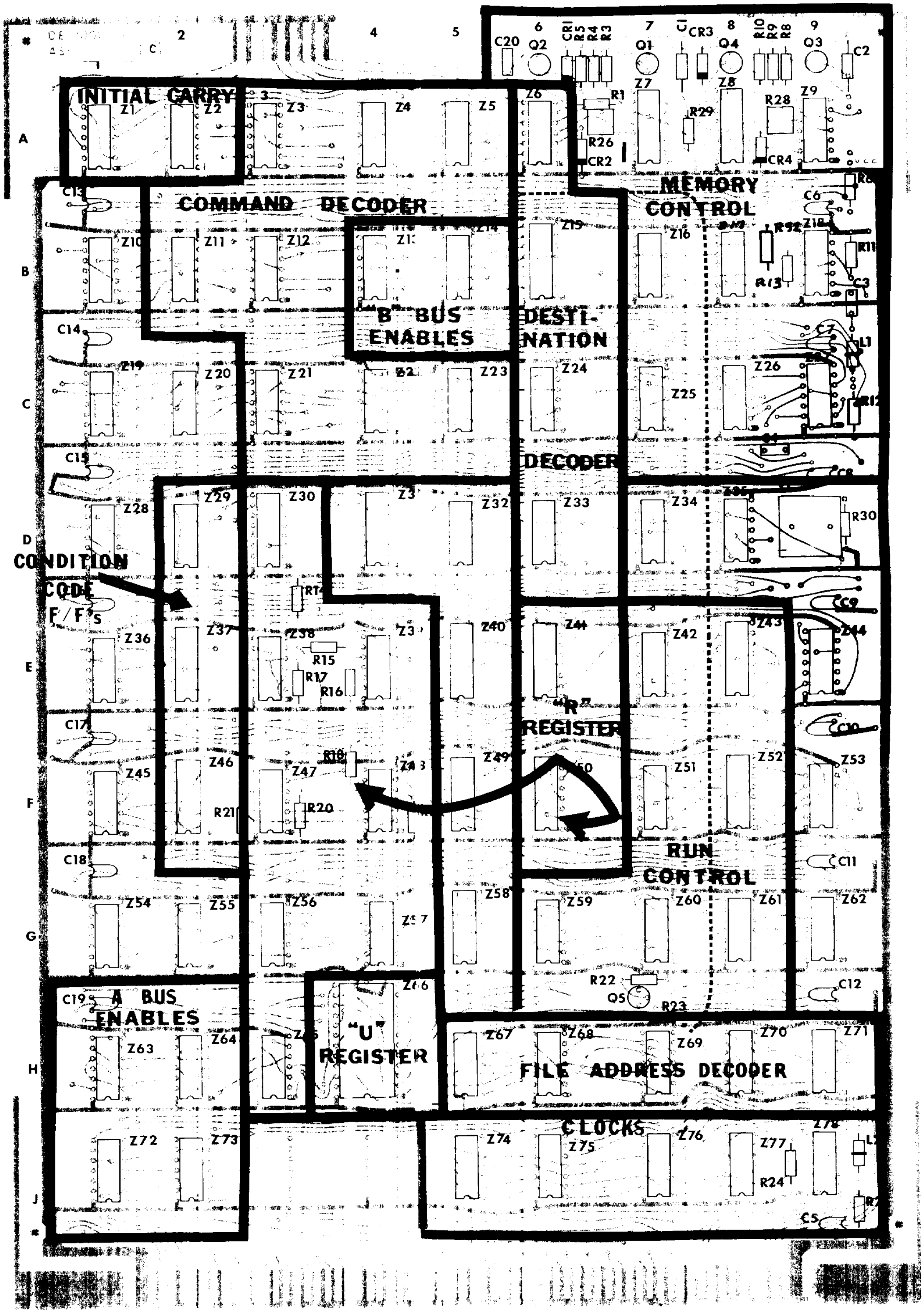
- L Register
- M Register
- N Register
- R2 - Read Only Storage - 8 high order bits
- R1 - Read Only Storage - 8 low order bits
- A Bus

When the machine is halted the output of the read only storage is the same as the contents of the R register, and is the next command to be executed.

CONTROL BOARD

The control board, shown in Figure 9, is a plug-in printed circuit board assembly. The location of the control board within the computer is shown in Figure 6.

The control board is interconnected to the backplane through a 65-pin, double row connector. (130 total pins). The connector on the board contains a locating slot, offset from the centerline, to insure that the board is properly oriented when being installed in the computer.



INITIAL CARRY
COMMAND DECODER
"B" BUS ENABLES
DESTI-NATION DECODER
MEMORY CONTROL
CONDITION CODE F/F's
"R" REGISTER
RUN CONTROL
A BUS ENABLES
"U" REGISTER
FILE ADDRESS DECODER
CLOCKS

FIGURE 9

The board is a rectangle 12.5 inches by 8.875 inches.

Components are mounted only on one side of the board. The boards are inserted into the cabinet with the component side on top.

Figure 9 also shows the control board "blocked out" with respect to the major functions performed by this sub-assembly and include and includes the following:

R Register

Command Decoder

Memory Control

Destination Decoder

Run Control

U Register

Clocks

File Address Decode

ROS Address Counter Bits 8, 9

A Bus Enable

B Bus Enable

Initial Carry

I/O Control

Oscillator (4.55 MHZ)

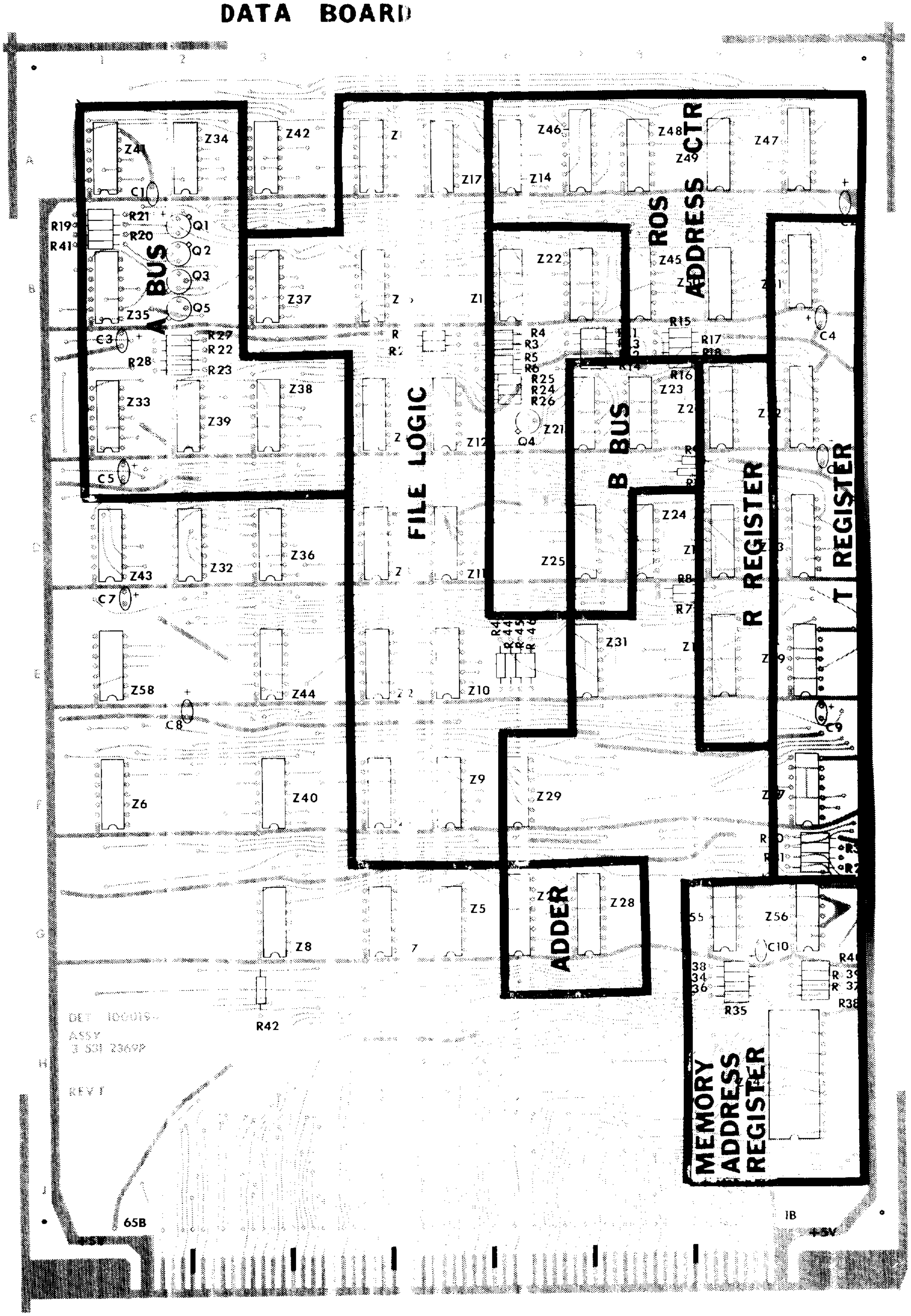
The board is arranged in a latter number Matrix, A through J (excluding I) by 1 through 9.

DATA BOARD

The data board, shown in Figure 10, is a plug-in printed circuit board assembly. The processor contains two data boards, Number 1 for bits 0 through 3, and Number 2 for bits 4 through 7. Figure 6, illustrates the relative location of both data boards in the computer.

The data boards are identical and interchangeable, and with some minor exceptions basically perform identical functions in the system. The data board is connected to the backplane through a 65-pin double row connector. The connector on the board contains a locating slot,

DATA BOARD



'IGURE 10

offset from the centerline to insure that the board is properly oriented when being installed in the computer.

The backplane mating connector wiring is configured to accommodate the functional differences in operation of the two data boards.

The data boards are of rectangular shape, 12.5 inches long by 8.875 inches wide. Components are mounted only on one side of the board.

Figure 10 also shows the data board blocked out with respect to the major functions performed and contained on this sub-assembly. They are:

File Logic

A Bus

B Bus

T Register

R Register

L Logic (ROS Address Counter)

Adder

Memory Address Register

The data boards are arranged in a letter/number matrix A through J (excluding I) by 1 through 10.

READ ONLY STORAGE

The read only storage (ROS) board shown in Figure 11, is a plug-in printed circuit board assembly. The location of read only storage boards in the computer is shown in Figure 6. A maximum of four ROS boards can be housed in the computer.

Physically, the ROS boards are identical but are not interchangeable in the four locations in the computer. Each ROS board contains a different section of the microprogram in the diode matrix (MAP) and randomly interchanging ROS boards would result in a non-functional program. The ROS address locations assigned to the four connectors are shown in Figure 2.

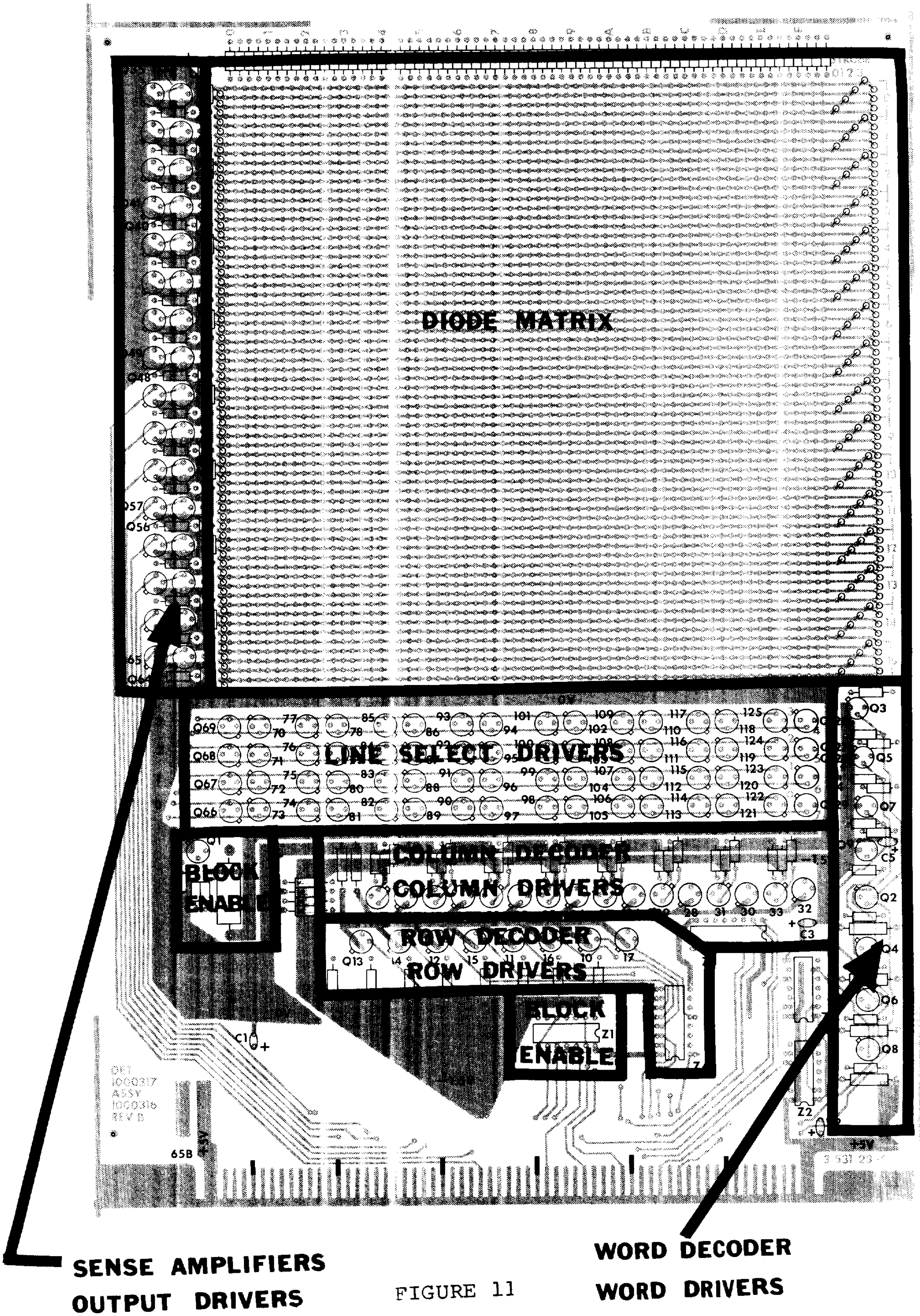

DIODE MATRIX
LINE SELECT DRIVERS
BLOCK ENABLE
COLUMN DECODER
COLUMN DRIVERS
ROW DECODER
ROW DRIVERS
BLOCK ENABLE
SENSE AMPLIFIERS
OUTPUT DRIVERS
WORD DECODER
WORD DRIVERS

FIGURE 11

The ROS boards are interconnected to the backplane through a 65-pin connector. The connector on the board contains a locating slot, offset from the centerline to insure that the board is properly oriented when being installed in the computer.

The ROS boards are of rectangular shape 12.5 inches long by 8.875 inches wide. Components are mounted only on one side of the board.

Figure 11 also shows the ROS board blocked out with respect to the major functions performed and contained on this sub-assembly. They are:

Diode Matrix (MAP)

Sense Amplifiers and Output Drivers

Word Decoder and Word Drivers

Line Select Drivers

Column Decoder and Column Drivers

Block Enable

Row Decoder and Row Driver

The power requirement for the ROS board is a function of usage. When the ROS board is selected the power requirement is:

+5V at 1.05a

-1.5V at 950ma

When the ROS board is not selected the power requirement is:

+5V at 770ma

-1.5V at 0a

MEMORY BOARD

The memory board assembly consists of two interconnected sub-assemblies arranged in a sandwich configuration. The upper sub-assembly (Figure 12) is a combination of the sense inhibit circuitry and the core frame boards and the lower assembly shown in Figure 13 contains the drive board circuitry. The two boards are mechanically and electrically interconnected to form the memory board assembly.

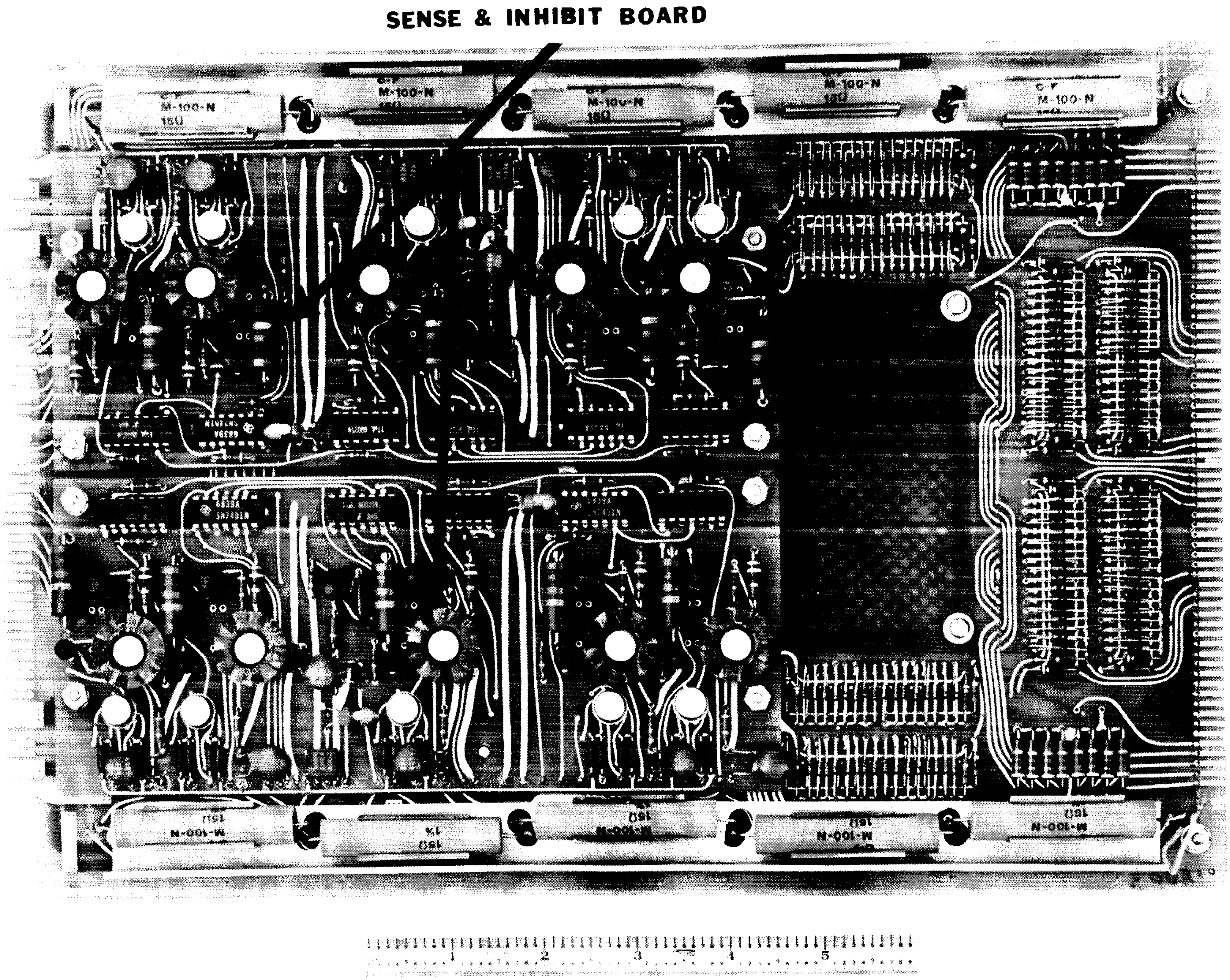
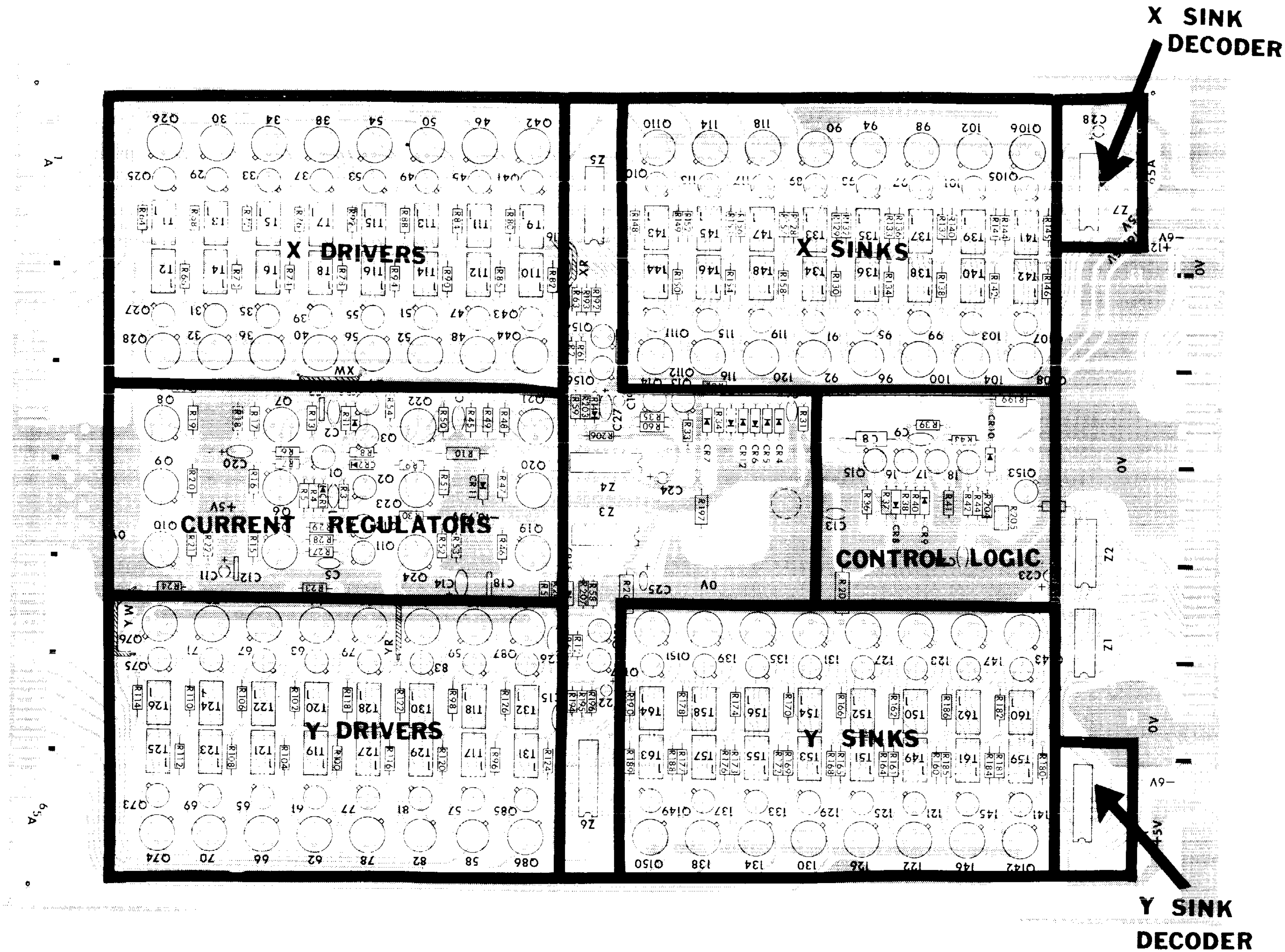


FIGURE 12



X SINK DECODER
X DRIVERS
X SINKS
CURRENT REGULATORS
CONTROL LOGIC
Y DRIVERS
Y SINKS
Y SINK DECODER

FIGURE 13

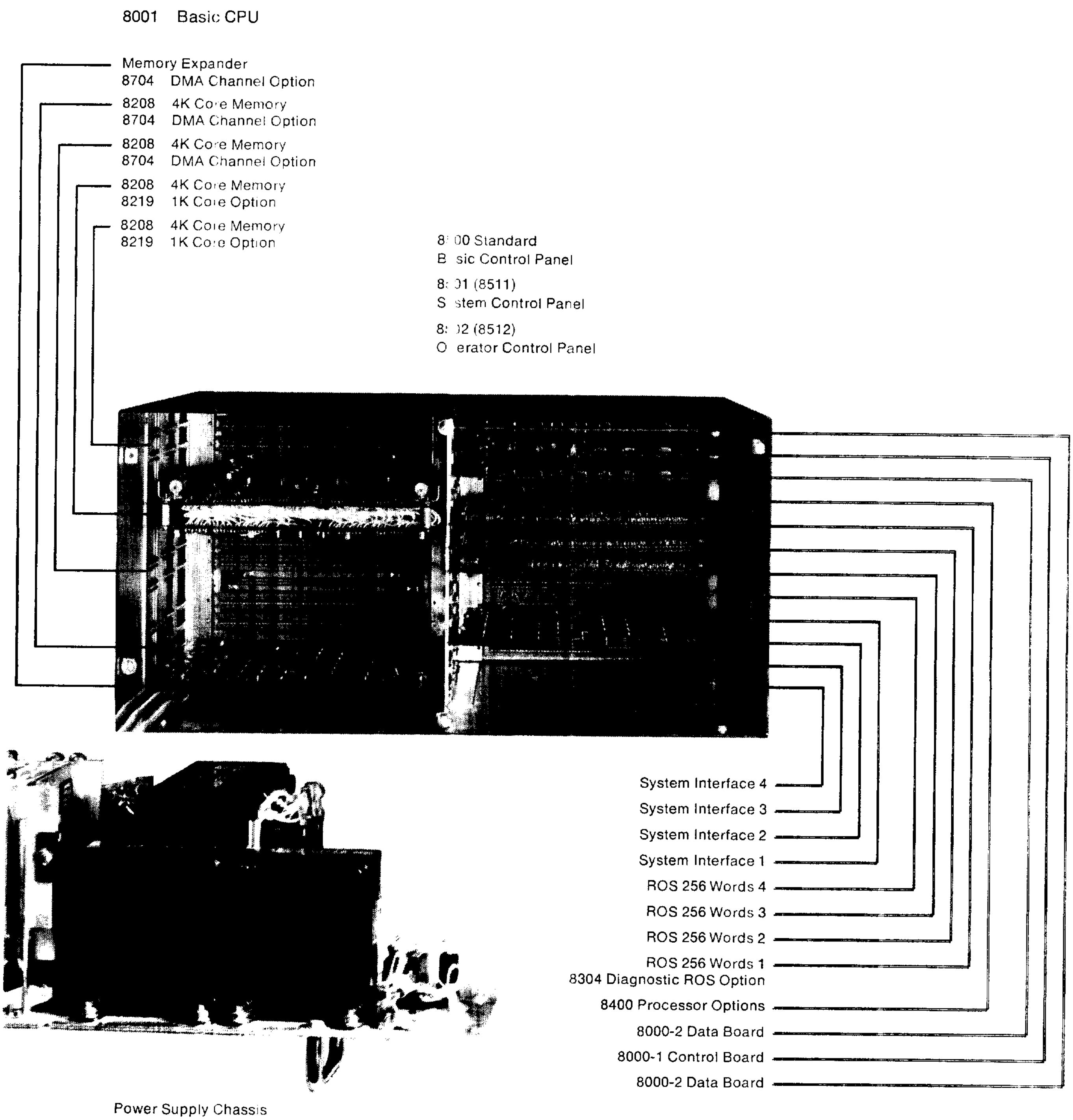

8001 Basic CPU
Memory Expander
8704 DMA Channel Option
8208 4K Core Memory
8704 DMA Channel Option
8208 4K Core Memory
8704 DMA Channel Option
8208 4K Core Memory
8219 1K Core Option
8208 4K Core Memory
8219 1K Core Option
8 00 Standard
B sic Control Panel
8 01 (8511)
S stem Control Panel
8 02 (8512)
O erator Control Panel
System Interface 4
System Interface 3
System Interface 2
System Interface 1
ROS 256 Words 4
ROS 256 Words 3
ROS 256 Words 2
ROS 256 Words 1
8304 Diagnostic ROS Option
8400 Processor Options
8000-2 Data Board
8000-1 Control Board
8000-2 Data Board
Power Supply Chassis

FIGURE 14

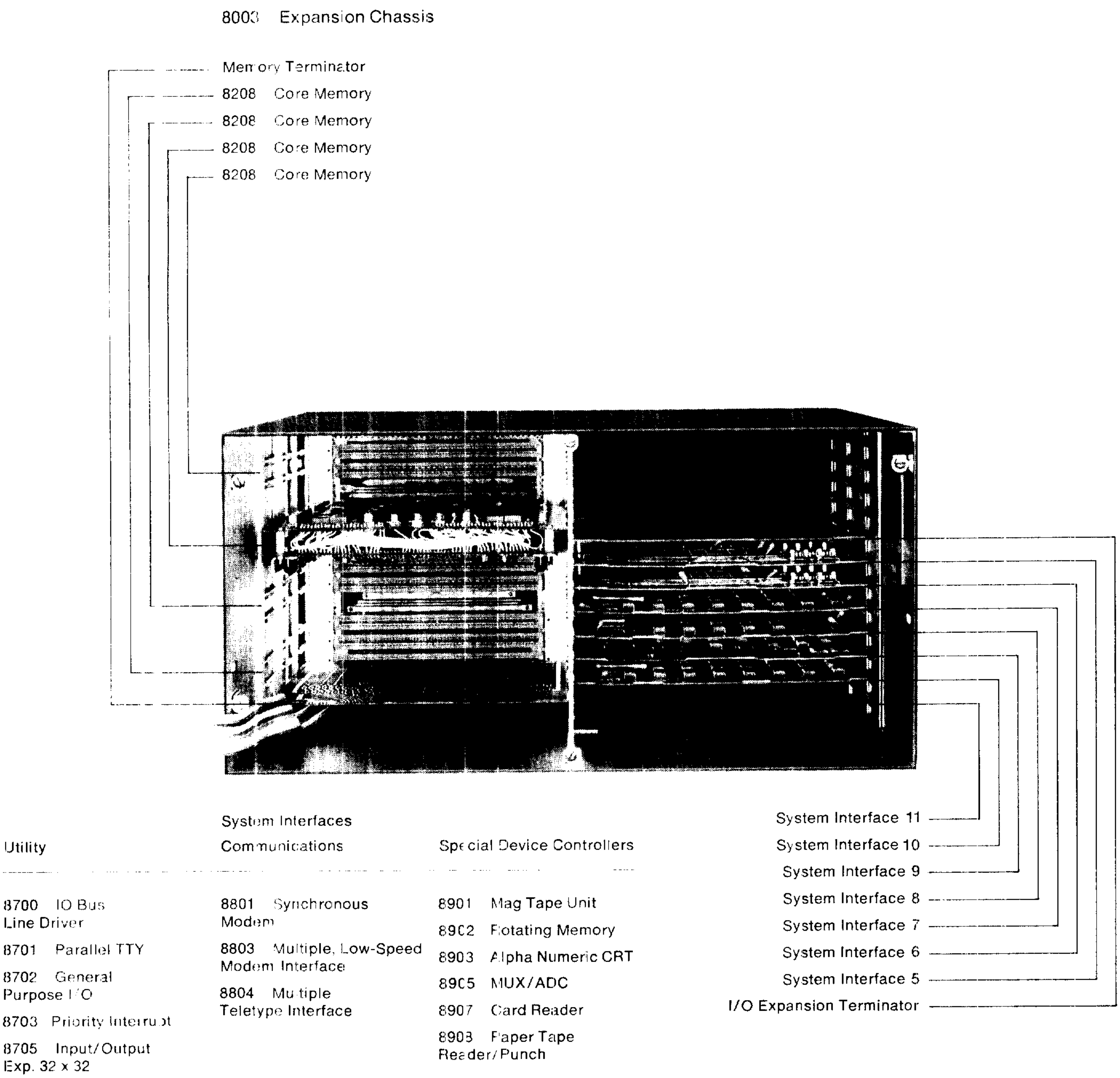

8003 Expansion Chassis
Memory Terminator
8208 Core Memory
8208 Core Memory
8208 Core Memory
8208 Core Memory
System Interface 11
System Interface 10
System Interface 9
System Interface 8
System Interface 7
System Interface 6
System Interface 5
I/O Expansion Terminator
Utility
8700 IO Bus Line Driver
8701 Parallel TTY
8702 General Purpose I/O
8703 Priority Interrupt
8705 Input/Output Exp. 32 x 32
System Interfaces Communications
8801 Synchronous Modem
8803 Multiple, Low-Speed Modem Interface
8804 Multiple Teletype Interface
Special Device Controllers
8901 Mag Tape Unit
8902 Rotating Memory
8903 Alpha Numeric CRT
8905 MUX/ADC
8907 Card Reader
8908 Paper Tape Reader/Punch

FIGURE 15

The drive board, Figure 13, contains the X and Y drives and sinks X and Y driver and sink decoders, control logic and current regulators.

Each board contains a double row connector, each row of 65 pins for mating to the backplane.

The location of the interconnected memory sub-assemblies within the computer is shown in Figure 6. A maximum of four memory assemblies can be housed in the basic computer cabinet. Memory expansion capabilities and capacity are presented in Section 1.2.3.

1.2.3 System Configurator

The computer has the flexibility for substantial expansion. This section shows the expansion capabilities and gives a brief explanation of the interconnect and the function of the expansion sub-assemblies.

Figure 14 shows the basic computer and the two types of control panels, core memory and ROS boards. Associated with each board is an identifying part number. The power supply is also part of the basic computer.

Figure 15, shows the additional hardware configuration utilizing the expansion chassis. If an expansion chassis (Figure 15) is required, the basic computer must include a memory expander board to interface with the additional memory of the expansion unit and its own power supply.

The following information lists the various options available and gives a brief description of their functions.

STANDARD OPTIONS

Central Processor Option Boards

8401 Power Fail and Automatic Restart - Provides

interrupt when loss of power is imminent and when power is turned on.

8402 Memory Parity - Includes the memory parity

generator and checker logic and an interrupt when an error is detected.

<u>8404 Real Time Clock</u> - Provides an internal interrupt at a crystal controlled timing rate.

<u>8400 Option Board</u> - Includes all of the above processor option items.

Utility Interfaces

<u>8700 Input/Output Line Driver and Receiver Board</u> - Expands the internal I/O bus to an external I/O bus to an external bus allowing integration of up to 10 peripheral interfaces under program control, or concurrent data transfer with interrupt.

<u>8701 Parallel Teletype Controller</u> - Assembles and disassembles serial information to and from the teletype for parallel transfer to and from the computer under program control or concurrent block transfer.

<u>8702 General Purpose I/O Board - Wire Wrap</u>

Accomodates 14, 16, or 24 pin integrated circuit sockets in the following quantities:

- 135 units - 14 or 16 pin sockets
- 24 units - 24 pin sockets

<u>8703 Priority Interrupt Board</u> - Allows interfacing of 8 external interrupt lines with expansion capability to 64 lines using 8 boards. Priority, timing, storage of interrupt, address generator functions and independent enabling or disabling of each interrupt are provided.

<u>8704 Direct Memory Access Selector Channel</u> - Provides for transfer of 8 bit bytes directly between external devices and core memory. Transfer is in single block form or continuous cycling of one or linked blocks. An internal interrupt indicates "end of transfer" to the CPU program.

8705 Input/Output Expander - Full Word (32 bits) - Expands the 8 bit I/O bus into multiple (4) byte I/O under processor control. The outputs are independently latched. Outputs and inputs are standard DTL or TTL logic levels with the capability to interface with MUX-ADC's, DAC's, keyboards, and low speed peripheral devices such as incremental tape units, buffered line printers, and X-Y plotters.

Communications Options

8801 Synchronous Modem Controller - An interface to a 201 or equivalent data set, this option operates with point to point, or switched networks with optional automatic calling-answering for either 2-wire or 4-wire service. Data transfers are on a byte basis under concurrent input/output or programmed control. A sync character detection circuit is provided in the interface for obtaining character synchronization. Interface levels are per EIA Standard RS-232-B.

8803 Multiple, Low-Speed Modem Interface - This interface is designed to accommodate up to sixteen 103 type modems. It provides for two output circuits and four input circuits to each modem. Identical signals for all eight modems are transferred in parallel via the computer's byte I/O bus. All interface circuits comply with EIA Standard RS-232-B.

8804 Multiple, Teletype Interface - This interface board can accommodate up to 24 locally connected teletypes. Operation is 4-wire full duplex with 20 ma currents (60 ma is available as an option). Data for one of the 3 groups of eight teletypes is transferred in parallel via the byte I/O bus.

Device Interfaces

8907 Card Reader - Provides control of an 80 column card reader, 12 lines per column in hollerith or two binary bytes. Uses the Mohawk Data Sciences Corp. SCCR 6002, or equivalent. Code Conversion to BCD or binary is selectable under program control and data transfer can be on a character or on block basis with card reading rates of 225 or 400 cards per minute.

8908 Paper Tape Reader/Punch - Consists of two separate functions which can be mounted on the same board. Data transfer is either a single word or concurrent block transfer with end of block interrupts provided. The punch data is buffered.

Special Interfaces

Numerous special interfaces of options can be provided by Micro Systems Inc., with relatively short lead times. These include I/O device controller interfaces such as alpha numeric CRT; rotating memory; magnetic tape unit, and MUX/ADC.

1.3 COMPUTER SPECIFICATIONS

Type - A microprogrammable general purpose computer.

Arithmetic Unit - Parallel, binary, fixed point. One's and two's complement for negative numbers.

Commands - 16 basic commands each 16 bits in length.

Speed - 4.55 MHz clock rate. All instructions are executed in 220 nanoseconds except for the jump and skip commands, which require an additional 220 nanoseconds interval.

Core Memory - Memory modules of 4,096 bytes by 8 or 9 bits and 1,024 by 9 bits are available. Wide temperature range lithium cores are used. Operation in the system is a 1.1 microseconds full cycle and 0.66 microsecond half cycle. Memory is expandable to a maximum of 32,768 bytes.

Read Only Storage - Read Only Storage (ROS) uses discrete diodes in printed circuit board modules of 256 16-bit words. The ROS cycle time in the system is 220 nanoseconds.

Input/Output - An 8-bit parallel byte I/O bus permits programmed and fully automatic concurrent transfers. A serial I/O interface allows interfacing teletypes or similar devices. Up to two Direct Memory Access (DMA) channels permit a maximum combined transfer rate of up to 909,000 bytes per second.

Interrupts - An interrupt request flag, which can be tested by micro commands is available. Any I/O interfaces may be designed to generate priority interrupts via the byte I/O bus.

Computer Cabinet - The processor, memory to 16K, I/O interfaces, power supply and fan are enclosed in a cabinet measuring 8 3/4 inches high, 19 inches wide, and 23 inches deep. Fully expanded cabinet weight is 75 pounds.

Power - 115/230VAC $\pm$10%, 47-63 Hz, 340 watts.

Environment - 0° - 50° (32° - 122°F) 10-90% humidity (without condensation).

Software - AP800 is an Assembly Program, written in FORTRAN IV, used to generate the Read Only Storage diode maps.

1.4 FUNCTIONAL DESCRIPTION

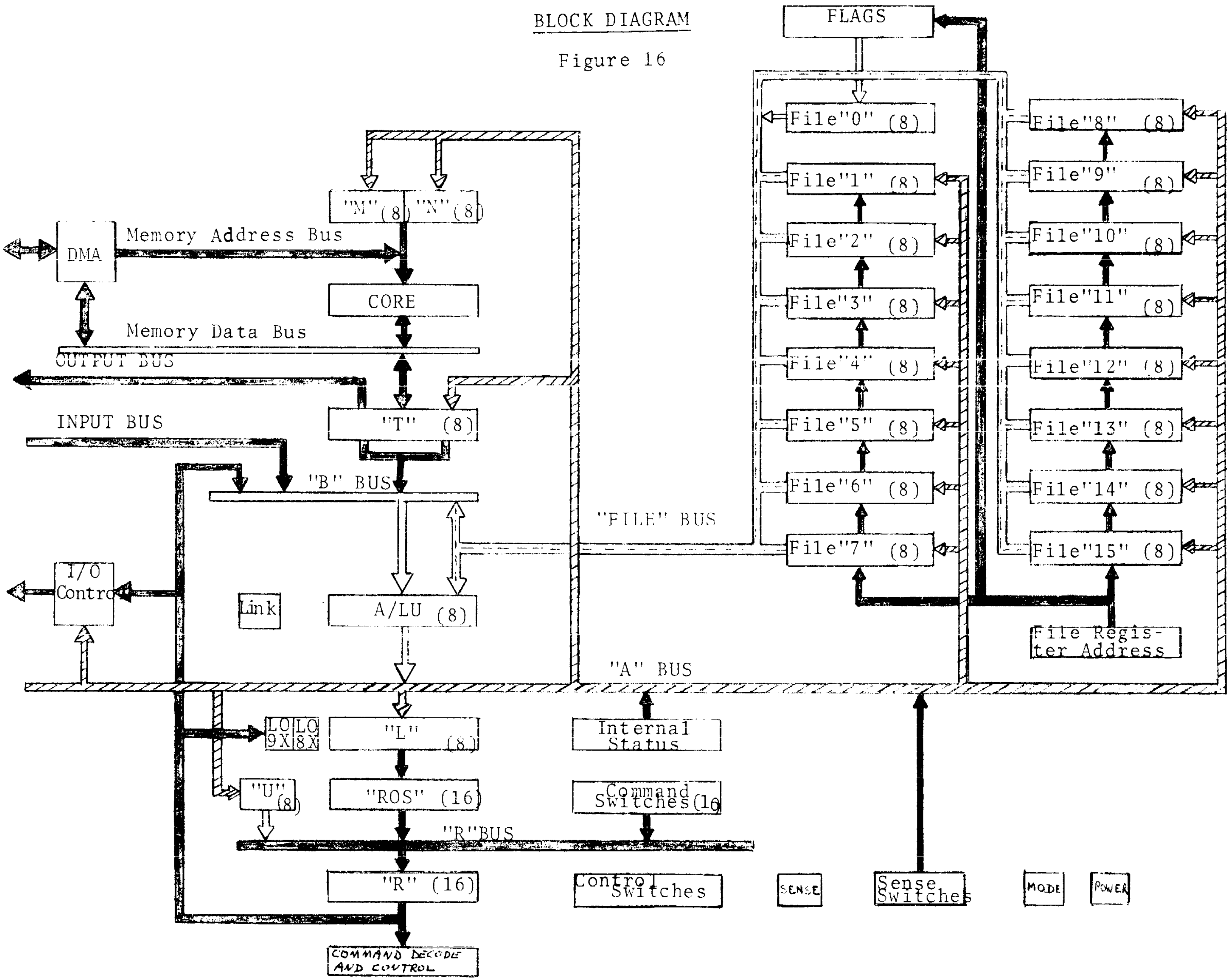
The computer is a bus organized machine designed around a file of 16 programmable registers and employing microprogrammed control. The basic elements of the machine are shown in the block diagram of Figure 16.

The machine is organized around an 8 bit arithmetic/logic unit (ALU) which performs all arithmetic, logic and shifting functions. One of the inputs to the ALU is from the file of registers containing 15 general purpose registers and one register of internal and external condition flags. The other input to the ALU is from the B bus which derives its input from the T register, the input bus or an eight-bit literal contained in the command. The type of command, selection bits in command and the state of the I/O control register determine the B bus input which may be zero or all one bits. The output of the ALU is the input to the file registers and other machine registers.

The read only storage is organized into 256 word modules. Each of the modules (four maximum) receives an address from the machine program counter (L Register) which contains the read only storage address of the next command to be executed. The output of the read only storage is gated into the R bus which is then clocked into the 16 bit command register (R Register) where the command is decoded. The U Register is allowed to OR onto the eight high order bits of the R bus under certain

COMPUTER FUNCTIONAL BLOCK DIAGRAM

Figure 16



conditions to allow for dynamic modification of the ROS program steps. The control console command switches may be entered onto the R bus, instead of the read only storage modules, to provide for manual entry of the commands.

The core memory consists of 4096 byte modules with expansion to a maximum of 32,768 bytes. Data transforms between the core memory modules and the processors T Registers on the Direct Memory Access (DMA) modules are performed over the bi-directional memory data bus. The memory address from the processor's memory address register (M and N) or the DMA module.

Input/Output is performed by an eight-bit input bus, an eight-bit output bus (which originates with the T register) and a group of control lines which are under microprogram control through the I/O Control registers.

1.5 GLOSSARY OF TERMS AND SYMBOLS

This section is devoted to the definition of terms and symbols used herein, on the hardware items and in the documentation.

Definitions for the headings on the following table are:

TERM: The abbreviation for the control term or signal being described.

JACK NO.: The connector identification number for the board to which the signal is related.

BOARD: The board upon which the signal is found (CB: Control Board; DB: Data Board; etc.).

DEFINITION: A short definition of the signal, in words.

In general, logic terms are identified by a four letter mnemonic. Logical negation is designated by a slash (/) following the last letter (e.g. ADSB/ is the complement of the term ADSB).

TERM	JACK NO.	BOARD	DEFINITION
ADDX	J11	CB	A Bus Add Control
ADSB/	J11	CB	Commands Eight and Nine
ANDX	J11	CB	A Bus and Control
AENI	J11	CB	A Bus Enable Internal Status Control
AENS	J11	CB	A Bus Intersense Switch Control
AFLT	J11	DB#2	Adder/Overflow
ASRF	J11	CB	A Bus Shift Right File Control
AUO-	J10	DB#1	Adder Output
	J12	DB#2	
A--X	J10	DB#1	A Bus
	J12	DB#2	
AZ03	J10	DB#1	0 Detect on A bus 0-3
AZ47/	J12	DB#2	0 Detect on A bus 4-7
BENI	J11	CB	Enable Input Bus to B Bus
BENR	J11	CB	Enable R Register to B Bus
BO-X	J10	DB#1	B Bus
	J12	DB#2	
BNTM	J11	CB	T Register Complement Output Select to B Bus
CC-X	J11	CB	Condition Code (Flags Flip-Flops)
CGOX/	J11	CB	Control Group 0 Select
CG7X/	J11	CB	Control Group 7 Select
CLK-/	J11	CB	Clock Term
CLK2/	J11	CB	File Write
CLK3/	J11	CB	"L" Load
CLK4/	J11	CB	"T" Load
CLK5/	J11	CB	"L" Advance
CLK6	J11	CB	Ungated
CLRP/	Front Panel P.C.B.		Control Switch Common Return
CPEN/	Front Panel P.C.B.		Control Panel Enable
CPEN	Front Panel P.C.B.		

TERM	JACK NO.	BOARD	DEFINITION
CPH1	J11	CB	Clock Phase One
CPH2/	J11	CB	Clock Phase Two
CPXX	J11	CB	Command Six (Compare)
CR--/	Front Panel P.C.B.		Control Panel Command Switches
CRY-			Carry Output
CSTP	J11	CB	Clock Stop
CYIA	J11	CB	LSB Carry to ADDER
CYXX	J11	CB	Command Eleven
DENB/			
DES-	J11	CB	Destination Register Address
DMAH/	J11	CB	DMA Half Cycle
DMAR/	J11	CB	DMA Request
DMAW/	J11	CB	DMA Write Cycle
EXIO	J11	CB	External I/O Control
	J11	CB	
FAZD	J11	CB	File Register 0 Selected
FINH	J11	CB	File Output Inhibit Control
FLCK	J11	CB	File Latch Control
FO-X	J10	DB#1	File Register Output
	J11	DB#2	
FWRT	J11	CB	File Right Enable
HLTP/	Front Panel P.C.B.		Halt Switch
HLTL	J10	DB31	Console Interrupt Flip-Flop
INTC	J11	CB	
INTP/	Front Panel P.C.B.		Console Interrupt Switch
IO-X	J11	CB	I/O Control Register
IOXX	J11	CB	Command Seven
ISTX	J12	DB#2	Internal Status Interrupt
IST1	J10	DB#1	Internal Status Interrupt
LCRY/	J10	DB#1	L Register Carry from first 4 bits
LFAF/	J11	CB	Command Two or Three (Load File and Add to File)
LFXX	J11	CB	Command Two

TERM	JACK NO.	BOARD	DEFINITION
LJKX	J10	DB#1	
	J12	DB#2	
LINK	J11	CB	Link Flip-Flop
L--X	J10	DB#1	
	J11	CB	L Register
	J12	DB#2	
LR0X/	J11	CB	L Register Select
LR1X/	J11	CB	L Register Select
LRXX	J11	CB	Command One (Load Register)
LRSP			Load Control Group 7
LSGX	J11	CB	Commands Twelve, Thirteen, Fourteen and Fifteen
MBSY	J11	CB	Memory Busy
MCLR/	J11	CB	M Register Clear
MDNA/	J11	CB	Memory Data Not Available
MDO-	J10	DB#1	Memory Data Bus
	J12	DB#2	
MDRC/	J11	CB	Memory Data Read Control
MLCR/	J1-2	Drive Bd.	Master Reset
MRST/	Front Panel P.C.B.		
MRTX/	J11	CB	Memory Read Timing Control
MRXX/	J11	CB	M Register Select
MSTP	J11	CB	Memory Busy or DMA Request
MWTX	J11	CB	Memory Write Timing Control
MYXX	J11	CB	Command Ten
NRXX/	J11	CB	N Register Select
READ	J11	CB	Memory Read
RENU	J11	CB	U Register enable to Read Only Storage Data Bus
RINH	J11	CB	Run Inhibit Flip-Flop
RJKX	J11	CB	R Register Data Inhibit
RS--	J14	ROS	Read Only Storage Data Output
RTXX/	J11	CB	Read Timing
RUNH/	J11	CB	RUNX Reset due to Halt Command

TERM	JACK NO.	BOARD	DEFINITION
RUNL	J12	DB2	Run Lamp Output
RUNP	Front Panel	P.C.B.	Run Switch
RUNR	J11	CB	RUNX Reset due to Step Switch
RUNS	J11	CB	RUNX Set Term
RUNX	J11	CB	Run Flip-Flop
R--X	J10	DB#1	
	J11	CB	R Register
	J12	DB#2	
SHIO	J11	CB	A Bus Second Level Gating Control
SHLX	J11	CB	A Bus Shift Left Control
SHRX	J11	CB	A Bus Shift Right Control
SHXX	J11	CB	Command Fifteen
SBXX	J11	CB	Command Nine
STPP/	Front Panel	P.C.B.	Step Switch
SS1X	J11	CB	Switch Synchronizer Flip-Flop
SS2X	J11	CB	Switch Synchronizer Flip-Flop
TCLR/	J11	CB	T Register Clear
TDBC	J11	CB	T Register to Data Bus Control
TRXX/	J11	CB	T Register Select
TNXX	J11	CB	Command Five
TNZX/	J11	CB	Command Four or Five
TZXX			Command
UO-X	J11	CB	U Register
URXX/	J11	CB	U Register Select
WTXX/	J11	CB	Write Timing
XORX	J11	CB	A Bus Exclusive OR Control
X--X	J11	CB	X addressing line for File Register
Y--X	J11	CB	Y address lines for File Register

1.6 RELATIONSHIP OF DOCUMENTATION (DRAWING) NOTES TO HARDWARE CONFIGURATION

This section presents the user with an interpretation of drawing notations and their relationship to the physical hardware. The relationship will be presented in example form for a section of the control board schematic (a portion of the R Register) as shown in Figure 17.

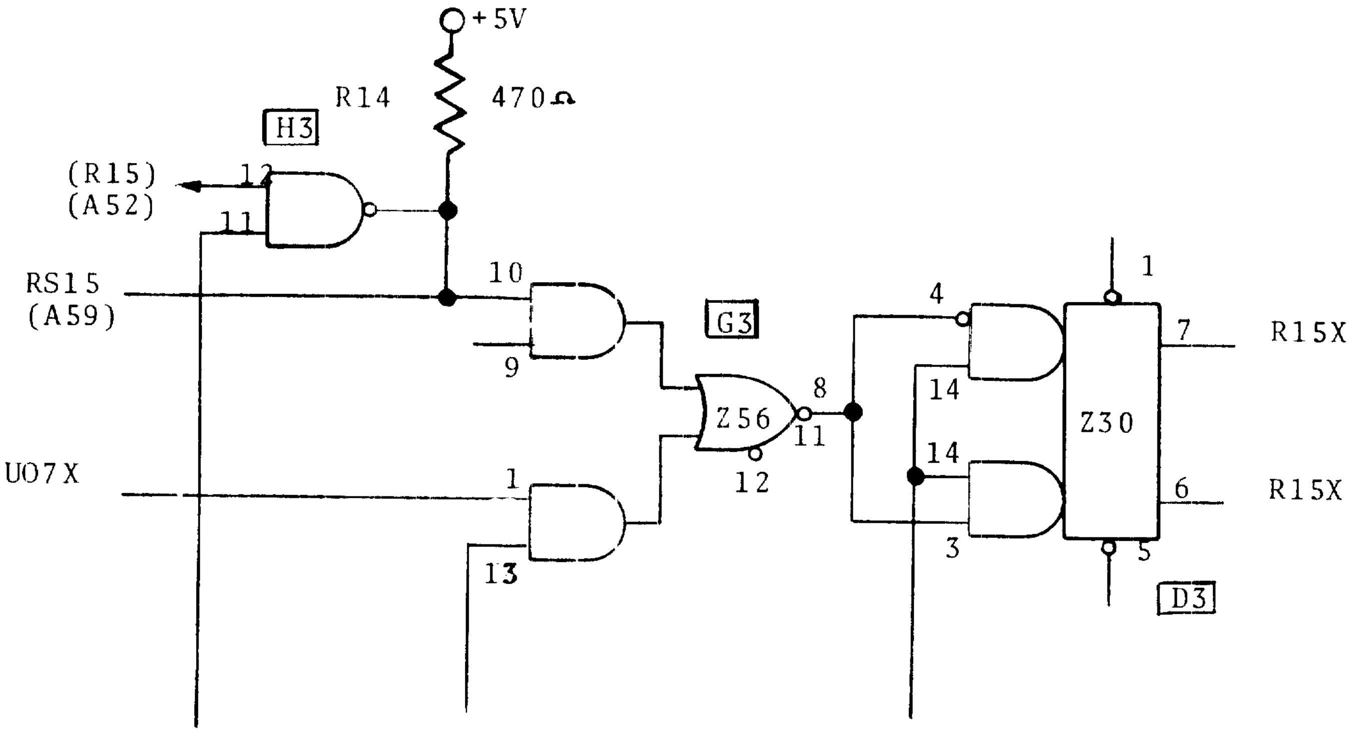


FIGURE 17

Portion of Control Board Schematic (Portion of the R Register)

Above the logic element Z65 is a notation which appears in a small rectangle and contains a letter and a number. This notation specifies a letter/number coordinate on the control board and allows the user to locate the Z65 component on the control board.

A sketch of the control board is shown in Figure 18.

The row of numbers from 1 to 10 and the column of letters A through H and J are typical of all circuit boards in the computer.

In a similar manner, components Z56 located at G3 and Z30 located at D3 may be found. This procedure is effective for all sub-assembly circuit boards in the machine.

Each side of a circuit board is designated by A for the solder side of the board and B for the component side. When designating connector terminations on the schematics, the letter A or B will appear with a number from 1 through 65. For example, the term A52 indicates that the wire (or signal) in question terminates at the connector on the solder side of the board at pin 52. In a like manner, the term B36 indicates the wire (or signal) in question terminates at the connector on the component side of the board at pin number 36.

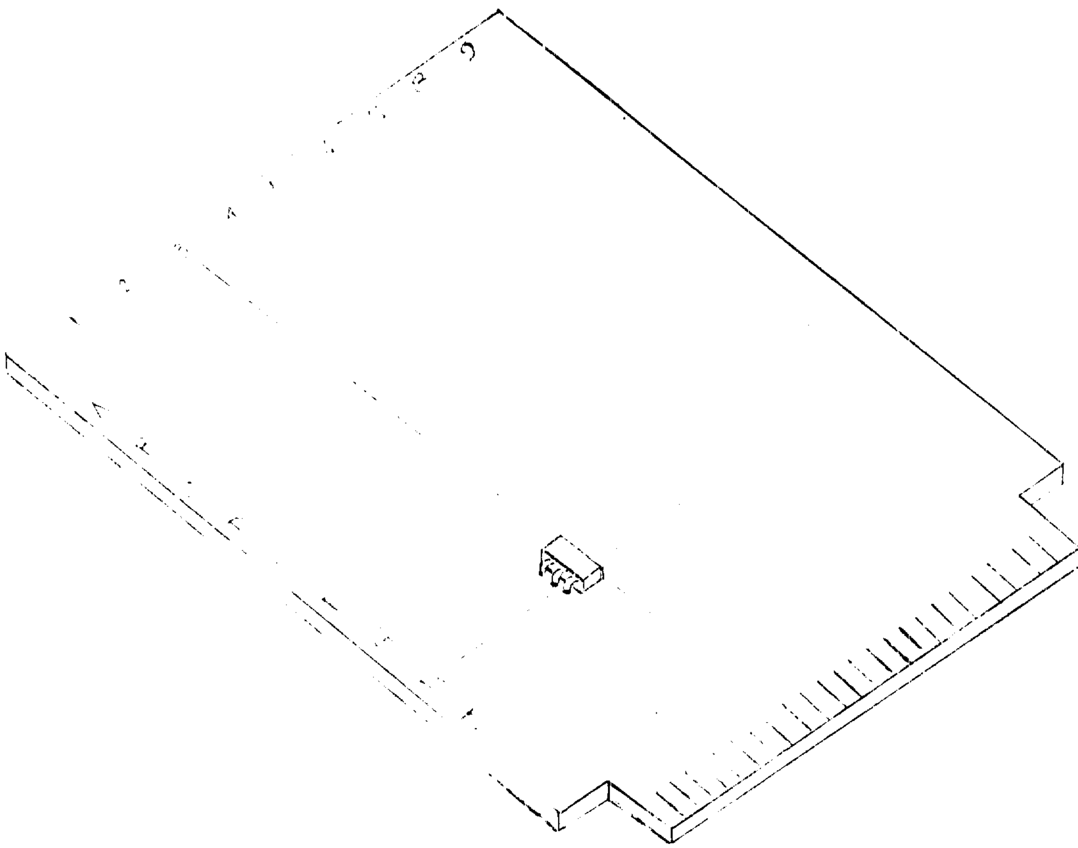


Figure 18

Sketch of Control Board

SECTION 2

PROGRAMMING AND OPERATION

2.1 PROGRAMMING

This section contains descriptions of the computer commands. With each description is a diagram showing the format of the command and its operation code, given in hexadecimal. Associated with the name of the command is its mnemonic code and a word description of the machine operation in response to the command. Each command takes one clock cycle (220 nanoseconds) unless the L Register is designated as the destination of the result, in which case the command execution time is two cycles.

2.1.1 Command Formats

There are three basic command formats. Each command is 16 bits in length and is contained in a single read only storage location.

a. Literal Commands

The literal class of commands have the following format:

OP	f/r	Literal
15		0

In this format the operation code occupies the four high order bits. Bits 11-8 contain either a file register designator (f) or a register or control group designator (r). Bits 7-0 contain an eight-bit literal which is transferred as an operand to the B-bus.

b. Operate Commands

The operate class of commands have the following format:

OP	f	c	*	r
15				0

In this format the operation code occupies the four high order bits. Bits 11-8 contain a file register designator (f) which specifies one of the 16 file registers to be used in command execution. Bits 7-4 contain control option bits (c) which are unique to the specific command. When bit 3 is a one, the result of an operate class command is inhibited from being placed in the designated file register. Symbolically, this is specified to the program assembler by appending an * to the command mnemonic. The register designator (r) in bits 2-0 specifies a processor register to receive the result of the operation. The register's identifier is added as a second character of the command mnemonic. The register codes are given in Table 1.

TABLE 1. REGISTER DESIGNATORS FOR OPERATE COMMANDS

DESIGNATOR	MNEMONIC	REGISTER
0		None
1	T	T Register
2	M	M Register
3	N	N Register
4	L	L Register-addresses: 000-0FF and 200-2FF
5	K	L Register-addresses: 100-1FF and 300-3FF
6	U	U Register
7	S	U Register ORed into command (except for Control command)

c. Execute Command

The execute command causes the contents of the U register to be ORed with the eight high order bits of the command to form an effective command. This operation is also performed when r = 7 for the operate class commands. The Execute command has zero-bits in the four high order bits. The remainder of the command has the format required for the effective command to be executed.

STATUS AND CONDITION FLAGS

Internal Status

Eight internal status bits are provided to designate a particular internal interrupt condition. When any of the internal status bits are a 1-bit, the internal interrupt flag (bit 4) in file register 0 is also a 1-bit. This flag bit is tested by the microprogram to detect the presence of the internal interrupt condition. The internal status bits are entered via the A-but into the selected file register by a Control command, at which time the status bits are cleared. The eight internal status bits have the assignments given in Table 2.

TABLE 2. INTERNAL STATUS BITS

BIT	INTERNAL STATUS
	Console Interrupt
	(spare)
	Real-Time Clock Interrupt
	Memory Protect Error Interrupt
	Memory Parity Error Interrupt
	Memory Boundary Error Interrupt
	Console Halt Switch
	Power Fail/Restart Interrupt

All the internal status bits except the console interrupt and halt are associated with processor options and may be reassigned for special applications.

Condition Flags

The overflow, negative and zero conditions resulting from an operation involving the arithmetic/logic unit may be stored in file register 0 The condition flags are updated for command 7 and for commands 8, 9, B—F if bit 4 is a 1-bit. These condition flags can be tested by the microprogram for implementing various conditional operations. Definition of the condition flags is as follows:

Overflow - The Overflow condition flag stores the arithmetic overflow condition during an Add, Subtract or Copy command. Arithmetic overflow occurs when the carry out of the high order bit of the adder differs from the carry into the high order bit. The overflow condition flag stores the shifted off end bit during a Shift command.

Negative - The Negative condition flag stores the high order bit of the result on the A-bus.

Zero - The Zero condition flag stores the zero test condition of the result on the A-bus. When the link control (bit 7) of the operate commands is a 1-bit, the zero condition flag may not be set to indicate a zero result unless it is already set; it may be reset to indicate a non-zero result. This provides a linked zero test over multiple bytes of a variable byte operation.

COMMAND TIMING

Each command is executed in a single clock cycle time, although execution may be delayed because of core memory or read only storage operations. The system clock rate is 4.55 mHz, and the clock cycle 220 nanoseconds.

Memory Busy Delays

If the memory is busy, because of processor or DMA operation, at the time a Read or Write memory command or a command which will modify the M or N registers is to be executed, execution is delayed until the memory operation is completed. These commands are executed on the last clock of the memory half or full cycle. If a DMA request is pending at the time a Read or Write memory command is to be executed, execution is delayed to give the DMA memory priority.

Memory Data Delays

Operate class commands which select the contents of either the T register or its complement during the first two cycles of a processor memory read operation are executed during the third cycle of the read operation. This allows time for the accessed byte to be placed in the T register.

Read Only Storage Delays

An extra cycle is required for command execution because of the look ahead nature of the read only storage for the following conditions:

- Jump command
- Test If Zero command when a skip occurs
- Test If Not Zero command when a skip occurs
- Compare command when a skip occurs
- Operate class commands which have the L register designated

2.1.2 Literal Commands

a. LT LOAD T

11/19	Literal
15	0

0001	0001	Literal
15		0

0001	1001	Literal
15		0

The contents of the eight-bit literal field are placed in the T register. If the spare memory bit option is implemented in the machine, T_8 is cleared with code 11 and is set to a 1-bit with code 19. The condition flags and LINK register are not affected.

Affected: T

b. LM LOAD M

12	Literal
15	0

0001	0010	Literal
15		0

The contents of the eight-bit literal field are placed in the M register. The condition flags and LINK register are not affected.

Affected: M

c. LN LOAD N

13	Literal
15	0

0001	0011	Literal
15		0

The contents of the eight-bit literal field are placed in the N register and the M register is cleared. The condition flags and LINK register are not affected.

Affected: M, N

d. LU LOAD U

16	Literal
15	0

0001	0110	Literal
15		0

The contents of the eight-bit literal field are placed in the U register. The condition flags and LINK register are not affected.

Affected: U

e. LZ LOAD ZERO CONTROL

10	Literal
15	0

0001	0000	Literal
15		0

The eight bits of the literal field may be used to perform control functions for special applications. No control functions in this group are implemented in the standard machine.

f. LS LOAD SEVEN CONTROL

17		Literal
15		0

0001	0 11	Literal
15		0

The eight bits of the literal perform control functions as described below. If more than one bit of the literal field is on at a time, the last two digits of the command are determined by ORing the bits of the literal.

1700 - No Operation

1701 - Enable Serial Teletype: The serial teletype input is gated to bit 6 of file register 0, (see Table 1) for one clock cycle when the spare memory bit option is implemented.

1702 - Reset T_8: When the spare memory bit option is implemented, T_8 is cleared.

1F02 - Set T_8: When the spare memory bit option is implemented, T_8 is set to a 1-bit.

1704 - Disable External Interrupts: Recognition of external interrupts is inhibited.

1708 - Enable External Interrupts: Recognition of external interrupts is enabled.

1710 - Disable Real Time Clock: The real-time clock and interrupt are disabled.

1720 - Enable Real Time Clock: The real-time clock and interrupt are enabled.

1740 - Load Protect Bit: The content of bit 8 of the T register (T_7) is placed in the memory protect control storage for the memory page currently addressed by the contents of the M register.

1780 - Halt The processor is halted.

g. JP JUMP

14/15/1C/1D	Literal
15	0

0001	0100	Literal
15		0

0001	0101	Literal
15		0

0001	1100	Literal
15		0

0001	1101	Literal
15		0

The contents of the eight-bit literal are placed in the eight low order bits of the L register; the content of bit 8 is placed in L_8 and the content of bit 11 is placed in L_9. The location of the next command to be executed is at the address specified by the new contents of the L register. The execution time of the command is two cycles. The Jump operation codes for the four 256 word pages in read only storage are as follows:

14 - Jump to locations 000-0FF (page 0)
15 - Jump to locations 100-1FF (page 1)
1C - Jump to locations 200-2FF (page 2)
1D - Jump to locations 300-3FF (page 3)

Affected: L

h. LF LOAD FILE

2	f	Literal
15		0

0010	f	Literal
15		0

The contents of the eight-bit literal field are placed in the file register designated by f. File register 0 cannot be loaded by this command. The condition flags and LINK register are not affected.

Affected: f

i. AF ADD TO FILE

3	f	Literal
15		0

0011		Literal
15		0

The contents of the eight-bit literal field are added to the contents of the file register designated by f and the sum replaces the original contents of the file register. Subtraction is performed by placing the 2's complement of the number in the literal field. The condition flags and LINK register are not affected.

Affected: f

j. TZ TEST IF ZERO

4	f	Literal
15		0

0101	f	Literal
15		0

If, for all the 1-bits of the literal field, the corresponding bits of the file register designated by f are 0-bits, the next command is skipped. The condition flags, LINK register and file register are not affected. If the skip is taken, the timing of the command is two clock cycles.

Affected: L

k. TN TEST IF NOT ZERO

5	f	Literal
15		0

0101	f	Literal
15		0

If, for any bit of the literal field which is a 1-bit, the corresponding bit of the file register designated by f is also a 1-bit, the next command is skipped. The condition flags, LINK register and file register are not affected. If the skip is taken the timing of the command is two clock cycles.

Affected: L

1. CP COMPARE

6	f	Literal

15 0

0110	f	Literal

15 0

If the sum of the contents of the file register designated by f and the contents of the eight-bit literal is greater than 2^8-1, the next command is skipped. The condition flags, and file register are not affected. If the skip is taken the timing of the command is two clock cycles. The LINK stores the carry out of the adder.

Affected: LINK, L

2.1.3 Operate Commands

a. K CONTROL

7	f	c	*	r

15 0

0111	f	c	*	r

15 0

Control operations associated with special data flow and input/output are performed by this command. The exact operation is designated by the c field as explained below. Source data from the file, internal status, console sense switches or input bus are placed in the file register designated by f, if * is a 0-bit, and the register designated by r. The condition flags are unconditionally updated. Destination r = 7 is undefined for this command.

When c equals 8-F, the operations are associated with external input/output, and the three low order bits of c are placed in the I/O Control register. In the same operation, data can be moved from the designated file register or the input bus, as determined by the current contents of the I/O Control register, to the designated file or destination register. The data source is specified as follows:

I/O Control Register Mode	Source
0-3	Designated file register
4-7	Input bus

The operations designated by c are described below:

c		Operation	Explanation
0	-	No Operation	
1	-	Enter Sense Switches:	The status of the four console sense switches are placed in the four high order bits of the file register designated by f. The four low order bits are set to 1-bits.
2	-	Shift File Right 4:	The four high order bits of the file register designated by f are placed in four low order bits of the file register. The four high order bits are set to 1-bits.
4	-	Enter Internal Status:	The eight internal status bits are placed in the file register designated by f.
7	-	Enter Console Switches:	The contents of the eight low order console command switches are ANDed with the eight low order bits of the next command. File register 0 must be selected to prevent any modification of the file during the execution of the Control command. The command preceding this operation must not cause a read only storage delay.
8	-	Clear I/O Mode:	The I/O Control register is cleared. Data from the designated file or Input bus can be transferred to the designated file register and register (r)

9-F - Set I/O Mode: The I/O Control register is loaded with the three low order bits of c placing it in one of seven I/O bus or serial teletype modes. These modes are described in Table 3. Data from the designated file or Input bus can be transferred to a designated file register and register (r).

Affected: F, I/O Control, Condition Flags, r.

TABLE 3. BYTE I/O CONTROL MODES

Mode	c-field	Control Activity
0	1000	None
1	1001	Control Output (COXX/)
2	1010	Data Output (DOXX/)
3	1011	Space Serial Teletype
4	1100	Spare
5	1101	I/O Acknowledge (IOAK/)
6	1110	Data Input (DIXX/)
7	1111	Spare

b. A ADD

8	f	c	*	r

15 0

1000	f	c	*	r

0

The selected operand is added to the contents of the file register designated by f. The sum is placed in the file register (f), if * is a 0-bit, and in the register designated by r. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result and modification of the condition flags as follows:

c-bits 7 6 5 4	Operation
1 x x x	Link Control: The content of LINK is added to the sum. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Add One: One is added to the sum.
x x 1 x	Select T: The contents of the T register or the input bus are selected as the operand. If the T register is not selected, the operand is zero.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, LINK, Condition Flags, r

c. S SUBTRACT

9	f	c	*	r

15 ... 0

1001	f	c	*	r

15 ... 0

The complement of the selected operand plus one is added to the contents of the file register designated by f. The difference is placed in the file register (f) if * is a 0-bit, and in the register designated by r. The result is a 2's complement subtraction. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result, and modification of the condition flags as follows:

c-bits 7 6 5 4	Operation
1 x x x	Link Control: The content of LINK is added to the sum. Selection of the LINK inhibits the automatic addition of one. The zero condition flag cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Inhibit Add One: If Link Control is not selected, one is automatically added to the result to produce a 2's complement subtraction. This control bit inhibits this addition, providing a 1's complement subtraction.
x x 1 x	Select T: The complement of the contents of the T register are selected as the operand. If not selected, the operand consists of a 1-bit in each bit position.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, LINK, Condition Flags, r

d. R READ MEMORY W WRITE MEMORY

A	f	c	*	r

15 0

1010	f	c	*	r

15 0

The contents of the file register designated by f is unaltered, incremented, or decremented as controlled by the c field. The result is placed in the file register (f) if * is a 0-bit, and in the register designated by r. At the same time, a read (R) or write (W) memory operation is initiated as controlled by bit 4. If the operation is a memory read, the T register is cleared and the accessed data is set into the T register after two clock cycle times. Data to be written into memory must be placed in the T register before the write memory command, if the operation is a half cycle write, and by the first clock cycle time after the write memory command on a full cycle write. The condition flags and

LINK are not affected. Execution of the memory command is delayed if the memory is in a busy condition from a previous R or W command or DMA operation.

The bits of the c field control the transfer of data from the file register and the type of memory operation as follows:

c-bits 7 6 5 4	Operation
0 0 x x	Transfer: The contents of the file register are transferred unaltered.
0 1 x x	Decrement: The contents of the file register minus one are routed as specified. If the M register is selected as the destination and the content of LINK is a 1-bit, the contents of the file register are transferred without being decremented. This provides a decrement with link control when M is the destination.
1 0 x x	Add Link: The content of LINK is added to the contents of the file register, and the sum is transferred as specified.
1 1 x x	Increment: The contents of the file register plus one are transferred as specified.
x x 1 x	Half Cycle: If this bit is a 1-bit, a half cycle memory operation is performed; otherwise a full cycle operation is selected.
x x x 1	Write: If this bit is a 1-bit, a write memory operation is performed; otherwise a read operation is selected.

Affected: F, Memory, r

e. C COPY

B	f	c	*	r
15				0

1011	f	c	*	r
15				0

The selected operand is placed in the file register designated by f, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand, incrementing the operand, and modification of condition flags as follows:

c bits 7 6 5 4	Operation
1 x x x	Link Control: The content of LINK is added to the sum. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Add One: One is added to the sum.
x x 1 x	Select T: The contents of the T register or Input bus are selected as the operand. If the T register is not selected, the operand is zero.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

f. O OR

C	f	c	*	r

15 ... 0

1100	f	c	*	r

15 ... 0

The selected operand is logically inclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c-bits 7 6 5 4	Operation
1 x x x	Link Control: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Select Complement T: The complement of the contents of the T register is selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	Select T: The Contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

g. X EXCLUSIVE OR

D	f	c	*	r

15 ... 0

1101	f	c	*	r

15 ... 0

The selected operand is logically exclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c bits 7 6 5 4	Operation
1 x x x	Link Control: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Select Complement T: The complement of the contents of the T register are selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	Select T: The contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, Condition flags, r

h. N AND

E	f	c	*	r

15 0

1110	f	c	*	r

15 0

The selected operand is logically ANDed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c-bits 7 6 5 4	Operation
1 x x x	Link Control: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Select Complement T: The complement of the contents of the T register are selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	Select T: The contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

i. H SHIFT

F	f	c	*	r
15				0

1111	f	c	*	r
15				0

The contents of the file register designated by f is shifted left or right one bit position and placed in the file register, if * is a 0-bit, and in the register designated by r. The high order or low order bit which is shifted off is placed in LINK and in the overflow flag if the modify condition flag is selected. The c field controls the direction of shift, entry of an end bit, and modification of the condition flag as follows:

c-bits 7 6 5 4	Operation
1 x x x	Link Control: The content of the LINK is inserted into the vacated low order or high order bit position. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	Insert One: A 1-bit is unconditionally inserted into the vacated low order or high order bit position; otherwise a 0-bit is inserted unless the contents of LINK is selected.
x x 1 x	Shift Right: If bit 5 is a 1-bit, the operation is a right shift; otherwise a left shift is performed.
x x x 1	Modify Condition Flags: The condition flags are modified by execution of the command. The content of the bit shifted out is placed in the overflow flag.

Affected: F, LINK Condition Flags, r

2.1.4 Execute Command

E EXECUTE

0	
15	0

The eight-bit contents of the U register are ORed with the eight high order bits of the Execute command to form an effective command. This provides a means of partially modifying the contents of a read only storage location. The ORing is performed before the output of the read only storage is gated into the R register. The meaning of bits present in positions 0-11 is dependent upon the desired effective operation code after the modification. Due to the look ahead feature of the read only storage, the new contents of the U register is not available until after one machine cycle following the transfer of data to it.

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter presents both a general and detailed functional description of the computer. The overall machine is initially functionally described followed by details related to each functional assembly.

3.2 GENERAL BLOCK DIAGRAM

The general block diagram for the computer is given in Figure 16. A description of the elements comprising the block diagram follows:

3.2.1 M Register

The eight bit M register contains the eight high order bits of the processor memory address. This register is gated onto the memory address bus at all times except when a DMA operation is in process.

3.2.2 N Register

The eight bit N register contains the eight low order bits of the processor memory address. This register is gated onto the memory address bus at all times except when a DMA memory operation is in progress.

3.2.3 Memory Buses

The memory data and address buses communicate between the four memory modules, the processor and the optional DMA hardware. Either the processor or the DMA may operate with the memory, with the DMA having top priority.

3.2.4 DMA

The direct memory access (DMA) option allows for direct connection to the memory address, data and control buses.

3.2.5 Core Memory

The magnetic core memory is organized into two board pluggable modules of 4096 bytes. The memory is addressed at the byte level and each byte contains 8 or 9 bits.

The memory is operated in read/write and full/half cycle operations. The full cycle memory timing is 1.1 microseconds (five 220nsec clock cycles); the half-cycle timing in the system is three clock cycles (660ns). For a read operation, the accessed data is placed in the T register two clock cycles after the start of the memory operation. Full cycle regeneration of the data in the memory does not require the use of the T register and T may be modified by the microprogram before completion of the restore part of the cycle.

3.2.6 T Register

The eight bit T register serves as the operand register for most of the operate class commands and as a buffer register for output and memory operations. The T register is expanded to nine bits when the spare memory bit option is included in the processor. Both the true and complement output of the T register can be gated to the B bus as an operand. When both the contents of T and its complement are selected as operands, the effective operand is all one bits; while if neither is selected, the operand is all 0-bits.

3.2.7 B Bus

The four inputs to the B bus are each enabled by their respective control terms. The B bus true outputs become inputs to the Arithmetic/Logic Unit.

3.2.8 Arithmetic/Logic Unit

The Arithmetic/Logic Unit (ALU) performs all manipulation of data including: addition, logical AND, logical OR, logical exclusive OR, and one bit left and right shifts. The output of the ALU is the A bus.

3.2.9 A Bus

The A bus output becomes the input to the file logic and the M, N, T, U and L registers.

3.2.10 L Register

The ten bit L register is the machine's program counter and contains the read only storage address of the next command to be executed, unless altered by a jump command. The eight low order bits of the L register are a counter which is incremented by one at each clock time when the processor is running unless there is a command execution delay imposed. The two high order bits serve as an ROS address counter.

3.2.11 Read Only Storage (ROS)

The read only storage (ROS) provides the storage for commands and constants of the microprogram. Its output is gated into the R register where it controls the operation of the machine at the next clock time.

3.2.12 R Bus

The R bus allows for modification of the microcommand by the U register output and enables microprogram control by either the ROS or operator command switch inputs.

3.2.13 R Register

The 16 bit R register holds the microcommand being executed. Its output is decoded and controls the operation of the processor at each clock time.

3.2.14 Command Decoding and Control

The command decoding and control logic is used to decode the microcommand and control those machine functions necessary to execute the command.

3.2.15 File Registers

The file consists of 16 eight-bit operational registers. All commands except the load register command specify a file register to be operated on or to provide an operand. All file registers are functionally identical except for file register 0 which contains eight flags and cannot be used for general storage.

3.2.16 I/O Control Register

The three-bit I/O control register generates the control signals for the I/O bus by decoding the contents of the R register. It is loaded and cleared by a control command and, therefore, the timing of I/O control signals is under command control. There are three output modes and four input modes. The high order bit of the register is the input flag. When this bit is a 1 bit, the input bus is substituted for the T register when it is selected and the input bus is the source of data when executing an external I/O control command.

3.2.17 Link Register

The one-bit link register holds the adder's high order carry from Add, Subtract, and Compare commands and the bit shifted off in the execution of the shift command.

3.2.18 U Register

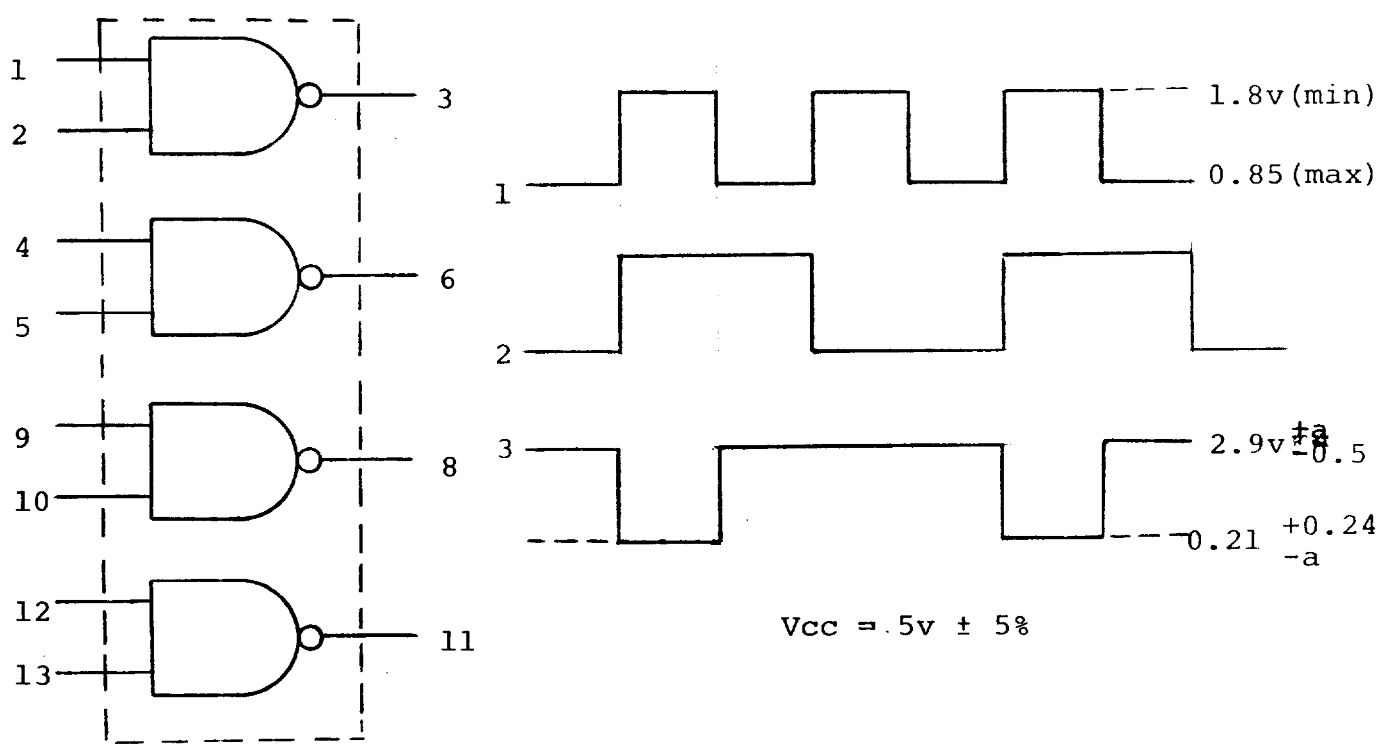
The eight-bit U register is used to modify the output of the read only storage. For commands with 0's in the four high order bits or 1's in bit 15 and the three low order bits, the contents of the U register is inclusive OR'ed with the eight high order bits of the ROS output as it is gated into the R register. This allows for dynamic modification and changing of operation codes and file register designators.

3.3 LOGIC ELEMENTS

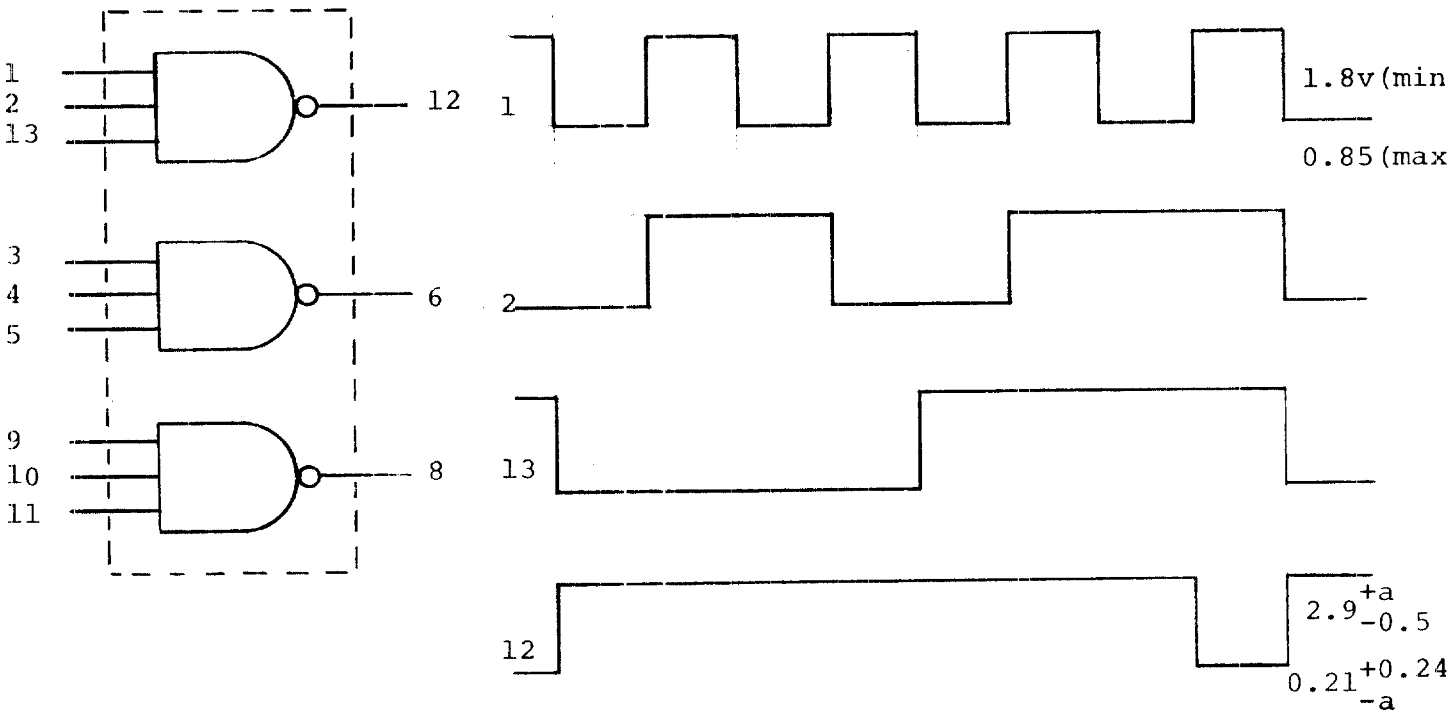
This section describes the logic elements used in the computer and presents the truth tables, voltage levels and timing diagrams associated with each element.

9000 series gates are active low level output AND gates commonly known as NAND gates. The gates are designed to provide low drive capability and good immunity to cross talk. The output impedance in the low state is approximately 10 ohms and, in the high state, approximately 20 ohms.

3.3.1 9002 Gate Element (NAND)

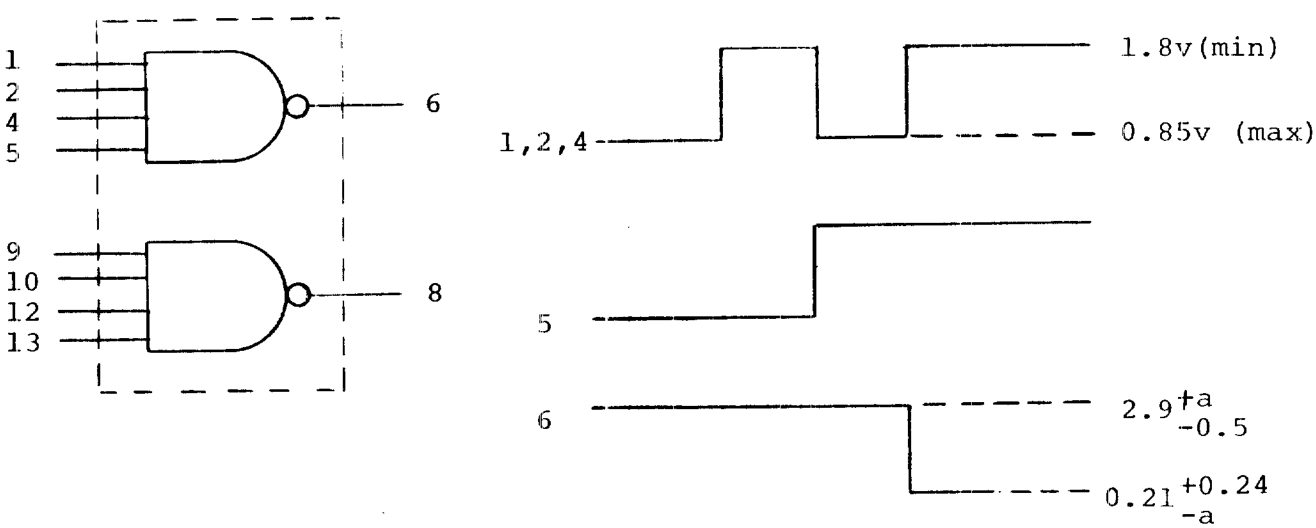


3.3.2 <u>9003 Gate Element (NAND)</u>

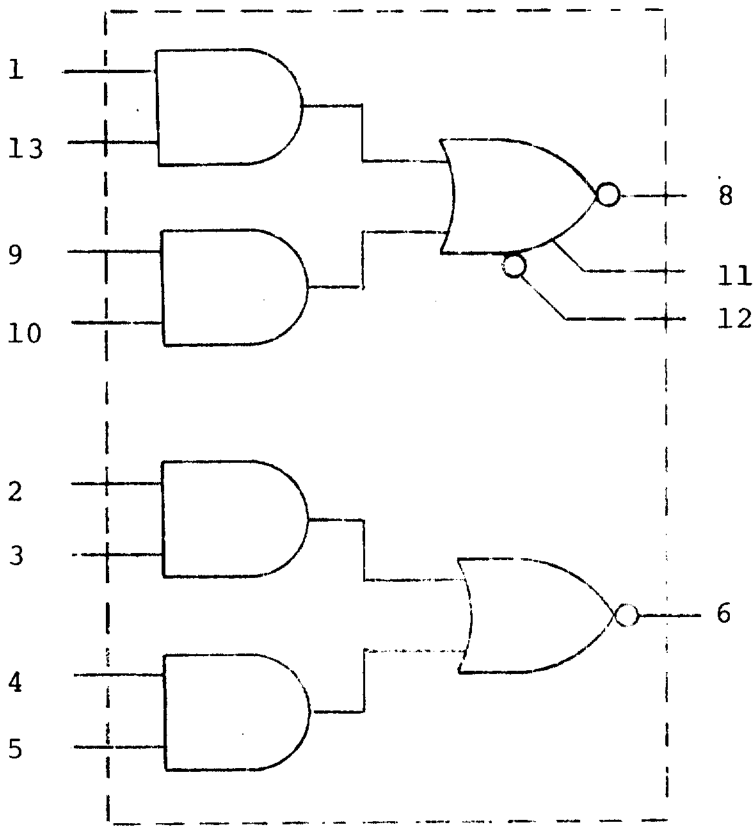


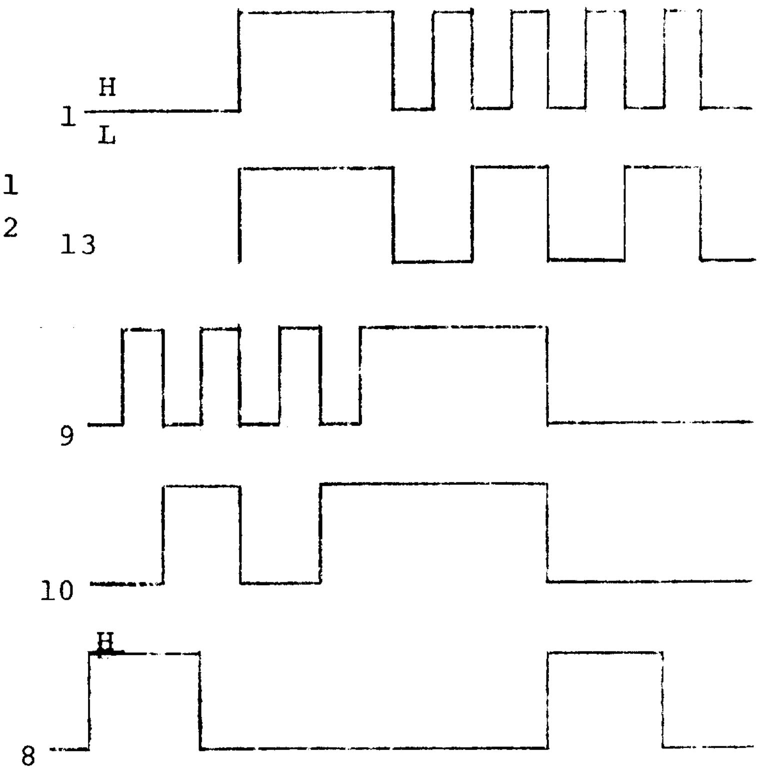
Vcc = 5.0v ± 5%

3.3.3 <u>9004 Gate Element (NAND)</u>



3.3.4 9005 Gate Element (AND/NOR)

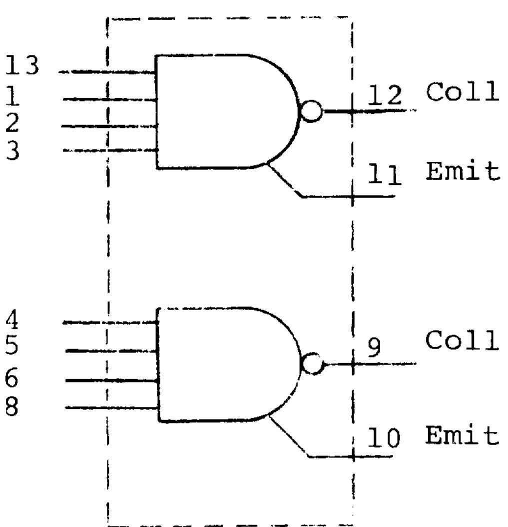




Input
H=1.8v(min)
L=0.85(max)
Vcc=5.0v±5%

Ouput
H=2.4v(min)
L=0.45(max)

3.3.5 9006 Gate Element (NOR)

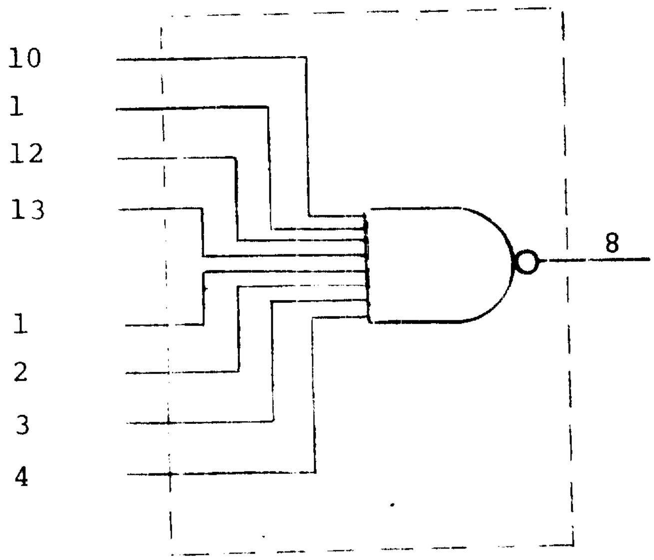


Term No.	Voltage Levels															
13	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Input
H=1.8v(min)
L=0.85v(max)

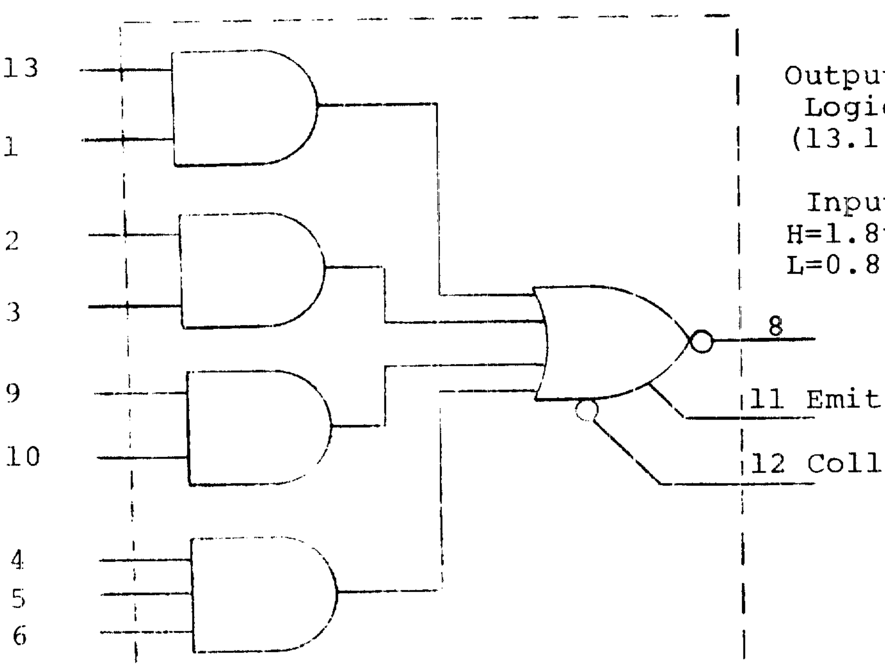
Output
H=2.4v(min)
L=0.45v(max)

3.3.6 9007 Gate Element (NAND)



Input	Output (2)
All inputs H	L
At least one input H	H
At least one input L	H
All inputs L	H
L= H=1.8v(min) L=0.85v(max)	H=2.4v(min) L=0.45v(max)

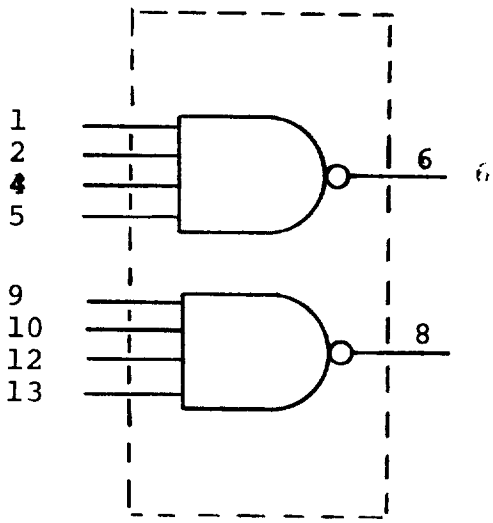
3.3.7 9008 Gate Element (AND/NOR)



Output (8) is L under the following Logic
(13.1)+(2.3)+(9.10)+(4.5.6)

Input	Output
H=1.8v(min)	H=2.4v(min)
L=0.85v(max)	L=0.45(max)

3.3.8 9009 Gate Element

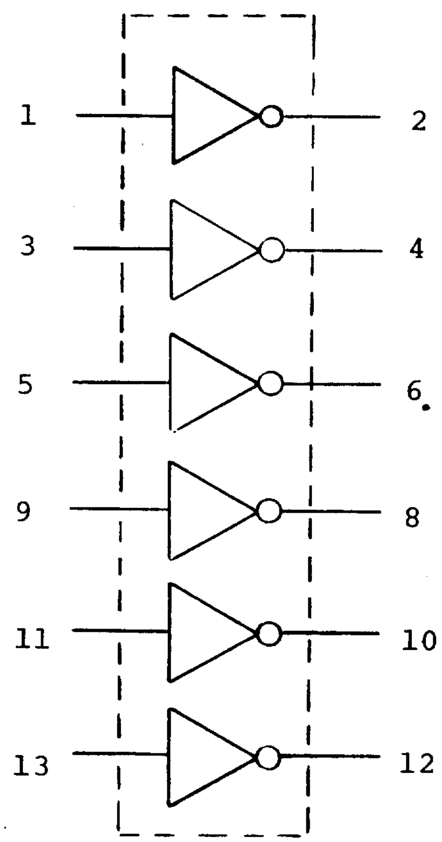


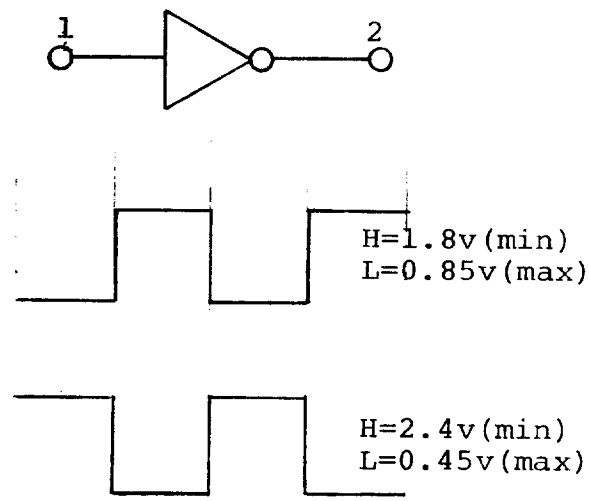
Term No.	Voltage Levels															
1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
4	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
5	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Input
H=1.8v(min)
L=0.85v(max)

Output
H=2.4v(min)
L=0.45v(max)

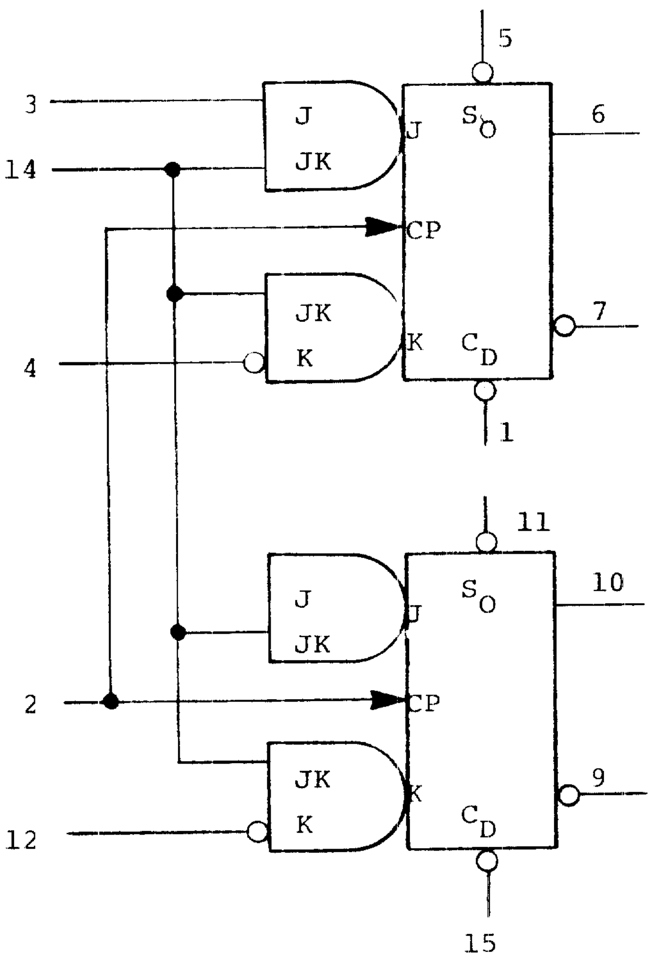
3.3.9 9016 Hex Inverter





3.3.10 9022 Dual JK Flip-Flop

The master-slave design of this flip flop offers the advantage of a DC threshold on the clock input initiating the transition of the outputs so that careful control of clock pulse rise and fall times is not required. Data is accepted on the master while the clock is in the low state. Transfer from the master to the slave occurs on the low to high transition of the clock When the clock is high, the J and K inputs are inhibited



*L Input does not go high at any time clock is low
*H Input is high at some time while clock is low
X Doesn't care

Synchronous Operation

Before Clock Outputs		Before Clock Inputs		Outputs after Clock	
One	Zero	J	K	One	Zero
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

Asynchronous Operation

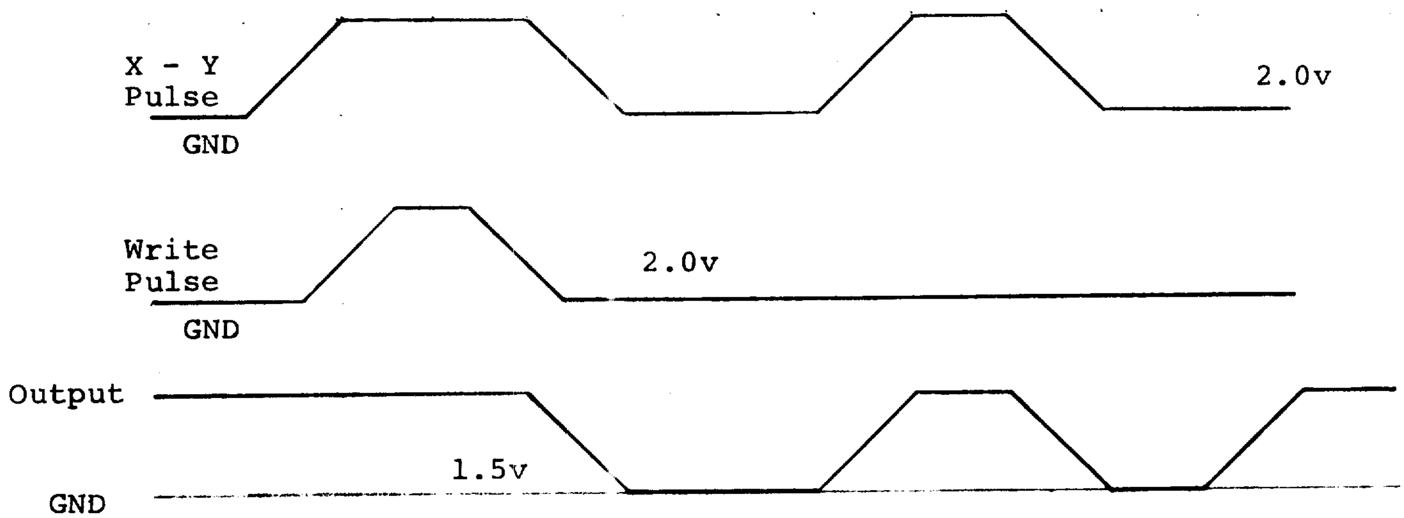
Inputs		Outputs	
S_D	C_D	One	Zero
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

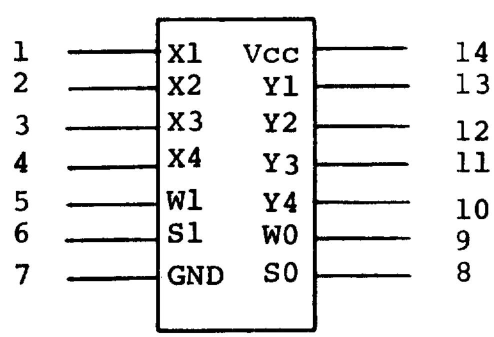
Input
H=1.8v(min)
L=0.85v(max)

Output
H=2.4v(min)
L=0.45v(max)

3.3.11 9033 16-Bit Memory Cell

This 16-bit memory cell consists of 16 R-S flip flops arranged in an addressable four-by-four matrix. The denied bit location is selected by raising the coincident X-Y address lines to a logic "H" level and holding the non-selected address lines at logic "L" level. Four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals.





If addressed bit location contains a 1 S_1 will be low, S_0 will be high.

If addressed bit location contains a 0 S_1 will be high, S_0 will be low.

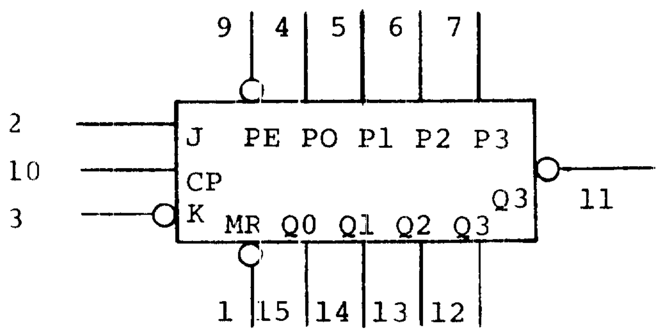
To write a 1, address bit location W_1 input raised to high level

To write a 0, address bit location W_0 input raised to high level

S - Sense Output
W - Write Input
X & Y - Address

3.3.12 9300 4-Bit Shift Register

The 9300 is a 4-bit shift register providing a JK input to the first flip flop in the register. There is no restriction on the activity of the J or K inputs for logical operation---except for the set up and release time requirements. Parallel inputs for all four stages are provided. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.



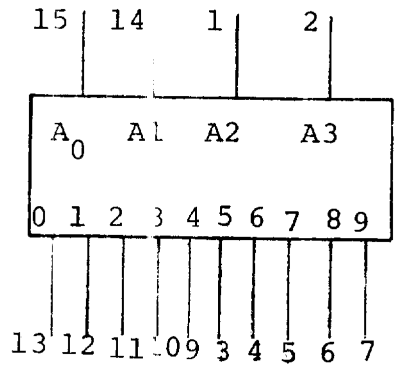
Truth Table for Serial Entry
PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock

J	K	Q0 at tn + 1
L	L	L
L	H	Q_0 at t_n (no charge)
H	L	Q_0 at t_n (toggles)
H	H	H

3.3.13 9301 One of Ten Decoder

This multipurpose decoder will accept four inputs and provide ten mutually exclusive outputs.

Input
H=1.7v(min)
L=0.8v(max)



Output
H=2.4v(min)
L=0.4v(max)

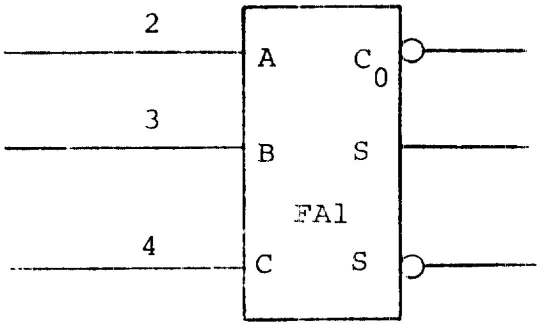
Truth Table

Input				Output									
A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

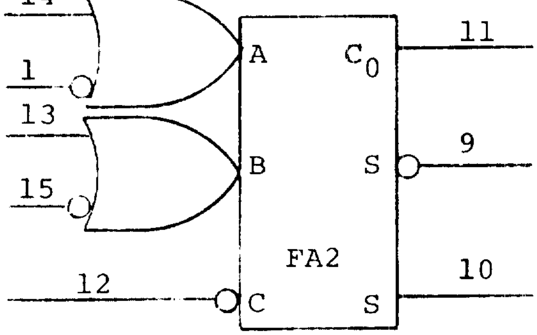
3.3.14 9304 Full Adder

The 9304 consists of two independent, high speed, binary full adders. This design allows a minimum carry propogation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs for the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used.

9304 Full Adder



Adder 1



Adder 2

ADDER 2							
INPUTS					OUTPUTS		
C	B_1	A_1	$\bar{B}_2$	$\bar{A}_2$	C_o	S	$\bar{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

Truth Table
9304

Adder 1					
INPUTS			OUTPUTS		
C	B	A	C_0	S	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

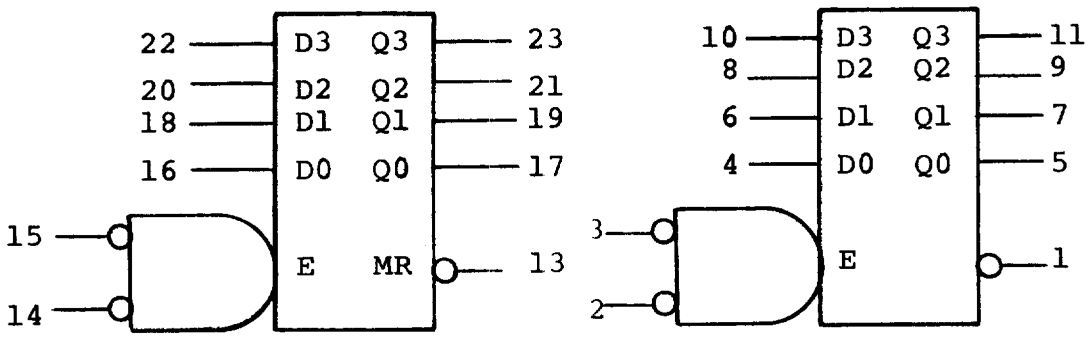
Inputs	Outputs
H=1.8v(min)	H=2.4V (min)
L=0.85v(max)	L=0.45V (max)

V_{CC} = 5.0V ±5%

3.3.15 9308 4-Bit Latch

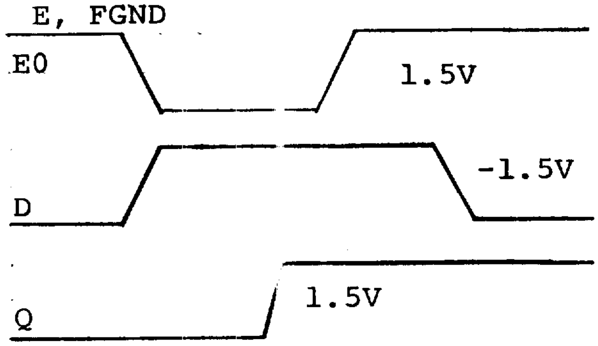
To enter data into the latch, both enable inputs are low and the output of the latch follows the inputs. If either enable input goes high, data present in the latch is held in the latch. MR forces the outputs of all latches low when MR is low.

4-Bit Latch



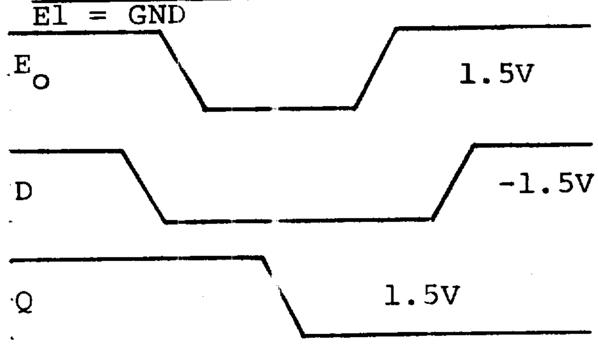
Storing a One

E, FGND



Storing a Zero

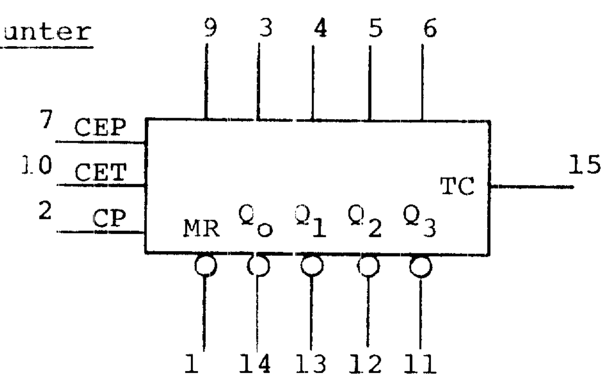
E1 = GND



3.3.16 4-Bit Binary Counter

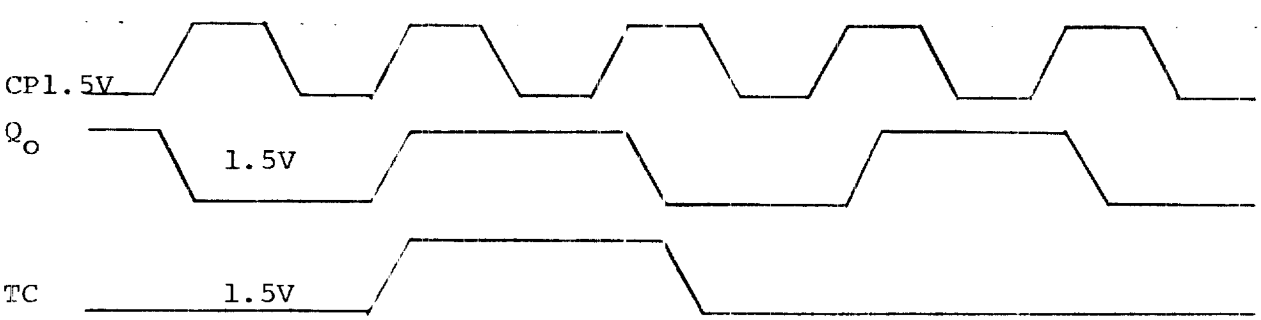
The 9316 is a high-speed synchronous 4-bit binary decade counter. It is synchronously presetable. A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel so the synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and S inputs. During the low-to-high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed, both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state; secondly, the data inputs (R and S) are enabled so that new data can enter the master.

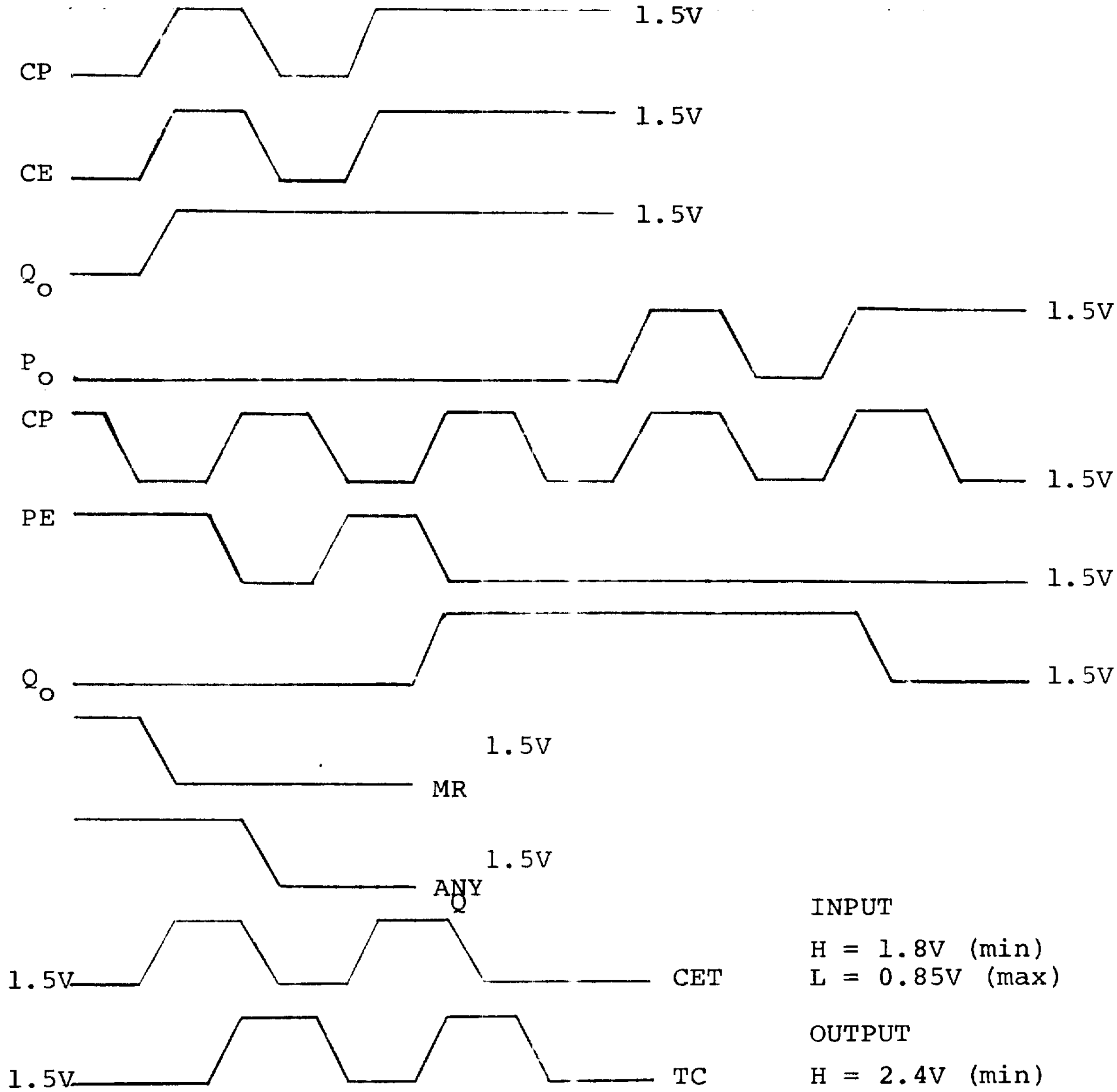
9316 4-Bit Binary Counter



CE (Count Enable) = CEP = CET

$TC = CET \cdot Q_o \cdot Q_1 \cdot Q_2 \cdot Q_3$





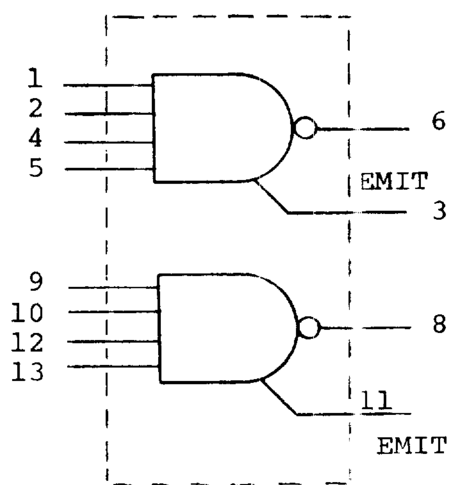
INPUT

H = 1.8V (min)
L = 0.85V (max)

OUTPUT

H = 2.4V (min)
L = 0.45V (max)

3.3.17 <u>9944 Gate Element (NAND)</u>



INPUT

H = 1.9V (min)
L = 1.1V (max)

OUTPUT

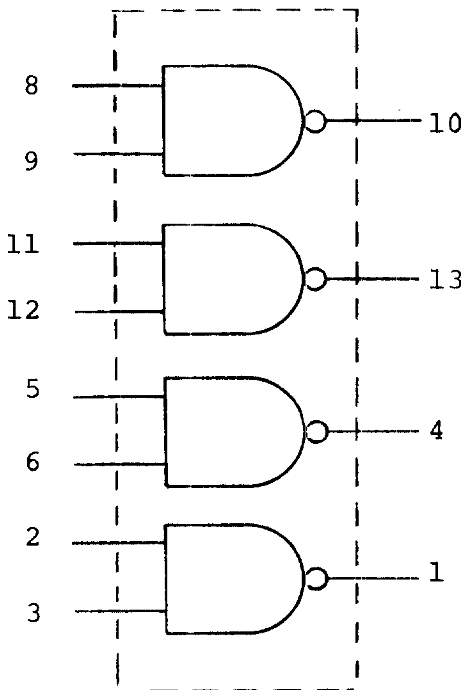
H = 2.6V (min)
L = 0.4V (max)

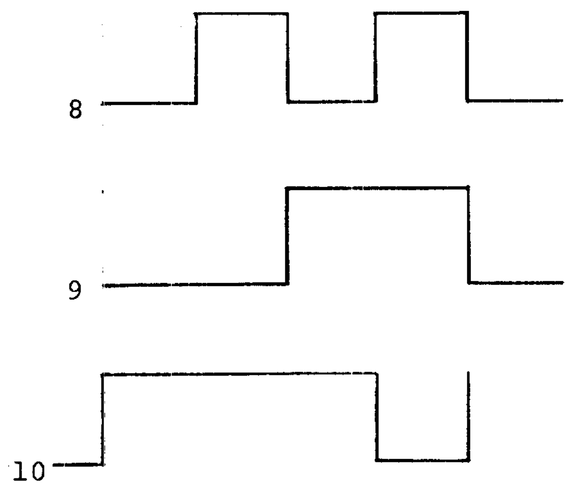
Logic similar to 9004 or 9006.

3.3.18 7401 Gate Element

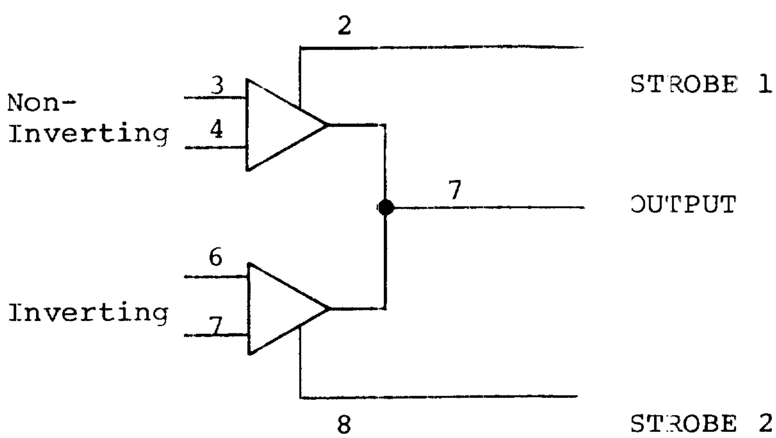
INPUT
H = 2V (min)
L = 0.8V (max)

OUTPUT
H =
L = 0.4V (max)





3.3.19 2711 Dual Differential Comparator



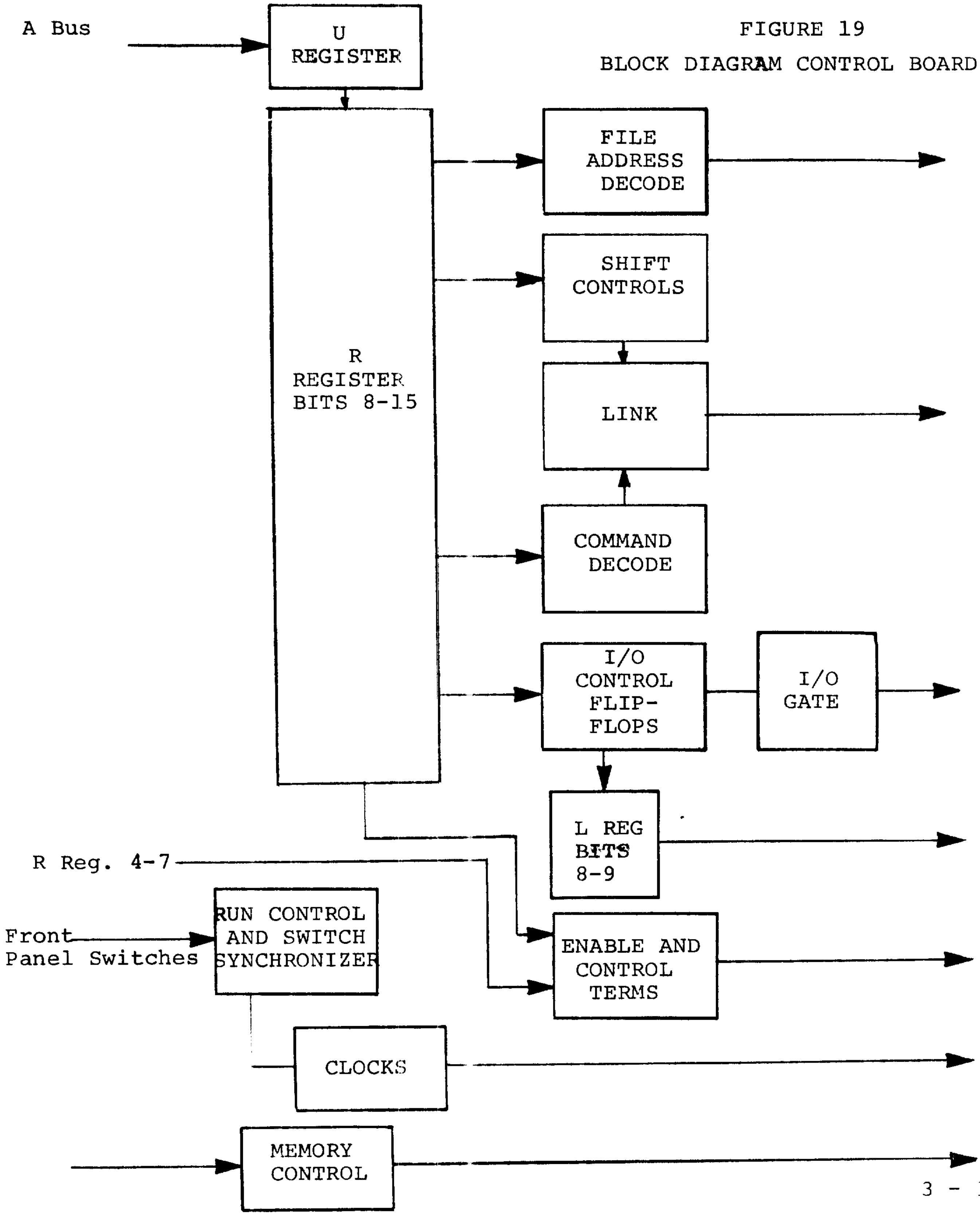
Input Voltage Range ($V^- = -7.0V$)
±.5V (min)
Differential Input Voltage Range
±5V (min)
Positive Output Level
5V (min)

3.4 <u>CONTROL BOARD</u>

The block diagram for the control board is shown in Figure 19.

FIGURE 19

BLOCK DIAGRAM CONTROL BOARD



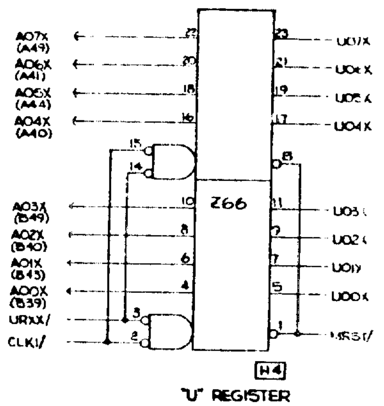


FIGURE 20

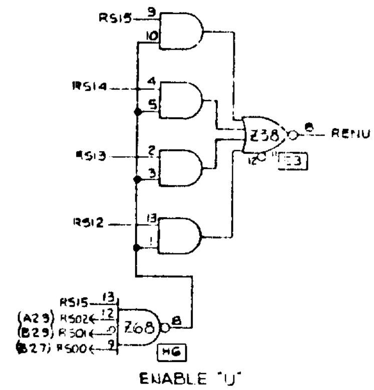


FIGURE 21

3.4.1 <u>U and R Registers</u>

The U register shown in Figure 20 is mechanized by a dual latch element (Z66). Its data inputs are provided by the A bus and it is clocked by CLK1/ and enabled by URXX/.

The input for the 8 high order bits to the R register is the AND-OR'ed combination of the Read Only Storage data bus (bits 8-15) and the U register. The U register is OR'ed into the R register under control of RENU, generated by the logic shown in Figure 21. The console control command switches are collector OR'ed into the read only storage data bus by gates Z57 and Z65 under control of CPEN (Control Panel Enable). The R register shown in Figure 22 is clocked by CLK6/. The master enable, RJKX, R Register Clock Inhibit, disables the clocking during the periods of command execution delay.

The RENU term allows the contents of the U register to be gated into the input of the R register (bits 8-15) along with the output of the read only storage. This control applies for the execute command and for the commands which have bit 0-2 set to a 1.

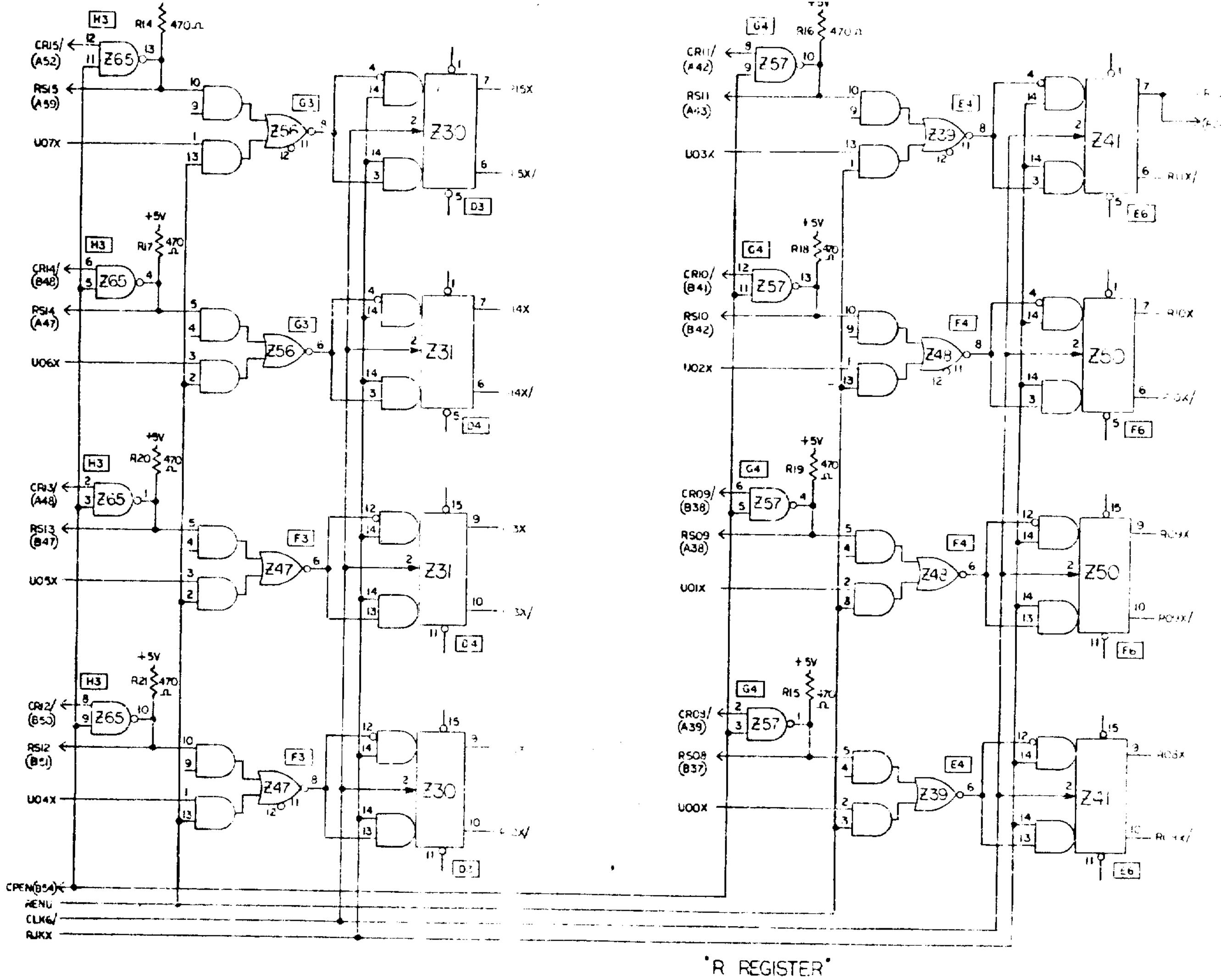


FIGURE 22

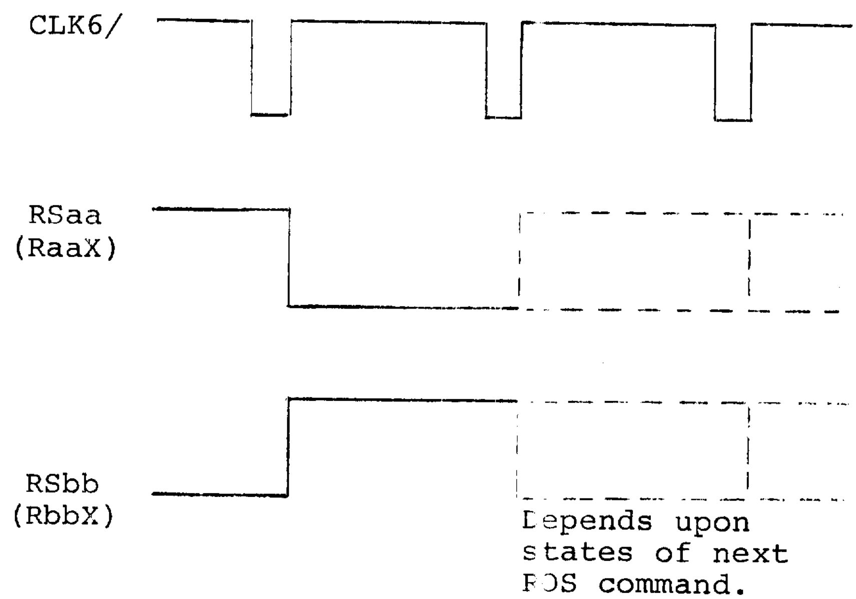
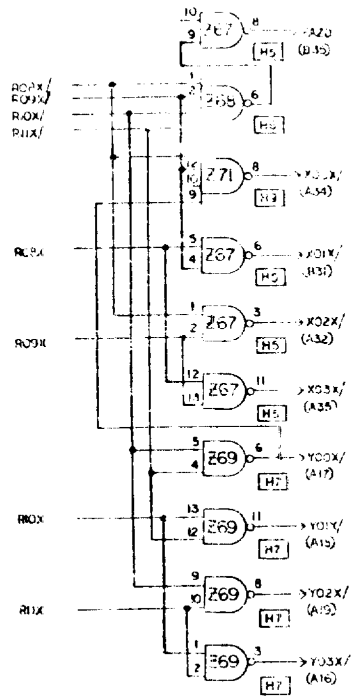


FIGURE 23

The timing signals associated with bits 8-15 of the R register operation are shown in Figure 23.



FILE ADDRESS DECODE

FIGURE 24

3.4.2 File Register

Bits 8-11 of the R register are decoded into 8 file addressing signals shown in Figure 24. R10X and R11X are decoded in Z69 to form Y00X/, Y01X/, Y02X/ and Y03X/. R08X and R09X are decoded to form X00X/, X01X/, X02X/ and X03X/. The X00X/ signal is inhibited if Y00X is true so that no file register will be selected when the file designator is 0. The term FAZD is true when file register 0 is selected. This signal enables the file register 0 inputs to be collector OR'ed into the file elements on the data boards. The truth table for the file address decode is given in Table 4.

R11X	R10X	R09X	R08X	FAZD	X00X/	X01X/	X02X/	X03X/	Y00X/	Y01X/	Y02X/	Y03X/
0	0	0	0	1	1	1	1	1	0	1	1	1
0	0	0	1	0	1	0	1	1	0	1	1	1
0	0	1	0	0	1	1	0	1	0	1	1	1
0	0	1	1	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	1	1	1	0	1	1
0	1	0	1	0	1	0	1	1	1	0	1	1
0	1	1	0	0	1	1	0	1	1	0	1	1
0	1	1	1	0	1	1	1	0	1	0	1	1
1	0	0	0	0	0	1	1	1	1	1	0	1
1	0	0	1	0	1	0	1	1	1	1	0	1
1	0	1	0	0	1	1	0	1	1	1	0	1
1	0	1	1	0	1	1	1	0	1	1	0	1
1	1	0	0	0	0	1	1	1	1	1	1	0
1	1	0	1	0	1	0	1	1	1	1	1	0
1	1	1	0	0	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	0	1	1	1	0

TABLE 4

TRUTH TABLE FOR FILE ADDRESS DECODE

3.4.3 Control Terms

The term ANDX is the control term enabling the ADD function to the A bus. ANDX is generated on the control board (logic shown in Figure 25) and is used as a control term for the file logic output F--X and the B bus output B--X on Data Boards 1 and 2. ANDX is high when any of the inputs to Z55 are low, which occur under the following conditions:

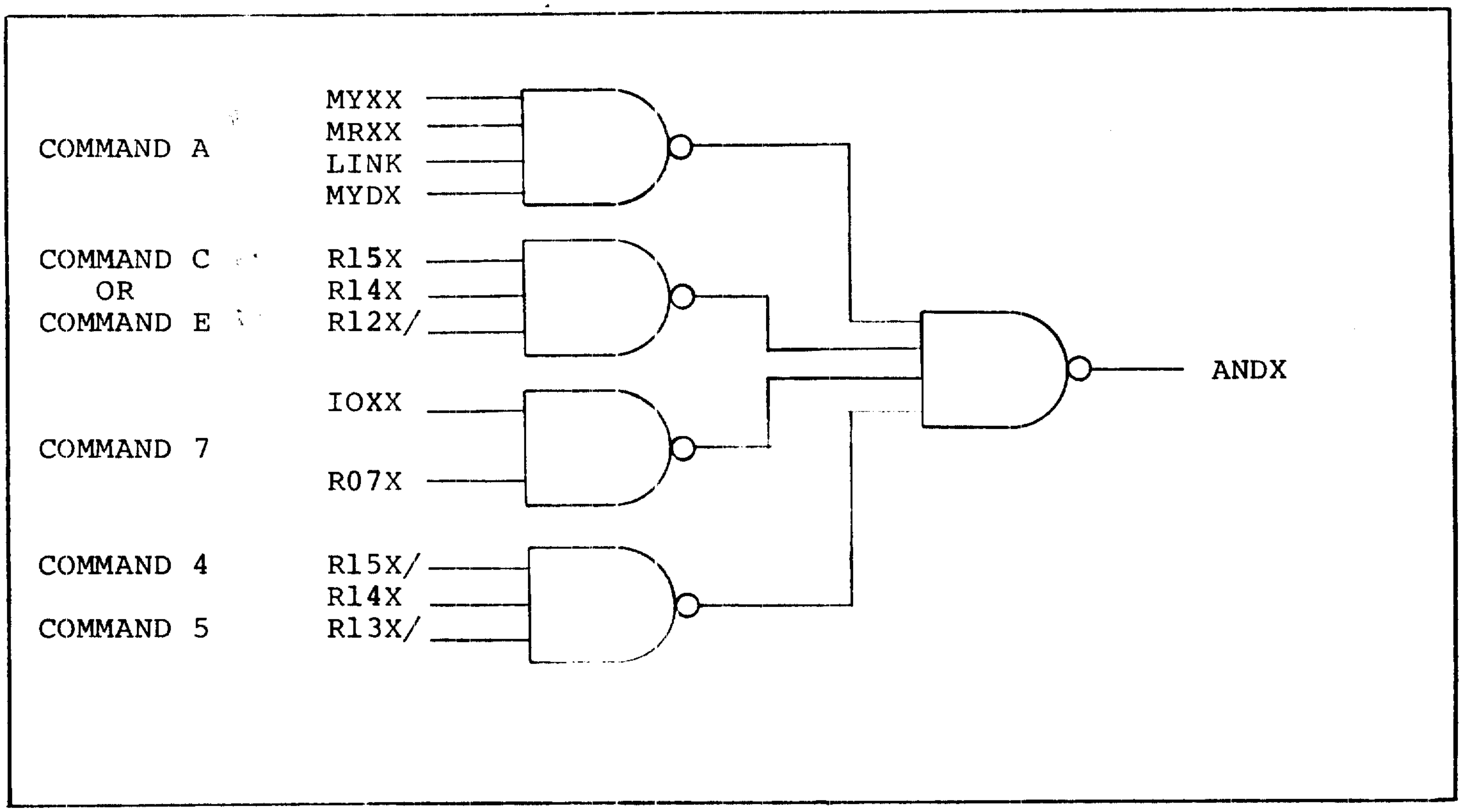


FIGURE 25

LOGIC FOR ANDX CONTROL SIGNALS

(1) MYXX is generated at the output of the command decoder during a read memory operation (Command A). BENR/ is enabled and allows R00X/, R01X/ and R02X/ to set the conditions for DES 0, 1 and 2 which establishes the register designator into which the contents of the

file designated in the command will be placed. When bits 6 and 7 are 1 and 0 respectively (MYDX is generated), and LINK is a 1-bit, the contents of the file register minus one are routed as specified.

(2) Command D (OR function) and Command E (AND function will result in generation of ANDX.

(3) Command 7, to clear or set I/O mode, will generate the ANDX control term by logical combination of IOXX generated at the command decoder with R07X.

(4) Command 4 (test if zero) and Command 5 (test if not zero) will result in generating ANDX.

Typical timing signal associated with control of ANDX is shown in Figure 26.

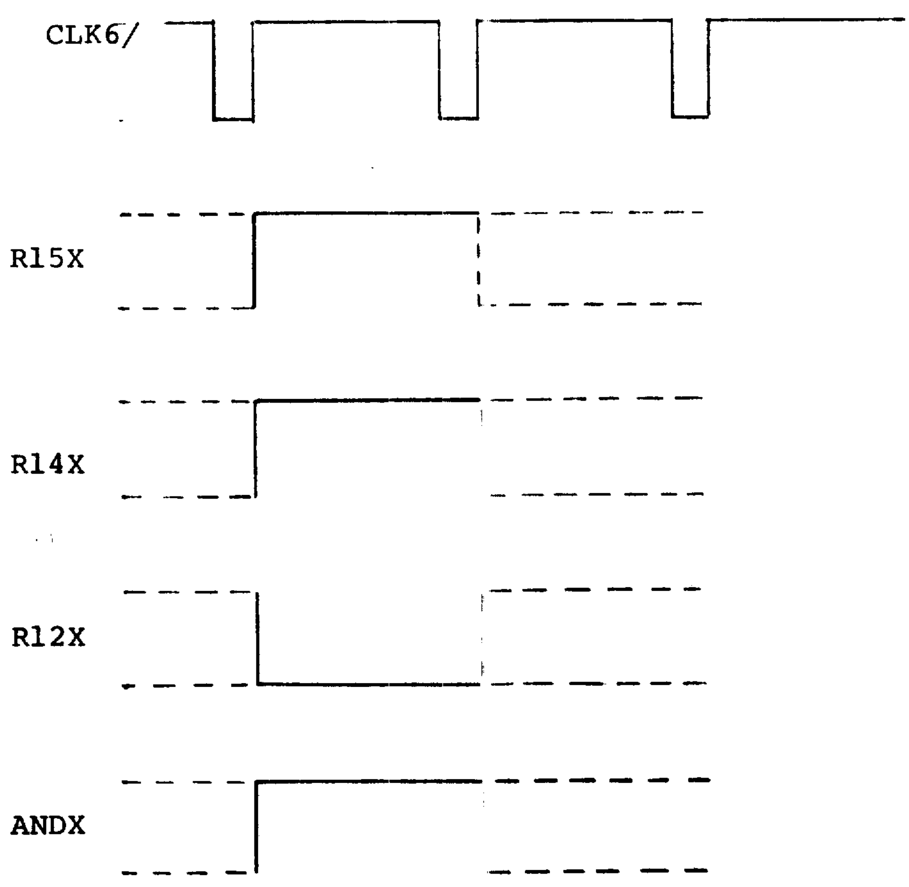


FIGURE 26

TIMING DIAGRAM FOR ANDX CONTROL TERM

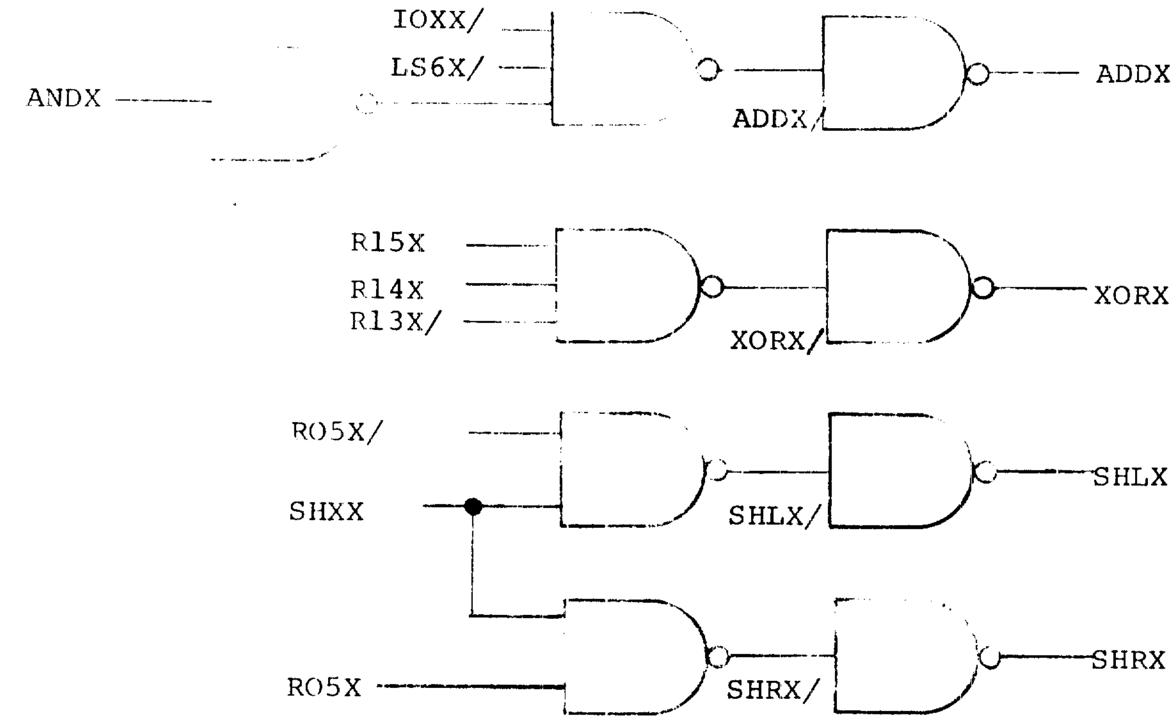


FIGURE 27

LOGIC FOR ADDX, XORX, SHLX AND SHRX

Timing diagrams for control terms ADDX, the adder to A bus enable, and XORX, the exclusive OR function to the A bus, are shown in Figure 28.

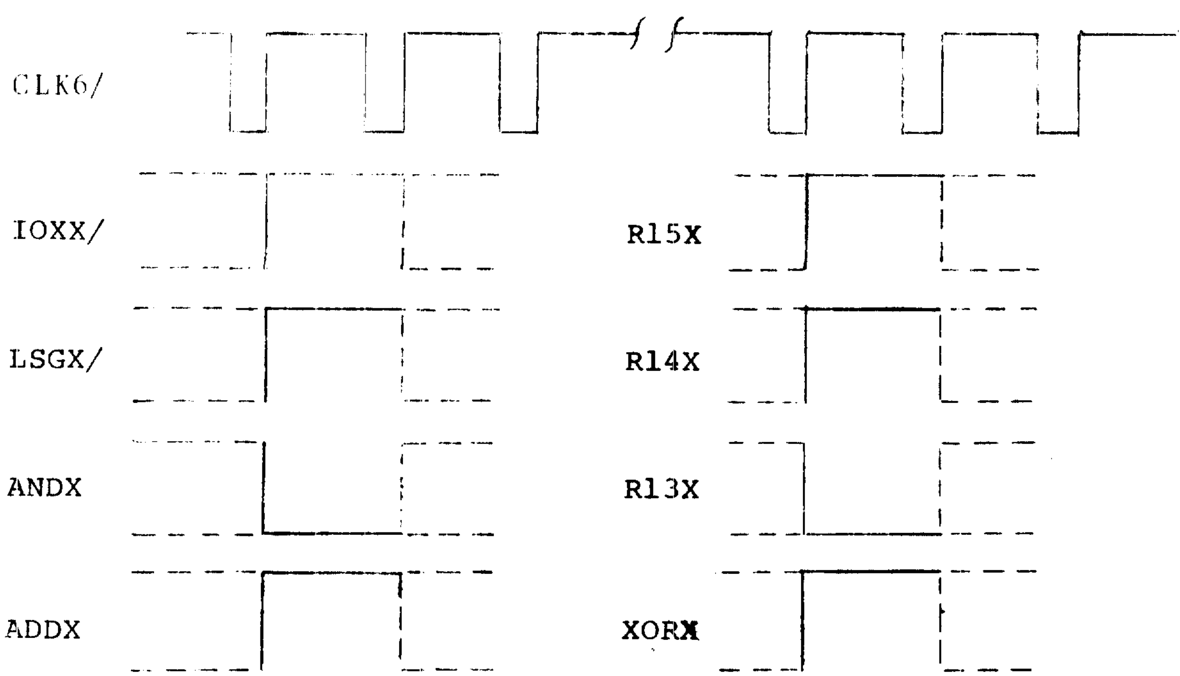


FIGURE 28

TIMING DIAGRAM FOR ADDX AND XORX

Similarly, the timing for the A bus shift right and shift left control terms is shown In Figure 29.

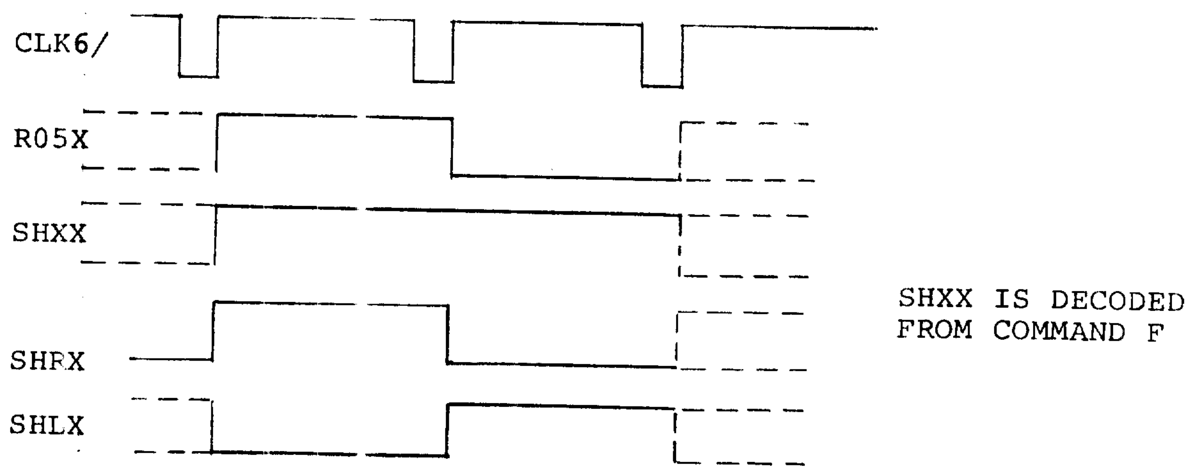


FIGURE 29

TIMING DIAGRAM FOR SHLX AND SHRX

3.4.4 Link Control

The link flip flop shown in Figure 30 stores the bit shifted off from the shift command or the carry out of the high order bit of the adder (CRY7) on the ADD, SUBTRACT or COMPARE commands. The output of the link is used as a carry input to the adder and as the bit shifted in on the SHIFT command as controlled by option bits in the commands. The inputs controlling the state of the link flip flop are generated by the bits shifted out of the file logic (F00X/ or F07X/) under control of the A bus shift enable commands, or the adder overflow, (CRY7) under control of the SHXX/ term.

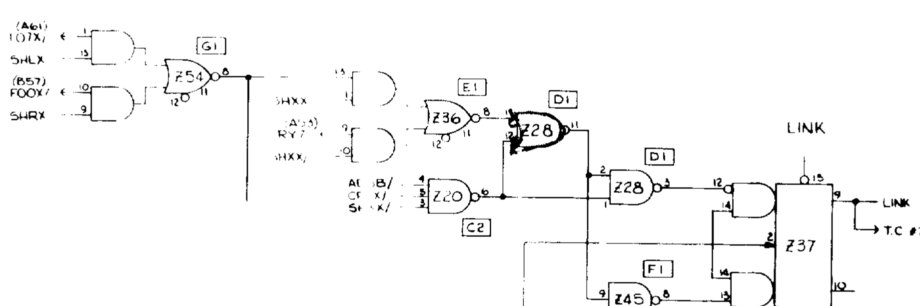


FIGURE 30

LINK FLIP-FLOP LOGIC DIAGRAM

Timing associated with the LINK when an ADD command is executed and CRY7 is high, is shown in Figure 31.

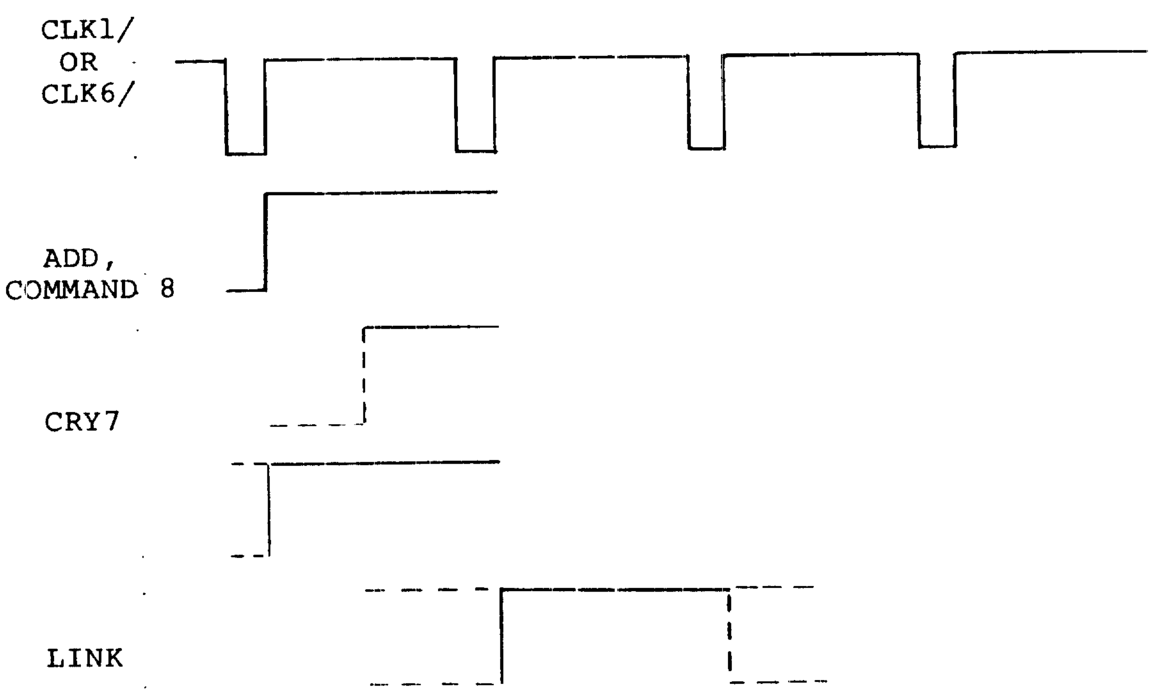


FIGURE 31

TIMING DIAGRAM FOR LINK FLIP-FLOP

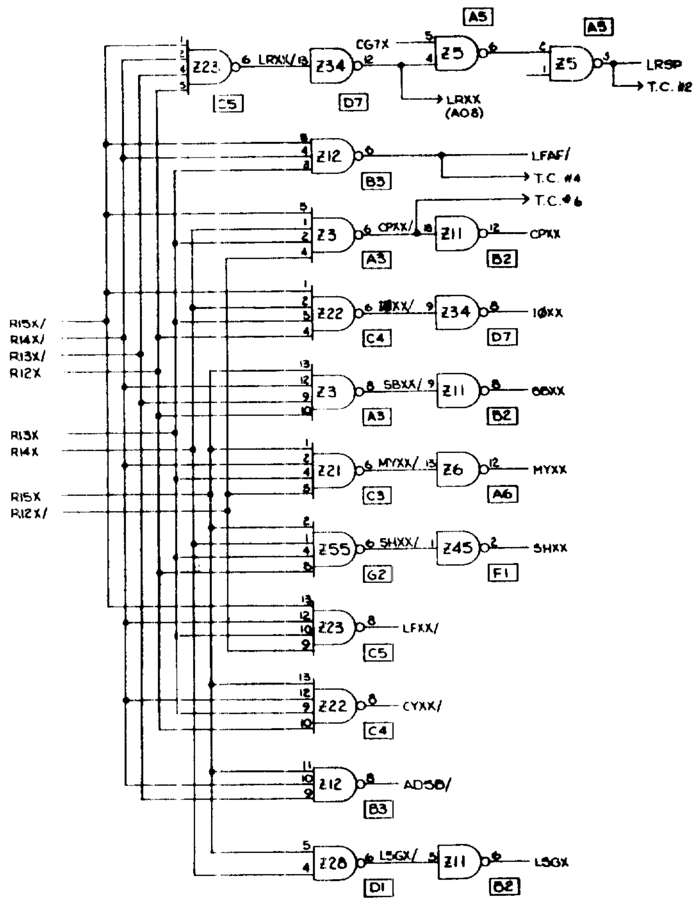
R15X	R14X	R13X	R12X	LRXX	LFAF/	C[illegible]XX	IOXX	SBXX	MYXX	SHXX	LFXX/	CYXX/	ADSB/	LSGX
0	0	0	0	0	1	0	0	0	0	0	1	1	1	0
0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
0	0	1	1	0	0	0	0	0	0	0	1	1	1	0
0	1	0	0	0	1	0	0	0	0	0	1	1	1	0
0	1	0	1	0	1	0	0	0	0	0	1	1	1	0
0	1	1	0	0	1	1	0	0	0	0	1	1	1	0
0	1	1	1	0	1	0	1	0	0	0	1	1	1	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
1	0	0	1	0	1	0	0	1	0	0	1	1	0	0
1	0	1	0	0	1	0	0	0	1	0	1	1	1	0
1	0	1	1	0	1	0	0	0	0	0	1	0	1	0
1	1	0	0	0	1	0	0	0	0	0	1	1	1	1
1	1	0	1	0	1	0	0	0	0	0	1	1	1	1
1	1	1	0	0	1	0	0	0	0	0	1	1	1	1
1	1	1	1	0	1	0	0	0	0	1	1	1	1	1

TABLE 5

TRUTH TABLE FOR COMMAND DECODER

3.4.5 Decoding Logic

All micro command OP code terms are decoded by a set of gates shown in Figure 32 whose inputs are a function of bits 12-15 of the R register. The truth table for the command decoder is given in Table 5.



COMMAND DECODER

FIGURE 32

LOGIC FOR COMMAND DECODER

Typical command decoding timing is given in Figure 33.

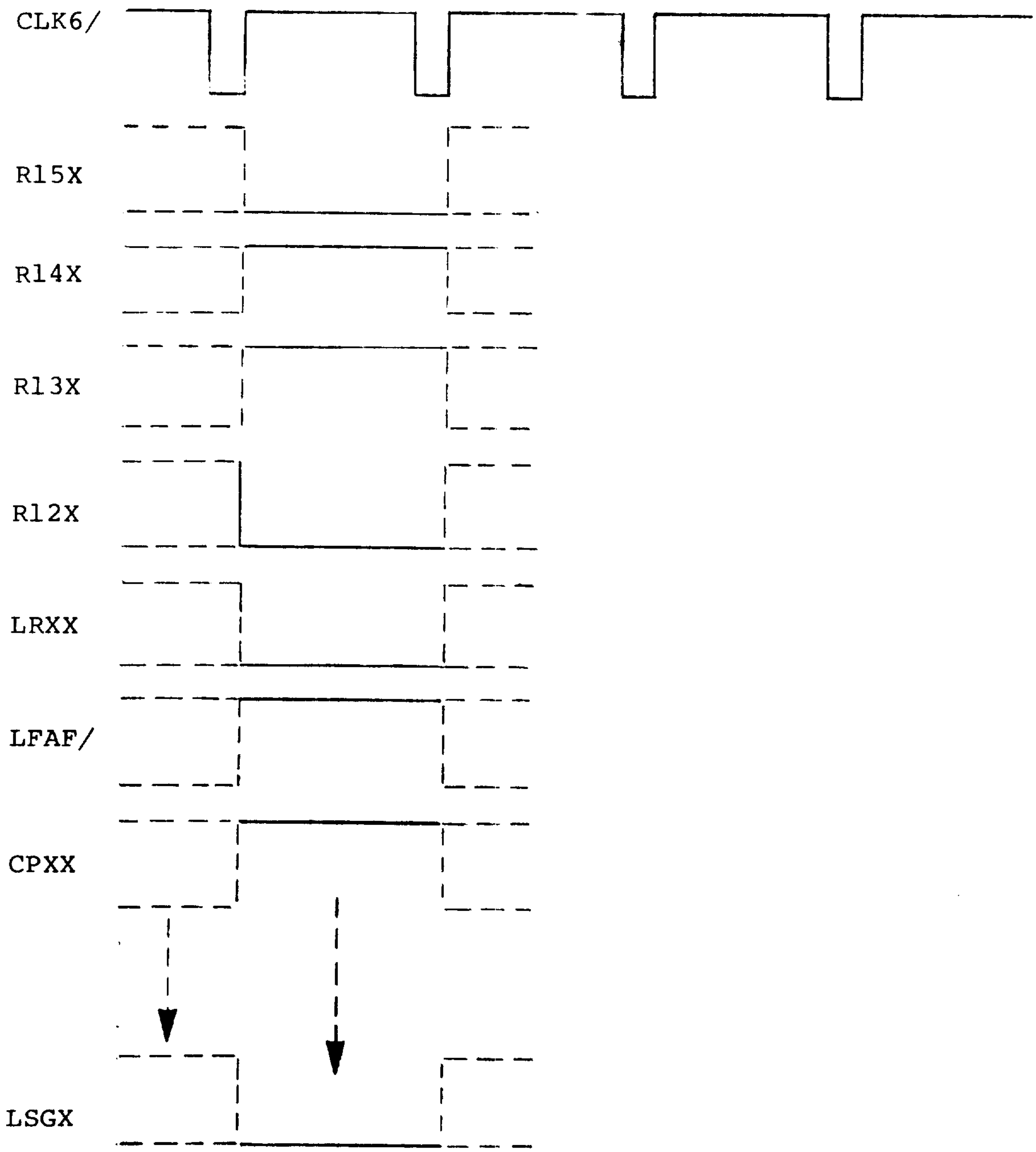


FIGURE 33

TIMING DIAGRAM FOR COMMAND DECODING TERMS

The destination decoder shown in Figure 34 provides the register designator decoding of bits 0-2 of the operate commands and 8-10 of the load register commands. The control term LRXX allows gating of bits 8-10 of the R register, whereas the term BENR/ allows gating of bits 0-2 of the R register. The truth table for the destination decoder is given in Table 6.

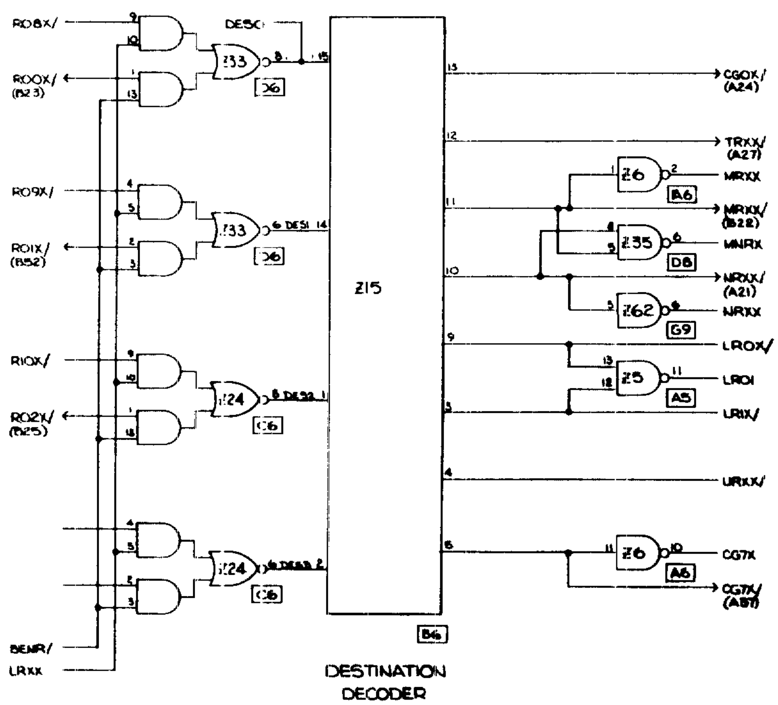


FIGURE 34

DESTINATION DECODER

It should be noticed that the term DES3, the high order bit into the decoder, is false only when one of the control terms (BENR/ or LRXX) is true. This is the condition for which the destination decoder output is to enable the selected register.

DES0	DES1	DES2	DES3	CG0X/	TRXX/	MEXX/	NRXX/	LR0X/	LR1X/	URXX/	CG7X/	LR01	MNRX
0	0	0	0	0	1	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	1	1	1	1	0	0
0	1	0	0	1	1	0	1	1	1	1	1	0	1
1	1	0	0	1	1	1	0	1	1	1	1	0	1
0	0	1	0	1	1	1	1	0	1	1	1	1	0
1	0	1	0	1	1	1	1	1	0	1	1	1	0
0	1	1	0	1	1	1	1	1	1	0	1	0	0
1	1	1	0	1	1	1	1	1	1	1	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	0	0
1	0	0	1	1	1	1	1	1	1	1	1	0	0
0	1	0	1	1	1	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	0	0
1	0	1	1	1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0	0

TABLE 6

TRUTH TABLE FOR DESTINATION DECODER

Typical timing for the destination decoder is given in Figure 35.

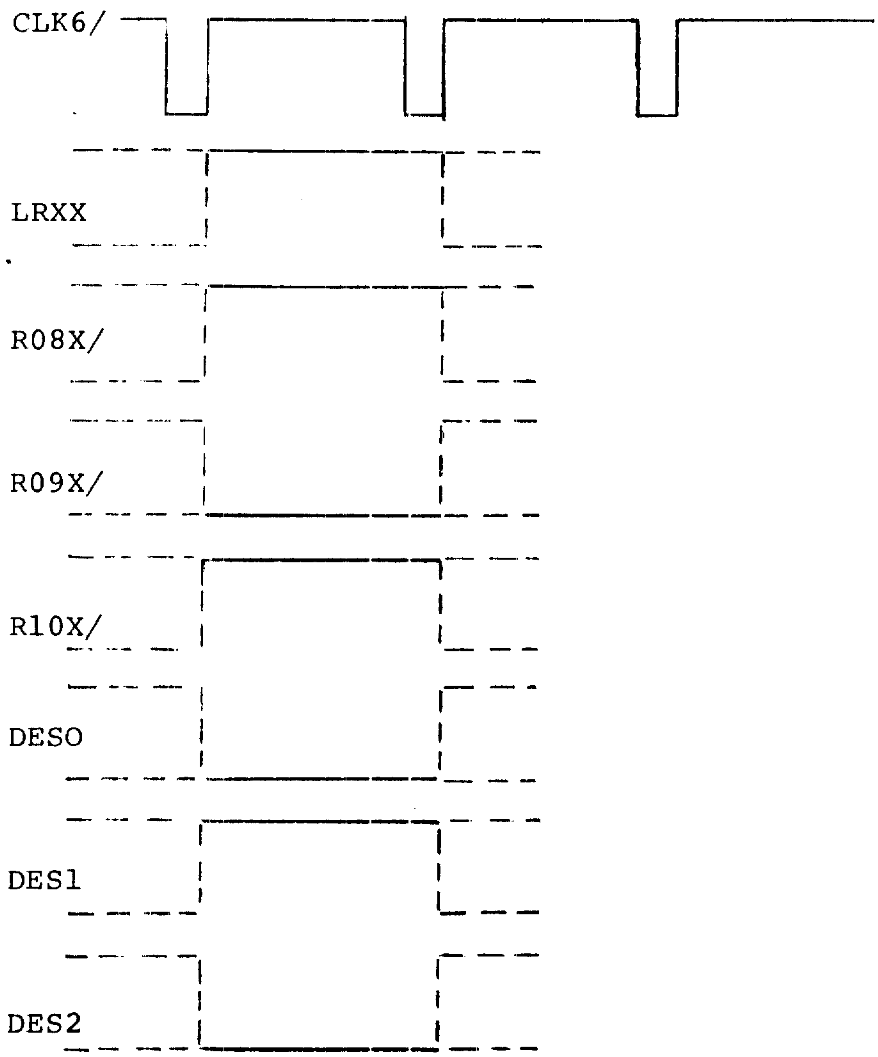


FIGURE 35

TIMING DIAGRAM FOR DESTINATION DECODER

The I/O control registers (IO1X, IO2X, and IO3X) shown in Figure 36 are mechanized by Z49 and Z40. These flip flops are cleared by master reset (MRST/) and clocked by CLK1/. The flip flops receive their inputs from bits 4-6 of the R register when EXIO is true during the execution of a control command with bit 7, a 1 bit. The INTC flip flop is set whenever the console interrupt switch is depressed and is cleared when internal status is read (AENI).

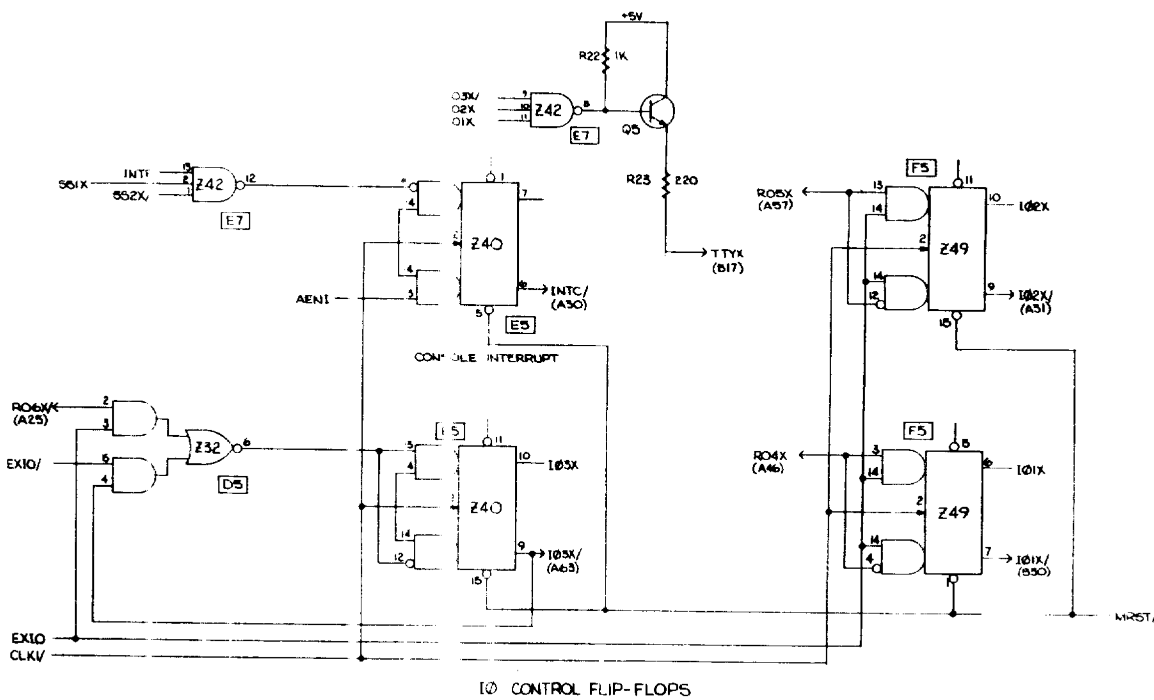


FIGURE 36

I/O CONTROL FLIP-FLOPS

Timing for the I/O control flip flops is shown typically in Figure 37.

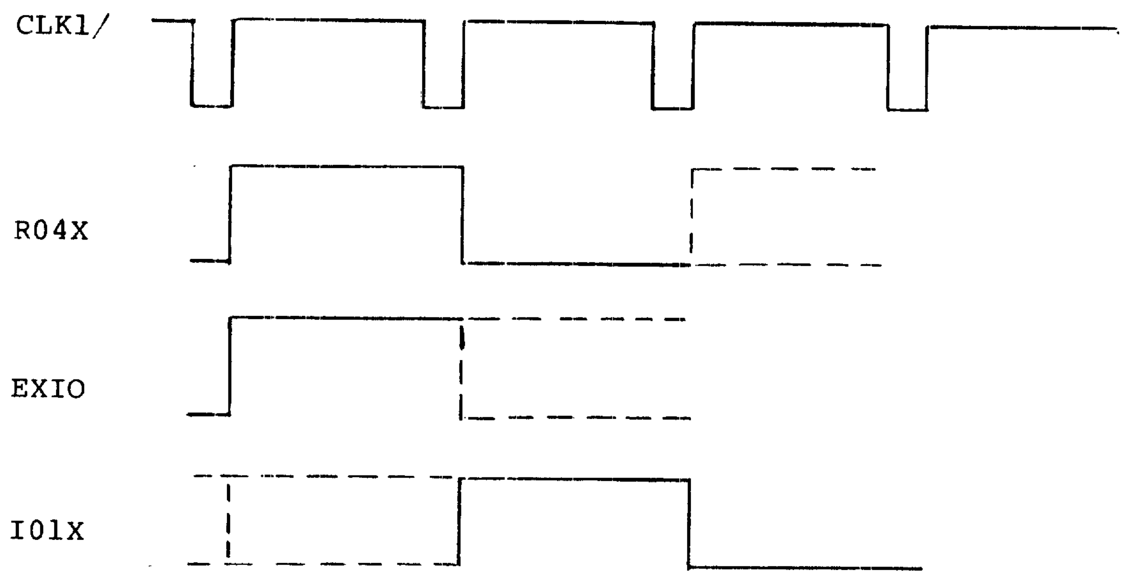
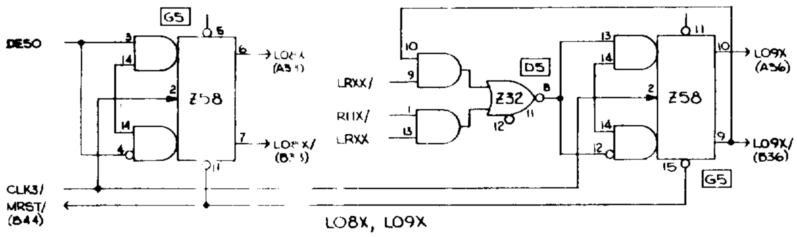


FIGURE 37

TIMING DIAGRAM FOR I/O CONTROL FLIP-FLOPS
(Typical)

3.4.6 L Register (Bits 8 and 9)

Bits 8 and 9 of the L register are generated by Flip Flop Z58. As shown in Figure 38, the true and complement outputs of these two flip flops are sent to the four read only storage boards for page select decoding. The input to L08X is the least significant bit of the commands register designator (DES0). The input to L09X is R11X for the jump command (LRXX) and the output of the flip flop itself for other commands which load the L register.



ROS ADDRESS COUNTER BITS 8, 9

FIGURE 38

L REGISTER BITS 8 AND 9

Bits 8 and 9 of the L register are used to select or enable a Read Only Store module (or board). The card slots in the computer which have been allocated for ROS, have been pre-wired for the proper addressing of each ROS module. The addressing follows:

Address		ROS Module	Card Slot
L09X	L08X		
0	0	0- 255	14
0	1	256- 511	15
1	0	512- 767	16
1	1	768-1023	17

3.4.7 Console Operation

The run, step, halt and console interrupt switches control operation of the computer through a set of latches consisting of 9002 type gates located on the control board. Logic for console operation is shown in Figure 39. The four latches are OR'ed together to form the term SSIS in gate Z51. This term becomes true when any one of the four console switches is depressed and the following clock pulse turns on the flip flop SS1X. The following clock pulse turns on SS2X and these two flip flops together form a switch synchronizer for strobing the output of the switch latches. The two flip flops turn off in the same order that they are turned on whenever the front panel switch is released.

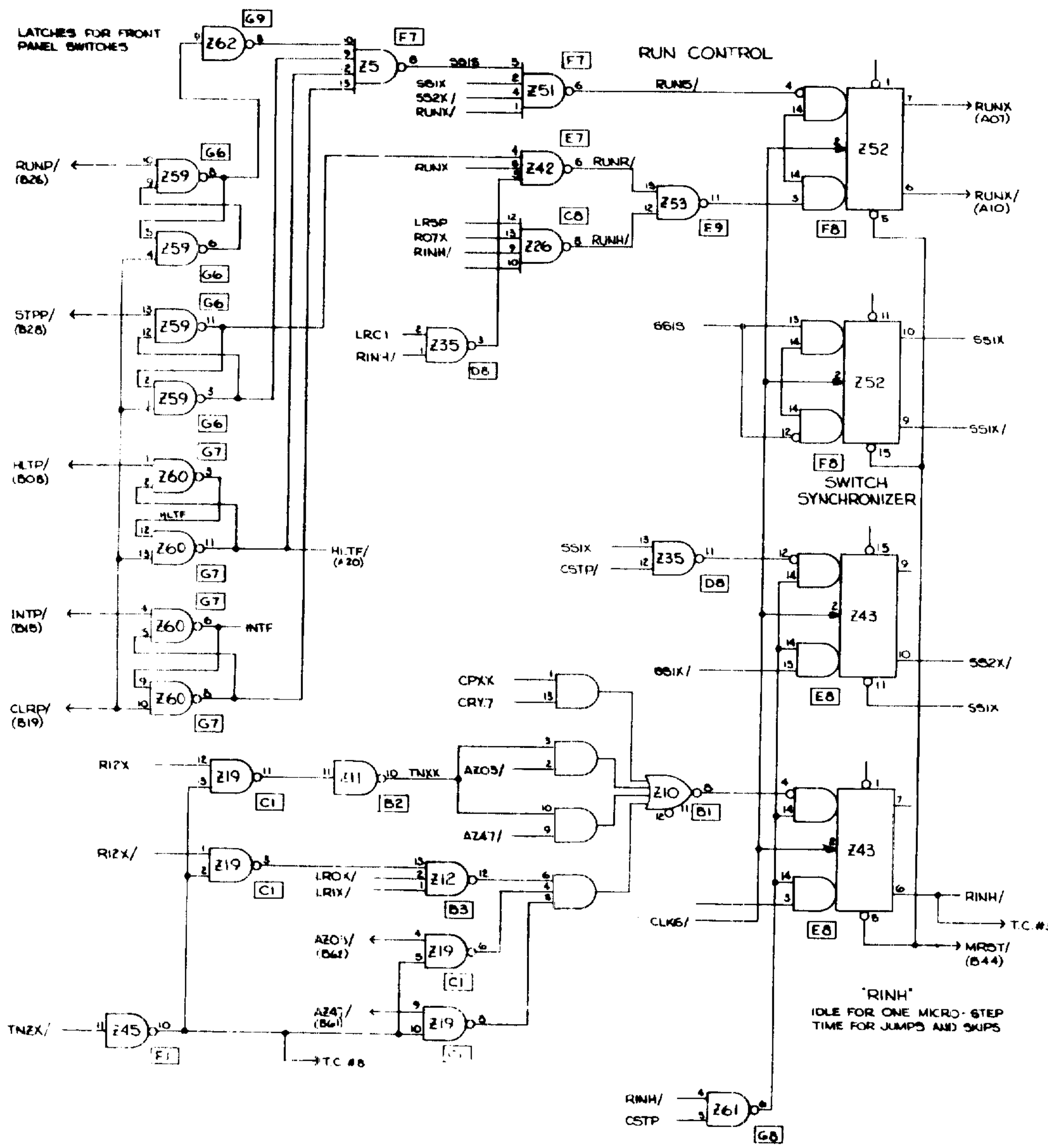


FIGURE 39

CONSOLE OPERATION LOGIC

The run control flip flop, RUNX, is turned on whenever one of the run, step or the halt front panel switches is depressed. It is turned off with the next clock pulse if the step switch is depressed (STEP controls RUNR) and by the halt command (RUNH). When single clock stepping the machine, the RUNX flip flop will be on for two clock times if the executed command causes a skip or jump to take place. The RINH flip flop controls idling of the machine for one clock time on jumps and skips.

The Halt lamp driver is energized, resulting in the halt lamp illuminating when RUNX is at a 0 state. The Run lamp driver is energized when RUNX/ is false (or at a 0 state). In each case the state of the Run control flip flop (Z52) is inverted to drive the lamp drivers and turn the lamps on or off as the flip flop is set or reset.

The Run lamp driver and Halt lamp drivers are located on Data Boards 1 and 2, respectively, and are shown in Figure 40.

FIGURE 40

RUN AND HALT LAMP DRIVERS

3.4.8 Clocks and Command Timing

There are eight clocks generated in the machine by ANDing together two outputs of the 4.55 MHz crystal oscillator. The clocks are shown schematically in Figure 41. The term CPH1 is the output of the oscillator as picked off by gate Z78. CPH2/ is 180° out of phase with CPH1 and is delayed by approximately 25 nanoseconds by an RLC network. The AND'ed coincidence of these two signals produces a 25 to 35 nanosecond clock pulse as gated by various control terms. CSTP/ is a clock stop term that is used on most of the gated clocks.

The clock is stopped under any of the following conditions:

(1) RINH/·RUNX (RINH/ idles the machine during skips and jumps; RUNX stops the clocks when the machine is OFF.)

(2) MYXX·MSTP stops the clock when the memory command is to be executed if memory read timing is on, memory write timing is on, or a DMA request is pending.

(3) MDNA·DMAS/·(BNTP+BNTM). The clock is stopped during processor memory read operations if the data is not available and the current instruction is selecting the T or complement of T as the operand on the B bus.

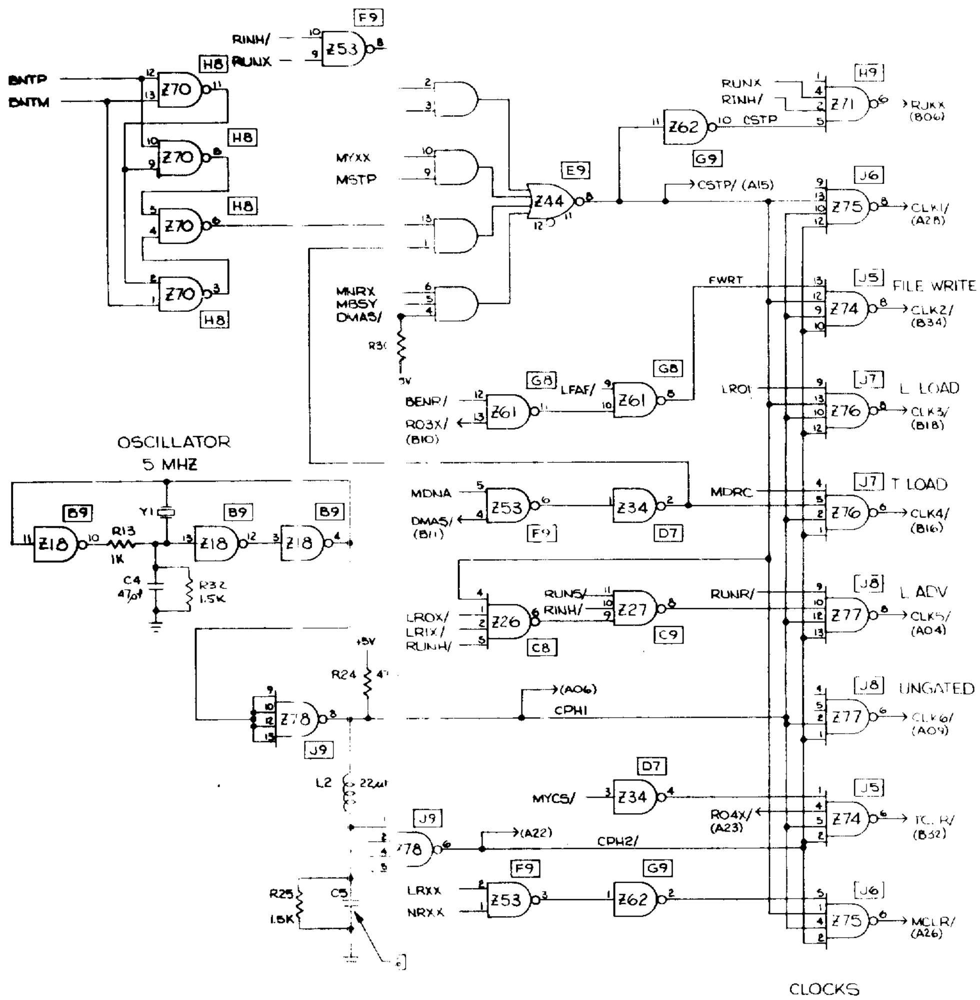


FIGURE 41

SCHEMATIC DIAGRAM FOR CLOCKS

Wave shapes and clock timing are shown in Figure 42.

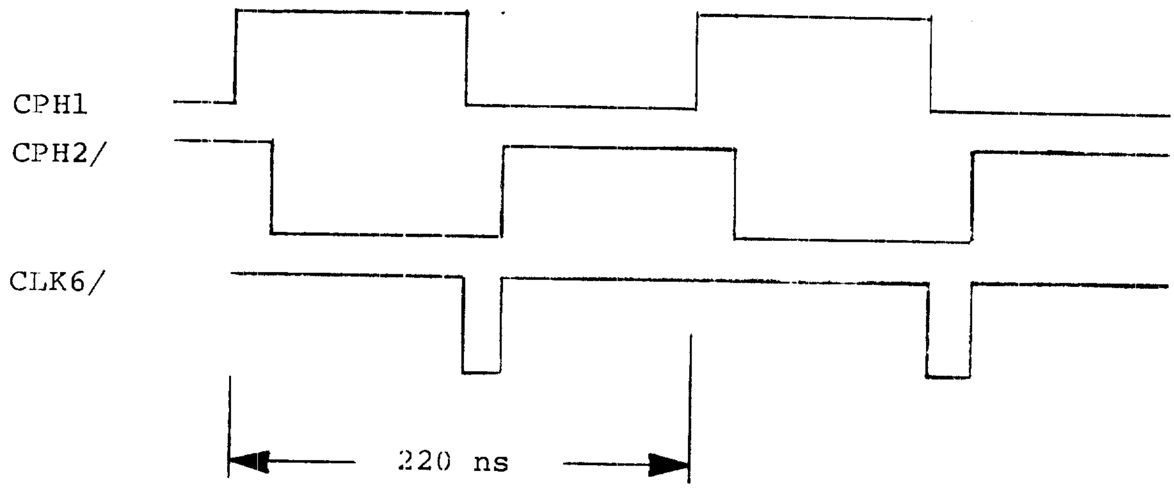


FIGURE 42

TIMING DIAGRAM FOR CLOCKS

(4) MNRX·MBSY·DMAS/. The clock is stopped if the current command is selecting M or N register and the memory is busy carrying out a processor memory operation.

The eight clocks are described below:

(1) CLK1/
This clock is gated with the clock stop term CSTP/.

(2) CLK2/
This file write clock is used for strobing the A bus into the selected file register and is gated with CSTP/ and FWRT. The FWRT term allows the file write clock to occur on a load file and add to file command (LFAF) and on operate commands if bit 3 is a 0 bit.

(3) CLK3/
The L register load clock causes the A bus to be loaded into the 8 low order bits of the L register and is gated with CSTP/ and LR02 which is generated when the L register is designated as the destination register.

(4) CLK4/
The T load clock gates data from the memory data bus into the T register via the direct set inputs. This clock occurs with the second clock following the start of a processor memory read operation (MDRC·MDNA·DMAS/).

(5) CLK5/
This clock allows the L register to advance its count. The L register advances its count by one on the clock pulse that turns on the RUNX flip flop and is inhibited from advancing on the clock pulse that turns RUNX off. The clock is also inhibited if the L register is the destination for the command or if CSTP is true, except for idles caused by skip commands. The inhibit logic for this clock is given by:

RUNR/·(RUNS+RINH+CSTP/·LROX/·LRIX·RUNH/)

(6) CLK6
This clock is ungated and is used in the memory, run control and other logic not sensitive to command execution. Generation of CLK6/ is shown in Figure 42.

(7) TCLR/
This clock clears the T register at the beginning of a processor memory read operation.

(8) MCLR/
This clock clears the M register when a literal is loaded into the N register (LRXX·MRXX).

The details of the clocks generated in the machine are repeated here for convenience. Reference should be made to the schematic diagram for circuit details. CPH1 is the output of the oscillator as picked off by Z78. CPH2/ is 180° out of phase with CPH1 and is delayed by approximately 25 ns by an RLC network. The AND'ed coincidence of these two signals produces a 25 to 35 ns clock pulse (CLK6/) as gated by various control terms. A general system timing diagram is shown in Figure 43.

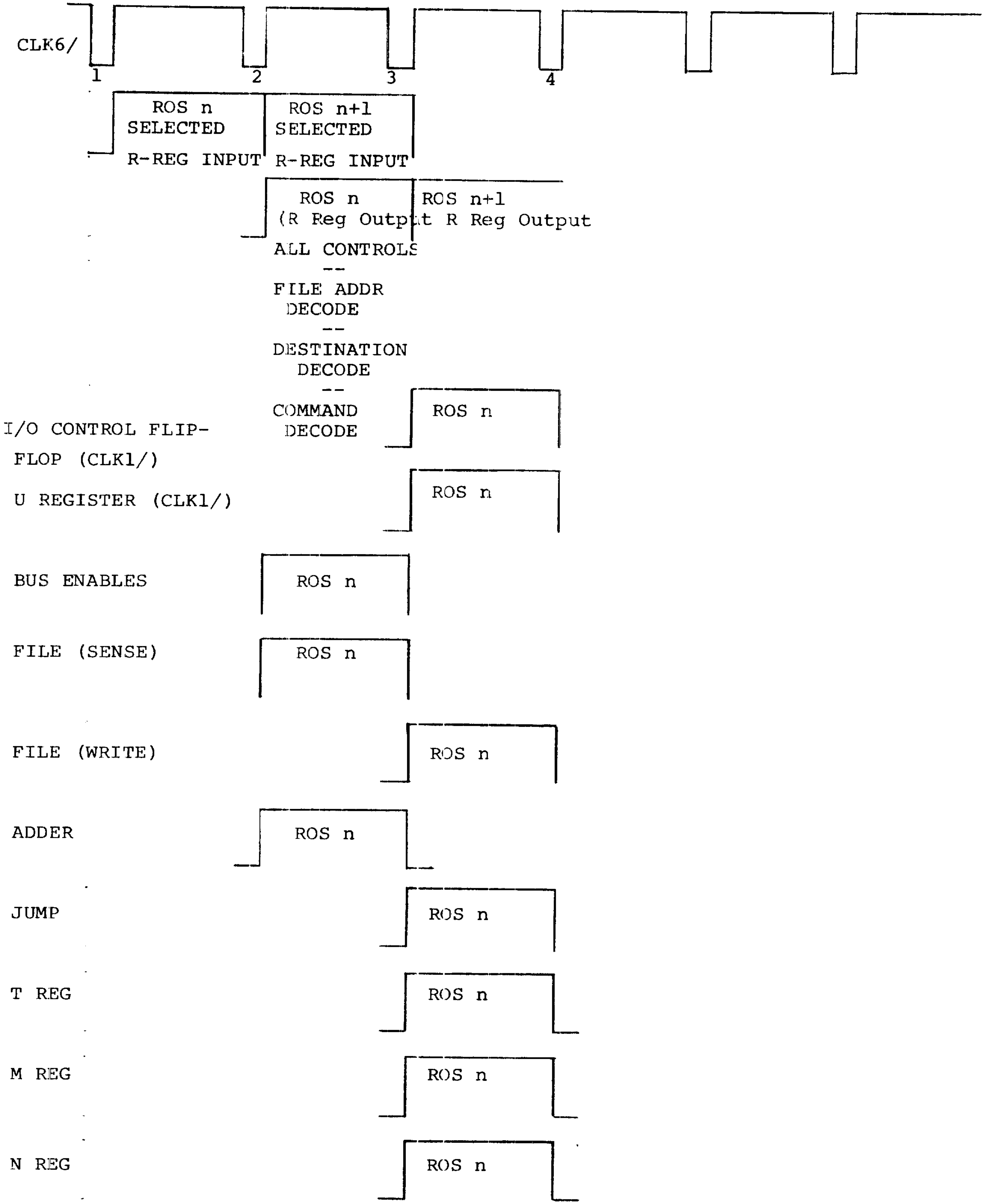


FIGURE 43

GENERAL TIMING DIAGRAM FOR COMPUTER CONTROL AND COMMAND EXECUTION

The general timing diagram illustrates when in the computer an ROS microcommand is decoded and/or used to update the contents of a register or flip flop.

In general, at the first clock pulse the next ROS microcommand is selected and it becomes the input to the R register. Upon the next clock pulse (shown as 2), the R register output is altered to reflect the state of its previous input. At this time, the next ROS command accessed becomes the input to the R register. The R register output is decoded and control terms are generated throughout the machine making ready to execute the command. At the third clock pulse (shown as 3), various registers and/or flip flops are updated to reflect the command being executed. At this time the second command input to the R register is now reflected at the R register output, control signals being generated for its execution.

Flow charts showing execution of two sample instructions of the machine's repertoire are given in Figures 45 and 46.

3.4.9 Condition Code Flip Flops

The condition code flip flops shown in Figure 47 store the condition on the A bus when the term ENCC is true. ENCC becomes true during a control command or an operate command with the exception of the memory command if bit 4 is true.

Flip flop CCOX stores the adder overflow on a command using the adder:

(AFLT·ADDX)

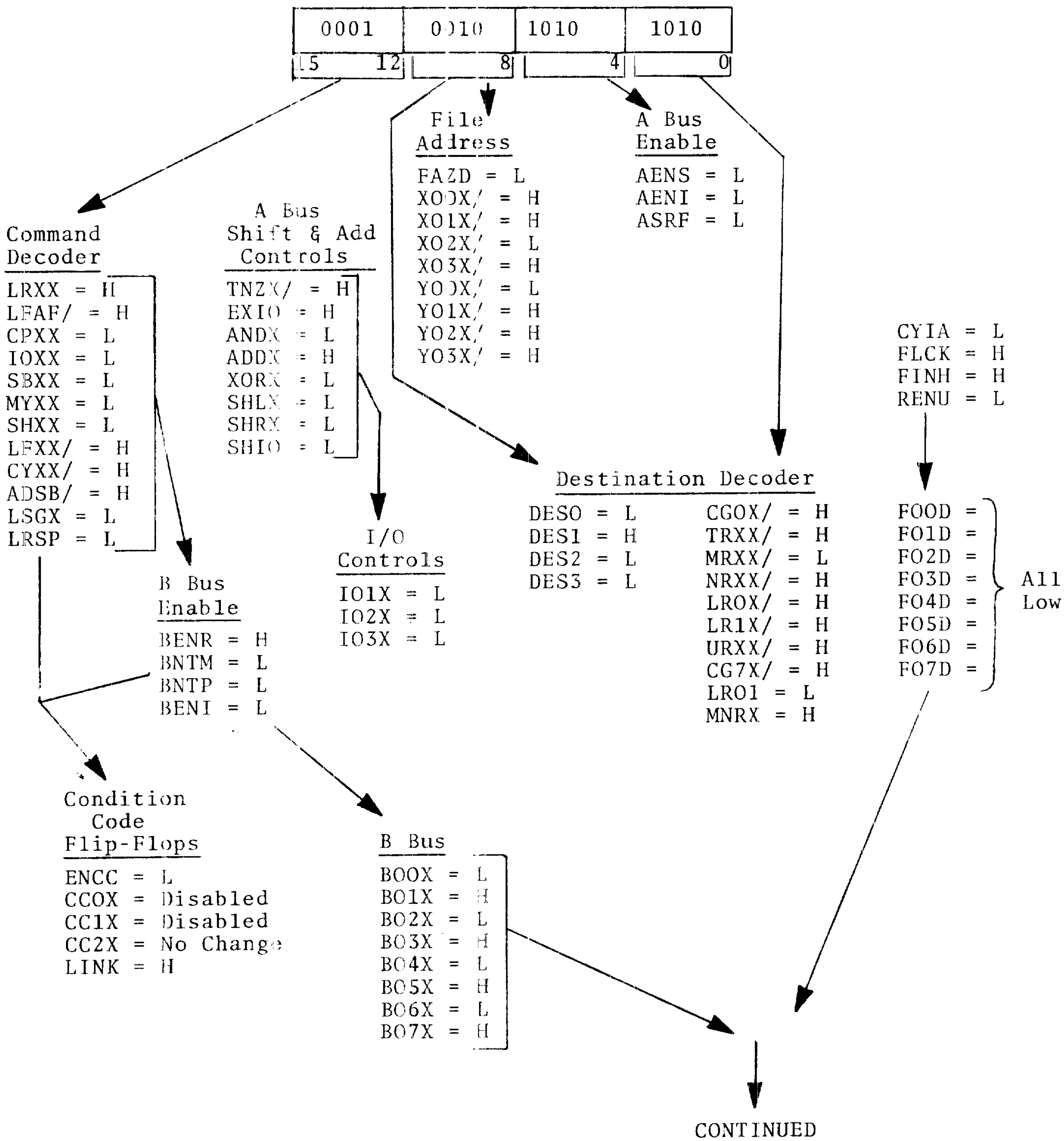
or CCOX will store the bit shifted off in a shift command

F07X·SHLX+FOOX·SHRX)

Flip flop CC1X stores the high order bit of the A bus. Flip flop CC2X stores the output of the zero detect on the A bus.

If the link control bit (R07X) is on, the flip flop can be reset, but cannot be set (R07X·CC2X/) to allow for a link 0 test across multiple bytes.

FIGURE 45 FLOW CHART FOR LOAD M COMMAND



Clocks

RJKX = H
CLK1/ = Running
CLK2/ = H
CLK3/ = H
CLK4/ = H
CLK5/ = Running
CLK6/ = Running
TCLR/ = H
MCLR/ = H

Adder

AU0X =
AU1X =
AU2X =
AU3X =
AU4X =
AU5X =
AU6X =
AU7X =

A-Bus

A00X =
A01X =
A02X =
A03X =
A04X =
A05X =
A06X =
A07X =

L-Reg
Advances at

CLK5/

T-Reg
Inhibited
Due to

TRXX/ = H

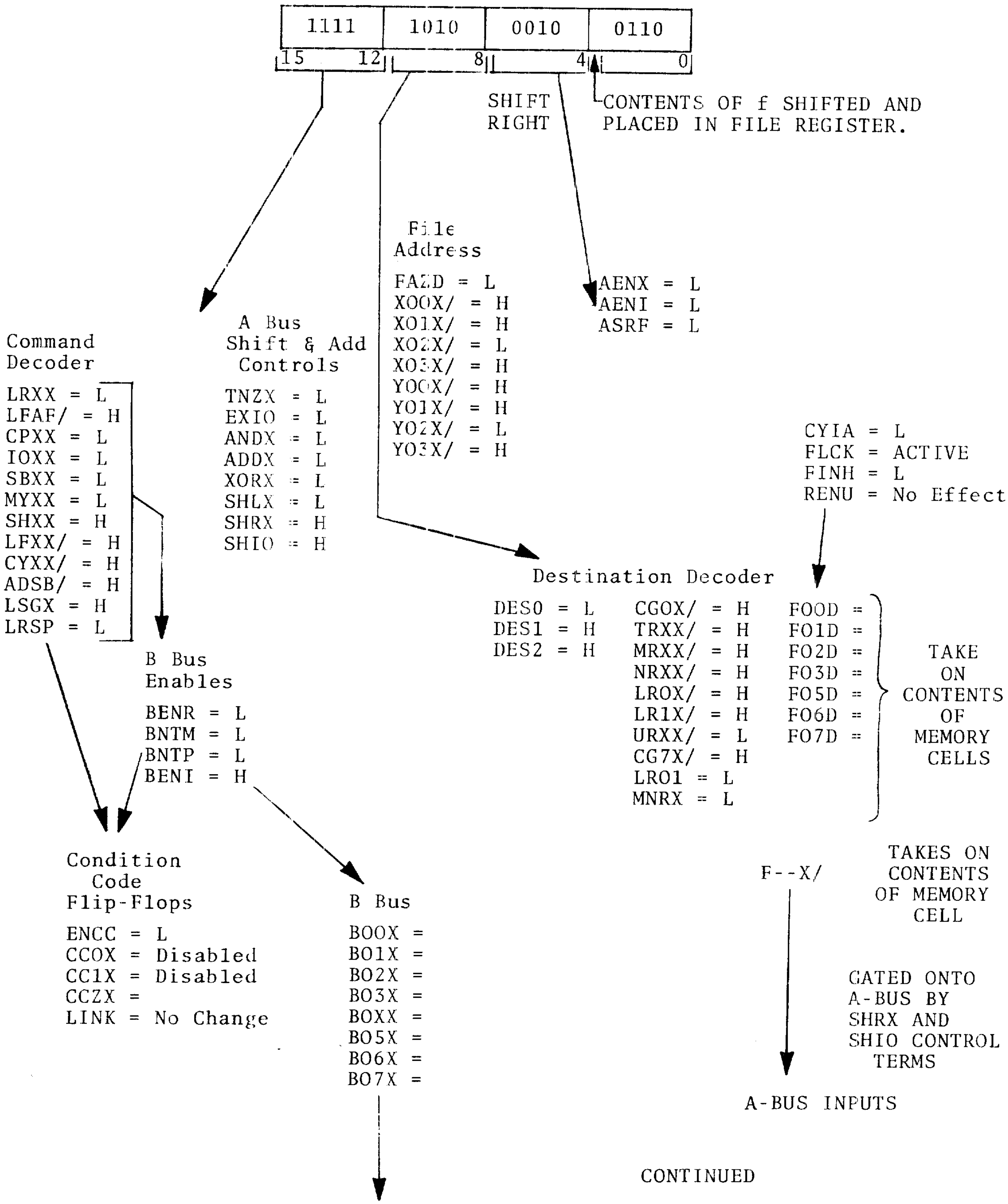
M-Reg

M00A/ = 1
M01A/ = 0
M02A/ = 1
M03A/ = 0
M04A/ = 1
M05A/ = 0
M06A/ = 1
M07A/ = 0

N-Reg
Inhibited
Due to

NRXX/ = H

FIGURE 46 FLOW CHART FOR SHIFT COMMAND



CONTINUED

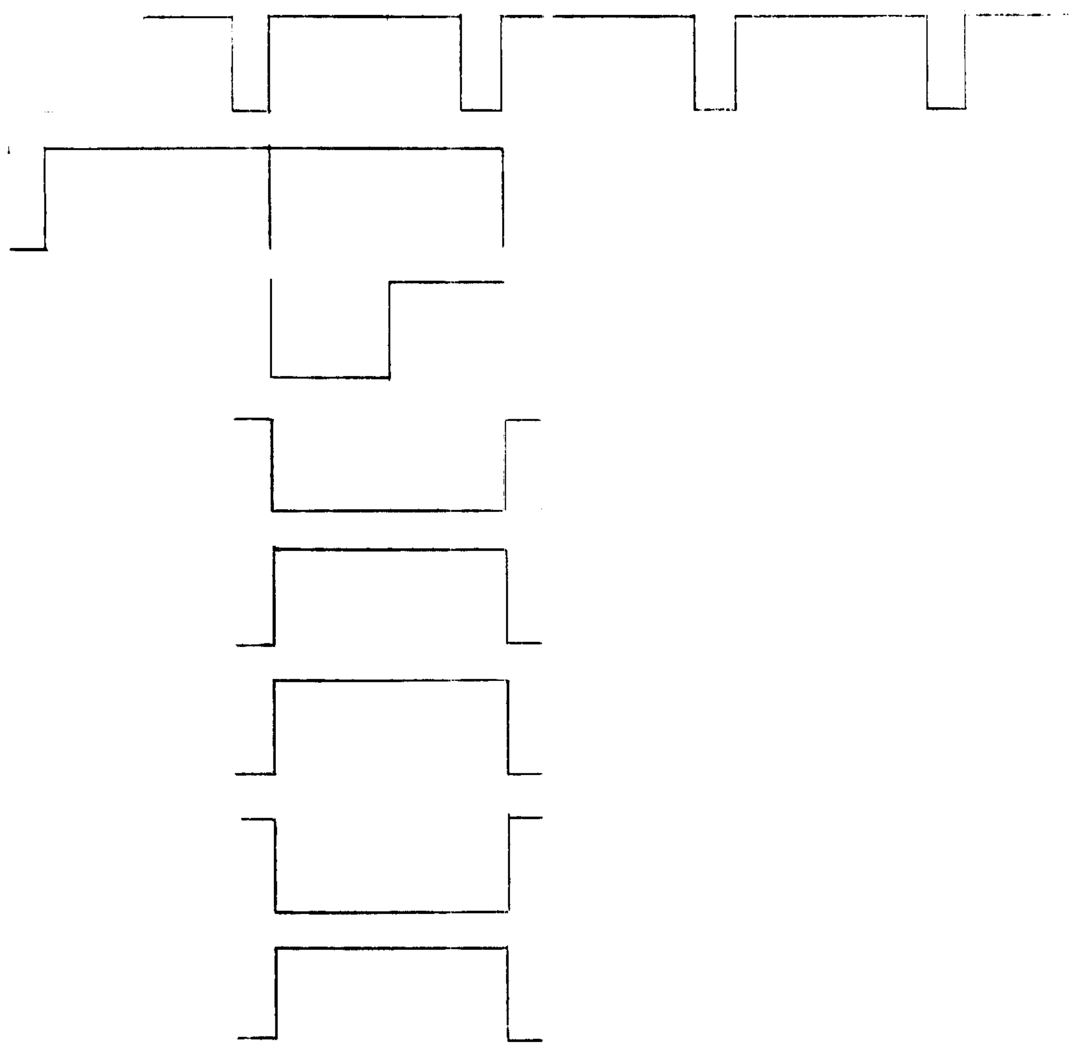
Clocks	Adder	A-Bus	
RJKX = H	Not gated	A00X/ =	
CLK1/ = Running	onto A-Bus	A01X/ =	TAKES
CLK2/ = Off	since control	A02X/ =	ON
CLK3/ = Off	term ADDX is	A03X/ =	STATES
CLK4/ = Off	POW.	A04X/ =	OF
CLK5/ = Running		A05X/ =	F--X/
CLK6/ = Running		A06X/ =	BITS
TCLR/ = Off		A07X/ =	
MCLR/ = Off			

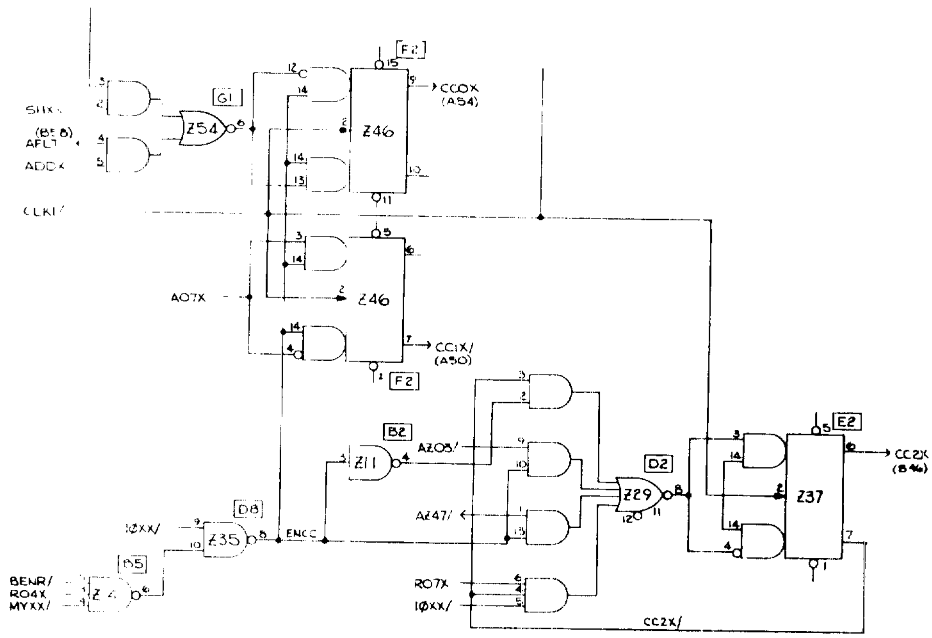
L-Reg Advances Under CLK5/

T-Reg Disabled (TRXX/ = H)

M-Reg Disabled (MRXX/ = H)

N-Reg Disabled (NRXX/ = H)





CONDITION CODE FLIP-FLOPS

3.4.10 Memory Control Circuits

The memory control logic shown in Figure 48 located on the control board, consists of two flip flops, MRTX and MWTX, which are used to control memory read and write timing delays, respectively. Each flip flop controls a delay circuit consisting of two transistors and an RC timing network. The read timing network which develops the TRXX/ signal is adjusted for 400 nanoseconds. The write timing delay which develops the WTXX/ control signal is adjusted for 450 nanoseconds. The two flip flops are turned off by the first clock pulse which occurs after the delay. The MRTX flip flop is turned on if a full cycle or read half cycle operation is to take place. The MWTX flip flop is turned on if a full cycle or half cycle write operation

CONTROL BOARD (J11)

1000200

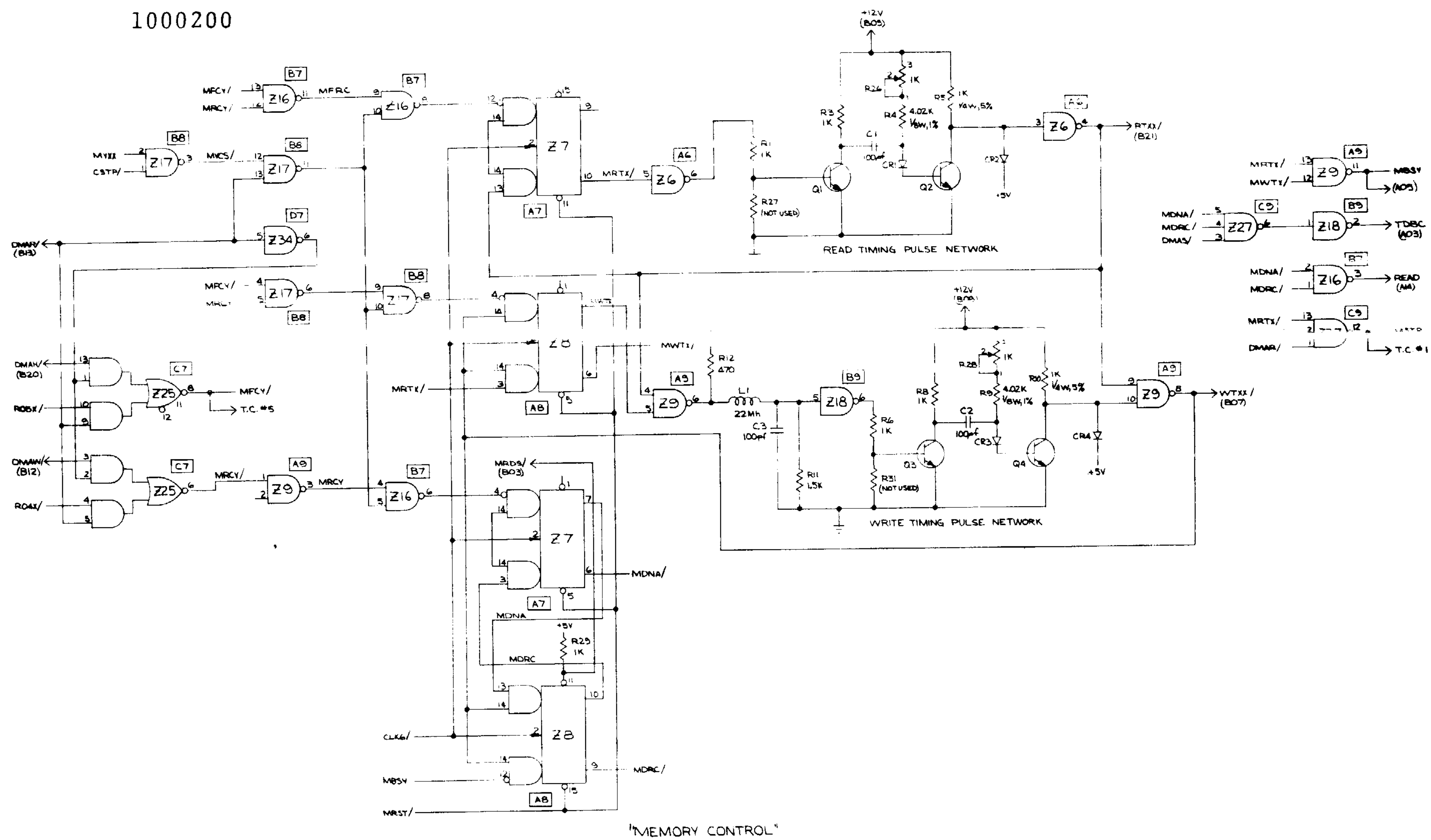


FIGURE 48

MEMORY CONTROL LOGIC

is to take place. The MWTX flip flop is turned on if a full cycle or half cycle write operation is to take place. If both flip flops are turned on, the write timing delay network does not time out after the read timing delay has elapsed. The MDNA flip flop is turned on at the same time as the two timing flip flops when a read operation is to take place and is turned off two clock pulse times later, after MDRC is turned on. MDRC controls the CSTP clock stop term in order to introduce a delay in command execution while waiting for data to be read from the memory. The MBSY signal indicates that the memory is busy. TDBC controls the gating of the T register onto the memory data bus. The READ signal indicates to the memory modules that they are performing a read operation and causes the output of the sense amplifiers to be gated onto the memory data bus for transfer to the T register, DMA and for regeneration. The MSTP signal is the OR combination of the DMA request, memory write timing or memory read timing.

The memory control enable signals, WTSB/ and RTSB/, are controlled by the read and write timing signals RTXX/ and WTXX/ and by each other as an interlock. The AND'ed combination of MSA, MSB and MSC forms a control term on WTSB/ and RTSB/. When RTXX/ goes to a 0 (initiated by MYXX), RTSB/ also goes to a 0. This initiates the read memory cycle current loops, IOXR and IOYR. When WTSB/ is generated in the second half cycle IOYW and IOXW, the write current loops are energized. The timing diagram for full cycle memory operation is shown in Figure 49.

B bus enable terms are generated via logic of Figure 50. BNTP enables the T register true output to the B bus . BNTM enables the T register complement output to the B bus. BENI enables the input bus to the B bus. BENR enables the R register to the B bus. Refer to Section 3.5.2 for a description of the operation of the B bus.

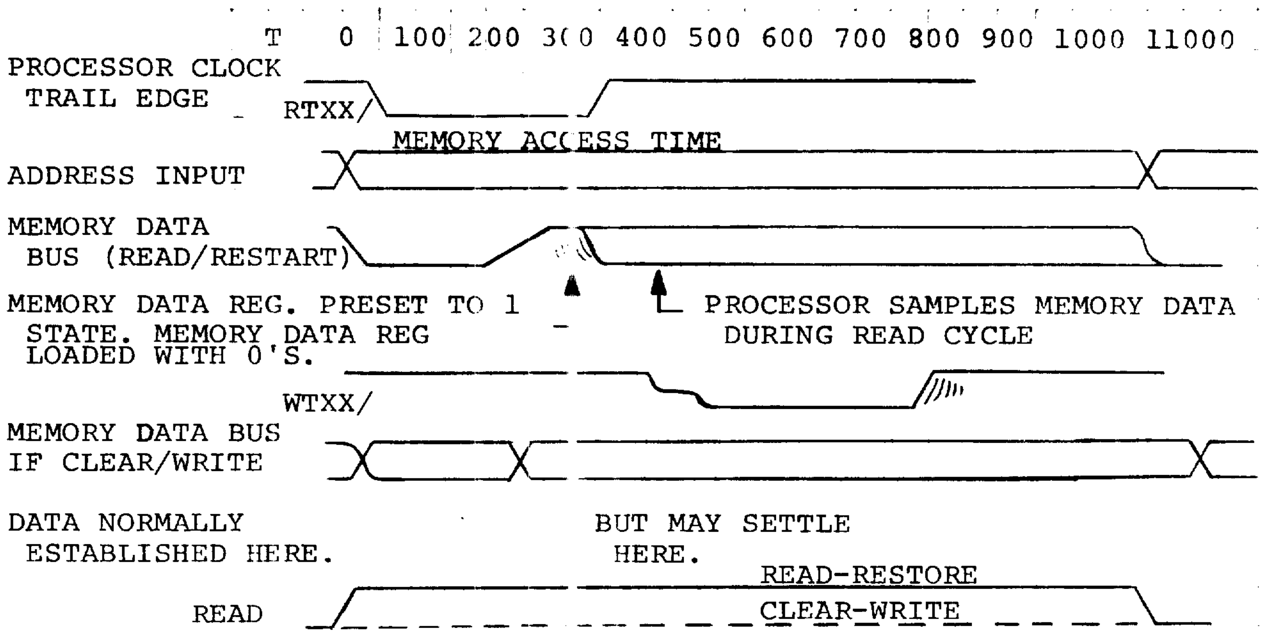
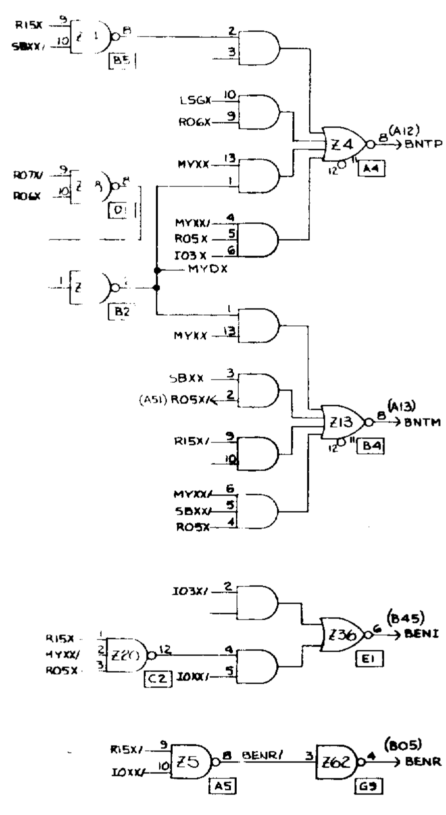


FIGURE 49
TIMING DIAGRAM FOR FULL CYCLE MEMORY OPERATION



B-BUS ENABLES

FIGURE 50

B-BUS ENABLE TERMS
LOGIC DIAGRAMS

A bus enable terms are generated via logic shown in Figure 51. The control term, SHIO, controls a second level of A bus gating, which includes a shift left and shift right of the file, entry of the internal status, the shift right by 4 bits of the file register and entry of the sense switches. The file shifted right 4 and the sense switch entry are entered into the same gating position, on the two data boards, since each uses four bits. The file shifted right 4 is entered onto Data Board No. 1 and the sense switches are entered onto Data Board No. 2.

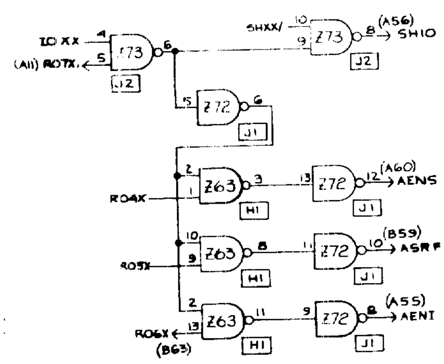


FIGURE 51
A-BUS ENABLE TERMS LOGIC DIAGRAM

CYIA is the initial carry (shown in Figure 52) into the low order bit of the adder and also serves to hold the bit "shifted in" on the shift command. CYIA is true in commands where bit 6 of the command is a 1 bit, except for SUBTRACT and MEMORY. On the memory command, CYIA is true if bits 6 and 7 are 1 bits. CYIA is true for commands where bit 7 of the command and the contents of the LINK register are both 1 bits. Also, CYIA is true for SUBTRACT if both bits 6 and 7 of the command are 0 bits.

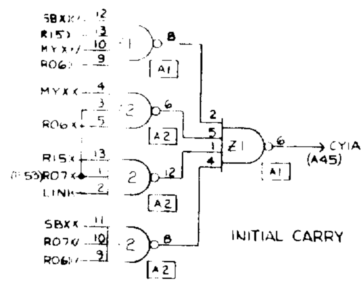


FIGURE 52
LOGIC DIAGRAM FOR INITIAL CARRY

The File Latch Control shown in Figure 53 is performed by FLCK and FINH. FINH is true for file load, load register and copy T commands and causes the output of the file to be forced to 0 bits. The FLCK term which controls the latching of the file latch circuit is basically the CPHZ plan of the clock circuit OR'ed with FINH.

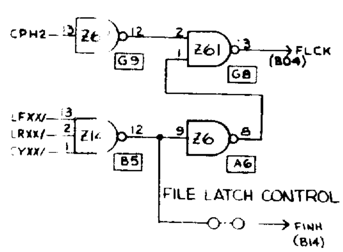
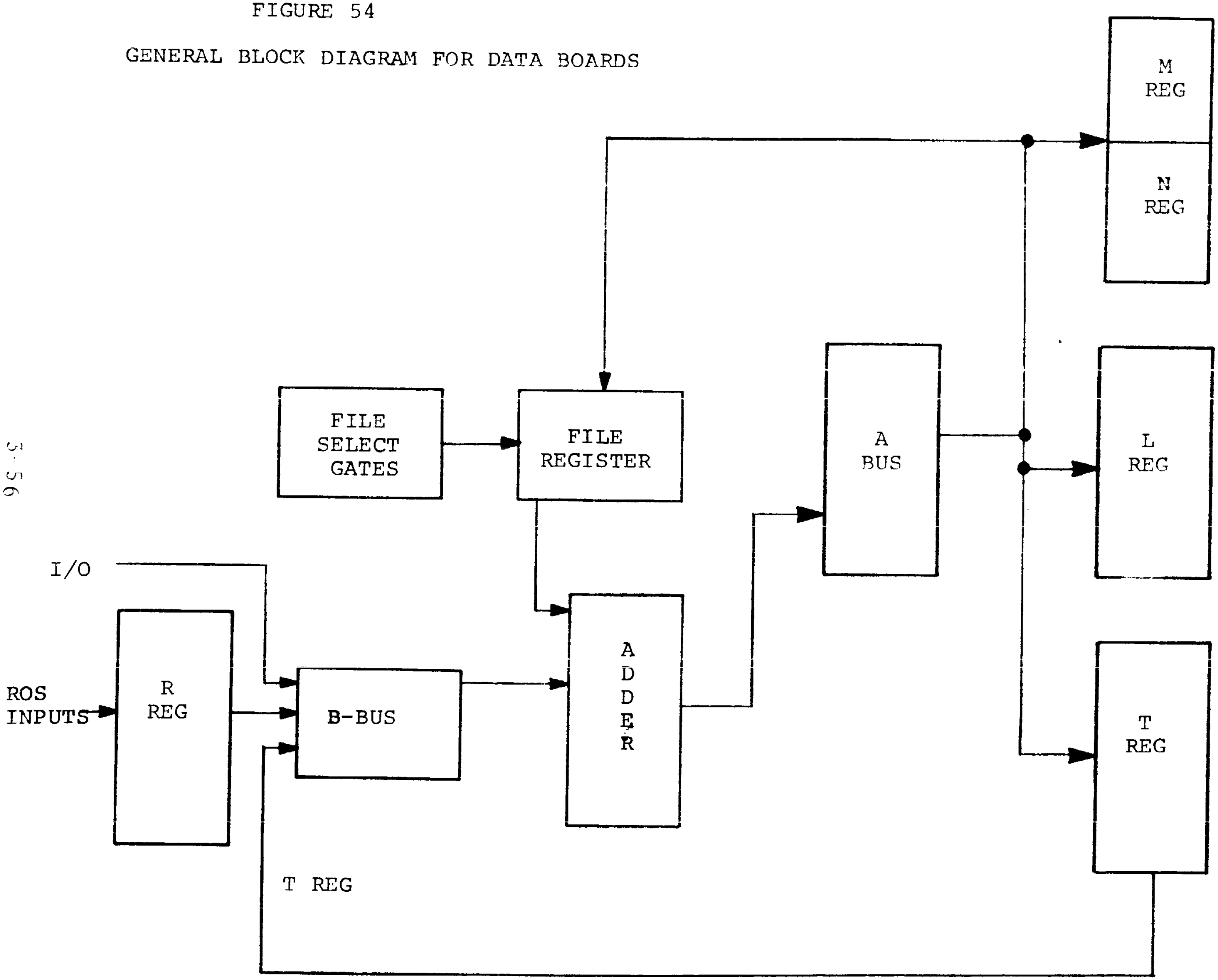


FIGURE 53
FILE LATCH CONTROL LOGIC DIAGRAM

FIGURE 54

GENERAL BLOCK DIAGRAM FOR DATA BOARDS



3.5.1 R Registers

The 8 low order bits of the R register (Bits 0-7) shown in Figure 55 are broken up into two parts and are located on Data Boards 1 and 2. Bits 0-3 on Data Board No. 1 and Bits 4-7 on Data Board No. 2. The inputs to these 8 bits of the R register come from the ROS or the control panel switches. The control panel switches are collector OR'ed to the read only storage by element Z18. The control panel switches are enabled by grounding CPEN/ or when the control instructions AENI and ASRF are both true. The R register flip flops are clocked by CLK6/.

DATA BOARD NO. 1 DATA BOARD NO. 2

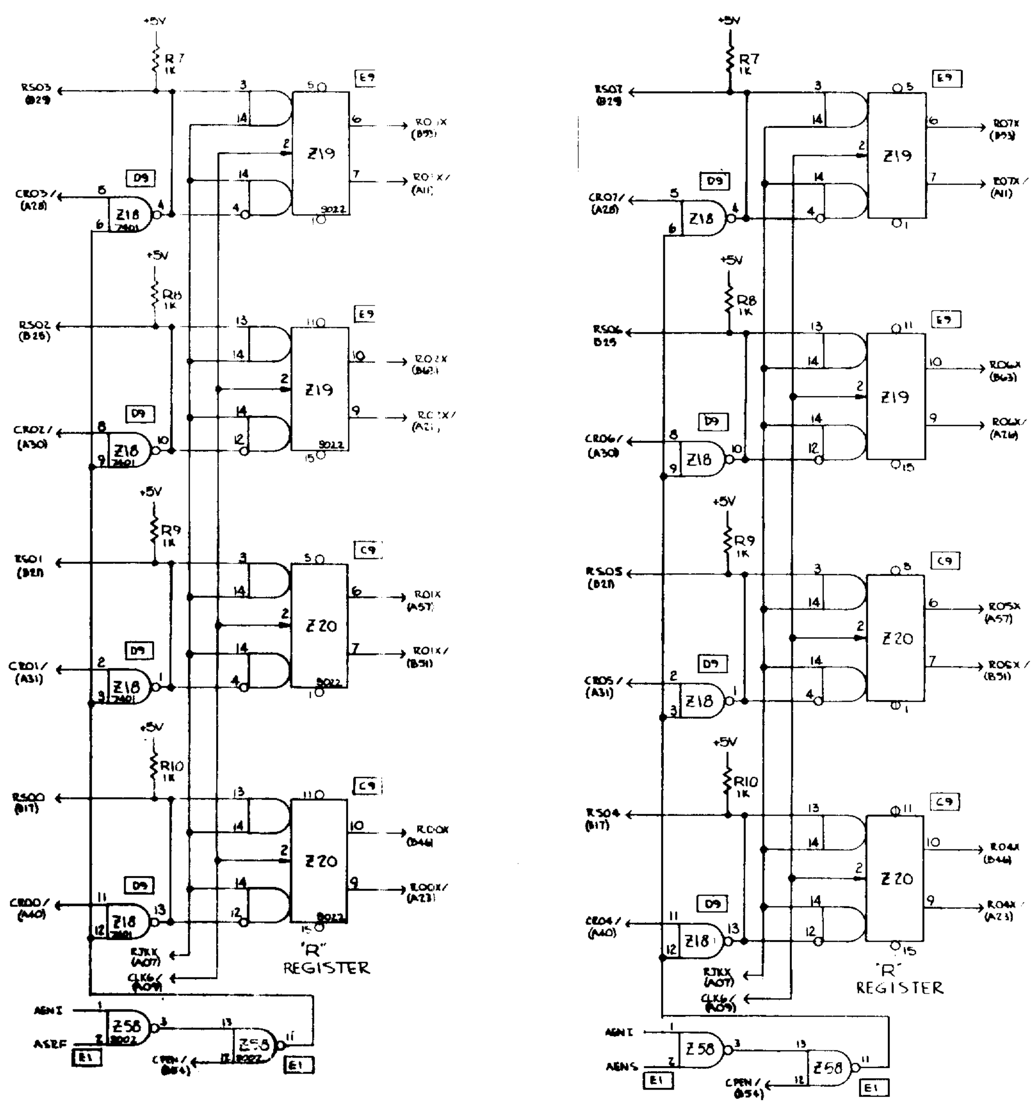


FIGURE 55

R-REGISTER
BITS 0-7

3.5.2 B Bus

B bus outputs B00X through B03X are on Data Board No. 1 and B04X through B07X are on Data Board No. 2. The four inputs to each of the eight elements comprising the B bus are enabled by control terms as follows:

FUNCTION	CONTROL
Input Bus to B Bus	BENI
R Register to B Bus	BENR
T Register True Output to B Bus	BNTP
T Register Complement Output to B Bus	BNTM

The B bus true outputs become inputs to the ADDER.

When all four control signals to the B bus are false (BENI, BENR, BNTP and BNTM are all zero), the B bus inputs to the ADDER are all true.

The adder is mechanized by logic elements Z27 and Z28 shown in Figures 56 and 57 whose inputs are the true B bus outputs (B0-X) and true input from the file (F0-D). The term CYIA is the carry into the least significant bit of the adder. CYIA is derived from the logical combinations of control terms generated by the command decodes and bits 6, 7 and 15 from the R register. CYIA is the carry term to Data Board No. 1 for bit location zero (AU00).

The carry term for Data Board No. 2 is the carry out of the adder bit three (AU03) and is termed CRY3. Each data board has an overflow detect circuit; however, only the output from that circuit on Data Board No. 2 is used. Both boards are identical hardwarewise

ADDER - THEORY OF OPERATION

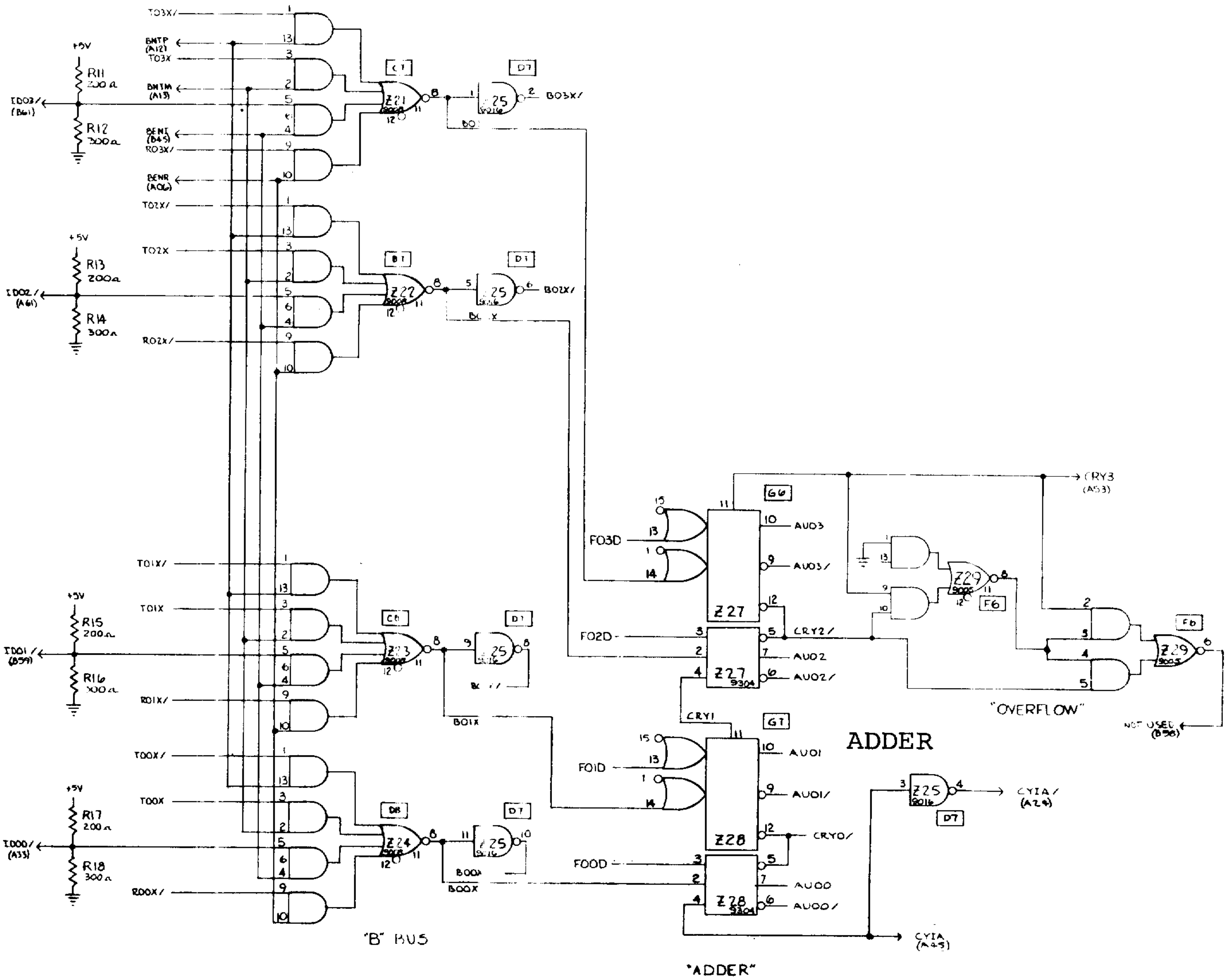


FIGURE 56

LOGIC DIAGRAM B-BUS AND ADDER BITS 0-3

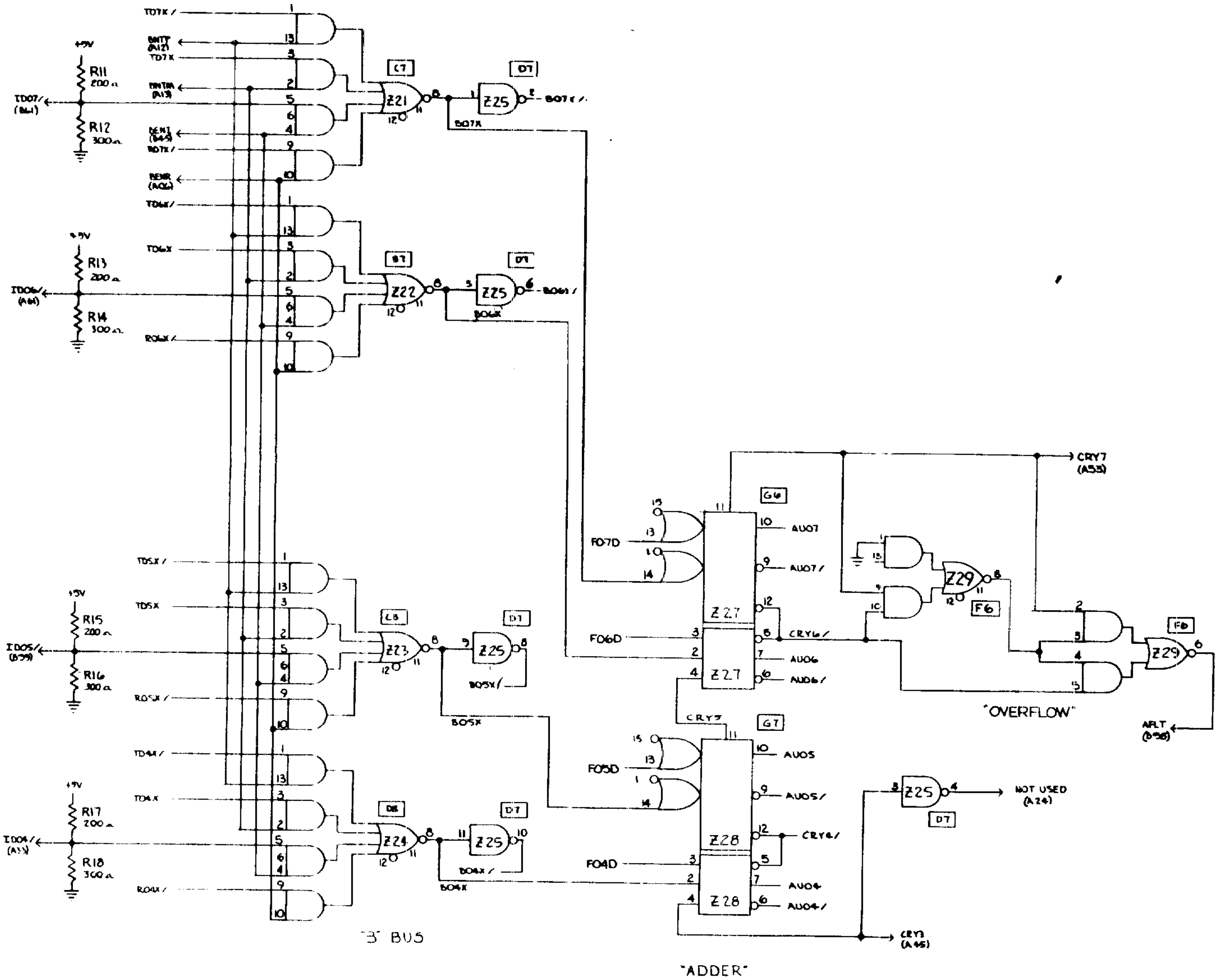
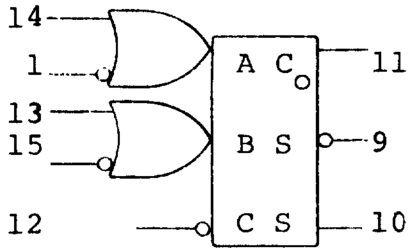
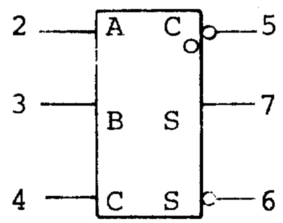


FIGURE 57

LOGIC DIAGRAM B-BUS AND ADDER BITS 4-7





The 9304 adder consists of two separate high speed binary full adders. Each adder has the sum and its complement as outputs. Single inversion circuitry is used in the carry logic to provide very low carry through delay. The second adder has provisions for either active high or active low inputs at the A or B operand inputs.

The adders produce a low carry and both low and high sum with active high inputs, or active high carry and both high and low sum when active low inputs are used.

The adder functions in the computer when the ADD (Command 8) and SUBTRACT (Command 9) microcommands are executed.

Take the condition during the ADD function when the C field bits are all zeros. The file address is decoded in bits 8, 9, 10 and 11. The output of the command decoder shows

LFAF/ = High with all other functions low.
LFXX/ = High
CYXX/ = High

BNTM and BNTP both become high and are used as the control gates enabling the true and complement states of the T register outputs to the B bus.

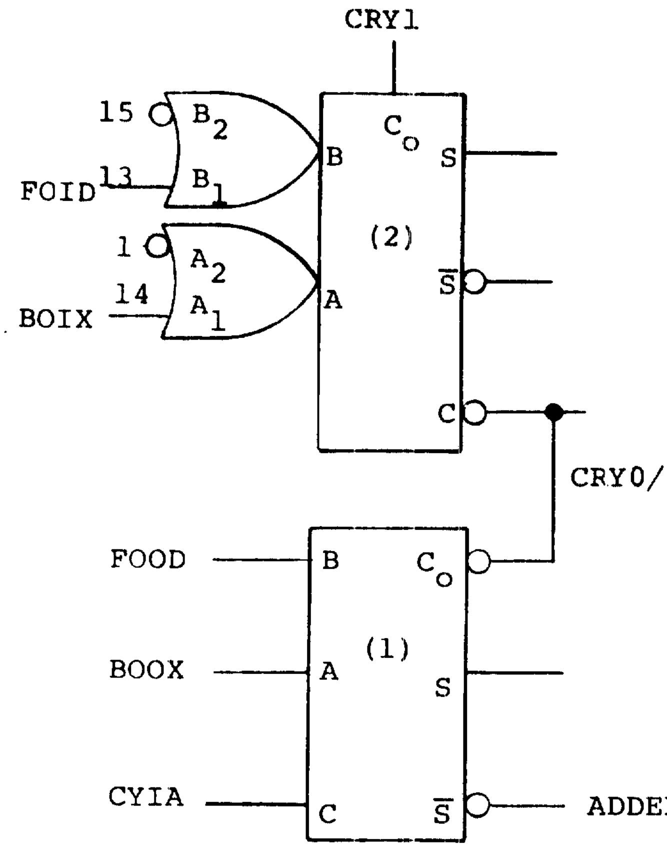
The B bus outputs and the sense line outputs of the file become inputs to the adder along with the initial carry term which is generated if the Add/ or Link control operand is selected.

If the ADD Command is being executed, with the C field bit 6 a one bit (add 1 option is selected), then CYIA becomes a one bit.

The inputs to the adder are the contents of the addressed file register, the B bus (which will be all zeros for the example cited) and the initial carry term.

As an example, assume the file register input to the adder is | 1111 1111 |.

With the CYIA term a one bit, Figure 58 illustrates adder operation for the first two bits in the adder where successive adder stages must be individually evaluated dependent upon the input and status of the carry line input.



ADDER 2

INPUTS			OUTPUTS		
$\overline{C}$	A1	B1	C_O	S	$\overline{S}$
L	L	H	H	L	H

ADDER 1

INPUTS			OUTPUTS		
C	B	A	$\overline{C_O}$	$\overline{S}$	S
H	H	L	L	H	L

FIGURE 58
ADDER OPERATION (1st 2 BITS)

In the example under discussion, where 1 is being added to 1111 1111, attention is now focused upon AU06 and AU07.

CRY5 is summed with F06D causing CRY6/ to go high and to be summed with F07D which in turn enables CRY7. The AND/OR circuitry of Z29 in turn generates AFLT, the adder overflow indication shown in Figure 57.

The ADDX term, being high and used as the control gate of the arithmetic unit output to the A bus is gated with AFLT to set the CCOX flip flop at the next CLK1/. Also the CRY7 term is gated with SHXX/ and under control of ADSB/ is used to set LINK at the next CLK1/.

Timing for the ADD operation with condition code CCOX and LINK being set is shown in Figure 59.

Subtraction (Command 9) is executed by the complement of the selected operand plus one being added to the contents of the selected file register. The result is a 2's complement subtraction.

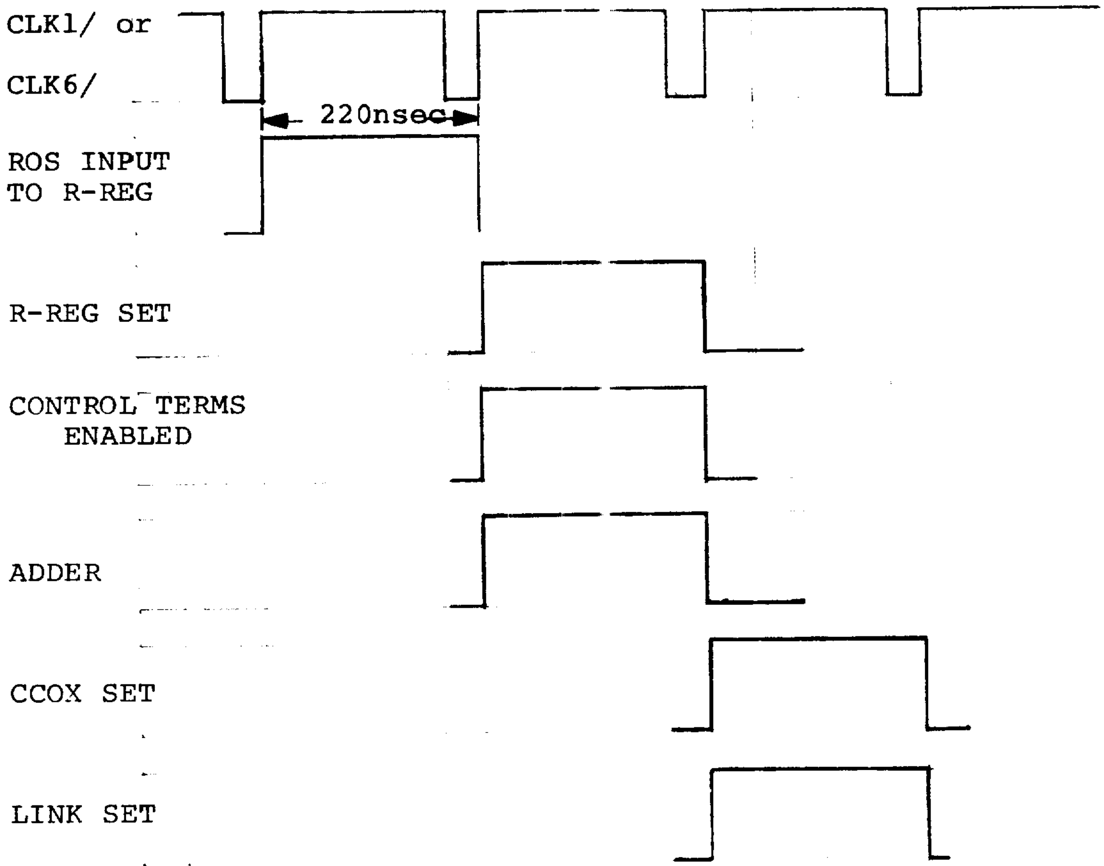


FIGURE 59

TIMING DIAGRAM
FOR
ADD OPERATION

Suppose, for example, the contents of the selected file was the number 7 (00000111) and 5 (00000101) was to be subtracted from it. The T register true output contains the number 5. Upon execution of Command 9

LFAF/ = H	ADDX = H
SBXX = H	
LFXX/ = H	
CYXX/ = H	

Bit 5 being a one bit (to select T) results in

BNTP = 0
BNTM = 1
CYIA = 1

The B bus enable BNTM becomes high enabling the complement output of the T register to be OR'ed into the B bus.

The CYIA term goes high, thereby adding one to the complement of the selected operand at the adder input.

F07D through F00D are (00000111) respectively. The truth tables shown in Section 3.3.14 yield the output states of the adder as shown in Figure 60.

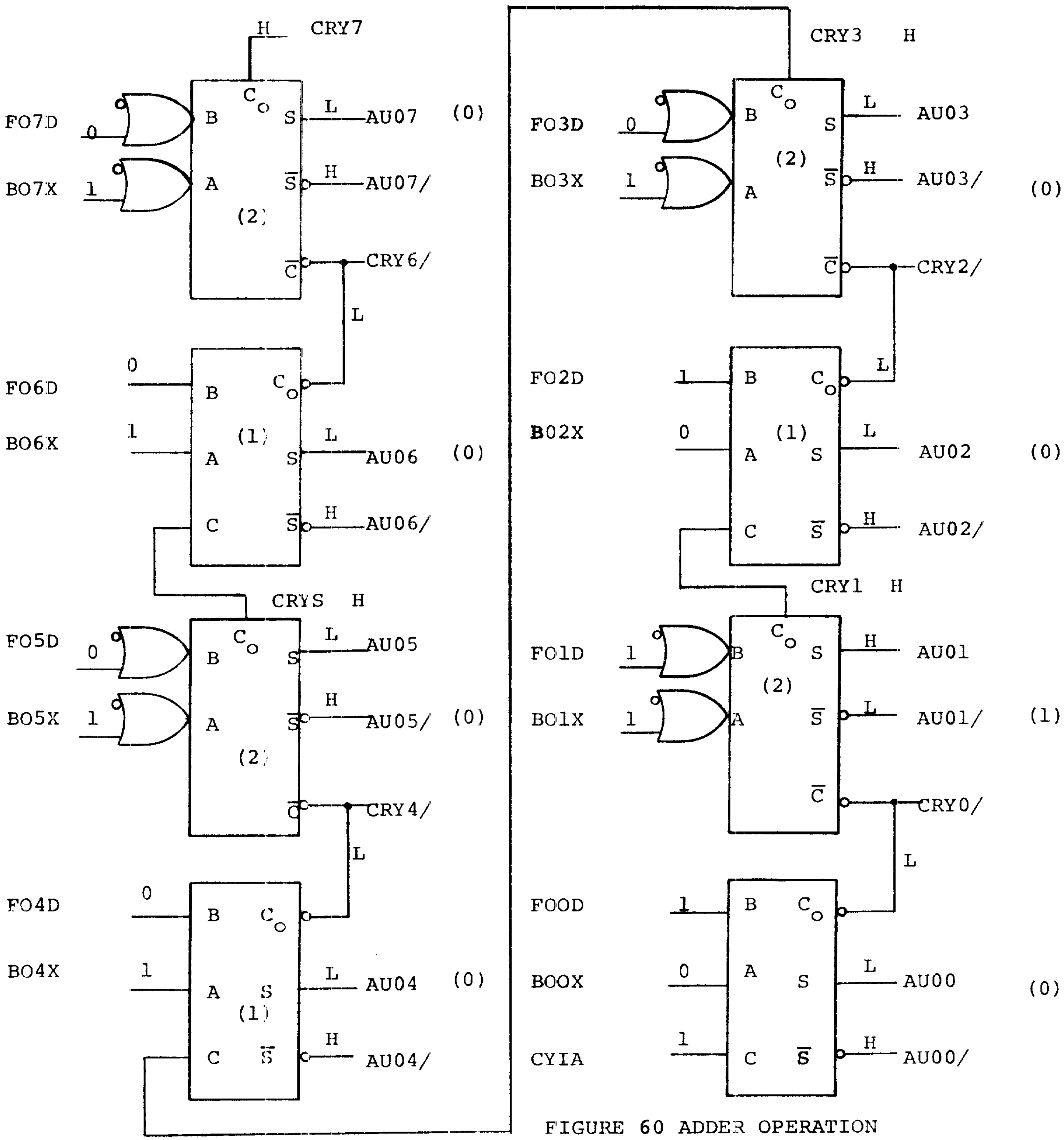


FIGURE 60 ADDER OPERATION

The adder true output shows the solution to the example problem to the 00000010 (=2).

AFLT is low and at the next clock pulse CCOX is not set. However, LINK is set.

As another example, suppose 9 were to be subtracted from 7. The selected file register contains the number 7 and the T register contains the number 9. Command 9 (SUBTRACT) is given with bit 5 a one bit, selecting T.

The adder true outputs become 1111 1110 indicating the remainder of 7-9 is -2.

In this case, AFLT is low, the condition code flip flop CCOX is not set and LINK is not set at the next CLK1/ clock pulse

3.5.3 A Bus

The A bus shown in Figures 61 and 62 is mechanized and functions under the following combination of control terms:

FUNCTION	CONTROL
EXCLUSIVE OR of F and B	XORX
Adder Output	ADDX
File Register Left Shift	SHIO and SHLX
File Register Right Shift	SHIO and SHRX
File Register Right Shift 4 bits	SHIO and ASRF
Sense Switches	SHIO and AENS
Internal Status	SHIO and AENI
AND of F and B	ANDX

The output of the A bus provides the input for the file logic and the M, N, T, U and L registers. The A bus, through element Z39, drives an NPN lamp driver transistor.

The four low order bits of the A bus are AND'ed to form AZ03, the zero detect term indicating those four bits are zeros. The four high order bits of the A bus are AND'ed to form AZ47/, the zero detect term indicating that A04X-A05X are zeros. AZ03/ and AZ47/ are used in the condition code flip flops to control the CC2X term and as a control on the RIN1 flip flop in the run control

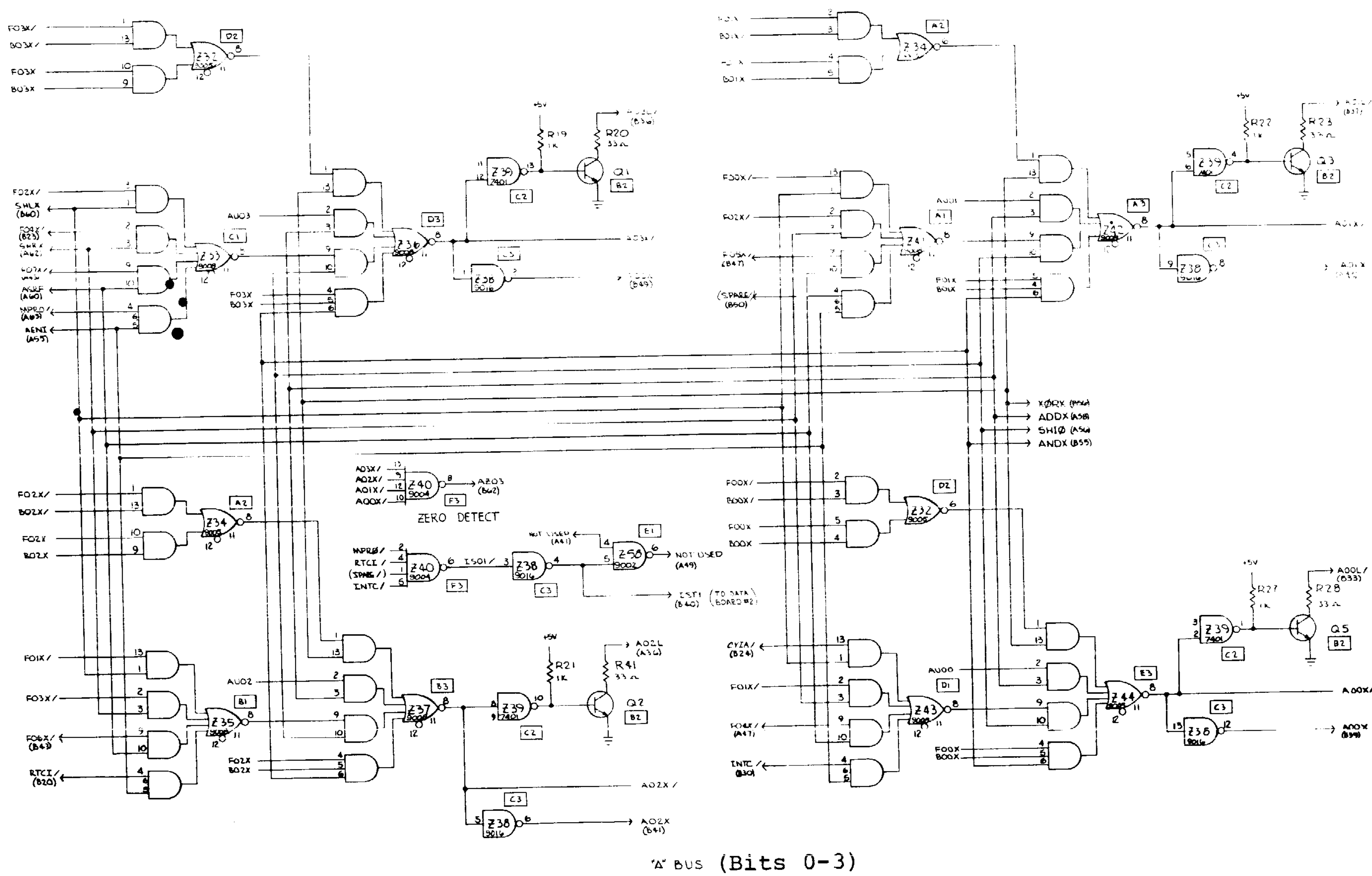
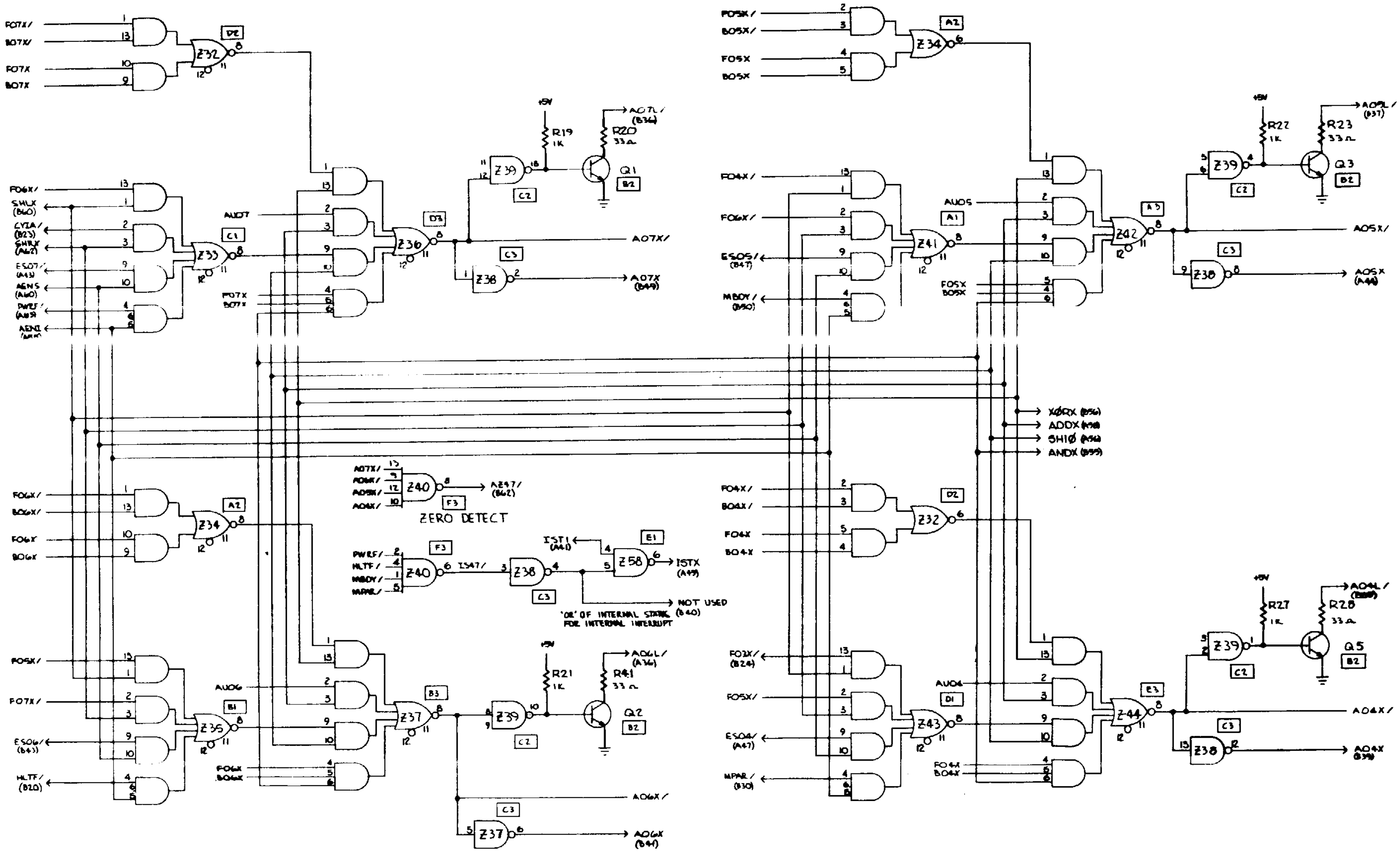


FIGURE 61

A-BUS BITS 0-3



'A' BUS (Bits 4-7)

FIGURE 62

A-BUS BITS 4-7)

circuitry. The internal status bits on Data Board No. 1 are AND'ed to form IST1, which is AND'ed with IS47, to form ISTX, a signal used to determine if any of the internal status bits is on.

3.5.4 File Registers

The four low order bits (0-3) of the file registers are generated on Data Board No. 1 (Figure 63) and the four high order bits (4-7) on Data Board No. 2 (Figure 64). Each 9033, 16-bit memory cell, is addressed by the X00X/ through X03X/ and Y00X/ through Y03X/, addressing lines.

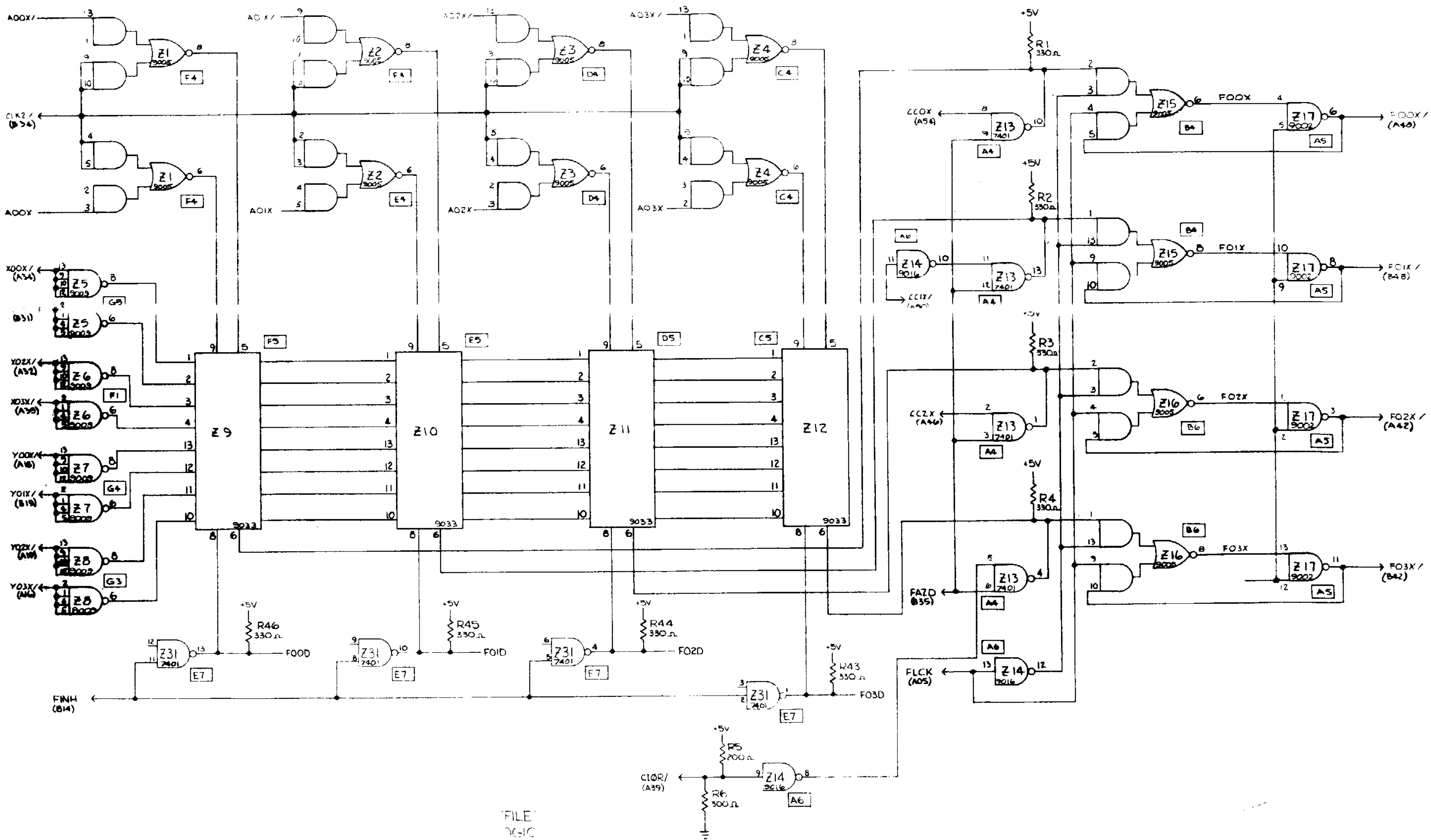
The data input to the file element originates with the A bus, and is clocked into the file element with the File Write Clock (CLK2/). When CLK2/ is a 0 (at ground potential), the true and complement A bus outputs are gated into the corresponding write terminals of the file element causing the addressed flip flops to be set in accordance with the A bus data.

When file register 0 is selected, the X addressing lines are prevented from going true (X00X/ through X03X/ are all true) thereby preventing a flip flop in the 9033 16-bit memory cell from being selected. Instead, the condition code flag flip flop states are collector OR'ed to file register 0 which is under control of FAZD.

The control term FLCK is used to control the latch on the output of the file. The timing diagram for FLCK is shown in Figure 65. When FLCK is false, the output of the memory cell is gated to the file register. The file output feedback is disabled. When FLCK becomes true, the memory cell output is disconnected as an input to the file register and the file register output is fed back and latched so that the data is retained while the memory cell is being written into.

Each memory cell has the term FINH collector OR'ed into its output. When FINH is true, the true output of the memory cell (Pin 8) is made false, so that the inputs to the Arithmetic Logic Unit (ALU) are all 0's. This occurs during the COPY T Command.

DATA BOARD #1 (J10)
1000196



(Bits 0-3)

FIGURE 63
FILE LOGIC BITS 0-3

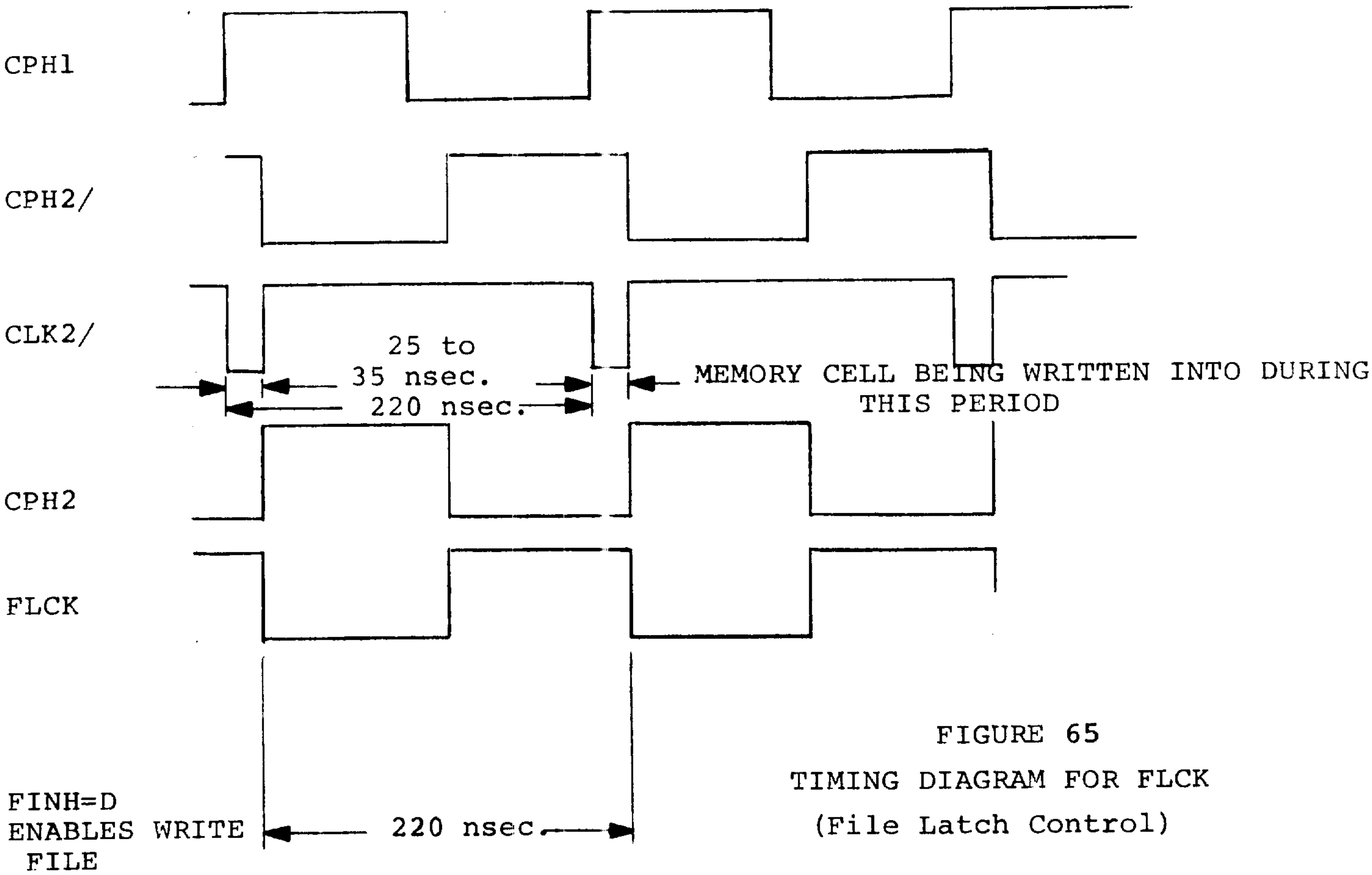


FIGURE 65

TIMING DIAGRAM FOR FLCK

(File Latch Control)

The true outputs of the memory cells are used for all ALU functions requiring the adder, including the COPY T command.

3.5.5 L Register

The L counter shown in Figure 66 is reset upon activation of the Master Reset signal, MRST/, resulting in an asynchronous input to the clear terminals of the flip flops. The flip flop outputs (L00X-L07X) are advanced under control of CPEN and clock CLK5/. Initially, or after MRST/ occurs, L00X-L07X are set to their zero states. At the first CLK5/ pulse and CPEN input at 0, L00X advances, starting the read only storage address counting, incrementing by one each clock pulse unless a jump command is being executed.

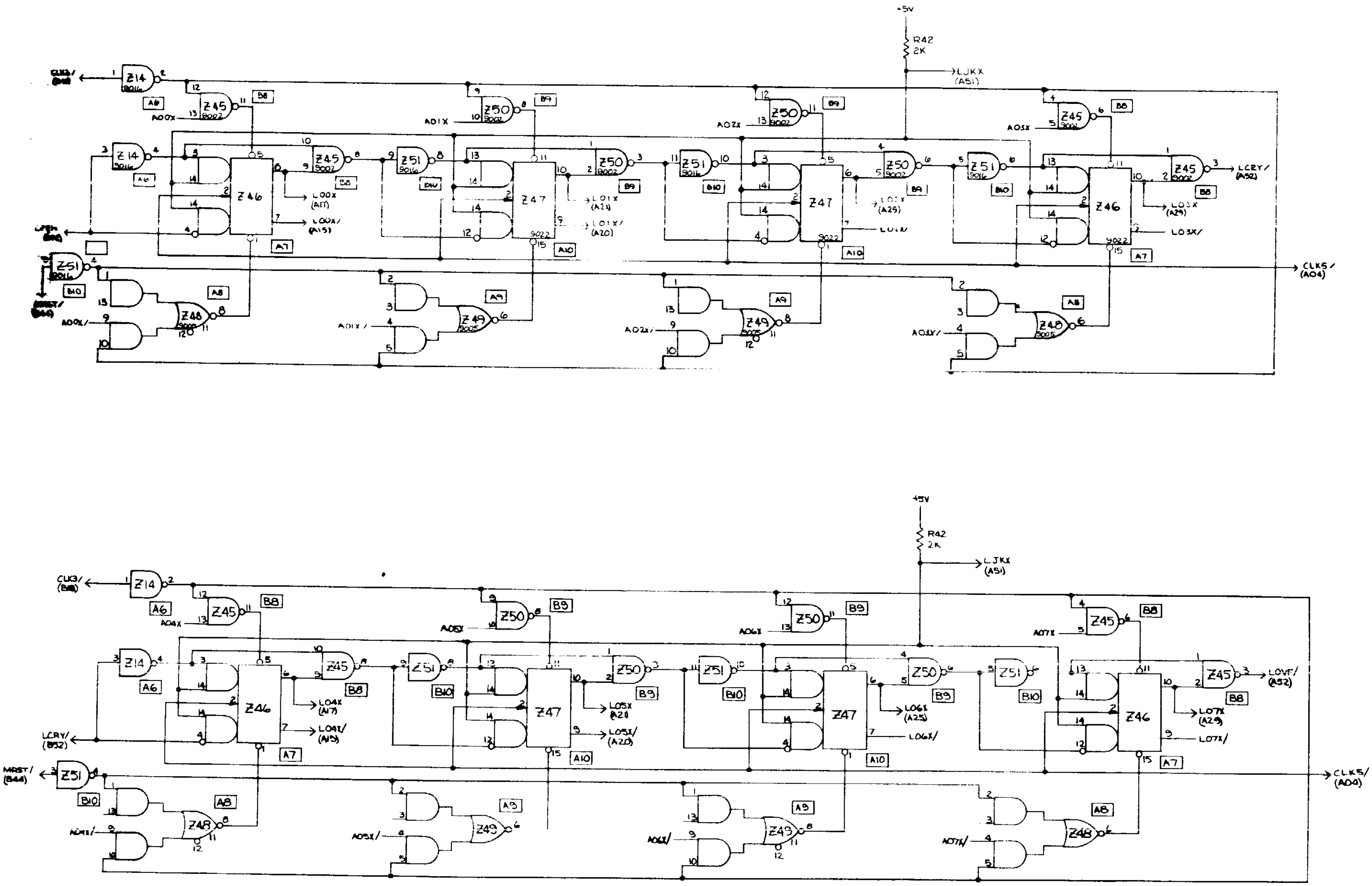


FIGURE 66

"L" LOGIC ROS ADDRESS COUNTER

The L counter is inhibited if LJKX is not true (goes to zero). If, CPEN, the control panel enable term is true, the L counter is disabled from advancing.

The counter has a direct set capability from a term generated by the logical combination of the A bus and the CLK3/ signal. CLK3/ is used to enable the A bus to set or reset the L counter flip flops for the jump command and when the L counter is the selected destination in the operate commands.

Bits 0-3 are located on Data Board No. 1 and bits 4-7 are located on Data Board No. 2. The carry term LCRY/, coming from Data Board No. 1, becomes the input to the section of the L counter located on Data Board No. 2.

The output states of the L counter flip flops go to the four read only storage boards and become the ROS address

L02X, L03X and L04X are decoded to select the row and L05X, L06X and L07X are decoded to select the column in the Read Only Store.

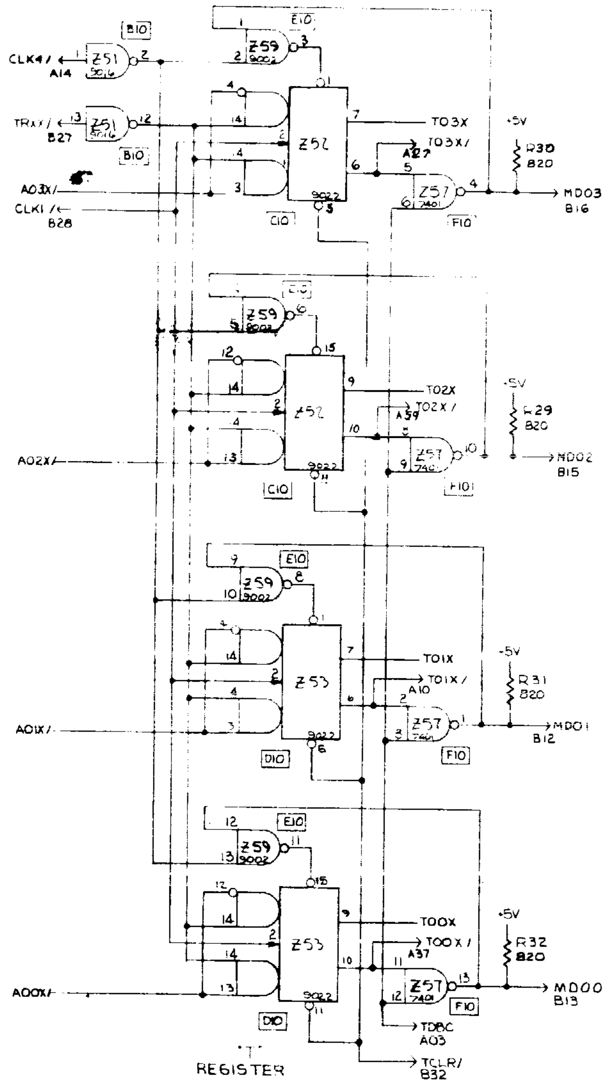
3.5.6 T Register

The T register shown in Figure 67 is directly reset (cleared) by the TCLR/ clock at the beginning of a memory read operation. The control term TRXX/, T register select, becomes zero under command one thereby enabling flip flops Z52 and Z53. When TRXX/ enables the R register, the A bus data and CLK1/ are used to establish the output states of the flip flops. The information on the memory data bus (MD00 through MD07) is used to set the T register flip flops under CLK4/ control, during a memory read operation. The complement output of the T register is used internally as the output bus and is under control of TDBC to the memory data bus. The T register is gated onto the data memory bus at all times except during a DMA memory operation and a memory read operation.

The T register is divided on the two data boards T00X through T03X on Data Board No. 1 and T04X through T07X on Data Board No. 2.

DATA BOARD #1 (J10)

1000196



DATA BOARD #2

1000273

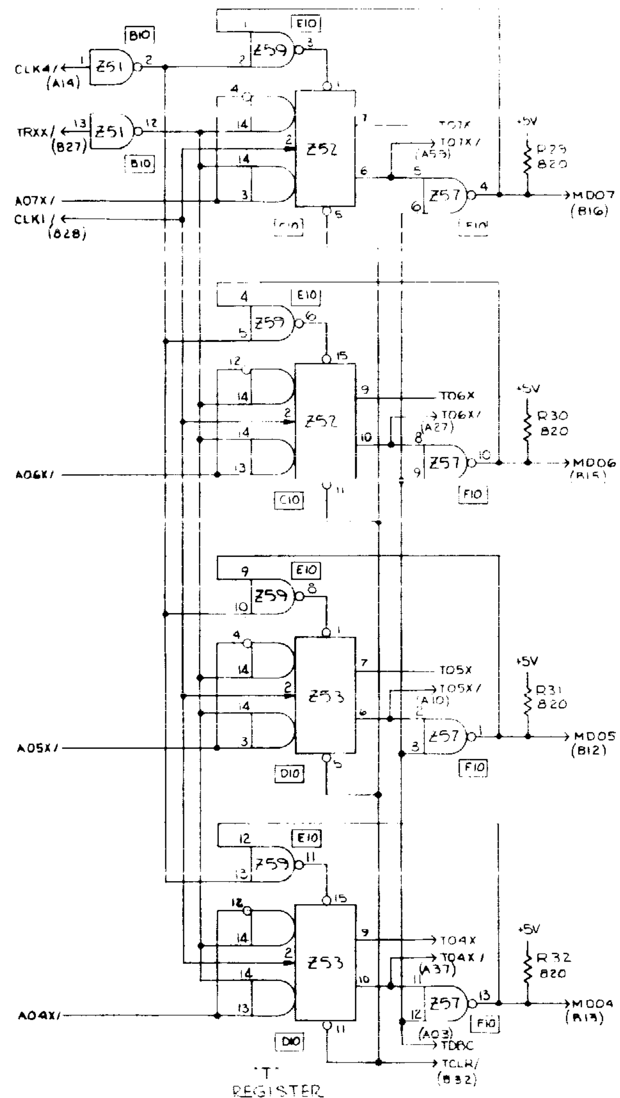


FIGURE 67

T-REGISTER

3.5.7 Memory Address Registers

The memory address register is divided into two sections located on Data Boards 1 and 2. The M and N registers shown in Figure 68 are the memory address register outputs. Each is an eight bit register. The low order bits (0-3) of both M and N are on Data Board No. 1 and the high order bits (4-7) on Data Board No. 2. The contents of the registers are generated by the output of a 9308 dual latch element which receives its input from the A bus. The dual latch is clocked by CLK1/ and is enabled by NRXX/ and MRXX/. The inputs to the M and N registers are enabled by the DMAS control term and form the core memory address bus. The term DMAS is false when a DMA memory operation is in progress, thus disabling the M and N registers from driving the memory address bus.

3.6 ROS BOARD

3.6.1 Word Select Decoder and Drivers

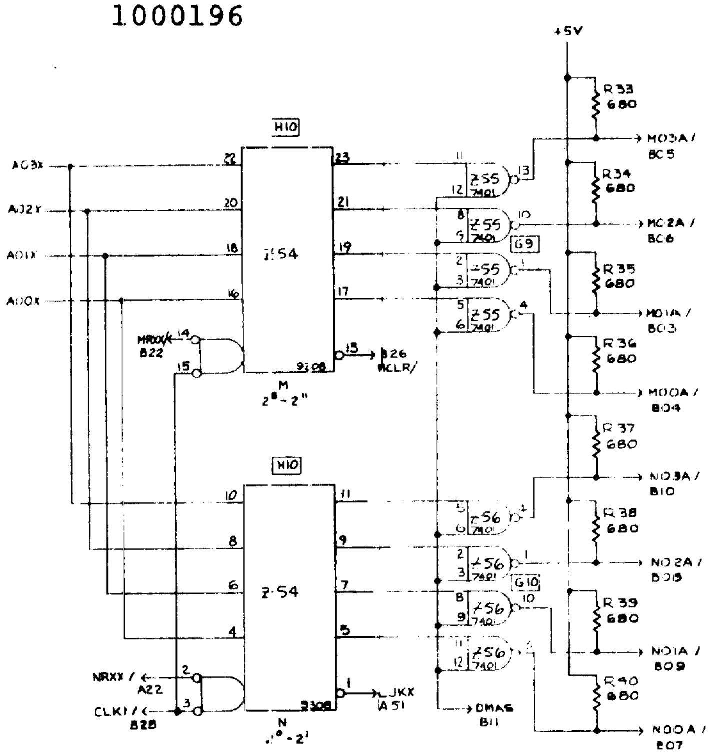
The address stored in the L register is decoded by separate word, row and column decoders located on the ROS Board. Each decoder decodes a portion of the address code.

The diode matrix of the read only store module is actually a 64 x 4 x 16 matrix. The 64 refers to lines, the 4 refers to words and the 16 refers to bits.

The four words of the diode matrix (WDO through WD3) as shown in Figure 69, are decoded from the least two significant bits of the L register after being enabled by the control term ENAB/.

These bits and their complements are applied to the word decoder which is divided into four separate sections, one for each word. Each section consists of a conventional AND-NOR logic and a pair of transistors arranged to form a non-inverting driver. This logic scheme was chosen for speed considerations and low power drain when the decoder is disabled by the enable signal (ENAB) from the block enable section. It should be noted that an individual word is selected or

DATA BOARD #1 (J10)
1000196



DATA BOARD #2 (J12)
1000273

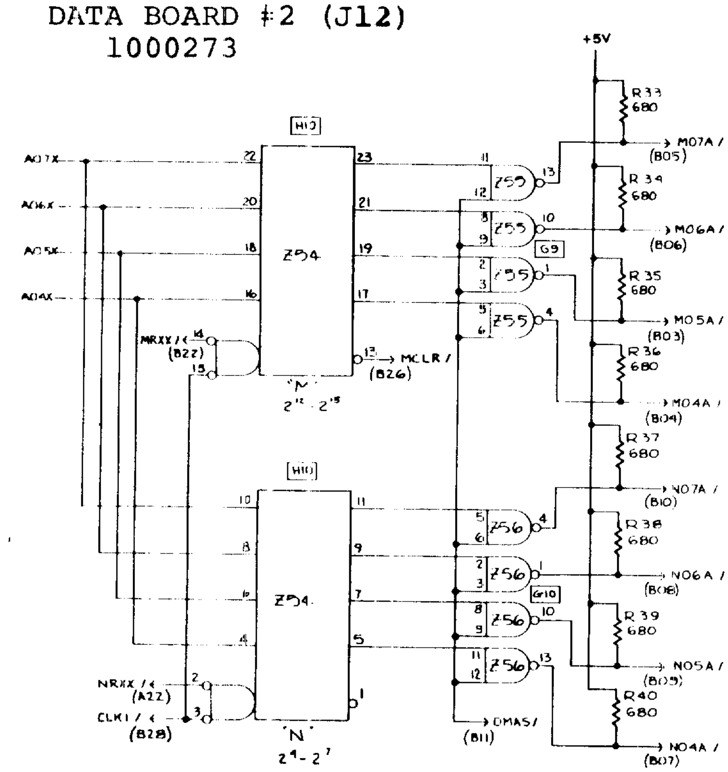


FIGURE 68

MEMORY ADDRESS REGISTERS

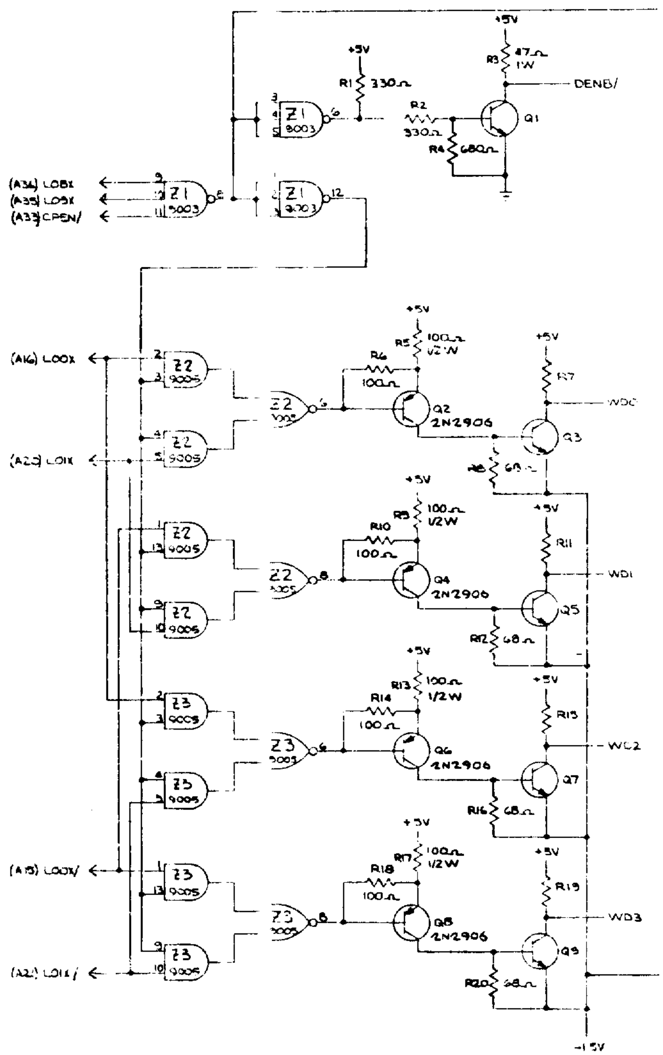


FIGURE 69

ROS DIODE MATRIX WORD SELECT

true when both input address bits are false and the enable signal is true. A truth table for the word select decoder is given in Table 7.

TABLE 7. TRUTH TABLE FOR WORD SELECT DECODER

ENAB	L01X	L00X	WD0	WD1	WD2	WD3
0	0	0	1	1	1	1
0	0	1	1	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

3.6.2 Row Decoder and Drivers

The row decoder and drive circuit along with the column decoder and drive circuit, both shown in Figure 70, are used to select a particular line driver within the line driver matrix.

The row decoder and driver section consists of a 1 of 10 decoder and 8 individual inverting drivers.

The decoder accepts four active high inputs and provides ten mutually exclusive active low outputs, only the first eight least significant outputs are used. The most significant input of the decoder is used as an inhibit function when the read only store module is not being addressed or the control panel enable switch is selected. The three least significant inputs to the decoder are bits 2, 3, and 4 of the L register.

The signal at the most significant input is ENAB/ which originates in the block enable section.

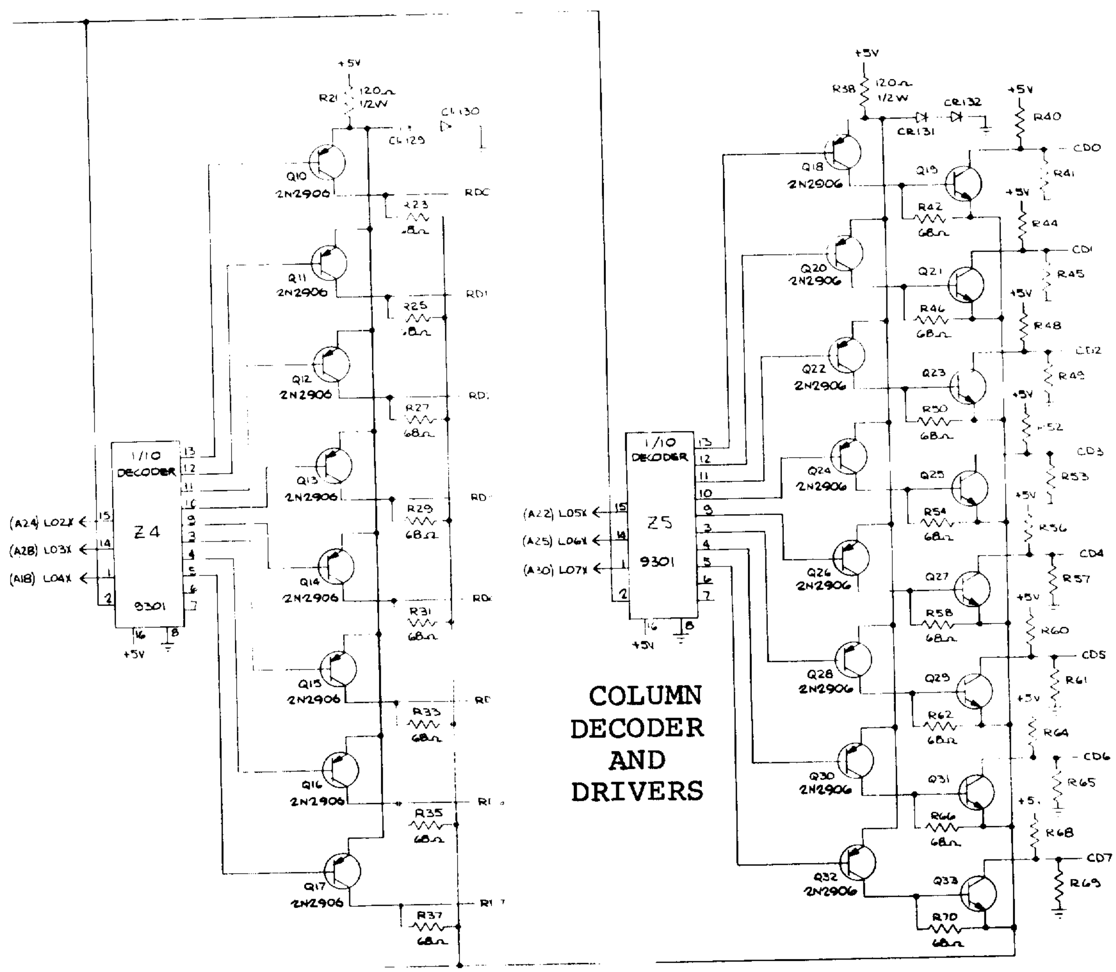


FIG. 70 - ROW DECODER AND DRIVERS

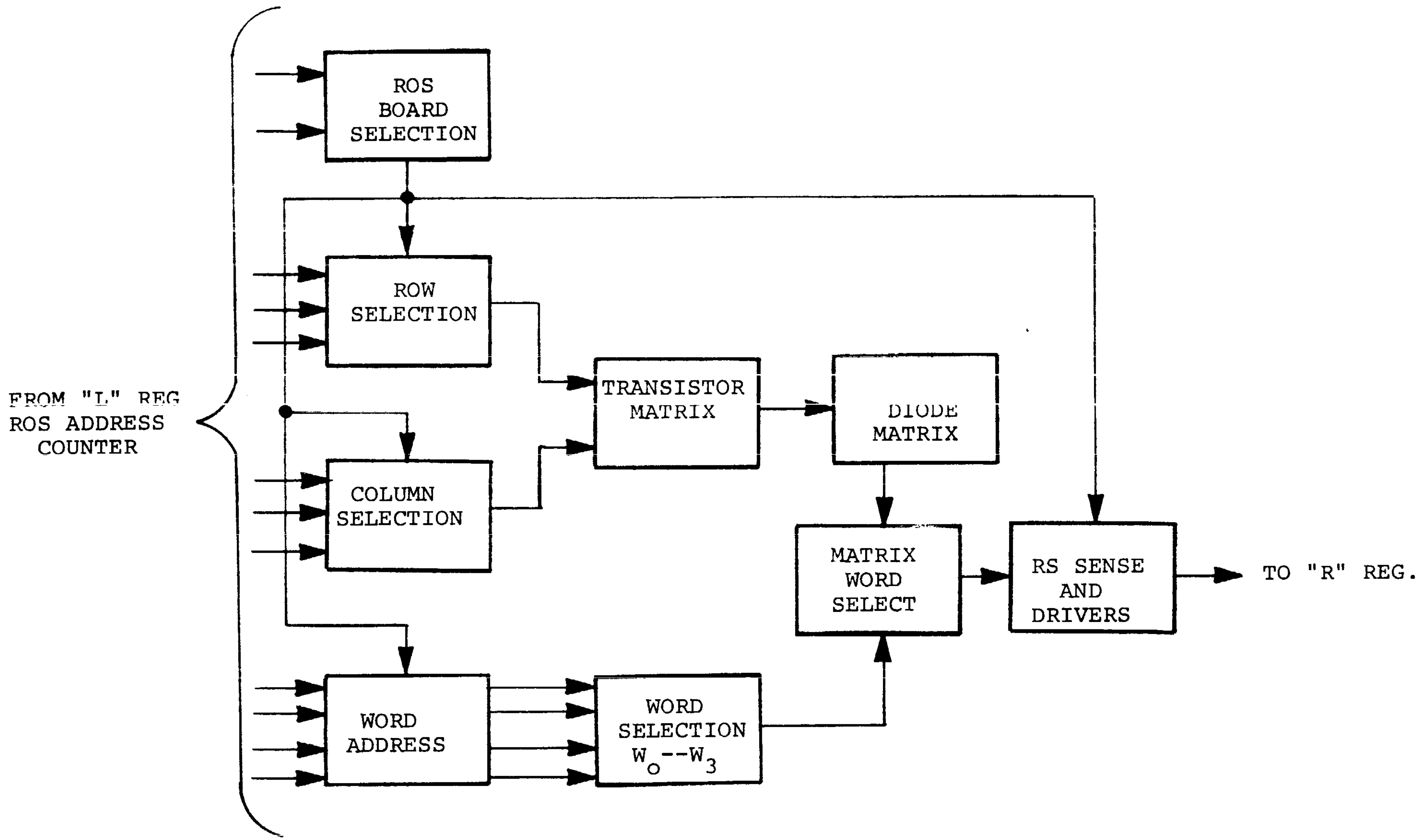

ROS
BOARD
SELECTION
ROW
SELECTION
FROM "L" REG
ROS ADDRESS
COUNTER
COLUMN
SELECTION
WORD
ADDRESS
TRANSISTOR
MATRIX
DIODE
MATRIX
MATRIX
WORD
SELECT
WORD
SELECTION
W_O--W₃
RS SENSE
AND
DRIVERS
TO "R" REG.

FIGURE 70-A

3.6.3 Column Decoder Driver

The column decoder and driver selects a particular line driver within the line driver matrix.

The column decoder and driver circuits consist of a 1 of 10 decoder and 8 individual non-inverting drivers.

The inputs to the decoder are bits 5, 6, and 7 of the L register and the enable signal from the block enable circuit.

The decoder accepts the four active high inputs and provides mutually exclusive active low outputs. The outputs of the decoder are then amplified by pairs of transistors arranged to form non-inverting drivers. This logic scheme reduces the power drain when the decoder is disabled either because of address bits in or the block enable signal. The truth table for the column decoder and driver circuit is given in Table 8.

3.6.4 ROS Transistor Matrix, Diode Word Sense and RS Drivers

a. Line Driver Matrix and Drivers

The line driver matrix consists of 64 transistor drivers arranged in rows and columns as shown in Figure 71. To each driver are connected the following two lines:

(1) a column drive line which connects to all drivers in the same column
(2) a row drive line which connects to all drivers in the same row

The column drive line is a ground true (OV) drive line when active. Each column drive line, of which there are eight, is connected to the emitter of eight transistors.

The row drive line is a positive true (+5V) drive line when active. Each row drive line, of which there are eight, is connected to the base of eight transistors. The presence of only an active row drive line or an active column drive line at an individual driver is half the requirement for turning the driver on.

INPUTS				OUTPUTS							
ENAB	L07X	L06X	L05X	CD0	CD1	CD2	CD3	CD4	CD5	CD6	CD7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1

TABLE 8. TRUTH TABLE FOR COLUMN DECODER AND DRIVERS

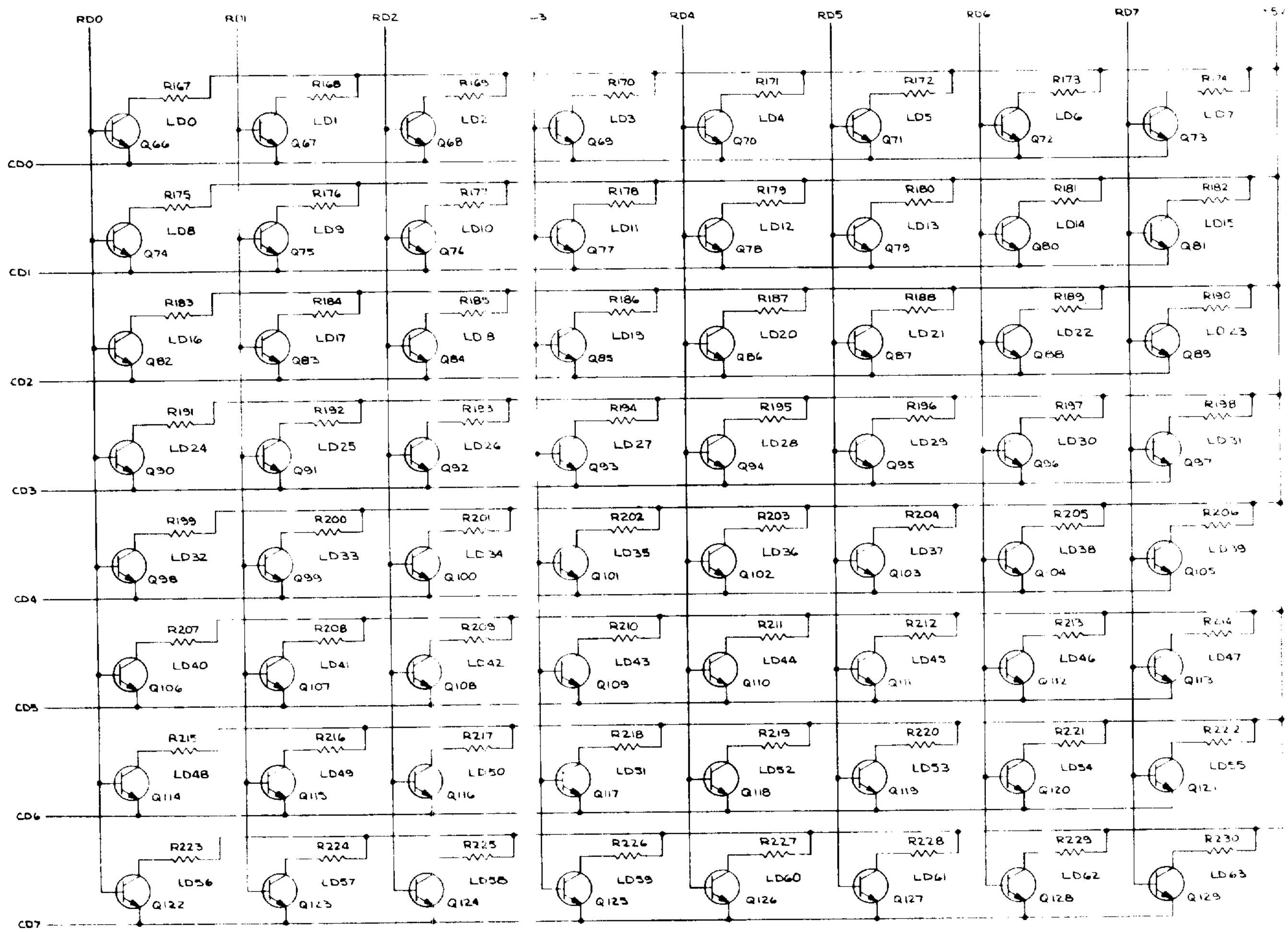


FIGURE 71

ROS LINE DRIVER MATRIX

However, the presence of both active drive lines at an individual driver will provide forward bias to the transistor, turning it on to ground.

Only one driver at a time in this 8 x 8 matrix will be selected (forward biased). Fifteen (15) other drivers will be ready, with only half the requirements present, to be turned on.

The line driver outputs are used in the diode matrix to select 1 of 64 lines in this array.

b. Diode Matrix

The diode matrix consist of drive lines and sense lines with diodes at the intersections where a one is required and no diode at those intersections requiring a zero.

The diode matrix is a 64 x 4 x 16 matrix. The 64 refers to lines, the 4 refers to words and the 16 refers to bits. The total number of words for the matrix is 256. The total number of bits is 4096.

The diode matrix is arranged in lines and sense lines. To each diode are connected the following two lines:

(1) a line select drive line which connects to all diodes in the same line
(2) a sense line which connects to all diodes in the same sense line.

The line select drive line is a ground true (OV) drive line when active. Each drive line, of which there are 64, is connected to the cathode of the diodes. Any number of diodes from 0-64 may be connected to these individual drives.

There are four sense lines for each data bit and sixteen data bits giving a total of 64 separate sense lines. The sense lines for each data bit are enabled separately depending on the word being selected. The possible number of diodes connected to any one sense line range from 0-64.

With a word selected, which selects 16 sense lines, one for each data bit, the diodes in each selected sense line has a positive voltage applied to its anode. This is only half the requirement for a forward biased diode. It is possible to have as many as 1024 diodes in this half selected condition. The other requirement for a forward biased diode is provided by the line select drive line when 1 of 64 of these drive lines goes to 0V or active state. This line along with the sense lines selected will forward bias one data word consisting of up to 16 diodes.

c. Sense Amplifiers and Output Drivers

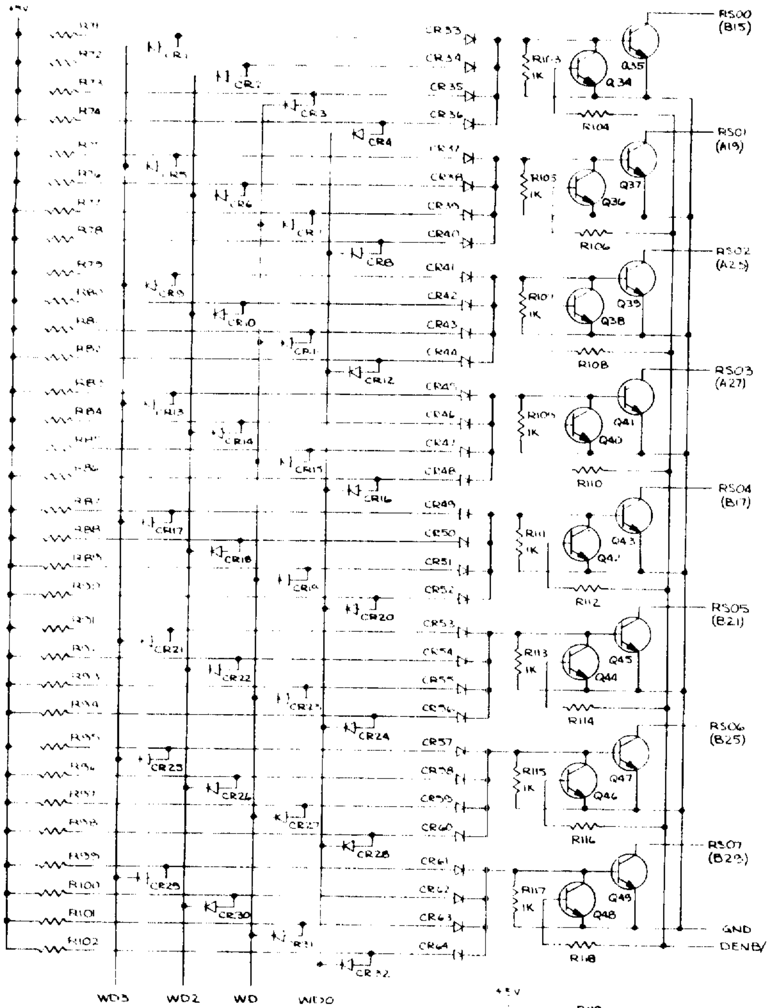
There is a sense amplifier and output driver for each bit in the data word as illustrated in Figure 72.

There are four words exclusively selectable for each sense amplifier and output driver.

The diodes with the word driver outputs connected to their cathodes are used to enable the sense lines. When a particular word is selected, the selected word driver output goes to a positive voltage where as the non-selected word driver outputs go to zero volts. This zero volts on the non-selected diodes provides a forward bias on these diodes clamping the sense lines to ground.

The selected word puts a reverse bias on its diode allowing the sense line to be enabled. The selected sense line will now take on a voltage level dependent upon the presence or absence of the diode in the diode matrix which is selected for this bit. If a diode exists in the diode matrix it will be forward biased, clamping the sense line to 0 volts. If no diode is present, the sense line remains at a positive voltage. For the condition, a diode exist in the diode matrix for the selected sense line the output driver is not properly biased, thus not conducting, allowing the output to go true or positive.

For the condition a diode is not present in the diode matrix for the selected sense line the output driver is forward biased, clamping



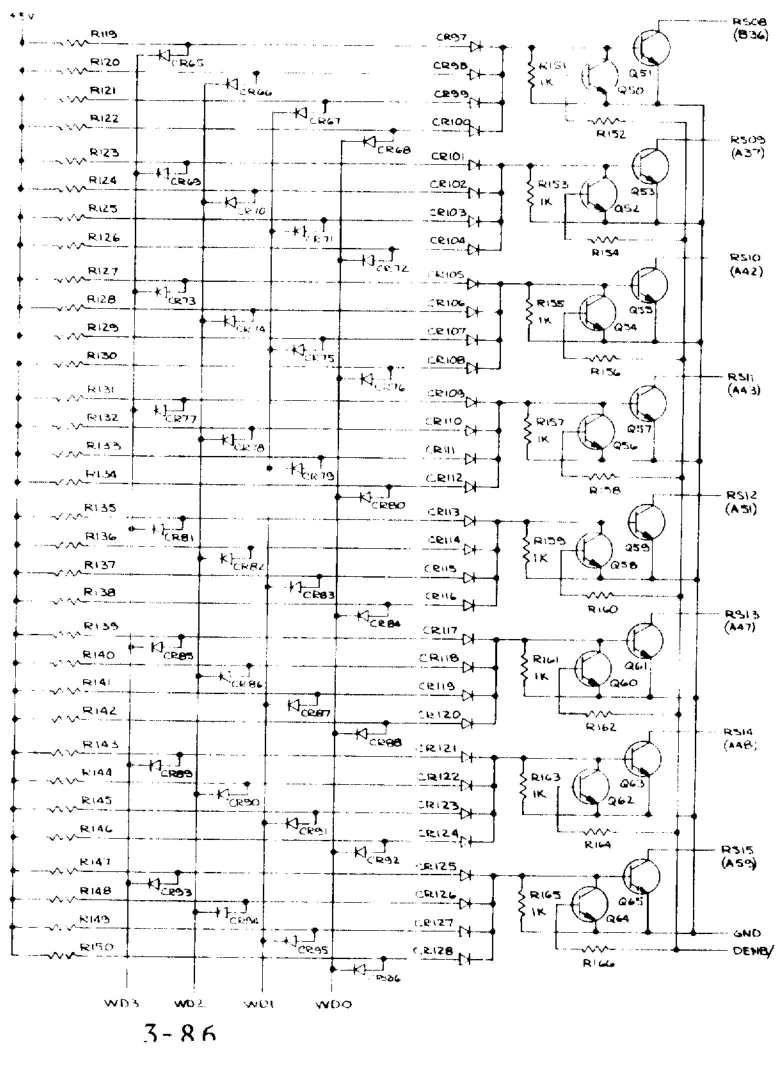


FIGURE 72

SENSE AMPLIFIER
AND
OUTPUT DRIVER
ROS CIRCUITRY

the output line to zero volts. To these output lines are connected the control panel switches, through a logic network, to simulate the read only store. When the control panel switches are enabled the signal ENAB/ goes positive switching on a transistor which inhibits the output driver from ever turning on.

3.7 MEMORY

3.7.1 General

Information is stored in an array of lithium ferrite cores. Each core may be set to one of two possible magnetic states thereby representing one bit of binary information. Nonvolatile storage is made possible by the core B-H characteristics which describe a near-rectangular hysteresis loop. The binary state of the core is defined by the polarity of flux within the core (see Figure 73).

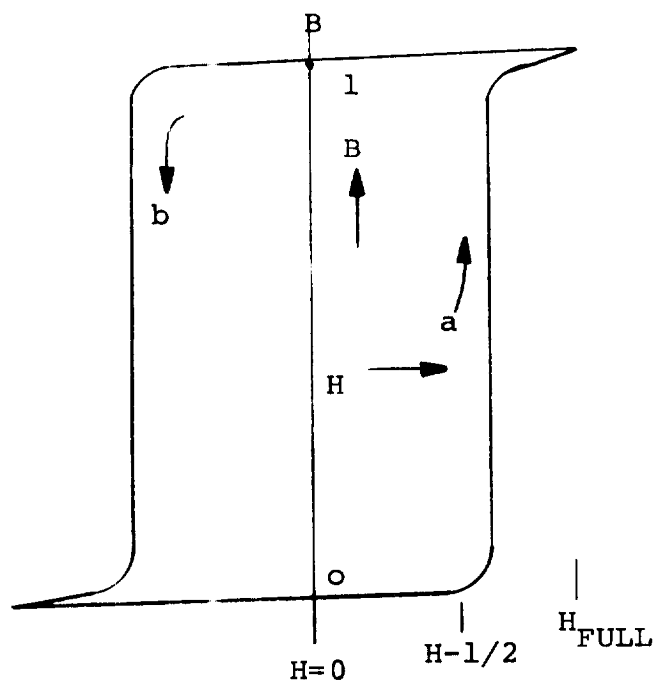


FIGURE 73

TYPICAL CORE CHARACTERISTIC

H is the magnetizing force proportional to current linking the core.

B signifies magnetic flux density within the core. These two quantities are related as shown in Figure 73. For example, if a core is initially in state 0, as magnetizing force is increased, B is slightly affected until H approaches $H_{\frac{1}{2}}$. As H increases from $H_{\frac{1}{2}}$ to H_{FULL}, total flux reversal occurs (path a). At H_{FULL} the core may be considered saturated in the opposite state such that an additional increase in H cannot significantly alter B. Irreversibility is shown by the fact that, as H is relaxed from H_{FULL} to 0, B returns to state 1 rather than starting point 0. However, state 0 can again be realized by applying sufficient H of opposite polarity to traverse path b.

The threshold characteristic of the device allows its use in a coincident-current selection scheme such as that shown in Figure H. Each core in the array is linked by an X and Y drive line. The current magnitude of one Y line or one X line corresponds to $H_{\frac{1}{2}}$ and their sum corresponds to a field exceeding H_{FULL}. Currents entering from opposite sides will have mutually cancelling fields resulting in $H = 0$. Write currents have the same amplitude but opposite polarity as do read currents.

During a Write Operation:

> (i.e. the second half of a Read/Restore, Clear/Write full cycle or a Write half cycle)

One X-Drive line will carry half current in the direction noted as Ixw.

One Y-Drive line will carry half current in the direction noted as Iyw.

The core at the intersection of the 2-Drive lines will switch to the state defined as a zero, unless INHIBIT current is also flowing.

If inhibit current is on it will oppose the Y-Drive current, effectively cancelling it. The net current will be Ixw half current which will not switch the core. This condition is defined as the One state.

The source for X and Y Drive current selection is the address provided by the computer. X and Y

Drive currents shown in Figure 74 are active in both the read and the write operations (although in reverse direction) inhibit current is only active in the write operation, and then only if the binary bit to be written is a ONE.

4096 Bit Array:

There are 64 X-Drive Lines $X_0 \rightarrow X_{63}$

There are 64 Y-Drive Lines $Y_0 \rightarrow Y_{63}$

A single sense and inhibit line threads through all 4096 cores in the fashion shown in Figure H.

Read and write operations are as described for the 16 bit ARRAY.

Figure 74 represents a 16 bit array.

Only 16 cores are shown in a 4 x 4 matrix. The important characteristics, however, are extandable to the full 64 x 64 matrix of 4096 cores. Operation will be described for the 16 bit array then extended to the full array.

There are 4 X-Drive Lines - X_0, X_1, X_2, and X_3 and

4 Y-Drive Lines - Y_0, Y_1, Y_2, and Y_3

A single sense and inhibit line threads through all 16 cores in a manner to minimize noise accumulation during sensing.

During a Read Operation:

(i.e. the first half of a Clear/Write, or Read/Restore full cycle or a Read half cycle)

One X-Drive line will carry half current in the direction noted as I_{xr}.

One Y-Drive line will carry half current in the direction noted as I_{yr}.

If the coincidence of the two half currents at their intersection causes the core to switch, the flux change will induce current in the sense and inhibit winding. This flux change will be interpreted in the Micro 800 as a binary <u>zero</u>. No flux change would signal a binary ONE.

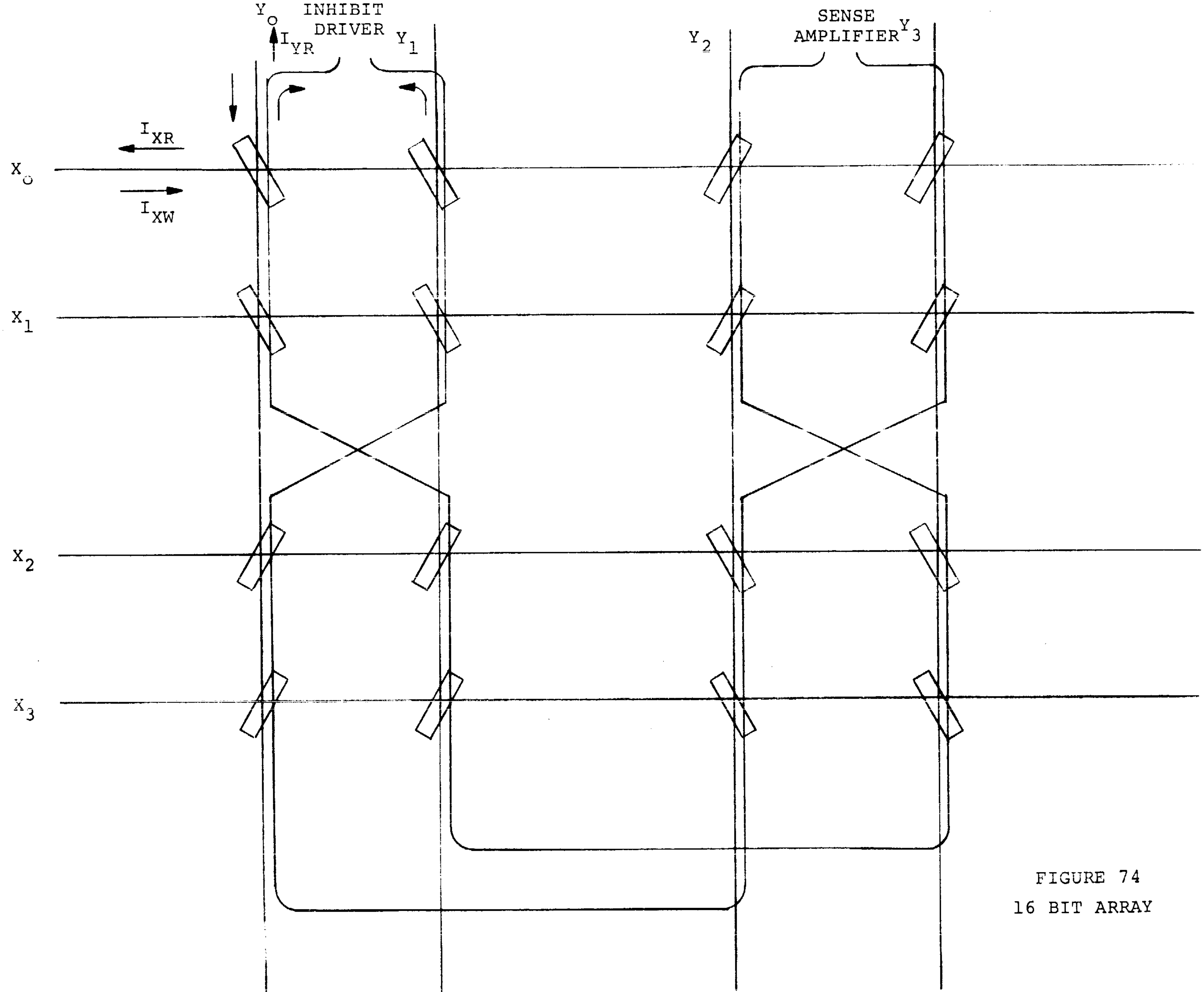


FIGURE 74
16 BIT ARRAY

The computer communicates address information to all memories via 15 address lines from the M and N registers. This allows addressing of up to 32,768 byte locations.

Three upper bits are used for memory unit selection and the lower 12 bits are decoded into individual byte locations within the unit. Bit significance and relationship between memory and central processor are shown in the following table.

	Processor	Memory	Significance	
Bit 00	N00A/	M00A/	2^0	
01	N01A/	M01A/	2^1	
02	N02A/	M02A/	2^2	
03	N03A/	M03A/	2^3	
04	N04A/	M04A/	2^4	
05	N05A/	M05A/	2^5	
06	N06A/	M06A/	2^6	
07	N07A/	M07A/	2^7	
08	M00A/	M08A/	2^8	
09	M01A/	M09A/	2^9	
10	M02A/	M10/	2^{10}	
11	M03A/	M11A/	2^{11}	
12	M04A/	M12A/	2^{12}	unit select
13	M05A/	M13A/	2^{13}	unit select
14	M06A/	M14A/	2^{14}	unit select

(N00A/ indicates the least significant bit of the N register, the slash "/" denotes the negation of the term.)

There are four identical decoders

2 for X and Y Drivers

2 for X and Y Sinks

Each decoder operates on 3 bits producing 8 outputs, only 1 of which is active at any one time.

Bits 0, 1, 2, are decoded into 8 lines which are routed to 16 drivers. Half are for read and half are for write. The 16 outputs are called XRD0 - XRD7 and XWD0 - XWD7. Bits 3, 4, 5, are decoded into 8 lines which enable current sinks. The current sinks are called XS0 - XS7. Each current sink is connected to 8 X Drive lines.

The process of driving current through a X line is:

Address bits 0, 1, and 2 and the read or write selection pick one of 16 current drivers. A corresponding sink is selected by address bits 3, 4, and 5. The X line which is common to both Driver and Sinks is the one which will carry X half current.

A similar activity takes place to find a Y Drive line using bits 6-11.

(Bits 6, 7, and 8 for Y Drivers and bits 9, 10, and 11 for Y Sinks.)

At the coincidence of the X and Y Drive lines, each carrying half current, is one core in each bit plane. The direction of current flow depends on whether read drivers or write drivers have been selected. This one core of 4096 in each plane has received full switching current in one direction (without considering the sense and inhibit line).

3.7.2 X-Y Sink and Drive Circuits

The X-Y sink and drive circuits contain four identical decoders as shown in Figure 75. Two for the X and Y drivers and 2 for the X and Y sinks. Each decoder operates on 3 bits producing 8 outputs, only one of which is active at any one time. Bits 0, 1 and 2 are decoded into 8 lines which are routed to 16 drivers. Half are for read, the other half for write. The 16 outputs are termed RD0X-RD7X and WD0X-WD7X. Bits 3, 4 and 5 are decoded into 8 lines which enable current sinks. The current sinks are termed

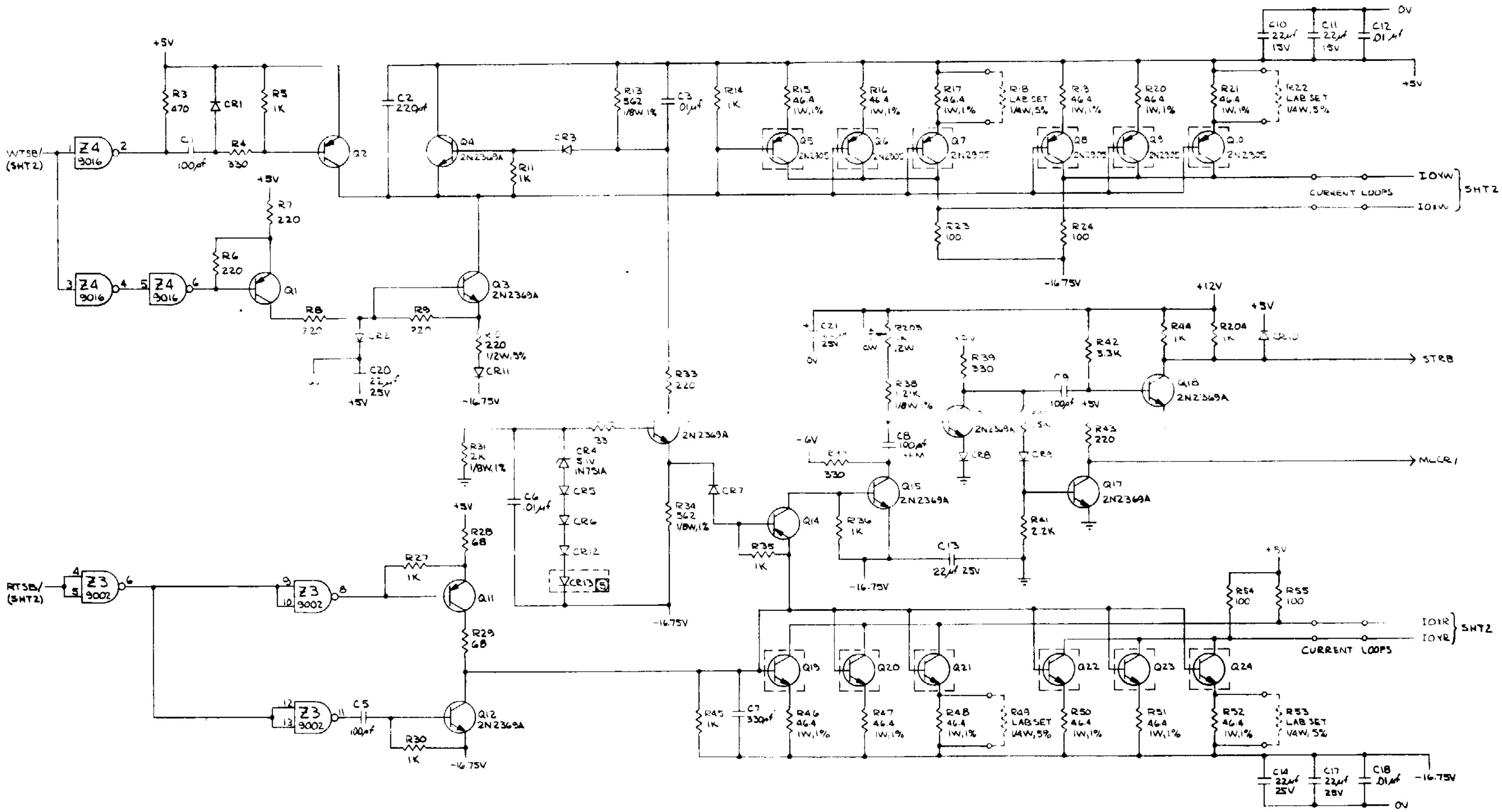


FIGURE 74

X AND Y DRIVE CURRENTS (LOOPS)

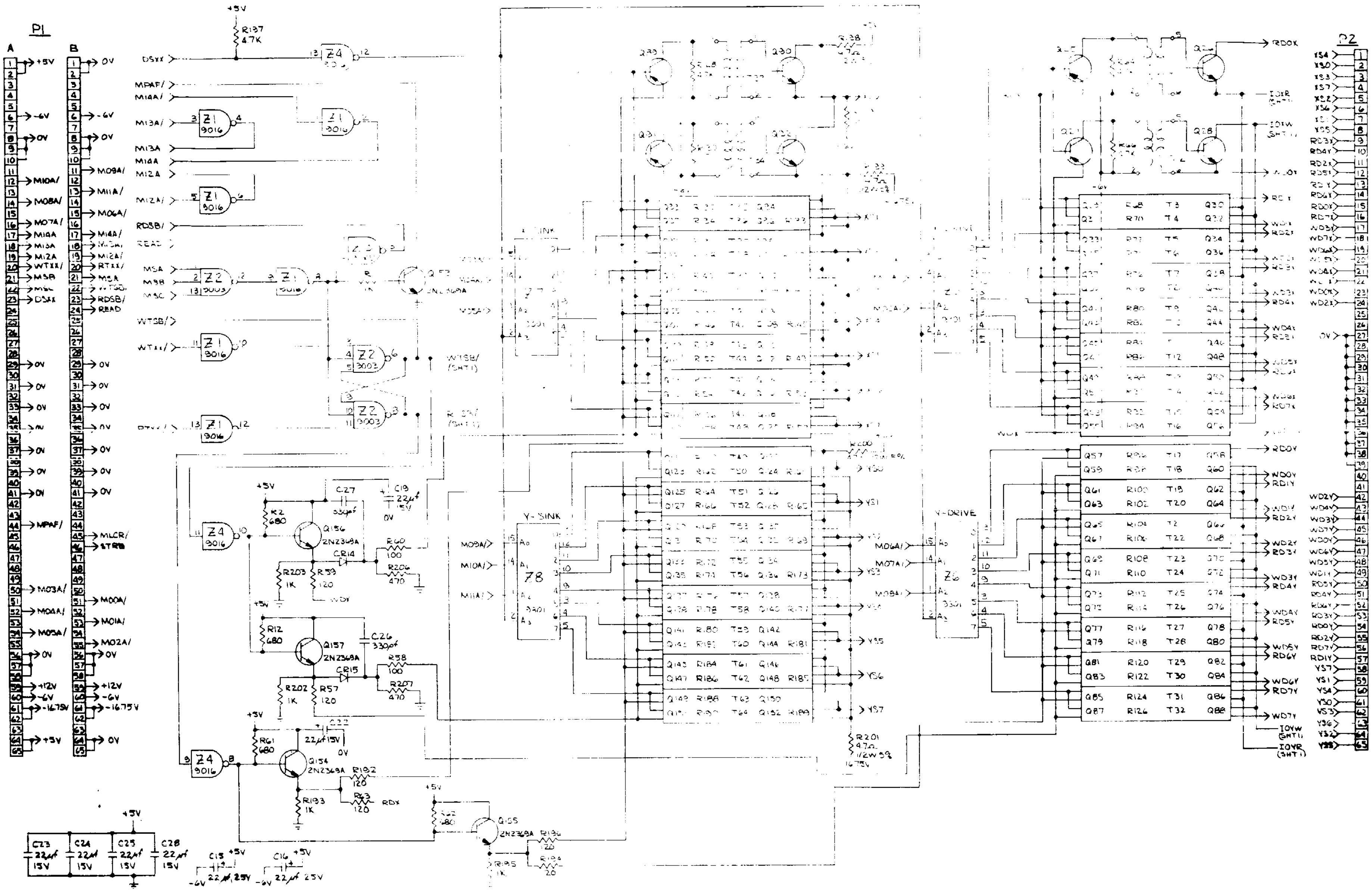


FIGURE 75

X-Y SINK AND DRIVE CIRCUITS

X READ/WRITE DRIVERS

ADDRESS $\overline{2}$ $\overline{1}$ $\overline{0}$	READ DRIVER	WRITE DRIVER
0 0 0	XRD0	XWD0
0 0 1	XRD1	XWD1
0 1 0	XRD2	XWD2
0 1 1	XRD3	XWD3
1 0 0	XRD4	XWD4
1 0 1	XRD5	XWD5
1 1 0	XRD6	XWD6
1 1 1	XRD7	XWD7

X DRIVE LINE

2	6	10	14	18	22	26	30
3	7	11	15	19	23	27	31
62	58	54	50	46	42	38	34
63	59	55	51	47	43	39	35
0	4	8	12	16	20	24	28
1	5	9	13	17	21	25	29
60	56	52	48	44	40	36	32
61	57	53	49	45	41	37	33

X SINKS ADDRESS 5 4 3	SINK
0 0 0	X S 0
0 0 1	X S 1
0 1 0	X S 2
0 1 1	X S 3
1 0 0	X S 4
1 0 1	X S 5
1 1 0	X S 6
1 1 1	X S 7

TABLE 9

X DECODING AND DRIVE LINE SELECTION

Y READ/WRITE DRIVERS

ADDRESS $\overline{8}$ $\overline{7}$ $\overline{6}$	READ DRIVER	WRITE DRIVER
0 0 0	YRD0	YWD0
0 0 1	YRD1	YWD1
0 1 0	YRD2	YWD2
0 1 1	YRD3	YWD3
1 0 0	YRD4	YWD4
1 0 1	YRD5	YWD5
1 1 0	YRD6	YWD6
1 1 1	YRD7	YWD7

Y DRIVE LINES

0	4	8	12	16	20	24	28
1	5	9	13	17	21	25	29
2	6	10	14	18	22	26	30
3	7	11	15	19	23	27	31
60	56	52	48	44	40	36	32
61	57	53	49	45	41	37	33
62	58	54	50	46	42	38	34
63	59	55	51	47	43	39	35

Y SINKS

ADDRESS $\overline{11}$ $\overline{10}$ $\overline{9}$	
0 0 0	Y S 0
0 0 1	Y S 1
0 1 0	Y S 2
0 1 1	Y S 3
1 0 0	Y S 4
1 0 1	Y S 5
1 1 0	Y S 6
1 1 1	Y S 7

TABLE 10

Y DECODING AND DRIVE SELECTION

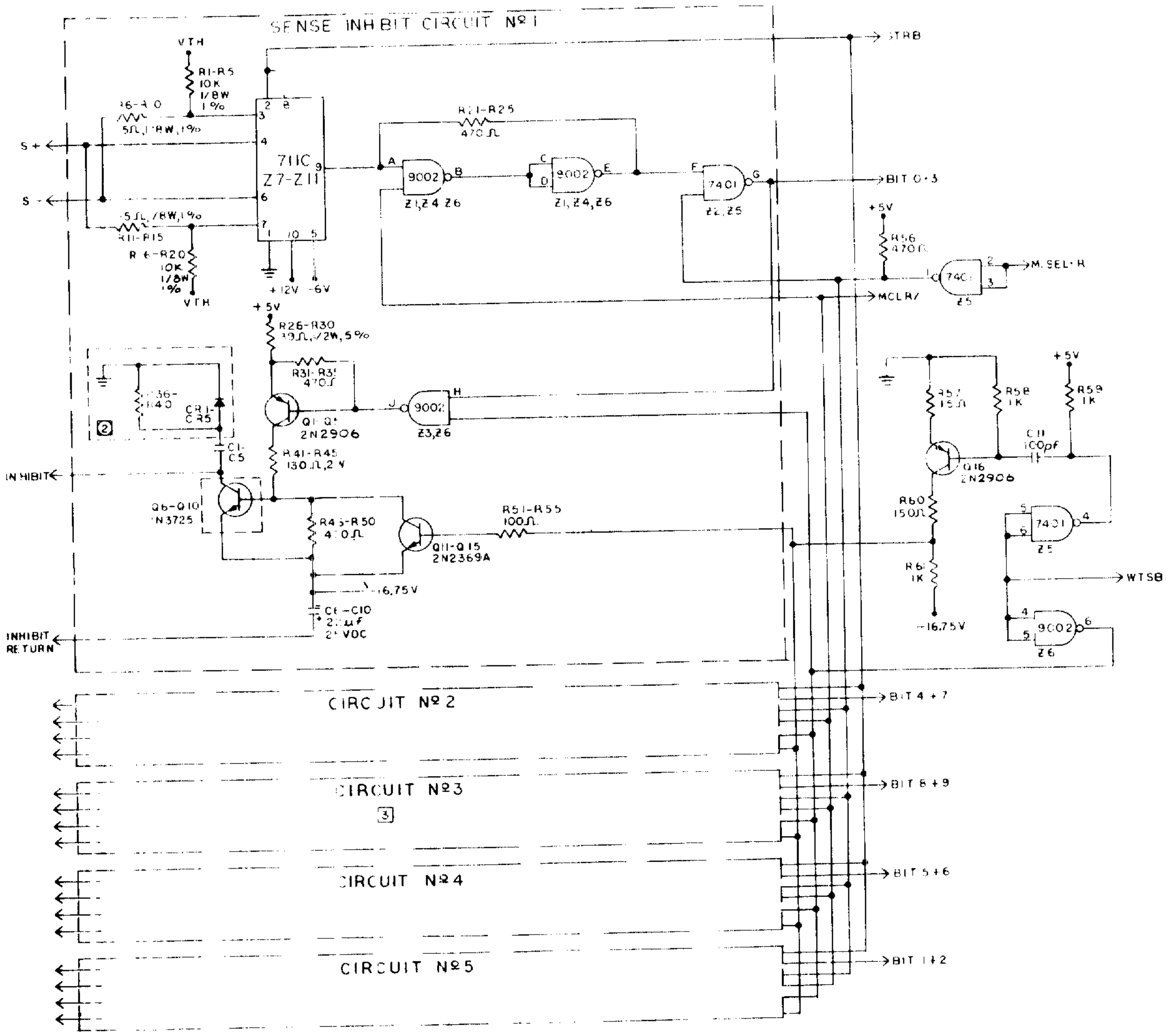
X50-X57. The read and write drivers are connected to the X-Drive lines through diodes. Each current sink is connected to an X-Drive line. The Y drivers and sinks are set up similarly with bits 6, 7 and 8 decoding the driver line and 9, 10 and 11 decoding the sink line. Thus one X and one Y drive and sink line are active at any one time. At the coincidence of the X and Y Drive lines, each carrying half current, is one core in each bit plane. The direction of current flow depends on whether read drivers or write drivers have been selected. Thus, one core of 4096 in each plane has received full switching current in one direction (neglecting the sense and inhibit line).

The decoding and line driver selection logic for the X and Y read/write drivers is given in Tables 9 and 10.

3.7.3 Sense Inhibit Circuits

The sense inhibit circuits shown in Figure 76 function differently in a write operation than they do in a read operation. In the read cycle RTSB/ goes to ground and gates the output at MD--/. With WTSB/, high, the INHIBIT line is not active and the sense of the core is read out under STRB control. Gates 9002 shown with the 470 ohm feedback resistor act as a latch to hold the contents of the core since the strobe pulse is approximately 50 nanoseconds wide. Gate 7401 inverts the core state and presents MD--/. When WTSB/ goes negative enabling the write cycle a 1 at MD--/ will result in a 0 being written into the core. This action occurs as follows:

If a 0 was read out of the core, the state of MD--/ would be a 1, turning output J of gate 9002 low. In addition Q6 (2N 3725) delivers current into the core array which is equal and opposite to the write current, when a zero is being written. If the output of gate 7401 were a 0, then INHIBIT current would not be delivered. Waveshapes and timing for the operation described above are given in Figure 77.



BIT	A	B	C	D	E	F	G	H	J
0+3	Z1-12	Z1-11	Z1-9	Z1-10	Z1-8	Z2-12	Z2-13	Z3-10	Z3-8
7+4	Z1-2	Z1-3	Z1-4	Z1-5	Z1-6	Z2-2	Z2-1	Z3-4	Z3-6
8+9	Z4-12	Z4-11	Z4-9	Z4-10	Z4-8	Z2-8	Z2-10	Z3-12	Z3-11
5+6	Z4-2	Z4-3	Z4-4	Z4-5	Z4-6	Z2-6	Z2-4	Z3-2	Z3-3
1+2	Z6-12	Z6-11	Z6-9	Z6-10	Z6-8	Z5-8	Z5-0	Z6-2	Z6-3

PAD Nº	TERM
1	S + 100
2	S - 100
3	INH. 100
4	INH.R.100
5	S + 200
6	S - 200
7	INH. 200
8	INH.R.200
9	BIT 0&3
0	BIT 4&7
1	WTSB/
2	+5V
3	VTH
14	OV
5	-6V
6	-16.75V
7	STRB
8	+12V
9	S + 300
20	S - 300

PAD Nº	TERM
21	INH. 300
22	INH.R.300
23	BIT 8&9
24	-16.75V
25	OV
26	+5V
27	MCLR/
28	M.SEL-R
29	BIT 6&5
30	S+400
31	S - 400
32	INH. 400
33	INH.R.400
34	BIT 1&2
35	S + 500
36	S - 500
37	INH. 500
38	INH.R.500

MCLR/	M.SEL-R	WTSB
Z1-13	Z2-11	Z3-9
Z1-1	Z2-13	Z3-5
Z4-13	Z2-9	Z3-13
Z4-1	Z2-5	Z3-1
Z6-13	Z5-9	Z6-1
	Z5-1	Z6-6
	R56	

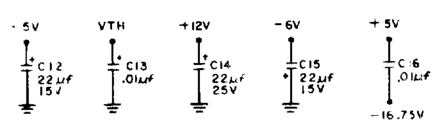


FIGURE 76

SENSE INHIBIT CIRCUIT

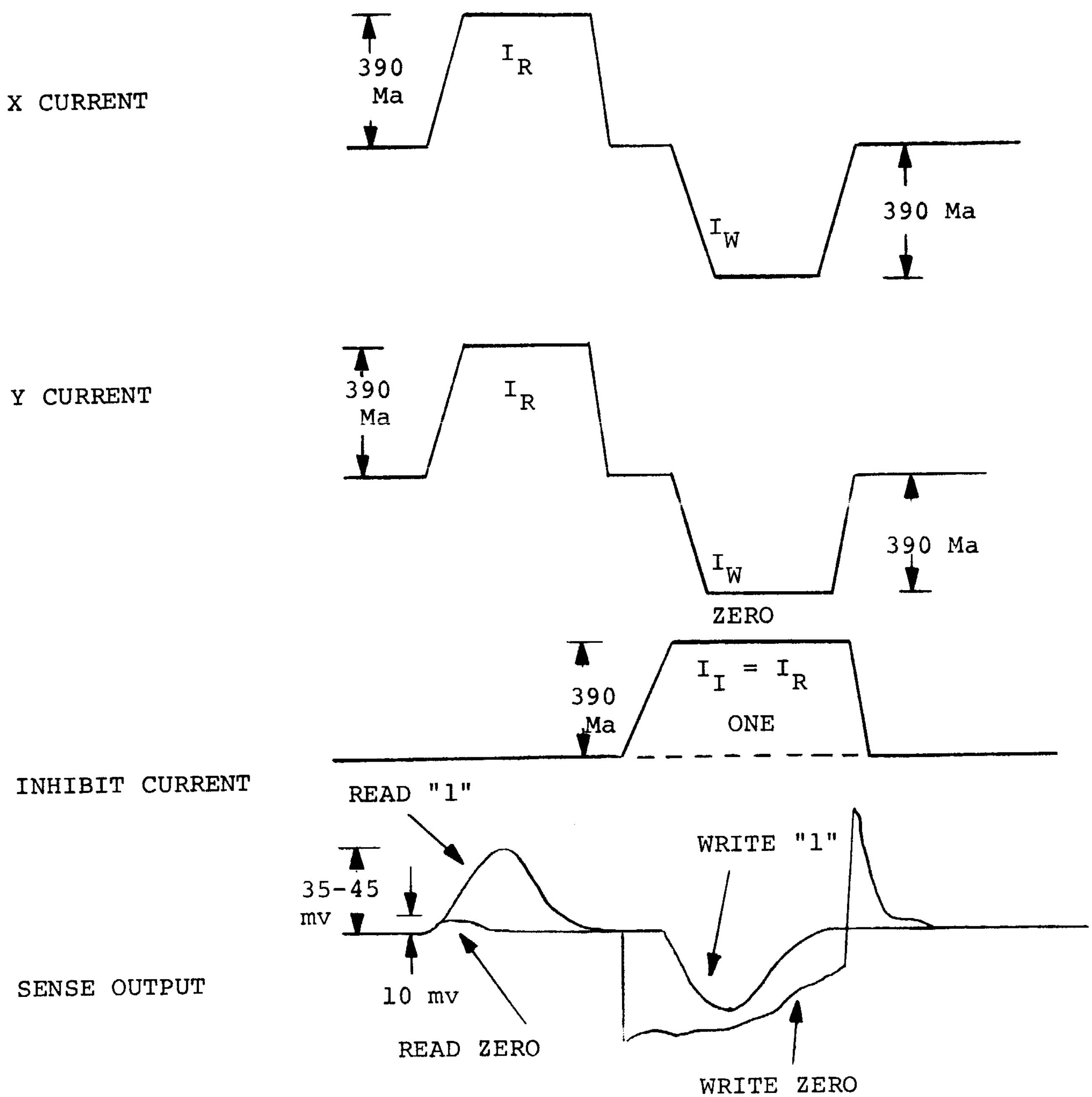


FIGURE 77

MEMORY TIMING DIAGRAMS (READ OR WRITE)

3.8 PROCESSOR OPTION BOARD

3.8.1 General

The Processor Option Board provides up to four separate computer options. Power fail protection and real time clock functions are combined on the same printed circuit board. An additional function permits processor control of the external interrupt lines.

Features of the processor option board include:

a. Power Failure Detection and Automatic Restart

b. Memory Parity Generation and Check

c. Real Time Clock

d. External Interrupt Enable/Disable

3.8.2 Functional Description

The Processor Option Board is available in three different configurations. Each type includes the external interrupt control function and one or more of the other optional functions. Figure 6 in Section I herein shows the Processor Option Board location in the machine is at J13.

3.8.3 Power Failure Detection

The power failure detection option shown in Figure 78 monitors the AC power line for significant voltage transients. This circuit is located in the power supply assembly and generates an interrupt to the computer during a power failure or interruption.

The normal DC supply voltages of the power supply will remain in regulation for at least two milliseconds after the detector signals the impending line loss. A computer software program is required to store all necessary information prior to an orderly shutdown. When the processor halts, the option board detects the new condition and generates a master reset which is held as the DC voltages relax.

The application of the master reset signal is entirely dependent upon the processor coming to a halt. If the service routine requires more than one millisecond, the shutdown may occur improperly.

As power returns, the master reset is held for approximately 150 milliseconds to allow the DC voltages to assume power regulation. When the reset is disabled, the interrupt is generated and the processor is set to the RUN mode. A computer software program is required to restore all information saved prior to the shutdown operation.

Firmware in the computer recognizes the power fail and automatic restart interrupt signals and enables the service routines via addresses stored in dedicated core memory locations. These pointers are as follows:

POWER FAILURE	008E	15-BIT ADDRESS OF POWER
	008F	FAILURE SERVICE ROUTINE
AUTOMATIC RESTART	0090	15-BIT ADDRESS OF AUTO-MATIC
	0091	RESTART SERVICE ROUTINE

The power fail and auto restart flip flop (Z6) is asynchronously controlled by an OR gate reset signal comprised of MRST/ or K2XX and AENI. K2XX is a clock signal generated by the NAND combination of CPH1 and CPH2/ and is identical to CLK6/ generated on the control board. When PWRD/ falls to a low level then the Z8 AND-OR-INVERT gate sets up the trigger for the power fail flip flop and sets PWRF. The PWRF flip flop is reset at the next K2XX/ gated under AENI which provides for an automatic restart by generating RUNP/ or upon the next master restart MRST/.

Real Time Clock

The real time clock option schematically shown in Figure 79 contains a 12-bit counter which is enabled by software commands and referenced to the processor master clock. When the counter is preset to the desired value and enabled, the processor is interrupted each time a carry bit is generated. The rate at which interrupts occur

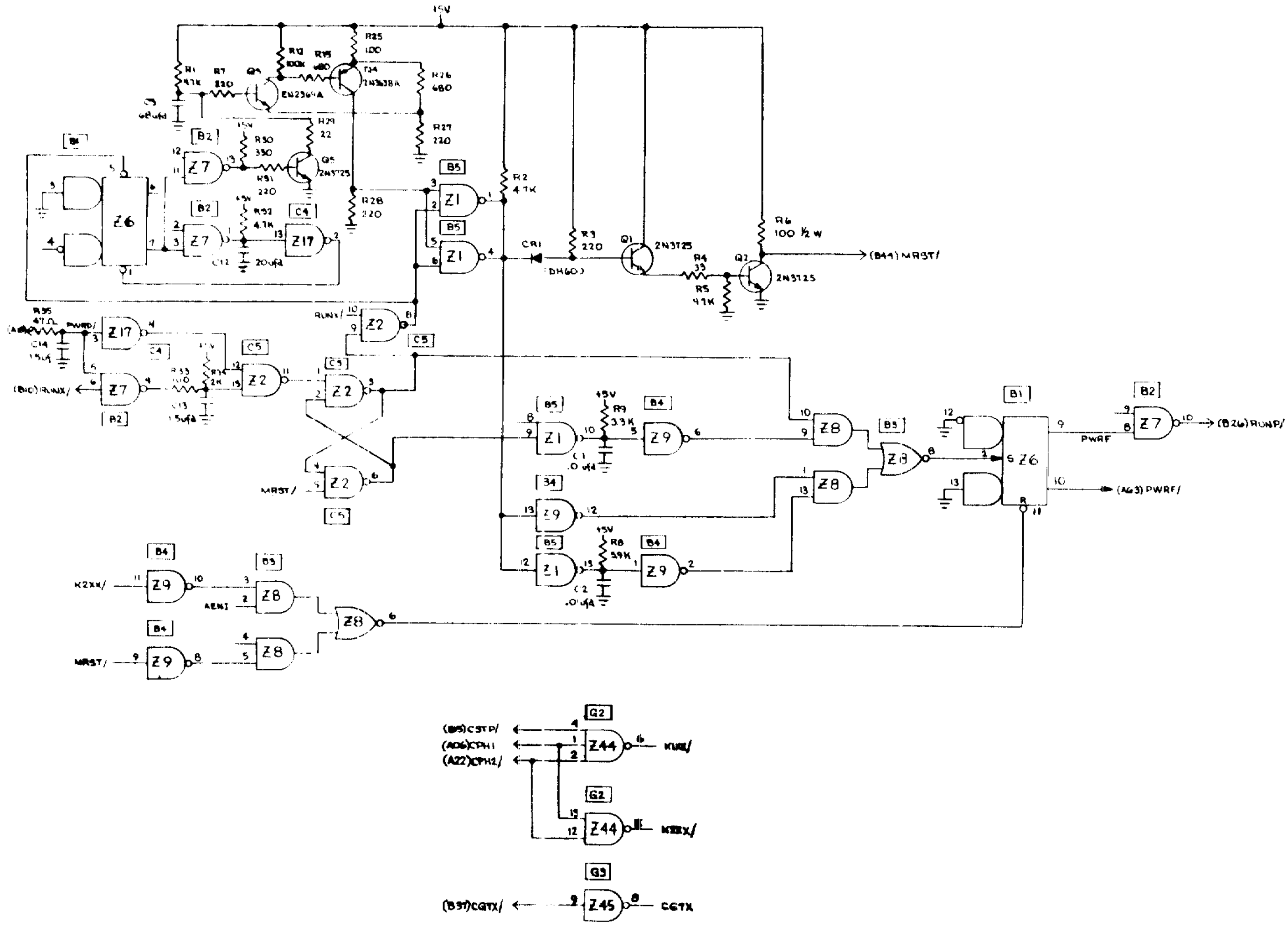


FIGURE 78

POWER FAIL AND AUTOMATIC RESTART LOGIC DIAGRAM

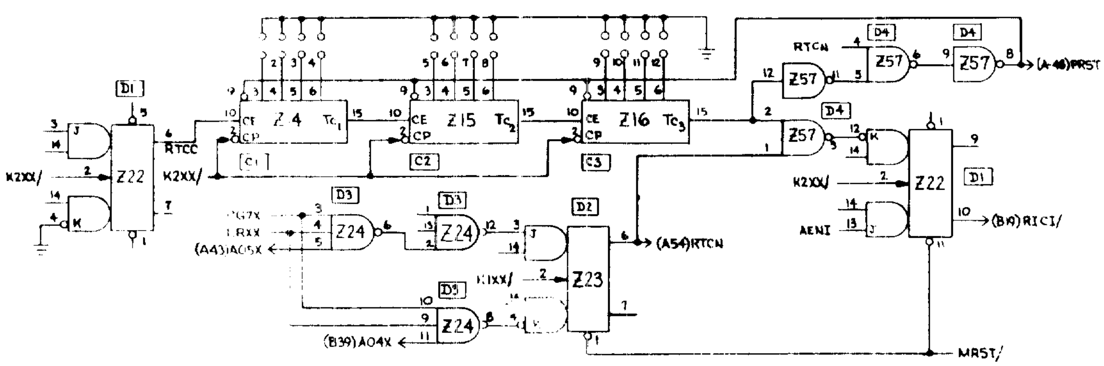


FIGURE 79

REAL TIME CLOCK LOGIC DIAGRAM

is adjustable by the selected preset value. The clock may be disabled by software command. The processor employs interrupt rates from one millisecond to 65.5 seconds based upon the software control. This range of interrupt rates may be altered by selection of wire jumpers on the circuit board.

Operation of this option consists of two distinct functions. When the 12-bit counter generates a carry (after counting from the preset condition), the content of a core memory location is incremented by one. This operation is implemented via firmware. When the incrementing causes the memory location to produce a carry bit, the processor is interrupted and the software program is switched to a service routine.

Dedicated memory locations in the computer are as follows:

0084	Counter	(Increments each Real Time Clock carry interrupt.)
0085		
0086	16-bit address to subroutine for handling memory counter (0084, 0085) carries.	
0087		

The preset values, selected by wire jumpers, are determined by the following simplified procedure. Since the 4.55 megahertz processor master clock signal (K2XX/) is connected to a flip flop on the processor option circuit board, the resultant timing signal (RTCC) which drives the 12-bit counter is 2.275 megahertz. This value is divided by the desired interrupt rate to yield the preset value N. The value N is converted to binary form with extended high order zero bits to give a total of 12 bits. The ONE's complement is obtained and incremented by one to yield the TWO's complement. The order of the binary bits is reversed to place the least significant bit on the left and the most significant bit on the right. Wire straps are installed in solder points 1 through 12 corresponding to the zero bits in the final value.

Example: Determine wire straps for 3 KHz interrupt rate.

1. RTCC = 2.275×10^6

2. $2.275 \times 10^6 / 3 \times 10^3 = 758_{10}$

This value corresponds to the number of counts required to obtain an interrupt.

4. 1001 000 1011 + 1 = 0101 0000 1011

5. Install wire straps: (Points 1, 3, 5, 6, 7, 8, 10.)

1	2	3	4	5	6	7	8	9	10	11	12
0	1	0	1	0	0	0	0	1	0	1	1

Software programming for the real time clock includes the machine instructions for enabling and disabling the function:

06_{16}	DRT	Disable Real Time Clock
07	ERT	Enable Real Time Clock

The dedicated core memory locations for the count value and execution address is as follows:

0084-0085 [ ] 16-bit Counter

0086-0087 [ ] 15-bit Address of Service Routine

Memory Parity Generator

The optional memory parity circuits shown in Figure 80 generate parity information for storage in core memory and check operations during memory access. This option is used with core memory modules employing Bit 09 as the parity indicator.

Even parity is used. For example, if the number of ONE's in the data byte is odd, the parity bit is set to a ONE to make the total number even. The parity bit is generated whenever data is first stored in a memory cell. Every time the cell is read thereafter, the parity bit is checked against the data content. If an error is detected, an interrupt is generated. Since data is rewritten from the memory internal register, during a Read/Restore full cycle, an error, once detected will remain in the same error condition for subsequent reads. The rewrite during restore does not regenerate parity. A parity failure detection causes generation of an internal interrupt with source indication in internal status byte, bit 04.

Firmware is provided in the computer to recognize this interrupt. A computer sub-routine is required to process the interrupt. Dedicated memory locations in the computer for parity fail interrupt subroutine pointers are as follows:

008A	15-bit address to subroutine
008B	for handling parity error

The true states of the memory data bus MD00 through MD07 are processed by a pyramid of AND-NOR gates and generates a high or low voltage at Z12 pin 8 which is a function of the number of 1's or 0's contained in MD00-MD07. When an even number of 1's is contained in MD00-MD07 Z12 Pin 8 output will be high and when an odd number of 1's are contained in MD00-MD07 the output at Z12 Pin 8 will be low. This output is logically combined with TDBC, T-register to Data Bus Control and READ/ to form a control gate which will set the state of the memory parity flip flop Z10. Z10 is clocked by K2XX/.

External Interrupt Enable/Disable

Interrupt control is mechanized with a control flip flop which is set and reset by microcommand. Installation of the option breaks the interrupt line and adds an overriding control to the interrupt line before passing it on to the CPU.

An external interrupt is indicated directly in File D. bit 07.

Special Micro Commands are:

1708 Literal to Register - Enable External-Interrupt

1704 Literal to Register - Disable-External-Interrupt

Dedicated macro instructions in Micro 810 are:

05 EIN Enable Interrupt System	These instructions translate directly into microcommands listed above.
04 DIN Disable Interrupt System	

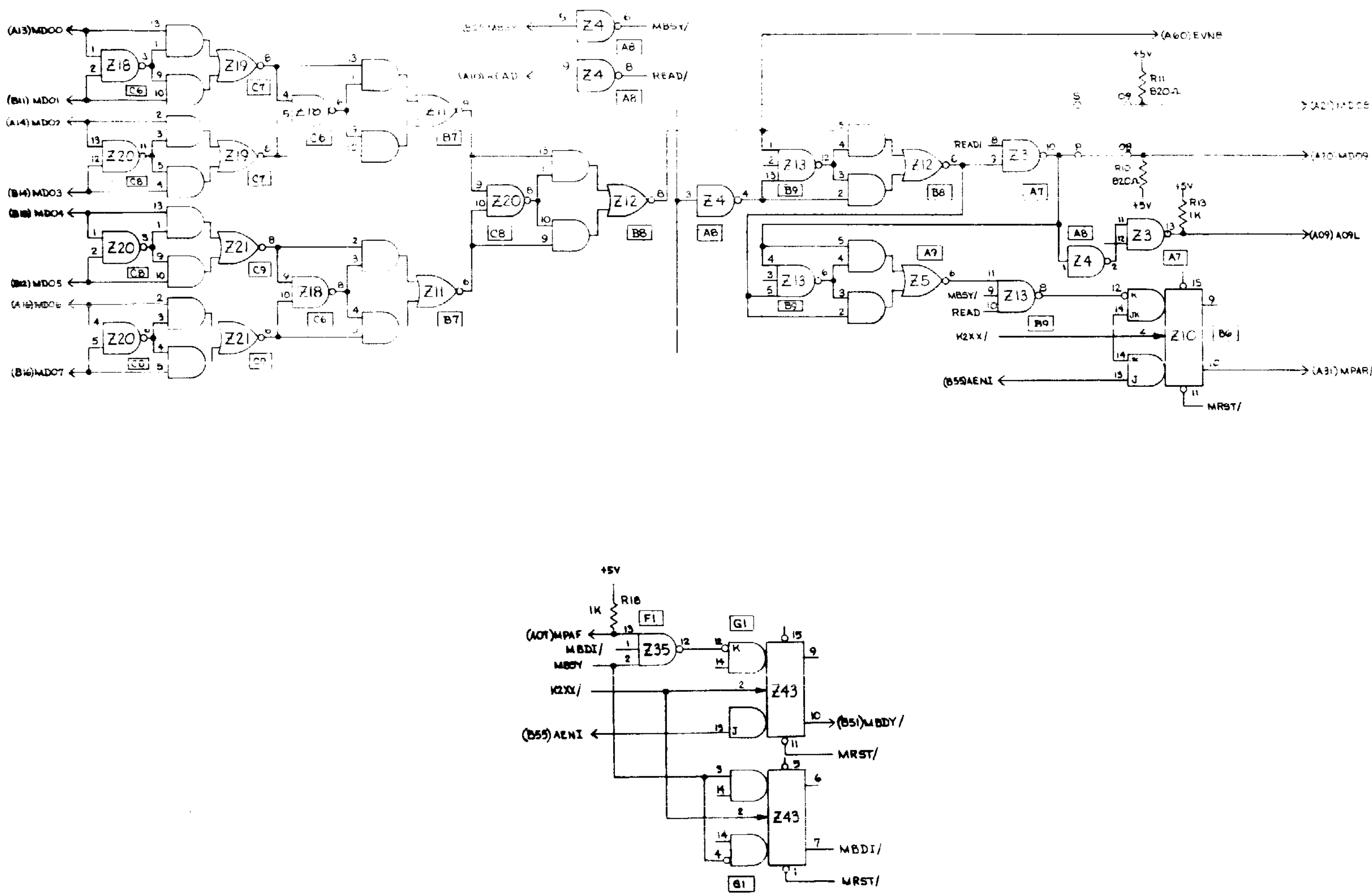


FIGURE 80

MEMORY PARITY LOGIC DIAGRAM

3.9 DIRECT MEMORY ACCESS

COXX and DOXX shown in Figure 81 are control outputs from the DMA channel to the I/O device. COXX/ indicates that control byte is available on DMA output lines MD00/ through MD07/. DOXX/ indicates that data byte is available on DMA output data lines MD00/ through MD07/. COXX/ and DOXX/ are derived from the states of the I/O control flip flops.

101A/ = 101X/

102A/ = 102X/

103A/ = 103X/

COXX/ = 101X·102A/·103A/

DOXX/ = 101A/·102X·103A/

CRDY/ is a signal from the DMA channel indicating that the channel is ready for block transfer.

EWRT/ is an input from the external device indicating whether a read or write operation is to take place.

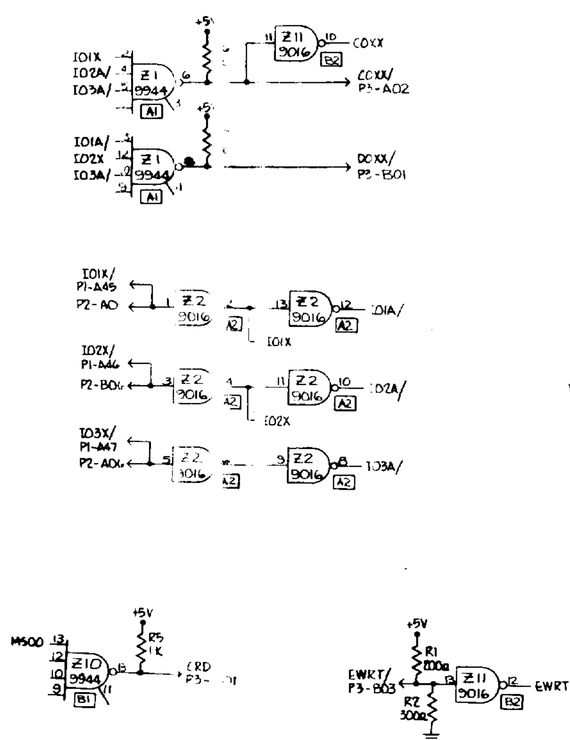


FIGURE 81

DMA CONTROL SIGNALS

The CLK1/ and CLK5/ clocks, Figure 82 used on the DMA channel are derived from the processor oscillator.

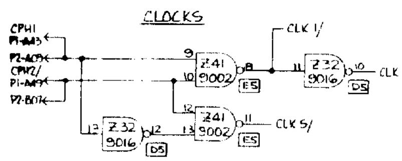


FIGURE 82

DMA CLOCKS

Figure 83 shows the timing diagram for the DMA clocks.

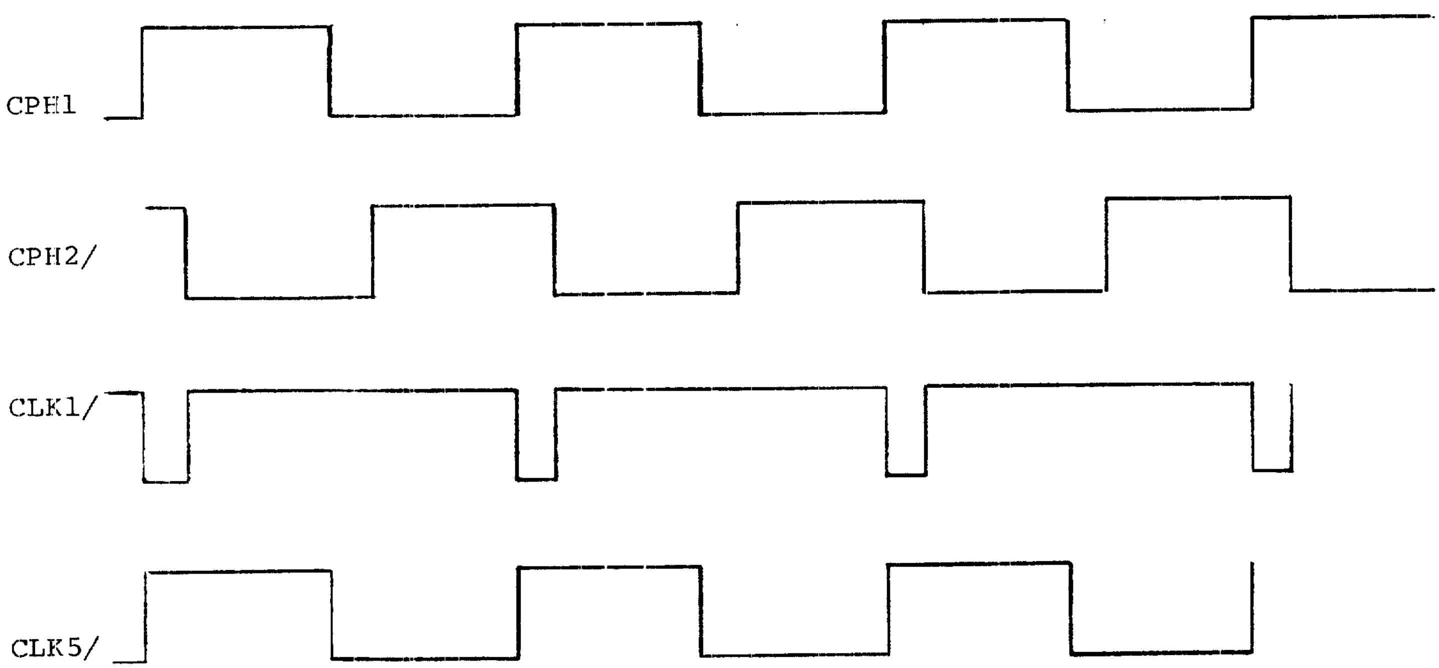


FIGURE 83

TIMING DIAGRAM DMA CLOCKS

CREQ/ shown in Figure 84 is an input signal from the addressed external device used to initiate each byte transfer. It may be pulsed for 250 nanoseconds to 1 microsecond or it may be reset on the leading edge of DRDY/ which is the Data Ready or Data Receive pulse from the DMA Channel. Maximum time from CREQ/ to DRDY; is 1.1 microsecond. If CREQ/ is tied to 0 volts, whenever the DMA channel is started by the processor, output bytes will be transferred at a memory cycle rate of 1.1 microsecond each.

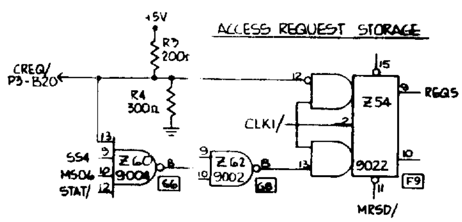


FIGURE 84

ACCESS REQUEST STORAGE

DRDY/ shown in Figure 85 is a control signal from the DMA channel to the I/O device indicating byte data is present on output lines MD00/ through MD07/ during an output operation or that the channel has captured the data byte on input lines DD00/ through DD07/ during an input operation.

DMAW/, (Figure 85) is a control signal from the DMA Channel to the processor indicating to the memory control whether a DMA write cycle is to be initiated.

DMAR/, DMA request, is generated by the following:

$$DMAR/ = S1 \cdot MBSY/$$

and enables the gates on the control board which set up the DMA half cycle and write cycle sequences.

DMAS/, DMA select, is generated by

$$DMAS = DMAR/ \cdot SS0$$

and is used as a control term on the control board.

CSTB/, start of buffer, is a control signal from the DMA channel to the I/O device indicating the start of each buffer transfer by the DMA channel.

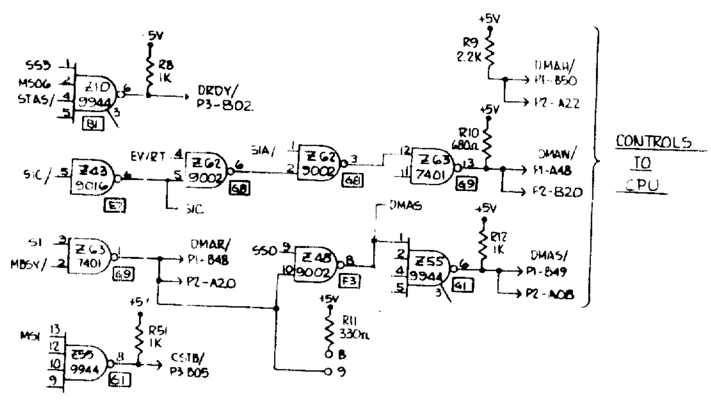


FIGURE 85

DMA CONTROLS TO COMPUTER

Major Activity Sequence

The mafor activity sequence shown in Figure 86 is basically comprised of control term activation of a 4-bit shift register. Parallel input operation is provided when Pin 9 of Z50 goes low. MRSD/ is a reset signal which sets the outputs of the shift register (MS1, MS2, MS3, MS4) to low states and initializes the major activity sequencer. When the parallel entry input (**Pin 9**) is high, the shift register performs a 1-bit shift for each clock pulse input. The shift occurs after the low-to-high transition of the clock input. When the parallel input is low the next condition of the shift register synchronous with the clock input is determined.

Control terms effecting the major activity sequencer are:

MS00/ = MS1/·MS4/

MS06/ = MS1/·MS4

MSK2/ = MS06·SS4·CEEQ·SS0

IABC/ = MS1·SS4·SS0

IBCW/ = MSK2·CA15

DA16 = MD02·MD02·MD03·MD04·MD00

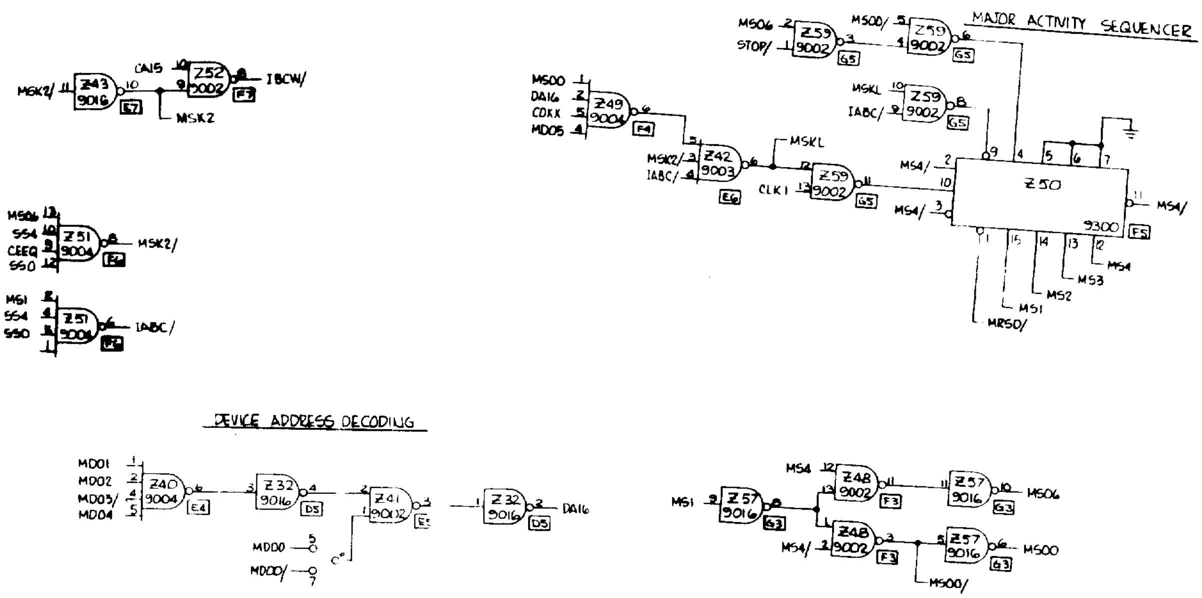


FIGURE 86

MAJOR ACTIVITY SEQUENCER

Memory Cycle Sequencer

The memory cycle sequencer shown in Figure 87 is comprised of a 4-bit shift register controlled by the S1 and SS04 control terms and CLK1/. The control terms are functions of the output states of the memory cycle and major activity sequences, along with other control terms such as MBSY, PRIN, COXX/, DOXX/, INST, etc. The memory cycle sequencer does not employ a parallel entry feature. The output states of SS1, SS2, SS3 and SS4 are low after the master reset MRST/.

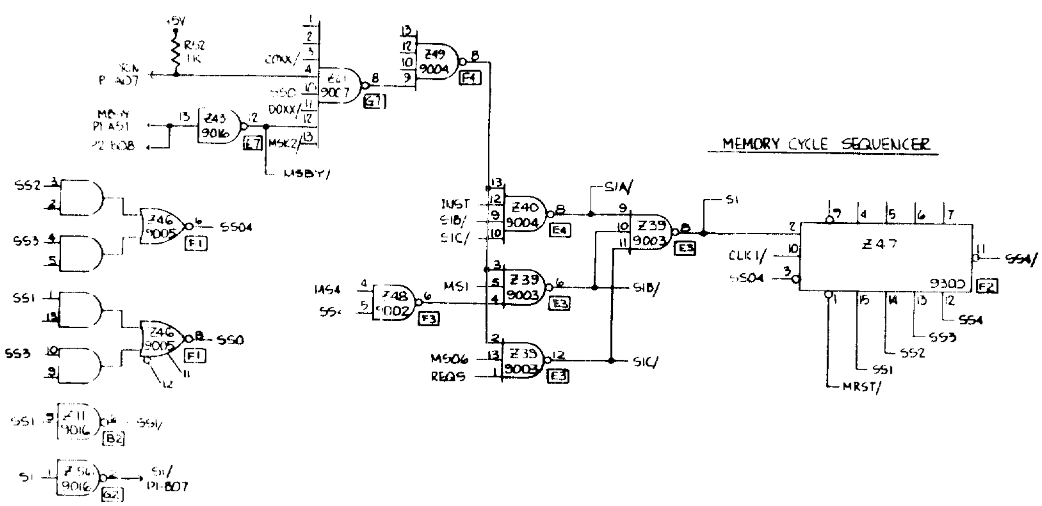


FIGURE 87

MEMORY CYCLE SEQUENCER

Address Generator for Block Control Words & Status Byte

The Address generator for block control words and status byte shown in Figure 88 is comprised of a series of gates whose inputs are controlled by the outputs of the Address Byte Counter, Block Control Word Counter and control terms.

STAT = STAS/·S1A/

CADD/ = DMAS·MS1

CDST = CADD/·STAT/

The Block Control Word Counter is clocked by IBCW/ and generates BCW1/ and BCW2/.

The Address Byte Counter is clocked by CLK5/ and reset by MRSD/. The Address Byte Counter is inhibited when IABC/ is high.

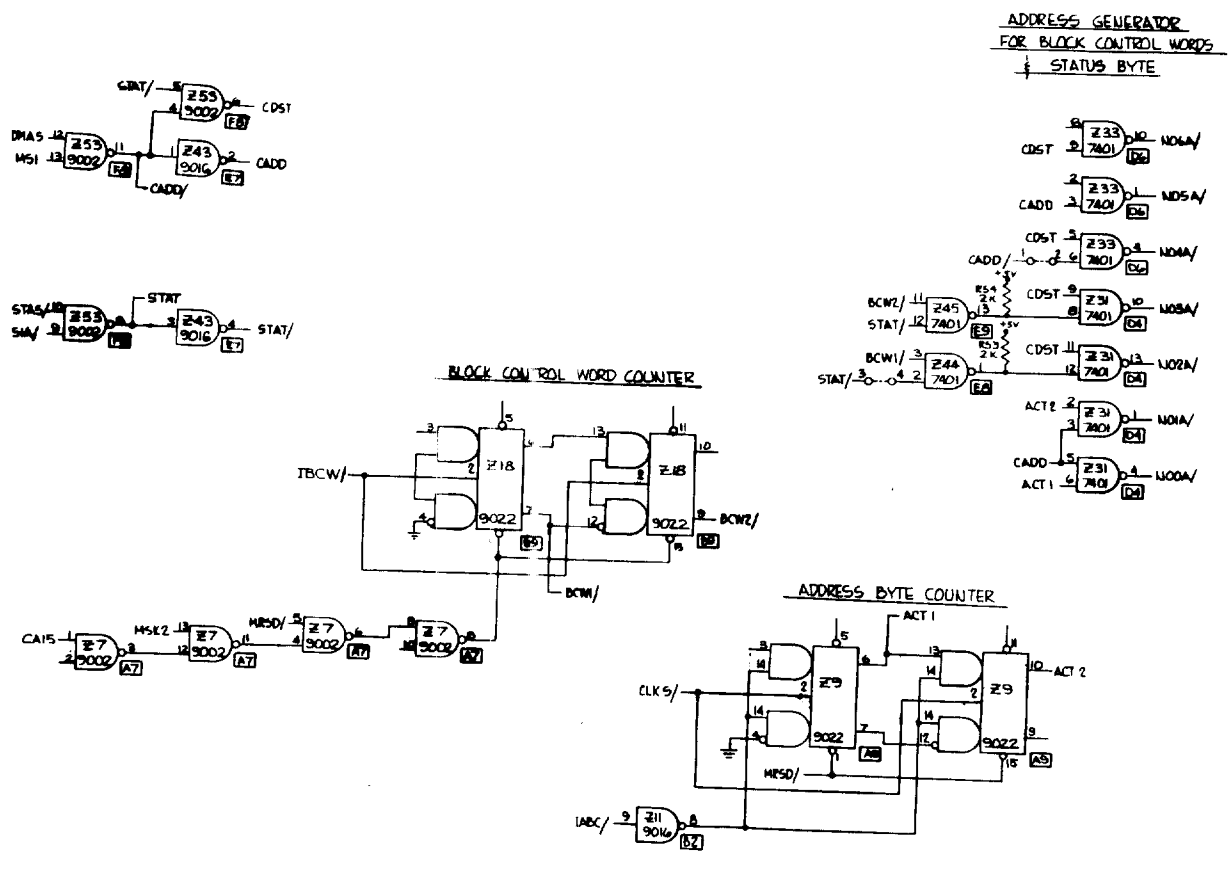


FIGURE 88

ADDRESS GENERATOR FOR BLOCK CONTROL WORDS AND STATUS BYTE

The status input cycle in progress indication shown in Figure 89 is generated by STAS which is controlled by S1A/ going low and flip flop Z8 clocked by CLK1/. The status input cycle is ended with SS4/ becoming low and the flip flop being reset on the next CLK1/.

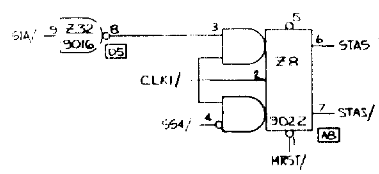


FIGURE 89

STATUS INPUT CYCLE IN PROGRESS

The instruction storage flip flop shown in Figure 90 is clocked by (DA16·COXX). The STOP/ control term, used as a parallel entry in the major activity sequencer, is set by MD06 and the (DA16·COXX) clock and reset by MD07/ and the clock.

The clock term generated by DA16·COXX is gated with MD07 to form MRSD/ which is used to asynchronously reset the logic elements in the DMA channel. MRSD/ is also formed upon application of MSRT/, the master reset which is a low signal used to clear all control flip flops to initialized conditions.

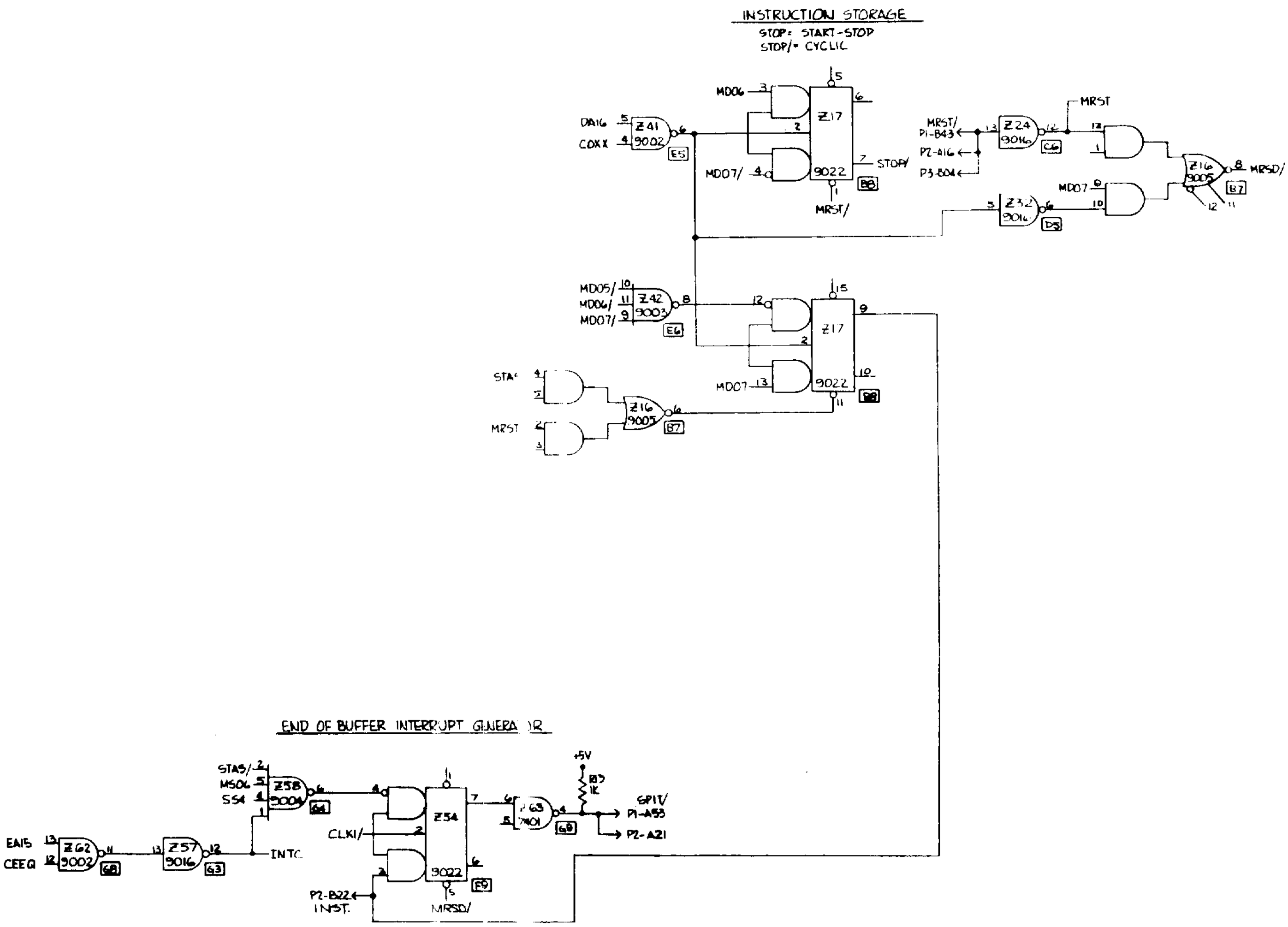


FIGURE 90

INSTRUCTION STORAGE

The Status Byte to Memory Data Bus shown in Figure 91 comprised of a series of gates with inputs derived from the I/O device status bits 1 through 6. Six device dependent status bits are transferred from the I/O device to dedicated memory locations.

These bits reflect the status of the I/O device all during the time it is connected for service and executing a block transfer operation. The memory data bus is enabled by STAT.

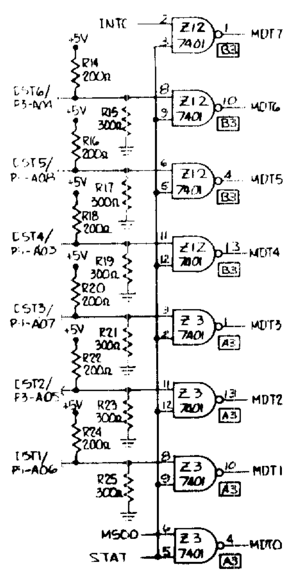
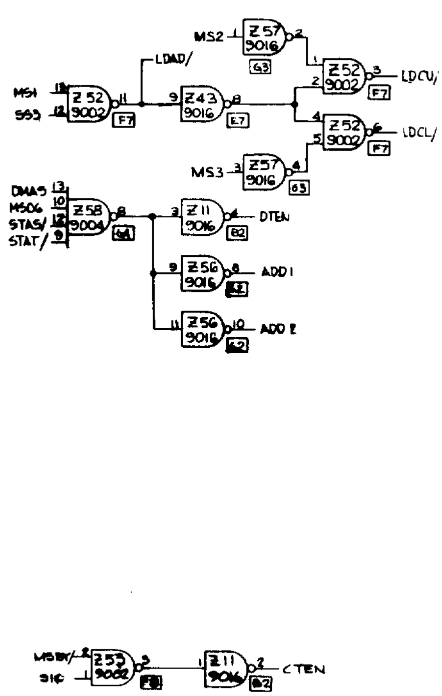


FIGURE 91

STATUS BYTE TO MEMORY DATA BUS

The current address register and counter circuitry shown in Figure 92 is comprised of four 4-bit binary counters which are parallel entry controlled to utilize T-register outputs MD00 through MD07 to generate the current address CA00 through CA15. The registers are loaded under control of LDCU/ (load upper section of the current address) and LDCL/ (load lower section of current address). The 4-bit binary counters are clocked and enabled by CTEN.

The address drivers also shown in Figure 92 which generate the M and N registers, establishing the memory address, are comprised of a series of gates. Address 1 (ADD1) enables the M-register gates whose inputs are CA08 through CA14. Address 2 (ADD2) enables the N-register whose inputs are CA00 through CA06.



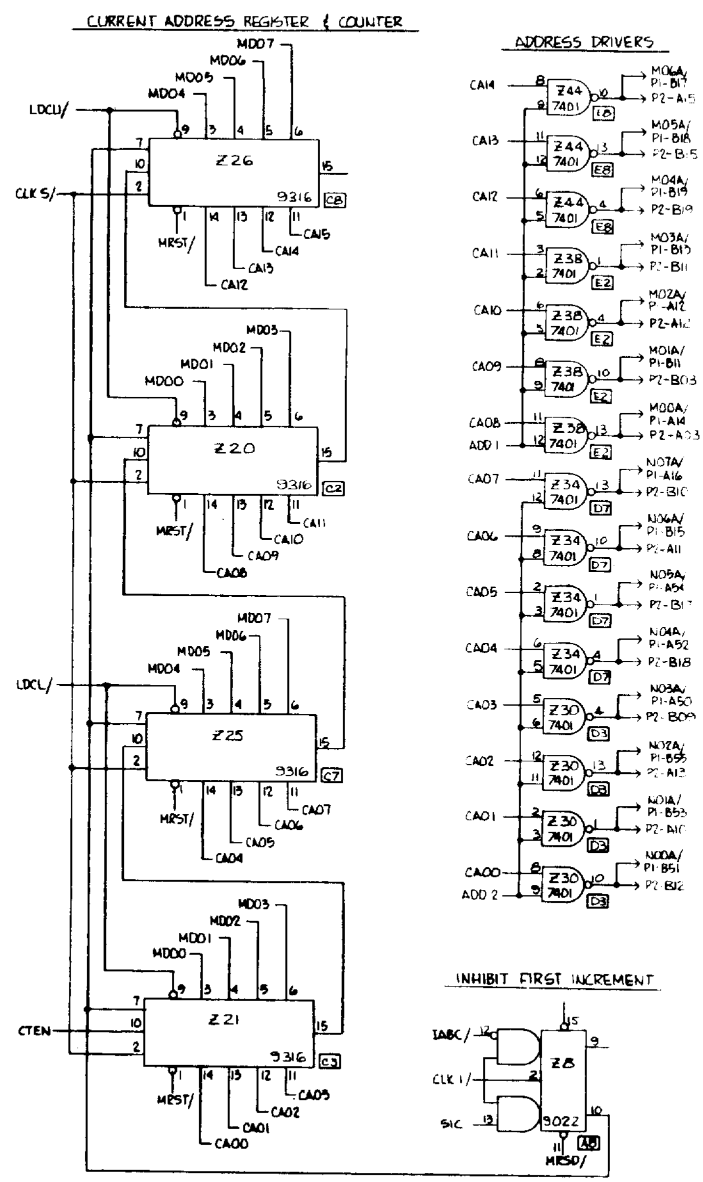


FIGURE 92

CURRENT ADDRESS REGISTER COUNTER AND ADDRESS DRIVERS

The End Address Register shown in Figure 93 is comprised of four 4-bit latches which are loaded under control of LOAD/ and MS4 (or MS4/). The T-register outputs MD00 through MD07 are used to set the latches whose outputs are named EA00 through EA15.

A comparator network also shown in Figure 93, compares the contents of the current address register with the contents of the end address register. If the comparison of EA-- and its counterpart CA-- results in the signal CEEQ going low (OV) then the end of buffer interrupt generator is activated and the control term INTC goes low, effecting the status byte being transferred to memory data bus. Again when CEEQ goes low the clock for the block control word counter is diabled.

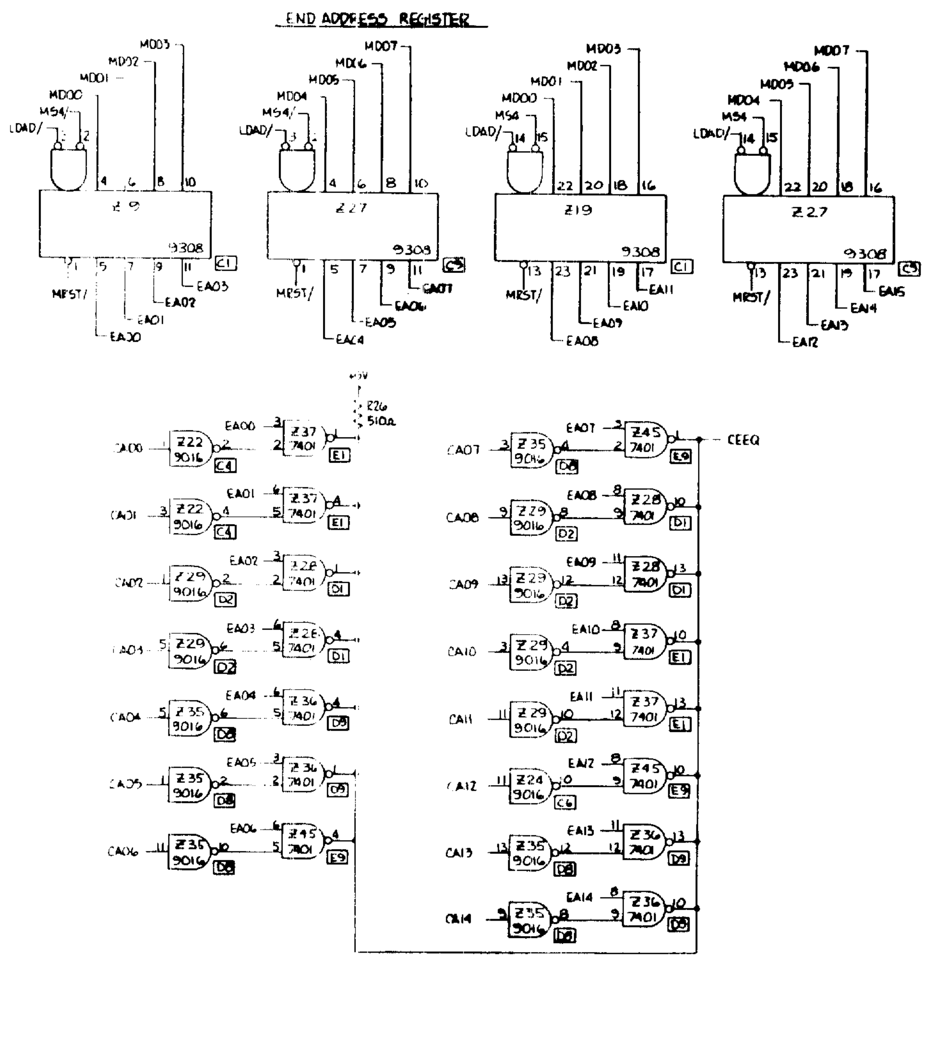


FIGURE 93

END ADDRESS REGISTER AND COMPARATOR

The data input buffer shown in Figure 94 is comprised of two 4-bit latches which are loaded under control of SS1/ and CLK1/. The input data is derived from the data input bits 0 through 7. The data byte stored in the latches is transferred to the memory data bus via a series of gates which are controlled by DTEN. The contents of the memory data bus (MD00 through MD07) is derived from the output data drivers which are a series of gates whose input is the data byte.

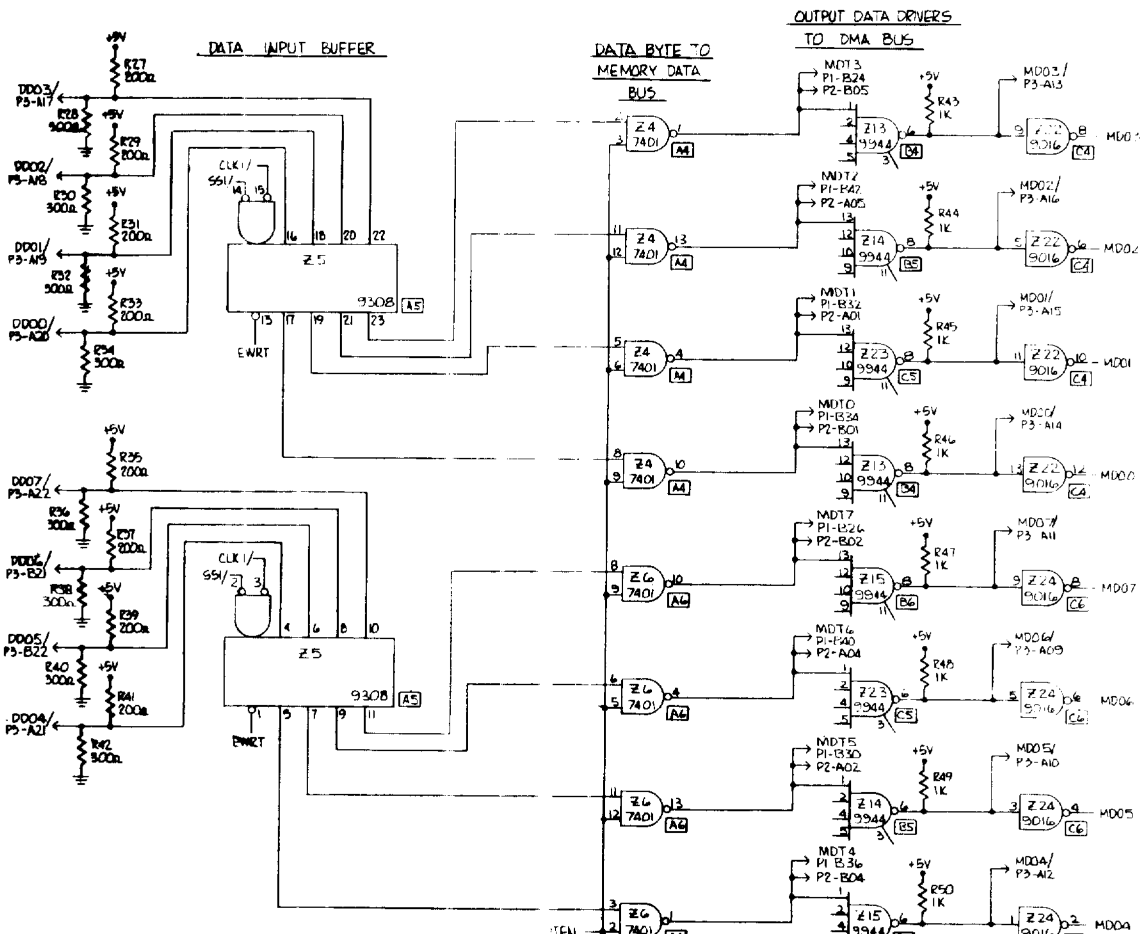


FIGURE 94

DATA INPUT BUFFER AND OUTPUT DATA DRIVERS TO DMA BUS

3.10 SYNCHRONOUS MODEM INTERFACE

3.10.1 General

The Synchronous Modem Interface enables the computer to transmit data over communication lines via a synchronous data set. Data rates up to 9600 baud are available for point to point, multipoint, or switched network communications with optional automatic calling and/or automatic answering features. The interfaced data sets may use two or four wire service. All control functions and interface levels between the Modem Interface and the data sets are per EIA Standard RS-232-B. The Synchronous Modem Interface employs the following features:

- Programmed data transfers (in and out)
- Concurrent data transfers (in and out, but not simultaneous
- Full duplex service
- Internal or external I/O bus control
- Search mode with auto sync detection
- Control by software, firmware, or both

The Synchronous Modem Interface is also available with optional features of automatic calling and answering, and a status request interrupt. The latter feature when enabled generates an interrupt on completion of a concurrent operation or when a ringing condition exists.

3.10.2 Functional Description

A functional block diagram of the Synchronous Modem Interface is shown in Figure 94. The processor is connected to the interface via the input and output data busses. Commands and data are decoded by logic circuits which enable the control circuits on the interface. The following is a brief description of each of the functional circuits on this device.

3.10.2.1 Input/Output Busses

Functional control, addressing, and data signals are transmitted via the eight-bit output bus from the processor. Routing of this information is directed by the control commands and the channel control logic for each peripheral device. Data and status information is routed to the processor via the eight-bit output bus from the interface.

3.10.2.2 Address Decoder

The address decoder circuits monitor the low order five bits of the output bus for the device address. Normally, the synchronous modem interface is designated address hexadecimal ten 10_{16}. Addressing is determined by the wire jumpers located on the circuit board and may be altered easily for a particular application. Detection of the jumpered device address in conjunction with a control command enables the respective response from the channel control and function store logic circuits.

The interface board is normally strapped for device address 10_{16} and sync codes 16_{16}. These values may be altered for a specific application by removing the unnecessary jumper wires and substituting connections according to Table 11. Points 2, 5, 8, 11, and 14 (silk-screened on the board) receive the address bits from the processor. To select a specific address the inverted or non-inverted bit is connected via jumper wires.

Points 48, 45, 42, 39, 36, 33, 30, and 27 determine the sync code used by the interface. Since the eight bits allow a total of 65,535 combinations, only the typical example is provided on Table 11. This jumper wire configuration produces the sync code of 16_{16}.

TABLE II

DEVICE ADDRESS JUMPER WIRES

	2		5		8		11		14	
	1	3	4	6	7	9	10	12	13	15
00		X		X		X		X		X
01		X		X		X		X	X	
02		X		X		X	X			X
03		X		X		X	X		X	
04		X		X	X			X		X
05		X		X	X			X	X	
06		X		X	X		X			X
07		X		X	X		X		X	
08		X	X			X		X		X
09		X	X			X		X	X	
0A		X	X			X	X			X
0B		X	X			X	X		X	
0C		X	X		X			X		X
0D		X	X		X			X	X	
0E		X	X		X		X			X
0F		X	X		X		X		X	
10	X			X		X		X		X
11	X			X		X		X	X	
12	X			X		X	X			X
13	X			X		X	X		X	
14	X			X	X			X		X
15	X			X	X			X	X	
16	X			X	X		X			X
17	X			X	X		X		X	
18	X		X			X		X		X
19	X		X			X		X	X	
1A	X		X			X	X			X
1B	X		X			X	X		X	
1C	X		X		X			X		X
1D	X		X		X			X	X	
1E	X		X		X		X			X
1F	X		X		X		X		X	

	48		45		42		39		36		33		30		27	
	47	49	44	46	41	43	38	40	35	37	32	34	29	31	26	28
16		X		X		X	X			X	X		X			X

3.10.2.3 Function Store

The high order three bits of the output bus are decoded and stored each time the device is addressed. The decoded functions are used to control subsequent input and output operations. A summary of the function codes is provided in Figure 95.

BIT 765	OUTPUT	INPUT	CONTROL
000	Data Out	Data In	
001	Function Out	Data Set Status	
010	Spare	ACU Status	
011	Spare	Spare	
100			Disconnect
101			Spare
110			Concurrent Input
111			Concurrent Output

FIGURE 95

FUNCTION CODE SUMMARY

The transfer of data into or out of the interface is dependent upon the type of command generated in the processor which may be via the firmware, software, or a combination of both. For example, to send data from the processor to the interface, the Output Byte From A instruction may be used to effect the transfer. This presumes of course that the desired data was previously loaded into the A register.

To receive data from the interface to the accumulator, the identical function code is used with the Input Byte to A instruction. In each of the above cases, the second byte consisted of the actual data which is transferred.

When bits 7, 6, and 5 of the function code are set to 001_2, the function output instruction enables or disables the control signals described in paragraph H below. If the input signal is used, the processor receives the data set status information. Similarly, the

ACU status information is obtained by using the function input signal with bits 7, 6, and 5 set to 010_2.

The concurrent input, concurrent output, and disconnect functions are obtained via the unique function codes. The second byte of information is not functional.

The format for the information required in the above operations consists of three bits of function codes (7, 6, 5) and five bits of device address 10_{16}. The second byte consists of eight bits which depend upon the source. For example, the Status Word contained in the second byte corresponding to the Data Set and ACU is as follows:

BIT	DATA SET STATUS	AUTOMATIC CALLING UNIT
0	Data In Request (DIR)	Not Used
1	Search Mode (SM)	Not Used
2	Concurrent Mode (CM)	Not Used
3	Data Out Request (DOR)	Present Next Digit (PND)
4	Carrier On (CO)	Abandon Call and Retry (ACR)
5	Ring Indicator On (RIO)	Data Line Occupied (DLO)
6	Clear to Send (CTS)	Data Set Selected (DSS)
7	Data Set Ready (DSR)	Power Indicator On (PIO)

3.10.2.4 Channel Control

The channel control logic detects I/O operations requested for this device and routes the data/function information to the appropriate register or selects the required data, status, or address word to be gated onto the input bus.

3.10.2.5 Data Switch and Bus Drivers

These circuits consist of logic switches for gating the data, status, or address word as selected by the channel control logic to the bus drivers. Data is gated into the input bus by open collector line drivers. These drivers are enabled by the channel control logic circuits.

3.10.2.6 Output Hold Register

This register stores data from the processor to be either transmitted via the output shift register or presented to the Automatic Calling Unit (ACU) as a digit for automatic dialing. The digit information is stored in binary coded decimal form and occupies only the least significant four bits of this register.

3.10.2.7 Output Shift Register

This register consists of a parallel to serial converter used to drive the transmitter circuits. Data to be transmitted is gated into this register in parallel from the output hold register. With the appropriate timing signals present, the data is shifted serially to the transmitter at the transmit clock rate. As the last bit is shifted out, a parallel transfer occurs to reload the last transmitted byte from the output hold register. In this manner, the program can repeatedly transmit the sync codes between data blocks with only one actual data transfer.

3.10.2.8 Control Storage

Storage for control lines to the ACU, Data Set, Interrupt, and Search Detect Logic is implemented in this section. Enabling and/or disabling of these lines is controlled by the second byte of the function out command from the computer. Following is the format of the second byte.

BIT	FUNCTION
7	Disarm Interrupt
6	Arm Interrupt
5	Spare
4	Spare
3	1 = enable call request
	0 = disable call request
2	1 = enable search mode
	0 = disable search mode
1	1 = enable data terminal ready
	0 = disable data terminal ready
0	1 = enable request to send
	0 = disable request to send

3.10.2.9 Input Shift Register

Serial to parallel converter. When "carrier on" occurs in the receiving data set, the "receive clock" is enabled and data is shifted in at the receive rate.

3.10.2.10 Sync Detector

To synchronize the receiver portion of the modem interface to the received data, a minimum number of sync codes must be transmitted prior to the block of data.

Initially the receiver is set into the search mode. In this mode, the eight bits of data in the input shift register are compared to a predetermined code set up by jumper wires on the modem interface board. (Refer to Table II.) Once found, the data is gated in parallel to the input hold register and a status flag is set signifying to the computer that a data input is requested. The program in the computer should input the data and then reset the search mode. The modem interface board will then parallel load from the input shift register to the input hold register every eight clock pulses. The "data in" status flag will be set for each parallel transfer. The program should test for the receipt of a minimum number of contiguous sync codes and then the first non-sync code shall be considered the first byte of the data block.

3.10.2.11 Input Hold Register

As each word is assembled in the input shift register, it is gated in parallel to the input hold register. As each word is loaded, the "data in" ready flag is set and will remain on until the processor inputs the data byte. (Note: Should the processor fail to input the data byte prior to the assembly of the next byte of data, the original piece of information will be lost.)

3.10.2.12 Timing Control

The timing control circuits synchronize data input and output requests and parallel transferring of data from output buffer to output shift and input shift to input buffer registers. In the current mode, the timing and control logic will enable the concurrent request to the processor, test for acknowledge, and place the device address on the input bus at the appropriate time. When the current address and the end address are equal, the firmware automatically issues a disconnect to the device to terminate the concurrent operation. However, the software may issue a disconnect command at any time to terminate the concurrent operation early, if so desired.

3.10.2.13 ETA Transmitters

Information sent to the data sets is transmitted in conformance to the EIA Standard RS-232-B. A positive signal into the transmitter results in a negative output while a ground into the transmitter results in a positive output.

3.10.2.14 EIA Receivers

Information is received from the data set in conformance with EIA Standard RS-232-B. A negative input to the receiver results in a positive output while a positive input results in a ground output.

3.10.3 Wire List Information

The following is a glossary of interface signals and a wire list for the connectors used on the circuit board.

Processor to Interface

ØD00/	0D00/	8 data lines from processor
CØXX/		Control out command line
DØXX/		Data out command line
DIXX/		Data in command line
ACK1		Acknowledge command line
PRIN/		Priority enable to interface unit
KØXX/		I/O clock
MRST/		Master reset

Interface to Processor

ID00/	ID07/	8 input data lines
EINT/		External interrupt request

Data Set

Frame GRD	Connected to frame of data set
Send Data	Data to be transmitted is sent serially over this line. Prior to transmission Request to Send, Clear To Send, and Data Set Ready must be on.
Received Data	Data is received serially over this line. Data is shifted into the Input Shift Register at a rate controlled by the receive serial clock.
Request to Send	Conditions data set to transmit. This line must be enabled during entire transmission of message and turned off no sooner than 1 ms after last bit transmitted.
Data Set Ready	Indicates the data set is operational and connected to a communication channel.
Data Terminal Ready	For point to point or multipoint data only service, this line is not required. For switched or called circuits, this line is enabled to permit the data set to be connected to the communication channel. When automatic calling is used, data terminal ready maintains the connection to the communications channel during transmission and is used to terminate the connection when the transmission is completed. When a station is being called, this line is used to connect the data set to the communication channel and, as before, terminates the connection when transmission is complete.

Data Carrier Detector	Indicates data carrier being received. An off condition represents end of transmission or fault.
Transmit Clock	Square wave generated by the data set to control shift rate of output shift register in the modem controller. This line is used with internal timing only.
Received Clock	Timing signal used to sample received data.
Ring Indicator	Used with automatic answering option. An on condition indicates a ringing signal from a remote station.
Signal Ground	Used to establish common reference for circuits in the modem controller and the data set.

COMPUTER INTERFACE CONNECTOR P1

A01	GND
A02	GND
A03	CØ1
A05	+12V
A06	CPH1
A07	DØ/
A08	-16V/-8V
A10	T05X/
A26	T02X/
A31	IØ2X/
A32	ID04/
A38	EINT/
A55	PROT/
A58	T07X/
A60	ID01/
A61	ID06/
A62	ID03/
A64	GND
A65	GND
B01	+5V
B02	+5V
B04	AK/
B05	DX/
B10	T01X/
B22	CPH2/
B26	T06X/
B31	IØ1X/
B32	ID00/
B37	T04X/
B39	T00X/
B42	ECIØ/
B44	MRST/
B54	PRIN/
B58	ID05/
B60	ID07/
B61	IØ3X/
B62	ID02/
B64	+5V
B65	+5V

Automatic Calling Unit P2

A01	CRQ/
A02	GND
A03	DPR/
A04	GND
A05	NB1
A06	GND
A07	NB2
A08	GND
A09	NB4
A10	GND
A11	NB8
A12	GND
A18	DLØ
A19	PWI
A20	ACR
A21	DSS
A22	PND
B18	GND
B19	GND
B20	GND
B21	GND
B22	GND

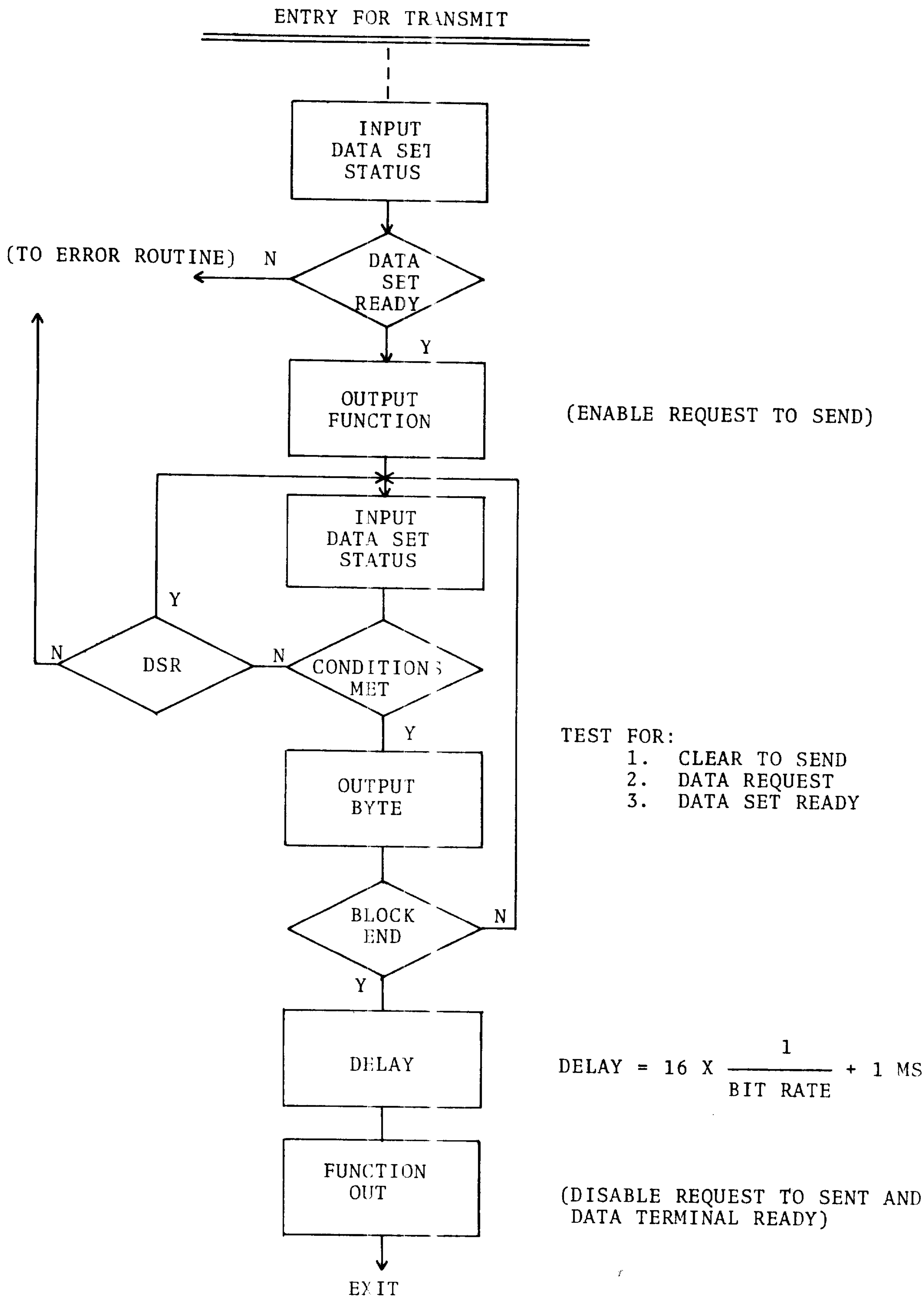
Data Set Interface Connector P3

A01	CTS
A02	DSR
A03	SCT
A04	SCR
A05	CAR
A06	RD
A07	RG1
A17	SD
A18	GND
A19	RC
A20	GND
A21	RS
A22	GND
B01	GND
B02	GND
B03	GND
B04	GND
B05	GND
B06	GND
B07	GND
B13	KEY

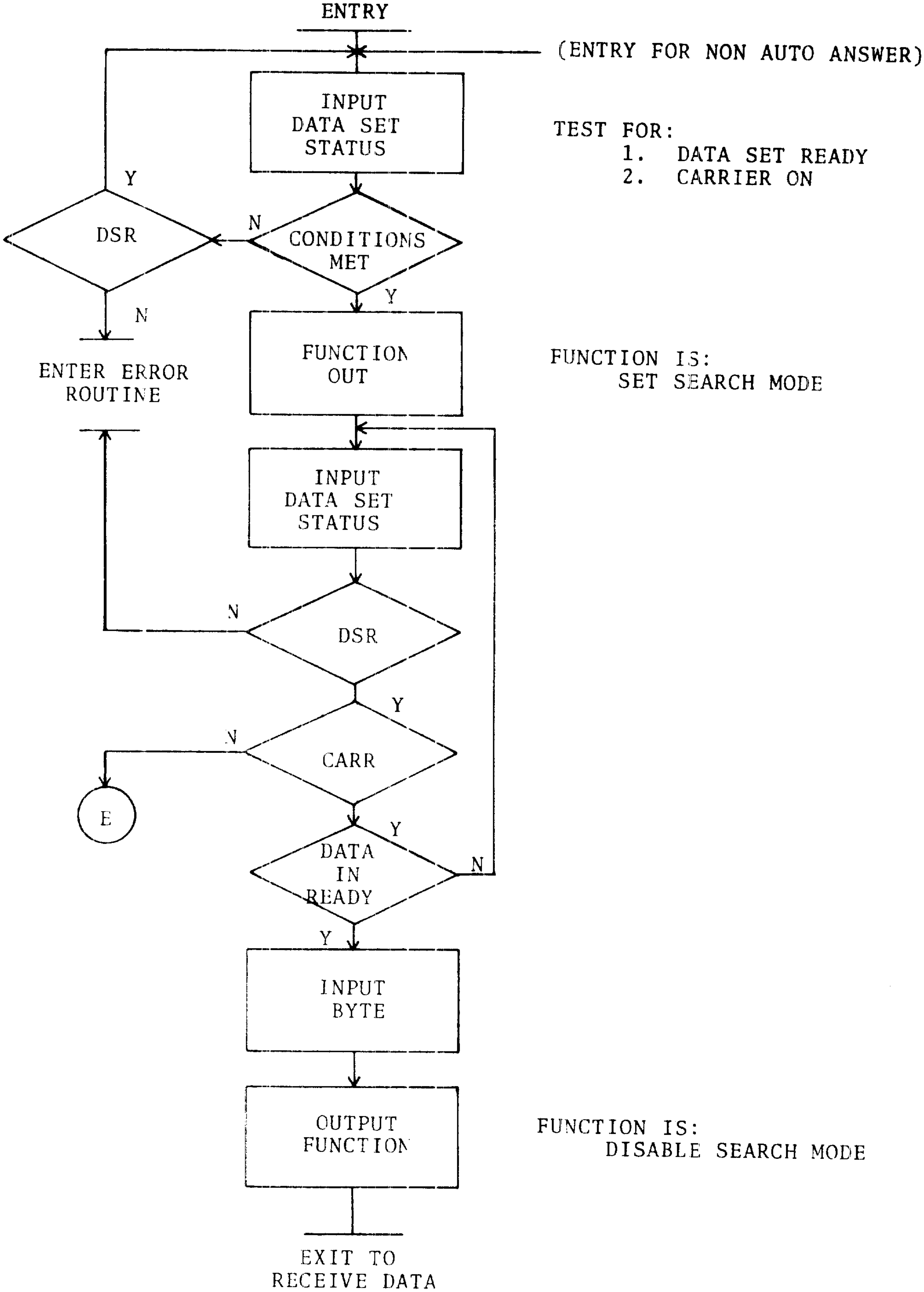
3.10.4 Flow Charts

The following flow charts are included to indicate the firmware routines which may be written to create specific routines related to operational use of the Synchronous Modem Interface.

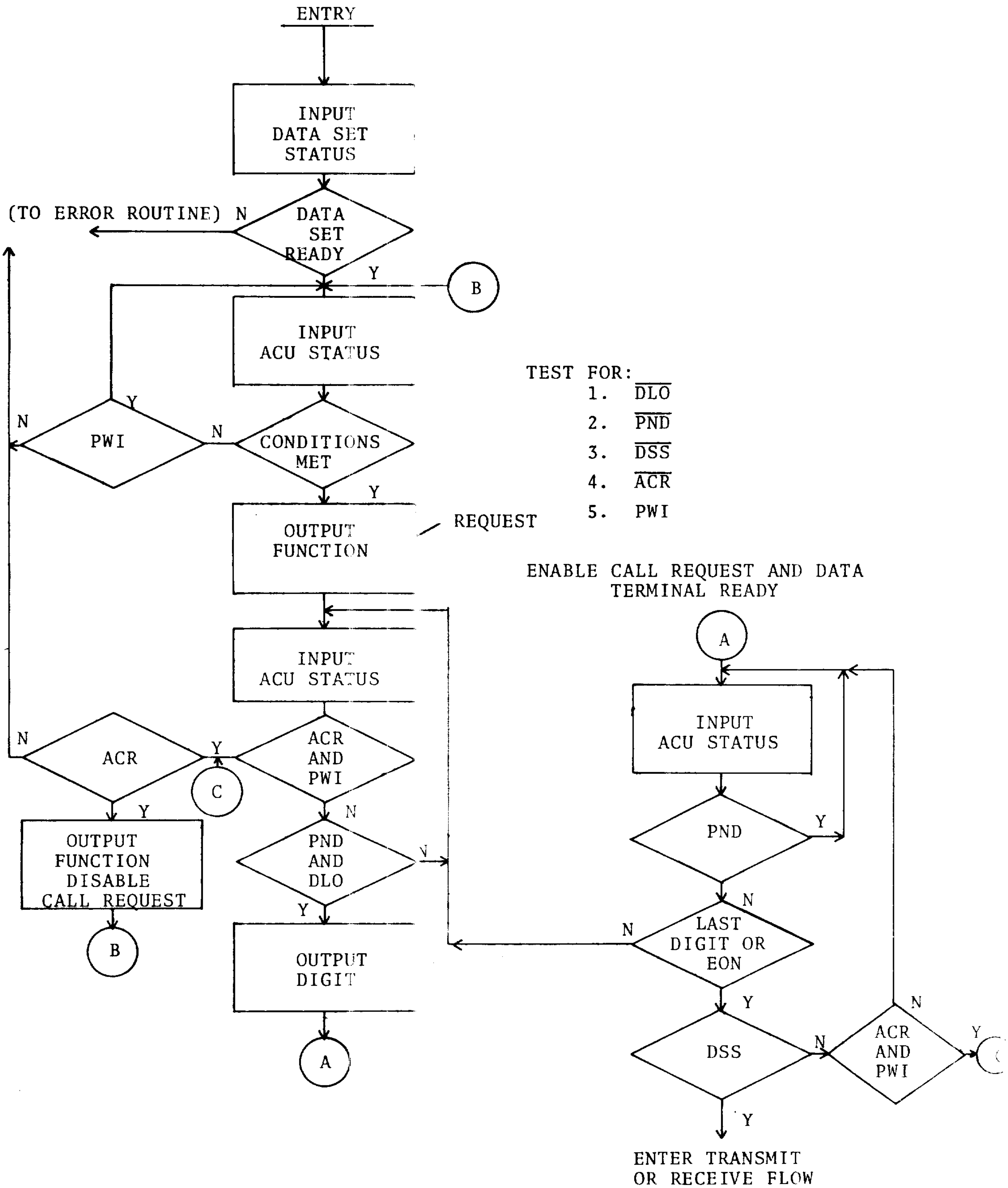
TRANSMIT INFORMATION FLOW



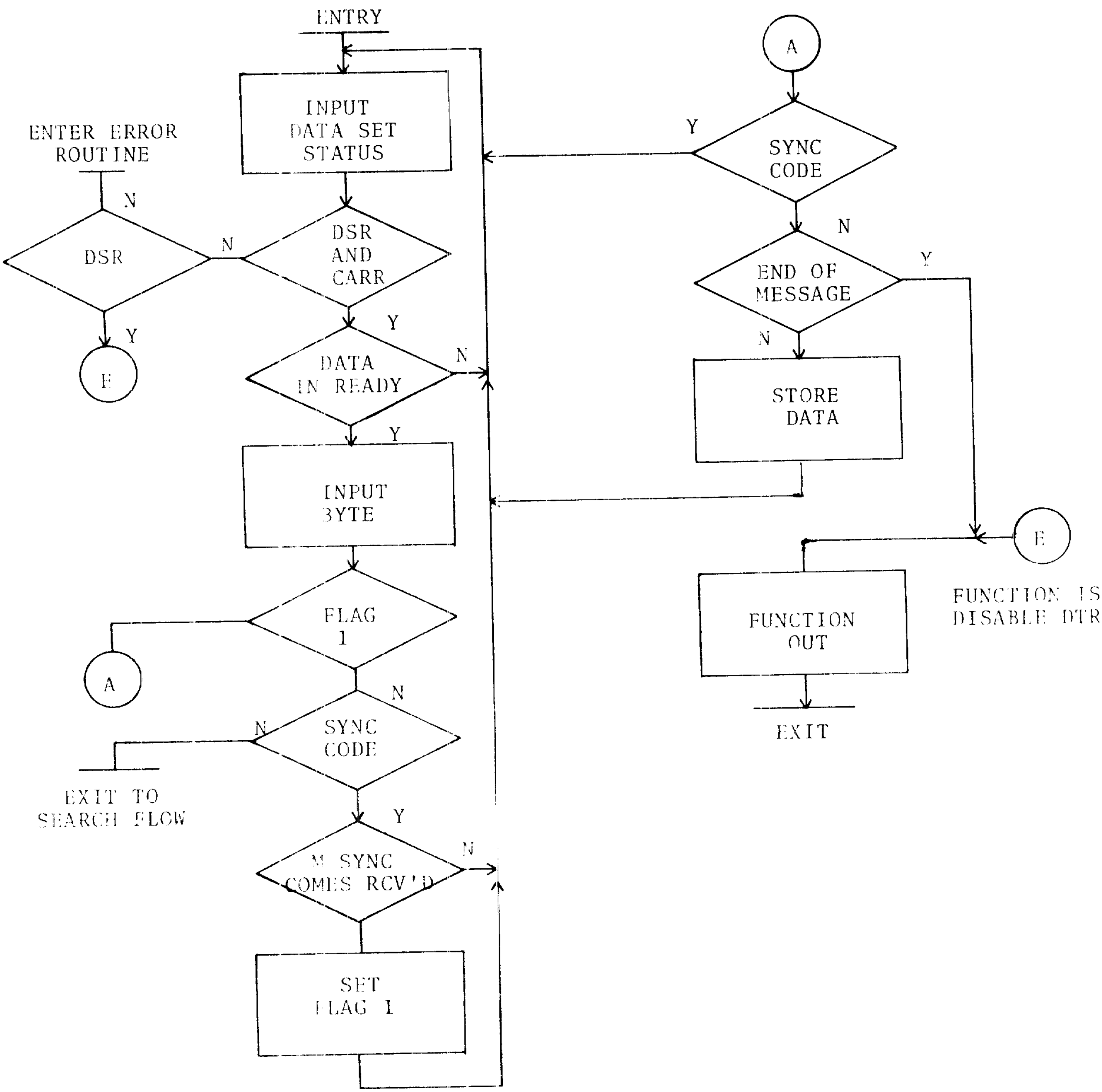
RECEIVE SYNC FLOW



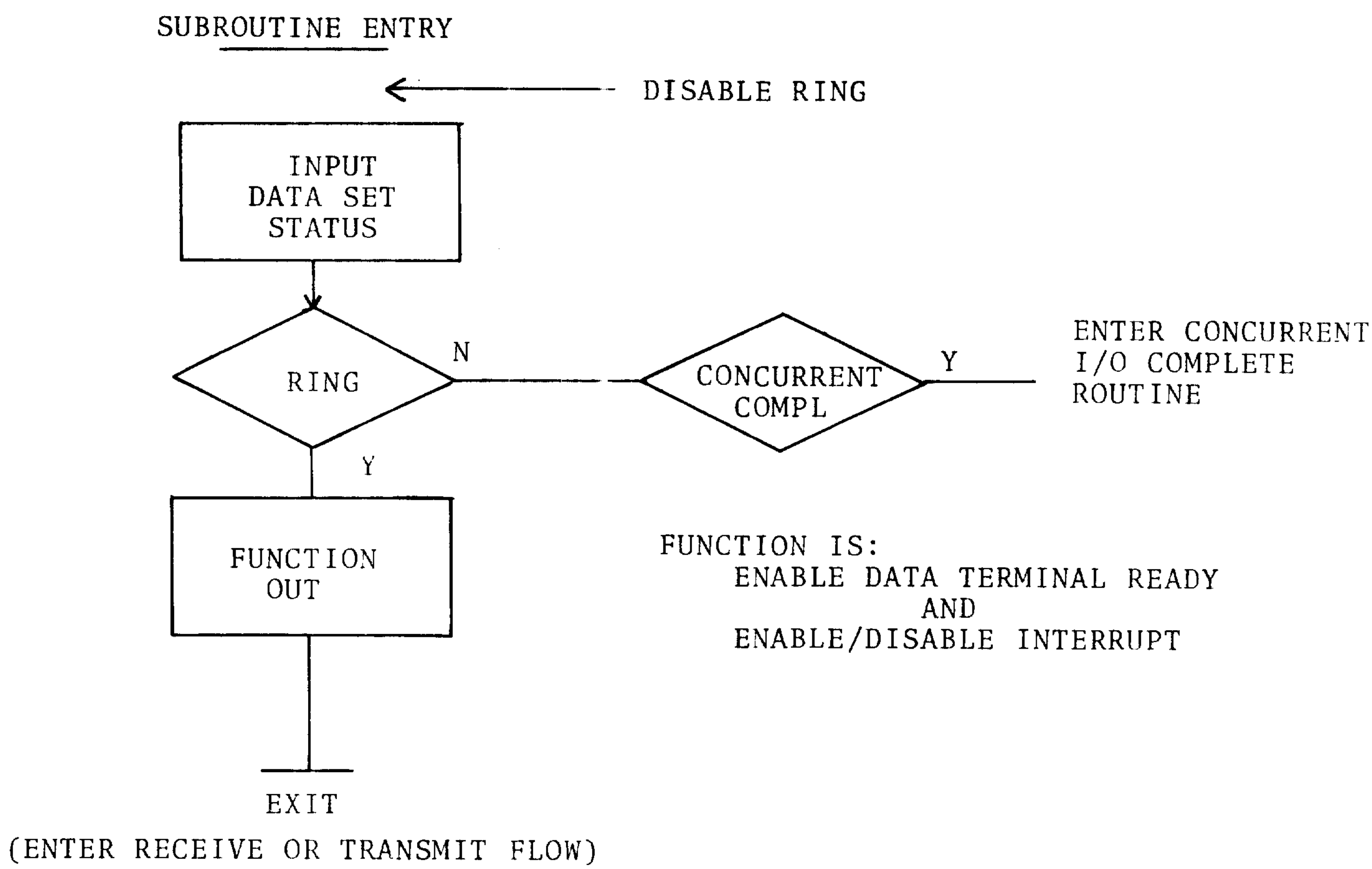
AUTO DIAL FLOW



RECEIVE DATA FLOW



AUTC ANSWER


SUBROUTINE ENTRY
DISABLE RING
INPUT DATA SET STATUS
RING
N
Y
CONCURRENT COMPL
Y
ENTER CONCURRENT I/O COMPLETE ROUTINE
FUNCTION OUT
FUNCTION IS:
ENABLE DATA TERMINAL READY
AND
ENABLE/DISABLE INTERRUPT
EXIT
(ENTER RECEIVE OR TRANSMIT FLOW)

3.11 INPUT/OUTPUT

3.11.1 General

This section describes the three primary input/output interfaces of the computer and provides guidelines for connecting external equipment to the interfaces. The information in this section should not be considered the final authority for the I/O interface configuration of any particular machine. The final authority in all cases is the latest revision of all applicalble engineering drawings and specifications.

Input/output operations in the computer are performed under control of microcommands designed for a wide range of I/O operations.

3.11.1.1 I/O System Organization

A block diagram of a typical computer system is illustrated in Figure 96. The three primary I/O interfaces shown in Figure 96 are the serial I/O interface between the Teletype and the processor, the parallel byte I/O interface (both internal and external), and the I/O interface to the direct memory access (DMA) channels.

These three interfaces provide the system designer with the flexibility to structure efficient I/O systems for a wide range of applications. The serial I/O interface, although normally used with a Teletype, can be used for other bit-serial devices as well. The byte I/O interface can be used by controller circuit boards that plug into the mainframe chassis, or it can be extended to an expansion chassis through the I/O Line Driver and Receiver circuit board option. In the configuration shown in Figure 96, an expansion chassis is used for additional controller and optional Priority Interrupt circuit boards. The Priority Interrupt boards can also be located in the mainframe chassis. The DMA interface provides the facility for external I/O devices to communicate directly with core memory through optional DMA channels located in the mainframe chassis.

3.11.1.2 Serial I/O Interface

The serial I/O interface is designed for communicating with a full duplex Teletype. Character assembly and disassembly, including all timing and synchronization, are performed at the microprogram level in the computer.

3.11.1.3 Byte I/O Interface

Data transfers through the byte I/O interface are basically two-phase operations. During the first phase a control byte is placed on the byte I/O bus. The control byte contains a device number specifying the address of one of the I/O devices connected to the bus and a device order signifying the type of operation to be performed during the transfer (data transfer, status/function transfer, and so on). All devices on the bus examine the device number, but only the device with a matching address accepts the control byte and logically connects itself to the bus for the subsequent data byte transfer. During the second phase of the byte I/O operation a single byte is transferred to or from the I/O device. After each byte transfer the device disconnects itself from the bus.

As shown in Figure 96, I/O devices can be connected to the byte I/O interface at the internal byte I/O bus inside the mainframe chassis or to the external byte I/O bus outside the mainframe chassis in an expansion chassis. The external byte I/O bus is an extension of the internal bus brought out of the mainframe chassis through an optional plug-in I/O Line Driver and Receiver board. The I/O Line Driver and Receiver board is one of several optional I/O interface circuit boards available for use with the computer. All of the boards are made to plug into the mainframe chassis, but they can be used as well in an expansion chassis.

Although the external byte I/O bus is an extension of the internal bus, there are a few major differences between them. These differences are as follows:

a. All nine output lines of the external byte I/O interface are buffered by nine type 944 DTL drivers for driving terminated lines.

b. Outputs from the three control flip flops of the I/O control register are directly abailable at the internal interface, but are decoded and made available at the external interface on seven individual lines buffered by type 944 DTL drivers.

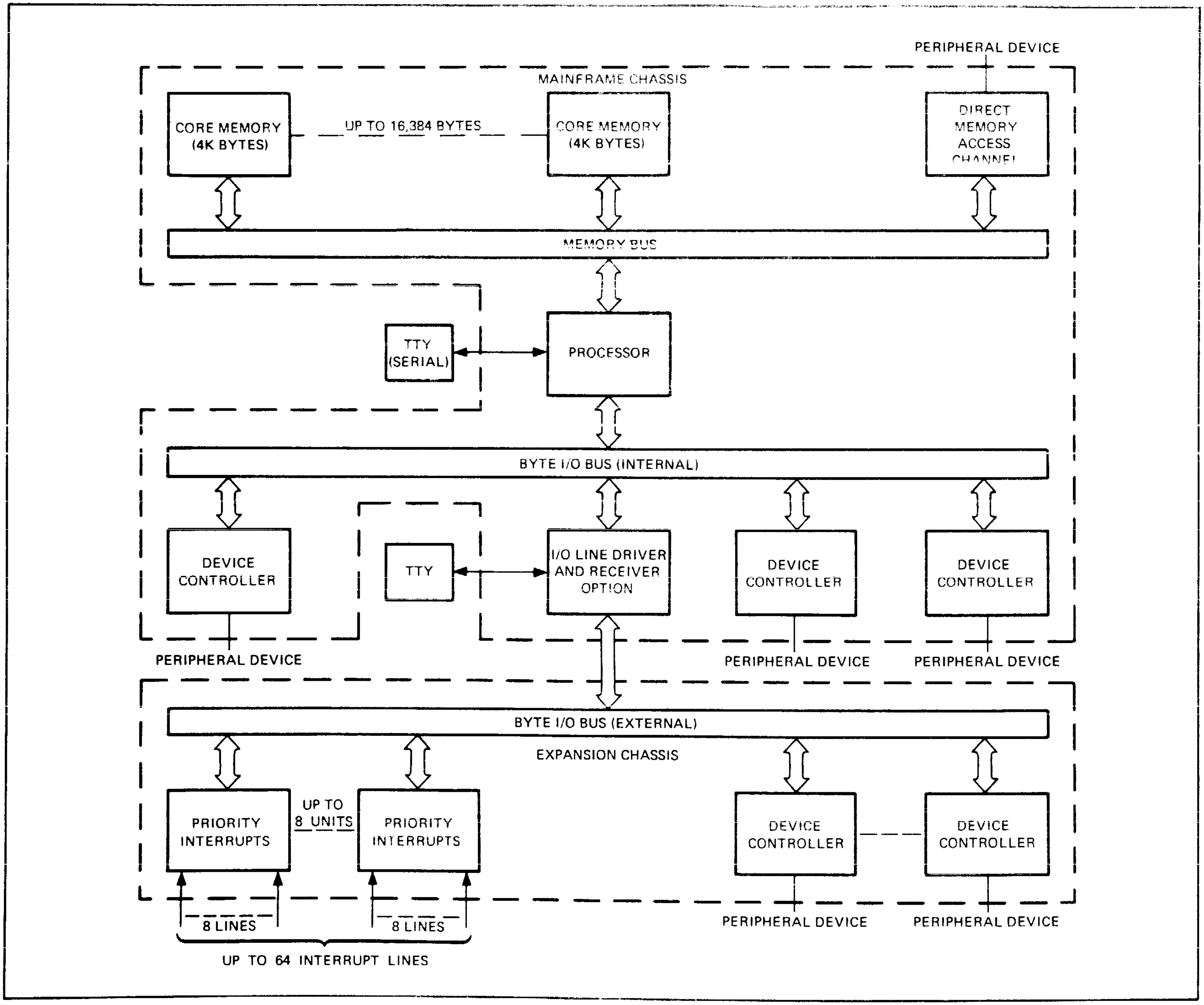

PERIPHERAL DEVICE
MAINFRAME CHASSIS
CORE MEMORY (4K BYTES)
UP TO 16,384 BYTES
CORE MEMORY (4K BYTES)
DIRECT MEMORY ACCESS CHANNEL
MEMORY BUS
TTY (SERIAL)
PROCESSOR
BYTE I/O BUS (INTERNAL)
DEVICE CONTROLLER
TTY
I/O LINE DRIVER AND RECEIVER OPTION
DEVICE CONTROLLER
DEVICE CONTROLLER
PERIPHERAL DEVICE
PERIPHERAL DEVICE
PERIPHERAL DEVICE
BYTE I/O BUS (EXTERNAL)
EXPANSION CHASSIS
PRIORITY INTERRUPTS
UP TO 8 UNITS
PRIORITY INTERRUPTS
DEVICE CONTROLLER
DEVICE CONTROLLER
8 LINES
8 LINES
UP TO 64 INTERRUPT LINES
PERIPHERAL DEVICE
PERIPHERAL DEVICE

FIGURE 96

c. The internal computer clock is used by interface boards connected to the internal bus, but a half-frequency, 50 percent duty cycle clock is used by boards connected to the external bus.

3.11.1.4 External Priority Interrupts

The external interrupt system of the computer operates through the byte I/O interface. Interrupts can originate from device controllers or from optional Priority Interrupt interface boards connected to the byte I/O bus. Each Priority Interrupt interface board provides control of eight interrupt signals. Up to eight boards can be used in one system to control a maximum of 64 interrupt signals.

The byte I/O interface contains a single interrupt line common to all I/O devices on the byte I/O bus and a hard-wired priority line that is carried through all devices on the bus. Each I/O device receives priority from the preceding device in the priority chain and passes it along to the next device in line if it is not ready to request an interrupt. A device receiving priority and ready to request an interrupt does not pass along the priority signal, but instead activates the interrupt signal.

After receiving acknowledgment of the interrupt request, the interrupting device places on the I/O bus an address byte that the processor uses to transfer program control to the proper interrupt servicing routine.

Detailed descriptions of the timing, logic, and instructions associated with the byte I/O interface are given later in this section.

3.11.2 Serial I/O Interface

3.11.2.1 General

The serial Teletype I/O interface is a standard feature of the computer. A Model 33 or 35 Teletype wired for four-wire, full duplex, 20-mA operation can be connected directly to the cable provided with the computer.

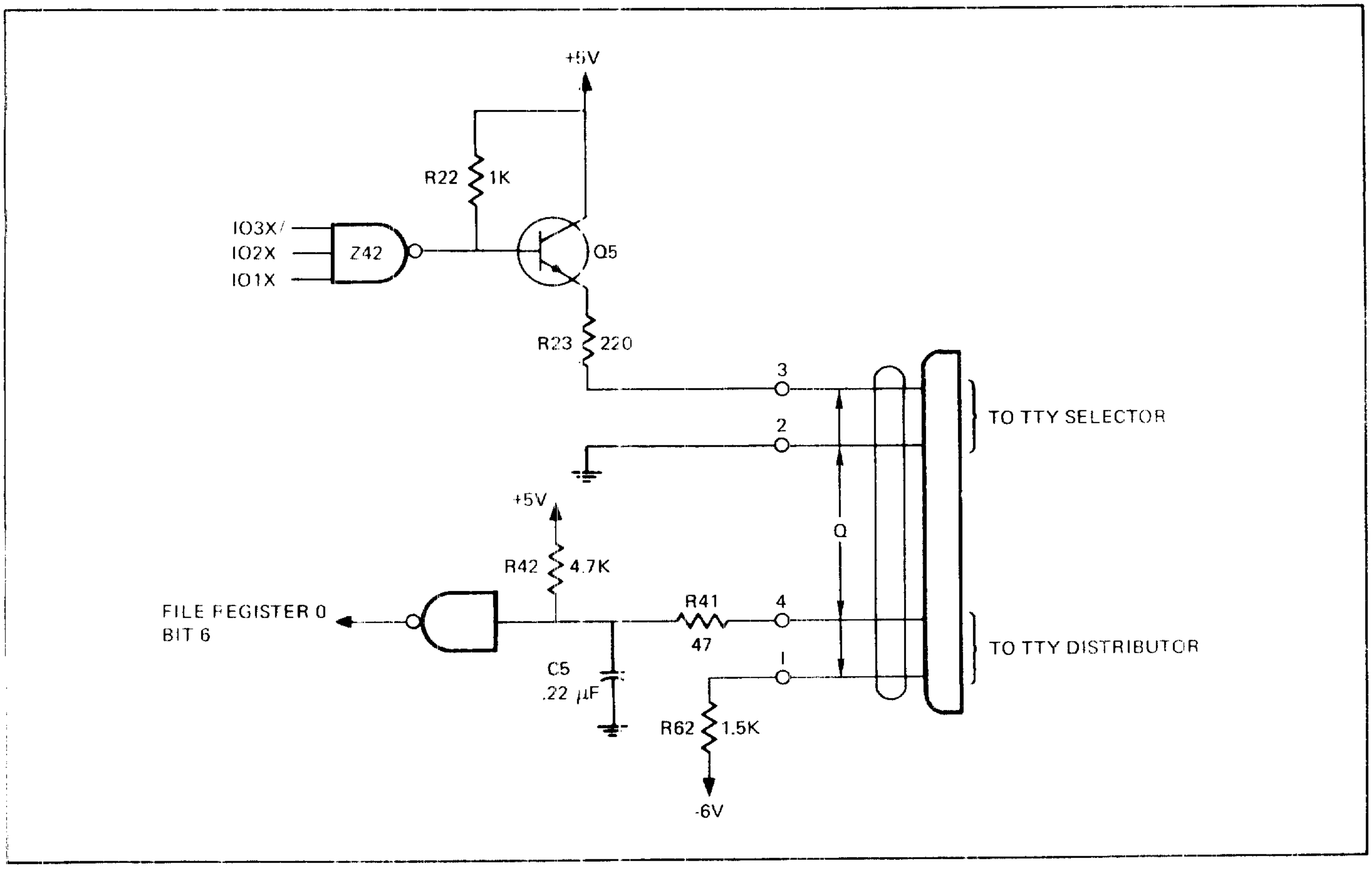


FIGURE 97

The four-wire I/O interface circuit is shown in Figure 97. The transmit portion of the circuit contains a 20-mA current source that can be turned on or off depending on the state of the I/O control register. When the I/O control register is in any mode other than mode 3, the output of gate Z42 is high, emitter follower Q5 conducts, and approximately 20-mA of current is available through resistor R23. This current holds the Teletype in the mark condition. When the I/O control register is set to mode 3 by a microcommand, the output of gate Z42 is low, emitter follower Q5 cuts off, and no current flows to the Teletype.

The receive portion of the interface circuit contains a low-pass filter network connecting the Teletype distributor to bit 6 of file register 0 where it may be sensed by microcommands. One side of the Teletype distributor is connected to -6V through resistor R62. The other side of the distributor is connected to a TTL gate, which forms bit 6 of file register 0. When the Teletype sends a mark signal, the output of the gate is held low and a 0-bit appears in bit 6 of file register 0. When the Teletype sends a space signal, a 1-bit appears in bit 6 of file register 0.

3.11.2.2 Character Assembly and Disassembly

Teletype character assembly, disassembly, synchronization, and timing in the computer is accomplished by a firmware routine. Figure 98 shows the timing for transmitting or receiving 110-baud Teletype characters.

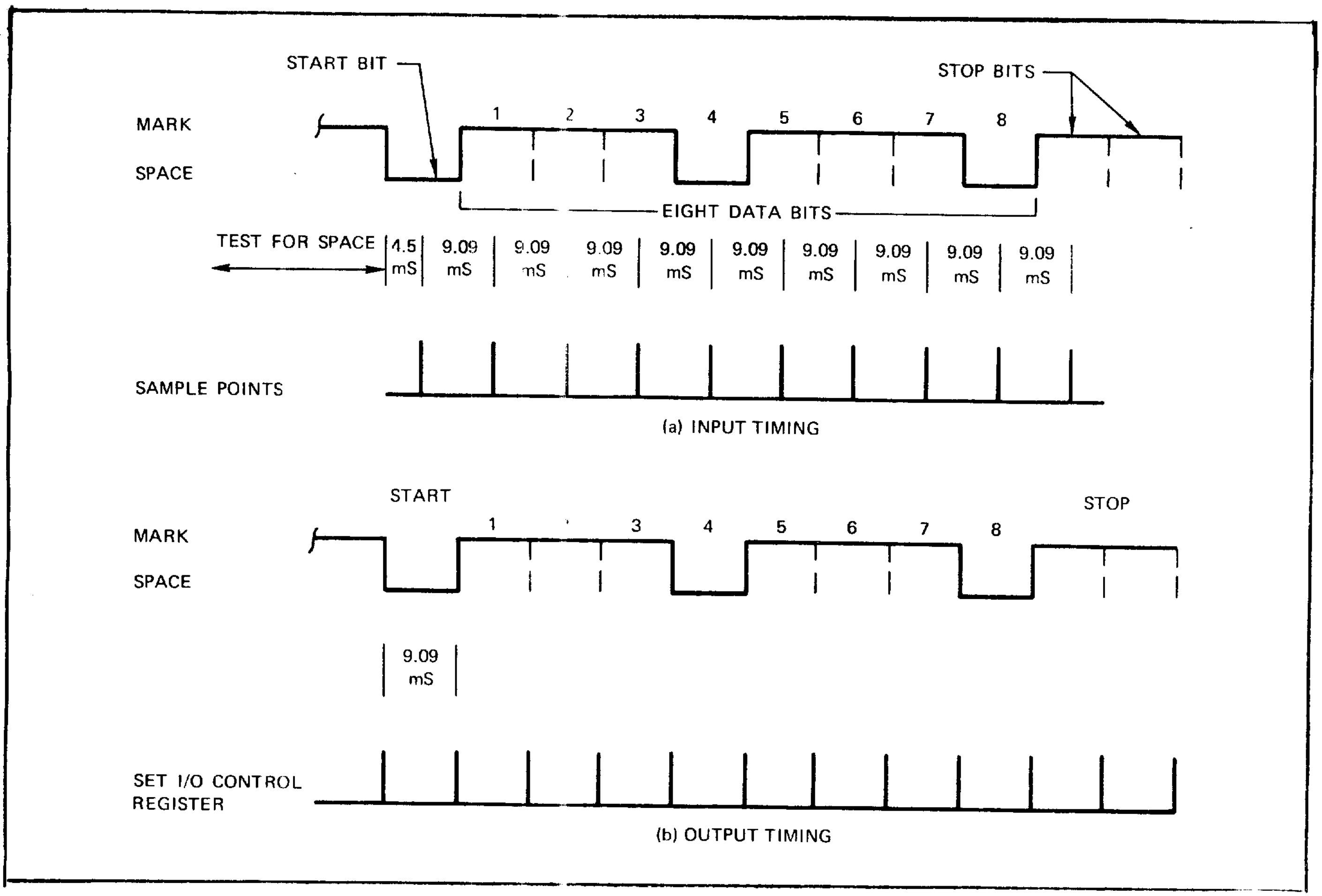


FIGURE 98

During an input operation the firmware program searches for the leading edge of the start bit by continuously testing the Teletype input lines. Once a space level is detected the firmware program delays 4.5 milliseconds and then samples the input every 9.09 milliseconds until the eighth information bit is shifted into the assembly register. The initial delay of 4.5 milliseconds after detecting the leading edge of the start bit causes sampling to occur in the middle of each signaling element.

During an output operation the firmware program sets the I/O control register to the appropriate mark or space condition every 9.09 milliseconds according to the start and stop bits and the data to be serially transmitted. Before the first information bit is transferred, the I/O control register is set to mode 3 to transmit the start bit. The firmware program for transmitting a Teletype character remains active for 11 intervals (100 milliseconds) to assure the proper stop interval before the next character is transmitted.

3.11.2.3 Microcommands for Serial I/O

References to the serial input bit and generation of serial output bits are under microcommand control.

The serial input bit is constantly available as bit 6 of file register zero. Access to this bit is usually performed by the Test Zero (TZ) or Test Non-Zero (TN) microcommands. These commands are 4040 and 5040 respectively.

The state of the serial output bit is affected by bits 4-7 of the Control microcommand. To space the serial Teletype, the Command instruction 7XBX is executed. To change the serial output bit to a mark state, any Control type command is executed with the value of bits 4-7 in the range of 1000 through 1111-excluding pattern 1011 which corresponds to the space operation.

3.11.3 Byte I/O Interfaces

3.11.3.1 General

The byte I/O interfaces (both internal and external) comprise eight input data lines, five input control lines, eight output data lines, ten (internal) or thirteen (external) output control lines, and three spare lines. Figure 99 shows the internal and external byte I/O data and control signals including the point of origin or destination in the processor for all interface lines. It also shows the interface logic on the I/O Line Driver and Receiver interface option (shown plugged into connector J21) and shows how the option is used to extend the byte I/O bus to logic external to the computer chassis.

3.11.3.2 Byte I/O Bus

The following paragraphs describe the input and output data lines and the control lines of the byte I/O bus. Except where specifically stated otherwise, the descriptions apply to both the internal and external byte I/O buses.

3.11.3.3 Input Data Lines

Input data lines ID00/through ID07/ are continuous from the last interface unit on the I/O cable through the I/O Line Driver and Receiver board, the backplane, and into the processor via B-bus. A termination network for each line is located in the processor. The lines are driven by DTL or TTL power gates (944 or equivalent) with uncommitted collectors. Because of the termination network, the lines are allowed to swing only between ground and +3V. Each line is at ground potential when any one of the power gates on the line is turned on. Each line is at +3V when all gates on the line are off. When a gate is switched on, the line to which it is connected places a logical 1 onto the B-bus and into the destination registers.

The input data lines are handled exactly the same whether a device controller is connected to mainframe connectors J16 through J21 or to the I/O cable in the expansion chassis.

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3.11.3.4 Output Data Lines

Output data lines T00X/ through T07X/ and 0D00/ through 0D07/ connect the processor T-Register to external I/O devices. The T-register is the physical source for output data. Data or address information to be transferred to an I/O device is first fetched from a register or memory and then placed in the T-register. From the T-register it is transferred to the I/O device.

Lines T00X/ through T07X/ are available at mainframe byte I/O connectors J16 through J21. Lines 0D00/ through 0D07/ are the external byte I/O equivalent of lines T00X/ through T07X/. They carry the same signals (slightly delayed) through the I/O cable to the expansion chassis.

To preserve the expansion capability of the output data bus, each device controller on the bus is restricted to a single unit load (one DTL or TTL gate) or 1.6 mA maximum on each output data line. Both the T0XX/ and 0DXX/ lines have the following characteristics:

T-Register Content	T0XX/	0DXX/
Binary 1	0V	0V
Binary 0	+4V (nom)	+3V (nom)

3.11.3.5 Input Control Lines

The five input control lines available at the byte I/O interface are:

a. ECIO/ - concurrent I/O request

b. ERPY/ - I/O reply

c. EINT/ - external interrupt

d. SELI/ - Select in

e. PRIN/ - priority return

All five lines are continuous from the last interface unit on the I/O cable, through the I/O Line Driver and Receiver board, the backplane, and into the processor. The lines are driven by DTL or TTL power gates (944 or equivalent) with uncommitted collectors. A termination network for each line is included in the processor. Because of the termination networks, the lines are allowed to swing only between ground and +3V. All five lines are active, or indicate assertion, when they are at ground potential. For example, ground on line EINT/ causes an external interrupt.

Input control lines ECIO/, ERPY/, and EINT/ provide inputs to file register 0 in the processor. The status of these lines can be determined in the microprogram by testing the associated bits of the file register.

Line ECIO/ is used as the concurrent I/O request signal and is shared by all device controllers. This signal becomes bit 3 of file register 0. It is typically used by the microprogram to initiate a concurrent type data transfer. It is included for those system designers who may want to effect their own microprogrammed I/O transfers.

Line EINT/ is the external interrupt line, which is shared by all Priority Interrupt boards and device controllers. It becomes bit 7 of file register 0. It typically causes the processor to discontinue normal macro instruction execution and begin a firmware sequence to determine the address of the interrupt device.

Line PRIN/ is the priority input line from the next higher priority controller. It is used by each controller in determining priority before requesting an external interrupt.

3.11.3.6 Output Control Lines

Of all the interface lines, only the output control lines are functionally different at the internal and external byte I/O interfaces.

The following lines are available at each interface:

Internal Interface	External Interface
I01X/	COXE/
I02X/	DOXE/
I03X/	SP1/
CPH1	CAKE/
CPH2/	IAKE/
MRST/	DIXE/
PROT/	SP3/
PRIN/	KOXE/
SEL0/	MRES/
SELI/	PROT/
CSTP/	PRIN/
	SEL0/
	SELI/

3.11.3.7 Internal Byte I/O Control Lines (Mainframe Chassis)

Internal I/O control lines I01X/ through I03X/ originate at the false outputs of the three I/O control flip flops in the processor. These flip flops are set and reset at the microcommand level. The eight states that the flip flops can assume are assigned meanings to indicate various I/O control modes. Definitions of the eight control flip flop states for the computer are given in Table 12. Other definitions can be applied for specialized computer configurations.

TABLE 12

0	None	None
1	Control output	COXX/
2	Data output	DOXX/
3	Space serial Teletype	SP1/
4	Spare	SP2/
5	I/O acknowledge	IOAK/
6	Data input	DIXX/
7	Spare	SP3/

As shown in Figure 99, lines IO1X/ through IO3X/ are decoded on the I/O Line Driver and Receiver board, and seven lines are then available (state 0 is not used) at the external interface. A device controller designed for use in the mainframe chassis must decode these three lines, as needed, as is done on the I/O Line Driver and Receiver board. Device controllers designed for the processor are required to decode only states 1 (COXE/), 2 (DOXE/), 4 (CAKE/), 5 (IAKE/), and 6 (DIXE/). These states represent control output, data output, concurrent acknowledge, interrupt acknowledge, and data input functions, respectively.

It is important to remember that a device controller in the mainframe chassis must decode the I/O control flip flop lines, but one in the expansion chassis does not, since the external bus is used to connect the two chassis.

Lines CPH1 and CPH2/ provide processor clock signals to device controllers connected to the mainframe byte I/O connectors. Each line can be used independently as a square wave source (4.55 MHz), or they may be used together in a NAND gate to produce a 35 ns clock pulse (CPH1 is inverted and delayed 35 ns from CPH2/). The relationship of the signals on lines CPH1 and CPH2/ is shown in Figure 100.

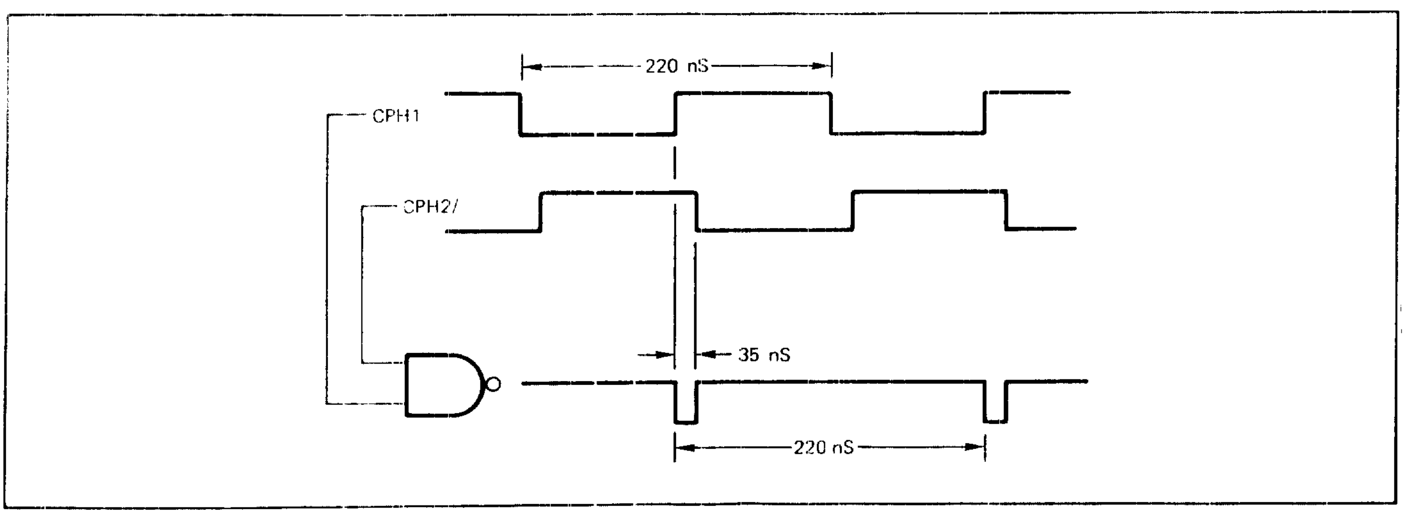

FIGURE 100

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Control line CSTP/ of the internal byte I/O interface carries a signal to indicate that the internal processor clock has been stopped for either of the following reasons:

a. The processor is halted.

b. The processor is executing a logical pause (for 1 to 5 clock times) while performing a jump or attempting to overrun a memory operation during a microcommand sequence.

Line CSTP/ is available to gate clocks in device controllers when intimate microlevel control of a device is required. It is not included in standard byte I/O interfaces and must be jumpered to an open pin of an option board connector if its use is required.

Control line MRST/ is the master reset line. It is activated by the RESET or SAVE switch on the operator's console, or by the optional power fail circuit during power failure or restart. It is used to clear all control flip flops to their initialized conditions. Ground potential is applied to this line when the RESET or SAVE switch is pressed. MRST/ is double buffered and becomes MRES/ in the expansion chassis.

Control line PROT/ carries the Interrupt priority signal from controller to controller. It becomes line PRIN/ at the input of the next lower priority controller. Backplane strapping on the mainframe chassis determines the relative priority of devices on the I/O bus. A modification of the strapping permits interface units in the mainframe chassis to have lower priority than units in the expansion chassis at the end of the I/O cable. Standard strapping is provided on connectors J18-J21 in that each board in order from J18-J21 has higher priority.

Line SEZI/ is the Priority input line from the next higher priority Controller. It is used by each Controller in determining priority during an interrupt or concurrent acknowledge sequence.

Control line SELO/ carries the priority signal from controller to controller to enable the requesting device to place its address on the bus during an I/O acknowledge sequence. This line becomes SELI/ at the input of the next lower priority device. Strapping of this priority line is standard on connectors J18-J21. A modification of the strapping permits interface units in the mainframe chassis to have lower priority than units in the expansion chassis.

3.11.3.8 External Byte I/O Control Lines (I/O Cable)

Figure 99 shows how the output control lines are modified in the I/O Line Driver and Receiver board to develop the control lines available in the I/O cable. As explained in the preceding paragraph, lines IO1X/ through IO3X/ are converted into unitary control lines. The main reason for this conversion is to eliminate ambiguity caused by flip flop cross-over variations. These crossover variations could produce spikes that would cause incorrect operation, if the decoded terms were used as clocks. This problem can be overcome in the mainframe chassis by using a synchronous clock created from signals CPH1 and CPH2/. Since this solution is unacceptable at the end of the I/O cable, the outputs of the three I/O control flip flops are converted into seven unitary lines on the I/O Line Driver and Receiver board after crossover skew has been eliminated.

Of the seven decoded control lines available at the I/O cable, only five are presently used for byte I/O operations: COXE/, DOXE/, CAKE/, IAKE/, and DIXE/. Lines SP1/, and SP3/ are spare control lines that are not used in the computer. They can be used to carry I/O control signals originated by special firmware.

NOTE

Although control line SP1/ is considered a spare, it represents I/O control state 3, which is the space serial Teletype mode. This line can be used only in the absence of the serial Teletype.

Control line COXE/ carries a low signal to specify that a control byte containing a device number and device order is on the output data lines. The device being addressed accepts the byte and decodes the order.

Control line DOXE/ carries a low signal to specify that an information byte is on the output data lines. The previously addressed device accepts the byte.

Control line IAKE/ carries a low signal to acknowledge a request from an I/O device for an interrupt. The requesting device uses the signal to transfer an address byte on the input data lines to the processor.

Control line CAKE/ carries a low signal to acknowledge a request from an I/O device for a concurrent transfer.

Control line DIXE/ carries a low signal that is used by a previously addressed I/O device to transfer an information byte on the input data lines to the processor.

Control line KOXE/ carries a 2.275-MHz, 50% duty cycle clock signal that can be used by external devices for timing.

Control lines PRIN/, SELI/, and SELO/ have the same meaning in the I/O cable as they do for the internal byte I/O interface.

3.11.3.9 Spare Lines

Spare lines SP4 through SP7 are continuous from the last interface unit on the I/O cable, through the I/O Line Driver and Receiver board, and onto the backplane. These lines are not terminated in any way and are provided only for special user requirements.

3.11.3.10 Byte I/O Fundamentals

Although the flexibility of the byte I/O system lends itself to customizing for individual applications, certain standard conventions have been adopted for byte I/O operations in the computer. These conventions are described in the following paragraphs.

3.11.3.11 Device Addressing

Each I/O device on the byte I/O bus is assigned a unique five-bit device address or number. On most controllers, the addresses are selected by the placement of jumper wires on the printed circuit board of the controller.

Each device controller on the I/O bus determines if it is being addressed by comparing its assigned address to the five-bit device number in the control byte sent to all controllers on the output data lines. The device number portion of the control byte appears on data lines T00X/ through T04X/ (OD00/ through OD04/). The assigned device address is also used to identify the I/O device requesting an interrupt or concurrent I/O transfer. The processor acknowledges each request with signal IAKE/ or CAKE/. On receiving the acknowledge signal, along with SELI/, the requesting device places its address (times 2) on input data lines ID01/ through ID05/.

Table 13 lists the device addresses assigned to the standard interface units. Customer-designed controllers should not use the assigned addresses if the use of standard controllers is planned.

Table 13. Standard I/O Device Addresses

Address (Hexadecimal)	I/O Device
00	Teletype (parallel interface)
01	Low-Speed Asynchronous Modem or Teletype Interface
02	High-Speed Paper Tape Reader
03	High-Speed Paper Tape Punch
04	Card Reader
05	Not assigned
06	Drum/Disc
07	Not assigned
08	32 x 32 Discrete Input/Output Interface option
09 and 10	Not assigned
11	Low-Speed Asynchronous Modem or Teletype Interface
12 and 15	Not assigned
16	DMA Selector Channel No. 1
17	DMA Selector Channel No. 2
18	Priority Interrupt Group 7
19	Priority Interrupt Group 6
1A	Priority Interrupt Group 5
1B	Priority Interrupt Group 4
1C	Priority Interrupt Group 3
1D	Priority Interrupt Group 2
1E	Priority Interrupt Group 1
1F	Priority Interrupt Group 0

3.11.3.12 Device Orders

Accompanying the five-bit device address in the control byte sent to all devices before each programmed transfer, is a three-bit device order specifying the I/O operation to be performed by the device. The device order portion of the control byte appears on output data lines T05X/ through T07X/ (OD05/ through OD07/). A list of standard device orders is given in Table 14. Not all device controllers are required to use all the orders listed in the Table. Their use is dictated by controller design.

ORDER NUMBER	OPERATION	DESCRIPTION
0	Data	The data order causes a data byte to be transferred between the processor and the addressed device. The direction of transfer depends on the type of instruction (input or output).
1	Status/function	The status/function order causes a status byte to be transferred from the addressed device to the processor, or a function byte to be transferred from the processor to the device depending on the type of instruction (input or output).
2	Block input	The block input order notifies the device to proceed with a concurrent block input to memory. This order can be sent with either an input or an output instruction.
3	Block Input with interrupt	The block input with interrupt order notifies the device to proceed with a concurrent block input to memory and to generate an interrupt at the end of the transfer. This order can be sent with either an input or output instruction.
4	Stop	The stop order causes the block input or output operation in progress to be stopped. An external interrupt is generated if an interrupt would normally have been generated at the end of the block transfer.

ORDER NUMBER	OPERATION	DESCRIPTION
5	Protect State	The protect state order allows the device to write into protected areas of memory with concurrent input. The device is taken out of this mode at the end of the transfer.
6	Block output	The block output order notifies the device to proceed with a concurrent block output from memory. This order can be sent with either an input or an output instruction.
7	Block output with interrupt	The block output with interrupt order notifies the device to proceed with a concurrent block output from memory and to generate an interrupt at the end of the transfer. This order can be sent with either an input or an output instruction.

TABLE 14

STANDARD I/O DEVICE ORDERS

3.11.3.13 Status Bytes

In response to a status order from the processor, the addressed I/O device places a status byte on input data lines ID00/ through ID07/.

3.11.3.14 Data Output Timing

The timing diagram for a typical data output operation is shown in figure 101. When an output byte instruction is executed, the second byte of the instruction containing the device address and order is placed on output data lines T00X/ through T07X/ (OD00/ through OD07/). A minimum of 220 ns later, control line COXX/ (COXE/) goes low to indicate the presence of a control byte on the output data lines. During the 880 ns that line COXX/ (COXE/) is low, each device controller on the bus examines lines T00X/ through T04X/ (OD00/ through OD04/) to determine if it is the controller being addressed. The controller whose address is on the lines connects itself for service and decodes and stores the device order on output data lines T05X/ through T07X/ (OD05/ through OD07/). When the controller is connected for service, it is susceptible to either data output or data input signals from the processor and transfers data accordingly. Once connected for service, the controller remains connected until a data output or data input signal occurs.

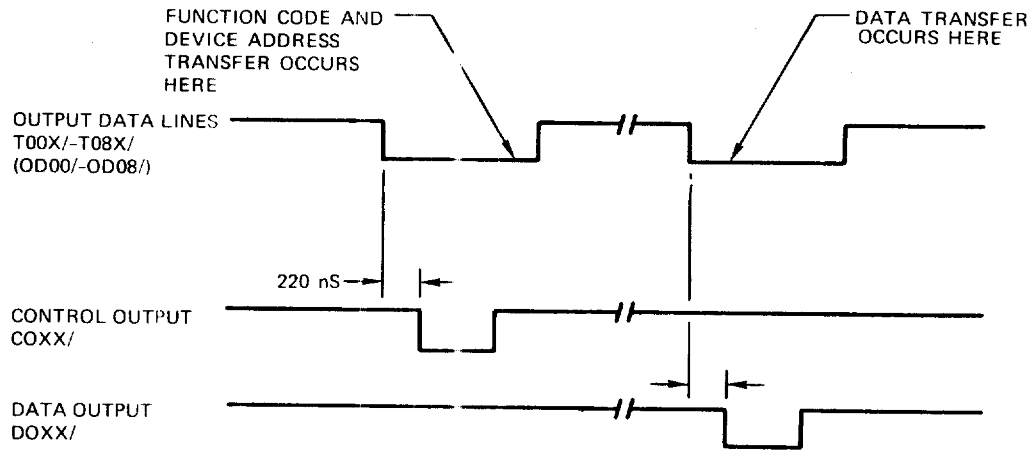


FIGURE 101
DATA OR FUNCTION OUTPUT TIMING

After removing the control output signal and control byte from the lines, the processor places a data byte on the output data lines. A minimum of 220 ns later, data output line DOXX/ (DOXE/) goes low to indicate the presence of data on the lines. The controller then strobes the data byte from the output data lines into its data register. When line DOXX/ (DOXE/) again goes high, the controller disconnects itself from further service.

3.11.3.15 Typical Data Output Logic

The timing diagram of figure 101 can be related to the typical data output logic shown in figure 102. The eight output data lines are connected to eight TTL or DTL inverters in the device controller. Each output line is buffered by an inverter or gate to minimize the loading on the line and to allow for expansion to the full number of devices. Receiver outputs (OD00/ through OD04/) are T00X/ through T07X/ applied to an address decoding circuit. In the example shown, the circuit is connected to decode a device address of 00 (all false terms are used).

Control lines COXX/ (COXE/) and DOXX/ (DOXE) are used for dual purposes in the example logic. Signal COXX (COXE) is used as a qualifying signal in the addressing decoding circuit, and its complement COXX/ (COXE/) is used to clock the connect-for-service flip-flop. Signal DOXX/ (DOXE/) is also used to clock the connect-for-service flip-flop and its complement (DOXX) (DOXE) generates the signal for strobing data into the controller register.

When the connect-for-service flip-flop sets, the controller is receptive to the actual transfer of data (the second phase of the data output operation). The signal for gating the output data lines into a device register or similar storage device is generated by the connect-for-service signal and control signal DOXX (DOXE) (data output).

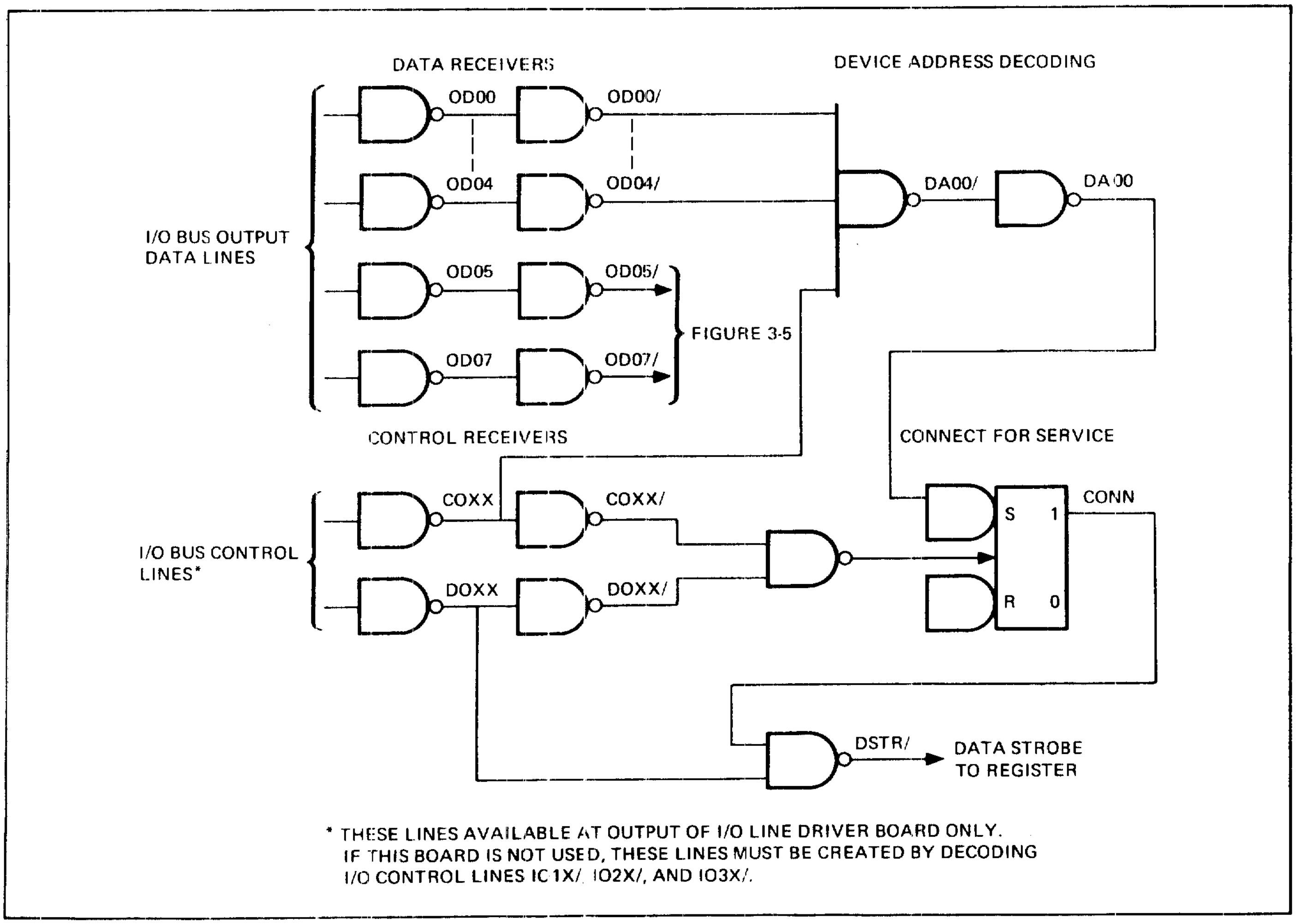


FIGURE 102
DATA OUTPUT LOGIC

3.11.3.16 Function Output Timing

The timing diagram shown in figure 101 for a data output operation is also valid for a function output operation. The function output operation is typically used to control a discrete action in an I/O device for which data transfer is not required. Rewinding tape is an example of such an action. The most efficient way to perform this operation is to issue a single instruction containing all the information necessary to alert the device and cause the tape to rewind.

On the 810 macro level, the output byte instruction (OBA, OBB, and OBM) is also used to perform the function output operation. The only difference in the instructions is the assignment of the f-code (bits 5 through 7) in the control byte of the instruction. When an output byte instruction is used for function output, the f-code of the control byte designates the unique function in the I/O device to be controlled. The assignment of f-codes for function operations precludes the use of the same codes for data transfer operations.

The function output operation is executed similarly to the data output operation described in paragraph 3.11.3.14. This data byte is usually ignored by the device controller, since the f-code of the control byte contains enough information to describe most function operations. However, should a controller require more function definition than is possible in the control byte, the data byte transferred during the function operation could be used to carry additional function information.

3.11.3.17 Typical Function Output Logic

The alerting of the device controller by sending the control output signal (COXX/) (COXE/) along with the device address is accomplished exactly as described for data output. When line COXX/ (COXE/) goes low, the controller examines TO5X/ through TO7X/ (OD05/ through OD07/) of the control byte and, if necessary, stores them so that it can perform the ordered function.

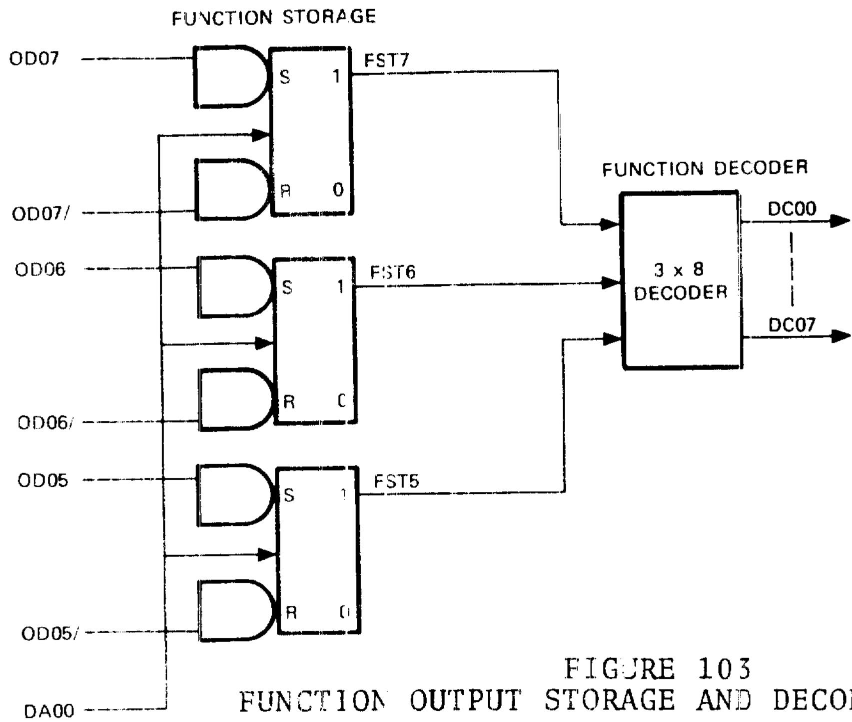


FIGURE 103
FUNCTION OUTPUT STORAGE AND DECODING LOGIC

Figure 103 shows typical logic for storing and then decoding the function bits. An alternative method would be to decode the function bits first (during DA00 time) and then store the decoded results in unitary flip-flops. This method would be advantageous when several control states are required, each one executing a separate function and each one having an asynchronous reset term dependent on the device.

The important point to remember is that functions needed for longer than the control pulse must be stored either before or after decoding. A suitable clock for storing this information is signal DA00, derived from the device address bits and signal COXX/ (COXE/).

3.11.3.18 Data Input Timing

The timing diagram for a typical data input operation is shown in figure 104. When an input byte instruction is executed, a two-phase data input operation, similar to data output, is performed. The first phase is identical to the first phase of the data output operation. The control byte containing the device address and order is placed on output data lines T00X/ through T07X/ (OD00/ through OD07/) by the processor, and then control output line COXX/ (COXE/) goes low. At that time the device controller connects itself for service and prepares to transfer data to the processor on input data lines ID00/ through ID07/. In terms of controller design, the device controller is not required to detect, during the device address phase, whether an input or output operation is to be performed. It can connect itself for service in either case and then allow the data input (DIXX/ or DOXE/) (DOXX/ or DOXE/) or data output control lines to direct its further activity.

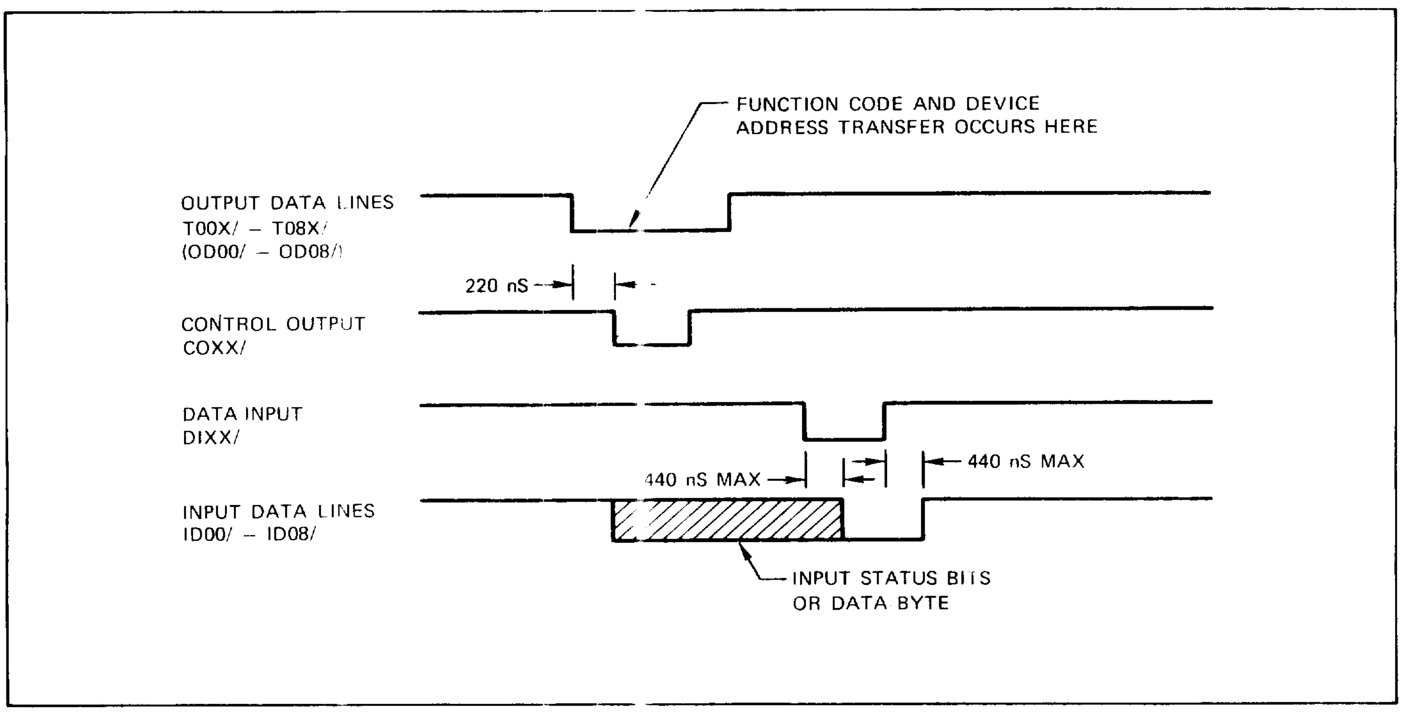


FIGURE 104
DATA OR STATUS INPUT TIMING

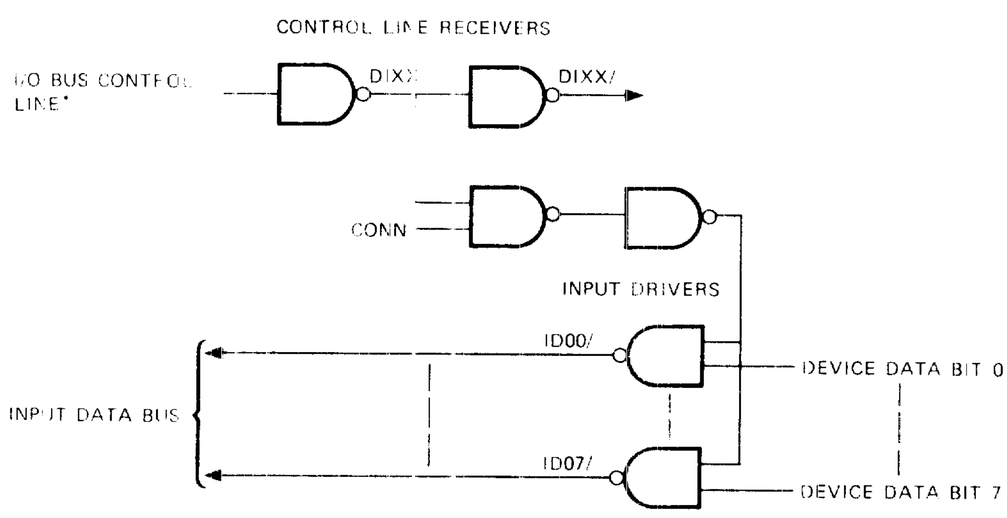
As shown in figure 104 after the control byte is removed from the output data lines, data input line DIXX/ (DIXE/) goes low. Device data to be transferred to the processor must be settled no later than 440 ns after line DIXX/ (DIXE/) goes low. The data byte can be applied to the input data lines as early as the beginning of signal COXX/ (COXE/). For interface design freedom, the input data may be applied even during an output byte instruction with no adverse effect.

The input data must be removed from the input data lines no later than 440 ns after line DIXX/ (DIXE/) goes high again.

For normal operation on the external byte I/O bus with less than a 30-foot twisted pair cable, it is feasible to use the DIXX/ (DIXE/) signal itself for gating or qualifying the application of input data to the input data lines.

3.11.3.19 Typical Data Input Logic

Figure 105 shows the additional logic required for a data input operation. Eight power drivers are used to drive the eight input data lines (ID00/ through ID07/). The power drivers are type 944 DTL or TTL (or equivalent) power gates with open collectors. A single pull-up resistor is contained in the processor. The power drivers must be held off when the device is not being addressed, and should be turned on only when the device is connected for service.



* THIS LINE AVAILABLE AT OUTPUT OF I/O LINE DRIVER BOARD ONLY. IF THIS BOARD IS NOT USED, THIS LINE MUST BE CREATED BY DECODING I/O CONTROL LINES IO1X/, IO2X/, AND IO3X/.

FIGURE 105 DATA INPUT LOGIC

3.11.3.20 Status Input Timing

The timing diagram shown in figure 104 for a data input operation is also valid for a status input operation. A similar relationship exists between a status input and data input operation as existed between a function output and data output operation. The input byte instructions are used both for data input and status input operations. To differentiate between the two operations, an f-code of 000 is used in the control byte for data transfer, but a code of 001 is used for status transfer. Otherwise, the operations are identical except that a status byte is placed on input data lines ID00/ through ID07/ instead of a data byte.

3.11.3.21 Typical Status Input Logic

Figure 106 shows the change in data input logic required to accommodate a status input operation. As shown in the example, the false terms of both data and status bits are used as inputs to the drivers. The function code stored during the control output phase of the operation (DC00 for data or DC01 for status) determines whether a data byte or a status byte is transferred to the processor over the input data lines.

The combination of logic shown in figures 102, 103 and 106 produces a device controller that can perform data output, data input, function output, and status input operations.

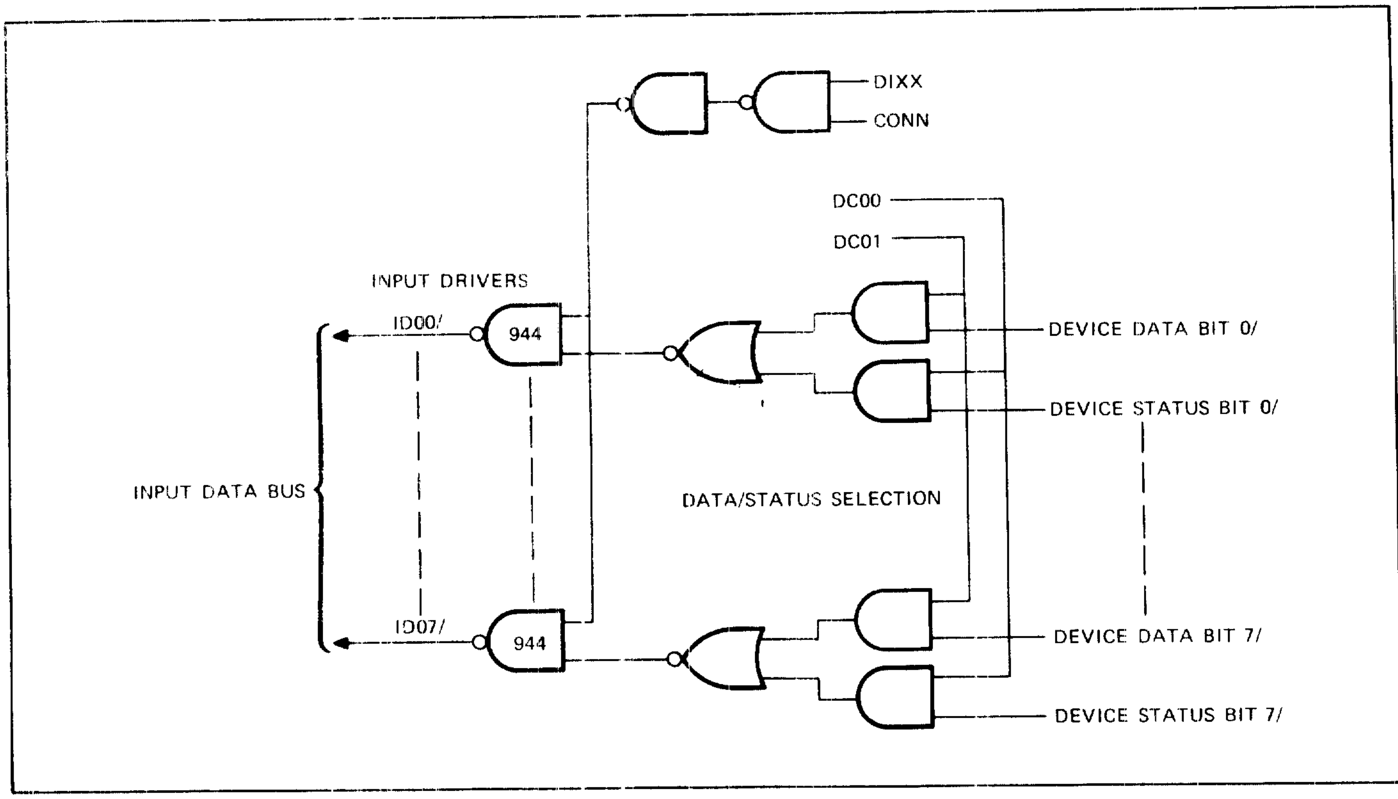


FIGURE 106
STATUS INPUT LOGIC

3.11.3.22 External Interrupt Operation

Interface lines PROT/ PRIN/, EINT/, IAKE/, and ID00/ through ID07/ are used by device controllers or optional Priority Interrupt interface boards on the byte I/O bus for external interrupt operations. Lines PROT/ and PRIN/ make up the hardwired priority chain that determines the relative priority of each controller and Priority Interrupt board on the byte I/O bus. These lines determine priority interrupt I/O operations. Lines EINT/ and IAKE/ carry the interrupt request and acknowledgement, respectively, between the interface units and the processor. Input data lines ID00/ through ID07/ carry an interrupt address byte from the interrupting interface unit to the processor in response to the I/O acknowledgement signal on line IAKE/. The interrupt address byte is used by the processor to locate the entry address in core memory page 1 of the interrupt servicing subroutine.

3.11.3.23 Priority Determination

Interface units on the byte I/O bus are assigned priority for control of external interrupt operations. The priority is achieved in the way that lines PROT/ and PRIN/ are used to link the interface units together. A typical example of priority wiring is shown in figure 107. In this example, three controllers in the mainframe chassis and four controllers in the expansion chassis are connected in the priority chain. The I/O Line Driver and Receiver board serves only to pass priority from the mainframe chassis to the expansion chassis and is not a functional part of the priority chain. As shown in the figure, the priority of an interface unit in the chain is not necessarily the same as the physical order of the unit on the I/O bus.

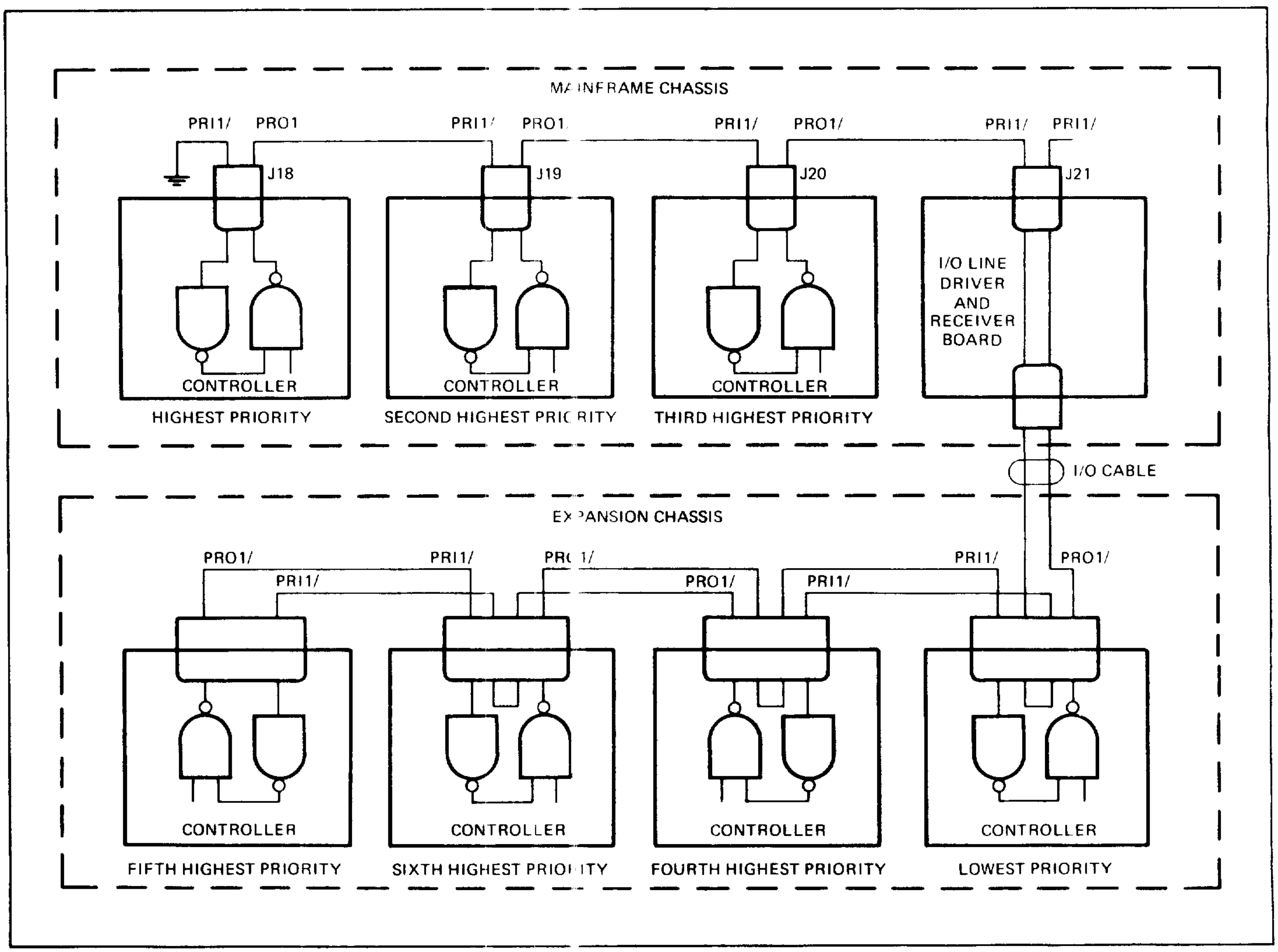


FIGURE 107
TYPICAL PRIORITY WIRING SCHEME

Before a controller can make an interrupt request, it must receive priority from the next higher priority controller on the chain in the form of a ground signal on the priority line. The ground signal indicates that the controller now has no request to make, it places a ground signal on the priority line to the next lower priority controller on the chain. A controller never passes priority along to a lower priority controller while making a request. Failure to follow these guidelines will result in improper operation.

3.11.3.24 Interrupt Requests

External interrupt requests from interface units are carried on line EINT/ to the processor where they appear in bit 7 of file register 0. The internal microprogram recognizes the presence of an external interrupt request by sensing bit 7 and then responds as dictated by interrupt handling firmware.

External interrupt line EINT/ can be used both by device controllers and by optional Priority Interrupt interface boards. The Priority Interrupt option provides the proper interface to the I/O bus, contains priority logic for each interrupt level, and permits processor control over the handling of interrupts. This standard option thus provides, on one circuit board, convenient hardware for eight levels of system interrupts. Because the basic interrupt facility makes use of the byte I/O bus, all device controllers have access to the interrupt request line and can react to the firmware interrupt handling sequences in the processor, provided they operate according to the design guidelines given in the following paragraph.

NOTE

> Requesting an interrupt removes priority from all controllers lower on the priority chain for interrupt operations.

3.11.3.25 Interrupt Sequence and Timing

Figure 108 shows the timing for a typical external interrupt sequence. The firmware, processor, and I/O device operation during the sequence is as follows:

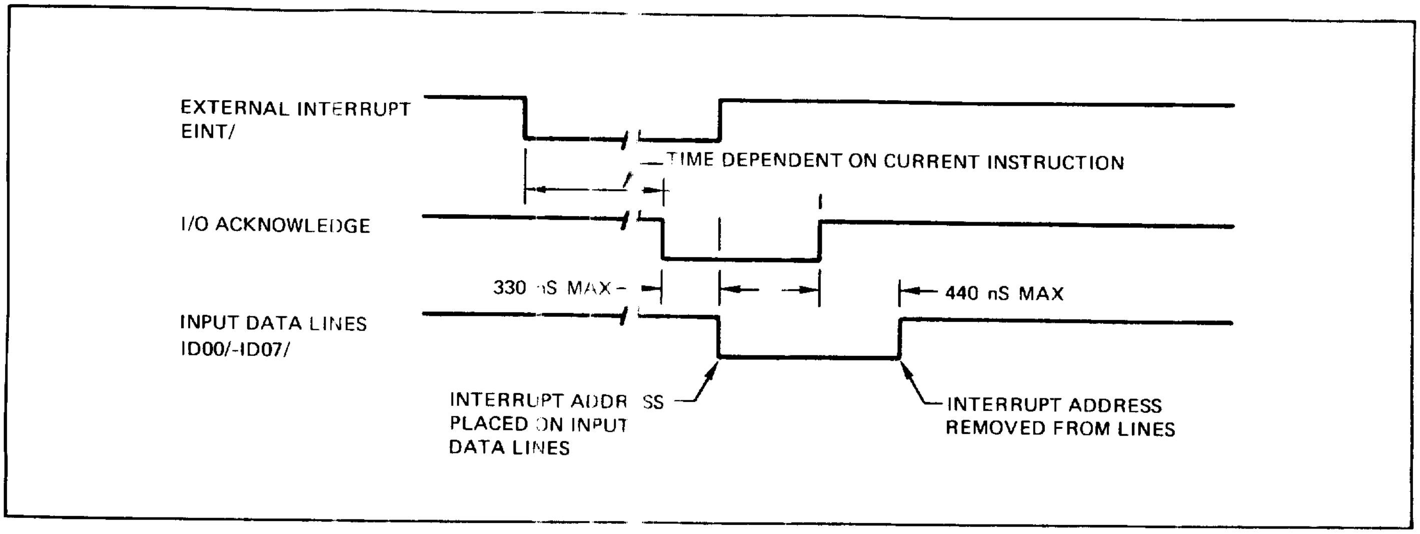


FIGURE 108
EXTERNAL INTERRUPT TIMING

a. The I/O device controller lowers line EINT/ to signal a request for microprogram attention.

b. At the end of the macro instruction currently being executed, the microprogram senses the interrupt request and jumps to a firmware subroutine to handle the request.

c. The mciroprogram lowers line IAKE/ to acknowledge the request.

d. In response to the acknowledgement and select in the device controller places an eight-bit interrupt address on input data lines ID00/ through ID07/. The interrupt address specifies the location in core memory page 1 of the two-byte entry address for the interrupt servicing subroutine.

e. The microprogram accepts the eight-bit interrupt address and raises line IAKE/.

f. The microprogram fetches the two-byte interrupt subroutine entry address from memory using the interrupt address byte supplied by the controller as the lower eight bitw of an address with the upper address bits set to 01 (page 1).

g. Using the two-byte entry address, the microprogram executes a pseudo return jump to the interrupt servicing routine.

h. The interrupt servicing subroutine then proceeds to service the interrupt.

3.11.4 DIRECT MEMORY ACCESS INTERFACE

3.11.4.1 General

The direct memory access (DMA) interface provides the facility for connecting external I/O device controllers to the memory address, data, and control buses through the DMA Selector Channel Interface option. Figure 109 is a simplified block diagram showing the points of interface between the processor, memory, DMA channels, and I/O devices. The remainder of this section describes the interface between the DMA Selector Channel and external devices.

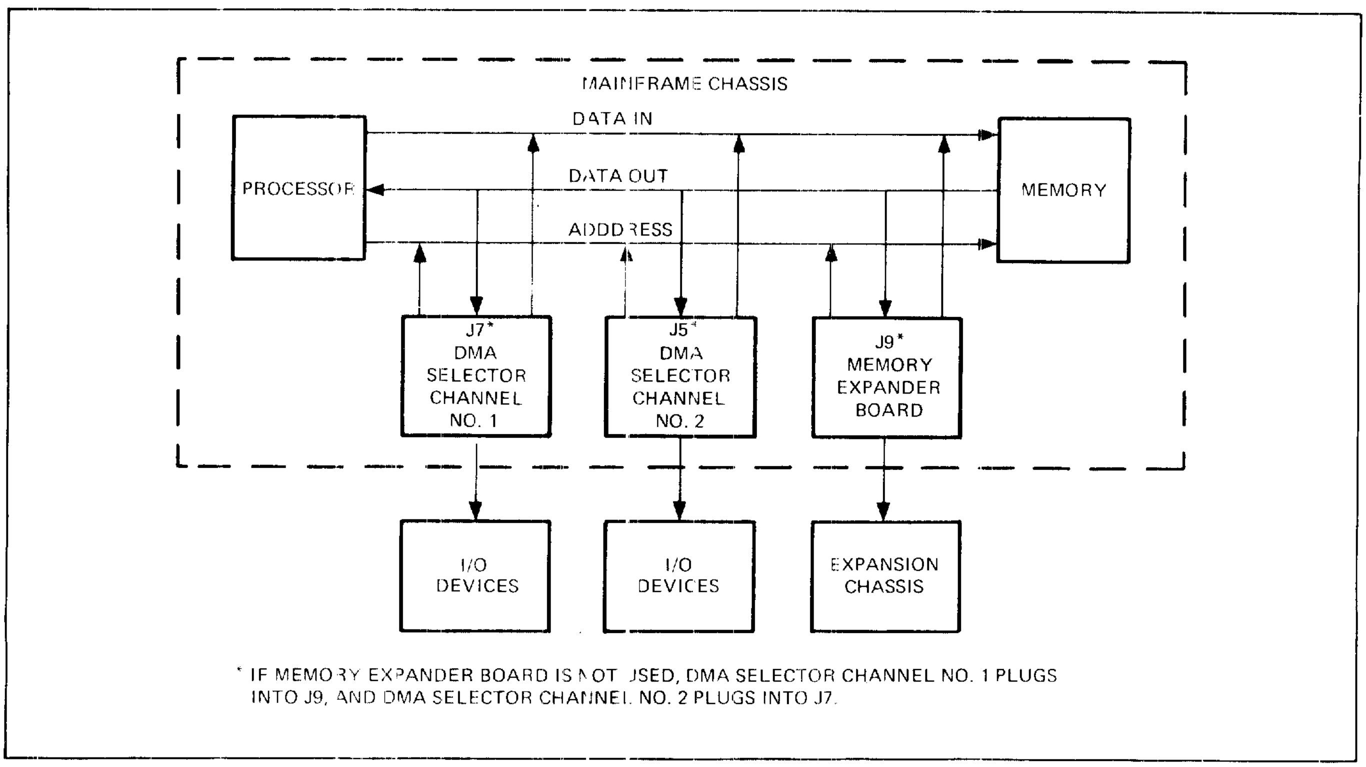


FIGURE 109
RELATIONSHIP OF PROCESSOR, MEMORY, AND DMA CHANNELS

3.11.4.2 DMA Selector Channels

Each DMA channel is physically contained on a single plug-in circuit board, which can be inserted into mainframe connector J9, J7, or J5. Connector J9 is wired to accept either a DMA Selector Channel or a Memory Expander board (used when additional memory is added in an expansion chassis). Connectors J7 and J5 are also wired to accept DMA boards so that two completely independent DMA channels can be added to the computer even though connector J9 is used for memory expansion. However, when connectors J7 and J5 are used for the DMA option, the maximum memory size that can be accommodated in the mainframe chassis is 8K bytes.

As shown in figure 109, DMA Selector Channels can be inserted in mainframe connector J5, J7, or J9, but the Memory Expander board can be inserted only in connector J9.

3.11.4.3 DMA External Interface Lines

The external DMA interface (between the DMA channel and I/O devices) comprises eight data output lines, eight data input lines, six device status lines, and eight control lines. These lines are described in the following paragraphs.

3.11.4.4 Data Output Lines

Data output lines MD00/ through MD07/ connect directly to the memory data bus. They are used for control of the devices connected to the DMA channel as well as for transferring data from memory to the devices. Because these lines reflect the operation of the byte I/O interface lines, they permit the use of output instructions to control DMA channels and the device controllers attached to them. During a direct memory output operation the lines are sampled by the controller when control line DRDY/ goes low.

3.11.4.5 Data Input Lines

Data input lines DD00/ through DD07/ connect to the memory data register in the DMA channel. The data applied to these lines by the controller must be settled when line CREQ/ goes low and must not be removed or changed until line DRDY/ goes low. The DMA channel accepts the data on these lines some time after line EREQ/ goes low.

3.11.4.6 Device Status Lines

Device status lines DST1 through DST6 are connected through the DMA channel to the memory data bus. The six bits of status information applied to these lines by the device controller are transferred to a dedicated memory location. The controller applies appropriate status to these lines all during the time it is connected for service and executing a block transfer operation.

3.11.4.7 Control Lines

The following eight control lines are available at the external DMA interface:

a. COXX/ - control output
b. DOXX/ - data output
c. MRST/ - master reset
d. EREQ/ - controller access request
e. EWRT/ - external write
f. CRDY/ - channel ready
g. DRDY/ - data ready
h. CSTB/ - start of buffer

Control output line COXX/ carries a low signal from the DMA channel to the controller to specify that a device address is on the data output lines. This line is exactly the same as line COXX/ on the byte I/O bus.

Data output line DOXX/ carries a low signal from the DMA channel to the controller to specify that an information byte is on the data output lines as the result of an output byte operation. This line is identical to the DOXX/ line on the byte I/O interface with the following exception:

The data output phase of an output byte operation is subject to alteration if performed during the time either DMA channel is connected and transferring data. For this reason, only function type I/O commands (those that use the COXX phase of the I/O operation) should be sent to device controllers on the DMA channel when the channel is active. This restriction applies only to device controllers connected to the DMA channels.

Master reset line MRST/ carries a low signal from the DMA channel to the controller to clear all control flip-flops to their initialized conditions. This line is identical to control line MRST/ on the byte I/O interface.

Controller access request line EREQ/ carries a low signal from the controller to the DMA channel whenever a direct memory input or output operation is requested by the controller. The line must be held low for a minimum of 250 ns and must be released when line DRDY/ goes low in order to prevent a second memory access immediately after the one requested.

External write line EWRT/ carries a signal from the controller to the DMA channel to indicate the direction of data transfer (input or output). A low signal on the line specifies an input to memory; a high signal specifies an output from memory. The line must be in the required state when line EREQ/ goes low and must remain in that state until line EREQ/ goes high again. As long as this rule is followed, the line can be changed during the transfer of one block of data in order to intermix input and output operations.

Channel ready line CRDY/ carries a low signal from the DMA channel to the controller to indicate that the channel is not in use. The high state of the line indicates that the channel is busy, has been commanded, and is operating in the block mode with some other device. The line stays high during the transfer of multiple blocks of data when a continuous block transfer operation is performed (see paragraphs 3.11.4.11 and 3.11.4.12).

Data ready line DRDY/ carries a low signal from the DMA channel to the controller to indicate that data is present on the data output lines during a memory output operation, or to indicate that the channel has the device data during a memory write operation. The signal is used as a strobe by the controller to capture the data on the data output lines when a memory output operation is being performed. When the signal occurs during a memory input operation, the controller can begin removing or altering data on the data input lines for subsequent accesses. In either case the signal lasts for 440 ns.

Start of buffer line CSTB/ carries a low signal to indicate the start of each new buffer transfer by the DMA channel. This signal is useful for identifying the starting point of a cyclic mode. Line CSTB/ then identifies the start of each block. The line goes micro seconds/low for approximately 4.4 n at the address initialization time of each block.

3.11.4.8 <u>DMA Control</u>

Each DMA channel uses pairs of control words to define the starting and ending addresses for each block of data to be transferred during a direct memory access operation. Each pair of control words identifies a buffer area in memory into which or from which a direct memory transfer operation is performed. One DMA channel can have up to four pairs of control words stored in memory. Normally only one pair is required for a simple (one block) transfer, but the four pairs can be used to link up to four buffer areas for a continuous block transfer.

Each control word occupies two bytes (16 bits) of core memory. Fifteen bits of each word contain address data. The sixteenth bit of each word is used as a link or interrupt flag. The flag bit in the starting address word is set if a block transfer with linked buffers is to be performed. The flag bit in the ending address word is set if an interrupt is to be generated at the end of the block transfer. This interrupt is an internal one that transfers control to a service routine whose address is stored in memory locations 82 and 83 (hexadecimal). The first instruction executed in the interrupt service subroutine must be Input Status, which resets the interrupt signal.

The four paris of control words for each channel are stored in dedicated locations in memory by the software program before the start of a block transfer operation. After being initialized by the software program, the channel automatically fetches its control words from memory. Thereafter, the block transfer operation proceeds automatically under control of the channel and device controller.

Figure 110 shows the dedicated memory locations allocated to the two DMA channels for storing the control words. The figure also shows the positions of the link and interrupt flag bits in the control words.

Each DMA channel is assigned a device address exactly as an I/O device: DMA channel 1 is assigned I/O address hexadecimal 16, and channel 2 is assigned address hexadecimal 17. Microcommands execute the control functions of the output byte instructions in the computer.

3.11.4.9 DMA Channel Operations

3.11.4.9.1 Simple Block Transfer

The timing diagram for a simple block transfer through the DMA channel is shown in Figure 111. Line CRDY/ goes high when a device controller is connected and communicating with the channel. Each time the controller is ready to send or receive a data byte it causes line EREQ/ to go low. The controller holds the line low for a minimum of 250 ns and must return the line to the high state by the time line DRDY/ goes low.

Line DRDY/ goes low when a data byte is present on the data output lines or when the channel has sampled the data byte on the data input lines. As shown in the diagram, data on the output data lines is valid from approximately 100 ns before line DRDY/ goes low until 200 ns after if goes high again. During this period the data is captured by the device controller. When the controller is transferring data to the channel, it must maintain the data input lines in the appropriate state from the time line EREQ/ goes low until line DRDY/ goes low. The termination of CRDY/ indicates that the block transfer operation is complete. All DMA channel devices must be ready to terminate all operations when line CRDY/ goes to the low state.

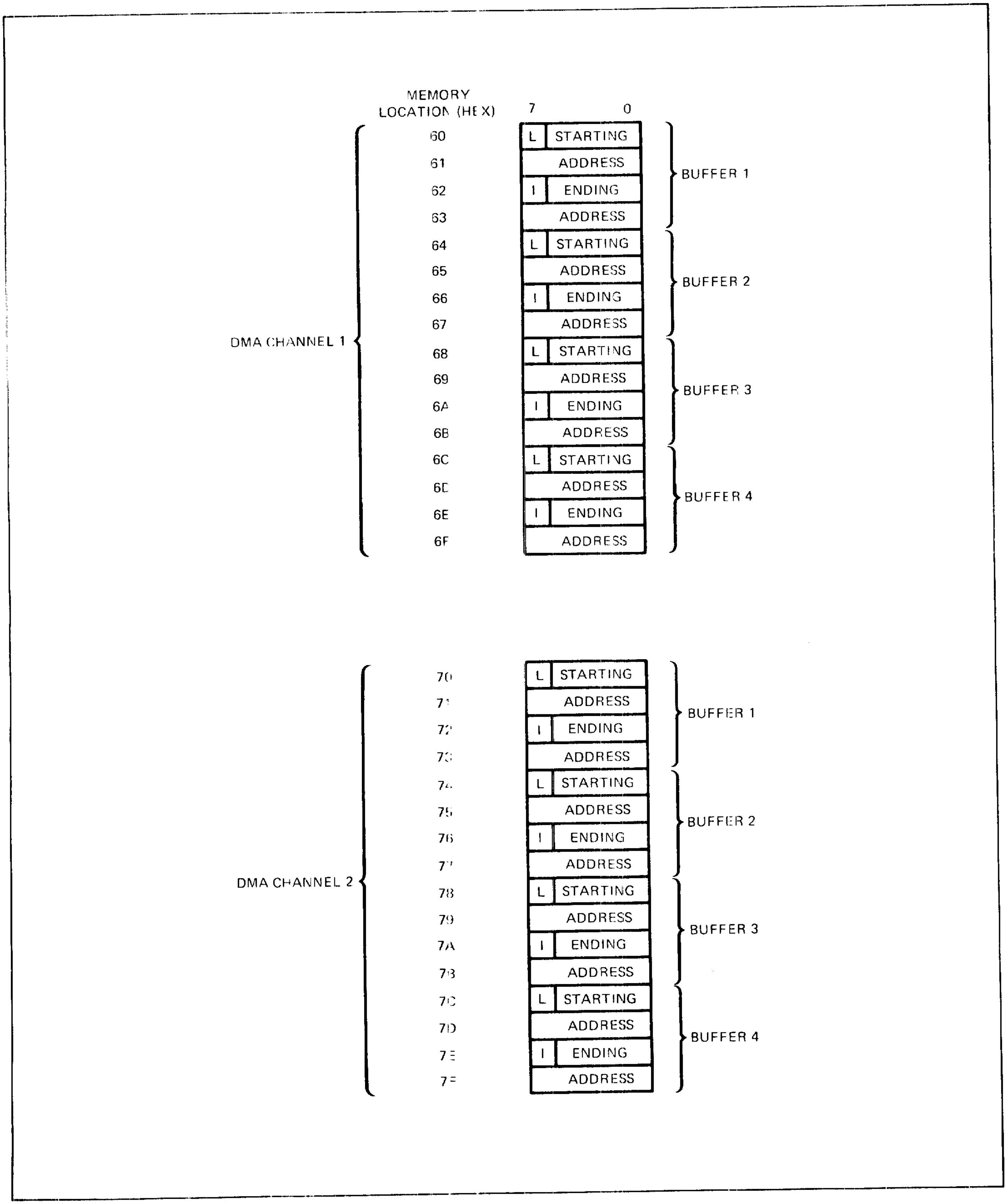


FIGURE 110
DMA CHANNEL CONTROL WORD MEMORY LOCATIONS

3.11.4.9.2 Continuous Block Transfer

The timing diagram shown in figure 111 for a simple block transfer is also valid for a continuous (cyclic) block transfer. The only difference is that line CRDY/ does not return to the low state at the end of a block, since the transfer continuously cycles through the same block. Instead, to terminate the operation, the processor must initiate a disconnect command. Examples of devices that operate in this mode are CRT controllers with continuous output to some recording media, and other analog-to-digital converters.

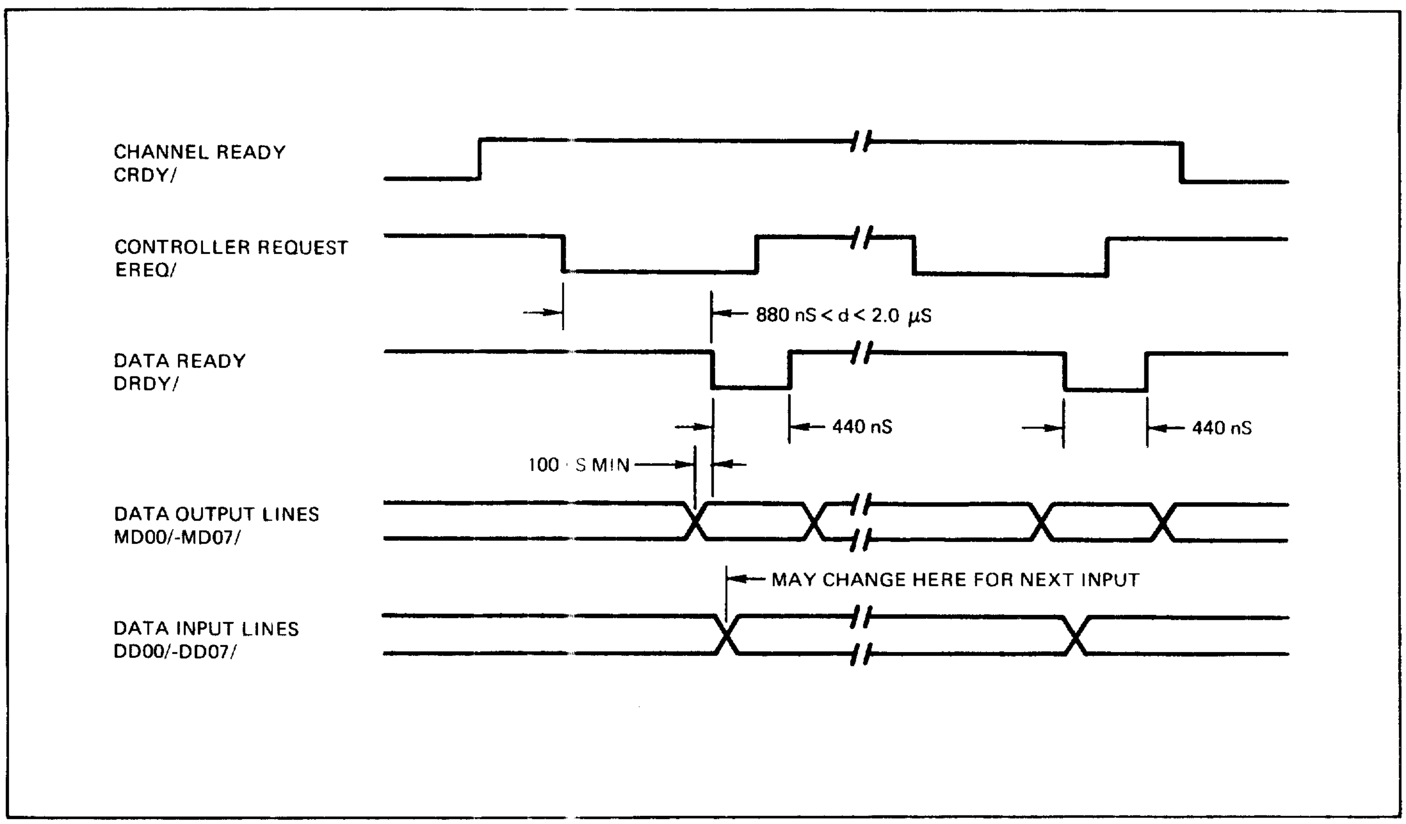


FIGURE 111
DMA CHANNEL BLOCK TRANSFER TIMING

3.11.4.9.3 Block Transfer with Linked Buffers

The timing diagram shown in figure 111 applies also to the linked buffer operation, whether the buffers are being handled on a start-stop basis or cyclically. If they are being cyclically transferred, line CRDY/ continues high indefinitely until the processor disconnects. During start-stop operation, the timing for one buffer transfer is equivalent to that shown in the diagram with the next buffer transfer occurring as directed by the instruction from the processor. The only difference between linked and unlinked operation is that the block control words are fetched from different memory locations when a linked operation is performed.

3.11.4.10 Interface to DMA Channel

The output from the DMA Channel is a multiplexed bus, that is, the drivers can accommodate multiple loads. The input channel is in the form of collector-ORed drivers. All of the input lines described in paragraphs 3.11.4.4 through 3.11.4.7 must be driven from the controller with DTL or TTL power gates (type 944 or equivalent). To maintain channel expandability, the output lines from the DMA channel should be received by DTL or TTL gates with only one load per device.

A single 44-pin connector (P3) on the DMA channel circuit board is used for connecting to I/O device controllers. If multiple device controllers are to share one DMA channel, they must be connected in a daisy-chain fashion as shown in figure 112.

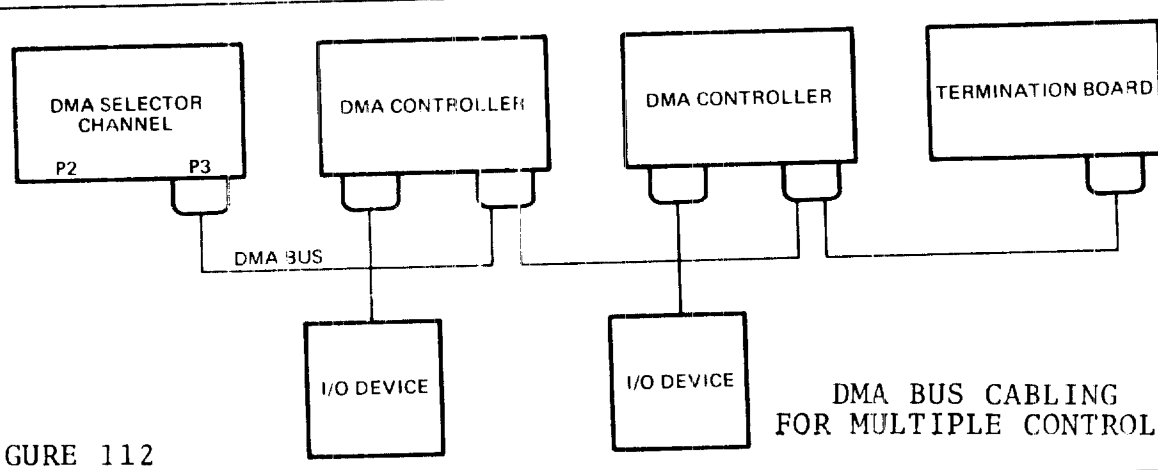


FIGURE 112 DMA BUS CABLING FOR MULTIPLE CONTROLLERS

DATA BOARD #2 (J12)

1000273

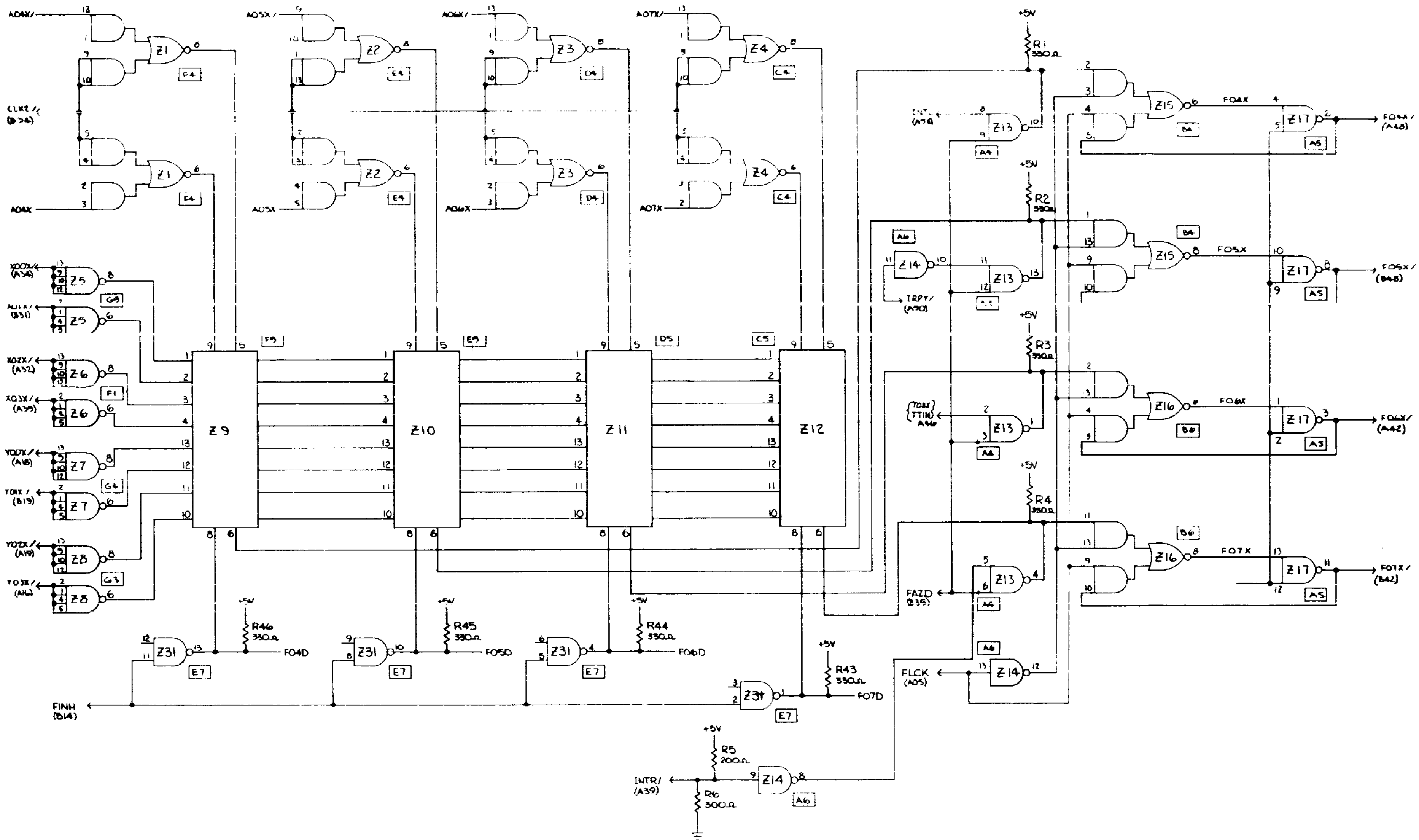


FIGURE 64

FILE LOGIC

(Bits 4-7)

SECTION 4

INSTALLATION AND MAINTENANCE

4.0 INTRODUCTION

This chapter presents the installation and maintenance procedure for operation of the computer from unpackaging through checkout and repackaging for shipment.

4.1 PACKAGING CONFIGURATION

The computer is shipped in two containers: One contains the computer chassis, and power distribution cables, core memory and all processor, control and option boards, but excluding power supply and power cord.

Optional printed circuit boards (if specified).

Documentation

The other contains the power supply with power cord.

Both containers consist of a 350 pound test single wall, corrugated box conforming to Federal Specification PPP-B-636, Class I. Both are sealed with reinforced tape conforming to Federal Specification UU-T-106 and banded. Two pound density Ester Polyurethane foam conforming to Federal Specification MIL-C-46842 is used to preclude movement of printed circuit boards.

The computer is shipped in a foam container fabricated from a polyurethane foam conforming to MIL-P-26514A. The foam holder is fabricated in three sections. Top and bottom section, P/N RM5-1917, center section, P/N RI17524, Reference Figure 1.

The foam container is banded in two places using nylon web straps (Reference Figure 113).

In Addition, the power supply is mounted on a sandwich type pallet cushioned with two pound density Ester Polyurethane, 2 1/8 inches thick, per Federal Specification MIL-P-26514. Securing of power supply to the sandwich is accomplished by utilizing wood clamps with hanger bolts and wing nuts. A sleeve of 350 pound test double wall, corrugated conforming to Federal Specification PPP-B-636, Type I, Class I, is placed top to bottom, side to side, and end to end to hold the pallet in a fixed permanent condition.

If a teletype is ordered with the computer, it will be packaged in a container supplied by the teletype vendor.

4.2 UNPACKING INSTRUCTIONS

Following is the procedure for unpacking the computer:

1: Be sure carton is in upright position as indicated by arrow labels on outside of carton.

2: Insert diagonal cutters under wire band and cut banding.

3: Remove wire from around carton.

4. Using a pair of carton cutters, cut reinforced tape around carton.

5. Open flaps of carton and remove the foam container.

NOTE

For precautionary measures it is advisable that the following steps are performed by two people.

6. Remove nylon web straps from foam container and remove top section and the insert (s). Remove computer from bottom section.

NOTE

DO NOT DESTROY FOAM CONTAINER OR CORRUGATED BOX. (USE FOR RETURN OF COMPUTERS FOR WARRANTY REPAIRS OR SHIPMENT OF COMPUTERS TO REMOTE LOCATIONS).

7. Cut polyurethane bag with scissors or knife.

8. Slide computer out of polyurethane bag.

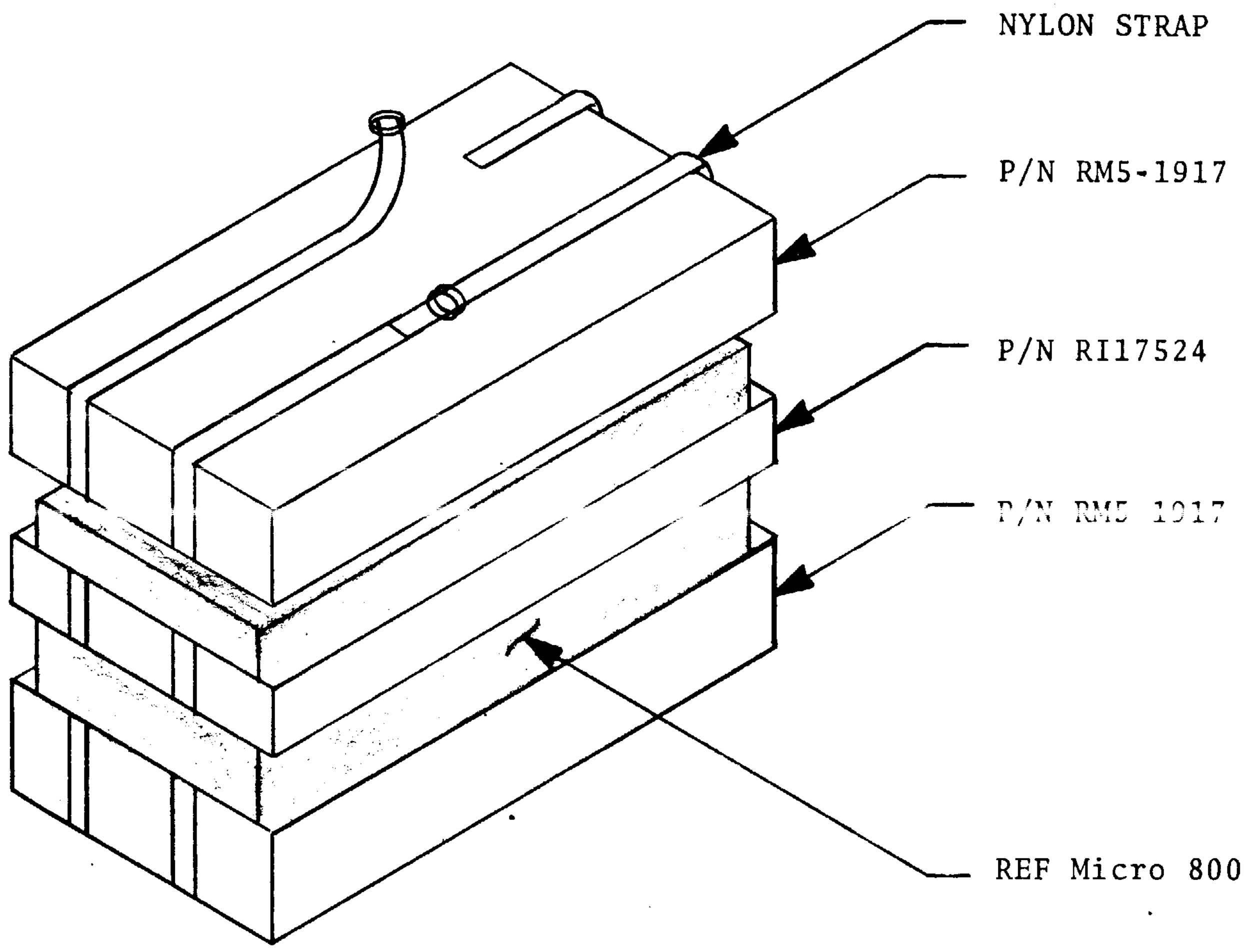


FIGURE 113

9. Remove wooden back from computer then remove foam shipping blocks from inside computer.

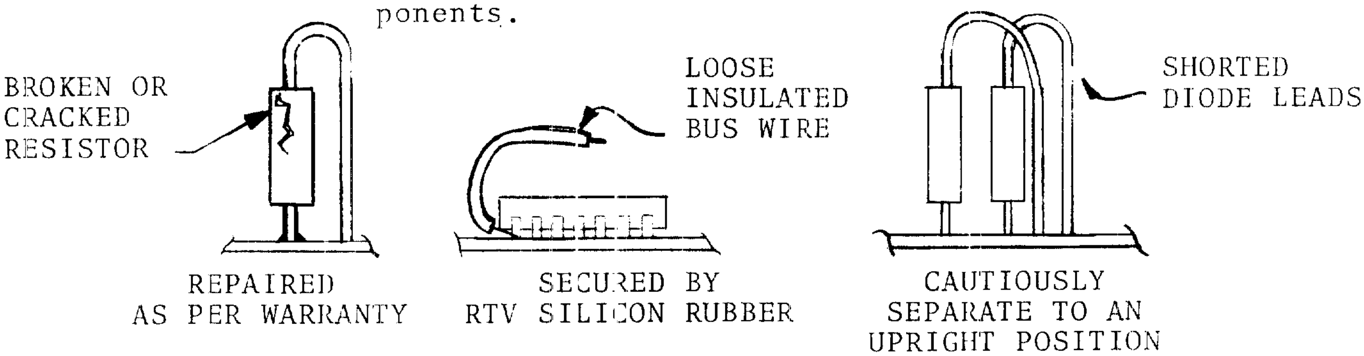
Following is the procedure for unpacking the power supply:

1. Refer to steps 1 through 4 listed above.
2. Remove sleeve of corrugated 350 pound test double wall from around power supply.
3. Remove wing nuts from hanger bolts.
4. Remove wood clamps and lift out power supply.

SEE NOTE ON PREVIOUS PAGE

4.3 SYSTEM INSPECTION

1. With board puller P/N 9002, move printed circuit boards (PCB) from the jacks. Exercise extreme care when handling PCB's. Component lead feed-through occasionally leaves rough/sharp edges on bottom side of board. Rough handling may result in skin abrasions or minor scratches.
2. Record type board, part number, and serial number as applicable.
3. Inspect PCB's for broken, loose, or shorted components.



4. Notice that each PCB has contacts on both ends.
5. The correct position of the board for proper insertion is shown below.

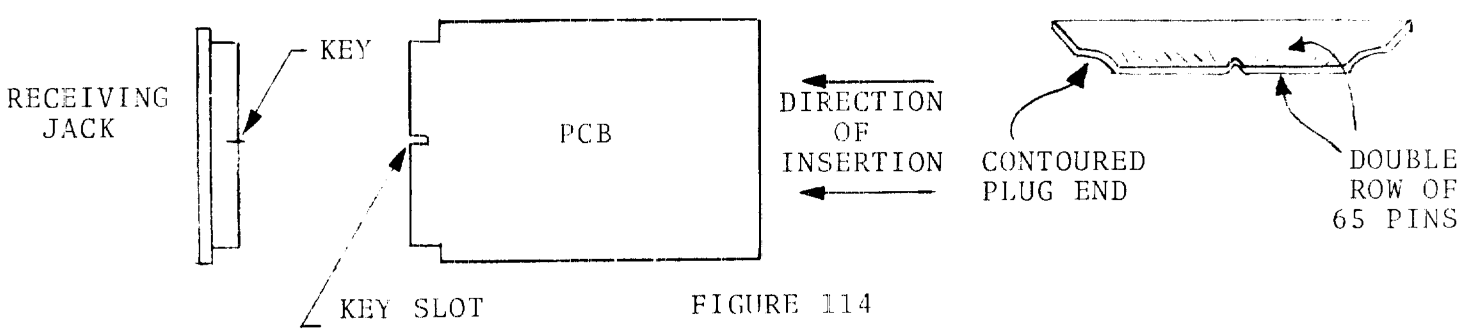


FIGURE 114

6. Exercise caution when handling the PCB during re-placment.

7. Figure 115 shows the proper location of PCB's within the chassis. Use this drawing as a guide for proper location of the boards during re-placment.

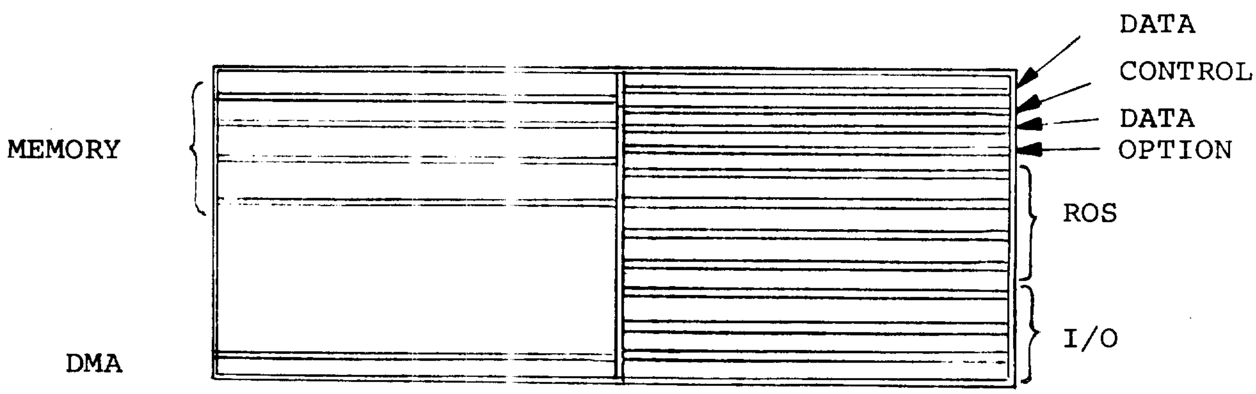


FIGURE 115

(END VIEW)

8. There are three (3) sets of guides that support and align each board with its respective jack. See Figure 116.

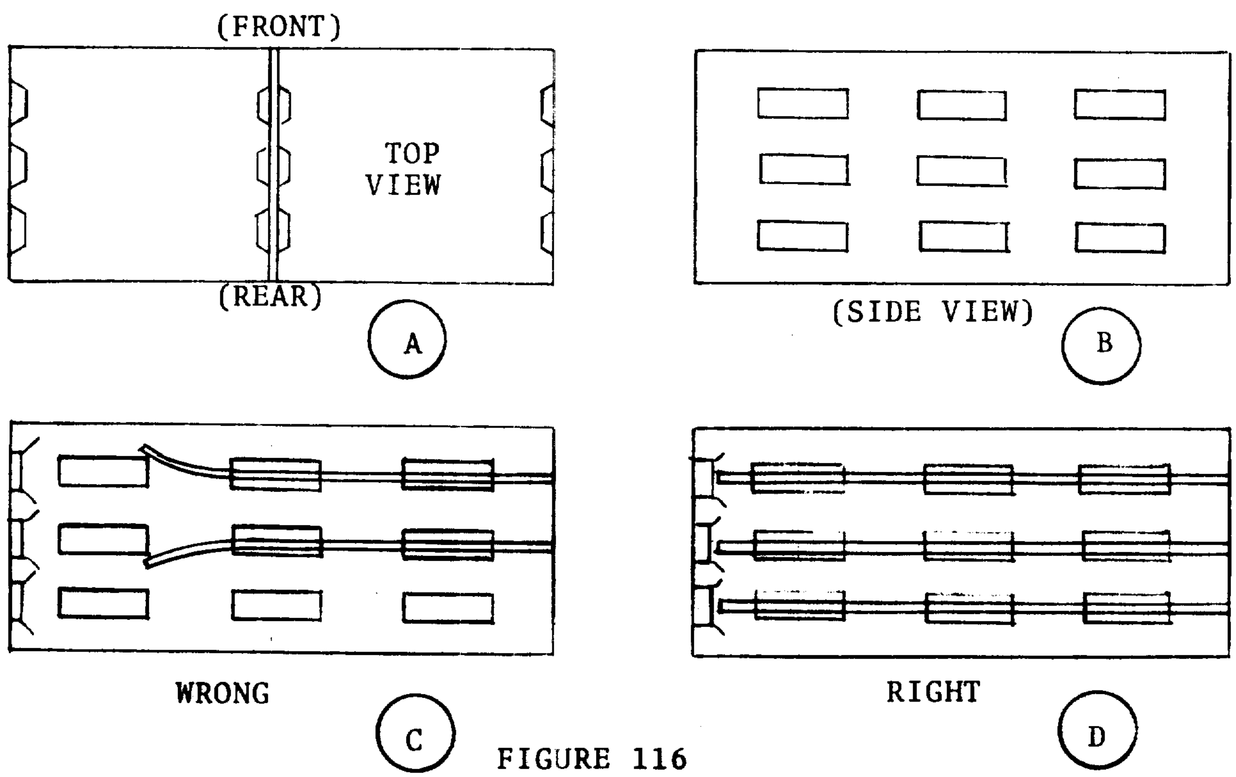


FIGURE 116

NOTE

It may be applicable to record by part number and serial number the location of each board.

9. Identify a data board P/N 1000193 (1000774). Insert this PCB in J10. Insure proper alignment with the guides.

10. Because of the necessity of good electrical connection, the PCB's will exercise an initial resistance upon full insertion into the jack.

11. To fully insert the board into the jack it may be necessary to push the board up and forward from the underneath. This will position the PCB at jack opening. See Figure 117.

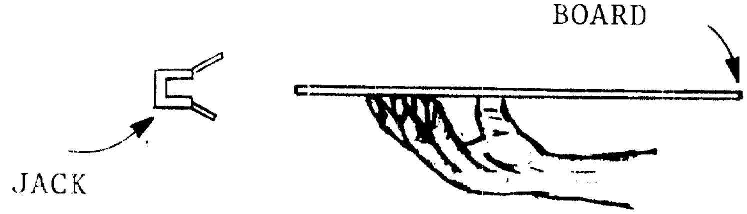


FIGURE 117

12. While securing the CPU from the front with your left hand, push the board fully into the jack. See Figure 118.

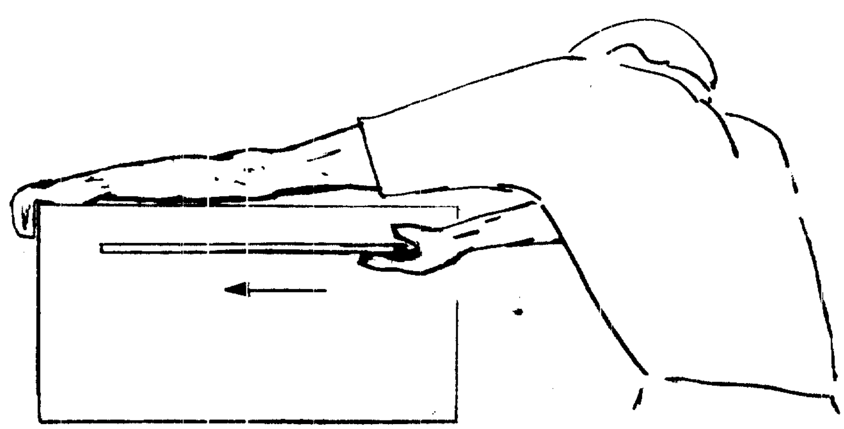


FIGURE 118

13. Another method may be used in conjunction to that above by gently pushing down or lifting up on the end of the board while pushing forward (board aligned correctly) and feeling the board "seat" in the jack. See Figure 119.

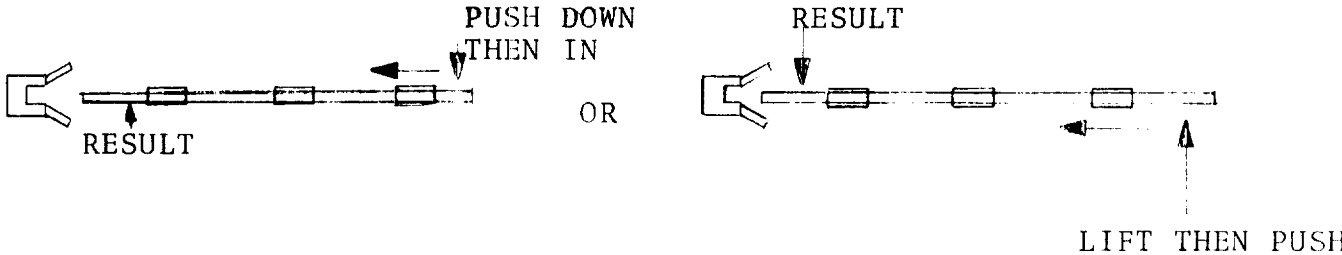


FIGURE 119

14. When the board has "seated" properly, you will usually hear a dull snap which will indicate that the board has bottomed out (seated) in the jack.

15. Insert the control board next, P/N 1000197 or 1000775 in J11.

16. Insert the second data board P/N 1000193 or 1000774 in J12.

NOTE

The two (2) data boards are interchangeable, but do <u>not</u> exchange the control board with a data, PCB electronic component damage may result.

17. Insert the processor option board as applicable in J13.

18. The read only storage (ROS) boards, those with groups of diodes have a significant installation sequence which must be adhered to or your CPU will not function properly.

19. The following chart is a guide to follow for correct ROS PCB installation

(Interchangeable within jack locations only)

J14 ROS #1	1000275	1000279	1000590
J15 ROS #2	1000276	1000280	1000591
J16 ROS #3	1000277	1000281	1000592

FIGURE 120

CAUTION

Exercise care when installing ROS PCB's. Improper handling may cause the shorting of diode leads which will result in CPU malfunction.

20. Install each ROS PCB as per Figure 120.

   a. If you have only three (3) ROS PCB's, insure that you skip jack location J17 before inserting the first I/O board.

   b. Insert the first I/O board in J18 (as applicable).

c. Insert remaining I/O boards in J19 through J21, (as applicable).

d. The magnetic core memory unit is a two (2) board module.

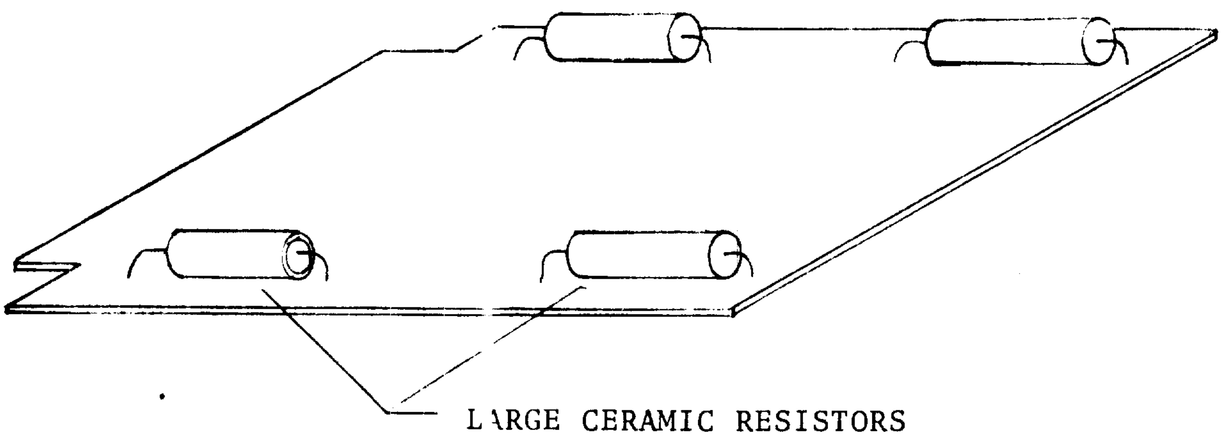


FIGURE 121

e. The side with the large ceramic resistors (mounted) in black colored heat sinks) is the top side of the memory module. This side contains the sense/inhibit circuitry.

f. The bottom side of the board is sink and drive cir- circuitry. Current loop wire (white insulated wire) should be secured to the board by RTU silicon com- pound. This is to prevent obstruction when inserting the next memory module.

g. With sense/inhibit side (large ceramic resistors) up, insert the memory module in the double sets of board guides.

h. Fully seat the memory module.

i. Insert remaining memory modules (as applicable).

j. Insert direct memory access PCB (as applicable).

k. Inspect power supply for loose hardware, loose or broken components.

l. Remove a CPU power cable/harness from plastic bag as applicable.

m. Place power supply on top of CPU (to the rear) or on table top near the CPU as applicable.

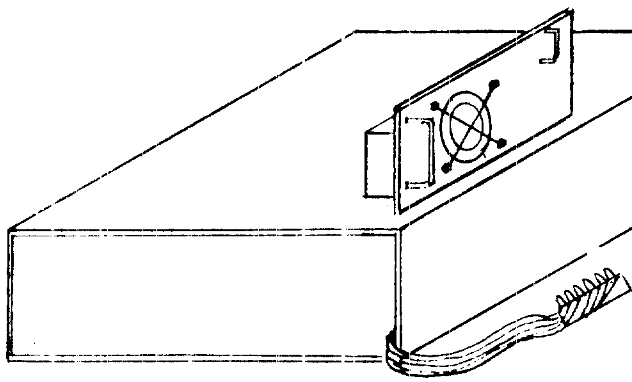


FIGURE 122

NOTE

220VAC POWER SUPPLY OPERATION

The computers are shipped wired for 115VAC power, 50 or 60 cycles. If operation at 230VAC is required, the following changes should be made to the power supply:

1. Observe that on the main transformer on the power supply are four screw-type terminals labeled "A" "B", "C", and "D".

2. Disconnect the ring-tongued terminal from "D" and connect it to "C".

The system is now operational for 230VAC power.

CAUTION

Do Not connect power cord to power source outlet at this time.

n. Remove power supply terminal strip cover (2 hex head nuts).

o. Set power supply toggle switch to OFF position.

p. With VOM or other suitable voltage measuring device measure the power supply output voltages.

q. Connect power supply cord twist lock connector to the power supply.

r. Connect power supply cord to 115-120 VAC 60 ohm power convenience outlet.

s. Set power supply switch to power ON.

t. Push power switch on front panel down (ON).

u. Measure the following voltages:

   1. +12V ±

   2. + 5V ±

   3. COM

   4. COM

   5. -1.5V ±

   6. -6V ±

   7. -V - -16.5V

   8. DET - +15V in normal operation - ground during power fail detect)

   9. REM - 115VAC

   10. PWR - 115VAC

v. Set power supply switch to power OFF.

w. Remove 115-120VAC power from the power supply by disconnecting the twist lock connector or power supply cord plug from 115-120VAC source.

   1. On the power supply terminal strip loose the ten (10) pan head screws to allow enough clearance for inserting the CPU power cable/harness.

   2. Install the CPU power cable/harness on the terminal strip.

   3. Tighten the terminal strip screws to secure the power harness.

   4. Insure that the front panel power switch is in the upper most position (should be released from its holding alternate action position).

5. Bring out the teletype cable (as applicable).
6. If you wish to install the power supply in chassis, carefully lift the power supply and turn at a right angle to the rear of the CPU, then lower the power supply and insert into the rear of the CPU.
7. Secure the power supply to the chassis with five (5) screws (as applicable).
8. Do not obscure the vent slots on each side of the CPU or the fan exhaust in the rear. An obstruction will result in the restriction of air flow and may cause the CPU to over heat. This will cause machine malfunction if not corrected.
9. Reconnect power 115-120VAC to the system.
10. Set the power supply switch to the ON position.

4.4 SYSTEM TURN-ON

NOTE

You are now ready to apply power to the CPU.

1. Set the SAVE switch ON.
2. Set the POWER switch ON.
3. The HALT lamp should be illuminated. If the HALT lamp does not illuminate to the next step.

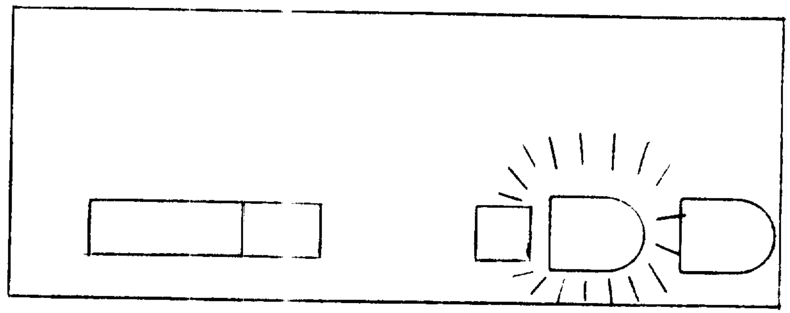


FIGURE 123

NOTE

Always remove power before removing or installing any PCB.

4. If the HALT lamp did not come on, perform the following as necessary:
   a. With power on, check +5VDC, +12VDC. If you do not have +5V, +12VDC go to (b).
   b. Depress power switch to OFF.
   c. With a ohmeter check fuses F1 and F2. Replace if found to be defective. Go to step 2.
   d. Proceed to step 1 of 4.6
   e. If power supply continues to blow fuses, check the following:
      i. Insure that the PCB on the power supply is properly seated.
      ii. With ohmeter, the voltage terminals to chassis ground should be open circuited. If you have an ADC power supply P/N 1000134, insure that the large heat sinks have not become loose and shorted to ground through its support. (At four (4) places).

f. If problem still exists replace power supply as per warranty.

g. Set power to OFF.

h. Remove HALT lamp lens by pulling out. Remove lamp, check with ohmeter. If open circuit, replace with a new ESB-12 lamp.

i. Replace lamp and indicator.

j. Return to step 4.5,1.

k. Set power to OFF.

l. Reset both Data Board #1 in J10 and control board in J11.

m. Return to step 1 of 4.5.

n. Set power to OFF.

o. Interchange Data Board #1 in J10 with Data Board #2 in J12.

p. Return to Step 1 of 4.5. If the HALT goes on, the data board in J12 is defective and must be replaced as per warranty.

q. Continue with the next step.

4.5 POWER DOWN PROCEDURE

If the CPU is on the "RUN" or "HALT" lamp will be illuminated. Depress switches in the following sequence to properly turn off power:

1. CLOCK (momentary) then,
2. RESET (momentary) then,
3. SAVE (alternate action) then,
4. POWER OFF (alternate action).

At this time the illuminated lamps will go out and the sound of the power supply fan will diminish.

4.6 TELETYPE INSTALLATION

If an ASR 33 type "TY" Teletype is purchased with the computer, the only requirement for use with the computer is to insert the computer cable connector into plug S2 (located at left rear of teletype).

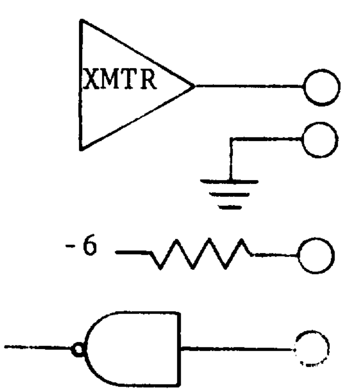
However, if an ASR 33 Teletype is not purchased with the computer the following procedure may be required to make the teletype compatible with it:

1. Remove cover of teletype.
2. Note terminal strip 151411 located at lower left of teletype viewed at rear of machine. Teletype Corporation wiring diagrams 6353 WD Sheet 1 are helpful, but not mandatory for the following changes.
3. Move purple wire from terminal 8 to terminal 9.
4. On terminal strip 151411, move white/blue wire from terminal 4 to terminal 5.
5. Move brown/yellow wire from terminal 3 to terminal 5.
6. Observe Power Resistor 181816 located at center of right side of teletype (viewing from the front with cover removed). When cover is in place, the resistor can be seen centered under the removable plate on the right side.
7. Move blue wire from terminal 3 to terminal 4 of the power resistor.

Connection to an ASR 35 Teletype

To modify an ASR 35 Type "TY" Teletype for use with the computer, perform the following procedure:

1. Remove the top cover from the teletype.
2. Observe the power terminal block (151415), denoted in wiring diagram by T, which is located at the right lower rear (viewing from the front) of the cabinet behind the teletype printing mechanism.
3. Remove strap between T6 and T7.
4. The existing cable from the computer must also be modified to connect to a Teletype ASR 35.
   a. Cut off the connector.
   b. Connect the four wires to the "T" terminal block in the Teletype as follows:



Old Connector Pin Number		Wire Color	Terminal Block Pin #
TTYX 8	Send Loop	White	7
GRD 7	to teletype	Black	8
TTIR 5	Receive Loop	Brown	6
TTIN 6	from teletype	Red	6

FIGURE 124

4.7 LOADING A PROGRAM TAPE

A Program Tape is loaded into memory via the basic paper tape loader. This basic loader is in the bootstrap format (1 data byte per frame of tape) and is spliced onto the front of the program tape The splice is made so that the last frame of the loader is followed immediately with the leader of the program tape. The microprogrammed bootstrap loader loads the basic loader and transfers control to it. Then the basic loader loads the program tape and, after a successful load, transfers control to the address contained in the end-of-tape record. Following is a procedure for loading a programmed paper tape through the teletype via the bootstrap and basic loaders:

Place the TTY in the off-line mode, place the reader control lever to the "free" position and enable the teletype reader. Type control and O.

Place the TTY in the on-line mode and insert the program tape in the reader with the first rub-out character at the read station. Set the reader control lever in the stop (center) position.

Set the front panel sense switches as follows:

Sense Switch 1: Off for serial TTY interface.
On for parallel TTY interface.

Sense Switch 2: Must be Off

Sense Switch 3: must be Off

Sense Switch 4: must be On. This selects the bootstrap loader whenever the run switch is selected and was preceded by a reset.

Press the TTY reader lever to the start position.

When the basic loader is loaded and operating properly, the teletype page printer mechanism will chatter whenever a record separator passes the read station. This is caused by the issuance of reader off and a reader on code between records.

If a checksum error is found, the message 'CE' is typed and the system will halt. Another attempt to properly load the record may be accomplished by backing up the tape to the previous record separator, (indicated by 3 successive rub-outs), placing the reader control lever in the stop (center) position, and pressing the run switch on the front console. When the tape is properly loaded, the reader will be stopped, and control will transfer to the loaded program. If another input device (card reader, high-speed paper tape, etc.) is available on the system, it may be used to load the program. The basic loader for that device is supplied as a separate paper tape and is read through the teletype reader by the previously described procedure. Following the loading of this short tape, the program will be automatically loaded via the other device.

4.8 TOS OPERATION

If TOS is in the machine, the R operator causes TOS to load a program tape. This operation can be configured for any standard input device, but normally the device will be the teletype paper tape reader. The tape must be inserted in the reader with the leader (any frame with the channel 8 present) placed at the read station before the R is typed. When the loader encounters a record with a zero byte count the loading process is terminated and control is transferred to TOS or to the transfer address. If there is no zero byte count record, loading will continue until the computer is halted or until the console interrupt is activated. A checksum is calculated for each record loaded and if it doesn't equal the checksum read with the record, the letters 'CE' will be typed and control will return to TOS. By backing up the tape to the previous separator and typing an R, another attempt may be made to load the tape.

4.9 DIAGNOSTIC TEST PROGRAMS

The system is now ready for use as a computer, to further ascertain the system operation proceed to run the following diagnostic test programs.

1. GIT - General Instruction Test
2. MDT - Memory Diagnostic Test
3. POT - Processor Option Test (if option board is used).

For description of tests and instructions or diagnostics operational procedure, consult the instruction manual P/N 70-1-0810-007, Memory Diagnostic Test, Processor Option Test and General Instruction Test.

4.10 PREVENTIVE MAINTENANCE

The computer does not require a rigid schedule of preventive maintenance routines. However, to insure the operational accuracy of the computer, it is recommended that the Diagnostic Tests cnn be conducted either on a daily basis or whenever other system maintenance is performed and that the +5 volt power supply be checked and verified for operation within 5 percent of its nominal value. When checking the power supply voltage level, turn on all input/output equipment and measure the voltage with a digital voltmeter having a full scale accuracy of 3 percent. Measure the voltage at the Control Board after the card extender has been inserted between the Control Board and the Backplane.

CAUTION

Do not remove the Control Board or insert the Control Board with the power on.

Measure the +5V supply on the Control Board with the power on.

Measure the +5V supply on the Control Board across the capacitor located between the components at coordinates A1 and B1. The voltage should measure 4.75V (min.) to 5.25V (max).

4.10.1 Power Supply Adjustment

If additional loads are added to the Power Supply, readjustment of the +5 voltage may be necessary. The procedure would be to monitor the voltage, either at the backplane or at the connector. Vary Trimpot R located on the regulator board to +5V +5 percent.

If the +5 volt supply is out of tolerance, then the appropriate power supply potentiometer is to be adjusted to set the correct voltage level. The potentiometer to be adjusted is located on the printed circuit board within the power supply.

If the power supply is the type as depicted in Figure 1C, then the potentiometer to be adjusted is the center one on the horizontally mounted circuit board.

If the power supply is the type as depicted in Figure 1E, then the potentiometer to be adjusted is the lower one on the vertically mounted circuit board.

4.10.2 Corrective Maintenance

Circuit Board Replacement. When troubles with the processor have been isolated to a circuit board level and it is necessary to replace that sub-assembly, the following procedure should be implemented:

1. Shut off the computer power and remove the power input connector to the computer.

2. Remove the five power supply panel mounting screws and remove the power supply from the computer.

   Be careful not to pinch or shear the rainbow wiring strip.

3. At this point, all the circuit boards are accessible. Firmly grasp the circuit board to be removed and pull outward. Grasp the assembly with both hands or a card extractor.

   CAUTION

   Do not use long nose pliers in place of a card extractor.

   Be careful not to damage components on the assembly by inadvertently banging them against other boards or structure within the body of the computer.

4. Insert the replacement card and insure that it is properly seated in the backplane connector. Sometimes it may be necessary to take the sag out of the circuit boards when inserting them. To accomplish this support the center of the board with one hand, keeping the board straight and use the other hand to apply sufficient force to seat the board in its mating connector.

5. Replace the power supply into position again being careful not to damage the rainbow wiring strip and secure the power supply to the chassis by replacing the five screws previously removed.

6. Replace the power connector and resume operation.

It is recommended that a diagnostic check and power supply voltage check be performed at this point.

Power Supply Replacement. The power supply is replaced by following the procedure outlined below:

1. Shut off the computer power and remove the power input connector to the computer.

2. Remove the five power supply panel mounting screws.

3. Loosen the 10 spade lugs on the rainbow wiring strip from terminal board TB1.

4. Withdraw the power supply.

   Be careful not to damage any wiring during this operation.

5. Insert the new power supply, being careful not to damage any wiring.

6. Fasten the 10 spade lugs to the appropriate terminals on TB1.

7. Secure the power supply panel with the five mounting screws.

8. Replace the power cord and resume operation.

Front Panel Replacement. Components located on the front panel may sometimes require replacement due to either burn-out or damage. This paragraph suggests procedures for maintaining the front panel.

Lamp Replacement

1. Remove plastic protective cap covering lamp to be replaced. The cap is a snap-on device and is removed by applying finger pressure across opposite sides and pulling outward.

2. Remove the lamp, to be replaced, from its bayonet socket.

3. Insert the new lamp.

4. Replace plastic protective cap.

Switch Replacement

1. Insure that power is disconnected from the computer.
2. Remove face plate by removing the four 6-32 X 1/2 Phillips screws at the corners of the face plate.
3. The front panel mounting plate is now exposed.
4. Remove the top center screw from the front panel mounting plate.
5. Do not remove the two lower screws. These screws are used to mount a connector located behind the front panel mounting plate.
6. Withdraw the front panel mounting plate from the chassis. It is being held by two connectors.

   Be careful not to damage the connectors by rocking the front panel from side to side or top to bottom when withdrawing the front panel.
7. Carefully tag the wiring and its location on the defective switch assembly.
8. Remove the wiring from the switch assembly.
9. Remove the mounting nuts which secure the switch assembly and remove the defective assembly.
10. Install the replacement switch assembly and carefully tighten the mounting nuts. Be sure the nuts do not damage the switch assembly mounting tabs due to overtightening them.
11. Install the wiring on the new switch.
12. Replace the front panel mounting place and insure that the connectors are properly mated.
13. Install the top outer mounting screw previously removed.
14. Replace the face plate and the four mounting screws.
15. Connect power and resume operation.

4.11 PACKAGING AND PACKING FOR SHIPMENT

There are times when the computer must be packaged for shipment, either to a remote location, or back to the computer manufacturer. In case of a need to ship the computer the following procedure should be followed using the packaging material the computer was delivered in if possible.

If the original packing case and material was destroyed or lost, the computer must be packed with extreme care adhereing to the following procedure as closely as possible with the available packing material.

Packing Method

The assembly when completed, and accepted for shipping, shall be placed in a pre-cut and shaped foam holder that is nested in a fiberboard box meeting the requirements of PPP-B-636, 350 pound test style, or to an equivalent industry standard.

The foam holder shall be fabricated from a polyether polyuerthane foam conforming to MIL-P-26514A.
The foam holder is fabricated in three sections. Top and bottom section, P/N RM5-1917. Center section, P/N RI17524. Reference Figure 125. The foam container shall be banded, using Nylon Web strap, in two directions (ref. Figure 125).

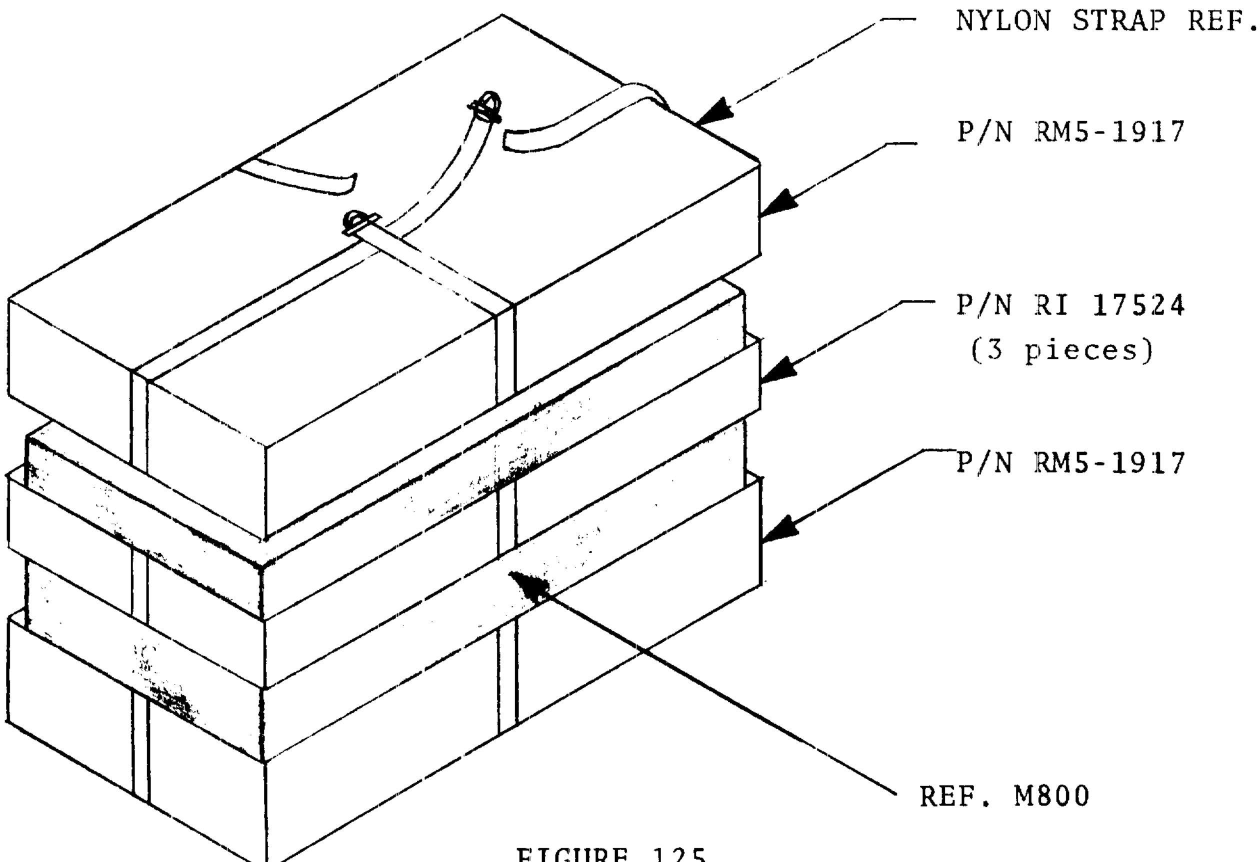


FIGURE 125

4.11.2 <u>Shipping Method</u>

The fiberboard container nesting the foam holder, shall be used as the shipping container.

The container may be fabricated, either as a rigid fully assembled box, or as a folded die cut box with flaps.

Sealing - The fiberboard container shall be sealed, using a three inch wide paper tape (gummed craft or equivalent) on the closure flap and the open ends.

4.11.3 <u>Marking of shipping container</u>

The shipping container shall be marked as shown in Figure 126. Marking labels shall be applied or marking may be hand lettered using marking pens. The marking shall be legible and readable from a distance of two feet.

4.11.4 <u>Power Supply Preparation</u>

Install Power Supply on foam package mounting block reference 127.

Place foam holder and power supply in fiber board container.

Place fiber board packing in place. Power cord and other accessories in proper package locations.

Seal fiber board container using three inch wide paper tape, on closure flap and open ends.

Preparation for delivery.

Mark shipping container as directed in 4.11.3, this specification.

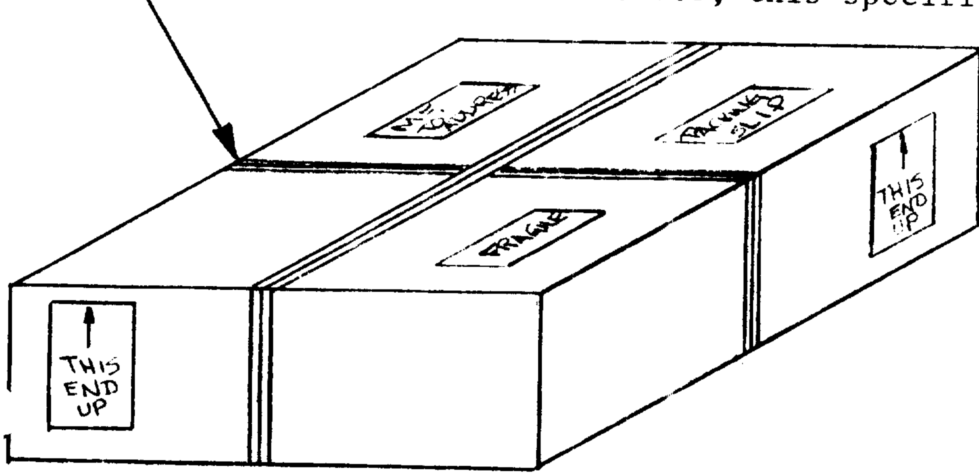


FIGURE 126

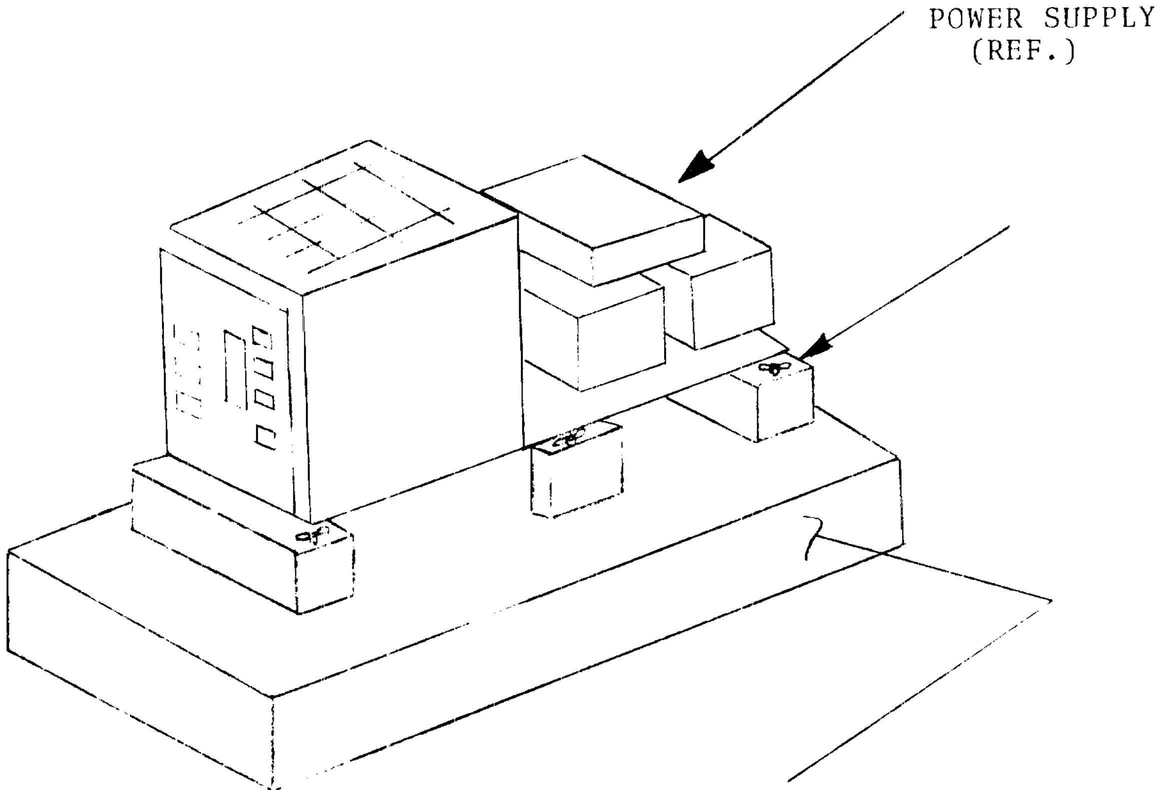


FIGURE 127

4.12 FIELD MAINTENANCE

Field maintenance is concerned with assuring that the computer system is performing properly, as well as for rapidly repairing a defective system.

4.12.1 Field Maintenance Kit

The following list specifies the minimum requirements for adequate performance of field maintenance goals.

Digital Volt Meter - Data Technology Corp. DT-430 (or equivalent)

Complete computer System
Maintenance Manual
Technical Manual
Test diagnostic programs and instructions
Electronic tool kit
Vacuum cleaner
Cleaning Solvant (MEK, FREON, etc)
Wiping cloths

4.12.2 Preventative Maintenance

Basic quality assurance check-out can take place on a time available basis, daily, weekly, or in conjunction with maintenance on other system equipment. Diagnostics can be run on the computer memory, the firmware, and peripheral equipment controllers at the same time. At intervals, not exceeding ninety days, complete system checkout should be run as listed in the following sections.

4.12.3 General Physical Clearing

Vacuum, as necessary, the inside of the computer, especially the power supply, and air vents. Heavy accumulation of dirt will hinder the cooling effects of the fan. If desired, an occasional clearing of logic cords and connectors with MEK, FREON, denatured alcohol, or other non-residue solution may be performed as needed.

4.12.4 System Diagnostic Tests

The (GIT), General Instruction Test, should be run to assure the proper operation of the firmware. (MDT) should be performed to test proper memory operations. Peripheral equipment diagnostic tests should be run on each piece of equipment.

4.12.5 Voltage Margin Test Procedure (reference 1000441)

Voltage margin testing can often isolate a failing system before a problem exists. The technique is to cary the power supply voltages about the nominal operating point while running a test program. If a marginal condition exists, this technique may find it.
Remove the power supply from the chassis and set it along-side the computer taking care not to damage the computer power wiring. Turn on the computer and run the core memory diagnostic program on one memory module. Use a digital volt meter to monitor the supply outputs.
Note: Monitor the voltages on the backplane if possible.
Set the supply voltages as specified in Figure 128 (B), and allow the memory diagnostic to make one complete pass for each setting. Memory test takes approximately four minutes for a 4K memory system. If errors occur, refer to MDT reference manual.

Test #	+5	+12	-16.75
1	5.25	12.60	-17.09
2	5.25	12.60	-16.41
3	5.25	11.40	-17.09
4	5.25	11.40	-16.41
5	4.75	12.60	-17.09
6	4.75	12.60	-16.41
7	4.75	11.40	-17.09
8	4.75	11.40	-16.41

FIGURE 128

After completion of this test, reset the supply voltages to their nominal +5.00, +12.00, and -16.75 volt levels.

4.13 DEPOT MAINTENANCE

The depot level is the second in the three levels of computer maintenance. It is at this point where most logic card and sub-system repair takes place. Repairs that cannot be accomplished here should be referred to the factory. Factory type repairs would include most intermittant component failures, damaged core memory mats, and slow switching diode problems on read only memory systems.

4.13.1 Test Equipment and Fixtures

The following list enumerates the various pieces of test equipment, test boards, computer programs, documentation, and tools required to perform depot level maintenance.

Oscilloscope - Tektronix Model 453 or equivalent
Digital Volt Meter - Data Technology Corp DT-430 or equivalent
Extender Board P/N 1000219
ROS P/N 1000590
ROS P/N 1000591
ROS Diagnostic Board P/N 1000593
System Control Panel P/N 1000237
Teletype ASR33-TTY
Memory Diagnostic Test Program P/N 11004
Basic Computer P/N 8001
Electronic Tool Kit
Technical Manual
Maintenance Manual
Schematics and wire lists for computer
Map and listing of ROS #1 board
Map and listing of ROS #2 board
Read Only Memory test program
General Instruction Test or equivalent P/N 11008

4.13.2 Read Only Memory Troubleshooting

General troubleshooting a ROS board, the engineer should have a thorough knowledge of the theory of operation of this system (refer to section 3, in the maintenance manual). Reference to drawing #1000192 for logic drawings, figure 129 for component location, and the diode map and ROS instruction listing for the particular board under test will be necessary.

Mechanical failures - Visually inspect the board under test for physical condition. Remove any foreign material from board that might tend to short electrical signals together. Check for cracked, broken, or otherwise damaged components. Replace any damaged components. Inspect the diode matrix for touching diode leads. If any are found, gently the touching leads apart. If any physical defect has been found then execute the Read Only Memory Test program to determine if the board now functions properly.

Electronic Failures - Electronic failures can be grouped into classes by symptoms. By determining the specific malfunction, the cause can normally be found. The following procedures will require the board under test to be plugged into the extender board which is inserted into J14 in a basic computer. The computer must be fitted with a system control panel. In the testing procedures, micro instructions will be executed from the system panel (refer to section of this manual if necessary). Apply power to the computer and release the SAVE switch. Ensure that the SELECT switch is in ROS mode Depress RESET. Display "L". All data lights will be out. Display "R2" and then "R1". If "R2" and "R1" do not display hexadecimal "FFFF", continue the following tests.

Voltage Checks measure the -1.5 volt etch bus with respect to ground. If this voltage reads less than zero volts but more positive, than -1.35 volts then replace capacitor C5. If this voltage reads positive with respect to ground then capacitor C3 or C4 is shorted. If the -1.5 volt bus reads zero volts then there is a short circuit between the bus and ground.

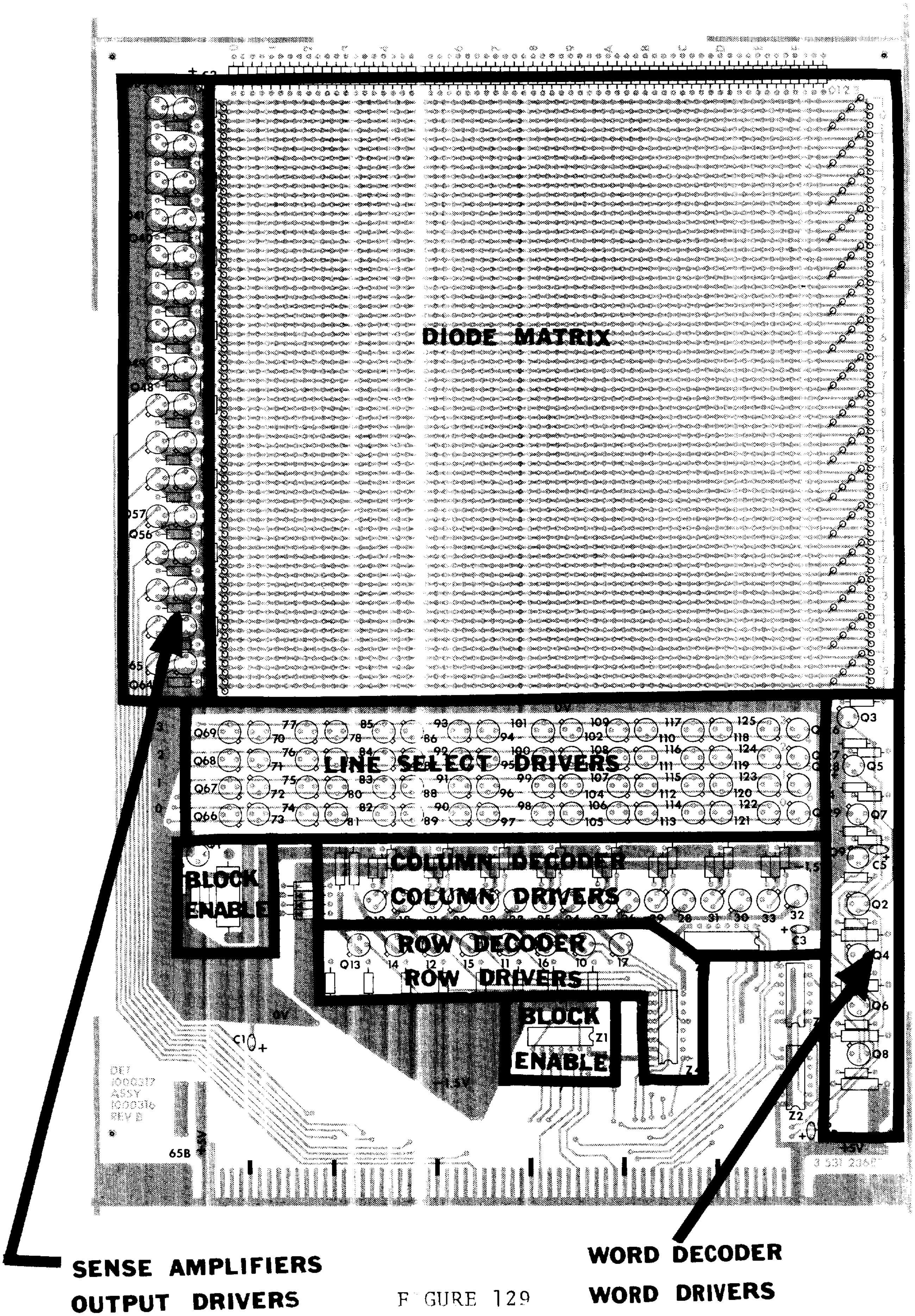

DIODE MATRIX
LINE SELECT DRIVERS
COLUMN DECODER
COLUMN DRIVERS
ROW DECODER
ROW DRIVERS
BLOCK ENABLE
BLOCK ENABLE
SENSE AMPLIFIERS
OUTPUT DRIVERS
WORD DECODER
WORD DRIVERS

FIGURE 129

Measure the +5 volt bus with respect to ground. If this voltage is less than +4.75 volts, then capacitor C1, C2, or C6 is shorted or there is an etch short circuit on the board.

Data Enable DENB/

The signal DENB/ (collector or case of Q1) and pin 8 of Z1 should be at logic zero. Pins 6 and 12 of Z1 should be at logic one. Pins 3, 4, 9, and 13 of Z2 and Z3 should be at logic one. If not, then analyze these circuits to find the bad components.

Word Select Lines WDX

After execution of the specified micro command, the following signals should be observed on the collectors (cases) of these transistors.

MICRO COMMAND	WD0		WD1		WD2		WD3	
	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
1400	-1.5	+5	-.5	-1	-.5	-1	-.5	-1
1401	-.5	-1	-1.5	+5	-.5	-1	-.5	-1
1402	-.5	-1	-.5	-1	-1.5	+5	-.5	-1
1403	-.5	-1	-.5	-1	-.5	-1	-1.5	+5

Row Select Lines RDX

After execution of the specified micro command, the following signals should be observed on the collectors (cases) of these transistors. Y = 0 volts, N = -1.5 volts

COMMAND	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7
	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17
1400	Y	N	N	N	N	N	N	N
1404	N	Y	N	N	N	N	N	N
1408	N	N	Y	N	N	N	N	N
140C	N	N	N	Y	N	N	N	N
1410	N	N	N	N	Y	N	N	N
1414	N	N	N	N	N	Y	N	N
1418	N	N	N	N	N	N	Y	N
141C	N	N	N	N	N	N	N	Y

Column Select Lines CDX

After execution of the following micro command, the following signals should be observed on the collectors (cases) of these transistors.
Y = -1.0 volts N = +2.5 volts

COMMAND	DC0	CD1	CD2	CD3	CD4	CD5	CD6	CD7
	Q19	Q21	Q23	Q25	Q27	Q29	Q31	Q33
1400	Y	N	N	N	N	N	N	N
1420	N	Y	N	N	N	N	N	N
1440	N	N	Y	N	N	N	N	N
1460	N	N	N	Y	N	N	N	N
1480	N	N	N	N	Y	N	N	N
14A0	N	N	N	N	N	Y	N	N
14C0	N	N	N	N	N	N	Y	N
14E0	N	N	N	N	N	N	N	Y

Line Drive Select Lines LDX

After execution of the specified micro command the indicated transistor collector (case) should be at a -1.0 volt potential. If a transistor is not selected, the voltage should be +5 volts.

COMMAND	Q	COMMAND	Q	COMMAND	Q	COMMAND	Q
1400	66	1440	82	1480	98	14C0	114
1404	67	1444	83	1484	99	14C4	115
1408	68	1448	84	1488	100	14C8	116
140C	69	144C	85	148C	101	14CC	117
1410	70	1450	86	1490	102	14D0	118
1414	71	1454	87	1494	103	14D4	119
1418	72	1458	88	1498	104	14D8	120
141C	73	145C	89	149C	105	14DC	121
1420	74	1460	90	14A0	106	14E0	122
1424	75	1464	91	14A4	107	14E4	123
1428	76	1468	92	14A8	108	14E8	124
142C	77	146C	93	14AC	109	14EC	125
1430	78	1470	94	14B0	110	14F0	126
1434	79	1474	95	14B4	111	14F4	127
1438	80	1478	96	14B8	112	14F8	128
143C	81	147C	97	14BC	113	14FC	129

Program (MAP) Diode Failure

If the above procedures have not isolated the problem then the next step is to verify the program matrix (MAP). The reference data for this test is the program listing for the board under test. The program listing has two columns of numbers. The left hand one is the address listing which is numbered 000-0FF, 100-1FF, 200-2FF, or 300-3FF. Corresponding to each address is a 16 bit, four hexadecimal digit number which is the particular command for the specified address. Successively execute the 14XX command and read out on the DATA lights "R2" and "R1" each location. For example if the first location is 200, execute the command 1400. "R2" will display the upper two hexadecimal digits and R1 the lower two. Make a list of the bad bit locations by address. After all programmed addresses have been examined, all that is required is to locate the bad diodes on the card and replace them. A missing "one" indicates an open diode. A missing "zero" should never occur.

Referring to Figure 129 shows that the diode layout is made up of sixty-four rows and sixty-four columns. The column headed by the resistor marked "0" has words with addresses X00, X01, X02, X03. The column associated with the very right-hand resistor has addresses XFC, XFD, XFE, XFF. This demonstrates that each column has four words in it. The two low order bits of the first word in each column are "00". The next word in each column has low order bits 01. Every fourth row of diode positions corresponds to one bit in one word within a particular column.

On the right-hand side of the card above sixteen groups of four diagnol mounted diodes each is the legend: STROBE
0 1 2 3

There are sixteen diodes in each column under this legend marked '0", "1", "2", and "3". The highest diode in the column marked "0" is in the row corresponding to bit position "0" in each word on the card whose address ends in binary "00". The highest diode in the column marked "1" in the same way marks the row for bit position "0" in each word whose address ends with binary "01". These groups of diodes are marked off for the bit positions which they mark.

From this it is seen that the four words in each column have their bits interleaved so that every fourth diode in a column is in the same word.

As an example if the first four words on the card were BF02, 2B00, 2A00, and 4010 then the column under resistor marked "0" would look like the following drawing.

A = diode in word X00
B = diode in word X01
C = diode in word X02
D = diode in word X03
N = no diode

ANNNNNNDABCNANNNABCNANNNABCNABNN NNNNNNNNNNNNNNNNDNNNNNNNNANNNNNNN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Using this information, replace the defective diodes.

Final Test

After going through the above troubleshooting procedures the correct operation of the board should be verified by the Read Only Memory Test program. If the board still fails this test, then it should be returned to the factory for checkout on automatic test equipment and repair. Slow switching diodes and intermittant components generally cannot be found at the depot level of maintenance.

4.14 BACKPLANE TROUBLESHOOTING

For this discussion the backplane and the front panel p.c. board will be covered as a unit. Refer to drawings 1000579, backplane, 1000260, front panel, p.c. board, and 1000269 wire list for interconnecting wiring between the two systems. The only two failure modes for this system are mechanical and electronic component.

Mechanical Failures

Remove the control panel and examine the pin side of the backplane for broken wires and bent pins. Examine the exposed side of the front panel p.c. board for foreign material which could cause a short between etch lines. Examine for broken wires and repair.

If a connector or contact pin is damaged the connector will have to be removed from the backplane. Remove the backplane and front panel p.c. board from the chassis. Using a low voltage soldering iron and solder extractor; one by one remove wires and solder from each pin on the bad connector. Replace the connector with a new one, solder to the backplane, and then replace the wires, if any, that were removed. Loosely bolt the backplane and front panel p.c. board into the chassis. Insert any logic cards in the connectors on the top and bottom two connectors to act as alignment guides. Tighten all the backplane hold down screws. Tighten the hold-down bolts for the front panel p.c. board.

Electronic Failures

Reference Drawing 1000260. The only electronics circuit in this assembly are on the Front Panel p.c. board. This electronics is used to filter the serial teletype line, provide passive pull-up loads for the front panel switches, and control the lamps on the front panel. Using the system control panel, select "Panel" mode and reset all "Command" switches. Display "R1" and "R2". "Data" lights "0" through "7" should be out.

Note any vamp that is illuminated. Enter all ones (FFFF) into the Command switches. Display R1 and R2 and note that data lights "0" through "7" should be on. Note any descrepency. Execute the following commands in this order from the front panel to set "L", "M", "N", and "D" to zeroes.

1300	Clear M,N
1400	Clear L
1100	Clear T

Set SELECT switch to ROS mode and display "L", "M", "N", and "D". All Data lights should be out. Execute the following commands to set all the above bits to "Ones".

13FF	Load N with ones
12FF	Load M with ones
1DFF	Load L with ones
2FFF	Load file F with ones

With the SELECT switch in ROS mode, bits "0" through "7" for DISPLAY "L", "M", "N", and "D" should be lighted. Also "L" bits "8" and "9" should also be on.
Any bad bits found in the above procedure can be fixed by replacing the integrated circuits and transistor assciated with that bit.

4.15 FAILURE ISOLATION

When a failure occurs in a computer system, probably the best method of fault isolation is on a module replacement basis. If the failure is random in nature, with long time intervals between failures, then replacement of the entire computer system would be advised - leaving problem isolation to the depot or factory. Past history of failure indications, in conjunction with failed sub-system information, can prove valuable establishing a sequence of sub-systems for test. For example, if a particular peripheral controller has experienced a high rate of failure, then this unit would probably be one of the first circuit boards to interchange with a known good one.

One at a time, replacement of each computer sub-system with a known good one until the fault disappears. Mark the last system removed as a suspect bad assembly. Next put the machine back to its original configuration while leaving the replaced assembly in place. Run entire system test to verify proper operation. If the system does not perform properly now, then repeat the assembly swapping as outlined above until the system is completely operation.

A typical order of assembly replacement would be:

1. Power Supply
2. Peripheral Equipment Controllers
3. Data Boards
4. Control Board
5. Read Only Memory Boards
6. Core Memory Systems
7. Chassis, Backplane, and Front Panel Board

4.16 TROUBLE-SHOOTING THE CONTROL PROCESSING UNIT (CPU)

For purposes of this discussion, it will be assumed that the reader has a thorough understanding of the engineering description of the Data Boards and Control Board (refer to Section 3.4). Section 4.17 should be reviewed, if necessary, for operation of the system control panel.

This section will try to point out useful test sequences to be used in fault isolation within the CPU. Each area of interest will be treated individually even though in actuality proper operation of one portion usually requires many other sub-systems to be functional. The System Control Panel will be used extended from the Front Panel P.C. Board by using a Front Panel P.C. Extender assembly. At times various boards of the CPU will have to be extended from the backplane to enable signal monitoring with an oscilloscope. It will be assumed that the Backplane, Power Supply, and System Control Panel are functioning normally. Data Board #1 (DB1) is in J10, Control Board (CB) is in J11, and Data Board #2 (DB2) is in connector J12. Pin numbers on the logic cards will be called out as DB1-G7-8 which indicates pin #8 of the chip in location G-7 on Data Board #1 which is in connector J10. Signals on the Backplane will be called out by connector number and pin number (J11-A46). Numbers at right of test stops refer to entries in Figure 130 for error conditions.

FRONT PANEL "CONTROL" SWITCHES AND RUN CONTROL

1. Remove ROS #1 from J14
2. Depress Save
3. Turn on Power
4. Select ROS Mode
5. Mode should be Halt
6. Release Save
7. Mode should be Halt
8. Display "L" should be all zeroes
9. Display "R2", "R1" should be all ones

10. Enter Command 1200

11. Observe "M", "N" are Hex 00

12. Enter Command 12FF

13. Observe "N" is Hex FF

<u>OTHER LOAD COMMANDS AND I/O CONTROL</u>

1. Release Save

2. Select ROS Mode

3. Depress Reset

4. Execute Command 11FF Load "T"

5. Execute Command B020

6. Display "D" for Hex FF

7. Execute Command 1100

8. Execute Command B020

9. Display "D" for Hex 00

10. Execute Command 1700

11. Depress Run

12. Depress Command bit 7

13. Observe Computer in Halt Mode

14. Execute Command 1617 Load "U"

15. Depress Run

16. Depress Command Switch 7

17. Note Computer in Halt Mode

18. Depress Reset

19. Execute 70F0 (Set IO1X, IO2X, IO3X)

10. Depress Clock

11. Mode should be Halt

12. Display "L" should be Hex 001

13. Depress Clock

14. Display "L" should be Hex 002

15. Depress Clock [illegible]53 more times to ensure that "L" reaches Hex Off.

16. Depress Clock, observe "L" to Hex 000

17. Depress Run, Mode should be Run

18. Depress Clock, Mode should be Halt

19. Depress Step, Mode should be Run

20. Depress Clock

21. Depress INT, Mode should be Run

22. Depress Reset, Mode should be Halt

COMMAND SWITCHES

1. Enter Command 11FF

2. Depress Run

3. Observe "L" is Hex 3FF

4. Enter Command 1400

5. Observe "L" is Hex 000

6. Enter Command 1300

7. Observe "M" is Hex 00

8. Enter Command 13FF

9. Observe "M" is Hex FF

20. Monitor with Oscilloscope pins J11-B30, J11-A31, J11-A63 should be Low

21. Execute Command 7080 (clear I10)

22. Monitor with Oscilloscope pins J11-B30, J11-A31, J11-A63 should be High

READ ONLY DIAGNOSTIC P/N 1000593

All other commands for the CPU are checked out with the Read Only Memory Diagnostic Board. This system has the capability of diagnosing various errors and halting or looping on the error for dynamic check-out of the CPU.

Figure 130 AREAS FOR INVESTIGATION

1. RUNX/, HLTL/
2. Run Control, latches for Front Panel Switches
3. MRST/ to L register
4. CPEN/, CLKG/, R register
5. CLK5/, LOOX, L register
6. RUNX, RUNL
7. MRST/ to Run Control
8. RJKX, CPEN/, R register
9. Destination Decoder, Command Decoder, BENR, "B" Bus, ANDX, ADDX, ADDER, CLK3 "A" Bus for particular bit in error
10. Destination Decoder (MRXX), Command Decoder (LRXX) BENR, "B" Bus, ADDX, ADDER, CLK1, "A" Bus, "M" register for bit in error
11. Destination Decoder (NRXX), Command Decoder (LRXX) Clocks (MCLR/, CLK1/), BENR, "B" Bus, ADDX, ADDER, "A" Bus, "N" register for bit in error
12. Destination Decoder (TRXX), Command Decoder (LRXX) CLK1, BENR, "B" Bus, ADDX, ADDER, "A" Bus, "T" register for bit in error
13. Destination Decoder (CG7X), Command Decoder (LRXX, LRSP), Run Control (RUNH/, RUNX/)
14. Destination Decoder (URXX1), Command Decoder (LRXX1), CLK1, BENR, "B" Bus, RENU, ADDX, ADDER, "A" Bus, "U" register for bit in error.
15. Command Decoder (IOXX), EXIO, CLK1/, IO1X/, IO2X/, IO3X/.

Core Memory Trouble-Shooting except under very unusual circumstances, repair of the core memory systems should not be attempted in the field. Refer to Section 3.7 for engineering information relating to this assembly.

4.17 SYSTEM CONSOLE OPERATING PROCEDURES

The operating procedures that are contained in this section will provide maintenance personnel with the following information:

1. System Control Console configuration
2. Abbreviated system commands
3. General practices
4. Initial set-up procedures
5. Exercising the systm control console
6. Load and display registers
   a. L Register
   b. R2 Register
   c. R1 Register
   d. M Register
   e. N Register
   f. T Register
   g. File Register
   h. Link Register
7. Performing register/data transfer utilizing:
   a. FILE Registers
   b. "C Field"
   c. Register Designators
   d. LITERAL Commands
8. Performing register/data control
9. Performing arithmetic operations
   a. ADD
   b. SUBTRACT
10. Performing logical operations
    a. COPY
    b. AND
    c. OR
    d. EXCLUSIVE OR
    e. SHIFT

11. Performing READ/WRITE Memory Operations

12. Application of System Control Console operation to system logic fault location:

    a. Broad Fault
    b. Major Logic Circuit Fault
    c. Logic Circuit Fault
    d. Component Fault (as applicable)

13. This information is for the express purpose of introducing to user the fundamentals of the system control console. It was not practical to use all possible combinations of each command nor all commands in the system command repertoire. Some commands are unique and can only be exercised in a total operating system. Manual manipulation of the controls do not allow such commands as loading the U register, I/O control register, load zero control, etc. to be implemented and observed on the data lamps. However, when troubleshooting and tracing through the logic with test equipment, these commands can be exercised and their results observed at the hardware level.

14. After you have used this seciton several times your proficiency will allow you to expand the use of System Control Console to meet your requirements.

4.17.1 <u>System Control Console Configuration</u>

The system console provides complete control and display facilities. It is primarily used for maintenance, system and firmware checkout. This console provides for display of the CPU registers in addition to the control functions activated by the operator. The features include:

Run and Halt indicators
Display of A-bus
Display of M, N, and L registers
Display of output of read only storage
Four sense switches
Six control switches including: Run, Step, Interrupt, Clock Reset, and Save.
Manual Command execution
Power On/Off

4.17.2 The system control console is shown in figure 31. A brief description of each major group of switches is given. A more detailed description is given in below.

4.17.3 System Control Console Switch Description

1. Display Selector

These seven interlocked switches select the register or bus to be displayed on the system console. The displays which can be selected are:

L-L Register,
R1-eight high order bits of the read-only-storage register
R2-eight low order bits of the read-only-register
M-M register,
N-N register,
D-A-bus.

2. Command

These 16 alternate action switches are substituted for the read only storage on the system and operator consoles when the SELECT switch is in the PANEL position. Depressing the CLOCK switch causes the command set on the switches to be executed. The command may also be executed repeatedly by depressing the RUN switch. These switches are used to gate registers to the A bus display and for entering data into the file and registers.

3. Control

a. Run

This momentary contact switch places the processor in the run mode causing it to exeucte microcommands.

b. Step

This momentary contact switch places the processor in the run mode and as long as the switch is depressed causes an internal interrupt. The halt internal interrupt is bit 7 of the internal status. This switch is normally microprogrammed to cause a processor halt. Since the processor is forced to run when the switch is depressed, the machine can be microprogrammed to cause a single macro instruction to be executed.

c. Interrupt

This momentary contact switch places the processor in the run mode and causes an internal interrupt. The console interrupt is bit 0 of the internal status. This switch is normally microprogrammed to cause a console interrupt.

d. Clock

This momentary contact switch causes the processor to execute a single microcommand. If the processor is running at the time the switch is depressed the processor will come to a forced halt.

e. Reset

This momentary contact switch halts the processor and clears the L register, I/O control register and other control flip-flops. The reset is made available to I/O devices. The computer should not be stopped by this switch. Starting the computer after a reset causes it to start execution at memory location 0.

f. Save

This alternate action switch is the same as the RESET switch but can be set for providing a continuous reset. If this switch is on at the time the power is turned on or off the contents of the memory will not be lost or altered.

4. Select

This alternate action switch selects the console panel command switches (PANEL) or the read only storage (ROS) as the command to be executed next. This switch is not available on the basic console.

5. Sense

The four alternate action sense switches are available on all consoles. The state of these switches may be transferred to a file register or machine register by the Control command. These switches may be used to provide manual control of micro level and macro level programs.

6. Power

This alternate action switch provides operating voltages to the system.

7. Displays

a. Run Lamp

The run lamp is illuminated when the processor is running.

b. Halt Lamp

The halt lamp is illuminated when the power is on and the process is not running.

c. Data Display

On the system console eight lamps (0-7) display the data which is on the A bus of the processor. When the processor is halted the contents of a file register or the T register can be displayed by setting the proper command in the COMMAND switches and enabling the switches by placing the SELECT switch in the PANEL position. The hexadecimal commands used for display are:

File Register f Cf00
T Register B020
Link Register B080

Lamps 8 and 9 make up a two bit register for ROS board selection.

4.17.4 Abbreviated System Commands

A brief outline of the System Commands, flags and registers are shown in Tables 4.17.1 thru 4.17.6.

4.17.5 General Practices

Contingent to daily use, it would be a good idea to physically inspect the system especially if the system has not been operated for several days. The following is only a guide and should be used as applicable to your system operation and environment.

1. Check out system in accordance with specifications in section .

NOTE

Always remove power (power down) before removal or replacement of a PCB.

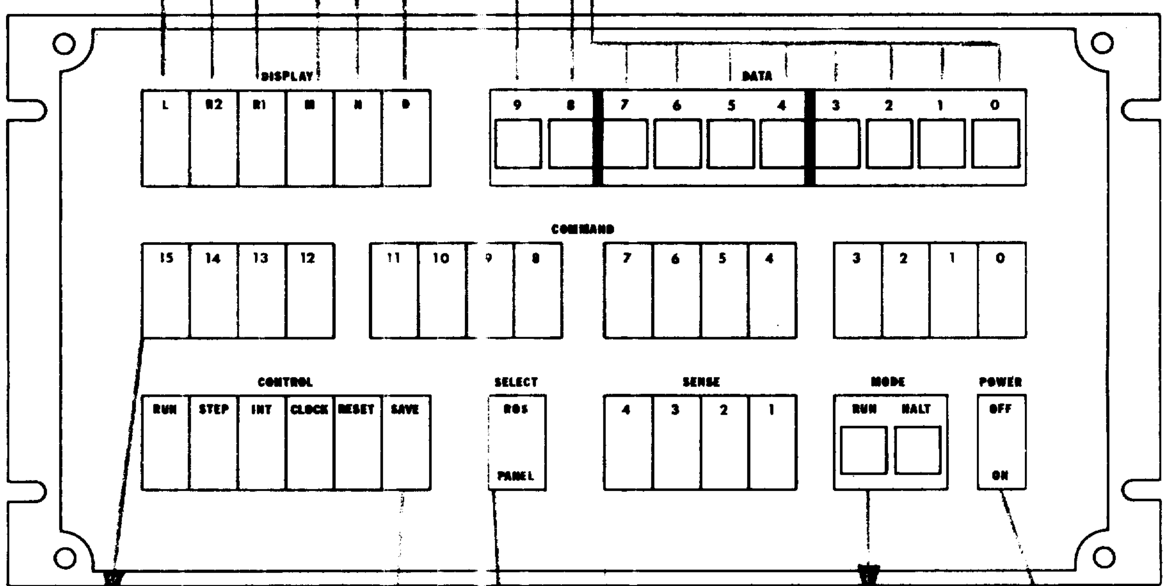
2. If you expect to be removing and replacing PCB boards, checking PCB boards on extender boards, etc. carefully place the power supply on top of the CPU chassis, or to the side.

3. Removal and replacement of a memory module or DMA PCB will require the power supply be moved to the side (to the left side as viewed from the rear of the CPU chassis).

4. Ensure that the cooling fan exhaust at the rear of the unit is not obstructed. Also the air vents on both sides of the chassis should be free of any foreign material to allow for proper cooling air flow through the unit.

DATA DISPLAY

- DISPLAY OF L REGISTER
- DISPLAY OUTPUT OF READ ONLY STORAGE
- DISPLAY OF M AND N REGISTERS
- DISPLAY OF A-BUS
- DISPLAY OF ROS BOARD ADDRESS
- EIGHT DISPLAY LAMPS



COMMAND

16 Alternate action switches provide for manual command execution.

MODE

RUN: Run lamp illuminated when CPU is running.

HALT: Halt lamp illuminated when CPU is not running.

POWER

Provide operating voltages to the system.

CONTROL

RUN: Momentary action places CPU in the RUN mode.

STEP: Momentary action causes execution of one instruction.

INTERRUPT: Momentary action places CPU in run mode and causes a console interrupt.

CLOCK: Momentary action causes CPU to execute a a single microcommand.

RESET: Halts the CPU.

SAVE: Alternate action provides continuous reset.

SENSE

Four alternate action switches provide manual control of micro/macro level programs.

SELECT

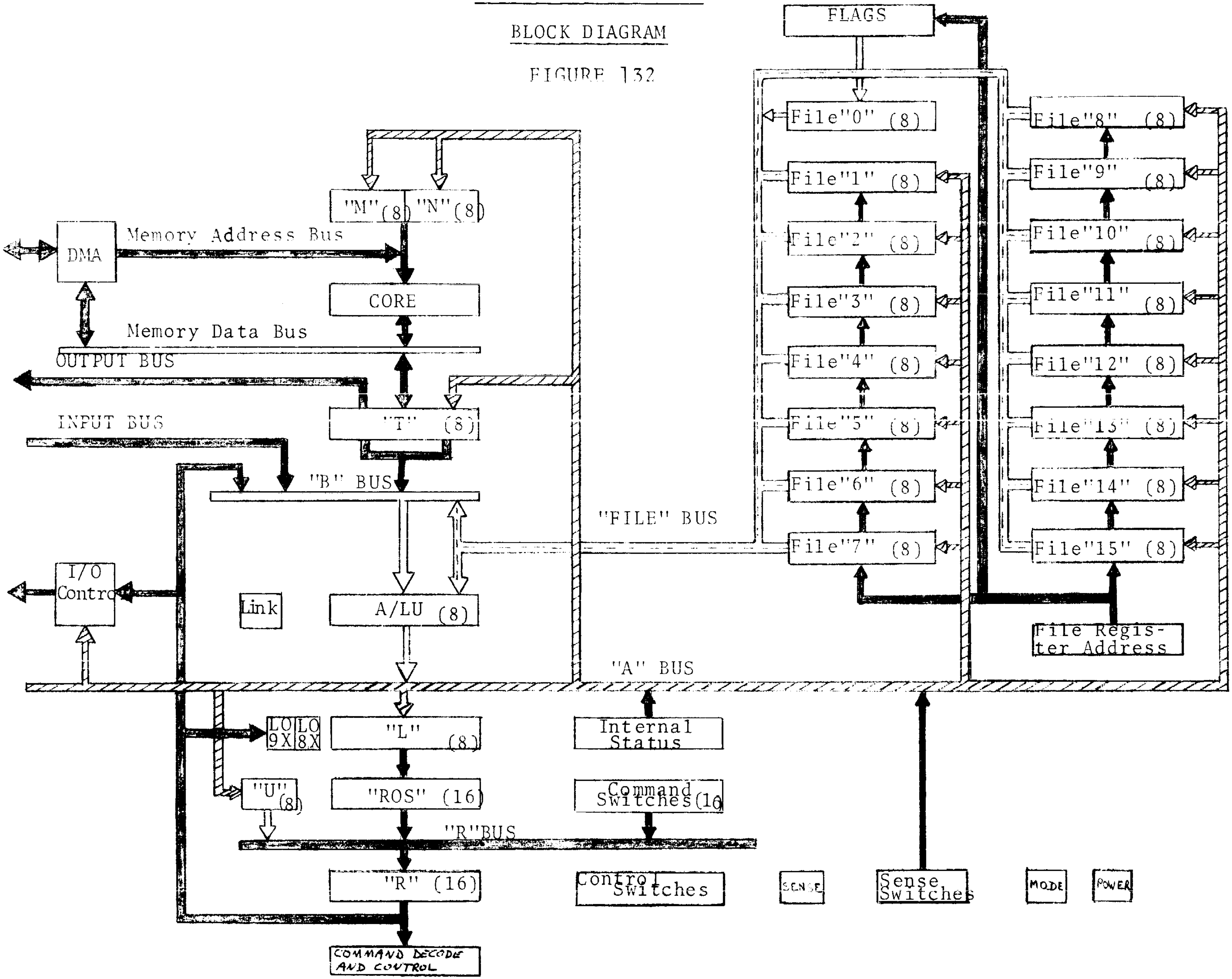
Alternate action selects panel or ROS as the command to be executed next.

FIGURE 131
SYSTEM CONTROL CONSOLE

COMPUTER FUNCTIONAL

BLOCK DIAGRAM

FIGURE 132



	CODE	MNEMONIC	NAME	OPERATION
LITERAL	0XXX	E	Execute	XXX is ORed with U Register
CLASS	10XX	LZ	Load Zero	No Operation
COMMANDS	11XX	LT	Load T	XX replaced contents of T
	12XX	LM	Load M	XX replaced contents of M
	13XX	LN	Load N	XX replaces N, and M is cleared
	14XX	JP	Jump	to page 0
	15XX	JP	Jump	to page 1
	1CXX	JP	Jump	to page 2
	1DXX	JP	Jump	to page 3
	16XX	LU	Load U	XX replaces contents of U
	17XX	LS	Load Seven	Internal Controls
	2fXX	LF	Load File (f)	f = File Number
	3fXX	AF	Add to File	f = File Number
	4fXX	TZ	Test if Zero	Skip on Full Mask
	5fXX	TN	Test if $\overline{\text{Zero}}$	Skip on Any Mask
	6fXX	CP	Compare	Skip on f + XX $> 2^8 - 1$

TABLE 4.17.4.1

continued....

	CODE	MNEMONIC	NAME	C FIELD (BINARY)
OPERATE CLASS COMMANDS	7fC*r	K	Control	0000 No Operation 0001 Enter Sense Switches 0010 Shift Right Four Bits 0100 Enter Console Switches 1000 Clear I/O Mode 1001 Control Output 1010 Data Output 1011 Space Serial TTY 1100 Spare 1110 Data Input 1111 Spare
	8fC*r	A	Add	0001 Modify Flags 0010 Select T 0100 Sum +1 1000 Sum + Link Bit
	9fC*r	S	Subtract	0001 Modify Flags 0010 Select T 0100 Inhibit Increment 1000 Difference + Link
	AfC*r	R/S	Read/Write Memory	00XX Transfer 01XX Decrement 10XX Add Link 11XX Increment XX1X Half Cycle XXX1 Write (Not Read)
	BfC*r	C	Copy	XXX1 Modify Flags XX1X Select T X1XX Sum + 1 1XXX Sum + Link
	CfC*r	0	OR	XXX1 Modify Flags XX1X Select T X1XX Select T Complement 1XXX Reset ZERO Flag
	DfC*r	X	Exclusive OR	Same as OR
	EfC*r	N	AND	Same as OR
	FfC*r	H	Shift	XXX1 Modify Flags XX1X Shift Right X1XX Insert ONE 1XXX Link Control

* = 1, result of operation placed in file (f).

TABLE 4.17.4.1

Operation Code	Mnemonic	Instruction Name
Control		
00	HLT	Halt
01	TRP	Trap
02	ESW	Enter Sense Switches
03	PMP	Protect Memory Page
04	DIN	Disable Interrupt System
05	EIN	Enable Interrupt System
06	DRT	Disable Real Time Clock
07	ERT	Enable Real Time Clock
08	R01	Reset Ovflo and Set WL to 1
09	R02	Reset Ovflo and Set WL to 2
0A	R02	Reset Ovflo and Set WL to 3
0B	R04	Reset Ovflo and Set WL to 4
0C	S01	Set Ovflo and Set WL to 1
0D	S02	Set Ovflo and Set WL to 2
0E	S03	Set Ovflo and Set WL to 3
0F	S04	Set Ovflo and Set WL to 4
34	NOP	No Operation
Conditional Jump		
10	JOV	Jump if Overflow Set
11	JAZ	Jump if A Equal to Zero
12	JBZ	Jump if B Equal to Zero
13	JXZ	Jump if X Equal to Zero
14	JAN	Jump if A Negative
15	JXN	Jump if X Negative
16	JAB	Jump if A Equals B
17	JAX	Jump if A Equals X
18	NOV	Jump if Overflow not Set
19	NAZ	Jump if A not Equal to Zero
1A	NBZ	Jump if B not Equal to Zero
1B	NXZ	Jump if X not Equal to Zero
1C	NAN	Jump if A not Negative
1D	NXN	Jump if X not Negative
1E	NAB	Jump if A not Equal to B
1F	NAX	Jump if A not Equal to X
Shift		
20	LLA	Logical Left A
21	LLB	Logical Left B
22	LLL	Logical Left Long
24	LRA	Logical Right A
25	LRB	Logical Right B
26	LRL	Logical Right Long
28	ALA	Arithmetic Left A
29	ALB	Arithmetic Left B
2A	ALL	Arithmetic Left Long
2C	ARA	Arithmetic Right A
2D	ARB	Arithmetic Right B
2E	ARL	Arithmetic Right Long

TABLE 4.17.4.2 continued....

Operation Code	Mnemonic	Instruction Name
Input/Output		
30	IBS	Input Byte Serially
31	IBA	Input Byte to A
32	IBB	Input Byte to B
33	IBM	Input Byte to Memory
38	OBS	Output Byte Serially
39	OBA	Output Byte from A
3A	OBB	Output Byte from B
3B	OBM	Output Byte from Memory
Register Operate		
40	ORA	OR B with A
41	XRA	Exclusive--OR B with A
42	ORB	OR A with B
43	XRB	Exclusive--OR A with B
44	INX	Increment X
45	DCX	Decrement X
46	AWX	Add Word Length to X
47	SWX	Subtract Word Length from X
48	INA	Increment A
49	INB	Increment B
4A	OCA	One's Complement A
4B	OCB	One's Complement B
4C	TAX	Transfer A to X
4D	TBX	Transfer B to X
4E	TXA	Transfer X to A
4F	TXB	Transfer X to B
Memory Reference		
60	JMP	Jump
68	RTJ	Return Jump
70	IWM	Increment Word in Memory
78	DWM	Decrement Word in Memory
80	LDX	Load X
88	STX	Store X
90	MUL	Multiply
98	DIV	Divide
A0	ADA	Add to A
A8	ADV	Add Variable
B0	SBA	Subtract from A
B8	SBV	Subtract Variable
C0	CPA	Compare A
C8	CPV	Compare Variable
D0	ANA	And
D8	ANV	And Variable
E0	LDA	Load A
E8	LDV	Load Variable
F0	STA	Store A
F8	STV	Store Variable

TABLE 4.17.4.2
continued....

Addressing Modes

0	Direct Page 0	6	Extended
1	Direct Relative	7	Literal
2	Indirect Page 0		Fixed Length
3	Indirect Relative		Two Byte with A
4	Indexed		Variable
5	Indexed with Bias		Indirect Jumps

TABLE 4.17.4.2

SOFTWARE INSTRUCTIONS

BIT	FLAG
0	- Overflow Result Condition
1	- Negative Result Condition
2	- Zero Result Condition
3	- Concurrent I/O Request Line
4	- Internal Interrupt
5	- I/O Reply Line
6	- Serial Teletype and/or T_8
7	- External Interrupt Line

TABLE 4.17.4.3

FILE REGISTER 0 FLAGS

DESIGNATOR	MNEMONIC	REGISTER
0		none
1	T	T Register
2	M	M Register
3	N	N Register
4	L	L Register-addresses: 000-0FF and 200-2FF
5	K	L Register-addresses: 100-1FF and 300-3FF
6	U	U Register
7	S	U Register ORed into command (except for Control command)

TABLE 4.17.4.4

REGISTER DESIGNATORS FOR OPERATE COMMANDS

BIT	INTERNAL STATUS
0	Console Interrupt
1	(spare)
2	Real-Time Clock Interrupt
3	Memory Protect Error Interrupt
4	Memory Parity Error Interrupt
5	Memory Boundary Error Interrupt
6	Console Halt Switch
7	Power Fail/Restart Interrupt

TABLE 4.17.4.5

INTERNAL STATUS BITS

MODE	CONTROL ACTIVITY
0	None
1	Control Output (COXX/)
2	Data Output (DOXX/)
3	Space Serial Teletype
4	Spare
5	I/O Acknowledge (IOAK/)
6	Data Input (DIXX/)
7	Spare

TABLE 4.17.4.6

BYTE I/O CONTROL MODES

5. READ through a section before performing the steps specified. Repeat the step through if the desired results are not obtained at first. Steps performed out of sequence or steps not properly performed may easily end in undesirable results.

6. When turning the CPU OFF, make it a Habit to perform the following steps in this sequence.

   a. DEPRESS CLOCK, then

   b. DEPRESS RESET, then

   c. DEPRESS SAVE.

   This will ensure that when power is turned OFF, the contents of memory will not be altered or lost.

7. When turning the CPU ON, ensure that the Save switch is ON (depressed in the Down Position). This will ensure that when the power is turned on, the contents of memory is not altered or lost.

8. Use the CPU System Block Diagram and logic diagrams to aid you while exercising the commands. When practical, use an oscilloscope to aid in circuit analysis. Make notes on your logic drawings as applicable.

9. If the CPU is used daily, it may not be necessary to perform all preliminary steps. However, if you should experience or suspect any problems, go to the applicable section and perform all preliminary steps.

4.17.6 Initial Set-Up Procesures

The CPU should conform to the specifications in section . Ensure that you have checked the central processor (data and control boards) with ROS diagnostic board P/N 1000593.

4.17.7 Exercising the System Control Console

At this point a static operation of the system control console will be performed. This will give you a feel of the switches.

NOTE

Before performing the static operation. remove the 115-120VAC from the CPU. This can be accomplished by setting the power supply toggle switch to OFF or removing the power cord from the CPU or AC source.

1. This system control console (SCC) incorporates three mechanically different switches. Physically they appear similar, however they exhibit different responses to being depressed.

2. These switches are categorized as:

   a. ALTERNATE Action (A)
   b. MOMENTARY Action (M)
   c. INTERLOCK Action (I)

   Shown in Figure 133 as applicable to each switch function.

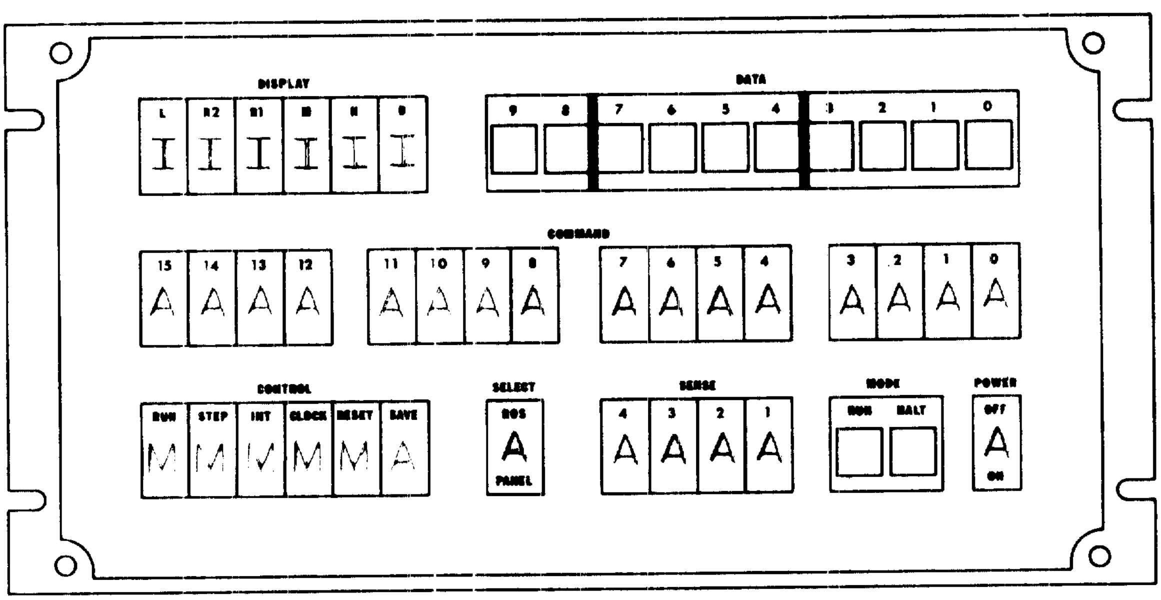


FIGURE 133 - SYSTEM CONTROL CONSOLE

3. Alternate Action Switch. - The SCC employs a spring loaded alternate action switch. When the switch is depressed it will remain locked in the down (ON) position. Depressing the switch again will release the locking mechanism, allowing the switch lever to return to its upper-most position (OFF).

NOTE

Do not push up to release the switch. Irreparable damage will result.

a. On the SCC, DEPRESS (SET) the power switch to the ON position. You will note the clicking sound of the locking mechanism.

b. On the SCC, DEPRESS (RESET) the power switch to the OFF position. You will not the clicking sound of releasing the locking mechanism.

c. ACTUATE the following switches in the same manner:

   1) SENSE Switches 1-4
   2) SELECT Switch
   3) SAVE Switch
   4) COMMAND Switches 0-15
      (It is possible to set more than one COMMAND switch at at time.)

4. Momentary Action Switch. - The SCC employs a spring loaded momentary action switch. When the switch is depressed it will make contact for as long as it is held down. Releasing the lever will allow the switch to return to its normal (upper-most) OFF position.

   a. In the control section on the SCC, DEPRESS the RUN switch, then release.

   b. ACTUATE the following switches in the same manner.

      1) STEP
      2) INT.
      3) CLOCK
      4) RESET

5. Interlock Action Switch. - The SCC employs six spring loaded interlock action switches located in one array. Depressing one switch will release and deactivate all others. Only one switch is to be depressed at a time.

   a. In the DISPLAY section on the SCC, DEPRESS the "L" switch, this will release any other switch that was down.

   b. DEPRESS the "R2" switch, the "L" switch will be released.

   c. Continue with the remaining DISPLAY selector switches.

6. Reconnect AC power to the power supply.

   a. Insure that the SAVE switch is ON (DOWN position).

   b. Insure that the POWER switch is OFF.

   c. Set the power supply AC toggle switch to the ON position. (uppermost position)

   d. Depress POWER ON. You should hear the power supply fan start up and blowing air. The HALT Lamp should be ON (illuminated). If you do not get these results go to section   for locating the problem.

   e. If the fan functions and the HALT lamp goes ON then proceed by re-resetting the SAVE switch to OFF.

NOTE

You are now ready to exercise the CPU system command.

NOTE

Figure 134 shows the conventions used throughout this section. These will provide an aid to the user so he may quickly and easily check his performance against the expected results.

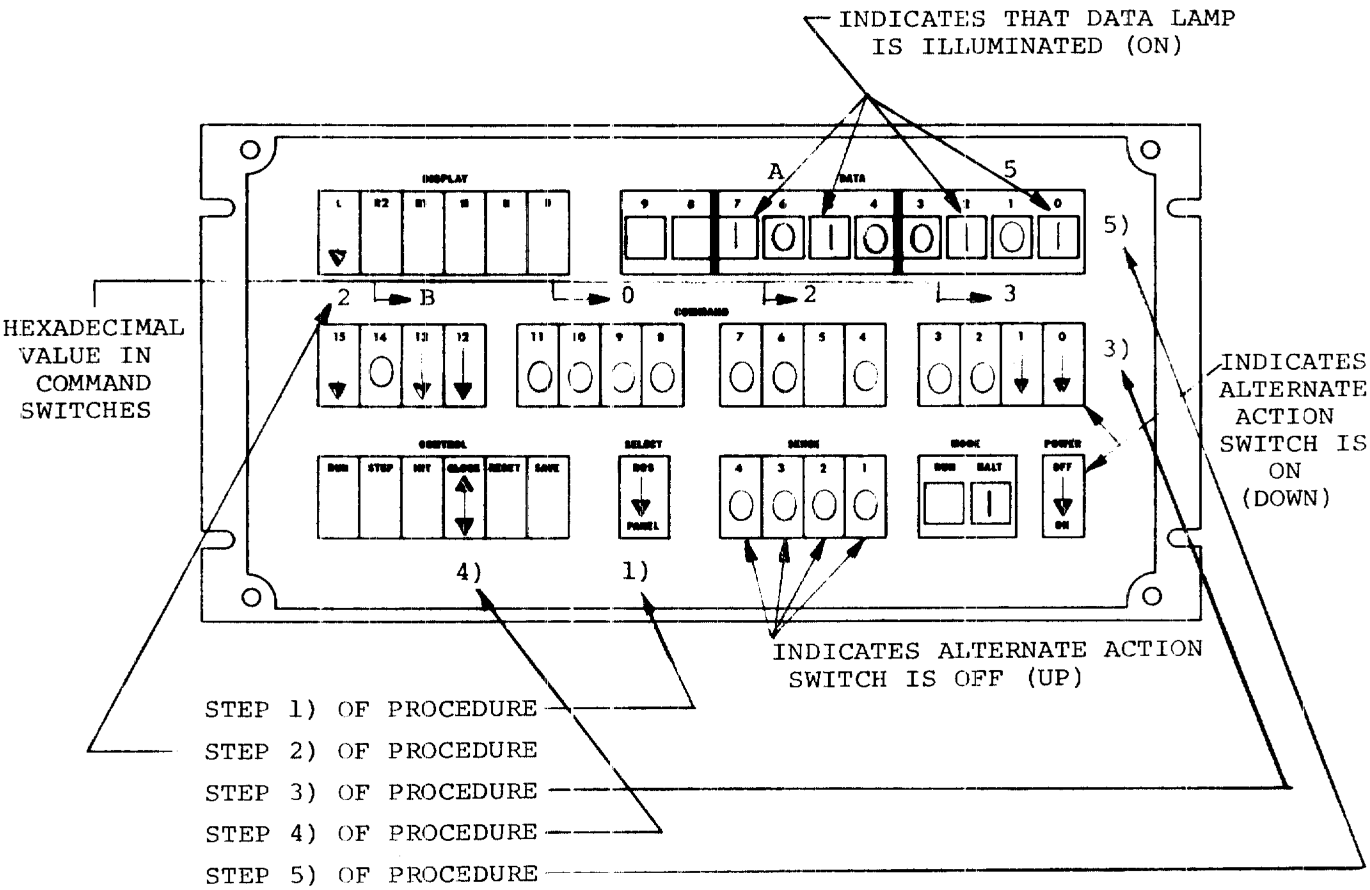


FIGURE 134

SYSTEM CONTROL CONSOLE

4.17.8 Load and Display Registers

Insure completion of section 4.17.7 (a-e).

4.17.9 L REGISTER

JP JUMP

14/15/1C/1D	Literal
15	0

The contents of the eight-bit literal are placed in the eight low order bits of the L register; the content of the bit 8 is placed in L_8 and the content of bit 11 is placed in L_9. The location of the next command to be executed is at the address specified by the new contents of the L register. The execution time of the command is two cycles. The Jump operation codes for the four 256 word pages in read only storage are as follows:

14 - Jump to locations 000-0FF (page 0)
15 - Jump to locations 100-1FF (page 1)
1C - Jump to locations 200-2FF (page 2)
1D - Jump to locations 300-3FF (page 3)

1. DEPRESS the SELECT switch to the PANEL position (DOWN).

2. DEPRESS "L" DISPLAY select switch.

3. Set the COMMAND switches with the hexadecimal (Hex) code of 1401_{16}.

4. DEPRESS the CLOCK switch.

5. OBSERVE the "0" DATA lamp. It should be ON.

6. DEPRESS the "D" DISPLAY switch.

7. OBSERVE the "0" DATA lamp. It should be ON.

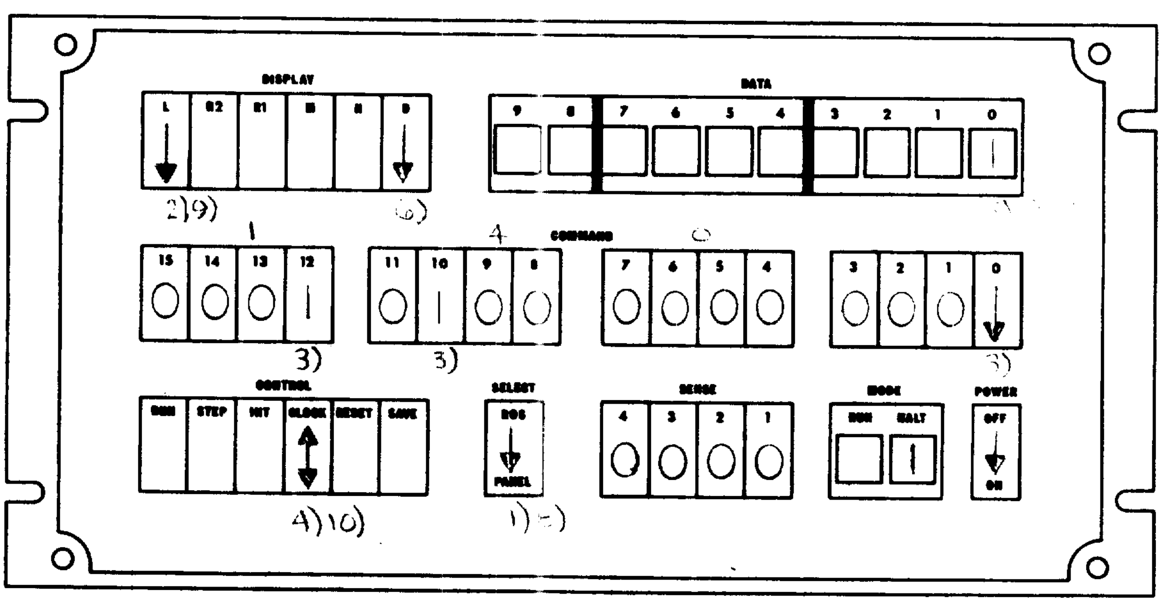


FIGURE 135 - SYSTEM CONTROL CONSOLE

NOTE

You have just manually entered a count of one (1) in the read only storage address counter as displayed by "L". The "D" display indicates that this data is still held on the "A" bus.

8. Reset the SELECT switch to ROS.

9. Depress "L" display switch.

10. Continuously DEPRESS the clock switch.

11. OBSERVE the data display lamps. Each time the CLOCK is DEPRESSED the displayed data will change.

NOTE

The sequence in which the displayed data changes is relative to the ROS microprogram. The first few commands appear in binary order. However, they will seem to jump around to different binary values. This is normal. You may want to observe the display and check it against the machine listing for your particular ROS. You may start at address "0" by simply depressing reset. This will always start the microprogram at address zero.

	Data Lamps 9 8
12. With both data lamps "8" and "9" out, ROS #1 (J14) was selected. To address (be sure to start with step 1).	
ROS #2 (J15) substitute 1501_{16} in step 3)	01
ROS #3 (J16) substitute $1C01_{6}$ in step 3)	10
ROS #4 (J17) substitute 1D01 in step 3)	11

DEPRESS the "L" display switch and OBSERVE the data lamps.

13. This MANUAL "L" register loading operation will allow you to enter at any point within the microprogram. Rather than stepping from location 000 up to 1C8, enter 15C8 in the command (step 3) and start at address 1C8 stepping through as required.

NOTE

REMEMBER, you must be in SELECT ROS mode to step through the addressing of the micro-program.

4.17.10 "R2" ("R" register most significant 8 Bits R07X Through R15X)

1. DEPRESS the SELECT switch to the PANEL position (down).

2. DEPRESS "R2" display.

3. Set the COMMAND switches with the HEX code of $FF00_{16}$.

4. OBSERVE the DATA lamps 0-7. All lamps should be ON (0-7).

5. Reset each command switch one at a time (8-15)

6. OBSERVE the data lamps go out (0-7). All lamps should be out.

NOTE

You have just manually entered a data value of FF_{16} into the upper half of the "R" register. You reset that same data. In effect, each flip-flop R08X through R15X was checked.

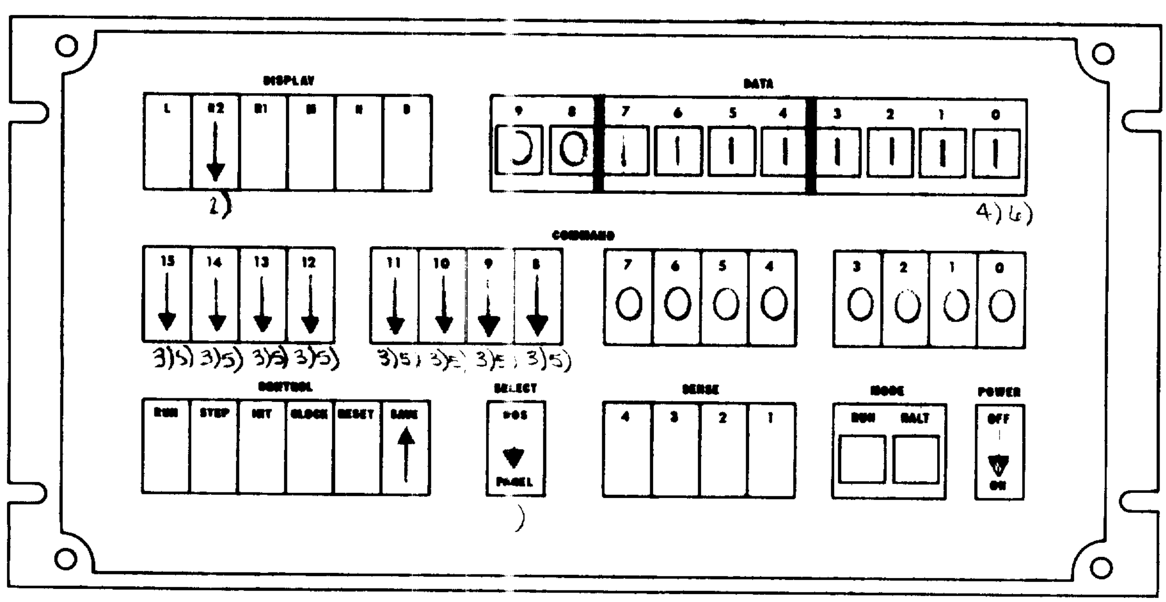


FIGURE 136 - SYSTEM CONTROL CONSOLE

4.17.11 "R1" ("R" Register Least Significant 8-Bits R00X-R07X

1. DEPRESS SELECT switch to the PANEL position (down).

2. DEPRESS R1 DISPLAY switch.

3. Set the command switches with a hex code of $00FF_{16}$.

4. OBSERVE the DATA lamps 0-7. All lamps should be ON (0-7).

5. RESET each command switch one at a time (0-7).

6. OBSERVE the data lamps go out (0-7). All lamps should be out.

NOTE

You have just manually entered a data value of FF_{16} in the lower half of the "R" register. You reset that same data. In effect, each flip-flop R00X through R07X was checked.

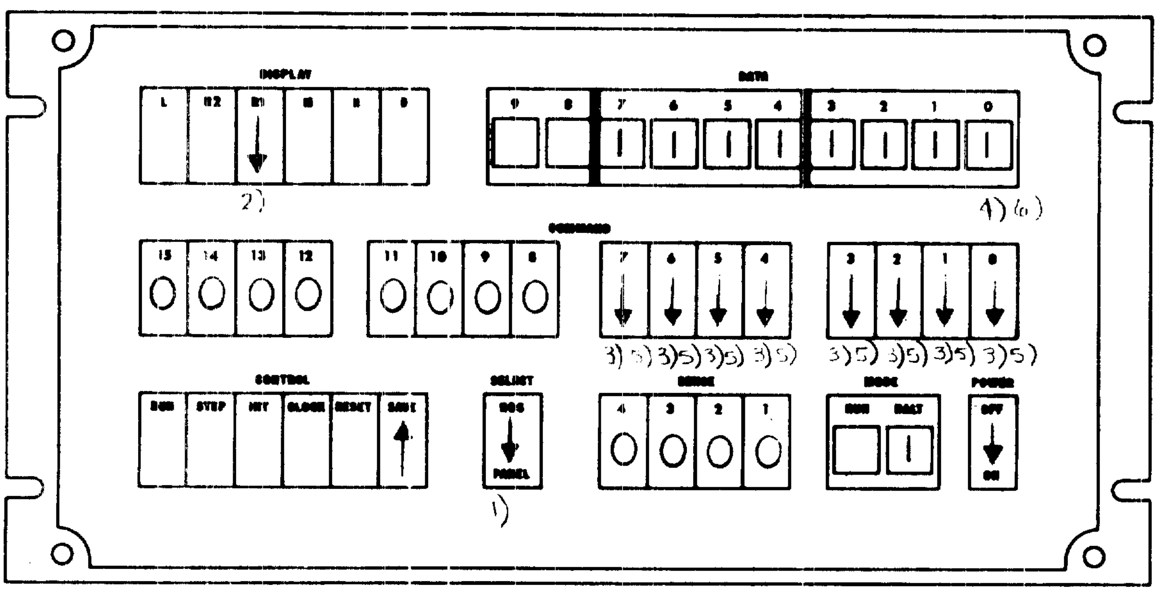


FIGURE 137 - SYSTEM CONTROL CONSOLE

	ROS DATA		
ROS ADDRESS	B F	0 2	HEXADECIMAL
0 0 0	1 0 1 1 1 1 1 1	0 0 0 0 0 0 1 0	BINARY
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	DATA LAMPS
DISPLAYED BY "L"	DISPLAYED BY R2	DISPLAYED BY R2	
	2 B	0 0	
0 0 1	0 0 1 0 1 0 1 1	0 0 0 0 0 0 0 0	
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	

etc.

NOTE

The following steps are set up to enable the user to step through his particular microprogram. This procedure shows you how to extract and display the data, but in no way is it meant to be exactly like your particular microprogram. Chart information is used in steps below. Substitute your microprogram for the one listed to obtain desired read out.

1. RESET the SELECT switch to the ROS position. (UP)
2. DEPRESS "L" display switch.
3. DEPRESS RESET switch.
4. OBSERVE data lamps 0-7. All lamps should be out.
5. DEPRESS "R2" display switch.
6. OBSERVE data lamps 0-7

4.17.12 ROS Data Display

The data information in Chart is typical of a microprogram routine. This example is entitled "Read Next Instruction." We exercise control of the ROS ("A") address counter, then observe the data in both halves of the "R" register. (Figure 138)

* Read Next Instruction

ROS ADDRESS	ROS DATA				
000	BF02	RNI0	CM	OV	Clear OV/W and M
001	2300		LF	PU,X'00'	Clear P
002	2A00		LF	PL,X'00'	
003	4010		TZ	F0,X'10'	Internal Interrupt
004	15F8		JP	INT2	Yes
005	7110		K	I,1	Enter Sense Switches
006	4180		TZ	I,X'80'	Switch 4 on
007	1574		JP	Load	Yes, Load Boot Strap
008	2F00	RNI1	LF	OV,X'00"	Clear OV/W
009	C302	RNI5	MM	PU	
00A	AA03	RNI4	RN	PL	Get OP Code
00B	1410		JP	RNI6	Ignore Interrupts
00C	8A43	RNI	IN	PL	Update P
00D	A382	RNI3	RM	PU,L	
00E	4098	RNI2	TZ	F0,X'98'	Test for Interrupts
00F	15D3		JP	INT	Service Request
010	B120	RNI6	C	I,T	Save OP Code
011	2C10		LF	S1,OTAB+16	Base Address of Table
012	7129		KT*	I,2	Shift Right 4
013	8C20		A	S1,T	
014	61A0		CP	I,X'A0'	Memory Reference
015	CC05		MK	S1	No

* Yes, Get Operand Address

CHART 4.17.7

With reference to chart
the data displayed would be:

ROS ADDRESS 000

HEX	B				F			
BINARY	1	0	1	1	1	1	1	1
"R1"	7	6	5	4	3	2	1	0

7. <u>DEPRESS</u> "R1" display switch.

8. OBSERVE the data lamps 0-7.

With reference to chart __________
the data displayed would be:

ROS ADDRESS 000

HEX	0				2			
BINARY	0	0	0	0	0	0	1	0
"R1"	7	6	5	4	3	2	1	0

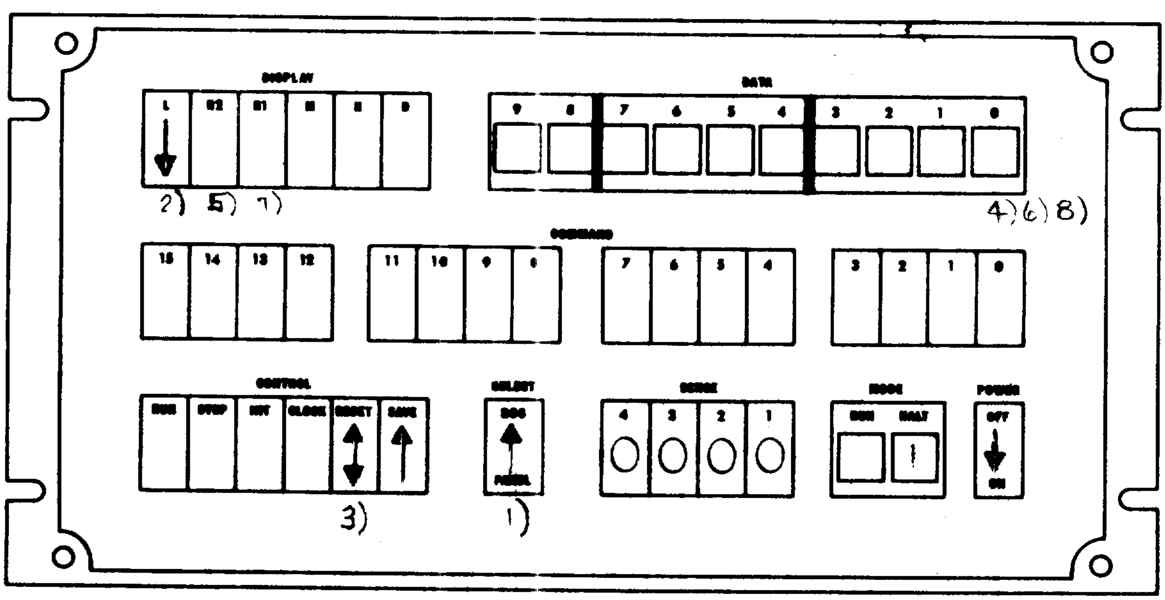


FIGURE 138 - SYSTEM CONTROL CONSOLE

NOTE

To start at some location other than 000 perform the following steps (also, see section 4.1.6.81.12).

9. With reference to Chart 4.17.7, the contents of address, 012 can be displayed.

10. DEPRESS the SELECT switch to PANEL position. (Down)

11. SET the COMMAND switches with the hex code 1412_{16} (Jump to page 0)

12. DEPRESS the CLOCK switch.

13. OBSERVE the data lamps 0-7. You should have:

1				2				← HEX
0	0	0	1	0	0	1	0	← BINARY
7	6	5	4	3	2	1	0	← DATA LAMPS

14. RESET the SELECT switch to the ROS position (up).

15. DEPRESS "R2" display switch.

16. OBSERVE the DATA lamps. You should have

7				1				← HEX
0	1	1	1	0	0	0	1	← BINARY
7	6	5	4	3	2	1	0	← DATA LAMPS

17. DEPRESS THE "R1" display switch.

18. OBSERVE the DATA lamps 0-7. You should have

2				0 9				← HEX
0	0	1	0	1	0	0	1	← BINARY
7	6	5	4	3	2	1	0	← DATA LAMPS

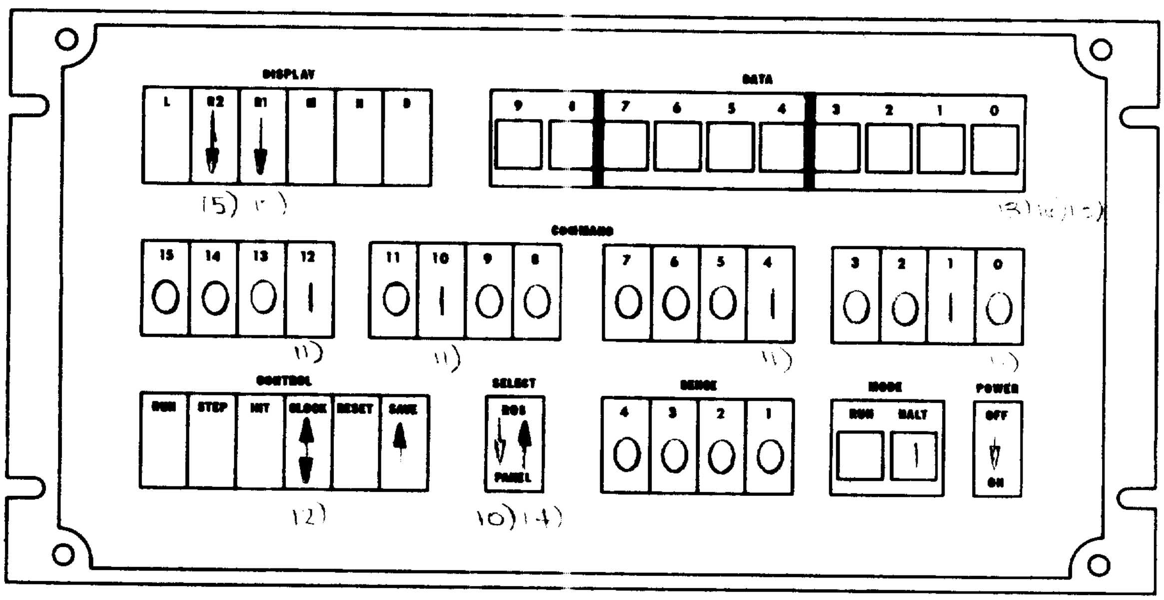


FIGURE 139 - SYSTEM CONTROL CONSOLE

4.17.13 <u>"M" REGISTER (12XX)</u>

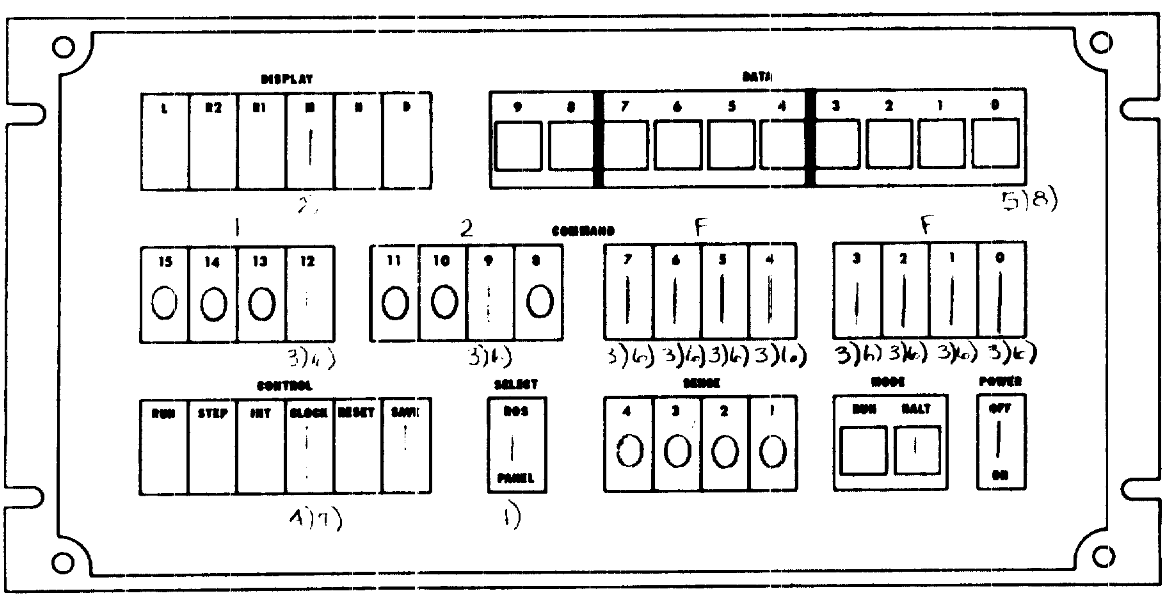
LM LOAD M

12	Literal
15	0

1. DEPRESS the SELECT switch to the PANEL position. (Down)
2. DEPRESS the "M" display switch.
3. SET the COMMAND switches to the HEX code $12FF_{16}$. (Load "M" with FF_{16}.)
4. DEPRESS the CLOCK switch.
5. OBSERVE the DATA lamps 0-7. All lamps should be ON (0-7).
6. RESET the COMMAND switches to the HEX code 0000_{16}.
7. DEPRESS the clock switch.
8. Observe the data lamps 0-7, all lamps should be out (0-7).

NOTE

Any hexadecimal value may be used to replace the "XX" in the command 12XX as you may require.



SYSTEM 140 - SYSTEM CONTROL CONSOLE

4.17.14 "N" REGISTER (13XX)

LN LOAD N

13	Literal

15 ... 0

The contents of the eight-bit field are placed in the N register and the M register is cleared.

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "N" display switch.
3. Set the COMMAND switches to the HEX code $13FF_{16}$ (load "N" and Clear "M").
4. DEPRESS the CLOCK switch.
5. OBSERVE the DATA lamps 0-7. All lamps 0-7 should be ON.
6. RESET the COMMAND switches to HEX code 0000_{16}.
7. DEPRESS the CLOCK switch.
8. OBSERVE the DATA lamps 0-7. All lamps should be out.

NOTE

Any hexadecimal value may be used to replace the "XX" in the command 13XX as you may require LN(1300) also clears "M" register.

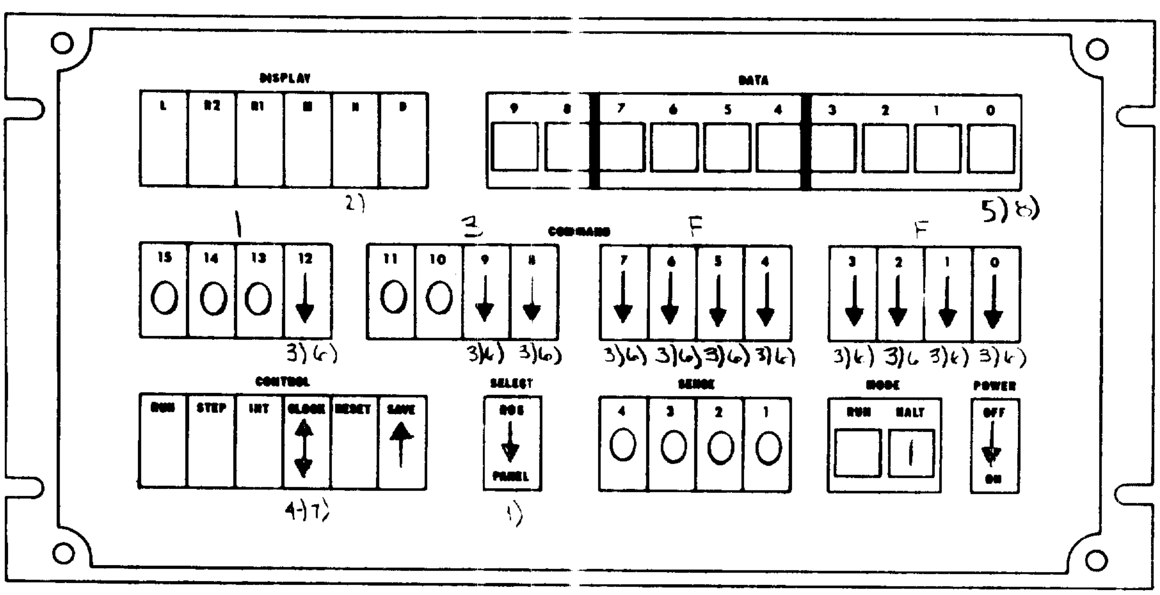


FIGURE 141 - SYSTEM CONTROL CONSOLE

4.17.15 "T" REGISTER (11XX)

LT LOAD T

11/19	Literal
15	0

The contents of the eight-bit literal field are placed in the T Register.

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "D" display switch.
3. Set the COMMAND switches with the HEX code $L1FF_{16}$ (load T with FF).
4. OBSERVE DATA lamps 0-7, as each switch 0-7 is depressed, the DATA lamp above it will go ON.
5. DEPRESS the CLOCK switch.
6. SET COMMAND switches with the HEX code $B020_{16}$ (copy T).
7. OBSERVE the DATA lamps 0-7. All lamps should be ON.
8. Set the COMMAND switches with the HEX code 1100_{16} (load T with 00).
9. OBSERVE DATA lamps 0-7. All lamps 0-7 should be out.
10. DEPRESS the CLOCK switch.
11. SET the COMMAND switches with the HEX code $B020_{16}$ (copy T).
12. OBSERVE the DATA lamps. All lamps should be out.

NOTE

Any hexadecimal value may be used to replace the "XX" in the command 13XX as required.

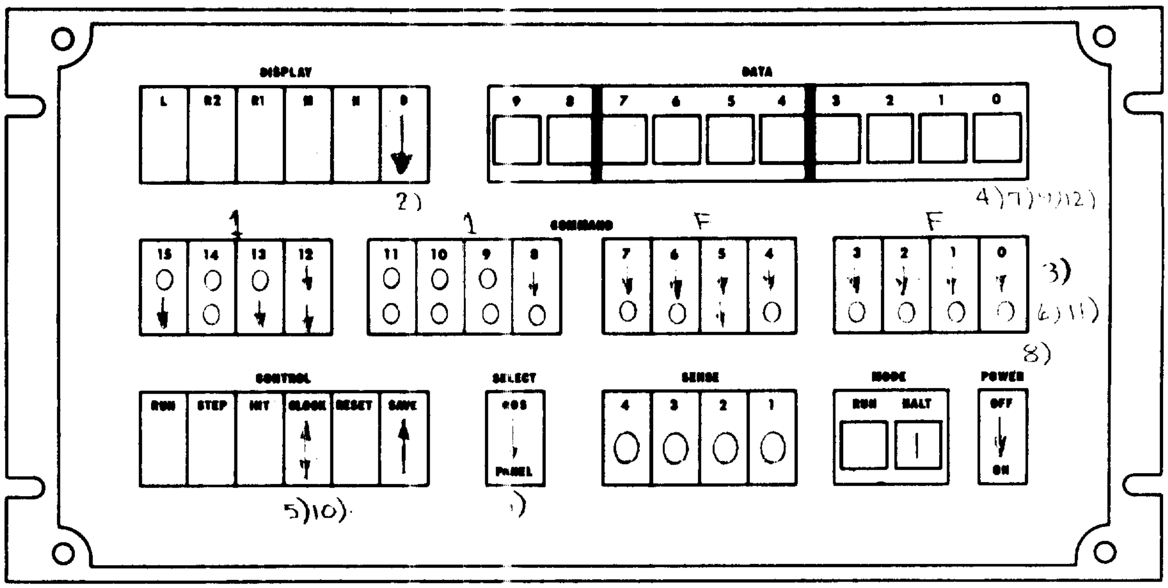


FIGURE 142 - SYSTEM CONTROL CONSOLE

NOTE

The command B020 used above is frequently utilized in checking the data flow through the CPU. It is the copy (BfC*r) command. B020 is defined as: copy the contents of the "T" register. Data is held on the "A" bus.

4.17.16 FILE ("f") REGISTERS (2fXX)

LF LOAD FILE

2	f	Literal
15		0

The literal command for loading a file is 2fXX, where "f" is defined as files 1 through 15. File "0" is used for flag status and cannot be loaded with a command.

1. DEPRESS the SELECT switch to the PANEL position (down).

2. DEPRESS the "D" display switch.

3. SET the COMMAND switches with the HEX code $21FF_{16}$. (Load file with FF.)

4. OBSERVE DATA lamps 0-7 go ON.

5. DEPRESS the clock switch.

6. SET the COMMAND switches to HEX code C100. (OR file 1 with 0)

7. OBSERVE DATA lamps 0-7, all should be ON.

8. SET the COMMAND switches with the HEX code 2100_{16} (load file 1 with 00)

9. DEPRESS the CLOCK switch.

10. OBSERVE the data lamps 0-7, all should be out.

11. SET the COMMAND switches with the HEX code C100.

12. OBSERVE DATA lamps 0-7, all should be out.

Any hexadecimal value from 1 through F may be used in the f field, so as to select the desired file. The command CfC*r is the inclusive OR function. C100 as used above is defined: Inclusive OR the contents of file 1 with "0". This will put the selected data in file 1 on the "A" bus.

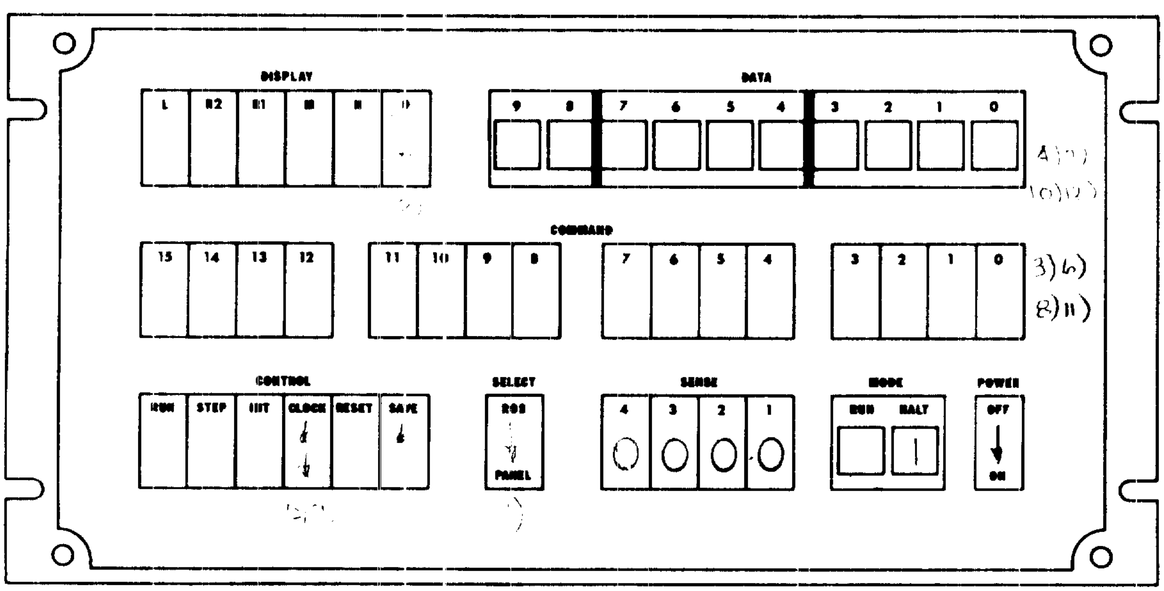


FIGURE 143 - SYSTEM CONTROL CONSOLE (page 4-76)

4.17.17 "LINK" REGISTER (Control Board J11)

1. DEPRESS SELECT switch to panel position (down).

2. DEPRESS "D" display switch.

3. SET the COMMAND switches with the HEX code $11FF_{16}$ (load T with FF).

4. OBSERVE DATA lamps 0-7, all should be ON.

5. DEPRESS CLOCK.

6. Check that "FF" was entered into the "T" register by entering $B020_{16}$ on the COMMAND switches.

7. OBSERVE DATA lamps 0-7, all should be ON.

8. Enter 2101_{16} (load file 1 with 01) on the COMMAND switches.

9. DEPRESS CLOCK.

10. Check that "01" was entered into file 1 by entering C100 on the command switches.

11. OBSERVE DATA lamps 0-7 only. Lamp #0 should be ON.

12. Enter 3120 (add to file 1 the contents of the "T" register, sum placed in file 1).

13. DEPRESS clock.

14. OBSERVE DATA lamps, all should go ON, as this is the "FF" data from the "T" register dumped into the "B" bus then put on the "A" bus.

NOTE

The addition of the FF_{16} to 1_{16} has just been accomplished. The result in 8 bits equals zero. The CARRY OUT (DATA BIT CRY7) one set the LINK register.

15. Check the sum of the addition by entering $C100_{16}$ (Inclusive OR the contents of file 1 with 0).

16. Observe data lamps 0-7, all should be Out.

17. CHECK the LINK register by entering $B080_{16}$ into the command switches.

18. OBSERVE DATA lamps 0-7, only lamp #0 should be ON.

19. CHECK the ZERO SET of the LINK register by sutstituting two numbers whose sum will equal no greater than FF_{16}. After the addition, the link register should be <u>zero set</u>.

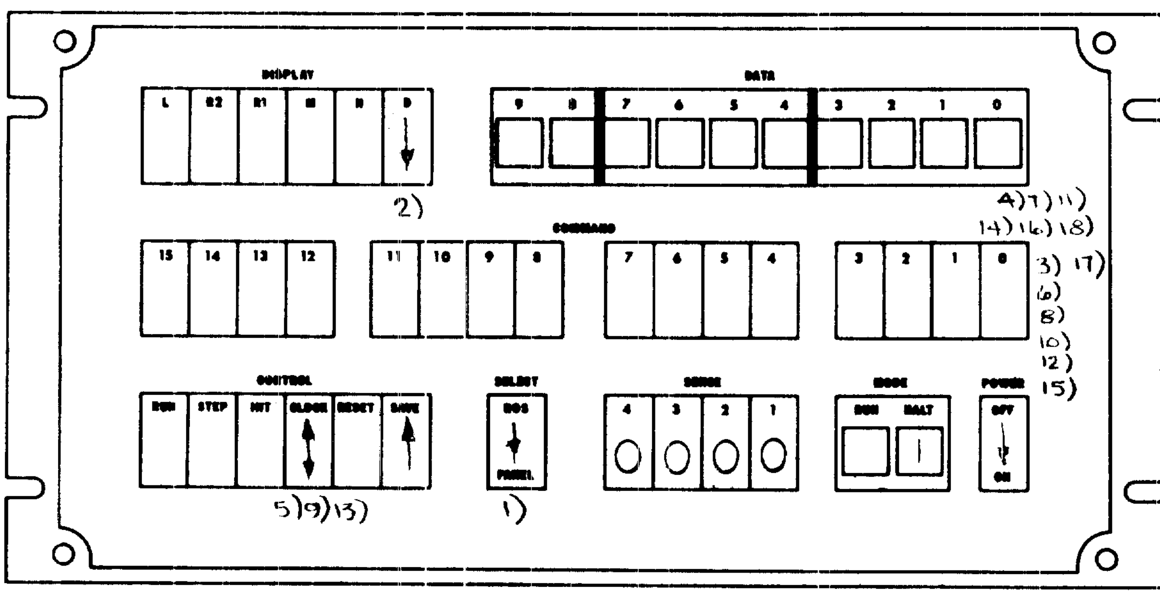


FIGURE 144 - SYSTEM CONTROL CONSOLE

4.17.18 Performing Register/Data Transfer

Transfer of data from the designated file register or the "T" register to designated registers is accomplished in the following procedures.

4.17.19 "T" Register Data Transferred to a Designated File Register

1. DEPRESS the SELECT switch to panel position (down).
2. DEPRESS the "D" DISPLAY switch.
3. Enter 1110_{16} on the command switches (load "T" with FQ6).
4. DEPRESS CLOCK.
5. CHECK the contents of the "T" register by entering $B020_{16}$ on the command switches.
6. OBSERVE that only data lamps 4-7 are ON.
7. ENTER 2100_{16} on the command switches (load file #1 with 00).
8. DEPRESS CLOCK.
9. Check the contents of File #1 by entering $C100_{16}$ on the command switches.
10. Observe the DATA lamps. All lamps should be out.
11. ENTER $B120_{16}$ on the command switches. (Copy "T" into File 1.)
12. DEPRESS CLOCK.
13. CHECK the contents of File #1 by entering C100 on command switches.
14. OBSERVE the DATA lamps 0-7, only lamps 4-7 should be on ($F0_{16}$).

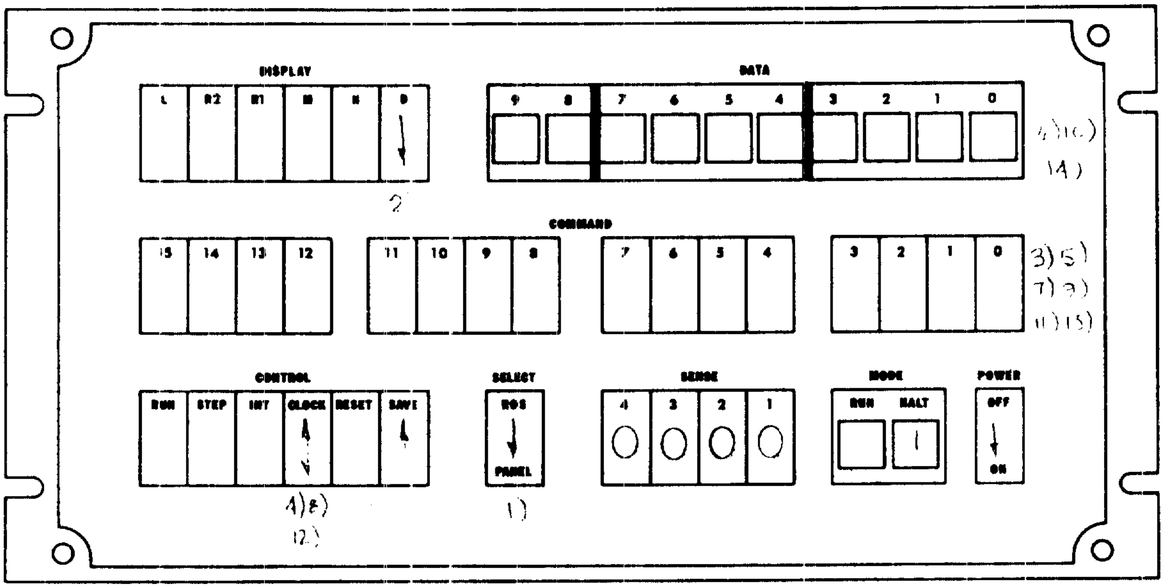


FIGURE 4.45 - SYSTEM CONTROL CONSOLE

4.17.20 <u>"T" Register Data Transferred to File #1 and Back to "T" Register</u>

1. DEPRESS the SELECT switch to PANEL position (down).

2. DEPRESS the "D" DISPLAY switch.

3. ENTER $11F0_{16}$ on the COMMAND switches (load T with $F0_{16}$).

4. DEPRESS CLOCK.

5. CHECK the contents of the "T" register by entering $B020_{16}$ on the COMMAND switches.

6. OBSERVE that only data lamps 4-7 are ON ($F0_{16}$).

7. Enter 2100_{16} on the COMMAND switches. (Load File #1 with 00_{16}).

8. DEPRESS CLOCK.

9. CHECK the contents of FILE #1 by entering $C100_{16}$ on the COMMAND switches.

10. OBSERVE that all DATA lamps are OUT (00_{16}).

11. ENTER $B161_{16}$ on the COMMAND switches. (Copy the contents of "T", ADD one, place sum in File #1 and back in "T".

12. DEPRESS CLOCK.

13. CHECK the contents of the "T" register by entering B020 on the COMMAND switches.

14. OBSERVE the DATA lamps. Lamps "0" and 4-7 should be on ($F1_{16}$).

15. CHECK the contents of File #1 by entering C100 on the COMMAND switches. (Same as 14).

NOTE

A value of $F0_{16}$ in "T" plus a value of 01_{16} was transferred to File #1 and back to "T". The value of "plus 01_{16}" came from the "C" field (bit 6) of the BfC*r command. This was used to show that the transfer of data back into "T" was accomplished.

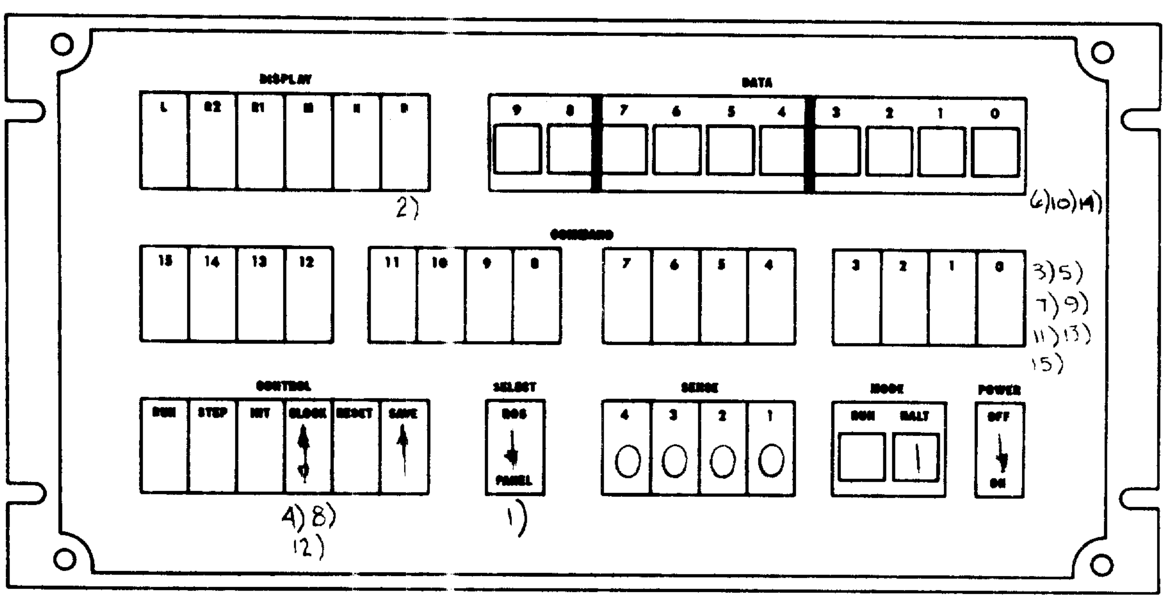
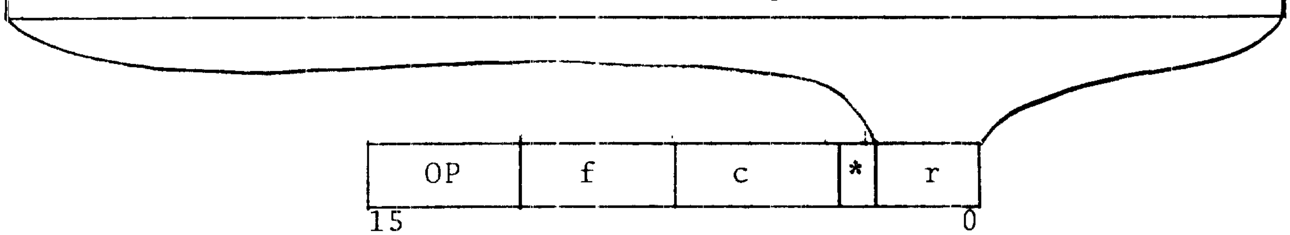


FIGURE 146 - SYSTEM CONTROL CONSOLE

4.17.21 Transfer of data to other registers is accomplished by changing the register designator code. Below gives the codes.

REGISTER DESIGNATORS FOR OPERATE COMMANDS

DESIGNATOR (HEXADECIMAL)	MNEMONIC	REGISTER
0		none
1	T	T Register
2	M	M Register
3	N	N Register
4	L	L Register - addresses: 000-Off and 200-2FF
5	K	L Register - addresses: 100-1FF and 300-3FF
6	U	U Register
7	S	U Register ORed into command (except for Control command)



4.17.22 To display the results of a transfer into a designated register the following is applicable.

T Register - Enter B020 on command switches.

M Register - Depress "M" display switch

N Register - Depress "N" display switch

L Register - Depress "L" display switch

4.17.23 The LINK control was exercised in Section 4.17.16 and will be used in another procedure.

4.17.24 Literal commands were used in Section 4.17.9 and will be used again in other procedures.

4.17.25 Performing register/data control.

4.17.26 Console Sense Switch Check (Control Command)

Enter Sense Switches: The status of the four console sense switches are placed in the four high order bits of the file register designated by f. The four low order bits are set to 1-bits.

K CONTROL

7	f	c	*	r

15 ... 0

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "D" DISPLAY switch.
3. ENTER 7110_{16} on the command switches. (Control-enter sense switch into File #1).
4. OBSERVE DATA lamps 0-7, only lamps 0-3 should be ON (OF_{16}).
5. DEPRESS SENSE switch 4.
6. OBSERVE DATA lamp #7. It should be ON.
7. DEPRESS remaining SENSE switches.
8. OBSERVE all lamps 4-7 are ON. Lamps 0-3 should remain ON.
9. RESET all SENSE switches.
10. OBSERVE DATA lamps, only 0-3, should be ON.

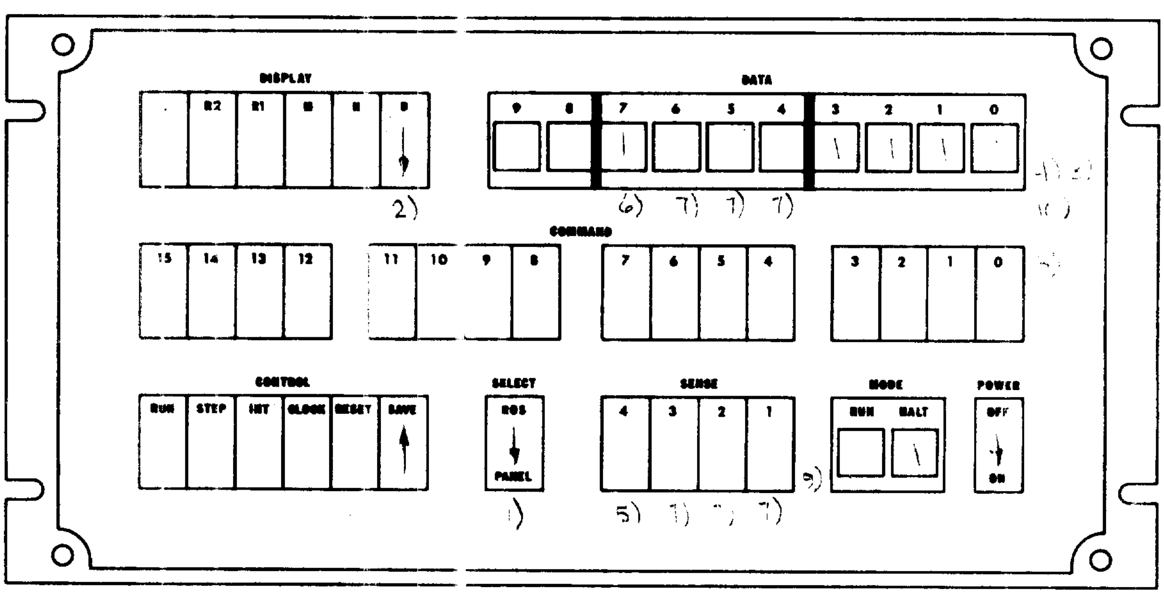


FIGURE 147 SYSTEM CONTROL CONSOLE

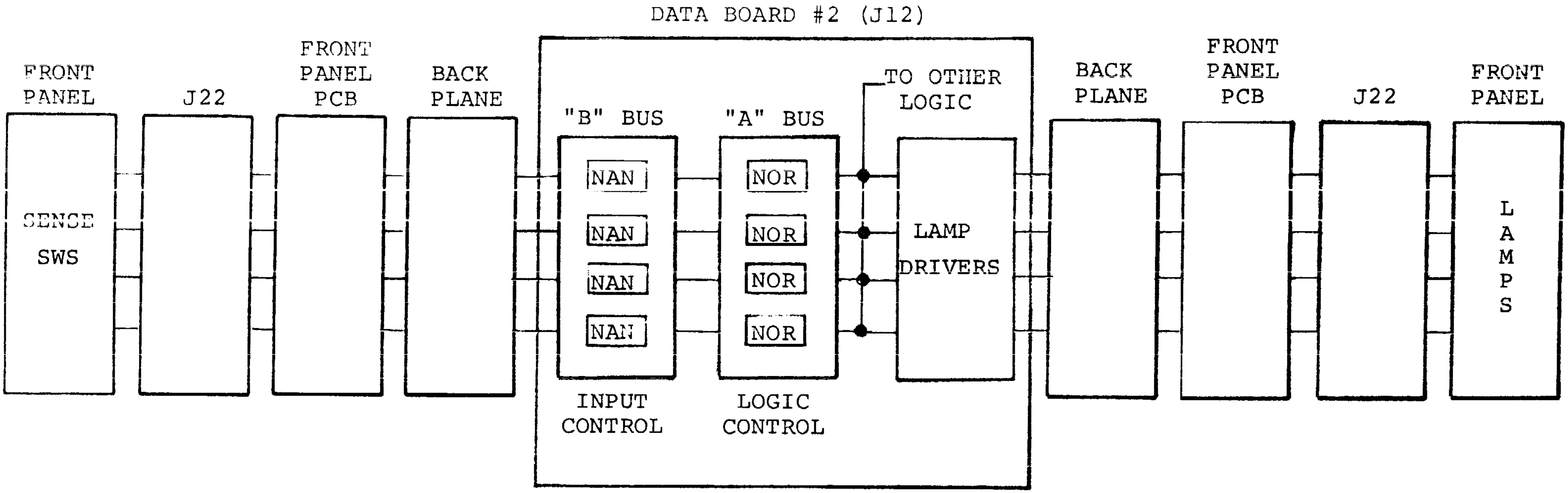


FIGURE 148

SENSE SWITCH DATA FLOW

1. DEPRESS the SELECT switch to the PANEL position (down).

2. DEPRESS the "D" DISPLAY switch.

3. ENTER 2160_{16} on the COMMAND switches (load File #1 with 60_{16}.)

4. DEPRESS CLOCK.

5. CHECK the contents of File #1 by entering $C100_{16}$ on the COMMAND switches.

6. OBSERVE that only data lamps #5 and 6 are on (60_{16}).

7. Enter 7120_{16} on the COMMAND switches. (Shift right file 4)

8. OBSERVE DATA lamps. All lamps except #0 and 3 are ON.

9. DEPRESS CLOCK.

10. CHECK the contents of File #1 by entering $C100_{16}$ on the COMMAND switches.

11. OBSERVE the DATA lamps. All lamps except #0 and #3 should be ON ($F6_{16}$).

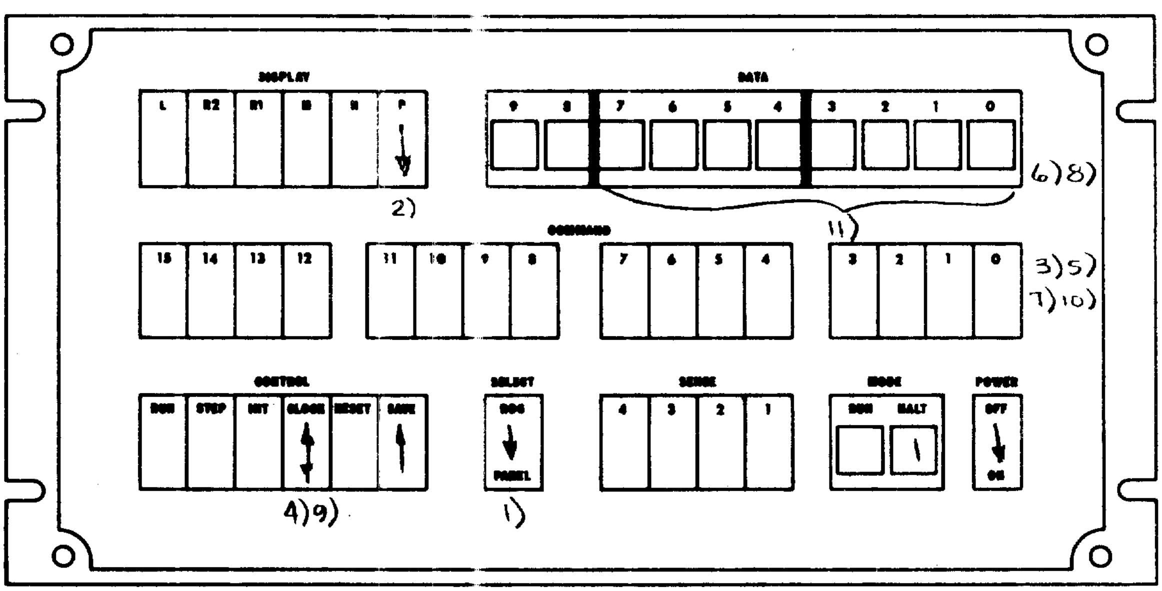


FIGURE 149 - SYSTEM CONTROL CONSOLE

NOTE

You have just checked the SENSE switches. Also, the logic associated with these switches. A block analysis would be as in Figure

Following the data in the logic diagram as you are exercising commands can aid you in trouble-shooting. You must use other commands to isolate logic functions through which known good data must flow. Most major hardware failures can be detected and bad component isolated by thorough examination with the commands manually executed on the system control console.

4.17.27 Shift Right File 4 (Control Command)

Shift File Right 4: The four high order bits of the file register designated by f are placed in four low order bits of the file register. The four high order bits are set to 1-bits.

4.17.28 Performing Arithmetic Operations

The eight-bit arithmetic/logic unit performs all manipulation of data including: addition, logical AND, logical OR, logical exclusive OR, and one bit left and right shifts. The output of this logic network is the A-bus which is the input to the file and other machine registers. All byte data movement is performed over this bus. The output of the file is one of the inputs to the arithmetic/logic unit; the other is the B bus. Inputs to this bus are determined by the command, its options, and the I/O mode. Bus inputs are the true output of the T register, the complement output of the T register, the Input bus and the eight bit literal contained in some commands.

4.17.29 Add (With Link Control)

A ADD

8	f	c	*	4

15 ... 0

The selected operand is added to the contents of the file register designated by f. The sum is placed in the file register (f), if * is a 0-bit, and in the register designated by r. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result and modification of the condition flags.

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "D" DISPLAY switch.
3. ENTER $210F_{16}$ on the COMMAND switches. (Load File #1 with $0F_{16}$.)
4. DEPRESS CLOCK.
5. CHECK the contents of the File #1 by entering C100 on the command switches.

7. Enter $11F0_{16}$ on the COMMAND switches (load "T" with $F0_{16}$).

8. DEPRESS CLOCK.

9. CHECK the contents of File #1 by entering B020 on the command switches.

10. OBSERVE that only DATA lamps 4-7 are ON.

11. ENTER 8101_{16} on the COMMAND switches. (Add to File #1 the contents of "T" plus 1 and place sum in File #1.)

12. DEPRESS CLOCK.

13. OBSERVE that only DATA lamps 0-3 are ON. ($0F_{16}$ File 1 Data)

14. DEPRESS COMMAND switch 5. (Select the contents of the "T" register, ($F0_{16}$).

15. OBSERVE that all DATA lamps are ON (FF_{16}).

16. DEPRESS COMMAND swithc 6. (ADD one to the sum; the sum of F & F.)

17. OBSERVE that all DATA lamps go out.

18. ENTER $E080_{16}$ on the COMMAND switches. (This will put the link register on the "A"bus.)

19. OBSERVE that only DATA lamp #0 is ON. This means that a carry out took place and was stored in the link register.

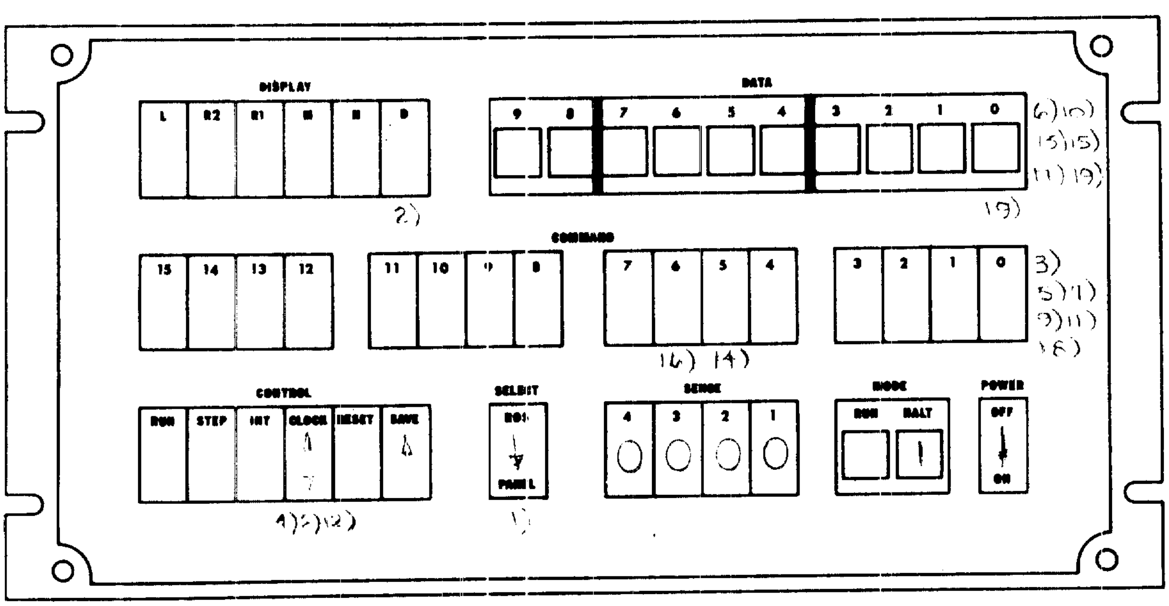


FIGURE 150 - SYSTEM CONTROL CONSOLE

4.17.30 Subtract (2's Complement)

S SUBTRACT

9	f	c	*	r

15 0

The complement of the selected operand plus one is added to the contents of the file register designated by f. The difference is placed in the file register (f) if * is a 0-bit, and in the register designated by 4. The result is a 2's complement subtraction. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result, and modification of the condition flags.

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "D" DISPLAY switch.
3. Enter $113f_{16}$ on the COMMAND switches. (Load "T" with $3F_{16}$)
4. DEPRESS CLOCK.
5. CHECK the contents of "T" by entering C100 on the COMMAND switches.
6. OBSERVE the DATA lamps, on 0-5 should be ON.
7. ENTER $217F_{16}$ on the COMMAND switches. (Load File #1 with $7F_{16}$.)
8. DEPRESS CLOCK.
9. CHECK the contents of File #1 by entering C100 on the COMMAND switches.

10. OBSERVE that only DATA lamps 0-6 are ON ($7F_{16}$).

11. ENTER 9120_{16} on the COMMAND switches. (Subtract the contents of "T" from File #1, place results in File #1.)

12. OBSERVE that only DATA lamp #6 is ON. ($7F_{16}$ - $3F_{16}$ = 40_{16}.)

13. DEPRESS CLOCK.

14. Check contents of File #1 by entering $C100_{16}$ on the COMMAND switches.

15. OBSERVE that only data lamp #6 is ON. The result of $7F_{16}$ - $3F_{16}$ = 40_{16}.

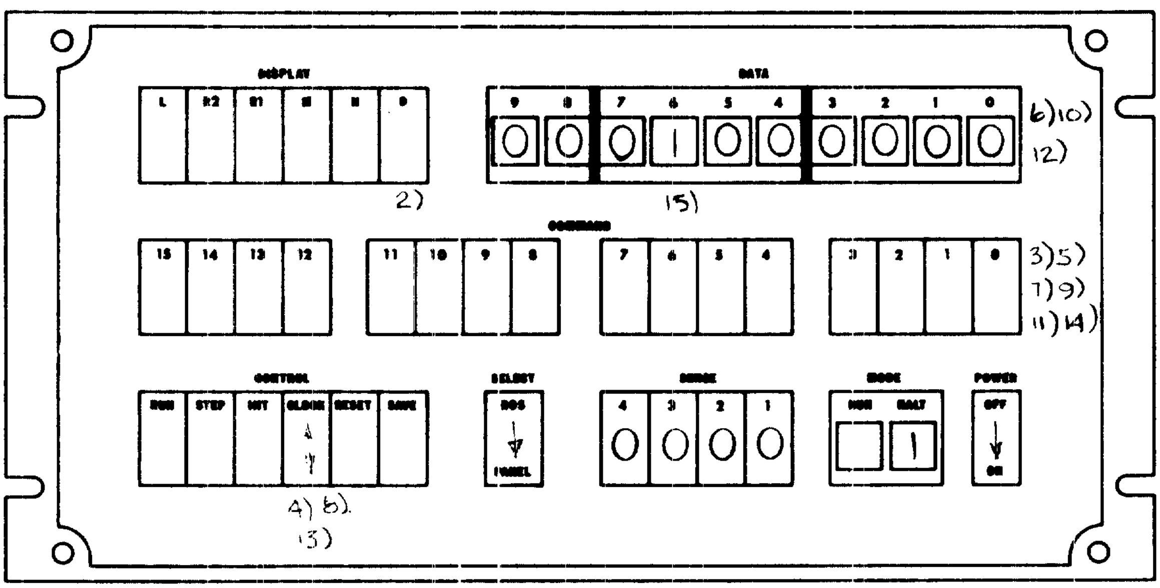


FIGURE 151 - SYSTEM CONTROL CONSOLE

4.17.31 <u>Performing Logical Operations</u>

4.17.32 <u>Copy (Mainly Used to Transfer The Contents of the "T" Register)</u>

C COPY

B	f	c	*	r
15				0

The selected operand is placed in the file register designated by f, if * is a 0-bit, and in the register designated by 4. The LINK is not affected. The c field controls selection of the operand, incrementing the operand, and modification of condition flags.

This command has been utilized in most of the covered procedures.

4.17.33 <u>AND</u>

N AND

E	f	c	*	r
15				0

The selected operand is logically ANDed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags.

1. DEPRESS the SELECT switch to the PANEL position (down).

2. DEPRESS the "D" display switch.

3. Enter $11FF_{16}$ on the COMMAND switches. (Load T with FF_{16}.)

4. DEPRESS CLOCK.

5. CHECK the contents of "T" by entering $B020_{16}$ on the COMMAND switches.

6. OBSERVE that all DATA lamps 0-7 are ON.

7. ENTER $21AA_{16}$ on the COMMAND switches. (Load File #1 with AA_{16}.)

8. DEPRESS CLOCK.

9. CHECK the contents of File #1 by entering $C100_{16}$ on the COMMAND switches.

10. OBSERVE that only DATA lamps #1, 3, 5, and 7 are ON (AA_{16}).

11. Enter $E123_{16}$ on the COMMAND switches. (The contents of "T" and File #1 are logically ANDED, results placed in File #1 and in the "N" register.)

12. DEPRESS CLOCK.

13. Check the contents of File #1 by entering $C100_{16}$ on the COMMAND switches.

14. Observe that only data lamps #1, 3, 5, and 7 are ON (AA_{16}).

15. DEPRESS the "N" DISPLAY switch.

16. OBSERVE that data is displayed the same as 14.

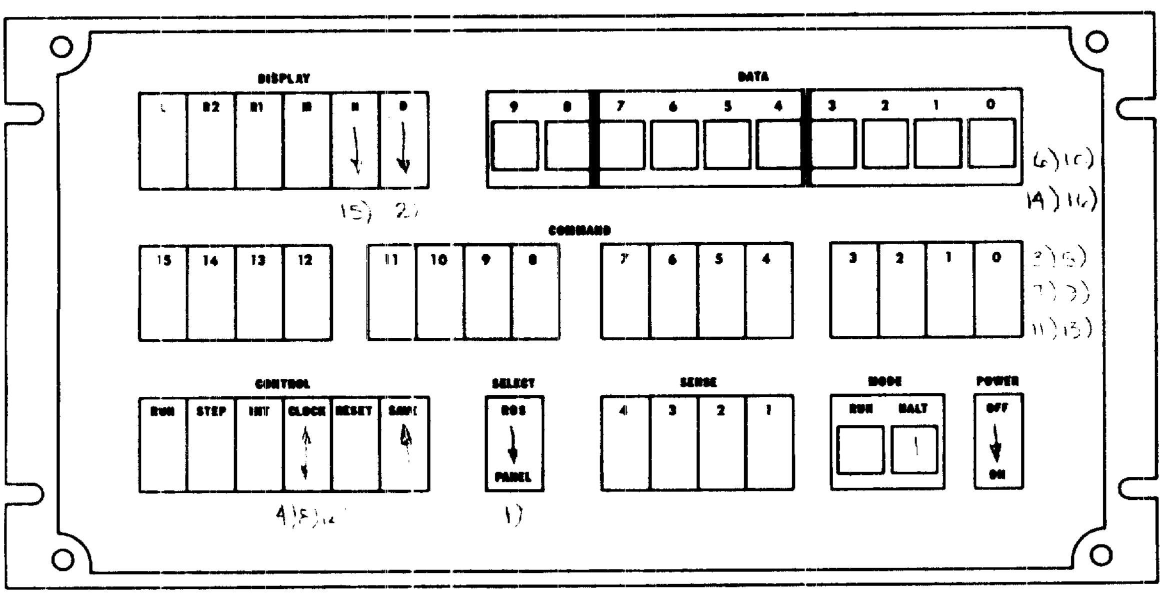


FIGURE 152 - SYSTEM CONTROL CONSOLE

4.17.34 OR

O OR

C	f	c	*	r

15 0

The selected operand is logically inclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags.

This command has been utilized by most of the covered procedures.

4.17.35 EXCLUSIVE OR

X EXCLUSIVE OR

D	f	c	*	r

15 0

The selected operand is logically exclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags.

1. DEPRESS the SELECT switch to PANEL position (down).

2. DEPRESS THE "D" display switch.

3. Enter 11AA$_{16}$ on the COMMAND switches. (Load "T" with AA$_{16}$.)

4. DEPRESS CLOCK.

5. CHECK the contents of "T" by entering $B020_{16}$ on the COMMAND switches.

6. OBSERVE that only DATA lamps 1, 3, 5, and 7 are ON (AA

7. Enter $21A5_{16}$ on the command switches. (Load file with $A5_{16}$) (down).

8. Check the contents of File #1 by entering C100 on the command switches.

9. OBSERVE that only DATA lamps 0, 2, 5 and 7 are on. (A

10. ENTER $D120_{16}$ on the command switches. (Logically EXCLUSIVE-OR the contents of "T" and File #1 and place results in File #1.

11. DEPRESS CLOCK.

12. CHECK the contents of File #1 by entering C100 in the command switches.

13. OBSERVE that only DATA lamps 0-3 are ON.

14. A5 was EXCLUSIVELY OR-ed with AA which resulted in a placement of

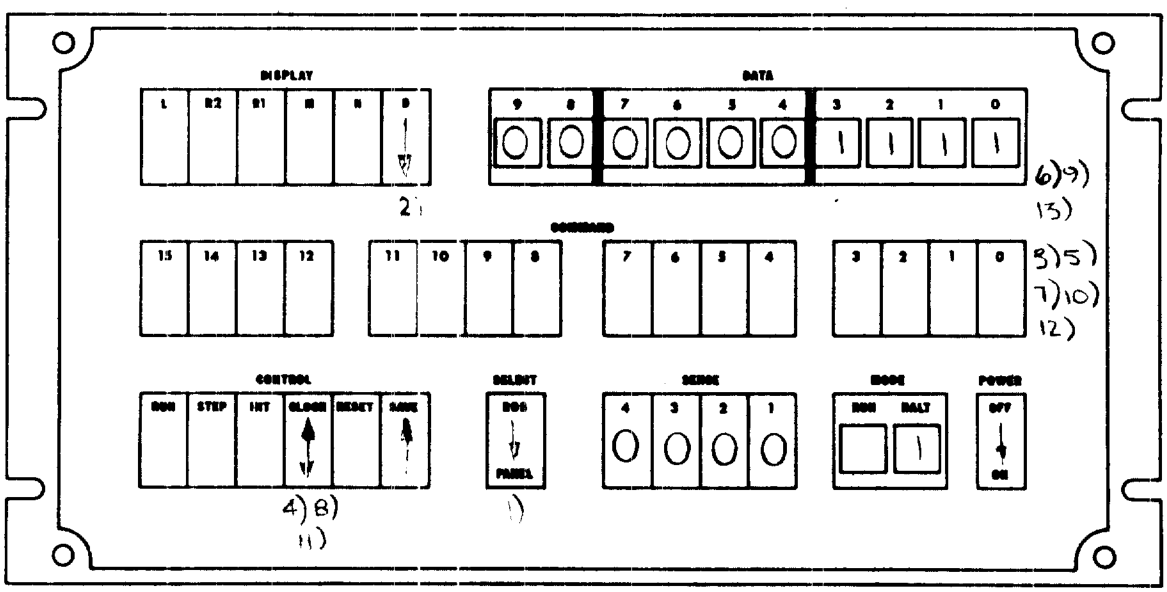


FIGURE 153 - SYSTEM CONTROL CONSOLE

4.17.36 SHIFT

H SHIFT

F	f	c	*	r

15 0

The contents of the file register designated by f is shifted left or right one bit position and placed in the file register, if * is a 0-bit, and in the register designated by 4. The high order or low order bit which is shifted off is placed in LINK and in the overflow flag if the modify condition flag is selected. The c field controls the direction of shift, entry of an end bit, and modification of the condition flags.

1. DEPRESS the SELECT switch to the PANEL position (down).

2. DEPRESS the "D" DISPLAY switch.

3. Enter 2101_{16} on the COMMAND switches. (Load File #1 with 01_{16}.)

4. DEPRESS CLOCK.

5. Check contents of File #1 by entering $C100_{16}$ on the command switches.

6. OBSERVE that only DATA lamp #0 is ON. (01_{16})

7. ENTER $F100_{16}$ on the data switches. (Shift the contents of File #1 left one bit position and place results in File #1.)

8. OBSERVE that only DATA lamp #1 is ON. The shift left process is active as soon as the command is decoded.

9. DEPRESS CLOCK.

10. OBSERVE the data lamps. Notice that Lamp #2 is now on and #1 is off.

11. DEPRESS the CLOCK switch until lamp #7 is on.

12. STOP.

13. DEPRESS COMMAND switch #5 (right shift).

14. DEPRESS CLOCK.

15. OBSERVE the BIT SHIFT RIGHT.

16. DEPRESS clock switch until lamp #1 is ON.

17. STOP.

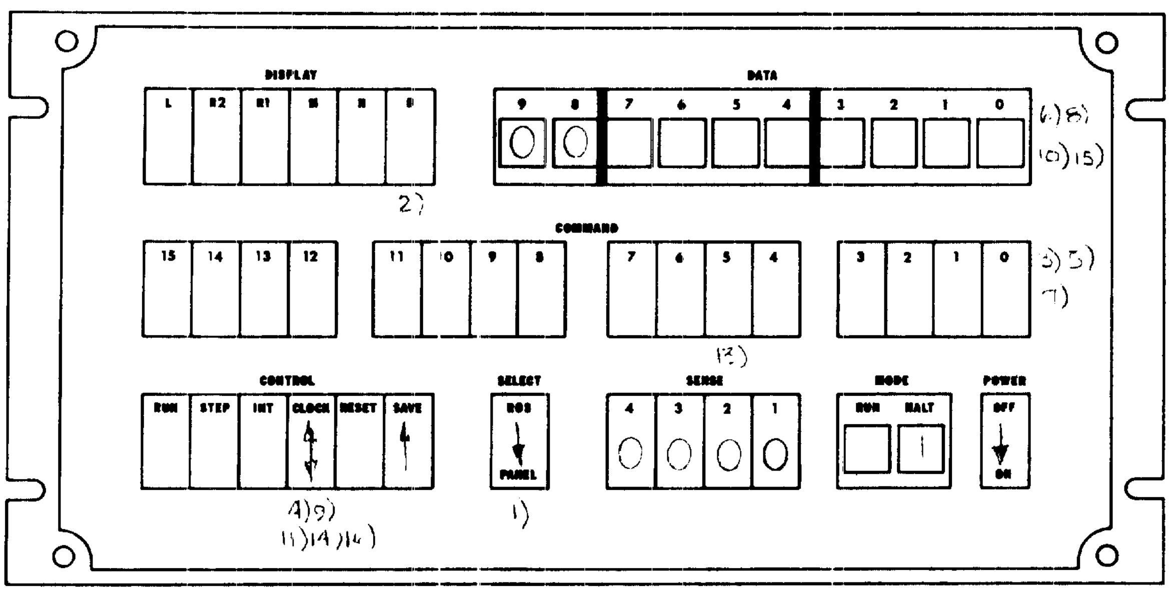


FIGURE 154 - SYSTEM CONTROL CONSOLE

4.17.37 Performing Memory Read/Write Operations

R READ MEMORY W WRITE MEMORY

A	f	c	*	r

15 0

The contents of the file register designated by f is unaltered, incremented, or decremented as controlled by the c field. The result is placed in the file register (f) if * is a 0-bit, and in the register designated by r. At the same time, a read (R) or write (W) memory operation is initiated as controlled by bit 4. If the operation is a memory read, the T register is cleared and the accessed data is set into the T register after two clock cycle times. Data to be written into memory must be placed in the T register before the write memory command, if the operation is a half cycle write, and by the first clock cycle time after the write memory command on a full cycle write. The condition flags and LINK are not affected. Execution of the memory command is delayed if the memory is in a busy condition from a previous R or W command or DMA operation.

The bits of the c field control the transfer of data from the file register and the type of memory operation.

4.17.38 WRITE into MEMORY (One Location)

1. DEPRESS the SELECT switch to the PANEL position (down).
2. DEPRESS the "D" DISPLAY switch.
3. Enter 1196_{16} on the COMMAND switches (Load 'T" with 96_{16}).
4. DEPRESS CLOCK.
5. Check the contents of "T" by entering $B020_{16}$ on the COMMAND switches.

6. OBSERVE that only DATA lamps #1, 2, 4, and 7 are ON (96_{16}).

7. ENTER 1300_{16} on the COMMAND switches. (Load "N" with 00_{16}).

8. DEPREWS CLOCK.

9. DEPRESS the "N" DISPLAY SWITCH.

10. OBSERVE that all DATA lamps are OFF.

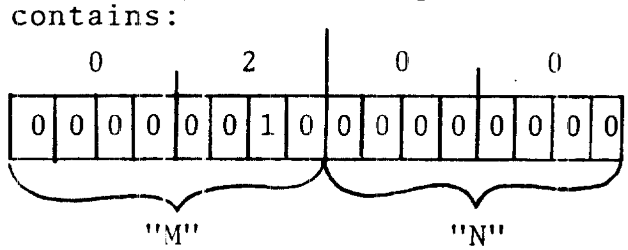
11. ENTER 1202 on the COMMAND switches. (Load "M" with 02_{16}.)

12. DEPRESS "M" display switch.

13. Observe that only data lamp #1 is ON (02_{16}).

<u>NOTE</u>

The memory address register now contains:



The data 96_{16} will be written into address 0200_{16}.

14. ENTER $A010_{16}$ on the COMMAND switches. (Memory full write of contents in the memory buffer ("T") register.)

15. DEPRESS CLOCK.

16. Data 96_{16} has been written into MEMORY.

17. To check this data, perform 4.1.6.13.2 READ from MEMORY (one location).

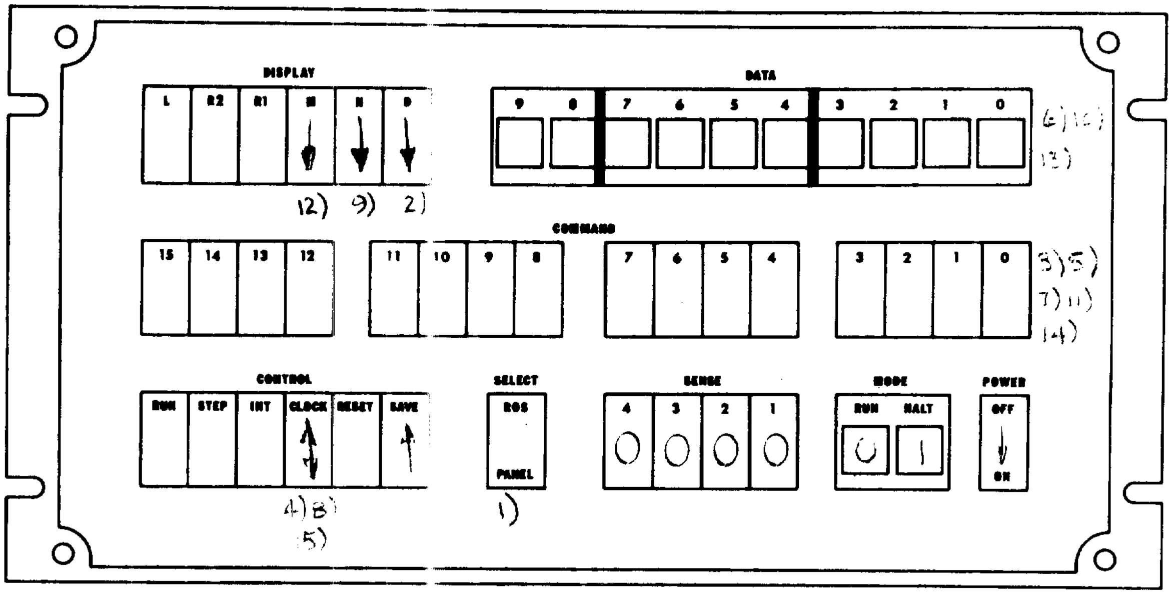


FIGURE 155 - SYSTEM CONTROL CONSOLE

4.17.39 READ from MEMORY (One Location)

1. DEPRESS the SELECT switch to the PANEL Position (down).

2. DEPRESS the "D" display switch.

3. Enter 1100_{16} on the COMMAND switches. (Load "T" with 00_{16} - Clear "T".)

4. DEPRESS CLOCK.

5. CHECK the contents of "T" by entering $B020_{16}$ on the COMMAND switches.

6. OBSERVE that all DATA lamps are OFF.

7. ENTER $A000_{16}$ on the COMMAND switches (full read).

8. DEPRESS CLOCK.

9. CHECK the contents of the "T" register by entering $B020_{16}$ on the command switches.

10. OBSERVE that only data lamps #1, 2, 4, and

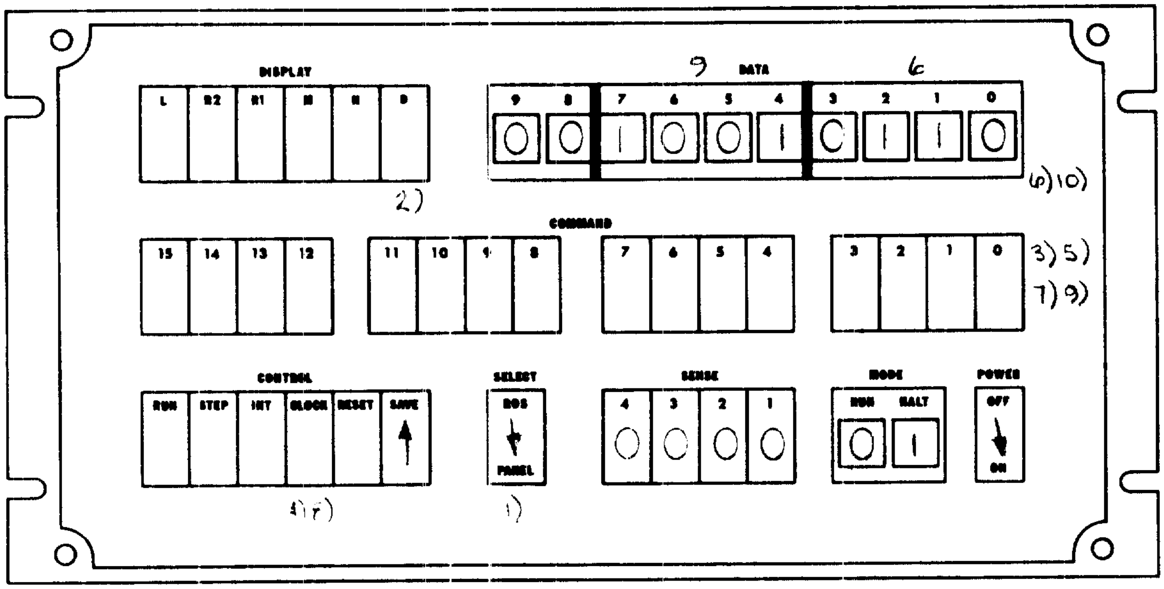


FIGURE 156 - SYSTEM CONTROL CONSOLE

4.17.40 WRITE into MEMORY (Successive Locations)

1. DEPRESS the SELECT switch to the PANEL Position (down).
2. DEPRESS the "D" DISPLAY switch.
3. ENTER $11A5_{16}$ on the COMMAND Switches. (Load "T" with $A5_{16}$.)
4. DEPRESS CLOCK.
5. Check the contents of "T" by entering $B020_{16}$ on the COMMAND switches.
6. OBSERVE that only DATA lamps #0, 2, 5, and 7 are ON ($A5_{16}$).
7. ENTER 1300_{16} on the COMMAND switches (load "N" with 00_{16}).
8. DEPRESS CLOCK.
9. DEPRESS the "N" Display switch.
10. OBSERVE that all DATA lamps are OFF.
11. ENTER 1200_{16} on the COMMAND switches (load "M" with 02_{16}).
12. DEPRESS CLOCK.
13. DEPRESS the "M" display switch.

14. OBSERVE that only data lamp #1 is ON (02_{16}).

15. ENTER 2100$_{16}$ on the COMMAND switches (load File #1 with 00_{16}).

16. CHECK the contents of File #1 by entering C100 on the COMMAND switches.

17. OBSERVE that all of the DATA lamps are OFF (00_{16}).

18. ENTER A113$_{16}$ on the COMMAND switches. (Full write into memory from the memory buffer register, contents of File #1 (transferred to "N".)

19. DEPRESS CLOCK.

20. DEPRESS COMMAND switch 6.

21. DEPRESS COMMAND switch 7.

22. DEPRESS the "N" display switch.

23. DEPRESS CLOCK.

24. OBSERVE the DATA lamps. Each time the CLOCK switch is depressed the "N" register is incremented.

NOTE

Actually, the file register #1 is incremented and each time the count is transferred to the "N" register.

25. DEPRESS the CLOCK switch approximately 10 times.

26. OBSERVE the DATA lamps as the "N" register count is incremented.

27. STOP.

28. If you wish to read from memory the data just entered go to the next step.

4.17.41 READ from MEMORY

1. DEPRESS the SELECT switch to the panel position (down).
2. DEPRESS the "D" display switch.
3. ENTER 1100_{16} on the COMMAND switches (load "T" - Clear "T" with 00_{16}.)
4. DEPRESS clock.
5. CHECK the contents of "T" by entering $B020_{16}$ in the command switches.
6. OBSERVE that ALL DATA lamps are OFF.
7. ENTER 1300_{16} in the COMMAND switches. (Load "N" with 00_{16}.)
8. DEPRESS CLOCK.
9. DEPRESS "N" DISPLAY switch.
10. OBSERVE that all DATA lamps are OFF.
11. Enter 1202_{16} on the COMMAND switches.
12. DEPRESS CLOCK.
13. DEPRESS the "M" DISPLAY switch.
14. OBSERVE that ONLY DATA lamp #1 is ON.
15. ENTER 2100_{16} into the COMMAND switches. (Load File #1 with 00_{16}.)
16. DEPRESS CLOCK.
17. CHECK the contents of File #1 by entering $C100_{16}$ on the COMMAND switches.
18. DEPRESS the "D" DISPLAY switch.
19. OBSERVE that ALL DATA lamps are OFF.
20. ENTER A103 in command switches memory read (file)
21. DEPRESS CLOCK.

22. DEPRESS "N" display switch.

23. OBSERVE that ALL DATA lamps are OFF.

24. CHECK the contents of "T" by entering $B020_{16}$ on the command switches.

25. DEPRESS the "D" display switch.

26. OBSERVE that only data Lamps #0, 2, 5, and 7 are ON.

NOTE

You have just read information stored in core memory at location 0200_{16}. The next steps will allow you to increment the address and read from any desired location.

27. ENTER A1C3 on the COMMAND switches. (Full read, increment word, transfer count to "N" register.)

28. DEPRESS the "N" DISPLAY switch.

29. DEPRESS CLOCK.

30. OBSERVE that only DATA lamp #0 is ON.

31. DEPRESS CLOCK successively 5 times and OBSERVE that the "N" register is incremented.

32. ADVANCE the count to a value of 0_{16} (Only data lamps "0" and "3" ON.)

NOTE

In procedure 4.17.39, approximately 12 to 15 locations were written into with a known bit pattern. If you should go beyond a value of 9_{16} in step (32) above you should still have the desired results. If not, start in with write procedure again (4.17.39).

33. CHECK the contents of "T" by entering $B020_{16}$ on the COMMAND switches.

34. DEPRESS the "D" Display switch.

35. OBSERVE that ONLY data lamps #0, 2, 5, and 7 are ON.

4.17.42 Application of System Control Console Operation to System Logic Fault Location

1. By use of the ROS diagnostic, the board fault can most usually be identified. The accompanied machine listing will indicate major area of the fault.

2. Manual operation by use of the system control console can step you through the logic. By exercising different commands, sections of each logic function can be eliminated until you have the bad component isolated.

3. A further check would be to use an oscilloscope and observe the logic levels at the suspected gate or flip-flop, etc. Failure of the logic function would normally indicate that the component requires replacement.

5.1 Expansion Cabinet

The basic computer cabinet provides for expansion of the system to certain limits. When a configuration exceeds space available within the basic enclosure, the standard expansion cabinet can be used for additional memory and/or input/output interfaces.

A drawing of the interconnected computer and expansion cabinets is shown in Figure 159. Memory and I/O are expanded independently by separate connector boards and cables. Figure 160 shows the connector assignments for memory and I/O boards in each cabinet.

5.2 Expansion Cabinet Components

The expansion cabinet consists of the following components (excluding plug-in memory and I/O boards):

I/O Bus Transmitter and Receiver Board
Memory Expander Board
I/O Terminator Board
Memory Terminator Board
Expansion Cabinet and Backplane
Power Supply

5.3 General

1. The expansion chassis comes in three possible configurations.

    a. I/O expansion
    b. Memory expansion
    c. I/O and Memory expansions

2. The unit consists of a Chassis, Power Supply, Modified Backplane, I/O Expander, or Memory Expander or both.

3. The Expansion Chassis does not have the capability for a DMA board.

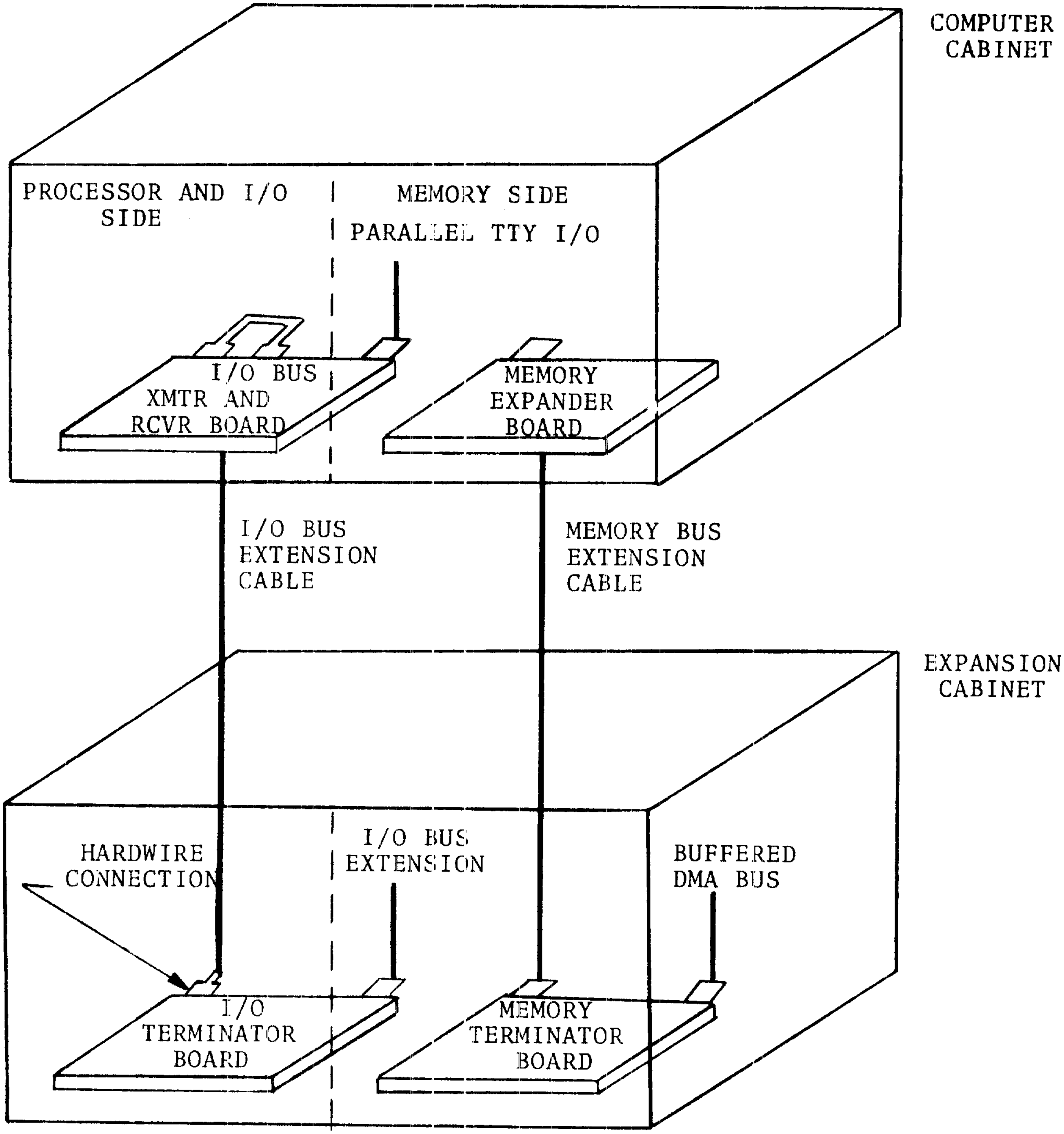


FIGURE 159

COMPUTER EXPANSION
(Front View)

5.4 Configuration

1. Figure 160 shows the configuration of the expansion chassis with no DMA installed in the main frame.

   a. The memory extension board goes in J9.
   b. The I/O extension board goes in J14.
   c. The memory expander goes in J9 of the main frame.
   d. The backplane assembly does require a modification.

      i. J2-A21 jumpered to J2-A17
      ii. J4-A21 jumpered to J4-A17
      iii. J6-B21 jumpered to J6-A17
      iv. J8-B21 jumpered to J8-A17

   e. The system, including the main frame is capable of driving 32K of core and 10 I/O controllers.

5.5 Preliminary Test Procedure - Expansion Chassis

2. Figure 161 shows the configuration of the chassis with one DMA installed in the main frame.

   a. In the main frame, the memory expander goes in J9 and the DMA in J7.
   b. The memory and I/O extensions remain the same in the expansion chassis. J9 and J14 respectively.
   c. Since the DMA goes in J7 of the main frame, the system now reduces to 28K of Core.
   d. The fourth memory now goes in J7 and J8 of the expansion chassis. Refer to figure 161 for proper addressing.
   e. The backplane modification.

      i. J2-A21 jumpered to J2-A17
      ii. J4-A21 jumpered to J4-A17
      iii. J6-B21 jumpered to J6-A17
      iv. J8-B21 jumpered to J8-B17

3. Figure 162 shows the configuration of the chassis with two DMA's installed in the main frame.

   a. In the main frame, the memory expander goes in J9 and the DMA's in J7 and J5.
   b. The system reduces to 24K of core.
   c. Refer to figure 3 for proper addressing
   d. The backplane modification.

      i. J2-A21 jumpered to J2-A17
      ii. J4-A21 jumpered to J4-A17
      iii. J6-B21 jumpered to J6-B17
      iv. J8-B21 jumpered to J8-B17

   e. Power

5.6 Power

The relay, located on the front of the expansion chassis, is controlled by the -16V on the computer. When properly connected, the power switch on the computer will control both supplies.

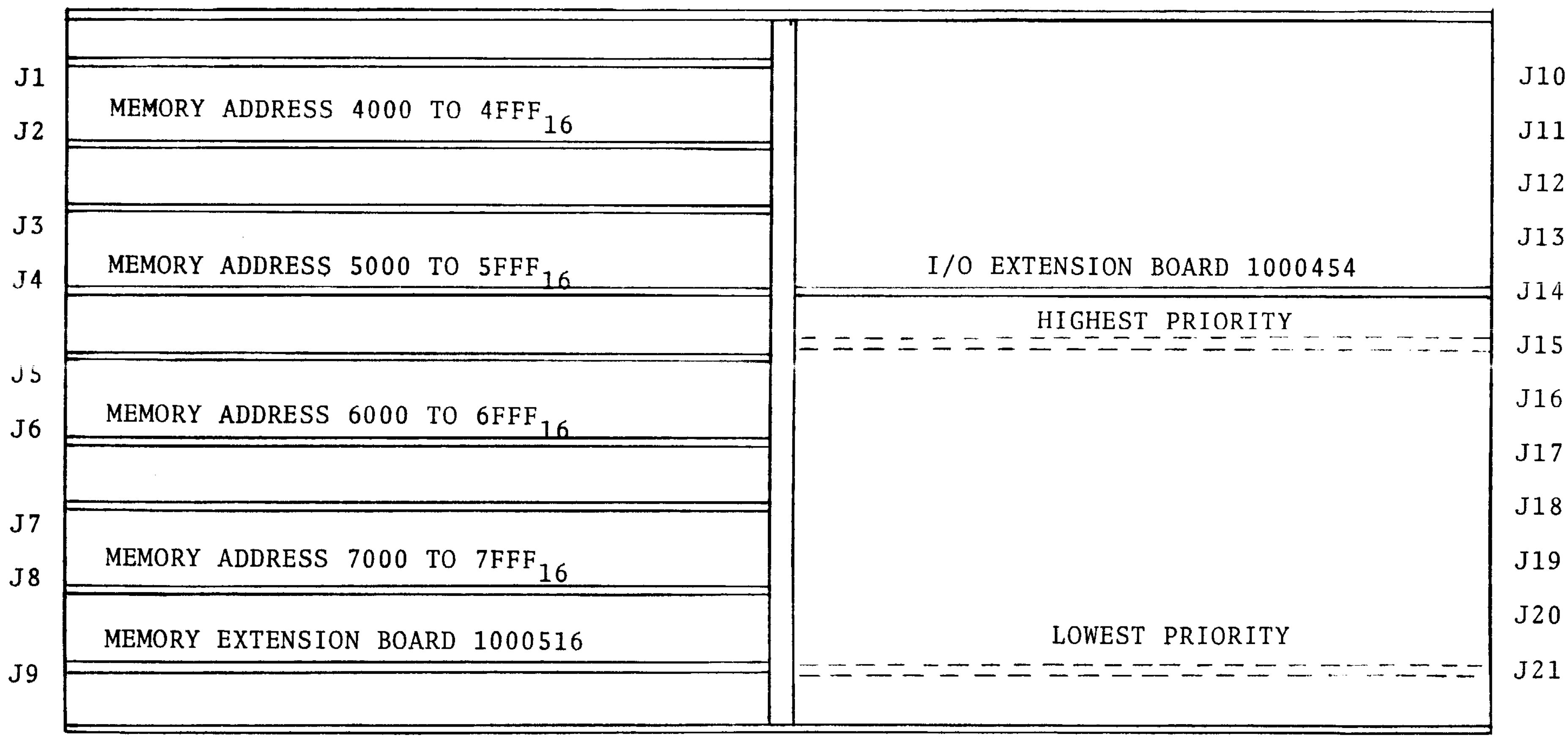


FIGURE 160

EXPANSION CHASSIS WITH NO DMA

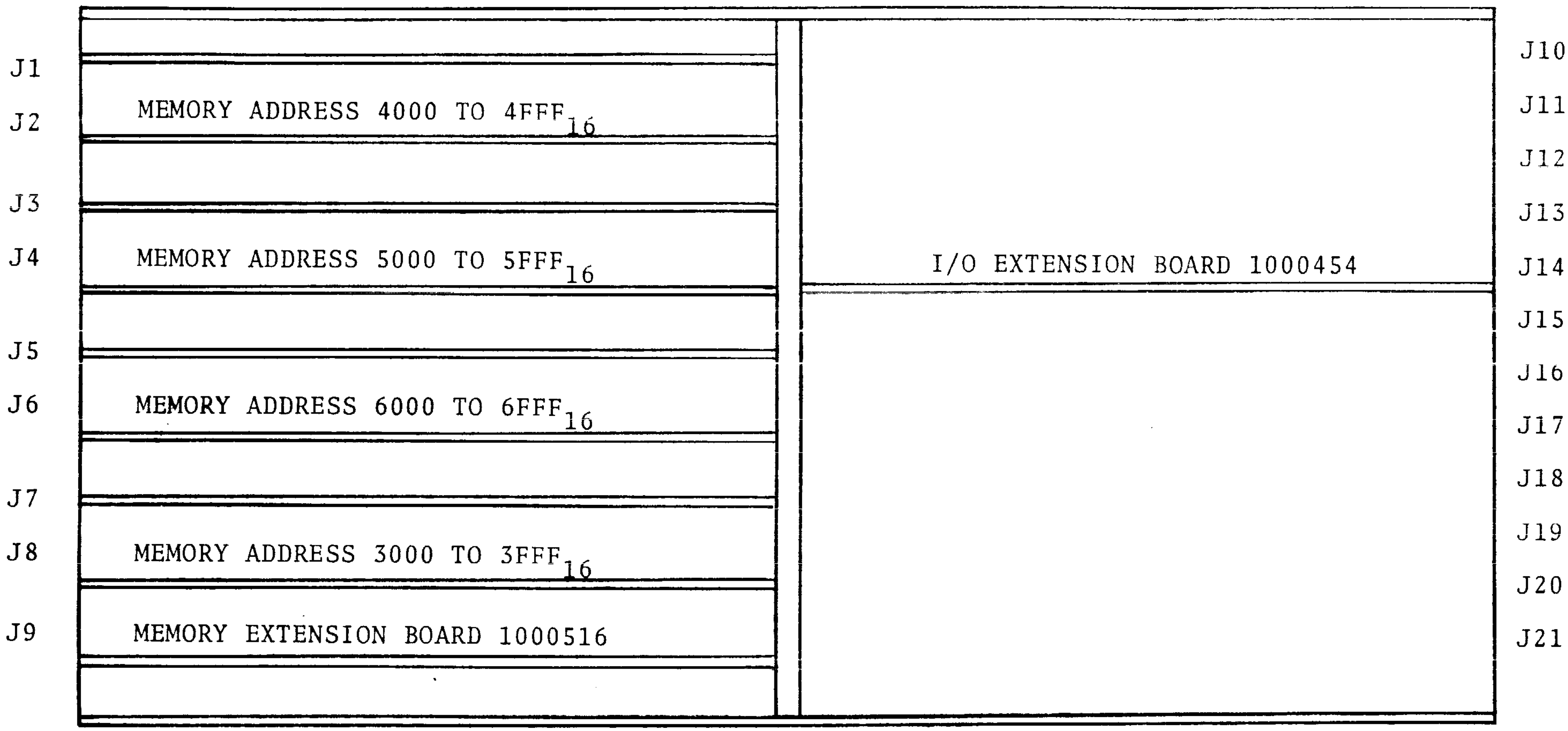


FIGURE 161

EXPANSION CHASSIS WITH ONE DMA

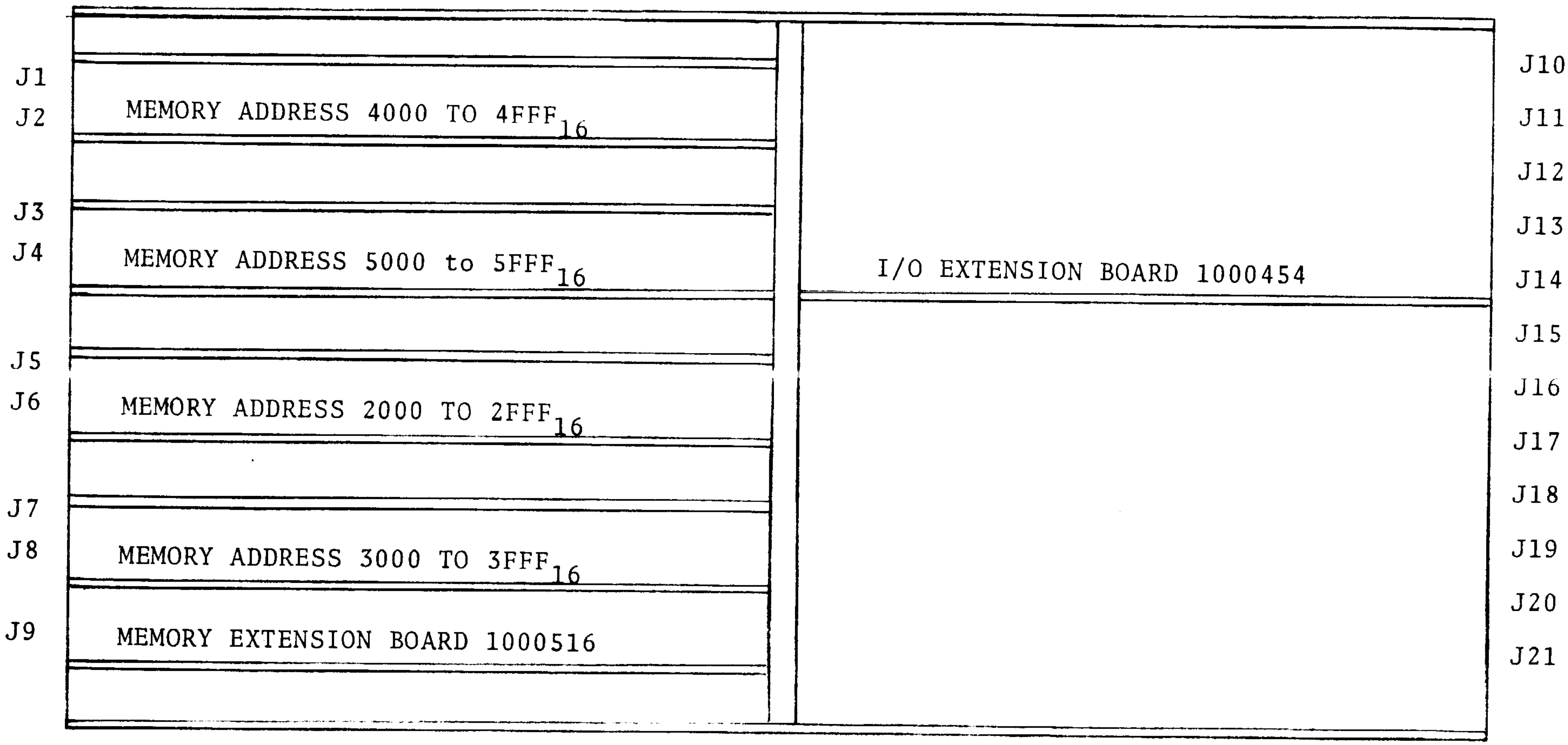


FIGURE 162

EXPANSION CHASSIS WITH TWO DMA

5.7 PARTS LIST AND COMPONENT LOCATION CHARTS

General

The parts list and component charts are provided in this manual for aiding the maintenance technician in location and identification of suspected bad components.

Parts Location

Each board is laid out on a matrix for location of components. In the example as shown in Figure the component Z37 is located at the intersection of 4 in the vertical direction and E in the horizontal direction. This component would be listed on the

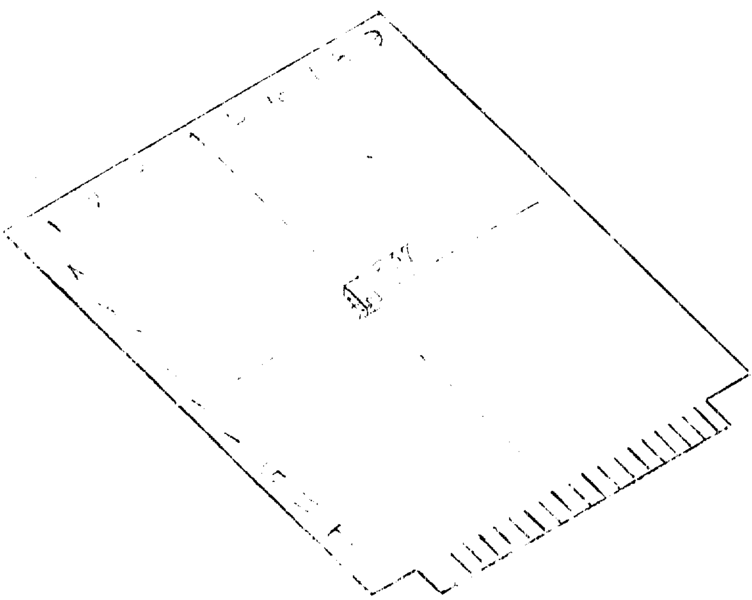


FIGURE 163

parts list as being located at matrix location E4 or Z reference location Z37, either method will locate the component. The user need only to look either of these directions up on the parts list and the list will give the component part number and the manufacturer.

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CONTROL BOARD PARTS LIST (ASSEMBLY PART NUMBER) 1000775 Ref. Fig.164

ITEM #	QTY	DESCRIPTION	PART NUMBER	MATRIX LOCATION	Z REF LOCATION	VENDOR
* 1	7	Integrated, Hex inv	U6A901659X SN74H04J	A6,B2,B9,D7,F1 G9,J1	Z6,11,18,34,45, 62,72	FAIRCHILD TI
* 2	16	,2 in nand	U6A900259X SN74H00J	A5,A9,B7,B8,C1,D1 D8,F9,G7,G8,H1, G8,H7,H8,J2	Z5,9,16,17,19,28, 35,53,60,59,61,63 61,69,70,73	FAIRCHILD TI
* 3	7	,3 in nand	U6A90035X SN74H10J	A2,B3,B5,C2,C9 E7,H2	Z2,12,14,20,27 42,64	FAIRCHILD TI
* 4	10	,4 in nand	U6A900459X SN74H20J	A1,A3,C3,C4,C8 F7,G2,H6,J7	Z1,3,21,22,23,26 51,55,68,76	FAIRCHILD TI
* 5	5	,Dur nand	U6A900959X SN74H40J	H9,J5,J6,J8,J9	Z71,74,75,77,78	FAIRCHILD TI
* 6	10	,2-2 And/ or inv	U6A900559X SN74H51J	C6,C7,D5,D6,C8 E4,F3,F4,G1,G3	Z24,25,32,33,26, 39,47,48,54,56	FAIRCHILD TI
* 7	6	,2-2-2-3 and/or inv	U6A900859X SN74H54J	A4,B1,B4,D2,E3,E9	Z4,10,13,29,38,44	FAIRCHILD TI
8	13	SKFF	U6B902259X	A7,AB,D3,D4,E2,E5 F5,E6,EB,F6,F8, G5	Z7,8,30,31,37,49 40,41,43,46,50,52 58	
9	1	Dual Quad Latch	U6N930859X	H4	Z66	
10	2	Decoder	U6B930159X	B6	Z15	
11	2	Quad 2 in nand open collector	SN7401N	G4,H3	Z57,65	TI
12	1	Oscillator Xtal	HBZ-oz (4.55 MHZ)	D9	Y1	BLILEY
13	1	Capacitor 478F	DM15-470J	D8	C4	ELMENCO
14	1	Capacitor 10PF	DM15-1005	J9	C5	ELMENCO
15	1	Capacitor 22PF	DM15-220J	J9	C5	ELMENCO
16	2	Capacitor 100PF 5%	CYFM10C101J	A8,A9	C1,C2	CORNING
17	1	Capacitor 100PF	DM15-101J	B9	C3	ELMENCO
18	14	Capacitor 22MF 15VDC	K22E75	Buss +5V	C6 Thav C19	KEMET
19	1	Capacitor 22MF 25VDC	K22E25	A6	C20	KEMET
20	4	Diode	FDH600	A6,A7,A8	CR1 thru CR4	FAIRCHILD
21	5	Transistor (T0-18)	2N2369A	A7,A6,A9,A8,H7	Q1 thru Q5	FAIRCHILD
22	2	Potentiometer	3260 W-1-102	A6,A8	R26 and R28	BOURNS
23	5	Transistor Pad	100-000			DELBERT BLINN
24	9	Resistor 1K 1/4w5%	RC07GF102J	A6,A6,B9,A9,B8,H7 A7,A7	R1,3,6,8,10,13,22, 2,9,5	
25	3	Resistor 1.5k 1/4w5%	RC07GF152J	B9,J9,B8	R11,25,32	
26	10	Resistor 470-56 1/4 w 5%	RC076F471J	C9,J8	R12,24,14 thru 21	
27	1	Resistor 220 1/4w5%	RC07GF221J	H7	R23	
28	2	Resistor 4.02K1/8w5%	RN55D (type)	A9,A8	R9 and R4	CORNING GLASS
29	1	Resistor 3.3K1/4w5%	RC07GF332J	D9	R30	
30	2	Choke 22 MH	70F225A1	C9,J9	L1 and L2	MILLER

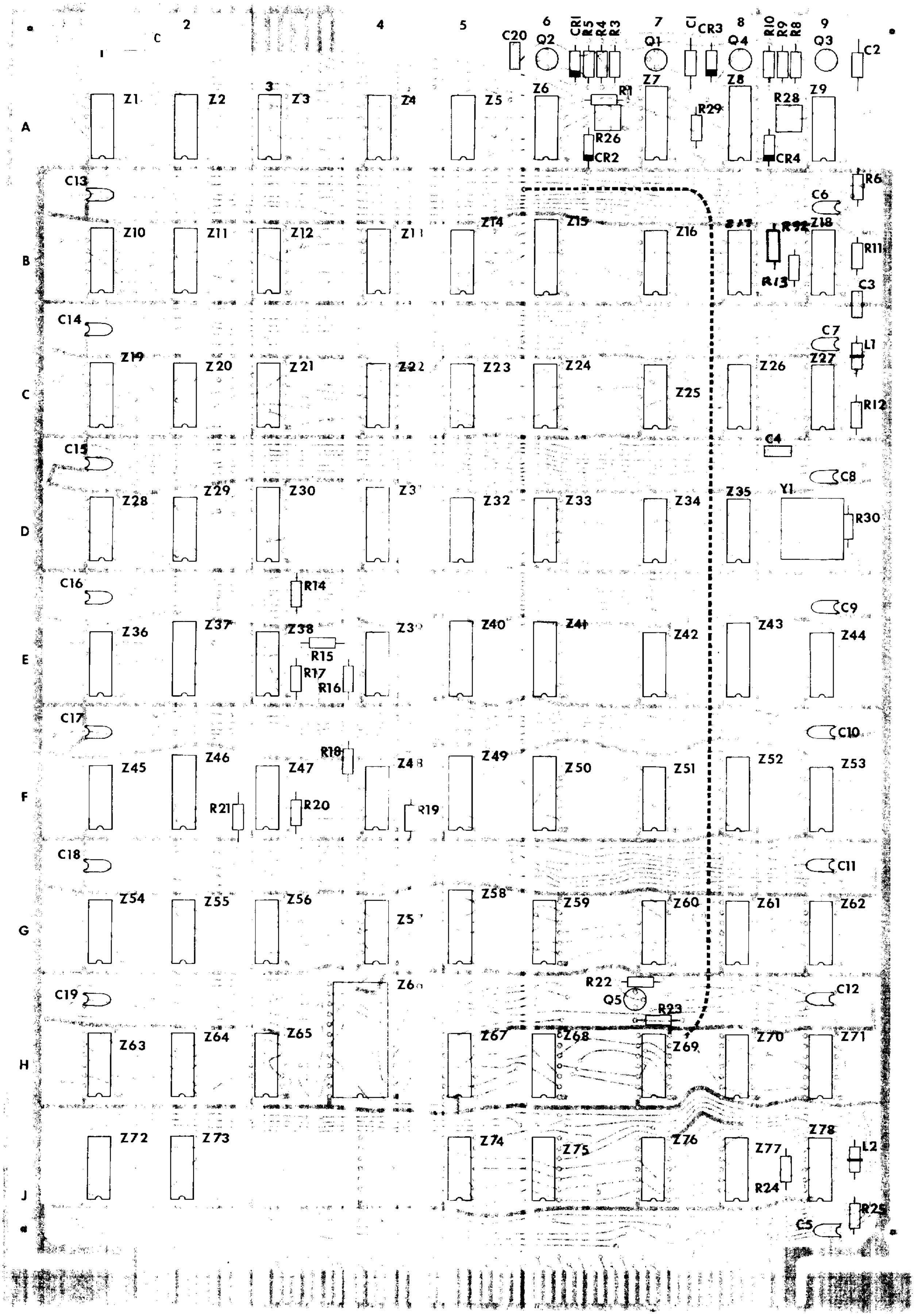


FIGURE 165
5-11

DATA BOARD PARTS LIST (ASSEMBLY PART NUMBER 1000774 Ref. Figure 166

ITEM #	QTY	DESCRIPTION	PART NUMBER	MATRIX LOCATION	Z REF LOCATION	VENDOR
1	6	Integrated-JKFF	U6B902259X	E9,C9,A7,C4,G9,C10 D10	Z19,20,46,47,52, 53	FAIRCHILD
* 2	4	,Hex inv.	U6A901659X SN74H04J	A6,D7,C3,B10 SN74H04J	Z14,25,38,51	
* 3	11	,2-2 and/or inv	U6A900559X SN74H51J	F4,E4,D4,C4,B4,B6, F6,D2,A2,A8,A9	Z1,2,3,4,15,16,29, 32,34,48,49	
* 4	5	,2 in nand	U6A900259X SN74H005	A5,B8,B9,E1,E10	Z17,45,50,58,59	
5	1	, Dual Quad Latch	U6N930859X	H10	Z54	
6	2	, Dual Adder	U6B930459X	G6,G7	Z27,28	
7	4	, 16 bit memory	U6A903359X	F5,E5,D5,C5	Z9,10,11,12	
8	4	, Power Nand	U6A900959X	G5,F1,G4,G3	Z5,6,7,8	
* 9	12	2-2-2-3 and/or inv	U6A900859X SN74H54J	C7,B7,C8,D8,C1 B1,D3,B3,A1,A3,D1, E3	Z21,22,23,24,33, 35,36,37,41,42,43 44	
*10	1	,4 in nand	U6A900459X SN74H20J	F3	Z40	
11	7	,3 in nand	SN7401N	A4,D9,E7,C2,G9 G10,F10	Z13,18,31,39,55, 56,57	TEXAS INSTRUMENTS
12	5	Resistor 1/4w±5%	RC07GF301J	C6,C7,C7,G8,C8	R6,12,14,16,18	
13	5	Resistor 300 1/4w ±5%	RC07GF301J	C6,C7,C7,G8,C8	R6,12,14,16,18	
14	2	Resistor,470 1/4w ±5%	RC07GF471J	C6,C6	R24,R26	
15	8	Resistor,1K, 1/4w±5%	RC07GF102J	E8,E8,D8,D8,B1,B1,C2 C2	R7,8,9,10,19,21,22 27	
16	4	Resistor,820 1/4w ±5%	RC07GF821J	G10,G10,G10,G10	R29,30,31,32	
17	8	Resistor,680 , 1/4w ±5%	RC07GF681J	H9,H9,H9,H9,H10,H10 H10,H10	R33,34,35,36,37,38, 39,40	
18	5	Resistor,33 , 1/4w ±5%	RC07GF330J	B1,C2,C6,C2,B1	R20,23,25,28,41	
19	5	Transistor(t0-18)	2N2369A	B2,B7,B2,C6,B2	Q1 thru Q5	
20	10	Capacitor,22MF,15 VDC	K22E15	C1 and B1,B10,C1,C10 D1,D10,E1,E10	C1 thru C10	CORMET
21	1	Resistor,2K,1/4w ±5%	RC07GF202J	H3	R42	
22	5	Transistor Pad	100-000			DELBERT BLINN
23	8	330 1/4w ±5%	RC07GF331J	C5,C5,C6,C6,E6,E6,E6, E6	R1,2,3,4,43,44,45 46	

* These components are used on the data board assembly part number 1000774

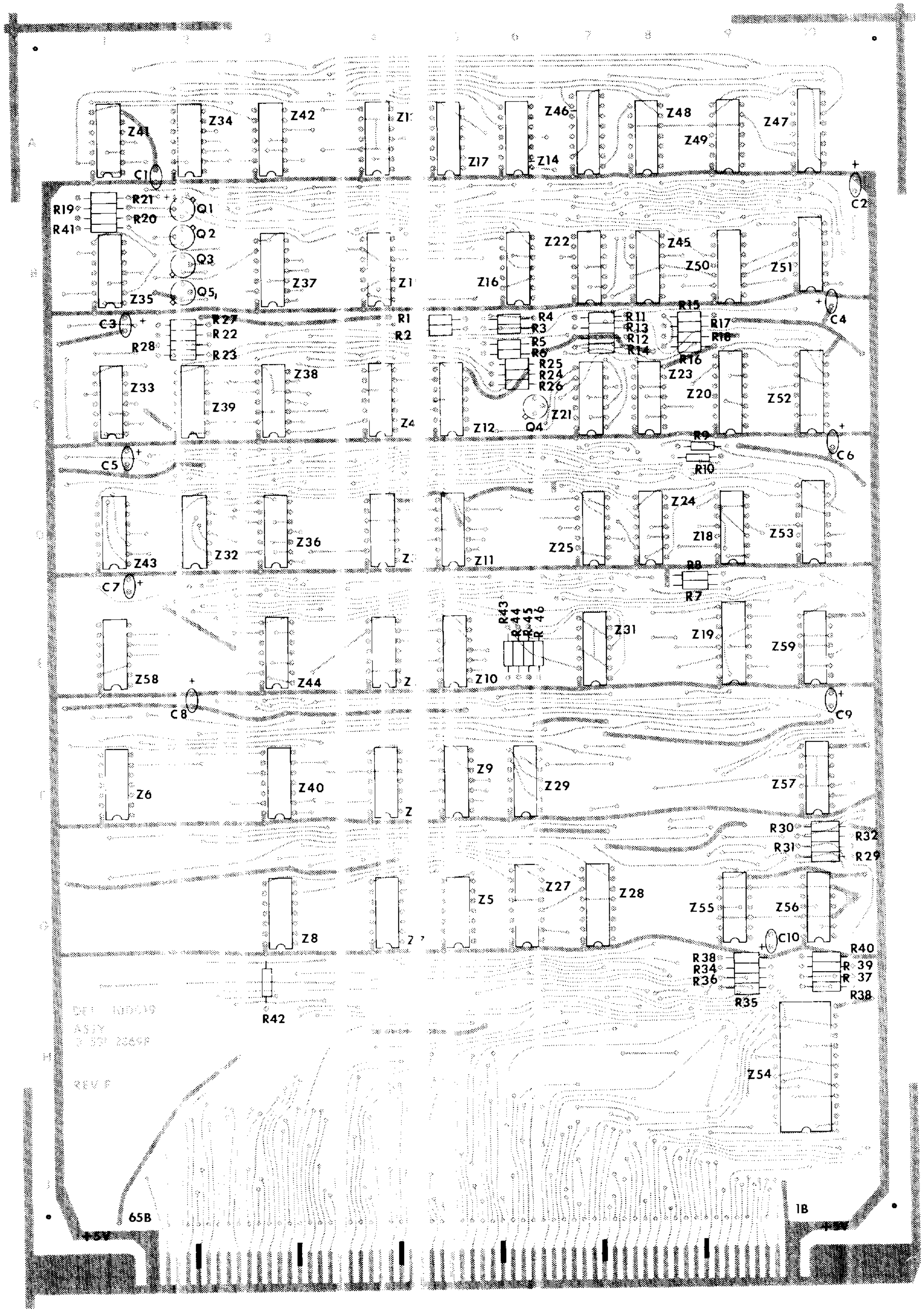

Z41
Z34
Z42
Z46
Z48
Z47
Z49
Z17
Z14
C1
C2
R19
R21
R20
R41
Q1
Q2
Q3
Q5
Z35
Z37
Z16
Z22
Z45
Z50
Z51
C3
R27
R22
R23
R28
R1
R2
R4
R3
R5
R6
R25
R24
R26
R11
R13
R12
R14
R15
R17
R18
R16
C4
Z33
Z39
Z38
Z4
Z12
Q4
Z21
Z23
Z20
Z52
C5
R9
R10
C6
Z24
Z36
Z43
Z32
Z11
Z25
Z18
Z53
C7
R8
R7
R43
R44
R45
R46
Z31
Z19
Z59
Z58
Z44
Z10
C8
C9
Z9
Z6
Z40
Z29
Z57
R30
R32
R31
R29
Z27
Z28
Z5
Z55
Z56
Z8
C10
R38
R34
R36
R35
R40
R39
R37
R42
Z54
65B
+5V
1B

FIGURE 167

READ ONLY MEMORY BOARD PARTS LIST (ALL ROM BOARDS) Figure 168

ITEM	QTY	PART NUMBER	DESCRIPTION	Z REFERENCE LOCATION	VENDOR
1	2	U6B930159X	Integrated, Decoder	Z4,Z5	FAIRCHILD
2	1	U6A900359X	,Triple ,3-in nand	Z1	
3	2	U6A900559X	.Dual 2-2 and/or inv	Z2,Z3	
4	20	2N2906	Transistor	Q2,Q4,Q6,Q8,Q10,Q11,Q12 Q13,Q14,Q15,Q16,Q17,Q18,Q20 Q22,Q24,Q26,Q28,Q30,Q32	
5	109	2N2369A	Transistor	Q1,Q3,Q5,Q7,Q9,Q19,Q21,Q23 Q25,Q27,Q29,Q31,Q33 thru 129	FAIRCHILD
6	6	K22E15	Capacitor 22uF15VDC	C1 thru C6	KEMET
7	20	RC07GF680J	Resistor 68 1/4w5%	R8,12,16,20,23,25,27,29,31,33, 35,37,42,46,50,54,58,62,66, 70	OHMITE
8	4	RC07GF101J	100	R6,10,14,18	
9	2	RC07GF331J	330	R1,2	
10	164	RC07GF471J	470	R7,11,15,19,40,41,44,45,48,49, 52,53,56,57,60,61,64,65,68, 69,71 thru 102,104,106,108, 110,112,114,116,118 thru 150,152 154,156,158,160,162,164,166 thru 230	
11	1	RC07GF681J	680	R4	
12	16	RC07GF102J	1K 1/4w 5%	R103,R105,107,109,111,113,115,117, 151,153,155,157,159,161,163,165	
13	4	RC20GF101J	Resistor 100 1/2w 5%	R5,9,13,17	
14	2	RC20GF121J	Resistor 120 1/2w 5%	R21,38	
15	1	RC32GF470J	Resistor 47 1w 5%	R3	OHMITE
16	132	FDH-600	Diode	CR1 thru CR132	FAIRCHILD
17	129	100-000	Transistor Pad		DELBERT BLINN
18	up to 4096	FDH-600	Diode	Map Diodes	FAIRCHILD

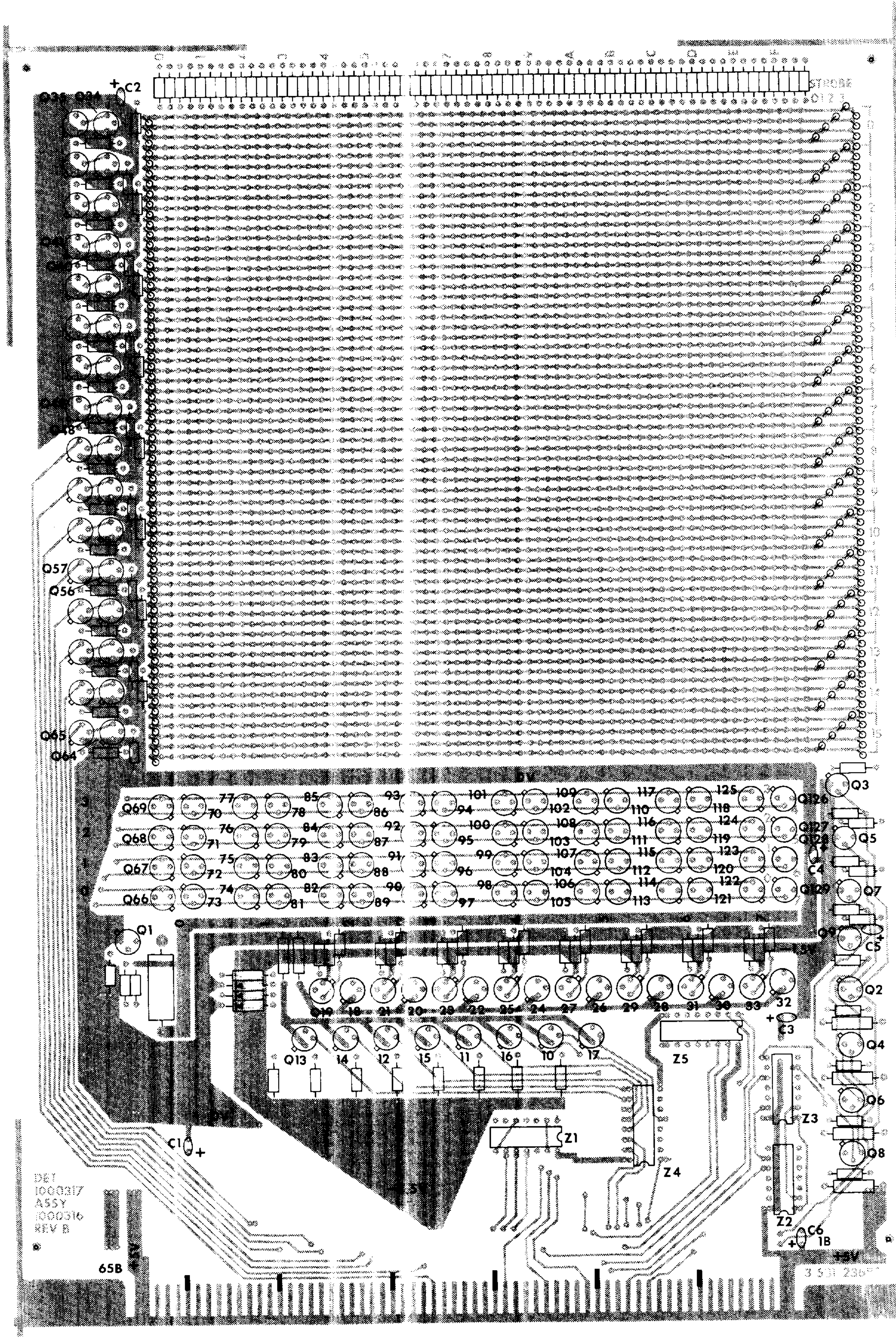

DET 1000317
ASSY 1000316
REV B
65B
+5V
STROBE
C1
C2
C3
C4
C5
C6
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q13
Q57
Q56
Q65
Q64
Q66
Q67
Q68
Q69
Z1
Z2
Z3
Z4
Z5

FIGURE 169

MEMORY SENSE INHIBIT ASSEMBLY P/N 1000563 (4 BIT) Figure 170

ITEM	QTY	PART NUMBER	DESCRIPTION	Z REF. DESTINATION	MATRIX LOC. N/A	VENDOR
1	4	U6A900259X	Integrated, 2 in nand	Z1,3,4,6		FAIRCHILD
2	2	SN7401N	Integrated Circuit	Z2,5		T.I.
3	4	TDC 2711	Integrated [1]	Z7-10		TRANSITRON
4	4	RC42GF131J	Res.130 2w 5%	R41, thru R44		OHMITE
5	4	RC20GF390J	39 1/2w 5%	R26 thru 29		OHMITE
6	13	RC07GF471J	470 1/4w 5%	R21 thru R24, R31 thru R34, R46 thru R49, R56		
7	8	RN55D(type)	15 1/8 1%	R6 thru R13		
8	8	RN55D(type)	10K,1/8w 1%	R1 thru R4, R16 thru R19		
9	4	RC07GF101J	100 1/2w 5%	R51 thru R54		OHMITE
10	3	RC07GF102J	1K,1/4w 5%	R58,59,61		
11	1	RC07GF151J	150 1/4w 5%	R60		
12	1	RC06GF150J	Res. 15 1/4w 5%	R57		
13	5	K22E25	Cap. 22MFD,25VDC	C6 thru C9,C14		KEMET
14	1	DM10-101J	Cap. 100PF	C11		ARCO-ELMENCO
15	5	2N2906	Transistor T0-18	Q1 thru Q4,Q16		FAIRCHILD
16	4	2N3725	Transistor T0-5	Q6 thru Q9		
17	4	2N2369A	Transistor T0-18	Q11 thru Q14		
18	2	K22E15	Cap. 22MFD 15VDC	C12,C15		KEMET
19	2	K065K103K	Cap. .01MFD, 200V	C13,C16		KEMET
20	4	TXBF-032-025B	Heat Sink			IERC
21	1	1000564	Detail Sense Inhibit Bd.			MSI
22	9	100-000	Transistor Pad T0-18			DELBERT BLINN
23	4	10076	Transistor Pad T0-5			MILTON ROSS

[1] Alternate part may be used in lieu of item 3 as follows: U5F771139X - Fairchild

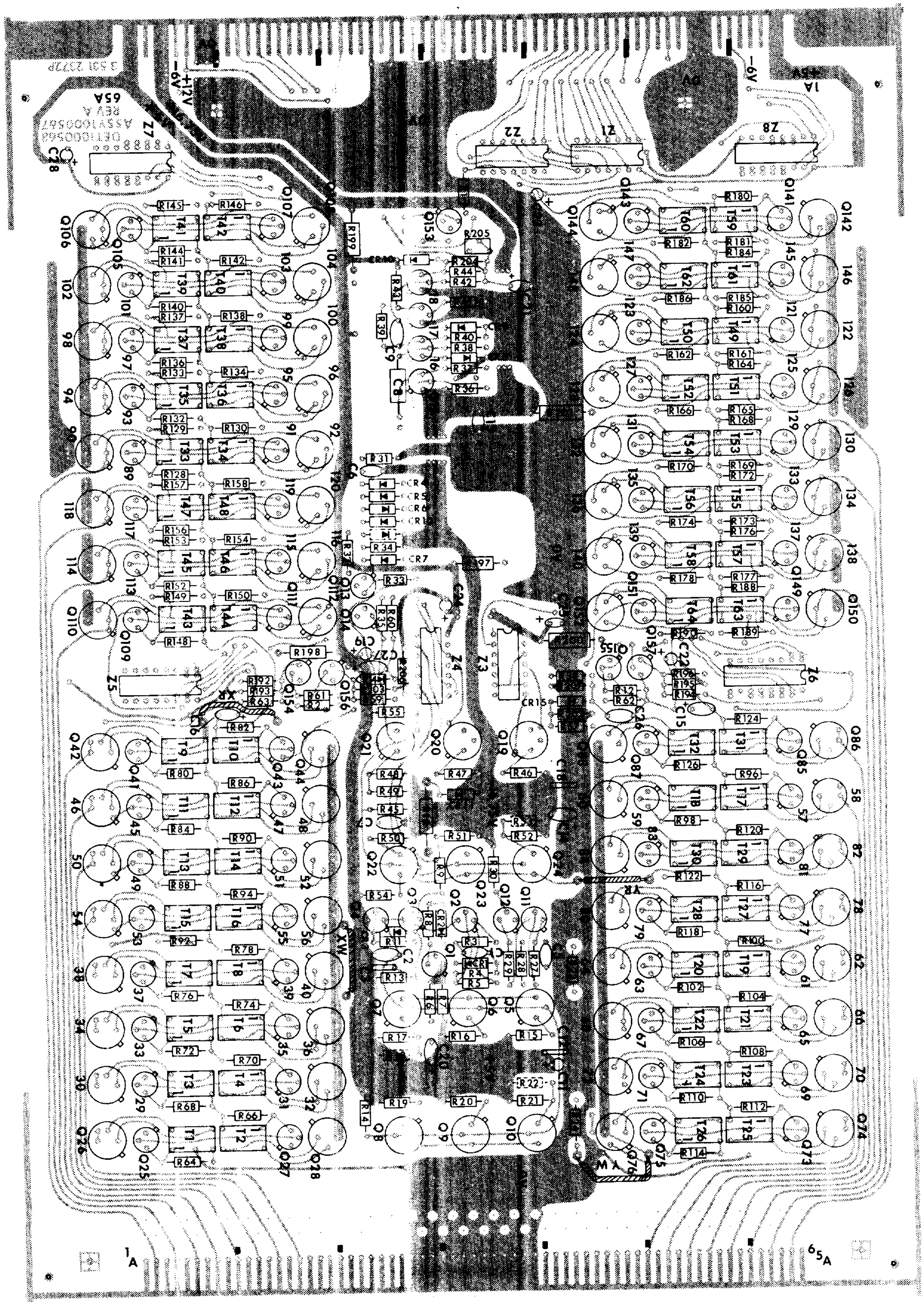
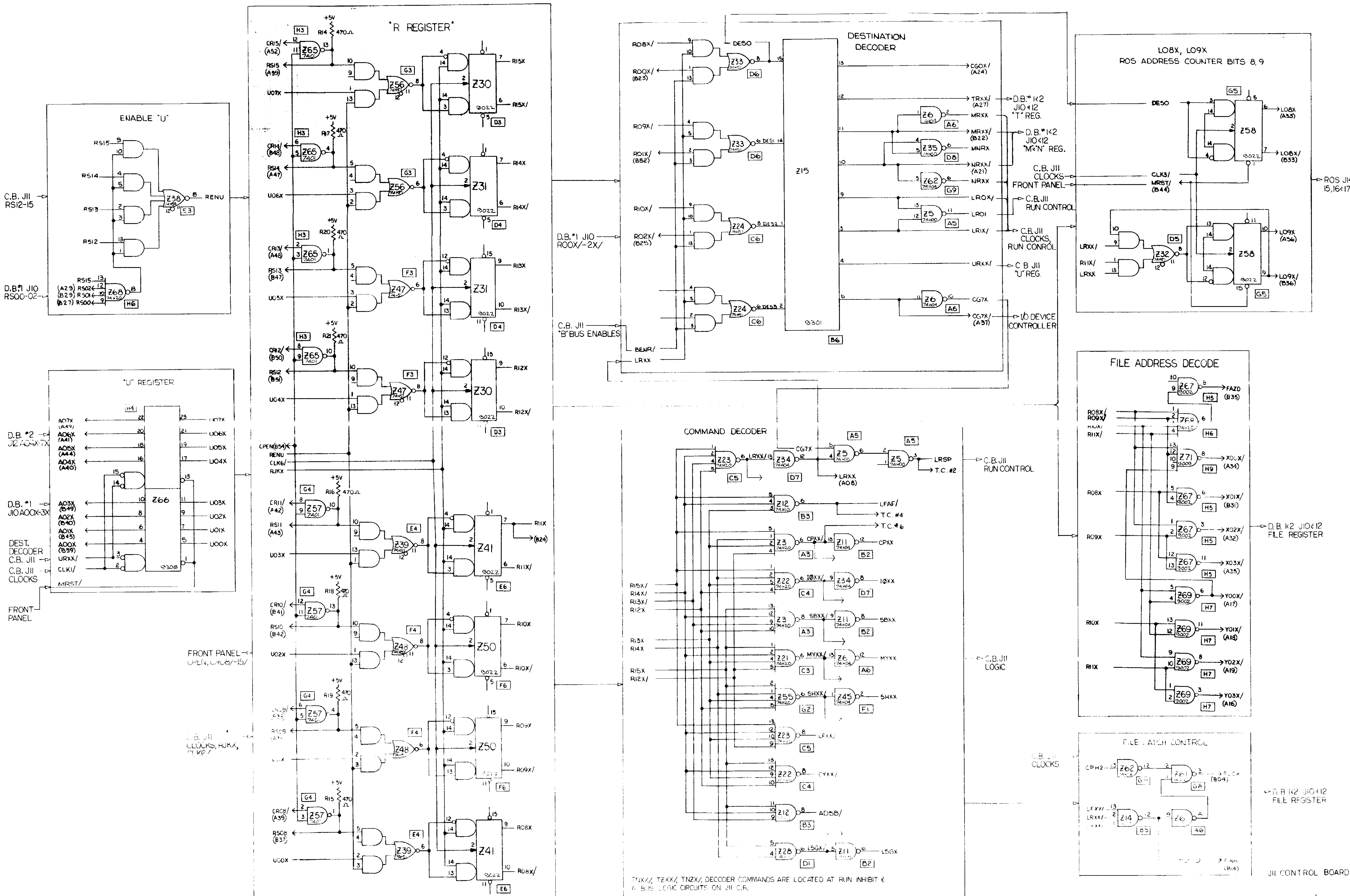
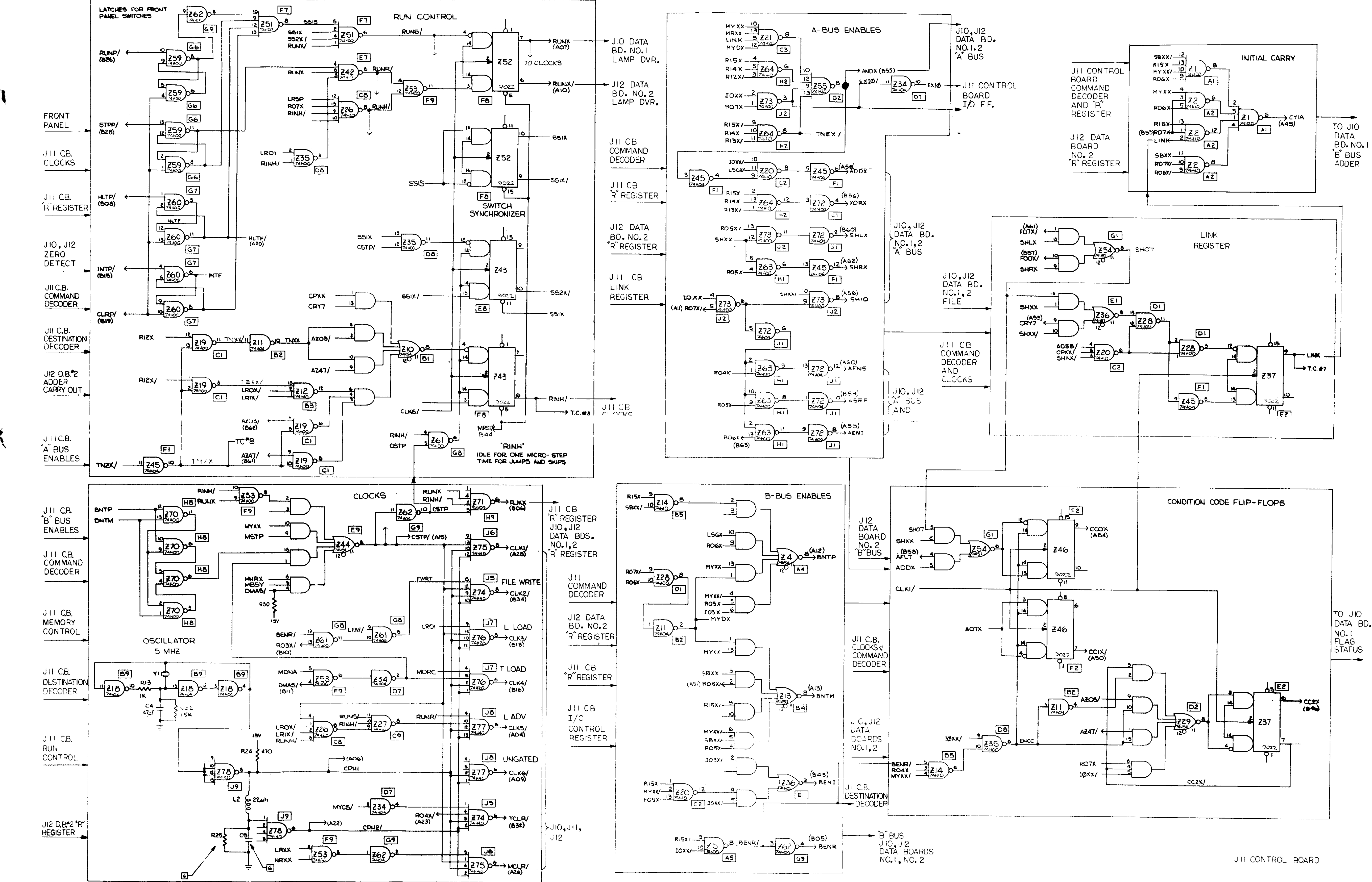
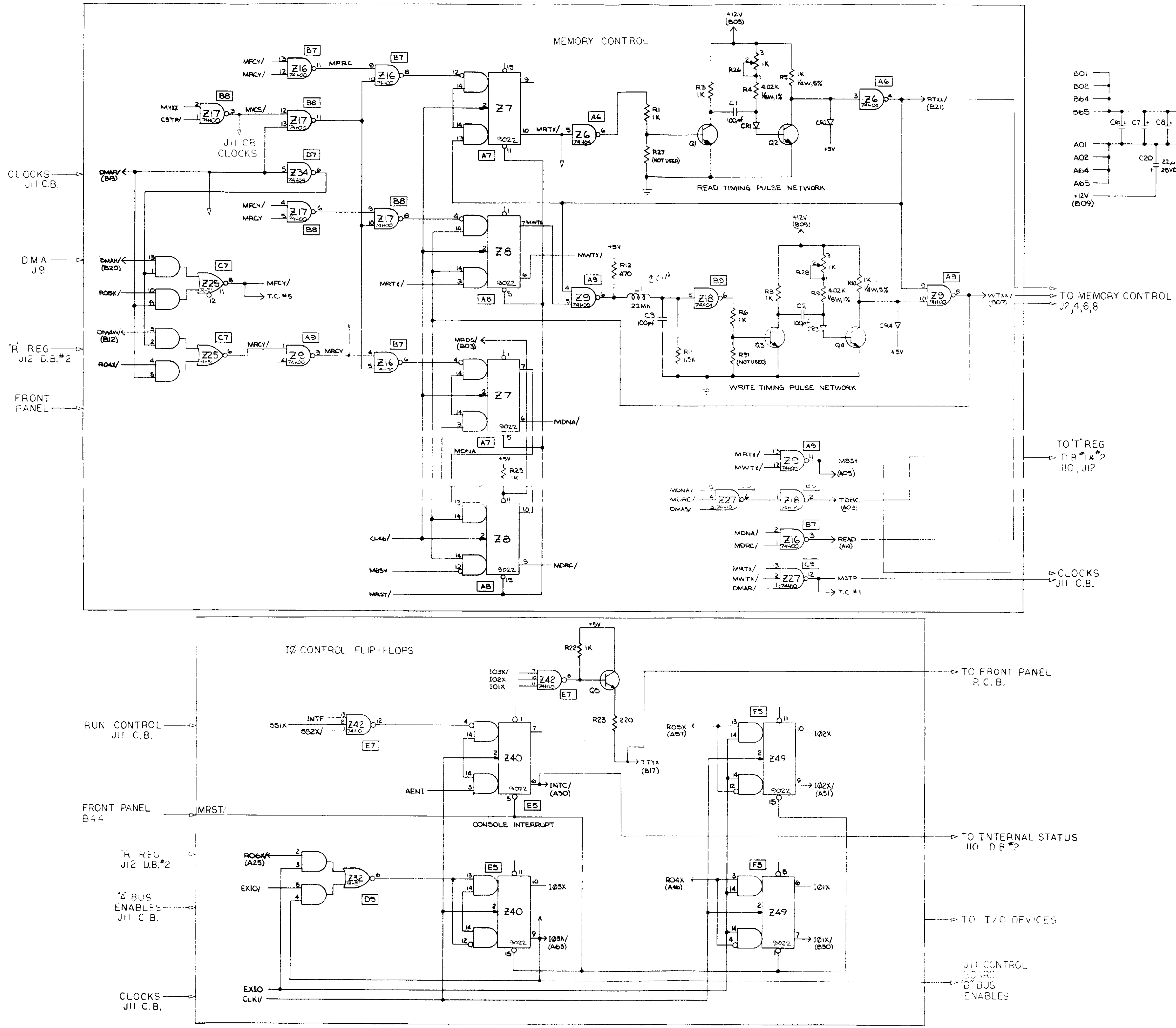


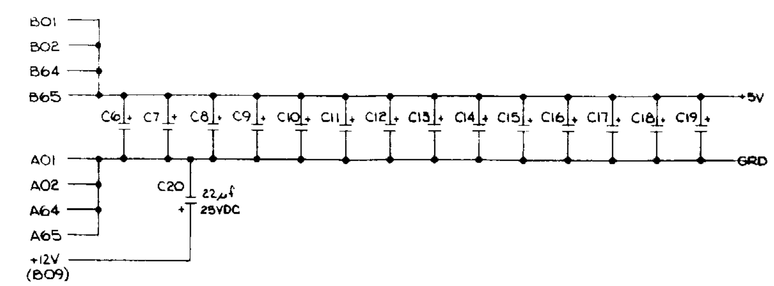
FIGURE 171



ENABLE "U"
"U" REGISTER
"R REGISTER"
DESTINATION DECODER
L08X, L09X
ROS ADDRESS COUNTER BITS 8, 9
COMMAND DECODER
FILE ADDRESS DECODE
FILE LATCH CONTROL
TNXX/, TZXX/, TNZX/ DECODER COMMANDS ARE LOCATED AT RUN INHIBIT & A BUS LOGIC CIRCUITS ON J11 C.B.


LATCHES FOR FRONT PANEL SWITCHES
RUN CONTROL
SWITCH SYNCHRONIZER
"RINH" IDLE FOR ONE MICRO-STEP TIME FOR JUMPS AND SKIPS
FRONT PANEL
J11 C.B. CLOCKS
J11 C.B. "R" REGISTER
J10, J12 ZERO DETECT
J11 C.B. COMMAND DECODER
J11 C.B. DESTINATION DECODER
J12 D.B.#2 ADDER CARRY OUT
J11 C.B. "A" BUS ENABLES
J10 DATA BD. NO. 1 LAMP DVR.
J12 DATA BD. NO. 2 LAMP DVR.
TO CLOCKS
A-BUS ENABLES
J10, J12 DATA BD. NO. 1, 2 "A" BUS
J11 CONTROL BOARD I/O F.F.
J11 CB COMMAND DECODER
J11 CB "R" REGISTER
J12 DATA BD. NO. 2 "R" REGISTER
J11 CB LINK REGISTER
INITIAL CARRY
J11 CONTROL BOARD COMMAND DECODER AND "R" REGISTER
J12 DATA BOARD NO. 2 "R" REGISTER
TO J10 DATA BD. NO. 1 "B" BUS ADDER
LINK REGISTER
J10, J12 DATA BD. NO. 1, 2 FILE
J11 CB COMMAND DECODER AND CLOCKS
CLOCKS
J11 C.B. "B" BUS ENABLES
J11 C.B. COMMAND DECODER
J11 C.B. MEMORY CONTROL
J11 C.B. DESTINATION DECODER
J11 C.B. RUN CONTROL
J12 D.B.#2 "R" REGISTER
OSCILLATOR 5 MHZ
FILE WRITE
L LOAD
T LOAD
L ADV
UNGATED
J11 CB "R" REGISTER J10, J12 DATA BDS. NO. 1, 2 "R" REGISTER
J10, J11, J12
B-BUS ENABLES
J11 COMMAND DECODER
J12 DATA BD. NO. 2 "R" REGISTER
J11 CB "R" REGISTER
J11 CB I/O CONTROL REGISTER
J12 DATA BOARD NO. 2 "B" BUS
J11 C.B. CLOCKS & COMMAND DECODER
J10, J12 DATA BOARDS NO. 1, 2
J11 C.B. DESTINATION DECODER
"B" BUS J10, J12 DATA BOARDS NO. 1, NO. 2
CONDITION CODE FLIP-FLOPS
TO J10 DATA BD. NO. 1 FLAG STATUS
J11 CONTROL BOARD

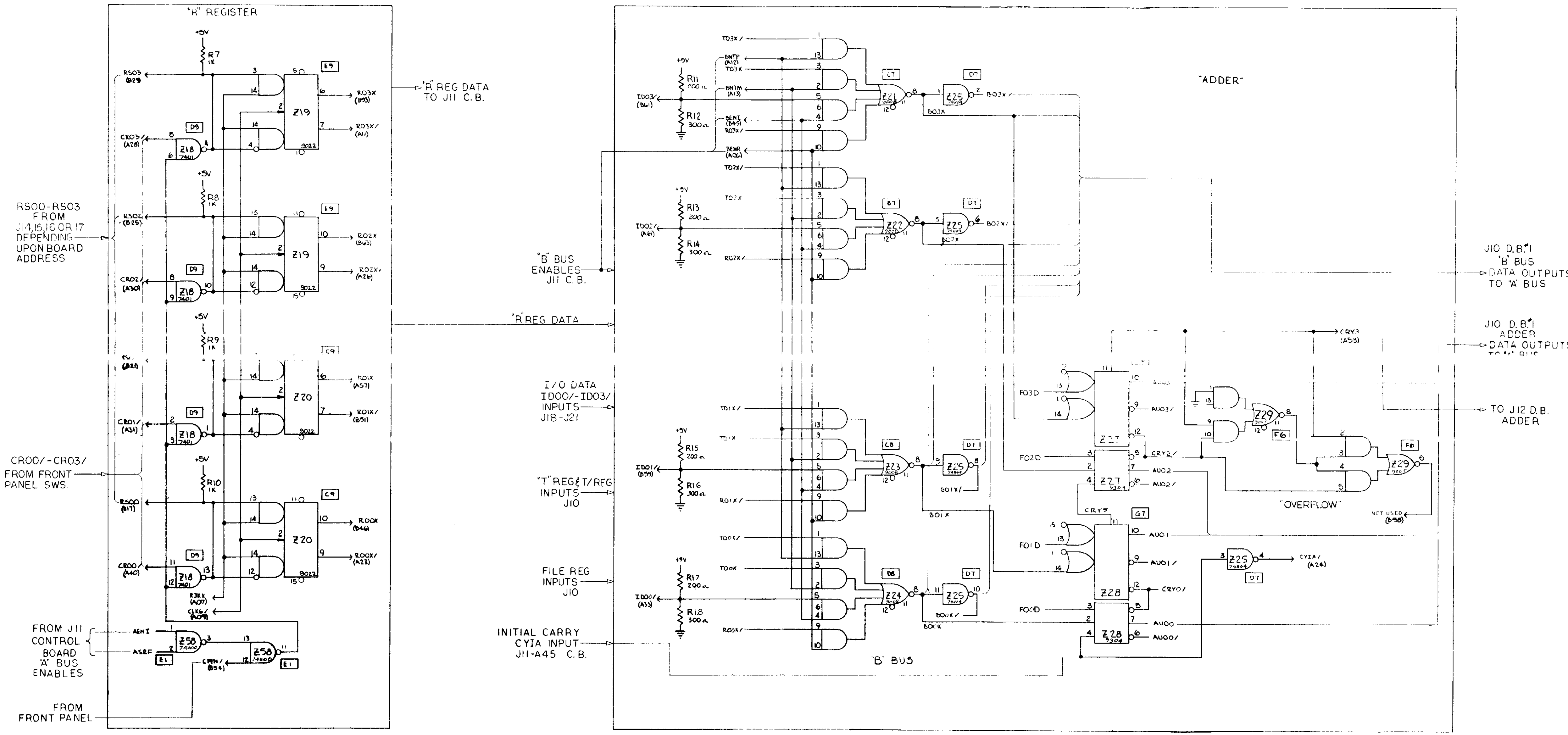


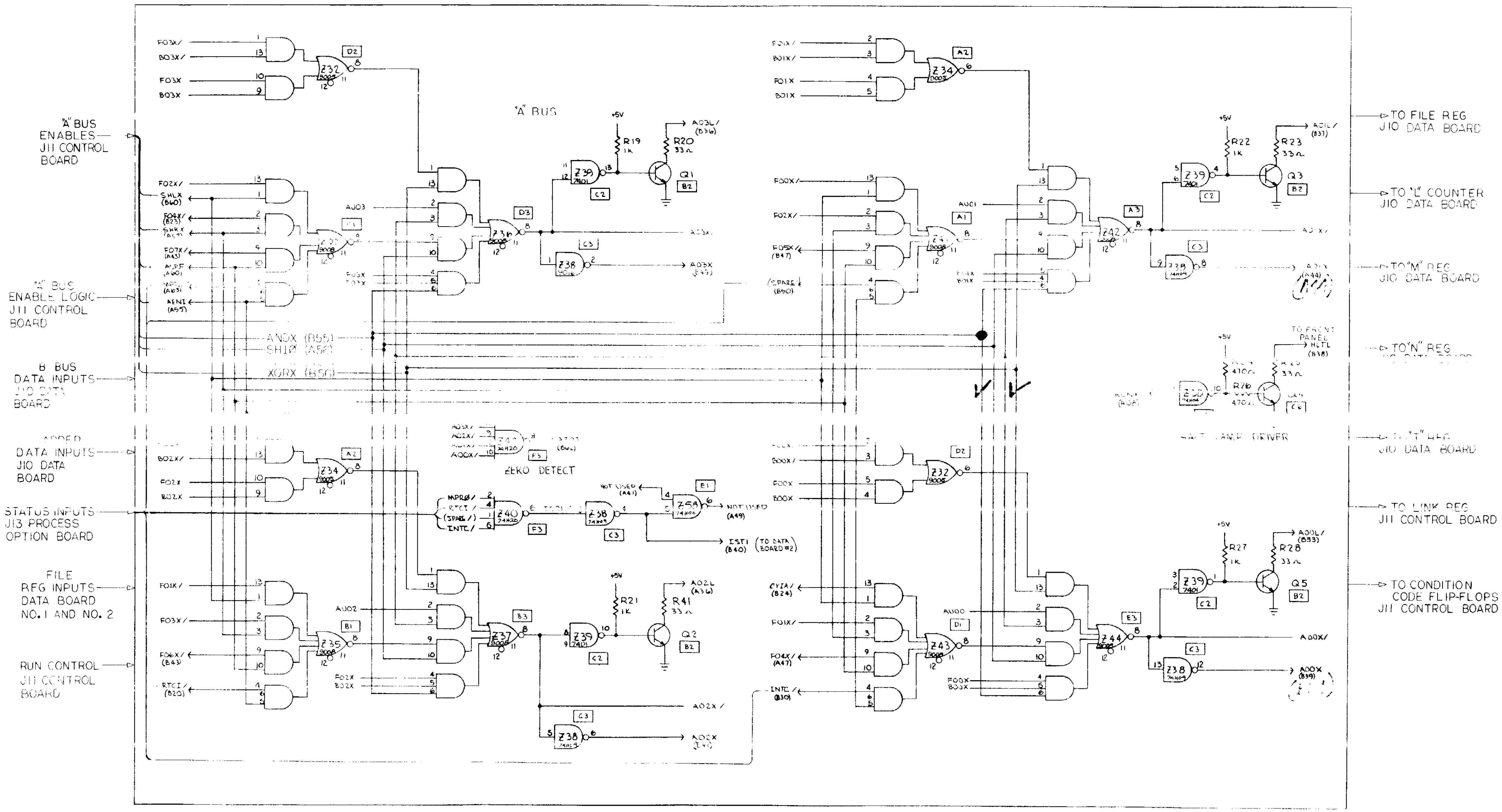


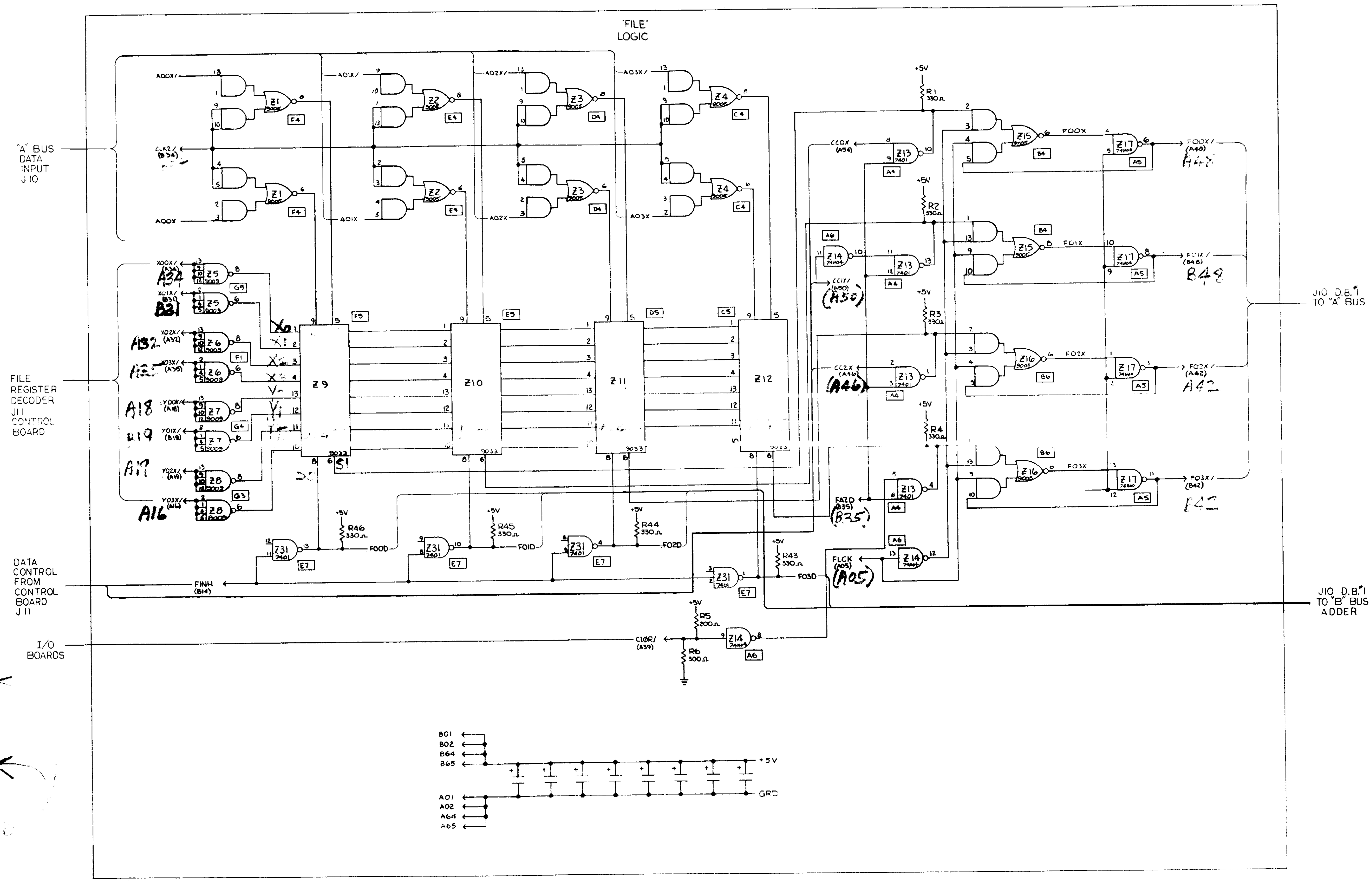
J11
PIN CHART

PIN	TERM	PIN	TERM	PIN	TERM
SOLDER SIDE		A45	CYIA	B24	R11X
A01	GRD	A46	RO4X	B25	RO2X/
A02	GRD	A47	RS14	B26	RUNP/
A03	TDBC	A48	CR13/	B27	RS00
A04	CLK5/	A49	A07X	B28	STPP
A05	MB5Y	A50	CC1X/	B29	RS01
A06	CPH1	A51	RO5X/	B30	IØ1X/
A07	RUNX	A52	CR15/	B31	XO1X/
A08	LRXX	A53	CRY7	B32	TCLR/
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A10	RUNX/	A55	AEN1	B34	CLK2/
A11	RO7X/	A56	SHIØ	B35	FAZD
A12	BNTP	A57	RO5X	B36	LO9X/
A13	BNTM	A58	ADDX	B37	RS08
A14	READ	A59	RS15	B38	CR09/
A15	CSTP/	A60	AEN5	B39	AOOX
A16	YO3X/	A61	FO7X/	B40	AO2X
A17	YOOX/	A62	SHRX	B41	CR10/
A18	YO1X/	A63	IØ3X/	B42	RS10
A19	YO2X/	A64	GRD	B43	AO1X
A20	HLTF	A65	GRD	B44	MRST/
A21	NRXX/	COMPONENT SIDE		B45	BEN1
A22	CPH2/	B01	+5V	B46	CC2X
A23	RO4X/	B02	+5V	B47	RS13
A24	CGOX/	B03	MRDS/	B48	CR14/
A25	RO6X/	B04	FLCK	B49	AO3X,
A26	MCLR/	B05	BENR	B50	CR12/
A27	TRXX/	B06	RJKX	B51	RS12
A28	CLK1/	B07	WTXX/	B52	RO1X/
A29	RS02	B08	HLTP/	B53	RO7X
A30	INTC/	B09	+12V	B54	CPEN
A31	IØ2X/	B10	RO3X/	B55	ANDX
A32	XO2X/	B11	DMAS/	B56	XØRX
A33	LO8X	B12	DMAW/	B57	FOOX/
A34	XOOX/	B13	DMAR/	B58	AFLT
A35	XO3X/	B14	FINH	B59	ASRF
A36	LO9X	B15	INTP/	B60	SHLX
A37	CG7X/	B16	CLK4/	B61	AZ47/
A38	RS09	B17	TTYX	B62	AZO3/
A39	CR08/	B18	CLK■/	B63	RO6X
A40	AO4X	B19	CLRP/	B64	+5V
A41	AO6X	B20	DMAH/	B65	+5V
A42	CR11/	B21	RTXX/		
A43	RS11	B22	MRXX/		
A44	AO5X	B23	ROOX/		

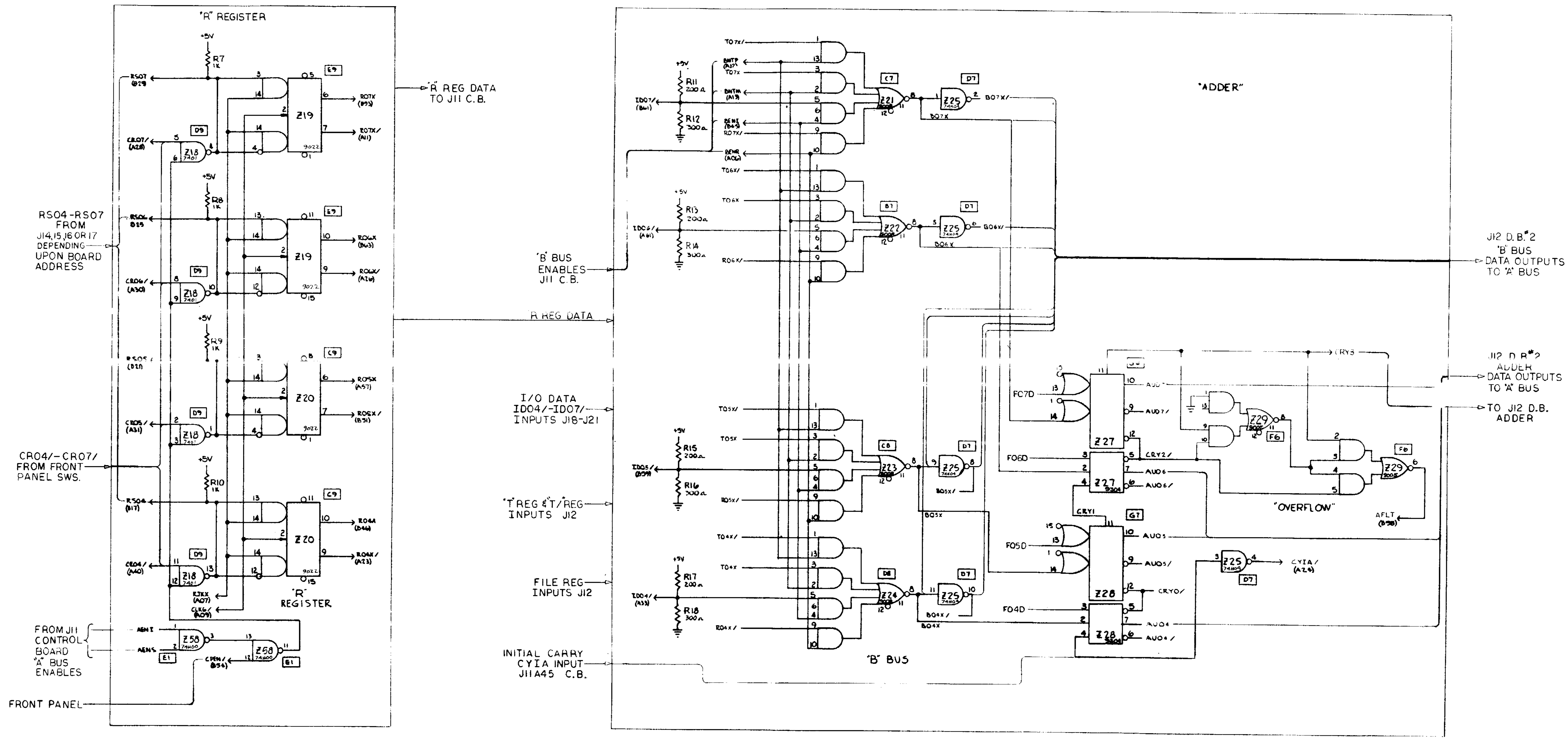
J11 CONTROL BOARD


"R" REGISTER
RS00-RS03 FROM J14,15,16 OR 17 DEPENDING UPON BOARD ADDRESS
CR00/-CR03/ FROM FRONT PANEL SWS.
FROM J11 CONTROL BOARD "A" BUS ENABLES
FROM FRONT PANEL
"R" REG DATA TO J11 C.B.
"B" BUS ENABLES J11 C.B.
"R" REG DATA
I/O DATA ID00/-ID03/ INPUTS J18-J21
"T" REG & T/REG INPUTS J10
FILE REG INPUTS J10
INITIAL CARRY CYIA INPUT J11-A45 C.B.
"ADDER"
"B" BUS
"OVERFLOW"
J10 D.B.#1 "B" BUS DATA OUTPUTS TO "A" BUS
J10 D.B.#1 ADDER DATA OUTPUTS
TO J12 D.B. ADDER
Z19
Z20
Z18
Z58
Z21
Z22
Z23
Z24
Z25
Z27
Z28
Z29
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18

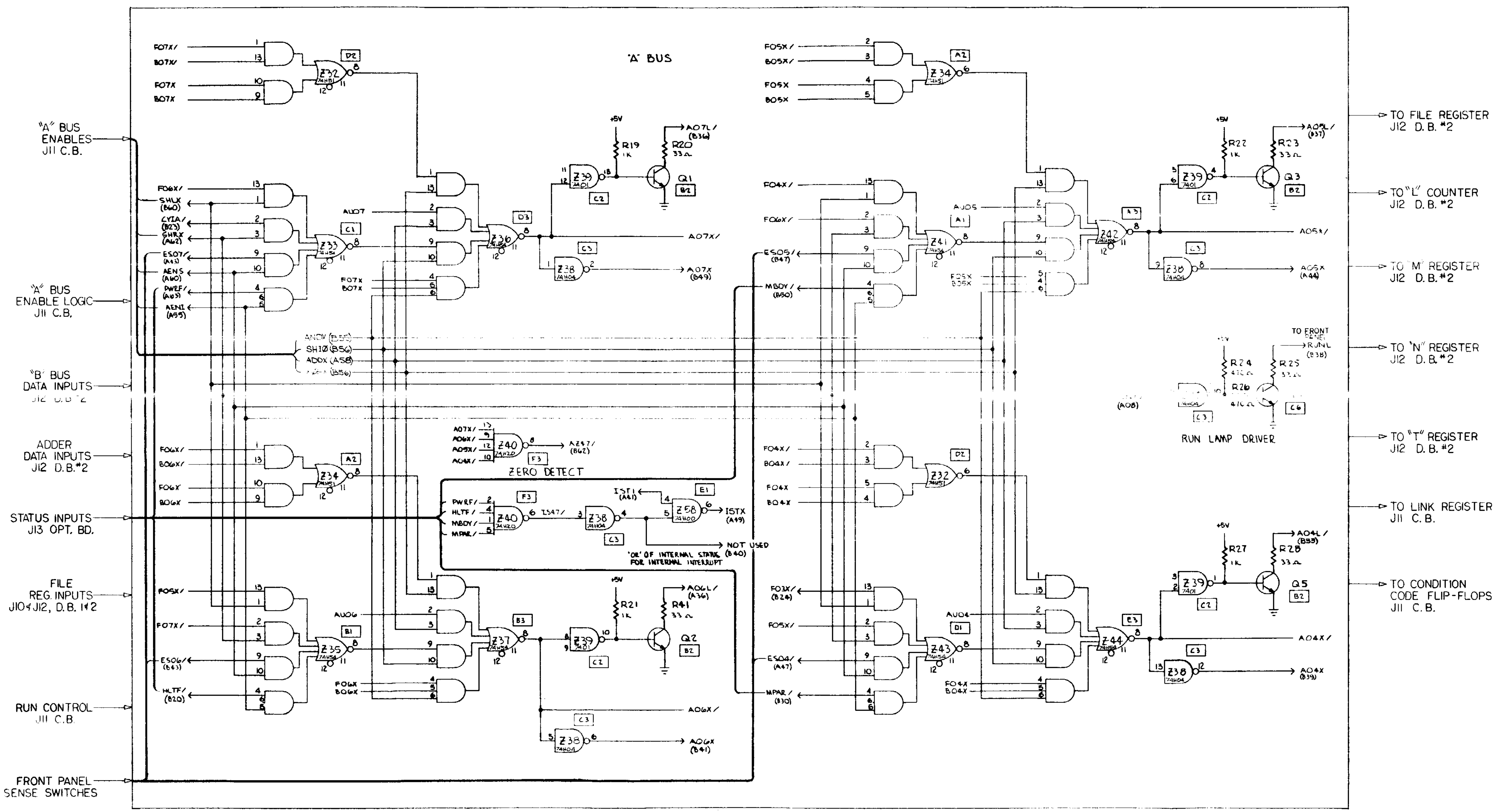

"A" BUS ENABLES J11 CONTROL BOARD
"A" BUS ENABLE LOGIC J11 CONTROL BOARD
B BUS DATA INPUTS J10 DATA BOARD
DATA INPUTS J10 DATA BOARD
STATUS INPUTS J13 PROCESS OPTION BOARD
FILE REG INPUTS DATA BOARD NO. 1 AND NO. 2
RUN CONTROL J11 CONTROL BOARD
"A" BUS
ZERO DETECT
ANDX (B55)
XORX (B56)
TO FILE REG J10 DATA BOARD
TO "L" COUNTER J10 DATA BOARD
TO "M" REG J10 DATA BOARD
TO "N" REG
TO LINK REG J11 CONTROL BOARD
TO CONDITION CODE FLIP-FLOPS J11 CONTROL BOARD
Z32
Z34
Z35
Z36
Z37
Z38
Z39
Z40
Z42
Z43
Z44
R19
R20
R21
R22
R23
R27
R28
R41
Q1
Q2
Q3
Q5
+5V
A03L/
A03X
A02X/
A02X
A01L/
A00L/
A00X/
A00X
F03X/
B03X/
F03X
B03X
F02X/
F01X/
F01X
B01X
F00X/
B00X/
F00X
B00X
NOT USED
(TO DATA BOARD #2)



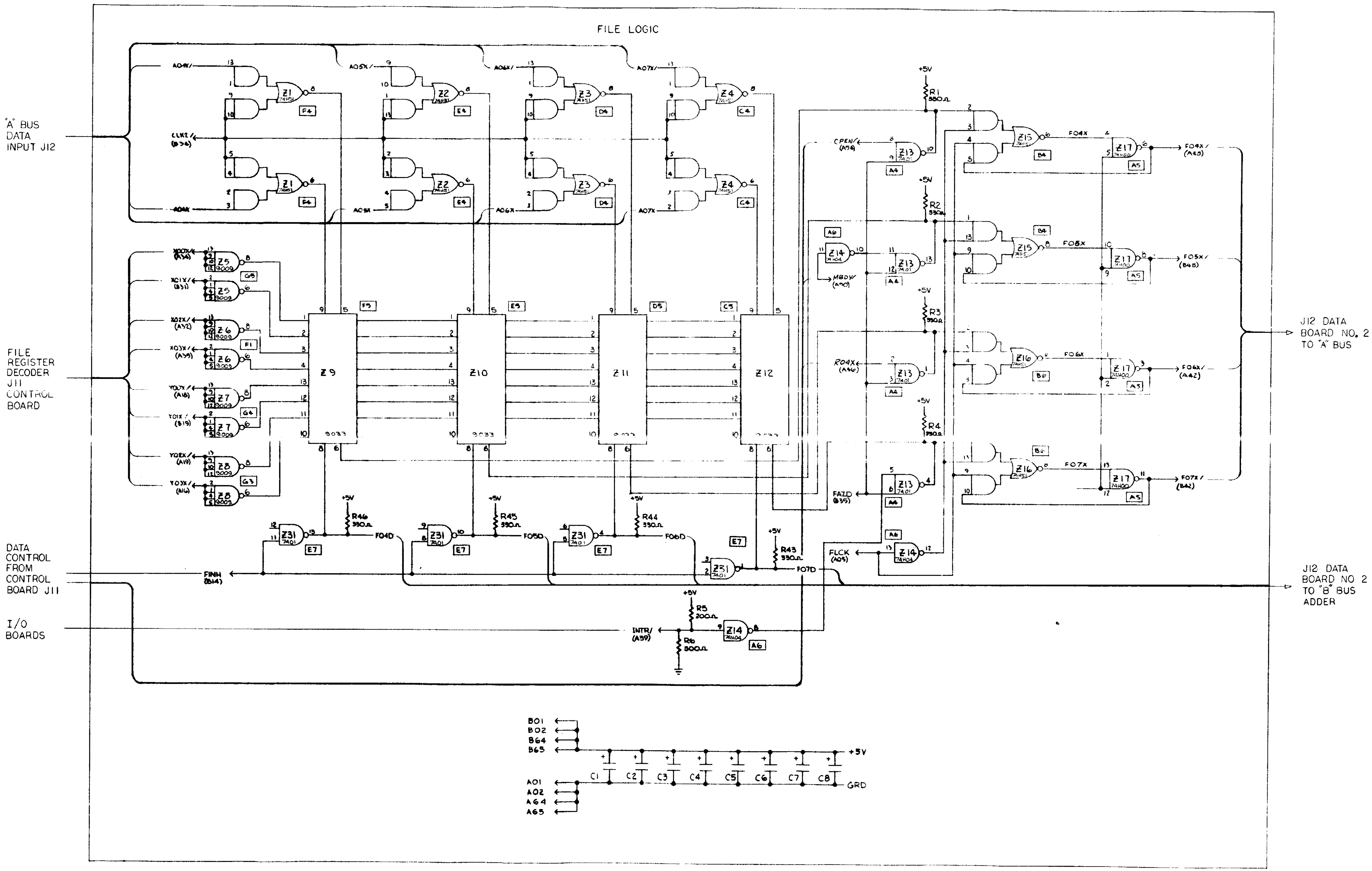
J12=SN2547←
J11=SN1360
J10=SN2414←



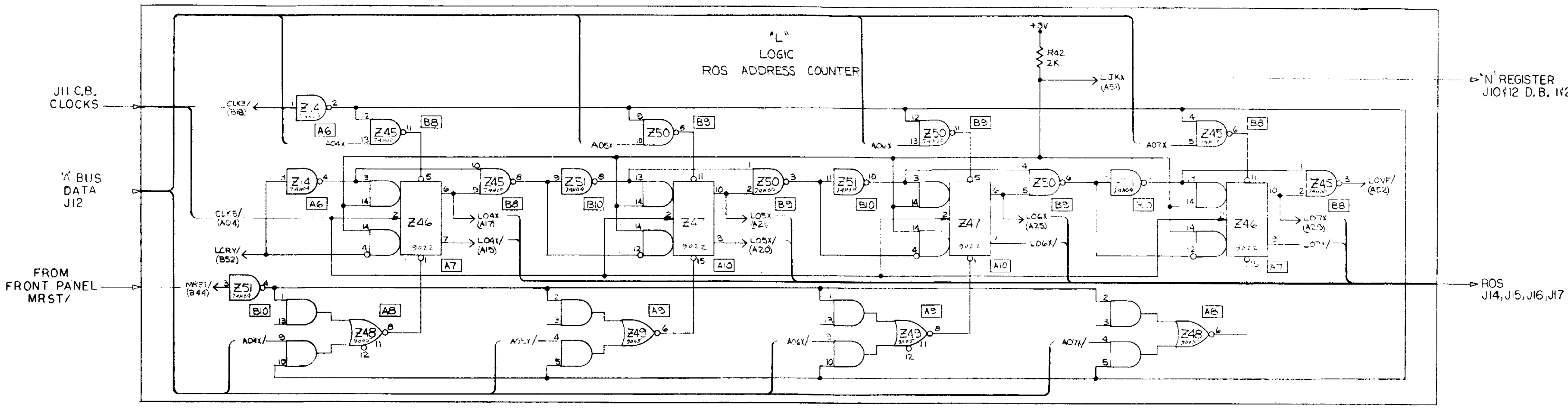
"R" REGISTER
"R" REG DATA TO J11 C.B.
RS04-RS07 FROM J14,15,16 OR 17 DEPENDING UPON BOARD ADDRESS
CR04/-CR07/ FROM FRONT PANEL SWS.
FROM J11 CONTROL BOARD "A" BUS ENABLES
FRONT PANEL
"R" REGISTER
"ADDER"
'B' BUS ENABLES J11 C.B.
R REG DATA
I/O DATA ID04/-ID07/ INPUTS J18-J21
"T" REG & "T/" REG INPUTS J12
FILE REG INPUTS J12
INITIAL CARRY CY1A INPUT J11A45 C.B.
'B' BUS
J12 D.B.#2 'B' BUS DATA OUTPUTS TO 'A' BUS
J12 D.B.#2 ADDER DATA OUTPUTS TO 'A' BUS
TO J12 D.B. ADDER
"OVERFLOW"

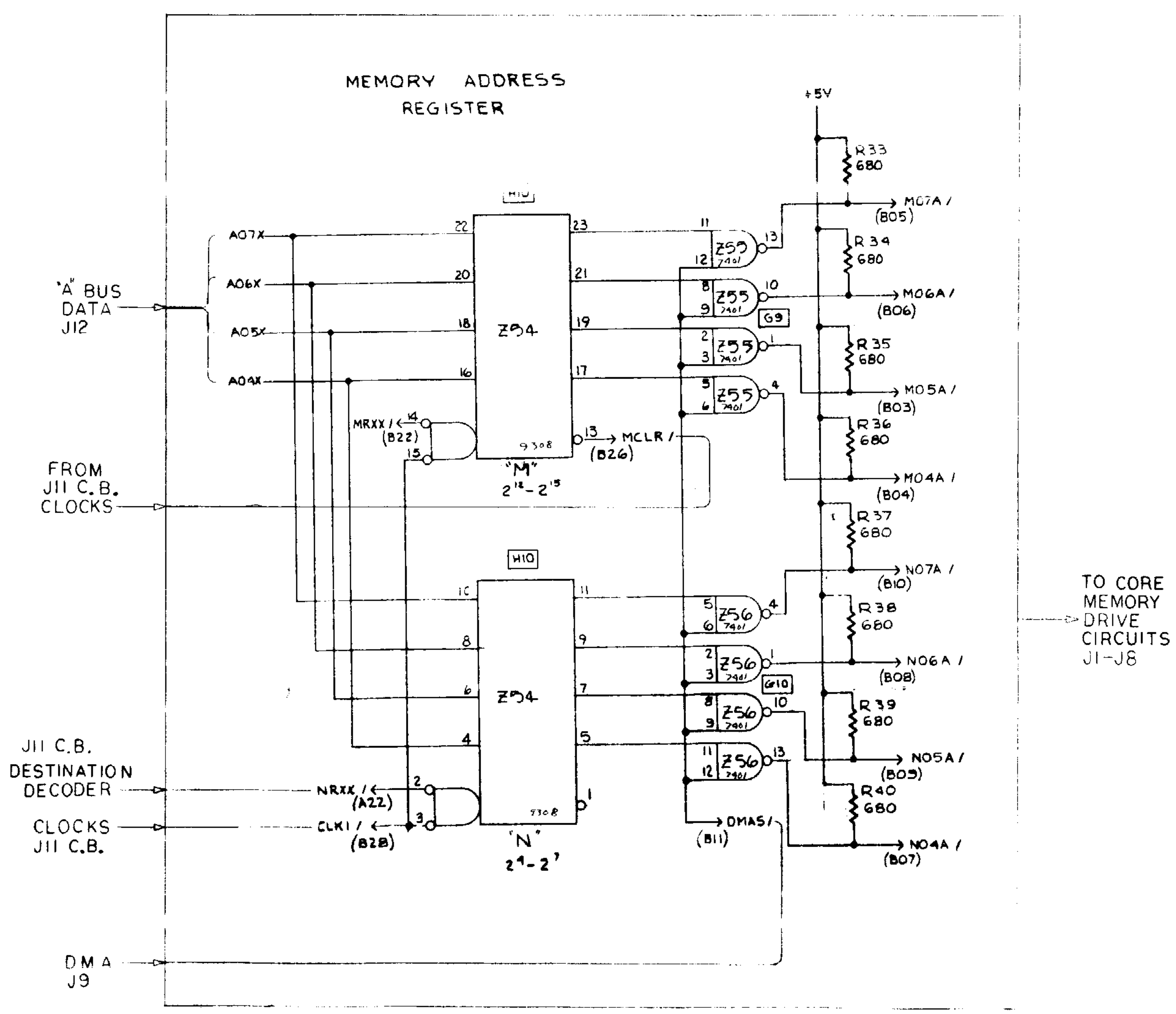


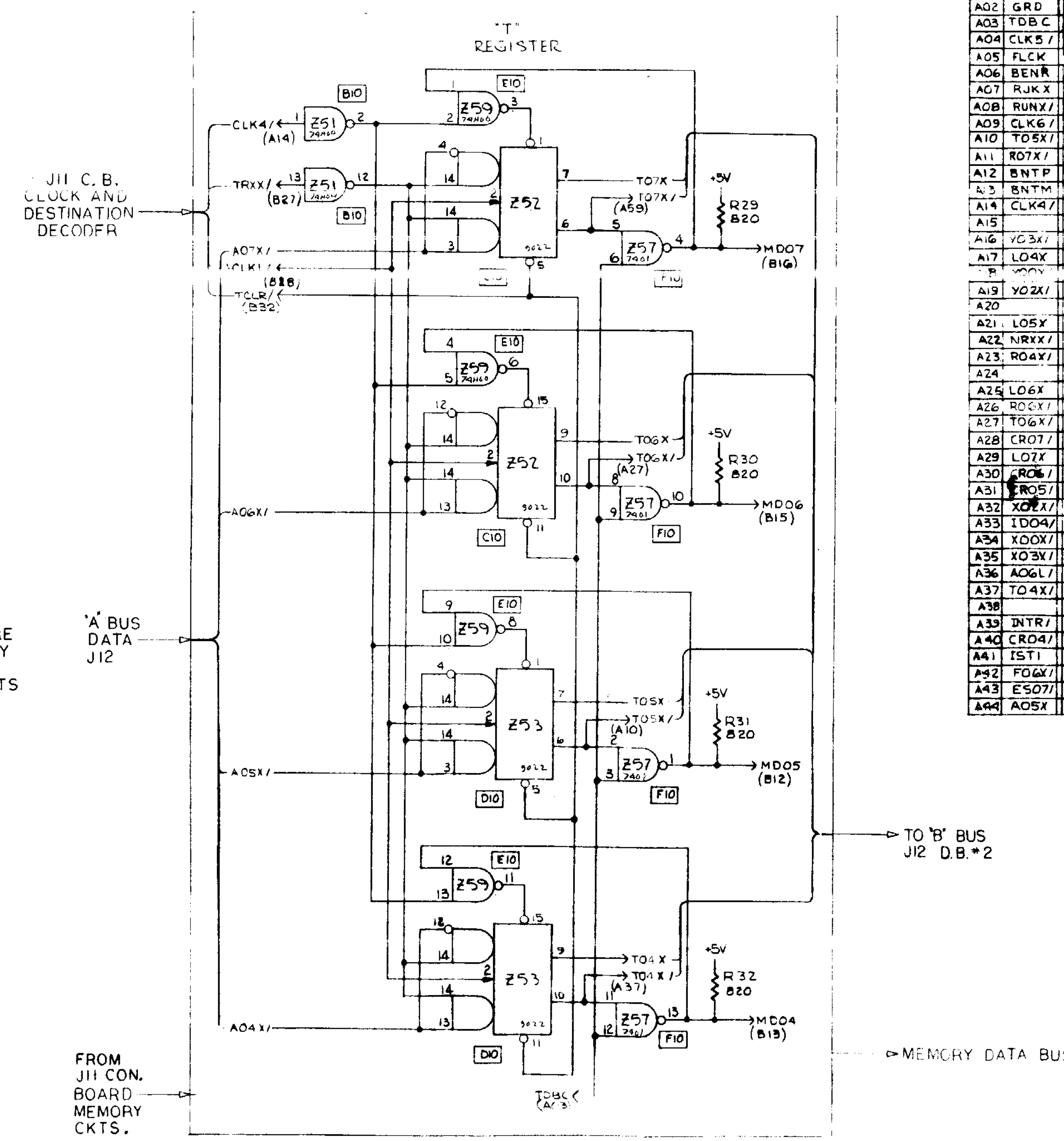
"A" BUS
"A" BUS ENABLES J11 C.B.
"A" BUS ENABLE LOGIC J11 C.B.
"B" BUS DATA INPUTS J12 D.B. #2
ADDER DATA INPUTS J12 D.B.#2
STATUS INPUTS J13 OPT. BD.
FILE REG. INPUTS J10 & J12, D.B. 1&2
RUN CONTROL J11 C.B.
FRONT PANEL SENSE SWITCHES
TO FILE REGISTER J12 D.B. #2
TO "L" COUNTER J12 D.B. #2
TO "M" REGISTER J12 D.B. #2
TO "N" REGISTER J12 D.B. #2
TO "T" REGISTER J12 D.B. #2
TO LINK REGISTER J11 C.B.
TO CONDITION CODE FLIP-FLOPS J11 C.B.
ZERO DETECT
RUN LAMP DRIVER
"OR" OF INTERNAL STATUS FOR INTERNAL INTERRUPT
NOT USED



FILE LOGIC
"A" BUS DATA INPUT J12
FILE REGISTER DECODER J11 CONTROL BOARD
DATA CONTROL FROM CONTROL BOARD J11
I/O BOARDS
J12 DATA BOARD NO. 2 TO "A" BUS
J12 DATA BOARD NO 2 TO "B" BUS ADDER

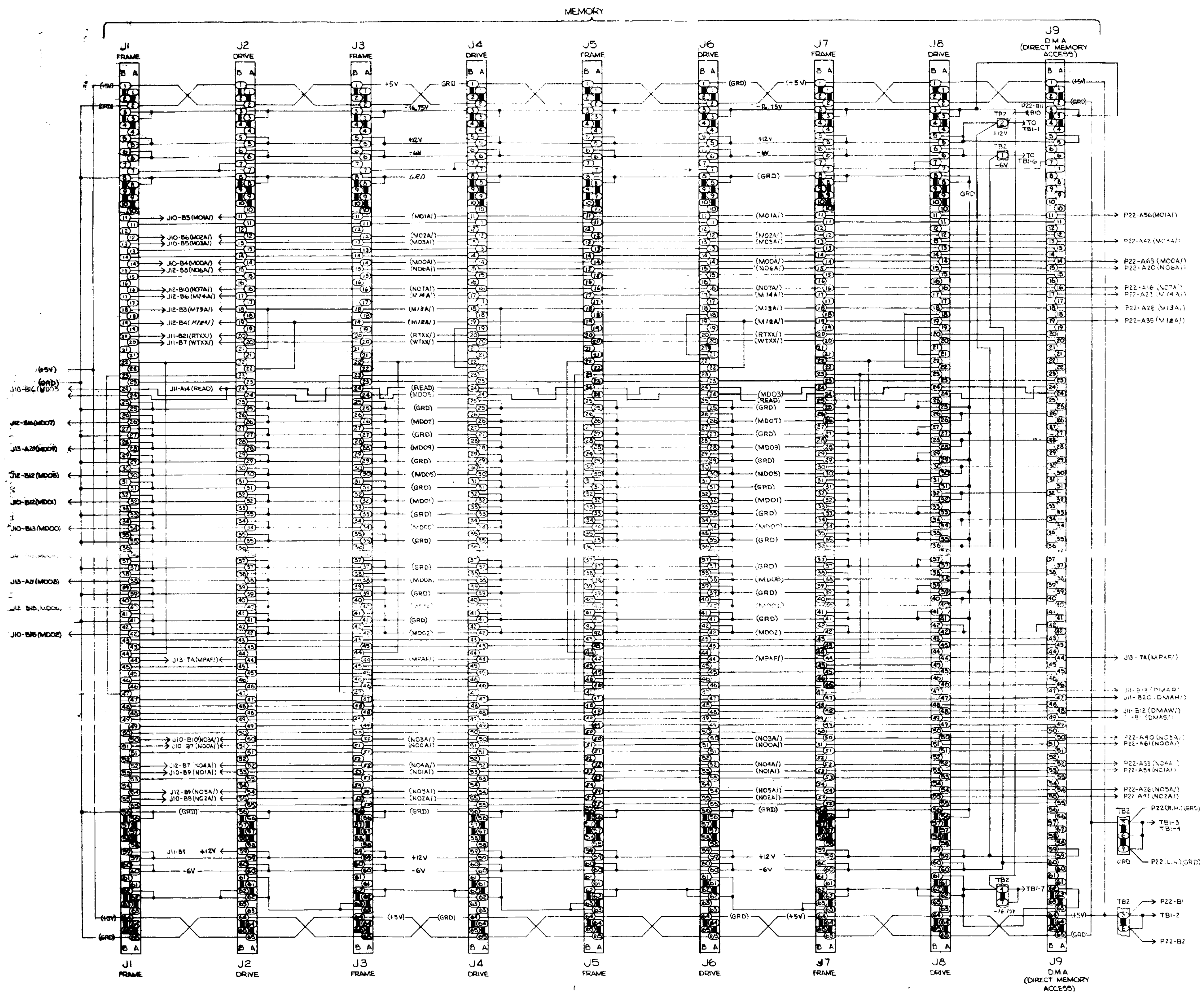




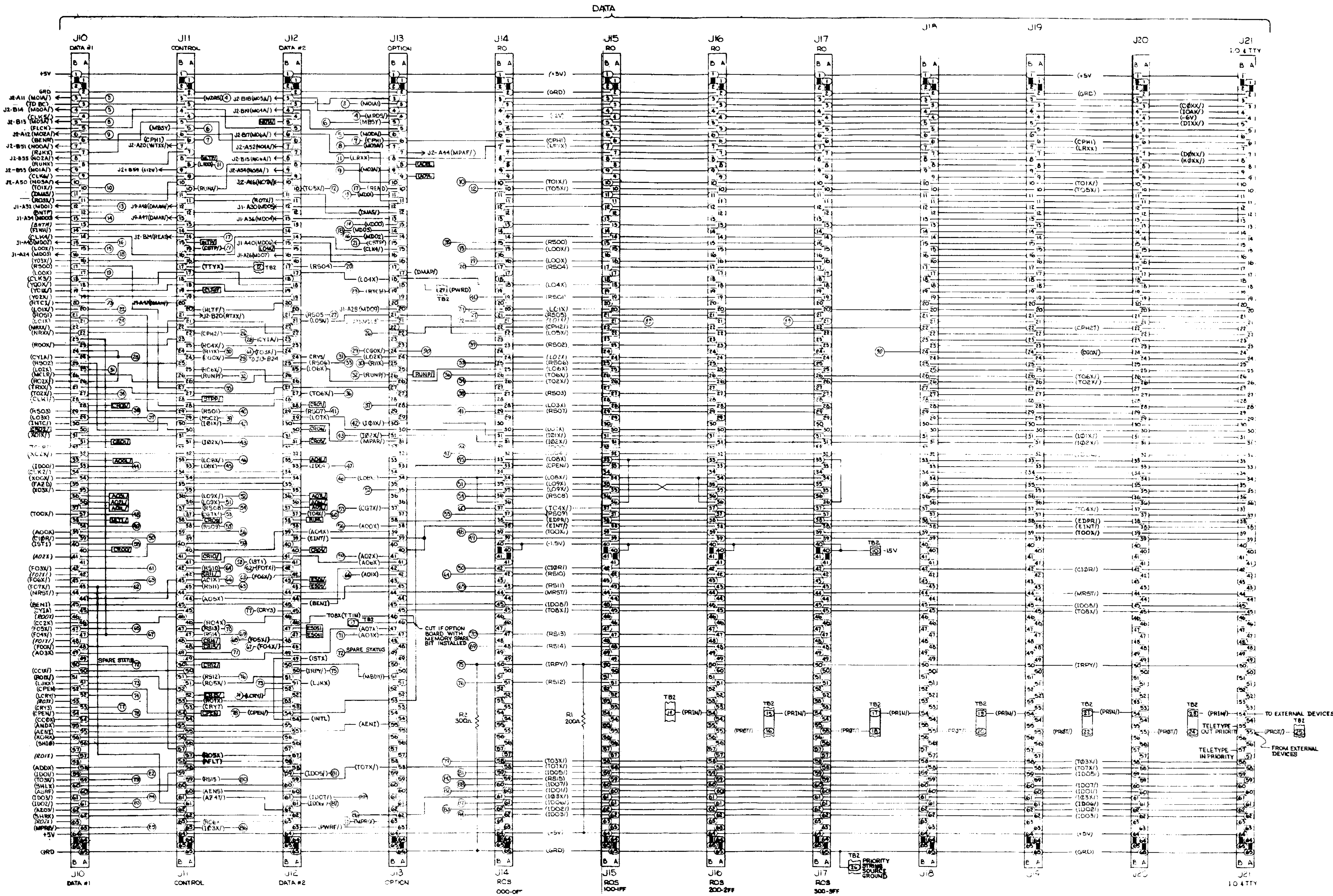


PIN CHART

PIN	TERM	PIN	TERM	PIN	TERM
SOLDER SIDE		A45	CRY3	B24	FO3X/
A01	GRD	A46	TO8X:TTIN	B25	RS06
A02	GRD	A47	ES04/	B26	MCLR/
A03	TDBC	A48	FO4X /	B27	TRXX/
A04	CLK5 /	A49	ISTX	B28	CLK1/
A05	FLCK	A50	IRPY/	B29	RS07
A06	BENR	A51	LJKX	B30	MPAR/
A07	RJKX	A52		B31	XO1X/
A08	RUNX/	A53	CRY7	B32	TCLR/
A09	CLK6 /	A54	INTL	B33	AO4L/
A10	TO5X/	A55	AEN I	B34	CLK2/
A11	RO7X/	A56	SHIO	B35	FAZD
A12	BNTP	A57	RO5X	B36	AO7L/
A13	BNTM	A58	ADDX	B37	AO5L/
A14	CLK4/	A59	TO7X/	B38	RUNL
A15		A60	AENS	B39	AO4X
A16	YO3X/	A61	IDO6/	B40	
A17	LO4X	A62	SHRX	B41	AO6X
[illegible]	[illegible]	A63	[illegible]	B42	[illegible]
A19	YO2X/	A64	GRD	B43	ES06/
A20		A65	GRD	B44	MRST/
A21	LO5X	COMPONENT SIDE		B45	BENI
A22	NRXX/	B01	+5V	B46	RO4X
A23	RO4X/	B02	+5V	B47	ES05/
A24		B03	MO5A/	B48	FO5X/
A25	LO6X	B04	MO4A/	B49	AO7X
A26	RO6X/	B05	MO7A/	B50	MBDY/
A27	TO6X/	B06	MO6A/	B51	RO5X /
A28	CRO7/	B07	NO4A/	B52	LCRY/
A29	LO7X	B08	NO6A/	B53	RO7X
A30	CRO6/	B09	NO5A/	B54	CPEN/
A31	CRO5/	B10	NO7A/	B55	ANDX
A32	XO2X/	B11	DMAS/	B56	XORX
A33	IDO4/	B12	MDO5	B57	
A34	XOOX/	B13	MDO4	B58	AFLT
A35	XO3X/	B14	FINH	B59	IDO5/
A36	AO6L/	B15	MDO6	B60	SHLX
A37	TO4X/	B16	MDO7	B61	IDO7/
A38		B17	RS04	B62	AZ47/
A39	INTR/	B18	CLK3/	B63	RO6X
A40	CRO4/	B19	YO1X/	B64	+5V
A41	ISTI	B20	HLTF/	B65	+5V
A42	FO6X/	B21	RS05		
A43	ES07/	B22	MRXX/		
A44	AO5X	B23	CY1A/		



2. THIS SYMBOL, [XXXX] REPRESENTS DISCRETE WIRES TO FRONT PANEL P.C. BOARD.
1. FOR WIRE LIST SEE DRAWING NUMBER 1000266
DRAWING NUMBER 1000269
NOTES: UNLESS OTHERWISE SPECIFIED



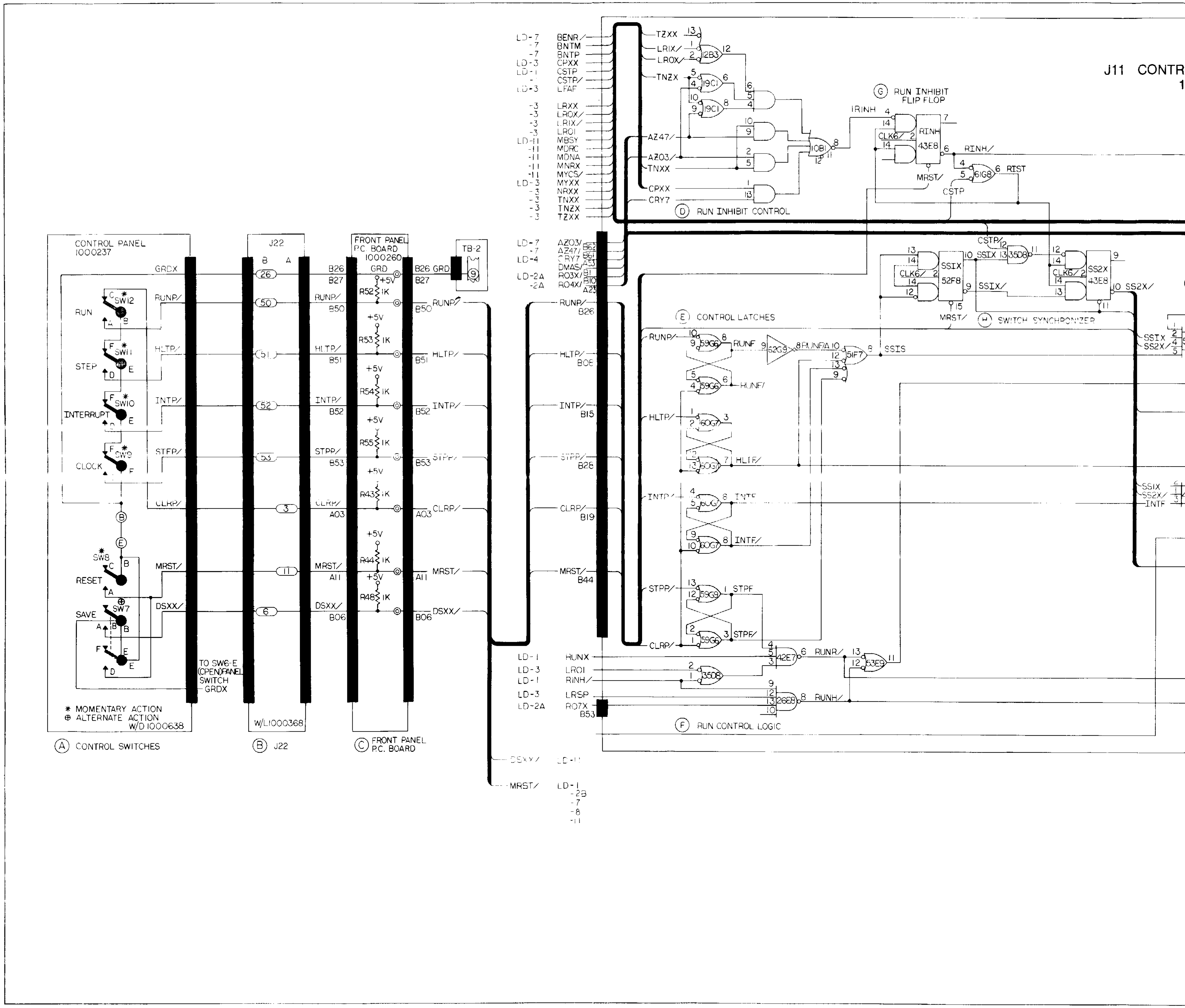
REVISIONS

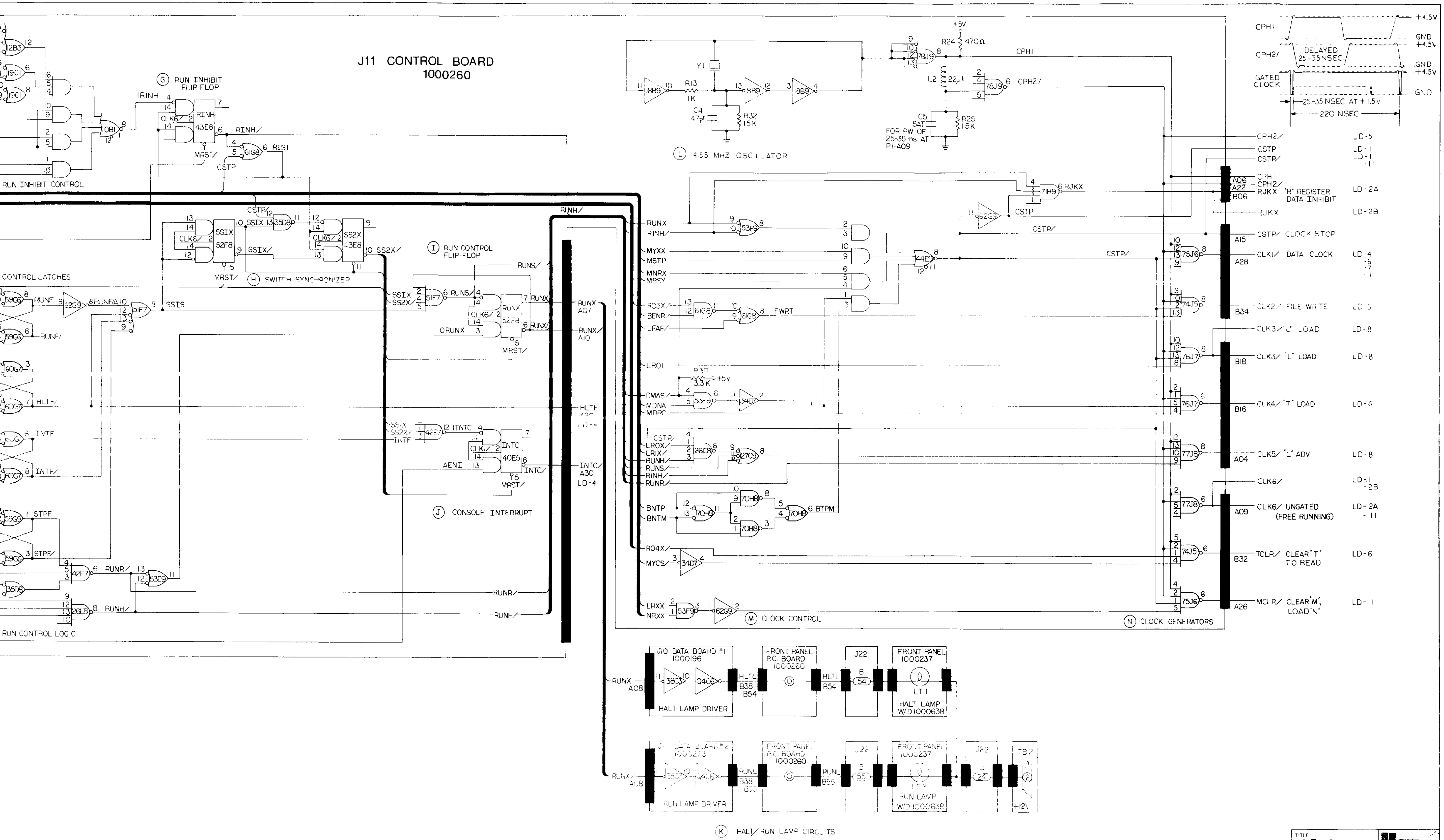
SCHEMATIC, BACK PLANE

MICRO SYSTEMS INC
SANTA ANA, CALIFORNIA

R 1000579 N/C

SCALE NONE


J11 CONTR
CONTROL PANEL 1000237
J22
FRONT PANEL P.C. BOARD 1000260
TB-2
RUN
STEP
INTERRUPT
CLOCK
RESET
SAVE
TO SW6-E (OPEN)PANEL SWITCH GRDX
* MOMENTARY ACTION
⊕ ALTERNATE ACTION
W/D 1000638
W/L1000368
(A) CONTROL SWITCHES
(B) J22
(C) FRONT PANEL P.C. BOARD
(D) RUN INHIBIT CONTROL
(E) CONTROL LATCHES
(F) RUN CONTROL LOGIC
(G) RUN INHIBIT FLIP FLOP
(H) SWITCH SYNCHRONIZER



TITLE LD-1
PANEL CLOCK CONTROL CIRCUITS

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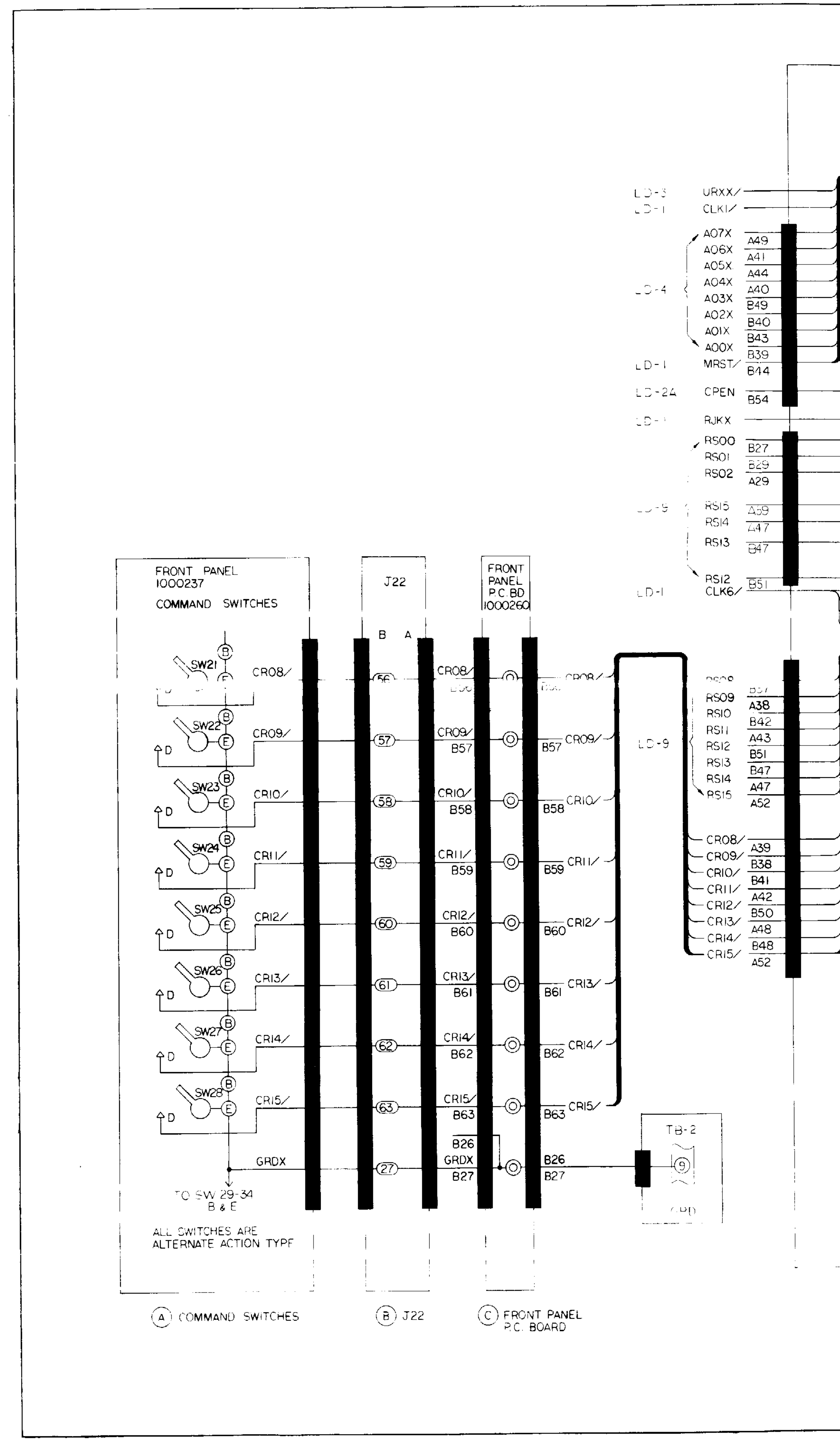
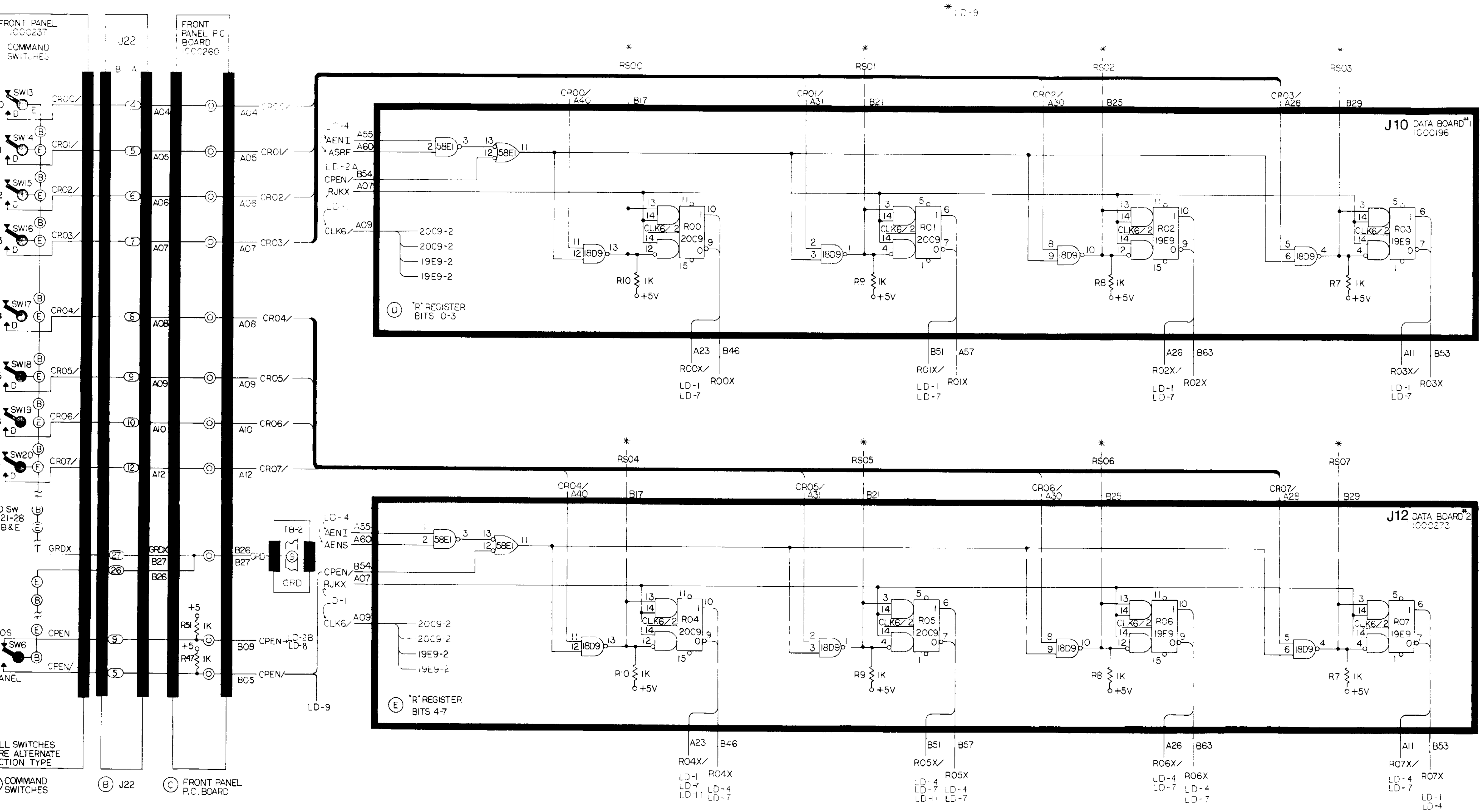
SHEET 1 OF 12 REV


FRONT PANEL
1000237
COMMAND SWITCHES
J22
FRONT PANEL P.C. BD 1000260
ALL SWITCHES ARE ALTERNATE ACTION TYPE
TO SW 29-34 B & E
TB-2
A COMMAND SWITCHES
B J22
C FRONT PANEL P.C. BOARD



TITLE: LD-2A

'R' REGISTER BITS 0-7

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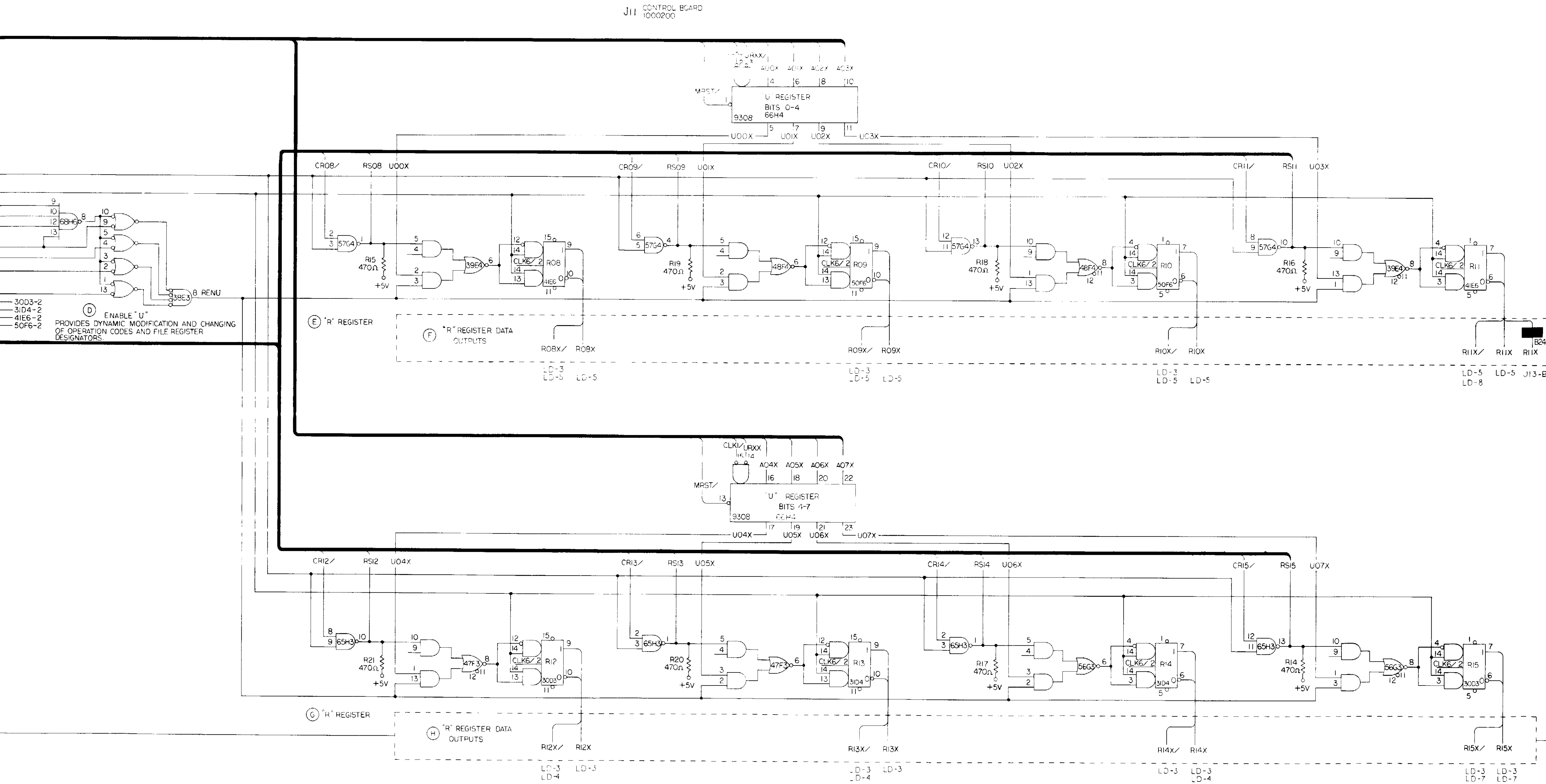
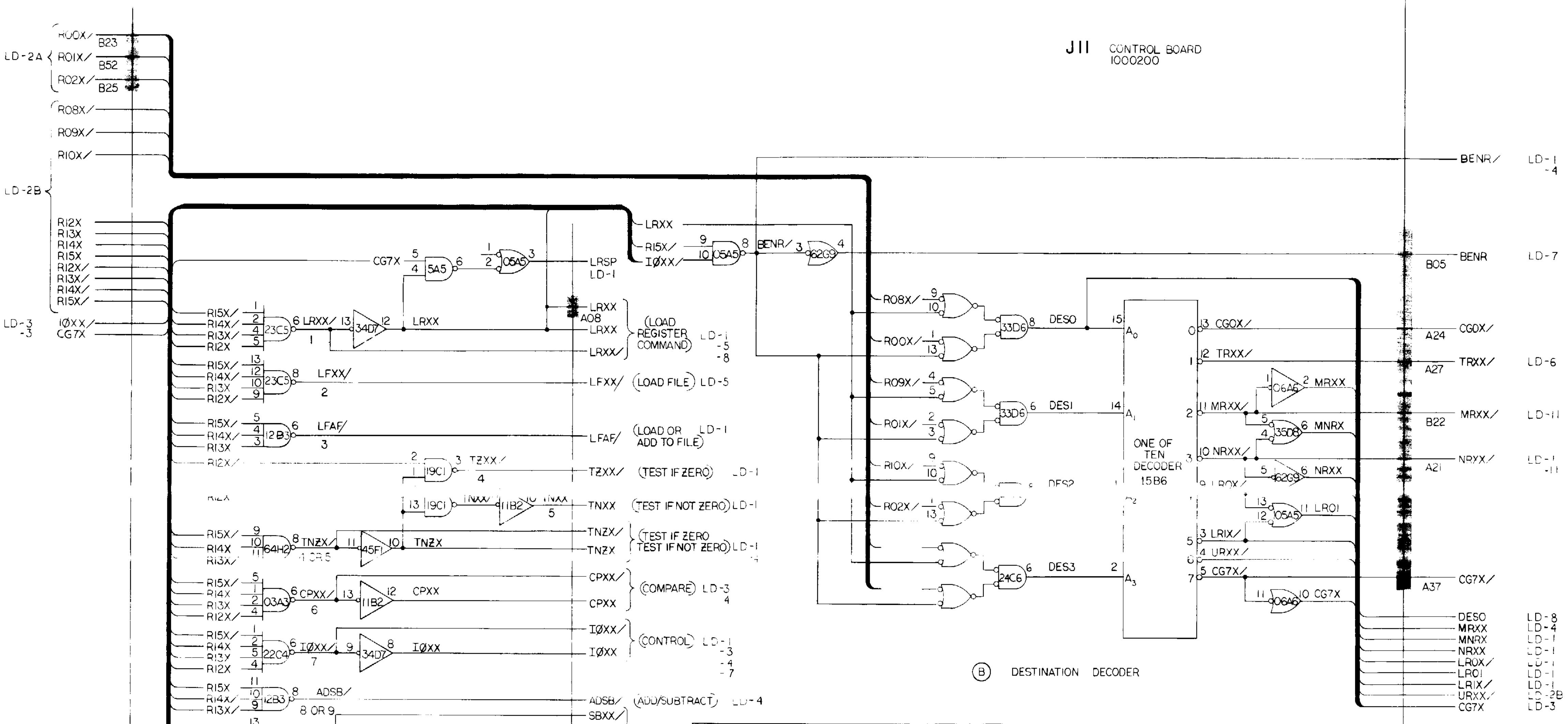
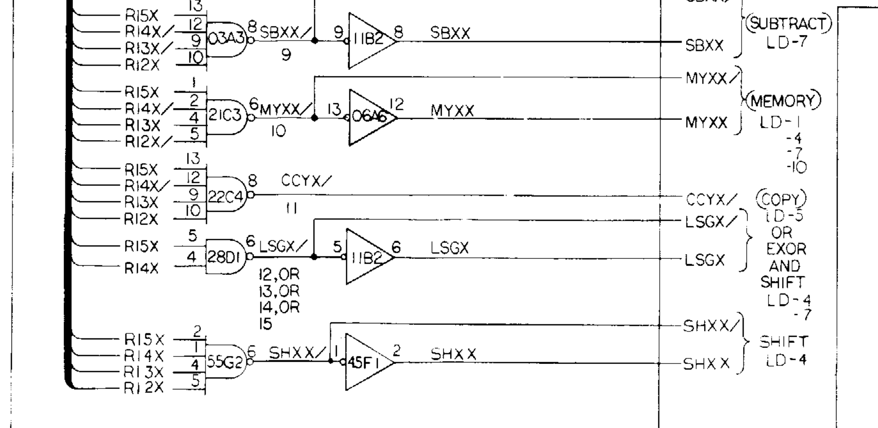


TITLE: LD-2B
"U" REGISTER
"R" REGISTER
BITS 7-15

SHEET 3



(B) DESTINATION DECODER



(A) COMMAND DECODER

(C) TABLE TLD-3·1

LITERAL COMMANDS LOAD REGISTER					OPERATE COMMANDS IØXX CONTROL COMMAND				OPERATE COMMANDS R15X/ COMMANDS			
COMMAND TERM	OP CODE	MNEMONIC	LRXX SELECTED	AFFECTED	REGISTER DESIGNATOR	MNEMONIC	REGISTER SELECTED	AFFECTED	REGISTER DESIGNATOR	MNEMONIC	R15X/ SELECTED	AFFECTED
CG0X/	10	LZ	LOAD ZERO CONTROL		0		NONE		0		NONE	
TRXX/	11/19	LT	LOAD T	T	1	T	T REGISTER	r	1	T	T REGISTER	r
MRXX/	12	LM	LOAD M	M	2	M	M REGISTER	r	2	M	M REGISTER	r
NRXX/	13	LN	LOAD N	N,M	3	N	N REGISTER	r	3	N	N REGISTER	r
LR0X/	14 15	JP JP	JUMP TO LOCATIONS 000-1FF (0) PAGE " 100-1FF (1)	L L	4	L	L REG ADDRESSES L "	r	4	L	L REG ADDRESSES L "	r
LRIX/	1C 1D	JP JP	" 200-3FF(2) " 300-3FF(3)	L L	5	K	L REG L REG	r	5	K	L " L "	r
URXX/	16	LU	LOAD U	U	6	U	U REGISTER	r	6	U	U REGISTER	r
CG7X/	17	LS	LOAD SEVEN CONTROL		7		NONE		7	S	U REGISTER ORDERED IN COMMAND	

1	1→D	LITERAL	
15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
OP CODE		DATA	

CONTENTS OF THE EIGHT BIT LITERAL FIELD ARE PLACED IN THE SPECIFIED REGISTER AS INDICATED IN OP CODE

7	f	C	*	r
15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
IØXX		DESIGNATES OPERATION		

CONTROL COMMAND

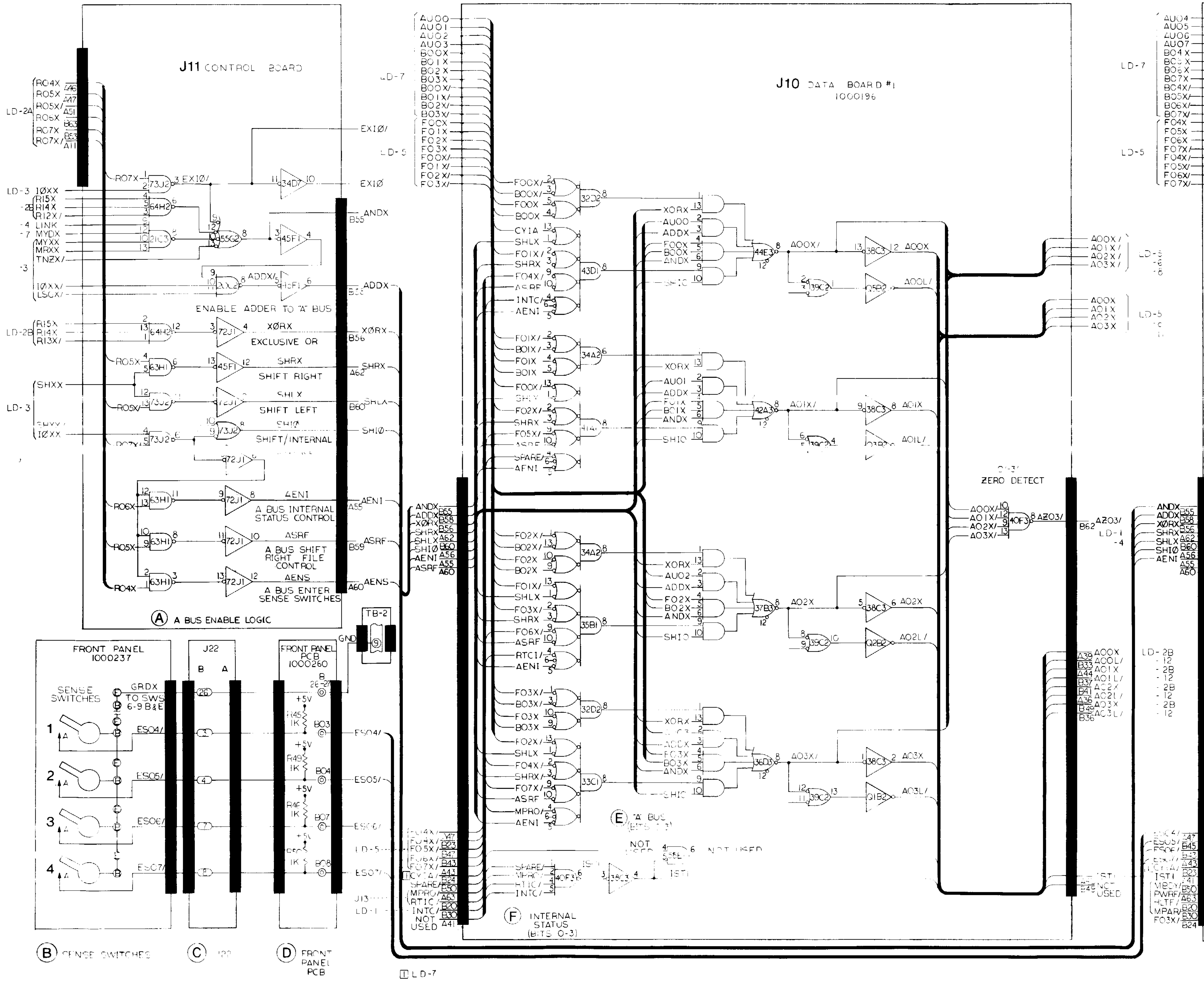
SOURCE DATA FROM f INTERNAL STATUS, CONSOLE SENSE SWITCHES, OR INPUT BUS ARE PLACED IN f (IF*=0) AND REGISTER DESIGNATED BY r

8-F	f	C	*	r
15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
OP CODE				

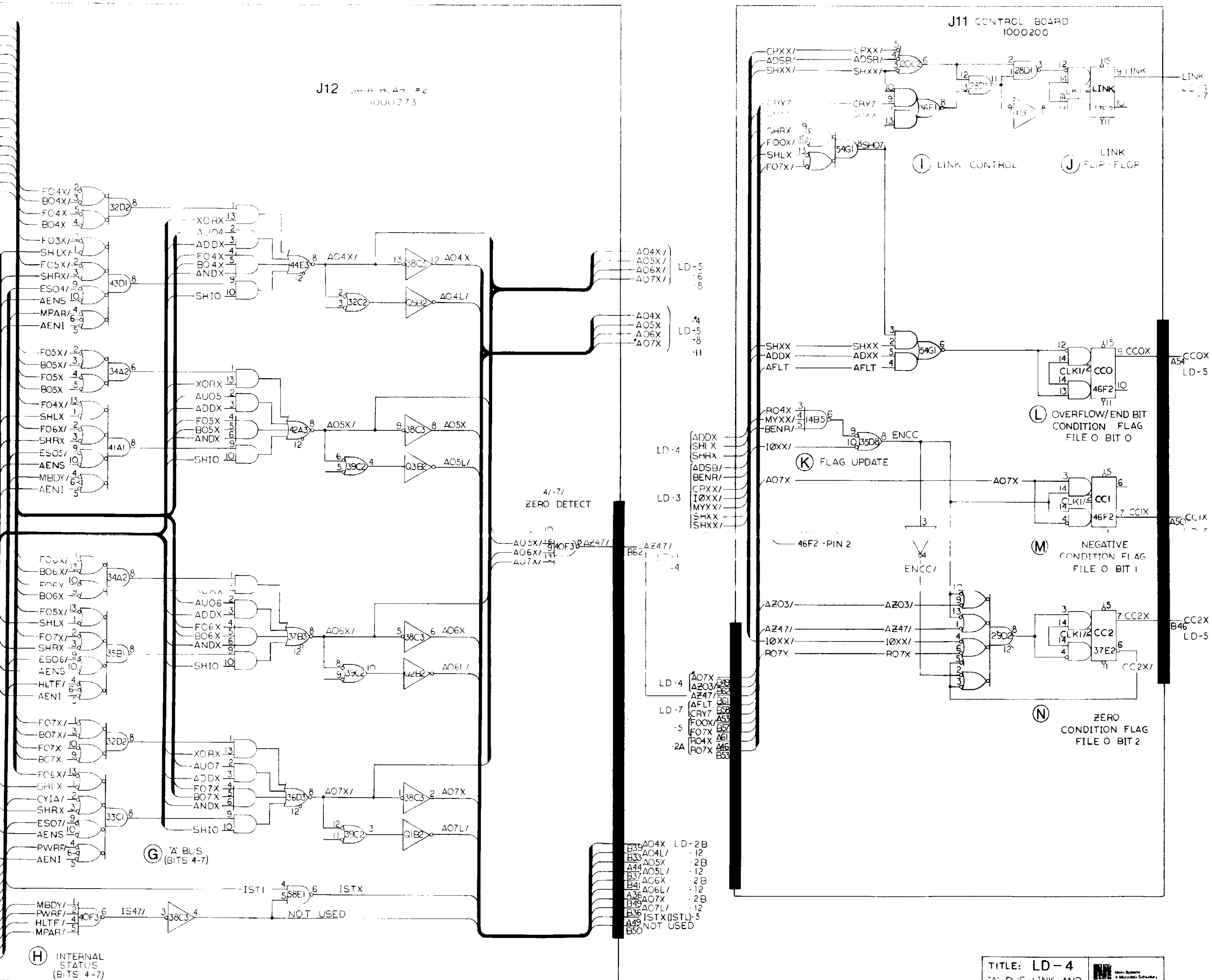
SELECTED OPERAND IS HANDLED WITH CONTENTS OF f. SUM IS PLACED IN f (IF*=0) AND IN REGISTER DESIGNATED BY r

TITLE
LD-3
COMMAND & DESTINATION DECODER

SHEET 4 OF 12 REV



J11 CONTROL BOARD
ENABLE ADDER TO "A" BUS
EXCLUSIVE OR
SHIFT RIGHT
SHIFT LEFT
SHIFT/INTERNAL
A BUS INTERNAL STATUS CONTROL
A BUS SHIFT RIGHT FILE CONTROL
A BUS ENTER SENSE SWITCHES
(A) A BUS ENABLE LOGIC
FRONT PANEL 1000237
SENSE SWITCHES
J22
FRONT PANEL PCB 1000260
TB-2
(B) SENSE SWITCHES
(C) J22
(D) FRONT PANEL PCB
J10 DATA BOARD #1 1000196
ZERO DETECT
(E) "A" BUS
(F) INTERNAL STATUS (BITS 0-3)
NOT USED



TITLE: LD-4

"A" BUS, LINK AND CONDITION CODE FLIP-FLOPS

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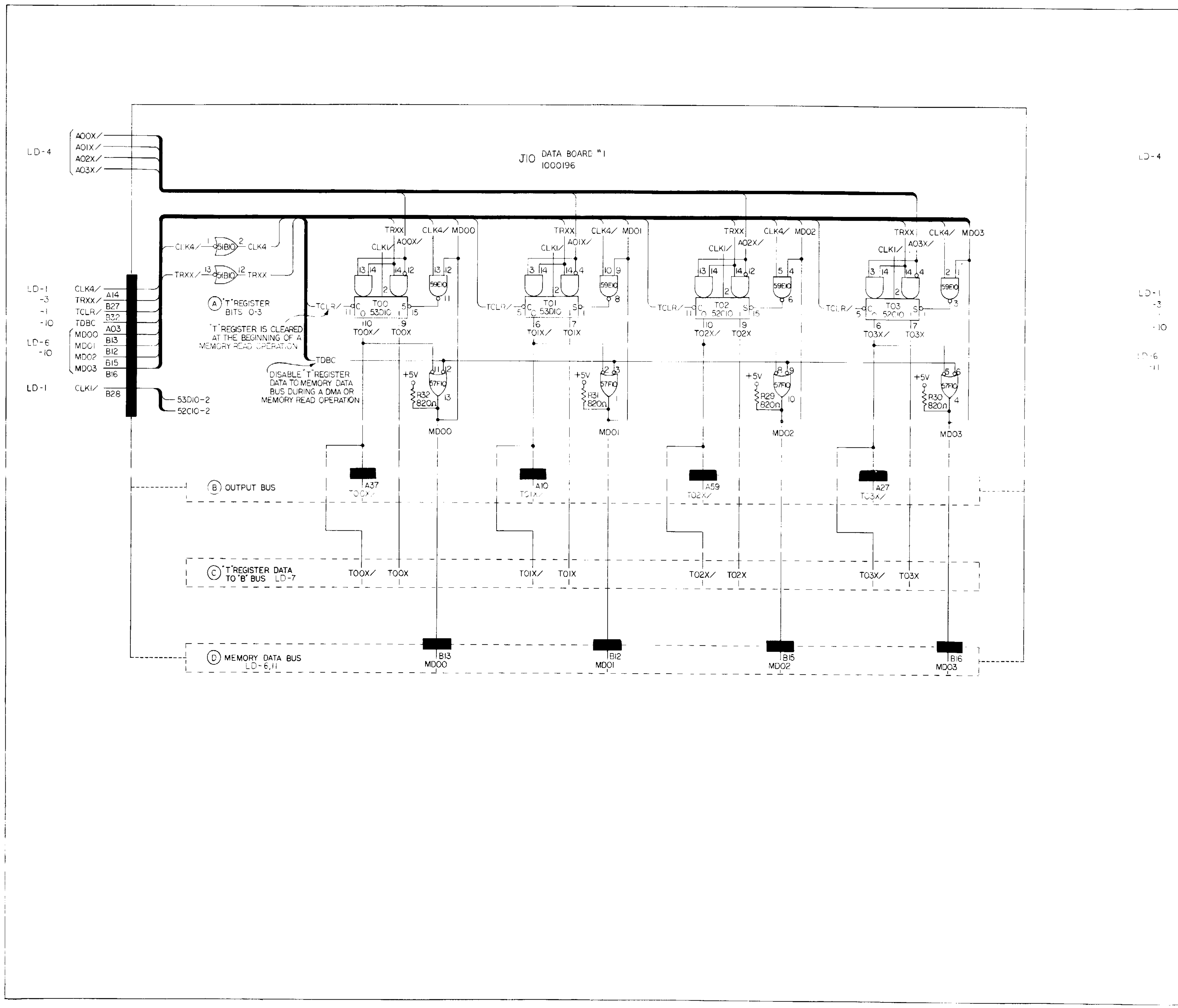
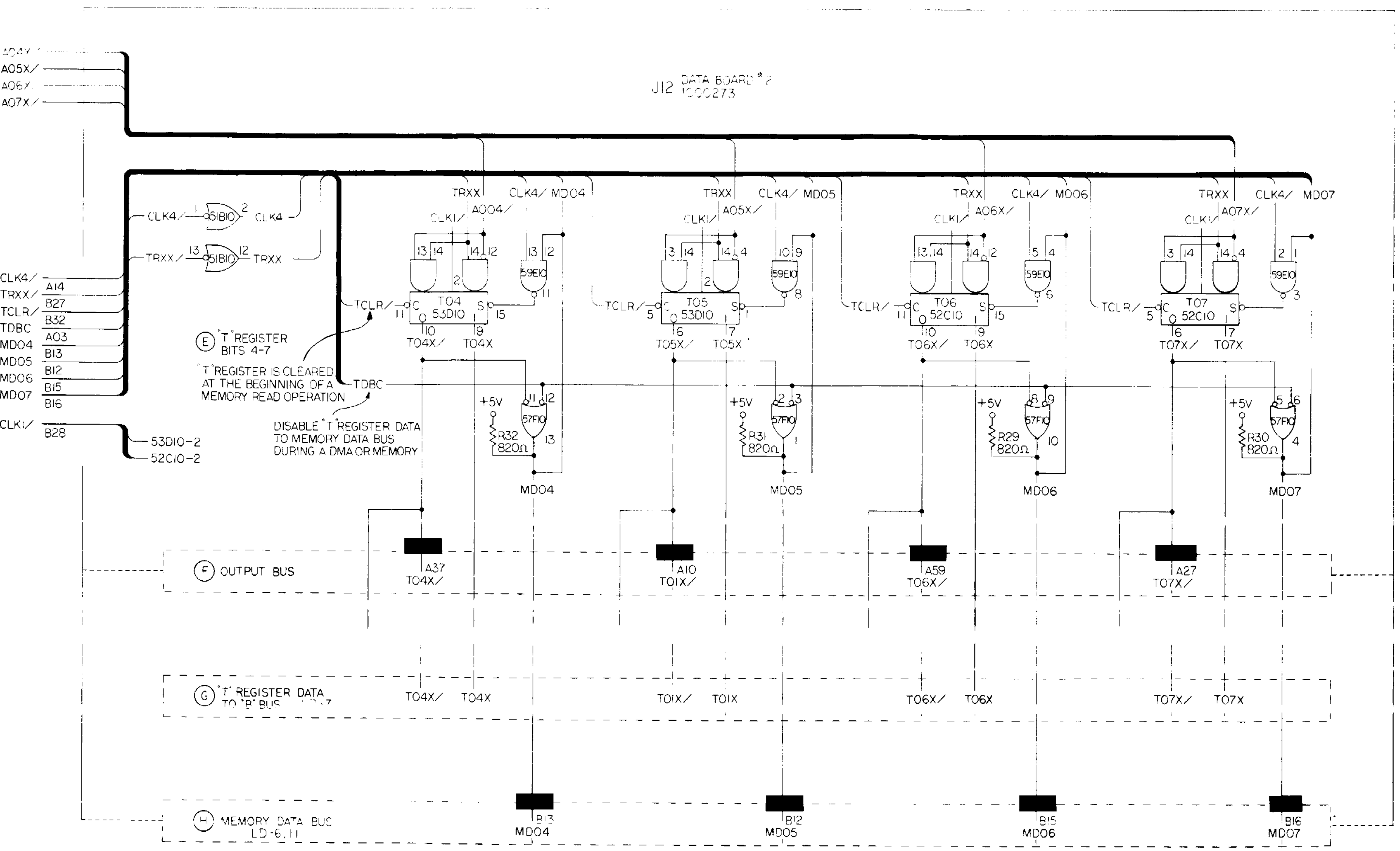
SHEET 5 OF 12 REV



J10 DATA BOARD #1
1000196
LD-4
A00X/
A01X/
A02X/
A03X/
LD-1
-3
-1
-10
LD-6
-10
LD-1
CLK4/ A14
TRXX/ B27
TCLR/ B32
TDBC A03
MD00 B13
MD01 B12
MD02 B15
MD03 B16
CLK1/ B28
53D10-2
52C10-2
(A) 'T' REGISTER BITS 0-3
'T' REGISTER IS CLEARED AT THE BEGINNING OF A MEMORY READ OPERATION
DISABLE 'T' REGISTER DATA TO MEMORY DATA BUS DURING A DMA OR MEMORY READ OPERATION
(B) OUTPUT BUS
(C) 'T' REGISTER DATA TO 'B' BUS LD-7
(D) MEMORY DATA BUS LD-6,11
T00X/ T00X
T01X/ T01X
T02X/ T02X
T03X/ T03X
A37
A10
A59
A27
B13 MD00
B12 MD01
B15 MD02
B16 MD03
+5V
R32 820Ω
R31 820Ω
R29 820Ω
R30 820Ω



TITLE: LD-6
'T' REGISTER

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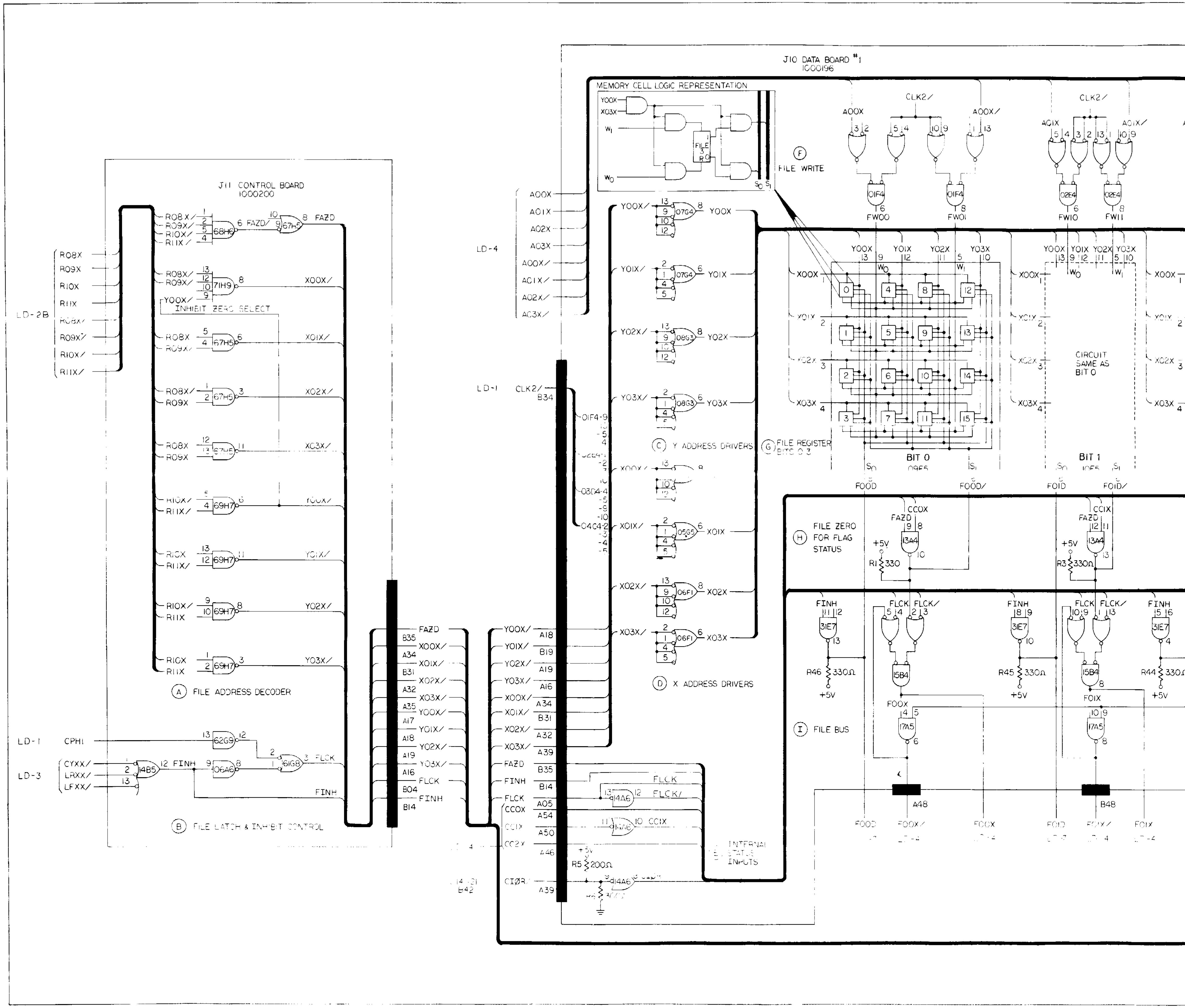
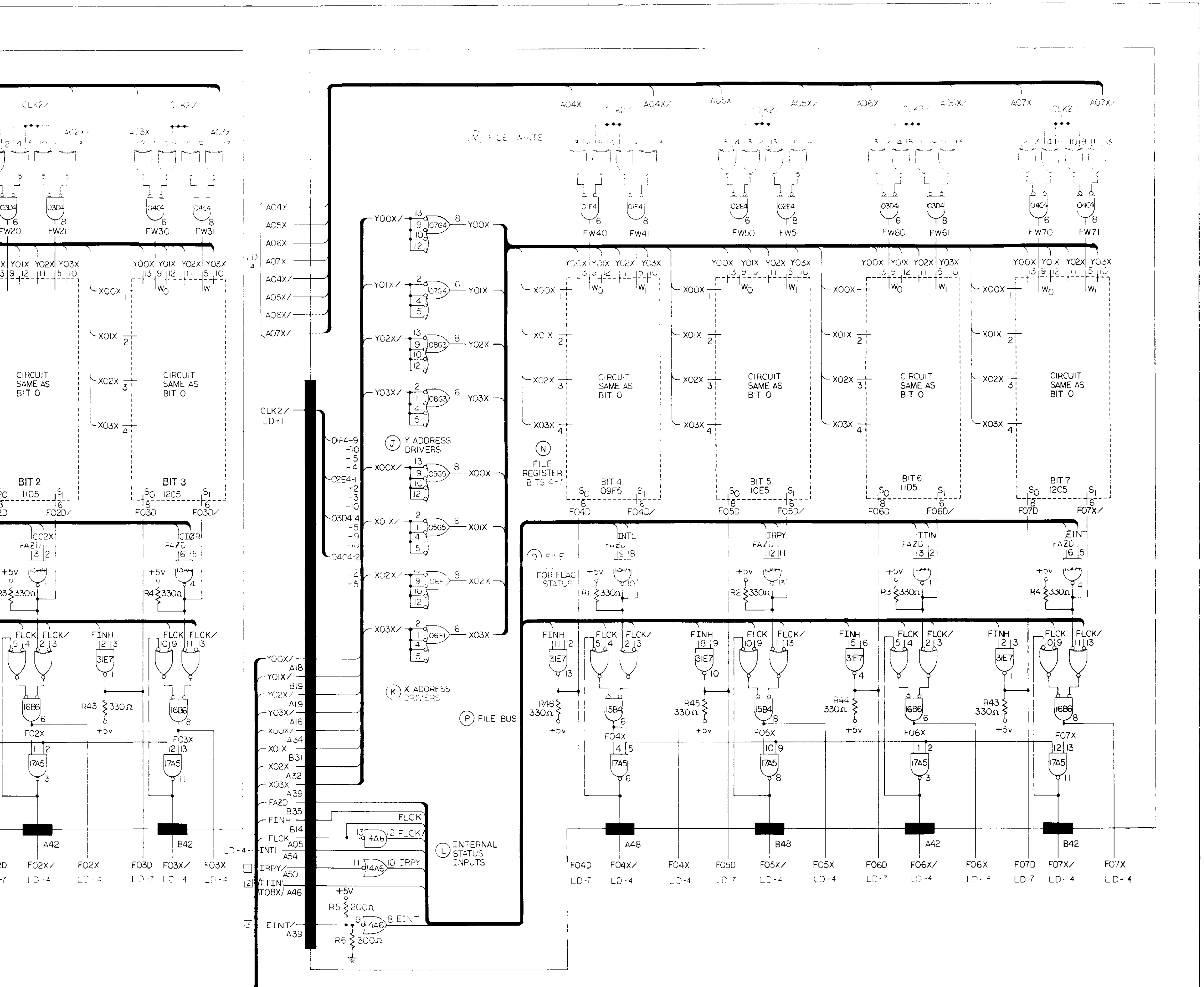
SHEET 7 OF 12 REV



J11 CONTROL BOARD
1000200
(A) FILE ADDRESS DECODER
(B) FILE LATCH & INHIBIT CONTROL
INHIBIT ZERO SELECT
LD-2B
LD-1
LD-3
LD-4
CPHI
FINH
FLCK
FAZD
J10 DATA BOARD #1
1000196
MEMORY CELL LOGIC REPRESENTATION
(F) FILE WRITE
(C) Y ADDRESS DRIVERS
(D) X ADDRESS DRIVERS
(G) FILE REGISTER
BIT 0
BIT 1
CIRCUIT SAME AS BIT 0
(H) FILE ZERO FOR FLAG STATUS
(I) FILE BUS
INTERNAL STATUS INPUTS
CLK2/
FW00
FW01
FW10
FW11



1. J14-21-B50: IO REPLY LINE
2. TELETYPE, SERIAL OR SPARE BIT
3. J14-21-A38: EXTERNAL INTERRUPT J13-A39-40

TITLE LD-5
FILE ADDRESS, DECODER, FILE BUS, & FILE REGISTER

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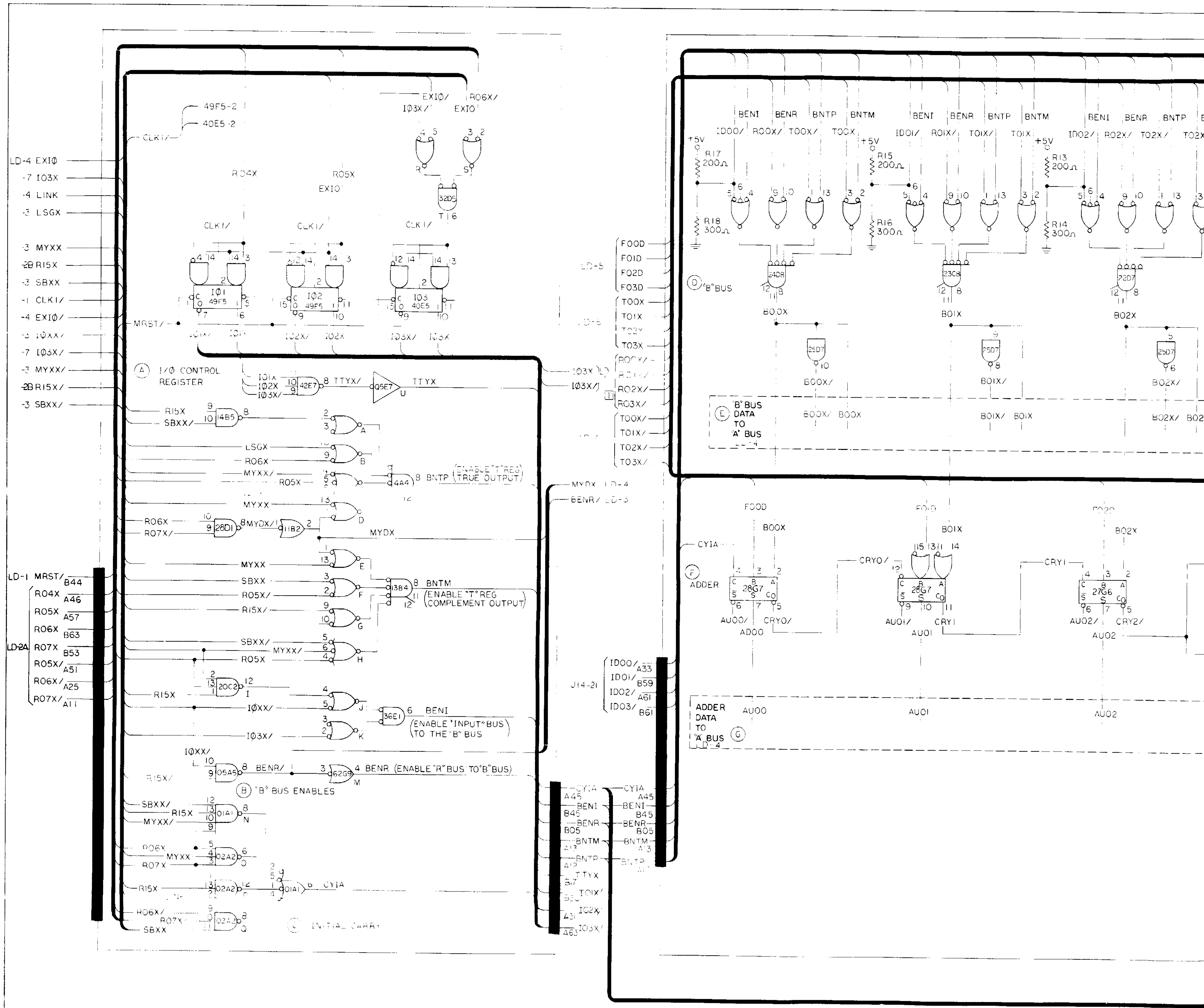
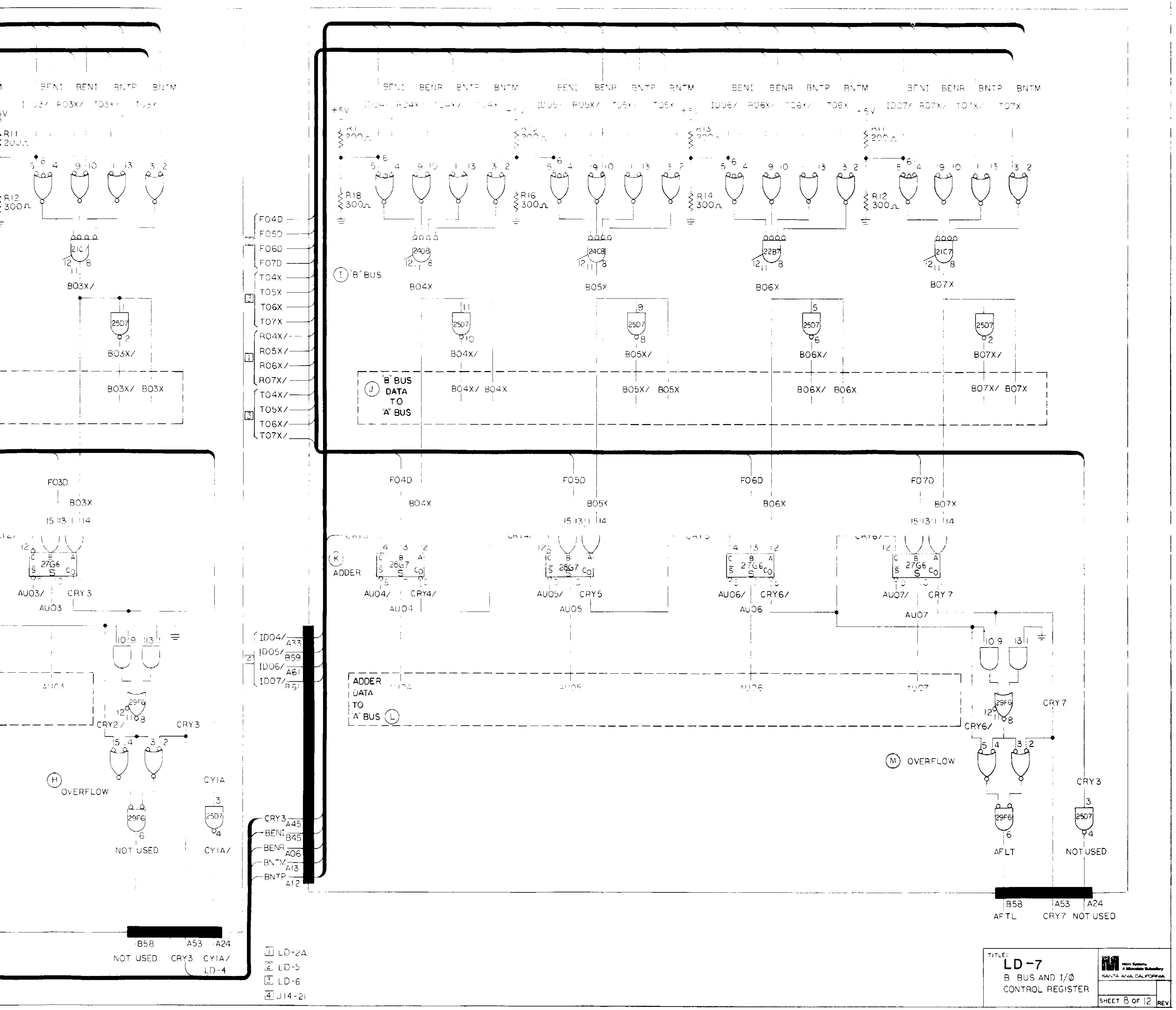
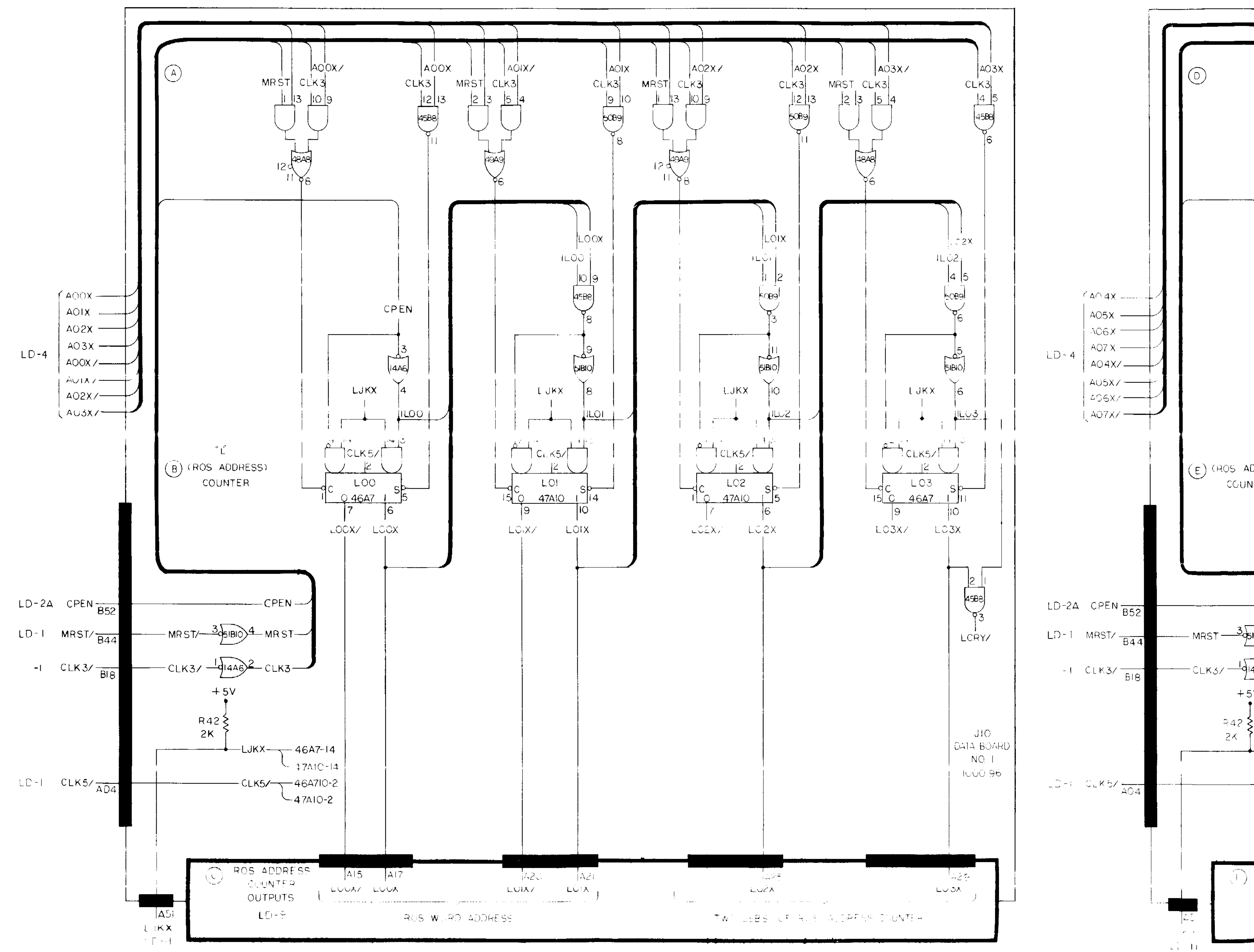
SHEET 6 OF 12 REV


I/Ø CONTROL REGISTER
"B" BUS ENABLES
INITIAL CARRY
"B" BUS
"B" BUS DATA TO "A" BUS
ADDER
ADDER DATA TO "A" BUS
ENABLE "T" REG (TRUE OUTPUT)
ENABLE "T" REG (COMPLEMENT OUTPUT)
ENABLE "INPUT" BUS TO THE "B" BUS
BENR (ENABLE "R" BUS TO "B" BUS)
LD-4 EXIØ
LD-1 MRST/
LD-2A
J14-21
LD-2A

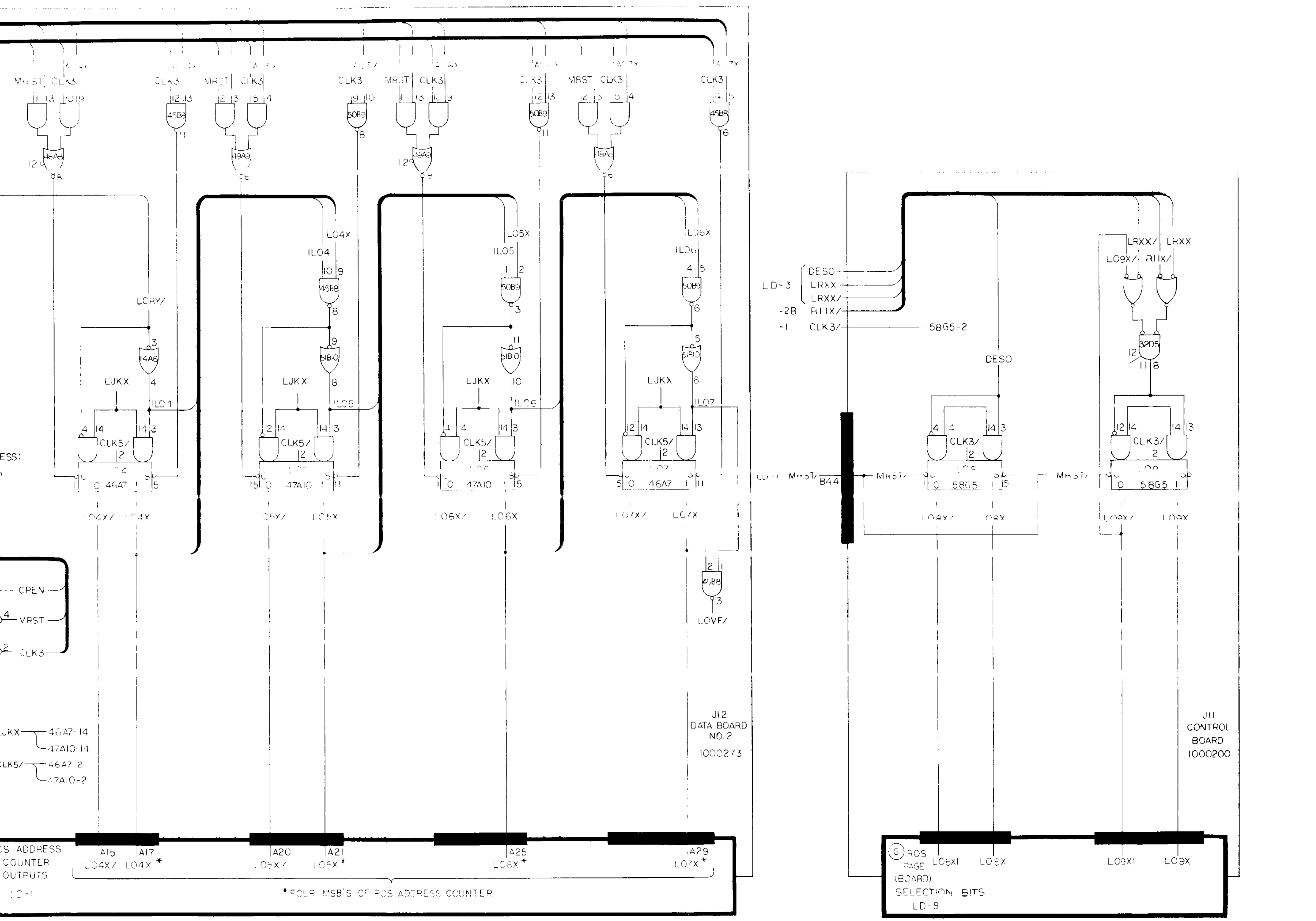


TITLE: LD-7
B BUS AND I/Ø CONTROL REGISTER

SHEET 8 OF 12 REV

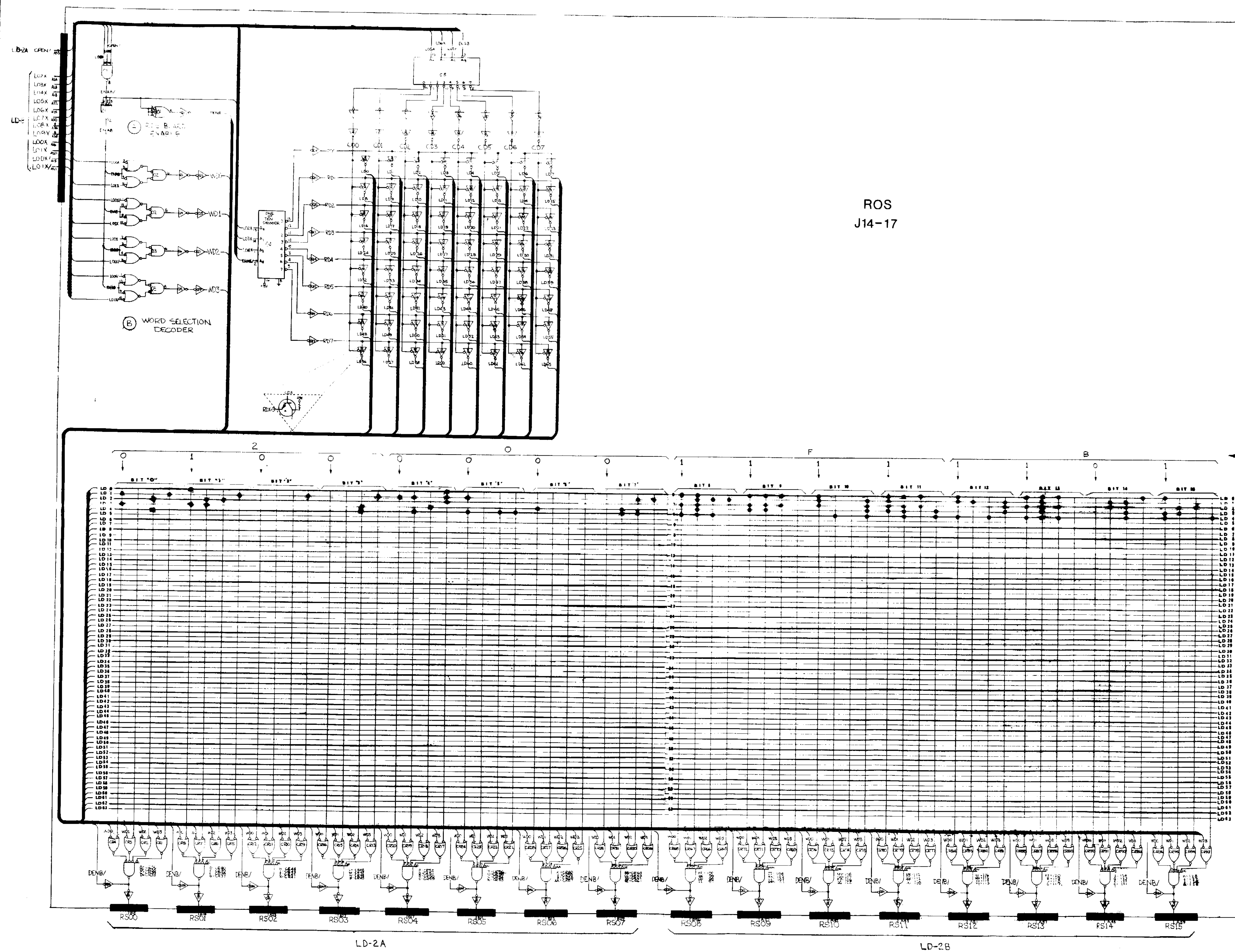


ROS ADDRESS COUNTER
ROS ADDRESS COUNTER OUTPUTS
LD-4
LD-2A CPEN
LD-1 MRST/
LD-1 CLK5/
CLK3/
LJKX
R42 2K
+5V
J10 DATA BOARD NO. 1
LCRY/
ROS WORD ADDRESS



TITLE: LD-8
'L' (ROS ADDRESS)
COUNTER

REV



REPRESENTS ONE DIODE AT THE POINT OF THE INTERSECTION, WHICH RESULTS IN A "ONE" AT THAT BIT POSITION. NO DIODE, RESULTS IN A "ZERO" AT THAT BIT POSITION.

ILLUSTRATED IN THIS DIAGRAM IS THE FIRST TWENTY INSTRUCTIONS OF A TYPICAL MICRO-PROGRAM AS LISTED BELOW:

* Read Next Instruction

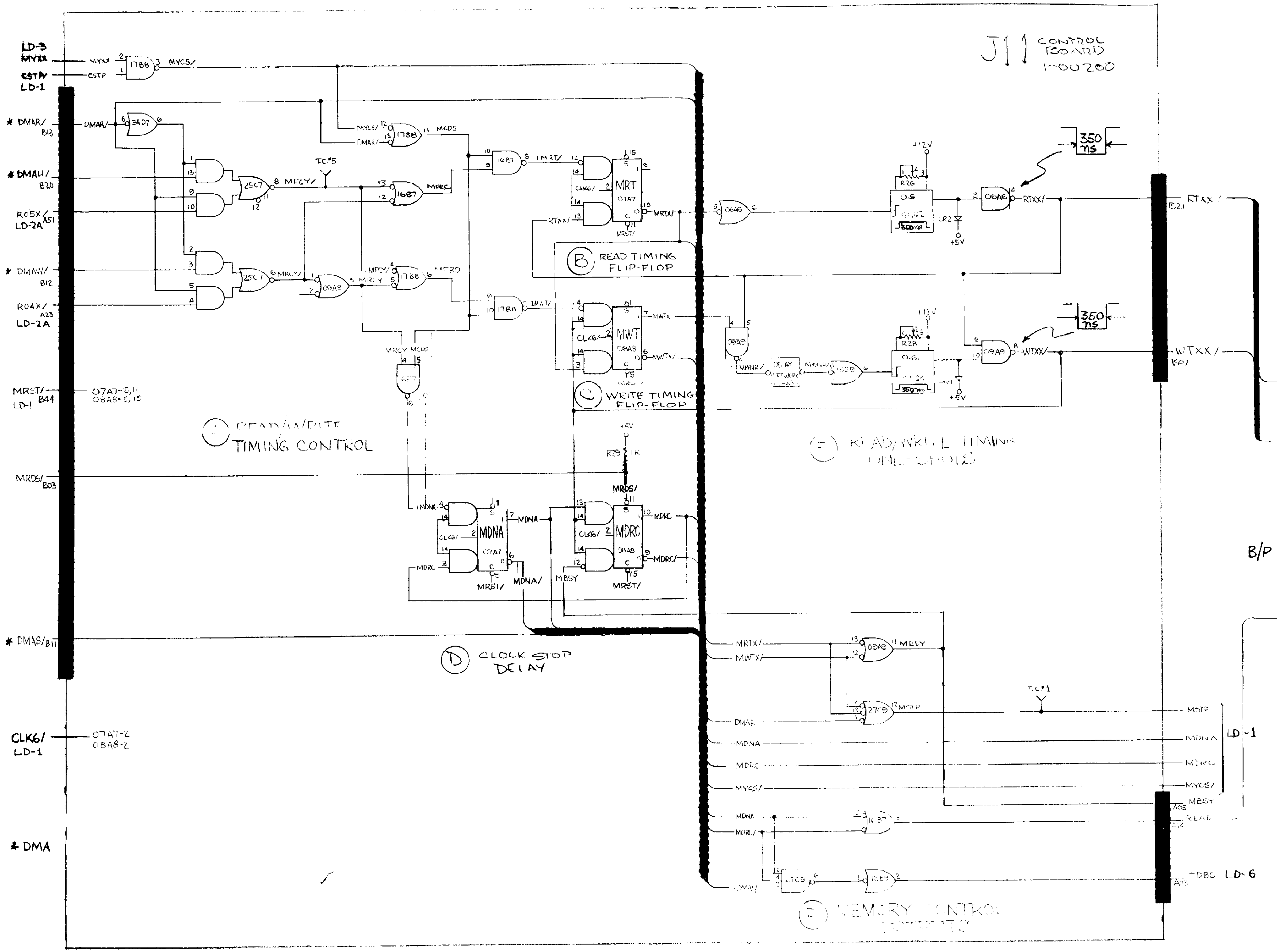
ROS ADDRESS	ROS DATA				
000	BF02	RNI0	CM	OV	Clear OV/W and M
001	2B00		LF	PH,X'00'	Clear P
002	2A00		LF	PL,X'00'	
003	4010		TZ	F0,X'10'	Internal Interrupt
004	13F8		JP	INT2	Yes
005	7110		K	I,1	Enter Sense Switches
006	4180		TZ	I,X'80'	Switch 4 on
007	[illegible]		JP	[illegible]	Yes, Load Boot Strap
008	2F00	RNI1	LF	OV,X'00'	Clear OV/W
009	[illegible]	RNI5	MM	PU	
00A	[illegible]	RNI4	RN	PL	Get OP Code
00B	1410		JP	RNI6	Ignore Interrupts
00C	5A43	RNI	IN	PL	Update P
00D	A982	RNI3	RM	PU,L	
00E	4098	RNI2	TZ	F0,X'98'	Test for Interrupts
00F	1505		JP	INT	Service Request
[illegible]	[illegible]	RNI6	[illegible]	I,T	Save OP Code
[illegible]	[illegible]		LF	[illegible]	Base Address of Table
01[illegible]	[illegible]		KT*	[illegible]	Shift Right 4
[illegible]	[illegible]		A	[illegible]	
[illegible]	[illegible]		CP	[illegible]	Memory Reference
[illegible]	[illegible]		MK	[illegible]	No

* Yes, Get Operand Address

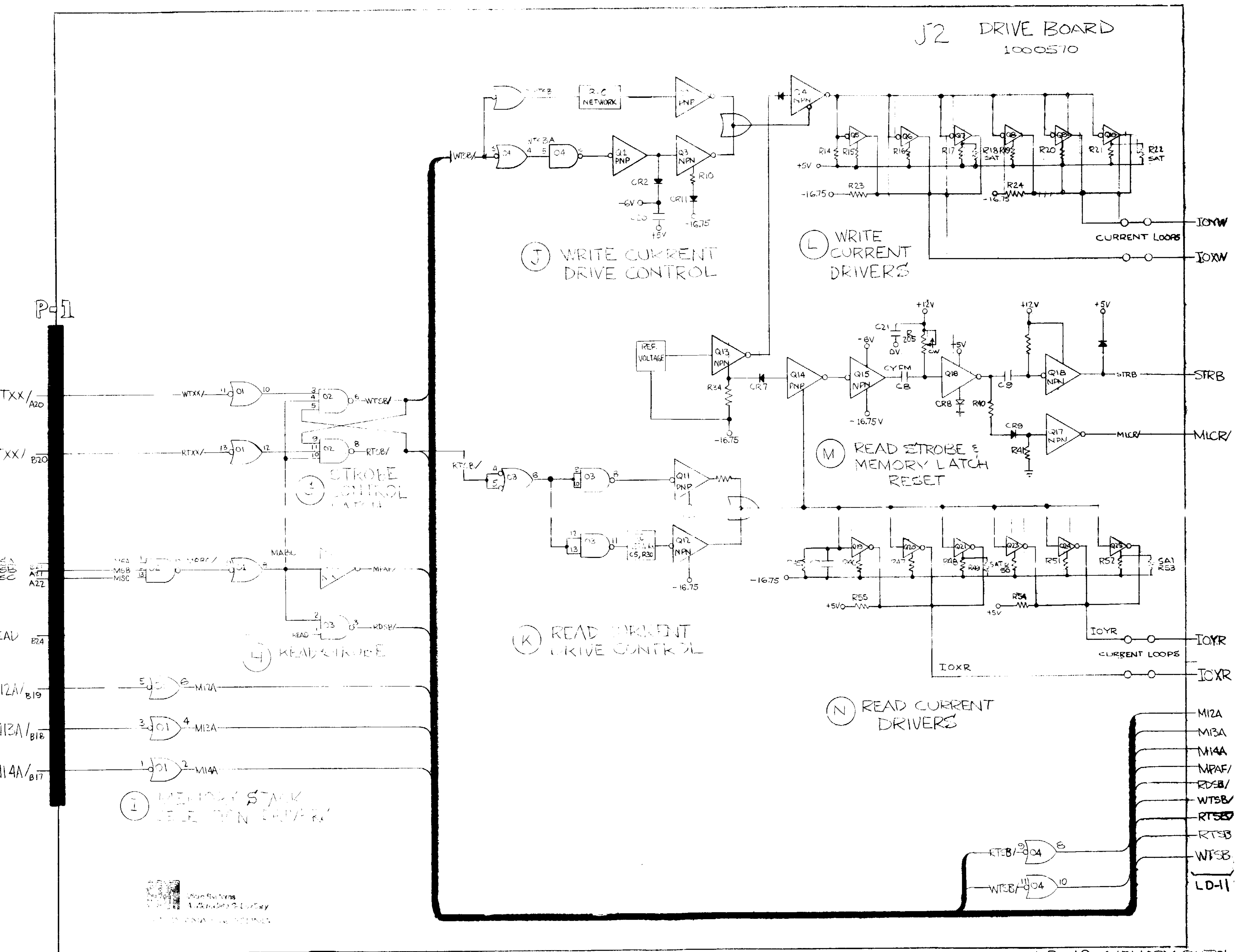
TITLE: LD - 9
ROS LOGIC

SANTA ANA, CALIFORNIA

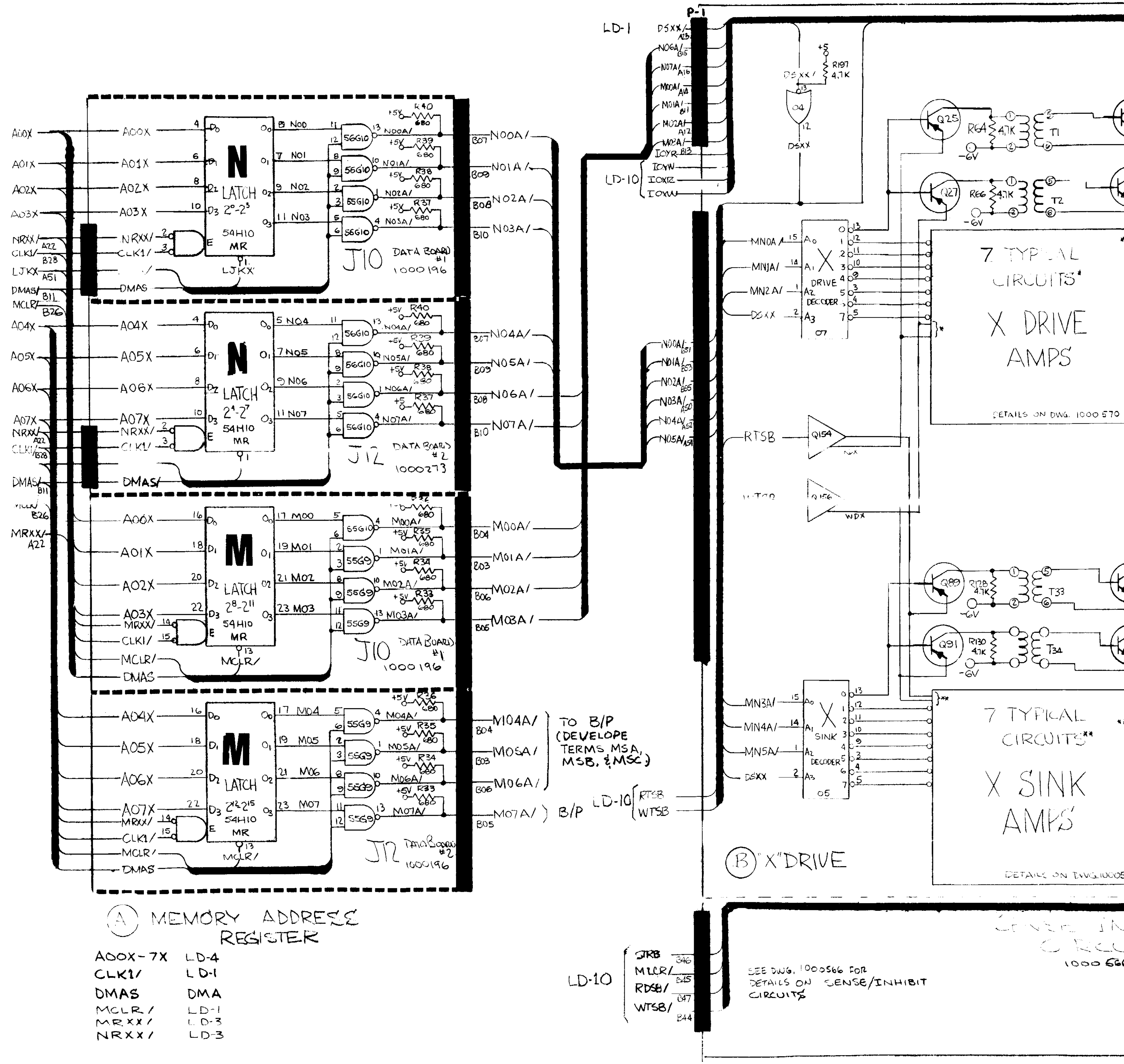
SHEET 10 OF 12 REV

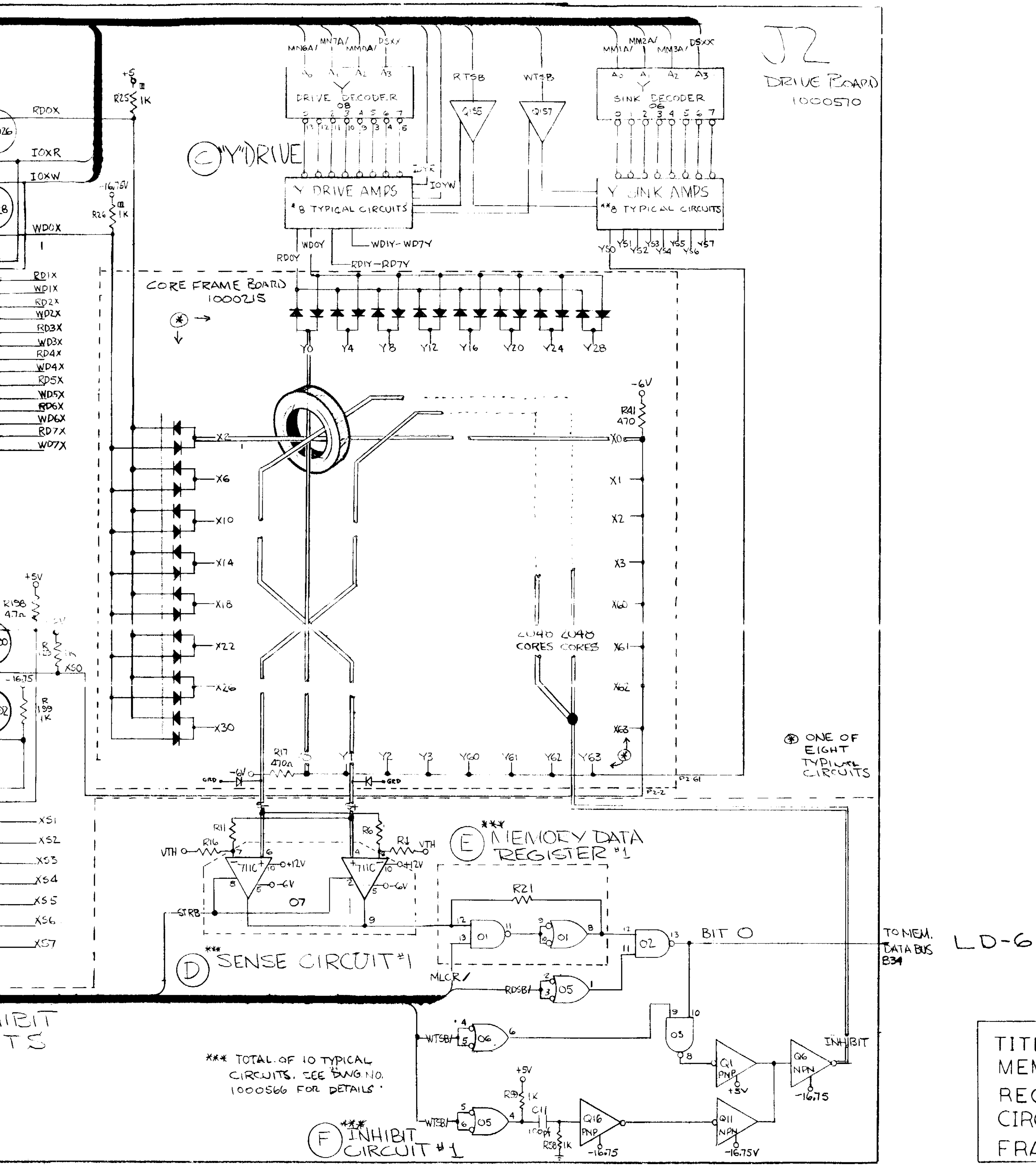


J11 CONTROL BOARD 1-00200
READ TIMING FLIP-FLOP
WRITE TIMING FLIP-FLOP
TIMING CONTROL
CLOCK STOP DELAY
350 ns
B/P
LD-1
LD-6



LD-10 MEMORY CONTROL

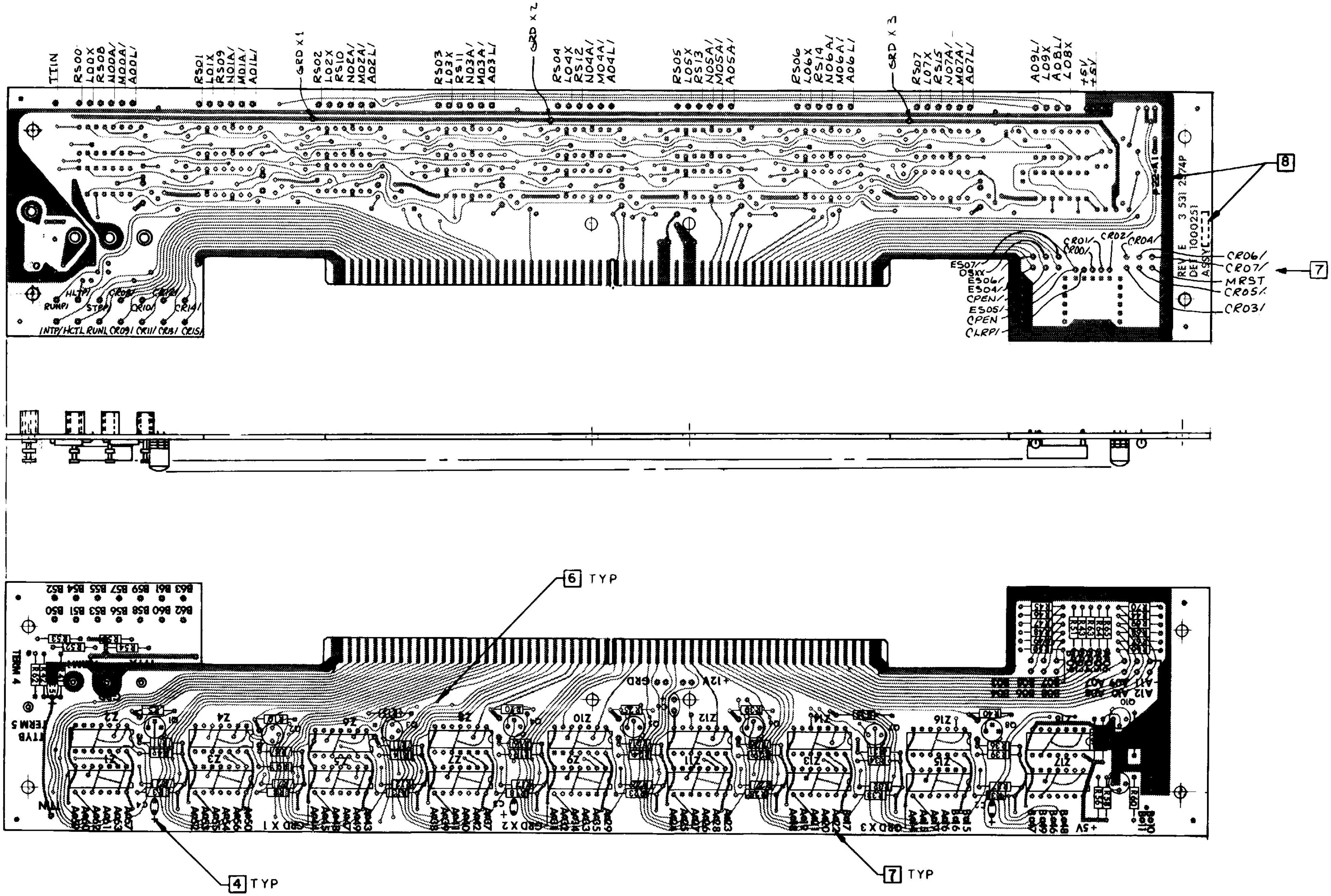

A MEMORY ADDRESS REGISTER
A00X-7X LD-4
CLK1/ LD-1
DMAS DMA
MCLR/ LD-1
MRXX/ LD-3
NRXX/ LD-3
N LATCH 2°-2³ 54H10 MR
N LATCH 2⁴-2⁷ 54H10 MR
M LATCH 2⁸-2¹¹ 54H10 MR
M LATCH 2¹²-2¹⁵ 54H10 MR
J10 DATA BOARD #1 1000196
J12 DATA BOARD #2 1000273
J10 DATA BOARD #1 1000196
J12 DATA BOARD #2 1000196
TO B/P (DEVELOPE TERMS MSA, MSB, & MSC)
B/P
LD-1
LD-10
P-1
B "X" DRIVE
X DRIVE DECODER
X SINK DECODER
7 TYPICAL CIRCUITS* X DRIVE AMPS
DETAILS ON DWG. 1000570
7 TYPICAL CIRCUITS** X SINK AMPS
SEE DWG. 1000566 FOR DETAILS ON SENSE/INHIBIT CIRCUITS



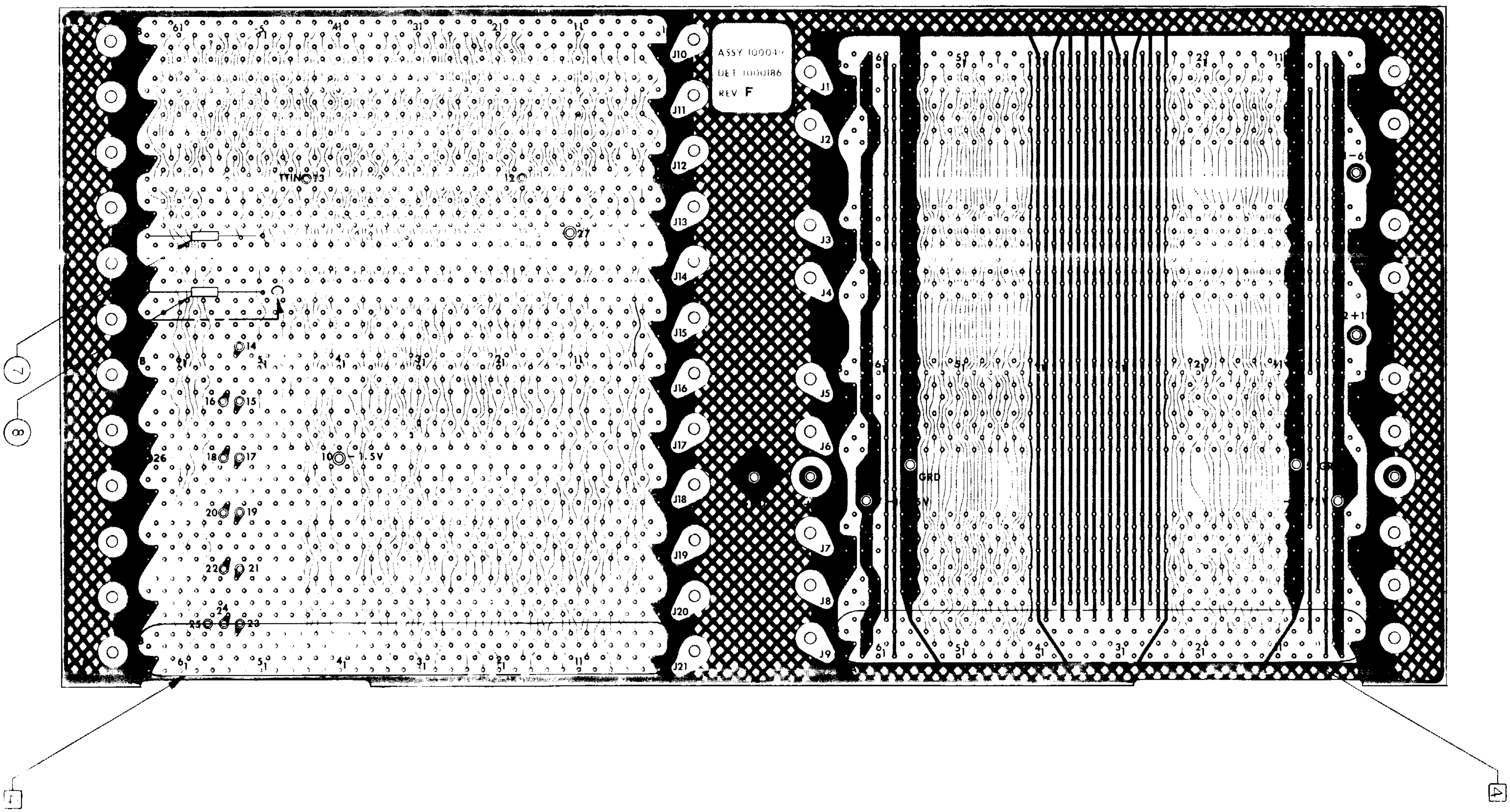
TITLE: LD-11
MEMORY ADDRESS REGISTER, DRIVE CIRCUITS, AND CORE FRAME BOARD

Micro Systems
A Microdata Subsidiary
SANTA ANA, CALIFORNIA

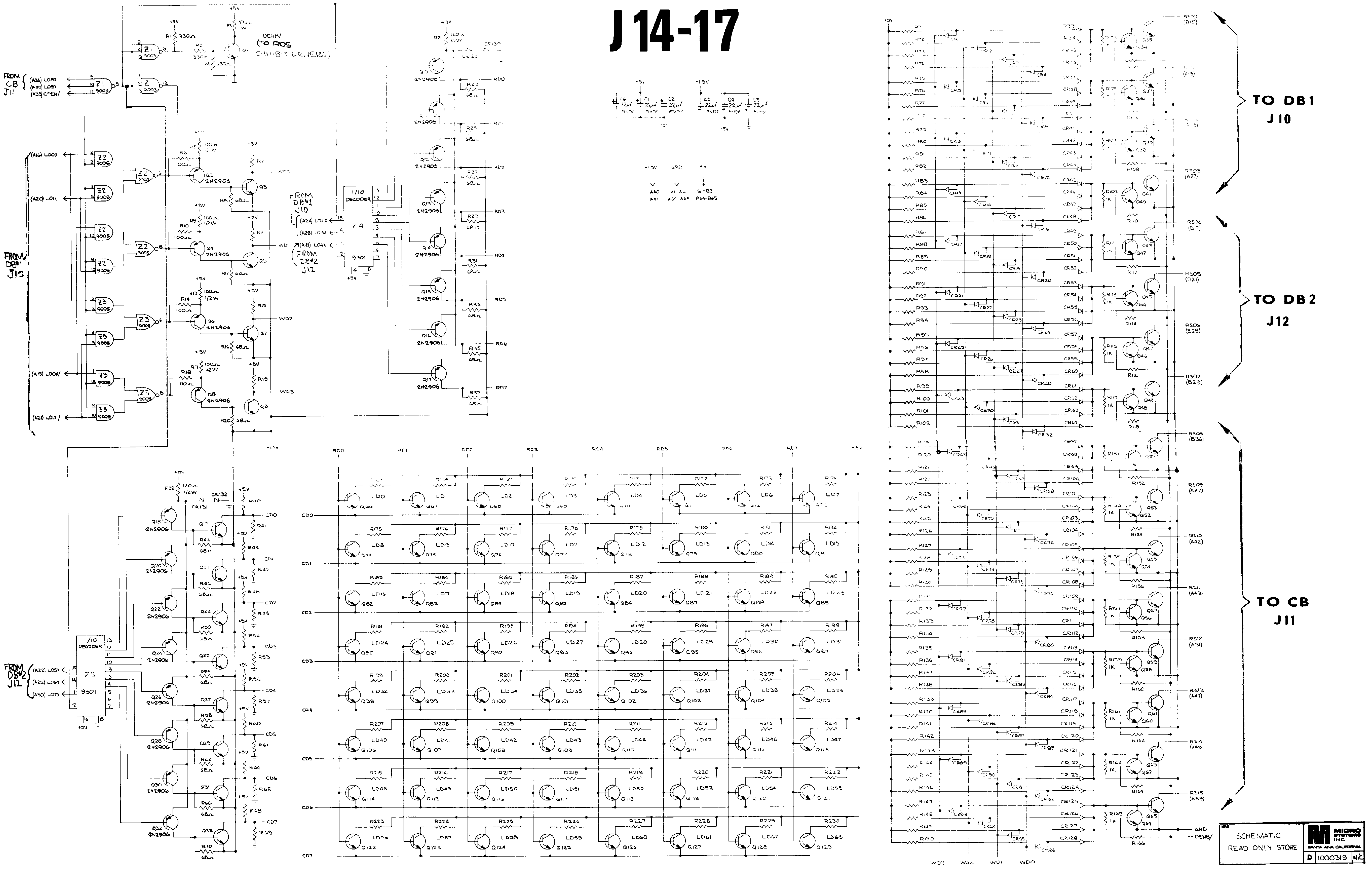
SHEET 11 OF 12 | REV



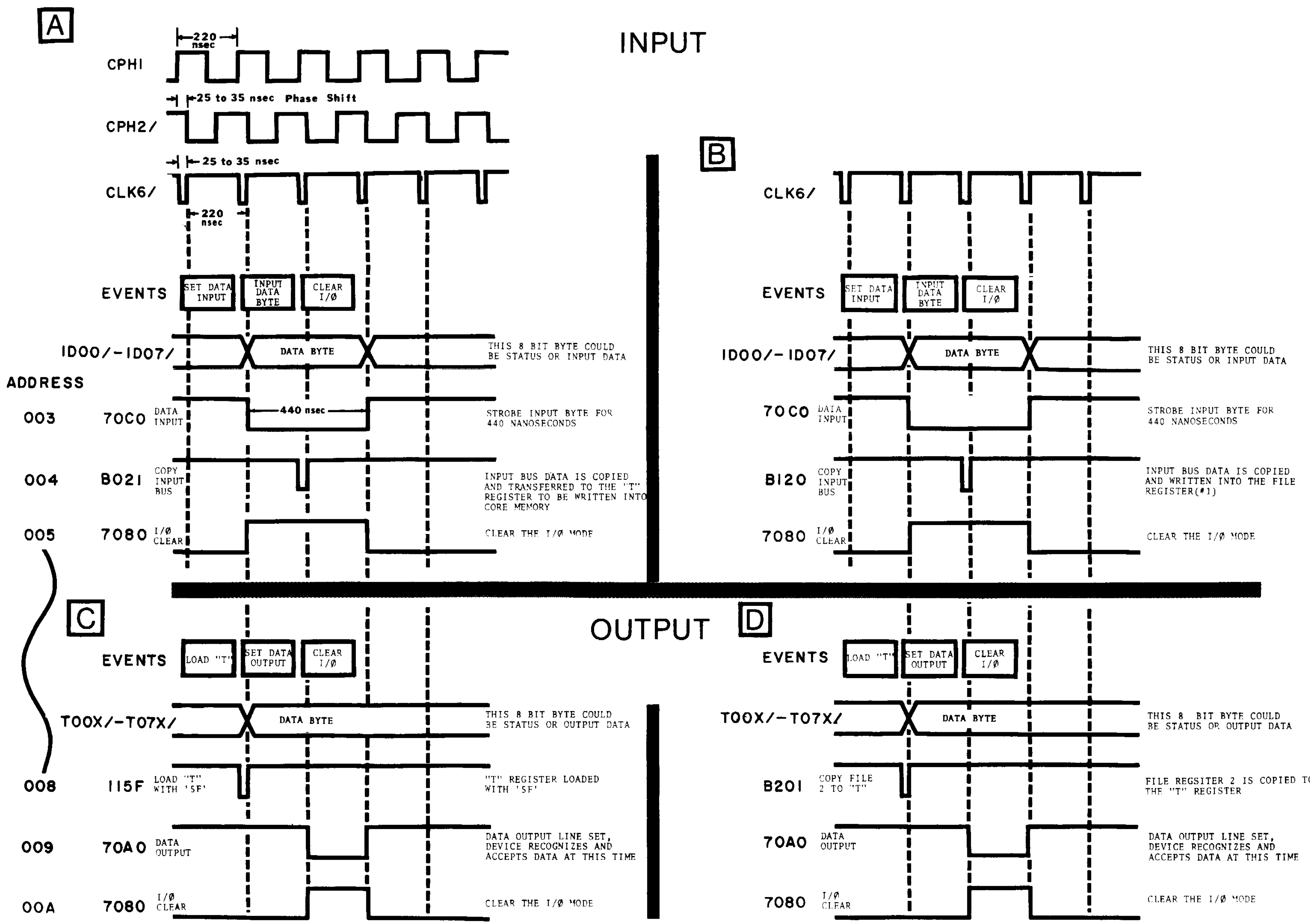
TTIN
RS00 L00X RS08 N00A/ M00A/ A00L/
RS01 L01X RS09 N01A/ M01A/ A01L/
GRD X1
RS02 L02X RS10 N02A/ M02A/ A02L/
RS03 L03X RS11 N03A/ M03A/ A03L/
GRD X2
RS04 L04X RS12 N04A/ M04A/ A04L/
RS05 L05X RS13 N05A/ M05A/ A05A/
RS06 L06X RS14 N06A/ M06A/ A06L/
GRD X3
RS07 L07X RS15 N07A/ M07A/ A07L/
A09L/ L09X A08L/ L08X
+5V +5V
8
CR01/ CR00/ CR02 CR04/
CR06/ CR07/ MRST CR05/ CR03/
7
ES07/ DSXX ES06/ ES04/ CPEN/ ES05/ CPEN CLRP/
HLTP/ RUNP/ STPP/ CR08/ CR10/ CR12/ CR14/
INTP/ HCTL RUNL CR09/ CR11/ CR13/ CR15/
REV E
6 TYP
4 TYP
7 TYP
GRD
+12V
+5V
GRD X1
GRD X2
GRD X3
Z2 Z4 Z6 Z8 Z10 Z12 Z14 Z16


ASSY 1000419
DET 1000186
REV F
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J17
J18
J19
J20
J21
GRD
-1.5V
TTINO13
27
26
7
8
4

J14-17

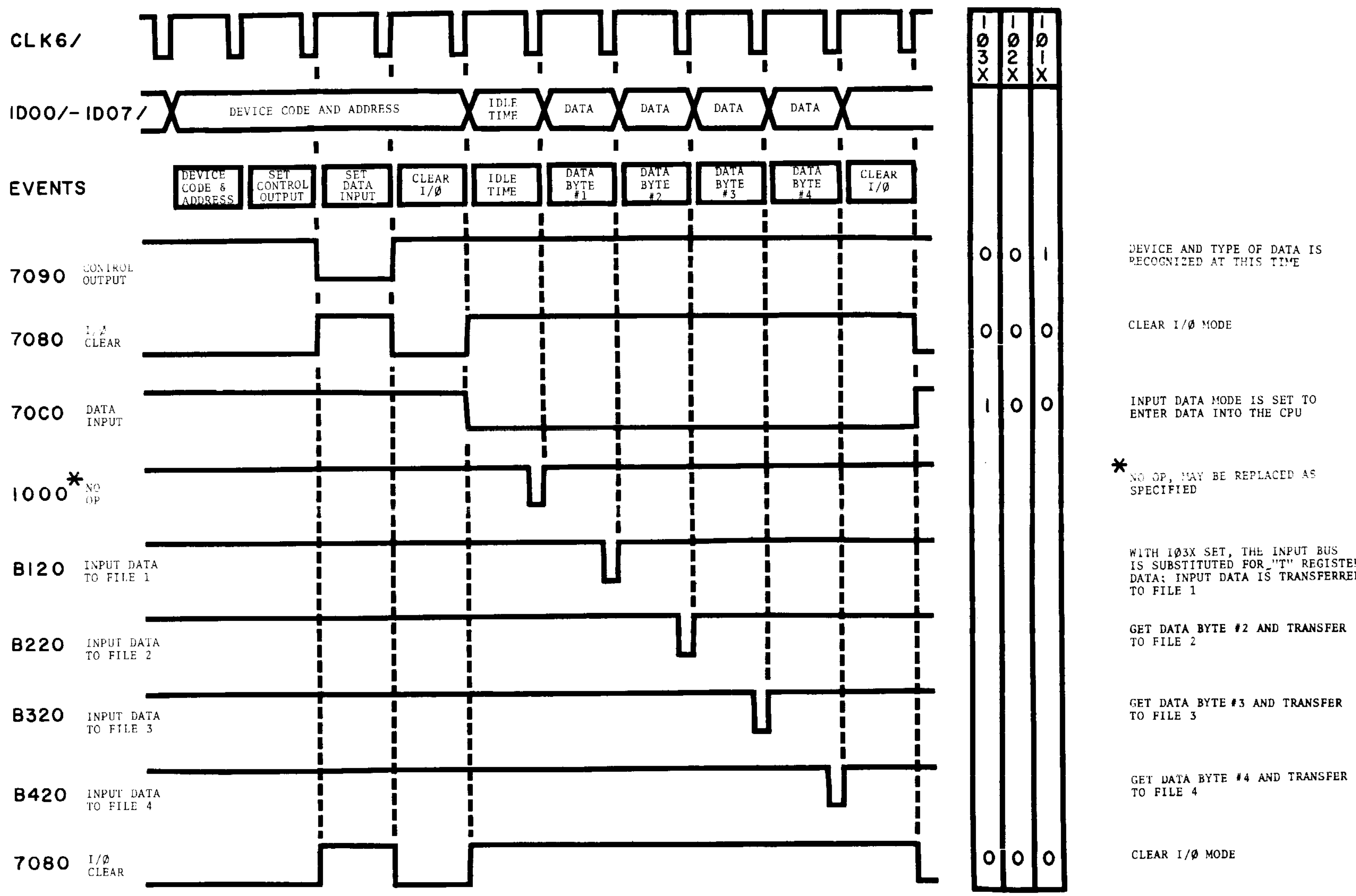


FROM CB J11
FROM DB#1 J10
FROM DB#2 J12
DENB/ (TO ROS INHIBIT DRIVERS)
1/10 DECODER Z4 9301
1/10 DECODER Z5 9301
TO DB1 J10
TO DB2 J12
TO CB J11
SCHEMATIC
READ ONLY STORE
MICRO SYSTEMS INC.
SANTA ANA CALIFORNIA
D 1000319 N/C



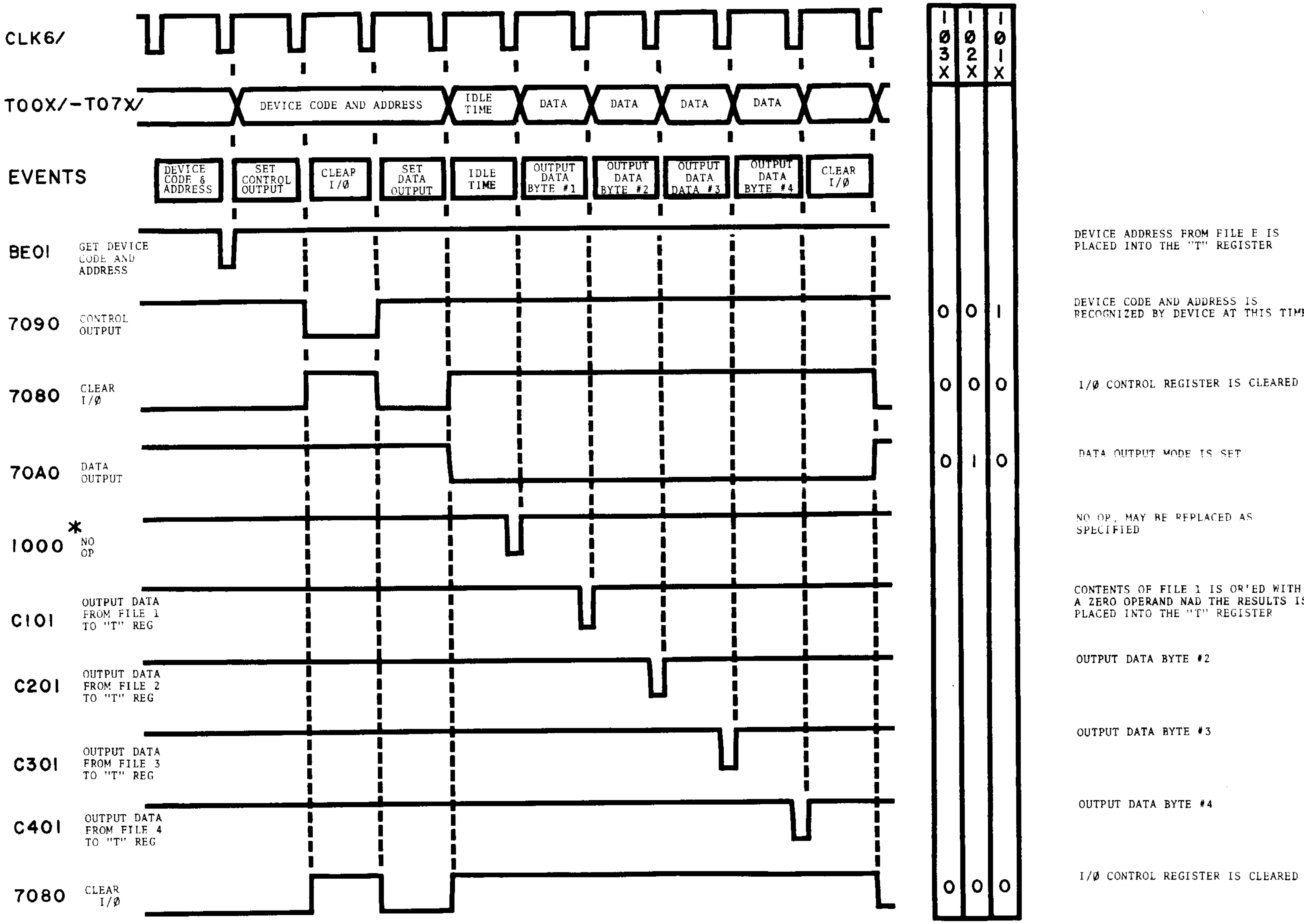
A
INPUT
CPHI
220 nsec
25 to 35 nsec Phase Shift
CPH2/
25 to 35 nsec
CLK6/
220 nsec
EVENTS
SET DATA INPUT
INPUT DATA BYTE
CLEAR I/Ø
ID00/-ID07/
DATA BYTE
THIS 8 BIT BYTE COULD BE STATUS OR INPUT DATA
ADDRESS
003 70C0 DATA INPUT
440 nsec
STROBE INPUT BYTE FOR 440 NANOSECONDS
004 B021 COPY INPUT BUS
INPUT BUS DATA IS COPIED AND TRANSFERRED TO THE "T" REGISTER TO BE WRITTEN INTO CORE MEMORY
005 7080 I/Ø CLEAR
CLEAR THE I/Ø MODE
B
CLK6/
EVENTS
SET DATA INPUT
INPUT DATA BYTE
CLEAR I/Ø
ID00/-ID07/
DATA BYTE
THIS 8 BIT BYTE COULD BE STATUS OR INPUT DATA
70C0 DATA INPUT
STROBE INPUT BYTE FOR 440 NANOSECONDS
B120 COPY INPUT BUS
INPUT BUS DATA IS COPIED AND WRITTEN INTO THE FILE REGISTER(#1)
7080 I/Ø CLEAR
CLEAR THE I/Ø MODE
OUTPUT
C
EVENTS
LOAD "T"
SET DATA OUTPUT
CLEAR I/Ø
T00X/-T07X/
DATA BYTE
THIS 8 BIT BYTE COULD BE STATUS OR OUTPUT DATA
008 115F LOAD "T" WITH '5F'
"T" REGISTER LOADED WITH '5F'
009 70A0 DATA OUTPUT
DATA OUTPUT LINE SET, DEVICE RECOGNIZES AND ACCEPTS DATA AT THIS TIME
00A 7080 I/Ø CLEAR
CLEAR THE I/Ø MODE
D
EVENTS
LOAD "T"
SET DATA OUTPUT
CLEAR I/Ø
T00X/-T07X/
DATA BYTE
THIS 8 BIT BYTE COULD BE STATUS OR OUTPUT DATA
B201 COPY FILE 2 TO "T"
FILE REGSITER 2 IS COPIED TO THE "T" REGISTER
70A0 DATA OUTPUT
DATA OUTPUT LINE SET, DEVICE RECOGNIZES AND ACCEPTS DATA AT THIS TIME
7080 I/Ø CLEAR
CLEAR THE I/Ø MODE

FIGURE 6



*ANY COMMAND THAT DOES NOT AFFECT AN I/Ø OPERATION OR SELECT THE "T" REGISTER OUTPUT FOR AN OPERAND. USE OF HOUSEKEEPING INSTRUCTIONS MAY BE EMPLOYED SUCH AS ADD TO FILE, ETC. DEPENDING UPON USER REQUIREMENTS, THIS IDLE TIME MAY NOT BE NECESSARY. IN THIS EXAMPLE, IF THE "NO OP" WERE TO BE REMOVED, THE PULSE WIDTH OF IØ3X WOULD BE SHORTER BY ONE CLOCK CYCLE.

FIGURE 7



* ANY COMMAND THAT DOES NOT AFFECT AN I/Ø OPERATION OR SELECT THE "T" REGISTER OUTPUT FOR AN OPERAND. USE OF HOUSEKEEPING INSTRUCTIONS MAY BE EMPLOYED SUCH AS ADD TO FILE, ETC. DEPENDING UPON USER REQUIREMENTS, THIS IDLE TIME MAY NOT BE NECESSARY. IN THIS EXAMPLE, IF THE "NO OP" WERE TO BE REMOVED, THE PULSE WIDTH OF IØ3X WOULD BE SHORTER BY ONE CYCLE.

FIGURE 8