VME SCSI/X Host Adapter

Hardware Specification 1.1

July 13, 1987

1.0 Features

The VME-SCSI/X will incorporate several advanced features.

* VME DMA data transfers will occur at 30 + megabytes per second.

* Synchronous and asynchronous SCSI data occur at 4 and 1.5 megabytes per second respectively.

* SCSI interface and control is achieved using the NCR 53C90 VLSI controller chip. The 53C90 device is capable of supporting 3 MByte/sec asynchronous, 4.8 MByte/sec synchronous data transfers across the SCSI bus. The enhanced transfer rates should support future changes to the ANSI SCSI specification.

* 64 KBytes (128 KBytes optional) of dual-ported **static** RAM are available for buffering data during simultaneous transfers **to or from** the VMEbus **and** SCSI bus.

* 4 KBytes of dual-ported scratchpad RAM are available for the resident 68000 CPU and the Host CPU. Control of the SCSI/X card by the Host, is achieved through this block of RAM.

* Eight diagnostic LED's are located on board. The LED's are used to indicate SCSI and VME bus status.

* The VME-SCSI Host Adapter will support EPROMS of the 27128, 27256, and 27512 variety with access times of 250 nS.

VME-SCSI/X Block Diagram

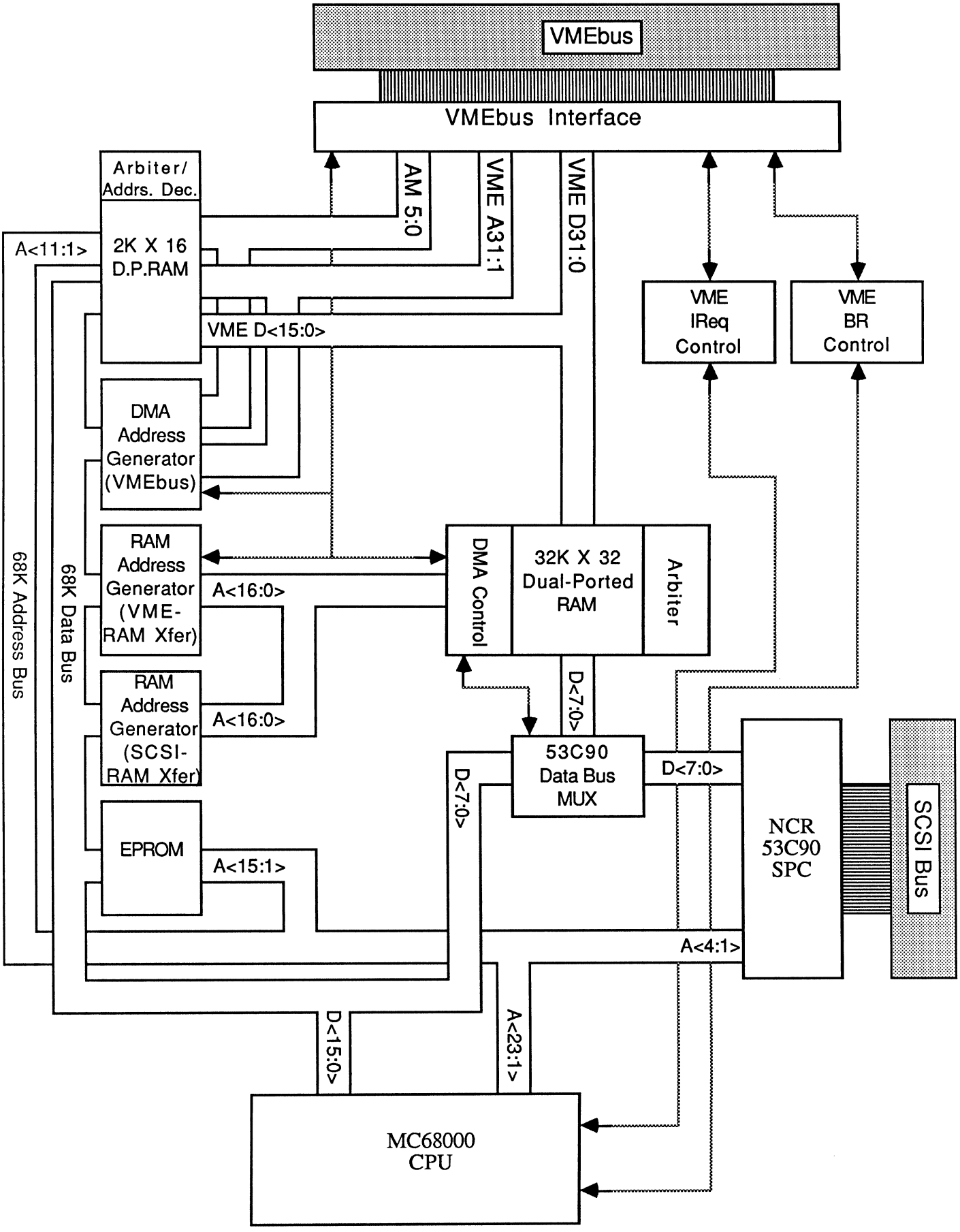


TABLE 1
VME-SCSI/X Memory Map

Function Description	Address Range
EPROM	0x000000 - 0x00FFFE
Dual-ported Scratchpad RAM	0x010000 - 0x01FFFE
Dual-ported RAM (DMA Buffer)	0x020000 - 0x05FFFE
VME-DMA Controller	0x060000 - 0x06FFFE
SCSI-DMA Controller	0x070000 - 0x07FFFE
NCR 53C90 SCSI Controller Registers	0x080000 - 0x08FFFE
VME Interrupt REQ	0x090000
SCSI Bus Reset Register	0x098000
Diagnostic LED Register	0x0A0000
VME Interrupt Vector Register	0x0A8000
VME-SYSFAIL* Register	0x0B0000
Board Configuration Register	0x0B8000

TABLE 2
VME-SCSI/X Diagnostic LED's

1) CPU Diagnostic LED	Lighted = TBD
2) VMEBus Master (Havebus)	Lighted = VME-SCSI/X is VMEBus Master
3) SCSI C/D	Lighted = SCSI Command phase
4) SCSI I/O	Lighted = SCSI Input phase
5) SCSI MSG	Lighted = SCSI Message Phase
6) SCSI BSY	Lighted = SCSI Bus Busy
7) SCSI Reset	Lighted = SCSI Bus Reset
8) SCSI REQ	Lighted = SCSI Bus Request

TABLE 3
68000 Interrupt Sources

Interrupt Level	**Interrupt Source**
Level 7 Autovector	(NMI) VME ACFAIL*
Level 6 Autovector	Clock Interrupt (125nS * 512 = 64uS)
Level 5 Autovector	VME Non-Existent Memory Access (VBERR or Timeout)
Level 4 Autovector	NCR 53C90 SCSI Controller
Level 3 Autovector	VME DMA Controller
Level 2 Autovector	VME Bus Clear (BCLR*)

TABLE 4
VME DMA Controller Registers

Description	68000 Address
VME Bus Address High (BAH)	0x060000
VME Bus Address Low (BAL)	0x060002
VME Bus Address Modifier (BAM)	0x060004
VME Transfer Byte Count (BC)	0x060006
VME DMA Parameter Register (DPR)	0x060007 (Byte)
VME Transfer Enable Register (TER)	0x060008 (Byte)
RAM DMA Start Address High (RDSAH)	0x06000A
RAM DMA Start Address Low (RDSAL)	0x06000C

TABLE 5
SCSI DMA Controller Registers

Description	Address
SCSI<> RAM Address High (SRAH)	0x070000
SCSI<> RAM Address Low (SRAL)	0x070002
SCSI<>RAM Transfer Count (SRTC)	0x070004
SCSI DMA Parameter Register (SDPR)	0x070005 (Byte)
SCSI DMA Transfer Enable (SDTE)	0x070006 (Byte)

2.0 Hardware - VME Slave Mode

A) The VME-SCSI/X card is supplied with two RAM arrays. The first array, 16KBytes X 32 (expandable to 32KBytes X 32) static RAM, is dedicated as a DMA data transfer buffer. This array is discussed in detail in Sections1.1 and 1.3. The second array is a dual-ported 2KByte X 16 bank of static RAM. This bank of RAM is used as a scratchpad area for the resident 68000 CPU and storage area where the Host CPU programs the board's Control Registers and Device Control Blocks. Only the upper 1Kbyte of this RAM array is mapped to the VMEbus for read/write useage by the Host CPU. The RAM array can be configured to reside in VME Standard Supervisory Data Access (VME Address Modifier = **0x3D**) or Short Supervisory Access (VME Address Modifier = **0x2D**). The VME starting address of the RAM array can be any multiple of 2K beginning at **0xFXX000** or **0xX000** depending on the VME Address Modifier used.

4K

B) The SCSI/X is capable of driving VME Interrupt Request Levels 1-7, jumper selectable. The 8 bit interrupt vector driven onto the VMEbus during the VME Interrupt Acknowledge Cycle is programmable. See the Firmware Specification section.

C) The board will support VME Bus Request Levels 0-3. The request level is jumper selectable.

D) The registers controlling SCSI/X operation are located in the 4KByte dual-ported RAM array. The SCR and DCB registers are accessed whenever the 68000 CPU addresses a RAM location in the range 0x010600 to 0x0107FF.

2.1 Hardware - VME Master Mode

A) Once the SCSI/X card captures the VMEbus, DMA data transfers to and from the bus are handled by an asynchronous state machine. Such a design will allow the board to transfer data at a rate of 30+ MBytes per second. The design of the dual-ported data buffer arbiter will be such that it will allow simultaneous data transfers between the VMEbus and buffer **and** the SCSI Protocol Controller chip and data buffer at slightly reduced VMEbus data transfer rates.

B) All VME data transfers are accompolished via a discrete 32 bit DMA controller (incorporated in PALs). The DMA controller is part of an asynchronous state machine which drives the data transfer. To maximize throughput, the first VMEbus cycle is started as a result of the 68K CPU programming the the DMA control registers. All subsequent transfers are driven by the SCSI/X board receiving VME DTACK from a slave. The SCSI/X card will relinquish control of the VMEbus once the DMA transfer count is decremented to zero. At the end of the data transfer, an autovector interrupt is sent to the resident 68K CPU signifying transfer complete.

2.2 Hardware - SCSI Interface

A) SCSI bus control is achieved using an LSI chip SCSI Protocol Controller(SPC). Data transfers to and from the SCSI bus are achieved under DMA control. The resident 68K CPU first programs the SPC chip's registers and then the discrete DMA controller, which will again be implemented in PALs. The SPC chip will interrupt the CPU upon completion of the data transfer.

2.3 Hardware - VME and SCSI DMA Controllers

A) The DMA data transfer controllers, which are crucial to the boards performance, will be incorporated using Programmable Array Logic devices. The VME DMA controller can be modeled as two counters with logic controlling VME and dual-ported Buffer RAM timing sequences. The VME Address counter/generator is a 12-bit wide counter with the higher order VME address bits held in a latch. The counter will be able to count by bytes, words, or long words depending upon how the CPU programs the DMA Parameter Register(DPR). **NOTE**: The type and width of the VME transfer is a result of the 68K CPU's interrogation of the Device Control Block as defined in the Firmware Specification section. Also, the value of the VME Address Modifier programmed into the Device Control Block will control the **type** of VME data transfer .. **standard** or **blockmode** transfer. Reference the VME DMA Register definition sheet. This architecture allows VME burst transfers of up to 4096 bytes to occur without CPU intervention, unless a VME bus error occurs in which case a level 5 autovector interrupt will be issued to the resident 68000 CPU. When the VME DMA transfer count is decremented to zero, a level 3 autovector interrupt is issued to the 68K CPU.

B) DMA transfers to the SPC chip will be controlled by a single RAM address counter/generator and a pointer to the SPC chip's data register. The counter will be 16 bits wide with the 17th bit (addressing for 128 kBytes of RAM) held in a latch. The counter being 16 bits wide will allow SCSI DMA transfers lengths of 64 KBytes to occur without CPU intervention. All data transfers to and from dual-ported Buffer RAM are executed 1 byte at a time as the SPC chip is a byte oriented device.

2.4 Hardware Memory

A) There are two memory arrays located on the SCSI/X board. The first is a 16 kByte X 32 bit array which can optionally be expanded to 32 kByte X 32. This dual-ported Buffer RAM provides intermediate storage for DMA read/write data until it can be transferred to it's end location. The second dual-ported RAM array (2KByte X 16) is for scratchpad use by the resident 68K CPU andadditionally provides the register interface by which the Host CPU controls the SCSI/X board.

3.0 Firmware Register Specification

A) The communications between the VME-SCSI/X card and the Host CPU is achieved through a set of registers located in the boards dual-ported Scratchpad RAM. The register array is comprised of 8 Device Control Blocks (DCB0-7), SCSI Control Register (SCR), Host Arbitration Register (HAR), and a Controller Arbitration Register (CAR). The Device Control Blocks occupy 16 words of memory each. The SCR, HAR, and CAR Registers consume 1 word of memory each. See attached document for an extended description of the Generic SCSI Controller register model.

VME DMA Control Registers

BAH Register

(MSB)

VME A31	VME A30	VME A29	VME A28	VME A27	VME A26	VME A25	VME A24	VME A23	VME A22	VME A21	VME A20	VME A19	VME A18	VME A17	VME A16

(LSB)

0x060000

BAL Register

VME A15	VME A14	VME A13	VME A12	VME A11	VME A10	VME A09	VME A08	VME A07	VME A06	VME A05	VME A04	VME A03	VME A02	VME A01	VME *A00

0x060002

* : A00 Isnt output to the VMEbus.

BAM Register

X	X	X	X	X	X	X	X	X	X	VME AM5	VME AM4	VME AM3	VME AM2	VME AM1	VME AM0

0x060004

BC Register

X	X	X	X	11	10	9	8	VME Transfer Byte Count	3	2	1	0

0x060006

TER Register

VME Transfer Enable/Disable

0x060008

DPR Register

X	X	X	Block Xfer	DMA R/W	DMA Size 2	DMA Size 1	DMA Size 0

0x060007

RDSAL Register

X	X	X	X	RAM A11									RAM A0

0x06000A

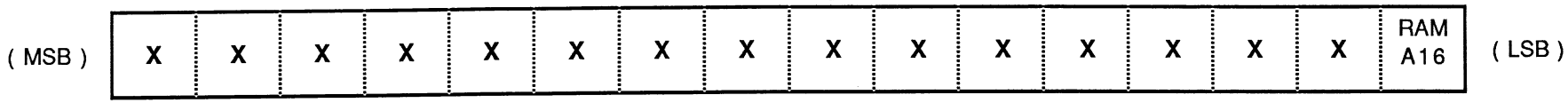
RDSAH Register

X	X	X	X	X	X	X	X	X	X	X	RAM A16	RAM A15	RAM A14	RAM A13	RAM A12

0x06000C

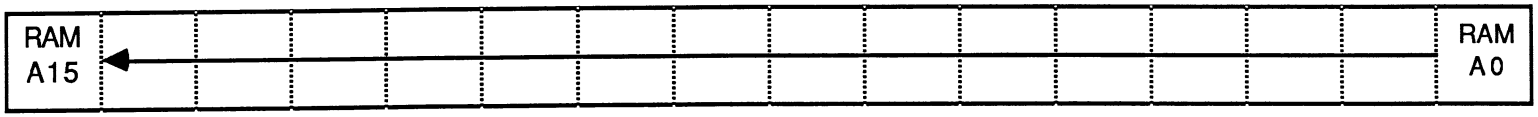
SCSI DMA Control Registers

SRAH Register



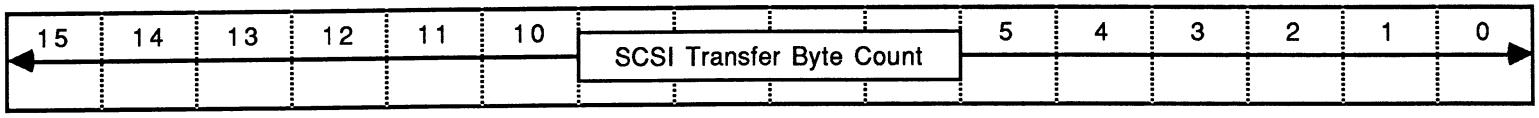
0x070000

SRAL Register



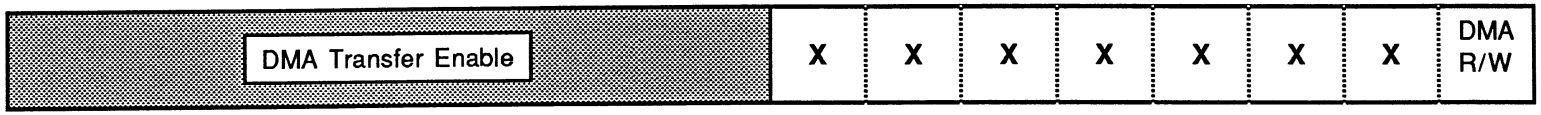
0x070002

SRTC Register



0x070004

SDPR Register



0x070006 0x070005

SCSI/X Initialization and Packet Processing

1.1 Hard Initialization Phase

The first phase of initialization is finished when the SCSI/X has completed diagnostics and turned auto reply off. Before any other commands are written to the SCSI/X, however, the host must provide it with the address of control registers and packet buffers in memory that will be used for all further communication. It does this through a hard initialization command protocol.

When the SCSI/X reads the $F1F1_H$ command and returns the one's compliment back to the host, the host immediately writes three words in succession to r0. The Address Modifier (AddMod) for the SCSI Control Register (SCR) is packed into the high byte of the first word. The next two words are the 32 bit address of the SCR. The SCSI/X computes the address of the SCSI Control Block (SCB) from the address of the SCR. If r0 is read any time after the last of the three words is received and auto reply is off, the SCSI/X returns $72xx_H$ (ident) which lets the host know that the initialization was completed successfully. The "xx" is the jumper selectable address of the SCSI/X on the SCSI bus which has a value between 1-7.

1.2 SCSI/X Control Register

The SCSI/X Control Register (SCR) is a three word memory location on the host CPU. It is one word wide, three words long and indicates when commands are pending for the SCSI/X, when the SCSI/X is busy, and whether or not the SCSI/X has completed a requested command. The MSB in the first word of SCR contains eight "GO" bits. Each of these bits corresponds to one of the eight possible devices on the SCSI/X bus. The SCSI/X controller itself is GO_x, where "x" is a value between 0-7 that represents the SCSI/X address on the SCSI bus.

The LSB in the first word of the SCR contains eight Device Busy (DB) bits that are set by the SCSI/X to indicate that it is currently busy performing some command initiated by a GO bit. After completing a job, the SCSI/X resets the GO bit, but leaves the DB set, so the host will know that its command has been completed.

If a "GO" bit is set in the SCR with no corresponding "DB" bit, the SCSI/X knows it has a job from the host. If a DB bit is set with no corresponding GO bit, the host knows that the SCSI/X has completed a job. If corresponding bits are set, the host knows that the SCSI/X is working on a particular job.

The second and third words of the SCR are the Host Arbitration Register (HAR) and the Controller Arbitration Register (CAR). They are essentially semaphors that are set either by the host or SCSI/X when one or the other wants to read, write, or modify the first word in the SCR. As long as either the host or SCSI/X has set its semaphore in its arbitration register, the other can not perform any action on the control register until the first is through. The HAR and CAR are provided only for installations without a true read, modify, write sequence. The structure of the SCR is shown in Figure 1-1.

1.3 Control Blocks

The SCSI/X Control Block (SCB) is a structure with eight consecutive Device Control Blocks (DCB). Each DCB is 16 words long with eight words having controller communication information (CCI) and eight words that create a Command Descriptor Block (CDB). The SCB is shown in Figure 1-1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GO7	GO6	GO5	GO4	GO3	GO2	GO1	GO0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Host Arbitration Register															
Controller Arbitration Register															
Device Control Block 0															
Device Control Block 1															
Device Control Block 2															
Device Control Block 3															
Device Control Block 4															
Device Control Block 5															
Device Control Block 6															
Device Control Block 7															

Figure 1-1. SCR and SCB Registers

After the SCSI/X knows the VME address of the SCR, it arbitrates for the VMEbus every 100 µs if there is a job in progress, every 1 Ms if there is not, to examine the GO bits in the control register of the SCR. If a bit is set, the SCSI/X obtains the appropriate Device Control Block from the SCB and begins to execute its instructions. The structure of the DCB is presented in Figure 1-2.

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	ERR	RSVD			CERR				STATUS							
1	INTE	DIR	SWP	NDC	Reserved				CDB Length							
2	DTW	AddMod							INT Vector							
3	Data Address MSB								Data Address 2nd MSB							
4	Data Address 3rd MSB								Data Address LSB							
5	Data Length MSB								Data Length 2nd MSB							
6	Data Length 3rd MSB								Data Length LSB							
7	Data Block Size MSB								Data Block Size LSB							
8	SCSI Command Code								LUN				Defined by Command			
9	Defined by Command types 0, 1, & 7								Defined by Command types 0, 1, & 7							
10	Defined by Command types 0, 1, & 7								Defined by Command types 0, 1, & 7							
11	Defined by Command types 1 & 7								Defined by Command types 1 & 7							
12	Defined by Command types 1 & 7								Defined by Command types 1 & 7							
13	Defined by Command type 7								Defined by Command type 7							
14	Defined by Command type 7								Defined by Command type 7							
15	Defined by Command type 7								Defined by Command type 7							

Figure 1-2. Device Control Block Structure

The CDB, which occupies the last eight words of the DCB, is identical to the CDB described by ANSI SCSI Standard 39.131-1986. A type 0 command is six bytes long, so the last five words are ignored. A type 1 command is ten bytes long, so the last three words are ignored. A type 7 command is vendor unique and may be as long as eight words.

1.4 Command Execution

Immediately after reading the three words sent during the hard initialization, the SCSI/X crosses the VMEbus and reads the SCR looking for GO bits. So the host must have already set a target's GO bit, if it wants the SCSI/X to respond to a target command immediately after a hard initialize. If a GO bit is set, the

SCSI/X sets the corresponding DB bit, fetches the DCB for the selected target, reads the appropriate fields in the DCB and the CDB and starts the command sequence. The command fields in the DCB and their interpretation are listed below:

LUN	The initiator indicates which of the 8 targets on the SCSI it has selected in the Logical Unit Number field. After the SCSI/X reads this field, it sends the target an IDENTIFY message to open a data transfer channel on the bus.
CDB Length	The Command Descriptor Block (CDB) length tells the SCSI/X how many bytes in the command itself are valid, so it sends that many bytes to the target.
Command Code	The SCSI/X only reads this field if the command is directed to it, rather than to one of the seven other targets. It does not pay attention to specific commands directed to a target. Not all commands in this field will request the transfer of data. If a request is made, however, the SCSI/X interprets the following DCB fields.
DIR	If the DIR bit is set, the data direction is from the host to the target. If the DIR is cleared, the direction is reversed.
SWP	If the swap bit is set, the SCSI/X will swap bytes in each word of data transferred to and from the SCSI target.
NDC	The no disconnect bit, if set to one (1) disables disconnects to the target which is not informed that the SCSI/X has the ability to disconnect and reconnect.
Data Address	The SCSI/X receives data from or sends data to the address specified by the 32 bit wide address pointer in the data address field.
DTW	The Data Transfer Width field is currently set to 16 bits. Future use of these two bits will encode an 8, 16, or 32 bit transfer across the VMEbus.
INTE	The interrupt enable bit is set when the host directs the SCSI/X to interrupt it after a command is completed. If this bit is not set, the SCSI/X still resets the GO bit in the SCR to zero when the command is completed, but does not generate an interrupt.
AddMod	The six bit wide address modifier field is taken from the Address Modifier field used with VMEbus addressing.
INTVector	Reserved for future use.
Data Length	If the 32 bit data length field of the DCB contains a count, and the data block size field is specified, the SCSI/X determines whether padding is required to make the transfer an even multiple of the specified block size. If so, the padding is added.
Data Block Size	The size of each data block is specified in this 16 bit field.

The SCSI/X passes commands that require no data transfers directly to the appropriate controller, and tracks commands that require transfers until they are competed by allowing the target to disconnect and reselect as often as necessary until the transfer is complete. After the last data is transferred, the SCSI/X returns status to the host. The status is returned in the zero word of the DCB, and consists of the following fields:

ERR	Bit 15 is reserved for a system error flag (ERR) to inform the host an error has occurred. This bit is set whenever CERR or the STATUS byte are non-zero.
CERR	The CERR bit is reserved for the SCSI/X controller. Error codes are summarized in Table 1.1.
STATUS	The STATUS byte returns status from the selected target, which are standard SCSI status returns. For convenience, the standard SCSI status returns are listed in Table 1.2.

Table 1-1. CERR Codes

Code	Interpretation
00_H	No error.
01_H	An error was detected in the command from the host.
02_H	The target failed to respond to a select command within approximately 250 µs.
03_H	The SPC failed to time out during select.
04_H	An anticipated interrupt arrived, but was of the wrong type, such as a disconnect interrupt from an unconnected target.
05_H	The firmware timed out waiting for a target to respond to a phase change; this error occurs while waiting for a bus service interrupt.
06_H	Phase control error: a bus service interrupt is directing the wrong sequence.
07_H	The VMEbus address was bad, either because it was not right in the DCB, or the SCSI/X miscalculated.
08_H	The target failed to return status.
09_H	A target that was connected or not active requested a reconnect.
$0A_H$	The data direction requested by the SPC does not match the direction requested by the host.
$0B_H$	The target disconnected without warning, that is, without sending a completion or status notice.
$0C_H$	A forced disconnect (Reset) was sent to the target because it did not relinquish the SCSI/X bus after a reasonable (>1 sec) interval. The target is forced off of the SCSI bus until a reset is requested by the host. All other targets forced off the bus will return $0D_H$ in response to this reset. The target that hung on the bus will return $0C_H$.
$0D_H$	This code is returned by all targets that were forced off the SCSI bus due to a forced reset, except for the hung target, as explained above.
$7FOA_H$	This code indicates any CERR or STATUS system level error.

Table 1-2. STATUS Codes

Code	Interpretation
00_H	Go7od Status
02_H	Check Condition
04_H	Condition Good
08_H	Device Busy
10_H	Intermediate: Linked/Good Status
12_H	Intermediate: Linked Condition
18_H	Reservation Conflict

1.5 SCSI/X Commands

Commands initiated by setting GO_X in the SCR (where "X" is the jumper selected SCSI bus address of the SCSI/X) are meant for the SCSI/X board itself, rather than one of the other 7 targets on the SCSI bus. These commands are defined by ISI, and other commands to the board are illegal and will be rejected.

Commands for the SCSI/X are written in the high byte of the CDB, as are all other target commands. If data needs to be sent or returned, the data address, length and block size fields are used. The command initiated by setting GO_X in the SCR is completed when the SCSI/X resets GO_X, but leaves the corresponding DB_X bit set. The STATUS byte and CERR bits are returned.

VME-SCSI/X Commands

Reset $F0_H$ — Resets the SCSI/X board and SCSI bus. No data is transferred. The data length field must be zero bytes; the DIR flag is ignored.

Init $F1_H$ — This is similar to the hard initialize command that is sent to register 0 when auto reply is off, except that this command does not wait until the SCSI/X is not busy. It does require that the SCSI/X has previously been initialized. The firmware accepts three words of data from the address presented in the data address field of the DCB and uses them for the address of a new SCR and SCB and as new DTW and AddMod fields. Other fields in the DCB that must be set include the data length, which is 6 bytes; the data block size, which is 1 byte; and the DIR flag, which is set to "send". The new SCR and SCB take effect when the GO bit is cleared in the SCR, and (optionally) the SCSI/X interrupts the host. All pending operations are aborted by the controller when it receives this command.

Status $F2_H$ — This debugging command may not be supported on all versions. The length and format of returned data is subject to change without notice, depending on the version of firmware used on any given board. The data that the SCSI/X returns status varies in length, depending on the data length requested by the host. The first word always consists of controller flags. The next eight words indicate the current status and command progression of all devices on the SCSI bus. Data length for this command is *n* bytes, depending on the host request. Data block size is one byte. The DIR flag must be set to receive.

Version $F3_H$ — Upon receiving this command, the SCSI/X returns the version of its firmware in four data words to the address specified in the data address field of the DCB. The format is six ascii characters: GPS_XX.X. Data length in the DCB must be 8 bytes; block size is 1 byte. The DIR flag is set to receive.

DumpMem $F4_H$ — This debugging command may not be supported on all versions. The length of returned data is specified when the driver loads an offset to the beginning RAM address in word 2 of the CDB (word 9 in Figure 1-2) and loads the transfer length in the Data Length fields of the DCB (words 4 and 6 in Figure 1-2). This command returns the controllers registers to the host. The format of the information is dependent on the firmware version of the controller. Data block size is 1 byte. The DIR flag is set to receive.

Diag $F5_H$ — The SCSI/X generates a number of error messages for the target when the first byte (Byte 0) in the CDB is $F5_H$. Bits 0-7 in byte 2 in the CDB correspond to the targets (0-7) on the SCSI bus. The target that is to be tested is identified by the bit pattern in byte 2. Byte 3 identifies the simulated error that the SCSI/X will generate. The bits in byte 3 are interpreted as follows:

Bit 0	Setting bit 0 generates a simulated message parity error.
Bit 1	Setting bit 1 generates a simulated status report parity error.
Bit 2	Setting bit 2 simulates an error that would normally be detected by the SCSI/X during a data transfer.

The sixth SCSI/X command is for diagnostic purposes only. Its purpose is to test the reaction of a target to an error message.