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Some New High-Speed Tunnel-Diode Logic Circuits

Abstract: Several high-speed tunnel-diode logic circuits are presented which perform majority-type logic or majority-type logic with inversion, and make use of a multiphase sinusoidal power supply to obtain signal directivity. Laboratory results are presented which show operation of these circuits at a 125 Mc/sec pulse repetition rate with 2 nsec delay per logical decision. The circuits have also been operated at 250 Mc/sec.

A comparison which is made between these circuits and some of the tunnel-diode logic circuits previously reported in the literature reveals certain system advantages of the new circuits. Preliminary results of both analog and digital computer analyses of the systems of nonlinear differential equations which describe these circuits are presented. These results have been in excellent agreement with those found in the laboratory. A full serial binary adder is described which produces a carry output in 2 nsec and the sum output in 4 nsec.

Introduction

This paper will describe some synchronous, tunnel-diode logic circuits which have been developed in the course of studying the feasibility of a high-speed computing system using tunnel diodes as the active elements.

Since the discovery of the tunnel diode by Esaki[1] in 1958, many circuit and system engineers in the digital computer field have attempted to design circuits which would capitalize on the inherent advantages of this new device for both memory and logic circuit applications. The inherent advantages of the tunnel diode are high speed, low power dissipation, device simplicity, small size, and high stability with changes in environmental conditions such as temperature and nuclear radiation.

Several tunnel-diode logic circuits have been reported in the literature—for example, the monostable,[2] bistable,[3] and, "Goto-pair"[4] circuits. The circuits which are described in this paper are similar to the "Goto-pair" circuit in that they contain a pair of matched tunnel diodes, perform majority-type logic, and make use of a multiphase ac power supply for signal directivity. However, all of the circuits which are described here have less severe tolerance requirements on the ac power supply, and one of the circuits described has larger output current and, therefore, larger fan-out than the "Goto-pair". Another circuit is described which has the following characteristics:

1) The output pulse has a flat top; this mitigates the timing tolerance problem.
2) The undesirable coupling of signals through the power supply is eliminated.
3) The power supply distribution problem is simplified and a certain flexibility in system layout is achieved.

In addition, some circuits are described which combine majority-type logic with various arrangements of signal inversion. It is felt that these circuits make the practical realization of a very-high-speed machine more nearly feasible.

A full serial binary adder is described which has been built to handle information at a bit rate of 125 Mc. The delay per logical stage is 2 nsec. The carry is produced in 2 nsec and the sum is available in 4 nsec.

Description of circuits

• *Balanced Inductor Logical Element*

The Balanced Inductor Logical Element (BILE) consists of a pair of matched tunnel diodes in series with two inductors, as shown in the circuit diagram in Fig. 1. A push-pull power supply which is composed of both a dc and a sinusoidal ac component is applied across this series combination. The logical input and output terminals of the circuit are at the midpoint of the pair of diodes. This element performs majority logic, i.e., the polarity of the output pulse is the same as the polarity of the majority of the input pulses. When a negative or positive dc voltage is applied at one of the inputs, the BILE can also perform the AND or OR function. To direct the flow of information in a system of BILE's, a multiphase power supply of the type suggested by Von Neumann[5] is used.

Fig. 2 shows the *V-I* characteristic of one diode of the pair, and several possible excursions of its operating point as an output pulse is generated. The dc power supply voltage is of such a magnitude that both diodes are placed at a stable operating point (I in Fig. 2) in the low-voltage, positive resistance region. The ac component of the power source supplies just enough voltage to carry one of the diodes into its negative resistance region, II; the other diode remains in the low-voltage, positive resistance region. The polarity of a small input signal at the midpoint of the pair of diodes determines which diode goes into the negative resistance region and hence the polarity of the output pulse. A necessary condition for operation of the BILE is that $L_s > R_s R_n C$,[6] where R_s is the total series resistance, including the resistance of the diode in the low-voltage state, L_s is the total series inductance, R_n is the negative resistance of the diode, and C is the capacitance of the diode plus stray capacitance. This condition makes region II unstable and causes the circuit to oscillate. The period of the oscillation and the path of the operating point are determined by the circuit parameters. The period of the ac component of the power supply must be such that when the operating point has traversed its path once, the ac voltage has re-established the diodes in their low-voltage, positive resistance regions. This insures the output of a single pulse per cycle of the power supply frequency.

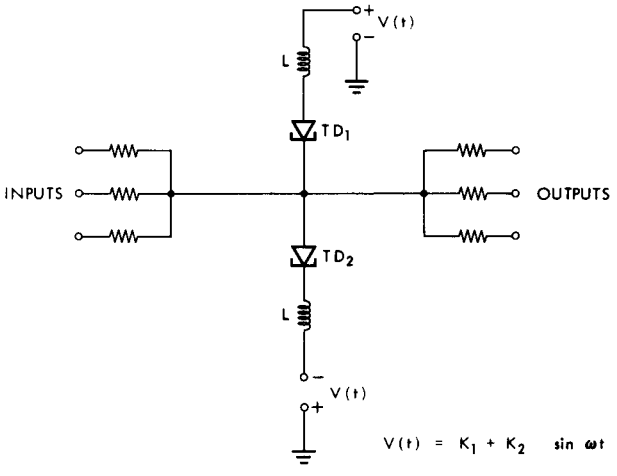


Figure 1 **Circuit diagram of Balanced Inductor Logical Element (BILE).**

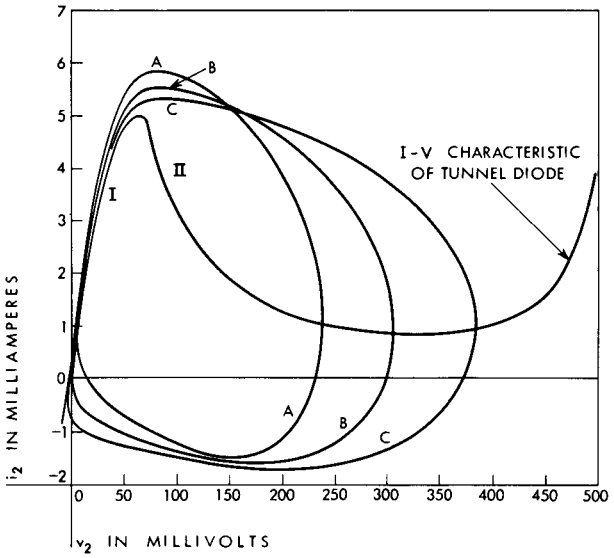


Figure 2 **Operating point paths for BILE circuit shown on the *V-I* characteristic of the tunnel diode that switches.**

Curve	$C_1=C_2$ *in pf*	$L_1=L_2$ *in nhy*	*Osc. period in nsec*
A	*5*	*5*	*1.4*
B	*5*	*10*	*2.4*
C	*5*	*20*	*3.9*

Figure 3 is the model of the BILE used in an analog computer study of the circuit. This study was carried out to gain further insight into the operation of the circuit, to obtain optimum parameters, and to determine tolerance requirements. The tunnel diode is represented by a capitance C and a current $f(v)$ through the indicated box as a nonlinear function of the voltage across the box. The nonlinear function $f(v)$ was stored in tabular form in a digital computer which was used in conjunction with the analog computer. The voltage-dependent capacitance of the diode is replaced by the constant capacitance C, which includes any stray or package capacitance. The lead inductance of the package is included in the inductor L. R_1 and R_2 are the

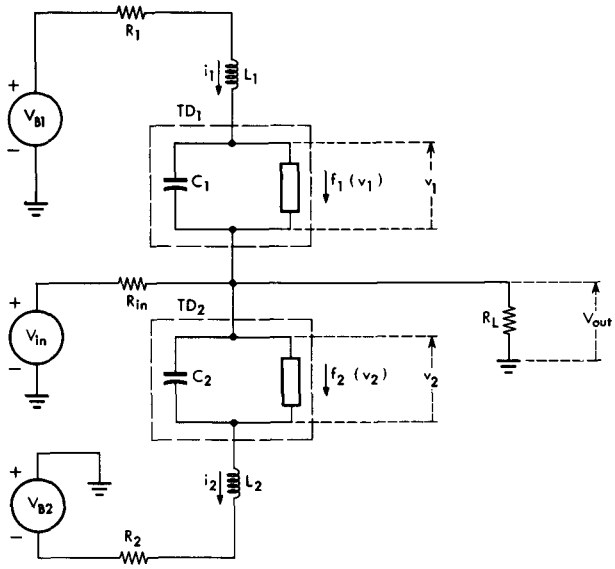


Figure 3 **Model of BILE used for analog computer analysis.**

internal resistances of the power supplies. The differential equations for this model are

$$L_1 \frac{di_1}{dt} = V_{B1} - R_1 i_1 - v_1 - \frac{R_L R_{in}}{R_L + R_{in}} (i_1 - i_2) - \frac{V_{in} R_L}{R_{in} + R_L}$$

$$L_2 \frac{di_2}{dt} = V_{B2} - R_2 i_2 - v_2 - \frac{R_L R_{in}}{R_L + R_{in}} (i_2 - i_1) + \frac{V_{in} R_L}{R_{in} + R_L}$$

$$C_1 \frac{dv_1}{dt} = i_1 - f_1(v_1)$$

$$C_2 \frac{dv_2}{dt} = i_2 - f_2(v_2)$$

$$v_{out} = \frac{V_{in} R_L}{R_{in} + R_L} + \frac{R_L R_{in}}{R_L + R_{in}} (i_1 - i_2) .$$

Some of the results of the analog study are presented here to point out a few of the salient features of the circuit operation. Experience in the laboratory dictated the choice of parameter values used in the study.

To illustrate the effects of L and C on the free-running frequency of the circuit, a dc power supply voltage and a dc logical input were applied to the BILE to carry tunnel diode 2, (TD_2), into its negative resistance region and produce a positive output pulse. Superimposed on the V-I characteristic of the 5-ma germanium tunnel diode in Fig. 2 are plots of i_2 versus v_2 for several values of L, along with a table showing the periods of the oscillations. The other circuit values for these runs were

$R_L = 50$ ohms $\qquad R_1 = R_2 = 0$

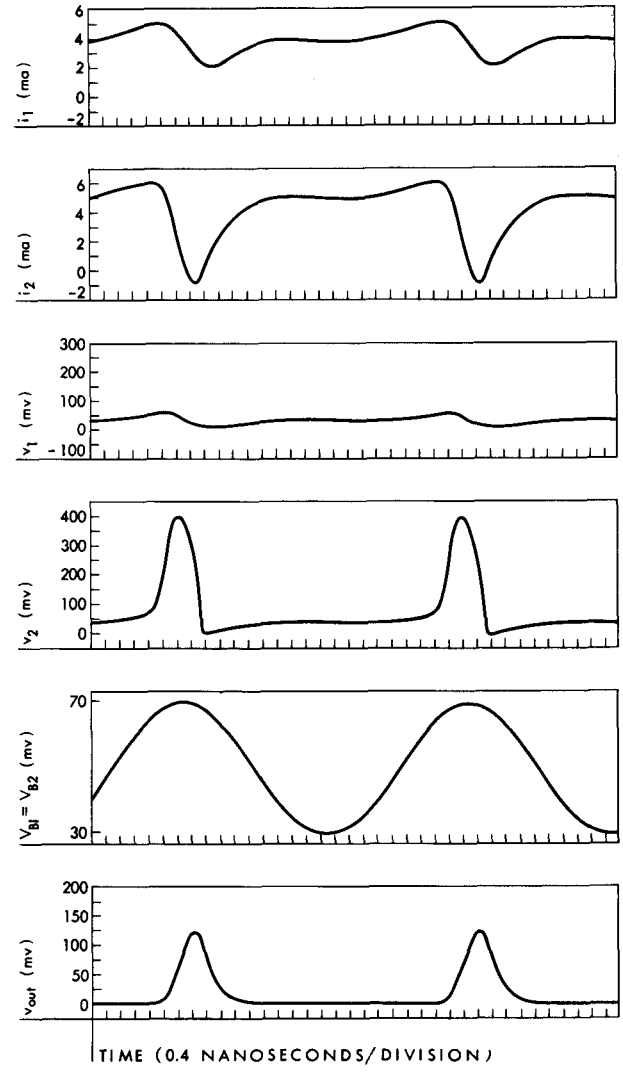
$R_{in} = 200$ ohms $\qquad V_{B1} = V_{B2} = 0.07$ v

$V_{in} = 0.1$ v .

The values of R_{in} and R_L used in these cases correspond to a fan-in plus fan-out of five with 200-ohm coupling resistors.

In the next case the diodes were dc biased in their low-voltage regions and a 125 Mc/sec sine wave was used to carry TD_2 into its negative resistance region. R_L was chosen to correspond to a fan-in plus fan-out of nine. The current supplied to the load, as an output

Figure 4 **Analog computer plots of currents and voltages for typical operation of BILE circuit at a pulse repetition rate of 125 Mc/sec.**



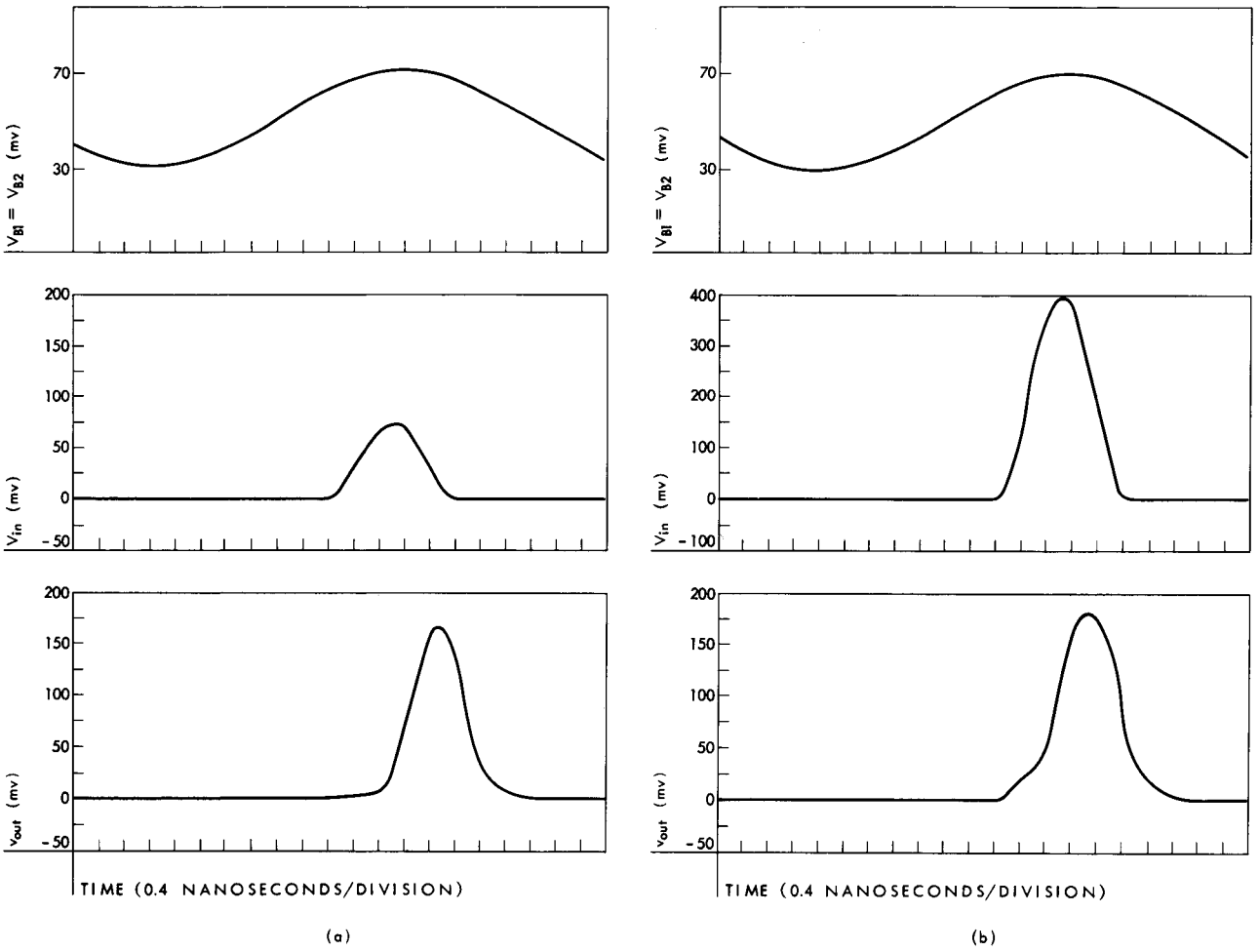


Figure 5 **Analog computer plots of BILE input, output and power supply voltages for two values of input voltage.** *(a) $V_{in\ max} = 75$ mv; (b) $V_{in\ max} = 400$ mv.*

pulse was generated, was 5.5 ma, a value greater than the peak current of the diode. The values of the parameters for this case were

$C_1 = C_2 = 5$ pf $\quad R_{in} = 200$ ohms

$L_1 = L_2 = 20$ nhy $\quad V_{in} = 0.1$ v

$R_L = 25$ ohms $\quad R_1 = R_2 = 0$

$V_{B1} = V_{B2} = 0.05 + 0.02 \sin(2\pi)(125 \times 10^6)t$ v .

Figure 4 shows the time plots of i_1, i_2, v_1, v_2, V_{B1}, and v_{out}.

In the performance of majority logic, either one unit or three units of current are presented at the inputs of the BILE, depending upon whether the majority is 2 out of 3 or 3 out of 3, respectively. The following two cases show the variations in amplitude and timing that occur in the output pulse when the amplitude of the input pulse is varied. In both cases the input pulse arrives at the same time in relation to the sine wave power supply. For a variation of the maximum input pulse amplitude from 75 mv to 400 mv, the output pulse amplitude increases 8.5% from 164 mv to 178 mv and the pulse, whose width is approximately 1.6 nsec, occurs 0.24 nsec earlier with respect to either the power supply or the input pulse. These results are shown graphically in Fig. 5. The values of the parameters here were

$C_1 = C_2 = 5$ pf $\quad R_{in} = 200$ ohms

$L_1 = L_2 = 20$ nhy $\quad R_1 = R_2 = 0$

$R_L = 50$ ohms

$V_{B1} = V_{B2} = 0.05 + 0.02 \sin(2\pi)(125 \times 10^6)t$ v .

Laboratory results have been in good agreement with results obtained in the analog computer study. Figure 6 shows typical BILE pulses obtained in the laboratory. A number generator constructed with BILE-type circuits produced an 8-bit word which was used as an

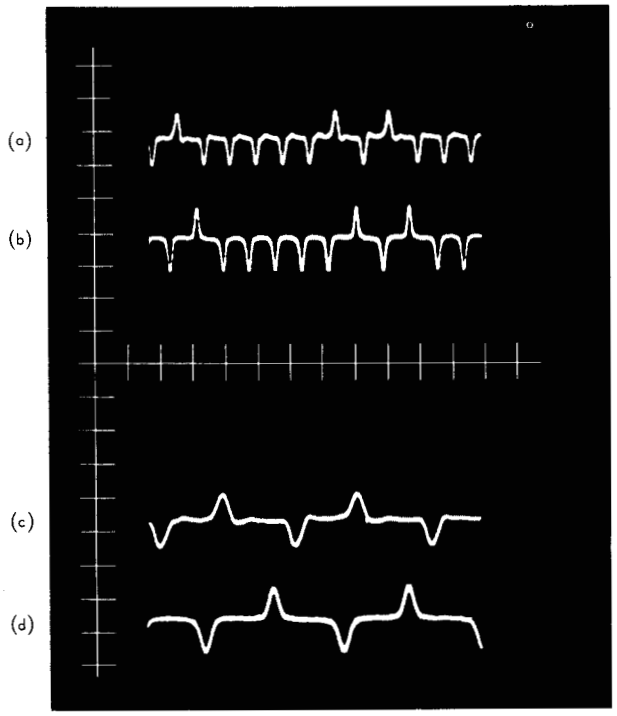


Figure 6 **Oscilloscope trace of input and output pulses of a BILE circuit operating at a 125 Mc/sec repetition rate.**
(a) Input pulses to BILE. Time scale: 10 nsec division, (b) Output pulses from BILE. Time scale: 10 nsec division, (c) Input pulses to BILE. Time scale: 4 nsec division, (d) Output pulses from BILE. Time scale: 4 nsec division.

input to a BILE under test. The BILE under test used 5-ma peak current diodes and delivered 4.5 ma to a load equivalent to a fan-in plus fan-out of nine.

A comparison of the BILE with the monostable, bistable, and "Goto-pair" circuits reveals certain advantages of the BILE. For both the single-diode monostable and the single-diode bistable circuits the logic signal shifts the load line over the peak of the diode characteristic. The gain of these circuits is, therefore, directly related to how close to the peak voltage the diode is biased. This necessitates the maintenance of strict tolerances on the diode characteristics and the bias supply. Gummel and Smits[7] conclude that for a bistable OR gate, powered from a three-phase supply, with a fan-in plus fan-out of five, worst case margins of less than $\pm 0.5\%$ are required on the power supply and on key diode and circuit parameters. For an AND gate the margins become even tighter. In the operation of the BILE the power supply shifts the load line over the peak and the logic signal is used only to determine the polarity of the output pulse by unbalancing the pair. Results of laboratory experiments indicate that with the same fan-in plus fan-out the BILE circuit can operate with less severe tolerance requirements than the single-diode circuits.

The maximum output current realizable from a "Goto-pair" circuit is equal to the difference between the peak and valley currents of the tunnel diode.[8] To approach this output current requires well-matched diodes and a tight tolerance on the ac supply voltage which swings one diode into its high-voltage stable state. As demonstrated in the analysis, the BILE is capable of delivering an output current greater than the peak current of the diode; this implies greater fan-in plus fan-out capability. The tolerance requirement on the amplitude of the ac component of the supply is greatly relaxed for the BILE due to the fact that its function is only to carry one diode somewhere into its negative resistance region. The amplitude of the ac voltage required for the BILE is small compared with the amplitude of the ac voltage necessary for the Goto-pair.

The high output current capability of the BILE makes it suitable for a synchronous-current pulse amplifier; such an amplifier could find application as a memory line driver or sense amplifier.

• *Balanced Line Logical Element*

The balanced line logical element (BLLE) consists of a pair of matched tunnel diodes in series with two delay lines, as shown in Fig. 7. A push-pull power supply, which is composed of both a dc and a sinusoidal ac component, is applied to the ends of the delay lines. Like the BILE and the Goto-pair, this element performs majority logic with the input and output terminals at the common point of the pair of diodes.

The magnitude of the dc component of the power supply must be such that the dc load line intersects the composite characteristic of the two diodes in series in its negative resistance region. When biased in this

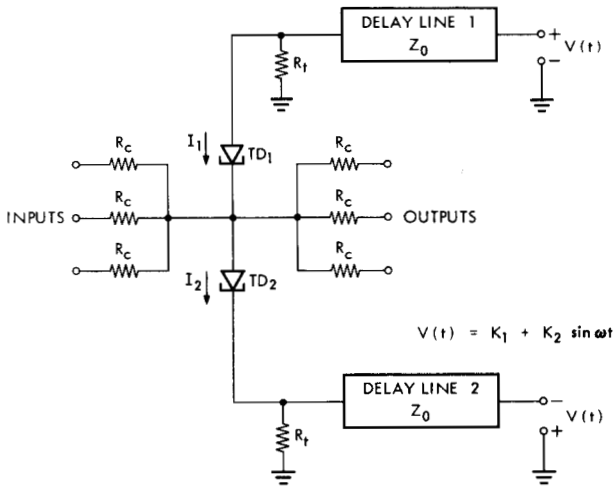


Figure 7 **Circuit diagram of Balanced Line Logical Element (BLLE).**

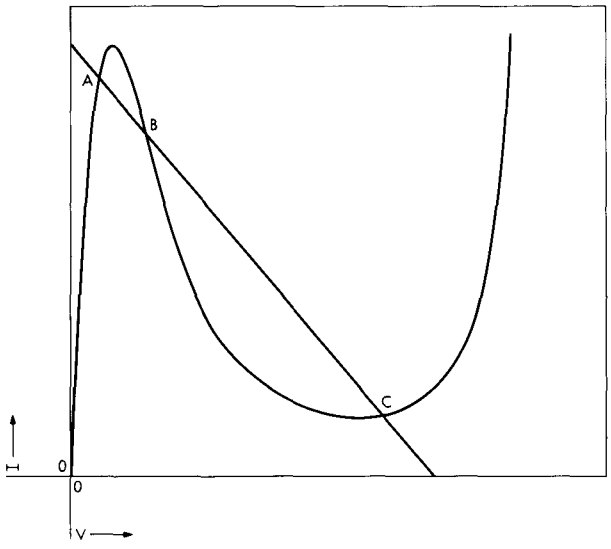


Figure 8 **Instantaneous load line drawn on *VI* characteristic of switching tunnel diode in BLLE circuit.**

manner, the circuit is unstable because the instantaneous load impedance across each diode is greater than its negative resistance. The instantaneous load impedance is equal to the impedance seen looking out of the diode terminals, with the delay lines replaced by their characteristic impedance. This impedance yields a load line which intersects the diode characteristic at *A*, *B*, and *C*, in Fig. 8. Intersections in the regions of *A* and *C* are quasi-stable. Intersections in the region of *B* are unstable.

In the absence of the sinusoidal component of the power supply, the BLLE will free run. The cycle of operation may best be explained by assuming that tunnel diode 2, (TD_2), switches from region *A* to region *C* while TD_1 remains in region *A*. The changes in the currents through the diodes cause a positive voltage step to be impressed on line 1 and a negative voltage step on line 2. The magnitude of the step on line 2 is greater than that on line 1 by an amount equal to

$$\frac{|I_1 - I_2|R_t Z_0}{R_t + Z_0},$$

where I_1 and I_2 are the currents in TD_1 and TD_2, respectively, and $I_1 - I_2$ is the output current. The voltage steps propagate to the power supply ends of the delay lines, where they are inverted and reflected by the very low power supply impedance. When these reflected steps return to the diode ends of the delay lines, they force TD_2 to return to region *A*. Further transients on the delay lines, initiated by the diode's transition to region *A*, cause the voltage across the diodes to increase toward the dc power supply voltage. The arrival of the diodes in their negative resistance region initiates another cycle.

A similar explanation can be given for the case where TD_1 switches into region *C*, resulting in a negative output pulse. The decision as to which diode switches into region *C* is determined by the polarity of the logical input at the time of switching. The logical input signal need only be of sufficient amplitude to overcome any unbalance in the circuit. This unbalance can be caused by mismatched diodes or resistors, an unbalanced power supply, and transients present on the lines from preceding cycles.

The sinusoidal component of the power supply is introduced in order to synchronize each BLLE circuit to the machine clock. The amplitude of this push-pull signal can be small with a loose tolerance. As with the BILE circuit, a multiphase sinusoidal power supply would be utilized in order to direct the flow of information.

The output pulses from the BLLE are characterized by a relatively flat top, whose width is determined by the length of the delay lines and whose rise and fall times are determined by the composite circuit *RC* time constant.

A digital computer analysis of the BLLE, using an IBM 7090, has been initiated. Such a study will allow us to observe circuit operation under conditions which cannot be easily reproduced in the laboratory and will

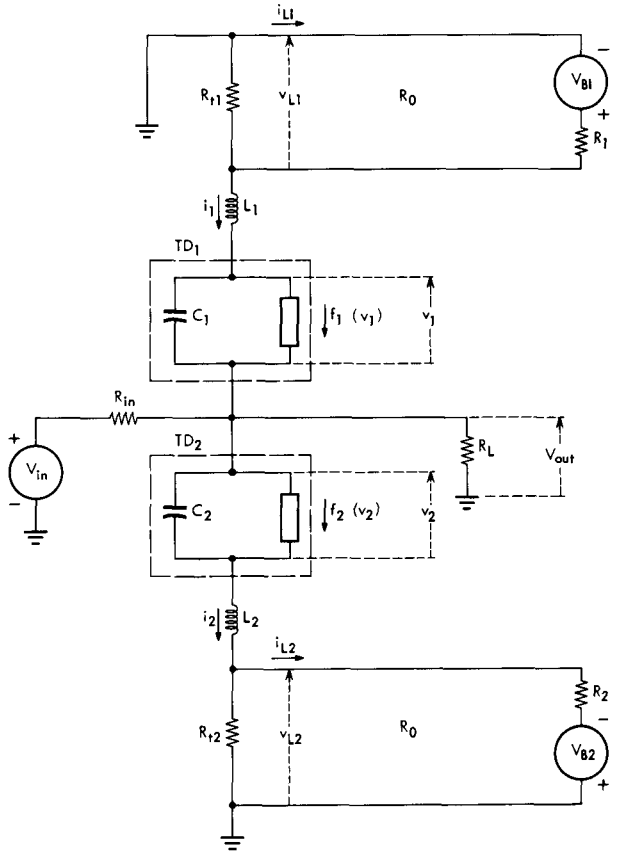


Figure 9 **Model of BLLE used in digital computer analysis.**

also allow us to determine the tolerance requirements on the circuit parameters for reliable operation. The model of the BLLE used in this study is shown in Fig. 9. The differential equations for this model are:

$$L_1 \frac{di_1(t)}{dt} = -v_1(t) - R[i_1(t) - i_2(t)] - R_{t1}[i_1(t) - i_{L1}(t)] - V(t)$$

$$L_2 \frac{di_2(t)}{dt} = -v_2(t) - R[i_2(t) - i_1(t)] - R_{t2}[i_2(t) - i_{L2}(t)] + V(t)$$

$$i_{L1}(t) = \frac{v_{L1}(t)}{R_0} + \frac{2}{R_0}\sum_{n=1}^{\infty} \rho_1{}^n v_{L1}(t - 2n\tau) + \frac{2}{R_0 + R_1}\sum_{n=0}^{\infty} \rho_1{}^n V_{B1}[t - (2n+1)\tau]^*$$

$$i_{L2}(t) = \frac{v_{L2}(t)}{R_0} + \frac{2}{R_0}\sum_{n=1}^{\infty} \rho_2{}^n v_{L2}(t - 2n\tau) + \frac{2}{R_0 + R_2}\sum_{n=0}^{\infty} \rho_2{}^n V_{B2}[t - (2n+1)\tau]$$

$$v_{L1}(t) = R_{t1}[i_1(t) - i_{L1}(t)]$$

$$v_{L2}(t) = R_{t2}[i_2(t) - i_{L2}(t)]$$

$$C_1 \frac{dv_1(t)}{dt} = i_1(t) - f_1(v_1)$$

$$C_2 \frac{dv_2(t)}{dt} = i_2(t) - f_2(v_2)$$

$$v_{out}(t) = V(t) + R[i_1(t) - i_2(t)],$$

where

$$R = \frac{R_L R_{in}}{R_L + R_{in}}, \qquad \rho_1 = \frac{R_0 - R_1}{R_0 + R_1},$$

$$\rho_2 = \frac{R_0 - R_2}{R_0 + R_2}, \qquad V(t) = \frac{R_L}{R_L + R_{in}} V_{in}(t)$$

and τ = time for signal to propagate down length of delay line.

The following results of the digital computer analysis are presented to illustrate the basic operation of the BLLE circuit, to show the shapes of typical BLLE output pulses and to demonstrate the effect of stray inductance on the output pulses.

With only the dc component of the power supply applied to the ends of the delay lines, the BLLE free runs. The time plots of the currents and voltages i_1, i_2, v_1, v_2, v_{L1}, v_{L2}, and v_{out} shown in Fig. 10 for such a free-running case, serve to illustrate the basic operation of the BLLE as previously described. The circuit parameters for this case were:

$R_0 = 50$ ohms	$R_{t1} = R_{t2} = 50$ ohms
$R_{in} = 200$ ohms	$R_1 = R_2 = 1$ ohm
$R_L = 50$ ohms	$L_1 = L_2 = 0.6$ nhy
$\tau = 2$ nsec	$C_1 = C_2 = 5$ pf
$V_{in} = 0.075$ v	$V_{B1} = V_{B2} = 0.075$ v.

The *VI* characteristic of the 5-ma peak current germanium tunnel diode used in this analysis is similar to the *VI* characteristic shown in Fig. 4. With lengths of delay line such that $\tau = 2$ nsec, the output pulse was about 4 nsec wide and the free-running period was 18 nsec. The values of R_{in} and R_L used in this case correspond to a fan-in plus fan-out of five with 200-ohm coupling resistors.

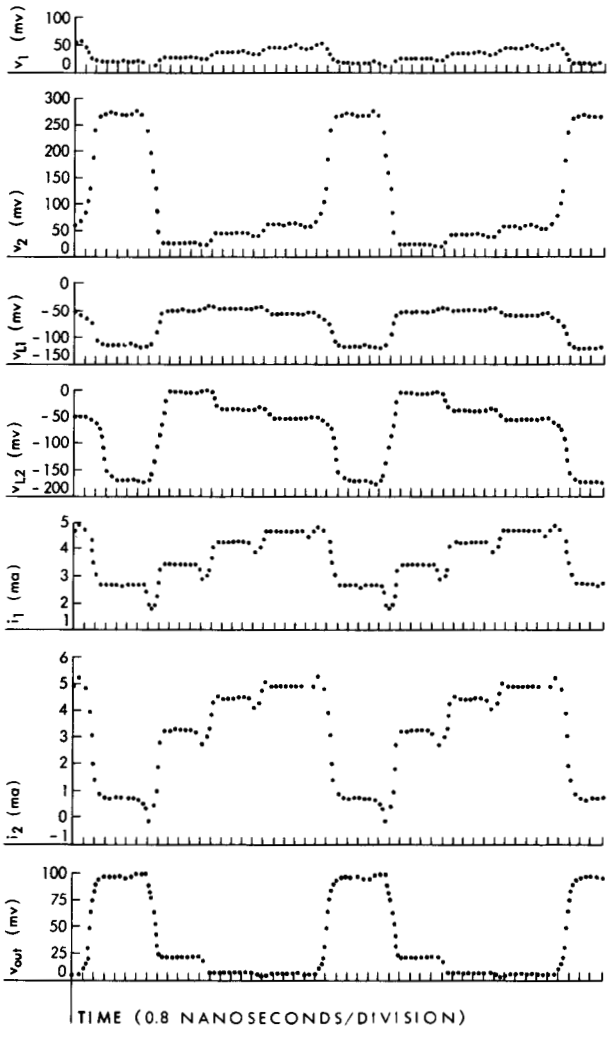


Figure 10 **Digital computer plots of currents and voltages of free-running BLLE.**

* See Appendix for derivation of delay-line equation.

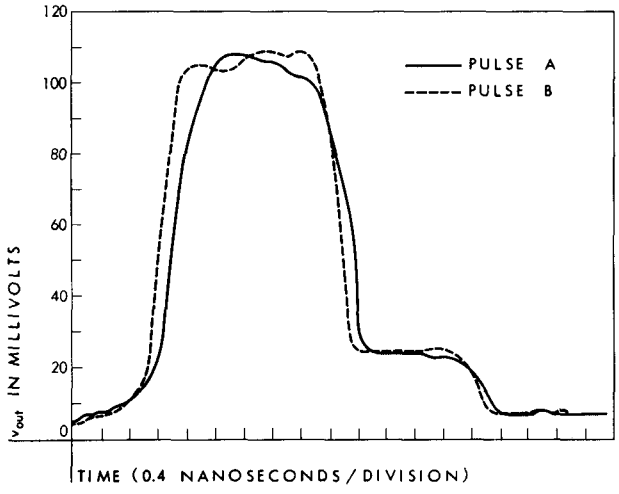


Figure 11 **Digital computer plots of output pulses from BLLE circuits operating at a 125 Mc/sec repetition rate.**
Pulse A: $L_1 = L_2 = 2$ nhy. Pulse B: $L_1 = L_2 = 6$ nhy.

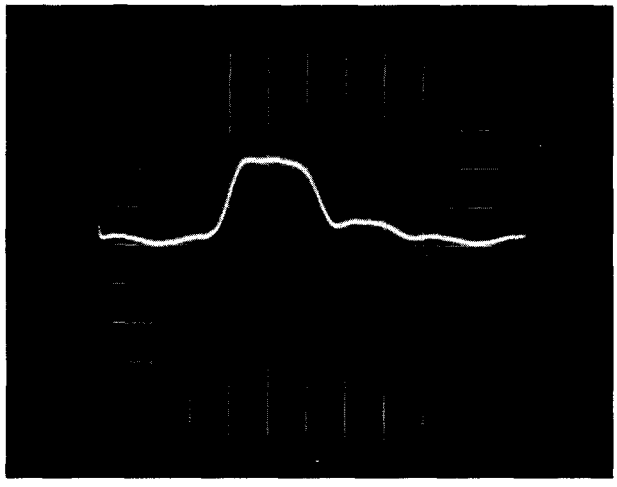


Figure 12 **Oscilloscope trace of a typical output pulse from a BLLE circuit operating at a pulse repetition rate of 125 Mc/sec.**
Time scale: 1 nsec/large division.

In the next case an ac component was included in the power supply to synchronize the BLLE to the clock frequency. The circuit parameters were the same as in the first case except that $V_{B1} = V_{B2} = 0.075 + 0.025 \sin(2\pi/16) \times 10^9 t$ v. This resulted in a pulse repetition rate of 62.5 Mc/sec.

With the delay lines shortened so that $\tau = 1$ nsec, the BLLE using 5 ma, 5 pf, tunnel diodes can be operated at a pulse repetition rate of 125 Mc/sec. Figure 11 shows the digital computer plot of two output pulses from BLLE's operated at 125 Mc/sec. Pulse A was from a BLLE with inductance $L_1 = L_2 = 2$ nhy and pulse B was from a BLLE with inductance $L_1 = L_2 = 6$ nhy. The effect of the larger inductance was a decrease in rise time, an overshoot at the leading edge of the pulse and some ringing on top of the pulse. The other circuit parameters were:

$R_0 = 50$ ohms $\quad R_{t1} = R_{t2} = 50$ ohms

$R_{in} = 200$ ohms $\quad R_1 = R_2 = 1$ ohm

$R_L = 50$ ohms $\quad C_1 = C_2 = 5$ pf

$\tau = 1$ nsec $\quad V_{in} = 0.1$ v

$$V_{B1} = V_{B2} = 0.075 + 0.025 \sin\left(\frac{2\pi}{8}\right) \times 10^9 t \text{ v}.$$

In order to obtain proper operation of any logic circuit, it is necessary that the input pulses coincide in time. The problem of achieving coincidence is somewhat mitigated by two properties of the BLLE circuit. The BLLE is sensitive only to input signals for a short time interval just before it switches. The input pulses, therefore, need only be coincident during that interval. The output pulse from the BLLE has a relatively flat top; for example, pulse B of Fig. 11 is within 5 mv of 105 mv for 2 nsec.

For majority logic of the type discussed in this paper, an odd number of input pulses to a stage of logic are linearly summed to produce a net input pulse, either positive or negative, which determines the polarity of the output pulse of that stage. This linear addition implies that for a variation of $\pm X\%$ on the pulse amplitude ($\pm V$) of each of n input lines, the absolute value of the sum can be as small as $(V - nXV)$. The value X is mainly determined by the difference between the output pulse amplitudes when the input is a majority of 2 out of 3 (i.e., one unit of input current) and when the input is a majority of 3 out of 3 (i.e., 3 units of input current). The digital computer tolerance analysis, when completed, will determine the value of X and whether there exist practical tolerance specifications on the circuit and power supply parameters so that $(V - nXV)$ is greater than the minimum signal required for reliable switching.

The computer results have been in excellent agreement with results obtained in the laboratory. Figure 12 is a photograph of an oscilloscope trace showing a typical output pulse from a BLLE circuit operating at a 125 Mc/sec bit rate. The circuit parameters for this BLLE were essentially the same as for the BLLE that was analyzed on the computer and produced pulse B in Fig. 11. The power supply impedance for the BLLE in the laboratory was capacitive instead of resistive and the magnitude of the stray inductance was not accurately determined.

Experiments in the laboratory to date have proven the BLLE to have decided advantages as a basic circuit for computer systems over the BILE and the Goto-pair circuits.

The amplitude of the ac power supply voltage required for operation of the BLLE and the BILE is much smaller than that required for the Goto-pair and the tolerance requirement on this amplitude is greatly relaxed. Both the BLLE and the BILE have been operated satisfactorily with large variations in the amplitude of the push-pull ac power supply.

The flat top output pulse waveform of the BLLE is far superior to the peaked waveform of the BILE when consideration is given to the timing tolerance on three signals arriving at a junction to form majority logic. The calculated output pulse waveform of the Goto-pair is comparable to that of the BLLE but does not have as flat a top.[9]

When either two BILE's or two Goto-pair circuits are operated in parallel from a common power supply, the one switching first causes a voltage drop across the internal impedance of the supply, tending to cause the second circuit to switch in the same direction. The gain for the second circuit is thereby a function of whether it is switching in the ONE or the ZERO direction. This problem, of course, gets worse as more circuits are powered from common power supply terminals. For example, if ten circuits were connected to a common power supply terminal, the first one to switch would tend to make the other nine go the same way, and if the first two went in the same direction, they would influence the remaining eight even more. This means that if the first nine all went in the ONE direction, they would tend very strongly to make the tenth circuit go in the ONE direction. It should be kept in mind that ideally all ten of these circuits should switch at the same time. The difference in time between the first ONE that switches and subsequent ONE's will be due only to slight differences in their characteristics and will generally be a small fraction of a nanosecond when a 125 Mc/sec power supply frequency is used. This rather serious system problem of the BILE and Goto-pair circuits can be mitigated by heavily decoupling each circuit. This entire problem does not exist with the BLLE circuit, because the power supply is not affected by a switching BLLE until a time after the switch equal to the propagation time down one of the delay lines. This time is much greater than the possible difference in time between the switching of any two circuits on the same power supply terminals.

The delay lines, which are part of the BLLE circuit, offer a flexibility in system layout that is not possible with either the BILE or the Goto-pair. A BLLE circuit can be distributed in space up to a distance equal to the length of its delay lines away from its low-impedance power source. It would be extremely difficult physically to connect several BILE'S or Goto-pairs to the terminals of a single low-impedance power source. Of course, this would probably never be done because of the need for decoupling to overcome the interaction of circuits operating in parallel.

In systems composed only of BLLE's it is necessary to use complementary logic in order to obtain signal inversion; that is, for each logic function formed, its complement is also formed and carried along through the system to be used wherever required. By using complementary logic, the total load on the push-pull power supply remains balanced to ground and independent of the particular information being processed. This balanced loading eliminates unwanted transients due to different voltage drops across each side of the push-pull power supply impedance.

• *Inverter circuits*

Two tunnel-diode inverter circuits and the logical functions they perform are shown in Fig. 13. The circuit configurations are similar, but their logical functions and design criteria are different. If three inputs, A, B, and C are presented to the circuit in Fig. 13a, the output at the center of the pair of diodes is $[ABC]$

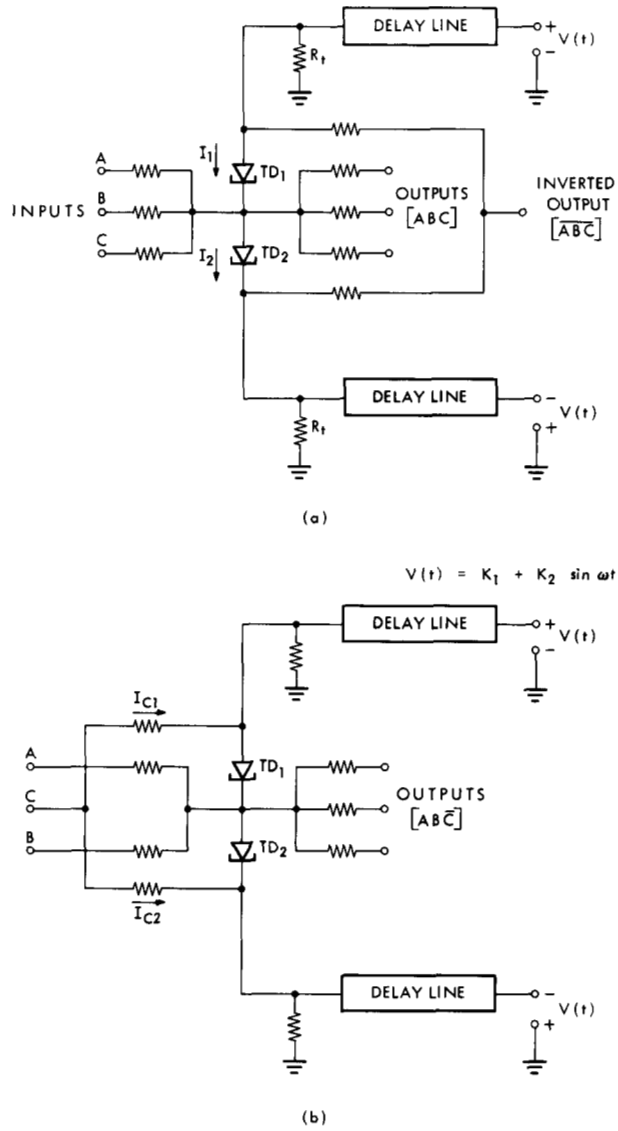


Figure 13 **Circuit diagram of inverter circuits.**

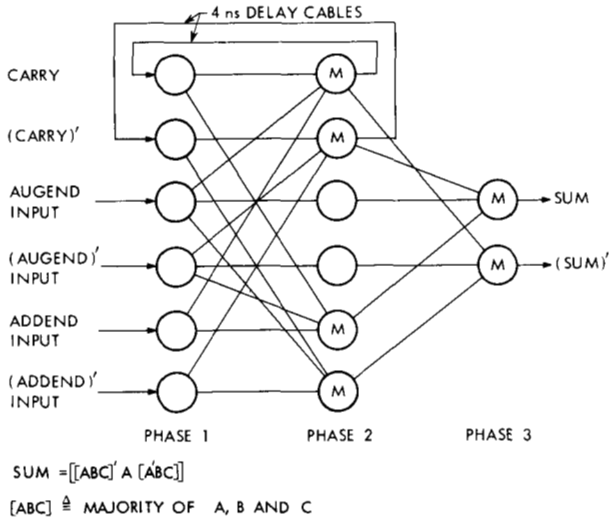


Figure 14 **Logical block diagram of full serial binary adder.**
Each circle represents a BLLE circuit.

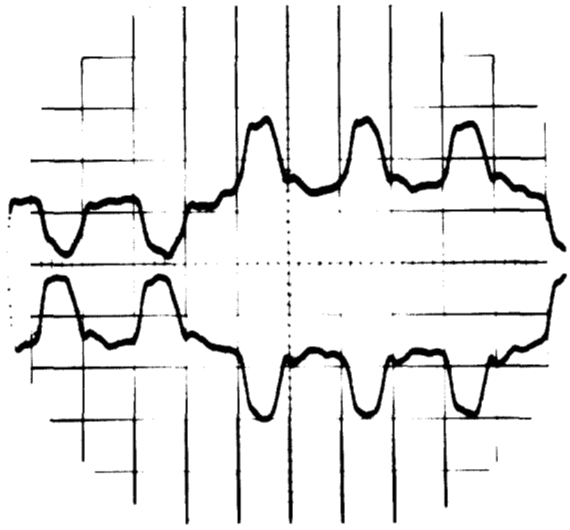


Figure 15 **Oscilloscope trace of sum and sum complement output waveforms of full serial adder.**
Time scale: 4 nsec/large division

(i.e., the majority of A, B, and C) and the inverted output is $[\overline{ABC}]$ (i.e., the complement of the majority of A, B and C or the minority of A, B, and C). The output of the circuit shown in Fig. 13b is $[AB\overline{C}]$ for inputs A and B applied at the center of the pair of diodes and input C applied at the junction of the two resistors as shown. With proper choice of delay line impedance, terminating resistors and coupling resistors, both circuits can perform the logic functions indicated without excessively loading the succeeding or preceding stage.

The operation of the circuits is similar to that of the BLLE described earlier. If the polarity of the majority of the input pulses to the circuit shown in Fig. 13a is positive, the output at the center of the pair of diodes is positive. The output current, I_{out}, is equal to $I_1 - I_2$, the difference of the currents that flow through TD_1 and TD_2. The directions of these currents are such as to establish a positive voltage with respect to ground across the resistor R_{t1} and a larger negative voltage with respect to ground across the resistor R_{t2}. The sum of these two voltages is negative and its magnitude is approximately equal to

$$|I_1 - I_2| \frac{R_T Z_0}{R_T + Z_0} .$$

This negative voltage supplies a negative pulse of current at the inverted output. The delay line impedance Z_0, the resistors R_t, and the coupling resistors R_c should be selected in such a manner that the magnitude of the inverted output is equal to the magnitude of the normal output. This is necessary if succeeding stages are to perform majority logic using both normal and inverted outputs from preceding stages. A similar explanation can be given for the case when the polarity of the majority of input pulses is negative.

The circuit shown in Fig. 13b operates as follows: If inputs A and B are not present, a positive input at C causes the currents I_{c1} and I_{c2} to flow. These currents unbalance the circuit and cause TD_1 to switch to its high state, resulting in a negative output. A negative input at C causes TD_2 to switch, resulting in a positive output. In order for the majority function to be formed, the unbalance in the circuit caused by an input at C must equal the unbalance in the circuit caused by an equal input at A or B. The delay line impedance Z_0, the resistors R_t, and the coupling resistors R_c can be chosen so that this occurs.

- *Full serial adder*

A full serial adder using BLLE circuits has been built and is operating satisfactorily at a bit rate of 125 Mc/sec. The adder uses complementary logic so that the sum, the carry, and their complements are available. Figure 14 shows the logical block diagram for this adder; each circle on the diagram represents a BLLE circuit of the type shown in Fig. 7 which performs majority logic. In this system three phases of a four-phase 125 Mc/sec power supply are used, resulting in a delay through the adder of 6 nsec. The first stage is being used for amplification and reshaping of the addend and augend word pulses so that essentially the generation of the carry requires 2 nsec and the generation of the sum 4 nsec. The loading on each BLLE is the same and corresponds to a fan-in plus fan-out of five. In cases where only one input and one output are required, a resistor is connected from the center point of the two diodes to ground to make up the additional loading.

A simple ac power distribution scheme is employed in the adder. Different lengths of 50-ohm coaxial cable are used to achieve the push-pull action and the three

phases of the 125 Mc/sec supply. The ac voltages at the ends of the delay lines of the BLLE are established across 0.001 μfd capacitors which have a reactance of about one ohm at 125 Mc/sec. Six BLLE circuits are connected across each pair of 0.001 μfd capacitors. The tunnel diodes are 5-ma peak current germanium units mounted in TO-18 headers with capacities of approximately 5 pf. The delay lines of the BLLE's are 50-ohm miniature coaxial cables with a length of 7.5", having approximately 1 nsec time delay. Five per cent, 1/4 watt carbon composition resistors were used throughout the adder.

Figure 15 is a photograph of an oscilloscope trace showing the sum and sum complement lines when binary 15 is added to binary 13. Time reads from left to right and the lowest order bit is on the left. The time scale is 4 nsec per large division (i.e., each pulse is just under 4 nsec wide).

Variations from the characteristic flat-top output pulse of the BLLE are due to inductance in series with the diodes, crosstalk between the resistors that couple one BLLE to another and other factors that are a function of the construction techniques used. The TO-18 headers introduce an inductance of approximately 6 nh in series with the diode. As shown in the computer results, this inductance improves the rise time and causes an overshoot at the leading edge of the pulse from the BLLE. At 125 Mc/sec the techniques used in the construction of this adder have been extended to near their maximum frequency limitation. In order to operate at higher frequencies or build larger systems at this frequency, consideration will be given to more sophisticated high-frequency components and construction techniques such as strip line, deposited resistors, multilayered structures, and better packaged diodes. Physically small strip transmission lines are most easily constructed with characteristic impedances in the 25 to 100 ohm range. Therefore, the input and output resistors of BLLE circuits can be used to match both ends of the strip lines used for signal transmission between logic circuits. For example, the 200-ohm coupling resistors used in the adder can each be replaced by a 100-ohm resistor at each end of a 100-ohm characteristic impedance strip line.

This adder was built to demonstrate the use of BLLE circuits in a small subsystem. A more efficient means of distributing the ac power will be used in future systems.

Conclusions

Several new tunnel-diode logic circuits have been presented in this paper, one of which, the BLLE, appears to be suitable as a basic circuit for computer systems. The BLLE circuit performs logic, amplification, reshaping and retiming. Assuming that the tolerance requirements for the circuit are found to be reasonable, an entire synchronous logical system, including shift and storage registers, could be built using only BLLE circuits.

There are two factors which determine the speed of logic circuits. One is the delay per logical decision and the other is the repetition rate at which the circuits can be operated. Logical designers of systems which make use of transistors and/or semiconductor diodes have minimized the delay per logical decision by making use of long chains of asynchronous circuits. These long chains of asynchronous circuits have an inherently low signal repetition rate. For some applications this low repetition rate is not an important factor because the maximum repetition rate of the system is limited not by the circuit's capability, but rather by either the rate at which information is available from memory or by the rate at which associated control signals can be made available. However, there are many cases where the maximum repetition rate is extremely important in determining the over-all machine speed. For example, higher speed adders and multipliers can be built with the high-repetition-rate synchronous circuits described in this report than can be built with asynchronous logic circuits having the same delay per logical decision and the same fan-in and fan-out.

To a great extent the practicability of a tunnel-diode machine will depend upon whether tunnel diodes can be made reproducibly, cheaply, with high reliability, and with good high-frequency characteristics. Recent improvements in tunnel-diode fabrication have made 5-ma peak current diodes available which can be used in a system of BLLE circuits at a 250-Mc/sec repetition rate with 1 nsec delay per logical operation.

Packaging is a problem common to all high-frequency computing machines. The state of this technology at present is a limiting factor on how fast a tunnel-diode system can be built. The ultimate machine speed achievable will depend not only on the devices, but also on the system layout and packaging. These problems will be eased by the low-power dissipation of tunnel-diode circuits (i.e., approximately 1 milliwatt for a BLLE with 5-ma peak current tunnel diodes) which permits a higher packing density than is possible with high-speed transistor circuits.

Appendix: Derivation of the delay line equation used in the analysis of the BLLE circuit

The general solution of the Laplace transformed differential equations for a transmission line with zero initial conditions is[10]

$$I(x, s) = A\varepsilon^{-\gamma x} + B\varepsilon^{\gamma x} \tag{1}$$

$$V(x, s) = AZ_0\varepsilon^{-\gamma x} - BZ_0\varepsilon^{\gamma x}, \tag{2}$$

where

$$\gamma = [(Ls + R)(Cs + G)]^{1/2} \quad \text{and} \quad Z_0 = \left[\frac{Ls + R}{Cs + G}\right]^{1/2}$$

R, L, C, and G are the standard delay line parameters. At $x = l$

$$V(l, s) = Z_R I(l, s) - V_B(s), \tag{3}$$

and from Eqs. (1) and (2)

$$I(l, s) = A\varepsilon^{-\gamma l} + B\varepsilon^{\gamma l} \tag{4}$$

$$V(l, s) = AZ_0\varepsilon^{-\gamma l} - BZ_0\varepsilon^{\gamma l}. \tag{5}$$

Substituting Eq. (4) into Eq. (3) and equating (3) and (5) yields

$$A(Z_0 - Z_R)\varepsilon^{-\gamma l} - B(Z_0 + Z_R)\varepsilon^{\gamma l} = -V_B(s). \tag{6}$$

At $x = 0$, from Eqs. (1) and (2)

$$I(0, s) = A + B \tag{7}$$

$$V(0, s) = AZ_0 - BZ_0. \tag{8}$$

Solving (6) and (8) simultaneously for A and B yields

$$A = \frac{-V_B(s) - \dfrac{V(0, s)}{Z_0}(Z_0 + Z_R)\varepsilon^{\gamma l}}{(Z_0 - Z_R)\varepsilon^{-\gamma l} - (Z_0 + Z_R)\varepsilon^{\gamma l}} \tag{9}$$

and

$$B = \frac{-V_B(s) - \dfrac{V(0, s)}{Z_0}(Z_0 - Z_R)\varepsilon^{-\gamma l}}{(Z_0 - Z_R)\varepsilon^{-\gamma l} - (Z_0 + Z_R)\varepsilon^{\gamma l}}. \tag{10}$$

Substituting (9) and (10) into (7) and rearranging terms results in

$$I(0, s) = \frac{2V_B(s)}{Z_0 + Z_R}\varepsilon^{-\gamma l}\frac{1}{1 - \rho\varepsilon^{-2\gamma l}} + \frac{V(0, s)}{Z_0}\left[\frac{1 + \rho\varepsilon^{-2\gamma l}}{1 - \rho\varepsilon^{-2\gamma l}}\right], \tag{11}$$

where $\rho = \dfrac{Z_0 - Z_R}{Z_0 + Z_R}$.

Rewriting (11) as an infinite series,

$$I(0, s) = \frac{V(0, s)}{Z_0} + \frac{2V(0, s)}{Z_0}\sum_{n=1}^{\infty}\rho^n\varepsilon^{-2n\gamma l} + \frac{2V_B(s)}{Z_0 + Z_R}\sum_{n=0}^{\infty}\rho^n\varepsilon^{-(2n+1)\gamma l}. \tag{12}$$

For a lossless line, i.e., $R = G = 0$ and with $Z_R = R_R$

$$Z_0 = \left(\frac{L}{C}\right)^{1/2} = R_0$$

$$\gamma = s(LC)^{1/2}$$

$$\gamma l = \tau s,$$

and Eq. (12) becomes

$$I(0, s) = \frac{V(0, s)}{R_0} + \frac{2V(0, s)}{R_0}\sum_{n=1}^{\infty}\rho^n\varepsilon^{-2n\tau s} + \frac{2V_B(s)}{R_0 + R_R}\sum_{n=0}^{\infty}\rho^n\varepsilon^{-(2n+1)\tau s} \tag{13}$$

Taking the inverse Laplace transform yields

$$i(0, t) = \frac{v(0, t)}{R_0} + \frac{2}{R_0}\sum_{n=1}^{\infty}\rho^n v(0, t - 2n\tau) + \frac{2}{R_0 + R_R}\sum_{n=0}^{\infty}\rho^n V_B[t - (2n + 1)\tau], \tag{14}$$

where $\rho = \dfrac{R_0 - R_R}{R_0 + R_R}$.

$i(0, t)$ and $v(0, t)$ correspond to $i_L(t)$ and $v_L(t)$ in the equations describing the BLLE circuit in the body of the paper.

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