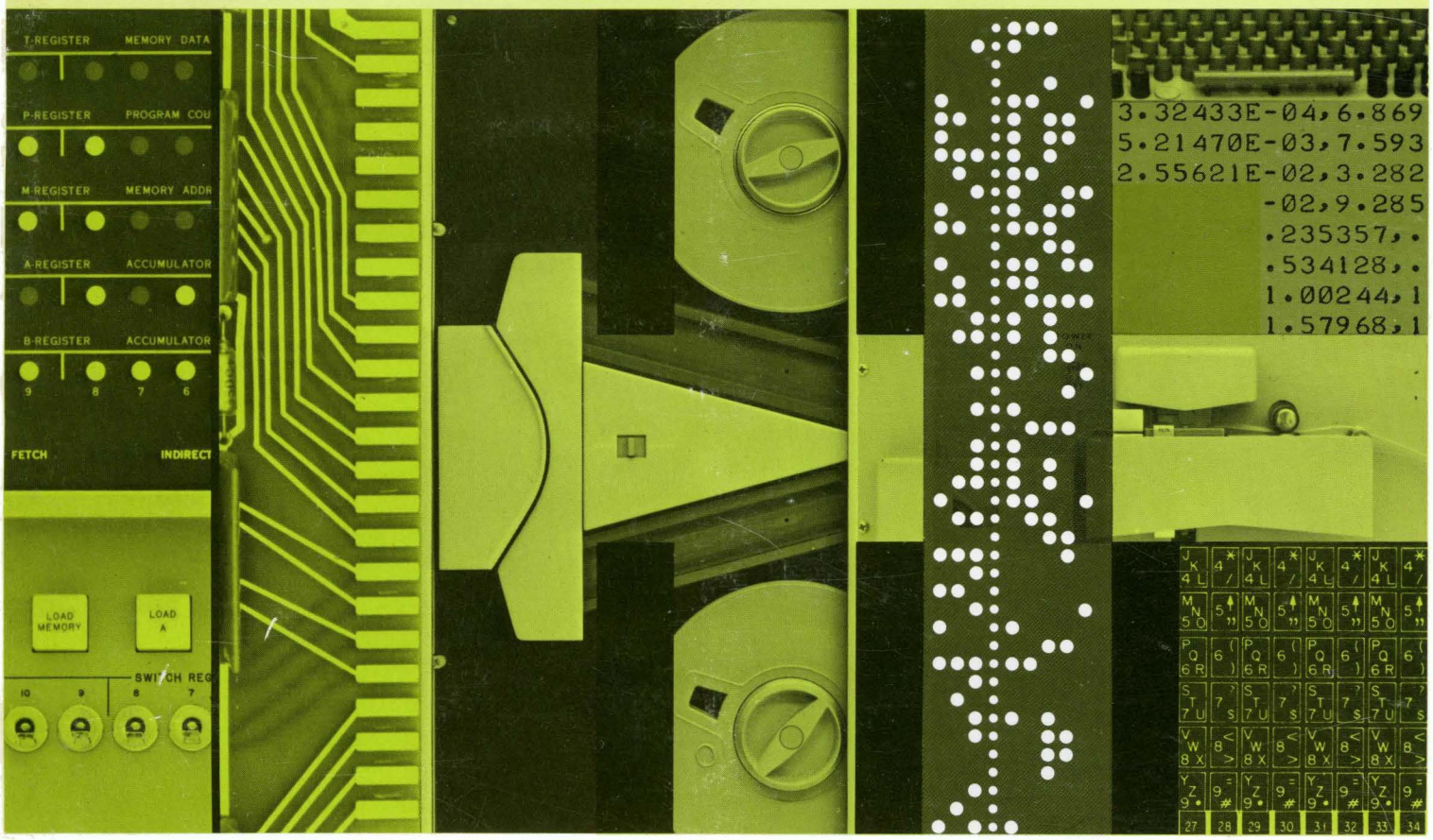
HEWLETT hp PACKARD

# COMPUTER MAINTENANCE COURSE




VOLUME III

2114A CENTRAL PROCESSOR UNIT

# HEWLETT-PACKARD

## COMPUTER MAINTENANCE COURSE

## VOLUME III

## STUDENTS MANUAL

# 2114A
# CENTRAL PROCESSOR UNIT

(HP STOCK NO. 5950-8705)

## -NOTICE-

The information contained in this manual is for training purposes only. Consult the Hewlett-Packard documentation supplied with the computer for current information concerning the specific computer system furnished.





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# FOREWORD

This 2114 A Maintenance Training Manual is written for the service technician responsible for actual repair and maintenance of the computer. It is the intention to provide a detailed description of the circuits where the operation is not obvious. The availability of the computer manuals volumes 1, 2, and 3 is assumed.

The material will be used for the introductory training course for the 2114A Computer. The course material on programming is a prerequisite (especially the machine language - word formats and machine instructions). The instructor will spend significant time in introducing the machine block diagrams, timing signals, and bus organization. The present volume presents these concepts in somewhat abbreviated form, and continues with specific circuit description. This will provide the student with supplementary study material and a reference volume.

The material is adequate for an experienced technician as a brief introduction to the specific circuits used in the 2114A. It is hoped it will also provide a handy reference volume when troubleshooting a malfunction in the 2114A Computer or its system.

If is assumed that the technician understands the function and operation of common test equipment (like oscilloscopes and voltmeters). The general purpose, description, and utilization of digital logic elements is readily available. Only the peculiarities of the TTL logic family as it relates to understanding the 2114A circuits and recognizing malfunctions are presented.

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introduction I

central processor unit II

section memory III

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# introduction

# SECTION I
# INTRODUCTION

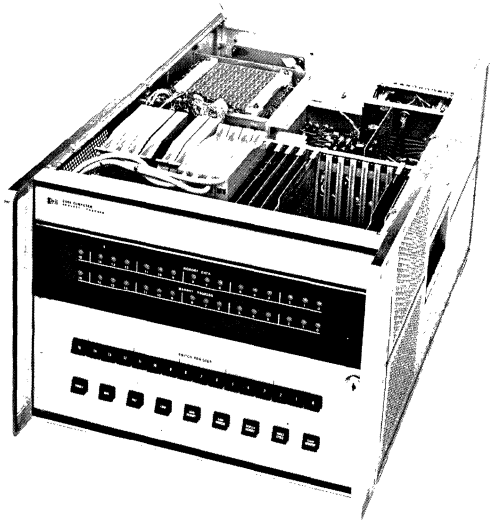


Figure 1-1. 2114A Computer

## 1-1. LOGICAL TROUBLESHOOTING

The operating computer system is rather complicated. There are certain techniques that the technician can use to simplify the troubleshooting problem. These techniques allow the isolation of possible faults to smaller functional blocks.

Try to determine the nature of the difficulty from the person reporting a malfunction. Try to outline briefly the software program being used. How was it expected to function? What were the actual results? Hopefully problems associated with the misuse of hardware or simple operating errors can be caught at this point.

## 1-2. HARDWARE PROBLEMS

Many reported problems have no hardware basis. It is usually good to begin by trying to run the diagnostic tests. This forms the basis of a go - no go decision, and helps determine the subsequent course of action. A fault which doesn't prevent the loader operation can be determined by the use of the diagnostic listings.

When the fault is serious enough to prevent the use of the loader the following order may prove helpful (Paragraphs 1-3 to 1-5). Check the power supply voltages (both D.C. level and A.C. ripple). Check the status of the PWF and PON signals. The computer will not operate without these.

## 1-3. FRONT PANEL CONTROLS AND INDICATIONS

All boards associated with the Memory and I/O can be removed. This would not be necessary unless it was suspected that certain buses might be shorted on the Memory or I/O boards.

With the Central Processor Boards installed proper operation of certain front panel controls can be ascertained. The M-Register should increment by SINGLE CYCLE, LOAD MEMORY, DISPLAY MEMORY, or RUN. The switches should operate, with lamps indicating their state. Contents of the A, B, T, and M-Registers should be capable of being set by LOAD MEMORY, or LOAD ADDRESS in any bit combination.

Difficulty in these tests can be diagnosed and repaired before proceeding. The duplicate Arithmetic Logic assemblies permits board exchange in those functions. Once this section appears to be functioning properly the Memory boards can be re-installed. Refer to 2114A Computer Manual Volume 2, Section 5-7 entitled "PRETEST CHECKOUT".

## 1-4. MEMORY SECTION

The installation of the Memory section will allow a much fuller exercise of the machine instruction set. Simple tests include loading "ones" and "zeros" through a given memory area, and displaying to determine that it is being done properly. This will give a tentative indication that the operation of the Sense Amplifiers, Inhibit Drivers, and Driver switches is normal. The Driver switches can be exchanged to compare symptoms. In the 8K installations the Sense Amplifiers and Inhibit Drivers can also be switched.

The use of the Parity Error assembly can be especially helpful for diagnosing memory problems. The Memory Address Register on the Parity Error assembly provides the address of the error. It is helpful when a single core is giving difficulty or intermittent problems exist.

The Memory Address test provides a fairly straightforward test of the memory and can be toggled in.

MEMORY ADDRESS TEST

| LOCATION | OCTAL CODE | | ASSEMBLY LANG. |
|---|---|---|---|
| 00002 | 006204 | | INB, CME |
| 00003 | 060023 | | LDA FRST |
| 00004 | 150000 | CMPAR | CPA Ø, I |
| 00005 | 002001 | | RSS |
| 00006 | 102000 | | HLT |
| 00007 | 052022 | | CPA LAST |
| 00010 | 024014 | | JMP START |
| 00011 | 002004 | | INA |
| 00012 | 024004 | | JMP CMPAR |
| 00013 | 000000 | | NOP |
| 00014 | 060023 | START | LDA FRST |
| 00015 | 170000 | STORE | STA Ø, I |
| 00016 | 050022 | | CPA LAST |
| 00017 | 024002 | | JMP CMPAR-2 |
| 00020 | 002004 | | INA |
| 00021 | 024015 | | JMP STORE |
| *00022 | 007777 | LAST | OCT 7777 |
| 00023 | 000024 | FRST | OCT 00024 |

* For 8K machines (22) 017777

Use 007677 or 017677 if you do not desire to test protected area.

Starting Address 14

Depress PRESET and RUN. The 2114A shall run. If it halts, there is an address error.

Extend bit shall blink on and off.

Locations 00022 and 00023 may be changed to test any core area.

## 1-5. LOADER OPERATION - DIAGNOSTICS

After the CPU and Memory have been checked out the Diagnostic tests provide a powerful tool for continued fault analysis. The tests should be utilized in the order prescribed in the Computer Manual Volume Two Part Three. Each succeeding diagnostic test requires functions tested in prior tests.

After the Diagnostic Tests have provided error indications the information in Chapter Two on detailed signal versus machine instruction may prove helpful. This provides convenient cross reference of the machine functions which are required in performing each instruction.

It is not possible to suggest many short programs to test each function because of the large number of combinations. The initialization of core is often helpful. Halt instructions loaded throughout core helps when improper addressing or jumps are experienced. Clearing core with zeros may also prove helpful.

The "Mickey Mouse" test is a very simple, and yet rather powerful test of the adder circuits on the Arithmetic Logic card. Set MEMORY switch (inside front panel) to OFF position. Load Ø2ØØØ1 in A-Register. Load Ø4ØØØ1 in the B-Register. Set address to Ø. Push RUN. Watch the M-Register increment. In about two seconds the program enters a tight loop. Push HALT. A-Register contains ØØØØØ2, B-Register contains 117776. A contains an effective NOP. B contains a JSB which (because of the MEMORY OFF) goes back to address Ø. Return Memory switch to NORMAL position after completing test.

Some computer problems are difficult. It takes an extremely talented person to diagnose and repair a computer without wasting time on false avenues. It is helpful to write simple notes which list the problems encountered, suspected cause, the signals observed and the results of the investigation.

Stepping back and viewing the proceedings in an objective manner periodically is time well spent. (Refer to figure 1-11.)

## 1-6. I/O DEVICES AND SOFTWARE

Once the basic processor has been repaired and tested the I/O interfaces and peripherals can be installed and tested. It is helpful to do this one device at a time.

When the entire computer system has been checked in this manner the hardware confidence level should be quite high. The clean bill of health on the hardware system suggests an attempt at the program conditions which initially failed to operate properly. This may prove to be the problem area. Unfortunately, it may prove to be the most difficult part to the technician because of the intimate marriage between the software and hardware. Trying to understand a strange program, which is probably not documented with flow charts and description, is difficult for even top notch technicians with wide experience. Solving a software problem like this is one of the highest compliments to a technician's expertise.

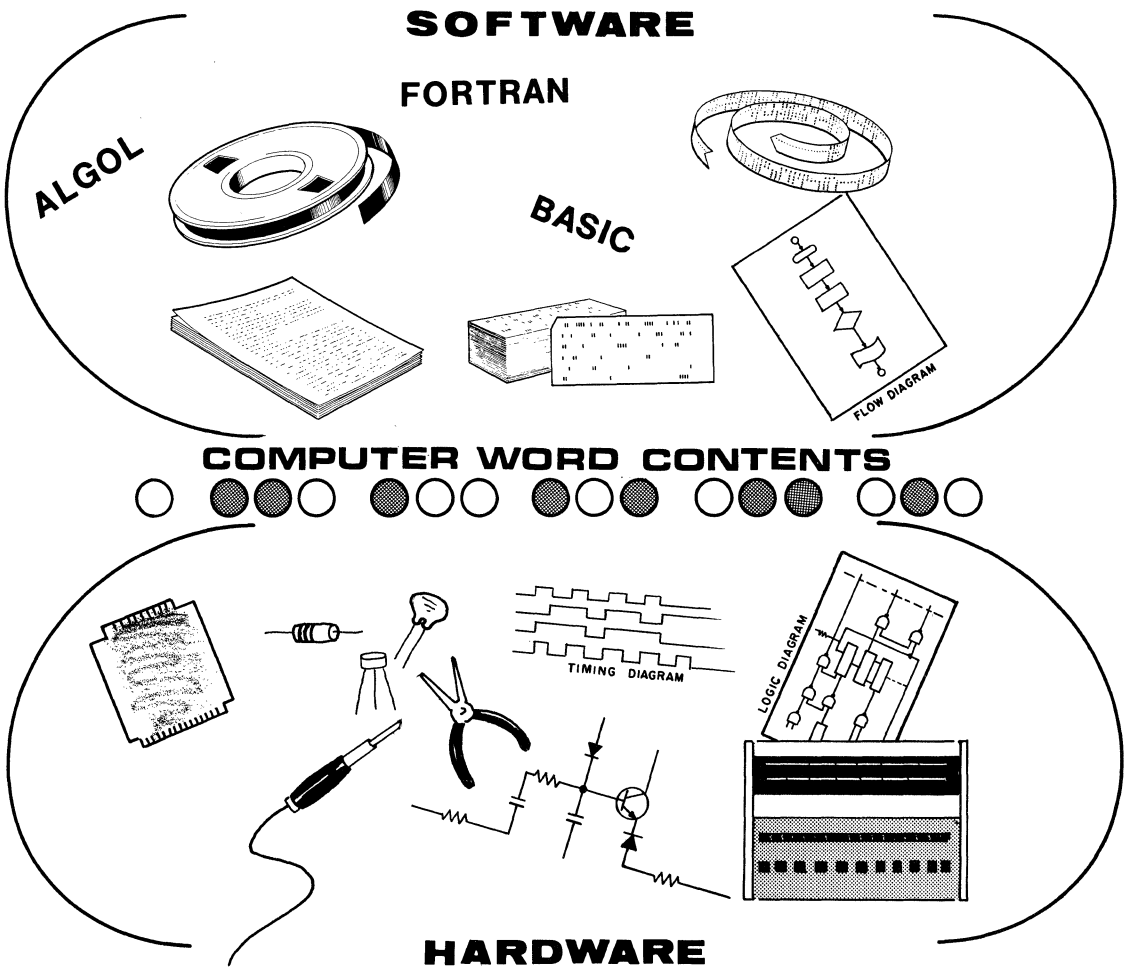



Figure 1-2. Software - Hardware

## 1-7. LOGIC PROBE

The HP 10525 Logic Probe is a powerful troubleshooting aid in servicing the computer. It is ideal for detecting pulses of short duration and low repetition rates that are normally difficult to observe on an oscilloscope. It is powered from the +5 volt bus.

A single pulse is stretched so as to provide a visual indication. A logic level or pulse greater than +1.4 volts is stretched to illuminate the probe light for Ø.1 seconds minimum. A low logic level or pulse less than +1.4 volts will extinguish the light for at least 0.1 seconds. A pulse train of higher repetition rate will result in a dim light level.

The real power of the logic probe becomes evident when trying to determine the proper operation of the front panel controls. LOAD MEMORY, SINGLE CYCLE and the other controls produce computer signals which are virtually impossible to observe on an oscilloscope, but give a positive indication with the logic probe.

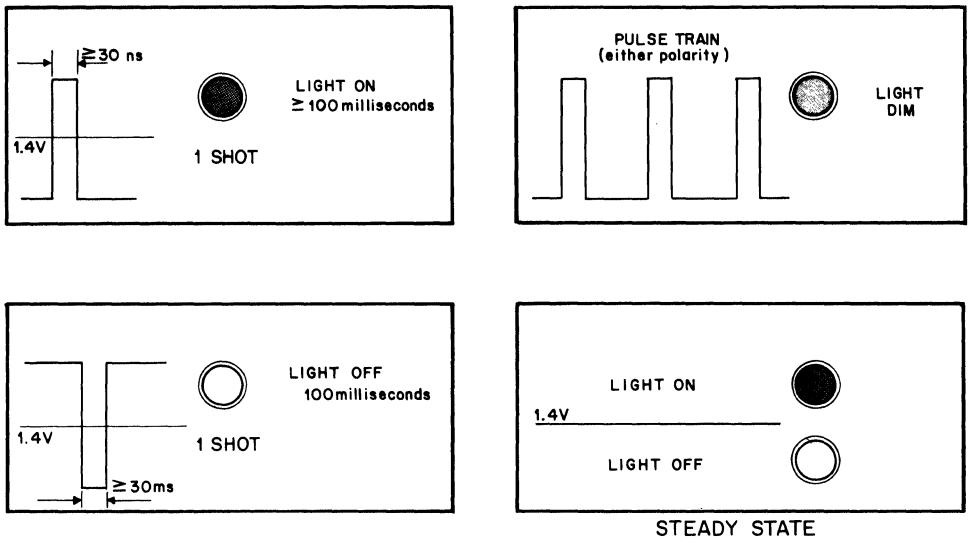



Figure 1-3. Probe Operating Conditions

1-8. INTEGRATED CIRCUIT DESCRIPTION

1-9 The logic type selected for use in the 2114A Computer is the TTL family. It requires only a +5.0 volt power supply and ground. The HP 1820-0956 CTL (Complementary Transistor Logic) AND gate is used to buffer input and output levels for compatibility with the HP family of I/O interface devices. Refer to Table 1-1 for stock number and description.

1-10. The TTL family is a high speed saturating logic. Characteristics for the normal family follow. Typical propagation delay is 13$\mu$sec per gate and 40$\mu$sec per flip flop. Power dissipation is 10 MW per gate and 60 MW per flip flop. Operating temperature range is 0°C to 70°C which is more than adequate for the 2114A.

1-11. The logic is built around the NAND gate. A sample of the circuit follows with approximate resistor values shown.

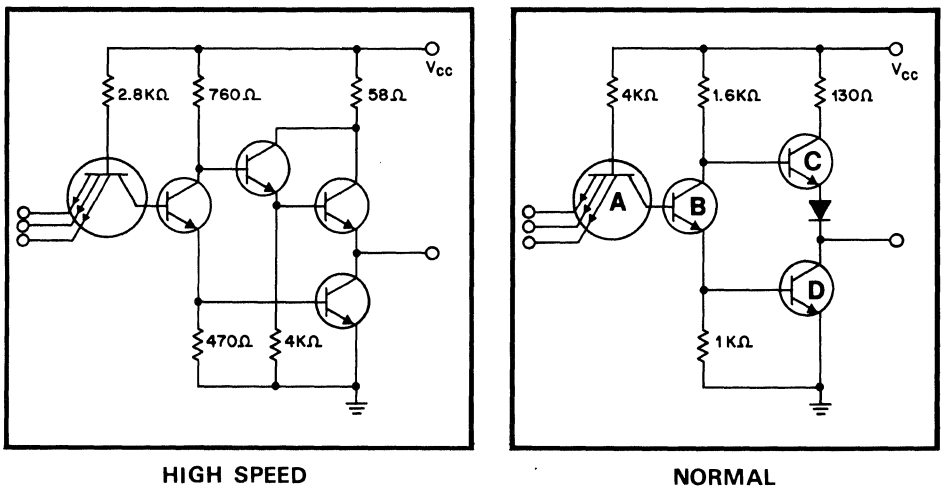



Figure 1-4. TTL "NAND" Basic Building Block

Table 1-1. 2114A Integrated Circuit Components

| HP Stock Number | Description | Mfg. Type |
|---|---|---|
| 1820-0054 | *TTL Quad 2-input NAND | 7400N |
| 1820-0063 | Dual 2-wide 2-input AND-OR-INV | 7451N |
| 1820-0065 | J-K FF | 7470N |
| 1820-0068 | Triple 3-input NAND | 7410N |
| 1820-0070 | 8-input NAND | 7430N |
| 1820-0071 | Dual 4-input NAND | 7440N |
| 1820-0074 | 4-wide 2-input AND-OR-INV | 7454N |
| 1820-0075 | Dual J-K Master/Slave FF | 7473N |
| 1820-0077 | Dual D FF | 7474N |
| 1820-0084 | 4-wide 2-input AND-OR-INV Exp | 7453N |
| 1820-0085 | Dual 4-input Exp | 7460N |
| 1820-0105 | Linear Ckt Voltage Reg | SL6160 |
| 1820-0111 | 1 out of 10 Decoder | 930159X |
| 1820-0127 | Quad 2-input NAND | 900259X |
| 1820-0129 | Triple 3-input NAND | 900359X |
| 1820-0130 | Dual 4-input NAND | 900459X |
| 1820-0132 | Hex Inverter | 901659X |
| 1820-0183 | Differential Amplifier | CA3028 |
| 1820-0301 | Quad Latch Buffer (D FF) | 7475N |
| 1820-0305 | JK M/S FF | 7483N |
| 1820-0310 | DTL Triple 3-input NAND | 15862N |
| 1820-0327 | Quad 2-input NAND | 7401N |
| 1820-0328 | Quad 2-input NOR | 7402N |
| 1820-0370 | HS Quad 2-input NAND | 74H00N |
| 1820-0371 | HS Triple 3-input NAND | 74H10N |
| 1820-0372 | HS triple 3-input AND | 74H11N |
| 1820-0374 | HS Dual 4-input AND | 74H21N |
| 1820-0377 | HS Dual 2-input AND-OR-INV Exp. | 74H50N |
| 1820-0378 | HS Dual 2-wide 2-input AND-OR-INV | 74H51N |
| 1820-0379 | HS 4-wide 2-2-2-3-input AND-OR Exp. | 74H52N |
| 1820-0380 | HS 4-wide 2-2-2-3-input AND-OR-INV Exp. | 74H53N |
| 1820-0381 | HS 4-wide 2-2-2-3-input AND-OR-INV | 74H54N |
| 1820-0382 | HS 2-wide 4-input AND-OR-INV Exp. | 74H55N |
| 1820-0383 | HS Dual 4-input Expander | 74H60N |
| 1820-0384 | Triple 3-input Expander | 74H61N |
| 1820-0956 | CTL Dual 2-input AND Buffer | SL3459 |

* Except DTL and CTL as noted.

A high speed version is used in some applications where higher fan out or improved speed is necessary. The power requirement doubles and the propagation delay halves compared to the normal unit.

1-12. OUTPUT

The totem pole output in the normal device gives a "one" output impedance of about 70 ohms. This helps provide good noise immunity. The logical "one" output has a guaranteed value of 2.4 volts minimum. Fan out, and drive criteria are based on a minimum of 2.0 volts which provides a noise immunity safety band.

1-13. The logical "zero" level is guaranteed at 0.4V maximum. Fan out and drive requirements are determined at 0.8V which provides a noise immunity safety band. An individual gate will normally change state as the input increases to about 1.4 volts.

1-14. CIRCUIT OPERATION

The TTL family is designed around the basic NAND circuit. Any number of emitters can be provided in the input transistor. Any one of the emitters pulled down to a logical "zero" will saturate transistor A. Refer to Figure 1-4. The output is pulled to ground by transistor D. Base drive to transistor D is provided through transistor B.

When all emitters are at the logical "one" level transistor A is non conducting and transistor C derives its base drive through the 1.6K resistor to the +Vcc bus.

1-15. FAILURE

The common failure modes include shorting in the output transistors which can hold the output either high or low. Failure in the input typically shorts emitter to emitter. This can pull an interconnection bus high by virtue of the shorted emitters.

1-16. OR TYING

The totem-pole output precludes OR tying gates together. Figure 1-5 shows the open collector output (alongside the normal output). One quad 2-input NAND gate is made this way - HP Stock No. 1820-0327. It allows OR tying for negative true signals. It is used extensively in the 2114A logic design, refer to the Bus structure design on the Arithmetic Logic assembly.

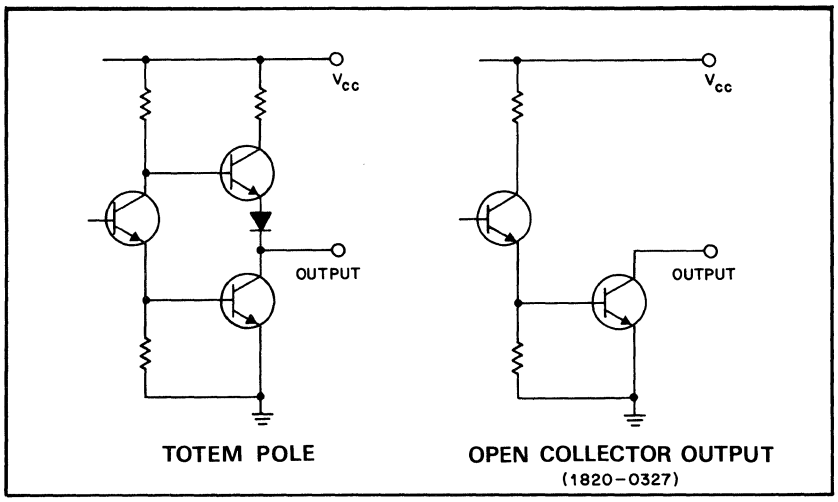



Figure 1-5. Open Collector

## 1-17. CTL COMPARISON

The CTL family used extensively in Hewlett-Packard computers differs somewhat in characteristics from the TTL logic. It requires a +4.5V supply and a -2.ØV supply. The input circuit is a transistor base with the tie down resistors to -2.ØV or ground. The output is an emitter follower and can be OR tied in positive true direction. A logical "zero" output is -Ø.3 volts. A logical "one" output is +2.3 volts.

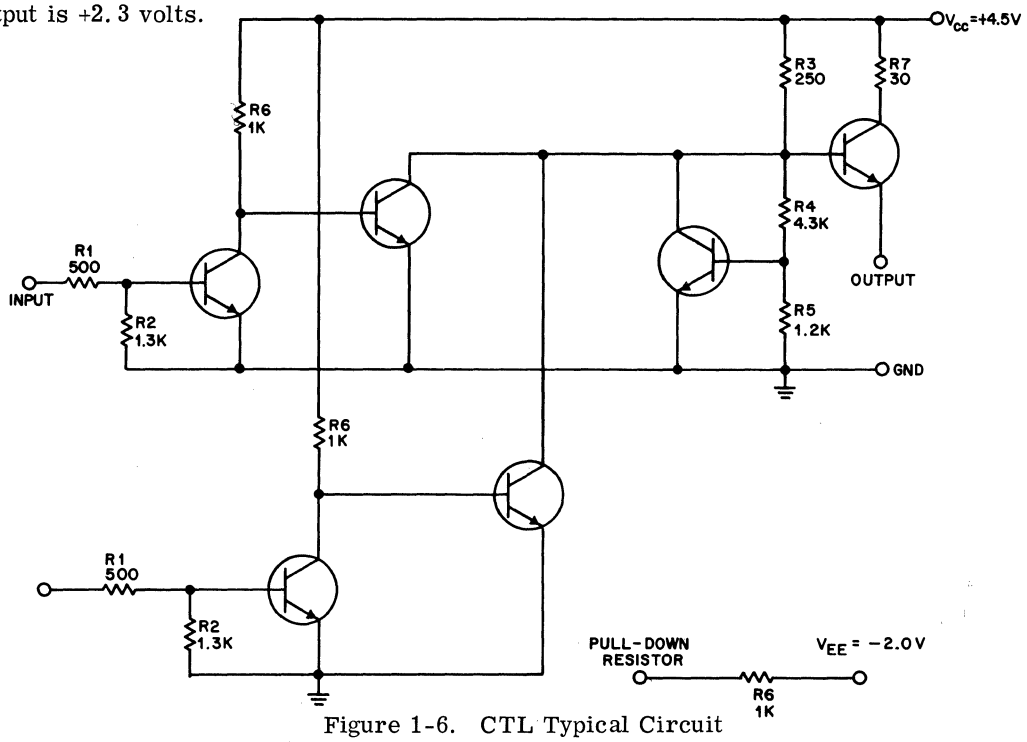



Figure 1-6. CTL Typical Circuit
(1820-0956)

## 1-18. TYPE D FF

A commonly used TTL circuit is the 1820-0077 Dual D type positive edge triggered flip flop. The FF is made up of NAND gates as shown in Figure 1-7. The preset and clear signal inputs are both negative true. Either (or both) negative will inhibit the FF operation.

When preset and clear are both high the state of the D input establishes certain conditions. The change in the clock input from low to high state will complete the establishment of the FF state. A subsequent change of D input level (even with the clock remaining high) will not affect the FF output. Figure 1-7 shows the functional block diagram.

## 1-19. AND-OR EXPANDERS

Because of the OR tie limitations inherent in the totem pole output stage a family of expandable OR circuits was developed. The basic circuit is an AND-OR structure. The output may be true or inverting. The OR or NOR output stage may accept additional inputs. These are of two types. In one a single true input permits an additional OR, the other requires both true and complementary inputs for the additional OR input.

## 1-20. BINARY FULL ADDER

The Full Adder is used on the arithmetic logic assembly for arithmetic adding operations. The R and S buses and the carry in are compared two by two. If at least two are high a carry out (negative true) is generated.

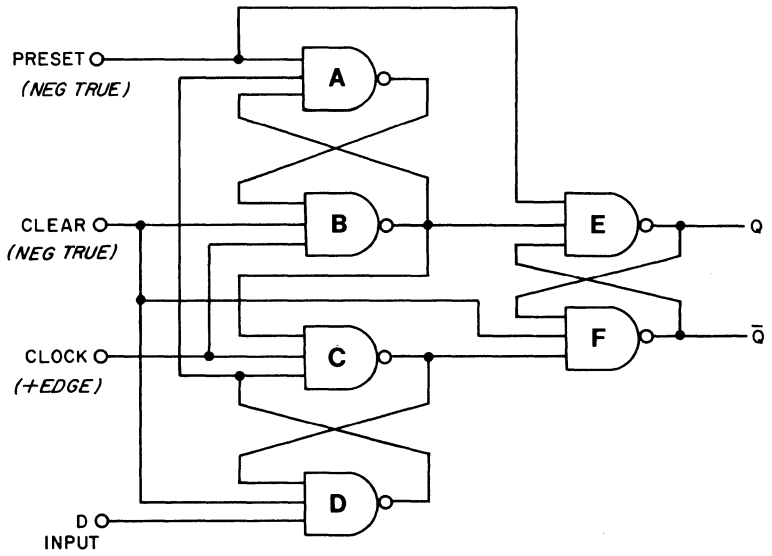



Figure 1-7. D Type Flip Flop (+Edge Trigger)

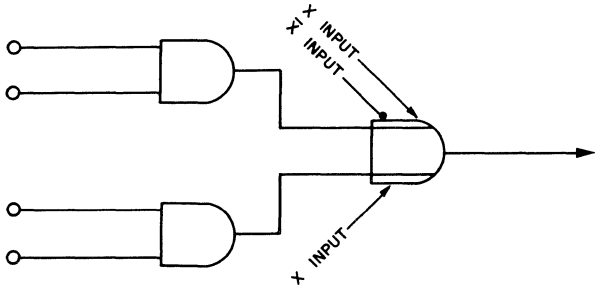



Figure 1-8. AND-OR Expander

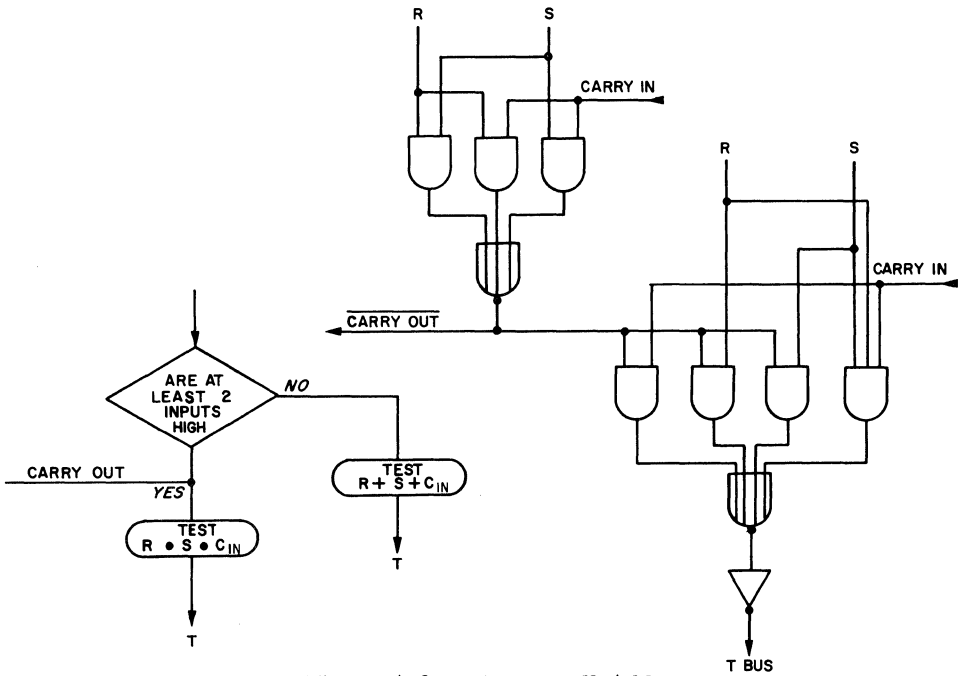



Figure 1-9. Binary Full Adder

If no carry out is generated either R, S, or Carry in can provide a T bus output. The presence of R, S, and Carry in will also generate a T bus output.

A glance at the adder circuit on the Arithmetic schematic will disclose that the R and S inputs are inverted in the second and fourth circuits, and the T bus output is inverted in the first and third. The polarity of the Carry out changes between each stage.

The parallel add - serial carry requires a typical delay of 8 $\mu$sec per stage. Whenever the 2114A uses the full adder two timing cycles are used (500 nsec) to insure adequate time for completion.

## 1-21. "D" LATCH

The flip flop follows the D input so long as the clock input is positive. The current FF condition is retained as the clock goes negative. HP Stock No. 1820-0301. Refer to figure 1-10.

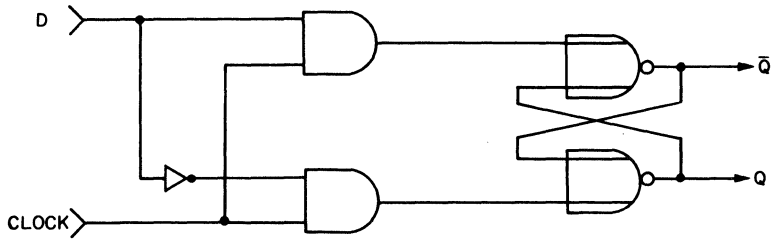



Figure 1-10. D Latch (1820-0301)

## 1-22. IC REPLACEMENT

The replacement of Integrated Circuit packs on the Printed Circuit board requires care. Too much heat can "measle" the board ruining its appearance. Too much heat or aggressive mechanical manipulation can damage the plating around holes.

An effective way to replace an IC pack follows: Cut the body out and remove each leg individually. A sharp diagonal cutting pliers will allow cutting each leg individually. Care must be exercised so that undue stress is not produced which might damage the plated hole. Use a light soldering iron with a tiny tip to remove each leg (from the component side). Each hole can be cleaned out with a round tapered toothpick (its size may have to be reduced to fit in the hole) or a vacuum device.

The new IC pack can be inserted, and carefully soldered. The rosin flux can be removed with Alpha cleaner (or other commercial product).

**If you're not making progress _____**
**REVIEW THE OVERALL SITUATION**

FIG. 1-11

# central processor unit

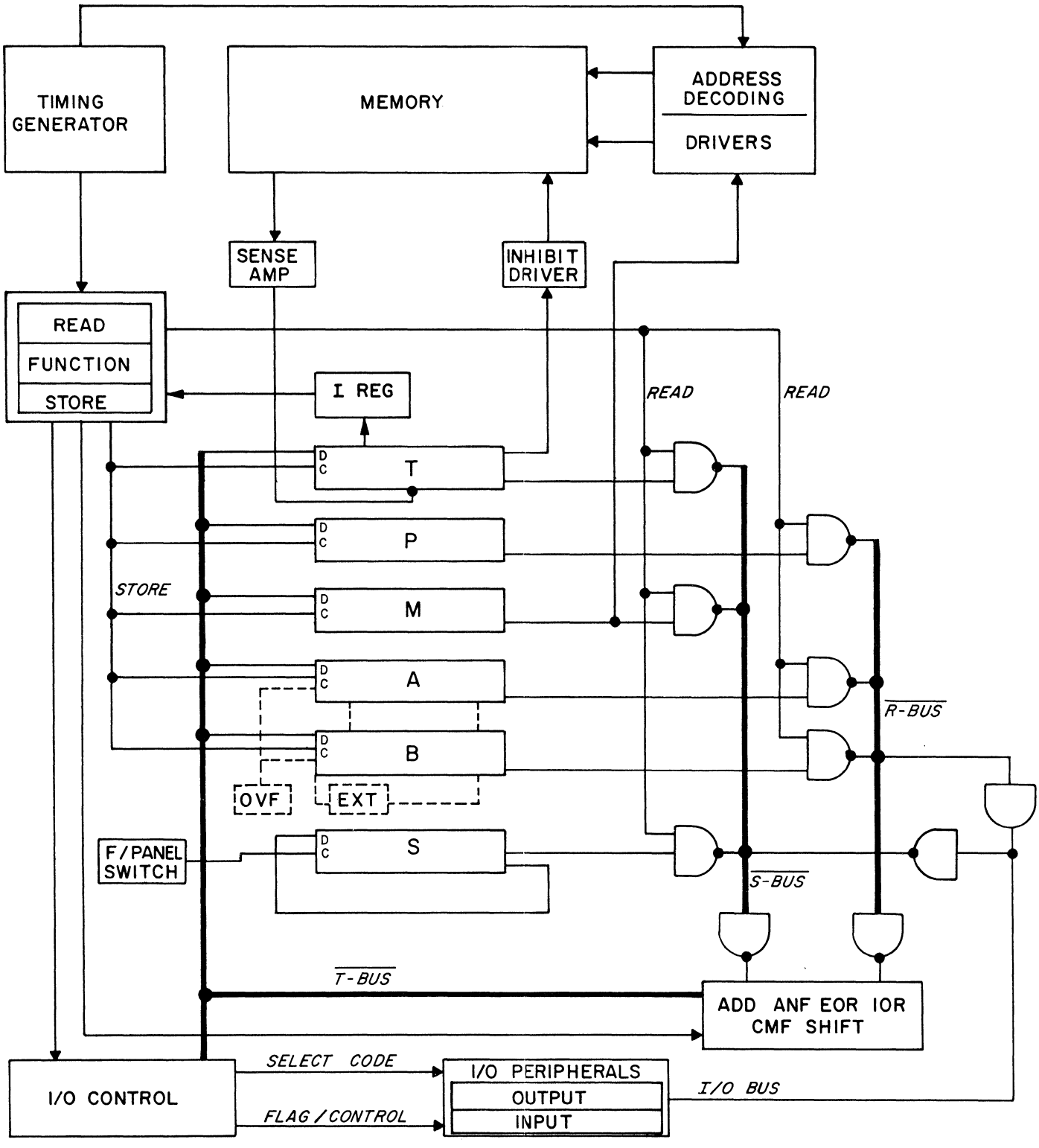



Figure 2-1. Bus Structure

# SECTION II
# CENTRAL PROCESSOR UNIT

## 2-1. INTRODUCTION

The central processor unit of the 2114A Computer consists of 7 printed circuit assemblies: 4 identical arithmetic logic assemblies, 1 timing generator, 1 instruction decoder, and 1 shift logic assembly. In conjunction with the front panel the central processor unit can accomplish certain arithmetic operations. It is possible to determine the operation of certain functions without any memory installed. The content of this chapter will be limited circuit description on the arithmetic logic and timing generator boards and fairly extensive analysis of the computer operation codes including the signals that they utilize. It is assumed that the service technician understands the operation of the simple TTL logic components utilized in the central processor design.

## 2-2. BUS STRUCTURE

Figure 2-1 shows a brief logic diagram of the 2114A Bus Structure. This consists of certain logical functions which can be separated by function. At the top of this Figure the memory module, the address decoding and driver switches, the sense amplifier, and inhibit driver are shown. The M-Register contains the memory address information for the core. This information is used by the driver switch assemblies to address the proper X and Y wires that traverse the core. The bit planes are interrogated by addressing currents. The sense amplifier is used to set the T-Register, and the T-Register is used in turn to drive the inhibit drivers to determine the proper writing data information.

This memory section consits of the 2 driver switch boards and the memory module which can contain a 4 K or an 8 K unit. One each of the sense amp and inhibit driver assemblies are required for each 4 K module. The minimum memory board count is 4 boards, the maximum would be 6 boards. The parity error is an additional board when this option is used. It is not shown on the bus structure diagram.

## 2-3. REGISTERS AND BUSES

The registers contained in the 2114A Computer are the T, P, M, A, B, and Switch Registers. These registers are contained on the arithmetic logic card (4 bits per board). It requires 4 Arithmetic Logic cards to provide all 16 bits. (Refer to Figure 2-1.) The information from these registers can be read onto the S bus or R bus. The information on the R and S buses is manipulated with certain logical functions and the resultant appears on the T bus. The T bus can be stored in each of the 5 registers. The outputs from the registers are gated to the negative true S bus, and negative true R bus. Both of these buses are inverted, which provides the positive true S bus and R bus. It is the positive true S and R buses on which the logical functions are accomplished. The output goes to the T bus which is negative true. This negative true T bus provides inputs to the 5 registers. The limitations of the TTL logic prescribes the polarities of this bus structure since the only gate which can be OR tied must be OR tied in the negative true direction. The T bus negative true provides the D inputs to the 5 registers. The positive true output from these 5 registers is taken from the $\overline{Q}$ side of the flip flops.

## 2-4. SWITCH REGISTER

The input to the Switch Register is the output of the proximity switch circuit on the front panel. Each time this proximity switch is operated the Switch Register toggles. Note that the output of the Switch Register comes from the Q side of the flip flop.

## 2-4. OVERFLOW AND EXTEND

The Overflow Register provides a one bit register to determine when an arithmetic operation causes the A-Register or B-Register to overflow. The Extend Register couples the A-Register and B-Register for rotation to the left or to the right. It also indicates arithmetic carry from bit 15.

## 2-6. READ - STORE - FUNCTION

The other signals required by the design of the central processor unit are the reading and storing signals and other logical functions. These are generated on the Instruction Decoder assembly and the Shift Logic assembly. The I-Register is located on the Instruction Decoder assembly and includes bits 10 through 15.

## 2-7. I/O INTERFACE

The I/O Control assembly provides the flag, control, and interrupt circuitry for servicing the I/O peripheral devices. It encodes the select code information which is hard wired to each individual I/O slot. The I/O interface cards provide input/output registers. These registers utilize the input/output bus for transferring data from the device to the computer and from the computer to the device. The I/O bus is read into the S bus for input information. The I/O bus receives information from the R bus for output operations.

The I/O Control assembly also provides select code and interrupt information for servicing I/O extender and I/O multiplex options.

## 2-8. ARITHMETIC LOGIC ASSEMBLY

The circuitry of the Arithmetic Logic assembly consists of 4 bits with the registers, bus structure, logic, arithmetic, and shift mechanisms. Figure 2-2 shows the information on the arithmetic logic card for bit 11. There are certain inputs and outputs that differ for specific bits on the arithmetic logic card. You will note that the signals are the specific inputs associated with bit 11.

## 2-9. HARDWARE REGISTERS

The arithmetic logic assembly contains 6 hardware registers, the T, P, M, A, and B-Registers and the Switch Register. It will be noted that the inputs to the T, P, M, A, and B-Registers is the T bus negative true to the input of this D type positive edge triggering flip flop. In order to utilize the information contained in these registers it is necessary to read information out of the registers onto the bus structure. After manipulation it is stored back in the appropriate register. The clock inputs to the T, P, M, A, and B-Registers allows storing the appropriate information from the T bus negative true. The 5 specific store instructions are the STBB, STBA, STBT, STM, and STP. The latter two being for bits 10-15. On the other arithmetic logic boards provisions are made for storing in the M- and P-Registers bits 0 through 9. Information is read from the 6 registers into the S and R bus with the following 6 instructions: ISR, RMSB, RTSB, RBRB, RARB, and RPRB.

## 2-10. S-R BUS

The contents of the hardware registers are read onto the S bus negative true, and R bus negative

true. Each of these buses is inverted generating the R bus and S bus positive true as well. The output from the logical and shift operations is on the T bus negative true. This T bus negative true provides the D inputs to the T, P, M, A, and B-Registers.

## 2-11. LOGIC OPERATIONS

The contents of the R and S buses are manipulated using 5 logic instructions Exclusive Or Function (EOF), And Function (ANF), Complement Function (CMF), Inclusive Or Function (IOF), and Add Function (ADF). The full adder for bit 11 is one quarter of the pack. The pack provides internal carry in from lower bits and external carry out at the end of each 4th bit. Interior carries (between bits on the card) are not required outside of the pack.

## 2-12. SHIFT - ROTATE

The shift and rotate functions on the arithmetic logic card are provided by 5 signals. These are: Shift Left Magnitude (SLM), Shift Right Magnitude (SRM), and Rotate Left 4 (RL4). Since this figure is drawn representing bit 11 the specific inputs R bus bit 12 for a rotate or shift right, R bus bit 10 for shift or rotate left, and R bus 7 for rotate left 4 are shown. The Set Address Loader (SAL) gate is in the same general area on the assembly.

## 2-13. I/O BUS

The I/O bus is brought to the arithmetic logic board. It is read into the S bus with the IOI input signal. It is possible to output from the R bus using IOCO, the input/output control signal. The Switch Register is also handled in the I/O system. The input to the Switch Register is a clock signal produced by the proximity switches on the front panel. The output $\overline{Q}$ is cross coupled providing the D input to the flip flop. This allows the flip flop contents to toggle each time the proximity switch is touched. The contents of the switch register are enabled to the bus structure with the Enable Switch Register (ISR). The contents of the A-Register or B-Register can be output to the Switch Register in order to illuminate the Switch Register lamps. This is accomplished by clearing the contents of the Switch Register with the Clear Switch Register (CSR) and then setting the Switch Register with the SSR signal which sets the Switch Register with the contents of the R bus.

## 2-14. REGISTER DISPLAYS

The contents of the hardware registers are available for driving lamp displays. The T-Register and M-Register are displayed on the 2114A front panel. The Switch Register is displayed on the front panel by lamps physically located under the proximity switch associated with the bit. The contents of the P-Register, A-Register, and B-Register do not have transistor drivers. The contents of those respective registers are available through isolation resistors on the 48 pin connector of the Arithmetic Logic board. External devices such as the Register Display Fixture utilize these outputs with their own transistor drivers to illuminate all of the hardware registers.

## 2-15. SYSTEM TIMING GENERATOR

The system timing generator assembly contains five significant circuits.

## 2-16. OSCILLATOR AND DIVIDER

Figure 2-3 shows the schematic for the oscillator and divider circuits. The oscillator is an integrated circuit design utilizing an 8 Mhz crystal. The output of this oscillator has sufficient rise time to operate the clock input of the CF flip flop. The CF flip flop is a divide by 2 circuit. The clock input is 8 Mhz, the output is 4 Mhz. Thus its output period is 250 nsec. The 4 Mhz signal

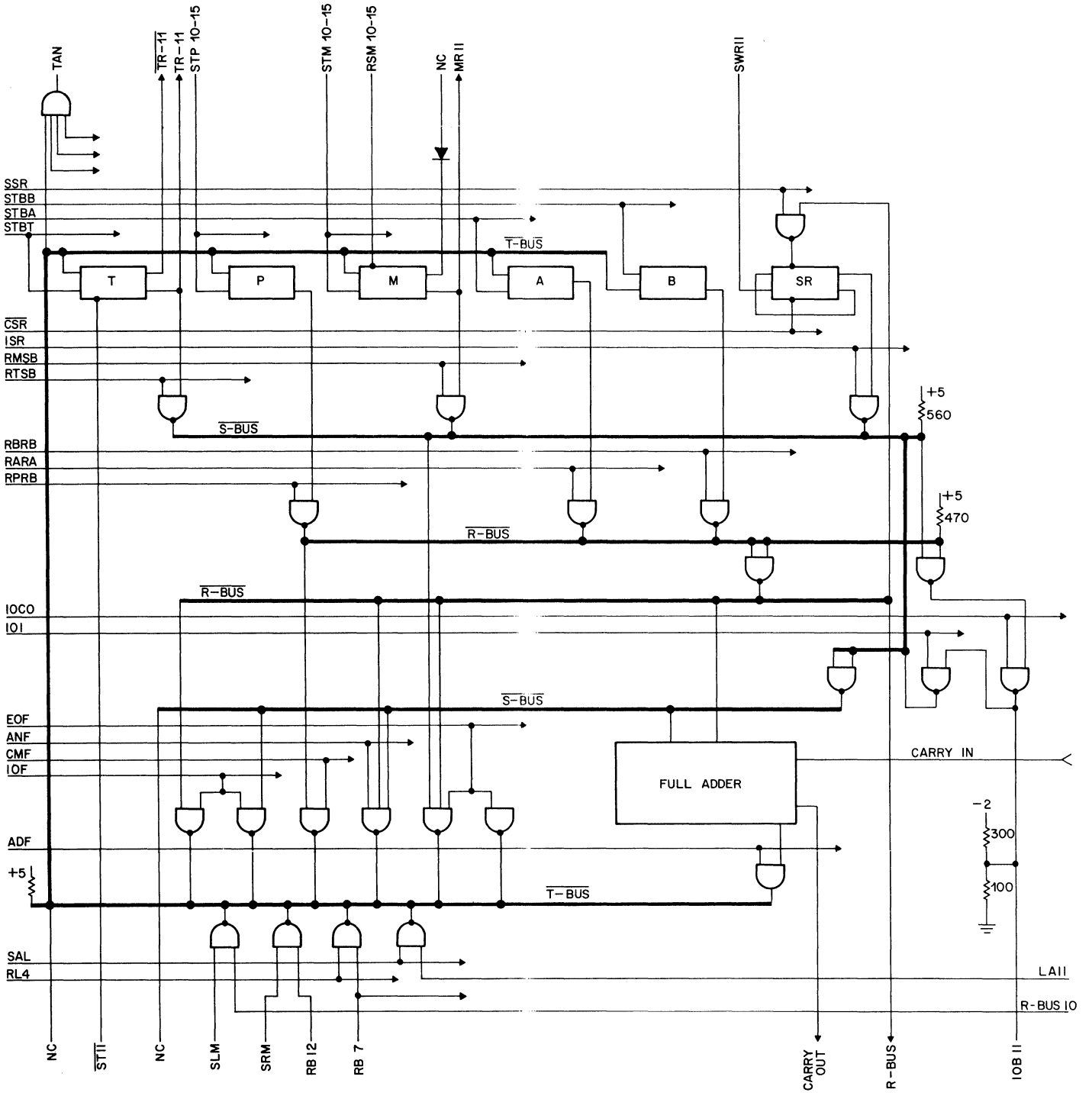



Figure 2-2. Arithmetic Logic

drives the clock inputs for the timing flip flops. The $\overline{Q}$ output drives the memory timing MST circuit. This Figure also shows the timing circuits used for generating the TS timing strobe signal. The output from integrated circuit pack MC71 pin 11 provides an approximate 120 nsec delay, and is used in the memory timing circuits.

Jumper W1 and the test points are used for in plant board test.

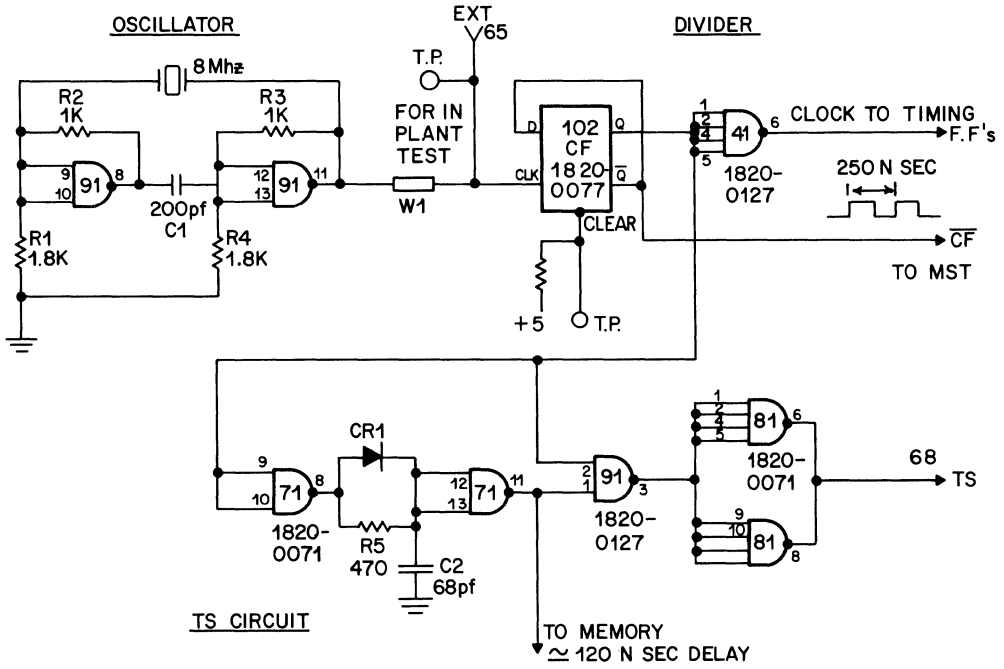


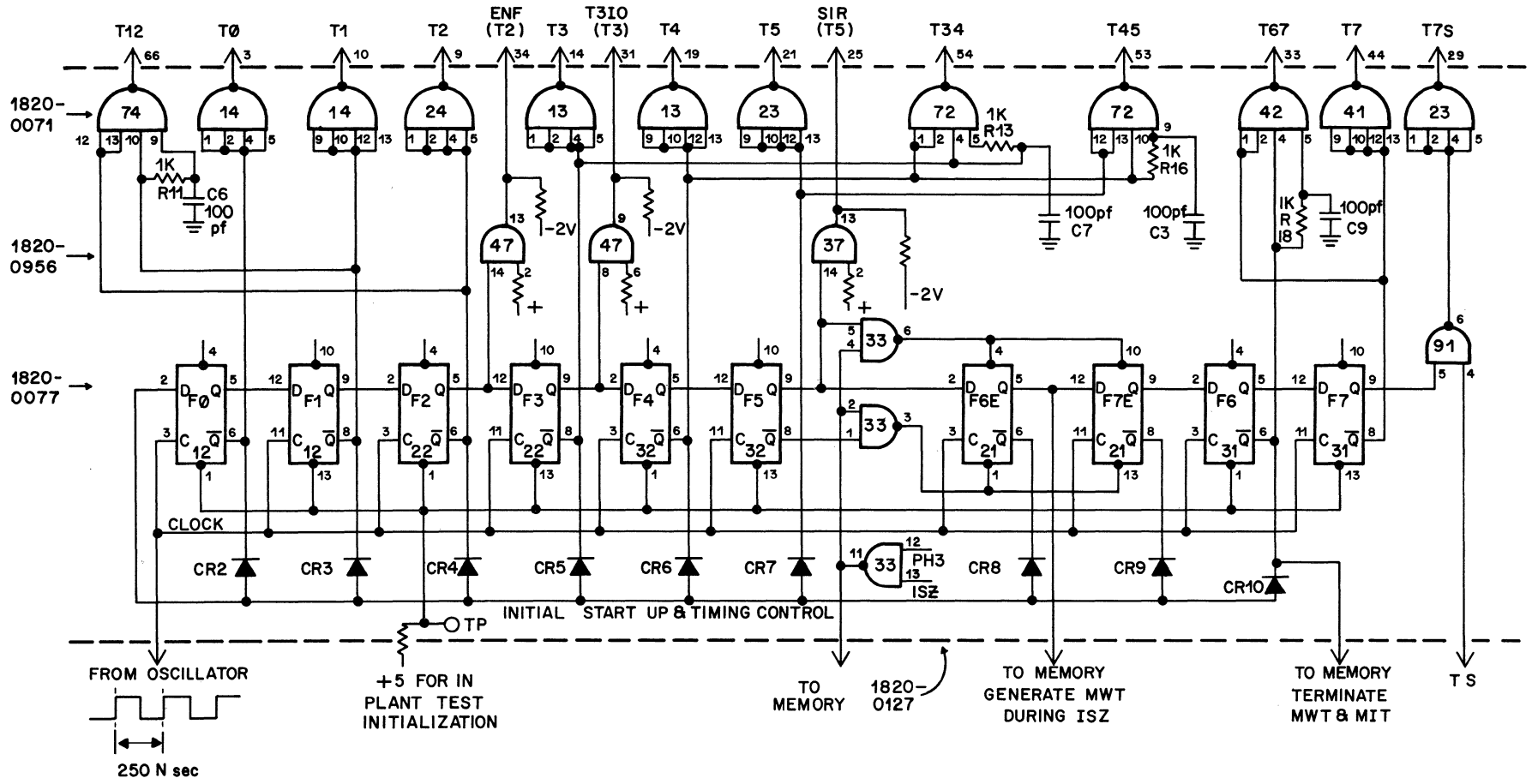

Figure 2-3. Oscillator and Divider

## 2-17. TIMING SIGNALS

Figure 2-4 shows the flip flops and buffering circuits for generating the computer timing signals. This circuit is reasonably straightforward. It consists of 8 flip flops for normal operation, plus two additional flip flops for time stretching required by the ISZ instruction. The output of the frequency divider CF flip flop in Figure 2-3 provides positive clock signals every 250 nsec. These clock signals are applied to each timing flip flop in parallel. It allows a timing pulse to propagate through the timing flip flops. The $\overline{Q}$ output of each timing flip flop drives a diode to the D input of flip flop FØ. Thus a pulse in any timing flip flop lowers the D input to flip flop FØ preventing the introduction of another timing pulse. When a timing pulse has propagated to flip flop F6 the D input to flip flop FØ is still held low. The next clock signal transfers the pulse from flip flop F6 to flip flop F7. At this point the D input to flip flop FØ goes high so that the next clock signal introduces the next timing pulse into flip flop FØ.

The outputs of the timing flip flops are buffered and provide timing signals to the computer. In addition to a normal TØ, T1, and so on, are certain composite signals. These include T12, T34, T45, and T67. The signals T2 called the ENF signal, T5 called the SIR signal, and T3 called the T3I/O, are available to the I/O section of the computer.

The operation of the pulse stretching circuits is as follows. In normal operation the ISZ signal is not present so that the NAND gate MC33 output pins 6 and 3 will normally go low when flip flop F5 is high. This negative true signal directly sets flip flops F6E and F7E. The high output from F7E allows the pulse train to propagate directly from F5 to F6. For operation with ISZ instruction during




# TIMING CIRCUITS

FIG. 2-4

phase 3 the NAND gates 33 are not enabled so that flip flops F6E and F7E are not set. The pulse train from flip flop F5 thus must propagate through the two additional flip flops. This allows the additional 500 nsec timing stretch for the ISZ instruction.

At Computer turn on the FF status is random. During the initial seven timing periods the status of the timing generator is correctly established. On each positive clock signal every pulse propagates through the flip flops, so that after a maximum of seven clock signals the proper operating conditions will have been established with one and only one pulse propagating. The computer PON signal is delayed by 300 milliseconds, thus no faulty computer operation can result during this required initialization.

## 2-18. MEMORY TIMING SIGNALS

Figure 2-5 presents the schematic for the memory timing circuit. The presence of the MTE Memory Timing Enable signal indicates that the computer is in phase 1-2-3, Memory On switch is set, and we are not addressing the protected area. The presence of MTE signal permits operation of the memory timing generator. The MRTØ signal is generated at time TØ. The MRT signal is delayed approximately 120 nsec. The MST signal is generated at time T1 · TS ANDed with the divider output from flip flop $\overline{CF}$. The MST signal can be inhibited by the presence of certain signals such as addressing the A and B-Register, JSB, ISG, and so on. The function of jumper W2 in the MST circuit allows varying the time of MST for the 4 or 8 K modules. The additional capacity in the 8 K module requires that the MST signal be delayed. In the 4 K installation jumper W2 is removed allowing MST signal to occur 30 or 40 nsec earlier.

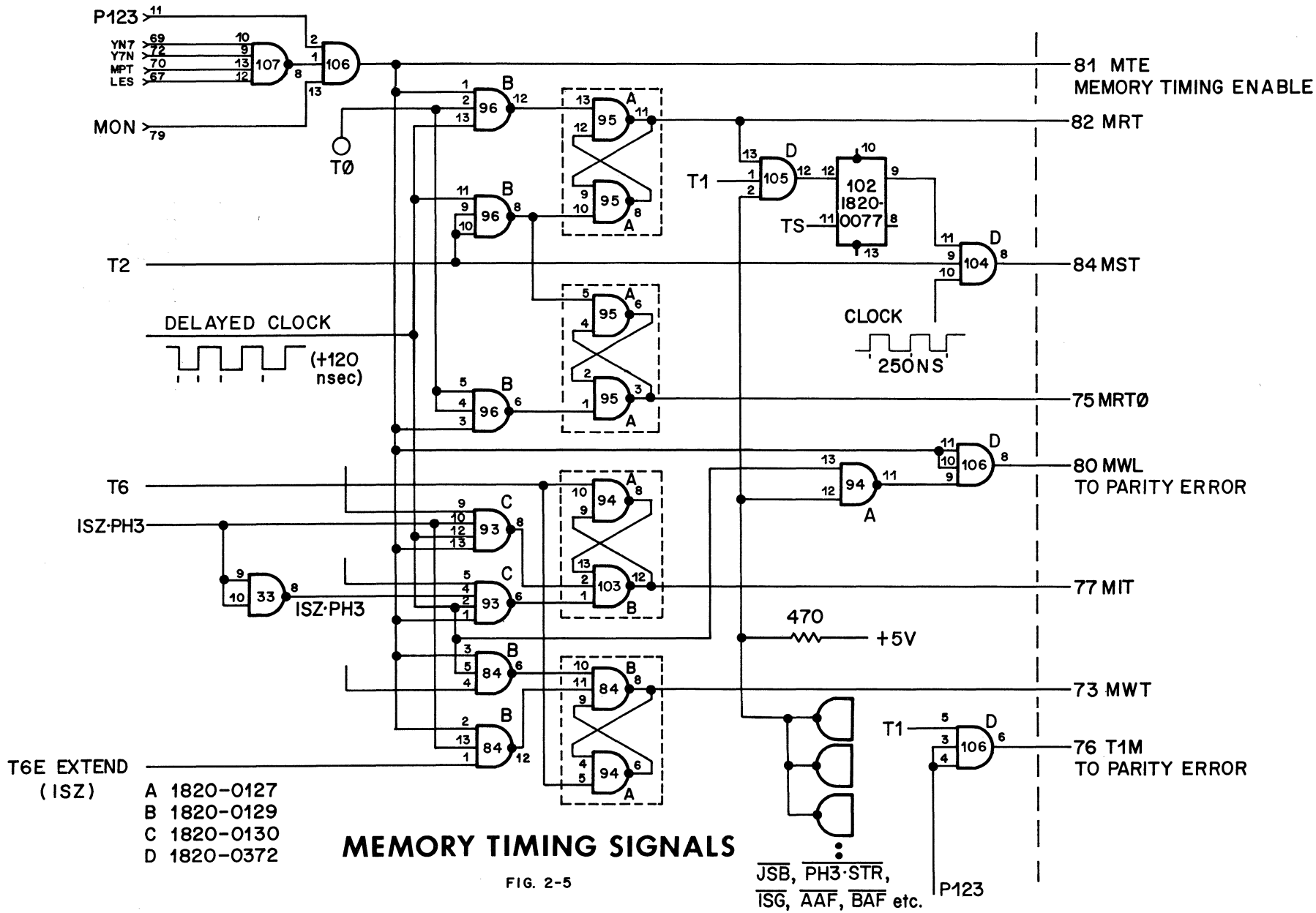
Inspection of the MIT, and MWT signals indicate inputs from the ISZ and PH3 signals. This permits delaying the MIT and MWT signals during the ISZ · PH3 operation.

## 2-19. RUN - STEP FF

Figure 2-6 indicates the logic for the RUN and STEP Flip Flops. The purpose of the STEP flip flop is to allow single cycle operation. It also allows the computer to operate once when the RUN button is pushed until a halt is encountered. If it were not for this feature when the RUN button were pushed, if the computer encountered a halt instruction it might restart before the RUN button could be released. The STEP flip flops provide logical control so that the RUN button must be released and then touched again to initiate another Computer Run cycle.

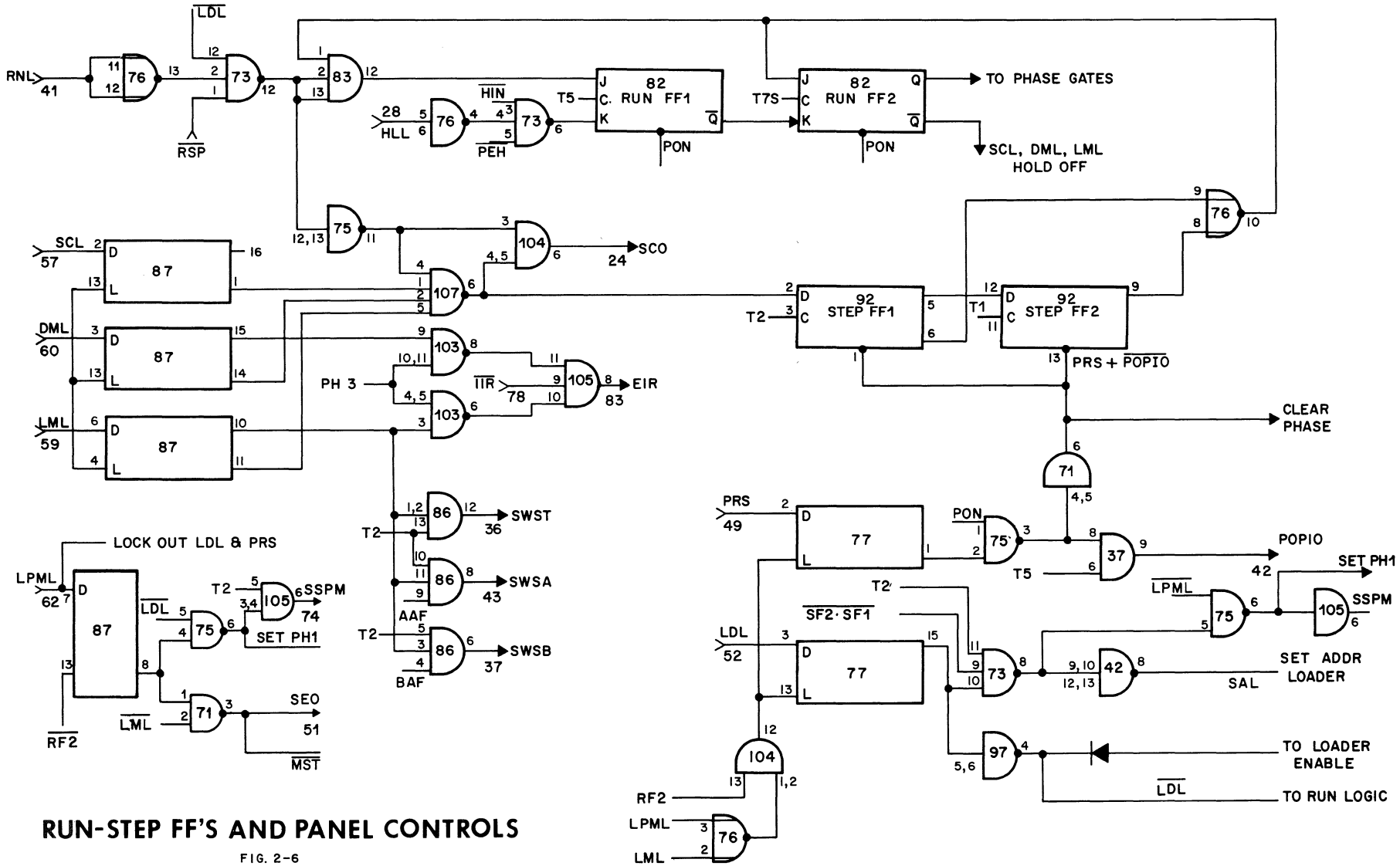
The operation of the STEP FF1 and FF2 is as follows. The D input to SF1 is normally low by virtue of pack MC107. When RUN is initiated by any one of the following: LOAD MEMORY, DISPLAY MEMORY, or SINGLE CYCLE, the D input to SF1 goes high. The next T2 the clear output of SF1 goes down. The Q output FF2 is still down therefore, a high J input is available on RUN FF2 but not on RUN FF1. At time T7S RUN flip flop two is set enabling phase gates for operation. At time T1 following, STEP FF2 is set which now removes the high input to RUN FF2. At time T7S RUN flip flop two is cleared and operation ceases. Removing finger from the front panel control enables STEP FF1 and FF2 to return to normal conditions.

The manner in which the computer begins to run is as follows. When the RUN button is pushed the STEP FF1 and FF2 operation is as described above. Now, however, a high J input to RUN FF1 is also present. Thus, at time T5 prior to enabling RUN FF2 the $\overline{Q}$ output of FF1 goes low. The J input to RUN FF2 goes high for one cycle as before, however, now as it goes low the K input is also low so that the state of RUN FF2 remains unchanged. The $\overline{RSP}$ pulse




**MEMORY TIMING SIGNALS**

FIG. 2-5




## RUN-STEP FF'S AND PANEL CONTROLS

FIG. 2-6

initiates STEP and RUN Flip Flop operation the same as RUN. The LOAD button for Automatic Load also operates the same way.

There are three ways to terminate computer operation. The status of RUN FF1 must be changed. This is accomplished by one of the three signals to the K input. They are $\overline{\text{PEH}}$, $\overline{\text{HIN}}$, and HLL.

## 2-20. PHASE OPERATION

Figure 2-7 shows the logic schematic for the phase circuits. The Phase operation follows a descending priority from phase 4 down to phase 1. A higher Phase request will inhibit any lower Phase request. The Phase 4 operation has the highest priority. It can be achieved under any computer conditions except a JSB or JMP simultaneous with an indirect IR15. Under any other circumstances Phase 4 can be requested.

Phase 3 can be requested by a DISPLAY MEMORY or LOAD MEMORY signal from the front panel, the completion of Phase 2 indirect, or the completion of Phase 1 which is not specifically a one phase only.

Phase 2 can be requested by a Phase 2 indirect instruction, or a Phase 1 indirect instruction.

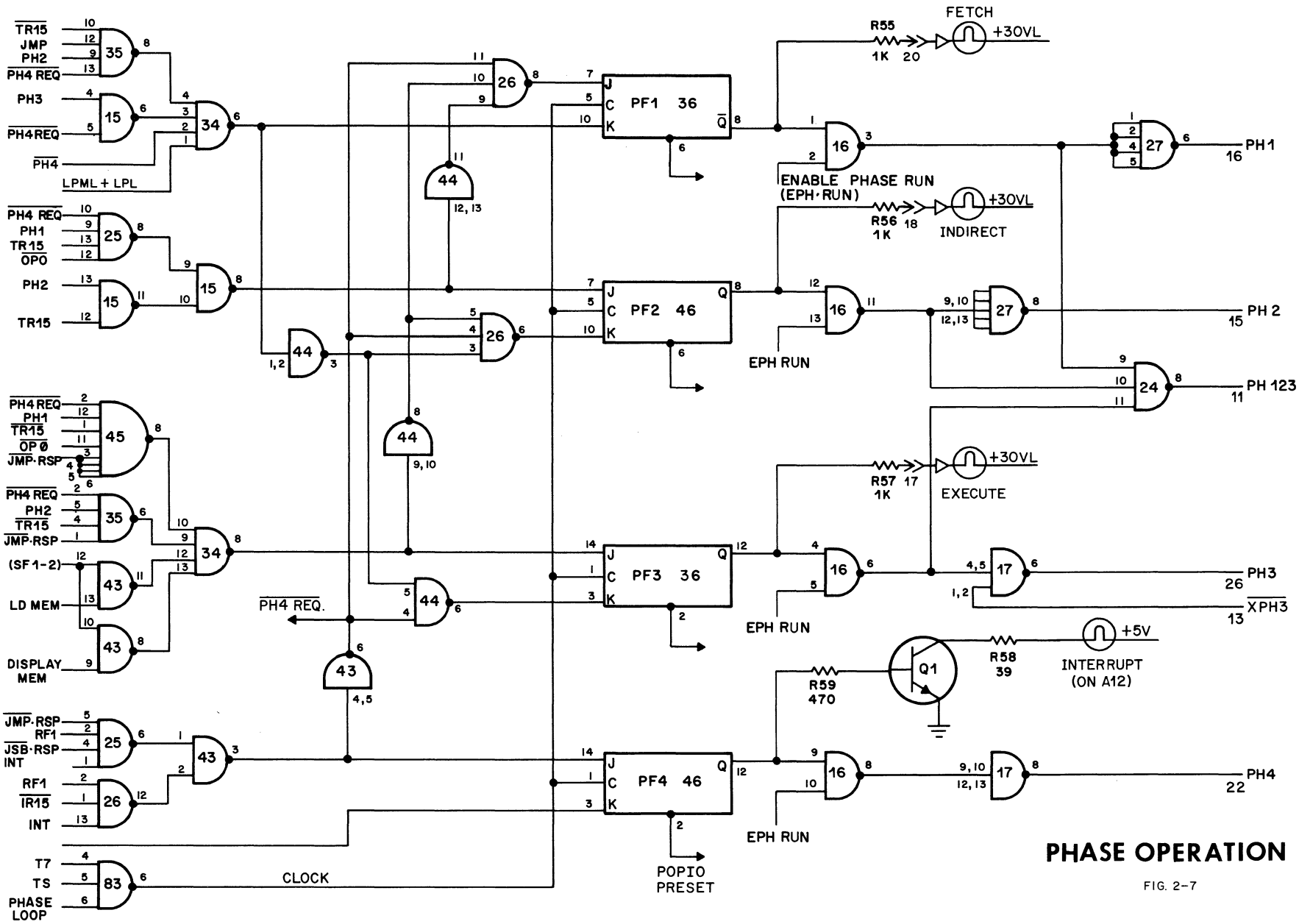
It will be noted that the phase requests are on the J inputs of flip flops for Phase 2, Phase 3, and Phase 4. The Phase 1 request is on the K input of Phase 1 flip flop.

Phase 1 operation is normally provided by the absence of a request for Phase 2, Phase 3, or Phase 4 operation. Specific requests for Phase 1 include the completion of a JMP Phase 2, a load LPML, or the completion of a Phase 3.

The outputs of the four Phase flip flops is NANDed with the ENABLE PHASE signal. It is then inverted to provide the Phase 1, Phase 2, Phase 3, and Phase 4 signals to the computer. The output of the Phase flip flops also drives the Phase 1, 2, and 3 indicators on the front panel. Phase 4 lamp is located on the Timing Generator assembly. Setting of the PHASE loop switch on the front panel prevents clocking the Phase flip flops, so phase cannot be changed.

Table 2-1. Set Phase Conditions

| PHASE | SET | PREVENT |
|---|---|---|
| PHASE 1 | 1) LOAD ADDRESS, Automatic LOAD<br>2) Following PH4<br>3) Following PH3 (no PH4 req)<br>4) Following JMP · PH2 if I not set (no PH4 req) | 1) PH2 req<br>2) PH3 req<br>3) PH4 req |
| PHASE 2 | 1) Following PH1, not OPO with I set (Bit 15)<br>2) Following PH2, I set | 1) PH1 req<br>2) PH3 req<br>3) PH4 req |
| PHASE 3 | 1) DISPLAY MEM (Step FF)<br>2) LOAD MEM (Step FF)<br>3) Following PH2, no I set, not JMP, and no PH4 req<br>4) Following PH1, I not set, not JMP, not single phase instruction, no PH4 req | 1) PH1 req<br>2) PH4 req |
| PHASE 4 | 1) INT req, computer running, no indirect<br>2) INT req, computer running, not JMP or JSB or RSP | 1) PH1 req |




# PHASE OPERATION

FIG. 2-7

## 2-21. INSTRUCTION DECODER

The Instruction Decoder assembly contains the Instruction Register bits 1Ø through 15. It contains encoding to generate the Memory Reference Instructions. These include JMP, IOA, CPA, JSB and so on. They also provide the SRG, IOG, ASG, and OPO signals. The rest of the logic on the Instruction Decoder Assembly includes the various store, read, and logical signals necessary for computer operation.

## 2-22. SHIFT LOGIC ASSEMBLY

The Shift Logic assembly contains numerous signals associated with shifting, rotating, I/O control, and the Overflow and Extend Flip Flops. In the upper left hand corner of the schematic diagram the various signals associated with shifting and rotating are generated.

In the upper middle of the schematic diagram the various signals associated with I/O control are present, such as, IOI, IOO, IOCO, CLC, STF, and so on. The right margin of the schematic diagram indicates the Overflow Register and Extend Register. The Overflow Register provides a numerical overflow from the A and B-Registers. It also provides a flag at select code Ø1. It can be interrogated to provide skip signals.

The logic for generating carry Ø is present in the lower margin of the schematic diagram. The addressable A and B flip flops are present in the lower left hand corner. Shifts and Rotates use $\overline{TBØ}$ and $\overline{TB15}$ for establishing conditions for bits 1 and 15. These circuits are on the left side of the schematic.

## 2-23. OVERFLOW REGISTER

The Overflow Register is a one bit register. It can be manipulated by various instructions in the I/O group. These include STF (S.C.Ø1), CLF (S.C.Ø1), SFC (S.C.Ø1), and SFS (S.C.Ø1). These instructions also have special op code (STO, CLO, SOC, SOS).

The Overflow register also is set by numerical overflow conditions when using the ADA, ADB, INA, and INB instructions. (Although overflow may result from the use of ISZ this will not set the Overflow bit.) The necessary conditions depend on the sign of the data. RB15 · SB15 · $\overline{TB15}$ is the condition experienced when adding large negative numbers. Bit 15 is set but bit 14 is zero for a large number. Thus no carry is generated by the bits 14 to give a TB15.

In large positive numbers bit 15 is zero but bit 14 is set. This provides a condition $\overline{RB15}$ · $\overline{SB15}$ · TR15 for large positive numerical overflow (ADA/B or INA/B).

In either case the Overflow bit should be cleared prior to the addition, and checked right afterwards.

Its status can also be determined by the front panel lamp. The lamp is on when the register is set.

## 2-24. EXTEND REGISTER

The Extend Register is a one bit register. It is used to detect a carry C16 from the ADA, ADB, INA, INB instruction. This would normally be encountered whenever adding two negative numbers (of any magnitude). The addition of a large positive number and a small negative number would also result in setting the Extend bit.

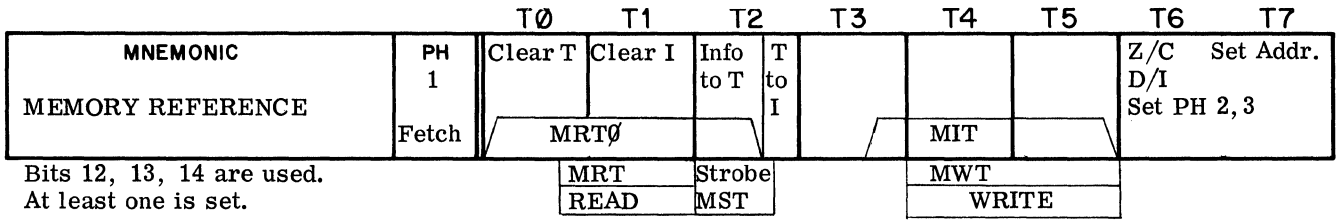
The Extend Register is very useful as an aid in linking the A and B-Registers while using multi-precision arithmetic. The EL A/B will clear or set the extend bit depending on the status of bit RB15. The ER A/B will clear or set depending on RBØ. Both instructions can be enabled in both time periods. This results in a rather complex logic circuit to permit all combinations.

The Direct instructions include CLE (Shift-Rotate, or Alterskip), CME, and CCE.

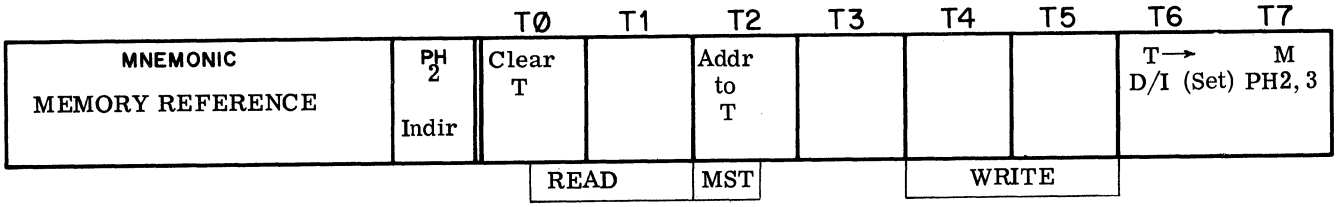
The status interrogation includes SEZ and SEZ RSS.

Table 2-2. Machine Instruction Timing and Signals

MEMORY REFERENCE INSTRUCTIONS



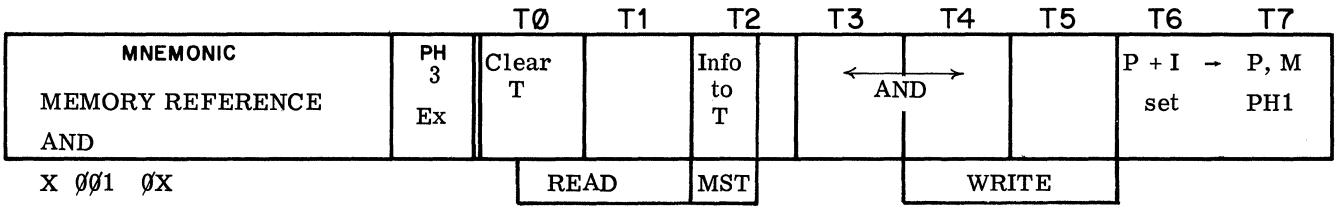

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T0 | A13-26 | P123 · T0 · TS → | STBT | Clear T Reg. |
| T1 | A13 | PH1 · T1 → | - | Clear I Reg. |
| T2 | A12-84 | MST | MST | Info to T Reg. |
| | A13 | PH1 · T2 · TS | - | TR 10-15 → I Reg. |
| T67 | A13-27 | PH1 · EIR · $\overline{\text{OPO}}$ · T67 → | RTSB | For Address Strobe to M |
| | A13-25 | P123 · T67 → | ADF | For ADDR to T bus |
| | A13-58 | PH1 · EIR · $\overline{\text{OPO}}$ · T7S → | STM 0-5 | Strobe in Address |
| | A13-63 | PH1 · EIR · $\overline{\text{OPO}}$ · T7S → | STM 6-9 | Strobe in Address |
| | A13-35 | PH1 · IR10 · $\overline{\text{OPO}}$ · T7S → | RSM 10-15 | Clear M Reg. 10-15 force zero page (Z) |
| | | | | Remain in current page (C) |
| | A12-26 | $\overline{\text{PH4 req.}}$ · PH1 · $\overline{\text{TR15}}$ · $\overline{\text{OPO}}$ · $\overline{\text{JMP}}$ · T7 · TS → | PH3 | Direct address (D) |
| | A12-15 | $\overline{\text{PH4 req.}}$ · PH1 · TR15 · $\overline{\text{OPO}}$ → | PH2 | Indirect address (I) |



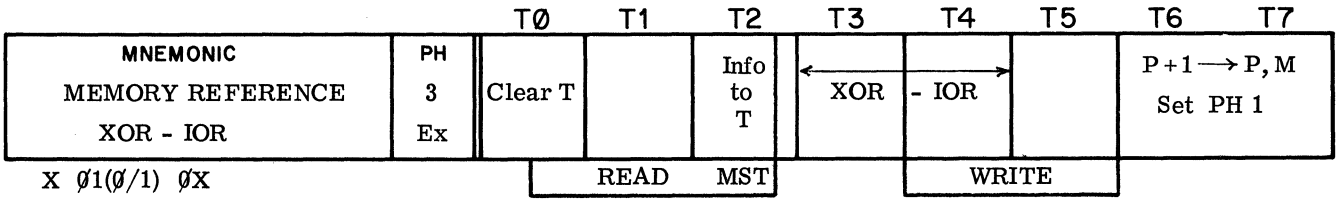

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T67 | A13-27 | PH2 · T67 · EIR → | RTSB | New address |
| | A13-25 | PH123 · T67 → | ADF | |
| | A13-58 | PH2 · T7S → | STM 0-5 | |
| | A13-63 | PH2 · T7S → | STM 6-9 | |
| | A13-66 | PH2 · T7S → | STM 10-15 | |
| | A12-15 | PH2 · TR15 · T7 · TS → (If no PH4 req.) | PH2 | Indirect (I) |
| | A12-26 | PH2 · $\overline{\text{TR15}}$ · T7 · TS → (If no PH4 req.) | PH3 | Direct (D) |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

MEMORY REFERENCE INSTRUCTIONS (cont'd.)




| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| TØ | A13-26 | P123 · TØ · TS → | STBT | Clear T Reg. |
| | | $\overline{IR11}$ · IR12 · $\overline{IR13}$ · $\overline{IR14}$ → | ANA | AND Encoded |
| T34 | A13-72 | PH3 · T34 · $\overline{IR11}$ · $\overline{IR14}$ → | RARB | (MC32) |
| | A13-27 | PH3 · T34 · EIR · $\overline{JSB}$ → | RTSB | (MC55) |
| | A13-23 | ANA · PH3 · T34 → | ANF | (MC25) |
| | A13-73 | PH3 · T5 · IR12 · $\overline{CPA}$ · AAF · TS → (MC25) | STBA | (MC1Ø4) |
| T67 | A13-65 | PH3 · T67 → | RPRB | |
| | A13-19 | PH3 · T67 → | SBØ | |
| | A13-25 | P123 · T67 → | ADF | |
| | | PH3 · T7S → | STP, M (ALL) | |




| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T34 | A13-71, 72 | PH3 · T34 · $\overline{IR14}$ · $\{\overline{IR11}, IR11\}$ → | R A/B RB | (MC32) |
| | A13-27 | PH3 · T34 · EIR · $\overline{JSB}$ → | RTSB | (MC55) |
| | A13-24 | PH3 · T34 · EIR · $\overline{XOA}$ → | EOF | (MC15) XOR |
| | A13-21 | PH3 · T34 · IOA → | IOF | (MC13) IOR |
| | A13-73, 74 | PH3 · T5 · IR12 · $\overline{CPA}$ · TS · $\{AAF, BAF\}$ → MC25 | STB A/B | (MC1Ø4, 94) |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)
MEMORY REFERENCE INSTRUCTIONS (cont'd.)

| MNEMONIC | PH | TØ | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MEMORY REFERENCE | 3 | Clear T | P+1 → T | | M → P | | | P+1 → P, M | |
| JSB | Ex | | | | | | | Set PH 1 | |
| | | | | | | | | *** | |
| X 001 IX | | | | * | | WRITE | ** | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T12 | A13-65 | PH3 · T12 · JSB → | RPRB | (MC21) |
| | A13-19 | PH3 · T12 · JSB → | SBØ | (MC32) |
| | A13-25 | PH3 · T12 · JSB → | ADF | (MC53) |
| | A13-26 | PH3 · T2 · TS · JSB → | STBT | (MC47) |
| T3 | A13-62 | PH3 · T34 · JSB → | RMSB | (MC45) |
| | A13-24 | PH3 · T34 · EIR · JSB → | EOF | (MC15) |
| | A13-67, 68 | PH3 · T4 · TS · JSB → | STPØ-9, 1Ø-15 | (MC86) |
| *T2 | A12-84 | PH3 · JSB → | $\overline{\text{MST}}$ | Inhibit Memory |

** T34 WRITE contents of M-Register is core ADDR for WRITE Cycle. T-Register contains the current program location plus 1 - This provides Inhibit Driver info to write the return address.

*** T67 P contains starting address for subroutine (NOP).

| MNEMONIC | PH | TØ | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MEMORY REFERENCE | 3 | Clear T | | Data to T | AD | | | P+1 → P, M | |
| AD A/B | Ex | | | | | | | Set PH 1 | |
| X 100 A/B X | | | READ | MST | | WRITE | | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T34 | A13-71, 72 | PH3 · T34 · ADD · $\{\overline{\text{IR11}}, \text{IR11}\}$ → | R(A/B)RB | (MC44) |
| | A13-27 | PH3 · T34 · EIR · $\overline{\text{JSB}}$ → | RTSB | |
| | A13-25 | PH3 · T34 · ADD → | ADF | |
| | A13-73, 74 | PH3 · T4 · ADD · TS · $\{\overline{\text{IR11}}, \text{IR11}\}$ → | STB (A/B) | (MC1Ø6) |
| | A14-62 | PH3 · T4 · ADD · C16 · TS → | E | numerical carry |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

MEMORY REFERENCE INSTRUCTIONS (cont'd.)

| T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|
| MNEMONIC<br>MEMORY REFERENCE<br>CP A/B | PH<br>3<br>Ex | Clear T | | Data to T | ← CP | A/B → | | P+1+C0→P,M<br>Set PH 1 |
| Compare, SKIP if UNEQUAL<br>X 101 A/B X | | | READ | MST | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T34 | A13-72 | $PH3 \cdot T34 \cdot CPA \cdot \{\overline{IR11}, IR11\} \rightarrow$ | R(A/B)RB | (MC94) |
| | A13-27 | $PH3 \cdot EIR \cdot T34 \cdot \overline{JSB} \rightarrow$ | RTSB | |
| | A13-24 | $PH3 \cdot T34 \cdot EIR \cdot CPA \rightarrow$ | EOF | (MC15) |
| | A14-57 | $PH3 \cdot T4 \cdot CPA \cdot \overbrace{SOR \cdot TS}^{TAN\ 1,2,3,4} \rightarrow$ | CØ | used at T67 |
| T67 | A13-65 | $PH3 \cdot T67 \rightarrow$ | RPRB | |
| | A13-19 | $PH3 \cdot T67 \rightarrow$ | SBØ | |
| | A13-25 | $P123 \cdot T67 \rightarrow$ | ADF | SBØ plus CØ |
| | A13-58, 63, 66, 67, 68 | $P3 \cdot T7S \rightarrow$ | STM, P (all) | |

| T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|
| MNEMONIC<br>MEMORY REFERENCE<br>LD A/B | PH<br>3<br>Ex | Clear T | | Data to T | ← LOAD | → | | P+1→P,M<br>Set PH 1 |
| X 110 A/B X | | | READ | MST | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| | A13 | $\overline{IR12} \cdot IR13 \cdot IR14 \cdot EIR \rightarrow$ | $\overline{LOD}$ | (MC81) |
| T34 | A13-27 | $PH3 \cdot T34 \cdot EIR \cdot \overline{JSB} \rightarrow$ | RTSB | (MC55) |
| | A13-24 | $PH3 \cdot T34 \cdot EIR \cdot \overline{LOD} \rightarrow$ | EOF | |
| T4 | A13-73, 74 | $PH3 \cdot T4 \cdot LOD \cdot TS \cdot \{\overline{IR11}, IR11\} \rightarrow$ | STB A/B | |

| T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|
| MNEMONIC<br>MEMORY REFERENCE<br>ST A/B | PH | Clear T | A/B to T REG | | | T to Driver | Inhibit | P+1→P,M<br>Set PH 1 |
| X 111 A/B X | | | READ | | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| | A13-64 | $IR12 \cdot IR13 \cdot IR14 \cdot EIR \rightarrow$ | STR | Store Encoded |
| T1 | A13-72 | $P123 \cdot T1 \cdot \{AAF, BAF\} \rightarrow$ | R(A/B)RB | |
| | A13-24 | $P123 \cdot T1 \rightarrow$ | EOF | |
| | A13-26 | $P123 \cdot T1 \cdot TS \cdot \{AAF, BAF\} \rightarrow$ | STBT | |
| T2 | A12-84 | $PH3 \cdot STR \rightarrow$ | $\overline{MST}$ | ref MC85 pin 10<br>Inhibits Memory |
| T45 | | $\overline{TREG}$ | IDØ-16 | Controls writing info<br>To Inhibit Drivers |

Table 2-2. Machine Instruction Timing and Signald (cont'd.)

MEMORY REFERENCE INSTRUCTIONS (cont'd.)

| MNEMONIC MEMORY REFERENCE JMP | PH 1 Fetch | T0 Clear T | T1 Clear I | T2 TR1Ø-15 to I | T3 | T4 | T5 | T6 T7 Z Ø→ M 1Ø-15 D T→ P,M (Ø-9) Set PH 1 I T→M (Set PH2 |
|---|---|---|---|---|---|---|---|---|
| D/I 010 1 Z/C | | | READ | MST | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T67 | A13-27 | PH1 · T67 · $\overline{OPO}$ · EIR → | RTSB | |
| | A13-25 | P123 · T67 → | ADF | |
| | A13-63,66 | PH1 · T7S · OPO · $\overline{EIR}$ → | STM Ø-5,6-9 | Current Page (C) |
| | A13-69 | PH1 · T7S · JMP · $\overline{IR15}$ → (Set PH1 by no — PH2,3,4 req) | STP Ø-9 | Direct Addr (D) |
| | A13-58,63 | PH1 · T7S · $\overline{OPO}$ · EIR → | STM Ø-5,6-9 | Current Page (C) |
| | A12-15 | PH1 · IR15 · $\overline{OPO}$ · $\overline{PH4\ REQ}$ → | SET PH 2 | Indirect Address (I) |
| | A13-35 | PH1 · T7S · $\overline{OPO}$ · $\overline{IR1Ø}$ → | RSM 1Ø-15 | Zero Page (Z) |

| MNEMONIC MEMORY REFERENCE JMP | PH 2 Ind | T0 Clear T | T1 | T2 Addr to T | T3 | T4 | T5 | T6 T7 D TR→ P,M SET PH 1 I TR→ M SET PH 2 |
|---|---|---|---|---|---|---|---|---|
| | | | READ | MST | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T67 | A13-27 | PH2 · T67 · E1R → | RTSB | |
| | A13-25 | P123 · T67 → | ADF | |
| | A13-58,63,66 | PH2 · T7S → | STP Ø-9, 1Ø-15 | |
| | A13-67,68 | PH2 · $\overline{TR15}$ · T7S · JMP → | STP Ø-9, 1Ø-15 | Direct Addr (D) |
| | A12-16 | PH2 · $\overline{TR15}$ · JMP · $\overline{PH4\ req}$ → | SET PH1 | |
| | A12-15 | PH2 · IR15 → | SET PH2 | Indirect Addr (I) |

| MEMORY REFERENCE ISZ | PH 3 Ex | T0 Clear T | T1 | T2 Data to T | T3 TR+1 | T4 T | T5 | Cycle Stretch F6E F7E | T6 T7 P+1+C0 → P,M Set PH 1 |
|---|---|---|---|---|---|---|---|---|---|
| X Ø11 1 X | | | READ | MST | | | WRITE | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| | | IR11 · IR12 · IR13 · $\overline{IR14}$ · E1R → | ISZ | |
| T34 | A13-27 | PH3 · T34 · E1R · $\overline{JSB}$ → | RTSB | |
| | A13-20 | ISZ · PH3 · T34 → | RBØ | |
| | A13-25 | $\overline{ISZ}$ · PH3 · T34 → | ADF | |
| | A13-26 | PH3 · ISZ · T4 · TS → | STBT | |
| | A14-57 | PH3 · ISZ · T4 · C16 → | CØ | used at T67 |
| T34 (Mem Inhibit) | | $\overline{PH3 \cdot ISZ}$ → | | (prevents MIT@ T3+120μsec MWT@T4) |
| T5 | | PH3 · ISZ → T5 to F6E to F7E to T6 | | (MC33 pin 11) (Extra 500μsec) |
| T5 (F6E & F7E) | | PH3 · ISZ · MTE · T5 · 120μsec delay → MIT<br>PH3 · ISZ · MTE · F6E → MWT | | (MC98 pin 8)<br>(MC84 pin 12) |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

SHIFT ROTATE INSTRUCTIONS

| | | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC<br>SHIFT-ROTATE<br>ALTER SKIP | PH<br>1<br>Fetch | Clear T Reg<br>STBT | Clear I Reg | T Reg→ I Reg | | T Reg to Inhibit Driver | | P+1+C0→P, M<br>Set PH 1 | |
| | | READ | | Strobe MST | | WRITE | | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| TØ | A13-26 | P123 · TØ · TS → | STBT | Clear T-Register |
| T1 | A13 | PH1 · T1 | | Clear I-Register |
| T2 | A13 | PH1 · T2 · TS | | TR 1Ø-15 → I-Register |
| T67 | A13-65 | OPO · T67 → | RPRB | |
| | A13-25 | P123 · T67 → | ADF | Includes SBØ and CØ |
| | A13-63, 65, 66, 67, 68 | OPO · T7S → | STM, P | |

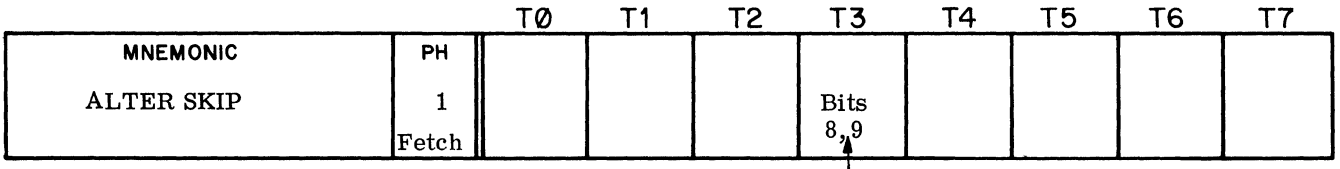
NOP SHIFT-ROTATE WITH NOTHING ENABLED. (i.e., Bits 9, 5, 4, 3 all zero)

| | | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC<br>ALL SHIFT-ROTATE | PH<br>1<br>Fetch | | | | Bits 6-9 | Bits 3, 5 | Bits 0-2, 4 | | |

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| T3 | A13-71, 72 | $\overline{SRG}$ · T3 → | R(A/B)RB | |
| | A14-80 | SRG · TR6, 7, 8 · T3 → | RL4 | *LF |
| | A14-78 | SRG · TR6 · T3 → | SRM | *RS, R*R, ER*, *LF |
| | A14-75 | SRG · $\overline{TR6}$ · T3 → | SLM | *LS, R*L, *LR, EL* |
| | A14-72 | SRG · T3 · TR6 · TR7 · $\overline{TR8}$ → | LRS | R*R |
| | A14-69 | SRG · T3 · $\overline{TR6}$ · TR7 · $\overline{TR8}$ → | SLØ | R*L |
| | A14-71 | SRG · T3 · $\overline{TR6}$ · TR7 → | SL14 | R*L, EL* |
| | A14-82 | SRG · E · T3 · $\overline{TR6}$ · TR7 · TR8 → | $\overline{TBØ}$ | EL* |
| | A14-24 | SRG · E · T3 · TR6 · $\overline{TR7}$ · TR8 → | $\overline{TB15}$ | ER*, *LR |
| | A13-73, 74 | SRG · T3 · TS · TR9 · $\{\overline{TR11}, TR11\}$ → | STB(A/B) | |
| T4 | A14 | SRG · T4 · TR5 | | Clear Extend CLE |
| | A13-73 | SRG · T45 · $\{\overline{IR11}, IR11\}$ → | R(A/B)RB | SL(A/B) |
| | A14-57 | SRG · $\overline{RBØ}$ · TR3 · T4 → | CØ | Skip condition |
| T5 | Refer T3 above<br>T3 → T5; TR8 → TR2; TR7 → TR1; TR6 → TRØ | | | |

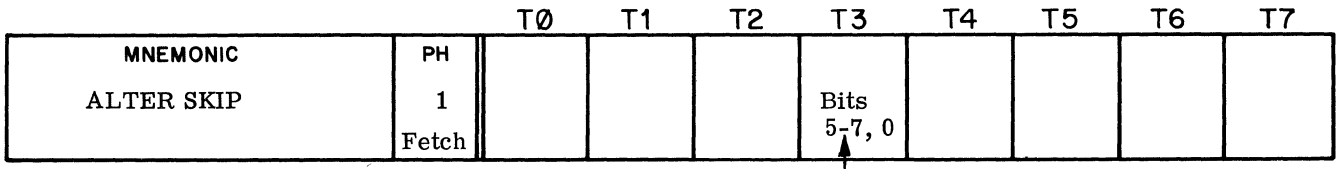
Table 2-2. Machine Instruction Timing and Signals (cont'd)

SHIFT ROTATE INSTRUCTIONS (cont'd.)




CLEAR & COMPLEMENT INSTRUCTIONS

| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| | | S BUS, R BUS are Ø | | |
| CL A/B | A13-24 | ASG · T3 · $\overline{TR9}$ → | EOF | |
| CM A/B | A13-73, 74 | ASG · (TR11) · T3 · TS → | STB(A/B) | |
| CM A/B | A13-71, 72 | ASG · $\overline{TR8}$ · T3 → | R A/B RB | |
| | A13-22 | ASG · TR9 · T3 → | CMF | |
| | A13-73, 74 | ASG · (TR11) · T3 · TS → | STB(A/B) | |
| | | S BUS AND R BUS ARE Ø | | |
| CC A/B | A13-22 | ASG · TR9 · T3 → | CMF | |
| | A13-73, 74 | ASG · (TR11) · T3 · TS | STB (A/B) | |

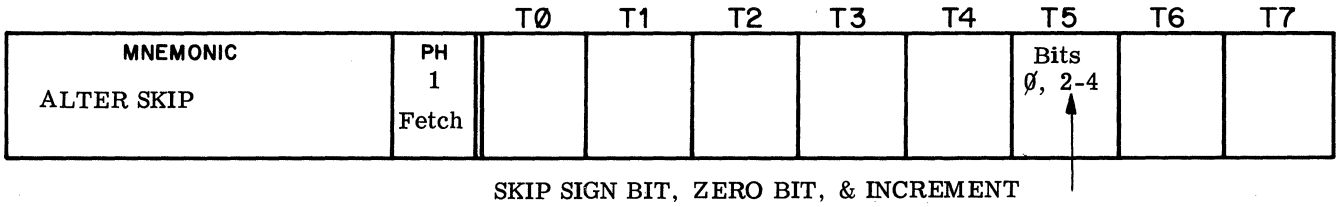



EXTEND REGISTER INSTRUCTIONS

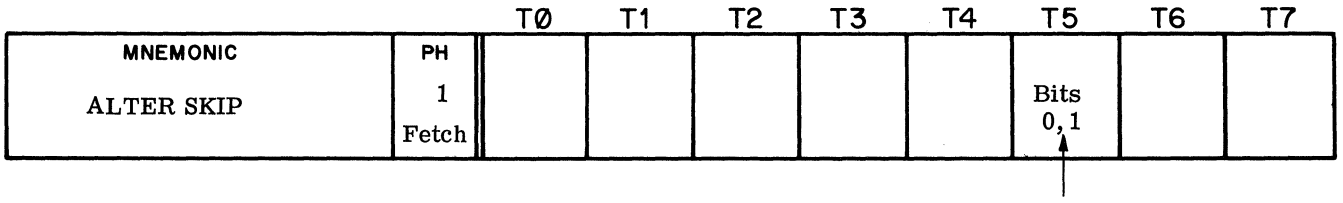
| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| CLE | | ASG · TR6 · $\overline{TR7}$ · T3 → | K INPUT | (MC61 Pin 6) Clock at TS |
| CME | | ASG · $\overline{TR6}$ · TR7 · T3 → | K INPUT | (MC42 Pin 8) |
| | | ASG · TR7 · T3 → | J INPUT | (MC103 Pin 6) |
| CCE | | ASG · TR7 · T3 → | J INPUT | (MC103 Pin 6) |
| SEZ | A14-57 | ASG · TR5 · T3 · $\overline{E}$ · $\overline{TRØ}$ → | CØ | at T67 |
| | | ASG · TR5 · T3 · E · TRØ → | CØ | at T67 |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

SHIFT ROTATE INSTRUCTIONS (cont'd.)



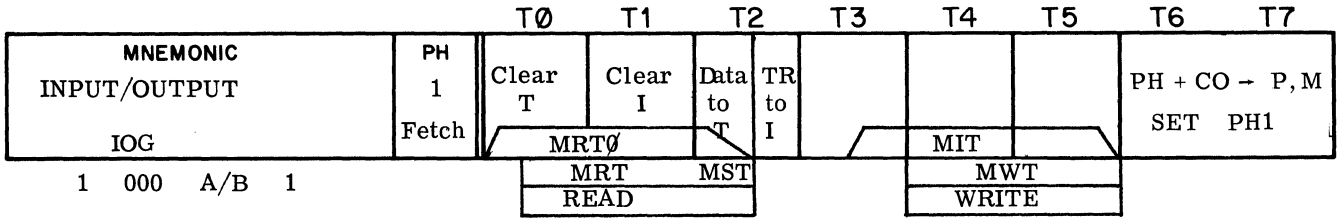

| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| SS A/B | A13-72 | ASG · T45 · $\{\overline{IR11}, IR11\}$ → | R(A/B)RB | |
| | | ASG · T4 · TR4 · $\overline{RB15}$ · $\overline{TRØ}$ → | CØ | MC56 Pin 10 |
| | | ASG · T4 · TR4 · RB15 · TRØ · $\overline{TR3}$ → | CØ | MC15 Pin 11, 12 |
| | | ASG · T4 · TR4 · RB15 · TRØ · TR3 · RBØ → | CØ | MC63 Pin 8 |
| | | (SL*) | | |
| SL A/B | A13-71, 72 | ASG · T45 · $\{\overline{IR11}, IR11\}$ → | R(A/B)RB | |
| | | ASG · T4 · TR3 · $\overline{RBØ}$ · $\overline{TRØ}$ → | CØ | MC75 Pin 9, 10 |
| | | ASG · T4 · TR3 · RBØ · TRØ · $\overline{TR4}$ → | CØ | MC64 Pin 9, 10 |
| | | ASG · T4 · TR3 · RBØ · TRØ · TR4 · RB15 → | CØ | MC63 Pin 8 |
| | | (SS*) | | |
| IN A/B (T4 & T5) | A13-71, 72 | ASG · T45 · $\{\overline{IR11}, IR11\}$ → | R(A/B)RB | |
| | A13-19 | ASG · TR2 · T45 → | SBØ | MC23 |
| | A13-25 | ASG · T45 → | ADF | MC54 |
| | | ASG · TR2 · T5 · $\{\overline{IR11}, IR11\}$ · TS → | STB(A/B) | MC93 Pin 6 |
| | | ASG · TR2 · C16 · T5 · TS → | EXTEND | MC21 Pin 6 |



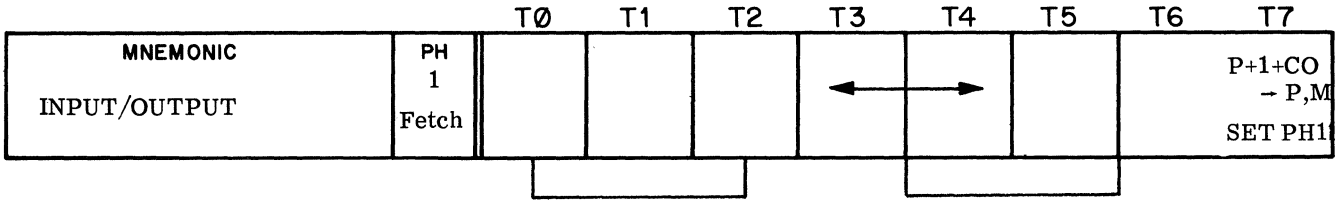

| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| SZ A/B | A13-72 | ASG · T45 · $\{\overline{IR11}, IR11\}$ → | R(A/B)RB | |
| | A13-25 | ASG · T45 → | ADF | |
| | | ASG · T5 · TR1 · $\overline{TRØ}$ · $\overline{SOR}$ → | CØ | MC63 |
| | | ASG · T5 · TR1 · TRØ · SOR → | CØ | MC64 Pin 11, 12 |
| | | TAN 1, 2, 3, 4 | | |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

INPUT/OUTPUT INSTRUCTIONS



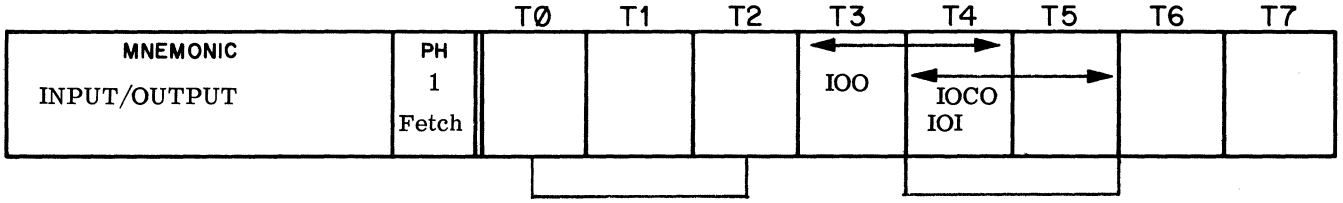

| TIME | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| | A13-53 | $\overline{TR12} \cdot \overline{TR13} \cdot \overline{TR14} \cdot PH1 \rightarrow$ | OPO | |
| | A13-52 | $OPO \cdot IR10 \cdot IR15 \rightarrow$ | IOG | |
| T0 | A13-26 | $P123 \cdot T0 \cdot TS \rightarrow$ | STBT | Clear T-Register |
| T1 | A13 | $PH1 \cdot T1 \rightarrow$ | - | Clear I-Register |
| T2 | A13 | $PH1 \cdot T2 \cdot TS \rightarrow$ | - | TR10-15 to I-Register |
| T67 | A13-65 | $OPO \cdot T67 \rightarrow$ | RPRB | |
| | A13-25 | $P123 \cdot T67 \rightarrow$ | ADF | SB0 plus C0 |
| | A13-58, 63, 66 | $OPO \cdot T7S \rightarrow$ | STM (all) | |
| | A13-67, 68 | $OPO \cdot T7S \rightarrow$ | STP (all) | |



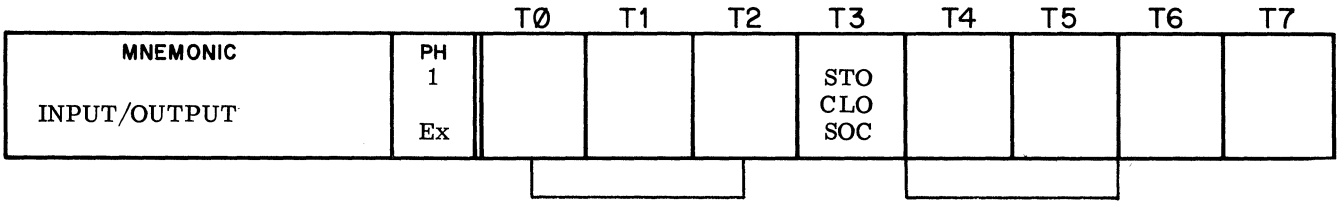

| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| STF<br>$TR6 \cdot \overline{TR7} \cdot \overline{TR8} \cdot T3$ | | STF sets Flag FF@ S.C. | | |
| | | STF → Clear Interrupt Control | | |
| | | T REG info present for select code<br>STF (SC00) sets IEN | | |
| CLF<br>$TR9 \cdot T4$ | | CLF → Reset Flag FF@ S.C. | | |
| | | CLF → Clear Int. Control | | |
| | | T REG info present for Select Code | | |
| SFC<br>$\overline{TR6} \cdot TR7 \cdot \overline{TR8}$ | | $SFC \cdot (SC\ 01) \cdot IOG \cdot \overline{OVF} \cdot T4 \rightarrow$ | C0 | |
| | | $SFC \cdot (\overline{INT\ ENABLE\ FF}) \cdot (SC\ 00) \rightarrow$ | SKF | |
| | | $SKF \cdot T4 \rightarrow$ | C0 | MC61 Pin 9 |
| | | $SFC \cdot SCM \cdot SCL \cdot IOG \rightarrow$ | SKF | (on INTERFACE) |
| SFS<br>$TR6 \cdot TR7 \cdot \overline{TR8}$ | | $SFC \cdot SCM \cdot SCL \cdot IOG \rightarrow$ | SKF | |
| | | $SKF \cdot T4 \rightarrow$ | C0 | |
| | | $SKS \cdot (SC01) \cdot IOG \cdot OVF \cdot T4 \rightarrow$ | C0 | |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

INPUT/OUTPUT INSTRUCTIONS (cont'd.)




| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| MI A/B | A13-71,72 | IOG · $\overline{TR6}$ → | RARB | |
| | A13-52 | IOG · $\overline{TR7}$ · TR8 · T45 → | IOI | |
| | | IOI · IOG · (SC) → | Data to IOB (BUS) | ON INTERFACE |
| | | IOI STROBES IOB | SBUS | |
| | A13-21 | IOG · T45 → | IOF | |
| | A13-73,74 | IOG · $\overline{TR7}$ · TR8 · T5 · TS $\{\overline{IR11}, IR11\}$ → | STB(A/B) | |
| | | TR9 · T4 → | CLF | |
| LA A/B | A13-52 | IOG · $\overline{TR7}$ · TR8 · T45 → | IOI | |
| | | IOI · IOG · (SC) → | Data to IOB (BUS) | INTERFACE |
| | | IOI STROBES IOB → | SBUS | |
| | A13-21 | IOG · T45 → | IOF | |
| | A13-73,74 | IOG · TR7 · TR8 · T5 · TS $\{\overline{IR11}, IR11\}$ → | STB(A/B) | |
| | | TR9 · T4 → | CLF | |
| OT(A/B) | A13-71,72 | IOG · $\overline{TR6}$ $\{\overline{IR11}, IR11\}$ → | RARB | |
| | A14-19 | $\overline{TR6}$ · TR7 · TR8 · T45 → | IOCO | |
| | | IOCO STROBES $\overline{R\ BUS}$ TO IOB (BUS) | | |
| | A14-13 | $\overline{TR6}$ · TR7 · TR8 · T34 · IOO | | |
| | | IOO · (SC) · STROBES IOB INTO BUFFER | | INTERFACE |
| | A14-17 | TR9 · T4 → | CLF | |




| INSTRUCTION | SOURCE | EQUATION | MNEMONIC | PURPOSE |
|---|---|---|---|---|
| STC | A14-25 | TR6 · TR7 · TR8 · $\overline{TR11}$ · T4 → | STC | |
| | | STC · (SC) → | SETS FF | |
| CLC | A14-23 | TR6 · TR7 · TR8 · TR11 · T4 → | CLC | |
| | | CLC · (SC) → | CLEARS FF | |
| STO | A14-15 | TR6 · $\overline{TR7}$ · $\overline{TR8}$ · T3 → | STF | |
| | | STF · (SCØ1) · IOG · TS → | Set OVF | |
| CLO | A14-17 | TR9 · T4 → | CLF | |
| | | CLF · IOG · (SCØ1) → | Clear OVF | |
| SOC | A14-21 | $\overline{TR6}$ · TR7 · $\overline{TR8}$ → | SFC | |
| | | SFC · (SCØ1) · IOG · T4 · $\overline{OVF}$ → | CØ at T67 | |
| | A14-17 | C - TR9 · T4 → | CLF | |
| SOS | A14-27 | TR6 · TR7 · $\overline{TR8}$ → | SFS | |
| | | SFS · OVF · IOG · (SCØ1) · T4 → | CØ at T67 | |
| | A14-17 | C - TR9 · T4 → | CLF | |

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

INPUT/OUTPUT INSTRUCTIONS (cont'd.)

| | | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC<br>INPUT/OUTPUT<br>HLT | PH<br>1<br>Fetch | Clear T | | MST | Info to I | | Reset RF1 | P→ | P, M Reset RF2 |
| | | | READ | | | WRITE | | | |

| SOURCE | EQUATION | MNEMONIC |
|---|---|---|
| A14-64 | IOG · $\overline{TR6}$ · $\overline{TR7}$ · $\overline{TR8}$ → | $\overline{HIN}$ |
| | HIN · T5 → | RESET RF1 |
| A13-65 | OPØ · T67 → | RPRB |
| A13-25 | P123 · T67 → | ADF |
| A13-58, 63, 66 | OPØ · T7S → | STM Ø-5, 6-9, 1Ø-15 |
| A13-67, 68 | OPØ · T7S → | STP Ø-9, 1Ø-15 |
| | $\overline{RF1}$ · T7S → | RESET RF2 |

PHASE 4

| | | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC<br>INTERRUPT * | PH<br>4 | | CM P → | P | INC P → | P | CMP → P | | CLM6$_{I5}$<br>STMØ-5<br>SET PH1 |

| TIME | EQUATION | MNEMONIC |
|---|---|---|
| T12 | PH4 · T12 → | RPRB |
| | PH4 · T12 → | CMF |
| | PH4 · T2 · TS → | STP Ø-9, 1Ø-15 |
| T34 | PH4 · T34 → | RPRB |
| | PH4 · T34 → | $\overline{SBØ}$ |
| | PH4 · T34 → | ADF |
| | PH4 · T45 · TS | STP Ø-9, 1Ø-15 |
| | PH4 · T3IO → | Clears Interrupt Control FF |
| T5 | PH4 · T5 → | RPRB |
| | PH4 · T5 → | CMF |
| | PH4 · T45 · TS | STP Ø-9, 1Ø-15 |
| T7 | PH4 · T7 → | $\overline{RSM}$ $\overline{6-9, 1Ø-15}$ |
| | $\overline{RSM}$ $\overline{6-9}$ → | Select Code to Central Int. Reg |
| | $\overline{RSM\ 6-9}$ → | Central Interrupt Reg → T Bus |
| | PH4 · T7S → | STM Ø-5 |
| | PH4 → | PH1 |

* Refer to Figure 4-1.

Table 2-2. Machine Instruction Timing and Signals (cont'd.)

PHASE 4 (cont'd.)

| MNEMONIC | PH | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| 1st machine cycle following interrupt PHASE 4 | 1 Fetch | | 1AK Clear Flag Buffer | Clear IRQ FF | | | | STM 6-9 Set Interrupt Inhibit FF | |

PERFORMS INSTRUCTION IN TRAP CELL.
This trap cell instruction is usually a JSB which stores the P-Register contents to allow a return to the Program in Process.

| TIME | EQUATION | MNEMONIC |
|---|---|---|
| T1 | PH1 · T1 $\overline{\text{INTERRUPT CONTROL}}$ → | IAK |
| | IAK · 1RQ FF (Device) → | Clears Flag Buffer |
| T2 | T2 | Clears IRQ FF (device) |
| T7 | PH1 · T7S · ($\overline{\text{OPO}}$ · EIR + OPO) → | STM 6-9 |
| | STM 6-9 → | Sets Interrupt Inhibit FF |

| MNEMONIC | PH | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
|---|---|---|---|---|---|---|---|---|---|
| 2nd Machine Cycle Following Interrupt PHASE 4 | 1, 2, 3 | T0 · T5 | | | | | | | |

PURPOSE

T0 · TS clears Interrupt Inhibit
This sets Interrupt Control FF.
After T0 Higher Priority Interrupts can be serviced (ESR High again).
Subroutine must clear Flag (device) to allow PRL line to function.

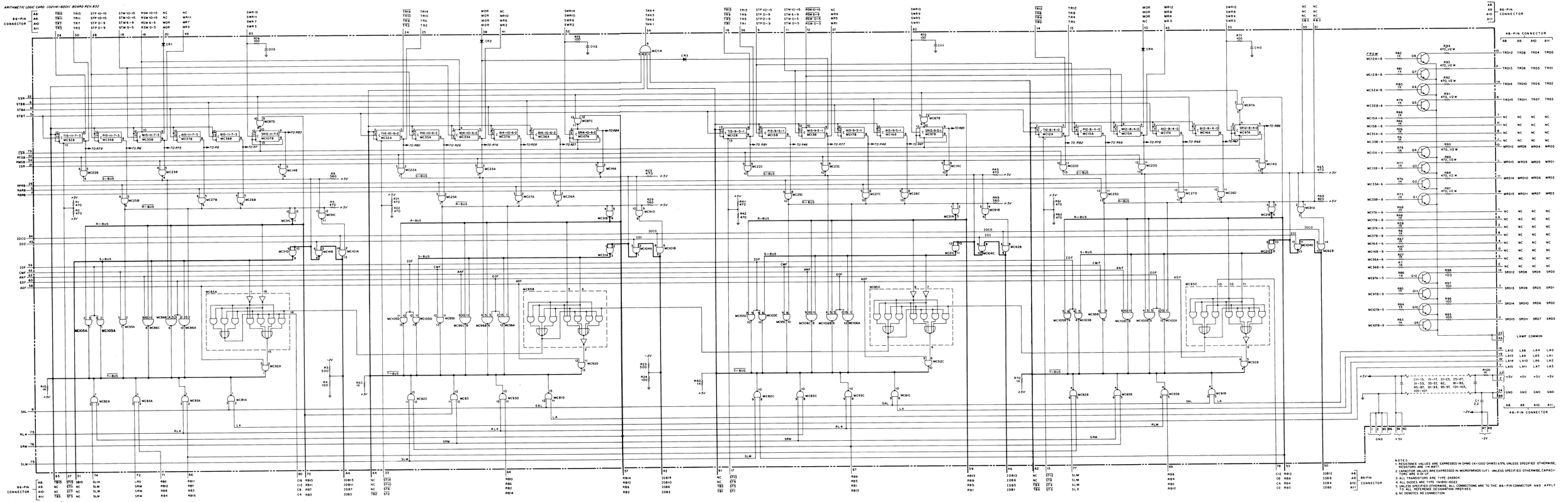



Figure 2-8. Logic Arithmetic Logic

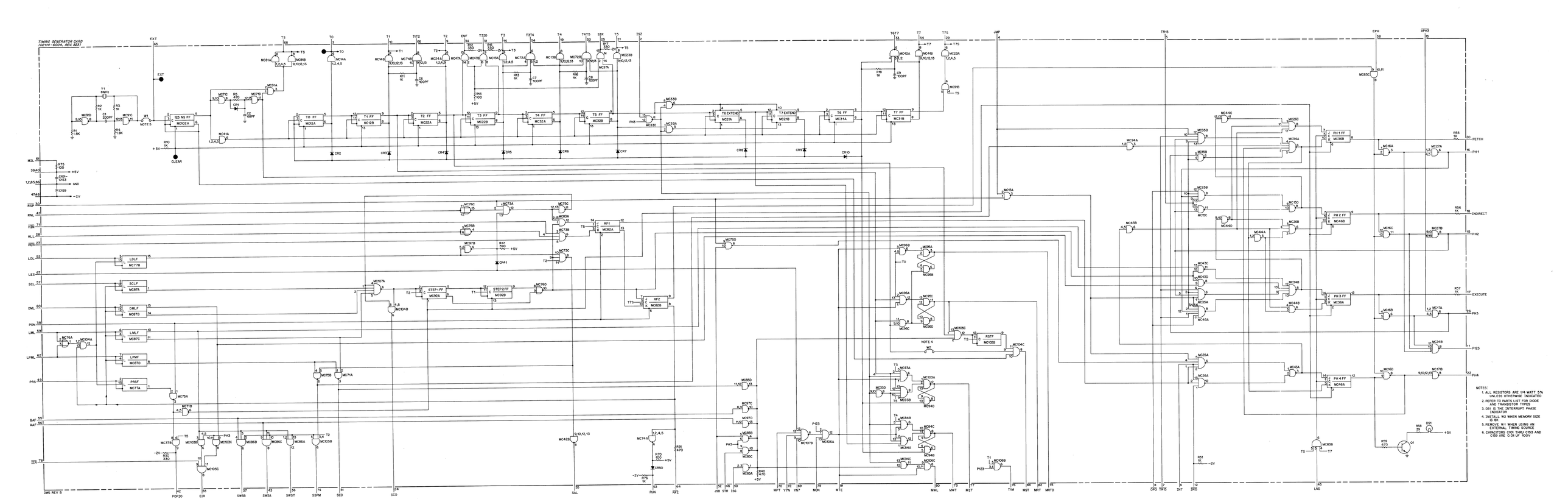



Figure 2-9. Logic System Timing Generator

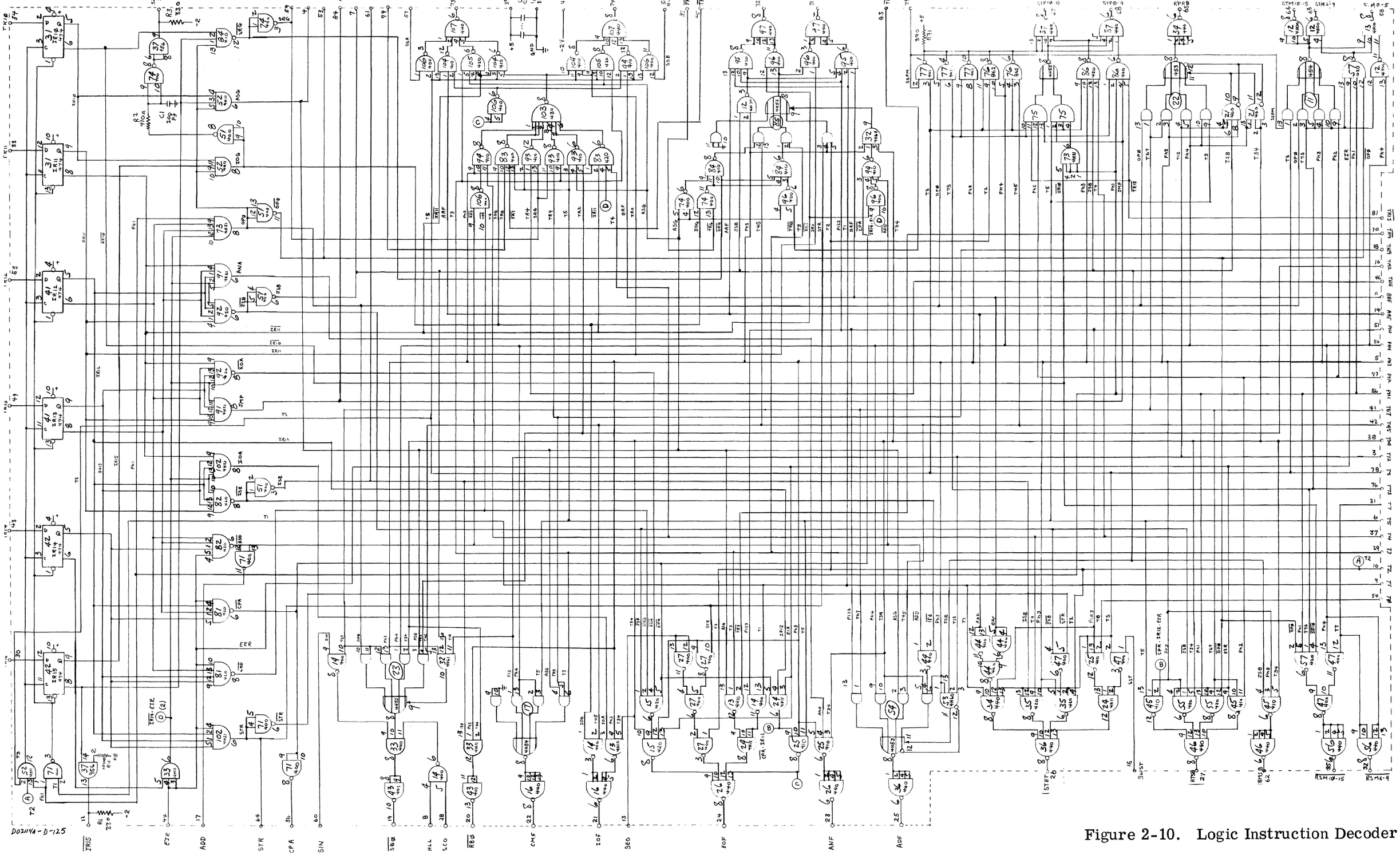



Figure 2-10. Logic Instruction Decoder

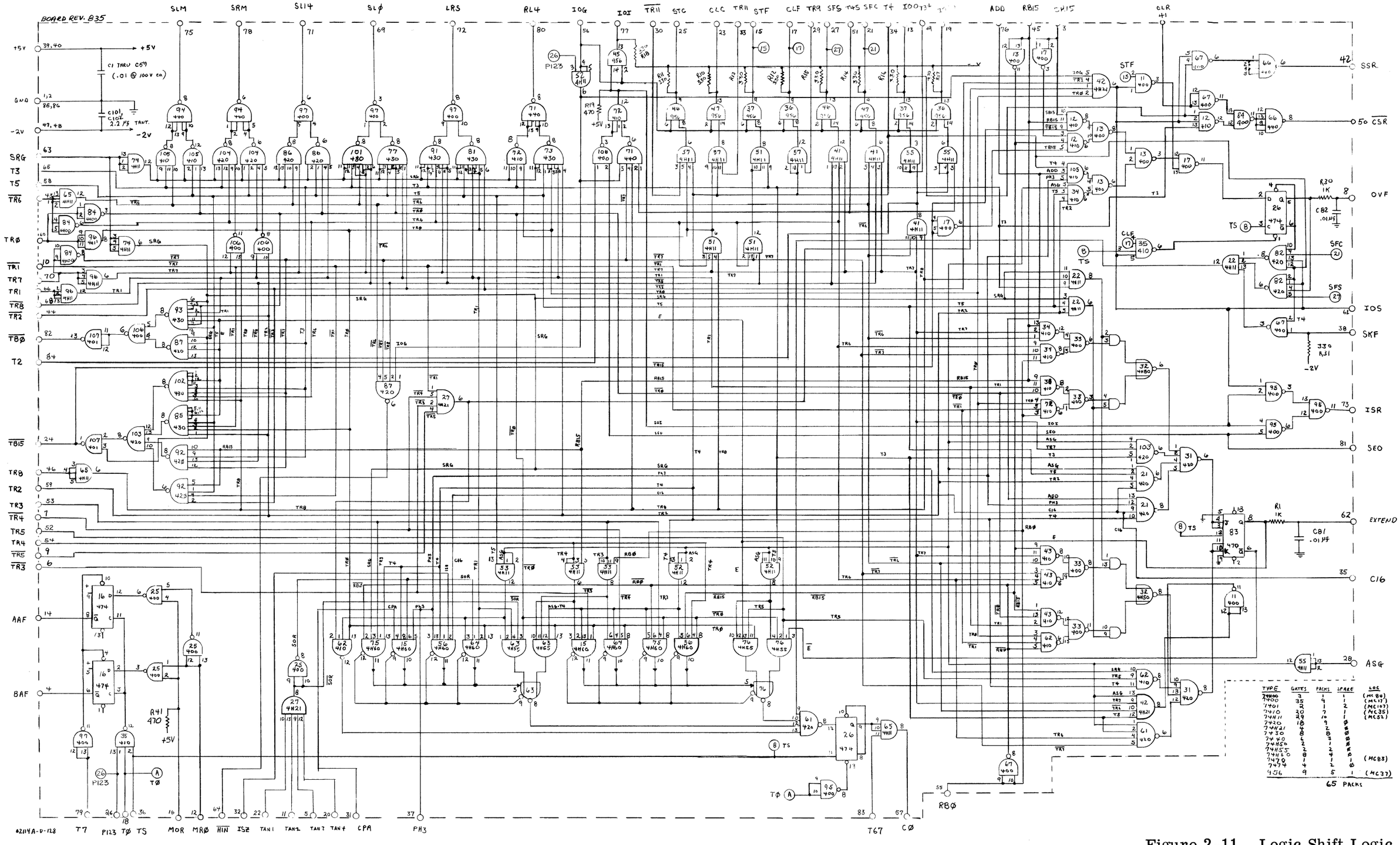



Figure 2-11. Logic Shift Logic

# section memory

III

# SECTION III
# MEMORY

## 3-1. INTRODUCTION

The 2114A computer contains a ferrite toroidal memory module. The cores are arranged in an array with appropriate address mechanisms. Driver-Switch boards provide the means to convert address information into actual core reading and writing currents. The Sense Amplifier detects the state of the core during read operation. The Inhibit Driver permits setting the state of the core during write cycles.

The core module design permits providing either 4096 addresses (called 4 "K") or 8192 (called 8 "K") within the package. The actual reading or writing requires power, but the passive core condition doesn't require any power consumption to retain the core information.

## 3-2. MEMORY TIMING

The basic computer memory timing remains the same during each cycle (except for ISZ). Early in the cycle the information is read out of the core. This process destroys the information content. It is necessary to rewrite the information back into core later in the cycle.

The approximate time required for the read or write operation is 500 nsec. The computer architecture was designed around the read time occuring during time periods TØ to T2, and write time T3 to T5. More specific timing information will be given in paragraph 3-9.

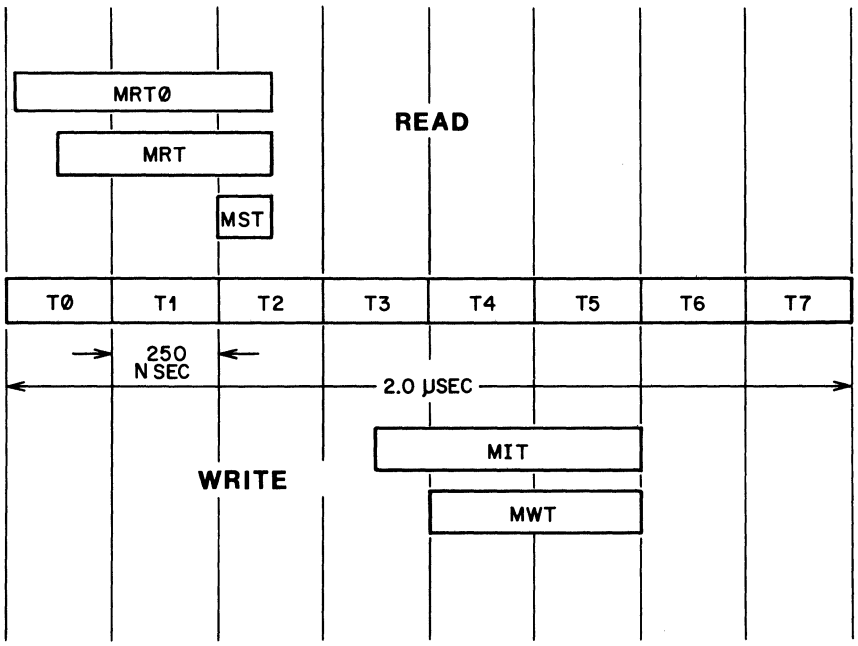



Figure 3-1. Memory Timing

## 3-3. FERRITE CORE CHARACTERISTICS

The utilization of ferrite materials for computer memories depended on the development of rectangular hysteresis loop material. Refer to Figure 3-2. The toroid provides a flux linkage between the primary winding and the secondary winding of a transformer. The flux will be oriented essentially one of two possible directions, referred to as being a "zero" or a "one".

The physical nature of the ferrite material retains the flux condition (polarity) until a certain current magnitude is applied to the primary winding. When the current increases to the proper level the flux refersal takes place rather abruptly and completely. Currents less than the critical amount are insufficient to cause flux changes.

The computer hardware design will provide a mechanism to establish full read-write currents causing flux reversal, or one half value currents with no flux changes. The induced voltage on the secondary winding will be 32 millivolts for a flux reversal, but less than 10 millivolts if no flux reversal takes place.

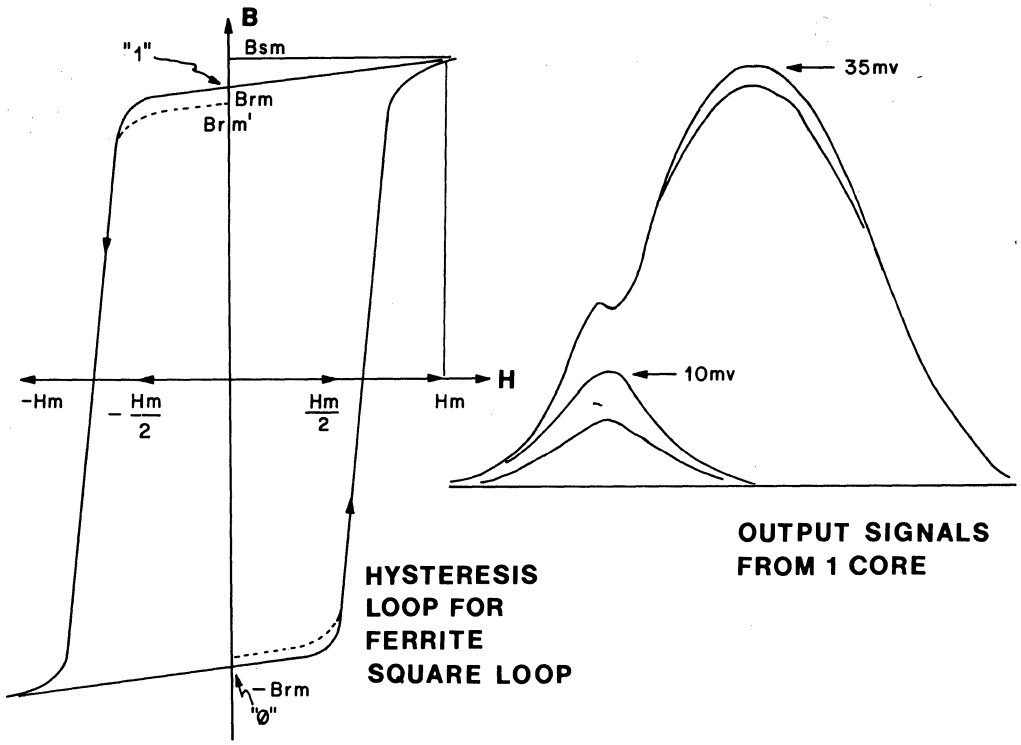



Figure 3-2. Core Characteristics

## 3-4. TOROID

The actual toroidal core is a tiny ring 30 thousands of an inch in diameter. The primary windings are X, Y, and Inhibit wires which merely go through the hole. The sense winding is the secondary and is coupled by the flux linkages.

The array of cores is traversed by both "X" and "Y" wires. The M register bits are encoded to select one X wire, and one Y wire. Each of these wires provides one half of the total necessary corrent for flux reversal. Current flows through both wires in the correct direction so that during read cycle the flux establishes the "zero" direction. During write cycle the currents establish the "one" direction. Each toroid contains four wires. The sense wire is a secondary which provides

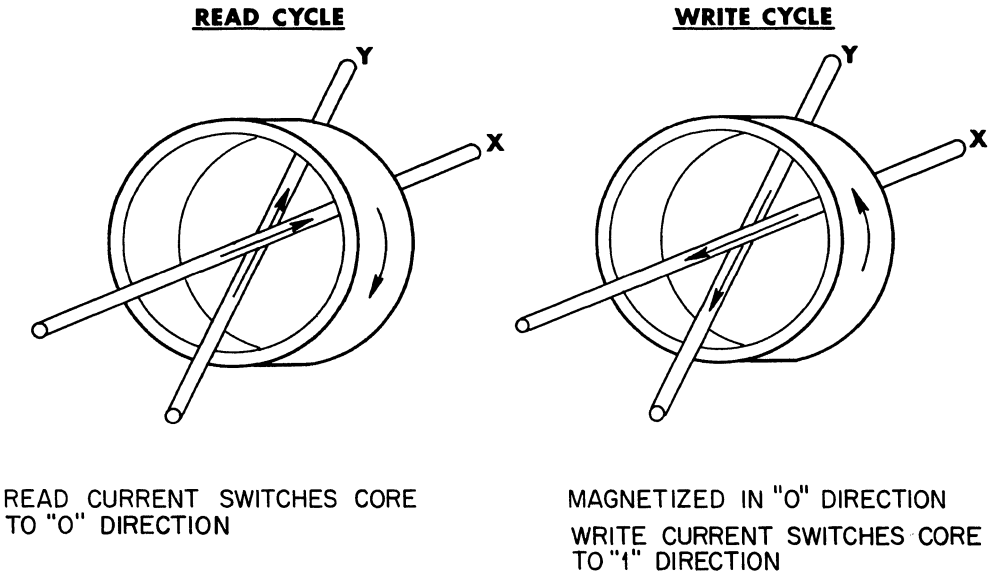



Figure 3-3. Read Write Currents vs. Core Status

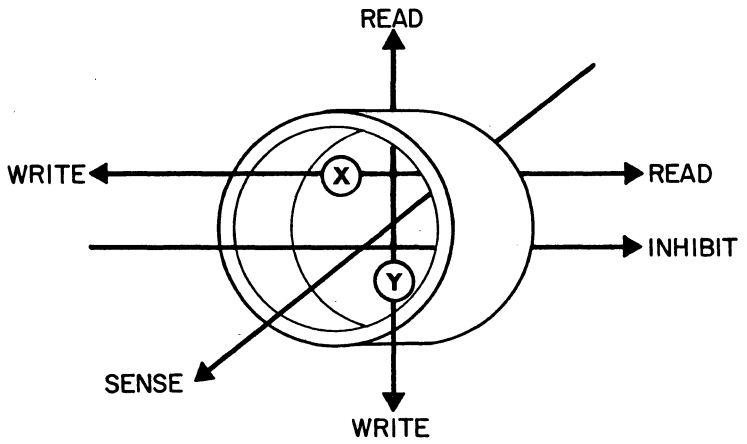



Figure 3-4. The 4-Wire System

interrogation during the read cycle to determine the previous state of the flux direction. The inhibit winding is the mechanism to prevent writing a one when the desired write state is a zero. This core system is commonly referred to as being a four wire - three dimensional system. The three dimension refers to the X-Y array on each bit plane, plus the "Z" dimension for 17 bits. Refer to Figure 3-5.

## 3-5. CORE ARRAYS

The toroids are arranged in a 64 by 64 array. (Refer to figure 3-6.) Each mat thus has 4096 cores. Each mat is associated with one specific bit in the computer word. A 4K module has 17 such mats. One for each bit from Ø to 15, plus the Parity bit. Associated with each bit mat is a

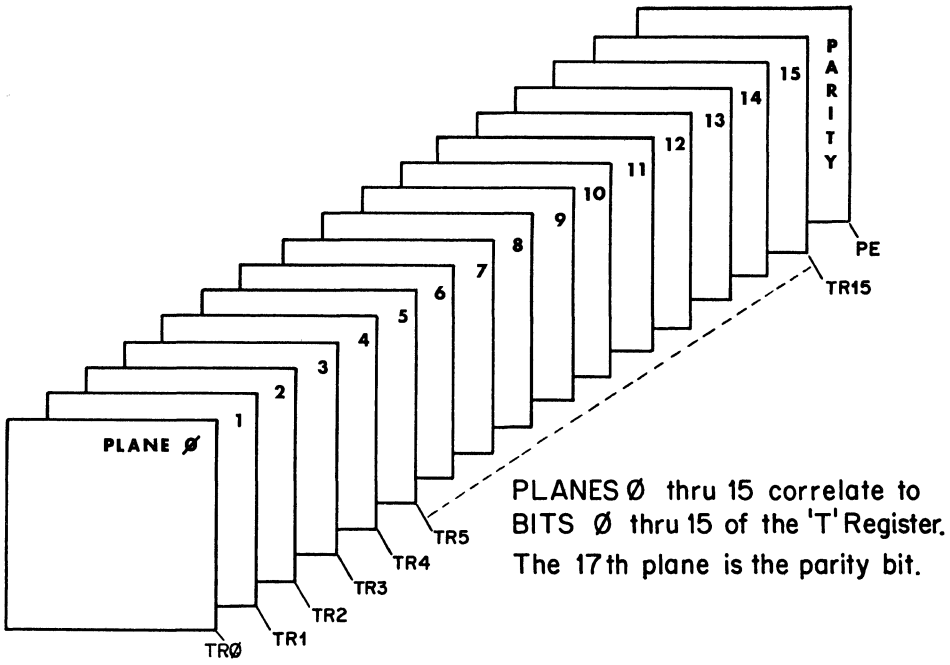



Figure 3-5. Each 4K Core Module has 17 Core Planes

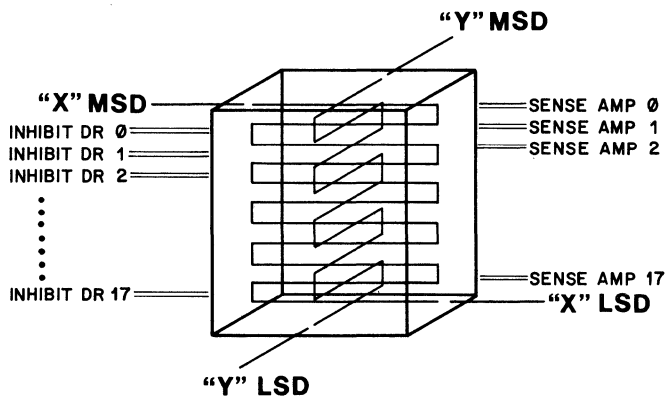



Figure 3-6. Core Module Addressing and Data

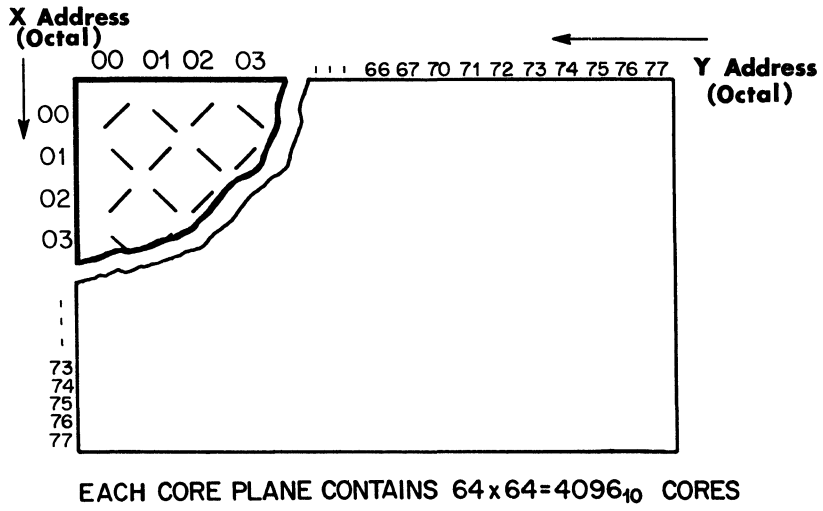



Figure 3-7. The Core Plane

Sense Amp winding and an Inhibit winding.

In the X direction the core has 64 wires which traverse all 17 mats. In the Y direction 64 wires also traverse the entire mat structure. The X address defines a plane through the entire core structure. The Y address defines a similar plane. The intersection of these two planes is a straight line defining 17 cores, one on each bit mat. (Refer to Figure 3-7).

It should be pointed out that this description is figurative and not literal. The actual core array in the 2114A has four bit planes on each frame.

## 3-6. ADDRESSING

The Memory Register contains the computer memory address. The information in the register is in binary form. The 64 address wires in each direction are designated in octal notation and range from ØØ to 77. The computer word address ranges from ØØØØ to 7777 providing the 4096 decimal locations. This requires 12 binary bits. These 4096 addresses are arranged in four pages. Paging will be discussed later. The maximum number of 4 K modules provided for in the 2114A is two. Another binary bit is required to indicate the lower or upper 4K module. The entire 2114A memory can be addressed with 13 binary bits (Ø to 12).

The X and Y wires through core are arranged in groups of eight. At the common end they are connected together in address groups of ØØ to Ø7, 1Ø to 17, 2Ø to 27, etc. The most significant octal digit corresponds to M reg. bits 3-5 for the X and 9-11 for the Y address.

The least significant end of these wires are connected together (using a diode matrix) in groups of eight. In the case of least significant octal digit corresponding to one, the addresses would be Ø1, 11, 21, 31, 41 and so on. The purpose of the driver switch circuit is to connect the common end (most significant digit) to the proper power supply voltage and to connect the diode end (least significant digit) to its proper supply voltage. The current polarity through these addressing wires is bi-polar. For read and write operation current must be capable of flowing in either direction. This is provided for on the least significant end by the diode matrix. Each individual wire is connected to two diodes, one anode and one cathode. The drivers and switches drive these diodes in groups of eight. Each wire thus has two possible diodes, either the common anode end or common cathode end. This provides current flow in the proper address wire and isolation by the back biased diode to the other 7 lines.

**M-REGISTER**

| | Y | | X | |
|---|---|---|---|---|
| | Dr. | Sw. | Dr. | Sw. |
| A | 7 | 4 | 0 | 1 |
| B | 7 | 5 | 7 | 6 |

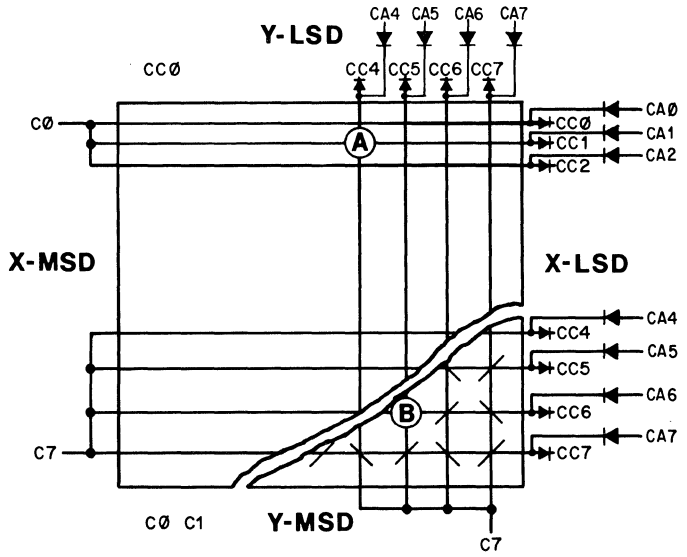



Figure 3-8. Memory Address Identification

## 3-7. DIODE MATRIX

The core module has two diode matrix boards. The purpose of these diode matrix boards is to allow the driver switch assembly to select the least significant bit, using the common anode or the common cathode for correct polarity current. Those address wires which are not in use will be eliminated from the circuit consideration by virtue of their back biased diodes. The least significant octal inputs to the diode matrix board are the eight common cathode leads associated with bits Ø through 7, and the eight leads associated with the common anode bits Ø through 7. The most significant octal bits are provided by the 8 common leads ØX to 7X.

Figure 3-9 shows the diode matrix circuit. The eight common inputs associated with most significant bits are shown on the right margin. The common cathode and common anode diode inputs associated with bits XØ through X7 are located on the lower margin. Figure 3-10 shows an enlarged portion of the diode decoders associated with common bits 3 and 6 and common cathode and common

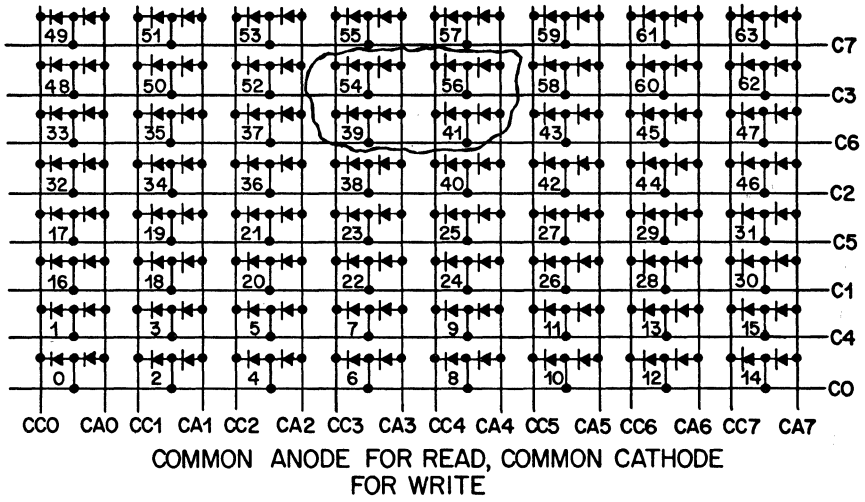



Figure 3-9. X-Y Diode Decoders

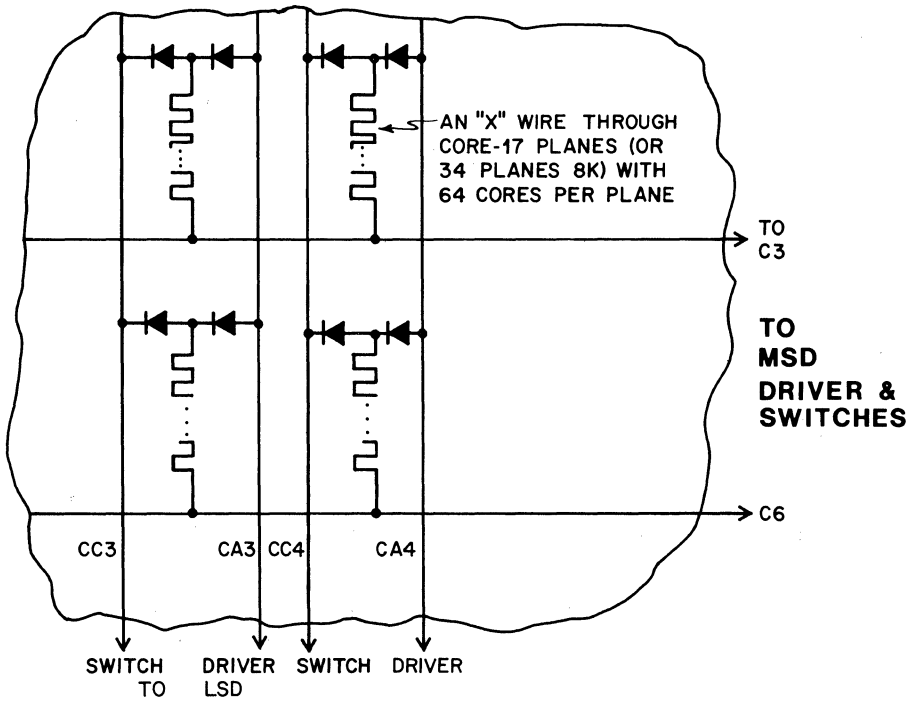



Figure 3-10. Octal Input Lines to Core

anode bits 3 and 4. The address wire (X or Y) which traverses core is shown in the figurative sense between the diode junction and the common lead. Each of these wires traverses the 17 bit planes associated with each 4K of memory.

Figure 3-11 shows figuratively how the driver switch assembly makes the appropriate connections to allow current to flow through these address wires. For example; if the common bit 3 is switched to the plus supply that means the current must flow through the common cathode bit 4 to the minus supply (ground). This establishes current flow through the "X" wire octal 34. If this had been necessary during the read portion of the cycle, then during the write portion of the cycle the currents are reversed and the common lead 3X would have to go to the minus supply and the common anode lead on bit X4 would be connected to the +20 volt bus.

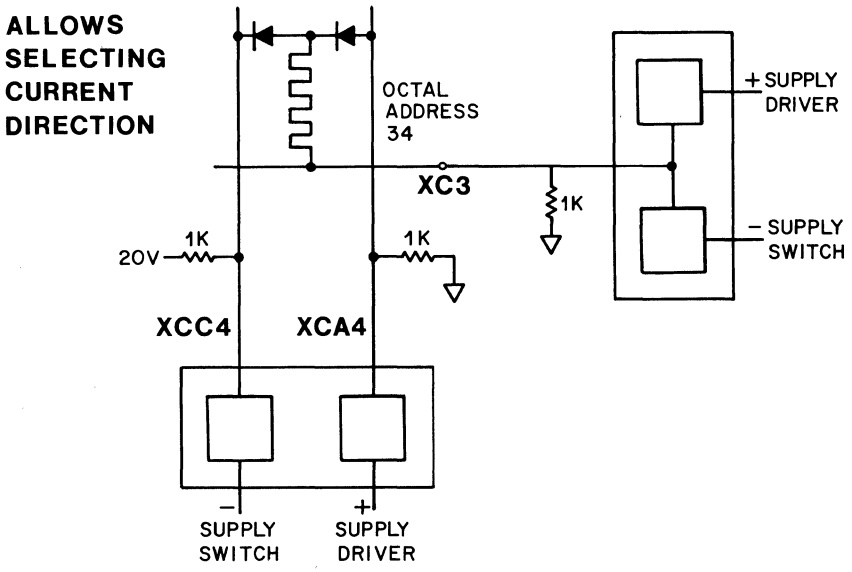



Figure 3-11. Driver Switch Voltage Buses

## 3-8. DRIVER-SWITCH ASSEMBLY

Figure 3-12 shows a selected pair of "X" driver-switch circuits. The common line corresponds to address X2. The function performed by this assembly will be to apply 20 volts through Q30 to the common lead 6 during write operations, and ground the common cathode end with Q16, 17. During write the common end is grounded through Q28, 29 and the common anode is connected to 20 volts through Q18. The operation above corresponds to addresses in the lower 4K module. The words read and write should be interchanged for operation in the upper core module. Refer section 3-10.

The ends which are switched to ground are directly coupled by transistor switches. The TTL logic level provides a convenient drive level to the transistor base. Transistors Q16 and Q17 on the common cathode, and Q28 and Q29 on the common line constitute the switch circuits.

The ends of the address line which must be connected to the +20 volt bus are done so by a single transistor - the DRIVER circuit. The DC design considerations for direct base drive would be difficult. A transformer provides the necessary DC isolation. The DC return for the transformer primary is provided to the +5 volt bus (when PON signal is present).

The NAND gate low output allows transformer primary current which forward biases the base to emitter junctions of transistors Q18 and Q30.

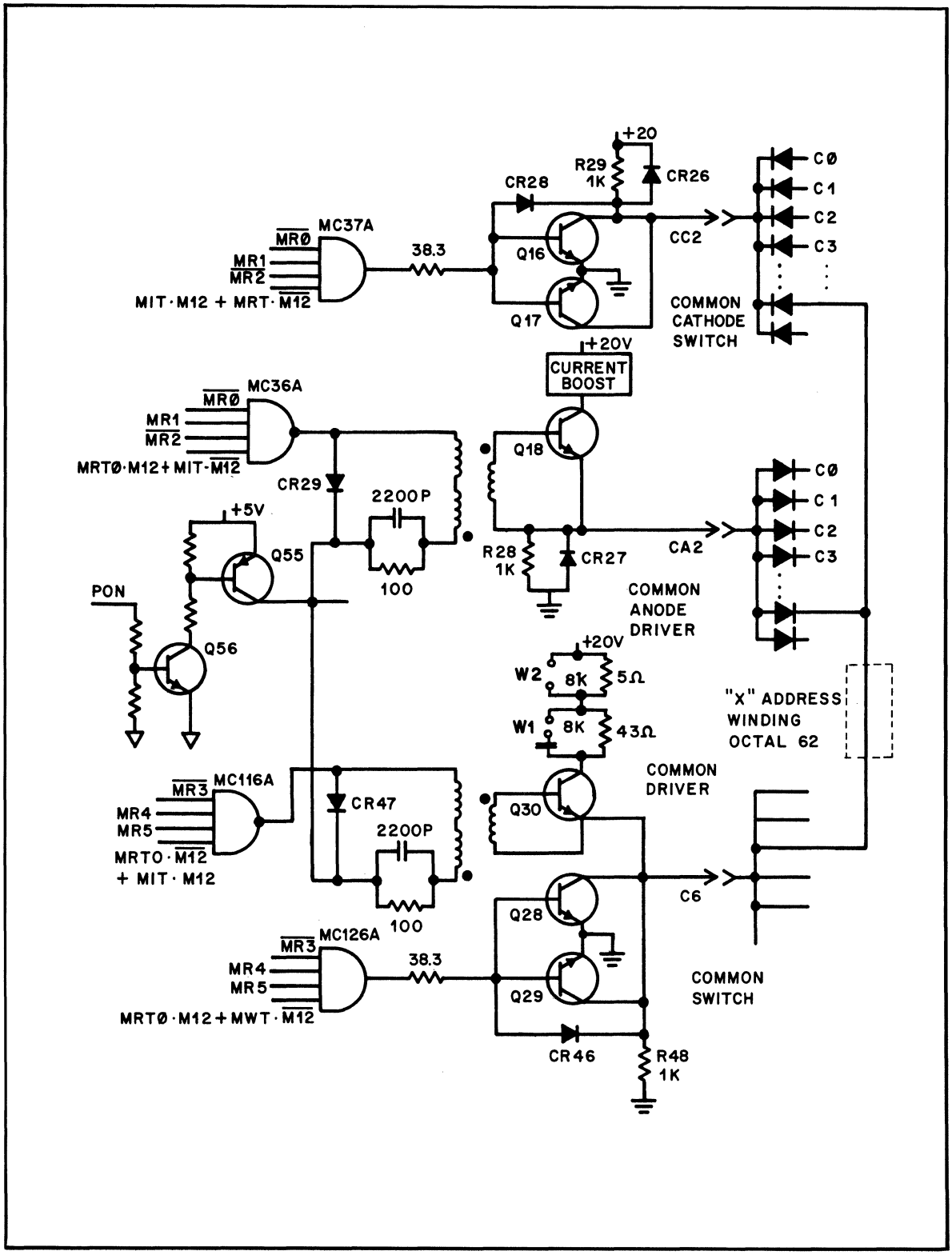



Figure 3-12. Driver/Switch

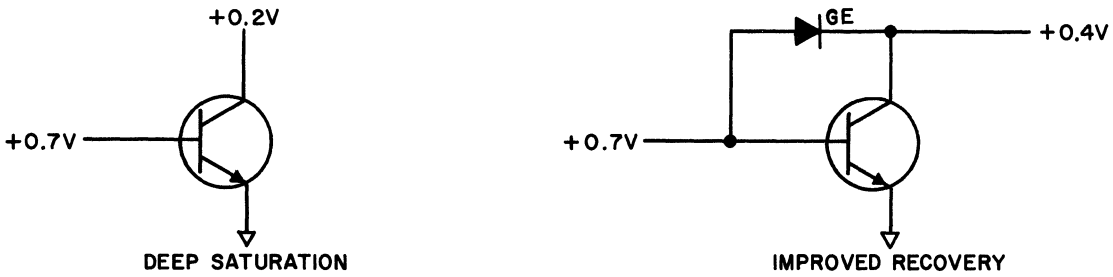
The RC network allows high turn on current to speed up the transformer output and overcome the transistor input capacity. The drive then reduces to an adequate hold on level.

## 3-9. DRIVER SWITCH TIMING

A review of Figure 3-1 will indicate the timing relationship between MRTØ and MRT, and between MIT and MWT. The Driver circuits are always switched on during the earlier memory timing pulse. This insures that the driver transistor (Q18 or Q30) is saturated before significant current must flow.

The power dissipation in the transistor switches is low during saturated conditions. The power dissipation is significant during turn on and turn off switching. Two transistors are provided to insure an adequate safety margin (even in the case of poor saturation voltage characteristics or slow transistors).

The transistor switches are also used to cut off the current flow at the end of the conduction pulse. Diodes CR28 and CR46 are germanium diodes to allow rapid switch off. A saturated transistor contains excess stored charge in the active transition region. The turn off delay depends greatly on the transistor doping and temperature.




The Germanium diodes CR28 and CR46 are used on the base to collector junctions to prevent such deep saturation. This controls the current waveshape and makes it less sensitive to individual component parameters.

## 3-10. COINCIDENCE - ANTI-COINCIDENCE

The core stack is designed so that the Coincidence of the X current of one half value plus the Y current of one half value is sufficient to change the flux polarity in the core for both read and write operation. A mechanism providing anti-coincidence current is used which enables the same X and Y wires to address the entire 8 K. This is accomplished by reversing the polarity of the X current between the 4 K modules. In the lower 4 K (when we are addressing the lower 4 K) both currents add up and allow flux changes. In the upper 4 K (that is from 4K to 8K) module both currents are present but because of the phasing of the X wire the currents cancel. The net current in the Non-addressed module is zero. It is possible thus, to use one set of driver switch boards to provide the X and Y currents for the entire core module. The current of the X wire is reversed in the upper module by physical construction. The current of the Y wire remains the same through the entire 8 K. Thus both X and Y wires traverse the 17 bit planes associated with the lower 4 K and continue then through the 17 bit planes associated with the upper 8 K. It is necessary to provide separate Sense Amp assembly and Inhibit Driver assemblies since these are necessary bit by bit. Bit 12 in the M-Register determines which core module is addressed. $\overline{M12}$ indicates the lower 4 K module and M12 indicates the upper 4 K module.

## 3-11. ADDRESS EXAMPLE

Consider an example in the lower 4K module with address XX62. Using Figure 3-12 we will trace through the sequence of events. Since we are assuming the lower module only those circuits in which $\overline{M12}$ occurs will be used. Those circuits using M12 will not be used.

The M-Register contents are available to the board. Binary bits Ø, 2, 3, and 12 are low, bits 1, 4, and 5 are high (EXAMPLE: O OOO OOO OOO ●●O O●O). Bits 6-11 associated with the Y address can be any condition in the example. The M-Register complimentary signals are also generated on the driver switch assembly.

Bits Ø-2 are associated with the common anode and common cathode memory lines. Only the driver and switch associated with octal address X2 can be energized. Similarly the bits 3-5 are encoded permitting operation of octal address 6X.

At TØ as MRTØ goes high NAND gate MC116A is enabled, saturating transistor Q30, pulling the common end to +20 volts. 120 $\mu$sec later as MRT signal goes true MC37A is enabled turning on transistors Q16 and Q17. Read current now flows through X address wire 62. At T2 plus 120 nsec the MRT and MRTØ signals fall. The switches cease to conduct, current stops, and address line 62 returns to its normal quiescent state.

At T3 plus 120 nsec MIT goes high turning the driver transistor Q18 on. At T4 MWT turns on Q28 and Q29 and write current flows through address wire 62. At the end of T5 the MIT and MWT signals go low, the switches cease to conduct, current stops, and address line 62 returns to its quiescent state.

## 3-12. PROTECTION DIODES

Certain protection devices are present to safeguard the components. In the common cathode switch circuit diode CR26 prevents the flux decay in the cores from pulling the common cathode line more positive than 20 volts thus protecting the collector junctions of transistors Q16 and Q17. The inductive kick as the X addressing current ceases would endanger the transistors without this protective diode. The common anode circuit transistor Q18 is protected by CR27. This prevents the inductive kick when the address current ceases from damaging transistor Q18 by pulling its emitter more negative than ground. In the transformer circuits diode CR29 in the bit 2 and diode CR47 in the common bit 6 are provided to protect the integrated circuit packs against the inductive kick due to the flux decay in the transformer. The design of the transformer circuit provides a current limiting resistor of 100 ohms and a speed-up capacitor of 2200pf which gives fairly high initial currents to overcome the stored charge in the transistor for quick turn on.

## 3-13. CURRENT BOOST

Current boost circuits are provided which allow shaping of the current pulses. The circuit associated with common bit 6 has a current boost associated with it. Observe the 43 ohm resistor between the +20 volt bus and the transistor collector. This 43 ohm resistor provides an exact current in the address wire. It will be noted that a jumper exists to use the bypass capacitor (520pf) for the 8 K core stack but is unused in the 4 K core stack. This jumper is W1. 5 ohm resistor is also present. Jumper W2 is used to short out this 5 ohm resistor for an 8K installation. In both cases the different characteristics of the 4 K and 8 K core module requires the changes. The 5 ohm resistor added in the 4 K module allows the total resistive component of the address wires to remain the same in both cases. The resistance difference between 4K and 8K is approximately 5 ohms. The inductive and capacitive loading of the address wire is also different between 4 and 8 K.

The purpose of the parallel 520pf capacitor in the 8 K unit is to allow current shaping which helps overcome the additional capacitance of the core stack.

The characteristics of the common lead 6 or common anode diode lead 2 in the core is different. The impedance as seen by the common lead 6 is essentially the inductance and capacitance associated with the 8 wires. On the common anode driver 2, however, the 8 wires are connected through the diodes, each in turn go through to the other end of the core and are electrically connected to 7 other wires which come back through core. The impedance seen through the common anode lead is essentially the capacitance of all 64 wires throughout core. Because of this greatly increased capacity it is necessary in utilizing the common anode driver to give an additional current boost. Figure 3-13 shows the current boost circuit utilized with the common anode driver. This circuit provides an additional 22 ohms to the +20 volt bus in parallel with 43 ohm or 48 ohm normally used.

As we follow the circuit operation we will see that the logical input is the MRTØ · M12 or MIT · $\overline{M12}$. When either of these signals is present transistor Q50 is saturated and the signal is AC coupled to transistor Q51 which is turned off allowing Q52 to conduct. Q52 turns on transistor Q53 which connects the 22 ohm resistor to the +20 volt bus. The amount of time that this boost circuit is required depends on the configuration whether 4 K or 8 K. The AC coupling between transistors Q50 and Q51 consist normally of the 330pf capacitor. For 8 K operation an additional 270pf capacitor is added. On the Y address driver, using pins 74 and 76, a jumper on the back plane enables an additional 220pf capacitor to be added. So we have a boost circuit, the time characteristics of which depend on the jumper configuration. Diodes CR9 and CR91 provide for a timely termination of this current pulse. Transistor Q53, if allowed to enter a deep saturation, would be difficult to turn off. Diode CR91 between collector and base prevents deep saturation in transistor Q53. The utilization of this boost circuit with the external jumper allows both driver switch boards to be identical but still provide different characteristics for the X and Y drivers.

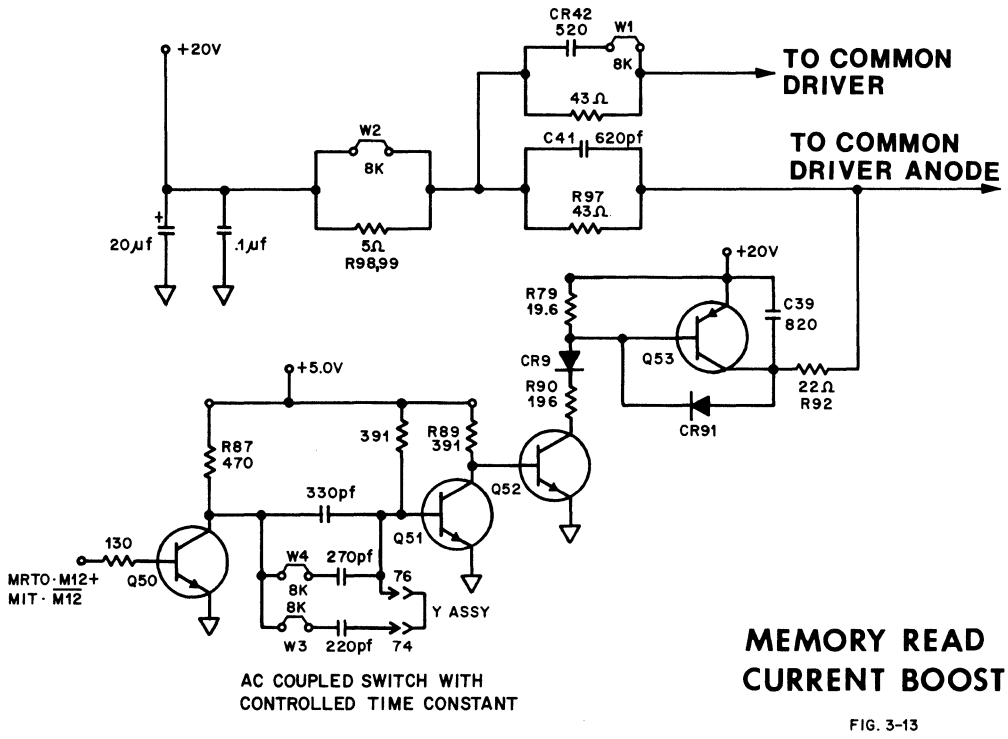
## 3-14. POWER ON

The Driver-Switch circuits are not enabled until the Power On signal is present. This prevents operating memory until PON is present. The voltage return for the transformer primaries for both of the driver circuits is returned to 5 volts through transistor Q55. Transistor Q55 is turned on and saturated whenever the PON signal is present. When computer power first comes on the PON signal is not present and it prevents the memory circuits from operating. When the PON signal does come up then the voltage to these driver circuits is enabled allowing normal memory operation.

## 3-15. PAGE ADDRESSING

The concept of page addressing and the utilization of T-Register bit 1Ø to designate the current page or the zero page sometimes needs clarification. The computer architecture utilizing 15 bits for memory addressing and the 16th bit for direct or indirect addressing, enables the addressing of 32 K of memory. The memory capacity of the 2114A computer is 8 K which means that bits Ø through 12 are sufficient for addressing all of core. This addressing information is contained in the M-Register.

In Memory Reference Instructions the bits which have been dedicated to the address are bits Ø through 9. Bit 1Ø enables us to remain in the current page or to force ourselves to the zero page. The 2114A computer has 8 pages of memory, the lower 4 K module has pages Ø, 1, 2, and 3, the upper 4 K module has pages 4, 5, 6, and 7. The bits associated with these pages are bits 9, 1Ø, and 11 plus bit 12 which designates the lower 4 K or the upper 4 K. In a Memory Reference type instruction


+20V
CR42
520
W1
8K
43Ω
TO COMMON DRIVER
W2
8K
C41
620pf
TO COMMON DRIVER ANODE
R97
43Ω
20μf
.1μf
5Ω
R98,99
+20V
R79
19.6
C39
820
CR9
Q53
22Ω
R92
R90
196
CR91
+5.0V
R87
470
391
R89
391
330pf
Q52
Q51
130
MRTO·M12+
MIT·M12
Q50
W4
270pf
8K
76
Y ASSY
8K
W3
220pf
74
AC COUPLED SWITCH WITH
CONTROLLED TIME CONSTANT
MEMORY READ
CURRENT BOOST
FIG. 3-13

the memory address contained in T-Register bits Ø through 9 contain the memory information within the current page. Bits 1Ø, 11, and 12 are retained in the M-Register and do not normally change with each individual instruction. It is possible to clear out bits 1Ø, 11, and 12 in the M-Register. This is accomplished by forcing bit 1Ø to Ø which clears out M-Register bits 1Ø, 11, and 12. The use of an indirect address utilizing bits Ø through 14 for the address and bit 15 for the direct-indirect allows setting all bits of the M-Register to a new value. Bit 1Ø thus serves the function of enabling a direct clear of the memory register bits 1Ø, 11, and 12 forcing the address into the base page. Figure 3-14 indicates the bit status and address limits of the memory pages.

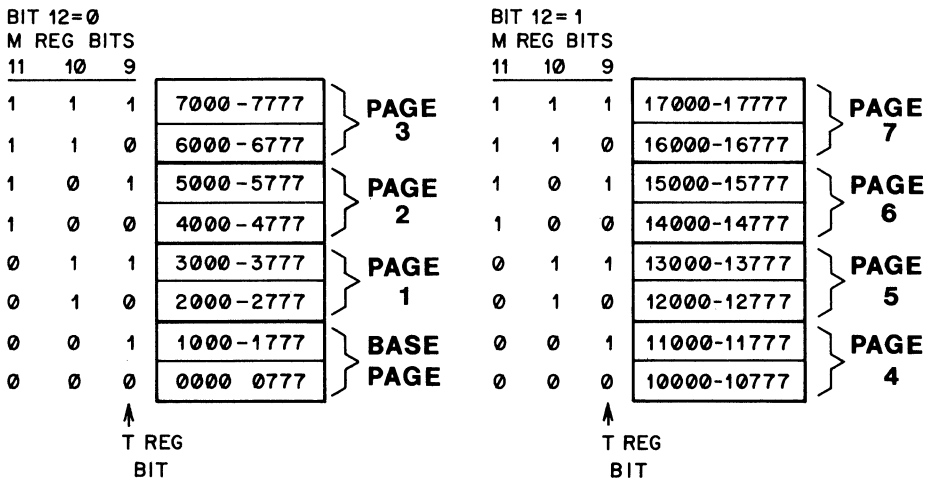



Figure 3-14. 8 K Core Page Addressing

## 3-16. MEMORY BIT INFORMATION

Information to this point has been dealing primarily with memory addressing. The utilization of X currents and Y currents enable addressing those 17 bits (Toroidal cores) associated with that address. The rest of the memory function will deal with the determination of the status of those 17 bits. Figure 3-15 shows a simplified example in which the X and Y currents enable reading or writing. These

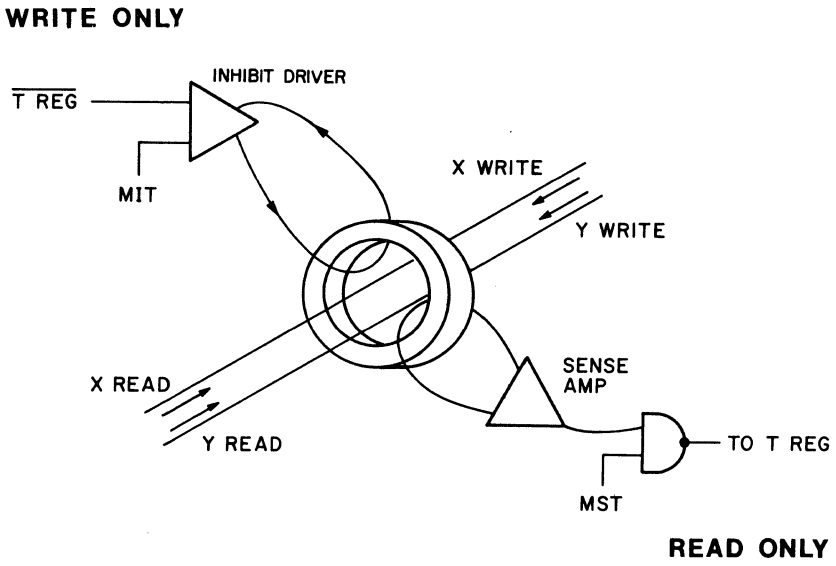



Figure 3-15. Four Wires

currents traverse the opening in the toroidal core. A secondary winding (the Sense Winding) also traverses the core and the changing flux orientation within the core enables the sense amp to determine the previous flux state. The information from the sense amp is then strobed with the Memory Strobe Timing (MST) pulse. It allows the sense amp information to set the T-Register.

During the Write part of the cycle the Inhibit Driver is controlled by the information contained in the T-Register. It allows inhibiting the address current so that the core can remain in zero state. If the inhibit current is not enabled the core is forced to the "one" condition by the X and Y write currents.

Figure 3-16 shows schematically the relationships of the Sense Amp and Inhibit Driver with the core stack and the T-Register Flip-Flop. This is drawn to represent data bit 9. The Sense Amp winding includes all 4096 cores on this bit 9 core plane. This winding provides an input to the sense amplifier. The output of the Sense Amplifier will be a one or a zero depending on what the previous state of the core was. The X and Y current drives the core toward the zero state and if the core changes state (which means that it has been a "one") then the sense amplifier will have an output. This output from the Sense Amp is enabled by the Memory Strobe Timing pulse. This output drives the direct clear side of the T-Register bit 9 and forces the T-Register to the one state. During the Write cycle the T-Register Q output is ANDed with the Inhibit Timing Pulse (MIT). If both signals are present the Inhibit winding allows current to flow which prevents the core from writing the "one" and allows the state to remain "zero".

It should be noted that the polarities of the signals are not obvious. The T-Register D input is the $\overline{TB9}$ (negative true signal), so the T-Register true output must come from the $\overline{Q}$ side of the flip flop. The sense amp goes to the direct clear (negative true). The presence of a flux change will give a sense amp output which is enabled by the Memory Strobe Timing. This negative true signal clears the T-Register flip flop which forces the $\overline{Q}$ high indicating a one in the T-Register. The Memory Inhibit Timing signal comes from the Q output (which is negative true) from the T-Register. If this is high it indicates that the T-Register contains a zero and we must inhibit the X and Y current from writing a one. The Inhibit Driver is enabled allowing current to flow through the Inhibit winding. This Inhibit winding traverses all 4096 cores in the bit 9 plane.

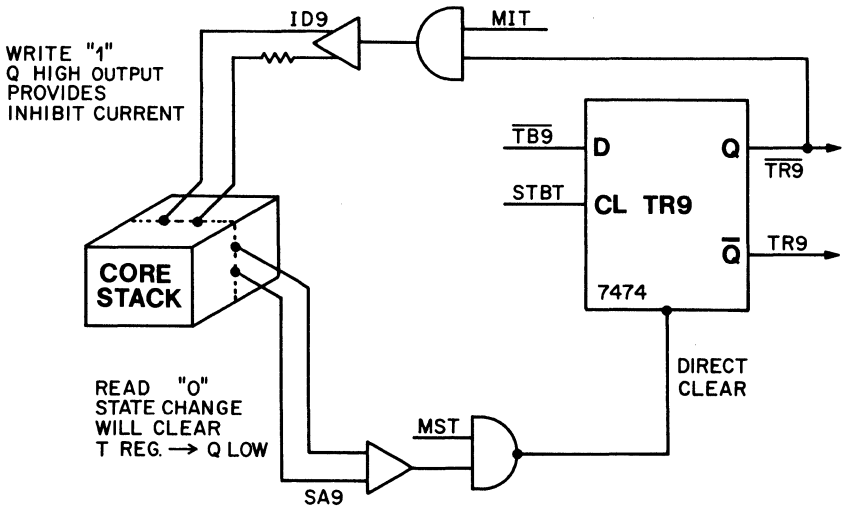



Figure 3-16. Data Sense And Inhibit

## 3-17. SENSE AMPLIFIER

The winding associated with the Sense Amplifier includes all 4096 cores on its respective bit plane. The output voltages indicated on Figure 3-2 represent the switching voltages for one core. As the Sense Amplifier winding passes through many cores the voltages are additive. To prevent the large number of cores which have one half current flowing from adding zero signal voltages giving a large apparent signal the sense winding must be wound in a special manner. The X addressing current flows through 64 cores of which one is the desired core being addressed. The Y current also flows through 64 cores of which only one is desired. The sense winding must enter these 127 cores one half in the positive sense, and one half in the negative sense. In this way the noise contribution (zero voltages) cancels. The anticipated signal thus is discerned from the noise by amplitude and by timing. The Sense Amplifier is strobed during the first 120 nsec of time T2. It also prescribes the requirement that the sense amplifier be able to handle both polarity signals.

Figure 3-17 shows a typical Sense Amplifier stage. The components are shown for bit Ø. This Sense Amplifier consists of a differential transistor pair, an accurate current source, a transistor amplifier and output gate. The integrated circuit pack contains the differential pair and a transistor to serve as an accurate current source. The base of this current source transistor goes to an emitter follower, transistor Q52. This transistor provides a stable voltage supply, and feeds all sense amplifier circuits. The current source transistor provides a stable current to the differential pair. This total current remains the same, so depending on sense winding inputs as one transistor current increases the other must decrease.

The voltage on the sense winding is applied to the bases of the differential pair. The current flow is approximately 7 milliamps total through the two differential transistors. This establishes steady state collector voltages of approximately +6.5 volts. As the low level sense winding voltage is applied to the bases one transistor increases current flow and the other transistor decreases current flow. The voltage changes on the collector resistors thus developing a differential voltage. This voltage across the collectors of the differential pair is applied to transistors Q49 and Q50. One of these transistors will be forward biased and will conduct. The collector voltage of the conducting transistor goes positive, pulling the emitter of the emitter follower Q51 positive, providing a high input to NAND gate MC37A. The Memory Strobe Timing (MST) signal, and the memory module information MR12 being present also enables NAND gate MC37A. This provides a negative true signal $\overline{\text{ST}\emptyset}$, which clears the T-Register.

The operation of this circuit is symmetrical so that either polarity signal on the sense winding operates the circuit in an identical fashion. In previous Sense Amplifier designs for the 2115A and 2116A computers a balancing potentiometer was necessary in the collector return. In this 2114A design a special integrated circuit pack is being used with tight specifications on the transistor balance eliminating the balancing potentiometer.

The voltages present on the Sense Amp winding are difficult to interpret. The voltages on the differential pair collectors and at the emitter follower output are better places to observe for troubleshooting purposes. The collector voltages on the differential pair are normally approximately +6.5 volts. Under signal conditions wave shapes will be visible with outputs at +4.5 volts and +5.8 volts. The wave shape on emitter follower Q51 will indicate large voltages at time T1 and T2, and T5 and T6. Only the signal present at time T2 is used by the MST signal.

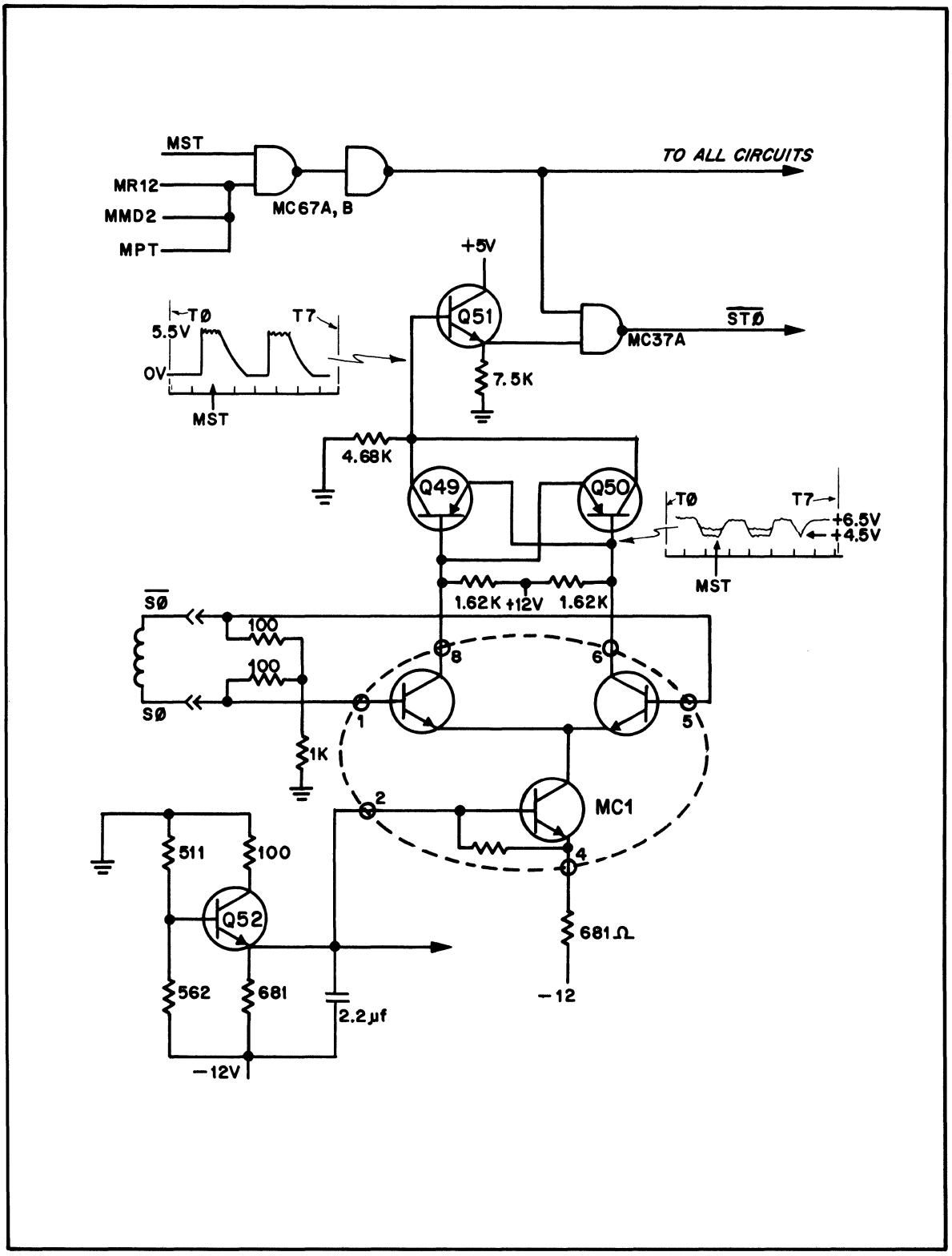



Figure 3-17. Sense Amplifier

3-18. INHIBIT DRIVER

The Inhibit Winding parallels the X current address winding on an entire bit plane. On the succeeding bit plane it follows the Y address winding. It thus alternates on alternating bit planes. The purpose of the inhibit driver circuit is to provide one half current through the inhibit winding which effectively cancels one half of the addressing current through the addressed core. This prevents the core flux to be written to the "one" state. One end of the inhibit winding is connected to the 20 volt bus through a 43 ohm resistor. A 1000pf capacitor provides current shaping to overcome the distributed capacitance of the core stack. The inhibit driver transistors, when conducting, ground the other end of the inhibit winding thus allowing current to flow.

The T-Register output (negative true) is wired directly to the Inhibit driver circuit. The presence of the $\overline{T}$-Register output along with the MIT signal permits operation of the Inhibit driver circuit. An individual Inhibit driver assembly is provided for the lower 4 K, and for the upper 4 K if installed. The MIT, MIL, and $\overline{MR12}$ signal is delayed between packs MC76B and MC76A NAND gates. This RC filter delays the start of the driver switch current. The transistor switches Q27 and Q28 have a germanium diode CR27 to prevent deep saturation. This allows expeditious termination of the Inhibit drive current pulse. Diode CR28 protects the transistor switches from the inductive spike when the inhibit driver current is terminated.

It will be noted that both the Inhibit Driver and Sense Amplifier assemblies have 17 circuits. Both provide the necessary bit for parity error operation.

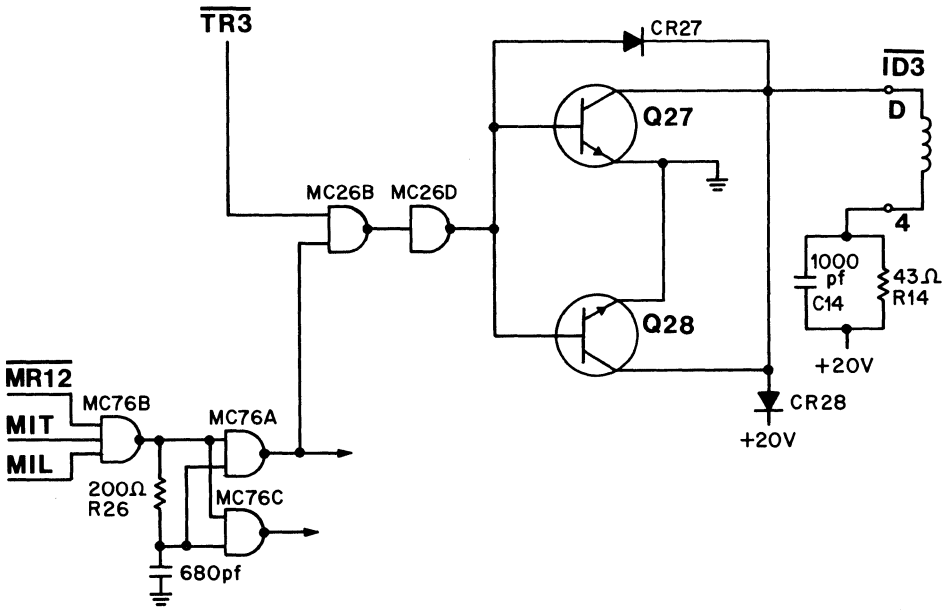



Figure 3-18. Inhibit Driver

3-19. MEMORY CORE MODULE CHARACTERISTICS

The 1/2 read and write currents are 320 milliamperes. The Rise and Fall times are 300 nsec, read and write pulse duration 400 nsec, inhibit pulse 500 nsec. The "one" voltage shall be at least 32 mv during the time period 400 to 500 nsec. The "zero" shall not exceed 10MV during the same period. The X and Y resistance is 5 and 8 ohms for 4 K and 8 K modules. The sense windings are about 16 ohms, the inhibit windings are 12 ohms.

The X and Y common address lines tie together sets of 8 adjacent lines. These lines alternate, 4 each on opposite sides. The inhibit windings alternately parallel the X and Y address lines on sequential planes through the stack.

## 3-20. 8 K CORE INSTALLATION

The installation of 8 K memory in a 2114A Computer requires changing the memory core module, and the addition of a Sense Amplifier assembly, and an Inhibit Driver assembly. The two Driver Switch assemblies remain sufficient, however, jumper changes must be made. On each Driver Switch assembly 4 jumpers must be added for 8 K installation. On the System Timing Generator (assembly 2114-6004) jumper W2 must be removed. The purpose of W2 is to delay the MST signal in an 8 K installation. When jumper W2 is removed in a 4 K installation it allows the MST signal to come earlier by 30 or 40 nsec. In the 8 K installation jumper W2 is installed delaying the MST signal to take care of the increased distributed capacitance between the 4 and 8 K memory module.

## 3-21. PARITY ERROR

The Parity Error option for the 2114 Computer is Accessory Model 12598A. This option provides parity interrupt to location 5, or computer halt when parity errors are encountered. The Parity Error assembly consists of control and flag circuitry for generating the interrupt, the bit comparison tree for determining odd or even number of bits in the computer word, and memory address flip flops.

The output of the bit comparison tree is compared with the parity bit. If this combination is odd no parity error exists. If this combination is even, indicating an apparent parity error, the interrupt circuitry is enabled. The memory address flip flops are set to the memory address at which the parity error occurred. Provisions on the 48 pin connector allows selection of parity error halt or parity error interrupt to a service subroutine.

## 3-22. BIT COMPARISON TREE

The bit comparison tree is made up of TTL, AND-OR-INV logic units. Each of these logic units compares 2 bits and determines whether the combination is odd or even. Thus the 16 bits in the computer word are compared two by two. The eight outputs of the first rank are compared two by two, the four outputs from the second rank are compared two by two. The two outputs of the third rank are compared. The single odd or even output representing the 16 bits is then compared with the parity bit flip flop. This final combination must be odd to prevent a parity error indication. The bit comparison must be odd to prevent a parity error indication. The bit comparison tree always compares the contents of the T-Register. This information is strobed only during time T3 when the MTE signal is present.

The output of the bit comparison tree is the $\overline{\text{TR16}}$ bit, which drives the inhibit driver. A negative signal on $\overline{\text{TR16}}$ will not enable the inhibit driver, thus writing a "one" in core. The parity bit flip flop is cleared during each T1M when memory is enabled. It is set by the Sense Amplifier Output $\overline{\text{ST16}}$.

The TTL logic packs in the bit comparison tree are high speed units. The typical delays in the AND-OR-INV is 7 nsec. The delay in the high speed NAND gates is 6 nsec. Typical delays through the entire bit comparison tree is in the order 70 nsec.

The use of the parity error assembly makes a powerful troubleshooting aid. It is necessary when installing the Parity Error assembly to reload all programs in order to generate the parity bit. Infor-

mation on the use of the Parity Error option is contained in the Operating and Service Manual for the Accessory 12598A, and in the Diagnostic Supplement.

## 3-23. MEMORY ERROR ADDRESS REGISTER

The Parity Error assembly contains 13 flip flops which are used to store the error producing memory location. The flip flops for bits Ø to 11 are D type latch flip flops. When the clock signal is positive the contents of the M-Register is allowed to set the flip flop. When the latch signal is negative the register contents will not change. Bit 12 ($\overline{M12}$) uses a D type edge triggering flip flop. Its operation is equivalent. The operation of the error address flip flops is inhibited by AAF and BAF signals (since the A and B-Registers do not contain parity bits), and the other conditions (LOAD ADDRESS, ISG, STR and JSB) which provide MWL positive except PH3 · ISZ. The operation under ISZ-PH3 operation is checked even though MWL is positive. When the comparison of the bit comparison tree and the Parity Bit Flip Flop is high (indicating no error) the latch inputs are negative preventing the contents from changing. When the comparison is low the latch inputs are held positive allowing the current contents of the M buses to set the address register. The contents of the address register are strobed to the IOB buses with an Input select code Ø5 instruction. Bit 15 is high during the same operation. (Bit 15 is used in the 2115A to differentiate between Parity Error and Memory Protect. This printed circuit assembly is used in both options with minor loading changes.)

## 3-24. FLAG AND INTERRUPT CIRCUITRY

The flag and interrupt circuitry on the Parity Error assembly are similar in operation to other flag and interrupt design. The computer Power On and PRESET control provide POPIO signal which sets up proper operating conditions for the Parity Error operation. The Parity Error operation can be inhibited with a CLF signal to select code 5. The functions of the Control Flip Flop, Flag Flip Flop, Flag Buffer Flip Flop, and IRQ Flip Flop is described in the I/O system operation volume 3. The interrupt outputs from this assembly are the IRQ5 address line and $\overline{PINT}$ signals or $\overline{PEH}$ depending on the hood orientation.

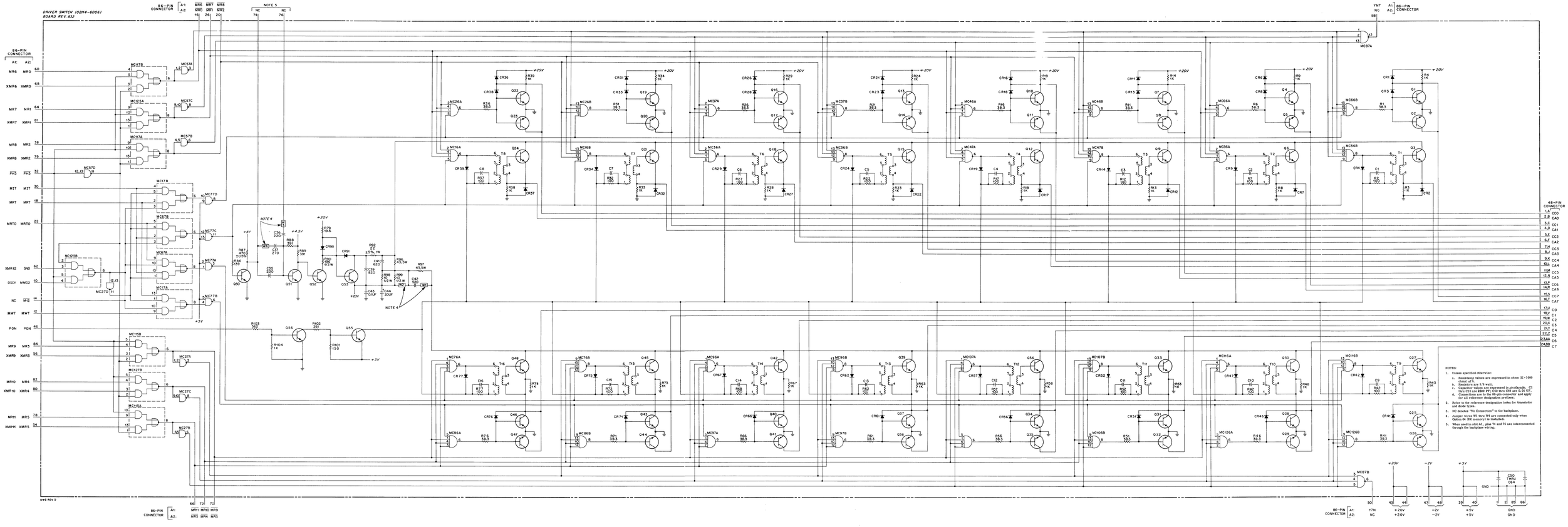



Figure 3-19. Logic Driver Switch

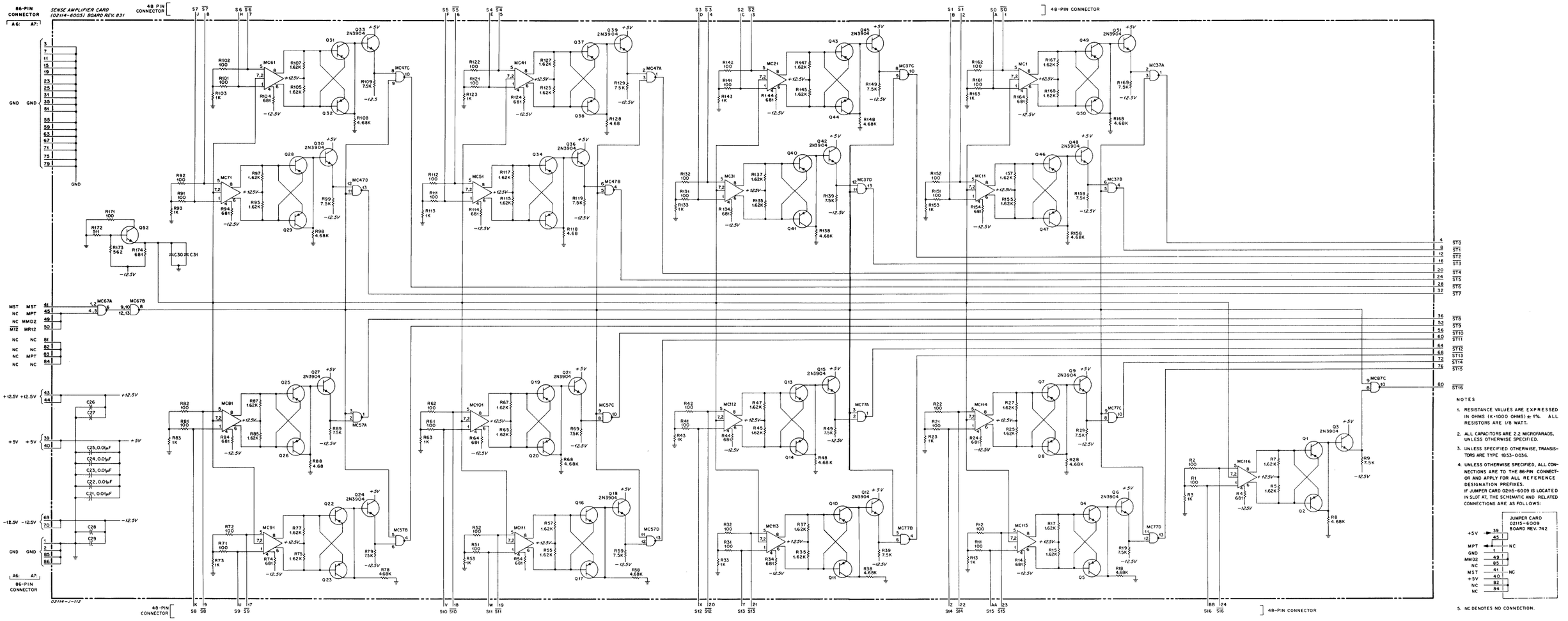



Figure 3-20. Logic Sense Amplifier

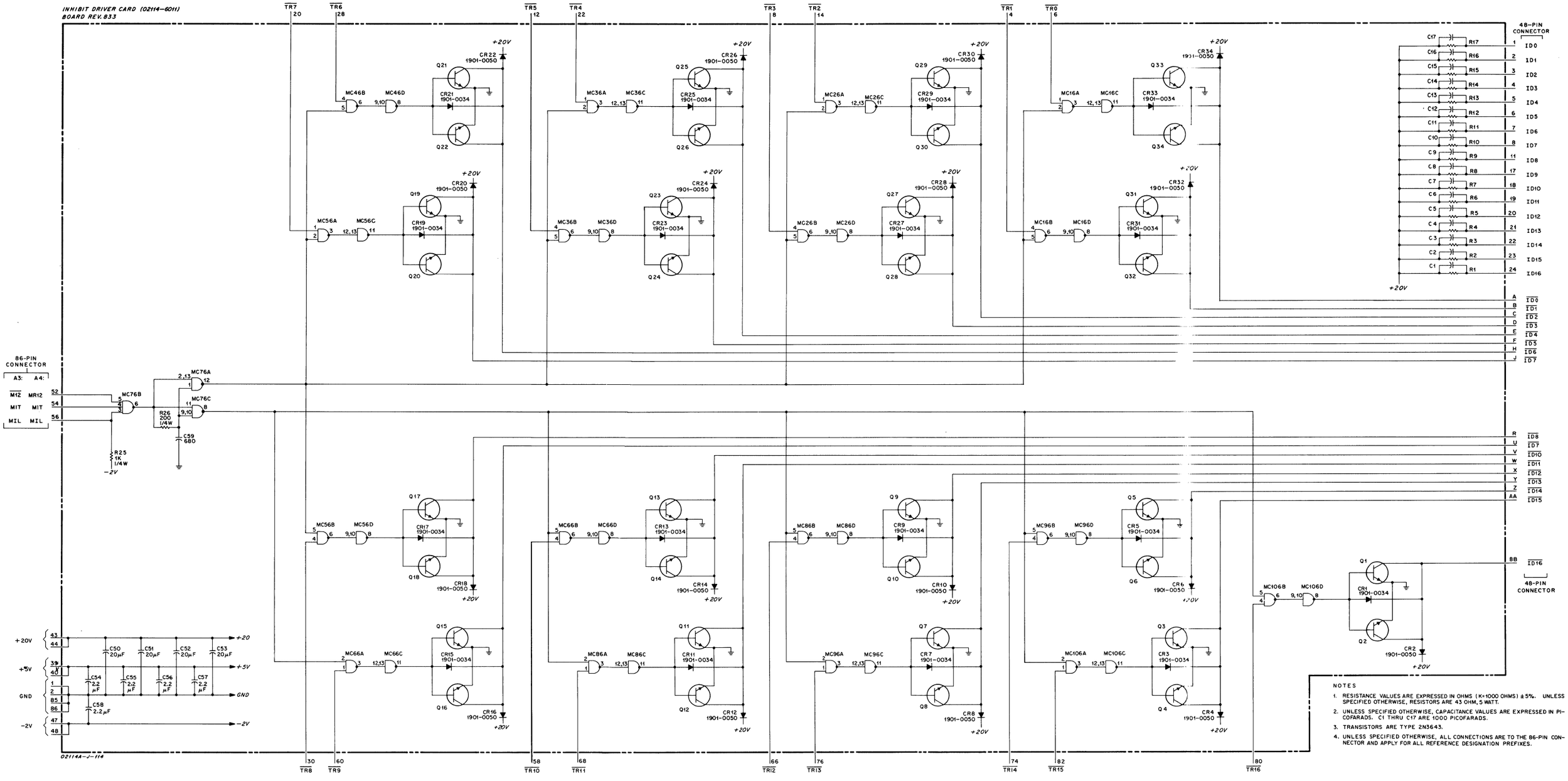



Figure 3-21. Logic Inhibit Driver

PARITY ERROR CARD (2114A)
BOARD REV. A-902-22

MTE 49 · T3 51 · PH3 30 · ISZ 28 · MWL 54 · BAF 56 · AAF 55 · ENF 22 · T1M 46 · STI6 60 · IAK 20 · IRQ5 29 · PEH 62 · PH5 21 · PINT 50 · TRI6 52

47 48 · 1 2 85 86 · 39 40

IOB15 33 · IOB12 34 · M12 42 · IOB11 74 · M11 71 · M10 72 · IOB10 73 · IOB9 76 · M9 67 · M8 68 · IOB8 75 · IOB7 83 · M7 79 · M6 80 · IOB6 84 · IOB5 82 · M5 77 · M4 78 · IOB4 81 · IOB3 8 · M3 14 · IOB2 9 · M2 13 · IOB1 5 · M1 12 · IOB0 7 · M0 11

+5V · -2V · -2V

MC83A · R51 1K · MC83(7) 1K · MC83A (1) 1K · MC83B · MC102B · R52 1K · MC103D · MC103C · MC75A · MC76C · MC76D · MC76A · MC76B · MC76E · MC94B · MC96D · MC94A · MC96C · MC95B · MC96B · MC95A · MC96A · MC104B · MC106D · MC104A · MC106C · MC105B · MC106B · MC105A · MC106A · MC16B · MC26D · MC16A · MC26C · MC15B · MC26B · MC15A · MC26A

MC73A · MC103A · MC92C · R49 1K · +5V · W4 · PB FF · MC102A · PB FF TEST POINT · MC22C · MC12E · MC12D · MC12F

+5V · R43 1K · MC93B

R46 1.5K · -2V · MC42A · R48 470 · R47 47 · C44 1000pf · R49 1K · +5V · MC42B

MC12 · MC22B 5,4 · MC22A 1,2

C41, 42, 43 2.2μF · -2V

C1-25, C27-40 .01μF · +5V

48-PIN CONNECTOR · S · 10 · 12

NOTE: REVERSE 48-PIN CONNECTOR FOR INTERRUPT ON PARITY ERROR

IRQ FF · MC92B · MC92D · MC92A · R44 470 · +5V

R50 1K · +5V · W5 · MC42C 11,12

MC84C · MC84D · FLAG BUFFER FF · MC74A · MC72C

FLAG FF · MC75C · MC84B · MC84A

MC74B · MC22D · MC73B

R31 470 · +5V · MC72A 1,2 · MC72D · R40 1.5K · -2V · MC72B

CONTROL FF · MC75A · MC73C · MC73D · MC85A · R54 1K · -2V

MC85B (7) 1K · -2V · MC85B · MC86B · MC86C · R41 470 · -2V · R34 1K · C26 .01μF · MC85A 1K · -2V · R45 1K · -2V

MC35 · MC25D 12,13 · MC25C 9,10 · MC25B 4,5 · MC25A 1,2

MC45 · MC33D · MC33C 9,10 · MC33B · MC33A 1,2

MC13 · MC23D · MC23C 9,10 · MC23B · MC23A 1,2

MC43 · MC32D · MC32C · MC32A · MC32B

MC46 · MC44D · MC44C · MC44A · MC44B

MC36 · MC34D · MC34C · MC34A · MC34B

MC24 · MC14D · MC14C · MC14A · MC14B

12595A-J-001

IOI 64 · IOG 57 · SCL(5) 66 · SCM(0) 59 · STF 19 · PEI 61 · POPIO 45 · CLF 32 · PRL5 58 · PRL4 63 · SIR(T5) 53 · TR0 41 · TR1 38 · TR2 35 · TR3 37 · TR4 25 · TR5 24 · TR6 26 · TR7 23 · TR8 17 · TR9 15 · TR10 16 · TR11 18 · TR12 10 · TR13 4 · TR14 6 · TR15 3

Figure 3-22. Parity Error Schematic

# input/output system

IV

# SECTION IV
# INPUT/OUTPUT SYSTEM

## 4-1. INTRODUCTION

A review of Figure 2-1, the bus structure of the 2114A Computer, shows the overall input/output relationship. The data is outputed on the IOB lines from the R bus, and inputed to the S bus. The I/O control assembly encodes the select code information, and provides flag, control, and interrupt capabilities. The 2114A Computer provides eight I/O slots. An I/O extender option HP 2151A provides additional I/O slots maintaining interrupt priority. An I/O Multiplex option allows the availability of the Computer signals for equipment the customer may design.

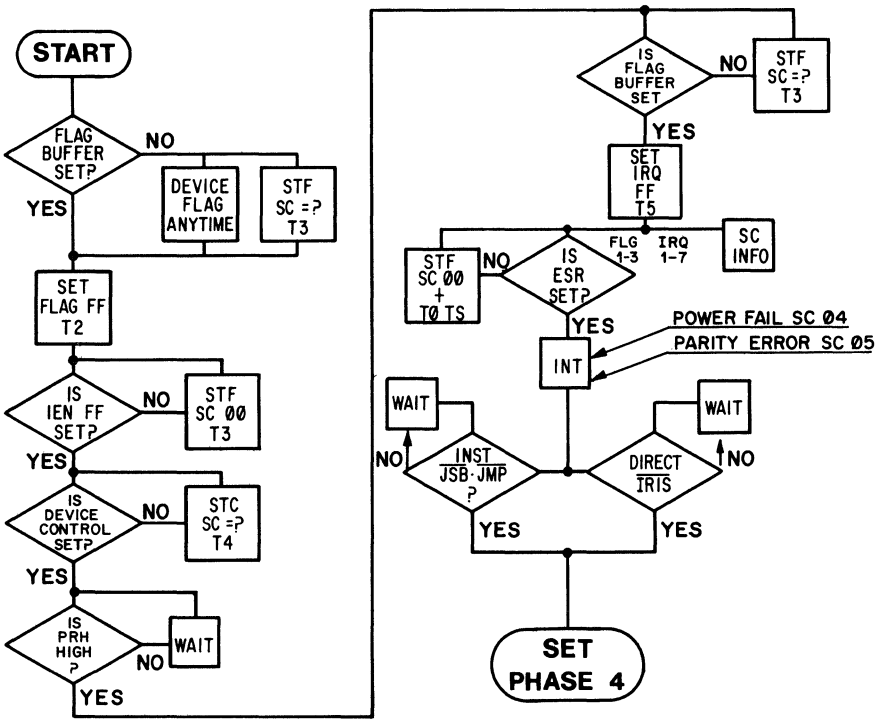



Figure 4-1. Steps to Achieve Interrupt - Phase 4

## 4-2. I/O CONTROL ASSEMBLY

The I/O Control assembly contains the circuitry for power fail interrupt, I/O device interrupt flip-flops, central interrupt address register, select code encoding, and select code output signals. The Volume 3 Input/Output System Operation Manual contains descriptions of the circuit operation for flag, control and interrupt. It also contains power requirements for I/O peripheral interfaces. It shows the signal pin assignments for the computer to interface connections, and for the I/O Control card to computer pin connections.

## 4-3. INTERRUPT PHASE 4

The Computer Phase 4 Interrupt operation provides for decrementing the P-Register, clearing the M-Register bits 6 to 15, setting the M-Register bits 0 to 5, and setting Phase 1. This forces the

next computer machine cycle to the memory address associated with the select code (called trap cell). The trap cell will normally contain a JSB which also allows the P-Register to be stored providing a return address to the computer program location prior to interrupt. Refer to Section 2-29.

## 4-4. INTERRUPT OPERATION FOLLOWING PHASE 4

A sequence of operations must follow the Interrupt Phase 4. The first machine cycle following Phase 4 is the contents of the trap cell. This instruction is normally a JSB which stores the P-Register contents allowing a return to the program in process. During time T1 the IAK signal is generated. This signal clears the interface (device) flag buffer. During T2 it clears the interface (device) IRQ flip-flop. During time T7S the Store T bus in the M-Register (bits 6 to 9) signal sets the Interrupt Inhibit flip-flop.

During the next machine cycle, which can be Phase 1, 2, or 3 the T0TS clears the Interrupt Inhibit flip-flop, and sets the Interrupt Control flip-flop. This completes the hardware routine following interrupt Phase 4. A software subroutine must clear the device flag to allow the PRL line to function. Without this operation no lower priority device can interrupt. Refer to Section 2-29.

## 4-5. CONDITIONS WHICH ALLOW PHASE 4

Figure 4-1 is a flow chart indicating the conditions which must be met to allow Phase 4 Interrupt operation. It will be noted that the Power Fail interrupt at select code 04, and the Parity Error interrupt at select code 05 can directly set Phase 4. Phase 4 operation takes precedence over all lower phase operations. Once the INT signal is generated the only conditions which will hold off Phase 4 are the coincidence of the JSB or JMP along with the indirect $\overline{\text{IR15}}$. The flow chart summarizes the control flag and interrupt conditions which are described in detail in the Computer Manual (Volume 3, Input/Output System Operation).

## 4-6. SELECT CODE GENERATION

The I/O Control assembly has the one out of ten decoders to encode the binary information in octal form. This select code octal information is available through the 86-pin connector to the backplane, and through the 48-pin connector for external use. The input TR0 to TR2 generates the least significant select code information SCL0 to SCL7. T-Register bits TR3 to TR5 generate the most significant select code bits SCM1 to SCM3.

## 4-7. CENTRAL INTERRUPT REGISTER

The interrupt request signals from the interrupting address are in octal form. The signals IRQ0 to IRQ7 are the least significant select code digits. The signals FLG1 to FLG3 are the most significant digits (and already are in binary form). These inputs are encoded into binary form. They are strobed into the Central Interrupt Register during Phase 4 operation at time T7. This Central Interrupt Register retains the select code address of the last interrupting location. This information is available to the computer via an input from select code 04, and is strobed onto the T bus bits 0 through 5.

## 4-8. I/O EXTENDER 2151A

The HP 2151A I/O Extender provides additional I/O addresses for the 2114A Computer. I/O address 17 contains the I/O Extender interface board. The interface board consists of traces to provide the necessary output signals for the extender module. Two cables are necessary, one on the I/O Control assembly, and one on the Extender Interface board. The I/O Extender picks up address 17

and adds addresses 20 to 27, and addresses 30 to 37. It retains the priority interrupt structure. The HP 2151A module is similar in design to the 2114A module, including power supply.

## 4-9. I/O MULTIPLEX

The 2114A Computer can also provide I/O Multiplex commonly called Party Line operation. The I/O Multiplex interface board can be inserted in any address slot address 10 to 17. The interrupt priority of the customer's designed system retains the priority of the address slot utilized. The multiplexed I/O Data assembly consists of buffers. The IOB input/output buses are buffered and provide OR-tying capabilities on the 48-pin connector (ground true signals). This allows data outputs to the external device, and inputs from the external device to the computer on these common buses. The computer control signals such as STC, SFS, CLF, and so on are buffered. Their outputs on the 48-pin connector are ground true. The cabling to this external I/O Multiplex device has two cable assemblies one from the Data board and one from the I/O Control board. The select code information on the I/O Control board must be ground true also.

The ground true signals from the I/O Control assembly are produced by minor modifications to the I/O Control assembly. The jumpers W1 to W11 provide positive true select code outputs and are used in the I/O Extender. For the I/O Multiplex these jumpers are physically removed. Eight additional integrated circuit buffers are plugged in the appropriate integrated circuit sockets. They invert the polarity of the select code lines providing ground true signals. It is necessary to remove the jumpers to prevent coupling between these signals which would be detrimental to rise time. Refer to Figure 4-5 for the Data schematic.

## 4-10. POWER FAILURE - AUTOMATIC RESTART

The Power Failure circuit with automatic restart provides an interrupt to select code 04. The trap cell 04 should contain either a halt, or the JSB to subroutine which services this power failure interrupt. The components associated with this power failure circuit provide the PON (Power Turn On) signal to the Computer, and the necessary control, flag, and IRQ flip-flops associated with the interrupt.

## 4-11. POWER FAILURE HALT

When the Power Failure Interrupt option is not provided, the power failure indication (PWF) from the power supply or the external power fail (XPF) from the external device provides a hardware halt through $\overline{\text{PEH}}$ bus. Both of these signals are ground true.

## 4-12. POWER ON CIRCUIT (PON)

The Power On circuit provides a turn on procedure insuring that the +5 volt computer power supply is high enough. During power failure it provides a timed delay power down condition. Refer to Figure 4-2. When PWF signal indicates the computer power is on transistor Q2 conducts. The input voltage to MC43C is low holding off transistor Q3. The collector of transistor Q3 is pulled high by zener diode CR1 to the +5 volt bus. The base of transistor Q4 is pulled up saturating Q4. Q5 is nonconducting, providing a high base signal to transistor Q6. This provides the computer power on signal (PON).

The purpose of zener diode CR1 is to ensure that the PON signal is not present unless the voltage on the +5 volt bus exceeds approximately +4.7 volts.

When PWF signal goes low, indicating power failure, transistor Q2 is nonconducting. The collector of Q2 allows a charge path for capacitor C52. The positive voltage on C52 changes the state of MC43C, resulting in the PON signal going toward ground. The time constant through resistor R32 and R33 into C52 is approximately 4 milliseconds. The sales specification is 1.5 milliseconds minimum. This provides a guaranteed minimum time for the computer to operate after power failure has been detected with guaranteed proper computer operation.

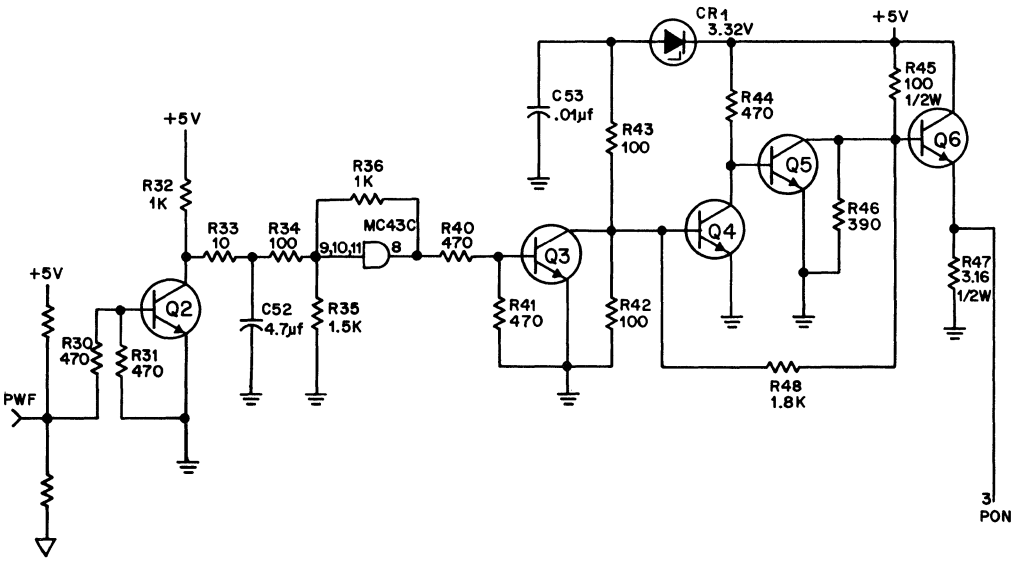



Figure 4-2. PON Circuit

## 4-13. POWER DOWN OPERATION SEQUENCE

During power turn on the power fail circuitry undergoes certain prescribed changes. (Refer to Figure 4-3.) After the initial request for Power Fail interrupt has been processed the Power Fail circuitry sits in a ready condition. That condition is as follows: The ARM flip-flop and Direction fli-flop are both set. The PWF signal from the power supply along with timing clock signals ensures the condition of these two flip-flops. The D input to the Flag flip-flop is high. Power failure will initiate a clock signal to the Flag flip-flop which will set the Flag flip-flop and the IRQ flip-flop resulting in the interrupt request. The Control flip-flop prevents subsequent power failure interrupts until cleared under program control. The status of the Direction flip-flop can be interrogated to determine whether computer power is coming up or going down.

The power failure sequence is as follows. The PWF signal goes negative indicating the sensing of failure on the AC line supply. This lowers the D input to ARM flip-flop. At time T1 the clock signal clears ARM flip-flop. The high output from ARM flip-flop pin 6 is NANDed with the set output pin 9 of the Direction flip-flop. These two signals lower the clock signal to the Flag flip-flop. At time T2 the clock signal to Direction flip-flop goes positive strobing the low input into Direction flip-flop. Conditions on MC33C are now such that the clock signal to Flag flip-flop goes positive. This sets the Flag flip-flop, and brings output pin 5 high. The Service Interrupt Request at time T5 sets the IRQ flip-flop. The output of the IRQ flip-flop requests an interrupt to select code 4, which

forces interrupt operation Phase 4. The setting of Flag flip-flop clears the Control flip-flop preventing another power fail interrupt until the Control flip-flop is serviced under program control. The interrupt to trap cell 4 performs a JSB to the service subroutine (which will be discussed in Paragraph 4-15), or a halt.

4-14. INITIAL POWER ON

On initial power turn on the low PON signal directly clears the ARM flip-flop, Direction flip-flop, and Flag flip-flop. The low PON signal in conjunction with the high clear output from Flag flip-flop sets the Control flip-flop and establishes the high PRL4 signal. The high input to the IRQ flip-flop pin 9 allows the ENF signal (T2) to clear the IRQ flip-flop.

After 0.3 seconds the PWF signal goes positive. Then the PON signal goes positive. This allows the power failure circuitry to function. The time T1 signal NANDed with PRL4 clocks the ARM flip-flop setting it. This provides the proper signals to MC33B to lower the clock input to Flag flip-flop. At the end of time T1 the high D input to Direction flip-flop is clocked in. The conditions on MC33B force the positive clock signal to Flag flip-flop, setting it. The following time T5 signal sets the IRQ flip-flop. The IRQ flip-flop forces select code 04, and INT signal.

The three inputs to gate MC16A are positive. The Direction flip-flop is high indicating power is on, PON signal high indicates sufficient +5 volt bus for computer operation including adequate timing delay, and Flag flip-flop output forces the gate. This provides the $\overline{\text{RSP}}$ restart pulse which initiates computer run condition.

The initial computer operation is Phase 4 Interrupt forcing memory address 4. The next operation performs the contents of memory address 04, which will normally be a JSB to the subroutine, or a halt signal.

The high IRQ flip-flop output clears the Flag flip-flop. Enable flag ENF at time T2 clears the IRQ flip-flop. The Control flip-flop must be cleared under program control. The completion of these operations leaves the computer in steady state run condition.

4-15. SERVICE SUBROUTINE

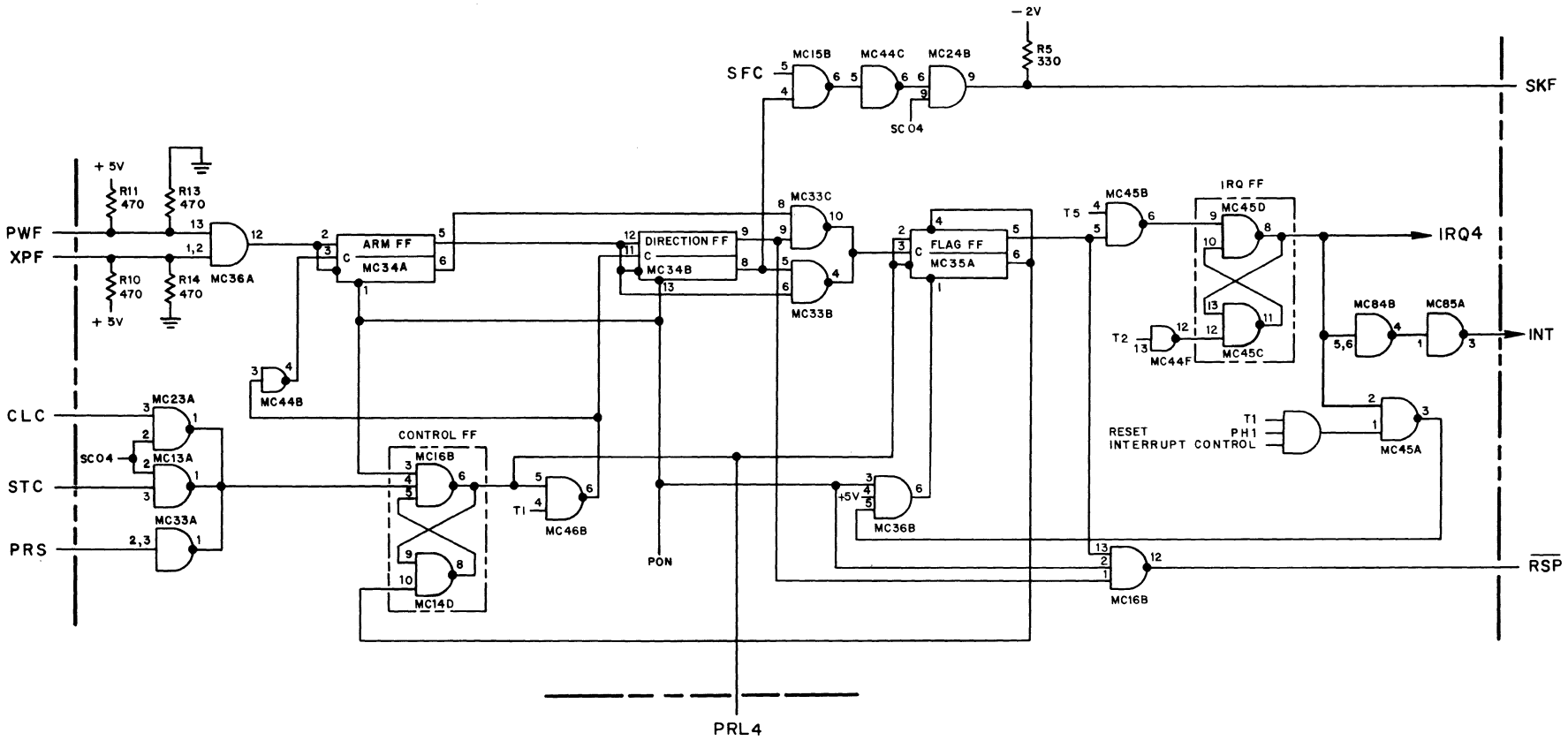
(This program is prepared by the customer, and is not supplied by HP). The power fail subroutine normally includes a test to determine whether power is coming up or failing. For power failure the subroutine will provide instructions to save the state of the interrupt system, A, B, E, O, and Switch registers. If required it will also provide saving the status of the output register such as general purpose registers, relay registers, and so on. Where motor control or process control is included it should also perform the orderly shutdown on these process control functions.

The power on subroutine should provide turn on procedures for process control. It should re-establish proper output conditions on general purpose registers, relay registers, and so on. It should restore the status of the interrupt system, A, B, E, O, and Switch registers. The final instruction prior to the JSB through the stored address will be to set the Control flip-flop. This will allow another power failure interrupt.

The worst case condition will be on initial computer power turn on. After the interrupt request the re-establishment and initialization of all registers and functions is performed. If power failure has occurred during this time an interrupt is generated which interrupts immediately following the JSB indirect instruction. The service routine for power failure must then be performed prior to

actual computer failure. This worst case condition requires that both store, and restore programs be completed within the 1.5 millisecond specification.

Hewlett-Packard diagnostic tests normally will not include either the Power Fail service routine, or the halt in location 4. It is very useful when servicing a computer to ensure the halt is in location 04.




**SIMPLIFIED POWER FAIL INTERRUPT CIRCUIT**

FIG. 4-3

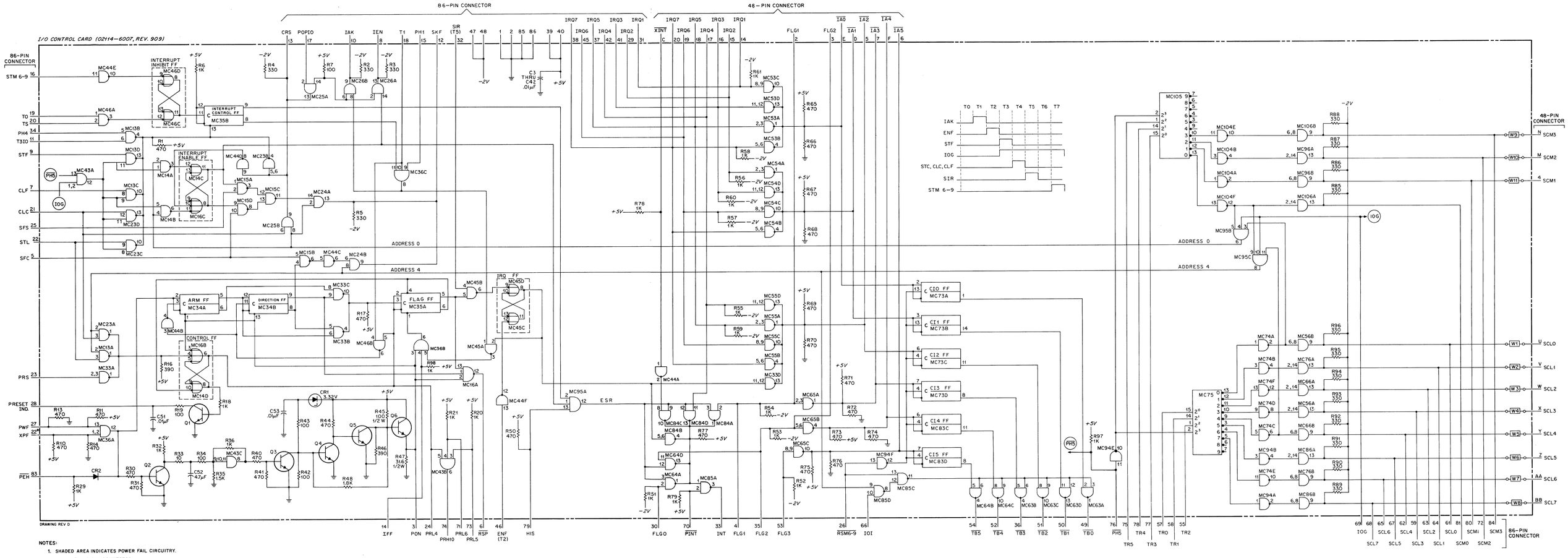



Figure 4-4. Logic I/O Control

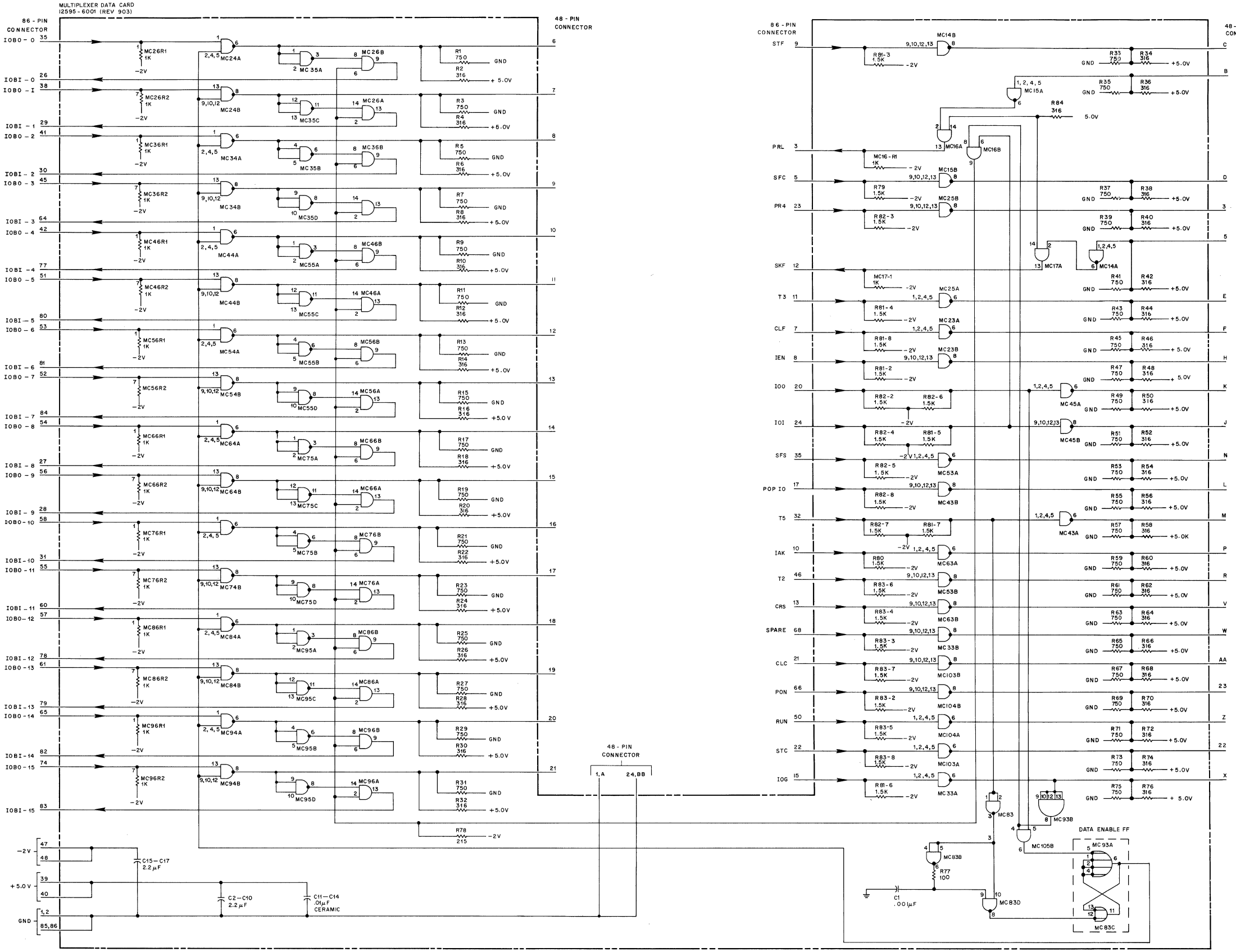



Figure 4-5. I/O Multiplex Data

# power supply

V

# SECTION V
# POWER SUPPLY

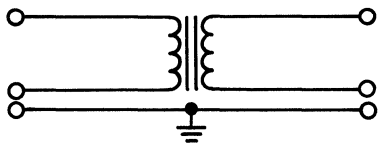
## 5-1. INTRODUCTION

The design and construction of this power supply presents a hazard to personnel and equipment. Section 5-5 on Safety Precautions should be carefully read prior to attempting instrument service.

## 5-2. EQUIPMENT FOR MAINTENANCE

1. Isolation Transformer
   115V:115V 800 volt-amp capacity
   (For 60 Hz operation only, 550 volt-amp will be adequate)

To 115 AC, 50/60 Hz
Grounded
Duplex
Receptacle



To Computer
115V Secondary

PAECO No. 6-4949

2. Variable AC Autotransformer 50/60 Hz, 7 amp.

3. Oscilloscope HP 180A or equivalent.
   HP 1801A Vert Amplifier
   HP 1720A Time Base
   HP 10004A Probes

4. Multimeter HP 427A
   For +20V bus improved accuracy is desired such as HP 412A or HP 3430A.

## 5-3. INTRODUCTION

The 2114A power supply is a 50-60 Hz, 115 volt AC input only. A step down transformer is required for operation from a 230 volt line. It is a dissipative type power supply. Any line voltage in excess of the minimum required is dissipated in the form of heat. This heat is dissipated primarily by those components situated on the heat sink.

The power supply consists of four basic sections:

1. The primary regulator establishes an input voltage of 85 volts to the primary of this transformer (T1).

2. The DC voltage buses are simple full wave rectifier, capacitor filter buses, and depend on the transformer turns ratio to determine the actual voltage.

3. The 20 volt regulator is a stable regulator with temperature compensation for the memory circuits.

4. A power fail circuit senses power failure and also provides a turn-on delay.

The purpose of this lesson on the power supply will be to study the circuits and gain a familiarity with how they operate. It will discuss the safety supply. A laboratory session will deal with wave shapes, troubleshooting and actual fault analysis.

## 5-4. PHYSICAL CONSTRUCTION

The physical parts of the power supply assembly consists of the rear panel of the instrument which houses the line filter, the fans and the voltage bus test points. The heat sink assembly contains those elements which dissipate significant amounts of power. The transformer, capacitor board and the capacitor assembly are mounted to the deck. The regulator board is a plug-in board and containing the small components associated with the primary regulator, 20 volt regulator, and power fail detect circuitry. The outputs of the power supply are the voltage buses with wiring attached to the computer back plane. All cabling associated with the primary regulator and AC line is physically separated from the DC voltage bus cabling. This is a safety precaution for personnel.

## 5-5. SAFETY PRECAUTIONS

There are safety hazards associated with troubleshooting and maintaining this power supply which differs from typical power supplies. The primary regulator determines the AC level to the primary winding on the transformer. All of the circuitry associated with the AC line thus is hot (i. e., connected electrically to the AC line). The series regulators, the regulator board, and the voltage and overload current protection circuits are all superimposed on the AC line voltage. Utmost care must be used in troubleshooting. Fault analysis and repair should not be performed without using an isolation transformer which allows this primary regulator circuit to float. Thus any single point can be grounded and become a reference node. Without this isolator transformer it is extremely difficult to troubleshoot this power supply.

Periodic inspection of the insulation of the cabling, especially following the replacement of components will establish that the insulation is still intact. Faulty insulation may result in serious danger to personnel, and to equipment. The routing of the cables must not be disturbed which may lead to contact between AC regulator circuitry and DC buses.

## 5-6. CIRCUIT DESCRIPTION

## 5-7. PRIMARY REGULATOR

Figure 5-1, the block diagram of the Line Regulator shows the 115 volt AC line supplying the transformer T1 winding and the series regulator circuitry. The winding design voltage is 83V AC. The series regulators absorb the excess voltage. Because it is not convenient to work with AC voltage

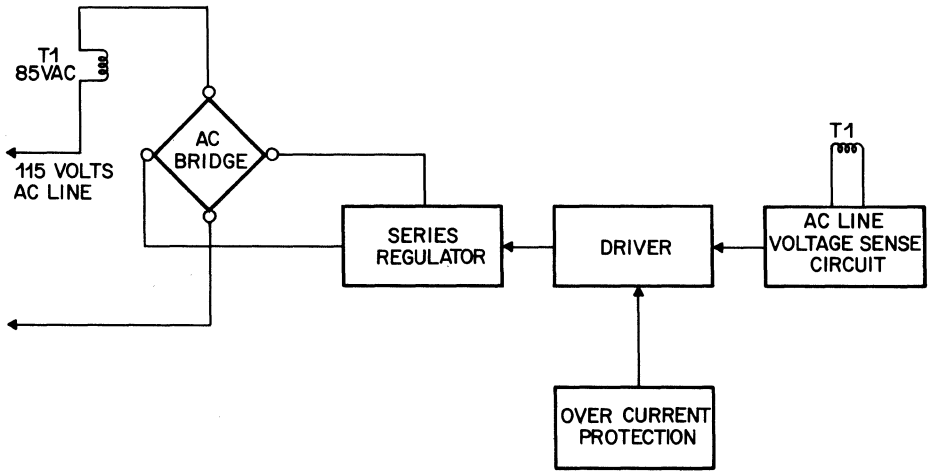



Figure 5-1. Line Regulator Block Diagram

in semi-conductor circuits a full wave bridge converts to pulsating DC. This allows the series regulators to be DC circuits instead of bi-polar.

The series regulators require a driver for current amplification. The driver is controlled by two circuits: The AC line voltage circuit which establishes the 83 volts on the primary of the transformer, and the over-current protection circuit which prevents short circuits or other malfunctions from drawing excessive current through the series regulators.

5-8. The AC bridge is a normal full wave diode bridge. We see that the series regulators are four transistors in parallel with current balancing resistors in the emitter circuit. A Driver transistor Q5 provides base current to the four series regulators. This driver transistor is controlled by two circuits: The AC voltage sense circuit, and the over current protection circuit.

5-9. AC VOLTAGE SENSE

The AC voltage sense circuit has a separate transformer winding with full wave rectification. The instantaneous voltage is applied to transistor Q7. When the voltage exceeds the zener breakdown voltage of diodes CR45 and CR46 transistor Q7 conducts. The collector voltage drops, reducing the drive to the Q5, which allows the series elements to bear the voltage in excess of the 83 volt requirement. Before the AC line voltage is high enough to cause diodes CR45 and CR46 to conduct the base of Q5 is pulled up by resistor R24. This 10,000 ohm resistor insures that the driver is initially turned on and the four series elements are saturated thus supplying full line voltage to the transformer primary. It must be pointed out that this is not an average DC type circuit. It is an instantaneous AC circuit. Thus it is not possible to troubleshoot this circuit using a voltmeter. You must use an oscilloscope to observe instantaneous waveshapes.

5-10. OVERCURRENT PROTECTION

The operation of the overcurrent protection circuit is as follows: All of the line current must flow through resistor R15. When the voltage drop across R15 increases sufficiently, transistor Q6 is turned on and the collector voltage drop reduces the base drive to Q5 so as to limit current at this level. It requires approximately 10 amps peak (4.1 RMS)to initiate this overcurrent action. Resistor R22 provides base current to Q6 depending on the AC line voltage. This reduces somewhat the critical current through R15 at elevated line voltages, and helps limit the peak dissipation of the regulators.

5-11. THERMAL SWITCHES

It will be noted that the base of transistor Q5 has two thermal switches between the driver and the voltage sense and overcurrent circuits. One of these thermal switches S302 is set for 75° centigrade operation and is physically located on the heat sink assembly. Thermal switch S301 is set to operate at 43° centigrade and is located in the air stream as it enters the computer. If either one of these switches opens, transistor Q5 does not drive the series elements thus preventing computer TURN ON.

5-12. HEAT DISSIPATION

It is important that the filters on the fan assemblies be checked and cleaned as necessary at frequent intervals.

At high line and maximum current each transistor must dissipate over 100 watts peak. To accomplish this, these transistors are mounted individually on each of the four vanes on the heat

sink assembly. In addition to the four series regulators, the Q5 driver transistor, two regulators in the 20 volt circuit, and the 4 diodes in the AC bridge are also located on the heat sink assembly. It is not wise to leave the computer in the overload current mode for extended periods of time.

5-13. TRANSISTOR INSULATORS

Care must be exercised in working around the Heat Sink assembly. The mica insulators for Q1 to Q5 are special insulators of larger physical size (HP 0340-0458). The high voltage noise spikes that may be on the AC line require insulators which will safely handle 1000 to 1500 volts. The mica protrudes over the edge of the heat sink. The mica edge must not be cracked, bent, or broken.

A thin uniform layer of silicon grease must be used on both surfaces of the insulator to insure adequate thermal conductivity.

When replacing the diodes do not allow them to rotate. Rotation will score and damage the mica insulators.

A varistar RV1 protects against high voltage noise spikes. At voltages in excess of 140V RMS the varistor breaks down, providing a low impedance to noise spikes.

5-14. PRIMARY REGULATOR - TROUBLESHOOTING

5-15. ISOLATION TRANSFORMER

It is necessary in troubleshooting the primary regulator that this circuit be isolated from the AC line. This is accomplished by using an isolation transformer. The isolation transformer should have a one to one ratio and be capable of handling 600 to 800 volt-amps. Such a large capacity is necessary because of the large peak to average currents in this supply. A transformer and variable AC autotransformer with less capacity may cause poor operation.

5-16. REGULATOR AND DRIVER SHORTS

A convenient troubleshooting aid is to remove the primary regulator board. When this board is removed Q5 does not provide drive current and the line regulators remain off. There will be some voltage applied to the primary of the transformer because of the current path through resistor R2 (250 ohms). This provides sufficient primary current so that there will be 1.5 or 2 volts present on the 5 volt bus and proportional amounts on the other voltage buses.

5-17. There should be no current through the series elements Q1 to Q4. This can be determined by measuring the voltage drop across emitter resistors R10, 11, 12, and 13. (These are physically located on the Kingman board to the rear of the heat sink assembly).

5-18. REGULATOR AND DRIVER OPEN CIRCUIT

Operation of the Regulator transistors can be checked without the regulator board by providing base drive. Use the isolation transformer and variable AC autotransformer in the line. Start with the AC autotransformer turned all the way down. Turn on Driver Q5 by connecting its base (+ terminal of C10 on Kingman Board) to the collector of Q1 or Q2 (on top side of heat sink) through a 1K resistor (1/4W ok). Use common node of R10-R15 for scope ground.

WARNING

This provides full line voltage to T1 primary. The line voltage should not exceed 85 to 90 volts. Now it is nece-

sary to protect the power supply manually. You no longer have voltage or overcurrent protection. This requires that the input AC line slowly be increased with the variable AC autotransformer while carefully monitoring both voltage and current of the line. This procedure will establish that the regulators, driver, and AC bridge are capable of proper operation.

Operation of the 5V bus should be an adequate indication. The above procedure will provide 5 volts DC with 0.3V P to P ripple at 85V AC Line.

5-19. WAVESHAPES

With the regulator board installed viewing waveshapes in the AC voltage sense and overcurrent circuits is a powerful troubleshooting aid. Specific changes take place as a function of line voltage. Use variable AC autotransformer and isolation transformers.

The regulator voltage (collector Q1 to R15) will have spikes as the AC line crosses zero voltage. They are cuased by the transformer flux decay as the diode bridge ceases to conduct. The voltage level is stable and they repeat each 8.3 millisecond. As the voltage is increased to 85V the regulators will begin to show a voltage peak. This collector voltage increases to 60V peak-to-peak at high line.

The collector waveshape of Q7 increases until at 85V line voltage it developes a dip. (Refer to Figure 5-2.) The increased base drive to Q7 (with increasing line voltage) results in the collector dropping to a level which maintains the 85V input to T1.

5-20. NONREGULATED BUSES

The voltage buses of the power supply are brute force (no voltage control or current limit), full wave rectifier, capacitor input lines. All circuits have fuse protection with the exeption of the 5 volt bus. The high current protection of the 5 volt bus is provided by the primary regulator overcurrent protection. The actual DC voltage of these buses is established by the turns ratio of the transformer windings. Proper adjustment of the line regulator establishes the 5 volt bus. The other buses fall where they will.

5-21. An important troubleshooting aid on these voltage buses is the DC voltage as well as the AC ripple on each bus. It will be noted that each large capacitor has a protection diode across it which reduces the danger due to inadvertent reverse voltage connection. The plus 30 volt lamp supply is independent of the normal 30 volt supply. Its filtering requirements are minimal so the acceptable ripple is substantially higher. Otherwise, the supplies are similar. Refer to Table 5-1 for normal operating voltage levels.

5-22. TROUBLESHOOTING

It is imperative that the high current carrying lines have good connections because of the extremely high peak currents. All of the mechanical connections in the 5V bus must be checked to determine that they make good contact. A poor connection in the 5 volt circuit compensated by raising the input regulator obviously will make all other voltage buses excessive. If error or fault occurs in only one or two of these nonregulated voltage buses the chances are good that it will be

associated either with the rectifiers or transformer windings. Check that the diodes are installed and operating correctly and that the transformer center tap and voltage windings are properly connected.

Table 5-1. Computer Voltage Bus

| VOLTAGE BUS | MAXIMUM * | MINIMUM ** | AC RIPPLE PEAK-TO-PEAK |
|---|---|---|---|
| + 5V | 5.5V | 4.3V | 0.5V |
| +12V | 13.0V | 11.8V | 0.3V |
| -12V | -13.0V | -11.9V | 0.3V |
| - 2V | - 2.8V | - 1.9V | 0.4V |
| +30V | 32.0V | 29.0V | 0.5V |
| +30V Lamp | 32.5V | 28.0V | 3.0V |
| +20V | 20.1V | 19.9V | 0.01V |

* High AC Line, minimum computer load.
** Low AC Line, maximum computer load.

5-23 60 CYCLE RIPPLE

If analysis of all voltage buses indicates the presence of 60 cycle ripple rather than 120 cycle ripple it may indicate that one of the diodes in the AC diode bridge or that one of the diodes or transformer windings in the voltage sense circuit is open so that voltage regulation is accomplished each half cycle.

5-24. FUSES

It will be noted that the fuses are connected between the rectifier and capacitor in some cases. This means the fuses are subjected to RMS currents which are higher than the average DC output of the respective buses. This may account for fuse failure apparently below its rating. 60 cycle ripple present in one or two buses would indicate trouble in the transformer winding or rectifier associated with the specific voltage bus.

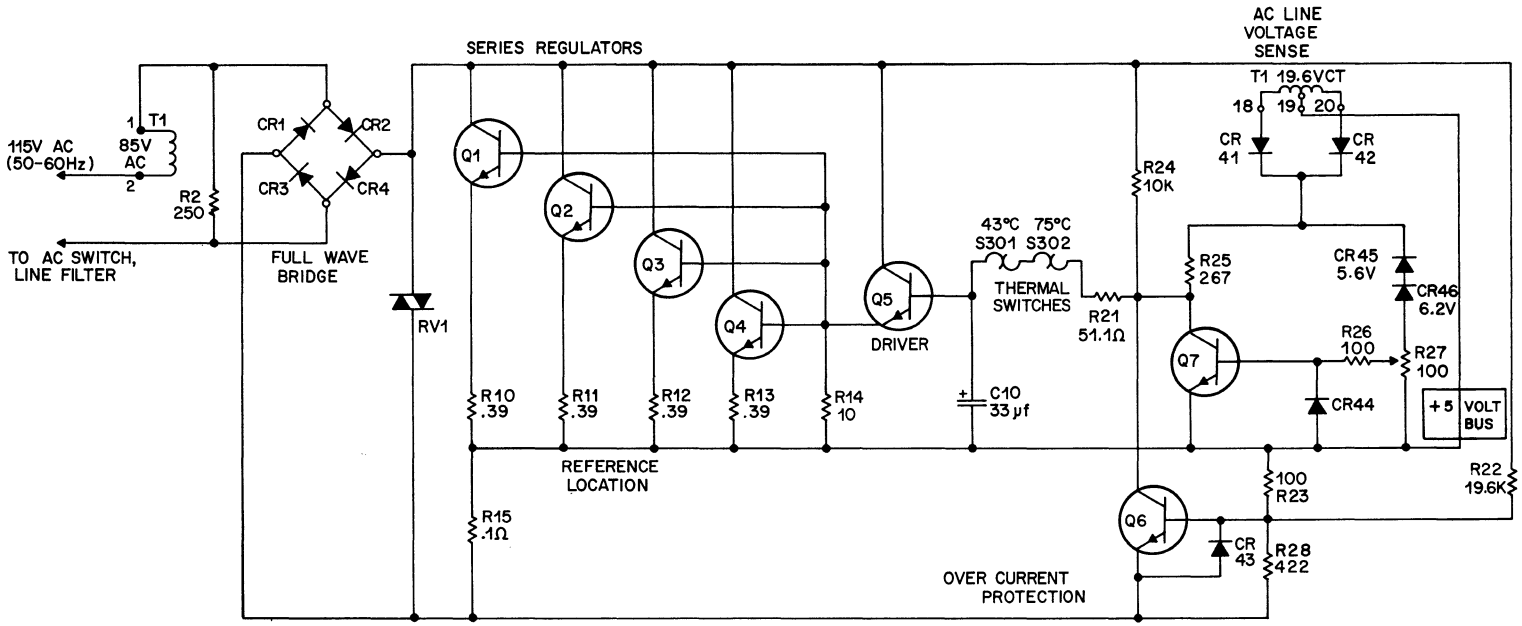
5-25. 20 VOLT REGULATOR

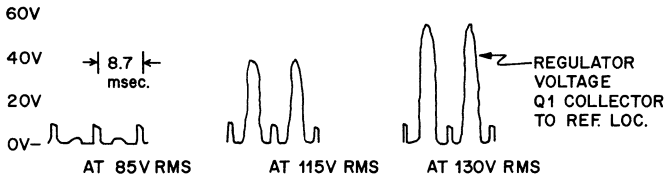
A glance at the block diagram (Figure 5-3) shows that this 20 volt regulator consists of series regulating elements with an appropriate driver, a complex integrated circuit, and the voltage adjustment potentiometer with several temperature compensation resistors. The sophisticated IC reduces the number of discrete components that are required.

5-26. CURRENT PROTECTION

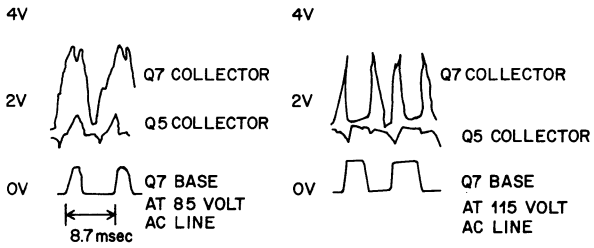
A look at the voltage overload graph shows that the output voltage is very stable up to its maximum established current - (which in this case is about 3.5 amps). Above this level any further attempt to increase the current reduces the current delivering capability. This current fold back characteristic affords protection by reducing worse case dissipation.

Standard circuit operation delivers about 2.5 amps continuously. It is not necessary to measure the overload curve unless circuit failure has damaged components. To spot check the short current operation short out the 20 volt bus before power is applied to the computer. Then bring up AC voltage slowly. The regulator shall stay in the reduced current mode drawing about 0.8 amp with negligible output voltage.




REGULATOR VOLTAGE FUNCTION OF AC LINE




AC LINE VOLTAGE SENSE FUNCTION OF AC LINE

## LINE REGULATOR

FIG. 5-2

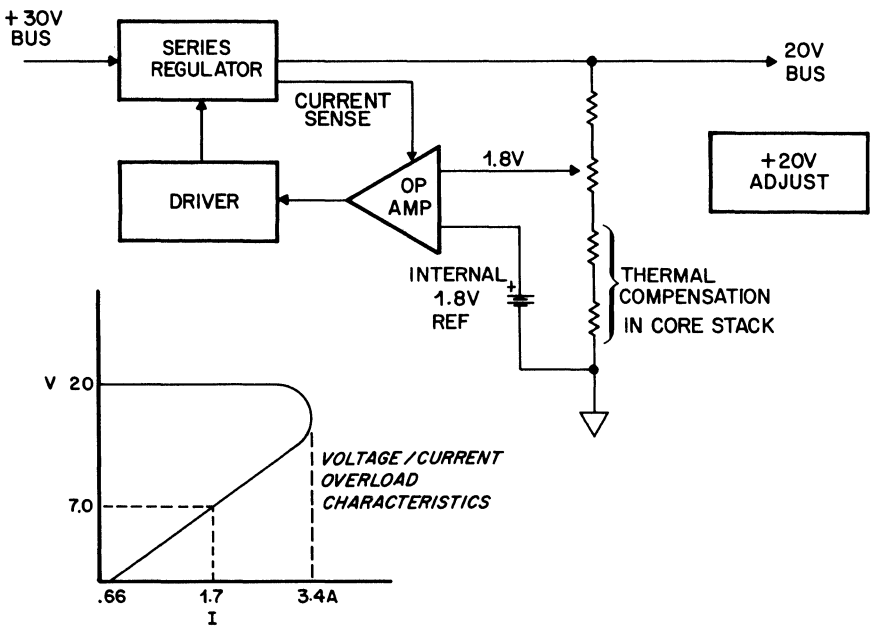



Figure 5-3. 20 Volt Regulator Block Diagram

5-27. 20 VOLT REGULATOR ADJUSTMENT

The proper DC level is 18.75V at 20° ±2°C. The adjustment for other temperatures is 18.75 + [-0.088 (Ambient Temp -25°C)] V. (For example, at 35°C set to 17.87V).

5-28. The 30 Volt bus (consisting of a full wave rectifier and capacitor filter) is the unregulated power input. The series regulators are transistors Q10 and Q11. These transistors must be able to dissipate the power required at 2-1/2 amps. These transistors are located on the upper rear of the heat sink. The two emitter resistors R16, 17 are located directly behind on the left end of the Kingman card assembly. The bases are driven by the driver transistor Q12 located on the 2114-6010 Regulator assembly. Q12 gets its drive from the IC pin 2 booster output.

5-29. REGULATOR BALANCE

The 20 volt output bus is connected to pin 8. Output current goes through the series elements and the emitter resistors. The emitter resistors provide current balancing so that each transistor dissipates approximately half the load. If either of the transistors is destroyed or becomes inoperative the other is apt to become destroyed also. Check to insure both transistors are conducting. This can be done by measuring the voltage drop across the two emitter resistors.

5-30. The other inputs include: pin 4 ground, pin 3 unregulated input voltage, pin 5 by-pass for internal circuitry, pin 6 is the feedback point for voltage control, pin 7 allows frequency compensation to prevent oscillation.

Pin 6 is a voltage feedback node and compares the circuit voltage with an internal reference. The resistor string consists of R35, R36, R27 and the two temperature compensating resistors which are physically located in the core stack. The normal DC operating level for Pin 6 is about 1.8 volts.

Pin 1 senses the current being drawn through the regulating circuit and allows the overload

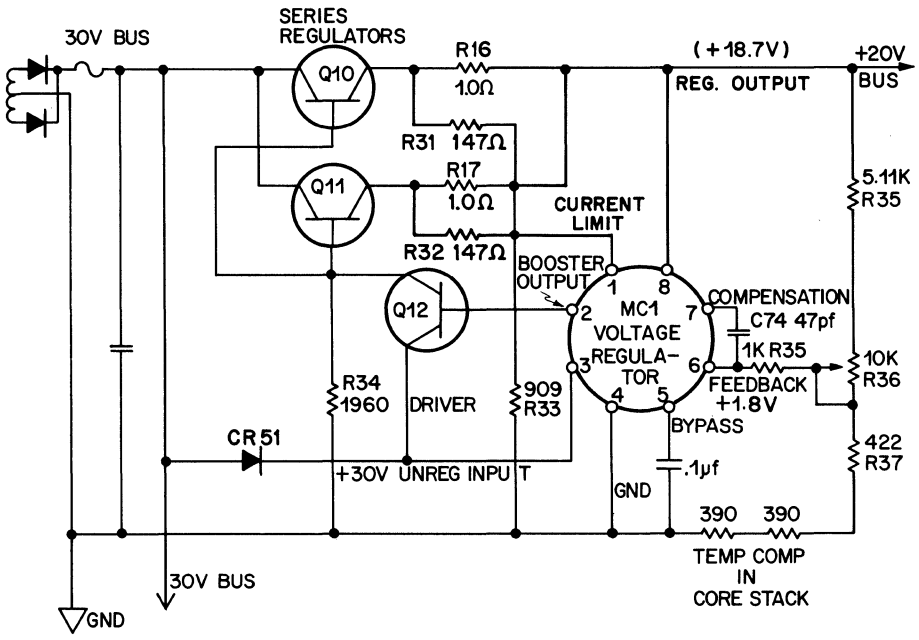



Figure 5-4. 20 Volt Regulator

characteristic for protection of the series elements. When the voltage between pins 1 and 8 exceeds about 1.5 volts it reduces the current pin 2 can provide.

5-31. 20 VOLT REGULATED BUS - TROUBLESHOOTING

An analysis of the DC levels is the most expiditious way to troubleshoot the circuit. Check first that the 30 volt unregulated bus is normal. The input voltage level to pin 6 integrated circuit the feedback point should be approximately 1.8 volts when it is operating. As the 20 volt adjustment is made with potentiometer R36 the voltage change at pin 6 is negligible. The adjustment range of this circuit is from 16 volts to 24 volts.

The voltage relationship of pins 2 and 3 are stable regardless of actual adjustment of the 20 volt bus. Pin 3 is approximately 0.7V below the 30 volt unregulated bus. Pin 2 is about 0.7V below pin 3. Pin 1 to Pin 8 voltage is a measure of the current being supplied by the regulator (voltage drop on emitter resistors of the regulators). When pin 1 exceeds pin 8 by 0.7 volts the booster output of pin 2 is reduced and the regulator enters the current fold back protection mode.

5-32. TEMPERATURE COMPENSATION

The temperature compensating resistors are located in the core stack. An allowance should be made of approximately 88 millivolts/degree C for voltage adjustment at temperatures other than 23-27°C (72-80°F) ambient. The voltage bus should be decreased by 88 millivolts per degree C. A decrease in temperature below normal ambient will require a voltage increase of 88mv/°C.

5-33. COMPENSATION RESISTORS

The only check of the temperature compensating resistors is a simple resistance measurement. A value of 675 to 900 ohms is an acceptable value. The component has a +7400 PPM/°C temperature coefficient. In case of component failure the computer can be brought up by substituting the closest resistor value available. Run Memory Checkerboard Program while slowly increasing voltage and note voltage at failure. Then restart test and decrease voltage to failure point. Set voltage at the middle

of the range. This will result in a reduced temperature operating range, but will suffice until the correct replacement can be obtained and installed.

The TC resistors are vendor supplied, and are not available through Hewlett-Packard. They are Texas Instruments sensistor TM 1/8W, 390 ohm ± 10%, +0.7% per °C. The closest substitute available through HP stock is 0811-2031 815 ohm, +5900 PPM/oc. Mount substitute on feedthrough insulators on memory bracket.

## 5-34. POWER FAIL DETECT CIRCUIT

The purpose of this power fail detect circuit is to allow orderly turn on of power in the computer, and in case of power failure to allow proper turn off. A view of the block diagram indicates an AC detector which senses the voltage from the transformer winding. It utilizes the plus and minus 12 volt transformer windings although it is independent of the actual voltage buses. The circuit consists of an AC detector with a turn off delay, the threshold detector zener diode, the pulse shaping gates, and an effective AND gate with the 5 volt bus (Q24), a DC section with a turn-on delay network followed by a pulse shaping network.

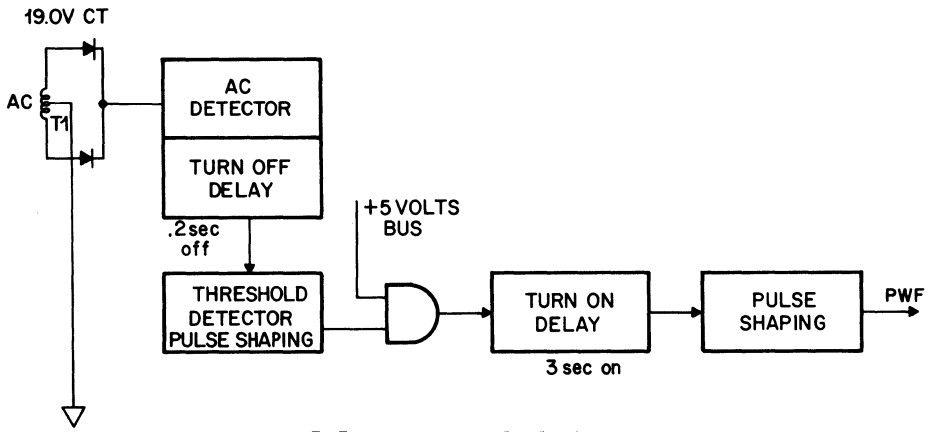



Figure 5-5. Power Fail Block Diagram

## 5-35. AC INPUT

As the AC power comes up the full wave rectifiers CR52 and 53 develop the voltage on C72. When the voltage has built up on this capacitor sufficiently high the zener diode CR54 begins to conduct at 6.2 volts and pulls up the input to the NAND gate MC2C. This voltage is pulled up through the forward biased diode CR55. The time constant of the RC network is approximately 20 milliseconds. Diodes CR55 and CR56 provide a hysteresis voltage level to the NAND gate inputs so that even if the voltage is somewhat near the turn on-turn off point for the NAND gates the output will not stutter. This provides an approximate 1.4 volt hysteresis range so that the operation will be stable even with minor variations in AC line.

## 5-36. TURN ON OPERATION

Now, let us follow the normal sequence as the AC power comes up. The voltage builds up on C72 until the voltage exceeds the level of CR54. The voltage on the input gate MC2C rises until it switches the NAND gate MC2C. The output of the first section goes down so the output of the second section comes up. Resistors R45 and R43 provide a feedback network for speed up, and hold on purposes.

The true output from MC2D saturates Q23 and holds off Q24.

5-37. TURN ON DELAY

The collector of Q24 goes high allowing C75 to charge up toward the +5V bus. The charging path is through R47 and R48. The time constant is about 300 milliseconds. When this voltage exceeds the threshold level on MC2B pin 5, MC2A and 2B switch providing a PWF high level output. The output of MC2D pin 8 is high and enables MC2B pin 4. R51 is a speed up resistor for pulse shaping.

5-38. TURN OFF MODE

When power failure reduces the AC line voltage the DC level on C72 discharges toward ground through R41 and R42. The time constant is about 20 milliseconds. Diode CR56 pulls the input to MC2C down until it falls below the turn on threshold. The output of MC2D drops disabling MC2B pin 4 which changes PWF to its negative true state.

Q24 turns on providing a discharge path for C75 to re-establish proper turn on time constant.

5-39. TROUBLESHOOTING

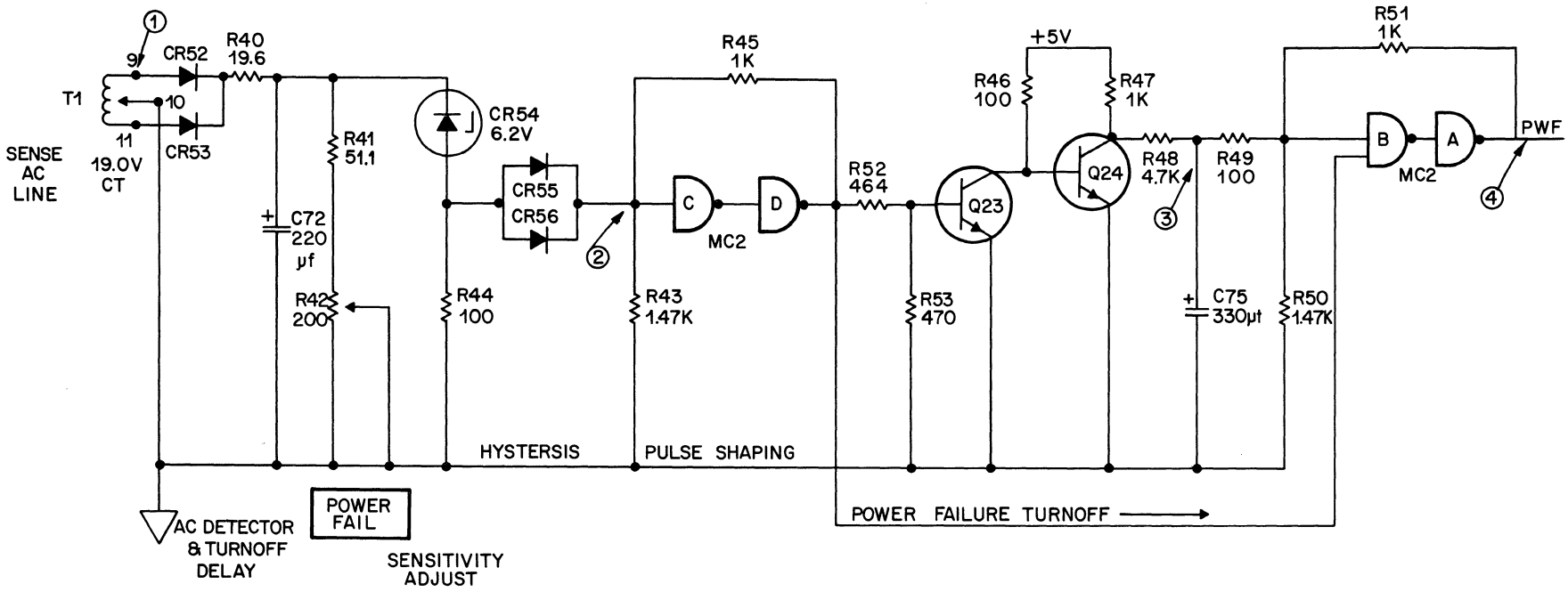
A variable AC autotransformer on the computer AC line provides the best method for trouble-shooting the circuit. The voltage on C72 will vary between approximately 7.7 to 8.3 volts DC (from 98 to 130 VAC line). The AC ripple will be 120 CPS with a 1.4V P.P. amplitude.

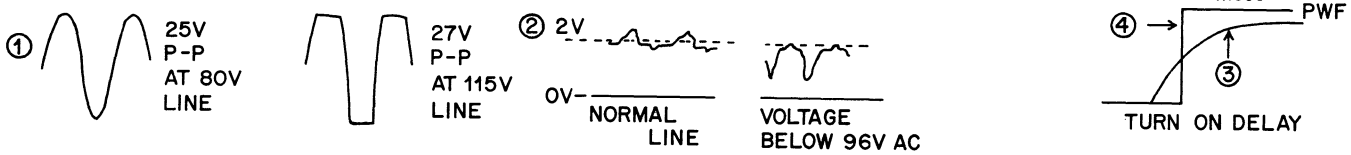
5-40. The input to MC2C will be 1.9 volts DC nominal. The AC waveshape at MC2C pin 12 will have a positive hump and a negative dip as CR55 and CR56 conduct. The relative size of the two will depend on the AC line voltage. When R42 is adjusted correctly the negative dip enlarges as the line voltage drops toward 98 VAC. At 98 to 100 VAC (96V minimum) the waveshape changes suddenly indicating that the states of MC2C and D have changed. (Refer to Figure 5-6.) At this point the PWF output will go low initiating the power failure sequence.

5-41. TURN ON DELAY

The delay function during turn on can be checked in a rough way by observing the waveshape on C75 and the PWF output simultaneously. Set horizontal sweep to 100 msec/div, sync on AC line. Turn on the computer AC switch when the trace just begins a new sweep. The waveshapes can be seen after a couple of attempts. Leave switch off for a few seconds to insure all voltage buses have discharged fully before repeating. A delay of 300 to 500 milliseconds is typical (including reaction time in turning on the switch).

5-42. The PWF signal to the computer allows determining the status of the AC input voltage. This allows proper turn off for power failure. When option 08 is installed the power failure option provides automatic restart when the power comes back on by interrupting to the software subroutine.




## POWER FAIL

FIG. 5-6

NOTES
1. CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED.

Figure 5-7. Logic Power Supply

# front panel

VI

# SECTION VI
# FRONT PANEL

6-1. INTRODUCTION

The Front Panel contains the various switches necessary to operate the 2114A Computer. The memory data register ("T" Register) and memory address ("M" Register) are both displayed on the front panel. The Switch Register is displayed with lamps under the actual proximity switch assembly. This permits display of the Switch Register for manual inputs, and output display under program control by outputing to select code 01.

The power switch and line fuse are accessible behind the panel. The rear of the front panel contains various switches for troubleshooting and service. The Front Panel Assembly can be locked to prevent access to the power switch or the diagnostic switches. The entire panel can be easily removed by the detachable hinges, and removal of the nut holding the ground braid.

6-2. EQUIPMENT FOR SERVICE

1. Oscilloscope HP 180A or equivalent
   Vertical amplifier HP 1801A
   Time base HP 1820A
   Probes HP 10004A
2. Voltmeter HP 427A
   If NULL adjustment is attempted with a digital voltmeter an HP 3430A or HP 2401A/2A is required.
3. Insulated tuning screwdriver for NULL adjustment.

6-3. ACCESS FOR SERVICE

The front panel can be removed from the front door to make the components visible for easier identification. Care should be exercised to prevent shorting any circuit to the instrument.

6-4. MASTER OSCILLATOR

The amplitude of the frequency determining portion of the oscillator is established by the nonlinearities of the transistors Q30 and Q32, (i.e., saturation). The signal is AC coupled to the power amplifier. The power amplifier has a voltage gain of one. In the positive direction the collector voltage of Q35 is about equal to the base of Q33. The output current through R126 reduces the current flow through Q34 thus reducing current through Q36. In this manner the output stage provides a low output impedance with small steady state dissipation. The output impedance is about 25 ohms, and the load is 25 proximity switch circuits in parallel (800 ohms effective impedance).

6-5. PROXIMITY SWITCH CIRCUIT

6-6. The two inputs to the proximity switch circuit are a DC Bias voltage, and an AC sinusoidal signal. The circuit also requires the ENABLE voltage in order to operate. Each circuit provides an output to the computer backplane, and drives the relay clicker circuit.

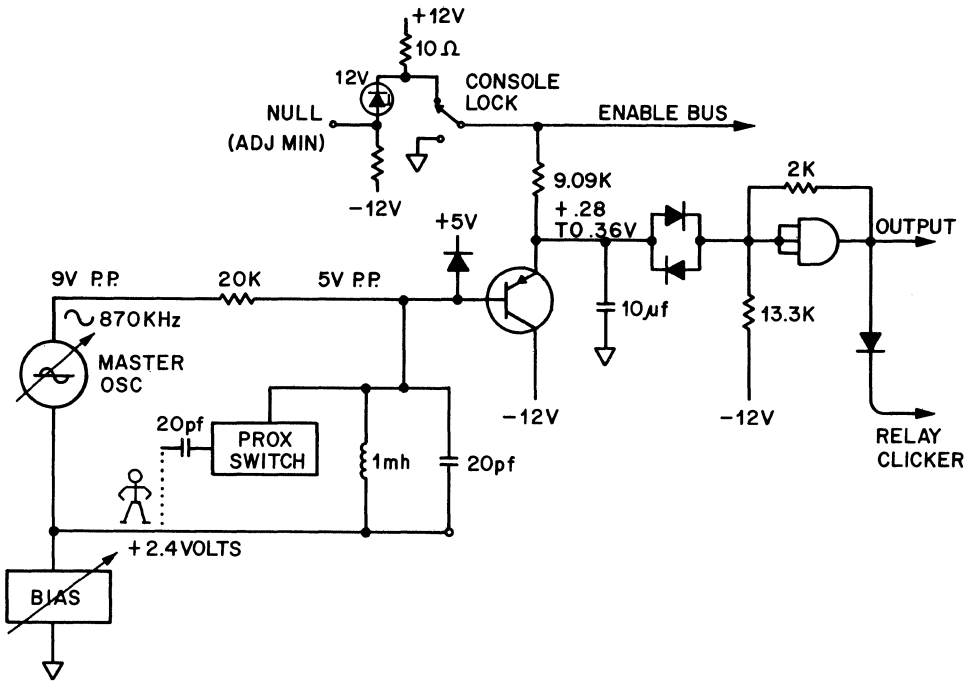



Figure 6-1. Proximity Switch Circuit

The master oscillator generates a sine wave signal. The frequency can be adjusted over the range 0.7 to 1.3 MHz by adjusting the NULL variable capacitor. This signal drives the parallel tuned circuit on the base of each emitter follower transistor. The DC return is through the inductor to the BIAS voltage bus which should be adjusted to +2.40V ±0.1 volts. The emitter capacitor charges to the negative peaks, normally +0.28 to +0.36 volts. This voltage holds the input to the AND gate in zero state.

6-7. The action of touching the proximity switch sensor is to increase the capacitance by about 20 pf in the parallel tuned circuit. This detunes the circuit resulting in a smaller signal envelope. The emitter capacitor voltage rises with the negative peaks. The diode pulls the AND gate input up until the AND gate switches to the one state. The 2K feedback resistor keeps the AND gate on until pulled down by the other diode, and also speeds up the output signal.

The AND gate switching to the one state energizes the relay clicker circuit, and provides a positive clock to the Switch Register FF on the Arithmetic Logic assembly. The diodes between the emitter capacitor and the AND gate provide a hysteresis voltage so the output will not stutter.

The diode between the base and the +5 volt bus is a clamp on the positive peak to protect the transistor and to limit the tuned circuit amplitude.

6-8. The NULL test point measures the voltage drop across the 10 ohm resistor between the ENABLE bus and the +12 volt bus (translated down by the zener diode to make measurement easier). As the master oscillator frequency is adjusted the transistor current increases to its maximum value (minimum voltage) at the average parallel resonance of the base circuits. This indication is subtle and must be observed carefully.

The ENABLE bus can be disabled by using the CONSOLE LOCK switch on the front panel assembly, or by removing the jumpers W1 and W2 on the board. The console lock can be defeated by replacing the jumpers W1 and W2 in the lower alternate positions.

6-9. ADJUSTMENTS

Set BIAS voltage to 2.4V ±0.1V DC. Adjust NULL to minimum (observe and adjust carefully); it requires 3 or 4 place accuracy for DVM measurement. An alternate NULL method is to observe emitter DC voltage (DC input, 0.05V/cm with 10:1 probe). Adjust NULL for minimum voltage -- +0.28 to +0.36 volts typical. Repeat for 5 to 10 switches and set NULL capacitor at the best average position. Oscillator frequency is 870 kHz typical.

Do not troubleshoot by looking at the base circuit with a scope probe (except for sensor failure noted below). The probe will detune the base enough to prevent proper operation.

The failure of the proximity switch sensor material may cause an intermittent connection. It can be checked by observing the signal envelope on the base circuit (at 20 msec/cm). Touching the sensor or moving it sideways should result in smooth envelope changes (not abrupt or jagged envelope).

6-10. The voltage on the emitter is the best indication of proper proximity operation. The normal level is +0.28 to +0.36 volts. It increases as the switch is touched. The AND gate switches and the clicker clicks at about 1.5 volts dc.

The light indicator is driven from circuitry on the Arithmetic Logic board. A clean envelope on the base and operation of the clicker at an emitter voltage of 1.5 volts usually indicates correct operation of the proximity circuit.

No adjustment of the values of the base circuit components exist. If the capacitor or inductor is changed it may be necessary to select this component to provide comparable switch sensitivity with the other switches. Slight change in oscillator frequency or Bias voltage may be helpful in establishing uniform switch sensitivity.

The clock input to the Switch Register FF is filtered with a 100 ohm, .01$\mu$f RC filter. This reduces improper triggering due to coupling in the cable. Replacement of the AND gate on the front panel may result in poor overall switch operation due to insufficient amplitude or rise time. It may be necessary to select an AND gate which will work properly.

6-11. LOAD CIRCUIT

The proximity switch circuit for the automatic use of the Basic Binary Loader is fundamentally the same. It has two additional features, however, which limits (or controls) the circumstances under which it can be operated. The Enable voltage for the emitter follower is disabled by the low PRS preset line. When the preset control is touched first this PRS line goes high which then allows normal operation of the Enable voltage to the emitter follower.

6-12. The $\overline{\text{RFB}}$ signal is low whenever the computer is running. Q4 is nonconducting and MC7 pin 1 is low preventing operation of load switch. When the computer is in halt mode RFB goes high. Now when PRS also goes high Q4 is conducting and MC7 pin 1 is enabled so that the load switch will operate.

## 6-13. SWITCH REGISTER LAMPS

The drive transistors for the Switch Register lamps are located on the Arithmetic Logic assembly. The proximity switch toggles the Switch Register flip-flop each time it is pushed. The contents of the Switch Register can be read into the S bus by the load memory or load address switch, or by an Input A or B instruction at select code 01.

The contents of the Switch Register can be set by an output (OT A/B) to select code 01. The register is cleared by $\overline{CSR}$ at T3, then the bits which are "one" are set at T4 by SSR and R bus. This allows using the lamps in the Switch Register to display information under program control.

The integrity of the lamp filaments can be checked by the LAMP TEST switch. (Refer to Figure 6-2.)

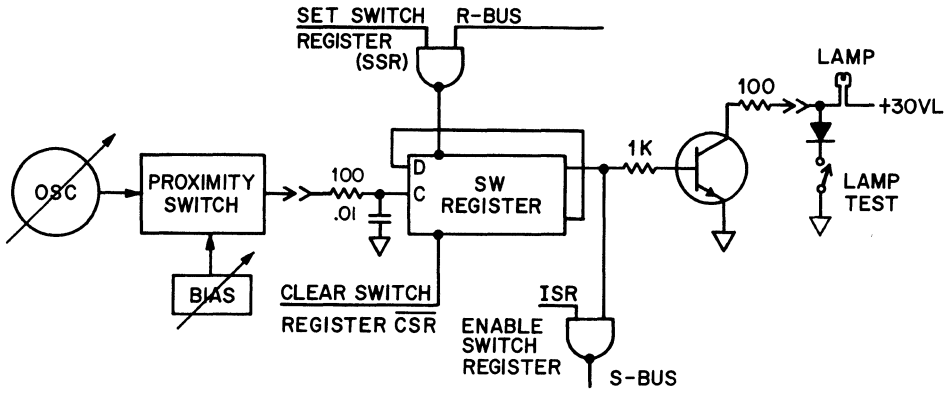



Figure 6-2. Switch Register Logic

## 6-14. RUN FF BUFFER

The RF2 is buffered on the front panel and the output $\overline{RFB}$ is used to control the LOAD, and to inhibit the LOAD MEMORY, LOAD ADDRESS, DISPLAY MEMORY, and SINGLE CYCLE switches.

A couple of isolated cases have arisen in which the value of C101 was too small and this allowed a malfunction in which the computer stepped 10 or 15 cycles or more. This can be quite confusing depending on what is in the affected memory locations.

## 6-15. FRONT PANEL TEST SWITCHES

The six switches accessible from the rear of the Front Panel assembly are useful for trouble-shooting and diagnostic purposes. It is wise to check their condition before starting to work on the machine.

## 6-16. CONSOLE LOCK

The Console Lock switch allows the operation of the Front Panel proximity switches to be inhibited. It removes the +12 volt Enable voltage from the proximity switch circuits.

Jumpers W1 and W2 are located in the upper right hand corner of the board (facing the components). They allow overriding the Console Lock by hardwiring the Enable lines to the +12 volt bus. W1 provides Enable voltage to the Switch Register. W2 provides Enable voltage to the Front Panel Control functions. This switch is used in applications where inadvertent operation of the Front Panel Controls or the Switch Register is undesirable.

6-17. LAMP TEST

The lamps used on the front panel are driven in many different ways. The use of this single switch applies voltage to the filaments of all front panel lamps. Some lamps will be brighter in Lamp Test. This results from the full 30 volt lamp supply voltage in test position. In normal operation the lamp driver has a current limiting resistor for lamp turn on and to establish a satisfactory illumination level.

The lamps associated with the Memory Register bits 14 and 15 are tested by the Lamp Test, but are not used by the computer in any operational sense. They can be used as spare lamps.

6-18. LOADER ENABLE

This Loader Enable switch provides a means to protect the top 64 core locations, but still to have access under certain conditions. It must be ON for core access. This allows using the bootstrap loader, or by direct toggling to enter the Basic Binary Loader instructions. The switch is then protected in NORMAL position.

The front panel PRESET-LOAD allows automatic access to the Basic Binary Loader without the necessity of manipulating this Loader Enable (protect) switch.

Occasions arise in which access is desired. If malfunctions occur in the PRESET-LOAD circuits operation in the manual mode might still be possible (enable the protected area Loader Enable to ON, set switch register to 0X7700, Load Address, Preset, Run).

The switch is also helpful to display contents of the protected area, and to allow Single Cycle operation for debugging.

6-19. SINGLE INSTRUCTION LOOP

The output of the Single Instruction switch in LOOP position is the signal SIN. This signal has one function. It holds the SB0 high at time T67. This prevents the P+1 → P, M. Thus, no incrementing of the P and M Registers occurs in the normal operations (Run, Single Cycle, Display Memory, Load Memory, etc.).

This allows performing the same instruction repetitively. It is usually easier than trying to write a short loop program. Refer to Phase Loop below.

6-20. PHASE LOOP

The output of the Phase Loop switch is the LNS negative true. This signal (negative) prevents clocking the Phase flip-flops. It thus retains the phase condition established at the time it is placed in the LOOP position.

It is useful for initializing core. An instruction like Store A is single cycled to execute phase. The Phase switch is then placed in LOOP condition. This allows the P and M Registers to increment. The contents of the A-Register are stored through core. This is one method used for checking the Sense Amplifiers.

A useful combination of Phase and Single Instruction Loop allows repetitive data store in a single memory location.

6-21. MEMORY OFF SWITCH

The Memory Switch in OFF position produces the MON negative signal. The positive MON is required to generate the MTE which in turn controls the memory timing generator. This OFF position essentially makes all core locations NOP instructions.

## 6-22. HALT BUTTON

The Halt switch provides two useful functions. If the HALT switch is touched during a LOAD MEMORY the P and M Registers are not incremented. It allows loading the A Register and executing the instruction without the necessity of loading address 0 in between.

The other use is in conjunction with the Interrupt Phase 4. The Run flip-flop is a required input to set Phase 4. Run FF is not set while using the Single Cycle button. Therefore, the computer can not execute a Phase 4 Interrupt through use of the Single Cycle button. Holding HALT while pushing RUN will result in executing a single machine cycle (like Single Cycle). Since the Run FF is set in this mode of operation the setting of Phase 4 is allowed.

## 6-23. FRONT PANEL OPERATING CONTROLS

The following material describes the logical functions used in the Front Panel Operating Controls. Refer to Figure 2-6 for the circuit diagram for the controls.

Table 6-1. Front Panel Operating Controls

| BUTTON | MNEMONIC | FUNCTION |
|---|---|---|
| RUN | RNL | Forces Single Cycle FF1, 2; providing conditions on Run FF1 (set input) to continue in Run mode. |
| HALT | HLL | Sets the K input to Run FF 1, causes halt after current machine cycle. |
| PRESET | PRS | Provides POPIO @ T5.<br>Clears Step FF1, 2.<br>Clears Phase FF 1-4. |
| CLEAR REGISTER | CLR | Generates $\overline{CSR}$ which directly clears the Switch Register FF's. |
| LOAD ADDRESS | LPML | Produces SSPM which generates all STM and STP strobes.<br>Produces SEO → EOF and ISR.<br>Holds off MST and sets MWL to overlook Parity condition.<br>Set Phase 1.<br>Operation does not require Single Cycle.<br>Holds off Preset and Load. |
| LOAD MEMORY | LML | Produces SWST (SWSA if addr Ø, SWSB if addr 1) Strobe signals.<br>Set Phase 3.<br>Force Single Cycle operation.<br>Set EIR to inhibit Instruction Register.<br>Produces SEO → EOF and ISR.<br>Holds off MST and sets MWL to overlook Parity condition.<br>Holds off Preset and Load |
| LOAD | LDL | Overrides Memory Protect giving MTE.<br>Forces Single Cycle and Run.<br>Sets Phase 1.<br>Generates SAL and SSPM to set Loader address.<br>$\overline{RF2}$ retains the sense of LDL as long as Run mode continues. |
| DISPLAY MEMORY | DML | Set Phase 3.<br>Initiate Single Cycle.<br>Set $\overline{EIR}$ to inhibit Instruction Register normal Phase 3 operation:<br>Clear T @TØ, Memory Timing for Read and Write, P + 1 → P.M. |
| SINGLE CYCLE | SCL | Operates Step FF 1, 2 to achieve one machine cycle. Single Cycle and Halt can be used together to prevent incrementing P and M Registers (holds off $\overline{SBØ}$). |

## 6-24. BASIC BINARY LOADER

CAUTION

To load CLEAR SWITCH REGISTER before PRESET and LOAD.

The Basic Binary Loader has two optional features in addition to the primary loading capability. The features are selected by bits Ø and 15. They include comparing the tape against core (without loading) and Check Sum (without loading). To insure proper load it is necessary to clear the Switch Register before loading the tape.

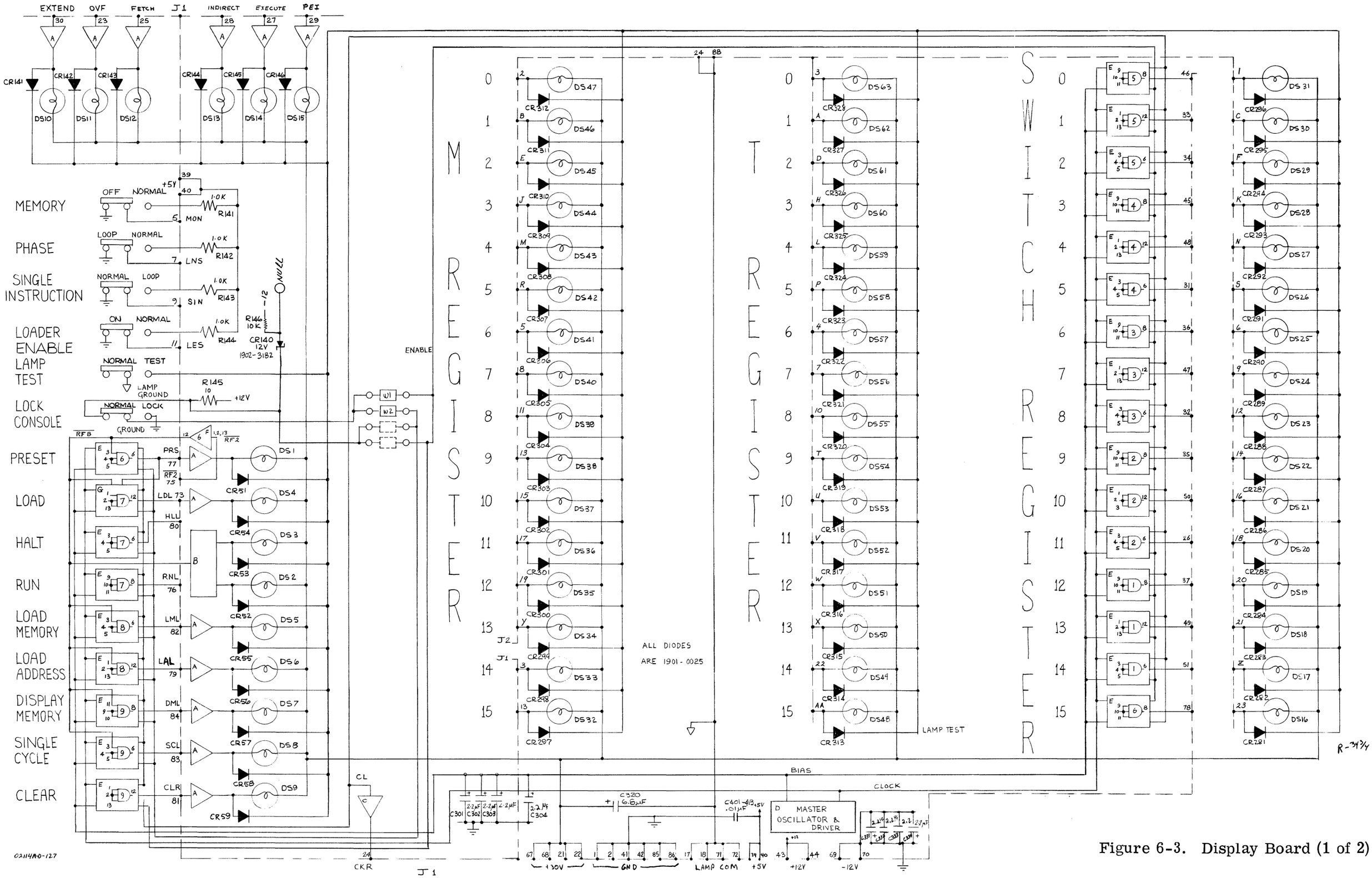
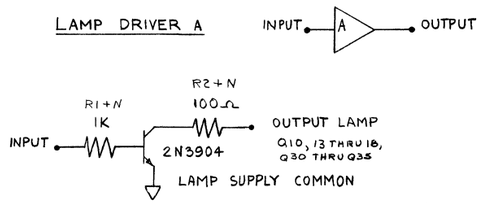


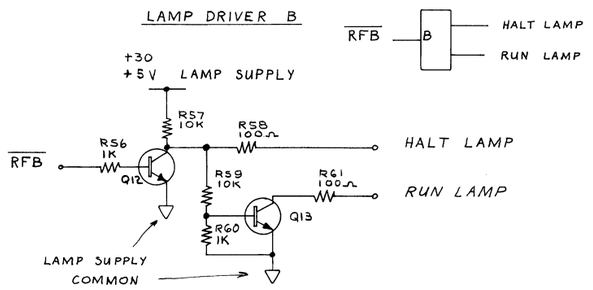

Figure 6-3. Display Board (1 of 2)

## LAMP DRIVER A

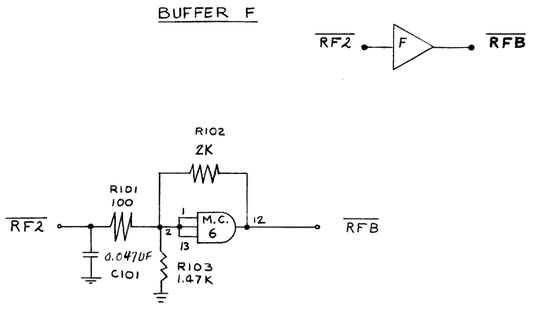



| | | |
|---|---|---|
| RESET | N= 50 | (R51, R52, Q11) |
| LOAD | N= 65 | (R66, R67, Q14) |
| LOAD MEMORY | N= 70 | (R71, R72, Q15) |
| LOAD ADDRESS | N= 75 | (R76, R77, Q16) |
| DISPLAY MEMORY | N= 80 | (R81, R82, Q17) |
| SINGLE CYCLE | N= 85 | (R86, R87, Q18) |
| CLEAR REGISTER | N= 90 | (R91, R92, Q19) |
| EXTEND | N= 150 | (R151, R152, Q40) |
| OVERFLOW | N= 155 | (R156, R157, Q41) |
| FETCH | N= 160 | (R161, R162, Q42) |
| INDIRECT | N= 165 | (R166, R167, Q43) |
| EXECUTE | N= 170 | (R171, R172, Q44) |
| PARITY | N= 175 | (R176, R177, Q45) |

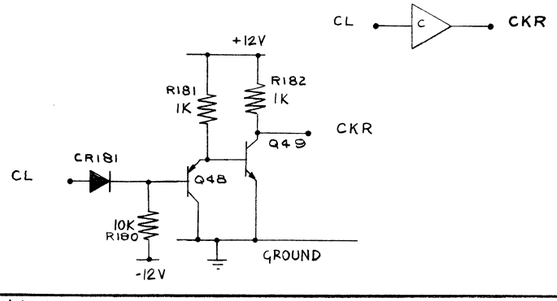
## LAMP DRIVER B



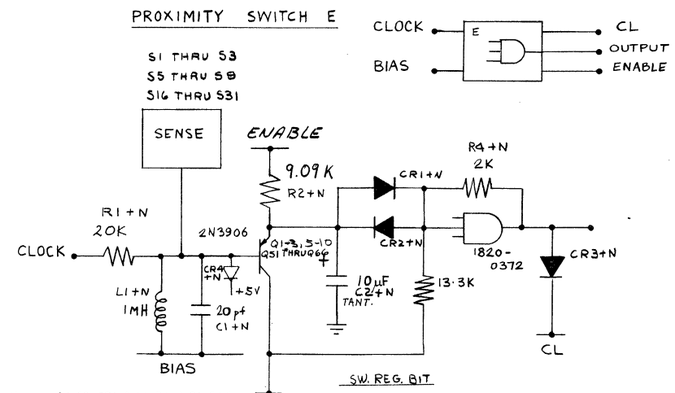

## BUFFER F




## RELAY DRIVER C




## PROXIMITY SWITCH E

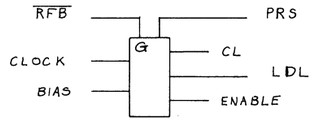


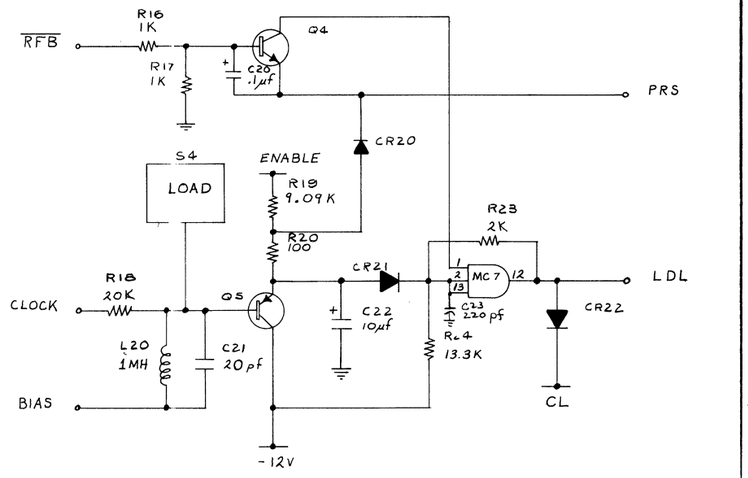

| | | |
|---|---|---|
| PRESET | 1 | N= 0 (C1, C2, CR1-4, L1, R1-4, Q1, S1) |
| RUN | 2 | N= 5 (C6, C7, CR6-9, L6, R6-9, Q2, S2) |
| HALT | 3 | N= 10 (C11, C12, CR11-14, L11, R11-14, Q3, S3) |
| LOAD MEMORY | 5 | N= 25 (C26, C27, CR26-29, L26, R26-29, Q5 S5) |
| LOAD ADDRESS | 6 | N= 30 (C31, C32, CR31-34, L31, R31-34, Q7, S6) |
| DISPLAY MEMORY | 7 | N= 35 (C36, C37, CR36-39, L36, R36-39, Q8, S7) |
| SINGLE CYCLE | 8 | N= 40 (C41, C42, CR41-44, L41, R41-R44 Q9, S8) |
| CLEAR REGISTER | 9 | N= 45 (C46, C47, CR46-49, L46, R46-R49, Q10, S9) |

SW. REG. BIT

| | | |
|---|---|---|
| 16 | 15: | N= 200 (C201, C202, CR201-204, L201, R201-204, Q51, S16) |
| 17 | 14: | N= 205 (C206, C207, CR206-209, L206, R206-209, Q52, S17) |
| 18 | 13: | N= 210 (C211, C212, CR211-214, L211, R211-214, Q53, S18) |
| 19 | 12: | N= 215 (C216, C217, CR216-219, L216, R216-219, Q54, S19) |
| 20 | 11: | N= 220 (C221, C222, CR221-224, L221, R221-224, Q55, S20) |
| 21 | 10: | N= 225 (C226, C227, CR226-229, L226, R226-229, Q56, S21) |
| 22 | 9: | N= 230 (C231, C232, CR231-234, L231, R231-234, Q57, S22) |
| 23 | 8: | N= 235 (C236, C237, CR236-239, L236, R236-239, Q58, S23) |
| 24 | 7: | N= 240 (C241, C242, CR241-244, L241, R241-244, Q59, S24) |
| 25 | 6: | N= 245 (C246, C247, CR246-249, L246, R246-249, Q60, S25) |
| 26 | 5: | N= 250 (C251, C251, CR251-254, L251, R251-254, Q61, S26) |
| 27 | 4: | N= 255 (C256, C257, CR256-259, L256, R256-259, Q62, S27) |
| 28 | 3: | N= 260 (C261, C262, CR261-264, L261, R261-264, Q63, S28) |
| 29 | 2: | N= 265 (C266, C267, CR266-269, L266, R266-269, Q64, S29) |
| 30 | 1: | N= 270 (C271, C272, CR271-274, L271, R271-274, Q65, S30) |
| 31 | 0: | N= 275 (C276, C277, CR276-279, L276, R276-279, Q66, S31) |

## PROXIMITY SWITCH G




## MASTER OSCILLATOR & DRIVER

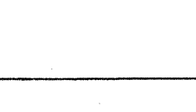






Figure 6-4. Display Board (2 of 2)

02114A-D-126

**Did I check WHAT switches first behind the front panel??**

FiG. 6–5

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