HONEYWELL CENTRAL PROCESSOR SUMMARY

SERIES 200 **NEW DIMENSIONS OF PROVEN COMPUTER PERFORM-**

ANCE WITH UNPARALLELED ABILITY TO MATCH THE EXACT DIMENSIONS OF YOUR BUSINESS



Copyright 1965 Honeywell Inc. Electronic Data Processing Division Wellesley Hills, Massachusetts 02181

CENTRAL PROCESSOR SUMMARY

Speed, simultaneity, capacity — three components of a common dimension. The processing dimension of Series 200 is a completely flexible approach to meeting today's processing requirements today — simply, efficiently, economically. It provides a framework of processing features which can be precisely tailored to provide optimum performance characteristics. Included in this framework are such job-oriented features as universal code translation, interrupt processing, floating-point arithmetic, storage protect, and financial edit. It provides a base from which to project processing power into new application areas: real time processing, communications, engineering, data reduction, etc. In short, the processing dimension of Series 200 is a key element of a practical and realistic approach to data processing --- dimensional data processing.

Projection of the processing dimension to fit a particular need encompasses five program-compatible processing units: Models 120, 200, 1200, 2200, and 4200. As will be seen on the pages that follow, the model designation associated with a system's processing dimension indicates the balance of speed (memory speeds from 188 nanoseconds to 3 microseconds per character), simultaneity (from 1 to 16 simultaneous input/output operations concurrent with computing), and capacity (core memory from 2K to 524K characters) selected by the user to solve his problems best.

SELECTING A PROCESSOR

Four tables are presented below which illustrate the free-form design of Series 200. Approximately 550 processor configurations can be formed through the use of these tables due to the complete modularity, flexibility, and compatibility within Series 200. By specifying values from each table, you can select a processor which is precisely tailored to your data processing requirements.

Figures 1, 2, and 3 illustrate the inherent characteristics of each processor model based on three power dimensions: speed, size, and simultaneity. Main memory speed is constant throughout the ranges of any one processor, while the dimensions of size and simultaneity are expandable. For instance, Model 2200 has a processing speed of 1 microsecond per character, yet ranges in memory size from 16,384 to 262,144 characters. In addition, Model 2200 can perform from 4 to 8 simultaneous peripheral operations while computing.

Figure 4 illustrates a number of processor features which may be added to the processor devised from Figures 1 through 3, depending upon your individual requirements and the applications of your system. Since these special features are offered as additional capabilities to various processors, a user need not be burdened with investment in a processing feature which is not required in the handling of his individual processing problems. As his needs grow or change, such features may be either added or deleted to meet the restless demands of his occupational growth.



Figure 1. PROCESSOR SIZE SE-LECTOR — Memory capacity is given in thousands of characters (nominal).



Figure 3. PROCESSOR SPEED SELECTOR — Speed is given in microseconds per character.



Figure 2. PERIPHERAL INTERFACE SELECTOR — Basic capabilities are shown in color. Additional capabilities shown in incremental sizes. (The number of input/output trunks determines the number of peripheral controls that can be connected to a processor model.)

	120	200	1200	2200	4200
AUTOMATIC CODE TRANSLATION	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD
ADVANCED PROGRAMMING			STANDARD	STANDARD	STANDARD
FINANCIAL EDIT			STANDARD	STANDARD	STANDARD
FLOATING-POINT ARITHMETIC	N/A	N/A			STANDARD
MEMORY PROTECT	N/A	N/A	N/A		

Figure 4. PROCESSOR FEATURE SELECTOR — Availability of special features is indicated in color.

A CLOSER ANALYSIS

PROCESSING UNIT: Complete data compatibility within Series 200 is insured by the use of a 6-bit character as the information unit for all processors. In addition to allowing intra-Series 200 communication, this character format provides compatibility with the majority of existing Honeywell and non-Honeywell data files. Other accepted data formats are handled by Series 200 processors by means of an automatic code translation capability.

ADDRESSING: Any memory location can be addressed in any one of three formats: direct, indirect, or indexed addressing. The use of binary addressing eliminates the necessity of complex machine-language coding schemes to represent memory addresses in expanded configurations. Index register usage is by no means restricted in Series 200; indexed addressing is possible in all instruction formats. In addition, indexed addressing is simplified by a convenient loop control technique which automatically increments and tests index register contents.

INSTRUCTION FORMAT: Instructions are coded in a two-address, variable-length format. However, one or perhaps both addresses may often be omitted, thereby saving memory space and speeding up instruction execution.

READ/WRITE CHANNELS: The data path between main memory and a peripheral device is completed by a programmer-assigned read/write channel. Since this channel is not a fixed connection to any one unit but is rather a floating link that can be used by any device, the optimum realization of the simultaneous capabilities of Series 200 is insured. As opposed to the conventional method of complex and costly high-speed and low-speed transmission lines, the read/write channel can be assigned to any device regardless of speed or mode of data transfer.

SIMULTANEITY: The simultaneous operation of peripheral devices is *automatically* monitored by traffic control hardware, so that peripheral demands are guaranteed immediate response. Complex software monitoring is rendered unnecessary due to this advanced design feature.

INTERRUPT SYSTEM: Series 200 processors feature an interrupt system in which an interrupt source, whether internal or external, meets automatic and immediate response. The interrupt source is properly identified, and a change in program sequence to service the interruption is automatically executed.

MEMORY PROTECTION: Models 2200 and 4200 have the ability to shield any specified portion of main

memory from unintentional interference. Memory can be divided into two portions — a "protected" area and an "open" area — each portion housing an individual routine or program. Not only is information in the protected area prevented from being written, but it can also be protected from being read. Thus, memory protection in Series 200 is double protection: since protected information can be neither written nor read, a program operating in the open memory area is not destroyed by the accidental reading of unrecognizable data from the protected area.

MODEL 120

- Memory speed: 3 microseconds per character
- Memory capacity: 2,048 to 32,768 characters
- Processing unit: six-bit character
- Instruction format: variable, two-address
- Index registers: 6
- Operations: Decimal and binary arithmetic, control, and logical operations; advanced programming and financial edit operations optional
- Automatic interrupt
- Read/write channels: 2 (standard); 3 (optional)
- Input/output trunks: 4 (standard); 8 (optional)
- Simultaneous operations: one input and one output (standard); one additional input or output (optional)

MODEL 200

- Memory speed: 2 microseconds per character
- Memory capacity: 4,096 to 65,536
- Processing unit: six-bit character
- Instruction format: variable, two-address
- Index registers: 6
- Operations: decimal and binary arithmetic (including multiply/divide), control, and logic operations; advanced programming and financial edit operations optional
- Automatic interrupt
- Control memory: 16 control registers
- Control memory access time: 250 nanoseconds
- Control memory cycle time: 500 nanoseconds
- Read/write channels: 3 (standard); 4 (optional)
- Input/output trunks: 8 (standard); 16 (optional)
- Simultaneous operations: 3 input/output operations (standard); 4 input/output operations (optional)

MODEL 1200

- Memory speed: 1.5 microseconds
- Memory capacity: 8,192 to 131,072 characters

- Processing unit: six-bit character
- Instruction format: variable, two-address
- Index registers: six
- Operations: Decimal and binary arithmetic (including multiply/divide), control, logic, financial edit, and advanced programming; binary scientific operations optional
- Range of normalized floating point values: 10⁻⁶¹⁶ to 10⁺⁶¹⁶
- Automatic interrupt
- Control memory: 16 control registers
- Control memory access time: 250 nanoseconds
- Control memory cycle time: 500 nanoseconds
- Read/write channels: 4 (standard)
- Input/output trunks: 16 (standard)
- Simultaneous operations: 4 input/output operations (standard)

MODEL 2200

- Memory speed: 1 microsecond per character
- Memory capacity: 16,384 to 262,144 characters
- Processing unit: six-bit character
- Instruction format: variable, two-address
- Index registers: 30
- Operations: Decimal and binary arithmetic (including multiply/divide), control, logic, financial edit, and advanced programming; binary scientific operations optional
- Range of normalized floating point values: 10⁻⁶¹⁶ to 10⁺⁶¹⁶

- Automatic interrupt
- Memory protect (optional)
- Control memory: 16 to 32 control registers
- Control memory access time: 250 nanoseconds
- Control memory cycle time: 500 nanoseconds
- Read/write channels: 4 (standard); 8 (optional)
- Input/output trunks: 16 (standard); 32 (optional)
- Simultaneous operations: 4 input/output operations (standard); 8 input/output operations (optional)

MODEL 4200

- Memory speed: 750 nanoseconds per four characters (188 nanoseconds per character)
- Memory capacity: 32,768 to 524,288 characters
- Processing unit: six-bit character
- Instruction format: variable, two-address
- Index registers: 30
- Operations: Decimal and binary arithmetic (including multiply/divide), control, logic, financial edit, advanced programming, and binary scientific operations
- Range of normalized floating point values: 10⁻⁶¹⁶ to 10⁺⁶²⁶
- Automatic interrupt
- Memory protect (optional)
- High-speed internal control registers
- Read/write channels: 8 (standard); 16 (optional)
- Input/output trunks: 32 (standard); 64 (optional)
- Simultaneous operations: 8 input/output operations (standard); 16 input/output operations (optional)

Honeywell ELECTRONIC DATA PROCESSING

SALES OFFICES AND DATA CENTERS IN PRINCIPAL CITIES OF THE WORLD

i

DSA-131 25265