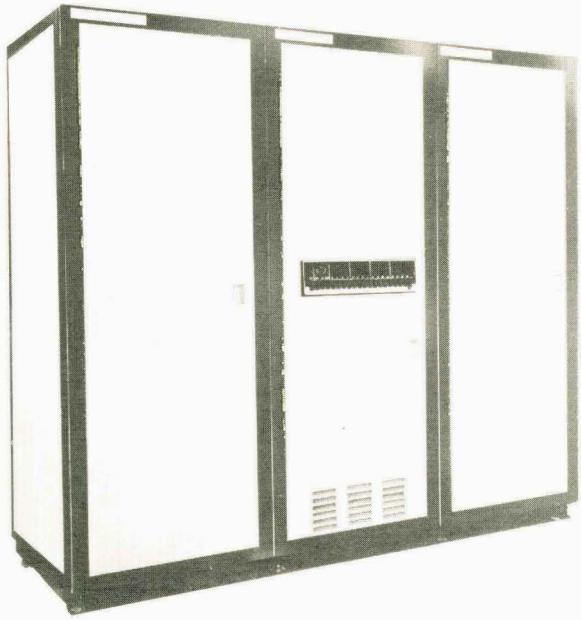
GE PAC 3010/2

A Mini-Based Computer System

GENERAL DESCRIPTION



GENERAL ELECTRIC

GET-6227
5/72 (1M)
$4.50

GE PAC 3010/2

A Mini-Based Computer System

GENERAL DESCRIPTION

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INTRODUCTION

This manual contains a functional description of the GE-PAC* 3010/2 process computer system, including all standard functional subsystems and options.

1.1 MAJOR FEATURES OF THE GE-PAC 3010/2 COMPUTER SYSTEM

The GE-PAC 3010/2 is a fully modular, cost/performance optimized, process computer system. The experience gained in producing the larger and more powerful GE-PAC 4000 series of process computers has led to the development of smaller and less expensive systems - the GE-PAC 3010 and the GE-PAC 3010/2. The 3010/2 offers functions and capabilities similar to the 3010, but utilizes a more modern, smaller, faster, and more powerful Central Processor.

The GE-PAC 3010/2 Central Processor features up to 65,536 bytes of random access Core Memory, a powerful processor which implements a set of 113 instructions plus automatic housekeeping and I/O operation, an interrupt structure and I/O interface which may serve up to 255 device and process I/O controllers, a Control Console which allows programming and maintenance personnel to observe and control the Central Processor operations, and a built-in I/O teletypewriter interface.

The physical size, complexity, and cost of the Processor are reduced through the use of a solid state nonvolatile Read-Only Memory (ROM). The ROM contains a micro-program which emulates the 113 user instructions and performs the housekeeping and automatic I/O sequences.

The user instructions include full subsets of fixed point and floating point arithmetic instructions, shift instructions, list processing instructions, branch instructions, logical instructions, and the Supervisor Call instruction. Supervisor Call is used by the application programs to interface with the operating system, RTMOS-30. The GE-PAC 3010/2 is upwardly program compatible with the GE-PAC 30-1, 30-2, 30-2E, and the 3010. Programs which run on these earlier machines will run on the 3010/2 with little or no modification, and at increased speed.

User instructions which address Core Memory may specify any address up to the maximum of 64K bytes, and no paging or indirect addressing is required. The core cycle time is 1.0 microsecond.

Sixteen hardware registers are available for temporary data storage and 15 of these registers may be used for indexing. The hardware registers store 16-bit halfwords. Thirty-two core locations are reserved as floating point arithmetic registers. These locations provide storage for eight 32-bit fullwords.

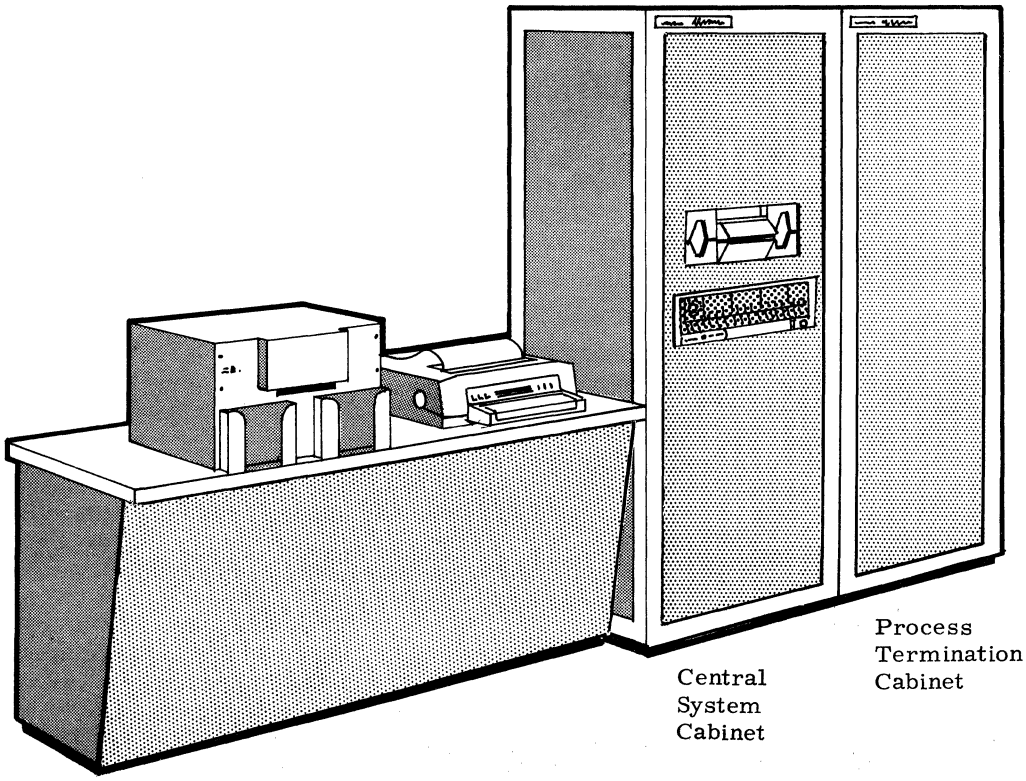

Fig. 1.1 GE-PAC 3010/2 Process Computer

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The principal interface between the Processor and the device and process I/O controllers is the Multiplexer Bus. Any controller may be implemented merely by plugging it into an available slot on the Multiplexer Bus and removing one jumper wire from the back panel. Interrupt priority for the controllers decreases as they are implemented in positions which are more distant from the Processor, so the controllers whose timely operation is more critical to the overall system operation are assigned positions nearer the Processor.

All optional system functions are fully modular and may be installed in the factory or in the field. A full line of peripheral devices, including typers, punches, readers, and video displays is available. The process I/O subsystems are capable of serving up to 2048 digital inputs, 2048 digital outputs, 256 analog input points, 16 absolute analog outputs, and 64 variable outputs to C/M or C/M/A stations. Additional process digital and/or analog I/O subsystems may be added to increase this capability.

1.2 SCOPE

This document defines the GE-PAC 3010/2 Computer System and its functional features. The features and performance of each module and subsystem available in the 3010/2 Computer System are described. The actual contents of any individual 3010/2 Computer System are described on the procurement documents for that system. General Electric reserves the right to modify at any time without notice to Customer the contents of this document or the design or functions of the system or any part thereof for reasons of improved performance and operational flexibility. If any conflicts exist between this General Description and General Electric Company's applicable Functional Design Specifications, the latter will take precedence. In a given transaction between General Electric Company and a customer, the provisions of the contract document will supercede this General Description and define General Electric Company's obligation to the customer.

1.3 REFERENCES

A detailed functional description of the Central Processor is provided in the GE-PAC 3010/2 Central Processor Reference Manual, GET-6047. That manual describes Core Memory, the Processor, the Multiplexer Channel and Bus, the optional Selector Channel, each of the 113 user instructions, interrupts, and automatic I/O operations.

GET-6174 combines in one manual the same type of information for the 3010/2 as was provided in GET-6047, the 30/3010 Reference Manual, and PCP-126, the Systems Interface Manual, for 3010 systems.

The theory of operation for the overall system and detailed theory of operation for each functional subsystem are provided in the Theory of Operation manuals shipped with each 3010/2 system. Computer maintenance information is also provided, including preventive maintenance, performance testing, adjustment, troubleshooting, and repair instructions.

The GE-PAC 3010/2 System Hardware Configurator, PCP-230, provides instructions for using the GE-PAC 3010/2 Price List and the 3010/2 System Hardware Specification sheets to configure a system. This General Description describes the functional features and operating features of each standard system module. When the implementation of an option requires that some other function be implemented, such information is given. Users of the Hardware Configurator may refer to appropriate sections of this manual to aid in determining which hardware should be implemented.

The GE-PAC 3010/2 system software is described in manuals which describe the standard system software and in special documentation provided when the application programs are developed by the General Electric Company for specific systems. The standard software manuals include GET-6171, the GE-PAC 30/3010 Programming Reference Manual; GET-3083, RTMOS-30 Reference Manual (for systems with Drum Memory); and GET-3082, RTMOS-30 Reference Manual (for all-core systems).

SOFTWARE

The GE-PAC 3010/2 software and hardware are designed to complement each other to the greatest extent possible, through careful consideration of which functions can be more efficiently and economically accomplished by hardware and by software. This feature is illustrated by the relation of RTMOS-30, the standard real-time multiprogramming operating system for the 3010, to such hardware features as the Processor's Protect Mode, which protects RTMOS-30 from interference from other programs. Another such feature is the user instruction set, which includes the powerful Supervisor Call instruction, SVC. SVC serves as the interface between RTMOS-30 and the programs which run under its control.

All of the standard software is fully modular, which greatly facilitates the compilation of the on-line programs for a system. The standard software may be divided into two classes: (1) programs which run while the computer is on-line and controlling the process, and (2) programs which run when the computer is off-line. All of the programs in the first group run under the control of RTMOS-30. The programs in the second group consist principally of assemblers, loaders, editors, and debugging programs. Hardware test programs might also be considered as members of the second class, but because they are used primarily by installation and maintenance personnel, they are supplied with the system maintenance materials, rather than with the system software.

The standard off-line programs are described in the GE-PAC 30/3010 Programming Reference Manual, GET-6171. This manual also describes much of the technique for using the system software, such as the assembler language, program loading, generation, and debugging. The system's instruction set, interrupt handling, programmed and automatic I/O sequences, and Display Panel operation are described in the GE-PAC 3010/2 Central Processor Reference Manual, GET-6174. The all-core version of RTMOS-30 is described in GET-3082. GET-3083 describes the Drum version of RTMOS-30.

GENERAL INFORMATION

This section provides general information which applies to all GE-PAC 3010/2 computer system equipment, unless specifically excepted in the detailed descriptions in Sections 4 through 12.

3.1 ENVIRONMENTAL SPECIFICATION

The detailed environmental specifications for the GE-PAC 3010/2 product line are described in the Functional Design Specifications and in the GE-PAC 3010/2 Environmental Specification. The system is designed to meet the performance specifications at any ambient temperature from 0° C to 50° C, provided that the relative humidity is such that no moisture condensation on the equipment occurs. If the following equipment options are implemented within or in the same environment as the Central System Cabinet, the operating temperature range is reduced as follows:

Drum Memory; 10° C to 40° C.
Teletypewriter; 18° C to 29° C.
TermiNet* Printer; 0° C to 40° C.
Magnetic Tape Transport; 2° C to 50° C.
Disc Unit; 15.6° C to 32.2° C.
Display Controllers/Terminals; 18°C to 29°C.
Card Punch; 18° C to 29° C.
Card Reader; 20° C to 27° C.

3.2 INPUT POWER

The primary AC supply to the computer system is connected to the AC entry panel in the Central System Cabinet (CSC). This must be from a single phase source, 103V to 127 VAC, 60 Hz ±3.0%, three wires (high, neutral, and safety ground), with harmonic voltage distortion no greater than 5%. It is strongly recommended that this supply be isolated from external noise sources by an isolation transformer which provides shielding between the source and load. Refer to the GE-PAC 3010/2 Site Planning Manual, GET-6046, for additional information.

3.2.1 Peripheral Devices

All of the peripheral devices plug into standard three-pin wall sockets and require 115 VAC ±10%. They should be supplied from the same distribution as the CSC.

3.2.2 Process I/O Termination Cabinets

The termination cabinets are supplied from the CSC. Voltage, frequency, and harmonic distortion requirements are as for the CSC.

3.2.3 Drum Cabinet

The Drum Cabinet requires 115 VAC ±10%, 57 to 63 Hz, single-phase, three-wire power.

3.3 CABLING

Interconnecting cables between major assemblies, cabinets, and peripheral devices, are plug connected, or connected via screw terminals. All cables with more than nine conductors are plug connected on at least one end.

3.4 CONSTRUCTION

3.4.1 Cabinets

All of the electronic circuitry in the computer system, except for that contained in peripheral devices, is housed in heavy duty cabinets suitable for use in an industrial environment. Where necessary to meet the environmental requirements, the cabinets are cooled by blower driven air. Air filters are provided in cabinets containing blowers to remove airborne dirt from the air supply. The following cabinets are employed as required (dimensions, approximate H x D x W): Central System Cabinet (75 x 28 x 30 inches), Process I/O Termination Cabinet (75 x 28 x 30 inches), Drum Cabinet (75 x 28 x 30 inches). The CSC provides for cable entry in an area at the bottom of the cabinet. The termination cabinet accepts cables either at the top or the bottom of the cabinet.

Where the CSC must be operated in a corrosive environment, the cabinet may be provided in an optional "purged air" version. When this option is implemented, the customer supplies fresh clean air at the top of the cabinet to maintain positive internal pressure, thereby prohibiting the entry of contaminated air (option no. 3010AJ4501).

3.4.2 Printed Wire Boards

The electronic components are installed on plug-in printed wire boards where practicable. The electronics are primarily monolithic integrated circuits.

3.4.3 Modularity

Most of the electronic modules in a 3010/2 system are located in the CSC. In addition to the CSC, 3010/2 systems typically have one or more process I/O termination cabinets, and several free-standing peripheral devices. The first Paper Tape Reader may be built into the front of the CSC. Systems with Drum, Disc, and Magnetic Tape Memory may have one or more bulk memory cabinets. All standard system options (except for some TermiNet Printer features) may be added in the factory or in the field by plugging-in or bolting-on the hardware and making minor wiring changes.

3.4.4 Maintainability

The system is designed for maximum availability. All system components are designed to permit quick and easy access to the internal hardware. Test programs, procedures, and test hardware are available, and they, and the system documentation are designed to minimize the degree of specialization required of maintenance personnel.

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The Central Processor is the computational and control center for the GE-PAC 3010/2 computer system. The basic Central Processor is contained in a single ultra-compact unit, which includes a Processor, the first 8,192 bytes of Core Memory, and may include additional core modules, Selector Channels, or I/O controllers. This basic unit accommodates up to eight 15" printed wire boards, of which five are devoted to the Processor and the basic 8K core module. The basic Central Processor includes a Control Console.

A block diagram of the Central Processor is provided on Fig. 4.1. The Central System Cabinet contains the basic Central Processor chassis, the basic System Power Supply, the system power control circuits, and may include one or more expansion chassis and System Power Supplies for the implementation of additional Core Memory, Selector Channel, or I/O controller boards.

The Processor's interface with the optional Universal Clock, Automatic Memory Protect Controller, and all other peripheral device and process I/O controllers, is provided by the Multiplexer Channel and Bus. The Selector Channel and Bus provide the interface to the bulk memory subsystem options, including Drum, Disc, and Magnetic Tape subsystems.

The 3010/2 process computer system achieves a functional capability similar to much larger and more complex computers through the use of a solid state non-volatile Read-Only Memory (ROM). The ROM greatly reduces the complexity of the Processor logic by executing micro-instruction routines which implement the 113 user instructions, effect the automatic I/O sequences, and perform housekeeping operations such as interrupt monitoring, Control Console service, and automatic register storage and restoration during power-down/restart sequences.

4.1 DATA AND INSTRUCTION WORD FORMATS

The Central Processor data and instruction words appear both in the hardware and in the documentation in the forms depicted on Fig. 4.1-1. These formats lend themselves to the use of hexadecimal notation, where each hexadecimal digit represents four binary bits ($2^4 = 16$). The hexadecimal digit set and its relation to binary, octal, and decimal notation are described on Table 4.1-1.

Fixed point data are represented in the form of 16-bit halfwords or 32-bit fullwords, where bit 0 is the sign bit. Positive numbers are represented as true binary numbers, with a sign bit of zero. Negative numbers are represented in two's complement form, with a sign bit of one.

Floating point data are represented in fullword form, with bit 0 serving as the sign bit. The number consists of a signed exponent (X) and fraction (F), as on Fig. 4.1-2.

4.2 FUNCTIONAL DESCRIPTION

The overall sequencing of the Central Processor is controlled by a current Program Status Word (PSW). The PSW is a 32-bit fullword. The upper halfword defines the program status and resides in a 16-bit PSW register in the Processor (Fig. 4.2-1). The lower half of the PSW defines the location of the next user instruction and it resides in the fourth microprogram register in the Processor's register stack.

Binary	Octal	Decimal	Hexadecimal
0000	0	0	0
0001	1	1	1
0010	2	2	2
0011	3	3	3
0100	4	4	4
0101	5	5	5
0110	6	6	6
0111	7	7	7
1000	10	8	8
1001	11	9	9
1010	12	10	A
1011	13	11	B
1100	14	12	C
1101	15	13	D
1110	16	14	E
1111	17	15	F

Binary (0 15)	Hexadecimal	Decimal	Octal
0111 1111 1111 1111	7FFF	32,767	77,777
0111 0000 0000 0000	7000	28,672	70,000
0000 0000 1111 1111	00FF	255	377
0000 0000 1000 0111	0087	135	207
0000 0000 0000 0111	0007	7	7

Table 4.1-1 Hexadecimal, Decimal, Octal and Binary Relationships

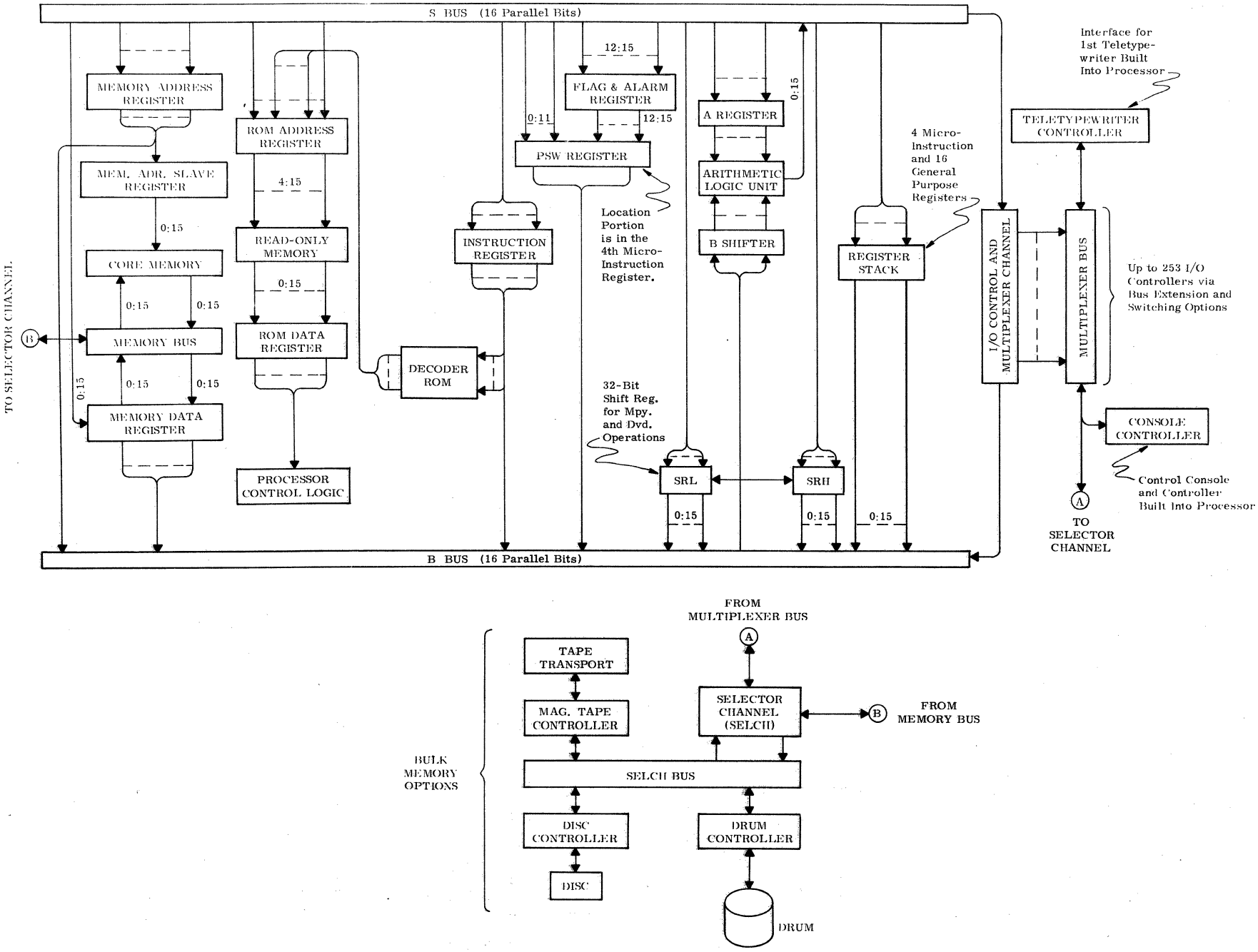


Fig. 4.1 3010/2 Central Processor

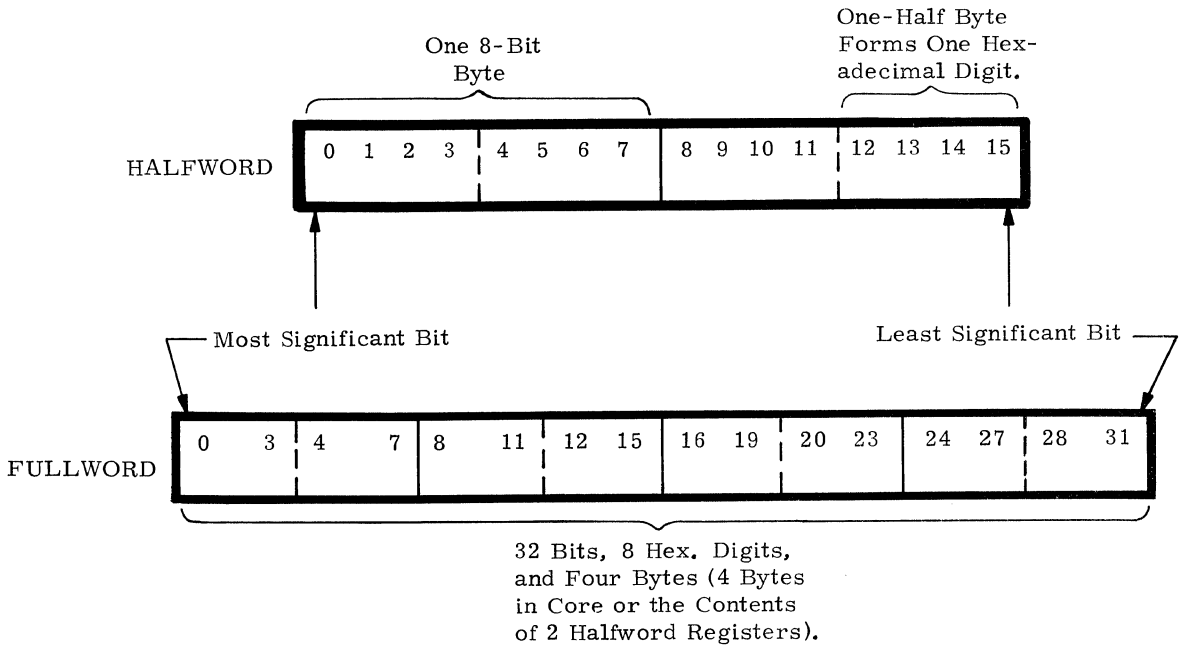


Fig. 4.1-1 Data and Instruction Word Formats

The PSW is automatically updated as program sequencing progresses, and it may be changed by the program.

The PSW is also involved in subroutine linkages and the servicing of interrupts. The program may load a new PSW or temporarily exchange the current PSW for a new one in order to initiate the execution of a new subroutine. Non-current PSW's are normally stored at core locations dedicated to specific interrupts. Interrupts may originate in the Processor or in external controllers, and each causes a PSW exchange, if it is not inhibited by the current PSW.

The Central Processor executes programs at two levels; the user level and the "micro" level. At the user level, the Central Processor accomplishes the work required by the user. For the purposes of this discussion, the user may be considered to be the people and the subsystems external to the Central Processor. The micro-level program executes micro-instructions in sequences which are built into the solid state Read-Only Memory (ROM). The operation code of each user instruction directs the Decoder ROM (DROM) to start the micro-program sequence which will emulate the user instruction. The DROM does this by loading the ROM starting address of the sequence into the ROM Address Register. Other micro-program sequences in the ROM handle the interrupt monitoring, Control Console, and housekeeping operations. The Processor control logic initiates the execution of these sequences.

The Processor hardware includes the logic necessary to execute the set of 16 micro-instructions as they are held in the ROM Data Register. The micro-program sequences are often referred to as "firmware" to indicate that they exist at some plane between "hardware" and "software".

For a more detailed description of the 3010/2 Central Processor, including a description of the user instruction set, interrupt handling, PSW control, and Control Console operating procedures, refer to the GE-PAC 3010/2 Central Processor Reference Manual, GET-6174.

4.2.1 Principal Processor Components

S Bus and B Bus. These two busses are 16-bit common tie points for the data destined to and from most of the registers and interfaces in the Processor. Most data is handled on a 16-bit halfword basis or in the form of an 8-bit byte. Usually the S Bus is the source of data destined to a Processor register. The B Bus is an intermediate destination for data from various Processor registers, core, and I/O interfaces, which may be modified by the B Shifter and the Arithmetic Logic Unit, on its way to a Processor register or core, via the S Bus.

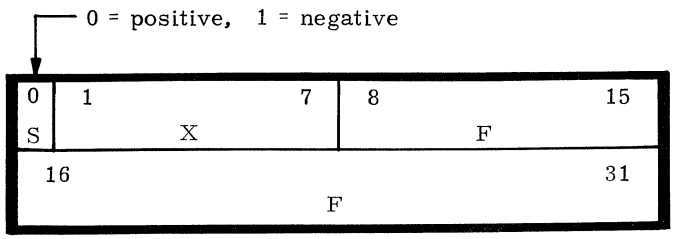


Fig. 4.1-2 Floating Point Data

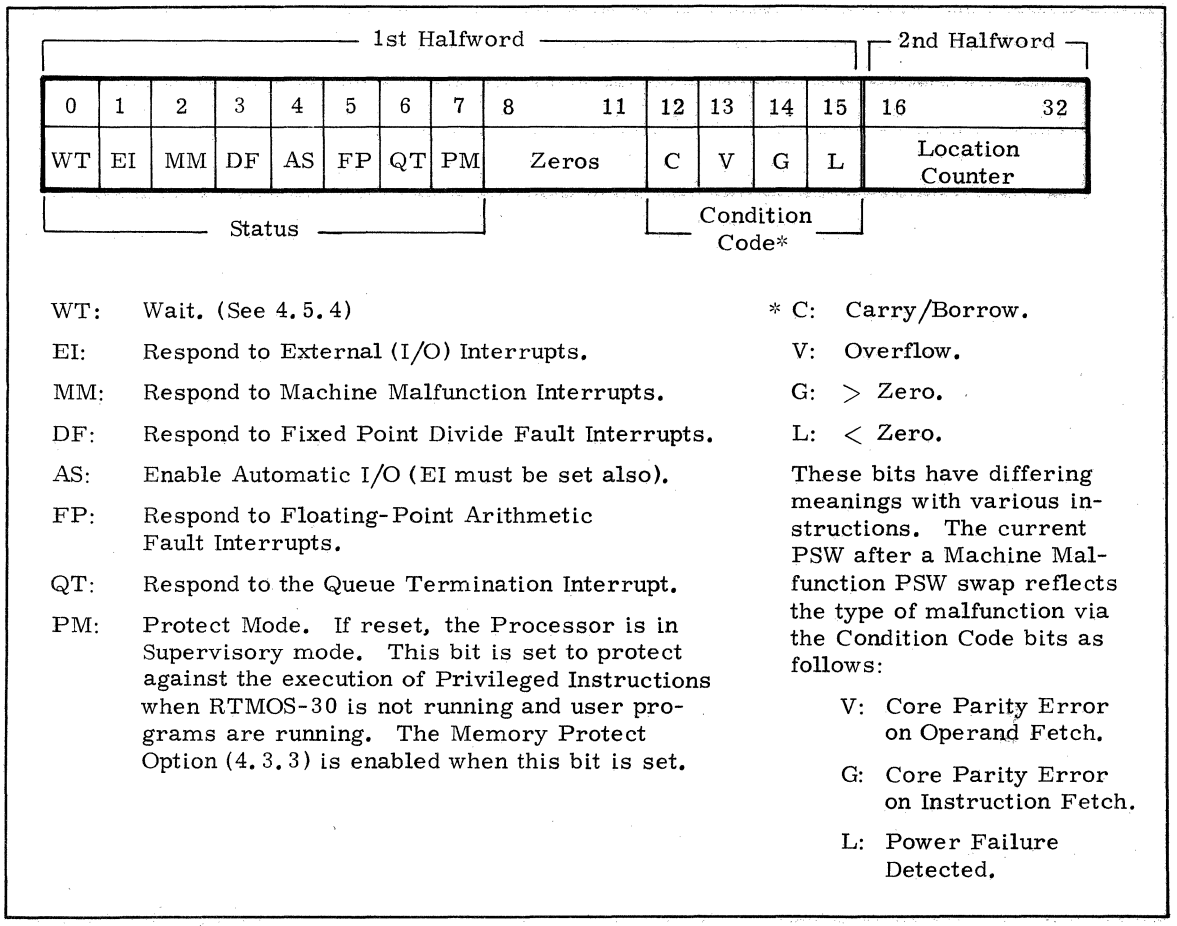


Fig. 4.2-1 Program Status Word

Instruction Register. This register holds the user instructions while they are decoded and executed.

Decoder ROM (DROM). The DROM translates the operation code of each user instruction held by the instruction Register to ROM addresses for entry into the micro-program sequence which emulates the user instruction. It contains 256 12-bit ROM address words.

Flag and Alarm Register. Four flag flip-flops record the result of user instruction execution for entry into the condition code of the current PSW. These flags are designated Carry/Borrow, Overflow, Greater than Zero, and Less than Zero, and reflect these conditions after arithmetic operations. The flag bits have differing meanings after execution of other user instructions. As an example, I/O instructions which cause the I/O controller status to be returned to the Processor copy the four least significant bits of the status byte into the condition code of the current PSW. Three alarm flip-flops record detected parity errors on operand fetches, instruction fetches, or a detected power failure. Any of these alarms causes a Machine Malfunction Interrupt and PSW swap. After the PSW swap, the new current PSW condition code reflects the type of malfunction, as indicated on Fig. 4.2-1. After a successful restart following a power failure detection, the condition code bits of the current PSW are all reset.

Register Stack. The register stack consists of 20 independent working registers for temporary data storage by the user program and the micro-program. Four of these 16-bit registers are dedicated for use by the micro-program only and the fourth of these stores the Location Counter halfword of the current PSW. The remaining 16 registers are General Purpose registers for use by the user program. All General Registers except General Register 0 may be used for indexing. General Register 0 cannot be used for indexing because the user instruction index field (bits 12 through 15) must be non-zero to specify indexing.

A Register. This register provides one 16-bit operand for the Arithmetic Logic Unit. The other ALU operand is derived from the B Bus via the B Shifter.

Arithmetic Logic Unit (ALU). The ALU performs arithmetic and logical functions required by the micro-instructions. The B Shifter manipulates the second operand prior to entry to the ALU, as required by the micro-instructions. The shifter may shift left, right, or may exchange the two byte in the B Bus halfword (cross shift).

Fullword Shift Register, SRH/SRL. SRH and SRL are interconnected to form a 32-bit shift register which is used in double precision operations such as shift, rotate, multiply, and divide.

Read-Only Memory. The ROM stores 1536 16-bit micro-instruction words. The micro-instruction words are loaded into the ROM Data Register from the address specified by the ROM Address Register. The ROM Data Register holds the micro-instruction word while it is interpreted and executed by the Processor control logic. The ROM consists of 24 high speed integrated circuits, each of which contains 256 4-bit digits. These are arranged into six pages, each of which contains 256 16-bit ROM data words. The data patterns are built into the integrated circuits. The micro-instruction cycle time is approximately 250 nanoseconds. The 256 12-bit DROM words are contained in three similar integrated circuits.

Multiplexer Channel and Bus. The Multiplexer Channel provides the Processor's interface to the Multiplexer Bus. The Multiplexer Bus is a universal interface to all of the 3010/2 system's I/O controllers except those connected to the Selector Channel Bus and possible custom designed Direct Memory Access Channels. The Multiplexer Bus provides an identical control signal and Data (D) Bus interface to all I/O controllers, including the Universal Clock (4.9), the Automatic Memory Protect Controller (4.3.3), all peripheral device controllers, remote communications controllers, and all process I/O controllers. The Multiplexer Bus control signals are actuated by the Processor control logic as directed by the micro-program. The D Bus is a 16-bit bidirectional bus which may transfer byte or halfword data in either direction. Output data is derived from the S Bus and input data is transferred to the B Bus. The physical location of the controllers on the bus determines the interrupt priority (4.4.2). The basic Multiplexer Bus may serve up to 16 I/O controllers. The Bus Extension and Switching options described in Section 5 of this manual may be used to extend the bus to the maximum of 253 controllers (in addition to the built-in Teletypewriter Controller and Control Console Controller) and to permit a common Multiplexer Bus section to serve more than one Central Processor.

Control Console Controller. The Programming and Maintenance Control Console is operated as a device and controller connected to the Multiplexer Bus. A micro-program sequence is dedicated to the operation of the console. The console controller is built into the Processor and is assigned device address X'01'*.

* The notation "X' ' ", indicates that the digits between the ' ' marks are expressed in hexadecimal form.

Refer to 4.5 in this manual for a description of the console and controller and to Section 7 of the 3010/2 Central Processor Reference Manual, GET-6174, for detailed operating instructions.

Teletypewriter Controller. The built-in Teletypewriter Controller provides a standard 20 milliampere current loop interface to a 3000AE12 ASR 33, ASR 35, or KSR 35 Teletypewriter. The controller is the second device on the Multiplexer Bus and is assigned device address X'02'. Teletypewriters and the operating sequence are described under 8.1 in this manual.

4.3 CORE MEMORY

Core Memory stores user instructions and data currently in use by the running program. If the system includes a bulk memory subsystem such as Drum or Disc Memories, user programs and data may reside in bulk memory, to be transferred to Core Memory as they are needed.

This memory is a three-wire, coincident current, random access, core memory. The basic Central Processor chassis contains the first 8K byte module ($K = 1024_{10}$) in each system. The maximum core size is 64K bytes, implemented as eight 8K memory boards (Model No. 3010AC1401 or AC1402). If implemented, the second, third, and fourth core modules are installed in the basic Central Processor Chassis. The fifth through eighth core modules are installed in a 15" universal expansion chassis, which is installed immediately below the Central Processor chassis in the Central System Cabinet.

The total Core Memory cycle time, including access and restoration, is 1.0 microseconds. The access time is 300 nanoseconds. Each 8K byte core module contains 4096 16-bit halfwords, and either byte in any halfword may be directly addressed by the Processor. Where both the Processor and a Selector Channel (Section 6 of this manual) are contending for memory access at the same time, the cycle is "stolen" from the Processor and the Processor waits while the Selector Channel is granted access. In addition to the core access channel used by the Processor, four other direct memory access channels are available. The Processor is always assigned the lowest priority and the Selector Channels (or possible custom designed direct memory interfaces) on the four direct access channels are assigned descending priorities from the first implemented to the fourth.

4.3.1 Core Memory Format and Addressing

Each of the possible 65,536 8-bit bytes in Core Memory is directly addressable by the Processor, as the user instruction operand addresses are all 16 bits in length. Each of the user instructions may require a byte, a halfword, or a fullword to be read from, or stored in core. However, each read or write cycle transfers one 16-bit halfword. The user instructions may utilize one byte from each halfword, the full halfword, or two successive halfwords.

The core addresses are assigned as successive hexadecimal byte addresses starting with 0000_{16} and ending with $FFFF_{16}$. A group of bytes combined to form a halfword or fullword is addressed by the lowest numbered byte address in the group. Halfword or fullword operands in core must be positioned at even numbered byte addresses. Because of assembler and listing format considerations, all operand addresses, including byte addresses are even numbered. Table 4.3-1 provides some examples of the core addressing scheme.

Should a core location higher than any implemented in a system be addressed, the memory cycle will occur, but the data will be lost on a write operation and all zeros will be read on a read operation.

4.3.2 Parity Option

Each core module implementing the Parity Option (Model No. 3010AC1402) includes a seventeenth bit which stores an "odd ones" parity bit with each halfword. The Processor contains logic which stores a binary one in the parity bit if the number of "one" data bits is even on a Processor write operation. The Processor checks for correct parity on each Processor read operation. If parity error is detected on a read operation, and if the Machine Malfunction Interrupt is enabled (PSW bit 2 set), a Machine Malfunction Interrupt and PSW swap occurs. If the "Machine Malfunction - New PSW" is successfully retrieved, the new PSW initiates an error recovery routine. The condition code field of the new PSW indicates the type of error as indicated on Fig. 4.2-1.

It is possible to have a mixture of 8K-byte core modules containing the parity bit and 8K-byte modules without the parity bit in the same system.

4.3.3 Automatic Memory Protect Option

The Automatic Memory Protect Controller (Model No. 3010AB3401) is an I/O controller installed on the Multiplexer Bus. It stores a Core Memory protection pattern provided by a user program. The memory protect controller continuously monitors the seven most significant bits of the Processor's Memory Address Register, and when a non-privileged Core Memory write operation is attempted by the Processor into one of the protected areas, the memory protect controller causes the Processor to convert the write cycle to a read cycle, attempts to interrupt the Processor, and sets bits 3 and 5 of the Automatic Memory Protect controller status byte.

Normally, the Automatic Memory Protect Controller is wired to protect 64 blocks of 1024 Core Memory bytes per block. This provides programmable protection for the largest available 3010/2 Core Memory (64K). A simple wiring change may be made in the

	FULLWORD				FULLWORD			
	HALFWORD		HALFWORD		HALFWORD		HALFWORD	
	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE
HEXADECIMAL ADDRESS	0050	0051	0052	0053	0054	0055	0056	0057
CORE CONTENTS	01	23	45	67	89	AB	CD	EF

If a user instruction specifies an operand address of 0050_{16}:

For a byte-oriented instruction the operand is 01_{16}.

For a halfword-oriented instruction the operand is 0123_{16}.

For a fullword-oriented instruction the operand is 01234567_{16}.

If a user instruction specifies an operand address of 0052_{16}:

For a byte-oriented instruction the operand is 45_{16}.

For a halfword-oriented instruction the operand is 4567_{16}.

For a fullword-oriented instruction the operand is $456789AB_{16}$.

Table 4.3-1 Core Memory Addressing

factory or in the field to change the block size to 512 bytes or 2048 bytes. Protection for 64 512-byte blocks provides protection to the first 32K bytes of core. Since there is no core above 64K, only 32 blocks are available if the 2048-byte block size is chosen.

Operating Sequence

The program sets up the memory protect controller by issuing an appropriate Output Command to the controller (Fig. 4.3-1) and then issuing up to eight Write Data instructions that transfer the appropriate 64-bit protection pattern as eight 8-bit bytes. The standard device address for the controller is X'AE', but the address may be changed by jumper wiring on the controller board.

Any Output Command issued to the controller resets a Write Data byte counter in the controller, and the first Write Data byte transferred to the controller following the Output Command transfers the protection pattern for the first eight blocks of core. If the block size is 1024 bytes, this first byte covers the first 8,192 core addresses (0000 through X'1777'). The first bit in the first data byte protects the lowest block of core, if it is set, and the remaining bits protect successively higher blocks. Subsequent 8-bit data bytes protect successively higher core areas of 8 blocks each. Should nine or more data bytes be transferred to the controller before the next Output Command, the protection pattern is overwritten, beginning with the lower core addresses.

Core Memory protection is activated only when the Processor is in the Protect Mode (PSW bit 7 set). Since the attempted execution of a privileged instruction while in the Protect Mode causes a Protect Mode violation interrupt before the instruction is executed (4.4.1), a memory protect violation can be detected only when a memory write is attempted during the execution of a non-privileged instruction. The Automatic Memory Protect Controller interrupts the Processor upon detection of a memory protect violation if bit 1 of the current PSW is set and if the last Output Command to the controller enabled the interrupt.

Since the program must use privileged instructions (4.4.1) to set up the memory protect controller and to respond to its interrupt, PSW bit 7 must be reset while instructions are issued to the controller. After the protection pattern has been specified, PSW bit 7 must be set to specify Protect Mode and to enable the detection of a memory protect violation.

Output Command instructions issued to the controller reset the data byte counter and transfer a command byte which specifies the modes of operation as follows (Fig. 4.3-1):

- Bits 0 and 1 = interrupt disarm and enable respectively. When enabled the interrupt queue flip-flop is set when a memory protect violation is detected. When disarmed, the memory protect controller's interrupt queue flip-flop is reset.

- Bit 2 = 1 = Protect On. PON specifies that the core areas specified by the protection pattern are to be protected. The 64-bit protection pattern may be changed by issuing up to eight data bytes to the controller via Write Data instructions.

- Bit 3 = 1 = Protect Off. POF overrides the memory protection. This command might be used to disable memory protection temporarily while the Processor remains in the Protect Mode.

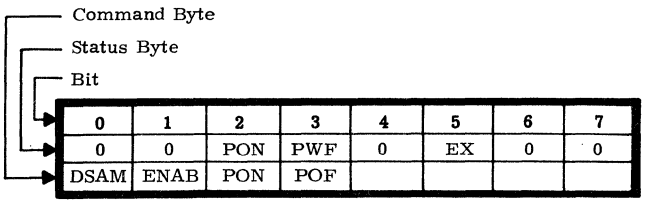
Sense Status instructions issued to the controller cause a status byte to be returned to the Processor as follows (Fig. 4.3-1):

- Bit 2 = 1 = Protection On. PON is set when protection has not been overridden by a POF Output Command.

- Bit 3 = 1 = Protect Write Flag. PWF sets when a memory protect violation is detected. PWF is reset by an Output Command, an Acknowledge Interrupt instruction, or when the INT button on the Control Console is pushed to initialize the hardware.

- Bit 5 = 1 = Examine. EX = PWF.

When the system hardware is initialized (4.5.3), the memory protect controller interrupt is disarmed, protection is overridden, the PON and PWF status bits are reset, and the protection pattern is unchanged. A power failure, restart, and hardware initialization (4.7), leaves the protection pattern register in an uncertain state because it is not initialized. The program should reestablish the protection pattern following a power failure and restart.



0	1	2	3	4	5	6	7
0	0	PON	PWF	0	EX	0	0
DSAM	ENAB	PON	POF				

Fig. 4.3-1 Automatic Memory Protect Controller Command and Status Bytes

4.4 INTERRUPTS

Interrupt signals request that the current Processor status be saved, and that the Processor branch to a service or corrective routine. Interrupts may originate within the Processor or outside the Processor. When the routine requested by the interrupt is completed, the status may be restored and the interrupted program may resume.

When an interrupt is serviced, the content of the Processor's PSW register is stored in a dedicated "old PSW" core location, and a new PSW pointing to the servicing routine is loaded into the PSW register. When the service routine is completed, the PSW register may be loaded with the old PSW and the interrupted program may resume.

The Processor's response to interrupts is under the control of the Program Status Words. The current PSW, which is stored in the Processor's PSW register, defines the current status, and controls the response to seven of the interrupt types. The following is a list of the types of interrupts and the PSW bits which control the seven inhibitable types. The program may permit interrupt servicing by setting the appropriate control bits and may inhibit interrupt servicing by resetting control bits. The I/O Controllers on the Multiplexer Bus store (queue) interrupts until they are acknowledged, unless they are disarmed by an Output Command issued to the controller. Output Commands may disable interrupts from some controllers, but allow the interrupt queue flip-flop to store the interrupt.

Type	Internal or I/O Control	PSW Control Bits
External	I/O	1
Machine Malfunction	Int.	2
Fixed Point Divide Fault	Int.	3
Automatic I/O Service	I/O	4
Floating Point Arithmetic Fault	Int.	5
Channel Termination	I/O	6
Protect Mode Violation	Int.	7
Illegal Instruction	Int.	Not Inhibitable
Termination Queue Overflow	I/O	Not Inhibitable
Supervisor Call	Int.	Not Inhibitable

For a detailed description of the use of interrupts and the Central Processor's responses, see Subsection 2.4 of the GE-PAC 3010/2 Central Processor Reference Manual, GET-6174. The following paragraphs describe the aspects of interrupt configuration, servicing, and priorities of particular significance in relating the descriptions of the 3010/2 functional subsystems in this General Description to the interrupt structure.

4.4.1 Protect Mode

Where the on-line system programs are under the control of an operating system such as RTMOS-30, the operating system normally runs in the Supervisory Mode with bit 7 of the current PSW reset. This allows the operating system to execute privileged instructions and to write in any area of Core Memory. The user level programs controlled by the operating system normally run in the Protect Mode with bit 7 of the current PSW set, which enables the memory protect option (4. 3. 3) and prevents the execution of privileged instructions.

Normally, only the operating system has the privilege of executing the subset of I/O and system control instructions: Auto Load, Write Data, Read Data, Sense Status, Output Command, Acknowledge Interrupt, Exchange Program Status, Load Program Status, Simulate Interrupt, and all variations of these types of instructions. If, when in the Protect Mode, an attempt is made to execute one of these privileged instructions a Protect Mode interrupt occurs. If such an interrupt occurs, the instruction is not executed, the location counter in the current PSW is not incremented, and the old PSW stored as a result of the PSW swap points to the location of the privileged instruction which caused the interrupt.

If the Automatic Memory Protect Controller (4. 3. 3) is implemented, and should a program running in the Protect Mode attempt to write in an area defined for protection by the pattern held by the controller, the memory protect controller will attempt to generate an external interrupt. If the interrupt is not disarmed, and if the current PSW has bit 1 set, the interrupt will be serviced. Regardless of the memory protect interrupt status, the protection feature will prohibit writing in the protected area, and if the program is not interrupted, instruction sequencing will continue.

4.4.2 I/O Interrupts

The Central Processor can be interrupted by any of the I/O controllers on the Multiplexer Bus to which it can address instructions. Since all I/O controllers sense the address in a single 8-bit byte, the Central Processor may address up to 256 devices. Since every Processor has a built-in Control Console Controller and a Teletypewriter Controller, and since most 3010/2 systems implement the Universal Clock Controller (4. 9), 251 addresses are left to accommodate additional input/output controllers of all types (address X'00' is not available).

I/O interrupt priority is determined by the electrical location of the controller on the Multiplexer Bus, and not by the device address. When the Processor is interrupted, it sends an Acknowledge pulse down the Multiplexer Bus. When the pulse encounters the controller with its interrupt queue flip-flop set, the pulse is stopped and the controller returns its device address to the Processor to indicate which controller originated the interrupt.

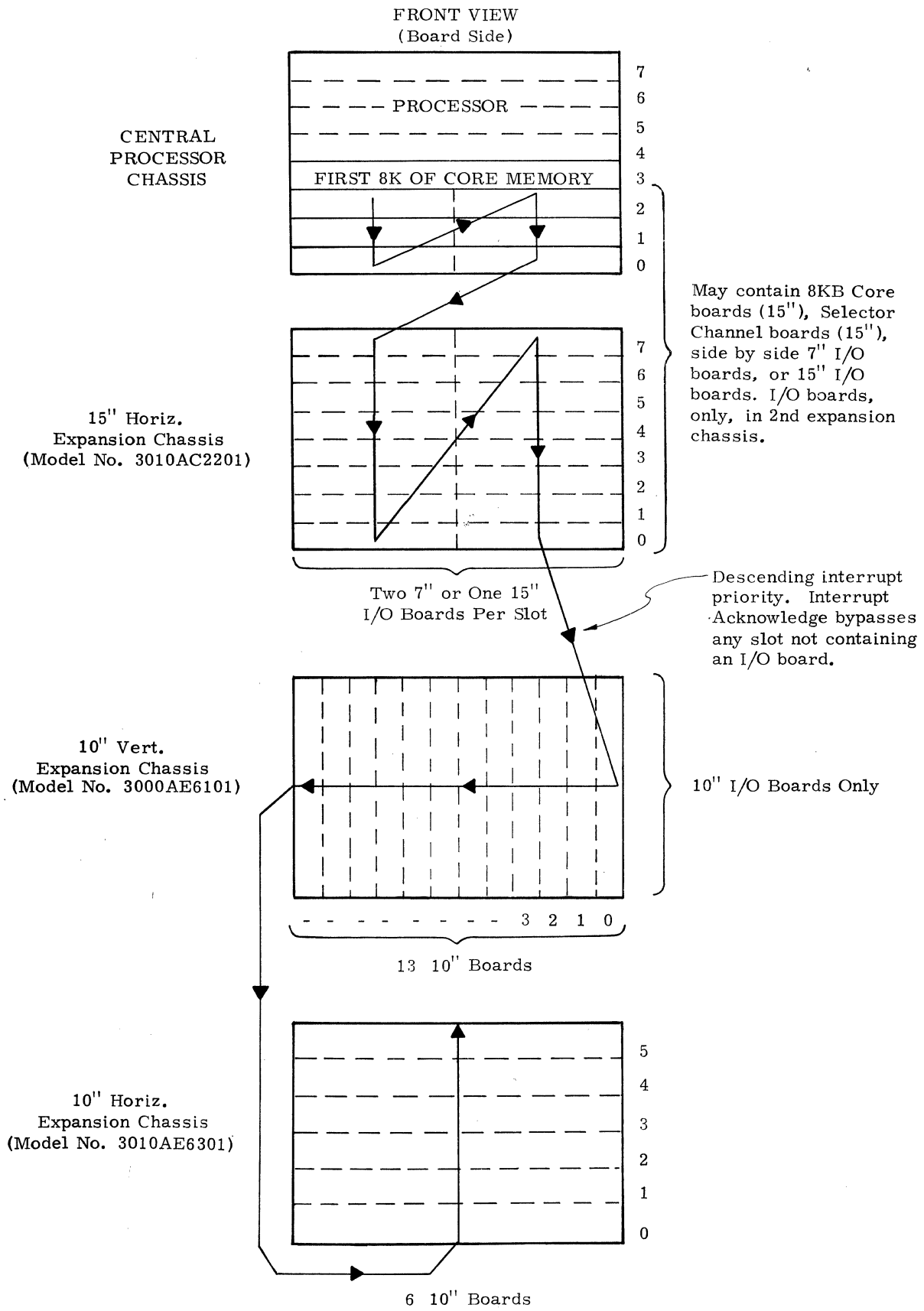


Fig. 4.4-1 I/O Interrupt Priorities

The Acknowledge pulse may be generated by the micro-program if Automatic I/O service is enabled (PSW bits 1 and 4 set), or it may be generated by the execution of an Acknowledge Interrupt instruction by the program (PSW bit 1 set and 4 reset). Since the Control Console interrupt is a special type of interrupt (4.5) and is not on the I/O interrupt priority chain, the built-in Teletypewriter Controller has the highest priority. If implemented, the Automatic Memory Protect Controller board is assigned to the Multiplexer Bus slot with the next highest interrupt priority. The Universal Clock board is normally mounted to the right of the memory protect board, so it is eight slots down the bus from the memory protect controller, if these boards are in an expansion chassis.

The Acknowledge pulse and interrupt priority travels first down the left side (front view) of the chassis which accept 15" horizontally mounted board assemblies. After it passes through the lower-left slot, it goes to the top-right slot in the same chassis, and then down the right side. The interrupt priority travels from the right to left (front view) in chassis which accepts 10" vertically mounted boards. Fig. 4.4-1 illustrates this scheme.

4.4.3 External Interrupt Module

Up to four 3000AF12 External (8-Line) Interrupt Modules may be implemented as I/O controllers on the Multiplexer Bus. Each such module provides an interface to as many as eight external interrupt terminations. The inputs are typically connected to terminations in the Central System Cabinet and may be relay isolated. Power (12 VDC) and contacts to control the relays are provided by the user, or the interrupts may be derived from the optional 3010AF16 Change Detect Digital Input Terminations (see 11.1.1).

Each external interrupt implemented uses one I/O Multiplexer device address. The external interrupts are armed or disarmed and masked or unmasked by Write Data instructions addressed to the lowest device number assigned to the module. Four such lowest device numbers are possible: X'20', X'28', X'30', and X'38'. Once initialized by pushing the Initialize button the Display Panel or issuing an Output Command to the interrupt module, the first Write Data instruction specifies which interrupt lines are to be armed or disarmed and the second Write Data instruction specifies which interrupts are to be masked or unmasked. Bits 0 through 7 of the data byte correspond to interrupts 0 through 7, with interrupt 0 having highest priority. Successive Write Data instructions are presumed to transfer arm/disarm and mask/unmask bytes, respectively.

A bit set in an arm/disarm byte allows the corresponding interrupt queue flip-flop to set when the corresponding relay energizes (if relay buffered). A bit set in a mask/unmask byte allows the interrupt to be applied to the Processor, and to be serviced if bit 1 of the current PSW is set. The lowest device address implemented on an External Interrupt Module is selected with jumper wiring on the module, and determines the device address corresponding to interrupts 0 through 7 as follows:

X'20' through X'27'.

X'28' through X'2F'.

X'30' through X'37'.

X'38' through X'3F'.

When the External Interrupt Module is initialized, all eight interrupts are disarmed and masked.

4.5 PROGRAMMING AND MAINTENANCE CONTROL CONSOLE

The Central Processor's Control Console allows direct communication with the machine by programming and maintenance personnel. It communicates with the Processor through the built-in Control Console Controller, which is an I/O controller on the Multiplexer Bus. The Control Console functions are effected by a micro-program sequence which is initiated by the console interrupt. The interrupt is generated when the EXEcute switch on the console is pushed. The running program may communicate with the console by issuing I/O user instructions to the Console Controller (device address X'01'). The console interrupt is not a normal I/O interrupt, and can be serviced by the program only if bit 4 of the current PSW is set. For additional console programming considerations, see 7.4 in the 3010/2 Central Processor Reference Manual, GET-6174.

Two register displays are provided and all 16 of the General Purpose Registers may be selected for display, two at a time. The displays can also display the current PSW, the next instruction to be executed, and the contents of any Core Memory location. The console's rotary selector selects the type of operation and display to be in effect the next time EXEcute is pushed. The panel also features a hardware initialize switch, a single step mode switch, a run switch, and 16 data switches.

4.5.1 Function Switches

Three function switches are used to select the Central Processor's mode of operation: Single (SGL), RUN, and a rotary selection switch. These three switches are used to place the Central Processor in one of six modes. All three switches must be placed in the correct position prior to pushing EXEcute to select a new mode. The six modes and the switch positions which select them are as follows (detailed console operating procedures are in Chapter 7 in the 3010/2 Central Processor Reference Manual, GET-6174):

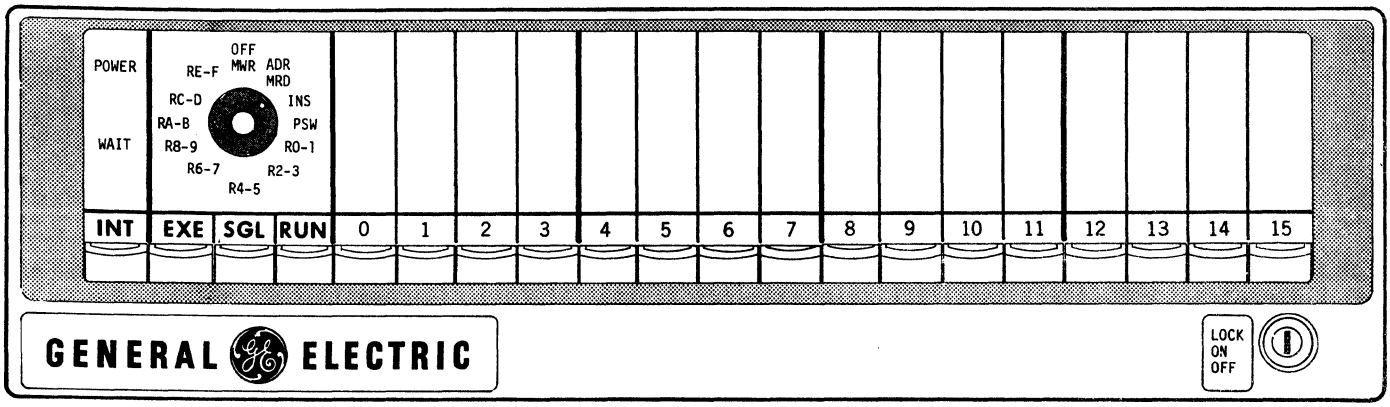


Fig. 4.5-1 Control Console

Address Mode. SGL-up, RUN-up, rotary to ADR/MRD; this mode is used to place an address in the location counter of the current PSW. The desired address must be placed in the 16 data switches and the function switches must be positioned before EXEcute is pushed to enter the address.

Memory Read Mode. SGL-down, RUN-up, rotary to ADR/MRD; this mode is used to read the contents of the core address specified by the location counter of the current PSW. When EXEcute is pushed, the upper console display shows the address plus 2, and the lower display shows the contents of the location specified before the location count was incremented. Subsequent depressions of EXEcute transfers consecutive memory halfwords into the lower display and increment the address by 2.

Memory Write Mode. SGL-down, RUN-up, rotary to OFF/MWR; this mode is used to write the content of the 16 data switches into the core address specified by the location counter of the current PSW. When EXEcute is pushed, the upper console display shows the address plus 2, and the lower display shows the data written into the location specified by the location counter of the current PSW before it was incremented. Subsequent depressions of EXEcute cause the data switch contents to be written into consecutive memory halfwords and increment the address by 2.

Single Mode. SGL-down, RUN-down, rotary to any position except OFF/MWR or ADR/MRD. This mode is used to execute one instruction each time execute is pushed. The rotary switch may be used to select any pair of the general registers, the PSW, or the next instruction to be executed for display. When the registers are displayed, the even numbered register is in the upper display, and the odd is in the lower display. In the PSW position, the status and condition code halfword is in the upper display, and the location counter is in the lower display. In the INS position, the next instruction is in the upper display and the core halfword following that instruction is in the lower display.

Halt Mode. SGL-up or down, RUN-up, rotary to any position except OFF/MWR or ADR/MRD. This mode is used to view various displays selected by the rotary switch without incrementing the location counter and executing instructions. The displays are the same as in Single Mode. If a display is selected, EXEcute must be pushed to make the change. When this mode is in effect, the WAIT indicator is lit. The WAIT indicator is also on when the program resets PSW bit 0 but, that state is interruptible, while the HALT mode wait state is not. The HALT mode is left by entering one of the five other modes.

RUN Mode. SGL-up, RUN-down, rotary to any position except OFF/MWR or ADR/MRD. This is the mode in which the program runs at normal speed. The two displays remain unchanged unless the program changes them via the console controller. The program may also read the content of the data switches in this mode and the Single Mode.

4.5.2 Data Switches

The 16 data switches line up below the corresponding bit indicators in the two displays. These are alternate position switches. A data switch in the "down" position enters a "one" into the corresponding bit in the PSW location counter when EXEcute is pushed upon entering the Address Mode or while in the address mode. When in the Memory Write Mode, data is written into the location specified by the current PSW. A data switch in the "up" position (as shown on Fig. 4.5-1) enters a "zero" in the corresponding bit position.

4.5.3 Initialize Switch and Keyswitch

The Initialize switch (INT) is a momentary switch which initializes the GE-PAC 3010/2 system hardware when pushed. Depression of INT starts a microprogram sequence which stores the contents of all of the General Registers and the complete PSW in dedicated core locations. When the initialize circuit is released, all of these registers are restored, and if

bit 2 of the PSW is reset (Fig. 4.2-1) program sequencing can resume from the point at which it was stopped. If PSW bit 2 is set, a Machine Malfunction Interrupt PSW swap takes place. Initialization resets all interrupt queue flip-flops in the I/O controllers and places all system hardware in a known state. Note, however, that initialization does not clear out the PSW nor the General Registers. The condition code should be checked before starting a program to see if the status and condition code are appropriate. If not, the PSW should be changed by loading a new PSW from core. See 7.3.4 in the 3010/2 Central Processor Reference Manual, GET-6174 for detailed instructions on program execution.

The keyswitch is a security lock which prevents unauthorized tampering with the console controls. When the key is inserted and rotated fully clockwise (LOCK) power is on and the console controls are locked out. When in the ON position, power is on and the console controls operate. When in the off position, power is off. If power is turned off and then back on, the system is initialized as described in the preceding paragraph. When power is on, the POWER indicator on the console is lit.

4.5.4 Wait State

The Wait State is a state where the Program or the micro-program is waiting for some external event, such as operator intervention, to occur. When the Processor is placed in the Wait State, the WAIT indicator on the console lights and instruction sequencing stops. The Processor can be placed in the Wait State in one of three ways:

- The program sets bit one of the current PSW.
- The Control Console is in the Halt Mode or is in the Single Mode and no instruction is in the process of execution.
- The INT switch is pushed while the console Function Switches are not set up for the Run Mode.

The program initiated Wait State is typically entered when the program requires some operator intervention before instruction sequencing can resume. Since the console controls would normally be set up to select the Run Mode when the program entered the Wait state, the operator can restart instruction sequencing after the necessary action has been taken by pushing EXEcute. Any enabled interrupt may also cause a PSW swap which would take the Processor out of the program initiated Wait State.

The console initiated Wait State (Single Mode or Halt Mode) is left by selecting another mode and pushing EXEcute.

4.6 INPUT/OUTPUT SUBSYSTEM

The principal elements of the Central Processor's Input/Output Subsystem are the Multiplexer Channel and Bus. The Multiplexer Channel and Bus provide a total of 30 data and control lines to each attached peripheral device controller, remote communications controller, or process I/O controller. When an optional Selector Channel (Section 6) is implemented, the Multiplexer Bus is connected through to the controllers on the Selector Channel's private bus when the Selector Channel is in the idle mode.

The basic Multiplexer Bus can serve up to 16 I/O controllers. The Multiplexer Bus Extension and Switching options described in Section 5 of this manual may be implemented to serve up to the maximum of 255 controllers, including the Control Console Controller and Teletypewriter Controller, which are built into the Processor. Extended portions of the bus may be located in the Central System Cabinet or in adjacent cabinets.

I/O controllers are manufactured in four basic forms:

- One controller on a 7" x 15" board which occupies 1/2 of a slot in a 15" horizontal air-flow chassis.
- One controller on a 15" x 15" board which occupies a full slot in a 15" horizontal air-flow chassis.
- One controller on a 10" x 10" board which occupies one slot in a 10" vertical air-flow chassis, one slot in a 10" horizontal air-flow chassis, or is adapted to one slot in a 15" horizontal air-flow chassis (using adapter no. 3010AE80001).
- One controller on multiple 10" square boards, which must be installed in adjacent slots in a 10" horizontal air-flow chassis, or a 10" vertical air-flow chassis.

Some 10" boards may employ mercury-wetted relays and must be mounted within 30° of vertical. Such boards must be installed in a 10" vertical air-flow chassis. The Multiplexer Bus Switch (Section 5) is one such board.

The physical form of each available controller is described in the GE-PAC 3010/2 Price List and in the 3010/2 Hardware Configurator, PCP-230. Any controllers on the portion of the Multiplexer Bus in the basic Central Processor chassis must be 7" or 15" horizontal types, or must be 10" boards in an adapter. Three types of expansion chassis are available:

- 15" Horizontal; accommodates up to 8 15" or 16 7" boards.

- 10" Horizontal; accommodates up to 6 10" boards, horizontally mounted.

- 10" Vertical; accommodates up to 13 10" boards, vertically mounted.

Input/output data on the Multiplexer Bus are transferred in the form of 16-bit halfwords or 8-bit bytes. Only controllers of the 7" and 15" form are capable of transferring halfword data and many of them use 8-bit bytes, only. The data lines on the 15" portion of the bus are 16 bidirectional lines. Most 10" controllers interface with 8 input lines and 8 output lines, and the conversion to this type of data interface is made in the cables which transfer the bus from the 15" portion to the 10" portion.

I/O operations and data transfers may be controlled entirely by the program or may be effected by the Automatic I/O micro-program under the control of the operating system and user level programs. When program controlled, user instructions address the appropriate controller, sense the status of the controller, transfer commands to the controller, and read from or write into the controller. Program controlled I/O may be interrupt driven or may rely upon status sensing to determine device availability, readiness for data transfer, alarm status, etc. Refer to Chapter 5 in the GE-PAC 3010/2 Central Processor Reference Manual, GET-6174, for a detailed description of the I/O subsystem and its operation.

4.7 POWER FAILURE DETECTION AND AUTOMATIC RESTART OPTIONS

The primary AC supply to the Central Processor is monitored by the optional Power Fail Detector. Should the line voltage decrease to 95 VAC or less, or should power be lost for more than one AC cycle, hardware initialization including register and PSW storage as described under 4.5.3, takes place. If power returns before the power control circuits have dropped the connection of the AC input to the power supplies, system operation can resume as if uninterrupted. If bit 2 of the current PSW is set, a Machine Malfunction interrupt and PSW swap takes place.

Should power be off long enough for the AC connection to break, the Automatic Restart circuit, which is provided with the Power Fail Detector, causes the power control circuits to reconnect the AC input to the power supplies, bringing system power back up.

A Restart Inhibit Timer is available (Model No. 3010AB1401) to inhibit an automatic restart after power has been off so long that a safe restart of the computer's control of the process cannot be made without manual intervention. The inhibit timer is manually adjustable to any interval from 10 seconds to 10 minutes.

The micro-program routine which stores the General Registers and PSW in core during a power-down sequence inhibits further operations by the Processor when it is concluded. Since all system functions are initialized, no further attempts to read from or write in core are made. Core memory retains the information it has stored until power returns.

If bit 2 of the current PSW is set and a Machine Malfunction interrupt occurs, the software routine initiated by the PSW swap must determine if it was initiated by an automatic restart or another malfunction such as a core parity error. Note that, as shown on Fig. 4.2-1, the condition code of the new PSW reflects the type of malfunction in the V, G, and L bits of the condition code. On resumption of program sequencing, the condition code can be cleared out by exchanging or loading a new PSW or by executing an instruction which effects the condition code.

4.8 SYSTEM ALARMS OPTION

The optional 3010AB33 System Alarms module provides a visual indication at the PWB front edge of six system alarm conditions. The alarm conditions may be sensed by the running program and are available as relay driver outputs from the module. The alarm module is a single 10" board, and may be mounted horizontally or vertically. The alarm conditions are:

- Power Failure. This alarm is set when the Power Fail Detector (4.7) detects a failure and when the system hardware is initialized during an automatic restart or by pushing the Initialize button on the Control Console.

- Stall Alarm. This alarm is set when the stall timer (4.8.1) times out.

- Parity Alarm. Sets when the optional core parity check logic (4.3.2) detects an error.

- Over-temperature Alarm. Sets when a temperature sensor in a Core Memory module detects an excessive temperature. The alarm point is set with a screwdriver adjustment on the System Alarms module. The adjustment range is from 40° C to 50° C.

- I/O Alarm. This alarm is set when the program issues a Write Data instruction to the System Alarms module with bit 6 of the data byte set. The meaning of this alarm is to be defined by the programmer.

- Programmable Alarm. This alarm is set when the program issues a Write Data instruction to the System Alarms module with bit 7 of the data byte set. The meaning of this alarm is to be defined by the programmer.

Each of these alarm conditions sets a bit in an Alarm Register and lights the corresponding lamp on the edge of the System Alarms Module PWB, as shown on Fig. 4.8-1.

The standard device address for the alarm module is X'18'. The address is selected by eight screwdriver actuated switches on the alarm module board.

4.8.1 Stall Alarm

The stall alarm feature is used to detect program or hardware malfunctions which cause a delay in program sequencing. If a program sequence delay exceeds the time period of the stall alarm timer, status bit 1 is set, and the System Alarms interrupt queue flip-flop sets. The timer is adjusted, by means of a screwdriver adjustment on the System Alarms module, to any period from 1 second to 5 seconds. An Output Command instruction which transfers a command byte with bit one set, restarts the timer. Such a command is placed at several appropriate points in programs which run with the timer enabled. If the stall alarm is set and bit one of the current PSW is reset, the PSW swap which occurs because of the System Alarms interrupt, may branch to a corrective routine. When the Processor acknowledges the interrupt, the queue flip-flop and the stall alarm status bit are reset, but the timer is not restarted.

A Stall Enable/Disable switch is provided on the front edge of the System Alarms PWB. In the Disable position, the switch locks out the stall alarm feature by resetting the timer and the interrupt queue flip-flop. Also, when in the Disable position, the switch lights the Stall Lockout indicator lamp and sets status bit 2 (Fig. 4.8-1).

4.8.2 Hardware Alarm

Alarm Register bit 5 (Fig. 4.8-1) is set when the Power Fail, Stall Alarm, Stall Lockout, and/or Parity Alarm bits are set. Three screwdriver actuated switches are provided on the System Alarms PWB to select the Over-temperature Alarm, I/O Alarm, and Programmable Alarm also, to set the Hardware Alarm indicator and relay driver, but not status bit 5.

Bit	0	1	2	3	4	5	6	7
Status Byte*	PWF	SALM	SLO	PTY	TEMP	HDW	I/O	PRGM
Command Byte	C	C		C			C	C
Relay Driver Alarm State	Off	Off	Off	On	On	On	On	On
Indicator Alarm State	On	On	On	On	On	On	On	On

Top — Bottom

* Transferred to Processor by Sense Status or Read Data Instructions.

PWF: Power Failure.

SALM: Stall Alarm.

SLO: Stall Lock-Out (Disable).

PTY: Core Parity Alarm.

TEMP: Overtemperature.

HDW: Hardware Alarm = PWF + SALM + SLO + PTY, (TEMP + I/O + PRGM Optional).

I/O: I/O Alarm.

PRGM: Programmable Alarm.

C: Clear the Alarm.

Fig. 4.8-1 System Alarms Command Byte, Status Byte and Alarm Indicators

4.8.3 Relay Driver Outputs

Each of the eight Alarm Register bits (Fig. 4.8-1) controls the state of a relay driver which may be used to provide an external indication of the alarm status. These outputs may be used to drive controls and indicators in external equipment such as process operator consoles.

When "on", each relay driver is capable of returning up to 200 milliamperes DC to a common return line. In the "off" condition, each driver can withstand up to +35V with respect to the common return. The drivers may be used to drive lamps directly if the inrush current, as occurs with incandescent lamps, does not exceed the maximum. A daughter-board location on the System Alarms PWB is reserved for the possible implementation of a daughter board with "keep warm" resistors, which would maintain a minimum current flow through the lamps while they are dark, minimizing the inrush current.

A 3010AF2401 Termination Assembly, into which a 3010AF2402 8-Point Output Relay Module is installed, is the standard relay interface with the alarm module. A +12 VDC power supply such as 3010AL35 or 3010AL38 is required to supply the relay power. The relay module requires a maximum of 350 ma of 12V power, so the power supply may be shared with other functions.

4.9 UNIVERSAL CLOCK

The Universal Clock module (Model No. 3010AF2401) provides a system time standard which may be derived from the primary AC input to the system, an internal 1 MHz ±0.01% oscillator, or an external time standard. The clock module is a standard controller which is installed on the Multiplexer Bus. It occupies one-half of a 15" horizontal board slot, and typically shares the slot with the Automatic Memory Protect Controller. The processor and program are notified of an elapsed time interval by an I/O interrupt from the clock module, and the clock module is normally assigned to the Multiplexer Bus slot which provides the eighth interrupt priority.

Functionally, the clock module is two independent I/O controllers; a Precision Interval Clock (PIC) and a Line Frequency Clock (LFC). The two controllers have separate addresses. The standard PIC address is X'6C' and the standard LFC address is X'6D'. The addresses may be changed by jumper wiring on the board, provided that the PIC address is always even and the LFC address is always odd. The interrupt logic on the clock module provides the first priority to the PIC and the second to the LFC.

4.9.1 PIC Operating Sequence

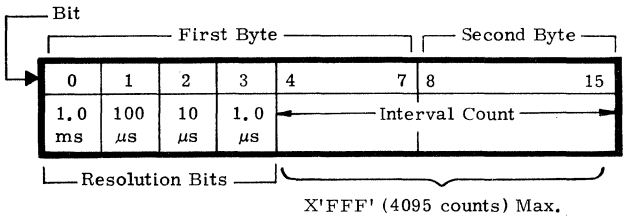
A typical PIC operating sequence is as follows:

1. Two Write Data instructions or one Write Halfword instruction transfers a resolution and interval count halfword to the PIC (Fig. 4.9-1), which is stored in an Input Buffer.

2. A Start Output Command (Fig. 4.9-2) is issued to the PIC, and that command transfers the content of the Input Buffer to the counter logic, leaving the Input Buffer unchanged.

3. The counter begins to decrement at the intervals specified by the resolution bit. When the count reaches zero, the PIC interrupt queue flip-flop is set if enabled, and the counter logic is reloaded from the input buffer.

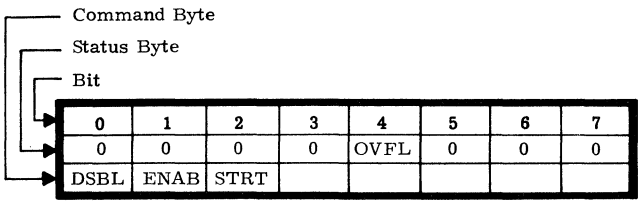
The PIC has an Output Buffer which reflects the current interval count. The contents of this buffer may be transferred to the Processor with two Read Data instructions or one Read Halfword instruction (Fig. 4.9-3). The contents of the Input Buffer, the counter logic, and the Output Buffer are unaffected by this interrogation of the Output Buffer, but the Input Buffer's byte count logic is toggled by any input or output byte transfer, so care must be taken to always use two Read Data instructions, two Write Data instructions, or single Read Halfword or Write Halfword instructions, so that the byte count will be zero when the byte containing the resolution bits is transferred to the Input Buffer.



X'1FFF' transferred to Input Buffer followed by a Start command with interrupts enabled would provide an interrupt every 4095 microseconds.

If more than one resolution bit is set, the lowest bit is used.

Fig. 4.9-1 PIC Resolution and Interval Bytes



DSBL: Disable the PIC interrupt but allow the queue flip-flop to store an interrupt.

ENAB: Enable the PIC interrupt.

STRT: Transfer Input Buffer to count logic and start counting.

OVFL: Interrupt Occurred between 1st and 2nd Write Data bytes.

Fig. 4.9-2 PIC Command and Status Bytes

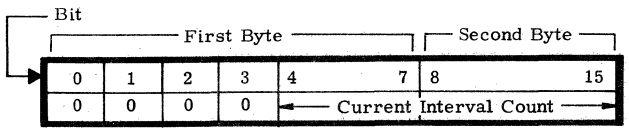


Fig. 4.9-3 PIC Output Buffer

The Input Buffer may be reloaded at any time without effecting the current count. However, should the interval counter go to zero between the transfer of the first byte and the end of the second byte transfer, bit 4 of the PIC status byte sets (Fig. 4.9-2) and counting stops. This Overflow bit is reset by a Sense Status instruction, and Acknowledge Instruction, or by hardware initialization. Counting is started at the new rate by a Start Output Command.

Hardware initialization leaves the PIC byte counter, resolution bits, and status byte reset. It also disables the PIC interrupt and stops the count.

If the Resolution bits are reset and a new Start command issued to the PIC, the count stops.

4.9.2 External Clock

An external time standard may be used in place of the PIC's internal 1 MHz oscillator. The external clock may run at any rate up to 1 MHz, but if it is not 1 MHz, the Resolution Bits will not represent the specific count intervals shown on Fig. 4.9-1. The external input drives the circuit shown on Fig. 4.9-4. The resolution interval count-down circuit in the PIC is toggled when the input lead is at OV. The negative going input pulses must be less than one-half of the resolution interval.

4.9.3 LFC Operating Sequence

The LFC interrupt queue flip-flop is set at twice the line frequency or every 8.33 milliseconds if the primary AC input is at 60 Hz. It is unaffected by Write Data or Read Data instructions and always returns a status byte of all zeros. Bit 0 of the byte transferred by an Output Command disables the LFC interrupt but allows the queue flip-flop to store an interrupt. Bit 1 of the command byte, if set, enables the LFC interrupt. See Fig. 4.9-5.

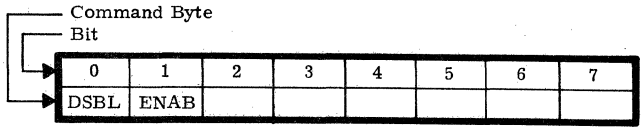


Fig. 4.9-5 LFC Command Byte

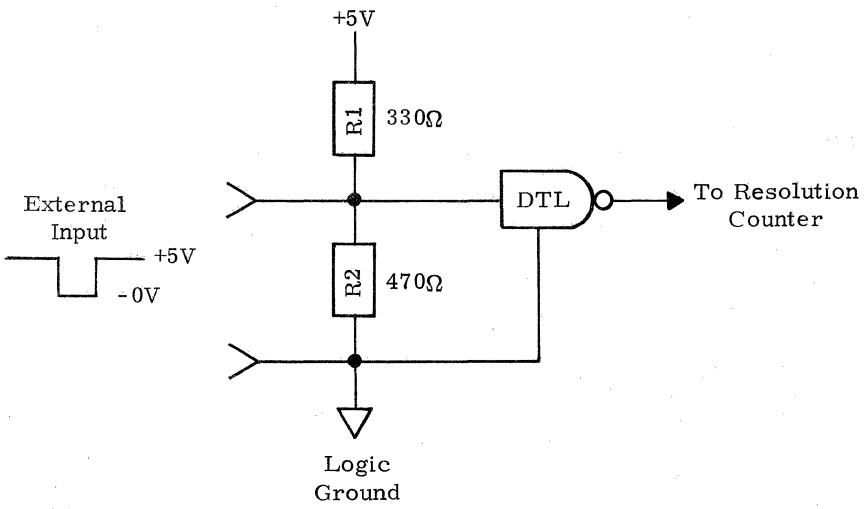


Fig. 4.9-4 PIC External Input Circuit

MULTIPLEXER BUS EXTENSION AND SWITCHING

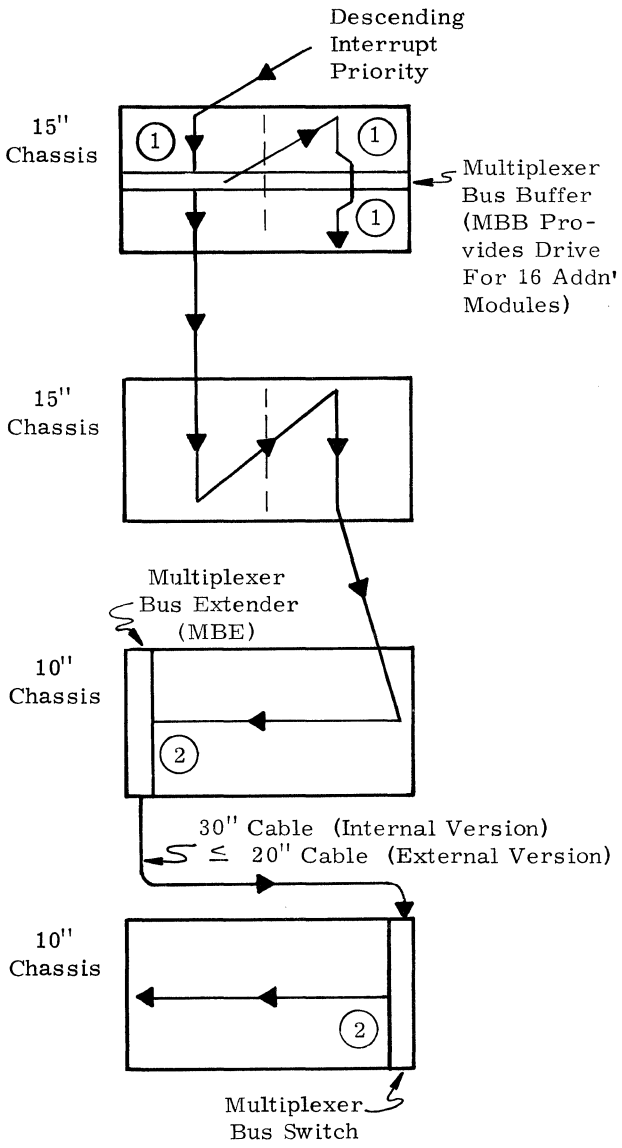
The Multiplexer Bus extension and switching options may be used to achieve any of a very large number of possible I/O controller complements and configurations. The basic Central Processor Multiplexer Channel and Bus may accomodate up to 16 I/O controllers of all types. The bus extension and switching options may be configured to extend the length of the bus, both physically and as to the number of controllers accomodated, up to the maximum of 255. These options also may be used to allow two or more GE-PAC 30, 3010, or 3010/2 computers to have access to one or more I/O controllers installed on a Multiplexer Bus which is common to the computers.

5.1 BUS EXTENSION

Since there are two basic physical variations of the Multiplexer Bus (refer to 4.6) two bus extender modules are available. A 3010AE7301 Multiplexer Bus Buffer (MBB) may be used to extend a portion of the bus on a 15" horizontal-board mounting chassis to additional controllers in the same chassis or another chassis. A 3000AE7102 Multiplexer Bus Extender (MBE) may be used to extend a portion of the bus on a 10" vertical-board mounting chassis to additional controllers in the same chassis or another chassis. Each of these modules uses one slot and provides a load equal to that of one controller to the unextended portion of the bus. As an example, if an MBB is used to extend a 15" bus, the basic bus can have 15 I/O controllers plus the MBB, and the MBB extends the bus to serve an additional 16 controllers. Fig. 5.1-1 illustrates some of the bus extension possibilities.

A 3000AE7102 Multiplexer Bus Extender (internal) may be used to extend a 10" portion of the bus to up to 21 additional I/O controllers, provided that the cable between the extender and the extended bus does not exceed 30 inches in length. For this purpose, the extender module is plugged into the final slot on the basic bus and the cable to the extended bus is attached to two daughter board locations near the front edge of the extender module. The extended bus is normally in one or two 10" vertical air-flow I/O Expansion Chassis.

The extended bus (10") may be up to 20 cable feet from the basic bus if a 3000AE7101 Multiplexer Bus Extender (external) and a 3010AE7401 Multiplexer Bus Switch (MBS) are implemented. In this case, the extender is plugged into the final slot on the basic bus and the switch module is plugged into the first slot on the extended bus. Each such extension provides the drive and buffering to accomodate up to 21 additional I/O controllers.



(1) Card slots in these areas are on the basic bus. The interrupt priority descends from the MBB and on down the extended bus only when a controller on the extended portion of the bus has an interrupt pending.

(2) This expansion provides drive for 21 addn'l. modules. External extension requires MBS in 2nd chassis, while internal expansion does not. Two or more MBS's may be used to allow more than one Processor to use the extended bus in the 2nd chassis.

Fig. 5.1-1 15" and 10" Bus Extension

5.2 MULTIPLEXER BUS SWITCHING

More than one GE-PAC 30, 3010, or 3010/2 Central Processor may have access to the I/O controllers installed on a common Multiplexer Bus (10"), if two or more Multiplexer Bus Switches are implemented on the common bus. Only one of the Central Processors has access to the controllers and devices on the common bus at any time, but the switch-over may be accomplished quickly and easily, either manually or by remote controls.

The Multiplexer Bus Switch (MBS) is, in effect, a single-pole single-throw switch, which when closed, allows the 27 data and control lines from the Multiplexer Bus in the user Processor to pass through the switch to the common bus. The common bus then becomes an extension of the user Processor's Multiplexer Bus (the dedicated bus), and the controllers and devices attached to the common bus operate as if they were on the user Processor's bus.

One MBS must be vertically mounted in a slot on the common bus for each Central Processor which is to use the common bus and only one MBS may be selected (closed) at any time, so that only one Processor may control the devices on the common bus. The addresses assigned to the devices on the common bus may not duplicate the address of any device on any of the Processor's dedicated busses. All data transfers on the common bus are 8-bit bytes.

The MBS's are completely transparent to all instructions and data passing through them. Instructions to devices on the common bus are executed at slightly reduced speeds due to a typical total one-way delay of approximately 160 nanoseconds.

Since the common bus, when connected to a dedicated bus, becomes a link in the Multiplexer Bus interrupt acknowledge daisy chain, the interrupt priority of the controllers on the common bus, with respect to those on the dedicated bus, may be determined by selecting the point at which the connection to the MBS is made. For example, if the connection was made at the midpoint on the dedicated bus, the controllers nearest the Processor would have the highest priority. The priority then would decrease down to the connection point, on down the common bus, and then would continue down the remainder of the dedicated bus. If the MBS connected to that dedicated bus is not selected, the interrupt acknowledge daisy chain is not broken, and the priorities are as if the MBS is not present.

5.2.1 MBS Options

The Multiplexer Bus Switch is available in two basic versions: Internal (3010AE7403 or 7404) and external (3010AE7401 or 7402). Each MBS is on a single board which must be mounted vertically. The internal version is used where the connection to the dedicated bus can be made with 30 inches of cable or less, as would be the case if the common bus was on an expansion card file adjacent to the dedicated bus. The external version is used when the cable connecting the MBS to the dedicated bus is more than 30 inches in length and equal to or less than 20 feet in length. When the external version is used, the MBS and common bus may be in a different cabinet than that containing the dedicated bus.

Where the external version MBS is used, a 3000AE7101 Multiplexer Bus Extender (10") must be installed on the dedicated bus to provide the drive and buffering needed to utilize the 20 ft. cable. Where the internal version MBS is used, no bus extender is required, but one slot on the dedicated bus must remain empty to accomodate the connection to the MBS. Fig. 5.2-1 provides some examples of MBS implementation.

Termination Resistors:

The first Multiplexer Bus Switch installed on a common bus must implement bus driver and bus receiver termination resistors. Subsequent MBS's installed on the same bus must not implement these resistors. Options 3010AE7401 (external) and 3010AE7403 (internal) include the termination resistors.

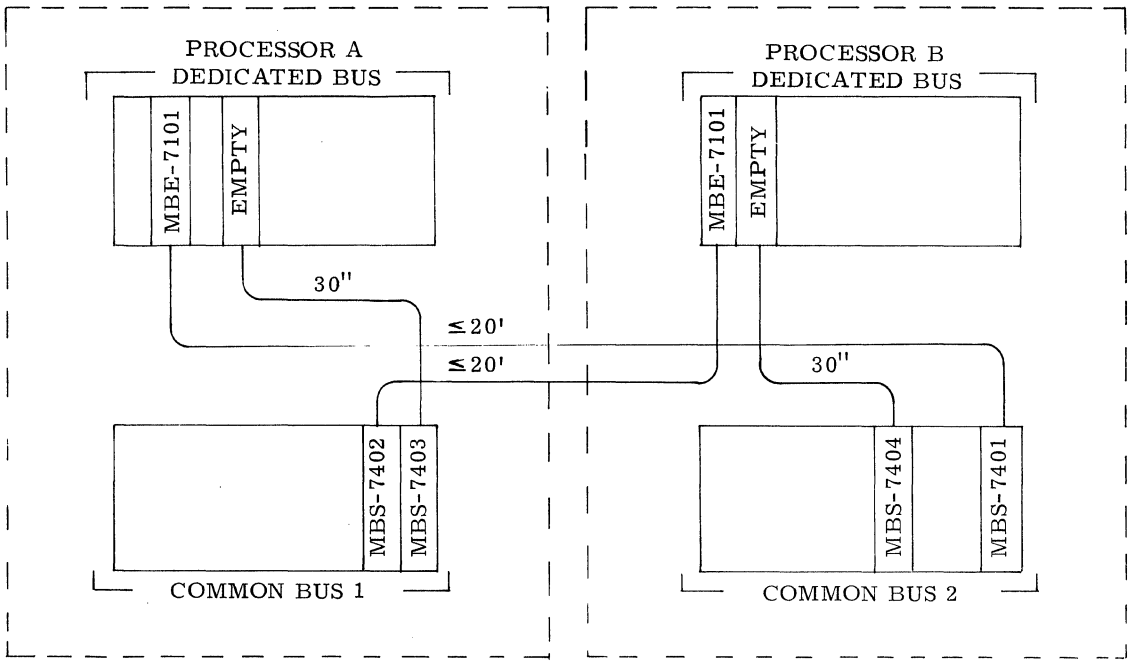
Remote Control:

The customer may provide a remote control circuit and a remote control cable to any Multiplexer Bus Switch to effect remote selection (closure) of the MBS. The remote control interface on each MBS includes both relay driver and logic level indications of the Remote/Local Mode status of the MBS and the Local Select status, if the MBS is in the Local Mode. If the logic level status is used, the cable may not exceed 20 ft. in length. Remote selection is enabled and local selection is made with two switches on the PWB front edge. A Remote Select indicator is also provided, as shown on Fig. 5.2-2.

If the MBS is in Remote Mode, it is selected when a form A contact set or relay driver in the remote control closes, applying a nominal 28 VDC at 38 milliamperes to the coil of the remote select relay on the MBS. This selection may be effected by Digital Output Terminations under program control, or by other automatic or operator actuated controls. The remote control circuit must ensure that only one MBS on any common bus will be selected at any time.

5.3 SELECTOR CHANNEL BUS EXTENSION AND SWITCHING

Selector Channel busses may be extended and/or switched in the same manner as Multiplexer Busses, using the same modules and options as for the Multiplexer Bus, provided that consideration is given to the effect upon instruction execution and data transfer rates of the delay through the bus extender and the Multiplexer Bus Switch. The Selector Channel



(All chassis viewed from board side)

NOTES:

MBE; 3000AE7101 Multiplexer Bus Extender
MBS; Multiplexer Bus Switch, 3010AE-

7401 - External, with termination resistors, cable provided separately.
7402 - External, without termination resistors, cable provided separately.
7403 - Internal, with termination resistors, 30" cable provided.
7404 - Internal, without termination resistors, 30" cable provided.

All chassis in these examples are 10" Vertical-Board mounting chassis. The MBS must be mounted vertically. It cannot be installed in a 15" adapter.

Fig. 5.2-1 Multiplexer Bus Switch Option Examples

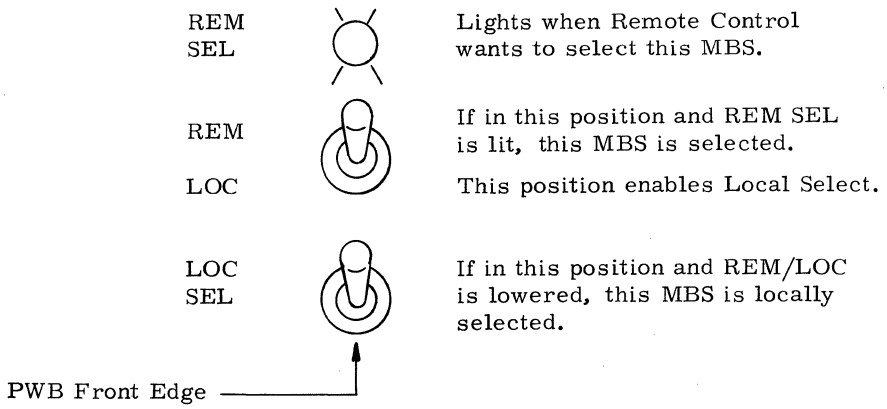


Fig. 5.2-2 MBS Remote/Local Controls

provides a bus which is functionally identical to the Multiplexer Bus to serve devices which have high data burst rates, and require access to Core Memory through cycle stealing. See Section 6 of this manual.

As an example, two Central Processors could have access to a Selector Channel bus which is common to both Central Processors, if each Central Processor implements a Selector Channel board in a 15" chassis. The common Selector Channel bus (10") is created in one of the two Central System Cabinets by installing a Multiplexer Bus Switch at the beginning of the common bus. The MBS allows one Selector Channel or the other to tie through to the common bus and use the devices on that bus.

5.4 CENTRAL PROCESSOR FAILURE RECOVERY

The MBS and the common bus require +15 VDC, -15 VDC, and +5 VDC for operation. This power is provided either by a power supply serving the common bus, only, or from a supply shared by the common bus and other functional modules. The common bus is not affected by failures of unselected Central Processors or their power supplies, provided that the common bus power remains available. If the common bus is switched from a failed Central Processor to one which is operational, the controllers and devices on the common bus may resume operation.

Power for the logic in the MBS which provides the switching functions and the interface with the dedicated bus, is derived from either the dedicated bus +15V supply or the common bus +15V supply. If one or the other of these supplies fails, the switching functions are not affected.

Failures of the power supplies affect the MBS and common bus operations as follows:

- Dedicated Bus Supplies - A failure of the +15V, -15V, or +5V dedicated bus supplies will not affect the MBS nor the common bus, provided the common bus power is still available. However, if the Processor associated with the dedicated bus uses these failed supplies, it will be inoperative.

- Common Bus -15V - The MBS will be unable to change the Local/Remote modes or to be changed from unselected to Local Select status. If it is already in the Remote mode, the remote control will still function.

- Common Bus +15V - If the dedicated bus +15V is still available, the operation will be unaffected. Controllers on the common bus which use +15V may be inoperative.

- Common Bus +5V - The MBS will go to Local mode and will not be selected. All controllers on the common bus will be inoperative and any MBS's on the common bus will be unselected.

The Selector Channel (Model No. 3010AD1201) controls the transfer of data between Core Memory and I/O subsystems such as Drum, Disc, and Magnetic Tape Subsystems. The Memory control logic in the Processor permits cycle stealing from the Processor by a Selector Channel (SELCH). Should the Processor and a SELCH request access to core at the same time, the SELCH is granted access first. Up to four SELCH's may be installed in a single Central Processor, all four have higher core access priority than the Processor, and each SELCH has descending priority from the first implemented to the fourth.

6.1 FUNCTIONAL DESCRIPTION

The Selector Channel creates a "private" SELCH bus which is functionally and electrically the same as the Multiplexer Bus, but allows the devices on the SELCH bus to exchange data with Core Memory without interrupting the running program (except when the SELCH steals a core cycle from the Processor). Once a SELCH data transfer is started, the running program may continue until it is notified that the transfer is complete by a SELCH interrupt. Up to 16 controllers may be installed on an unextended SELCH bus.

At the beginning of each data transfer sequence, the SELCH and all of the controllers on the SELCH bus are connected to the Multiplexer Bus as user devices. Early in each transfer sequence, the starting and ending core addresses for the block of data to be transferred are loaded into the SELCH address registers by Write Data instructions issued to the SELCH. When the transfer begins the SELCH goes BUSY, disconnects the SELCH bus from the Multiplexer Bus, and 8-bit bytes are transferred at up to 2,000,000 bytes per second. This maximum burst rate is dependent upon timely responses by the attached devices and controllers and the immediate granting of core access when requested. However, the transfer rate in all standard configurations is high enough that the rates specified for the user devices are not degraded.

6.2 OPERATING SEQUENCE

6.2.1 Initialization

When the system hardware is initialized (4.5.3), any data transfer in progress ceases, the SELCH goes to the Idle mode (users connected to the Multiplexer Bus), to the STOP mode, and to the Write mode. Also, if set, the SELCH interrupt queue flip-flop is reset.

6.2.2 Status Sensing

Sense Status instructions, Acknowledge Interrupt instructions, and Processor Status requests addressed to the SELCH cause a status byte to be returned to the Processor. Only bit 4 of the status byte has any meaning, and all other status bits are reset. Bit 4 is set when a data transfer is in progress and the SELCH is not ready to accept new commands. See Fig. 6.2-1.

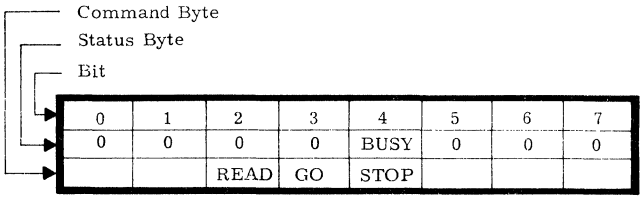


Fig. 6.2-1 SELCH Command and Status Bytes

6.2.3 Output Commands

Output Commands may be addressed to the SELCH and to users on the SELCH bus. Bits 2, 3, and 4 of the command byte transferred to the SELCH dictate the meaning of the command as follows (see Fig. 6.2-1):

- Bit 2 = 1 = READ. The READ command changes the SELCH mode from WRITE to READ (data to be transferred from the SELCH user to core). The SELCH automatically reverts to WRITE mode on completion of a READ transfer.
- Bit 3 = 1 = GO. GO initiates a data transfer after the starting and final core addresses have been loaded into the SELCH. Bits 2 and 3 may be set in the same Output Command byte. (GO or WRITE·GO = X'10'. READ = X'20'. READ·GO = X'30'.)
- Bit 4 = 1 = STOP. The STOP command terminates any data transfer in progress. If a Core Memory cycle is in progress, execution of STOP is delayed until the cycle is complete. (STOP = X'08'.)

6.2.4 Transfer Sequence

When the SELCH and users connected to the SELCH bus are idle, the SELCH bus appears as an extension of the Multiplexer Bus, and the desired user is then set up by issuing appropriate Output Commands and other instructions to the user. Four successive Write Data bytes are transferred to the SELCH by the program to load the starting and final core addresses for the block of data to be transferred, into the SELCH address registers. The sequence is as follows:

1. Starting address bits 0 through 7.
2. Starting address bits 8 through 15.

3. Final address bits 0 through 7.

4. Final address bits 8 through 15.

The starting address must begin on a halfword boundary (bit 15 = 0). If the final address ends on a byte boundary (bit 15 ≠ 0) and a READ transfer is executed, the final two odd bytes in core to which data is transferred will contain the same data. Appropriate Output Commands are then issued to the SELCH (READ and/or GO) and the transfer begins. Should a SELCH user be addressed while the SELCH is BUSY, Condition Code bit 13 (V) is set. For a WRITE operation, the SELCH acquires halfwords from core and transfers the data to the user as two bytes. For a READ operation, the SELCH accumulates two bytes from the user and transfers the data to core as a halfword*.

6.2.5 Termination

A SELCH data transfer may terminate due to any of five events:

1. The starting address (which is incremented as the transfers proceed) matches the final address. This is a normal termination.
2. The starting address increments from X'FFFF' to zero. This is an abnormal termination because no match of starting and final addresses occurred.
3. The SELCH detected a DU, EOM, or EX status bit set from the active user. An abnormal termination.
4. A STOP command is issued to the SELCH.
5. The Processor detects a power failure. See 4.7.

When a termination occurs, the SELCH BUSY status bit is reset, the SELCH interrupt queue flip-flop is set, and the SELCH returns to the idle and WRITE modes.

6.2.6 Final Address Verification

After the SELCH BUSY status bit is reset, the program may read the contents of the SELCH's incrementing address register by executing two Read Data instructions, addressed to the SELCH. The most significant address byte is transferred first and the least significant byte is transferred next.

6.2.7 Selector Channel Address

The SELCH is normally assigned device address X'F0'. The address may be changed by jumper wiring on the SELCH module.

* The SELCH is capable of halfword I/O. All current standard controllers on the SELCH bus use 8-bit bytes.

DRUM MEMORY

Drum Memory provides a large, reliable, economical, and quick access storage area for bulk data and programs which may not be currently needed in Core Memory. The data is recorded on a rotating cylindrical drum by fixed position heads which fly just above the drum surface.

7.1 FUNCTIONAL DESCRIPTION

Data is stored on the Drum in tracks of 32 sectors each. Each sector consists of 128 8-bit data bytes, and a special sector parity character. Each track is recorded and read by a single fixed position head. The storage capacity of the Drum is a function of the number of heads implemented. The Drum is available in 128K, 256K, 512K, 1024K, and 2048K byte sizes (K = 1024_{10}).

The 3000AD42 Drum and 3000AD41 Drum Controller are housed in a Drum Cabinet (Fig. 7.1-1). The Drum and controller communicate with Core Memory through the Selector Channel and the memory bus in the Central System Cabinet, as is shown on Fig. 4-1. Transfers of data between the Drum and core are made on a cycle stealing basis which results in very little use of Processor time. Once the user program starts the transfer of a block of data, the Processor is delayed only if it and the Selector Channel are requesting core access simultaneously, in which case access is granted to the Selector Channel. Each transfer must consist of an integral number of 128-byte sectors, up to a maximum of 512 sectors (65,536 bytes).

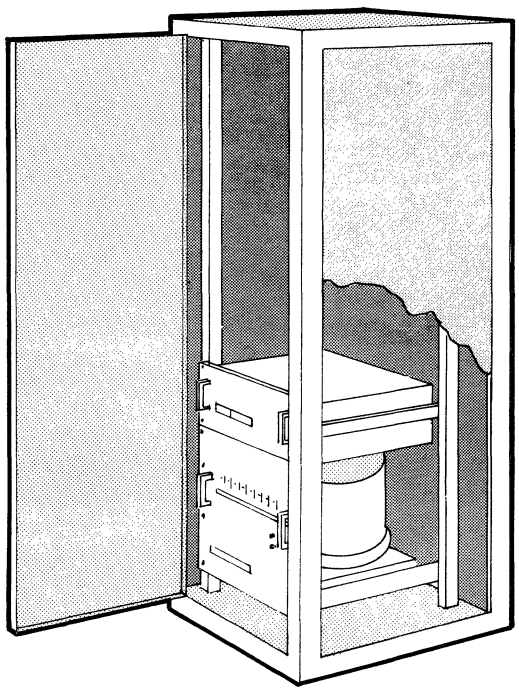


Fig. 7.1-1 Drum Cabinet

7.2 PRINCIPAL FEATURES

7.2.1 Average Access Time

The average time from a request for a Drum transfer until the first byte is transferred is 8.7 milliseconds.

7.2.2 Accuracy

The error rate does not exceed one bit per 10^{11} bits transferred.

7.2.3 Start Time

The Drum is up to speed and ready for operation within four minutes from the time power is applied to the motor.

7.2.4 Transfer Rate

Data are transferred at up to 230K bytes per second (burst rate).

7.2.5 Write Protection

Switches are provided on the Drum assembly to select groups of 16 successive tracks for protection. The entire Drum or any sixteen track area may be protected. If an attempt is made to write on a protected area, the WPV and EX bits in the Drum status byte (Fig. 7.3-1) are set and the transfer is terminated.

7.2.6 Parity Check

A special parity character which is representative of each group of 32 bytes on the drum is generated by the Drum Controller. Each parity character is written at the end of each 32 byte group, and each sector therefore contains four parity characters. When reading from the drum the controller regenerates each parity character and compares it with the appropriate recorded parity character. If an error is detected, the transfer is aborted and the PTY and EX bits in the drum status byte are set (Fig. 7.3-1).

7.3 OPERATING SEQUENCE

When the Selector Channel and Drum are idle, the Drum Controller appears on the Multiplexer Bus, and the program may monitor the controller's status and issue commands to the controller. Refer to Section 6 for a discussion of the Selector Channel operation. The starting Drum address is transferred to the Drum Controller and the starting and final core addresses are transferred to the SELCH prior to issuing a GO command to the SELCH. When a transfer sequence terminates, a SELCH interrupt occurs and the program may monitor both the Drum and SELCH status.

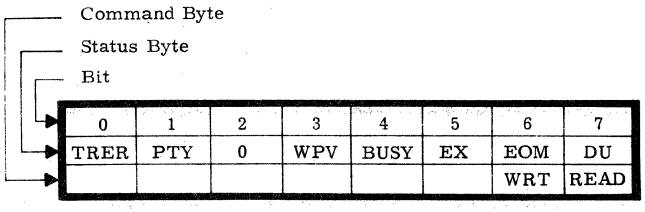
7.3.1 Initialization

When the system hardware is initialized (4.5.3) the Drum Controller is placed in the READ mode and all Drum status bits are reset.

7.3.2 Status

Sense Status instructions, Acknowledge Interrupt instructions, and Processor status requests addressed to the Drum Controller when the SELCH is idle, cause a status byte to be returned to the Processor. The status byte bits (Fig. 7.3-1) have the following meaning:

- Bit 0 = 1 = Transfer Error. This bit sets when a data byte is lost due to the failure of the SELCH, core memory bus, or Drum Controller to accept or provide a data byte when required. This bit is also set if an Output Command specifies both READ and Write, or neither READ nor Write.
- Bit 1 = 1 = Parity Error. See "Parity Check", 7.2.6.
- Bit 3 = 1 = Write Protect Violation. See "Write Protection", 7.2.5.
- Bit 4 = 1 = BUSY. On a read operation (Drum to core) BUSY is reset when the controller is ready to transfer a data byte through the SELCH. On a Write operation BUSY is reset when the controller is ready to accept a data byte from the SELCH.
- Bit 5 = 1 = Examine. EX = TRER+PTY+WPV. When this bit sets, any transfer in progress is terminated.



0	1	2	3	4	5	6	7
TRER	PTY	0	WPV	BUSY	EX	EOM	DU
						WRT	READ

Fig. 7.3-1 Drum Status and Command Bytes

- Bit 6 = 1 = EOM. The End of Medium bit is set if the Drum address register in the controller increments beyond the highest address implemented on the Drum, or if the starting address specified by the program is higher than any implemented on the Drum. If this bit sets, any transfer in progress is terminated.
- Bit 7 = 1 = Device Unavailable. This bit sets if the Drum rotational speed is not correct or the Drum heads are not actuated. The heads normally actuate to the operating position when the minimum Drum speed is reached. If this bit sets, any transfer in progress is terminated.

7.3.3 Output Commands

When the SELCH is idle, Output Commands may be addressed to the Drum Controller. Bits 6 and 7 of the command byte transferred to the controller dictate the meaning of the command as follows (Fig. 7.3-1):

- Bit 6 = 1 = Write. The WRT command places the Drum Controller in the Write mode for transfer of data from core to the drum (Write = X'01').
- Bit 7 = 1 = READ. This command places the Drum Controller in the READ mode for transfer of data from the drum to core (READ = X'02').

7.3.4 Drum Starting Address

Two successive Write Data instructions addressed to the Drum Controller transfer the Drum address from which, or to which, the first data byte is to be transferred. The first Write Data instruction transfers the most significant byte, and the least significant byte is transferred next. Max. starting addresses for each Drum size are: 128K, X'03FF'; 256K, X'07FF'; 512K, X'0FFF'; 1024K, X'1FFF'; and 2048K, X'3FFF'.

7.3.5 Device Address

The Drum Controller is normally assigned device address X'86'. The address may be changed by jumper wiring on the controller module.

DISC MEMORY

Disc Memory provides a very large economical bulk storage medium. Up to four Disc Units may be connected to a single Disc Controller, providing 2,457,600 bytes of storage per unit, or almost 10 million bytes, if four units are implemented. A movable head assembly in each Disc Unit records data on two disc surfaces of 200 tracks each. The disc cartridge is removable and, on units used for background programming, can be changed in about a minute, to provide supplemental capacity.

8.1 FUNCTIONAL DESCRIPTION

Data is stored on the disc in tracks of 24 sectors each. Each sector consists of a sector address, 256 data bytes, and a two-byte parity check character. Each track is read and recorded by one of two movable heads using a double frequency recording technique. One head reads and writes on the top of the disc and the other uses the bottom of the disc.

Since each side of the disc has 200 tracks, there are a total of 400 tracks. Each pair of tracks at the same distance from the center of the disc can be thought of as forming a cylinder, and the 200 track positions on each side of the disc are addressed as cylinders 0 through 199. The total disc storage capacity is derived as follows: 2 heads X 200 tracks X 24 sectors X 256 bytes per sector = 2,457,600 8-bit bytes.

The discs are compact light-weight units. (Model No. 3010AD5201), which mount into a rack near the front of a system cabinet. The disc rotates at 1500 RPM ±10% as maintained by an electronic control circuit. The head movement and positioning are also electronically controlled. The unit is designed for ease of maintenance and reliability. It uses no potentiometers, and no drive belts, chains, or pulleys. Two simple controls are provided at the front of the unit, with three indicators, as shown on Fig. 8.1-1.

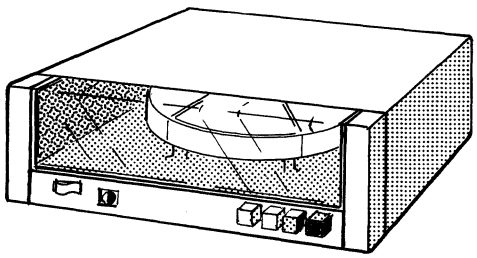


Fig. 8.1-1 Disc Unit

The Disc Memory Subsystem consists of two controller boards, one or more Disc Units, a Disc Cabinet, and associated power supplies. The two controller boards are the Disc Data Controller and the Disc Unit (File) Controller. Both boards are installed on a Selector Channel (SELCH) bus (10"). When the SELCH is idle, the Data Controller and each of the Disc Units appear on the Multiplexer Bus and SELCH bus as separately addressable controllers.

8.2 PRINCIPAL FEATURES

8.2.1 Access Times

The average latency time due to disc rotation is 20 milliseconds. Head positioning and settling times are 15 msec. maximum for movement to an adjacent track, and 135 msec. maximum to move 200 tracks. Average head positioning time is 70 msec., and overall average access time, including latency, is approximately 90 msec.

8.2.2 Start Time

When a cartridge is inserted and the Load/Run switch on the unit is switched to Run, the disc comes up to operating speed in approximately 50 seconds.

8.2.3 Transfer Rate

The 256 byte data field in each sector is transferred at 194,529 bytes per second. Assuming the transfer of a record consisting of two full tracks at the same cylinder, the 12,288 bytes in the record are transferred in 80 milliseconds ±1%, plus latency time, or about 150,000 bytes per second.

8.2.4 Write Protection

An entire Disc Unit is protected from inadvertent writing, and consequent destruction of recorded data, through the Write Protect feature, which is enabled when the Load/Run switch on the unit is switched from Load to Run. Write protection is disabled by pushing the Protect button on the unit. If disabled, Write Protection can be enabled again by moving the switch to Load and back to Run. When Write Protect is enabled, the Protect lamp on the unit is lit and bit 0 of the unit status byte is set (Fig. 8.3-3). An attempt to write on a protected unit sets controller status bit 7.

8.2.5 Parity Check

A special 2-byte parity character is written by the controller immediately after the 256-byte data field. The character is representative of the data in the sector and is checked by the controller on each read operation. Should the parity character regenerated as the data is read from a sector not compare with the parity character read from the sector, Data Controller status bit 7 is set (Fig. 8.3-1).

8.2.6 Sector Format Writing and Checking

The Data Controller's Write Format and Read Format modes permit semi-automatic writing and verification of the sector format, which is shown on Fig. 8.2-1. The entire disc may be rewritten and checked, or only a portion of the disc. Before the Write Format or Read Format Output Commands may be issued to the Data Controller, the heads must be positioned at the proper cylinder, and a 270 byte pattern stored in core for each sector to be written, as follows:

1. First Byte of the Sector Address.
2. Second Byte of the Sector Address.
3. Eight bytes, all containing zeros.
4. Two bytes containing the sync code; X'00', X'03'.
5. 258 bytes containing any data test pattern.

After the head assembly is positioned at the correct cylinder and the sector address has been transferred to the Data Controller, an Output Command specifying the Write Format or Read Format (Fig. 8.3-1) is issued to the Data Controller to start the transfer. The Read Format transfer should return the same format data and the controller hardware should verify a correct parity character. A jumper must be installed on the Data Controller board to enable the formatting operations, which are normally used by maintenance personnel, only.

A Read Format transfer should be effected only immediately after a Write Format transfer to the same disc addresses, or the results may be uncertain. If a normal read transfer follows a Write Format transfer apparent parity errors may be detected. Therefore, a Read Format command should only follow a Write Format command, and normal write command should transfer data to the reformated area before normal reading from the area.

8.2.7 Environment

The Disc Unit operating temperature range is 60° F to 90° F (15.6° C to 32.2° C), where the relative humidity ranges from 20% to 80% with no condensation. The Disc Controller operating environment is the same as for the Central Processor.

8.3 OPERATING SEQUENCE

When the Selector Channel is idle, the Data Controller and all of the Disc Units appear to be on the Multiplexer Bus. The Data Controller responds to Output Command, Write Data, Read Data, Sense Status, and Acknowledge Interrupt instructions. Each of the Disc Units responds to all of those instructions except Read Data.

The Data Controller and selected Disc Unit are set up to perform a required operation by addressing instructions directly to them. If the operation includes the transfer of data between the selected Disc Unit and core, via the SELCH, the SELCH is provided the starting and final core addresses for the data transfer via four Write Data instructions, and when the SELCH, Data Controller, and selected Disc Unit are ready, the SELCH is issued a GO Output Command. When a transfer sequence terminates, the SELCH status goes Not-Busy, and the SELCH interrupt queue flip-flop sets. The program may then monitor the status of the SELCH, the Data Controller, and the Disc Units. Refer to Section 6 of this manual for a discussion of the SELCH operation.

Should an instruction be issued to the SELCH, the Data Controller, or one of the Disc Units while a transfer is in progress and the SELCH is Busy, there will be no response to the instruction and condition code bit 13 (V) of the current PSW will be set.

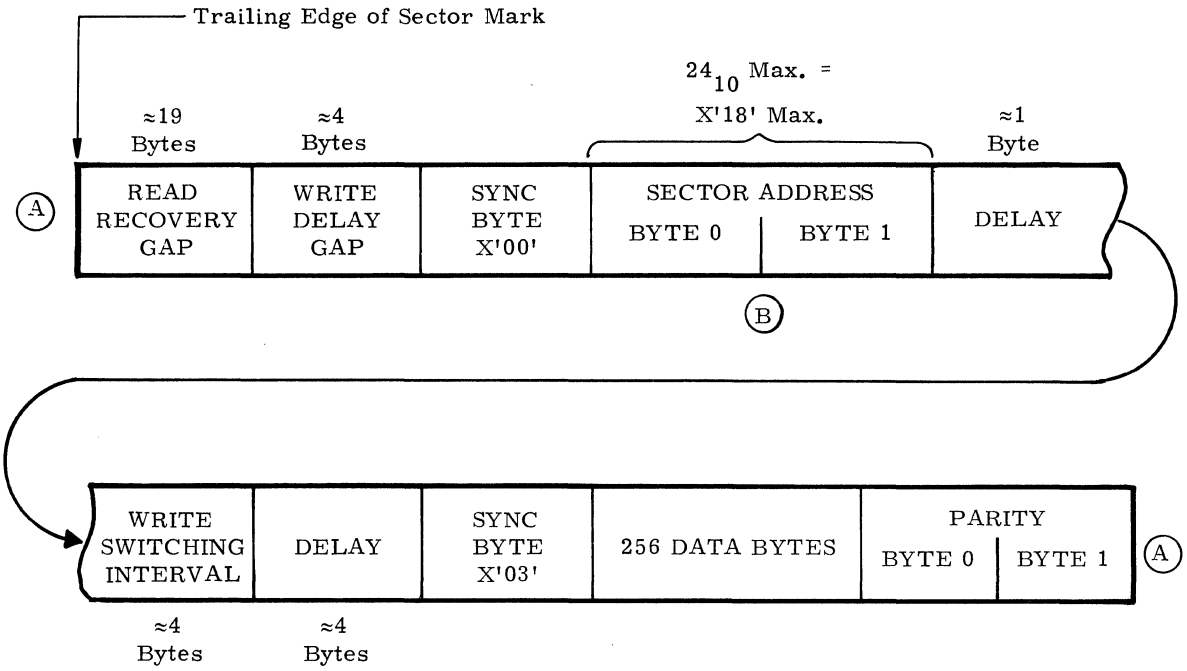
8.3.1 Cylinder Seek

If the head assembly is not known to be positioned at the proper cylinder prior to a transfer sequence, the unit must first be commanded to seek out the proper cylinder. After sensing the SELCH status and Disc Unit status and finding both ready, the cylinder address is transferred to the unit by a Write Data instruction (X'00' - X'CA'). Then an Output Command is issued to the unit specifying Seek or Return to Zero (Fig. 8.3-3). First the Data Controller status goes Not-Idle, and then when head movement starts, Idle. The unit status byte will reflect Not-RSRW when the heads start to move, and then RSRW (Fig. 8.3-3) when the seek is complete. While the seek on one unit is in progress, another may be commanded to start a seek, a data transfer on another unit may be started, or the program can undertake other work while the seek is in progress.

8.3.2 Transfer Sequence

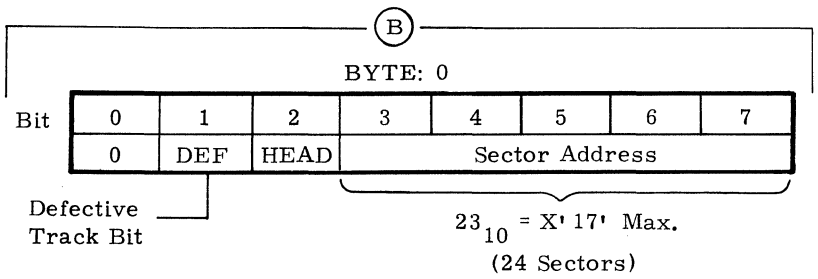
With the heads at the proper cylinder, a data transfer may be started. Typically, after the status of the Data Controller and Disc Unit are checked, the SELCH should be given the starting and final core addresses (6.2.4). Then the cylinder address is transferred to the Disc Unit via a Write Data instruction (X'00' - X'CA'). Another Write Data instruction transfers the head number (0 or 1) and the starting sector address to the Data Controller (Fig. 8.3-2). Finally, an Output Command is issued to the Data Controller (Fig. 8.3-1) to specify the operation to take place. The first data transfer will not take place for at least 90 microseconds, so this time period can be used to issue a GO command to the SELCH.

To find the desired sector on the selected track, the Disc Unit and controller keeps track of the sector positions in a counter, and when the correct sector



Each byte interval is 5.1 μs. Where the no. of bytes is shown as approximate (≈), variation is due to drift in disc speed, etc.

(A) Inter-Sector Interval; about 37 byte times or 159 Msec.



Byte 1: Cylinder Number: 202_{10} = X'CA' Max.

(200 basic cylinders plus 3 spares)

Fig. 8.2-1 Disc Sector Format

comes up, the address bytes are read from the sector and checked with the requested address. If they compare, the transfer begins as the data portion of the sector passes the head. The address check is not made again during the transfer sequence.

The length of each data transfer between core and the SELCH is specified by the starting and final core addresses transferred to the SELCH prior to starting the transfer. When the SELCH finds a match between the current address and the final address, it terminates the transfer, resets the SELCH BUSY status bit, and the SELCH interrupt queue flip-flop sets. The Disc Unit and Data Controller, however, must continue through to the end of the current sector so that the parity character may be written or checked. For a Write transfer, in the absense of any new data from the SELCH, the reminder of the sector data field is filled with the last byte received from the SELCH.

A disc transfer may be up to 12,288 bytes in length, if the transfer begins at sector 0 on head 0. The Data Controller sector address is automatically incremented as the transfer progresses. If the transfer begins on head 0 and continues through sector 24, the head number is incremented to 1 and the transfer continues through sector 24 of the second track. Should the SELCH not terminate before sector 24 of the second track is transferred, the Data Controller's Overrun status bit sets (Fig. 8.3-1).

8.3.3 Device Addresses

The standard device addresses for the Data Controller and Disc Units are as follows:

Data Controller - X'B6'

Disc Unit 0 - X'C6'

Disc Unit 1 - X'D6'

Disc Unit 2 - X'E6'

Disc Unit 3 - X'F6'

The addresses may be changed with jumper wiring on the controller, but only bits 1, 2, and 3 may be altered.

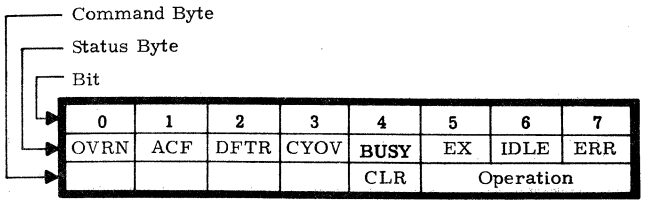


Fig. 8.3-1 Data Controller Command and Status Bytes

8.3.4 Output Commands to Data Controller

Output Command instructions issued to the Data Controller transfer a command byte, the contents of which have the following meaning (Fig. 8.3-1):

- Bit 4 = 1 = Clear the Data Controller. A command with CLR set initializes the Data Controller.
- Bits 5, 6, and 7 specify the type of Data Controller operation;

Command Byte	Operation
X'01'	Read Data Transfer. When the previously specified beginning sector is found and the address checked, data is read from the disc for transfer to core via the SELCH.
X'02'	Write Data Transfer. When the previously specified beginning sector is found and the address checked, data is transferred from core to the disc via the SELCH.
X'03'	Read Check. This operation is similar to Read Data transfer except that no data is transferred through the SELCH. The first sector address is checked and then the data is sampled to regenerate the parity character and check it.
X'05'	Read Format. When the previously specified beginning sector is found, a Read Format check as described under 8.2.6 is made.

8.3.5 Data Controller Status

Sense Status and Acknowledge Interrupt instructions issued to the Data Controller return a status byte, the contents of which have the following meaning (Fig. 8.3-1):

- Bit 0 = 1 = Overrun. OVRN sets if the specified sector has not been found in two disc revolutions following a data transfer command. This error may be due to the specification of a non-existant sector.
- Bit 1 = 1 = Address Compare Failure. ACF sets if during a read or write operation, the address character from the first sector does not compare with starting sector address held by the Data Controller.

- Bit 2 = 1 = Defective Track. DFTR sets if the Disc Unit detects a defective track. If it sets, DFTR will set at the beginning of a sector.

- Bit 3 = 1 = Cylinder Overflow. CYOV sets if the SELCH tries to transfer additional data after the Disc Unit has read sector 24 on head 1.

- Bit 4 = 1 = BUSY. BUSY is set when the selected Disc Unit and the Data Channel are exchanging data. When BUSY is reset, the SELCH may transfer a byte. This signal is used only by the SELCH, normally is set only while the SELCH is busy, and should not be apparent to the program.

- Bit 5 = 1 = Examine. EX = OVRN + ACF + DFTR + CYOV.

- Bit 6 = 1 = Controller Idle. IDLE is set when the controller is ready to accept a new command.

- Bit 7 = 1 = Error. ERR sets if during any read operation, the parity character read from a sector does not compare with the parity character regenerated by the controller. Should a read data transfer end before the end of the sector, the setting of ERR may occur some time after SELCH termination. This bit is also set if an attempt is made to write on a Disc Unit under Write Protection (8.2.4).

8.3.6 Sector Address to Data Controller

The starting head and sector address is transferred to the Data Controller prior to any read or write operation by a single Write Data instruction. Fig. 8.3-1 illustrates the meaning of the data byte bits.

8.3.7 Data Byte From Data Controller

A Read Data instruction addressed to the Data Controller while the controller is IDLE, transfers a data byte containing the current sector address to the Processor. The address is in the form shown on Fig. 8.3-2. It is possible that the data byte might be transferred at the time the sector counter is being updated, in which case the data might not be valid.

A Read Data instruction addressed to the Data Controller while it is Not-Idle, transfers the current content of the controller's data register to the Processor.

Should a Read Data to the controller be attempted while the SELCH is busy, it will not reach the controller, an instruction time-out will occur, and condition code bit 13 (V) in the current PSW will set.

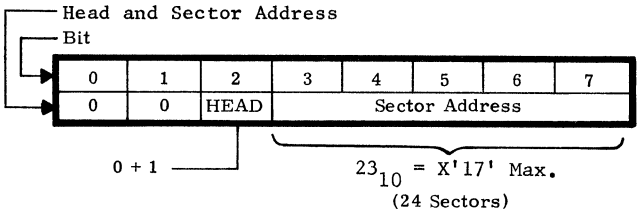


Fig. 8.3-2 Sector Address Data Byte

8.3.8 Output Commands to Disc Unit

The command byte transferred by an Output Command to a Disc Unit controller has the following meaning (Fig. 8.3-3):

- Bits 0 and 1 are Interrupt Control bits -

  $\overline{0}\cdot\overline{1}$ = no change.

  $\overline{0}\cdot 1$ = enable the Disc Unit interrupt.

  $0\cdot\overline{1}$ = disable the interrupt but allow the queue flip-flop to store an interrupt.

  $0\cdot 1$ = disarm interrupts, reset the queue flip-flop.

- Bit 6 = 1 = SEEK. This command initiates a Cylinder Seek. See 8.3.1.

- Bit 7 = 1 = Return to Zero. RTZ initiates a seek to return to cylinder zero (Restore). Should command bits 6 and 7 be set, RTZ is executed.

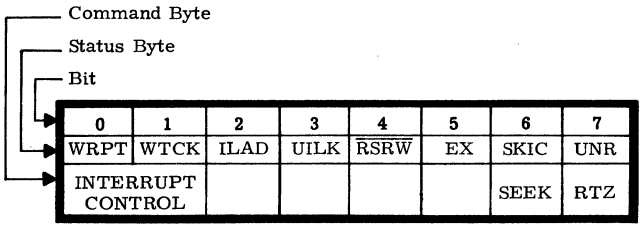


Fig. 8.3-3 Disc Unit Command and Status Bytes

8.3.9 Disc Unit Status

The status byte returned by a Disc Unit in response to a Sense Status instruction addressed to a Disc Unit controller has the following meaning (Fig. 8.3-1):

- Bit 0 = 1 = Write Protect. WRPT is set when the unit is in Write Protect mode. See 8.2.4.

- Bit 1 = 1 = Write Check. WTCK is set by either of two hardware faults; improper head selection (2 heads or no head) or low DC supply voltage.

- Bit 2 = 1 = Illegal Address. ILAD sets if a sector address greater than 202_{10} (X'CA') is specified for a seek operation. If this bit sets, the seek will not occur. The next legal SEEK or RTZ command will clear this condition.

- Bit 3 = 1 = Unit Interlock. UILK is set while this unit is being set up to respond to a command. If a new command is issued to this unit or another unit while this bit is set it may not be executed or the unit selection may not change. The program should always wait for UILK to reset after issuing a command to a unit before issuing a new command.

- Bit 4 = 1 = Not Ready to Read, Seek, or Write. $\overline{\text{RSRW}}$ is set while this unit is executing a SEEK or Return to Zero. It resets when the heads have arrived at the correct position.

- Bit 5 = 1 = Examine. EX = WTCK + ILAD.

- Bit 6 = 1 = Seek Incomplete. SKIC sets if the unit cannot complete a Cylinder Seek. This might happen because the head assembly arrived at its mechanical stops because the cylinder address register got out of step with the head assembly. A Return to Zero seek clears this condition.

- Bit 7 = 1 = Unit Not Ready. A Disc Unit is not ready for any operation unless it has a cartridge loaded and is running up to speed. A non-existant unit will always reflect UNR.

8.3.10 Disc Subsystem Interrupts

The Disc Controller has five interrupt queue flip-flops; one for each of the four possible units and one for the Data Controller. The controller establishes the relative interrupt priorities as follows:

1. Data Controller
2. Disc Unit 0
3. Disc Unit 1
4. Disc Unit 2
5. Disc Unit 3

The SELCH interrupt could be considered as the highest Disc Subsystem interrupt. As is described in Section 6, the SELCH interrupt queue flip-flop is set whenever a transfer terminates. This occurs for a normal termination when the currect core address held by the SELCH matches the final core address transferred to the SELCH by the program. An abnormal termination occurs when the Examine bit in the Data Controller Status byte sets, and this also causes a SELCH interrupt.

The Data Controller interrupt queue flip-flop sets when the IDLE status bit sets (8.3.5).

The interrupt queue flip-flop for any Disc Unit sets under the following unit status conditions (8.3.9):

- Write Check (WTCK) sets.
- Illegal Address (ILAD) sets.
- Not Ready to Read, Seek, or Write ($\overline{\text{RSRW}}$) resets.
- Seek Incomplete (SKIC) sets.
- Unit Not Ready (UNR) sets.

MAGNETIC TAPE SUBSYSTEM

Magnetic tape is an additional bulk storage medium which provides the largest bulk storage capacity at lower cost than equivalent Drum or Disc memory. While the capacity of a tape reel is determined in part by the format the program prescribes, a 10 1/2 inch reel containing about 2400 feet of tape could store more than 10 million 8-bit bytes at 800 bytes per inch.

The tape transport is designed to provide quick reel exchanges, and if a library of several reels is maintained, a very large amount of digital data may be stored. The tape subsystem is designed for compatibility with tapes written and reproduced by other equipment manufacturers, such as IBM 2415 Tape Transports, and if the CRCC option is implemented, the IBM 2400 series.

9.1 FUNCTIONAL DESCRIPTION

Data is stored on the tape in the form of 7 or 9 track characters as shown on Fig. 9.1-2. Each character includes an "odd ones" parity bit which is generated as each character is written and checked as each character is read. The data is written in records consisting of four or more characters and files of one or more records.

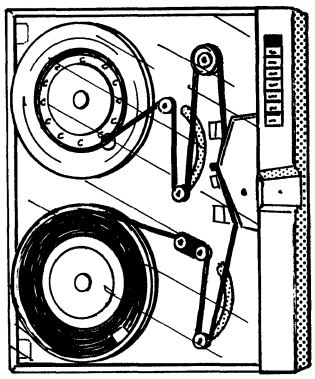


Fig. 9.1-1 Magnetic Tape Transport

The Magnetic Tape Subsystem consists of a Magnetic Tape Controller, which is installed in two adjacent slots on a 10" portion of a Selector Channel bus, an optional Cyclic Redundancy Check Character generator, which occupies a thirds slot on the SELCH bus, and a Magnetic Tape Transport. If there is sufficient space, the transport can be installed in a cabinet, such as the Central System Cabinet, which shares other functions. If necessary, a separate Magnetic Tape Cabinet can be provided.

9.1.1 Options

Two basic Magnetic Tape Subsystem versions are available. The first reads and records 7-track characters at 556 bits per track per inch or 800 bits per inch. The second version reads and writes 9-track characters at 800 bits per inch, only. Three combinations of controllers and transports are therefore possible:

7-Track, 556 bpi; 3000AD3101 Controller and 3000AD3201 Transport.

7-Track, 800 bpi; 3000AD3102 Controller and 3000AD3201 Transport.

9-Track, 800 bpi; 3000AD3103 Controller and 3000AD3202 Transport.

To attain compatibility with IBM 2400 series transports, a 3000AD3301 Cyclic Redundancy Check Character (CRCC) Generator may be added to the 9-track version. The CRCC character is not used on 7-track tapes.

9.2 PRINCIPAL FEATURES

9.2.1 Tape Speed

For reading, writing, and back-space operations the tape travels at 25 inches per second ±1%. The tape rewinds at 150 inches per second. The tape is accelerated and decelerated smoothly under electronic control. Tape start and stop times are nominally 15 milliseconds. The tape is stopped after reading and writing each record. It also stops when the end of tape indicator on the tape is detected and when the tape arrives at the load point after a rewind or upon loading the tape.

9.2.2 Transfer Rate

Characters are written and read at a burst rate of 20,000 bytes per second at 800 bpi, or 13,900 bytes per second at 556 bpi.

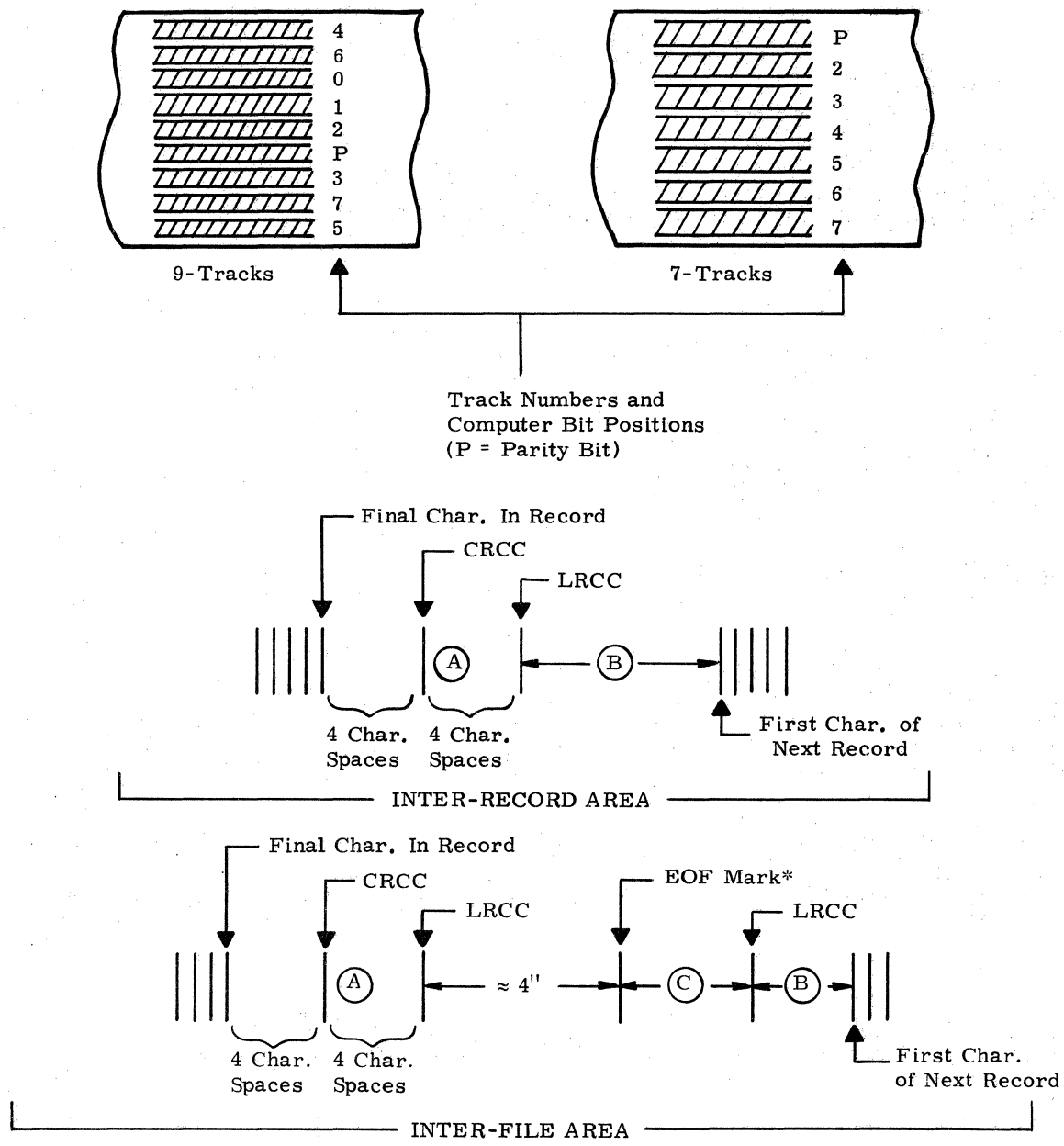
9.2.3 Tape Supply

The transport accepts standard 0.5 in. wide, 0.0015 in. thick, computer grade tape on reels up to 10.5 inches in diameter.

9.2.4 Parity Checking

As is indicated on Fig. 9.1-2, three parity indications are written on the tape when recording; a lateral parity bit accompanies each character written on the tape, a CRCC follows the last character in each 9-track record, and a longitudinal redundancy check character (LRCC) is also included in the interrecord gap. The lateral parity bit is checked as each character is read from the tape and each LRCC is checked before the tape is stopped between records.

The lateral parity bit provides an "odd ones" parity sense for each data character and each CRCC and



(A) CRCC and this space are missing on 7-track tapes.

(B) 0.6" on 9-track and 0.75" on 7-track.

(C) 8 char. spaces on 9-track; 4 char. spaces on 7-track.

* X'13' (9-track) or X'0F' (7-track).

Fig. 9.1-2 Magnetic Tape Formats

LRCC character. Each bit in the LRCC character, except the lateral parity bit, is representative of the number of ONE bits preceding it in the track. A correct LRCC bit provides an even number of ONE's in the track for the entire record.

The CRCC character is written only to provide compatibility with other tape subsystems (9-track tapes only). If the CRCC Generator option is not implemented, a dummy CRCC is written. The dummy CRCC is representative of track zero. If track zero contains an even number of ONE's the CRCC will be X'80'; if it contains an odd number of ONE's the CRCC will be X'00'.

9.2.5 Environment

The Tape Transport operating temperature range is 2° C to 50° C (35° F to 122° F). The Magnetic Tape Controller environment is the same as for the Central Processor.

9.3 OPERATING SEQUENCE

The Magnetic Tape Subsystem is relatively free of programming restrictions, and the program may issue commands to the controller in any reasonable sequence. The controller hardware provides the timing necessary to ensure that the tape can start and stop as required. Commands requiring tape motion or a change in tape direction will not be accepted by the controller unless controller status bit 3 is set (NMTN). Commands which call for tape motion in the same direction are executed immediately. Commands requiring a change in tape direction are executed after a turn-around delay of 10 milliseconds.

Data is exchanged between Core Memory and the tape, via the Selector Channel (SELCH), only while the tape is in forward motion. There is ample time from when forward tape motion command is executed, to set up the SELCH with the starting and ending core addresses and issue a GO command to the SELCH (see Section 6 of this manual).

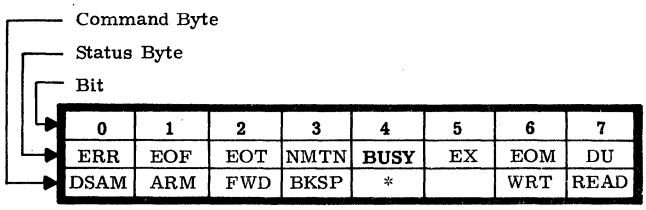
9.3.1 Device Address

The standard device address for the Magnetic Tape Controller is X'85'. The address may be changed by changing jumper wiring on the controller module.

9.3.2 Output Commands

Output Command issued to the controller transfer a command byte to the controller. The meaning of the command byte bits is as follows (Fig. 9.3-1):

- Bit 0 = 1 = Interrupt Disarm. DSAM resets the controller interrupt queue flip-flop and prevents the controller from interrupting the Processor.



0	1	2	3	4	5	6	7
ERR	EOF	EOT	NMTN	**BUSY**	EX	EOM	DU
DSAM	ARM	FWD	BKSP	*		WRT	READ

* Used in Rewind and End of File commands. See text.

Fig. 9.3-1 Magnetic Tape Controller Command and Status Bytes

- Bit 1 = 1 = Interrupt ARM. ARM enables the controller interrupt. The controller cannot reach the processor while the SELCH is BUSY with a data transfer.

- Bit 2 = 1 = Forward. FWD indicates the tape direction. FWD must be accompanied with WRT or READ.

- Bit 3 = 1 = Backspace. BKSP indicates reverse tape motion. BKSP must be accompanied with READ. The tape reverses one record and stops.

- Bit 6 = 1 = Write. WRT specifies write mode. WRT should be accompanied with FWD. In write mode, data is transferred from core to the tape.

- Bit 7 = 1 = READ. This bit should be accompanied by FWD to cause data to be transferred from the tape to core. If READ is accompanied by BKSP, the tape will reverse one record and stop. No data is transferred to core on a backspace, but the controller and transport must be in READ mode to find the inter-record gap.

To rewind the tape to the load point (beginning of the tape), a command byte with bits 2, 3, and 4 set is issued to the controller. A rewind command is executed immediately even if the tape is in forward motion. The rewind may take several seconds, and the program is notified when it is complete as the NMTN status bit sets.

An end of file mark is written in the inter-record gap (Fig. 9.1-2) after approximately 4 inches of blank tape are created, when a command byte with bits 2 and 3 set, and bit 4 equal to zero is issued to the controller.

The legal command bytes are as follows (ARM or DSAM may be issued independently at any time):

Write; X'22'.

Arm, Write; X'62'.

Disarm, Write; X'A2'.

Read; X'21'.

Arm, Read; X'61'.

Disarm, Read; X'A1'.

Backspace; X'11'.

Arm, Backspace; X'51'.

Disarm, Backspace; X'91'.

Rewind; X'34'.

Arm, Rewind; X'74'.

Disarm, Rewind; X'B4'.

End of File; X'30'.

Arm, End of File; X'70'.

Disarm, End of File; X'B0'.

9.3.3 Status Sensing

Status bytes returned to the Processor in response to Sense Status and Acknowledge Interrupt instructions have the following meaning (Fig. 9.3-1):

- Bit 0 = 1 = Error. ERR sets if a lateral parity error or an LRCC error is detected while reading from the tape. ERR also sets if the SELCH fails to transfer a character within a character period.

- Bit 1 = 1 = End of File. EOF sets when an End of File mark is detected in an Inter-file gap.

- Bit 2 = 1 = End of Tape. EOT is set when the transport detects the end of tape mark or the beginning of tape mark. If EOT is set at the end of tape, a Rewind command or initialization of the system hardware is necessary to reset this bit. If EOT is set at the beginning of tape, a command specifying forward tape motion is required to reset EOT.

- Bit 3 = 1 = No Motion. NMTN is set when the tape is stopped and the transport is in the idle state. The controller can accept tape motion commands only when this bit is set. The tape stops automatically at all inter-file and inter-record gaps, and NMTN sets when the tape is completely stopped.

- Bit 4 = 1 = BUSY. BUSY is set when the controller is in the process of transferring a character, and resets when it is ready to accept another character for transfer to the tape, or is holding a character for transfer to the Processor. The controller's interrupt queue flip-flop is set as BUSY resets, if not disarmed. This bit is used by the SELCH to determine when data should be transferred and normally has no significance to the program.

- Bit 5 = 1 = Examine. EX = EOF + NMTN.

- Bit 6 = 1 = End of Medium. EOM sets when the end of a record is detected. The controller detects the end of a record by noting the absense of characters in the inter-record or inter-file gaps. If ERR or EOF conditions are detected, those status bits set prior to EOM.

- Bit 7 = 1 = Device Unavailable. DU sets if the tape transport is off line, power is not applied to it, or if tape is not loaded or not positioned properly.

9.3.4 Data Transfers

The controller will respond to Read Data and Write Data instructions if the Selector Channel is idle, but data transfers are normally made through the SELCH.

A complete 8-bit byte is transferred in the 9-track Mag. Tape Subsystem and the controller generated and checked lateral parity bit is recorded in the ninth track. Seven-track subsystems ignore bits 0 and 1 of each byte to be written, and bits 0 and 1 are set to zero in bytes read from the tape. The seventh bit in 7-track systems is also the lateral parity bit.

9.3.5 Interrupts

The Mag. Tape Controller interrupt queue flip-flop sets (if not disarmed) when the BUSY status bit resets and when tape motion stops.

PERIPHERAL DEVICES

SECTION 10

Peripheral devices provide man/machine interfaces through which programs and data may be transferred in and out of the computer. All of these devices communicate through device controllers which are connected to the Multiplexer Bus. Each attached device communicates through its own individual device controller in an 8-bit byte format.

Every system must implement, as a minimum peripheral device complement, at least one input/output typer for program communication and one paper type reader for loading programs.

10.1 TYPERS

Two basic typer versions are available: Teletypewriters or TermiNet 300 Printers. Several typers of either type may be implemented in any combination. TermiNet printers are available as output only or input/output devices. Teletypewriters are available only in input/output models. Either typer is available as an ASR (Automatic Send and Receive) unit, featuring an I/O typer, a paper tape punch, and a paper tape reader, in one unit.

10.1.1 TermiNet 300 Printers

TermiNet 300 Printers are quiet, compact, medium speed units that are available as Model 4272B, a Keyboard Send and Receive (KSR) unit, or Model 4273B, a Receive Only (RO) unit. The RO model has no keyboard and cannot transfer data to the computer. A paper tape punch and paper tape reader are available as accessories to the KSR model. When the punch and reader are implemented, they are installed in a desk, and the Printer normally rests on the desk top.

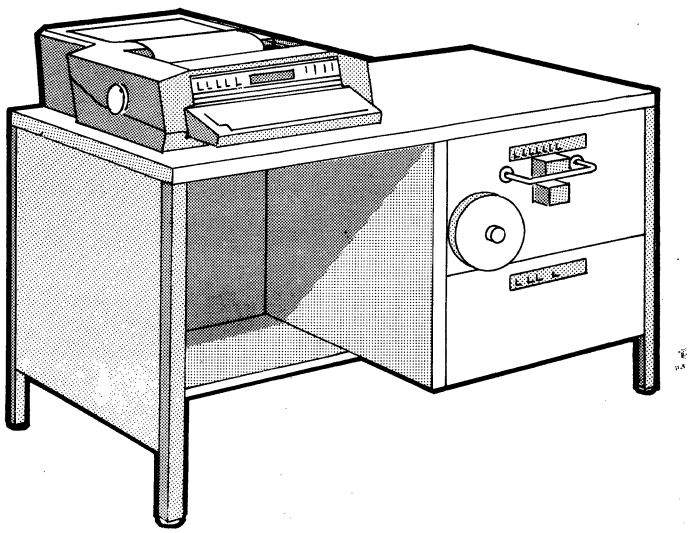


Fig. 10.1-1 TermiNet 300 Printer

The Printer is primarily electronic and features a rotating type belt. The belt contains two complete character sets and the characters are printed by firing a hammer as the correct character passes the desired position on the print line. The principal features are as follows.

Data Transfer Rate; up to 30 characters per second. A High Speed Transmission option is available for the ASR version which allows the paper tape reader to read 120 characters per second for transmission to the computer at 1200 baud. The unit cannot print copy when in the high speed mode.

Character Code; character exchanges between the computer and the keyboard and printer are 7-bit ASCII codes, with an optional even parity bit in the most significant bit position. Received parity bit checking is a printer option. If this option is implemented, an alarm sounds on detection of a parity error, and if the received character is detected as a printing character, a diamond symbol is printed in its place. Since the device interface does not generate or check the parity bit, it must be generated and checked by the program. Character exchanges between the computer and the paper tape punch and reader (ASR units) are straight 8-bit binary characters. Each character also includes one start bit and one stop bit, for a total of ten serial bits.

Device Interface; asynchronous bit-serial characters are transferred at 300 baud (bit/sec.) (1200 baud when the high speed reader option is utilized). TermiNet Printer Interface Model 3000AE2101 connects to the printer via an EIA RS-232C interface on a cable up to 50 feet in length. Interface Model 3000AE2201 connects to the printer via a current loop interface on a cable up to 2000 feet in length.

Typer; friction feed or pin feed platens are available to handle 8-1/2 inch paper where the 80 character per line option is selected. A 118 character per line option is also available which uses 12.85 inch width paper.

Tape Punch and Tape Reader (ASR unit); punch and read 8-level characters on tape one inch in width. When the high speed reader option is to be used, the rate switch on the unit must be placed in the 120 char./sec. and an appropriate Output Command issued to the interface.

Status Sensing; Sense Status instructions, Acknowledge Interrupt instructions and Processor status requests addressed to the TermiNet Printer Interface cause a status byte to be returned to the Processor. The status byte bits (Fig. 10.1-2) have the following meaning -

- Bit 0 = 1 = Overflow. In the READ mode, OV is set if the Processor fails to input a

data byte before the next byte is received by the interface module. OV = 0 in the Write mode.

- Bit 2 = 1 = Break. The BRK bit is set when the Interrupt button on the device is pushed. The Interrupt button causes the Transmitted Data line from the device to go to the space state (0, false) for approximately 268 milliseconds.

- Bit 3 = 1 = On-Line. ONLN is set when the device is connected to the computer and the Request to Send line from the device is in a true state. Request to Send from the device goes false (standby mode) when the Standby or Local button on the printer are pushed, or when the rate switch is in the 120 CPS position (high speed reader option).

- Bit 4 = 1 = BUSY. When the interface is in the Write mode, the BUSY bit is reset when the interface is ready to accept a byte for transfer to the device and is set while a character is being serially shifted out to the device. When the interface is in the READ mode, BUSY is reset when the interface has a character ready for transfer to the Processor and is set when the Processor accepts the byte. The interrupt queue flip-flop sets as BUSY resets. (When changing from READ to Write modes, the interrupt queue flip-flop sets while BUSY remains true. The program should ignore the interrupt if BUSY is set.)

- Bit 5 = 1 = Examine. EX = OV + BRK.

- Bit 7 = 1 = Device Unavailable. DU is set when the Data Terminal Ready line from the device is in the false state. Data Terminal Ready from the device goes false when device power is off or in Local mode.

Command Byte

Status Byte

Bit

0	1	2	3	4	5	6	7
OV	0	BRK	ONLN	BUSY	EX	0	DU
DSBL	ENAB	UNBL	BLK	WRT	READ	CB1	CB2

Fig. 10.1-2 TermiNet Printer Command and Status Bytes

Output Commands; the Output Command bits have the following meaning (Fig. 10.1-2) -

- Bits 0 and 1 = interrrupt disable and enable, respectively. When enabled, the interrupt occurs as the BUSY status bit resets, and is therefore, a data-ready (READ mode) or a ready to transfer (Write mode) interrupt.

- Bit 2 = 1 = Unblock. UNBL causes data entered from the keyboard or tape reader to be returned to the printer to produce copy. If the paper tape punch is on, the data will also be punched.

- Bit 3 = 1 = Block. BLK inhibits the return of keyboard or reader data to the printer.

- Bit 4 = 1 = Write. WRT places the interface in the Write mode for transfer of data from the computer to the printer and, if on, the punch.

- Bit 5 = 1 = READ. READ places the interface in the READ mode for transfer of data from the keyboard or paper tape reader to the Processor.

- Bits 6 and 7 set the interface to the 300 or 1200 baud rate. If both CB1 and CB2 are set, the interface is set up to receive data from a paper tape reader in a TermiNet unit implementing the 120 char./sec. option. If either bit 6 or bit 7 is reset, the interface operates at 300 baud (30 char./sec.) If CB1 = 1 and CB2 = 0, the Data Set Ready line to the device goes to the true state, but this line is not monitored by the TermiNet unit and has no meaning.

Device Address; when a TermiNet Printer is the first typer implemented in a system, it is normally assigned device address X'12'. The address may be changed by jumper wiring on the interface module. Standard addresses for subsequent typers are X'32' and X'42'.

Data and Control Character Transfers; Read Data and Write Data instructions addressed to the TermiNet Printer interface module are used to transfer data bytes between the computer and the device. Several ASCII control characters which may originate in the computer or in the TermiNet unit are decoded by the device to effect various operations and exercise various options. The control character set and sequences is extensive, and is not described in detail here. Refer to the TermiNet 300 Printer Programmer's Manual and the Operator's Manual for additional information. These manuals are GE publications GEK-15002 and GEH-2184, respectively.

Program Control of Paper Tape Punch and Reader; for ASR units, four control characters are available to effect program control of the paper tape punch and reader. These characters are part of the control character set described in the preceding paragraph and may be transferred by Write Data instructions.

- With the TermiNet unit on-line with the computer, and the Transparency switch on the unit in the Off position, a DC1 character (X'91', X-ON) starts the tape on the reader. A DC3 character (X'93', X-OFF) stops the tape. When starting, the tape may move

one or two characters before data is transferred, and when stopping the tape may continue one or two characters. Tapes to be read under program control, therefore, should be prepared to allow for such overlap. (Note - When loading programs using the 50 Sequence bootstrap loaders, the Transparency switch on the device must be in the On position, the device in Standby mode, and the reader must therefore be operated manually.)

- A DC2 character (X'92', TAPE ON) starts the paper tape punch and DC4 (X'94', TAPE OFF) stops the punch. The Transparency switch must be off. Both of these characters are punched on the tape.

Initialization; when the Initialize button on the Display Panel is pushed, the DSBL, BLK, and READ command functions are set, status bits BRK, EX, and DU are reset, BUSY is set, and the interrupt queue flip-flop is reset.

10.1.2 Teletypewriters

Teletypewriters are available as Model 35 for rugged duty, or the more economical Model 33, where the unit will be subjected to light duty. Either model is available as an ASR unit, and Model 35 is available as a KSR (keyboard send and receive) unit. The model numbers are as follows:

3000AE1201 - ASR 33

3000AE1202 - ASR 35

3000AE1203 - KSR 35

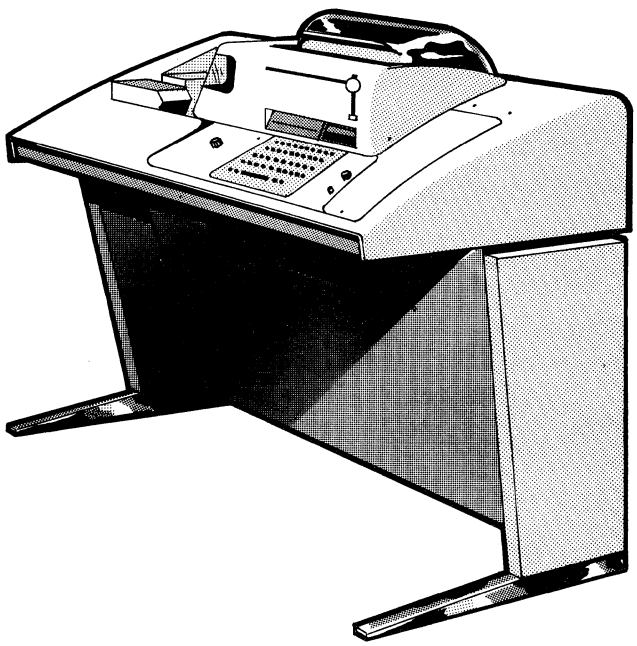


Fig. 10.1-3 Teletypewriters

The principal teletypewriter features are:

Data Transfer Rate; up to ten characters per second. Full-duplex 20 milliampere current loops are utilized for bit-serial asynchronous-character exchanges between the computer and the teletypewriter.

Character Code; character exchanges between the computer and the keyboard and printer are 7-bit ASCII codes, with an even parity bit in the most significant bit position. However, the interface and teletypewriter do not check the parity bit on characters transferred to the teletypewriter. Character exchanges between the computer and the paper tape punch and reader (ASR units) are straight 8-bit binary characters. Each character also includes one start bit and two stop bits, for a total of eleven serial bits.

Operating Modes; KSR models have a rotary Line/Off/Local switch which selects operation on-line with the computer, power off, and local operation, respectively. In the Local position, the keyboard may operate the printer. ASR models also have a Line/Off/Local switch which operates in conjunction with a K/KT/T/TTS/TTR mode switch as follows -

1. K (Keyboard). Line - Input from the keyboard to the computer is operable. If command function UNBL is set, input data is returned to the printer. Local - The keyboard is connected to the typer. The punch and reader are disabled in both Line and Local.

2. KT (Keyboard-Tape). Line - All functions, keyboard, printer, punch and reader, are operable. Local - Keyboard and reader are connected to the punch. This is the normal mode when on-line with the computer.

3. T (Tape). Line - The paper tape reader is operable. Data may be transferred from the computer to the printer. The keyboard is connected to the paper tape punch. Local - The reader is connected to the printer and the keyboard is connected to the punch.

4. TTS (Tape-Tape Send). Line - The paper tape punch and reader are operable, while the keyboard and printer are disabled. Local - Tapes read by the reader are duplicated on the punch.

5. TTR (Tape-Tape Receive). Line - The paper tape punch is operable while the keyboard, printer and reader are disabled. Local - no function.

Data and Control Character Transfers; Read Data and Write Data instructions addressed to the Teletypewriter Interface are used to transfer data bytes between the computer and teletypewriter. For ASR models, four control characters are available to effect control of the paper tape punch and paper tape

reader. These characters are transferred via Write Data instructions and are decoded in the teletypewriter -

- With the paper tape reader on-line with the computer (see "Operating Modes") and with the reader's START/STOP/FREE switch in the STOP position, an ASCII DC1 character (X'91', X-ON) starts the tape, and a DC3 character (X'93', X-OFF) stops the tape. When starting, the tape may move one or two characters before data is transferred, and when stopping, the tape may continue for one or two characters. Tapes to be read under program control, therefore, should be prepared to allow for such overlap.

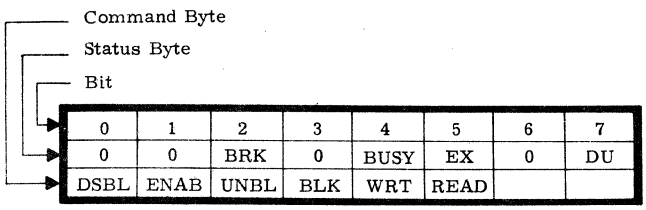
- With the paper tape punch on-line with the computer, an ASCII DC2 character (X'92', TAPE ON) starts the punch, and a DC4 character (X'94', TAPE OFF) stops the punch. The program should transfer two or three rub out characters (X'FF') after TAPE ON, to allow the punch and interface to synchronize. TAPE OFF will be punched on the tape.

Typer; sprocket fed 8-1/2 inch paper, 80 characters per line, 12 characters per horizontal inch, 6 lines per vertical inch.

Tape Punch and Reader (ASR unit); punch and read 8-level characters on tape one inch in width.

Device Interface Options; model 3000AE1101 is capable of driving up to 50 feet of computer to device cable. Model 3010AE1301 is capable of driving up to 2000 feet of cable. The first teletypewriter implemented in a system uses the built-in interface in the processor with up to 50 feet of cable.

Status Sensing; Sense Status instructions, Acknowledge Interrupt instructions, and Processor status requests addressed to the Teletypewriter Interface cause a status byte to be returned to the Processor. The status byte bits (Fig. 10.1-4) have the following meaning -



0	1	2	3	4	5	6	7
0	0	BRK	0	BUSY	EX	0	DU
DSBL	ENAB	UNBL	BLK	WRT	READ		

Fig. 10.1-4 Teletypewriter Command and Status Bytes

- Bit 2 = 1 = Break. The BRK bit is set while the Break key on the keyboard is depressed or when the teletypewriter is disconnected from the computer.

- Bit 4 = 1 = BUSY. When the interface is in the Write mode, the BUSY bit is reset when the interface is ready to accept a byte for transfer to the teletypewriter and is set while a character is being serially shifted out to the teletypewriter. When the interface is in the READ mode, the busy bit is reset when the interface has a character ready for transfer to the Processor and is set when the Processor accepts the byte.

- Bit 5 = 1 = Examine. EX = BRK.

- Bit 7 = 1 = Device Unavailable. The DU bit is set when the teletypewriter is in Local mode or when teletypewriter power is off or disconnected.

Output Commands; the Output Command bits have the following meaning (Fig. 10.1-4) -

- Bits 0 and 1 = interrupt disable and enable, respectively. When enabled, the interrupt occurs as the BUSY status bit resets, and is therefore, a data-ready (READ mode) or a ready to transfer (Write mode) interrupt.

- Bit 2 = 1 = Unblock. UNBL causes data entered from the keyboard or the paper tape reader to be returned to the printer to produce copy.

- Bit 3 = Block. BLK inhibits the return of keyboard or reader data to the printer.

- Bit 4 = 1 = Write. WRT defines the meaning of the BUSY status bit and the interrupt as required for transfer of data from the computer to the teletypewriter.

- Bit 5 = 1 = READ. READ defines the meaning of the BUSY status bit and the interrupt as required for transfer of data from the teletypewriter to the computer.

Device Address; the built-in Teletypewriter interface in the Processor has device address X'02', which cannot be changed. Standard addresses for subsequent typers are X'12', X'32', and X'42'.

Inititalization; when the Initialize button on the Display Panel is pushed, the DSBL, BLK, and READ command functions are set, status bits BRK, EX, and DU are reset, and BUSY is set.

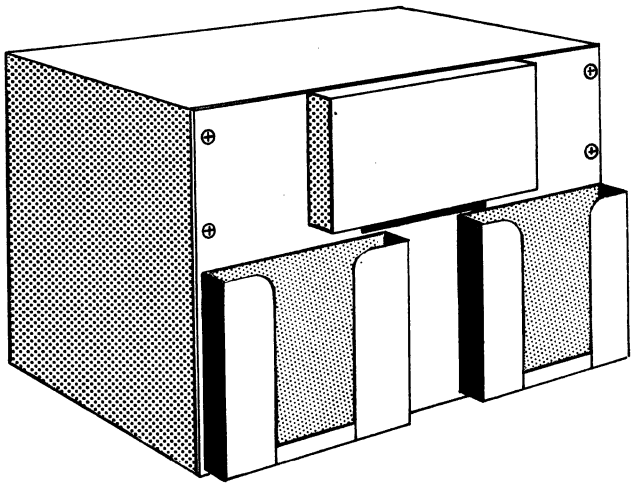


Fig. 10.2-1 Paper Tape Punch

10.2 PAPER TAPE PUNCH

The 3010AE33 Paper Tape Punch records character bytes transferred from the Processor through the Multiplexer Bus in the form of punched holes on a paper tape. A tape supply reel, a fan-fold supply box, and a fan-fold receiver box are provided. The punch is a free-standing unit and is connected to the computer by up to 25 feet of cable. The principal features are:

Punching Rate; up to 60 characters (bytes) per second.

Tape; one-inch width.

Character Format; 8-level characters, ten characters per inch.

Device Interface; where both a Paper Tape Punch and a Paper Tape Reader are implemented, a single common 3000AE3103 Paper Tape Punch/Reader Interface module may be used to serve both units. This common interface does not allow simultaneous operation of the two devices. An individual 3000AE3102 Paper Tape Punch Interface module is also available. If the punch and reader are served by individual interfaces, simultaneous operation is possible.

Status Sensing; the meaning of the bits in status bytes returned from the interface to the Processor is as follows (Fig. 10.2-2) -

- Bit 4 = 1 = BUSY. BUSY is set when the interface module holds a character for transfer to the punch and is reset when ready to accept another character from the Processor.
- Bit 6 = 1 = Device Unavailable. DU is set when the punch is off-line or when power is not applied to the punch.

Output Commands; the Output Command bits have the following meaning (Fig. 10.2-2) -

- Bits 0 and 1 = interrupt disable and enable, respectively. When enabled, the interrupt occurs as the BUSY status bit resets, and is therefore a ready to transfer interrupt.
- Bit 2 = 1 = STOP. STOP stops the tape after the next character is punched and turns the punch motor off.
- Bit 3 = 1 = RUN. RUN starts the punch motor.
- Bit 5 = 1 = Write. WRT specifies that tape is to be punched. RUN and WRT must be issued before data may be transferred. RUN·WRT = X'14'.

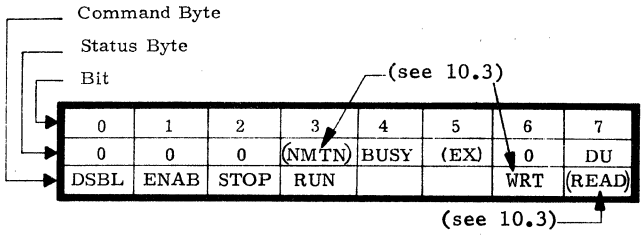


Fig. 10.2-2 Paper Tape Punch Command and Status Bytes

Initialization; when the Initialize button on the Display Panel is pushed, status bits NMTN, BUSY, and EX are set, command functions DSBL, STOP and READ are set, and the interrupt queue flip-flop is reset.

Device Address; if a single interface module is used to serve both a punch and reader, device address X'13' is normally assigned. If a punch, only, is implemented, device address X'13' is normally assigned. The address may be changed by jumper wiring on the interface module.

10.3 PAPER TAPE READER

A Paper Tape Reader reads characters from paper tapes for transfer to the Processor via the Multiplexor Bus. The tape to be read is held in a supply box and passes into a receiver box as it is read. Paper Tape Reader Model 3000AE3201 is mounted in the Central System Cabinet and extends through an opening in the front door (Cabinet Door 3010AJ4604 must be implemented). Paper Tape Reader Model 3010AE3401 is a free-standing unit and is connected to the computer by up to 25 feet of cable.

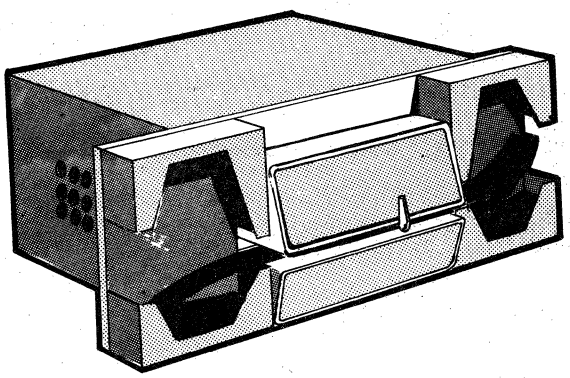


Fig. 10.3-1 Paper Tape Reader

The principal features of the Paper Tape Reader are:

Reading Rate; up to 300 characters per second.

Tape; one-inch width.

Character Format; 5, 6, 7, or 8-level characters are read into the Processor as a single byte. The reader normally is used to read tapes of the format prepared by the teletypewriter punch, the TermiNet punch or the punch described under 10.2.

Device Interface; where both a Paper Tape Reader and a Paper Tape Punch are implemented, a single common 3000AE3103 Paper Tape Punch/Reader Interface module may be used to serve both units. The common interface does not allow simultaneous operation of the two devices. An individual 3000AE3101 Paper Tape Reader Interface module is also available. If the reader and punch are served by individual interfaces, simultaneous operation is possible.

Status Sensing; the meaning of the bits in status bytes returned from the interface to the Processor is as follows (Fig. 10.3-2) -

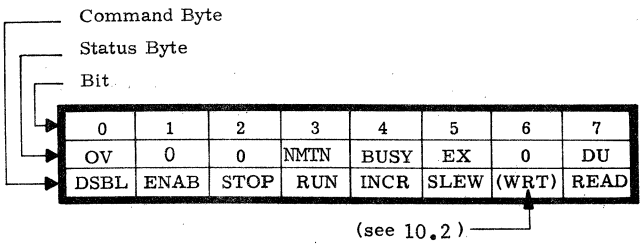


Fig. 10.3-2 Paper Tape Reader Status and Command Bytes

- Bit 0 = 1 = Overflow. OV is set when a character is lost due to the receipt of a new character by the interface module before a previously received character has been read into the Processor.

- Bit 3 = 1 = No Motion. NMTN is set when the reader tape is stopped after a STOP command has been issued.

- Bit 4 = 1 = BUSY. BUSY is reset when the interface module is holding a character ready for transfer to the Processor. It is set when the Processor reads-in a character.

- Bit 5 = 1 = Examine. EX = OV + NMTN.

- Bit 7 = 1 = Device Unavailable. DU is set when the reader is off-line or power is not applied to the reader motor.

Output Commands; the Output Command bits have the following meaning (Fig. 10.3-2) -

- Bits 0 and 1 = interrupt disable and enable respectively. When enabled, the interrupt occurs as the BUSY status bit resets, and is therefore a data ready interrupt.

- Bit 2 = 1 = STOP. STOP stops the tape after the next character has been read, placing the following character at the sensing station on the reader.

- Bit 3 = 1 = RUN. This command places the interface in the RUN mode and starts the tape moving.

- Bit 4 = 1 = Increment. In the INCR mode, characters are read on an incremental basis. The tape is not advanced to a new character position until the preceding character has been transferred to the Processor by a Read Data instruction.

- Bit 5 = 1 = SLEW. In the SLEW mode, the tape is advanced continuously and each character is transferred to the interface module as it passes the sensing station.

- Bit 7 = 1 = READ. READ specifies that tape is to be read. RUN and READ must be issued before data may be transferred. RUN·INCR·READ = X'19'. RUN·SLEW·READ = X'15'.

Initialization; when the Initialize button on the Display Panel is pushed, status bits NMTN, BUSY, and EX are set, command function DSBL, STOP, and READ are set, and the interrupt queue flip-flop is reset.

Device Address; if a Paper Tape Reader, only is implemented, it is normally assigned device address X'03'. If a punch and reader are served by the same interface module, address X'13' is normally assigned. The address may be changed by jumper wiring on the interface module.

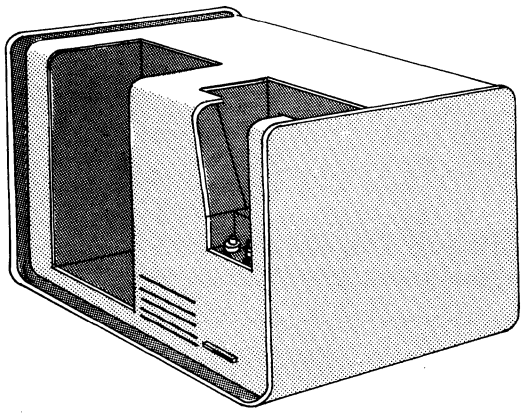


Fig. 10.4-1 Card Reader

10.4 CARD READER

The 3000AE42 Card Reader senses 12-bit characters, column by column, from standard 80-column computer cards, for transfer to the Processor via the Multiplexer Bus. The Card Reader is a free-standing unit and is connected to the computer by up to 15 feet of cable. The principal features are:

Reading Rate; up to 225 cards per minute.

Hopper and Stacker Capacities; up to 500 cards each. The input hopper supply may be replenished during operation of the reader.

Data Format; each Read Data instruction transfers one-half column (six bits) to the Processor. Bits 0 and 1 of each data byte are reset, and the remaining bits contain the half-character. Two reads are required to transfer each column; the upper six rows are read first, then the lower six rows.

Device Interface; Model 3000AE4101 Card Reader Interface.

Status Sensing; the meaning of the bits in status bytes returned from the interface to the Processor are as follows (Fig. 10.4-2) -

Command Byte
Status Byte
Bit

0	1	2	3	4	5	6	7
OV	TBL	HE	NMTN	BUSY	EX	EOM	DU
DSBL	ENAB	FEED					

Fig. 10.4-2 Card Reader Status and Command Bytes

- Bit 0 = 1 = Overflow. OV is set when a character is lost because the Processor did not read-in the last character before the next is read from the card.

- Bit 1 = 1 = Trouble. TBL is set when a card motion error, light current error, or dark current error is detected by the reader. A light current error is detected if light is not sensed in all bits when no card is in the read station. A dark current error is detected if all bits are not sensed as dark sometime between the end of each card and column-1 and sometime between column-80 and the other end of the card. Manual recovery for all three errors is required.

- Bit 2 = 1 = Hopper Empty (HE).

- Bit 3 = 1 = No Motion. NMTN is set except from when a FEED command is issued until the card has passed through the read station. NMTN also sets when HE sets as the last card is fed out of the hopper.

- Bit 4 = 1 = BUSY. BUSY is reset when the interface module is holding a data column for transfer to the Processor. It is set while the next column is transferred to the interface module.

- Bit 5 = 1 = Examine. EX = OV + TBL + HE + NMTN.

- Bit 6 = 1 = End of Medium. EOM = HE + NMTN.

- Bit 7 = 1 = Device Unavailable. DU = TBL.

Output Commands; the Output Command bits have the following meaning (Fig. 10.4-2) -

- Bits 0 and 1 = interrupt disable and enable, respectively. When enabled, the interrupt occurs as the BUSY status bit resets, and is therefore a data ready interrupt.

- Bit 2 = 1 = FEED. If status bits TBL, HE, and DU are reset, and if the reader and interface are not in a card read cycle, FEED initiates a new feed cycle and read cycle. One FEED command per card is required.

Initialize; when the Initialize button on the Display Panel is pushed, status bit OV is reset, NMTN, BUSY, EX, and EOM are set, and the interrupt queue flip-flop is reset.

Device Address; the Card Reader is normally assigned device address X'04'. The address can be changed by jumper wiring on the interface module.

10.5 CARD PUNCH

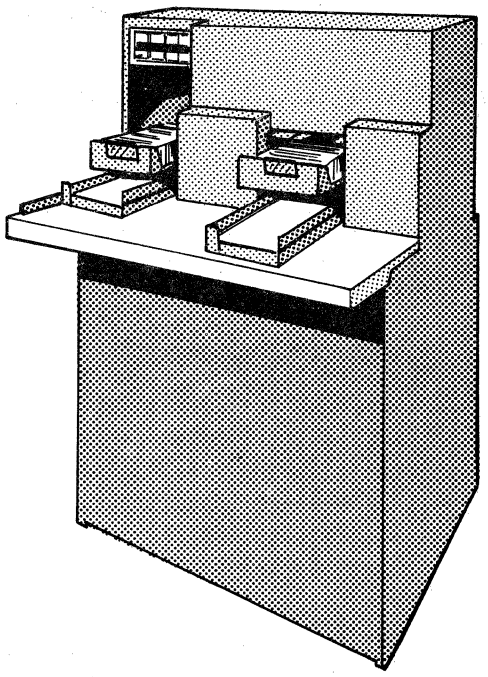
Card Punch Model 4283C records data transferred from the Processor on standard 80-column, 12-row data cards. Data are punched column by column. Each column consists of one 12-bit character and each character is transferred as two data bytes.

Punching Rate; varies by the number of columns punched on each card. If 80 columns are punched, the rate is 60 cards per minute. If 10 or fewer columns are punched, the rate is 200 cards per minute.

Hopper and Stacker Capacities; 1500 cards each.

Device Interface; 3010AE8601 High Speed Data Link Transmitter.

Data Format; after having transferred an appropriate Output Command byte to the interface, the program transfers a data byte containing a byte count specifying one less than the number of bytes to be transferred (159 max. = X'9F'). Each subsequent data byte transfers data to alternate groups of six rows. Bits 0 and 1 of each data byte are discarded. The first data byte is punched in the first six rows and alternate groups of rows are punched from alternate data bytes. The two bytes for a column must be delivered within 4.5 milliseconds. All bytes transferred to the punch are accompanied by one or two Control Line pulses. All bytes but the final byte in a record (one card) are accompanied by one Control Line pulse and the final byte is accompanied by two Control Line pulses. When the punch recognizes the final byte, the punched card is ejected and a new card made ready for punching.



10.5-1 Card Punch

Parity Checking; the interface hardware generates an even parity bit which is checked by the Card Punch but not punched.

Status Sensing; the meaning of the bits in status bytes returned from the Card Punch interface to the Processor is as follows (Fig. 10.5-2) -

- Bit 0 = 1 = Alarm 3. AL3 sets if the punch detects late data, a data parity error, or late card ejection.
- Bit 1 = 1 = Alarm 2. AL2 sets if the punch detects a bin alert.
- Bit 2 = 1 = Alarm 1. AL1 sets if the punch has an open interlock, a mechanism jam, or has detected a misfeed.
- Bit 3 = 1 = Alarm 0. AL0 sets if the punch is off-line, power is off at the punch, or the punch is not connected to the interface.
- Bit 4 = 1 = BUSY. BUSY is set when the interface is not ready to accept data byte. It resets when the interface is ready to accept the next data byte.
- Bit 6 = End of Medium. EOM sets when the last byte for the card has been transferred.
- Bit 7 = 1 = Device Unavailable. DU sets if any one of the Alarm status bits is set or if the punch does not acknowledge a data byte within 700 milliseconds.

Output Commands; command byte bits to the Card Punch interface have the following meaning (Fig. 10.5-2) -

- Bits 0 and 1 are interrupt control bits,

  $\overline{0}\cdot\overline{1}$ = no change.

  $\overline{0}\cdot 1$ = enable interrupts.

  $0\cdot\overline{1}$ = disable interrupts but allow the queue flip-flop to store an interrupt.

  $0\cdot 1$ = disarm interrupts, reset the queue flip-flop.

- Bit 2 = Clear. CLR initializes the High Speed Data Link Transmitter.
- Bit 5 = Not Parity. $\overline{\text{PTY}}$ specifies no parity bit generation. This bit should not be set when a Card Punch is connected to the interface.
- Bits 6 and 7 are record control bits. One or both of these bits must be set in the command byte which precedes the byte count to the interface.

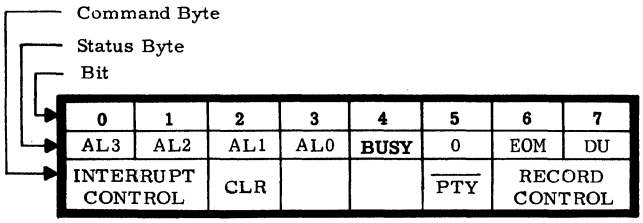


Fig. 10.5-2 Card Punch and Line Printer Command and Status Bytes

Device Address; the standard device address for the Card Punch is X'14'. The address may be changed by screwdriver actuated switches on the interface board.

Interrupts; the interface attempts to interrupt the Processor when it is ready to accept a byte count or a data byte.

10.6 LINE PRINTER

Line Printer Model 4262C accumulates up to 120 characters from the Processor and prints the characters on a single line. The printer employs one print hammer for each pair of character positions and uses a unique method of paper shuttling to print each line with two hammer strokes. A paper transport shifts the paper vertically according to a preplanned format, under program control.

Printing Rate; up to 300 lines per minute.

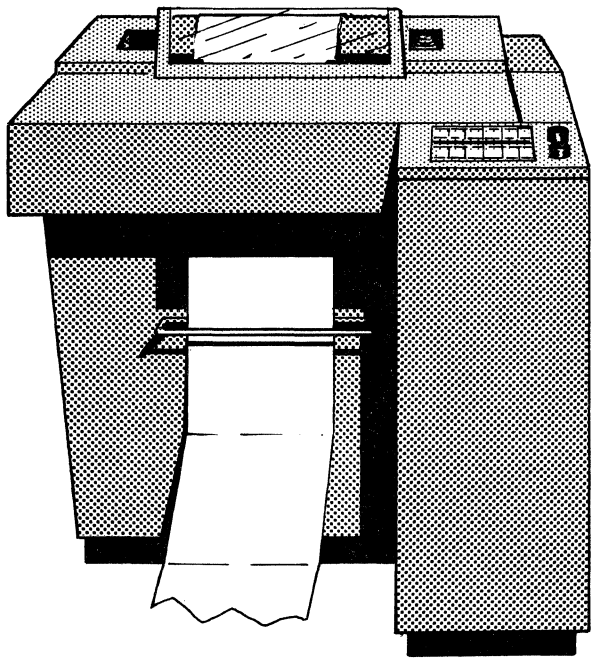
Printer Features; ten characters per horizontal inch and six lines per vertical inch are printed. Vertical skipping speed is 27.5 inches per second, nominal. The paper may be skipped according to a format punched in a vertical format tape, which is installed in the printer, or returned to the top of a page. The character repertoire consists of 63 ASCII upper case characters plus space. Type style is modified open Gothic.

Device Interface; 3010AE8601 High Speed Data Link Transmitter.

Data Format; after having transferred an appropriate Output Command byte to the interface, the program transfers a data byte containing a byte count specifying one more than the number of characters to be printed on the next line (120 + 1 = 122 max. = X'7A'). The program then transfers up to 120 characters to be printed, followed by a vertical format code (X'00' - X'07'). The vertical format code indicates to the printer which of 7 vertical format spacings, pre-punched on the vertical format tape, to use after the line is printed. Finally, the program transfers DC4 (X'14') which is decoded as a print command, the line is printed, and the paper is shifted as dictated by the vertical format code.

Status Sensing; the meaning of bits in status bytes returned from the Line Printer interface to the Processor is as follows (Fig. 10.5-2) -

- Bit 0 = 1 = Alarm 3. AL3 is always zero when the attached device is a Line Printer.
- Bit 1 = 1 = Alarm 2. AL2 sets when the printer detects the yoke open or low paper.
- Bit 2 = 1 = Alarm 1. AL1 sets when the printer has a blown fuse or paper runaway.
- Bit 3 = 1 = Alarm 0. AL0 sets when the printer is off line, power is off, or the printer is not connected to the interface.
- Bit 4 = 1 = BUSY. BUSY is set when the interface is not ready to accept data byte. It resets when the interface is ready to accept the next data byte.
- Bit 6 = End of Medium. EOM sets when the last byte for the card has been transferred.
- Bit 7 = 1 = Device Unavailable. DU sets if any one of the Alarm status bits is set or if the punch does not acknowledge a data byte within 700 milliseconds.



10.6-1 Line Printer

Output Commands; command byte bits to the Line Printer interface have the following meaning (Fig. 10.5-2) -

- Bits 0 and 1 are interrupt control bits,

  $\overline{0}\cdot\overline{1}$ = no change.

  $\overline{0}\cdot 1$ = enable interrupts.

  $0\cdot\overline{1}$ = disable interrupts but allow the queue flip-flop to store an interrupt.

  $0\cdot 1$ = disarm interrupts, reset the queue flip-flop.

- Bit 2 = Clear. CLR initializes the High Speed Data Link Transmitter.

- Bit 5 = Not Parity. $\overline{\text{PTY}}$ specifies no parity bit generation. Since the Line Printer does not check parity, this bit should be set in command bytes issued to the interface.

- Bits 6 and 7 are record control bits. One or both of these bits must be set in command byte which precedes the byte count to the interface.

Device Address; the standard device address for the Line Printer is X'62'. The address may be changed by screwdriver actuated switches on the interface board.

Interrupts; the interface attempts to interrupt the Processor when it is ready to accept a byte count or a data byte.

DIGITAL I/O SUBSYSTEM

The 1401 Digital Input/Output Subsystem controls and monitors process operator interfaces, areas within the process, and process control devices, through digital inputs and digital outputs. The process input and output connections are made at termination assemblies which include terminal strips to which the customer's connections may be made with solderless terminals.

The primary Digital I/O Subsystem provides relay contact outputs, an optional pulse output for stepping motor control stations, digital input terminations featuring signal conditioning, filtering, and optional change detection. Where the digital I/O requirements are less extensive, a smaller Digital I/O Subsystem may be implemented, utilizing a Control Line Module and/or a Sense Line Module.

The small Digital I/O Subsystem may be implemented entirely within the Central System Cabinet and is capable of serving up to sixteen output points and sixteen input points, utilizing terminations of the same type as the larger subsystem. The primary Digital I/O Subsystem is capable of serving a total of 2048 input points and 2048 output points, where a point is defined as one input contact pair or one output contact pair.

11.1 PRIMARY DIGITAL I/O SUBSYSTEM

Where both digital inputs and digital outputs are implemented, both the input and output operations are effected under program control by a 3000AF31 Digital I/O Controller and Multiplexer. The same controller is required if inputs only, or outputs only, are implemented.

11.1.1 Digital Inputs

A block diagram of the digital input portion of the Digital I/O Subsystem is provided on Fig. 11.1-1. The 3000AF31 Digital I/O Controller connects to the computer's Multiplexer Bus, as do all I/O controllers. The controller is capable of serving up to

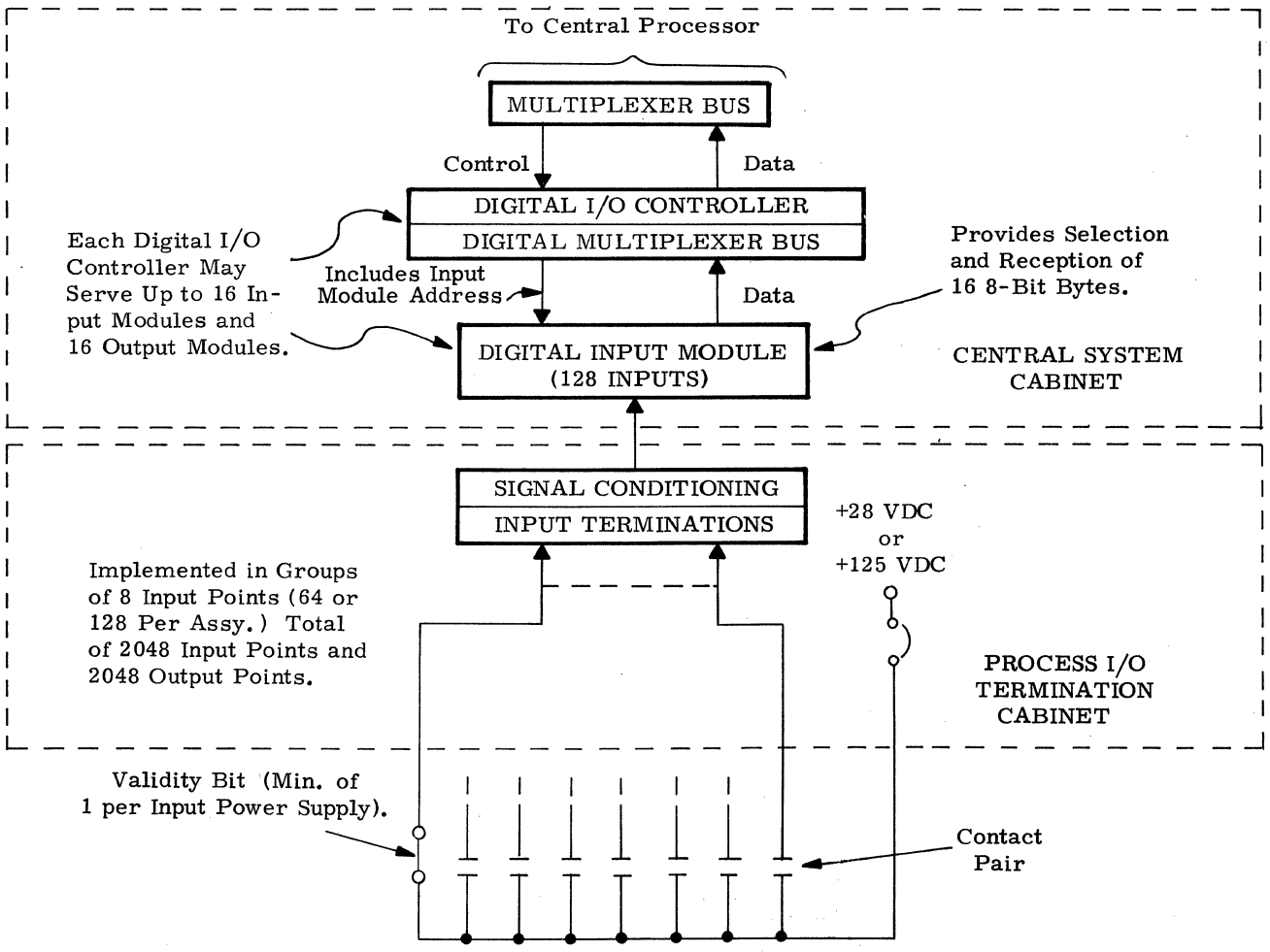


Fig. 11.1-1 Digital Inputs

16 Digital Input Modules and up to 16 Digital Output Modules. The basic 3000AF3101 controller and multiplexer handles up to four input or output modules, and up to seven 3000AF3104 Digital I/O Multiplexers may be added, each to accommodate four additional I/O modules.

Each of up to 16 3010AF3102 Digital Input Modules is capable of selecting and accepting any of sixteen 8-bit input bytes, or the input from up to 128 points. The Input Terminations and Signal Conditioning boards are mounted in a 3010AJ42 Termination cabinet, which may share other process input and output terminations.

The program transfers the address of one of up to 16 Digital Input Modules through the Digital I/O Controller. The four least significant bits in the address byte specify the 8-bit group connected to the selected input module to be read into the Processor in the form of an 8-bit byte. A closed contact pair sets the corresponding bit in the input byte.

Input Signal Conditioning and Terminations:

A 3010AF1401 Digital Input Termination Assembly is capable of accommodating up to 64 input points. A 3010AF Digital Input Termination Assembly may accommodate up to 128 input points. Each of the input Signal Conditioning boards accommodates eight input points. The DC power supply for the input contacts is chosen according to the contact environment. If the contacts are in an environment where they may be contaminated quickly, a +125V supply is chosen. For a normal contact environment, a +28V supply is chosen.

The 3010AF15 or 3010AF16 Signal Conditioning boards are chosen according to the input contact power supply implemented and the filter constant desired. 3010AF15 boards include change detection logic. 3010AF15 boards are standard Signal Conditioning boards and are available as follows:

3010AF1501; 28V, 75 microsecond filter constant.

3010AF1502; 125V, 75 microsecond filter constant.

3010AF1511; 28V, 1 millisecond filter constant.

3010AF1512; 125V, 1 millisecond filter constant.

3010AF1521; 28V, 22 millisecond filter constant.

3010AF1522; 125V, 22 millisecond filter constant.

Change Detect Option:

Any or all Signal Conditioning boards may be specified to incorporate a change detection feature, which generates an interrupt signal as the status of any of the eight inputs to the board changes. The interrupt signal is connected to one of the inputs to the External Interrupt Module (4.4.3). The interrupt may be used to inform the program that a change in one of the inputs has taken place and that the contents of the group should be read.

Standard Digital Input Termination assemblies are wired with the interrupt lines from all input groups tied in an OR connection, so that any change in any of the 64 or 128 inputs will generate a single external interrupt. This wiring may be changed to generate an individual interrupt from any one of the 8-point groups, or any combination from one through eight groups. Signal Conditioning boards incorporating change detection are available as follows:

3010AF1601; 28V, 500 microsecond filter constant.

3010AF1602; 125V, 500 microsecond filter constant.

3010AF1611; 28V, 22 millisecond filter constant.

3010AF1612; 125V, 22 millisecond filter constant.

11.1.2 Digital Outputs

As is shown on Fig. 11.1-2, a 3000AF3101 Digital I/O Controller connected to the computer's Multiplexer Bus serves up to 16 Input Modules and up to 16 Output Modules. The basic 3000AF3101 controller handles up to four input or output modules, and up to seven 3000AF3104 Digital I/O Multiplexers may be added, each to accommodate four additional I/O modules.

Each 3000AF3103 Digital Output Module is capable of selecting any of sixteen 8-point digital output groups, and specifying the status of the eight output relays in the selected group, for a total of 128 output points.

The program transfers the address of one of up to 16 Digital Output Modules through the Digital I/O Controller. The four least significant bits in the address byte specify the 8-bit output group connected to the selected output module, whose relay configuration is to be changed. After the output module and group selection, a data byte is transferred which picks up each relay in the selected group which corresponds to a set data bit, and drops each relay which corresponds to a reset data bit. The relays are held in the last state specified by the Digital Output Module. Loss of power causes all relays to drop (revert to the de-energized state).

Output Relays:

Each 8-point Output Group consists of eight relays with one form A contact pair per relay (single-pole, single-throw). The 3010AF2401 Output Group features relays with 100 VA mercury wetted contacts. The 3010AF2404 Output Group has relays with dry contacts rated for a 10 watt resistive load.

Pulse Generator:

The 3010AF4301 Pulse Generator provides 30 Hz or 60 Hz pulse outputs, generated by an interposer relay, which is activated by the program. Where the customer provides a suitable voltage to the interposer relay contacts, the output pulse train may be used to

drive stepping motor process control stations. The Pulse Generator occupies one Digital Output group slot and is activated when the program transfers an address byte specifying the Output Group address of the Pulse Generator. Other Digital Output Terminations may be used to distribute the pulse train to selected control stations. The program may count the number of pulses generated by counting external interrupts, if an interrupt output from the generator is connected to the External Interrupt Module (4.4.3).

11.1.3 Digital I/O Operating Sequence

The Digital I/O Subsystem may operate in a random addressing mode or a sequential addressing mode. In both modes, the first Write Data instruction immediately following an Output Command transfers the I/O module address to the controller. In the random mode, the next Write Data or Read Data instruction addressed to the Digital I/O Controller transfers data to or from the selected group. In the sequential mode, subsequent Write Data or Read Data instructions transfer the data and automatically increment the I/O module/group address by one.

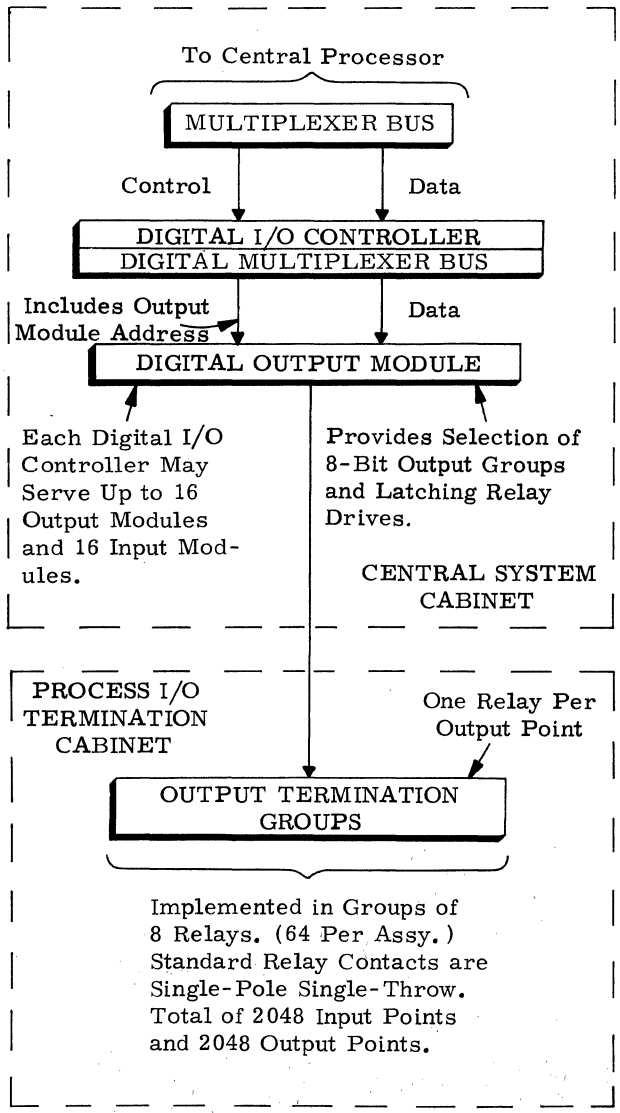


Fig. 11.1-2 Digital Outputs

Status Sensing; Sense Status instructions, Acknowledge Interrupt instructions, and Processor status requests cause a status byte to be transferred from the Digital I/O Controller to the Processor. The meaning of the status byte bits is as follows (Fig. 11.1-3):

- Bit 3 = 1 = External Interrupt. EI is set when one of the attached I/O modules has received an external interrupt.
- Bit 4 = 1 = BUSY. BUSY is reset when the controller is holding a data byte for transfer to the Processor (read) or when it is ready to accept a byte from the Processor (write).
- Bit 5 = 1 = Examine. EX = EI.
- Bit 7 = 1 = Device Unavailable. DU sets when a non-existent I/O module is addressed.

Command Byte
Status Byte
Bit

0	1	2	3	4	5	6	7
0	0	0	EI	BUSY	EX	0	DU
INTERRUPT CONTROL				RAND	SEQ	WRT	READ

Fig. 11.1-3 Digital I/O Controller Command and Status Bytes

Output Commands; a command byte is transferred to the Digital I/O Controller when an Output Command addressed to the controller is executed. The command byte bits have the following meaning (Fig. 11.1-3):

Bits 0 and 1 are interrupt control bits -

$0 \cdot \overline{1}$ = disable the interrupt but allow the queue flip-flop to store an interrupt.

$0 \cdot 1$ = disarm interrupts; hold the queue flip-flop reset.

$\overline{0} \cdot 1$ = enable interrupts.

The controller interrupt occurs when BUSY resets, and in this case, is a data ready or ready to transfer interrupt. The interrupt also occurs if the external interrupt line to one of the I/O modules is grounded.

- Bit 4 = 1 = Random. RAND specifies the random addressing mode.
- Bit 5 = 1 = Sequential. SEQ specifies the sequential addressing mode.
- Bit 6 = 1 = Write. In the WRT mode, data bytes are transferred to the selected digital output group by Write Data instructions.
- Bit 7 = 1 = READ. In the read mode, data bytes are read-in from the selected digital input group by Read Data instructions.

Initialization:

When the initialize button on the Display Panel is pushed, the controller goes to the random read mode, all status bits are reset, and the interrupt queue flip-flop is reset.

Digital I/O Controller Address:

The controller is normally assigned device address X'4B'. The address may be changed by jumper wiring on the controller.

I/O Module Addressing:

The I/O module addresses are assigned sequentially from 0 to 15 (X'0' through X'F'). The I/O module is addressed by the byte transferred by the first Write Data instruction addressed to the Digital I/O Controller, following an Output Command addressed to the controller. The I/O module address is contained in bits 0 through 3 of that byte. Each I/O module may serve up to 16 I/O groups and the group address is specified by bits 4 through 7 of the address byte.

11.2 SMALL DIGITAL I/O SUBSYSTEM

The Small Digital I/O Subsystem consists of a 3000AF1201 Sense Line Module and/or a 3000AF2102 Control Line Module, plus up to 32 Digital I/O Terminations. Each such subsystem implements up to 16 digital input points and up to 16 digital output points.

11.2.1 Sense Line Module Inputs

The Sense Line Module is installed in any available slot on the Computer's Multiplexer Bus and provides an inexpensive means to sense the status of up to 16 digital inputs. The data on the 16 input lines is read into the Processor by the program through the transfer of two data bytes in response to Read Data instruction addressed to the Sense Line Module. Logic is contained within the module which causes alternate 8-line groups to be read. The first Read Data instruction following an RSET Output Command addressed to the module transfers the data from the most significant 8 inputs and the second data byte transfers the least significant data byte. Subsequent Read Data instructions are presumed to transfer alternate upper and lower bytes. An external interrupt input point is provided on the module which may be grounded momentarily by a customer connection to generate a Sense Line Module interrupt which informs the program that the inputs should be read.

The Sense Line Module is normally assigned device address X'11'. The address may be changed by jumper wiring on the module.

Status Sensing; the status byte is meaningful only if the customer has connected a jumper wiring option which resets the BUSY bit (bit 4) when new sense line data is available to be read-in.

Output Commands; the command byte bits have the following meaning (Fig. 11.2-1):

- Bits 0 and 1 = interrupt disable and enable, respectively. When the interrupt is disabled, the queue flip-flop is not reset, and may queue interrupts until serviced. The interrupt is meaningful only if the user elects to implement the external interrupt line to the Sense Line module.
- Bit 3 = 1 = Reset. RSET sets up the Read Data steering logic so that the next Read Data instruction will read the upper 8-bit byte.

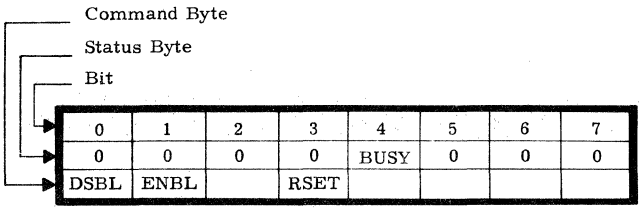


Fig. 11.2-1 Sense Line Module Status and Command Bytes

Input Terminations:

The terminations are made at a 3010AF33 Termination Assembly into which one or two 8-point 3010AF2401 Buffer Relay boards are installed. The relays may be powered by customer supplied power (12V) or by 3010AL35 or AL38 power supplies. In this application, the customer's input energizes the corresponding relay coil, which then closes its contacts to set the corresponding bit in the input data byte. The relay coil draws a nominal 11 milliamperes at 12 VDC.

11.2.2 Control Line Outputs

A Control Line Module provides an inexpensive means of controlling up to 16 digital output points. This module may be installed in any available slot on the computer's Multiplexer Bus. Each of the 16 output lines is controlled by an individual flip-flop and relay driver in the module. The 16 flip-flops are configured by the program through the transfer of two data bytes to the Control Line Module. A single Output Command instruction resets all of the flip-flops, turning off the relay drivers.

The data bytes are transferred by two Write Data instructions addressed to the Control Line Module. The first Write Data instruction following an Output Command transfers the most significant eight bits. The lower eight bits are transferred by a second Write Data instruction. Subsequent Write Data instructions are presumed to be transferring alternate upper and lower bytes. The Control Line Module generates no interrupts. It is normally assigned device address X'71'. The address may be changed by jumper wiring on the module.

The output terminations are implemented by a 3010AF33 Termination Assembly into which one or two 8-point 3010AF2401 Buffer Relay boards may be installed. The relays are powered by 3010AL35 or AL38 12V power supplies and are controlled by the drivers in the Control Line Module. A set bit in a data byte ~~energizes~~ the corresponding output relay and ~~closes~~ its form A contact pair. The contacts are mercury wetted and rated for 100 VA.

de-energizes

opens

4/17/91 DMD

ANALOG INPUT/OUTPUT SUBSYSTEM

The 1102 Analog Input/Output Subsystem may incorporate an analog input scanner, absolute analog outputs, and variable analog current pulse outputs. A basic 3010AG63 Analog I/O Controller provides the interface between the computer's Multiplexer Bus and any or all three functional analog I/O areas. The process input and output connections (except absolute analog outputs) are made in termination cabinets. Up to 16 absolute analog output point terminations are made in the Central System Cabinet. Fig. 12.1 is a block diagram of the overall subsystem. All subsystem functions are optional and may be added on a plug in basis.

The analog inputs may be representative of a wide variety of process conditions such as temperatures, pressures, flow rates, voltages, etc., and these are converted to a digital data for input to the Central Processor. The variable current pulse outputs provide precise set point control signals to process supervisory or control stations. The absolute analog output voltages are suitable for driving strip recorders, meters, analog set point controllers, etc.

All Analog I/O Subsystem operations are initiated by the execution of input/output instructions by the Central Processor. The Analog I/O Controller decodes the commands issued by the program and initiates the appropriate action. All three functional areas may operate independently of each other and all three can function simultaneously, provided that the sequence of commands necessary to initiate one operation is completed before another command sequence is started to initiate another operation.

12.1 ANALOG INPUTS

Up to 256 analog input points may be scanned by a single subsystem. As many as four subsystems (each including the basic 3010AG63 controller) may be incorporated in a GE-PAC 3010 system to bring the total number of points scanned to 1024. The subsystem accepts the following types of input signals for conversion to digital data words of 12 bits plus a sign bit, at up to 100 randomly scanned points per second.

- Voltages with full scale values in the range of ± 10 millivolts to ± 500V.
- Currents ranging from 1 milliampere to 50 milliamperes.
- Bridge Circuit Resistances in the range of 9.5 ohms to 1050 ohms.
- Thermocouples of any type are accommodated by a Cold Junction Reference for standard precision or a Termination/Reference Unit for high precision.

12.1.1 Analog Input Parameters

The terms used in the accuracy statements are defined in Appendix A of this manual and on G. E. drawing no. 70A121205. When properly maintained and when the recommended offset error correction methods* are used by the software, the accuracy and principal parameters of the analog scanner are:

- Speed; 200 points per second in a random scan mode. A pin selectable 100 pps option is provided.
- Point Switching; Form C.
- Subsystem Gain Error; ±0.025% of full range ±5 μv, referred to the input.
- Repeatability Error; ±0.025% of full range ±10 μv, referred to the input.
- Common Mode Voltage Rejection; 10^6:1 minimum at a gain setting of 1000:1. Maximum common mode voltage at any input termination point is ±250 VDC or 500V peak to peak at 60 Hz.
- Crosstalk Rejection; 120 db minimum from DC to 60 Hz.
- Gain Error Temperature Coefficient; ±0.0045% of full range per °C.
- Alarm Indications Available to the Program: A/D Converter Overflow; Multiple Relay Selection Error.

12.1.2 Amplifier and Gain Options

The 3010AG69 Analog Input Amplifier amplifies the output of the input point multiplexer to the optimum level for input to the A/D Converter. It also provides isolation between the multiplexer and converter and isolates common mode voltages from the converter input. Three amplifier options are available:

*RTMOS-30 makes the offset correction from offset data accumulated by the user program. The program periodically scans a shorted input after issuing an Output Command with bit 4 of the command byte set (see Output Commands under 12.4).

- 3010AG6903 Fixed Gain Amplifier; the gain of this amplifier is specified as one of the following - 1.0, 2.0, 4.0, 31.25, 62.5, 125, 250, 500, 1000, and 2000.

- 3010AG6904 Selectable Gain Amplifier; the gain of this amplifier is selected by a control on the amplifier as one of the following - 2.0, 4.0, 31.25, 62.5, 125, 250, 500, 1000, and 2000.

- 3010AG6905 Programmable Gain Amplifier; the gain of this amplifier is set by the program (12.4.1) to one of the following gain ratios -

Ratio	Full Scale Input
1.0:1	10 volts
62.5:1	160 mv
125:1	80 mv
250:1	40 mv
500:1	20 mv
1000:1	10 mv

12.1.3 Analog Input Terminations

Each analog input signal is connected by the customer to an analog input point on a 3010AG61 Termination Assembly. This assembly accommodates up to 32 inputs on terminal strips which accept solderless terminals. Up to eight termination assemblies may be installed in a 3010AJ42 Termination Cabinet, and the 256 points which may be scanned by a single 1101 Analog I/O Subsystem may therefore be accommodated in a single termination cabinet. If a smaller number of input points are implemented, other process I/O terminations may share the cabinet.

Input Multiplexer and Signal Conditioning:

The Analog Input Multiplexer consists of one 3010AG62 Point Switch for each four points implemented, and one 3010AG70 Matrix Switch for each 32-point Termination Assembly. Signal conditioning is accomplished by boards which plug into the termination assembly in slots which alternate with the Point Switches. Each Signal Conditioning board has four identical circuits to accommodate up to four input points. The signal conditioning circuits convert the input signal into representative voltage within the input range of the Analog Input Amplifier. Signal Conditioning boards may also provide appropriate low pass filtering of the input signals. Standard Signal Conditioning boards of the following types are available. Refer to G.E. drawing no. 70A122720 for an index and description of available Signal Conditioning boards.

Signal Conditioning

3010ASFL Filter, ±10 mv to ±640 mv

3010ASAF Attenuator, to ±500V

3010ASIM Current Input, to 50 ma

3010ASOT Thermocouple Input with Open TC Detector

3010ASRT Resistance Bridge (RTD) Inputs

3010ASAP Attenuator with Slidewire Power Output

Thermocouple Inputs. The transition from thermocouple wire to copper wire for thermocouple input points is made at the input termination points in an analog input Termination Cabinet for the standard precision method, or in an external module for the high precision method. Since the transition points, themselves form thermocouples, it is necessary to measure the temperature of the termination interface and to provide an analog voltage representation of that temperature to the program through an additional analog input point. The program uses the digitized representation of the reference temperature to compensate for the termination temperature.

- 3010AG64 Cold Junction Reference: This package provides the reference signal for standard precision thermocouple terminations. The termination cabinet temperature is monitored to develop the temperature reference analog input signal. When this option is implemented the reference temperature error is ±2 °C maximum.

- 4161A Thermocouple Termination/Reference: This optional package provides high precision thermocouple terminations in a separate module located physically and electrically between the termination cabinet and the process. The module may accommodate up to 64 thermocouple terminations of any mixture. The thermocouple signal voltages and the reference temperature voltage are cable connected via copper wire to the standard analog input terminations in the termination cabinet. When this option is implemented, the reference temperature error is ±0.5 °C maximum.

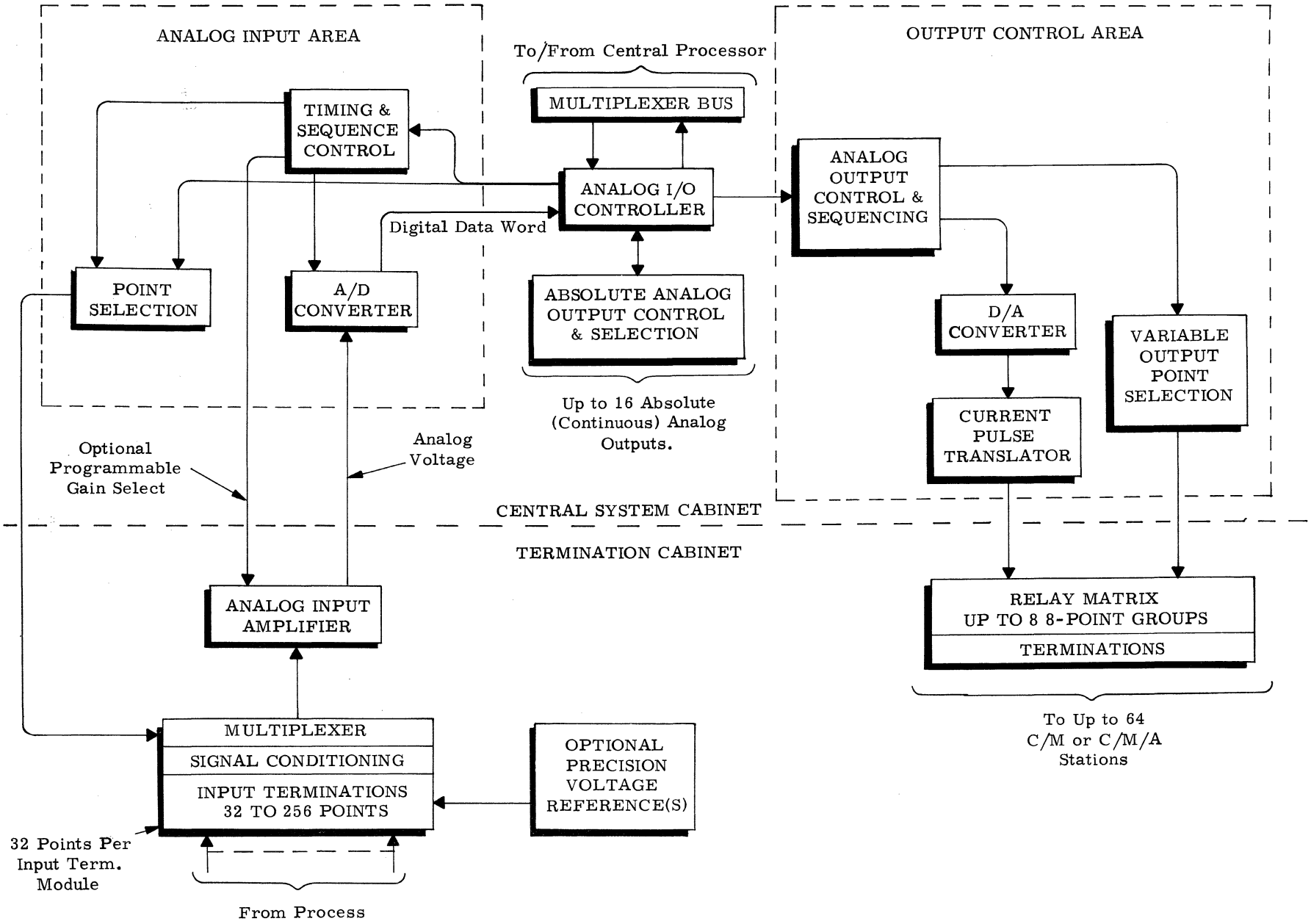


Fig. 12.1 Analog I/O Subsystem

Precision Voltage Reference. The 3010AG86 Voltage Reference module provides precise (±0.01%) reference outputs of 10, 20, 40, 80, 160, 320, and 640 millivolts. The module is installed in a Termination Cabinet and one or more of the outputs may be connected to analog input points for accuracy checking and Analog Input Subsystem maintenance.

12.2 ABSOLUTE ANALOG OUTPUTS

The Absolute Analog Outputs are continuously applied to user devices such as trend recorders, plotters, meters, etc. The basic 3010AG6301 Analog I/O Controller must be implemented, plus a 3010AG6303 Output Control. In addition, from one to eight Analog Output boards are installed in the Analog I/O module. These are 3010AG6303 (10-bit resolution) or 3010AG6304 (12-bit resolution). A 3010AL51 or AL42 15V Power Supply must be installed in the CSC to supply power to these output boards. Up to 16 customer supplied terminations may be served by a cable from the Analog Output boards.

With the Analog I/O Subsystem in the Absolute Analog Output Mode, the program transfers the address of a point whose output value is to be changed and a 2-byte data word to the controller. The new value is then directed to the selected point. The output parameters are as follows:

- Output Voltage. One of the following output vcltage ranges is selected by jumper pins on each implemented Absolute Analog Output board;

  0V to +10V

  -5V to +5V

  -10V to +10V

- Conversion Accuracy. ±0.1% of full range (12-bit resolution); ±0.2% of full range (10-bit resolution).
- Stability. ±0.1% of full range over 1000 hours (12-bit); ±0.2% of full range over 1000 hours (10-bit).
- Minimum Load Resistance. 100 ohms.
- Output Data Word. The digital data word consists of 10 bits or 12 bits. If the -5V to +5V range or the -10V to +10V range is selected, the full scale negative output voltage is generated when the data word is all zeros. The output voltage is zero if only the most significant bit is set, and the full scale positive output is generated when all bits are set.

12.3 VARIABLE OUTPUTS

Up to 64 computer/manual or computer/manual/automatic process control stations may be served by the Variable Output Modules. The variable output signals are precise analog current pulses which are representative of a digital data word transferred to the Variable Output Controller by the program. The pulses are typically applied to a holding amplifier in the selected control station to direct the station to establish a new set point value within the process.

The basic 3010AG6301 Analog I/O Controller must be implemented, plus a 3010AG6305 Variable Output Controller. In addition, a 3010AJ42 Termination Cabinet must implement a 3010AG25 64-Point Variable Output Termination Assembly, a 3010AG27 Overload/Output Disable module, and from one to eight 3010AG26 8-Point Variable Output Multiplexers.

When the Analog I/O Subsystem is in the Variable Output mode, the program transfers a point address to the Variable Output Controller, followed by a two-byte digital data word. When the output point has been selected, a two-millisecond current pulse is applied to the selected station. The current pulse amplitude corresponds to the contents of the output digital data word. The Variable Output parameters are as follows:

Speed; random point addresses may be selected at up to 200 points per second. Any single point may be selected up to 50 points per second.

Pulse Type and Duration; incremental 2.00 millisecond ±0.02% current pulses of variable amplitude.

Full Scale Amplitude; from -12.500 milliamperes to +12.488 milliamperes. The smallest incremental current change is 0.012 milliamperes.

Accuracy; ±0.075% of full range. Temperature coefficient is ±0.005% of full range per °C. Each of these terms is as measured at the output termination terminals.

Maximum Common Mode Voltage; 1 VDC or peak AC at 60 Hz.

Alarm Indication Available to Program; Multiple Relay Selection Error.

Resolution; the digital output data words consists of ten bits plus a sign bit.

12.3.1 Control Station Interface

Terminals are provided in the output termination assembly to permit the output wiring to be configured as required to drive various types of stations. As an example, a single output line may be directed to all stations and the relay multiplexer may select the stations by providing a common return line, or each station may be served by individual output lines which are selected by the multiplexer.

12.4 ANALOG I/O SUBSYSTEM OPERATING SEQUENCES

The subsystem is exercised by user instructions addressed to the Analog I/O Controller. The mode of operation of the subsystem is specified by Output Command instructions, subsystem status is reflected in status bytes returned in response to Sense Status or Acknowledge Interrupt instructions, I/O point addresses are specified by Write Data instructions, data are input by Read Data instructions, and output data is transferred by Write Data instructions. A special Detailed Status byte may be returned to the Processor by a Read Data instruction when the controller is in the Read Detailed Status mode.

Status; the overall subsystem status is reflected in the status byte illustrated on Fig. 12.4-1 and the status bits have the following meaning;

- Bits 0 and 1 reflect the controller mode as specified by the last Output Command. The bits have the same form as bits 2 and 3 of the Output Command.
- Bit 2 = 1 = Input Conversion Complete. The "I" bit sets when the controller is in the Analog Input Mode and the conversion of the specified analog input point value to digital data is complete. The controller interrupt occurs when "I" sets, if enabled.
- Bit 3 = 1 = Output Complete. The "O" bit sets when a Variable Output current pulse has been delivered to the selected point. The controller interrupt occurs when "O" sets, if enabled.
- Bit 4 = 1 = BUSY. BUSY sets when the functional area specified by the Output Command mode bits has begun the conversion of data for the specified operation, and remains set until the operation is complete. The Analog I/O Controller interrupt queue flip-flop sets as the BUSY bit resets, if it has not been disarmed by an Output Command.
- Bit 5 = 1 = Examine. EX indicates that a hardware alarm condition has been detected and the Detailed Status should be read.
- Bit 6 = 1 = End of Medium. EOM is reset when data transfers are in progress. New Output Commands specifying input or output operations should be issued only when EOM is set.
- Bit 7 = 1 = Device Unavailable. DU = EX.

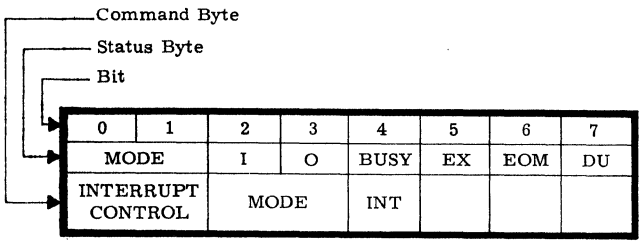


Fig. 12.4-1 Analog I/O Subsystem Command and Status Bytes

Output Commands; the Output Command bits have the following meaning (Fig. 12.4-1);

- Bits 0 and 1 specify the controller interrupt logic status as follows -

  $0 \cdot \overline{1}$ = Disable interrupts but allow the queue flip-flop to store interrupts.

  $\overline{0} \cdot 1$ = Enable interrupts.

  $0 \cdot 1$ = Disarm interrupts reset the queue flip-flop.

  $\overline{0} \cdot \overline{1}$ has no effect on the controller.

- Bits 2 and 3 specify the mode of operation for the subsystem as follows -

  $\overline{2} \cdot \overline{3}$ = Read Detailed Status.

  $\overline{2} \cdot 3$ = Analog Input Mode.

  $2 \cdot \overline{3}$ = Variable Output Mode.

  $2 \cdot 3$ = Absolute Analog Output Mode.

  } Reset Byte Counter

- Bit 4 = 1 = Initialize. INT initializes the controller (used for testing only).

Read Detailed Status Mode: After the controller is placed in the Read Detailed Status mode, a Read Data instruction will transfer the Detailed Status byte to the Processor. The Detailed Status bits have the following meaning (Fig. 12.4-2);

- Bit 0 = 1 = Overflow. OVF sets if an analog input data conversion overflows due to the magnitude of the input to the A/D Converter exceeding the capacity of the 12-bit plus sign converted data register.

- Bit 1 = 1 = Relay Error - Input. RLI sets if more than one input point multiplexer relay picked up as an input point selection was attempted.

- Bit 2 = 1 = Relay Error - Output. RLO sets if more than one output point multiplexer relay picked up as an output point selection was attempted.

- Bits 3 and 4 are representative of the controller byte counter which retains a count of Read Data and Write Data byte transfers necessary for various subsystem operations.

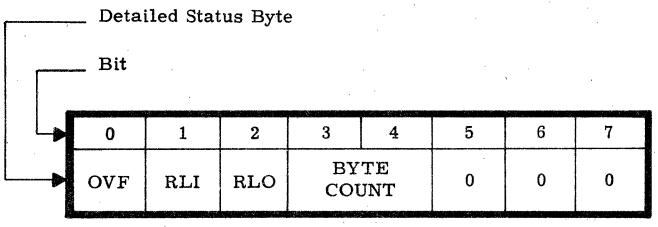


Fig. 12.4-2 Detailed Status Byte

Device Address: The first Analog I/O Controller implemented in a system is normally assigned device address X'5A'. Subsequent controllers are normally assigned X'6A', X'7A', and X'8A'. The controller address is selected with screwdriver actuated switches on the module.

12.4.1 Analog Input Mode

The first Write Data (WD) instruction addressed to the Analog I/O Controller after it has been placed in the Analog Input mode, transfers a byte which specifies the Programmable Amplifier gain, if that option is implemented. The first WD also enables the relay multiplexer (unless bit 4 was set), and sets the byte counter to 01 (Fig. 12.4-3).

A second WD specifies the point to be selected (Fig. 12.4-3), sets the EOM and BUSY status bits, and resets the byte count to 00. When the conversion is complete status bit I is set, BUSY clears, and the interrupt queue flip-flop sets.

The converted digital data is transferred to the processor by two Read Data (RD) instructions (Fig. 12.4-3). After the first RD, the byte counter goes to 01. When the second RD is executed, the byte counter goes to 00.

If additional WD instructions are issued when the byte counter is clear, the byte transferred to the controller by those instructions specifies a new point to be selected and initiates another conversion.

12.4.2 Variable Output Mode

The first WD instruction addressed to the Analog I/O Controller after it has been placed in the Variable Output mode, transfers the variable output point address and sets the byte count to 10. The second WD instruction transfers the sign bit and 7 most significant data bits, and decrements the byte count to 01. A third WD transfers the 3 least significant data bits, initiates the conversion of data, clears the byte counter, and sets status bits EOM, and BUSY. See Fig. 12.4-4.

When the conversion of data and delivery of the current pulse to the selected point is complete, status bit "O" is set, BUSY resets, and if enabled, the controller interrupt is generated. Any attempt to issue a WD or RD instruction to the controller while the BUSY status bit is set will be ignored. The controller mode may be changed when the EOM status bit or the BUSY status bit is set.

12.4.3 Absolute Analog Output Mode

The first WD instruction addressed to the Analog I/O Controller after it has been placed in the Absolute Analog Output mode, transfers the absolute output point address and sets the byte count to 10. The second WD instruction transfers the sign and seven most significant data bits, and decrements the byte counter to 01. The third WD transfers the two least significant data bits, initiates data conversion, the application of the output to the selected point sets the EOM status bit, and resets the byte count to 00. See Fig. 12.4-5.

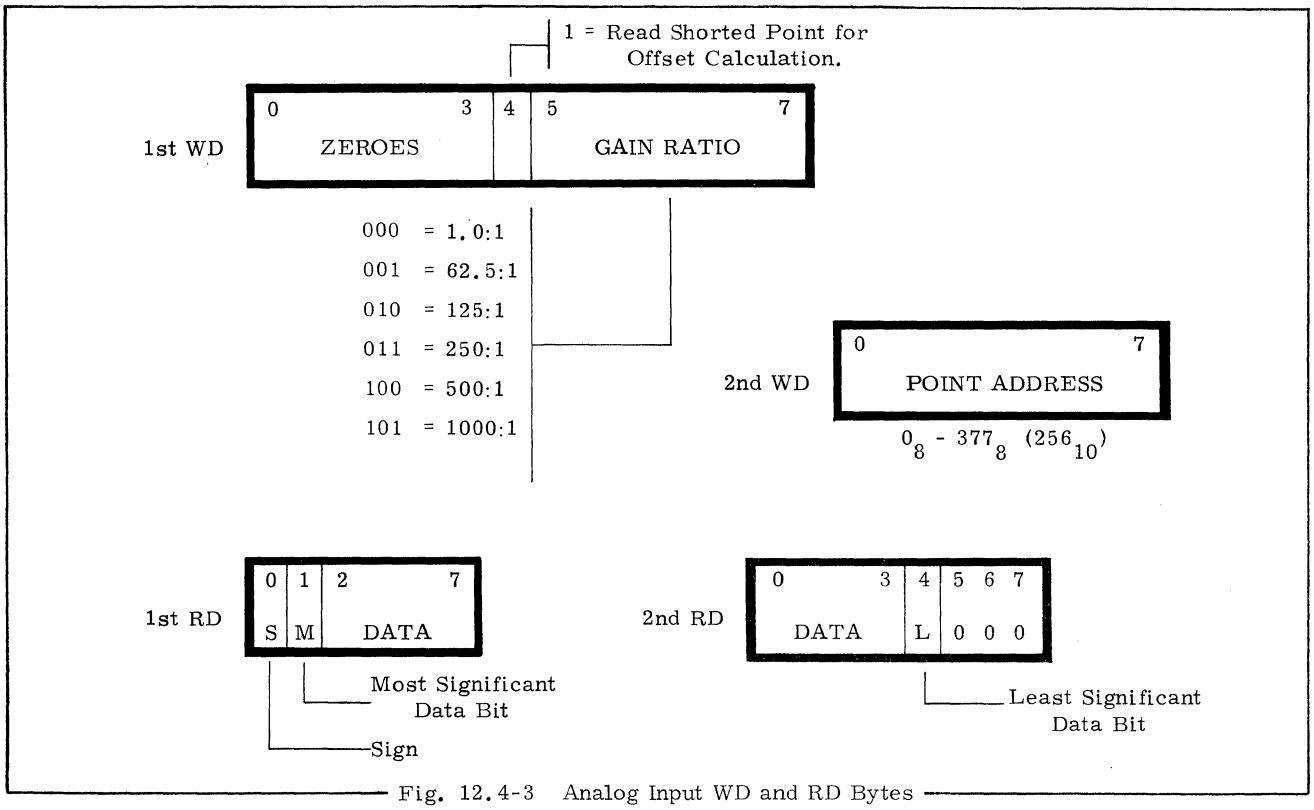


Fig. 12.4-3 Analog Input WD and RD Bytes

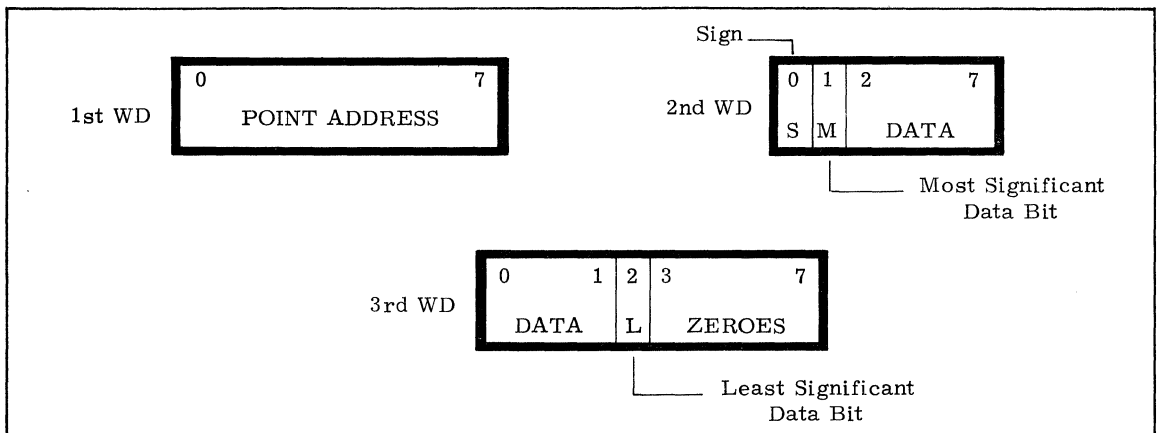


Fig. 12.4-4 Variable Output WD Bytes

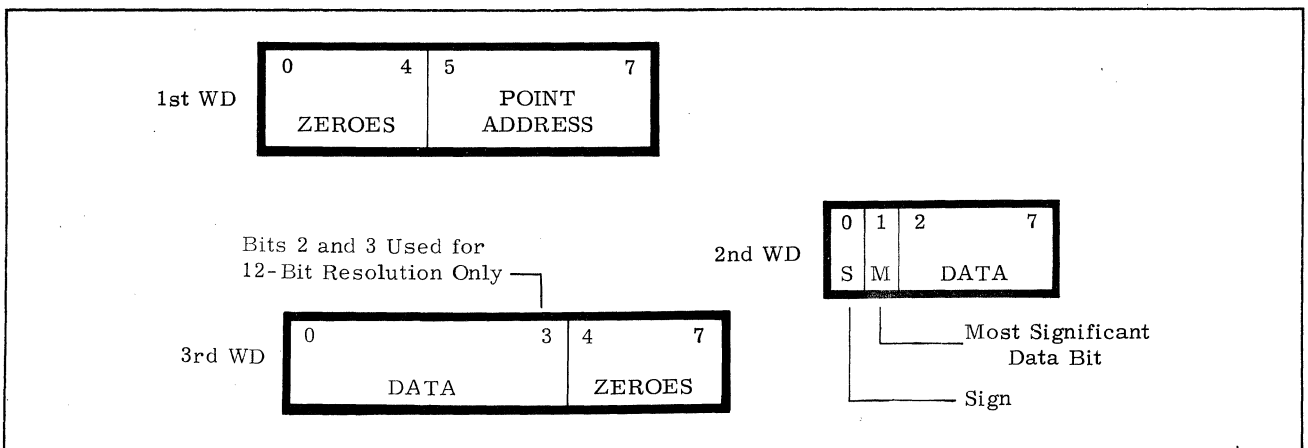


Fig. 12.4-5 Absolute Analog Output WD Bytes

ALPHA-NUMERIC VIDEO DISPLAYS

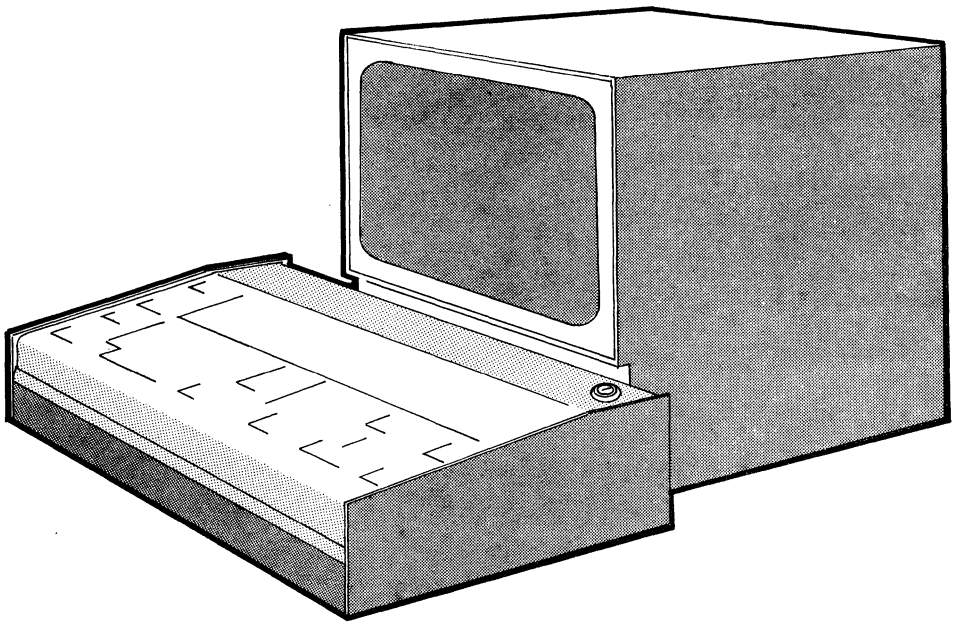


Fig. 13.1 Display Terminal

The standard GE-PAC 3010 Process Operator's Console is a video Display Terminal which consists of a television type display and a keyboard. The interface between the computer and the Display Terminal is provided by a free-standing table-top style 4291BS026 Display Controller Unit (DCU-776). Other process operator/computer interfaces are possible, such as consoles which interface with the Digital I/O Subsystem and incorporate switches, indicator lamps, digital displays, etc., but the Display Terminal provides a more flexible interface with an almost unlimited variety of display formats, at lower cost in most cases.

The interface between the Multiplexer Bus in the Central Processor and the Display Controller is provided by a 3010AH1401 Synchronous Drive Interface which is located in the Central System Cabinet (see 14.1). The synchronous drive and the Display Controller are interconnected by a single multi-conductor cable, up to 50 feet in length. The Display Controller and Display Terminal are interconnected by two coaxial cables, which may be up to 1000 feet in length.

13.1 OPTIONS

13.1.1 Display Controller Units

Display Controller Units are available with and without table tops. While the standard Display Controller serves a Display Terminal with 22 display rows with 46 character positions per row and a total of 1012 character positions per display, 92 characters per row Display Controllers are also available, providing a total of 2024 character positions on the display. A 46 characters per row Display Controller may implement a Memory Expansion Unit (MEU) which allows the controller to serve a second Display Terminal. The model numbers for each of the available Display Controller Units are as follows:

4291BS025; without table top, 46 characters per row, serving a single Display Terminal.

4291BS026; with table top, 46 characters per row, serving a single Display Terminal.

4291BS027; without table top, 46 characters per row, serving two Display Terminals.

4291BS028; with table top, 46 characters per row, serving two Display Terminals.

4291BS033; without table top, 92 characters per row, serving a single Display Terminal.

4291BS034; with table top, 92 characters per row, serving a single Display Terminal.

When directly connected to the Synchronous Drive Interface in the CSC, the Display Controller may be located up to 50 cable feet from the connection point. In this case, a Direct Timing Source (DTS) must be installed in the Display Controller to provide the communications channel clocks at 4800 baud. If synchronous digital data sets, such as Model 4293AS032, are

implemented at each site, the communications may be over telephone lines at 2000, 2400, or 4800 baud, as dictated by the data sets used. The interface complies with EIA Standard RS-232C.

The Display Controllers listed previously include the Direct Timing Source. Where data sets are used, the DTS is not used, and the clocks are supplied by the data sets. To determine the model number for a Display Controller without the DTS, subtract four from the number for a 46 characters per row unit (4291BS026 becomes 4291BS022), or subtract two from the number for a 92 characters per row unit (4291BS034 becomes S032).

13.1.2 Display Terminals

The standard Process Operator's Console consists of a Display Monitor with a 14" diagonal screen size and an EKB-765 Operator Oriented Keyboard. 23" Display Monitors are also available, as are EKB-761 "office style" keyboards.

The EKB-765 Operator Oriented Keyboards have the letter and number keys arranged in alpha-numeric order and may include up to 45 Action Keys which initiate the transmission of a message to the computer, including two pre-determined function codes to identify which key was pushed, plus the contents of the first row on the display. These keyboards also have an Entry Marker Control key group (EMC).

The EKB-761 keyboards have the alpha-numeric keys arranged as on an office keyboard. These keyboards may have up to 16 Function Keys which initiate the transmission of a message to the computer starting at the first position on the display and continuing to the position of the entry marker at the time the Function Key was pushed. The message includes a function code character which identifies which key was pushed. EKB-761 keyboards may also include an Entry Marker Control key group (EMC).

The standard Process Operator's Console is a Display Terminal with a 14" monitor and an EKB-765 Operator Oriented Keyboard with at least 15 Action Keys. The model numbers for the available Display Terminals are as follows:

4292AS012; 14", EKB-761, with EMC, no Function Keys.

4292AS013; 14" EKB-761, with EMC and 16 Function Keys.

4292AS014; 14", EKB-765, no Action Keys.

4292AS015; 14", EKB-765, 15 Action Keys.

4292AS016; 14", EKB-765, 30 Action Keys.

4292AS017; 14", EKB-765, 45 Action Keys.

4292AS022; 23", EKB-761, with EMC, no Function Keys.

4292AS023; 23", EKB-761, with EMC and 16 Function Keys.

4292AS024; 23", EKB-765, no Action Keys.

4292AS025; 23", EKB-765, 15 Action Keys.

4292AS026; 23", EKB-765, 30 Action Keys.

4292AS027; 23", EKB-765, 45 Action Keys.

A Display Terminal may have any number of repeater monitors connected in parallel with the primary monitor, so long as the total display video cable length does not exceed 1000 feet. Model no. 4292AS011 is a 14" repeater monitor. Model no. 4292AS021 is a 23" repeater monitor.

13.2 OPERATIONAL FEATURES

The Display Controller utilizes a magnetostrictive delay line memory to store the information displayed on one terminal. New information may be entered from the computer or from the keyboard. A single controller may serve two separately addressable memories and terminals by incorporating a second Terminal Memory Unit (TMU). The second memory may be added in the field by installing a Memory Expansion Unit (MEU), using MEU Adder 4291BS041.

Each display consists of 22 character-lines with 46 character positions on each line, or 1012 character positions per display. The TMU serving each Display Terminal stores the displayed characters while a composite video generator in the Display Controller reproduces the characters on a standard 525 raster line, 30 frames per second, interlaced scanning, television type display.

An entry marker (blinking overline) indicates the character position where the next character from the computer or the keyboard will be entered. The entry marker may be positioned by control characters in messages from the computer or by the keyboard operator. When transmitting messages to the computer, the entry marker indicates the first text character in the message.

Keyboards are available which allow the operator to place an end-of-text symbol (▮) in any position on the display to indicate that the preceding character is the final character to be transmitted in a message to the computer. The standard Operator Oriented Keyboard used in this application (EKB-765) does not place such a symbol on the display, but enables logic in the Display Controller which automatically terminates messages at the end of one line.

After having composed a message on line one of the display and having visually verified its contents, the operator initiates a transmission request via one of 45 Action Keys. These keys cause the entry marker to be positioned in the first position on the display. When the Display Controller services the transmission request, the entry marker moves across the first displayed line as the message is transmitted, and stops in position one on the next line. The Display Controller includes two function code characters in the message which identify which key was pushed. The program identifies the action requested by evaluating the two function code characters. The keys may be specially marked for individual process applications to indicate the action requested in process operator terms.

Two additional transmit request keys are provided which function in the same manner as the Action Keys, except that one moves the entry marker to the beginning of the current line and the other does not move the entry marker. These two keys initiate message transmissions, from the beginning of the line containing the entry marker, or from the current entry marker position.

13.2.1 Message Formats

Message exchanges between the computer and the Display Controller utilize synchronous bit-serial ASCII character transmissions. Each character consists of seven data bits and an odd parity bit. Each message header includes an address character which indicates to which of the Display Terminals a message is directed, or from which Display Terminal the message originated. Messages may be information messages, acknowledgement messages, or negative acknowledgement messages. A reply to each information message is expected, and if it is a "negative acknowledge" reply, retransmission of the last information message is expected.

Each of the ASCII upper case alpha/numeric characters is included in the character set. Five special characters are also provided, four of which may be used to generate graphic displays: | , | , ‾‾ , and ⌜‾ . The fifth is a "blink" character, which causes all displayed characters following it, up to the next space or the end of the line, to blink.

Each message header is preceded by at least four ASCII synchronization characters (SYN, 026_8) which synchronize the Display Controller and the computer's Synchronous Drive Interface. The SYN characters from the computer are generated by the program, and those from the Display Controller are generated automatically by the hardware.

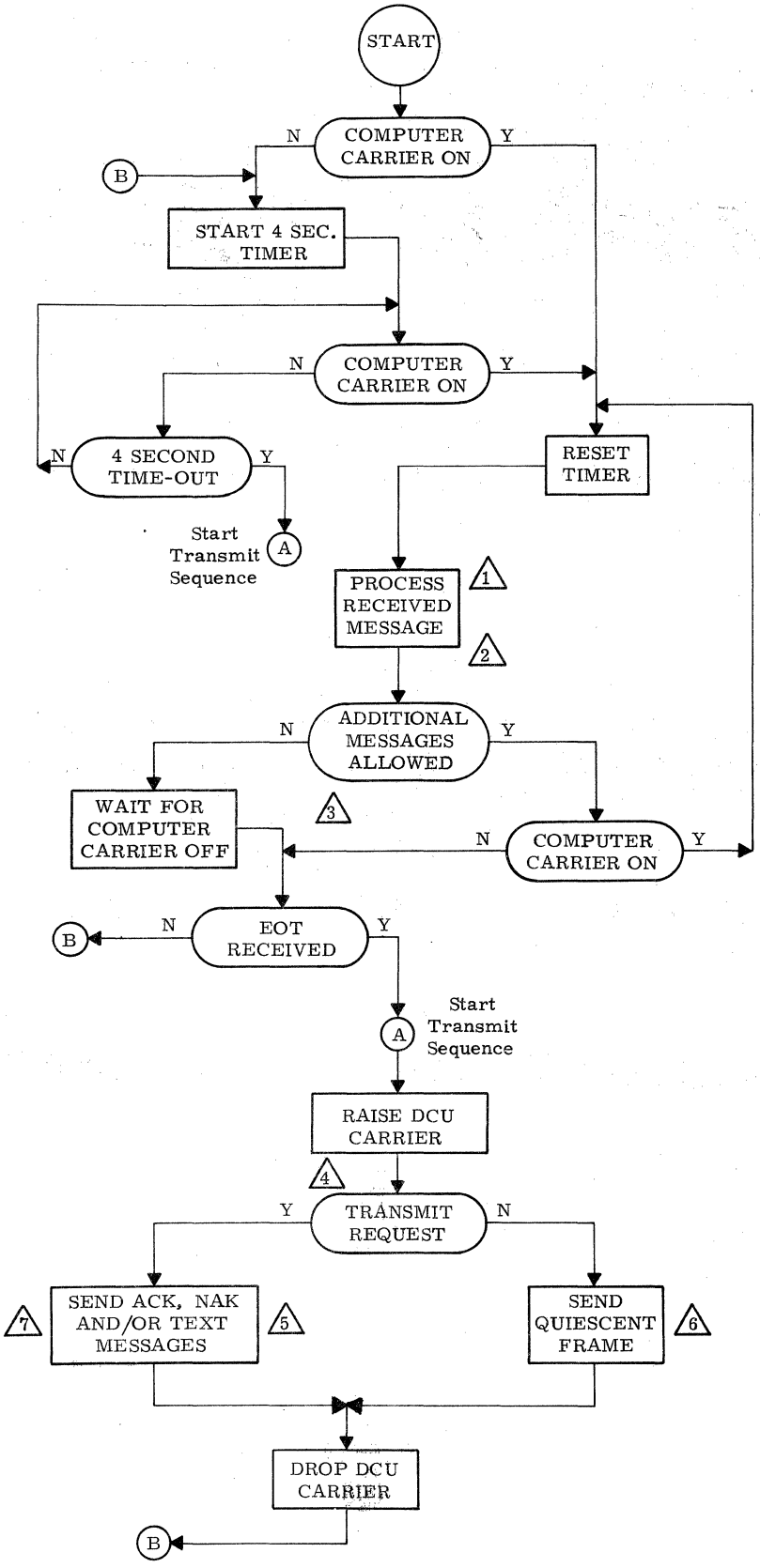
The 3010AH1401 Synchronous Drive Interface (14.1) is used as the computer's interface with the Display Controller Unit. Fig. 13.2-1 illustrates the DCU message sequences and Fig. 13.2-2 indicates the content of the computer/DCU messages.

The time required for the computer to fill a 1012 character display at the various baud rates (baud = bits per second) is approximately as follows:

4800 baud; 1.7 seconds

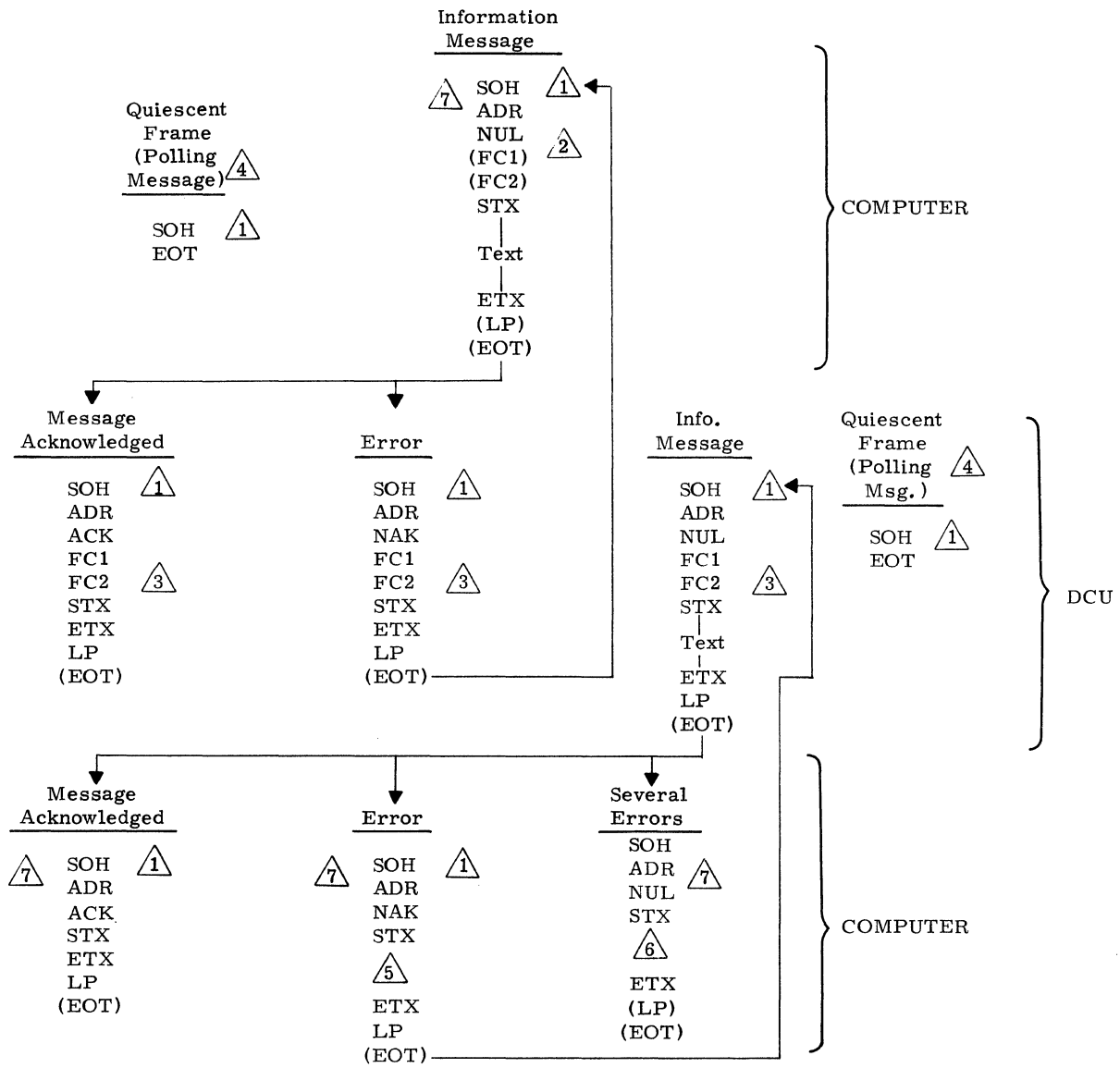
2400 baud; 3.4 seconds

2000 baud; 4.1 seconds



1. Lock keyboard at STX time.
2. Unlock keyboard at LP time. If not a NAK message, replace double entry marker with single.
3. One NAK message allowed, or one ACK and one text message for each TMU are allowed.
4. May be a keyboard request or a retransmission request due to a NAK message reception. Keyboard locked until transmission is complete. Entry marker is double until non-NAK message (ACK or NUL) is received.
5. Any ACK or NAK message for TMU-A is sent first, then any ACK or NAK for TMU-B, then one text message if any are waiting. TMU-A and TMU-B messages are sent in alternate frames, if both are waiting.
6. SOH followed by EOT
7. Terminal goes busy and computer messages are ignored from transmit request until transmission is complete.

Fig. 13.2-1 Display Controller Message Sequencing



1. When synchronous communication channels are in use, all SOH characters are preceded by at least four hardware generated SYN characters (026_8).

2. Function code characters may be included in computer messages if convenient, but are ignored by the DCU.

3. Function code characters will be "space" (SP, 040_8) from DCU-765, and from DCU-776, when messages without function codes are transmitted. FC1 and FC2 are "spaces" in virtually all ACK and NAK messages.

4. Quiescent Frames are optional from computer and are sent by DCU if no other message is to be sent in a transmission frame. In the absence of message exchanges, DCU sends quiescent frame each 4 seconds.

5. Move entry marker to start of message.

6. Graphic characters spell out error message to operator.

7. If valid SOH and ADR are not received by DCU, the entire message is ignored, and no ACK or NAK reply is sent.

Fig. 13.2-2 Computer/DCU Message Formats

REMOTE COMMUNICATIONS

In many applications, the GE-PAC 3010/2 system must communicate with remotely located terminals, such as distant computer systems, a distant process area, or a distant data terminal. The GE-PAC 3010/2 offers both serial data links suitable for communication via data sets (modems) and a high speed parallel data link.

The communications modules serve three application areas: (1) Communication via digital data sets over telephone lines or other communications media. (2) Communication with a nearby terminal, such as another GE-PAC computer or a Video Display Subsystem, via a direct cable connection. (3) Control and monitoring of a remotely located process area which implements GE-TAC* 7000 series Supervisory Control and Digital Telemetry equipment, via digital data sets. The three applications are served by the communications modules as follows:

Application	Communications Modules
(1)	Synchronous Drive Interface, Asynchronous Data Set Adapter
(2)	High Speed Data Link, Synchronous Drive Interface
(3)	GE-TAC Communications Coupler, Telemetry Communications Coupler

14.1 SYNCHRONOUS DRIVE INTERFACE

The 3010AH14 Synchronous Drive Interface (SDI) is a synchronous-character serial-bit communications interface, suitable for communications via data sets or via a directly connected cable up to 50 feet in length. This module consists of an input controller and output controller on the computer's Multiplexer Bus, providing a receiver and a transmitter. The SDI is suitable for communications via data sets such as the American Telephone and Telegraph Co. 201 series. The interface with the data sets or the opposite terminal complies with EIA Standard RS-232C. While this module utilizes two mother boards and two slots on the Multiplexer Bus, it has only one Multiplexer Bus interface and a single device address.

14.1.1 Speed

Characters are transmitted at any rate, up to 9600 baud (bits per second). When directly connected to a 4291 Display Controller (Section 11), the rate is 4800 baud, as determined by the Direct Timing Source in the Display Controller. When data sets are employed, the baud rate is determined by the data sets. The data set at the 3010 computer site and the data set at the remote site must operate at the same rate. Where data sets such as the American Telephone and Telegraph Co. 201A3 are in use, the rate will be 2000 baud. If American Telephone and Telegraph Co. 201B1 data sets or equivalent are used, the rate is 2400 baud.

*Registered Trademark of General Electric Company

14.1.2 Data Format

The standard SDI transmitted and received data consists of characters of 7 data bits plus a parity bit. The hardware generates the transmitted parity bit and checks the received parity bit. The program may specify odd or even parity bit when communicating with a Display Controller; odd parity bits are transmitted by the Display Controller and must be transmitted by the SDI.

Transmitted and received characters are exchanged between the Processor and the SDI in the form of 8-bit bytes. For transmitted characters, the most significant bit (bit 0) has no meaning and the hardware replaces it with the parity bit as it converts the parallel byte to serial form. The SDI assembles the 7 bits in each received character in to 8-bit parallel bytes in which the most significant bit is always equal to zero.

The SDI hardware provides no character recognition, other than received synchronization characters, and all message structuring and character recognition must be handled by the program.

14.1.3 Data Link Synchronization

The hardware at the two ends of the communications lines must be synchronized so that the bit-serial synchronous characters can be reassembled into meaningful data. Synchronization is accomplished by the transmission of at least two synchronization characters before the first information character in any message.

The standard SDI is synchronized after two ASCII synchronization characters (SYN, X'16', 026_8) with correct parity have been received. The computer program should transfer at least four such characters before transferring the first message character, to insure the greatest probability that the opposite terminal will be synchronized.

There can be no time interval between characters on a synchronous communications channel, because such an interval would cause a loss of synchronization. Should the program fail to transfer a subsequent character within a serial character transmission period, while the SDI remains in the Write mode, a NUL (all zeros) character is transmitted and the Overflow status bit sets (see Status Sensing under 14.1.4).

14.1.4 SDI Operating Sequences

The program controls and monitors the device interface via the Output Command instruction and Sense Status instructions. The data set Ring signal may be monitored by the program to implement automatic

answering. If a dial or switched telephone network is used, calls from the 3010 computer site are initiated manually. Eight-bit data bytes are transferred between the SDI and the Processor by Write Data and Read Data instructions.

Status Sensing; the meaning of the bits in status bytes returned to the Processor is as follows (Fig. 14.1-1) -

- Bit 0 = 1 = Overflow. OV is set if the Processor fails to transfer a received or transmitted data byte on a timely basis, such that data in the serial data stream is lost. If, while the SDI remains in the Write mode, the Processor fails to supply a new character within one character period (1664 usec @ 4800 baud), a NUL character is transmitted in the next character period, and OV sets at the beginning of that period. If, while the SDI is in the READ mode and not in the Sync Search mode, the Processor fails to read a character held by the SDI before it is replaced by the next received character, OV sets. The SDI interrupt queue flip-flop sets as OV sets.

- Bit 1 = 1 = Parity Failure. PF sets if the received lateral parity bit does not agree with the Parity Mode established by command bit 2. When communicating with a DCU, the parity bit should be odd. The SDI interrupt queue flip-flop sets as PF sets.

Command Byte
Status Byte
Bit

	0	1	2	3	4	5	6	7
Status Byte	OV	PF	SYNC	RING	BUSY	EX	COF	DU
Command Byte	DSBL	ENAB	PM	①	DTR	DSCN	WRT	READ

① Read Mode: SSCH
Write Mode: CTS

Fig. 14.1-1 Synchronous Data Link Command and Status Bytes

- Bit 2 = 1 = SYNC. When the SDI is in the Sync Search mode, status bit 2 sets as the first valid receive synchronization character is assembled, and remains set until a non-synchronization character is assembled. After the SDI is synchronized, SYNC is set by each valid sync character received in the message stream, and is reset as the SDI receives non-sync characters. The SDI interrupt queue flip-flop is set as SYNC sets.

- Bit 3 = 1 = RING. RING sets when the ring line from the attached data set or terminal goes true. Video Display Controllers do not use the ring line. The SDI interrupt queue flip-flop sets as RING sets.

- Bit 4 = 1 = BUSY. BUSY is set when the SDI is in the Write mode and Clear to Send from the device interface is not yet true, when the SDI is in the process of transferring a character to or from the device, and BUSY is set during a 150 ms Disconnect cycle. The SDI interrupt queue flip-flop is set as BUSY resets.

- Bit 5 = 1 = Examine. EX = OV + PF + RING

- Bit 6 = 1 = Received Carrier and Request to Send Off. COF is set if both the received carrier and the SDI's Request to Send signals at the device interface are off. This indicates that the interface is neither ready for transmission nor reception. A transition of this bit in either direction sets the SDI interrupt queue flip-flop.

- Bit 7 = 1 = Device Unavailable. DU is set if AC power is not connected to the attached device or if no device is connected to the SDI's device interface. This bit reflects the state of the Data Set Ready lead at the device interface. The SDI interrupt queue flip-flop sets as this bit sets.

Output Commands; the command byte bits have the following meaning (Fig. 14.1-1) -

- Bits 0 and 1 = interrupt disable and enable, respectively. When interrupts are disabled, the interrupt queue flip-flop may still store an interrupt.

- Bit 2 = 1 = Odd Parity Mode. If bit 2 of the command byte is set, the generation of an odd lateral parity bit for each transmitter character, and the checking of an odd lateral parity bit on each received character is specified. If command byte bit 2 is reset, even lateral parity checking and generation is specified. Odd parity must be specified when the SDI communicates with Display Controllers directly or through data sets.

- Bit 3 = 1 = Sync Search or Clear to Send modes. If bit 3 of the command byte is set when the SDI is in the READ mode, or if the same command byte specifies READ mode, the SDI is placed in a sync search mode, so that it will not be able to transfer characters to the Processor until it has received two valid synchronization characters with correct parity. If bit 3 of the command byte is reset in READ mode, the Output Command initiates character timing and characters are assembled from that time for transfer to the Processor. If bit 3 of the command byte is set when the SDI is in the Write mode, or if the same command byte specifies Write mode, character transmissions are enabled when the Clear to Send signal from the de-

vice interface is on. If bit 3 is not set in the Write mode, the transmitted data line is held in the mark state, the BUSY status bit is reset as soon as the Clear to Send signal is received, and even if the Processor does not supply a character within a character period, the OV status bit cannot set. This latter condition is referred to as the REST mode, and is used to hold the interface in a non-data transfer state while the program is busy and unable to service SDI interrupts.

- Bit 4 = 1 = Data Terminal Ready. DTR turns on the Data Terminal Ready signal at the device interface. This signal informs the attached device that the SDI is ready to receive or transmit data. If the SDI is connected to a data set on a switched (dial) line, this signal must be on to permit the data set to go to the Data mode. If the data set implements an Automatic Answer feature, this signal must be on to allow calls to be answered, the data set to go to the Data mode, and to remain in the Auto mode.

- Bit 5 = 1 = Disconnect. If the Data Terminal Ready signal at the device interface is on, DSCN causes it to go off for approximately 150 milliseconds, during which time the BUSY status bit is set. This command is used to cause a data set connected to a switched line to disconnect (hang-up). Since the Data Terminal Ready signal returns to "on" after the disconnect, automatic answering can be implemented. This feature is not used when the SDI is directly connected to a Display Controller or a data set using leased non-switching lines. The SDI interrupt queue flip-flop is set at the end of the disconnect period.

- Bit 6 = 1 = Write Mode. In the Write mode, data bytes may be transferred from the Processor to the SDI for transmission through a data set or to a Display Controller.

- Bit 7 = 1 = READ. In the READ mode, the SDI may accumulate serial data characters from the attached device for transfer to the Processor. The change from READ mode is delayed if the SDI is in the process of transmitting a character.

SDI Device Address:

The address for the first SDI implemented in a system is normally assigned as X'72'. The second through fourth SDI's are typically assigned X'82', X'92', and X'A2', respectively. A single SDI connected to a dial type data set is typically assigned address X'0E'.

14.2 HIGH SPEED DATA LINK

The primary application of the 3010AE86 High Speed Data Link is communication with another GE-PAC computer via a directly connected cable up to 2000 feet in length. In this application, a 3010AE8601 High Speed Data Link Transmitter, and a 3010AE8602 High Speed Data Link Receiver are implemented on the computer's Multiplexer Bus. As secondary functions, the High Speed Data Link Transmitter, only, may be implemented to communicate with a 4320A Console Drive Module or an Output Peripheral Device, such as a 4262C Line Printer, a 4253 Paper Tape Punch, or a 4283C Card Punch.

The interface with the opposite computer or the attached device consists of AC coupled line drivers and receivers which send and receive control signals and transfer data in the form of bytes consisting of eight parallel bits plus a program-option parity bit. 35,000 or more bytes per second may be transferred (3010/2 to 3010/2).

In the primary application, the High Speed Data Link (HSL) may communicate with another 3010 computer system implementing another 3010AE86 HSL or it may communicate with a 4000 series GE-PAC computer system implementing a 4202X090/190, 4820BS12, or 4821AS12 Computer Communications Link. The transmitter and receiver are functionally independent of each other, separately addressable, and the data transfers may be full-duplex with information in transit in both directions at the same time, if the program permits.

14.2.1 Data Format

The data transferred is in the form of one or more 8-bit bytes in each record, and one or more records in each file. The program in the transmitting computer indicates the length of the next record by transferring a byte count byte to the transmitter after issuing an Output Command with bit 6 and/or bit 7 of the command byte set. If command byte bit 6 is reset and bit 7 is set, the program has specified that the next record is the final record in a file. When communicating with another GE-PAC 3010 computer, a record may contain up to 256 bytes. Records transmitted to GE-PAC 4000 series computers are generally limited by the TIM tables to 189 bytes. The byte count byte must be equal to the byte count minus one. For example, a byte count of X'04' specifies a 5-byte record. A byte count of X'FF' specifies a record of X'100' or 256_{10} bytes.

Each transmitted byte is accompanied by control line pulses which indicate to the receiver that the byte is a byte within a record, the final byte within a record, or the final byte in a file. The program in the receiving computer may determine the byte/record/file status by examining status bytes returned to the Processor from the receiver. Subsequent byte transmissions cannot proceed until the preceding byte has

been acknowledged by the receiver. The byte transmissions are asynchronous, the program may transfer a byte for transmission at any time after the BUSY status bit resets.

14.2.2 HSL Operating Sequences

The program controls and monitors the data link via Output Command and Sense Status instructions. The byte count byte and data bytes are transferred to the transmitter by Write Data instructions. Received data bytes are transferred to the Processor by Read Data instructions.

Transmitter Status:

When used in a high speed computer to computer data link, the meaning of the bits in status bytes returned from the transmitter to the Processor is as follows (Fig. 14.2-1). (Definition of the transmitter status bits when it is connected to a Console Drive Module or a peripheral device is provided in the High Speed Data Link Transmitter theory, publication no. 3010AE86T-T.)

- Bit 0 = 1 = Flag 1. FL1 is set when the opposite computer returns a Flag 1 response to a byte transmission. Normally, a Flag 1 or Flag 2 response is made only to the final byte in a record. The program in the opposite computer specifies a normal response, a Flag 1 response, or a Flag 2 response by issuing appropriate Output Commands to the High Speed Data Link Receiver. The meaning of the flag responses is defined by the software.

- Bit 1 = 1 = Flag 2. FL2 is set when the program in the opposite computer specifies a Flag 2 response to a byte transmission. The meaning is defined by the software.

- Bit 4 = 1 = BUSY. BUSY is set when the transmitter is not ready to accept a byte count byte nor a data byte from the Processor. The transmitter interrupt queue flip-flop sets as BUSY goes false. It also sets when an Output Command specifies that the transmission of a new record is to begin.

- Bit 5 = 1 = Examine. EX = (FL1 + FL2) · $\overline{\text{BUSY}}$

- Bit 6 = 1 = End of Medium. EOM is set as the final byte in a record is transmitted.

- Bit 7 = 1 = Stall Out. STO is set if the opposite computer does not acknowledge a byte transmission within approximately 700 milliseconds.

Transmitter:

Command Byte
Status Byte
Bit

0	1	2	3	4	5	6	7
FL1	FL2	0	0	BUSY	EX	EOM	STO
INTERRUPT CONTROL		CLR			$\overline{\text{PTY}}$	RECORD CONTROL	

Receiver:

0	1	2	3	4	5	6	7
PTE	EOF	DMD	0	BUSY	EX	EOM	0
INTERRUPT CONTROL		CLR	FL	FL	$\overline{\text{PTY}}$	RECORD CONTROL	

Command Byte
Status Byte
Bit

Fig. 14.2-1 High Speed Data Link Command and Status Bytes

Transmitter Output Commands:

The meaning of the bits in a command byte transferred to the transmitter is as follows (Fig. 14.2-1);

- Bits 0 and 1 are interrupt control bits -

  $\overline{0}\cdot\overline{1}$ = no change.

  $\overline{0}\cdot 1$ = enable interrupts.

  $0\cdot\overline{1}$ = disable interrupts but allow the queue flip-flop to store and interrupt.

  $0\cdot 1$ = disarm interrupts, reset the queue flip-flop.

- Bit 2 = 1 = Clear. CLR initializes the transmitter, resetting all status bits.

- Bit 5 = 1 = Disable Parity Bit. $\overline{\text{PTY}}$ disables the transmission of an even parity bit which otherwise accompanies each 8-bit transmitted data byte. This bit has no effect unless bit 6 and/or bit 7 is set.

- Bits 6 and 7 are record control bits -

  $\overline{6}\cdot\overline{7}$ = no change.

  $\overline{6}\cdot 7$ = the next record transmitted will be the final record in a file.

  $6\cdot\overline{7}$ = the next record transmitted will be an intermediate record within a file.

  $6\cdot 7$ = the next record transmitted will be an intermediate record within a file.

Receiver Status:

The meaning of the bits in status byte returned to the Processor from the receiver is as follows (Fig. 14.2-1);

- Bit 0 = 1 = Parity Error. PTE sets if the receiver hardware detects incorrect parity on a received data byte.
- Bit 1 = 1 = End of File. EOF is set as the final byte in a file is received.
- Bit 2 = 1 = Demand. DMD is set as the first byte in a record is received. DMD sets only if BUSY is reset because the program has not yet issued an Intermediate Record Response or Last Record Response Output Command to the receiver. The reception of the first byte sets the interrupt queue flip-flop if it is not disarmed.
- Bit 4 = 1 = BUSY. BUSY is set while the receiver is awaiting the arrival of the next byte from the transmitter. If not disarmed, the interrupt queue flip-flop sets as busy resets.
- Bit 5 = 1 = Examine. EX = DMD except after the receipt of the final byte in a record. After the receipt of the final byte in a record, EX = PEF. PEF is set if a parity error was detected on any byte in the record or if EOF is set.
- Bit 6 = 1 = End of Medium. EOM is set as the final byte in a record is received. When the Processor accepts the final byte, the interrupt queue flip-flop is set if not disarmed, to request an Output Command specifying a normal or flag response be sent to the transmitter, in response to the last byte.

Receiver Output Commands:

The meaning of the bits in a command byte transferred to the receiver are as follows (Fig. 14.2-1);

- Bits 0 and 1 are interrupt control bits -

  $\overline{0} \cdot \overline{1}$ = no change.

  $\overline{0} \cdot 1$ = enable interrupts.

  $0 \cdot \overline{1}$ = disable interrupts but allow the queue flip-flop to store an interrupt.

  $0 \cdot 1$ = disarm interrupts, reset the queue flip-flop.

- Bit 2 = 1 = Clear. CLR initializes the receiver, resetting all status bits.
- Bit 5 = 1 = Disable Parity Check. $\overline{\text{PTY}}$ disables parity checking. Since the transmitter in a GE-PAC 4000 series computer does not send a parity bit with each byte, parity checking should be disabled when the opposite computer is a 4000 series system. This bit has no effect unless bit 6 and/or bit 7 is set.
- Bits 6 and 7 are recond control bits -

  $\overline{6} \cdot \overline{7}$ = no change.

  $\overline{6} \cdot 7$ = final record in a file response.

  $6 \cdot \overline{7}$ = intermediate record response.

  $6 \cdot 7$ = intermediate record response.

- Bits 3 and 4 are flag response bits used to specify flag responses to the final record in a file. The meaning of the two flag responses is defined by software. No response is made unless bit 6 and/or 7 is also set.

  Bit 3 = 1 = Flag 1 response.

  Bit 4 = 1 = Flag 2 response.

Device Addresses:

The first High Speed Data Link in a system is normally assigned X'CE' for the transmitter and X'CF' for the receiver. The normal addresses for a second HSL are X'DE' (transmitter) and X'DF' (receiver). The addresses are selected by eight screwdriver actuated switches on each module.

14.3 GE-TAC COMMUNICATIONS COUPLER

The 3010AH6101 GE-TAC Communications Coupler is a single module on the computer's Multiplexer Bus which includes both a transmitter and a receiver. It is intended to transmit commands to, and receive data from, GE-TAC 7000 series Supervisory Control and Digital Telemetry stations, via digital data sets and telephone lines. The following data sets or their equivalents may be used: American Telephone and Telegraph Co. 103F, 202C, 202D, 201C, 201D; GE TDM-110, and GE TDM-210. The data set interface complies with EIA Standard RS-232C. Several optional features available through hardware selection or implemented by software are chosen for compatibility with the GE-TAC equipment served.

This coupler may be used with two-wire single channel data sets which require line turn-around time to change the direction of transmission, or with four-wire dual channel data sets, in which case, line turn-around time is eliminated. A screwdriver actuated switch on the module selects the appropriate data set interface configuration.

14.3.1 Data Format

Data word transmissions and receptions over the communications channel are in the form of 16-bit or 32-bit words, in bit-serial, word-asynchronous form. The most significant bits are transmitted and received first. The first bit in each transmitted and received word is a zero (space) start bit. The next bit specifies the length of the word. If the second bit is a one (mark), the current word is 32 bits in length. If the second bit is a zero (space) the current word is 16 bits in length. All data exchanges between the Processor and the coupler are in the form of 8-bit bytes. A 16-bit word therefore, requires 2-byte exchanges and a 32-bit word requires 4-byte exchanges. The final five bits in the last byte in each word are reserved as a polynomial check segment. If the check segment in the received data word agrees with the data received, the least significant five bits in the final byte are set to zero. If the received check segment does not agree, one or more of the final five bits transferred to the Processor are ones. The final five bits in the last byte to be transmitted must be set to zero by the program to allow the coupler hardware to generate a polynomial check segment for transmission.

14.3.2 Speed

The transmission and reception baud rate is selected as required by the data sets and telephone lines in use for the communications channel. The rate is selected with four screwdriver actuated switches on the coupler module for one of the following rates: 150, 300, 600, 900, 1200, 1800, 2400, or 4800 bits per second.

14.3.3 Operating Sequence

The program controls and monitors the data set interface via Sense Status instructions and Output Command instructions. Eight-bit data bytes are transferred between the coupler and the Processor by Write Data and Read Data instructions. If enabled, the coupler interrupts the Processor when it is ready to accept a byte for transmission or is holding an accumulated received byte.

Output Commands: The program controls the operating status of the coupler by executing Output Command instructions to the coupler. The command bits have the following meaning (Fig. 14.3-1);

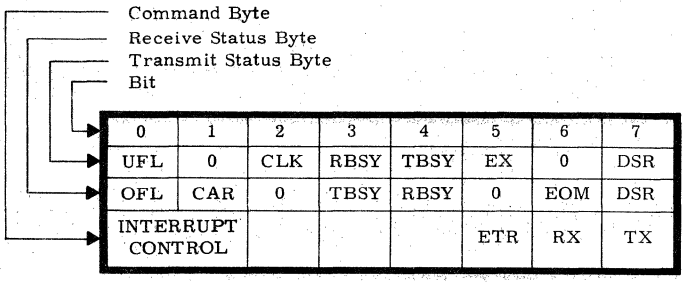
- Bits 0 and 1 are interrupt control bits -

  $\overline{0}\cdot\overline{1}$ = no change.

  $\overline{0}\cdot 1$ = enable interrupts.

  $0\cdot\overline{1}$ = disable interrupts, but allow the queue flip-flop to store an interrupt.

  $0\cdot 1$ = disarm interrupts and reset queue flip-flop.



0	1	2	3	4	5	6	7
UFL	0	CLK	RBSY	TBSY	EX	0	DSR
OFL	CAR	0	TBSY	RBSY	0	EOM	DSR
INTERRUPT CONTROL					ETR	RX	TX

Fig. 14.3-1 GE-TAC Communications Coupler Command and Status Bytes

- Bits 5, 6, and 7 are mode control bits. Bit 5 has no effect unless bit 6 or 7 is set. If bit 5 is set while the controller is being placed in the receive or transmit modes, the coupler is allowed to begin transmission or reception immediately. Otherwise, the coupler waits several milliseconds before changing from TX to RX or RX to TX, to allow the communication lines to settle following a line turn-around.

  $\overline{6}\cdot\overline{7}$ = no change.

  $\overline{6}\cdot 7$ = transmit mode.

  $6\cdot\overline{7}$ = receive mode.

  $(6+7)\cdot 5$ = enable immediate change from TX to RX or RX to TX.

  $6\cdot 7$ = disconnect (idle mode and drop data terminal ready signal to data set).

Status: Two status bytes are defined for the GE-TAC Communications Coupler because the information returned to the Processor differs when the coupler is in the transmit mode from that of the receive or idle modes. The status bits have the following meaning (Fig. 14.3-1);

- Receive Status -

  Bit 0 = 1 = Overflow. OFL sets if the Processor fails to accept a data byte before it is altered by the reception of the next byte.

  Bit 1 = 1 = Carrier. CAR is reset when the data set has detected the carrier from the distant data set. The carrier must be on during data reception. CAR is set when the received carrier is off. Normally, CAR set indicates that the coupler should be changed to TX mode.

  Bit 3 = Transmitter Busy. TBSY is normally reset in the receive mode. If it is set, it is because the transmitter is still serializing data after the coupler has been changed to receive mode.

Bit 4 = 1 = Receiver Busy. RBSY is reset when the receiver is ready to transfer a data byte to the Processor. The coupler interrupt occurs, if enabled, when RBSY resets.

Bit 6 = 1 = End of Message. EOM sets when an END pattern is recognized in an incoming 16-bit word, indicating the end of a message.

Bit 7 = 1 = Data Set Ready. DSR is set when the data set ready signal from the data set is true.

- Transmit Status -

Bit 0 = 1 = Underflow. UFL sets if the Processor fails to provide a new data byte before the next byte transmission period begins.

Bit 2 = 1 = Clock Set. CLK is derived from the coupler timing circuits and is set for half a bit period and reset for half a bit period. CLK, therefore, runs at the baud rate.

Bit 3 = 1 = Receiver Busy. RBSY is normally reset in transmit mode. If it is set, it is because the receiver is still in the process of accumulating an incoming byte after being changed to transmit mode.

Bit 4 = 1 = Transmitter Busy. TBSY is reset when the transmitter is ready to accept a byte from the Processor for transmission. The coupler interrupt sets when busy resets.

Bit 5 = 1 = Examine. EX = UFL.

Bit 7 = 1 = Data Set Ready. DSR is set when the data set ready signal from the data set is true.

Device Address:

The standard device addresses for GE-TAC Communications Couplers are X'8E' for the first, then X'8F', X'9E', and X'9F' for fourth coupler. The addresses may be changed with screwdriver actuated switches on the printed circuit board.

14.4 TELEMETRY COMMUNICATIONS COUPLER

The 3010AH6201 Telemetry Communications Coupler is a single module on the computer's Multiplexer Bus which includes both a transmitter and a receiver. It is intended to exchange information with GE-TAC telemetry stations which transmit and receive 23-bit words with no polynominal check segment, via digital data sets and telephone lines. The following data sets or their equivalents may be used: GE TDM-210, GE TDM-110, American Telephone and Telegraph Co. models 103F, 202C, 202D, 201A, and 201B. The data set interface complies with EIA Standard RS-232C.

This coupler may be used with two-wire single channel data sets which require line turn-around time to change the direction of transmission, or with four-wire dual channel data sets, in which case, line turn-around time is eliminated. A screwdriver actuated switch on the module selects the appropriate data set interface configuration.

14.4.1 Data Format

Data word transmissions and receptions over the communications channel are in the form of 23-bit fixed length words, in bit-serial, word-asynchronous form. The most significant bits are transmitted and received first. The first bit in each transmitted word is a zero (space) start bit, which is transferred in the most significant bit position in the first byte transferred to or from the Processor. The final two bits in each word (bits 22 and 23) are one (mark) stop bits, which are transferred in the lowest two bit positions in the final byte transferred to or from the Processor. The final bit in the final byte in each word exchange between the coupler and Processor is a fill bit equal to one, which also appears on the communications line as an extra mark or stop bit between words. The total of 24 bits exchanged between the Processor and coupler are transferred in the form of three 8-bit bytes. All binary data between the start bit and the stop bits is information to or from the GE-TAC equipment.

14.4.2 Speed

The transmission and reception baud rate is selected as required by the data sets and telephone lines in use. The rate is selected by four screwdriver actuated switches on the coupler module for one of the following rates: 150, 300, 600, 900, 1200, 1800, or 4800 bits per second.

14.4.3 Operating Sequences

The program controls and monitors the coupler via Sense Status instructions and Output Command instructions. Eight-bit data bytes are transferred between the Processor and the coupler by Write Data and Read Data instructions. If enabled, the coupler interrupts the processor when it is ready to accept a byte for transmission or is holding an accumulated received data byte.

Output Commands: The program controls the operating status of the coupler by executing Output Command instructions to the coupler. The command bits have the following meaning (Fig. 14.4-1);

- Bits 0 and 1 are interrupt control bits -

$\overline{0} \cdot \overline{1}$ = no change.

$\overline{0}\cdot 1$ = enable interrupts.

$0\cdot\overline{1}$ = disable interrupts, but allow the queue flip-flop to store an interrupt.

$0\cdot 1$ = disarm interrupts and reset queue flip-flop.

- Bits 6 and 7 are mode control bits. Bit 5 has no effect unless bit 6 or 7 is set. If bit 5 is set while the controller is being placed in the receive or transmit modes, the coupler is allowed to begin transmission or reception immediately. Otherwise, the coupler waits several milliseconds before changing from TX to RX or RX to TX, to allow the communication lines to settle following a line turn-around.

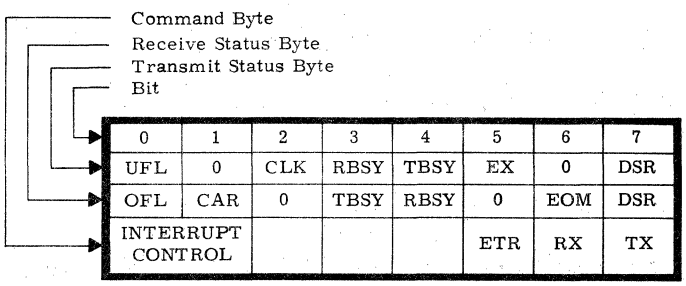
$\overline{6}\cdot\overline{7}$ = no change.

$\overline{6}\cdot 7$ = transmit mode.

$6\cdot\overline{7}$ = receive mode.

$(6+7)\cdot 5$ = enable immediate change from TX to RX or RX to TX.

$6\cdot 7$ = disconnect (idle mode and drop data terminal ready signal to data set).



0	1	2	3	4	5	6	7
UFL	0	CLK	RBSY	TBSY	EX	0	DSR
OFL	CAR	0	TBSY	RBSY	0	EOM	DSR
INTERRUPT CONTROL					ETR	RX	TX

Fig. 14.4-1 GE-TAC Communications Coupler Command and Status Bytes

Status: Two status bytes are defined for the GE-TAC Communications Coupler because the information returned to the Processor differs when the coupler is in the transmit mode from that of the receive or idle modes. The status bits have the following meaning (Fig. 14.4-1);

- Receive Status -

  Bit 0 = 1 = Overflow. OFL sets if the Processor fails to accept a data byte before it is altered by the reception of the next byte.

  Bit 1 = 1 = Carrier. CAR is reset when the data set has detected the carrier from the distant data set. The carrier must be on during data reception. CAR is set when the received carrier is off. Normally, CAR set indicates that the coupler should be changed to TX mode.

  Bit 3 = Transmitter Busy. TBSY is normally reset in the receive mode. If it is set, it is because the transmitter is still serializing data after the coupler has been changed to receive mode.

  Bit 4 = 1 = Receiver Busy. RBSY is reset when the receiver is ready to transfer a data byte to the Processor. The coupler interrupt occurs, if enabled, when RBSY resets.

  Bit 6 = 1 = End of Message. EOM sets as the third byte in each word is transferred to the Processor.

  Bit 7 = 1 = Data Set Ready. DSR is set when the data set ready signal from the data set is true.

- Transmit Status -

  Bit 0 = 1 = Underflow. UFL sets if the Processor fails to provide a new data byte before the next byte transmission period begins.

  Bit 2 = 1 = Clock Set. CLK is derived from the coupler timing circuits and is set for half a bit period and reset for half a bit period. CLK, therefore, runs at the baud rate.

Device Address:

The standard device address for the Telemetry Communications Coupler is X'BE' for the first and X'BF' for the second. The addresses may be changed with screwdriver actuated switches on the printed circuit board.

14.5 ASYNCHRONOUS DATA SET ADAPTERS

Two Asynchronous Data Set Adapters are available to provide interfaces with bit-serial asynchronous character data sets. Model 3000AH2101, 103 Data Set Adapter, operates at up to 300 baud, and Model 3000AH2201, 202 Data Set Adapter, operates at up to 1800 baud. Each adapter has an EIA Standard RS-232 data set interface.

Each of the Asynchronous Data Set Adapters requires two adjacent slots on the Multiplexer Bus. Each adapter provides half-duplex communication. It is possible to implement two identical adapters to provide full-duplex communication. The optional Parity Adders are installed on the basic modules.

14.5.1 Data Format

Each of the Asynchronous Data Set Adapters transfers bit-serial characters 6, 7, or 8 bits in length. Each character begins with a zero (space) start bit and ends with at least one (mark) stop bit. The least significant bits are transferred first on the serial data line. All data exchanges between the adapter and the Processor are in the form of 8-bit bytes. Where fewer than 8 bits per character are transferred, zeros are exchanged between the Processor and the adapter in the unused (most significant) bit positions. The start and stop bits are not included in the data exchanges with the Processor. The character length is selected by jumper wiring on the adapter.

14.5.2 Speed

The 103 Data Set Adapter operates at 110, 150, or 300 bits per second, as selected by jumper wiring on the module. The 202 Data Set Adapter operates at 1200 or 1800 bits per second, as selected by jumper wiring on the module.

14.5.3 Parity Option

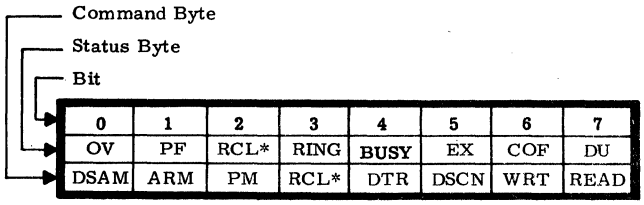
The Asynchronous Data Set Adapters may implement an optional Parity Adder which provides for hardware generated and checked parity bits in the most significant bit position of each received character. The parity option is not available if the 8-bit character format is implemented. The Parity Adder for the 103 Data Set Adapter is Model No. 3000AH2103. For the 202 Data Set Adapter, the Parity Adder is Model No. 3000AH2203.

14.5.4 Operating Sequence

The program controls and monitors the data set interface through Output Commands issued to the adapters and through status byte transfers to the Processor. Read Data and Write Data instructions are used to exchange data bytes between the Processor and the adapters. The data set Ring signal may be monitored by the program to implement automatic answering. If enabled, the adapters generate interrupts upon a change in any of several of the status byte bits, including the resetting of the BUSY bits, which requests transfer of the next data byte.

Status Sensing: The meaning of the bits in status bytes returned from either Asynchronous Data Set Adapter is as follows (Fig. 14.5-1);

- Bit 0 = 1 = Overflow. OV sets if the Processor does not transfer a byte before it is overwritten by the receipt of a new byte from the data set, or if the Processor fails to supply a new byte for transmission by the time the serialization of the previous character is complete. The interrupt queue flip-flop is set, if armed, when OV sets.



* 202 Data Set Adapter, only.

Fig. 14.5-1 Asynchronous Data Set Adapter Command and Status Bytes

- Bit 1 = 1 = Parity Failure. PF sets if the received parity bit does not compare with the parity mode established by bit 2 of the last command byte to the adapter.

- Bit 2 = 1 = Reverse Channel Line. RCL is set when the reverse channel lead from the data set is true. This bit is set by the 202 Data Set Adapter, only. A transition of RCL in either direction sets the interrupt queue flip-flop, if armed.

- Bit 3 = 1 = RING. RING sets when the ring line from the data set is true. If armed, the interrupt queue flip-flop sets when this bit sets.

- Bit 4 = 1 = BUSY. BUSY is set when the adapter is not ready to exchange a character with the Processor. The interrupt queue flip-flop sets, if armed, when this bit resets.

- Bit 5 = Examine. EX = OV + PF + RING.

- Bit 6 = Carrier Off. COF is set when the received carrier at the data set is off and the adapter is in the READ mode. The setting of this bit normally indicates that the adapter should be changed from READ to Write mode. A transition of this bit in either direction sets the interrupt queue flip-flop, if it is armed.

- Bit 7 = 1 = Device Unavailable. DU is set if AC power is not applied to the data set, or if the data set is not connected to the adapter. This bit reflects the state of the data set ready lead at the data set interface. If armed, the adapter interrupt queue flip-flop sets as this bit sets.

Output Commands: The command byte bits have the following meaning (Fig. 14.5-1);

- Bits 0 and 1 = interrupt disarm and arm, respectively. When disarmed, the interrupt queue flip-flop is held reset.

- Bit 2 = 1 = Parity Mode. PM if set, specifies the generation and checking of odd parity, or if reset specifies the generation and checking of even parity. This bit has meaning only if the Parity Adder is implemented. Typically, asynchronous communication channels use even parity.

- Bit 3 = 1 = Reverse Channel Line. RCL sets the reverse channel line at the data set interface "true". This bit has meaning for the 202 Data Set Adapter, only. RCL is typically set near the end of the reading of a message from the data set to offset the effects of echo suppression networks used in standard telephone links.

- Bit 4 = 1 = Data Terminal Ready. DTR sets the data terminal ready line at the data set interface "true". This line must be true to allow the data set to transfer data, if the data set is connected to a switched (dial) telephone network. This line must also be true to allow calls to be automatically answered with data sets incorporating an Automatic Answer feature.

- Bit 5 = 1 = Disconnect. If the data terminal ready line at the data set interface is true, DSCN causes it to go false for approximately 150 milliseconds, during which time BUSY status bit is set. This command is used to cause a data set connected to a switched network to disconnect (hang-up). Since the data terminal ready signal returns true after the disconnect, automatic answering can be implemented. This feature is not used when the adapter is connected to a data set using private or leased (non-switched) lines. The adapter interrupt queue flip-flop sets, if armed, at the end of the disconnect period.

- Bit 6 = 1 = Write Mode. In the WRT mode, data may be transferred from the Processor to the adapter for transmission through the data set. If this command causes a switch from READ mode, the change is delayed and the BUSY status bit is set for 80 to 120 milliseconds, to allow the lines to settle after the turn-around. When the turn-around is complete and the adapter ready for the first data byte, the interrupt queue flip-flop is set, if armed.

- Bit 7 = 1 = READ Mode. In the READ Mode, the adapter may accumulate bit-serial data characters from the data set for transfer to the Processor. The change to READ is delayed if the adapter is in the process of transmitting a character.

Device Address:

The standard address for the first 103 or 202 Data Set Adapter is X'5E' and for the second is X'5F'. The address may be changed by jumper wiring on the module.

APPENDIX A

ANALOG I/O SUBSYSTEM - DEFINITION OF TERMS

The following statements define the terms used in describing the Analog I/O Subsystem performance in Section 12 of this manual.

1. System Performance

The term system performance contained herein pertains only to the analog signal relationships as described below:

a. Analog Inputs

The performance described specifies the analog relationship from the multiplexer inputs terminals (S +, S -) to the A/D Converter output. The digital code for the A/D Converter is true binary for positive voltages at the multiplexer input and 2's compliment for negative voltages when referenced at the A/D Converter output.

b. Variable Outputs

The performance described specifies the relationships from the digital code at the input of the D/A Converter to the Analog output located at the VOC output multiplexer terminals.

c. Absolute Analog Outputs

The performance described specifies the relationship from the digital code input of the AAO generator to the generator output terminals.

2. Scan Rate

Scan Rate is defined as the maximum random scan rate the system is capable of, in points per second. Some degradation in performance may occur if a single point is scanned more than once per second.

3. Repetitive Scan Rate

Repetitive Scan Rate is defined as the maximum rate any one point may be scanned.

4. Full Range

Full Range is defined as the algebraic difference between the minimum and maximum values to which the Analog Input/Output Subsystem is specified.

Example

Specification	Full Range
$\pm$10 mv	20 millivolts
-10 mv to +50 mv	60 millivolts

5. Gain Error

Gain Error is defined as the deviation of the mean of a normal or Gaussian distribution from the actual value. Gain Error is specified in % FR and as a error which is gain dependent. When measuring Gain Error, proper offset techniques must be applied. Gain Error is specified at 25^{o} C $\pm$ 3^{o} C and the proper Gain Error coefficient must be taken into account as the temperature deviates from this range. When measuring Gain Error using Hg relay multiplexers for Analog Inputs, the maximum repetitive scan rate is one point/second.

6. Repeatability Error

The graph of Fig. A. 1 describes a Gaussian distribution of count values about the mean count value $\overline{X}$. $\overline{X}$ is calculated by taking N samples and then averaging them. Repeatability Error is expressed as a plus and minus three sigma deviation from the mean, $\overline{X}$. Three σ means that for a normal distribution 99.7% of all readings are within this $\pm 3\sigma$ range. In terms of evaluation of the analog subsystems, $\pm 3\sigma$ specifies that 0.3% of N readings may be disregarded. The readings to be disregarded are the readings furthest from the mean. Repeatability Error is expressed as a percentage of full range.

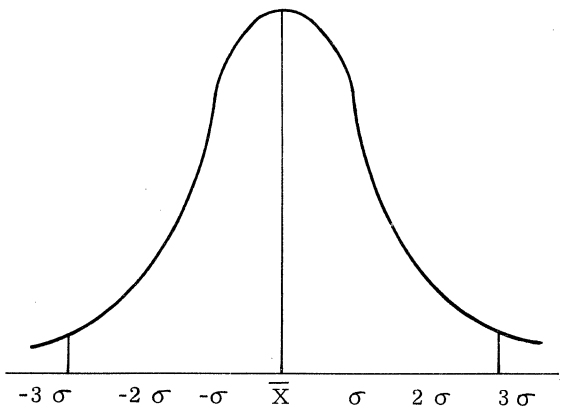


Fig. A. 1 Frequency Distribution of Count Values - Gaussian Curve

7. Common Mode Voltage

The voltage at both the S+ and S- terminals can be raised above and below the system logic ground. Common Mode Voltage is defined as the voltage with respect to system logic ground that these inputs may be raised while the system still processes the differential input signal. The Maximum Common Mode Voltage is the sum of the Common Mode Voltage plus the signal voltage when referenced in this specification.

8. Common Mode Rejection

The Common Mode Rejection of the Analog Input Subsystem is defined as the ability of the system to reject a signal that is common to both differential inputs (S+, S-) with a source unbalance of 100 ohms or less. Proper signal conditioning must be used when making this measurement (60 db filters). The CMR is specified from DC to 60 Hz AC and in db.

9. Crosstalk

Crosstalk effects are defined as the errors created by signal or common mode voltages from one point into or affecting the point being measured. Crosstalk is specified in terms of the ability of the system to reject these signals from the point being measured from DC to 60 Hz.

10. Offset

Offset is defined as the magnitude of the output when the input is zero. When measuring Gain Error, Repeatability Error, CMRR, and Crosstalk, proper offset techniques must be applied.

11. RTI (Referred to the Amplifiers Inputs)

An error that has a RTI Contribution is gain dependent.

An example is:

GE = $\pm$0.025%FR $\pm$10 μv RTI

To convert the 10 μv RTI affect in terms of FR, refer to the table below:

System Gain	FR	%FR	Total GE (%FR)
1000	20 mv	.05	.075
500	40 mv	.025	.05
250	80 mv	.0125	.0375

Where:

$$\% \text{ FR} = \frac{10\ \mu v}{\text{FR}} \times 100$$

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SECTION 4

GE-PAC 3010 CENTRAL PROCESSOR

(GE-PAC 30-2E)

This section describes the Central Processor provided with GE-PAC 3010 process computer systems. It may be used as a replacement for Section 4 in editions of the 3010/2 General Description, GET-6227.

The Central Processor is the computational and control center for the computer system. The GE-PAC 3010 Central Processor is a complete mini-computer system, including a Processor, Core Memory, a Multiplexor Channel and Bus, and an optional Selector Channel and Bus. The Central Processor is located in the Central System Cabinet (CSC).

Refer to Fig. 4.1. The Multiplexor Channel and Bus provide the input/output interface with the peripheral devices and the Process I/O Subsystem. The Selector Channel and Bus provide the interface to the optional Drum Memory, and automatically control direct transfers between the core and drum memories.

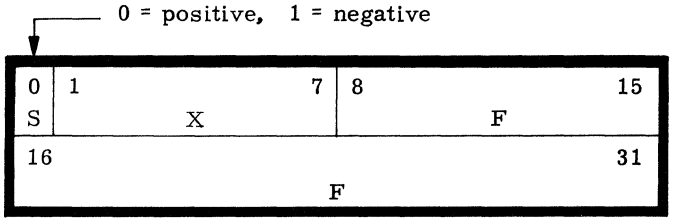
The mini-computer achieves a functional capability similar to much larger and more complex computers through the use of two "read only" memories. These are pre-wired, non-volatile memory units, which greatly reduce the complexity of the Processor logic, by executing micro-instruction subroutines, which in turn, emulate the user instructions.

4.1 DATA AND INSTRUCTION WORD FORMATS

The Central Processor data and instruction words appear both in the hardware and in the documentation in the forms depicted on Fig. 4.1-1. These formats lend themselves to the use of hexadecimal notation, where each hexadecimal digit represents four binary bits ($2^4 = 16$). The hexadecimal digit set and its relation to binary, octal, and decimal notation are described on Table 4.1-1.

Fixed point data are represented in the form of 16-bit halfwords or 32-bit fullwords, where bit 0 is the sign bit. Positive numbers are represented as true binary numbers, with a sign bit of zero. Negative numbers are represented in two's complement form, with a sign bit of one.

Floating point data are represented in fullword form, with bit 0 serving as the sign bit. The number consists of a signed exponent (X) and fraction (F):



Binary	Octal	Decimal	Hexadecimal
0000	0	0	0
0001	1	1	1
0010	2	2	2
0011	3	3	3
0100	4	4	4
0101	5	5	5
0110	6	6	6
0111	7	7	7
1000	10	8	8
1001	11	9	9
1010	12	10	A
1011	13	11	B
1100	14	12	C
1101	15	13	D
1110	16	14	E
1111	17	15	F

Binary (0 15)	Hexadecimal	Decimal	Octal
0111111111111111	7FFF	32, 767	77, 777
0111000000000000	7000	28, 672	70, 000
0000000011111111	00FF	255	377
0000000010000111	0087	135	207
0000000000000111	0007	7	7

Table 4.1-1 Hexadecimal, Decimal, Octal and Binary Relationships

4.2 FUNCTIONAL DESCRIPTION

The overall sequencing of the Processor is controlled by a current Program Status Word (PSW), which is stored in two 16-bit registers in the Micro-Program Register Stack. The left half of the PSW (Fig. 4.2-1) defines the program status. The right half of the PSW defines the location of the next user instruction to be fetched from Core Memory. The PSW is automatically updated as program sequencing progresses and it may be changed by the program.

The PSW is also involved in subroutine linkages and the servicing of interrupts. The program may load a new PSW or temporarily exchange the current PSW

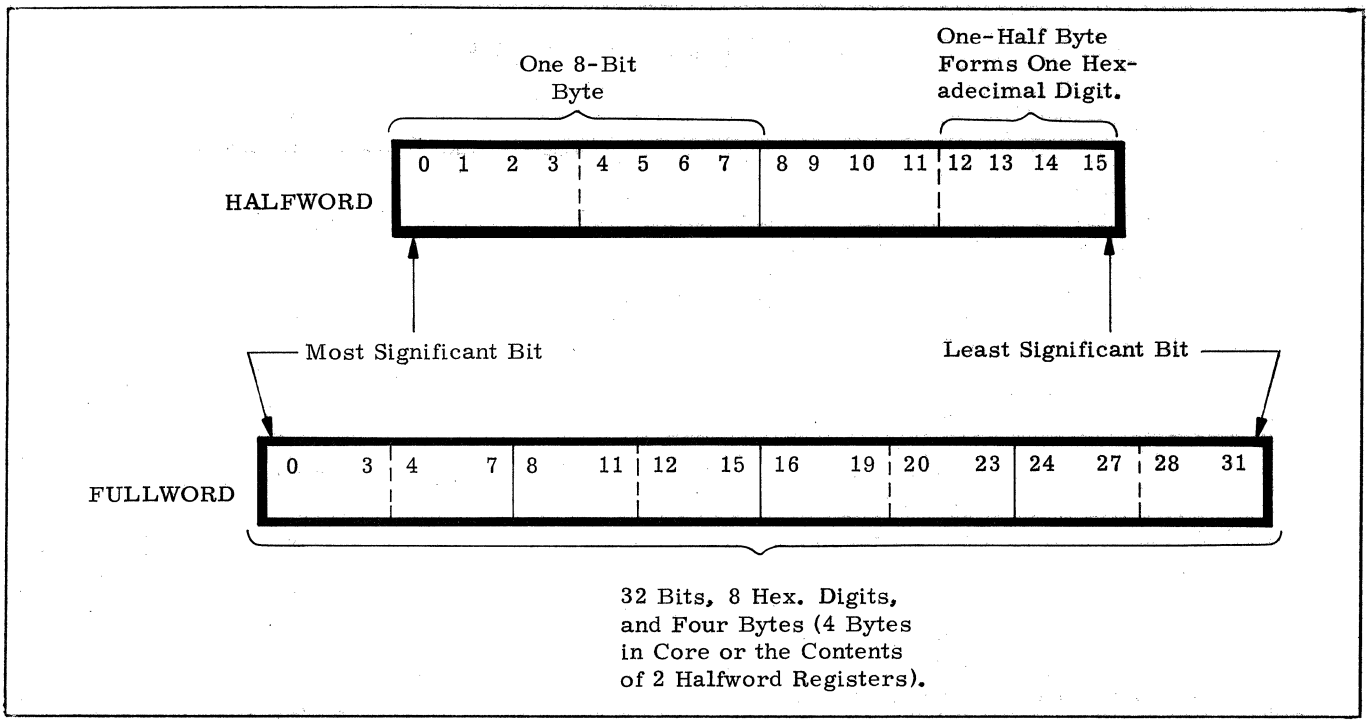


Fig. 4.1-1 Data and Instruction Word Formats

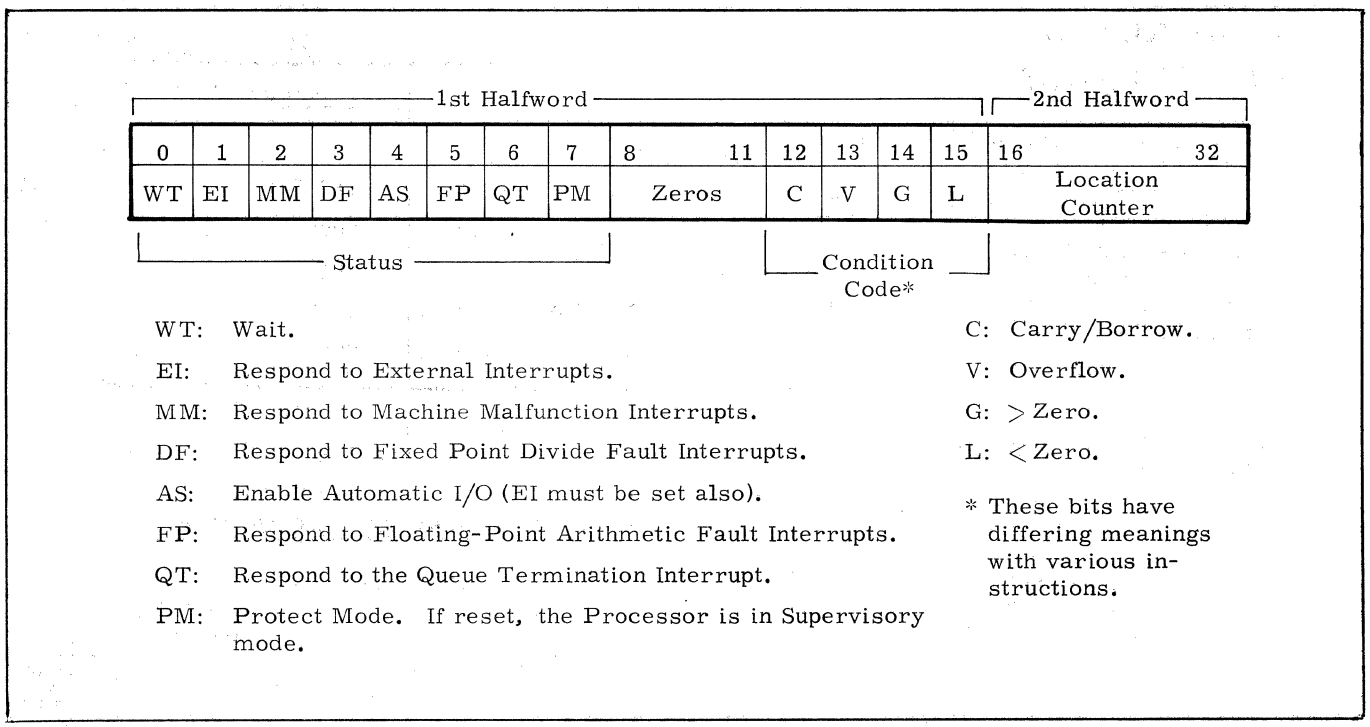


Fig. 4.2-1 Program Status Word

for a new one in order to initiate the execution of a new subroutine. Interrupts which may originate in the Processor or in external controllers, also cause a PSW exchange if they are not inhibited by the current PSW.

The Central Processor executes programs at two levels; the user level, and the "micro" level. At the user level, the Processor accomplishes the work required by the user. For the purpose of this discussion, the user may be considered to be the people and the subsystems external to the Central Processor. The micro-level program executes micro-instructions in a sequence which is pre-wired into the Read Only Memory (ROM). The micro-program subroutines achieve the results specified by the user instructions, by executing micro-instructions, as directed by the ROM.

The Processor hardware includes the logic necessary to execute the set of 17 micro-instructions. The user instructions are not actually executed by hardware but by micro-programs stored in the ROM. Those programs are often referred to as "firmware", to indicate that they exist at some plane between "hardware" and "software".

For a more detailed description of the functions of the GE-PAC 30-2E mini-computer which is used as the 3010 Central Processor, including a description of the instruction set, interrupt handling, and PSW control, refer to the GE-PAC 30/3010 Reference Manual, GET-6047.

4.2.1 Principal Processor Components

S Bus and B Bus. These two busses are 16-bit common tie points for the data destined to and from most of the registers and interfaces in the Processor. Most data is handled on a 16-bit halfword basis or in the form of an 8-bit byte. Usually the S Bus is the source of halfwords and bytes destined to a register. The B Bus typically is an intermediate destination for bytes and halfwords on their way to a register, or a memory or I/O interface. Control logic within the Processor gates data to and from the busses.

Instruction Register. This register stores the user instructions while they are decoded and executed.

Decoder ROM. The Decoder ROM (DROM) translates the operation codes of the user instructions held in the Instruction Register to ROM addresses for entries into the micro-program sequences which emulate the user instructions and service interrupts.

Flag Register. This register stores four bits which reflect carry, overflow, greater than zero, and less than zero results of arithmetic and logical micro-instructions. The Branch on Condition micro-instruction tests the contents of this register in determining the state of the specified condition.

Condition Code Register. This register serves as bits 12 - 15 of the PSW. The register is loaded from the Flag Register after the micro-program has executed the user instruction to indicate the carry, overflow, greater than zero, and less than zero result of the user instruction.

Micro-Register Stack. These are eight working registers used by the micro-instructions. The PSW location code occupies the next to highest of these 16-bit registers and the PSW status halfword is in the highest numbered of these registers.

General Register Stack. These are sixteen 16-bit general purpose registers which may be specified as source and destination registers by user instructions. The general purpose registers may also be used as index registers.

A Register. This register provides one 16-bit operand for the Arithmetic Logic Unit. The other ALU operand is derived from the B Bus.

Arithmetic Logic Unit. The Arithmetic Logic Unit (ALU) performs the arithmetic, logical, and shift functions required by the micro-instructions.

Read Only Memory. The Read Only Memory stores 1536 micro-instruction words. (512 micro-instruction words are wired into the DROM module and the remaining 1024 words are wired into the ROM module.) These 16-bit words are loaded into the ROM Data Register from the address specified by the ROM Address Register. A current pulse line is threaded through 16 "U" shaped linear ferrite cores in each ROM word. For the cores representing a TRUE bit, the current pulse line is threaded inside the core and for those representing a FALSE bit, the line passes outside the core. When a word is to be read, current is pulsed through the line, producing a small voltage pulse into each read-out amplifier connected to a TRUE core. The outputs from the read-out amplifiers load the ROM Data Register.

Multiplexor Channel and Bus. The Multiplexor Channel provides device selection and control logic signals to the Multiplexor Bus, and through that bus, to the optional Selector Channel and/or bus extender. Up to 255 controllers may be connected to the bus. A bus extender module is required for each group of 25 controllers implemented after the first 25. Data passing through the bus in either direction is in the form of 8-bit bytes. The physical location of the modules connected on the bus determines the interrupt priority of the attached controllers and devices.

4.3 CORE MEMORY

The Core Memory stores user instructions and data currently in use by the Central Processor. If the system implements a bulk memory subsystem, such as a drum memory, user programs and data may reside on bulk memory, to be transferred to Core Memory as they are needed. If the system implements Core Memory, only, all instructions and data reside in core.

The Core Memory is a three-wire, coincident current, random access, magnetic core memory. The basic Central Processor includes the first 8K bytes ($K = 1024_{10}$) in each system. The maximum core size is 64K bytes, implemented in modules of 8K each. Core Modules which implement the core above the basic 8K are installed in one or two memory expansion chassis. The Core Memory cycle time (access plus restoration time) is 1.0 microseconds.

4.3.1 Core Memory Format and Addressing

Each of the possible 65,536 8-bit bytes in Core Memory is directly addressable, as the user instruction operand addresses are all 16-bits in length. Each user instruction may require a byte, a halfword, or a fullword to be read from, or stored in Core Memory. However, each core read or write operation transfers one 16-bit halfword. The user instructions may utilize one byte from each halfword, the full halfword, or two successive halfwords.

The core addresses are assigned as successive hexadecimal byte addresses starting with 0000_{16} and ending with $FFFF_{16}$. A group of bytes combined to form a halfword or a fullword are addressed by the lowest numbered byte in the group. Halfword or fullword operands in core must be positioned at even numbered byte addresses. Table 4.3-1 provides some examples of the core addressing scheme.

4.3.2 Parity Option

Where the parity generation and check option is implemented, an "odd ones" parity bit is provided for each 8-bit core byte. The parity bit is generated and stored on a write operation and checked for odd parity on a read operation. If a parity error is detected on a read operation, a Machine Malfunction interrupt and PSW swap occurs. If the "Machine Malfunction - New PSW" is successfully retrieved, the new PSW initiates an error recovery routine.

4.3.3 Memory Protect Options

The basic Memory Protect module protects 16 areas of equal size in Core Memory. These areas are blocks of 256, 512, 1024, 2048, or 4096 bytes. Any or all of the 16 blocks may be selected for protection by jumper wiring or by customer provided switching. If the Programmable Memory Protect Controller option is implemented, the blocks protected may be selected under program control.

Normally, the basic module is wired to protect blocks of 1024 bytes. A simple wiring change (four wires) may be made in the factory or in the field to select any of the other block sizes. Where the block size is 1024 bytes, the first 16K bytes in core are protectable. It follows then, that if blocks of 4096 bytes are protected, an entire 64K byte memory may be protected (4096 X 16 = 65,536 bytes).

	FULLWORD				FULLWORD			
	HALFWORD		HALFWORD		HALFWORD		HALFWORD	
	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE
HEXADECIMAL ADDRESS	0050	0051	0052	0053	0054	0055	0056	0057
CORE CONTENTS	01	23	45	67	89	AB	CD	EF

If a user instruction specifies an operand address of 0050_{16}:

For a byte-oriented instruction the operand is 01_{16}.

For a halfword-oriented instruction the operand is 0123_{16}.

For a fullword-oriented instruction the operand is 01234567_{16}.

If a user instruction specifies an operand address of 0055_{16}:

For a byte-oriented instruction the operand is AB_{16}.

For a halfword-oriented instruction the operand is $89AB_{16}$.

For a fullword-oriented instruction the operand is $89ABCDEF_{16}$.

Table 4.3-1 Core Memory Addressing

An override lead is brought out from the basic module to allow the protection to be defeated temporarily. Grounding a block select line defeats protection for that block. When an attempt is made to write in a protected location, the write request is treated as a read request, and an error flip-flop is set. The flip-flop output is available to the Programmable Memory Protect Controller or to the user, if manual selection is used.

Programmable Memory Protect Controller

The 3000AB3102 Programmable Memory Protect Controller (PMPC) option occupies one slot on the Multiplexor Bus (refer to 4.6) and utilizes one device address, normally X'AE'*. If the PMPC is implemented, the Central Processor must implement Core Memory with the basic memory protect option.

The program sets up the PMPC by issuing an appropriate Output Command to the controller (Fig. 4.3-1) and then issuing two Write Data instructions which transfer the appropriate protect pattern to the PMPC. The first byte transferred specifies the upper half of the pattern, and the second byte specifies the pattern for the lower half of core. Each of the sixteen bits controls one of the sixteen protect blocks in the basic memory protect module. The more significant bits control the higher protected core addresses. A bit set protects its associated block and if reset, writing in the block is permitted.

Should an attempt be made to write in a protected area, if external interrupts are enabled by the current PSW, and if the last Output Command to the PMPC enabled interrupts, the PMPC will interrupt the running program, as the error flip-flop in the basic protect module sets.

Command Byte
Status Byte
Bit

0	1	2	3	4	5	6	7
0	BS	PON	PWF	0	EX	0	0
DARM	ENAB	PON	POFF	NBS	BS		

Fig. 4.3-1 PMPC Command and Status Bytes

Status; the status bits have the following meaning (Fig. 4.3-1):

- Bit 1 = 1 = Block Switch. BS will normally be reset in 3010 systems. In systems with more than 64K bytes of core, BS is set when the core above 64K is selected for protection. Maximum core size in 3010 systems is 64K bytes.

*The notation "X' ' ", indicates that the digits between the single quote marks are expressed in hexadecimal form.

- Bit 2 = 1 = Protection On. PON is set when memory protect is enabled.

- Bit 3 = 1 = Protect Write Flag. PWF sets when an attempt is made to write in a protected area. PWF is reset by another Output Command, an Acknowledge Interrupt instruction, or when the Initialize button on the Display Panel is pushed.

- Bit 5 = 1 = Examine. EX = PWF.

Output Commands; the Output Command bits have the following meaning (Fig. 4.3-1):

- Bits 0 and 1 = interrupt disarm and enable, respectively. When enabled, the interrupt occurs when the error flip-flop in the basic protect module sets, indicating an attempt to write in a protected core area. When disarmed, the PMPC interrupt queue flip-flop is reset.

- Bit 2 = 1 = Protect On. PON specifies that the areas to be specified by the next two Write Data instructions be protected.

- Bit 3 = 1 = Protect Off. POF turns on the override signal to the basic protect module to disable memory protection.

- Bit 4 = 1 = Not Block Switch. NBS specifies that the protection pattern applies to the lower 64K of core. Since 3010 systems cannot have more than 64K, this bit is normally set in each Output Command.

- Bit 5 = 1 = Block Switch. This bit is not used with 3010 systems. In systems with more than 64K of core, this bit specifies that the protection pattern applies to core above 64K.

It is possible to protect smaller blocks of core and still cover all of a 64K Core Memory by implementing a second PMPC, wiring the basic Memory Protect module to specify blocks of 2048 bytes, and using the two PMPC's to maintain 16-bit protect patterns specifying protection for 64K bytes (32 x 64K = 65,536 bytes).

4.4 INTERRUPTS

Interrupt signals request that the current Processor status be saved, and that the Processor branch to a service or corrective routine. Interrupts may originate within the Processor or outside the Processor. When the routine requested by the interrupt is completed, the status may be restored and the interrupted program may resume.

When an interrupt is serviced, the content of the Processor's PSW register is stored in a dedicated "old PSW" core location, and a PSW pointing to the

servicing routine is loaded into the PSW register. When the service routine is completed, the PSW register may be loaded with the old PSW and the interrupted program may resume.

The Processor's response to interrupts is under the control of the Program Status Words. The current PSW, which is stored in the Processor's PSW register defines the current status, and controls the response to seven of the interrupt types. The following is a list of the types of interrupts and the PSW bits which control the seven inhibitable types. The program may permit interrupt servicing by setting the appropriate control bits and may inhibit interrupt servicing by resetting control bits. The I/O Controllers on the Multiplexor Bus store (queue) interrupts until they are acknowledged, unless they are disarmed by an Output Command issued to the controller. Output Commands may disable interrupts from some controllers, but allow the interrupt queue flip-flop to store the interrupt.

Type	Internal or I/O Control	PSW Control Bit
External	I/O	1
Machine Malfunction	Int.	2
Fixed Point Divide Fault	Int.	3
Automatic I/O Service	I/O	4
Floating Point Arithmetic Fault	Int.	5
I/O Termination	I/O	6
Protect Mode Violation	Int.	7
Illegal Instruction	Int.	
Termination Queue Overflow	I/O	
Supervisor Call	Int.	

For a detailed discussion of the use of interrupts and the Central Processor's responses, see Section 2 of the GE-PAC 30/3010 Reference Manual, GET-6047. The following paragraphs describe some aspects of interrupt configuration, servicing, and priorities, of particular significance in GE-PAC 3010 systems.

4.4.1 Protect Mode

Where the system programs are under the control of an operating system such as RTMOS-30, PSW bit 7 is set to specify Protect Mode when the user programs controlled by the operating system are running. PSW bit 7 is reset when the operating system programs are running. Only the operating system has the priviledge of executing the subset of I/O and PSW exchange instructions (Output Command, Read Data, Write Data, Sense Status, Acknowledge Interrupt, Auto Load, Exchange PSW, Simulate Interrupt, etc.). When in the Protect Mode, if an attempt is made to execute one of these "priviledged" instructions, a Protect Mode interrupt occurs. If such an interrupt occurs, the instruction is not executed, the location counter in the current PSW is not incremented, and the old PSW stored as a result of the swap initiated by the interrupt points to the location of the priviledged instruction which caused the interrupt.

If the Programmable Memory Protect Controller is implemented, and should a user program attempt to write in an area defined for protection by the pattern held by the PMPC, the PMPC will attempt to generate an external interrupt. If the PMPC interrupt is not disarmed, and if the current PSW has bit 1 set, the interrupt will be serviced. Regardless of the PMPC interrupt status, the protection feature will prohibit writing in the protected area, and if the program is not interrupted, instruction sequencing will continue.

4.4.2 I/O Interrupts

The Central Processor may be interrupted by any of the I/O controllers on the Multiplexor Bus to which it may address instructions. Since all I/O instructions have an 8-bit device address field, the Central Processor may address up to 256_{10} devices. Since every GE-PAC 3010 system has a Programming and Maintenance Display panel, an I/O typer, and in most cases, a 60 Hz Clock module, 253 addresses are left to accomodate additional input/output controllers of all types.

I/O interrupt priority is determined by the physical location of the controller on the Multiplexor Bus, and not by the device address. When the Processor is interrupted, the Processor sends an Acknowledge pulse down the Multiplexor Bus. When the pulse encounters a controller with the interrupt queue flip-flop set, the pulse is stopped and the device address is returned to the Processor to indicate which controller originated the interrupt.

The Acknowledge pulse may be generated by the micro-program if Automatic I/O service is enabled (PSW bits 1 and 4 set) or it may be generated by the execution of an Acknowledge Interrupt instruction by the program (PSW bit 1 set and bit 4 reset). Typically the first controllers on the Multiplexor Bus are the Display Panel Controller, the Programmable Memory Protect Controller (if implemented), the 60 Hz Clock module (if implemented), and the I/O typer controller. The Display Panel would then have the highest interrupt priority, and the priority decreases by one as each controller is implemented on the bus.

4.4.3 External Interrupt Module

Up to four 3000AF11 External Interrupt Modules may be implemented as I/O modules on the Multiplexor Bus. Each such module provides an interface to as many as eight external interrupt terminations. The

inputs are connected to terminations in the Central System Cabinet and are relay isolated. Power (12 VDC) and contacts to control the relays are provided by the user or the interrupts may be derived from the optional 3010AF16 Change Detect Digital Input Terminations (see 9.1.1).

Each external interrupt implemented uses one I/O Multiplexor device address. The external interrupts are armed or disarmed and masked or unmasked by Write Data instructions addressed to the lowest device number assigned to the module. Four such device numbers are possible: X'20', X'28', X'30', and X'38'. Once initialized by pushing the Initialize button on the Display Panel or issuing an Output Command to the interrupt module, the first Write Data instruction specifies which interrupt lines are to be armed or disarmed and the second Write Data instruction specifies which interrupts are to be masked or unmasked. Bits 0 through 7 of the data byte correspond to interrupts 0 through 7, with interrupt 0 having highest priority. Successive Write Data instructions are presumed to transfer arm/disarm and mask/unmask bytes, respectively.

A bit set in an arm/disarm byte allows the corresponding interrupt queue flip-flop to set when the corresponding relay energizes. A bit set in a mask/unmask byte allows the interrupt to be applied to the Processor, and to be serviced if bit 1 of the current PSW is set. The lowest device address implemented on an External Interrupt Module is selected with jumper wiring on the module, and determines the device address corresponding to interrupts 0 through 7 as follows:

X'20' through X'27'.

X'28' through X'2F'.

X'30' through X'37'.

X'38' through X'3F'.

When the External Interrupt Module is initialized, all eight interrupts are disarmed and masked.

4.5 PROGRAMMING AND MAINTENANCE DISPLAY PANEL

The Central Processor Display Panel allows direct communication with the machine by programming and maintenance personnel. It communicates with the Processor through a Display Controller module on the Multiplexor Bus. The Display Panel functions are effected by a micro-program sequence which is initiated by a console interrupt. The interrupt is generated when the Execute button on the panel is pushed. The running program may also communicate with the console by issuing I/O user instructions to the Display Controller (Device address X'01'. See subsection 5.6 of the GE-PAC 30/3010 Reference Manual, GET-6047).

Two register displays are provided and all 16 of the General Registers may be selected for display, two at a time. The panel features a speed control selector, which allows user instruction sequencing to proceed at variable speeds or in a single step mode, 16 input data switches, a Power On button, a hardware Initialize button, and the Execute button. The control functions are as follows (refer to Fig. 4.5-1):

4.5.1 Mode Control Switch

The Mode Control Switch selects the Central Processor's mode of operation. When a new mode is selected, the Execute button must be pushed to effect the change. The modes are as follows:

Run. Instruction sequencing is continuous at full speed. Displays 1 and 2 do not change in this mode.

Halt/Flt. Instruction sequencing stops when the Execute button is pushed and the registers selected by the Register Display switch are displayed in Display 1 and Display 2. In this mode the register displays are in the floating point format which is illustrated at the top of the panel and is described in subsection 4.1 of this manual.

Halt/Fix. Instruction sequencing stops when the Execute button is pushed and the registers selected by the Register Display switch are displayed in Display 1 and Display 2. In this mode the register displays are in fixed point format.

Vari/Flt. Instruction sequencing proceeds at the speed selected by the Speed Control and the registers selected by the Register Display switch are displayed in Displays 1 and 2. In this mode the register displays are in floating point format.

Vari/Fix. Instruction sequencing proceeds at the speed selected by the Speed Control and the registers selected by the Register Display switch are displayed in Display 1 and Display 2. In this mode the register displays are in fixed point format.

Adrs. With the system in the Halt mode, the content of the 16 Data Switches is entered in the Location counter field of the PSW Register when the Execute button is next pushed.

Memr. With the system in the Halt mode, the content of the Core Memory halfword specified by the PSW Location counter is displayed in Display 2 when Execute is next pushed. The address from which the data was read is displayed in Display 1. The PSW Location counter is incremented after Execute is pushed.

Memw. With the system in the Halt mode, the content of the 16 Data Switches is written in the Core Memory location specified by the PSW Location counter. The data written in core is displayed in Display 2 and the core address in which

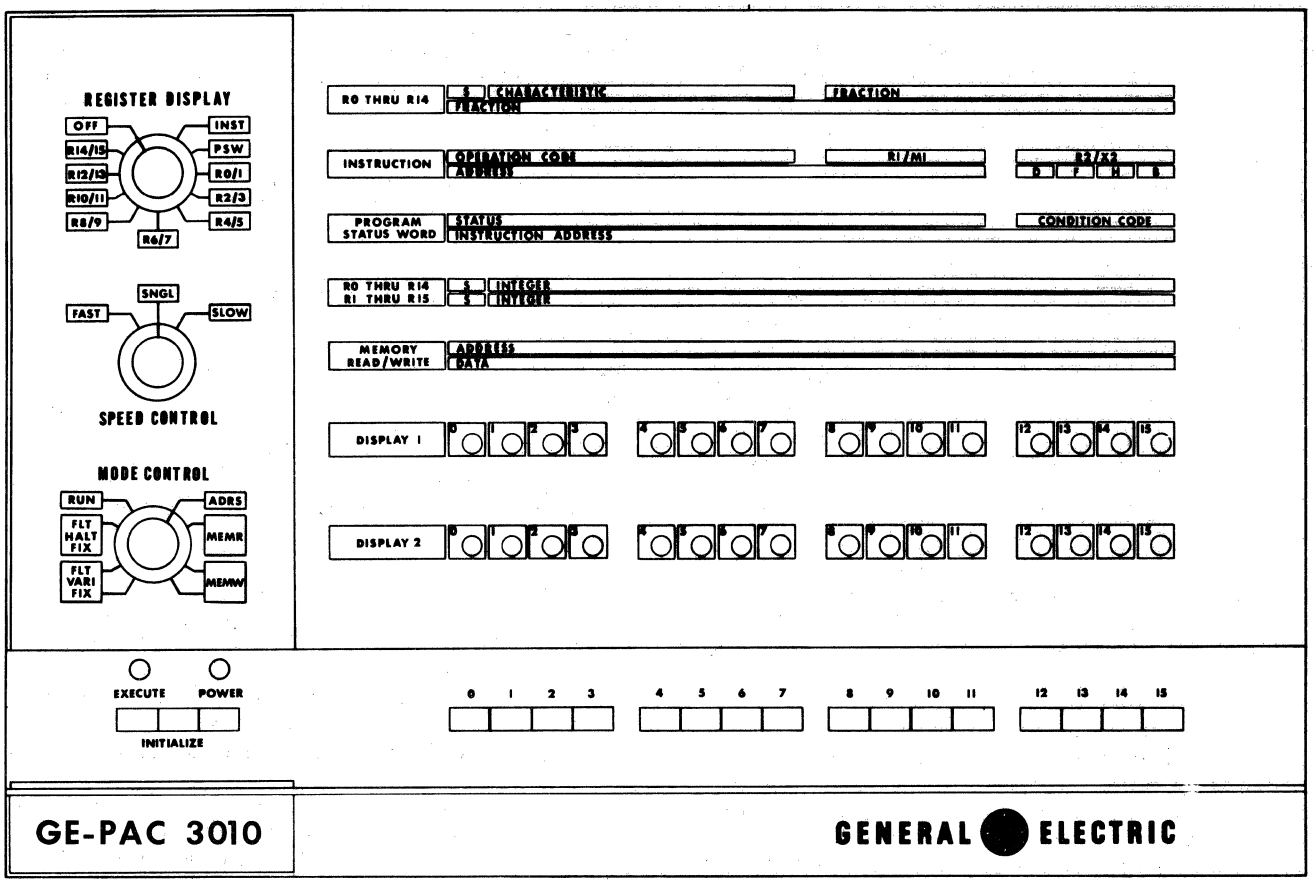


Fig. 4.5-1 Display Panel

it was written is displayed in Display 1. The PSW Location counter is incremented after Execute is pushed.

4.5.2 Speed Control

The Sngl position is the most counter clockwise position of the control and if in one of the two Variable speed modes, specifies the execution of one instruction each time the Execute button is pushed. When rotated between the Slow and Fast positions, instructions are executed at from 1 instruction per second to 100 instructions per second, as determined by an oscillator in the Display Controller which generates the console interrupt at the rate selected by the Speed Control.

4.5.3 Register Display Switch

The Register Display switch selects pairs of Processor registers to be displayed when in one of the Halt or Variable speed modes. If a new display pair is selected, Execute must be pushed to change the display. Diagrams on the panel define the content of the displays for each switch position, except Off, which will cause Displays 1 and 2 to be blank after Execute is pushed.

4.5.4 Data Switches

The 16 data entry switches at the bottom of the panel mechanically latch in when first pushed and then release when pushed again. When in the depressed position, the switches enter a "one" in the corresponding bit position of the PSW Location counter, when Execute is pushed while in the Address mode. When in the Memory Write mode, data is written in the core location specified by the Location counter. A released Data Switch enters a "zero" in the corresponding bit position.

4.5.5 Power, Initialize, and Execute Buttons

The Power switch is a latching switch which turns on the logic power supplies in the Central System Cabinet when in the depressed position, providing primary AC power is applied to the cabinet. When the logic supply is on, the lamp above the Power switch is lit.

The Initialize button activates a momentary switch which initializes all logic hardware in the Central Processor and on the Multiplexor Bus.

The Execute button activates a momentary switch that generates a console interrupt which initiates the Display Panel micro-program, effecting any changes called for by the Mode Control or Register Select Switch.

The indicator above the Execute button is the Wait lamp which is lit when bit 0 of the current PSW is set, instruction sequencing is halted, and the program is awaiting operator action or an interrupt to resume sequencing. If, while this lamp is lit, Run mode is selected and Execute pushed, instruction sequencing will continue from the core address specified by the Location counter field of the PSW register.

4.6 INPUT/OUTPUT SUBSYSTEM

The principal elements of the Central Processor's Input/Output Subsystem are the Multiplexor Channel and Multiplexor Bus. The Multiplexor Channel and Bus provide a total of 27 data and control lines to each attached device controller, remote communications controller, or process I/O controller. The Multiplexor Bus also provides control lines via the Selector Channel (section 6) to the controllers which communicate with core through the High Speed Memory Bus Controller.

The Multiplexor Bus may serve as many I/O controllers as the Central Processor can address, so the maximum number is 256. Every system has to start with at least a Programming and Maintenance Display Panel Controller, and I/O typer controller, and in most systems, a 60 Hz Clock Module, so 253 addresses are left to accomodate additional controllers of all types.

All I/O controllers have virtually identical interfaces to the Multiplexor Bus and consist of one or two printed wire boards (PWB's). Any such modules may be installed on the bus in the factory or in the field, if empty slots are available. Usually only the removal of one or two back-panel wires is necessary to implement a new controller.

Input/Output data are transferred on the bus in the form of 8-bit bytes. The transfers are program controlled by user instructions which address the appropriate controller, sense the status of the controller, and read from or write into the controller. Interrupt driven I/O capability is also included in the Processor. Refer to Section 3 of the GE-PAC 30/3010 Reference Manual, GET-6047, for a detailed description of the Input/Output operations.

The basic Multiplexor Channel can serve up to 25 I/O controllers and 3000AE71 Multiplexor Bus Extender modules must be added to accomodate additional groups of 21 controllers. 3010AE74 Multiplexer Bus Switches may also be implemented to allow two or more Central Processors to communicate on a mutually exclusive basis, with controllers on a bus which is common to the Central Processors. Refer to Section 5 for additional information on bus extension and switching.

4.7 POWER FAIL DETECTOR AND AUTOMATIC RESTART

The primary AC supply to the Central Processor is monitored by a Power Fail Detector. Should the line voltage decrease to 95 VAC or less, or should power be lost for more than one cycle, the contents of the General Register Stack and the PSW Register are automatically stored in Core Memory and an orderly shut-down of the power subsystem is initiated.

If the primary power returns to normal before the optional Restart Inhibit Timer runs out, the hardware is initialized, the General Registers and PSW Register are automatically restored, and if bit 2 of the restored PSW is reset, instruction sequencing continues from the point at which the shut-down occurred.

If bit 2 of the restored PSW is set, a "Machine Malfunction" PSW swap occurs. The software routine thus initiated must determine if it was initiated by an automatic restart or a malfunction such as a core parity error. If the routine finds the "Machine Malfunction - Old PSW" dedicated core location contents equal to the contents of the location at which the current PSW was stored, an automatic restart has occurred.

4.7.1 Restart Inhibit Timer Option

The optional 3010AB14 Restart Inhibit Timer prevents automatic restarts if enough time has elapsed since power failure was detected, that the computer cannot be safely restarted without manual intervention. The timer may be adjusted with a calibrated dial in a range from 10 seconds to 10 minutes. The time selected is determined by the customer's consideration of the effect of an automatic restart on the process, controls which may "back-up" the computer, etc.

4.8 SYSTEM ALARMS OPTION

The optional 3010AB33 System Alarms module provides a visual indication at the PWB front edge of six system alarm conditions. The alarm conditions may be sensed by the running program and are available as relay driver outputs from the module. The alarm conditions are:

- Power Failure. This alarm is set when the Power Fail Detector (4.7) detects a failure and when the system hardware is initialized during an automatic restart or by pushing the Initialize button on the Display Panel.
- Stall Alarm. This alarm is set when the stall timer (4.8.1) times out.
- Parity Alarm. Sets when the optional core parity check logic (4.3.2) detects an error.
- Overtemperature Alarm. Sets when a temperature sensor in a Core Memory module detects an excessive temperature. The

alarm point is set with a screwdriver adjustment on the System Alarms module. The adjustment range is from 40° C to 50° C.

- I/O Alarm. This alarm is set when the program issues a Write Data instruction to the System Alarms module with bit 6 of the data byte set. The meaning of this alarm is to be defined by the programmer.

- Programmable Alarm. This alarm is set when the program issues a Write Data instruction to the System Alarms module with bit 7 of the data byte set. The meaning of this alarm is to be defined by the programmer.

Each of these alarm conditions set a bit in an Alarm Register and lights the corresponding lamp on the edge of the System Alarms module PWB, as shown on Fig. 4.8-1.

4.8.1 Stall Alarm

The stall alarm feature is used to detect program or hardware malfunctions which cause a delay in program sequencing. If a program sequence delay exceeds the time period of the stall alarm timer, status bit 1 is set, and the System Alarms interrupt queue flip-flop sets. The timer is adjusted, by means of a screwdriver adjustment on the System Alarms module, to any period from 1 second to 5 seconds. An Output Command instruction which transfers a command byte with bit one set, restarts the timer. Such a command is placed at several appropriate points in programs which run with the timer enabled. If the stall alarm is set and bit one of the current PSW is reset, the PSW swap which occurs because of the System Alarms interrupt, may branch to a corrective routine. When the Processor acknowledges the interrupt, the queue flip-flop and the stall alarm status bit are reset, but the timer is not restarted.

A Stall Enable/Disable switch is provided on the front edge of the System Alarms PWB. In the Disable position, the switch locks out the stall alarm feature by resetting the timer and the interrupt queue flip-flop. Also, when in the Disable position, the switch lights the Stall Lockout indicator lamp and sets status bit 2 (Fig. 4.8-1).

4.8.2 Hardware Alarm

Alarm Register bit 5 (Fig. 4.8-1) is set when the Power Fail, Stall Alarm, Stall Lock-out, and/or Parity Alarm bits are set. Three screwdriver actuated switches are provided on the System Alarms PWB to select the Overtemperature Alarm, I/O

Bit	0	1	2	3	4	5	6	7
Status Byte*	PWF	SALM	SLO	PTY	TEMP	HDW	I/O	PRGM
Command Byte	C	C		C			C	C
Relay Driver Alarm State	Off	Off	Off	On	On	On	On	On
Indicator Alarm State	On	On	On	On	On	On	On	On

Top — Bottom

*Transferred to Processor by Sense Status or Read Data Instructions.

PWF: Power Failure.

SALM: Stall Alarm.

SLO: Stall Lock-Out (Disable).

PTY: Core Parity Alarm.

TEMP: Overtemperature.

HDW: Hardware Alarm = PWF + SALM + SLO + PTY, (TEMP + I/O + PRGM Optional).

I/O: I/O Alarm.

PRGM: Programmable Alarm.

C: Clear the Alarm.

Fig. 4.8-1 System Alarms Command Byte, Status Byte, and Alarm Indicators

Alarm, and Programmable Alarm also, to set the Hardware Alarm indicator and relay driver, but not status bit 5.

4.8.3 Relay Driver Outputs

Each of the eight Alarm Register bits (Fig. 4.8-1) controls the state of a relay driver which may be used to provide an external indication of the alarm status. These outputs may be used to drive controls and indicators in external equipment such as process operator consoles.

When "on", each relay driver is capable of returning up to 200 milliamperes DC to a common return line. In the "off" condition, each driver can withstand up to +35V with respect to the common return. The drivers may be used to drive lamps directly if the inrush current, as occurs with incandescent lamps, does not exceed the maximum. A daughter board location on the System Alarms PWB is reserved for the possible implementation of a daughter board with "keep warm" resistors, which would maintain a minimum current flow through the lamps while they are dark, minimizing the inrush current.

A 3010AF2401 Termination Assembly which implements a 3010AF2402 8-Point Output Relay module is the standard relay interface with the alarm module. A +12V power supply such as 3010AL35 or 3010AL38 is required to supply the relay power.

4.9 60 HZ CLOCK

System timekeeping is accomplished by programs which utilize timed interrupts generated by the 3000AF41 60 Hz Clock module. Operating systems such as RTMOS-30 require the clock module for system timekeeping. The 60 Hz Clock module is a standard controller module which may be installed in any slot on the Multiplexor Bus, but is normally assigned the second highest interrupt priority (the Display Panel is normally assigned the highest priority. See 4.5).

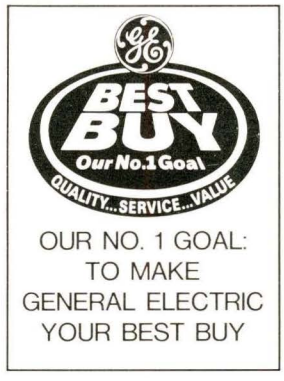
The computer's primary AC supply is used to control the clock module timing. When enabled, the interrupt queue flip-flop in the clock module is set every 25 milliseconds (every three 60 Hz half-cycles) or every 250 milliseconds (every 30 60 Hz half-cycles), as specified by a command byte.

The 60 Hz Clock module responds only to Output Commands and Acknowledge Interrupt instructions. When the computer is initialized, the clock interrupts are disabled. Output Commands transfer command bytes to the module to specify the mode of operation as indicated on Table 4.9-1. The interrupt queue flip-flop is reset when each interrupt is acknowledged.

The 60 Hz Clock module is normally assigned device address X'4C'. The address may be changed by reconnecting jumper wiring on the clock module.

Command Byte	Definition
X'40'*	Enable the clock interrupt at the last rate specified.
X'08'	Select the 25 ms rate.
X'04'	Select the 250 ms rate.
X'02'	Disable the clock.
X'80'*	Disable the clock interrupt but allow the interrupt queue flip-flop to store the next interrupt.
* These commands could also specify a rate change, i.e., X'48', X'84', etc.	

Table 4.9-1 60 Hz Clock Command Bytes



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TO MAKE
GENERAL ELECTRIC
YOUR BEST BUY

GENERAL ELECTRIC