M243XL

Magnetic Tape Subsystem Maintenance Manual



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PART I FIELD TESTER FUNCTIONS AND OPERATIONS

INTRODUCTION

Part I of the Maintenance Manual is divided into three sections. Section 1 describes the field tester front panel controls and indicators.

Section 2 describes the use of the field tester when connected to the MTU. In this mode, the field tester is used to control the MTU during fault isolation, testing, and while making adjustments during maintenance. During normal operation, if a problem occurs in the MTU, then:

- (1) An error code is displayed on the MTU operator panel.
- (2) An error code is stored in the FMT register.
- (3) A code is sent to the host controller.

MTU troubleshooting is accomplished by using the Maintenance Manual as an error code look-up table that directs the user to corrective action. The field tester, when connected to the MTU, assists in these tasks, including checks and adjustments after the corrective action is taken.

Section 3 describes the use of the field tester when connected to the FMT. In this manual, the field tester is used to implement diagnostic routines and to examine diagnostic routine numbers and error codes stored in the FMT registers. The field tester can also be used in more complex operations by control of the microprocessor. This application is intended for those users who have been thoroughly trained in extended use of the field tester and the Test Magnetic Tape System (TMTS) routine. However, this extended usage is also included at the end of Section 3 as reference material.

PART I.1 FIELD TESTER FUNCTIONS

The field tester consists of 12 lamps and 11 switches. The primary purpose of the field tester is to assist in maintenance. The field tester can perform many functions; however the most common functions used in this maintenance manual are to:

- (1) Initiate diagnostics of the FMT and MTU.
- (2) Display error codes stored in the FMT registers.
- (3) Exercise manual control of the MTU.

The field tester also provides the capability of register display, register write, command control, and microprogram control.

The eternal appearance and names of switches on the field tester are shown in Figure 1.

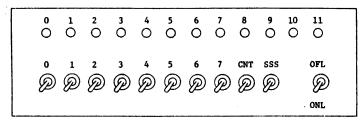
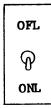


Figure 1. Field tester front panel.

OFL/ONL (two-position toggle switch)



The OFL/ONL switch is used to change the FMT between the online and offline states. When it is switched, the FMT executes System Reset.

The OFL setting places the FMT/MTU under control of the field tester. When in this mode, FMT or MTU will ignore commands from other units. The ONL setting allows the FMT or MTU to respond to other devices while the field tester monitors and/or interrupts operations.

SO through S7 (two-position toggle switches)



These switches are used to set the register address, command, byte count, or start/stop address to be displayed and provide control information such as a command/microprogram control. Generally, the up position indicates a "1" or logical high; the down position indicates a "0" or logical low. The switches can be used in various number formats (hexidecimal, binary) as explained in subsequent paragraphs that describe field tester applications.

PART I.1 FIELD TESTER FUNCTIONS

CNT (two-position momentary toggle switch)

CNT

9

This nonlock-type switch is used to set the various control modes of the field tester. It is also used to display the contents of the internal register.

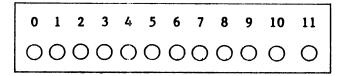
SSS (two-position momentary toggle switch)

SSS

9

This nonlock-type switch is used to set the data necessary to control the internal register, to start a command execution, and to step the microprogram for various control functions provided on the field tester.

LO through L11 (lamps)



The 11 lamps are used to display the data of various display functions. They are active (asserted) when lit.

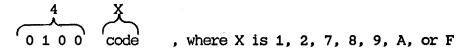
Field tester control functions, when connected to the MTU at 1C05, are summarized in Table 1. Each of these control functions are described in more detail later in this section.

Table 1. Field tester/MTU control functions.

						Switt	h				Contents				
SVOK	Command	0	ı	2	3	4	5	6	7	HEX					
											Ol Forward Normal Continuous go to EOT				
											U2 Forward Streaming Continuous go to EUT				
١. ا						1					07 Forward Fast go to EOT				
ı	Forward read	0	0	0	0	-	Co	ie		ΟX	OR Load-Uniond Repeat action				
	2 61 100										09 Forward Normal Continuous - Rewind Repeat action				
						1					UN Forward Streaming				
0											OF Auto Load				
						1				41 Backward Normal Continuous go to EOT					
						1					42 "Streaming				
	Backward read action	0	ı	0	0		Со	Code		4X	47 Rewind 49 Backward Normal Continuous - Forward Fast repeat				
	ACCION		İ								4A " Streaming " "				
					1						4F Union				
		<u> </u>	<u> </u>			 		T		1X	Short time turn				
	Turn	0	Long/ Short	0	1	FWD	t ine-	HWD	t Ime	5X	long time turn				
			 -	 		 		 		2 X	Forward Start/Stop (Short time) - Rewind repeat				
			BWD/		Long/			١		3X	" (Long time) " "				
	Start/Stop	0	FWD	1	Shore	Co	up	Go d	UAU	6x	Backward Start/Stop (Short time) Forward Fast repeat				
				1	ŀ			1		7X	" (Long time). "				
					L			····							
			Settlin				Switch [4,5	, ,			10 11				
1			Turn an Stop	d St	erc/		16.7		•		10 11				
			,			Mode		0.	_	85	8 mg 20 ms				
							t time	50 .	f		400 ms 1000 ms				
			.,,		· 1			нь/	High/						
	Write	1	O	0	0	WRT/ ERS	SACC	LD	Low	8x	Continuous Write or Erase to EUT				
	AGC OF GSD	1	0	1	1	Stop	Singl/ Repeat		0	BX	SAGC or GSD action (Stice level is to be Normal.) Forward Read (Settle the gain of GCR.)				
	DGC AMP	1	1 1	0	EWU/	CN8	CN4	CN2	CNI	CX DX	Hackward Rend (")				
						WRT/		HD/		+	Hattard Commission Michiel				
	Hode set	1	1	1	0	RD	STRHU	LD	0	EX	Read , Normal , Low Density set				
1						0	LVI.TO	LVLT1	LVLT2		Set Slice level.				
l	Slice level	ı	1	1	1					7,7%	F9 Set Slice level to 90%.				
1	set	•	1.1	•	•	ı		- Code-		٠	FA " 100%. Only GCR, PE				
			ŀ							_	FB " 110Z,				
1/0	Photo sensor					0	1	0	ı	95	BOT/EOT sennor, Error Code check				
	check	1	l°	0	1	1	ERCUT	0	High/ Normal	9x	Capatan tacho pulse check of High/Normal Speed (When ERCUT is equal to 0, it stops once by error.)				
			1			0	ATRDV	SOLVI.	PRSVL		Air supply motor, Solesoid/Pressure Valve drive				
	Air system action	1	0	1	0	1	0	Capstan	BWD/ FWD	1 ^ X	For Check and Adjustment of Capacitive Sensor				
		 	1					•		T	81/89 Cartridge drive				
										1	B2/RA Auto cleaner drive				
"	Hechanism	1	0	1	ı	Repeat	<u> </u>	Code		- BX	84/BC Error marker drive				
	action	٦									86/SE Window drive				
1	1									1	B7/BF Drive all of above				
	Capstan	1	1	0	0	0	0	0	0	co	D/A Converter action check				
	circuit check Reel drive	1	1,	0	1	Slow/ Fast	BWD/ FWD	HR	FR	DX	Machine and File reel drive				
1,40		١.	+	—	1.			.	1	77	Reset (some as Reset button of the operator panel)				
1/0	Reset	1	1	1	ī	1	1	1	l ·	77	Reset (same as Reset button of the operator panel				

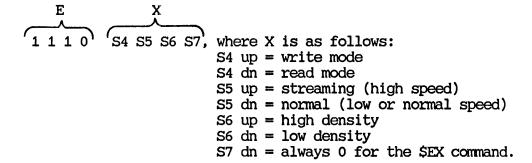
The field tester control functions summarized in Table 1 fall into two categories. An example of each type is given below.

Example 1: All eight switches are coded in hexidecimal notation. Consider the \$4X command.



If the switches are set to \$42 (refer to Table 1) and the field tester SSS front panel switch is momentarily set to up and released (toggled), then the MTU tape will rotate in a reverse (backward) direction at a high speed (streaming) until the BOT (beginning of tape) marker is detected. The tape will stop automatically at a predetermined position. These commands in normal operation are supplied by the host/controller, decoded by the FMT, and issued to the MTU. Using the field tester, virtually all commands normally supplied by the FMT, can now be supplied by the field tester in an offline mode. Under these conditions, the field tester is an extremely valuable tool for maintenance and troubleshooting.

Example 2: The first 4 (or 3) switches are coded in hexidecimal notation and the second group of four (or 5) switches are decimal (where each switch has a separate function). Consider the \$EX command:



The actual values for high speed and low speed are dependent on the specific MTS model. The same is true for the actual value of high/low density.

COMMAND MODE

Execute MTU commands as follows:

- (1) Put the MTU in the offline mode. (Press OFFLINE on the MTU front panel.)
- (2) Set the OFL/ONL switch on the field tester to OFL.
- (3) Set a command using field tester switches 0 through 7. (See Tables 1 and 2.)
- (4) Toggle the SSS switch on the field tester. The operation starts and lamp (LED) 9 illuminates.
- (5) The operation stops (when LED 9 is on) if the SSS switch is toggled again.

Forward/Backward Motion (\$0X, \$4X)

During this operation, the MTU enters read status automatically. See Table 2, below.

Table 2. Forward and backward read action.

Direction	Switch settings (0 through 7)	Contents				
	\$01	Continuous running in forward direction to EOT (end of tape) in normal speed mode.				
	\$02	Continuous running in forward direction to EOT (end of tape) in streaming (high speed) mode.				
	\$07	Continuous running in forward direction to EOT (end of tape) at abouty 200 ips.				
Forward	\$08	Repeated auto load and unload operation.				
	\$09	Continuous running in forward direction in streaming mode and rewind on EOT (end of tape).				
	\$0A	Continuous running in forward direction in normal mode and rewind on EOT (end of tape).				
	\$0F	Auto load.				

Table 2. Forward and backward read action. (continued)

Direction	Switch settings (0 through 7)	Contents
	\$41	Continuous running in backward direction to BOT (beginning of tape marker) in normal mode.
	\$42	Continuous running in backward direction to BOT (beginning of tape marker) in streaming mode.
Backward	\$47	Rewind
	\$49	Continuous running in backward direction in normal (lowspeed) mode and on BOT (beginning of tape) high speed in forward direction.
	\$4A	Continuous running in backward direction in streaming (high speed) mode and upon BOT, high speed in forward direction.
	\$4F	Unload

Bidirectional Start/Stop Motion (\$1X, \$5X)

When performing bidirectional start/stop motion at a specified interval, the time in the forward direction is set by SW4/5 and in the backward direction by SW6/7. When SW1 is on, the action time is long; when SW1 is off, the action time is short.

Switch number										
0	1	2	3	4	5	6	7			
0	1 = long 0 = short	0	1	Forward time (see table below)		Backward time (see table below)				
		U	_							

SW 4,5 and 6,7 Mode	0 0	0 1	1 0	1 1
Short	0 ms	3 ms	8 ms	20 ms
Long	50 ms	150 ms	400 ms	1000 ms

Start/Stop Motion: Single Direction (\$2X, \$3X \$6X, \$7X)

When performing start/stop motion in one direction at a specified interval, the direction (forward/backward) is specified by SW1. The action time (short/long) is specified by SW3. The go-time is set by SW4/5; stop time is set by SW6/7.

For the block write mode, perform the command \$2X or \$3X after setting the mode as described below.

	Switch number											
0	1	2	3	4	5	6	7					
0	1:Backward	1	1:Long	Go time		Stop time	ime					
0	0:Forward	.	0:Short	GO time		Stop time						

Write Action (\$8X)

When writing or erasing to EOT with the tape continuously running:

- (1) Write or erase is specified by SW4.
- (2) Self-adjust gain control (SAGC) on or off when in the group coded recording (GCR) mode is specified by SW5.
- (3) High density or low density is specified by SW6.
- (4) Write density is specified under each density mode by SW7.

	Switch number											
0	1	2	3	4	5	6	7					
				1:Write	1:SAGC ON	1: High density	1:High					
1	0	0	0	0:Erase	0:SAGC OFF	0: Low density	0:Low					

Record density SW7	6250	1600	800	
1 : High	9042 fci	3200 fci	800 fci	
0 : Low	3014 fci	1600 fci	200 fci	

AGC/GSD Action (\$BX)

When performing the actions of SAGC (self adjust gain control) and GSD (gain step down after 1 block read/write) at a proper interval when the tape is written continuously at 9042 fci:

- (1) Stop at the error or no stop at error is specified by SW4.
- (2) Single or repeat is specified by SW5.
- (3) SAGC action or GSD-1 is specified by SW6.

	Switch number											
0	0 1 2 3 4 5 6 7											
4		4	4	1:Error stop	1:Single	1:GSD	_					
_		1		0:Non stop	0:Repeat	0:SAGC	U					

DGC AMP Action (\$CX, \$DX)

To set the count value of DGC AMP in the GCR mode:

- (1) Forward or backward is specified by SW3.
- (2) The count value is specified in hexadecimal notation by SW4 through SW7.

	Switch number											
0	0 1 2 3 4 5 6 7											
1	1		1:Backward	Count 8	Count 4	Count 2	Count 1					
	-		0:Forward	count 8	Count 4	Count 2	Count					

Mode Setting (\$EX)

When setting the mode of each MTU:

- (1) Write or read is specified by SW4.
- (2) Streaming or normal speed is specified by SW5.(3) High density or low density is specified by SW6.

	Switch number											
0	1	2	3	4	5	6	7					
1	4	4	0	1:Write	1:Streaming	1: High density						
	Δ.	1	0	0:Read	0:Normal	0: Low density	U					

Slice Level Setting (\$FX)

The slice level is specified by the combination of switches 5, 6, and 7. Settings for switches 5, 6, and 7 are further defined as follows:

Purpogo	Swite	ch nu	mber	R	ead	Write	Mode
Purpose	5	6	7	FWD	BWD	FWD	Mode
	1	1	1		125 <u>+</u> 12%		
	1	1	0		100 <u>+</u> 12%		Group
	1	0	1		80 <u>+</u> 8%		coded recording
Diagnosis	1	0	0		64 <u>+</u> 8%		(GCR)
	0	1	1		51 <u>+</u> 5%		or
	0	1	0		41 <u>+</u> 5%		Phase encode
Marginal	0	0	1	15 <u>+</u> 2%	10 <u>+</u> 1% 15 (AGCC or more)	37 <u>+</u> 4%	(PE)
Normal	0	0	0	10 <u>+</u> 1%	7 <u>+</u> 1% 10 (AGCC or more)	20 <u>+</u> 2% 25 (AGCC or more)	
Marginal	х	Х	1		26 <u>+</u> 4%	50 <u>+</u> 5%	MDZT
Normal	х	Х	0		17 <u>+</u> 2%	40 <u>+</u> 5%	NRZI

Note: "X" indicates that the switch setting at this position has no impact (commonly referred to as "don't care").

For adjustment of read amplifier, slice levels of 90%, 100%, and 110% are provided below. Each slice level can be adjusted by observing the signals of TMSR0 through 8 (select \$1E as a register address in the display mode).

To display register contents:

- (1) Set switches 0 through 7 as follows:
 - \$80 (displays the addressed register contents continuously.)
 - \$AO (displays the addressed register contents at the moment of running.)
 - \$CO (displays the addressed register contents at the time that the Unit Check signal [error] is generated.)

(2) Push CNT switch up (toggle) to display the addressed register contents are displayed.

SWO through 7 (Hexidecimal)	Contents
F9	Sets slice level at 90%.
FA	Sets slice level at 100%
FB	Sets slice level at 110%

Photo Sensor Check (\$9X)

Switch setting \$9X is used to check beginning (BOT), end of tape (EOT), error code indicator, and capstan tachometer. When checking the capstan tachometer, the motor can be rotated with a varying speed by setting SW5 on, even if a tachometer error is detected.

SW0 through 7 (Hexidecimal)	Contents
95	Used to check and adjust BOT/EOT and to check the error code indicator panel. (a) BOT and EOT signals are displayed at bits (Lamps) 4 and 5 of address \$14 of jump condition. (b) To check the MTU error code indicator front panel, the two digit display will increment as follows: 00 -> 11 -> 22 99 -> -> 00
98	Used to check duty and phase of the capstan tachometer. An error code is displayed in case of an error. In the case of error, setting SWO through 7 to \$9C causes the motor to rotate with a fixed voltage.
99	Used to check the capstan tachometer in high speed rotation. An error code is displayed in case of an error. In the case of error, setting SWO through 7 to \$9D will cause the motor to rotate with a fixed voltage.

Air System (\$AX)

This code is used to control the air system during maintenance actions.

	Switch number											
0	1	2	3	4	5	6	7					
1	0	1	0	0	1:Air drive	1:Solenoid valve drive	1:Pressure valve drive					
-	0		0	U	0:Off	0:Off	0:Off					

The \$AX code is also used to check and adjust the capacitive sensor.

	Switch number												
0	1	2	3	4	5	6	7						
1	O	1	0	1	0	1:Capstan drive	1:Backward						
_		.	0	<u> </u>	0	0: Coast	0:Forward						

In the check and adjustment of the capacitive sensor:

- (1) Set SWO through 7 to \$A8, stop the tape loop at the center of each column sensor, and adjust the reel.
- (2) Set SWO through 7 to \$AA or \$AB. Check by moving tape loops. \$AA causes the capstan to rotate the tape loop forward (without reel motion). \$AB causes the tape to rotate backwards (effectively adjusting the tape loops in the vacuum column without the file/machine servos [motors] being turned on). This procedure is especially useful during the tape loop detection checks.

Mechanism Action (\$BX)

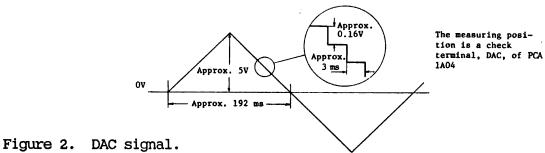
This command is used to control the cartridge, autocleaner, error marker, and window. These actions can be performed once (SW4 off) or repeatedly (SW4 on).

Table 3. Mechanism action.

SW0 through 7 (hexidecimal)	Contents
B1	Used to open cartridge.
B9	Used to repeat open and close of cartridge.
B2	Used to drive auto cleaner.
BA	Used to repeat on and off of auto cleaner.
B4	Used to drive error marker.
BC	Used to repeat on and off of error marker.
B6	Used to close window.
BE	Used to repeat open and close of window.
B7	Used to open cartridge, drive, auto cleaner, activate error marker and close window.
BE	Used to repeat B7 action.

Capstan Circuit Check (\$C0)

Confirm the action of capstan drive circuit by checking the DAC (D/A converter) signal.



- (1) Set switches 0 through 7 to \$CO, and check DAC.
- (2) If the DAC signal is a stepped waveform, as shown in Figure 2, the action is normal and no adjustment is required.

Reel Drive (\$DX)

Confirm the action of the reel motor drive circuit by rotating the reel motor clockwise or counterclockwise.

- Slow or fast is specified by SW4.
 Forward or backward is specified by SW5.
 SW6 specifies machine reel.
 SW7 selects the file reel.

	Switch number											
0	0 1 2 3 4 5 6 7											
1	1	0	4	1:Slow	1:Counter- clockwise		1:File reel drive					
<u> </u>	Τ.	U	1	0:Fast	0:Clockwise	0:Stop	0:Stop					

CONNECTION OF FIELD TESTER TO FMT

- (1) Open the front door of the FMT.
- (2) Connect the field tester to slot 1A08 of the FMT logic gate. (See PCA location chart in Part II.)
- (3) Perform the lamp test to verify that the lamps are operating properly. Set field tester switches SO through S7 to \$FO. Lamps LO through L11 should be on.

PERFORMING OFFLINE DIAGNOSTICS

The following conditions are required to perform offline diagnostics:

- (1) The MTU to be tested must be selected and placed in an online status.
- (2) A full reel of good-quality work tape (SRM 3200 or equivalent) with a file-protect ring must be used.
- (3) If interface cables between an FMT and controller are connected, the host controller power should be turned on. (Routine 00 runs all diagnostic program and is independent of the controller power status.)

Table C-1 in Section C of this Maintenance Manual is a list of offline diagnostics that can be performed with the field tester. This table lists all offline diagnostics routine numbers, names, and execution times. A more detailed description of the routines themselves are provided in Section C.5.

Follow these steps to initiate offline diagnostics:

- (1) Ensure that the field tester is connected to slot 1A08 of the FMT.
- (2) Set the ONL/OFL switch on field tester front panel to OFL.
- (3) Set field tester switches 0 through 7 to \$B2, and then toggle the CNT switch.
- (4) Set the field tester switches 0 through 7 to the routine number desired (\$XX), and then toggle the SSS switch. (See Table C-1 for routine numbers.)
- (5) Set switches to \$39 and toggle the SSS switch.
- (6) Set switches to \$B2 and toggle the CNT switch.
- (7) Set switches to \$00 and toggle the SSS switch. (Use \$01 for MTU #1. etc.)
- (8) Set switches to \$3E and toggle the SSS.
- (9) Set switches to \$A8 and toggle the CNT to start offline diagnostics.
- (10) Set switches to \$80 to set interface display mode.

While an offline diagnostic program is in progress, indicator lamp L1 on the field tester front panel remains on (lit). When the offline diagnostic is completed or is terminated for any reason and errors have been detected, lamp L8 will be lit. The routine number for which

the error was detected is stored in an FMT register. The error code is also stored. The error code and associated routine number can be accessed by the field tester to evaluate the error. (Corrective actions are described in Section C.4.)

To read the routine number and error code, follow these steps:

- (1) Set field tester switches S0 through S7 to \$35 and toggle CNT. The routine number (upper byte) is displayed in hexidecimal notation
- (2) Set field tester switches S0 through S7 to \$36 and toggle CNT. The error code (lower byte) is displayed in hexidecimal notation.

PERFORMING ONLINE DIAGNOSTICS

Online diagnostics are initiated using a "start-test" command from the host/controller. A summary of the routine numbers, names, and execution time is listed in table C-2 of Section C in this Maintenance Manual. All tests are run automatically when Test Magnetic Tape System (TMTS) is issued from the controller. TMTS is also commonly shown as Routine 00. 01. and "start test."

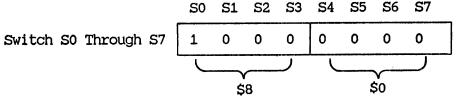
If the TMTS is successfully run, the MTS will not assert octal code 302, and the host/controller will know that the MTS is operational. Otherwise, 302 will be asserted, and routine and error code will be stored in hex notation in FMT registers \$2A and \$2B. The FMT registers can be accessed using the field tester. The routine number and associated error codes can be found in the Error Code Table (see Section C.4) and corrective action can then be implemented. The Error Code Table also lists the faulty printed circuit card (PCA) or subassembly that caused the error.

DISPLAY FUNCTIONS

This section explains the various field tester display functions in both online and offline modes of the FMT.

Display of Channel Interface Signals and Associated Signals

If switches S0 through S7 are set to \$80, the signals below are displayed on lamps LO through L11. \$80 means that 80 in the hexidecimal notation is to be set. Switches are '1' when they are ON (up) and '0' when they are OFF (down).



L11 L8 L9 L10 LO L1 L2 L3 L4 L5 L6 L7 Lamp LO Through TRAK SSC NSP B1600 ERRF ACMP PHLT PERR L11 START BUSY DXFO TREQ

START: Start signal

When this signal is active (LO lit), the FMT is selected by

the controller.

BUSY: Busy signal

When this signal is active (L1 lit), the FMT is connected to the controller and communication has been established.

DXFO: Data-Transfer-Out signal

> This signal indicates the data transfer direction between the FMT and controller. When this signal is active (L2 lit), it means data is transferred from the controller to

the FMT (Write operation).

TREQ: Transfer Request signal

This signal is active (L3 lit) when the FMT requests data.

Transfer Acknowledge signal TRAK:

This signal is active (L4 lit) when the controller acknowledges the data transfer request signal from the FMT.

SSC: Slave Status Change signal

This signal is active (L5 lit) when the FMT asserts SSC

signal.

NSP: Normal Speed Mode

This signal is active (L6 lit) when the FMT is in the normal

speed mode.

B1600:

1600 BPI signal

This signal is active (L7 lit) when the FMT is in the 1600

BPI mode.

ERRF:

Error Flag signal

This lamp informs operators of an error detected by the microprogram when the FMT is offline. This lamp also lights

when an error is detected during execution.

ACMP:

Address Compare signal

This signal is active (L9 lit) if the microprogram has passed the address specified by the SAD (stop address) register explained later. This signal can be reset by

toggling the SSS switch.

PHLT:

Processor Halt signal

This signal is active (L10 lit) when the microprocessor is

in a HALT status.

PERR:

Processor Error signal

This signal is active (L11 lit) if an erorr is detected in

the microprocessor hardware.

Display of Microprogram Registers (Register display)

If switch 0 is set to '0', the contents of any of the microprogram register whose address is specified by switches S1 through S7 is displayed on lamps L0 through L7. The latest register contents are played if the microprogram is pausing. If the microprocessor is running, the microprogram is interrupted as listed below and the contents at that moment are displayed

- When the CNT switch is ON.
- If the microprogram passes the stop address specified by the SAD register when executing the Address Compare Display operation.

S4 **S5** S6 S7 S0 S1 S2 S3 RAO RA1 RA2 RA3 RA4 RA5 RA6

Switch S0 Through S7

Sets the register address to be displayed

L7 L8 L9 L10 L11 LO L1 L2 L3 L4 L5 L6 REGO REG1 REG2 REG3 REG4 REG5 REG6 REG7

Display register contents

Display of Stop Address

If switches S0 through S7 are set to \$A0 and \$A1, the contents of the SAD register are displayed on L0 through L7.

			Sv	vita)						Disp	play				
S0	S1	S2	S3	S4	S 5	D6	S7	HEX	LO	L1	L2	L3	L4	L5	L6	L7
1	0	1	0	0	0	0	0	AO				SAX0	SADO	SAD1	SAD2	SAD3
1	0	1	0	0	0	0	1	A1	SAD4	SAD5	SAD6	SAD7	SAD8	SAD9	SAD10	SAD11

Display of Branch Address/Register Write Data

If switches SO through S7 are set to \$A2, the contents of the lower 5 bits of the branch address, or 8 bits of the register write data are displayed on L3 through L7.

\$A2

Switch	s	0 S1	S2	S3	S4	S 5	S 6	S 7
Setting	1	0	1	0	0	0	1	0

Display of Microprogram Address

If switches S0 through S7 are set to \$A4, the contents of the micro-program address (CAD 0 through 11) are displayed on L0 through L11.

\$A4

Switch	S0	S1	S2	S3	S4	S5	S 6	S 7
Setting	1	0	1	0	0	1	0	0

Display of Address Compare Control Flag

If switches S0 through S3 are set to \$C the status of the Address Commpare Flag is displayed on L4 through L7.

PART I.3 FIELD TESTER OPERATION WITH THE FMT

\$CX

Switch	S0	S1	S2	S3	S4	S5	S6	S 7
Setting	1	1	0	0	х	х	x	х

*X means don't care (the switch has no effect on operations)

\$CX

Lamp	LO	L1	L2	L3	L4	L5 I	.6 L7	
Indication	1	1	0	0	S.DAC	B.ADC	I.ADC	W.ADC

The indications

- S.DAC
- B.ADC
- I.ADC
- W.ADC

are defined below. See "Setting the Address Compare Flag."

Display of Microprogram Control Flag

If switches SO through S3 are set to \$EX, the status of the microprogram control flag is displayed on L4 through L7.

\$EX

Switch	S0	S1	S2	S 3	S4	S5	S 6	S 7
Setting	1	1	1	0	х	х	х	Х

Lamp	LO	L1	L2	L3	L4	L5	L6	L7
Indication	1	1	0	0	STEP	ROSF	SINH	SPARE

See "Control of Microprogram," for definitions of STEP, ROSF, SINH, and SPARE.

Lamp Test

If switches S0 through S3 are set to \$F, lamps L0 through L11 will light indicating that the lamps are operating properly.

EXECUTION OF OFFLINE COMMAND OPERATION

The field tester can allow the FMT to execute commands. Operation of the field tester for this function are described in the following paragraphs.

Write into the Microprogram Register

Any data can be written into any microprogram register as follows:

(1) Setting the Register Write mode

If switches \$0 - \$7\$ are set to \$B2 and the CNT switch is toggled, the Register Write mode is set.

(2) Setting of data to be written in the microprogram register

After setting to Register Write mode, data to be written is set by switches \$0 - \$7 and the SSS switch is toggled. Then by setting switches \$0 - \$7 to \$A2, write data as indicated on lamps L4 - L11.

(3) Write into the microprogram register is summarized below.

Switch Set Register \$7 \$1 \$2 \$3 \$4 \$5 \$6 Set Write Mode \$0 Write Mode 0 0 0 1 0 1 1 1 Ė 2

Toggle CNT switch

 Register Data
 \$0
 \$1
 \$2
 \$3
 \$4
 \$5
 \$6
 \$7

 RWD0
 RWD1
 RWD2
 RWD3
 RDW4
 RWD5
 RWD6
 RWD7

Data to be set in Register

Toggle SSS switch

Setting the Command Code

Using the Register Write function, any desired command code can be written into the Command Register whose register address is \$3D.

Setting the Device Address

Using the Register Write function, any desired Device Address can be written into the Device Address Register whose register address is \$3E.

Three bits (bits 5 through 7) of the register are used to set the device address in binary notations.

Bit 0 indicates SBCT (to be explained later).

Setting the Byte Count

Using the Register Write function, any desired Byte Count can be written into the Byte Count Register whose Register Address is \$3F.

The Byte Count value set by switches \$0 to \$7 changes weight depending on the bit 0 "\$BCT" of the register whose address is \$3E.

TABLE 4. Weight of byte count value

Switch Weight of Byte Count	\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7
\$BCT = True	2 ⁷	₂ 6	₂ 5	2 ⁴	23	22	21	2.0
\$BCT = False	2 ¹¹	210	2 ⁹	2 ⁸	27	26	2 ⁵	2 ⁴

Setting the Command Parameter

Any desired parameter can be set with the Register Write function.

Bit assignments of the microprogram registers whose register addresses are \$3C and \$3E are as follows:

TABLE 4. Command parameters

Reg. Name Address	0	1	2	3	4	5	6	7
Off-line Control \$3C	U.STP	UC.RP	UX.STP	UX.RW	UX.RV	RPOS	REPET	TUSCAN
Off-line Device Address \$3E	SBCT					DVA0	DVA1	DVA2

U.STP : UNIT CHECK, STOP

If Unit Check occurs during command execution, the microprogram stops after executing the command.

UC.RP : UNIT CHECK, REPOSITION

If Unit Check occurs during command execution, Repositioning is performed to retry the command after completing the command execution.

If UCK occurs during write command execution, Back Space and Erase operation is automatically performed.

UX.STP: UNIT EXCEPTION, STOP

If Unit Exception occurs curing command execution, the microprogram after executing the command.

UX.RW: UNIT EXCEPTION, REWIND

If Unit Exception occurs during command execution, Rewinding is done after completing the command execution.

UX.RV : UNIT EXCEPTION, REVERSE

This is valid for the Read and Read Bqackward commands. If a Tape mark is detected when executing a command, the tape running direction is reversed.

RPOS : REPOSITION

After executing the command, the tape is automatically repositioned to process the same block again.

REPET: REPEAT

The command is repeated as long as this bit is '1'. However, it is not generated if SINH (stop inhibit) bit is true.

TUSCAN: TAPE UNIT SCAN

If this bit is active, the device address is incremented after executing each command. After that, when a restart is indicated, the command is executed on the device whose address is the incremented value. If execution is impossible, the device address is increased until a device on which the command can be executed appears: When the device address becomes '8', the device address after increment is '0'.

SBCT : SMALL BYTE COUNT

This determines the weights of bits of the Byte Count used in the offline command control. Refer to MAP M0006 "Set of Byte Count."

Start of Command Execution

After performing the operations described above, if SINH bit is not active, the command is issued when the SSS switch is toggled. If the SINH bit is active, a command is not issued.

A command is executed once unless "REPET" is specified. After that, each time the SSS switch is toggled, the command is executed once. The result can be monitored using the function described in MAPs M0003 through M0005.

If "REPET" is specified, command execution starts when the SSS switch is toggled. The next command is automatically issued without toggling the SSS switch. This is valid as long as the SINH bit remains inactive.

Command execution can be stopped by setting the "REPET" bit to OFF.

Registers related to offline command execution are as follows: These registers are described later.

TABLE 5. Registers used when commands are issued in the offline mode:

	Offline Control	Offline Command	Offline Device	Offline Byte Count
Register Address	Address \$3C		\$3E	\$3F
Bit				·
0	U.STP	A	SBCT	A
1	UC.RP			
2	UX.STP	Command	RPSCY	Byte
3	UX.RW	Code	REVCY	Count
4	UX.RV		OFSCY	
5	RPOS		DVA0	
6	REPET		DVA1	
7	TUSCAN	₩	DVA2	▼

CONTROL OF MICROPROGRAM

Pause, single step, and address comparison of the microprogram can be executed from the field tester. These functions are explained in this section. Functions described in this section are valid regardless of the FMT condition (online or offline) and they are not reset when ONL/OFL is switched.

Specify/Release of Microprogram Control Function

After setting switches \$0 through \$3 to \$EX and setting the bits of switch \$4 through \$7, control functions of the microprogram are specified when the CNT switch is toggled. The lamps of the corresponding bits (L4 through L7) light.

	\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7
Switch \$0-\$7	1	1	1	0	STEP	ROSF	SINH	SP1

Toggle the CNT switch

STEP: Set to '1' to put the microprogram into the single step

mode. Single step is executed with the SSS switch.

ROSF : READ ONLY STORAGE FUNCTION

While this bit is active, data is continuously read from the control ROM in the microprocessor and is parity checked.

When any parity error occurs, the program stops at the address where the error was detected.

When this bit is active, commands in the offline mode are

inhibited.

START INHIBIT

SP1 : SPARE 1

Setting the Stop Address

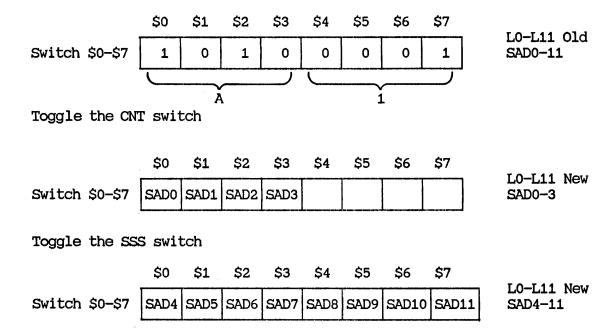
SINH :

(1) Setting the Stop Address Mode

If switches \$0 through \$7 are set to \$A1, the stop address at SAD0 to SAD11 is indicated on L0 through L11 (See "Display of Stop Address"). To change the stop address, set switches \$0 through \$7 to \$A1 and toggle the CNT switch.

(2) Setting the Stop Address

After setting Stop Address Mode, set the upper 4 bits of a stop address (SAD 0 through 3) on switches \$0 through \$3 and toggle the SSS switch. Then, set the lower 8 bits of the stop address (SAD 4 through 11) on switches \$0 through \$7 and toggle the SSS switch ON. The set stop address can be confirmed with the Stop Address Display function.



Toggle the SSS switch

(STOP ADDRESS Set complete)

Setting the Branch Address

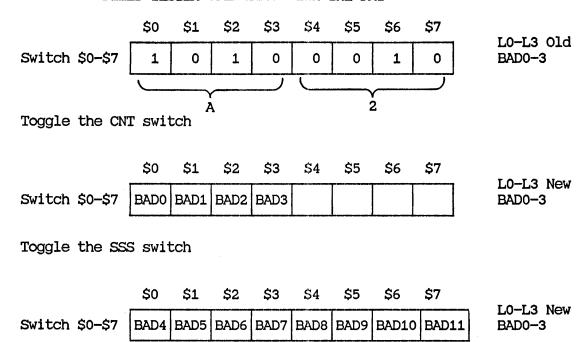
(1) Setting the Branch Address Mode

Set switches \$0 through \$7 to \$A2 and toggle the CNT switch.

(2) Setting the Branch Address

After setting the Branch Address Mode, set the upper 4 bits of the branch address on switches \$0 through \$3 and toggle the SSS switch. The Branch Address of the upper 4 bits set can be confirmed with the Branch Address Display function. The lower 8 bits of the branch address are set by switches \$0 through \$7. (The Branch Address Register is provided only for the upper 4 bits.)

PART I.3 FIELD TESTER OPERATION WITH THE FMT



(BRANCH ADDRESS set complete)

Setting the Microprogram Address

When the microprogram is in the step mode, the microprogram can be branched to a certain address from the field tester by changing the contents of the CS address register. After changing the CS address, if the program is single-stepped using the SSS switch, the program is executed from the changed address. If the step mode is released, the microprogram automatically starts from the changed address.

(1) Setting the Microprogram Address Mode

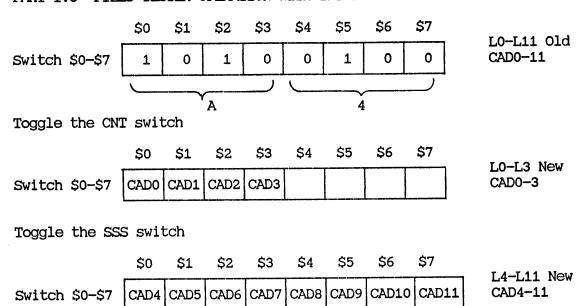
After setting the microprocessor into the Step Mode and setting switches \$0 through \$7 to \$A4, switches \$0 through \$7 are set to the CS address mode by toggling the CNT switch.

(2) Setting the CS Address Register

After setting Microprogram Address Mode, set the upper 4 bits of the CS address (CADO through 3) on switches \$0 through \$3 and toggle the SSS switch. Set the lower 8 bits of the CS address on switches \$0 through \$7 and the SSS switch.

The address can be confirmed using the Microprogram Address Display function.

PART I.3 FIELD TESTER OPERATION WITH THE FMT



(CS Address set complete)

Setting the Address Compare Control Flag

Set switches \$0 through \$3 to \$C and set the desired Address Compare Control Flag on \$4 through \$7. Then, toggle the CNT switch.

	\$0		—	• -	\$4		=	\$7
Switch \$0-\$7	1	1	0	0	s.ADC	B.ADC	I.ADC	W.ADC

Toggle the CNT switch

(Address Compare Control Flag Set complete)

S.ADC : STOP, ADDRESS COMPARE

When the address of the microprogram coincides with the address specified by the Stop Address Register, the microprogram stops.

B.ADC : BRANCH, ADDRESS COMPARE

When the microprogram coincides with the address specified by the Stop Address Register, the microprogram is forced to branch to the address indicated by the Branch Address Register and SWO through SW7.

I.ADC : INDICATE, ADDRESS COMPARE

When the microprogram coincides with the aaddress specified by the Stop Address Register, the contents of the register whose address is specified by SW1 through SW7 is displayed on L0 through L7.

W.ADC : WRITE, ADDRESS COMPARE

When the microprogram coincides with the address specified by the Stop Address Register, the contents of the RWD (Register Write Data) register is written into the register whose address is specified by SW1 through SW7.

LAMP TEST/SYSTEM RESET

If switches \$0 through \$3 are set to \$F, lamps L0 through L11 turn ON. Also, System Reset is performed if the CNT switch is toggled.

Note: Since System Reset affects the Microprogram Control function depending on conditions of \$4 through \$7, exercise caution.

OFFLINE COMMAND EXECUTION PARAMETERS

Reg. Name Address	0	1	2	3	4	5	6	7
Off-line Control \$3C	U.STP	UC.RP	UX.STP	UX.RW	UX.RV	RPOS	REPET	TUSCAN
Off-line Device Address \$3E	SBCT					DVA0	DVA1	DVA2

(1) SDIAO through SDIA3 are the same as the 4 byte diagnostic flag (listed below).

SDIA0 (address \$38)
SDIA1 (address \$39)
Diagnostic flag bytes
SDIA2 (address \$3A)

SDIA3 (address \$3B)

When FMT is in offline status and if diagnostic flag bytes are set directly in these registers (without executing the above commands), the specified diagnostic operation can be performed by executing the command operation (without chaining to SDIA command). The SDIA data once set will not be altered until the FMT is set to the online status or to system reset.

(2) Tape Unit Scan

When the OFCNTL register TUSCAN byte is set '1', the OFLDVA register (OFDVAO through 6 byte data) is advanced by 1. If the repeat bit has also been set '1', commands are issued serially to all MTUs.

(3) REPEAT

When the OFLCNT register REPEAT bit is reset ('0'), a command is executed whenever the SSS switch is toggled.

If the REPEAT bit is '1', the command activated by SSS switch is repeated continuously. In this case, all the functions specified by other bits are valid.

(4) Reposition

The following offline repositioning operations are performed when the OFLCNT register RPS bit is set. The commands and addresses entered in OFLCMD and OFLDVAO through 2 remain unchanged after offline repositioning is complete.

TABLE 6. Offline reposition.

Commands set in OFLCMD register	Offline Reposition Operation
\$01 (Write)	Back space command is executed after a Write Command. However if IDBSK (ID Burst check) at sense byte 5 bit 3 or SAGC (byte8, bit4) is activated, the Rewind Command will be executed instead of the Back Space Command.
\$02 (Read)	Back Space Command follows the Read Command. However, if NCAP (Not capable) has occurred, the Rewind Command will be executed.
\$0C (Backward Read)	Space Command follows the Backward Read Command.
Other Commands	No operation.

(5) UEX Function

The following operation is executed when UEX bit is included in the END status by using combinations of STP, UEX, REW, UEX, REV.UEX in OFLCNT register.

TABLE 7. UEX functions.

STP .UEX	REW .UEX	REV .UEX	UEX Function Description
1	Х	х	Processing is looped within the offline service routine from the time UEX bit is turned on till STP.UEX bit is reset '0' or SINH is specified.
0	0	0	No operation (UEX bit is not checked)
0	0	1	When UEX bit is set '1' the OFLCMD register command codes are replaced by Reverse Commands as follows: Old OFLCMD -> New OFLCMD WT(\$01) -> BRD(\$0C) RD(\$02) -> BRD(\$0C) BRD(\$0C) -> RD(\$02) SP(\$37) -> BSP(\$27) BSP(\$27) -> SP(\$37) ERS(\$17) -> BRD(\$0C) WTM(\$1F) -> BSPF(\$2F) DSE(\$97) -> BSPF(\$2F) NOP(\$03) -> BRD(\$0C) Others -> Not changed
0	1	0	Rewind Command is issued when UEX bit is set "1".
0	1	1	Rewinds MTU by issuing a rewind command when UEX bit is set ('1'). At this stage the MTUs are reversed from normal speed to high speed or from high speed mode to normal speed.

(6) UCK Function

If UCK bit is included in End Status, the operations shown in Table 8 are performed. The operations are specified by combinations of the STP.UCK, RPS.UCK bits. ERERF lamp is turned ON when the UCK bit is set '1' (Errors exist when the lamp is ON).

TABLE 8. UCK functions.

STP .UCK	RPS .UCK	UCK Function Description
0	0	UCK bit is not checked.
0	1	The repositioning operation described in step (4) is executed when the UCK bit is set ('1'). Any errors in this operation are ignored (UCK).
1	0	Processing is looped within the offline service route from the time UCK bit is set ('1') until STP.UCK bit is reset or SINH is asserted.
1	1	The repositioning operation in (4) is executed when the UCK bit is set. Any new errors (UCK) during repositioning operation are looped in the offline service routine until STP.UCK bit is reset '0' or SINH is asserted.

(7) SINH (Start Inhibit)

When SINH bit on the field tester is asserted, commands from SSS switch are inhibited.

A loop created by STP.UCK or STP.UEX bits may be released by setting the SINH bit. (If SINH is turned OFF again, commands will again be issued (if REPEAT is active).

Commands are temporarily inhibited if SINH bit is set (ON) when REPEAT has been specified. This facilitates temporary stopping or starting of commands in manual mode.

OPERATIONAL FUNCTIONS OF THE FIELD TESTER

Table 9 lists various functions of field tester operation. Examples of field tester operation are described after Table 9. Expressions used in the examples are as follows:

- (a) Expression \$0F indicates that \$0 through \$7 are to be set to a hexadecimal 0F, and expression \$0F CNT indicates that after \$0 through \$7 are set to \$0F, the switch CNT is toggled.
- (b) Similarly, expression \$3B SSS indicates that \$0 through \$7 are set to a hexadecimal 3B and switch SSS is toggled.
- (c) Expression "ONL/OFL = ONL" indicates that the switch field tester ONL/OFL is set to the ONL position.
- (d) Accordingly, expression "ONL/OFL = OFL" indicates that this switch is set to the OFL position.
- (e) The practical examples given are for maintenance, and do not explain all functions listed in Table 9.

TABLE 9. Operational functions of the field tester.

Item				Swite	ħ				**	0-4					-		Dis	play					
105"	\$Ø	\$1	\$2	\$3	\$4	\$ 5	\$6	\$7	Hex. code	Set. key		LØ	IJ	L2	L3	L4	1.5	L6	L7	L8	LĐ	LIØ	Ш
1	Ø	RAØ	RAI	RA2	RA3	RA4	RA5	RA6	ØØ7F	_	Register display	REG Ø	REG 1	REG 2	REG 3	REG 4	REG 5	REG 6	REG 7				
2	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	80	-	Interface signal S display		Œ	DXFO	RQIA	RIA	DXRQ	MCY	B160	ERRF	ACMP	PHLT	PERR
3	1	Ø	1	Ø	Ø	Ø	Ø	1	Al	_	Stop address display	SAD	620	CND	CND CND	- CAD	CAD	CAT	GND	90	SAD 9	975	ann.
	1	Ø	1	Ø	Ø	Ø	Ø	1	Al	CML	Stop address mode	ø	SAD 1	SAD 2	SAD 3	SAD 4	SAD 5	SAD 6	SAD 7	SAD 8		SAD 10	SAD 11
	SAD Ø	SAD 1	SAD 2	SAD 3		-	_	_	xx	SSS	Set upper SAD												
	SAD 4	SAD 5	SAD 6	SAD 7	SAD 8	SAD 9	SAD 10	SAD 11	ХX	SSS	Set lower SAD												
4	1	Ø	1	Ø	Ø	Ø	1	Ø	A2	_	Branch address												
	1	Ø	1	Ø	Ø	Ø	1	Ø	A2	CNT	display Branch address mode	BAD	BĄD	BAD	BAD BAD	RWD	RWD	RWD	RWD	RWD		RWD	RWD
	BAD Ø	BAD 1	BAD 2	BAD 3					xx	SSS	Set upper BAD	Ø	1	2	3	Ø	1	2	3	4	5	6	7
	BAD 4	BAD 5	BAD 6	BAD 7	BAD 8	BAD 9	BAD 10	BAD 11	xx	—	Set lower BAD												
5	1	Ø	1	Ø	Ø	1	Ø	Ø	A4		CS address display												
	1	Ø	1	Ø	Ø	1	Ø	Ø	A4	ONT	CS address mode	CAD	CAD	CAD 2	CAD 3	CAD	CAD 5	CAD	CAD 7	CAD 8	CAD	CAD 19	CAD 11
	CAD	CAD 1	CAD 2	CAD 3					xx	SSS	Set upper CAD	Ø	1	2	3	4	5	6	7	8	9	10	11
	CAD 4	CAD 5	CAD 6	CAD 7	CAD 8	CAD 9	CAD 1Ø	CAD 11	ХX	SSS	Set lower CAD												
6	1	Ø	1	1	Ø	Ø	1	Ø	B2	_	Register write												
	1	Ø	1	1	Ø	Ø	1	Ø	B2	ONT	display Register write mode	BAD	BAD	BAD	BAD 3	RWD	RWD	RWD	RWD	RWD		FWD.	RWD
	RWD Ø	RWD 1	RWD 2	RWD 3	RWD 4	RWD 5	RWD 6	RWD 7	ХX	SSS	Register write data	Ø	1	2	3	Ø	1	2	3	4	5	6	7
		RAØ	RAL	RA2	RA3	RA4	RA5	RA6	хх	SSS	Register addess												1
7	1	1	Ø	Ø	S. ADC	B. ADC	I. ADC	W. ADC	СХ	CML	Address compare con- trol & display	\$Ø	\$1	\$2	\$3	S. ADC	B. ADC	I. ADC	W. ADC				
8	1	1	1	Ø	STEP	ROSF	SINH	SP2	EX	CNT	MP control RSL & display	\$Ø	\$1	\$2	\$3	STEP	ROSF	SP1	SP2				
9	1	1	1	1					FX		Lamp test	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	STEP	ROSF	SINH	SP2	FX	CNT	System reset & MP control	1	1	1	1	1	1	1	1	1	1	1	1

REGISTER DISPLAY MODE

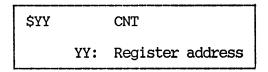
The FMT microprocessor accomplishes predetermined operations through the control of 104-byte register (out of which 64 bytes are used for the RAM). See Table 10 for a list of FMT registers. Using a field tester, the contents of these registers can be displayed at any time.

The procedure to display the register contents is to set \$0 through \$7 and toggle the CNT switch.

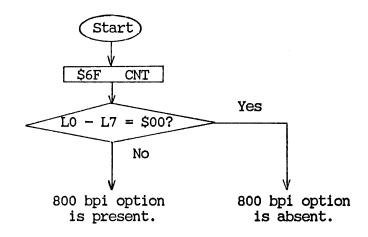
If the microprocessor is in the halt status, the register contents will be displayed when switches \$0 through \$7 are set. If the microprocessor program is running, the CNT switch must be toggled after setting \$0 through \$7.

When the microprocessor in the FMT is set in the STEP or halt status, the PHLT bit (L10 when \$0 through \$7 are set to \$80) lights.

Register display:



For example, use Table 10 to check for the presence or absence of 800. The 800 bpi option PCA is installed in slot 1A01 of the FMT. To check whether the 800 bpi option is present, display the contents of register address \$6F (ZOP register) as follows:

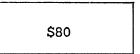


4		0																
			1	2	3	4	5	6	7	8	9	A	В	С	D	E	F	
Nickname	10	DVENQO BINOO	DVENQ1	DVENQ2	DVENQ3	DVENQ4	DV ENQ5	DVENQ6	DV ENQ7	SCMD	SCANP	DSB	LCMD	DVSO	DVS1	DVS3	DVS8	W(-1
	10-	SINQO	BINQ1	BINQ2	BINQ3	BINQ4	BINQ5	BINQ6	BINQ7	DS0	SAMEADR		+	BWD	EXTF	VELO	HERS	Nicknam
l	1	DINOO	SINQL	SINQ2	SINQ3	SINQ4	SINQ5	SINQ6	SINQ7	DS1	TIESEQ		LAST	NFP	RSTK	VELL	HACT	1
	14	SSCMO	DINQI	DINQ2	DINQ3	DINQ4	DINQ5	DINQ6	DINQ7	1	TACHSEQ		MCY-CMD CODE		DSE	RHLD/STRF		+ 1/2
0	1	USEMO	USEAT	SSCM2 USEM2	SSCM3	SSCM4	SSCM5	SSCM6	SSCM7	CMDE	LWRFH	BSY		BOT	7TRK	SKIPF		1 3 .
	15	ONLMI	ONLM2	ONLH2	USEM3	USEM4	USEM5	USEM6	USEM7	CHD0		CHE		WRS	TEST	611		-2 0
	1	OMAIL	ORLEIZ	UNLAZ	ONLM3	ONLM4	ONLM5	ONLM6	ONLM7	CMD1	DVAO	DVE		ONL	DUAL	613		3
1	7	RDYMO	RDYM1	RDYM2	RDYM3	RDYM4				CMD2	DVA1	UCK		TUC	HID	615	H1600	6
Nickname		WO	W1	W2	W3	W4	RDYM5	RDYM6	RDYM7	CMD3	DVA2	UEX		RDY	6250TU	616	TM	7
	10				7.7	1 114	W5	W6	W7	MCYENT	CMDSEQ	SUBO	SUB1	Q0	QI	YO	YI	Nickname
	1				 				 	LNGCRS	LIBGF						+	01
i	2							 		NTRTIME	NOCK						1	ī
1	3								 	STRMM	LWR RW						1	2
1 -	4									STRMFLG WRT.OP	XFROP							3 1
	5									SKP.OP	CMCODE0 CMCODE1							4
1	6								 	BC0	CMCODE2		· · · · · · · · · · · · · · · · · · ·				,	5
	7								 	BC1	CMCODE3							6
Nickname	2	SB0	SB1	SB2	SB3	SB4	SB5	SB8	SB9	SBIO	SB11	SB22	CD22					7
	0		NOIS	ET0	VRC	MPHE		IBGD	102CR	STRJ	RWTO	-	SB23	RO	R1	CMD	DVA	Nickname
!	1	IRQ		ET1	MLT/LRC	RJTU		ET8	VLCG	CMRJ	MISP	 	- 					0
l	2	BOC		ET2	SKW	TI	WIMCK		XFBC	CTRJ	TAGIC	FRU-1	FRU-2	DOCT.	1 1			1
2	3	EQC	TOVR	ET3	EDC/CRC	WTVRC	IDBCK	EBRC	CRC 3	NBLK	REGE	1	1.40-4	POSI COUNT		MCY .		2
_	4	DCK	BOT	ET4	ENVC		STRDC	SAGC		DYRV	DMPE	 	 	UPPER	LOWER	CMD		3 2
	12	OVRN	WRS	ET5	1600	LWR TYPEOP	PREC	SBRC		TCSF	ROME	 		UFFER	TUMER	CODE		141
	10	WCZ CNCTD	FP	ET6	BWD	TUC	POSAE	SERC		(SRJF)	MPTRP	 			 		DVAO	5
Nickname	11	SNSPD RJC	NCAP RWE	ET7	PCMP	WCALM	WECOVF	VLRY		VLCK	TUROM	 						6
DICKRAME	10	RJC7	WIMCK		RTRY	SNSCNT	Y2	Y3	LDVA	SDIAO	SDIAL	SDIA2	SDIA3	OFLENT	OFLCID	OFLDVA	BCT	7
l	1	RJC6	UCE	DTP CRC		 	 			DMW/DMR	LWP TUIF			UCK.STP	DSO	*16BY		0
1	13	RJC5	PREC	**0**						MARG	INV	MASKO-7	GDT 8-F	UCK.REP		RUM		+ 11
3	3	RJC4	MLTE	WRS			 			IHPS/XFR			(LOW)	UEX.STP		(RPSCY)		2
•	4	RJC3	MISC	4P	 		 			GDT		MRG CODE		UEX.REW	CMDE	(REVCY)		3
1	5	RJC2	EDC	5P			 			IHPR/MARA		0-7		UEX.REV	CMDO	(OFSCY)		3
!	6	RJC1	VELCNG	67				 		LWR RW	MASKP			RROS	CMD1	OFLDVAO		3
	7	RJC0		7P				 	ļ'	MASK		GDT 0-7		REPEAT	CMD2	OFLDVAL		6
Nickname		-	-		-		-			TMTC		(UP)		TUSCAN	CMD3	OFLDVAZ		7
	0								 	<u> </u>	-	-		-	-	-	 -	Nickname
	1								 									0
	2																	1
	3								 									2
•	4											ļi						3 ,
	5							· ·				<u> </u>						[4]
	6																	5
	17	<u></u>		,														
Nickname		EXX0						١,	1									6
	0		EMX1	EMX2	EMX3	EMX4	EXS	E4X6	EMX7	CMR	ADR	FCIIST	THET					7
		*DT7	*WTHCK	*RJC7	*TI	*EMX47	*EMXS7	EMX6 *EMX67	EMX7 *EMX77	CMR DSQ	ADR TRAK	FCUST		SIF	BUS	XCTL	XSNS	6 7 Nickname
1	1	*DT6	*WTHCK *UCE	*RJC7 *RJC6	*TI *BOT	*EMX47 *EMX46	*EMX57 *EMX56		*EMX77	CMR DS0 DS1	TRAK	IDBST	HDENS	TULHT	BIO(A)/BOO	DXFI	XSNS 16TH/*ABPE	7 Nickname
1	2	*DT6 *DT5	*UTHCK *UCE *PREC	*RJC7 *RJC6 *RJC5	*TI *BOT *NSP	*EMX47 *EMX46 *EMX45	*EMX57 *EMX56 *EMX55	*EMX67 *EMX66 *EMX65	*EMX77 *EMX76 *EMX75	DSO		IDBST	HDENS FPOS	TULHT IRECV	BIO(A)/BOO BIL(*B)/BO1	DXFI DXFO	XSNS 16TH/*ABPE SETBC/BLKE	7 Nickname
5	3	*DT6 *DT5 *DT4	*WTHCK *UCE *PREC *MLTE	*RJC7 *RJC6 *RJC5 *RJC4	*TI *BOT *NSP *FP	*EMX47 *EMX46 *EMX45 *EMX44	*EMX57 *EMX56 *EMX55 *EMX54	*EMX67 *EMX66 *EMX65 *EMX64	*EMX77 *EMX76 *EMX75 *EMX74	DSO DS1	TRAK R.BPE/BUSPE	IDBST TMS	HDENS FPOS EOTS	TULHT IRECV ENDAT	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2	DXFI DXFO RECV	XSNS 16TH/*ABPE SETBC/BLKE DXFE	6
5	3	*DT6 *DT5 *DT4 *DT3	*WTHCK *UCE *PREC *MLTE *MISC	*RJC7 *RJC6 *RJC5 *RJC4 *RJC3	*TI *BOT *NSP *FP *BWD	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43	*EMX57 *EMX56 *EMX55 *EMX54 *EMX53	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63	*EMX77 *EMX76 *EMX75 *EMX74 *EMX73	DSO DS1 START	TRAK R.BPE/BUSPE SLX2	IDBST TMS OVEN	HDENS FPOS EOTS BOTS	TULHT IRECV ENDAT TUSMP	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2 BI3/BO3	DXFI DXFO RECV MTREQ/TREQ	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP	6 7 Nickname 0 1 2 3 4
5	3	*DT6 *DT5 *DT4 *DT3 *DT2	*WTHCK *UCE *PREC *MILTE *MISC *EDC	*RIC7 *RIC6 *RIC5 *RIC4 *RIC3 *RIC2	*TI *BOT *NSP *FP *BWD *HD	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42	*EMXS7 *EMX56 *EMX55 *EMX54 *EMX53 *EMX53	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62	*EMX77 *EMX76 *EMX75 *EMX74 *EMX73 *EMX72	DSO DS1 START CMDE CMD0 CMD1	TRAK R.BPE/BUSPE SLX2 SLX1	IDBST TMS OVRN CRERR	HDENS FPOS EOTS BOTS WRTS	TULHT IRECV ENDAT TUSMP EMXPSL	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2 BI3/BO3 BI4/BO4	DXF1 DXF0 RECV MTREQ/TREQ BLOCK	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP REWS	6 7 Nickname 0 1 2 3 4 5
5	3	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1	*WTHCK *UCE *PREC *MILTE *MISC *EDC *VELCNG	*RJC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC1	*TI *BOT *NSP *FP *BWD *HD *RDY	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX41	*EMXS 7 *EMXS 6 *EMXS 5 *EMXS 4 *EMXS 3 *EMXS 2 *EMXS 2 *EMXS 2	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX62	*EPOC77 *EMX76 *EMX75 *EMX74 *EMX74 *EMX73 *EHX72 *EHX72	DSO DS1 START CMDE CMD0 CMD1 CMD2	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1	IDBST TMS OVEN CREER DCK REJECT SSC	HDENS FPOS EOTS BOTS WRTS ONLS	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2	BIO(A)/BOO BI1(*B)/BO1 BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP REWS AROBR	6
	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP	*WTHCK *UCE *PREC *MLTE *MISC *EDC *VELCNG *DIAGL/*CRC	*RJC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC2 *RJC1 *RJC0/"0"	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX41 EMX40/EMX4P	*EMXS 7 *EMXS 6 *EMXS 5 *EMXS 4 *EMXS 3 *EMXS 2 *EMXS 2 *EMXS 1 EMXS 0/EMXS P	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 EMX60/EMX6P	*EMX77 *EMX76 *EMX75 *EMX74 *EMX73 *EMX72 *EMX71 EMX70/EMX7P	DSO DS1 START CMDE CMDO CMD1 CMD2 CMD3	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2	IDBST TMS OVEN CREER DCK REJECT	HDENS FPOS EOTS BOTS WRTS ONLS NRZI	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2 DVAMPX1	BIO(A)/BOO BI1(*B)/BO1 BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP FEWS AROBR BIBSY	Nickname 0 1 2 3 5 6
5 Nickname	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK	*WTHCK *UCE *PREC *MILTE *MISC *EDC *VELCNG *DIAGL/*CRC DACTL	*RJC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC1 *RJC0/"0# WTCTL	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS RDCTL	*EMX47 *EMX46 *EMX45 *EMX45 *EMX44 *EMX43 *EMX42 *EMX41 EMX40/EMX4P MODE	*EMX57 *EMX56 *EMX55 *EMX54 *EMX53 *EMX52 *EMX52 *EMX51 EMX50/EMX5P RDSNS	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 EMX60/EMX6P CRCST	*EMX77 *EMX76 *EMX75 *EMX74 *EMX73 *EMX72 *EMX72 *EMX71 EMX70/EMX7P FMERR	DSO DS1 START CMDE CMDO CMD1 CMD2 CMD3 TSMS	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT	IDBST TMS OVEN CREER DCK REJECT SSC	HDENS FPOS EOTS BOTS WRTS ONLS NRZI	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6 BI7/BO7	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP EEUS AROBR BIBSY SCNP	Nickname Nickname 1 2 3 4 5 6 7
	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK MASKO	*WTHCK *UCE *PREC *MLTE *MISC *EDC *VELCNG *DIAGL/*CRC DACTL DMW	*RIC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC1 *RJC0/"0" WTCTL WTM	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS RDCTL ROK	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX41 EMX40/EMX4P HODE HOCY	*EMX57 *EMX56 *EMX55 *EMX54 *EMX53 *EMX52 *EMX51 EMX50/EMX5P RDSNS HN01S	*ENX67 *ENX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX62 *EMX61 ENX60/ENX6P CRGST *MCRC	*ENX77 *EMX76 *ENX75 *ENX74 *ENX74 *ENX73 *ENX72 *ENX71 ENX70/ENX7P PHERR *STRDC	DSO DS1 START CMDE CMD0 CMD1 CMD2 CMD3 TSNS *TSNSO	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT *DET0	IDBST THS OVEN CREER DCK REJECT SSC BUSY BLENT *102CR	HDENS FPOS EOTS BOTS WATS ONLS NRZI RDYS RDERR AVRCE	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2 DVAMPX1 DVAMPX0 2ETK ETKO	BIO(A)/BOO BI1(*B)/BO1 BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRG	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP EEUS AROBR BIBSY SCMP ZOP	Nickname
	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK	*WTHCK *UCE *PREC *PREC *MISC *MISC *EDC *VELCNG *DIAGL/*CRC DACTL DMW DMW	*RIC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC1 *RJC0/"0" WTCTL WTM IBW	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS RDCTL ROK STPHK	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX41 EMX40/EMX4P HODE HCY BUD	*EMX57 *EMX56 *EMX56 *EMX54 *EMX53 *EMX52 *EMX51 EMX50/EMX5P RDSNS HNOIS HBLK	*ENX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 EMX60/EMX6P CRCST *MCRC	*EMX77 *EMX76 *EMX76 *EMX75 *EMX74 *EMX73 *EMX73 *EMX72 *EMX71 EMX70/EMX7P FMERR *STRDC *EDC	DSO DS1 START CMDE CMD0 CMD1 CMD2 CMD3 TSNS *TSNSO *TSNS1	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT *DET0 *DET1	IDBST TMS OVRN CRERR DCK REJECT SSC BUSY BLFNT *102CR *DET8	HDENS FPOS EOTS BOTS WRTS ONLS NRZI RDYS RDERR	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2 DVAMPX1 DVAMPX0 2ETK ETKO	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6 BI7/BO7 ZCTL SFCRC	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC *NVRCE	XSNS 16TH/*ABPE SETBC/BLKE DXFB STOP REMS AROBR BIBSY SCMP ZOP +	6
Nickname	3 4 5 6 7	*DT6 *DT5 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK MASK0 MASK1	*WTHCK *UCE *PREC *PREC *MITE *MISC *EDC *VELONG *DIAGL/*CRC DACTL DMW DMR THPRE	*RIC7 *RIC6 *RIC6 *RIC5 *RIC4 *RIC3 *RIC2 *RIC1 *RIC0/"0" WTCTL WTM WEC	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS RDCTL ROK STPHK VFOS	*EMX47 *ENX46 *EMX45 *EMX44 *EMX43 *EMX43 *EMX41 EMX40/EMX4P MODE MCX BWD WRS	*EMX57 *EMX56 *EMX55 *EMX54 *EMX53 *EMX53 *EMX51 EMX50/EMX51 EMX50/EMX5P RDSNS RNO1S HBLK HTM	*ENX67 *ENX66 *ENX65 *ENX64 *ENX62 *ENX62 *ENX61 ENX60/ENX6P CRCST *MCRC *MCRCZ *EP=CR	*EMX.77 *EMX.76 *EMX.75 *EMX.74 *EMX.73 *EMX.73 *EMX.71 EMX.71 EMX.71 EMX.71 EMX.72 *EMX.71 EMX.72 *EMX.71 EMX.73 *EMX.71 EMX.73 *EMX.71 EMX.71 EMX.7	DSO DS1 START CHIDE CMDO CMD1 CMD2 CHD3 TSNS *TSNS0 *TSNS0 *TSNS1 *TSNS1	TRAK R.BPE/BUSPE SLX2 SLX0 TUAD2 TUAD2 TUAD1 TUAD0 POINT *DET0 *DET1 *DET2	IDBST THS OVERN CREER DCK REJECT SSC BUSY #102CR *DETB *TSNS8	HDENS FPOS EOTS BOTS WRTS ONLS NRZI RDYS RDERR 4VRCE *MLTE/*LRCE *SKEWE	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2 DVAMPX1 DVAMPX0 2ETK ETKO	BIO(A)/BOO BII(*B)/BOI BI2(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6 BI7/BO7 ZCTL SFCRC	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRG *MVRCE ETK8	XSNS 16TH/*ABPE SETBC/BLKE DXPE STOP REWS AROBR BIBSY SCMP ZOP + 800	0
	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK MASKO MASKI MASK2	*WTHCK *UCE *PREC *PREC *MITE *MISC *EDC *VELCNG *DACTI. DMW DMR IHPRE IHPOS	*RJC7 *RJC6 *RJC5 *RJC4 *RJC3 *RJC2 *RJC1 *RJC0/"0" WTCTL WTM IBW WEC ALIWT	*TI *BOT *NSP *FP *BWD *HD *RDY *OVL/*WRS RDCTL ROK STPHK STPHK IHDXF	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX42 *EMX41 EMX40/EMX4P MODE MCY B&D WRS ZRD	*EMX57 *EMX56 *EMX55 *EMX54 *EMX54 *EMX52 *EMX52 *EMX51 EXX50/EMX5P RDSNS HNO1S HRO1S HRM WIND	*EMK67 *EMK66 *EMK65 *EMK64 *EMK63 *EMK64 *EMK62 *EMK62 *EMK61 EMK60/EMK6P CRCST *MCRCZ *MCRCZ *EP~CR *B~D	*ENC77 *ENK76 *ENK75 *ENK75 *ENK74 *ENK74 *ENK72 *ENK72 *ENK71 ENK70/ENK7P FMERR *STRDQ *EDC *SLIPC *MOISC	DSO DS1 START CMDE CMDD CMD1 CMD2 CMD3 TSMS *TSMS0 *TSMS1 *TSMS2 *TSMS2	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT *DET1 *DET1 *DET2	IDBST TMS OVRN CREER DCK REJECT SSS BUSY BLFNT *102CR *DETB *TSNS8 *DIBG	HDENS FPOS EOTS BOTS WATS ONLS NRZI RDYS RDERR *VRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMXPSL DVAMPX2 DVAMPX1 DVAMPX0 ETKO ETK1	BIO (A)/BOO BII (*B)/BOI BI2 (SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6 BI7/BO7 ZCTL SFCRC LRC	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC *NVRCE ETX8 *NSKWE	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP REMS AROBR BIBSY SCMP ZOP + 800 OPTION	6 7 Nickname U 1 2 3 4 5 5 6 7 Nickname O 1 1 2 2
Nickname	3 4 5 6 7	*DT6 *DT5 *DT5 *DT3 *DT2 *DT1 *DT1 *DT0/*DTP MASK MASKO MASKI MASKI MASK2 MASK3	*WTHCK *UCE *PREC *PREC *MITE *MISC *EDC *VELONG *DIAGL/*CRC DACTL DMW DMR THPRE	*RIC7 *RIC6 *RIC5 *RIC4 *RIC3 *RIC2 *RIC2 *RIC1 *RIC0/"0" WICTL WITH IBM WEC ALIUT WOK	*TI *BOT *MNSP *MNSP *FP *BWD **HD **RDY *OVL/*WRS RDCTL ROK STPHK VFOS IHDXF IHCOR	*EHX47 *EHX46 *EHX45 *EHX44 *EHX44 *EHX43 *EHX42 *EHX41 EHX40/EHX4P HODE HCY BAD WRS ZRD 6250	*EMX57 *EMX56 *EMX55 *EMX55 *EMX54 *EMX53 *EMX52 *EMX52 *EMX51 EMX50/EMX5P RDSNS HND01S HBLK HTM HTND PHOK	*ENX67 *ENX66 *ENX65 *ENX64 *ENX63 *ENX62 *ENX62 *ENX60/ENX6P CRCST *MCRC *MCRC *MCRC *ENC8 *MCRC *MCRC *ENC8 *ENC	#EPC77 #EM76 #EM75 #EM75 #EM74 #EM73 #EM73 #EM71 EM70/EM7P FMERR #STRDC #SLIPC #NOISC #W80C	DS0 DS1 DS1 DS1 START CMDE CMD0 CMD1 CMD1 CMD2 CMD3 TSNS *TSNS0 *TSNS1 *TSNS1 *TSNS2 *TSNS3 *TSNS3	TZAK R. BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT *DET0 *DET1 *DET1 *DET2 *DET3 *DET4	IDBST TMS OVEN CRERE DCK REJECT SSC BUSY BLFNT *102CR *TSNS8 *TSNS8 *DIBG *DNOIS	HDENS FPOS EOTS BOTS WRTS ONLS NRZI RDYS RDERR *VRCE *MILTE/*LRCE *SKEWE *DBCK *DBCK	TULHT IRECV ENDAT TUSMP EMXPSI DVAMPX2 DVAMPX1 DVAMPX0 2ETK ETK0 ETK1 ETK2	BIO (A) / BOO BII (*B) / BOO BII (*B) / BOO BIZ (SDI) / BOO BIZ / BOO BIJ /	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRG *MVRCE ETK8	XSNS 16TH/*ABPE SSTBC/BLKE DXFE STOP REWS AROBR BIBSY SCMP ZOP † 800 OPTION	6 7 Nickname 0 1 2 3 5 6 7 7 Nickname 0 1 2 2 3 6 1 1 1 1 1 1 1 1 1
Nickname	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT0/*DTP MASK MASKO MASKI MASK2 MASK3 MASK3	*WTHCK *UCE *PPEC *MITE *MISC *EDC *MULTE *MISC *EDC *DIAGL/*CRO DACTL DMW DMR THPRE 1HPOS	*RJC7 *RJC6 *RJC6 *RJC3 *RJC2 *RJC2 *RJC1 *RJC0/"0" *RJC1 *RJCD/"0" *RJCD/"0	*TI *BOT *NSP *FP *FP *BWD *HD *RDY *CVL/*WS RDCTL ROK STPHK VPOS IHDXF IHCOR LOKG	*EMX47 *EMX46 *EMX45 *EMX44 *EMX43 *EMX42 *EMX42 *EMX41 EMX40/EMX4P MODE MCY B&D WRS ZRD	*EMXS7 *EMXS6 *EMXS6 *EMXS5 *EMXS4 *EMXS2 *EMXS2 *EMXS2 *EMXS1 *E	*EMX67 *EMX66 *EMX66 *EMX64 *EMX63 *EMX62 *EMX61 *EMX61 *EMX61 *MCRC *MCRC *BMCR	*EPC77 *ENY76 *ENY76 *ENY75 *ENY75 *ENY74 *ENY73 *ENY72 *EPC71 PMY70/PMYP PMER *STRDC *EDC *STRDC *MOISC *WOC *WOC *WOC *WOC *WOC *WOC *WOC *WO	DS0 DS1 DS1 DS1 DS1 START CHDE CHDE CHD0 CHD1 CHD1 CHD2 CHD3 TSNS *TSNS0 *TSNS0 *TSNS1 *TSNS2 *TSNS2 *TSNS3 *TSNS4 *TSNS5	TRAK R.BE/BUSPE SLX1 SLX0 TUAD2 TUAD1 TUAD0 POINT *DET0 *DET1 *DET1 *DET2 *DET3 *DET4 *DET3	IDBST TNS OVEN CREER DCK REJECT SSC BUSY *102CR *DETA **TSNS8 **DIBG **DNOIS **DNOIS **DBOB	HDENS FPOS EOTS BOTS WRTS ONLS NRZI RDYS AVRCE **WITE/**LRCE **SKEWE **DBCK **D	TULHT IRECY ENDAT TUSMP EMXPSL DVAMPXL DVAMPXL DVAMPXO 2ETK ETKO ETKL ETKL ETKL ETKL ETKL ETKL	BIO (A)/BOO BII(*B)/BOI BIZ(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI6/BO6 BI7/BO7 ZCTL SFCRC LRC CRC	DXFI DXFO DXFO DXFO DXFO DXFO DXFO DXFO MTREQ/TREQ BLOCK OPINC MPRD SCAN ZWRC *NVRCE ETX8 *NSKWE SDRST/*LRCE	XSNS 16TH/*ABPE SETBC/\$LKE DXFE STOP KEMS AROSE 31BSY SCMP ZOP + 900 OPTION	Nickname
Nickname	3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT1 *DT1 *DT1 *ASK *DT0/*DTP *MASK *MASK0 *MASK1 *MASK2 *MASK3 *MASK4 *MASK4 *MASK4 *MASK5	#VINCK #UCE #PREC #MILTE *MISC #EDC #VELCNG #DIAGL/#CRG DACTL DMW LHPOS LHPOS LNVLD ALMSK	*RJC7 *RJC6 *RJC4 *RJC3 *RJC2 *RJC2 *RJC2 *RJC1 WICTL WICTL WIN IBM WEC WEC WICTL WI	*TI *BOT *NSP *FP *FP *BWD *HD *RDY *ROTIL ROK *STPPHK VPOS THEOR LONG TSPHE LONG TSPHE	*EHX47 *EHX46 *EHX45 *EHX45 *EHX44 *EHX43 *EHX42 *EHX41 *EHX41 *EHX41 *EHX41 *EX40/FHX4P **HODE **HO	PEMXS7 *ENXS6 *ENXS5 *ENXS5 *ENXS4 *ENXS3 *ENXS2 *ENXS1 *E	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 *EMX60 *EMX60 *EMX60 *EMX6CC *MCRC *EMCRC *AMCRC *EMCRC *EMC *EMCRC *EMC	#EMC77 #EMT76 #EMT76 #EMT75 #EMT73 #EMT73 #EMT72 #EMT72 #EMT71 #EMT70 #E	DS0 DS1 START CMDE CMD0 CMD1 CMD1 CMD3 TSNS *TSNS0 *TSNS0 *TSNS0 *TSNS1 *TSNS0 *TSNS4 *TSNS4 *TSNS4 *TSNS4 *TSNS5	TARK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET0 *DET1 *DET2 *DET3 *DET4 *DET5 *DET5	IDBST TMS OVEN CREER DCK REJECT SSC BUST *102CR *DETB *TSMS8 *DIBG *DHOIS	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMEPSI DVAMPXI DVAMPXI DVAMPXI ETK	BIO (A)/BOO BIL(*B)/BOI BIZ(SDI)/BO2 BI3/BO3 BI4/BO4 BI5/BO5 BI5/BO5 BI6/BO6 BI7/BO7 CCTL SFCRC LRC CRC RBLKH BLKED CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO6 CRCHGBO7 CRCH	DXFI DXFO DXFO DXFO DXFO DXFO DXFO MTREQ/TREQ BLOCK OPINC MPRD SCAN ZIRG **NYRCE ETX8 **NSXWE SDRST/*LRCE THO	XSNS 16TH/*ABPE SETBC/BLKE DAFE STOP KEMS AROBR BIBSY SCHP ZOP † BOO OPTION	6 7 Nickname U 1 2 3 5 5 6 7 Nickname O 1 1 2 2 3 4 6 5 5 6 7 7 Nickname O 1 1 2 2 3 5 6 5 6 7 7 6 7 7 7 7 7 7 7 7 7 7 7 7 7
Nickname	3 4 5 6 7 0 1 2 3 4 5 6	*DT6 *DT5 *DT4 *DT3 *DT2 *DT1 *DT1 *DT0/*DTP *MASK MASK1 MASK2 MASK3 MASK4 MASK5 MASK4 MASK5 MASK6	*WITHCK *#UCE *#PCEC *MLTE *MISC *EDC *VELCNG *VELCNG *DIAGL/*CRC DMM DMR IHPRE IHPOS INVLD ALHSK MASK	*RJC7 *RJC6 *RJC4 *RJC3 *RJC2 *RJC2 *RJC2 *RJC1 WICTL WICTL WIN IBM WEC WEC WICTL WI	*TI *BOT *NSP *PP *PP *BWD *HD *RDY *RDY *RDCTL ROK VFOS IEDUXP IHCOR LONG ISPHE SKIMG	*EHX47 *EHX46 *EHX45 *EHX44 *EHX44 *EHX44 *EHX42 *EHX42 *EHX42 *EHX41 *EHX40/EHX4P *MODE MCY BS4D WRS ZRD 1600 CER	*EMX57 *EMX56 *EMX55 *EMX55 *EMX53 *EMX53 *EMX52 *EMX51 *E	#EMX67 #EMX66 #EMX65 #EMX63 #EMX63 #EMX63 #EMX62 #EMX61 EMX60/EMX6P CRCST #MCRC #EP=CR #B=0 #B=0 #MCRCZ #A=B *XBIC	*EMC77 *EMC76 *EMC75 *EMC75 *EMC74 *EMC73 *EMC73 *EMC73 *EMC71 *EMC70/EMC7P FMERR *STRDC *SLIPC *NOISC *WBOC *WWC *AWWC *AWWC *AWWC *AWWC *CMP	DS0 DS1 START CMDE CMDE CMD1 CMD2 CMD2 CMD2 CMD3 TSNS *TSNS0 *TSNS1 *TSNS1 *TSNS3 *TSNS3 *TSNS4 *TSNS5	TZAR R.BPE/BUSPE SLX1 SLX1 SLX1 TUAD2 TUAD2 TUAD0 POINT *DET0 *DET1 *DET2 *DET3 *DET5 *DET5 *DET5 *DET5	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMXPSI DVAMPX2 DVAMPX2 DVAMPX0 2ETK ETKO ETKI ETKZ ETKZ ETKS ETKS ETKS ETKS	BIO(A)/BOO BIL(AB)/BOI BIZ(SDI)/BO2 BIZ(SDI)/BO2 BIZ(SDI)/BO3 BIZ(BO) BIZ(BOS	DXFI DXFO DXFO DXFO DXFO DXFO MFREQ/TREQ BLOCK OPTINC MPRD SCAN ZPRC *NVRCE ETK8 SDRST/*LRCE THO TM1	XSNS 16TH/*ABPE SETBC/SLKE DXFE STOP ESHS AROBR 31BSY SCMP ZOP + 800 OPTION	Nickname
Nicicname 6	3 4 5 6 7 0 1 2 3 4 5 6	*DT6 *DT5 *DT14 *DT14 *DT13 *DT11 *DT07 *DT07 *DT07 *DT07 *AASK MASK0 MASK1 *MASK1 *MASK2 *MASK4 *MASK5 *MASK4 *MASK5 *MASK5 *MASK5 *MASK6 *MASK5 *MASK6 *MASK7	*VITHCK *UCE *PEREC *MILTE *MISC *EDC *VELONG *VELONG DACTL DMW DMW IHPRE IRPOS INVLD ALMSK MASK MASK	*RJC7 *RJC6 *RJC3 *RJC3 *RJC2 *RJC2 *RJC1 *RJC0/"0" MTCTL MTM IBM WEC ALIUT MOK "0" BFUL R. BCY/BCY	*TI *BOT *BOT *NSP *FP *FP *FP *RDY **RDY **RDY **ROK ROK STPHK VFOS STPHK UFOS LONG ISPHE SKIMG ITPCNT	#EHX47 #EHX46 #EHX45 #EHX43 #EHX43 #EHX43 #EHX43 #EHX41 #E	#EMX57 #EMX56 #EMX56 #EMX55 #EMX53 #EMX53 #EMX52 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX54 #EMX52 #EMX51 #EMX54 #EMX55 #EMX55 #EMX54 #EMX55 #EMX56 #E	PENKG 7 *ENKG 6 *ENKG 6 *ENKG 6 *ENKG 3 *ENKG 2 *ENKG 1 *ENKG 1 *ENKG 1 *ENKG 1 *ENKG 2 *ENKG 1 *ENKG 2 *ENKG 6 *ENKG 6 **ENKG 6 *	#EMC/77 #EMC/76 #EMC/75 #EMC/75 #EMC/75 #EMC/73 #EMC/73 #EMC/73 #EMC/72 #EMC/71 PMC/70 #EMC/71 #EMC/71 #EMC/70	DS0 DS1 START CMDE CMD0 CMD1 CMD2 CMD3 TSNS *TSNS1 *TSNS1 *TSNS2 *TSNS3 *TSNS4 *TSNS5 *TSNS5 *TSNS6 *TSNS6 *TSNS6 *TSNS6 *TSNS7 *TSNS7	TAK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET1 *DET1 *DET2 *DET4 *DET5 *DET6 *DET6 *DET7 UDID	IDBST TMS OVEN CREER DCK REJECT SSC BUST *102CR *DETB *TSMS8 *DIBG *DHOIS	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMKPSL DVAMPX1 DVAMPX1 DVAMPX0 ZETK ETKO ETKL ETKS ETKS ETKS ETKS ETKS ETKS ETKS ETKS	BIO(A)/BOO BIL(AB)/BOI BIZ(SDI)/BO2 BIZ(SDI)/BO2 BIZ(SDI)/BO3 BIZ(BO) BIZ(BOS	DXFI DXFO DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC *NVRCE EITA *NSKWE SDRST/*LRCE THO TM1 TM2	XSNS 16TH/*ABPE SETBC/SLKE DXFE STOP ESHS AROBR 31BSY SCMP ZOP + 800 OPTION	6 7 Nickname U 1 2 3 5 5 6 6 7 7
Nicicname 6	3 4 5 6 7 1 2 3 4 5 6 7	*DT6 *DT5 *DT14 *DT14 *DT13 *DT13 *DT17 *DT07 *DT07 *DT07 *MASK MASK0 MASK1 MASK2 MASK3 MASK4 MASK5 MASK5 MASK5 MASK5 MASK6 MASK7 THCTL TPCNTM INTVLM	*WITHCK *UCE *UCE *PREC **MISC *MILTE *MISC *EDC *VELCNG *VELCNG DACTI DMY DMY IHPRE IHPRE IHPOS INVLD ALMSK MASK MASK MASK MASK TIMER	*RJC7 *RJC6 *RJC6 *RJC4 *RJC3 *RJC2 *RJC2 *RJC2 *RJC1 WICTL WITH IBM WEC WICK WEC BFUL R. BCY/BCY DVSEL	*TI *BOT *NSP *PP *PP *PP *PP *PP *PU *HID *RUY *RUY *RUY *RUY *RUY *RUY *RUY *RUY	#EHX47 #EHX46 #EHX45 #EHX44 #EHX44 #EHX44 #EHX42 #EHX42 #EHX42 #EHX42 #EHX41 #E	PEMXS7 *ENXS6 *ENXS5 *ENXS4 *ENXS3 *ENXS3 *ENXS2 *ENXS1 PEMS9/PRXSP RDSNS RNO1S RNO1S HBLK HTM HTM HTM PPDK PREA POSA EPOSA DVBO DBOO	*EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX62 *EMX62 *EMX62 *EMX60/EMX6P CRCST *MCRC *MCRC *MCRC *BP-CR *B-C *NCRCC *NCRC *NCRC *SB-C *NCRC *NCRC *SB-C *NCRC *	#EMC77 #EMT76 #EMT76 #EMT76 #EMT75 #EMT74 #EMT73 #EMT72 #EMT72 #EMT72 #EMT71 PMERR #STRDC #STLPC #MOISC #WDCC #WDC	DS0 DS1 START CMDE CMD0 CMD1 CMD2 CMD2 CMD3 TSMS *TSMS0 *T	TARK R.BPE/BUSPE SLX2 SLX1 SLX0 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET0 *DET1 *DET2 *DET3 *DET4 *DET5 *DET7 UQ1D FIDO	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMXPSI DVAMPX2 DVAMPX2 DVAMPX0 ZETK ETKO ETKI ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ	BIO(A)/BOO BIL(AB)/BOI BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIL/BOO BIL/BOO CRCL SFCRC LRC CRC CRC CRC CRC CRC CRCRG CRCRG CRCRG CRCRG R. ROB/RDB. S	DXFI DXFO DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC ANVRCE ETKB ANSKWE SDRST/*LRCE THO TMI TMI TM2 TM3 CEA	XSNS 16TH/*ABPE SETBC/SLKE DXFE STOP EEMS AROBR 31BSY SCMP ZOP + 800 OPTION ID	Nickname
Nicicname 6	3 4 5 6 7 1 2 3 4 5 6 7	*DT6 *DT5 *DT4 *DT3 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1	*VITHCK *UCE *PREC *MULTE *MISC *MEDC *VELONG *VELONG *VELONG DACTL DMW DMW THPRE 1HPOS INVLD ALHSK HASK HASK CTD/CT8	*RJC7 *RJC6 *RJC7 *RJC4 *RJC3 *RJC3 *RJC2 *RJC1 *RJC1 *RJC1 WIN ITCTL WIN IN UNC ALIWI WOK "O" BEUL R.BCY/BCY DVSEL TAGI	*TI *BOT *NSP *FP *FP *BWD *HD *HD *HD *RDY *OVL/*WRS RDCTL ROK SIPHK VYOS IHDXP IHCOR LONG ISPHE SKWMG TPCNT /CTO /CTI	#EMX47 *EMX46 *EMX45 *EMX45 *EMX43 *EMX43 *EMX41 EMX40/EMX41 EMX40/EMX41 HOVE BAD WRS 2RD 6250 16600 CGR DVTAG GO TAGVIL	#EMX57 #EMX57 #EMX55 #EMX55 #EMX54 #EMX53 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX50 #E	PENMG 7 *ENMG 6 *ENMG 6 *ENMG 5 *ENMG 3 *ENMG 3 *ENMG 1 *ENMG 1 *ENMG 1 *ENMG 1 *ENMG 1 *ENMG 6 *MCRC 2 *B-C *B-C *B-C *B-C *A-B *XBIC DBII DBII DBII	#EMC/77 #EMC/76 #EMC/76 #EMC/75 #EMC/75 #EMC/73 #EMC/73 #EMC/71 #EMC/7	DS0 DS1 START CMDE CMD0 CMD1 CMD3 TSNS *TSNS0 *TSNS0 *TSNS0 *TSNS3 *TSNS2 *TSNS2 *TSNS4 *TSNS5 *TSNS5 *TSNS5 *TSNS5 *TSNS5 *TSNS6 *TSNS7 RSV	TRAK R.BPE/BUSPE SLX2 SLX1 SLX0 TUAD2 TUAD2 TUAD1 TUAD0 POINT *DET1 *DET1 *DET2 *DET3 *DET5 *DET5 *DET5 *DET5 *DET6 *DET7 UQ1D FID0	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMMPSI DVAMPXI DVAMPXI DVAMPXO ZETK ETKO ETKI ETKI ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ	BIO(A)/BOO BIL(AB)/BOI BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIL/BOO BIL/BOO CRCL SFCRC LRC CRC CRC CRC CRC CRC CRCRG CRCRG CRCRG CRCRG R. ROB/RDB. S	DXFI DXFO DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC ANVRCE ETX8 *NSKWE SDRST/*LRCE TH0 TH1 TH2 TH3 TM3 CEA	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP KEMS STOP KEMS 31BSY SCMP ZOP + 0 0 0 0 0 0 0 0 1 0 1 0 1 0 1 0 1 0 1	6 7 Nickname U 1 2 3 3 5 6 7 Nickname 0 1 2 2 3 4 5 6 7 7
Niciename 6	3 4 5 6 7 1 2 3 4 5 6 7	*DT6 *DT5 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1 *DT1	*VTHCK *UCE *UCE *PREC *MITE *MISC *EDC *VELONG *BILAGL/*CNC DACTL DMW DMR IHPPE IHPOS INVLD ALHSE *MASE *ASE *CTO/CT8 CTJ/CT9 CTJ/CTA CTJ/CT8	*RIC7 *RIC6 *RIC6 *RIC4 *RIC3 *RIC2 *RIC2 *RIC1 *RIC0/"0" WICTL WICTL WICTL WEC ALIWI WDC *COP BEUL R.BCY/BCY DVSEL TAGI C. CRY	*TI *BOT *NSP *FP *FP *FP *FP *FP *FU **HD **HD **ROT *ROK STPHK VFOS THEOR LONG THEOR LONG TFCTI /CTI /CTI /CTI	#EHX47 #EHX46 #EHX45 #EHX45 #EHX44 #EHX43 #EHX42 #EHX42 #EHX41 #EHX40 #E	#EMX57 #EMX56 #EMX55 #EMX54 #EMX53 #EMX52 #EMX51 #EMX51 #EMX51 #EMX50/FMX5P RDSNS RUNO1S RRELK HTM WIND PHOK PREA POSA EPOSA DV80 D800 D801 D801	#EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 *EMX60 *BMCRC *EMCRC *MCRC *MCRC *MCRC *MCRC *B=0 *B=0 *MCRC *MCRC *MCRC *MCRC *MCRC *MCRC *B=0 *B=0 *MCRC	#EMC/77 #EMC/76 #EMC/76 #EMC/75 #EMC/75 #EMC/73 #EMC/73 #EMC/73 #EMC/72 #EMC/71 #EMC/71 #EMC/70 #EMC/7	DS0 DS1 START CMDE CMD0 CMD1 CMD1 CMD2 TSNS *TSNS0 *TSNS0 *TSNS0 *TSNS1 *TSNS2 *TSNS3 *TSNS3 *TSNS3 *TSNS4 *TSNS5 *TSNS5 *TSNS5 *TSNS6 *TSNS7 RSV0 RSV0 RSV1 RSV2	TARK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET1 *DET1 *DET2 *DET4 *DET5 *DET5 *DET7	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDER AVRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT INECV ENDAT TUSMP EMMPS1 DVAMPX2 DVAMPX1 DVAMPX0 ZETK ETKO ETKI ETKZ ETKZ ETKZ ETKZ ETKZ ETKA TINT /TIHR /TIHR	BIO(A)/BOO BIL(AB)/BOI BIL(AB)/BOI BIZ(SDI)/BO2 BIJ/BO3 BIJ/BO3 BIJ/BO3 BIJ/BO7 CCTL SFCRC LRC CRC RBLKM BLKED CRCRG CRCRG RBLKM RLED CRCRG RBLKM RLED REPER/RDB REPER/RDB	DXFI DXFO DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC ANVRCE ETKB ANSKWE SDRST/*LRCE THO TMI TMI TM2 TM3 CEA	XSNS 16TH/*ABPE SETBC/SLKE DXFE STOP EEWS AROUR BIBSY SCHP ZOP + 0900 OPTION ID	Nickname
Nickname 6	3 4 5 6 7 1 2 3 4 5 6 7	#DT6 #DT5 #DT4 #DT3 #DT3 #DT1 #DT1 #DT1 #DT1 #DT1 #DT1 #DT1 #DT1	*WITHCK *UCE *UCE *PREC **MISC *EDC *VELONG *VELONG *VELONG DACTI. DMW DMR IHPRE IHPRE IHPOS INVLD ALMSK MASK MASK TIMER CTO/CT8 CTI/CT9 CTI/CT3 CTI/CT3 CTI/CTG CTI/CTC	*RJC7 *RJC6 *RJC4 *RJC3 *RJC2 *RJC2 *RJC2 *RJC1 *RJC1 WICTL WICTL WICTL WICTL WICTL WICTL WEG BEUL RJC7 BEUL RJC7 BEUL TAGI C.CRY *WDVENB/XCAL	*TI *BOT *NSP *FP *FP *FP *FP *RDY *AUT **NSP *FP *FP *FP *FP *FP *FP *FP *FP *FP *F	*EHX47 *EHX46 *EHX45 *EHX44 *EHX44 *EHX44 *EHX42 *EHX42 *EHX41 *E	#EMX57 #EMX56 #EMX55 #EMX54 #EMX53 #EMX53 #EMX53 #EMX52 #EMX51 EMX50/EMX5P RDSNS RNO1S HBUK HTM WIND PHOK PREA POSA EPOSA DV80 DB01 DB02 DB02	*EMX67 *EMX66 *EMX65 *EMX63 *EMX63 *EMX63 *EMX62 *EMX62 *EMX62 *EMX60 EMX60 EMX60 *EMX62 *MCRC2 *EP=CR *B=D *NGCC *S=C *S=C *S=C *S=C *S=C *S=C *S=C *S	*EMC/77 *EMM/76 *EMM/76 *EMM/75 *EMM/73 *EMM/73 *EMM/73 *EMM/72 *EMM/71 *EMM/7	DS0 DS1 START CMDE CMD1 CMD2 CMD1 CMD2 CMD3 TSNS *TSNS0 *TSNS1 *TSNS1 *TSNS1 *TSNS3 *TSNS3 *TSNS4 *TSNS3 *TSNS5 *TSNS5 *TSNS5 *TSNS7 RSV RSV0 RSV1 RSV2 RSV3	TARK R.BPE/BUSPE SLX2 SLX1 SLX0 SLX0 TUADD TUADD TUADD TUADD POINT *DETO *DETT	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EDTS BOTS WATS ONLS NRZI RDYS RDERR *VRCE *VRCE *SKEWE *DBCR *DBCR *DBCR *DBCR *DBCR *DBCR *DBCR *OROE *POSAE **OO **OO **OO **OO **OO **OO **OO **	TULHT IRECV ENDAT TUSMP EMXPSI DVAMPX2 DVAMPX2 DVAMPX0 2ETK ETKO ETKI ETKZ ETKZ ETKS ETKS ETKS ETKS TINT /TIMR /TIMR	BIO(A)/BOO BIL(AB)/BOI BIL(AB)/BOI BIZ(SDI)/BO2 BIJ/BO3 BIJ/BO3 BIJ/BO3 BIJ/BO7 CCTL SFCRC LRC CRC RBLKM BLKED CRCRG CRCRG RBLKM RLED CRCRG RBLKM RLED REPER/RDB REPER/RDB	DXFI DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZMRC ETKB **NYRCE ETKB **NSKME SDRST/*LRCE THO TM1 TM2 TM1 TM2 TM3 CEA PEVN	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP EEWS STOP EEWS STOP EEWS 31BSY SCMP ZOP + 800 OPTION IID - IID - IT - IT - IT - IT - IT - IT	Nickname
Nickname 6	3 4 5 6 7 1 2 3 4 5 6 7	#DT6 #DT5 #DT4 #DT3 #DT3 #DT0 #DT0/*DTP #ASK #ASK0 #ASK1 #ASK2 #ASK3 #ASK4 #ASK5 #ASK5 #ASK6 #ASK7 THCTL INTVLH C. OTTP LWRFNT R. CRT7/S. CMT	*VITHCK *UCE *UCE *PREC *MLTE *MISC *MESC *VELONG *VELONG *VELONG DACTL DMW DMR THPRE THPOS TINVLD ALHSK HASK HASKB TIMER CTI/CT9 CTI/CT9 CTI/CT6 CTI/CT6 CTI/CT6 CTI/CT7	*RJC7 *RJC6 *RJC7 *RJC6 *RJC4 *RJC3 *RJC2 *RJC1 *RJC1 *RJC1 WTCTL WTM IBM WEC ALIVI WOK "O" DVSEL R.BCT/BCY DVSEL TAGI C.CRY *DVENB/XCAL	*TI *BOT *NSP *PP *PP *PP *PP *PP *PP *PP *PP *RUT *HUT *RUT *ROTIL ROK STPPHK VFOS IHDXF IHCOR LONG ISPHE SKMMG TPCNT /CT1 /CT2 S.UCT/CT3 S.DCT/CT4 TSTP/CT5	#EHX47 *EHX46 *EHX45 *EHX44 *EHX43 *EHX44 *EHX43 *EHX41 *EHX40/EHX4P HODE HCY BAD UCZ EN TAG 6250 1600 CER DYTAG GO TAGVIL STS CTIL DBMPX	PEMIS 7 *ENCS 6 *ENCS 6 *ENCS 5 *ENCS 3 *ENCS 3 *ENCS 2 *ENCS 1 *ENCS 2 *ENCS 1 *ENCS 2 *ENCS 3 *ENCS	#EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 *EMX61 *EMX61 *EMX60 *EMX61 *EMX60 *EMX61 *EMX60 *EMX61 *EMX61 *EMX60 #EMC/77 #EMC/76 #EMC/76 #EMC/75 #EMC/75 #EMC/73 #EMC/73 #EMC/73 #EMC/72 #EMC/71 #EMC/7	DS0 DS1 START CMDE CMD0 CMD1 CMD2 CMD3 TSNS TSNS1 *TSNS1 *TSNS2 *TSNS3 *TSNS4 *TSNS5 *TSNS5 *TSNS6 *TSNS6 *TSNS7 RSV RSV0 RSV1 RSV2 RSV2 RSV2	TANK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET1 *DET1 *DET1 *DET2 *DET2 *DET5 *DET6 *DET7 *UIT *DET7	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EOTS BOTS WRTS ONLS NRZI RDYS RDERR *VRCE *MLTE/*LRCE *SKEWE *DBCK	TULHT IRECV ENDAT TUSMP EMXPSI. DVAMPX2 DVAMPX1 DVAMPX0 ZETK ETK0 ETK1 ETK2 ETK3 ETK4 ETK5 ETK6 ETK7 TINT /TINT	BIO (A) / BOO BIL (AB) / BOI BIZ (SDI) / BOO BIZ (SDI) / BOO BIZ (SDI) / BOO BIZ / BOO BIZ / BOO BIZ / BOO CCTL SPCRC LRC CRC RELKN BLKED CRCHG GRCHG R. RDB / RDB. S MPERR RENB / RDB. S RPER / OFL	DXFI DXFO DXFO PRECV MTREQ/TREQ BLOCK OPINC OPINC PRED SCAN ZMRC ANVRCE EITA ANSKWE SDRST/*IRCE THO THI TM2 TM3 TM3 TM3 FEVN EERAF FEVN EERAF	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP EENS STOP EENS SLOP ZOP + 00 OPTION ID CEB //CEIV /ACP /OFST //SINH	6 7 Nickname 0 1 2 3 3 5 6 6 7 Nickname 0 1 1 2 2 3 6 6 7 Nickname 0 1 1 2 2 3 6 6 7 Nickname 0 1 1 1 Nickname 0 1 1 1 Nickname 0 1 1 1 Nickname 0 1 1 Nickname 0 Nickname	
Nickname 6	3 4 5 6 7 1 2 3 4 5 6 7	#DT6 #DT5 #DT4 #DT3 #DT1 #DT0/*DTP HASK MASK0 MASK1 HASK2 HASK3 MASK4 MASK5 MASK6 MASK6 MASK6 MASK6 MASK6 MASK7 THCTL TPCNTM INTVLM C. QTP LURPMI R. CTU/CNTU R. CTU/CNTU	*VITICK *UCE *UCE *UCE *PREC **MITE **MITSC *EDC *VELCNG *VELCNG *DIAGL/*CRG DACTL DMW IMR IHPRE IHPRE INVLD ALMSK HASKS TIMER CTO/CT8 CTI/CT9 CT2/CTA CT3/CTB CT4/CTC CT5/CTD CT6/CTE	*RIC7 *RIC6 *RIC6 *RIC3 *RIC3 *RIC3 *RIC3 *RIC3 *RIC1 *RIC0/"0" WICTL WICTL WICTL WEC ALIWI WDK "0" BFUL R.BCY/BCY DVSEL TAGI C.CEY *DVSEL SULTAGI DVBSY DVAO DVAL	*TI *BOT *NSP *PP *PP *PP *PP *PP *PP *PP *PP *RUT *HUT *RUT *ROTIL ROK STPPHK VFOS IHDXF IHCOR LONG ISPHE SKMMG TPCNT /CT1 /CT2 S.UCT/CT3 S.DCT/CT4 TSTP/CT5	#EHX47 #EHX46 #EHX45 #EHX44 #EHX43 #EHX43 #EHX42 #EHX42 #EHX41 #EHX40 #EHX41 #EHX40 #EHX41 #EHX40 #EHX41 #EHX40 #EHX41 #E	#EMX57 #EMX56 #EMX55 #EMX54 #EMX53 #EMX53 #EMX52 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX50 #E	#EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX60 *EMX60 *EMX60 *EMX60 *MCRC *MCRC *EMCRC *EMCRC *BMCRC *BMCRC *BMCRC *EMCRC *BMCRC	#EMC/77 #EMM/76 #EMM/76 #EMM/75 #EMM/73 #EMM/73 #EMM/73 #EMM/73 #EMM/72 #EMM/72 #EMM/79 #FMERR #STRDC #STLPC #MOISC #WOCC #WOC	DS0 DS1 START CMDE CMD0 CMD1 CMD1 CMD3 TSNS *TSNS0	TARK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET0 *DET1 *DET2 *DET3 *DET4 *DET5 *DET5 *DET5 *DET5 *DET6 *DET7 UQ1D FID0 FID0 FID0 FID1 FID2 FID3 FID4 FID5	IDBST TNS OVEN OVEN CREER DCL CREER DCL SSC BUSY *102CR *102CR *DETB *TSNS8 *DIBG *DIBG *DBOB *DBARA *DITM	HDENS FPOS EDTS BOTS WARTS ONLS NRZI RDYS RDYS RDER AVECE *MLTE/*LRCE *SKEWE *DBCK *DBCM *	TULHT INECV ENDAT TUSMP EMORSI. DVAMPX2 DVAMPX1 DVAMPX0 ZETK ETKO ETKI ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ ETKZ	BIO(A)/BOO BIL(AB)/BOI BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(SDI)/BOO BIZ(BOO BOO BIZ(BOO BOO BIZ(BOO BOO BOO BOO BOO BOO BOO BOO BOO BOO	DXFI DXFO DXFO PRECV MTREQ/TREQ BLOCK OPINC OPINC PRED SCAN ZMRC ANVRCE EITA ANSKWE SDRST/*IRCE THO THI TM2 TM3 TM3 TM3 FEVN EERAF FEVN EERAF	XSNS 16TH/*ABPE SETBC/SLKE DXFE STOP EENS AROBR BIBSY SCMP ZOP † 800 OPTION III † CEB //CEIV //ACP //OFST //SINH	6 7 Nickname 0 1 2 3 5 6 7 Nickname 0 1 2 2 3 4 6 5 6 7 Nickname 0 1 2 2 3 4 6 5 6 7 7 Nickname 0 1 2 3 7 Nickname 0 1 2 2 2 2 3 7 Nickname 0 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
Nickname 6	3 4 5 6 7 1 2 3 4 5 6 7	#DT6 #DT5 #DT4 #DT3 #DT3 #DT0 #DT0/*DTP #ASK #ASK0 #ASK1 #ASK2 #ASK3 #ASK4 #ASK5 #ASK5 #ASK6 #ASK7 THCTL INTVLH C. OTTP LWRFNT R. CRT7/S. CMT	*VITICK *UCE *UCE *UCE *PREC **MITE **MITSC *EDC *VELCNG *VELCNG *DIAGL/*CRG DACTL DMW IMR IHPRE IHPRE INVLD ALMSK HASKS TIMER CTO/CT8 CTI/CT9 CT2/CTA CT3/CTB CT4/CTC CT5/CTD CT6/CTE	*RJC7 *RJC6 *RJC4 *RJC3 *RJC2 *RJC2 *RJC2 *RJC1 *RJC1 WICTL WIN IBM WEC *BUUL *WOK **O** *	*TI *BOT *NSP *FP *FP *FP *BWD *HID *HID *HID *RDY *OVL/*WRS RDCTL ROK STPHK VPOS IHDXP IHCOR LONG ISPHE SKMMG TPCNT /CT1 /CT2 S.UCT/CT3 S.DCT/CT4 CTSTP/CT5 R.RCT/CT6	#EMX67 #EMX66 #EMX46 #EMX45 #EMX43 #EMX43 #EMX42 #EMX42 #EMX41 EMX40/EMX4P MODE MCY BAD URS CZRD 6250 16600 CGR DVTAG GO TAGVIL STS CTL DBMPX TSP0 TSP1	#EMX57 #EMX56 #EMX55 #EMX54 #EMX53 #EMX53 #EMX52 #EMX51 #EMX51 #EMX51 #EMX51 #EMX51 #EMX50 #E	#EMX67 *EMX66 *EMX65 *EMX64 *EMX63 *EMX62 *EMX61 *EMX61 *EMX61 *EMX60 *EMX61 *EMX60 *EMX61 *EMX60 *EMX61 *EMX61 *EMX60 #EMC/77 #EMC/76 #EMC/76 #EMC/75 #EMC/75 #EMC/73 #EMC/73 #EMC/73 #EMC/72 #EMC/71 #EMC/7	DS0 DS1 START CMDE CMD0 CMD1 CMD2 CMD3 TSNS TSNS1 *TSNS1 *TSNS2 *TSNS3 *TSNS4 *TSNS5 *TSNS5 *TSNS6 *TSNS6 *TSNS7 RSV RSV0 RSV1 RSV2 RSV2 RSV2	TANK R.BPE/BUSPE SLX2 SLX1 SLX1 SLX0 TUAD2 TUAD2 TUAD0 POINT *DET1 *DET1 *DET1 *DET2 *DET2 *DET5 *DET6 *DET6 *DET7 *UQ1D FID0 FID0 FID1 FID2 FID2 FID3 FID5 FID6 FID7 FID7 FID7 FID7 FID7 FID7 FID7 FID7	IDBST TNS OVEN OVEN CREER DCJ CREER DCJ SSC BUST *102CR *DETB *TSNSB *TSNSB *DIBG *DIBG *DBOB *DARA *DITM	HDENS FPOS EOTS BOTS WARTS ONLS NRZI RDYS RDERR *VYCE *MLTE/*LRCE *DBCK *DBCK *DBCK *DBCK *DBCK *DBCK *POSAE *OP	TULHT IRECV ENDAT TUSMP EMXPSI. DVAMPX2 DVAMPX1 DVAMPX0 ZETK ETK0 ETK1 ETK2 ETK3 ETK4 ETK5 ETK6 ETK7 TINT /TINT	BIO(A)/BOO BIL(AB)/BOI BIL(AB)/BOI BIZ(SDI)/BO2 BIJ/BO3 BIJ/BO3 BIJ/BO3 BIJ/BO7 ZCTL SFCRC LEC CRC HBLKM BLKED CRCHG CRC	DXFI DXFO DXFO RECV MTREQ/TREQ BLOCK OPINC MPRD SCAN ZIRG ANVRCE ETXB ANSKWE SDRST/*IRCE THO TM1 TN2 TM1 TN2 CEA PEVN ERRF EPCSK 2NDFLAG	XSNS 16TH/*ABPE SETBC/BLKE DXFE STOP EEWS STOP EEWS STOP EEWS 31BSY SCMP ZOP † 300 OPTION ID	6 7 Nickname 0 1 2 3 3 4 5 6 6 7 Nickname 0 1 2 2 3 3 6 6 7 Nickname 0 1 2 2 3 3 6 7 Nickname 0 1 2 3 3 7	

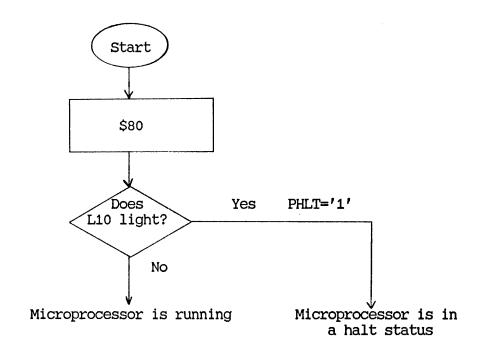
INTERFACE SIGNAL DISPLAY

Principal interface signals that indicate the operational condition of the FMT, and signals indicating the status of the microprocessor, can be displayed by a field tester. The display function is available when the FMT is in any status. The procedure for display is to set SO through S7 to \$80. Then, the interface signals are displayed on LO through L11.

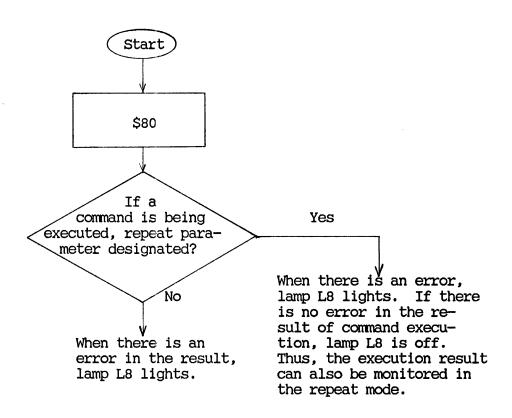
Interface Signal Display:



Example 1: Inspect the microprocessor to determine whether it is in the Halt status. When the PHLT (L10) signal is '1', it indicates that the microprocessor is in the halt status.



Example 2: Monitoring of ERRF Bit. When setting the FMT in the offline status and executing a command from a field tester, the FMT is informed of the result of the execution through ERRF bit. When ERRF='1', it indicates that there is an error.



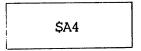
MICROPROGRAM ADDRESS DISPLAY

A microprogram for the FMT is stored in the ROM which plays the role of control storage (CS). The processor takes micro-instructions from the CS. The content of the address register for reading out micro-instructions from the CS can be displayed using a field tester.

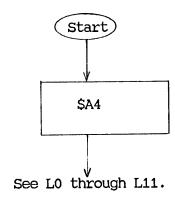
When the processor is in the 'STEP' status, the step forwarding of the program sequence can be verified. If the processor is in the 'RUN' status, LO will light, which is effective for maintenance.

The procedure for display is to set \$0 through \$7 to \$A4.

CS ADDRESS DISPLAY:

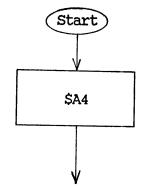


Example 1: Inspect the CS address with the processor in the 'RUN' status.



• When the FMT is in the idle state, the program is stored in lower address (\$0X to \$1X). L0 through L2 are off and L3 through L11 are half lit (half lighting of \$1F).

Example 2: Observe CS address during the execution of command.



L0 - L11 are observed.

LO - L11 blink during command execution.

REGISTER WRITE

Data can be written in registers controlled by the microprocessor of the FMT using a field tester.

Using this function, the operator can provide the microprogram of the FMT with various data. For example, in case of the executive of a command in the offline mode, various parameters necessary for the execution of a command can be specified by writing data in a particular register. For maintenance purpose, the register write function is a means of specifying parameters.

Writing predetermined data in a register is accomplished as follows:

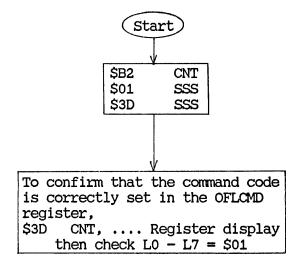
Register Write:

'B2'	CNT	
'dd'	SSS	dd: Write data
'aa'	SSS	aa: Register address

Example 1: Command Code Setting to Offline Command Register

To issue a command from a field tester in the offline mode of the FMT, the commandcode needs to be set in the OFLCMD register (address \$3D).

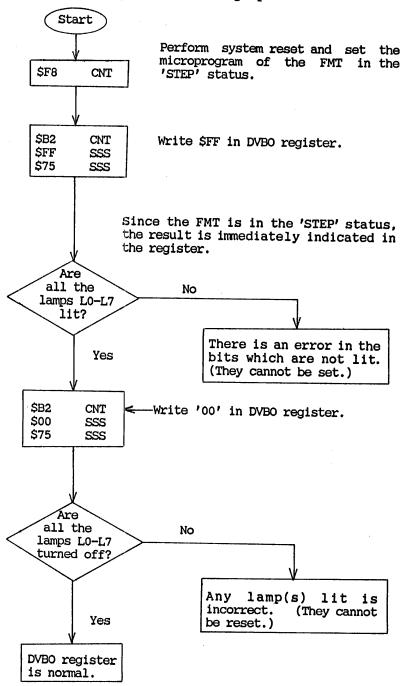
Write the write command code (\$01) in the OFLCMD register as follows:



Example 2: Register Function Check.

If there is doubt about the function of a register, a field tester is useful for writing data in the register by using the register write function. Use DVBO register (address \$75) as an example.

The compare address is set by the following operations.



CS PARITY SCAN

With the field tester, all addresses (\$0000 to \$1FFF) of CS can be scanned to check parity. To start CS parity scan, the ROSF bit must be set. When the scan begins, it is repeated until the ROSF bit is reset or a parity error is detected. When the STEP bit and ROSF bit are set, the scan is stepped forward by toggling the SSS switch.

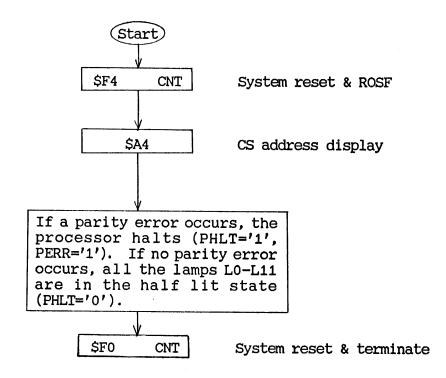
To start CS Parity Scan

\$F4 CNT

To end (reset)

\$FO CNT

Example: Perform parity scan of all CS addresses.



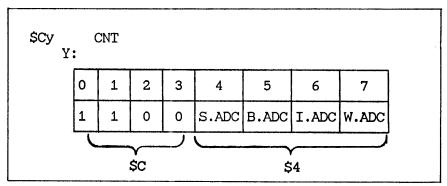
ADDRESS COMPARE

A field tester can ensure that control passes a particular microprogram address. When control passes the address, the field tester can direct the processor to halt, to bypass to another address, to display the content of register, to write data in a register, and so on.

However, to use these functions efficiently, knowledge of the contents of the microprogram and register is required. Therefore, these functions are not normally used for the maintenance purpose. This example is for reference only.

Whether or not control passes a particular microprogram address can be verified by displaying the ACMP signal. The ACMP signal can be reset by toggling the SSS switch.

Other functions are specified by the following procedure.



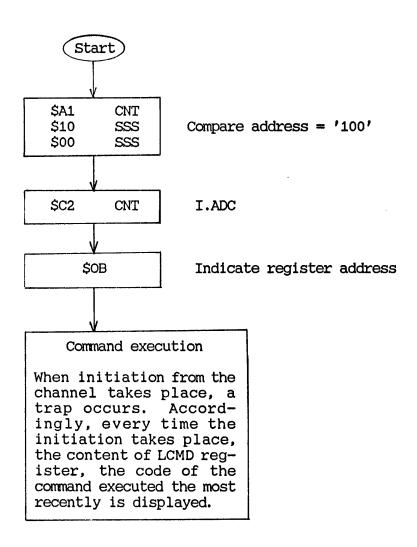
The compare address is set by the following operation.

\$Al	CNT		
\$1X	SSS	x:	Arbitrary
\$mn	SSS	1mn:	Compare address

In addition, since the compare output appears at card pin BEZ of 1A07, the timing can be observed by an oscilloscope.

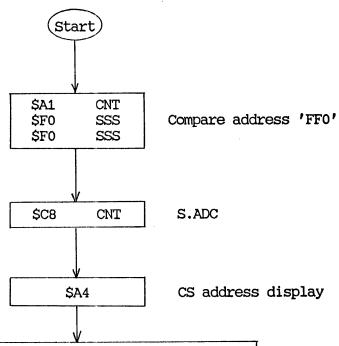
Example 1: Confirm the execution of an Analysis Routine

When an Interrupt occurs in the processor of the FMT, control passes microprogram address '100'. The example of displaying the content of LCMD register (address \$0B) at the time when an Interrupt occurs is explained below.



Example 2: Address Compare Stop

The example of halting the processor immediately after control passes microprogram address 'FF0' of the FMT is shown below. Address 'FF0' is the address which control passes when a reset routine is executed.



When is it intended to execute the reset routine, the processor halts. Then, L0 - L11 (CS address) displays the next address. To release the processor from the halt status, switch SSS has to be turned on. However, if the address compare is successful again, the processor will halt.

COMMAND EXECUTION IN THE OFFLINE STATUS OF THE FMT

If the FMT is in the offline mode, a command can be issued to the FMT by using a field tester. Command code, byte count, device address and other parameters can be provided by writing appropriate data in predetermined registers.

All the registers concerned with command execution in the offline mode of the FMT are listed below.

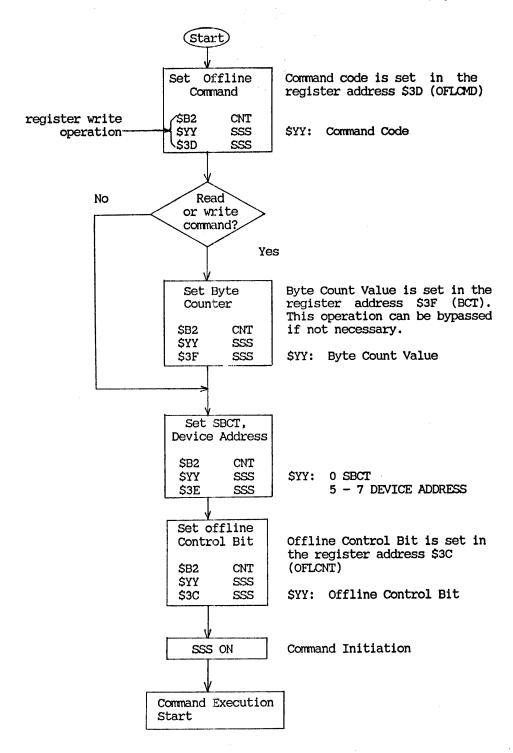
```
SDIA0
       (address $38)
SDIA1
       (address $39)
                             Diagnostic flag bytes 0 - 3
SDIA2
        (address $3A)
SDIA3
       (address $3B)
OFLCNT (address $3C)
                        ... Command execution control parameter
                        ... Command code
OFLCMD (address $3D)
OFLDVA (address $3E)
                        ... Device address
BCT
       (address $3F)
                        ... Byte count
```

Since these registers are not reset except the case of the FMT power on, once they are set, it is not necessary to set them again unless any change is required.

- Note 1: The write data in a write command is always \$FF. Also, the data read by a read command is not sent out to the channel.
- Note 2: When the command reverse function (REV.UEX parameter) is specified, the content of OFLCMD register changes. Also, when TUSCAN parameter is specified the content of OFLDVA register changes.

Example: Command Execution

Contents of SDIA0 - SDIA3 are usually \$00. The following operation is carried out when it is ensured that the contents of these registers are \$00. The content of SINH is '0'.



UNIT CHECK PARAMETER

When a command is executed in the offline mode of the FMT by a field tester, the following operations can be done if the result of the command execution causes an error (unit check is set). These operations are specified by UC.STP (unit check-step) and UC.RP (unit check-repeat) bits (bit 0 and bit 1) of OFLCNT register (address \$3C).

Unit Check Parameters

UC.STP	UC.RP
0	0 No function
0	 When UCK (unit check) occurs, the repositioning operation
1	0 When UCK occurs, the microprogram performs "looping" after executing a command. Looping continues until SINH 2 bit is set, UC.STP parameter is reset, or system reset is asserted.
1	1 When UCK occurs, the repositioning operation is performed. If there is a new error during repositioning, the microprogram performs looping after the repositioning operation. The release condition for looping is the same as above.

Notes:



Repositioning operation

For the write command ----> After backspacing an error block, an erase command is executed. (In case an error occurs during writing, a rewind command is executed.)

For the read command ----> An error block is backspaced.

For the read backward command

nd ----> An error block is spaced.

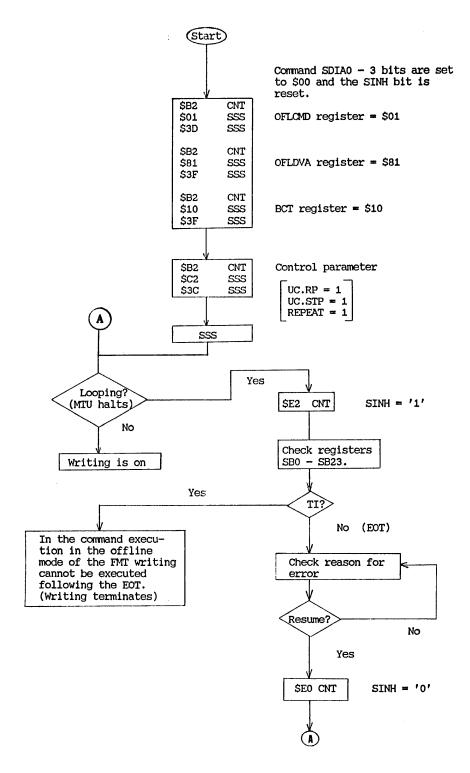
For other commands ----> No operation



If UC.STP or UEX.STP parameter is specified and the microprogram is in a loop, the loop is released when SINH bit is set. If the REPEAT parameter is specified, the next command is suppressed by setting SINH bit on. The command execution can be resumed by resetting the SINH bit.

Example: Writing 16-byte data to the MTU.

It is assumed that writing is performed as far as the EOT, and when there is a write error, repositioning takes place. Also, when there is an error during reposition, writing is interrupted, looping is executed and then the sense byte is checked.



UNIT EXCEPTION PARAMETER

When the field tester executes a command in the FMT offline mode, the following operations can be handled by the field tester if the microprogram termination status contains the 'Unit-Exception' parameter.

Г	— UEX Par	ameters —			
	UEX.STP	UEX.REW	UEX.REV		
	1	x	x	••••	When UEX is detected, the microprogram is looped. Release from the loop can be done by resetting UEX.STP parameter, setting the SINH bit, or by the system reset.
	0	0	0	• • • • •	No function
	0	0	1		When UEX is detected, the content of OFLCMD register is converted into the reverse command code 1 and execution is continued.
	0	1	0	••••	When UEX is detected, the Rewind command is executed.
	0	1	0	••••	When UEX is detected, the REWIND command is executed. The speed mode is then reversed (Normal speed <> high speed) to continue the command execution.

Note:

1 Reverse commands

Old OFLCMD	Reversed new OFLCMD					
WRT (06)	RDB (05) RDF (04) BSP (09) SP (0B) RDB (05) BSPF(08) BSPF(08)	• • • • • • • • • • • • • • • • • • • •	When When When When When	a tape a tape a tape a tape EOT is	mark is	s detected s detected s detected s detected ed

Example: Repetitive forward and backward read of blocks between two adjacent tape marks is shown in Figure 3.

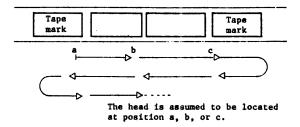
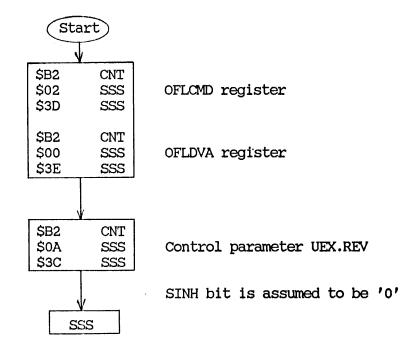


Figure 3. Repetitive forward/backward read.



In this example,

- (1) \$B2 = "Enter the register write mode."
- (2) \$02 = "Data to be written into the register."

 In this case, \$02 means "write in a streaming mode to EOT."
- (3) \$3D = "Register location in which the data is being written."

 In this case, \$3D is the location of the OFLCMD register. OFLCMD = offline command

The offline command is issued here to write in a streaming (high speed) mode. The next box selects the MTU to be used. OFLDVA = offline device address. \$00 means MTU #0.

The next group of instructions sets the control parameter OA = data to be written into register \$3C which is OFLCNT. OFLCNT = offline control. Entering \$0A at this register sets UX.RV and REPEAT. UX.RV causes the tape rotation direction to reverse when the tape mark is detected.

When all of these instructions are accomplished, the tape will be set in motion when SSS is toggled. If nothing happens (no tape movement), this means SINH is set to '1'. This can be checked by displaying register CEB (\$7). SINH is bit 3 (lamp 3). If the lamp is on, SINH (start inhibit) has been set and motion cannot be accomplished. To clear the register (set SINH to 0), first enter \$B2, CNT; second, enter \$00, (00 will set all bits including SINH to 0) and toggle SSS. Finally, select the CEB (\$7F) register and toggle the SSS switch. This should clear the register, thereby setting SINH to '0'. Check this by displaying the CEB register.

TUSCAN PARAMETER

When the FMT is in the offline mode, a field tester can issue a command to all the MTUs connected to the FMT sequentially. The parameter used for this purpose is TUSCAN bit (bit 7 of OFLCNT register address \$3C).

When the TUSCAN parameter is specified, the device address of OFLDVA register is increased by 1 (when the address is #7, it is incremented to #0) when the FMT microprogram completes the execution of a command to a particular MTU (including repositioning).

If a REPEAT parameter is not set, the SSS switch must be toggled for each MTU. If a REPEAT parameter is specified, the SSS switch is only toggled to start execution.

It is not practical to use the TUSCAN parameter together with UC.STP parameter since UCK is reported by MTUs which are in the NOT READY status (or which are not operational) and therefore, looping is not performed when the command is issued to the address of that MTU.

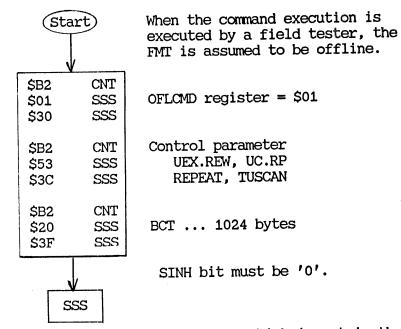
It is recommended that the TUSCAN parameter is used with UC.RP parameter and REPEAT parameter (not with UC.STP parameter) to operate a number of MTUs concurrently and observe their operation.

Example: Writing 1024-byte data on MTUs #0 - #3

When writing reaches the EOT, the tape is rewound, and writing continued. (UEX.REW parameter)

When an error occurs during the write operation, repositioning is implemented. (UC.RP parameter)

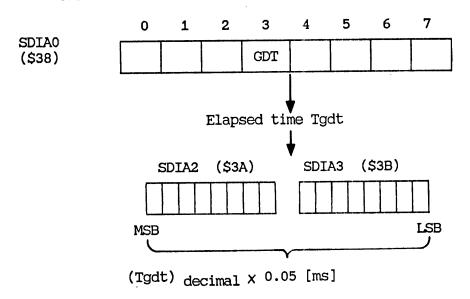
When an error occurs during the repositioning, looping is prohibited.



Although the MTU which is not in the READY status is set in UCK (IRQ), the command is executed. (No looping) Accordingly, the MTU may be set in the READY status after executing the above operation. In this case, when the MTU is set in the READY status, the write operation can start.

GO-DOWN-TIME PARAMETER

GDT parameter provides predetermined elapsed time between the termination command and when the next command is executed. This elapsed time is determined by the content of registers SDIA2 and SDIA3.



Note:

The diagnostic flag byte register (SDIAO - SDIA3, address \$38 to \$3B) is effective when the FMT is offline. When the FMT is in the online mode, the diagnostic flag byte register is given by a Set Diagnose command.

Example: Repetitive Forward Reading of Data Block N at every 6.4 ms (Using RPOS parameter)

MTU #0 is loaded with a tape with at least 3 data blocks written as shown in Figure 4. The magnetic head is assumed to be located at position(a).

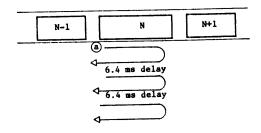
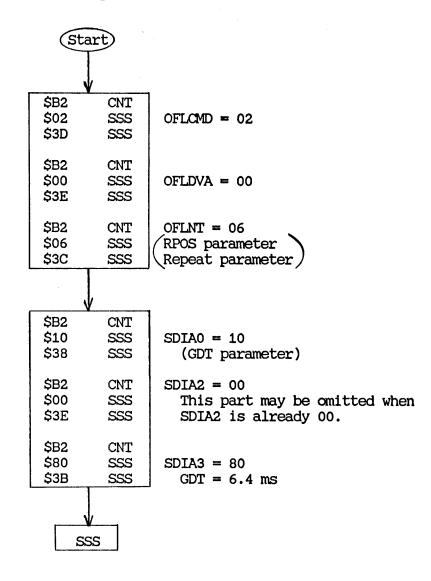


Figure 4.

Repetitive forward read using RPOS parameter (continued).



TEST MIS

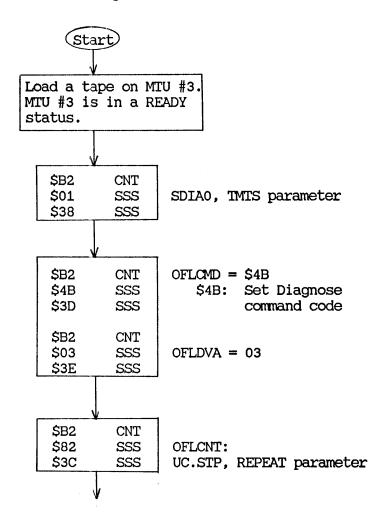
When the TMTS parameter is set at bit 7 of the diagnostic flag byte register 0 (SDIAO - address \$38), and a SET DIAGNOSE command (command code \$4B) is issued, a diagnostic program for the FMT can be executed.

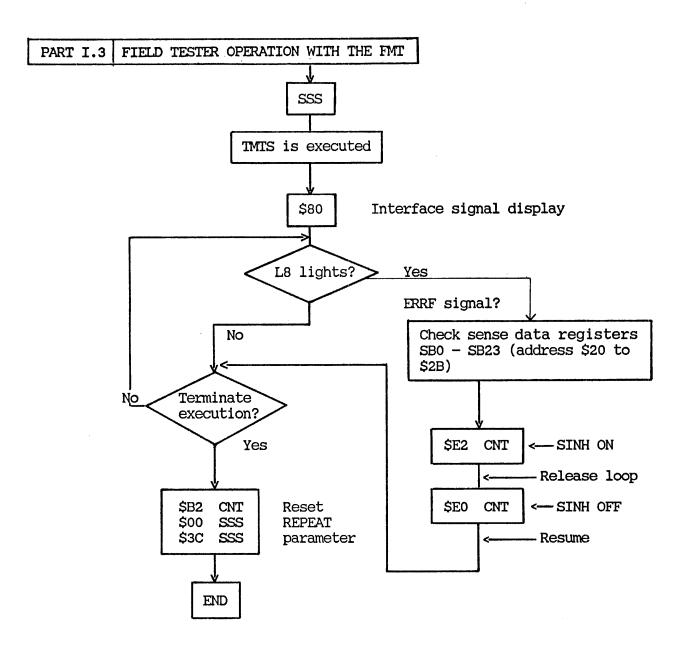
	0	1	2	3	4	5	6	7
SDIA0 (\$38)								TMTS

If there is an error in the diagnostic result, the unit check is contained in the end status. (EQC) The operator of field tester can obtain the diagnostic result by checking whether ERRF (L8 at SO - \$80) is lit or DSB (address \$08). To execute the TEST MTS, a SET DIAGNOSE command must be issued to the MTU which is the READY status.

Example: Execute Test MTS for MTU #3.

It is assumed that the execution uses REPEAT parameter and the UC.STP parameter and is repeated until an error occurs.





PART II MAINTENANCE

INTRODUCTION

Part II of the Maintenance Manual is divided into 11 sections. In general, the material contained in Part II will be used to determine what corrective actions to take when the MTU is not operating properly. In most cases, the user will refer to sections on troubleshooting error codes that are displayed on the MTU front panel or error codes that are accessible when the field tester is connected to the FMT.

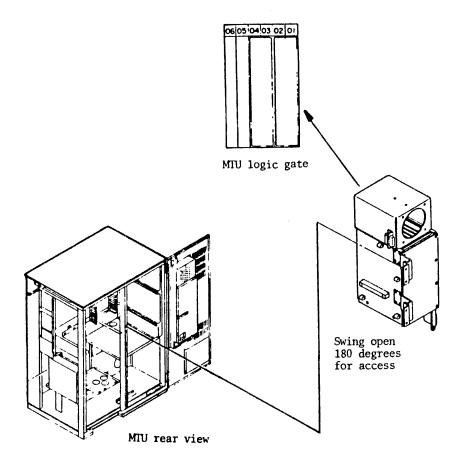
When a fault has been isolated, Part II directs the user to the proper maintenance action. The user will then perform either a check and adjustment procedure, or replace the faulty equipment, as specified by the error code description or troubleshooting flowchart.

To assist the user in quick locating a maintenance action, tabs are provided to identify each topic. The topics covered in Part II are as follows:

- Section A: MTU error codes and troubleshooting
 Section B: Power supply unit troubleshooting
- Section C: FMT and MTU offline and online diagnostics
- Section D: Status line troubleshooting
- Section H: Preventive maintenance
- Section J: Cleaning
- Section K: Check and adjustment procedures
- Section L: Subassembly replacement
- Appendix A: Glossarv of terms
- Appendix B: Signals used in logical circuits
- Appendix C: MTU registers

PCA LOCATION

Throughout Part II of the Maintenance Manual, printed circuit assemblies (PCAs) are identified by slot number in the MTU or FMT logic gates or by their common names, such as write/read PCA. Use Figure 1 and Table 1 to locate PCAs in the MTU. For example, in model M2434L1 (master unit), slot 1A05 of the MTU logic gate contains the PCA identified as 512648U (P/N C16B-5126-048#U). This PCA is referred to as "1A05 in the MTU" throughout the Maintenance Manual. Similarly, use Figure 2 and Table 2 to locate PCAs in the FMT. When removing PCAs from a logic gate, use PCA removal tool (P/N C960-0300-T001).



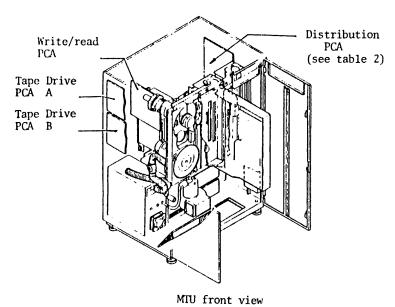


Figure 1.

PART II MAINTENANCE

Table 1. MTU PCA location

Model		MIU PCA	logic gate		Tape drive	Write/read		
number	1AØ1/1AØ2	1AØ3/1AØ4	1AØ5	1AØ6	A PCA	B PCA	PCA	
M243ØL (slave to M2434L)	Power unit	P/N B16B- 7190-0020 A#U TKBMU	P/N C16B- 5126-0480 #U 512648U	P/N C16B- 5126-Ø49Ø #U 512649U	A#U	P/N B16B- 7210-0200 A#U Tape drive TVBMU	-0200 7210-0200 A#U e drive Tape drive	P/N B16B- 7240-0030 A#U WRIMU
M2431L (slave to M2434L)	UMLQV				Tape drive			P/N B16B-7260 -0020 A#U WRKMU
M2432L (slave to M2435L/6L)							P/N B16B-7230 -0030 A#U WRHMU	
M2433L (slave to M2435L)							P/N B16B-7250 -0020 A#U WRJMU	
M2434L1							P/N B16B-724Ø -ØØ3Ø A#U WRIMU	
M2434L2								
M2435L1							P/N B16B-7230 -0030 A#U WN-IMU	
M2435L2	·	P/N B16B-7190 -0100 A#U TKHMU	İ					
M2436L1			P/N C16B- 5325-Ø21 #U 532521U					
M2436L2								
м24361.8					·	·	5	

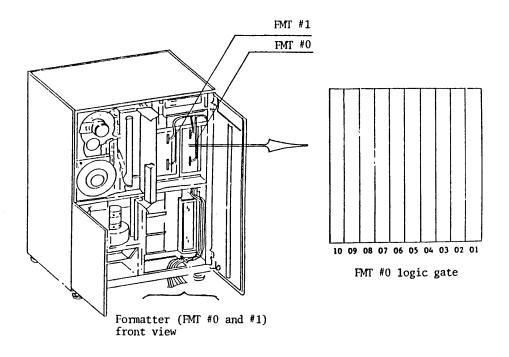


Figure 2. FMT PCA location diagram.

PART II MAINTENANCE

Table 2. FMT PCA location.

Model number	FMT PCA logic gate											
namber	1AØ1	1AØ2	1AØ3	1AØ4	1AØ5	1AØ6	1AØ7	1AØ8	Distribution board			
M243ØL (slave to M2434L)												
M2431L (slave to M2434L)	V	Vo.	V				,					
M2432L (slave to M2435L/6L)	None	None	None	None	None	None	None	None	None			
M2433L (slave to M2435L)												
M2434L1		P/N C16B- 5121-Ø88Ø #U 512188U		P/N C16B- 5500-0880 #U 550088U	P/N C16B- 5126-Ø36Ø #U 512636U	P/N C16B- 5121-Ø86Ø #U 512186U	P/N C16B- 5127-Ø92Ø #U 512792U	P/N C16B- 5125-Ø67Ø #U 512567U	P/N B16B-7390- 0010A 739001 DGAMU			
M2434L2	(read) (800 bpi)	d) (read)					(VFO)	(DV INT)	(write)	512/920	5125670	P/N B16B-7390- 0020A 739002
M2435L1		٠.	None	P/N C16B- 5500-0870 #U (VFO)			;		P/N B16B-7390- ØØ1ØA 7390Ø1 DGAMU			
M2435L2				(410)					P/N B16B-7390- Ø02ØA 739ØØ2			
M2436L1	None						P/N C16B- 5326-0610 #U 532661U		P/N B16B-7390- 0010A 739002 DGAMU			
M2436L2							3320010		P/N B16B-739Ø ØØ2ØA 739ØØ2			
M2436L8	None	None	None	None	None	None	None	None	None			

A0000 MTU ERROR CODES AND TROUBLESHOOTING

INTRODUCTION

Section A provides MTU troubleshooting based on the 2-digit error code displayed on the MTU front panel. Begin troubleshooting by looking up the error code in the MTU Error Code Table beginning on the following page (A0001). A description of the error and a reference to the troubleshooting flow chart (MAP) is given for each error code.

In all cases for which the correction action involves replacing more than one PCA (printed circuit assembly), the recommended method is to replace the first PCA listed and determine if the problem has been corrected. If the problem has not been corrected, replace the second PCA listed.

Prior to PCA or subassembly replacement, the user should perform any checks and adjustments (Section K) associated with the problem description. The same checks and adjustments should also be performed after corrective maintenance actions. the user should also enusre that the shorting plugs on a replaced PCA are the same on the replacement PCA.

A field tester is normally connected to the MTU logic gate during MTU troubleshooting. Refer to Part I of this manual for instructions on how to connect and operate the field tester. To assist in MTU troubleshooting or checkout after corrective action, the diagnostic routines (Section C) can be performed.

Error code		Description	Cause of error	Refer to
00	0	When the Unit Check is lit on the MTU front panel, a parity error of the ROM is detected before execution of the microprogram	error	A0030
01	0	Faulty operation of arithmetic logic unit (ALU) during power on.	Hardware error	A0030
02	0	Faulty execution of a microprogram sub- routine during power on.	Hardware error	A0030
03	0	Faulty operation of register at file address \$00 through \$03 during power on.	Hardware error	A0030
04	0	Faulty operation of register at file address \$04 through \$07 during power on.	Hardware error	A0030
05	0	Faulty operation of register at file address \$08 through \$0B during power on.	Hardware error	A0030
06	0	Faulty operation of generated register at file address \$0C through \$0F during power on.	Hardware error	A0030
07	0	Faulty operation of timer 0 at file address \$10 during power on.	Hardware error	A0030
08	0	Faulty operation of timer 1 at file address \$11 during power on.	Hardware error	A0030
10		Faulty operation of the counter at file address \$12.	Hardware error	A0030
11		Faulty operation of general register at file address \$13.	Hardware error	A0030
12		There is inconsistency between 3 signals o Tape present (TP) o Beginning of tape (BOT) o End of tape (EOT)	Hardware error	A0031
13		ROMPE (ROM Parity Error)signal, RGPE (Register Parity Error) signal, or HUBLK (Hub Lock) signal is set incorrectly.	Hardware error	A0031
15		TSFL (Test Flag) signal or TST (Test Start) signalis set correctly.	Hardware error	A0031

Error code	Description	Cause of error	Refer to
16	Faulty operation of the register at file address \$18.	Hardware error	A0030
17	ONL (Online), INATRP (Interruption), UCHLD (Unit Check Hold), TUCHK (Tape Unit Check), GAPCT (Gap Control), or TWA (Tape Warning Area) signal is set incorrectly.	Hardware error	A0031
18	RTLAL (Right Tape Loop Alarm), LTLAL (Left Tape Loop Alarm), HUBAL (Hub Lock Alarm), ECER (erase Circuit Error), WCER (Write Circuit Error), or WRIST (Write/Read PCA Installed) is incorrect.	Hardware error	A0031
19	CLINF (Column In File), CLINM (Column In Machine), or EMMVD (Error Marker Moved) signal is set incorrectly.	Hardware error	A0031
20	Failure in STEP6 (Step 6 ALL) - PE level setting is incorrect.	Hardware error	A0031
21	WVON (Write Voltage ON), ECON (Erase Current ON), AGCOK (SAGC OK) or VELO.1 (Velocity Mode 0.1) signal is incorrect.	Hardware error	A0031
22	One of the read data detecting signal, TMSR 0 - 7, (time sensor 0 through 7) is incorrectly set at '1'.	Hardware error	A0031
23	One of the read data detecting signal, TMSR $0-7$, (time sensor 0 through 7) is incorrectly set at $'1'$.	Hardware error	A0031
24	GOB (Go Tag), STS (Status Tag), TMSR8 (Time Sensor 8), DNOIS (Detected Noise), DBOB (Detected Beginning of Block), DTM (Detected Tape Mark), or 0 (Logical '0') signal is incorrectly set at '1', or DIBG (Detected Inter Block Gap) signal is incorrectly set at '0'.	Hardware error	A0046
25	TMSR8, DNOIS, or DBOB signal is set at '0', or DIBG signal is set at '1'.	Hardware error	A0031
28	A parity error is detected in ROM during the execution of an instruction.	Hardware error	A0030
29	A parity error occurs in LSI register in file address \$00 to \$0B.	Hardware error	A0030

Error code	Description	Cause of error	Refer to
30	Current flows even after resetting the error marker drive.	Hardware error	A0043 A6000
31	The window does not close within a prescribed time.	Operator or Hardware error	A0110
32	Reel hub lock signal is erroneously detected.	Hardware error	A0041
35	Front door open is detected during unloading. Check that the front door is firmly closed.	Operator or Hardware error	A0420
36	File column in signal is not set to OFF during unloading.	Hardware error	A3020
37	Machine column in signal is not set to OFF during unloading.	Hardware error	A3020
38	Tape present signal is not set to OFF after the tape has been completely rewound onto the file reel during unloading.	Hardware error	A3030
40	Front door open is detected during unloading. Check that the front door is firmly closed.	Operator or Hardware error	A0420
41	Cartridge does not open. Check cartridge position.	Hardware error	A0120
42	The low tape is not detected within a prescribed number of rotations of the machine reel.	Hardware error	A0300
43	Auto hub is not locked.	Hardware error	A0320
45	The window is not closed. Press the reset and load button.	Hardware error	A0110
46	File column in signal is incorrectly detected.	Hardware error	A0310
47	Machine column in signal is incorrectly detected.	Hardware error	A0310

Error code	Description	Cause of error	Refer to
48	Tape present signal is detected after the tape has been rewound for a load retry.	Hardware error	A3030
49	The tape has not passed the BOT/EOT sensor. (Tape present signal is not detected.	Hardware error	A0350
50	Reel loaded signal is erroneously detected.	Hardware error	A0360
51	Reel loaded signal is not detected.	Hardware error	A 0360
52	The length from the starting tip of tape to the BOT marker is too short. (This length should be 4.3 to 5.5 m or 14 to 18 feet.)	Operator error	A0380
53	BOT marker cannot be detected within the prescribed distance.	Operator or Hardware error	A0400
54	Machine column in signal is not detected.	Hardware error	A0310
55	File column in signal is not detected.	Hardware error	A0310
56	Loop alarm is detected after machine reel column in signal.	Hardware error	A0430
57	Loop alarm is detected after file reel column in signal.	Hardware error	A0430
60	Loop alarm in file reel column is detected when the capstan speed down (HSCF) is on.	Hardware error	A0170 A2000
61	Loop alarm in file reel column is detected when the capstan speed down (HSCF) is off.	Hardware error	A0170 A2000
62	Loop alarm in machine reel column is detected when the capstan speed down (HSCM) is on.	Hardware error	A0170 A2000
63	Loop alarm in machine reel column is detected when the capstan speed down (HSCM) is off.	Hardware error	A0170 A2000

Error code	Description	Cause of error	Refer to
64	Reel hub lock is released.	Hardware error	A0320
65	Front Door open is detected after tape is loaded. Check that the front door is firmly closed.	Operator or Hardware error	A0420
70	Tach pulse is not detected when capstan motor is started.	Hardware error	A0550
71	The phase of capstan tach pulse A/B is incorrect.	Hardware error	A0550
72	Capstan continues to turn back and forth during position control. (Direction detecting signal OD remains set at '1'.)	Hardware error	A0500
73	Capstan does not turn back and forth during position control. (Direction detecting signal OD remains at '0'.)	Hardware error	A0500
74	The range of stop position of the capstan is too long (longer than \pm 36 QTP = quarter tach pulse.)	Hardware error	A0450
75	The stop position of the capstan is not stable when servo lock is applied after the capstan stops.	Hardware error	A0450
80	Write voltage is turned on during the read status, or write voltage is not turned off within a prescribed time.	Hardware error	A0330
81	Write voltage is turned off during the write status, or write voltage is not turned on within a prescribed time.	Hardware error	A0330
82	Erase current is turned on during the read status, or erase current is not turned off within a prescribed time.	Hardware error	A0330
83	Erase current is turned off during the erase status, or the erase current is not turned on within a prescribed time.	Hardware error	A0330
84	Error in the +12 V supply.	Hardware error	A0330

Error code	Description	Cause of error	Refer to
85	Write voltage was not turned on within a prescribed distance during write operation in the streaming mode.	Hardware error	A0340
86	File protect was turned on during write erase operation. Turn protect switch off.	Operator or Hardware error	A5000
87	File protect was turned on during the DSE (Data Security Erase) operation. Turn protect switch off.	Operator or Hardware error	A5000
88	An error occurred in the level setting for the PE (phase encode) mode.	Hardware error	A0044
99	Error is in the tape. (This error is displayed after unloading is completed. However, the Unit Check light remains off.)	Tape or Hardware error	Replace the tape

Use the MTU PCA location chart (see divider tab at the beginning of Part II) to locate MTU printed circuit assemblies (PCAs). When locating or replacing PCAs, observe these procedures:

- (1) Turn off the MTU power supply.
- (2) Use extraction tool P/N C960-0300-T001.
- (3) Mark the connector before removing to ensure correct replacement.
- (4) Avoid bending connector pins when installing a PCA.

Some corrective actions require monitoring a signal at the MTU motherboard. Figure A-1 shows the system by which the pins are identified. The location of pin ADV is given as an example.

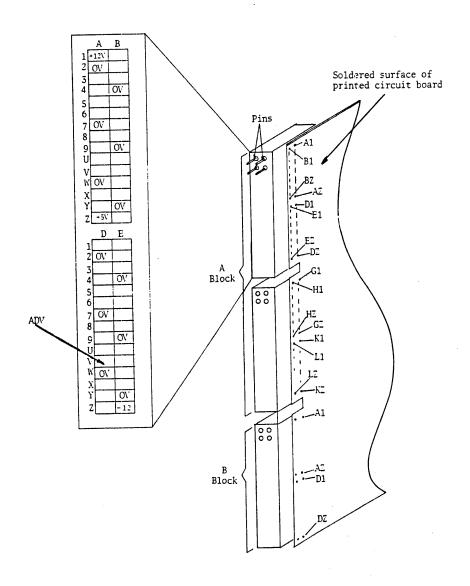
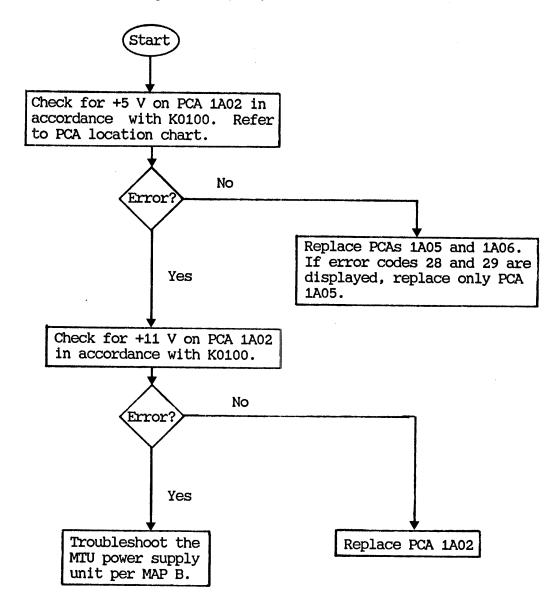


Figure A-1. Signal-monitoring points (pins) on MTU motherboard ADV location is shown as an example.

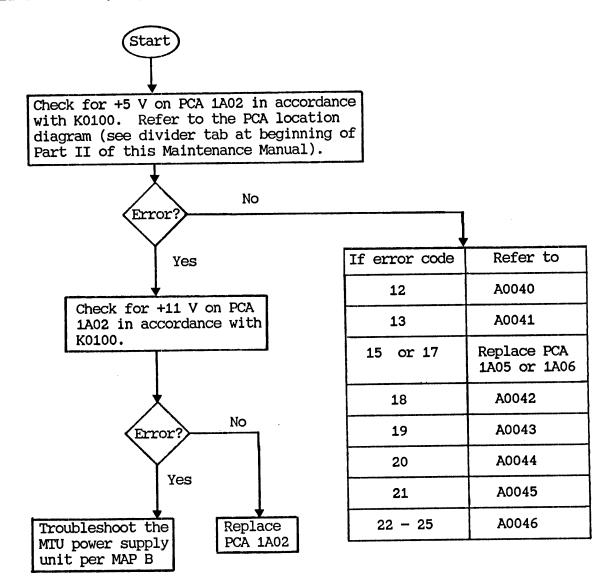
A0030 MTU TROUBLESHOOTING

Error Codes 00 through 11, 16, 28, and 29.



A0031 MTU TROUBLESHOOTING

Error Codes 12, 13, 15, and 17 through 25.



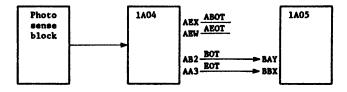
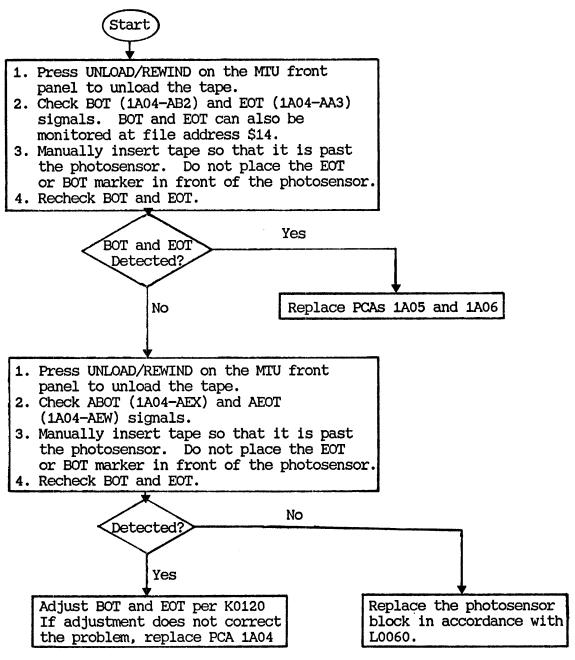


Figure A-2. Troubleshooting Error Code 12.

A0040 MTU TROUBLESHOOTING

Error Code 12 continued. Inconsistency among tape present, BOT, and EOT signals.



Notes:

(1) File address \$14

Bit 0 TP: Tape present

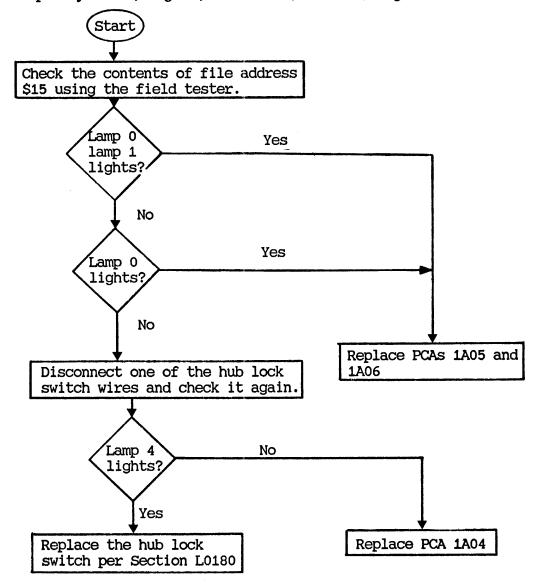
Bit 4 BOT: Beginning of tape

Bit 5 EOT: End of tape.

(2) A detected signal corresponds to a logical high (nominal 5 V or a "1").

A0041 MTU TROUBLESHOOTING

Error Codes 13 (continued) and 32. ROMPE (ROM parity error) signal, RGPE (register parity error) signal, or HUBLK (hub lock) signal is set.



- (1) File address \$15:
 - Bit O ROMPE: ROM parity error
 - Bit 1 RGPE: Register parity error
 - Bit 4 HUBLK: Hub lock.
- (2) If necessary, refer to Part I of this Maintenance Manual for instructions on how to display a register file address using the field
- (3) Refer to Section L for subassembly removal instructions.(4) Refer to PCA location chart (see divider tab) when replacing PCAs.

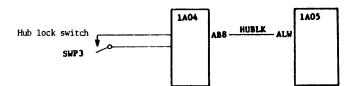
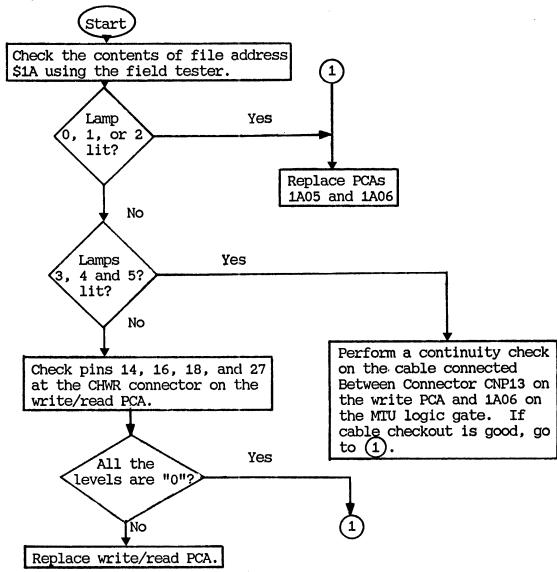


Figure A-3. Troubleshooting Error Codes 13 and 32.

A0042 MTU TROUBLESHOOTING

Error Code 18 (continued). Either RTLAL (right tape loop alarm) LTLAL (left tape loop alarm), HUBAL (hub lock alarm) ECER (erase circuit error), WCER (write circuit error), or WRIST (write/read PCA installed) is incorrectly set.



- (1) File address \$1A:
 - Bit 0 RTLAL: Right tape loop alarm Bit 1 LTLAL: Left tape loop alarm
 - Bit 2 HUBAL: Hub lock alarm
 - Bit 3 ECER: Erase circuit error
 - Bit 4 WCER: Write/read installed.
- (2) If necessary, refer to Part I of this manual for instructions on how to display a register file address using the field tester.
- (3) Refer to Section L for subassembly removal and replacement instructions.

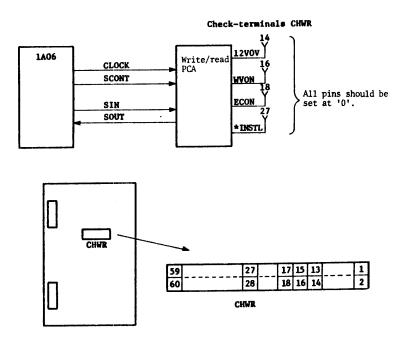
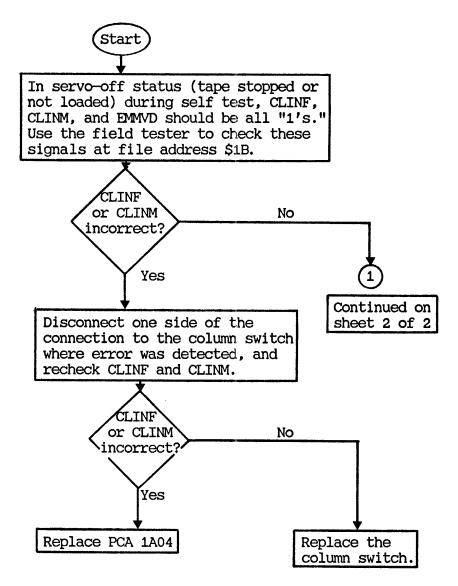


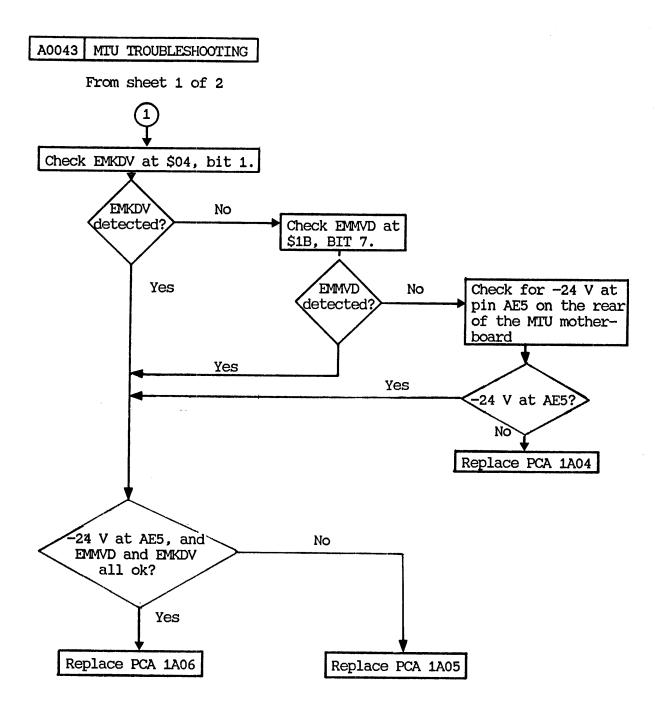
Figure A-4. Write/read PCA.

A0043 MTU TROUBLESHOOTING

Error Codes 19 (continued) and 30. Column in file (CLINF), column in machine (CLINM) error marker moved (EMMVD) signal is set incorrectly.



- (1) File address \$1B:
 - Bit 3 CLINF: Column in file. (Tape in the file column has been detected.)
 - Bit 4 CLINM: Column in machine. (Tape in machine column has been detected.)
 Bit 7 EMMVD: Error marker moved.
- (2) If necessary, refer to Part I of this Maintenance Manual for instructions on how to display a register file address using the field tester.
- (3) Refer to Section L for subassembly removal and replacement instructions.



Note:

(1) For pin designations such as AE5 on the MTU motherboard, refer to A0020, Figure A-1.

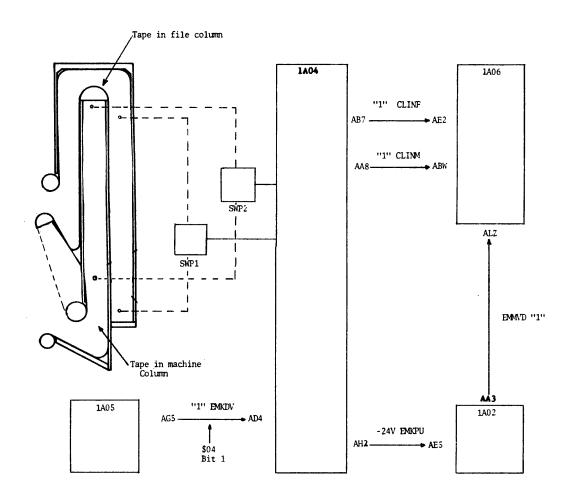
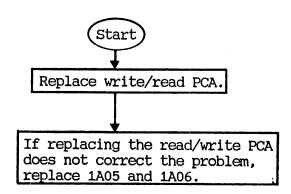


Figure A-5. Troubleshooting Error Codes 19 and 30.

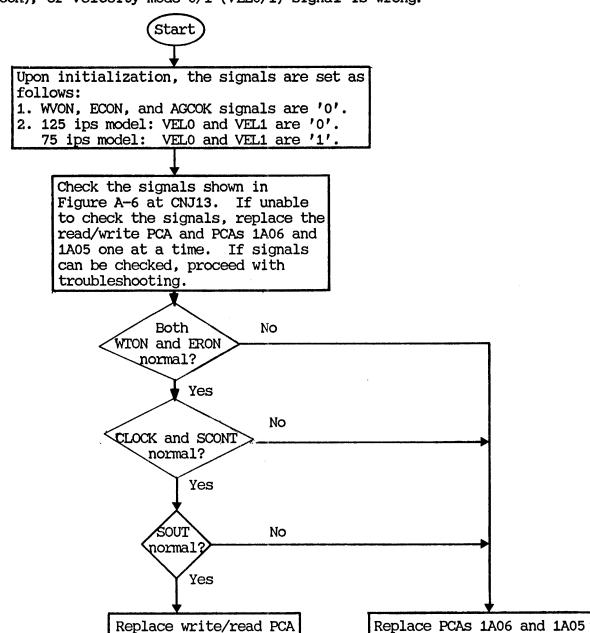
A0044 MTU TROUBLESHOOTING

Error Codes 20 (continued) and 88. Faulty phase encode setting.



A0045 MTU TROUBLESHOOTING

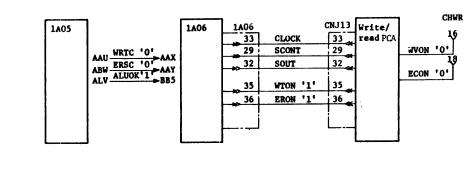
Error Code 21. Write voltage ON (WVON), erase current ON (ECOK), SAGC OK (AGCOK), or velocity mode 0/1 (VEL0/1) signal is wrong.



- (1) File address S1D:
 - Bit 1 WVON : Write voltage ON
 - Bit 2 ECON: Erase current ON
 - Bit 5 AGCOK: SAGC OK
 - Bit 6 VELO: Velocity model 0 Bit 7 VEL1: Velocity model 1.
- (2) If necessary, refer to Part I of this Maintenance Manual for instructions on how to display a register file address using the field tester.

File address \$1D

Bit 1 WVON: Write Voltage ON
2 ECON: Erase Current ON
5 AGCOK: SAGC OK
6 VELO: Velocity Model 0
7 VEL1: Velocity Model 1



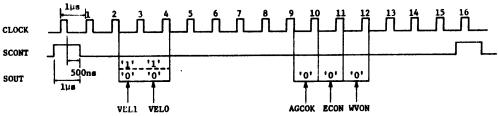


Figure A-6. Troubleshooting Error Code 21.

A0046 MTU TROUBLESHOOTING

Error Codes 22 through 25. Abnormality on file address \$1E and \$1F.

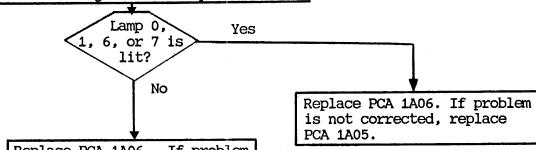


In the initial diagnostics at power on while write-to-read operation is being performed, the signal states are as follows:

- 1. If no write data is sent, all the read data detecting signals (TMSR, DNOIS, DBOB, and DTM) should not be detected. The DIBG should be detected.
- If write data is sent, all the read data signals (TMSR, DNOIS and DBOB) should be detected. DTM and DIBG signals should not be detected.

In addition to the above, GOB and STS signals should not be detected at initialization.

Check file address \$1F using the field tester during the write cycle.



Replace PCA 1A06. If problem is not corrected, replace PCA 1A05. If still not corrected, replace the write/read PCA.

	•			
(1)	File address	\$1E:	<u>Read</u>	<u>Write</u>
	Bit 0 TMSR0:	Time sensor 0	0	1
	Bit 1 TMSR1:	Time sensor 1	0	1
	Bit 2 TMSR2:	Time sensor 2	0	1
	Bit 3 TMSR3:	Time sensor 3	0	1
	Bit 4 TMSR4:	Time sensor 4	0	1
	Bit 5 TMSR5:	Time sensor 5	0	1
	Bit 6 TMSR6:	Time sensor 6	0	1
	Bit 7 TMSR7:	Time sensor 7	0	1
(2)	File address	\$1F:	<u>Read</u>	<u>Write</u>
	Bit O GOB :	Go tag	0	0
	Bit 1 STS :	Status flag	0	0
	Bit 2 TMSR8:	Time sensor 8	1	0
	Bit 3 DNOIS:	Detected noise	1	0
	Bit 4 DBOB:	Detected beginning of block	1	0
	Bit 5 DIBG:	Detected inter block gap	0	1
	Bit 6 DTM :	Detected tape mark	0	0
	Bit 7 0 :	Logical '0'.	0	0

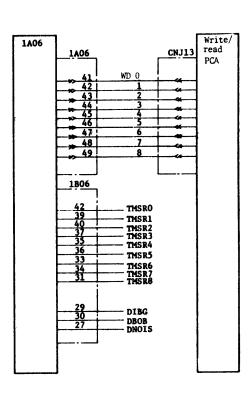
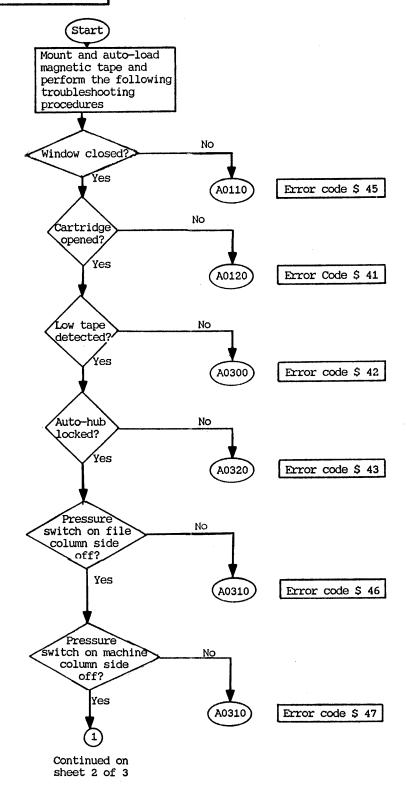
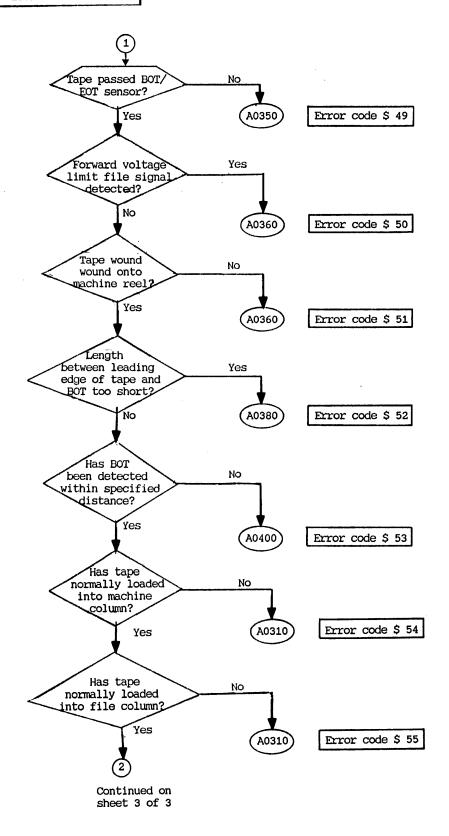
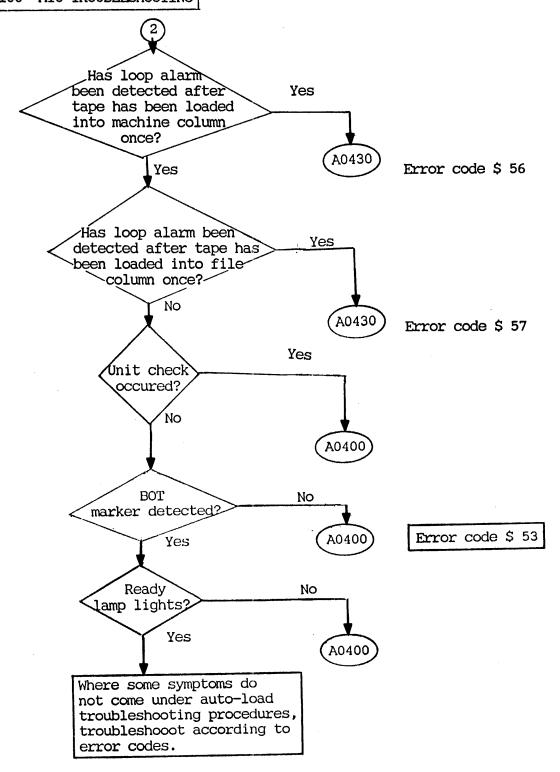


Figure A-7. Troubleshooting Error Codes 22 through 25.

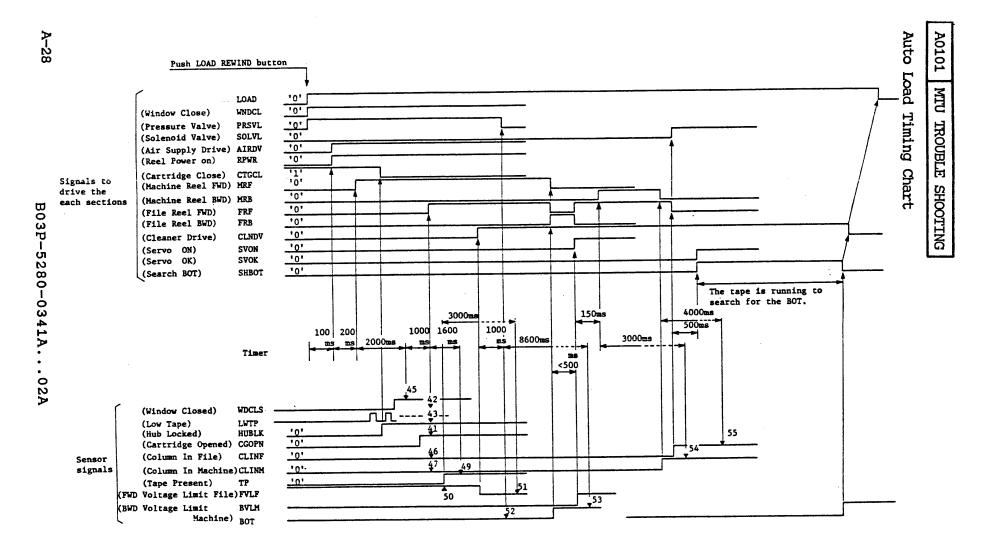




A0100 MTU TROUBLESHOOTING



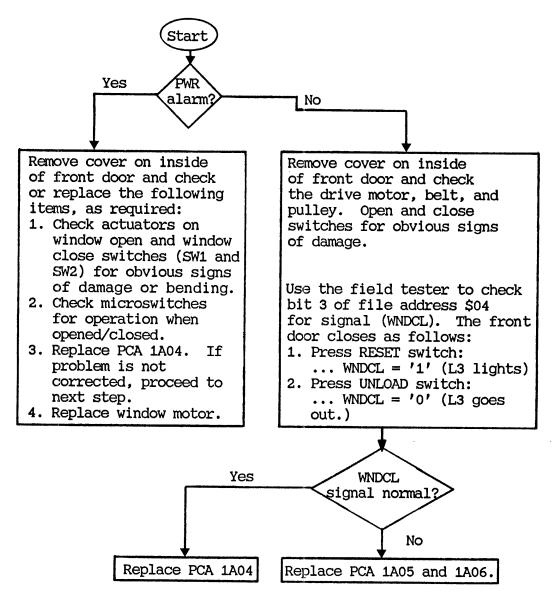
- (1) Unit check lamp flashes if the error occured during a load sequence.
- (2) Push the Reset button to reset error.



Note: The marks 'v' indicate the timings when the program checks the logical level of each sensor during auto loading. The hexadecimal number in upper of the mark 'v' means Error code which is set to ER register.

A0110 MTU TROUBLE SHOOTING

Error codes 31 and 45. Window open/close failure.



- (1) Window open/close failure is due to drive system, microprograms, or mechanism.
- (2) Use the field tester to issue command \$B6 to open and close the window.

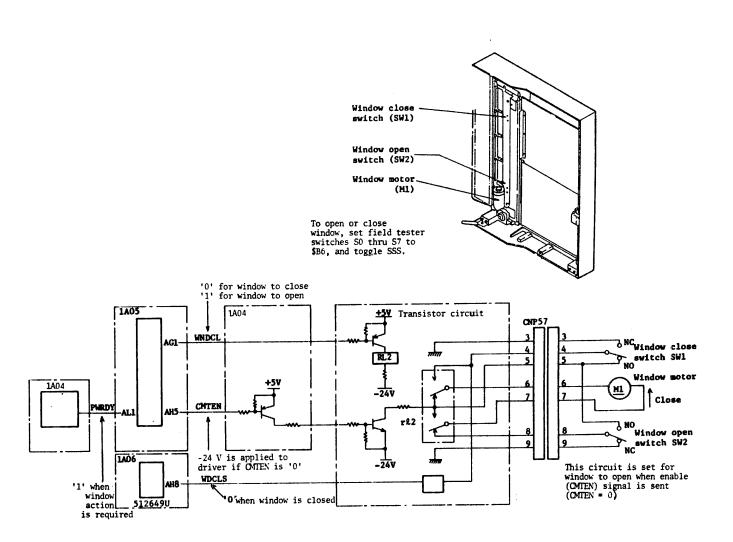
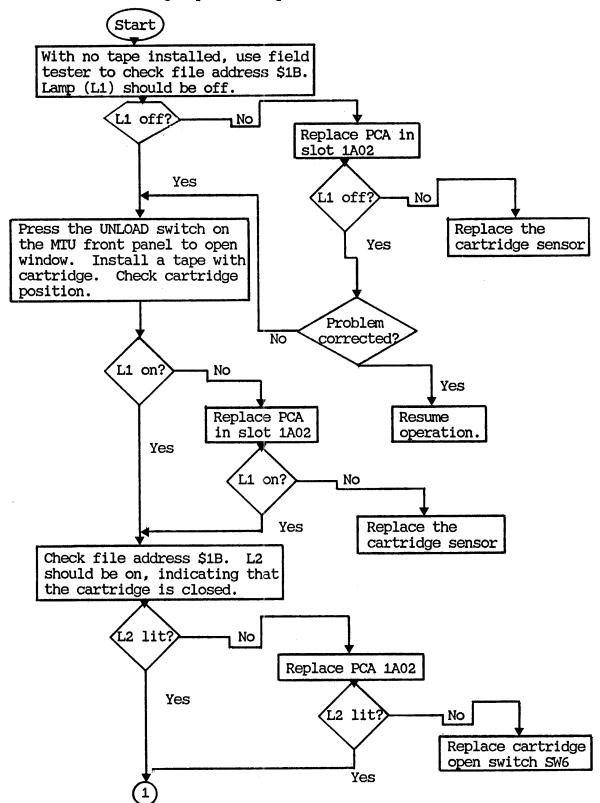


Figure A-8. Troubleshooting Error Code 31.

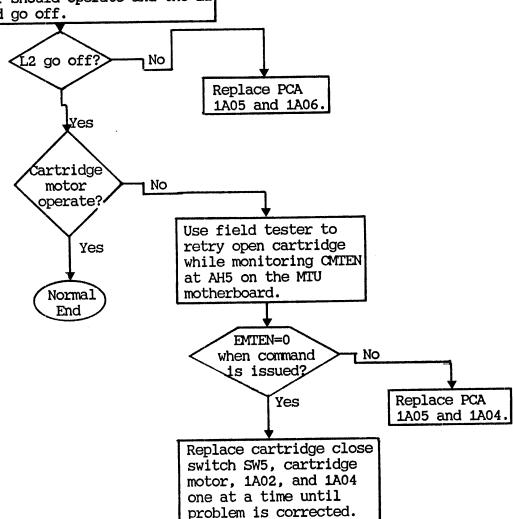
A0120 MTU TROUBLE SHOOTING

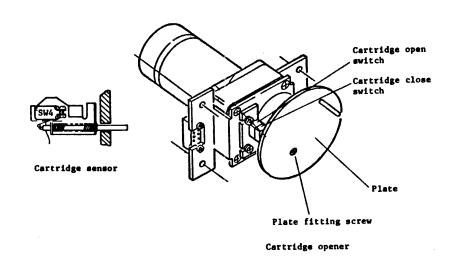
Error Code 41. Cartridge open/close problem.





Check file address \$04. L2 should be on. Set field tester switches to \$1B (open cartridge) and toggle SSS. The cartridge opener should operate and the L2 should go off.





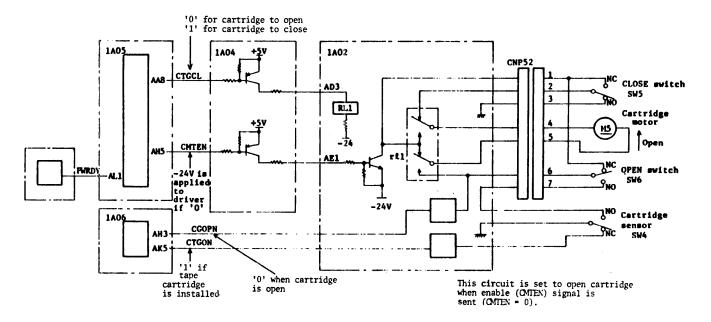
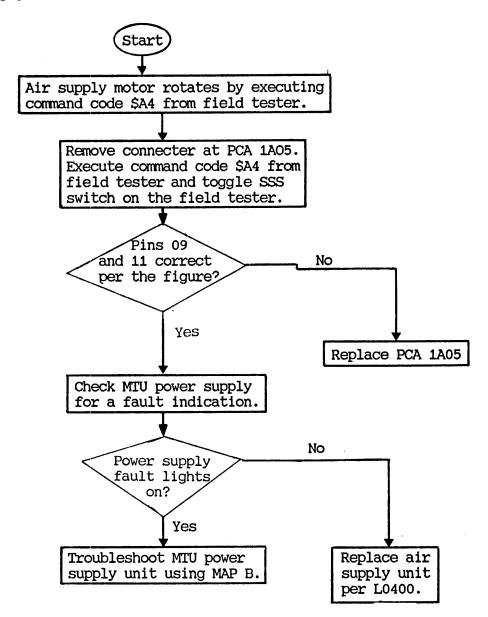
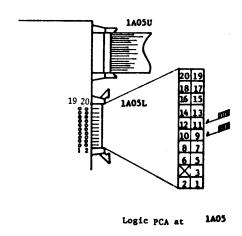


Figure A-9. Troubleshooting Error code 41.

Air Supply Motor Problem





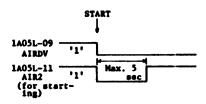
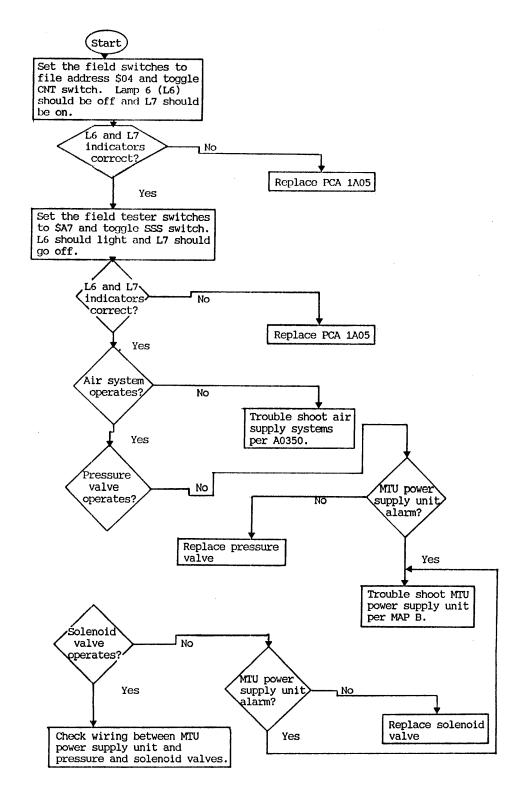
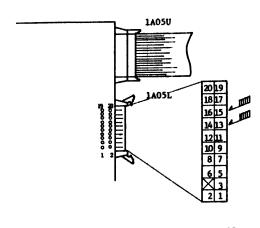


Figure A-10. Timing chart.

Pressure and Solenoid Valves problem.





Logic PCA at 1A05

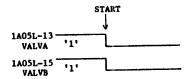
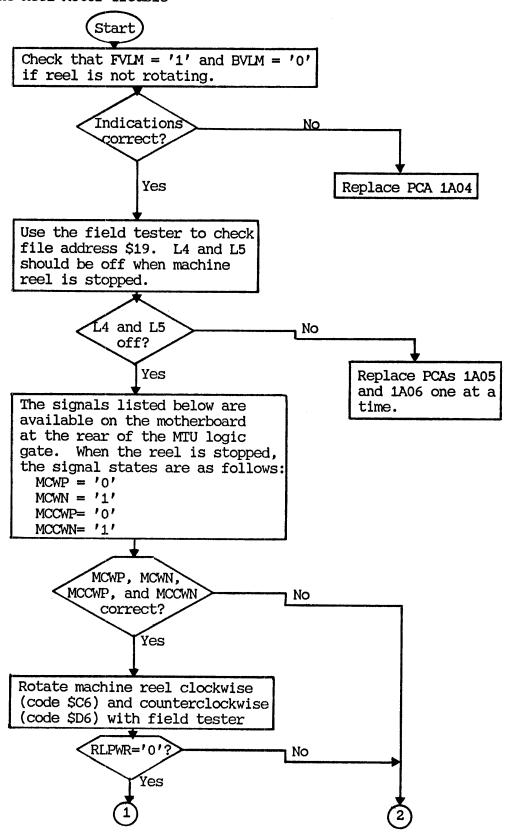


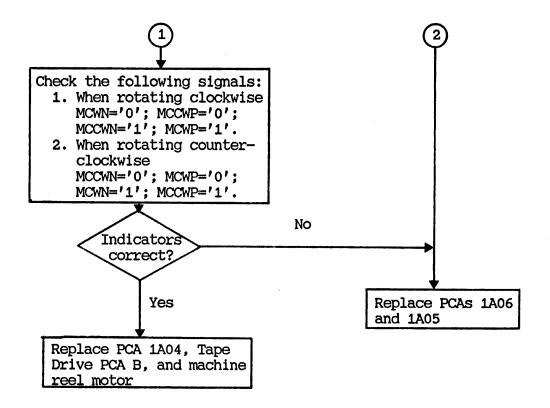
Figure A-11. Timing chart.

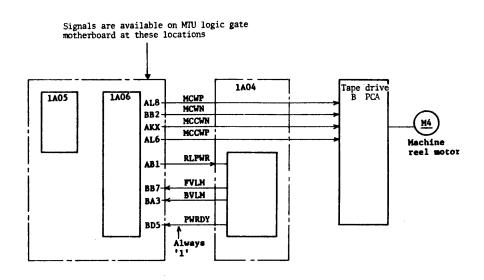
A0140 MTU TROUBLE SHOOTING

Machine Reel Motor Trouble



A0140 MTU TROUBLE SHOOTING





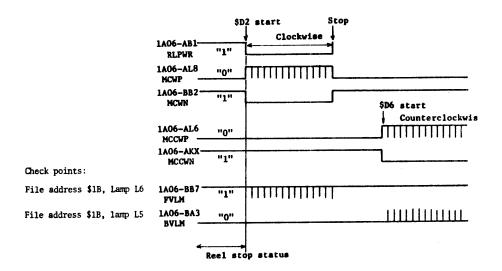
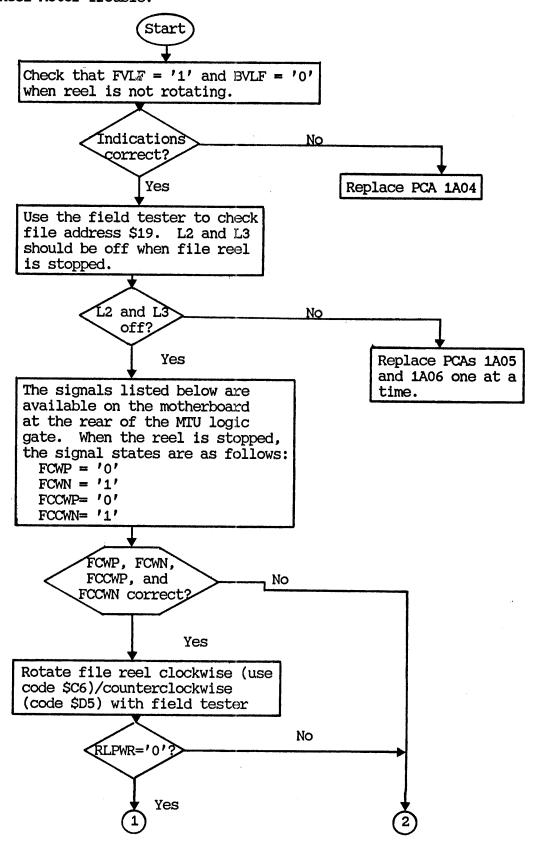


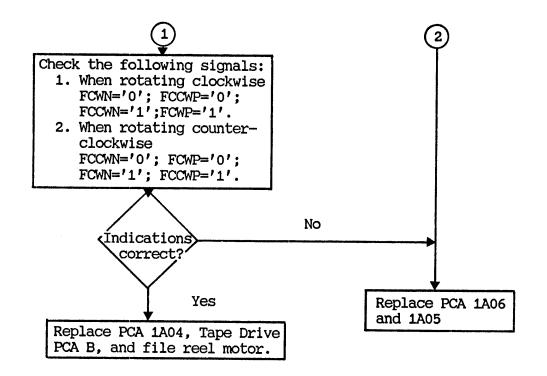
Figure A-12. Machine reel motor troubleshooting.

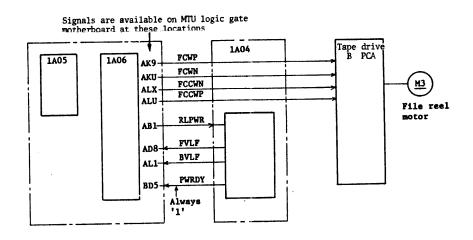
A0141 MTU TROUBLESHOOTING

File Reel Motor Trouble.



B03P-5280-0341A...02A





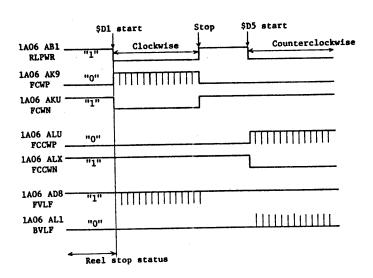
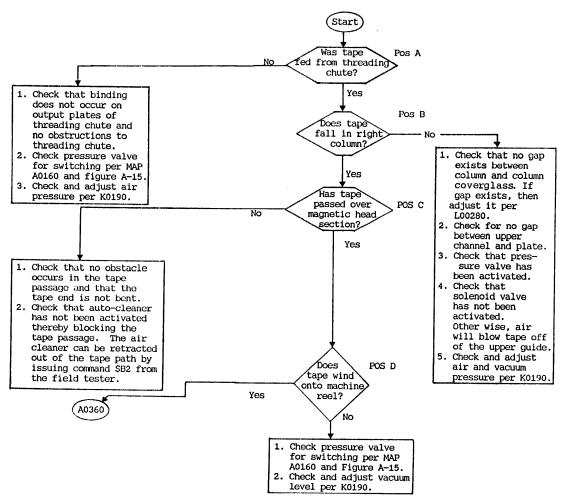


Figure A-13. File reel motor troubleshooting.

Tape does not Wind onto the Machine Reel.



Note:

- Tape does not wind onto machine reel even though it has been loaded from file reel.
- (2) See accompanying figure for referenced tape positions (pos).

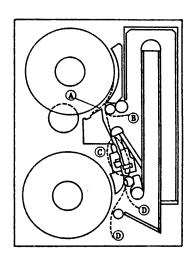
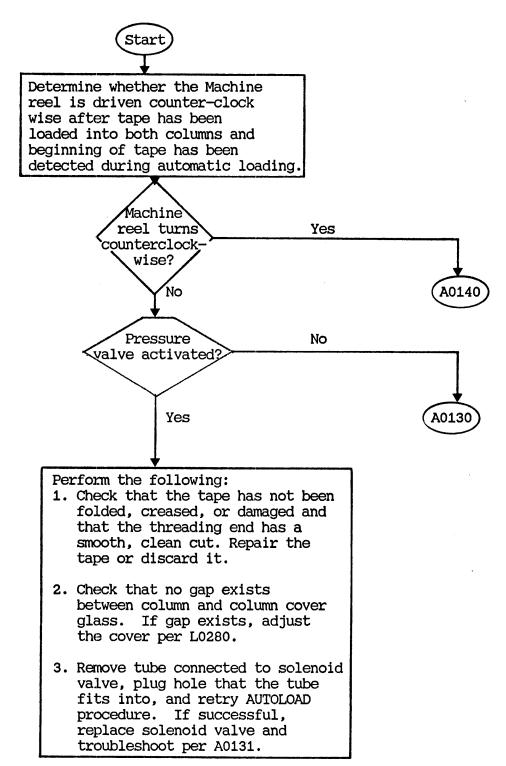


Figure A-14.

Tape in Vacuum Column Problem.



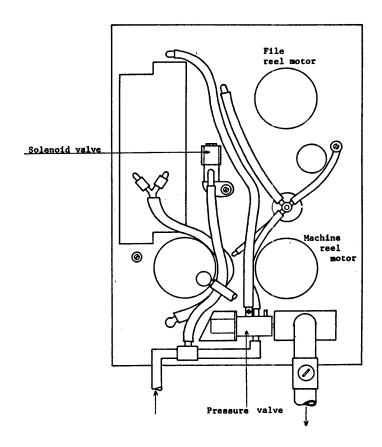
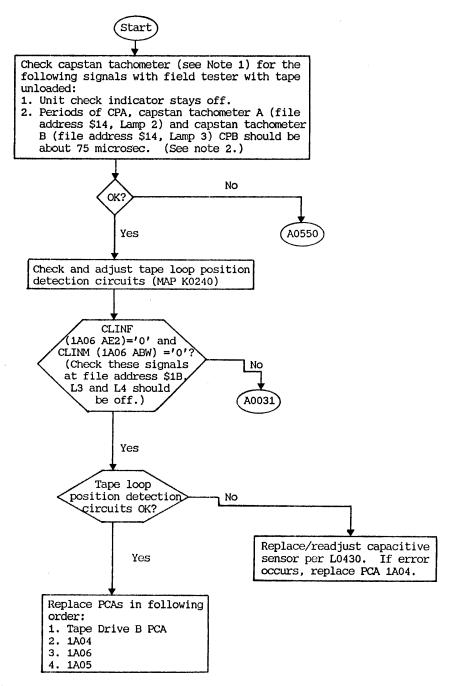


Figure A-15.

A0170 MTU TROUBLE SHOOTING

Error Codes 60, 61, 62, and 63. Tape Loop Alarm

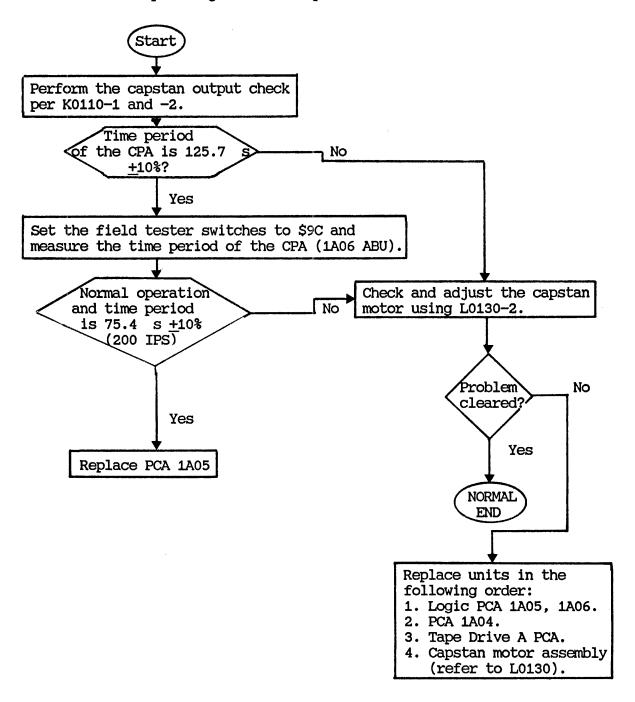


Notes:

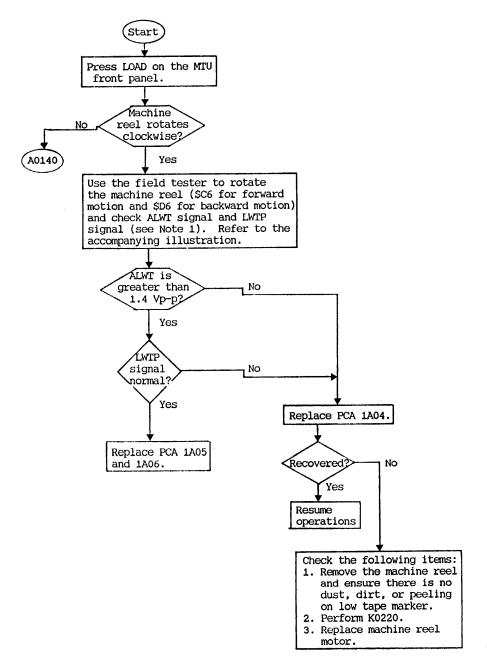
- (1) The unit check signal can be monitored at file address \$04, bit 0.
- (2) CPA and CPB can also be monitored at AA6 using an oscilloscope and AB6 at the MTU logic gate motherboard, respectively.
- (3) A complete checkout of the capstan and tape loop is contained in K0110 and K0240.

A0180 MTU TROUBLESHOOTING

Problem while operating at normal speed



Error code 42. Low tape marker detection problem.



Note:

(1) Signals can be monitored at the MTU logic gate motherboard.

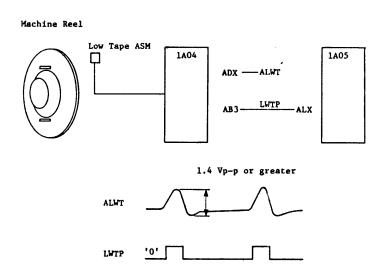
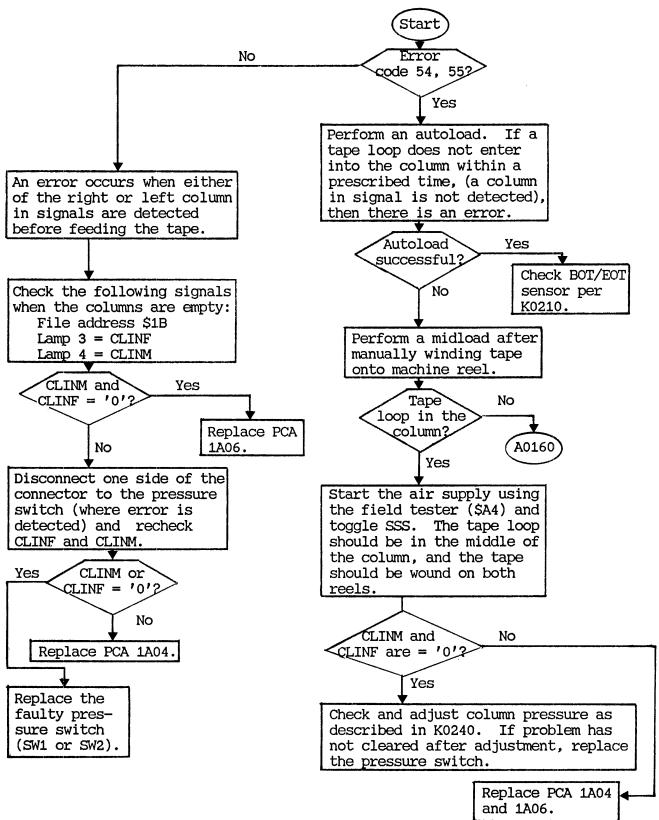


Figure A-16. Troubleshooting Error Code 42.

A0310 MTU TROUBLESHOOTING

Error Codes 46, 47, 54, or 55.



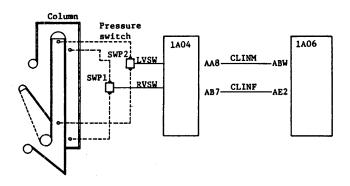
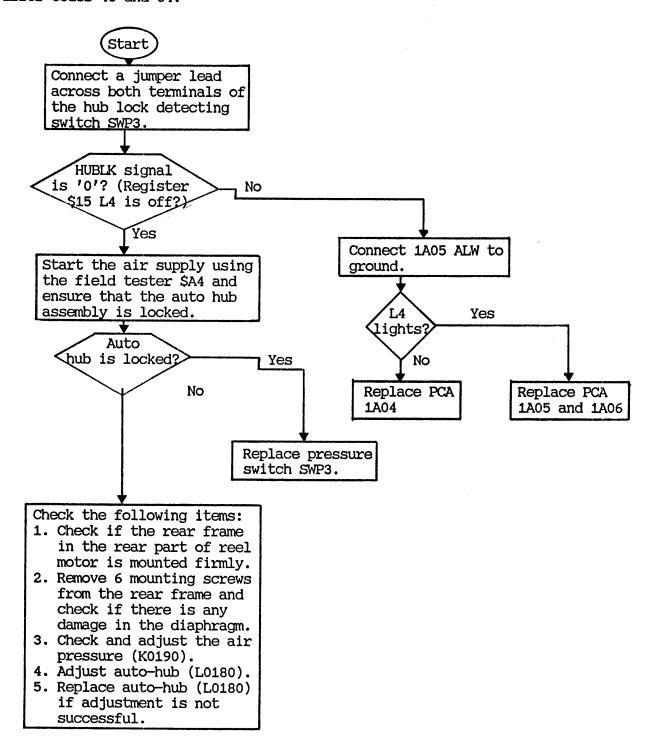


Figure A-17. Troubleshooting Error Codes 46, 47, 54, and 55.

Error Codes 43 and 64.



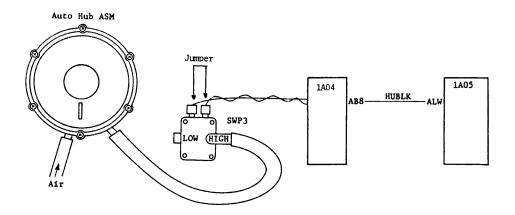
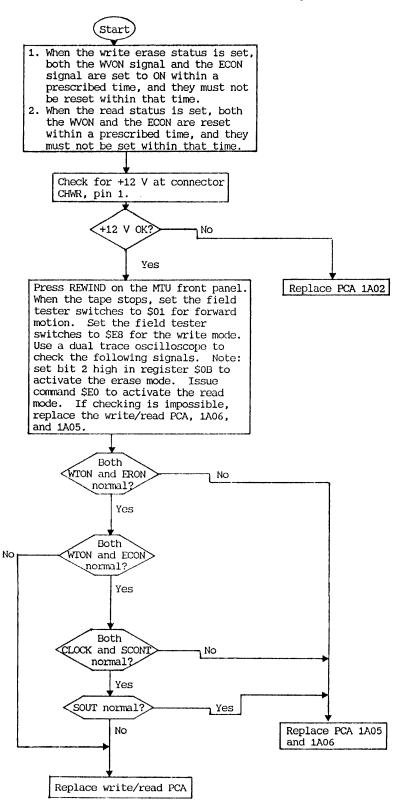
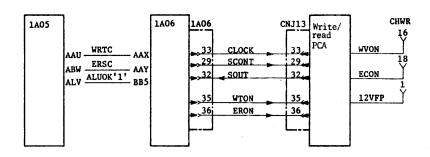
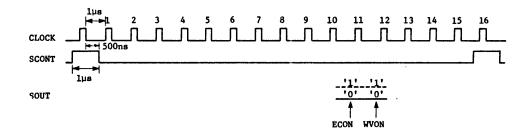


Figure A-18. Troubleshooting Error Codes 43 and 46.

Error Codes 80, 81, 82, 83, and 84. Abnormality in Write/Read Status.







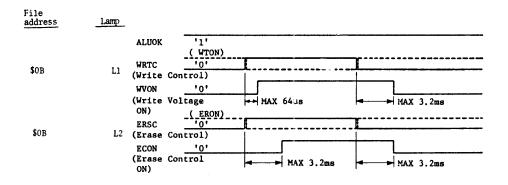
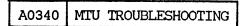
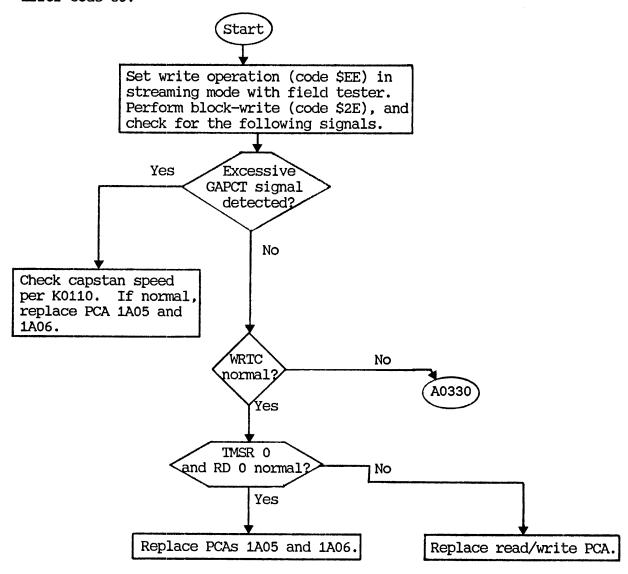


Figure A-19. Troubleshooting Error Codes 80 through 84.



Error Code 85.



Notes:

- (1) An error results if no IBG (inter-block gap) is detected within a specified distance. Write voltage is normally set to ON within the IBG when writing data in the streaming mode.
- (2) Signals can be accessed on the MTU logic gate motherboard.

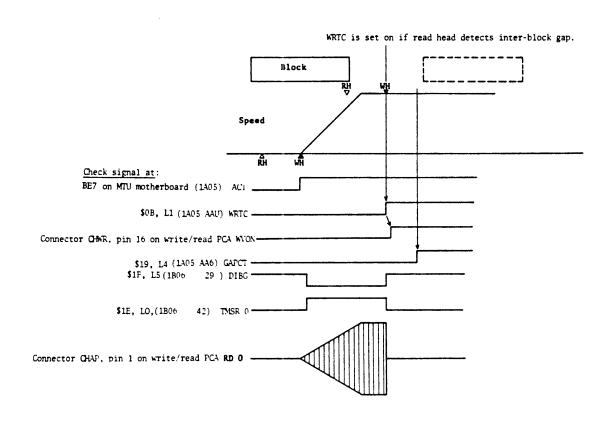
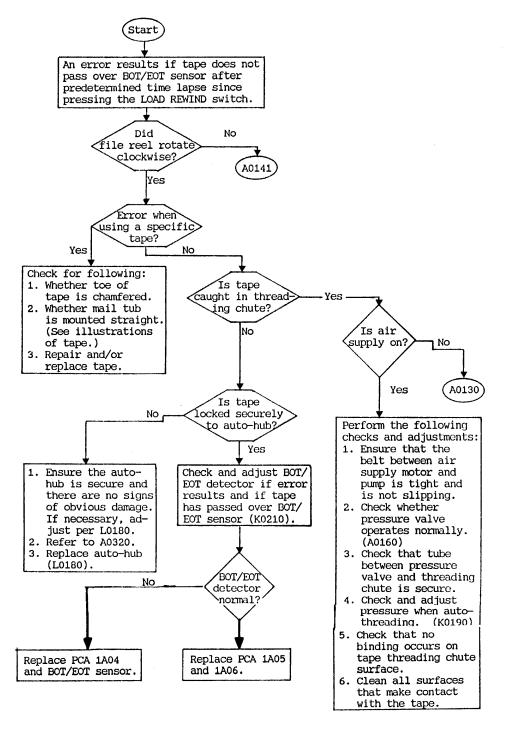


Figure A-20. Troubleshooting Error Code 85.

A0350 MTU TROUBLESHOOTING

Error Code 49. Tape did not reach BOT sensor.



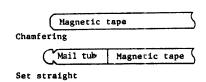


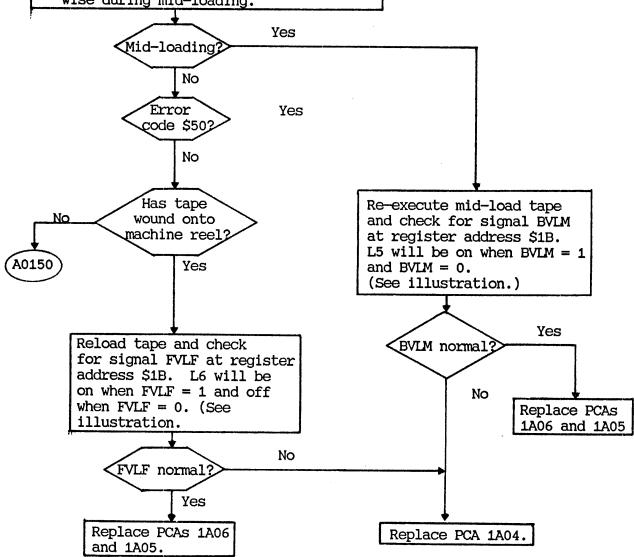
Figure A-21. Tape rim end.

Error Codes 50 and 51.



An error is detected if:

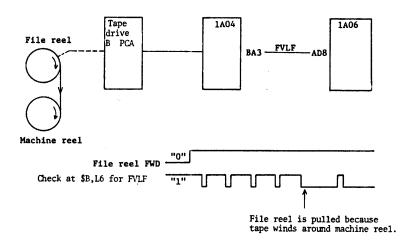
- 1. Reel loaded signal (FVLF) is detected before BOT/EOT.
- No reel loaded signal is detected after predetermined elapsed time after tape passed over BOT/EOT sensor during autoloading.
- 3. Reel loaded signal (BVLM) is detected before file reel rotates counterclock-wise during mid-loading.



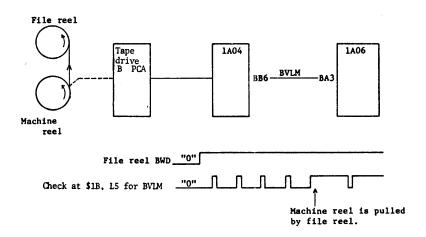
Notes: FVLF: Forward voltage limit file.

BVLM: Backward voltage limit machine.

FVLF: Forward Voltage Limit File
BVLM: Backward Voltage Limit Machine



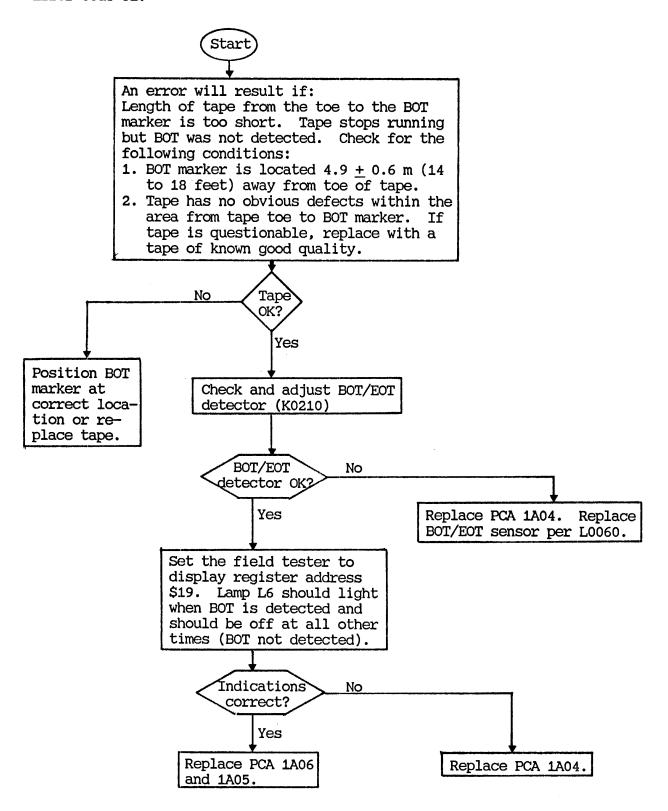
Reel loaded check when auto-loading



Reel loaded check when mid-loading.

Figure A-22. Reel loaded check when mid-loading.

Error Code 52.



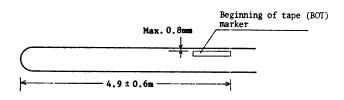
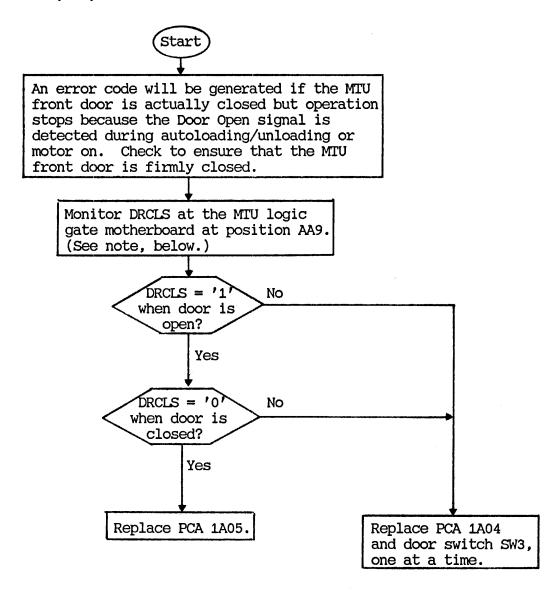


Figure A-23. Trouble shooting error code 52.

A0420 MTU TROUBLESHOOTING

Error codes 35, 40, and 65.



Note:

See A0020, Figure A-1 for pin location on the MTU motherboard.

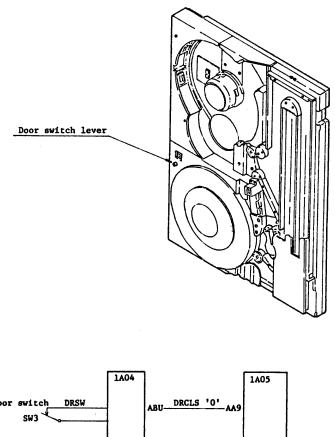
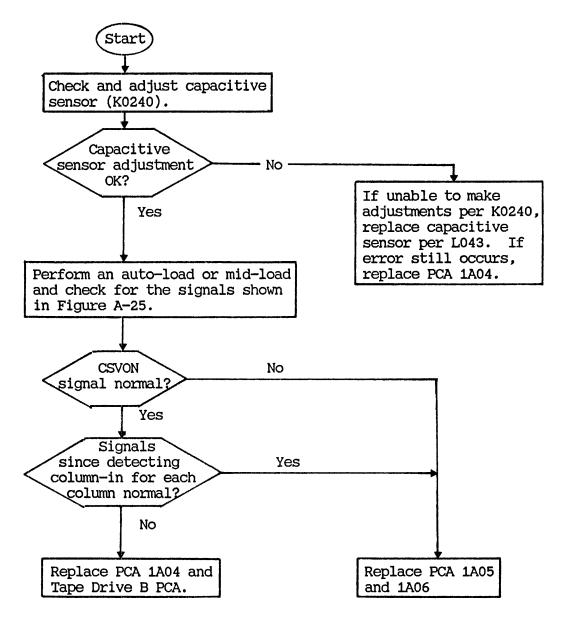


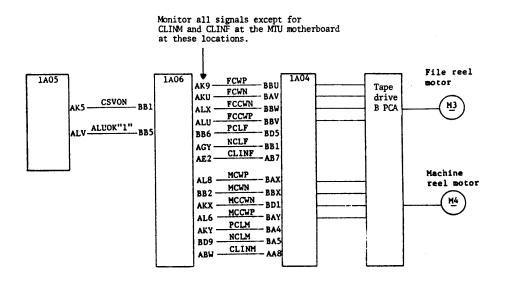
Figure A-24. Troubleshooting Error Code 35, 40, and 65.

A0420 MTU TROUBLESHOOTING

Error Codes 56 and 57.



Note: An error results if the tape loop passes the warning detection hole after the column-in signal (tape in vacuum column) has been detected during loading.



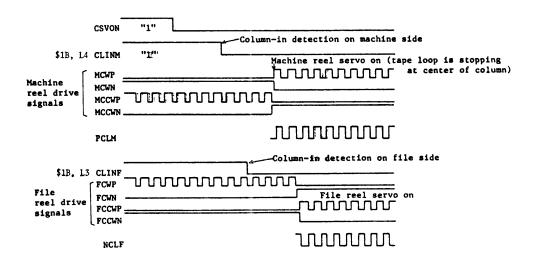
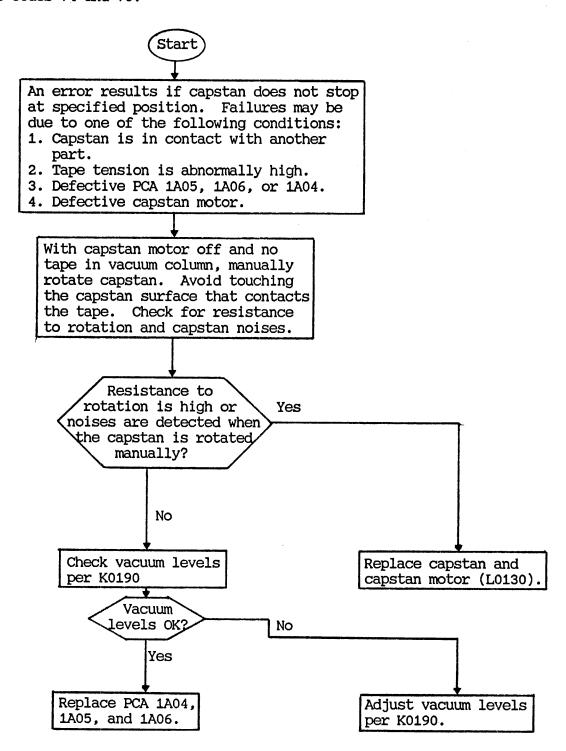


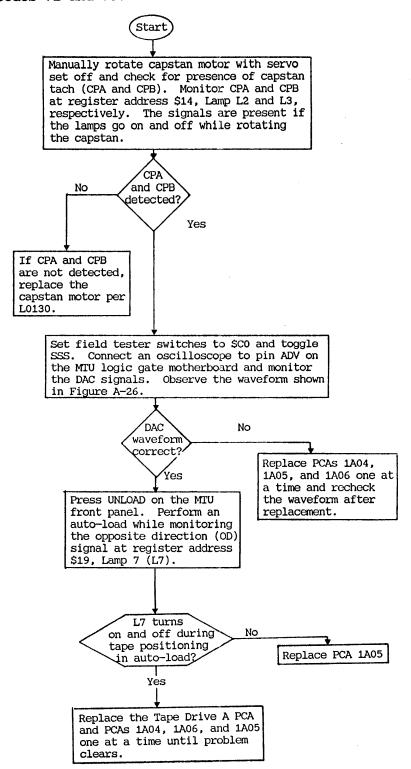
Figure A-25. Troubleshooting Error Code 56 and 57.

Error codes 74 and 75.



A0500 MTU TROUBLESHOOTING

Error codes 72 and 73.



Note: See A0020, Figure A-1 for ADV pin location on the MTU motherboard.

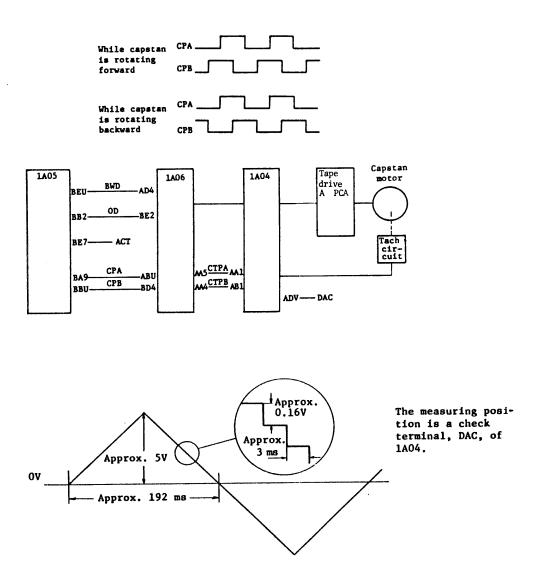
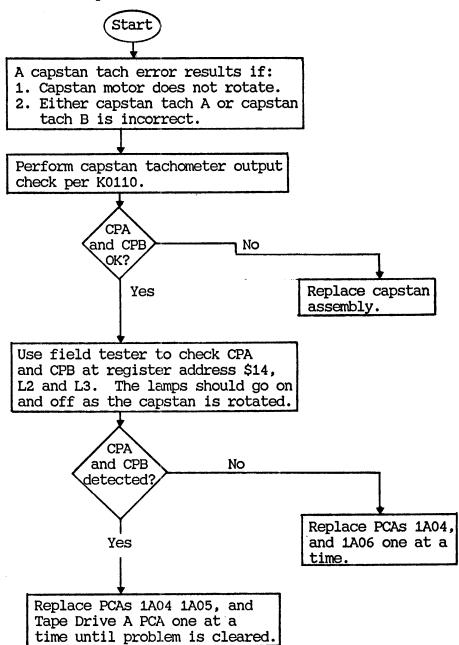


Figure A-26. Troubleshooting Error Code 72 and 73.

A0550 MTU TROUBLESHOOTING

Error Codes 70 and 71. Capstan Tach Error



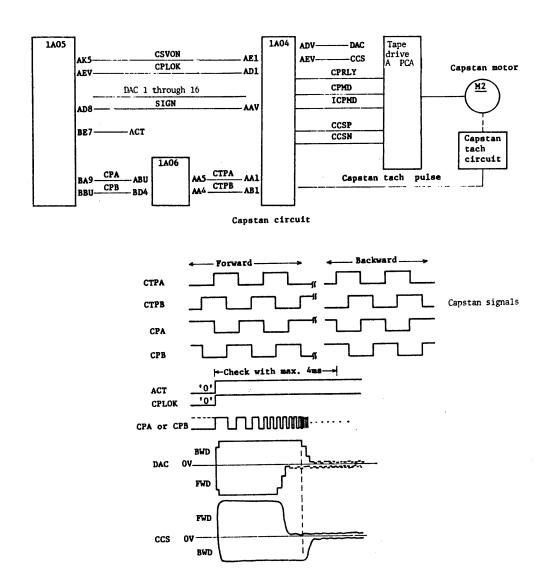
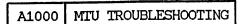
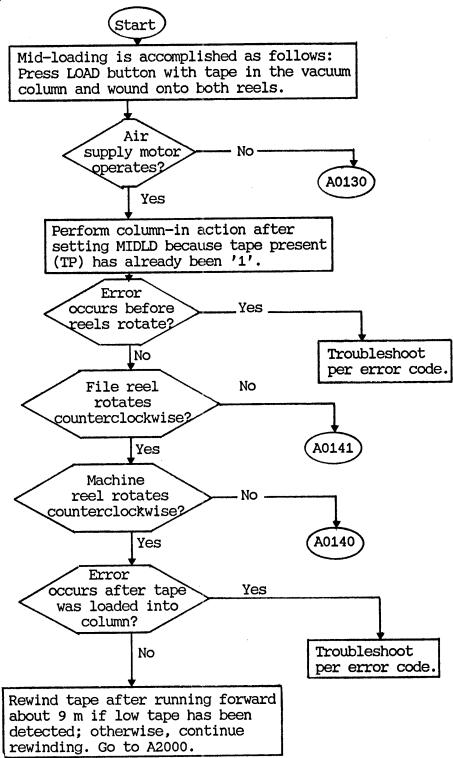
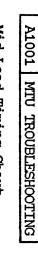


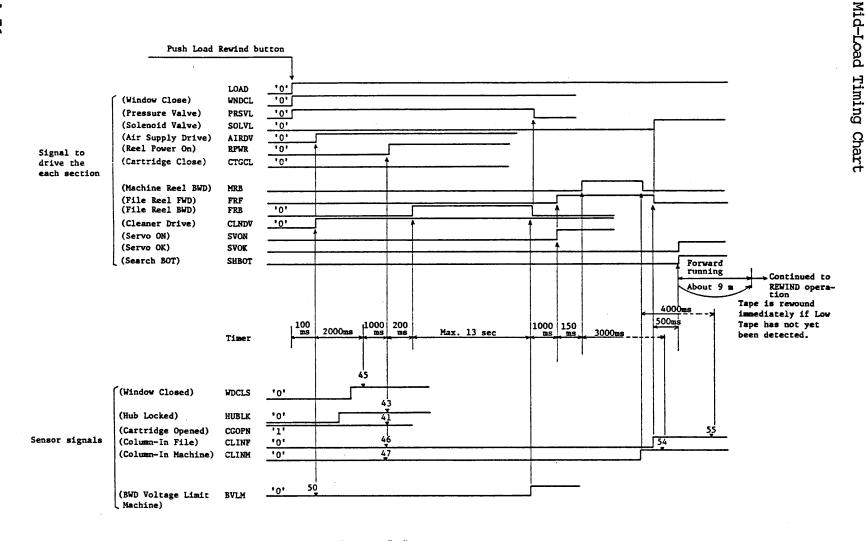
Figure A-27. Capstan circuit and signals.



Mid-Loading Trouble



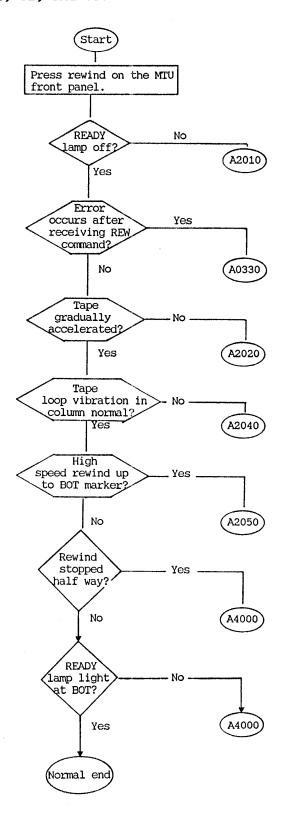




Note: The marks " • " indicate the timings when the program checks the logical level of sensors during mid-loading. The hexadecimal number in upper of the mark " • " means Error code which is set to ER register.

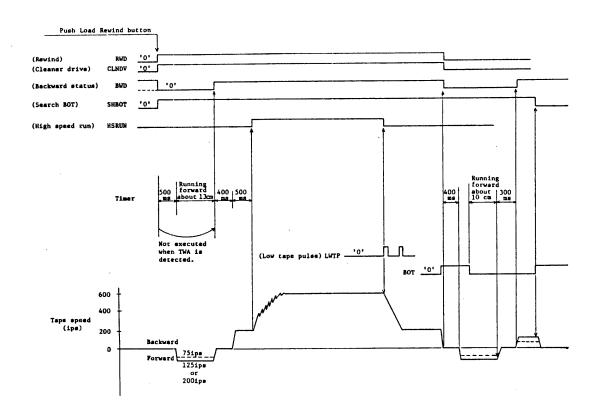
A2000 MTU TROUBLESHOOTING

Error Codes 60, 61, 62, and 63.

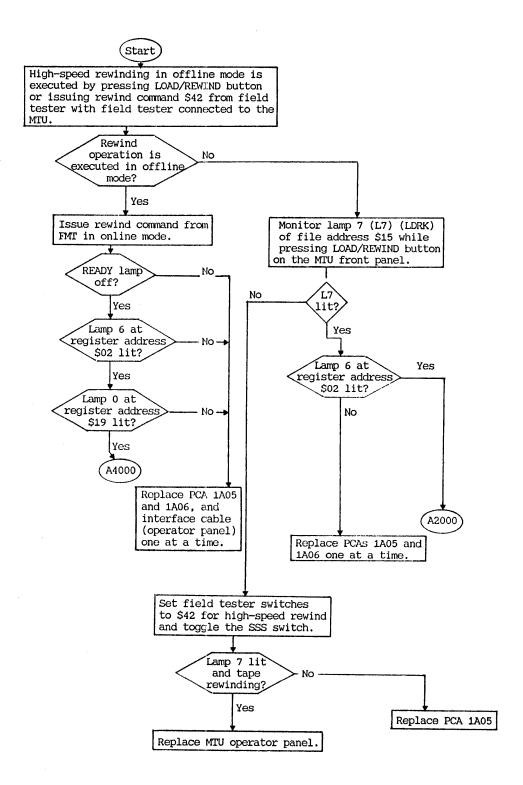


A2001 MTU TROUBLESHOOTING

Rewind Timing Chart

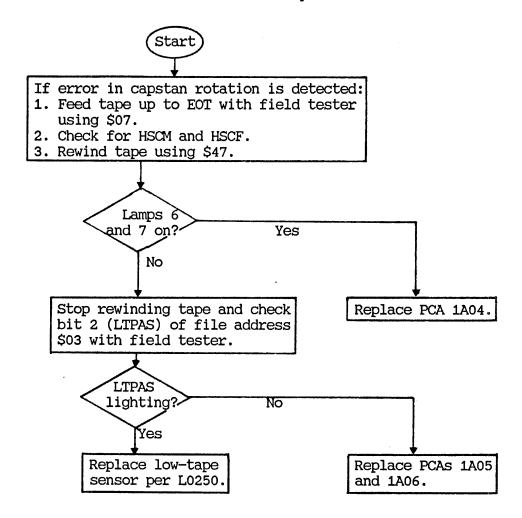


No Rewind Operation is Performed



A2020 MTU TROUBLESHOOTING

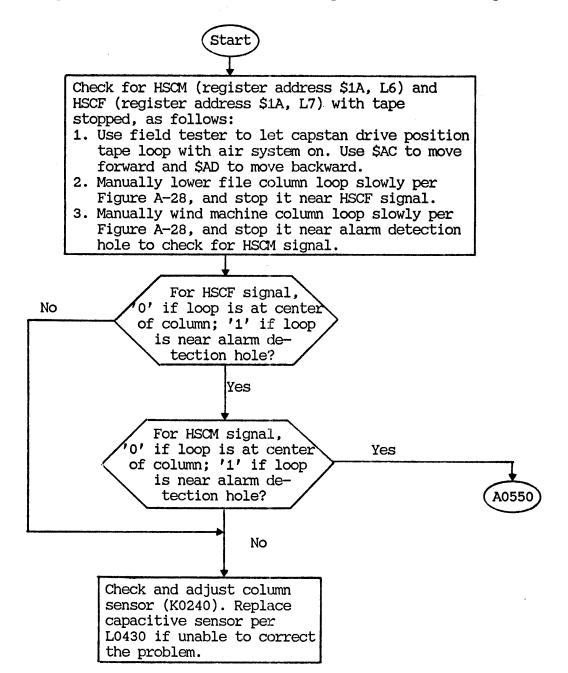
Capstan Rotation does not Accelerate Gradually



Notes: If tape warning area (TWA) signal has not been detected, tape is wound forward about 13 cm at constant speed, then runs backward for 0.5 seconds at 200 ips. Tape speed then increases to 600 ips or 500 ips. However, forward running will not occur if TWA has been detected.

A2040 MTU TROUBLESHOOTING

Tape Loop Trouble in Columns (200 to 600 ips, and 600 to 200 ips)



Notes: After tape is rewound for 0.5 seconds at 200 ips, tape speed accelerates gradually by 40 ips per 100 ms if speed down signal (HSCM/HSCF) from reel controller does not become '1.' Speed decelerates gradually by 40 ips per 100 ms if speed down signal becomes '1.' If low tape marker is detected, then tape speed decelerates gradually at intervals of 100 ms.

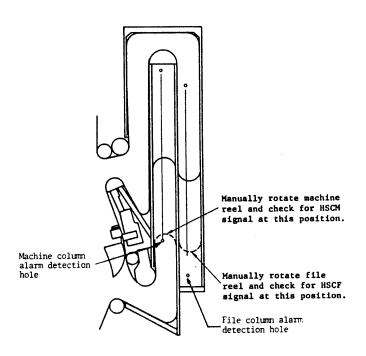
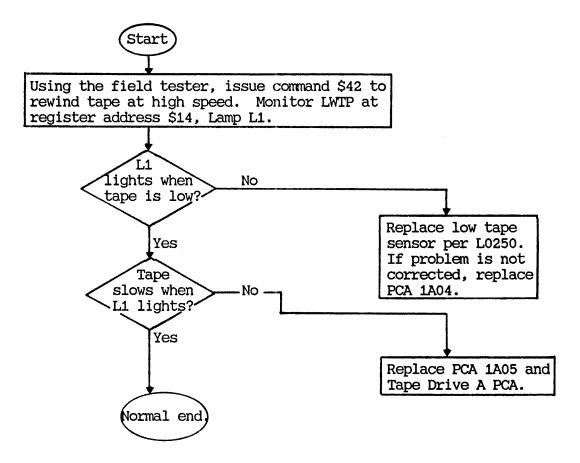


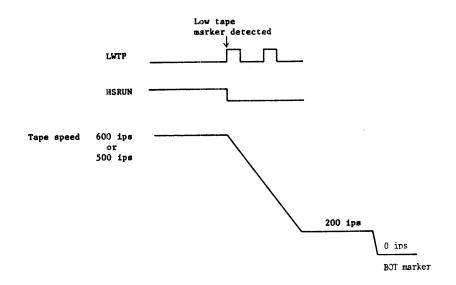
Figure A-28.

A2050 MTU TROUBLESHOOTING

Tape is Rewound at High Speed Until the BOT



Notes: If tape is rewound at high speed and runs low, then tape speed lowers from 600 or 500 ips to 200 ips until BOT is detected.



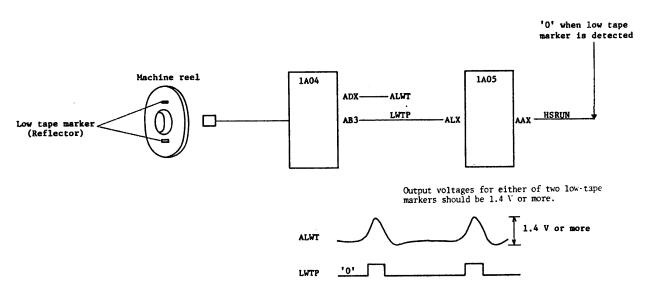
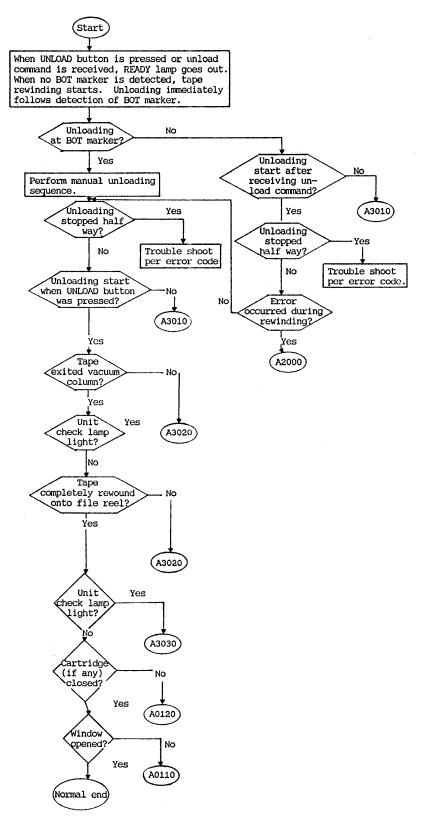
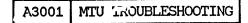


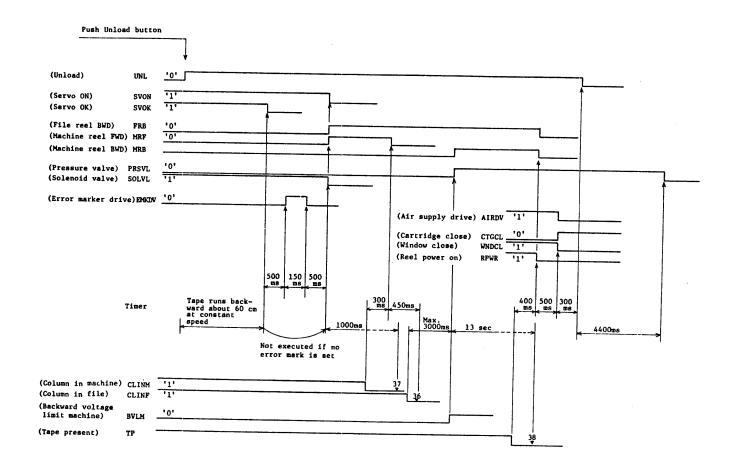
Figure A-29.

Trouble During Unloading



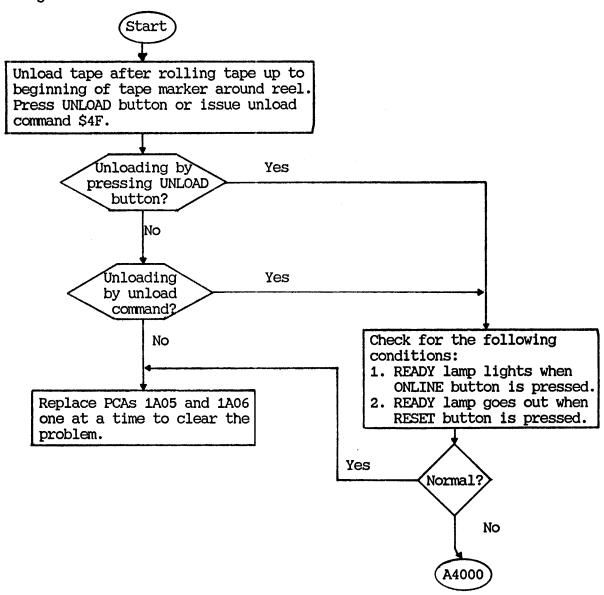


Unload Timing Chart



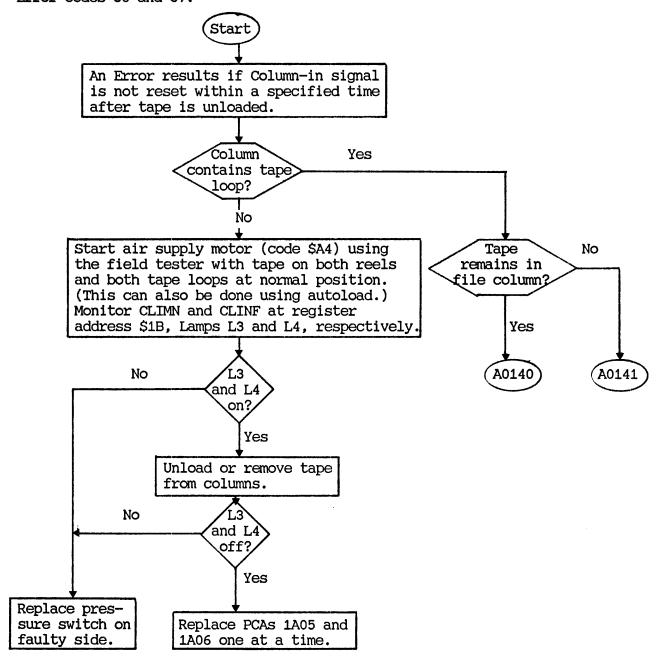
A3010 MTU TROUBLESHOOTING

Unloading Failure



A3020 MTU TROUBLESHOOTING

Error Codes 36 and 37.



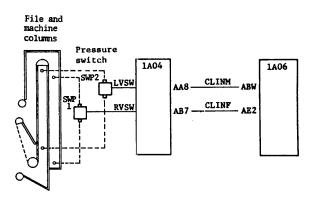
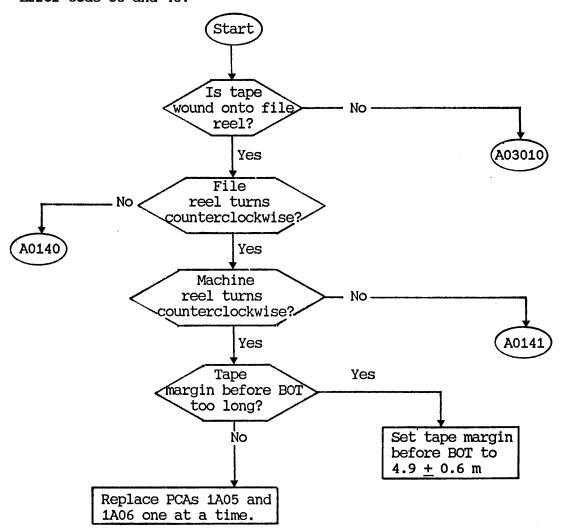


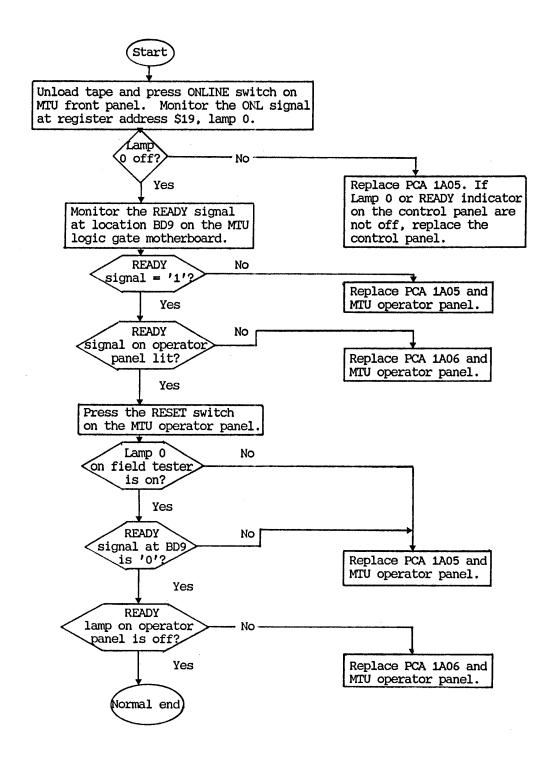
Figure A-30. Troubleshooting Error Codes 36 and 37.

A3030 MTU TROUBLESHOOTING

Error Code 38 and 48.



Ready Troubleshooting



Notes: After loading magnetic tape:

- 1. When ONLINE button is pressed, ONL (online) is set to '0' and
- READY is set to '1', then READY lamp lights.
 When RESET button is pressed, ONL is set to '1' and READY is set to '0', then READY lamp goes out.

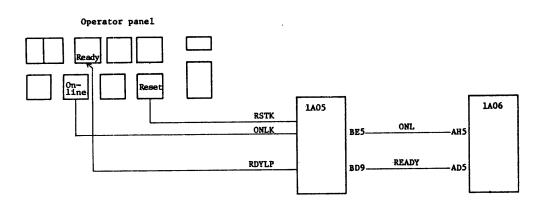
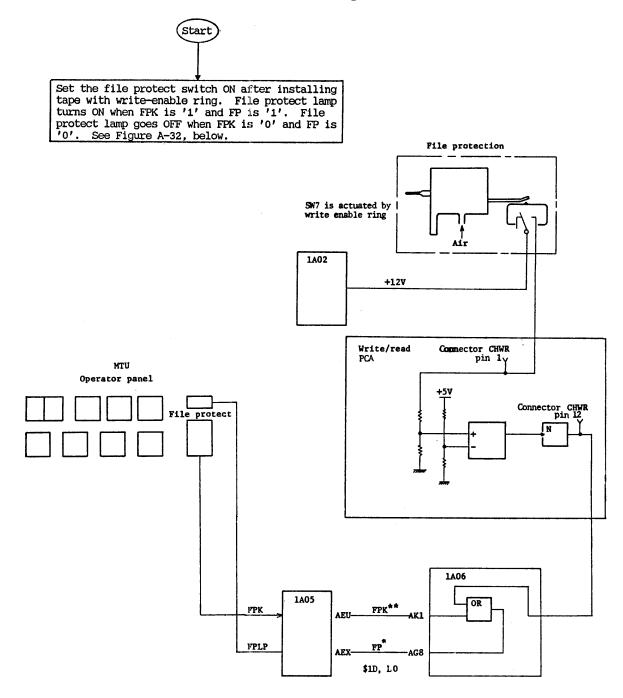


Figure A-31. Ready troubleshooting.

A5000 MTU TROUBLESHOOTING

Error Codes 86 and 87. File Protection and Lamp Trouble



SWRS (Set write status), SERS (Set erase status), WRTC (Write control) and ERSC (Erase control) are reset in idling routine of microprogram, by FP (File Protect).

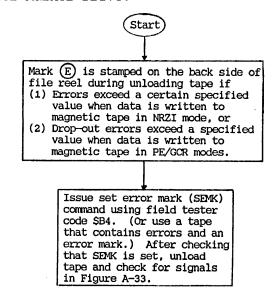
Figure A-32. File protection and lamp troubleshooting.

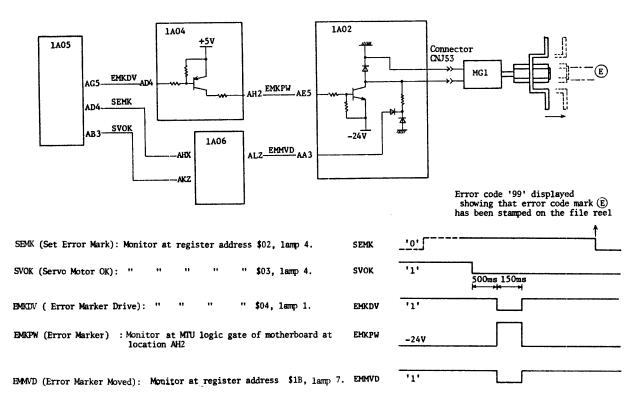
Notes:

- SWRS (set write status), SERS (set erase status), WRTC (write control), and ERSC (erase control) are reset by FP (file protect).
 Monitor FP at register address \$1D, Lamp 0 using the field tester.
 Monitor FPK at the MTU logic gate motherboard at location AEU.

A6000 MTU TROUBLESHOOTING

Error Code 30. Error Marker Drive.





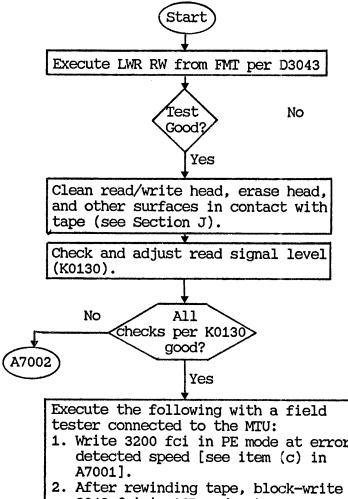
```
1 SEMK (set error mark): Monitor at register address $02, lamp L4.
2 SVOK (servo motor OK): Monitor at register address $03, lamp L4.
3 EMKDV (error marker drive): Monitor at register address $04, lamp L1.
4 EMKPW (error marker drive): Monitor at MTU logic gate motherboard at location AH2.
```

(5) EMMVD (error marker moved): Monitor at register address \$1B, lamp L7.

Figure A-33.

A7000 MTU TROUBLESHOOTING

Read/Write Troubleshooting Procedures

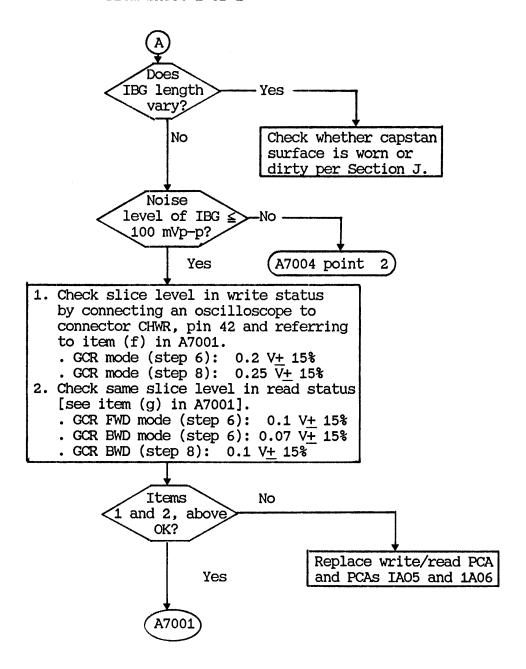


1. Write 3200 fci in PE mode at error

- 9042 fci in GCR mode at same speed [see item (d) in A7001].
- 3. After rewinding tape, read tape written at in GCR mode at same speed. Use an oscilloscope to check terminals CHAJ, pin 1 to CHAR, pin 1 on the write/read PCA [see item (e) in A7001].

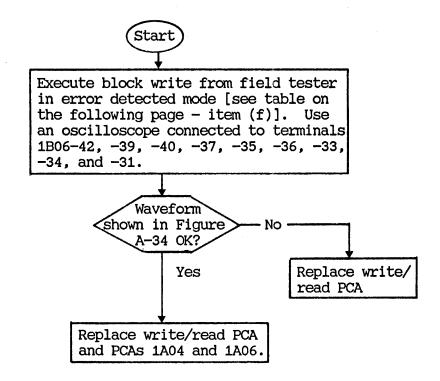
Continued on sheet 2 of 2

From sheet 1 of 2



A7001 MTU TROUBLESHOOTING

Read/Write Troubleshooting



A7001 MTU TROUBLESHOOTING

Item	Operation	Procedure	Field tester Code	Setting switch	Remarks
(a)	Write mode	1	Low speed PE : \$E8 Low speed GCR : \$EA High speed PE : \$EC High speed GCR: \$EE	SSS	
(b)	Read mode	1	Low speed PE : \$E0 Low speed GCR : \$E2 High speed PE : \$E4 High speed GCR: \$E6	SSS	
(c)	PE 3200 fci write	1	Set to PE write mode at item (a)	SSS	
		2	\$89	SSS	
(d)	Block write	1	Set to write mode specified at item (a)	SSS	
		2	\$25	SSS	
(e)	FWD read	1	Set to read mode specified at item (b)	SSS	
		2	Low speed: \$01 High speed: \$02	SSS	
(f)	GCR write mode with specified step	1	Step specification: Step 6: \$C6 Step 8: \$C8	Toggle SSS switch twice	First toggle causes tape to run; second causes tape to stop
		2	Low speed GCR write: SEA	SSS	
(g)	GCR read mode with specified step	1	Step/running direction specification: FWD step 6: \$C6 FWD step 8: \$C8 BWD step 6: \$D6 BWD step 8: \$D8	Toggle SSS switch twice	First toggle causes tape to run; second causes tape to stop

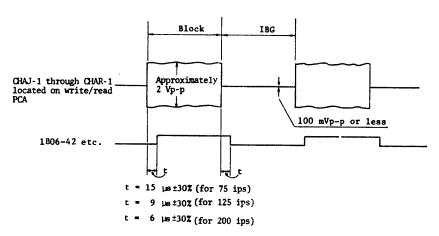
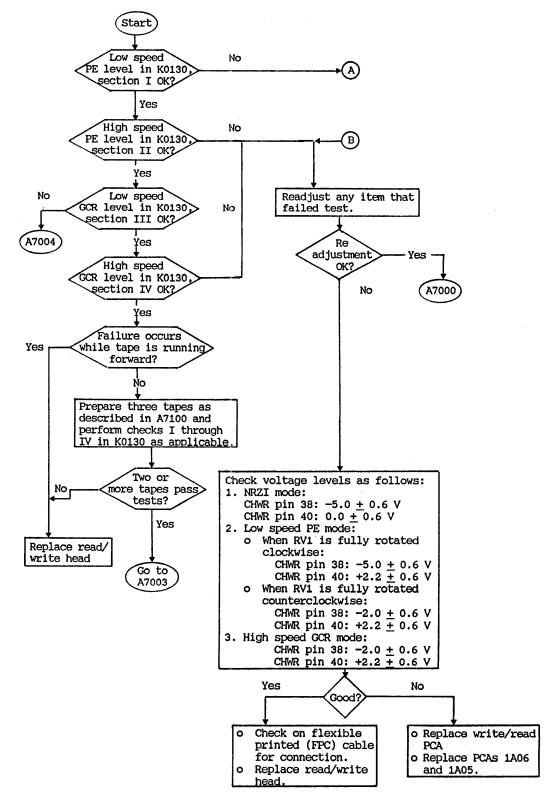
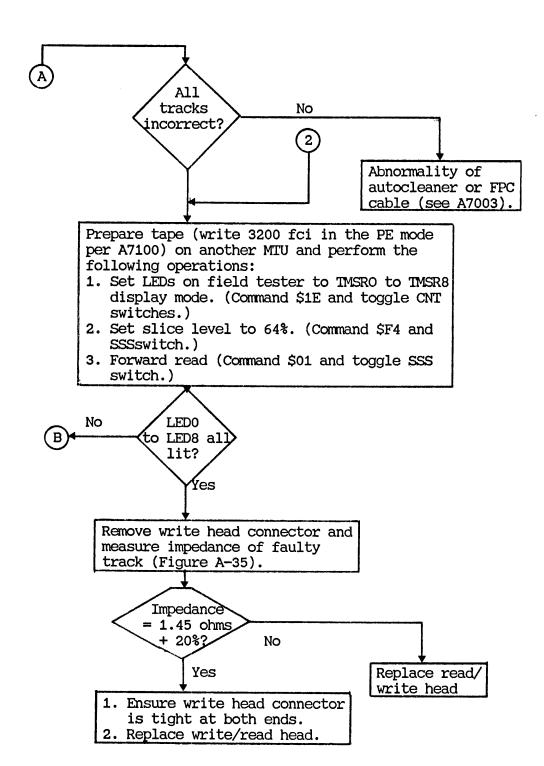


Figure A-34. Read/write troubleshooting.

Abnormality for Read Level



Flexible printed cable



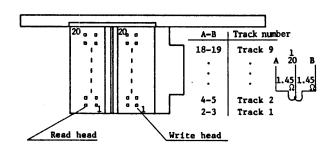
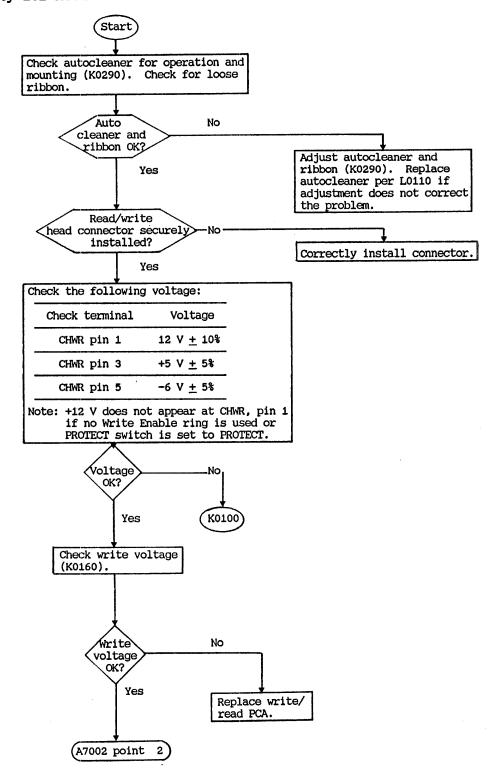


Figure A-35. Read/write head (viewed from head connector side).

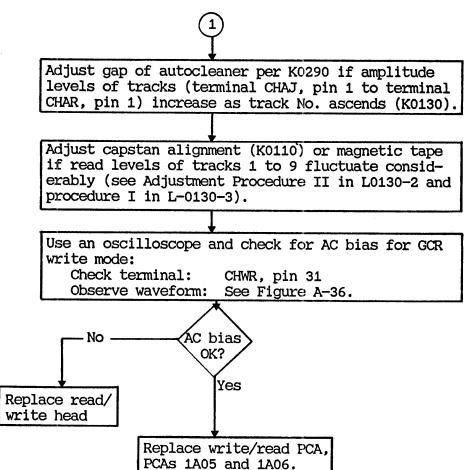
A7003 MTU TROUBLESHOOTING

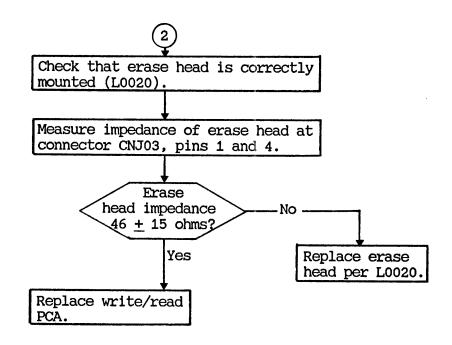
Abnormality for Read Level



A7004 MTU TROUBLESHOOTING

Abnormality for Read Level





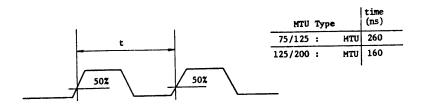
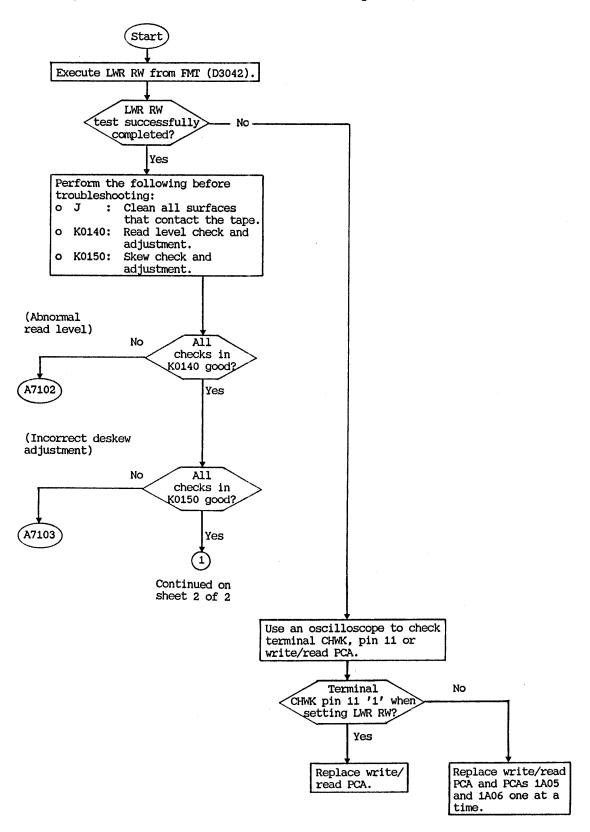


Figure A-36. AC bias waveform (CHWR pin 31).

Troubleshooting for Read/Write Section (1600/800 rpi MTU)

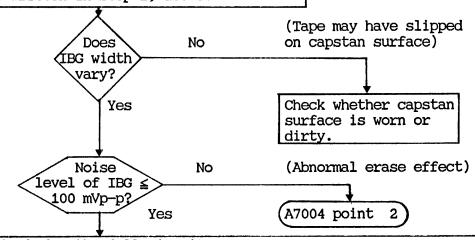


Continued from sheet 1 of 2



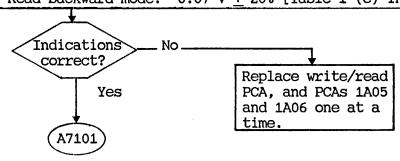
Refer to A7101, Table 1 while performing the following with field tester connected to MTU:

- 1. Write NRZI 800 fci at low speed [see Table 1 (c) in A7101]
- 2. Block write 3200 fci in PE mode at error detected speed after rewinding tape. Rewind tape by setting field tester switches to \$42.
- 3. Observe waveform at terminals CHAJ pin 2 and CHAR pin 2 on the read/write PCA while performing item (e) in A7101, Table 1. Use the same read mode that was written in step 2, above.



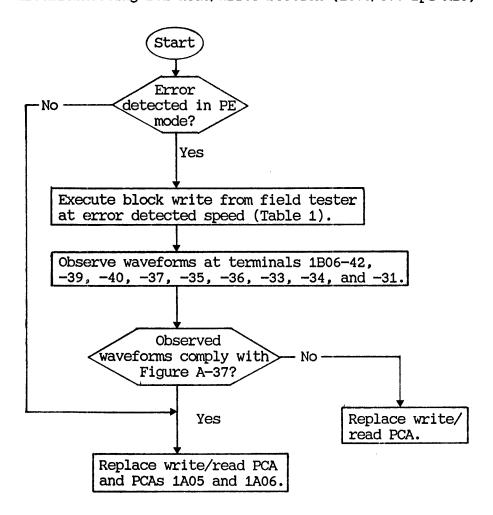
Check for the following items:

- 1. Check the slice level at terminal CHWR pin 44 in the read/write PCA in the NRZI mode:
 - . Write mode: 0.4 V + 20% [Table 1 (a) in A7101]
 - . Read mode: 0.17 V + 20% [Table 1 (b) in A7101]
- 2. Check the slice level at terminal CHWR, pin 42 in the read/write PCA in the PE mode:
 - . Write mode: $0.25 \text{ V} \pm 20\%$ [Table 1 (a) in A7101]
 - . Read forward mode: $0.10 \text{ V} \pm 20\%$ [Table 1 (e) in A7101]
 - . Read backward mode: 0.07 V + 20% [Table 1 (e) in A7001]



A7101 MTU TROUBLESHOOTING

Troubleshooting for Read/Write Section (1600/800 rpi MTU)



A7101 MTU TROUBLESHOOTING

Item	Operation	Procedure	Field tester Code	Switch	Remarks
(a)	Write mode	1	NRZI : \$E8 Low speed PE : \$EA High speed PE: \$EE	SSS	
(b)	Read mode	1	NRZI : \$E0 Low speed PE : \$E2 High speed PE: \$E6	SSS	
(c)	NRZI 800 fci write	1	\$89	SSS	
(d)	Block write	1	Set to write mode specified at item (a)	SSS	
		2	\$25	SSS	
(e)	FWD read action	1	Set to read mode specified at item (b)	SSS	Do not operate at high speed while in NRZI
		2	Low speed FWD: \$01 High speed FWD: \$02 Low speed BWD: \$41 High speed BWD: \$42	SSS	mode.

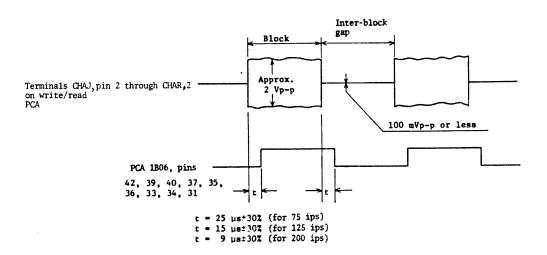
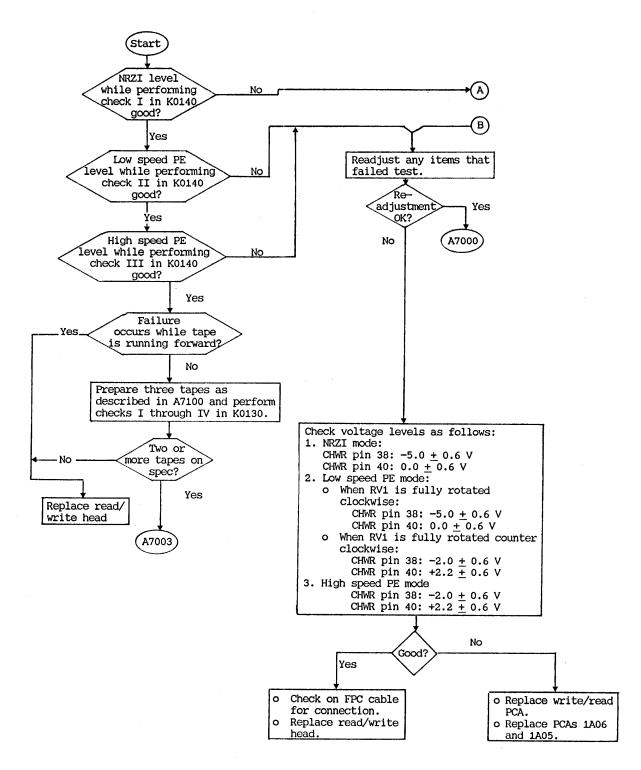


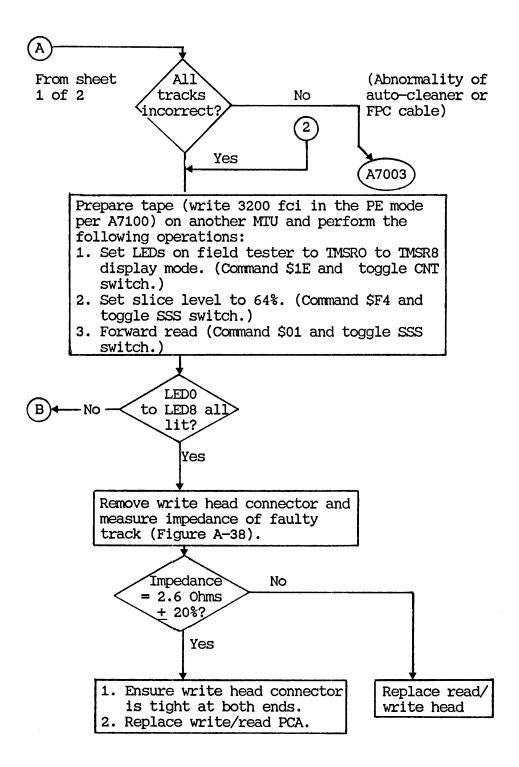
Figure A-37. Read/write troubleshooting.

A7102 MIU TROUBLESHOOTING

Abnormality for Read Level (1600/800 rpi MTU).

Note: Continued from A7100.





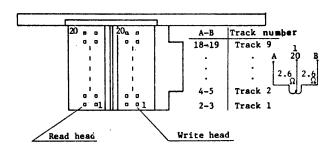
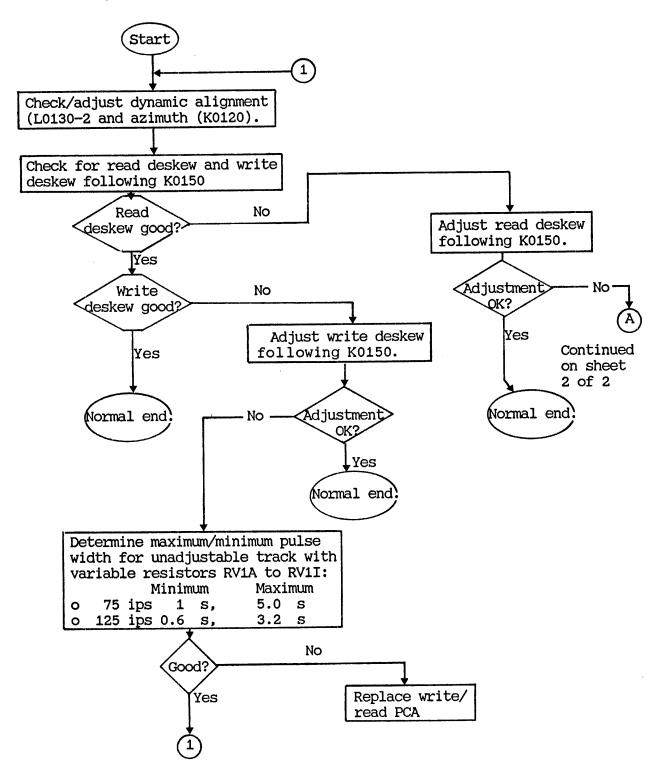


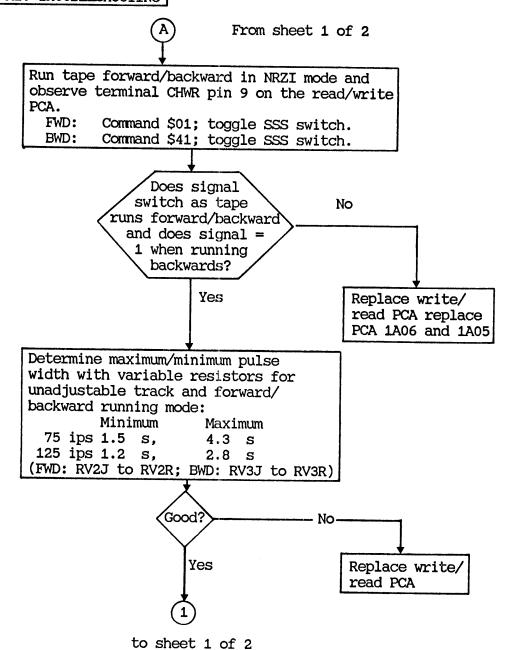
Figure A-38. Read/write head (viewed from head connector side).

A7103 MTU TROUBLESHOOTING

Abnormality for Read Level (1600/800 rpi MTU).



A7103 MTU TROUBLESHOOTING



B0000 POWER SUPPLY TROUBLESHOOTING

This section provides FMT and MTU power supply unit troubleshooting, MAP B0001 and B0100, respectively. Power supply troubleshooting includes power related problems that are actually outside of the power supply unit. For example, if an external device draws too much power, a power alarm will be generated. Alarm lights on the power supply unit front panel indicate that the cause of that alarm is external to the power supply. An illustration of each power supply unit front panel is included below for reference.

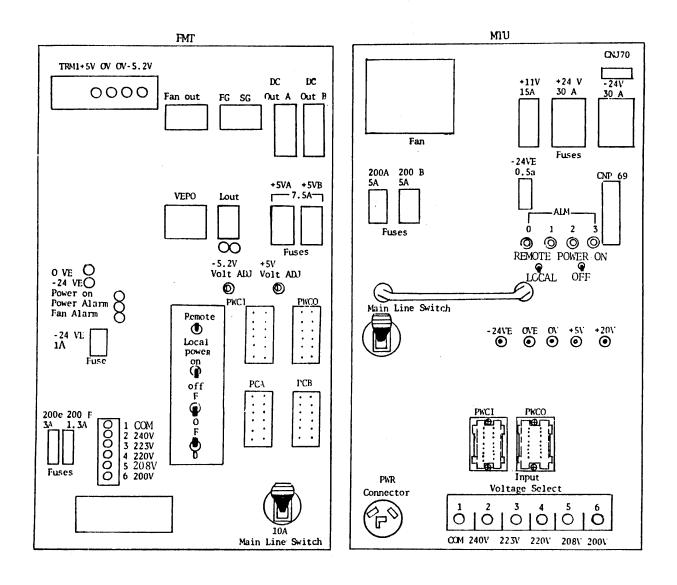
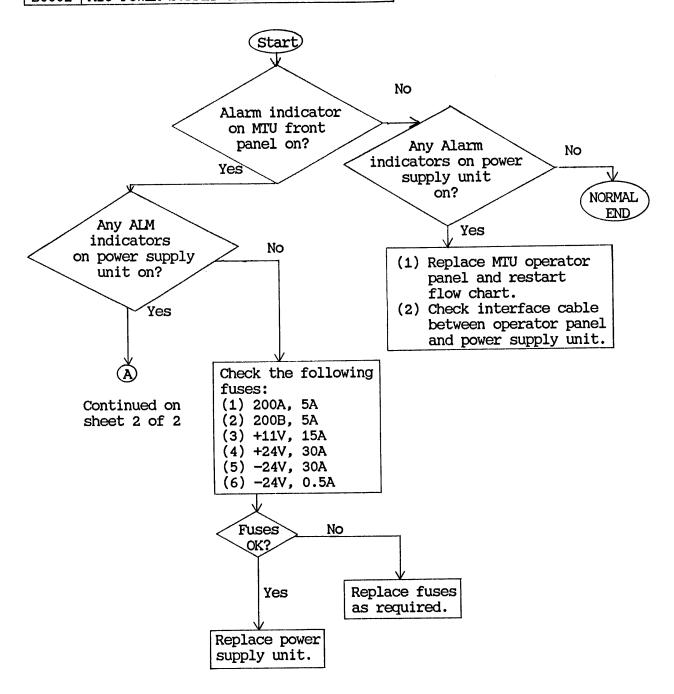


Figure B-1. FMT power supply unit. Figure B-2. MTU power supply unit.

B0001 MTU POWER SUPPLY UNIT TROUBLESHOOTING



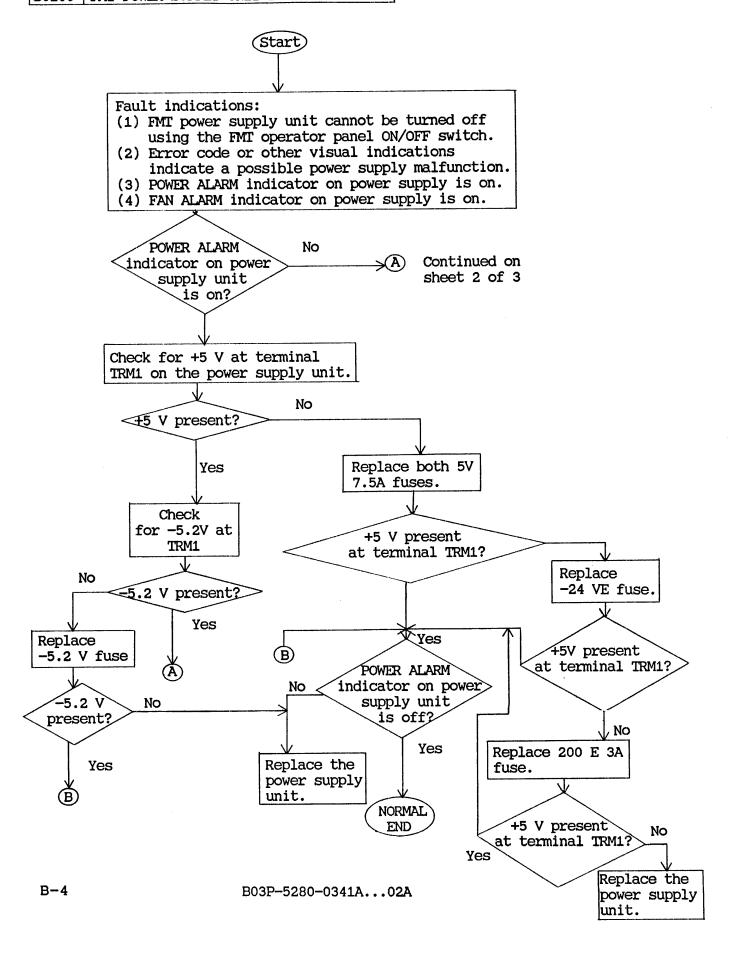
B0001 MTU POWER SUPPLY UNIT TROUBLESHOOTING

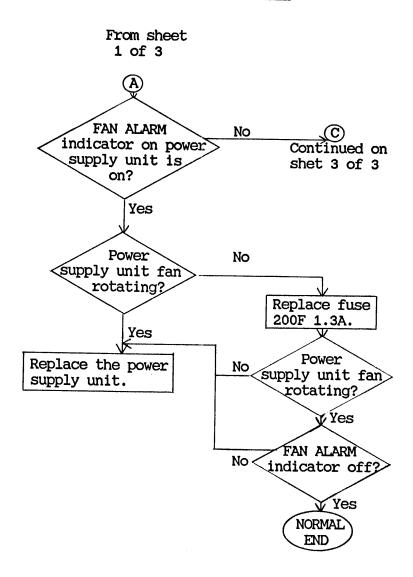
Continued from sheet 1 of 2

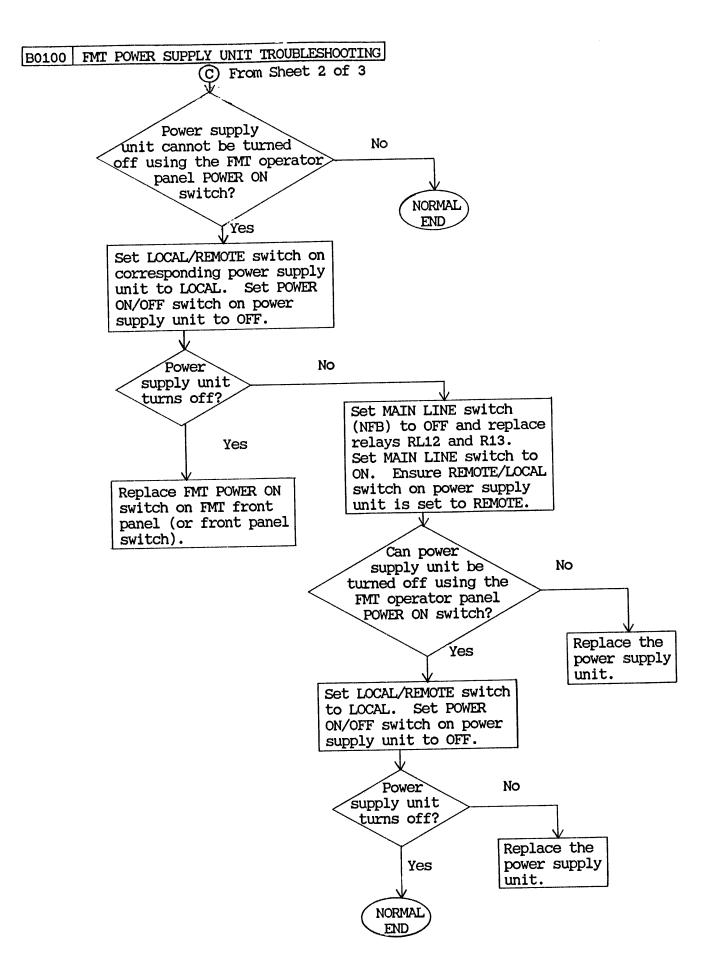
(A)

Note: The following indications are power related but do not indicate a malfunction in the MTU power supply unit. The problem is in the assembly.

Fault	indicator	c Lamps on	MTU power	supply	unit	Fault area or faulty subassembly
	0	1	2	3		
1.	off	off	off	on		PCA 1A02 in the MTU
2.	off	off	on	off		PCA 1A02
3.	off	on	on	off		Tape drive A PCA on MTU side panel
4.	off	on	on	on		PCA 1A02
5.	on	off	off	off		PCA 1A02
6.	on	off	off	on		PCA 1A02
7.	on	off	on	off		PCA 1A02
8.	on	off	on	on		Tape drive A PCA on MTU side panel
9.	on	on	off	on		Tape drive B PCA on MTU side panel
10.	on	on	on	off		Tape drive B PCA on MTU side panel
11.	on	on	on	on		Power supply cables not connected properly







С

C.1 INTRODUCTION

This section provides offline and online diagnostic routines for the Magnetic Tape System (MTS). The section is organized into four main topics:

- (1) A listing of routine numbers, names, and execution times.
- (2) Procedures for initiating and terminating offline or online routines.
- (3) A listing of error codes resulting from malfunctions encountered during performance of a routine together with the probable cause of the malfunction.
- (4) A detailed description of each routine.

The diagnostics are a maintenance tool to determine if the MTS is operating properly. If a fault exists, the operations will stop and the operator can use a field tester to determine the error code. A description of the error and the most probable cause(s) of the error are listed with the error code number. The user can then either replace that item or implement other tests associated with that item.

Example:	Routine	Error code	Description	Fault location
	54	32	MTU capstan motor abnormal	Capstan motor

The user can either replace the capstan motor assembly or test the capstan motor using L0130.

In other cases that require replacement of a printed circuit assembly (PCA), refer to the PCA location charts. (A tab is provided for quick reference to the PCA location charts.)

Offline and online diagnostics are similar to one another in that most routines are the same. However, execution times (run times) may differ, and offline diagnostics executes 11 routines that are not possible in the online mode. In addition, more control is offered in the offline mode.

C.2 OFFLINE DIAGNOSTICS

Offline diagnostics are performed with the field tester. Table C-1 lists offline diagnostics routine numbers, names, and execution times. More detailed descriptions of routines are provided in the last part of FMT/MTU Diagnostics (see Section C.5).

If an illegal routine is attempted during diagnostics, no test routine will be performed, and the routine indicator will display 00. An illegal routine is defined as any offline diagnostics routine number that does not appear in Table C-1, below.

Offline diagnostics self-test programs for the FMT and MTU are stored in an FMT microprogram. Individual routines or sets of routines are executed sequentially and are performed with the field tester. The following conditions are required:

- (1) The operator should be familiar with the field tester (see Part I of this maintenance Manual for a description of the field tester).
- (2) The MTU to be tested must be selected and placed in an online status.
- (3) A full reel of good-quality work tape (SRM 3200 or equivalent) with a file-protect ring must be used.
- (4) If interface cables between an FMT and controller are connected, the host controller power should be turned on. (Routine 00 runs all diagnostic programs and is independent of the controller power status.)

Routines 80, 83 and 90 through 98 are utility programs. These routines have unique requirements and conditions for the tape used during execution. Refer to Section C.5 for those requirements and conditions.

Table C-1. Summary of offline diagnostics routines.

Rout numb		Maximum execution times	
00	Test all diagnostics routines	5 to 6	minutes
01	Test all routines (host controller power on)	5 to 6	minutes
10	Microprocessor self diagnostics	1.6	seconds
11	LSR test partial	1.6	seconds
12	Local memory read/write test	1.6	seconds
14	External register write and sense bus test	1.6	seconds
15	Timer function test	1.6	seconds
20	Diagnostics program of controller	1.6	seconds
	interface printed circuit assembly PCA 1		
21	Diagnostics program of controller	1.6	seconds
	interface printed circuit assembly 2		_
22	Diagnostics program of tape unit	1.6	seconds
	interface printed circuit assembly	_	_
23	Routine to confirm MTU selection	1.6	seconds
24	FMT—MTU data bus test	1.6	seconds
25	Tacho pulse signal test	1.6	seconds
26	Tape speed detection circuit test	1.6	seconds
28	Repositioning counter and counter control test	1.6	seconds
29	Trap circuit test	5.0	seconds
30	FMT LSI scan test	1.6	seconds
31	Time sensor and decoder test	2.2	seconds
32	Loop write/read (LWR) FMT phase encoded format	1.6	seconds
33	Loop write/read (LWR) FMT group coded recording	1.6	seconds
34	Loop write/read FMT nonreturn to zero I (NRZI)	1.8	seconds

Table C-1. Summary of offline diagnostics routines (continued).

numi	Routine Routine name Maximum					
	110410110	037	Maximum			
		exe	ecution times			
35	Loop write/read TU IF (tape unit interface)					
	phase encode	1.6	seconds			
36	Loop write/read TU IF group coded recording	1.6	seconds			
37	Loop write/read TU IF nonreturn to zero I	1.8	seconds			
38	Loop write/read R/W phase encode	3.4	seconds			
39	Loop write/read R/W group coded recording	4.2	seconds			
40	Error correction logic phase encode	2.6	seconds			
41	Group coded recording 1 track correction test	1.9	seconds			
42	Group coded recording 2 track correction test	1.8	seconds			
43	Group coded recording 3 track mask test	1.6	seconds			
44	Phase error pointer test	2.3	seconds			
45	Nonreturn to zero I correction test	2.6	seconds			
46	FMT control circuit test	1.7	seconds			
50	Reel servo test (simple turn)	8.6	seconds			
51	Reel servo margin test		31 seconds			
52 53	Capstan simple running test		27 seconds			
54	Write current on test	3	seconds (a)			
55	14 seconds					
55	Capstan servo margin test 1600 rows per inch write	38 to 4	13 seconds			
56						
	Capstan servo margin test 1600 rows per inch forward and backward read	1.1 to 1	.5 minutes			
57						
0,	Capstan servo margin test 6250 rows per 24 to 36 seconds inch write		6 seconds			
58	Capstan servo margin test 6250 rows per	00 += 0				
	inch forward and backward read	26 to 3	8 seconds			
60	Erase effect test	7.0				
61	Self amplitude gain control circuit test	7.3 7.4	seconds			
62	Group coded recording normal write test	7.5	seconds (a)			
63	Phase Encode normal write test	7.5 8	seconds (b)			
64	Nonreturn to zero I normal write test	7.9	seconds (b)			
65	Slice margin and read level test	6.4	seconds (b)			
66	IBG (Inter block gap) length check test	15.1	seconds (b)			
70	Feed through test	7.3	seconds (b)			
71	Cross talk test	6.9	seconds (b)			
73	Phase Encode total read and write test	11.1	seconds (b)			
74	Group coded recording total read and write		seconds (b)			
_	test	10.3	seconds (b)			
75	Non return to zero I total read and write		200011db (b)			
	test	9.3	seconds (b)			
79	Special routine to test ready status	1.6	seconds			
80	Test program for installation check out of					
83	azimuth and capstan alignment					
03	Test program for conversion check out of read amplifier	8.8	seconds			
	GUINTITIEL		1			

Table C-1. Summary of offline diagnostics routines (continued).

Rou ⁿ	tine Routine name per	exe	Maximum ecution times
90 91 92 93 94 95 96 97	Tape retention action utility Data security erase and rewind utility Read check to tape mark Group coded recording write running utility Phase Encode write running utility Nonreturn to zero I write running utility Back space to beginning of tape Space to end of tape	1.6 — — — — — —	seconds

- (a) Execution time may be increased up to 12 seconds depending on tape quality.
- (b) Execution time may be increased up to 50 seconds depending on tape quality.

C.2.1 Performing Offline Diagnostics

Follow these steps to initiate offline diagnostics:

- (1) If the MTU is Model L2, (dual FMT) set all ENABLE/DISABLE switches on the FMT operator panel to ENABLE.
- (2) With the power turned off, connect the field tester to slot 1A08 of the FMT. See Part I of this Maintenance Manual for a description of how to use the field tester.
- (3) Verify that the lamps are operating properly by setting field tester switches to \$FO. All lamps should be on. If lamps are not on, replace the field tester.
- (4) Turn power on and set the OFL/ONL switch on the field tester to OFL. Ensure the two-digit display on the MTU is "00" and that the Check Unit light is off.
- (5) Set the field tester switches S0 through S7 to \$B2 and toggle the CNT (register contents display) switch.
- (6) Set the field tester switches to \$00 and toggle the SSS switch.
- (7) Set the field tester switches to \$39 and toggle the SSS switch.
- (8) Set the field tester switches to \$B2 and toggle the CNT switch.
- (9) Set the field tester switches to \$00 and toggle the SSS switch.
- (10) Set the field tester switches to \$3E and toggle the SSS switch.
- (11) Set the field tester switches to \$B2 and toggle the CNT switch.
- (12) Set the field tester switches to \$03 and toggle the SSS switch.
- (13) Set the field tester switches to \$3C and toggle the SSS switch.
- (14) Set the field tester switches to \$A8 and toggle the CNT switch to start the diagnostic routine. Lamp L1 on the field tester will go ON.
- (15) When the diagnostic routine terminates or is complete, lamp L1 will go OFF. Check lamps L8 and L11. If they are off, no error exists and FMT checkout is complete.
- (16) If either lamp L8 or L11 is on, set the field tester switches to \$35 and toggle the CNT switch to display the routine number.
- (17) Set the field tester switches to \$36 to display the error code.
- (18) Refer to Section C.4 for corrective actions.

C.3 ONLINE DIAGNOSTICS

C.3 ONLINE DIAGNOSTICS

Online diagnostics can be initiated using a "start-test" command from the host/controller or by issuing \$00 (or \$01) from the field tester (see C.3.1). A summary of the routine numbers, names, and execution times is listed in Table C-2. All tests are run automatically when Test Magnetic Tape System (TMTS) is issued from the controller. TMTS is also commonly shown as Routine 00, 01, and "start test."

Note that the routines and error codes for online diagnostics are identical to those for offline diagnostics except for execution times and for routines 79 through 83 and routines 91 through 98. These routines cannot be executed by the online diagnostics.

Table C-2. Summary of online diagnostic routines.

Rout numb		Maximum execution times	
00	Test all diagnostics routines	5 to 6	minutes
10	Microprocessor self diagnostics	400	S
11	LSR test partial	400	s
12	Local memory read write test	900	ន
14	External register write and sense bus test	400	ន
15	Timer function test	800	S
20	Diagnostics program of controller	1.2	ms
]	interface printed circuit assembly 1		
21	Diagnostics program of controller	1.2	ms
	interface printed circuit assembly 2		:
22	Diagnostics program of tape unit	1.8	ms
	interface printed circuit assembly		
23	Routine to confirm MTU selection	400	S
24	FMT—MTU data bus test	1.2	ms
25	Tach pulse signal test	5	ms
26	Tape speed detection circuit test	3	ms
28	Repositioning counter and counter control test	5	ms
29	Trap circuit test	5	seconds
30	FMT LSI scan test	12	seconds
31	Time sensor and decoder test	500	ms
32	Loop write/read (LWR) FMT phase encode	6	ms
33	Loop write/read FMT group coded recording	3	ms
34	Loop write/read FMT nonreturn to zero I	6	ms
35	Loop write/read TU IF (tape unit interface)		
	phase encode	6	ms
36	Loop write/read TU IF group coded recording	3	ms
37	Loop write/read TU IF nonreturn to zero I	6	ms
38	Loop write/read phase encoded format	3	seconds
39	Loop write/read Group coded recording	4	seconds
40	Error correction logic phase encode	5	seconds
41	Group coded recording 1 track correction test	22	ms
42	Group coded recording 2 track correction test	16	ms

C.3 ONLINE DIAGNOSTICS

Table C-2. Summary of online diagnostic routines (continued).

Rout numb		exe	Maximum execution times		
43	Group coded recording 3 track mask test	3	ms		
44	Phase error pointer test	32	ms		
45	Nonreturn to zero I correction test	24	ms		
46	FMT control circuit test	22	ms		
50	Reel servo test (simple turn)	8	seconds		
51	Reel servo margin test	30	seconds		
52	Capstan simple running test	27	seconds		
53	Write current on test	2	seconds		
54	Auto cleaner test	15	seconds		
55	Capstan servo margin test 1600 rows per inch write	42	seconds		
56	Capstan servo margin test 1600 rows per	1	minute,		
	inch forward and backward read	30	seconds		
57	Capstan servo margin test 6250 rows per inch write	38	seconds		
58	Capstan servo margin test 6250 rows per per inch forward and backward read	40	seconds		
60	Erase effect test	7	seconds		
61	Self amplitude gain control circuit test	7	seconds		
62	Group coded recording normal write test	7	seconds		
63	PE normal write test	7	seconds		
64	Nonreturn to zero I normal write test	7	seconds		
65	Slice margin and read level test	6	seconds		
66	IBG (inter block gap) length check test	15	seconds		
70	Feed through test	7	seconds		
71	Cross talk test	7	seconds		
73	Phase Encode (PE) total read and write test	10	seconds		
74	Group coded recording (GCR) total read and				
	write test	10	seconds		
75	Non return to zero I total read and write test	8	seconds		
90	Tape retention action utility	600	s		

C.3.1 Performing Online Diagnostics

Follow these steps to initiate online diagnostics:

- (1) Connect the field tester to the FMT (refer to Part I for a description of how to use the field tester.)
- Set the ONL/OFL switch on the field tester to OFL.
- (3) Set the field tester switches 0-7 to \$B2, and then toggle the CNT switch.
- (4) Set switches to \$17 and toggle the SSS switch.
- (5) Set switches to \$3D and toggle the SSS switch.(6) Set switches to \$B2 and toggle the CNT switch.
- (7) Set switches to \$00 and toggle the SSS switch. (\$01 would select MTU #1, etc.)
- (8) Set switches to \$3E and toggle the SSS switch.

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- (9) Set switches to \$B2 and toggle the CNT switch.
- (10) Set switches to \$82 and toggle the SSS switch. (Stop and repeat modes.)
- (11) Set switches to \$3C and toggle the SSS switch.
- (12) Set switches to \$B2 and toggle the CNT switch.
- (13) Set switches to \$01 and toggle the SSS switch.
- (14) Set switches to \$38 and toggle the SSS switch.
- (15) Set switches to \$B2 and toggle the CNT switch.
- (16) Set switches to \$XY and toggle the SSS switch. (XY = any desired online routine.)
- (17) Set switches to \$39 and toggle the SSS switch.
- (18) Toggle the SSS switch to start the routine.

If the repeat and error stop modes (\$82) are set (\$00 disables these modes), the FMT repeats the command until an error is detected.

C.3.2 Termination of Online Diagnostics

If the TMTS is successfully run, the MTS will not assert octal code 302, and the host/controller will know that the MTS is operational. Otherwise, 302 will be asserted, and routine and error code will be stored in hex notation in FMT registers XX and XY. The FMT registers can be accessed using the field tester. The routine number and associated error codes can be found in the error code table (see Section C.4) and corrective action can then be implemented. The error code table also lists the faulty circuit card and/or subassembly that caused the error.

C.4 ERROR CODE TABLE AND FAULT ISOLATION

This section lists error codes for both offline and online diagnostics. All routine numbers and error codes are in hex notation. The error code 00 for any routine means that the diagnostics were successfully completed, and no error was detected. The designation xx for routine number means that the associated error code can occur in any routine number. Similarly, an x designation for error code, for example x, means any error code ending with the digit 5, where x = any digit from 0 through 9.

Double			
Routine number	Error Code	Description	Fault location
xx	80	Interruption by manual action in MTU.	Operator error
xx	81	TAG control was attempted to MTU, but the response signal (TAG IN signal) was not set.	532403U
xx	82	Although MTU failed to be set in write or erase status, HWC and HEC (write or erase) were reported normally. MTU failed in status/control/command TAG operation.	532401U
хх	83	MTU was not set to write status because HWC or HEC (write or read) cannont be on.	Write/read printed circuit assembly
ж	84	MTU was not set in erase status HWC was reported or HEC was not reported.	
хх	85	When MTU was not set in forward status or backward status, HWC or HEC was reported.	Write/read printed circuit assembly
xx	95	Stop signal was detected during online diagnostic routine. (Only the controller should reset stop signal).	PCA 1A07 in the FMT
xx	96	Beginning of tape was not detected during rewind operation.	Beginning of tape sensor, TKBMU
xx	97	Tag in signal was set during sense tag operation of MTU sense byte BYTE 3.	532403U

Routine number	Error Code	Description	Fault location
xx	98	Online signal was reset during rewind operation; verify tape operation.	Operator error
10	01	LM (Local memory) \$10 access error.	PCA 1A08 in the FMT
10	77	Error was detected at command instruction of microprocessor.	PCA 1A08 in the FMT
11	01	LM (Local memory) \$11 through \$17 access error.	PCA 1A08 in the FMT
12	01	Data cannot be written/read in Work Register 0 and 1 (W0, W1) of microprocessor.	PCA 1A08 in the FMT
12	02	Error was detected in local storage memory other than the work register.	PCA 1A08 in the FMT
14	01	Error was detected at external register selection circuit on printed circuit assembly (microprocessor address 4X).	PCA 1A08 in the FMT
14	02	Error was detected at external register on printed circuit assembly (microprocessor address 4X).	PCA 1A08 in the FMT
14	03	Error was detected at on printed circuit assembly (microprocessor). (Test magnetic tape system flag bit error.)	PCA 1A08 in the FMT
14	04	CMR register or ADR register error.	PCA 1A07 in the FMT
14	05	Error was detected at controller interface, FCUST register error.	PCA 1A07 in the FMT
14	07	SIF register error.	PCA 1A07 in the FMT
14	08	XCTL register error.	PCA 1A07 in the FMT
14	09	Error was detected at write PCA. MASK register error.	PCA 1A06 in the FMT

Routine number	Error Code	Description	Fault location
14	10	Error was detected at write PCA. DACTL register error.	PCA 1A06 in the FMT
14	11	Error was detected at write PCA. WICTL register error.	PCA 1A06 in the FMT
14	12	Error was detected at write PCA. RDCTL register error.	PCA 1A06 in the FMT
14	13	Error was detected at write PCA. MODE register error.	PCA 1A06 in the FMT
14	14	Error was detected at write PCA. RDSNS register error.	PCA 1A06 in the FMT
14	15	Error was detected at write PCA. CRCST register error.	PCA 1A06 in the FMT
14	16	Error was detected at write PCA. FMERR register error.	PCA 1A02 or PCA 1A06 in the FMT
14	17	Error was detected at external register on read PCA. TSNS register error.	PCA 1A02 in the FMT
14	18	Error was detected at external register on read PCA. POINT register error.	PCA 1A02 in the FMT
14	19	Error was detected at external register on read PCA. BLFMT register error.	PCA 1A01, 1A02, or 1A06 in the FMT
14	20	Error was detected at external register on read formatter. RDERR register error.	PCA 1A02, in the FMT
14	21	Printed circuit assembly (PCA) for nonreturn to zero I mode was not mounted for tri-density unit testing.	PCA 1A01 in the FMT
14	22	Selecting address \$6, read bus error detected.	PCA 1A01 or 1A08 in the FMT
14	23	ZEIK register error.	PCA 1A01 in the FMT
14	24	ZCTL register error.	PCA 1A01 in the FMT
14	25	ZMRG register error.	PCA 1A01 in the FMT

Routine	Error		
number	Code	Description	Fault location
14	26	Error was detected at external register on MTU interface. TMCTL register error.	PCA 1A05 in the FMT
14	27	Error was detected at external register on MTU interface. DVBO register error.	PCA 1A05 in the FMT
14	28	Error was detected at external register on MTU interface. DVBI register error.	PCA 1A05 in the FMT
15	10	M.TMR bit cannot be reset.	PCA 1A05 in the FMT
15	11	CTRU bit cannot be reset.	PCA 1A05 in the FMT
15	12	CTRU bit cannot be set.	PCA 1A05 in the FMT
15	13	CTRU bit cannot be set.	PCA 1A05 in the FMT
15	14	Data was not set correctly in the upper bytes of timer.	PCA 1A05 in the FMT
15	15	Error was detected at the lower bytes of timer.	PCA 1A05 in the FMT
15	16	Error was detected at the lower bytes of timer.	PCA 1A05 in the FMT
15	17	Error was detected at the lower bytes of timer.	PCA 1A05 in the FMT
15	18	CTRU bit cannot be set.	PCA 1A05 in the FMT
15	19	Error was detected at the upper bytes of timer.	PCA 1A05 in the FMT
20	01	Data was not set correctly in external register. Error occurs only during online diagnostics.	PCA 1A05 in the FMT
20	02	Data in CMR register is changed during BUSY. Error occurs only during online diagnostics.	PCA 1A07 in the FMT
20	03	BUSPE bit was not reset.	PCA 1A07 in the FMT

Routine number	Error Code	Description	Fault location
20	05	Data of ADR register was changed during BUSY. Error occurs only during online diagnostics.	PCA 1A07 in the FMT
20	06	Data was not set correctly in FCUST register.	PCA 1A07 in the FMT
20	07	Data was not set correctly in TUST/SIF register.	PCA 1A07 in the FMT
20	08	SIF register read/write error.	PCA 1A07 in the FMT
20	09	MXTL register read/write error.	PCA 1A07 in the FMT
20	15	ADR register was not reset. Error occurs only during offline diagnostics.	PCA 1A07 in the FMT
21	01	Data was not set correctly in external register. Error occurs only during online diagnostics.	PCA 1A07 in the FMT
21	02	Data in CMR register is changed during BUSY. Error occurs only during online diagnostics.	PCA 1A07 in the FMT
21	03	BUSPE bit was not reset.	PCA 1A07 in the FMT
21	04	TREQ/TRAX (Transfer request/ transfer acknowledge) bit was not set/reset. Error occurs only during offline diagnostics.	PCA 1A07 in the FMT
21	05	Data of ADR (address) register was changed during BUSY. Error occurs only during online diagnostics.	PCA 1A07 in the FMT
21	06	Data was not set correctly in FCUST register.	PCA 1A07 in the FMT
21	07	Data was not set correctly in TUST/SIF (Tape unit status/ status in function) register.	PCA 1A07 in the FMT
21	08	SIF (status in function) register read/write error.	PCA 1A07 in the FMT

Routine number	Error Code	Description	Fault location
21	09	MXTL register read/write error.	PCA 1A07 in the FMT
21	15	ADR (address) register was not reset. Error occurs only during offline diagnostics.	PCA 1A07 in the FMT
22	01	D.FTP and D.QTP bits were not reset.	PCA 1A05 in the FMT
22	02	Data was not set/reset correctly in TMCTL register.	PCA 1A05 in the FMT
22	03	Data was not set/reset correctly in TMCTL register.	PCA 1A05 in the FMT
22	04	Data was not set/reset correctly in IMCTL register.	PCA 1A05 in the FMT
22	05	Data was not set/reset correctly in TMCTL register.	PCA 1A05 in the FMT
22	06	Data was not set/reset correctly in TIMER register.	PCA 1A05 in the FMT
22	07	Data was not set/reset correctly in TIMER register.	PCA 1A05 in the FMT
22	08	Data was not set/reset correctly in DVSEL register.	PCA 1A05 in the FMT
22	09	Data was not set/reset correctly in DVSEL register.	PCA 1A05 in the FMT
22	11	Data was not set/reset correctly in TPCNT register.	PCA 1A05 in the FMT
22	12	Data was not set/reset correctly in DVTAG register.	PCA 1A05 in the FMT
22	13	Loop data was not sensed.	PCA 1A05 in the FMT
22	14	Loop data was not sensed.	PCA 1A05 in the FMT
22	15	Error in write data mode.	PCA 1A05 in the FMT
22	16	Malfunction in DBMPX Bit. Error in write data mode.	PCA 1A05 in the FMT
22	17	Malfunction in DBMPX Bit. Error in write data mode.	PCA 1A05 in the FMT

Routine number	Error Code	Description	Fault location
22	18	Malfunction in DBMPX Bit. Error in write data mode.	PCA 1A05 in the FMT
22	19	Malfunction in DBMPX Bit.	PCA 1A05 in the FMT
22	20	UQID was not sensed.	PCA 1A05 in the FMT
23	Х1	Error detected in MIU #0 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MIU #0
23	X2	Error detected in MFU #1 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #1
23	ХЗ	Error detected in MTU #2 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #2
23	X4	Error detected in MTU #3 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MIU #3
23	Х5	Error detected in MIU #4 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #4
23	Х6	Error detected in MIU #5 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #5
23	Х7	Error detected in MTU #6 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #6
23	X8	Error detected in MIU #7 selection logic.	PCA 1A05 and distribution board in the FMT 532403U in MTU #7

Routine number	Error Code	Description	Fault location
23	Х9	TAG control executed to the selected MTU, but TAG IN signal was not set.	PCA 1A05 and distribution board in the FMT 532403U in MTU
23	10	Data was not set/reset correctly at the selection MTU.	PCA 1A05 and distribution board in the FMT 532403U in MTU
23	20	Communication register of selected MTU cannot be reset.	532403U distribution board in the FMT in MTU
24	04	Error in data transfer between formatter and MTU.	PCA 1A05 and distribution board in the FMT 532403U in MTU
25	01	Malfunction of tach stop pulse detection.	PCA 1A05 in the FMT
25	02	Malfunction of tach pulse stop detection.	PCA 1A05 or 1A06 in the FMT
25	03	Malfunction of tach stop pulse detection.	PCA 1A05 in the FMT
25	04	D.FTP or D.QTP were not detected.	TU interface cable, PCA 1A05 and distribu- tion board PCA in the FMT 532403U and PCA 1A04 in the MTU
25	05	D.FTP or D.QTP were not detected.	TU interface cable, PCA 1A05 and distribu- tion board PCA in the FMT 532403U and PCA 1A04 in the MTU
25	06	The number of D.FTP and D.QTP is incorrect.	532403U and PCA 1A04 in the MTU, PCA 1A05 in in the FMT
25	07	The number of D.FTP and D.QTP is incorrect.	532403U and PCA 1A04 in the MTU, PCA 1A05 in in the FMT

Routine number	Error Code	Description	Fault location
25	08	Error in sequence of FTP (Full tacho-pulse) and QTP (Quarter	532403U and PCA 1A04 in the MTU, PCA 1A05 in
26	01	tacho-pulse) signals. Error detected in GAPC (Gap control) signal.	in the FMT 532403U, PCA 1A05 and distribution board PCA in the FMT
26	02	Malfunction of speed detection.	PCA 1A05 in the FMT
26	03	VLOK (Velocity OK) signal was not detected.	PCA 1A05 in the FMT, PCA 1A04 or tape drive A in the MTU, or Capstan motor assembly photo sense block
26	04	Error detected in GAPC (Gap control) signal.	PCA 1A05 in the FMT, PCA 1A04 or tape drive A in the MTU, or Capstan motor assembly photo sense block
26	05	Error detected in GAPC (Gap control) and VLOK (Velocity OK) signal.	PCA 1A05 in the FMT, PCA 1A04 or tape drive A in the MTU, or Capstan motor assembly photo sense block
26	10	VLCHG (Velocity charge) signal was not reset.	PCA 1A05 or 1A06 in the FMT
26	11	VLCHG (Velocity charge) signal was not reset.	PCA 1A05 or 1A06 in the FMT
26	12	VLCHG (Velocity charge) signal was not detected.	PCA 1A05 or 1A06 in the FMT
26	13	VLOK (Velocity check) signal was not reset.	PCA 1A05 or 1A06 in the FMT
28	01	Error detected in the UP count mode of reposition counter.	PCA 1A05 in the FMT
28	10	Error detected in the UP count mode of reposition counter.	PCA 1A05 in the FMT
28	11	Carry bit of reposition counter was not detected.	PCA 1A05 in the FMT

Routine number	Error Code	Description	Fault location
28	12	Carry bit of reposition counter was not reset.	PCA 1A05 in the FMT
28	13	Error detected in the down count mode of reposition counter.	PCA 1A05 in the FMT
28	14	Reposition counter was not reset.	PCA 1A05 in the FMT
29	01	Expected timer trap did not occur.	PCA 1A05 or 1A08 in the FMT
29	02	MTU was interrupted by manual action, or unexpected interruption occured.	532401U, in the MTU PCA 1A05, 1A08, or distribution board in the FMT
29	03	Tacho stop was detected in spite of GAPC and VLOK (Velocity check) assertion.	PCA 1A05 in the FMT
29	04	MTU was interrupted by manual action, or unexpected interruption occured.	532401U, in the MTU PCA 1A05, 1A08, or distribution board in the FMT
29	05	Tacho stop signal was not detected within the specified period.	PCA 1A05 in the FMT
29	10	MTU was interrupted by manual action, or unexpected interruption occured.	532401U, in the MTU PCA 1A05, 1A08, or distribution board in the FMT
29	11	T.INT signal was not detected within the specified period.	532401U in the MIU, or PCA 1A05 in the FMT
29	15	Unexpected trap occured.	PCA 1A05 or 1A07 in the FMT
29	8X	TAG control was executed at the specified MTU address, but failed.	
30	01	Error detected in LSI of write formatter.	PCA 1A06 or 1A07 in the FMT

Routine number	Error Code	Description	Fault location
30	02	Error detected in LSI of write formatter.	PCA 1A06 or 1A07 in the FMT
30	11	Error detected in LSI of read formatter.	PCA 1A02 or 1A07 in the FMT
30	12	Error detected in LSI of read formatter.	PCA 1A02 or 1A07 in the FMT
31	01	GCR (group coded recording) MP (micro program) mode (time sense P bit on) test error.	550157U, PCA 1A02 or 1A05 in the FMT
31	02	PE (phase encode) MP (Micro Program) mode (time sense P bit on) test error.	550157U, PCA 1A02 or 1A05 in the FMT
31	03	GCR (group coded recording) MP (micro program) mode (time sense 0 - 7 on) test error.	550157U, PCA 1A02, 1A05 or 1A06 in the FMT
31	04	PE (phase encode) MP (Micro Program) mode (time sense 0 - 7 on) test error.	550157U, PCA 1A02, 1A05 or 1A06 in the FMT
31	05	GCR (group coded recording) MP (micro program) mode (time sense P bit off) test error.	550157U or PCA 1A02 in the FMT
31	06	PE (phase encode) MP (Micro Program) mode (time sense P bit off) test error.	550157U or PCA 1A02 in the FMT
. 31	07	GCR (group coded recording) MP (micro program) mode (time sense 0 - 7 off) test error.	550157U or PCA 1A02 in the FMT
31	08	PE (phase encode) MP (Micro Program) mode (time sense 0 - 7 off) test error.	550157U or PCA 1A02 in the FMT
31	12	ALL1W (all 1 write) mode time sense error.	PCA 1A05 or 1A06 in the FMT
31	13	ALL1W (all 1 write) mode time sense error.	PCA 1A05 or 1A06 in the FMT
31	14	ALL1W (all 1 write) mode time sense error.	PCA 1A05 or 1A06 in the FMT

Routine number	Error Code	Description	Fault location
31	15	ALL1W (All 1 Write) mode time sense error.	PCA 1A05 or 1A06 in the FMT
31	20	Block format in formatter read status cannot be detected.	PCA 1A05 or 1A06 in the FMT
31	21	Block format in formatter read status cannot be detected.	PCA 1A05 or 1A06 in the FMT
31	23	Block format in formatter read status cannot be detected.	PCA 1A05 or 1A06 in the FMT
31	29	BCU BIT was not detected.	PCA 1A05, 1A06, or 1A08 in the FMT
32	10	TNSNS (time sense) signal was not set correctly on more than one track.	550157U or PCA 1A02 in the FMT
32	11	DBOB (detection of beginning of block) signal was not set correctly.	PCA 1A02 in the FMT
32	12	HBLX or HNOIS signal was not set correctly.	PCA 1A02 or 1A06 in the FMT
32	13	PHOK (phase OK) signal was not set correctly.	PCA 1A06 in the FMT
32	14	PREA (preamble detected) signal was not set correctly.	PCA 1A02 or 1A06 in the FMT
32	15	Unexpected STRDC signal detected.	PCA 1A06 in the FMT
32	16	POSA (postamble) signal was not detected in time.	PCA 1A02, 1A06, or 1A07 in the FMT
32	17	Error correction pointer was detected.	550157U, PCA 1A02, 1A05, or 1A06 in the FMT
32	19	DBOB (detection of beginning of block) signal was detected before detection of EPOSA.	PCA 1A06 in the FMT
32	20	FMT detected postamble error.	PCA 1A08 in the FMT

Routine number	Error Code	Description	Fault location
32	21	IBG (inter block gap) was not detected correctly.	550157U
32	22	FMT detected end data check.	PCA 1A02, 1A05, or 1A06 in the FMT
32	23	Error was detected at BCU interval during storage of write data into the data buffer.	PCA 1A05 or 1A06 in the FMT
32	26	BIBSY (bus in busy) signal was not reset correctly.	PCA 1A05 or 1A07 in the FMT
32	27	FMT detected slip check.	PCA 1A06 in the FMT
32	41	FMT detected skew error.	550157U, or PCA 1A02 in the FMT
32	42	FMT detected drop out error.	PCA 1A02 in the FMT
32	43	FMT detected VRC (vertical redundancy check) error.	PCA 1A02 in the FMT
32	44	FMT detected multi-track error.	PCA 1A02 in the FMT
32	45	FMT detected postamble error.	PCA 1A02 in the FMT
32	46	FMT detected WVRC (write VRC) error.	PCA 1A02 in the FMT
32	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
32	48	FMT detected over-run error.	PCA 1A01, 1A02, or 1A06 in the FMT
32	54	CRC (cyclic redundancy check) status transfer buffer is being checked.	PCA 1A05, 1A06, or 1A07 in the FMT
32	55	CRC (cyclic redundancy check) status was A ≠ B.	PCA 1A06 in the FMT
32	56	BUS parity error was detected.	PCA 1A07 in the FMT
32	8X	TAG control was executed at the specified MTU address but failed.	

Routine	Error		
number	Code	Description	Fault location
33	10	TNSNS (time sense) signal was not set correctly on more than one track.	550157U, PCA 1A02 or 1A05 in the FMT
33	11	DBOB (detection of beginning of block) signal was not set correctly.	PCA 1A02 in the FMT
33	12	HBLX or HNOIS signal was not set correctly.	PCA 1A02 or 1A06 in the FMT
33	13	PHOK (phase OK) signal was not set correctly.	PCA 1A02 or 1A06 in the FMT
33	14	PREA (preamble detected) signal was not set correctly.	PCA 1A02 or 1A06 in the FMT
33	15	Unexpected STRDC signal detected.	PCA 1A02 or 1A06 in the FMT
33	16	POSA (postamble) signal was not detected in time.	PCA 1A02 or 1A06 in the FMT
33	17	Error correction pointer was detected.	550157U, PCA 1A02 in the FMT
33	19	DBOB (detection of beginning of block) signal was detected before detection of EPOSA (postamble read end condition).	PCA 1A06 in the FMT
33	20	FMT detected postamble error.	PCA 1A02 in the FMT
33	21	IBG (inter block gap) was not detected correctly.	550157U
33	22	FMT detected end data check.	PCA 1A02 or 1A06 in the FMT
33	23	Error was detected at BCU interval during storage of write data into the data buffer.	PCA 1A05 or 1A06 in the FMT
33	26	BIBSY (bus in busy) signal was not reset correctly.	PCA 1A05 or 1A07 in the FMT
33	27	FMT detected slip check.	PCA 1A06 in the FMT

Routine number	Error Code	Description	Fault location
33	40	FMT detected deskewing buffer error.	PCA 1A02 in FMT
33	41	FMT detected skew error.	550157U, PCA 1A02 in the FMT
33	42	FMT detected drop-out error.	PCA 1A02 in the FMT
33	43	FMT detected VRC (vertical redundancy check) error.	PCA 1A02 or 1A05 in the FMT
33	44	FMT detected multi-track error.	PCA 1A02 in the FMT
33	45	FMT detected postamble error.	PCA 1A02 in the FMT
33	46	FMT detected WVRC (write vertical redundancy check) error.	PCA 1A06 in the FMT
33	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
33	48	FMT detected over-run error.	PCA 1A01, 1A02 or 1A06 in the FMT
33	54	CRC (cyclic redundancy check) status transfer buffer is being checked.	PCA 1A05, 1A06, or 1A07 in the FMT
33	55	CRC (cyclic reduncancy check) status was A ≠ B.	PCA 1A06 in the FMT
33	56	BUS parity error was detected.	PCA 1A07 in the FMT
33	8X	TAG control was executed at the specified MTU address but failed.	
34	01	RDB.S signal is not set correctly.	PCA 1A01 and 1A06 in the FMT
34	02	FMT cannot reset RDB.S signal.	PCA 1A01 in the FMT
34	03	MBLKZ signal was not set correctly.	PCA 1A01 in the FMT

Routine number	Error Code	Description	Fault location
34	04	LRC (longitudinal redundancy check), CRC (cyclic redundancy check), BLKED (NRZ block end), CRCHG (CRC horizontal gap) or CRCRG (CRC recording gap) signal was detected at illegal timing.	PCA 1A01 in the FMT
34	05	RDB.S signal did not appear in specified period.	PCA 1A01 in the FMT
34	06	LRC (longitudinal redundancy check), CRC (cyclic redundancy check), BLKED (NRZ block end), CRCHG (CRC horizontal gap) or CRCRG (CRC recording gap) signal was detected at illegal timing.	PCA 1A01 in the FMT
34	09	CRCRG and CRCHG signal was set at the same time.	PCA 1A01 in the FMT
34	10	CRC data was detected too early. Timing error.	PCA 1A06 in the FMT
34	11	RDB.S signal was not set correctly with the CRC data.	PCA 1A06 in the FMT
34	12	LRC signal was not set.	PCA 1A04 in the FMT
34	13	RDB.S signal was not set correctly with the CRC data.	PCA 1A06 in the FMT
34	15	CRCHG signal was detected, but LRC data was detected.	PCA 1A06 in the FMT
34	16	CRCHG and LRC data were not detected.	PCA 1A01 in the FMT
34	17	CRC data and LRC signal were not detected.	PCA 1A01 or 1A06 in the FMT
34	18	CRC data and LRC data were not detected.	PCA 1A01 in the FMT
34	19	BLKE (Block End) signal was detected before CRC and LRC data.	PCA 1A01 in the FMT

Routine number	Error Code	Description	Fault location
34	20	Noise data was detected after LRC data.	550157U, PCA 1A06 in the FMT
34	21	BLKE signal was detected too early. Timing error.	PCA 1A01 in the FMT
34	22	CRCHG signal was not detected within the specified period.	PCA 1A01 in the FMT
34	27	Slow end error.	PCA 1A06 in the FMT
34	28	BLKE signal was detected too early. Timing error.	PCA 1A01 in the FMT
34	29	CRCHG signal was not detected.	PCA 1A01 in the FMT
34	30	BLKE signal was not detected within the specified period.	PCA 1A01 in the FMT
34	31	Slow end error.	PCA 1A06 in the FMT
34	32	VRC (vertical redundancy check) error.	PCA 1A01 in the FMT
34	33	Skew error.	PCA 1A01 in the FMT
34	34	LRC (longitudinal redundancy check) error.	PCA 1A01 in the FMT
34	35	SDRST (sense data reset) function error.	PCA 1A01 in the FMT
35	10	TNSNS (time sense) signal was not set correctly on more than one track.	550157U, distribution PCA in the FMT
35	40	FMT detected deskewing buffer error.	PCA 1A02 in the FMT
35	41	FMT detected skew error.	532403U
35	42	FMT detected drop out error.	532403U
35	43	FMT detected VRC (vertical redundancy check) error.	PCA 1A02 or 1A05 in the FMT, 550157U
35	44	FMT detected multi-track error.	PCA 1A02 in the FMT
35	45	FMT detected postamble error.	PCA 1A02 in the FMT

Routine number	Error Code	Description	Fault location
35	46	FMT detected WVRC (write vertical redundancy check) error.	PCA 1A06 in the FMT
35	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
35	48	FMT detected over-run error.	PCA 1A01, 1A02, or 1A06 in the FMT
35	54	CRC (cyclic redundancy check) status (transfer buffer is being checked).	PCA 1A06 or 1A07 in the FMT
35	55	CRC status was A ≠ B.	PCA 1A06 in the FMT
35	56	BUS parity error was detected.	PCA 1A07 in the FMT
35	8X	TAG control was executed at the specified MTU address but failed.	
36	10	TNSNS (time sense) signal was not set correctly on more than one track.	550157U, PCA 1A05 or distribution PCA in the FMT
36	40	FMT detected deskewing buffer error.	PCA 1A02 in the FMT
36	41	FMT detected skew error.	532403U
36	42	FMT detected drop-out error.	532403U
36	43	FMT detected VRC (vertical redundancy check) error.	PCA 1A02 or PCA 1A05 in the FMT, 550157U
36	44	FMT detected multi-track error.	PCA 1A02 in the FMT
36	45	FMT detected postamble error.	PCA 1A02 in the FMT
36	46	FMT detected WVRC (write vertical redundancy check) error.	PCA 1A06 in the FMT
36	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
36	48	FMT detected over-run error.	PCA 1A01, 1A02, or 1A06 in the FMT

Routine number	Error Code	Description	Fault location
36	54	CRC status (transfer buffer is being checked).	PCA 1A06 or 1A07 in the FMT
36	55	CRC status was A ≠ B.	PCA 1A06 in the FMT
36	56	BUS parity error was detected.	PCA 1A07 in the FMT
36	8X	TAG control was executed at the specified MTU address but failed.	
37	01	RDB.S signal is not set correctly.	PCA 1A01 or 1A06 in the FMT, 550157U
37	02	FMT cannot reset RDB.S signal.	PCA 1A01 in the FMT
37	8X	TAG control was executed at the specified MTU address but failed.	
38	10	TNSNS (time sense) signal was not set correctly on more than one track.	Write/read printed circuit assembly, or cable between 532403U and write/read printed circuit assembly
38	12	HBLX or HNOIS signal was not set correctly.	Write/read printed circuit assembly
38	14	PREA (preamble) signal was not set correctly.	Write/read printed circuit assembly
38	16	POSA (postamble) signal was not detected in time.	Write/read printed circuit assembly
38	19	DBOB (detection of beginning of block) signal was detected before detection of EPOSA.	Write/read printed circuit assembly
38	20	FMT detected postamble error.	Write/read printed circuit assembly
38	21	IBG (inter block gap) was not detected correctly.	Write/read printed circuit assembly
38	22	FMT detected end data check.	Write/read printed circuit assembly

Routine number	Error Code	Description	Fault location
38	41	FMT detected skew error.	Write/read printed circuit assembly
38	42	FMT detected drop-out error.	Write/read printed circuit assembly
38	43	FMT detected VRC (vertical redundancy check) error.	Write/read printed circuit assembly
38	44	FMT detected multi-track error.	Write/read printed circuit assembly
38	45	FMT detected postamble error.	Write/read printed circuit assembly
38	46	FMT detected WVRC (write VRC) error.	PCA 1A06 in the FMT
38	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
38	48	FMT detected over-run error.	PCA 1A01, 1A02 or 1A06 in the FMT
38	54	CRC (cyclic redundancy check) status (transfer bus is being checked).	PCA 1A06 or 1A07 in the FMT
38	55	CRC status was A ≠ B.	PCA 1A06 in the FMT
38	56	BUS parity error was detected.	PCA 1A07 in the FMT
38	8X	TAG control was executed at the specified MTU address but failed.	
38	96	Error was detected at beginning of tape sensor.	Operator error or beginning of tape sensor
38	98	Manual operation was detected in selected MTU.	Operator error

Routine number	Error Code	Description	Fault location
39	10	TNSNS (time sense) signal was not set correctly on more than one track.	Write/read printed circuit assembly or cable between 532403U and write/read printed circuit assembly
39	12	HBLX or HNOIS signal was not set correctly.	Write/read printed circuit assembly
39	14	PREA (preamble) signal was not set correctly.	Write/read printed circuit assembly
39	16	POSA (postamble) signal was not detected in time.	Write/read printed circuit assembly
39	19	DBOB (detection of beginning of block) signal was detected before detection of EPOSA (postamble read end condition).	Write/read printed circuit assembly
39	20	FMT detected postamble error.	Write/read printed circuit assembly
39	21	IBG (inter block gap) was not detected correctly.	Write/read printed circuit assembly
39	22	FMT detected end data check.	Write/read printed circuit assembly
39	38	Beginning of tape signal cannot be reset.	Beginning of tape sensor or faulty tape
39	40	FMT detected deskewing buffer error.	PCA 1A02 in the FMT
39	41	FMT detected skew error.	Write/read printed circuit assembly
39	42	FMT detected drop out error.	Write/read printed circuit assembly
39	43	FMT detected VRC (vertical redundancy check) error.	Write/read printed circuit assembly

Routine number	Error Code	Description	Fault location
39	44	FMT detected multi-track error.	Write/read printed circuit assembly
39	45	FMT detected postamble error.	Write/read printed circuit assembly
39	46	FMT detected WVRC (write vertical redundancy check) error.	PCA 1A06 in the FMT
39	47	FMT detected write bus out parity error.	PCA 1A06 or 1A07 in the FMT
39	48	FMT detected over-run error.	PCA 1A01, 1A02 or 1A06 in the FMT
39	54	CRC status (transfer buffer is being checked).	PCA 1A06 or 1A07 in the FMT
39	55	CRC (cyclic redundancy check) status was A ≠ B.	PCA 1A06 in the FMT
39	56	BUS parity error was detected.	PCA 1A07 in the FMT
39	8X	TAG control was executed at the specified MTU address but failed.	
39	90	FMT failed to set the MTU into group coded recording status.	532401U, 532403U
40	01	Error detected in ECC (error correction character) function.	PCA 1A02 in the FMT
40	03	P-bit (parity bit) pointer was not matched with mask bit.	PCA 1A02 in the FMT
40	04	Pointer does not match mask pattern.	PCA 1A02 in the FMT
40	05	VRC (vertical redundancy check) error bit was set incorrectly.	550157U, or PCA 1A02 in the FMT
40	07	1 or 2 MLT (multiple track) and VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT

Routine number	Error Code	Description	Fault location
40	09	1 or 2 VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
40	10	TSNS (time sense) did not match MASK pattern.	PCA 1A02 in the FMT
40	14	1 or 2 was set in write mode.	PCA 1A02 in the FMT
41	01	Error detected in ECC (error correction character) function.	PCA 1A02 in the FMT
41	03	P-bit (parity bit) pointer was not matched with mask bit.	PCA 1A02 in the FMT
41	04	Pointer does not match mask pattern.	PCA 1A02 in the FMT
41	05	VRC (vertical redundancy check) error bit was set incorrectly.	550157U, or PCA 1A02 in the FMT
41	07	1 or 2 MLT (multiple track) and VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
41.	09	1 or 2 VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
41.	10	TSNS (time sense) did not match MASK pattern.	PCA 1A02 in the FMT
42	01	Error detected in ECC (error correction character) function.	PCA 1A02 in the FMT
42	03	P-bit (parity bit) pointer was not matched with mask bit.	PCA 1A02 in the FMT
42	04	Pointer does not match mask pattern.	PCA 1A02 in the FMT
42	05	VRC (vertical redundancy check) error bit was set incorrectly.	PCA 1A02 in the FMT
42	07	1 or 2 MLT (multiple track) and VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
42	09	1 or 2 VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT

Routine number	Error Code	Description	Fault location
42	10	TSNS (time sense) did not match MASK pattern.	PCA 1A02 in the FMT
43	01	Error detected in ECC (error correction character) function.	PCA 1A02 in the FMT
43	05	VRC (vertical redundancy check) error bit was set incorrectly.	PCA 1A02 in the FMT
43	07	1 or 2 MLT (multiple track) and VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
43	09	1 or 2 VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
43	10	TSNS (time sense) did not match MASK pattern.	PCA 1A02 in the FMT
44	01	Error detected in ECC (error correction character) function.	PCA 1A02 in the FMT
44	03	P-bit (parity bit) pointer was not matched with mask bit.	PCA 1A02 in the FMT
44	04	Pointer does not match mask pattern.	550157U, PCA 1A02 in the FMT
44	05	VRC (vertical redundancy check) error bit was set incorrectly.	PCA 1A02 in the FMT
44	06	MLT (multiple track) and VRC (vertical redundancy check) were set in two bits in mask/group coded recording/RD mode.	PCA 1A06 in the FMT
44	07	1 or 2 MLT (multiple track) and VRC (vertical redundancy check) were set.	PCA 1A02 in the FMT
44	10	TSNS (time sense) did not match MASK pattern.	PCA 1A02 in the FMT
44	14	1 or 2 was set in write mode.	PCA 1A02 in the FMT
45	01	RDB.S signal is not set correctly.	550157U, PCA 1A01 or PCA 1A06 in the FMT

Routine number	Error Code	Description	Fault location
45	02	FMT cannot reset RDB.S signal.	PCA 1A01 in the FMT
45	03	MBLKZ signal was not set correctly.	PCA 1A01 in the FMT
45	04	LRC (longitudinal redundancy check), CRC (cyclic redundancy check), BLKED (NRZ block end), CRCHG (CRC horizontal gap) or CRCRG (CRC recording gap) signal was detected at illegal timing.	PCA 1A01 in the FMT
45	05	RDB.S signal did not appear in specified period.	PCA 1A01 in the FMT
45	06	LRC (longitudinal redundancy check), CRC (cyclic redundancy check), BLKED (NRZ block end), CRCHG (CRC horizontal gap) or CRCRG (CRC recording gap) signal was detected at illegal timing.	PCA 1A01 in the FMT
45	09	CRCRG and CRCHG signal was set at the same time.	PCA 1A01 in the FMT
45	10	CRC data was detected too early. Timing Error.	PCA 1A06 in the FMT
45	11	RDB.S signal was not set correctly with the CRC data.	PCA 1A06 in the FMT
45	12	LRC signal was not set.	PCA 1A01 in the FMT
45	13	RDB.S signal was not set correctly with the CRC data.	PCA 1A06 in the FMT
45	15	CRCHG signal was detected, but LRC data was detected.	PCA 1A06 in the FMT
45	16	CRCHG and LRC data were not detected.	PCA 1A01 in the FMT
45	17	CRC data and LRC signal were not detected.	PCA 1A01 or 1A06 in the FMT
45	18	CRC data and LRC data were not detected.	PCA 1A01 in the FMT

Routine number	Error Code	Description	Fault location
45	19	BLKE (block end) signal was detected before CRC and LRC data.	PCA 1A01 in the FMT
45	20	Noise data was detected after LRC data.	550157U, PCA 1A06 in the FMT
45	21	BLKE signal was detected too early. Timing error.	PCA 1A01 in the FMT
45	22	CRCHG signal was not detected within the specified period.	PCA 1A01 in the FMT
45	27	Slow end error.	PCA 1A06 in the FMT
45	28	BLKE signal was detected too early. Timing error.	PCA 1A01 in the FMT
45	29	CRCHG signal was not detected.	PCA 1A01 in the FMT
45	30	BLKE signal was not detected within the specified period.	PCA 1A01 in the FMT
45	31	Slow end error.	PCA 1A06 in the FMT
45	32	VRC error.	PCA 1A01 in the FMT
45	33	Skew error.	PCA 1A01 in the FMT
45	34	LRC (longitudinal redundancy check) error.	PCA 1A01 in the FMT
45	35	SDRST (sense data reset) function error.	PCA 1A01 in the FMT
46	01	Window signal cannot be detected.	PCA 1A06 in the FMT
46	02	NOISE signal was not detected within specified period.	PCA 1A06 in the FMT
46	03	SLIPC (not slip check) signal was not detected within specified period.	PCA 1A01 or 1A06 in the FMT
46	04	SRDC (set condition) signal was not detected within specified period.	PCA 1A01 or 1A06 in the FMT

Routine number	Error Code	Description	Fault location
46	05	EDC (end data check) signal was not detected within specified period.	PCA 1A06 in the FMT
46	12	Noise signal was not detected within specified period.	PCA 1A01 or 1A06 in the FMT
46	13	SLIPC (not slip check) signal was not detected within specified period.	PCA 1A01 or 1A06 in the FMT
46	14	SRDC (set condition) signal was not detected within specified period.	PCA 1A01 or 1A06 in the FMT
46	15	EDC (end data check) signal was not detected within specified period.	PCA 1A06 in the FMT
50	11	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during forward run.	PCA 1A04 in the MTU, or capacitive sensor
50	12	Tape loop alarm right. Error detected in servo on file reel side. Error was found during forward run.	PCA 1A04 in the MTU, or capacitive sensor
50	14	MTU check was found. Error was found during forward run.	
50	18	Ready signal was off. Error was found during forward run.	MTU PCA 1A05, 1A06 or operator error
50	21	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during backward run.	PCA 1A04 in the MTU, or capacitive sensor
50	22	Tape loop alarm right. Error detected in servo on file reel side. Error was found during backward run.	PCA 1A04 in the MTU, or capacitive sensor

Routine number	Error Code	Description	Fault location
50	24	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB (Drive Sense Byte) 6 (for online diagnostics). Error was found during backward run.	Refer to MTU Error Code Table (See A.2)
50	28	Ready signal was off. Error was found during backward run.	MTU PCA 1A05, 1A06 or operator error
50	31	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during change of direction from forward to backward.	PCA 1A04 in the MTU or capacitive sensor
50	32	Tape loop alarm right. Error detected in servo on file reel side. Error was found during change of direction from forward to backward.	PCA 1A04 in the MTU capacitive sensor
50	34	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB (drive sense byte) 6 (for online diagnostics). Error was found during change of direction from forward to backward.	Refer to MTU Error Code Table (See A.2)
50	38	Ready signal was off. Error was found during change of direction from forward to backward.	MTU PCA 1A05, 1A06 operator error
50	41	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during backward short run.	PCA 1A04 in the MTU capacitive sensor
50	42	Tape loop alarm right. Error detected in servo on file reel side.	PCA 1A04 in the MTU capacitive sensor

Routine number	Error Code	Description	Fault location
50	44	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB (drive sense byte) 6 (for online diagnostics). Error was found during backward short run.	Refer to MTU Error Code Table (See A.2)
50	48	Ready signal was off. Error was found during backward short run.	MTU PCA 1A05, 1A06 operator error
51	11	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during short go up/down forward run.	PCA 1A04 in the MTU, or capacitive sensor
51	12	Tape loop alarm right. Error detected in servo on file reel side. Error was found during short go up/down forward run.	PCA 1A04 in the MTU, or capacitive sensor
51	14	Error was found during short go up/down forward run.	Troubleshoot using error code indicated on front panel. Refer to Section A for error code list.
51	18	Ready signal was off. Error was found during short go up/down forward run.	MTU PCA 1A05, 1A06 or operator error
51	21	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during long go up/down forward run.	PCA 1A04 in the MTU or capacitive sensor
51	22	Tape loop alarm right. Error detected in servo on file reel side. Error was found during long go up/down forward run.	PCA 1A04 in the MTU or capacitive sensor
51	24	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB 6 (for online diagnostics). Error was found during long go up/down forward run.	Refer to MTU Error Code Table (See A.2)

Routine number	Error Code	Description	Fault location
51	28	Ready signal was off. Error was found during long go up/down forward run.	MTU PCA 1A05, 1A06, or operator error
51	31	Tape loop alarm left. Error detected in servo on machine reel side.	PCA 1A04 in the MTU, or capacitive sensor
51	32	Tape loop alarm right. Error detected in servo on file reel side. Error was found during short forward to backward change of direction.	PCA 1A04 in the MTU, or capacitive sensor
51	34	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB 6 (drive sense byte) (for online diagnostics). Error was found during short forward/backward change of direction.	Refer to MTU Error Code Table (See A.2)
51	38	Ready signal was off. Error was found during short forward to backward change of direction.	MTU PCA 1A05, 1A06 operator error
51	41	Tape loop alarm left. Error detected in servo on machine reel side. Error was found during long forward to backward change of direction.	PCA 1A04 in the MTU or capacitive sensor
51	42	Tape loop alarm right. Error detected in servo on file reel side. Error was found during long forward to backward change of direction.	PCA 1A04 in the MTU or capacitive sensor
51	44	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB 6 (drive sense byte) (for online diagnostics). Error was found during long forward to backward change of direction.	Refer to MTU Error Code Table (See A.2)

Routine number	Error Code	Description	Fault location
51	48	Ready signal was off.	MTU PCA 1A05, 1A06, or operator error
51	51	Tape loop alarm right. Error detected in servo on machine reel side.	PCA 1A04 in the MTU, or capacitive sensor
51	52	Tape loop alarm right. Error detected in servo on file reel side.	PCA 1A04 in the MTU, or capacitive sensor
51	54	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB 6 (for online diagnostics). Error was found during long go up/down backward run.	Refer to MTU Error Code Table (See A.2)
51	58	Ready signal was off. Error was found during long go up/down backward run.	MTU PCA 1A05, 1A06, or operator error
51	61	Tape loop alarm right. Error detected in servo on machine reel side. Error was found during short go up/down backward run.	PCA 1A04 in the MTU or capacitive sensor
51	62	Tape loop alarm right. Error detected in servo on machine reel side. Error was found during short go up/down backward run.	PCA 1A04 in the MTU or capacitive sensor
51	64	Analysis was done by error code of operator panel on MTU (for offline diagnostics). Analysis was done on MTU error code of DSB 6 (for online diagnostics). Error was found during short go up/down backward rum.	Refer to MTU Error Code Table
51	68	Ready signal was off. Error was found during short go up/down backward run.	MTU PCA 1A05, 1A06, or operator error
52	01	GAPC (gap control) did not reset during backward run.	MTU PCA 1A05 or 1A06

Routine number	Error Code	Description	Fault location
52	02	MTU ready signal was a '0' during forward run.	MTU PCA 1A05 or 1A06
52	03	FMT detected interruption signal from MTU in ready status during forward run.	MTU PCA 1A05 or 1A06
52	04	MTU online signal was a '0' during forward run.	Manual interruption; if no manual action, PCA 1A05 or 1A06 in the MTU
52	05	Tape loop alarm—left, during forward run.	Refer to MTU Error Code Table (See A.2)
52	06	TU (tape unit) check occurred during forward run.	Capacitive sensor or PCA "B" on MTU side panel
52	07	Tape loop alarm right during forward run.	Capacitive sensor or PCA "B" on MTU side panel
52	08	Velocity error during forward run.	Tape drive A PCA on MTU side panel, PCA 1A04 in the MTU, or Capstan motor assembly
52	09	Manual action to MTU during forward run.	Operator error
52	10	Tape running direction was incorrect during forward run.	MTU PCA 1A04, 1A05 or 1A06
52	12	Tacho signal was not detected by MTU during forward run.	Interface cable, PCA 1A05, or distribution board in the FMT
52	13	Error detected in CPFWD (Capstan forward) signal detection circuit during forward run.	Interface cable, PCA 1A05, or distribution board in the FMT
52	21	GAPC (gap control) did not reset during backward run.	MTU PCA 1A05 or 1A06
52	22	MTU ready signal was a '0' during forward run.	MTU PCA 1A05 or 1A06

Routine number	Error Code	Description	Fault location
52	23	FMT detected interrupt signal from MTU in ready status during backward run.	MTU PCA 1A05 or 1A06
52	24	MTU online signal was a '0' during backward run.	Manual interruption; if not manual action, MTU PCA 1A05 or 1A06
52	25	Tape loop alarm left during backward run.	Refer to MTU Error Code Table (See A.2)
52	26	TU (tape unit) check occurred durring backward run.	Capacitive sensor, or Tape drive B PCA on MTU side panel
52	27	Tape loop alarm right during backward run.	Capacitive sensor, or Tape drive B PCA on MTU side panel
52	28	Velocity error during forward run.	Tape drive A PCA on MTU side panel, PCA 1A04 in the MTU, or capstan motor assembly
52	29	Manual action to MTU during forward run.	Operator error
52	30	Tape running direction was incorrect during backward run.	MTU PCA 1A04, 1A05, or 1A06
52	32	TACH signal was not detected by MTU during backward run.	Interface cable, PCA 1A05, or distribution board in the FMT
52	33	Error detected in CPFWD signal detection circuit during backward run.	Interface cable, PCA 1A05, or distribution board in the FMT
53	01	Write current or erase current error in write/erase head.	Write/read printed circuit assembly, or 532403U
53	03	Defects in MTU read amplifier.	Write/read printed circuit assembly, or PCA 1A06 in the FMT
53	04	At least 1 bit of dead track was detected (bit 0 - 8).	Write/read printed circuit assembly or PCA 1A06 in the FMT

Routine number	Error Code	Description	Fault location
53	05	Tape error. The tape should be changed and this routine repeated. (See explanation of Routine 53 in Section C.5.)	Tape
53	06	Interrupt from MTU by TU (tape unit) check.	Operator error
53	07	Interrupt from MIU.	Operator error
53	31	GAPC signal was not set within the specified period.	Interface cable; MIU PCA 1A05, 1A06, or distribution PCA; or 1A05 in the FMT
53	37	Beginning of tape cannot be detected.	Operator error, beginning of tape sensor
53	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code
54	01	MTU interrupt signal was not detected during backward run.	Beginning of tape sensor, or MTU PCA 1A05 or 1A06
54	02	Tape unit check.	Refer to MTU Error Code Table (See A.2)
54	03	Manual interruption.	Operator error
54	04	Auto cleaner did not return to normal position.	Auto cleaner
54	05	Temporary error of auto cleaner.	Auto cleaner
54	30	Tach pulse was not set within the specified period.	Operator error
54	31	GAPC (gap control) signal was not set within the specified period.	MTU PCA 1A05 or 1A06
54	32	MTU capstan motor error detected.	Capstan motor assembly
54	33	D.QTP signal detection circuit error detected.	PCA 1A05 in the FMT

Routine	Error	-	
number	Code		Fault location
54	34	Tach A/B signal error detected.	PCA 1A05 in the FMT
54	35	Dynamic reverse was detected.	Tape drive A PCA on MTU side panel, or PCA 1A02 in the MTU
54	36	Tach A/B signal error detected.	PCA 1A05 in the FMT
54	37	Beginning of tape was not detected.	Beginning tape sensor
54	8X	TAG Control was executed at the specified MTU address but failed.	Check MTU front panel for error code
54	96	Beginning of tape was not detected.	Beginning of tape sensor, or marker
54	98	Online signal was reset during rewind.	Operator error
55	01	Velocity retry count out.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or capstan motor assembly
55	02	Excessive retrys.	Capstan motor assembly
55	04	HNOIS signal was not detected.	Change tape and retry this routine; PCA 1A04 in the MTU, or PCA 1A06 in the FMT
55	05	Velocity change.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or capstan motor assembly
55	06	Slip check was detected.	Capstan roller
55	30	Tach pulse signal was not detected within the specified period.	Operator error
55	31	CAPC signal was not set within the specified period.	MTU PCA 1A05 or 1A06
55	32	MTU capstan motor error detected.	Capstan motor assembly

Routine number	Error Code	Description	Fault location
55	33	D.QTP signal detection circuit error detected.	PCA 1A05 in the FMT
55	34	Tach A/B signal error detected.	PCA 1A05 in the FMT
55	35	Dynamic reversal error was detected.	Tape drive A PCA on MTU side panel, or PCA 1A04 in the MTU
55	36	Tach A/B signal error was detected.	PCA 1A05 in the FMT
55	8X	TAG control was executed at the specified MTU address but failed.	
56	01	Loop alarm-left.	PCA 1A04 in the MIU, or capacitive sensor
56	02	Loop alarm-right.	PCA 1A04 in the MIU, or capacitive sensor
56	04	Air bearing alarm on, miscellaneous error.	Air supply of MTU
56	08	Ready signal was reset.	Operator error
56	11	Stop position at IBG (Inter Block Gap) is not correct.	Capstan motor assembly, tape drive A PCA on MTU side panel, or PCA 1A04 in the MTU
56	13	HNOIS signal was not detected.	Write/read printed circuit assembly
56	15	Excessive speed change over + 7% of the specified value.	Tape drive A PCA on MTU side panel, or PCA 1A04 in the MTU
56	31	CAPC signal was not set within the specified period.	MTU PCA 1A05 or 1A06
56	32	Capstan motor error detected.	Capstan motor assembly
56	33	D.QTP signal detection circuit error detected.	PCA 1A05 in the FMT
56	34	Tach A/B signal error detected.	PCA 1A05 in the FMT

Routine number	Error Code	Description	Fault location
56	35	Dynamic reversal error was detected.	Tape drive A PCA on MTU side panel, or PCA 1A04 in the MTU
56	36	Tach A/B signal error was detected.	PCA 1A05 in the FMT
56	8X	TAG control was executed at the specified MTU address but failed.	
57	01	Velocity retry count out.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or capstan motor assembly
57	02	Excessive retrys.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or capstan motor assembly
57	04	HNOIS signal was not detected.	Change tape and retry this routine. PCA 1A04 in the MTU, or PCA 1A06 in the FMT
57	05	Velocity change.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or capstan motor assembly
57	06	Slip check was detected.	Capstan roller
57	30	Tach pulse signal was not detected within the specified period.	Operator error
57	31	CAPC signal was not set within the specified period.	MTU PCA 1A05 or 1A06
57	32	MTU capstan motor error detected.	Capstan motor assembly
57	33	D.QTP signal detection circuit error detected.	PCA 1A05 in the FMT
57	34	Tach A/B signal error detected.	PCA 1A05 in the FMT
57	35	Dynamic reversal error was detected.	Tape drive A PCA on MTU side panel, or PCA 1A04 in the MTU

Routine number	Error Code	Description	Fault location
57	36	Tach A/B signal error was detected.	PCA 1A05 in the FMT
57	38	Beginning of tape was detected where not expected.	Beginning of tape sensor, or tape
57	8X	TAG Control was executed at the specified MTU address but failed.	
57	90	Group coded recording status was not set by command tag operation.	532401U
58	01	Loop alarm-left.	Tape drive B PCA or MTU side panel, or capacitive sensor
58	02	Loop alarm-right.	Tape drive B PCA or MTU side panel, or capacitive sensor
58	04	Air bearing alarm on miscellaneous error.	Air supply of MTU
58	08	Ready signal was reset.	Operator error
58	11	Stop position at IBG (inter block gap) is not correct.	Capstan motor assembly, tape drive B PCA or MTU side panel, or PCA 1AO4 in the MTU
58	13	HNOIS signal was not detected.	Write/read printed circuit assembly
58	15	Excessive speed change over + 7% of the specified value.	Tape drive B PCA or MTU side panel, or PCA 1A04 in the MTU
58	31	CAPC signal was not set within the specified period.	MTU PCA 1A05 or 1A06
58	32	MTU capstan motor error detected.	Capstan motor assembly
58	33	D.QTP signal detection circuit error detected.	PCA 1A05 in the FMT
58	34	Tach A/B signal error detected.	PCA 1A05 in the FMT

Routine number	Error Code		Fault location
58	35	Dynamic reversal error was detected.	Tape drive B PCA or MTU side panel, or PCA 1A04 in the MTU
58	36	Tach A/B signal error was detected.	PCA 1A05 in the FMT
58	8X	TAG control was executed at the specified MTU address but failed.	
60	01	Either bit of TSNS (time sense) 0-8 was detected.	Erase head, or cable between erase head and write/read PCA
60	02	Tach pulse was stopped during erase diagnostics.	Operator error
60	30	Tach pulse stopped during erase.	Operator error
60	31	GAPC (Gap Control) signal was not detected within the specified period during erase.	MTU PCA 1A05 or 1A06 or operator error
60	8X	TAG control was executed at the specified MTU address but failed.	Check the MTU front panel for an error code
61	30	Tach pulse stopped during erase.	Operator error
61	31	GAPC signal was not detected within the specified period during erase.	MTU PCA 1A05 or 1A06 or operator error
61	32	Tach pulse signal was not set within the specified period.	MIU PCA 1A05 or 1A06
61	33	QTP (quarter tach pulse) signal detection error.	MIU PCA 1A05 or 1A06
61	34	Tach A/B signal error detected.	MTU PCA 1A05 or 1A06
61	35	Dynamic reverse error was detected.	MTU PCA 1A05 or 1A06
61	38	Beginning of tape was detected where signal was not expected.	Beginning of tape sensor or tape

Routine number	Error Code	Description	Fault location
61	61	During WRT (write), suitable place for diagnostics was not found within 15 m from beginning of tape.	Tape error
61	62	During WRT (write), tach pulse stopped.	Operator error
61	63	Although suitable place for diagnostics was found during WRT (write), a trap was issued from MTU.	Operator error
61	64	During WRT (write), SAGC check error was set incorrectly.	Write/read printed circuit assembly, MTU PCA 1A05 or 1A06
61	65	SAGC (self adjust gain control) check error was incorrectly set in read mode, although it was not expected.	Write/read PCA
61	66	SAGC check detection circuit error detected.	Write/read PCA
61	67	Although TU (tape unit) interrupt was found, the cause is not SAGC check.	Write/read PCA
61	68	Count of SAGC counter error detected.	Write/read PCA, or MTU PCA 1A05 or 1A06
61	69	Count is preset in SAGC counter, but GSD was not performed in MTU.	Write/read PCA
61	8X	TAG control was executed at the specified MTU address but failed.	Check the MTU front panel for an error code
61	90	GCR (group coded recording) status was not set by command tag operation.	532401U
62	01	Early begin read check was detected.	Write/read PCA or head
62	02	Slow check was detected.	Capacitive sensor

Routine number	Error Code	Description	Fault location
62	03	Start read check was detected.	PCA 1A04 in the MTU, tape drive A PCA on MTU side panel, or PCA 1A04 in the FMT
62	04	While waiting for POSA (postamble) signal, DBOB (detection of beginning of block) signal was reset.	Write/read PCA
62	05	Postamble error was detected.	Write/read PCA
62	06	End data check was detected.	Write/read PCA
62	07	Start read check was detected because tape speed was incorrect.	PCA 1A04 in the MTU, or tape drive A PCA on MTU side panel
62	08	Tape speed was incorrect when postamble signal was reported.	PCA 1A04 in the MTU, or tape drive A PCA on MTU side panel
62	21	Tach stop signal was set.	Operator error
62	22	Tape error. The tape should be changed and this routine should be repeated.	Operator error
62	23	BCY signal was not set.	PCA 1A05 in the FMT
62	26	BIBSY (bus in busy) signal was not reset.	PCA 1A07 in the FMT
62	30	Tach pulse stopped during erase.	Operator error
62	31	GAPC (gap control) signal was not detected within the specified period during erase.	MTU PCA 1A05 or 1A06 or operator error
62	32	Tach pulse signal was not set within the specified period.	MIU PCA 1A05 or 1A06
62	33	QTP (quarter tach pulse) signal detection error.	MTU PCA 1A05 or 1A06
62	34	Tach A/B signal error detected.	MTU PCA 1A05 or 1A06
62	35	Dynamic reverse error was detected.	MIU PCA 1A05 or 1A06

Routine number	Error Code	Description	Fault location
62	38	Beginning of tape was detected where signal was not expected.	Beginning of tape sensor, or tape
62	40	Deskewing buffer check was detected.	PCA 1A02 in the FMT
62	41	Skew error was detected.	PCA 1A02 in the FMT
62	42	Drop out error was detected.	PCA 1A02 in the FMT
62	43	VRC (vertical redundancy check) error was detected.	PCA 1A02 in the FMT
62	44	Multi-track error was detected.	PCA 1A02 in the FMT
62	45	Postamble error was detected.	PCA 1A02 in the FMT
62	46	Write trigger VRC (vertical redundancy check) error was detected.	PCA 1A02 in the FMT
62	47	Write bus out check was detected.	PCA 1A06 or 1A07 in the FMT
62	48	Over-run error (in offline mode only) was detected.	PCA 1A06 or 1A07 in the FMT
62	54	Transfer in, register parity error was detected.	PCA 1A06 or 1A07 in the FMT
62	55	CRCA-CRCB error was detected.	PCA 1A06 in the FMT
62	56	FMT detected bus parity error in controller interface.	PCA 1A07 in the FMT
62	61	During the write (WRT) mode, a suitable place for diagnostics was not found within 15 m from beginning of tape.	Tape error
62	62	During the write (WRT) run, tach pulse stopped.	Operator error
62	63	Although a suitable place for diagnostics was found during the write (WRT) mode, a trap was issued from MTU.	Operator error

Routine number	Error Code	Description	Fault location
62	64	During the write (WRT) mode, SAGC (self adjust gain control) check error was set incorrectly.	Write/read printed circuit assembly, or MTU PCA 1A05 or 1A06
62	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code
62	90	GCR (group coded recording) status was not set by command tag operation.	532401U
63	01	Early begin read check was detected.	Write/read PCA, or head
63	02	Slow check was detected.	Capacitive sensor
63	03	Start read check was detected.	PCA 1A04 in the MTU, tape drive A PCA in MTU side panel, or PCA 1A04 in the FMT
63	04	While waiting for POSA (postamble) signal, DBOB (detected beginning of block) signal was reset.	Write/read PCA
63	21	Tach stop signal was set.	Operator error
63	22	Tape error. The tape should be changed and this routine should be repeated.	Operator error
63	23	BCY signal was not set.	PCA 1A05 in the FMT
63	26	BIBSY (bus in busy) signal was not reset.	PCA 1A07 in the FMT
63	30	Tach pulse stopped during erase.	Operator error
63	31	GAPC (gap control) signal was not detected within the specified period during erase.	MTU PCA 1A05 or 1A06 or operator error
63	41	Skew error was detected.	PCA 1A02 in the FMT
63	42	Drop out error was detected.	PCA 1A02 in the FMT

Routine number	Error Code	Description	Fault location
63	43	VRC (vertical redundancy check) error was detected.	PCA 1A02 in the FMT
63	44	Multi-track error was detected.	PCA 1A02 in the FMT
63	45	Postamble error was detected.	PCA 1A02 in the FMT
63	46	Write trigger VRC (vertical redundancy check) error was detected.	PCA 1A06 in the FMT
63	47	Write bus out check was detected.	PCA 1A06 or 1A07 in the FMT
63	48	Over-run error (in offline mode only) was detected.	PCA 1A06 or 1A07 in the FMT
63	54	Transfer in, register parity error was detected.	PCA 1A06 or 1A07 in the FMT
63	55	Cyclic Redundancy Check A and B (CRCA—CRCB) error was detected.	PCA 1A06 in FMT
63	56	FMT detected bus parity error in the host controller interface.	PCA 1A07 in the FMT, or Controller
63	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code
64	01	Tach signal was stopped during waiting first data.	Operator error
64	02	Tach signal was stopped during waiting LRC.	Operator error
64	03	NOIS (Noise) signal was set.	Write/read PCA, or head
64	20	Velocity retry excessive.	PCA 1A04 in the MTU, or tape drive A PCA on MTU side panel
64	21	Tach signal was stopped.	Operator error
64	22	Tape error. The tape should be changed and this routine should be repeated.	Tape

Routine number	Error Code		Fault location
64	23	BCY signal was not set.	PCA 1A05 in the FMT
64	26	BIBSY (bus in busy) signal was not reset.	PCA 1A07 in the FMT
64	30	Tach pulse stopped during erase.	Operator error
64	31	GAPC (gap control) signal was not detected within the spedified period during erase.	MIU PCA 1A05 or 1A06, or operator error
64	41	Skew error was detected.	PCA 1A01 in the FMT
64	46	Write trigger VRC (vertical redundancy check) error was detected.	PCA 1A06 in the FMT
64	47	Write bus out check was detected.	PCA 1A06 or 1A07 in the FMT
64	48	Over-run error (in offline mode only) was detected.	PCA 1A06 or 1A07 in the FMT
64	51	VRC (vertical redundancy check) error in nonreturn to zero I mode was detected.	PCA 1A01 in the FMT
64	52	LRC (longitudinal redundancy check) error was detected.	PCA 1A01 in the FMT
64	54	Transfer in, register parity error was detected.	PCA 1A06 or 1A07 in the FMT
64	55	CRCA-CRCB (cyclic redundancy check A and B) error was detected.	PCA 1A06 in the FMT
64	56	FMT detected bus parity error in the host controller interface.	PCA 1A07 in the FMT, or host controller
64	8X	TAG control was executed at the specified MTU address but failed.	
64	98	Manual interrupt to MTU.	Operator error

Routine number	Error Code	Description	Fault location
65	10	Tape error. Change tape and retry this routine.	Tape
65	21	Manual interruption.	Operator error
65 (o	30 r)	Complete read signal was not detected at slice level 15%.	Amplitude setting of write/read PCA
65	30	Tach pulse stopped during erase.	Operator error
65	31	GAPC signal was not detected within the specified period during erase.	MTU PCA 1A05, 1A06, or operator error
65	38	Beginning of tape was detected where not expected.	Beginning of tape sensor, or tape
65	50	Complete read signal was not detected at slice level 41%.	Amplitude setting of write/read PCA
65	70	Complete read signal was not detected at slice level 51%.	Amplitude setting of write/read PCA
65	8X	TAG control was executed at the specified MTU address but failed.	
65	90	Complete read signal was not detected at slice level 64%.	Amplitude setting of write/read PCA
65	96	Beginning of tape was not detected.	Operator error
65	98	Manual interruption during rewinding.	Operator error
66	01	IBG (Inter Block Gap) length is too long in phase encode mode.	MTU PCA 1A05, 1A06, or dirty tape path
66	02	IBG length is too short in phase encode mode.	MTU PCA 1A05, 1A06, or dirty tape path
66	03	IBG length is too long in group coded recording mode.	MTU PCA 1A05, 1A06, or dirty tape path
66	04	IBG length is too short in group coded recording mode.	MTU PCA 1A05, 1A06, or dirty tape path
66	21	Manual interruption.	Operator error

Routine number	Error Code	Description	Fault location
66	22	Tape error. Change tape and retry this routine.	Tape
66	30	Tach pulse stopped during erase.	Operator error
66	31	GAPC signal was not detected within the specified period during erase.	MTU PCA 1A05, 1A06, or operator error
66	38	Beginning of tape was detected where not expected.	Beginning of tape sensor, or tape
66	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code
66	90	Group coded recording status not set by command tag operation.	532401U
66	96	Beginning of tape was not detected.	Operator error
66	98	Tape error. Change the tape and retry.	Tape
70	01	Excessive feed through signal was detected.	Write/read head
70	21	Manual interruption.	Operator error
70	22	Tape error. Change the tape and retry.	Tape
70	38	Beginning of tape detected where not expected.	Beginning of tape sensor, or tape
70	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code
70	90	Group coded recording status cannot be set by command tag operation. After rewind end, tape is not at beginning of tape.	Operator error

Routine number	Error Code	Description	Fault location	
70	96	Group coded recording status cannot be set by command tag operation. After rewind end, tape is not at beginning of tape.	Operator error	
70	98	Manual operation error.	Operator error	
71	01	Excessive cross-talk signal was detected.	Write/read head	
71	22	Tape error. Change the tape and retry.	Tape	
71	38	Beginning of tape detected where not expected.	Beginning of tape sensor, or tape	
71	8X	TAG control was executed at the specified MTU address but failed.	Check MTU front panel for error code	
71	96	Group coded recording status cannot be set by command tag operation. After rewind end, tape is not at beginning of tape.	Operator error	
71	98	Manual operation error.	Operator error	
73	01	WIM (write tape mark command) retry excessive in phase encode mode.	Write/read PCA	
73	02	Manual interrupt (reset key).	Operator error	
73	03	Drop out error.	Write/read PCA	
73	2X	REJECT error was detected in command 1 through 8 (see footnote 1).	MTU PCA 1A05, 1A06, write/read PCA, or PCA 1A06 in the FMT	
73	3X	Excessive velocity change during write operation. PCA 1A04 in the Moreover or tape drive A Post MTU side panel		
73	4X	Start read check was detected.	Capstan motor assembly or PCA 1AO4 in the FMT	

Routine number	Error Code		Fault location
73	5X	PREC (partial record), EDC (end data check) check was detected.	Capstan motor assembly or PCA 1A04 in the FMT
73	6X	Multi-track error was detected.	Capstan motor assembly or PCA 1A04 in the FMT
73	7X	VRC (vertical redundancy check) and CRC (cyclic redundancy check) skew error was detected.	Write/read PCA, head, or PCA 1A06 in the FMT
73	05	IDBCK was detected.	Write/read PCA or head
73	06	Beginning of tape was detected during backward operation.	Tape error, or auto cleaner
73	07	OVRN (not overrun) was detected during offline diagnostics.	PCA 1A07 in the FMT
74	01	WIM (write tape mark command) retry excessive in phase encode mode.	Write/read PCA
74	02	Manual interruption (reset key).	Operator error
74	03	Drop out error.	Write/read PCA
74	2X	REJECT error was detected in command 1 through 8 (see footnote ¹).	MTU PCA 1A05, 1A06 Write/read PCA, or PCA 1A06 in the FMT
74	3X	Excessive velocity change during write operation.	PCA 1A04 in the MTU, or tape drive A PCA on MTU side panel
74	4X	Start read check was detected.	Capstan motor assembly, or FMT PCA 1A04
74	5X	PREC, EDC check was detected.	Capstan motor assembly, or FMT PCA 1A04
74	6X	Multi-track error was detected.	Capstan motor assembly, or FMT PCA 1A04
74	7X	VRC, CRC, skew error was detected.	PCA 1A02 or 1A06 in the FMT
1 1.=BS	SP, 2=FS	PF, 3=SP, 4=RD, 5=BRD, 6=WRT, 7=WI	M, 8=ERS

Routine number	Error Code	Description	Fault location
74	05	IDBCK (ID burst check) was detected.	Write/read PCA, or head
74	06	Beginning of tape was detected during backward operation.	Tape error, or auto cleaner
74	07	OVRN (not overrun) was detected during offline diagnostics.	PCA 1A07 in the FMT
75	01	WIM (write tape mark) retry excessive in phase encode mode.	Write/read PCA
75	02	Manual interruption (reset key).	Operator error
75	2X	REJECT error was detected in command 1 through 8 (see footnote ¹ .)	MTU PCA 1A05, 1A06, Write/read PCA, or PCA 1A06 in the FMT
75	3X	Excessive velocity change during write operation.	PCA 1A04 in the MTU, or tape drive A PCA on MTU side panel
75	7X	VRC (vertical redundancy check) CRC (cyclic redundancy check) skew error was detected.	PCA 1A01 or 1A05 in the FMT
75	06	Beginning of tape was detected during backward operation.	Tape error, or auto cleaner
75	07	OVRN (overrum) was detected during offline diagnostics.	PCA 1A07 in the FMT
79	01	SLTAG (select TAG) signal was not set correctly.	PCA 1A05 int he FMT
79	02	Inconsistency between FMT and distribution PCA.	Cable between PCA 1A05 and distribution board in the FMT
79	03	TAGI signal was not set.	MTU interface cable
79	04	MTU ready signal or online signal was not set.	532403U
79	05	DVENB (device enable) signal was not set.	FMT distribution PCA
79	06	DVBSY (device busy) signal was not set.	FMT distribution PCA

Routine number	Error Code	Description	Fault location			
79	07	LWR (loop write read) FMT signal was not set correctly.	PCA 1A05 in the FMT			
79	08	DBMPX (device bus multiplex) PCA 1A05 in the FMT signal was not set correctly.				
79	09	Error detected at interface bus when LWR FMT mode was set, or error detected in DBMPX function.	PCA 1A05 in the FMT			
79	10	Error was detected at interface bus when LWR FMT mode was set (P bit).	PCA 1A05 in the FMT			
79	11	Error detected at interface bus when LWR FMT mode was set (P bit), or error detected in DBMPX function.	532403U, MTU interface cable, or FMT distribution PCA			
79	12	Sense tag was not set correctly.	PCA 1A05 in the FMT			
79	13	MPXBO (multiplex bus out) signal was not set correctly.	PCA 1A05 in the FMT			
79	14	LWR FMT or DBMPX (device bus multiplex) signal error.	PCA 1A05 in the FMT			
79	15	Online and ready signal is always set in MTU.	532403U			
79	16	MTU indicates operation possible at all times.	532403U			
79	17	Interface cables between FMT and MTU connected incorrectly, or the diagnostics MTU address was specified by mistake.	Cable connection, or address mistake			
79	18	Although SLTAG (select TAG) signal is reset, operation possible was posted.	Distribution PCA in the FMT			
80	37	Although interrupt signal from MTU was detected, beginning of tape was not detected.	Operator error			
1 1=BS	SP, 2=FS	PF, 3=SP, 4=RD, 5=BRD, 6=WRT, 7=WI	IM, 8=ERS			

Routine number	Error Code	Description		Fault location		
80	38	Beginning of tape was when not expected.	detected	Operator error		
80	8X	TAG control was execuspecified MTU address failed.		Check MTU front panel for error code		
80	WW	WW is defined as foll	.ows:			
		FWD: WW 43 through 5 WW indicates quantity below.	BWD: WW 63 through 72 means capstan needs alignme FWD: WW 43 through 54 means azimuth needs adjustment www indicates quantity of skew for each error code below. (See Section K for checks and adjustments.)			
		Error cod FWD	le BWD	Quantity of skew		
		43	63	50		
}		44	64	46		
]		45	65	42		
]		46	66	38		
		47	67	33		
1		50	70	29		
		51	71	25		
		52	72	21		
		53		17		
		54 		13		
83	01	Manual interruption o while executing this		Operator error		
83	10	Read amplifier setting low and requires adjusted		Read amplifier adjustment		
83	11	Read amplifier settin high and requires adj		Read amplifier adjustment		
83	90	Group code recording status was not set by command tag operation.		532401U		
90	8X	TAG control was execuspecified MTU address failed.		Check MTU front panel for error code		

Routine	Error		
number	Code	Description	Fault location
91	01 (r)	Although the device sense was executed, the response signal (TAGI signal) was not set.	Distribution PCA in the FMT
91	01	Online signal was reset during execution of DSE (data security erase) command.	Operator error
91	8X	TAG Control was executed at the specified MTU address but failed.	Check MTU front panel for error code
91	96	Beginning of tape marker was not detected during rewind.	Operator error, or beginning of tape sensor
91	98	Online signal was reset by rewind.	Operator error
92	YY	The code number YY shows the result of counting the number of data checks until the detection of tape mark. The number is decimal.	
93	37	Beginning of tape was not detected during backward mode.	Operator error, or beginning of tape sensor
93	YY	The code number YY indicates the number of data checks when write operation is executed in group coded recording from beginning to end of tape. The number is decimal.	
94	YY	The code number YY indicates the number of data checks when the write operation is executed in phase encode mode from beginning of tape to end of tape. The number is decimal.	
95	YY	The code number YY indicates the number of data checks when the write operation is executed in nonreturn to zero I mode from beginning of tape to end of tape.	

Routine number	Error Code	Description	Fault location	
96 (c	37 r)	Beginning of tape was not detected during backward mode.	Operator error, or beginning of tape sensor	
96	37	Beginning of tape could not be detected. Operator error E sensor		
96	8X	TAG control was executed at the specified MTU address but failed.	Check the MTU front panel for an error code	
97	01	Manual interruption during space to end of tape.	Operator error	
97	8X	TAG control was executed at the specified MTU address but failed.	Check the MTU front panel for an error code	
98	01	MP (microprogram) halt was indicated during ROM SCAN operation but MP CONTROL FLAG (STEP) was not set correctly.	PCA 1A08 in the FMT, or diagnostics panel	
98	02	MP halt was indicated, but halt bit was not set correctly (bit 10).	PCA 1A08 in the FMT, or diagnostics panel	
98	03	ROM SCAN (\$E4, CNT) is indicated, but MP controller flag was not set correctly (bit 5).	PCA 1A08 in the FMT, or diagnostics panel	
98	04	Parity error was detected during ROM SCAN operation, PERR (parity error) bit was set (bit 11).	PCA 1A07 in the FMT	
98	05	MP halt was indicated, but MP controller FLAG (STEP) was not set correctly.	PCA 1A08 in the FMT	
98	06	MP halt was indicated, but halt bit was not set correctly (bit 10).	PCA 1A08 in the FMT	
98	07	MP halt mode was not reset.	set. PCA 1A08 in the FMT, or diagnostics panel	
98	08	ROM scan mode was not reset.	PCA 1A08 in the FMT, or diagnostics panel	

Routine	Error		
number	Code	Description	Fault location
98	39	MP halt was indicated during ROM SCAN mode and MP halt mode was not set.	PCA 1A08 in the FMT
99	01	Lamp test was incorrect in power on RST routine.	PCA 1A08 in the FMT, or diagnostics panel
99	02	PHLT (processor halt) bit was ON in idle, or cable was disconnected.	Cable between panel and PCA 1A08 in the FMT
99	03	FMT detected error in POWDIA check.	PCA 1A02, 1A05, 1A06, or 1A08 in the FMT
99	04	CS (control storage) parity error was detected.	PCA 1A08 in the FMT
99	05	Register parity error was detected.	PCA 1A01, 1A02, 1A05, 1A06, 1A07, or 1A08 in the FMT
99	06	M PERR (parity error) bit on, but no CS (control storage) or register parity error existed.	PCA 1A07 in the FMT
99	11	Address compare (\$CX, CNT) function was not performed.	PCA 1A08 in the FMT
99	12	MP (microprogram) control (\$EX, CNT) function was not performed.	PCA 1A08 in the FMT
99	22	FMT was not set to diagnostics mode, but offline bit was not set.	PCA 1A08 in the FMT, or diagnostics panel
99	23	When setting FMT to diagnostics mode, busy bit was on.	PCA 1A07 in the FMT
99	24	FMT was set to diagnostics PCA 1A08 in the mode, but M PHLT (processor halt) bit was on.	
99	25	FMT was set to diagnostics mode, but CSPER (control storage parity error) bit was on.	PCA 1A07 in the FMT

Routine	Error			
number	Code	Description	Fault location	
99	26	FMT was set to diagnostics mode, but register parity error bit was on.	PCA 1A08 in the FMT	
99	27	Routine number was not set correctly.	PCA 1A08 in the FMT, or diagnostics panel	
99	28	TU (tape unit) address was not set correctly.	PCA 1A08 in the FMT, or diagnostics panel	
99	29	Diagnostics command was issued, but duty on timed out.	PCA 1A02, 1A06, 1A07, or 1A08 in the FMT	
99	40	After FMT was set to diagnostics mode, busy signal was set, but diagnostics condition flag within FMT was not set.	PCA 1A08 in the FMT	
99	41	BUSY bit was off, but IBUSY bit was on.	PCA 1A08 in the FMT	
99	42	BUSY bit was on, but IBUSY bit was off.	PCA 1A07 in the FMT	
99	43	After diagnostics routine was started, MPHLT was detected.	PCA 1A08 in the FMT	
99	51	Error flag was on at diagnostics end, but error code is all 0.	PCA 1A08 in the FMT	
99	59	Error flag was off at diagnostics end, but error code was all 0.	PCA 1A08 in the FMT	
99	61	IM test error in power on test routine for diagnostics panel.	PCA 1A08 in the FMT, or diagnostics panel	
99	62	Microprogram of diagnostics panel is in error.	Diagnostics panel	

Routine number	Error Code	Description	Fault location
99	99	Diagnostics was initiated at the specified MTU address and failed because MTU is in not- ready status.	If MTU is ready, run Routine 79. Routines 10, 11, 12, 14, and 15 can run even if the MTU is in not-ready status, but the MTU should be powered on. FMT checks TAG in signal response.
FF	FF	Routine number error (occurs with online diagnostics or field tester only).	Indicated routine number was not 00 through 99

This section provides a description of the routines for both FMT and MTU offline and online diagnostics. The description of each routine includes:

- (1) The routine number and title. Routines are listed in numerical order from 00 to 99.
- (2) The conditions that are required for that routine, if applicable.
- (3) A summary of error codes for that routine.
- (4) A description of what the routine diagnoses and how it functions.

In general, during the execution of a given routine, lamp 1 on the field tester panel will remain on. When the routine is completed or terminated for any reason, lamp 1 will go off. If an error was detected, lamp 8 will go on. To determine the routine number and error code number:

- (1) Set the field tester switches S0 through S7 to \$35, and then toggle the CNT switch.
- (2) The routine number is displayed on the field tester lamps in hex notation.
- (3) Set the field tester switches S0 through S7 to \$36, and toggle the SSS switch.
- (4) The error code is displayed on the field tester lamps in hex notation.
- (5) Consult section C.4, Error Code Table and Fault Isolation, for the appropriate error code.
- (6) Consult the following list for a more detailed description of the routine itself.

Routine 00: Test All Diagnostic Routines.

Conditions: Host controller can be powered off even if interface cables are connected.

Error Codes:

- 78 00 All applicable routines listed in Section C.4 (routines 10 to 78) were tested, and there were no errors.
- XX YY Error was detected in routine XX, and its error code is YY.
- 99 XX The Test All Diagnostics routine implementation was not successful. Refer to the Error Code Table in Section C.4.

- Routines 10 through 78 listed in Section C.4 are executed sequentially. Undefined routine numbers are skipped.
- If the addressed MTU is a dual-density model, the diagnostic routine for the 800 rpi mode is skipped.
- When an error is detected, the program terminates at that routine. Lamp L8 on the field tester lights, and the error code is stored in the FMT register. The error code can be read using the field tester.

Routine 01: Test All Routines (Host Controller Power On).

Conditions:

If interface cables between the formatter and host controller are connected, the host controller power must be turned on. Some routines test the bidirectional data bus of the controller interface by routing data from the driver (DV) to the receiver (RV). If the controller is not pulled up by +5V, the signal level of the data bus cannot be pulled up to high level. This would invalidate the test.

Error Codes:

- 78 00 All applicable routines listed in Section C.4 (routines 10 to 78) were tested, and there were no errors.
- XX YY Error was detected in routine XX, and its error code is YY.
- 99 XX The Test All Diagnostics routine implementation was not successful. Refer to the Error Code Table in Section C.4.

General Description:

- Routines 10 through 78 listed in Section C.4 are executed sequentially. Undefined routine numbers are skipped.
- The byte count to be written in LWR (loop write read) or normal WRT (write) routines is longer than routine 00. The block length of LWR or normal WRT routine in routine 01 is up to 4K bytes, but in routine 00 it is only 55 bytes.
- Execution time for each model:

50 ips DD 4 minutes, 43 seconds 50 ips TD 4 minutes, 54 seconds 75 ips DD 5 minutes, 00 seconds 75 ips TD 5 minutes, 08 seconds 125 ips DD 5 minutes, 28 seconds

Execution time may be longer, depending on the tape used.

Routine 10: Microprocessor Self Test Diagnostics.

Error Codes:

- 10 00 No error in FMT microprogram.
- 10 77 Microprocessor error detected.
- 00 97 MTU is not operational.

General Description:

This test program checks correct performance of all commands of the FMT processor by means of condition code just before and after command execution and some changes in local memory.

Explanation:

Local memory used are registers W0, W1, SB22, and SB23. EXR is not used. The tests are applied in the following order:

- (1) Unconditional branch \$0000 \$0001
 - \$0003 \$1FF0

\$1FFX - \$0005

- (2) Branch on condition
- (3) Test bit branch
- (4) Exclusive—OR
- (5) Plus
- (6) Minus
- (7) Branch on condition indirect
- (8) Call on condition
- (9) Register operation
- (10) OR, AND, etc.
- (11) Test bit call
- (12) Move half indirect
- (13) Move full indirect
- (14) Branch indirect
- (15) Call indirect
- (16) Branch on condition indirect.

Routine 11: LSR (Local Storage Register) Test Partial.

Error Codes:

- 11 00 Local storage memory can be sensed and selection of local storage is confirmed.
- 11 XX An error was detected in register selection circuit, write bus, or read bus of LSR.
- 00 97 MTU is not operational.

Routine 11: LSR (Local Storage Register) Test Partial. (continued)

General Description:

One local memory address is selected and all "0" and all "1" data is written into RAM. By reading local memory data, the write bus and read bus around LSR RAM is confirmed. The local memory address is then changed and the test is repeated at the new address. In this way, the register select lines are checked W0 - W7 (address \$10 - \$17). When run in offline diagnostics, this routine runs normally even if the MTU is in a power-on state and has a not-ready status.

Routine 12: Local Memory Read/Write Test.

Error Codes:

- 12 00 All local storage RAM (64 bytes) in the FMT is tested and no error was detected.
- 12 XX Error is detected in the RAM.
- 00 97 MTU is not operational.

General Description:

- o All "1's" are written in LM (local memory). When all "1's" are sensed, then all "0's" are written in. If all "0's" are sensed. "0's" are checked. The data of LM, which must be stored in FMT, is saved in LM whose data has been confirmed.
- o When run in offline diagnostics, this routine runs normally even if the MTU is in a power-on state and has a not-ready status.

Routine 14: External Register Write and Sense Bus Test.

Conditions: FMT microprocessor self-test diagnostic routine has been executed without error.

Error Codes:

- 14 00 Basic execution of read/write to external register in routine has no error.
- 14 XX Error detected.
- 00 97 MTU is not operational.

- Selects registers that can be sensed by the FMT microprocessor. Register select circuit, register write clock, write bus, and read bus are checked.
- When run in offline diagnostics, the routine runs normally even if the MTU is in a power-on state and has a not-ready status.

Routine 14: External Register Write and Sense Bus Test. (continued)

Tests are applied with the following order:

- (1) Register address \$40 through \$4F
- (2) PCA 1A08 in the FMT
- (3) PCA 1A07 in the FMT
- (4) PCA 1A06 in the FMT
- (5) PCA 1A02 in the FMT
- (6) PCA 1A01 in the FMT
- (7) PCA 1A05 in the FMT.

Routine 15: Timer Function Test.

Error Codes:

- 15 00 Basic function of the FMT microprogram counter FMT is confirmed.
- 15 XX Error detected.
- 00 97 MTU is not operational.

General Description:

- When the hardware timer (16 bits) for the FMT microprogram is in the clock count mode, function of timer over flow and counter preset is checked.
- When run in offline diagnostics, the routine runs normally even if the MTU is in a power-on state and has a not-ready status.

Routine 20: Diagnostic Program of Controller Interface Printed Circuit Assembly - 1.

Error Codes:

- 20 00 Diagnostics successfully completed with no errors.
- 20 XX Error detected.

- After writing test patterns into all registers and register files that can be read/written, this routine confirms that the pattern is sensed.
- For registers that cannot be written, this routine confirms data comparison within this routine.
- Before this routine, data comparison of data bus and tag control between MTUs and the formatter has not been confirmed.
- BMX registers \$50 through \$57 are tested only in online diagnostics.

Routine 21: Diagnostic Program of Controller Interface Printed Circuit Assembly - 2.

Error Codes:

- 21 00 Diagnostics successfully completed with no errors.
- 21 XX Error detected.

General Description:

- This routine is the same as Routine 20 during diagnostics.
- There are some differences in the offline mode; for example: SSC and TREQ signal are also tested in this routine.
- This routine does not check register bits that cannot be turned on/off while formatter is in an online status.

Routine 22: Diagnostic Program of MTU Interface Printed Circuit Assembly.

Error Codes:

- 22 00 Diagnostics successfully completed with no errors.
- 22 XX Error detected.

General Description:

- After writing test pattern in registers that can be read/written, this routine confirms that the pattern can be sensed.
- This routine confirms timer controls and repositioning counter control bits.

Routine 23: Routine to Confirm MIU Selection.

Error Codes:

- 23 00 Diagnostics successfully completed with no errors.
- 23 XX Error detected.

- o This routine checks all connected MTUs used by the FMT.
- o MTU selection logic is checked by using a communication register in the MTU. First bit 4 of communication register 1 in addressed MTU is set. Then, this routine checks that bit 4 of all other MTUs is off.

Routine 24: FMT/MTU Data Bus Test.

Error Codes:

- 24 00 Diagnostics successfully completed with no errors.
- 24 OX Data bus error.
- 24 8X Tag control error.

General Description:

• This routine confirms that the MTU can be set to loop write/read status. If confirmed, the data bus between the formatter and MTU is checked using test patterns.

Routine 25: Tach Pulse Signals Test.

Error Codes:

- 25 00 Diagnostics successfully completed with no errors.
- 25 XX Error detected.

General Description:

• After moving tape, this routine diagnoses the sequence of QTP and FTP, the number of pulse signals, and tach stop detection.

Routine 26: Tape Speed Detection Circuit Test.

Error Codes:

- 26 00 Diagnostics successfully completed with no errors.
- 26 XX Error detected in the speed detection circuit.
- 26 8X Tag control error detected.

General Description:

• This routine moves the tape and verifies that no error exists in the gap control signal, speed detection, and speed change detection.

Routine 28: Repositioning Counter and Counter Control Function.

Error Codes:

- 28 00 Diagnostics successfully completed with no errors.
- 28 XX Error detected.
- 28 8X Tag control error detected.

Routine 28: Repositioning Counter and Counter Control Function. (continued)

General Description:

This routine moves the tape and confirms the following:

- The repositioning counters operate normally when the DFTP (diagnostic function tape positioning) signals are set.
- Carry bits are set at the correct timing.
- Carry bits and repositioning counters are reset.

Routine 29: Trap Circuit Test.

Error Codes:

29 00 Diagnostic routine successfully completed with no errors.

29 XX Error detected.

General Description:

(1) Timer trap test

This routine sets the timer in the FMT to start while in a trap suppressed status. The check timer trap (T.TMR) signal is set within a fixed time, and checks that a trap is not issued.

(2) Tach pulse trap test

This routine moves the tape forward, while in a trap suppressed status. (Trap mask bit and tach stop gate signal are set, but tach stop trap mask bit is reset.)

(3) MTU interrupt test

While in trap suppressed status, this routine moves the tape backward until the beginning of the tape is detected. The routine then checks that the device interrupt signal is asserted and that the microprogram is not trapped.

Routine 30: FMT Large-Scale Integration Scan Test.

Error Codes:

- 30 00 Diagnostics successfully completed with no errors.
- 30 OX Error detected in large-scale integration circuits of write formatter.
- 30 1X Error detected in large-scale integration circuits of read formatter.

General Description:

This routine applies data scan to the large-scale integration used in the write formatter and read formatter, and confirms that all large-scale integration flip-flops operate normally.

Routine 31: Time Sense and Block Format Decoder Test.

Error Codes:

- 31 00 Diagnostics successfully completed with no errors.
- 31 OX Error detected in the time sense diagnostics (MP [microprogram] mode).
- 31 1X Error detected in the time sense diagnostics (ALL1W [all "1's" write] mode).
- 31 2X Error detected in the block format diagnostics (read status).

General Description:

- After setting the formatter to loop write/read FMT mode, this routine repeats on/off motion of a specified pattern in DVBO (device bus out) register for a specified period of time. Then the routine confirms that time sense of all the bits are set. After a series of on/off repetitions, the routine confirms that time sense signals of all bits are reset.
- Next, this routine confirms that time sense signals are normally set/reset by means of an all "1\$" write function.
- Keeping the formatter in loop write/read FMT mode, this routine loops noise, block, and tape patterns for a given period, and confirms normal detection of the pattern and of the phase O.K. signals.

Routine 32: Loop Write/Read FMT Phase Encode Test.

Error Codes:

- 32 00 No error detected during loop write/read operation.
- 32 XX Data check or other error was detected.

- This routine executes loop write/read operation in the phase encoded mode, and checks that no error occurs and that the FMT function works normally.
- All variable frequency oscillator (VFO) tape speeds (50, 75, and 125 ips) are tested. Data is random, and block length is 4K bytes. When this routine is executed in Routine 00, block length is 55 bytes.

Routine 33: Loop Write/Read FMT Group Coded Recording Mode.

Error Codes:

- 33 00 Diagnostics routine successfully completed with no errors.
- 32 XX Error detected.

General Description:

- Same test as Routine 32 except for density mode.
- Routine performs tests in the group coded recording mode.

Routine 34: Loop Write/Read FMT Nonreturn to Zero I Mode.

Error Codes:

- 34 00 Diagnostics routine successfully completed with no errors.
- 34 XX Error detected.

General Description:

- Same test as Routine 32 except for density mode.
- Routine performs tests in the nonreturn to zero I mode. If the nonreturn to zero I read printed circuit assembly 1A01 is not installed in the FMT, this routine is bypassed.

Routine 35: Loop Write/Read TU Interface Phase Encode Mode.

Error Codes:

- 35 00 Diagnostics routine successfully completed with no errors.
- 35 XX Error detected.

General Description:

- This routine is the same as Routine 32 except for the loop position of write data.
- Loop write/read (LWR) tape unit (TU) interface operation in the phase encode mode.
- In this operation, write data loop is performed at DV/RV of the MTU logic printed circuit assembly.

Routine 36: Loop Write/Read TU Interface Group Coded Recording Mode.

Error Codes:

- 36 00 Diagnostics routine successfully completed with no errors.
- 36 XX Error detected.

Routine 36: Loop Write/Read TU Interface Group Coded Recording Mode. (continued)

General Description:

• This routine is the same as Routine 35 except that the mode is group coded recording.

Routine 37: Loop Write/Read TU Interface Nonreturn to Zero I Mode.

Error Codes:

37 00 Diagnostics routine successfully completed with no errors.

37 XX Error detected.

General Description:

• This routine is the same as Routine 35 except that the mode is nonreturn to zero I.

Routine 38: Loop Write/Read Read/Write Amplifier Phase Encode Mode.

Error Codes:

38 00 Diagnostics routine successfully completed with no errors.

38 XX Error detected.

General Description:

- The write-to-read read/write amplifier operation is performed in the phase encode mode.
- Tape speed depends on the specific MTU model, and the test is performed in normal speed only. Data is random.
- If the test is executed in Routine 00, block length is 55 bytes.
- If the test is executed in Routine 01 or Routine 38, block length is 4k bytes.

Routine 39: Loop Write/Read Read/Write Amplifier Group Coded Recording Mode.

Error Codes:

39 00 Diagnostics routine successfully completed with no errors.

39 XX Error detected.

- Same test as Routine 38 except for execution mode.
- First the tape is moved from beginning of tape and, for the MTU inner status, is set to group coded recording.
- Then, the loop read/write operation is executed in the group coded recording mode.

Routine 40: Error Correction Logic-Phase Encode Mode.

Error Codes:

- 40 00 Error correct function operates normally.
- 40 XX Error is detected in error correction circuit.

General Description:

- Masking one track, this routine executes the loop-write/read FMT operation (same as Routine 32) in the phase encode mode. Mask track is shifted from logical track 0 to track P. The test is performed in both the read status and write modes.
- Data and block length are the same as Routine 32. In this routine, loop write read operation is performed 18 times (nine mask patterns by two status).
- The routine also checks that the error track pointer is equal to masked track. VRC error is set in write status operation and is not set in read status operation. Confirms check functions in read circuit.

Routine 41: Group Coded Recording 1-Track Correction Test.

Error Codes:

- 41 00 Routine successfully completed with no errors.
- 41 XX Error detected.

General Description:

- This routine is executed with the FMT in the loop write/read mode of operation with one tape track masked.
- This routine confirms that the error correction function operates without error detection during write and read modes.

Routine 42: Group Coded Recording 2-Track Correction Test.

Error Codes:

- 42 00 Routine successfully completed with no errors.
- 42 XX Error detected.

- Mask pattern is shifted from logical track 0 and 1, 1 and 2, 2 and 3, ..., to 7 and P.
- This routine confirms that the two-track correction function operates without error detection during read status and that a VRC error is detected in the write mode.

Routine 43: Group Coded Recording 3-Track Correction Test.

Error Codes:

- 43 00 Error detection circuit operates normally.
- 43 XX Error detected in the error detection function.

General Description:

- This routine is executed with the FMT in the loop write/read mode of operation with three tape tracks masked.
- The mask tracks are logical tracks 1, 4 and 6. This routine confirms the error detection function and that the pointer circuit operates normally.

Routine 44: Phase Error Pointer Test.

Error Codes:

- 44 00 The phase error pointer circuit in read printed circuit assembly functions normally.
- 44 XX Error detected in phase error pointer circuit.

General Description:

• This routine exercises the issue phase error function in the phase encode and group coded recording loop write/read modes. The phase is inverted by force, which causes the phase error signal to be generated in the variable frequency oscillator (VFO) printed circuit assembly (PCA 1A04 in the FMT). The phase error track is one track and is shifted from track 0 to track P.

Routine 45: Nonreturn to Zero I Correction Test.

Error Codes:

- 45 00 Error track register and correction circuit functions normally.
- 45 XX Error detected.

General Description:

• This routine is executed in the loop write/read, nonreturn to zero I mode. One track is masked and a data pattern (all "1's") is sent to the error track register (register for error correction). The masked track is then shifted from track 0 to P.

Routine 46: Format Control Circuit.

Error Codes:

- 46 00 Hardware counters that check the block format and format error detection circuit function normally.
- 46 XX Error detected.

General Description:

- (1) Noise check (NOISC) signal. This test checks each bit for early-begin read-back errors. Using the loop write/read FMT function, the noise check signal is sent via detection of beginning of block signal. The timing is -20% of the time for read/write head gap length after onset of write. All tracks are masked for 80% of the read/write head gap length for onset of write.
- (2) Slip check signal. This test checks each bit for slow-begin read-back errors. This test is similar to the NOISC test except for timing. In this test, -20 % is replaced by +7% of read/write head gap length.
- (3) Start read signal. Checks bits for preamble. All tracks written with all "1's" in the loop write/read mode. The routine confirms that the start-read check signal is set within fixed time.
- (4) End data check signal. Checks bits for postamble length error. When the postamble is detected in loop write/read mode, the write pattern is changed to all "1's". Writing continues while the routine confirms that the end data check signal is set within fixed time.

Routine 50: Reel Servo Test (Tape Turning Test).

Conditions:

- A work tape should be used for this test.
- This routine does not read or write the tape.
- After completion of test, the other command operations are not affected.

Error Codes:

- 50 00 Reel motor operation is confirmed.
- 50 1X Error detected during forward test.
- 50 2X Error detected during backward test.
- 50 XX Error detected.

Routine 50: Reel Servo Test (Tape Turning Test). (continued) General Description:

- Tape runs forward/backward for a few seconds.
- Test with time delay and with tape running.
- Test without time delay and with tape running.
- Tests are applied with the following order:
 - (1) Run forward without stops 3 s
 - (2) Pause 100 ms
 - (3) Run backward without stops 2 s
 - (4) Pause 100 ms
 - (5) Run forward without stops 1 s

Routine 51: Reel Servo Margin Test.

Conditions:

- A work tape should be used for this test.
- This routine does not read or write the tape.
- After test is completed, the other command operations are not affected.

Error Codes:

51 00 The reel and reel servo both function without error when subjected to servo-control worst-case conditions.

51 XX Error detected.

General Description:

Run time, pause time, and reel motion reverses are executed so that load is the maximum at reel motion, and forward turn/backward turn are performed.

Details:

Each test is done 10 times in the following order:

Speed	125	ips	75 i	ps	50 i	ps
Item	Go up	Go Down	Go up	Go down	Go up	Go down
	time	time	time	time	time	time
	(ms)	(ms)	(ms)	(ms)	(ms)	(ms)
1 Forward run 2 Forward run 3 FWD/BWD run 4 FWD/BWD run 5 Backward run 6 Backward run	80	80	50	50	20	20
	160	160	100	100	40	40
	160	160	100	100	40	40
	320	320	200	200	80	80
	160	160	100	100	40	40
	80	80	50	50	20	20

Routine 52: Capstan Simple Running Test.

Conditions:

- A work tape longer than 50 meters is used for this test.
- Data contained on the tape must be in continuous, normal format.

Error Codes:

- 52 00 The capstan motor functions normally without error.
- 52 XX Errors are detected when tach pulse, gap control, gap control signal, running direction, and running speed are checked.

General Description:

The tape runs forward for about 30 m at a constant speed, the tape then runs backward about 30 m at a constant speed.

Details:

The following items are checked for both forward/backward runs.

- GAPC signal is on.
- Handler action signal is on.
- Tach A signal is on.
- Tape speed is constant.
- Running direction is checked via the MTU handler backward signal and capstan forward signal of FMT.
- Tape unit check indication is not asserted.

Routine 53: Write Current On Test.

Conditions:

- A work tape must be used because write current is sent to the write head.
- A tape having continuous scratches must be used.

Error Codes:

- 53 00 When current flows in the write amplifier, write current/erase current are normal and data is detected from the read head.
- 53 XX An error is detected.

- During writing in the phase encode mode, write current and erase current are normal. When all the tracks are written at 3200 FCI, the test checks whether the read signal of all the tracks is detected within about 15 m from beginning of tape.
- When tape error (Error Code 05) is displayed, the tape must be changed to another tape, and the test must be repeated.
- The Error Code 05 is normal because the tape itself has an error (this proves the error can be detected during write attempts). Next the tape is changed to a good tape to prove that there is no error in the hardware.

Routine 54: Autocleaner Test.

Conditions:

• A work tape with gaps between the data is used for this routine.

Error Codes:

54 00 The autocleaner functions properly.

54 XX Error detected.

General Description:

All "1's" are written on Track 8 (about 4 inches) around beginning of tape in phase encode mode. The autocleaner is activated. Track 8 is read after rewinding the tape, and the data on at least 0.9 cm of tape is checked. This check is repeated five times.

Routine 55: Capstan Servo Margin Test (1600 rpi Write Test)

Conditions:

- A full reel of good quality work tape is used. Data must contain gaps due to data write functions.
- Routine 5 should be followed by Routine 56.

Error Codes:

55 00 No errors detected.

55 XX An error is detected.

General Description:

- Five combinations of start/stop time are executed so that the load is the maximum at the capstan servo. Slippage and speed change are also checked.
- All "1's" are written on all the tracks at 3200 fci. Inter-block gap (IBG) length is 0.6 inches. Postamble and preamble are not written.

Details:

- Go tag signal is on. After the gap control signal is set, this test checks whether tape speed is steady at the start of writing in 0.6-inch IBG mode. If the tape speed is not constant, Velocity Retry Operation is executed. Errors are detected at Retry Out and excessive retries.
- The intervals between start of writing and detection of read data are checked. Slippage is also checked.
- Start/stop time and the number of blocks written are shown below.

The blocks are written in the following order:

T.L	Write block length	50 ips Go down			ips Go down	125	Go down
Item	(bit cell)	Blocks	time (ms)	Blocks	time (ms)	Blocks	time (ms)
1	300	64	10	128	6	256	4
2	1100	64	10	128	6	256	4
3	4300	64	10	128	6	256	4
4	17100	64	10	128	6	256	4
5	25500	32	10	32	6	32	4

Routine 56: Capstan Servo Margin Test (1600 rpi and Backward Read)

Conditions:

• After completion of Routine 55, this routine should be issued without changing tape position so that all the blocks written at Routine 55 are used.

Error Codes:

56 00 No errors detected.

56 XX Error detected.

- Go down time of the blocks written during routine 55 is set to 10 ms at 50 ips, 6 ms at 75 ips, and 4 ms at 125 ips. When backward read is normal at all the blocks, forward read is then executed.
- While data is being detected, this routine checks whether tape speed is within <u>+</u> 7% of the normal speed. During 29 tach pulses after detection of IBG, the "crease tape check" is executed.

Routine 57: Capstan Servo Margin Test (6250 RPI and Write)

Conditions:

A full reel of good quality work tape should be used. Data will contain gaps due to the nature of the test.

Error Codes:

57 00 No errors detected.

57 XX Error is detected.

General Description:

MTU is in 6250 rpi mode and SAGC count is set to step 6. Read slice level is the same as that of normal write. At 9042 fci, all the tracks are written, but formatting is not done. IBG length is 0.3 inches. The same procedure as that for Routine 55 is followed, and capstan slippage and speed change are checked.

Details:

- At the start of writing, this test checks whether the tape speed is constant. If tape speed is not constant, Velocity Retry Operation is executed. In case of retry out and excessive retry times, an error is detected.
- Start/stop times are shown below. Tests are applied in the following order:

Item	Write block length (bit cell)		ips Go down time (ms)		ips Go down time (ms)	Blocks	ips Go down time (ms)
1 2 3 4 5	600 2200 8600 34200 51000	64 64 64 64 32	5 5 5 5 5	128 128 128 128 32	4 4 4 4	256 256 256 256 256 32	3 3 3 3 3

Routine 58: Capstan Servo Margin Test (6250 rpi Forward and Backward Test)

Conditions:

• This routine should be run after Routine 57. This routine is executed without changing tape position so that all the blocks written in Routine 57 are used.

Error Codes:

58 00 No errors detected.

58 XX Error detected.

General Description:

- Go down time of the blocks written in Routine 57 is set to 5 ms at 50 ips, 4 ms at 75 ips, and 3 ms at 125 ips. When backward read is normal at all the blocks, forward read is then be executed.
- While data is being detected, this routine checks whether tape speed is within <u>+</u> 7%. During 10 tach pulses after detection of IBG, "crease tape check" is executed.

Routine 60: Erase Test.

Conditions:

• A good quality work tape should be used.

Error Codes:

60 00 No errors detected.

60 XX Error detected.

General Description:

The tape is rewound, and after running forward 10 inches from beginning of tape, all "1's" are written on all the tracks for 10 inches at 1700 rpi. After 8.6 inches of back space, the MTU is placed in the erase mode. While 8.6 inches are erased, data is read at a slice level of 7%. If data is not detected, the effects of erasing are checked.

Routine 61: Self Amplitude Gain Control Circuit Test

Conditions:

- Work tape should be used.
- There should be no scratches longer than 15 cm on the tape within 15 m from the beginning of tape marker.

Error Codes:

- 61 00 No errors detected.
- 61 Error detected on the tape. The tape should be changed and tests repeated.
- 61 XX Error detected.

General Description:

- The tape is rewound, and the MTU is set to the 6250 rpi mode.
 The SAGC count of step 6 and the read slice level of 51% is confirmed.
- After spacing 10 inches from beginning of tape and writing on all the tracks at 9042 fci, the test program searches for a place where the time sense signals of all tracks are on. If not found within 150 mm, writing is stopped and the tape is backspaced 150 mm. At this position, the test is applied to SAGC circuit.

Details:

Tests are run with the following sequence:

- (1) All "1's" are written on all the tracks and SAGC operation is executed in the MTU. The routine then confirms that SAGC check error is not set.
- (2) The head is returned to the place specified in the general description. Using the forward read, the SAGC operation is executed in MTU. The routine confirms that SAGC check has not been set.
- (3) While tracks are masked and bits 7, 6, 5, 4, 3, 2, 1, 0, 8, are written at every track, SAGC operation is executed. The routine confirms that SAGC check error has not been set.
- (4) During writing on all the tracks masked, SAGC operation is executed. SAGC check error and step 12 of SAGC count is confirmed.
- (5) After SAGC check is found at step 12, the block write is executed. The gain step down operation is checked by the SAGC count, decreasing to step 11.

Routine 62: Group Coded Recording Normal Write Test

Conditions:

• A work tape should be used for this test.

Error Codes:

- 62 00 No errors detected.
- 62 22 Tape error. After changing the tape, repeat the test.
- 62 XX Errors detected.

General Description:

- The SAGC is checked in a manner similar to Routine 61. After setting a SAGC count suitable for the tape, the tape will be verified. When an area of good quality is selected, 10 blocks are written.
- Write data is random data. Block length is 55 bytes during online diagnostics (or Routine 00 of offline diagnostics), and 4 k bytes during offline diagnostics.

Details:

(1) Verification of the tape.

All "1's" are written at normal slice level. Tape is advanced 20 inches until time sense signals of all the tracks are on. A tape error is detected when a good area of 20 inches cannot be found within 60 m.

- (2) Write data.
 - Random write data is generated by the microprogram. Write data is written in the transfer buffer byte-by-byte until the buffer is full.
 - Using the forward read, the SAGC operation is executed in MTU. The routine confirms that SAGC check has not been set.
 - After the start of writing data, the data is read from the transfer buffer. The data is fed to the controller interface bi-directional data bus as well as to the write modulation circuit.
 - During that time, the accepting data (RECV) signal is reset, and data is looped from driver to receiver and is written in the transfer buffer again.
- (3) Read-after-write check.
 - This check also verifies whether or not "data check" is detected by the error-detection circuit.

Routine 63: Phase Encode Normal Write Test

Conditions:

• A work tape is used for this test.

Error Codes:

- 63 00 No error detected.
- 63 22 Tape error is detected.
- 63 XX Errors detected.

General Description:

- The tape is rewound, and the MTU is set to the 1600 rpi mode.
- At normal slice level, the tape is verified so that no defect area in 40 inches of tape is found. Ten data blocks are written in the no-defect area, and no "check data" should be detected.
- Creating the data and block length is the same as in Routine 62.

Routine 65: Slice Margin and Read Level Test

Error Codes:

- 65 00 No errors detected.
- 65 10 Tape error is detected.
- 65 XX Errors detected.

General Description:

The read slice level is changed 10%, 15%, 41%, 51%, and 64%. The routine then checks that the time sense signal of all tracks is on for 256 tach pulse lengths at each slice level. This routine checks read amplifier gain adjustment and head wear.

Routine 66: Inter-Block Gap Length Test

Error Codes:

- 66 00 No errors detected.
- 66 XX Error is detected during the IBG length check.

General Description:

This routine writes ten blocks in phase encode and group coded recording modes and measures IBG length by counting tach pulses while continuous backward running for the ten blocks. The blocks are 256 tach pulses in length. The generated IBG in this routine is not normal IBG. Rather, 218 QTP length (0.512 inches) in the phase encode mode, and 116 QTP length (0.275 inches) in the group code recording mode.

Routine 70: Feed-Through Test

Error Codes:

70 00 No errors detected.

70 XX Errors detected.

General Description:

This routine writes 3200 fci data in the phase encode mode and then checks the read signal in low (7%) slice level. The time sense signal should not be detected in any track until the read head reaches actual data. The routine checks for 50-QTP length after the start of write.

Routine 71: Cross-Talk Test

Error Codes:

71 00 No errors detected.

71 XX Errors detected.

- This routine writes all "1's" in the phase encode mode (1600 fci) on tracks 1, 3, 5, 7, and 9, and erases tracks 2, 4, 6, and 8.
- While writing 2.4 inches of tape, the routine reads low slice level and checks the noise level.

Routine 73: Phase Encode Read and Write Test

Error Codes:

- 73 00 The routine is successfully completed with no errors detected.
- 73 XX Error detected.

- The tape is first rewound. After an ID burst in the 1600 rpi mode is written, 25 inches of tape is verified.
- Commands are executed with the following order:

(1)	Write tape mark	10	times
(2)	Write 4k byte	1	time
(3)	Back space file	9	times
(4)	Forward space file	9	times
(5)	Back space	9	times
(6)	Write 4k byte	1	time
	Write 2k byte	1	time
	Write 1k byte	1	time
	Write 512 byte	1	time
	Write 256 byte	1	time
	Write 128 byte	1	time
	Write 64 byte	1	time
	Write 32 byte	1	time
	Write 16 byte	1	time
(7)	Write tape mark	1	time
(8)	Read backward	11	times
(9)	Read forward	10	times
(10)	Back space	5	times
(11)	Space	5	times

- From the above execution of commands, this routine confirms that no unit check (data check and some problem with MTU unit) occurs.
- The basic routine is also confirmed, since each command is executed by the basic routine that is ordinarily used during function operation.
- Write byte is always 55 bytes during online diagnostics or execution of Routine 00.

Routine 74: Group Coded Recording Read and Write Test

Conditions:

• A good quality work tape should be used for this routine.

Error Codes:

- 74 00 The routine is successfully completed with no errors detected.
- 74 XX Error detected.

General Description:

• The tape is first rewound. After an ID burst in the 1600 rpi mode is written, 25 inches of tape is verified.

Routine 75: Nonreturn to Zero I Total Read and Write Test

Conditions:

- A good quality work tape should be used for this routine.
- When this routine is issued to a dual density unit, the diagnostic routine will not be executed and the test will terminate with no error detected.

Error Codes:

- 75 00 Normal end. (Test is by-passed in the dual density unit.)
- 75 XX Error detected.

- The tape is first rewound. After an ID burst in the 1600 rpi mode is written, 25 inches of tape is verified.
- The commands specified in Routine 73 are executed.

Routine 79: Special Routine to Test Ready Status

Conditions:

• This routine is executed when the error code is 99 99 during offline diagnostics.

Error Codes:

- 79 00 No errors are detected at the interface between MTU and FMT as a result of the test by Routine 79. The cause of error code 99 99 is an operator error.
- 79 XX An error is detected at the interface between the FMT and the MTU.

General Description:

This test checks whether the detected error is in the device select circuit of the FMT or in the MTU interface cable. This routine can be executed in MTU not-ready status. No other routines can be executed in MTU not-ready status.

Routine 80: Test Program for Installation Checkout of Azimuth and Capstan Alignmen

Conditions:

- A master skew tape (BM BV MT 351d) or equivalent is used during execution of this routine.
- Do not rewind tapes by hand. Use Routine 96 to return the tape to beginning of tape.
- Error free diagnostic Routines 10 through 59 are a prerequisite for this routine.

Error Codes:

80 00 No error detected.

80 XX Error detected.

General Description:

- Mode: TD model is executed in 800 rpi. DD model is executed in 1600 rpi.
- Forward read from beginning of tape.
- If no errors are detected, the routine stops at beginning of tape.
- If no errors are detected, the routine unloads.
- If errors are detected, the tape stops at the error position. Start this routine again after azimuth alignment is complete.
- Skew marginal function signals (TM 0-3) of FMT 800 rpi read printed circuit assembly (1A01 in the FMT) are changed by the microprogram so that quantity of skew in read data is measured.

Routine 80: Test Program for Installation Checkout of Azimuth and Capstan Alignment. (continued)

- On master skew tape, all "2's" are written at 800 rpi. Width of sampling the differentiated pulse is changed from 50% of the intervals to 13%. This routine confirms that the read pulses in all the tracks are correct in the specified area (at least 200 bit/cell).
- If the quantity of skew is within 13% of the intervals, the test is terminated with no errors detected. If quantity of skew is more than 13%, the error code shows the percentage where the error appears.
- When the percentage of intervals is from 50% to 21% in backward mode, and skew is not within 21%, errors detected are due to incorrect capstan alignment.

Routine 83: Checkout Program for Conversion of Read Amplifier

Conditions:

- A good quality master tape (SRM 3200 or equivalent) is used.
- The test is executed only after cleaning the head and tape path.
- Error-free diagnostic routines 10 through 59 are a prerequisite for this routine.

Error Codes:

- 83 00 No error detected.
- 83 XX Error detected.

General Description:

- All "1's" are written from beginning of tape in 3200 fci. The MTU read slice level is set to 64%. The routine then checks that the time sense signal of all the tracks of 10 inches is on and that the slice level is set to 125%. This program checks that the time sense signal of all the tracks of 10 inches is off.
- The MTU is set to the group coded recording mode and SAGC count is set to step 6. All "1's" are written by 9042 fci and the slice level is set to 41%. This routine then checks whether time sense signal of all the tracks of at least 10 inches is on.

Routine 90: Tape Retention Action

Conditions:

• The tape to be rewound is mounted and is set to ready.

Error Codes:

- 90 00 Tape retention action is ordered to MTU. MTU starts this action.
- 90 XX Though tape retention action is ordered to MTU, it is not executed or errors are detected before execution.

General Description:

When tape retention action is ordered by the FMT, a ready signal goes off (online signal is still on). At the stop position, autocleaner will start and space to end of tape in 200 ips. At the end of tape, the tape automatically rewinds. When beginning of tape is detected after rewinding, ready signal will be "1." The tape retention action is ordered by the FMT. When MTU goes into the ready status, busy signal will go off and the set diagnose commands end as soon as MTU ends this action, the SSC signal will be on.

Routine 91: Data Security Erase Rewind Utility

Conditions:

 This routine completely erases the tape from beginning of tape to end of tape.

Error Codes:

- 91 00 No errors detected.
- 91 01 Error detected.

General Description:

First, the tape is rewound, and the DSE command is then issued from the MTU. Detecting end of tape, the unit rewinds the tape. While this routine is executed, the FMT is busy until completion of the MTU operation.

Routine 92: Read Check to Tape Mark.

Conditions:

- This routine can be used only during offline diagnostics.
- In dual density units, a tape written in 800 rpi should not be used.

Error Codes:

00 00 No errors detected.

XX YY YY (decimal) data checks were detected.

General Description:

This routine reads the tape during offline diagnostics and counts the number of data checks. The routine proceeds from the stop position to detect one tape mark block. The data check count is saved in register Y0/Y1. Register Y0 contains the upper bytes.

Routine 93: Group Coded Recording Write Running Utility.

Conditions:

• The tape used is a work tape. This routine can be used only during offline diagnostics.

Error Codes:

00 No errors detected.

XX YY YY (decimal) data checks were detected.

General Description:

The tape is rewound to beginning of tape, and 4k byte blocks are written to end of tape in the 6250 rpi mode. When a write error is detected, backspace is done automatically. Write is done after erase. The routine stops at detection of end of tape. Upper bytes of error count are saved in register Y0. Lower bytes are saved in register Y1.

Routine 94: Phase Encode Write Running Utility

Conditions and Description:

• Function is the same as Routine 93, except for writing in 1600 rpi.

Routine 95: Nonreturn to Zero I Write Running Utility

Conditions and Description:

 This routine cannot be used with a dual density unit. Function is similar to that of routine 93, except that writing is in 800 rpi.

Routine 96: Back Space to Beginning of Tape

Conditions:

• This routine returns the tape to beginning of tape. A master skew tape should not be used.

Error Codes:

96 00 No errors detected.

96 XX Error detected.

General Description:

The tape is returned to beginning of tape from the stop position at a constant speed. During execution, FMT is busy.

Routine 97: Space to End of Tape Utility

Conditions:

• When tests near the end of tape are necessary the tape can be advanced to end of tape by using this utility.

Error Codes:

97 00 The tape stops at the end of tape.

97 01 Manual interruption during execution is detected.

97 XX An error is detected during execution of this routine.

General Description:

The tape is advanced to the end of tape from the stop position. The tape stops at the end of tape. FMT is busy until completion of this execution.

This section is intended to be used when a problem occurs during operation and a reject code is sent from the formatter (FMT) to the host/controller. The user can then refer to the reject code table, that reference the associated troubleshooting flow chart. Because the error could result from an operator mistake or a problem in the MTU, the user should evaluate the quickest method to correct the problem. All PCAs described in this section are located in the FMT unless otherwise noted.

D0000 TROUBLESHOOTING ACCORDING TO REJECT CODE

If REJECT signal is asserted, the reject code is provided in error multiplex byte 2, bit 0 through 7.

Table D-1. Reject codes

Octal	Description	Nickname	Cause of error	MAP No.
001	Addressed MTU is online and in a not ready status.	IRQ	Operator error	D0020
101	Addressed MTU is selected by another formatter.	USED		
002*	Parity error is detected in microprogram.	CSPE	Hardware error	D0030 D1011
102*	Parity error is detected in microprogram register.	REGE	Hardware error	D1012
202	Abnormality of ALU circuit is detected.		Hardware error	Run offline diagnostics from the FMT
302	Abnormality is detected in part of formatter hardware during power-on diagnostics, test formatter operation, or patrol diagnostics.	DIAGE	Hardware error	?
003*	Timeout of TRAK response to first TREQ (more than 75 msec.) occurred on WRT or LWR command.	WCZ	Hardware error	Run offline diagnostics from the FMT
004*	FMT cannot analyze cause of microprogram trap.	UEX TRAP	Hardware error	Run offline diagnostics from the FMT
104*	Unexpected trap on MTU interface occurred.	UEX DV TRAP	Hardware error/ Operator error	Run offline diagnostics from the FMT
005	Addressed MTU is in file protect status when WRT, WIM or ERS command attempted.	FP	Operator error	Install new tape, or over-write/ erase data. Remove write protect ring or switch write protect off.

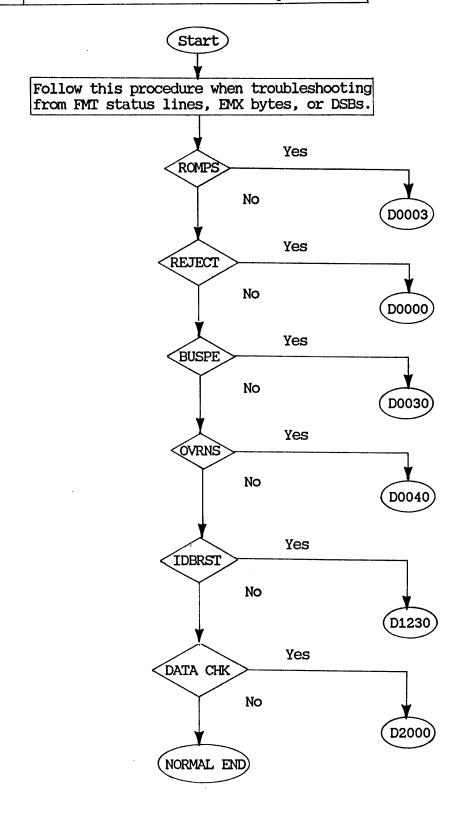
Octal	Description	Nickname	Cause of error	MAP No.
006*	Addressed MTU did not go to erase status only.	set ERS	Hardware error	D1410
106*	Addressed MTU could not be set to low slice level.	Set LOWSL	Hardware error	D1420
206*	Addressed MTU could not be reset from low slice level.	Reset LOWSL	Hardware error	D1420
007	Addressed MTU is not in write status when DSE command attempted.	DSE RJC	Operator error	Install new tape, or overwrite/ erase data. Remove write- protect ring, or switch write protect off.
107	Requested command is invalid.	Invalid Code	Operator error	Review/retry command.
207	Condition of MTU does not match requested diagnostic operation.	DIAG NCAP	Operator error	MTU error code? Ready light ON?
010*	Addressed MTU did not go to read status.	Set RDS	Hardware error	D1410
110*	Addressed MTU did not go to high speed mode.	Set HSP	Hardware error	D1420
210*	Addressed MTU did not go to normal speed mode.	Set NSP	Hardware error	D1410
011*	Tape subsystem does not have NRZI capability and no ID burst detected.	NCAP NRZ	Operator error/ Hardware error	D0070
111*	MTU does not have GCR capability and attempted to read GCR tape.	NCAP GCR	Operator error	D0070
211*	Command operation is attempted in tape speed which does not meet capability of VFO circuit.	VFO Not Capable	Installa- tion error	D0070

0cta1	Description	Nickname	Cause of error	MAP No.
012*	Addressed MTU did not assert gap control signal.	GAPC Error	MTU hard— ware error	D1320
112*	After starting command, tape speed did not reach acceptable limits within specified length.	Velocity check	MTU hardware error	D1330
013	Addressed MTU is not in online status.	Busy	Operator error	
113	Addressed MTU is not operational.	Not install	Operator error	D0020
213	Corresponding enable switch to MTU is set to disable.	Disable	Operator error	D0020
014*	Addressed MTU did not go to write status after WRT, WIM, or ERS command issued.	Set WRS error	MTU hardware error	D1410
114*	LWR TUIF mode of MTU could not be set.	Set LWR error	MTU hard- ware error	D1410
214*	LWR TUIF mode of the MTU could not be reset.	Reset LWR	MTU hard— ware error	D1410
015*	Reserved.			
115*	During backward motion after detecting ARA-ID, BOT was not reached in expected distance.	ARAID BRD error	Tape	D1240
215*	During forward motion in a diagnostic mode, EOT was detected.	DIAG EOT	Operator error	
016*	Addressed MTU did not go to backward status.	Set BWD error	MTU hard- ware error	D1410
116*	Instructed disconnect FSF operation was not initiated by MTU.	Set FSF error	MTU hardware error	D1420
216*	Instructed disconnect BSF operation was not initiated by MTU.	Set BSF error	MTU hardware error	D1420

0cta1	Description	Nickname	Cause of error	MAPNo.
316*	Tape mark cannot be detected correctly.	SKIPF error	Operator error	D1465
017*	Noise (possible data) was detected during an erase operation of an ERS or WIM command.	NOIS IN ERS	Tape hardware error	D2100
020	Reserved.			
021*	Ready status of MTU was reset bu TUC *2.	TUCK	Operator error/MIU hardware error	Retry/run offline diagnostics
121*	Ready status of MTU was reset by reset key.	RST KY	Operator error	D1300
221	TAG IN response by MTU was not detected within specified limit.	TAG IN check	Hardware error	D1440
022*	PE or GCR ID burst was not written correctly.	IDB WRT error	Tape error /hardware error	D1230
023	Backward type command (except RWD or UNL command) was issued when tape was positioned at beginning of tape.	BWD BOT	Operator error	Retry/run offline diagnostics.
024*	In ARA burst (just read), specified signal pattern was not detected and SAGC check was not reported by MTU.	SAGC circuit error	MTU hardware error	D1260
124*	During SAGC operation, gain adjustment of read amplifier was not performed within specified limit.	SAGC check	Tape error	D1260
025*	IBG longer than 20 m was detected on RD, FSP, or FSF command.	20 m check	Operator error/ Hardware error	D0060

Octa1	Description	Nickname	Cause of error	MAPNo.
125*	Error during read or write operation was detected.	R/W OVRN	Operator error Hardware error	D1450
026*	LWRRW mode of MTU could not be set.	Set LWR2 error	Hardware error	D1420
126*	LWRRW mode of TMU could not be reset.	Reset LWR2 error	Hardware error	D1420
226*	An error was detected in data of the MTU communication register.	Communi- cation register error	Hardware error	D1420
027*	Instructed rewind operation was not initiated by MTU.	Set REW error	Hardware error	D1430
127*	Instructed unload operation was not initiated by MTU.	Set UNL error	Hardware error	D1430
227*	Instructed DSE operation was not initiated by MTU.	Set DSE error	Hardware error	D1430
327*	TUC or TUINT in MTU could not be reset.	Reset TU	Hardware error	D1410
030*	Instructed density could not be set.	Mode set error	Hardware error	D1410
031*	MTU was in high speed mode and in NRZI mode.	WCARM	Hardware error	Run offline diagnostics
131*	Write circuit alarm of MTU was detected during positioning operation.	WCARM	Hardware error	Run offline diagnostics
032*	After tape motion was started, tach pulse not detected within specified limit.	Tach start failure	Hardware error	D1320
132*	During tape motion, the tach pulse was not detected within the specified limit.	Tach stop failure	Hardware error/ Operator error	Run offline diagnostics

Octal.	Description	Nickname	Cause of error	MAPNo.
033*	Reserved.			
133*	Set ERM instruction was not performed.	Set ERM error	Hardware error	D1430
233*	Dynamic reversal error was detected.	DYRV	Hardware error	D1310
034*	No IBG following ID or ARA-ID burst within distance.	IBG not detected	Tape error/ Hardware error	D1255
035*	Addressed MTU attempted to backspace over bad record just written or read but was unable to detect record.	Missing position	Tape error/ Hardware error	D1460
036*	ARA-ID was not written correctly and could not be read back.	ARAID write error	Tape error	D1230
037*	During read back check of WRT command, no data detected.	No block	Tape error/ Hardware error	D1270
137*	On write tape mark command, tape mark was not written correctly with seven retry operations.	WIM retry out	Tape error/ Hardware error	D1220



ı								
	D0002	Error	Multiplex	and	Drive	Sense	Bytes	(DSB)

The formatter status lines are as follows:

(1)	Reject	(REJECT)
(2)	Operation incomplete	(OP-INC)
(3)	ROM parity error	(ROMPS)
(4)	Data bus parity error	(BUPER)
(5)	Overrun status	(OVRN)
(6)	Data check	(DCK)
(7)	ID burst	(ID BRST)
(8)	Corrected error	(CRERR)

Table D-2. Error multiplex bus decode.

MUX byte										
Dycc	P	7	6	5	4	3	2	1	0	Description
0	DTP	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DTO	Dead tracks
1	CRC ERR	WIM	UCE	PART REC	MLT ERR	MISC DATA ERR	END DATA CHK		DIAG MODE	Read/write errors
2	TACH	RJC7	RJC6	RJC5	RJC4	RJC3	RJC2	RJC1	RJC0	Reject code
3	WRTS	EOTS	BOTS	NSPM	PROS	BWDS	HDNS	RDYS	ONLS	Drive sense byte 0
4				Re	eserve	d				
5										
6										
7				Re	eserve	i				

DOOO2 Error Multiplex and DSB

Table D-3. Drive sense bytes.

Bit byte	P	7	6	5	4	3	2	1	0			
DSBO	WRTS	EOTS	BOTS	NSPM	FPS	BWDS	HDNS	RDYS	ONLS			
1	'0'	'1'	'1'	D1	D0	'0'	M2	M1	МО			
2	'0'	'0'	'0'	S1	S0	'o'	'0'	'0'	'0'			
3	'0'	TUC	Reset key	DSE	Test mode		SAG	C count				
4	'0'	HERS	HACT	HBWD	HWCON	H65S	TOVR	H1600	IMD			
5	′0′	MISC error	TLA left	TLA right	ROM parity error	Write circuit alarm	'0'	Air bearing alarm	Load failure			
6	'0'		MTU error code									
7	LWR TUIF	ing File s		High speed mode	Low slice mode	0	Slice 1	level 2	LWR RW			
8	'0'			T	U unique	∋ ID high	n order					
9	101			T	U unique	∋ ID low	order					
10	'0'				FMT fo	unction 1	[D					
11	′0′	IBG detect	Start read check	CRC III check	Early begin read back check	SAGC check/ noise error	Slow begin read back check	Slow end read back check	PCMP			
12	'0'	X-call	800 BPI feature	LWR FMT	Velo- city retry	SKEW	WEC over flow		Write trigger VRC			
13	'0'	27		Write	error (count			20			
14	'0'				FRU1							
15	'0'				FRU2							

D0002 Error Multiplex and DSB

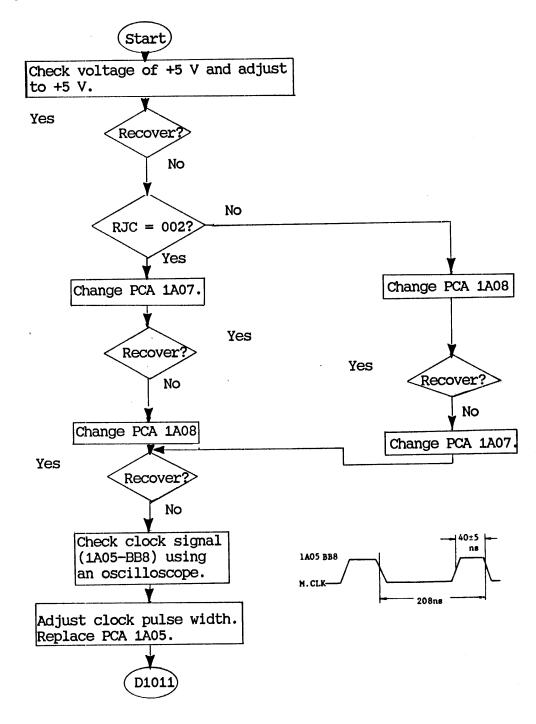
FRU refers to a field replaceble unit. When cyclic redundancy (CRC) error in error multiplex byte 1 is set or PCMP in drive sense byte 11, FRU1 and FRU2 have the following meaning:

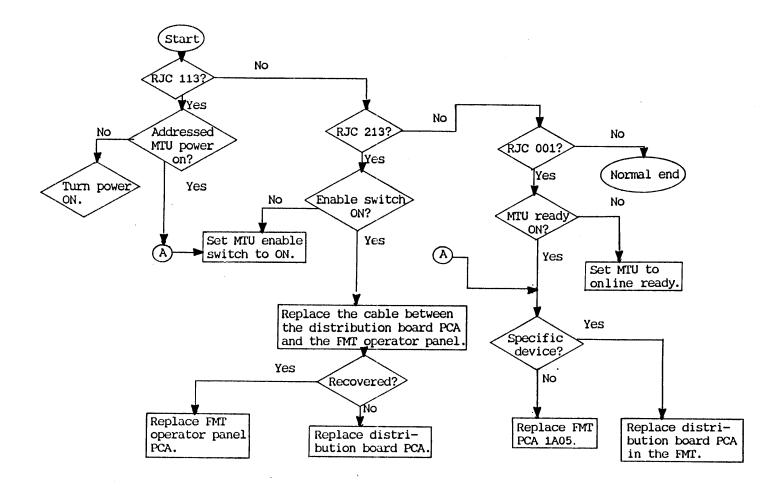
	P	7	6	5	4	3	2 .	1	0
FRU1	'0'	'0'	′0′	′0′	'1'	'0'	AB reg parity C	DB check	Write BOC
FRU2	'0'	Unmatch CRC	Unmatch CRC zoro		B≠D	B≠C	Unmatch CRCC	A≠B	XBIC

D0003 ROM Parity Error

This error signal is asserted when there is an incorrect parity word in microprogram control storage (EPROM), or an incorrect parity byte in local storage register (RAM). When the above error occurs, microprogram traps address "00E0" and loops to waiting START signal.

Reject Code (RJC) Octal (002) EPROM Parity Error Reject Code (RJC) Octal (102) RAM Parity Error





D0030 Data Bus Parity Error - 1

Parity error is detected in transferred data from or to the controller through bi-directional data bus.

(1) Write or loop-write-to-read command:

Data transferred from the controller is checked at the receivers of bi-directional data bus. The check timing is the same as data setting timing to bus out register. If this error occurs, data check will be set. MUX byte 1; bit P, CRC ERROR, and bit 3, MISC DATA ERROR will be set.

(2) Read or read backward command:

Read data transferred from the FMT is checked through receivers at the reading edge of TRAK signal. Generated parity bit is added to the input data to the drivers of bi-directional data bus.

(3) SDIA command:

Diagnostic flag bytes transferred from the controller is checked in the same manner as the write command. It is checked when TREQ and TRAK signals are asserted.

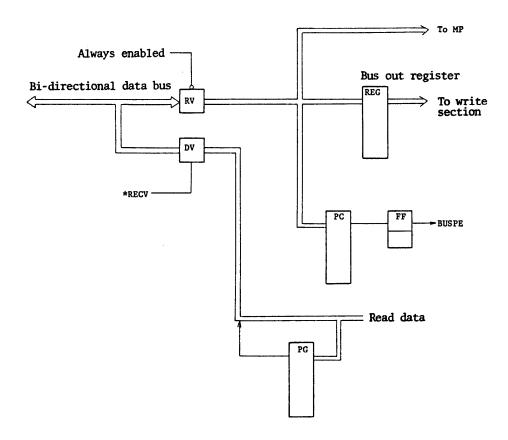
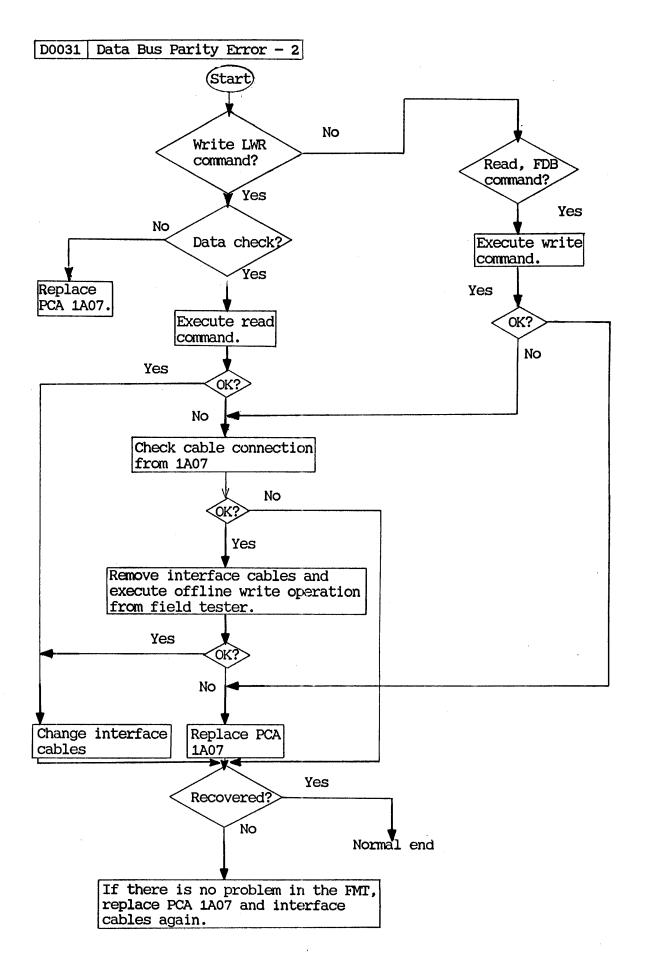


Figure D-1.



Overrun Status

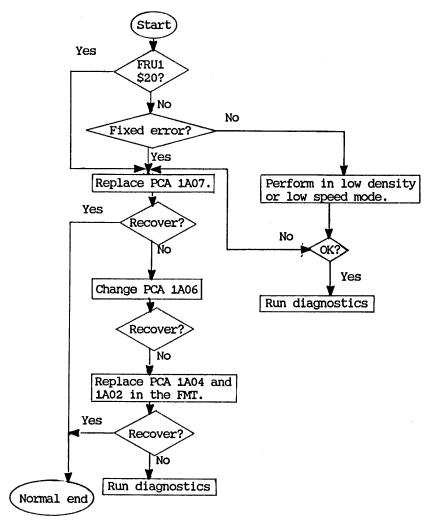
This error is reported when controller has not responded to transfer request within the capability of data transfer buffer.

FRU1 (SB14) \$21 FRU2 (SB15) The content of XCTL register

- (1) In the write or loop-write-read command, this error will be set if the amount of data in the transfer buffer becomes less than 6 bytes (in 6250 RPI mode) or zero byte in 1600/800 RPI mode) before receiving stop signal.
- (2) In the read or read backward command, this error will be set if transfer buffer becomes full during reading data.

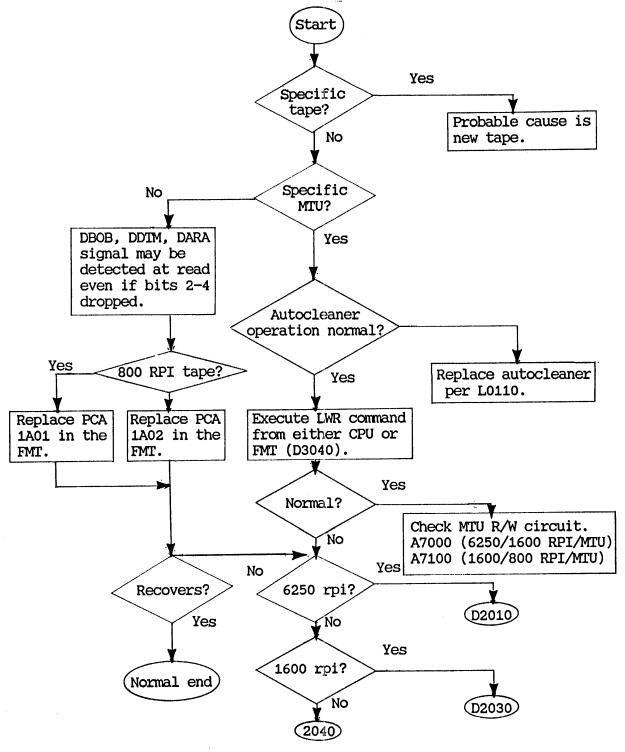
FRU1 (SB14) \$20 FRU2 (SB15) The content of XCTL register

For failure in the data transfer sequence control circuit or the transfer buffer circuit, this error will be set. Transfer buffer does not become empty even after all read or write operations end.



B03P-5280-0341A...02A

This check is generated when any data was not detected for more than 20 m at read command. (BOB, DTM, ARA, or NRZ data byte was not detected.)



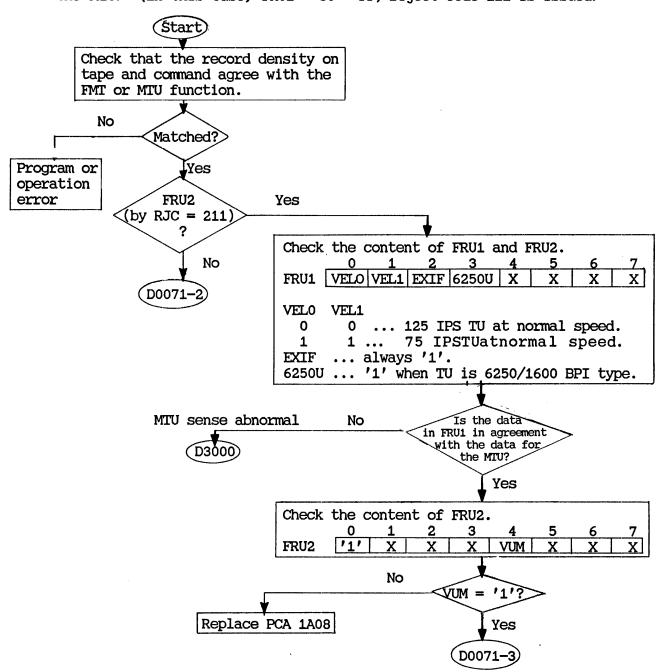
Notes:

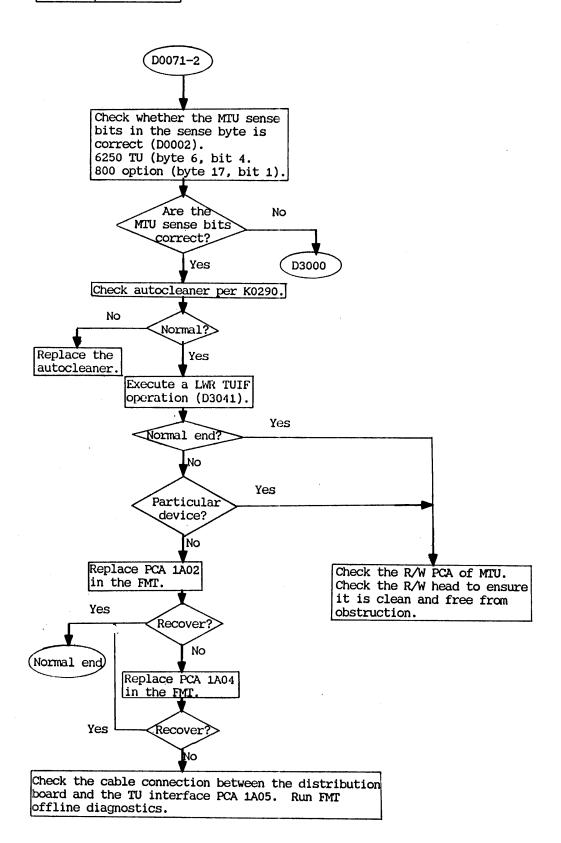
- (1) DBOB = Detection of beginning of block.
- (2) DARA = Detected automatic read amplification.
- (3) DMT = Detected tape mark.

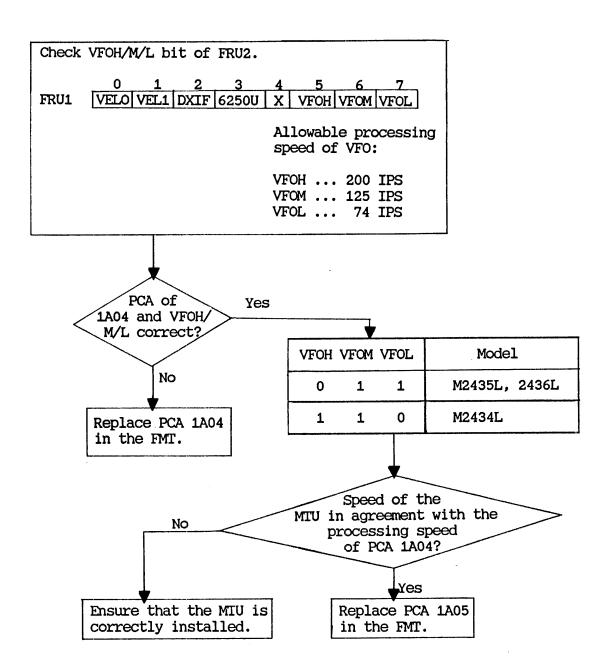
D0070 Not Capable (Reject Code 011, 111, 211)

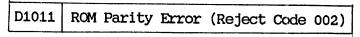
Not capable is generated:

- (1) If an attempt is made to read 800 BPI tape through the FMT or MTU without the 800 BPI feature or function, reject code 011 is issued.
- (2) If an attempt is made to read 6250 BPI tape through the MTU without the 6250 BPI function, reject code 111 is issued.
- (3) If the specification for the maximum possible processing speed of the demodulation circuit is not in agreement with that for the speed of the MTU. (In this case, FRU2 = 80 FF) reject code 211 is issued.











Use ROM scan function with field tester as follows:

- (1) Set ONL/OFL switch to OFL.
- (2) Set switches S0 through S7 to \$F4, then toggle the CNT. The ROM scan function begins.
- (3) Set switches SO through S7 to \$A4, and lamps
 L0 through L11 will be in a half-lit condition
 if a ROM parity error has not occurred. When
 a ROM parity error occurs, microprocessor is
 halted immediately.
- (4) Set switches SO through S7 to \$FO, then toggle the CNT to terminate the ROM scan function. Return the ONL/OFL switch to ONL after all troubleshooting.

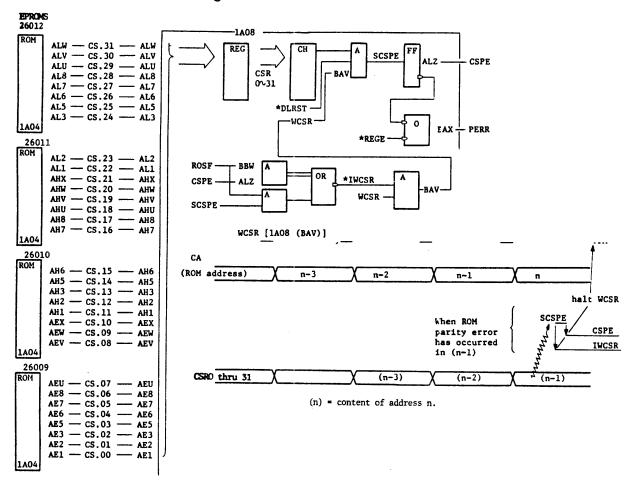
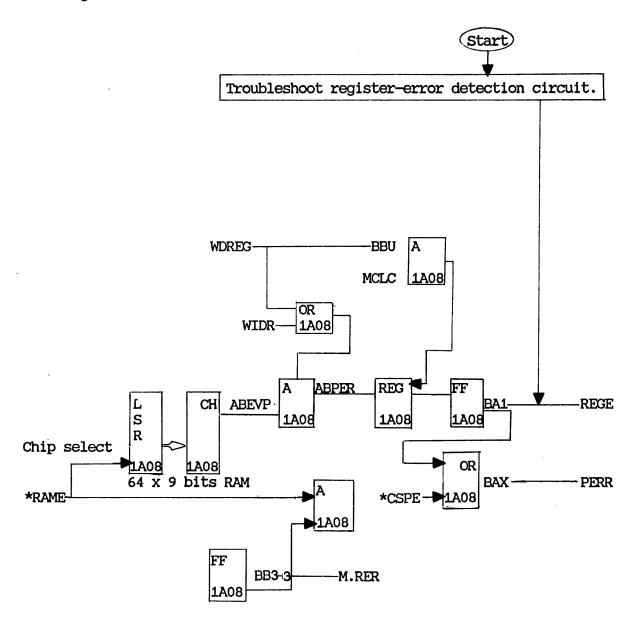


Figure D-2.

D1012 Register Parity Error (Reject Code 102)

When the microprocessor takes the data stored in register LSR (Local Storage Register) at register address 00-3F, the parity is checked if a M.RER signal has been set. If the parity is incorrect (even parity), the REGE signal is set.

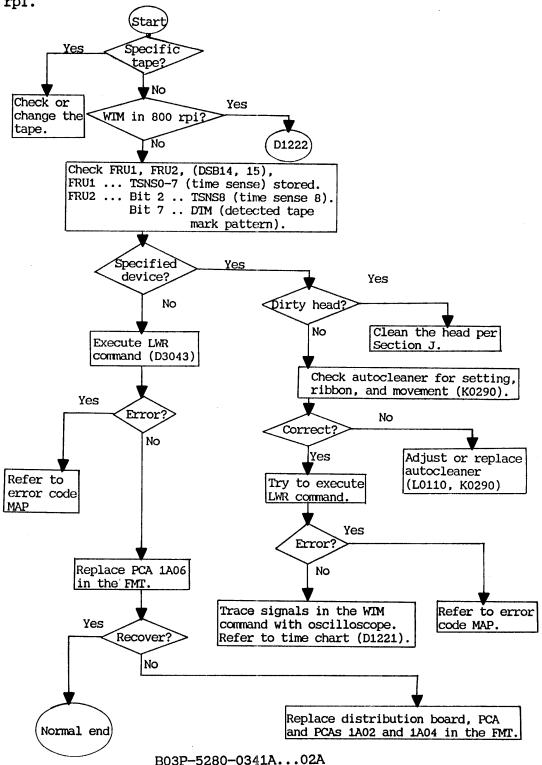


D1220 Write Tape Mark Error - 1

This error occurs when TM (Tape Mark) is written incorrectly as follows:

- (1) When the TM pattern cannot be detected within the specified length from the end of recording the TM block in 6250/1600 rpi operation.
- (2) When IBG cannot be detected within the specified length from the end of the TM block in 6250/1600 rpi operation.
- (3) When the TM code cannot be detected in 800 rpi operation.

The contents of time sense are stored in FRU1 (DSB14) in 6250/1600 rpi.



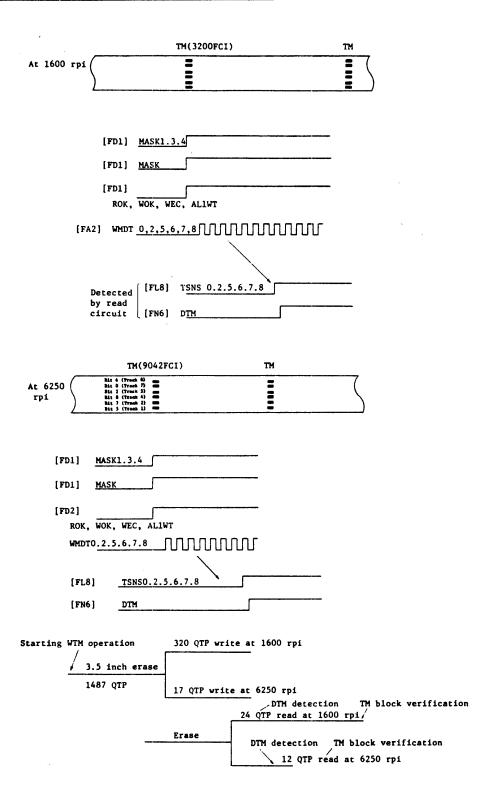


Figure D-3.

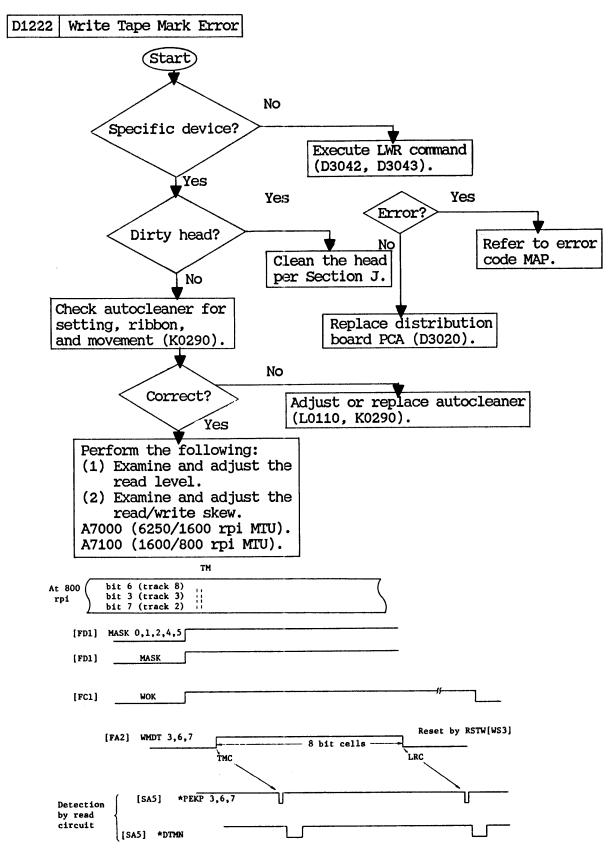


Figure D-4.

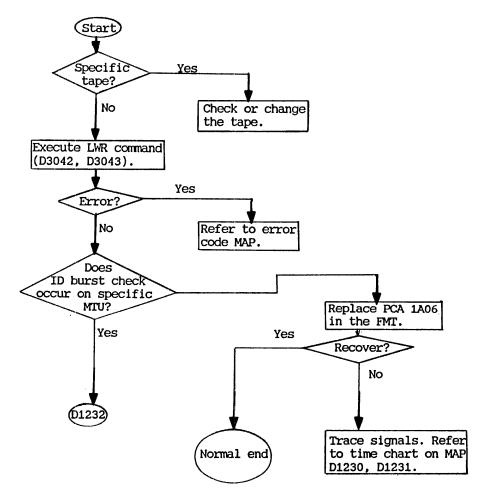
D1230 ID Burst Check

ID burst check is generated when recording density identification (ID), ARA, and IVTM (ARA ID) are written incorrectly, as described below.

(1) ID burst could not be detected.

- (2) ARA burst was written incorrectly (D1260). SAGC check (sense byte 8, bit 4) is set.
- (3) IVIM could not be detected.

The contents of time sense are stored in FRU1 (DSB14) and FRU2 (DSBM15).



D-26

B03P-5280-0341A...02A

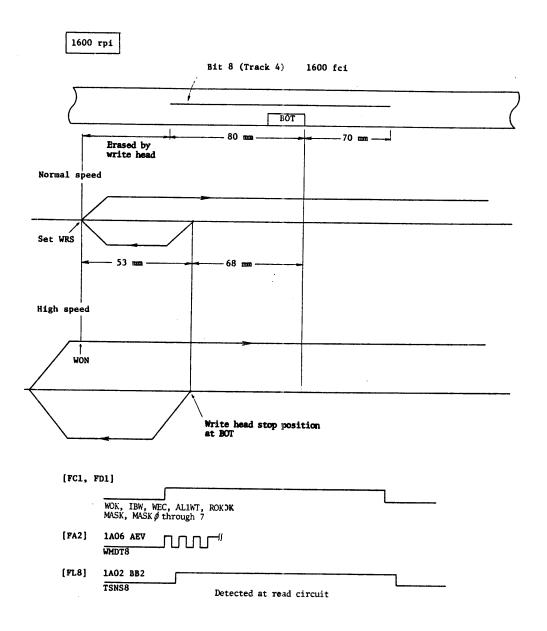
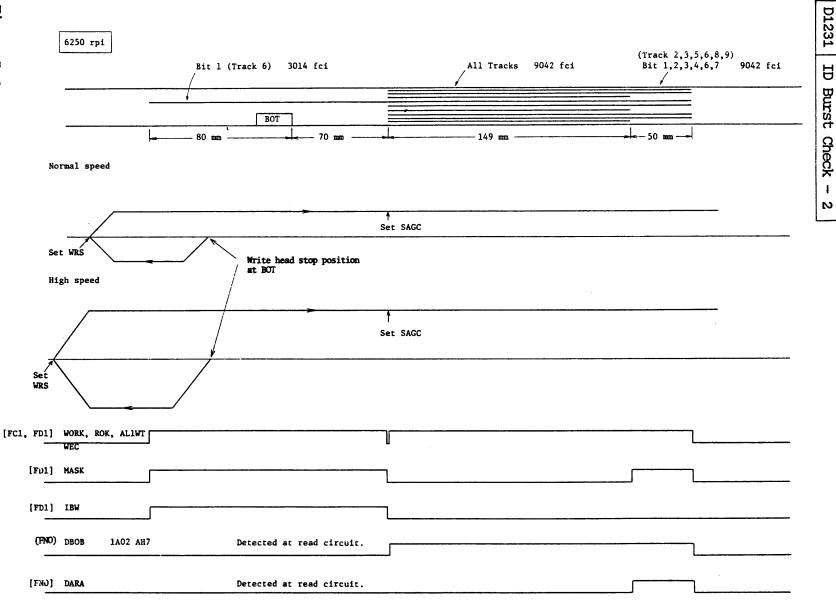
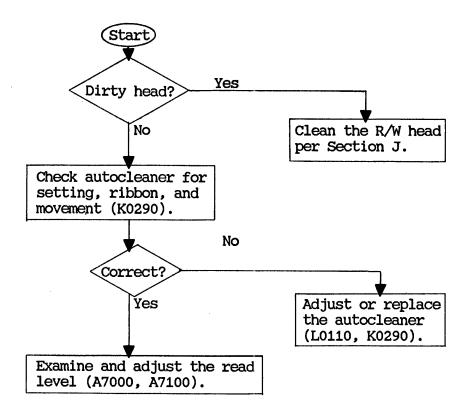


Figure D-5.



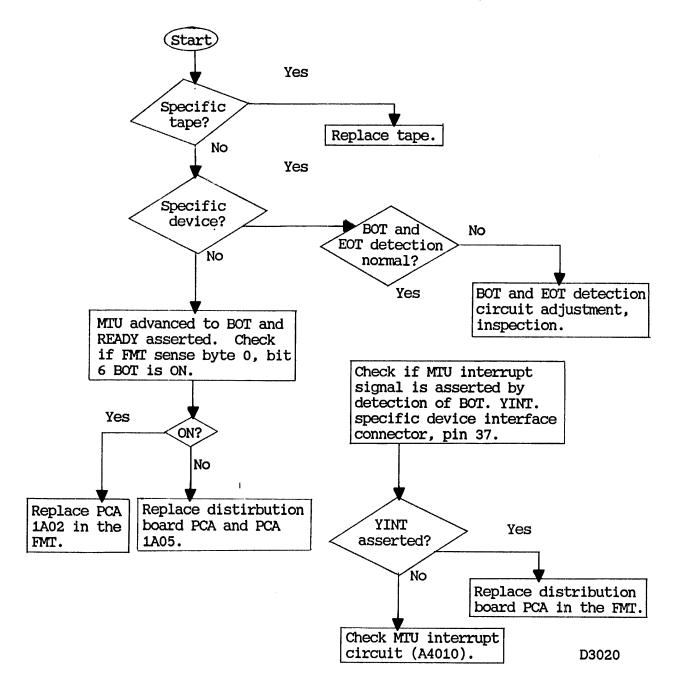
D1232 ID Burst Check - 3



D1240 Reject Code 115

An error will be generated if:

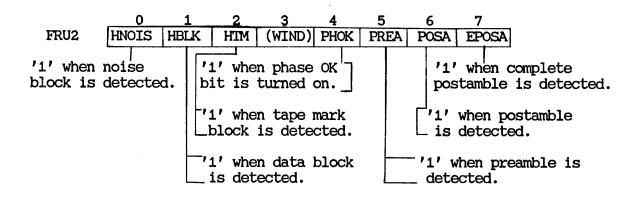
- ARA (automatic read amplification) ID burst (IVTM) was detected, but (BOT) beginning of tape mark was not detected within the prescribed length during 6250 rpi backward operation.
- ARA ID burst code was detected for 28TP (6.7 mm).



D1250 IBG Detected

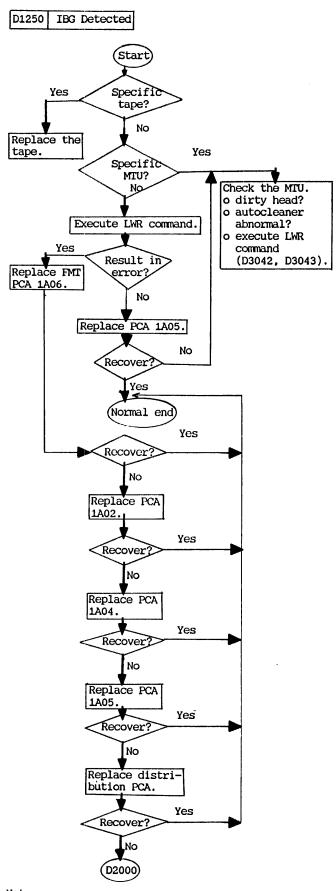
An error will be generated when an inter-block gap (IBG) is detected during write or loop write-to read operation. The data check line bit is asserted in this case. EVC (DSB12, bit 1) may also be set in 6250/1600 rpi write operation. The following FRUs may be indicated on DSB 14, 15.

FRU1 (DSB14) \$A8
FRU2 (DSB15) Content of RDSNS register.



Notes:

(1) FRU = Field replaceable unit.



Notes:

- (1) IBG = Inter-block gap(2) FRU = Field replaceable unit
- All PCAs in this troubleshooting flowchart are in the FMT.

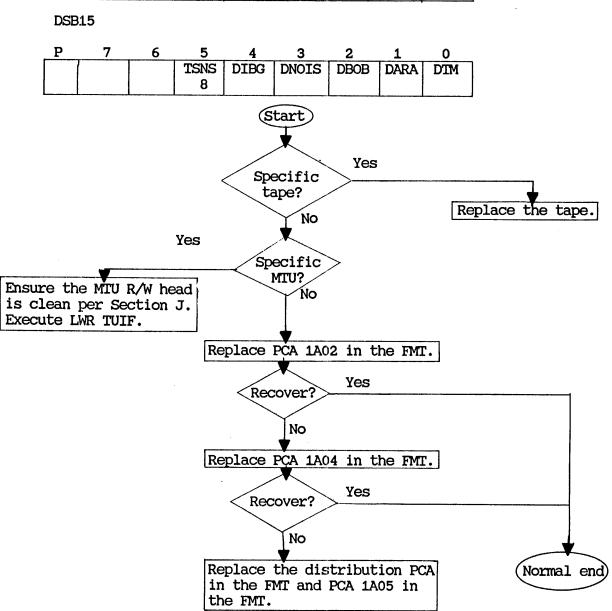
D1255 IBG Not Detected (Reject Code 034)

An error will be generated when:

- (1) Inter-block gap (IBG) is notdetected within 44 cm from the point that automatic read amplification (ARA) burst was recognized in 6250 rpi read operation.
- (2) IBG is not detected within 10 m from the point ID burst wasrecognized in 1600 rpi read operation. Reject and operation incomplete lines are asserted. DSB14 and 15 give time sense information:

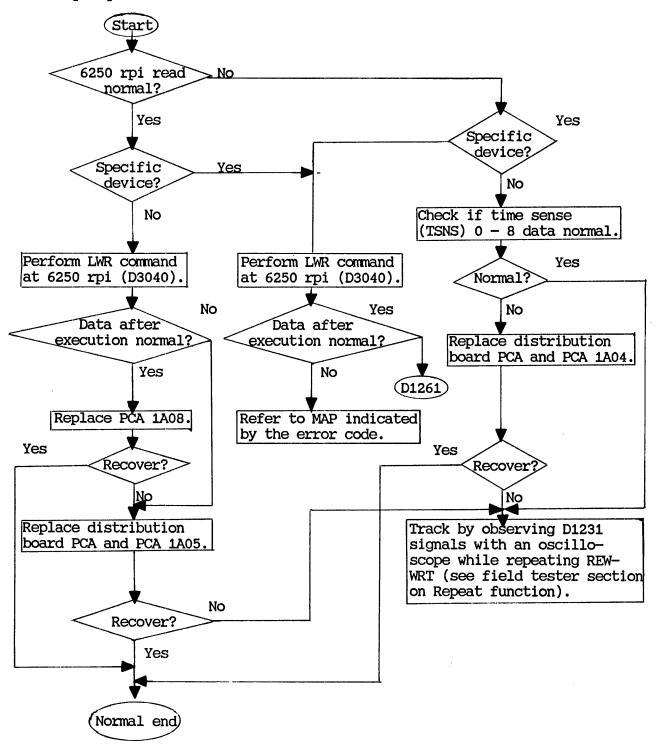
DSB14

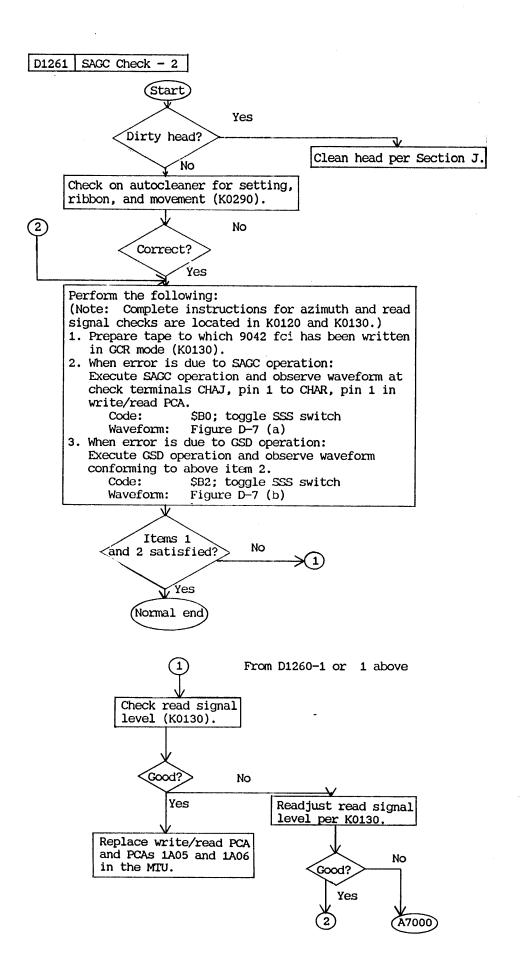
P	7	6	5	4	3	2	1	0
0	TSNS	TSNS	TSNS	TSNS	TSNS	TSNS	TSNS	TSNS
	0	1	2	3	4	5	6	7



D1260 SAGC Check - 1

Self-adjust gain control (SAGC) check is generated when automatic read amplification (ARA) burst read or write was performed incorrectly during 6250 rpi operation.





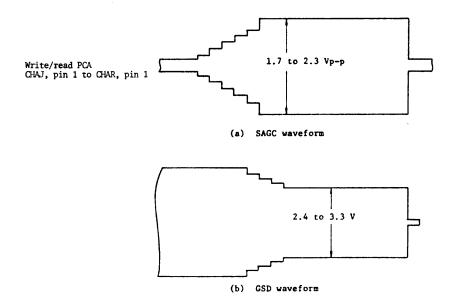


Figure D-7.

D1270 No Block Detected

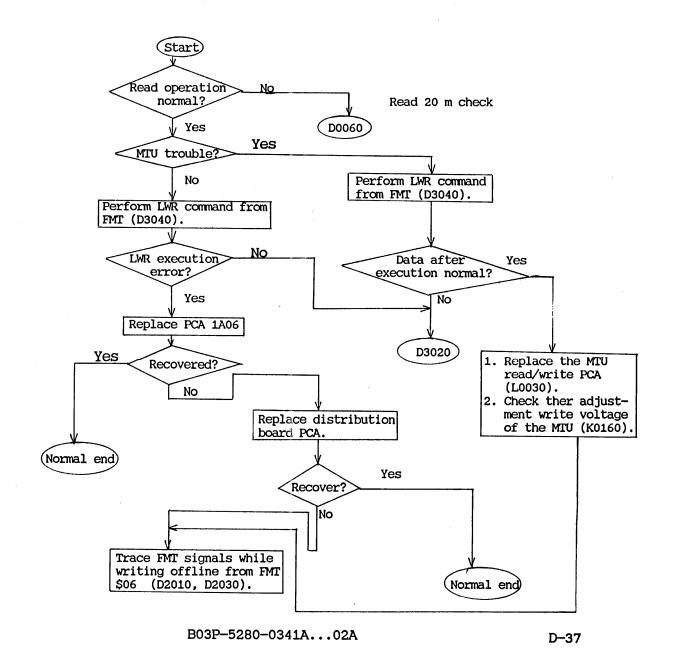
This error is generated when writing is started and data block cannot be detected within the prescribed length after the writing has ended (at write command). (Detected at 70 QTP.)

When DNIS (detection of noise pattern) signal continues as long as 46 bit cells in the 6250 rpi mode or 22 bit cells in the 1600 rpi mode, HNOIS signal is generated.

Detection of data block depends on whether HNOIS signal is generated.

DNOIS detection pattern at 6250/1600 rpi write

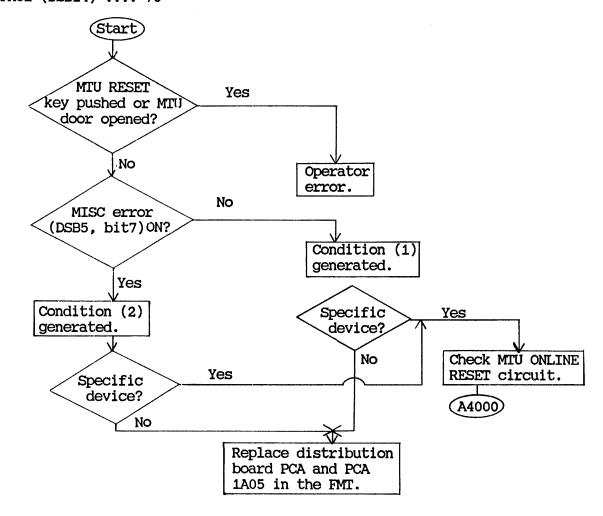
0.4.6+1.2.8+3.5.7+(0+4+6)(1+2+8)(3+5.7)



D1300 Reset Key (Reject Code 121)

This error is generated:

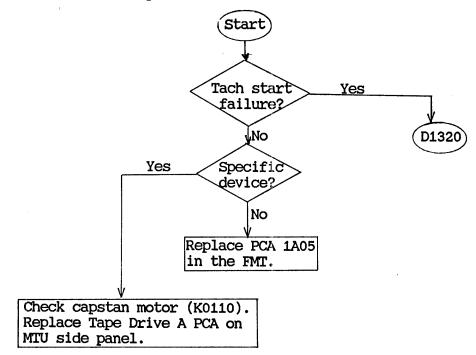
- (1) When MTU RESET key is pushed mistakenly during MTU drive. (DSB3, bit 6, reset key is set.) FRU1 (DSB14) 70
- (2) When MTU door is opened inadvertently during operation. (DSB3, bit 6, reset key and DSB5, bit 7, miscellaneous error set.)
 FRU1 (DSB14) 70



D1310 Reject Code 233

This error is generated when:

- (1) The tape is operated more than the prescribed QTP (quarter tach pulse) number in reverse direction at MTU starting.
 - o FRU1 (sense byte 22) CC
 - o FRU2 (sense byte 23) TQP count number (length of running of drive direction.)
- (2) Error when operated 108TP in reverse direction.



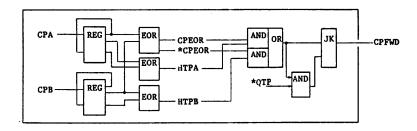


Figure D-8.

D1320 Tach Start Failure - 1 (Reject Code 032, 012)

This error will be generated in the following cases:

(1) Reject code 032

When prescribed QTP length is not detected within the prescribed time after MTU start.

FRU1 (DSB14) 108-QTP count total (drive direction and reverse direction)

FRU2 (DSB15) 20-drive direction QTP count

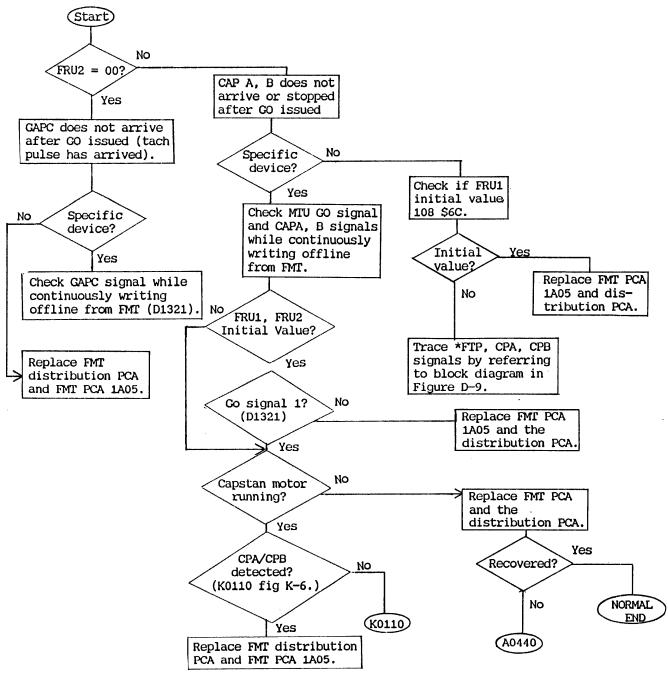
(2) Reject Code 012

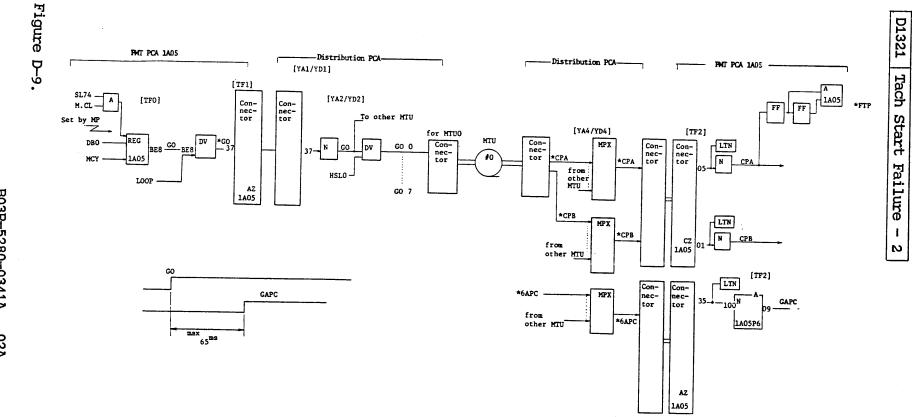
when GAP CTL is not detected within prescribed time after MTU start.

FRU1 108-QTP spacing

FRU2 00

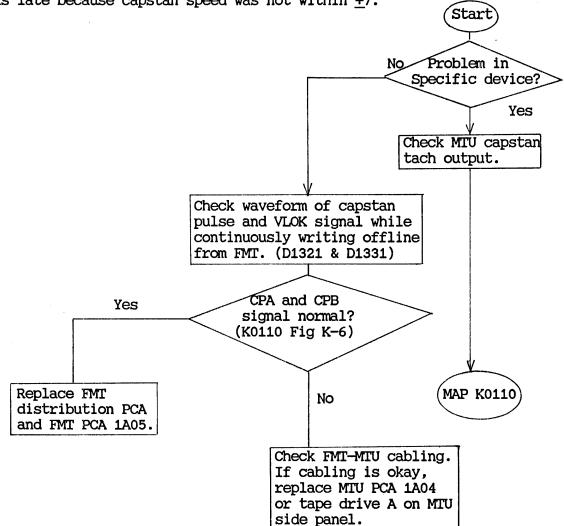
Prescribed time 65 ms





D1330 Velocity Check (Reject Code 112)

This error will be generated when velocity retry (over 16 times) has occurred during write operation. Velocity retry - DSB 12, bit 4. Write start was late because capstan speed was not within +7.



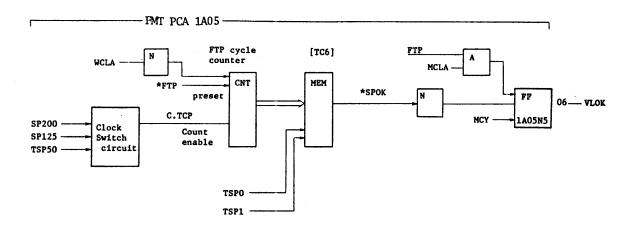
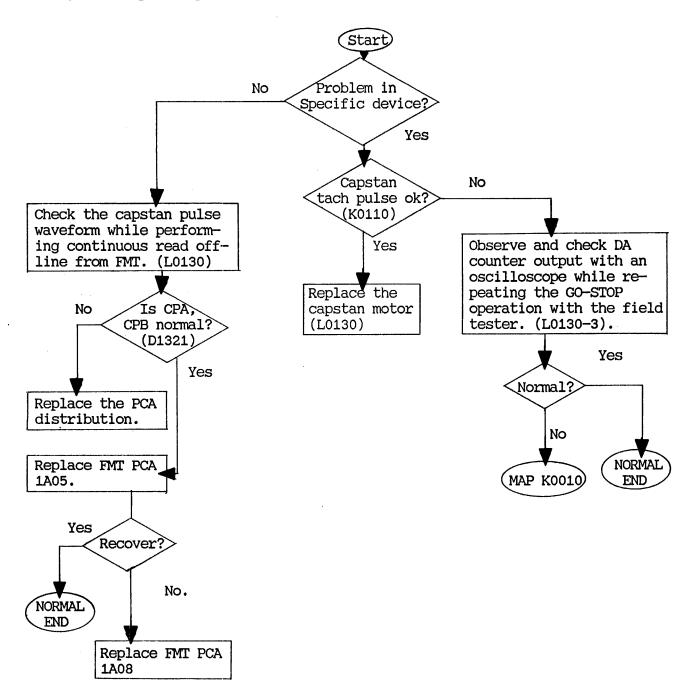


Figure D-10. Velocity check circuit.

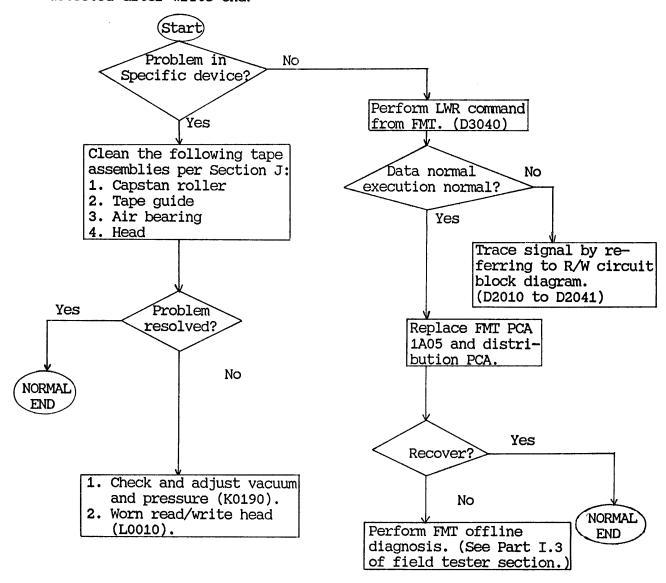
D1340 | Velocity Error

Error Multiplex Byte 1, bit 1. Velocity error is generated when the designated capstan speed is exceeded during write operation.



D1350 Early Begin, Slow Begin, and Slow-End Read Back Check.

- Early begin read back check (DSB11, bit 4) Error is generated in the following cases:
 - (1) When data-byte (800 bpi) or DBOB pattern (1600/6250 rpi) is detected within time (a) (see Figure D-11) at write command execution. (Data is detected too early.)
 - (2) When IBG is detected during writing (WOK signal on) at 800 rpi (IBG detected too early).
- Slow begin read back check (DSB11, bit 2) Error is generated when data-byte (800 bpi) or No. 5 pattern (1600/6250 rpi) is detected within time (b) (Figure D-11). (Data is detected too slow.)
- Slow end read back check (DSB11, bit 1)
 Error is generated when IBG is detected at over 70 QTP after block end detected after write end.



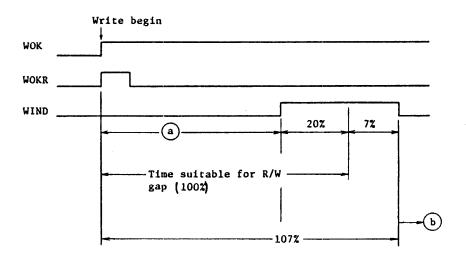


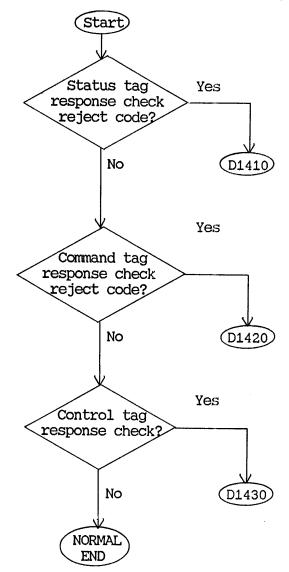
Figure D-11. Slip check timing.

D1400 Status Command and Control Tag Response Check

The FMT uses three tag signal lines (Status tag, Control tag, and Go tag) to control the MTU. The FMT uses the status tag line in conjunction with the control tag line as a command tag line when both the status and the control tag lines are activated.

When the FMT uses the status tag, control tag, and command tag lines to control the MTU, the FMT receives a response from the MTU. When the response is not normal, the status tag response check, control tag response check, and command tag response check are set.

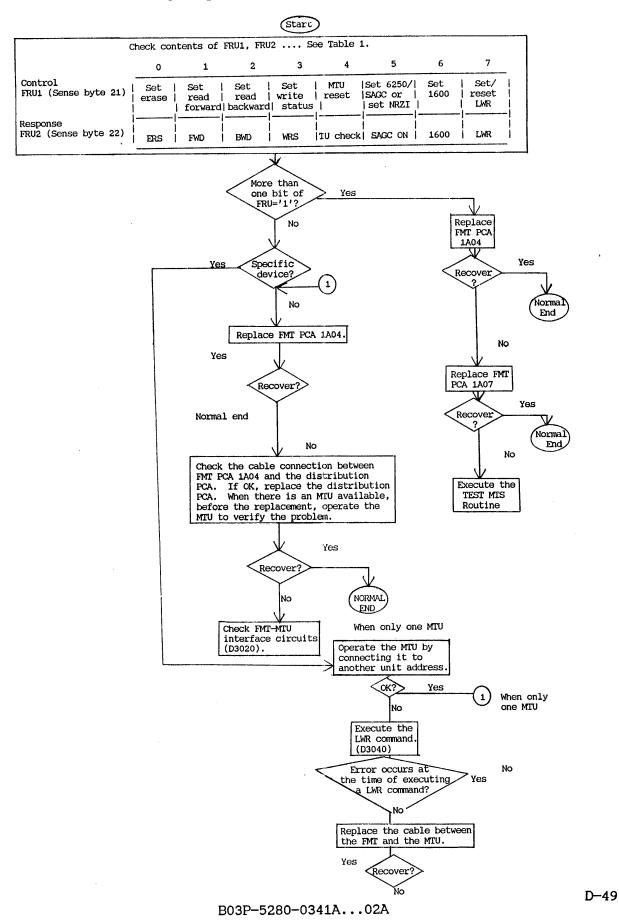
FRU1 (DSB14) ... Control data
(Content of DVBO register)
FRU2 (DSB15) ... Response data
(Content of DVBO register)

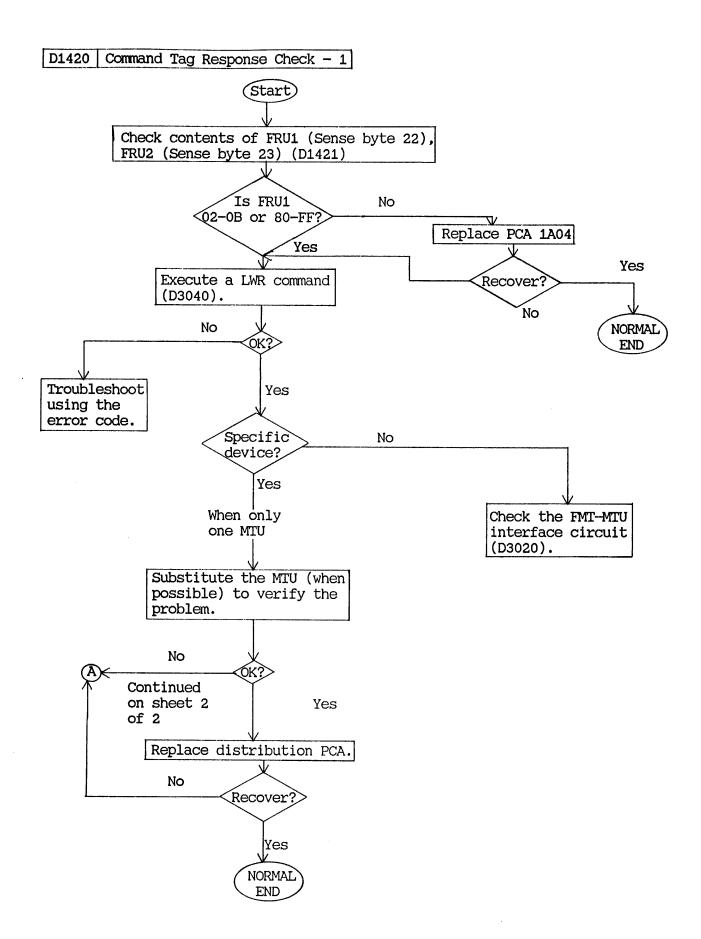


D1410 Status Tag Response Check

Table 1 Response check with status tag control

Control (FRU1) bit	Function	Response (FRU2) check	Time out
bit 0	Set ERASE ("1")	ERS=1, LWR=0 FWD=1, BWD=0	500 ms
bit 1	Set read forward ("1")	BWD=1, ERS=0 FWD=0 WR =0 LWR=0	500 ms
bit 2	Set read backward ("1")	BWD=1, ERS=0 FWD=0 WRS=0 LWR=0	500 ms
bit 3	Set read backward ("1")	ERS=1, BWD=0 FWD=1, LWR=0 WRS=1	500 ms
bit 4	Reset MTU ("1")	TU check = 0 (DVINT = 0)	10 μs (100 μs)
bit 5	Set GCR/NRZI ("1")	1600 = 0	13.6 ms
bit 6	Set PE ("1")	1600 = 1 SAGC = 0	13.6 ms
bit 7	Set LWR Reset LWR ("1")	LWR = 1 LWR = 0	13.6 ms

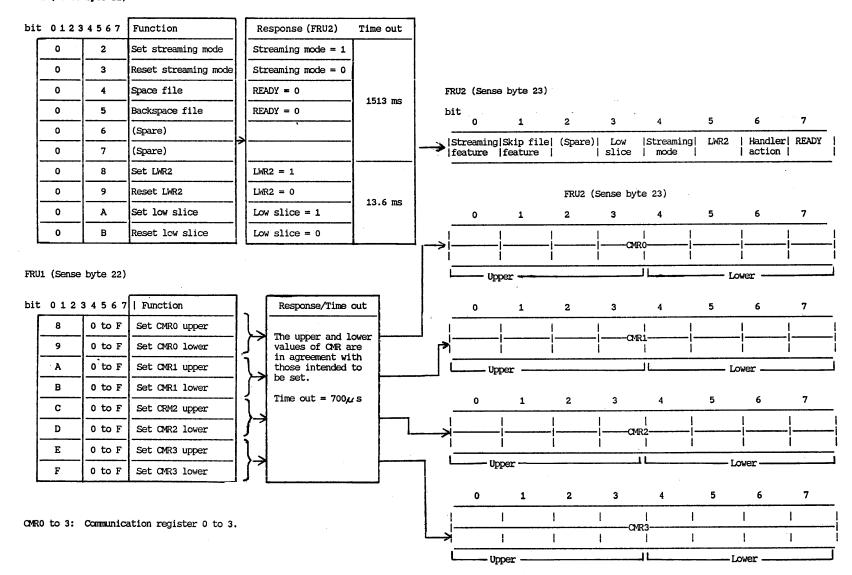




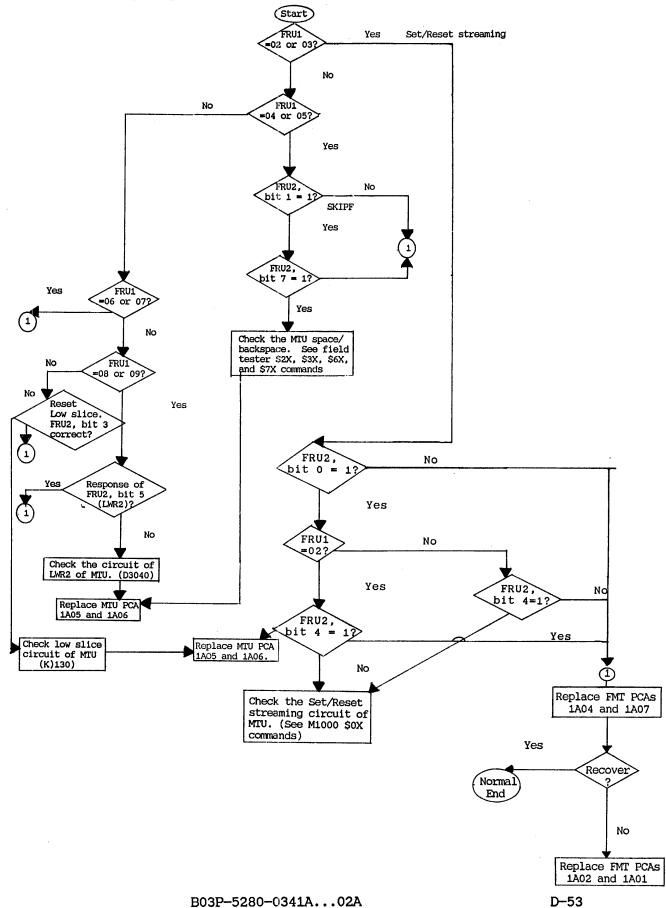
D1420 | Command Tag Response Check - 1 | Continued from sheet 1 of 2 No = 80 - FF Yes Tag-IN Yes response check (byte 11, bit 7)? D1440) No Does bit 3 Yes of FRU1 indicate 1? No Check that the lower 4 bits Check that the lower 4 bits of FRU1 are in agreement of FRU1 are in agreement with the lower 4 bits of with the upper 4 bits of FRU2? FRU2? 0 1 2 3 4 5 6 7 FRU1 FRU1 FRU2 FRU2 Yes (In agreement? No Replace FMT PCAs 1A04 and 1A07. Check the communicationregister circuit of MTU.

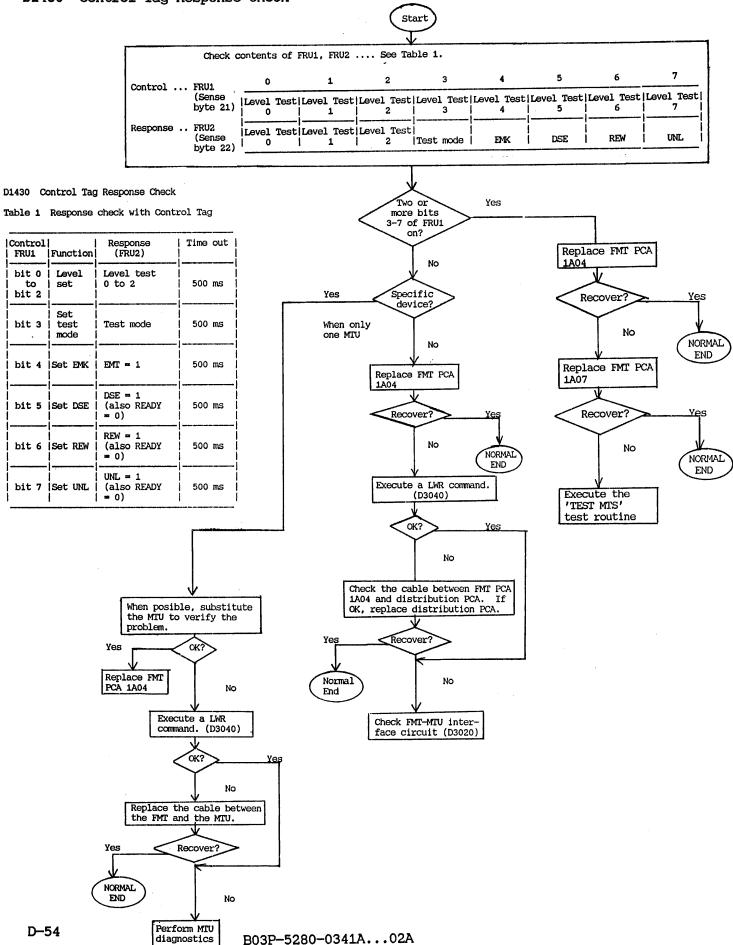
Replace MTU PCA 1A06.

FRU1 (Sense byte 22)



D1422 Command Tag Response Check - 3

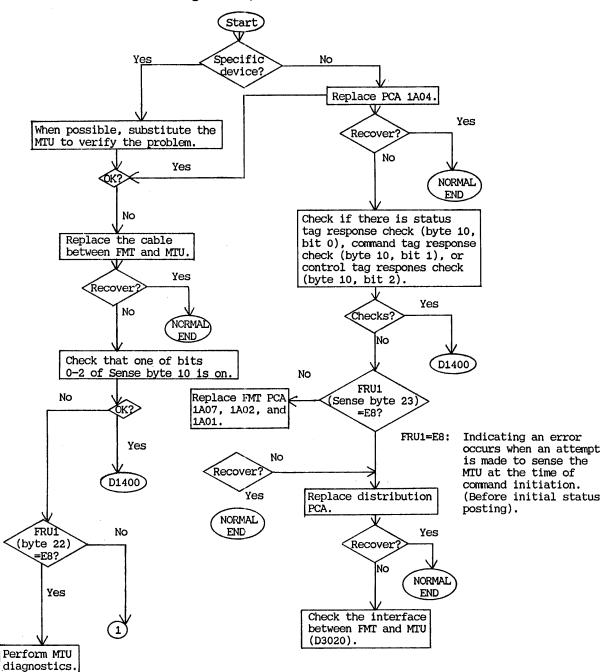




D1440 Tag In Check

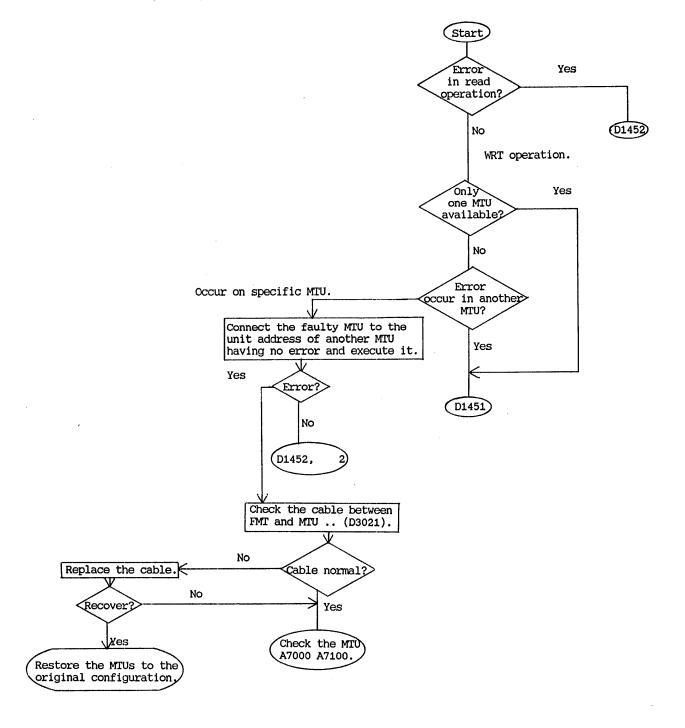
Error is generate when TAG-IN signal response does not arrive from MTU within the prescribed time.

(Prescribed time = 3 through 7 s)

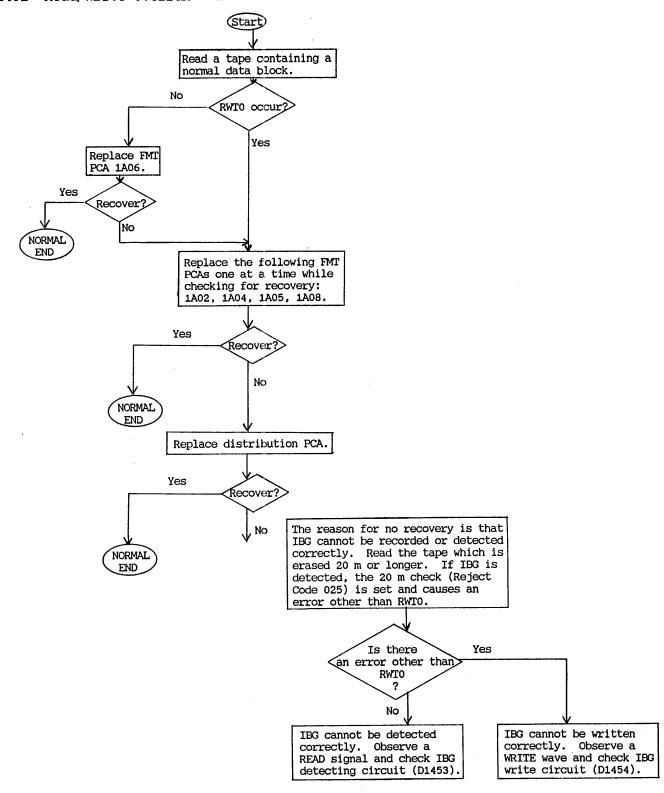


Sets when the write and read operations of one data block are carried out over 15 m or the time interval equivalent to 15 m run. RWTO

 $FRU1 \quad (DSB14) = 77$



D1451 Read/Write Overrun - 2



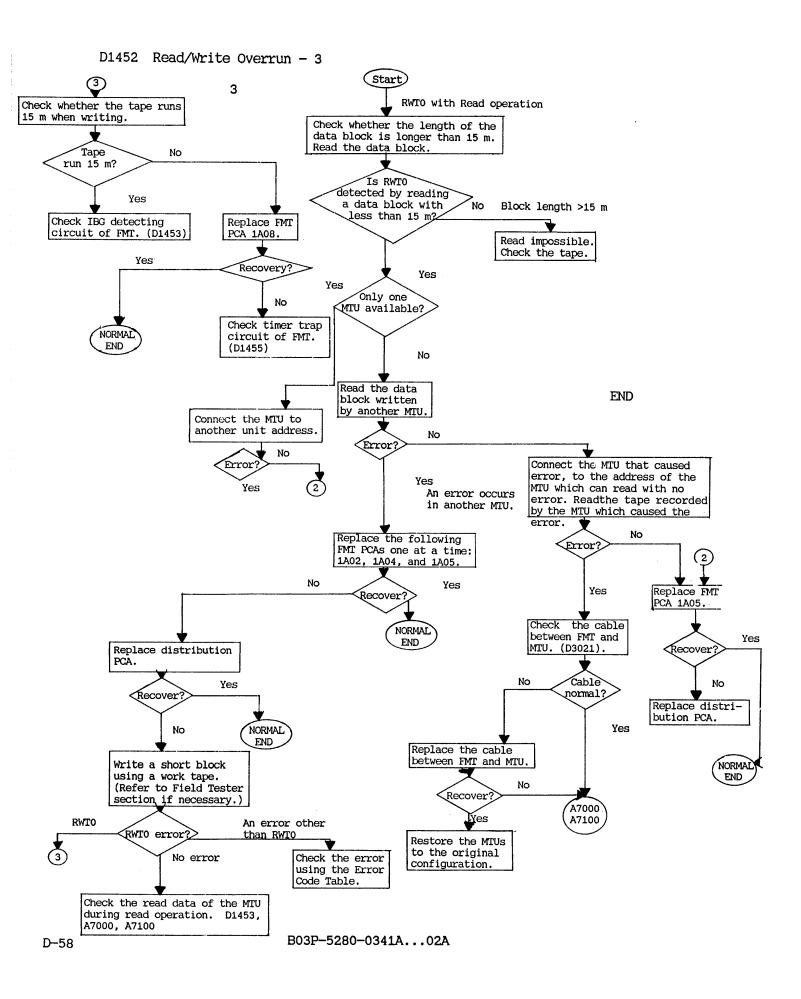


Figure D-12.

Time sense decode circuit.

logic

DIBG

BA4 -- DTM

[FN0] [TF2,TF3] [AA9] [FL7] - DBOB Time MET AG3 - DNOIS BE6 - DVB10- AA3 AA8 -- *PEKPO -BD8 TSNSO --- AH3 AH7 sense BA4 - DVBI1 - AD6 AG4 -AD1 - *PEKP1 -BD9 TSNS1 --- BB7 circircuit BBX - DVBI2 - ADU 12 ----- DARA ADZ - *PEKP2 -- BE7 cuit TSNS2 --- AH2 BD5 - DVBI3 - AG5 AH1 --- *PEKP3 ---- BDU TSNS3 --- AH1 11 -BAX - DBVI4 - AG9 AGY -- *PEKP4 -- BDV TSNS4 --- AG1 BAV - DVBI5 - - ALX AKZ --- *PEKP5 ---- BE3 TSNS5 --- BE1 BE2 - DVBI6 - BA9 BA4 --- *PEKP6 ----TSNS6 --- BB3 BD1 - DBV17 - BAX BD3 -- *PEKP7 -- BE2 TSNS7 --- BB5 BE3 - DBV18 - BDZ BDV - *PEKP8 -- BE6 TSNS8 --- BB2 1A02 WRS -1A02 1A05 1A04 *DTMN _ Distribution PCA Tape mark pattern signal issued in the 800-bpi mode ROK DVBIO to 8 Other MTU TSNSO to 8 DBOB Selection DIBG

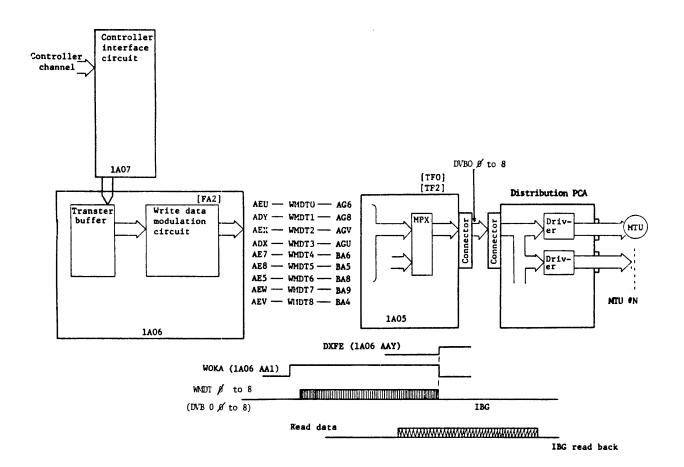


Figure D-13. Write data circuit.

D1455 RWTO Trap

FTP pulses generated from CPA and CPB tach signal are counted by 16 bit counter. When the counter overflows (65536 count), TMINT signal is generated and a microprocessor trap occurs. If FTP signal has been generated correctly, the trap takes place after 8.23/4.94/3.09 seconds have elapsed in the 75/125/200 ips speed mode. GO signal to the MTU is turned off if IBG has been detected before the time elapse.

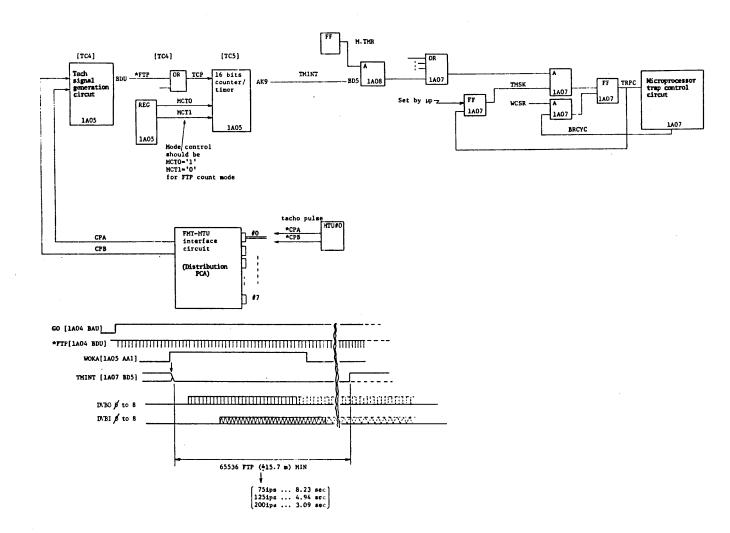


Figure D-14. RWTO trap.

D1460 Missing Position - 1 (Reject Code 035)

When a data check error is generated in write, Read or Read backward command operation, the information concerned with the length of block recorded in the operation is stored in communication register of MTU. For error recovery the Back Space command corresponding to the Read and Write command or the Space command corresponding to the Read Backward command is issued. The space length (associated with Space or Back Space command) is compared with the error block length stored in communication register. When the difference between the lengths is larger than the requirement, Reject Code 035 is generated.

FRU1 (DSB14) and FRU2 DSB15) provide information of the length discrepancy.

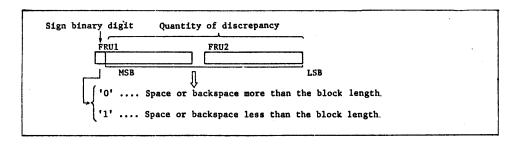
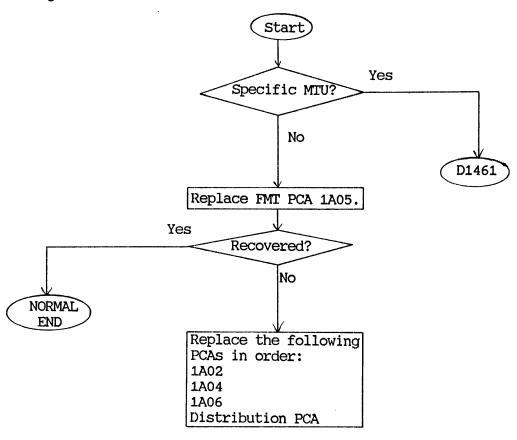


Figure D-15.



D1461 | Missing Position - 2

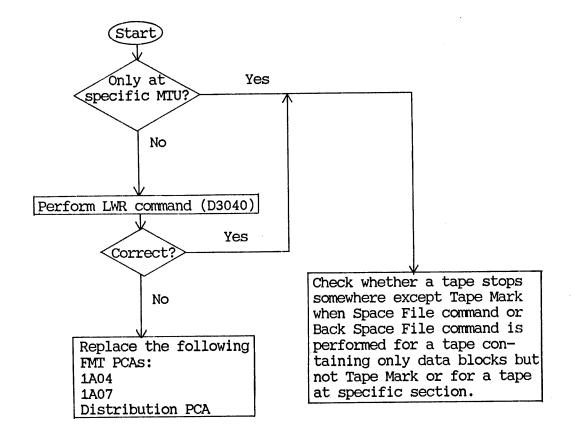
Check for abnormality of capstan. (K0110)

D1465 | Missing Tape Mark Reject Code 316

After instructing MTU to search for Tape Mark Search in order to perform Space File or Back Space File command an error occurs:

- 1) When Tape Mark block cannot be detected correctly, though MTU enters ready status. (Bit 7 of TU sense byte, (Tape Mark) is 0.)
- 2) When MTU detects an interruption (except BOT detection and Tape overrun of the MTU).

Note: In this case, RWTO (Sense byte 11, bit 0) is also generated.



Data check occurs when the following errors are detected:

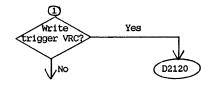
(1) R/W and internal circuit error:

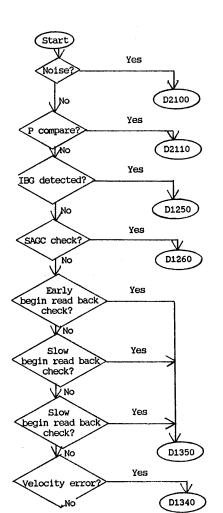
CRC error	MUX byte	1 - P
Uncorrectable error/skew error	byte	6
Partial Record	byte	5
Multiple track error/LRC error	byte	4
Miscellaneous Data error	byte	3
End of Data check/VRC error	byte	2

Details of Miscellaneous Data error

IBG Detected	DSB	11 - 7
Start Read check	DSB	- 6
CRC III check	DSB	- 5
SAGC check/Noise error	DSB	– 3
P compare	DSB	- 0
Skew error	DSB	12 - 3
Write Error Count Overflow	DSB	- 2
Envelope check	DSB	- 1
Write Trigger VRC	DSB	- 0

(2) Tape speed error





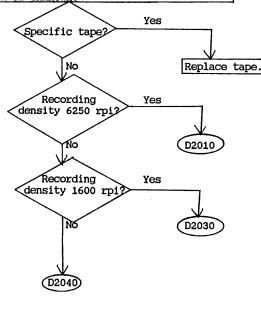
R/W data errors:

Refer to D2001, 2 for a description of each error. Check error track from sense data.

- o 6250 rpi error track
- Track at which dropout, invalid pattern, phase error generated.
- o 1600 rpi error track
- Track where dropout, phase error generated.
- 800 rpi error track

Track at which error was generated when there was an error at a single track.

'1' is set in bits 6, 7 when there was an error, but the track is unknown



D2001 Data Check Sense Byte Explanation - 1

- Uncorrectable error occurs:
 - (1) When recoverable VRC error generated at read (read backward command).
 - (2) When VRC error generated at write (LWR command). (May have CRC error set also.)
- Multiple track error/LRC error occurs:
 - (1) When there is a pointer of 2 tracks or more at 6250 rpi write (LWR command).
 - (2) When there is a pointer of 3 tracks or more at 6250 rpi read (read backward).
 - (3) When there is a pointer of 2 tracks or more at 1600 rpi read (read backward).
 - (4) When 800 rpi horizontal parity check error was generated. (Error Track may have been reset by RESYNC at 6250 rpi read operation.)

• Skew error occurs:

(1) When excessive skew detected at 6250/1600 rpi read, read backward, write command.

6250 rpi write	RIC-ROC	2
1600 rpi write	RIC-ROC	14
6250 rpi read	RIC-ROC	30
1600 rpi read	RIC-ROC	15

- (2) When excessive skew detected at 800 rpi write, write tapemark command.
- End data check/CRC error occurs:
 - (1) When postamble cannot be detected at 1600 rpi read operation. (No READEND)
 - (2) When postamble is not all "1"s at 6250 rpi or not all "0"s at 1600 rpi.
 - (3) When postamble is too long.
- Envelope check occurs:

When dropout detected at 1600 rpi/6250 rpi write operation.

Notes:

- (1) Envelope check does not cause Data check at 6250 rpi operation.
- (2) Use D2010 D2020 for 6250 rpi.
- (3) Use D2030 D2032 for 1600 rpi.
- (4) Use D2040 D2041 for 800 rpi.

D2002 Data Check Sense Byte Explanation - 2

- Start read check
 - (1) When IBG is encountered before data detected after block is detected (at 6250/1600 rpi operation).
 - (2) When data is not detected within the prescribed time after block is detected (at 6250/1600 rpi operation).
- Partial record
 When IBG encountered in data at 6250/1600 rpi.
- IBG detected When IBG is detected while reading data at 6250/1600 rpi write command.
- CRC error occurs:
 - (1) When CRC is not normal pattern.
 - (2) When CRC III error is set.

D2003 Explanation of CRC III Error

- CRC III error occurs:
 (1) When CRC-B byte and CRC-D byte match at 6250 rpi write (read command).
 (2) When CRC-C byte was incorrect pattern (at 6250 rpi read backward).
 (3) When CRC-B byte and CRC-C byte didn't match (at 1600/800 rpi write command).

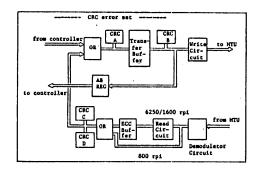
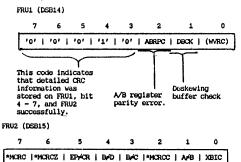


Figure D-16. CRC generation circuit.

Mode	6250 rpi	1600/800 rpi	Sense		
Write	A≠B	A≠B	P compare		
WEICE	B≠D	B/= C	CRC III error		
Read	A≠B	A≠B	P compare		
Reau	B≠D	_	CRC III error' .		
Read	A≠B	A≠B	P compare		
	CAMatch pattern		CRC III Error		

- o CRCA: CRC pattern is generated from transfer buffer input.
 o CRCB: CRC pattern is generated from transfer buffer input.
 o CRCC: CRC pattern is generated from read data.
 o CRCO: Set CRC of read data at 6250 rpi.
 o When CRC III error or P Compare error is indicated (in the DSB11 FRU1 and FRU2 described below).

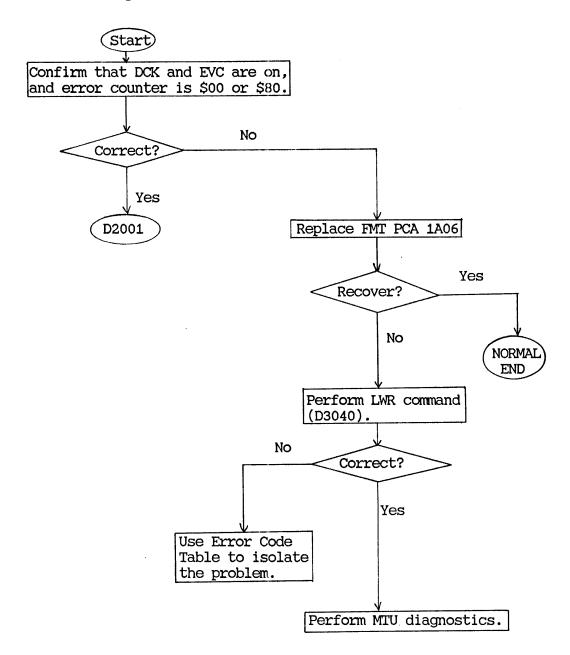


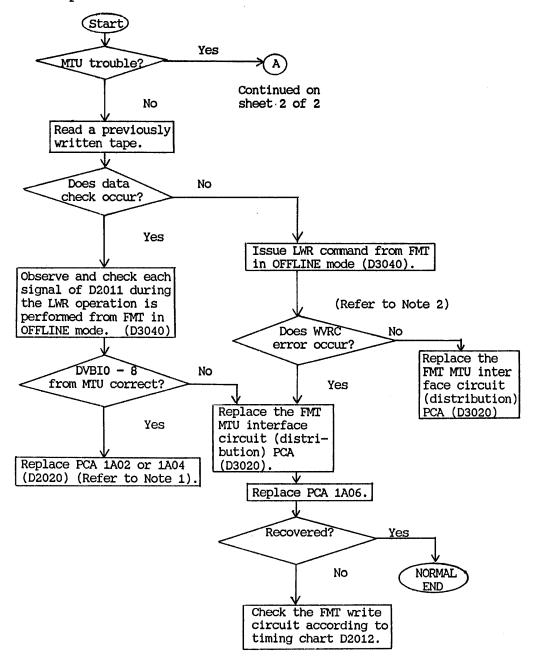
Contents of CRCST register

- o *MCRC (Not match CRC)
 "1" when CRC pattern generated as a result of read operation is not normal.
- o *MCRCZ (Not match CRC zero)
 "1" when CRC pattern generated as a result of read operation is not all
 '0's.
- o EP/CR "1" when CRC pattern does not match EP (error pattern) register.
- o B#D "1" when CRCD does not match CRCB.
- o B/C "1" when CRCB does not match CRCC.
- o *MCRCC (Not match CRCC)
 "1" when CRC pattern obtained from read data excluding CRC byte is not normal.
- o A#B
 "1" when CRCA does not match CRCB.
- XBIC Transfer buffer bus in check, "1" when illegal XFR Buffer input data is applied.

D2004 Error Count Overflow

The error counter is incremented if EVC (Envelope check: DSB12, bit 1) is generated as a result of performing the write operation in the 6250/1600 rpi mode. When performing write operation in 6250 rpi mode, if the error counter reaches \$00 or \$80, ECOVF (error counter overflow: DSB12, bit 2) is generated. ECOVF is generated each time 128 EVC errors are detected. The error counter is provided for each MTU.



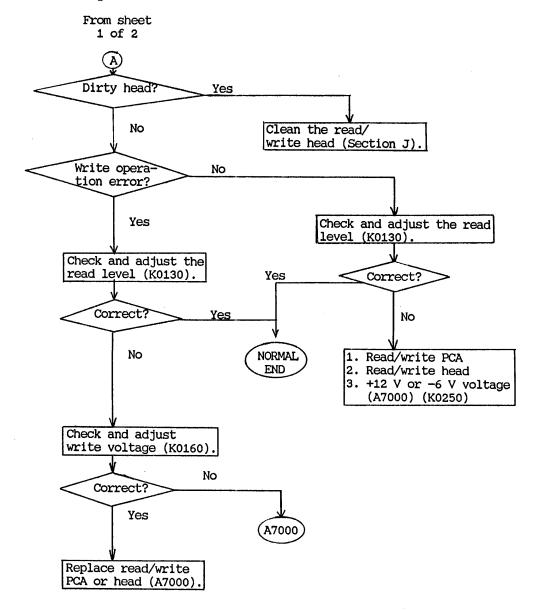


Note 1: How to search error track:

- (1) Place the FMT in offline mode and perform LWR command (D3040)
- (2) After the LWR command is performed, an errored track can be checked by displaying the register at \$22.

Note 2: How to search error:

- (1) Display the contents of the register at \$24.
- (2) WVRC is bit 3.



- Note 1: How to search error track:
 - (1) Place the FMT in offline mode and perform LWR command (D3040)
 - After the LWR command is performed, an errored track can be checked by displaying the register at \$22.

Note 2: How to search error:

- Display the contents of the register at \$24.
 WRC is bit 3.

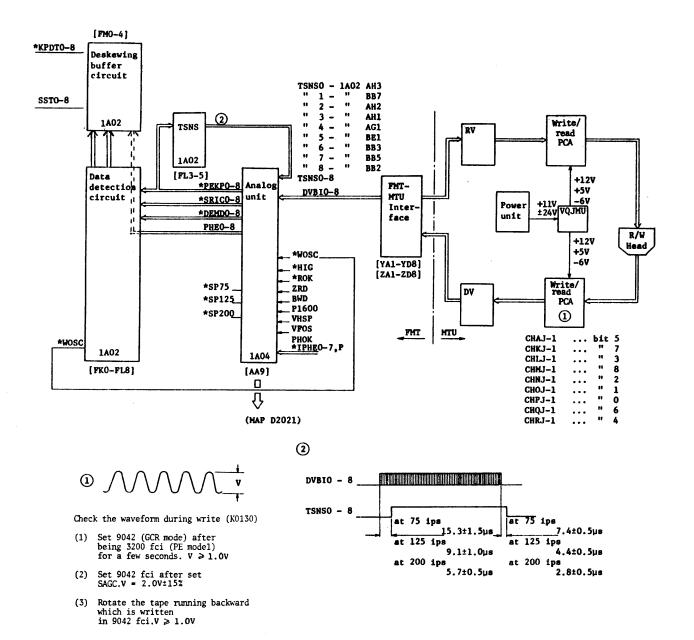
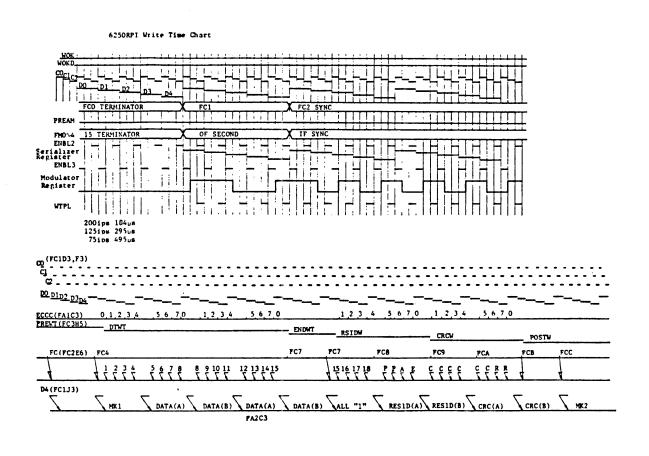


Figure D-17. 6250 rpi data check.



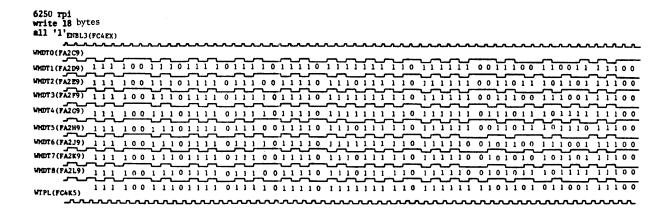


Figure D-18.

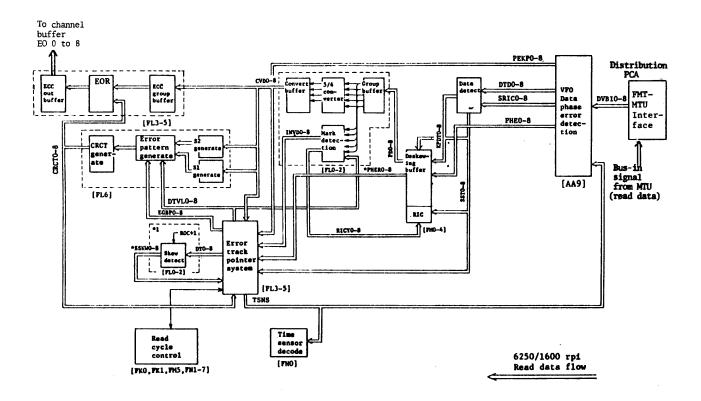
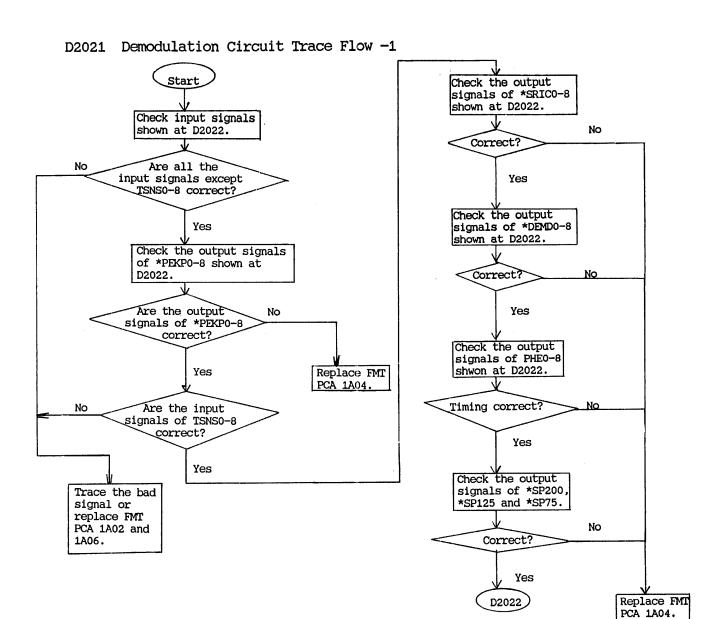


Figure D-19.



Note:

- (1) See next page for input signals.
- (2) See following page for output signals.

Table 1. Input signals.

		_	Bit									
Item	Signal name	Contents		1	2	3	4	5	6	7	8	Reference
1	Peak signal (DVBIØ-8)	Read peak position signal from MTU	AA3	AD6	ADU	AG5	AG9	ALX	GA9	BAX	BDZ	Figure D-20 Table 3
2	Time sense (TSNSØ-8)	VFO input changing signal	AAU	AAV	ADY	AHZ	AK1	AKV	BA6	BD5	BD6	Figure D-22
3	Error genera- ted signal (IPHEØ-8)	Read peak position signal from MTU	AB7	AD3	AEV	АН7	AHW	BB1	BB3	BE2	BEW	Ordinarily +2.4 V +5.0 V
4	Read OK (*ROK)	Read start signal signal from MTU		AL7						Figure D-22		
5	Z read (*ROK)	Signal indicating 800 bpi		AK6								
6	Backward (BWD)	Signal indicating tape running direction	AL6						alad valero de 1800 tres turo			
7	Write clock (*WOSC)	Clock signal of basic frequency	AKU						Figure D-21 Table 3			
8	VFO start (*VFOS)	Signal to reset VFO and start		AK8						Figure D-22		
9	Speed signal (*HSP)	Signal indicating tape speed		AL3								
10	1600 signal (P1600)	Control signal indicating record density	AL5									
11	High gain signal (HIG)	Control signal indicating record density	BB5						Figure D-22 Table 4			
12	Phase OK (PHOK)	Signal to start data demodulation	AK4						Figure D-22			

D2022 Demodulation Circuit Trace Flow - 2

Table 2. Output signals.

T# cm	Signal name	Combonts	Bit									Reference
Item Signal name	Signar name	Contents		1	2	3	4	5	6	7	8	Reference
1	Peak pulse (*PEKPØ-8)	Rising and falling pulses of peak signl	AA8	AD1	ADZ	AHl	AGY	AKZ	BA4	BD3	BDW	Figure D-20,
2	Read clock (*SRICØ-8)	Clock to get demodulation data	AA6	ABX	AD8	AEX	AGX	ALB	BBU	BZY	BDX	Figure D-23
3	Demodulation data (*DEMDØ-8)	Data recognized with 1 and 0	AV3	AE6	ADV	АН5	AHU	AKY	BBU	BZY	BDX	Figure D-23
4	Phase error (PHEØ—8)	Phase error detected signal	AA5	AAX	AEW	AG4	AGV	ALW	BAl	BD1	BD8	Figure D-24
5	*SP200 *SP125 *SP75	Signal indicating speed function of VFO	AEL AK3 AK5									

Table 3. Cycle of Tl and T2.

Record density	Tape speed	Tl and T2
	200 ips	555 <u>+</u> 100 s
625Ø	125 ips	885 <u>+</u> 18Ø s
rpi	75 ips	1475 <u>+</u> 300 s
	50 ips	22Ø <u>+</u> Ø.5 s
	200 ips	1.56 <u>+</u> 0.3 s
1600	125 ips	2.50 <u>+</u> 0.5 s
rpi	75 ips	4.20 <u>+</u> 0.8 s
	50 ips	6.25 <u>+</u> 1.3 s

Table 4. High gain.

Record density	Write/read	*HIG			
6250 rpi	Write	+2.4~+5.0 V			
0230 Ipi	Read	Figure D-23			
1600 rpi	Write/read	+2.4~+5.0 V			

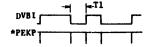


Figure D-20. DVBI and PEKP.

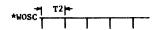


Figure D-21. WOSC.

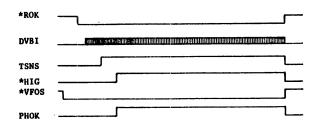


Figure D-22. Input timing.

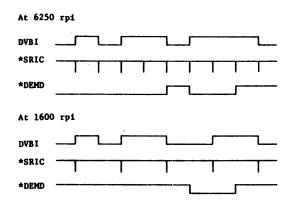


Figure D-23. Output timing.

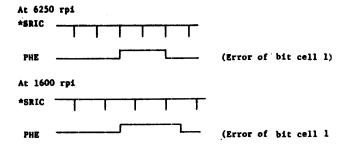
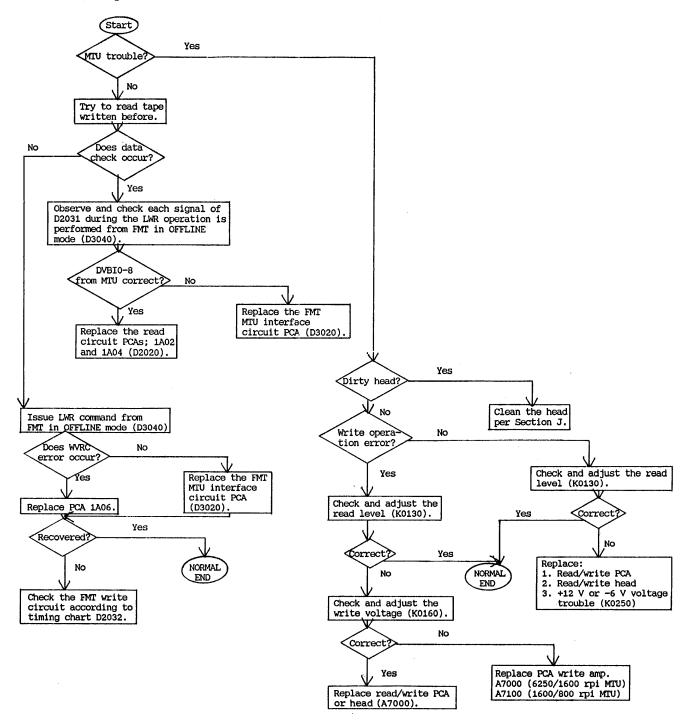


Figure D-24.

D2030 1600 rpi Data Check - 1



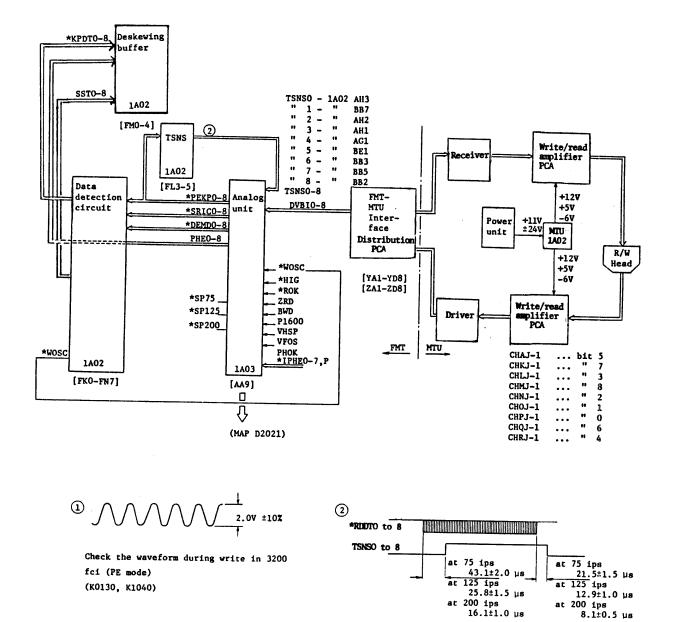


Figure D-25.

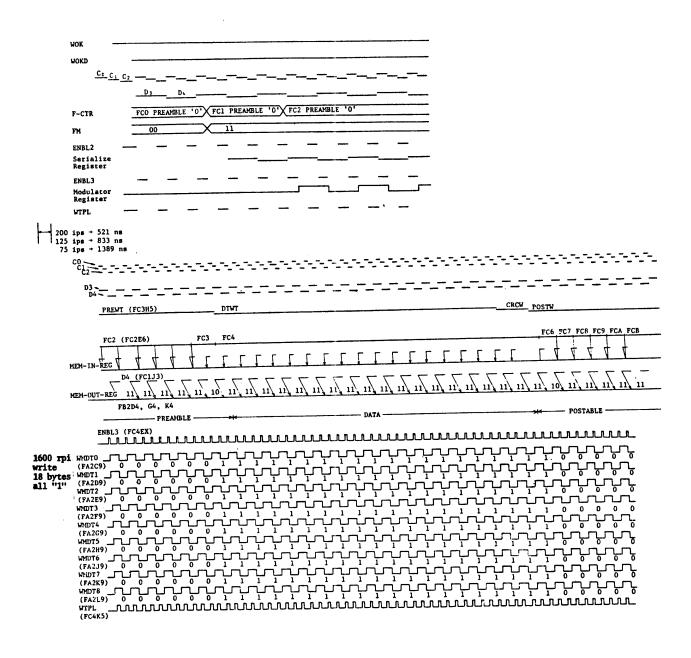
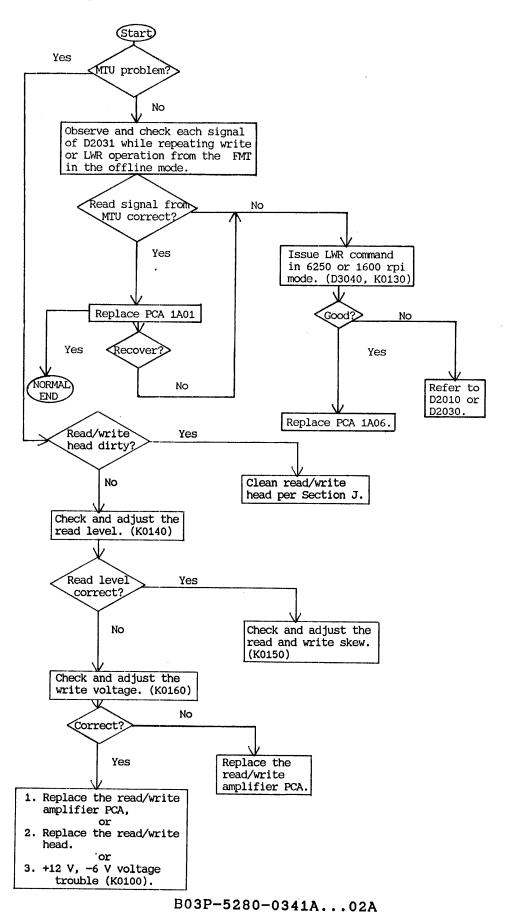


Figure D-26.



```
Bit 0: 1A04 AA8
                                          Bit 0: 1A04 AA3
                     Bit 1: 1A04 AD1
                                          Bit 1: 1A04 AD6
                     Bit 2: 1A04 ADZ
                                          Bit 2: 1A04 ADU
                     Bit 3: 1A04 AH1
                                          Bit 3: 1A04 AG5
                     Bit 4: 1A04 AGY
                                          Bit 4: 1A04 AG9
                     Bit 5: 1A04 AKZ
                                          Bit 5: 1A04 ALX
                     Bit 6: 1A04 BA4
                                          Bit 6: 1A04 BA9
                     Bit 7: 1A04 BD3
                                          Bit 7: 1A04 BAX
                     Bit 8: 1A04 BDV
                                          Bit 8: 1A04 BDZ
     {FB1}
                  (SA1 through SA7)
                                                 AA9
Transfer
                                                 Analog
buffer
                                                 unit
       NRD 0 through 8
                         (3)*PEKP0 through 8
                                                           DVBIO through 8
1A06
                                                   1A04
(YA1 through YD8)
(ZA1 through ZD8)
Distribution PCA
                                                                      FMT
  (1A1)
RV
          ⇒ Read/write
                                                                      MTU
            amplifier
            PCA
                                           R/W
Power
                         +12V
                                           head
supply
           +11V, +24V
                         +5V
unit
                         -6V
                  PCA
                  1A02
                  in MTU
DV
          Read/write
          amplifier
          PCA
              (1)
                        CHAJ-1 ... Bit 5 (Track 1)
                        CHKJ-1 ... Bit 7 (Track 2)
                        CHLJ-1 ... Bit 3 (Track 3)
                        CHMJ-1 ... Bit 8 (Track 4)
                        CHNJ-1 ... Bit 2 (Track 5)
                        CHOJ-1 ... Bit 1 (Track 6)
                        CHPJ-1 ... Bit 0 (Track 7)
                        CHQJ-1 ... Bit 6 (Track 8)
                        CHRJ-1 ... Bit 4 (Track 9)
```

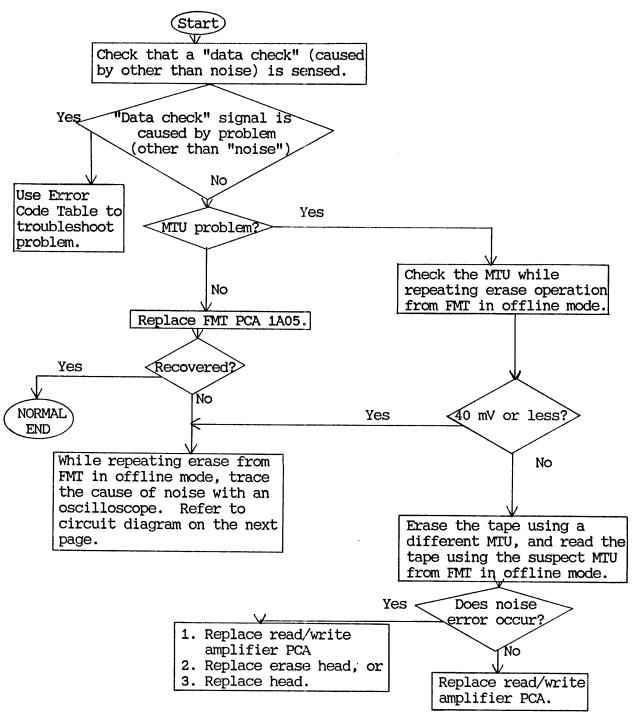


Observe the wave form while repeating the write operation in 800 fci (NRZI mode from the field tester. $\mbox{(KO130)}$

Figure D-27.

Noise error occurs when:

- (1) Data check is set to on during the read or read backward command.
- (2) A noise block is detected read or read backward command.
- (3) Data is detected during the erase, write tape mark, or write command.



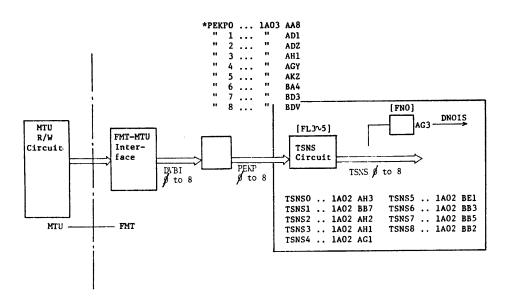


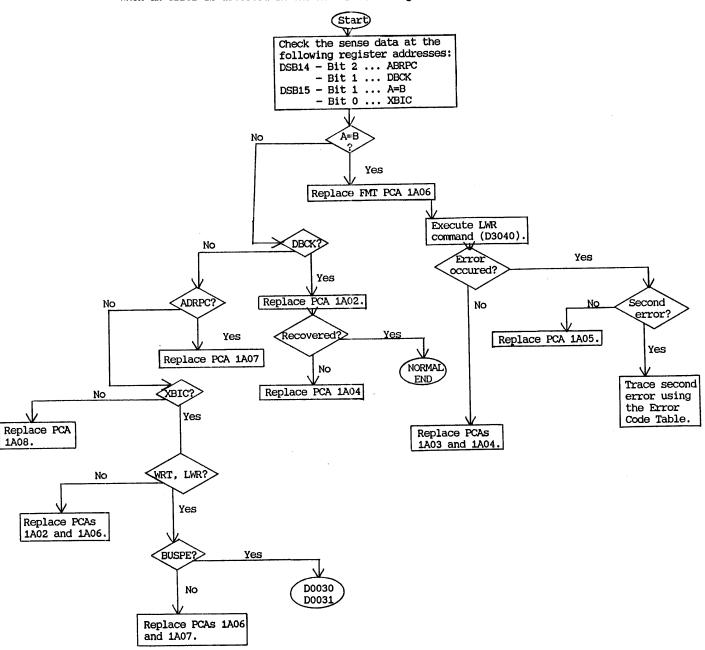
Figure D-28.

D2110 P (Parity) Compare

 ${\tt P}$ compare means FMT parity check or compare check. ${\tt P}$ compare occurs in the following cases.

- (1) Transfer buffer check (A≠B): when the comparison between transfer buffer input and output data does not agree. (CRCA ≠ CRCB).
- (2) Parity check transfer buffer (XBIC):
- When a partiy error is detected in the transfer buffer input data.

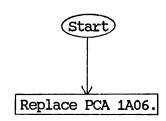
 (3) A/B register error (ABRPC):
- When a parity error is detected in the A/B register at read operation.
- (4) Deskewing buffer check (DBCK):
 When an error is detected in the ROC of deskewing buffer.



D2120 W-VRC Error

W-VRC error occurs when:

- (1) Parity error occurs in WTDO through 8 at write trigger VRC circuit. In this case, "IBG detected" is not set.
- (2) Writing on creased tape. IN thins case, "IBG detected" is set.



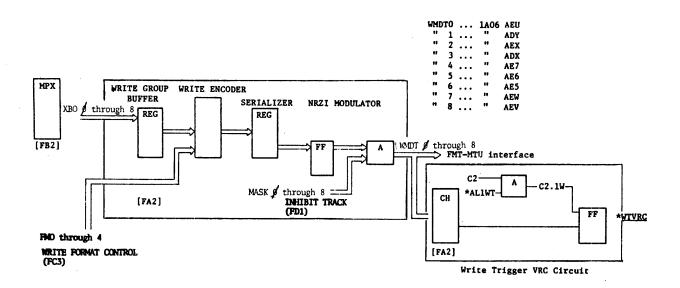


Figure D-29.

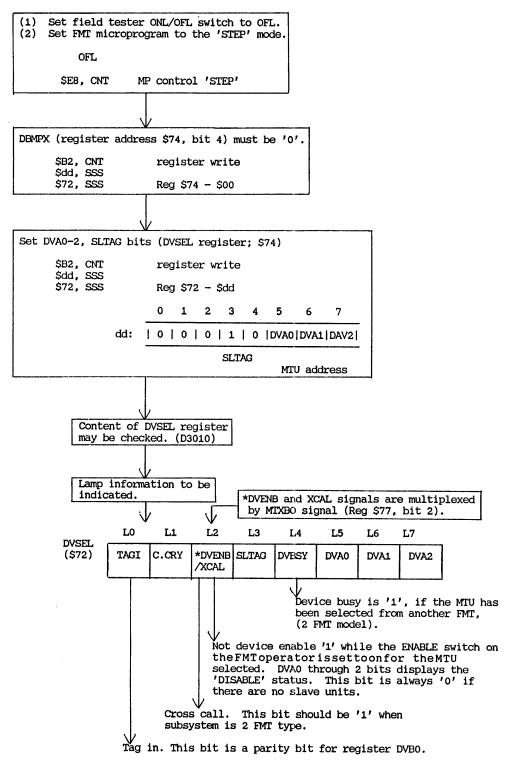
D3000 MTU Sense Error

D3000 MTU Sense Error

The MTU status (BWD, NOT-FP, TWA or BOT, WRS, ONL, READY, etc.) can be displayed on field tester.

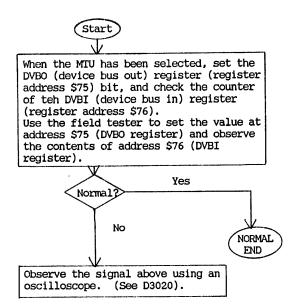
MTU sense bytes representing the MTU status are listed in D3010.

To inspect TU (tape unit) sense bytes, use the instructions below:



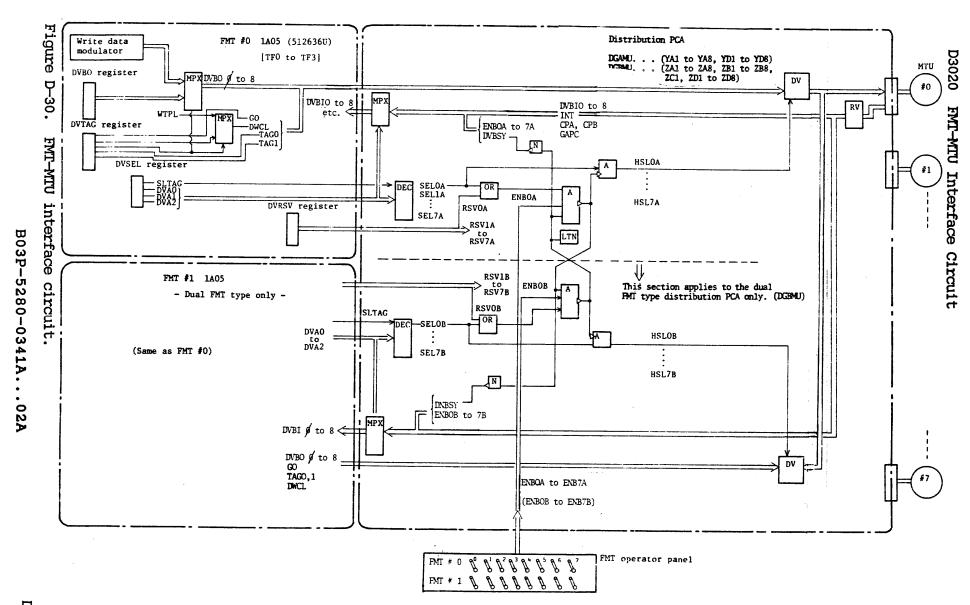
Note: '1' means on or lit condition.

D3010 MTU Sense Bytes Configuration



MTU sense bytes.

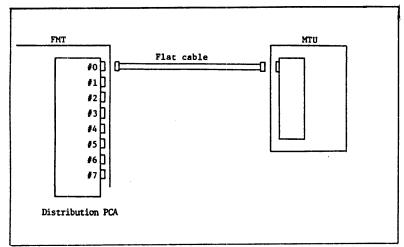
TU sense byte	Ø	1	2	3		4		5	6	7	8																								
Bus-out bb: Bus-in	\$Ø1 (\$ØØ)	\$Ø2	\$Ø 4	\$	\$Ø8		1Ø	\$2Ø	\$4Ø	\$8Ø	\$41																								
Bit Ø	BWD	New function	MISC error	VE	LØ	/	27	SAGC count Ø	Read data Ø	Error code Ø	Handler erase current ON																								
Bit 1	NOT FP	Reset key	Tape loop alarm left	VE	Ll			SAGC count 1	Read data 1	Error code 1	Handler action																								
Bit 2	TWA	DSE	Tape loop alarm right	Ready hold						hold								hold		hold		hold		hold		hold		hold		uniq	unit ue ID order	SAGC count 2	Read data 2	Error code 2	Handler backward status
Bit 3	вот	7 tracks	ROM parity error	1	212	10w	l	SAGC count 3	Read data 3	Error code 3	Handler write current ON																								
Bit 4	Write status	Test mode	Write circuit alarm		211			EC level 2	Read data 3	Error code 4	Handler 65% slice																								
Bit 5	ONLINE	Dual density	Fuse alarm	Tape uniqu	e ID			EC level 2	Read data 5	Error code 5	Handler overrun																								
Bit 6	TU CK	High density	Air bearing alarm	nign	order			EC level 2	Read data 6	Error code 6	Handler PE mode																								
Bit 7	READY	625Ø	Load failure		28		2 ^Ø	EC level 2	Read data 7	Error code 7	Tape mark																								
Bit 8	TAG-IN	TAG-IN	TAG-IN	TAG	/ HIN		_IN	TAG-IN	Read data 8	TAG-IN	TAG-IN																								

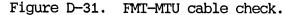


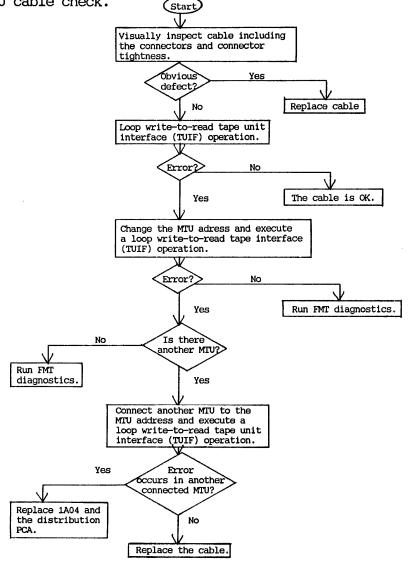
D3021 Investigation of the Cable beteen the FMT and the MTU

If a failure occurs in a specific MTU, check the cable between the FMT and

the MTU.







D3040 Loop Write-to-Read Command (LWR) Execution - 1

Execute the loop write-to-read tape unit interface (LWR TUIF) operation offline from the FMT using the field tester, as follows:

- (1) If the FMT is not connected with a field tester, proceed to step (2). If a field tester is connected, proceed to step (7).
- (2) Set the field tester ONL/OFL switch of to OFL. Connect the field tester to 1A08 on the FMT.
- (3) To execute system reset and lamp test, steps (4) to (5) should be performed; otherwise, proceed to step (7).
- (4) Set field tester switches SO to S7 to \$FO. (Lamp test). LO to L11 must all light or the field tester is not operating correctly.
- (5) Toggle the CNT switch. (System reset).
- (6) L8 (ERRF), L10 (PHLT), and L11 (PERR) should go off.
- (7) To set a command code, the field tester is operated in the following sequence. When register address \$3D is displayed in the register and command code is already set, this procedure may be omited.

```
S0 - S7
          SB2
CNT-SW
          ON
S0 - S7
          $80 (LWR TUIF bit)
SSS-SW
          ON
S0 - S7
          $39 (SDIA1 Reg.)
SSS-SW
          ON
S0 - S7
          $B2
CNT-SW
          ON
S0 - S7
          $86 (6250 rpi)
          $46 (1600 rpi)
          $06 (800 rpi)
SSS-SW
          ON
S0 - S7
          $3D
SSS-SW
          ON
```

(continued on D3040-2)

D3040 Loop Write-to-Read Command (LWR) Execution - 2

(8) To set a device address, the field tester is operated in the following sequence. When register address \$3E is displayed in the register and the device address is set, this procedure may be omitted.

$$SO - S7$$
 \$B2
 $CNT-SW$ $ON \triangle \triangle$
 $SO - S7$ \$
 $SSS-SW$ ON
 $SO - S7$ \$3E
 $SSS-SW$ ON

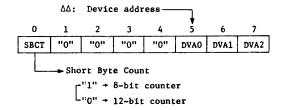


Figure D-32.

(9) To set the byte count, the field tester is operated in the following procedure. When register address \$3F is displayed in the register and is already set at a predetermined byte count value, this procedure may be omitted.

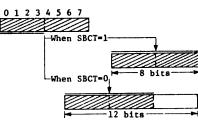


Figure D-33.

(continued on D3041)

D-94

B03P-5280-0341A...02A

D3041 LWR TUIF Operation Execution - 3

(10) Preparation for executing an LWR TUIF operation is completed by performing steps (7) and (8). Various parameters are available for the execution of an LWR command. To modify the execution of the LWR TUIF using these parameters, registers the parameters into SDIAO TUIF (address \$38) to SDIA3 (address \$38) and OFLCNT (address \$3C). Refer to field tester section for operation instructions, if necessary.

When performing these operations, if there is doubt about the register contents, observe the contents of registers.

These registers are never reset except when the FMT is powered on.

(11) Execution of an LWR TUIF operation

An LWR TUIF operation is executed immediately when the SSS switch of field tester is toggled. When the 'REPEAT' parameter is designated, the executio of an LWR TUIF is repeated (without toggling the SSS switch) until 'REPEAT' parameter is reset, a stop condition is made by such parameter as 'UNIT-CHECK-STOP', or 'SINH' is indicated. If there is no 'REPEAT' parameter in the register, an LWR TUIF is executed when the SSS switch is toggled.

(12) Confirmation of the execution result

When the execution of an LWR TUIF results in an error, ERRF bit, L8 (L8 lamp is used when S0 to S7 are set to \$80) lights. When this bit lights, it indicates that an error is contained in the END status of the executed command. This lamp remains lit from generation of the END status to the next command. The END status is stored in DSB register at address \$0A.

(13) Sense byte

Since the sense data that indicates the cuase of error is stored in SBO (address \$20) to SB23 (address \$2B) when the ERRF lights (when the UNIT CHECK of DSB register address \$0A is set on), check the contents of these register through the register display function of field tester instead of issuing a sense command.

(14) Reject Code

If REJECT signal is set, the reject code is stored in RJC (address \$30).

D3042 LWR RW Operation

The LWR RW operation allows the MTU to bypass write data at different points shown in Figure D-34, below. LWR RW operation is useful during MTU Read/Write fault isolation.

When a Read/Write problem occurs on a specific MTU, examine LWR RW operation. If LWR RW operation has resulted in succewss, the fault probably is in the Write/Read amplifier, Read/Write head, or in an amplifier/head adjustment refer to A7000, A7100.

If LWR RW operation has resulted in failure, LWR TUIF operation should be executed. Then the faulty PCA can be replaced.

To execute LWR TUIF operation with an MTU, procedure (1) - (6) in D03040 should be performed. To execute LWR RW operation, detailed procedures are described in D3043.

- Restriction -

- 1) Reject Code 207 is set when the MTU detects BOT or is in the 800 rpi mode.
- 2) Executing LWR RW operation clears the SAGC-count of the MTU.

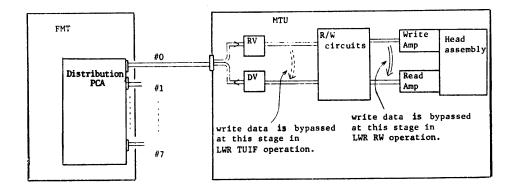


Figure D-34. LWR and LWR2.

D3043 LWR RW Execution

Perform LWR RW execution as fcllows:

- (1) Refer to Part I of this Maintenance Manual for information on the field tester, if necessary.
- (2) Store the MTU address and byte count to OFLDVA, BCT register. See procedures (8) (9) in D3040.

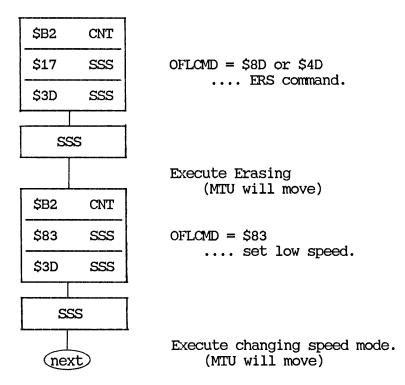
$$OFLDVA = dd$$

 $BCT = bb$

(3) Store the offline execution parameter to OFLCNT register. Here, parameter is all '0' (single command execution).

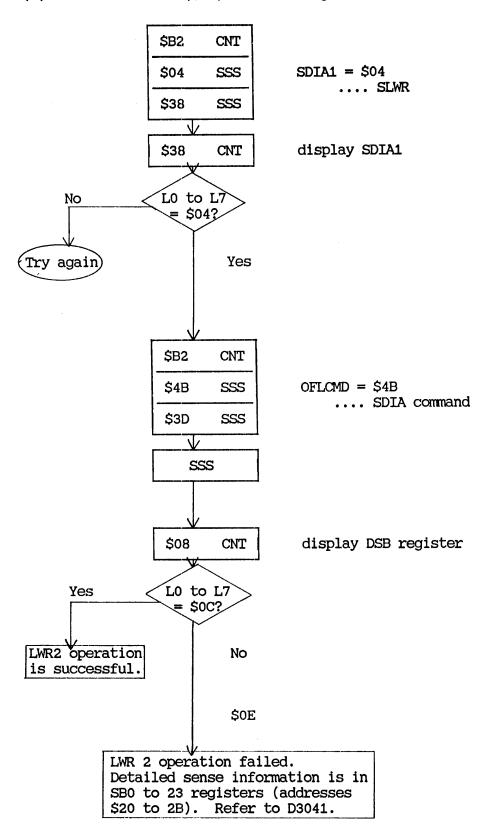
$$OFLCNT = 00$$

- (4) To allow the MTU to move forward if the MTU is in the BOT detected status, issue WRT, WIM, or ERS command to the MTU.
- (5) If a specific tape speed is to be tested set either the high-speed or low-speed command.
- (6) If the MTU is in the BOT detected status, set density-select bit ('0' or '1').

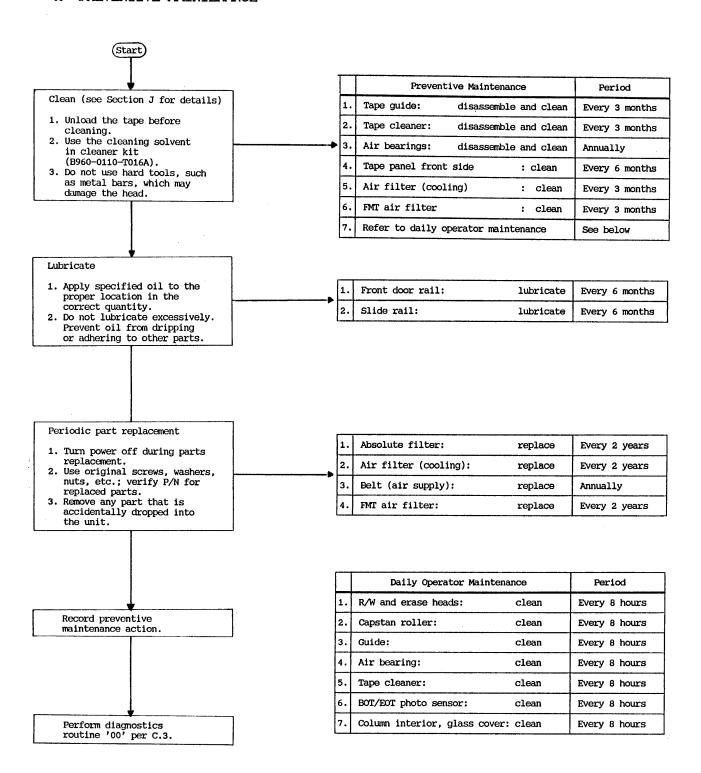


(continued on next page)

(7) Store SLWR bit (\$04) to SDIA1 register. Issue SDIA1 command.



H PREVENTIVE MAINTENANCE



Note: Air filters should be cleaned or replaced every 3 months, and must be replaced every 2 years. See replacement schedule in Section L.

J CLEANING

J.1 INTRODUCTION

This section contains instructions for MTU cleaning. Use the cleaning agent (solvent) that is supplied with the cleaner kit (B960-0110-T016A). In general, never apply rough or abrasive material or hard tools, such as metal bars, when cleaning MTU components. Clean the surfaces shown in Figure J-1 and listed below with a gauze cloth soaked in solvent.

J.2 READ/WRITE AND ERASE HEADS

Clean Read/Write and Erase heads every 8 hours as follows:

- (1) Open the front door of the MTU.
- (2) Lift up auto cleaner to access the lower part of read/write head.
- (3) Use a circular motion while applying a gauze cloth soaked in solvent to the heads.
- (4) Inspect the heads after cleaning.
- (5) Remove adhering gauze thread with a cotton swab or clean cloth.

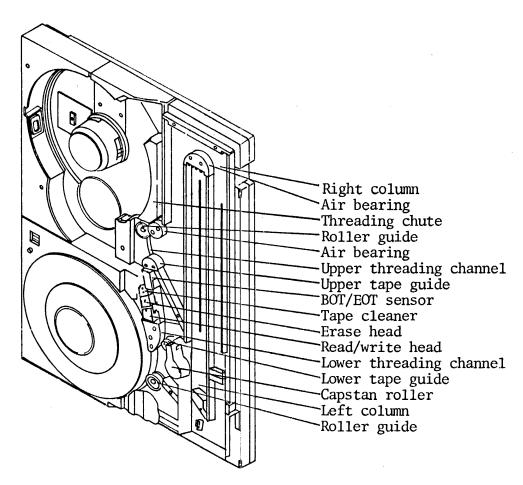


Figure J-1. MTU components requiring cleaning.

J CLEANING

J.3 CAPSTAN ROLLER

Clean the capstan roller every 8 hours as follows:

- (1) Wear clean gloves or cover hands with a gauze cloth. Do not touch the capstan surface with uncovered hands.
- Manually turn the capstan and clean carefully with a gauze cloth soaked in solvent.
- (3) Inspect the capstan for gauze threads and remove with a clean cloth.

J.4 TAPE CLEANER

Clean the edges of the tape cleaner every 8 hours with a cotton swab or gauze soaked in solvent.

J.5 OTHER MTU COMPONENTS SHOWN IN FIGURE J-1.

Clean each of the following items every 8 hours with a gauze cloth or cotton swab containing solvent. To remove dirt from more inaccessible locations, use a brush dipped in solvent. After brushing, apply a gauze cloth or cotton swab soaked in solvent to these surfaces.

- Tape guide (upper and lower) (1)
- (2) Air bearing (see two locations in Figure J-1)
- (3) Threading chute
- (4) Roller guide
- (5) Upper threading channel
- (6) Lower threading channel
- (7) Column interior
- (8) Glass cover
- (9) Photo sensor (beginning of tape and end of tape sensor).

J.6 TAPE GUIDES

The upper and lower tape guides should be removed, disassembled, and cleaned with a cotton swab, gauze cloth, or brush every 3 months.

- (1) Refer to L0070 for removal and replacement of the tape guides.
- (2) Clean all surfaces with the cleaning solvent.
- (3) Ensure that the upper guide air-outlet hole is free of dust.(4) Clean the panel surfaces on which the guides are mounted.
- (5) Inspect the guides and flanges for damage or wear.
- (6) Replace any damaged components.
- (7) Reinstall the upper and lower tape guides.

J CLEANING

J.7 AIR BEARINGS

The two air bearings shown in Figure L-1 should be removed and cleaned with a cotton swab, gauze cloth, or brush every 12 months.

- (1) Unscrew each of the air bearings and remove from the panel.
- (2) Clean all surfaces.
- (3) Ensure that the air outlet holes in each bearing is free of dust.
- (4) Clean the panel surfaces on which the air bearings are mounted.
- (5) Reattach the two air bearings.

J.8 TAPE CLEANER

The tape cleaner should be removed (see L 0050) and thoroughly cleaned every 3 months with a cotton swab, gauze, or brush soaked in cleaning solvent. Clean the mounting base and replace the tape cleaner.

J.9 BOT/EOT LOW TAPE SENSORS

- (1) Refer to L0060 and L0250 for removal and replacement procedures.
- (2) Clean all surfaces every 8 hours with a brush soaked in cleaning solvent.

J.10 MACHINE REEL, PANEL SURFACES, AND GLASS DOORS

Clean all external and internal surfaces every 6 months with a gauze cloth soaked in cleaning solvent. Vacuum the mechanism from the rear of the MTU.

J.11 AIR FILTERS

- (1) Remove air filters every 3 months (see L0370 and L0380).
- (2) Clean the air filters with a vacuum cleaner.
- (3) Replace air filters every 2 years.

K0000 CHECK AND ADJUSTMENT PROCEDURES

Follow these general procedures during checks and adjustments:

- (1) Adjust the oscilloscope before measurement, if the procedure requires such equipment.
- (2) Unless otherwise noted, adjust readings, such as voltage or pressure levels, to the mid-value of a specified range.
 (3) Record the data during both checks and adjustments.
- (4) Handle the master skew tape carefully. Always remove the writeenable ring during check and adjustment. Operation requires file protection.

FMT Check and adjustment items	Map No.	Period
Power supply voltage	K0001	Annually
Variable frequency oscillator (VFO) free-running frequency (6250,1600 rpi)	К0002	Every 6 months

MTU Check and adjustment items	Map No.	Period
Power supply voltage	K0100	Annually
Clock pulse check	K0101	Annually
Capstan tachometer output	K0110	Every 3 months
Azimuth	K0120	Every 6 months
Read signal level (6250/1600 rpi MTU)	K0130	Every 6 months
Read signal level (1600/800 rpi MTU)	K0140	Every 6 months
Read and write skew (1600/800 rpi MTU)	K0150	When necessary
Write voltage	K0160	Annually
Erase effect	K0170	When necessary
Hose and tube	K0180	When necessary
Pressure and vacuum level	K0190	When necessary
Vacuum blower and motor pulleys	K0191	When necessary
Air supply unit belt tension	K0200	When necessary
BOT/EOT detection circuit	K0210	Annually
Low tape detection circuit	К0220	Annually
Tape loop position detection circuit	K0240	Annually
File protect mechanism	K0260	Every 6 months
Front door synchronous belt tension	K0280	When necessary
Autocleaner	K0290	When necessary

K0001 CHECK AND ADJUSTMENT PROCEDURES

FMT Power Supply Voltage Check and Adjustment

(1) Use a digital voltmeter to check and adjust the following DC voltage levels on FMT #0 for a single FMT system.

Voltage	Range	
+5 V	+4.75 to +5.25 V. Adjust the +5 V ADJ on the power supply unit as required.	
-5.2 V	-5.46 to -4.94 V. Adjust the -5.2V ADJ on the Power supply unit as required.	

(2) Check FMT #1 for a dual FMT system. Adjust DC voltage levels, if necessary, to the same range as that for FMT #0.

K0002 CHECK AND ADJUSTMENT PROCEDURES

FMT Variable Frequency Oscillator (VFO) Free-Running Frequency Check

Follow these steps for VFO free-running frequency check (6250 rpi, 1600 rpi).

- (1) Connect the field tester to the FMT (see Part I on the field tester) and set the ONL/OFL switch to OFL.
- (2) Set the tape speed and density of the FMT as follows:
 - a. Field tester tape speed set-up
 - (1) \$B2 and then toggle CNT.
 - (2) Set switches 5 through 7 per table below. (Set all other switches to 0.) Toggle SSS.
 - (3) \$74 and then toggle SSS.

FMT model	Tape speed (ips)	Field te	ester s	switches 7
M2434L	75	0	1	0
110110	125	1	0	1
M2435L	125	1	0	0
	200	1	1	1

b. Field tester density set-up

- (1) \$B2 and then toggle CNT.
- (2) Set switches 4 and 5 per table below. (Set all other switches to 0.) Toggle SSS.
- (3) \$64 and then toggle SSS.

Density (rpi)	Field test	ter switches 5
6250	1	0
1600	0	1

K0002 CHECK AND ADJUSTMENT PROCEDURES

(3) Clamp the following back-panel pins located on PCA 1A04 to ground. Measure the oscillation frequency of VFO.

Bit	0 V clamp point		Measurement point	
0 1 2 3 4 5 6 7 8	 AK4 	AB8 AE2 AE5 AG1 AHX AKX BA5 BE3 BEV	AA9 AAY ADX AH3 AL1 BB2 BA3 BD4 BDU	AA6 ABX AD8 AEX AGX AL8 BB7 BAV BEU

(4) Measure the oscillation frequency of VFO.

Recording density	Tape speed (ips)	Allowable range (<u>+</u> 15%)
	200	1.80 MHz
6250 rpi	125	1.13 MHz
	75	678 kHz
	200	320 kHz
1600 rpi	125	200 kHz
	75	120 kHz

(5) Remove the ground clamps.

K0100 CHECK AND ADJUSTMENT PROCEDURES

MTU Power Supply Unit Check and Adjustment

Check and adjust the following items on the MTU with a digital voltmeter. Check and adjustment points are shown in Figures K-1 through K-3.

Voltage	Location	Range	Adjustment position
+ 5 V	MTU logic gate + 5 V AK1 PCA 1A02 GND AK2	+ 5V <u>+</u> 2%	Potentiometer RV1
+12 V	Write/read PCA CHWR pin 1	+12V <u>+</u> 8%	
- 6 V	Write/read PCA CHWR pin 5	- 6V <u>+</u> 8%	
<u>+</u> 13 V	MTU logic gate +13 V ADV PCA 1A01 -13 V AEV	<u>+</u> 13V <u>+</u> 8%	

Follow these steps when replacing PCA 1A02:

- (1) Check the +24 V across points 6 and 7 (GND), the -24 V across points 8 and 7 (GND), and the +11 V across points 4 and 5 (GND) shown in Figure K-3 (TRM 41).
- (2) Adjust variable resistor RV1 on PCA 1A02 to satisfy that the voltage across +5 V check point and GND is 5 V \pm 2%.
- (3) Check the + 5 V and confirm +12 V, -6 V, and \pm 13 V are within allowable ranges in the Table above.
- (4) If the requirements of +24 V and +11 V are not satisfied, replace the power supply unit.
- (5) If the requirements of +5 V, +12 V, -6 V and \pm 13 V are not satisfied, replace PCA 1A02.

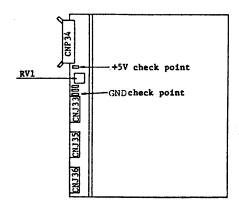


Figure K-1. PCA 1A02 in the MTU.

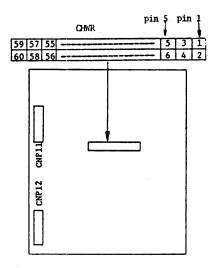


Figure K-2. Write/read amplifier PCA.

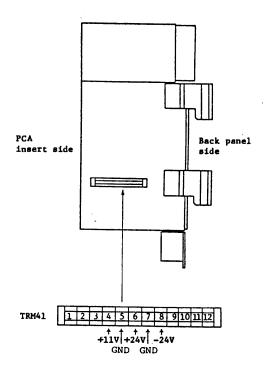


Figure K-3. ± 24 V and +11 V check points.

K0101 CHECK AND ADJUSTMENT PROCEDURES

Clock Pulse Check

Check the following clock pulses with an oscilloscope.

Clock pulses (see below)	Check point (MTU logic gate)	Allowable range
CL8M	1A06 BB8	$T_0 = 125 \text{ ns } \pm 1.5\%$ Duty $(Tw_0/T_0) = 50 \pm 15\%$
CL1MA	1A06 BAX	$T_1 = 1 \mu s + 1.5$ %
DSPCL	1A05 ALV	$T_2 = 500 \text{ ns} + 50 \text{ ns}$
PTYCL	1A06 BBX	$T_3 = 750 \text{ ns} + 50 \text{ ns}$
		Tw_1 , Tw_2 , Tw_3 = 62.5 ns \pm 20 ns

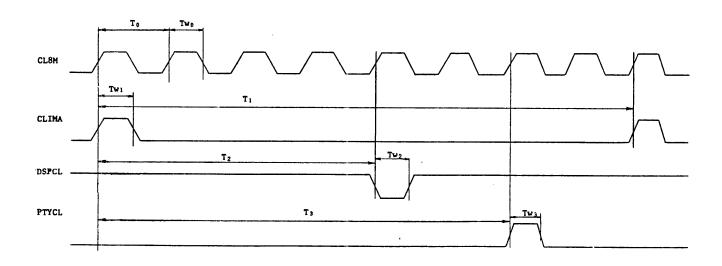


Figure K-4. Clock pulses.

K0110 CHECK AND ADJUSTMENT PROCEDURES

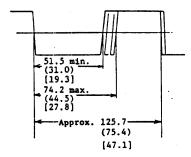
Capstan Tachometer Output Check

I. Duty Cycle Check

- (1) Connect a field tester to the MTU at 1C05 and load a magnetic tape.
- (2) Use an oscilloscope to observe CPA and CPB during forward (Command code \$01) and backward (command code \$41) directions.
- (3) Check that both directions of motion satisfy the requirements shown in Figure K-5.

Capstan tachometer	Measurement location MTU logic gate motherboard	Requirement	
CPA CPB	1A01 AA6 1A01 AB6	Shown in Fig. K-5	

(4) If the requirements as shown on Figure K-5 are not correct, see paragraph III for adjusting the duty cycle.



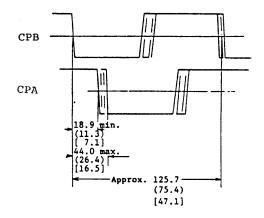
Notes:

- (1) All values are in microseconds (us)
- (2) Values designated by () are for 125 ips model. Values designated by □ ☐ are for 200 ips model.

Figure K-5.

II. Phase Check

- A. Measurement running in forward direction (field tester command code \$01). Toggle the SSS switch to start motion and toggle the SSS switch again to stop motion.
 - (1) Run the tape in the forward direction.
 - (2) Observe CPA and CPB simultaneously.
 - (3) Check that the requirements shown in Figure K-6 are satisfied when triggered by trailing edge of the pulse CPB.
- B. Measurement running in backward direction (field tester command code \$41).
 - (1) Run the tape in the backward direction.
 - (2) Measure at the same terminals as in forward running, except reverse the oscilloscope leads.
 - (3) Check that the measured values satisfy the requirements shown in Figure K-6.



Notes:

- (1) All values are in microseconds (μs)
 (2) Values designated by () are for 125 ips model.
 Values designated by □ □ are for 200 ips model.

Figure K-6.

K0110 CHECK AND ADJUSTMENT PROCEDURES

Capstan Tachometer Output Check

III. Capstan High-Speed Rotation Check

- (1) Remove the magnetic tape.
- (2) Connect the field tester to the MTU at connector 1C05. Set switches 0 through 7 to \$9D and toggle the SSS switch. The capstan motor will rotate at high speed. Check the tachometer CPA and CPB.
- (3) If an error occurs, unit check LED is illuminated and error code is displayed. In this case, the capstan motor rotates at an unstable speed.
- (4) If the capstan pulse CPA or CPB does not satisfy the requirements, adjust the potentiometer that corresponds to CPA or CPB at the capstan motor. (See Figure K-7.) However, never adjust the potentiometer unless the tests indicate a need to do so.

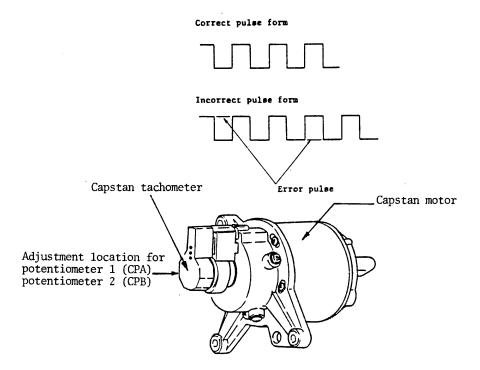


Figure K-7.

K0120-1 CHECK AND ADJUSTMENT PROCEDURES

Azimuth Check

- (1) Press the UNLOAD/REWIND button on the MTU front panel and remove the tape from the reel.
- (2) Demagnetize the read/write (R/W) head with the head eraser (P/N CT-HE-3-AC117 V-60 Hz-Sony).
- (3) Install master skew tape (P/N BM.BvMt 351d) and press LOAD/REWIND on the MTU control panel.
- (4) Connect a dual-trace oscilloscope to the Write/Read amplifier PCA, tracks 1 and 9, as shown in Figure K-8. The designations on the write/read amplifier PCA for tracks 1 through 9 are shown in Figure K-9. Five pins are associated with each track on the PCA. Connect the oscilloscope to pin #5.

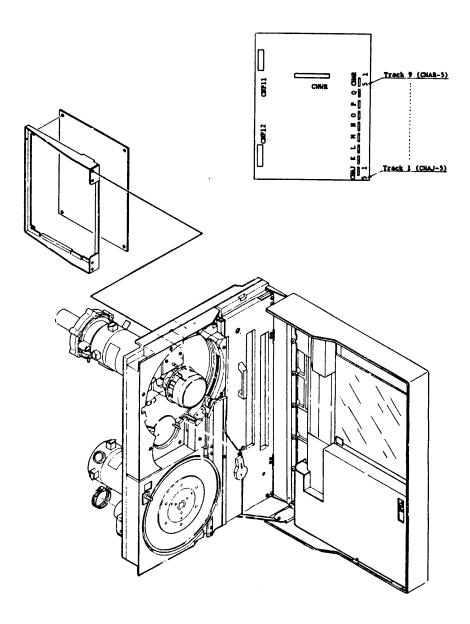


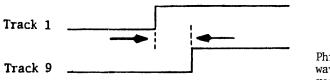
Figure K-8. Read/write amplifier PCA.

K0120-1 CHECK AND ADJUSTMENT PROCEDURES

(5) Set the field tester ONL/OFL switch to OFL. Set the field tester switches S0 through S7 to \$E2 for 6250/1600 rpi; (or) Set the field tester switches to \$E0 for 1600/800 rpi. After setting the switches, toggle the SSS switch.

(6) Use Phase Encode (PE) mode, and set the field tester switches for forward (FWD) read using command code \$01. Toggle the SSS switch.

(7) Check that the phase difference with the read output of tracks 1 and 9 shown in Figure K-9 satisfies the requirements of FWD skew in the table.



Phrase difference between rising waveforms (µs) should meet skew requirements in next table.

Track Number	Designation on write/read amplifier PCA
1	CHAJ
2	CHAK
3	CHAL
4	CHAM
5	CHAN
6	CHAO
7	CHAP
8	CHAO
9	CHAR

Figure K-9. Phase difference of tracks 1 and 9.

K0120-1 CHECK AND ADJUSTMENT PROCEDURES

FWD and BWD skew requirements. To use this table, verify model number of unit to be tested. Use skew requirement for FWD and BWD directions (shown in right-hand column) for that model.

Model Number	Specification	Check between	Requirement: skew must be within
M2435L1/L2 M2432L	125 ips 6250/1600 bpi (WRHMU)	Track 1 versus 2 thru 9	FWD 0.6 us BWD 1.0 us
M2434L1/L2 M2430L	75 ips 6250/1600 bpi (WRIMU)	Track 1 versus 2 thru 9	FWD 1.0 \(\triangle s \) BWD 1.6 \(\triangle s \)
M2433L	125 ips 1600/800 bpi (WRJMU)	Track 1 versus 2 thru 9	FWD 0.4 AS BWD 0.4 AS
M2431L	75 ips 1600/800 bpi (WRKMU)	Track 1 versus 2 thru 9	FWD 0.7 \(\text{\sigma} \) S BWD 0.7 \(\text{\sigma} \) S
M2436L1/L2 & L8	200 ips 6250/1600 bpi (WRHMU)	Track 1 versus 2 thru 9	FWD 0.4 Ms BWD 0.6 Ms

- (8) Check the FWD skew of tracks 2 through 8 against track 1. Verify that skew is within the values shown in the table.
- (9) Initiate the backward (BWD) operation by setting field tester switches to \$41.
- (10) Verify that skew is within the values shown in the table for BWD operation. Check the BWD skew of tracks 2 through 9 against track 1.
- (11) If either FWD or BWD operations do not satisfy the requirements in the table, adjust the azimuth according to instructions in the K0120-2.

K0120-2 CHECK AND ADJUSTMENT PROCEDURES

Azimuth Adjustment

- (1) Perform the dynamic alignment procedures in L0130-2.
- (2) Connect an oscilloscope to tracks 1 and 9 as described in K0120-1 and observe the phase difference in the rising waveforms. Use track 1 as the trigger. Adjust the phase of the two waveforms using the azimuth adjusting screw (A) (Figure K-10) until the requirements listed in the table (K0120-1) are met.
- (3) Checkthat tracks 2 through 8 (compared to track 1) meet the same requirements.
- (4) Observe backward (BWD) operation. If the requirements in the table in K0120-1 are satisfied, no adjustment is needed.
- (5) If the requirements are not satisfied (6250/1600 rpi MTU), turn the upper capstan alignment adjusting screw until the backward skew is correct. If track 9 leads track 1, turn the screw counterclockwise. If track 1 leads track 9, turn the screw clockwise.
 - Note: Rotation of the azimuth adjusting screw must not exceed 1/4 turn.
- (6) If any adjustments are made, recheck the forward and backward skew.

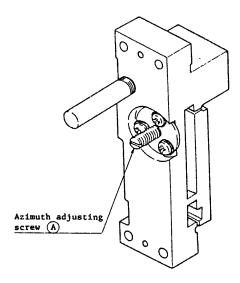


Figure K-10. Head block (rear of the MTU).

K0130 CHECK AND ADJUSTMENT PROCEDURES

Read Signal Check and Adjustment, and Head Replacement Specification (6250/1600 rpi MTU)

This section provides instructions for checking and adjusting the readsignal levels for the following modes:

- Low-speed phase encode
- High-speed phase encode
- Low-speed group code recording (GCR)
- High-speed GCR.

Ensure that the conditions listed below have been satisfied before initiating read-signal checkout:

- (1) Clean the read/write and erase heads.
- (2) Install an SRM3200 tape or a tape of equivalent quality. Push the LOAD/REWIND button on the MTU front panel.
- (3) Verify that the column vacuum level is adjusted to specifications. (See K0190.)
- (4) Ensure that capstan alignment is normal. (See L0130.)

If any adjustments in the following procedures cannot be performed, or if criteria cannot be satisfied, replace the head and perform checks I through IV. See L0010 for head replacement. If adjustments fail after head replacement, see A7000.

I. Low-Speed Phase Encode Checkout

- (1) Set field tester switches S0 through S7 to \$1E, and toggle the CNT switch to select the register address.
- (2) Set the field tester switches SO through S7 to \$EA, and toggle the SSS switch to set the read mode, tape speed, and density. (For models M2431L and M2433L, use \$E8 setting.)
- (3) Set the field tester switches S0 through S7 to \$FA, and toggle the SSS switch to set the slice level to 100%.
- (4) Set the field tester switches SO through S7 to \$89, and toggle the SSS switch to set the write, low-speed, phase encode mode. Lamps O through 8 will come on and should be semi-luminous (barely glowing).
- (5) Adjust the corresponding potentiometers (RV1R through RV1J) in Figure K-11, if necessary, to obtain semi-luminous status for lamps 0 through 8. Toggle the SSS switch to stop the tape.
- (6) Set the field tester switches S0 through S7 to \$F9, and toggle the SSS switch to set the slice level to 90%.
- (7) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch to set the write, low-speed, phase encode mode. Lamps 0 through 8 should be brightly lit.
- (8) Adjust the corresponding potentiometers shown in Figure K-11, if necessary. Toggle the SSS switch to stop the tape.
- (9) Set the field tester switches S0 through S7 to \$FB, and toggle the SSS switch to set the slice level to 110%.
- (10) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch. Lamps 0 through 8 should be off.

(11) Adjust the corresponding potentiometers shown in Figure K-11, if necessary. Toggle the SSS switch to stop the tape.

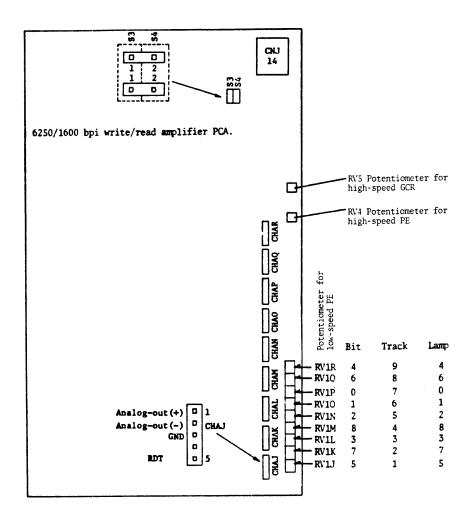


Figure K-11. Potentiometers and check terminals for lamps 0 through 8 on write/read amplifier PCA.

II. High-Speed Phase Encode Checkout

- (1) Set the field tester switches S0 through S7 to \$1E, and toggle the CNT switch to select the register address.
- (2) Set the field tester switches S0 through S7 to \$EC, and toggle the SSS switch to set the tape to the high-speed mode.
- (3) Set the field tester switches S0 through S7 to \$FA, and toggle the SSS switch to set the slice level to 100%.
- (4) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode.
- (5) Adjust potentiometer RV4 shown in Figure K-11 so that four or more of lamps 0 through 8 are lit. After adjustment, toggle the SSS switch to stop the tape.

K0130 CHECK AND ADJUSTMENT PROCEDURES

- (6) Set the field tester switches S0 through S7 to \$F5, and toggle the SSS switch to set the slice level to 80%.
- (7) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode. Lamps 0 through 8 should be lit.
- (8) Adjust potentiometer RV4 if necessary. Toggle the SSS switch to stop the tape.
- (9) Set the field tester switches S0 through S7 to \$F7, and toggle the SSS switch to set the slice level to 125%.
- (10) Set the field tester switches SO through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode. Lamps 0 through 8 should be off.
- (11) Adjust potentiometer RV4 if necessary. Toggle the SSS switch to stop the tape.

III. Low-Speed GCR Checkout

- (1) Set the field tester switches SO through S7 to \$1E, and toggle the CNT switch to set the register address.
- (2) Set the field tester switches SO through S7 to \$EA, and toggle the SSS switch to set the tape to the low-speed mode.
- (3) Set the field tester switches S0 through S7 to \$F3, and toggle the SSS switch to set the slice level to 51%.
- (4) Set the field tester switches SO through S7 to \$C6, and toggle the SSS switch to set the DGC amplifier. Toggle the SSS switch again to stop the tape.
- (5) Set the field tester switches SO through S7 to \$8B, and toggle the SSS switch for write, low-speed GCR mode. Lamps O through 8 should be on.
- (6) Toggle the SSS switch to stop the mode.
- (7) Set the field tester switches S0 through S7 to \$F5, and toggle the SSS switch to set the slice level to 80%.
- (8) Set the field tester switches SO through S7 to \$8F, and toggle the SSS switch to perform SAGC operation in write, low-speed, GCR mode. Lamps O through 8 should be on.
- (9) Toggle the SSS switch.
- (10) Set the field tester switches S0 through S7 to \$F7, and toggle the SSS switch to set the slice level to 125%.
- (11) Set the field tester switches SO through S7 to \$8B, and toggle the SSS switch for write, low-speed, GCR mode. Lamps O through 8 should be off.
- (12) Toggle the SSS switch.
- (13) Set the field tester switches S0 through S7 to \$F3, and toggle the SSS switch to set the slice level to 51%.
- (14) Set the field tester switches SO through S7 to \$41, and toggle the SSS switch for read backward in the low-speed, GCR mode. Lamps O through 8 should be on.
- (15) Toggle the SSS switch.

IV. High-Speed GCR Checkout

(1) Set the field tester switches S0 through S7 to \$1E, and toggle the CNT switch to set the register address.

K0130 CHECK AND ADJUSTMENT PROCEDURES

- (2) Set the field tester switches S0 through S7 to \$EA, and toggle the SSS switch to set the tape to the low-speed mode.
- (3) Set the field tester switches SO through S7 to \$8F, and toggle the SSS switch for write, low-speed GCR mode. After a few seconds, toggle the SSS switch again to stop the tape.
- (4) Set the field tester switches SO through S7 to \$EE, and toggle the SSS switch to set the tape to high-speed mode.
- (5) Set the field tester switches SO through S7 to \$FA, and toggle the SSS switch to set the slice level to 100%.
- (6) Set the field tester switches S0 through S7 to \$8B, and toggle the SSS switch for write, high-speed GCR mode.
- (7) Adjust potentiometer RV5 in Figure K-11 so that four or more of lamps 0 through 8 are on. Toggle the SSS switch after adjustment to stop the tape.
- (8) Set the field tester switches S0 through S7 to \$F4, and toggle the SSS switch to set the slice level to 64%.
- (9) Set the field tester switches SO through S7 to \$8B, and toggle the SSS switch for write, high-speed, GCR mode. Lamps O through 8 should be lit.
- (10) Adjust potentiometer RV5, if necessary, so that lamps 0 through 8 are lit. Toggle the SSS switch to stop the tape.
- (11) Set the field tester switches S0 through S7 to \$F7, and toggle the SSS switch to set the slice level to 125%.
- (12) Set the field tester switches S0 through S7 to \$8B, and toggle the SSS switch for write, high-speed, GCR mode. Lamps 0 through 8 should be off.
- (13) Adjust potentiometer RV5, if necessary, so that lamps 0 through 8 are off, and then toggle the SSS switch to stop the tape.
- (14) Set the field tester switches S0 through S7 to \$F3, and toggle the SSS switch to set the slice level to 51%.
- (15) Set the field tester switches S0 through S7 to \$42, and toggle the SSS switch to read backward, high-speed, GCR mode. Lamps 0 through 8 should be off.
- (16) Adjust potentiometer RV5, if necessary, until lamps 0 through 8 are off.
- (17) When read-signal checks and adjustment are completed, toggle the SSS switch to terminate the test.
- (18) Press the LOAD/REWIND button on MTU front panel to rewind the tape.

K0140 CHECK AND ADJUSTMENT PROCEDURES

Read Signal Check and Adjustment, and Head Replacement Specification (1600/800 rpi MTU)

This section provides instructions for checking and adjusting the readsignal levels for the following modes:

- Nonreturn to zero I (NRZI)
- Low-speed phase encode
- High-speed phase encode.

Ensure that the conditions listed below have been satisfied before initiating read-signal checkout:

- (1) Clean the read/write and erase heads.
- (2) Install an SRM3200 tape or a tape of equivalent quality. Push the LOAD/REWIND button on the MTU front panel.
- (3) Verify that the column vacuum level is adjusted to specifications. (See K0190.)
- (4) Ensure that capstan alignment is normal. (See L0130.)

If adjustments in the following procedures cannot be performed, replace the head with a new one. See L0010 for head replacement.

I. NRZI Check and Adjustment

- (1) Set field tester switches S0 through S7 to \$81, and toggle the SSS switch for write 800 fci in the NRZI mode.
- (2) Adjust potentiometers RV1J through RV1R, shown in Figure K-12, so that terminals CHAJ pin 1 through CHAR pin 1 develop 2.0 Vp-p + 10% against ground. Use an oscilloscope for these checks.

II. Low-Speed Phase Encode Checkout

- (1) Set field tester switches S0 through S7 to \$1E, and toggle the CNT switch to select the register address.
- (2) Set the field tester switches S0 through S7 to \$EA, and toggle the SSS switch to set the tape to low speed mode.
- (3) Set the field tester switches S0 through S7 to \$FA, and toggle the SSS switch to set the slice level to 100%.
- (4) Set the field tester switches SO through S7 to \$89, and toggle the SSS switch to set the write, low-speed, phase encode mode. Four or more lamps should come on.
- (5) If necessary, adjust potentiometer RV1. Toggle the SSS switch to stop the tape.
- (6) Set the field tester switches S0 through S7 to \$F5, and toggle the SSS switch to set the slice level to 80%.
- (7) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch to set the write, low-speed, phase encode mode. Lamps 0 through 8 should be brightly lit.
- (8) Toggle the SSS switch to stop the tape.
- (9) Set the field tester switches S0 through S7 to \$F7, and toggle the SSS switch to set the slice level to 125%.

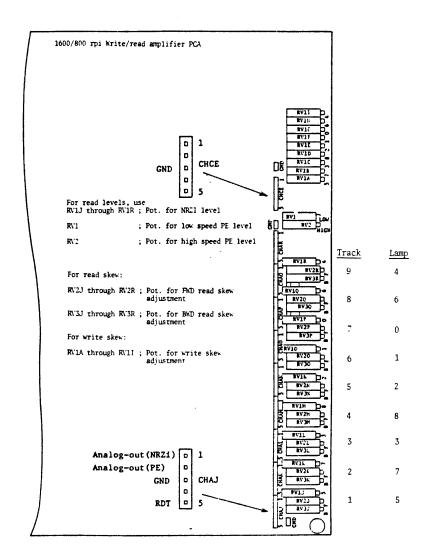


Figure K-12. Potentiometer and check terminals for lamps 0 through 8 on the 1600/800 rpi write/read amplifier PCA.

- (10) Set the field tester switches SO through S7 to \$89, and toggle the SSS switch. Lamps O through 8 should be off.
- (11) Toggle the SSS switch to stop the tape.

III. High-Speed Phase Encode Checkout

- (1) Set the field tester switches S0 through S7 to \$1E, and toggle the CNT switch to select the register address.
- (2) Set the field tester switches S0 through S7 to \$EC, and toggle the SSS switch to set the tape to the high-speed mode.
- (3) Set the field tester switches S0 through S7 to \$FA, and toggle the SSS switch to set the slice level to 100%.
- (4) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode.

K0140 CHECK AND ADJUSTMENT PROCEDURES

- (5) Adjust potentiometer RV2 shown in Figure K-12 so that four or more of lamps 0 through 8 are lit. After adjustment, toggle the SSS switch to stop the tape.
- (6) Set the field tester switches S0 through S7 to \$F5, and toggle the SSS switch to set the slice level to 80%.
- (7) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode. Lamps 0 through 8 should be lit.
- (8) Toggle the SSS switch to stop the tape.
- (9) Set the field tester switches SO through S7 to \$F7, and toggle the SSS switch to set the slice level to 125%.
- (10) Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch for write, high-speed, phase encode mode. Lamps 0 through 8 should be off.
- (11) Toggle the SSS switch to stop the tape.

K0150 CHECK AND ADJUSTMENT PROCEDURES

Read and Write Skew Check and Adjustment (1600/800 rpi MTU)

- I. Check and adjust the read skew by taking the following steps:
 - (1) Degauss the magnetic and erasing heads with the demagnetizer (eraser) and clean the heads.
 - (2) Mount a field tester.
 - (3) Load a standard skew adjustment tape. Check that the FILE PROTECT lamp on the operator panel is ON.
 - (4) Run the tape forward or backward in the NRZI mode.

Operation of the field tester is as follows:

Table 1.

	Field tester			
Item	Code	Toggle Switch	Operation	Remarks
1	\$E0	SSS	Set to the NRZI mode	
2	\$01	SSS	Forward running	The tape stops running if a beginning of tape or an end
2	\$41	SSS	Backward running	of tape marker is detected.

(5) Check that the pulse width developed at check terminal CHAN pin 5, for track 5 meets the value shown below. Adjust the pulse width for the specified value with RV2N (forward running) and RV3N (backward running).

See Figure K-12 (K0140) for location of potentiometers and check terminals.

Table 2.

Speed	Checked/adjusted pulse width (tw)	Observed waveform for CHAN, pin 5	
75 ips (for 75/125 ips device)	3.0µs ± 10%	tw 2.4 to 5 V	
125 ips (for 125/200 ips device)	2.0 _M s <u>+</u> 10%	0 to 0.4 V	

- (6) Check that the rise times of pulses for the respective tracks meet the specifications in Table 3 for forward and backward running when the output levels of other tracks are observed. Use the output level of check terminal CHAN, pin 5 for track 5 as a reference.
- (7) Adjust the rise times with RV2J to RV2R (except RV2N; forward running) and RV3J to RV3R (except RV3N; backward running).

Table 3.

Speed	Running direction	Variable resistors	Check terminals	Specification (\Delta t) (see Figure K-13)	
75 inc	Forward	RV2J to RV2R (except RV2N)	CHAJ, pin 5	0.3 Ms or less	
75 ips	Backward	RV3J to RV3R (except RV3N)	to		
125 ips	Forward	RV2J to RV2R (except RV2N)	CHAR, pin 5	0.0 a en loga	
	Backward	RV3J to RV3R (except RV3N)	(except CHAN, pin 5)	0.2 _M s or less	

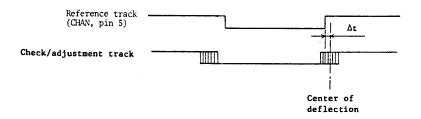


Figure K-13. At for check track vs. reference track (CHAN, pin 5).

K0150 CHECK AND ADJUSTMENT PROCEDURES

- II. Check and adjust the write skew by taking the following steps:
 - (1) Load a good quality tape (SRM 3200 or equivalent).

(2) Write 800 fci in the NRZI mode. Set the field tester switches S0 through S7 to \$89, and toggle the SSS switch.

(3) Observe the deskew clock pulse width for track 5 of the write circuit at check terminal CHCE, pin 1. Check that the clock pulse width meets the value shown in Table 4. Adjust the pulse width for the specified value with RV1E. See Figure K-12 (K0140) for locations of potentiometers and check terminals.

Table 4.

Speed	Adjusted pulse width (tw)	Observed waveform for CHCE, pin 1		
75 ips (for 75/125 ips device)	3.0 _/ s <u>+</u> 10%	tw 	2.4 to 5V	
125 ips (for 125/200 ips device)	2.0 _/ /s <u>+</u> 10%		0 to 0.4V	

- (4) Check that the rise times of pulses for the respective tracks meet the specifications in Table 5 when the output levels of other tracks are observed. Use the output level of check terminal CHAN, pin 5 for track 5 as a reference.
- (5) Adjust the rise time with RV1A to RV1I (except RV1E).

Table 5.

Speed	Variable resistor	Check terminal	Specification (∆t) (See Fig. K-13 for∆t)
75 ips (for 75/125 ips device)	RV1A to RV1I	CHAJ, pin 5 to	0.3 As or less
125 ips (for 125/200 ips device)	(except RV1E)	CHAR, pin 5 (except CHAN, pin 5)	0.2 As or less

K0160 CHECK AND ADJUSTMENT PROCEDURES

Check for Write Voltage

- (1) Connect a field tester and load a good quality tape (SRM 3200 or equivalent).
- (2) Set the field tester to the write mode (in phase encode mode), erase mode, or read mode, as shown in the table below.
- (3) Check for voltage at each check point shown in Figure K-14.

MTU type	Revision of PCA	Check point	Write mode		Erase mode	Read mode	
оуро			\$E9 (SSS) \$8B (SSS)	ECC (SSS) \$8B (SSS)	\$83	\$A2	
	All units	CHWR, pin 6	11.2 <u>+</u> 1 V		Max. +0.4 V	Max. +0.4 V	
6250/ 1600 rpi	WRHMU WRIMU (B)	CHWR, pin 8	5.6 <u>+</u> 0.4V		Mov. 40 4 V	Mov. 10 4 V	
	WRIMU (E)	olimit, pin o	5.2 <u>+</u> 0.4V	5.8 <u>+</u> 0.4V		Max. +0.4 V	
	All units	CHWR, pin 10	2.4 <u>+</u> 0.4V		2.4 ± 0.4 V	Max. +0.4 V	
1600/ 800	All units	CHWR, pin 6	10.5 <u>+</u> 1 V		Max. +0.4 V	Max. +0.4 V	
rpi	All units	CHWR, pin 10	2.4 <u>+</u> 0.4V		2.4 <u>+</u> 0.4 V	Max. +0.4 V	

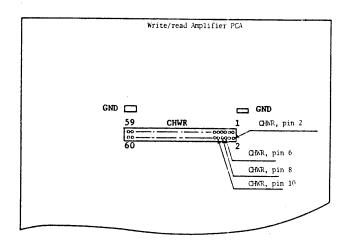


Figure K-14. Check points for write voltage on write/read PCA.

K0170 CHECK AND ADJUSTMENT PROCEDURES

Check for Erase Effect

- (1) Prepare a tape onto which all "1's" have been written in the 1600 phase encode mode.
- (2) Connect a field tester and load the tape.
- (3) Erase the tape content by issuing an erase command from the field tester (command code \$83).
- (4) Read the tape content, and check that the output levels at the respective check points meet the following specifications. Locations of check points are shown in Figure K-11 (see K0130 for 6250/1600 rpi MTU) and in Figure K-12 (see K0140 for 1600/800 rpi MTU).

MTU type (rpi)	Read mode (code)	Check points	Allowable range	
6250/1600	Phase encode (\$E0, \$01)	CHAJ, pin 1, to CHAR, pin 1	40 min_n	
1600/800	Phase encode (\$E2, \$01)	CHAJ, pin 2, to CHAR, pin 2	- 40 mVp-p maximum	

K0180 CHECK AND ADJUSTMENT PROCEDURES

Hose and Tube Check

- (1) Visually check to ensure that no cracks or abrupt bends, kinks, or other obvious problems exist on the hoses and tubes.
- (2) Check for loose connections of tubes (between the hoses and capacitive sensor) or disconnected tubes.

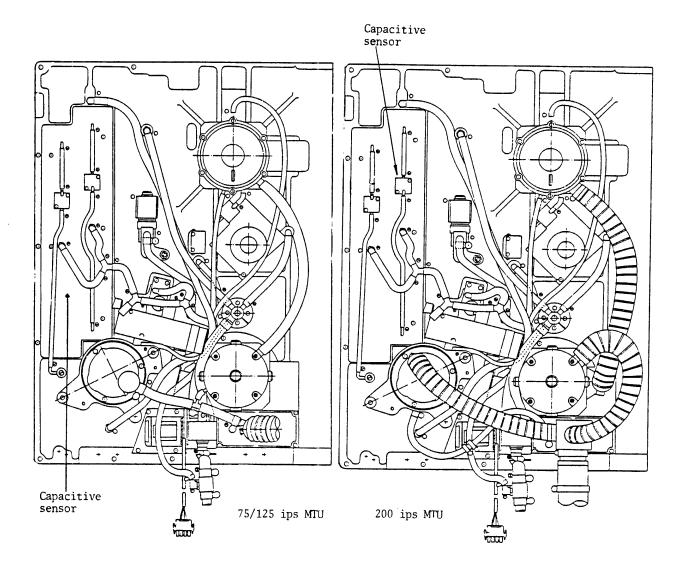


Figure K-15. Location of capacitive sensor.

K0190 CHECK AND ADJUSTMENT PROCEDURES

Check and Adjustment of Pressure and Vacuum Levels

Load an SRM3200 tape or a tape of equivalent quality as follows:

- (1) Install the reel of tape on the file (upper) reel.
- (2) Position the tape leader between the two white scribe marks on the upper restraint. (For a cartridge, omit this step.)
- (3) Close the door.
- (4) Press the LOAD/REWIND button on the MTU front panel.

The air system (pneumatics) will now come on, the window will close, and the file reel will rotate clockwise (CW) to feed the tape. Tape will load into columns, search forward, search backward, and stop at beginning of tape (BOT). If the 2-digit display on the MTU operator panel is other than 00, refer to the MTU error codes in Section A of this Maintenance Manual.

To allow for thermal stabilization, the pneumatics assembly must operate for at least 30 minutes before adjustment. Use pressure gauge B91L-0020-0001A and vacuum gauge BMz 198a for the following checks. Repeat the procedures in the following sequence for each MTU and whenever vacuum/pressure adjustment is made.

Column Vacuum

- (1) Remove the white nylon screw from the column vacuum measuring port shown in Figure K-16.
- (2) Connect the vacuum gauge to the column vacuum measuring port.
- (3) Refer to the pressure check level in the table below for column vacuum.
- (4) If necessary, adjust the vacuum restrictor so that vacuum pressure is within air pressure adjustment level listed.

Air pressure specifications.

Check point	Air pressure check levels (mm H ₂ O)	Air pressure adjustment levels (mm H ₂ O)	
Column vacuum	950 <u>+</u> 100	950 <u>+</u> 50	
Air bearing pressure	2600 <u>+</u> 100	2600 <u>+</u> 50	
Restraint pressure	450 <u>+</u> 50	450 <u>+</u> 20	

Air-Bearing Pressure

Air-bearing pressure check requires tape to be fully loaded into columns.

- (1) Ensure that field tester ONL/OFL switch is set to OFL. Set field tester switches S0 through S7 to \$01 and toggle the SSS switch.
- (2) Remove the white nylon fitting and connect the pressure gauge to the air-bearing measuring port.

- (3) Refer to the pressure check specification in the table above for air-bearing pressure.
- (4) If necessary, adjust the pressure-relief valve shown in Figure K-16 until the pressure is within the air bearing pressure adjustment level listed.

Restraint Pressure

- (1) Press the UNLOAD button on the MTU front panel.
- (2) When rewinding is complete, remove the tape from the file reel hub.
- (3) Mount the pressure-adjustment tool (B960-0110-T026A) on the air outlet of restraint member.
- (4) Connect pressure gauge (B91L-0020-0001A) to the restraint member pressure port E.
- (5) Set field tester switches to \$A5 and toggle the SSS switch.
- (6) Refer to the pressure check specification in the table.
- (7) If necessary, adjust the distributor screw until pressure is within restraint pressure adjustment specification.
- (8) Toggle the SSS switch on the field tester to turn the air system off.

 Rear view of MTU tape drive

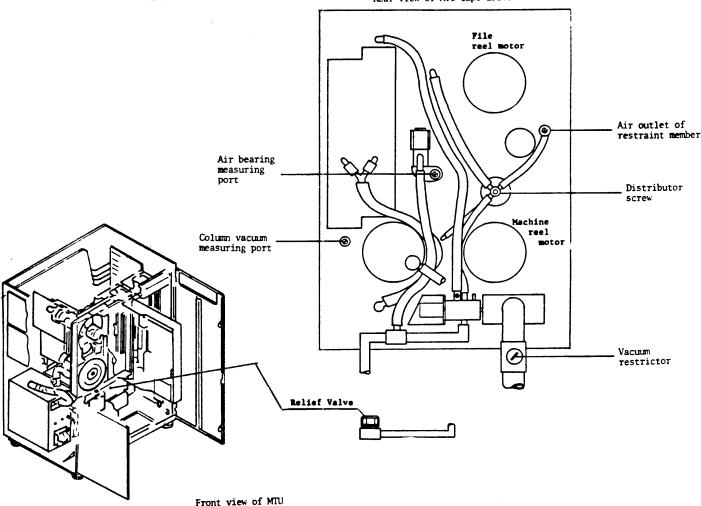


Figure K-16. Pressure check and adjustment points.

K0191 CHECK AND ADJUSTMENT PROCEDURES

I. Frequency Setting.

- (1) Confirm whether facility input frequency is 50 or 60 Hz.
- (2) Remove the cover of the air supply unit. This cover is located on the front of the MTU. The label on the cover specifies whether the unit is set for 50 or 60 Hz input.
- (3) For 60-Hz input, verify that CNP66 is connected to CNJ66B and that CNP66C is connected to CNJ66A. These connections are shown in Figure K-17.

For 50-Hz input, verify that CNP66 is connected to CNJ66A and that CNP66C is connected to CNJ66B. These connections are also shown in Figure K-17.

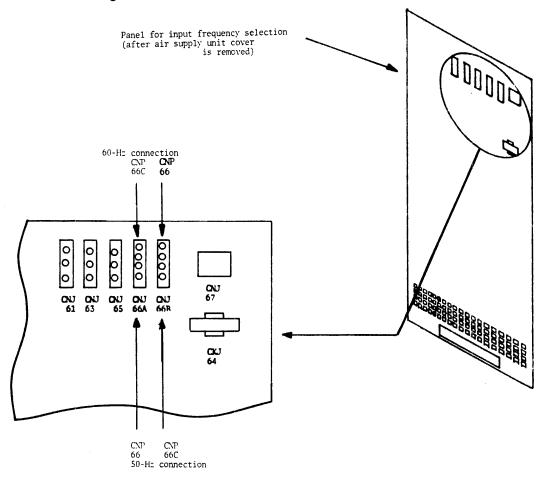


Figure K-17. Input power frequency setting.

II. Figure K-18 shows the location of pulleys for the vacuum blower and the air-pressure pump on the air supply unit. These pulleys are dependent on input-power frequency (50 or 60 Hz). The vacuum blower pulley is also dependent on altitude.

K0191 CHECK AND ADJUSTMENT PROCEDURES

Caution:

Do not remove or install belts by prying with shop tools. Use the adjustment screws on the air supply unit to loosen pulleys and belts. Use tension tool (B96L-0110-004A) to adjust belt tension.

A. Vacuum Blower Pulley

(1) Verify that the correct frequency-dependent pulley has been installed in accordance with Table 1. When delivered, the device is pre-set for either 50 Hz or 60 Hz input. For 50-Hz input, use P/N B30L-1940-0101A; for 60-Hz input, use P/N B30L-1940-0102A.

(2) Verify that the correct altitude-dependent pulley has been installed. If the unit operates at an altitude above 3000 feet, install the vacuum blower pulley in accordance with Figure K-19 and Table 1.

Table 6. Input-frequency and altitude adjustment.

Installation condition	Vacuum blower pulley	Motor pulley
50 Hz input frequency	Use P/N B30L-1940-0101A	Large-diam. pulley
60 Hz input frequency	Use P/N B30L-1940-0102A	Small-diam. pulley
Low altitude (<3000 ft)	Large-diam. pulley	No adjustment
High altitude (>3000 ft)	Small-diam. pulley	No adjustment

- (3) Remove the pulley, reverse its orientation, and reinstall.
- (4) Check and adjust belt tension (K0200).
- (5) Check and adjust pressure and vacuum levels (K0190).

B. Motor Pulley

The motor pulley driving the air pump can be oriented for operation at either 50 or 60 Hz, as shown in Figure K-19 and Table 1. If the MTU operates on 50 Hz, connect the belt to the large diameter pulley. If the MTU operates on 60 Hz, connect the belt to the small diameter pulley. Check and adjust belt tension (K0200) and pressure and vacuum levels (K0190).

(a) Rear view of slave unit

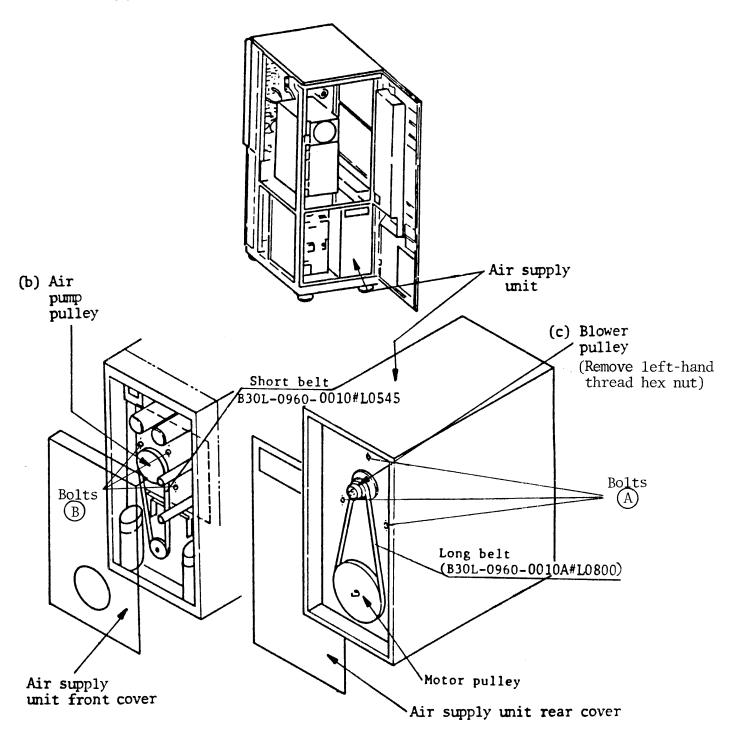


Figure K-18. Air supply unit: vacuum blower and motor pulleys.

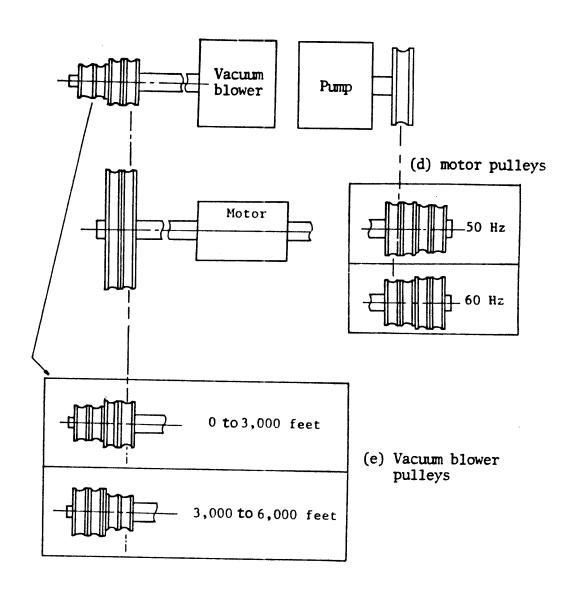


Figure K-19. Air supply unit: vacuum blower and motor pulleys.

Belt Tension Check and Adjustment

- (1) Remove the MTU air supply unit (L0400).
- (2) Remove the air supply unit front and rear covers and refer to Figure K-18 for location of belts.
- (3) Install the tension meter, as shown in Figure K-20. Turn the motor pulley 3 to 5 turns by hand before measuring the tension. Push up the lever with a finger as shown in Figure K-20. Snap the belt. Read the value in pounds when the belt hits the tension meter (at location "A").
- (4) Adjust the belt tension by positioning the vacuum blower or air pump.
 - If the belt is to be replaced, the new belt must be adjusted so that the tension levels in Table 1 are satisfied.
 - If the old belt is to be used again, measure the tension before removing it, and adjust the belt to that tension when reinstalling it. The direction of rotation of the belt must be the same when reinstalling it.

Table 1. Belt tension. (Refer to Note 1, below.)

Belt	Minimum	Adjusted value		
Beit	tension	New belt	Old belt	
Belt between motor and vacuum blower (longer belt)	16.5 lbs.	29 to 34 lbs.	Original tension (refer to Note 2)	
Belt between motor and air pump (shorter belt)	12.5 lbs.	29 to 34 lbs.	(Terer to Note 2)	

Notes:

- Belt tension rapidly deteriorates in several days or several months. Replace the belt if Table 1 requirements are not met.
- 2. If an old belt has been stretched, its life may be extremely short if its tension is adjusted to the value for a new belt. Replace old belt as soon as possible.

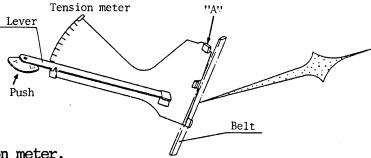


Figure K-20. Tension meter.

KO210 CHECK AND ADJUSTMENT PROCEDURES

Check and Adjustment of BOT and EOT Detection Circuits

(1) Obtain a magnetic tape and install two new reflective markers as shown in Figure K-21.

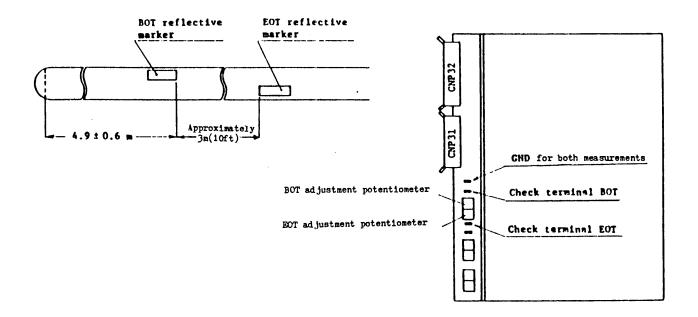


Figure K-21. Beginning of tape and end of tape reflective markers.

Figure K-22. MTU PCA 1A04

- (2) Before loading tape, check the voltage levels at terminals BOT/GND and EOT/GND (see Figure K-22) with a digital voltmeter.
- (3) If voltage is not +2.0 V, adjust potentiometers for BOT and EOT, respectively, on the MTU PCA 1A04.
- (4) Mount the tape and press LOAD/REWIND on the MTU front panel.
- (5) After the tape automatically stops at BOT, measure the voltage at the BOT terminal.
- (6) If the level is lower than +2.0 V, adjust the level to +2.0 V using BOT potentiometer.
- (7) Set the field tester switch to \$01.
- (8) Toggle the SSS switch to run the tape forward. Tape automatically stops at EOT.
- (9) Measure the voltage level at the BOT terminal and adjust voltage to lower than +0.3 V.
- (10) Measure the EOT level.
- (11) If EOT level is lower than +2.0 V, adjust the level to +2.0 V using potentiometer EOT.
- (12) Set the field tester switches to \$41.
- (13) After the tape automatically stops at BOT, check that the EOT level is lower than +0.3 V.
- (14) Repeat these steps for each MTU in the system.

K0220 CHECK AND ADJUSTMENT PROCEDURES

Check of Low Tape Detection Circuit

Check the low tape detection circuit as follows:

- (1) Unload the tape and connect the field tester to the MTU at 1006.
- (2) Set the field tester to machine reel FWD (command code \$02).(3) Check that the output voltage on the MTU logic gate motherboard (location AB8) is +1.4 Vp-p or more, as shown in Figure K-23.

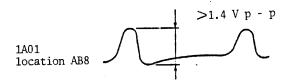


Figure K-23. Low tape output.

K0240 CHECK AND ADJUSTMENT PROCEDURES

Check and Adjustment of Tape Loop Position Detection Circuit

- (1) Wind tape on the machine reel.
- (2) If air pressure is not on, set field tester switches SO through S7 to \$A8 and toggle the SSS switch.
- (3) Manually adjust the tape inside the column to positions F0 and M0 shown in Figure K-24. (Hold the file reel in position by taping the reel to the column door.)

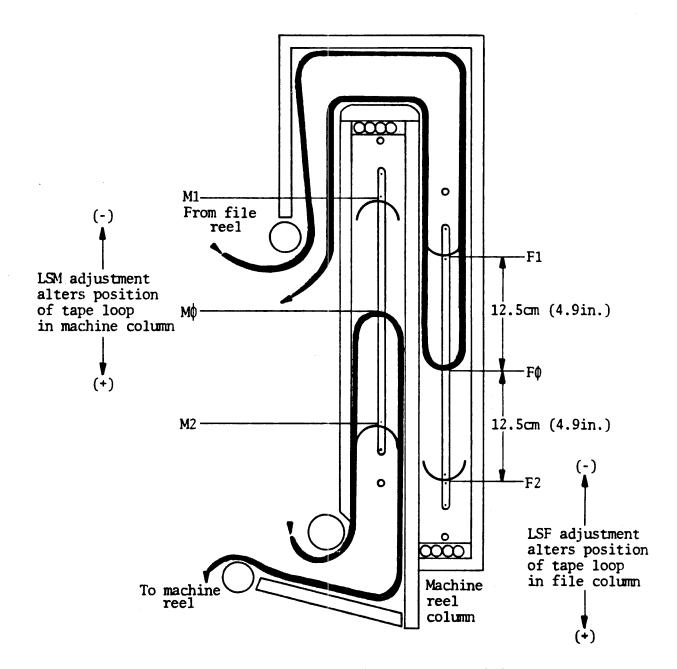


Figure K-24. Tape loop positions. Tape is shown at positions F0 and M0.

(4) Ensure that the column vacuum and the air-bearing pressure have been adjusted to 950 mm H2O \pm 100 and 2600 mm H2O \pm 100, respectively. (Refer to K0190.)

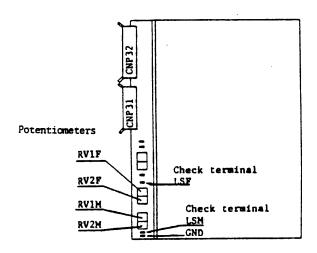


Figure K-25. MTU PCA 1A04.

- (5) Adjust potentiometers RV1F and RV1M shown in Figure K-25 so that the output voltage is 0 + 0.2 V.
- (6) Set the field tester switches to command code \$AA. Toggle the SSS switch to start the capstan moving forward. Toggle the SSS switch again when the loop of magnetic tape is at positions F1 and M1 in Figure K-24. The tape will stop.
- (7) Adjust RV2F and RV2M so that the voltage at LSF and LSM is $6.5 \pm 0.2 \text{ V}$.
- (8) Set the field tester switches to command code \$AB. Toggle the SSS switch to start the capstan moving backward. Toggle the SSS switch when the tape is at positions F2 and M2 in Figure K-24. The tape will stop.
- (9) Adjust RV2F and RV2M so that the voltage is no lower than 6.5 V and no higher than 8.5 V.
- (10) Toggle the SSS switch to terminate the test.

Check and Adjustment of File Protection Mechanism

Check and adjustment of the file protection mechanism is performed by confirming the position of the pin head of the file protection in both (1) a normal state (no tape loaded or tape without a write enable ring loaded) and (2) when magnetic tape with the write enable ring is loaded.

(1) Normal state (no tape loaded or tape without a write enable ring loaded).

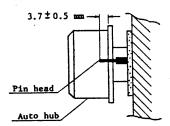


Figure K-26.

(2) Magnetic tape with write enable ring is loaded. Push the pin head as far as the flange surface and press the LOAD/REWIND button. Check that the distance between flange surface and pin head is 2.5 mm or more. If incorrect, the file protection mechanism must be replaced.

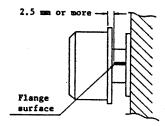


Figure K-27.

(3) Push the pin head by hand. Check that the microswitch is actuated before the pin point is moved 1 to 2.8 mm. If not actuated, remove the file protection mechanism from the panel and adjust the position of the microswitch.

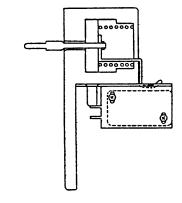


Figure K-28.

Check and Adjustment of Front Door Synchronous Belt Tension

Check and adjust the front door synchronous belt tension as follows:

- (1) Use a spring scale (1 kg maximum) as the measuring instrument.
- (2) Check Procedures
 Open the front door and remove cover to gain access to the belt.
 Place the spring scale against the belt at the position indicated
 by the arrow 1 (Figure K-29). When the belt deflection is about
 7.8 mm, the deflection force should be 0.11 to 0.17 kg. For the
 measurement, the slide-rail part must be removed from the belt
 and the belt must be free.
- (3) Adjustment Procedures
 Belt tension adjustment is performed by loosening one screw of
 the upper pulley, shown in Figure K-29. Move the pulley up or
 down to adjust tension.

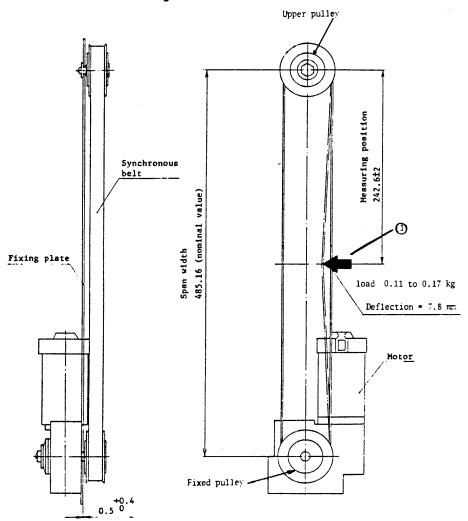


Figure K-29. Location of spring scale against belt.

K0290 CHECK AND ADJUSTMENT PROCEDURES

Check of Autocleaner

- (1) The autocleaner can be positioned with the guide pins on the magnetic head, as shown in Figure K-30.
- (2) Check that the ribbon is taut and is properly mounted on the ribbon guide and slide part.
- (3) If ribbon is loose, depress the load button after turning the power on. When the motor turns automatically, the sag is eliminated.

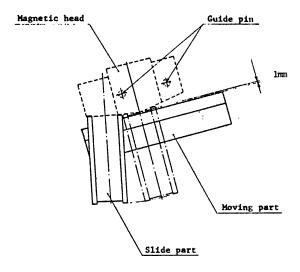


Figure K-30. Magnetic head and autocleaner.

LOOOO SUBASSEMBLY REPLACEMENT

During replacement of subassemblies, follow these general precautions:

(1) Turn off the power supply before initiating work.

(2) Use calibrated tools when specified by the replacement procedure.

(3) Retain all removed screws, washers, and nuts. Refer to the part numbers in the Illustrated Parts Catalog when replacing any parts.

(4) Remove parts that fall into the equipment.

(5) Document all trouble prior to replacement to ensure that those conditions have been corrected.

List of subassembly replacement procedures contained in Section L.

Subassembly	Map No.
Read/write head	L0010
Erase head	L0020
Write/read amplifier PCA	L0030
Threading channels	L0040
Tape cleaner	L0050
EOT/BOT sensor	L0060
Tape guides	L0070
Roller guides	L0080
Auto cleaner	L0110
Capstan motor	L0130
Threading chute and restraint member	L0140
Cartridge opener	L0150
Error marker	L0160
File protect assembly and microswitch	L0170
Auto hub and reel boss	L0180
Machine reel	L0230
Low tape sensor	L0250

Subassembly	Map No.
Reel motors	L0260
Vacuum column cover (glass plate)	L0270
Vacuum column cover (roller catch)	L0280
Microswitch and bracket for auto open window	L0300
Front door clutch assembly	L0310
Vacuum and pressure valve assembly	L0330
Restrictor	L0350
Fans	L0360
Cooling air filter	L0370
Absolute filter	L0380
Air supply unit and belts	L0400
Threading cover	L0410
Cartridge sensor	L0420
Capacitive sensor	L0430
Power supply unit	L0440
PCA shorting plugs	L0480

L0010 SUBASSEMBLY REPLACEMENT

Read/Write Head

I. Removal

- (1) Remove the erase head per L0020.
- (2) Remove the board connectors and the chassis ground terminal from the read/write head.
- (3) Loosen the block screw and remove the block.
- (4) Loosen the two head plate screws, and remove the read/write head.

II. Installation

Install the read/write head by reversing the steps for removal.

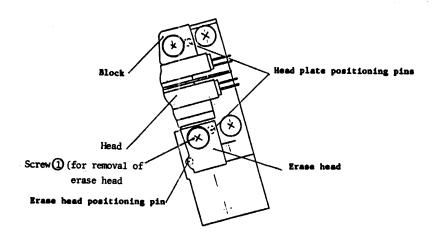


Figure L-1. Read/write head and erase head.

L0020 SUBASSEMBLY REPLACEMENT

Erase Head

I. Removal

- Remove screw 1 shown in Figure L-1. Pull the erase head out far enough to access the push-on connectors. Remove the two connectors and remove the erase head. (1)
- (2)

II. Installation

Install the erase head by reversing the steps for removal.

L0030 SUBASSEMBLY REPLACEMENT

Write/Read PCA

I. Removal

- (1) Turn off power to the MTU.
- (2) Tag and remove all connectors at the write/read PCA. (Refer to PCA location chart.)
- (3) Pull to release the two white PCA hold-downs that secure the PCA to the PCA frame.
- (4) Remove the PCA.

II. Installation

Install the PCA by reversing the steps for removal.

- III. Verify the replacement PCA by performing the following tests and adjustments:
 - (1) Write voltage (see K0160).
 - (2) Read signal level (see K0130, K0140).
 - (3) Read and write skew (see K0150).
 - (4) Perform offline diagnostic routine "00" (see Section C.2.1).

L0040 SUBASSEMBLY REPLACEMENT

Threading Channels

I. Removal

- Open the column cover and threading cover to gain access to the upper and lower threading channels shown in Figure L-2.
- (2) Remove three screws and the upper channel.
- (3) Remove two screws and the lower channel.

II. Installation

Install the upper and lower threading channels by reversing the steps for removal.

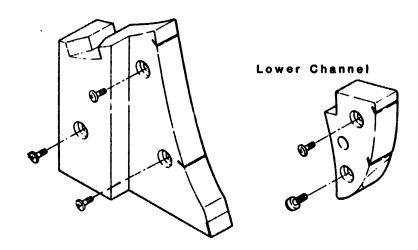


Figure L-2. Upper and lower threading channels.

L0050 SUBASSEMBLY REPLACEMENT

Tape Cleaner

I. Removal

- Remove two screws shown in Figure L-3. (1)
- Remove the tape cleaner. (2)

- Place the tape cleaner onto its positioning pin. Tighten the two screws shown in Figure L-3. (1)
- (2)

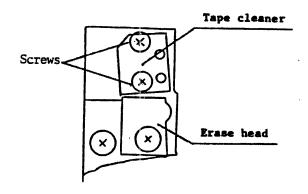


Figure L-3. Tape cleaner.

LOOGO SUBASSEMBLY REPLACEMENT

EOT/BOT Sensor

I. Removal

- (1) Remove connector (CNJ54) from the photosensor block.
- (2) Remove the two screws and remove the photosensor block.

- (1) Install the photosensor block by reversing the steps for removal.
- (2) Check and adjust the BOT and EOT detector circuits (see K0210).

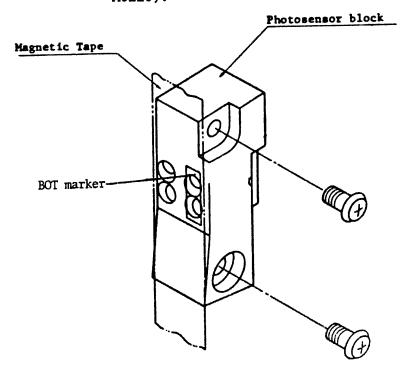


Figure L-4. Beginning of tape and end of tape sensor.

L0070 SUBASSEMBLY REPLACEMENT

Fixed Upper and Lower Tape Guides

I. Removal

- (1) Remove two screws at the front of the upper guide shown in Figure L-5 and remove the guide.
- (2) Remove two screws and remove the flange from the guide.

Note: Some models have a spring on the flange. Retain the spring for installation.

- (3) Remove two screws and remove the lower guide.
- (4) Remove four screws and remove the flanges from the front and rear of the guide.

II. Installation

Install the upper and lower guides by reversing the steps for removal.

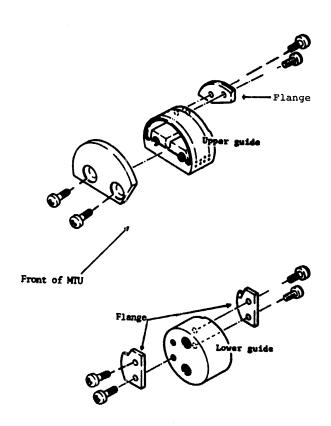


Figure L-5. Fixed upper and lower tape guides.

L0080 SUBASSEMBLY REPLACEMENT

Roller Guides

I. Removal

Insert a flat-blade screwdriver into the slot of the roller guide and rotate it counterclockwise. The roller guide is shown in Figure L-6.

II. Installation

Install the roller guide in the reverse order of removal.

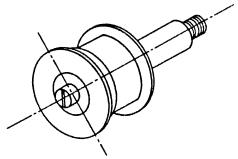


Figure L-6. Roller guide.

L0110 SUBASSEMBLY REPLACEMENT

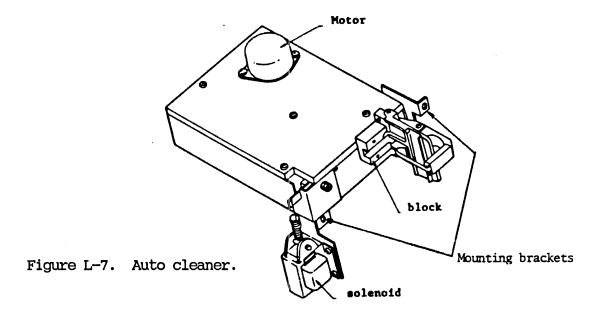
Auto Cleaner

I. Removal

- (1) Disconnect (and tag) the connector from the upper motor. Disconnect (and tag) the connector from the lower motor and solenoid.
- (2) Remove the four screws securing the mounting bracket to the mounting block and remove auto cleaner shown in Figure L-7.

Note: Do not allow the auto cleaner to contact the read/write head during removal.

- (1) Place the auto cleaner onto its positioning pin at the rear of block, and push down the cleaner until it reaches the block.
- (2) Install four screws securing the mounting bracket.
- (3) Connect the two connectors from the upper and lower motor and solenoid.
- (4) Perform auto cleaner checks and adjustments per K0290.



L0130-1 SUBASSEMBLY REPLACEMENT

Capstan Motor Removal and Installation

I. Removal

- (1) Disconnect connectors CNJ51 and CNP82.
- (2) Remove two nuts, washers, and springs accessible from the rear of the MTU, as shown in Figure L-8.
- (3) Carefully slide the motor out and off the shaft.

Note: Avoid damaging the capstan roller.

II. Installation

(1) Slide the motor onto the shaft of spring section.

Note: Avoid damaging the capstan roller.

- (2) Install two springs, washers, and nuts. Tighten the nuts (9 to 9-1/2 turns) to compress the spring.
- (3) Connect connectors CNJ51 and CNP82.
- (4) Perform capstan motor adjustment procedures (see L0130-2).

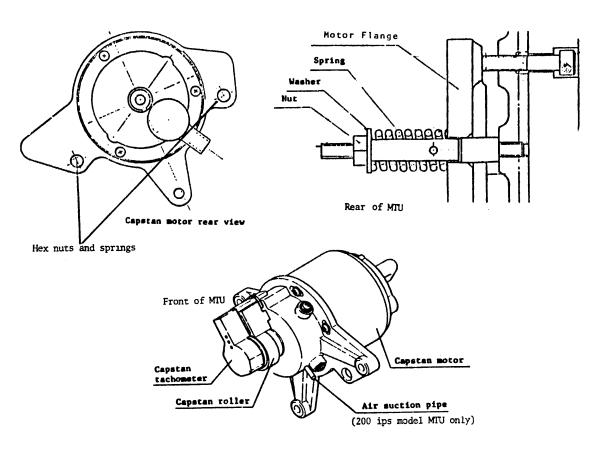


Figure L-8. Capstan motor.

L0130-2 SUBASSEMBLY REPLACEMENT

Capstan Motor Adjustment

I. Adjustment Precautions

- (1) Perform capstan motor adjustment procedures whenever the capstan motor has been replaced.
- (2) Use a good quality tape (12.63 to 12.65 mm wide).
- (3) Install the capstan motor so that the largest clearance is obtained between capstan and rib (see ① on Figure L-9).
- (4) If the adjusting screws ② and ③ are rotated two turns or more, check the clearance between capstan, rib ① and casting face ④ to prevent capstan damage.
- (5) During adjustment, check for the correct tape speed.

II. Adjustment Procedure

- Perform an auto load by mounting a tape and pressing LOAD/ REWIND pushbutton on the MTU front panel. Remove the threading cover and lower channel.
- (2) Remove the front flange of lower tape guide (5) (see L0070) and re-install the tape guide.
- (3) Issue command \$01 then toggle the SSS switch using the field tester to rotate the tape in the forward direction. Adjust LH screw 3 so that the front edge of tape is just at the edge of the tape guide.
- (4) Issue command \$41 to rotate the tape in a reverse (backward) direction. Adjust the RH screw ② so that the front edge of tape is just at the edge of the tape guide.
- (5) Repeat steps 3 and 4 until the front and rear of the tape does not change positions when the tape motion is changed from forward to reverse, and back again.
- (6) After adjustment, rotate both the RH and LH adjusting screws clockwise. When the tape is in FWD or REW mode, the surface guides (B and C shown in Figure L-10) must be slightly visible for type A, or the surface guide of B must be slightly visible for type E.

Note: Excessive tape movement in the transverse direction requires that the adjustment be performed again.

(7) Remove the tape by pressing UNLOAD and re-install the front flange of tape guide (5), threading cover, and lower channel.

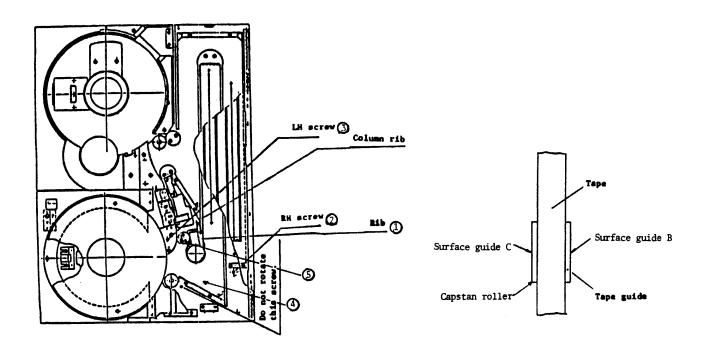


Figure L-9. Capstan adjustment.

Figure L-10. Tape guides.

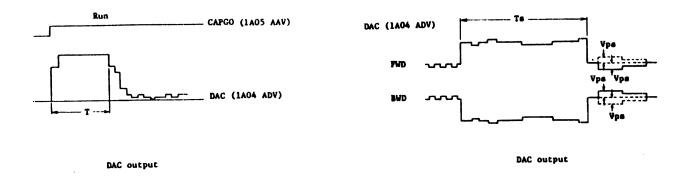


Figure L-11. DAC Output-Start Time. Figure L-12. DAC Output-Stop Time.

L0130-3 SUBASSEMBLY REPLACEMENT

Electrical Check of Capstan Motor

- I. Capstan Starting Time/Stop Time (Normal mode)
 - (1) Issue command \$E0 with a field tester to put the MTU in the normal speed mode.
 - (2) Issue command \$30 to perform the forward start/stop operation.
 - (3) Trigger the leading edge of signal CAPGO at 1A05 AAV. 1A05 AAV and 1A04 ADV are also available on the MTUlogic gate motherboard. Check that the time T shown in Figure L-11 is in accordance with Table 1.
 - (4) Check that the time Ts shown in Figure L-12 is in accordance with Table 2.
 - (5) Issue command \$6A and perform a backward start/stop operation. Check the time T and Ts in the same manner as above.

Table 1. Starting time, T.

Running Starting time			Check location	
direction	75 ips	125 ips	200 ips	Tocacton
FWD	1.50 to 2.00 ms	0.70 to 1.10 ms	0.70 to 1.10 ms	(DAC) PCA 1A04
BWD	1.80 to 2.70 ms	0.90 to 1.25 ms	0.80 to 1.20 ms	at ADV

Table 2. Stop time, Ts.

Model	Stop time Ts (FWD/BWD)	Vps (Maximum)	Check location	
75 ips	2.15 <u>+</u> 0.2 ms	1.0 V	(DAC)	
125 ips	1.30 <u>+</u> 0.2 ms	1.7 V	PCA 1A04 at ADV	
200 ips	1.20 <u>+</u> 0.3 ms	1.7 V	ac ADV	

L0130-3 SUBASSEMBLY REPLACEMENT

II. Capstan Starting Time/Stop Time (Streaming Mode)

- (1) Issue command \$E4 with a field tester to put the MTU in the streaming mode.
- (2) Issue command \$25 to perform the forward start and stop operation. (See Figure L-13.)
- (3) Trigger the leading edge of signal ACT at 1A05 BE7, 1A05 E7, and 1A04 ADV are also available on the MTU logic gate motherboard. Check that the time Tst and Tsp shown in Figure L-13 is in accordance with Table 3.
- (4) When in a streaming mode, the start and stop time can be measured by moving the tape either forward or backward. The backward start/stop operation is performed by issuing command \$65.

Table 3. Streaming start (Tst) stop time (Tsp).

Model	Direction	Tst	Tsp	Max. Vco	
125 ips	FWD	2.8 to 3.9 ms	1.3 ± 0.2 ms	1 4 77 37	
125 lps	BWD	2.4 to 3.6 ms		<u>+</u> 1.7 V	
200 ips	FWD	1.4 to 1.9 ms		25100 == 145	. 4 🖭
200 lps	BWD	1.3 to 1.8 ms	2.5 <u>+</u> 0.2 ms	<u>+</u> 1.7 V	

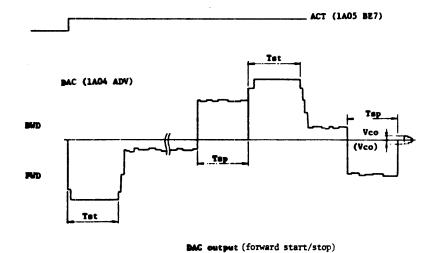


Figure L-13. DAC output (forward start/stop).

L0140 SUBASSEMBLY REPLACEMENT

Threading Chute and Restraint Member

I. Removal

- (1) Unscrew three threading chute mounting screws and remove the threading chute shown in Figure L-14.
- (2) Unscrew four restraint member mounting screws and remove the restraint member.

- (1) Mount threading chute onto the positioning pins and secure with three screws.
- (2) Prior to installing the restraint member, press the gasket of the restraint member with finger. Ensure that the gasket returns to its original shape. If it does not return to original shape, replace the gasket.
- (3) Mount the restraint member on to the positioning pin and secure with four screws.

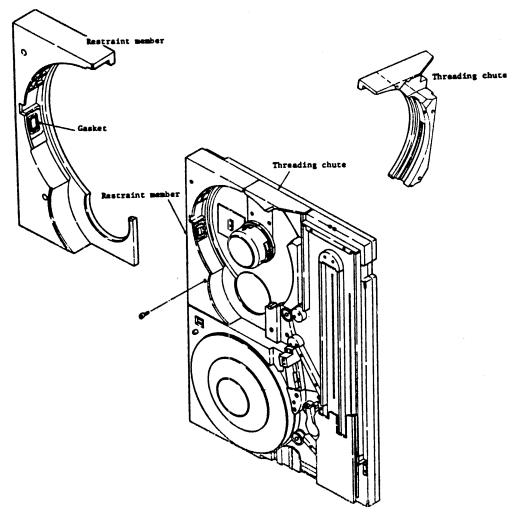


Figure L-14. Threading chute and restraint member.

L0150 SUBASSEMBLY REPLACEMENT

Cartridge Opener

I. Removal

- (1) Remove the plate retaining screw, shown in Figure L-15, and remove the plate.
- (2) Open the rear door on the MTU, and disconnect connector CNP52.
- (3) Remove the three screws (A), and remove the cartridge opener.

- (1) Secure the cartridge opener onto the casting using three screws (A).
- (2) Connect connector CNP52.
- (3) Install the plate and the plate retaining screw.

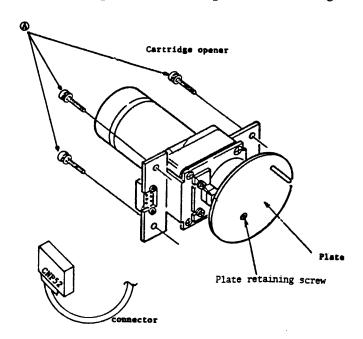


Figure L-15. Cartridge opener.

L0160 SUBASSEMBLY REPLACEMENT

Error Marker

I. Removal

- (1) Open the rear door and disconnect connector CNP53 located above the file reel motor.
- (2) Remove the two error marker retaining screws shown in Figure L-16 and remove the error marker.

II. Installation

Install the error marker by reversing the steps for removal.

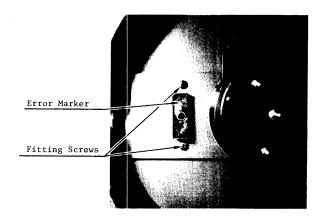


Figure L-16. Error marker.

L0170 SUBASSEMBLY REPLACEMENT

File Protection Assembly and Microswitch

I. Removal

- (1) Remove the two screws securing the file protection assembly on the panel shown in Figure L-17.
- (2) Pull out the file protection assembly and remove the air tube shown in Figure L-18.
- (3) Disconnect and tag the microswitch lead wires and remove the microswitch.
- (4) Remove the metal bracket from the file protection assembly.

- (1) Install the microswitch on the file protection assembly with the glass cloth between the microswitch and the metal bracket.
- (2) Connect the microswitch lead wires.
- (3) Install the microswitch assembly onto the file protection assembly.
- (4) Connect the air tube.
- (5) Install the file protection assembly on the panel using two screws.
- (6) Check and adjust the file protection assembly (see K0260).

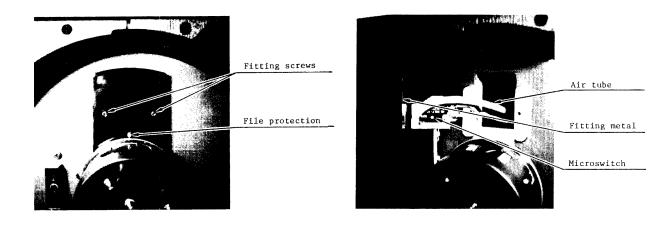


Figure L-17. File protection assembly (front view of MTU).

Figure L-18. Microswitch (rear view of MTU).

L0180 SUBASSEMBLY REPLACEMENT

Auto-Hub and Reel Boss

I. Removal

- (1) Peel off the adhesive cover shown in Figure L-19.
- (2) Insert the 7.5 mm-thick cam alignment spacer (B960-0110-X085A) between the cover assembly and the cam.
- (3) Remove screws (A) shown in Figures L-20 and L-21 and remove the rear cover.
- (4) Remove screw (B) shown in Figure L-20 and remove the clamp.
- (5) Remove the rear housing assembly.
- (6) Remove the bushing.
- (7) Hold down the spring-loaded cover assembly while removing 3screwsCshown in Figure L-19. Remove the cover assembly.
- (8) Remove the cam assembly and cam return spring shown in Figure L-19.
- (9) Remove the latch assemblies together with the latch return, spring and roller assemblies shown in Figure L-19 and L-22.
- (10) Remove screw ① shown in Figure L-19, and remove the reel boss from the motor shaft.

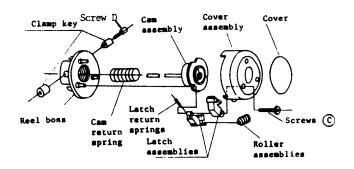


Figure L-19. Cover and reel boss assembly.

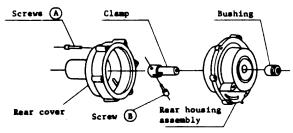


Figure L-20. Rear housing and rear cover assembly.

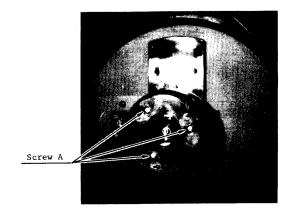


Figure L-21. Auto-hub rear cover assembly.

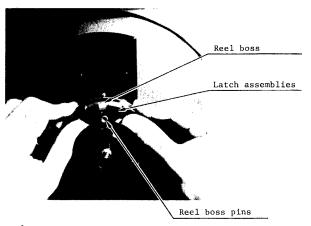
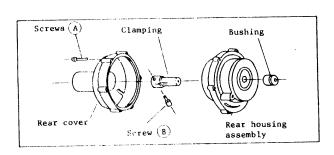


Figure L-22. Removal of cam assembly.

- (1) Mount the reel boss to the reel motor shaft using a clamp key, and adjust the reel boss position as follows (see Figure L-23):
 - (a) Remove the threading chute (L0140).
 - (b) Set the short pointer of dial gauge 4mm to 6mm and adjust the long hand of dial gauge 0.79 mm on the main column surface.
 - (c) Place the adjustment tool on the column surface.
 - (d) Adjust the reel boss position so that the distance between the vacuum column surface and the rubber ring on the reel boss surface is 2.79 ± 0.05 mm.

 The long pointer of the dial gauge should indicate 0 + 0.05 mm.
- Mount the roller assemblies and latch assemblies to the reel boss pins and the mount latch return springs (Figures L-19 and L-22).
- (3) Mount the cam assembly and cam return spring so that the three notches of the cam assembly are aligned with the pin positions.
- (4) While pressing the cover assembly by hand, install the three screws (C), shown in Figure L-19.
- (5) Insert the cam alignment spacer between the cover assembly and the cam.
- (6) Install the bushing on the reel motor shaft.
- (7) Mount the rear housing assembly so that the bushing is inserted into the bearing of the rear housing assembly. The housing assembly should be oriented so that the stopper screw on the rear side of the file reel (see Figure L-24) can be inserted into the screw hole on the housing.
- (8) Insert the clamp into the rear housing assembly. Install screw (B) shown in Figure L-20.
- (9) Install the rear cover using screws (A).
- (10) Remove the cam alignment spacer.
- (11) Install a new cover shown in Figure L-19.



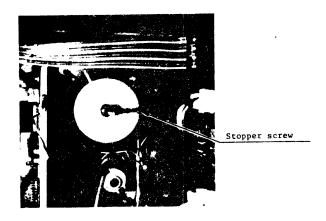


Figure L-23. Adjustment of reel boss position.

Figure L-24. Rear of file reel with stopper screw.

L0230 SUBASSEMBLY REPLACEMENT

Machine Reel

I. Removal

- (1) Remove the three screws (A) shown in Figure L-25, and remove the machine reel.
- (2) Remove screw (B), and remove the joint from the reel motor shaft.

- (1) Use calipers to measure the distance between the joint flange surface and the reel motor shaft © in Figure L-25. Adjust the distance to 7.5 mm, and tentatively secure the joint with the screw B.
- (2) Secure the machine reel with the screws (A). Remove the screws (D) and remove the front flange.
- (3) Remove the left threading channel.
- (4) Install the adjustment tool (B960-0110-T015A) on the main column surface, as described in L0180. The short pointer of the dial gauge must indicate 4 mm or 5 mm.
- (5) Place the adjusting tool on the reference plate, and hold it so that the dial gauge pin comes into contact with the rear flange at (E) in Figure L-25.
- (6) While manually rotating the machine reel, check whether the dial gauge reading, including fluctuation, is within the specified range.
- (7) Slightly pull out the whole assembly prior to the adjustment, and adjust the distance (F) into the specified range by gradually pushing in the assembly while measuring the distance.
- (8) Adjust the distance between the rear flange and the reference plate (F) in Figure L-25 to from 0 to 0.1 mm using the adjusting tool (B960-0110-T010A) shown in Figure L-26.
- (9) Tighten joint screw (B).
- (10) Install the front reel flange.

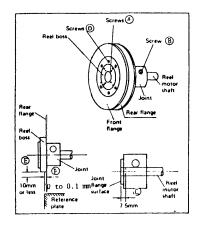


Figure L-25. Machine reel.

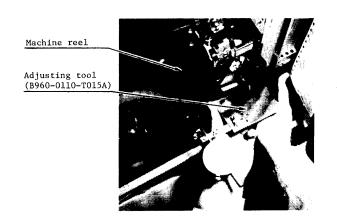


Figure L-26. Adjustment of machine reel.

L0250 SUBASSEMBLY REPLACEMENT

Low Tape Sensor

I. Removal

- (1) Remove three screws (A) shown in Figure L-27, and remove the machine reel.
- (2) Disconnect connector CNJ56.
- (3) Remove two low tape sensor mounting screws and remove the low tape sensor.

- (1) Install the low tape sensor by reversing the steps, above, for removal.
- (2) Check low tape sensor detector level (see K0220).

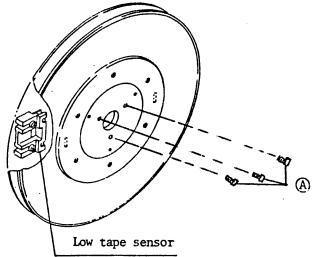


Figure L-27. Machine reel.

L0260 SUBASSEMBLY REPLACEMENT

Machine Reel Motor and File Reel Motor

- I. Removal of File Reel Motor (See Figure L-28)
 - (1) Remove the error marker (see L0160).
 - (2) Remove rear cover, clamping, rear housing assembly, and bushing (see L0180).
 - (3) Loosen the reel boss securing screw and pull out the autohub (see L0180).
 - (4) Disconnect connector CNJ86.
 - (5) Remove the four mounting bolts and remove the motor.
- II. Removal of the Machine Reel Motor (See Figure L-29)
 - (1) Remove the machine reel (see L0230).
 - (2) Disconnect connector CNP88.
 - (3) Remove the four mounting bolts and remove the motor.

III. Installation

Install the reel motors in the reverse order of removal.

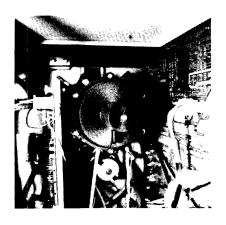


Figure L-28. File reel motor.

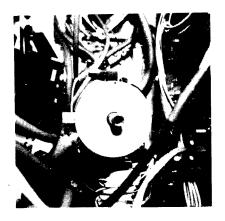


Figure L-29. Machine reel motor.

L0270 SUBASSEMBLY REPLACEMENT

Vacuum Column Cover (Glass Plate)

I. Removal

- (1) Open column cover and remove five glass plate screws (see Figure L-30).
- (2) Removethe spring that holds the glass plate.

II. Installation

(1) Install the glass plate in reverse order of removal.

(2) Press the glass plate gently by hand in the vicinity of the spring. Check that the glass plate returns to its original position when released.

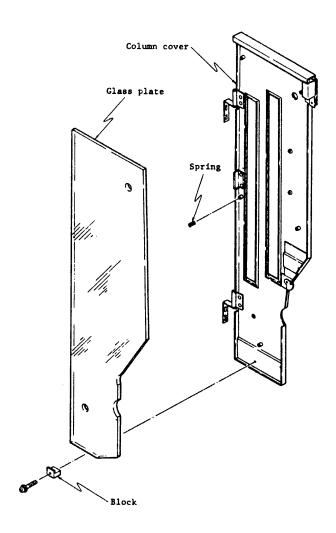


Figure L-30. Vacuum column cover.

LO280 SUBASSEMBLY REPLACEMENT

Column Cover (Roller Catch)

I. Removal

Remove two roller catches located at the top and bottom left hand side of the column (see Figure L-31) by removing the attaching screws.

- (1) Install each roller catch by re-installing the two screws.
- (2) When the cover is closed, check that each roller catch is firmly installed and that there is no gap between the column ribs and the glass.
- (3) If incorrect, adjust the roller catch within the oval mounting holes.

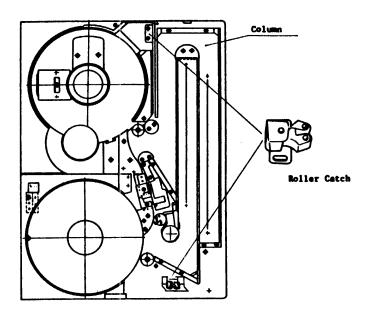


Figure L-31. Roller catch.

L0300 SUBASSEMBLY REPLACEMENT

Microswitch for Auto-Open Window

I. Removal

- (1) Remove the cover ① of the front door. (See Figure L-33 in L0300-2.)
- (2) Remove the cover (2) over the two window microswitches.
- (3) Remove the microswitch to be replaced. See Figure L-32 for location of two microswitches.
- (4) Detach the leads from the terminal.

II. Installation

(1) Install the window microswitch(es) in the reverse order of removal.

Note: When the microswitch is being adjusted, the power supply unit must be turned off. However, the unit can be turned on, the window placed in the open or closed position by issuing command \$B6 from the field tester, and the power turned off again. Before putting the microswitch in the detecting status, loosen the mounting plate screws to prevent the actuator from being bent.

- (2) Adjust the gap between the microswitch and the actuator from 0.33 mm to 0.55 mm by loosening the adjustment screws, as shown in Figure L-32.
- (3) When the power supply is turned on and the window is opened and closed, check that the top of the window touches the sponge surface and that it is 0 to 2 mm above the bottom. If incorrect, readjust.

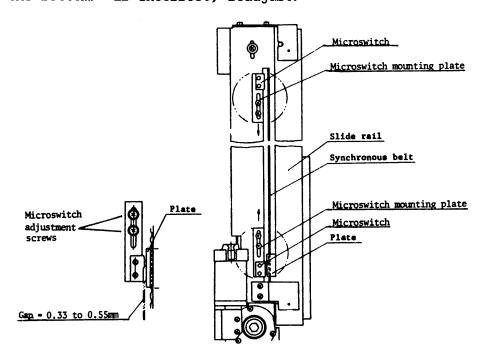


Figure L-32. Microswitch removal and adjustment.

L0300-2 SUBASSEMBLY REPLACEMENT

Front Door Auto Window Bracket

I. Removal

- (1) Open the front door, and remove six cover screws and the covers.
- (2) Remove three window screws.
- (3) Disconnect connector CNP57.
- (4) Remove three auto window bracket screws and loosen the remaining screw. Slide the window to the left and remove the auto window bracket.

- (1) Mount the auto window bracket onto the loosened screw, install the remaining screws, and tighten all four screws.
- (2) Install the window and tighten three screws. Connect connector CNP57.
- (3) Install covers. When mounting covers, do not place wires and cables between the cover and door.
- (4) After assembly is complete, ensure that the window operates correctly. Issue command \$B6 with the field tester.

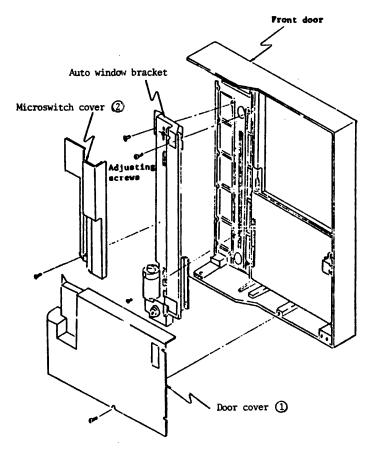


Figure L-33. Auto window bracket.

L0310 SUBASSEMBLY REPLACEMENT

Front Door Clutch Assembly

I. Removal

- (1) Loosen the hex socket screw on the moving pulley shown in Figure L-34 to decrease belt tension.
- (2) Remove the belt from the fixed pulley. Loosen the hex screw and remove the fixed pulley.
- (3) Remove four microswitch screws.

Caution:

Never remove or loosen screws on the base plate. These screws have been adjusted for proper positioning.

- (4) Remove cable clamping screws.
- (5) Remove four clutch assembly screws and the clutch assembly.
- (6) When replacing the belt, first remove four screws from the slide rail mounting plate and remove the mounting plate. Remove and replace the belt.

- (1) Install the front door clutch assembly by reversing the steps, above, for removal.
- (2) Check that the belt tension is from 0.11 to 0.17 kg at a deflection of 7.8 mm and at a distance of 242 mm from the center of either pulley.

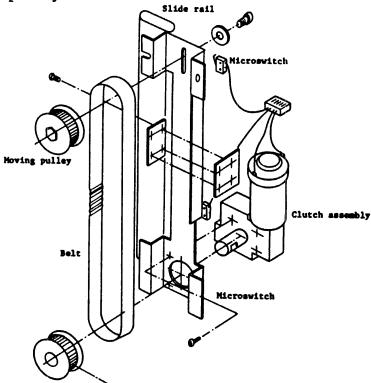


Figure L-34. Clutch assembly.

L0330 SUBASSEMBLY REPLACEMENT

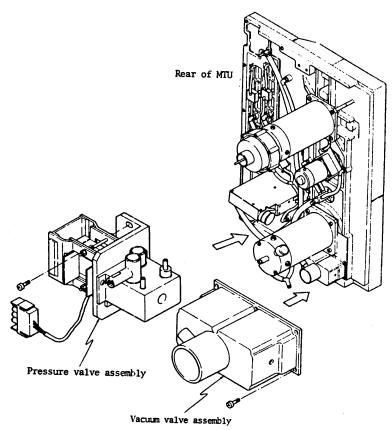
Vacuum and Pressure Valve Assembly

I. Removal

- (1) Disconnect all hoses and tubes from the rear of vacuum and pressure assembly shown in Figure L-35.
- (2) Disconnect connector CHP65, located on the rear of the MTU power supply unit. To access CNP65, open the lower, left-hand front door of the MTU. Remove six screws and the access plate.
- (3) Remove six mounting screws on the vacuum assembly and four mounting screws on the pressure assembly. Remove the two assemblies. (Note that in some models, the assemblies are joined to form a single unit.)

II. Installation

- (1) Install the vacuum and pressure valve assembly by reversing the steps, above.
- (2) Install the vacuum assembly first and the pressure assembly next (when these units are separate).



(Note: on some models, the vacuum and pressure assemblies are joined to form a single unit).

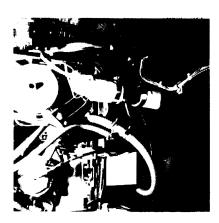
Figure L-35. Vacuum and pressure valve assembly.

L0350 SUBASSEMBLY REPLACEMENT

Restrictor

Removal and Installation

- (1) Loosen the hoses bands at both ends of the restrictor shown in Figure L-36. Remove the restrictor. When attaching the restrictor, connect the hoses to both ends, and fasten them with the hose bands.
- (2) Check and adjust the pressure and vacuum level. (See K0190.)



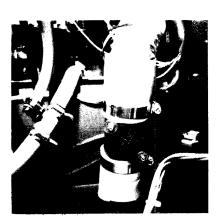


Figure L-36. Restrictor.

L0360 SUBASSEMBLY REPLACEMENT

FMT and MTU Logic Gate Fans

I. Removal

- (1) Open the rear doors and disconnect the connectors from the fans shown in Figure L-37.
- (2) Remove four fan mounting screws and remove the fans.

II. Installation

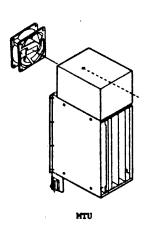
- (1) Install the FMT and MTU logic gate in the reverse order of removal.
- (2) Ensure the fans are operational (rotating) after replacement.

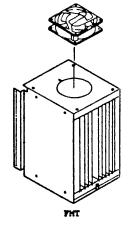
Air Supply Unit Cooling Fans

I. Removal

- (1) Open the lower left-hand doors on the MTU front panel.
- (2) Remove the filter, and disconnect connector CNH42.
- (3) Remove fourscrews and remove the fan.

- (1) Install the air supply cooling fan in the reverse order of removal.
- (2) Ensure that the fan is operational (rotating) after replacement.





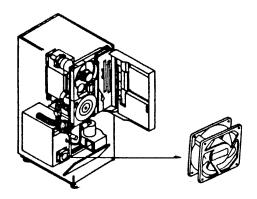


Figure L-37. FMT/MTU logic gate fans.

Figure L-38. Air supply unit cooling fans.

L0360 SUBASSEMBLY REPLACEMENT

Rear Door Fan

I. Removal

- (1) Disconnect connector CNP45.
- (2) Remove six nuts and remove the duct from the rear door shown in Figure L-39.
- (3) Remove two screws and remove the fan.

II. Installation

- (1) Install the rear door fan in the reverse order of removal.
- (2) Ensure the fan is operational after replacement.

Fan Assembly

I. Removal

- (1) Open the lower left-hand door on the MTU front panel and open the internal door by removing two screws.
- (2) Remove six screws and remove the panel to gain access to the fan assembly shown in Figure L-40.
- (3) Disconnect connector CNP43.
- (4) Remove two screws and remove the fan assembly.

- (1) Install the fan unit in the reverse order of removal.
- (2) Ensure the fan is operational (rotating) after replacement.

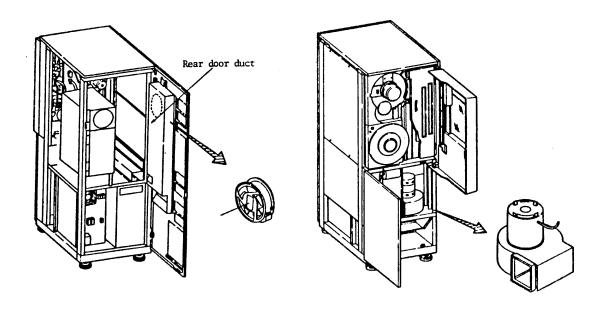


Figure L-39. Rear door fan.

Figure L-40. Fan assembly.

L0360 SUBASSEMBLY REPLACEMENT

FMT/MTU Power Supply Unit Fans

I. Removal

The FMT power supply fan is located on the top of each power supply unit. The MTU power supply fan is located at the rear of the MTU on the power supply unit. Unplug each fan, remove four screws, and remove the fan.

II. Installation

Install each fan by reversing the steps, above, for removal.

L0370 SUBASSEMBLY REPLACEMENT

Cooling Air Filter

I. Removal

- Open the lower left-hand front door of the MTU and remove (1) the filter shown in Figure L-41. Clean the filter (J0001).
- (2)

II. Installation

Ensure the filter is completely dry before replacement.

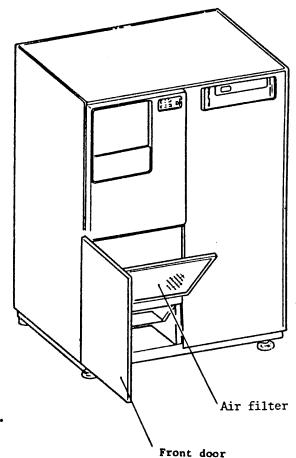


Figure L-41. Air filter.

L0380 SUBASSEMBLY REPLACEMENT Absolute Filter

I. Removal

- (1) Open the lower left-hand front door of the MTU to locate the absolute filter.
- (2) Remove the tube from the hose tap, as shown in Figure L-42.
- (3) Remove three screws.
- (4) Carefully unscrew the absolute filter off the joint.

II. Installation

CAUTION:

When mounting the absolute filter, do not turn the hose tap, shown in Figure L-42.

Install the absolute filter by reversing the steps, above, for removal.

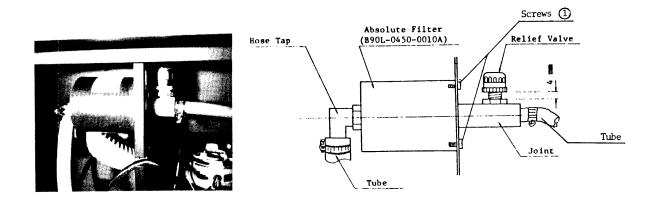


Figure L-42. Absolute figure.

L0400 SUBASSEMBLY REPLACEMENT

Air Supply Unit

I. Removal

- (1) Open the MTU lower left-hand door. Remove six screws and remove the plate to gain access to the front of the air supply unit.
- (2) Disconnect the hose from the blower air inlet and blower air outlet, shown in Figure L-43.
- (3) Disconnect the tube at the pump outlet.
- (4) Disconnect power connector CNP44 of air supply.
- (5) Remove two screws ① at the front of the air supply unit.
- (6) Open the MTU rear door and remove four screws ② and remove the air supply unit mounting bracket.
- (7) Remove the air supply unit.

- (1) Install the air supply unit by reversing the steps, above, for removal.
- (2) Perform the pressure check in K0190.

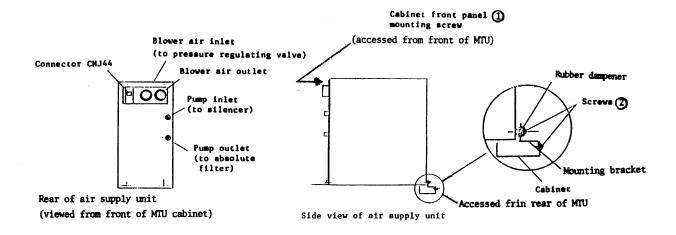


Figure L-43. Air supply unit.

L0400 SUBASSEMBLY REPLACEMENT

Air Supply Unit Belts

Note: The air pump belt can be replaced and adjusted while the air supply unit remains in the cabinet. Replacement and adjustment of the vacuum blower belt requires that the air supply unit be removed from the cabinet.

I. Removal

- (1) Remove the cover plate to gain access to the belts, shown in Figure L-44. Refer to K0190 and K0200 for additional belt installation data.
- (2) Loosen the upper pulley and remove the old belt.

- (1) Install the new belt with the upper pulley adjustment screws loosened. Note the correct pulley orientation shown in Figure L-45. Refer to K0190 and K0200 for additional installation data.
- (2) Place a spring balance against the belt at a position midway between upper and lower pulleys.
- (3) Adjust the belt tension to 29 to 34 pounds, and tighten the pulley adjustment screws.

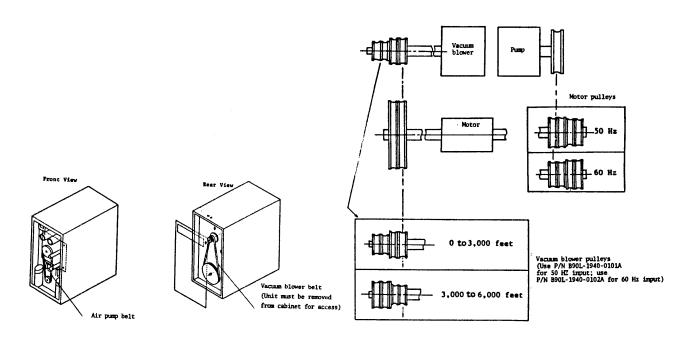


Figure L-44. Air supply unit belts.

Figure L-45. Air supply unit pulleys.

LO410 SUBASSEMBLY REPLACEMENT

Threading Cover

I. Removal

- (1) Open the vacuum column cover and threading cover.
- (2) Remove two screws from the upper hinge.
- (3) Pull up the threading cover and remove it.

- (1) Install the threading cover in the reverse order of removal.
- (2) Check to be sure that no interference occurs between the vacuum column cover and threading cover.

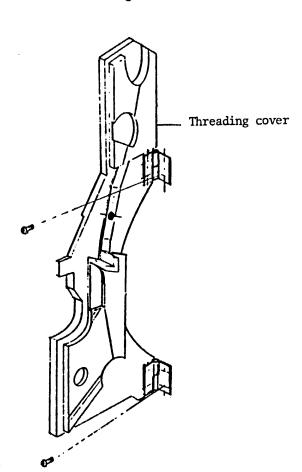


Figure L-46. Threading cover.

L0420 SUBASSEMBLY REPLACEMENT

Cartridge Sensor

I. Removal

- (1) Open the MTU rear door and remove two cartridge sensor mounting screws.
- (2) Disconnect the microswitch leads and remove the cartridge sensor.

- (1) Install the cartridge sensor in the reverse order of removal.
- (2) Ensure that the cartridge detector rod operates smoothly and returns by spring force.

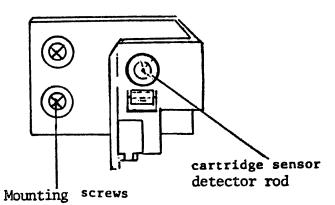


Figure L-47. Cartridge sensor.

L0430 SUBASSEMBLY REPLACEMENT

Cartridge Sensor

I. Removal

- Disconnect connectors CNJ55R and CNJ55L, and terminals (1) SWP1 and SWP2 from the capacitive sensor, shown in Figure
- Disconnect the air tubes at the location shown in Figure (2) L-49.
- Remove six capacitive sensor mounting screws and remove (3) the capacitive sensor.

- Install the capacitive sensor by reversing the steps, (1) above, for removal.
- (2) Perform the checks and adjustments described in K0240.

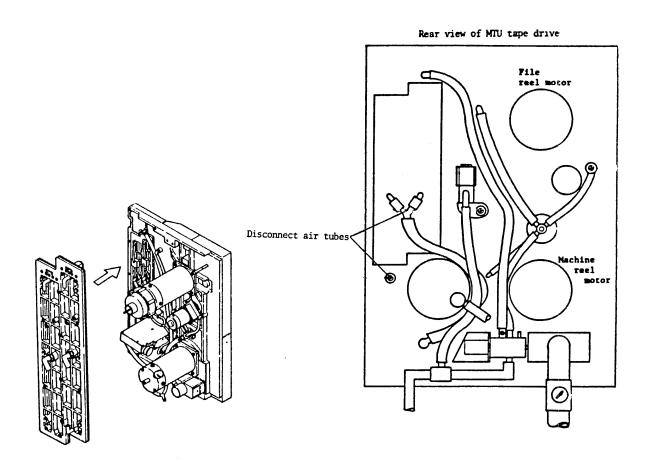


Figure L-48. Capacitive sensor. Figure L-49. Air tubes.

L0440 SUBASSEMBLY REPLACEMENT

Power Supply Unit

WARNING:

Ensure that the power cord has been disconnected from facility power before proceeding.

I. Removal

- (1) Disconnect and tag all connectors and leads from the power supply unit including the fan connector and frame ground leads.
- (2) Remove four screws and the mounting bracket.
- (3) Remove the power supply unit at the rear of the MTU.

II. Installation

- (1) Install the power supply unit by reversing the steps, above for removal.
- (2) Connect all terminals and connectors.

CAUTION:

For the MTU power supply unit, connect CNP66 to CNJ66A, and CNP66C to CNJ66B for 50 Hz input. Connect CNP66 to CNJ66B and CNP66C to CNJ66A for 60 Hz input.

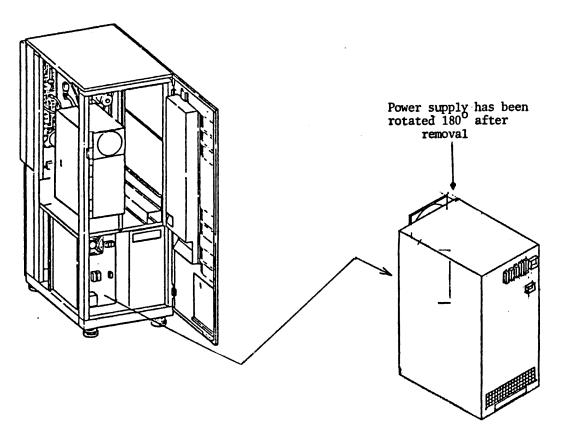


Figure L-50. MTU power supply unit.

L0480 PCA Shorting Plugs

Some printed circuit assemblies in the MTU and FMT have short-circuit options for setting contents, such as tape drive serial number or density. If a PCA is replaced, check and set short circuits as described below.

EXPLANATION OF THE SHORTING PLUG/TERMINALS

The positions (Figure L-51) in which the shorting plugs are installed on the shorting terminals represent a binary code.

Short-terminal



Figure L-51. Short-circuit location on PCA 1A06.

Example: In Table 4, below, when the shorting plug is installed between pins 3 and 4, a logical "1" is set. When the plug is installed between pins 2 and 3, a logical "0" is set. This sets the extended interface function.

Table 4. MTU PCA 1A06, mounting position AG4.

	Extended interface	File Search feature
Setting of '1'	3 - 4	6 - 7
Setting of '0'	(2 - 3)	(5 - 6)

Table 5 summarizes the shorting plug settings for both the MTU and FMT. MTU shorting plugs.

PCA	Mounting position	Level '0' (not enable)	Level '1' (enable)	Setting (see notes)	Contents
1A02				(b)	
		02 - 03	03 - 04	'0' (b)	
1A05	BG7	05 - 06	06 - 07	'0' (b)	
IAUS	BG/	09 - 10	10 - 11	'0' (a)	APR is supported
		12 - 13	13 - 14	'0' (Ď)	
	AF4	02 - 03 05 - 06 09 - 10 12 - 13	03 - 04 06 - 07 10 - 11 13 - 14	'0' (a) '0' (a) '0' (a) '0' (a)	Reserved Reserved Reserved APR installed
	AG4	02 - 03 05 - 06 09 - 10	03 - 04 06 - 07 10 - 11	'1' (b) '1' (b) '0' (b)	Extended interface File search by tape drive Tape drive serial number
1A06	AG5	12 - 13 02 - 03 05 - 06	13 - 14 03 - 04 06 - 07	(a)	Tape drive serial number
	AG6	09 - 10	10 - 11	(a)	Tape drive serial number
	AG7	12 - 13	13 - 14	(a)	Tape drive serial number
	AJ6	02 - 03 05 - 06 (Step C) 12 - 13	03 - 04 06 - 07 (Step A) 13 - 14	(a) '0' (a) '1' (b)	Optional density— select panel Threshold gain step for switching read slice level Tri-or dual density tape unit
Read/ write PCA		S3 S4		(b) (b)	S3 = 200 ips S4 = 125 or 200 ips

⁽a) Setting is determined by factory but can be changed.(b) Factory set. Do not change.

Table 5. (continued) FMT shorting plugs.

PCA	Mounting position	Level '0' (not enable)	Level '1' (enable)	Setting (see notes)	Contents
1A04	AQ7			(b)	
1A05	AF1 AF2 AF3 AG4 AF5 AF6 AF7			(b)	
	AG7	02 - 03 05 - 06 09 - 10 12 - 13	03 - 04 06 - 07 10 - 11 13 - 14	'0' (a) '0' (a) '0' (a) '0' (a)	20 - meter check
	АН7	02 - 03 05 - 06 09 - 10 12 - 13	03 - 04 06 - 07 10 - 11 13 - 14	'0' (a) '0' (a) '0' (a) '0' (a)	Reserved
1A07	AJ7	02 - 03 (c) 05 - 06 09 - 10 (c)	06 - 07	'0' (a) '0' (a) '0' (a)	CMDE is supported APR is supported Address line 2 is supported

⁽a) Setting is determined by factory but can be changed.
(b) Factory set. Do not change.
(c) Valid when '0'.
(d) Invalid when '1'.

Procedure 1: Setting the Serial Number

Read the serial number of the right lower side at the back of MTU, and convert the number to 13 bit binary code.

Example: If the serial number is 538 (or 0538), install shorting plugs on the shorting terminals at locations AG4, AG5, AG6, and AG7 as follows:

	AG4	AG6			AG5			AG7					
Setting of '1'	13–14	3-4	6-7	10-11	13–14	3-4	6–7	10-11	13-14	3-4	6–7	10-11	13-14
Setting of '0'	12–13	2–3	5–6	9–10	12–13	2-3	5–6	9–10	12–13	2–3	5–6	9–10	12–13

Procedure 2: Setting the Engineering Change Level

Convert the engineering change level to 4 bit binary code, and set SH09 (AF4) in the MTU as follows:

Correspondence of each bit and connected Pin No.

Setting of '1	3-4	6-7	10-11	13-14	Cor
Setting of '(2-3	5-6	9–10	12-13	COI

Connected pin No.

Note:

If the engineering change level is not changed, the PCA setting is the same as that for the previous PCA.

Example: When the engineering change level is 05

Binary code 0 1 0 1

Setting

Connected pin No. 2-3 6-7 9-10 13-14

Procedure 3: Setting the Function (AJ6) in the MTU

	Optional density	Gain step feature	Tri- or dual density
Setting of '1'	3 - 4	(6 - 7)	13 - 14
Setting of '0'	2 - 3	5 – 6	12 - 13

Note:

 ${\tt Gain\ step\ }\ldots\ldots$. If the read slice level changes when the SAGC step is greater than C, set it

to 0.

Tri- or dual density Always 1. Do not change.

ARPE A or B register parity error

AD Address ADR MTU address **AGCOK** SAGC OK ALAuto loading ALLIWT Write all 1's All "Ø"'s ALL ALMØ Alarm Ø ALMSK Alarm mask

ALU Arithmetic logic unit

ARA Automatic read amplification

AROBR A or B register

BAD Branch address
BCOK Byte count ok

BCT:3F Offline byte counter BDCK Deskewing buffer check

BEQ Branch if equal

BEQI Branch if equal indirect

BFUL Buffer full BI Bus in BIBSY Bus in busy BLFMT Block format BLKE Block end BLKED NRZ block end BLOCK Block sensed BLOCK Block status

BNE Branch if not equal

BNEI Branch if not equal indirect

BCC Branch on condition

BOCI Branch on condition indirect

BOT Beginning of tape

BOTS Beginning of tape status

BPS Bits per second (data transfer rate)

BSF Backspace file command
BSP Backspace command
BUSER Data bus parity error

BUSY Formatter busy

BWD Backward

BWDS Backward status

CBR Transfer buffer read
C-Cry Reposition counter's carry
CEQ Call subroutine if equal

CEQI Call subroutine if equal indirect

CLF Clock full CLH Clock half

CLNRZ Clock nonreturn to zero I

CLINF Column in file
CLINM Column in machine
CLR Drive clear command

CMD Command

Command extend mode **CMDE** Command sequence **CMDSEO** Compare CMR Call subroutine if not equal CNE Call subroutine if not equal indirect CNEI Control CNT Call subroutine on condition COC Call subroutine on condition-indirect COCI Capstan forward **CPFWD** Cyclic redundancy check CRC CRC error CRC ERR CRC horizon gap **CRCHG** CRC recording gap CRCRG CRC status CRCST Corrected error status CRERR Control storage CS CS parity error **CSPE** Control storage register CSR Control CTL CTSTP Counter stop Diagnostic control DACTL Detected automatic read amplification DARA Data check DATA CHK Data bus DB Data block format DBF Detection of beginning of block DBOB Device bus multiplex DBMPX Dual-density MTU DDF Stored in the source register of "1" DΕ Detect error track DET Detected error track 8 DET8 Diagnostic mode DIAG MODE Offline diagnostic test DIAG Detected inter block gap DIBG DSE inquiry DINQ Diagnostic mode read DMR Diagnostic mode set command DMS Detected noise DNOIS Condition register DRFG Drop out error DROE Define storage DS Density select (lines 0 to 1) DS Ø--1 DSB Drive sense byte Data security erase DSE Detected tape mark DTM Data transfer rate DTR Duration of unscheduled incidents DUI Device address multiplex DVAMPX Device busy DVBSY Device enable DVENB

Device inquiry

DVENO

DVINT Device interrupt
DVSNS Device sense
DXFI Data transfer in
DXFO Data transfer out

ECC Error correction character

ECER Erase circuit error ECON Erase current ON

EDC End data check (signal)

EDCK End data check

EMMVD Error marker moved

EMX Error multiplex

ENDATP End of data pulse

EOT End of tape

EOTS End of tape status

EPOSA Postamble read end condition

EQU Equivalence
ERRMX Error multiplex
ERS Erase command
ETK8 NRZ error track 8
EXCY Extend cycle
EXR External register

FMT Formatter

FMTST Formatter status
FPOS File protect status
FPS File protect status
FRPI Flux reversals per inch

FSF Space file command FSP Space command

FTP Full tach pulse signal

FWD Forward

GAPC Gap control GAPCT Gap control

GCR Group coded recording (format)

GDT Go down time
GO Device go
GOB Go tag

HBLKN NRZ block
HCLR Hardware clear
HDENS High density status
HDNS High density status

HIG High gain

HNIS Noise block detected

HUBAL Hub lock alarm

HUBLK Hub lock Hz Hertz

I IBG ID-BRST IHPOS IHPRE INATRP INCOR INDXF INULD IPOS IPS IRECU ISINT ISPHE ISV	Indirect bit Inter-block gap Identification burst Inhibit postamble Inhibit preamble Interruption Inhibit correction Inhibit data transfer Invalid code Inhibit postamble Inches per second Expecting data Initial selection interrupt Issue phase error (function) Instantaneous speed variation
KB/sec Kcal/H	Kilobits per second Kilocalories per hour
L LI LCMD LD LD* LDI LDI* LDI* LDIA LIBG LM L/RB LRC LRC LRCE LSI LSICL LSV LTLAL LWR LWRFMT LWRFMT	Lamp Lamp 1, Lamp 2 (L2), etc. Last command code Load D-register Load D-register and return Load D-register indirect Load D-register indirect and return Lost device address Long (IBG) counter Local memory Loop rewind button LRC cycle Longitudinal redundancy check LRC error Large-scale integration LSI clock Long-term speed variation Left tape loop alarm Loop write to read command Loop write to read in formatter Low slice
MARG MAS MASK8 M.CL MCRC MCRCZ MCY MCYENT MF MF	Marginal status set Monetary action switch Mask - 8 Micor clock Unmatch CRC (cyclic redundancy check) Unmatch CRC zero Machine cycle MCY entry parameter Modify Modify and return Modify-D register

MFD Modify-D register and return

M.INS INS trap mask
M.INT Device trap mask
MISC-ERROR Miscellaneous error

MLI Machine language immediate

MLITE Multiple track error

MP Microprogram
MPRD Microprogram read
MPXBO Multiplex bus—out
M.RER Mask register error

MSEC Milisecond

MSK Mask MSKA Mask A

MTBF Mean time before failure
M.TCS Mask tacho-pulse-stop trap

M.TMR Timer trap mask
MTREQ Microprogram in TREQ
MTTR Mean time to repair
MTU Magnetic tape repair

MUX Multiplexer

MV Move

MV* Move and return MVFI Move full indirect

MVFI* Move full indirect and return

MVHI Move half indirect

MVHI* Move half indirect and return

MVR Move register

MVR* Move register and return

NOISC Noise check (signal)
NOP No operation command

NRZI Nonreturn to zero change at "1" (recording format)

NSEC Nanosecond

NSKWE NRZ skew error

NSPM Normal speed mode

NURCE NRZ-URC error

OFL Offline

OFLCMD Offline command register
OFLONT Offline control register
OFLDVA Offline device address

ONL Online
ONIM Onine memory
ONLM Onine memory
ONLS Online status

OPINC Operation incomplete

ORG Origin
OSC Oscillator
OVRN Not overrun
OVRNS Overrun status

Printed circuit assembly PCA Parity error or compare error PCMP Phase encoded (recording format) PΕ Interrupt signal is set on when ROM parity error or Perr LSR parity error has occured. Processor halt PHLT Phase OK PHOK Pointer multiple PNMLT Pointer POINT:69 Postamble detected POSA Postamble error POSAE Power ready PRDY Preamble detected PREA Partial record PREC Subroutines in MCY Q Quarter tach-pulse signal (0.06m) QTP R Registers Register address RA Reset byte cycle/byte cycle R.BCY/BCY Reset bus out parity error/data bus parity error R.BPE/BUSPE Retry counter RCNT Reset counter/starter counter R.ONT/S.ONT Reposition counter RCTO - RCT7 Reset counter upper entry mode/counter upper entry mode R.CTRU/CTRU Read cycle RCY Read command RD Read backward command **RDB** Read control RDCTL RDYM Ready memory Ready status RDYS Bus direction receive mode REC Expecting data RECV Register error REGE REJECT Command reject Register enable RENB System reset RESET Rewind command REW Rewinding status REWS Register parity error RGPE Rewind inquiry RINQ Reject code stacks RJC Relay RLR.PER Reset processor error RO Read Output ROM parity error ROMPE

Reset reposition counter

ROM party error Rows per inch

ROMPS

R.RCT

RPI

Reset RST Right tape loop alarm RTLAL Return; "1" if returned from subroutine RTN Reset velocity change/velocity change R.VLC Adress stack; "1" if subroutine call S Self-adjust gain control SAGC Scan mode SCAN Scan pointer SCANP Initiated command SCMD Special compose SCMP Subroutine call/return SC/R Start down count S.DCT Set diagnose command SDIA SDRST/LRCE Sense data reset/not LRC error Selection reset SERT SETBC Set byte counter Shift CRC register **SFCRC** SHSP Set high speed command Status in function SIF SINH Start inhibit Skip inquiry SINQ Skew error SKEW Skip file feature SKIPF Skew marginal SKWMG Slip check SLIPC Select tag SLTAG Select multiplex SLX SLX2 - SLXØ Select multiplex 2 - select multiplex Ø Scheduled maintenance SM Sense drive status command SNS SNSCNT Sense counter Set normal speed SNSP Start read check SRDC Set condition SRDC Slave status change SSC SSCM SSC memory SSS Start, step, stop Initiate command START Step 6 ALL STEP6 Terminate command STOP Stand-by phase OK STPHK Slow register STR Store register and return STR* Start read check STRCK Streaming feature STRMF Status tag STS STS Status Subparameter SUB Start-up count SUCT SW Switches Reset signals systems reset SYRT

Tl	Transfer one
T2	Transfer two
T	Test
TA	Track assignment
TACH	Tachometer
TAGVL	Tag valid
TBB	Test bit and branch
TBBI	Test bit and branch indirect
TBC	Test bit and call subroutine
TBCI	Test bit and call subroutine indirect
TCSG	Tach-stop gate
TCSTP	Tach-stop
TCSP	Tach stop (signal)
TFMT	Test formatter
Th	Thermal
TIE	Track-in-error operation
T.INS	Trap by initial selection
T. INT	Trap by device interuption
TLA Left	Tape loop alarm left
TLA Right	Tape loop alarm right
TMCTL	Timer control
TMD	Tape mask detected
TMINT	Timer interrupt
TMS	Tape mark status
TMSR	Time sensor
TMTS	Test magnetic tape system
TOVR	Tape overrun
TP	Tape present
T.PER	Trap by processor error
TRAK	Transfer acknowledge
TREQ	Transfer request
TSFL	Testflag
TSNS	Time sense
TSPO	Tape speed code
TST	Test start
TTM	Tape transport mechanism
T.TMR	Timer trap (signal)
T.TMR	Trap by timer carry
TU	Tape unit
TUC	Tape unit check
TUCHK	Tape unit check
TUIF	Tape unit interface
	Tape unit interruption
TUINT	Refer to TUST
TULHT	MTU status register control
TUSMP	MTU status
TUST	
TWA	Tape warning area
U64S	Unit 64% slice
UACT	Unit action
UBWD	Unit backward
UCE	Uncorrectable error

UCHLD Unit check hold UCK Unit check

UERS Unit erase current

UFOS UFO start
UHSD UFO high speed
UNL Unload command

UPE Unit phase encoded mode

UQID Function ID USEM Used memory

UWCON Unit write current on

V Voltage

VELØ Velocity mode Ø VELl Velocity made l VEL ERR Velocity error

VFO Variable frequency oscillator

VICHG Velocity change VIOK Velocity OK

VRC Vertical redundancy check

VRCE VRC error

W Work register

WCER Write circuit error

WCY Write cycle

WEC Write error count overflow

WIND Window
WOK Write OK
W/R Write/read
W.REG W register

WRIST Write/read PCA installed

WRT Write command WRTS Write status

WTBOC Write data bus-out check
WTM Write tape mark command
WTMCK Write tape mark check
WTM-CHK Write tape mark check

WTURC Write URC

WVON Write voltage ON

XCALL Cross call

X-Call Cross-call feature XCTL Transfer control

XFR Transfer
XSNS Transfer sense

Y Subroutines in MCY

ZCTL NRZ control
ZETK NRZ error track
ZMRG NRZ marginal code

ZOP NRZ option ZRD NZR read

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
ABOT	(TK2P26)	Beginning of tape (BOT) detecting signal
ACEN	(RM3Q74)	
ACEN	(RM3N44)	Indicates that capstan motor is
*ACEN	(RM2G64)	rotating
ACT	(RGIJ65)	
ADBØØ′	(RG2B24)	
ADBØ1	(RG2B25)	Indicates the content of one from
ADBø2	(RG2B26)	the upper 4 bits of the return address register of a subroutine
ADBØ3	(RG2B27)	·
ADCRY	(RM1L54)	Indicates the carry bit of address counter
ADRØØ	(RM1K57)	
ADRØ1	(RM1K56)	
ADRØ2	(RM1K55)	
ADRØ3	(RM1K54)	
ADRØ4	(RM1F57)	
ADRØ5	(RM1F56)	Indicates the content of each bit
ADRØ6	(RM1F55)	from Ø to 11 address counter
ADRØ7	(RM1F54)	
ADRØ8	(RM1B57)	
ADRØ9	(RM1B56)	
ADR1¢	(RM1B55)	
ADR11	(RM1B54)	
*ADSET	(RM1N44)	Adress preset signal

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
AEOT	(TK2P24)	Indicates that end of tape is detected
AGCOK	(RW2G66)	Self-adjusted gain control (SAGC) OK signal from read amplifier
AGCON	(RG5E45)	Indicates that the AGC operation is
*AGCON	(RW5M24)	being carried out
AGC8F	(RW4J94)	Indicates that the content of SAGC counter is greater than 8.
AIRDV	(RG1F65)	
*AIRDV	(CB1D34)	Directs the drive of air—supply motor
*AIR2	(CB1F34)	MOCOL
ALAMÓ	(TK2C23)	
ALAM1	(TK2C24)	
ALAM2	(TK2C25)	
ALAM3	(TK2C26)	Alarm signal
*ALMØ	(CB1K34)	
*ALM1	(CB1J34)	
*ALM1	(VQ1C26)	
*ALM2	(VQ1D24)	
*ALM2	(CB1H34)	
*ALM3	(CB1G34)	
*ALM3	(VQ1D25)	
*ALM4	(VQ1D26)	
*ALM5	(VQ1E23)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
ALUOK	(RG1Q44)	
ALUOK	(RG1G26)	_ ,, , ,, ,, ,, ,, ,, ,, ,, ,, ,, ,, ,,
*ALUOK	(RG1Q34)	Indicates that the Arithmetic logic unit (ALU) operation is normal
ALUP	(AL1CY4)	Tudington the Buithmetic legic
ALUP	(AL1BX6)	Indicates the Arithmetic logic unit (ALU) output bus bit Ø through
ALUP	(AL1BX4)	7 and parity
ALUØ′	(AL1G74)	
ALUØ	(AL1B63)	
ALU1	(AL1B64)	
ALU1	(AL1B74)	
ALU2	(AL1J74)	
ALU2	(AL1B65)	Indicates Arithmetic logic unit (ALU)
ALU3	(AL1K74)	output bus bit 9' through 7 and parity
ALU3	(AL1B66)	
ALU4	(AL1G44)	
ALU4	(AL1G33)	
ALU5	(AL1B34)	
ALU5	(AL1H44)	
ALU6	(AL1J44)	
ALU6	(AL1B35)	
ALU7	(AL1B36)	
ALU7	(AL1K44)	
ALWT	(TK2P25)	Indicates that low tape is detected

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description	
BGO	(SN1N24)	Backward GO signal	
BK	(SN1C95)		
BK	(B15C94)	Indicates that capstan motor is	
*BKRUN	(TK1E24)	rotating backward	
BMD9'7	(MX1K44)		
BMD0/8	(RM2B34)		
*BMDØ8	(RM2B24)		
BMDØ9	(RM2D34)		
*BMD09	(RM2D24)		
BMD1ø	(RM2F34)	Indicates ROM data bit 7 through 1,0, 14 and 15	
*BMD1Ø	(RM2F24)	and 15	
BMD14	(RM2H34)		
*BMD14	(RM2H24)		
BMD15	(RM2K34)		
*BMD15	(RM2K24)		
BOEVN	(BI1LY4)	Indicates that Bus Out signal is even	
BOT	(TK2A26)		
BOT	(SN1J44)	Indicates that beginning of tape is	
BOTS	(BI1A54)	detected	
B09/	(BO3B44)		
*BOØ	(BO3B34)	Indicates individual contents of 8 bits from Ø to 7 of Bus Out signal form the	
B01	(BO3E44)	MTC	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*B01	(BO3E34)	
B02	(BO3H44)	
*B02	(BO3H34)	
В03	(BO3L44)	Indicates individual contents of 8
*B03	(BO3L34)	bits from 0 to 7 of Bus Out signal from the MTC
B04	(BO3B94)	
*B04	(BO3B84)	
B05	(BO3E94)	
*B05	(BO3E84)	
B06	(BO3H94)	
*B06	(BO3H84)	
B07	(BO3L94)	
*B07	(BO3L84)	·
BRUN	(SN1G34)	Indicates that capstan motor is rotating backward
BUSEN	(B13Q34)	Indicates that Bus In and Bus Out are
*BUSEN	(B13P24)	enabled
	(320121)	
BUSØØ′	(RG1B24)	
BUSØ1	(RG1B25)	Indicates individual contents of bus bits of a register file
BUSØ2	(RG1B26)	
BUSØ3	(RG1B27)	
BUSØ4	(RG1C24)	
BUSØ5	(RG1C25)	
BUSØ6	(RG1C26)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
BUS07	(RG1C27)	
BUS10	(RG1B64)	
BUS11	(RG1B65)	
BUS12	(RG1B66)	
BUS13	(RG1B67)	
BUS14	(RG1C64)	
BUS15	(RG1C65)	
BUS16	(RG1C66)	
BUS17	(RG1C67)	
BUS20	(RG1BX4)	Indicates individual contents of bus bits
BUS21	(RG1BX5)	of a register file
BUS22	(RG1BX6)	
BUS23	(RG1BX7)	
BUS24	(RG1CX4)	
BUS25	(RG1CX5)	
BUS26	(RG1CX6)	
BUS27	(RG1CX7)	
BUS3Ø	(RG2D24)	
BUS31	(RG2D25)	
BUS32	(RG2D26)	
BUS33	(RG2D27)	
BUS34	(RG2F24)	
BUS35	(RG2F25)	
BUS36	(RG2F26)	
BUS37	(RG2F27)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
BVLF	(TK2BX4)	Directs the drive of power amplifier for file reel
BVLM	(TK2CX6)	Directs the drive of power amplifier for machine reel
BWD	(RG1G25)	Indicates that the MTU is in the backward status
CAPGO	(RG1L25)	GO signal used in the MTU
CARY	(AL1GY2)	Indicates the content of carry bit of the calculated result in the arithmetic logic unit (ALU)
СВІЙ	(BI2B54)	
CBI1	(BI2F54)	
CBI2	(BI2H54)	
CBI3	(BI2M54)	Indicates individual contents of 8 bits
CBI4	(BI2BX4)	of Bus In signal to the MTC
CBI5	(BI2FX4)	
CBI6	(BI2HX4)	
CBI7	(BI2MX4)	
*CB0&	(BOIB24)	
*CB01	(BOIC24)	
*CBO2	(BOID24)	Indicates individual contents of 9 bits of Bus Out signal to the MTC
*CB03	(BOIH24)	
*CBO4	(BOIJ24)	
*CB05	(BOIK24)	
	<u> </u>	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*CB06	(BOIB64)	
*CB07	(BOIC64)	Indicates individual contents of 9 bits
		of Bus Out signal to the MTS
CB08	(BOID74)	
*CB08	(BOID64)	
ccs	(TK2N26)	Indicates the magnitude of capstan motor current
CCTL	(B01J74)	Control tag signals from the MTC
*CCTL	(BO1J64)	
CEN	(RW1N74)	Directs the drive of address counter
*CEON	(CE1J54)	Indicates that maintenance panel is connected to the MTU
CERST	(BO2P64)	Error Reset signal from the MTC
cco	(B01K74)	·
*CGO	(BO1K64)	Go tap signal from the MTC
*CGOPN	(VQ1A24)	Cartridge open signal
CGRLY	(TK2A64)	Directs the drive of cartridge drive relay
*CLINF	(TK2D24)	Column In signal (File reel, machine reel)
*CLINM	(TK2D25)	
CLNDV	(RG1F64)	
*CLNDV	(CB1E34)	Auto cleaner drive signal
CLOCK	(RW5F24)	1-MHz clock

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*CLR	(RM3N45)	Directs the MTU to clear its entire logical circuit network
CNIMD	(RG3H24)	Count mode signal
CNT1	(RW4B34)	Indicates the content of control counter
CNT2	(RW4B35)	specifying either serial or parallel control
CNØ	(RG3N47)	
CN1	(RG3N46)	
CN2	(RG3N45)	
CN3	(RG3N44)	Indicates individual contents of 8 bits of a counter
CN4	(RG3K47)	or a counter
CN5	(RG3K46)	
CN6	(RG3K45)	
CN7	(RG3K44)	
CPA	(SN1C34)	Specifies either capstan tachometer A
СРВ	(SN1D34)	or B
*CPLOK	(TK1C24)	Directs filter switching
CSF	(TK2PX4)	Indicates the magnitude of file reel motor current
CSLO	(RG1GX6)	Specifies the number of steps for
CSL1	(RG1GX7)	counter
CSM	(TK2NX4)	Indicates the magnitude of machine reel motor current

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
CSTS	(BO1H74)	Status Tag signal from the MTC
*CSTS	(BO1H64)	
CSVON	(TK1B34)	Makes servo control of capstan motor effective
*CSVON	(TK1B24)	
CTA	(SN1C52)	Capstan tach signal synchronized with
CTB	(SN1C56)	clock signal
CIGCL	(TK1H34)	Cartridge Close signal
CIGCL	(RG1E66)	Carcifuge Close Signal
CTGON	(VQ1A23)	Cartridge On signal
OIGGN	(V&IAZO)	Calcifuge on Signal
CIL	(B03P84)	
CTLTG	(B02C54)	Control Tag signal from the MTC
	(57.000)	
CTPA	(TK2A23)	
CTPB	(TK2A24)	Capstan tach signals A/B
C1024	(RG3N76)	Indicates that the contents of the upper bit of counter is 1024
C200U	(CL1J74)	Clock with a cycle of 200 us
C256	(RG3N74)	
C512	(RG3N75)	Indicates that individual contents of the upper bits of counter are 256, 512, 2048, and 4095, respectively
C2048	(RG3N77)	Jiz, zpio, and ipjo, respectively
C4Ø95	(RG3P74)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
DAC	(TK2N25)	Indicates the magnitude of output voltage of D/A converter
DAC1	(RG1K67)	
DAC2	(RG1K66)	
DAC4	(RG1K65)	Indicates individual contents of 5
DAC8	(RG1K64)	bits to D/A converter
DAC16	(RG1J67)	
DBOB	(RW3F34)	Indicates that a data block is detected
DBUSO	(MX3B32)	
DBUS1	(MX3B34)	
DBUS2	(MX3B36)	
DBUS3	(MX3C32)	
DBUS4	(MX3C34)	Indicates individual contents of Data Bus signals to the arithmetic logic
DBUS5	(MX3C36)	unit (ALU)
DBUS6	(MX3E32)	·
DBUS7	(MX3E34)	
DDF	(RW4M64)	Indicates that the MTU is a dual— density unit
DEGUS	(RW1G84)	Degauss signal
DGO	(RW2L94)	Go signal
DIAG	(RG1EX5)	Indicates that the MTU is in
*DIAG1	(TK1M24)	diagnostic mode
DIBG	(RW3F33)	Indicates that IBG is detected

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
DNOIS	(RW3F35)	Indicates that a noise block is detected
*DOPEN	(CB1P66)	Indicates that door open is detected
DOPN	(CB1Q84)	
*DRCLS	(TK2E26)	Indicates that the door is closed
DSE	(RG1K25)	Indicates that the data security erase operation is being carried out
*DSPCL	(CL1G94)	
*DSPCL	(CL1GX4)	1-MHz clock
DTM	(RW3F32)	Indicates that tape mark block is detected
*DTUCK	(AA1C66)	Tape Unit Check Signal
*ECDCL	(MX3L64)	Directs the MTU to indicate an error code
ECDSP	(MX3N44)	
ECDØ	(RG1L64)	
ECD1	(RG1L65)	
ECD2	(RG1L66)	
ECD3	(RG1L67)	Indicates individual contents of 8
ECD4	(RG1M64)	bits of an error code
ECD5	(RG1M65)	
ECD6	(RG1M66)	
ECD7	(RG1M67)	
ECER	(RW1E64)	Indicates that the erase circuit fails

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*ECHCL	(RW1CY4)	Clock for checking the erase circuit
ECON	(RW4G64)	Directs the MTU to put on the erase current
ECO	(BI4F94)	
EC1	(BI4E94)	Indicates individual contents of 4
EC2	(BI4D94)	bits of EC level signal
EC3	(BI4C94)	
EMKDV	(RG1E65)	
*EMKDV	(TK1F34)	Error Marker Drive signal
EMKPW	(TK2A66)	
*EMMVD	(VQ1B23)	Directs the MTU to check the error marker operation
ENITR	(B14K94)	Indicates that interrupt is enabled
*ENLVL	(RW6D44)	Directs the MTU to set a slice level from an external unit
EOT	(SN1L44)	Indicates that the end of tape (EOT) marker is detected
EOT	(TK2B23)	
EQL1	(AL1D37)	
EQL2	(AL1D37)	Indicates that values compared through
EQUAL	(AL1GY5)	the execution of a compare instruction at the ALU are equal to each other
*ERON	(RW5E24)	Directs the MTU to set the erase current

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
ERRST	(RG1H24)	
*ERRST	(AA1L34)	Directs the MTU to reset an error
*ERRST	(AA1J24)	
ERSC	(RG1LX6)	Directs the MIU to set the erase current
*ERSP	(B12P64)	Gate condition for sense information
*ESLVØ	(RW6B74)	
*ESLV1	(RW6C74)	
*ESLV2	(RW6D74)	
*ESLV3	(RW6E74)	Indicates individual contents of 8
*ESLV4	(RW6F74)	bits of a slice level set signal from an external unit
*ESLV5	(RW6G74)	
*ESLV6	(RW6H74)	
*ESLV7	(RW4D85)	
*ESTDL	(RG4Q34)	Capstan tach signal synchronized with clock signal
EVEN	(AL1M94)	Indicates the content resulting from parity checking for ROM data
*FCCWN	(TD1EX4)	Drives the file reel motor counter clockwise
2 3 3 112	,/	
*FCWN	(TD1CX4)	Drives the file reel motor clockwise
FCWP	(TD1BX4)	Drives the file reel motor clockwise
*FDRUN	(TK1D24)	Indicates that capstan motor is rotating in the forward direction

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*FFRST	(AA1P94)	Directs the MTU to reset the unit check
FGO	(AA2F34)	Forward Go signal
FILE	(RG1FX7)	Indicates that the skip file operation is being executed
FP	(BI1E34)	File Protect signal
FP	(RW5F55)	
FPK	(CB1N84)	Indicates the state of (PROTECT) switch on the operating panel
*FPK	(CB1DX6)	
FPLP	(CB1F84)	Turns on (PROTECT) LED
FRBWD	(RG5G94)	Indicates that the file reel is rotating backward when the MTU is in the servo off status
FRFWD	(RG5G92)	Indicates that the file reel is rotating in the forward direction
FRUN	(SN1F34)	Indicates that capstan motor is rotating in the forward direction
FTP-A	(RG2MY6)	
*FTPA	(SN1GY4)	Indicates that one cycle of this signal is equal to 4 QTP of capstan
*FTPB	(SN1HY4)	tachometer pulse
FVLF	(TK2BX#)	Directs the MTU to drive the power amplifier for file reel
FVLM	(TK2CX5)	Directs the MTU to drive the power amplifier for the machine reel

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
FW	(SN1C96)	Indicates that capstan motor is rotating in the forward direction
FWD	(SN1C96)	Forward Status signal
FWD	(BI2G24)	
GAPCT	(RG3J94)	Gap Control Signal
GAPEN	(RG1EX6)	Signal to control the gap control
GCR	(RW3E54)	Specifies the Group Coded Recording mode
GND	(RM3B24)	ov
GO	(RW5H24)	
GO	(B12N24)	
GO	(B02D54)	Go signal
GO	(B02E64)	
GOB	(RW3C94)	
*HDER	(RW1K74)	Indicates that parity error occurs in the ROM or in the register file large—scale integration
*HIC	(RW3B74)	Directs the MTU to put on the high current
*HIC	(RB3B64)	
HID	(BI1E74)	Indicates that the MTU is in the high—density mode
HRDER	(RW1K84)	Indicates that parity error occurs in the ROM or in LSI

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*HSBRK	(TK2LX3)	Indicates that file reel motor brake is applied during high-speed operation
HSC	(RG1LX7)	Indicates that the tape is running at aspeed greater than 200 ips
HSCF	(TK2DX4)	Specifies the upper limit of capstan speed in response to the reel during high-speed rewinding
HSCM	(TK2DX5)	
HSMD	(RG1MX6)	Indicates that the tape is running in the high-speed mode
*HSP	(TD1A84)	This signal is kept in the on stage until the low tape is detected during rewinding
HSRUN	(RG1L24)	
HUBAL *HUBLK	(AA1G64) (TK2D26)	Indicates that the auto hub has been locked
*INHCK	(AA1FX4)	Gate signal for the Alarm signals
INRST	(TK1C74)	Put on initial reset
*INRST	(TK1CX4)	
INSTL	(PG1EX4)	PCA Installed signal
INTRP	(AA2B74)	Interrupt signal to the MTC
*ISTLP	(VQ1C25)	Indicates that the PCA has been connected

APPENDIX B SIGNALS IN LOGIC CIRCUITS

	IGNALS IN LOGIC	
Nickname	Pin-Index	Description
*JMPOK	(MX3E36)	Gan Mild and I down addess I
*JUMP	(MX1KY4)	Conditional jump signal
		·
KCNT	(CE1D56)	(CNT) switch on the maintenance panel
*KCNT	(CE1C56)	
KOFL	(CE1B56)	(OFL) switch on the maintenance panel
*KOFL	(CE1B54)	
KSSS	(CE1D54)	(SSS) switch on the maintenance panel
*KSSS	(CE1C54)	(SSS) Switch on the maintenance panel
KT	(RG5D92)	Capstan start signal
*LDCLK	(RW4B54)	Clock for setting the sense
	(information sent from the read circuit network
		CITCUIT Network
LDCMD	(AL1H23)	LOAD instruction
LDFL	(BI1J74)	Signal to inform the MTU that tape
		loading fails
LDRK	(CB1J84)	Indicates the state of (LOAD REWIND)
		switch on the operating panel
*LDRK	(CB1FX6)	
LEDØ	(MX3BY4)	
LED1	(MX3BY6)	Drives individual luminescent diodes
LED2	(MX3CY4)	for indicating the states of the corresponding switches on the
LED3	(MX3CY6)	maintenance panel
LED4	(MX3FY4)	
	<u> </u>	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
LED5	(MX3FY6)	
LED6	(MX3GY4)	
LED7	(MX3GY6)	
LED8	(MX3KY4)	Drives individual luminescent diodes for indicating the states of the
LED9	(MX3KY6)	corresponding switches on the maintenance panel
LED1&	(MX3LY4)	
LED11	(MX3LY6)	
F T1774	(1/04/00 4)	
LINE1	(VQ1G24)	
LINE2	(VQ1F26)	
LINE3	(VQ1G25)	
LINE4	(VQ1P25)	Not used at present
LINE5	(VQ1P26)	
LINE6	(VQ1Q23)	
LINE7	(VQ1Q25)	
LOAD	(RG1FX6)	Indicates that auto loading is being executed
LOCK	(RGIJ64)	Signal to control the stop position of capstan
LSF	(TK2PX5)	Indicates the magnitude of capacitive sensor output voltage for the column on the file reel side
LSM	(TK2NX6)	Indicates the magnitude of capacitive sensor output voltage for the column on the machine reel side
LTLAL	(AA1H64)	Alarm signal for left column

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
LTP	(AA1D74)	Low tape detecting signal
LTPAS	(RG1L26)	
	(= a, = a,)	
LVLTØ	(RG1J24)	
LVLT1	(RG1J25)	
LVLT2	(RG1J26)	
*LVL1	(RW2B82)	
*LVL16	(RW4D82)	
*LVL2	(RW4B83)	Specifies slice levels
*LVL32	(RW4D83)	
*LVL4	(RW4B84)	
*LVL64	(RW4D84)	
LVL65	(RG5P96)	
*LVL8	(RW4B85)	
LVL90	(RG5Q92)	
	_	
LWR	(RG5H42)	
*LWR	(RO2E44)	Loop Write-to-Read signal
LWRGO	(BO2M64)	
LWR2	(RG5H45)	
LWSL	(RG1LX4)	Low slice signal to direct the MTU to
*LWSL	(RW4C54)	set the slice level to 7%
	(14004)	
LWIP	(TK2B24)	Indicates that low tape detected
*MARGN	(VQ1NY4)	Directs the MTU to execute the margin test

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
MASK	(RG1HX7)	Directs the MTU to inhibit interrupt to the microprogram
*MCCWN	(TD1MX4)	Directs the MTU to drive machine reel counterclockwise
MCCWP	(TDINX4)	000,10020200,11120
*MCWN	(TD1KX4)	Directs the MTU to drive machine reel
MCWP	(TD1JX4)	clockwise
MDOØ	(RM3NX4)	
MDØ1	(RM3MX4)	
MDØ2	(RM3LX4)	
MDØ3	(RM3KX4)	
MDØ4	(RM3JX4)	
MDØ5	(RM3HX4)	
MD Ø 6	(RM3GX4)	
MDØ7	(RM3FX4)	
MDØ8	(RM3EX4)	Indicates individual contents of 24 bits of memory data
MDØ9	(RM3DX4)	
MD1Ø	(RM3CX4)	
MD11	(RM3BX4)	
MD12	(RM3N74)	
MD13	(RM3M74)	
MD14	(RM3L74)	
MD15	(RM3K74)	
MD16	(RM3J74)	
MD17	(RM3H74)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
MD18	(RM3G74)	
MD19	(RM3F74)	
MD2Ø	(RM3E74)	Indicates individual contents of 24
MD21	(RM3D74)	bits of memory data
MD22	(RM3C74)	
MD23	(RM3B74)	
MISCE	(RG5B54)	Miscellaneous Error signal to be set by the microprogram
MMET	(TK2B64)	
*MMET	(TK2B64)	Drives the moving meter
*MMTDV	(TK1N24)	
MOD	(AL1G26)	Control signal for the arithmetic logic unit (ALU)
MPXA	(B02K64)	Specifies sense information for Bus In
MPXB	(B02L64)	
MPX\06	(RM2C84)	
MPXQ7	(RM2B86)	Specifies the jump condition of register file
MPXØ8	(RM2B84)	
MPXØ9	(RM2C86)	
MPX1	(BI1KX2)	Specifies sense byte
MPX1Ø	(RM2M34)	Specifies the jump condition of register file

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
MPX2	(BI1KX3)	Specified sense byte
MPX4	(BI1KX4)	
MRBWD	(RG5H92)	Signal issued when the MTU is in the servo off status to direct the MTU to rotate the machine reel in the backward direction
MRFWD	(RG5G96)	Signal issued when the MTU is in the servo off status to direct the MTU to drive machine reel in the forward direction
*MRSLW	(TK2K94)	Directs the MTU to drive machine reel motor at low speed
*M6ALM	(VQ1C23)	Alarm signal for the -6V stabilizing circuit
NCLF	(TK2AX4)	Directs the MTU to drive the power amplifier for the file reel
NCLM	(TK2CX3)	Directs the MTU to drive the power amplifier for machine reel
NEWF	(BI4H94)	Specifies the MTU having the streaming function or the skip file function
NRZI	(BO2J54)	Sets the MTU in the Non Return to Zero Change on One (NRZI) mode
OD .	(SN1CX4)	Indicates that capstan runs in the direction opposite the Status signal
ODD	(AL1M96)	Indicates the content resulting from parity checking from ROM data

APPENDIX B SIGNALS IN LOGIC CIRCUITS

<u>Nickname</u>	Pin-Index	Description
ONL	(AA1C62)	Indicates that the MTU is in the online status
*ONL	(AA1C63)	
ONLK	(CB1K84)	Indicates the state of (ONLINE) switch on the operating panel
*ONLK	(CB1EX5)	
OPTNØ	(MX2M34)	
OPIN1	(MX2N34)	Indicates the content of the specified option
OPTN2	(MX2P34)	
OPTN3	(MX2Q34)	
OVCF	(TK2AX6)	Specifies the upper limit of the maximum current to file reel motor
OVCM	(TK2CX4)	Specifies the upper limit of the maximum current to machine reel motor
PCLF	(TK2KX5)	Directs the MTU to drive the power amplifier for file reel
PCLM	(TK2BX5)	Directs the MTU to drive the power amplifier for machine reel
PDTO	(RG1JX4)	
PDT1	(TG1JX5)	
PDT2	(RG1JX6)	Preset data signals for Timer 0
PDT3	(RG1JX7)	
PDT4	(RG1KX4)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
PDT5	(RG1KX5)	
PDT6	(RG1KX6)	Preset data signals for Timer Ø
PDT7	(RG1KX7)	
PE	(RG1H27)	Sets the MTU in the Phase Encode mode
POWAL	(CB1B54)	Turns on (ALARM) lamp on the operating board
PRSET	(RG5Q96)	Directs the MTU to reset the counter for DGC amplifer control
PRSVL	(RG1F66)	Drives the pressure valve
PTYCL	(CL1B94)	1-MHz clock
PWRDY	(TK2B25)	Indicates that power supply is ready
PWRDY	(TK1C64)	
P1US	(CL1C66)	Clock to divide a frequency of 8 MHz
P250N	(CL1C64)	
*P5ALM	(VQ1B24)	Alarm signal for +-5V stabilizing circuit
Р5фри	(CL1C65)	Clock to divide a frequency of 8 MHz
QIP	(SN1F74)	Quarter Tach Pulse signal
RAMON	(RM1Q74)	Indicates that the RAM is connected to an external device
*RAMON	(RE3E47)	to all excellial device

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
RD	(SN1H24)	Read Status signal
RDINH	(RG5P92)	Directs the MTU to inhibit sending the read data
RDST	(RW1E24)	Indicates that the MTU is in the read status
RDT ø	(RW5M54)	
RDT1	(RW5L56)	
RDT2	(RW5L54)	
RDT3	(RW5K56)	
RDT4	(RW5K54)	Indicates individual contents of 9
RDT5	(RW5J56)	bits of read data
RDT6	(RW5J54)	
RDT7	(RW5H56)	
RDT8	(RW5H54)	
RDYHL	(RG5G42)	Indicates that ready signal to set
RDYLP	(CB1B84)	Directs the MTU to turn on (READY) lamp on the operating panel
READ	(BI2P34)	Output gate signal for read data
READ	(BI2N34)	•
READY	(RG1EX7)	Indicates that the MTU is in the ready status
*RESET	(RW5L24)	Directs the MTU to result the counter for the DGC amplifier control

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
RGB0	(MX1#84)	
RGB1	(MX1F84)	
RGB2	(MX2E24)	
RGB3	(MX2F24)	Indicates individual contents of 8
RGB4	(MX2E64)	bits of output bus of register file large—scale integration (LSI)
RGB5	(MX2F64)	
RGB6	(MX2EX4)	
RGB7	(MX2FX4)	
RGPE	(RW1L64)	
RGPE0	(RG1N24)	Indicates individual contents of
RGPE1	(RG1N64)	parity errors in register file LSI
RGPE2	(RG1NX4)	·
*RGW	(RG2K34)	Directs the MTU to write the content of general register
RLACT	(RG1J27)	Indicates that capstan is in operation
*RLPWR	(TK1Q74)	Directs the MTU to make the reel motor drive mechanism effective
*RLSLW	(TKI1P74)	Directs the MTU to drive file reel motor at low speed
RLSTP	(RG1M26)	Indicates that reel motor is in halt
*RLSTP	(TK1K24)	
*RNOIS	(RG4G34)	Directs the MTU to reset the Noise Block Detect signal
ROMCK	(RW1N64)	Parity error signal for the ROM

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
ROMOK	(RW1Q64)	Parity OK signal for the ROM
*ROMOK	(RW1Q66)	ratity of signal for the non-
ROMPE	(RW1K64)	Parity error signal for the ROM
ROMØØ	(RM1N85)	
ROMØ1	(RM1N84)	
*ROMØ2	(RM1P94)	
ROMØ3	(RM1N82)	
ROMØ3	(RM1NY4)	
ROM ∮ 4	(RM1M85)	
ROMØ5	(RM1M84)	
ROM@5	(RM1LY4)	
ROMØ6	(RM1M83)	
ROMØ7	(RM1M82)	
ROMØ8	(RM1H85)	
ROMØ9	(RM1H84)	
ROM10	(RM1H83)	Indicates individual contents of 24
ROM11	(RM1H82)	bits of ROM data.
ROM12	(RM1G85)	
ROM13	(RM1G84)	
ROM14	(RM1G83)	
ROM15	(RM1G82)	
ROM16	(RM1C85)	
ROM17	(RM1C84)	
ROM18	(RM1C83)	·

APPENDIX B SIGNALS IN LOGIC CIRCUITS

APPENDIX B SI	GNALS IN LOGIC	CIROUID
Nickname	Pin-Index	Description
ROM19	(RM1C82)	
ROM2Ò((RM1B85)	Indicates individual contents of 24
ROM21	(RM1B84)	bits of ROM data.
ROM22	(RM1B83)	
ROM23	(RM1B82)	
RPWR	(RG5H94)	Directs the MTU to make the reel motor drive mechanism effective
RSPB	(AA1N94)	
RSTK	(CB1M84)	Indicates the state of (RESET) switch on the operating panel
*RSTK	(CB1EX6)	• • • • • • • • • • • • • • • • • • •
RSTKS	(AA1M82)	
RSVSW	(RG1M27)	Directs the MTU to make servo control of reel motor effective
*RSVSW	(TK1L24)	
RTLAL	(AA1J64)	Alarm signal for right column
*RTSFL	(RG4P34)	Reset signal upon completing the maintenance panel operation
*RUCHL	(RG4H34)	Directs the MTU to reset the unit check signal
RVSL	(RG1L27)	Indicates that a predetermined time passes after capstan motor stopped
RWD.	(RG1K26)	Indicates that the rewind operation is in execution
SAGC	(RG5M96)	Indicates that the MTU is in the Self-Adjust Gain Control mode

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
SAGCÒ	(RW4K62)	
SAGC1	(RW4J66)	Indicates individual contents of 4
SAGC2	(RW4J64)	bits of count information in AGC counter
SAGC3	(RW4J62)	
*SBIQ	(BI1B36)	
*SBI1	(BK1F36)	·
*SBI2	(BI1K36)	
*SBI3	(BI1B66)	Indicates individual contents of 8
*SBI4	(BI1F66)	bits of sense byte
*SBI5	(BI1K66)	
*SBI6	(BI1B96)	
*SB17	(BI1F96)	
SBOT	(SN1D54)	Indicates that beginning of tape (BOT) is detected
*SBYT	(BI3G64)	Gate signal for the sense byte output signal
SCONT	(RW5G24)	Directs the MTU to control the serial/parrallel transmission
SDF	(TK2PX6)	Directs the MTU to drive file reel
SDM	(TK2NX3)	Directs the MTU to drive machine reel
SECON	(RW4Q34)	Directs the MTU to set the erase current on
SEMK	(RG1K24)	Directs the MTU to stamp the error mark

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*SENS	(BO2F64)	Gate signal for the sense byte output
SEOT	(SN1D56)	Indicates that end of tape (EOT) is detected
SERS	(RG1G24)	Indicates that the MTU is in the erase mode
SET	(RG5Q94)	Directs the MTU to inhibit the operation of the counter for the DGC amplifier control
*SET	(RW5N24)	
SETP2	(RG4K34)	
SETP3	(RG4134)	Pulse signals for setting
SETP5	(RG4N34)	
SFBLS	(CB1P84)	Indicates whether or not the window safety mechanism operates (* = not operational)
*SFBLS	(TK2L63)	
SHBOT	(RG1FX5)	Indicates that the processing for detecting the BOT is in execution
*SIGN	(RG1J66)	Signal for switching the polarity of D/A converter
SIN	(RW4KY4)	Indicates the content of the parallel serial transmission of data to the write/read printed-circuit assembly
SIRPT	(RG4M34)	Indicates the condition for setting an interrupt signal

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
SKIPF	(BI4J94)	Indicates that the MTU is provided with the skip file function
SLOW	(RG5H96)	Directs the MTU to drive the reel at low speed
*SLS0	(MX1L34) (MX1M34)	Specifies the jump condition for register file
	(MXLM34)	
SOUT	(RW5F57)	Indicates the paralle/serial trans- mission data from write/read printed- circuit assembly
SPOS	(RG1MX4)	Positioning control signal for capstan
*SSSON	(CE1LX4)	Indicates the state of (SSS) switch on the field tester
SSTEP *SSTEP	(RG5P94) (RW5P24)	Clock signal for the counter for the DGC
STBIØ	(BI5DY4)	
STBI1	(BI5DY6)	
STBI2	(BI5EY4)	
STB13	(BI5EY6)	Indicates individual contents of 8
STB14	(BI5HY4)	bits of the Bus In signal to be issued when the MTU receives the
STB15	(B15HY6)	Status Tag signal
STB16	(BI5JY4)	
STB17	(BI5JY6)	
STEP6	(RW4F62)	Indicates that the number of the steps of the counter for the DGC amplifier control is 6

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
STPCK	(RG5D94)	Directs the MTU to check the position control when capstan stops
STRMD	(RG1FX4)	Directs the MTU to set the streaming mode
STRMD	(RG1H25)	
STRMF	(RW4K64)	Indicates that the MTU is provided with the streaming mode function
*STRST	(AA2D64)	Directs the MTU to reset the error detecting circuit
STS	(BO2B54)	Status Tag signal
SUCHL	(AA1CX4)	Sets the unit check holding signal
SVOK	(RG1M24)	
*SVOK	(SN1P44)	Directs the MTU to set reel/capstan motor in the servo control state
SVON	(RG1M25)	
SWCER	(RW1E74)	Alarm signal for the write and erase circuits
SWCON	(RW4P34)	Directs the MTU to set the magnitude of the write voltage
SWRS	(RG1G27)	Indicates the write status
*SWRS	(RS1G74)	
SW Ø	(CE1NY6)	
SWØ	(MX3H94)	Indicates individual contents of 8
*SWØ	(CE1NY5)	switches 0-7 on the field tester
*SWØ	(CE1H54)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
SW1	(CE1NY3)	
*SW1	(CE1NY2)	
*SW1	(CE1H56)	
SW2	(CE1MY6)	
*SW2	(CE1G56)	
SW3	(CE1MY3)	
*SW3	(CE1G54)	To Marchael 1991 1991
SW4	(CE1KY6)	Indicates individual contents of 8 switches 0-7 on the field tester
*SW4	(CE1F56)	
SW5	(CE1KY3)	
*SW5	(CE1F54)	
SW6	(CE1JY6)	
*SW6	(CE1E56)	
SW7	(CE1JY3)	
*SW7	(CE1E54)	
SØ	(AL1G22)	
S1	(AL1G23)	Signals for arithmetic logic unit
S2	(AL1G24)	(ALU) control
S3	(AL1G25)	
*TAGIN	(B13F83)	Indicates that Tag signals from the MTC are normal
TEST	(CE1QX4)	Indicates the content of (SSS) switch on the field tester
TGPE	(BO2B34)	Indicates the content resulting from parity check for Tag and Bus out
*TGPE	(BO2B36)	partity check for tay and bus out
		,

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*THALM	(VQ1C24)	Termpreature alarm signal for power supply circuit
TIDØ	(BI4K64)	
TID1	(BI4J64)	
TID2	(BI4H64)	
TID3	(BI4G64)	Indicates individual contents of 13 bits for unit number setting
TID4	(BI4F64)	bits for wife homber secting
TID5	(BI4E64)	
TID6	(BI4D64)	
TID7	(BI4C64)	
TID8	(BI4K34)	
TID9	(BI4J34)	
TID1Ø	(BI4H34)	
TID11	(BI4G34)	
TID12	(BI4F34)	
*TLV1	(RW6B34)	
*TLV16	(RW6C35)	
*TLV2	(RW6B36)	Indicates individual contents of 7
*TLV32	(RW6C36)	bits for slice level setting from an external device
*TLV4	(RW6B37)	
*TLV64	(RW6C37)	
*TLV8	(RW6C34)	
TM	(RG5D45)	Indicates that a tape mark block is detected

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
TMOD	(RG5G45)	Indicates that the MTU is in the test mode
™OV¢	(RG2MY4)	Indicates that timer overflows
TMOV1	(RG3E94)	
TMSRØ	(RW5M57)	
TMSR1	(RW5M55)	
TMSR2	(RW5L57)	
TMSR3	(RW5K57)	
TMSR4	(RW5K55)	Indicated that the smalltude of the
TMSR5	(RW5J57)	Indicates that the amplitude of the read data reaches a predetermined
TMSR6	(RW5J55)	value
TMSR7	(RW5H57)	
TMSR8	(RW5G57)	
тмфф	(RG2KY6)	
TMØ1	(RG2KY4)	
TMØ2	(RG2JY6)	
тмøз	(RG2JY4)	
TMØ4	(RG2DY6)	Indicates individual contents of 8 bits of timer Ø
TMØ5	(RG2DY4)	DICE OF CHIEF A
тмø6	(RG2CY6)	
TMØ7	(RG2CY4)	
TM1Ø	(RG3G47)	
TM11	(RG3G46)	Indicates individual contents of 8
TM12	(RG3G45)	bits of timer 1
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APPENDIX B SIGNALS IN LOGIC CIRCUITS

APPENDIX B S.	IGNALS IN LOGIC	Oliootis
Nickname	Pin-Index	Description
TM13	(RG3G44)	
TM14	(RG3D47)	Indicates individual contents of 8
IM15	(RG3D46)	bits of timer 1
IM16	(RG3D45)	
IM17	(RG3D44)	
TOVRN	(RG5E42)	Indicates that no block is detected within a predetermined distance
TP	(SN1K34)	Indicates that the tape is present in the tape transmission mechanism
TSBØ	(MX4B34)	
TSB1	(MX4F34)	
TSB2	(MX4K34)	
TSB3	(MX4B74)	
TSB4	(MX4F74)	Indicates individual contents of 8
TSB5	(MX4K74)	bits of register files or test signals
TSB6	(MX4BY4)	
TSB7	(MX4FY4)	
*TSCL	(RW2B74)	Clock for write data composition
TSFL	(CE1M95)	Indicates that the maintenance panel is in use
TSL ø ø	(RG1HX4)	
'TSL1Ø	(RG1GX4)	Specifies the number of steps for
TSL11	(RG1GX5)	timer Ø and 1

APPENDIX B SIGNALS IN LOGIC CIRCUITS

	Din Indox	
<u>Nickname</u>	Pin-Index	Description
TST	(CE1M92)	Indicates the state of (SSS) switch on the field tester
*TST	(CE1M93)	
TUCHK	(AA1F84)	
TUCK	(BI5G94)	Indicates that failure of MTU is detected
TUERR	(AA1E64)	
AWT	(SN1L64)	Indicates that end of tape (EOT) is detected when the tape runs in the forward direction
IWRCL	(RW2GY4)	Write clock and write data from the maintenance panel
TWRDT	(RW2F94)	
T1US	(CL1D74)	Pulse signal with a cycle of 1 μ s
TI6US	(RW4C34)	Pulse signal with a cycle of 16 , s
U-SPØ	(RG4C34)	
U-SP1	(RG4D34)	Indicates individual contents of the upper 4 bits of the Set Pulse signal
U-SP2	(RG4E34)	apper 4 5105 of one see fatter signal
*USP3	(RG4F34)	·
UCHLD	(AA1DX4)	Directs the MTU to set the unit check signal in the holding state
*UCHLD	(AA1DX6)	
UCK	(AA1B94)	Indicates that failure of the MTU is detected
UCK	(AA1E84)	
	+	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

	IGNALS IN LOGIC	
Nickname	Pin-Index	Description
UCKLP	(CB1D84)	Directs the MTU to turn on (UNIT CHECK) lamp
UCKLP	(RG1E64	(Only Salott) Lang
UNL	(RG1E64)	Indicates that unloading is in execution
UNLK	(CB1L84)	Indicates the state of (UNLOAD) switch on the operating panel
UNLK	(CB1FX4)	switch on the operating paner
*VALVA	(CB1B34)	Directs the MTU to drive the valve
*VALVB	(CB1C34)	
VELØ	(RW4K66)	Specifies the unit speed
VEL1	(RW4M62)	
VSF	(TK2NX5)	Indicates the detected magnitude of the file reel motor voltage
VSM	(TK2MX5)	Indicates the detected magnitude of the machine reel motor voltage
V ó	(RM3F44)	
V1 .	(RM3F45)	
V1Ø	(RM3H47)	
V11	(RM3H47)	
V12	(RM3J45)	Indicates individual contents of 24 data bits issued when the RAM is
V13	(RM3J46)	connected with an external device
V14 _.	(RM3J47)	
V15	(RM3K44)	
V16	(RM3K45)	·
V17	(RM3K46A)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
V18	(RM3K47)	
V19	(RM3L44)	
V2	(RM3F46)	
V2ø	(RM3L46)	
V21	(RM3L47)	
V22	(RM3M44)	,
V23	(RM3M45)	Indicates individual contents of 24
V3	(RM3F47)	data bits issued when the RAM is connected with an external device
V4	(RM3G44)	
V5	(RM3G45)	
V6	(RM3G46)	
V7	(RM3G47)	
V8	(RM3H44)	
V9	(RM3H46)	
WCER	(RW1D64)	Indicate failure in the write circuit
*WCHCL	(RW1BY4)	Clock signal for checking the write operation
*WDCLS	(TK2K65)	Indicates that the window has been closed
WDTØ	(RW2K34)	
WDT1	(RW2K36)	
WDT2	(RW2L34)	Indicates individual contents of 9 bits of write data
WDT3	(RW2L36)	DICS OF WELLE data
WDT4	(RW2K64)	·
WDT5	(RW2K66)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
WDT6	(RW2L64)	
WDT7	(RW2L66)	Indicates individual contents of 9
WDT8	(RW2K94)	bits of write data
WKSL 0	(RG1HX5)	Specifies a work register
WKSL1	(RG1HX6)	
WK ØØ	(RG1E24)	
WKØ1	(RG1E25)	
WKØ2	(RG1E26)	
WK Ø 3	(RG1E27)	
WK 0 4	(RG1F24)	Sets individual bits of the work
WKØ5	(RG1F25)	register
₩K Ø 6	(RG1F26)	
WKØ7	(RG1F27)	
WK58 0	(RG4C84)	
WK581	·	
	(RG4C85)	
WK582	(RG4C86)	
WK583	(RG4C87)	
WK584	(RG4F84)	Sets individual bits of the work registers 5-8
WK585	(RG4F85)	-
WK586	(RG4F86)	
WK5 <u>8</u> 7	(RG4F87)	
WNDCL	(RG1E67)	Directs the MTU to close the window
*WNDCL	(TK1P24)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
WPOS	(RG1MX5)	Directs the MTU to carry out positioning control on the write operation
WRCL	(BO1BY4)	Write Clock signal
*WRIST	(RW4F64)	Indicates that the write/read printed-circuit assembly has been connected
WRTC	(RG1LX5)	Write voltage setting signal
WRTCL	(RW2K96)	Write clock signal
*WSELØ	(RM2F83)	
*WSEL1	(RM2F84)	
*WSEL2	(RM2F85)	
*WSEL3	(RM2F86)	
*WSEL5	(RM2G83)	
*WSEL6	(RM2G84)	
*WSL4Ø	(RM2H94)	
*WSL41	(RM2H95)	Indicates individual contents of bits
WSL42	(RG3G74)	to direct the MTU to specify and set registers
*WSL42	(RM2H96)	
*WSL43	(RM2H97)	
WSL50	(RG4J24)	
*WSL50	(RM2J94)	
*WSL51	(RM2J95)	
*WSL52	(RM2J96)	
*WSL53	(RM2J97)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
*WSL60	(RG5B24)	
*WSL61	(RG5B25)	Indicates individual contents of bits
*WSL62	(RG5B26)	to direct the MTU to specify and set registers
*WSL63	(RG5B27)	
*WICLK	(RW5C24)	Write Clock signal
WIOK	(RW5A44)	Indicates that the MTU is in the write voltage
*WTOK	(RW5B24)	
*WION	(RW5D24)	Directs the MTU tp set the write voltage
WVON	(RW4G62)	Directs the MTU to set the write
WVON	(RW4G84)	voltage on
XBUSØ	(MX1B94)	
XBUS1	(MX1J94)	
XBUS2	(MX2B34)	
XBUS3	(MX2J34)	Indicates individual contents of 8
XBUS4	(MX2B74)	bits of register files or test signals
XBUS5	(MX2J74)	
XBUS6	(MX2BY4)	
XBUS7	(MX2JY4)	
YBIØ	(BI3B34)	
YBI1	(BI3C34)	
YBI2	(B13D34)	Indicates individual contents of 9
YB13	(BI3J34)	bits of the Bus In signal to the MTC

APPENDIX B SIGNALS IN LOGIC CIRCUITS

APPENDIX B 5.	IGNALS IN LOGIC	
Nickname	Pin-Index	Description
YB14	(BI3K34)	
YBI5	(BI3L34)	
YBI6	(BI3BX4)	Indicates individual contents of 9 bits of the Bus In signal to the MTC
YBI7	(BI3CX4)	bits of the bas in signar to the mo
YBI8	(BI3DX4)	
YBO Ø	(BO2JX4)	
YBO1	(BO2JX6)	·
YBO2	(BO2JX7)	
YBO3	(BO2KX4)	Indicates individual contents of 9
YBO4	(B02KX6)	bits of the Bus Out signal from the MTC
YB05	(B02KX7)	
YB06	(B02LX4)	
YB07	(BO2LX6)	
YBO8	(BO2LX7)	
YCPA	(BI3K74)	Capstan Tach signals A/B to the MTC
YCPB	(BI3L74)	
YCTL	(BO2MX7)	Control Tag Signal from the MTC
YGAPC	(BI3JX4)	Gap Control signal to the MTC
YGO	(BO2NX4)	Go signal from the MTC
YINT	(BI3J74)	Interrupt signal to the MTC
YRSV	(BO2HX4)	Reserve and Reserved signals from the MTC

APPENDIX B SIGNALS IN LOGIC CIRCUITS

	Description			
(BO2MX6)	Status Tag signal from the MTC			
(BO2NX6)	Write Clock signal from the MTC			
(RG2G64)				
(RG2G66)				
(RG2H64)				
(RG2H66)	Indicates individual contents of 8			
(RG2L64)	bits of ROM data or general register 0			
(RG2L66)				
(RG2M64)				
(RG2M66)				
(BO2H64)	Directs the MTU to set the slice level of read amplifier to "0"			
(AA1JY4)	Interrupt signal to the microprogram			
(BO2M84)				
(BOIQY4)				
(BI4QX4)	Indicates that the MTU is in the			
(AL1QY4)	status of logical "Ø"			
(RG1QX4)				
(RG5QY4)				
(RG5PY4)				
(BI4PX4				
(BI3QX4)	Indicates that the MTU is in the			
(B01PY4)	status of logical "1"			
	(BO2NX6) (RG2G64) (RG2G66) (RG2H64) (RG2H66) (RG2L64) (RG2L66) (RG2M64) (RG2M66) (BO2H64) (BO2H64) (BO2H84) (BOIQY4) (BI4QX4) (RG1QX4) (RG5QY4) (RG5PY4) (RL1PY4) (BI4PX4 (BI3QX4)			

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
ZØ1F	(AA1NY4)	
ZØ1F	(RW4PX4)	
Ø	(RW4NX4)	
ø	(RW5Q24)	
ø	(RW2NY4)	
ø	(RG3QY4)	
φ	(RG2QY4)	
φ	(RM1QY4)	Indicates that the MTU is in the
ø	(AA1QY4)	status of logical "Ø"
ø	(BO2Q84)	-
ф	(BI1QY4)	
ø	(MX2PY4)	
ф	(MX1QY4)	
ф	(MX3PY4)	
φV	(CB1E94)	
ø٧	(CB1MY4)	φv
φv	(PW6Q24)	
1	(RW1QY4)	
1	(RW4MX4)	
1	(SN1QY4)	
1	(RG3PY4)	Indicates that the MTU is in the status
1	(CL1PY4)	status of logical "1"
1	(MX2QY4)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

APPENDIA D 3	IGNALS IN LOGIC	011/00/110
_Nickname	Pin-Index	Description
+13V	(VQ1A64)	
+13V	(VQ1A54)	
+13V	(VQ1A44)	+13V
+13V	(TK2A94)	
+13V	(TK2A84)	
FECO	(1/04)11/0)	
+5TST	(VQ1NY3)	
+5V	(TK2G65)	+5V
+5V	(TK2H54)	
+5V	(CB1C94)	
-13V	(TK2Q84)	·
-13V	(TK2Q94)	
-13V	(VQ1Q65)	-13V
-13V	(VQ1Q54)	
-13V	(VQ1Q44)	
*12ALM	(VQ1B25)	Alarm signal for +12V stabilizing circuit
12VOV	(RW4F66)	-12V overcurrent is detected
16QTP	(SN1H94)	Capstan Tach signal
1600	(RG1H26)	Indicates that the MTU is in the 1600 rpi mode
2¢¢US	(CL1L64)	
2øøus	(CL1K64)	Pulse signal with a cycle of 200 Ms
2øøus	(CL1L54)	

APPENDIX B SIGNALS IN LOGIC CIRCUITS

Nickname	Pin-Index	Description
3.2MS	(CL1P44)	Pulse signal with a cycle of 3.2 mms
3.2MS	(CL1P34)	
4US	(RW4A44)	Pulse signal with a cycle of 4 /u s
5ØØK	(CL1D64)	Pulse signal with a cycle of 500 KHz
51MS	(CL1P64)	
51MS	(CL1P54)	Pulse signal with a cycle of 51 ms
625ØF	(RW4M84)	Indicates that the MTU is provided
625ØF	(RW4M66)	with the function of 6250 rpi mode
*75IPS	(TK1Q24)	Indicates that the MTU is running at 75 ips

APPENDIX C MTU REGISTERS

Signals	Address	Bit	
0	1F	7	Logical "0"
OD	19	7	Opposite direction
	08	2	Auto load is complete
	06	2	Capstan motor backward
1600	01	6	1600 rpi mode
6250F	1D	3	6250 rpi (GCR) moded
ACADV	0A	1	Accelerate air drive
ACT	06	1	Capstan action
AGCOK	1D	5	SAGC OK
AGCON	18	3	Self adjust gain control (SAGC)
AIRDV	04	5	Air drive
ALUOK	01	2	Arithmetic logic unit OK
BFBOT	0A	3	
ВО	1E	0 - 7	Before BOT (beginning of tape) during unload Bus out signal
BOT	19	6	Beginning of tape
BOTS	08	4	(BOT) sensed
BVLM	1B	5	Backward voltage limit—machine reel
BWD	01	1	Backward
CAPGO	03	1	Capstan go
CARY	17	4	Carry
CGOPN	1B	2	Cartridge opened
CLINF	1B	3	Column in file
CLINM	1B	4	Column in machine
CLNDV	04	4	Auto cleaner drive
CMTDV	0A	6	Cartridge drive
CN	12	0 - 7	
CNOVO	17	2	Counter 0 overflow
CNOVI	17	3	Counter 1 overflow
CSL0	09	2	Counter 0 select
CSL1	09	3	Counter 1 select
CIGCL	04	2	Cartridge close
CIGON	13	1	Cartridge on (installed)
CTL	1F	2	Control. log
CTPA	14	2	Capstan tach pulse A
CTPB	14	3	Capstan tach pulse B
DAC1	06	7	D/A convertor (capstan drive correct level)
DAC2	06	6	D/A convertor (capstan drive correct level)
DAC4	06	5	D/A convertor (capstan drive correct level)
DAC8	06	4	D/A convertor (capstan drive correct level)
DAC16	06	3	D/A convertor (capstan drive correct level)
DBOB	1F	4	Detected beginning of block
DDF	1D	4	Dual density feature
DIAG	08	1	Diagnostic for photo sensor
DIBG	1F	5	Detected inter block gap
DNOIS	1F	3	Noise detected
DO PN	15	3	Door open
DSE	02	5	Data security erase
DIM	1F	6	Detected tape mark
L		10 0	

Signals	Address	Bit	
Signais	Address	DIC	
ECDO	07	0 - 7	Error code/key register
ECER	1A	3	Erase circuit error
ECON	1D	2	Erase current on
EMKDV	04	1	Error marker drive
EMMVD	1B	7	Error marker moved
ENITR	1C	5	Enable interrupt
ERRST	01	4	Error reset
ERSC	0B	2	Erase control
ESTDL	14	7	End stop delay
EQUAL	17	5	ALV input equal
MTU	OB	7	MTU configuration
FILE	08	7	Search for tape mark
FIPA	14	6	Full tach pulse A
FP	1D	0	File protect
FRB	19	3	File reel backward
FRF	19	2	File reel forward
FULF	1B	6	Forward voltage limit-file
GAPCT	19	4	Gap control
GA PEN	08	2	Gap control enable
GOB	1F	0	Go tag B
HSC	0B	3	High speed control
HSCF	1A	7	High speed control file
HSMD	0B	6	High speed mode
HS	13	0 - 7	High speed rewind
HSCM	1A	6	High speed control machine
HSRUM	03	0	High speed run
HUBAL	1A	2	Hub lock alarm
HUBLK	15	4	Auto lock alarm
INSTL	08	0	Installed (power supply)
INTRP	19	1	Interrupt signal
K	07	0 - 7	
KT	19	0	Capstan motor start time
LDRK	15	7	Load rewind key
LOAD	80	6	Auto load
LOCK	06	0	Capstan lock
LTLAL	1A	1	Right tape loop alarm
LTPAS	03	2	Low tape pass
LVL64	1A	4	Slice level 64%
LVL90	1A	5	Slice level 90%
LVLTO	02	0	Level test 0
LVLT1	02	1	Level test 1
LVLT2	02	2	Level test 2
LWR	18	6	Loop write to read
LWR2	18	7	Loop write to read 2
LWSL	0B	0	Low slicee level
LWTP	14	1	Low tape
MARGN	11	7	Margin test
MASK	09	7	Interrupt control
MIDLD	03	3	Mid load Miscellaneous error
MISCE	18	"	LITOCETTOTICORD CTTOT

APPENDIX C MIU REGISTERS

MRB 19 5 Machine reel backward MRF 19 4 Machine reel forward NEWF 1C 6 New function (streaming or skip file) ONL 19 0 Online PE 01 7 Phase encoded recording mode PRESET 1A 7 Counter reset REDET 08 3 MTU ready RETEND 08 3 MTU ready RECORD 15 1 Reel servor swit	Signals	Address	Bit				
MRF 19 4 Machine reel forward NEWF 1C 6 New function (streaming or skip file) ONL 19 0 Online PE 01 7 Phase encoded recording mode PRESET 1A 7 Counter reset PRSVL 04 7 Pressure valve drive RDINH 1A 2 Inhibit read data RDYHL 18 4 Ready hold READY 08 3 MTU ready RETENS 0A 4 Tape retention RGPE 15 1 Register parity error RLACT 02 3 Reel action RLSTP 03 6 Reel stop RSVW 03 7 Reel servo switch RNOIS 14 0 Reset noise ROMPE 15 0 RDM parity error RFMR 19 6 Reel power RSTK 15 2 Reset key RTLAL 1A 0 Right tape loop alarm RTSFL 14 6 Reset field tester flag RUCHL 14 1 Reset unit check hold RVSL 03 3 Reversal RWD 02 6 Rewind SAGC 1A 1 Self adjust gain control SBOT 14 Sense BOT (beginning of tape) SERS 01 0 Set error status SET 1A 6 Set (DGC amplifier control counter) SIGN 06 2 Sigh bit SIRPT 14 4 Set interrupt	MRB	19	5	Machine rool backward			
NEWF 1C 6 New function (streaming or skip file) ONL 19 0 Online PE 01 7 Phase encoded recording mode PRESET 1A 7 Counter reset PRSVL 04 7 Pressure valve drive RDINH 1A 2 Inhibit read data RDYHL 18 4 Ready hold READY 08 3 MTU ready RETENS 0A 4 Tape retention RGPE 15 1 Register parity error RLSTP 03 6 Reel action RLSTP 03 6 Reel stop RSVW 03 7 Reel servo switch RNOIS 14 0 Reset noise RCMPE 15 0 RDM parity error RPWR 19 6 Reel power RSTK 15 2 Reset key RTLAL 1A 0 Right tape loop alarm RTSFL 14 6 Reset field tester flag RUCHL 14 1 Reset unit check hold RVSL 03 3 Reversal RWD 02 6 Rewind SAGC 1A 1 Self adjust gain control SBOT 14 5 Sense BOT (beginning of tape) SERS 01 0 Set error status SET 1A 6 Set (DGC amplifier control counter) SHBOT 08 5 Search for BOT (beginning of tape) SIRPT 14 4 Set interrupt	1	T T	1				
ONL 19 0 Online PE 01 7 Phase encoded recording mode PRESET 1A 7 Counter reset PRESVL 04 7 Pressure valve drive RDINH 1A 2 Inhibit read data RDYHL 18 4 Ready hold READY 08 3 MTU ready RETENS 0A 4 Tape retention RGPE 15 1 Register parity error RLACT 02 3 Reel action RLSTP 03 6 Reel stop RSVW 03 7 Reel servo switch RNOIS 14 0 Reset noise ROMPE 15 0 RDM parity error RPWR 19 6 Reel power RSTK 15 2 Reset key RTLAL 1A 0 Right tape loop alarm RTSFL 14 6 Reset field tester flag RUCHL 14 1 Reset unit check hold RVSL 03 3 Reversal RWD 02 6 Rewind SAGC 1A 1 Self adjust gain control SBOT 14 5 Sense BOT (beginning of tape) SERS 01 0 Set error status SET 1A 6 Set (DGC amplifier control counter) SHBOT 08 5 Search for BOT (beginning of tape) SIGN 06 2 Sigh bit STRPT 14 4 Set interrupt	1 -		1				
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RGPE RLACT RLACT RLSTP RLSTP RSVW RSVW RSVW RNOIS RCMPE RSTW ROMPE RSTK RTLAL RESTE RTLAL RESTE RTLAL RESTE REST REST		0A	4				
RLACT RLSTP 03 6 Reel stop RSVW 03 7 Reel servo switch RNOIS 14 0 Reset noise ROMPE 15 0 RDM parity error RPWR 19 6 Reel power RSTK 15 2 Reset key RTLAL 1A 0 Right tape loop alarm RTSFL 14 6 Reset field tester flag RUCHL 14 1 Reset unit check hold RVSL 03 3 Reversal RWD 02 6 Rewind SAGC 1A 1 Self adjust gain control SEMK 02 4 Sense BOT (beginning of tape) SEMK 02 4 Set error mark SEOT 14 5 Sense EOT (end of tape) SERS 01 0 Set error status SET 1A 6 Set (DGC amplifier control counter) SHBOT 08 5 Sigh 06 2 Sigh bit SIRPT 14 4 Set interrupt	1	15	1				
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SIGN 06 2 Sigh bit SIRPT 14 4 Set interrupt		1 1	5	Search for BOT (beginning of tape)			
		1	2	Sigh bit			
		1 1		Set interrupt			
SKIPF 1C 7 Skip file feature	1	1C	7				
SLOW 19 7 Reel slow		I I					
SP-KT 19 2 Capstan motor stop time	1	i I		Capstan motor stop time			
SOLVL 04 6 Solenoid valve drive		1 1		Solenoid valve drive			
SPOS OB 4 Set positioning							
SSTEP 1A 3 SGAC (self adjust gain control) step pulse	1	1 1		SGAC (self adjust gain control) step pulse			
SILP 6 1C 0 Step 6, all tracks	! !			Step 6, all tracks			
STPCK 19 1 Stop lock check (capstan motor)		1:		Stop lock check (capstan motor)			
STRMD 01 5 Streaming (high speed) mode	i I	1		Streaming (high speed) mode			
STRMF 1C 4 Streaming (MTU has high speed function)	l .			Streaming (MTU has high speed function)			
SIS IF 1 Status lag				Status lag			
SVOK 03 4 Servo OK							
SVON 03 5 Servo ON		l I					
SWO 16 0 - 7 Field test switch signal	I I			Field test switch signal			
SWRS 01 3 Set write status	CAMC	01	3	Set write status			

APPENDIX C MTU REGISTERS

Signals	Address	Bit	
TM	18	1	Tape mark
TMO	10	0 - 7	Time count register 0
TM1	11	0 - 7	Time count register 1
TMOD	18	5	Test mode
TMOV0	17	0	Timer 0 overflow
TMOU1	17	1	Timer 1 overflow
TMSR	1E	0 - 7	Time sensor
TMSR8	1F	2	Time sensor 8
TOVRN	18	2	Tape overrun
TP	14	0	Tape present
TSFL	17	6	Test flag (online/offline)
TSL0	09	4	Timer 0 select
TSL1	09	0	Timer 1 select
TST	17	7	Test start
TUCHK	19	3	Tape unit check
TWA	19	5	Tape wwarning area
WCER	1A	4	Write circuit error
WDCLS	1B	0	Window switch closed
WK00-WKD7		0 - 7	Work register 0
WK10-WK17	0C		Work register 1
WK20-WK27	OD		Work register 2
WK30-WK37	0E		Work register 3
WK40-WK47	OF		Work register 4
WK58	13		Work register 5
WKSL0	09	5	Work select registers
WKSL1	09	6	Work select registers
WNDCL	04	3	Window close
WPOS	0B	5	Write positioning
WRIST	1A	5	Write/read PCA installed
WIRC	OB	1	Write control
WVON	1 D	1	Write voltage on
UCHLD	19	2	Unit check hold
UCKLP	04	0	Unit check lamp
UNL	02	7	Unload
UNLK	15	6	Unload key
VEL0	1D	6	Velocity mode 0
VELI	1D	7	Velocity mode 1

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