

440/480

FLEXIBLE DISK DATA STORAGE SYSTEMS

SERVICE MANUAL

QUALOGY

Formerly Data Systems Design
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PREFACE

This manual provides theory of operation and service instructions for the DSD 440 and the DSD 480 Flexible Disk Data Storage Systems.

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1.0 GENERAL INFORMATION

1.1 Purpose and Scope

The intended purpose of this publication is to provide detailed theory of operation and necessary servicing information for the DSD 440 and DSD 480 Flexible Disk Data Storage Systems.

The manual contains five major sections. Section 1 contains general information, a list of related publications, a summary of follow-on services available to the customer, and a statement concerning our service philosophy. Section 2 provides information about the three computer interface modules available for use with the systems. Section 3 contains a detailed description of the operation of the controller module used with the systems. Section 4 contains instructions for servicing the equipment, lists recommended test equipment, and provides fault analysis procedures. Section 5 contains an illustrated parts breakdown, a power distribution panel assembly drawing, component layout drawings, and schematics for the equipment.

The Shugart Service Manuals listed in Paragraph 1.2 are shipped with The System User's Manuals, as obtained from Shugart. Data Systems Design accepts no responsibility for the content or accuracy of these publications.

1.2 Related Publications

The following is a list of related publications referenced in this manual. The service technician attempting repair of the DSD 440 and 480 Flexible Disk Data Storage Systems must be thoroughly familiar with the contents of the listed publications.

- DSD 440 Flexible Disk System Installation and Programming Manual
- DSD 480 Flexible Disk System Installation and Programming Manual
- Shugart SA800/801 Single-Sided Diskette Drive Service Manual (applicable to DSD 440)
- Shugart SA850/851 Double-Sided Diskette Drive Service Manual (applicable to DSD 480)
- Intel MCS-80/85[™] Family User's Manual

1.3 Service Philosophy

The service philosophy of Data Systems Design has been to limit any field maintenance to preventive maintenance and the replacement of subsystem modules (controller, interface modules, disk drives, power supply, and interface cable). The maintenance instructions contained in the User's Manuals are considered adequate for that level of maintenance.

The detailed theory of operation, error code analysis, and servicing procedures contained in the following sections of this manual are intended for use by senior level technicians who may be required to repair individual subsystem modules at facilities with required bench test setups.

1.4 Special Support Items

For those activities doing field service on the DSD 440 and 480 equipment, the DSD Customer Service Department has the following items available:

- Subsystem Spares Kits
- Component Spares Kits
- DSD 440/480 Extended Self-Test Kit.

For information concerning these items, contact either of the listed offices:

DSD CUSTOMER SERVICE

Data Systems Design maintains a fully staffed Customer Service Department. If at any time during inspection, installation, or operation of the equipment you encounter a problem, contact one of these offices. Our trained staff can help you diagnose the cause of failure, and if necessary, speed replacement parts to you. Any time you need to return a product to the factory, please contact Customer Service for a Material Return Authorization Number.

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For products sold outside the United States, contact your local DSD distributor for parts and customer service assistance.

1.5 Service Limitations

It should be noted that any repair actions or modifications that change the performance characteristics, affect the integrity of board traces, or otherwise render the equipment beyond economical repair will void the warranty and make the module ineligible for factory exchange.

2.0 INTERFACE MODULES

2.1 Introduction

Data Systems Design manufactures interface modules for the DEC LSI-11, PDP-11, and PDP-8 computers. Two of these modules, DSD Part No. 4432 (LSI-11) and DSD Part No. 4430 (PDP-11), are used with both the DSD 440 and DSD 480 Systems. The PDP-8 Interface Module, DSD Part No. 2131, is used only with the DSD 440 System.

Both the systems User's Manuals (440 and 480) provide information concerning installation of the interface modules in the host computer, and detailed discussion of the programming protocols for each operational mode used to interface communications between the DSD Controller Module and the host computer.

2.2 Interface Bus Specifications

The DSD 440/480 Interface Bus (I-Bus) connects the system controller modules, or the diskette storage subsystem, to the computer interface modules, which in turn connects to the input/output bus of the host computer. The I-Bus is implemented on 26-conductor flat cable. It consists of 11 low-true signals, a serial data line, associated hand-shaking, and parallel status signals.

Signals and Pin Connections

Table 2-1 lists all cable pin connections, identifies each by signal and source of the signal, and type termination used on each line.

Signal Descriptions

IERROR L (Error line): The error line is asserted by the controller whenever a given function is terminated because of an error. When the controller is asserting the Error line, both the Done line and the Data-To-CPU line are also asserted. The Error line is negated either when the interface generates an initialize, or when a new command is sent to the controller. PDP-11 and LSI-11 interface modules may also assert the Error line when a non-existent memory error occurs during a DMA operation. This will cause the controller to execute an error termination.

IFINIT L (Initialize line): The INIT line is asserted by the interface module in response to an I/O reset, or some other resetting function. The controller responds to an INIT by jumping to a special portion of microcode which initializes the controller/drive subsystem. The controller can mask out the INIT interrupt so that certain important operations, such as SECTOR WRITE routines, are not halted at critical times. Accordingly, the INIT line is latched in the controller until properly processed. The minimum pulse width for the INIT signal is one microsecond.

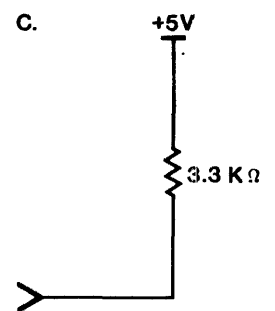
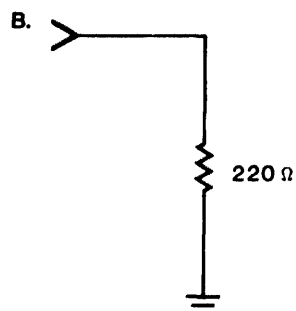
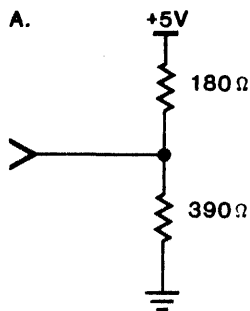
The initialization microcode in the controller includes the following: (The INIT sequence is further described in Section 4.)

- 1) Resets the Error and Done lines
- 2) Runs the controller self-tests
- 3) Checks the switch bank to see if the HyperDiagnostic[®] modes have been selected
- 4) Initializes all variables
- 5) Determines what drives are present and homes them
- 6) Reads Track 1, Sector 1 of Drive 0 into the DATA BUFFER

Table 2-1. I-Bus Signals and Pin Connections

Pin No.	Signal	Source	Termination ¹	
			Controller	Interface
1	Ground	N/A		
2	Ground	N/A		
3	Ground	N/A		
4	Ground	N/A		
5	Ground	N/A		
6	Ground	N/A		
7	Ground	N/A		
8	Ground	N/A		
9	Ground	N/A		
10	Ground	N/A		
11	Ground	N/A		
12	Ground	N/A		
13	Ground	N/A		
14	I 12BM L	Interface	A	
15	I SHIFT L	Controller		A
16	I DATATOCPU L	Controller		A
17	IFDATA L	Bidirectional	A	A
18	IF RDY L	Interface	A ⁺	
19	IFTRREQ L	Controller		A
20	IFINIT L	Interface	A	
21	IDONE L	Controller	C	A
22	IERROR L	Bidirectional ²	A	A
23	KEY ³	N/A		
24	IACLOW L	Controller		B
25	IDMA MODE L	Interface	A	
26	Ground	N/A		

Notes: 1. Termination Types:



2. DSD 2131 interface cannot source this signal.
3. Pin 23 reserved for key.

If all the tasks are successfully completed, the Done line will be asserted. If an error occurs during any initialization function, both the Done and the Error lines will be asserted. If the controller enters the HyperDiagnostic mode, neither Done nor Error will be asserted.

IDMAMODE L (DMA Mode line): When the DMA Mode line is asserted by the interface card, this indicates to the controller that Direct Memory Access is to be employed when performing the FILL BUFFER, EMPTY BUFFER, AND READ ERROR CODE/READ EXTENDED STATUS functions. If the DMA Mode line is negated, this indicates that the interface card is capable only of programmed I/O. The controller microcode tests this line in many places to determine the protocol used on the I-Bus. The DMA Mode line should be asserted only when the controller is in the RX02 mode.

I12BM L (12-Bit Mode line): This line is asserted by the interface card to indicate that it is connected to a 12-bit computer, such as the PDP-8. The I-Bus protocols are again modified according to the state of this line.

IDATATOCPU L (Data-To-CPU line): When this line is asserted by the controller, the direction of data transfer on the data line is from the controller to the interface (floppy disk to CPU). Conversely, when negated, the direction of data transfer is from the interface to the controller. An INIT function always negates this signal.

Normally, the Data-To-CPU line is placed in the appropriate state by the controller before TRANSFER REQUEST is asserted. In RX02 DMA Mode, however, the controller also uses the Data-To-CPU line in conjunction with the Transfer Request line to inform the interface when to switch from doing data transfers by programmed I/O, to doing them by DMA. The DMA mode is initiated when the controller asserts the Data-To-CPU line while the Transfer Request line is asserted. If the direction of data transfer, specified by the remainder of the current command, is from computer to controller, the controller will negate the Data-To-CPU line again. The interface should return to programmed I/O mode when the controller asserts the Done line.

IFDATA L (Interface Data line): The Interface Data line is bidirectional. It is used to transfer data, commands, and some status between the interface board and the controller in the form of 8- or 12-bit serial data streams. The most significant bit is always shifted first. DSD interface boards place an odd parity bit on the Interface Data line at the end of any 8- or 12-bit shift, when the direction of data transfer is from interface to controller. The controller performs a parity check only for commands and parameters, not for data. The controller does not generate parity.

ISHIFT L (Shift line): The Shift line is pulsed by logic in the controller and acts as a clock for the Interface Data line, moving data in and out of shift registers connected to each end of the Interface Data line.

IDONE L (Done line): The Done line, when negated, indicates that the controller is busy performing some function and cannot accept a new command (an INIT function may be performed at any time). When the Done line is asserted and the Data-To-CPU line is negated, the controller is ready to accept a new command.

IACLOW L (AC Low line): This line is essentially a power fail detect signal. The controller asserts this line to indicate a drive box power failure. When a power fail is detected, all controller operations are terminated at their normal completion point, and no further operations are started. The driver on the controller is a 2N4124 emitter-follower, sourcing +5 volts and current limited by a 47 ohm, $\frac{1}{4}$ -watt resistor.

ITRREQ L (Transfer Request line): Transfer Request is the principal signal by which the controller initiates the propagation of serial data streams between the controller and the interface board. Transfer Request works in conjunction with the Data-To-CPU line and IFRDY to form a three wire bidirectional handshake.

When Data-To-CPU is asserted (data input to the CPU), the controller asserts Transfer Request as soon as it has sent enough shift pulses to load the data into the interface shift register. When the data has been input to the CPU, the interface asserts the IFRDY line. On detecting this, the controller negates the Transfer Request line. The interface, in turn, negates IFRDY. The result is that a byte has been transferred from the controller to the interface and on to the CPU.

The controller asserts Transfer Request with Data-To-CPU negated when it needs data from the interface. The interface, when it obtains data from the CPU, asserts the IFRDY line. This indicates that the data is in the interface shift register. The controller then negates Transfer Request, causing the interface to negate IFRDY. The controller then shifts the data from the interface shift register, using the Shift line as a clock (except that DMA memory addresses are not shifted).

IFRDY L (Interface Ready line): The Interface Ready line works in conjunction with the Transfer Request line during data transfers, as described above.

In addition, the interface board uses IFRDY to transfer a new command to the controller. When the controller is awaiting a new command, the Done line will be asserted and the Data-To-CPU line will be negated. The controller interprets IFRDY as an indication that a command is available to be shifted over on the Data line, using the Shift line as a clock. On receipt of the command, the controller will negate the Done line and the interface should negate IFRDY.

Detailed Timing

The following paragraphs discuss details of timing of data transfers on the I-Bus. Protocols associated with specific commands are covered in your DSD 440/480 Systems User's Manuals.

Transfers of data and commands are generally under the control of the controller module. The direction of data transfer is determined by the state of the IDATATOCPU line. The following general rules apply:

1. The interface can drive the Interface Data line only when the Data-To-CPU line is negated. The controller will drive the Interface Data line only when the Data-To-CPU line is asserted.
2. The interface may assert the Interface Ready line only when the controller is asserting the Transfer Request line, or asserting the Done line (new command).

3. Data is always transferred most significant bit first. When the direction of transfer is to the controller (Data-To-CPU line negated), the interface should place the first bit on the line as soon as it is available from the CPU. A new bit should be shifted onto the Interface Data line on each high-to-low transition of the Shift line. The interface must maintain a parity count (odd parity) and the parity bit must be placed on the Data line on the last shift pulse. This parity bit must remain available on the Data line until the controller asserts Transfer Request, or Data-To-CPU. Figure 2-1 (timing diagram) shows details of the operation.

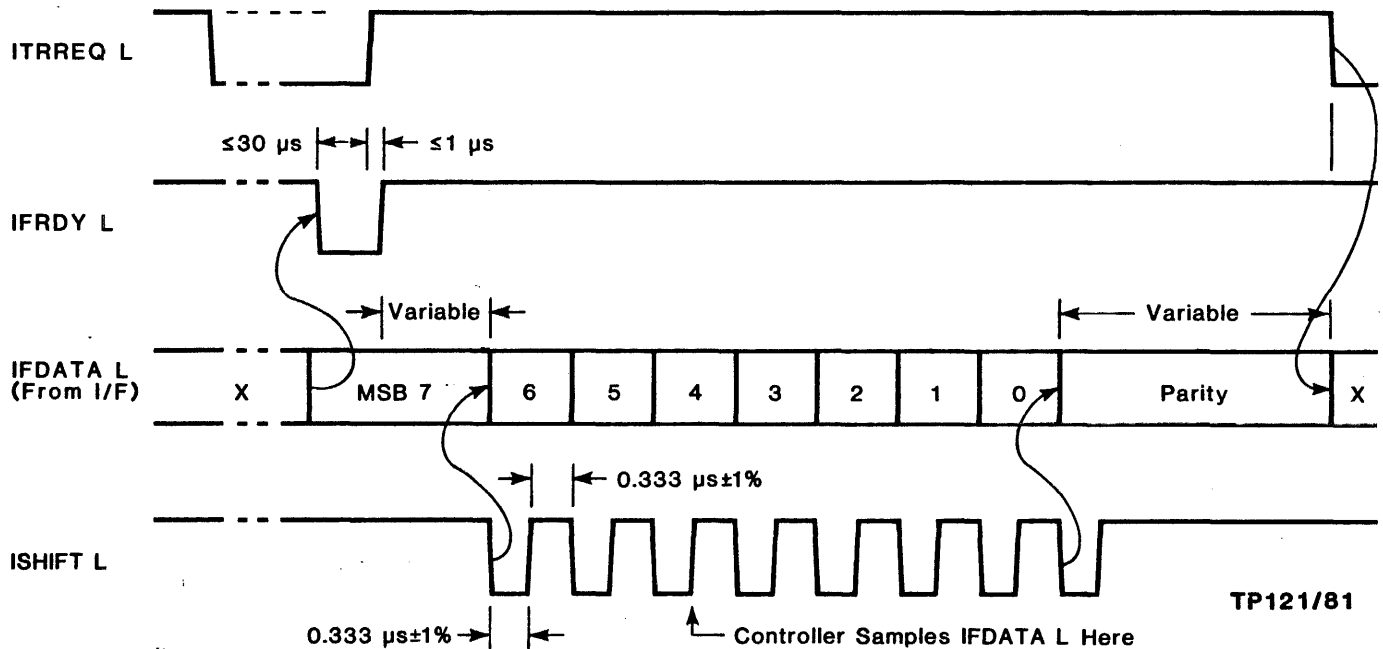
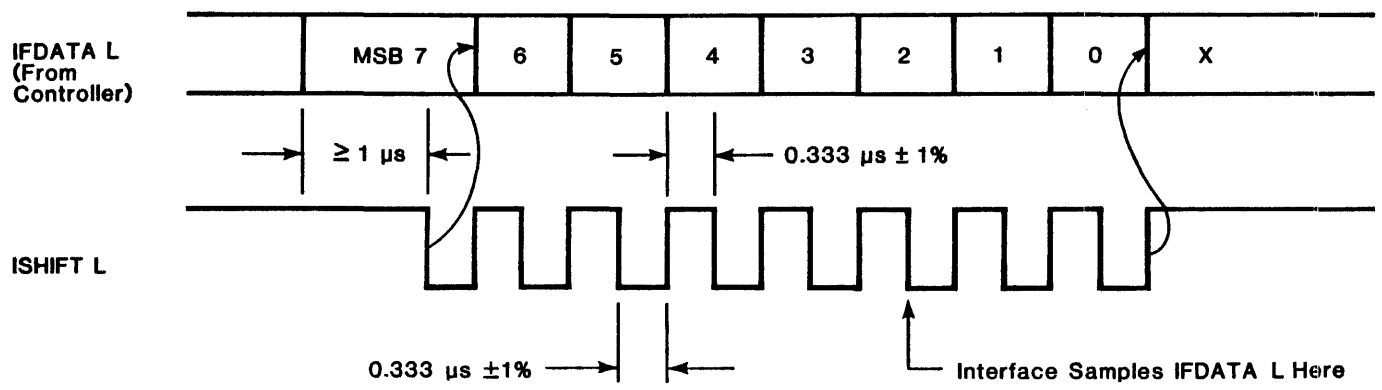


Figure 2-1. Timing, Interface to Controller

4. When the direction of data transfer is toward the CPU, the controller will assert Data-To-CPU and will control the Interface Data line. The interface must be able to accept new data at any time. The controller will place the most significant bit on the Data line. The interface should shift the bit into its shift register on the high-to-low transition of the Shift line. The controller will shift a new bit onto the Data line near the low-to-high transition of the Shift line. The controller does not generate parity. The Data line is meaningless after the last shift. Figure 2-2 (timing diagram) shows the details of this operation.
5. When the controller asserts Transfer Request, the interface is expected to eventually assert Interface Ready. On sensing Interface Ready, the controller will negate Transfer Request within 30 microseconds. On sensing the negation of Transfer Request, the interface should negate Interface Ready within 1 microsecond.



TP122/81

Figure 2-2. Timing, Controller to Interface

3.0 CONTROLLER MODULE

3.1 Introduction

As currently shipped from the factory, the controller modules for the DSD 440 and 480 Systems are identified as follows:

DSD Part No. 804840-01	480 Systems
DSD Part No. 804840-02	440 Systems

Functionally, the controller module used in both systems is the same. The differences between the two boards are because of the extended IBM format available only with the DSD 480 System. Basically, the differences reside in the microcode used, but also, a larger RAM chip is used on the DSD 480 controller module to accommodate the 1 K-byte sectors used in the extended IBM format.

The following theory of operation of the controller module is, therefore, applicable to both the DSD 440 and 480 system controller modules. In this manual, these modules are hereafter called the DSD 440/480 controller. The remainder of this section is arranged as follows:

- Overview
- 8085 Microprocessor
- Cable Connections
- Read/Write Controller
- Serial Data Path
- Phase-Locked-Loop Circuitry
- DC Power Sensing Circuit

3.2 Overview

The DSD 440/480 controller is a general purpose floppy disk controller that can accommodate IBM single-density format and IBM, or DEC double-density format. It is implemented with state of the art LSI technology, and incorporates both an MOS microprocessor and a bipolar bit-slice microprocessor. It includes a high precision phase-lock-loop to guarantee accurate recovery of data from the floppy disk. It requires a single +5 volt supply, and is packaged on a single board measuring approximately 4.65 by 17.1 inches.

The DSD 440/480 controller was designed to accommodate a wide range of disk data formats. In order to accomplish this, a dual processor architecture was adopted. The first processor is the bi-polar bit-slice processor, based on the 2900 chip set. This high speed processor takes serial disk data and converts it to parallel, 8-bit wide data, that can be handled by the MOS microprocessor. The high speed bit-slice controller, called the Read/Write Controller (R/WC), has a basic cycle rate of 333 nanoseconds per instruction. There is enough microcode contained in the R/WC to recognize special data patterns, called address marks, that are present in the disk data formats used. The R/WC also contains all the logic to control the digital sections of the phase-lock-loop circuitry.

The controller module also contains an 8085 MOS microprocessor. The 8085 was chosen because it is a powerful, low cost, general purpose, 8-bit microprocessor that requires a single +5 volt supply. In addition, the 8155 MOS RAM with I/O ports and timer was incorporated because it includes a large number of essential functions in a relatively small space. The 8085 receives its instructions from up to four 2716 type PROMs.

The DSD 440/480 controller is a synchronous controller. A crystal controlled oscillator drives the 8085 microprocessor which, in turn, generates a signal called CLK that provides timing information for the rest of the circuitry.

There are seven major busses in the DSD 440/480 controller. Three of these busses, the data bus, the address bus, and the control bus are related to the MOS microprocessor sections of the controller. Three additional busses, the microaddress bus, the P-Bus, and the next address bus are related to the R/WC. A final bus, the clock bus, consists of the various timing signals that drive major sections of the controller module. See Table 3-1 for a summation of the internal busses.

The DSD 440/480 schematic diagrams are located in Section 5 of this manual. Portions have been incorporated within the descriptive paragraphs that follow, where applicable. The user of this manual is expected to use the foldout feature of the schematics to follow the discussion.

3.3 8085 Microprocessor

Internal Busses: (Reference sheet 2 of controller schematic)

Data Bus: The data bus is used to transfer 8-bit data bytes between the 8085 microprocessor and the various memory locations and I/O ports accessible to the microprocessor. The lower eight address bits are time multiplexed with the eight data bits. Note that on the schematic diagram, the data bus is labelled AD0 through AD7 on the microprocessor side of the bus jumper (C8), and D0 through D7 on the opposite side of the jumper.

A special feature of the data bus is the NO-OP logic (Figure 3-1). This feature is used for maintenance purposes, and consists of a tri-state driver (C9), a bus jumper (C8), and the associated logic. The NO-Op logic forces all zeroes onto bus lines AD0 through AD7 whenever the 8085 does any bus cycle that asserts \overline{RD} . This will only happen if the free run jumper (J23) is installed. Octal jumper C8 must be removed to prevent bus contention problems. Since 00 (Hex) is a NO-Op to the 8085, this exercise should cause the processor to increment through its address space. Using a frequency counter, or oscilloscope, is a quick way to check-trace the address lines. Address lines should be observed with an oscilloscope in relation to the ADDRESS LATCH ENABLE (ALE) pulse. The ALE pulse is used to indicate the valid address timing.

Address Bus: The upper eight address bits (A8 through A15) come directly out of the 8085 microprocessor. During memory reference cycles, these lines will contain the upper byte of the memory address. During I/O reference cycles, A8 through A15 will contain the 8-bit address of the selected I/O port.

The lower eight address bits (A0 through A7) are stable at the output of the demultiplexing latch (C7) following the trailing edge of ALE. The IO/\overline{M} line has essentially the same timing as address bits A8 through A15. When IO/\overline{M} is low, a memory reference bus cycle is specified.

Bus Control Lines: The primary control lines which are sourced by the 8085 are \overline{WR} , \overline{RD} , ALE, and Reset (Figure 3-2). The Reset line serves as a master clear/power-on reset. Most counters and latches on the board have their clear inputs tied to the Reset line. The ALE signal is used to latch address bits A0 through A7 into octal latch C7. It also drives the watchdog timer circuitry. All devices which can be read by the microprocessor, typically, have an output enable line tied to the \overline{RD} signal, in combination with some address decoding selection logic. Similarly, the \overline{WR} signal is part of either a memory, or I/O cycle that strobes the data into the destination. Refer to the 8085 User's Manual by Intel for detailed information on timing diagrams and signal relationships.

Table 3-1. DSD 440/480 Busses

Name	Number of Signals	Schematic Designation	Source(s)	Destination	Function/Note
Data Bus	8	DO-D7	8085, PROM, 2111s, 8155, IF SR, DATA SR, Input Ports, R/WC Error Register	8085, 2111s, 8155 IF SR, DATA SR	Carry 8-bit parallel data from/to 8085
Address Bus	17	A0-A15, IO/M	8085	PROM, 8155, 2111s, Select Logic, R/WC Vector Logic	Selects program memory, I/O ports
Control Bus	4	RD, WR, ALE, RESET	8085	Miscellaneous Logic	Controls read/write cycles of 8085
Micro-Address	12	μ AO- μ A8, Test 1, Test 2, Test 3	Read/Write Controller 2911s	Read/Write Controller PROMS (and misc. Test Logic).	Read/Write Controller busses
P-Bus	32	P0-P31	Read/Write Controller 74S472 PROM	Read/Write Controller Instruction Register	
Next Address	9	NA0-NA8	Read/Write Controller Instruction Register	Read/Write Controller 2911s	
Clock	5	X1, X2, CLK, R/WC CLK, PL CLK	Crystal Oscillator 8085	Miscellaneous Logic	Synchronize functions

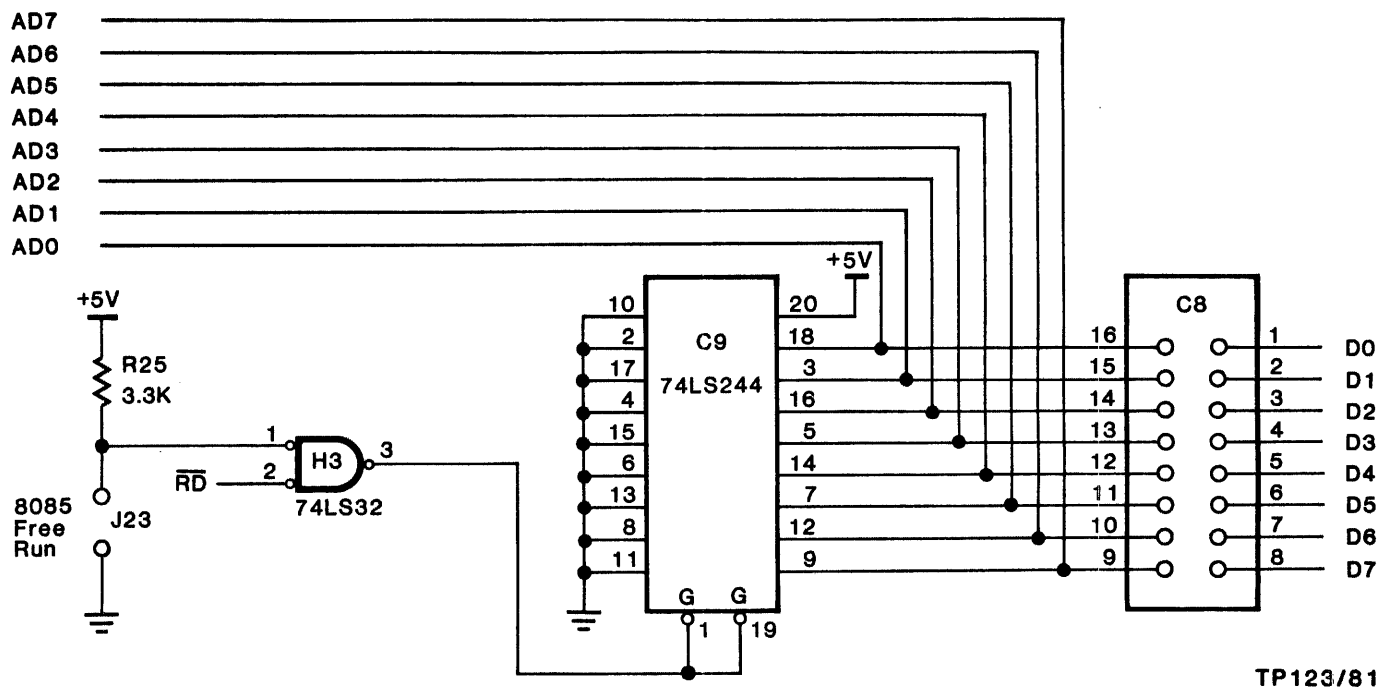


Figure 3-1. NO-OP Logic Circuit

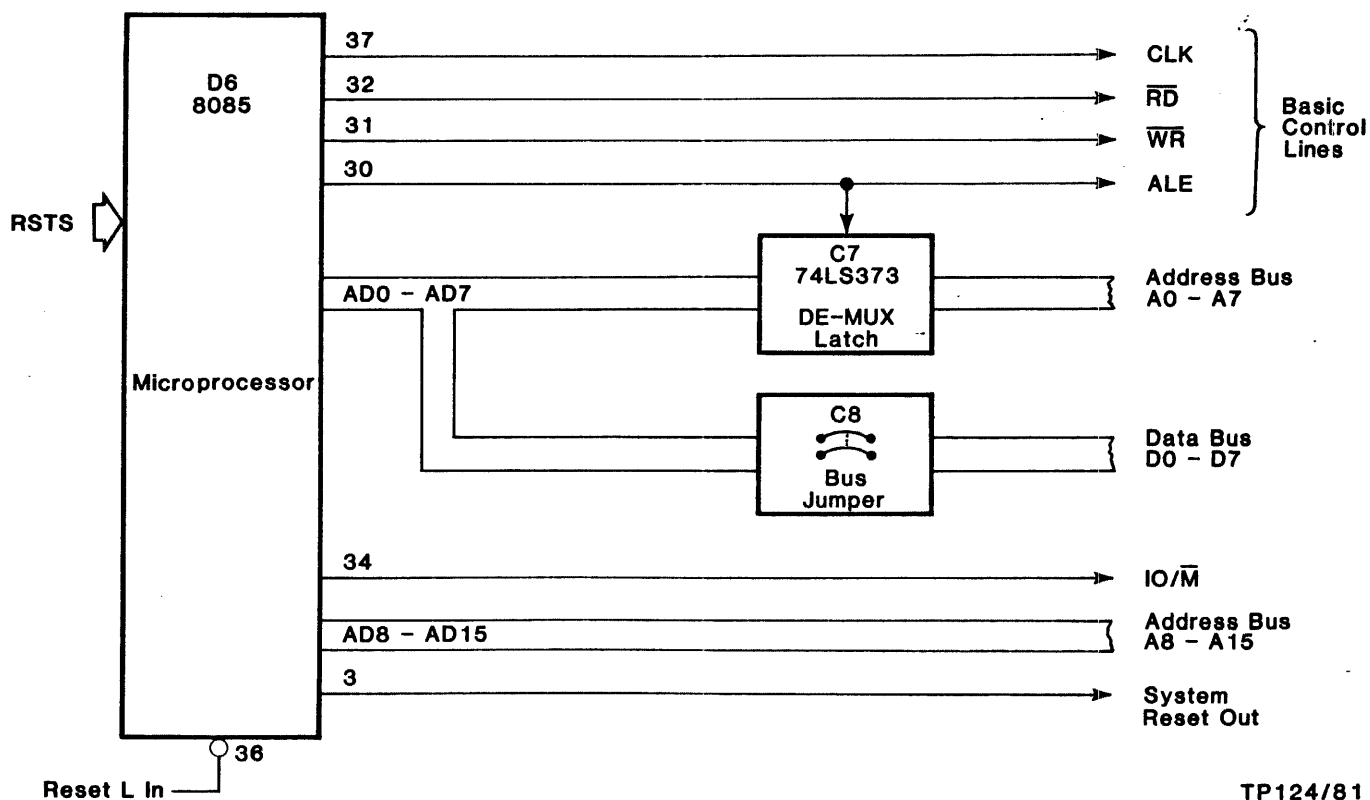
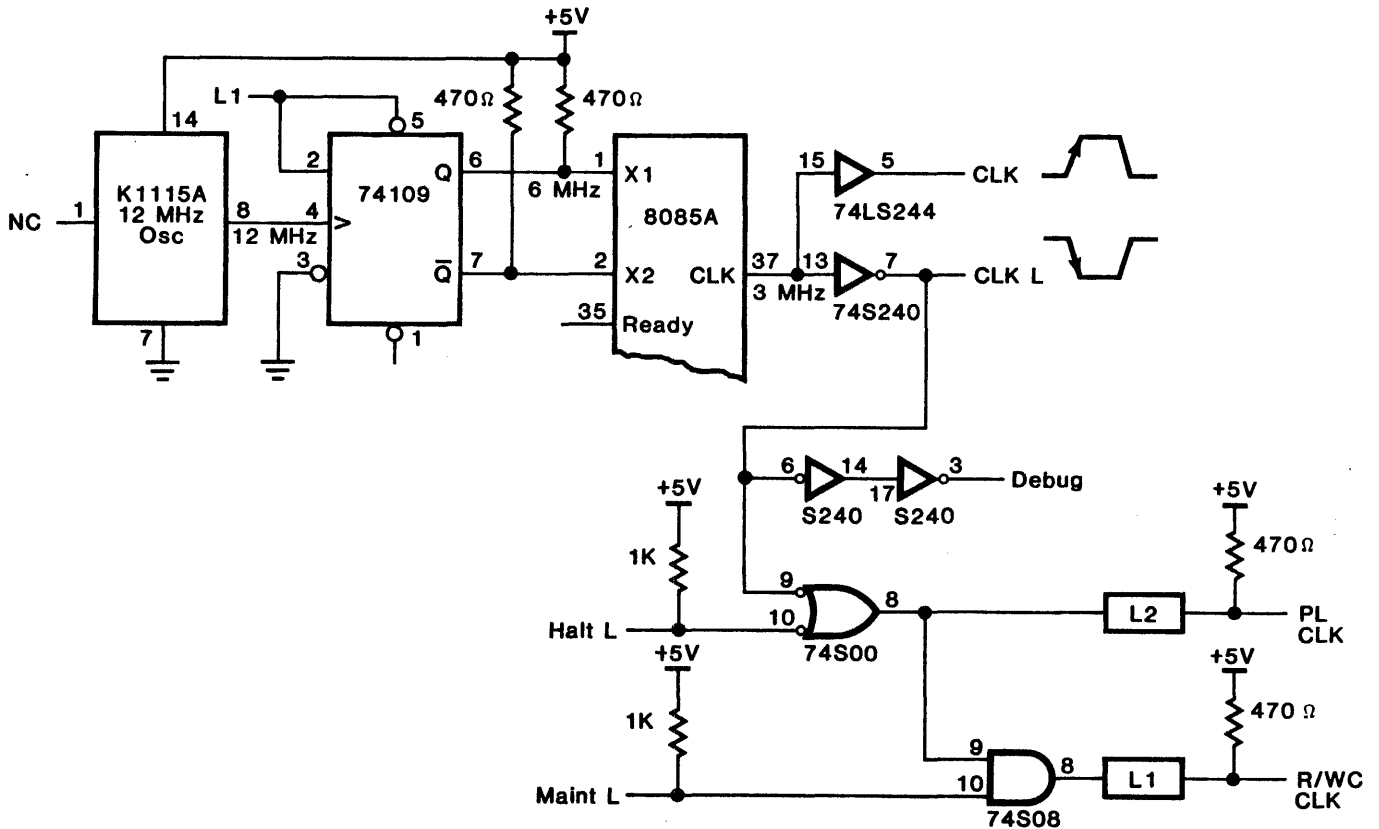


Figure 3-2. Bus Control Lines

Master Oscillator and Clocks: The DSD 440/480 controller modules are synchronous controllers. A self-contained 12 MHz crystal oscillator provides the master clock. See Figure 3-3.



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Figure 3-3. Clock Circuitry

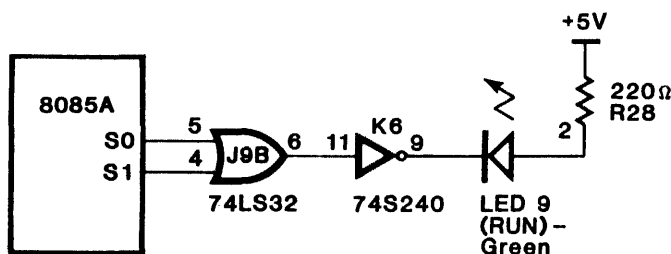
A flip-flop converts the 12 MHz signal into two non-overlapped 6 MHz lines that are then applied directly to the clock generator inputs of the 8085. The 8085 clock period is then 333 nanoseconds (3 MHz). The minimum CLK cycle period specified for the 8085 is 320 nanoseconds (3.125 MHz).

The 3 MHz CLK (out) signal, on pin 37 of the 8085, is used to generate clock signals that are used throughout the controller module. The R/WC bipolar, bit-slice processor is driven by PL CLK and R/WC CLK. Both signals being generated by the 8085 CLK (out) signal.

Data Bus Status Lines: The two Data Bus Status lines, S0 and S1, encode the activity, or lack of it, on the data bus according to the following:

	<u>S1</u>	<u>S0</u>
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

Using the circuit as shown in Figure 3-4, the RUN LED should be on as long as the 8085 is not halted. As the table indicates, the HALT condition is indicated when both S0 and S1 are zeroes.



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Figure 3-4. Status Lines

Master Controller: The nucleus of the master controller consists of several blocks that will be discussed independently of each other. These blocks supply the 8085 microprocessor with the basic information to process the commands sent from the interface and drives. The blocks included in this nucleus are; the 8085, RAM, ROM, mode/option selection, switches, decoders, watchdog timers, and I/F to external control blocks. A block diagram of the master controller nucleus is shown in Figure 3-5.

Control PROMs/ROMs: The 8085 control PROMs/ROMs consist of a combination of 2716, 2732, and/or 2758 EPROMs, or the equivalent ROMs. The type of PROM is selectable by using jumpers to select the various combinations of Address and Control lines to the PROMs. There are four locations for PROMs included on the controller module, referred to as Bank 0 to Bank 3. The individual bank is selected by the address decoder PROM, which is described later. A typical PROM location, and its associated jumper scheme, is shown in Figure 3-6.

RAM Sector Buffer: The RAM sector buffer may consist of two type 2111, 256 x 4 RAM chips on the DSD 440 controller module, or two type 2114, 1K x 4 RAM chips on the DSD 480 module. These RAM chips are used to store the 128 to 1024 bytes of data stored in the diskette sectors. The number of bytes stored depends upon the diskette density, diskette format, and the system capabilities. The DSD 440 System cannot access the extended IBM format, which uses less than 26 sectors per track.

CAUTION

To prevent damage to the RAM chips, the jumpers shown in Figures 3-7 and 3-8 MUST match the type of RAM chip installed.

8155 RAM/I/O/Timer: The 8155 chip is an LSI device which contains RAM, I/O ports, and a timer. The 8155 RAM is addressed by asserting the IO/M line (active low), and selecting a memory address in the range of 3800 to 38FF (Hex).

The 8155 RAM memory is used for the 8085 stack operations, and for storage of variables associated with the current functions and drive status.

The 8155 timer is used to create the step pulse required for the drive logic. The pulse is set under software control for ten microseconds width. This pulse is then generated on command of the 8085. The pulse is a one-shot sequence and is not repeated until the next command is given.

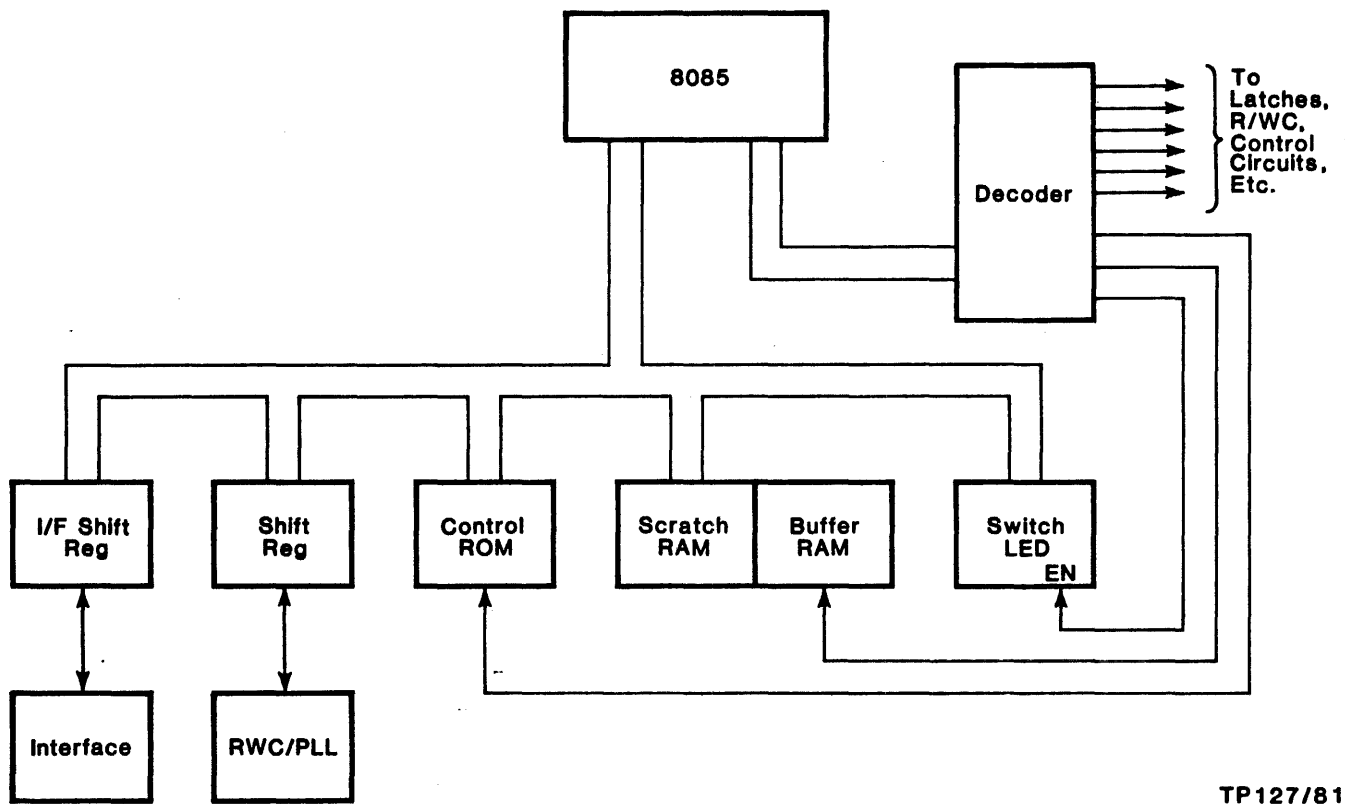


Figure 3-5. Master Controller Nucleus Block Diagram

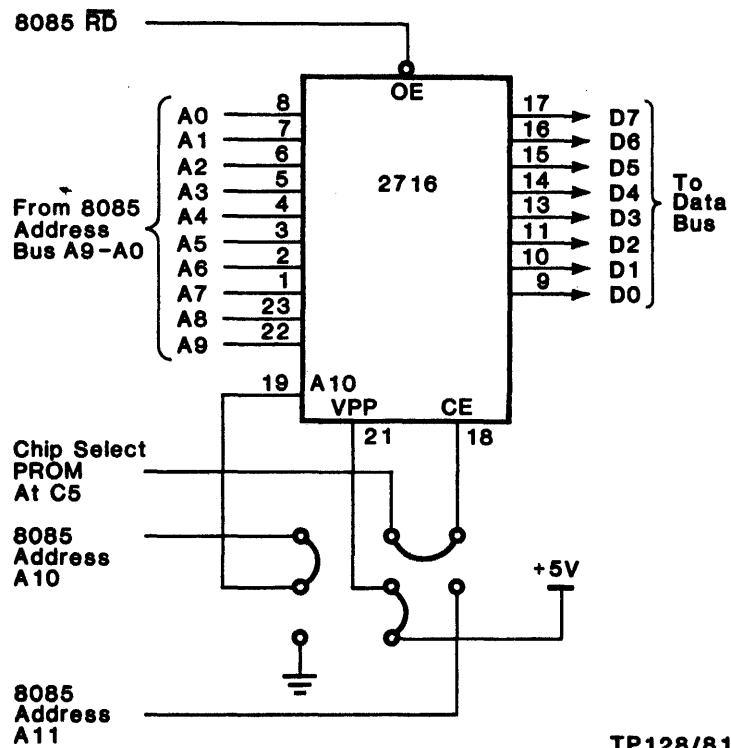


Figure 3-6. Typical PROM Installation

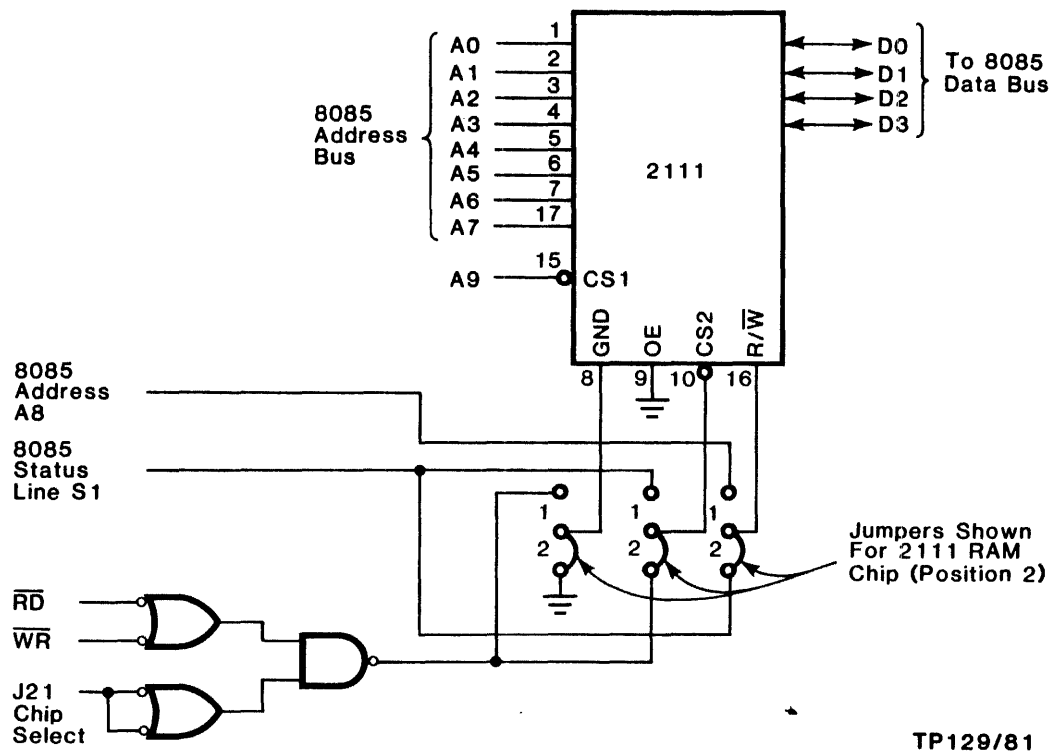


Figure 3-7. 2111 RAM Selection on Controller Module

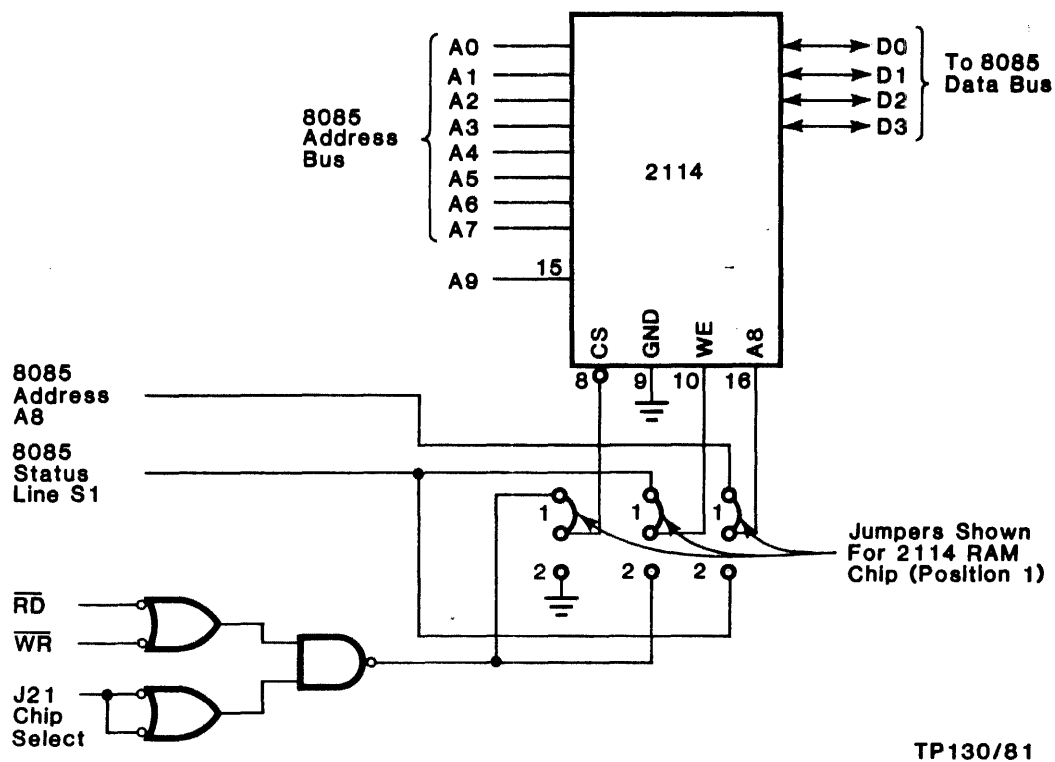


Figure 3-8. 2114 RAM Selection on Controller Module

The 8155 I/O ports are addressed using the 8085 In/Out instructions. The I/O addresses associated with the 8155 I/O ports are 00 to 05 (Hex). Port 00 is used for input of the operator selectable switch bank shown in Figure 3-10. Ports 01 and 02 are used for the Drive Control lines, and are buffered before the signals are put onto the drive cable (see Figure 3-9).

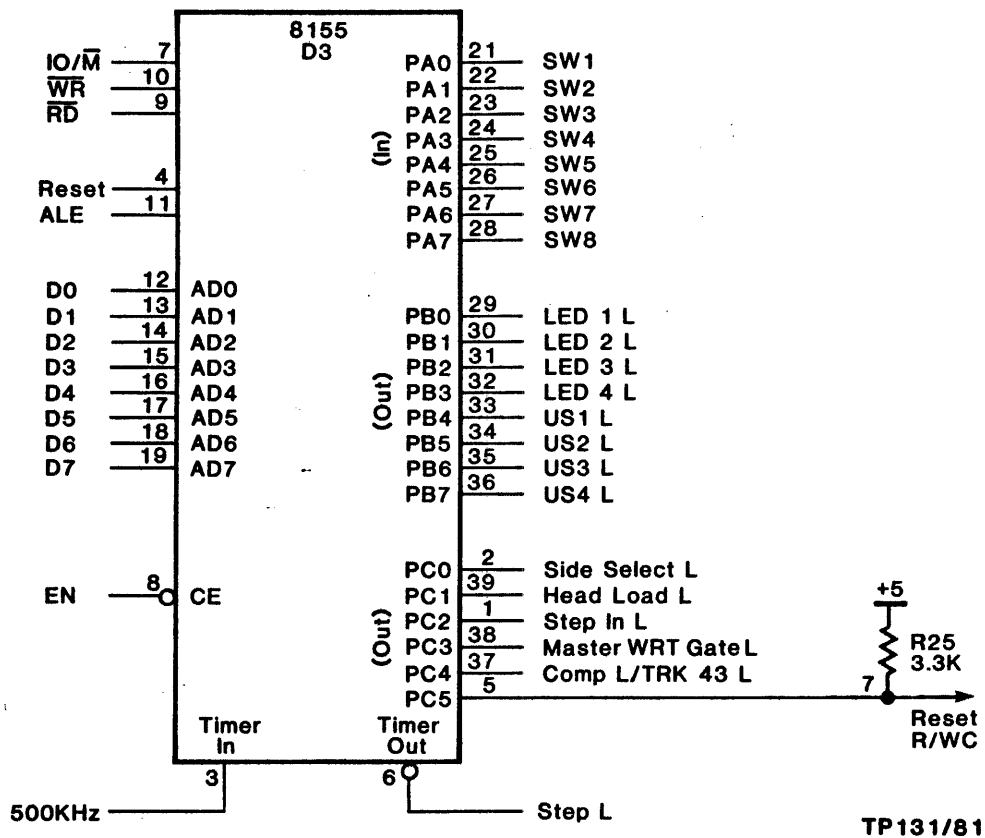


Figure 3-9. 8155 RAM/I/O/Timer

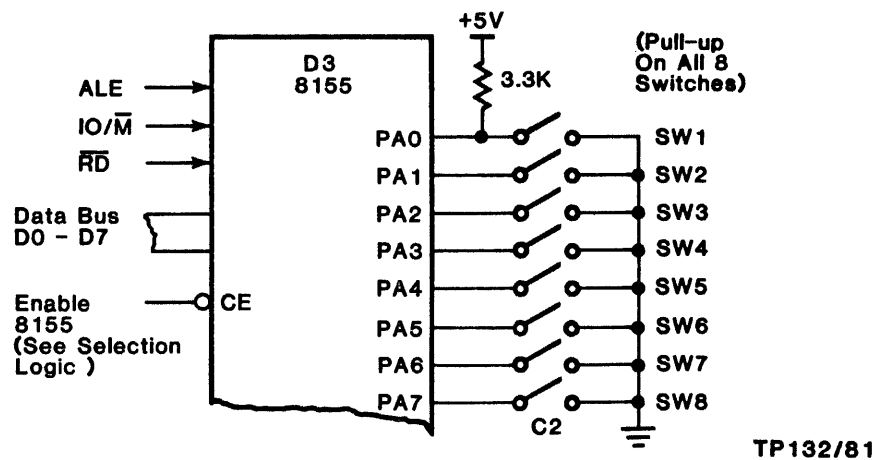
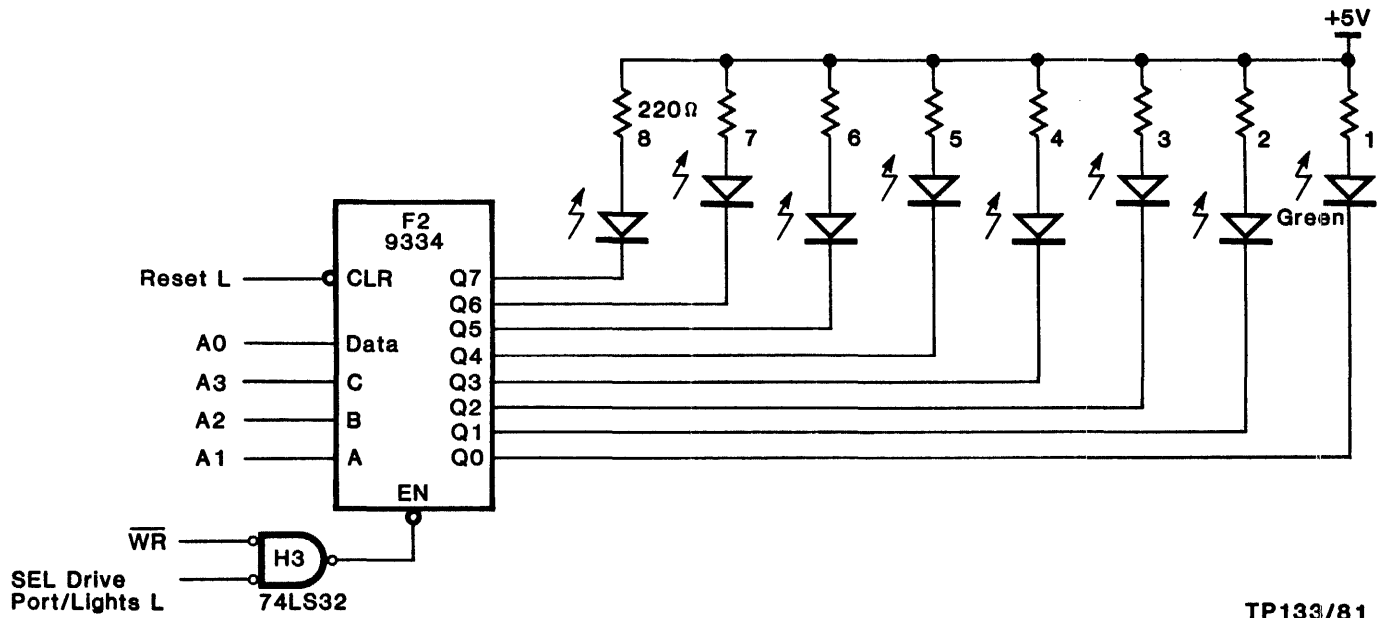


Figure 3-10. Eight Position Dipswitch to 8155 Interface



OUTPUT PORT ADDRESS FOR:

<u>LED #</u>	<u>ON</u>	<u>OFF</u>
1	20	21
2	22	23
3	24	25
4	26	27
5	28	29
6	2A	2B
7	2C	2D
8	2E	2F

Microcode Interface:

NOTE: Input or output instruction may be used to turn on/off LEDs. The accumulator data is ignored.

Special Circuit Features:

- 1) If power is available, and there is a failure in the power-up/reset logic causing the signal RESET L to be held asserted, the 9334 latch will be held cleared. This type of failure situation is easy to diagnose because all 8 LEDs are held ON.
- 2) Note that the 9334 is a write only latch, and that no WAIT states are imposed using the 8085 Ready line.
- 3) See Controller LED Decoding Chart for interpretation specifics.

Figure 3-11. LED Indicator Bank

READ/WRITE PORTS

8155 Ports

NOTE

For complete description of the 8155 refer to Intel MCS 80/85 Family User's Manual.

These ports implement:

1. The switch (option) input register.
2. The unit select/drive activity LED control port.
3. The drive control port.

These ports are implemented by chip D3 (8155). (Sheet 1 of schematic)

Port: CS8155 (00H)

Output Mode

<u>Bit(s)</u>	<u>Purpose</u>
0	Defines port A as Input (0), or Output (1)
1	Defines port B as Input (0), or Output (1)
3-2	Defines port C: 00 = ALT 1 (Input port) 11 = ALT 2 (Output port) 01 = ALT 3 (Control/Output port) 10 = ALT 4 (Control port)
4	Enables (1) or disables (0) port A interrupts
5	Enables (1) or disables (0) port B interrupts
7-6	Controls the 8155 timer: 00 = NOP: does not affect timer operation 01 = STOP: NOP if timer has not started; stop counting if timer is running 10 = STOP AFTER TC: NOP if timer has not started; stop immediately after present TC is reached if timer is running 11 = START: load mode and count length and start immediately after loading if timer is not running. If timer is running, start the new mode and count length immediately after the present TC is reached.

Input Mode

<u>Bit(s)</u>	<u>Purpose</u>
0	port A interrupt request
1	port A buffer fill/empty
2	port A interrupt enable status

- | | |
|---|--|
| 3 | port B interrupt request |
| 4 | port B buffer fill empty |
| 5 | port B interrupt enable status |
| 6 | timer interrupt (This bit is latched high when terminal count (TC) is reached, and is reset to low upon reading of the 8155 control/status register, or starting a new count.) |

Port: JUMPER (01H)

This port is used to input the option switch bank. It is configured by the controller microcode for input operations only.

<u>Bit</u>	<u>Switch</u>
0	1 (Leftmost switch)
1	2
2	3
3	4
4	5
5	6
6	7
7	8 (Rightmost switch)

Port: USLED (02H)

This port implements the unit select and drive activity LED controls.

<u>Bit</u>	<u>Purpose</u>
0	LED-1 (drive 0 activity LED)
1	LED-2 (drive 1 activity LED)
2	LED-3 (drive 2 activity LED, Reserved)
3	LED-4 (drive 3 activity LED, Reserved)
4	US-1 (drive 0 unit select)
5	US-2 (drive 1 unit select)
6	US-3 (drive 2 unit select, Reserved)
7	US-4 (drive 3 unit select, Reserved)

Port: PORTC (03H)

Used for drive control.

<u>Bit</u>	<u>Name</u>	<u>Purpose</u>
0	———	Write current control, 0 = tracks 43-76, 1 = 0-42
1	MASWTG	Master write gate control, 0 = enable, 1 = disable
2	HEADLD	Head load control, 0 = load, 1 = unload
3	STEPIN	Step direction control, 0 = in, 1 = out
4	———	Side select (SA850 drives only) - Reserved
5	RESRW	Reset read/write controller, 0 = reset, 1 = run
6	———	— does not exist, unused —
7	———	— does not exist, unused —

Port: CT8155 (04H)

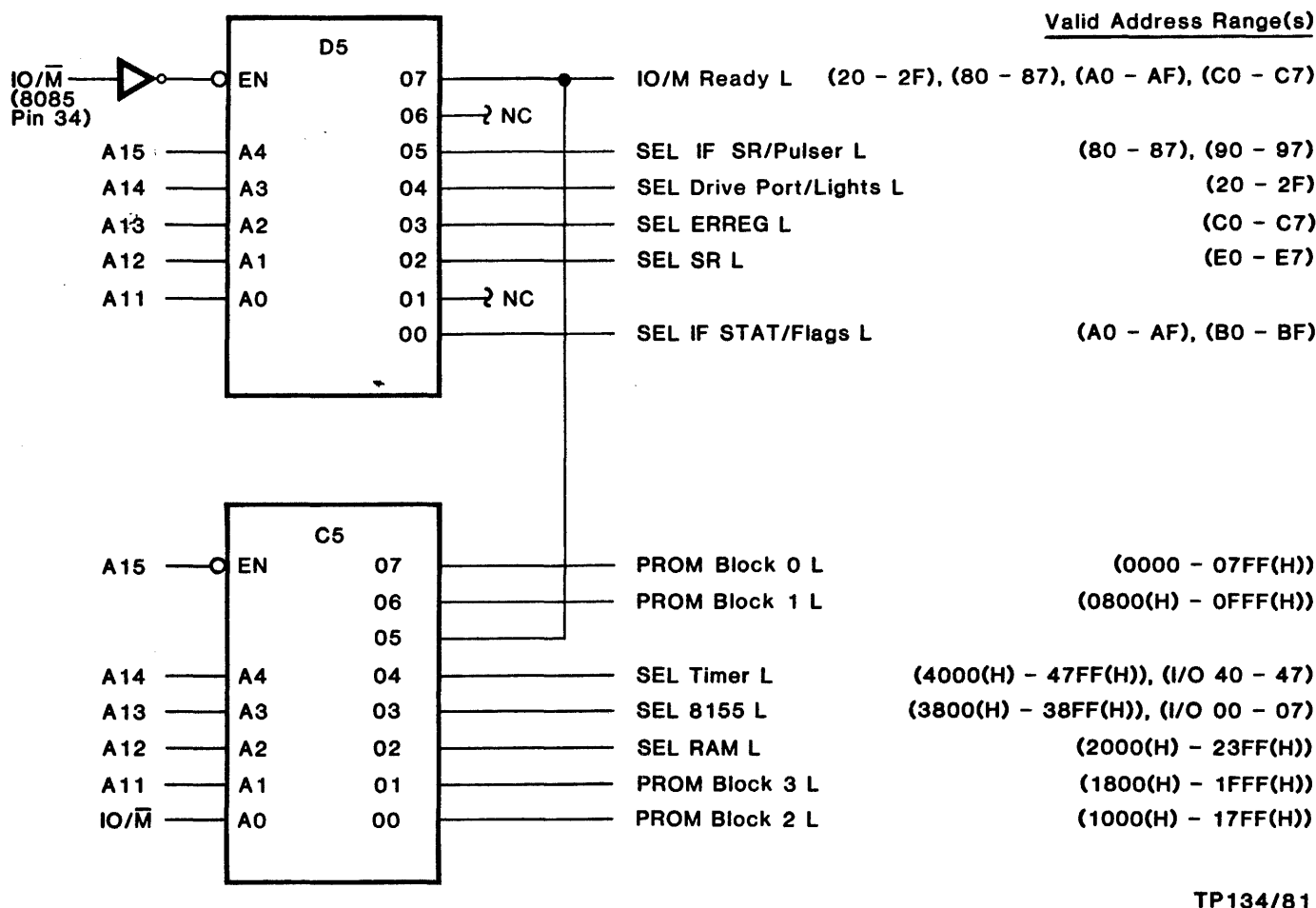
Used for timer control and as the MSB of the count length of the timer. May be read or written.

<u>Bits</u>	<u>Purpose</u>
5-0	MSB of timer count length
7-6	Timer mode: 00 = Output low during second half of count 01 = Square wave output 10 = Single pulse on TC 11 = Pulse and restart on TC

Port: CT8155+1 (05H)

Used for the LSB of the timer count length. May be read or written.

Decoder PROMs: The 8085 device selection is decoded by the two PROMs at locations C5 and D5 on the controller. These PROMs are shown in Figure 3-12. The PROM used in both cases is an 82S23 open collector PROM with enable pin.



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Figure 3-12. Decoder PROMs

The decoder at C5 is used for decoding both I/O port addresses and memory blocks. The decoder at D5 is used solely for decoding I/O port addresses and is only enabled during In/Out cycles of 8085.

All selection lines have an associated 3.3K pull-up resistor. Jumpers are provided on the 8155 enable, 8253 (timer) enable, and RAM enable lines to disable these devices for testing individual devices in an isolated situation.

The Ready line to the 8085 also includes a jumper to force the 8085 ready input, ACTIVE HIGH, for testing 8085 circuitry without the interference of the R/WC or other timeout devices.

See the schematic for details on the jumpers and pull-up resistor networks.

Table 3-2 is a summary of the address assignments and their use.

Figure 3-12 is a diagram of the two decoder PROMs. It shows the function and address selected by each output.

3.4 Cable Connections

There are three cables that connect to the DSD 440/480 Controller Modules. They are; (1) the dc power cable, (2) the interface bus cable, and (3) the drive bus cable. Each of these cables will be discussed in detail.

Power Supply Cable:

<u>Pin No.</u>	<u>Wire Color</u>	<u>Signal</u>
1	Unused	
2	Brown	Common - return for 5 V power
3	Green	Common - return for 5 V power
4	Red	5 V power source
5	White	5 V power source

A five-pin, Molex connector (denoted P2 on the schematic) is used to supply the controller module with 5 Vdc power. The male half of the connector is mounted on the rear, foil side of the board. Pin 1 is closest to the edge of the board.

Interface Bus Cable: The interface bus cable connects the controller module to an interface module installed in some nearby host computer. A 26-pin, male, 3M connector (denoted P3 on the schematics) accepts the I-Bus cable. Note that pin 23 has been removed so that the mating connector, which should have pin 23 plugged, can only be installed in the correct way. A complete description of the I-Bus cable signal timing and protocol can be found in Section 2 of this manual.

Table 3-2. Summary of Address Assignments

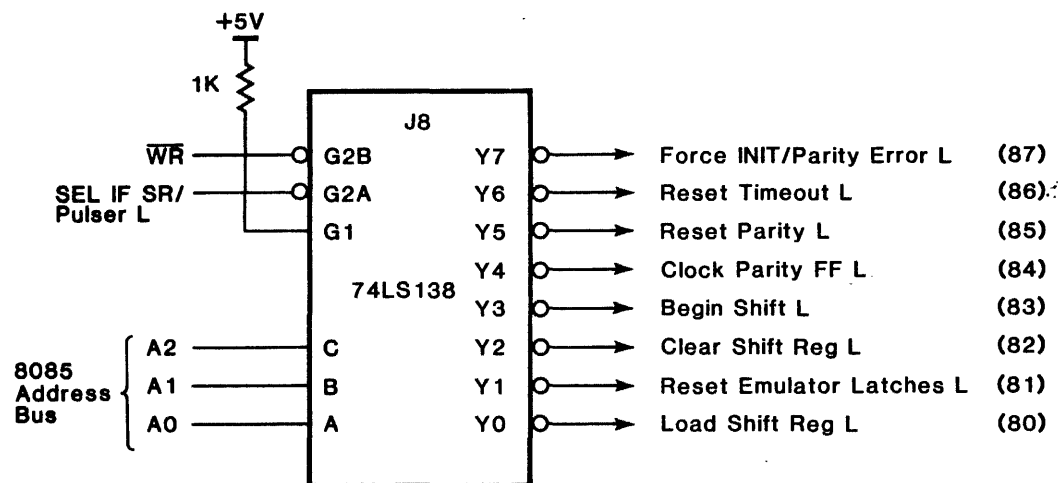
Device	Read Write	Memory I/O	Select/ RDY PROM Source	IO/M RDY L	Address Bits																Comments	
													← I/O									
					A7 A6 A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0															
PROM Block 0	R	M	C5	0	0	0	0	0														
PROM Block 1	R	M	C5	0	0	0	0	0	1													
PROM Block 2	R	M	C5	0	0	0	0	1	0													2716
	R	M	C5	0	0	0	0	1	0	1	X											3624
PROM Block 3	R	M	C5	0	0	0	0	1	1													2716
	R	M	C5	0	0	0	0	1	1	1	X											3624
8155 RAM	R/R	M	C5	0	0	0	1	1	1	X	X	X										
8155 I/O	R/W	I/O	C5	0	0	0	0	0	0	—Dev Sel—												
8253	R/W	M	C5	0	0	1	0	0	0	X	X	X	X	X	X	X	X	X	Reg Sel			
	R/W	I/O	C5	0	0	1	0	0	0	X	Reg Sel											
RAM Select	R/W	M	C5	0	0	0	1	0	0	X	X	X										
I/F Status	R	I/O	D5	1	1	0	1	Wait	X	X	X	X										} Waits for I/F
I/F Flags	W	I/O	D5	1	1	0	1	Wait	—Bit Sel—			Polar										
IF Shift Reg	R/W	I/O	D5	1	1	0	0	0	0	0	0	0										
IFTRCL Select	R/W	I/O	D5	1	1	0	0	1	0	0	0	0										
Pulser	W	I/O	D5	1	1	0	0	Wait	0	—Bit Sel—												If Oper=R, A0-A3=X Waits for I/F; sets transfer flag Wait for I/F
Drive Port	R	I/O	D5	0	0	0	1	0	X	X	X	X										
LED	W	I/O	D5	0	0	0	1	0	—LED Sel—			Sense										
R/WC ERREG	R	I/O	D5	0	1	1	0	0	0	X	X	X										
R/WC Shift Reg	R/W	I/O	D5	1	1	1	1	0	0	X	Vector											Waits for R/WC

0=Auto Ready, 1=Wait

Wait, when set together with the IO/M RDY Line, forces a wait for the interface.

Pulser Output Circuits: The pulser circuit enables the microprocessor to address pulses to eight specific points of interest in the controller. The 74LS138, at J8, serves to route the pulse to the output addressed by A0, A1, and A2 during the WR pulse sent from the 8085. When A0, A1, and A2 are all 0, Y0 emits a pulse which passes through a pulse delay (R28a, C39a, J9b) before strobing the shift register (E8). The other seven pulse ports do the following: (See Figure 3-13.)

<u>Address</u>	<u>Name</u>	<u>Purpose</u>
80 (W)	LDSH	Load data from data bus to shift register
80 (R)	RDSHR	Dump I/F shift register onto data bus
81	RSTEMU	Reset all the emulator latches (Shifter, Parity, L INIT)
82	CLRISR	Clear the interface shift register
83	BEGSHF	Start an interface bus shift operation (4-bit or 8-bit)
84	CLKPAR	Clock the parity status flip-flop (load final parity bit)
85	PREPAR	Pre-set the parity status flip-flop
86	RSTTRP	Reset the time-out trap flip-flop
87	FLINIT	Force the parity and INIT flops set



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Figure 3-13. Pulsed Outputs

General Control Ports: These ports control the status of the serial data path, read/write controller, and interface emulator.

Implemented by chip F9 (9334). Appears on page 6 of the print set. (See Figure 3-14.)

<u>Address</u>	<u>Name</u>	<u>Purpose</u>
A0	NPRCMP	Turns off write precompensation
A1	PRECMP	Turns on write precompensation
A2	NDECMD	Turns off DEC MMFM coder/decoder
A3	DECMOD	Turns on DEC MMFM coder/decoder
A4	DISWTG	Disables the R/WC write gate
A5	ENWRTG	Enables the R/WC write gate
A6	DATFLP	Sets data direction to data-to-floppy
A7	DATCPU	Sets data direction to data-to-cpu
A8	CLRERR	Clears the interface error latch
A9	ERROR	Sets the interface error latch
AA	DD8BIT	Sets double-density PLL clock and 8-bit shifts
AB	SD4BIT	Sets single-density PLL clock and 4-bit shifts
AC	CLRDON	Clears the interface DONE latch
AD	DONE	Sets the interface DONE latch
AE	CLRTRR	Clears the interface TR latch
AF	TRREQ	Sets the interface TR latch
BD	DONEW	Sets the interface DONE latch and waits for ready
BF	TRREQW	Sets the interface TR latch and waits for ready

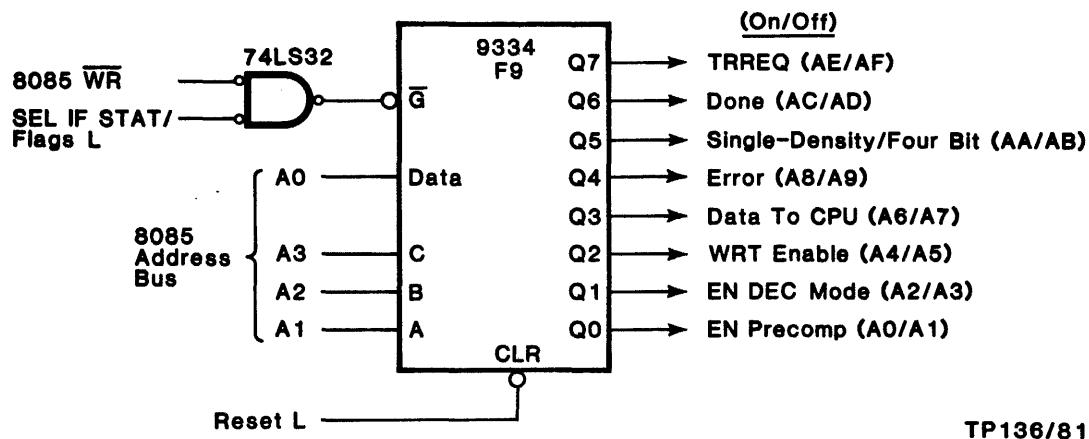


Figure 3-14. Latched Outputs

8085 I/O Status Ports: The 8085 microprocessor may also access status of the drive, the interface, and the R/WC error conditions. Drive status is accessed through port 20 H. The bits returned by the 8085 IN instruction are coded as follows:

<u>Bit</u>	<u>Name</u>	<u>Purpose</u>
0	DISKCH	Indicates "disk changed" status
1	WP2	Reserved for "write protect switch 2"
2	WP1	Reserved for "write protect switch 1"
3	2Sided	Reserved for "two-sided" disk indication
4	WRTPRT	Indicates "write-protected" diskette status
5	DSKRDY	Indicates "drive-ready" status
6	TRK00	Indicates "track 0" sensor status
7	INDEX	Indicates "index" sensor status

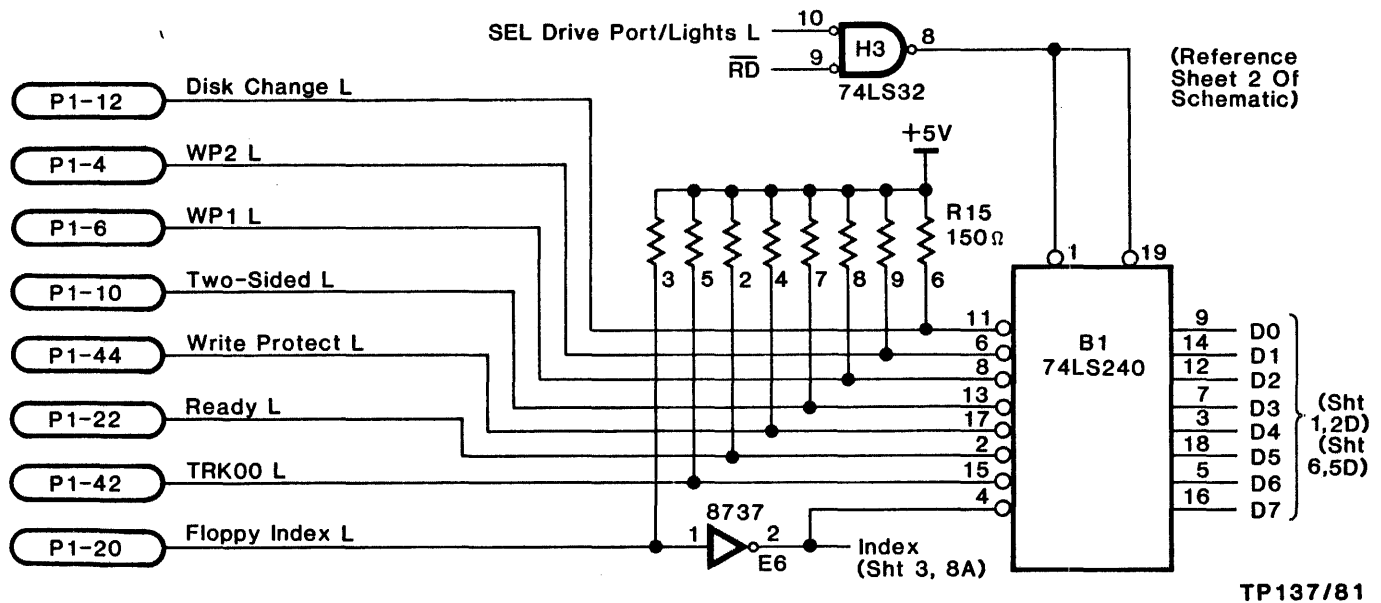


Figure 3-15. Drive Status Port

Interface status is accessed through reading port A0 H. The bits returned by the I/O read cycle to port A0 are coded as shown below. (See Figure 3-15.)

<u>Bit</u>	<u>Name</u>	<u>Purpose</u>
0	BKWRDS	Indicates "cable backwards" test status
1	IFERR	Indicates "interface-error" status
2	ACOK	Indicates "ac power ok" sensor status
3	DMAIF	Indicates "DMA mode interface"
4	TWELVE	Indicates "12-bit interface mode"
5	LINT	Indicates "latched initialize" status
6	PERROR	Indicates "interface parity error" status
7	IFRDY	Indicates "interface ready" status

If an error occurs in the R/WC, the error is placed into the R/WC error register. This register may be read at port C0 by the 8085. The error is coded into the lower four bits. The upper four bits read are insignificant. Refer to the R/WC section for more information.

Interrupt Logic (Restarts): The controller microprocessor makes use of the RST5.5, RST6.5, and the RST7.5 interrupts. (See Figure 3-16.) The first interrupt we will discuss is RST7.5, which has the highest priority. As can be seen on schematic sheet 3, RST7.5 is derived from the signal FILL/EMPTY INTERRUPT that comes from the third counter in the 8253. Notice that this counter is configured to count transfer request flags. The counter gate is tied to logic 1, so the counter is always enabled. A hardware counter is utilized to count the bytes transferred while doing either a FILL BUFFER or EMPTY BUFFER cycle. When all 128 or 256 bytes have been transferred, the counter overflows and an interrupt is generated.

The purpose of using a dedicated hardware counter for the fill/empty routines is to speed up the tight loops associated with these routines. Normally, the 8085 microprocessor has to count the transfers by decrementing or incrementing a register. This process takes four

cycles, or 1.33 microseconds for each transfer. By using the hardware counter, approximately 340 microseconds can be saved for a typical 256-byte sector.

The RST6.5 interrupt can be generated by any one of three sources. These are; (1) R/WC error, (2) parity error, or (3) the Latched INIT. The 8085 will be interrupted if any of these events takes place. The microprocessor must be able to determine which event caused the interrupt so that this information can be reported back to the interface. The microprocessor reads the IF STAT/FLAGS Register (sheet 6 of the schematic, location D8) to get this information.

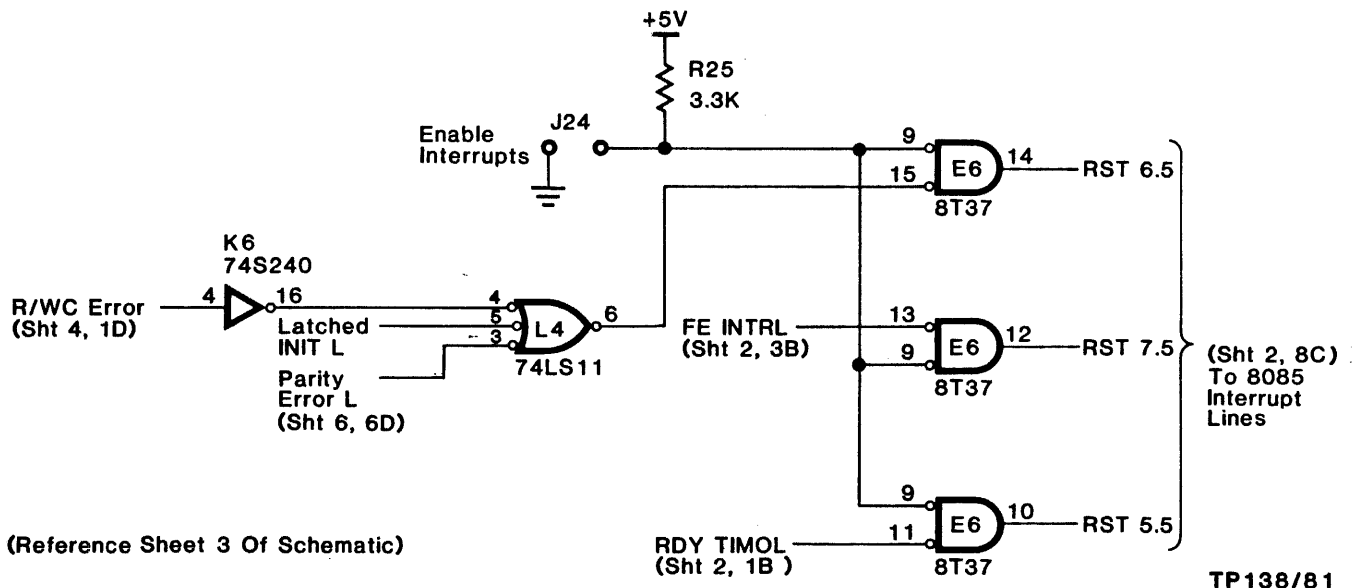


Figure 3-16. Interrupt Logic

The RST5.5 interrupt is generated when the READY TIME-OUT flip-flop becomes set. This will happen when the R/WC does not return with READY before the watchdog timer times out. This interrupt insures that the controller will not become hung if it has difficulty locating a particular address mark.

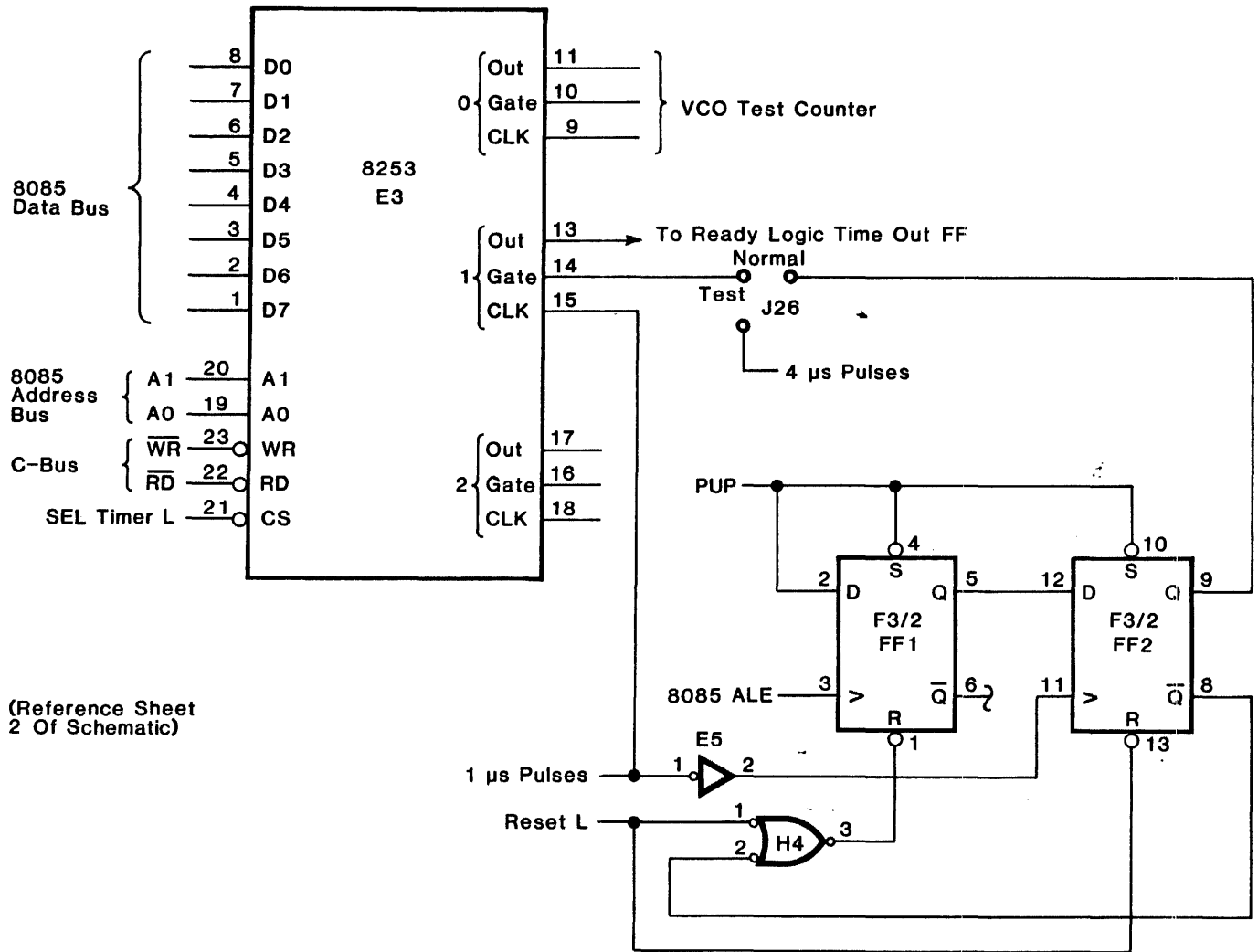
8253 Timers: The 8253 LSI chip contains three counter/timers that are used for the watchdog timer, the fill/empty counter, and the VC0 test circuitry.

Counter No. 1: The timeout watchdog timer circuit is shown in Figure 3-17. The function of this circuit is to detect the loss of the READY signal to the 8085. The READY signal may be delayed because of an R/WC problem or an inactive interface (no CPU action). The 8253 timer is preset with the expected timeout value, and is then gated on/off by the occurrence or non-occurrence of the 8085 ALE Control line. The timeout provides the 8085 with an escape route so that the system will not hang if an unexpected timeout occurs.

Figure 3-18 shows the watchdog timer timing during a normal I/O sequence. Three examples are shown which result from the timing relationship of the 0.1 microsecond pulse to the 0.333 microsecond CLK pulse from the 8085. During the T(W) state, the 8085 is in wait state, but the 8253 is still counting the 0.1 microsecond pulses. During normal operation, the 8253 counter does not complete its count while the 8253 gate has been enabled. There will not

be a terminal count pulse at the 8253 output unless terminal count has been reached, and the completion ALE pulse has not occurred. The accuracy of this circuit is approximately a 0.1 microsecond period during which the ALE pulse may have occurred, but has not inhibited the 8253 gate and output.

Counter No. 2: The fill/empty counter was described in the interrupt section of the 8085 circuitry. The counter records the number of transfer requests. When the correct number have occurred, an RST5.5 interrupt is generated to stop the fill/empty routine currently in progress.



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Figure 3-17. Watchdog Timer

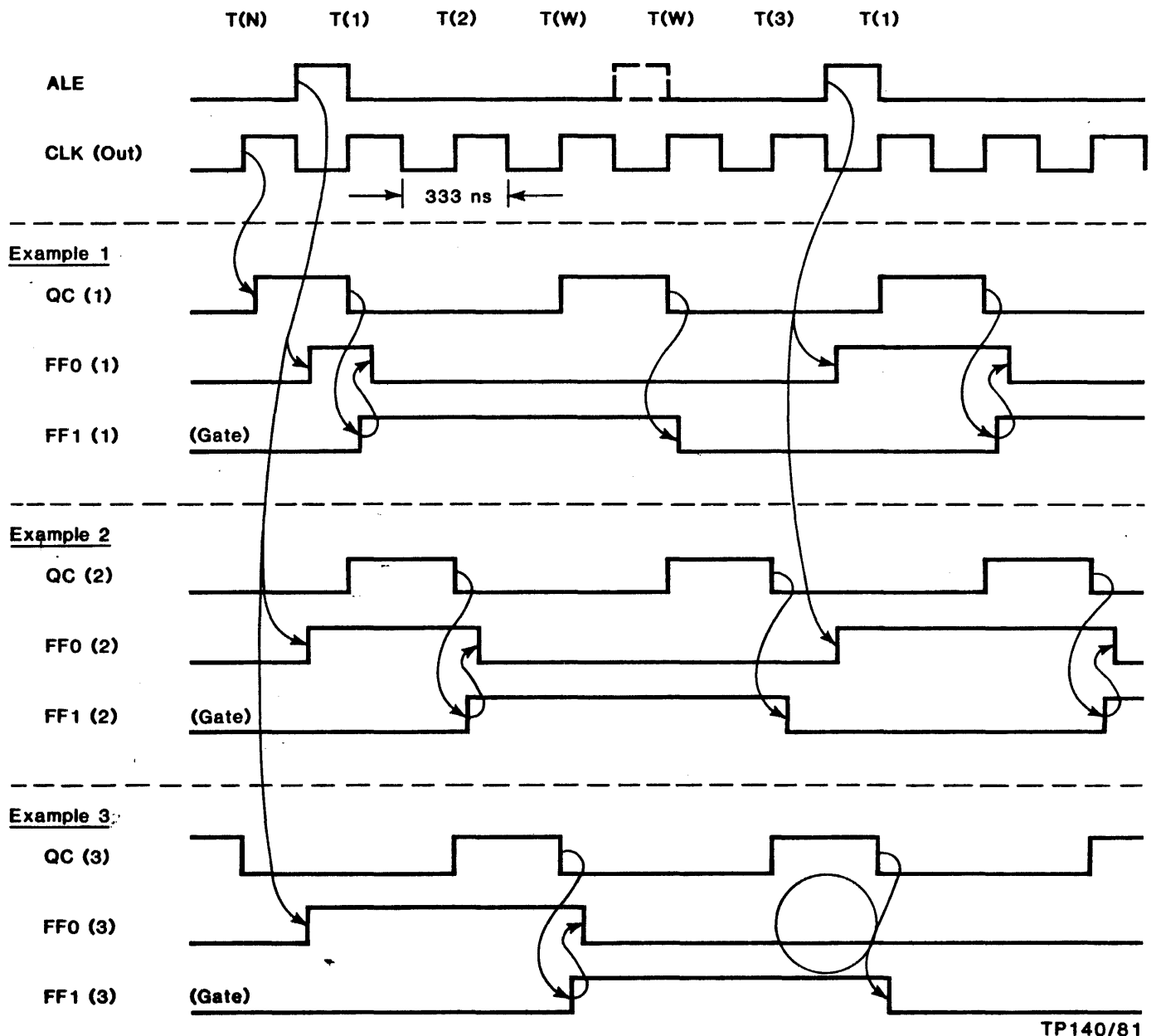


Figure 3-18. Watchdog Timer Timing

Counter No. 3: The third counter section of the 8253 timer is used to verify the accuracy of the VCO in the phase-locked-loop. This counter is used by the hardware self-test to count the number of VCO cycles during a given period, as measured by the 8085 12 MHz crystal oscillator. This timing measurement is done under software control, and the output is read through the 8253 software registers. The 8253 ports are assigned as shown below:

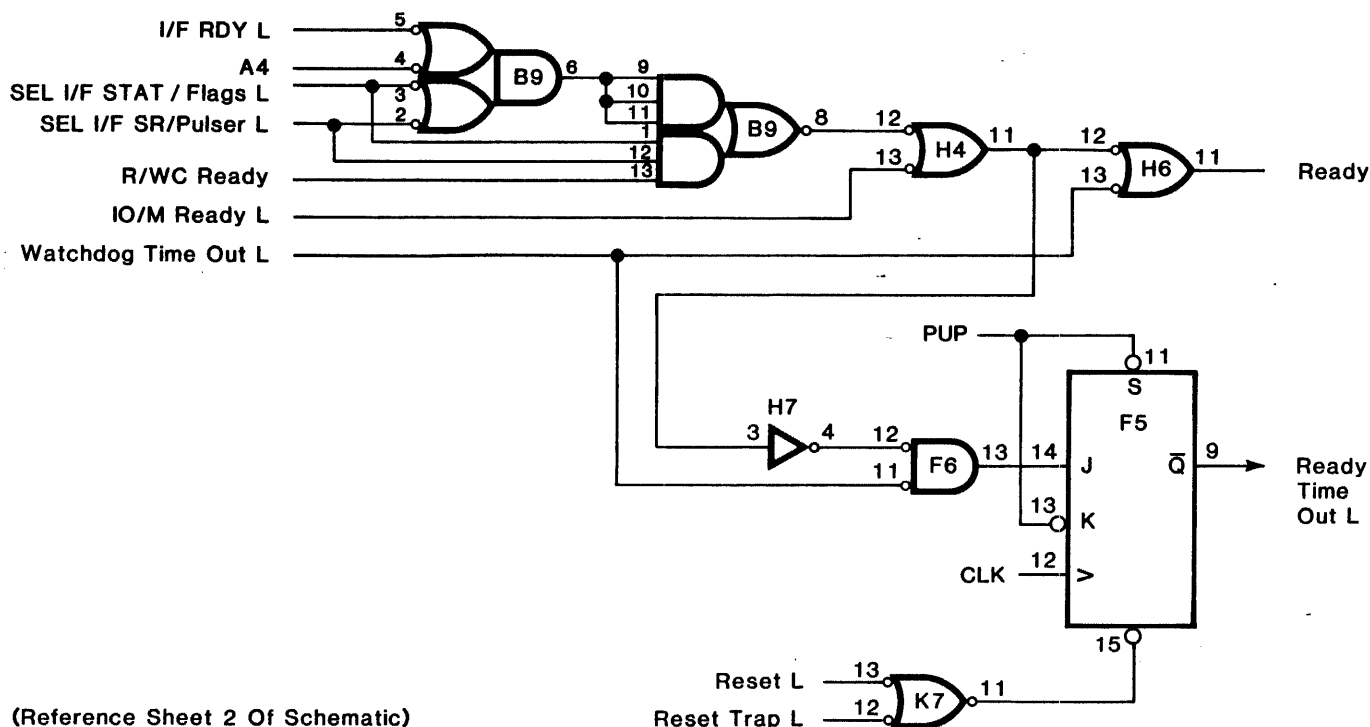
<u>Port Number</u>	<u>Use/Comment</u>
40	VCO counter test access port
41	Timeout counter access port
42	DMA fill/empty counter access port
43	8253 control port - write only (Sets the mode of the ports 40 through 42 described in the Intel/NEC Product Data Books.)

8085 Ready Logic: Figure 3-19 shows the READY hardware logic that drives the 8085 READY input. The Ready line is used to inhibit 8085 operation when the interface has been accessed and the interface is not ready, or when the R/WC is not ready and the 8085 is not trying to access the interface (during read/write operations for example). The READY logic derives its inputs from the decoder PROMs, the R/WC Status line, the watchdog timer, and Address line A4.

If the controller has failed due to a ready timeout, the watchdog timer will force the READY signal. After the ready has been asserted, the 8085 will be forced into a timeout routine by an interrupt, also caused by the watchdog timer.

It is possible to access the interface without inhibiting ready, by accessing the interface at addresses B0 to BF for interface STATUS, or 90 to 97 for interface DATA. This causes Address line A4 to be low (0) and will cause the Ready line to be asserted. Refer to the discussion on the watchdog timer.

One unique feature of the I-Bus cable is the ability of the master controller to diagnose a cable that has been installed backwards. Pins 1 through 13 are all connected together to ground on both the controller module and the interface module. If the I-Bus cable is installed incorrectly, all the signals (pins 14 through 26) will be shorted together instead of all the grounds on pins 1 through 13. Refer to Figure 3-20. During the cable reversal test, the 8085 asserts Data-To-CPU and IFDATA lines to provide a sufficient current sink. The IDONE signal is asserted, at this time, by E9-11. The 8085 looks at IDONE through E9-2. If the cable is backwards, it will be low. If the cable is installed correctly or is missing, it will be high.



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Figure 3-19. READY Hardware Logic

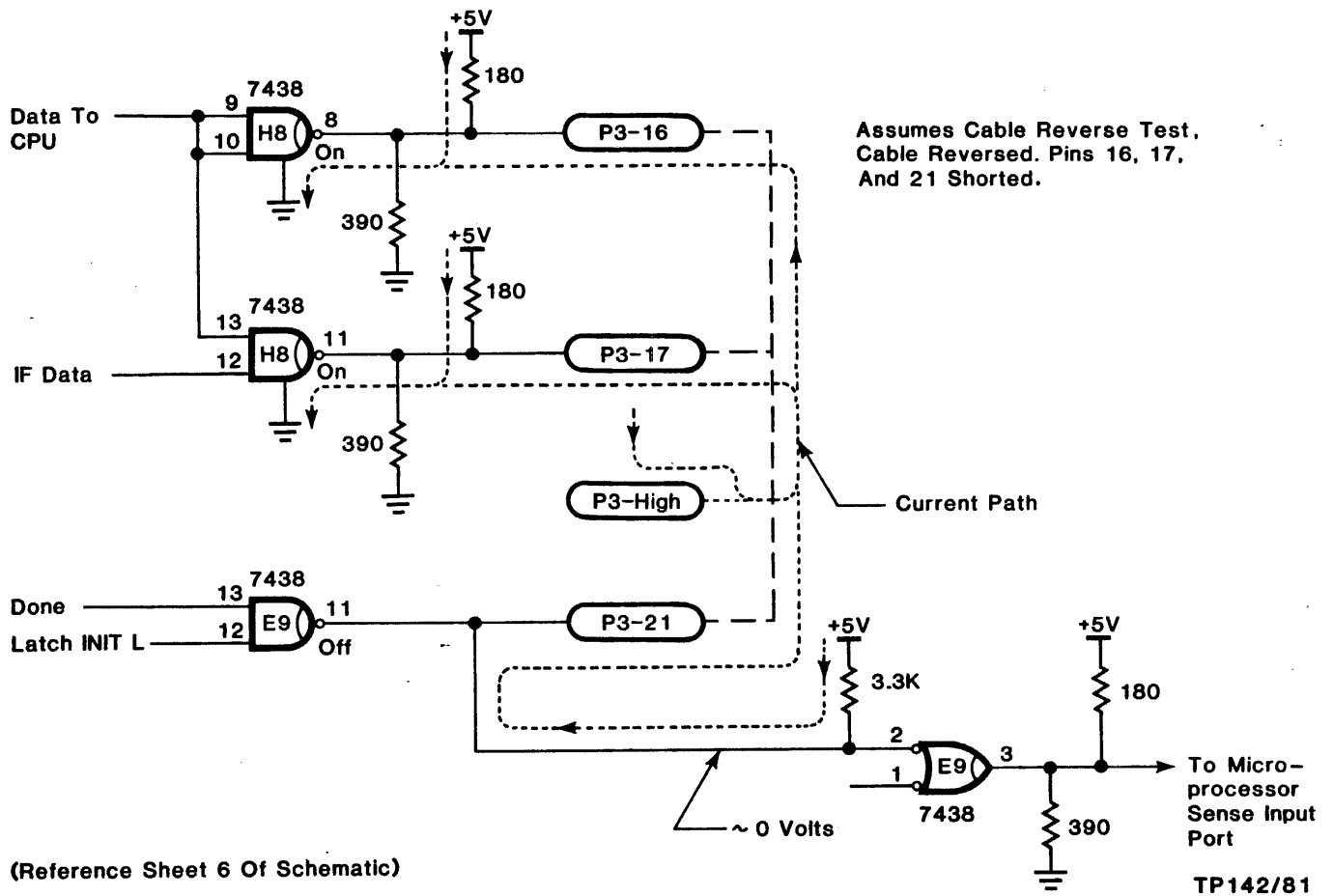


Figure 3-20. Cable Reversal Test Logic

Controller Interface To The I-Bus

There are six input lines into the controller from the 26-pin I-Bus cable. Two of the lines, IFDATA L and IERROR L, are bidirectional. The IDMA mode, I12BM, IFRDY, and IERROR I-BUS lines are fed into the 8085 via the tri-state buffer at location D8. These lines may be read by doing an I/O read operation at the If STAT/FLAGS port (addresses A0 through AF or B0 through BF).

The IF INIT input is used to clock the latched INIT flip-flop at F8. This FF may be read at any time after it has been latched. This allows an INIT to occur while the 8085 is engaged elsewhere. The INIT can still be recognized later.

The IF DATA input is fed into the interface shift register and into the parity check circuit. The parity check circuit performs a parity test on all shifted data from the interface. The parity check circuit is also driven by the PULSER circuit of the 8085. This allows the parity check circuits to be tested by forcing and clearing the parity error, and checking that the circuit output is valid.

An integral part of the interface circuitry is the shift circuit which consists of FFs at J5, J6, and the counter at J7. See Figure 3-21. This circuit produces the actual shift pulses used to shift the I/F data. The number of shifts can only be done in multiples of four or eight shifts, depending upon the D input of the counter. A simplified schematic and timing diagram are shown in Figure 3-22 for the case of the 4-bit shift and data going both from and to the floppy.

The direction of the data on the I-Bus cable is determined by the 8085 controller with the Data-To-CPU line. This line is driven by the latched control bits at F9. This line is used to determine the direction of the shifts in the interface shift register, and as an output to the interface.

Transfer Request Flag (IFTRCL)

The transfer request flag is generated by the D flip-flop at location F8, or by asserting the latched bit (bit 7) from the 9334 at location F9. See Figure 3-23.

Several features of the transfer request flag have been optimized for speed. This occurs for several reasons. First, the transfer request controller receives a valid IFRDY signal. IFRDY is only asserted when the I/F has valid data for the controller. Secondly, the transfer request flag has been used to start shifting the data. This is accomplished by starting the begin shift sequence when the transfer request goes away. This eliminates the over head associated with the 8085 having to detect IFRDY and starting the shift process.

This ability of the transfer request to start the shift sequence is used in the instruction IN IFTRCL and OUT IFTRCL. These instructions allow the 8085 to complete a sequence of events by using only one instruction. This speed is used in the DMA transfer of data during the fill/empty commands. By having the transfer request start the shift, there are approximately seven to ten, 8085 cycles saved per word. This accounts for 256 words X 2 microseconds equaling approximately 500 microseconds in a typical sector transfer.

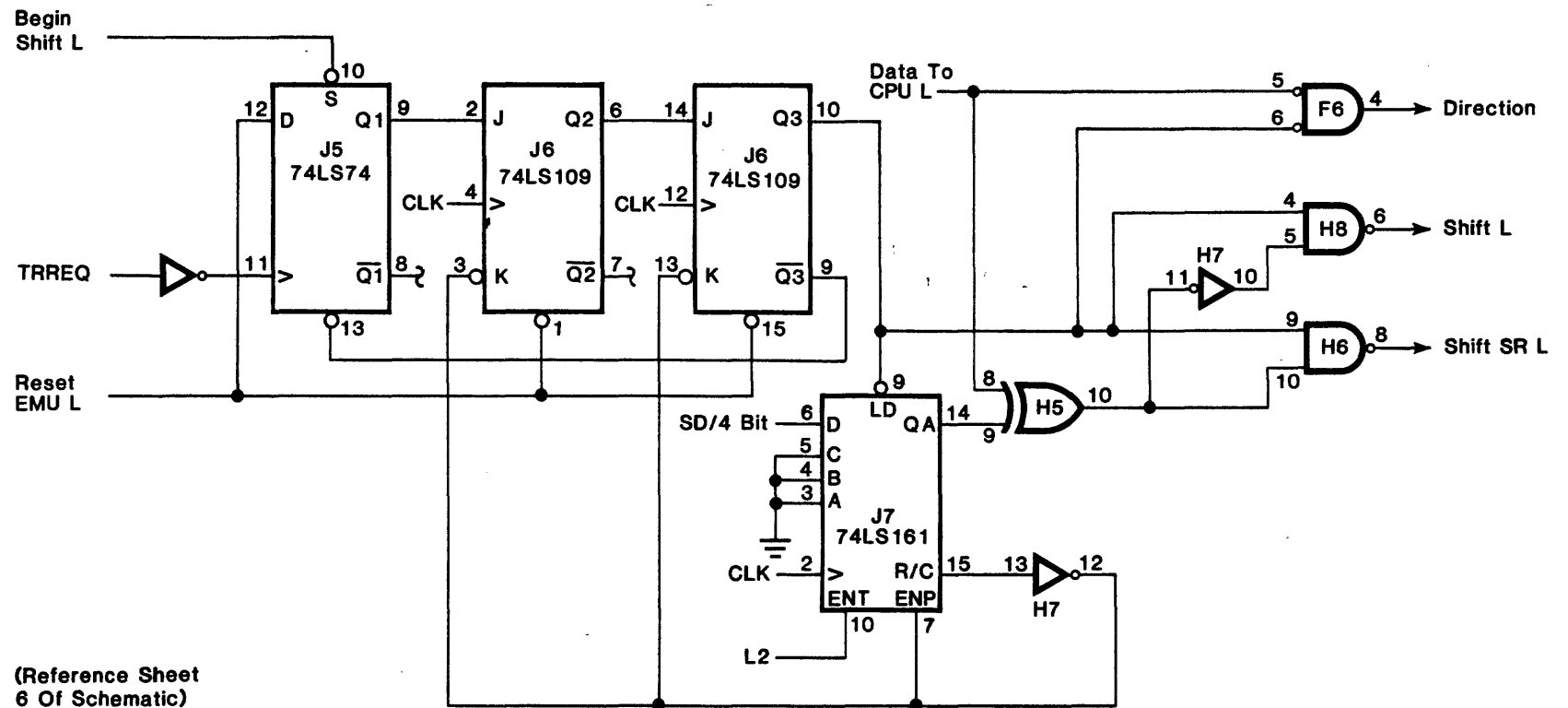
The OUT IFTRCL command does the following:

1. Outputs content of accumulator to the I/F shift register
2. Sets the transfer request flag
3. Starts shift when IFRDY is asserted at interface and is request flag

The IN IFTRCL command does the following:

1. Loads accumulator with the current contents of shift register
2. Sets the transfer request flag asking for next data byte
3. Starts shift of next byte when data is ready as indicated by IFRDY being asserted

The transfer request is cleared by an EMU RESET, the INTERFACE RDY being asserted, or by the CLR SR pulse from the 8085.



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Figure 3-21. IF Cable Interface

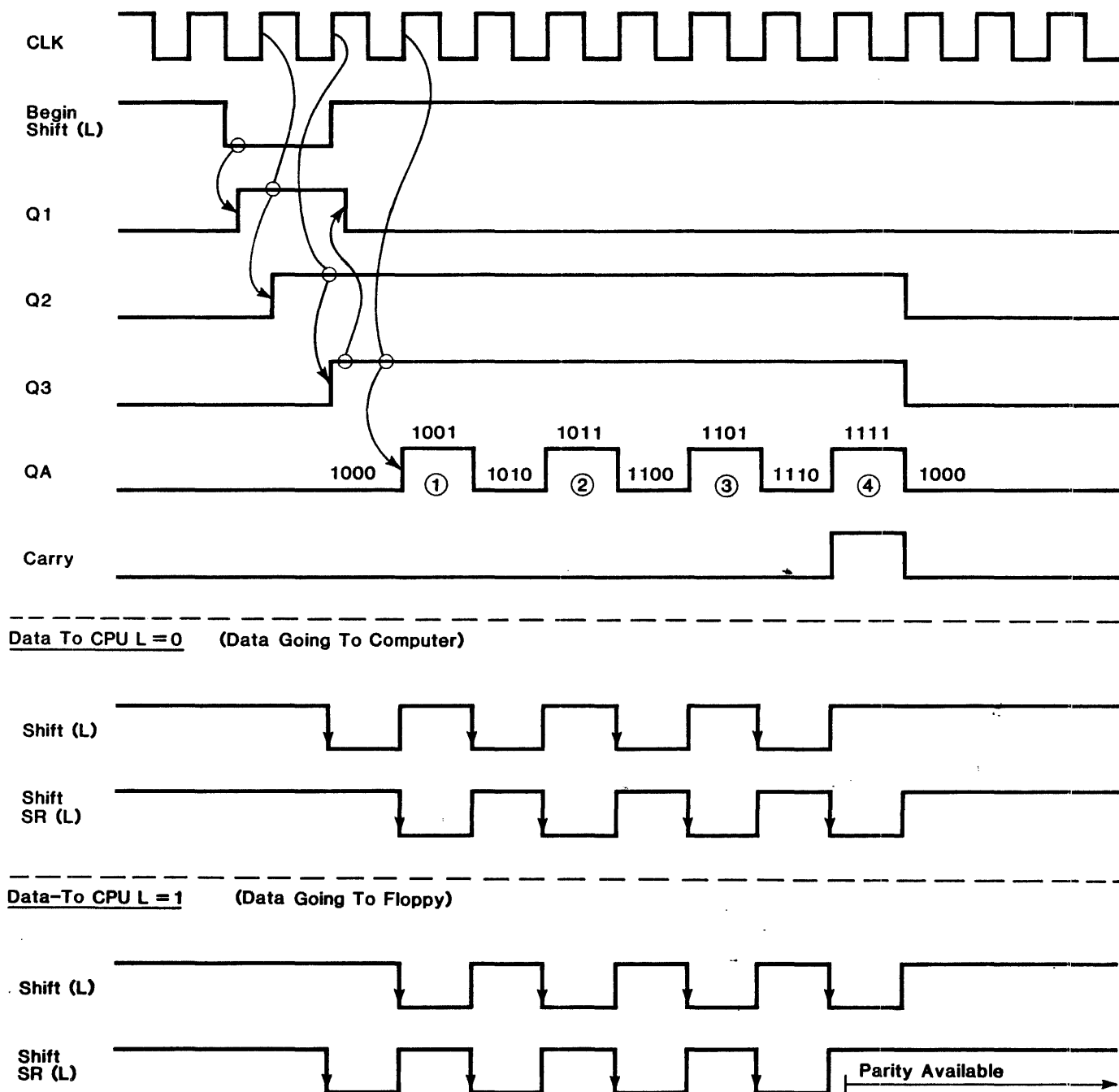
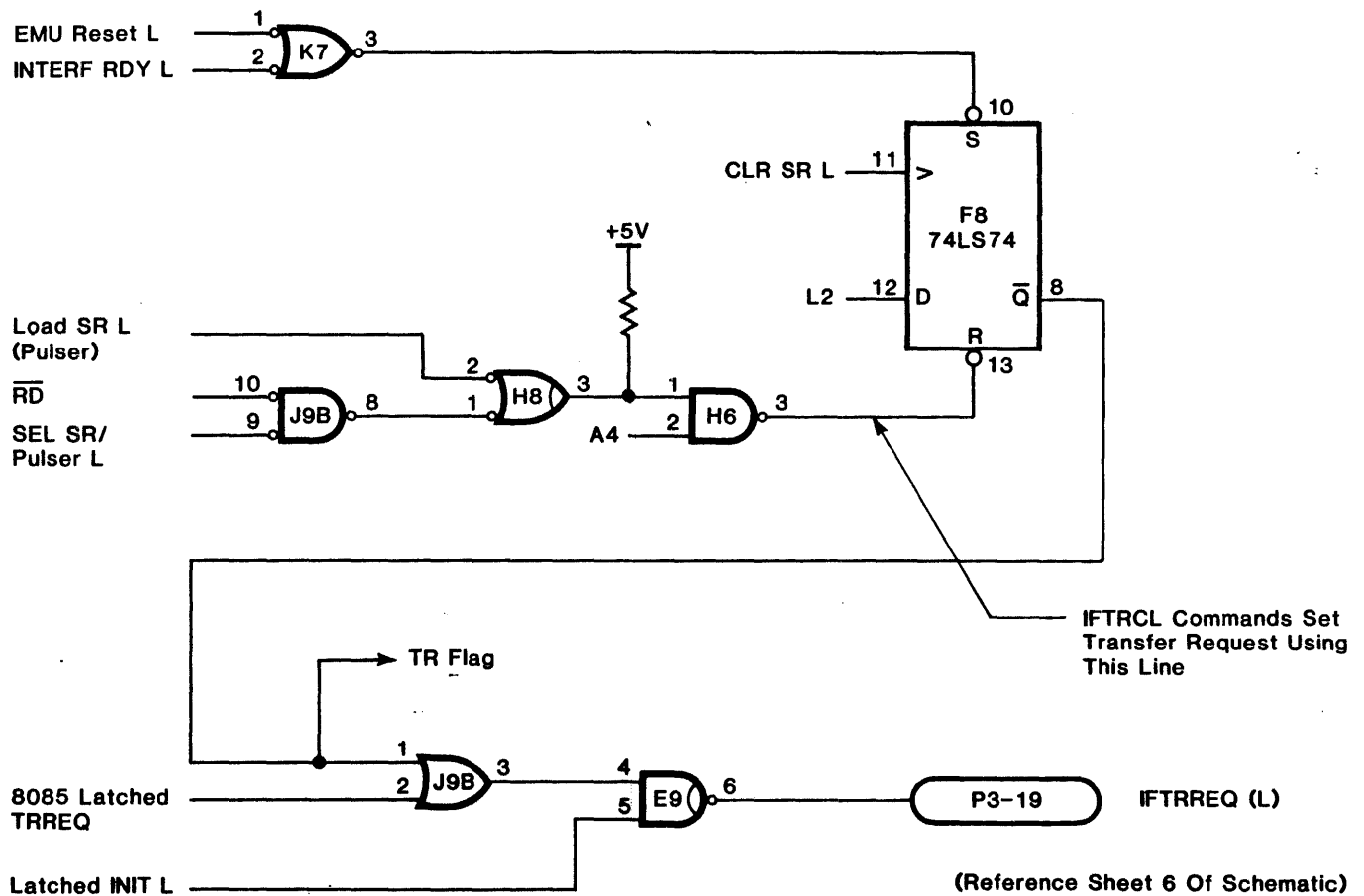


Figure 3-22. Shift Circuit Timing

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EMU Reset

The EMU RESET is generated at the 8085 pulser circuit. This output is used to reset the LATCHED INIT, the shift circuit, the parity check circuit, and the TRANSFER REQUEST FLAG. It is also used to do testing of the parity and LATCHED INIT circuits.



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Figure 3-23. Transfer Request Circuit

Floppy Disk Drive Cable Connections

Table 3-3 defines the 50-conductor drive bus cable. Pin 11 is removed and is plugged on the mating connector to act as a key. The signal DISK CHANGE does not really have an individual ground line associated with it. The connector is male, denoted P1 on the schematic. The even numbered pins are signals, while the odd numbered pins are grounds. Pin 1 is located closest to the dipswitch. Backwards cable installation can be sensed by the microprocessor by reading the Drive Compensate line on P1-2. If the cable is installed backwards, all the signals will be shorted together (on the ground plane) and drive compensate will be sensed as being low.

Table 3-3. Disk Drive Cable

Pin Number		Used on Shugart Drive	Signal Name		Source	Terminated at (2)
Signal	Ground					
2	1	850	Drive Compensate L	MUX	Controller	Disk
4	3	800/850	WPZ L		Disk (1)	Controller
6	5	800/850	WPI L		Disk (1)	Controller
8	7	800/850	LED Z L		Controller	Disk
10	9	850	Two-Sided L	MUX	Disk	Controller
12	11	800/850	Disk Change L	MUX	Disk	Controller
14	13	850	Side Select L	MUX	Controller	Disk
16	15	800/850	LED 1 L		Controller	Disk
18	17	800/850	HEAD LOAD L	MUX	Controller	Disk
20	19	800/850	Floppy Index L	MUX	Disk	Controller
22	21	800/850	READY L	MUX	Disk	Controller
24	23	—	(Not used)		—	—
26	25	800/850	US1 L		Controller	Disk
28	27	800/850	US2 L		Controller	Disk
30	29	800/850	US3 L (3)		Controller	Disk
32	31	800/850	US4 L	MUX	Controller	Disk
34	33	800/850	STEPIN L (4)	MUX	Controller	Disk
36	35	800/850	STEP L	MUX	Controller	Disk
38	37	800/850	WRITE DATA L	MUX	Controller	Disk
40	39	800/850	WRITE GATE L	MUX	Controller	Disk
42	41	800/850	TRK 00 L	MUX	Disk	Controller
44	43	800/850	WRITE PROTECT L	MUX	Disk	Controller
46	45	800/850	READ DATA L	MUX	Disk	Controller
48	47	800/850	LED3 L		Controller	Disk
50	49	800/850	LED4 L		Controller	Disk

- Notes:
1. WP1 L and WP2 L are generated by user-supplied switches wired to individual disk drives.
 2. Terminators are either 180/390 pairs, or 150 Ω pull-ups.
 3. Shugart numbers drives as 1 through 4 (as in US1, US2, US3, US4).
 4. Signals with MUX after them are multiplexed lines connected to all drives in the chain. Termination would only be at the drive at the end of the chain.

The controller can individually assert, or negate the drive LED lines for use in error reporting. The controller, upon detection of an error, will flash the door LED on the drive associated with the problem. The LED lines and the Unit Select lines are driven by the 8155 RAM/I/O chip described in the 8085 NUCLEUS write up. These lines are accessed through Port B of the 8155. The Unit Select lines are 26, 28, 30, and 32 on the drive cable. The LED lines are 8, 16, 48, and 50.

The 8155 port C controls the drive Side Select, Head Load, Step Direction, and Drive Compensation lines to the floppy drive. These lines are time multiplexed with the Unit Selection lines.

Time multiplexing allows the same drive lines to be used for several drives at the same time. The signal has significance only if one of the Unit Selection lines are asserted.

All the output lines to the drive are driven by open collector drivers. This prevents possible problems when the cable is inserted backwards.

The line inputs into the controller were described in the 8085 section of this manual. The lines were: Disk Protect, Ready, Track 0 Sense, Disk Changed, Write Protection Switch 1, Write Protection Switch 2, and Floppy Index Sense.

The index and unseparated data from the drive are both available to the R/WC as two of the conditional branch input lines. Refer to the R/WC branch circuit for more detail on these lines.

The last three signal lines on the drive cable are: Write Data, Write Gate, and Read Data. The Write Data line is generated in the serial data path circuit, refer to that section for more detail. The Write Data line is buffered by an open collector driver before leaving the controller.

The Write Gate signal is used to enable the writing of data on the floppy disk. The Write Gate line is generated as the logical AND of the 8155 write gate enable output and the R/WC Write Gate. The signal is then qualified by the System Reset line of the controller. This enables the Reset line to discontinue the write operation if a reset occurs. The Reset line also prevents any garbage data from being written while the R/WC is being reset.

The Read Data input is received by the master controller and is shaped by two one-shot circuits. The outputs of the one-shots are used to drive the phase-lock-loop (PLL) and UD input of the R/WC. Refer to the R/WC conditional branch logic description, and to the PLL description for more information.

3.5 Read/Write Controller (R/WC)

The Read/Write Controller provides the necessary speed and logic to interface the 8085 controller to the floppy drive data and status. It has been designed to provide the necessary functions required to read, write, and format diskettes written with DEC double-density, IBM double-density, or IBM single-density.

As shown in the block diagram of Figure 3-24, the R/WC is a bit-slice microprocessor. The clock, PL CLK, is a 333 nanosecond clock derived from the 8085 clock output and buffered to drive the various R/WC devices. Not shown in the block diagram, but included in the R/WC, are the necessary lines to interface the controller to external RAM/ROM test/development of the read/write microcode.

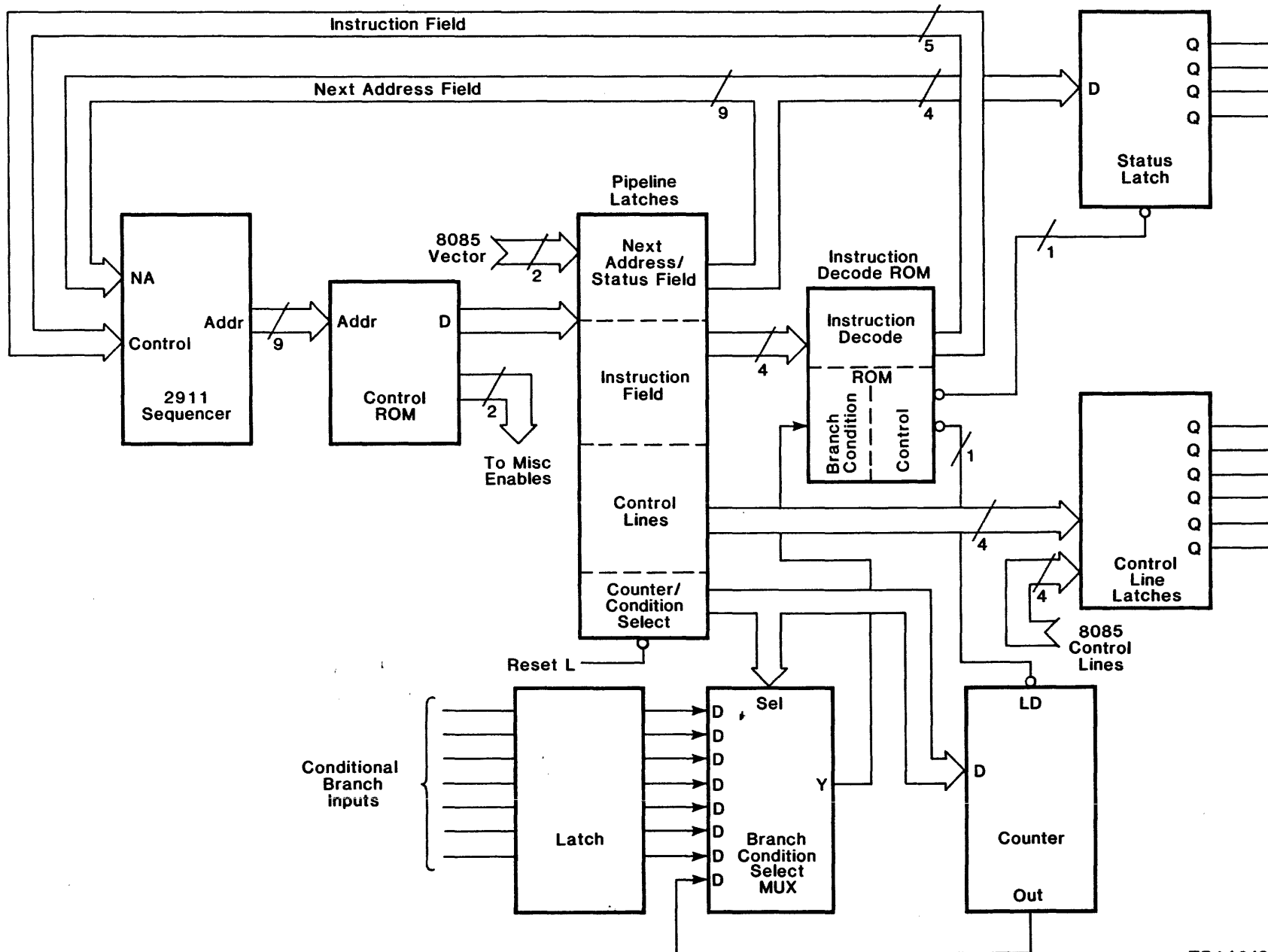


Figure 3-24. Read/Write Controller Block Diagram

Table 3-4. Bit Controller Instructions

I3 to I0	Mnemonic	Definition	Test	Destination	Stack	S0	S1	FE	PUP	RE	LDST		LD CTR
0 0 0 0	JUMP	Jump to next address	- -	Next Addr -	No Change -	1 -	1 -	1 -	0 -	1 -	1 -	-	1 -
0 0 0 1	CBR	Conditional branch to next address, if test true	0	+.1	No Change	0	0	1	0	1	1		1
			1	Next Addr	No Change	1	1	1	0	1	1		1
0 0 1 0	CBRF	Conditional branch to next address, if test false	0	Next Addr	No Change	1	1	1	0	1	1		1
			1	+.1	No Change	0	0	1	0	1	1		1
0 0 1 1	JMS	Jump to subroutine	-	Next Addr	Push	1	1	0	1	1	1		1
			-	-	-	-	-	-	-	-	-	-	-
0 1 0 0	CJMS	Conditional jump to subroutine if test true	0	+.1	No Change	0	0	1	0	1	1		1
			1	Next Addr	Push	1	1	0	1	1	1		1
0 1 0 1	CJMSF	Conditional jump to subroutine, if test false	0	Next Addr	Push	1	1	0	1	1	1		1
			1	+.1	No Change	0	0	1	0	1	1		1
0 1 1 0	RTN	Return from subroutine	-	Top of Stack	POP	1	0	0	0	1	1		1
			-	-	-	-	-	-	-	-	-	-	-
0 1 1 1	CRTN	Conditional return from subroutine, If test true	0	Next Addr	No Change	1	1	1	0	1	1		1
			1	Top of Stack	POP	1	0	0	0	1	1		1
1 0 0 0	CRTNF	Conditional return from subroutine, if test false	0	Top of Stack	POP	1	0	0	0	1	1		1
			1	Next Addr	No Change	1	1	1	0	1	1		1
1 0 0 1	CBRR	Next address, if test false; REG if test true	0	Next Addr	No Change	1	1	1	0	1	1		1
			1	REG	No Change	0	1	1	0	1	1		1

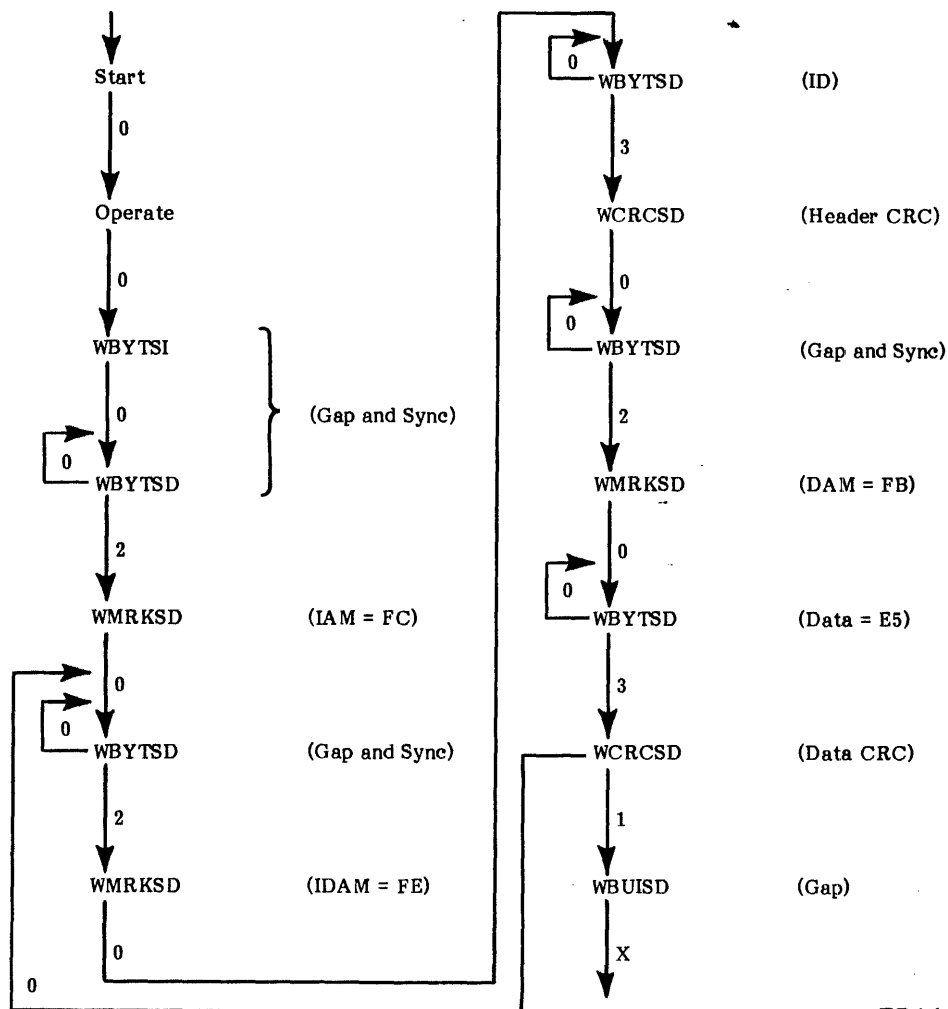
Table 3-4. Bit Controller Instructions (Cont)

13 to I0	Mnemonic	Definition	Test	Destination	Stack	S0	S1	FE	PUP	RE	LDST		LD CTR
1 0 1 0	STATUS	Continue, and load status	-	+.1	No Change	0	0	1	0	1	0		1
			-	-	-	-	-	-	-	-	-	-	-
1 0 1 1	CJMSR	Jump to subroutine @ next address if test false; @ REG if test true	0 1	Next Addr REG	Push Push	1 0	1 1	0 0	1 1	1 1	1 1		1 1
1 1 0 0	CJMSRF	Jump to subroutine @ REG, if test false; @ next address, if test true	0 1	REG Next Addr	Push Push	0 1	1 1	0 0	1 1	1 1	1 1		1 1
1 1 0 1	LDRC	Load register and counter	-	+.1	No Change	0	0	1	1	1	1		0
			-	-	-	-	-	-	-	-	-	-	-
1 1 1 0	BRLC	Branch to next address and load counter	-	Next Addr	No Change	1	1	1	0	1	1		0
			-	-	-	-	-	-	-	-	-	-	-
1 1 1 1	CRTNRF	Conditional return from subroutine, if test false; REG if test true	0 1	Top of Stack REG	POP POP	1 0	0 1	0 0	0 0	1 1	1 1		1 1

Notes: TEST is defined as "SEL 3 (Bit15)" + "MUX W"

Macros: RTN is defined as, CRTN .+1,,
 JMS is defined as, CJMS DEST,,
 NOOP is defined as, CBR .+1,,
 JUMP is defined as, CBR DEST,,
 OVERRUN is defined as, JUMP OVERUN,,,READY

Another very important function of the next address field is to provide vectoring information for the R/WC from the 8085 microprocessor. The R/WC is set up in functional blocks of microcode. At the completion of the normal functions, the R/WC will prepare to receive one of four instructions based on what the current instruction was. Depending upon the current instruction, the R/WC may wait for an instruction, or it may expect the 8085 to have already given a new instruction. In the latter case, the 8085 will have gone into a wait state. This may be checked by the R/WC. If an instruction is not present when required, an overrun occurs. The instruction vector is passed as the lower order two bits in the next address field. The two bits used for vectoring are selected in the 8085 code by doing an In or Out instruction to ports E0 through E3. The lower two bits of the 8085 address bus are used to create the instruction vector. The actual use and decoding of these two bits is controlled by the R/WC. The contents of the accumulator are not used in the vector process. The microcode of the R/WC can choose to ignore the two lower bits by proper selection of the Enable Vector line inside the R/WC. Note that a maximum of four vectors may be sent to the R/WC during each vectoring process. The functions are set up so that all 25 functions may be reached by suitably ordering the functions required to do a task. For example, at reset the R/WC will do a self-test sequence. This sequence will leave the controller in the start function. From the start function the R/WC can be vectored into the operate, delays, or delayed mode of operation. An example of this functional sequence is given in Figure 3-26. This is an example of how an IBM single-density diskette would be formatted. Table 3-5 is a complete list of the individual R/WC function, and what the vectors 0, 1, 2, and 3 will cause to happen next.



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Figure 3-26. Functional Sequencing Example

Table 3-5. R/WC Vectoring

<u>From</u>		Vector			
		0	1	2	3
START		OPERATE	<OVER>	DELAYS	DELAYD
OPERATE		WBYTSI	FMRKDD	FPRES	WBYTDI
FIND SD PREAM	(FPRES)	FMRKSD	FMSDDD	<OVER>	<OVER>
FIND SD MARK	(FMRKSD)	RBYTSD	RCRCSD	FPRES	START
FIND SD MARK IN DD	(FMSDDD)	RBYTDD	FMRKDD	RCRCDD	<OVER>
FIND DD MARK	(FMRKDD)*	RBYTDD	FMRKDD	RCRCDD	<OVER>
READ BYTE SD	(RBYTSD)	RBYTSD	RCRCSD	FPRES	START
READ BYTE DD	(RBYTDD)	RBYTDD	FMRKDD	RCRCDD	START
READ CRC SD	(RCRCSD)	START	<OVER>	DELAYS	DELAYD
READ CRC DD	(RCRCDD)	START	<OVER>	DELAYS	DELAYD
WAIT INDEX, WRT BYTE SD	(WBYTSI) *	WBYTSD	WLASTS, START	WMRKSD	WCRCS
WAIT INDEX, WRT BYTE DD	(WBYTDD) *	WLASTD, START	WBYTDD	WMRKDD	WCRCD
WRITE BYTE SD	(WBYTSD)	WBYTSD	WLASTS, START	WMRKSD	WCRCS
WRITE BYTE DD	(WBYTDD)	WLASTD, START	WBYTDD	WMRKDD	WCRCD
WRITE MARK SD	(WMRKSD)	WBYTSD	WBYTDD	<OVER>	<OVER>
WRITE MARK DD	(WMRKDD)	WLASTD, START	WBYTDD	WMRKDD	WCRCD
WRITE CRC SD	(WCRCS)	WBYTSD	WBUISD	TSTCRC	WCRCS
WRITE CRC DD	(WCRCD)	WBUIDD	WBYTDD	TSTCRC	WCRCD
DELAY SD	(DELAYS)	START	FPRES	DELAYS	W1BTSD
DELAY DD	(DELAYD)	START	FMRKDD	W1BTDD	DELAYD
WRITE 1st BYTE SD	(W1BTSD) *	WBYTSD	WLASTS, START	WMRKSD	WCRCS
WRITE 1st BYTE DD	(W1BTDD) *	WLASTD, START	WBYTDD	WMRKDD	WCRCD
WRT BYTE SD UNTIL INDEX	(WBUISD)	START	START	START	START
WRT BYTE DD UNTIL INDEX	(WBUIDD)	START	START	START	START
TEST CRC BY READ CRC GEN. (TSTCRC)		START	START	START	START

↑ * = NO READY

Branch Condition Selection and Counter Loading

The specific branch condition and the counter load value are both selected by the Read/Write Controller lines SEL0 through SEL3. These are generated from the microinstruction bits P15 to P12. The type of instruction determines the purpose of these bits. During conditional branch or subroutine jumps, these instructions can select the desired test condition. The actual condition selected is shown and described as follows.

<u>Pipeline</u>				<u>Assembler Mnemonics</u>	<u>Comments</u>
15	14	13	12		
0	0	0	0	NPLMTM	Not phase-lock-loop time
0	0	0	1	COUNT	Ripple carry of counter
0	0	1	0	NWAIT	8085 not waiting for R/WC
0	0	1	1	RAWDAT	Unseparated data
0	1	0	0	PLLDTI	PLL Data = 1
0	1	0	1	INDEX	Diskette index hole seen
0	1	1	0	CRCERR	CRC generator error flag
0	1	1	1	DTOUT	Data out = 1

If the instruction is a load counter function, the negative value of the number of counts is loaded into the counter. The counter will count up until the carry is set and carry bit is used as a condition flag for the R/WC. Notice that the mnemonic used represents the actual count value desired. This avoids some of the confusion involved in making the calculations required to load the counter. See the following.

LOAD COUNTER

<u>Pipeline</u>				<u>Assembler Mnemonics</u>
15	14	13	12	
0	0	0	0	M15
0	0	0	1	M14
0	0	1	0	M13
0	0	1	1	M12
0	1	0	0	M11
0	1	0	1	M10
0	1	1	0	M9
0	1	1	1	M8
1	0	0	0	M7
1	0	0	1	M6
1	0	1	0	M5
1	0	1	1	M4
1	1	0	0	M3
1	1	0	1	M2
1	1	1	0	M1
1	1	1	1	ZERO

Read/Write Controller - Control Lines

The Read/Write Controller code is written in a psuedo-assembly language. The microinstruction, previously described, controls the flow of action, but it does not do anything as far as the outside world is concerned. The actual control is done by various control fields in the microinstruction.

The Data Source control field consists of two bits, DS0 and DS1. DS0 is generated by BIT 30 and DS1 is generated by BIT 31 of microinstruction. These bits control the flow of the data through the serial data path. DS0 and DS1 are the control lines for a dual 4:1 MUX which can direct the write or read data to the shift registers, CRC generator, and/or the coder/decoder, as required. These bits are defined in Table 3-6 and in the serial data path description.

The control of the shift register functions are done by the R/WC lines SRC1 and SRC0. With these control lines, the R/WC can control shift direction and the loading of data into the shift register. These bits are not latched in the R/WC pipeline latches. The SRC1 and SRC0 lines are used as enable lines for the desired function. The actual operation occurs when the shift register is clocked by the PL CLK feeding the shift register. These bits are further defined in Table 3-7.

Table 3-6. Out Data Source Control Field

DS1	DS0	Mnemonic	Codec Source	Data Out Source
0	0	DATA	PLL DATA	PLL DATA
0	1	RD DATA	PLL DATA	DECODED DATA
1	0	CRC	CRC OUTPUT	WRITE DATA L
1	1	SR	SH.REG.QH(E7)	SH.REG.QH(E7)

Table 3-7. Shift Register Control

SRC1	SRC0	Mnemonic	Operation
0	0	(DEFAULT)	HOLD
0	1	SHIFT	SHIFT RIGHT
1	0	SHIFT L	SHIFT LEFT
1	1	LOAD	LOAD

SCR1 = Bit 29 of microinstruction.

SCR0 = Bit 28 of microinstruction.

The other control lines, used by the Read/Write Controller, are defined in Table 3-8.

Table 3-8. Output (EMIT) Bit Definitions

Bit	State	Mnemonic	Definition
17	0 1	Vector (Default)	Selects vector as next address (NA8,NA7,NA2,A1,A0)
18	0 1	Ready (Default)	Informs 8085 when bit controller is ready
19	0 1	CHState (Default)	Permits precomp, DEC mode, and write gate to take effect
20	0 1	Strobe (Default)	Strobes data into the coder/decoder
21	0 1	WRTSTB (Default)	Disk data write strobe
22	0 1	PRECRC (Default)	Presets the disk generator
23	0 1	CLKCRC (Default)	Clocks the CRC generator
24	0 1	ENCTR (Default)	Enables 4-bit counter to count
25	0 1	DISWDT (Default)	Disables the write data MUX (output = 0)
26	0 1	SYNCH (Default)	Synchronizes PLL with unseparated data from floppy
27	0 1	CLKTIM (Default)	Enables MFM (or DEC MFM) clock pulse generation

Read/Write Controller Branch Inputs: There are eight conditions upon which the R/WC can branch. These inputs are first conditioned, and then selected, by the 8:1 MUX at location M6. The selection is done by the microinstruction field SEL2, SEL1, and SEL0.

The conditioning of the input signals is done by the registers at locations M7 and M8. The three signals PLL DATA, UD, and INDEX are double-buffered to provide a glitch-free signal to the R/WC. The signals DATA OUT, CRCERR, and 8085 WAITING L are only buffered once because these signals are derived from the same clock as the R/WC. See Figure 3-27 for a simplified schematic of the signals discussed.

The VCO OUT input to the R/WC is further conditioned by the circuit shown in Figure 3-28. The differentiator circuit is designed to generate one 333 nanosecond wide, low going pulse, after VCO OUT is high, during a positive going edge of R/WC CLK.

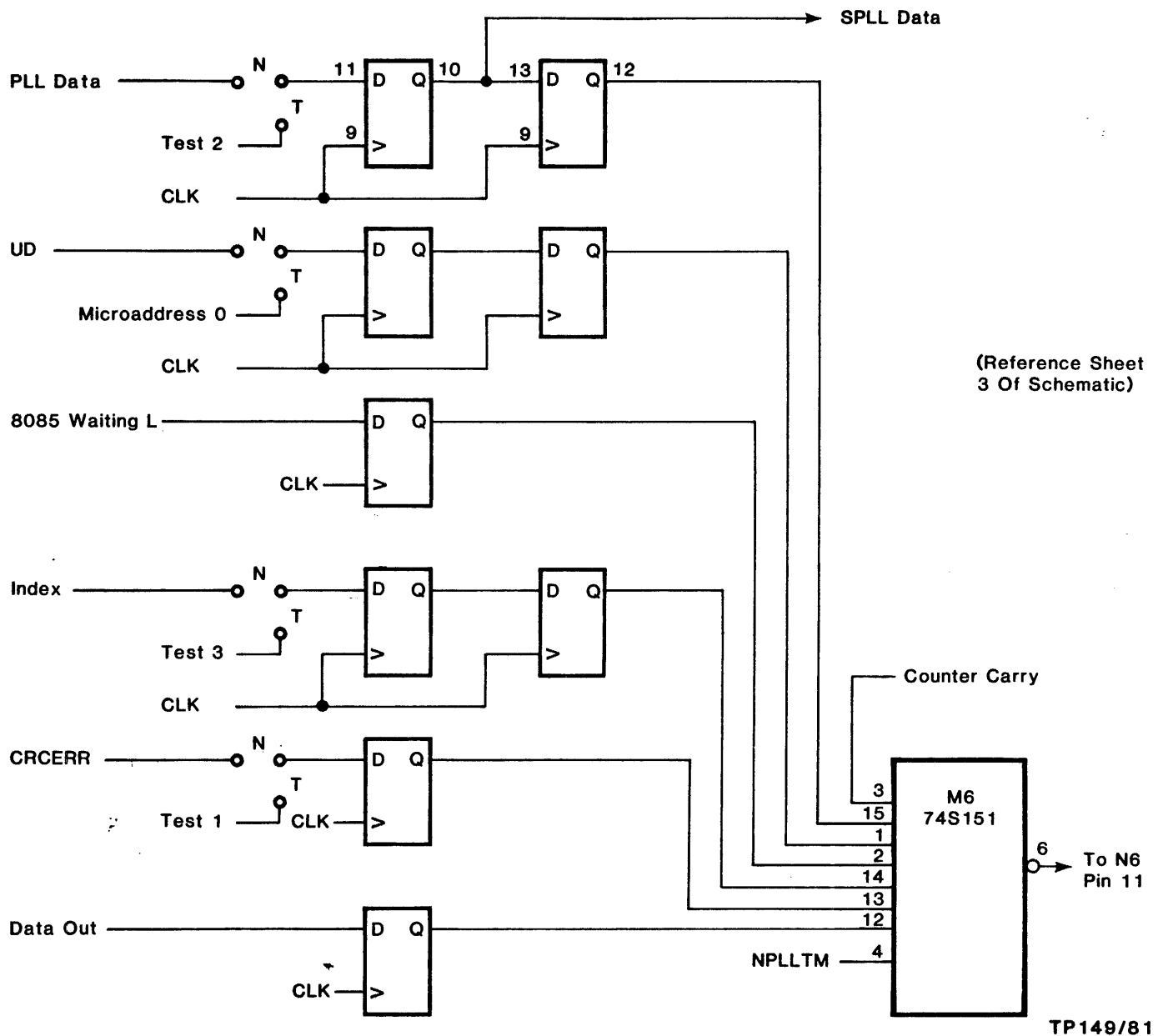
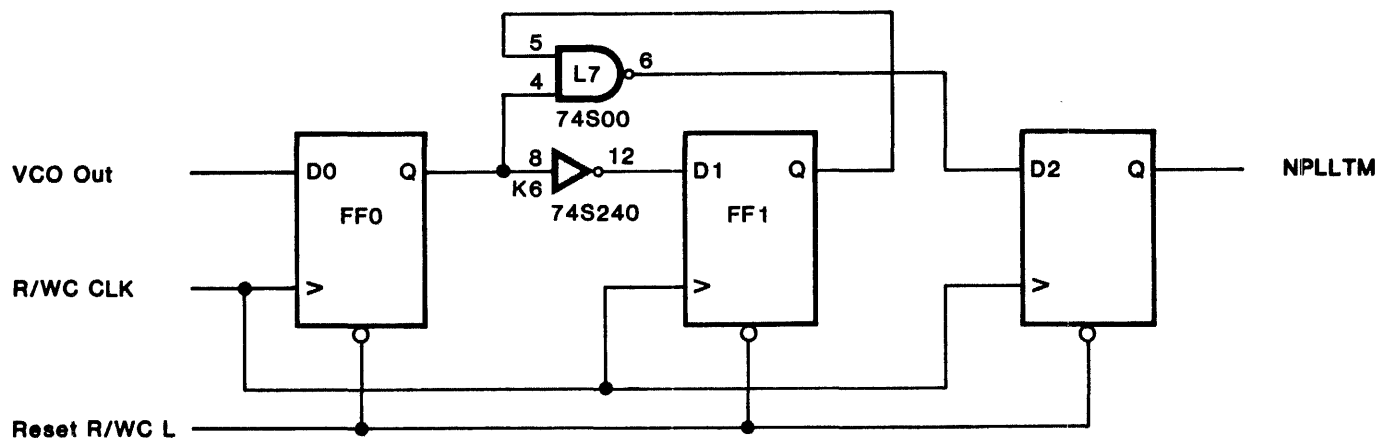
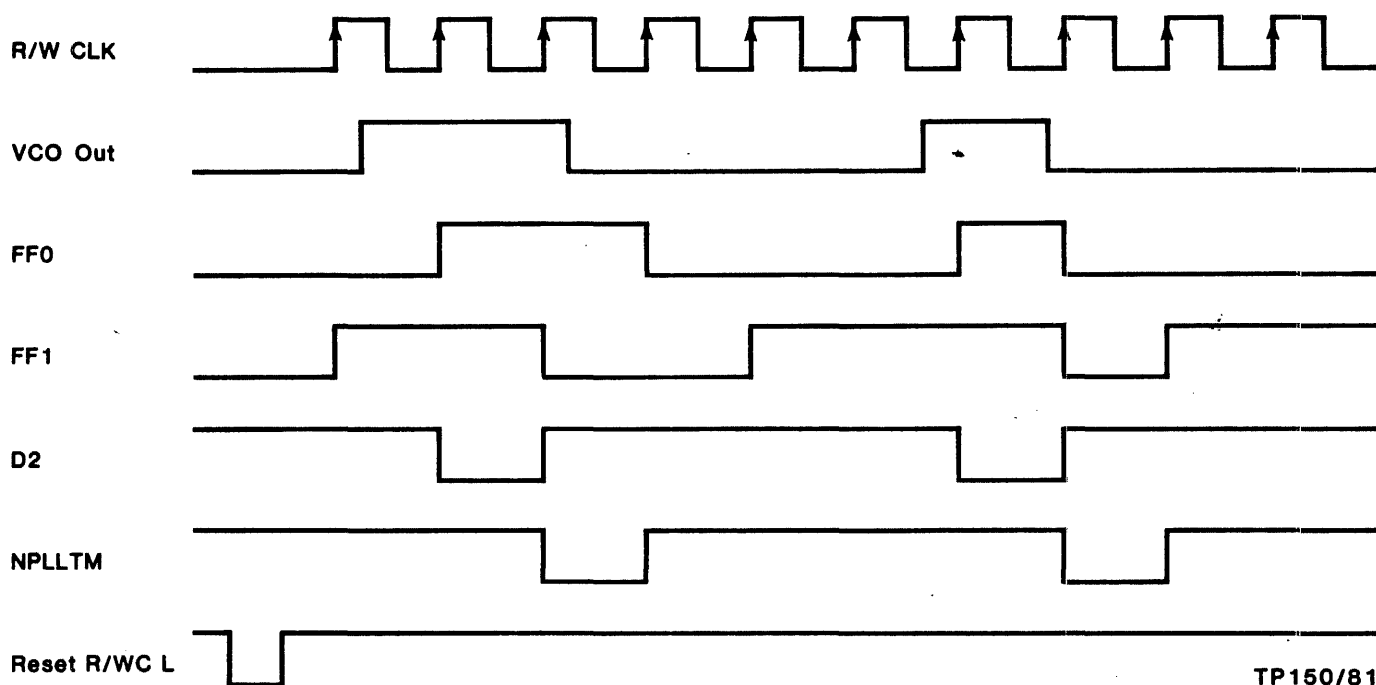


Figure 3-27. R/WC Branch Conditioning Circuitry

8085 Control Lines Synchronized by the R/WC: Four of the lines used in the PLL, serial data path area are generated by the 8085. These lines are: Precompensation, DEC Mode, DD/SD, and R/WC WRT GATE. These signals are passed by the R/WC through the registers in location H9. This conditioning allows the R/WC to inhibit the lines until it has completed its necessary functions. This register also acts to synchronize the 8085 Control lines to the PL CLK so that glitches are not produced in the external circuitry.



(Reference Sheet 3 Of Schematic)



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Figure 3-28. VCO Differentiator Conditioner

8085 - R/WC Vector Handshake Timing: There are two cases to be noted about the 8085 - R/WC vector handshake. The first case is when the R/WC has completed a function and is waiting for the next set of instructions. The R/WC does not time out and the 8085 can wait as long as required before the new vector is given. The R/WC will recognize the new vector when it samples the 8085 WAITING L line, and sees that the 8085 has given a command and is waiting for the R/WC to accept the command by asserting the R/WC Ready line. When R/WC READY is asserted, the 8085 can continue and the R/WC can perform its function.

The second case occurs when the R/WC has been processing a command and expects the 8085 to be waiting with a new command before the current command is completed. After the 8085 has given a command to the R/WC, the command is acknowledged by the R/WC asserting

the Ready line. When the 8085 receives the READY back, it can continue the processing it has. Before the R/WC is finished, the 8085 must have set up a new command. The R/WC can check for an overrun by verifying that the 8085 is waiting with a command. This technique is used in the read/write code of the 8085 to speed up the storing and checking of pertinent variables. In single-density format, the 8085 has approximately 32 microseconds to process information and set up the next command. In double-density, this time is reduced to 16 microseconds.

Read/Write Controller Status: When an error occurs, the Read/Write Controller normally alerts the 8085 by forcing an interrupt. The R/WC also outputs a status to the status register at K8. This register is a holding register for the error and allows the 8085 to request the status as part of the interrupt handler. The bits used to load the status register are the next address bits NA7 to NA4. The load status enable is provided by one of the output lines of the microinstruction decoder. The error type associated with each status code is shown below.

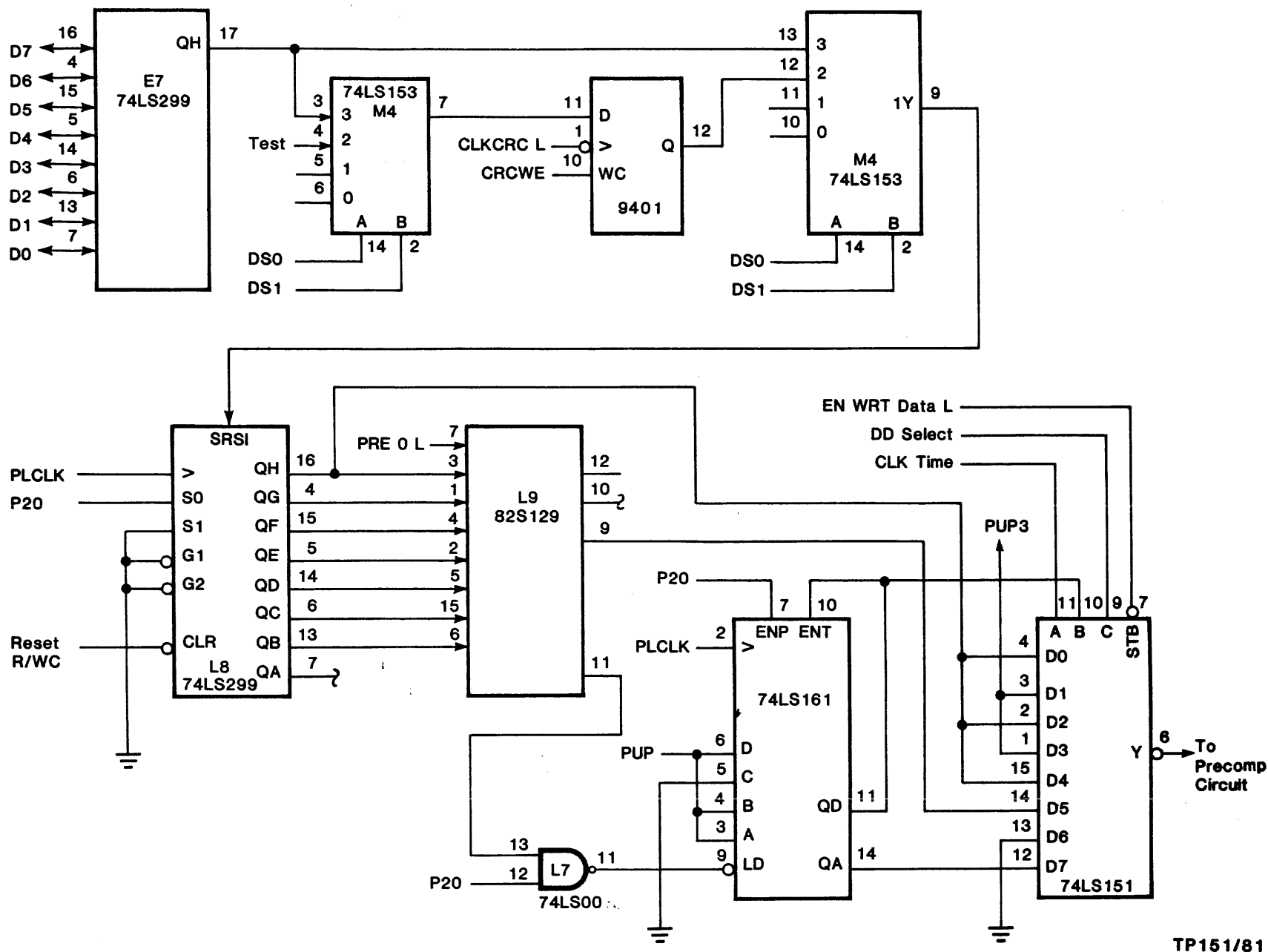
<u>Status</u>	<u>Mnemonic</u>	<u>Definition</u>
0000	K0	No error
0001	K1	R/WC overrun
0010	K2	48 microsecond time out
0011	K3	CRC error
0100	K4	Bad mark (SD or DD)
0101	K5	Not used
0110	K6	Bad preamble
0111	K7	Not used
1000	K8	Not used

3.6 Serial Data Path

The serial data path is the interface between the 8085 controller and the floppy disk drive data. The R/WC controls the data flow, depending upon the function selected by the 8085.

A simplified schematic of the serial data path is shown in Figure 3-29. The interface to the 8085 is done through the serial shift register at location E7. During a write operation, the 8085 data is written one byte at a time into the serial shift register. When a data byte has been written, the R/WC is given the command to write the data onto the diskette. This command causes the data to be shifted through the MUX circuits at location M4. From here the data is directed into the CRC generator and the encoder circuitry. While the data is being written, the CRC is calculated and stored in the 9401 CRC generator for recovery at the end of the write operation. Either data or the CRC may be written out to the diskette, depending on the MUX input selected by the R/WC lines DS0 and DS1.

The encoder circuit consists of a shift register/buffer, a ROM encoder, and a circuit used to create the DEC-modified MFM code. As each data bit is written on the diskette, the encoder ROM calculates a clock bit and checks for the 011110 pattern associated with the DEC-modified MFM. If the 011110 data pattern has not been detected, the data is alternately shifted out with the necessary clock pulses. This clock, data, clock pattern is selected by the 8:1 MUX at location K9. The MUX data/clock selection is controlled by the R/WC line P20.



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Figure 3-29. Write Serial Data Path

The DEC-modified MFM coding will only be used if the write operation is on a DEC double-density diskette, and the 011110 data pattern is detected. Only then will the MUX take the input from the DEC-modified MFM generation circuit. This circuit will force the DCD CDCDCDCD pattern from 00101010100 to 01000100010. This prevents marks from being detected in the double-density data fields. This same circuit is used in both single- and double-density write operations. The difference between the single- and double-density write operations is that during the single-density FM format, the clock is always forced to be a 1, and the MUX will not select the DEC-modified MFM data. The actual data/clock timing is determined by the R/WC PL CLK. Each R/WC instruction takes 333 nanoseconds. The clock data/cell is six R/WC instructions or 2 microseconds.

During a read operation, the serial data path is reconfigured to the circuit block diagram in Figure 3-30. Normally, the SPLL data input is shifted into the decoder ROM. The decoder PROM is the same ROM used for encoding write data. However, a separate output is used to separate the clock/data stream into a useful data stream. The decoded data is then fed through the selection MUX into the CRC generation chip and into the 8085 interface shift register, where it can be read by the 8085. After the read operation, the error output of the CRC generator is checked by the R/WC to verify the data.

Some other points should be discussed regarding the serial data path. One output of the precompensation circuitry is the PRE0 L line. This line is the data bit that just precedes the DD7 input of the encoder ROM during a write operation. PRE0 L, logically ANDed with DD7, is used to generate the clock pulse between DD7 and the data represented by PRE0.

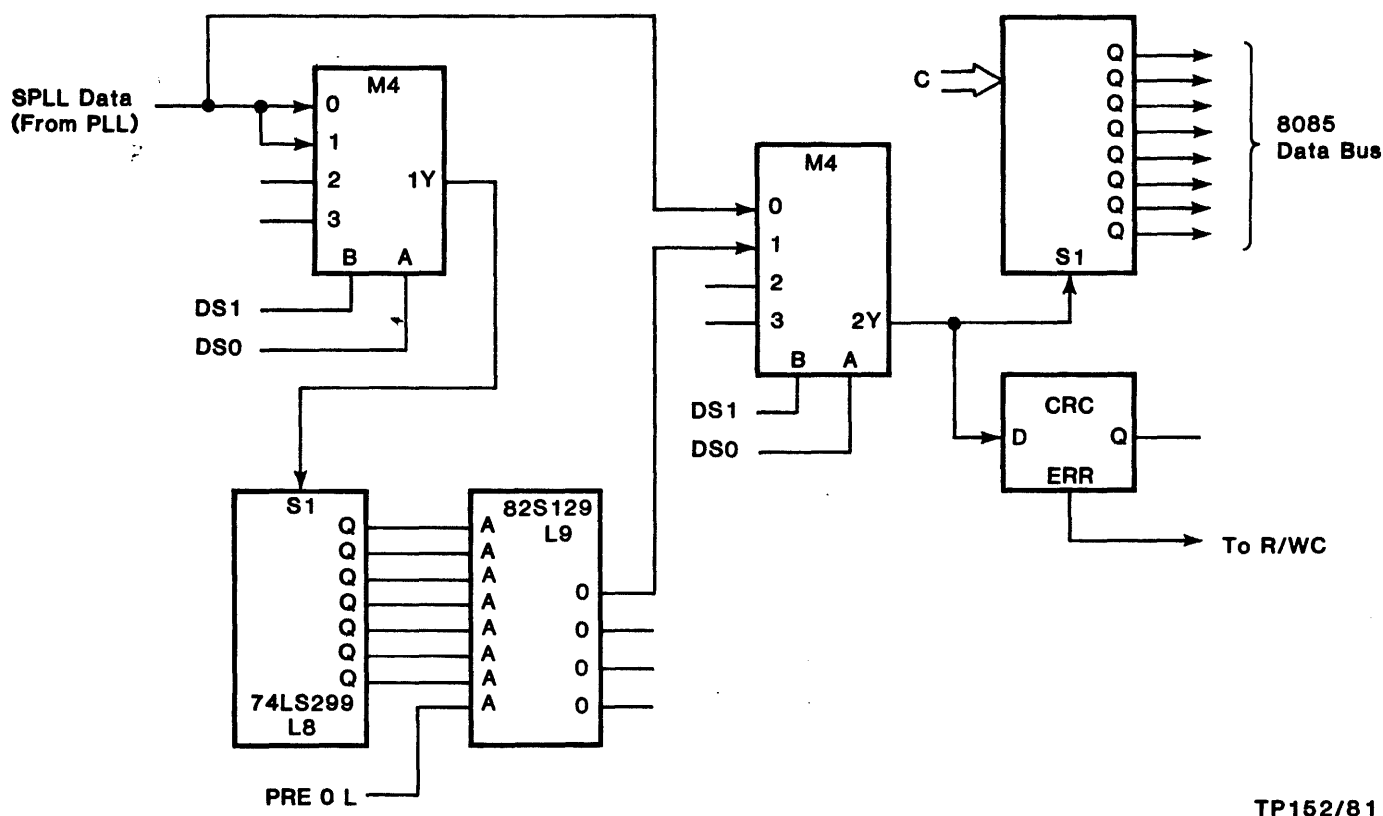


Figure 3-30. Read Serial Data Path

It is also possible for the R/WC to select the SPLL DATA to be shifted directly to the 8085 - R/WC shift register interface. This feature is used to read the various disk marks and allow the 8085, instead of the R/WC, to decide the mark. The same find mark routine is used in the R/WC for all the various disk marks.

Figure 3-31 shows the timing involved for substitution of the DEC-modified MFM code for the normal 011110 data patterns unless two distinct 011110 patterns are repeated. Thus, the pattern 011110011110 will result in two consecutive DEC-modified patterns, whereas the pattern 01111011110 will result in only one modified pattern.

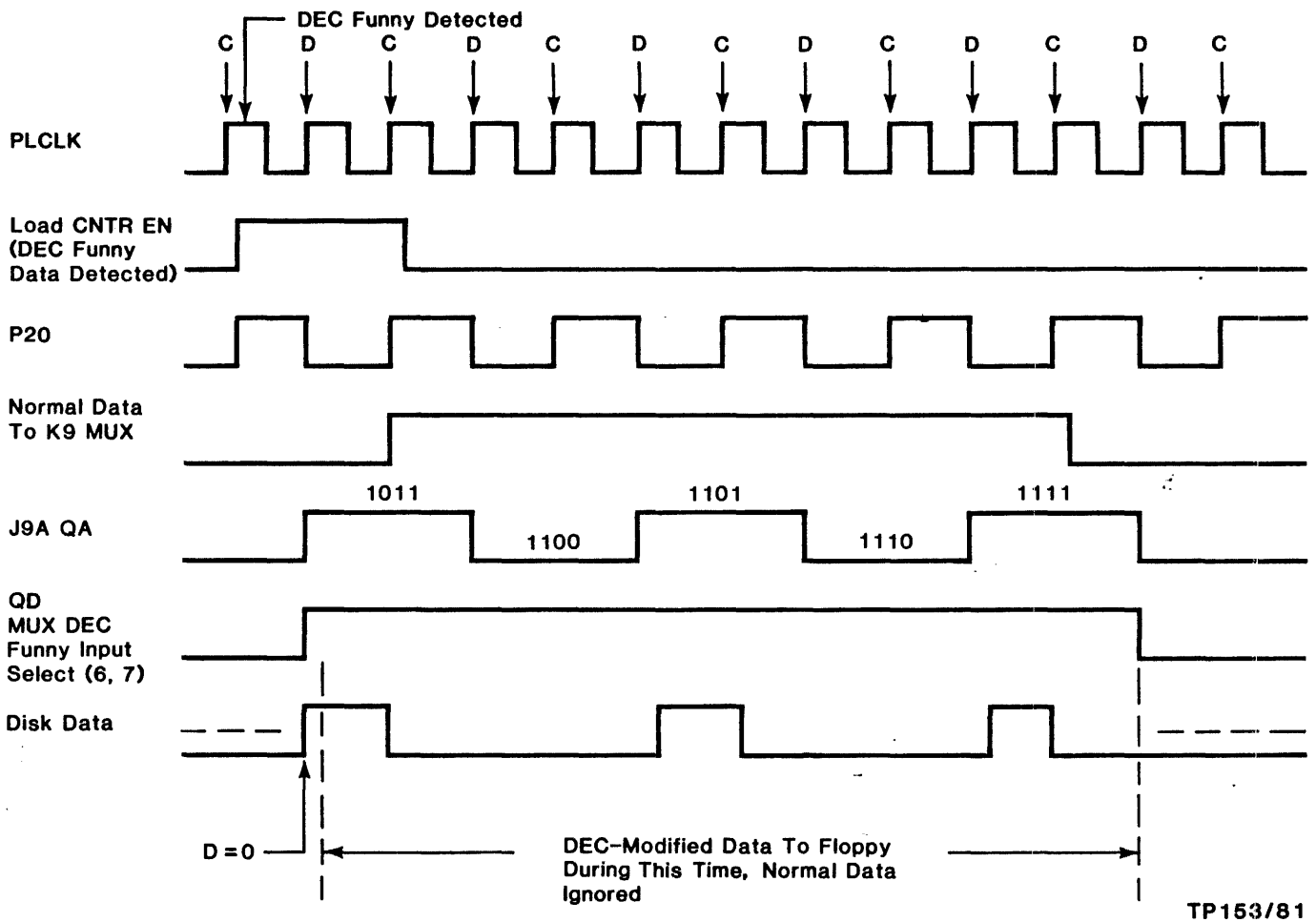


Figure 3-31. Generation of DEC-Modified Area Of MFM Coding

Write Precompensation Circuitry

Adjacent magnetic transitions will migrate away from each other, if they are of like polarity, and migrate toward each other, if they are of opposite polarity. The more that magnetic data drifts away from the exact position where it belongs on the magnetic media, the greater the chance the controller will misinterpret a data bit when trying to read the data stream back from the media. The write precompensation circuit decides, when writing a data or clock pulse, whether to write that particular pulse on time, slightly late, or slightly early, depending on the polarity of the pulses to be on either side of the one currently being written.

For example, if the pulse being written was to be a 1, and the pulses on both sides of the one being written were of the same polarity (i.e., both 0 or both 1), then the pulse being written would be written on time. Any distortion induced by the pulse on the left hand side, would be exactly compensated for by the pulse on the right hand side. If we do not have this type of pulse polarity symmetry, we would then write the middle pulse slightly late or slightly early. The net polarization, caused by the neighboring pulses, will be exactly compensated for when all of the pulses are placed on the media. The 440/480 controller only employs the precompensation circuitry while writing double-density data, using a special MFM data encoding algorithm. When data is being written in single-density format, using the conventional FM data encoding algorithm, the data is not packed tight enough to require the use of precompensation techniques. The following is a description of the precompensate circuits.

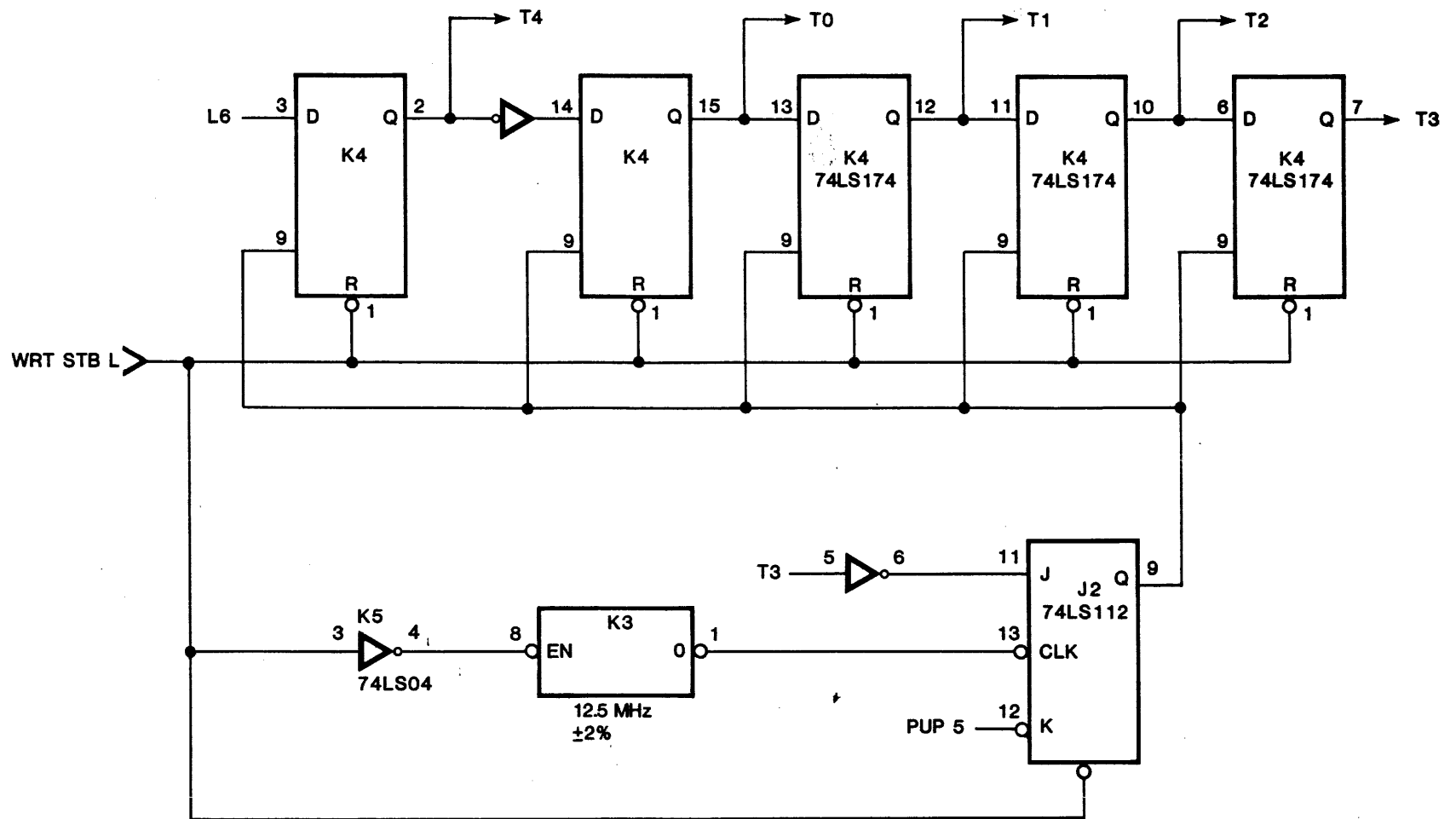
The precompensation network provides the necessary shift for the data going to the disk. See Figure 3-32. All write data is sent through this circuit. To determine if the data requires compensation, the registers of J3 are configured as a 5-bit shift register. Only the data bits are significant. The first, third, and last bits are considered by the MUX at J4; the clock bits are ignored. The 5-bit shift register will only shift when pre-enabled by P21 (WRITE STROBE ENABLE) and clocked by the R/WC write strobe. This insures synchronization between the compensation network and the data/clock stream.

The MUX at J4 controls the actual data to the disk. It is fed by three inputs, T0, T1, and T2. These inputs are derived from a state machine that produces these non-overlapped, clock pulses relative to the write strobe pulse. The timing of these pulses is shown in Figure 3-33. The MUX at J4 selects the appropriate T(x) pulse according to the following table. Note that data strobe to the disk is inhibited if the data/clock is a zero.

<u>Prior</u>	<u>Current</u>	<u>Following</u>	<u>Clock Used</u>	<u>Comments</u>
0	0	0	NONE (0)	No pulse
0	0	1	NONE (0)	No pulse
0	1	0	T1	On time
0	1	1	T2	Late pulses
1	0	0	NONE (0)	No pulse
1	0	1	NONE (0)	No pulse
1	1	0	T0	Early pulse
1	1	1	T1	On time pulse

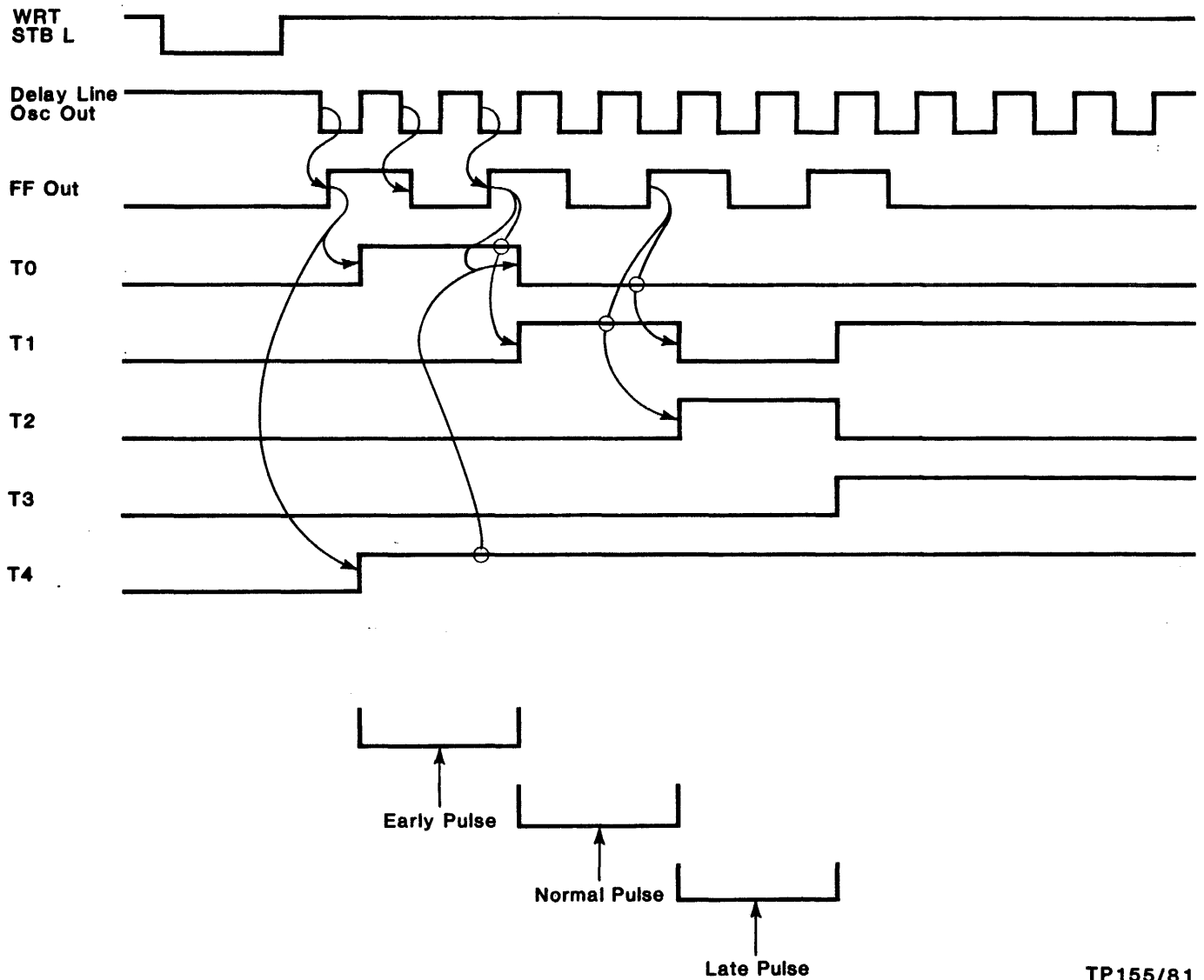
The current bit to be written is contained in bit 3 of the 5-bit shift register. This bit controls the output enable strobe of the MUX at J4. If the data bit is a zero, the strobe will be held high; no transition will be sent to the floppy drive. Also note that the data bit following the current bit is sent back to the ROM at location L9. This is the PRE0 L line on the schematic.

Compensation is enabled, or disabled, by the 8085 circuitry. Normally, only DEC double-density coding is precompensated. If IBM double-density or single-density is written, the 8085 will disable compensation.



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Figure 3-32. Write Precompensate Circuit



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Figure 3-33. Precompensate Timing

Coder-Decoder PROM: The Coder/Decoder PROM located at L9 is a 256 X 4 bipolar PROM. This PROM is used in the serial data path to eliminate the necessary logic required to detect DEC-modified MFM, generate the DEC modified MFM, and to supply the DD clock for normal MFM.

This PROM must have an access time of less than 55 nanoseconds to insure the outputs have settled before the next PL CLK occurs and changes the shift register.

The logic equations that relate the input lines to the output lines are shown in Table 3-9.

Table 3-9. Coder/Decoder PROM Logic Equations

OUTPUT 1

$$\text{Data Decode} = \overline{\text{DD3}} + \overline{\text{DD1}} \cdot \overline{\text{DD2}} + \overline{\text{DD4}} \cdot \overline{\text{DD5}} \\ (\text{Data}=1)$$

OUTPUT 2

$$\text{DEC-Modified Mark Required} = \overline{\text{DD2}} \cdot \text{DD3} \cdot \text{DD4} \cdot \text{DD5} \cdot \text{DD6} \cdot \overline{\text{DD7}}$$

OUTPUT 3

Not Used

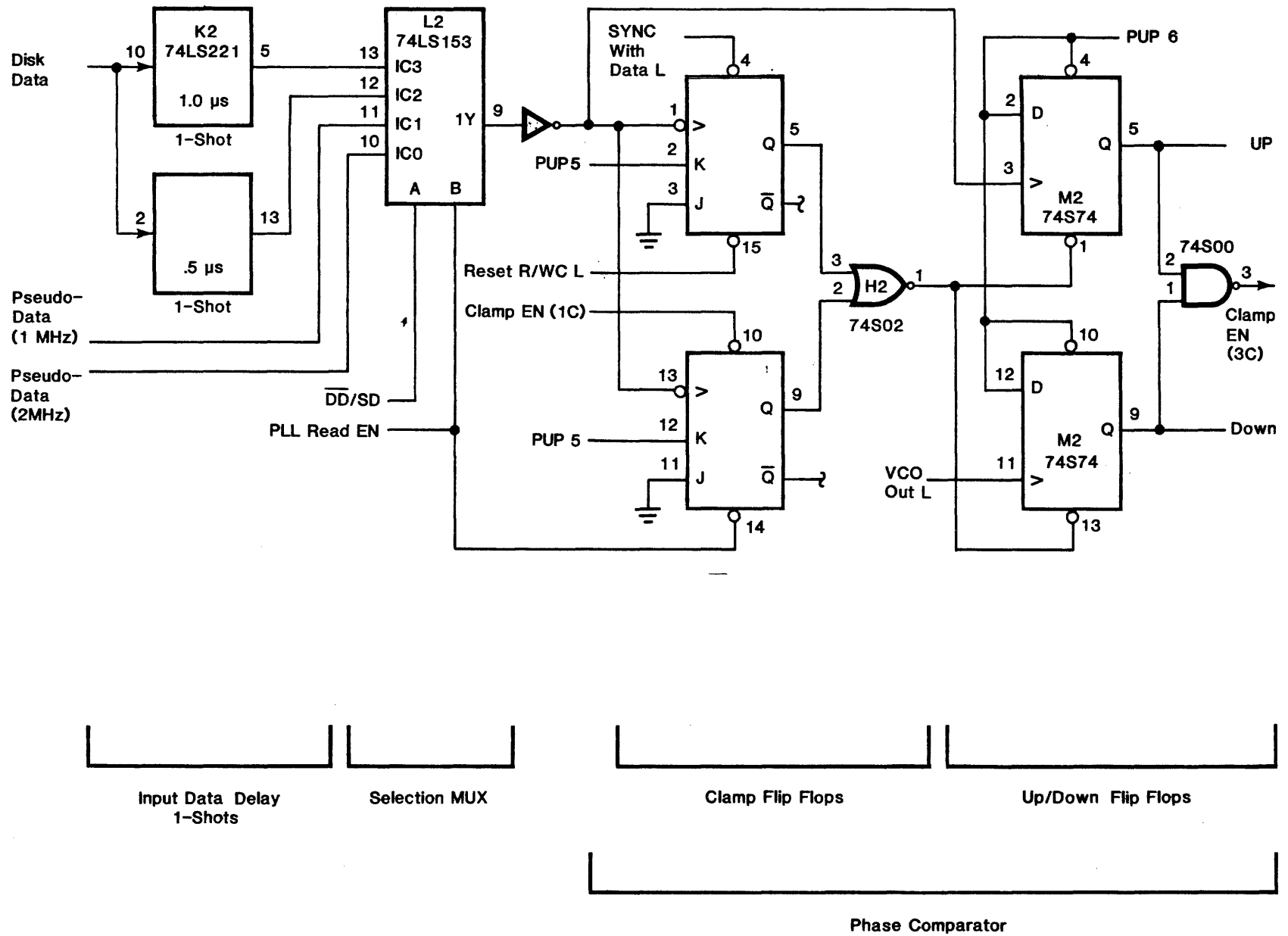
OUTPUT 4

$$\text{MFM Clock} = \text{PRE0 (L)} \cdot \overline{\text{DD7}} \\ (\text{Clock}=1)$$

3.7 Phase-Lock-Loop Circuitry

In order to construct a phase-locked-loop with the most stable possible characteristics, it is necessary to construct circuitry to augment the basic PLL. This circuitry is specific to the data pattern and timing that will be fed to the PLL. The DSD 440/480 PLL is designed to handle the IBM single- and double-density formats and the DEC double-density format. External circuitry to the PLL recognizes two bytes of preamble before the PLL is allowed to look at the incoming data from the diskette. During the time that the PLL is not connected to the diskette data, it is connected to pseudo-data generated from the 8085 clock and a counter. This provides the PLL with a signal that is nearly identical to the preamble signal from the diskette.

The incoming data from the diskette is fed to a pair of one-shots at IC location K2. These one-shots provide a 500 nanosecond or a 1000 nanosecond pulse that are selected for double- or single-density operation respectively. These one-shots are referred to as the data delay one-shots. The outputs of these one-shots are routed to a 4:1 MUX at IC location L2. The MUX provides the selection of either the single- or double-density pseudo-data, or single- or double-density real data from the floppy via the one-shots. The output of the data selection MUX is fed into the phase comparator. See Figure 3-34. The phase comparator is made up of four flip-flops. The first flip-flop is located at IC location J1. The SYNC FLIP-FLOP is controlled by the R/WC SYNC WITH DATA line. The SYNC flip-flop is set when the SYNC WITH DATA line is asserted low. This will clamp the UP and DOWN flip-flops, inhibit the VCO output, and load the VCO counter at IC location L1. The counter is loaded with a value that is one less than the normal eight count for double-density or 16 count for single-density. When the first data/clock bit occurs, the SYNC flip-flop is reset. This enables the VCO counter and the VCO output. The VCO output from the VCO at IC location P1 is delayed from going low for 1.4 cycles. Since the UP and DOWN flip-flops have been clamped, the VCO output is very close to the nominal preamble frequency. After a delay of 1.4 cycles, the VCO output starts clocking the VCO counter. Since it was loaded with one count less than normal, the output of the VCO counter will only be off by .4 VCO output cycles, which is 1/16 of the nominal double-density clock. This can be calculated to be a 2.5 percent basic phase error when the PLL is initially synchronized.



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Figure 3-34. Phase Comparator

The second flip-flop in the phase comparator is the clamp flip-flop. The clamp flip-flop is normally set when the initial synchronization is done, and whenever the UP and DOWN flip-flops are both set.

The last two flip-flops in the phase comparator circuit are the UP and DOWN flip-flops. The UP flip-flop is set whenever the data delay one-shot provides a pulse. The DOWN flip-flop is set whenever the VCO counter provides a pulse based on the VCO output. The outputs of these two flip-flops are fed, via transistor driver/isolators, to the VCO filter. The VCO filter is comprised of the operational amplifier and associated circuitry located at P1. When the UP flip-flop is asserted, the filter integrates, and the output to the VCO rises. When the DOWN flip-flop is asserted, the filter output voltage decays. The range of the VCO input voltage is determined by the duration of the UP and DOWN pulses and the circuit parameters.

The output of the active filter is fed into the VCO at location N1. The VCO output is fed into the synchronized VCO counter at IC location L1. The counter is normally connected to provide a divide by 8 or 16 output, based on the VCO output. The outputs of the VCO counter are fed to the input data selection MUX, various points in the PLL, and to the R/WC.

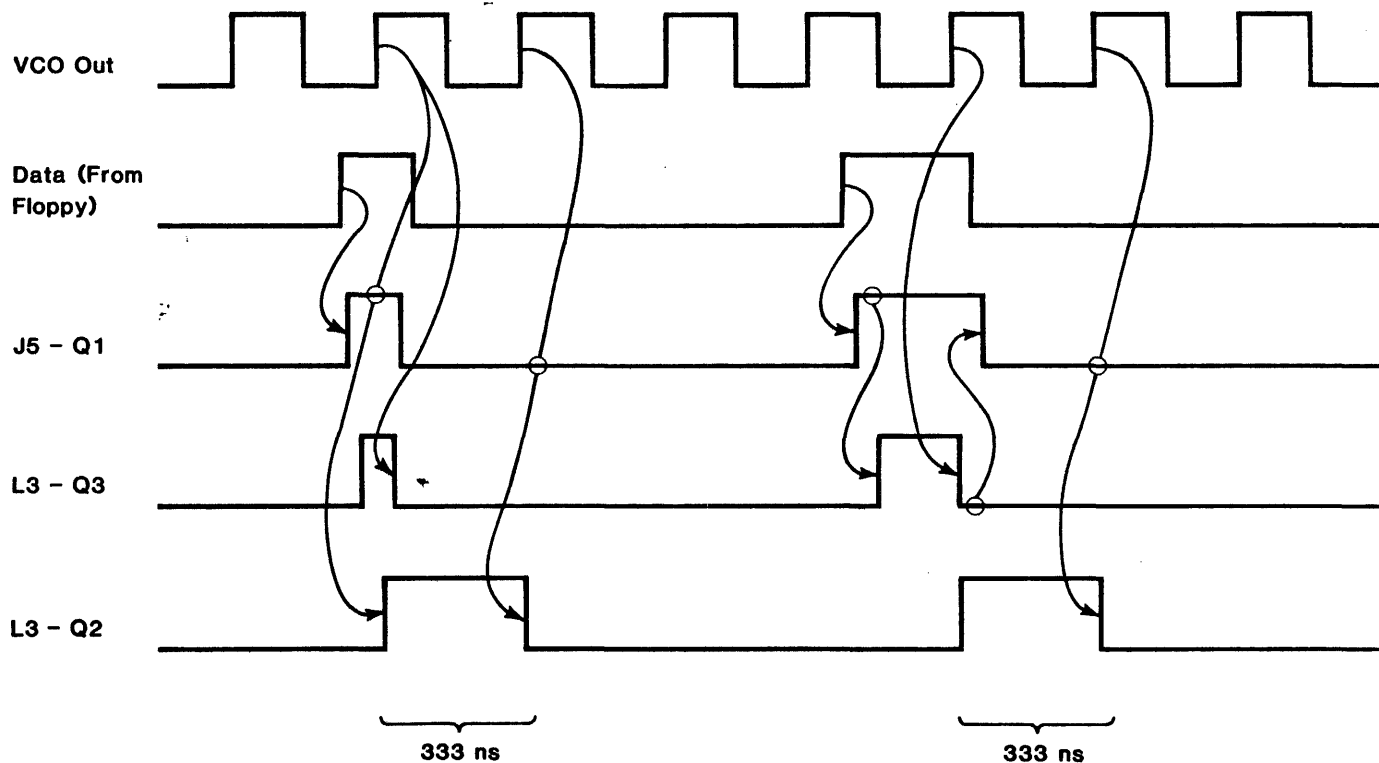
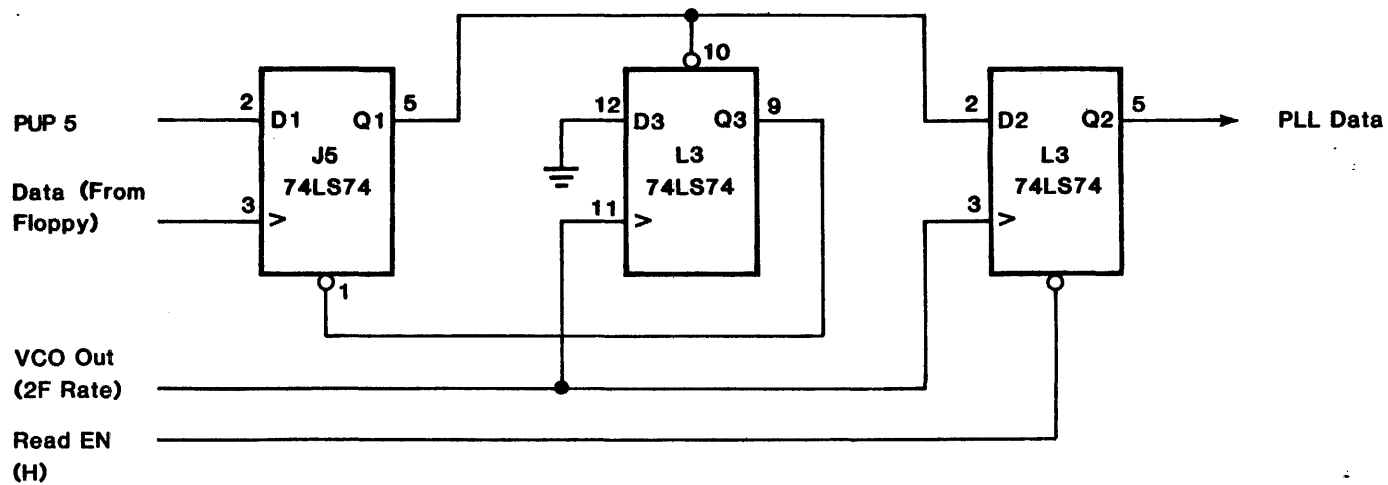
The rising edge of the VCO counter output is used as a boundary between bit cells. The falling edge, which occurs in the middle of a data bit cell, is used to clock the DOWN flip-flop. The output of the counter, as selected by the VCO SD/DD selection multiplexer, is compared with the incoming data.

The interface between the PLL and the read/write bit-slice controller consists of a set of three flip-flops. See Figure 3-35. Two of the flip-flops are connected to form an edge triggered set/reset flip-flop. These flip-flops provide an active high 333 nanosecond pulse for each data pulse that is detected. The output of this interface is fed to the R/WC.

The active filter and the VCO are provided with a filtered +5 volt power distribution system. The filter is comprised of several ferrite beads with a base inductance of approximately 10 microhenries, and a 1.0 microfarad capacitor. The 3 dB point of this filter is approximately 4.8 Kiloherz, and is sufficient to isolate the PLL from the rest of the controller board.

Critical Components: The pulse duration of the input one-shots must be set within +5%. To obtain this accuracy, there are adjustable resistors provided on the controller for both the 500 nanosecond and the 1000 nanosecond pulses. The range of adjustment is selected by the 100 pF (+10%) capacitor at locations C40 and C41. The adjustment pot for the 500 nanosecond pulse is located at R32. The adjustment for the 1000 nanosecond pulse is at R29. The components of the active filter are selected to approximate a second order system with a natural frequency of 60K radians/second and a damping constant of .4. These components are not particularly critical; 5 to 10% components are sufficient. The VCO base frequency should be accurate. Therefore, a 39 pF silver mica capacitor was selected for use.

Charge Pump Circuit: The charge pump circuit, shown in Figure 3-36, provides the +7 volts required by the CA3130 (location P1) in the PLL. The ferrite bead is required to suppress noise from the PLL getting into the charge pump circuit. The transistor (Q5) drives switches Q6 and Q7. C65 is the primary filter element, and is used as a storage device for the charge pump. C64 is the device that actually provides the boosted voltage through D3 into C65. The output can be tested using a DVM at test point 10.



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Figure 3-35. PLL Interface to Read/Write Controller

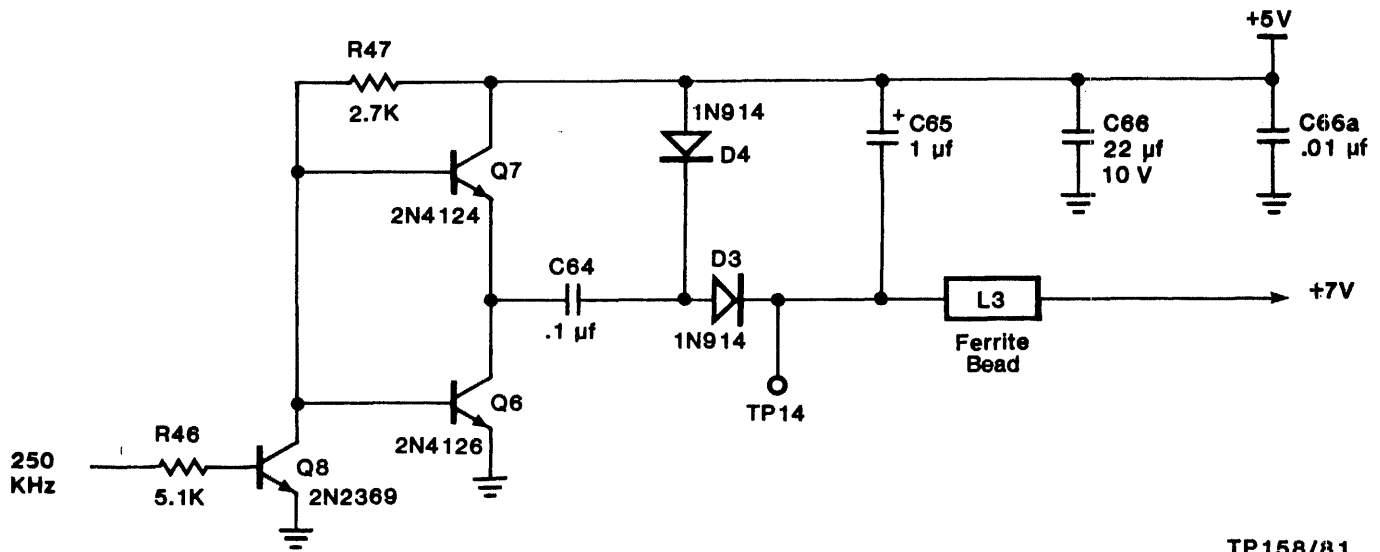


Figure 3-36. PLL Charge Pump Circuit

3.8 DC Power Sensing Circuit

This circuit generates the SYS RESET L signal, if +5 volt power is not within 25 millivolts of +5 volts. This signal resets the entire controller board, preventing either processor from executing microcode, and preventing the signals, WRT GATE, HEAD LOAD, and STEP from being asserted on the drive bus.

The 8211 takes voltage at pin 8, and using an internal regulator, creates a stable operating supply voltage for the internal circuitry whenever pin 8 is above approximately 2 volts. (See Intersil Specification.)

When the open collector 8211 is turned off, C1 starts charging through R2. When the voltage exceeds two diode drops, Q1 turns on and causes Q1 collector to go low. This turns Q2 off, and causes SYS RESET L to go high. Figures 3-37 and 3-38 show the circuit and timing for the power up/down circuit.

R3A (1 megohm) resistor provides positive feedback. It is intended to turn Q1 on faster, when Q2 first starts turning off.

R6 adds hysteresis to the circuit to stabilize it. This is needed, because when SYS RESET first negates, all the logic starts clocking away. This, typically, draws more current from the +5 supply, and causes it to drop slightly in voltage. R6 helps drive up the threshold voltage slightly when Q2 is off to prevent a motor boating effect.

R3 discharges the base-emitter capacitance voltage in Q1 when power goes low. This enables a rapid turn off of Q1. The 8211 output may go low right away, but current won't flow backwards through the diode, so R3 pulls current out of the base to turn Q1 off.

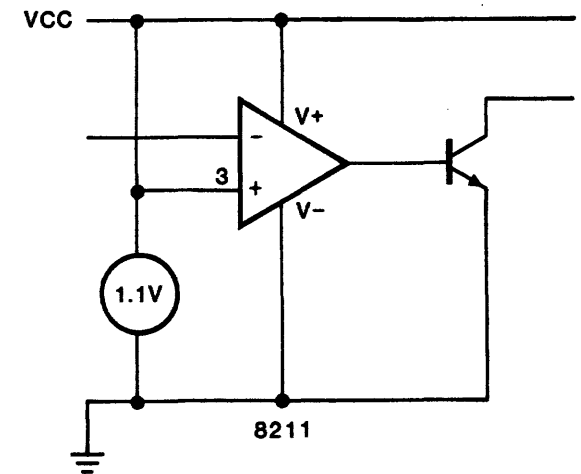
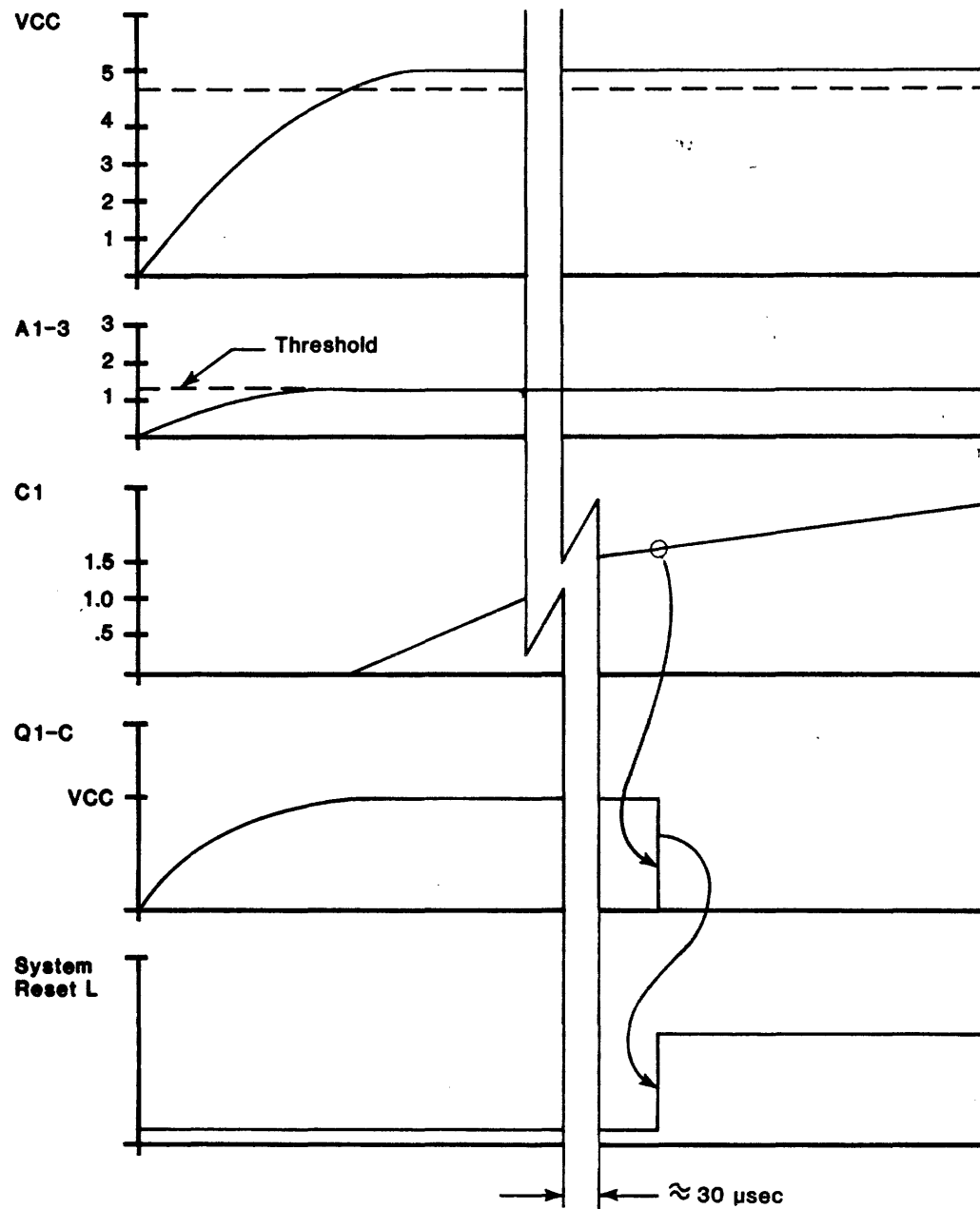
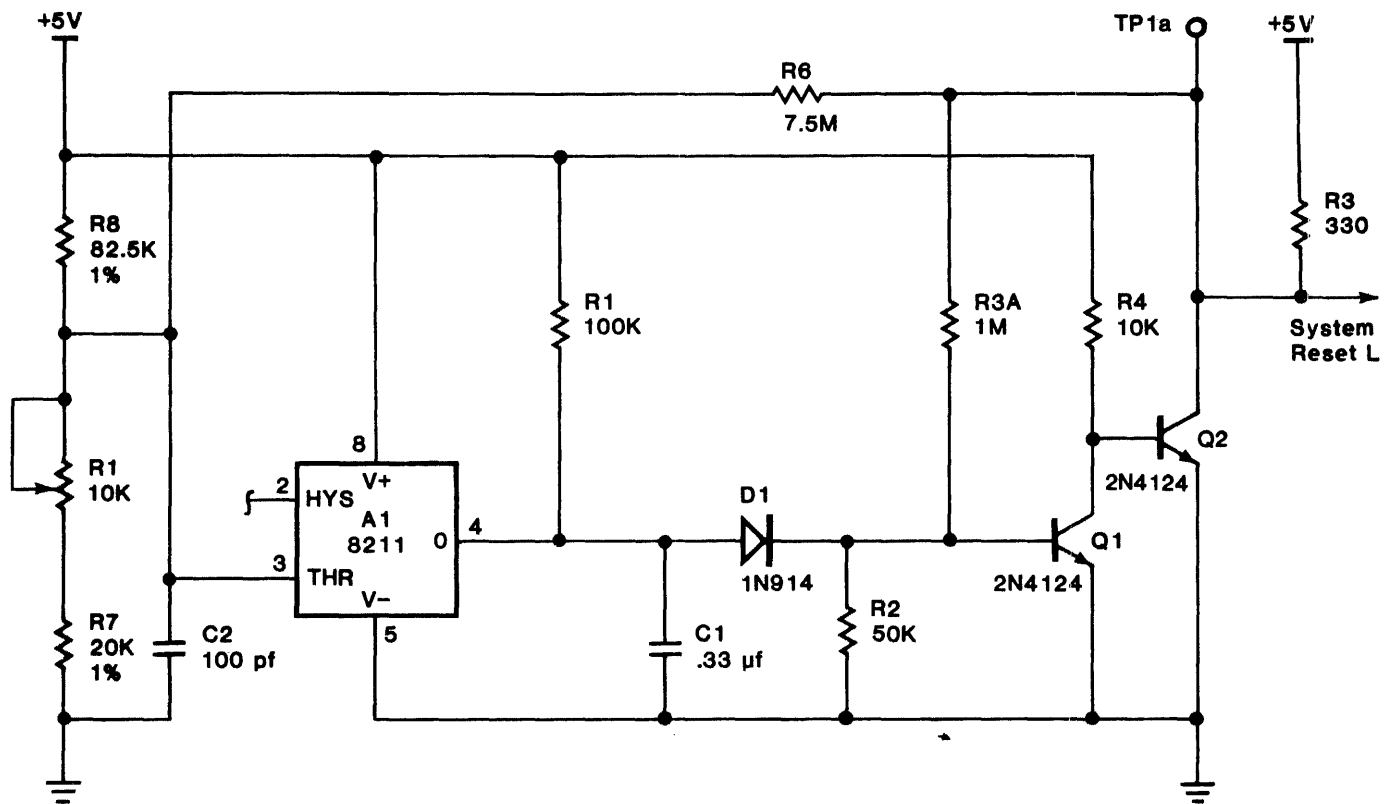


Figure 3-37. DC Power Up/Down Timing



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Figure 3-38. DC Power Up/Down Circuit

Reset Circuits: SYS RESET L, generated by the power sensing circuit, is applied to the 8085 master processor as RESET IN input, and disables WRT GATE, HEAD LOAD, and STEP outputs to the drive.

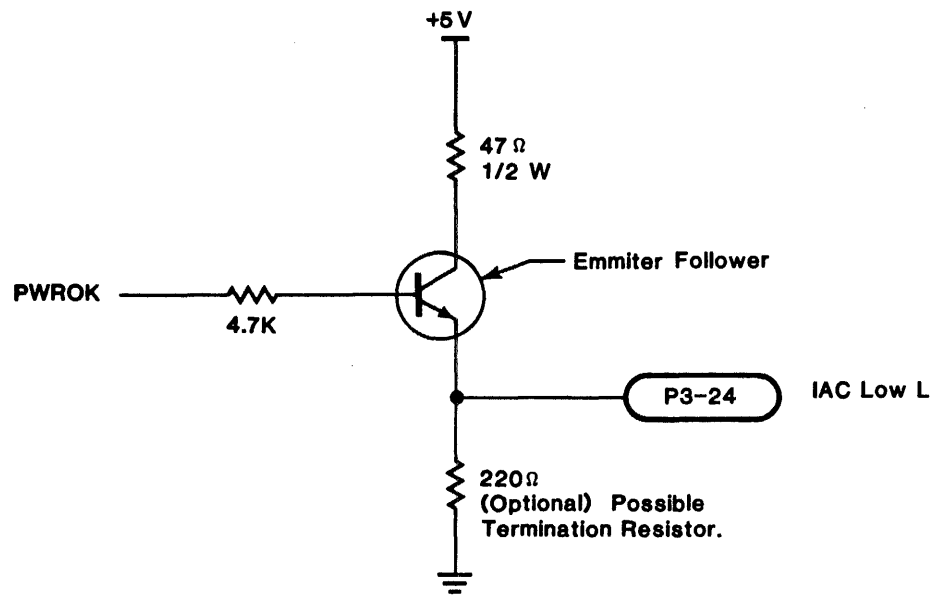
The circuit keeps SYS RESET asserted until the +5 volt power has been above +4.85 V (adjusted by trim pot) for roughly 30 microseconds. SYS RESET will be asserted as soon as the +5 volt power drops below the adjusted tolerance threshold (approximately +4.75 V).

NOTES: (regarding 8085 RESET IN line, to which SYS RESET L is connected.)

- RESET IN is latched every clock.
- If it is asserted, the microprocessor will assert RESET OUT at the beginning of the next state.
- To guarantee proper synchronization of the CPU, RESET IN should always be a minimum of 3 clock cycles wide (1 microsecond in this case).

IAC LOW L tells the host computer interface card whether dc power is present at the controller board. The I-Bus signal line driver circuit is shown in Figure 3-39.

NOTE: The 47 Ohm, current limiting resistor prevents the transistor from overheating if P3-24 accidentally is shorted to ground while PWROK is asserted.



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Figure 3-39. I-Bus Signal Line Driver Controller

4.0 MAINTENANCE

4.1 Introduction

This section contains servicing instructions and related information for field repair of subsystem modules of the DSD 440 and 480 Flexible Disk Systems.

The DSD 440 and 480 Systems are manufactured with field proven disk drives. The 440/480 Controller module is burned in under extreme conditions to insure trouble-free operation. Complete systems are thoroughly exercised and subjected to stringent quality assurance standards.

The service technician attempting field repair of subsystem modules must be thoroughly familiar with the contents of this manual, and those related publications listed in Section 1. In addition, the technician should be experienced in the maintenance of floppy disk drives, microprogrammed controllers, power supplies, and the repair of multi-layer printed circuit boards.

4.2 Preventive Maintenance

The DSD 440 and 480 Systems are designed to minimize the amount of periodic maintenance required. The prime factor in maintaining electronic equipment is ensuring it is operated within its design parameters and specified environmental limits. Cleanliness should be considered as part of the environmental requirement. During any routine or scheduled maintenance, the first step should always be a visual inspection. Check for corrosion, dirt, and undue wear on moving parts. Check all connector assemblies for proper and firm installation.

Cleaning of the SA850 drive heads used in the DSD 480 System is not recommended at this time. Contact a Customer Service Representative for further information. Addresses and phone numbers are provided in Section 1.

4.3 Servicing of Disk Drives and Power Supply

Packaged with the System User's Manuals are copies of Shugart Service Manuals for the SA800/801 single-sided drives, and the SA850/851 double-sided drives. These are used with the DSD 440 and DSD 480 Systems, respectively. For service instructions concerning the drives or the electronics associated with them, refer to the appropriate Shugart Manual.

The HyperDiagnostic routines of the DSD 440/480 controllers are a valuable aid in alignment of drives. Refer to System User's Manual for instructions in use of this capability.

Except for the dc output adjustments contained in paragraph 4.7, all servicing information and the schematic diagram for the power supply are contained in Appendix E of the Systems User's Manual.

4.4 Test Equipment

The following test equipment, or its equivalent, is recommended:

- Fluke, Model 8020A, Digital Voltmeter
- Fluke, Model 1900A, Frequency Counter
- Phillips, Model 3262, Oscilloscope (with delayed sweep)
- Paratronics, Model 532, Logic Analyzer, with:
Model 50, 16-Bit Analyzer Probe
Model 52, Probe Terminator
- Digital, Model W984A, Dual Wide Extender Board
- Digital, Model W987A, Quad Wide Extender Board

4.5 Test Points and Jumpers

The location of test points and jumpers for the DSD controller and interface modules are provided in the System User's Manual, and are not repeated here.

4.6 Other Test Points

Test points for measurement of dc output voltages of the power supply are located on the power distribution panel. These test points are shown in Figure 4-1, and described in Table 4-1.

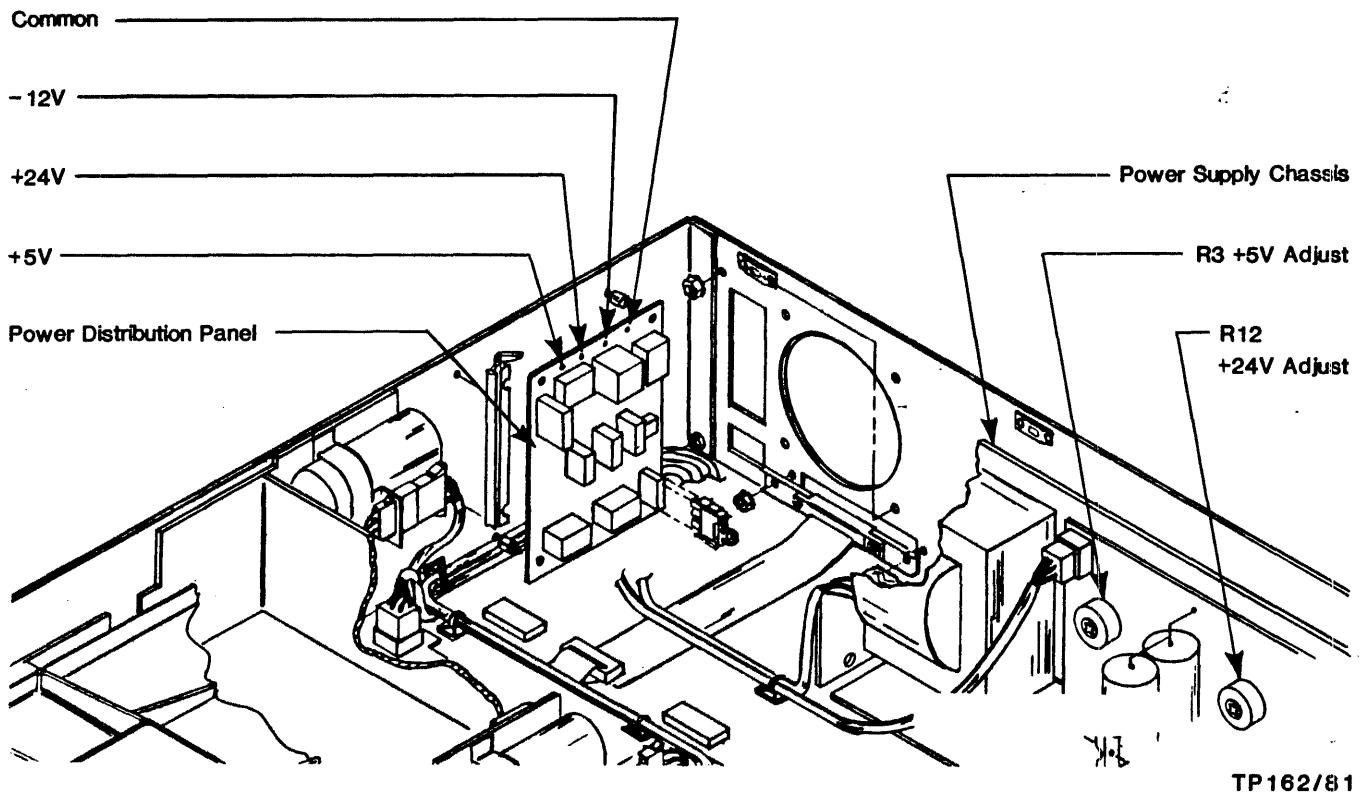


Figure 4-1. Other Test Point Locations

Table 4-1. Other Test Points

Value	Test Equipment	Adjust Pot	Measurement
AC Ripple	Scope	—	10 millivolt Peak to Peak Max
+5 volts	DC Voltmeter	R3	+5.05 V \pm 0.05 volts
+24 volts	DC Voltmeter	R12	+24 V \pm 0.5 volts
-12 volts Unreg.	DC Voltmeter	None	-9 to -16 volts

4.7 Adjustment Procedures

The following paragraphs provide instructions for the adjustment of the power supply output voltages, the PLL voltage control oscillator frequency, and the DCOK threshold voltage level. The latter two adjustments are made on the DSD 440/480 controller module. There are no adjustments to be made on the interface modules.

Power supply adjustment procedure:

WARNING

Voltage levels, that are dangerous to the technician, are present at the input terminals on the transformer mounted on the power supply chassis. Observe caution when making the following adjustments.

- (a) Remove the top cover of the unit.
- (b) Connect voltmeter to +24V and COM test points on the power distribution panel (see Figure 4-1.). Observe meter polarity.
- (c) Turn both the system and the voltmeter power to ON.
- (d) If required, adjust R12 for meter indication of +24V, \pm 0.5 volts.
- (e) Disconnect meter and reconnect to the +5V and COM test points; observe meter polarity (see Figure 4-1).
- (f) If required, adjust R3 on the power supply chassis until the meter indicates +5.05 V dc \pm 0.05 volts.
- (g) Disconnect the meter leads and reinstall the top cover.

This completes the adjustment of the power supply voltages. There is no adjustment for the -12V supply.

PLL Circuit VCO adjustment procedure:

(The adjustment pots, R29 and R32, are set at the factory and sealed with glyptol during final test. Adjustment in the field is normally not required.)

Figure 4-2 shows the location of referenced test points and jumpers for this adjustment procedure.

- (a) Remove the top cover and apply power to the unit.
- (b) Refer to Figure 4-2 and move the Berg jumper on J29A from normal position to test position
- (c) With oscilloscope, observe pulse at test point 8, located just to the right of R29. (See Figure 4-2.)
- (d) If necessary, adjust R32 for a 500 nanosecond pulse width at TP8.
- (e) Move oscilloscope connection to TP9.
- (f) If necessary, adjust R29 for a 1 microsecond pulse width at TP9
- (g) Disconnect oscilloscope. Reseal both trim pots with glyptol, and replace Berg jumper to normal position.
- (h) Replace top cover.

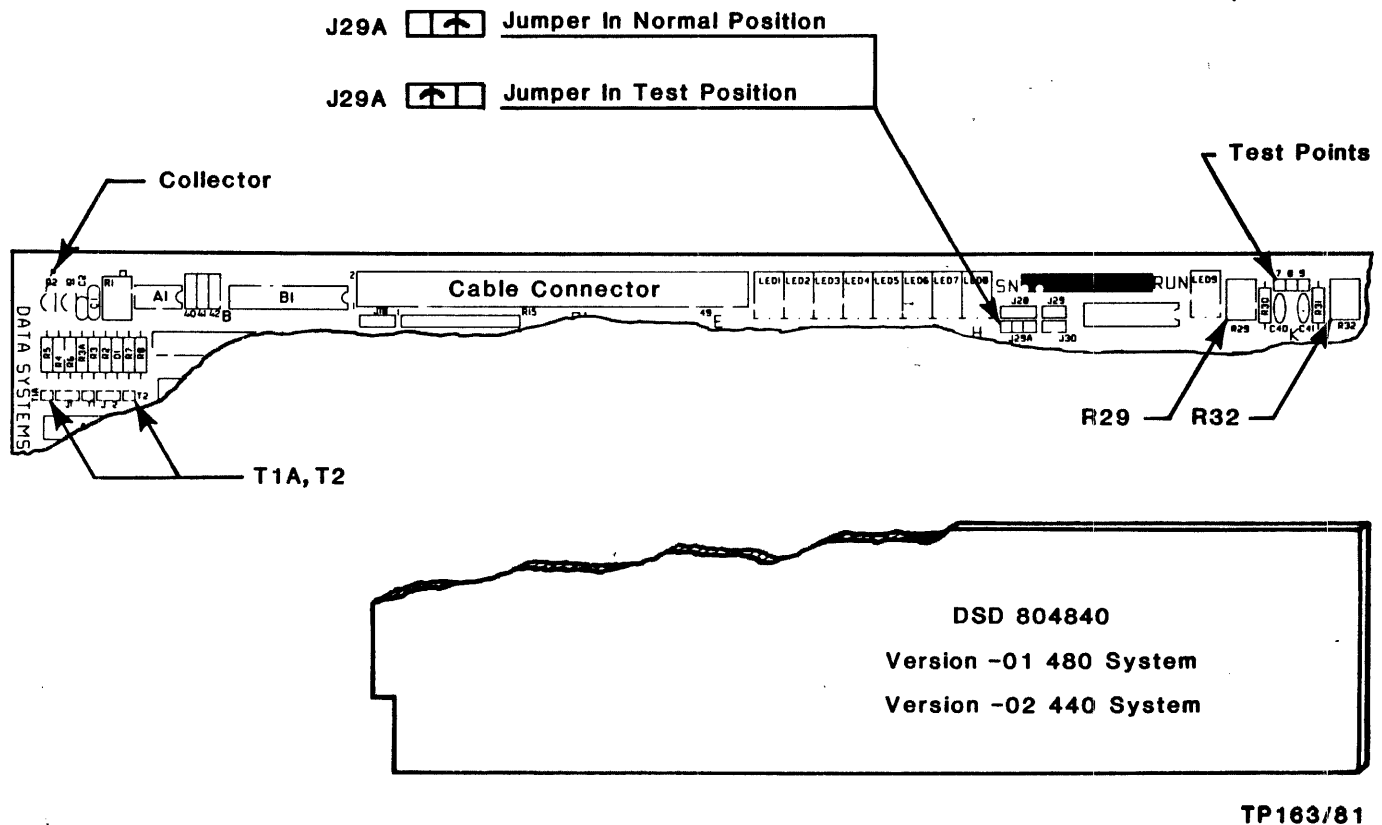


Figure 4-2. Controller Board Test Points and Jumpers

Setting threshold voltage on dc power sensing circuit:

The factory setting for this circuit is: the circuit will disable controller operation at a level of +4.75 volts, and restore controller operation when the voltage rises above +4.85 volts. Figure 4-2 shows the location of Q2, T1A, and R in the upper left hand corner of the module. Note that T1A and the collector of Q2 are at the same dc potential.

- (a) Remove top cover and apply power to the unit.
- (b) Connect oscilloscope and/or dc voltmeter to T1A (collector of Q2). Dipswitches 1, 2, and 3 (at board location C2) should be in closed position.
- (c) If necessary, adjust the trim pot R1 so that the voltage at T1A switches from low to high at +4.85 volts (going high). (This allows for 100 millivots of hysteresis in the circuit.)
- (d) Readjust power supply. See step 4.7 (e).
- (e) Remove the test equipment. Reseal the trim pot, and replace the top cover.

4.8 Removal and Replacement Procedures

With the exception of components on the controller and interface modules, removal and replacement of major assemblies and repair of these is straight forward. Extreme care must be exercised in removal and replacement of components on the multi-layered printed circuit boards. Careless or sloppy de-soldering and re-soldering techniques can cause numerous problems, and may render the boards beyond economical repair. (See Paragraph 1.5, Servicing Limitations.)

NOTE

A cardboard shipping disk was inserted into the drives of double-sided disk drives prior to shipment from the factory. These cardboard disks should be retained and used to prevent damage to the heads during handling or shipping.

4.9 Troubleshooting Techniques

When a system's reliability is in question, several methods exist to evaluate the possible problem(s). The first level of troubleshooting is observation of the DSD 440/480 Normal Operation Mode Self-Test. These self-tests are performed each time power is applied to the controller, and each time an initialization is activated. If an error occurs during these tests, the controller board will halt. The error detected will be displayed in the LEDs. Refer to the Controller LED Decoding Chart in the Systems User's Manuals for a description of the LEDs and their meaning.

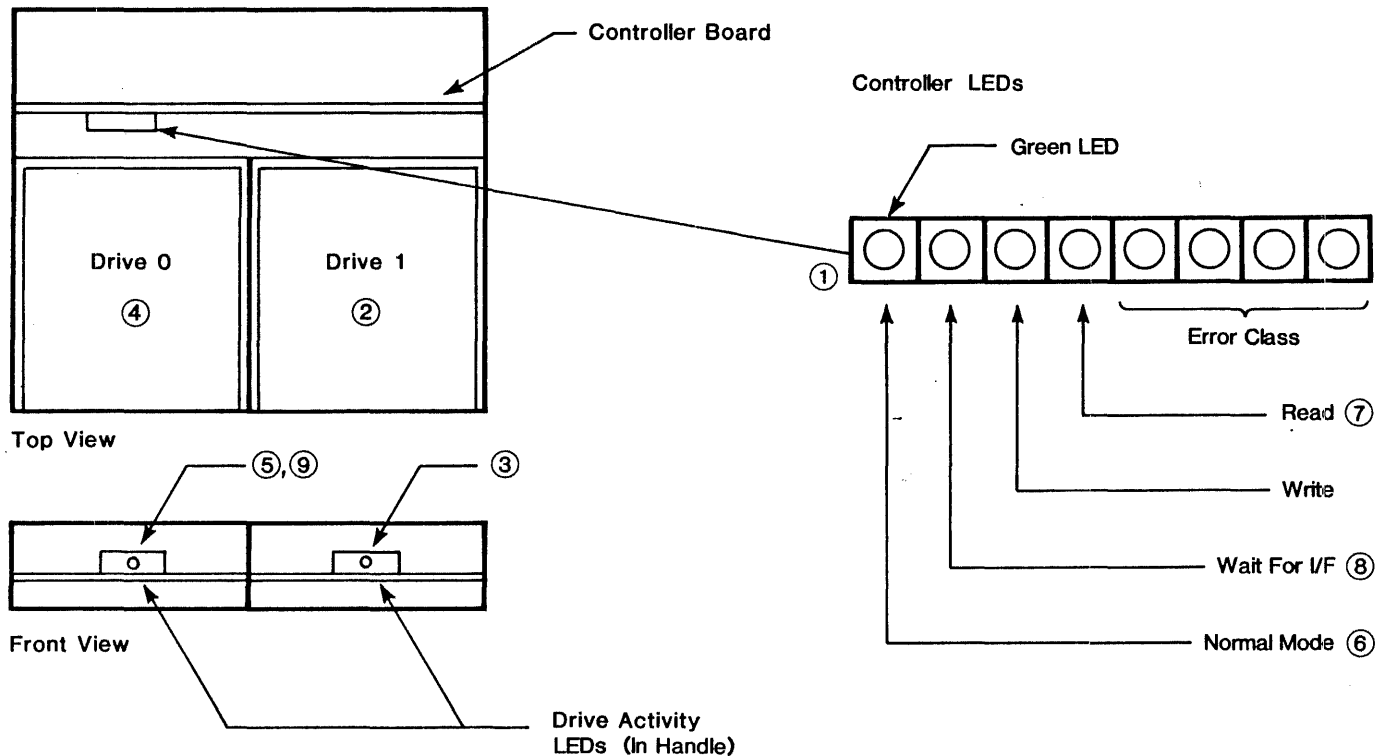
The second troubleshooting method is the use of the FLPEXR or FRD 440 test program. FLPEXR and FRD 440 are described in the User's Manuals. A further interpretation of the error codes is found in Appendix I of the DSD 440 manual, and Appendix H of the DSD 480 manual. The program provides extensive testing and error data collection facilities. It is the best method to use for evaluation of intermittent malfunctions.

The third method is the use of the HyperDiagnostic programs for your system. The HyperDiagnostic tests are self-contained on the controller module and provide extensive test capability when a host computer is unavailable, or when the system will not boot. These tests do not test the interface module, but several drive tests are available. Refer to your System User's Manual for further information on the use of HyperDiagnostics.

There is another troubleshooting tool, the Extended Self Test program. This program's use and interpretation are fully described in the instructions accompanying the kit, and are not repeated in this manual.

NOTE

The circled numbers in Figure 4-3 refer to notes indicated on the flow chart that follows.



TP164/81

Figure 4-3. Reference Notes

4.10 Normal Initialization Sequence

The following two flow charts, Figures 4-4 and 4-5, show the normal initialization sequence in detail. The following assumptions have been made in presenting these:

- 2 drives
- Diskette in drive 0
- Doors closed
- Cover off
- Power applied
- I-Bus connected to live CPU
- Everything healthy
- Normal mode

4.11 Troubleshooting a Failure During Bootstrap

The following information provides an analysis of possible causes and corrective action to be taken if a disk fails to boot in an LSI-11 or PDP-11 system.

- (a) If you have looked at the registers, tried to restart the system, cycled power, or tried to initialize the system since the halt or hang; try to reboot. Any of the actions mentioned may cause the error register on the floppy to be modified. If this happens, the error codes cannot be recovered and troubleshooting cannot be continued; try to reboot the disk.
- (b) If the system is now halted, or has been halted because of a loop, record the address displayed on the terminal (on LSI-11), or record the address displayed in LEDs (on PDP-11).
- (c) Go to Paragraph 4.12, How to Obtain Definitive Error Status, and get the definitive error returned in R4. Insure that you use the correct program for either an RX01 or RX02 system.
- (d) Record the contents of R4 with the halt address previously obtained in step (b) above.
- (e) Try to localize the trouble using the information in Tables 4-2 and 4-3 that follow this procedure, and the definitive error codes found in Appendix I of the DSD 440 User's Manual, and/or Appendix H of the DSD 480 User's Manual.

NOTE

The bootstrap is contained in Track 1, Sector 1, of any bootable disk furnished with the system. Word 0 of the bootstrap data should always be 240.

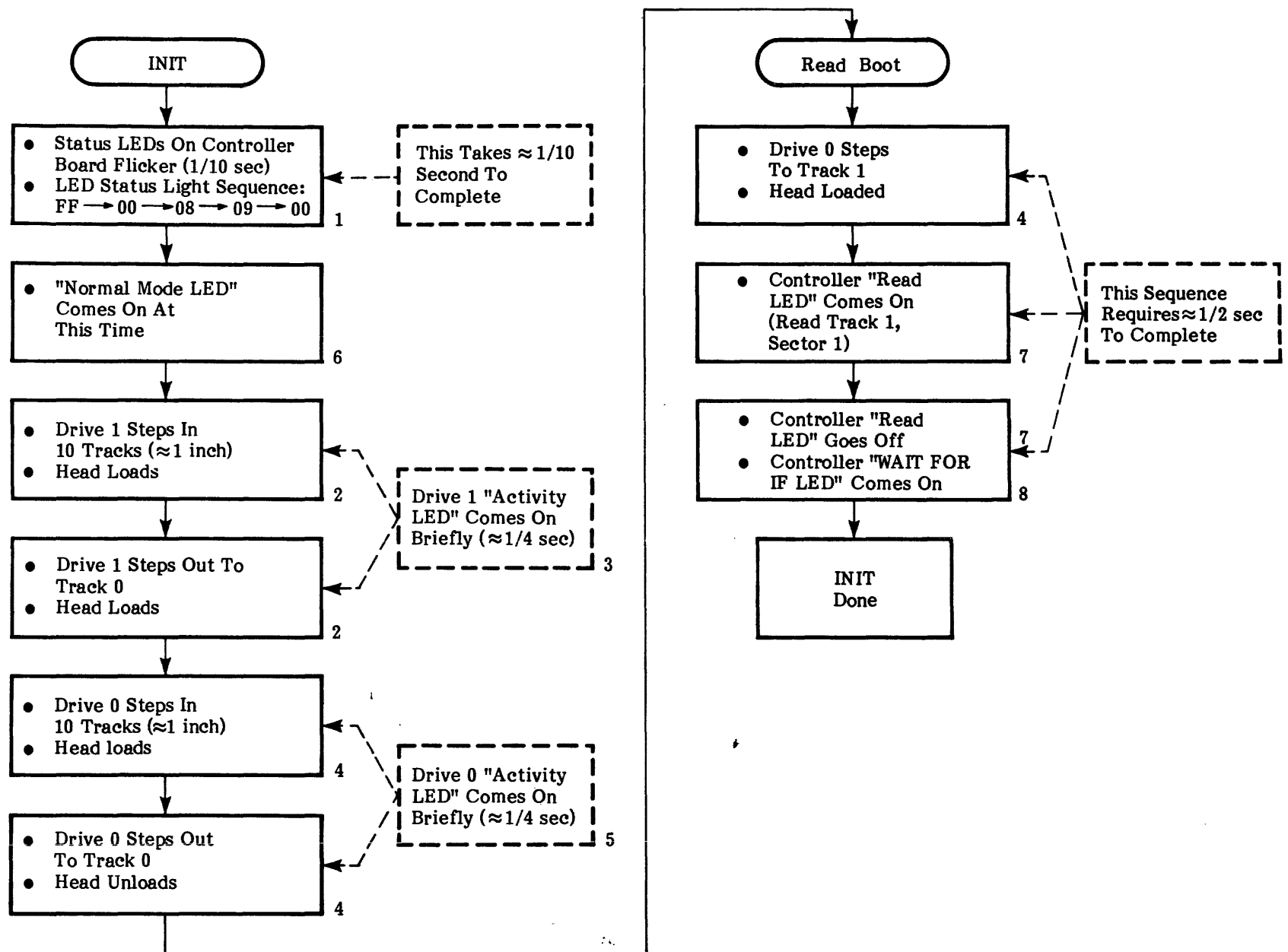


Figure 4-4. INIT Sequence

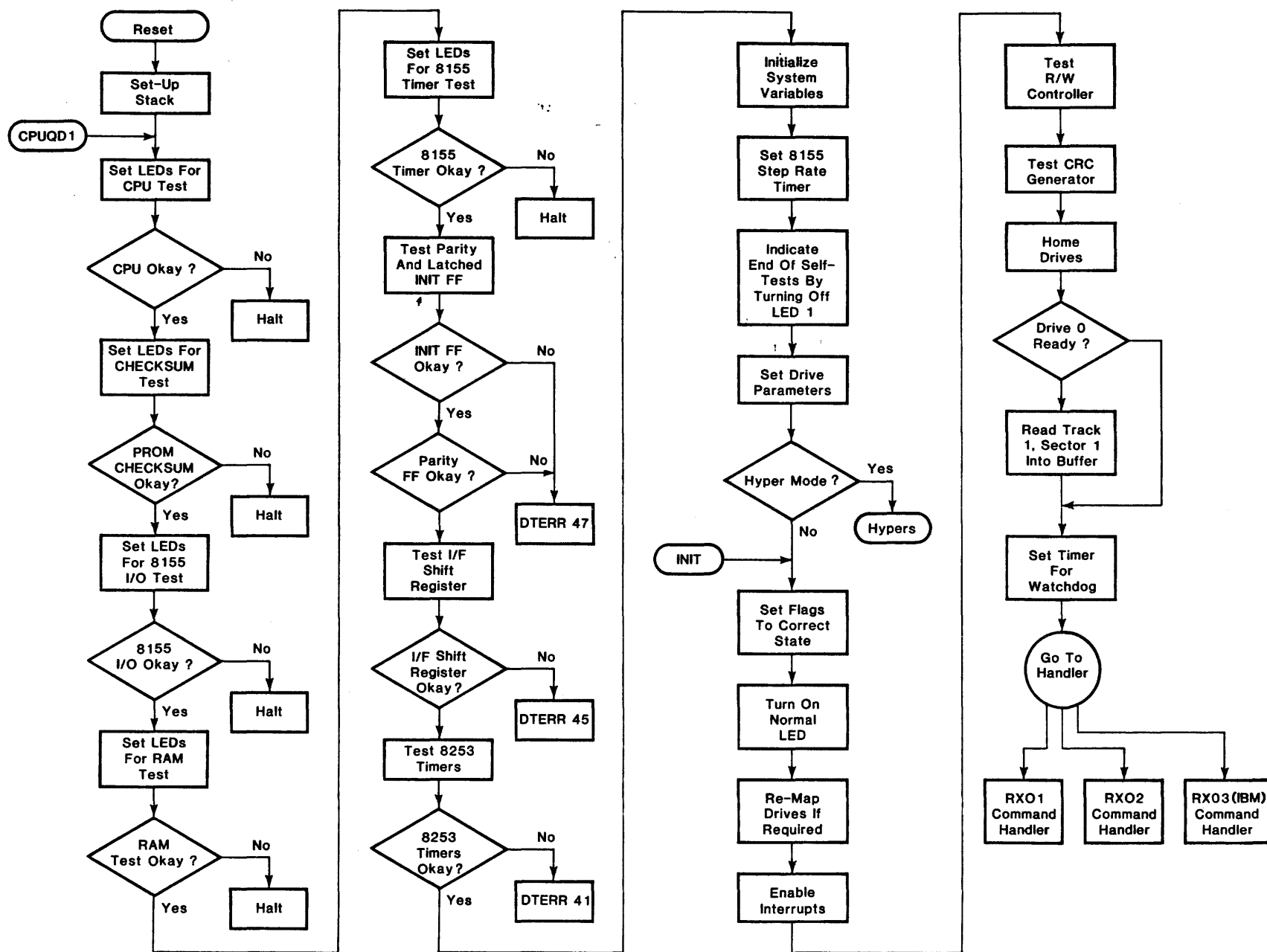


Figure 4-5. INIT Sequence in Microcode

Table 4-2. Bootstrap Halt Errors

XXX002	Error:	<ul style="list-style-type: none"> ● Bootstrap does not respond.
	Possible cause:	<ul style="list-style-type: none"> ● Bootstrap disable on interface. ● Bootstrap start address is not set correctly. ● Interface not installed into backplane. ● Computer malfunction. ● Interface malfunction. ● Address range of memory board extends into bootstrap area. ● Address conflict with other board in computer.
	Troubleshooting:	<ul style="list-style-type: none"> ● Check setup on interface jumpers, boot address range, and computer memory. ● Insure interface correctly installed into backplane. ● Verify computer can access 173000 without error. ● Verify boot enabled. ● Make sure another device does not respond at boot address when interface is removed.
XXX156 XXX204	Error:	<ul style="list-style-type: none"> ● Memory error at location contained in register R4. ● R0 has data expected.
	Possible cause:	<ul style="list-style-type: none"> ● Bad memory or CPU. ● No refresh on dynamic RAM.
	Troubleshooting:	<ul style="list-style-type: none"> ● Run DEC memory diagnostics to verify error. ● Check if memory location can be accessed. ● Check if refresh is okay. Write 125252_g in location and wait two minutes. Verify contents are unchanged.
XXX252	Error:	<ul style="list-style-type: none"> ● Memory error (if REG #5 = Boot Base Address +112_g, stack pointer (R6) = 5002). ● Fill empty error (if REG #5 = Boot Base Address +522_g, stack pointer (R6) = 5000).
	Possible cause:	<ul style="list-style-type: none"> ● Interface and controller are not in same mode. ● INHIBIT INCR ADR jumper on interface is installed. ● In RX02 mode, KD11-F is being used to refresh external RAM from CPU.
	Troubleshooting:	<ul style="list-style-type: none"> ● Replace interface. ● Run memory tests. ● If using KD11-F, refresh memory using REV-11 or on board memory refresh. ● Remove INCR ADR INHIBIT jumper on interface, if installed. ● Put interface and controller in same mode (RX01 or RX02).

Table 4-2. Bootstrap Halt Errors (Cont)

XXX324	Error:	<ul style="list-style-type: none"> ● Error flag set in RXCS after a system INIT (RXES=010).
	Possible cause:	<ul style="list-style-type: none"> ● Interface cable disconnect. ● Interface cable is backward. ● DSD 440 chassis power is off. ● Controller error or system error detected by controller. ● Drive not ready (pulley).
	Troubleshooting:	<ul style="list-style-type: none"> ● INIT DSD 440 System using front panel, or by writing 40000₈ into RXCS. If Error Flag is still on, check: <ol style="list-style-type: none"> 1. Interface cable connection. 2. AC power to DSD 440. 3. Error shown on 440 controller's LEDs. ● See if correct pulley is installed on drive 0 and drive 1 (for frequency being used). ● Try swapping logical drives by changing controller switch 5, then reboot. If drive boots okay, physical drive 0 is bad. <p>NOTE: If drive 1 is bad, but you're booting on drive 0, it should still boot okay.</p>
XXX342	Error:	<ul style="list-style-type: none"> ● RXCS has latched bit error (expects 5460)
	Possible cause:	<ul style="list-style-type: none"> ● RXCS register error (interface bad).
	Troubleshooting:	<ul style="list-style-type: none"> ● Service interface PCB assembly.
XXX364	Error:	<ul style="list-style-type: none"> ● RXDB latched bit error.
	Possible cause:	<ul style="list-style-type: none"> ● RXDB bad (interface bad).
	Troubleshooting:	<ul style="list-style-type: none"> ● Service interface PCB assembly.
XXX774	Error:	<ul style="list-style-type: none"> ● Floppy read error.
	Possible cause:	<ul style="list-style-type: none"> ● No disk in drive being booted. ● Door open on drive to be booted. ● Disk inserted incorrectly. ● Bad disk in drive to be booted. ● Incorrect pulley for frequency being used. <p>NOTE: Typing P on LSI-11, or Control Cont on PDP-11 will result in next drive being used to boot.</p>
	Troubleshooting:	<ul style="list-style-type: none"> ● Swapping drives. ● Insuring bootable disk in drive 0. ● Inserting disk correctly.

Table 4-3. Bootstrap Loop Errors

XXX314	Error:	<ul style="list-style-type: none"> ● Device is not responding where boot expects.
	Possible cause:	<ul style="list-style-type: none"> ● Board not correctly jumpered for desired ADDR. ● Bootstrap not started at correct address for device selected. ● I/F cable loose or disconnected. ● Interface not working correctly.
	Troubleshooting:	<ul style="list-style-type: none"> ● See if device will respond to where address is set. ● Insure address jumpering is correct. ● Check I/F cable connection at both ends. ● Repair interface and/or computer, if necessary.
XXX400-402 XXX414-416 XXX452-454	Error:	<ul style="list-style-type: none"> ● Transfer request error during a fill empty routine.
	Possible cause:	<ul style="list-style-type: none"> ● Bad interface or controller.
	Troubleshooting:	<ul style="list-style-type: none"> ● Service interface PCB and/or controller
XXX576-600 XXX604-606 XXX652-654 XXX666-670	Error:	<ul style="list-style-type: none"> ● Transfer request error during the actual bootstrap operation.
	Possible cause:	<ul style="list-style-type: none"> ● Bad interface or controller.
	Troubleshooting:	<ul style="list-style-type: none"> ● Service interface PCB and/or controller.
XXX742-746	Error:	<ul style="list-style-type: none"> ● Wait routine hangup (for Done, Transfer Request, or Error flags).
	Possible cause:	<ul style="list-style-type: none"> ● DMA jumper removed on interface during RX02 mode boot. ● If LED 4 on controller is on before Halt, may be blank disk (formatted, but no boot).
	Troubleshooting:	<ul style="list-style-type: none"> ● Known good, bootable disk. ● Insure DMA jumper installed on interface.

4.12 How to Obtain Definitive Error Status

The two following procedures outline the steps to be taken to obtain the definitive error status from the register. Use the appropriate program for the RX01 and RX02 as applicable to your system.

RX02

When you are using ODT, the definitive error status may be obtained in RX02 mode by following these steps:

- 1) Do not initialize the system (the RXs and error status will be lost).
- 2) Enter the program given below starting at location 002000.
- 3) Enter the number 002000 into the program counter, R7.
(R7/XXXXXX 002000 CR)
- 4) Type P (proceed in ODT), or press CONTROL CONT on a PDP-11.
- 5) The program will halt pointing at location 0002036. The status may then be obtained as follows:
 - A) R3=RX2s(177172) at time of error.
 - B) R4=Definitive error code.
 - C) The definitive error status information may be obtained starting at location 0. This information is explained in the User's Manual.

RXCS=177170
RXDB=177172

<u>Mem Addr</u>	<u>Enter This</u>				
2000	012700	START:	MOV	#RXDB, R0	; R0=RXDB
2002	177172				
2004	010001		MOV	R0,R1	; R1=RXDB
2006	011003		MOV	(R0),R3	; R3=RXES before DEF ERR
2010	012741		MOV	#17, -(R1)	; R1=RXCS, command=#17
2012	000017				
2014	105711	1\$:	TSTB	(R1)	; Wait for TRREQ
2016	100376		BPL	1\$	
2020	005010		CLR	(r0)	; Error buffer at LOC 0
2022	132711	2\$:	BITB	#40, (R1)	; Wait for Done
2024	000040				
2026	001776		BEQ	2\$	
2030	013704		MOV	@ #0,R4	; Move DEF ERR to R4
2032	000000				
2034	000000		HALT		; Done
			, END START.		

RX01

While in RX01 mode, the definitive error code may be recovered by following these steps:

NOTE

Do not initialize system, or floppy, as this will destroy error code in RXES.

- 1) Enter the following program:

<u>Mem Addr</u>	<u>Enter This</u>				
2000	012700	START:	MOV	#RXDB, R0	; R0=RXDB
2002	177172				
2004	010001		MOV	R0, R1	; R1=RXDB
2006	011003		MOV	(R0), R3	; R3=RXES before DEF ERR
2010	012741		MOV	#17, -(R1)	; R1=RXCS,
2012	000017				; COMMAND=#17
2014	132711	1\$:	BIT	#40, (R1)	; Wait on DONE
2016	000040				
2020	001776		BEQ	1\$	
2022	011004		MOV	(R0), R4	; MOV DEF ERR to R4
2024	000000		HALT		; DONE

5.0 MAINTENANCE DOCUMENTS

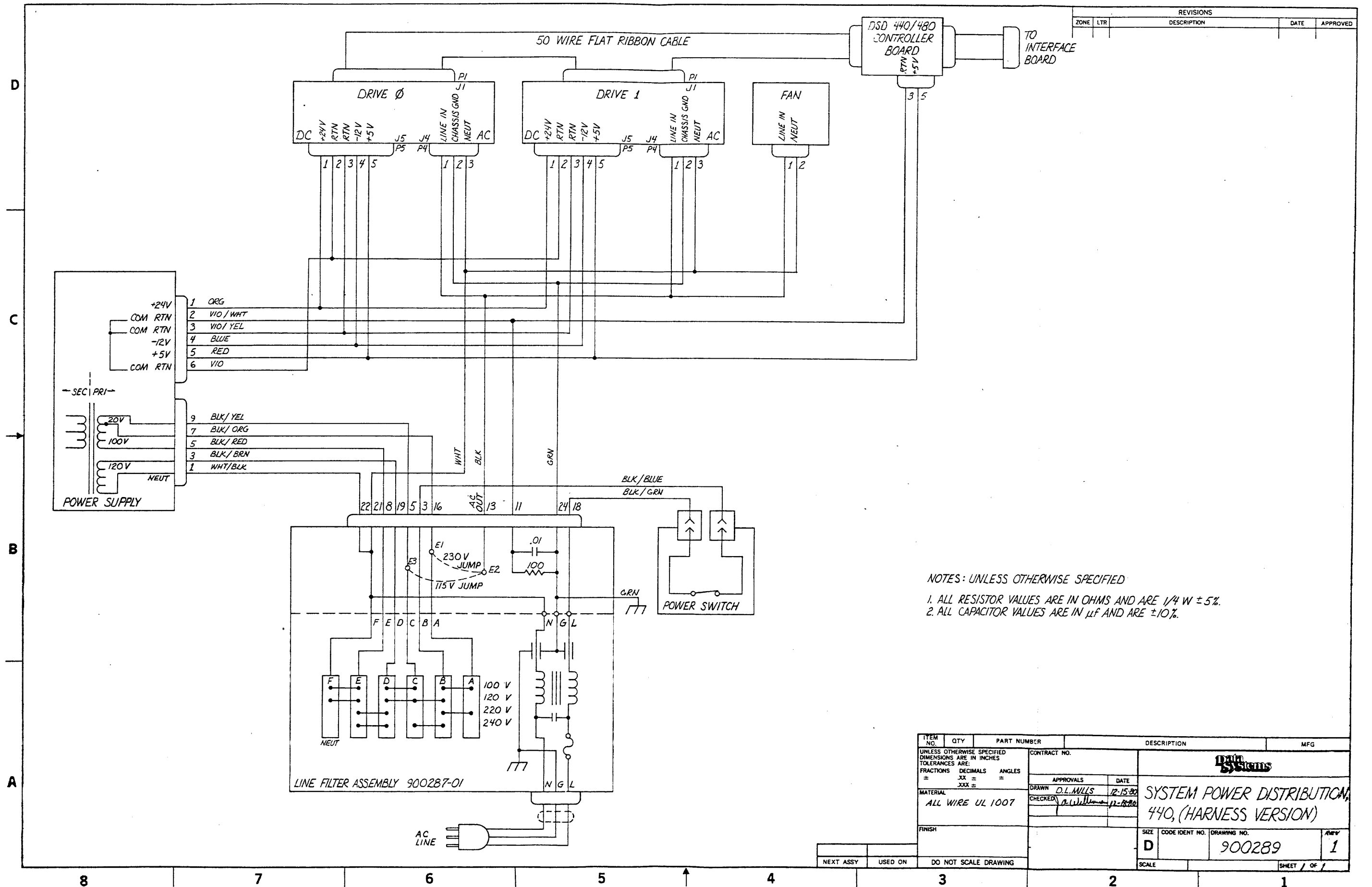
5.1 Illustrations

This section provides the diagrams, schematics, and parts lists for the DSD 440 and 480 Systems. It contains system power distribution diagrams, and schematics for the controller module and interface modules.

The schematic diagrams for the DSD 440/480 Controller Module have been formatted with 8-1/2 inch aprons so that the complete schematic may be unfolded to follow the theory discussion contained in Section 3 of this manual.

5.2 Parts Lists

Component parts lists have been made an integral part of the applicable illustrations for easy reference.

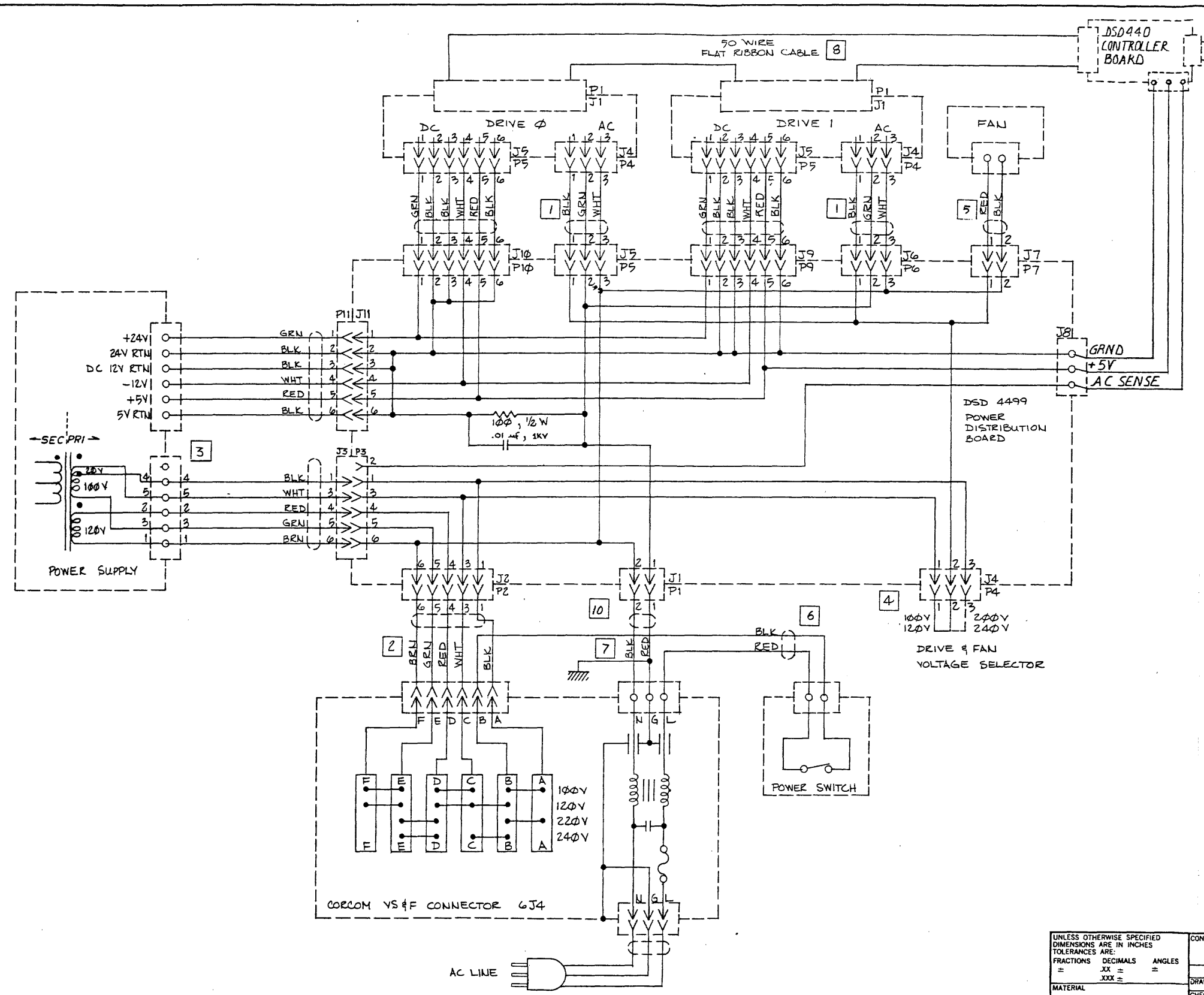


D

C

B

A



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		PER ECO# 114 & 117	6-17-80	AKK
		DRG # CHANGED FROM 9600001	3-23-81	

- NOTE:
- 1 6500010
 - 2 6501111
 - 3 6500004
 - 4 FOR 115V-6501113
FOR 230V-6501128
 - 5 6501115
 - 6 6501118
 - 7 6501119
 - 8 6504420
 - 9 6504428

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES = .XX = .XXX =	CONTRACT NO.	DATA Systems		
MATERIAL	APPROVALS DATE DRAWN J. MOISE 6-9-78			
FINISH	CHECKED DES ENG J. MOISE 6-12-78 PROJ ENG J. MOISE 6-12-78 MFG ENG J. MOISE 6-12-78			
DO NOT SCALE DRAWING	SIZE D	CODE IDENT NO. S/D	DRAWING NO. 900343	REV A
	SCALE NONE	SHEET 1 OF 1		

PARTS LIST, 4840-01/-02 CONTROLLER MODULE

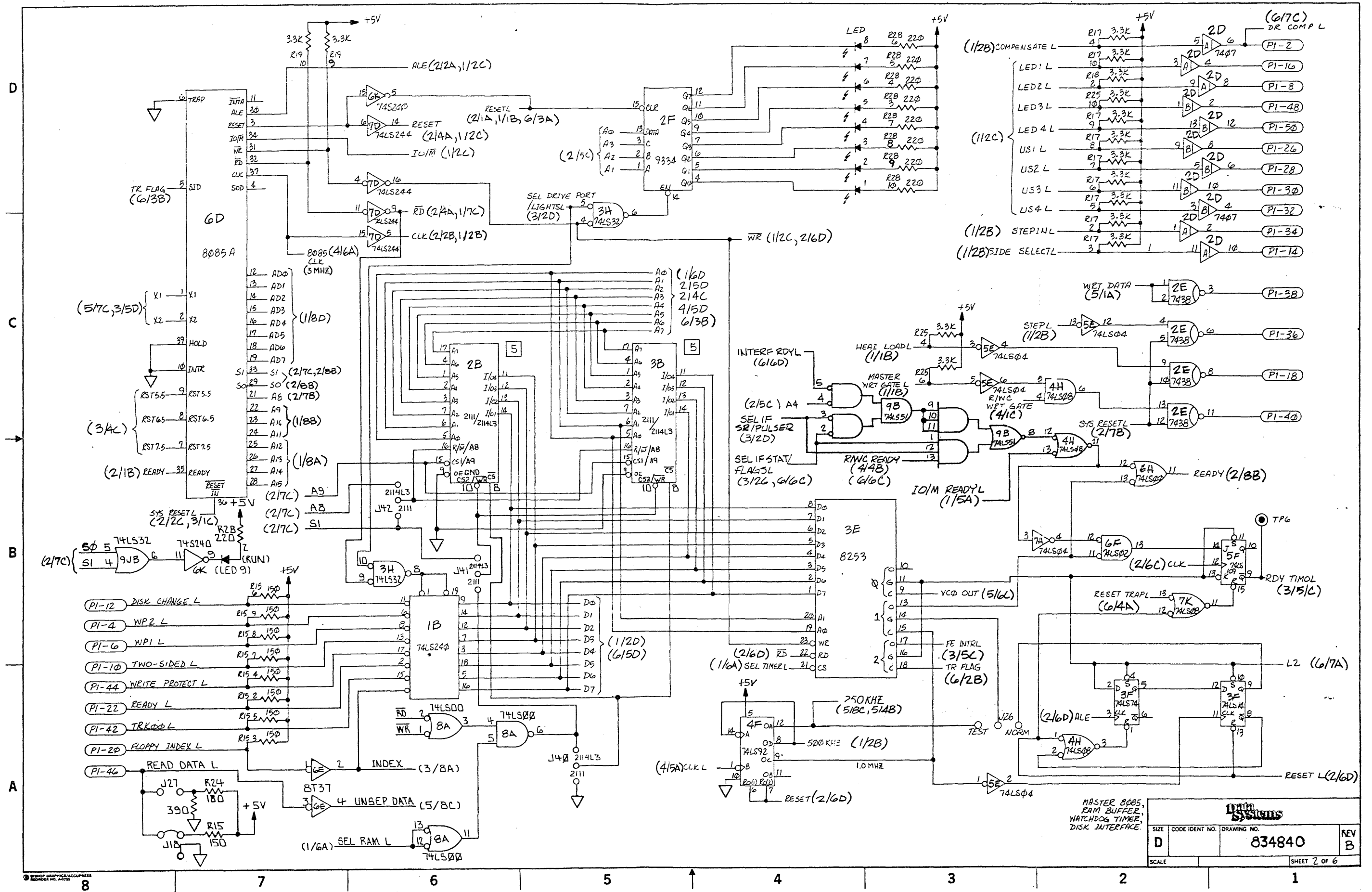
<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
1	080046-01	PROM ASSY, BRD PSTN 9L	1
2	080047-01	PROM ASSY, BRD PSTN 6N	1
3	080048-01	PROM ASSY, BRD PSTN 5C	1
4	080049-01	PROM ASSY, BRD PSTN 5D	1
5	080078-01	PROM ASSY, BRD PSTN 8B (DSD 440)	1
	080098-01	PROM ASSY, BRD PSTN 8B (DSD 480)	1
6	080079-01	PROM ASSY, BRD PSTN 7B (DSD 440)	1
	080099-01	PROM ASSY, BRD PSTN 7B (DSD 480)	1
7	080080-01	PROM ASSY, BRD PSTN 6B (DSD 440)	1
	080120-01	PROM ASSY, BRD PSTN 6B (DSD 480)	1
8	080102-01	PROM ASSY, BRD PSTN 6P	1
9	080103-01	PROM ASSY, BRD PSTN 5P	1
10	080104-01	PROM ASSY, BRD PSTN 3P	1
11	080105-01	PROM ASSY, BRD PSTN 4P	1
12	300121	IC, 8111 A-4 RAM (DSD 440)	2
	290009	IC, 2114 RAM (DSD 480)	2
13	300001	IC, 74LS00	2
14	300031	IC, 74S00	1
15	300002	IC, 74LS02	1
16	300032	IC, 74S02	1
17	300003	IC, 74LS04	4
18	300005	IC, 74LS11	1
19	300050	IC, 7407	2
20	300010	IC, 74LS08	2
21	300033	IC, 74S08	1
22	300007	IC, 74LS32	2
23	300051	IC, 7438	3
24	300008	IC, 74LS51	1
25	300009	IC, 74LS74	4
26	300035	IC, 74LS74	1
27	300011	IC, 74LS92	2
28	300012	IC, 74LS109	2
29	300052	IC, 74109	1
30	300013	IC, 74LS112	2
31	300037	IC, 74S112	1
32	300038	IC, 74S124	1
33	300014	IC, 74S138	1
34	300041	IC, 74S151	1
35	300015	IC, 74LS151	2
36	300075	IC, 74LS153	2
37	300017	IC, 74LS161	2
38	300060	IC, 74LS161A	1
39	300020	IC, 74LS193	1
40	300018	IC, 74LS173	3
41	300019	IC, 74LS174	3
42	300021	IC, 74LS221	1
43	300022	IC, 74LS240	2
44	300045	IC, 74S240	1
45	300023	IC, 74S244	2

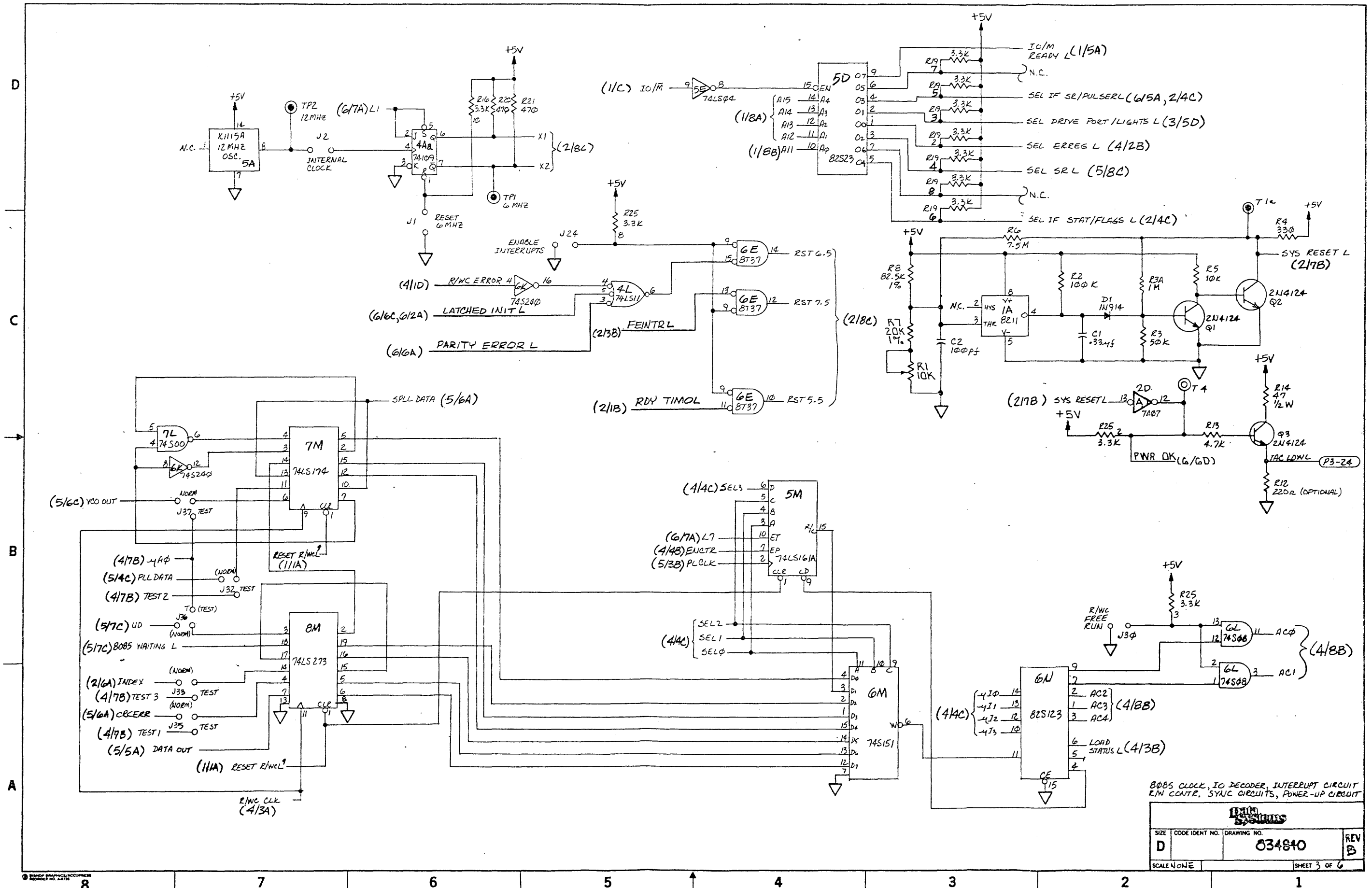
PARTS LIST, 4840-01/-02 CONTROLLER MODULE (Cont)

<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
46	300058	IC, 9334	2
47	300025	IC, 74LS273	3
48	300026	IC, 74LS299	3
49	300027	IC, 74LS373	1
50	300028	IC, 74LS374	2
51	300029	IC, 74LS378	1
52	300059	IC, 74LS386	1
53	330003	IC, 8155	1
54	330004	IC, 2911A	3
55	300054	IC, 8837	1
56	330002	IC, 8085A	1
57	300055	IC, 8211	1
58	330001	IC, 8253	1
59	300057	IC, 9401	1
60	310003	IC, CA3130E	1
61	380002	XTAL OSC, 12MHz	1
62	380001	XTAL OSC, 12.5 MHz, DELAY LINE	1
63	240002	LED, RED, RIGHT ANGLE	7
64	240001	LED, GREEN, RIGHT ANGLE	2
65	340002	TRANSISTOR, 2N4124, TO-92	4
66	340003	TRANSISTOR, 2N4126, TO-92	1
67	340001	TRANSISTOR, 2N2369, TO-92 or TO-18	2
68	240004	DIODE, 1N914	4
69	340004	TRANSISTOR, MPS 3640, TO-92, SWITCH	1
70	200007	RESISTOR, 1K, 1/4 W, 5%, CC/CF	3
71	200017	RESISTOR, 1 MEG, 1/4 W, 5%, CC/CF	1
72	200015	RESISTOR, 10K, 1/4 W, 5%, CC/CF	1
73	210004	RESISTOR, 10K, 1/4 W, 1%, MF	1
74	200016	RESISTOR, 100K, 1/4 W, 5%, CC/CF	1
75	200006	RESISTOR, 2.2K, 1/4 W, 5%, CC/CF	2
76	200013	RESISTOR, 2.7K, 1/4 W, 5%, CC/CF	1
77	200021	RESISTOR, 3.3K, 1/4 W, 5%, CC/CF	5
78	200011	RESISTOR, 330 OHM, 1/4 W, 5%, CC/CF	2
79	200005	RESISTOR, 47 OHM, 1/2 W, 5%, CC	1
80	200001	RESISTOR, 4.7K, 1/4 W, 5%, CC/CF	1
81	210006	RESISTOR, 4.99K, 1/4 W, 1%, MF	1
82	200012	RESISTOR, 5.1K, 1/4 W, 5%, CC/CF	2
83	210005	RESISTOR, 5.62K, 1/4 W, 1%, MF	4
84	200014	RESISTOR, 51K, 1/4 W, 5%, CC/CF	1
85	200018	RESISTOR, 7.5 MEG, 1/4 W, 5%, CC/CF	1
86	210001	RESISTOR, 82.5K, 1/4 W, 1%, MF	1
87	210003	RESISTOR, 20K, 1/4 W, 1%, MF	1
88	230029	RESISTOR, VARIABLE, 10K	3
89	230001	RESISTOR, VARIABLE, 500 OHM, .5 W, +20%	Factory Select
90	230013	RESISTOR, SIP, 150 OHM, 1.5 W, 2%, 10 PIN	1
91	230007	RESISTOR, SIP, 220 OHM, 1.5 W, 2%, 10 PIN	1
92	230011	RESISTOR, SIP, 3.3K, 1.5 W, 2%, 10 PIN	5

PARTS LIST, 4840-01/-02 CONTROLLER MODULE (Cont)

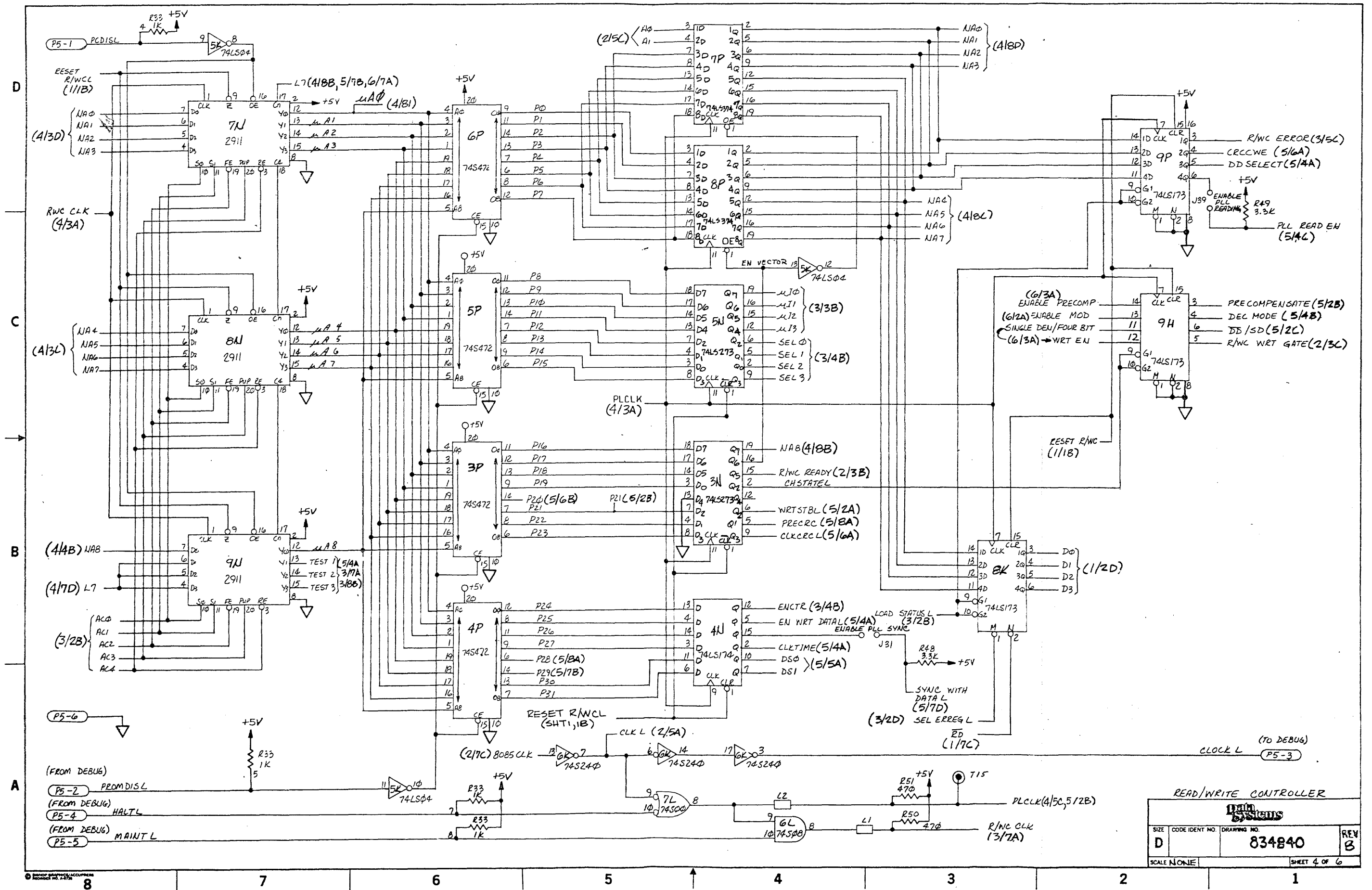
<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
93	230009	RESISTOR, SIP, 180/390 OHM, 2.1 W, 2%, 8 PIN	2
94	230012	RESISTOR, SIP, 1K, 1.5 W, 2%, 10 PIN	1
95	250007	CAPACITOR, .01 Mf, 50V, CER, RAD	8
96	260001	CAP, 22 Mf, 16V, TANT, RAD	2
97	250002	CAP, 39 Pf, 16V, MONO, CER, RAD	1
98	250013	CAP, .33 Mf, 100V, MONO, CER, RAD	1
99	250012	CAP, 1 Mf, 50V, MONO, CER, RAD	3
100	250003	CAP, 100 Pf, 100V, MONO, CER, RAD	4
101	250009	CAP, .01 Mf, 50V, MONO, CER, RAD	4
102	250011	CAP, .1 Mf, 50V, MONO, CER, RAD	1
103	250005	CAP, 470 Pf, 50V, MONO, CER, RAD	2
104	170001	SWITCH, DIP, 8 POSITION	1
105	130001	SHUNT, DIP, 8 POSITION, 16 PIN	1
106	200008	RESISTOR, 750 OHM, 1/4 W, 5%, CC/CF	1
107	200031	RESISTOR, 470 OHM, 1/4 W, 5%, CC	4
108	200003	RESISTOR, 68 OHM, 1/4 W, 5%, CC	1
109	250010	CAP, .1 Mf, 50V, Z5U, AXIAL	54

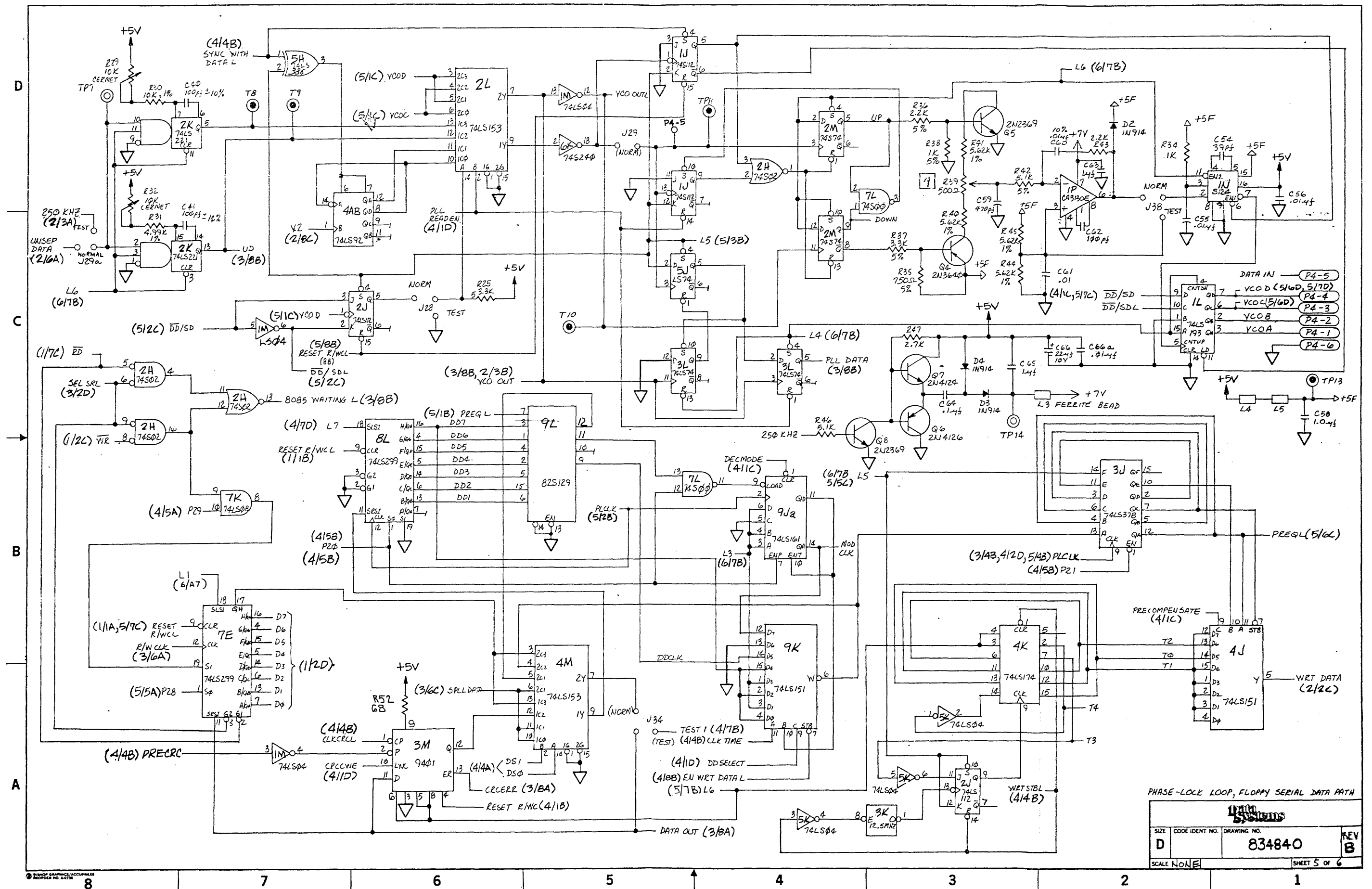


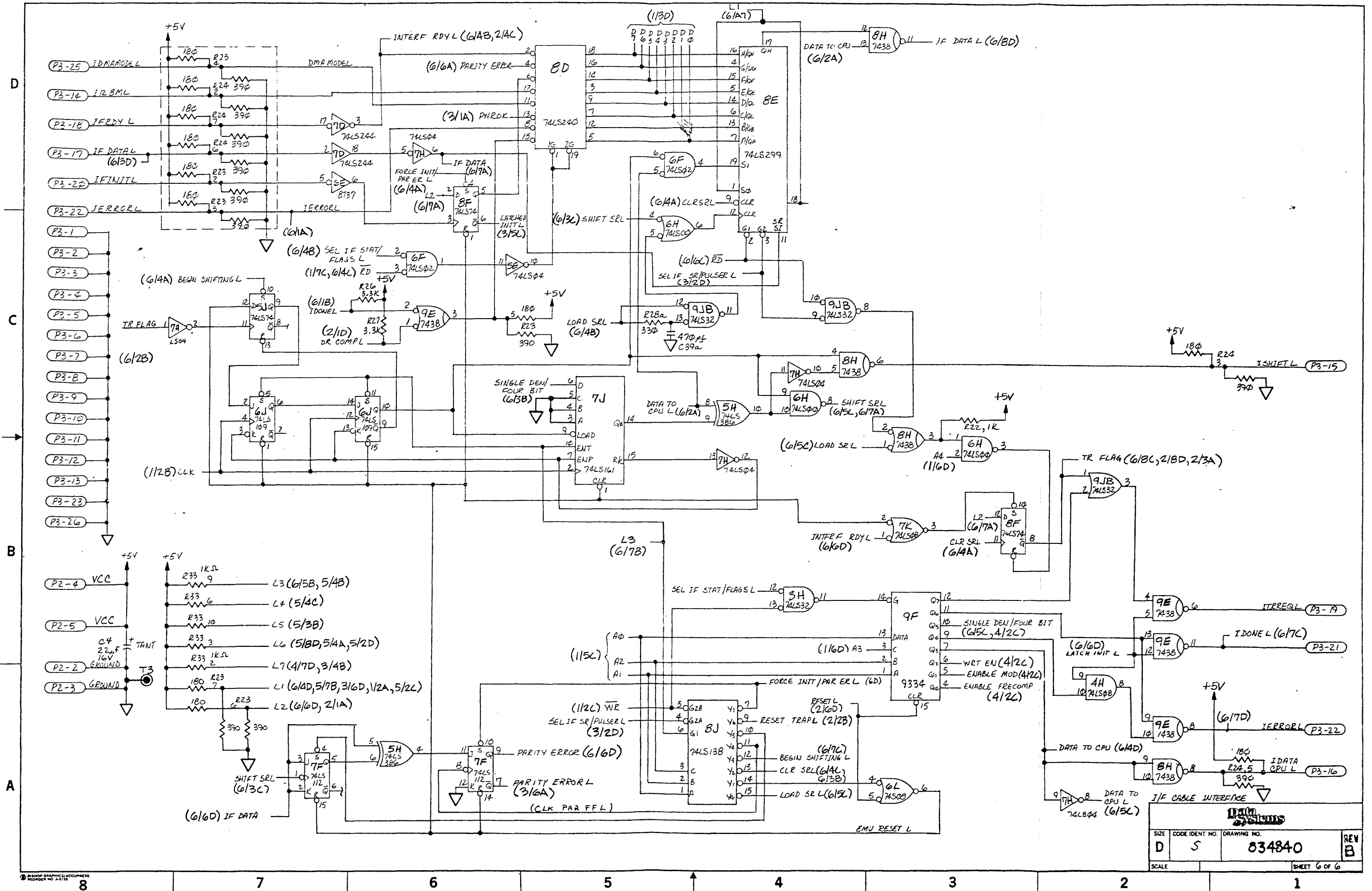


8085 CLOCK, IO DECODER, INTERRUPT CIRCUIT
R/W CONTR. SYNC CIRCUITS, POWER-UP CIRCUIT

Data Systems		
SIZE	CODE IDENT NO.	DRAWING NO.
D		034840
SCALE NONE	REV B	
		SHEET 3 OF 6

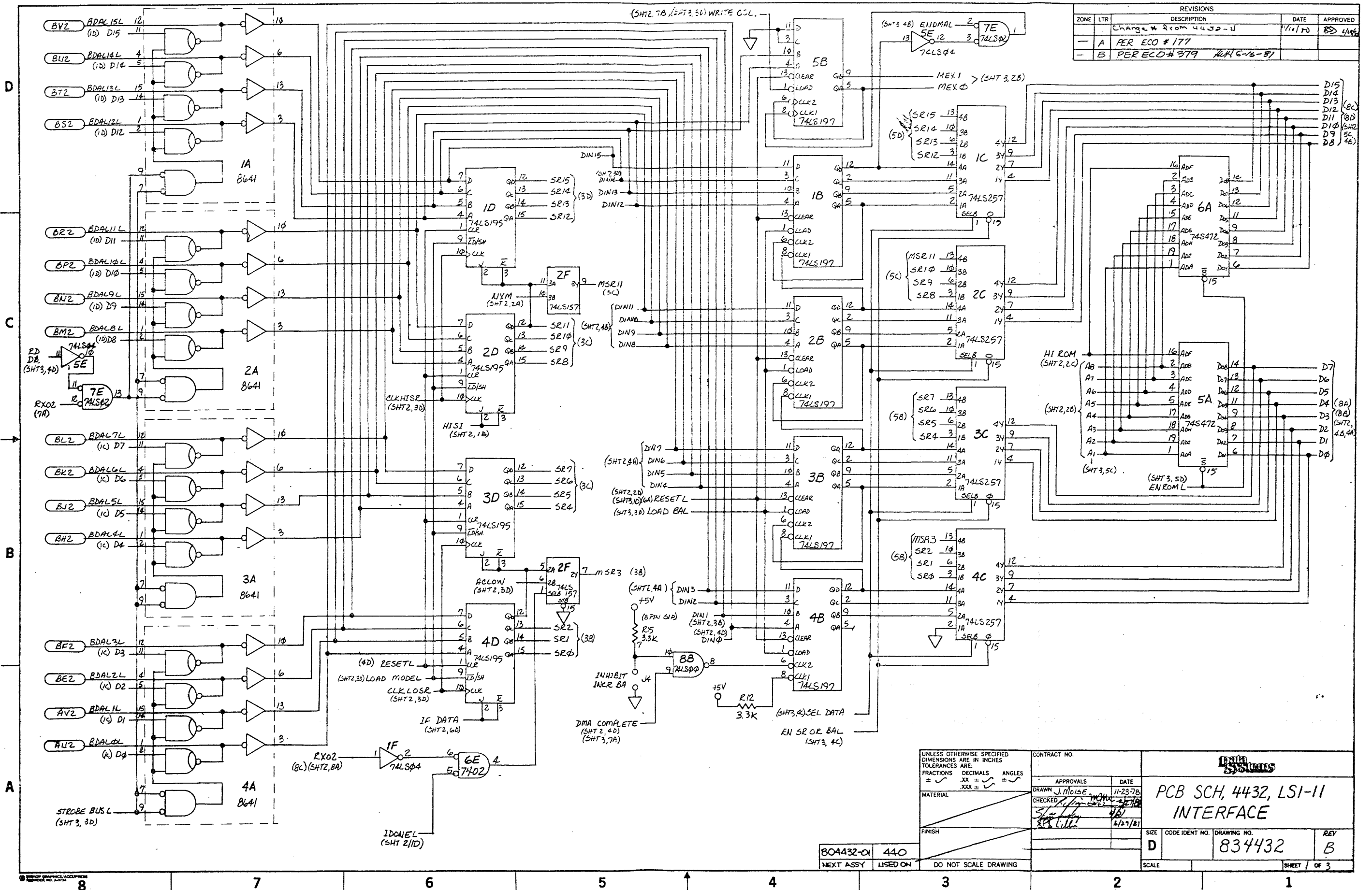






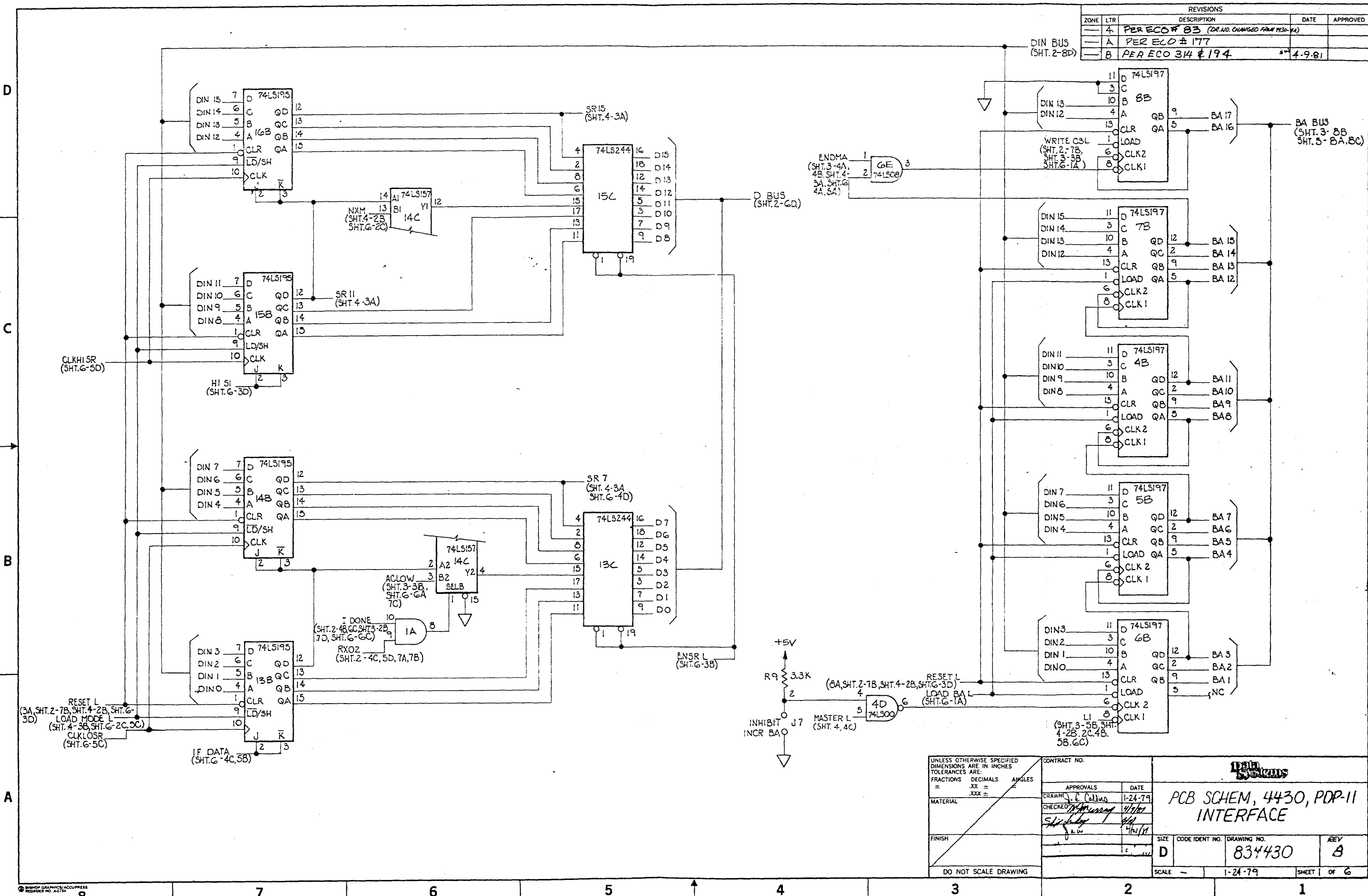
PARTS LIST, 4432, LSI-11 INTERFACE MODULE

<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
1	080032-01	PROM ASSY, BRD PSTN 4H	1
2	080033-01	PROM ASSY, BRD PSTN 7C	1
3	080034-01	PROM ASSY, BRD PSTN 5C	1
4	080035-01	PROM ASSY, BRD PSTN 5A	1
5	080036-01	PROM ASSY, BRD PSTN 6A	1
6	080037-01	PROM ASSY, BRD PSTN 7H	1
7	080038-01	PROM ASSY, BRD PSTN 9H	1
8	130001	SHUNT, DIP, 8 PSTN, 16 PIN	1
9	130023	SHUNT, DIP, 4 PSTN	1
10	300001	IC, 74LS00	1
11	300002	IC, 74LS02	1
12	300003	IC, 74LS04	3
13	300010	IC, 74LS08	4
14	300004	IC, 74LS10	1
15	300007	IC, 74LS32	1
16	300072	IC, 7402	1
17	300051	IC, 7438	3
18	300035	IC, 74LS74	1
19	300009	IC, 74LS74	1
20	300013	IC, 74LS112	3
21	300019	IC, 74LS174	1
22	300016	IC, 74LS157	1
23	300107	IC, 74LS195	4
24	300073	IC, 74LS197	6
25	300024	IC, 74LS257	8
26	300025	IC, 74LS273	1
27	300022	IC, 74LS240	1
28	300027	IC, 74LS373	1
29	300090	IC, 74LS375	1
30	300054	IC, 8837	1
31	300053	IC, 8641	5
32	300115	IC, 9602	1
33	380002	XTAL OSC, 12 MHz	1
34	200004	RESISTOR, 120 OHM, 1/4W, 5%, CC	2
35	200002	RESISTOR, 220 OHM, 1/4W, 5%, CC	1
36	200026	RESISTOR, 390 OHM, 1/4W, 5%, CC	4
37	200033	RESISTOR 390 OHM, 1/4 W, 5%, CC	4
38	200021	RESISTOR 3.3K, 1/4 W, 5%, CC/CF	8
39	200015	RESISTOR, 10K, 1/4W, 5%, CC/CF	1
40	230027	RESISTOR, SIP, 180/390, 2.7W, 5%, 10 PIN	1
41	200025	RESISTOR, 33K, 1/4 W, 5%, CC	1
42	230024	RESISTOR, SIP, 3.3K, 1.1 W, 2%, 8 PIN	1
43	230011	RESISTOR, SIP, 3.3K, 1.5 W, 2%, 10 PIN	1
44	240004	DIODE, 1N 914	1
45	250026	CAP, 1 Mf, 50V	1
46	250007	CAP, .01 Mf, 50V, CER, RAD	33
47	250023	CAP, 820 Pf, 50V	2
48	250016	CAP, 3900 Pf, 50V	1
49	260012	CAP, 100 Mf, 16V, ALM, ELEC, AXIAL	1
50	200016	RESISTOR, 100K, 1/4 W, 5%, CC/CF	1



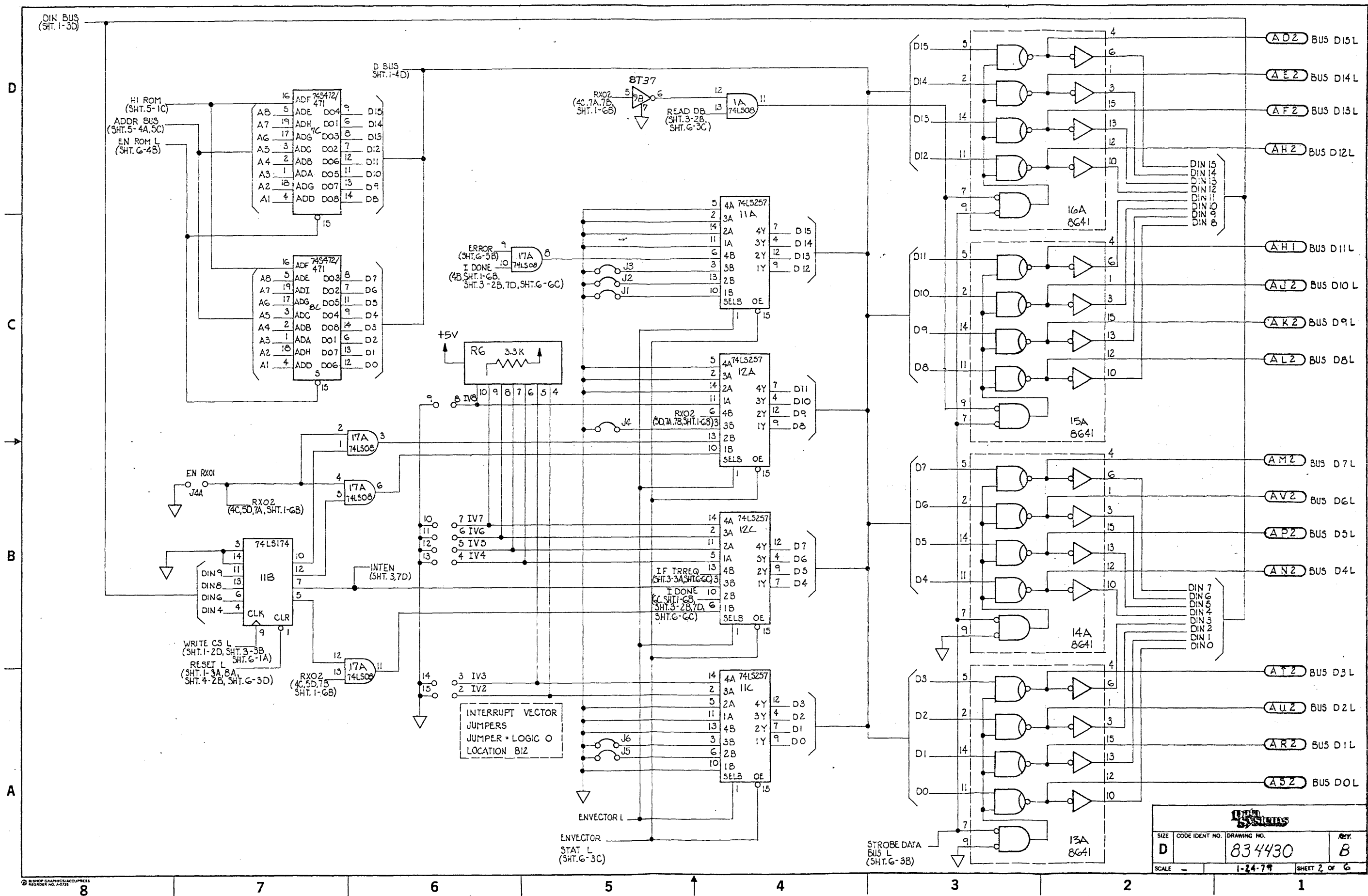
PARTS LIST, 4430, PDP-11 INTERFACE MODULE

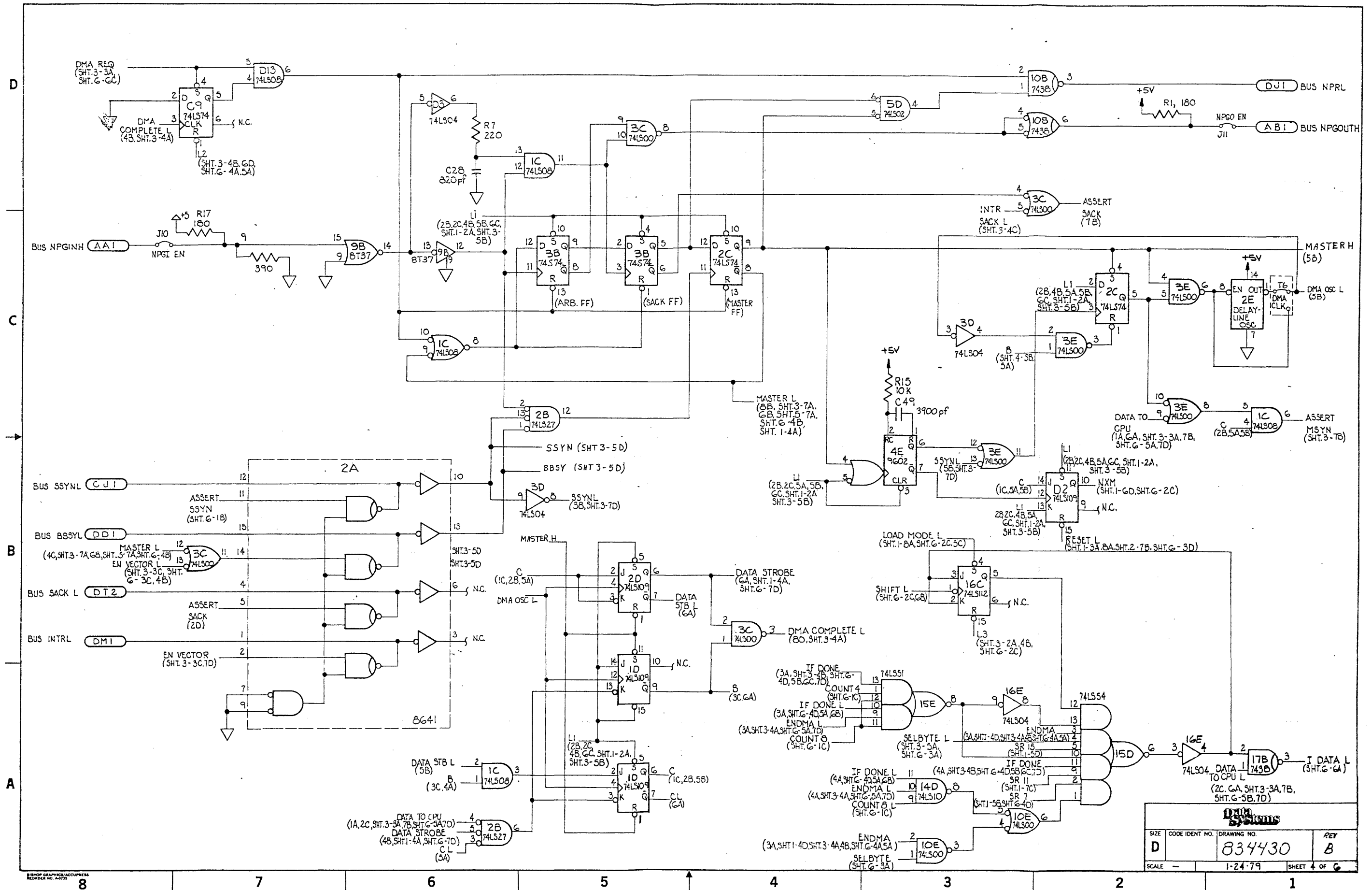
<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
1	080039-01	PROM ASSY, BRD PSTN 4C	1
2	080040-01	PROM ASSY, BRD PSTN 8C	1
3	080041-01	PROM ASSY, BRD PSTN 7C	1
4	130023	SHUNT, DIP, 4 PSTN	1
5	130001	SHUNT, DIP, 8 PSTN, 16 PIN	2
6	300001	IC, 74LS00	7
7	300002	IC, 74LS02	2
8	300003	IC, 74LS04	3
9	300010	IC, 74LS08	6
10	300004	IC, 74LS10	2
11	300006	IC, 74LS27	1
12	300005	IC, 74LS11	1
13	300007	IC, 74LS32	2
14	300051	IC, 7438	2
15	300008	IC, 74LS51	2
16	300094	IC, 74LS54	3
17	300035	IC, 74LS74	2
18	300009	IC, 74LS74	2
19	300012	IC, 74LS109	2
20	300016	IC, 74LS157	1
21	300019	IC, 74LS174	1
22	300107	IC, 74LS195	4
23	300073	IC, 74LS197	6
24	300022	IC, 74LS240	1
25	300024	IC, 74LS244	2
26	300024	IC, 74LS257	4
27	300105	IC, 74LS266	1
28	330011	IC, 8160	1
29	300054	IC, 8837	1
30	300053	IC, 8641	10
31	300115	IC, 9602	1
32	380001	XTAL OSC, 12.5 MHz, DELAY LINE	1
33	200016	RESISTOR, 100K, 1/4W, 5%, CC	1
34	200004	RESISTOR, 120 OHM, 1/4W, 5%, CC	1
35	200026	RESISTOR, 390 OHM, 1/4W, 5%, CC	1
36	200032	RESISTOR, 180 OHM, 1/4W, 5%, CC	3
37	200007	RESISTOR, 1K, 1/4W, 5%, CC/CF	6
38	200002	RESISTOR, 220 OHM, 1/4W, 5%, CC	3
39	200015	RESISTOR, 10K, 1/4W, 5%, CC/CF	1
40	230027	RESISTOR, SIP, 180/390, 2.7W, 5%, 10 PIN	1
41	230011	RESISTOR, SIP, 3.3K, 1.5 W, 2%, 10 PIN	3
42	250007	CAP, .01 Mf, 50 V, CER, RAD	48
43	260012	CAP, 100 Mf, 16V, ALM, ELEC, AXIAL	2
44	250023	CAP, 820 Pf, 50 V	3
45	250016	CAP, 3900 Pf, 50 V	1



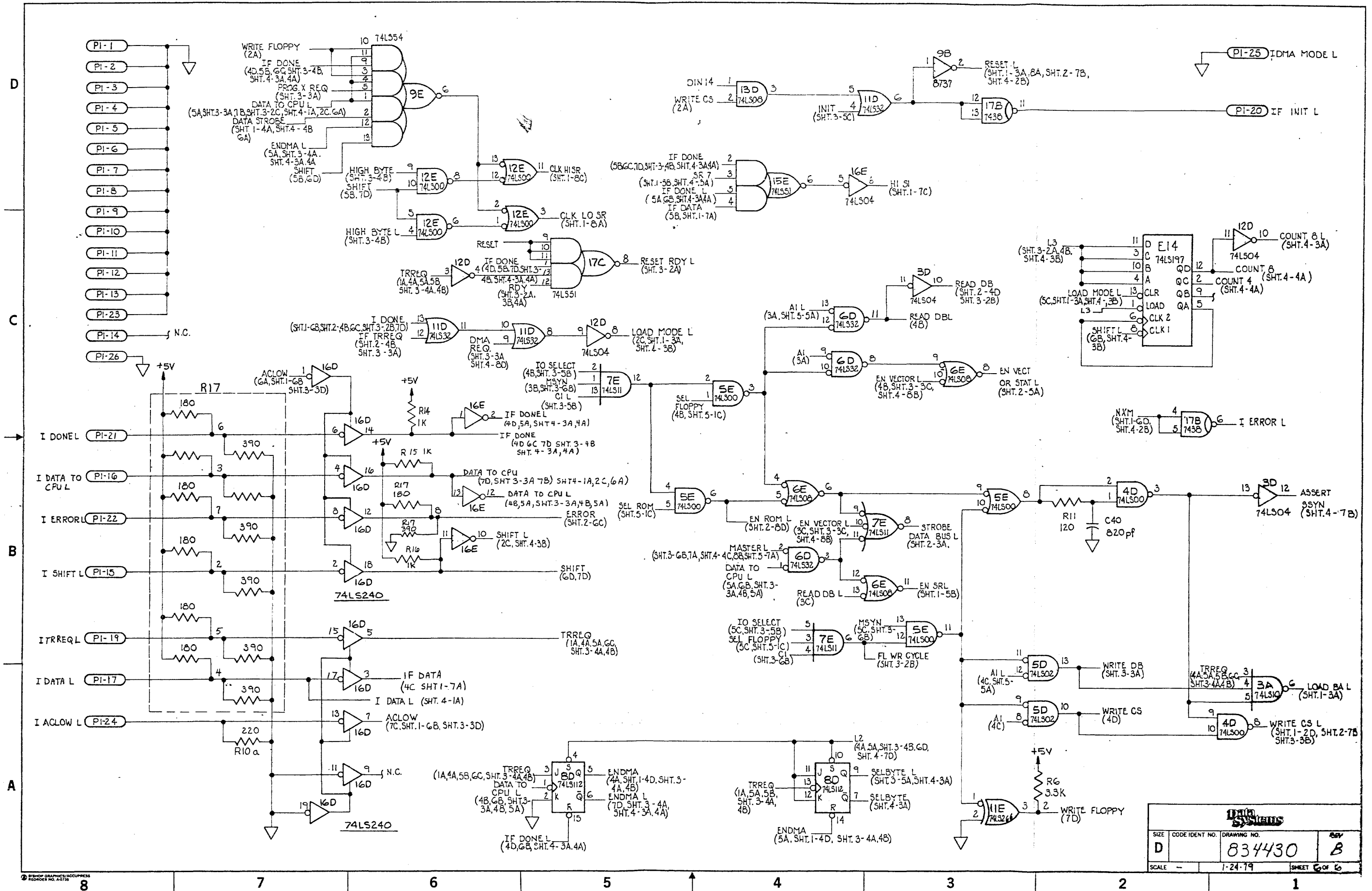
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
4		PER ECO # 83 (DR. NO. CHANGED FROM 1130-11)		
A		PER ECO # 177		
B		PER ECO 314 & 194	4-9-81	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES = .XX = .XXX =		CONTRACT NO.	
APPROVALS DRAWN: C. G. G. 1-24-79 CHECKED: S. J. J. 4/1/81 DATE: 4/1/81		DATE: 4/1/81	
MATERIAL		PCB SCHEM, 4430, PDP-11 INTERFACE	
FINISH		SIZE: D CODE IDENT NO. 834430 REV: B	
DO NOT SCALE DRAWING		SCALE: 1-24-79 SHEET 1 OF 6	



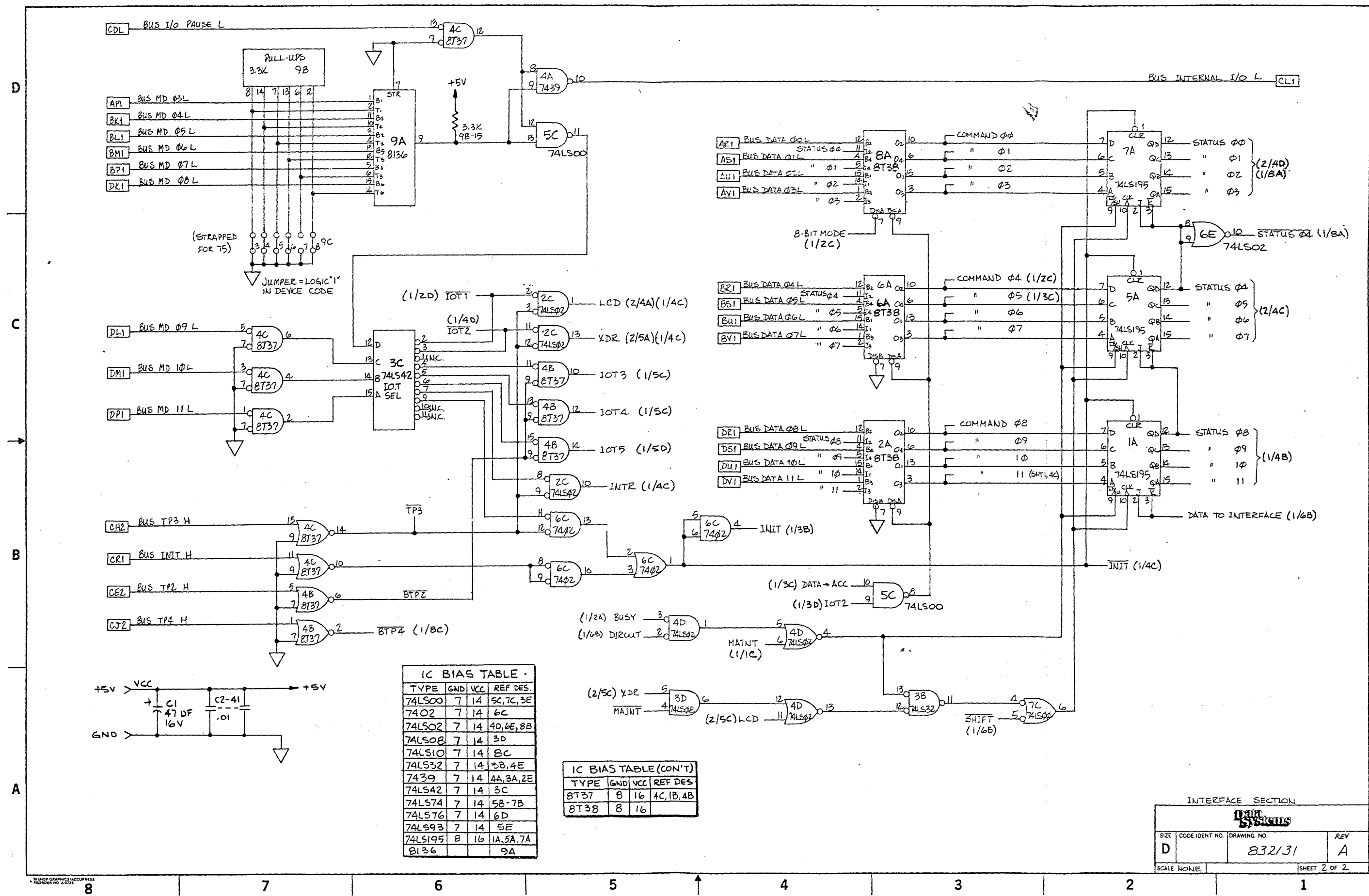


D			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		834430	B
SCALE	1-24-79		SHEET 4 OF 6



PARTS LIST, 2131, PDP-8 INTERFACE MODULE

<u>ITEM</u>	<u>DSD PART NO.</u>	<u>DESCRIPTION/REMARKS</u>	<u>QTY</u>
1	300072	IC, 7402	1
2	300117	IC, 7439	3
3	330012	IC, 8136	1
4	300054	IC, 8837	3
5	300111	IC, 8838	3
6	300001	IC, 74LS00	3
7	300002	IC, 74LS02	4
8	300010	IC, 74LS08	2
9	300004	IC, 74LS10	1
10	300007	IC, 74LS32	2
11	300064	IC, 74LS42	1
12	300009	IC, 74LS74	5
13	300108	IC, 74LS76	1
14	300096	IC, 74LS93	1
15	300107	IC, 74LS195	3
16	230018	RESISTOR, DIP, 220/330, 1.75 W, 2%, 16 PIN	1
17	230020	RESISTOR, DIP, 3.3K, 1.75 W, 2%, 16 PIN	1
18	260007	CAP, 47 Mf, 16 V, ALM, ELEC, AXIAL	1
19	250007	CAP, .01 Mf, 50 V, CER, RADIAL	40



INTERFACE SECTION			
Data Systems			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		832/31	A
SCALE NONE	SHEET 2 OF 2		

We've changed our name
from Data Systems Design to

QUALOGY