

[illegible]

```
77777777 999999 000000 DDDDDDDD EEEEEEEEE FFFFFFFF
77777777 999999 000000 DDDDDDDD EEEEEEEEE FFFFFFFF
      77 99 99 00 00 DD DD EE FF
      77 99 99 00 00 DD DD EE FF
      77 99 99 00 0000 DD DD EE FF
      77 99 99 00 0000 DD DD EE FF
      77 99999999 00 00 00 DD DD EEEEEEE FFFFFFFF
      77 99999999 00 00 00 DD DD EEEEEEE FFFFFFFF
      77 99 0000 00 DD DD EE FF
      77 99 0000 00 DD DD EE FF
      77 99 00 00 DD DD EE FF
      77 99 00 00 DD DD EE FF
      77 999999 000000 DDDDDDDD EEEEEEEEE FF
      77 999999 000000 DDDDDDDD EEEEEEEEE FF
```

....
....
....
....

```
MM MM DDDDDDDD LL
MM MM DDDDDDDD LL
MMMM MMM DD DD LL
MMMM MMM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM MM DD DD LL
MM MM DDDDDDDD LLLLLLLLLL
MM MM DDDDDDDD LLLLLLLLLL
```

.TITLE 790DEF -- 11/790 macro definitions

Version: 'V04-000'

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FACILITY: VAX/VMS CPU-dependent Code Macro Libraries

ABSTRACT:

This file contains the MDL source for 11/790-specific macro definitions.

ENVIRONMENT:

n/a

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AUTHOR: Trudy C. Matthews CREATION DATE: 23-Jul-1982

MODIFIED BY:

V03-010 WMC0004 Wayne Cardoza 08-Jul-1984
Assorted spec changes (VENREG82)
V03-009 TCM0007 Trudy C. Matthews 04-Apr-1984
New values for symbols STXCS\$C_READP and STXCS\$C_WRITEP.
V03-008 TCM0006 Trudy C. Matthews 02-Jun-1983
Update register definitions according to latest spec (VENREG80).

V03-007 TCM0005 Trudy C. Matthews 27-Apr-1983
Add symbols STXC\$C_READP and STXC\$C_WRITEP (read and
write physical block).

V03-006 TCM0004 Trudy C. Matthews 15-Dec-1982
Correct definition of MERG register.

V03-005 TCM0003 Trudy C. Matthews 1-Dec-1982
Add \$STXC\$DEF and \$STXDBDEF.

V03-004 WMC0002 Wayne Cardoza 16-Nov-1982
Fix error in cache sweep register.

V03-003 WMC0001 Wayne Cardoza 05-Nov-1982
Add missing mask bit definitions.

V03-002 TCM0002 Trudy C. Matthews 20-Oct-1982
Added \$MDCTL register definitions.

V03-001 TCM0001 Trudy C. Matthews 11-Aug-1982
Add SBIA\$V_TYPE and SBIA\$V_REV fields to \$SBIADEF.

```
;++  
: PAMM - Physical Address Memory Map bit and field definitions for 11/790  
: (IPRs 40 (PAMM access register) and 41 (PAMM location register))  
:--
```

```
$STRUCT PAMM                                ;11/790 Physical Address Memory Map  
V      <M  
      CODE,4                                ; PAMM type code  
      CACHE,1                              ; Cache disable bit  
      ,15                                  ; MBZ  
      PAMADD,10                             ; PAMM physical address field  
      ,2                                  ; MBZ  
      >  
C <PAMM, $C                                ;Configuration field bit definitions  
      MEM0,0                               ;Internal array slot 0  
      MEM1,1                               ;internal array slot 1, etc.  
      MEM2,2  
      MEM3,3  
      MEM4,4  
      MEM5,5  
      MEM6,6  
      MEM7,7  
      IOA0,8                               ;ABUS I/O Adapter 0  
      IOA1,9                               ;ABUS I/O Adapter 1  
      IOA2,10                              ;ABUS I/O Adapter 2  
      IOA3,11                              ;ABUS I/O Adapter 3  
      NEXM,15                             ;Non existant memory  
      >  
E
```

```
:++  
: CSWP -- Cache sweep register (IPR 42)  
:--
```

```
$STRUCT CSWP      : Cache sweep register  
V          <M  
          COENA,1   : Cache 0 enable  
          C1ENA,1   : Cache 1 enable  
          VAL,1     : Leave cache valid after sweep  
          INV,1     : Invalidate cache after sweep  
>
```

```
E
```

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```

:++
:--
MDCTL  - Memory Data Control Register (IPR 45)
$STRUCT MDCTL
V      <M
      LNGPER,4          ; Generate longword parity error.
      4
      CHPERR,1          ; Enable cache byte parity error.
      INVREG,1          ; Enable invert register.
      DISECC,1          ; Disable ECC correction on data.
      INHBAD,1          ; Inhibit bad data flag.
      ABUSPE,1          ; Enable ABUS longword parity error.
      CHKREAD,1         ; Read check bits from selected cache rams.
      INHDPE,1         ; Inhibit data parity error check.
      >
E
```

```

:++
: ACCS -- Accelerator Control and Status Register (IPR 4B)
:--
$STRUCT ACCS          ; Floating point accelerator register
V  <M
   TYPE,8             ; Signals presence and type of acc.
   7
   ENABLE,1           ; Enable FP acceleration
   REV,8              ; Revision level of VENUS FBOX
>
E
```

```
;++  
: CRBT -- Console reboot register (IPR 48)  
:--
```

```
$STRUCT CRBT  
F ADDRESS,B ; Console address used to force reboot  
F CODE,B ; Reboot code  
E
```

++
: MENA -- M-box error report enable register (IPR 44)
--

\$STRUCT MENA

V<M

CHDATPEBW,1	: Cache byte write data parity error
,2	: MBZ
CHDATPENBW,1	: Cache non byte write data parity error
WBYTEPE,4	: Write byte parity error mask
TBTAGPE,1	: TB tag parity error
PTEAPE,1	: PTE A parity error
PTEBPE,1	: PTE B parity error
TBVALID,1	: TB valid error
,7	: MBZ
ABUSAPE,1	: ABUS address parity error
ABUSCPE,1	: ABUS control parity error
ABUSDPE,1	: ABUS data parity error
CPRAPE,1	: CPR A parity error
CPRBPE,1	: CPR B parity error
,8	: MBZ
>	

E

```
;++  
: MDECC -- Memory data ECC error status register (IPR 43)  
:--  
$STRUCT MDECC  
V<M  
    DIAG,8           ; Diagnostic control bits  
    ,1  
    SYNDROME,6       ; Syndrome for error  
    DLWP1,1          ; Data longword parity is inverted  
    ,2  
    DAPE,1           ; Data address parity error  
    RDS,1            ; Multiple-bit data error  
    CRD,1            ; Single-bit data error  
    BDE,1            ; Known bad data written  
    MULT,1           ; Multiple memory errors occurred  
  
>  
E
```

++
: MERG -- Memory Error Register (IPR 47)
: --

\$STRUCT MERG

V<M

DIAG,8

MME,1

1

INHCRD,1

ABUSEVEN,1

INHDMA,1

; Diagnostic bits

; Memory management enable

; MBZ

; Inhibit corrected error reporting

; Generate ABUS command w/ even parity

; Inhibit DMA requests from SBIA

>
E

```
;++
: EHSR -- Error Handling Status Register (IPR 4A)
:--
```

```
$STRUCT EHSR
V<M
```

```
IBOXGPR,1      : Error in IBOX register RAMs
EBOXA,1        : Error in A side of EBOX scratchpad
EBOXB,1        : Error in B side of EBOX scratchpad
FBOXGPR,1      : Error in FBOX register RAMs
FBOXERR,1      : Error in FBOX hardware
VMS,1          : "VMS mcheck module entered" flag
EHM,1          : Error Handling Microcode entered flag
MBOXERR,1      : Error in MBOX hardware
DIAGFLT,1      : Mcheck caused by fault insertion
,16
AUTOSHUT,1     : Severe error detected by error microcode
MEARSAV,1      : Means something to microcode
ICS,1          : Error in IBOX control store
IDRAM,1        : Error in IBOX data RAM
FDRAM,1        : Error in FBOX data RAM
FBACS,1        : Error in FBOX adder control store
FBMCS,1        : Error in FBOX multiplier control store
```

```
>
E
```

++
IBESR -- IBOX Error Status Register (internal)
--

\$STRUCT IBESR
V<M

8		
UOP_SEL,3		; Specifies OP-bus data source
UTPR,3		; Specifies which port cause u-trap
7		
ICSPE,1		; IBOX control store parity error
DRAMPE,1		; IBOX data RAM parity error
IAMUXPE,1		; IBOX AMUX parity error
RLOGPE,1		; Parity error in register log
IBUFPE,1		; Instruction buffer parity error
IBMUXPE,1		; IBOX BMUX parity error
RSV,1		; Reserved mode
IWBUSPE,1		; WBUS parity error detected by IBOX
IAMUXEC,2		; ?

>
E

```
;++
EDPSR -- EBOX Data path status register (internal)
--
```

```
$STRUCT EDPSR
```

```
V<M
```

```
BRAM,1      ; Scratchpad RAM to BMUX parity error
AWBUS,1     ; WBUS to AMUX parity error
ARAM,1      ; Scratchpad RAM to AMUX parity error
OPER,1      ; Operand parity error
,1          ; MBZ
RSLT,1      ; Result parity error
BOPBUS,1    ; OPbus to BMUX parity error
BWBUS,1     ; WBUS to BMUX parity error
EDPMISC,1   ; Miscellaneous source parity error
,2
WREG,1      ; W-register parity error
VMQBYTE,4   ; Which byte of EDP VMQ contains error
,8
AMXBYTE,4   ; Which byte of EDP AMUX contains error
BMXBYTE,4   ; Which byte of EDP BMUX contains error
```

```
>
E
```

```
:++  
: MSTAT2 -- MBOX Status Register  
:--
```

```
$STRUCT MSTAT2
```

```
V<M
```

```
ACRPE,1  
MBXLCK,1  
IOBUFF,1  
NXM,1  
CACHEW,1  
CTAGW,1  
CTAG,1  
MUL1,1  
SBIADG,8
```

```
: Access control RAM parity error  
: Error occurred during MBOX lock  
: CP buff error on I/O request  
: Non-existent memory error  
: "Cache written" bit  
: Cache error in written bit of tag  
: Cache tag parity error  
: Multiple error flag  
: Diagnostic status from SBIA
```

```
>  
E
```

```
:++
: CSHCTL -- Cache state register
:--
```

```
$STRUCT CSHCTL
```

```
V<M
```

```
COENA,1      : Cache 0 Enable
C1ENA,1      : Cache 1 Enable
FRCHIT,1     : Force cache hit
FRCMIS,1     : Force cache miss
```

```
>
```

```
E
```

```
:++
: CSES -- Console control store correction status
:--
```

```
$STRUCT CSES
```

```
V<M
```

```
CODE,3       : Code identifying CS to correct
5
CSYN,8       : Control store syndrome
CSADDR,13    : Control store address
2
CORR,1       : Console has corrected the error
```

```
>
```

```
E
```

```
;++  
: CSLSR -- Console state and error register  
:--
```

```
$STRUCT CSLSR
```

```
V<M
```

```
STATUS,16  
SYND,16
```

```
; Console status  
; Console RAM error syndrome
```

```
>  
E
```

```

:++
: 11/790 Synchronous Backplane Interconnect Adapter register definitions
:--

```

```

$STRUCT SBIA          :11/790 SBI ADAPTER
F          CR,L        :CONFIGURATION REGISTER
V          <M
          REV,4         : ADAPTER REVISION LEVEL
          TYPE,4        : ADAPTER TYPE CODE FIELD
          ,12
          MEMSEP,10     :MEMORY SEPARATOR
          >
F          CSR,L        :CONTROL/STATUS REGISTER
V          <M
          ,24
          TRSEL1,1      :DMA TR SELECT 1
          TRSEL2,1      :DMA TR SELECT 2
          TRSEL4,1      :DMA TR SELECT 4
          TRSEL8,1      :DMA TR SELECT 8
          ,1
          CI,1          : Enable SBI Cycles In
          CO,1          : Enable SBI Cycles Out
          MIE,1         : Master interrupt enable
          >
F          SUMRY,L      : Error summary register
V          <M
          IIE,3         : IOA detected parity error on DMAI
          DIT,1         : DMA Interlock Timeout
          IAE,3         : IOA detected parity error on DMAA
          ,1
          IBE,3         : IOA detected parity error on DMAB
          ,1
          ICE,3         : IOA detected parity error on DMAC
          ,1
          MCE,1         : Multiple CPU error
          ,1
          IME,1         : IOA State Machine Parity Error
          CAE,1         : Command address error
          AE,1          : Address error on CPU transaction
          RCP,1         : Register Control parity error
          ADP,1         : Register address/data parity error
          BEL,1         : CPU buffer error lock
          ,2
          CMDLEN,2      : ABUS command length
          CMDCOD,4      : ABUS command code
          >
F          DIAGNOS,L    : Diagnostic control
V          <M
          ,1
          FSP,1         : Force state machine parity error
          LBM,1         : Force loop back mode
          FQD,1         : Force quad data
          DCP,1         : Disable control parity
          DAD,1         : Disable address/data parity
          ,10
          DMAIBSY,1     : Force DMAI busy

```

```

DMAABSY,1      ; Force DMAA busy
DMABBSY,1      ; Force DMAB busy
DMACBSY,1      ; Force DMAC busy
>
F DMAICA,L      ;DMAI COMMAND ADDRESS REGISTER
F DMAIID,L      ;DMAI ID REGISTER
V <
IID,5,,M       ;ID
>
F DMAACA,L      ;DMAA COMMAND ADDRESS REGISTER
F DMAAID,L      ;DMAA ID REGISTER
V <
AID,5,,M       ;ID
>
F DMABCA,L      ;DMAB COMMAND ADDRESS REGISTER
F DMABID,L      ;DMAB ID REGISTER
V <
BID,5,,M       ;ID
>
F DMACCA,L      ;DMAC COMMAND ADDRESS REGISTER
F DMACID,L      ;DMAC ID REGISTER
V <
CID,5,,M       ;ID
>
F SBISILO,L     ; SBI silo register
F SBIERR,L      ; SBI error register
V <M
,8
ERRCONF,1      ; Error confirmation
,1
CTS,2          ; CPU timeout status
CTO,1          ; CPU timeout
>
F TMOADDRS,L    ; SBI timeout address
V <M
SBIA_ADR,28    ; Physical address
>
F SBISTS,L      ; SBI fault status
V <M
,16
SLOLCK,1       ; Silo lock
FAULT,1        ; SBI fault signal
FIE,1          ; Fault interrupt enable
FLTILA,1       ; Fault latch
,2
POPTY,1        ; P0 parity error
P1PTY,1        ; P1 parity error
,2
XMTR,1         ; Transmitted during fault
MLTPL,1        ; Multiple transmit fault
ISF,1          ; Interlock sequence fault
RDF,1          ; Unexpected read data fault
WSF,1          ; Write sequence fault
PTYFLT,1       ; Parity fault
>
F SILOCMP,L     ;SBI SILO COMPARATOR

```

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F MAINT,L
F UNJAM,L
F SBIQC,L
E

;SBI MAINTENANCE REG
;SBI UNJAM REGISTER
;SBI QUAD CLEAR

CL

```
;++
: STXCS -- Console storage control and status register definitions.
:--
```

```
$STRUCT STXCS
```

```
V<M
```

```
    FUNC,4
```

```
    2
```

```
    IE,1
```

```
    READY,1
```

```
    LBN,16
```

```
    STATUS,8
```

```
>
```

```
; Function.
```

```
; MBZ
```

```
; Interrupt enable.
```

```
; Ready bit.
```

```
; Logical block number of current xfer.
```

```
; Status.
```

```
: Function codes.
```

```
    C    NOP,0
```

```
    C    WRITEP,5
```

```
    C    READP,6
```

```
; No operation.
```

```
; Write physical block.
```

```
; Read physical block.
```

```
: Function/status codes.
```

```
    C    ABORT,3
```

```
    C    DEVSTAT,4
```

```
; Abort current transfer/transfer aborted.
```

```
; Read device status/status returned.
```

```
: Status codes.
```

```
    C    COMPLT,1
```

```
    C    CONT,2
```

```
    C    HNDERR,128
```

```
    C    HWERR,129
```

```
    E
```

```
; Transaction complete.
```

```
; Continue transaction.
```

```
; Handshake error during transaction.
```

```
; Hardware error during transaction.
```

```
;++  
: STXDB -- Console storage data byte register.  
:--
```

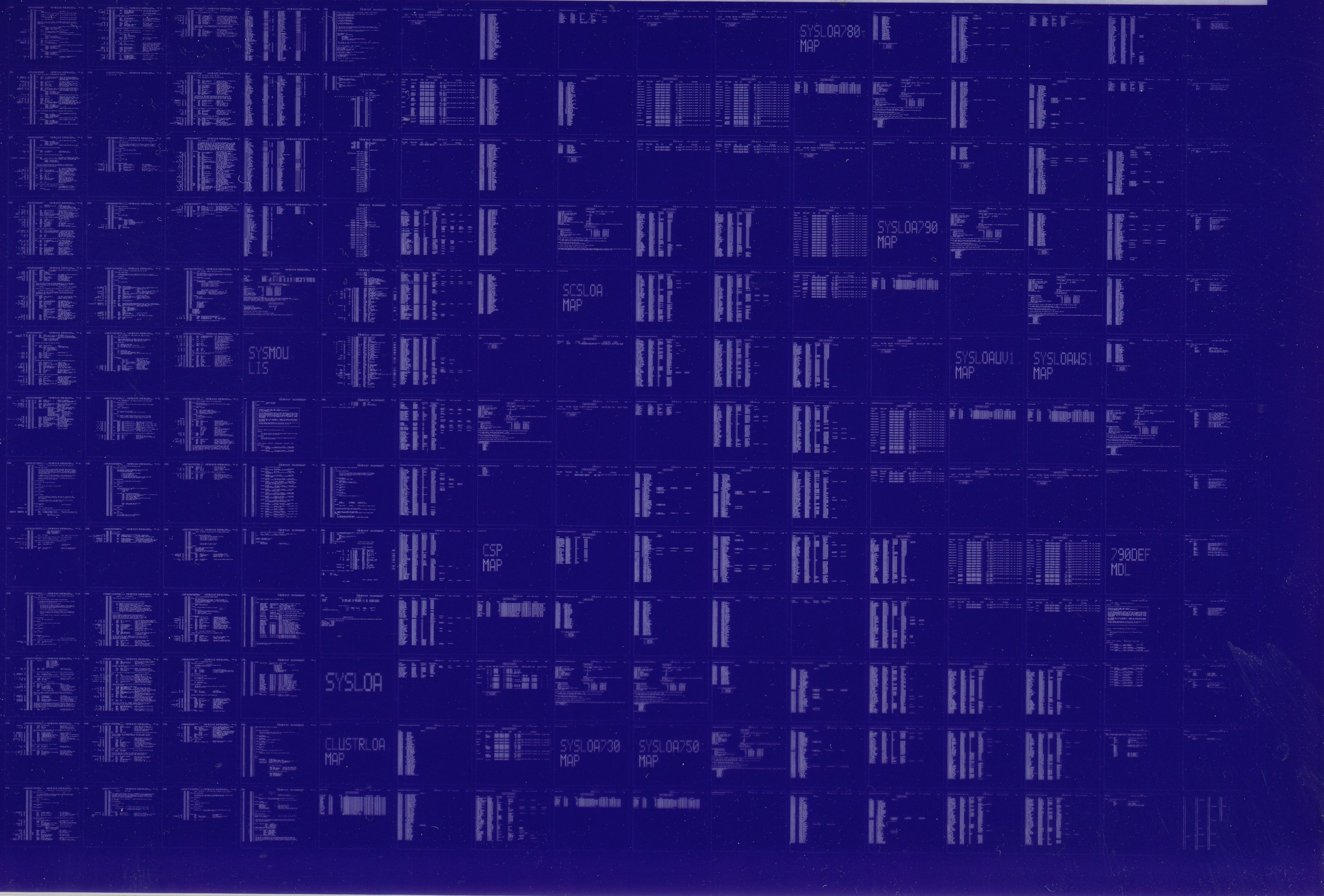
```
$STRUCT STXDB
```

```
V<M
```

```
DATA,16
```

```
; Word of data.
```

```
>  
E
```



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VAX/VMS V4.0

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