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CONTROL DATA CORPORATION

CDC® CYBER 180 COMPUTER SYSTEM MODELS 810 AND 830

VIRTUAL STATE

VOLUME I
SYSTEM DESCRIPTION
FUNCTIONAL DESCRIPTIONS

HARDWARE REFERENCE MANUAL

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New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV	PAGE	REV	PAGE	REV	PAGE	REV	PAGE	REV
Front Cover	A	I-2-21	A						
Title Page	A	I-2-22	A						
2	A	I-2-23	B						
3/4	B	I-2-24	B						
5	B	I-2-25	A						
6	B	I-2-26	A						
7	A	I-2-27	A						
8	A	I-2-28	A						
1-1-1	B	I-2-29	A						
1-1-2	B	I-2-30	A						
1-1-3	A	I-2-31	A						
1-1-4	A	I-2-32	A						
1-1-5	B	I-2-33	A						
1-1-6	B	I-2-34	A						
1-1-7	A	I-2-35	B						
1-1-8	A	I-2-36	A						
1-1-9	A	Comment Sheet	B						
1-1-10	B								
1-1-11	B								
I-2-1	A								
I-2-2	A								
I-2-3	A								
I-2-4	A								
I-2-5	A								
I-2-6	A								
I-2-7	A								
I-2-8	A								
I-2-9	A								
I-2-10	A								
I-2-11	B								
I-2-12	A								
I-2-13	A								
I-2-14	A								
I-2-15	A								
I-2-16	B								
I-2-17	A								
I-2-18	A								
I-2-19	A								
I-2-20	B								

PREFACE

This manual contains hardware reference information for the CDC® CYBER 180 Computer System Models 810 and 830 in their virtual states of operation.

This manual provides model-dependent information regarding the system description and functional descriptions of the computer systems' hardware. Additional systems' hardware information is available in manuals listed in the publication index on the following page.

AUDIENCE

This manual is for use by customer, marketing, and training personnel who want a general yet technical description of the computer system.

Other manuals applicable to the models 810 and 830 computer systems are:

Control Data Publication	Publication Number
CYBER 180 Computer Systems Models 810 and 830 Power Distribution and Warning System	60455210
CYBER 180 Computer Systems Models 810 and 830 CYBER 170 State Hardware Reference Manual	60469420
CYBER 180 Computer System Models 810 and 830 Hardware Operator's Guide	60458440
NOS/VE Operations Usage	60463914

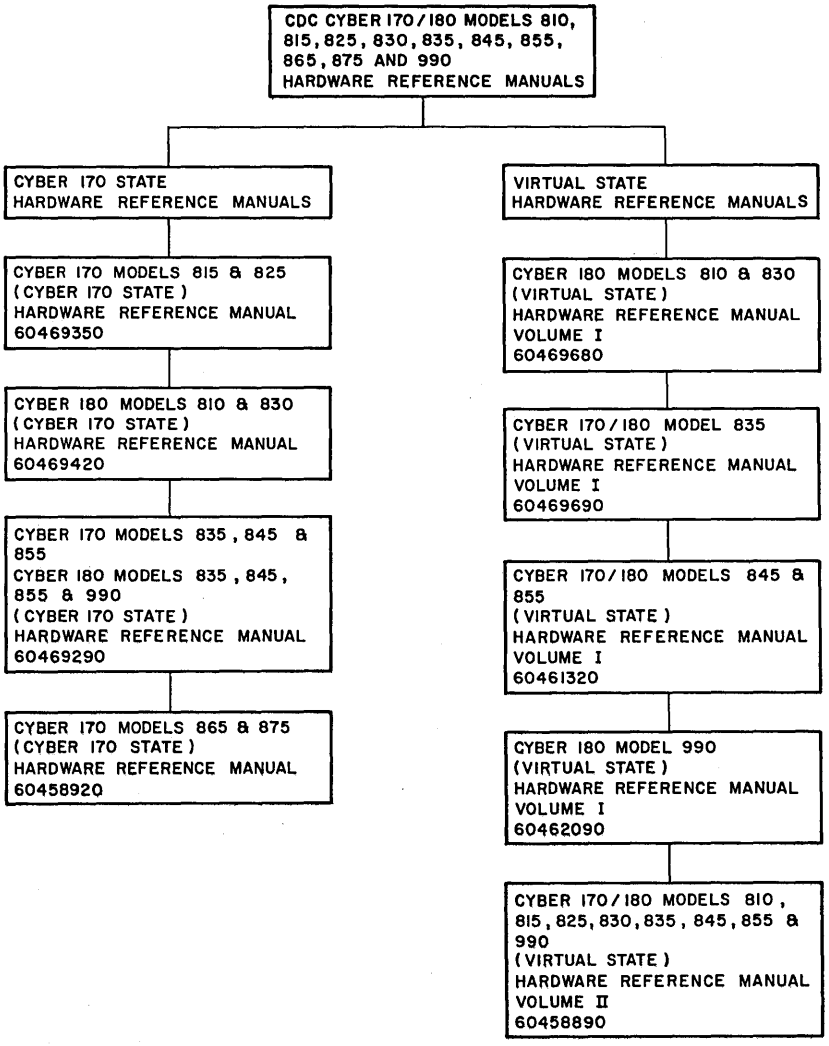
Publication ordering information and latest revision levels are available from the Literature Distribution and Services catalog, publication number 90310500.

This manual does not contain an index.

WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device persuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

PUBLICATION INDEX



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CONTENTS

1. SYSTEM DESCRIPTION I-1-1

Introduction I-1-1
Physical Characteristics I-1-2
Functional Characteristics I-1-2
CP General Functional Characteristics I-1-3
CP Virtual State Functional Characteristics I-1-3
Main Registers I-1-3
Processing Capabilities I-1-3
Modes of Operation and Interrupts I-1-4
Program Monitoring I-1-4
Access Protection I-1-4
Dual-CP System (Optional) I-1-5
CP CYBER 170 State Functional Characteristics I-1-5
CM Functional Characteristics I-1-5
IOU Functional Characteristics I-1-6
Major System Component Descriptions I-1-6
Central Processor I-1-6
Instruction Section I-1-7
Operand Issue Section I-1-7
Execution Section I-1-7
Map I-1-9
Business Data Processing (BDP) Section I-1-9
Maintenance Access Control (MAC) I-1-9
Central Memory (CM) I-1-10
Input/Output Unit (IOU) I-1-10
Display Stations I-1-11

2. FUNCTIONAL DESCRIPTIONS

CP Operating States I-2-1
Environment Interface (EI) I-2-1
Intrastate Modes Of Operation I-2-1
Virtual State Job Mode I-2-3
EI Operations in Virtual State Job Mode I-2-3
Virtual State Monitor Mode I-2-3
EI Operations in Virtual State Monitor Mode I-2-3
CYBER 170 State Job Mode I-2-3
CYBER 170 State Monitor Mode I-2-3
Mode Switching within CYBER 170 State I-2-4
Transferring from CYBER 170 State to Virtual State I-2-4
Dual-CP Operation I-2-4
Monitor Mode Operation I-2-5
Interrupt Handling I-2-5
Process Switching I-2-5
Job Mode Operation I-2-6
Central Processor (CP) I-2-7
Instruction Section I-2-7
Instruction Prefetch I-2-7
Instruction Decode and Initiation I-2-7
Interrupt Handling I-2-7
Operand Issue Section I-2-7
Process State Registers I-2-8
Operating Registers I-2-11
Interrupt-Handling Registers I-2-11
Processor State Registers I-2-16
Job Process State (JPS) Register I-2-16
Monitor Process State (MPS) Register I-2-17
Execution Section I-2-18
General Network I-2-18
Multiply/Divide Network I-2-18
Addressing Network I-2-19
Map Address Translation I-2-19
Map Access Validation I-2-19
Business Data Processing (BDP) Section I-2-20
Maintenance Access Control (MAC) I-2-20
Central Memory (CM) I-2-20
Address Format I-2-21
CM Access and Cycle Times I-2-22
CM Ports and Priorities I-2-22
SECDED I-2-22
CM Bounds Register I-2-24
CM Maintenance Registers I-2-24
CM Reconfiguration I-2-24
Virtual Memory I-2-25
Segments I-2-25
Pages I-2-25
Address Translation I-2-26
Access Protection I-2-28
Attributes I-2-29
Rings of Protection I-2-29
Keys and Locks I-2-29
Input/Output Unit I-2-29
Peripheral Processor I-2-30

Deadstart I-2-30
Barrel and Slot I-2-30
PP Registers I-2-31
A Register I-2-31
K Register I-2-31
P Register I-2-31
Q Register I-2-33
R Register I-2-33
PP Numbering I-2-33
PP Memory I-2-33
I/O Channels I-2-34
Display Station Controller I-2-34
Real-Time Clock I-2-34
Two-Port Multiplexer I-2-34
Maintenance Channel I-2-35
IOU Maintenance Registers I-2-35
Central Memory Access by PPs I-2-35

FIGURES

I-1-1 Models 810 and 830 Computer System I-1-1
I-1-2 Chassis Configuration, (Top Cutaway View) I-1-2
I-1-3 Models 810 and 830 Computer System Block Diagram I-1-8
I-2-1 Operating States Interaction I-2-2
I-2-2 Monitor Mode Request Processing in Dual-CP System I-2-6
I-2-3 Virtual State Exchange Package I-2-9
I-2-4 Interstate Exchange Package I-2-10
I-2-5 MCR and UCR Interrupt Mechanism I-2-14
I-2-6 JPS and MPS Functions in Exchange Operation I-2-17
I-2-7 Address Format for 12, 16 MB I-2-21
I-2-8 Segments in a Process I-2-26
I-2-9 Pages in a Segment I-2-27
I-2-10 Segment/Page Table Role in Address Translation I-2-28
I-2-11 IOU Barrel and Slot I-2-32

TABLES

I-2-1 Process State Registers I-2-11
I-2-2 Monitor Condition Register I-2-13
I-2-3 User Condition Register I-2-15
I-2-4 Processor State Registers I-2-16
I-2-5 Port Priority I-2-22
I-2-6 SECDED Syndrome Codes/ Corrected Bits I-2-23
I-2-7 CM Maintenance Registers I-2-24
I-2-8 IOU Maintenance Registers I-2-35

SYSTEM DESCRIPTION 1

This section introduces the CYBER 180 Computer System Models 810 and 830, identifies their physical and functional characteristics, and provides descriptions of the major system components.

INTRODUCTION

Models 810 and 830, shown in figure I-1-1, are medium scale, high-speed computer systems for both business and scientific applications. The systems include the following components:

- Central processor (CP)
- Central memory (CM)
- Input/output unit (IOU)
- Display Station (optional)

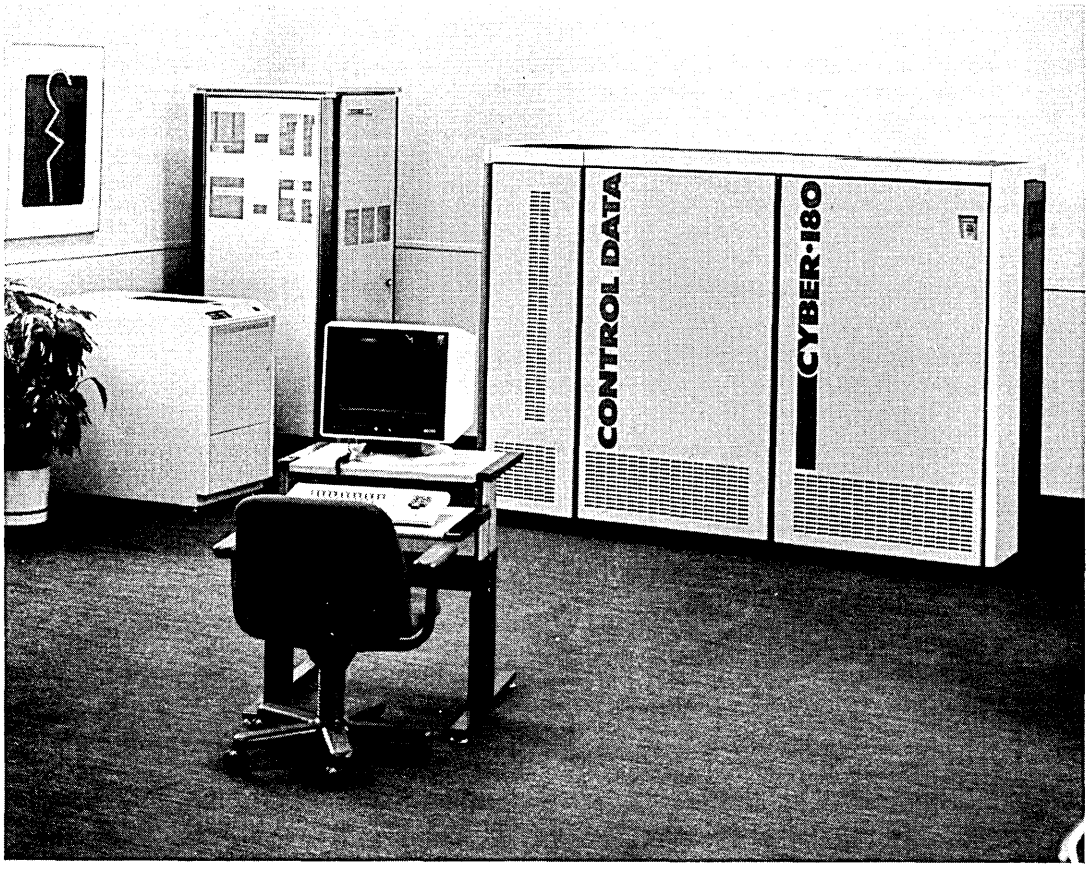


Figure I-1-1. Models 810 and 830 Computer System
(Display station is a required option.)

The system shown also includes a network processor unit (NPU, in the left corner), an intelligent small magnetic tape (ISMT, to the left of NPU), and an intelligent small disc (ISD, in the bolt-on cabinet left of the main cabinet), which are all system options.

PHYSICAL CHARACTERISTICS

The mainframe configuration, shown in figure I-1-2, includes a single three-section cabinet for the CP, CM, and IOU. The cabinet contains a logic chassis with plug-in circuit boards. The cabinet also contains fans to cool the logic chassis, an ac/dc control section with voltage margin testing facilities, and dc power supplies.

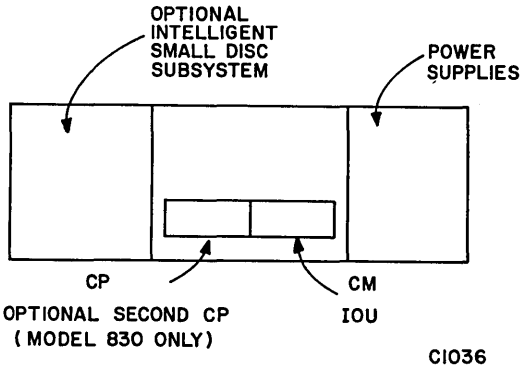


Figure I-1-2. Chassis Configuration, (Top Cutaway View)

FUNCTIONAL CHARACTERISTICS

To achieve high computation speeds, the computer systems use emitter-coupled logic (ECL). High speed is also the objective of the CP design. The CP design is based on the assumption that both instructions and data are, in most cases, accessed from successive memory locations. Accordingly, the CP prefetches instructions expected to be used next while the current instruction is being processed.

The CP supports two states of operation.

- Virtual State — Operation as a computer with virtual memory byte addressing, using the Virtual State instruction set and data formats. Virtual State is the native operating state of the CP.
- CYBER 170 State — Operation as a computer with real memory word addressing, using the CYBER 170 State CP instruction set and data formats.

The Virtual State and CYBER 170 State environments may be present at the same time with the CP executing in either environment. NOS/VE is the operating system of Virtual State; NOS is the operating system of CYBER 170 State.

The semiconductor memory is divided into two or four independent banks to minimize conflicts among central memory requests. These banks may all be simultaneously in the process of completing read and write requests. System input/output speeds are determined by the capabilities of existing external devices.

CP GENERAL FUNCTIONAL CHARACTERISTICS

The following CP characteristics are common to both Virtual State and CYBER 170 State:

- 50-nanosecond clock period
- Microprogram control
- Prefetch of next sequential instruction
- Separate arithmetic units for fixed-/floating-point binary and decimal data processing
- Hardware data format checking, conversion, and editing
- Parity checking on selected data and address paths

CP VIRTUAL STATE FUNCTIONAL CHARACTERISTICS

The following CP characteristics are exclusive to Virtual State.

Main Registers

The following CP registers hold most of the operands and addresses used for computational purposes:

- Sixteen 48-bit address (A) registers
- 64-bit program address (P) register
- Sixteen 64-bit operand (X) registers

Processing Capabilities

The CP processing capabilities have the following characteristics:

- 64-bit internal word (8 bytes)
- Packed instructions (16- and 32-bit instructions in 64-bit words)
- Integer arithmetic (32/64-bit operands)
- Floating-point arithmetic (12-bit exponent plus sign bit, 48/96-bit coefficient plus sign bit)

- Business data processing (11 decimal data types and an alphanumeric data type supported by move/compare/edit instructions)
- Call and return mechanism
- Load and store fields of one through eight bytes
- Extract and insert strings of 1 through 64 bits
- Load and store multiple address (A) and operand (X) registers
- Process immediate data from instruction word

Modes of Operation and Interrupts

The CP modes of operation and CP interrupt structure have the following characteristics:

- Monitor and job modes of operation
- Exchange instructions causing exchange of operating mode and executing process
- Trap interrupts on monitor mode conditions, with trap handled within present operating mode
- Trap interrupts on job mode conditions, with trap handled within present operating mode
- Exchange interrupts on job mode conditions, with an exchange to monitor mode for interrupt processing

Program Monitoring

CP program monitoring has five maskable classes of debug interrupts on up to 32 process virtual address ranges.

Access Protection

The CP security features include the following:

- Controlled access to segments which a process may access
- Fifteen rings of protection
- Segment locks and keys
- Eight types of segment access (read/write/execute with subdivisions)
- Controlled and protected entry points into shared code

Dual-CP System (Optional)

The dual-CP configuration has the following characteristics:

- Supports both Virtual State and CYBER 170 State operation
- Both CPs access a common queue of processes awaiting execution
- Both CPs share Virtual State monitor mode and its interrupt-handling routines

CP CYBER 170 STATE FUNCTIONAL CHARACTERISTICS

For CP characteristics exclusive to CYBER 170 State, refer to the CYBER 170 State Hardware Reference Manual listed in the Publication Index in the preface.

CM FUNCTIONAL CHARACTERISTICS

The CM has the following functional characteristics:

- 72-bit data word [64 data bits and 8 single-error correction double-error detection (SECDED) bits]
- Dynamic semiconductor memory, options available from 262K words (2MB) to 4192K words (32 Megabytes)
- Organization of two independent banks for 262K memory and four banks for larger memories
- Directly addressable process virtual address space of up to 4096 segments, with up to 2 billion bytes per segment
- System virtual address space of up to 65K segments
- Real memory page size ranging from 2K to 16K bytes
- Bounds register to limit write access
- 50-nanosecond clock period
- Maximum data transfer rate of one word every 100 nanoseconds
- 450-nanosecond read access time for model 830; 1250-nanosecond for model 810
- 400-nanosecond read/write cycle time for model 830; 1200-nanosecond for model 810
- 800-nanosecond partial-write cycle time for model 830; 1600-nanosecond for model 810
- SECDED CM data verification
- Parity checking on all major data, address, and control paths

IOU FUNCTIONAL CHARACTERISTICS

The IOU has the following functional characteristics:

- Ten peripheral processors (PPs). A 20-PP option is available. Each PP has a 4K independent memory (PPM) composed of 16-bit words. The PPs are compatible with CYBER 170 State PP instructions, data formats, and channels.
- Execution of 12- or 16-bit PP code.
- Port to central memory.
- Eight I/O channels (2-ICI/6-170 or 4-ICI/4-170) available to external devices, (1-ICI/3-170) options available for up to 16 channels (4-ICI/12-170 or 6-ICI/10-170).
- External interface to real-time clock, display controller, and two-port multiplexer.
- Bounds register controlling write access to CM.
- Parity checking on all major data and address paths.
- Maintenance channel giving PPs access to CP, CM, and IOU registers to perform system initialization and maintenance functions.
- Operating speed of 500 nanoseconds and a minor cycle of 50 nanoseconds.

MAJOR SYSTEM COMPONENT DESCRIPTIONS

The major system components are:

- Central processor (CP)
- Central memory (CM)
- Input/output unit (IOU)

The remainder of this section provides brief descriptions of the major system components. The descriptions relate to the computer system block diagram shown in figure I-1-3.

CENTRAL PROCESSOR

The CP consists of the following:

- Instruction section
- Operand issue section
- Execution section
- Map
- Business data processing (BDP) section
- Maintenance access control (MAC)

The CP is isolated from the input/output unit and is thus able to carry on computation or character manipulation unencumbered by I/O requirements.

Instruction Section

The instruction section directs the arithmetic and manipulative functions for instruction execution. Instruction section functions include:

- Initializing registers, controls, and memories
- Storing, accessing, decoding, and initiating a microprogram which controls CP operation in both CYBER 170 State and Virtual State
- Prefetching and disassembling instructions from CM
- Initiating interrupts when an error or exception condition occurs during an instruction execution

Operand Issue Section

The operand issue section contains the registers of the two CP register categories:

- Process state registers
- Processor state registers

These registers are located in the 256-word register file or throughout the hardware as various live registers.

The process state registers contain information related to the current process (job). This information includes operands and exchange package data required for instruction execution. These registers change upon the switching of processes. The 256-word register file contains the operating registers for instructions. These are the A, B, and X registers for CYBER 170 State instructions, and the A and X registers for Virtual State instructions. Refer to Process State Registers described under Operand Issue Section in section 2.

The processor state registers contain information related to the system and the CP hardware. The live registers are processor state registers which supply data for various operations and collect data from the CP operating environment. Refer to Processor State Registers described under Operand Issue Section in section 2.

Execution Section

The execution section consists of the arithmetic and logical network (ALN) and the addressing network. The ALN performs the logical, arithmetic, shift, and character manipulation functions for instruction execution and address formation. These functions include data formatting, positioning, testing, and comparison, plus data streaming control for BDP operations.

The ALN performs operations on values supplied by the operand issue section or, in some cases, the BDP section. The BDP section performs most BDP operations independently. All results return to the operand issue section except for exception conditions, which are sent to the instruction section to initiate interrupt handling.

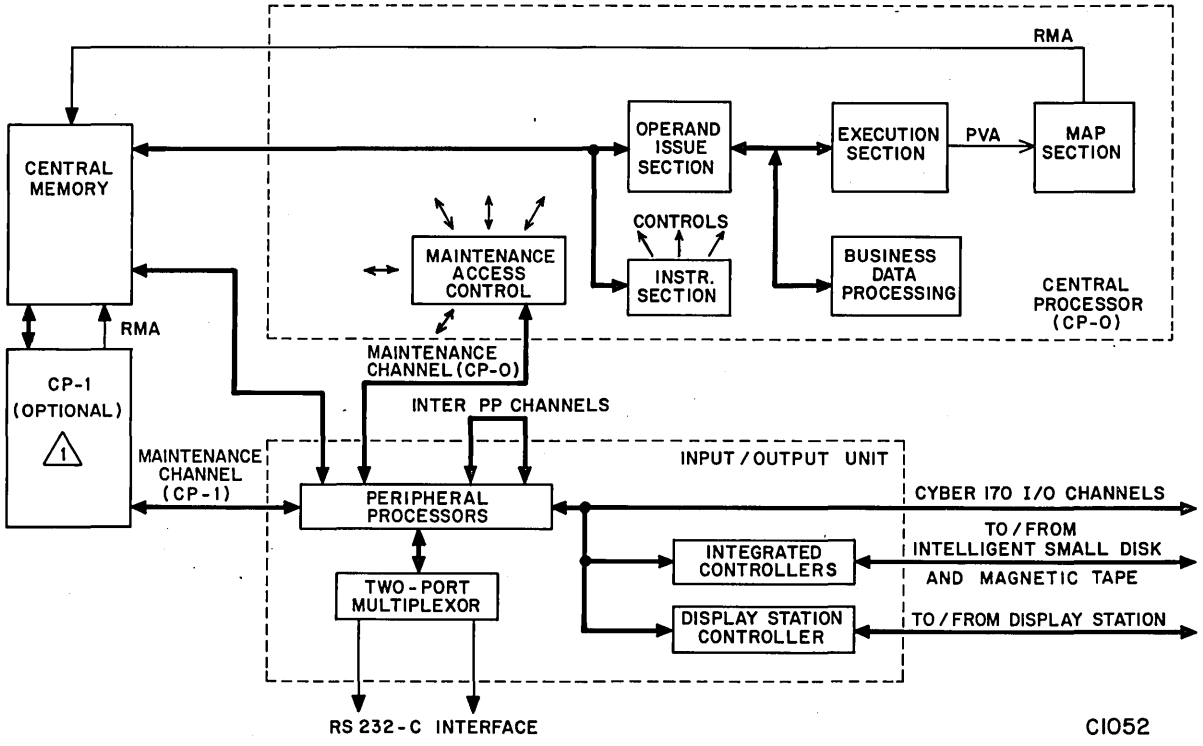


Figure I-1-3. Models 810 and 830 Computer System Block Diagram

The ALN consists of a general network and a multiply/divide network. The general network adds and subtracts integers and FP coefficients, as well as performing exponent arithmetic associated with all FP operations. It also performs Boolean, FP normalize, shift, and conditional branch test functions. The multiply/divide network forms Virtual State integer products and FP product coefficients for both CYBER 170 State and Virtual State.

The addressing network performs the following functions:

- Forms the byte number of addresses sent to CM for register file data or BDP stream data
- Provides controls for data streams from CM to the BDP section and vice versa
- Processes the load and store bit, byte, and word instructions

Map

Map contains the hardware to convert process virtual addresses (PVAs) to real memory addresses (RMAs).

To reduce CM access time, map contains up to 64 of the most recently used segment and page numbers and their corresponding page frame addresses (PFAs). If the segment and page numbers of the PVA match one of the segment and page numbers contained in map, map provides the corresponding PFA and forms the RMA. If there is no match, the execution unit performs the translation.

Map also performs all of the access validations for addressing memory. These include security ring tests, key and lock tests, and read/write/execute privilege validity tests.

Business Data Processing (BDP) Section

The BDP section performs BDP operations on 12 types of binary, alphanumeric, and decimal data. Although the BDP section performs most BDP operations independently, for some operations it may require processing assistance from the ALN in the execution section.

Maintenance Access Control (MAC)

The MAC performs initialization and maintenance operations. These operations, controlled by a dedicated peripheral processor in the IOU, include the following:

- Initialize registers, controls, and memories
- Communicate CP error and status information to the IOU when requested by a PP
- Read and write CP-resident registers and memories
- Read and write maintenance registers in all system components
- Reconfigure hardware
- Start and stop CP execution

The IOU sends codes to MAC to indicate the operations to be performed and the affected memory device, registers, and addresses.

CENTRAL MEMORY (CM)

The CM, shown in figure I-1-3, is a refresh-type metal-oxide semiconductor (MOS) memory organized into either two or four independent banks. Memory data words comprise 64 data bits plus 8 SECDED bits. The SECDED bits allow CM to correct single-bit failures and detect double-bit failures during a read operation before sending the data to the requesting unit. For double-bit failures, the CP logs the error and the system software determines corrective action.

The CM also controls the flow of data between CM and the requesting system components through multiple ports and, in addition, resolves port conflicts. The CM contains a distributor which multiplexes data from ports to CM. The distributor includes the error correction code (ECC) generator, SECDED, and partial-write logic.

The CM ports allow access to CM from:

- CP-0
- CP-1 (optional second CP)
- IOU

INPUT/OUTPUT UNIT (IOU)

The IOU, shown in figure I-1-3, consists of the following:

- Ten logically independent peripheral processors (PPs). An option is available to increase the total to 20 PPs.
- Internal interface to 12 I/O channels. An additional 12 channels are available in 6-channel increments.
- External interfaces to I/O channels.
  - 4, 6, 7, 9, 10, or 12 CYBER 170 channels
  - Display controller interface (radial) (channel 10_8)
  - Maintenance channel interface (radial) (channel 17_8)
  - Real-time clock interface (channel 14_8)
  - Two-port multiplexer interface (channel 15_8)
  - 2, 3, 4, 5, or 6 Integrated controller interfaces
- One port to central memory.
- Bounds register to limit writes to CM.

The PPs are organized in groups of ten, called barrels. The PPs in a barrel time-share common hardware. Each PP has its own 4K independent memory and communicates with all I/O channels and with central memory.

DISPLAY STATIONS

The optional display station, shown in figure I-1-1 and required for system operation, is a two-way communications facility between the system and the computer operator. Two types are available: the CC545 Display Station and the CC634B Display Station. Symbol and position information from the computer enables the display of program information on a cathode ray tube (CRT). The station also contains an alphanumeric keyboard which enables an operator to send data to the computer.

The keyboard and CRT combination permits the computer operator to monitor and control system operation. The computer outputs two alternate, nonrelated data streams. The operator can select either of the data streams or select both for presentation on the CRT. For further display station information, refer to Display Station Programming in Volume II, section 2, listed in the Publication Index in the preface.

FUNCTIONAL DESCRIPTIONS 2

This section describes the CP operating states, environment interface (EI), intrastate modes of operation, and dual-CP operation. It also provides functional descriptions of the central processor (CP), central memory (CM), and input/output unit (IOU). The CP, CM, and IOU functional descriptions relate to the block diagram shown in figure I-1-3. Functional descriptions for the cooling systems are in their respective manuals listed in the Publication Index in the preface.

CP OPERATING STATES

The CP supports two states of operation: Virtual State and CYBER 170 State. Virtual State uses the Virtual State instruction set and data formats. CYBER 170 State uses the CYBER 170 State instruction set and data formats.

As stated earlier, although Virtual State is the native operating state of the system, both environments may be present at the same time with the CP executing in either environment. Portions of Virtual State support and track CYBER 170 State operation. However, Virtual State is transparent to the CYBER 170 State operating system and any user jobs executing in the CYBER 170 State environment.

ENVIRONMENT INTERFACE (EI)

The EI is a Virtual State operating system routine that provides the interface between CYBER 170 State and Virtual State. EI directly supports the CYBER 170 State environment by simulating those portions of that environment not provided by the CP hardware.

The basic EI tasks include:

- Supporting system initialization and deadstart of the CYBER 170 State environment
- Simulating CYBER 170 State hardware and software error processing
- Processing Virtual State errors occurring in CYBER 170 State

Refer to Intrastate Modes of Operation for additional information on Virtual State EI operations.

INTRASTATE MODES OF OPERATION

Virtual State and CYBER 170 State each have two modes of execution: job mode and monitor mode. Job mode executes programmed sequences of instructions (jobs) in the CP. Monitor mode executes various operating system routines such as job sequencer, trap handler, and memory manager which control the loading, scheduling, executing, and outputting of user jobs. The monitor mode routines are always available to the CP when it requests any type of monitor mode intervention.

The CYBER 170 State environment exists within Virtual State job mode. The operating system supports this environment somewhat like a special purpose Virtual State job. CYBER 170 State has the characteristics of CYBER 170 computer system CPs. For detailed information on CYBER 170 State, refer to the appropriate CYBER 170 State Hardware Reference Manual listed in the preface.

The CP always operates in one of the following environments:

- Virtual State job mode
- Virtual State monitor mode
- CYBER 170 State job mode
- CYBER 170 State monitor mode

These four modes, plus specific EI operations, are briefly described in the following paragraphs. Figure I-2-1 shows the interaction among operating states, intrastate modes of operation, and EI.

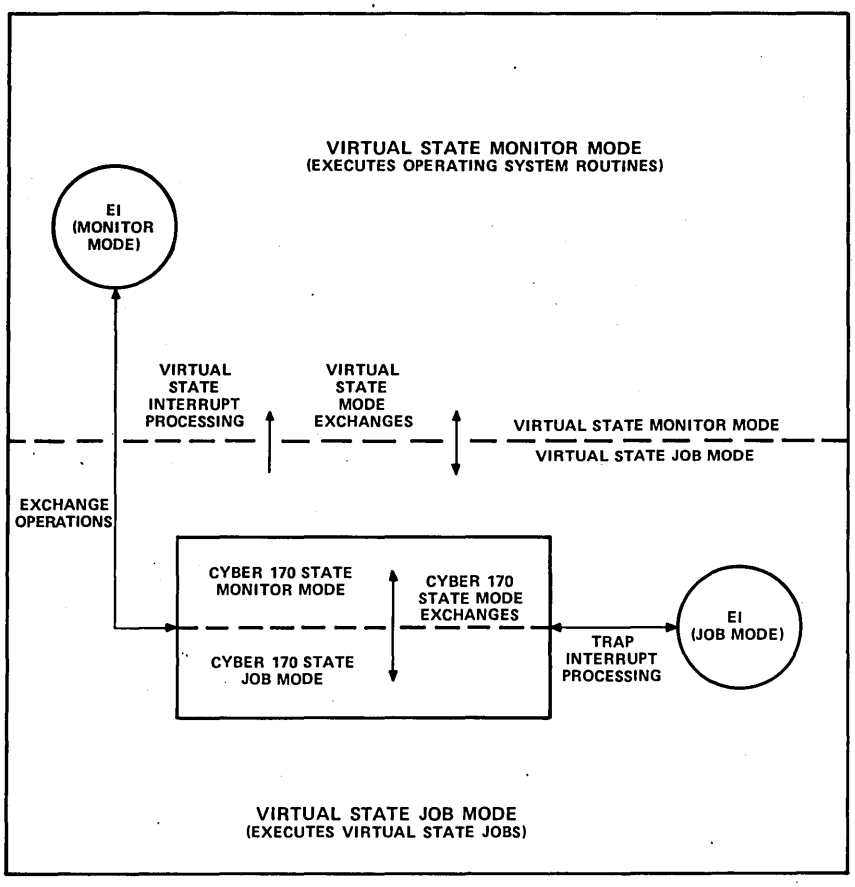


Figure I-2-1. Operating States Interaction

VIRTUAL STATE JOB MODE

Virtual State job mode executes programmed sequences of Virtual State instructions in the CP. While in Virtual State job mode, exchange iterrupts or an exchange instruction cause an exchange to Virtual State monitor mode.

CYBER 170 State monitor and job modes exist within Virtual State job mode. Refer to the corresponding headings in this section for further detail.

EI Operations in Virtual State Job Mode

EI operations occur in both Virtual State job and monitor modes. Monitor mode operations are described under Virtual State Monitor Mode. The primary EI job mode task is to perform CYBER 170 State interrupt processing, which comprises:

- Simulating CYBER 170 State error exit conditions.
- Trapping from CYBER 170 State to routines in Virtual State job mode that:
  - Ready the CP for transition from Virtual State to CYBER 170 State
  - Transfer blocks of CM or UEM words either within the CYBER 170 State environment or between operating states

VIRTUAL STATE MONITOR MODE

Virtual State monitor mode executes operating system routines that perform Virtual State monitor activities. This mode performs exchange and trap interrupt processing, simulates certain CYBER 170 State instructions, executes restricted CP instructions, and processes hardware and software errors detected in both Virtual State and CYBER 170 State.

EI Operations in Virtual State Monitor Mode

The primary EI monitor mode task is to perform exchange operations within CYBER 170 State if hardware or software errors are detected in CYBER 170 State job or monitor mode.

CYBER 170 STATE JOB MODE

CYBER 170 State job mode executes programmed sequences of CYBER 170 State instructions in the CP. This mode, along with CYBER 170 State monitor mode, exists within Virtual State job mode.

CYBER 170 STATE MONITOR MODE

CYBER 170 State monitor mode executes operating system routines that perform CYBER 170 State monitor activities.

Mode Switching Within CYBER 170 State

Within CYBER 170 State, switching between monitor mode and job mode does not require an exchange to Virtual State monitor mode. This transition may be caused by:

Job-to-monitor	PP-directed CYBER 170 State exchange request
	CYBER 170 State exchange jump instruction
	Hardware or conditional software error
Monitor-to-job	CYBER 170 State exchange jump instruction

Transferring from CYBER 170 State to Virtual State

The following CP conditions cause a transfer (exchange or trap) to Virtual State from CYBER 170 State monitor or job mode:

- Explicit trap instruction (trap)
- Conditional software error in CYBER 170 State monitor mode (exchange)
- Illegal instruction in CYBER 170 State monitor mode (exchange)
- Virtual State errors detected in CYBER 170 State monitor or job mode (exchange)

For further information, refer to Exception Handling in CYBER 170 State in volume II, section 2, listed in the Publication Index in the preface.

DUAL-CP OPERATION

Both the NOS and NOS/VE operating systems support a second, identical CP as an option for Model 830. CP-0 and the optional CP-1 operate independently; neither manages the other. The dual-CP configuration has the following characteristics:

- CP-1 operates identically to CP-0, executing the entire Virtual State instruction set independently.
- The CPs share central memory but translate virtual addresses and access CM independently.
- The CPs maintain separate maps.
- The CPs share Virtual State monitor mode and its interrupt-handling routines.
- The CPs access a common process queue for process dispatching.

The implementation of dual CPs requires some monitor and job mode constraints so that the CPs operate free of conflicts.

MONITOR MODE OPERATION

Virtual State monitor mode services requests from both CPs, but monitor mode is unaware of an additional CP in the system. The operating system provides a convention for servicing either CP's monitor mode requests in an orderly, nonconflicting fashion.

When either CP requests monitor mode intervention, the operating system determines whether the request is for interrupt handling or process switching and proceeds accordingly with request processing.

INTERRUPT HANDLING

Interrupt handling in a dual-CP system is identical to a single-CP system: the CPs exchange and execute independently in job or monitor mode without interference. However, if the CPs issue concurrent monitor mode requests, a software convention determines how these requests are processed. For more information, refer to figure I-2-2. This convention:

- Assigns a monitor request code (MRC) to each request from either CP.
- Establishes groupings of MRCs (request groups) that are associated with specific sets of monitor mode routines (request processors). Each request group has its own request processor.

Assigning a request processor to a request group allows the monitor mode interrupt handler to simultaneously process unlike requests (as indicated by unlike MRCs). If the CPs issue concurrent requests which must be handled by the same request processor, monitor mode forces an interlock on one CP until the request processor is available. However, if the CPs issue concurrent requests which can be handled by different request processors, monitor mode can process both requests simultaneously.

Whenever there are successive requests for the same request processor, monitor mode serializes such requests and executes them when the request processor is available. Some requests never require interlocks; monitor mode processes these as though the process issued a specific request.

PROCESS SWITCHING

Process switching in a dual-CP configuration occurs when one process has executed beyond its execution interval or process execution has completed. Monitor mode maintains a collection of task tables describing the state of each process active in the system. A CP request for process switching references the task tables to select a new process from the process queue common to both CPs. The CP then exchanges to job mode to execute it.

Monitor mode's process-switching routine provides an additional tag to prevent both CPs from simultaneously selecting the same process from the common process queue. The tag, maintained in the task tables, shows which processes are executing and which are ready to execute.

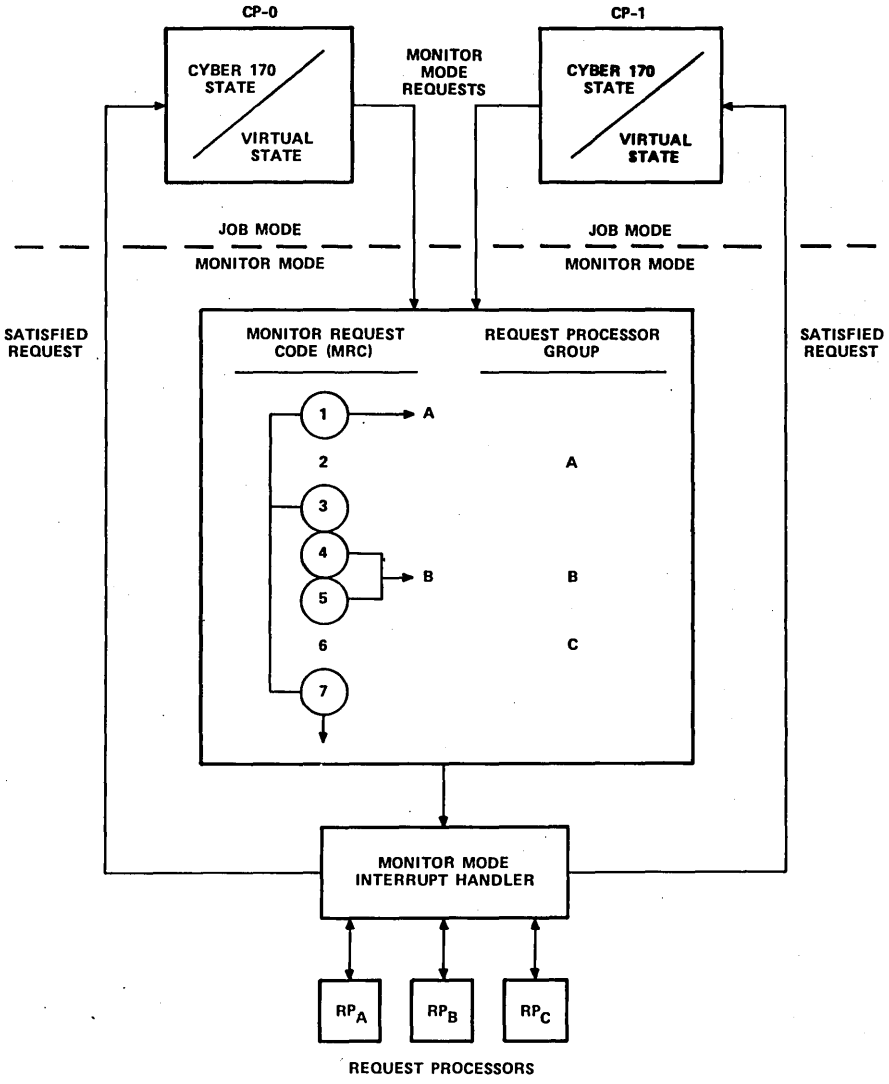


Figure I-2-2. Monitor Mode Request Processing in Dual-CP System

JOB MODE OPERATION

The dual-CP configuration places few restrictions on job mode operation. These restrictions include the following:

- The operating system ensures that processes do not reference or update exchange packages of other processes.
- Because the dual-CP configuration requires fast CP-to-CP communication for page table maintenance, traps in monitor mode must not be disabled frequently or for an extended period of time.

CENTRAL PROCESSOR (CP)

The CP consists of the instruction section, operand issue section, execution section, map section, business data processing (BDP) section, and maintenance access control (MAC).

INSTRUCTION SECTION

The instruction section consists of logic for instruction prefetch, decode, and initiation. To implement the CYBER 170 State and Virtual State instruction sets, the instruction section initiates microprogram sequences that obtain instruction operands and provide the control signals for execution. It also performs CP interrupt handling by initiating an interrupt-handling routine when an error or exception condition occurs while an instruction is executing.

Instruction Prefetch

To improve instruction flow, the instruction section prefetches a maximum of 8 instructions from CM to make the next instruction immediately available when the previous instruction completes execution. This occurs by reading instructions from CM into a series of buffer ranks.

Instruction Decode and Initiation

In CYBER 170 State, instruction words contain from one to four instructions. In Virtual State, instruction words read from CM contain from two to four instructions combined in a parcel arrangement. The instruction section decodes the CM instruction word into its separate instructions and issues control information to functional units in the execution section to start instruction execution.

In CYBER 170 State, a two-parcel instruction is not permitted to cross a word boundary; in Virtual State it is permitted. During Virtual State BDP operations, one- or two-parcel BDP descriptors follow the instruction parcels through execution.

Interrupt Handling

The instruction section can initiate an interrupt-handling routine when an error or exception condition occurs while an instruction is executing. The error/exception conditions are a combination of stackable or unstackable conditions, allowing the instruction section to interrupt selectively.

The error and exception conditions accumulate in the monitor and user condition registers (refer to the description under Operand Issue Section). The instruction section examines the error/exception inputs to determine the type of interrupt. It then addresses the appropriate interrupt-handling routine in monitor mode.

OPERAND ISSUE SECTION

The operand issue section consists of the process state and processor state registers, which are located in the 256-word register file or throughout the CP hardware as various live registers.

The 256-word register file contains the operating registers for CYBER 170 State and Virtual State instructions. These operating registers are A, B, and X for CYBER 170 State, and A and X for Virtual State. The register file also holds other exchange package information and provides holding registers for intermediate results.

The live registers contain control information for various CYBER 170 State and Virtual State CP operations. The CP uses the constant output of the live registers during on-line operations. The live registers give the CP access to exchange package information which otherwise would have to be obtained from the register file.

Some of the live registers are writable under microprogram control but copies which are maintained in the register file may also be read. These registers typically contain control information rather than data. Normally they are loaded from an exchange package at the same time that exchange package enters the register file from central memory. Other live registers are read-only registers under microprogram control. The contents of these registers change as a result of changes in the CP hardware environment. These changes typically impact system operation and require monitoring.

All register-file registers and live registers are either process state or processor state registers. This distinction arises because the state of the process and the state of the processor characterize CP operation. The contents of the process state registers can be written into memory as a Virtual State exchange package for either a Virtual State process or a CYBER 170 State process. Figures I-2-3 and I-2-4 show the respective exchange packages. For detailed information on exchange packages and state-switching operations, refer to Interstate Programming in volume II, section 2, listed in the Publication Index in the preface.

The principal registers of each category are described in the following paragraphs. For detailed functional descriptions of the remaining registers, refer to CP Registers in volume II, section 2, listed in the Publication Index in the preface.

Process State Registers

The process state registers relate to a specific Virtual State process executing in the CP. Various process state registers also support CYBER 170 State operation. The exchange package for each process contains the step-by-step operating register contents as directed by that process's execution. In addition, the exchange package holds other detailed process state information such that the CP may dynamically switch between exchange packages (processes) while preserving process integrity.

When a process executes in the CP, its exchange package resides in the process state registers. When a process awaits execution, its exchange package resides in central memory. The process state registers include the following:

- Operating Registers
  - Sixteen 48-bit address (A) registers, numbered A0 through AF
  - Sixteen 64-bit operand (X) registers, numbered X0 through XF
- Interrupt-handling Registers
  - Monitor condition register (MCR) and monitor mask register (MMR), (16 bits each)
  - User condition register (UCR) and user mask register (UMR), (16 bits each)
- Additional Process State Registers

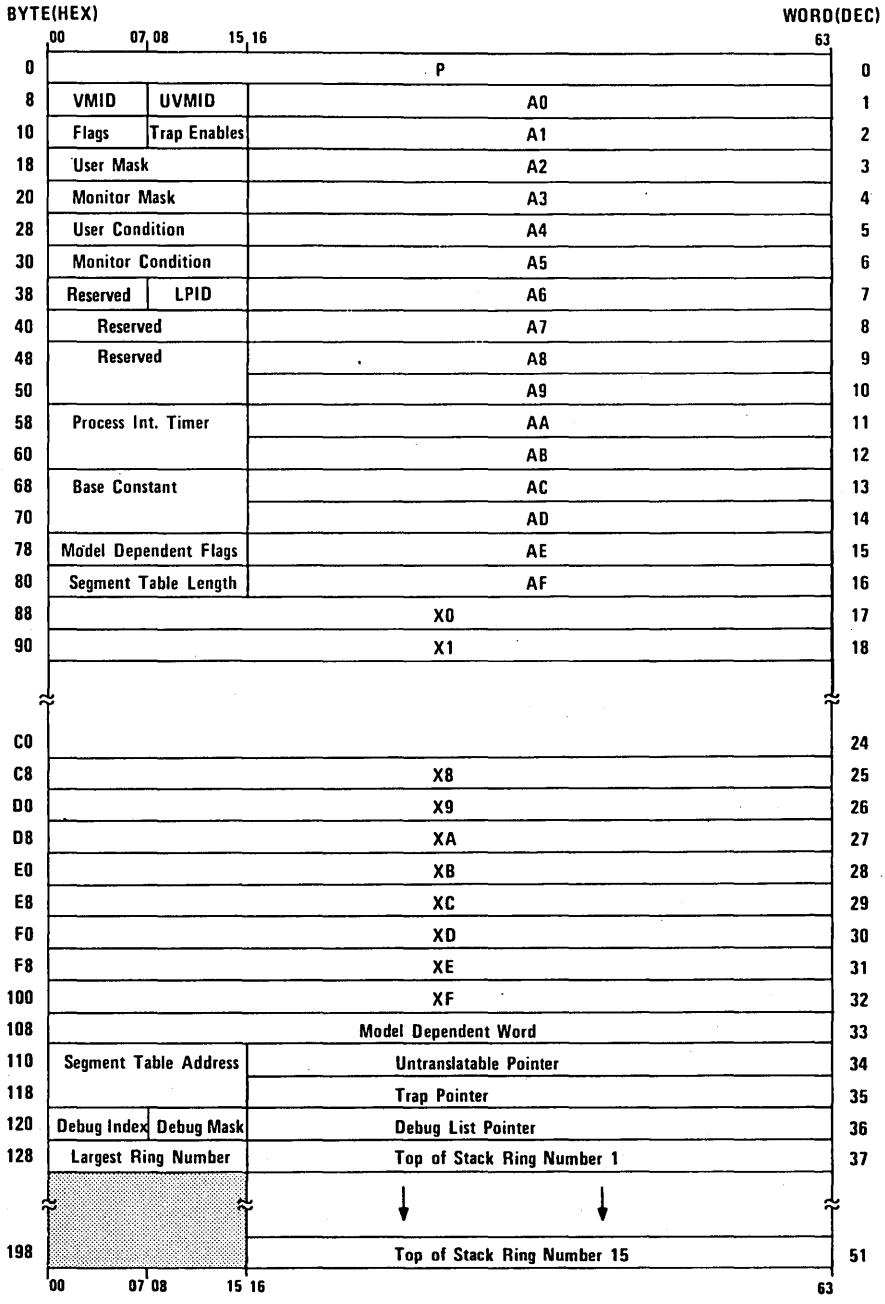
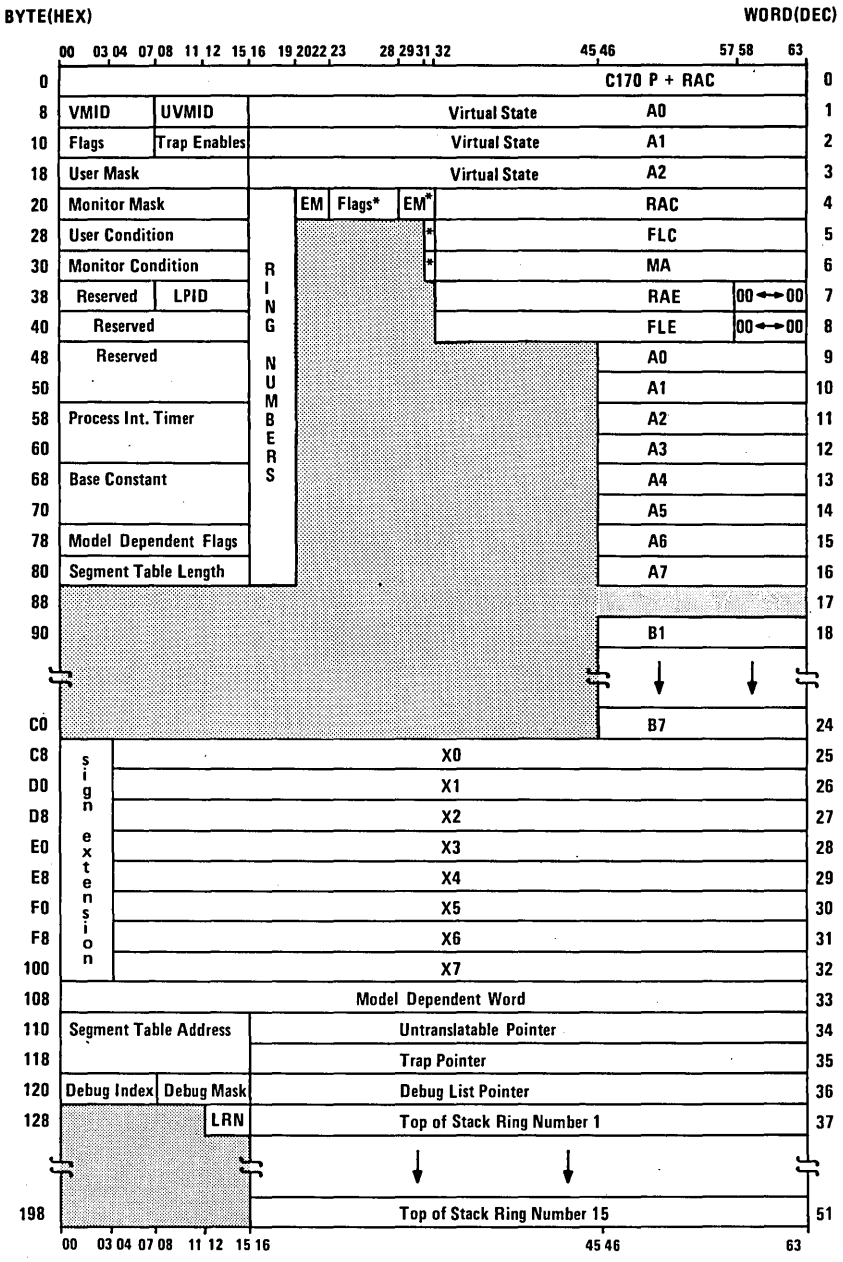


Figure I-2-3. Virtual State Exchange Package



* Flags:

Bit 23, Word 4	UEM Enable Flag
Bit 24, Word 4	Expanded Addressing Select Flag (ESM Mode Flag)
Bit 25, Word 4	Extended Block Copy Flag
Bit 26, Word 4	Software Flag
Bit 27, Word 4	Instruction Stack Purge Flag
Bit 28, Word 4	Software Flag
Bit 29, Word 4	EM-Indefinite Operand
Bit 30, Word 4	EM-Infinite Operand
Bit 31, Word 4	EM-Address out of Range
Bit 31, Word 5	C170 Monitor Flag
Bit 31, Word 6	Exit Mode Halt

Figure I-2-4. Interstate Exchange Package

Refer to table I-2-1 for a complete listing of the process state registers. The principal process state registers are described in this section. The remaining process state registers are described under CP Registers in volume II, section 2, listed in the Publication Index in the preface.

Table I-2-1. Process State Registers

Register Name		Register Name	
Address Base constant (BC) Debug index (DI) Debug list pointer (DLP) Debug mask (DM) Flags Critical frame (CFF) On condition (OCF) Process not damaged (PND) Largest ring number (LRN) Last processor identification (LPID) Monitor condition (MCR) Monitor mask (MMR) Operand		Process interval timer (PIT) Program address (P) Segment table address (STA) Segment table length (STL) Top-of-stack pointer Trap enables (TE) Trap pointer (TP) Untranslatable pointer (UTP) Untranslatable virtual machine identifier (UVMID) User condition (UCR) User mask (UM) Virtual machine identifier (VMID)	

Operating Registers

The operating registers consist of the address (A) and operand (X) registers, which minimize memory references for arithmetic operands and results.

The time that an exchange package resides in CP hardware is called an instruction interval. During this interval, the operating register contents can be changed by CP instructions. The other process state registers change only as a result of an exchange jump, copy-to-state-register instruction, or branch-on-condition-register instruction.

Address (A) Registers - The A registers are primarily CM operand address registers which contain process virtual address (PVAs).

Operand (X) Registers - The X registers are primarily data-handling registers for computation. Depending on the operation, the registers contain a logical quantity, a signed binary integer, or a signed floating-point number. Operands and results transfer between CM and the X registers.

Interrupt-Handling Registers

The monitor condition and user condition registers, and the associated monitor mask and user mask registers, provide the CP interrupt structure. These registers detect interrupt conditions which cause any of the following CP responses:

Exchange — An exchange interrupt switches CP execution to a monitor mode interrupt-handling routine after an inter-mode exchange occurs. An exchange can only be caused by an interrupt condition occurring in job mode. Monitor (system) conditions cause nearly all exchange interrupts; exceptions are user (process) conditions that occur with traps disabled.

Halt — The CP halts and the IOU takes steps to resolve the problem.

Stack — The CP records the condition but temporarily defers processing of the interrupt.

Trap — A trap interrupt switches CP execution to another section of code in the same address space as the executing process. It does not cause an exchange of processes and may occur in both job and monitor modes. A trap triggers from the occurrence of a certain process interrupt condition. The trapped-to code executes a specific routine that resolves the interrupt and returns control to the process.

These responses to MCR and UCR interrupts depend on whether traps are enabled or disabled and what the current operating mode is when the interrupt occurs.

The CP usually runs with traps enabled. Traps are disabled to keep them from occurring when certain sections of code are executing. In monitor mode, traps are disabled to prevent interrupts caused by the operating system or peripheral devices. In job mode, traps are disabled to prevent trap interrupts from interrupting the execution of job mode trap-handling routines. Traps caused by monitor conditions can interrupt these trap-handling routines even if traps are disabled.

CP interrupt responses characteristic of the operating mode are described under Monitor Condition Register (MCR) and User Condition Register (UCR) later in this section.

Monitor Condition Register (MCR) - The MCR provides the CP interrupt structure for interrupt conditions which must be serviced by monitor mode. The MCR contains 16 bits, each of which records a different interrupt condition in the CP. The MCR conditions are of higher priority and are processed before the UCR conditions.

The MCR conditions include:

- Hardware errors
- Major software errors
- Addressing and security errors in CP or CM
- Page faults

The specific MCR conditions and corresponding CP responses are listed in table I-2-2, and described in detail under CP Interrupts in volume II, section 2, listed in the Publication Index in the preface.

An MCR bit set in job mode with traps enabled or disabled causes an exchange to a monitor mode to execute an interrupt-handling routine. This routine analyzes the error and determines corrective action. An MCR bit set in monitor mode with traps enabled transfers control to a trap-handling routine within monitor mode. An MCR bit set in monitor mode with traps disabled causes the CP to stack the condition or halt, depending on the condition.

Each bit in the MCR has an associated mask bit in the MMR. The 16 mask bits allow selective processing of MCR interrupts.

Monitor Mask Register (MMR) - The MMR contains 16 bits, each of which is a mask bit associated with a specific MCR condition. The mask bits control interrupt response when a corresponding MCR bit sets. (At certain times during program execution, it may be necessary to defer processing of specific MCR conditions. For example, when executing in CYBER 170 State, the CYBER 170 State exchange request (MCR bit 53) from Virtual State should not be processed and stacks until execution of the previous CYBER 170 State process terminates.

Table I-2-2. Monitor Condition Register

P RGTR	BIT NUMBER AND DEFINITION			ASSOCIATED MONITOR MASK REGISTER BIT SET				MASK BIT CLEAR
				TRAP ENABLED		TRAP DISABLED		TRAP ENABLED OR DISABLED
				JOB MODE	MONITOR MODE	JOB MODE	MONITOR MODE	JOB OR MONITOR MODE
–	48	Detected Uncorrectable Error	Mon	EXCH	TRAP	EXCH	HALT	HALT
–	49	Unassigned		EXCH	TRAP	EXCH	HALT	HALT
P+	50	Short Warning	Sys	EXCH	TRAP	EXCH	STACK	STACK
P	51	Instruction Specification Error	Mon	EXCH	TRAP	EXCH	HALT	HALT
P	52	Address Specification Error	Mon	EXCH	TRAP	EXCH	HALT	HALT
P+	53	170 Exchange Request	Sys	EXCH	TRAP	EXCH	STACK	STACK
P	54	Access Violation	Mon	EXCH	TRAP	EXCH	HALT	HALT
P	55	Environment Specification Error	Mon	EXCH	TRAP	EXCH	HALT	HALT
	56	External Interrupt	Sys	EXCH	TRAP	EXCH	STACK	STACK
	57	Page Table Search Without Find	Mon	EXCH	TRAP	EXCH	HALT	HALT
	58	System Call	Status - This bit is a flag only and does not cause any hardware action.					
P+	59	System Interval Timer	Sys	EXCH	TRAP	EXCH	STACK	STACK
P/P+*	60	Invalid Segment/Ring Number Zero	Mon	EXCH	TRAP	EXCH	HALT	HALT
P	61	Outward Call/Inward Return	Mon	EXCH	TRAP	EXCH	HALT	HALT
P+	62	Soft Error Log	Sys	EXCH	TRAP	EXCH	STACK	STACK
–	63	Trap Exception	Status - This bit is a flag only and does not cause any hardware action.					

* P, unless P+ for RNO on loads

All MMR bits are set if no masking of interrupts is desired. Clearing an MMR bit masks its corresponding interrupt condition in the MCR. The CP Copy-to-State-Register instructions are used to set and clear specific MMR bits. Refer to volume II, section 1, listed in the Publication Index in the preface.

The MCR is normally all zeros. An interrupt condition sets the appropriate MCR bit. The CP performs a logical product (AND) of the 16 MCR and MMR bits. Refer to figure I-2-5. If the corresponding MMR bit is set (unmasked), an interrupt or trap occurs depending on whether the process is in Virtual State job mode or monitor mode. If the corresponding MMR bit is clear (masked), the CP either halts or stacks the condition and processes the interrupt later when the mask bit sets.

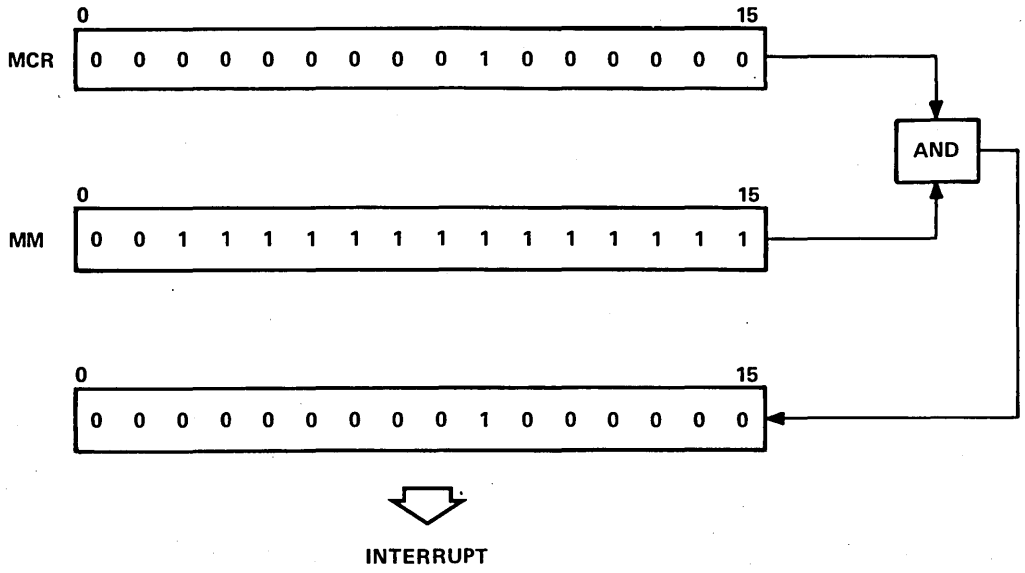


Figure I-2-5. MCR and UCR Interrupt Mechanism

User Condition Register (UCR) - The UCR provides the CP interrupt structure for conditions which relate primarily to instruction execution, and which do not require monitor mode intervention. The UCR contains 16 bits which, like the MCR, record different interrupt conditions in the CP. The UCR conditions include:

- Execution errors
- Arithmetic errors
- Invalid data
- Invalid instructions

The specific UCR conditions are listed in table I-2-3 and described in detail under CP Interrupts in volume II, section 2, listed in the Publication Index in the preface.

A UCR bit set in job or monitor mode with traps enabled causes a trap to a trap-handling routine within the address space of the process. A UCR bit set in job or monitor mode with traps disabled generally causes the CP to stack the condition. For the monitor-type conditions grouped within the UCR, an interrupt in job mode causes an exchange to monitor mode to execute an interrupt-handling routine, and an interrupt in monitor mode halts the CP.

Each bit in the UCR has an associated mask bit in the (UMR). The 16 mask bits allow selective processing of UCR interrupts.

Table I-2-3. User Condition Register

P RGTR	BIT NUMBER AND DEFINITION			ASSOCIATED USER MASK REGISTER BIT SET				MASK BIT CLEAR
				TRAP ENABLED		TRAP DISABLED		TRAP ENABLED OR DISABLED
				JOB MODE	MONITOR MODE	JOB MODE	MONITOR MODE	JOB OR MONITOR MODE
P	48	Privileged Instruction Fault	Mon	TRAP	TRAP	EXCH	HALT	These mask bits are permanently set.
P	49	Unimplemented Instruction	Mon	TRAP	TRAP	EXCH	HALT	
P	50	Free Flag	User	TRAP	TRAP	STACK	STACK	
P+	51	Process Interval Timer	User	TRAP	TRAP	STACK	STACK	
P	52	Inter-ring Pop	Mon	TRAP	TRAP	EXCH	HALT	
P	53	Critical Frame Flag	Mon	TRAP	TRAP	EXCH	HALT	
–	54	Reserved	User	–	–	–	–	
P	55	Divide Fault	User	TRAP	TRAP	STACK	STACK	STACK
P	56	Debug	User	TRAP	TRAP	STACK	STACK	STACK
P	57	Arithmetic Overflow	User	TRAP	TRAP	STACK	STACK	STACK
P+	58	Exponent Overflow	User	TRAP	TRAP	STACK	STACK	STACK
P+	59	Exponent Underflow	User	TRAP	TRAP	STACK	STACK	STACK
P+	60	F. P. Loss of Significance	User	TRAP	TRAP	STACK	STACK	STACK
P	61	F. P. Indefinite	User	TRAP	TRAP	STACK	STACK	STACK
P	62	Arithmetic Loss of Significance	User	TRAP	TRAP	STACK	STACK	STACK
P	63	Invalid BDP Data	User	TRAP	TRAP	STACK	STACK	STACK

User Mask Register (UMR) - The UMR contains 16 bits which, like the MMR, are mask bits associated with specific UCR conditions. The mask bits control interrupt action when a corresponding UCR bit sets. At certain times during program execution, it may be necessary or desirable to defer processing of specific UCR conditions. For example, when testing and debugging a new program, it may be desirable to disable interrupts caused by out-of-range arithmetic results, UCR bit 57.

All UMR bits are set if no masking of interrupts is desired. Clearing a UMR bit masks its corresponding interrupt condition in the UCR. The CP copy instruction is used to set/clear specific UMR bits. Refer to CP Copy Instructions in volume II, section 1, listed in the Publication Index in the preface.

The UCR is normally all zeros. An interrupt condition sets the appropriate UCR bit. The CP performs a logical product (AND) of the 16 UCR and UMR bits. Refer to figure I-2-5. If the corresponding UMR bit is set (unmasked), an interrupt occurs. If the UMR bit is clear (masked), the CP stacks the condition and processes the interrupt later when the mask bit sets. Certain UCR conditions, shown in table 1-2-3, require direct attention and cannot be masked.

Additional Process State Registers - The remaining process state registers are accessible to the CP and the PPs. Several of these registers are used by software for program debugging. Registers also exist to assist the translation from a virtual address to an address used to access data from central memory. These registers are listed in table I-2-3, and described in detail under CP Registers in volume II, section 2, listed in the Publication Index in the preface.

Processor State Registers

The processor state registers contain information about the state of the CP hardware rather than a unique process. This group of registers comprises maintenance registers and other various processor state registers. Refer to table I-2-4.

The maintenance registers provide information about the condition of CP hardware. In some cases, they can be set to force faults in the CP to verify the integrity of the fault detection hardware. The other processor state registers contain pointers/parameters of tables and exchange packages in CM. All processor state registers are accessible to the CP and to the PPs. These registers change only as a result of an exchange jump, if at all. Some may also change under monitor-mode control.

The principal processor state registers are described in this section. The remaining processor state registers are described under CP Registers in volume II, section 2, listed in the Publication Index in the preface.

Table I-2-4. Processor State Registers

Register Name		Register Name	
Dependent Environment Control (DEC) Element Identification (EI) Job Process State (JPS) Monitor Process State (MPS) Options Installed (OI) Page Size Mask (PSM) Page Table Address (PTA) Page Table Length (PTL)		Processor Fault Status (PFS)* Processor Identification (PI) Processor Test Mode (PTM)* Status Summary (SS) System Interval Timer (SIT) Virtual Machine Capability List (VMCL)	
* Processor model-dependent (refer to CP Registers in volume II, section 2, listed in the Publication Index in the preface).			

Job Process State (JPS) Register

The JPS register holds the real memory address of the first entry in an exchange package in CM. This address indicates where a job's process state registers are:

- Stored in CM in a job-to-monitor mode exchange
- Retrieved from CM in a monitor-to-job mode exchange

The JPS register works in tandem with the monitor process state (MPS) register in a Virtual State exchange operation. In an exchange from monitor mode to job mode, the CP stores the environment of the monitor mode process in an exchange package at MPS. Refer to figure I-2-6. The CP then initiates the process whose exchange package is located at JPS. This monitor-to-job mode exchange is initiated by an exchange instruction from within the monitor mode process.

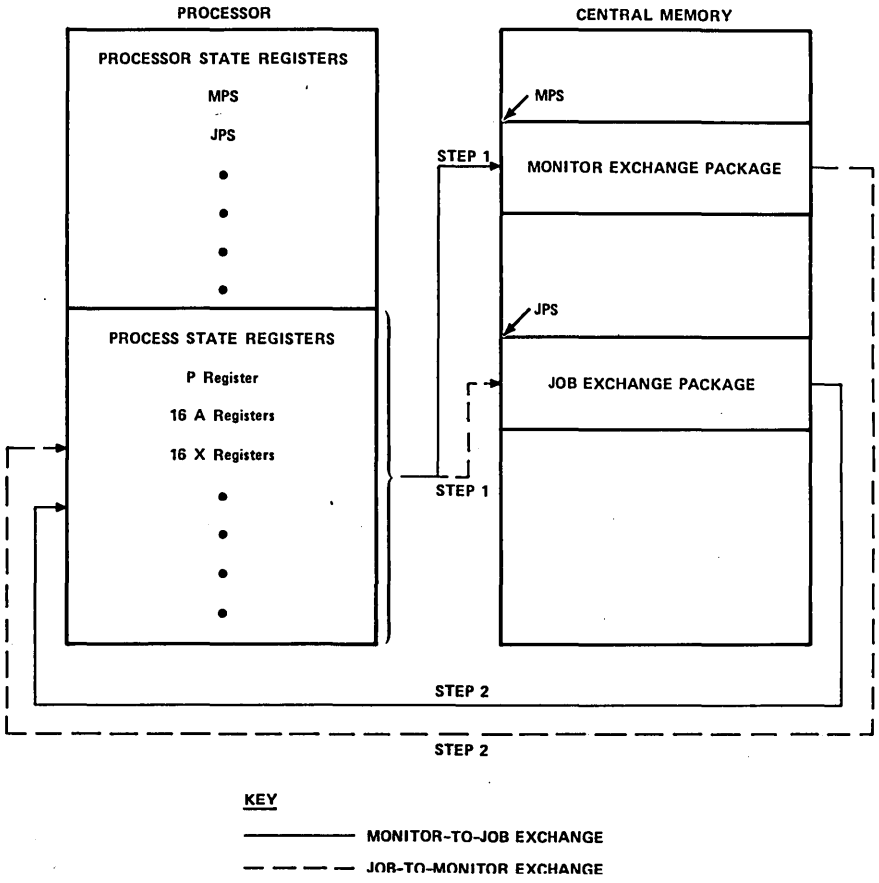


Figure I-2-6. JPS and MPS Functions in Exchange Operation

In an exchange from job mode to monitor mode, the CP stores the environment of the job mode process in an exchange package at JPS (refer to figure I-2-6). The CP then initiates the process whose exchange package is located at MPS. This job-to-monitor mode exchange is initiated either from an exchange instruction or the occurrence of some interrupt condition requiring monitor mode intervention.

Monitor Process State (MPS) Register

The MPS register holds the real memory address that points to the first entry in an exchange package in central memory. This address indicates where a job's process state registers are:

- Stored in CM in a monitor-to-job mode exchange
- Retrieved from CM in a job-to-monitor mode exchange

The MPS register works in tandem with the JPS register in a Virtual State exchange operation. Refer to Job Process State Register and to figure I-2-6.

EXECUTION SECTION

The CP execution section consists of the arithmetic and logical network (ALN) and the addressing network. The ALN contains hardware required to execute all floating-point (FP) and integer add, subtract, multiply, and divide instructions found in the CYBER 170 State and Virtual State instruction sets. The ALN also processes CYBER 170 State and Virtual State shift and Boolean instructions, as well as CYBER 170 State pack/unpack, normalize, and population count instructions.

The ALN plays a role in branch instructions by evaluating branch conditions. It performs operations during most other CYBER 170 State and Virtual State instructions, passing operands between register file locations, comparing operands, or completing other required arithmetic steps.

The ALN performs operations on values supplied by the operand issue section or, in some cases, the business data processing (BDP) section. The BDP section performs most BDP operations independently. All results return to the operand issue section except for exception conditions, which are sent to the instruction section to initiate interrupt handling.

The ALN consists of a general network and a multiply/divide network.

General Network

The general network adds and subtracts integers and FP coefficients, and performs exponent arithmetic associated with all FP operations. In addition, the general network performs Boolean, FP normalize, shift, and conditional branch test functions.

The integers are 60 bits in CYBER 170 State and 64 bits in Virtual State. FP operations use data in the form of an exponent, an exponent bias, a 48-bit (single precision) or 96-bit (double precision) coefficient, and a coefficient bias.

Negative CYBER 170 State operands typically are represented in ones-complement form, with negative Virtual State operands represented in twos-complement form. Operands may be 18 or 60 bits for CYBER 170 State operations; 32 or 64 bits for Virtual State operations.

Multiply/Divide Network

The multiply/divide network forms Virtual State integer products and FP product coefficients for both CYBER 170 State and Virtual State. In the former case, the product may be represented as a 32-bit or 64-bit Virtual State signed integer. In the latter case, the product may be represented as a 48-bit signed coefficient (CYBER 170 State FP operations), or a 48- or 96-bit coefficient in signed-magnitude form (Virtual State FP operations).

The network performs divide operations in which the coefficient of the dividend and divisor operands may be represented as a 32- or 64-bit signed integer (Virtual State only), or in one of the FP coefficient formats described in volume II, section 2, listed in the Publication Index in the preface.

Addressing Network

The addressing network has the following functions:

- Performs address arithmetic and data manipulation for loading and storing data in CM. The load and store instructions involve transferring a single bit, byte stream, word, or multiple words between register file locations (in the operand issue section) and CM locations.
- Performs the Test and Set Bit instruction, which transfers one bit from a CM location to a specified, constant bit position in an X register.
- Contains address streaming logic for BDP instructions.

MAP

Map provides the capability to translate process virtual addresses (PVAs) to real memory addresses (RMAs). During this translation, map also performs the security tests for addressing CM. To reduce CM access time, map contains up to 64 of the most recently used segment and page numbers as well as their corresponding page frame addresses (PFAs) and validity information.

Map Address Translation

For the PVA-to-RMA translation, map obtains PVAs from A registers (for load and store instructions) and the P register (for addressing instructions). Map performs the translation by comparing the segment and page numbers of the PVA to the segment and page numbers existing in its files. If a match occurs, map provides the corresponding PFA. The PFA joins the page offset from the PVA to form the RMA. If a match does not occur, the execution section searches the segment table and system page table, brings the required descriptors, and performs PVA-to-RMA translation under microprogram control. In this case, map updates its files by replacing the least recently used entry by the most recently translated address information. For further information, refer to Virtual Memory or to Virtual Memory Programming in volume II, section 2, listed in the Publication Index in the preface.

Map Access Validation

The security mechanism in map provides controlled access to all code and data. This protects the operating system from users, users from each other, and users from the operating system. The basic element of protection is the user's address space, which is the set of addresses the operating system assigns to an executing process. This address space is defined by the set of segment descriptors in the operating system-maintained segment descriptor table (SDT). Each segment descriptor defines the security protection features for one segment. The protection features consist of security ring tests, key and lock tests, and read/write/execute privilege validity tests. For every CM access attempted, all of these tests must be successful. For further information, refer to Virtual Memory Programming in volume II, section 2, listed in the Publication Index in the preface.

BUSINESS DATA PROCESSING (BDP) SECTION

The BDP section executes BDP instructions that operate on CM data fields up to 256 bytes in length. Although the BDP section performs most BDP operations independently, for some operations it may require processing assistance from the ALN in the execution section. BDP operations use any of the following data types:

- Packed decimal
- Unpacked decimal
- Binary
- Alphanumeric

In many cases, the data types may be freely mixed as the hardware performs the type translations required for various BDP operations. Refer to BDP Programming in volume II, section 2, for descriptions of the data types.

BDP instructions reference BDP data via data descriptors, which are in the main instruction stream and which contain information about the location, size, and type of data. The BDP data descriptors also specify two data fields in CM: the source field and the destination field. The former modifies, replaces, or compares to the latter.

MAINTENANCE ACCESS CONTROL (MAC)

The MAC performs initialization and maintenance operations. These operations, controlled by a dedicated peripheral processor in the IOU, include the following:

- Initialize registers, controls, and memories
- Read and write CP-resident registers and memories
- Read and write maintenance registers of the system components
- Monitor and record CP error/status information
- Verify error detection and correction hardware
- Reconfigure CP

The IOU sends codes to MAC to indicate the operations to be performed and the affected memory device, registers, and addresses. Certain MAC registers contain CP and CM fault isolation information. Other registers control the internal configuration and operation of the CP and verify that errors are properly reported and recorded. For more detailed information, refer to Maintenance Channel Programming in volume II, section 2, listed in the Publication Index in the preface.

CENTRAL MEMORY (CM)

The CM performs the following functions:

- Two or four memory banks store from 262K to 4192K 64-bit words with 8-bit single error correction, double error detection (SECDED) codes.
- Two ports make CM accessible to the CPs and every PP.

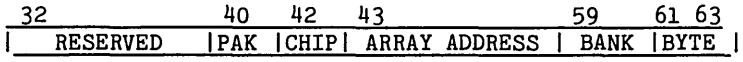
- CM bounds register limits writes to CM from any or all ports.
- Generates SECDED code bits and stores them with each word. SECDED circuits check circuits, correct single-bit errors, and detect double-bit errors.
- Maintenance channel interface gives a PP in the IOU access to the CM maintenance registers for system initialization, corrective action, error reporting and diagnostics, and for setting the port bounds register.

The CM also contains central memory control (CMC) that includes:

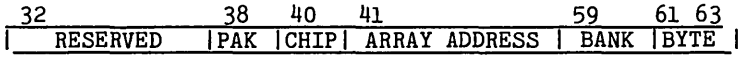
- Ports and distributor
- SECDED logic which corrects single-bit errors and detects double-bit errors
- Partial-write logic which modifies one or more bytes in a memory word
- Memory control logic which controls CM reads and writes, and resolves CM bank conflicts and simultaneous CM request conflicts
- Maintenance registers which monitor CM and CMC errors and provides the means for testing and reconfiguring CM for maintenance purposes

ADDRESS FORMAT

Figure I-2-7 illustrates the address format.



12, 16 MB (64K CHIP) ADDRESS FORMAT



16, 32 MB (256K CHIP) ADDRESS FORMAT

Figure I-2-7. Central Memory Address Format

The following list defines the address fields.

- Byte select specifies one of eight bytes in a word. These 3 bits are not part of the word address sent to CM.
- Bank select specifies one of four banks. Since the bank address is the lower 2 bits of the storage address, sequential addressing results in a phased-bank operation which allows a maximum data transfer rate of one word each clock period.
- Pak select specifies one of four paks for the selected bank.
- Chip select specifies one of the two groups of chips in the selected pak.
- Row and column address bits specify a word in the selected group of chips.

CM ACCESS AND CYCLE TIMES

The CM access time for a read operation is 450 nanoseconds for model 830; 1250 for model 810.

Cycle time for read or write operation is 8 clock periods (400 nanoseconds) for model 830; 24 clock periods (1200 nanoseconds) for model 810. Cycle time for partial write (read/write/modify) is 16 clock periods (800 nanoseconds) for model 830; 32 clock periods (1600 nanoseconds) for model 810.

The CM bounds register limits CM write access to an area between two addresses specified in this register. The CM bounds register is set through the maintenance channel. Refer to Maintenance Channel Programming in volume II, section 2, listed in the Publication Index in the preface.

CM PORTS AND PRIORITIES

A priority network resolves port access conflicts on a rotating basis, preventing long term lockout of any port. In case of simultaneous requests, the CP has priority. Refer to table I-2-5 for maximum request lockout time.

Table I-2-5. Port Priority

	MAX REQUEST LOCKOUT TIME IN BANK CYCLES*	
PORT	READ OR WRITE REQUESTS	READ/MODIFY/WRITE REQUESTS
(REFRESH)	1	2
CPU PORT	2	3
IOU PORT	3	5
* 1 bank cycle = 8 clock periods = 400 ns for model 830 1 bank cycle = 24 clock periods = 1200 ns for model 810		

SECDED

The SECDED logic corrects single-bit errors during a CM read operation, permitting unimpeded computer operation. The SECDED logic prepares for the error correction by generating error correction code (ECC) bits for each data word and by storing these ECC bits in CM with the data word during the CM write. Table I-2-6 lists the hexadecimal codes for all the combinations of syndrome bits with the number of the data bit assigned each code or a note categorizing each code. Then, during a CM read, CM performs the following SECDED sequence:

1. Read one CM word and generate new ECC bits for data portion of CM word.
2. Compare new ECC bits with CM word ECC bits.
3. If old and new ECC bits match, no error exists. Send data to requesting unit.
4. If bits do not match, generate syndrome bits from result of ECC compare.
5. Decode syndrome bits to determine if single- or multiple-bit failure.
6. If single-bit failure, correct by inverting failing bit in data word. Send corrected word to requesting unit. (Also sets Soft Error Log bit in MCR.)

Table I-2-6. SECDED Syndrome Codes/Corrected Bits

Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit
00	(6)	20	66 (2)	40	65 (2)	60	(3)	80	64 (2)	A0	(3)	C0	(3)	E0	0 (1)
01	71 (2)	21	(3)	41	(3)	61	(4)	81	(3)	A1	(4)	C1	(4)	E1	0 (5)
02	70 (2)	22	(3)	42	(3)	62	(4)	82	(3)	A2	(4)	C2	(4)	E2	16 (5)
03	(3)	23	(4)	43	(4)	63	(3)	83	(4)	A3	(3)	C3	(3)	E3	16 (1)
04	69 (2)	24	(3)	44	(3)	64	(4)	84	(3)	A4	(4)	C4	(4)	E4	2 (5)
05	(3)	25	(4)	45	(4)	65	(3)	85	(4)	A5	(3)	C5	(3)	E5	2 (1)
06	(3)	26	(4)	46	(4)	66	(3)	86	(4)	A6	(3)	C6	(3)	E6	18 (1)
07	44 (1)	27	60 (5)	47	46 (5)	67	62 (1)	87	45 (5)	A7	61 (1)	C7	47 (1)	E7	18/63 (5)
08	68 (2)	28	(3)	48	(3)	68	(4)	88	(3)	A8	(4)	C8	(4)	E8	1 (5)
09	(3)	29	(4)	49	(4)	69	(3)	89	(4)	A9	(3)	C9	(3)	E9	1 (1)
0A	(3)	2A	(4)	4A	(4)	6A	(3)	8A	(4)	AA	(3)	CA	(3)	EA	17 (1)
0B	12 (1)	2B	28 (5)	4B	14 (5)	6B	30 (1)	8B	13 (5)	AB	29 (1)	CB	15 (1)	EB	17/31 (5)
0C	(3)	2C	(4)	4C	(4)	6C	(3)	8C	(4)	AC	(3)	CC	(3)	EC	3 (1)
0D	40 (1)	2D	56 (5)	4D	41 (5)	6D	58 (1)	8D	41 (5)	AD	57 (1)	CD	43 (1)	ED	3/59 (5)
0E	8 (1)	2E	24 (5)	4E	10 (5)	6E	26 (1)	8E	9 (5)	AE	25 (1)	CE	11 (1)	EE	19/27 (5)
0F	(3)	2F	(4)	4F	(4)	6F	(3)	8F	(4)	AF	(3)	CF	(3)	EF	19 (1)
10	67 (2)	30	(3)	50	(3)	70	36 (1)	90	(3)	B0	4 (1)	D0	32 (1)	F0	(3)
11	(3)	31	(4)	51	(4)	71	36 (5)	91	(4)	B1	4 (5)	D1	32 (5)	F1	(4)
12	(3)	32	(4)	52	(4)	72	52 (5)	92	(4)	B2	20 (5)	D2	48 (5)	F2	(4)
13	(4)	33	(3)	53	(3)	73	52 (1)	93	(3)	B3	20 (1)	D3	48 (1)	F3	(3)
14	(3)	34	(4)	54	(4)	74	38 (5)	94	(4)	B4	6 (5)	D4	34 (5)	F4	(4)
15	(4)	35	(3)	55	(3)	75	38 (1)	95	(3)	B5	6 (1)	D5	34 (1)	F5	(3)
16	(4)	36	(3)	56	(3)	76	54 (1)	96	(3)	B6	22 (1)	D6	50 (1)	F6	(3)
17	44 (5)	37	60 (1)	57	46 (1)	77	54/62 (5)	97	45 (1)	B7	22/61 (5)	D7	47/50 (5)	F7	63 (1)
18	(3)	38	(4)	58	(4)	78	37 (5)	98	(4)	B8	5 (5)	D8	33 (5)	F8	(4)
19	(4)	39	(3)	59	(3)	79	37 (1)	99	(3)	B9	5 (1)	D9	33 (1)	F9	(3)
1A	(4)	3A	(3)	5A	(3)	7A	53 (1)	9A	(3)	BA	21 (1)	DA	49 (1)	FA	(3)
1B	12 (5)	3B	28 (1)	5B	14 (1)	7B	30/53 (5)	9B	13 (1)	BB	21/29 (5)	DB	15/49 (5)	FB	31 (1)
1C	(4)	3C	(3)	5C	(3)	7C	39 (1)	9C	(3)	BC	7 (1)	DC	35 (1)	FC	(3)
1D	40 (5)	3D	56 (1)	5D	42 (1)	7D	39/58 (5)	9D	41 (1)	BD	7/57 (5)	DD	35/43 (5)	FD	59 (1)
1E	8 (5)	3E	24 (1)	5E	10 (1)	7E	26/55 (5)	9E	9 (1)	BE	23/25 (5)	DE	11/51 (5)	FE	27 (1)
1F	(4)	3F	(3)	5F	(3)	7F	55 (1)	9F	(3)	BF	23 (1)	DF	51 (1)	FF	(3)

Notes:
1 Corrected single-bit error.
2 Syndrome code bit failed (single code bit set).
3 Double error or multiple error (even number of code bits set).
4 Multiple error reported as a single error.
5 Double error or multiple error with indicated bit(s) inverted.
6 No error detected.

7. If multiple-bit or other uncorrectable error, send uncorrectable error response code to CP or IOU. (Also sets Detected Uncorrectable Error bit in MCR.) A PP in the IOU may then analyze the syndrome bits using the maintenance channel.

Certain CM registers assist in SECDED analysis. The Corrected Error Log (CEL) register displays details of the first corrected error and the Uncorrectable Error Log (UEL) register displays details of the first two uncorrected errors. For detailed descriptions of these registers, refer to CM Registers in volume II, section 2, listed in the Publication Index in the preface. The syndrome bits may be analyzed through the maintenance channel.

CM BOUNDS REGISTER

The CM bounds register limits the write access to CM from specified ports. The ports are limited to the area between an upper and lower bound as specified in the CM bounds register. Bits in byte 0 specify the port(s) from which the write access is limited. The CM bounds register is set through the maintenance channel. For further information, refer to Maintenance Channel Programming in volume II, section 2, listed in the Publication Index in the preface.

CM MAINTENANCE REGISTERS

The CM contains maintenance registers which hold memory status and error information. These registers are accessible through the maintenance channel. Table I-2-7 lists the CM maintenance registers. For detailed decriptions of these registers refer to CM Registers in volume II, section 2, listed in the Publication Index in the preface.

Table I-2-7. CM Maintenance Registers

Register Name	
Bounds Register	
Corrected Error Log	
Element Identification (EI)	
Environment Control (EC)	
Free-Running Counter	
Options Installed (OI)	
Status Summary	
Uncorrectable Error Log 1	
Uncorrectable Error Log 2	

CM RECONFIGURATION

CM reconfiguration permits the computer operator to restructure the CM addresses so that a failing part of CM can be quickly locked out to provide a continuous block of usable CM from address zero. CM reconfiguration is accomplished by setting the parameters in the deadstart display to manipulate the upper address bits. For further information, refer to the hardware operator's guide listed in the preface.

VIRTUAL MEMORY

Central memory functions as a virtual memory. Virtual memory effectively gives each user a vast, unique address space complete with a copy of the operating system. Actually, most user code and data reside in external mass storage, and virtual memory code sharing enables the apparent duplication of product set and operating system routines such as Fortran compiler, trap handler, and memory manager.

Virtual memory is discussed in the following paragraphs. For information regarding operation of CYBER 170 State (real) memory, refer to the appropriate CYBER 170 State hardware reference manual listed in the preface.

The operating system, with hardware support, manages virtual memory by segmenting virtual memory code and data and mapping this information to real memory pages.

Segments

Segments, shown in figure I-2-8, are the units of virtual memory storage. Each user's executing process operates in a unique virtual address space divided into a number of segments. A maximum of 4096 segments may exist for each process, and over 65,000 segments may exist system-wide for all user processes. Each segment has a capacity of 2000 Megabytes (262 million words). Segment size varies according to the amount of information it contains.

In addition to partitioning the virtual address space, the segment typically provides the natural divisions of code and data in a process. For instance, one segment may hold data files used by the process, another executable code unique to the process, and another a duplicate copy of operating system code shared with other users.

To optimize the use of real memory, operating system segments which reside in user address space (that is, monitor mode interrupt handler) are shared by several users, and thus conceptually exist as multiple copies in virtual memory.

Segments also play an important role in access protection. Each segment is assigned a set of read, write, and execute attributes which characterize the use of that segment by various users. For further information, refer to Access Protection or to Virtual Memory Programming in Volume II, section 2, listed in the Publication Index in the preface.

Pages

Pages, shown in figure I-2-9, are the units of real memory storage. Pages also serve as the common storage unit between virtual and real memory. Although pages exist within segments, hardware carries the pages only as bookkeeping in virtual memory. The virtual-to-real page translation facilitates the efficient use of available CM through demand paging. This translation eliminates the need for programmer-created program overlays.

Page size (the number of memory words per page) is a fixed length selected at system initialization and is constant from one deadstart to the next. Pages may be 2K, 4K, 8K, or 16K bytes in length. The number of pages per segment is proportional to page size.

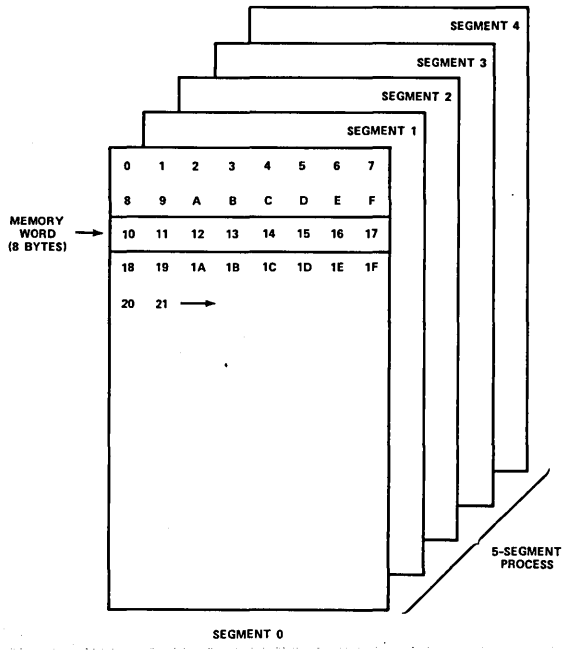


Figure I-2-8. Segments in a Process

Central memory comprises physical sections of equal size called page frames. Pages are the same size as page frames; thus, one page of information from external mass storage loads (on demand) into one page frame in CM. A page may or may not reside in CM, depending on its recent use and the competing demand for CM space in retrieving other process's pages from external mass storage. Many more pages exist in virtual memory than in real memory, and pages are brought from virtual into real memory on a demand basis. Data transfers between CM and external mass storage one page at a time.

Address Translation

CP instructions address memory by way of process virtual addresses (PVAs). A PVA is the only type of address a user sees. To locate the requested memory word, the CP translates a PVA to a real memory address (RMA). Hardware performs the translation in two steps by 1) converting a PVA to a system virtual address (SVA), and 2) converting an SVA to an RMA.

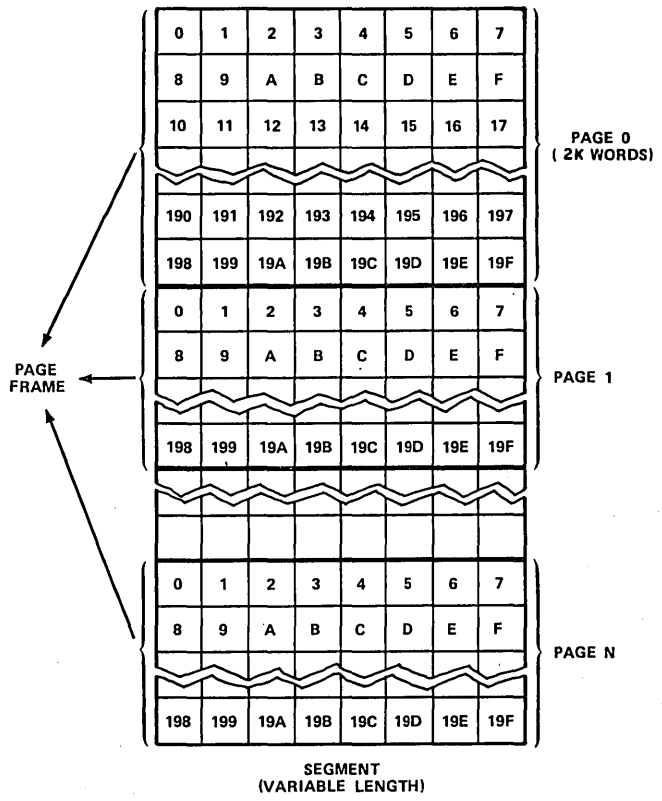


Figure I-2-9. Pages in a Segment

The distinctly different functions performed by the two steps are:

- The PVA-to-SVA translation performs a security check which determines whether the process has the necessary privilege to access the requested code/data.
- The SVA-to-RMA translation performs the memory management task of converting the system-wide virtual address to an RMA, which locates the requested code/data in central memory or external mass storage. In the latter, the operating system retrieves the relevant real memory page from external mass storage into CM.

The operating system maintains tables in memory which make possible the PVA-to-SVA-to-RMA conversion with access protection (refer to figure I-2-10). When translating a PVA to an SVA, the CP uses a software-managed segment descriptor table that describes the unique address space for that segment. When translating an SVA to an RMA, the CP uses the software-managed system page table that contains a page descriptor for each active page in CM.

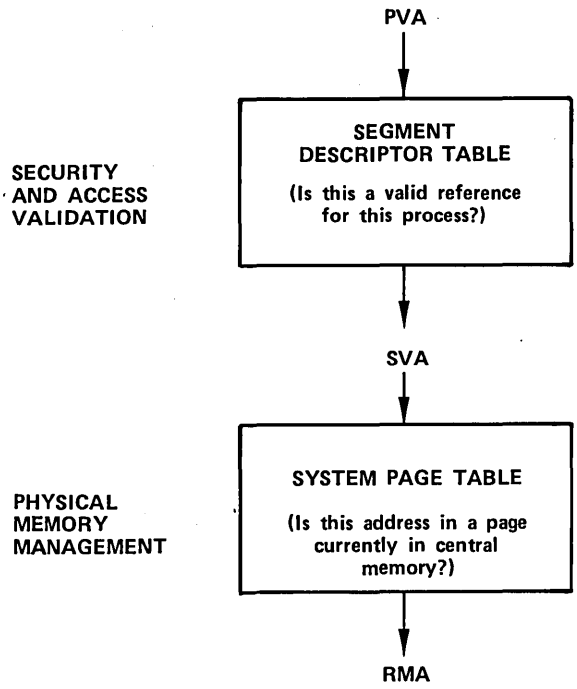


Figure I-2-10. Segment/Page Table Role in Address Translation

Access Protection

Access protection consists of constraining each user to an address space and preventing unauthorized reading, writing, or executing of code or data outside this address space. As previously mentioned, the nature of virtual memory allows the operating system to exist in the programmer's address space. Access protection mechanisms are therefore necessary to ensure that protection between system code and user code/data occurs at all times.

The operating system sets access requirements and privileges from information on file or by responding to legitimate requests from the user. The user cannot directly change access requirements or increase access privileges as set by the operating system because the operating system lists the access requirements of process segments in user-inaccessible areas in CM and places access privilege information with the program counter and address registers.

When the CP presents an address for translation, hardware tests for proper access privilege. Testing of privilege occurs by way of attributes, rings of protection, and keys and locks. All three tests must be successful, or the CP interrupts the process and performs an exchange to another process. The monitor mode interrupt handler determines appropriate action for the interrupted process.

Attributes

The operating system assigns a set of read/write/execute attributes to each segment; any combination may be assigned. These attributes characterize the use of that segment by various users. The operating system records the attributes in a segment descriptor table for each process and references them at the PVA level of address translation. It is possible for more than one process to share a segment with each process having different access attributes. This forms the basis for code sharing.

When first referencing a PVA, the CP compares the type of reference (read/write/execute) to the attributes of the segment where the PVA resides. To complete the operation, the reference privilege must match a like segment attribute. For instance, reading a particular data segment cannot occur unless the requested segment has a read attribute.

Rings of Protection

The system virtual address space comprises 15 rings of protection. The rings primarily prevent unauthorized access, although rings typically also separate code and data segments. The 15 rings have a hierarchical organization such that the lower the ring number, the higher the privilege. For instance, operating system segments occupy the lowest rings, and the least privileged user segments occupy the highest rings.

Code and data segments for a process may exist in several rings. When this occurs, the segment is said to reside in a ring bracket. There are four ring brackets associated with each segment. These are read, write, execute, and call brackets. The brackets are an extension of the read/write/execute access attributes. On an initial reference to a PVA, the CP compares the ring bracket of the process attempting the read, write, execute, or call to the ring number of the segment where the PVA exists. To complete the access, the referenced segment must reside in an accessible ring bracket.

Keys and Locks

Keys and locks provide a protection mechanism for segments that reside within the same ring of protection. This function includes:

- The protection of local data used by a particular procedure(s)
- The isolation of competing applications residing in the same ring

The CP associates a lock with each segment and, in general, only grants access to one segment from another if the keys exactly match the locks. Thus, this protection mechanism has no hierarchical significance but depends only on whether the keys and locks match.

INPUT/OUTPUT UNIT

The IOU performs the functions necessary to locate, select, and initialize the external devices connected to the system. The IOU also controls the transfer of data between a selected device and CM, as well as performing system maintenance functions.

The IOU contains the following functional areas:

- Peripheral processors (PPs)
- I/O channels
- Maintenance channel
- CM access

PERIPHERAL PROCESSOR

The basic IOU contains 10 PPs and can be expanded to 20 PPs with one increment. Each PP is a logically independent computer with its own memory. Each 10-PP group is organized into a multiplexing system which allows the PPs to share common hardware for arithmetic, logical, and I/O operations without losing independence. This multiplexing system comprises ten ranks of registers termed a barrel. Each rank contains information related to the instruction being executed by one PP.

Each PP can communicate with:

- Other PPs over the I/O channels and through CM
- The CP via CM read and write operations
- The CP (in CYBER 170 State operation) by issuing a CYBER 170 State exchange request to a specific CYBER 170 State exchange package associated with the issuing PP

Each PP can also cause an interrupt condition with the CP operating in either Virtual State or CYBER 170 State.

Each PP executes programs alone or with other PPs to control data transfers between external devices and CM. These programs, called I/O drivers, comprise IOU instructions combined to interact with operating system requests issued through CM. The I/O drivers translate generalized operating system requests into control functions for accessing the external devices and may also perform device scheduling and optimization. The I/O drivers use PP memory as a buffer for the data transfer between external devices and CM to isolate IOU data transfers from variations in CM transfer rate.

DEADSTART

A deadstart sequence allows the IOU to initialize itself. This deadstart sequence is initiated from the operator console. The deadstart display includes parameters for assigning any PP memory (PPM) to PP0. For further information, refer to the Hardware Operator's Guide listed in the preface.

BARREL AND SLOT

The barrel, shown in figure I-2-11, consists of the A, K, P, Q, and R registers, each of which has ten ranks numbered 0 through 11_8. Information in these registers is transferred from one rank to the next at a uniform 20-megahertz rate, providing a multiplexed system of

ten PPs, each operating at a 2-megahertz rate. The registers are stationary while the PPs rotate. For example, rank 4 registers contain PP0 through PP11$_8$ in succession, each consuming 50 nanoseconds of the total cycle time of 500 nanoseconds. Since the PP memories operate at a slower rate, independent memory with its own address and data registers is provided for each PP.

Each time data enters the slot, a portion of the instruction for that data is executed. The slot performs tasks such as arithmetic and logic operations, and program address manipulation. Complete execution of an instruction may require the A, K, P, Q, and R register quantities to go more than one trip around the barrel and through the slot.

The PPM may be referenced once each time the PP passes around the barrel and through the slot. During its slot time, the PP may also communicate with CM or any of the I/O channels.

PP REGISTERS

The PP registers consist of the A, K, P, Q, and R registers. The registers and their descriptions follow.

A Register

The 18-bit A register contains one of two operands for arithmetic and logic operations. The content of A may be an arithmetic operand, a CM address or part of a CM address, an I/O function, an I/O data word, or a word count for a block I/O or CM transfer. Various instructions operate on 6, 12, or 18 bits of the A register. Calculation results are always placed in the A register, although some instructions also write the result into PP memory.

When the A register provides the CM address, parity is generated with the address for transmission to memory control. When the A register provides data or function words for I/O activities, channel parity is always generated on 16 bits of A.

At deadstart, the A register is set to 10000$_8$.

K Register

The 12-bit K register is visible to the programmer through the maintenance channel and the IOU deadstart panel. This register holds the operation code field of an instruction for display and is used for maintenance purposes. When a PP is halted (idled), this register contains all ones.

P Register

The 12-bit P register is the PP program address counter. Also, during block I/O and CM transfers, the P register temporarily contains the PP memory address of the data transfer. At deadstart, the P register is set to 7777$_8$.

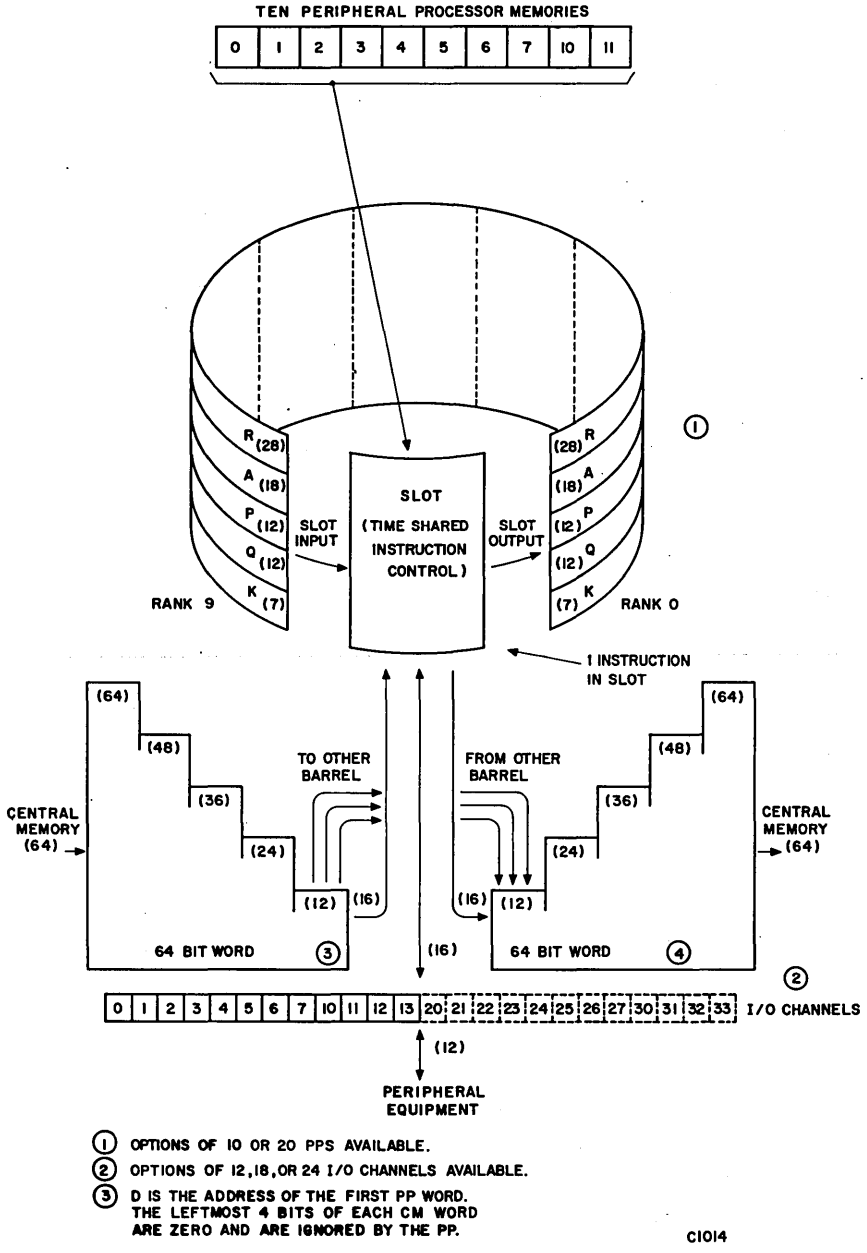


Figure I-2-11. IOU Barrel and Slot

Q Register

The 12-bit Q register may hold the following data:

- Operand address for direct and indirect addressing
- Peripheral address of data used during single-word CM read/write instructions
- Shift count
- Word count for CM block transfers
- Upper 6 bits during constant mode PP instructions
- Target address for relative jump
- Channel number for all I/O and channel instructions

At deadstart, each rank of the Q register is set to a corresponding PP number Rank 0 is set to PP0, rank 2 is set to PP2, and so on.

R Register

The 22-bit R register, in conjunction with the A register, forms an absolute CM address for CM read/write instruction. Refer to Central Memory Access by PPs.

PP NUMBERING

PPs are numbered in octal as follows:

Barrel	PPs
0	00 through 11
1	20 through 31

The deadstart sequence decodes deadstart program parameters to determine PP numbering within a barrel. The sequence assigns barrel numbers according to the switch settings and, during the first minor cycle after deadstart, loads a zero into the Q register in barrel 0. This defines all the data in that rank of the barrel as belonging to PP0 and since Q is the channel selector, assigns PP0 to channel 0. During the next minor cycle, Q loads with a 1. This defines PP1 and assigns it to channel 1. This process occurs in parallel in all barrels until the IOU assigns each rank of the barrel with a PP number and a channel number. Reassignment can only be done at deadstart.

PP MEMORY

Each PP has an independent 4K word memory; each word contains 16 data bits and 1 parity bit. PP0 reads the deadstart program from the deadstart display during the deadstart operation. Therefore, PP memory 0 must be operational. A PP memory reconfiguration feature allows the user to restore IOU operation if the IOU detects a fault in the PP memory normally assigned to PP0.

To reconfigure, the operator assigns a good PP memory to PP0, and the operating system removes the failing PP memory. Computer operation can continue without the failing PP memory, and repairs can be made during scheduled maintenance. The system must be deadstarted to reconfigure PPs.

I/O CHANNELS

The I/O channels comprise an internal interface that allows common hardware and software to control the external devices, and an external interface that allows the IOU to communicate with the external devices using 12/16-bit data channels or an 8-bit maintenance channel.

The internal interface can transfer data between two PPs, or between a PP and an external device, at a maximum rate of one word every 500 nanoseconds. This rate can be sustained for the maximum practical channel transfer (4096 words). During transfers between PPs, if the PPs are not in the slot at the same time, the transfer rate is one every 1000 nanoseconds.

The external interface contains the interface mechanisms to connect the appropriate channel for an external device. The transfer rate between an I/O device and a PP is a function of the channel type and the maximum data transfer rate of the I/O device.

All PPs communicate with external devices through the independent I/O channels. Each channel may be connected to one or more pieces of external equipment, but only one piece of equipment can use a channel at one time. All channels can be active simultaneously.

DISPLAY STATION CONTROLLER

The display station controller (DSC) is the IOU interface between the PPs and the CC545 display station; the DSC services both the keyboard and the cathode-ray tube (CRT). The DSC transmits function words and digital symbol size/position data to the display station and receives digital character codes from the keyboard. It also receives digital symbol codes from the PPs and converts these to analog symbols to the CRT.

REAL-TIME CLOCK

The real-time clock is a 12-bit free-running counter, incrementing at a 1-megahertz rate. It is permanently attached to channel 14_8. This channel may be read at any time since it is active and full flags are always set.

TWO-PORT MULTIPLEXER

The two-port multiplexer provides communication capability between a PP and two attached terminals. It can simultaneously drive the two terminals at different baud rates. One port is reserved for maintenance purposes, and the other port is for CDC 721 display terminals. The two-port mulptiplexer is permanently attached to channel 15_8.

MAINTENANCE CHANNEL

The maintenance channel (MCH) is used for initialization of the CP and CM maintenance registers and monitoring of error status.

The maintenance channel consists of the maintenance channel interface on channel 17_8, a maintenance access control (MAC) in the CP, CM, IOU, and a set of interconnecting cables.

Any PP can be programmed to act as the maintenance control unit (MCU). However, hardware dictates PP0 as having special deadstart functions such that PP0 optimally serves as the MCU. In any case, the PP acting as the MCU performs initialization and maintenance functions that include:

- Initializing registers, controls, and memories
- Monitoring and recording error information
- Verifying error detection and correction hardware

The MCU directs these operations by sending function words (instructions) over the maintenance channel to the CP, CM, and IOU. The MCU retains all normal PP capabilities and, except for PP0 deadstart functions, does not gain any special hardware capabilities.

IOU MAINTENANCE REGISTERS

The MAC in the IOU contains several maintenance registers which hold IOU status or error information. Table I-2-8 lists the IOU maintenance registers. For detailed descriptions of these registers, refer to IOU Registers in volume II, section 2, listed in the Publication Index in the preface.

Table I-2-8. IOU Maintenance Registers

Register Name	
Element Identification (EI)	
Environment Control (EC)	
Fault Status Mask	
Fault Status 1	
Fault Status 2	
Options Installed (OI)	
OS Bounds	
Status Register	
Test Mode	

CENTRAL MEMORY ACCESS BY PPS

Any PP can access CM. During a write from the IOU to CM, the IOU assembles four successive 16-bit PP words into one 64-bit CM word (Virtual State) or five successive 12-bit PP words into one 60-bit CM word (CYBER 170 State). During a CM read, the IOU disassembles a 64-bit CM word into four 16-bit PP words (Virtual State), or a 60-bit CM word into five 12-bit PP words (CYBER 170 State).

To find the CM address, a PP reads the A register. If bit 17 of the A register is clear, the PP uses the contents of the A register for the CM address. If bit 17 of the A register is set, the PP adds the relocation address from the R register to the A register to for the CM address.

A maximum of 20 PPs in various stages of assembly/disassembly can simultaneously read CM words, and 5 PPs can write CM words.

COMMENT SHEET

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