60458110

CONTROL DATA CORPORATION

CDC® CYBER 170 COMPUTER SYSTEMS MODELS 815, 825, 835, 845, AND 855

CDC® CYBER 180 COMPUTER SYSTEMS MODELS 810, 830, 835, 845, 850, 855, 860, AND 990

MAINTENANCE REGISTER CODES BOOKLET

REVISION RECORD

REVISION	DESCRIPTION
A (12-30-82)	Manual released.
B (07-08-83)	Manual revised. Includes engineering change order 44612. This edition obsoletes all previous editions.
C (07-15-84)	Manual revised to add support of CYBER 170 Model 845 and CYBER 180 Models 810, 830, 835, 845, 850, 855, 860, and 990 Computer Systems. Because extensive changes are made, change bars and dots are not used, and all pages reflect the latest revision level. This edition obsoletes all previous editions.

Publication No.
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REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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or use Comment Sheet in the back of this manual.

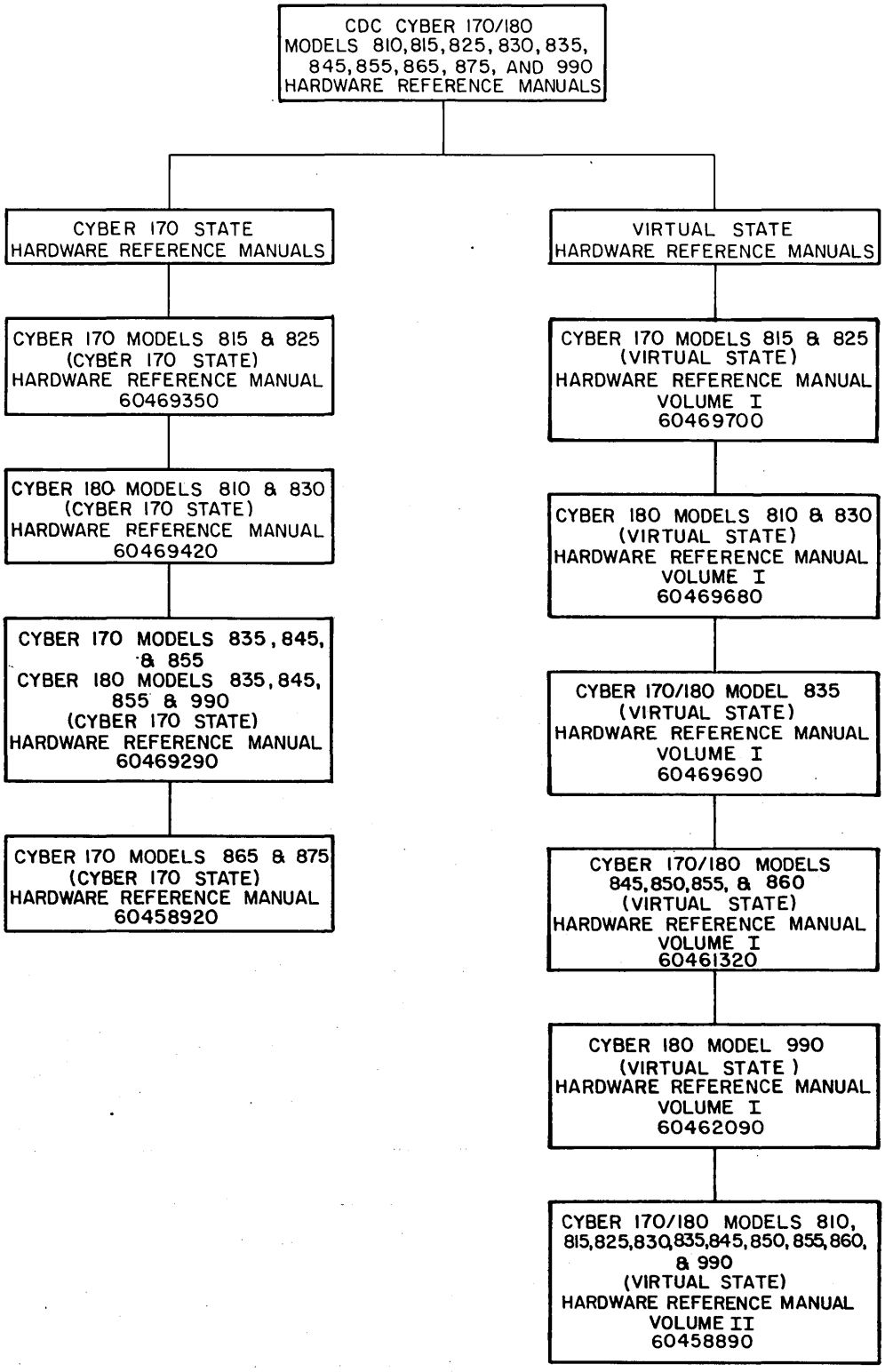
PREFACE

This maintenance register codes booklet provides bit descriptions of all maintenance registers for the CONTROL DATA® CYBER 170 Computer Systems, Models 815, 825, 835, 845, and 855 and CDC® Computer Systems, Models 810, 830, 835, 845, 850, 855, 860, and 990.

The systems publication index following the preface lists the hardware reference manuals that are applicable to the CYBER 170 Computer Systems, Models 815, 825, 835, 845, and 855 and CYBER 180 Computer Systems, Models 810, 830, 835, 845, 850, 855, 860, and 990.

Refer to the Literature and Distribution Services Catalog for the latest manual revision levels and literature ordering procedures.

SYSTEM PUBLICATION INDEX

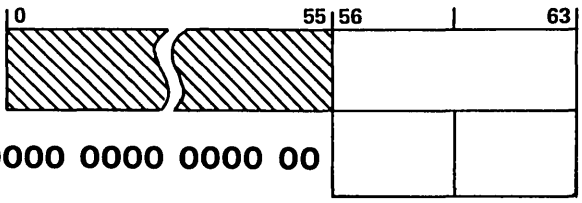


CONTENTS

INTRODUCTION

This codes booklet is a complete listing of all the maintenance registers and codes related to the CYBER 170 Computer Systems, Models 815, 825, 835, 845, and 855 and the CYBER 180 Computer Systems, Models 810, 830, 835, 845, 850, 855, 860, and 990. Additional information may be found in the appropriate computer systems hardware reference manual listed in the preface. All mnemonics listed in this booklet apply to the COMPASS assembly language.

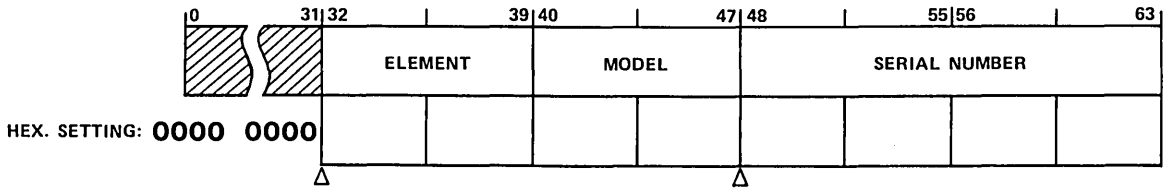
STATUS SUMMARY REGISTER (00) (MODELS 810 THROUGH 990)



Bit	IOU-810 through 990	MEM-810 through 990	PROC-810 through 990
00 through 55	(Not used)	(Not used)	(Not used)
56	(Not used)	Oscillator selected*	(Not used)
57	(Not used)	Oscillator selected*	(Not used)
58	(Not used)	Clock tuning mode	C180 monitor mode
59	Summary status	(Not used)	Short warning
60	Processor halt	(Not used)	Processor halt
61	Uncorrectable error	Uncorrectable error	Uncorrectable error
62	(Not used)	Corrected error	Corrected error
63	Long warning	Long warning	Long warning

* 00 normal
  01 +2 percent
  10 -2 percent

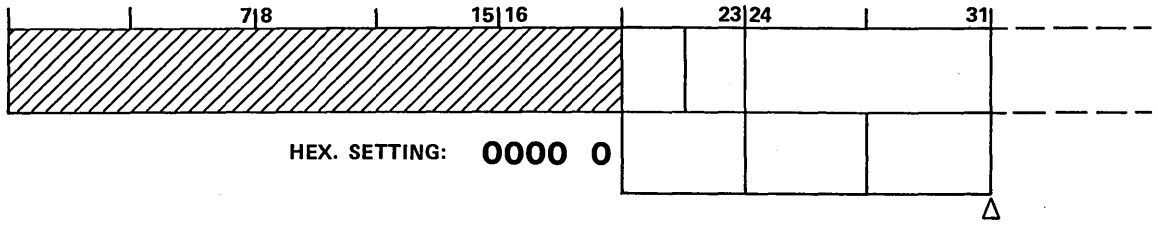
EID REGISTER (10) (MODELS 810 THROUGH 990)



Element	Element No.	Model No.
PROC-810	00	14
MEM-810	01	14
IOU-810	02	14
PROC-815	00	11
MEM-815	01	11
IOU-815	02	11
PROC-825*	00	12
MEM-825	01	12
IOU-825	02	12
PROC-830*	00	13
MEM-830	01	13
IOU-830	02	13
PROC-835*	00	20
MEM-835	01	20
IOU-835 through 990	02	20
PROC-845*	00	31
MEM-845, 855	01	30
MEM-850, 860	01	31
PROC-850	00	33
PROC-860*	00	32
PROC-855*	00	30
PROC-990*	00	40
MEM-990	01	40
ECS COUPLER	03	20
PEM	04	20

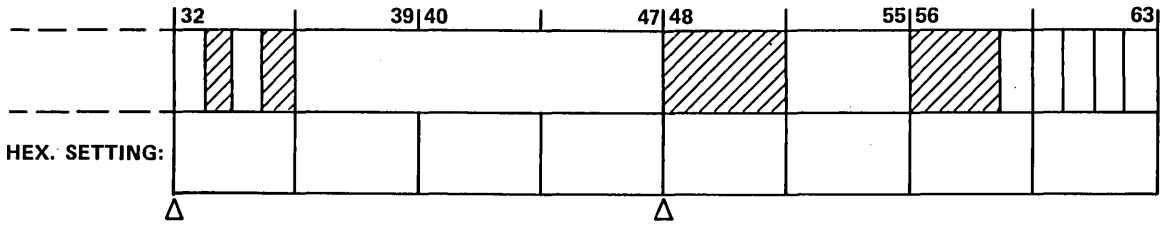
* Applies to both single and (optional) dual CP

IOU-810 THROUGH 990 OI REGISTERS (12)



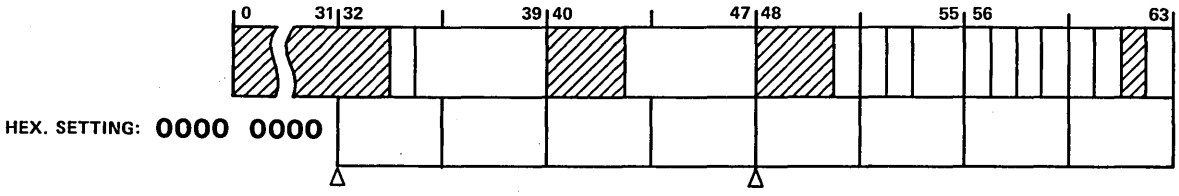
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	(Not used)
04	(Not used)
05	(Not used)
06	(Not used)
07	(Not used)
08	(Not used)
09	(Not used)
10	(Not used)
11	(Not used)
12	(Not used)
13	(Not used)
14	(Not used)
15	(Not used)
16	(Not used)
17	(Not used)
18	(Not used)
19	(Not used)
20	Barrel 3, PP 25 through 31
21	Barrel 2, PP 20 through 24
22	Barrel 1, PP 5 through 11
23	Barrel 0, PP 0 through 4
24	Channel 7
25	Channel 6
26	Channel 5
27	Channel 4
28	Channel 3
29	Channel 2
30	Channel 1
31	Channel 0

IOU-810 THROUGH 990 0I REGISTERS (12)



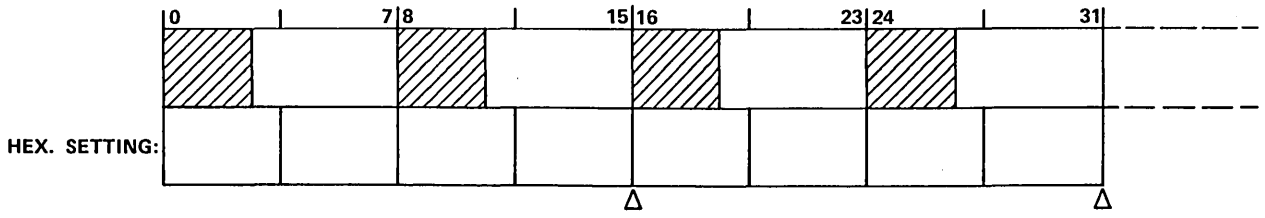
Bit	Description
32	Channel 17
33	(Not used)
34	Channel 15
35	(Not used)
36	Channel 13
37	Channel 12
38	Channel 11
39	Channel 10
40	Channel 27
41	Channel 26
42	Channel 25
43	Channel 24
44	Channel 23
45	Channel 22
46	Channel 21
47	Channel 20
48	(Not used)
49	(Not used)
50	(Not used)
51	(Not used)
52	Channel 33
53	Channel 32
54	Channel 31
55	Channel 30
56	(Not used)
57	(Not used)
58	(Not used)
59	Radial interface 5, 6 (835 through 990), not used (810 through 830)
60	Radial interface 3, 4 (835 through 990), not used (810 through 830)
61	Radial interface 1, 2 (835 through 990), not used (810 through 830)
62	Two-port multiplexer
63	CC545 controller

IOU-810 THROUGH 990 EC REGISTER (30)



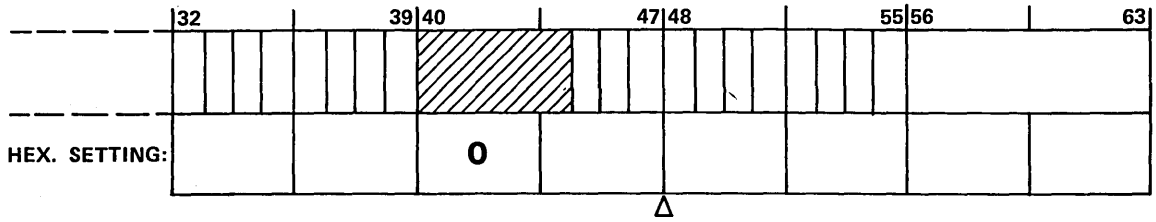
Bit	Description
00 through 31	(Not used)
32	(Not used)
33	(Not used)
34	Auto mode (IOU-835 through 990)
35	Peripheral processor number
36	Peripheral processor number
37	Peripheral processor number
38	Peripheral processor number
39	Peripheral processor number
40	(Not used)
41	(Not used)
42	(Not used)
43	Channel number
44	Channel number
45	Channel number
46	Channel number
47	Channel number
48	(Not used)
49	(Not used)
50	(Not used)
51	Load mode
52	Dump mode
53	Idle mode
54	Register select } A, P, Q, K
55	Register select }
56	Pulse width margin, wide } (IOU-835 through 990 only)
57	Pulse width margin, narrow }
58	Enable deadstart/dump/idle
59	Enable test mode
60	Enable operating system bounds checking
61	Enable (R) + (A) to PP memory
62	(Not used)
63	Enable error stop

IOU-810 THROUGH 990 FS1 REGISTER (80)



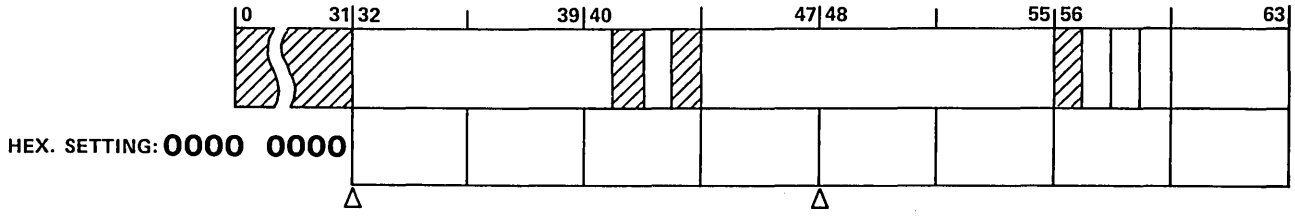
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	Error, Barrel 0 PP4 (IOU-810 through 990)
04	Error, Barrel 0 PP3 (IOU-810 through 990)
05	Error, Barrel 0 PP2 (IOU-810 through 990)
06	Error, Barrel 0 PP1 (IOU-810 through 990)
07	Error, Barrel 0 PP0 (IOU-810 through 990)
08	(Not used)
09	(Not used)
10	(Not used)
11	Error, B0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 990)
12	Error, B0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 990)
13	Error, B0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 990)
14	Error, B0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 990)
15	Error, B0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 990)
16	(Not used)
17	(Not used)
18	(Not used)
19	Error, B1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 990)
20	Error, B1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 990)
21	Error, B1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 990)
22	Error, B1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 990)
23	Error, B1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 990)
24	(Not used)
25	(Not used)
26	(Not used)
27	Error, B1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 990)
28	Error, B1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 990)
29	Error, B1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 990)
30	Error, B1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 990)
31	Error, B1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 990)

IOU-810 THROUGH 990 FS1 REGISTER (80)



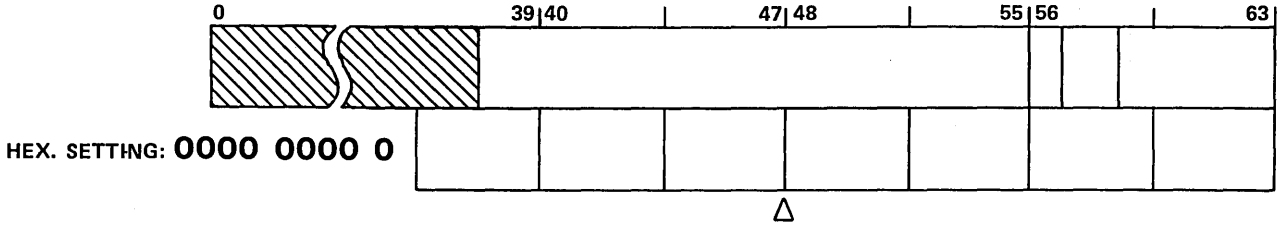
Bit	Description
32	Error on A/R (IOU-815, 825), on CL pak (IOU-810, 830), on 7VDO (IOU-835 through 990)
33	Error on P/Q (IOU-815, 825), on CR pak (IOU-810, 830), on 7VEO (IOU-835 through 990)
34	Firmware error (on CP pak for IOU-810, 830)
35	PP memory data-out error (IOU-815, 825, 835 through 990), error on CM pak (IOU-810, 830)
36	Error in ADU (IOU-815, 825), on CP pak (IOU-810, 830), on 7VGO (IOU-835 through 990)
37	12/16 Conversion error (IOU-815, 825), on CP pak (IOU-810, 830), on 7VJO (IOU-835 through 990)
38	PP memory address error (IOU-815, 825, 835 through 990)
39	PP memory data-in error (on CM pak for IOU-810, 830)
40	(Not used)
41	(Not used)
42	(Not used)
43	(Not used)
44	(Not used)
45	Operating system bounds violation
46	Operating system bounds address parity error
47	ADU barrel priority, ROM parity error (IOU-835 through 990), not used (IOU-810 through 830)
48	CM data-out error (IOU-810, 830), CM read-buffer error (IOU-835 through 990), not used (IOU-815, 825)
49	Uncorrected CM read error
50	Uncorrected CM write error
51	CM reject
52	Input CM tag error (IOU-835 through 990), CM tag-out error (IOU-810 through 830)
53	CM response code error
54	CM data-in error (IOU-815, 825), CM data-out error (IOU-810, 830, 835 through 990)
55	CM address-out error (IOU-835 through 990), not used (IOU-810 through 830)
56	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 0
57	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 1
58	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 2
59	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 3
60	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 4
61	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 5
62	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 6
63	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 990), byte 7

IOU-810 THROUGH 990 FS2 REGISTER (81)



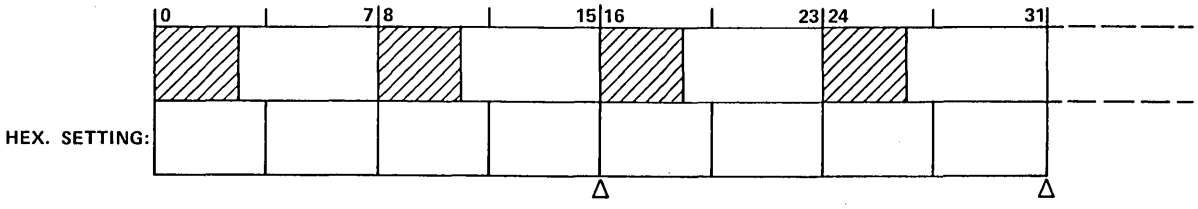
Bit	Description
00 through 31	(Not used)
32	Error, channel 7
33	Error, channel 6
34	Error, channel 5
35	Error, channel 4
36	Error, channel 3
37	Error, channel 2
38	Error, channel 1
39	Error, channel 0
40	Error, channel 17
41	(Not used)
42	Error, channel 15
43	(Not used)
44	Error, channel 13
45	Error, channel 12
46	Error, channel 11
47	Error, channel 10
48	Error, channel 27
49	Error, channel 26
50	Error, channel 25
51	Error, channel 24
52	Error, channel 23
53	Error, channel 22
54	Error, channel 21
55	Error, channel 20
56	(Not used)
57	Radial interface 5/6 (IOU-835 through 990), not used (IOU-810 through 830)
58	Radial interface 3/4 (IOU-835 through 990), not used (IOU-810 through 830)
59	Radial interface 1/2 (IOU-835 through 990), 2/3 (IOU-810 through 830)
60	Error, channel 33
61	Error, channel 32
62	Error, channel 31
63	Error, channel 30

IOU-810 THROUGH 990 STATUS REGISTER (40)



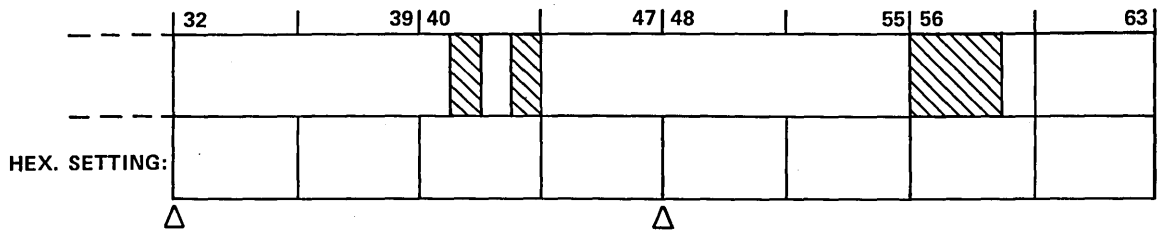
Bit	Description
00 through 37	(Not used)
38 through 55	Internal register (A, P, Q, K)
56	LDS bit
57	Timing margin - fast (IOU-835 through 990)
58	Timing margin - slow (IOU-835 through 990)
59	Barrel reconfiguration (IOU-810 through 990)
60	PP reconfiguration (IOU-810 through 830), barrel reconfiguration (IOU-835 through 990)
61	PP reconfiguration (IOU-810 through 990)
62	PP reconfiguration (IOU-810 through 990)
63	PP reconfiguration (IOU-810 through 990)

IOU-810 THROUGH 990 FAULT STATUS MASK (18)



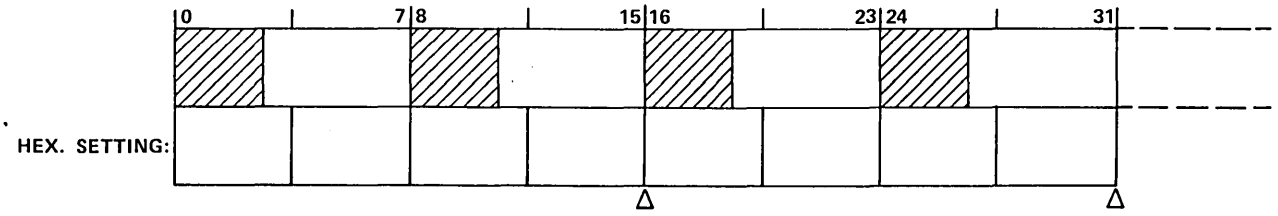
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	Mask vector, Barrel 0 PP4 (IOU-810 through 990)
04	Mask vector, Barrel 0 PP3 (IOU-810 through 990)
05	Mask vector, Barrel 0 PP2 (IOU-810 through 990)
06	Mask vector, Barrel 0 PP1 (IOU-810 through 990)
07	Mask vector, Barrel 0 PP0 (IOU-810 through 990)
08	(Not used)
09	(Not used)
10	(Not used)
11	Mask vector, B0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 990)
12	Mask vector, B0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 990)
13	Mask vector, B0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 990)
14	Mask vector, B0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 990)
15	Mask vector, B0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 990)
16	(Not used)
17	(Not used)
18	(Not used)
19	Mask vector, B1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 990)
20	Mask vector, B1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 990)
21	Mask vector, B1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 990)
22	Mask vector, B1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 990)
23	Mask vector, B1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 990)
24	(Not used)
25	(Not used)
26	(Not used)
27	Mask vector, B1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 990)
28	Mask vector, B1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 990)
29	Mask vector, B1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 990)
30	Mask vector, B1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 990)
31	Mask vector, B1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 990)

IOU-810 THROUGH 990 FAULT STATUS MASK (18)



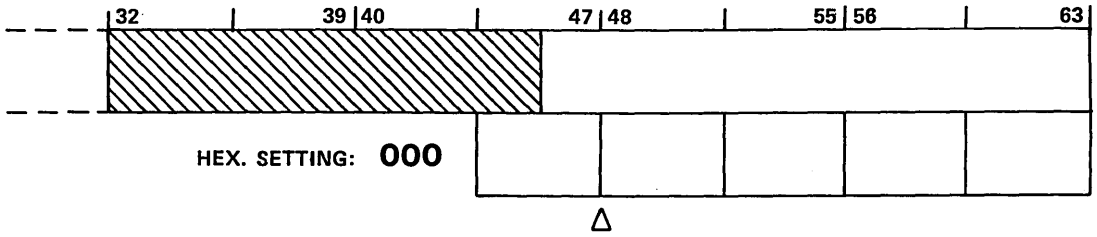
Bit	Description
32	Mask vector, channel 7
33	Mask vector, channel 6
34	Mask vector, channel 5
35	Mask vector, channel 4
36	Mask vector, channel 3
37	Mask vector, channel 2
38	Mask vector, channel 1
39	Mask vector, channel 0
40	Mask vector, channel 17
41	(Not used)
42	Mask vector, channel 15
43	(Not used)
44	Mask vector, channel 13
45	Mask vector, channel 12
46	Mask vector, channel 11
47	Mask vector, channel 10
48	Mask vector, channel 27
49	Mask vector, channel 26
50	Mask vector, channel 25
51	Mask vector, channel 24
52	Mask vector, channel 23
53	Mask vector, channel 22
54	Mask vector, channel 21
55	Mask vector, channel 20
56	(Not used)
57	Mask vector, radial interface 5/6 (IOU-835 through 990), not used (IOU-810 through 830)
58	Mask vector, radial interface 3/4 (IOU-835 through 990), not used (IOU-810 through 830)
59	Mask vector, radial interface 2/3 (IOU-810 through 830), 1/2 (IOU-835 through 990)
60	Mask vector, channel 33
61	Mask vector, channel 32
62	Mask vector, channel 31
63	Mask vector, channel 30

IOU-810 THROUGH 990 OPERATING SYSTEM (OS) BOUNDS REGISTER (21)



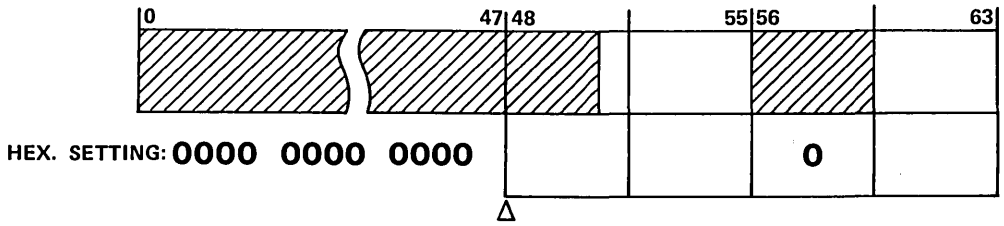
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	Bit vector, Barrel 0, PP4 (IOU-810 through 990)
04	Bit vector, Barrel 0, PP3 (IOU-810 through 990)
05	Bit vector, Barrel 0, PP2 (IOU-810 through 990)
06	Bit vector, Barrel 0, PP1 (IOU-810 through 990)
07	Bit vector, Barrel 0, PP0 (IOU-810 through 990)
08	(Not used)
09	(Not used)
10	(Not used)
11	Bit vector, B0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 990)
12	Bit vector, B0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 990)
13	Bit vector, B0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 990)
14	Bit vector, B0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 990)
15	Bit vector, B0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 990)
16	(Not used)
17	(Not used)
18	(Not used)
19	Bit vector, B1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 990)
20	Bit vector, B1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 990)
21	Bit vector, B1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 990)
22	Bit vector, B1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 990)
23	Bit vector, B1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 990)
24	(Not used)
25	(Not used)
26	(Not used)
27	Bit vector, B1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 990)
28	Bit vector, B1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 990)
29	Bit vector, B1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 990)
30	Bit vector, B1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 990)
31	Bit vector, B1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 990)

IOU-810 THROUGH 990 OPERATING SYSTEM (OS) BOUNDS REGISTER (21)



Bit	Description
32 through 45	(Not used)
46 through 63	Operating system boundary address

IOU-810, 815, 825, 830 TM REGISTER (AO)

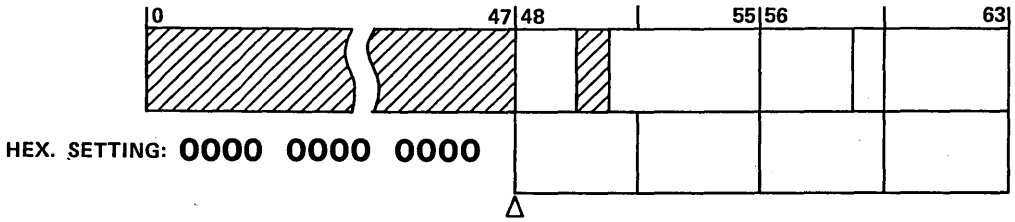


Bit	Description
00 - 50	(Not used)
51	Logical barrel and bits (IOU-810 through 830)
52	Logical PP, 00 through 11 (IOU-810 through 830)
53	Logical PP, 00 through 11 (IOU-810 through 830)
54	Logical PP, 00 through 11 (IOU-810 through 830)
55	Logical PP, 00 through 11 (IOU-810 through 830)
56	(Not applicable)
57	(Not applicable)
58	(Not applicable)
59	Test code (IOU-810, 830) (not available) Not used (IOU-815, 825)
60	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
61	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
62	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
63	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)

Detail, bits 60 through 63 (IOU-815, 825): invert parity

0	(Not used)
1	Invert Y register parity
2	Invert PP to channel parity
3	Invert A register parity at output of A adder and shifter
4	Force error at firmware parity checker
5	Force error at A shifter control ROM parity checker
6	Invert CM function code parity
7	Force zero CM address-in parity (4 bits)
8	Force error at bounds register parity checker
9	Invert Q register parity at output of Q mux
A	Invert CM tag-in parity
B	Force zero CM data-in parity (8 bits)
C	Invert data-out parity (bytes 0 through 7)
D-F	(Not used)

IOU-835, 845, 850, 855, 860, 990 TM REGISTER (AO)



Bit	Description
00 through 47	(Not used)
48	Barrel select (0 barrel 0, 1 barrel 1, 2 barrel 2, 3 barrel 3)
49	Barrel select
50	(Not used)
51	Invert PP parity code
52	Invert PP parity code
53	Invert PP parity code
54	Invert PP parity code
55	Invert PP parity code

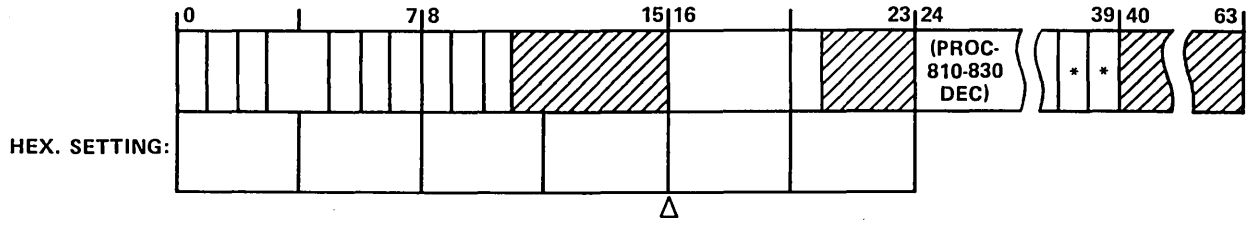
Detail, bits 51 through 55 (IOU-835 through 990): invert parity

1	A-adder input B (PP memory)
2	A-adder input A (A barrel on channel)
3	Shift ROM
4	Firmware ROM (00 through 07)
5	PP memory data to Q-adder (B) or P-incrementor
6	P-incrementor input
7	Q-adder input A (P or Q barrel)
8	Firmware ROM (08 through 15)
9	PP memory data
A	F/W ROM (16 through 35, 46 and 47, 58 through 82)
B	Selected ROM addresses
C	PP memory data
D	R-barrel
E	A-barrel data to R-adder
F	PP memory data
10	Channel data
11	Address to PP memory
12	Data written into PP memory
13	Data to PP memory from CM read buffers
14-1F	(Not used)

56	Force errors in IOU maintenance register
57	Force errors in IOU maintenance register
58	Force errors in IOU maintenance register
59	Invert channel parity
60	Invert parity
61	Invert parity
60	Invert parity
62	Invert parity
63	Invert parity

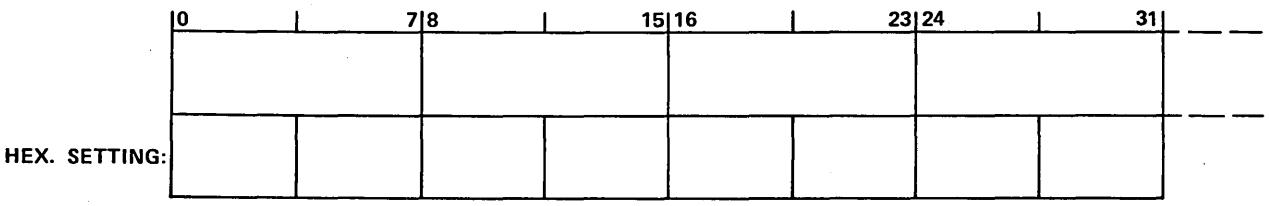
0-7	(Not used)
8	Invert memory FCN code parity
9	Invert mark parity
A	Force ones on address parity
B	Force ones on data parity
C	Invert tag parity
D	Invert write parity ROM parity bit
E	Invert response code parity
F	Invert input data parity

MEM-810, 815, 825, 830 EC REGISTER (20)



Bit	Description
00	Disable parity checking (MEM-815, 825)
01	Disable SEC/DED (MEM-815, 825)
02	Noninterleaved mode (MEM-815, 825)
03	00 Normal
04	01 Write byte 0 10 Read byte 0 11 Read syndrome
05	Micro step (PROC-815, 825)
06	Enable PFS trap (PROC-815, 825)
07	Force even parity
08	Disable C port (MEM-810, 830), P port (MEM-815, 825)
09	Disable D port (MEM-810, 830), I and J ports (MEM-815, 825)
10	Disable M port (MEM-815, 825)
11	(Not used)
12	(Not used)
13	(Not used)
14	(Not used)
15	(Not used)
16	Pulse width margin, UP pak +15 percent
17	Pulse width margin, UP pak -15 percent
18	Pulse width margin, SA pak +15 percent
19	Pulse width margin, SA pak -15 percent
20	Exchange preserve (PROC-815, 825)
21	(Not used)
22	(Not used)
23	(Not used)
24 through 37	(Refer to PROC-810 through 830 DEC register)
38	Suppress corrected error reporting via ports
39	Disable corrected error log
40 through 63	(Not used)

MEM-835, 845, 850, 855, 860, 990 EC REGISTER (20)



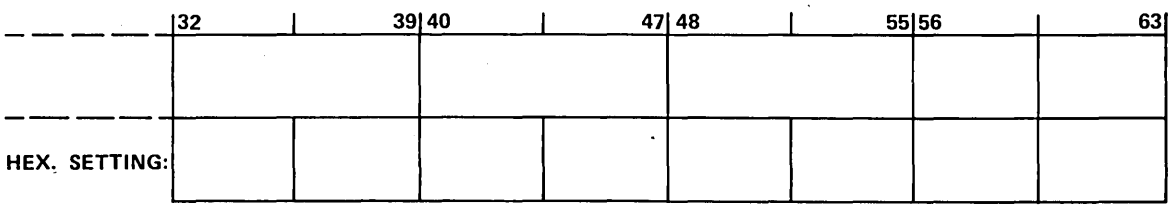
Bit	Description
00	Disable parity checking
01	Disable SECDED
02	Noninterleaved mode
03	Write check/read check/read syndrom bits
04	Write check/read check/read syndrome bits
05	Force address to corrected error log (MEM-990), timing margins (MEM-835 through 860)
06	Not used (MEM-990), timing margins (MEM-835 through 860)
07	Priority port (MEM-835), not used (MEM-845 through 990)

Bits 03 and 04	
00	Normal
01	Write byte 0 to correction byte
10	Read correction byte to byte 0
11	Read syndrome to byte 0

Bits 05 and 06	
00	Normal
01	Narrow
10	Wide
11	Wide

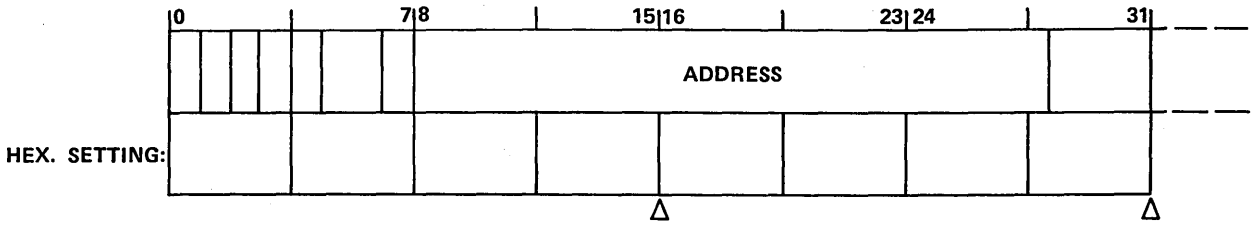
Bit	Description
08 - 15	(Not used)
16	Bit vector for half-speed port 0 (MEM-835), not used (MEM-845 through 990)
17	Bit vector for half-speed port 1 (MEM-835), not used (MEM-845 through 990)
18	Bit vector for half-speed port 2 (MEM-835), not used (MEM-845 through 990)
19	Bit vector for half-speed port 3 (MEM-835), not used (MEM-845 through 990)
20 - 23	(Not used)
24 - 31	(Not used)

MEM-835, 845, 850, 855, 860, 990 EC REGISTER (20)



Bit	Description
32	Bit vector for port 0 disable (MEM-835, 990), CP-0 port (MEM-845 through 860)
33	Bit vector for port 1 disable (MEM-835, 990), CP-1 port (MEM-845 through 860)
34	Bit vector for port 2 disable (MEM-835, 990), standard port (MEM-845 through 860)
35	Bit vector for port 3 disable (MEM-835, 990), IOU port (MEM-845 through 860)
36	(Not used)
37	Disable refresh (MEM-845 through 860), not used (MEM-835, 990)
38	Suppress corrected-error reporting via ports
39	Disable corrected error log entry
40 through 63	(Not used)

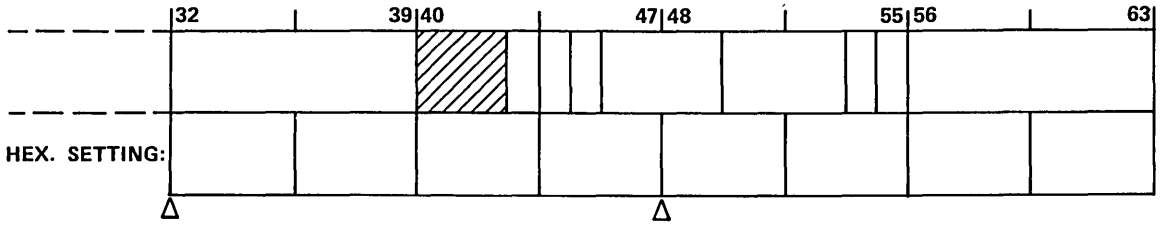
MEM-810, 830 UEL1 REGISTER (A4)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	+Illegal function
03	+Memory bounds fault
04	Partial write error
05	Port code
06	Port code
07	Refresh port
08	(Not used)
09	Address bit 38
10	Address bit 39
11	Address bit 40
12	Address bit 41
13	Address bit 42
14	Address bit 43
15	Address bit 44
16	Address bit 45
17	Address bit 46
18	Address bit 47
19	Address bit 48
20	Address bit 49
21	Address bit 50
22	Address bit 51
23	Address bit 52
24	Address bit 53
25	Address bit 54
26	Address bit 55
27	Address bit 56
28	Address bit 57
29	Address bit 58
30	Address bit 59
31	Address bit 60

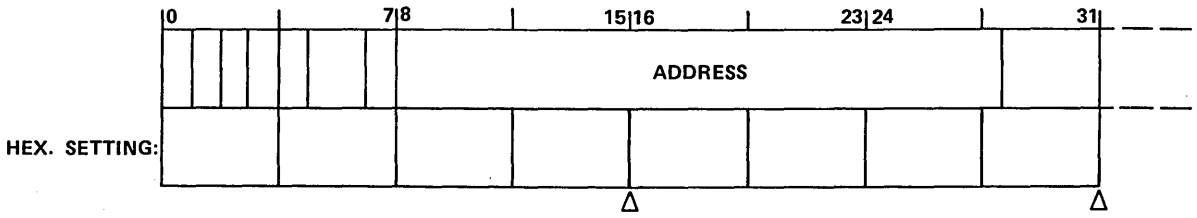
Port code	
00	-
01	CP-1
10	I/O
11	CP-0

MEM-810, 830 UEL1 REGISTER (A4)



Bit	Description
32	Data-in parity error, pak DD1
33	Data-in parity error, pak DD2
34	Data-in parity error, pak DD3
35	Data-in parity error, pak DD4
36	(Not used)
37	(Not used)
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	(Not used)
43	+Tag-in parity error
44	+Function parity error
45	+Mark parity error
46	+Address parity error 4
47	+Address parity error 5
48	+Address parity error 6
49	+Address parity error 7
50	Function code associated with uncorrectable error
51	Function code associated with uncorrectable error
52	Function code associated with uncorrectable error
53	Function code associated with uncorrectable error
54	Function code parity
55	Mark bits parity
56	Mark bits associated with uncorrectable error
57	Mark bits associated with uncorrectable error
58	Mark bits associated with uncorrectable error
59	Mark bits associated with uncorrectable error
60	Mark bits associated with uncorrectable error
61	Mark bits associated with uncorrectable error
62	Mark bits associated with uncorrectable error
63	Mark bits associated with uncorrectable error

MEM-815, 825 UEL1 REGISTER (A4)

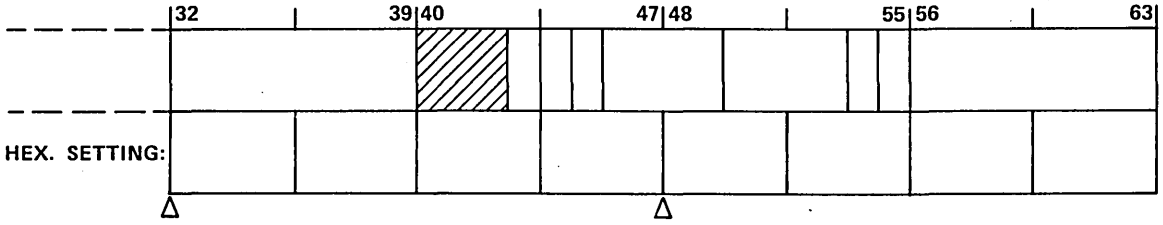


Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	+Illegal function
03	+Memory bounds fault
04	Partial write error
05	Port code
06	Port code
07	Refresh port
08	Address bit 40
09	Address bit 41
10	Address bit 42
11	Address bit 43
12	Address bit 44
13	Address bit 45
14	Address bit 46
15	Address bit 47
16	Address bit 48
17	Address bit 49
18	Address bit 50
19	Address bit 51
20	Address bit 52
21	Address bit 53
22	Address bit 54
23	Address bit 55
24	Address bit 56
25	Address bit 57
26	Address bit 58
27	Address bit 59
28	Address bit 60
29	Address bit P5
30	Address bit P6
31	Address bit P7

Port code (05, 06) →

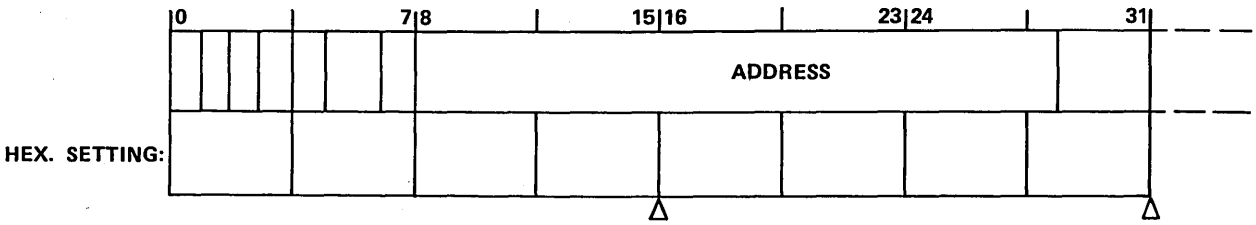
00	J port
01	M port
10	I port
11	O port

MEM-815, 825 UEL1 REGISTER (A4)



Bit	Description
32	+Write data parity error, byte 0
33	+Write data parity error, byte 1
34	+Write data parity error, byte 2
35	+Write data parity error, byte 3
36	+Write data parity error, byte 4
37	+Write data parity error, byte 5
38	+Write data parity error, byte 6
39	+Write data parity error, byte 7
40	(Not used)
41	(Not used)
42	(Not used)
43	+Tag-in parity error
44	+Function parity error
45	+Mark parity error
46	+Address parity error 4
47	+Address parity error 5
48	+Address parity error 6
49	+Address parity error 7
50	Function code associated with uncorrectable error
51	Function code associated with uncorrectable error
52	Function code associated with uncorrectable error
53	Function code associated with uncorrectable error
54	Function code parity
55	Mark bits parity
56	Mark bits associated with uncorrectable error
57	Mark bits associated with uncorrectable error
58	Mark bits associated with uncorrectable error
59	Mark bits associated with uncorrectable error
60	Mark bits associated with uncorrectable error
61	Mark bits associated with uncorrectable error
62	Mark bits associated with uncorrectable error
63	Mark bits associated with uncorrectable error

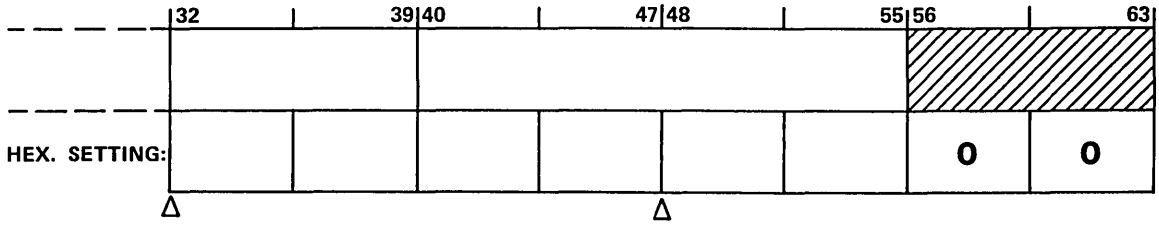
MEM-810, 830 UEL2 REGISTER (A8)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	Data-out path parity error
03	SECDED double bit error
04	+Tag-out parity error
05	Port code
06	Port code
07	Refresh code
08	(Not used)
09	Address bit 38
10	Address bit 39
11	Address bit 40
12	Address bit 41
13	Address bit 42
14	Address bit 43
15	Address bit 44
16	Address bit 45
17	Address bit 46
18	Address bit 47
19	Address bit 48
20	Address bit 49
21	Address bit 50
22	Address bit 51
23	Address bit 52
24	Address bit 53
25	Address bit 54
26	Address bit 55
27	Address bit 56
28	Address bit 57
29	Address bit 58
30	Address bit 59
31	Address bit 60

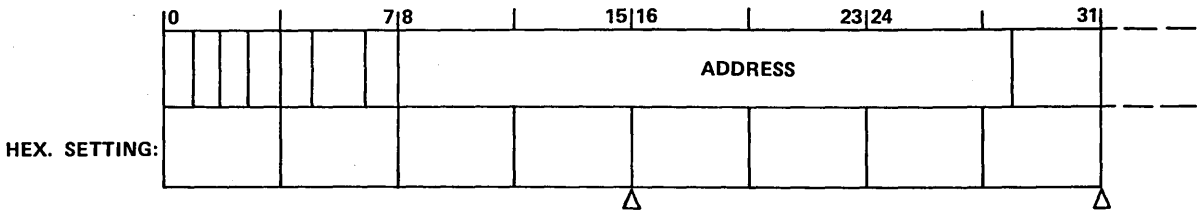
Port code	
00	-
01	CP-1
10	I/O
11	CP-0

MEM-810, 830 UEL2 REGISTER (A8)



Bit	Description
32	+Data-out path parity error, byte 0
33	+Data-out path parity error, byte 1
34	+Data-out path parity error, byte 2
35	+Data-out path parity error, byte 3
36	+Data-out path parity error, byte 4
37	+Data-out path parity error, byte 5
38	+Data-out path parity error, byte 6
39	+Data-out path parity error, byte 7
40 through 55	Reserved for external port buffer error detection
56 through 63	(Not used)

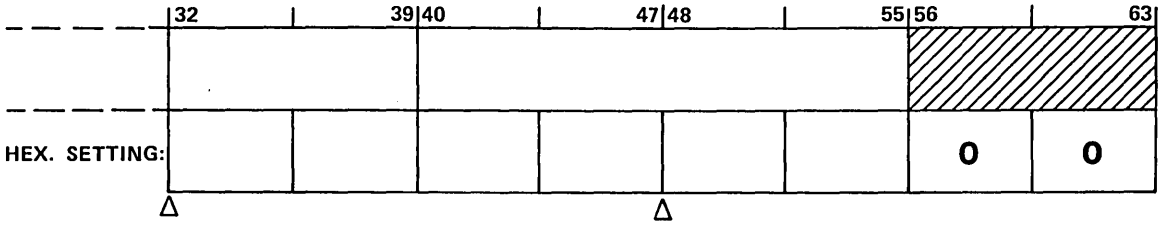
MEM-815, 825 UEL2 REGISTER (A8)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	Data-out path parity error
03	SECDED double bit error
04	+Tag-out parity error
05	Port code
06	Port code
07	Refresh port
08	Address bit 40
09	Address bit 41
10	Address bit 42
11	Address bit 43
12	Address bit 44
13	Address bit 45
14	Address bit 46
15	Address bit 47
16	Address bit 48
17	Address bit 49
18	Address bit 50
19	Address bit 51
20	Address bit 52
21	Address bit 53
22	Address bit 54
23	Address bit 55
24	Address bit 56
25	Address bit 57
26	Address bit 58
27	Address bit 59
28	Address bit 60
29	Address bit P5
30	Address bit P6
31	Address bit P7

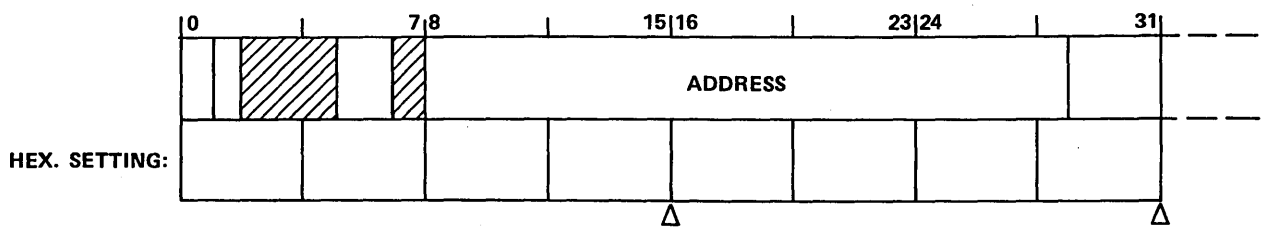
Port code	
00	J port
01	M port
10	I port
11	C port

MEM-815, 825 UEL2 REGISTER (A8)



Bit	Description
32	+Data-out path parity error, byte 0
33	+Data-out path parity error, byte 1
34	+Data-out path parity error, byte 2
35	+Data-out path parity error, byte 3
36	+Data-out path parity error, byte 4
37	+Data-out path parity error, byte 5
38	+Data-out path parity error, byte 6
39	+Data-out path parity error, byte 7
40 through 55	Reserved for external port buffer error detection
56 through 63	(Not used)

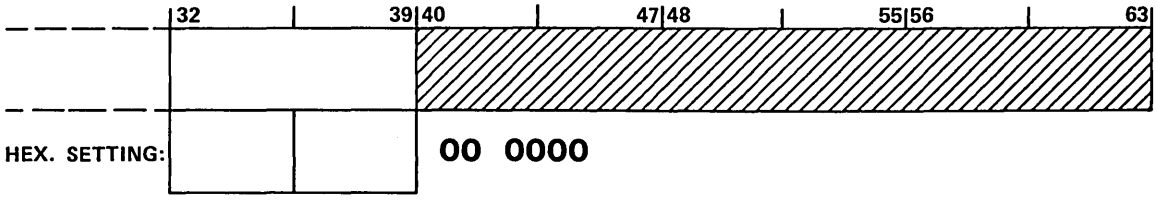
MEM-810, 830 CEL REGISTER (AO)



Bit	Description
00	Valid bit
01	Unlogged corrected error
02	(Not used)
03	(Not used)
04	(Not used)
05	Port code
06	Port code
07	(Not used)
08	(Not used)
09	Address bit 38
10	Address bit 39
11	Address bit 40
12	Address bit 41
13	Address bit 42
14	Address bit 43
15	Address bit 44
16	Address bit 45
17	Address bit 46
18	Address bit 47
19	Address bit 48
20	Address bit 49
21	Address bit 50
22	Address bit 51
23	Address bit 52
24	Address bit 53
25	Address bit 54
26	Address bit 55
27	Address bit 56
28	Address bit 57
29	Address bit 58
30	Address bit 59
31	Address bit 60

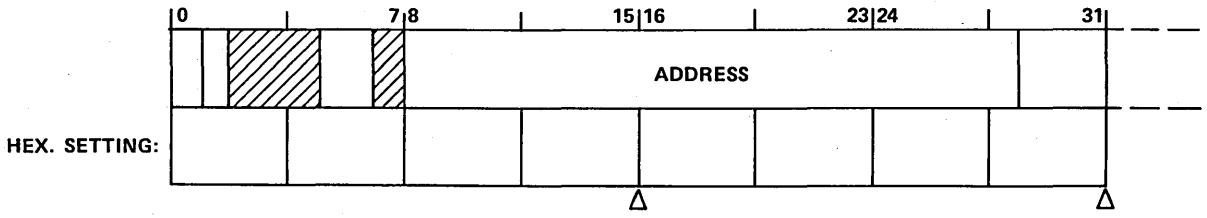
Port code	
00	-
01	CP-0
10	I/O
11	CP-1

MEM-810, 830 CEL REGISTER (AO)



Bit	Description
32	Syndrome bit 0
33	Syndrome bit 1
34	Syndrome bit 2
35	Syndrome bit 3
36	Syndrome bit 4
37	Syndrome bit 5
38	Syndrome bit 6
39	Syndrome bit 7

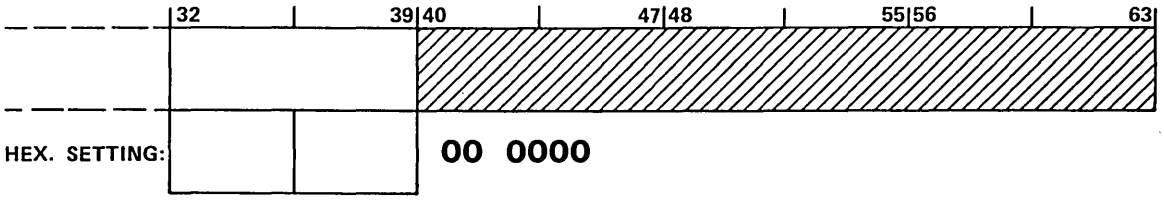
MEM-815, 825 CEL REGISTER (AO)



Bit	Description
00	Valid bit
01	Unlogged corrected error
02	(Not used)
03	(Not used)
04	(Not used)
05	Port code
06	Port code
07	(Not used)
08	Address bit 40
09	Address bit 41
10	Address bit 42
11	Address bit 43
12	Address bit 44
13	Address bit 45
14	Address bit 46
15	Address bit 47
16	Address bit 48
17	Address bit 49
18	Address bit 50
19	Address bit 51
20	Address bit 52
21	Address bit 53
22	Address bit 54
23	Address bit 55
24	Address bit 56
25	Address bit 57
26	Address bit 58
27	Address bit 59
28	Address bit 60
29	Address bit P5
30	Address bit P6
31	Address bit P7

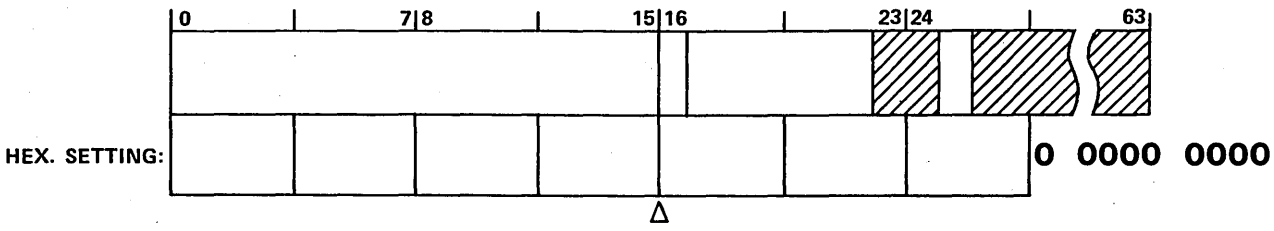
Port code (05, 06):
- 00 J port
- 01 M port
- 10 I port
- 11 C port

MEM-815, 825 CEL REGISTER (AO)



Bit	Description
32	Syndrome bit 0
33	Syndrome bit 1
34	Syndrome bit 2
35	Syndrome bit 3
36	Syndrome bit 4
37	Syndrome bit 5
38	Syndrome bit 6
39	Syndrome bit 7

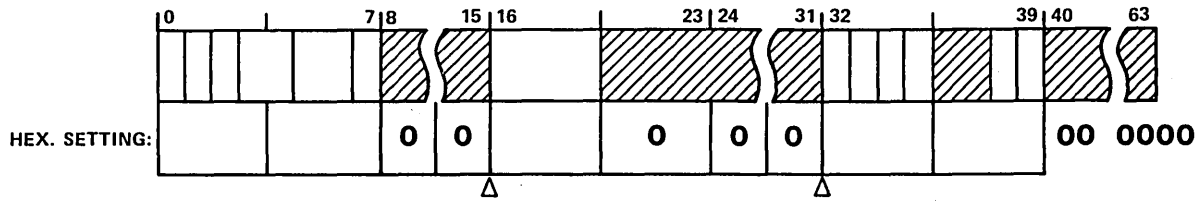
MEM-810 THROUGH 990 0I REGISTERS (12)



Bit	Description	Column A: Bit 12 = 0	Column B: Bit 12 = 1
00	Memory installed:	1MB	2048 MB
01	Memory installed:	2MB	1024 MB
02	Memory installed:	3MB	512 MB
03	Memory installed:	4MB	256 MB
04	Memory installed:	5MB	128 MB
05	Memory installed:	6MB	64 MB
06	Memory installed:	7MB	32 MB
07	Memory installed:	8MB	16 MB
08	Memory installed:	10MB	8 MB
09	Memory installed:	12MB	4 MB
10	Memory installed:	14MB	2 MB
11	Memory installed:	16MB	1 MB
12	Memory installed control bit*	-	-
13	Model-dependent options		
14	Model-dependent options		
15	Model-dependent options		
16	Any memory configuration switch up		
17	Memory configuration switch SW1		
18	Memory configuration switch SW2		
19	Memory configuration switch SW3		
20	Memory configuration switch SW4		
21	Memory configuration switch SW5		
22	Memory configuration switch SW6		
23	(Reserved)		
24	(Not used)		
25	External port installed (MEM-815, 825 only)		
26 through 63	(Not used)		

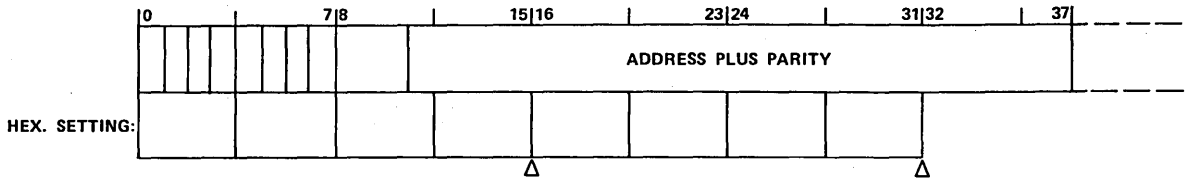
* If bit 12 = 0, interpret bits 0 through 11 as shown in column A.
  If bit 12 = 1, interpret bits 0 through 11 as shown in column B.

MEM-835, 845, 850, 855, 860, 990 EC REGISTER (20)



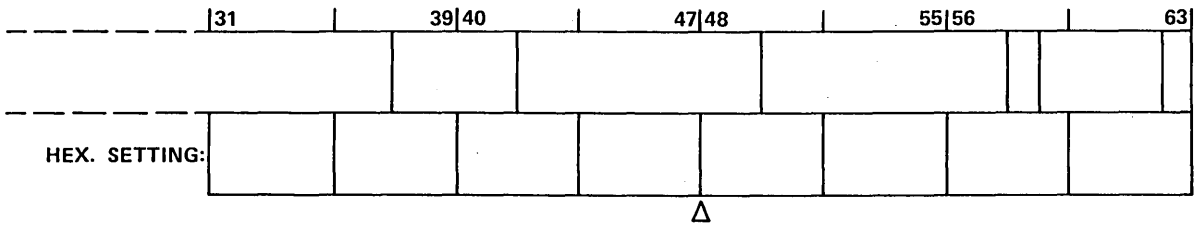
Bit	Description
00	Disable parity checking
01	Disable SECDED
02	Noninterleaved mode
03	00 Normal 01 Write byte 0
04	10 Read byte 0 11 Read syndrome
05	Timing margins (MEM-835 through 860) 00 Normal 01 Narrow 10 Wide 11 Wide Force address to corrected error log (MEM-990)
06	Timing margins (MEM-835 through 860) (refer to bit 05) Not used (MEM-990)
07	Priority port (MEM-835 only)
08 through 15	(Not used)
16	Bit vector for half-speed port 0 (MEM-835 only)
17	Bit vector for half-speed port 1 (MEM-835 only)
18	Bit vector for half-speed port 2 (MEM-835 only)
19	Bit vector for half-speed port 3 (MEM-835 only)
20 through 31	(Not used)
32	Bit vector for port 0 disable (MEM-835, 990), CP-0 (MEM-845 through 860)
33	Bit vector for port 1 disable (MEM-835, 990), CP-1 (MEM-845 through 860)
34	Bit vector for port 2 disable (MEM-835, 990), standard port (MEM-845 through 860)
35	Bit vector for port 3 disable (MEM-835, 990), IOU (MEM-845 through 860)
36	(Not used)
37	Disable refresh (MEM-845 through 860 only)
38	Suppress corrected error reporting to ports
39	Disable corrected error log
40 through 63	(Not used)

MEM-835, 845, 850, 855, 860 UEL1 REGISTER (A4 THROUGH A7)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	Illegal function (MEM-835, 845, 855), multiple-bit memory error (MEM-850, 860)
03	Multiple-bit error (MEM-835, 845, 855), CMC parity error (MEM-850, 860)
04	Memory bounds fault (MEM-835, 845, 855), CSU parity error (MEM-850, 860)
05	1st level parity error (MEM-835), CMC parity error (MEM-845, 855), port number (MEM-850, 860) (same as CEL and UEL2)
06	2nd level parity error (MEM-835), CSU parity error (MEM-845, 855), port number (MEM-850, 860) (same as CEL and UEL2)
07	Common memory request from port buffer (MEM-835), common memory address bit 01 (MEM-845, 855), port number (MEM-850, 860) (same as CEL and UEL2)
08	Port number (MEM-835, 845, 855) (same as CEL and UEL2), address plus parity (MEM-850, 860)
09	Port number (MEM-835, 845, 855) (same as CEL and UEL2), address plus parity (MEM-850, 860)
10	Port number (MEM-835, 845, 855) (same as CEL and UEL2), address plus parity (MEM-850, 860)
11	Address plus parity, (Not used)
12	Address plus parity, (Not used)
13	Address plus parity, array pak select
14	Address plus parity, array pak select
15	Address plus parity, chip row select
16	Address plus parity, chip row select
17	Address plus parity, chip column address
18	Address plus parity, chip column address
19	Address plus parity, chip column address
20	Address plus parity, chip column address
21	Address plus parity, chip column address
22	Address plus parity, chip column address
23	Address plus parity, chip column address
24	Address plus parity, chip row address
25	Address plus parity, chip row address
26	Address plus parity, chip row address
27	Address plus parity, chip row address
28	Address plus parity, chip row address
29	Address plus parity, chip row address
30	Address plus parity, chip row address
31	Address plus parity, bank

MEM-835, 845, 850, 855, 860 UEL1 REGISTER (A4 THROUGH A7)

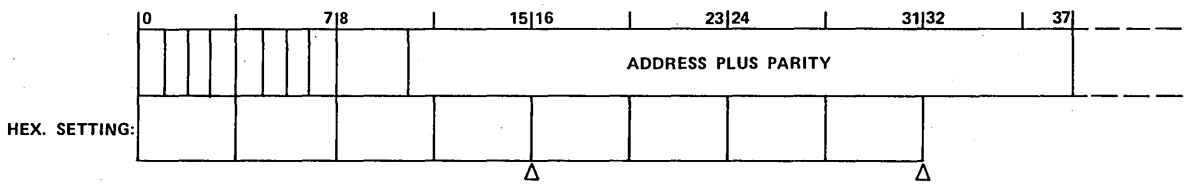


Bit	Description
32	Address plus parity, bank
33	Address plus parity, bank
34	Address plus parity, (not used)
35	Address plus parity, parity 5
36	Address plus parity, parity 6
37	Address plus parity, parity 7
38	Parity error byte position
39	Parity error byte position
40	Parity error byte position
41	Parity error byte position
42	Data-in parity error bits
43	Data-in parity error bits
44	Data-in parity error bits
45	Data-in parity error bits
46	Data-in parity error bits
47	Data-in parity error bits
48	Data-in parity error bits
49	Data-in parity error bits
50	Mark bits
51	Mark bits
52	Mark bits
53	Mark bits
54	Mark bits
55	Mark bits
56	Mark bits
57	Mark bits
58	Mark parity bit
59	Function bits
60	Function bits
61	Function bits
62	Function bits
63	Function parity bit

Bits 38 - 41	MEM-835, 990	MEM-845 - 860
1111	No error	Tag parity error
1110	Function code parity error	Write data byte 7 parity error
1101	Mark parity error	(Not used)
1100	(Not used)	(Not used)
1011	Address byte 5 parity error	(Not used)
1010	Address byte 6 parity error	(Not used)
1001	Address byte 7 parity error	(Not used)
1000	Data byte 0 parity error	(Not used)
0111	Data byte 1 parity error	Address byte 3 parity error
0110	Data byte 2 parity error	Address byte 2 parity error
0101	Data byte 3 parity error	Address byte 1 parity error
0100	Data byte 4 parity error	Address byte 0 parity error
0011	Data byte 5 parity error	(Not used)
0010	Data byte 6 parity error	Mark parity error
0001	Data byte 7 parity error	Function code parity error
0000	Tag parity error	No error

Register No.	Distributor No.
A4	0
A5	1
A6	2
A7	3

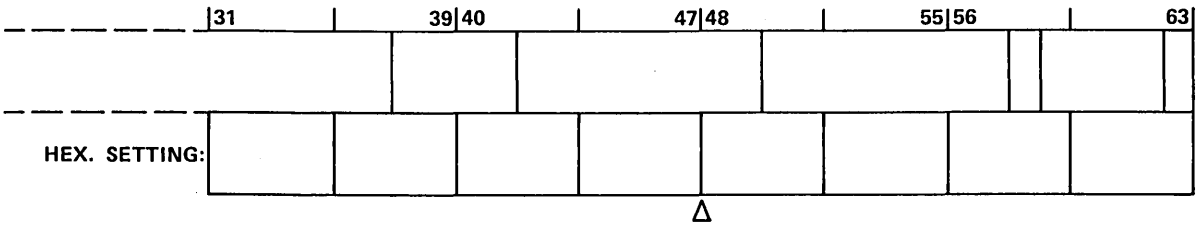
MEM-990 UEL1 REGISTER (A4 THROUGH A7)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	Illegal function
03	Multiple-bit memory error
04	Memory bounds fault
05	(Not used)
06	CSU parity error
07	(Not used)
08	Port number
09	Port number
10	Port number
11	Address plus parity
12	Address plus parity
13	Address plus parity
14	Address plus parity
15	Address plus parity
16	Address plus parity
17	Address plus parity
18	Address plus parity
19	Address plus parity
20	Address plus parity
21	Address plus parity
22	Address plus parity
23	Address plus parity
24	Address plus parity
25	Address plus parity
26	Address plus parity
27	Address plus parity
28	Address plus parity
29	Address plus parity
30	Address plus parity
31	Address plus parity

Bits 8 through 10	Port	Port Code
000	0	CP-0 port B
001	1	CP-0 port A
010	2	CP-0 port C
011	3	Standard port 1
100	4	CP-1 port B
101	5	CP-1 port A
110	6	CP-1 port C
111	7	Standard port 2

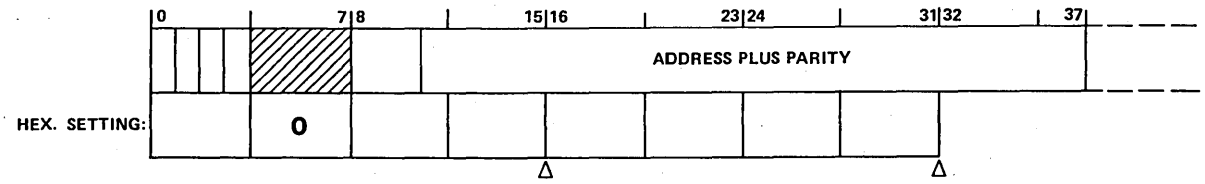
MEM-990 UEL1 REGISTER (A4 THROUGH A7)



Bit	Description
32	Address plus parity
33	Address plus parity
34	Address plus parity
35	Address plus parity
36	Address plus parity
37	Address plus parity
38	Address plus parity
39	(Not used)
40	Write data parity error, bit 0
41	Write data parity error, bit 1
42	Write data parity error, bit 2
43	Write data parity error, bit 3
44	Write data parity error, bit 4
45	Write data parity error, bit 5
46	Write data parity error, bit 6
47	Write data parity error, bit 7
48	Read or partial-write data parity error, bit 0
49	Read or partial-write data parity error, bit 1
50	Read or partial-write data parity error, bit 2
51	Read or partial-write data parity error, bit 3
52	Read or partial-write data parity error, bit 4
53	Read or partial-write data parity error, bit 5
54	Read or partial-write data parity error, bit 6
55	Read or partial-write data parity error, bit 7
56	Address parity error, bit 4
57	Address parity error, bit 5
58	Address parity error, bit 6
59	Address parity error, bit 7
60	Mark parity error
61	Tag parity error
62	Function parity error
63	Partial-write parity error

Register No.	Distributor No.
A4	0
A5	1
A6	2
A7	3

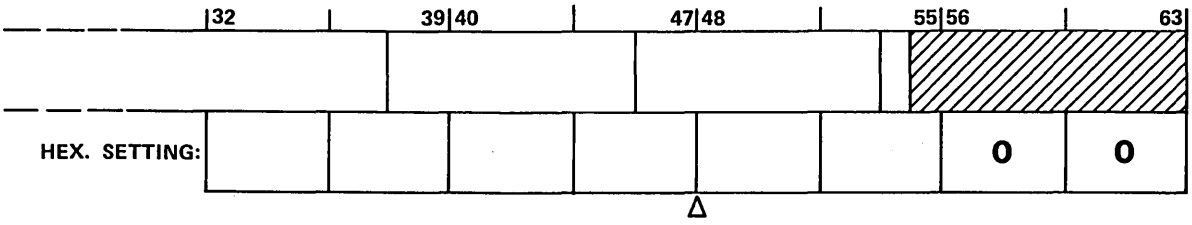
MEM-835, 845, 850, 855, 860, 990 UEL2 REGISTER (A8 THROUGH AB)



Bit	Description
00	Valid bit
01	Unlogged uncorrectable error
02	Partial-write parity error (MEM-835, 845, 855, 990), illegal function (MEM-850, 860)
03	Data-out path parity error (MEM-835, 845, 855, 990), bounds fault (MEM-850, 860)
04	(Not used)
05	Not used (MEM-835, 845, 855, 990), port number (MEM-850, 860)
06	Not used (MEM-835, 845, 855, 990), port number (MEM-850, 860)
07	Not used (MEM-835, 845, 855, 990), port number (MEM-850, 860)
08	Not used (MEM-850, 860), port number (MEM-835, 845, 855, 990)
09	Not used (MEM-850, 860), port number (MEM-835, 845, 855, 990)
10	Not used (MEM-850, 860), port number (MEM-835, 845, 855, 990)
11	Address plus parity, (Not used)
12	Address plus parity, (Not used)
13	Address plus parity, array pak select
14	Address plus parity, array pak select
15	Address plus parity, chip row select
16	Address plus parity, chip row select
17	Address plus parity, chip column address
18	Address plus parity, chip column address
19	Address plus parity, chip column address
20	Address plus parity, chip column address
21	Address plus parity, chip column address
22	Address plus parity, chip column address
23	Address plus parity, chip column address
24	Address plus parity, chip row address
25	Address plus parity, chip row address
26	Address plus parity, chip row address
27	Address plus parity, chip row address
28	Address plus parity, chip row address
29	Address plus parity, chip row address
30	Address plus parity, chip row address
31	Address plus parity, bank

0	Port 0
1	Port 1
2	Port 2
3	Port 3
4	(Not used)
5	(Not used)
6	No request
7	Refresh

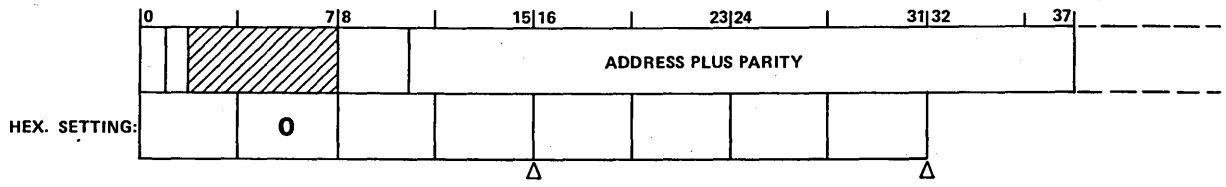
MEM-835, 845, 850, 855, 860, 990 UEL2 REGISTER (A8 THROUGH AB)



Bit	Description
32	Address plus parity, bank
33	Address plus parity, bank
34	Address plus parity, (not used)
35	Address plus parity, parity 5
36	Address plus parity, parity 6
37	Address plus parity, parity 7
38	Data-out path parity error, byte 0
39	Data-out path parity error, byte 1
40	Data-out path parity error, byte 2
41	Data-out path parity error, byte 3
42	Data-out path parity error, byte 4
43	Data-out path parity error, byte 5
44	Data-out path parity error, byte 6
45	Data-out path parity error, byte 7
46	Partial-write parity error, byte 0
47	Partial-write parity error, byte 1
48	Partial-write parity error, byte 2
49	Partial-write parity error, byte 3
50	Data-out path parity error, byte 4
51	Partial-write parity error, byte 5
52	Partial-write parity error, byte 6
53	Partial-write parity error, byte 7
54	Tag parity error (MEM-835, 990 only)
55	(Not used)
56	(Not used)
57	(Not used)
58	(Not used)
59	(Not used)
60	(Not used)
61	(Not used)
62	(Not used)
63	(Not used)

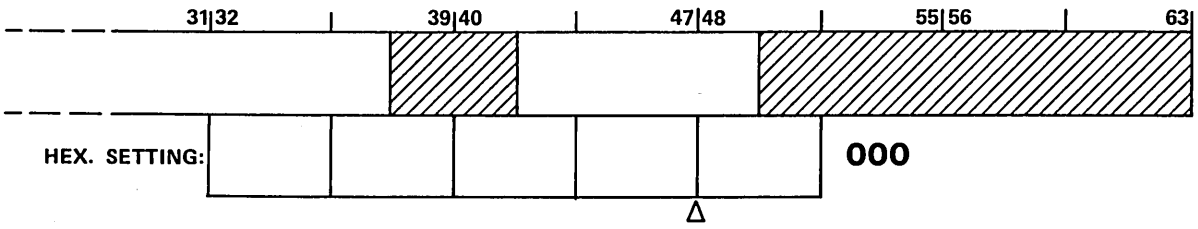
Register No.	Distributor No.
A8	0
A9	1
AA	2
AB	3

MEM-835, 990 CEL REGISTER (A0 THROUGH A3)



Bit	Description		
00	Valid bit		
01	Unlogged corrected error		
02	(Not used)		
03	(Not used)		
04	(Not used)	0	Port 0
05	(Not used)	1	Port 1
06	(Not used)	2	Port 2
07	(Not used)	3	Port 3
		4	(Not used)
08	Port number	5	(Not used)
09	Port number →	6	No request
10	Port number	7	Refresh
11	Address plus parity, (Not used)		
12	Address plus parity, (Not used)		
13	Address plus parity, array pak select		
14	Address plus parity, array pak select		
15	Address plus parity, chip row select		
16	Address plus parity, chip row select		
17	Address plus parity, chip column address		
18	Address plus parity, chip column address		
19	Address plus parity, chip column address		
20	Address plus parity, chip column address		
21	Address plus parity, chip column address		
22	Address plus parity, chip column address		
23	Address plus parity, chip column address		
24	Address plus parity, chip row address		
25	Address plus parity, chip row address		
26	Address plus parity, chip row address		
27	Address plus parity, chip row address		
28	Address plus parity, chip row address		
29	Address plus parity, chip row address		
30	Address plus parity, chip row address		
31	Address plus parity, bank		

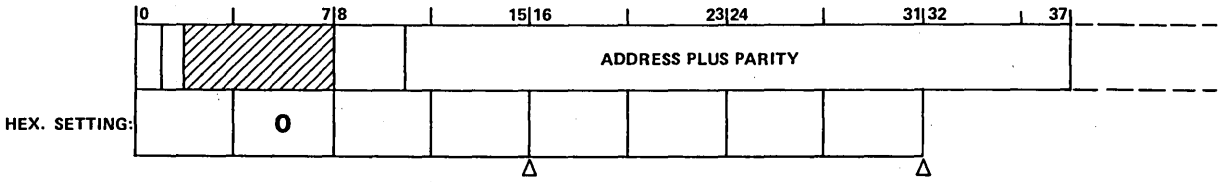
MEM-835, 990 CEL REGISTER (A0 THROUGH A3)



Bit	Description
32	Address plus parity
33	Address plus parity
34	Address plus parity
35	Address plus parity
36	Address plus parity
37	Address plus parity
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	Syndrome bit 0
43	Syndrome bit 1
44	Syndrome bit 2
45	Syndrome bit 3
46	Syndrome bit 4
47	Syndrome bit 5
48	Syndrome bit 6
49	Syndrome bit 7
50	(Not used)
↓	↓
63	(Not used)

Register No.	Distributor No.
A0	0
A1	1
A2	2
A3	3

MEM-845, 850, 855, 860 CEL REGISTER (A0 THROUGH A3)

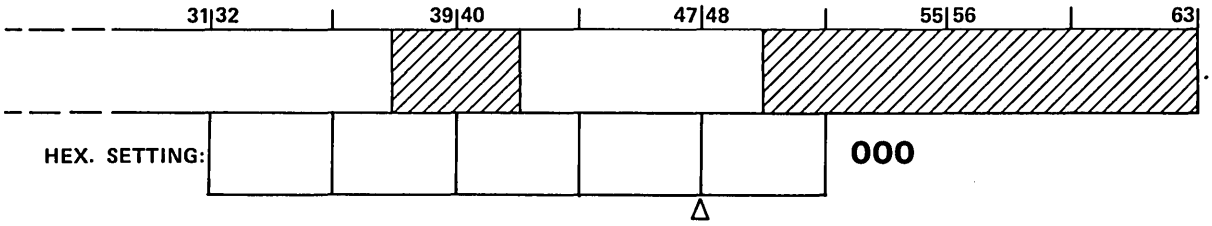


Bit	Description
00	Valid bit
01	Unlogged corrected error
02	(Not used)
03	(Not used)
04	(Not used)
05	Not used (MEM-845, 855), port number (MEM-850, 860) (refer to detail)
06	Not used (MEM-845, 855), port number (MEM-850, 860) (refer to detail)
07	Not used (MEM-845, 855), port number (MEM-850, 860) (refer to detail)
08	Port number (MEM-845, 855) (refer to detail), address plus parity (MEM-850, 860)
09	Port number (MEM-845, 855) (refer to detail), address plus parity (MEM-850, 860)
10	Port number (MEM-845, 855) (refer to detail), address plus parity (MEM-850, 860)
11	Address plus parity
12	Address plus parity
13	Address plus parity
14	Address plus parity
15	Address plus parity
16	Address plus parity
17	Address plus parity
18	Address plus parity
19	Address plus parity
20	Address plus parity
21	Address plus parity
22	Address plus parity
23	Address plus parity
24	Address plus parity
25	Address plus parity
26	Address plus parity
27	Address plus parity
28	Address plus parity
29	Address plus parity
30	Address plus parity
31	Address plus parity

Bits 05 through 07 (Models 850 and 860); Bits 08 through 10 (Models 845 and 855)

	Port
0	CP-0
1	IOU
2	Standard port
3	CP-1
4	(Not used)
5	(Not used)

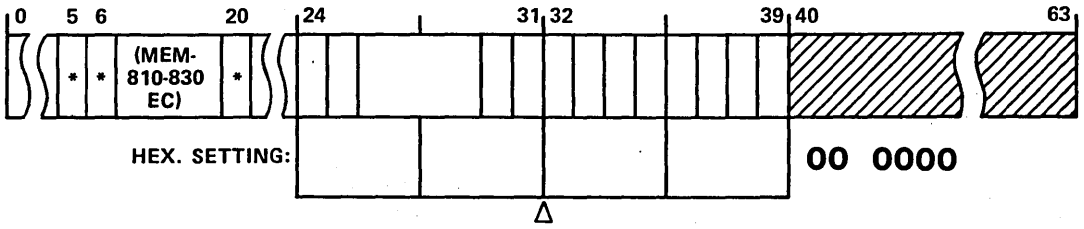
MEM-845, 850, 855, 860 CEL REGISTER (A0 THROUGH A3)



Bit	Description
32	Address plus parity
33	Address plus parity
34	Address plus parity
35	Address plus parity
36	Address plus parity
37	Address plus parity
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	Syndrome bit 0
43	Syndrome bit 1
44	Syndrome bit 2
45	Syndrome bit 3
46	Syndrome bit 4
47	Syndrome bit 5
48	Syndrome bit 6
49	Syndrome bit 7
50	(Not used)
↓	↓
63	(Not used)

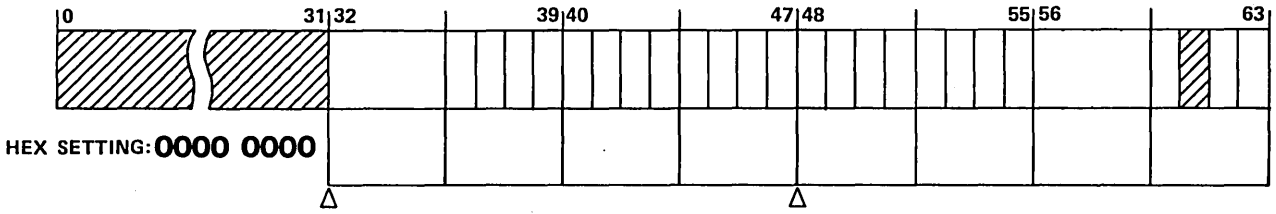
Register No.	Distributor No.
A0	0
A1	1
A2	2
A3	3

PROC-810, 815, 825, 830 DEC REGISTER (30)



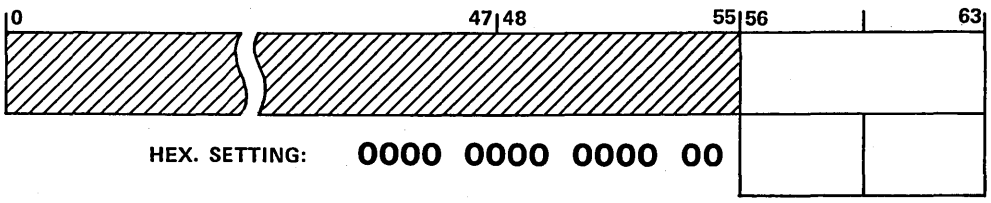
Bit	Description
5	Control store micro-step enabled
6	Processor fault status traps enabled
7	(Not used)
↓	↓
23	(Not used)
24	Processor fault status enabled
25	Map real memory address mode enabled
26	Map file 0 enabled
27	Map file 1 enabled
28	Map file 2 enabled
29	Map file 3 enabled
30	Instruction retry enabled
31	Instruction step enabled
32	Maintenance scan halt enabled
33	Test mode enabled
34	Physical ECS present (never set)
35	Disable corrected error to SS register (MEM-810 through 830)
36	Control store breakpoint enabled
37	Control store sweep enabled
38	Force good response on SBE (MEM-810 through 830)
39	Disable corrected error log (MEM-810 through 830)

PROC-810, 815, 825, 830 PFS0/PFS1 REGISTERS (80/81)



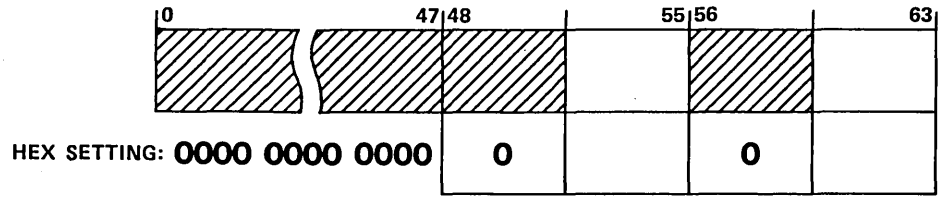
Bit	Description
00 through 31	(Not used)
32	ARVI parity error bits 0 through 7, 32 through 39
33	ARVI parity error bits 8 through 15, 40 through 47
34	ARVI parity error bits 16 through 23, 48 through 55
35	ARVI parity error bits 24 through 31, 56 through 63
36	Uncorrected memory write error
37	Memory reject
38	Memory tag parity error
39	Response code parity error
40	FP exception trap index ROM parity error
41	AD or BD bits 0 through 15 parity error
42	LD box ROM parity error
43	ADS or BDS ROM parity error
44	Shift type ROM parity error or shifter input
45	Uncorrected memory read error
46	AD or BD bits 16 through 31 parity error
47	AD-UN parity error; MAC write parity error
48	Memory response time-out
49	CYBER ROM parity error
50	Instruction parity error
51	XBD ROM parity error
52	AD or BD bits 32 through 47 parity error
53	BDP adder, data ROM, RJB, RKB parity error
54	Immediate ROM
55	AD or BD bits 48 through 63 parity error
56	Map parity error bits 32 through 39
57	Map parity error bits 40 through 47
58	Map parity error bits 48 through 55
59	Map parity error bits 56 through 63
60	Map multiple hit fault
61	(Not used)
62	MAC error
63	Any CS data parity error

PROC-810, 815, 825, 830 MCEL REGISTER (93)



Bit	Parity Error Location
00 through 55	(Not used)
56	File 0, pak location C22, C23, or C24
57	File 0, pak location D1 or D2
58	File 1, pak location C22, C23, or C24
59	File 1, pak location D1 or D2
60	File 2, pak location C22, C23, or C24
61	File 2, pak location D1 or D2
62	File 3, pak location C22, C23, or C24
63	File 3, pak location D1 or D2

PROC-810, 815, 825, 830 PTM REGISTER (A0)



Bit	Description
00 through 47	(Not used)

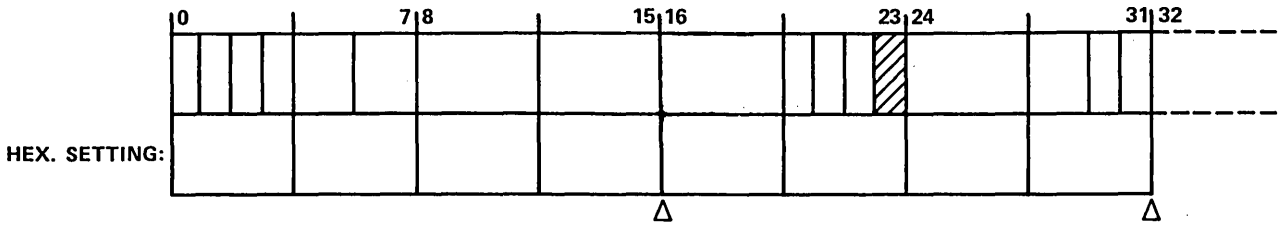
Hexadecimal Code (48 through 63)

0800	Nanocode ROM
0900	Invert memory function parity
0A00	Invert memory tag parity
0B00	Invert memory mark parity
0C00	Invert execution data/address parity, byte 0, 1
0D00	Invert execution data/address parity, byte 2, 3
0E00	Invert execution data/address parity, byte 4, 5
0F00	Invert execution data/address parity, byte 6, 7
0008	(Not used)
0009	Invert floating-point trap index
000A	Invert floating-point trap ROM
000B	Invert MAC bus data parity
000C	Invert adder latch data parity
000D	(Not used)
000E	(Not used)
000F	(Not used)

PROC-810 THROUGH 990 0I REGISTERS (12)

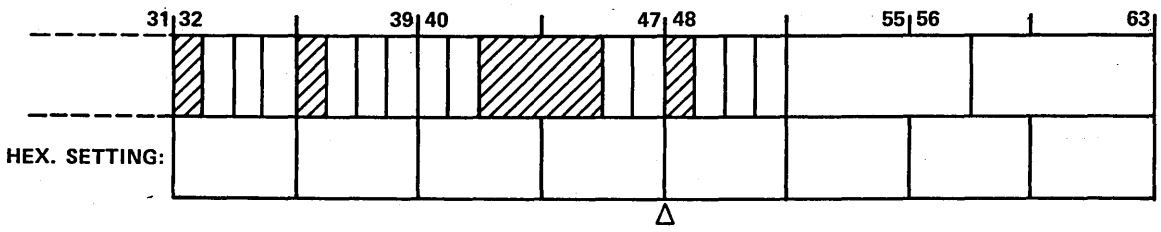
Bit	Description
810, 815, 825, 830	
0 through 28	(Not used)
29	A170 mode option installed
30	(Not used)
31	PMF installed
32 through 63	(Not used)
835	
0 through 59	(Not used)
60	A170 mode option installed
61	32K-byte cache installed
62	Second central memory port installed
63	PMF installed
845, 850, 855, 860	
0 through 60	(Not used)
61	PMF/ECS I/F option installed
62	32K-byte cache installed
63	PMF installed
990	
0 through 61	(Not used)
62	Vector instruction option installed
63	PMF installed

PROC-835 DEC REGISTER (30)



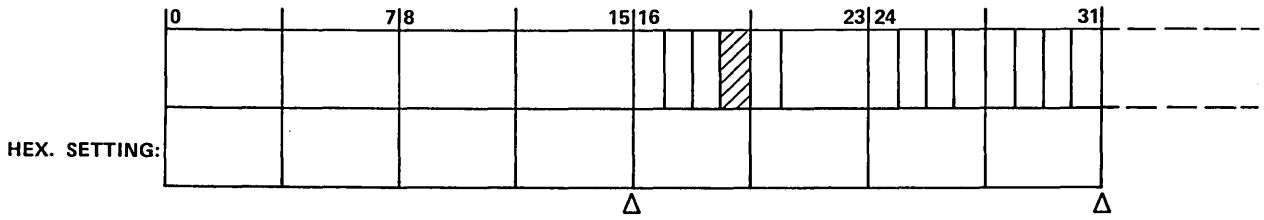
Bit	Description
00	Control store sweep mode selected
01	Micro-step enabled
02	Instruction step enabled
03	Control store breakpoint enabled
04	Memory port 0 enabled
05	Memory port 1 enabled
06	Memory port 0 parity check disabled
07	Memory port 1 parity check disabled
08	Cache enabled: 1st quarter, 0 through 7K
09	Cache enabled: 2nd quarter, 8 through 15K
10	Cache enabled: 3rd quarter, 16 through 23K
11	Cache enabled: 4th quarter, 24 through 32K
12	Cache conflict: register 0 enabled
13	Cache conflict: register 1 enabled
14	Cache conflict: register 2 enabled
15	Cache conflict: register 3 enabled
16	Enable retry diagnostic check
17	Enable deadstart diagnostic check
18	Force page file hit
19	(Not used)
20	Cache CEL logging disabled
21	Map DEL logging disabled
22	Test port number
23	(Not used)
24	Map disable, page buffer 0
25	Map disable, page buffer 1
26	Map disable, page buffer 2
27	Map disable, page buffer 3
28	Map disable, segment/buffer 0
29	Map disable, segment/buffer 1
30	Map RMA mode enabled
31	Lock last translation into map

PROC-835 DEC REGISTER (30)



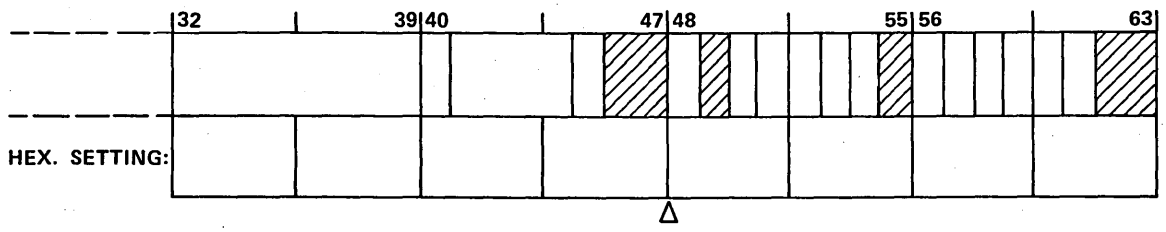
Bit	Description
32	Preserve and disable PP exchanges
33	Test mode enabled
34	Physical ECS present
35	Disable corrected error to status summary register
36	(Not used)
37	Enable memory port select
38	Select memory port
39	Cache allocation on read miss enabled
40	Maintenance scan halt enabled
41	Instruction counter halt enabled
42	(Not used)
43	(Not used)
44	(Not used)
45	(Not used)
46	PFS micro-traps disabled
47	Instruction retry enabled
48	(Not used)
49	Disable cache kill on input parity error
50	Disable register file write kill on parity error
51	Disable port 1 response
52	Force wide margins, panel A
53	Force wide margins, panel B
54	Force wide margins, panel C
55	Force wide margins, panel C
56	Force wide margins, panel D
57	Force wide margins, panel E
58	Force narrow margins, panel A
59	Force narrow margins, panel B
60	Force narrow margins, panel C
61	Force narrow margins, panel C
62	Force narrow margins, panel D
63	Force narrow margins, panel E

PROC-835 PFS0 REGISTER (80)



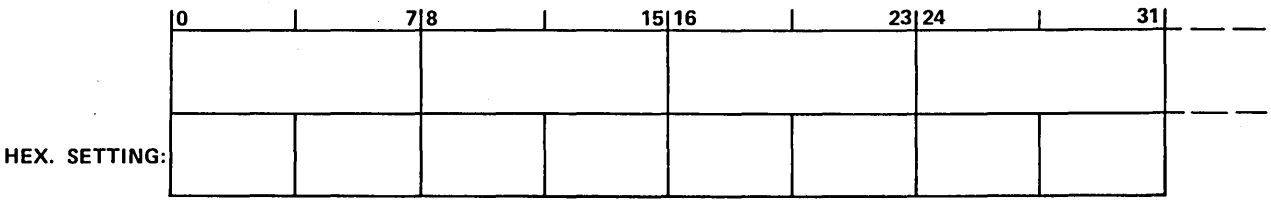
Bit	Description
00	Cache input, bytes 0 and 1, address 0
01	Cache input, bytes 2 and 3, address 1
02	Cache input, bytes 4 and 5, address 2
03	Cache input, bytes 6 and 7, address 3
04	Cache output, bytes 0 and 1
05	Cache output, bytes 2 and 3
06	Cache output, bytes 4 and 5
07	Cache output, bytes 6 and 7
08	Data, port 0, bytes 0 and 1
09	Data, port 0, bytes 2 and 3
10	Data, port 0, bytes 4 and 5
11	Data, port 0, bytes 6 and 7
12	Data, port 1, bytes 0 and 1
13	Data, port 1, bytes 2 and 3
14	Data, port 1, bytes 4 and 5
15	Data, port 1, bytes 6 and 7
16	Identifier/response code, port 0
17	Identifier/response code, port 1
18	Identifier, function, partial-write cache input
19	(Not used)
20	CFR status good
21	Response code = 1 error
22	Response code = 5 error
23	Response code = 7 error
24	Cache ID and CFR empty
25	CFR multiple hit
26	Identifier, cache out
27	Cache time-out
28	No overflow on simultaneous response buffer
29	Function code valid, cache input
30	Incremented ident, cache input
31	MAC ROMS

PROC-835 PFS0 REGISTER (80)



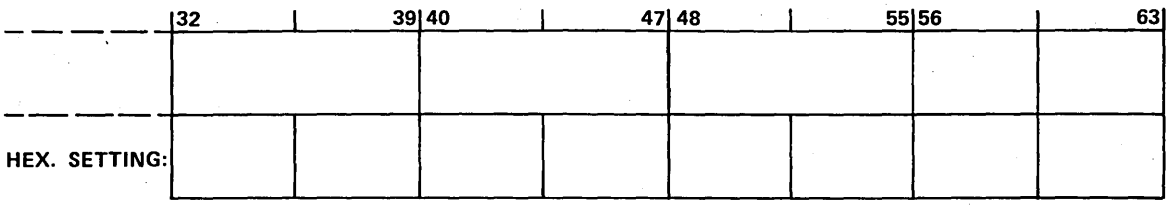
Bit	Description
32	Register file, byte 0
33	Register file, byte 1
34	Register file, byte 2
35	Register file, byte 3
36	Register file, byte 4
37	Register file, byte 5
38	Register file, byte 6
39	Register file, byte 7
40	Segment number
41	I MUX, B MUX address
42	I MUX, B MUX address
43	I MUX, B MUX address
44	I MUX, B MUX address
45	Ring parity
46	Address select ROMs
47	(Not used)
48	Invalidation address, exchange address
49	(Not used)
50	BDP J stream parity error
51	BDP K stream parity error
52	BDP output parity error
53	BDP control to edit
54	BDP branch or CYBER convert ROM
55	(Not used)
56	Floating-point trap ROM
57	Exponent address function address decode
58	ROM and partial write
59	(Not used)
60	Identifier from cache
61	Immediate control ROMS
62	(Not used)
63	(Not used)

PROC-835 PFS-1 REGISTER (81)



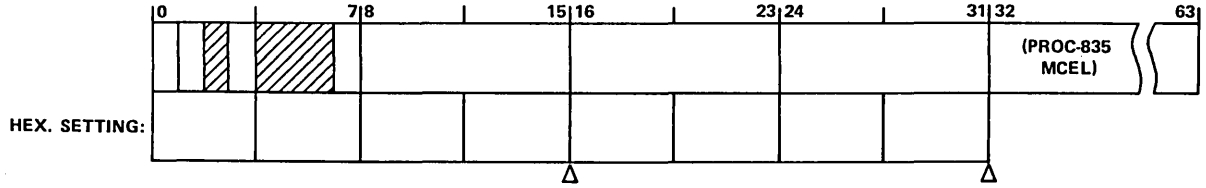
Bit	Description
00	Control store parity error, byte 0
01	(Not used)
02	(Not used)
03	(Not used)
04	(Not used)
05	(Not used)
06	(Not used)
07	(Not used)
08	Control store parity error, byte 1
09	(Not used)
10	(Not used)
11	(Not used)
12	(Not used)
13	(Not used)
14	(Not used)
15	(Not used)
16	Control store parity error, byte 2
17	(Not used)
18	(Not used)
19	(Not used)
20	(Not used)
21	(Not used)
22	(Not used)
23	(Not used)
24	Control store parity error, byte 3
25	(Not used)
26	(Not used)
27	(Not used)
28	(Not used)
29	(Not used)
30	(Not used)
31	(Not used)

PROC-835 PFS1 REGISTER (81)



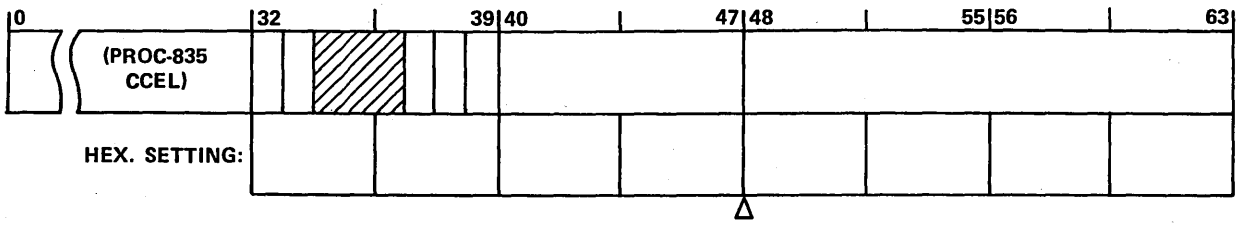
Bit	Description
32	Control store parity error, byte 4
33	(Not used)
34	(Not used)
35	(Not used)
36	(Not used)
37	(Not used)
38	(Not used)
39	(Not used)
40	Control store parity error, byte 5
41	(Not used)
42	(Not used)
43	(Not used)
44	(Not used)
45	(Not used)
46	(Not used)
47	(Not used)
48	Control store parity error, byte 6
49	(Not used)
50	(Not used)
51	(Not used)
52	(Not used)
53	(Not used)
54	(Not used)
55	(Not used)
56	Control store parity error, byte 7
57	(Not used)
58	(Not used)
59	(Not used)
60	(Not used)
61	(Not used)
62	(Not used)
63	(Not used)

PROC-835 CCEL REGISTER (92)



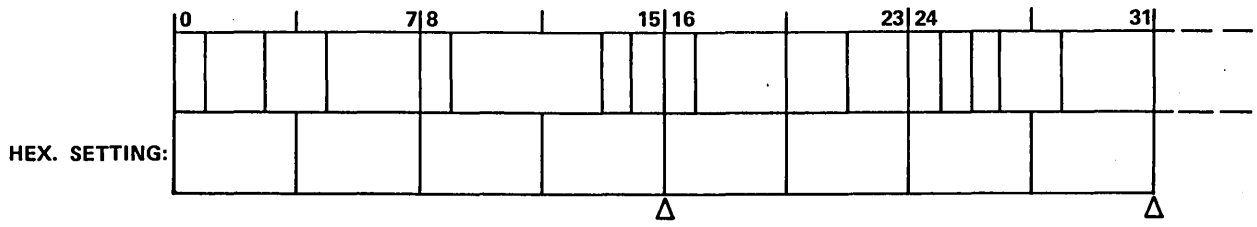
Bit	Description
00	Valid cache CEL entry
01	Unlogged error
02	(Not used)
03	Parity error, LRU status array counters
04	(Not used)
05	(Not used)
06	(Not used)
07	No multiple hit in tag arrays
08	No parity errors, BN in tag array, blocks 0 and 1
09	No parity errors, BN in tag array, blocks 2 and 3
10	No parity errors, BN in tag array, blocks 4 and 5
11	No parity errors, BN in tag array, blocks 6 and 7
12	No parity errors, ASID in tag array, blocks 0 and 1
13	No parity errors, ASID in tag array, blocks 2 and 3
14	No parity errors, ASID in tag array, blocks 4 and 5
15	No parity errors, ASID in tag array, blocks 6 and 7
16	ASID compare, block 0
17	ASID compare, block 1
18	ASID compare, block 2
19	ASID compare, block 3
20	ASID compare, block 4
21	ASID compare, block 5
22	ASID compare, block 6
23	ASID compare, block 7
24	BN compare, block 0
25	BN compare, block 1
26	BN compare, block 2
27	BN compare, block 3
28	BN compare, block 4
29	BN compare, block 5
30	BN compare, block 6
31	BN compare, block 7

PROC-835 MCEL REGISTER (93)



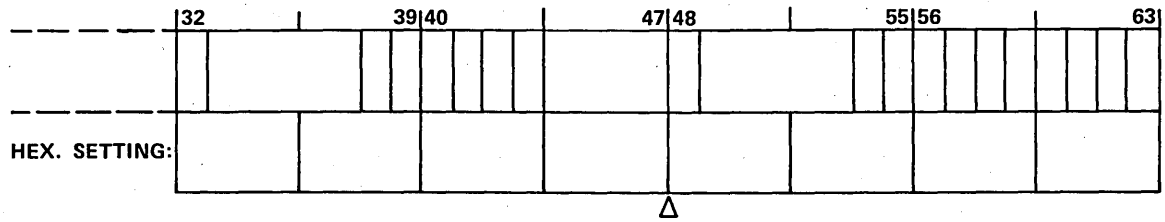
Bit	Description
32	Valid map CEL entry
33	Unlogged error
34	(Not used, always zero)
35	(Not used, always zero)
36	(Not used, always zero)
37	Parity error, segment file tag
38	Multiple hit, segment file
39	Multiple hit, page file
40	Parity error segment, file 0, pak location D06
41	Parity error segment, file 1, pak location D06
42	Parity error segment, file 0, pak location D07
43	Parity error segment, file 1, pak location D07
44	Parity error segment, file 0, pak location D08
45	Parity error segment, file 1, pak location D08
46	Parity error segment, file 0, pak location D09
47	Parity error segment, file 1, pak location D09
48	Parity error page, file 0, pak location D06
49	Parity error page, file 1, pak location D06
50	Parity error page, file 2, pak location D06
51	Parity error page, file 3, pak location D06
52	Parity error page, file 0, pak location D07
53	Parity error page, file 1, pak location D07
54	Parity error page, file 2, pak location D07
55	Parity error page, file 3, pak location D07
56	Parity error page, file 0, pak location D08
57	Parity error page, file 1, pak location D08
58	Parity error page, file 2, pak location D08
59	Parity error page, file 3, pak location D08
60	Parity error page, file 0, pak location D09
61	Parity error page, file 1, pak location D09
62	Parity error page, file 2, pak location D09
63	Parity error page, file 3, pak location D09

PROC-835 PTM REGISTER (A0)



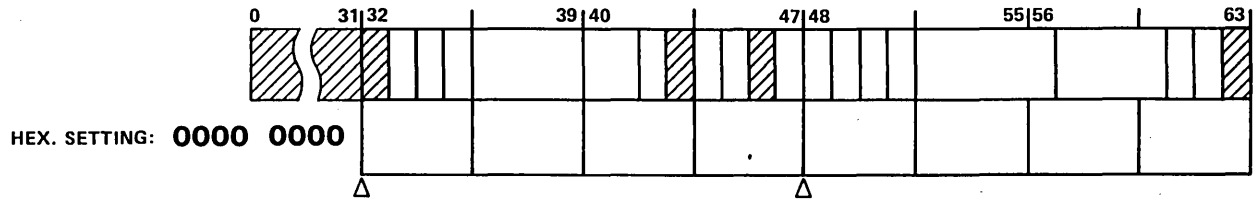
Bit	Description
00	Force bad parity to WAR, byte 0
01	Invert address parity, byte 5
02	Invert address parity, byte 4
03	Invert segment parity
04	Invert segment parity
05	Invert register file parity, byte 7
06	Invert register file parity, byte 6
07	Invert register file parity, byte 5
08	Force bad parity to WAR, byte 1
09	Invert register file parity, byte 4
10	Invert register file parity, byte 3
11	Invert register file parity, byte 2
12	Invert register file parity, byte 1
13	Invert register file parity, byte 0
14	Invert exponent adder ROMs parity
15	Invert floating-point trap ROMs parity
16	Force bad parity to WAR, byte 2
17	Invert segment file parity
18	Invert segment file parity
19	Invert segment file parity
20	Invert address parity, byte 7
21	Invert address parity, byte 6
22	Invert data parity, byte 2
23	Invert data parity, byte 1
24	Force bad parity to WAR byte 3
25	Invert data parity, byte 0
26	Invert generator identifier/LRU counter parity
27	Invert ASID parity, byte 1
28	Invert ASID parity, byte 0
29	Invert page file parity
30	Invert page file parity
31	Invert page file parity

PROC-835 PTM REGISTER (A0)



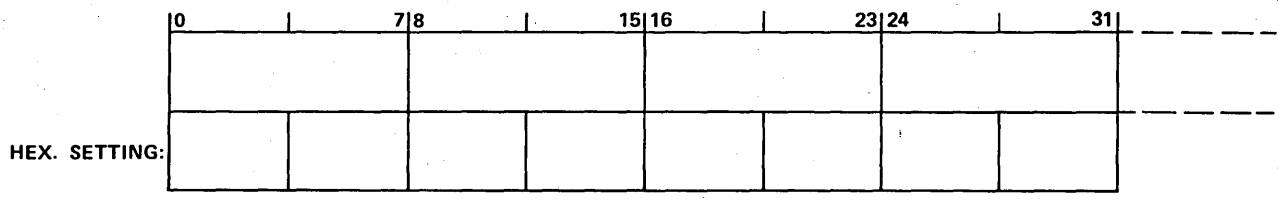
Bit	Description
32	Force bad parity to WAR, byte 4
33	Invert page file parity
34	Invert page file parity
35	Invert page file parity
36	Invert page file parity
37	Invert page file parity
38	Invert segment file parity
39	Invert identifier/AD select ROM parity
40	Force bad parity to WAR, byte 5
41	Invert function code parity
42	Invert mark lines parity
43	Invert tag in parity
44	Invert address parity, byte 3
45	Invert address parity, byte 2
46	Invert address parity, byte 1
47	Invert address parity, byte 0
48	Force bad parity to WAR, byte 6
49	Invert data parity, byte 7
50	Invert data parity, byte 6
51	Invert data parity, byte 5
52	Invert data parity, byte 4
53	Invert data parity, byte 3
54	Invert BDP K stream input parity
55	Invert BDP J stream input parity
56	Force bad parity to WAR, byte 7
57	Invert BDP output ROMs parity
58	Invert BDP control ROMs parity
59	Invert MAC ROMs parity
60	Invert CYBER convert ROMs parity
61	Invert immediate select ROMs parity
62	Invert exchange/invalidate address parity
63	Invert partial-write parity

PROC-845, 850, 855, 860 DEC REGISTER (30)



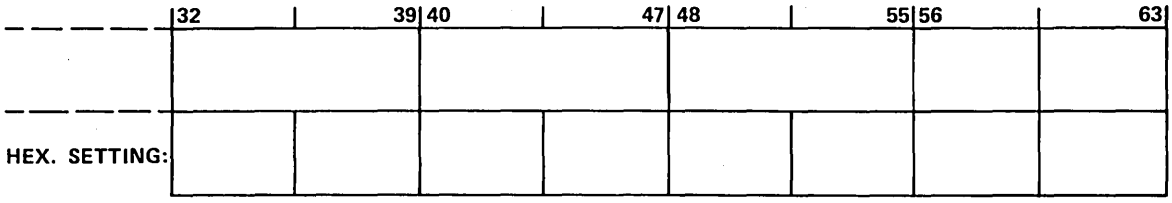
Bit	Description
00 through 31	(Not used)
32	(Not used)
33	Test mode enabled
34	(Not used)
35	Disable corrected error to PROC-845 through 860 status summary register
36	Page map configuration, enable set 0
37	Page map configuration, enable set 1
38	Page map configuration, enable set 2
39	Page map configuration, enable set 3
40	Segment map configuration, enable set 0
41	Segment map configuration, enable set 1
42	Control store sweep
43	(Not used)
44	Control store breakpoint enable
45	Instruction step enable
46	(Not used)
47	Disable detected uncorrectable error
48	Wide clock margins applied (+10 percent)
49	Narrow clock margins applied (-10 percent)
50	Enable cache lookahead
51	Disable unconditional cache lookahead
52	Error retry limit plus parity
53	Error retry limit plus parity
54	Error retry limit plus parity
55	Error retry limit plus parity
56	Error retry limit plus parity
57	Cache configuration, enable set 0
58	Cache configuration, enable set 1
59	Cache configuration, enable set 2
60	Cache configuration, enable set 3
61	Cache fake central memory
62	Force real memory address
63	(Not used)

PROC-990 DEC REGISTER (30)



Bit	Description
00	Disable set 0 of IBS (when set)
01	Disable set 1 of IBS (when set)
02	Disable set 2 of IBS (when set)
03	Disable set 3 of IBS (when set)
04	Bit 0 of 4-bit lookahead count
05	Bit 1 of 4-bit lookahead count
06	Bit 2 of 4-bit lookahead count
07	Bit 3 of 4-bit lookahead count
08	Enable miss on segment map parity error
09	Enable miss on page map parity error
10	Enable segment map set 0
11	Enable segment map set 1
12	Enable page map set 0
13	Enable page map set 1
14	Enable page map set 2
15	Enable page map set 3
16	(Not used)
17	(Not used)
18	(Not used)
19	Divide network bit 1 (result taken from)
20	Divide network bit 2 (result taken from)
21	Divide network upper bit (to compare against)
22	Divide network lower bit (to compare against)
23	Enable DEC register bits 19 through 22
24	Disable stale data
25	(Not used)
26	Disable issue timeout timer (when set)
27	Set issue timer bit 0 to zero
28	Set issue timer bit 1 to zero
29	Set issue timer bit 2 to zero
30	Set issue timer bit 3 to zero
31	Set issue timer bit 4 to zero

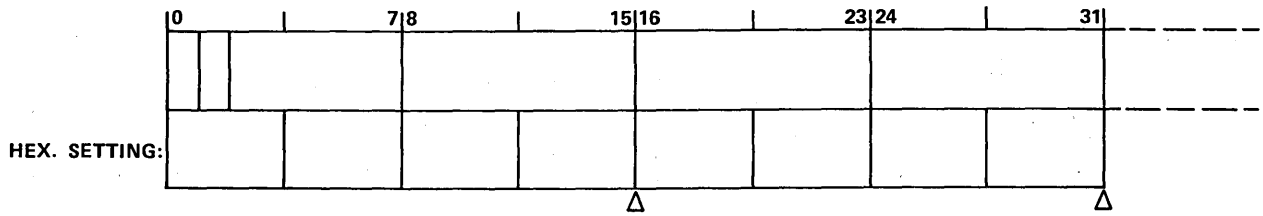
PROC-990 DEC REGISTER (30)



Bit	Description
32	Enable master clear to P-left
33	Enable copy instruction to write PTM
34	Test event/state counters register status summary
35	Disable setting corrected error bit (status summary register)
36	Enable set monitor mode on master clear
37	Enable master clear to segment maps
38	Enable master clear to page maps
39	Enable initialize on MAC access
40	Retry count bit 0
41	Retry count bit 1
42	Retry count bit 2
43	Retry count bit 3
44	Enable control store breakpoint (IDU) Disable control store breakpoint (IN2)
45	Enable control store address compare
46	Set IDU to master-cleared state (IDU) Purge CIR registers (IN2)
47	Disable PDMS (no error interrupts) (EPN) Disable PDMS (no error interrupts) (IDU) False copy of disable PDMS (for EPN) (IN1) False copy of disable PDMS (for EPN) (ACU)
48	Enable prefetch forward
49	Enable prefetch reverse
50	Enable prefetch on a store
51	Prefetch on store to word 0
52	Prefetch on store to word 3
53	Prefetch next block on miss
54	Cache prefetch (4 words ahead)*
55	Cache prefetch (8 words ahead)*
56	Enable cache set 0
57	Enable cache set 1
58	Enable cache set 2
59	Enable cache set 3
60	Force predict-branch-taken (when set)
61	Enable cache step mode
62	Set machine in RMA mode
63	Determine VMID state when PTM (A3) bit 26 is set on master clear

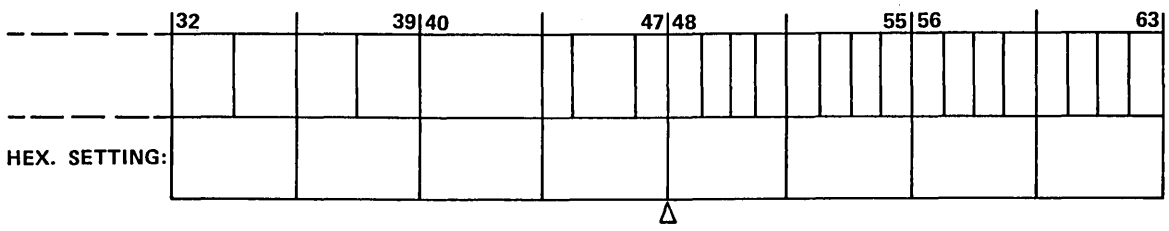
* When set together, DEC bits 54 through 55 provide a cache prefetch of 12 words.

PROC-845, 850, 855, 860 PFS0 REGISTER (80)



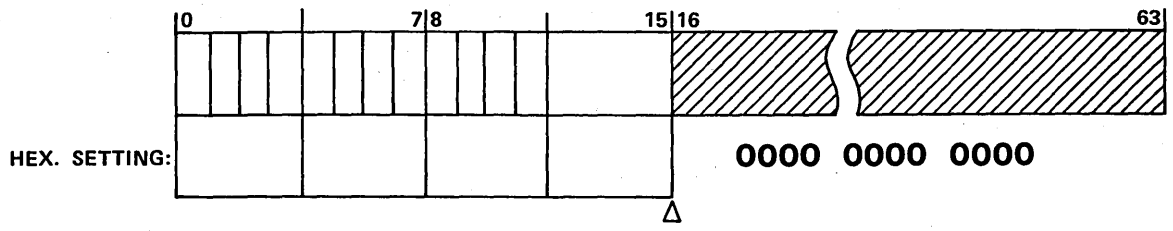
Level 3 Diagram	Bit	Description
ICC 3.1	00	R60 after PONR MCR bit 0: uncorrectable parity error
ICC 3.1	01	Correctable/soft/bypass error, MAC operation PDM
AC 3.15	02	AC address mux to LM parity error, byte 2
AC 3.15	03	AC address mux to LM parity error, byte 3
AC 3.15	04	AC address mux to LM parity error, byte 4
AC 3.15	05	AC address mux to LM parity error, byte 5
AC 3.15	06	AC address mux to LM parity error, byte 6
AC 3.15	07	AC address mux to LM parity error, byte 7
AC 3.8	08	A/C stream data assembly register parity error, byte 0
AC 3.8	09	A/C stream data assembly register parity error, byte 1
AC 3.8	10	A/C stream data assembly register parity error, byte 2
AC 3.8	11	A/C stream data assembly register parity error, byte 3
AC 3.8	12	A/C stream data assembly register parity error, byte 4
AC 3.8	13	A/C stream data assembly register parity error, byte 5
AC 3.8	14	A/C stream data assembly register parity error, byte 6
AC 3.8	15	A/C stream data assembly register parity error, byte 7
AC 3.9	16	A/C stream data buffer register parity error, byte 0
AC 3.9	17	A/C stream data buffer register parity error, byte 1
AC 3.9	18	A/C stream data buffer register parity error, byte 2
AC 3.9	19	A/C stream data buffer register parity error, byte 3
AC 3.9	20	A/C stream data buffer register parity error, byte 4
AC 3.9	21	A/C stream data buffer register parity error, byte 5
AC 3.9	22	A/C stream data buffer register parity error, byte 6
AC 3.9	23	A/C stream data buffer register parity error, byte 7
AC 3.12	24	B stream data buffer register parity error, byte 0
AC 3.12	25	B stream data buffer register parity error, byte 1
AC 3.12	26	B stream data buffer register parity error, byte 2
AC 3.12	27	B stream data buffer register parity error, byte 3
AC 3.12	28	B stream data buffer register parity error, byte 4
AC 3.12	29	B stream data buffer register parity error, byte 5
AC 3.12	30	B stream data buffer register parity error, byte 6
AC 3.12	31	B stream data buffer register parity error, byte 7

PROC-845, 850, 855, 860 PFSO REGISTER (80)



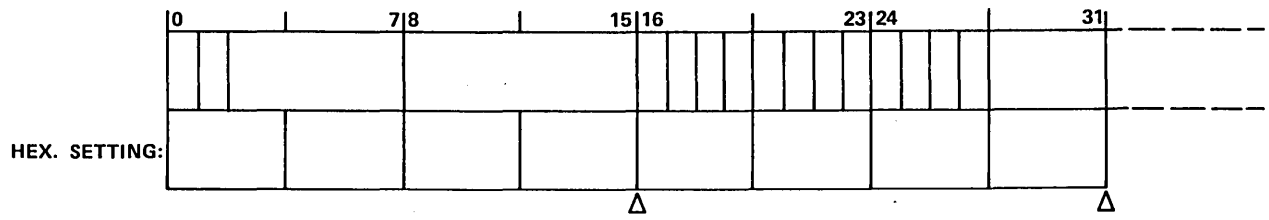
Level 3 Diagram	Bit	Description
AC 3.15	32	A/C stream ASID register parity error, byte 0
AC 3.15	33	A/C stream ASID register parity error, byte 1
AC 3.15	34	B stream ASID register parity error, byte 0
AC 3.15	35	B stream ASID register parity error, byte 1
AC 3.13	36	Address offset select mux parity error, byte 2
AC 3.13	37	Address offset select mux parity error, byte 3
AC 3.0/18	38	AC micrand parity error, byte 0
AC 3.0/18	39	AC micrand parity error, byte 1
AC 3.15	40	Recovery address register parity error, byte 0
AC 3.15	41	Recovery address register parity error, byte 1
AC 3.15	42	Recovery address register parity error, byte 2
AC 3.15	43	Recovery address register parity error, byte 3
ALN 3.1	44	ALN soft control data-out register parity error
AC 3.2	45	AC soft control 2 data-out register parity error
AC 3.1	46	AC soft control 1 data-out register parity error
AC 3.14	47	ALN shift count register parity error
AC 3.13/18	48	A/C stream length counter parity error
AC 3.13/18	49	B stream length counter parity error
AC 3.9	50	A stream data byte to BDP parity error
AC 3.12	51	B stream data byte to BDP parity error
AC 3.8	52	Store bit/all other operation select mux parity error
ALN 3.15/24	53	Convert-to-binary data byte from BDP parity error
BDP 3.8/33	54	B stream stage 1 data register parity error
BDP 3.5/33	55	A stream stage 1 data register parity error
BDP 3.15/33	56	Register file A address counter parity error
BDP 3.15/33	57	Register file B address counter parity error
BDP 3.16/33	58	Register file A data parity error
BDP 3.16/33	59	Register file B data parity error
BDP 3.25/33	60	Decimal adder bits 10 through 17, convert-to-decimal parity error
BDP 3.15/33	61	Table load limit register stage 3 parity error
BDP 3.13/33	62	Common stage 7 register parity error
MAC 3.11/9	63	PFS board 0 internal parity error

PROC-845, 850, 855, 860 PFS1 REGISTER (81)



Level 3 Diagram	Bit	Description
BDP 3.14/33	00	Buffer RAM address counter parity error
BDP 3.20/33	01	C stream stage 2 data register parity error
BDP 3.3/33	02	Specification error RAM, x256 RAM address parity error
BDP 3.3/33	03	Specification error RAM, x256 RAM out data parity error
BDP 3.5/33	04	A stream stage 2 data register parity error
BDP 3.8/33	05	B stream stage 2 data register parity error
BDP 3.2/33	06	Aj descriptor parity error
BDP 3.2/33	07	Ak descriptor parity error
BDP 3.22/33	08	Translate RAM address parity error
BDP 3.22/33	09	Translate RAM output data parity error
BDP 3.23/33	10	Convert-to-binary/decimal RAM address parity error
BDP 3.23/33	11	Convert-to-binary/decimal RAM output data parity error
BDP 3.1/33	12	BDP micrand byte 0 or 1 parity error
BDP 3.1/33	13	BDP micrand byte 2 or 3 parity error
BDP 3.1/33	14	BDP micrand byte 4 or 5 parity error
BDP 3.1/33	15	BDP micrand byte 6 or 7 parity error
	16 through 63	(Not used)

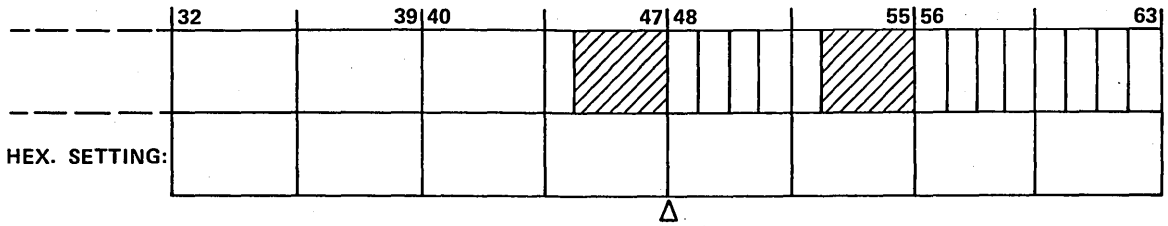
PROC-845, 850, 855, 860 PFS2 REGISTER (82)



Level 3

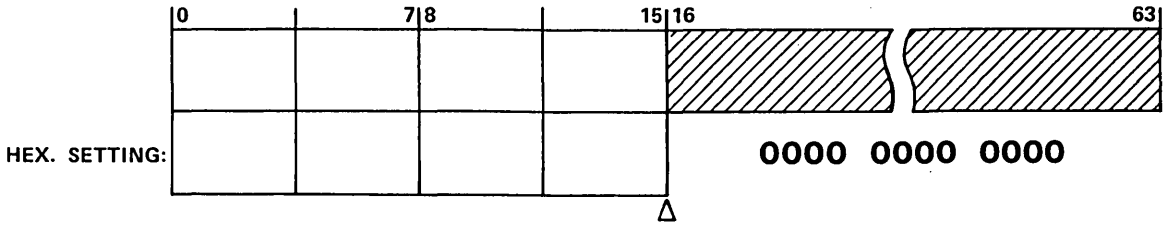
Diagram	Bit	Description
BDP 3.11/33	00	Immediate data byte in scale counter parity error
BDP 3.29/33	01	Edit mask byte register parity error
LM 3.21	02	Cache address register parity error, byte 0
LM 3.21	03	Cache address register parity error, byte 1
LM 3.21	04	Cache address register parity error, byte 2
LM 3.21	05	Cache address register parity error, byte 3
LM 3.21	06	Cache address register parity error, byte 4
LM 3.21	07	Cache address register parity error, byte 5
LM 3.21	08	Cache write-data parity error, byte 0
LM 3.21	09	Cache write-data parity error, byte 1
LM 3.21	10	Cache write-data parity error, byte 2
LM 3.21	11	Cache write-data parity error, byte 3
LM 3.21	12	Cache write-data parity error, byte 4
LM 3.21	13	Cache write-data parity error, byte 5
LM 3.21	14	Cache write-data parity error, byte 6
LM 3.21	15	Cache write-data parity error, byte 7
LM 3.20	16	Multiple cache hit
LM 3.20	17	Multiple cache allocate error
LM 3.14	18	Cache tag file parity error
LM 3.14	19	Cache tag file address parity error
OPI 3.19	20	DAI parity error: LM read data mux, direct CMC data 3
OPI 3.19	21	DAI parity error: LM read data mux, cache read data 2
OPI 3.19	22	DAI parity error: LM read data mux, real memory address 1
OPI 3.19	23	DAI parity error: LM read data mux, buffer CMC data 0
LM 3.21	24	Cache write data from CPU parity error
LM 3.21	25	Cache block fill data from CM port parity error
LM 3.5/21	26	Cache address register parity error 4: cache associative tag
LM 3.21	27	Cache mark data parity error
LM 3.21	28	Cache address register parity error: address mux 0: invalidate
LM 3.21	29	Cache address register parity error: address mux 1: AC address
LM 3.21	30	Cache address register parity error: address mux 2: IF address
LM 3.21	31	Cache address register parity error: address mux 3: interrupt

PROC-845, 850, 855, 860 PFS2 REGISTER (82)



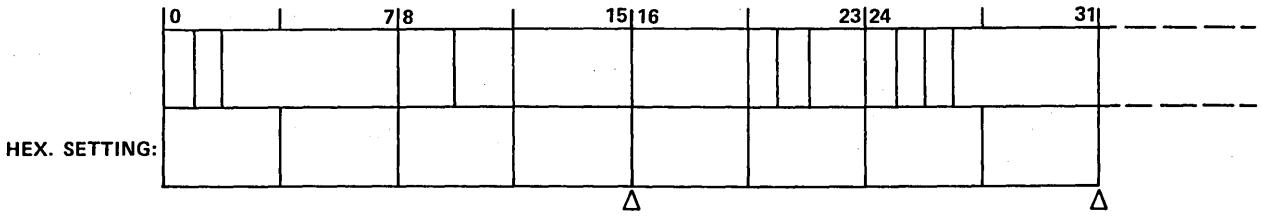
Level 3 Diagram	Bit	Description
LM 3.3/21	32	Modified purge code (from SM) parity error
LM 3.3/21	33	LM micrand parity error, byte 0
LM 3.3/21	34	LM micrand parity error, byte 1
	35	(Not used)
LM 3.12	36	Page map status parity error, set 0
LM 3.12	37	Page map status parity error, set 1
LM 3.12	38	Page map status parity error, set 2
LM 3.12	39	Page map status parity error, set 3
LM 3.12	40	Page map parity error, set 0
LM 3.12	41	Page map parity error, set 1
LM 3.12	42	Page map parity error, set 2
LM 3.12	43	Page map parity error, set 3
LM 3.12	44	Page frame address parity error
	45	(Not used)
	46	(Not used)
	47	(Not used)
LM 3.10	48	Page table length register parity error
LM 3.10	49	Page table address register parity error
LM 3.10	50	Page offset register parity error
LM 3.6	51	Page size mask parity error
LM 3.7	52	Stream mode exchange word tag parity error
	53	(Not used)
	54	(Not used)
	55	(Not used)
LM 3.8	56	CMC response 2: corrected error write
LM 3.8	57	CMC response 6: corrected error read
LM 3.8	58	CMC response 1: uncorrectable error write
LM 3.8	59	CMC response 5: uncorrectable error read
LM 3.8	60	CMC response 7: reject
LM 3.8	61	CMC response 7: parity error
LM 3.8	62	CMC tag register parity error
MAC 3.11/9	63	PFS board 1 internal parity error

PROC-845, 850, 855, 860 PFS3 REGISTER (83)



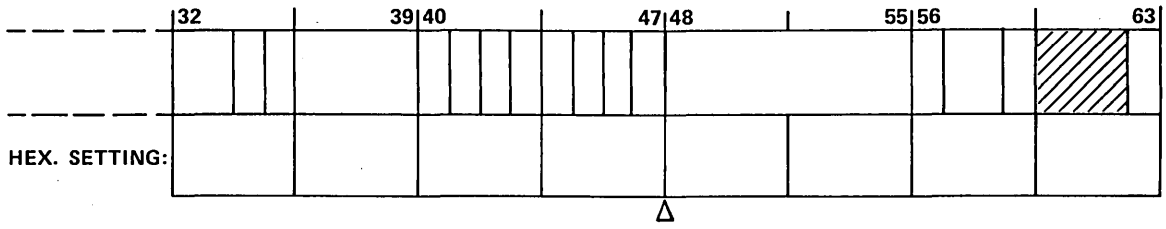
Level 3 Diagram	Bit	Description
LM 3.21	00	Cache address parity error, set 0
LM 3.21	01	Cache address parity error, set 1
LM 3.21	02	Cache address parity error, set 2
LM 3.21	03	Cache address parity error, set 3
LM 3.21	04	Cache tag RAM parity error, set 0
LM 3.21	05	Cache tag RAM parity error, set 1
LM 3.21	06	Cache tag RAM parity error, set 2
LM 3.21	07	Cache tag RAM parity error, set 3
OPI 3.19	08	DAI parity error, cache data, set 0
OPI 3.19	09	DAI parity error, cache data, set 1
OPI 3.19	10	DAI parity error, cache data, set 2
OPI 3.19	11	DAI parity error, cache data, set 3
OPI 3.19	12	DAI parity error: DAI mux, local memory read data 3
OPI 3.19	13	DAI parity error: DAI mux, byte load data 2
OPI 3.19	14	DAI parity error: DAI mux, ALN result data 1
OPI 3.19	15	DAI parity error: DAI mux, functional unit micrand 0
	16 through 63	(Not used)

PROC-845, 850, 855, 860 PFS4 REGISTER (84)



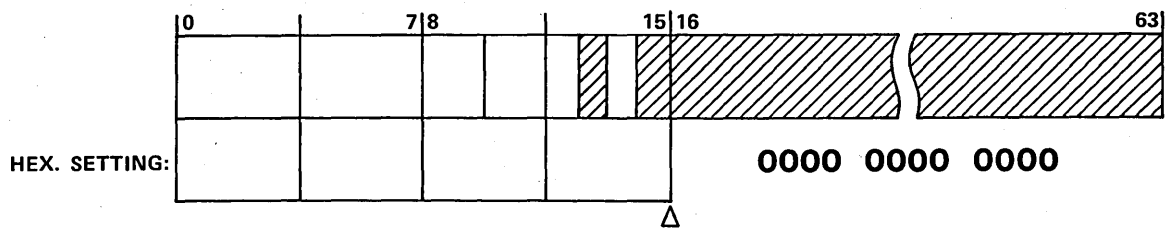
Level 3 Diagram	Bit	Description
SM 3.3/5	00	Segment descriptor mux-out parity error, set 0
SM 3.3/5	01	Segment descriptor mux-out parity error, set 1
SM 3.1/5	02	Segment descriptor mux parity error, byte 0
SM 3.1/5	03	Segment descriptor mux parity error, byte 1
SM 3.1/5	04	Segment descriptor mux parity error, byte 2
SM 3.1/5	05	Segment descriptor mux parity error, byte 3
SM 3.1/5	06	Segment descriptor mux parity error, byte 4
SM 3.1/5	07	Segment descriptor mux parity error, byte 5
SM 3.0/5	08	Segment table length parity error, byte 0
SM 3.0/5	09	Segment table length parity error, byte 1
SM 3.0/5	10	Segment table address register parity error, bytes 0 and 3
SM 3.0/5	11	Segment table address register parity error, bytes 1 and 2
SM 3.1/5	12	New P register parity error, byte 0
SM 3.1/5	13	New P register parity error, byte 1
SM 3.1/5	14	New P register parity error, byte 2
SM 3.1/5	15	New P register parity error, byte 3
SM 3.0/5	16	PVA register bits 4 through 7 (CBP VMID) parity error
SM 3.0/5	17	PVA register bits 12 through 15 (CBP R3) parity error
SM 3.0/5	18	PVA register parity error, byte 2
SM 3.0/5	19	PVA register parity error, byte 3
SM 3.3/5	20	Segment descriptor mux-out parity error: neither set select
SM 3.3/5	21	Valid status RAM error: parity error or double hit
SM 3.4/5	22	SM micrand parity error, byte 0
SM 3.4/5	23	SM micrand parity error, byte 1
SM 3.4/5	24	Purge code parity error
ICP 3.1	25	Rank 32 BDP descriptor data type register parity error
ICP 3.1	26	Rank 32 j,k register parity error
ICP 3.0	27	Rank 50 UTP register parity error, byte 2
ICP 3.0	28	Rank 50 UTP register parity error, byte 4
ICP 3.0	29	Rank 50 UTP register parity error, byte 5
ICP 3.0	30	Rank 50 UTP register parity error, byte 6
ICP 3.0	31	Rank 50 UTP register parity error, byte 7

PROC-845, 850, 855, 860 PFS4 REGISTER (84)



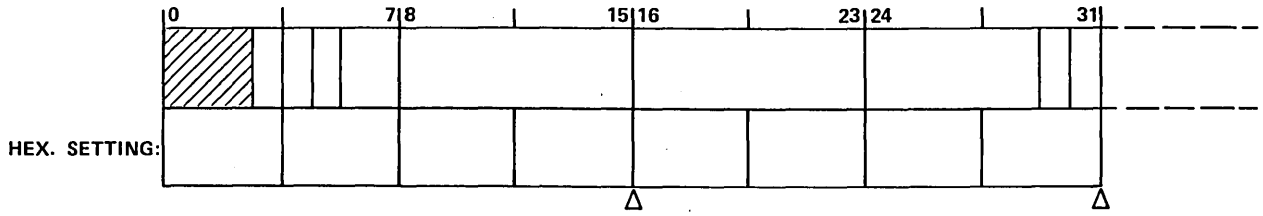
Level 3 Diagram	Bit	Description
ICC 3.3	32	Live register write-data parity error, byte 0
ICC 3.3	33	Live register write-data parity error, byte 1
ICC 3.3	34	Rank 41 general micrand parity error 2, byte 3
ICC 3.3	35	Rank 41 general micrand parity error 1, byte 2
ICP 3.0	36	Rank 50 P register parity error, byte 4
ICC 3.0	37	Rank 50 P register parity error, byte 5
ICC 3.0	38	Rank 50 P register parity error, byte 6
ICC 3.0	39	Rank 50 P register parity error, byte 7
ICP 3.3	40	Rank 41 general micrand parity error 3 (byte 4)
ICP 3.3	41	Successful retry
ICP 3.6	42	Deadman time-out
ICP 3.7	43	Debug mask parity error
ICC 3.0	44	MAC operation PDM
ICC 3.9	45	Retry counter register parity error
ICC 3.6	46	PDM during exchange (exchange mode set)
ICC 3.7	47	Rank 50 before PONR PDM
OPI 3.12	48	DAI parity error 1: register file write data parity error, byte 0
OPI 3.12	49	DAI parity error 2: register file write data parity error, byte 1
OPI 3.12	50	DAI parity error 3: register file write data parity error, byte 2
OPI 3.12	51	DAI parity error 4: register file write data parity error, byte 3
OPI 3.12	52	DAI parity error 5: register file write data parity error, byte 4
OPI 3.12	53	DAI parity error 6: register file write data parity error, byte 5
OPI 3.12	54	DAI parity error 7: register file write data parity error, byte 6
OPI 3.12	55	DAI parity error 8: register file write data parity error, byte 7
OPI 3.1	56	Minipipe rank 50 register file write address parity error
OPI 3.5	57	Register file read data register parity error, bytes 0 through 3
OPI 3.5	58	Register file read data register parity error, bytes 4 through 7
OPI 3.16/19	59	CMC tag (from LM) parity error
	60	(Not used)
	61	(Not used)
	62	(Not used)
MAC 3.11/9	63	PFS board 2 internal parity error

PROC-845, 850, 855, 860 PFS5 REGISTER (85)



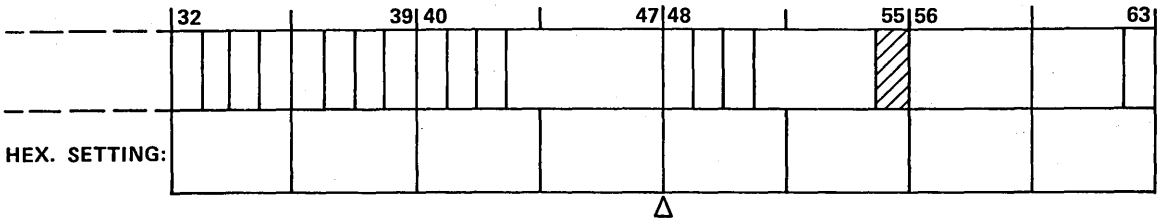
Level 3 Diagram	Bit	Description
OPI 3.6	00	Rank 22 P register parity error, byte 4
OPI 3.6	01	Rank 22 P register parity error, byte 5
OPI 3.6	02	Rank 22 P register parity error, byte 6
OPI 3.6	03	Rank 22 P register parity error, byte 7
OPI 3.6	04	R22 BDP descriptor data type field parity error
OPI 3.6	05	Rank 22 j,k field parity error
OPI 3.6	06	Rank 22 immediate operand parity error, byte 0
OPI 3.6	07	Rank 22 immediate operand parity error, byte 1
OPI 3.0	08	Functional unit microrand parity error, byte 6
OPI 3.0	09	Functional unit microrand parity error, byte 7
OPI 3.16/19	10	Register data select write field parity error, byte 0
OPI 3.16/19	11	Register data select write field parity error, byte 1
OPI 3.16/19	12	Increment j,k field parity error
	13	(Not used)
OPI 3.17	14	Microsecond counter parity error
	15	(Not used)
	16 through 63	(Not used)

PROC-845, 850, 855, 860 PFS6 REGISTER (86)



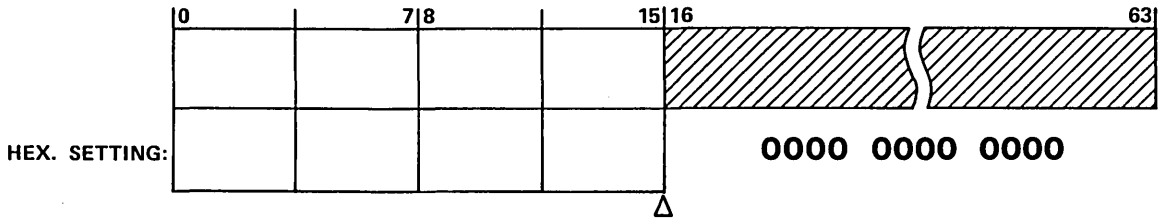
Level 3 Diagram	Bit	Description
	00	(Not used)
	01	(Not used)
	02	(Not used)
CST 3.4	03	Micrand address register parity error
CST 3.5	04	CST write data (from MAC) parity error, byte 0
CST 3.5	05	CST write data (from MAC) parity error, byte 1
CST 3.1/0	06	MSC field register parity error, byte 0
CST 3.1/0	07	MSC field register parity error, byte 1
CST 3.5	08	FU micrand buffer register (t23) parity error, byte 0
CST 3.5	09	FU micrand buffer register (t23) parity error, byte 1
CST 3.5	10	FU micrand buffer register (t23) parity error, byte 2
CST 3.5	11	FU micrand buffer register (t23) parity error, byte 3
CST 3.5	12	FU micrand buffer register (t23) parity error, byte 4
CST 3.5	13	FU micrand buffer register (t23) parity error, byte 5
CST 3.5	14	FU micrand buffer register (t23) parity error, byte 6
CST 3.5	15	FU micrand buffer register (t23) parity error, byte 7
CST 3.5	16	FU micrand register (t31) parity error, byte 0
CST 3.5	17	FU micrand register (t31) parity error, byte 1
CST 3.5	18	FU micrand register (t31) parity error, byte 2
CST 3.5	19	FU micrand register (t31) parity error, byte 3
CST 3.5	20	FU micrand register (t31) parity error, byte 4
CST 3.5	21	FU micrand register (t31) parity error, byte 5
CST 3.5	22	FU micrand register (t31) parity error, byte 6
CST 3.5	23	FU micrand register (t31) parity error, byte 7
CST 3.5	24	General micrand register (t22) parity error, byte 2
CST 3.5	25	General micrand register (t22) parity error, byte 3
CST 3.5	26	General micrand register (t22) parity error, byte 4
CST 3.5	27	General micrand register (t22) parity error, byte 5
CST 3.5	28	General micrand register (t22) parity error, byte 6
CST 3.5	29	General micrand register (t22) parity error, byte 7
OPI 3.14	30	A-start, X-start counter register parity error
OPI 3.14	31	A-terminate, X-terminate counter register parity error

PROC-845, 850, 855, 860 PFS6 REGISTER (86)



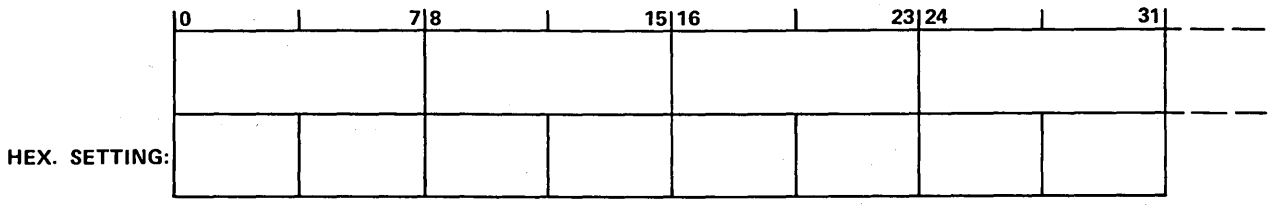
Level 3 Diagram	Bit	Description
MAC 3.1/8	32	Maintenance channel out register (to IOU) parity error
MAC 3.8	33	Maintenance channel input: write data or function word parity error
MAC 3.0/8	34	Maintenance channel input data fanout parity error
MAC 3.0/8	35	Read data (to maintenance channel out register) mux parity error
MAC 3.6/8	36	Reference ROM address parity error
MAC 3.5/8	37	Address translation mux parity error
MAC 3.6/8	38	Reference ROM data parity error
OPI 3.14	39	N counter register parity error
IF 3.1/4	40	First level instruction C170 odd RAM A parity error
IF 3.1/4	41	First level instruction C170 even RAM A parity error
IF 3.1/4	42	First level instruction C180 RAM A parity error
IF 3.3/4	43	IB12 P register, byte 4
IF 3.3/4	44	IB12 P register, byte 5
IF 3.3/4	45	Rank 12 instruction buffer opcode
IF 3.3/4	46	IB12 instruction mux bits 3, 12 through 15, 24
IF 3.3/4	47	IB12 instruction mux bits 16 through 23
IF 3.1/4	48	First level instruction C170 odd RAM B parity error
IF 3.1/4	49	First level instruction C170 even RAM B parity error
IF 3.1/4	50	First level instruction C180 RAM B parity error
IF 3.3/4	51	IB12 P register, byte 6
IF 3.3/4	52	IB12 P register, byte 7
IF 3.3/4	53	IB12 P instruction mux bits 33 through 40
IF 3.3/4	54	IB12 P instruction mux bits 25 through 32
	55	(Not used)
IF 3.5	56	Branch address A register parity error, byte 0
IF 3.5	57	Branch address A register parity error, byte 1
IF 3.5	58	Branch address A register parity error, byte 2
IF 3.5	59	Branch address A register parity error, byte 3
IF 3.5	60	Branch address B register parity error, byte 1
IF 3.5	61	Branch address B register parity error, byte 2
IF 3.5	62	Branch address B register parity error, byte 3
MAC 3.11/9	63	PFS board 3 internal parity error

PROC-845, 850, 855, 860 PFS7 REGISTER (87)



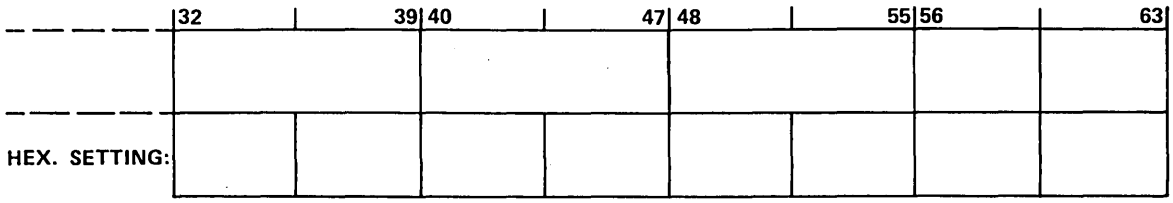
Level 3 Diagram	Bit	Description
IF 3.5/4	00	Branch address adder input parity error, byte 0
IF 3.5/4	01	Branch address adder input parity error, byte 1
IF 3.5/4	02	Branch address adder input parity error, byte 2
IF 3.5/4	03	Branch address adder input parity error, byte 3
IF 3.5	04	Branch address register parity error, byte 4
IF 3.5	05	Branch address register parity error, byte 5
IF 3.5	06	Branch address register parity error, byte 6
IF 3.5	07	Branch address register parity error, byte 7
IF 3.2	08	IBO2 parity error, byte 0; Instruction mux bits 3, 12 through 15, 24
IF 3.2	09	IBO2 parity error, byte 1; Instruction mux bits 16 through 23
IF 3.2	10	IBO2 parity error, byte 2; Instruction mux bits 25 through 32
IF 3.2	11	IBO2 parity error, byte 3; Instruction mux bits 33 through 40
IF 3.3	12	IB11 parity error, byte 0; Instruction mux bits 3, 12 through 15, 24
IF 3.3	13	IB11 parity error, byte 1; Instruction mux bits 16 through 23
IF 3.3	14	IB11 parity error, byte 2; Instruction mux bits 25 through 32
IF 3.3	15	IB11 parity error, byte 3; Instruction mux bits 33 through 40
	16 through 63	(Not used)

PROC-845, 850, 855, 860 PFS8 REGISTER (88)



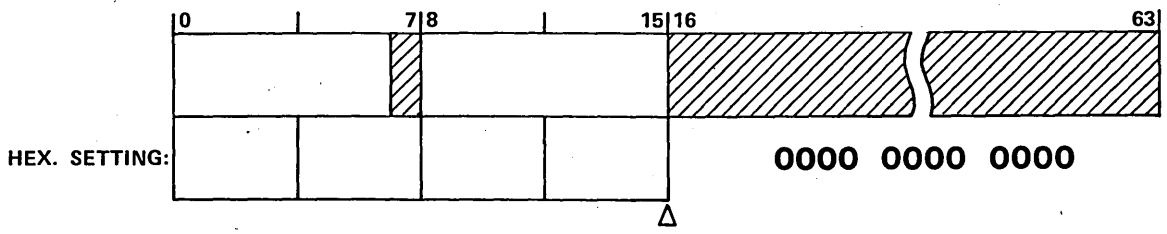
Level 3 Diagram	Bit	Description
IF 3.0/4	00	Instruction assembly register parity error, byte 0
IF 3.0/4	01	Instruction assembly register parity error, byte 1
IF 3.0/4	02	Instruction assembly register parity error, byte 2
IF 3.0/4	03	Instruction assembly register parity error, byte 3
IF 3.0/4	04	Instruction assembly register parity error, byte 4
IF 3.0/4	05	Instruction assembly register parity error, byte 5
IF 3.0/4	06	Instruction assembly register parity error, byte 6
IF 3.0/4	07	Instruction assembly register parity error, byte 7
IF 3.0/4	08	Parcel 3 save register parity error, byte 0
IF 3.0/4	09	Parcel 3 save register parity error, byte 1
IF 3.4	10	Parity error mux parity error, byte 0
IF 3.4	11	Parity error mux parity error, byte 1
IF 3.4	12	Parity error mux parity error, byte 2
IF 3.4	13	Parity error mux parity error, byte 3
ALN 3.2/24	14	Multiply/divide minor cycle control register parity error, byte 0
ALN 3.2/24	15	Multiply/divide minor cycle control register parity error, byte 1
ALN 3.13/24	16	C register data parity error, byte 0
ALN 3.13/24	17	C register data parity error, byte 1
ALN 3.13/24	18	C register data parity error, byte 2
ALN 3.13/24	19	C register data parity error, byte 3
ALN 3.13/24	20	C register data parity error, byte 4
ALN 3.13/24	21	C register data parity error, byte 5
ALN 3.13/24	22	C register data parity error, byte 6
ALN 3.13/24	23	C register data parity error, byte 7
ALN 3.14/24	24	B register data parity error, byte 0
ALN 3.14/24	25	B register data parity error, byte 1
ALN 3.14/24	26	B register data parity error, byte 2
ALN 3.14/24	27	B register data parity error, byte 3
ALN 3.14/24	28	B register data parity error, byte 4
ALN 3.14/24	29	B register data parity error, byte 5
ALN 3.14/24	30	B register data parity error, byte 6
ALN 3.14/24	31	B register data parity error, byte 7

PROC-845, 850, 855, 860 PFS8 REGISTER (88)



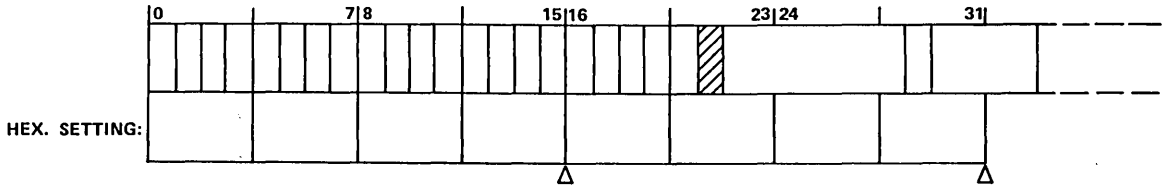
Level 3 Diagram	Bit	Description
ALN 3.10	32	Large adder input parity error, byte 0
ALN 3.10	33	Large adder input parity error, byte 1
ALN 3.10	34	Large adder input parity error, byte 2
ALN 3.10	35	Large adder input parity error, byte 3
ALN 3.10	36	Large adder input parity error, byte 4
ALN 3.10	37	Large adder input parity error, byte 5
ALN 3.10	38	Large adder input parity error, byte 6
ALN 3.10	39	Large adder input parity error, byte 7
ALN 3.10	40	Large adder input parity error, byte 8
ALN 3.10	41	Large adder input parity error, byte 9
ALN 3.10	42	Large adder input parity error, byte 10
ALN 3.10	43	Large adder input parity error, byte 11
ALN 3.10	44	Large adder group 0 carry error
ALN 3.10	45	Large adder group 1 carry error
ALN 3.10	46	Large adder group 2 carry error
ALN 3.10	47	Large adder group 3 carry error
ALN 3.10	48	Large adder group 4 carry error
ALN 3.10	49	Large adder group 5 carry error
ALN 3.10	50	Large adder group 6 carry error
ALN 3.10	51	Large adder group 7 carry error
ALN 3.10	52	Large adder group 8 carry error
ALN 3.10	53	Large adder group 9 carry error
ALN 3.10	54	Large adder group 10 carry error
ALN 3.10	55	Large adder group 11 carry error
	56	(Not used)
	57	(Not used)
ALN 3.4/24	58	Shift count (from AC) parity error, byte 0
ALN 3.4/24	59	Shift count (from AC) parity error, byte 1
ALN 3.16/24	60	Multiply final adder carry error, group 0
ALN 3.16/24	61	Multiply final adder carry error, group 1
	62	(Not used)
MAC 3.11/9	63	PFS board 4 internal parity error

PROC-845, 850, 855, 860 PFS9 REGISTER (89)



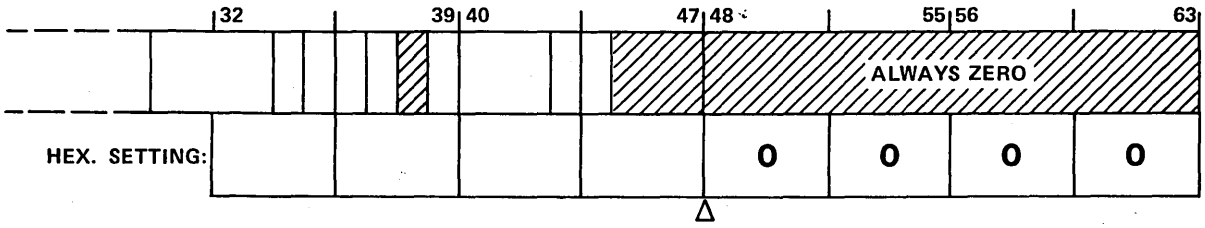
Level 3 Diagram	Bit	Description
ALN 3.16/24	00	Multiply final adder carry error, group 2
ALN 3.16/24	01	Multiply final adder carry error, group 3
ALN 3.16/24	02	Multiply final adder carry error, group 4
ALN 3.16/24	03	Multiply final adder carry error, group 5
ALN 3.16/24	04	Multiply final adder carry error, group 6
ALN 3.16/24	05	Multiply final adder carry error, group 7
ALN 3.16/24	06	Multiply final adder carry error, group 8
ALN 3.16/24	07	(Not used)
ALN 3.0/24	08	ALN micrand parity error, byte 0
ALN 3.0/24	09	ALN micrand parity error, byte 1
ALN 3.0/24	10	ALN micrand parity error, byte 2
ALN 3.0/24	11	ALN micrand parity error, byte 3
ALN 3.0/24	12	ALN micrand parity error, byte 4
ALN 3.0/24	13	ALN micrand parity error, byte 5
ALN 3.0/24	14	ALN micrand parity error, byte 6
ALN 3.3/24	15	ALN micrand parity error, byte 7
	16 through 63	(Not used)

PROC-845, 850, 855, 860 PTM REGISTER (A0)



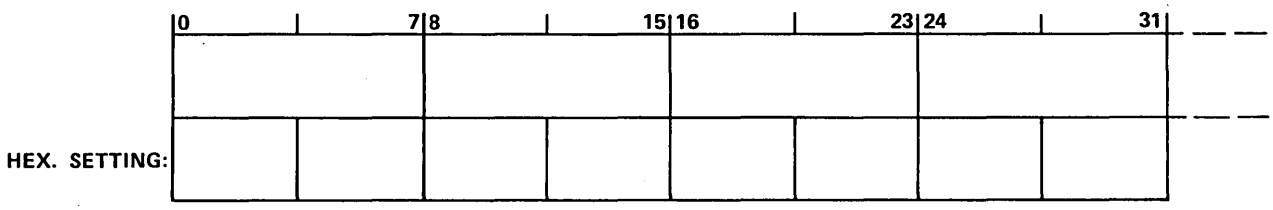
Bit	Description
00	Address control, data to length counter
01	Address control, 8-bit adder
02	Address control, ALN shift count
03	BDP, AJ port formatting
04	BDP, AK port formatting
05	BDP, scan register file address
06	BDP, specification error ROM address
07	BDP, encode
08	IC, Test retry hardware
09	Address control, mark lines
10	Local memory, page offset
11	Local memory, segment/page identifier
12	Operand issue, write address pipeline input
13	Operand issue, data subfunction select
14	Operand issue, literal data
15	Instruction fetch, instruction decode muxes
16	ALN, force C register parity error
17	ALN, force shift fault
18	MAC, MAC data output
19	CMC partial parity disable
20	CSU partial parity disable
21	(Not used)
22	Purge address counter parity invert
23	Page map status parity invert, set 0
24	Page map status parity invert, set 1
25	Page map status parity invert, set 2
26	Page map status parity invert, set 3
27	Tag file parity invert
28	Local memory tag to CMC parity invert
29	CMC response code parity invert
30	Local memory, RMA
31	Local memory, RMA

PROC-845, 850, 855, 860 PTM REGISTER (A0)



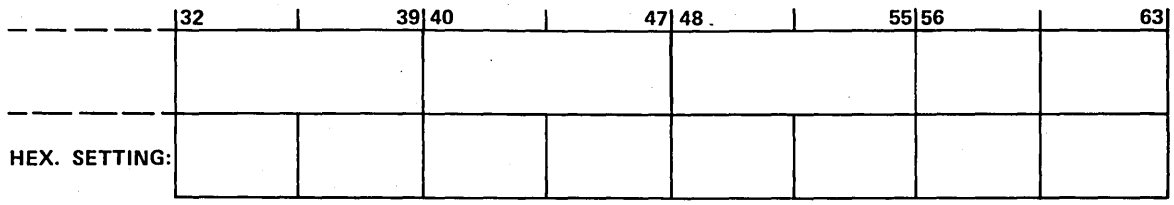
Bit	Description
32	Local memory, RMA
33	Local memory, RMA
34	Local memory, function code
35	Operand issue, (companion with bit 13)
36	Operand issue, force parity error on RDSW to instruction counter
37	Operand issue, force parity error on microsecond counter
38	(Not used)
39	Force cache set 1 allocate
40	Force tag file 0 valid
41	Force tag file 1 valid
42	Force tag file 2 valid
43	Force LM tag parity error
44	Force minipipe parity error
45	(Not used)
46	(Not used)
47	(Not used)
48	(Always zero)
49	(Always zero)
50	(Always zero)
51	(Always zero)
52	(Always zero)
53	(Always zero)
54	(Always zero)
55	(Always zero)
56	(Always zero)
57	(Always zero)
58	(Always zero)
59	(Always zero)
60	(Always zero)
61	(Always zero)
62	(Always zero)
63	(Always zero)

PROC-990 PFS0 REGISTER (80)



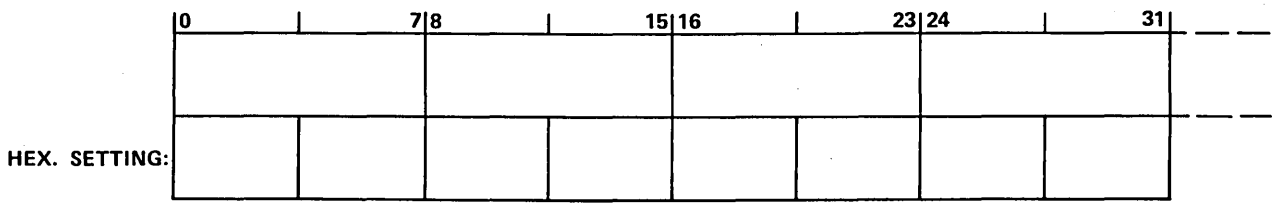
Bit	Description
00	Detected uncorrected error (DUE)
01	Corrected error
02	IOU data parity error
03	Functional unit read data parity error
04	Register 31 parity error, byte 6
05	Register 31 parity error, byte 7
06	Register 32 parity error, byte 6
07	Register 32 parity error, byte 7
08	Copy out data parity error, byte 0
09	Copy out data parity error, byte 1
10	Copy out data parity error, byte 2
11	Copy out data parity error, byte 3
12	Copy out data parity error, byte 4
13	Copy out data parity error, byte 5
14	Copy out data parity error, byte 6
15	Copy out data parity error, byte 7
16	Parity error on out-register to IOU, byte 0
17	Parity error on out-register to IOU, byte 1
18	Parity error on out-register to IOU, byte 2
19	Parity error on out-register to IOU, byte 3
20	Parity error on out-register to IOU, byte 4
21	Parity error on out-register to IOU, byte 5
22	Parity error on out-register to IOU, byte 6
23	Parity error on out-register to IOU, byte 7
24	Copy data-in register parity error, byte 0
25	Copy data-in register parity error, byte 1
26	Copy data-in register parity error, byte 2
27	Copy data-in register parity error, byte 3
28	Copy data-in register parity error, byte 4
29	Copy data-in register parity error, byte 5
30	Copy data-in register parity error, byte 6
31	Copy data-in register parity error, byte 7

PROC-990 PFS0 REGISTER (80)



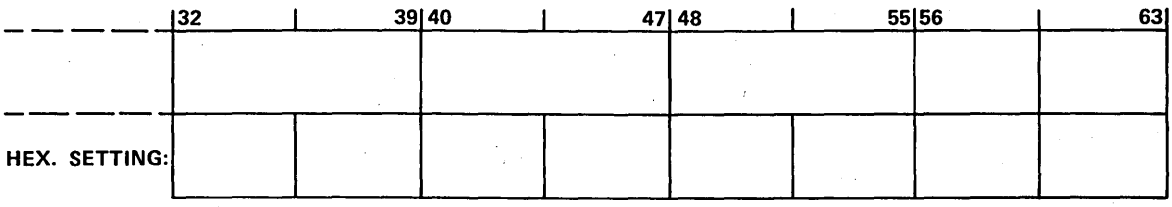
Bit	Description
32	Assembly register parity error, byte 0
33	Assembly register parity error, byte 1
34	Assembly register parity error, byte 2
35	Assembly register parity error, byte 3
36	Assembly register parity error, byte 4
37	Assembly register parity error, byte 5
38	Assembly register parity error, byte 6
39	Assembly register parity error, byte 7
40	History file (X data) parity error, byte 0
41	History file (X data) parity error, byte 1
42	History file (X data) parity error, byte 2
43	History file (X data) parity error, byte 3
44	History file (X data) parity error, byte 4
45	History file (X data) parity error, byte 5
46	History file (X data) parity error, byte 6
47	History file (X data) parity error, byte 7
48	History file (A data) parity error, byte 8
49	History file (A data) parity error, byte 9
50	History file (A data) parity error, byte 10
51	History file (A data) parity error, byte 11
52	History file (A data) parity error, byte 12
53	History file (A data) parity error, byte 13
54	History file (P-right) parity error, byte 14
55	History file (P-right) parity error, byte 15
56	History file (P-right) parity error, byte 16
57	History file (P-right) parity error, byte 17
58	IN2 error tag parity error
59	PSR error tag parity error
60	ACU error tag parity error
61	Soft control memory parity error, byte 0
62	Soft control memory parity error, byte 1
63	Soft control memory parity error, byte 2

PROC-990 PFS1 REGISTER (81)



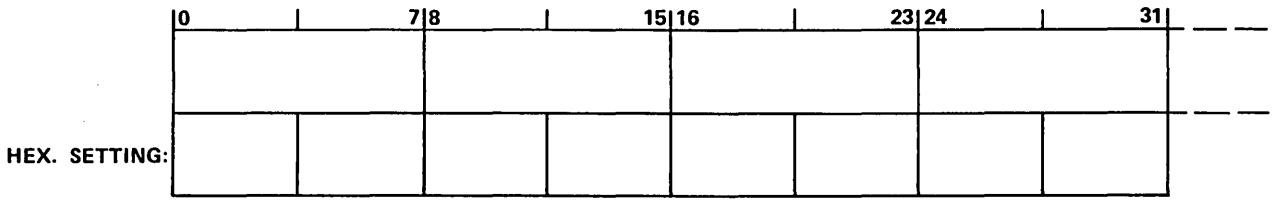
Bit	Description
00 through 15	MAC write assembly register parity error, bytes 0 through 15
16	CS data parity error, byte 8 or SM chip auxiliary board H
23	CS data parity error, byte 15 or SM auxiliary board A
24	CS data parity error, byte 0 or 16, auxiliary board H
25	CS data parity error, byte 1 or 17, auxiliary board G
26	CS data parity error, byte 2 or 18, auxiliary board F
27	CS data parity error, byte 3 or 19, auxiliary board E
28	CS data parity error, byte 4 or 20, auxiliary board D
29	CS data parity error, byte 5 or 21, auxiliary board C
30	CS data parity error, byte 6 or 22, auxiliary board B
31	CS data parity error, byte 7 or 23, auxiliary board A

PROC-990 PFS1 REGISTER (81)



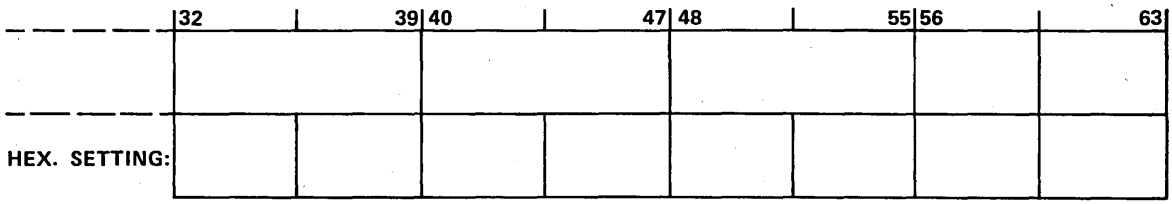
Bit	Description
32	Control word parity error, byte 0
33	Control word parity error, byte 3
34	Control word parity error, byte 6
35	Control word parity error, byte 9
36	Control word parity error, byte 12
37	Control word parity error, byte 15
38	Control word parity error, byte 18
39	Control word parity error, byte 21
40	Control word parity error, byte 1
41	Control word parity error, byte 4
42	Control word parity error, byte 7
43	Control word parity error, byte 10
44	Control word parity error, byte 13
45	Control word parity error, byte 16
46	Control word parity error, byte 19
47	Control word parity error, byte 22
48	Control word parity error, byte 2
49	Control word parity error, byte 5
50	Control word parity error, byte 8
51	Control word parity error, byte 11
52	Control word parity error, byte 14
53	Control word parity error, byte 17
54	Control word parity error, byte 20
55	Control word parity error, byte 23
56	CWD rank BDP descriptor parity error, byte 0
57	CWD rank BDP descriptor parity error, byte 1
58	CWD rank BDP descriptor parity error, byte 2
59	CWD rank BDP descriptor parity error, byte 3
60	CIR rank BDP descriptor parity error, byte 0
61	CIR rank BDP descriptor parity error, byte 1
62	CIR rank BDP descriptor parity error, byte 2
63	CIR rank BDP descriptor parity error, byte 3

PROC-990 PFS2 REGISTER (82)



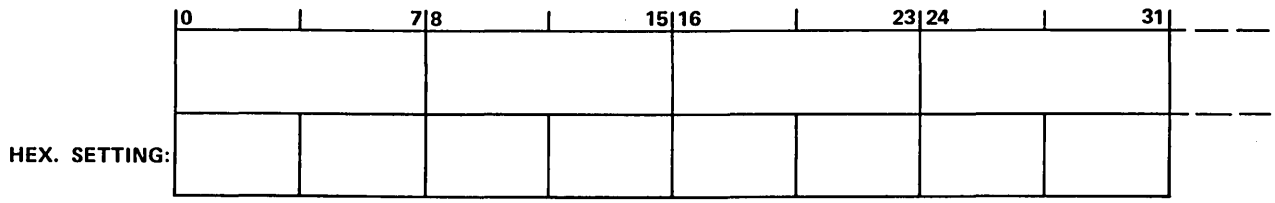
Bit	Description
00	CSA rank P register parity error, byte 0
01	CSA rank P register parity error, byte 1
02	CSA rank P register parity error, byte 2
03	CSA rank P register parity error, byte 3
04	CSD rank P register parity error, byte 0
05	CSD rank P register parity error, byte 1
06	CSD rank P register parity error, byte 2
07	CSD rank P register parity error, byte 3
08	CWD rank P register parity error, byte 0
09	CWD rank P register parity error, byte 1
10	CWD rank P register parity error, byte 2
11	CWD rank P register parity error, byte 3
12	CIR rank P register parity error, byte 0
13	CIR rank P register parity error, byte 1
14	CIR rank P register parity error, byte 2
15	CIR rank P register parity error, byte 3
16	CSA rank UTP address register parity error, byte 0
17	CSA rank UTP address register parity error, byte 1
18	CSA rank UTP address register parity error, byte 2
19	CSA rank UTP address register parity error, byte 3
20	CWA rank UTP address register parity error, byte 0
21	CWA rank UTP address register parity error, byte 1
22	CWA rank UTP address register parity error, byte 2
23	CWA rank UTP address register parity error, byte 3
24	CIR rank UTP address register parity error, byte 0
25	CIR rank UTP address register parity error, byte 1
26	CIR rank UTP address register parity error, byte 2
27	CIR rank UTP address register parity error, byte 3
28	CSA instruction register parity error, byte 0
29	CSA instruction register parity error, byte 1
30	CSA instruction register parity error, byte 2
31	CSA instruction register parity error, byte 3

PROC-990 PFS2 REGISTER (82)



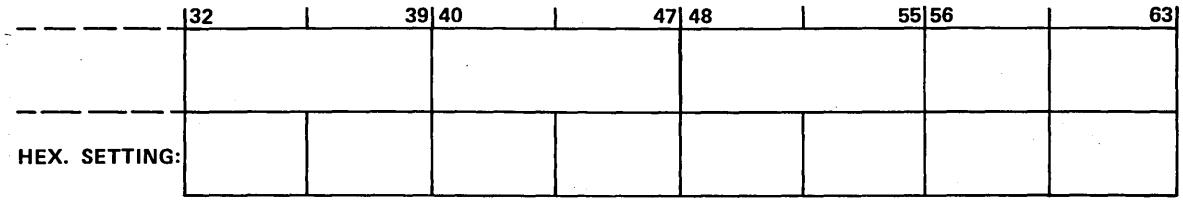
Bit	Description
32	CSD instruction register parity error, byte 0
33	CSD instruction register parity error, byte 1
34	CSD instruction register parity error, byte 2
35	CSD instruction register parity error, byte 3
36	CWA instruction register parity error, byte 0
37	CWA instruction register parity error, byte 1
38	CWA instruction register parity error, byte 2
39	CWA instruction register parity error, byte 3
40	CSA rank J descriptor parity error, byte 0
41	CSA rank J descriptor parity error, byte 1
42	CSA rank J descriptor parity error, byte 2
43	CSA rank J descriptor parity error, byte 3
44	CSD rank J descriptor parity error, byte 0
45	CSD rank J descriptor parity error, byte 1
46	CSD rank J descriptor parity error, byte 2
47	CSD rank J descriptor parity error, byte 3
48	CWA rank J descriptor parity error, byte 0
49	CWA rank J descriptor parity error, byte 1
50	CWA rank J descriptor parity error, byte 2
51	CWA rank J descriptor parity error, byte 3
52	CSA rank K descriptor parity error, byte 0
53	CSA rank K descriptor parity error, byte 1
54	CSA rank K descriptor parity error, byte 2
55	CSA rank K descriptor parity error, byte 3
56	CSD rank K descriptor parity error, byte 0
57	CSD rank K descriptor parity error, byte 1
58	CSD rank K descriptor parity error, byte 2
59	CSD rank K descriptor parity error, byte 3
60	CWA rank K descriptor parity error, byte 0
61	CWA rank K descriptor parity error, byte 1
62	CWA rank K descriptor parity error, byte 2
63	CWA rank K descriptor parity error, byte 3

PROC-990 PFS3 REGISTER (83)



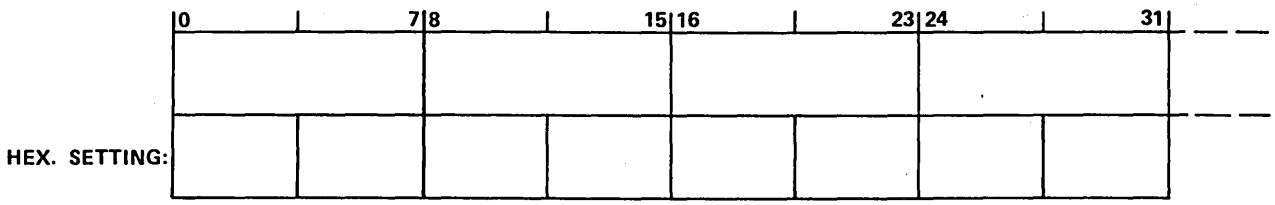
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	Illegal soft control address auxiliary 1
04	Illegal soft control address auxiliary 2
05	LSU mark lines parity error
06	Immediate data, scale count parity error
07	Mark lines parity error
08	AJ data parity error, byte 0
09	AJ data parity error, byte 1
10	AJ data parity error, byte 2
11	AJ data parity error, byte 3
12	AJ data parity error, byte 4
13	AJ data parity error, byte 5
14	AJ data parity error, byte 6
15	AJ data parity error, byte 7
16	AJ data hold register parity error, byte 0
17	AJ data hold register parity error, byte 1
18	AJ data hold register parity error, byte 2
19	AJ data hold register parity error, byte 3
20	AJ data hold register parity error, byte 4
21	AJ data hold register parity error, byte 5
22	AJ data hold register parity error, byte 6
23	AJ data hold register parity error, byte 7
24	AK data register parity error, byte 0
25	AK data register parity error, byte 1
26	AK data register parity error, byte 2
27	AK data register parity error, byte 3
28	AK data register parity error, byte 4
29	AK data register parity error, byte 5
30	AK data register parity error, byte 6
31	AK data register parity error, byte 7

PROC-990 PFS3 REGISTER (83)



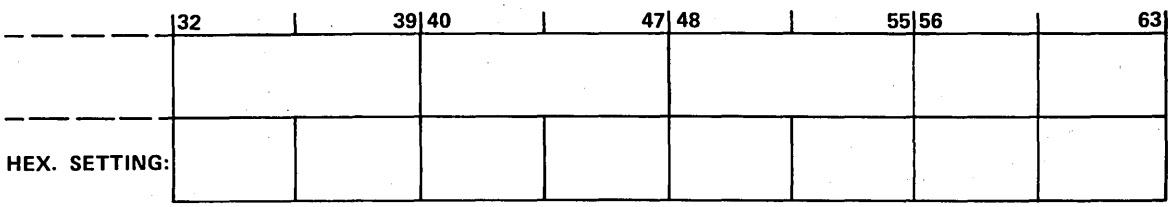
Bit	Description
32	AK data hold register parity error, byte 0
33	AK data hold register parity error, byte 1
34	AK data hold register parity error, byte 2
35	AK data hold register parity error, byte 3
36	AK data hold register parity error, byte 4
37	AK data hold register parity error, byte 5
38	AK data hold register parity error, byte 6
39	AK data hold register parity error, byte 7
40	AJ descriptor
41	AK descriptor
42	J length counter subtrahend
43	K length counter subtrahend
44	J length count
45	J length count after subtract
46	K length count
47	K length count after subtract
48	Output data parity error, byte 0
49	Output data parity error, byte 1
50	Output data parity error, byte 2
51	Output data parity error, byte 3
52	Output data parity error, byte 4
53	Output data parity error, byte 5
54	Output data parity error, byte 6
55	Output data parity error, byte 7
56	Soft control memory parity error, board 1
57	Soft control memory parity error, board 2
58	Convert data hold register parity error
59	Convert data register parity error
60	IOU micrand register parity error
61	IOU micrand register parity error, byte 1
62	Soft control address parity error, board 1
63	Soft control address parity error, board 2

PROC-990 PFS4 REGISTER (84)



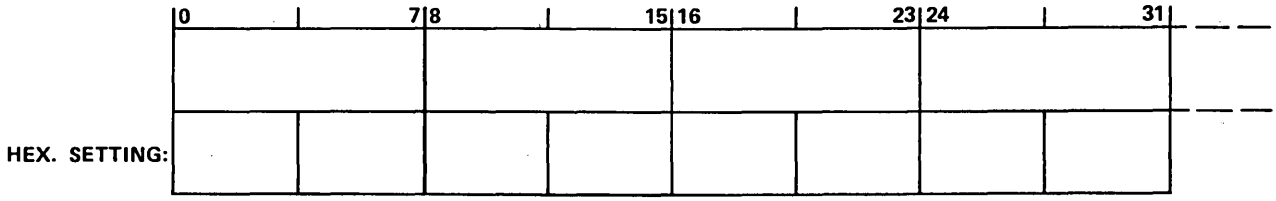
Bit	Description
00	IMU/FPM compare fault
01	Divide miscompare
02	BDP byte parity error
03	(Not used)
↓	↓
31	(Not used)

PROC-990 PFS4 REGISTER (84)



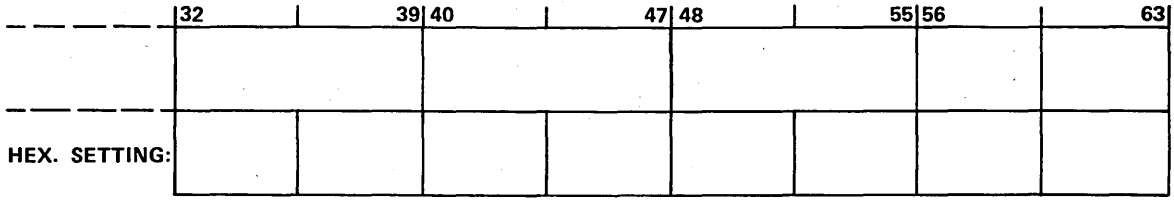
Bit	Description
32	(Not used)
33	(Not used)
34	Rank 6 error
35	Invalid SCM 4
36	Port A tag
37	SCM4 function code
38	Page map multiple hit
39	SCM4 parity error
40	Port A RMA register parity error, byte 0
41	Port A RMA register parity error, byte 1
42	Port A RMA register parity error, byte 2
43	Port A RMA register parity error, byte 3
44	Port B RMA register parity error, byte 0
45	Port B RMA register parity error, byte 1
46	Port B RMA register parity error, byte 2
47	Port B RMA register parity error, byte 3
48	Port C RMA register parity error, byte 0
49	Port C RMA register parity error, byte 1
50	Port C RMA register parity error, byte 2
51	Port C RMA register parity error, byte 3
52	Port C SVA register parity error, byte 0
53	Port C SVA register parity error, byte 1
54	Port C SVA register parity error, byte 2
55	Port C SVA register parity error, byte 3
56	Port A length counter parity error, byte 0
57	Port A length counter parity error, byte 1
58	Port C length counter parity error, byte 2
59	Port C length counter parity error, byte 3
60	Port C store tag parity error
61	Rank 6 PFSA register parity error, byte 0
62	Rank 6 PFSA register parity error, byte 1
63	Rank 6 PFSA register parity error, byte 2

PROC-990 PSF5 REGISTER (85)



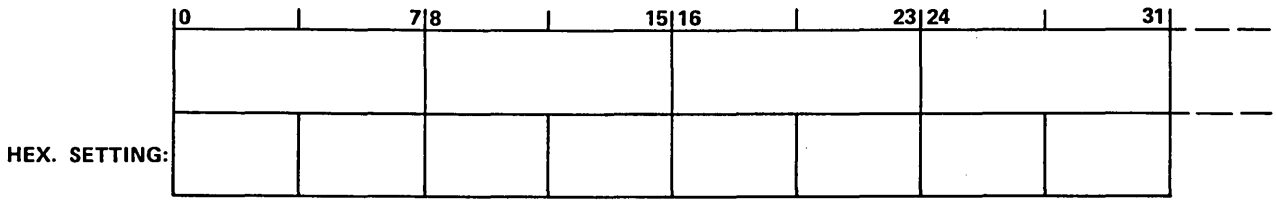
Bit	Description
00	Page table address, byte 0
01	Page table address, byte 1
02	Rank 4/5 SVA parity error, byte 0
03	Rank 4/5 SVA parity error, byte 1
04	Rank 4/5 SVA parity error, byte 2
05	Rank 4/5 SVA parity error, byte 3
06	Rank 4/5 SVA parity error, byte 4
07	Rank 4/5 SVA parity error, byte 5
08	Page table length parity error
09	Rank 6 SVA parity error, byte 0
10	Rank 6 SVA parity error, byte 1
11	Rank 6 SVA parity error, byte 2
12	Rank 6 SVA parity error, byte 3
13	Rank 6 SVA parity error, byte 4
14	Rank 6 SVA parity error, byte 5
15	Rank 6 SVA parity error, byte 6
16	Rank 5 ring/segment parity error, byte 0
17	Rank 5 ring/segment parity error, byte 1
18	Cache purge SVA parity error, byte 0
19	Cache purge SVA parity error, byte 1
20	Cache purge SVA parity error, byte 2
21	Cache purge SVA parity error, byte 3
22	Cache purge SVA parity error, byte 4
23	Cache purge SVA parity error, byte 5
24	Rank 6 ring/segment parity error, byte 0
25	Rank 6 ring/segment parity error, byte 1
26	Rank 6 LSU tag parity error, byte 0
27	Rank 6 LSU tag parity error, byte 1
28	Rank 6 LSU tag parity error, byte 2
29	Rank 6 LSU tag parity error, byte 3
30	Rank 6 LSU tag parity error, byte 4
31	Rank 6 LSU tag parity error, byte 5

PROC-990 PSF5 REGISTER (85)



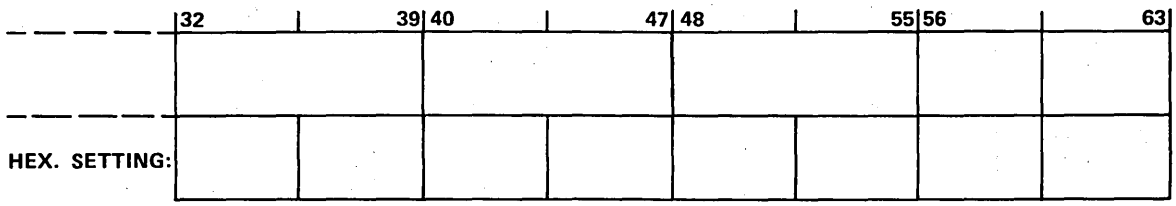
Bit	Description
32	SDE/PTE parity error, byte 0
33	SDE/PTE parity error, byte 1
34	SDE/PTE parity error, byte 2
35	SDE/PTE parity error, byte 3
36	SDE/PTE parity error, byte 4
37	SDE/PTE parity error, byte 5
38	SDE/PTE parity error, byte 6
39	SDE/PTE parity error, byte 7
40	Alternate PTE parity error, byte 0
41	Alternate PTE parity error, byte 1
42	Alternate PTE parity error, byte 2
43	Segment/page identifier parity error, byte 0
44	Segment/page identifier parity error, byte 1
45	Segment/page identifier parity error, byte 2
46	Segment/page identifier parity error, byte 3
47	Segment/page identifier parity error, byte 4
48	Debug mask parity error
49	Page size mask parity error
50	Data result parity error, byte 0
51	Data result parity error, byte 1
52	Data result parity error, byte 2
53	Data result parity error, byte 3
54	Data result parity error, byte 4
55	Data result parity error, byte 5
56	Miss tag parity error, byte 0
57	Miss tag parity error, byte 1
58	Miss tag parity error, byte 2
59	Miss tag parity error, byte 3
60	Page map parity error, set 0
61	Page map parity error, set 1
62	Page map parity error, set 2
63	Page map parity error, set 3

PROC-990 PFS6 REGISTER (86)



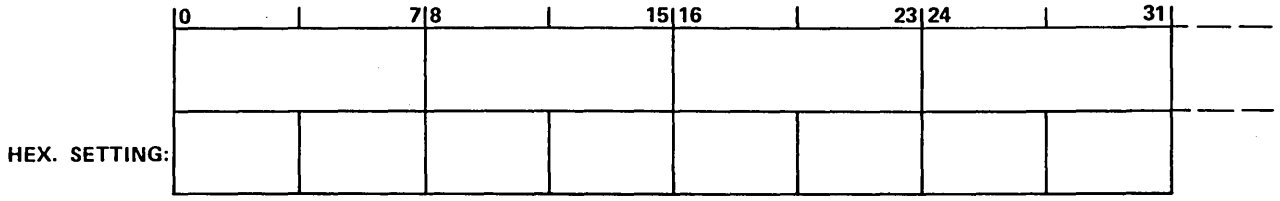
Bit	Description
00	Micrand parity error, byte 0
01	Micrand parity error, byte 1
02	Micrand parity error, byte 2
03	Micrand parity error, byte 3
04	Immediate byte, scale count parity error
05	Buffer address parity error
06	Register file A address parity error
07	Register file B address parity error
08	Register file A data out parity error
09	Edit mask parity error
10	Decimal convert parity error
11	C stream adder parity error
12	AJ descriptor parity error
13	AK descriptor parity error
14	A port stage-2 data parity error
15	B port stage-2 data parity error
16	C stream stage-7 data parity error
17	Table load limit register parity error
18	Register file B data-out parity error
19	C stream stage-4 address (convert) parity error
20	C stream stage-4 address (EBCDIC) parity error
21	ROM address (specification error, X256) parity error
22	ROM address (specification error, X256) parity error
23	A port stage-1 data parity error
24	C stream stage-5 data parity error (EBCDIC)
25	Convert data-out parity error
26	B port stage-1 data parity error
27	Write address parity error
28	MAC write data parity error
29	Error on SCM 2
30	Error on SCM 3
31	Error on MEM-990 rank 4

PROC-990 PFS6 REGISTER (86)



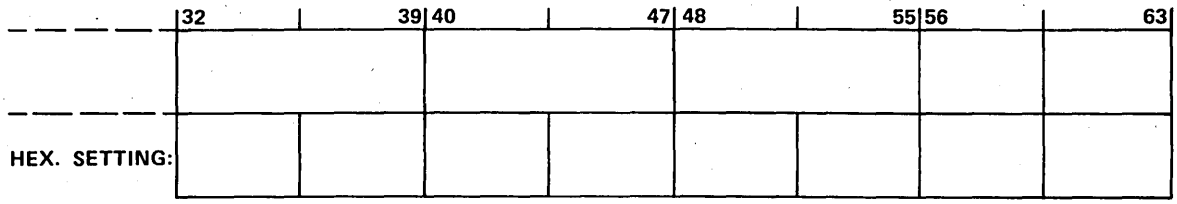
Bit	Description
32	Error on transfer count from IDU
33	Instruction descriptor parity error, byte 0
34	Instruction descriptor parity error, byte 1
35	Instruction descriptor parity error, byte 2
36	BDP descriptor parity error, byte 0
37	BDP descriptor parity error, byte 1
38	BDP descriptor parity error, byte 2
39	BDP descriptor parity error, byte 3
40	M1 micrand register parity error, byte 0
41	M1 micrand register parity error, byte 1
42	M1 micrand register parity error, byte 2
43	M1 micrand register parity error, byte 3
44	Parity error on P-right from IN1, byte 0
45	Parity error on P-right from IN1, byte 1
46	Parity error on P-right from IN1, byte 2
47	Parity error on P-right from IN1, byte 3
48	SVA BN register parity error, byte 0
49	SVA BN register parity error, byte 1
50	SVA BN register parity error, byte 2
51	SVA BN register parity error, byte 3
52	SVA BN buffer register parity error, byte 0
53	SVA BN buffer register parity error, byte 1
54	SVA BN buffer register parity error, byte 2
55	SVA BN buffer register parity error, byte 3
56	Increment adder operand A parity error, byte 0
57	Increment adder operand A parity error, byte 1
58	Increment adder operand A parity error, byte 2
59	Increment adder operand A parity error, byte 3
60	Increment adder operand B parity error, byte 0
61	Increment adder operand B parity error, byte 1
62	Increment adder operand B parity error, byte 2
63	Increment adder operand B parity error, byte 3

PROC-990 PFS7 REGISTER (87)



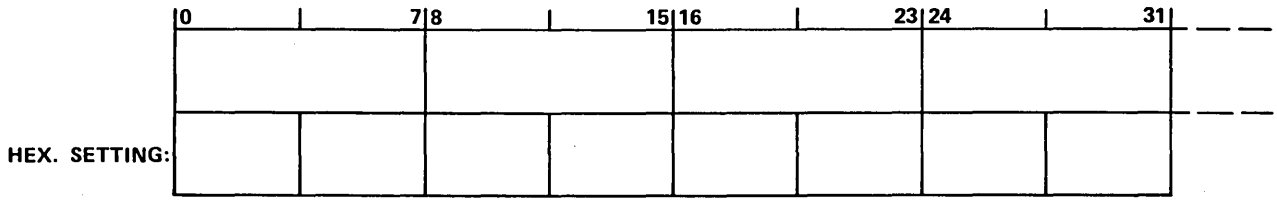
Bit	Description
00	Data error on SDE RMA adder, byte 0
01	Data error on SDE RMA adder, byte 1
02	Data error on SDE RMA adder, byte 2
03	Data error on SDE RMA adder, byte 3
04	Carry error on SDE RMA adder, byte 0
05	Carry error on SDE RMA adder, byte 1
06	Carry error on SDE RMA adder, byte 2
07	Length mux/register parity error
08	Rank 4 SDE register copy 1 parity error, byte 0
09	Rank 4 SDE register copy 1 parity error, byte 1
10	Rank 4 SDE register copy 1 parity error, byte 2
11	Instruction descriptor parity error, bits 16 through 23 copy 2
12	Segment table length parity error, byte 0
13	Segment table length parity error, byte 1
14	Rank 3 function code parity error
15	Rank 4 function code parity error
16	Rank 3 LSU microrand parity error
17	Rank 5 LSU tag parity error, byte 0
18	Rank 5 LSU tag parity error, byte 1
19	Rank 5 LSU tag parity error, byte 2
20	Rank 4 LSU tag parity error
21	Rank 5 LSU tag parity error, byte 0
22	Rank 5 LSU tag parity error, byte 1
23	Rank 5 LSU tag parity error, byte 2
24	Invalid function code, MEM-835, 990
25	Invalid function code, MEM-845 through 860
26	Rank 3 RN/SEG register parity error, byte 0
27	Rank 3 RN/SEG register parity error, byte 1
28	Rank 4 RN/SEG register parity error, byte 0
29	Rank 4 RN/SEG register parity error, byte 1
30	Rank 3 RN/SEG buffer parity error, byte 0
31	Rank 3 RN/SEG buffer parity error, byte 1

PROC-990 PFS7 REGISTER (87)



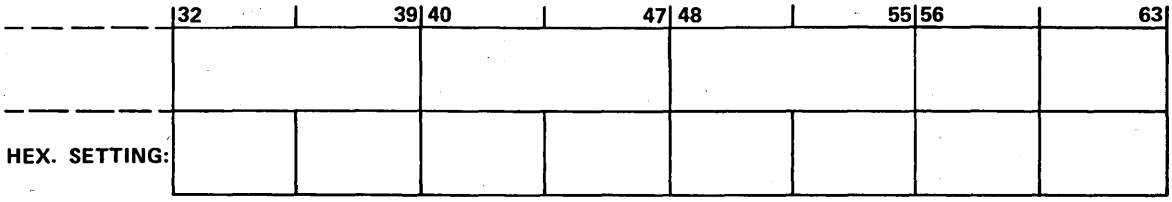
Bit	Description
32	RN/SEG holding register parity error, byte 0
33	RN/SEG holding register parity error, byte 1
34	Vector length register parity error, byte 0
35	Vector length register parity error, byte 1
36	P-left register parity error, byte 0
37	P-left register parity error, byte 1
38	P-left register parity error, byte 2
39	P-left register parity error, byte 3
40	New P-segment holding register parity error, byte 0
41	New P-segment holding register parity error, byte 1
42	New P-ring holding register parity error
43	B counter register parity error
44	ASID holding register parity error, byte 0
45	ASID holding register parity error, byte 1
46	Rank 4 ASID register parity error, byte 0
47	Rank 4 ASID register parity error, byte 1
48	Global key parity error
49	RAC+FLC register parity error, byte 0
50	RAC+FLC register parity error, byte 1
51	RAC+FLC register parity error, byte 2
52	Local key parity error
53	RAE+FLE register parity error, byte 0
54	RAE+FLE register parity error, byte 1
55	RAE+FLE register parity error, byte 2
56	Segment map error, set 0
57	Segment map error, set 1
58	Segment map error, multiple hit
59	(Not used)
60	(Not used)
61	(Not used)
62	(Not used)
63	(Not used)

PROC-990 PFS8 REGISTER (88)



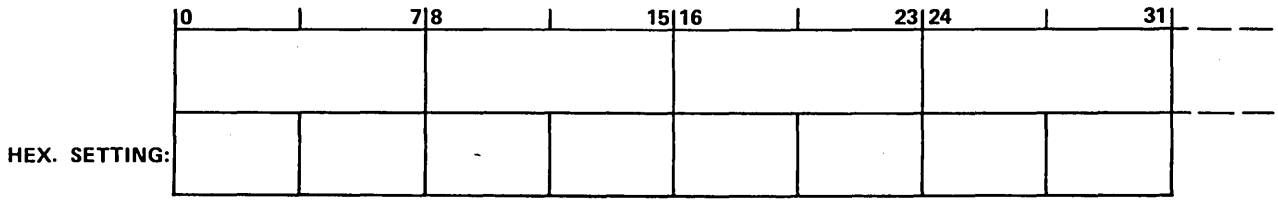
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	(Not used)
04	(Not used)
05	(Not used)
06	(Not used)
07	(Not used)
08	Load BDP latch parity error, byte 0
09	Load BDP latch parity error, byte 1
10	Load BDP latch parity error, byte 2
11	Load BDP latch parity error, byte 3
12	Load BDP latch parity error, byte 4
13	Load BDP latch parity error, byte 5
14	Load BDP latch parity error, byte 6
15	Load BDP latch parity error, byte 7
16	Load state latch parity error, byte 0
17	Load state latch parity error, byte 1
18	Load state latch parity error, byte 2
19	Load state latch parity error, byte 3
20	Load state latch parity error, byte 4
21	Load state latch parity error, byte 5
22	Load state latch parity error, byte 6
23	Load state latch parity error, byte 7
24	A-data buffer output latch parity error, byte 0
25	A-data buffer output latch parity error, byte 1
26	A-data buffer output latch parity error, byte 2
27	A-data buffer output latch parity error, byte 3
28	A-data buffer output latch parity error, byte 4
29	A-data buffer output latch parity error, byte 5
30	A-data buffer output latch parity error, byte 6
31	A-data buffer output latch parity error, byte 7

PROC-990 PFS8 REGISTER (88)



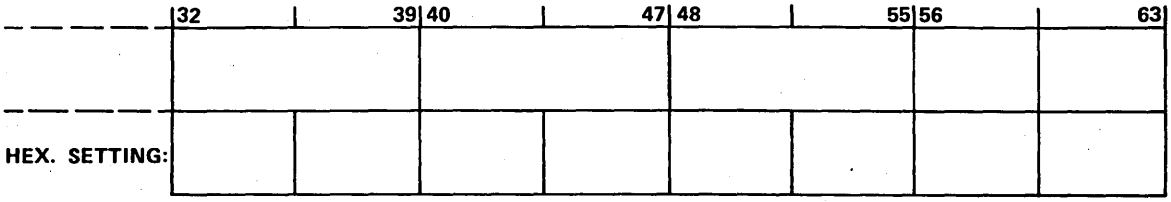
Bit	Description
32	A-data buffer output latch 1 parity error, byte 0
33	A-data buffer output latch 1 parity error, byte 1
34	A-data buffer output latch 1 parity error, byte 2
35	A-data buffer output latch 1 parity error, byte 3
36	A-data buffer output latch 1 parity error, byte 4
37	A-data buffer output latch 1 parity error, byte 5
38	A-data buffer output latch 1 parity error, byte 6
39	A-data buffer output latch 1 parity error, byte 7
40	A-data buffer output latch 2 parity error, byte 0
41	A-data buffer output latch 2 parity error, byte 1
42	A-data buffer output latch 2 parity error, byte 2
43	A-data buffer output latch 2 parity error, byte 3
44	A-data buffer output latch 2 parity error, byte 4
45	A-data buffer output latch 2 parity error, byte 5
46	A-data buffer output latch 2 parity error, byte 6
47	A-data buffer output latch 2 parity error, byte 7
48	B-data buffer output latch parity error, byte 0
49	B-data buffer output latch parity error, byte 1
50	B-data buffer output latch parity error, byte 2
51	B-data buffer output latch parity error, byte 3
52	B-data buffer output latch parity error, byte 4
53	B-data buffer output latch parity error, byte 5
54	B-data buffer output latch parity error, byte 6
55	B-data buffer output latch parity error, byte 7
56	B-input data latch parity error, byte 0
57	B-input data latch parity error, byte 1
58	B-input data latch parity error, byte 2
59	B-input data latch parity error, byte 3
60	B-input data latch parity error, byte 4
61	B-input data latch parity error, byte 5
62	B-input data latch parity error, byte 6
63	B-input data latch parity error, byte 7

PROC-990 PFS9 REGISTER (89)



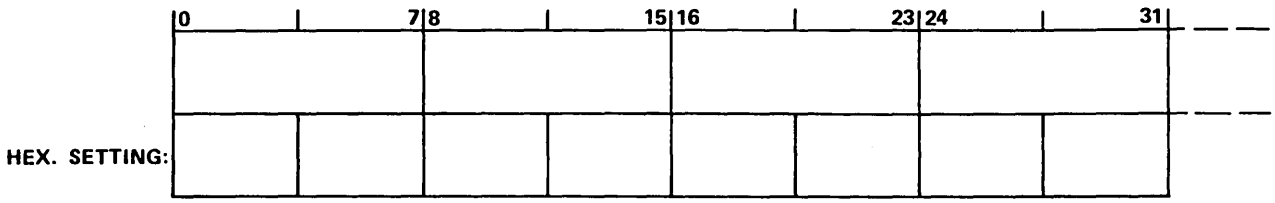
Bit	Description
00	Load X latch parity error, byte 0
01	Load X latch parity error, byte 1
02	Load X latch parity error, byte 2
03	Load X latch parity error, byte 3
04	Load X latch parity error, byte 4
05	Load X latch parity error, byte 5
06	Load X latch parity error, byte 6
07	Load X latch parity error, byte 7
08	Store input latch 2 parity error, byte 0
09	Store input latch 2 parity error, byte 1
10	Store input latch 2 parity error, byte 2
11	Store input latch 2 parity error, byte 3
12	Store input latch 2 parity error, byte 4
13	Store input latch 2 parity error, byte 5
14	Store input latch 2 parity error, byte 6
15	Store input latch 2 parity error, byte 7
16	Store buffer output latch parity error, byte 0
17	Store buffer output latch parity error, byte 1
18	Store buffer output latch parity error, byte 2
19	Store buffer output latch parity error, byte 3
20	Store buffer output latch parity error, byte 4
21	Store buffer output latch parity error, byte 5
22	Store buffer output latch parity error, byte 6
23	Store buffer output latch parity error, byte 7
24	Store data latch 3 parity error, byte 0
25	Store data latch 3 parity error, byte 1
26	Store data latch 3 parity error, byte 2
27	Store data latch 3 parity error, byte 3
28	Store data latch 3 parity error, byte 4
29	Store data latch 3 parity error, byte 5
30	Store data latch 3 parity error, byte 6
31	Store data latch 3 parity error, byte 7

PROC-990 PFS9 REGISTER (89)



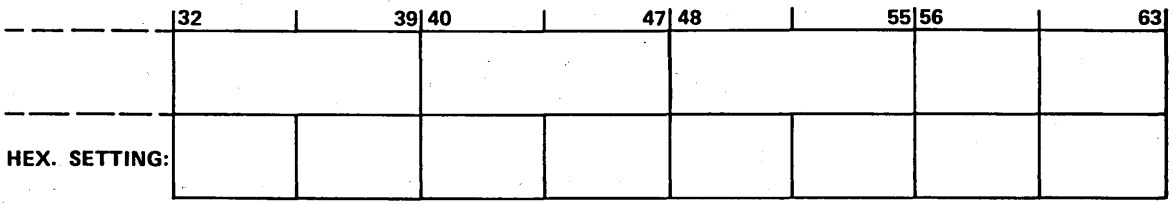
Bit	Description
32	Load A input data latch parity error, byte 0
33	Load A input data latch parity error, byte 1
34	Load A input data latch parity error, byte 2
35	Load A input data latch parity error, byte 3
36	Load A input data latch parity error, byte 4
37	Load A input data latch parity error, byte 5
38	Load A input data latch parity error, byte 6
39	Load A input data latch parity error, byte 7
40	Load A 170 RAC latch parity error, byte 0
41	Load A 170 RAC latch parity error, byte 1
42	Load A 170 RAC latch parity error, byte 2
43	Load A 170 RAC latch parity error, byte 3
44	Load A 170 temp latch parity error, byte 0
45	Load A 170 temp latch parity error, byte 1
46	Load A 170 temp latch parity error, byte 2
47	Load A 170 temp latch parity error, byte 3
48	Store mark byte output parity error
49	BDP store mark lines input latch parity error
50	Hit buffer input latch parity error, byte 0
51	Hit buffer input latch parity error, byte 1
52	Hit buffer input latch parity error, byte 2
53	Hit buffer input latch parity error, byte 3
54	Hit buffer input latch parity error, byte 4
55	Hit buffer input latch parity error, byte 5
56	BDP store control latch parity error
57	BDP load control input latch parity error
58	Hit buffer output latch parity error, byte 0
59	Hit buffer output latch parity error, byte 1
60	Hit buffer output latch parity error, byte 2
61	Hit buffer output latch parity error, byte 3
62	Hit buffer output latch parity error, byte 4
63	Hit buffer output latch parity error, byte 5

PROC-990 PFSA REGISTER (8A)



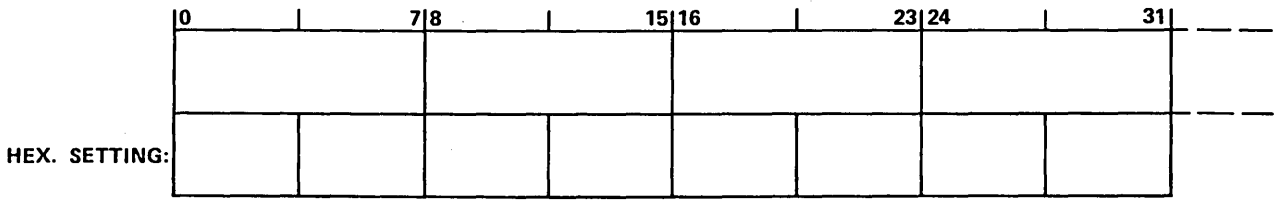
Bit	Description
00	Load control mux/latch parity error, byte 0
01	Load control mux/latch parity error, byte 1
02	Load control mux/latch parity error, byte 2
03	Load control mux/latch parity error, byte 3
04	Load control mux/latch parity error, byte 4
05	Load control mux/latch parity error, byte 5
06	Load control mux/latch parity error, byte 6
07	Load control mux/latch parity error, byte 7
08	Load control mux/latch parity error, byte 8
09	Load control mux/latch parity error, byte 9
10	Load control mux/latch parity error, byte 10
11	Load control mux/latch parity error, byte 11
12	Load control mux/latch parity error, byte 12
13	Load control mux/latch parity error, byte 13
14	Vector control input latch parity error
15	Illegal soft control access
16	IDU control latch parity error, byte 0
17	IDU control latch parity error, byte 1
18	IDU control latch parity error, byte 2
19	IDU control latch parity error, byte 3
20	IDU control latch parity error, byte 4
21	ACU control latch parity error, byte 0
22	ACU control latch parity error, byte 1
23	ACU control latch parity error, byte 2
24	Vector tag input latch parity error, byte 0
25	Vector tag input latch parity error, byte 1
26	IDU load control input latch parity error, byte 0
27	IDU load control input latch parity error, byte 1
28	IDU load control input latch parity error, byte 2
29	IDU load control input latch parity error, byte 3
30	IDU load control input latch parity error, byte 4
31	IDU load control input latch parity error, byte 5

PROC-990 PFSA REGISTER (8A)



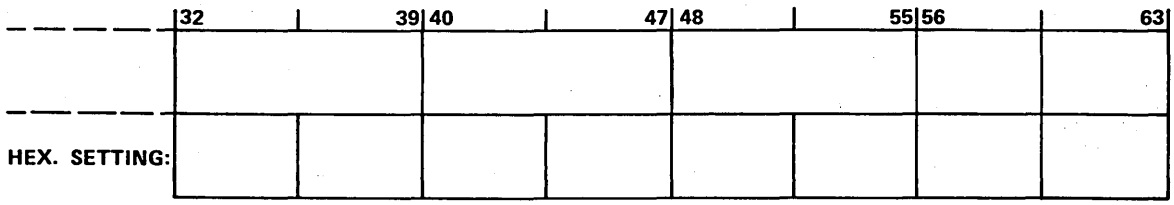
Bit	Description
32	Vector tag output latch parity error, byte 0
33	Vector tag output latch parity error, byte 1
34	B-control buffer ACU output latch parity error, byte 0
35	B-control buffer ACU output latch parity error, byte 1
36	B-control buffer ACU output latch parity error, byte 2
37	B-control buffer ACU output latch parity error, byte 3
38	B-control buffer ACU output latch parity error, byte 4
39	B-control buffer ACU output latch parity error, byte 5
40	B-control buffer IOU output latch parity error, byte 0
41	B-control buffer IOU output latch parity error, byte 1
42	B-control buffer IOU output latch parity error, byte 2
43	B-control buffer IOU output latch parity error, byte 3
44	B-control buffer IOU output latch parity error, byte 4
45	B-control buffer IOU output latch parity error, byte 5
46	B-control buffer IOU output latch parity error, byte 6
47	B-control buffer IOU output latch parity error, byte 7
48	Soft-control load input latch parity error, byte 0
49	Soft-control load input latch parity error, byte 1
50	Soft-control load input latch parity error, byte 2
51	Soft-control load input latch parity error, byte 3
52	Load control latch 2 parity error, byte 0
53	Load control latch 2 parity error, byte 1
54	Load control latch 2 parity error, byte 2
55	Load control latch 2 parity error, byte 3
56	Load control latch 3 parity error
57	MAC load control latch parity error
58	Load A output latch 1 parity error
59	Load A output latch 2 parity error, byte 0
60	Load A output latch 2 parity error, byte 1
61	Load A output latch 3 parity error, byte 0
62	Load A output latch 3 parity error, byte 1
63	Load A output latch 3 parity error, byte 2

PROC-990 PFSB REGISTER (8B)



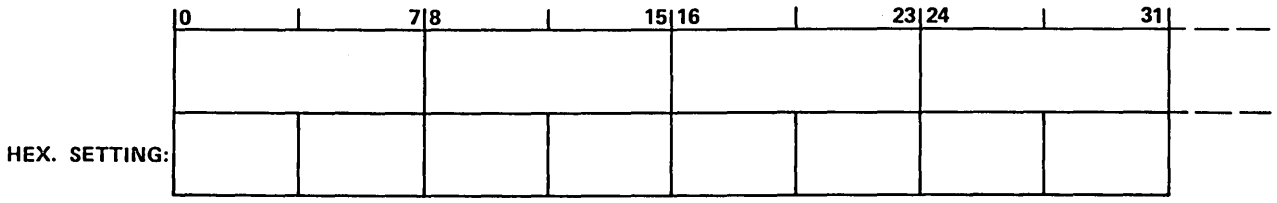
Bit	Description
00	Store control input latch 1 parity error, byte 0
01	Store control input latch 1 parity error, byte 1
02	Store control input latch 1 parity error, byte 2
03	Store control input latch 1 parity error, byte 3
04	Store control input latch 2 parity error, byte 0
05	Store control input latch 2 parity error, byte 1
06	Store control input latch 2 parity error, byte 2
07	Store control input latch 2 parity error, byte 3
08	Store control select mux latch parity error, byte 0
09	Store control select mux latch parity error, byte 1
10	Store control select mux latch parity error, byte 2
11	Store control select mux latch parity error, byte 3
12	Store control latch 2 parity error, byte 0
13	Store control latch 2 parity error, byte 1
14	Store control latch 3 parity error
15	(Not used)
16	(Not used)
17	(Not used)
18	(Not used)
19	(Not used)
20	(Not used)
21	Issue time-out
22	RPL rank 12 parity error, byte 0
23	RPL rank 12 parity error, byte 1
24	RPL rank 12 parity error, byte 2
25	RPL rank 11 parity error, byte 0
26	RPL rank 11 parity error, byte 1
27	RPL rank 11 parity error, byte 2
28	RPL rank 10 parity error, byte 0
29	RPL rank 10 parity error, byte 1
30	RPL rank 10 parity error, byte 2
31	RPL rank 9 parity error, byte 0

PROC-990 PFSB REGISTER (8B)



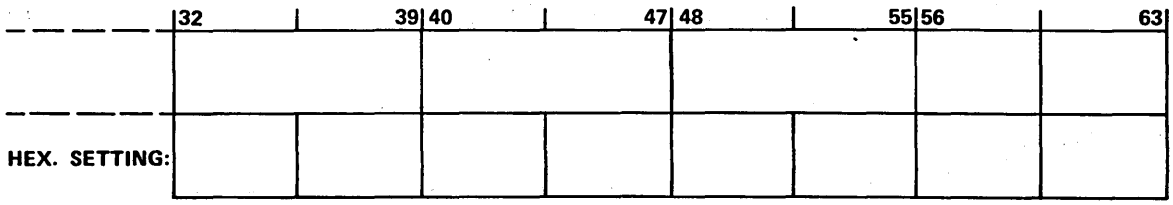
Bit	Description
32	RPL rank 9 parity error, byte 1
33	RPL rank 9 parity error, byte 2
34	RPL rank 8 parity error, byte 0
35	RPL rank 8 parity error, byte 1
36	RPL rank 8 parity error, byte 2
37	RPL rank 7 parity error, byte 0
38	RPL rank 7 parity error, byte 1
39	RPL rank 7 parity error, byte 2
40	RPL rank 6 parity error, byte 0
41	RPL rank 6 parity error, byte 1
42	RPL rank 6 parity error, byte 2
43	RPL rank 5 parity error, byte 0
44	RPL rank 5 parity error, byte 1
45	RPL rank 5 parity error, byte 2
46	RPL rank 4 parity error, byte 0
47	RPL rank 4 parity error, byte 1
48	RPL rank 4 parity error, byte 2
49	RPL rank 3 parity error, byte 0
50	RPL rank 3 parity error, byte 1
51	RPL rank 3 parity error, byte 2
52	RPL rank 2 parity error, byte 0
53	RPL rank 2 parity error, byte 1
54	RPL rank 2 parity error, byte 2
55	RPL rank 1 parity error
56	Issue time-out error, bit 0
57	Issue time-out error, bit 1
58	Issue time-out error, bit 2
59	Issue time-out error, bit 3
60	Issue time-out error, bit 4
61	Issue time-out error, bit 5
62	Issue time-out error, bit 6
63	Issue time-out error, bit 7

PROC-990 PFSC REGISTER (8C)



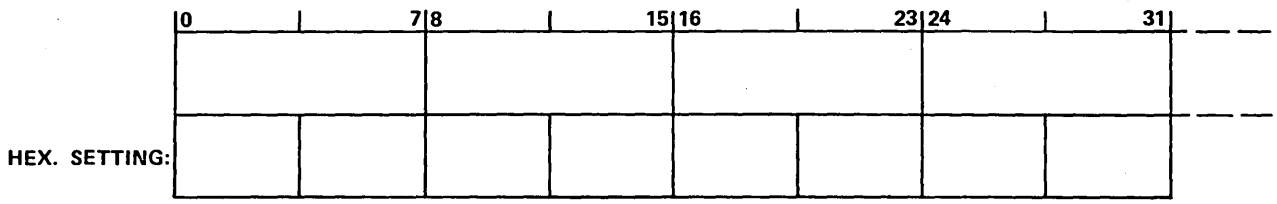
Bit	Description
00	State load latch rank 1 parity error, byte 0
01	State load latch rank 1 parity error, byte 1
02	State load latch rank 1 parity error, byte 2
03	State load latch rank 1 parity error, byte 3
04	State load mux latch rank 1 parity error, byte 4
05	State load mux latch rank 1 parity error, byte 5
06	State load mux latch rank 1 parity error, byte 6
07	State load mux latch rank 1 parity error, byte 7
08	State load latch rank 2 parity error, byte 0
09	State load latch rank 2 parity error, byte 1
10	State load latch rank 2 parity error, byte 2
11	State load latch rank 2 parity error, byte 3
12	State load latch rank 2 parity error, byte 4
13	State load latch rank 2 parity error, byte 5
14	State load latch rank 2 parity error, byte 6
15	State load latch rank 2 parity error, byte 7
16	Store tag data latch parity error, byte 0
17	Store tag data latch parity error, byte 1
18	Store tag history buffer latch parity error, byte 0
19	Store tag history buffer latch parity error, byte 1
20	Load error parity error, byte 0
21	Load error parity error, byte 1
22	State load RK 2 parity error, byte 6
23	State load RK 2 parity error, byte 7
24	State output mux register parity error, byte 0
25	State output mux register parity error, byte 1
26	State output mux register parity error, byte 2
27	State output mux register parity error, byte 3
28	State output mux register parity error, byte 4
29	State output mux register parity error, byte 5
30	State output mux register parity error, byte 6
31	State output mux register parity error, byte 7

PROC-990 PFSC REGISTER (8C)



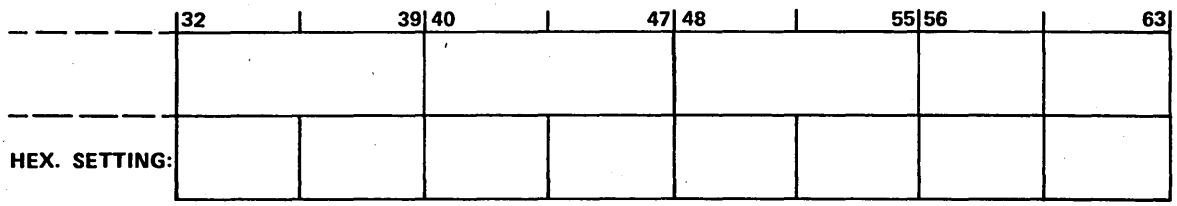
Bit	Description
32	State read mux parity error, byte 0
33	State read mux parity error, byte 1
34	State read mux parity error, byte 2
35	State read mux parity error, byte 3
36	State read mux parity error, byte 4
37	State read mux parity error, byte 5
38	State read mux parity error, byte 6
39	State read mux parity error, byte 7
40	History tag parity error, byte 0
41	History tag parity error, byte 1
42	Load path tag parity error
43	History tag path parity error, byte 0
44	History tag path parity error, byte 1
45	History tag path parity error, byte 2
46	History tag path parity error, byte 3
47	History tag path parity error, byte 4
48	MAC write data parity error
49	MAC read data parity error
50	UTP buffer register parity error, byte 0
51	UTP buffer register parity error, byte 1
52	UTP buffer register parity error, byte 2
53	UTP buffer register parity error, byte 3
54	UTP buffer register parity error, byte 4
55	UTP buffer register parity error, byte 5
56	Assembly/disassembly parity error, byte 0
57	Assembly/disassembly parity error, byte 1
58	Assembly/disassembly parity error, byte 2
59	Assembly/disassembly parity error, byte 3
60	Assembly/disassembly parity error, byte 4
61	Assembly/disassembly parity error, byte 5
62	Assembly/disassembly parity error, byte 6
63	Assembly/disassembly parity error, byte 7

PROC-990 PFSD REGISTER (8D)



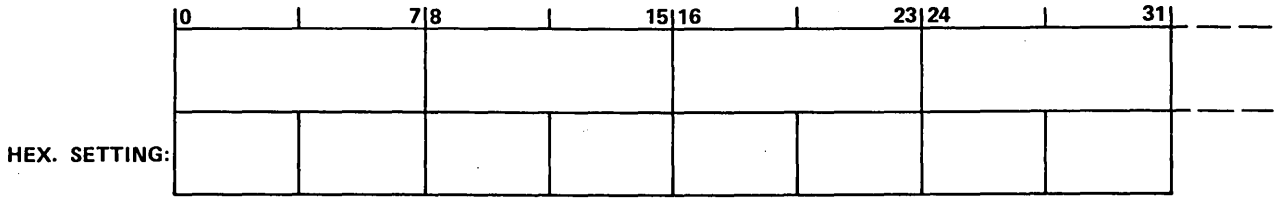
Bit	Description
00	Response latch parity error, byte 0
01	Response latch parity error, byte 1
02	Response latch parity error, byte 2
03	JPS auxiliary board FU 1A parity error
04	JPS auxiliary board FU 1B parity error
05	User mark or monitor mark parity error
06	MDW byte 0 parity error
07	MDW byte 1 parity error
08	(Not used)
09	PTL, STL, or KM parity error
10	Auxiliary board FU 1C parity error
11	Auxiliary board FU 1B parity error
12	Auxiliary board FU 1A parity error
13	Auxiliary board FU 2A parity error
14	Auxiliary board FU 2B parity error
15	Auxiliary board FU 3A parity error
16	(Not used)
17	Data result register parity error, byte 0
18	Data result register parity error, byte 1
19	Data result register parity error, byte 2
20	Data result register parity error, byte 3
21	Data result register parity error, byte 4
22	Data result register parity error, byte 5
23	Data result register parity error, byte 6
24	(Not used)
25	(Not used)
26	Port A response code bit 0
27	Port A response code bit 1
28	Port B response code bit 0
29	Port B response code bit 1
30	Port C response code bit 0
31	Port C response code bit 1

PROC-990 PFSD REGISTER (8D)



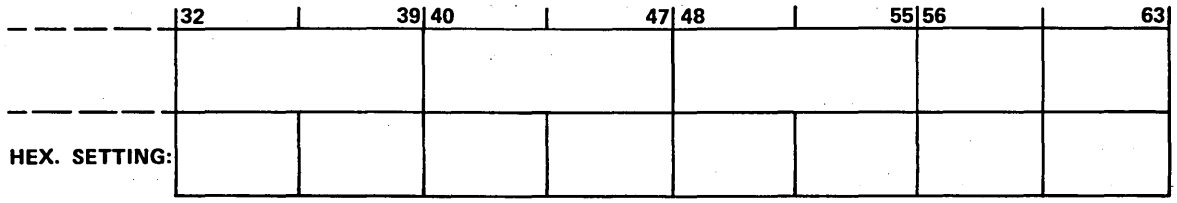
Bit	Description
32	(Not used)
33	(Not used)
34	(Not used)
35	(Not used)
36	(Not used)
37	(Not used)
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	Register 22 parity error, byte 2
43	Register 22 parity error, byte 3
44	Register 22 parity error, byte 8
45	Register 22 parity error, byte 9
46	Register 22 parity error, byte 10
47	Register 22 parity error, byte 11
48	Register 22 parity error, byte 12
49	Register 22 parity error, byte 13
50	Register 22 parity error, byte 14
51	Register 22 parity error, byte 15
52	Buffer input latch number 1 parity error, byte 4
53	Buffer input latch number 1 parity error, byte 5
54	Buffer input latch number 1 parity error, byte 6
55	Buffer input latch number 1 parity error, byte 7
56	Buffer input latch number 2 parity error, byte 1
57	Buffer input latch number 2 parity error, byte 2
58	Buffer input latch number 2 parity error, byte 3
59	Buffer input latch number 2 parity error, byte 4
60	Buffer input latch number 2 parity error, byte 5
61	Buffer input latch number 2 parity error, byte 6
62	Buffer input latch number 2 parity error, byte 7
63	MAC read data parity error

PROC-990 PFSE REGISTER (8E)



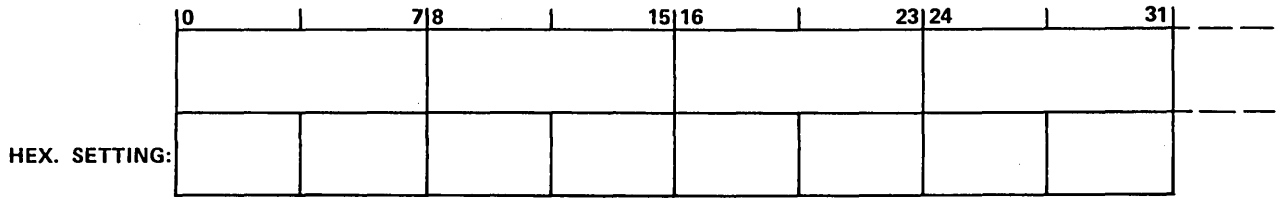
Bit	Description
00	180 map output register parity error, byte 0
01	180 map output register parity error, byte 1
02	180 map output register parity error, byte 2
03	180 map output register parity error, byte 3
04	180 map output register parity error, byte 4
05	180 map output register parity error, byte 5
06	170 map output register parity error, byte 6
07	170 map output register parity error, byte 7
08	Map instruction register parity error, byte 0
09	Map instruction register parity error, byte 1
10	Map instruction register parity error, byte 2
11	Map instruction register parity error, byte 3
12	Map address register parity error, byte 0
13	Map address register parity error, byte 1
14	Map address register parity error, byte 2
15	Map address register parity error, byte 3
16	IBA1 register parity error, byte 0
17	IBA1 register parity error, byte 1
18	IBA1 register parity error, byte 2
19	IBA1 register parity error, byte 3
20	SVA register parity error, byte 0
21	SVA register parity error, byte 1
22	SVA register parity error, byte 2
23	SVA register parity error, byte 3
24	RMA register parity error, byte 0
25	RMA register parity error, byte 1
26	Destination tag register parity error, byte 0
27	Destination tag register parity error, byte 1
28	CMC response counter error, set 0
29	CMC response counter error, set 1
30	CMC response counter error, set 2
31	CMC response counter error, set 3

PROC-990 PFSE REGISTER (8E)



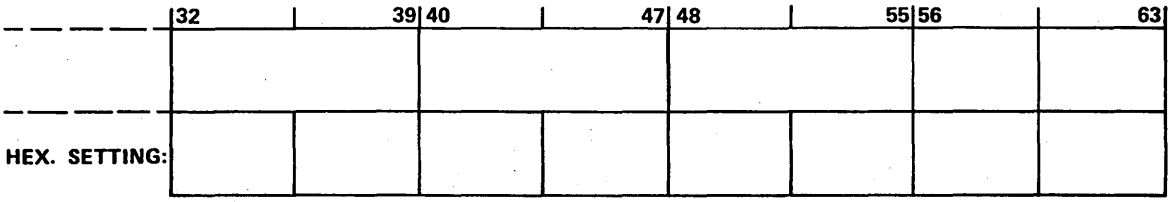
Bit	Description
32	CMC destination code register parity error
33	PFSA register parity error, byte 0
34	PFSA register parity error, byte 1
35	PFSA register parity error, byte 2
36	IBS error, set 0
37	IBS error, set 1
38	IBS error, set 2
39	IBS error, set 3
40	Lookahead multiple hit
41	IBS read multiple hit
42	(Not used)
43	(Not used)
44	(Not used)
45	(Not used)
46	(Not used)
47	(Not used)
48	(Not used)
49	(Not used)
50	(Not used)
51	(Not used)
52	(Not used)
53	(Not used)
54	(Not used)
55	(Not used)
56	(Not used)
57	IN2 error tag parity error
58	PSR error tag parity error
59	ACU error tag parity error
60	Soft control memory parity error, byte 0
61	Soft control memory parity error, byte 1
62	Soft control memory parity error, byte 2
63	Soft control invalid access

PROC-990 PFSF REGISTER (8F)



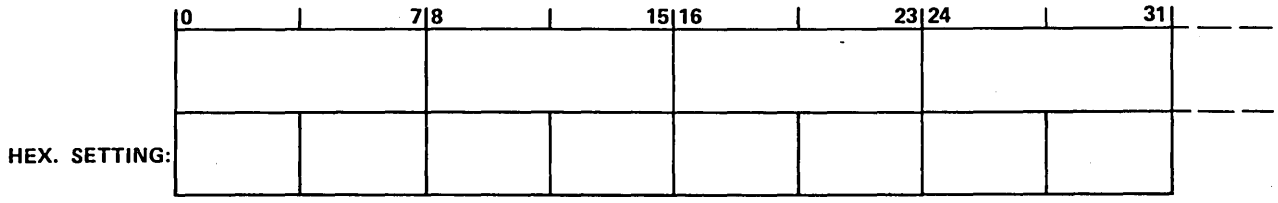
Bit	Description
00	Data memory parity error, set 0
01	Data memory parity error, set 1
02	Data memory parity error, set 2
03	Data memory parity error, set 3
04	Tag memory parity error, set 0
05	Tag memory parity error, set 1
06	Tag memory parity error, set 2
07	Tag memory parity error, set 3
08	Tag address parity error, set 0
09	Tag address parity error, set 1
10	Tag address parity error, set 2
11	Tag address parity error, set 3
12	State address parity error, set 0
13	State address parity error, set 1
14	State address parity error, set 2
15	State address parity error, set 3
16	Data memory parity error, byte/board 0
17	Data memory parity error, byte/board 1
18	Data memory parity error, byte/board 2
19	Data memory parity error, byte/board 3
20	Data memory parity error, byte/board 4
21	Data memory parity error, byte/board 5
22	Data memory parity error, byte/board 6
23	Data memory parity error, byte/board 7
24	Data/tag mux to MAC parity error
25	Multiple tag hit
26	Set allocation error
27	(Not used)
28	CI address or SVAPTC parity error, byte 0
29	CI address or SVAPTC parity error, byte 1
30	CI address or SVAPTC parity error, byte 2
31	CI address or SVAPTC parity error, byte 3

PROC-990 PFSF REGISTER (8F)



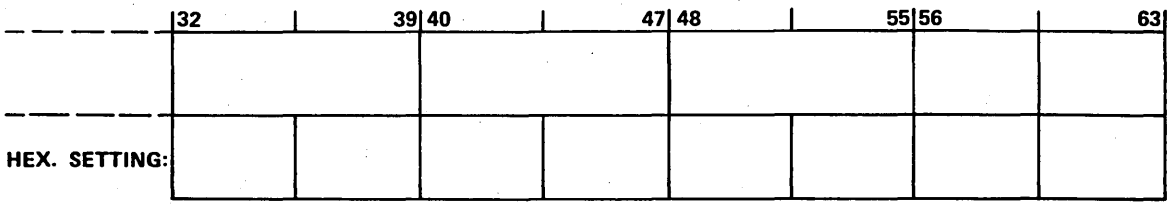
Bit	Description
32	CI address or SVAPTC parity error, byte 4
33	CI address or SVAPTC parity error, byte 5
34	Input SVA parity error, byte 0
35	Input SVA parity error, byte 1
36	Input SVA parity error, byte 2
37	Input SVA parity error, byte 3
38	Input SVA parity error, byte 4
39	Input SVA parity error, byte 5
40	Register 2 SVA parity error, byte 0
41	Register 2 SVA parity error, byte 1
42	Register 2 SVA parity error, byte 2
43	Register 2 SVA parity error, byte 3
44	Register 2 SVA parity error, byte 4
45	Register 2 SVA parity error, byte 5
46	Register 2 second rank SVA parity error, byte 0
47	Register 2 second rank SVA parity error, byte 1
48	Register 2 second rank SVA parity error, byte 2
49	Register 2 second rank SVA parity error, byte 3
50	Register 2 second rank SVA parity error, byte 4
51	Register 2 second rank SVA parity error, byte 5
52	Prefetch SVA parity error, byte 0
53	Prefetch SVA parity error, byte 1
54	Prefetch SVA parity error, byte 2
55	Prefetch SVA parity error, byte 3
56	Prefetch SVA parity error, byte 4
57	Cache load register 2 parity error
58	Cache load address parity error, byte 0
59	Cache load address parity error, byte 1
60	Cache load address parity error, byte 2
61	Cache load address parity error, byte 3
62	Cache load address parity error, byte 4
63	Cache load address parity error, byte 5

PROC-990 PTM REGISTER (A0)



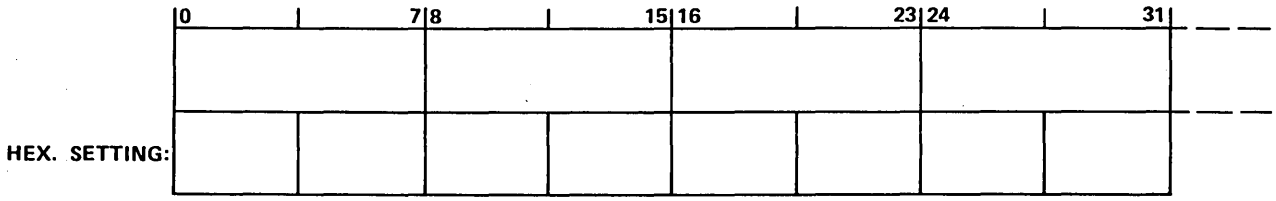
Bit	Description
00	Force parity error on MAC CIR read, byte 0
01	Force parity error on MAC CIR read, byte 1
02	Force parity error on MAC CIR read, byte 2
03	Force parity error on MAC CIR read, byte 3
04	Force parity error on MAC CIR read, byte 4
05	Force parity error on MAC CIR read, byte 5
06	Force parity error on MAC CIR read, byte 6
07	Force parity error on MAC CIR read, byte 7
08	Force parity error on XFER CNT to AC1
09	Force parity error on LSM IC2 to LSU
10	(Not used)
11	Force parity error on byte 0 to ACUMIC to AC1
12	Force parity error on byte 1 to ACUMIC to AC1
13	Force parity error on byte 2 to ACUMIC to AC1
14	Force parity error on byte 3 to ACUMIC to AC1
15	Force parity error on byte 4 to ACUMIC to AC1
16	Force control store sequencing error
17	Force parity error on byte 0 of CIC RDT to IN2
18	Force parity error on byte 1 of CIC RDT to IN2
19	Force parity error on LSMIC 4 to LSU
20	Force parity error on LSMIC 7 to LSU
21	Force parity error on byte 0 of IWSCRP to AC1
22	Force parity error on byte 1 of IWSCRP to AC1
23	Force parity error on byte 2 of IWSCRP to AC1
24	Force parity error on byte 0 of BDPMIC to BDP
25	Force parity error on byte 1 of BDPMIC to BDP
26	Force parity error on byte 0 of LSMIC1 to LSU
27	Force parity error on byte 1 of LSMIC1 to LSU
28	Force parity error on byte 2 of LSMIC1 to LSU
29	Force parity error on byte 0 of LSMIC5 to LSU
30	Force parity error on byte 1 of LSMIC5 to LSU
31	Force parity error on byte 2 of LSMIC5 to LSU

PROC-990 PTM REGISTER (A0)



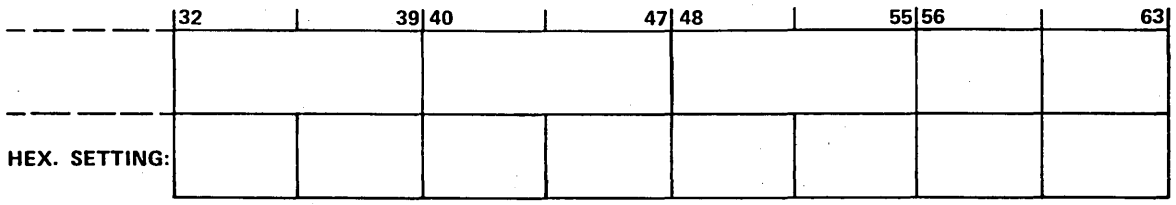
Bit	Description
32	(Not used)
33	(Not used)
34	(Not used)
35	(Not used)
36	(Not used)
37	(Not used)
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	(Not used)
43	(Not used)
44	(Not used)
45	(Not used)
46	(Not used)
47	(Not used)
48	Force auxiliary board 0 chip clock error
49	Force auxiliary board 1 chip clock error
50	Force auxiliary board 2 chip clock error
51	Force auxiliary board 3 chip clock error
52	Force auxiliary board 4 chip clock error
53	Force auxiliary board 5 chip clock error
54	Force auxiliary board 6 chip clock error
55	Force auxiliary board 7 chip clock error
56	PTM bit, control store branch, wait
57	(Not used)
58	(Not used)
59	(Not used)
60	(Not used)
61	Enable MAC write of P register
62	(Not used)
63	Force parity error on LSMIC6 to LSU

PROC-990 PTM REGISTER (A1)



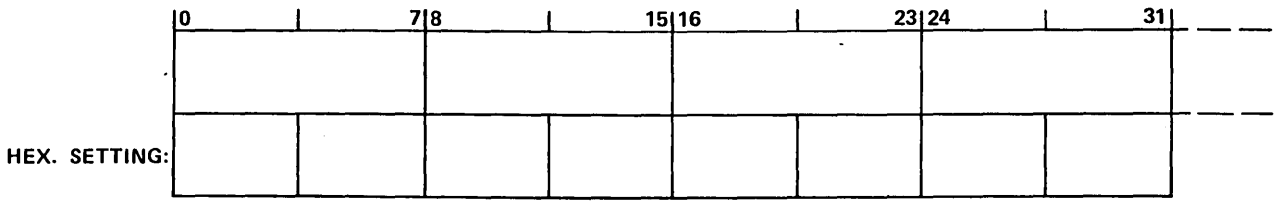
Bit	Description
00	(Not used)
01	(Not used)
02	(Not used)
03	(Not used)
04	Force zero parity on IOU data
05	Force parity error on MAC copy data to IOU
06	(Not used)
07	(Not used)
08	Force parity error on length mux/register
09	Force parity error on byte number adder
10	Force parity error on interval register
11	Force parity error on LSU micrand (0 through 15, 24 through 31)
12	Force parity error on valid holding register
13	Force parity error on X data to P register (0 through 15)
14	Force parity error on SFSA global/local key register
15	(Not used)
16	(Not used)
17	(Not used)
18	Force parity error on length to adder operand B
19	Fill buffers 1 and 2
20	Fill buffers 3 and 4
21	Force upper bit of execute PROM when in RMA mode
22	Force upper bit of execute PROM when in RMA mode
23	Force slow unit delay
24	Set issue timer bit 5 to 0
25	Set issue timer bit 6 to 0
26	Set issue timer bit 7 to 0
27	Enable short stop counters
28	Force parity error on rank 2 ring and segment
29	(Not used)
30	Force parity error on error register
31	Force parity error on LRNSF register

PROC-990 PTM REGISTER (A1)



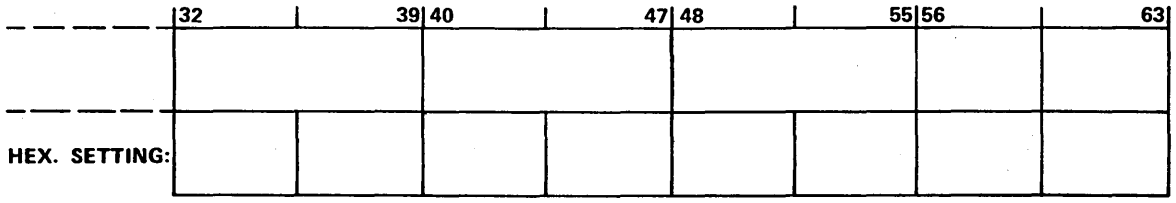
Bit	Description
32	Force parity error on page index/search RMA
33	(Not used)
34	(Not used)
35	Force parity error on page offset-upper
36	(Not used)
37	Force zero parity on port B miss tag
38	Force parity error on CMC function
39	Force parity error on page RMA
40	(Not used)
41	Force backup
42	Force parity error on port A tag
43	Force parity error on rank 4 masked SVA
44	Force parity error on data result
45	Force parity error on M4 loop
46	Force parity error on MAC address
47	Force parity error on store tag
48	Force divide compare error, byte 0
49	Force divide compare error, byte 1
50	Force divide compare error, byte 2
51	Force divide compare error, byte 3
52	Force divide compare error, byte 4
53	Force divide compare error, byte 5
54	Force divide compare error, byte 6
55	Force divide compare error, byte 7
56	Force FPM holding register to 0
57	(Not used)
58	(Not used)
59	Select IMU compare counter
60	Clear IMU compare counter
61	Disable IMU compare
62	Force error in IMU compare
63	Force parity error in IMU BDP byte

PROC-990 PTM REGISTER (A2)



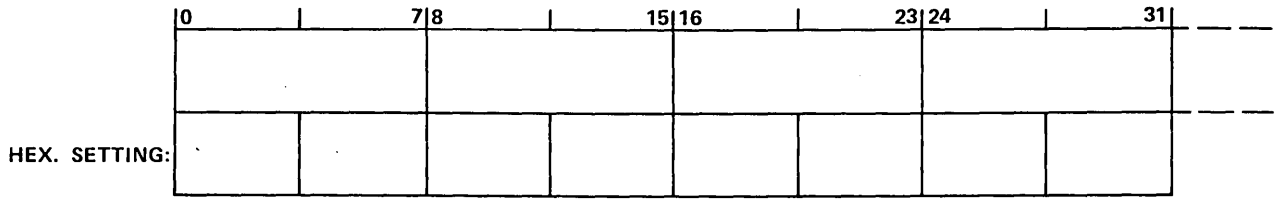
Bit	Description
00	Force parity error on address byte 4, port 0A
01	Force parity error on address byte 4, port 0B
02	Force parity error on address byte 4, port 0C
03	Force parity error on address byte 4, port 1
04	Force parity error on address byte 4, port 2A
05	Force parity error on address byte 4, port 2B
06	Force parity error on address byte 4, port 2C
07	Force parity error on address byte 4, port 3
08	Force parity error on address byte 5, port 0A
09	Force parity error on address byte 5, port 0B
10	Force parity error on address byte 5, port 0C
11	Force parity error on address byte 5, port 1
12	Force parity error on address byte 5, port 2A
13	Force parity error on address byte 5, port 2B
14	Force parity error on address byte 5, port 2C
15	Force parity error on address byte 5, port 3
16	Force parity error on address byte 7, port 0A
17	Force parity error on address byte 7, port 0B
18	Force parity error on address byte 7, port 0C
19	Force parity error on address byte 7, port 1
20	Force parity error on address byte 7, port 2A
21	Force parity error on address byte 7, port 2B
22	Force parity error on address byte 7, port 2C
23	Force parity error on address byte 7, port 3
24	Force destination tag parity error
25	(Not used)
26	(Not used)
27	(Not used)
28	Force short warning
29	Force long warning
30	Force parity error on MAC read data
31	Force parity error on CMC response code

PROC-990 PTM REGISTER (A2)



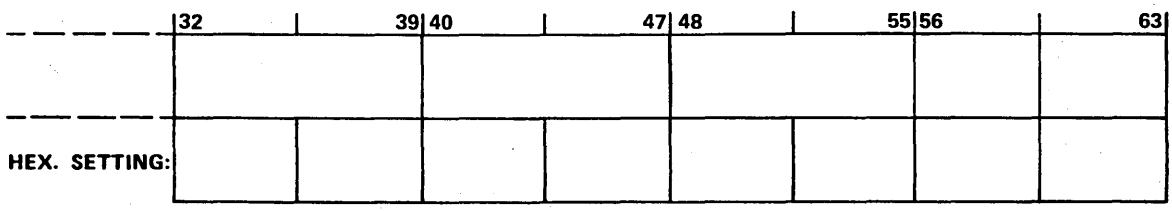
Bit	Description
32	(Not used)
33	Force response code parity error
34	Force IBS lookahead multiple hit
35	Force IBS read multiple error
36	Force parity error on RMA register bytes 3 and 4
37	Force parity error on IBS input data (C170 mode)
38	Force parity error on IBA0 register
39	Force parity error on destination tag signal to ACU
40	Force parity error on mark lines
41	(Not used)
42	Force parity error on read state input micrand
43	Force parity error on write state input micrand
44	Force parity error on ACU ring number
45	Force parity error on P ring number
46	Force parity error on C170 exchange mux
47	Force parity error on data bits 40 through 63
48	Force parity error on X data
49	Force parity error on move bytes micrand
50	Force parity error on byte 0 of destination tag to IN1
51	Force parity error on byte 1 of destination tag to IN1
52	Force parity error on store data mux/latch 2
53	(Not used)
54	(Not used)
55	(Not used)
56	(Not used)
57	(Not used)
58	(Not used)
59	Force parity error on SVA bits 48 through 50 to tag memory
60	Force parity error on tag address bits 51 through 60
61	Disable cache hit
62	Force parity error on MAC address OCA
63	Force parity error on bits 16 through 23 TAGDAT

PROC-990 PTM REGISTER (A3)



Bit	Description
00	Force parity error on error-enable table
01	Conditional branch and repeat
02	Force error bit 5 of SCU errors
03	Force error bit 9 of IGU errors
04	Force error bit 8 of FPU errors
05	Force parity error on error tag
06	Clear entry to first micrand and delay store flip-flops
07	Master-set fatal P and P+ FFs
08	Force parity error on MPS register
09	Force parity error on SIT register
10	Force parity error on VMID register
11	Force parity error on MAC load MICRAND
12	Force parity error on STA register
13	Force parity error on PIT register
14	Force parity error on PTA bit 63
15	Force parity error on UVMID
16	Force parity error on trap enable
17	Force parity error on debug mask
18	Force parity error on page size mask to ACU
19	Force parity error on debug index byte 0
20	Force parity error on user condition register
21	Force parity error on bytes 0 and 1 of SFSA word 2
22	Force parity error on Virtual State exchange package flags
23	Force parity error on keypoint class number
24	Force parity error on load-errors data
25	Force parity error on monitor condition register
26	Enables VMID loaded at MC
27	Force parity error on BH12 of STLNTH
28	Force parity error on byte 0 of buffer input latch 1
29	Force parity error on byte 1 of buffer input latch 1
30	Force parity error on byte 2 of buffer input latch 1
31	Force parity error on byte 3 of buffer input latch 1

PROC-990 PTM REGISTER (A3)



Bit	Description
32	Force parity error on byte 0 of buffer input latch 2
33	Force parity error on byte 1 of buffer input latch 2
34	Master-set upper half of error flip-flops
35	Master-set lower half of error flip-flops
36	(Not used)
37	(Not used)
38	(Not used)
39	(Not used)
40	(Not used)
41	(Not used)
42	(Not used)
43	Force pause on Aj stream
44	Force pause on Ak stream
45	Force parity error on store mark lines
46	Force parity error on LSU load micrand
47	Force parity error on error tag
48	Force parity error on length counter subtrahends
49	Force parity error on move bytes mark line
50	Force parity error on LSU store micrand
51	Force parity error on BDP/BP3 MAC address
52	(Not used)
53	Force zero parity on X-data HF input
54	Force zero parity on A-data HF input
55	Force zero parity on byte of HF output
56	(Not used)
57	(Not used)
58	(Not used)
59	Force parity error on A-port stage 2 data
60	Force parity error on B-port stage 2 data
61	Force edit mask to all ones
62	Force parity error on specification error ROM address
63	Force output stage 3 data to zero, parity = 1

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