
**CONTROL DATA®
1700 SYSTEM
MAINTENANCE MONITOR (SMM17)**

**VOLUME 2
REFERENCE MANUAL**

RECORD of REVISIONS

REVISION	NOTES
01 (5-13-66)	Original Printing, preliminary edition.
02 (8-8-66)	Publications Change Order 14307. Reprint with revision which obsoletes all previous editions. Tests were updated and the following new tests were added: 1711/1712 Teletype, 1729 Card Reader, 1731 Magnetic Tape, 1706/1716 Buffered Data Channel and Coupling, Random Protect, 1700 SMM Edit Routine, and Enter Program.
A (5-1-67)	Manual released. Publication Change Order 16368. The following new tests are added: 0B (1718 Satellite Coupler Test), 0C (1742 Line Printer Test), and 3D (Enter Program). Other tests were extensively revised and updated. This edition obsoletes all previous editions.
B (9-14-67)	Publication Change Order 17146. To revise existing tests and add new tests. Introduction: page 5 revised. Description: pages 7, 12, 15, 18, 25, 26, 27, 30 and 35 revised. Pages 30-a and 30-b added. Tests: pages 90-1, 90-2, 100-7, 100-8, 100-10, 101-2, 101-7, 202-1, 202-7, 205-2, 206-6 thru 206-10, 207-3, 208-2 and 208-6 revised. Page 100-8a added. Tests sections: 102, 201, 203, 212, 213 and 214 added. Sections 102 Rev A, 201 Rev A and 203 Rev A removed.
C (2-28-68)	Publications Change Order 18929. To add 1728 Card Reader/Punch test, No. D.
D (6-11-68)	Publications Change Order 19818, to make miscellaneous publication corrections. Pages 37, 100-2, 100-18, 101-9, 102-7, 200-10, 201-6, 202-9, 203-7, 204-1, 204-12, 205-14, 206-9, 206-10, 207-4, 208-21, 210-4, 210-6, 211-13, and 215-23 revised. Pages 207-5 and 212-24 added.
E (1-6-69)	Manual Revised, Engineering Change Order 21307, publications change only. Information included through Edition 2.1. Pages 35, 90-1, 90-2, 90-6, 101-10, and 208-1 thru 208-21 revised; pages 30-c through 30-f, 51 through 60, 103, 216, 217, 218, 219, 220, 221, 222 and red tab dividers added. Manual divided into two volumes.
F (12-15-69)	Manual revised, Engineering Change Order 21883. This manual is complete through Edition 2.3.
G (2-15-70)	Manual revised. New tests are added and editorial corrections made. This manual is complete through Edition 2.2.
H (12-15-70)	Manuals revised. This publication is complete through Ed. 2.3. All previous editions are obsolete.
J (2-5-73)	Manuals revised. New tests are added and minor corrections are made. This publication is complete through Ed. 3.0.
K (9-20-73)	Manuals revised. Tests are added, deleted, and corrected.
L (2-1-74)	Manuals revised. Tests are added, deleted, and corrected. This publication is complete through Edition 3.1.

FORM CA230 REV. 1-67

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PREFACE

MANUAL STRUCTURE

This manual is intended to serve as a reference aid for field and checkout personnel involved in the running of the CONTROL DATA® 1700 System Maintenance Monitor (SMM17). It consists of two sections:

SMM17 DESCRIPTION

A detailed description of the operation and use of the monitor, instructions for the operator, restrictions and necessary parameters. An asterisk (*) on the left of the page will highlight operator tasks. Supplements are included in the back of this section.

TESTS

Detailed test descriptions complete the three volume reference manual.

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1706 BUFFERED DATA CHANNEL TEST

(BD100A Test No. 0A)

OPERATIONAL PROCEDURE

A. RESTRICTIONS

Sections 3, 4, and 5 do not select density on the MT units. However, it is recommended that 200 BPI be selected to allow greater accuracy in testing the CWA register.

B. LOADING PROCEDURE

1. The test operates under control of 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17.
3. The test can be restarted after loading from Initial address.

C. PARAMETERS

1. If bit 0 of the Stop/Jump word is set, the program will have one monitor stop displaying \$A31 in the A register and the Stop/Jump word in the Q register. Two additional stops with the test parameters displayed in the A and Q registers are defined as follows:

- Stop 2 A = WE01, where the W field is bits 15-11 and defines the BDC to be tested. Enter 2, 7, or C for the BDC numbers 1, 2, or 3 respectively. The E field is bits 10-7 and specifies the equipment number of the 1731/1732 Magnetic Tape Controller.
- Q = 000U, where U specifies the 601/608/609 Tape Unit which will be used for I/O.
- Stop 3 A = XXXX, the End of Operation interrupt line for the BDC. Only 1 bit is set in this word which must indicate the interrupt line. For example if the End of Operation interrupts are to be received on line 5, Bit 5 would be set.
- Q = XXXX, the sections of the BDC test to run. Bit 0 of Q will select Section 1 to be run, etc. There are five sections in all. If all five sections were to be run, Q would be set to 001F.
- Stop 4 A = XXXX, illegal equipment (enter into A an equipment address that is unused on your system. This equipment address is used to check internal rejects)
- Q = XXXX, unused (prestored as 0001)

2. If bit 0 of the Stop/Jump word is not set, the test will be run using the prestored parameters. These parameters assume the following:
 - a. BDC number 1 is to be tested and the tape controller is number 3.
(WE01 = 1181)
 - b. Tape unit 7 is the tape to use for I/O.
 - c. The interrupts on End of Operation from the BDC are received on line 3.
 - d. All five sections of the test will be run.
3. A timeout of selected parameters will occur after last stop.

D. SELECTIVE SKIP AND STOP SETTINGS

1. STOP - must be set for running of SMM17.
2. SKIP - when the Stop/Jump word is displayed in Q.

E. MESSAGES

1. Timeouts or Alarms

a. Normal Program Timeouts

- 1) Test identification at start of test
BD100A, 1706 BUFFERED DATA CHANNEL TEST IA = XXXX, FC = XX
- 2) End of test timeout

A	Q	A	Q
0A24	S/J	Pass No.	Return Address

b. Error Alarms

- 1) The following is typed out:
 - a) Identification word
 - b) Stop/Jump parameter
 - c) Section/Error number
 - d) Return address
 - e) Information dependent upon specific error
 - f) Information dependent upon specific error

2. Error Codes

An error code is displayed in the lower two digits of the A register on the second stop of all error stop sequences. A description of the error codes used and the data displayed in the A and Q registers of the third stop is listed as follows:

- Error 01 - Incorrect equipment parameter was entered. Program will make another parameter stop if placed in Run.
A = the equipment parameter entered
Q = 0000
- Error 02 - External reject on input of BDC status. If the error condition is not repeated (Bit 4 of Stop/Jump word set) the test will be terminated.
A = the contents of Q when the input instruction was executed
Q = 0000
- Error 03 - Internal reject on input of BDC status. If the error condition is not repeated, the test is terminated.
- Error 04 - Ready not set on BDC status. If the condition is not repeated, the test is terminated.
A = BDC status
Q = 0000
- Error 05 - External reject on input of BDC current address.
A = contents of Q when the input instruction was executed
Q = 0000
- Error 06 - Internal reject on input of BDC current address.
A = contents of Q when the input instruction was executed
Q = 0000
- Error 07 = External reject on Terminate Buffer.
A = contents of Q when the input instruction was executed
Q = 0000
- Error 08 = Internal reject on Terminate Buffer.
A = contents of Q when the input instruction was executed
Q = 0000
- Error 09 = External reject on attempt to output a function to the BDC.
A = contents of Q when output was attempted
Q = contents of A when output was attempted

- Error 0A - Internal reject on attempt to output a function to the BDC.
A = contents of Q when output was attempted
Q = contents of A when output was attempted
- Error 0B - External reject on direct output of a function to the 1731 Tape Controller.
A = contents of A when output was executed
Q = contents of Q when output was executed
- Error 0C - Internal reject on direct output of a function to the 1731 Tape Controller.
A = contents of A when output was executed
Q = contents of Q when output was executed
- Error 0D - External reject on input of status 1 of the 1731 Tape Controller.
A = the contents of Q when the input was executed
Q = 0000
- Error 0E - Internal reject on input of status 1 of the 1731 Tape Controller.
A = the contents of Q when the input was executed
Q = 0000
- Error 0F - External reject on input of status 2 of the 1731 Tape Controller.
A = the contents of Q when the input was executed
Q = 0000
- Error 10 - Internal reject on input of status 2 of the 1731 Tape Controller.
A = the contents of Q when the input was executed
Q = 0000
- Error 11 - No write ring in selected tape unit. If this error condition is not repeated, the test is terminated.
A = the selected tape unit
Q = status 2 of the selected tape unit
- Error 12 - The selected tape unit is protected. If this error condition is not repeated, the test will be terminated.
A = the selected tape unit
Q = status 1 of the selected tape unit

- Error 13 - External reject on attempt to initiate buffered output to tape.
A = the first word address minus 1 of the buffer area
Q = contents of Q when the output instruction was executed
- Error 14 - Internal reject on attempt to initiate buffered output to tape.
A = the first word address minus 1 of the buffer area
Q = contents of Q when the output instruction was executed
- Error 15 - External reject on the attempt to initiate a buffered input from tape.
A = the first word address minus 1 of the buffer area
Q = the contents of Q when the output instruction was executed
- Error 16 - Internal reject on the attempt to initiate a buffered input from tape.
A = the first word address minus one of the buffer area
Q = the contents of Q when the output instruction was executed
- Error 17 - Busy bit (bit 1) of the BDC status was not set after initiating a buffered output.
A = BDC status
Q = 0000
- Error 18 - Busy bit (bit 1) of the BDC status was not set after initiating a buffered input.
A = BDC status
Q = 0000
- Error 19 - Reply bit (bit 9) of the BDC status was not set after initiating a buffered output.
A = BDC status
Q = 0000
- Error 20 - Reply bit (bit 9) of the BDC status was not set after initiating a buffered input.
A = BDC status
Q = 0000
- Error 21 - Reject bit (bit 8) of the BDC status was never set (over an arbitrary length of time) after initiating a buffered output.
A = BDC status
Q = 0000

- Error 22 - Reject bit (bit 8) of the BDC status was never set (over an arbitrary length of time) after initiating a buffered input.
A = BDC status
Q = 0000
- Error 23 - End of Operation bit (bit 4) of the BDC status is set at the same time as the Busy bit.
A = BDC status
Q = 0000
- Error 24 - End of Operation bit (bit 4) of the BDC status is not set after the Busy cleared at the end of a buffered output.
A = BDC status
Q = 0000
- Error 25 - End of Operation bit (bit 4) of the BDC status is not set after the Busy cleared at the end of a buffered input.
A = BDC status
Q = 0000
- Error 26 - No reject received from the BDC when attempting a direct output when the BDC was Busy.
A = BDC status
Q = 0000
- Error 27 - No interrupt received from the BDC on End of Operation (buffered output).
A = BDC status
Q = 0000
- Error 28 - Alarm bit set in tape status 1 after a buffered output was complete.
A = Tape status 1
Q = 0000
- Error 29 - No interrupt received from the BDC on End of Operation (buffered input).
A = BDC status
Q = 0000

Error 2A - Interrupt bit (bit 2) of the BDC status was not set after an End of Operation interrupt occurred.

A = BDC status when interrupted

Q = 0000

Error 2B - Data error

A = Data read

Q = Expected value

A = Failing address

Q = 0000

Error 2C - Current address of the BDC was not equal to one greater than the FWA-1 after initiating a buffered output.

A = Current address which was input

Q = 0000

Error 2D - The current address which was input from the BDC was neither the same as or up to two greater than the previous current address input.

A = Previous current address

Q = Current address

Error 2E - End of Operation status bit (bit 4) was not set in the BDC status when an Interrupt on End of Operation occurred.

A = BDC status

Q = 0000

Error 2F - Buffer terminated at incorrect address.

A3 = Actual address buffer terminated at

Q3 = Expected last word address, at EOP

Error 33 - Incorrect status after initiating buffer to non-existent equipment (parameter A4) on this 17X6.

A3 = Expected channel status after initiating a buffer

Q3 = Actual channel status after initiating a buffer

A4 = Expected address register status

Q4 = Actual address register status

A5 = Equipment address when error occurred

Q5 = Iteration count (range = FFFC-0003)

Error 34 - Current word address was not one greater than FWA-1 after initiating a buffer to illegal equipment on BDC.

A3 = Expected channel status

Q3 = Actual channel status

A4 = FWA-1 output to BDC to initiate buffer

Q4 = CWA of BDC on terminate buffer command

A5 = Same as error 33

Q5

Error 35 - Internal reject on clear controlled direct through BDC

A3 = BDC expected status

Q3 = BDC actual status

A4 = Equipment expected status

Q4 = Equipment actual status

A5 = Equipment address when error detected

Q5 = Not available

Error 36 - External reject on clear controller

Same as error 35

Error 37 - Channel busy or not ready

A3 = 0

Q3 = BDC actual status

A4 = 0

Q4 = 0

A5 = Same as error 33

Q5

Error 38 - Unit/Equipment busy

A3 = 0

Q3 = BDC actual status

A4 = 0

Q4 = Unit status

A5 = Same as error 33

Q5 = Same as error 33

Error 39 - Buffer terminated before programmed LWA+1

A3 = Not available

Q3 = BDC status

A4 = Actual CWA status at EOP

Q4 = Expected CWA status at EOP

A5 = Same as error 33

Q5

Error 3A - Buffer did not terminate at last word ADDES+1

A3 = Not available

Q3 = BDC status

A4 = Current word address when buffer was terminated

Q4 = Expected LWA register

Error 3C - 17X6 not busy before CWA=LWA+1

A3 = Expected BDC status

Q3 = Actual BDC status

A4 = CWA register status

Q4 = LWA+1 sent to BDC

A5 = Same as error 33

Q5

Error 3D - 17X6 buffer hung before CWA=LWA+1 when doing buffered equipment status inputs or buffered clear controller outputs.

A3 = Expected status of BDC

Q3 = Actual status of BDC

A4 = CWA register status of hung buffer

Q4 = Expected LWA+1 of buffer

A5 = Same as error 33

Q5 = Same as error 33

3. Error Stops

Error stops will occur if bit 3 of the Stop/Jump word is set and an error occurs in the test.

II. DESCRIPTION

A. INITIALIZATION (UNIT)

1. Convert bias value and frequency count to ASCII and store in typeout routine.
2. Type out test title, initial address, and frequency count.

3. Set up return address (IA+5).
4. Parameter entry stop.
5. Check for correct W field in equipment code. Error stop if incorrect.
7. Exit to SMM.

B. SECTION ONE (S1)

This section checks static conditions of BDC then proceeds to check the CWA register, LWA register, adder, buffer read capabilities, and buffer write capabilities.

1. Check status for ready.
2. Input current address; no Reject expected.
3. Execute terminate buffer and input current address to
 - a. No Reject expected.
4. Check EOP interrupt select and clear.
5. Attempt buffer output to non-existent equipment on channel.
 - a. Start with FWA-1=0. Expect BDC to hang with CWA one greater than FWA-1. Expect status to be busy.
 - b. Do until FWA-1 = \$7FFF.
 - c. Do a and b three times
6. Attempt buffer input from non-existent equipment on channel (same as 5).
7. Do direct FCN clear controller to selected Equipment Expect Reply.
8. Do 500₁₀ word buffer out of clear controller.
 - a. Monitor CWA. Expect termination when CWA=LWA+1.
 - b. Monitor BDC status. Expect busy until CWA=LWA+1.
 - c. Do 100₁₀ times.
9. Do direct input status 1 of selected equipments. Save for use in next step. Expect reply.
10. Do 500₁₀ word buffer input of status 1 from selected device.
 - a. Same as 8a and 8b.
 - b. Compare data from step 9 and report errors.
 - c. Do 100₁₀ times.

C. SECTION TWO (S2)

This section checks static conditions on the BDC, tape controller, and tape unit.

1. Connect selected tape unit.
2. Check for write enable. Error if not present.
3. Check for tape unit unprotected. Error if protected.
4. Rewind tape.
5. Exit section two.

D. SECTION THREE (S3)

This section does a 500-word buffered Write and Read.

1. Request interrupt line from SMM.
2. Select tape unit and rewind it.
3. Select binary mode.
4. Initiate a 500-word buffered write.
5. Check BDC status for Busy. Repeat from item 2 if Not Busy.
6. Check BDC status for Reply. Should be set.
7. Check BDC status for Reject during output. Should be set.
8. Exit to SMM until buffer is complete.

9. Rewind tape.
10. Repeat from item 4 for a 500-word read.
11. Clear interrupt request in SMM.
12. Exit section three.

E. SECTION FOUR (S4)

This section writes and reads ten 500-word records for each of fifteen patterns. End of Operation interrupt is checked after each record.

1. Request interrupt line from SMM.
2. Select tape.
3. Pick up current data pattern.

4. Select binary mode if pattern number is Odd. Select BCD mode if pattern number is Even.
5. Clear interrupt flag.
6. Select EOP interrupt on BDC.
7. Initiate 500-word buffered write.
8. Check for reject during buffered operation.
9. Exit to SMM until buffer is complete.
10. Check for EOP interrupt. Error if not present.
11. Check tape status for EOT, Parity, Lost Data, and Alarm.
12. Repeat from item 5 for 10 records.
13. Update data pattern.
14. Repeat from item 2 for 15 patterns.
15. Rewind tape.
16. Blank out storage data.
17. Repeat from item 5 using a Read instead of a Write. Data is checked for each record.
18. Exit section four.

F. SECTION FIVE (S5)

This section tests the current word address.

1. Request interrupt line from SMM.
2. Rewind tape, select binary mode.
3. Initiate buffered output. Word Count = $7FFE_{16}$ -LOCSEX.
4. Input current address to A. Address should be one greater than the CWA.
5. Store current address.
6. Input current address to A. This address should be equal to or up to two greater than previous address. Error if not one of these two conditions.
7. If current address is one greater than previous address, repeat from item 4.
8. If current address equals previous address, check BDC status for EOP. Loop to item 4 if not set.
9. Check tape status for EOT, Parity, Lost Data, and Alarm. Error if any of these are set.
10. Clear interrupt request.
11. Exit section five.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIRED

Approximately 2000 locations.

B. INPUT AND OUTPUT TAPE MOUNTINGS

The 601/608/609 Tape Unit selected for I/O must have a write ring and must be ready.

C. TIMING - approximately 1 minute 15 seconds.

D. EQUIPMENT CONFIGURATION

1. 17X4 Computer
2. 17X5 Interrupt Data Channel
3. 1706 Buffer Data Channel
4. 1731/1732 Magnetic Tape Controller
5. 601/608/609 Magnetic Tape Unit

1706/1716 CHANNEL TEST

(BD200F Test No. 0F)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

None available

B. LOADING PROCEDURE

1. The test operates under control of 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17. The test number for the 1706/1716 test is F.
3. The test can be restarted after loading from initial address.

C. PARAMETERS

1. If bit 0 of the Stop/Jump word is set, the program will allow for test parameter display and/or entry. The first stop made in the parameter sequence displays the identification word in A (0F31) and the Stop/Jump word in Q.

The second and third stops display the test parameters. The test parameters can be changed by the operator at the time when they are displayed. The contents of the A and Q registers on the second and third stops is defined below. (Parameter timeout will occur after last stop)

a. Stop 2

A = WE01, where the W field is bits 15-11 and identifies the 17X6* equipment address. The allowable values for the 5-bit W field are:

00010 - for 17X6 number 1

00111 - for 17X6 number 2

01100 - for 17X6 number 3

The E field is bits 10-7 and identifies the 1731/1732 Magnetic Tape Controller
Q = 000U, where U specifies the 601 or 602 Magnetic Tape Unit which will be used for I/O in sections 2, 3, and 4.

*17X6 refers to either 1706 or 1716, whichever is being used or tested.

b. Stop 3

A = The End of Operation interrupt line for the 17X6. Only one bit is set in this word. The bit position must identify the interrupt line. For example, if the End of Operation interrupts from the 17X6 are to be received on line 5, only bit 5 of this word would be set. Q register contents are described below:

- Bit 15 = 1: A 1716 is connected to this computer.
- Bit 15 = 0: A 1706 is connected to this computer.
- Bit 14 = 1: This computer will initiate the first output if section 6 is selected to be run.
- Bit 14 = 0: The other computer will initiate the first data transfer if section 6 is selected to be run.
- Bit 5 = 1: Run test section 6. This section will use the 1716 to transfer data between two computers which are necessary to run this section. A common 1716 must be connected to both the computers. Bit 14 of this parameter must be set in one of the computers. Bit 14 of the other computer must be equal to zero. The decision to repeat Section 6 must be made in the computer which has bit 14 = 0.
- Bit 4 = 1: Run test Section 5. This section will use the 1716 to make block transfers of data within a computer's core storage.
- Bit 3 = 1: Run test Section 4. This section uses the 17X6 1731/1732 and a 601/608/609 to test direct output/input of data.
- Bit 2 = 1: Run test Section 3. This section uses the 17X6, 1731/1732 and a 601/608/609 to test the current word address of the 17X6.
- Bit 1 = 1: Run test Section 2. This section will use the 17X6, 1731/1732 and a 601/608/609 to test buffered output/input.
- Bit 0 = 1: Run test Section 1. This section will check the ability of the 17X6 to accept all legal functions (reject should not be received). If a 1716 is connected, this section will also test the flags, masks, and interrupts when corresponding masks and flags are both set.

2. If bit 0 of the Stop/Jump word is not set, the test will be run using the set of prestored parameters. These parameters assume the following:
 - a. 1706 number 1 and equipment number of the 1731/1732 Magnetic Tape Controller is 3.
 - b. Tape unit 7 is ready and write-enabled.
 - c. The End of Operation interrupts from the 17X6 will be received on line 4.
 - d. Test Sections 1, 2, 3, and 4 will be run.
3. Selective Skip and Stop Settings
 - a. STOP switch must be set for running SMM17.
 - b. SKIP switch, when set, displays the Stop/Jump word in Q.

D. MESSAGES

1. Typeouts or Alarms

a. Normal Program Typeouts

- 1) Test identification at start of test
BD200F, 1706/1716 DATA CHANNEL TEST
IA = XXXX, FC = XX
- 2) End of test typeout

A	Q	A	Q
0F24	S/J word	Pass number	Return Address

b. Error Typeouts

If an error occurs, the following information is typed out:

- 1) Identification word
- 2) Stop/Jump word
- 3) Test section/error number
- 4) Return address
- 5) Additional information related to the specific error

A sample error typeout is shown and described as follows:

A	Q	A	Q	A	Q
0F38	000F	0107	0507	0201	1800

0F38 is the identification word where

F is the test number

3 is the number of stops in this error stop sequence

8 identifies the stop as an error stop (bit 3 set)

000F is the Stop/Jump word

0107 is the section number and error number (Section 1, error number 7)

0507 is the address in the program (list address) where the error occurred.

0201 was the status of the 17X6 prior to the attempt to terminate the buffer (see information under error number 7).

1800 was the contents of Q when the attempt to terminate the buffer was made (see information under error 7).

2. Error Codes

An error code is displayed in the lower two digits of the A register on the second stop of all error stop sequences. A description of the error codes used and the additional information displayed on each error is described below.

<u>Error</u>	<u>Description</u>
01	Incorrect test parameter was entered. The program will make another parameter stop when restarted.
02/03	External/internal reject on attempt to input 17X6 status. If this error condition is not repeated (bit 4 of the Stop/Jump word set), the test will make a final exit to SMM. A = 0000 Q = Contents of Q when the input was attempted
04	Ready not set on 17X6 status. If the condition is not repeated the test will be terminated. A = 17X6 status Q = Equipment address of the 17X6

<u>Error</u>	<u>Description</u>
05/06	External/internal reject on input of the 17X6 current address A = 0000 Q = Contents of Q when input was attempted
07/08	External/internal reject on Terminate Buffer operation on 17X6 A = 17X6 status prior to the Terminate Buffer operation Q = Contents of Q when Terminate Buffer was attempted
09/0A	External/internal reject on attempt to output a function to the 17X6 A = Contents of A when output was attempted Q = Contents of Q when output was attempted A = Status of the 17X6 prior to the output Q = 0000
0B/0C	External/internal reject on direct output of a function to the 1731/1732 A = Contents of A when the output was attempted (function) Q = Contents of Q when output was attempted A = Status 1 of the 1731/1732 prior to output Q = Status of the 17X6 prior to the output
0D/0E	External/internal reject on input of status one of the 1731/1732 A = Status of the 17X6 prior to the input Q = Contents of Q when the input was attempted
0F/10	External/internal reject on input of status two of the 1731/1732 A = Status of the 17X6 prior to the input Q = Contents of Q when the input was attempted
11	No write ring in selected tape unit A = Status 2 of the tape unit Q = WEOU, where W is the address of the 17X6, E is the equipment number of the 1731/1732 and U is the selected tape unit.
12	Selected tape unit is protected A = Status 1 of the tape unit Q = WEOU

<u>Error</u>	<u>Description</u>
13/14	<p>External/internal reject on attempt to initiate a buffered output to the 601/608/609.</p> <p>A = Contents of A when output was attempted (FWA-1) Q = Contents of Q when output was attempted</p> <p>A = Status 1 of the tape unit prior to the output Q = Status of the 17X6 prior to the output</p>
15/16	<p>External/internal reject on attempt to initiate a buffered input from the 601/608/609.</p> <p>A = Contents of A when the output was attempted (FWA-1) Q = Contents of Q when the output was attempted</p> <p>A = Status 1 of the tape unit prior to the output Q = Status of the 17X6 prior to the output</p>
17/18	<p>Busy bit of the 17X6 status did not set after initiating a buffered output/input</p> <p>A = 17X6 status Q = 0000</p>
19/1A	<p>The Device Reply bit (bit 9) of the 17X6 status was never set within a time period after initiating a buffered output/input.</p> <p>A = the last 17X6 status input Q = 0000</p>
1B/1C	<p>The Device Reject bit (bit 8) of the 17X6 status was never set within a time period after initiating a buffered output/input.</p> <p>A = The last 17X6 status input Q = 0000</p>
ID	<p>The End of Operation bit (bit 4) of the 17X6 status is set at the same time as Busy (bit 1) is set.</p> <p>A = 17X6 status Q = 0000</p>
1E/1F	<p>The End of Operation bit (bit 4) of the 17X6 status is not set after the Busy dropped at the completion of a buffered output/input.</p> <p>A = 17X6 status Q = 0000</p>

<u>Error</u>	<u>Description</u>
20/21	<p>No reject received from the 17X6 on an attempt to execute a direct output/input to the 17X6 when the 17X6 was Busy.</p> <p>A = Status of the 17X6 prior to the output Q = 0000</p>
22/23	<p>No interrupt received from the 17X6 on end of operation after a buffer was completed.</p> <p>A = Status 1 of the tape after the buffer was completed Q = Status of the 17X6 after the buffer was completed</p>
24/25	<p>Alarm bit set in tape status 1 after a buffered output/input was completed</p> <p>A = Status 1 of the tape after the buffer was completed Q = Status of the 17X6 after the buffer was completed</p>
26/27	<p>Interrupt bit (bit 2) of the 17X6 status was not set after an End of Operation interrupt occurred when a buffer output/input was completed.</p> <p>A = Status 1 of the tape unit after the buffer was completed Q = Status of the 17X6 after the buffer was completed</p>
28	<p>Data error occurred</p> <p>A = Data read Q = Expected value</p> <p>A = Word number within the block which is incorrect Q = 0000</p>
29	<p>Current address of the 17X6 was not equal to 0008 after initiating a buffered output with first word address equal to 0007. (The 1731/1732 will accept the first data word and the 17X6 will increment the current address prior to the program inputting the current address.)</p> <p>A = The current address which was input Q = 0000</p>

<u>Error</u>	<u>Description</u>
2A	<p>The current address input from the 17X6 was neither greater nor the same as the previous current address input while a buffered output was active.</p> <p>A = The previous current address Q = The last current address input</p>
2B/2C	<p>The End of Operation status bit (bit 4) was not set in the 17X6 status when an Interrupt on End of Operation occurred after a buffered output/input was completed.</p>
2D	<p>Reserve bit (bit 3) in the 1716 status is still set after executing a Terminate Buffer.</p> <p>A = 1716 status Q = 0000</p>
2E	<p>Reserve bit (bit 3) in the 1716 status is still set after executing the function to clear it.</p> <p>A = Contents of A when the function was output Q = Contents of Q on the output</p> <p>A = 1716 status after the function Q = 0000</p>
2F	<p>Flag bit not set in the 1716 status after executing function to set it.</p> <p>A = Contents of A when function was output Q = Contents of Q when function was output</p> <p>A = 1716 status after the function Q = 0000</p>
30	<p>Flag bit set in the 1716 status after executing function to clear it.</p> <p>A = Contents of A when function was output Q = Contents of Q when function was output</p> <p>A = 1716 status prior to function Q = 1716 status after executing function</p>

<u>Error</u>	<u>Description</u>
31	<p>No interrupt received from the 1716 after setting a Mask bit and then setting the corresponding flag bit.</p> <p>A = Contents of A to set mask Q = Contents of Q used when setting the Mask and the Flag bits</p> <p>A = Contents of A to set Flag bit Q = Present status of the 1716</p>
32/33	<p>External/internal reject received from the 1716 when attempting to initiate a buffered transfer.</p> <p>A = Contents of A when output was attempted Q = Contents of Q when output was attempted</p> <p>A = Status of the 1716 prior to attempting the buffered transfer Q = Status of the 1716 after receiving the reject</p>
34	<p>Flag status bits are not equal to the expected flags. The other computer set a certain configuration of flags and then stored a word in this computer's core storage indicating the present state of the flag bits. The flags did not correspond to the indication word.</p> <p>A = Status of the 1716 Q = Expected status of the 1716 (flag bits are in bits 10-14)</p>
35	<p>Data error in data the other computer sent this one. If the error condition is to be repeated, set bit 4 in the Stop/Jump word of the other computer when it types out error number 36.</p> <p>A = Data received from other computer Q = Data expected</p> <p>A = Word number within data block Q = 0000</p>
36	<p>The other computer detected at least one data error in the data this computer sent it. (The other computer has typed out error number 35 (one or more times).</p> <p>A = Number of errors found by other computer Q = 0000</p>

<u>Error</u>	<u>Description</u>
37	Data error in data this computer sent the other computer and then read back to this one. A = Data word read back Q = Data word originally sent to other computer A = Word number within block Q = 0000
38	Interrupt bit not set in the 1716 status after an interrupt occurred because the corresponding mask bit and flag bit were both set. A = Status of the 1716 after the interrupt occurred Q = 0000
39/3A	Alarm bit set in status 1 of the 1731/1732 after a direct output/input A = Status 1 of the 1731/1732 Q = Status of the 1716
3B	Interrupt not received after a data transfer was completed. A = Status of the 1716 Q = 0000

E. ERROR STOPS

Error stops will occur if bit 3 of the Stop/Jump word is set, the STOP switch is set, and an error occurs.

II. DESCRIPTION

A. METHOD

1. Initialization

- a. Convert bias value and frequency count and store in typeout routine.
- b. Type out the test title, and frequency count.
- c. Store return address.
- d. Make parameter stop if bit 1 of Stop/Jump word is set.
- e. Set up for control to be given to distributor on return from SMM.
- f. Return control to SMM.

2. Distributor

- a. Run Section 1 if selected.
- b. Stop at end of section if bit 1 of Stop/Jump word is set.
- c. Go to a if bit 5 of Stop/Jump word is set (repeat section).
- d. Run Section 2 if selected.
- e. Stop at end of section if bit 1 of Stop/Jump word is set.
- f. Go to d if bit 5 of Stop/Jump word is set.
- g. Run Section 3 if selected.
- h. Stop at end of section if bit 1 of Stop/Jump word is set.
- i. Go to g if bit 5 of Stop/Jump word is set.
- j. Run Section 4 if selected.
- k. Stop at end of section if bit 1 of Stop/Jump word is set.
- l. Go to j if bit 5 of Stop/Jump word is set.
- m. Run Section 5 if selected.
- n. Stop at end of section if bit 1 of Stop/Jump word is set.
- o. Go to m if bit 5 of Stop/Jump word is set.
- p. Run Section 6 if selected.
- q. Add 1 to pass counter.
- r. Stop at end of test if bit 2 of Stop/Jump word is set.
- s. Go to b if bit 6 of Stop/Jump is set (repeat test).
- t. Check if new parameters are to be entered (bit 10 of Stop/Jump word set).
- u. Load bias and exit to SMM.
- v. Go to a if SMM returns control (test frequency was greater than 1).

3. Section 1

- a. Purpose: Check the static conditions of a 17X6. Checks for no rejects on all legal functions which will not initiate data transfer.
- b. Procedure:
 - 1) Check for Ready set on 17X6.
 - 2) Check for no reject received on input of current address.

- 3) Check for no reject received on Terminate Buffer.
- 4) Check for reserve clear if 1716.
- 5) Check for no reject received on Select and Clear interrupt functions.
- 6) If 1706 return to distributor.
- 7) Clear all masks and flags.
- 8) Test for interrupts after setting each mask and then the corresponding flag.
- 9) Return to distributor.

4. Section 2

a. Purpose: To test the data transfer capabilities of the 17X6. Interrupt on End of Operation is also tested.

b. Procedure:

- 1) Set reserve bit if 1716.
- 2) Check for selected tape unit write-enabled and non-protected.
- 3) Rewind.
- 4) Select 200 BPI.
- 5) If this is an odd record of the current data pattern, select binary; if even, select BCD.
- 6) Select interrupt from 17X6 on End of Operation
- 7) Initiate buffer output.
- 8) Check for Busy set in 17X6 status.
- 9) Check for device Reject set.
- 10) Check for a reject on output to 17X6 while 17X6 is Busy.
- 11) Check for device Reply set in 17X6 status.
- 12) Return control to SMM.
- 13) Check for End of Operation bit set after Busy clears.
- 14) Check if interrupt occurred on End of Operation.
- 15) Check if Interrupt and End of Operation bits were set in 17X6 status when interrupt occurred.
- 16) Check tape status.

- 17) If 20 records of current data pattern have not been written, go to 5).
- 18) If all data patterns have not been used, change patterns and go to 5).
- 19) Rewind.
- 20) If odd record, select binary; if even, select BCD.
- 21) Select Interrupt on End of Operation from 17X6.
- 22) Initiate buffer input.
- 23) Check for Busy set on 17X6.
- 24) Check for device Reject set in 17X6 status.
- 25) Check for a reject on output to 17X6 while it is Busy.
- 26) Check for device Reply set in 17X6 status.
- 27) Return control to SMM.
- 28) Check for End of Operation bit set when Busy clear.
- 29) Check if Interrupt on End of Operation occurred.
- 30) Check if Interrupt and End of Operation bits were set in 17X6 status when interrupt occurred.
- 31) Check tape status.
- 32) Check data.
- 33) If 20 records of current data pattern have not been read, go to 20).
- 34) If all data patterns have not been read, change patterns and go to 20).
- 35) Rewind.
- 36) Clear reserve if 1716.
- 37) Return to distributor.

5. Section 3

- a. Purpose: Check the ability of the 17X6 to increment the current address correctly.
- b. Procedure
 - 1) Set reserve if 1716.
 - 2) Rewind and select 200 BPI.
 - 3) Initiate buffer output with FWA = 0007.
 - 4) Input current address of 17X6 and check for 0008.

- 5) Input current address and check for equal or one greater than the previous one input.
- 6) If End of Operation is not set go to 5).
- 7) Clear reserve if 1716.
- 8) Return to distributor.

6. Section 4

- a. Purpose: Check the direct I/O of data to a 601/608/609 via the 17X6.
- b. Procedure:
 - 1) Set Reserve bit if 1716.
 - 2) Rewind and select 200 BPI.
 - 3) If odd record of current data pattern, select binary; if even, select BCD.
 - 4) Do direct output of 500 words.
 - 5) Check for alarm up on tape unit.
 - 6) If 20 records of current data pattern have not been written go to 3).
 - 7) If all data patterns have not been used, change patterns and go to 3).
 - 8) Rewind.
 - 9) Initialize data pattern and record count.
 - 10) If odd record, select binary; if even, select BCD.
 - 11) Do direct input of 500 words.
 - 12) Check for alarm up on tape unit.
 - 13) Check the data.
 - 14) If 20 records of current pattern have not been read, go to 10).
 - 15) If all data patterns have not been used, change patterns and go to 10).
 - 16) Rewind.
 - 17) Return to distributor.

7. Section 5

- a. Purpose: Check the ability of a 1716 to transfer a block of data from an area of storage to a different area within the same computer.

b. Procedure

- 1) Set reserve on 1716.
- 2) Set up output area.
- 3) Select Interrupt on End of Operation.
- 4) Initiate buffered transfer and exit to SMM until complete.
- 5) Check if interrupt occurred.
- 6) Check data.
- 7) Go back to 3) if the current data pattern has not been buffered 100 times.
- 8) Change data patterns and go back to 2) if all patterns have not been used.
- 9) Clear reserve.
- 10) Return to distributor.

8. Section 6

a. Purpose: Check the ability of a 1716 transfer data between two 17X4 Computers.

b. Procedure: In the following sequence of steps, Computer A is initially defined as the computer in which bit 14 of Q equals 1 on the third parameter stop. The other computer is B. TMESS is an absolute location in "this" computer (location 0052). OMESS is the same absolute location in the "other" computer.

- 1) If computer B, go to 22).
- 2) Set reserve on 1716.
- 3) Wait for B to set OMESS to its FWA of data area.
- 4) Initiate buffered transfer to B.
- 5) Set flags equal to the lower five bits of code which identify the data pattern.
- 6) Transfer data code to OMESS.
- 7) Wait for OMESS to change values.
- 8) If negative, B found at least one data error.
- 9) Initiate buffered transfer from B to A.
- 10) Check data.

- 11) Go to 4) if current pattern has not been transferred 100 times.
- 12) Go to 14) if all data patterns have been transferred.
- 13) Change data patterns and go to 4).
- 14) If this computer was initially B, go to 18).
- 15) Clear reserve on 1716.
- 16) Store 0 at TMESS, -0 at OMESS.
- 17) Switch names of computers and go to 22).
- 18) Stop at end of section.
- 19) If section is to be repeated, go to 15).
- 20) Store 0 at TMESS, 0 at OMESS.
- 21) Clear reserve and return to distributor.

Computer B

- 22) Clear reserve on 1716.
- 23) Set TMESS equal to FWA of buffer area.
- 24) Wait for TMESS to change values.
- 25) If TMESS is -0, go to 31).
- 26) If TMESS is 0, go to 32).
- 27) Check for flags equal to same configuration as lower 5 bits of TMESS.
- 28) Check data.
- 29) If data errors, store the complement of the number of errors at TMESS and go to 24).
- 30) Go to 32).
- 31) Store 0 at TMESS, change names, and go to 2).
- 32) Stop at end of section.
- 33) Return to distributor.

III. PHYSICAL REQUIREMENTS

- A. SPACE REQUIRED - Approximately 2500_{10} locations.
- B. INPUT AND OUTPUT TAPE MOUNTINGS - If Section 2, 3, or 4 is selected to be run a 601/608/609 Tape Unit must be write-labeled and non-protected.

C. TIMING - 3 min. 15 sec.

D. EQUIPMENT CONFIGURATION - computer with 8K memory.

1. Section 1 - 17X4, 1705, 17X6
2. Section 2 - 17X4, 1705, 17X6, 1731/1732, 601/608/609
3. Section 3 - 17X4, 1705, 17X6, 1731/1732, 601/608/609
4. Section 4 - 17X4, 1705, 17X6, 1731/1732, 601/608/609
5. Section 5 - 17X4, 1705, 1716
6. Section 6 - two 17X4's, two 1705's, one 1716

1738/853, 854 DISK PACK TEST

(DP1008 Test No. 8)
(CP=2F)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

- a. The range of cylinders upon which data will be written may be limited during the parameter stop. However, the lower limit is ignored in Section 12 (data is written in cylinder 0 to be autoloading).
- b. A large number of typeouts and/or stops may occur for error codes 14, 1B, and 1D unless bit 11 of the Stop/Jump parameter is set.
- c. There may be insufficient core for a long buffer operation if memory is only 8k and more than one test is loaded before the disk pack test is loaded. In this case neither section 6 nor 9 will be run unless the operator selects one or both of them. If the operator selects 6 or 9 in this case, short buffer operations are performed and each of these two sections may take an hour for an 853 disk drive unit.
- d. Section 7 (overlap seek) requires two disk packs. If an attempt is made to run this section with only one disk pack, the program will loop on an external reject of an output from A, and the director status will become Not Ready and Not on Cylinder.
- e. In Section 12 (autoload) the program may be destroyed if unnecessary data is loaded into core by the Autoload function. Memory wraparound will occur if an attempt is made to run this section with only 4k of memory.
- f. When using a new pack it is necessary to ensure that the pack is filled with correct data and checkwords. Data can be destroyed in shipment. Running section 6 first will ensure that the pack contains correct data required for other sections.
- g. Bits 2 and 3 of SMM parameter word must specify the correct machine type.

B. LOADING PROCEDURE

1. The test operates as a subprogram under control of the 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17.
3. The test can be restarted after loading from initial address.

C. PARAMETERS

1. Normal operation requires no parameters. The following sections will be run under this condition:
 - a) Section 1
 - b) Section 2
 - c) Section 3
 - d) Section 4
 - e) Section 5
 - f) Section 8
 - g) Section 9 (unless core size is insufficient)
 - h) Section 13

The test will be run on unit 0, the unit will be assumed to be an 853, and cylinders 0 through 99 will be tested. The interrupt line will be line 2.

2. To alter the parameters, follow the directions stated in SMM17. If the bit is set, the corresponding section or condition will be selected. The parameter words to be displayed are as follows:
 - a. First stop: A = 0831, Q = Stop/Jump parameter
 - b. Second stop:
 - Bit 0 of A = Section 1 - static status check
 - Bit 1 of A = Section 2 - random positioning
 - Bit 2 of A = Section 3 - write, read, compare
 - Bit 3 of A = Section 4 - same as section 3 except under control of Alarm and End of Operation interrupts.
 - Bit 4 of A = Section 5 - force address errors, check write and read into next cylinder.
 - Bit 5 of A = Section 6 - surface test, Alarm and End of Operation interrupts selected.
 - Bit 6 of A = Section 7 - check overlap seek (two disk packs needed)
 - Bit 7 of A = Section 8 - same as section 3 except under control of Alarm and Ready, Not Busy interrupts
 - Bit 8 of A = Section 9 - same as Section 6 except under control of Alarm and Ready, Not Busy interrupts
 - Bit 9 of A = Section 10 - write address tags

Bit 10 of A = Section 11 - positioning timing check
 Bit 11 of A = Section 12 - autoload check (Caution: See Restriction).
 Bit 12 of A = Section 13 - check for recoverable errors
 Bit 13 of A = 0, Unit 0
 Bit 13 of A = 1, Unit 1
 Bit 14 of A Not used
 Bit 15 of A = 0, 853
 Bit 15 of A = 1, 854
 Q=XXYY
 XX=lowest numbered cylinder to be written on (Section 12 ignores this limit)
 XX=00-standard
 YY=highest numbered cylinder to be written on.
 YY=63₁₆ - standard for 853
 YY=CA₁₆ - standard for 854

c. Third stop:

A = interrupt line (e.g., bit 3 in A set for interrupt line 3)
 Q = not significant.

d. SELECTIVE JUMP AND STOP SETTINGS

It is advisable to set bit 11 of the Stop/Jump parameter to decrease the number of error typeouts for error code 14 (sections 3, 4, 5, 8), error

3. A typeout of parameters will occur after last stop.

D. SELECTIVE JUMP AND STOP SETTINGS

It is advisable to set bit 11 of the Stop/Jump parameter to decrease the number of error typeouts for error code 14 (sections 3, 4, 5, 8), error code 1B (sections 6, 9), and error code 1D (section 12).

E. MESSAGES

1. Typeouts or Alarms

a. Normal Program Typeouts

1. Disk pack identification during test initialization:

```

DP1A08 1738 DISK PACK TEST
CP2F, VER. 3.1
IA = XXXX, FC = XX
  
```

2. End of Test

A	Q	A	Q
0824	Stop/Jump Parameter	Pass Number	Return Address

b. Error Alarms

All information shown is displayed after General Display Format.

General Display Format:

A	Q	A	Q
Information	Stop/Jump	Section	Return
Word (838 for 3 stops, 848 for 4 stops)	Parameter	Error Code	Address

c. Error Codes

01 - Internal reject of input to A

A = BADD

Q = contents of Q upon input to A

A = contents of A upon last output from A

Q = contents of Q upon last output from A

02 - Internal reject on output from A

A = director status

Q = address register status

A = contents of A upon output from A

Q = contents of Q upon output from A

03 - Interrupt status bit not set when interrupt occurred

A = selected interrupts

1 - Ready, Not Busy

2 - End of Operation

4 - Alarm

Q = status upon interrupt

A = contents of A upon last output from A

Q = contents of Q upon last output from A

04 - Non-selected interrupt occurred (or interrupt occurred too soon)

Display is the same as for error code 03

05 - Interrupt status bits not cleared by Clear Interrupt function

A = status upon interrupt

Q = status after attempting to clear interrupts

A = contents of A upon last output from A (other than Clear Interrupt function)

Q = contents of Q upon last output from A (other than Clear Interrupt function)

06 - Ready status not present

A = director status

Q = address register status

A = contents of A upon last output from A (other than Clear Interrupt function)

Q = contents of Q upon last output from A (other than Clear Interrupt function)

07 - On Cylinder status not present

A = director status

Q = address register status

08 - Busy not present after an output from A. Display same as for error code 06

09 - Storage parity error

Display same as for error code 06

0A - Defective track

Display same as for error code 06

0B - Address error

Display same as for error code 06

0C - Seek error

Display same as for error code 06

0D - Lost data

Display same as for error code 06

0E - Checkword error

Display same as for error code 06

0F - Protect fault

Display same as for error code 06

10 - Alarm condition present but Alarm Status bit not set Display same as for error code 06

11 - Address register status does not equal loaded address after loading address and waiting for Not Busy

A = BADD

Q = director status

A = address register status

Q = loaded address

12 - Not used

13 - Not used

14 - Word written does not equal word read. (This may occur in sections 3, 4, 5, and 8 of the test) Set bit 11 in the Stop/Jump parameter to ignore checking for more errors in this sector.

A = address register status

Q = number of word in error

A = word written

Q = word read

15 - No compare status present

A = director status

Q = address register status after load address

16 - Alarm interrupt did not occur when attempting to force address error by loading illegal address

A = loaded address

Q = director status

A = interrupt line

Q = selected interrupts (see error code 03)

17 - An address error was forced but the address error status bit was not set

A = loaded address

Q = director status

- 18 - No alarm interrupt occurred when attempting to force address error by initiating checkword check with illegal address
Display same as for error code 16
- 19 - Address error status not present when writing off the end of disk pack
Display same as for error code 17
- 1A - Not used
- 1B - Unexpected data was read during surface test. Set bit 11 in the Stop/Jump parameter to ignore rest of errors in this sector or track.
A = sector in error
Q = number of work in error
A = data expected
Q = data read
- 1C - Maximum positioning time (145 ms) was exceeded
A = time required (ms, hexadecimal)
Q = loaded address
- 1D - Autoload failed to load correct data
Set bit 11 in the Stop/Jump parameter to ignore the rest of the words in error
A = BADD
Q = number of word in error
A = word written
Q = word in core after autoload
- 1E - End of Operation status not present
Display same as for error code 16
- 1F - Status other than Ready, On Cylinder is present (ignoring protect status) during static status check
Display same as for error code 07.
- 20 - Alarm interrupt did not occur when writing off the end of disk pack
Display same as for error code 16

- 21 - No interrupt occurred when End of Operation or Ready,
Not Busy interrupt was selected
- A = selected interrupts (see error code 03)
Q = director status
- A = contents of A upon last output from A
Q = contents of Q upon last output from A
- 22 - Not used
- 23 - Not used
- 24 - Alarm status bit set, no alarm conditions
Display same as for error code 06
- 25 - No Compare status not set after attempting to force
No Compare status
- A = director status
Q = address register status
- 26 - First unit went to incorrect address during overlap seek
- A = BADD
Q = director status
- A = loaded address
Q = address register status
- 27 - Second unit went to incorrect address during overlap seek.
Display same as for error code 26
- 28 - Through 2F - Not used
- 30 - Address upon completion of a Read, Write, Compare, or
Checkword Check operation is not equal to the expected
address
- A = contents of Q upon last output from A (other than Clear
Interrupt function)
Q = director status
- A = address register status
Q = expected address
- 31 - Recoverable error occurred during Checkword Check
(section 13)
- A = address of track causing error
Q = director status when last error occurred

32 - Non-recoverable error occurred during Checkword Check
(Section 13)

Display same as for error code 31

33 - through 3F - Not used

40 - Operator error. Interrupt line or equipment address in
error. Test must be reloaded.

A = Selected equipment address

Q = Selected interrupt line (if any)

41 - EXT reject on input to A

A = BADD

Q = Equipment address

A = Contents of A (last output)

Q = Contents of Q (last output)

42 - EXT reject output from A

A = Status

Q = Equipment address

A = Last function contents of A

Q = Last function contents of Q

d. Error Stops

Stops will occur upon errors if Bit 3 in the Stop/Jump parameter
is set.

II. DESCRIPTION

A. METHOD

1. Section 1 - Static Status Check

a. Select unit

b. Input director status

1) Ready should be present .

2) On Cylinder should be present.

3) No other status (other than protected) should be present.

c. Loop to step a 499 times

2. Section 2 - Random Positioning Check

a. Generate 96 random numbers.

b. Convert random number to legal addresses.

c. Select unit.

- d. Load address.
 - e. Check for expected address.
 - f. Check alarm conditions and End of Operation status.
 - g. Update address.
 - h. Loop to step c 95 times.
3. Section 3 - Write, Read, Compare
- a. Generate 96 random words and one random address.
 - b. Select unit.
 - c. Load address, check for expected address, alarm conditions, and End of Operation status.
 - d. Write one sector.
 - e. Check Not Busy address.
 - f. Check alarm conditions and End of Operation status.
 - g. Loop to step b if repeat conditions selected.
 - h. Select unit.
 - i. Load address.
 - j. Read one sector.
 - k. Check Not Busy address.
 - l. Check alarm conditions.
 - m. Loop to step n to repeat conditions.
 - n. Select unit.
 - o. Execute checkword check.
 - p. Check alarm conditions and End of Operation status.
 - q. Check Not Busy address.
 - r. Loop to step n to repeat conditions.
 - s. Select unit.
 - t. Load address, check for expected address, check alarm conditions and End of Operation status.
 - u. Execute Compare function.
 - v. Check for Not Compare status.
 - w. Check alarm conditions and End of Operation status.

- x. Check Not Busy address.
 - y. Loop to step s to repeat conditions.
 - z. If no alarm condition or unexpected address occurred, compare input buffer with output buffer area.
 - aa. Execute read and loop to step Z to repeat condition.
 - ab. Loop to step a 95 times.
4. Section 4 - Write, Read, Compare Under Interrupt Control Same as Section 3 except interrupts on Alarm and End of Operation are selected prior to performing a Load Address, Read, Write, Checkword Check, and Compare operation. After the interrupt occurs, the status upon interrupt is checked for alarm conditions.
5. Section 5 - Force Address Errors and Check Writing Into Next Cylinder
- a. Generate illegal address (00F0).
 - b. Select unit.
 - c. Select interrupt on alarm.
 - d. Load illegal address.
 - e. Check whether correct interrupt occurred.
 - f. Check address Error status.
 - g. Loop to step c to repeat conditions.
 - h. Select interrupt on alarm.
 - i. Initiate checkword check .
 - j. Check whether correct interrupt occurred.
 - k. Check address Error status.
 - l. Loop to step h to repeat conditions.
 - m. Generate an illegal address (FF00).
 - n. Loop to step b once.
 - o. Form last sector address of unit (CA9F for 854, 639F for 853).
 - p. Jump to step v if range of cylinders to be written into is not high enough to include this cylinder.
 - q. Load address, check alarm conditions.
 - r. Write 97 words (off end of disk pack).
 - s. Check whether correct interrupt occurred.
 - t. Check address Error status.
 - u. Loop to step q to repeat conditions.

- v. Generate legal address.
- w. Load address, check alarm conditions.
- x. Write 97 words.
- y. Load address, check alarm conditions.
- z. Add one to second word of buffer area.
- aa. Execute Compare function.
- ab. Check No Compare status (it should be set).
- ac. Loop to step w to repeat conditions.
- ad. Generate address of last sector of a cylinder.
- ae. Load address, check alarm conditions.
- af. Write 97 words (into next cylinder).
- ag. Check alarm conditions.
- ah. Loop to step ae to repeat conditions.
- ai. Load address, check alarm conditions.
- aj. Execute Compare function.
- ak. Check No Compare status and alarm conditions.
- al. Loop to step ai to repeat conditions.
- am. Load address, check alarm conditions.
- an. Read 97 words.
- ao. Check alarm conditions.
- ap. Loop to step am to repeat conditions.
- aq. If no alarm conditions occurred between steps ae to aq, compare input buffer area with output buffer area.
- ar. Loop to step a 95 times.

6. Section 6 - Surface Check

- a. Set up Read and Write routines for a 1536-word buffer (one track) or a 96-word buffer (one sector) depending on available core.
- b. Generate address of first cylinder to be written on.
- c. Generate pattern, 6161 for first pass through section, CECE for second pass.

- d. Fill buffer area with pattern, alternate words complemented.
 - e. Select unit, select interrupts on Alarm and End of Operation.
 - f. Load address and write under interrupt control.
 - g. Check for correct interrupts and alarm conditions.
 - h. Check Not Busy address.
 - i. Loop to step e to repeat conditions .
 - j. Increment address.
 - k. Loop to step f unless address is greater than last cylinder to be written into.
 - l. Re-initialize address.
 - m. Select unit, select interrupts on Alarm and End of Operation.
 - n. Load address and read under interrupt control.
 - o. Check for correct interrupts and alarm conditions.
 - p. Check Not Busy address.
 - q. If not alarm conditions occurred in step m , check whether expected pattern was read .
 - r. Loop to step m to repeat conditions .
 - s. Increment address.
 - t. Loop to step n unless address is greater than address of last cylinder to be written into.
 - u. Loop to step b once.
7. Section 7 - Check Overlap Seek
- a. Generate 96 random numbers.
 - b. Convert to legal addresses.
 - c. Select first unit (unit specified in parameter word during initial parameter stop).
 - d. Load address.
 - e. Wait for End of Operation status (may still be Busy).
 - f. Select other unit.
 - g. Load address.

- h. Wait for End of Operation status (may still be Busy).
 - i. Select first unit.
 - j. Wait for Not Busy.
 - k. Check whether address register status equals loaded address.
 - l. Select other unit .
 - m. Wait for Not Busy.
 - n. Check whether address register status equals loaded address.
 - o. Loop to step c 95 times.
8. Section 8 - Write, Read, Compare under Interrupt Control Same as Section 4 except interrupts on Alarm and Ready, Not Busy are selected
9. Section 9 - Surface Check
Same as Section 6 except interrupts on Alarm and Ready, Not Busy are selected
10. Section 10 - Write Address Tags
- a. Generate address of first cylinder to be written onto.
 - b. Select unit.
 - c. Write addresses on track .
 - d. Wait Not Busy.
 - e. Increment track number.
 - f. Loop to step c unless address is greater than address of last cylinder to be written in.
11. Section 11 - Positioning Time Check
- a. Generate 96 random numbers.
 - b. Convert random numbers to legal addresses.
 - c. Make several of the addresses equal to the lowest and highest possible addresses, alternately.
 - d. Initiate load address, initialize ms count.
 - e. Wait 1 ms.
 - f. Increment ms count.
 - g. Check status for Busy.
 - h. Loop to step e if Busy.

- i. Error if ms count greater than 145_{10} .
 - j. Loop to step d 95 times.
12. Section 12 - Autoload (Caution: See Restrictions)
- a. Move first 1536 (600_{16}) words of core to buffer area.
 - b. Select unit.
 - c. Load address, cylinder zero, track zero, sector zero.
 - d. Wait Not Busy.
 - e. Write 1536 words.
 - f. Change one location in low core.
 - g. Stop.
 - h. Operator should push AUTOLOAD button.
 - i. Compare buffer area with low core.
13. Section 13 - Check Recoverable Errors
- a. Initial address equals zero.
 - b. Select unit.
 - c. Initialize attempt counter.
 - d. Initiate checkword check.
 - e. Wait Not Busy.
 - f. Check status for Checkword, Lost Data, Seek Storage Parity, defective track errors.
 - g. Jump to step m if none set.
 - h. Save Error status.
 - i. Increment attempt counter.
 - j. Loop to step d unless attempt counter equals 10.
 - k. Error is not recoverable.
 - l. Jump to step n.
 - m. No errors if attempt counter equals initial value, recoverable error if not.
 - n. Increment track address.
 - o. Loop to step c unless address is greater than last possible address.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

About 2550_{10} memory locations are required. If sufficient core is available, 1440 additional locations will be used.

B. TIMING (Test Running Alone, No Errors)

1. Section 1 = about 1/4 second
2. Section 2 = 8 to 9 seconds
3. Section 3 = 18 to 22 seconds
4. Section 4 = 18 to 22 seconds
5. Section 5 = 36 to 37 seconds
6. Section 6 = about 3 minutes 35 seconds for an 853, probably twice as long for an 854. Sufficient core will enable writing a track at a time. Without sufficient core for a long buffer, the section is not run unless the operator selects it. In this case, one sector is written at a time. The test will then probably take 16 times as long, or 1 hour.
7. Section 7 = 8 to 9 seconds
8. Section 8 = 18 to 22 seconds
9. Section 9 = same as section 6
10. Section 10 = 30 seconds for an 853, 1 minute for an 854
11. Section 11 = 8 to 9 seconds
12. Section 12 = Variable, operator intervention required
13. Section 13 = 35 seconds for an 853, 70 seconds for an 854. Total for sections 1, 2, 3, 4, 5, 8, 9, 11, and 13 (standard run) is about 6 minutes.

C. ACCURACY

Section 11, the positioning timing check, bases the 145 milliseconds on instruction execution time. If the instruction execution time is a few percent less than 1.1 microseconds, error typeouts may occur which are not true. Thus, in a cool room, error code 1C with calculated time = 92_{16} may be ignored.

D. EQUIPMENT CONFIGURATION

1. 17X4 Computer with 8K memory
2. 17X5 Interrupt Data Channel
3. 1738 Disk Storage System
4. One 853 or 854 Disk Storage Drive (two 853's or 854's are required for section 7).

1739 CARTRIDGE DISK DRIVE CONTROLLER
(CDD078 Test No. 78)
(CP = 2F)

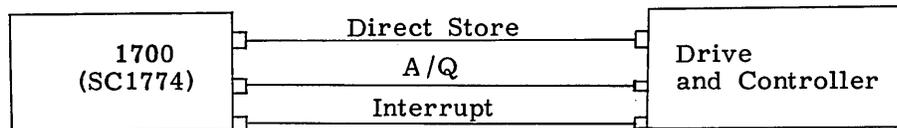
I. INTRODUCTION

The purpose of this test is to verify the operation of the Cartridge Disk Controller and Drive. The test is meant to be an engineering, manufacturing, and field maintenance test. The test will be run in an ascending order, each test becoming progressively more complex.

II. REQUIREMENTS

A. HARDWARE

The test is intended to verify the 1739 Cartridge Disk Controller. The controller is connected to the DSA and to the AQ Channel of the 1704/1705, SC1774/1773/1775, or 1784.



B. SOFTWARE

The test will reside under SMM17 and all rules of SMM17 apply.

NOTE

All references made in this document are to the 1700 System Maintenance Monitor (SMM17) Reference Manual.

C. ACCESSORIES

None

III. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

- a. The range of cylinders upon which data will be written on disk 0 (cart-ridge) may be limited during the parameter stop. The low limit must be zero for Section 12 (data is written on cylinder 0 to be autoloading). Range limits do not apply to fixed disk.
- b. A large number of typeouts and/or stops may occur for error codes 14, 1B, and 1D unless bit 11 of the Stop/Jump parameter is set.
- c. In Section 12 (Autoload) the diagnostic may be destroyed if the Autoload function is not working properly. Section 12 should not be run on a Maintenance Pack.
- d. When using a new pack, it is necessary to ensure that the pack has address tags, correct data, and checkwords. Data may be destroyed in shipment. Section 10 and then Section 7 should be run to ensure that the pack contains the correct data required for other sections.
- e. Bits 2 and 3 of the SMM parameter word must specify the correct machine type.

B. LOADING PROCEDURE

1. The test operates as a sub-program under control of the 1700 System Maintenance Monitor (SMM17).
2. The test mnemonic is CDD, number 78.
3. The calling sequence is that specified by SMM17.

C. PARAMETERS

1. If no parameter stop is made, the following sections will be run.
 - a. Section 1
 - b. Section 2
 - c. Section 3
 - d. Section 4
 - e. Section 5
 - f. Section 6
 - g. Section 8
 - h. Section 9
 - i. Section 13
 - j. Section 15

The test will run on disk 0 (cartridge) and will ignore fixed disk. Cylinder 5 through CA₁₆ will be tested. The interrupt line will be line 3.

2. To alter the parameters, follow directions stated in the SMM17 Reference Manual. If bit is set, the corresponding section or condition will be selected. The parameter words to be displayed are as follows:

a. First Stop: A = 7821, Q = Stop/Jump Parameter.

b. Second Stop:

Bit 0 of A = Section 1 - preliminary check.

Bit 1 of A = Section 2 - register verification test.

Bit 2 of A = Section 3 - positioner check.

Bit 3 of A = Section 4 - read, write, and compare.

Bit 4 of A = Section 5 - same as Section 4 except under control of Alarm and End of Operation interrupts.

Bit 5 of A = Section 6 - read, write, compare through cylinders.

Bit 6 of A = Section 7 - surface test.

Bit 7 of A = Section 8 - worst pattern and checkword generator test.

Bit 8 of A = Section 9 - same as Section 4 except under Control of Alarm and Ready, Not Busy interrupts.

Bit 9 of A = Section 10 - write address tags.

Bit 10 of A = Section 11 - positioning time test.

Bit 11 of A = Section 12 - autoload check.

Bit 12 of A = Section 13 - checkword check.

Bit 13 of A = Section 14 - protect test.

Bit 14 of A = Section 15 - crosstrack test.

Bit 15 of A = 0 means cartridge only present.

Bit 15 of A = 1 means fixed disk also present.

Q = XXYY

XX = lowest numbered cylinder to be written on (Section 12 ignores this limit)

XX = 05 - standard

YY = highest numbered cylinder to be written on

YY = CA₁₆ - standard

c. Third Stop:

A = interrupt line (for example, bit 3 in A set for interrupt line 3)

Q = interrupt line (for example, bit 3 in Q set for interrupt line 3)

d. Fourth Stop:

A = 0 - BAD track address

Q = N/A

Enter known bad track addresses in A and run.

Clear A and run to proceed with test.

- e. SELECTIVE SKIP and STOP Settings:
 - 1) STOP - must be set for running of SMM17.
 - 2) SKIP - when set, the Stop/Jump word is displayed in Q.

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

- 1. Normal Program Typeouts
 - a. Test identification during test initialization:

CDD078, Cartridge Disk Controller Test
 CP2F, Ver. 3.1
 IA = XXXX, FC = XX

- b. During test Section 14 one of the following typeouts will occur:

Set PROTECT switches
 Clear PROTECT switches

- c. End of Test

A	Q	A	Q
7824	Stop/Jump Parameter	Pass Number	Return Address

- 2. Error Alarms

All information shown is displayed after General Display Format.

General Display Format:

A	Q	A	Q	etc.
Information Word (7838 for 3 stops) (7848 for 4 stops)	Stop/Jump Parameter	Section/ Error Code	Return Address	Additional Data

B. ERROR CODE DICTIONARY

Message Code (Hexadecimal)	Program Tag Name	Message and Description
00	INP OUTPUT	External Reject Q = Contents of Q at Reject A = N/A

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
01	INP CLRCON IECHK IED	Internal reject on input to A A = BADD Q = Contents of Q when input to A A = Contents of A during last output Q = Contents of Q during last output
02	OUTPUT IEA	Internal reject on output A = Director status Q = Cylinder register status A = Contents of A when output attempted Q = Contents of Q when output attempted
03	IEC	Interrupt received but interrupt status bit not set A = Selected interrupts Q = Director status at interrupt A = Contents of A during last output Q = Contents of Q during last output
04	IEB	Interrupt other than was selected occurred (or interrupt occurred too soon) Display same as error code 03
05	IEE	Interrupt status bits not cleared by clear interrupt function A = Director status at interrupt Q = Director status after clear interrupt function A = Contents of A during last output Q = Contents of Q during last output
06	CONALARM	Ready status bit not present A = Director status Q = Cylinder register status A = Director status at instant of alarm. (True cylinder status when seek error (code B) is detected.) Contents of A on last output if no alarm detected Q = Contents of Q on last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
07	SECIA	On cylinder status bit not present A = Director status Q = Cylinder register status A = Contents of A at last output Q = Contents of Q at last output
08	BUSYPRES	Busy not present as expected A = Director status Q = N/A
09	CONALARM	Storage parity error Display same as error code 06
0A	CONALARM	Drive fault (non-recoverable) Display same as error code 06
0B	CONALARM	Seek error (controller). This error should recover. Display same as error code 06
0C	CONALARM	Address error Display same as error code 06
0D	CONALARM	Lost data Display same as error code 06
0E	CONALARM	Checkword error Display same as error code 06
0F	CONALARM	Protect fault Display same as error code 06
10	CONALARM	Alarm condition present but alarm status bit not set Display same as error code 06
11	ADDRESS	Cylinder register status does not equal expected value A = BADD Q = Director status A = Cylinder register status Q = Expected cylinder register

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
12	WAIT	Controller hung or busy A = Director status Q = Address of originating routine (BIASED) A = Director status at instant any alarm occurred Q = Contents of Q during last output
13	CONALARM	Seek error (drive) Display same as error code 06
14	COMPARE	Data compare error. Write buffer and read buffer are compared in computer A = Cylinder register status Q = Number of word in sector that is wrong A = Word written Q = Word read (By setting bit 11 in Stop/Jump parameter, multiple errors in the same buffer can be eliminated)
15	COMBUF CB2	No compare status bit set A = Director status Q = Cylinder register status
16	SEC6B	No alarm interrupt occurred when forcing an add- ress error by sending illegal difference A = Illegal difference sent Q = N/A
17	SEC6D	An address error was forced but status bit not set A = Illegal address Q = Interrupt status
18	SEC1N	Cylinder, CWA, Checkword, or True cylinder not clear after clear controller was sent A = Contents of incorrect register Q = Function code for incorrect register
19	SEC6I	Address error status not set when writing off end of file Display same as for error code 17

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
1A		Not used
1B	SEC7 ERROR	Surface check detected error A = Address of sector in error Q = Number of words into sector A = Data written Q = Data read (By setting bit 11 in Stop/Jump parameter, multiple errors in the same buffer can be eliminated)
1C	SEC11B	Maximum positioning time exceeded (96 milliseconds) A = Actual length to position Q = Address positioned to A = Address positioned from Q = N/A (To make this error valid, bit 2 in SMM parameter must be set for SC1774)
1D	S12D	Auto load failed to load correct data A = BADD Q = Word in error A = Word written Q = Word in core after autoloading
1E	CONALARM	End of operation status not present Display same as error code 06
1F	SEC1J-SEC1B	Status other than Ready and On Cylinder after an output function A = Director status Q = Expected status
20	SEC6X	Alarm interrupt did not occur when writing off end of file A = Last address of file Q = N/A
21	ADPRINTP WRT1 RD 1 CW 1 CB 1	No interrupt occurred when EOP, Ready, Not Busy interrupts were selected A = Selected interrupt Q = Director status A = Contents of A during last output Q = Contents of Q during last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
22	SEC1K	Expected external reject on forced busy did not occur A = 0 - illegal reply; 100-internal reject Q = N/A
23	CWACOMP	Current Word Address register incorrect A = Actual CWA contents Q = Expected CWA contents A = Contents of A during last output Q = Contents of Q during last output
24	CONALARM	Alarm bit set, no alarm conditions set. Display same as error code 06
25	SEC6M	No compare status bit not present A = Director status Q = Cylinder register status
26	CDFFA	Cylinder register status does not equal true cylinder status (upper 8 bits only) A = Cylinder register status Q = True cylinder status A = Contents of A during last output Q = Contents of Q during last output
27	CNFE	Cylinder register status incorrect after an operation A = Cylinder register status Q = Expected register contents A = Contents of A during last output Q = Contents of Q during last output
28	SEC1M	Did not get external reject on illegal input director 06 and 07 A = 10 - illegal reply; 0 - internal reject Q = Contents of Q during input
29	SEC14G	Expected protect fault did not occur A = Director status Q = N/A A = Contents of A during last output Q = Contents of Q during last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
2A		CWA did not indicate word address of protect fault A = Contents of CWA at protect fault Q = Address that protect fault should have occurred
2B	SEC14B	Illegal reply or internal reject on unprotected output command
2C	SEC14C	Input instruction was not accepted on protected controller
2D		Not used
2E	SEC1Q	Output buffer length with immediate input of CWA gave incorrect results A = Contents of CWA register Q = Value sent as buffer length
2F		Not used
30	CHKTRK	Cylinder register not equal to expected value after an operation was executed A = Last output function Q = Director status A = Cylinder register status Q = Expected cylinder status
31	SECTION 13	Recoverable error occurred during checkword check A = Address of track causing error Q = Director status when last error occurred
32	SECTION 13	Non-recoverable error occurred during checkword check. Display same as error code 31
33	SEC2J	Suspected DSA address error (Read/Write must have been verified). In a manufacturing test environment test 2 is necessarily run before test 4 because of degree of difficulty. However, when error 33 occurs, then test 4 must be run before test 2 can be completely verified A = DSA address at failure (THIS IS FWA) Q = N/A A = Data written as determined by software Q = Data read from disk

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
34	SEC15	Crosstrack error A = Address of the error detected Q = First of the three tracks that were used
35	STBT SEC7	Table of Bad Track has been exceeded (limit is 10)
36	SEC8E, G, H, etc.	An incorrect checkword was detected A = Checkword status Q = Expected checkword status
37	S11T3	Cylinder to cylinder position time exceeded A = Actual time Q = Specified limit
38	RE1A	Unrecovered seek error A = Director status after recovery attempt Q = Cylinder status after recovery attempt (Exit from this error will be an automatic abort and restart of test)
39-3F		Not used
40		Operator error. Interrupt line or equipment address in error. Restart of test A = Selected equipment address Q = Selected interrupt line if any

V. DESCRIPTION

A. GENERAL DESCRIPTION

1. Cartridge Disk Drive Controller (CDD-78) test is divided into 15 individually selectable test sections. Sections 1 through 6, 8, 9, 13, and 15 are normally selected tests. Sections 7, 10, 11, 12, and 14 are optional.

CDD-78 test sections are divided into subsections and are labeled with program tags such as SEC 8A, B, C, etc. Sec 8 is Section 8 and the letter indicates the subsection.

- a. The standard test error messages contain the section currently executing. Each error code defined in the error list contains a program reference tag and each test description contains the applicable error codes. The Return address in error messages (may or may not be biased) gives the listing address the error it came from. It is important to note that the Return address may just give a subroutine area which generated the error. To trace back the error, it may be necessary to go to the beginning of the routine and look in the Return Jump address to get the area in the test you came from. This may have to be done more than once to actually get back to the section that the error indicates caused the error.
- b. Sections are structured to run sequentially.
- c. If an error is encountered, it may be helpful to run other sections for trouble analysis and to get a more favorable sequence of operation.
- d. Normally, the test should run with the entire surface available; however, it may be desirable to restrict the test to certain areas (see parameters).

NOTE

The test may be restricted to as little as one cylinder.

- e. Operations performed with a repeat condition are shown in the test description.
- f. Section 7 is used to determine defective tracks. However, this section cannot be run until there is a high degree of confidence that the Read, Write, and Compare operations are relatively error free.
- g. With a new cartridge or fixed disk, Sections 10 and 7, in that order, must be selected individually to assure address tags and data on entire disk. Failure to do this will cause unrecoverable errors.
- h. Approximate section execution times:

<u>Section</u>	<u>Minutes</u>	<u>Seconds</u>
01		15
02		15
03		15
04		15
05		15
06		5
07	2	22
08		8

<u>Section</u>	<u>Minutes</u>	<u>Seconds</u>
09		15
10		25
11		10
12		N/A
13		20
14		N/A
15		28

Total normal parameter running time is 2 minutes and 20 seconds.
 (Time does not include increased length when second disk is tested.)

B. SECTIONS DESCRIPTION

SECTION 1 PRELIMINARY CHECKS

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
0101 0106	SEC1C	*	Clear controller function Input cylinder register status Input director status
0107 011F	SEC1A		Verify on cylinder present Verify only on cylinder and ready present
0127	SEC1E		Verify cylinder register after CL CONT RC
0101 0102 0102	SEC1F	*	Clear controller function Output clear interrupt function Position forward one cylinder
0127	SEC1F		Check alarms Verify cylinder register RC
011F	SEC1J	*	Verify EOP drops on output function RC
0122	SEC1K	*	Clear controller function Verify busy status give external reject RC WAIT NOT Busy

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC1L		Clear controller function Position to cylinder 1
0117	SEC1LA	*	Verify excess negative difference - address error Verify address error and alarm RC
0128	SEC1M	*	Verify external reject on input director 06 and 07 Execute illegal input function RC
0118	SEC1N	*	Verify all registers zero after clear controller Check CWA status Check checkword status Check true cylinder status RC
012E	SEC1Q	*	Verify all bits operational in CWA register RC Next iteration - jump to SEC1C Repeat section

SECTION 2 REGISTER VERIFICATION TEST

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
0227	SEC2G	*	Clear controller Position cylinder to 5515 ₁₆ Verify cylinder register RC
0227	SEC2A	*	Clear controller Position to cylinder AA8A ₁₆ Verify cylinder register RC

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
0227	SEC2A1	*	Clear controller Position to cylinder CA00 ₁₆ Verify cylinder register RC
0227 0226 0223	SEC2D	*	Verify sector count and advance position to low range Execute Write operation RC Increase sector count Return to position until sector 29
0227 0226 0223	SEC2F	*	Verify buffer lengths Position to low range Execute Write operation RC Change buffer lengths to check all bit positions and return to positioning unless done
0227 0226 0223	SEC2J	*	Verify DSA addressing Execute Write operation Attempt to determine if all DSA addresses are operational (Necessarily this test is dependent on cor- rect DSA address of input buffer when attempting to verify data.) RC Next iteration jump to SEC2G Repeat section

SECTION 3 POSITIONING TEST

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC3		Generate 192 random addresses Clear controller
0327 0326 0323	SEC3A	*	Position to random address Write 60 word buffer RC Update for new address. Return to position until done Repeat section

SECTION 4 READ, WRITE, COMPARE TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC4	Set passcount Clear controller
	SEC4A	Generate random data and random first address
	SEC4B	*# Write 60 word buffer RC
	SEC4C	* Read 60 word buffer RC
	SEC4D	* Checkword check of track RC
0415 0430	SEC4E	* Compare 60 word buffer Check cylinder register advance RC
0414	SEC4F	* Compare data read against data written RSC RC Next iteration jump to SEC4A Repeat section

SECTION 5 READ, WRITE, COMPARE UNDER INTERRUPT CONTROL

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC5	Set section passcount Clear controller
	SEC5Z	Request interrupt
	SEC5D	Generate random data and random address
0521 0530	SEC5A	*# Write under interrupt control Check cylinder register advance RC
0521 0530	SEC5B	* Read under interrupt control Check cylinder register advance RC

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
0521	SEC5C	* Checkword check under interrupt control RC
0521 0515 0530	SEC5E	* Compare under interrupt control Check cylinder register advance RC
0514	SEC5F	* Compare read and write buffers RSC RC Next iteration jump to SEC5D Repeat section

SECTION 6 READ, WRITE, COMPARE THROUGH CYLINDERS

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC6	Set section passcount
	SEC6A	Request interrupt Clear controller
	SEC6F	* Select interrupt
0616	SEC6B	Verify illegal address alarm interrupt Send illegal address (00FF)
0617	SEC6D	Verify address error status set
	SEC6C	RC Change to a second illegal address (FF00) If second disk not available, skip to SEC6M
	SEC6L	* Clear controller Set address to last sector in file Select interrupt
0620 0619	SEC6X	Write 97 word buffer off end of file Check address error status RC
0625	SEC6M	* Verify no compare circuits Write 97 word buffer Change 1 or 97 word on alternate passes Compare 97 word buffer
	SEC6N	RC

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC6NA	*	Move position to last sector in track Write 97 word buffer RC
0615	SEC6NB	*	Compare 97 word buffer RC
	SEC6NC	*	Read 97 word buffer RC
0614	SEC6NN		Compare read and write buffers RC Next iteration jump to SEC6F Repeat section

SECTION 7 SURFACE TEST

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC7		Set passcount Select appropriate buffer length per core availability Clear bad track table and set flag 2 to avoid selecting an alternate track
	SEC7H, A, C		Set up patterns to be used
	SEC7F		Request interrupt from SMM Clear controller
0730	SEC7X	*	Write a sector or track Verify cylinder register RC
	SEC7R1		Update one sector or track Jump back to SEC7X until file is complete When done, clear controller, prepare for read
0730	SEC7Y	*	Read a sector or track Verify cylinder register
071B	SEC7F		Compare data bit for bit RC

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC8G	* Write buffer of all zeros with last word a 0001 ₁₆ and verify a checkword of 80F ₁₆ RC
	SEC8H	* Same as above except last word of FFF ₁₆ and checkword 3A ₁₆ RC
	SEC8K	* Last word FFFF ₁₆ checkword of 3C6 ₁₆ RC
	SEC8L	* First word 0001 ₁₆ checkword of 55D ₁₆ RC
	SEC8LA	* 97th word 0001 ₁₆ checkword 2nd sector after zero padding 55D ₁₆ RC
	SEC8M	* All words of buffer floating one Checkword of 486 ₁₆ RC

SECTION 9 READ, WRITE, COMPARE, USING READY NOT BUSY INTERRUPT

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
		Same as Section 5 except interrupt on "Ready and Not Busy" is used

SECTION 10 WRITE ADDRESS TAGS

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC10	Initialize section Clear controller
	SEC10A	Load address
	SEC10B	* Write address tags Check alarm RC Advance track count Jump back to SEC10A until first disk complete

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
		Check for fixed disk - if present, jump to SEC10A RC Repeat section
SECTION 11 MAXIMUM TIME TO POSITION TEST		
<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC11	Set up random positions Convert to legal addresses Preset some addresses to high and low extreme Set time for correct computer (SC or 1704) Clear controller
	SEC11T1	* Initialize millisecond count and move one cylinder
	SEC11T0	Measure time till end of position Verify less than 8 milliseconds Check for end of file
0B37	S11T3	Report excessive time
	S11T4	Repeat condition to S11T1
	SEC11A	Move up new address Momentarily jump to monitor
0B1C	SC11D	* Position to new address Measure time to busy drop RC Next iteration to SC11A Repeat section

SECTION 12 AUTOLOAD CHECK

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC 12	Set section passcount to one Set disk to address 0

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	S12A	Move copy of program to buffer area Write 2784 ₁₀ location onto first track
	S12B	Wait for not busy Change one location in low core STOP - operator must press autoloader
0C1D	S12D	Compare autoloader data Repeat section (In case of multiple errors, set Stop/ Jump parameter bit 11)

SECTION 13 CHECKWORD CHECK OF ENTIRE SURFACE

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC13	Set section passcount to one Initialize first and last address Clear controller
	S13F	* Set attempt counter
0D31 0D32	S13A	Load address Execute checkword check Make 10 attempts if alarms set-Jump S13A RC Increment until end of disk jump to S13F Check if fixed disk present; if yes, jump to S13F RC Repeat section

SECTION 14 PROTECT CIRCUITS TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC14	Set passcount to one
0E29	SEC14G	* Set address to low range limit Protect one word in input buffer area Execute a read buffer Verify a protect fault

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
0E2A	SEC14A	Verify CWA is approximately at protect fault address Clear protect on one word previously protected RC
0E2B	SEC14B	* Verify reject on output command RC
0E2C	SEC14C	* Verify acceptance of input command even though not protected RC Clear PROTECT switches Protect entire program except half of input buffer Set device protect
	SEC14D	* Execute a read, write, compare, and check for no faults RC Clear PROTECT switches Unprotect entire program RC Next iteration jump to SEC14G Repeat section

SECTION 15 CROSSTRACK TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC15	Clear subroutine flag for write or compare Generate random addresses Convert to legal addresses Clear controller Set section passcount to 5 Set buffer output to all ones

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC15B	* Clear count Get 3 consecutive tracks alternately at high and then at low range limits Set number of random positions count Write first track with all one's Write 3rd track with all one's
0F34	SEC15A	Write random data on 2nd track Random position Return to SEC15A for 20 times Compare outer tracks for correct data RC Next iteration jump SEC15B Repeat section

C. SUB-PROGRAM DESCRIPTION

Some major programs (subroutines) are contained in this section and ordered alphanumerically by call name (that is, the entry address tag to the subroutine is the call name of the subprogram.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
XX21	ADPRINTP	Routine to position under interrupt control Select interrupt Position Wait for interrupt Check for errors during interrupt processing Check cylinder register status Exit
	ADSR	Routine to compute difference to get to a new address
XX12	BUSYPRES	Routine to wait for busy to drop and to return control to monitor as required
XX26	CBINTP	Routine to compare under interrupt control
	CDFA	Routine to compare true cylinder and cylinder register status

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	CLRCON	Clear controller routine Execute clear controller function Input director status Wait for on cylinder to drop, then wait for on cylinder to come back up Exit
XX27	CNFE	Routine to compare cylinder register sta- tus with a predicted value after an oper- ation
XX14	COMPARE	Compare write buffer with read buffer internally by computer
	CONALARM	Routine to check for EOP and for absence of all alarms
	CONV	Routine to convert random numbers to legal addresses
	CSCY	Compute expected cylinder status using buffer length for anticipated operation
XX23	CWACOMP	Add buffer length to FWA and check CWA after operation
	CWINTP	Execute checkword check under interrupt control
	IECHECK	Check for any errors during an interrupt
	INC	Routine will cause an increment of values to check bit positions in a 16 bit register
	INCREMENT	Routine to sequentially increment addresses by sector or by tracks (used in Section 7)
	INTPROC	Interrupt processor Stores Q Input status Output clear interrupt Input status Verify both statuses and set appropriate flags Store return address Load Q Exit

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	NEXTSECT	Routine to select sections of test
	READ	Position and read one sector under interrupt control
	ROUT 1	Routine to position. Enter routine with Q = to buffer length and A = to new address Store Q and A Check if address is in bad track table (except Section 7 which assigns new bad tracks) Checks for fixed disk and limit addresses as a result of presence or absence Executes ADSR routine Outputs buffer length Executes position Predict address after contemplated operation (CSCY) Exit
	ROUT 2	Routine to read, write, and compare Enter routine with A = FWA and Q = to function Store A in CWACOMP routine Execute operation Wait not busy Check alarms
XX27		Execute CNFE routine
XX26		Execute CDFA routine
XX23		Execute CWACOMP routine Exit
	WRITE	Position and write one sector under interrupt control

VI. APPLICATIONS

A. Suggestions for manufacturing test in the use of this diagnostic test:

An acquaintance with the SMM Reference Manual will enable an operator in better use of SMM tests to aid in resolution of errors and easy maintenance of device being tested.

If possible, a partial debug of controller should be made using the maintenance test panel that is available for this device. However, it is possible to run if clear controller and director status input functions have been debugged. A short, hand-punched program such as the following can be used.

E000		LDQ
0X00	or	OX01
0B00		NOP
02FE		INPUT
0000		STOP

Load SMM test number 78 Cartridge Disk Drive test (CDD). Set Stop/Jump parameter to 49₁₆. Select each test individually. Set range limits if applicable. Assure correct interrupt line is selected.

Attempt sections in following order:

Section 1

Section 10

Section 2 If error 33 occurs, abort test and continue until Section 4 is verified.

Section 3

Section 7 Run until first surface error, then abandon and go to Section 4. (This effectively puts data on entire surface of disk so as to avoid unrecoverable checkword check errors).

Section 4 If an error occurs, you may limit range to as little as one cylinder. By setting repeat condition at proper time and with range limit set to one cylinder, you can debug read, write, compare, or checkword check on only one cylinder. If repeat subsection is selected, you can do all four previously mentioned operations all on one cylinder.

NOTE

The advantage of doing an operation on one cylinder avoids unnecessary positioning time.

Sections 5 and 9 These two tests are similar to test 4 but using interrupt control.

The remaining sections can be run in any order.

B. Explanation of an error and an example of how to repeat an error.

Example of error typeout:

A	Q	A	Q	A	Q	A	Q
7848	0049	041E	017F	0009	C801	0000	0205
(IDENT)	(STOP/JUMP)	(SEC/ERR)	(RET.ADD)	VARIABLE		DATA(either 2 or 4 words)	

The first word of the error typeout is the identifier. The second word is the Stop/Jump parameter. The third word contains the section number and the error code. For example, 041E means Section 4 had an end of operation failure. That is, EOP status bit did not set as expected. The fifth word, according to the error explanation, is the director status. The sixth word is the cylinder address that the error occurred at. The seventh word is the status at the instant of an alarm. (Since no alarm is present, this status is not applicable.) The eighth word contains the function code of the last output that was attempted before the error.

At this point, several options are available to the operator:

1. Check if the error is repetitive. Set repeat condition and check for same error again. If error is the same and operator determines that debug will be attempted at this point, a disable typeout can also be set in Stop/Jump parameter and selective stop removed and test will cycle on error.
2. If operator is not sure of the operation being performed at the time of the error, he may want to look at the test description and determine what was being attempted. The operator should proceed as follows:

Go to Section 4 description and look for error code; if error code is not listed, it indicates that it was not the major test performed in this section. Then the operator should use the error information that tells the last function attempted and look for this function in the Section 4 description. The test description shows that a compare function is executed in Section 4E (0205 indicates compare function). By scanning the entire section description, the operator can determine the sequence of events being attempted and determine how many of these will be repeated when he selects repeat condition. A closer detailed observation of the section can be obtained by looking at the listing for this test.

In some types of errors, the fourth word of the typeout or return jump address can point directly to the section where the error occurred.

- C. Suggestions for running test for maintenance of a unit known to have been operating previously.

Load SMM test number 78 Cartridge Disk Drive test (CDD). Set Stop/Jump parameter to 49_{16} . If sectors containing bad surfaces are known, enter an A on fourth parameter stop. If bad areas are known, test would be initiated as follows:

At first stop, set Q = to Stop/Jump of 49_{16} . Hit run and at second stop leave A set to normally selected sections and check Q for correct range limits. Hit run and at third stop set A and Q to correct interrupt line. Hit run and at fourth stop set A = to track number of bad sector. Hit run and at stop enter next bad track address or clear to zero and run and test will execute. If address of bad sectors are unknown, test will have to be initiated as suggested for a manufacturing operation.

VII. PHYSICAL REQUIREMENTS

- A. STORAGE REQUIREMENTS - approximately 8K
- B. TIMING - N/A
- C. EQUIPMENT CONFIGURATION:
1. 17X4 Computer with 8K memory
 2. 1705 Interrupt Data Channel
 3. 1 Cartridge Disk Drive (1739/FV227)
 4. Device for loading SMM tests into computer

APPENDIX A

DICTIONARY OF TAG NAMES AND ABBREVIATIONS

<u>Name</u>	<u>Definition</u>
* (Asterisk)	See definition of RC.
Cylinder Register Status	This phrase refers to the contents of the register only and does not always indicate the head position (see true cylinder status).
True Cylinder Status	This status gives the actual cylinder address as read from the disk when a read, write, or compare operation is attempted (only upper eight bits are used).
CWA	Current word address.
Function Code	Refers to equipment code and director bits.
Difference	A 16 bit value consisting of eight lower bits which are absolute and eight upper bits indicating the number of cylinders forward or backward (as determined by bit 5) required to move in order to get to a new address.
RC	Repeat condition, if selected go back to statement marked *.
EOP	End of operation.
DSA	Direct storage access.
FWA	First word address.
Position	Execute a load address difference function to get to a new address.
Range	Selectable parameter entry which limits the area to be written on cartridge portion of drive only.
Compare	Defined by the type of error received. An error with a 14 code indicates an internal compare of read and write data by a computer. A 15 code indicates an error detected when a compare function was executed.
Bad Track	Entire track of 29 sectors labeled as bad by software when any sector or portion of the track will not verify all data checks.
#	See RSC.
RSC	Repeat subsection, if selected go back to statement marked #.

APPENDIX B

FUNCTION CODES

<u>Dir Bits Q Register</u>	<u>Output From A</u>	<u>Input to A</u>
0	Load buffer length	Clear controller
1	Director function	Director status
2	Cylinder register status	Load address difference
3	Write	CWA status
4	Read	Checkword status
5	Compare	True cylinder status
6	Checkword check	
7	Write address tag	

DIRECTOR STATUS

XXX1 - Ready	X1XX - Checkword error
XXX2 - Busy	X2XX - Lost data
XXX4 - Interrupt	X4XX - Address error
XXX8 - On cylinder	X8XX - Seek error (cont)
XX1X - EOP	1XXX - Not used
XX2X - Alarm	2XXX - Storage parity
XX4X - No compare	4XXX - Protect fault
XX8X - Protected	8XXX - Seek error (drive)

DIRECTOR FUNCTIONS

XXX2 - Clear Interrupt
XXX4 - Next Ready and Not Busy Interrupt Request
XXX8 - EOP Interrupt Request
XX1X - Alarm Interrupt Request

BG504A/H DRUM CONTROLLER DIAGNOSTIC
(DRMP80 Test No. 80)

I. IDENTIFICATION

Test - BG504A/H Drum Controller Test
Number - 80
Mnemonic - DRM

II. RESTRICTIONS

Bit 8 of SMM control word must be set at load time to select MBS.

III. DESCRIPTION AND OPERATION

A. SCOPE

1. This specification describes the BG504A/H Drum Controller diagnostic. It will operate under the control of SMM17 V3.0 or above and has been assigned Test No. 80 in the SMM17 library list. The purpose of this specification is to describe the comprehensive set of test sections for both factory checkout and field maintenance.

B. APPLICABLE DOCUMENTS

1. Software
 - a. 1500/VW SMM17 Software Subset of SMM17 V3.0
 - b. SMM17 Manual Pub. No. 60182000
 - c. MBS subset of SMM17 V3.0 ERS
2. Hardware
 - a. 1700 Reference Manual Pub. No. 60153100
 - b. SC-1700 Reference Manual Pub. No. 60270600
 - c. BG504 Drum Subsystem Pub. No. 39731700

C. DESCRIPTION

1. Communication

Communication with the diagnostic will be through either console or teletype. Refer to latest SMM17 manual for loading information.

2. General Test Description

- a. The following areas will be tested:
 - 1) Functions
 - 2) Status
 - 3) Interrupts
 - 4) Data
 - 5) Alarms
- b. The method of testing is to make each succeeding test section more complex, forming a bootstrapping-sequential technique aimed at reducing troubleshooting time. For example:
 - 1) Sector, initial core, and final core address registers will be verified prior to drum transfers.
 - 2) All controller data registers will be verified prior to checking drum transfers.
- c. The type of response (reply or reject) to all I/O instructions, except when reading status, will be verified against predicted values. This will include timer information to the nearest millisecond. For example, the controller may be busy, external reject, up to 17 milliseconds after initiating a Write operation. The actual checking is performed in the monitor; the test supplies the data.
- d. All four status words are copied after each function, read or write. The only exception is Section 2 where only director and sector address status is copied. Although four status words are copied, only those applicable to the I/O operation will be verified.
- e. To verify all eight alarm conditions, it will be necessary to "bug" specific logic areas. To achieve this, a card extender and clip lead are required. Although this procedure is primarily used by QA, it can be helpful both in checkout and in the field.
- f. Preset Input Parameters

	A	Q
Stop 1	8051	020D
Stop 2	04DE	0200
Stop 3	4500	0000
Stop 4	0000	0000
Stop 5	5A5A	8060

1) Refer to the latest edition of the SMM17 Reference Manual for an explanation of Stop 1.

2) Stop 2

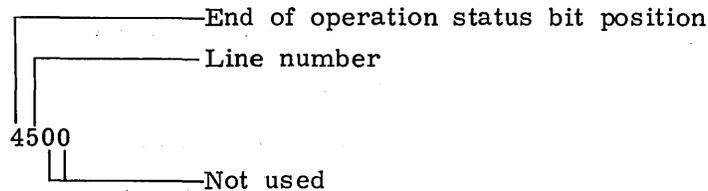
(A)	<u>Bit</u>	<u>Sections</u>
	0	Bit clock adjust procedure/buffer addresses
	1	Sector address counter
	2	Initial sector address register/sector address compare
	3	Initial and final core address/core address compare
	4	Sector overrange/data registers
	5	Guarded address
	6	Serialize test
	7	Worst case patterns
	8	CE section (manipulative)
	9	Auto load/protect
	10	Checkword check
	11	Clear timing error
	12	Not used
	13	Not used
	14	ON = 50 Hz, OFF = 60 Hz
	15	Indicates the maintenance bell troubleshooting aid. If set, the teletype bell will be rung prior to each error message. It is to be used in conjunction with the omit typeouts and repeat conditions featured as an aid to isolating intermittent errors.
(Q)		Number of tracks (drum size). Bit 06=64 tracks, bit 07=128 tracks, etc.

3) Stop 3

(A) Interrupt data in the form BLBL.

B = Bit position in director status

L = Line number



(Q) = 0

4) Stop 4

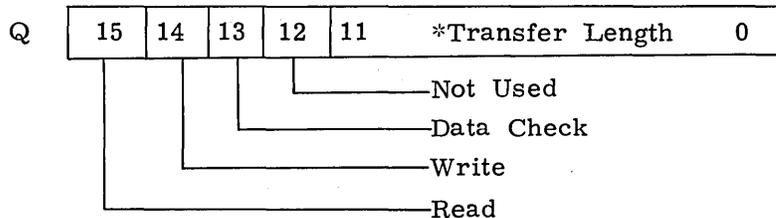
(A) Bits 0-14 = first available track/sector address

(Q) = Highest guarded track address

5) Stop 5

(A) Section 4, 8 data pattern

(Q) Section 8 control



*Transfer length: Max. = 3072 (1 track)

Min. = 1 word

3. I/O CYCLE

a. The I/O cycle is a collection of monitor calls, common to all test sections.

All I/O requests to the monitor including status, function output, read, write, status, and interrupt timing are grouped in a specific order and located near the beginning of the test. It is called as a subroutine with the name tag "IOCYL".

All function requests result in an "early I/O cycle exit". Requests for data transfers complete the I/O cycle (see flow chart).

b. The following monitor calls are used in the I/O cycle.

<u>Monitor Subroutine</u>	<u>Description</u>	<u>I/O Cycle Pointer No.</u>	<u>Monitor Error No. (s)</u>
Check Status	Copy and check requested number of status words against predicted values.	X0	0003
Function	Output values to load ICA, FCA, and ISA registers. Begin copying status 60 microseconds after output. Reply to output instruction is verified against the predicted reply. External reject (if any) timing is checked. Maximum time to wait is 32,767 milliseconds.	X1	0001, 0002
Read/Write	Initiate Read or Write operation. Response and timing same as function. Begin copying status approx. 100 microseconds after output.	X6/X7	0001, 0002
Recheck	Verify last status(es) copied against predicted values.	X2	0003
Recognize Interrupt	Copy and check all requested status while waiting for an interrupt. Control is passed to the monitor while waiting.	X3	0003, 0004
Monitor Status	Copy and check all requested status while waiting for a specific status bit to change state within a specified time. The last status(es) copied which saw the bit change is not verified.	X4	0000, 0003
Recheck	Same as above.	X5	0003
Select Interrupt	Makes the occurrence of an interrupt legal to the monitor.	NONE	NONE
Deselect Interrupt	Makes the occurrence of an interrupt illegal.	NONE	NONE

c. Interrupt Processor

The interrupt processor, like the test sections, uses the I/O cycle to acknowledge interrupts. The I/O cycle pointer no. for Check Status, function and (1st) Recheck Status is changed to X8, X9, and XA respectively. Error messages are shorter for acknowledge interrupt because only the first two status words are copied.

Alarm interrupt results in the following:

1. Clear controller.
2. Enable or disable end of operation and/or alarm interrupt as requested by the test section.
3. Deselect the line to the monitor thereby making the occurrence of an interrupt illegal. The line is reselected prior to the next request for a data transfer.

End of operation interrupt results in 2 and 3 of the above.

4. Initialize

- a. A task of the section search routine, located at the beginning of the test, is to initialize each section prior to passing control to that section.

Initialize performs the following sequence of operations:

- 1) Adjust timing values if connected to 50 Hz power.
- 2) Clear all status calls (except last recheck status) in the I/O cycle.
- 3) I/O cycle switches:
 - a) Set early exit
 - b) Set function
 - c) Clear interrupt
- 4) Set error code to zero (SSEE).
- 5) Direct monitor to copy status 1 and 2 only. See F for status description.
- 6) Set first recheck status, status 1 value to expect ready and data.
- 7) Execute clear controller.
- 8) Direct monitor to copy all four status words.
- 9) Set check status, status 1 value to expect ready and data.
- 10) Return to section search routine.

5. Error detection reporting

a. The test uses six monitor subroutines to perform the following operations.

- 1) Execute I/O
 - a) Read
 - b) Write
 - c) Function
- 2) Process interrupts
- 3) Copy status
- 4) Check status
- 5) Monitor status
- 6) Detect errors

The test calls these subroutines from a common area near the front of the test. The sequence of calls is referred to as the "I/O Cycle" (see the I/O cycle flow chart). The monitor supplies the error type number for all monitor detected errors.

NOTE

Data errors are reported by the test.

The I/O cycle position pointer and test section pointer are supplied in each message.

b. Generalized Error Format:

A1	Q1	A2	Q2
XXY8	S/J	SSE ₁ E ₂	RTN ADDR

XX - Test no.

Y - No. of A/Q pairs

8 - Error message

S/J - Stop/Jump parameter

Stops

Bit 0	Stop 1	Stop to enter test parameters
Bit 1	Stop 2	Stop at end of test section
Bit 2	Stop 4	Stop at end of test
Bit 3	Stop 8	Stop on error

Jumps

Bit 4	Repeat conditions
Bit 5	Repeat test section
Bit 6	Repeat test
Bit 7	Build test list
Bit 8	Omit typeouts
Bit 9	Display memory address in stops
Bit 10	Re-enter test parameters
Bits 11-15	Not used

SS -	Section no.
E ₁ -	Section position pointer
E ₂ -	I/O cycle position pointer

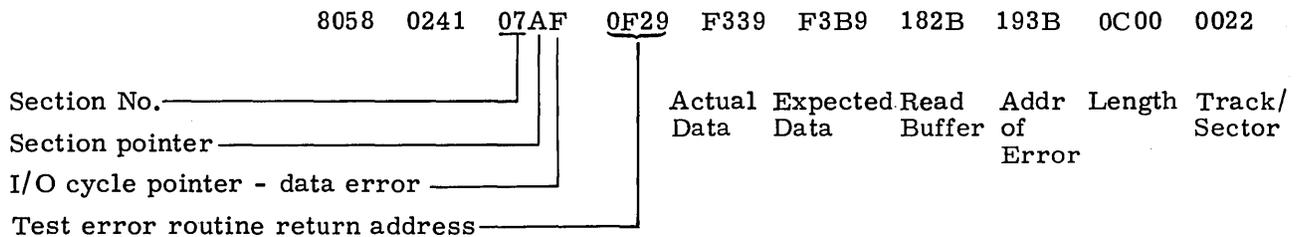
c. RTN ADDR - Memory location of error routine

DATA ERRORS - A dummy I/O cycle pointer (XXXF) is used for data errors.

For all data errors the information following the generalized error format will be as follows:

A3	Q3	A4	Q4	A5	Q5
Actual	Expected	Read buffer address	Error address	Transfer length attempted	This track address

1) Data Error Example:



The error indicates bit 07 was dropped in track 1 sector 2. The transfer length attempted was 3072 words or one complete track.

d. Monitor Detected Errors

For monitor detected errors, the I/O cycle pointer will be X0 -- XA; numbers X8 -- XA are used for the interrupt processor. The message following the generalized error format will be in two parts.

Part 1

A3	Q3	A4	Q4
Monitor error Number	LORR	Last Operation (A)	Last Operation (Q)

1) Monitor Error No.

- 0000 *Busy status bit did not change state within specified time (status time out), two revolutions.
- 0001 *I/O time out. External reject to output instruction for a period longer than specified.
- 0002 I/O response error. Reply to output instruction was other than predicted.
- 0003 Status error. Actual did not equal expected.
- 0004 *Interrupt time out. Interrupt did not occur within specified time.

2) LO = Last Operation Performed

- 10 = Write
- 20 = Read
- 30 = Function

a. RR = Response to Last Operation Output Instruction

- 10 = Reply
- 20 = External reject
- 30 = Internal reject

- 3) Last Operation (A) = Contents of the A register for last operation.
- 4) Last Operation (Q) = Contents of the Q register for last operation.

*Time is measured to the nearest millisecond.

Part 2

<u>Monitor Error No.</u>	<u>A5</u>	<u>Q5</u>	<u>A6</u>	<u>Q6</u>	<u>A7</u>	<u>Q7</u>
00	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time (msec)	*Status control Word
01	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time (msec)	0000 (not used)
02	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4		
03	Actual Status 1	Expected Status 1	Actual Status 2	Expected Status 2	Actual Status 3	Expected Status 3
	Actual Status 4	Expected Status 4				
04	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time (msec)	Mask Register

Expected 0000 (not used)
int. line one hex character per line.

Status 1 = Director status (ST 1) Status 3 = Memory address (ST 3)
Status 2 = Sector address (ST 2) Status 4 = Last data word (ST 4)
See F for complete status description.

*Status control word = 0CBS

0 = Not used

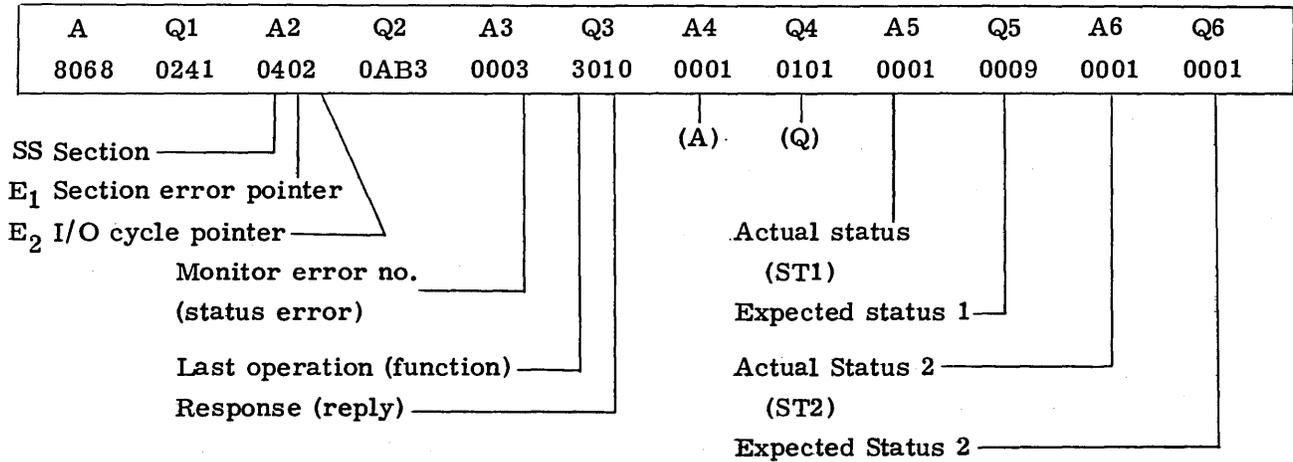
C = Condition; 1 = Wait for status bit to go "off"

0 = Wait for status bit to go "on"

B = Bit position in status word

S = Status word (0-3)

e. Monitor Error Example



This error indicates that the data status (bit 03) is missing from ST1 after a clear controller to equipment no. 2. The section error pointer (E₁) indicates the function was issued from the initialize routine. The I/O cycle pointer (E₂) indicates the error was detected in the first re-check status subroutine which verifies the status copied after issuing the clear controller function (see Drum I/O Cycle Flow Chart attached).

Note the actual and expected values for ST2 (A6, Q6) are equal. Although the status error is in ST1, the error message will contain actual and expected values for all status words copied as a diagnostic aid.

f. Refer to test section for section error codes.

NOTE

If the error was the result of an alarm condition, the test will issue a clear controller function before continuing. A two-drum revolution delay will result for timing track errors to ensure controller will be not busy.

D. TEST SECTIONS

1. Section 0

a. Controller Clock Adjustment/Buffer Addresses

This section does not require the computer for I/O. Its purpose is to instruct personnel in adjusting the controller clock to be in sync with the bit clock on the drum. The bit clock is approximately 342 nanoseconds for a 60 Hz drum and 400 nanoseconds for a 50 Hz drum.

- b. The following message will be output:

CONTROLLER CLOCK ADJ *=TEST POINT

1. SYNC (+) CARD A26*1
2. ADJUST ZERO GOING CLOCK A26* 4+/-5 NSEC.
3. ALL MEASUREMENTS REF. AT +1.5V.

READ BUFFER = YYYY

WRITE BUFFER = ZZZZ

- c. The clock should be adjusted every 6 months or whenever the drum is replaced.

2. Section 1

- a. Sector Address Counter

- b. The purpose of this section is to verify the sector address counter. The diagnostic will test for the following conditions:

- 1) A bit "stuck" on
- 2) A bit "stuck" off
- 3) An intermittent bit

Either of the above conditions would cause addressing errors, resulting in potential catastrophic failures.

- c. To accomplish this, the sector address register status is read at approximately 40 Hz rate for 17 milliseconds, or one revolution, and the status stored in a continuous 850 word buffer. The data is then examined for proper incrementing. To scope this section, set bits 5, 8 in the SMM Stop/Jump word. Bit 05 sets repeat section; bit 08 omits the typeout.
- d. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Read sector address status for one revolution.	0 11X
2. Check for data = all zeros.	0 12X
3. Verify the incremented sector addresses.	0 13X

3. Section 2

- a. Initial Sector Address Register/Sector Address Compare
- b. This section will verify the Initial Sector Address (ISA) register and Sector Address Compare logic using all 32 sectors. The ISA will be preloaded at zero. The sector address compare bit and sector address status will be monitored to see that a complete revolution does not occur without sensing sector compare. After detecting sector address compare, the sector address status will be verified. This will check for improper loading of the ISA register.
- c. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Load ISA register (first time = zero).	021X
2. Wait for sector address compare, verify sector address status.	022X
3. Increment sector address and repeat steps 1 and 2. Exit after last sector.	

4. Section 3

- a. Initial Core/Final Core Address/Core Address Compare
- b. This section will verify the loading of the initial/final core address registers and the address compare logic. This test does not require DSA transfers, therefore the incrementing logic will be checked in another section. The method is as follows:
 - 1) Load initial and final address registers to zero, verify compare and core address status.
 - 2) The final address register bit 00 is set and no compare verified.
 - 3) The initial address register bit 00 is set and compare status verified.
 - 4) The procedure is repeated with bits 00 and 01. After each pass the next significant bit is added until all the bits are verified.

A sliding ones/zeros and random pattern will then be used to determine if there is interaction on the A-write lines.

- c. Improper loading of the initial core address register will be verified by the final core address status. Since the same register is used for both operations, this will be a quick check.
- d. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Set first pattern	
2. Load ICA register, do not expect core address compare.	031X
3. Load FCA register with pattern from step 2, expect core address compare status.	032X
4. Shift pattern one place and repeat from step 2. After 16 shifts get next word type and repeat from step 2. There are four word types.	

5. Section 4

- a. Sector Overrange/Drum Data Register
- b. The purpose of this section is to verify the sector overrange logic and the three data registers between DSA and the drum. The section will perform a drum write using the data pattern from the fifth parameter stop (see f).
- c. To verify sector overrange (SOR) an attempt is made to write into the first non-existent sector as determined from the second parameter stop (see f). Refer to Table 1 for SOR jumper assignment.
- d. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Load ICA with write buffer address.	041X
2. Load FCA with write buffer address (ICA).	042X
3. Load ISA with illegal address.	043X
4. Enable alarm interrupt if requested.	044X
5. Attempt a one-word write on first non-existent sector.	045X
6. Clear controller if interrupts not selected.	046X
7. Enable end of operation interrupt.	047X
8. Load last good ISA value.	048X
9. Initiate a one-word write on last sector.	049X

The data registers located on cards A06-A07 are checked. DSA control for drum write is checked on card A11. Drum write control on A12 is checked except for checkword generation and transfer of write data to the drum.

TABLE 1. CARD POSITION A16

No. of Tracks	SOR Jumper Position			
	3-4	5-6	7-8	9-10
64	0	0	0	0
128	0	0	0	1
192	0	0	1	0
256	0	0	1	1
320	0	1	0	0
384	0	1	0	1
448	0	1	1	0
512	0	1	1	1
576	1	0	0	0
640	1	0	0	1
704	1	0	1	0
768	1	0	1	1
832	1	1	0	0
896	1	1	0	1
960	1	1	1	0
1024	1	1	1	1

6. Section 5

- a. Guarded Address
- b. The purpose of this section is to verify the guarded address logic and the Enable Guarded Address switch. A message will be output to set the switch.
- c. The highest guarded address parameter (see f) determines which track will be used (sector 0) to verify the illegal write. Refer to Table 2 for track address jumper assignment.

- d. After reading from the guarded sector, the section attempts a write to the same address. The error is verified and a one-sector write on the last track, sector 0 is performed. The Guarded Address switch is reset and the previously guarded sector is written using the same data.
- e. Interrupts are not required for this section.
- f. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Output message to set Guarded Address switch.	
2. Load ICA register with address of read buffer.	051X
3. Load FCA register with address of read buffer +95.	052X
4. Load ISA registers with highest guarded track, sector zero.	053X
5. Initiate Read operation	054X
6. Load ICA register with address of read buffer.	055X
7. Initiate Write operation on guarded track, sector zero. Expect error.	056X
8. Clear controller	057X
9. Load ISA register with last track address, sector zero.	058X
10. Initiate Write operation on last track, sector zero.	059X
11. Load ISA register with highest guarded address, sector zero.	05AX
12. Load ICA register with address of read buffer.	05BX

<u>Operation</u>	<u>Section Error Pointer</u>
13. Output message to clear Guarded Address switch.	
14. Initiate Write operation on a guarded sector using the same data (see step 7) to preserve the guarded sector.	05CX

TABLE 2. CARD SLOT A-16

Jumper Address		Highest Guarded Track
31	32	128
33	34	64
35	36	32
37	38	16
39	40	8
41	42	4
43	44	2
45	46	1
NOTE: No jumper = track 0		

7. Section 6

a. Surface Address Test

- b. The purpose of this section is to verify the address logic from the controller to the drum surface. The serialize method is used to write each sector with its own address. For 512 tracks, the data would appear on the drum as follows:

<u>Track</u>	<u>Sector</u>	<u>Word 0</u>	<u>Word 1</u>				<u>Word 95</u>
0	0	0000	0000	—	—	—	0000
0	1	0001	0001	—	—	—	0001
1	0	0020	0020	—	—	—	0020
1	10	002A	002A	—	—	—	002A
511	0	3FE0	3FE0	—	—	—	3FE0
511	31	3FFF	3FFF	—	—	—	3FFF

- c. The entire drum surface, or that area specified by the input parameters (see f) is also data checked. After serializing is complete, the sector address is reset to the first track, then read and compared to predicted values for that track. This procedure is repeated until all tracks have been verified.
- d. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Enable end of operation interrupt if requested.	061X
2. Load final core address register.	062X
3. Load initial core address register.	063X
4. Load initial sector address register.	064X
5. Set up write buffer (1 track).	
6. Write 1 track.	065X
7. Repeat from step 3 until all tracks written.	
8. Load final core address register.	066X

<u>Operation</u>	<u>Error Section Pointer</u>
9. Load initial core address register.	067X
10. Load initial core address register.	068X
11. Generate first (next) track in write buffer.	
12. Read 1 track.	069X
13. Compare read and write buffers.	06AF
14. Repeat from step 9 until last track read and checked.	

8. Section 7

a. Worst Case Patterns

b. The purpose of this section is first, to test the drum surface for bad spots and second, to test the head assembly and drum electronics for rate sensitivity problems. Each track is written with the same data which contains 37 sets of data. Except for one, each set is 83 words in length. See Table 3.

TABLE 3

Data	Length	Description
Random	83	Random
Sliding zeros	83 x 16	Each of 16 patterns is 83 words
Sliding ones	83 x 16	Each of 16 patterns is 83 words
1010101010	83	Maximum rate change
110011001100	83	50.0% max.
000111000111	84	33.3% max.
000011110000	83	25.0% max.
	<hr style="width: 20%; margin: 0 auto;"/> 3072 Total	

c. The following sequence is performed.

	<u>Operation</u>	<u>Section Error Pointer</u>
1.	Enable end of operation interrupt if requested.	071X
2.	Load final core address register.	072X
3.	Load initial core address register.	073X
4.	Load initial sector address register.	074X
5.	Write 1 track.	075X
6.	Load final core address register.	076X
7.	Load initial core address register.	077X
8.	Load initial sector address register.	078X
9.	Read 1 track.	079X
10.	Verify the data.	07AF
11.	If last track verified, exit. If not, increment the track address and go to step 2.	

9. Section 8

a. Maintenance

b. The purpose of this section is to allow the operator to design a mini diagnostic which operates under I/O cycle control. The following modes are available as defined in 5).

Operating Mode

1. Write only
 2. Read only
 3. Write, read
 4. Write, read, and data check
 5. Read only, data check
- c. Data transfers may be made with or without interrupts as determined by Stop 3. See 3).
- d. The initial track/sector address is entered via Stop 4. See 4). For example, track 4 sector 12 = 008C.
- e. The transfer length is entered concurrent with the operating mode.
- f. The data pattern to be written is entered via Stop 5. See 2).
- g. This section is designed to loop indefinitely. The method used to stop execution and redefine the operating conditions is as follows:
- 1) Set the skip key.
A = SMM ID word Q = S/J
 - 2) Set bit 10 in the Stop/Jump word. This is a request to stop to re-enter parameters.
 - 3) Hit run; the second SMM stop is displayed.
 - 4) Hit run again; the test will stop for parameter entry. Remove bit 10 from the Stop/Jump word and make parameter changes.
- The skip key is checked a maximum of six times in the I/O cycle and once in the monitor. Therefore, it's possible to repeat step 1 seven times (worst case) before reaching the re-enter parameter stop.
- h. This section should be used as a diagnostic aid in troubleshooting specific problem areas. A high degree of sync control for scoping is available through the length of transfer and initial sector address value parameters.
- i. The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Enable end of operation interrupt if requested.	081X
2. Load final core address based on length parameter.	082X
3. Load initial core address register.	083X
4. Load initial sector address based on parameter data.	084X
5. Write, length based on parameter data.	085X
6. Repeat steps 1 - 6 for write only. Continue to step 7 for read.	
7. Load final core address based on length parameter.	086X
8. Load initial core address register.	087X
9. Load initial sector address value from step 4.	088X
10. Read, length based on parameter data.	089X
11. Verify data if requested, if not go to step 1.	08AF

Step 1 also checks the skip key to determine if a stop to re-enter parameter has been requested.

10. Section 9

- a. Autoload and Program Protect
- b. This section is in two parts. Part 1 verifies the autoload logic and part 2 checks the protect logic.

- 1) Part 1 is checked by saving the autoloading image (1536 words) in the write buffer, writing the autoloading area, clearing core from 0 - 5FF, initiating an autoloading and comparing the data to the write buffer. If an error is detected, the write buffer image is returned to low core and the data error reported. Note the actual error is destroyed.
- 2) Part 2 verifies both the controller and computer protect fault logic. The conditions stated in Table 4 are checked for the proper response. Interrupts are disabled during the protect section.

TABLE 4.

Controller PP Switch	I/O PP Bit	Controller Response
1	1	Reply
1	0	Ext. Reject
0	1	Reply
0	0	Reply

c. To verify controller protect fault, a read drum is initiated under the following conditions.

- 1) Read buffer, length = 1536 words, is protected.
- 2) Drum PROTECT switch is off.
- 3) CPU PROTECT switch is on.
- 4) Output instruction is not protected.

After processing the protect fault, the read buffer is checked to ensure no DSA transfers had taken place. If a data error is detected, the following message is added to the normal data error:

CPU SHOULD NOT HAVE ACCEPTED DSA
DATA DURING FORCED PROTECT FAULT.

d. It is possible for the controller to write, under protected conditions, to the CPU and not detect a protect fault. An example is as follows.

- 1) Read buffer protected.
- 2) Output instruction protected.
- 3) CPU PROTECT switch on.

A faulty DSA transmitter for bit 17 (protect) would indicate to the CPU that the output instruction was not protected and would not write into memory. The CPU sends the DSA protect fault signal but it is not sensed in the controller. The problem could be a bad cable, receiver, or another DSA device holding down bit 17.

e. The missed protect fault is checked as follows:

- 1) Generate random data in read buffer.
- 2) Generate same data in write buffer.
- 3) Read autoload area under protected conditions (d).
- 4) Compare read/write buffers, expect no compare.
- 5) Print the following message after compare:

```
DSA PROTECT FAULT NOT  
DETECTED BY CONTROLLER  
P = XXXX
```

The following sequence is performed.

	<u>Operation</u>	<u>Section Error Pointer</u>
1.	Enable end of operation interrupt if requested.	091X
2.	Load FCA register = WRBUF+1535.	092X
3.	Load ICA register = WRBUF.	093X
4.	Load ISA register = track 0, sector 0.	094X
5.	Write autoload area.	095X

	<u>Operation</u>	<u>Section Error Pointer</u>
6.	Print autoloading message. clear core from 0-5FF, wait 10 seconds.	
7.	Verify the data.	096F
8.	Print message to set drum and console PROTECT switches.	
9.	Load FCA register = RDBUF+1535 (autoloading area).	097X
10.	Load ICA register = RDBUF.	098X
11.	Fill read and write buffers with same data.	
12.	Initiate read, expect external reject.	099X
13.	Print message to clear drum PROTECT switch. Protect read buffer.	
14.	Initiate read, expect protect fault. Verify memory address status = RDBUF+1.	09AX
15.	Clear controller.	09BX
16.	Check read buffer data to verify no DSA transfers. A special message is added to the normal data error.	09AF
17.	Load ICA register = RDBUF.	09CX
18.	Read 16 sectors beginning track 0, sector 0. Output instruction is protected.	09DX

<u>Operation</u>	<u>Section Error Pointer</u>
19. Check data determine if protect fault occurred. If yes, print special message.	
20. Clear read buffer protect bits.	
21. Print clear CPU PROTECT switch message.	

11. Section 10

a. Checkword check

- 1) This section should be run to check the drum surface when the customer will not allow writing on the drum.
- 2) That portion of the drum surface as defined to the test during parameter input time, is read a track at a time. The data is stored in the read buffer but not checked. Status is checked before, during, and after each operation.
- 3) For 60 Hz power timing is approximately 30 tracks per second.
- 4) The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Enable end of operation interrupt if requested.	0A1X
2. Load FCA register.	0A2X
3. Load ICA register.	0A3X
4. Load ISA register.	0A4X
5. Initiate Read operation.	0A5X
6. Check for last track. If not last, increment track address and repeat from step 3. If last, exit.	

12. Section 11

a. Clear timing error

- 1) This section verifies that a clear controller function issued after sensing a timing error interrupt will result in a timing error cleared interrupt.
- 2) The interrupt line must be connected in order to execute this section.
- 3) The following sequence is performed.

<u>Operation</u>	<u>Section Error Pointer</u>
1. Print the generate timing error message: MOMENTARILY GND A14*2.	
2. Enable alarm interrupt.	0B1X
3. Output a dummy function to enable I/O cycle to select interrupts then wait for clear timing error interrupt.	0B2X

- 4) A 1 second delay after sensing the timing error prevents multiple interrupts.

E. SPECIAL TESTS

1. Checkword Check

- a. The checkword will be held in ST4 (status word 4) when test point All *26 is grounded. Four unique checkwords will be verified using Section 8 to control the number of words written on the drum.
- b. Set the stop on error bit (03) in the Stop/Jump word. Set up Section 8, see 5), to perform a write and read only using the values in Table 5. Ground test point A11*26. Start test and observe the error. The actual value for ST4 should contain the checkword as described in Table 5.

Repeat for all four conditions.

TABLE 5.

No.	No. of Words	Data	Checksum (ST4*)	
1	96	0000	0000	0001
2	96	5555	FFEA	FFEB
3	96	AAAA	002A	002B
4	96	FFFF	FFC0	FFC1

F. STATUS DESCRIPTION

	<u>Status 1 (ST 1)</u>	<u>Director Status</u>
A0	Ready **	
A1	Busy	
A2	Interrupt	
A3	Data (Ready not busy)	
A4	End of operation	
A5	Alarm	
A6	Lost data **	
A7	Protected	
A8	Checksum error **	
A9	Protect fault **	
A10	Guarded address enable	
A11	Timing track error **	
A12	Power failure **	
A13	Sector address compare	
A14	Guarded address error **	
A15	Sector overrange **	
	<u>Status 2 (ST 2)</u>	<u>Sector Address Status</u>
A0-A4	Sector	
A5-A14	Track	
A15	Core address compare	

*Status in either column is good. The LSB is actually the MSB of the first word of the next sector.

**Generates alarm.

Status 3 (ST 3)

A0-A15 Core address

Core Address Status

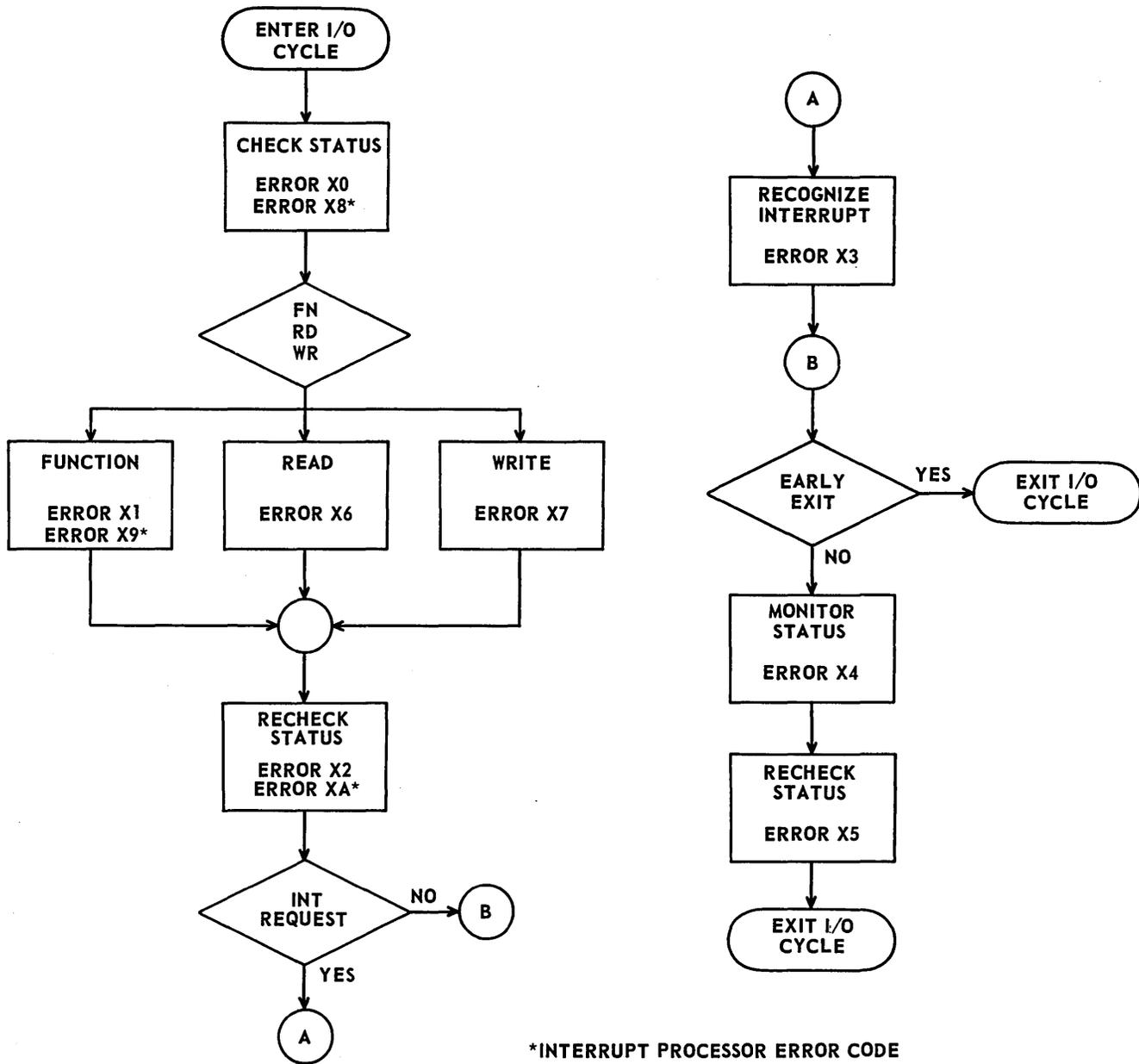
Status 4 (ST4)

A0-15 Last drum data word

Last Data Status

G. FUNCTIONAL DESCRIPTIONS

<u>Q3</u>	<u>Q2</u>	<u>Q1</u>	<u>Q0</u>	<u>Function</u>
0	0	0	0	Write
0	0	0	1	A0 Clear Controller
				A1 Disable/Clear Interrupt
				A3 Enable EOP Interrupt
				A4 Enable Alarm Interrupt
0	1	0	0	Read
1	0	0	0	Load initial sector address
1	1	0	0	Load initial core address
1	1	1	0	Load final core address



DRUM I/O CYCLE

1738 DISK QUICK LOOK TEST
(DP5P84 Test No. 84)

I. OPERATING INSTRUCTIONS

A. RESTRICTIONS

1. This is a one section test; therefore, there is no sections parameter.
2. Do not select Read and Write buffers and transfer length that could destroy either the monitor or test(s).

B. LOADING PROCEDURE

1. Called as external test under SMM17 V3.0 or above.
2. This test uses the MBS control package in V3.0; therefore, bit 08 must be set in the SMM control word after Quick Look executes.

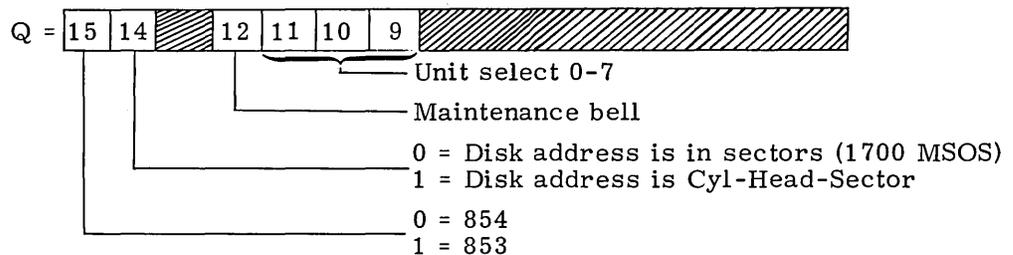
C. PARAMETERS

If bit 00 of the SMM Stop/Jump parameter is set at the start of the test, a parameter stop occurs.

<u>Stops</u>	<u>A</u>	<u>Q</u>
1	8451	SJ
2	P 035B	P 035B
3	P 095C	0600
4	0000	0000
5	4400	0000

Stops

- 1 A = ID
Q = Stop/Jump
- 2 A = First available location after test
Q = FWA-1 Write buffer
- 3 A = FWA-1 Read buffer
Q = Maximum transfer length
- 4 A = First available disk address



Stop

- 5 A = Interrupt data - BLBL (status bit-line no., status bit-line no.)
 See supplement E. II-D-3 for detailed explanation. A=0 to run without interrupts.

 Q = 0

D. MESSAGES

No message will occur if bit 08 of the Stop/Jump word is set.

1. Test title and initial address typeout:

1738 QUICK LOOK TEST 84
IA = XXXX

XXXX is the initial address of the test.

2. Parameter list type out after last stop:

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
8451	S/J	XXXX	YYYY	ZZZZ	0600	0000	4000	4400	0000

(See Stops)

3. End of 1738 Test:

A1	Q1	A2	Q2	A3	Q3
8434	S/J	Pass No.	Return Address	Error Count	0000

4. Error Messages

All error messages are in the format specified by SMM17.

A1	Q1	A2	Q2
84X8	S/J	00YY	Return Address

X = Number of pairs of words to be typed
YY = Error code

Additional information is given depending on the error type.

E. ERROR STOPS

1. The test reports two types of errors.

- a. MBS Detected Errors

All MBS detected errors must be decoded based on the A3 error stop which will contain a number 0000 - 0004. The most often reported error is 0003 (status error).

Section/
Error Code

Application

000A	Verify ready, on cylinder, and EOP for no interrupts; ready and on cylinder after interrupt processing. Verify cylinder address status.				
000B	Load same address used for write.				
000C	If selected, wait 1 millisecond for interrupt. Verify ready and busy while waiting.				
000D	Wait 100 milliseconds for busy to drop. Verify ready and busy while waiting.				
000E	Interrupts; verify ready and on cylinder. No interrupts; verify ready, on cylinder, and EOP. Verify cylinder address status.				
000F	Read random length, random data record.				
0010	If selected, wait 200 milliseconds for the interrupt. Verify ready and busy while waiting.				
0011	Wait 200 milliseconds for busy to drop. Verify ready and busy while waiting.				
0012	Interrupts; verify ready and on cylinder. No interrupts; verify ready, on cylinder, and EOP. Verify cylinder address status.				
0013	Data error.				
A3	Q3	A4	Q4	A5	Q5
Actual	Expected	Compare Address	Error Address	Transfer Length	Last Address Output
** Interrupt Processor **					
0014	Verify status after interrupt. After load address verify ready, interrupt, and EOP. Ignore cylinder address status. After data transfer verify ready, interrupt, on cylinder, and EOP. Verify cylinder address status.				
0015	Reselect unit, enable interrupts.				
0016	After load address verify ready status only. Ignore cylinder address status. After data transfer verify ready and on cylinder. Verify cylinder address status.				

II. DESCRIPTION

A. PROGRAM DESCRIPTION

This test is designed to be a quick check of the controller and drive through the use of random data, transfer length, and drive positioning. Test parameters allow the user to place the Read and Write buffers anywhere in unused memory. They are preset to follow the test. The number of words transferred will be between 1 and the maximum length as described in the test parameters. The data will be random.

To simulate 1700 MSOS protected operation, reset the SLS key and set the PROTECT key. The protect option may be turned on and off while the test is running.

B. BASIC PROGRAM FLOW

1. Load random address.
2. Write random data, random length.
3. Reload the same address.
4. Read disk.
5. Compare data.
6. Repeat test 1024 times.

C. MAINTENANCE AIDS

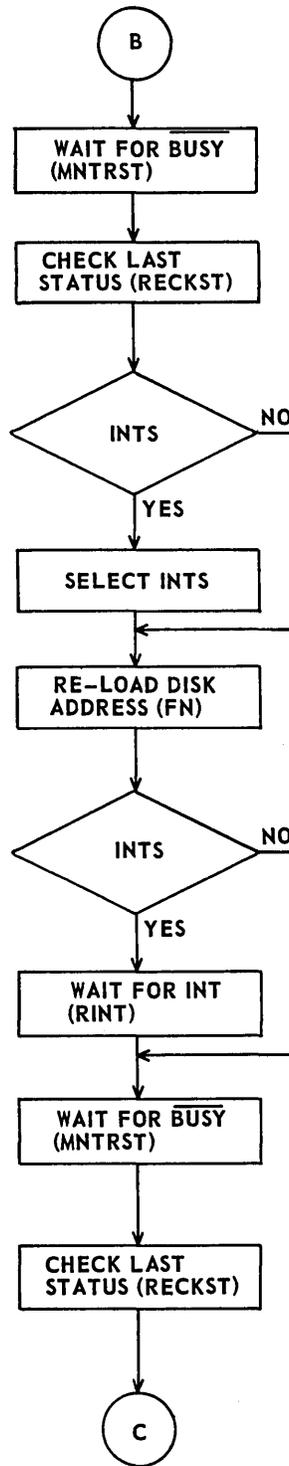
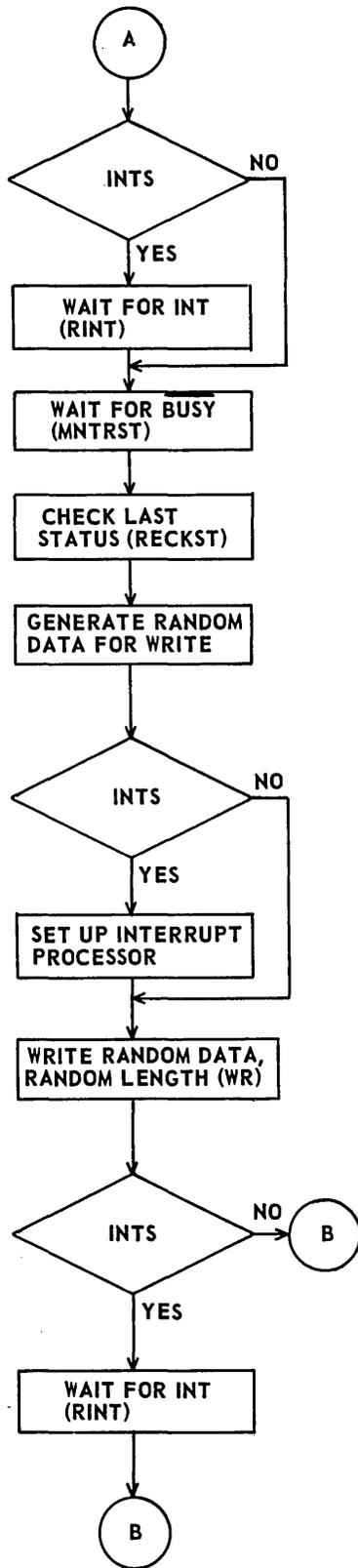
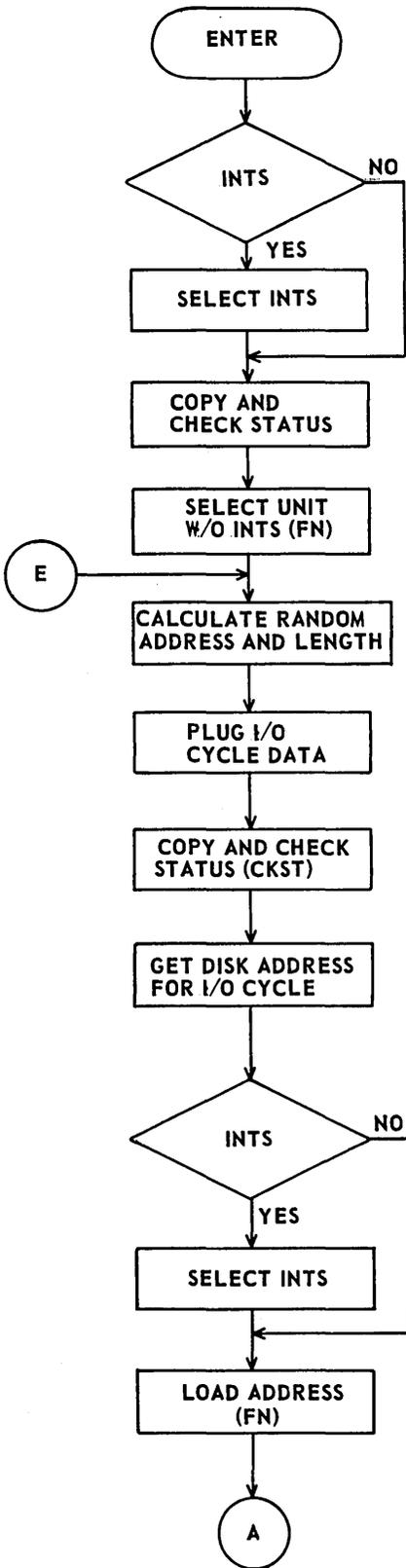
1. For systems with a teletype, the test will ring the teletype bell (parameter) after detecting an error. It is intended to be used with the omit typeout feature as an aid in locating intermittent failures. For example, card and cable checking could be done in this mode. The failure would be indicated without waiting for the printout before resuming the test.
2. For unattended runs, the omit typeout feature could be used. After the run, clear the omit typeout bit. The end test message will contain the total accumulated errors. Restarting the test clears the error counter.

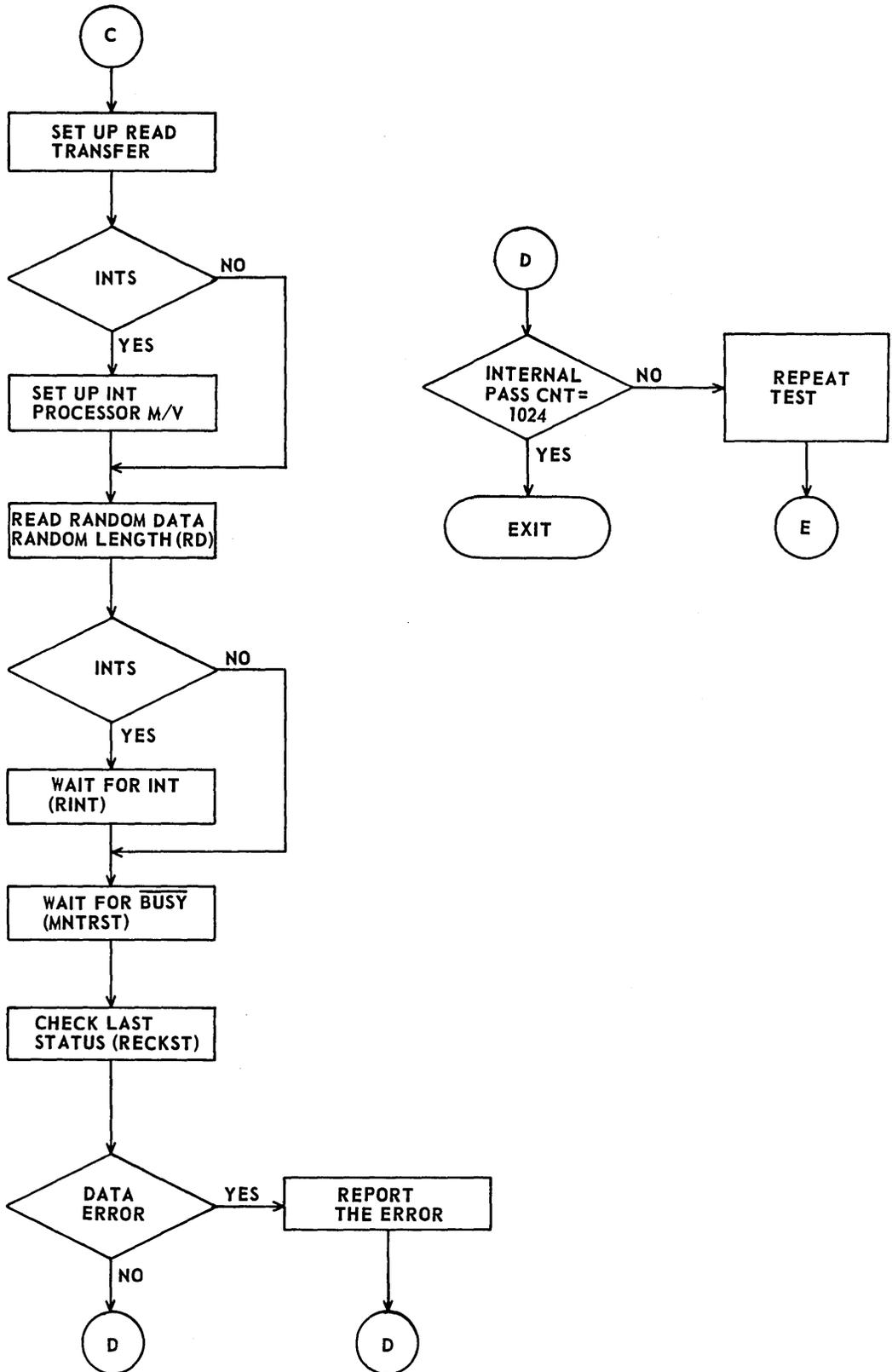
D. RUNNING TIME

Approximately 3 minutes on a 1704.

E. DETAILED FLOW CHARTS

TEST DP5 1738 Q/L





1738, 1733-1/853, 854, and QSE 4730 DISK PACK TEST

(DP3027, Test No. 27)

(CP = 2F)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

- a. The range of cylinders upon which data will be written may be limited during the parameter stop. The lower limit is ignored in Section 12 (data is written in cylinder 0 to be autoloaded).
- b. A large number of typeouts and/or stops may occur for error codes 14, 1B, and 1D unless bit 11 of the Stop/Jump parameter is set.
- c. In Section 12 (Autoload) the diagnostic may be destroyed if Autoload function is not working properly. Section 12 should not be run on a Maintenance Pack.
- d. When using a new pack, it is necessary to ensure that the pack has address tags and data on the entire surface before checkword functions are performed. Running Section 10 and then Section 6 will ensure that the pack contains correct data required for other sections.
- e. Caution should be exercised when running Section 15 if DT193 is installed because it involves core to core transfer from originating computer to computer on other access. The transfer is one for one, so at the end of the section, computer 2 will have the same thing in core as computer 1, except location 0 which must be hand loaded if SMM is to be started from location 0.
- f. Bits 2 and 3 of the SMM parameter word must specify the correct machine type.

B. LOADING PROCEDURE

1. The test operates as a sub-program under control of the 1700 System Maintenance Monitor (SMM17).
2. The test mnemonic is DP3, number 27.
3. The call sequence is that specified by SMM17.

C. PARAMETERS

1. If no parameter stop is made, the test will use prestored parameters as follows:
 - a. Sections 1 through 5, 8, 11, and 13.
 - b. Range limits: cylinder C_{16} -low limit, cylinder 63_{16} -upper limit.

- c. Interrupt line: preset to interrupt line 3
 - d. Unit number: preset to unit 0
2. To alter parameters, follow directions stated in SMM17. (See SMM/Operator Interface Section V.)
- a. First Stop: A = 2721, Q = Stop/Jump parameter.
 - b. Second Stop:
 - Bit 0 of A = Section 1 - static status check
 - Bit 1 of A = Section 2 - random positioning
 - Bit 2 of A = Section 3 - write, read, compare
 - Bit 3 of A = Section 4 - write, read, compare using interrupts
 - Bit 4 of A = Section 5 - force address errors, check write and read into next cylinder
 - Bit 5 of A = Section 6 - surface test, Alarm, and EOP interrupt selected
 - Bit 6 of A = Section 7 - check overlapping seek
 - Bit 7 of A = Section 8 - variable sector length check
 - Bit 8 of A = Section 9 - protect test
 - Bit 9 of A = Section 10 - write address tags
 - Bit 10 of A = Section 11 - positioning timing check
 - Bit 11 of A = Section 12 - autoloading check (CAUTION: see restrictions)
 - Bit 12 of A = Section 13 - check word check of surface
 - Bit 13 of A = Section 14 - 1733-1 extra options check
 - Bit 14 of A = Section 15 - core to core transfer and check
 - Bit 15 of A = 0, 853 type disk drive
 - Bit 15 of A = 1, 854 type disk drive
- Range limits Q = XXYY
- XX = lowest numbered cylinder to be written on (Section 12 ignores this limit)
- XX = $0C_{16}$ - preset value
- YY = highest number cylinder to be written on
- YY = 63_{16} - preset value is for 853
- YY = CA_{16} - value to be entered for 854

c. Third Stop:

A = interrupt line (e.g., bit 3 in A set for interrupt line 3)

Q = set bit X to run unit X. The lowest unit selected will be run in all sections except Section 7, (overlap seek) where all units selected will be run (bit 0 = unit 0, bit 1 = unit 1, etc.)

d. SELECTIVE SKIP and STOP Settings:

1. STOP - should be set for SMM17 running.
2. SKIP - should only be set to display Stop/Jump parameters for purposes of changing same.

II. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Program Typeouts

a. Test identification during test initialization:

DP 3027, 1700 Disk Subsystem CP2F, Ver. 3.1 IA - XXXX, FC = XX
--

b. End of Test

A	Q	A	Q
2724	Stop/Jump Parameter	Pass Number	Return Address

2. Error Messages

General format of error display is shown under SMM/Operator Interface Descriptions in Section V of SMM Manual.

General Display Format:

A	Q	A	Q	A	Q
Information	Stop/Jump	Section/	Return	Additional	Additional
Word (2738	Parameter	Error	Address	Data	Data
for three		Code			
stops and 2748					
for four stops)					

B. ERROR CODE DICTIONARY

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
00	INP OUTPUT	External reject A = Director status at reject Q = Contents of Q at reject
01	INP IECHK IED	Internal reject of input to A A = BADD Q = Contents of Q upon input to A A = Contents of A at last output from A Q = Contents of Q at last output from A
02	OUTPUT IEA	Internal reject on output from A A = Director status Q = Address register status A = Contents of A at last output from A Q = Contents of Q at last output from A
03	IEC	Interrupt status bit not set when interrupt occurred A = Selected interrupts 1 - Ready, not busy 2 - End of operation 4 - Alarm Q = Status at interrupt A = Contents of Q at last output
04	IEB	Non-selected interrupt occurred (or interrupt occurred too soon) Display same as error code 03
05	IEE	Interrupt status bits not cleared by clear interrupt function A = Status at interrupt Q = Status after clearing interrupt A = Contents of A at last output from A Q = Contents of Q at last output from A (other than Clear Interrupt function)

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
06	CONALARM SEC1C	Ready status not present A = Director status Q = Address register status A = Address register previous to this operation Q = Contents of Q at last output from A
07	SEC1A	On Cylinder status not present A = Director status Q = Address register status
08	BUSYPRES	Busy not present after an output from A Display same as for error code 06
09	CONALARM	Storage parity error Display same as for error code 06
0A	CONALARM	Defective track Display same as for error code 06
0B	CONALARM	Address error Display same as for error code 06
0C	CONALARM	Seek error Display same as for error code 06
0D	CONALARM	Lost data Display same as for error code 06
0E	CONALARM	Checkword error Display same as for error code 06
0F	CONALARM	Protect fault Display same as for error code 06
10	CONALARM	Alarm condition present but alarm status bit not set Display same as for error code 06

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
11	ADDRESS	Address register status does not equal loaded address after load address and waiting for Not Busy A = BADD Q = Director status A = Address register status Q = Loaded address
12	SX15	Controller reserved during attempt to check core to core transfer (MC other computer.) Execute clear reserve
13	S8X15	No compare status bit set during an uneven sector compare A = Director status Q = Cylinder status A = Buffer length Q = Expected cylinder address
14	COMPARE	Data compare error. Write and read buffer are compared in computer A = Cylinder register status Q = Number of word in error A = Word written Q = Word read (By setting bit 11 in Stop/Jump parameter, multiple errors in same buffer can be eliminated)
15	COMBUF	No compare status bit set A = Director status Q = Cylinder register status
16	SEC5B	No alarm interrupt occurred when forcing an address error by loading an illegal address A = Loaded address Q = Director status A = Interrupt line Q = Selected interrupts (see error code 03)

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
17	SEC5D SEC5V	An address error was forced but status bit not set A = Loaded address Q = Director status
18	SEC5U	No alarm interrupt occurred when attempting to force address error by initiating checkword check with illegal address Display same as error code 16
19	SEC5I	Address error not present when writing off end of pack Display same as error code 17
1A	BUSYPRES	Controller hung busy (automatic abort if run after error) A = Director status Q = Return address of routine calling busy A = Contents of A during last output Q = Contents of Q during last output
1B	SEC6 ERROR	Surface check detected data error A = Address of sector in error Q = Number of word into sector A = Data expected Q = Data read (Set bit 11 in Stop/Jump parameter to ignore rest of errors in this sector or track.)
1C	SC11B	Maximum positioning time (165 milliseconds) was exceeded A = Time required (milliseconds, hexadecimal) Q = Loaded address
1D	S12D	Autoload failed to load correct data. Set bit 11 in the Stop/Jump parameter to ignore the rest of the words in error A = BADD Q = Number of word in error A = Word written Q = Word in core after autoload

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
1E	CONALARM	End of operation status not present Display same as for error code 16
1F	SEC1B	Status other than Ready, On Cylinder is present (ignoring protect status) during static check Display same as for error code 07
20	SEC5X	Alarm interrupt did not occur when writing off the end of disk pack Display same as for error code 16
21	ADRINTP WRT1 RD1 CW1 CB1	No interrupt occurred when End of Operation or Ready, Not Busy interrupt was selected A = Selected interrupts (see error code 03) Q = Director status A = Contents of A upon last output from A Q = Contents of Q upon last output from A
22	ADW2 SEC8	During a wait for operation to complete busy dropped before expected address was attained A = Director status Q = Cylinder status A = Buffer length Q = Expected address
23	ADW5 SEC8	During a wait for operation to complete expected address was attained; however, busy did not drop Display same as error code 22
24	CONALARM	Alarm status bit set, no alarm condition Display same as error code 06
25	SEC5M	No compare status not set after attempting to force no compare status A = Director status Q = Cylinder register status

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
26	CKAC	Unit went to incorrect address during overlaps seek A = Unit number Q = Director status A = Loaded address Q = Cylinder register status
27	S5X3	Reject during Off Cylinder when attempting a director function A = 0 if internal reject; 1 if external reject Q = N/A
28	S5XE	Second address accepted when sent during Off Cylinder A = 200 if a reply 0 if internal reject Q = N/A
29	S14X1	Unit Not Ready, On Cylinder after a Clear Controller function A = Director status Q = Expected status
2A	S14X3	Checksum error A = Actual checksum Q = Predicted checksum
2B	CERR	Controller went not reserved, however no interrupt received A = Director status Q = N/A
2C	ADW2	Cylinder address went beyond that expected A = Director status Q = Cylinder status A = Buffer length Q = Expected address

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
2D	CC1	Return cylinder function address not the same as cylinder status A = Return cylinder address (after reconstruction) Q = Cylinder status
2E	S14X71	Buffered load address does not compare with address expected A = Actual address Q = Address sent via buffered load address
2F	VFYCWA	Current word address register incorrect A = Expected CWA Q = Actual CWA
30		Address upon completion of a Ready, Write, Compare, or Checkword Check operation is not equal to the expected address A = Contents of Q upon last output from A (other than Clear Interrupt function) Q = Director status A = Address register status Q = Expected address
31		Recoverable error occurred during checkword check (Section 13) A = Address of track causing error Q = Director status when last error occurred
32		Non-recoverable error occurred during checkword check (Section 13) Display same as for error code 31
33	S9X13	No protect fault status when forced A = Director status Q = N/A
34	S9X2	Non-protected output instruction replied on a protected controller A = N/A Q = N/A

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
35	S9X3	Non-protected input instruction rejected on protected controller A = N/A Q = N/A
36	S9X32	Protected unit select failed A = N/A Q = N/A
37		Protect status not present A = Director status Q = N/A
38		Non-protected write sequence on protected unit did not reject A = N/A Q = N/A
39 through 3F		Not used
40		Operator error. Interrupt line or equipment address in error. Test must be reloaded. A = Selected equipment address Q = Selected interrupt line (if any)

III. DESCRIPTION

A. GENERAL DESCRIPTION

1. The 1738 (or 1733-1) 85X Disk Sub-System Diagnostic (DP3-27) Test is divided into 15 individually selectable test sections. Sections 1 through 5, 8, 11, and 13 are prestored as normally selected tests. Sections 7, 9, 10, 12, 14, and 15 must be selected by the operator. Section 7 should have at least two units selected. Sections 14 and 15 should not be run on a 1738 or a 1733-1 without DT193 installed in the 1733-1.

B. SECTIONS DESCRIPTION

1. Section 1 - Static Status Check
 - a. Select unit.
 - b. Input director status.
 - 1) Ready should be present.
 - 2) On Cylinder should be present.
 - 3) No other status (other than protected) should be present.
 - c. Loop to step a 499 times.
2. Section 2 - Random Positioning Check
 - a. Generate 96 random numbers.
 - b. Convert random number to legal addresses.
 - c. Select unit.
 - d. Load address.
 - e. Check for expected address.
 - f. Check alarm conditions and End of Operation status.
 - g. Update address.
 - h. Loop to step c 95 times.
3. Section 3 - Write, Read, and Compare
 - a. Generate 96 random words and one random address.
 - b. Select unit.
 - c. Load address, check for expected address, alarm conditions, and End of Operation status.
 - d. Write one sector.
 - e. Check Not Busy address.
 - f. Check alarm conditions and End of Operation status.
 - g. Loop to step b if repeat conditions selected.
 - h. Select unit.
 - i. Load address.
 - j. Read one sector.
 - k. Check Not Busy address.
 - l. Check alarm conditions.
 - m. Loop to step n to repeat conditions.

- n. Select unit.
 - o. Execute checkword check.
 - p. Check alarm conditions and End of Operation status.
 - q. Check Not Busy address.
 - r. Loop to step n to repeat conditions.
 - s. Select unit.
 - t. Load address, check for expected address, alarm conditions, and End of Operation status.
 - u. Execute Compare function.
 - v. Check for Not Compare status.
 - w. Check alarm conditions and End of Operation status.
 - x. Check Not Busy address.
 - y. Loop to step s to repeat conditions.
 - z. If no alarm condition or unexpected address occurred, compare input buffer with output buffer area.
 - aa. Loop to step z to repeat condition.
 - ab. Loop to step a 95 times.
4. Section 4 - Write, Read, and Compare Under Interrupt Control
- Same as Section 3 except interrupts on Alarm, End of Operation, and Next Ready Not Busy are selected prior to performing a Load Address, Read, Write, Checkword Check, and Compare operation. After the interrupt occurs, the status at interrupt is checked for alarm conditions.
5. Section 5 - Force Address Errors and Check Writing Into Next Cylinder
- a. Generate illegal address (00F0).
 - b. Select unit.
 - c. Select interrupt on alarm.
 - d. Load illegal address.
 - e. Check whether correct interrupt occurred.
 - f. Check address Error status.
 - g. Loop to step c to repeat conditions.

- h. Select interrupt on alarm.
- i. Initiate checkword check.
- j. Check whether correct interrupt occurred.
- k. Check address Error status.
- l. Loop to step h to repeat conditions.
- m. Generate an illegal address (FF00)
- n. Loop to step b once.
- o. Form last sector address of unit (CA9F for 854, 639F for 853).
- p. Jump to step v if range of cylinders to be written into is not high enough to include this cylinder.
- q. Load address and check alarm conditions.
- r. Write 97 words (off end of disk pack).
- s. Check whether correct interrupt occurred.
- t. Check address Error status.
- u. Loop to step q to repeat conditions.
- v. Generate legal address.
- w. Load address and check alarm conditions.
- x. Write 97 words.
- y. Load address and check alarm conditions.
- z. Add one to second word of buffer area.
- aa. Execute Compare function.
- ab. Check No Compare status (should be set).
- ac. Loop to step w to repeat conditions.
- ad. Generate address of last sector of a cylinder.
- ae. Load address and check alarm conditions.
- af. Write 97 words (into next cylinder).
- ag. Check alarm conditions.
- ah. Loop to step ae to repeat conditions.
- ai. Load address and check alarm conditions.

- aj. Execute Compare function.
- ak. Check No Compare status and alarm conditions.
- al. Loop to step ai and repeat conditions.
- am. Load address and check alarm conditions.
- an. Read 97 words.
- ao. Check alarm conditions.
- ap. Loop to step am to repeat conditions.
- aq. If no alarm conditions occurred between steps ae to aq, compare input buffer area with output buffer area.
- ar. Loop to step a 95 times.

6. Section 6 - Surface Check

- a. Set up Read and Write routines for a 1536-word buffer (one track) or a 96-word buffer (one sector), depending on available core.
- b. Generate address of first cylinder to be written on.
- c. Generate pattern, 6161 for first pass through section, CECE for second pass.
- d. Fill buffer area with pattern, alternate words complemented.
- e. Select unit and select interrupts on Alarm and End of Operation.
- f. Load address and write under interrupt control.
- g. Check for correct interrupts and alarm conditions.
- h. Check Not Busy address.
- i. Loop to step c to repeat conditions
- j. Increment address.
- k. Loop to step f unless address is greater than last cylinder to be written into.
- l. Re-initialize address.
- m. Select unit and select interrupts on Alarm and End of Operation.
- n. Load address and read under interrupt control.
- o. Check for correct interrupts and alarm conditions.
- p. Check Not Busy address.

- q. If no alarm conditions occurred in step m, check whether expected pattern was read.
 - r. Loop to step m to repeat conditions.
 - s. Increment address.
 - t. Loop to step n unless address is greater than address of last cylinder to be written into.
 - u. Loop to step b once.
7. Section 7 - Check Overlap Seek
- a. Generate 96 random numbers.
 - b. Convert to legal addresses.
 - c. Select first unit (unit specified in parameter word during initial parameter stop).
 - d. Load address.
 - e. Wait for End of Operation status (may still be busy).
 - f. Select another unit.
 - g. Load address.
 - h. Wait for End of Operation status (may still be busy).
 - i. Repeat for all units selected.
 - j. Select first unit.
 - k. Wait for Not Busy.
 - l. Check whether address register status equals loaded address.
 - m. Select another unit.
 - n. Wait for Not Busy.
 - o. Check whether address register status equals loaded address.
 - p. Repeat for all units selected.
 - q. Loop to step c 95 times.
8. Section 8 - Various Sector Length Checks
- a. Initialize, passcount, input buffer, less sector value.
 - b. Generate a random data buffer.
 - c. Set output buffer to less than one sector.

- d. Select unit and reserve.
- e. Load address.
- f. Write partial sector.
- g. Check Cylinder status.
- h. Check alarms.
- i. Repeat conditions to step d.
- j. Load address.
- k. Read one sector.
- l. Check alarms.
- m. Repeat conditions to step j.
- n. Clear part of buffer not written for zero fill check.
- o. Compare Write and Read buffer.
- p. Repeat condition to step d for continuous write.
- q. Load address.
- r. Execute a less than full sector compare.
- s. Check Cylinder status.
- t. Check alarms.
- u. Repeat conditions to step q.
- v. Repeat sub-section to step c.
- w. Change value of less than sector.
- x. Generate a random buffer of length specified by passcount and Buffer table.
- y. Set FWA-1 in output buffer.
- z. Set address to low address limit.
- aa. Load address.
- ab. Predict Cylinder address after executing transfer.
- ac. Execute a Write.
- ad. Wait for operation to complete by checking for expected Cylinder address.
- ae. Repeat condition to step aa.
- af. Load address.

- ag. Execute a Compare.
 - ah. Wait for operation to complete by checking for expected Cylinder address.
 - ai. Check No Compare status.
 - aj. Repeat condition to step af.
 - ak. Loop to step g until passcount is zero.
9. Section 9 - Protect Test
- a. Initialize passcount and output buffer
 - b. Set address to low limit.
 - c. Select and reserve.
 - d. Position.
 - e. Clear all protect bits in core.
 - f. Set one location in buffer protected.
 - g. Set protect on computer and clear device protect.
 - h. Execute a Read operation.
 - i. Check for Protect Fault status.
 - j. Repeat condition to step c.
 - k. Set device protect.
 - l. Clear PROTECT switch on computer.
 - m. Position to low limit.
 - n. Set protect bits for output of unit select.
 - o. Set PROTECT switch
 - p. Execute a unit select with protected instruction.
 - q. Input director status to check protect status bit.
 - r. Check that a Clear Interrupt function is rejected.
 - s. Repeat condition to step w.
 - t. Check Input Cylinder status is accepted.
 - u. Repeat condition to step w.
 - v. Execute a Write sequence with unit protect set. Expect a reject.
 - w. Clear PROTECT switch.

- x. Repeat condition to step m.
- y. Clear unit protect.
- aa. Repeat condition to step m.
- ab. Repeat sections.

NOTE: In order to present errors through SMM with PROTECT switch set, A stop is first executed to allow protect to be taken off. (A) = F000 indicates this.

10. Section 10 - Write Address Tags

- a. Generate address of first cylinder to be written onto.
- b. Select unit.
- c. Write addresses on track.
- d. Wait not busy.
- e. Increment track number.
- f. Loop to step c unless address is greater than address of last cylinder to be written in.

11. Section 11 - Positioning Time Check

- a. Generate 96 random numbers.
- b. Convert random numbers to legal addresses.
- c. Make several of the addresses equal to the lowest and highest possible addresses, alternately.
- d. Initiate load address and initialize millisecond count.
- e. Wait 1 millisecond.
- f. Increment millisecond count.
- g. Check status for busy.
- h. Loop to step e if busy.
- i. Error if millisecond count greater than 165_{10} .
- j. Loop to step d 95 times.

12. Section 12 - Autoload (CAUTION: See Restrictions, page 205-1)

- a. Move first 1536 (600_{16}) words of core to buffer area.
- b. Select unit.

- c. Load address, cylinder zero, track zero, sector zero.
 - d. Wait not busy.
 - e. Write 1536 words.
 - f. Change one location in low core.
 - g. Stop.
 - h. Operator should push AUTOLOAD button.
 - i. Compare buffer area with low core.
13. Section 13 - Check Recoverable Errors
- a. Initial address equals zero.
 - b. Select unit.
 - c. Initialize attempt counter.
 - d. Initiate checkword check.
 - e. Wait not busy.
 - f. Check status for Checkword, Lost Data, Seek Storage Parity, Defective Track errors.
 - g. Jump to step m if not set.
 - h. Save Error status.
 - i. Increment attempt counter.
 - j. Loop to step d unless attempt counter equals 10.
 - k. Error is not recoverable.
 - l. Jump to step n.
 - m. No errors if attempt counter equals initial value; recoverable error if not.
 - n. Increment track address.
 - o. Loop to step c unless address is greater than last possible address.
14. Section 14 - 1733 Optional Test (DT193 must be installed)
- a. Set passcount to 96.
 - b. Check reserve.
 - c. Send a Clear Controller.
 - d. Wait for On Cylinder.

- e. Repeat condition to step b.
- f. Release reserve.
- g. Check Ready, On Cylinder status.
- h. Build an output buffer for checkword check.
- i. Select Alarm and Seek interrupt.
- j. Check reserve.
- k. Load address and check for Seek interrupt.
- l. Select EOP and Alarm interrupt.
- m. Write buffer.
- n. Repeat condition to step i.
- o. Check (CWA) Current Word Address register.
- p. Repeat sub-condition to step i (bit 11).
- q. Check reserve.
- r. Load address.
- s. Select Read Checkword function.
- t. Set input buffer to one extra word.
- u. Execute a Read sequence.
- v. Repeat condition to step q.
- w. Check CWA register.
- x. Release reserve.
- y. Compare input and output buffer internally.
- z. Repeat sub-section to step i (bit 12).
- aa. Compare actual and expected checkword.
- ab. Repeat condition back to step q (bit 11).
- ac. Check reserve.
- ad. Select Return Address function.
- ae. Execute a three-word read.
- af. Repeat condition to step ac.
- ag. Compare Buffered Cylinder register and Cylinder status.

- ah. Repeat sub-condition to step ac (bit 11).
 - ai. Prepare buffer for masked compare.
 - aj. Load address.
 - ak. Select Masked Compare function.
 - al. Execute a Compare operation.
 - am. Repeat condition to step aj.
 - an. Execute special Checkword Check operation.
 - ao. Check status and alarms.
 - ap. Repeat condition to step an.
 - aq. Execute a buffered load address using address 5595 or 2A6A (Hex).
 - ar. Compare cylinder status with address buffered out.
 - as. Repeat condition to step aq.
 - at. Check Interrupt on next not reserved.
 - au. Next iteration to step b.
 - av. Repeat section to step a.
15. Section 15 - Core to Core Transfer Test; Program Transfer to Other Computers (CAUTION: see restrictions at I. A.)
- a. Check if controller is reserved.
 - b. Report if controller is reserved, and loop back to a.
 - c. Set input buffer the same as output buffer.
 - d. Select unit and reserve controller.
 - e. Transfer 96 word buffer to other computer.
 - f. Check alarms and status.
 - g. Clear output buffer.
 - h. Transfer 96 word buffer from other computer.
 - i. Check alarms and status.
 - j. Compare output buffer to input buffer as stored in step c.
 - k. If repeat condition, reset output buffer and loop to step d.
 - l. Save location 0.

- m. Store Last Word address of program in location 0.
- n. Execute core to core transfer of entire program to other computer (all except location zero).
- o. Check alarms and status.
- p. Reset location zero.
- q. Release controller reserve.
- r. Repeat condition to step l.
- s. Repeat section to step a.

NOTE: If program is started from IA (initial address) of test, no problem will be encountered.

IV. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

About $1C00_{16}$ core is required.

B. TIMING (Test running alone, no errors)

1. Section 1 = approximately	1	second
2. Section 2 = approximately	7.5	seconds
3. Section 3 = approximately	16	seconds
4. Section 4 = approximately	17	seconds
5. Section 5 = approximately	10	seconds
6. Section 6 = approximately	8	minutes
7. Section 7 = approximately	7	seconds
8. Section 8 = approximately	3	seconds
9. Section 9 = N/A (operator intervention)		
10. Section 10 = approximately	1 minute	13 seconds
11. Section 11 = approximately	10	seconds
12. Section 12 = N/A (operator intervention)		
13. Section 13 =	1 minute	17 seconds
14. Section 14 = approximately	30	seconds
15. Section 15 = less than 1 second		

(All times measured using 854.)

C. ACCURACY

Section 11 (the positioning timing check) bases the 165 milliseconds on instruction execution time. If instruction execution time is a few percent less than 1.1 or 1.5 microseconds, error typeouts may occur.

D. EQUIPMENT CONFIGURATION

Computer with 8K memory 1704/14/1705 or 1774/1773/1775, 1784

Disk Controller 1738 or 1733-1

Disk Drive 853 or 854s.

APPENDIX A FUNCTION CODES

<u>Dir Bits</u> <u>Q Register</u>	<u>Output From A</u>	<u>Input to A</u>
0	*Core to Core Normal	
1	Director Function	Controller Status
2	Load Address A/Q	File Address Status
3	Write	*Current Word Address
4	Read	
5	Compare	
6	Checkword Check	
7	Write Address Tag	
8	*Core to Core Reverse	
A	*Enable DSA Load Address	
E	*Checkword Check	

DIRECTOR STATUS

XXX1 - Ready	X1XX - Checkword Error
XXX2 - Busy	X2XX - Lost Data
XXX4 - Interrupt	X4XX - Seek Error
XXX8 - On Cylinder	X8XX - Address Error
XX1X - EOP	1XXX - Defective Track
XX2X - Alarm	2XXX - Storage Parity Error
XX4X - No Compare	4XXX - Protect fault
XX8X - Protected	8XXX - ¶Reserved

* These function codes and director function bits are only available in a 1733-1 (FA102) with Special Option 60141 (DT193) installed.

¶ These director function bits and status are available in a standard 1733-1.

DIRECTOR FUNCTIONS

XXX1 - $\overline{\text{r}}$ Clear Controller
XXX2 - Clear Interrupt
XXX4 - Ready Not Busy Interrupt Request
XXX8 - EOP Interrupt Request
XX1X - Alarm Interrupt Request
XX2X - *Not Reserved Interrupt Request
XX4X - *Seek Interrupt Request
XX8X - Release Unit Select
X1XX - Unit Select and Reserve
X2XX - Unit Select bit 2⁰
X4XX - Unit Select bit 2¹
X8XX - $\overline{\text{r}}$ Unit Select bit 2²
1XXX - *Enable Mask on Compare
2XXX - *Return Cylinder Address
4XXX - *Read Checkword
8XXX - $\overline{\text{r}}$ Release Reserved

* These function codes and director function bits are only available in a 1733-1 (FA102) with Special Option 60141 (DT193) installed.

$\overline{\text{r}}$ These director function bits and status are available in a standard 1733-1.

1733-2 MULTIPLE CARTRIDGE DISK DRIVE CONTROLLER
(MDC07A Test No. 7A)
(CP = 2C)

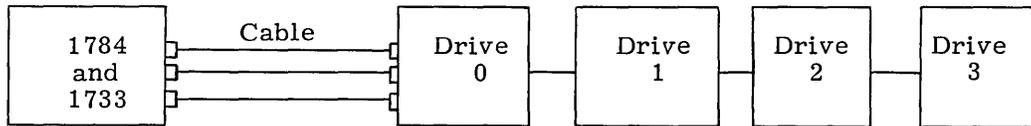
I. INTRODUCTION

The purpose of this test is to verify the operation of the Cartridge Disk Controller and Drives. The test is meant to be an engineering, manufacturing, and field maintenance test. The test will be run in an ascending order, each test becoming progressively more complex.

II. REQUIREMENTS

A. HARDWARE

The test is intended to verify the 1733-2 Cartridge Disk Controller. The controller is connected to the internal DSA and to the AQ Channel of the 1784.



B. SOFTWARE

The test will reside under SMM17 and all rules of SMM17 apply.

NOTE

All references made in this document are to the 1700 System Maintenance Monitor (SMM17) Reference Manual.

C. ACCESSORIES

None

III. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

- a. The range of cylinders upon which data will be written on disk 0 (cart-
ridge) may be limited during the parameter stop. The low limit must
be zero for Section 12 (data is written on cylinder 0 to be autoloaded).
- b. A large number of typeouts and/or stops may occur for error codes 14,
1B, and 1D unless bit 11 of the Stop/Jump parameter is set.
- c. In Section 12 (Autoload) the diagnostic may be destroyed if the Autoload
function is not working properly. Section 12 should not be run on a
Maintenance Pack.
- d. When using a new pack, it is necessary to ensure that the pack has
address tags, correct data, and checkwords. Data may be destroyed
in shipment. Section 3 and then Section 7 should be run to ensure that
the pack contains the correct data required for other sections.
- e. Range limits must be set for single dens drives if there is a mixture
of drives on this controller.

B. LOADING PROCEDURE

1. The test operates as a sub-program under control of the 1700 System Main-
tenance Monitor (SMM17) Version 3.0 on.
2. The test mnemonic is MDC number 7A.
3. The calling sequence is that specified by SMM17.

C. PARAMETERS

1. If no parameter stop is made, the following sections will be run.
 - a. Section 1
 - b. Section 2
 - c. Section 4
 - d. Section 5
 - e. Section 6
 - f. Section 7
 - g. Section 8
 - h. Section 11
 - i. Section 13
 - j. Section 15

The test will run on disk 0 and the fixed disk. Cylinder 0 through CA80₁₆
will be tested. The interrupt line will be line 3.

Q = Stop/Jump Parameters

Bits 0-10 - Defined by SMM

11 - Report only first date error of this read.

- 12 - Section 2 only - repeat condition with clear controller while doing incremental addressing test only.
- 13 - Section 2 only - repeat condition with clear controller while doing random addressing only.
- 14 - Section 4 only - SLS must be set. This forces a stop with
 - A = Data pattern you want to be used by this section.
 - Q = Disk address to be used by this section. This condition will repeat until bit 14 is dropped.

2. To alter the parameters, follow directions stated in the SMM17 Reference Manual. If bit is set, the corresponding section or condition will be selected. The parameter words to be displayed are as follows:

a. First Stop: A = 7A41. Q = Special

b. Second Stop:	Bit 15 = Fixed Disk
Crosstrack Test	Bit 14 = Section 15*
Protect Test	Bit 13 = Section 14
Checkword Check	Bit 12 = Section 13*
Auto Load Check	Bit 11 = Section 12*
Position Time Text	Bit 10 = Section 11*
Overlapping Operations	Bit 9 = Section 10
Head and Sector Address Test	Bit 8 = Section 9
Worst Pattern, Checkword Gen.	Bit 7 = Section 8*
Surface Test	Bit 6 = Section 7*
Status Forcing	Bit 5 = Section 6*
Same-Sec 4-EOP and Alm Int.	Bit 4 = Section 5*
Read, Write, Compare Test	Bit 3 = Section 4*
Write Address Tags	Bit 2 = Section 3*
Positioner Test	Bit 1 = Section 2*
Preliminary Test	Bit 0 = Section 1*

Q = Unit Select Bit 0 = Unit 0 Bit 1 = Unit 1 etc.

c. Third Stop:

A = OLLL low cylinder address to write on (0000)

LLL = lowest numbered cylinder to be written on (Section 12 ignores this limit)

LLL = 00 - standard

Q = OHHH high cylinder address to write on (0195) or (00CA)

HHH = highest numbered cylinder to be written on

HHH = 195_{16} - standard

d. Fourth Stop:

A = IRPT line

Q = O = single dens drive (202 cylinders)

\bar{O} = double dens (405 cylinders)

e. Range limits (parameter A3/Q3) affect all selected drives equally; therefore, if there is a mixture of drives, the limits must be set for maximum 100TPI drive.

Internal Test Stop = bad cylinder address file, enter cylinder addresses in A and run terminate list via A = O. This affects all selected drives equally.

f. Selective SKIP and STOP Settings:

1) STOP - may be set for running of SMM17

2) SKIP - when set, forces an SMM STOP A = ID Q = MSTJP

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Program Typeouts

a. Test identification during test initialization:

MDC07A Cartridge Disk Controller Test IA = XXXX, FC = XX VR=3.1 CP=2C
--

b. During test Section 14 one of the following typeouts will occur:

Set PROTECT switches

Clear PROTECT switches

c. End of Test

A	Q	A	Q
7424	Stop/Jump Parameter	Pass Number	Return Address

2. Error Alarms

All information shown is displayed after General Display Format.

General Display Format:

A	Q	A	Q	etc.
Information Word (7A48 for 3 stops) (7A48 for 4 stops)	Stop/Jump Parameter	Unit Number/Section/ Error Code	Return Address	Additional Data

B. ERROR CODE DICTIONARY

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
00	INP OUTPUT	External Reject Q = Contents of Q at Reject A = N/A
01	INP CLRCON IECHK IED	Internal reject on input to A A = BADD Q = Contents of Q when input to A A = Contents of A during last output Q = Contents of Q during last output
02	OUTPUT IEA	Internal reject on output A = Director status Q = Cylinder register status A = Contents of A when output attempted Q = Contents of Q when output attempted
03	IEC	Interrupt received but interrupt status bit not set A = Selected interrupts Q = Director status at interrupt A = Contents of A during last output Q = Contents of Q during last output
04	IEB	Interrupt other than was selected occurred (or interrupt occurred too soon) Display same as error code 03
05	IEE	Interrupt status bits not cleared by clear interrupt function A = Director status at interrupt Q = Director status after clear interrupt function A = Contents of A during last output Q = Contents of Q during last output
06	CONALARM	Ready status bit not present A = Director status Q = Cylinder register status A = Director status at instant of alarm. (True cylinder status when seek error (code B) is detected.) Contents of A on last output if no alarm detected Q = Contents of Q on last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
07	SECIA	On cylinder status bit not present A = Director status Q = Cylinder register status A = Contents of A at last output Q = Contents of Q at last output
08	BUSYPRES	Busy not present as expected A = Director status Q = N/A
09	CONALARM	Storage parity error Display same as error code 06
0A	CONALARM	Drive fault (non-recoverable) Display same as error code 06
0B	CONALARM	Address error Display same as error code 06
0C	CONALARM	Seek error (controller). This error should recover Display same as error code 06
0D	CONALARM	Lost data Display same as error code 06
0E	CONALARM	Checkword error Display same as error code 06
0F	CONALARM	Protect fault Display same as error code 06
10	CONALARM	Alarm condition present but alarm status bit not set Display same as error code 06
11	ADDRESS	File address status does not equal computed value A = BADD Q = Director status A = Cylinder register status Q = Expected cylinder register

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
12	WAIT	Controller hung or busy A = Director status Q = Address of originating routine (BIASED) A = Director status at instant any alarm occurred Q = Contents of Q during last output
13	CONALARM	Seek error (drive) Display same as error code 06
14	COMPARE	Data compare error. Write buffer and read buffer are compared in computer A = Cylinder register status Q = Number of word in sector that is wrong A = Word written Q = Word read (By setting bit 11 in Stop/Jump parameter, multiple errors in the same buffer can be eliminated)
15	COMBUF CB2	No compare status bit set A = Director status Q = Cylinder register status
16	SEC6B	No alarm interrupt occurred when forcing an address error by sending illegal difference A = Illegal difference sent Q = N/A
17	SEC6D	An address error was forced but status bit not set A = Illegal address Q = Interrupt status
18	SEC1N	Cylinder, CWA, Checkword, or True cylinder not clear after clear controller was sent A = Contents of incorrect register Q = Function code for incorrect register
19	SEC6I	Address error status not set when writing off end of file Display same as for error code 17

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
1A		Seek complete did not come up at end of seek A = Drive cylinder status (status 5) Q = Unit number expecting seek complete
1B	SEC7 ERROR	Surface check detected error A = Address of sector in error Q = Number of words into sector A = Data written Q = Data read (By setting bit 11 in Stop/Jump parameter, multiple errors in the same buffer can be eliminated)
1C	SEC11B	Maximum positioning time exceeded (96 milliseconds) A = Actual length to position Q = Address positioned to A = Address positioned from Q = N/A (To make this error valid, bits 2 and 3 in SMM parameter must be set for SC1784) 600 or 900 ns
1D	S12D	Auto load failed to load correct data A = BADD Q = Word in error A = Word written Q = Word in core after autoloading
1E	CONALARM	End of operation status not present Display same as error code 06
1F	SEC1J-SEC1B	Status other than Ready and On Cylinder after an output function A = Director status Q = Expected status
20	SEC6X	Alarm interrupt did not occur when writing off end of file A = Last address of file Q = N/A
21	ADPRINTP WRT1 RD 1 CW 1 CB 1	No interrupt occurred when EOP, Ready, Not Busy interrupts were selected A = Selected interrupt Q = Director status A = Contents of A during last output Q = Contents of Q during last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
22	SEC1K	Expected external reject on forced busy did not occur A = 0 - illegal reply; 100-internal reject Q = N/A
23	CWACOMP	Current Word Address register incorrect A = Actual CWA contents Q = Expected CWA contents A = Contents of A during last output Q = Contents of Q during last output
24	CONALARM	Alarm bit set, no alarm conditions set. Display same as error code 06
25	SEC6M	No compare status bit not present A = Director status Q = Cylinder register status
26	CDFA	Cylinder register status does not equal computed cylinder status A = Cylinder register status Q = True cylinder status A = Contents of A during last output Q = Contents of Q during last output
27	CNFE	Cylinder register status incorrect after an operation A = Cylinder register status Q = Expected register contents A = Contents of A during last output Q = Contents of Q during last output
28	SEC1M	Did not get external reject on illegal input director 06 and 07 A = 10 - illegal reply; 0 - internal reject Q = Contents of Q during input
29	SEC14G	Expected protect fault did not occur A = Director status Q = N/A A = Contents of A during last output Q = Contents of Q during last output

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
2A		Not available
2B		Not available
2C		Not available
2D		On cylinder status did not drop after doing a seek from zero to maximum limit A = Actual status Q = 0001
2E	SEC1Q	Output buffer length with immediate input of CWA gave incorrect results A = Contents of CWA register Q = Value sent as buffer length
2F		Not used
30	CHKTRK	Cylinder register not equal to expected value after an operation was executed A = Last output function Q = Director status A = Cylinder register status Q = Expected cylinder status
31	SECTION 13	Recoverable error occurred during checkword check A = Address of track causing error Q = Director status when last error occurred
32	SECTION 13	Non-recoverable error occurred during checkword check. Display same as error code 31
33	SEC2J	Suspected DSA address error (Read/Write must have been verified). In a manufacturing test environment test 2 is necessarily run before test 4 because of degree of difficulty. However, when error 33 occurs, then test 4 must be run before test 2 can be completely verified A = DSA address at failure (THIS IS FWA) Q = N/A A = Data written as determined by software Q = Data read from disk

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
34	SEC15	Crosstrack error A = Address of the error detected Q = First of the three tracks that were used
35	STBT SEC7	Table of Bad Track has been exceeded (limit is 10)
36	SEC8E, G, H, etc.	An incorrect checkword was detected A = Checkword status Q = Expected checkword status
37	S11T3	Cylinder to cylinder position time exceeded A = Actual time Q = Specified limit
38		Not used
39		During overlapping operations unit is found not prepared for address A = Director status Q = N/A
3A		Data error during overlapping operations A = N/A Q = Number of word in buffer A = Expected data Q = Actual data
3B		Lost seek complete with address counters A = Unit 0 address count (number of addresses sent this unit) Q = Unit 1 address count (number of addresses sent this unit) A = Unit 2 address count (number of addresses sent this unit) Q = Unit 3 address count (number of addresses sent this unit)
3C		Lost seek complete with address A = Present address unit 0 Q = Present address unit 1 A = Present address unit 2 Q = Present address unit 3
40		Operator error. Interrupt line or equipment address in error. Restart test A = Selected equipment address Q = Selected interrupt line if any

<u>Message Code (Hexadecimal)</u>	<u>Program Tag Name</u>	<u>Message and Description</u>
41		Operator error. No unit selected. Test will restart A = Unit selection Q = N/A
50		Illegal reply to unprotected output instruction and a protected controller A = Data output Q = Equipment address
60		External reject of unprotected output instruction and an unprotected controller A = Last status Q = Contents of Q on last status A = Data output Q = Contents of Q on last output
61		Internal reject - same as error 60

NON ERROR MESSAGES

A = (ID) 7A1F

Q = Message code

1 = Clear 1784 PROTECT switch

1F = Set 1784 PROTECT switch

V. DESCRIPTION

A. GENERAL DESCRIPTION

1. Cartridge Disk Drive Controller (MDC-7A) test is divided into 15 individually selectable test sections. Sections 1, 2, 4 through 8, 11, 13 and 15 are normally selected tests. Sections 3, 9, 10, 12 and 14 are optional. MDC-7A test sections are divided into subsections and are labeled with program tags such as SEC 8A, B, C, etc. Sec 8 is Section 8 and the letter indicates the subsection.
 - a. The standard test error messages contain the section currently executing. Each error code defined in the error list contains a program reference tag and each test description contains the applicable error codes. The Return address in error messages (may or may not be biased) gives the listing address the error it came from. It is important to note that the Return address may just give a subroutine area which generated the error. To trace back the error, it may be necessary to go to the beginning of the routine and look in the Return Jump address to get the area in the test you came from. This may have to be done more than once to actually get back to the section that the error indicates caused the error.

- b. Sections are structured to run sequentially.
- c. If an error is encountered, it may be helpful to run other sections for trouble analysis and to get a more favorable sequence of operation.
- d. Normally, the test should run with the entire surface available; however, it may be desirable to restrict the test to certain areas (see parameters).

NOTE

The test may be restricted to as little as one cylinder.

- e. Operations performed with a repeat condition are shown in the test description.
- f. Section 7 is used to determine defective tracks. However, this section cannot be run until there is a high degree of confidence that the Read, Write, and Compare operations are relatively error free.
- g. With a new cartridge or fixed disk, Sections 3 and 7, in that order, must be selected individually to assure address tags and data on entire disk. Failure to do this will cause unrecoverable errors.

B. SECTIONS DESCRIPTION

SECTION 1 PRELIMINARY CHECKS

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
U101 U106	SEC1C	*	Clear controller function Input cylinder register status Input director status
U107 U11F	SEC1A		Verify on cylinder present Verify only on cylinder and ready present
U127	SEC1E		Verify cylinder register after CL CONT RC
U101 U102 U102	SEC1F	*	Clear controller function Output clear interrupt function Position forward one cylinder
U127	SEC1F		Check alarms Verify cylinder register RC
U11F	SEC1J	*	Verify EOP drops on output function RC

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
U122	SEC1K	*	Clear controller function Verify busy status give external reject RC WAIT NOT Busy
	SEC1L		Clear controller function Position to cylinder 1
U117	SEC1LA	*	Verify excess negative difference - address error Verify address error and alarm RC
U128	SEC1M	*	Verify external reject on input director 06 and 07 Execute illegal input function RC
U118	SEC1N	*	Verify all registers zero after clear controller Check CWA status Check checkword status Check true cylinder status RC
U12E	SEC1Q	*	Verify all bits operational in CWA register RC Next iteration - jump to SEC1C Repeat section

SECTION 2

POSITIONING TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC2	Position to each legal address on the disk
U327	SEC2X3	* Position to random address
U326		Write 60 word buffer RC
U323		Update for new address. Return to position until done Repeat section

SECTION 3

WRITE ADDRESS TAGS

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC3	Initialize section Clear controller
	SEC3A	Load address
	SEC3B	Write address tags Check alarm RC Advance track count Jump back to SEC3A until first disk complete Check for fixed disk - if present, jump to SEC3A RC Repeat section

SECTION 4 WRITE, READ, COMPARE TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC4	Set passcount Clear controller
	SEC4A	Generate random data and random first address
	SEC4B	*# Write 60 word buffer RC
	SEC4C	* Read 60 word buffer RC
	SEC4D	* Checkword check of track RC
U415 U430	SEC4E	* Compare 60 word buffer Check cylinder register advance RC
U414	SEC4F	* Compare data read against data written RSC RC Next iteration jump to SEC4A Repeat section

SECTION 5 READ, WRITE, COMPARE UNDER INTERRUPT CONTROL

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC5	Set section passcount Clear controller
	SEC5Z	Request interrupt
	SEC5D	Generate random data and random address
U521 U530	SEC5A	*# Write under interrupt control Check cylinder register advance RC
U521 U530	SEC5B	* Read under interrupt control Check cylinder register advance RC

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
U 521	SEC5C	* Checkword check under interrupt control RC
U 521 U 515 U 530	SEC5E	* Compare under interrupt control Check cylinder register advance RC
U 514	SEC5F	* Compare read and write buffers RSC RC Next iteration jump to SEC5D Repeat section

SECTION 6

STATUS FORCING AND
READ, WRITE, COMPARE THROUGH CYLINDERS

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC6	Set section passcount
	SEC6A	Request interrupt Clear controller
	SEC6F	* Select interrupt
U 616	SEC6B	Verify illegal address alarm interrupt Send illegal address (00FF)
U 617	SEC6D	Verify address error status set
	SEC6C	RC Change to a second illegal address (FF00) If second disk not available, skip to SEC6M
	SEC6L	* Clear controller Set address to last sector in file Select interrupt
U 620 U 619	SEC6X	Write 97 word buffer off end of file Check address error status RC
U 625	SEC6M	* Verify no compare circuits Write 97 word buffer Change 1 or 97 word on alternate passes Compare 97 word buffer
	SEC6N	RC

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC6NA	*	Move position to last sector in track Write 97 word buffer RC
U615	SEC6NB	*	Compare 97 word buffer RC
	SEC6NC	*	Read 97 word buffer RC
U614	SEC6NN		Compare read and write buffers RC Next iteration jump to SEC6F Repeat section

SECTION 7 SURFACE TEST

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC7		Set passcount Select appropriate buffer length per core availability Clear bad track table and set flag 2 to avoid selecting an alternate track
	SEC7H, A, C		Set up patterns to be used
	SEC7F		Request interrupt from SMM Clear controller
U730	SEC7X	*	Write a sector or track Verify cylinder register RC
	SEC7R1		Update one sector or track Jump back to SEC7X until file is complete When done, clear controller, prepare for read
U730	SEC7Y	*	Read a sector or track Verify cylinder register
U71B	SEC7F		Compare data bit for bit RC

SECTION 8

WORST PATTERN, CHECKWORD GENERATION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC8G	* Write buffer of all zeros with last word a 0001 ₁₆ and verify a checkword of 80F ₁₆ RC
	SEC8H	* Same as above except last word of FFF ₁₆ and checkword 3A ₁₆ RC
	SEC8K	* Last word FFFF ₁₆ checkword of 3C6 ₁₆ RC
	SEC8L	* First word 0001 ₁₆ checkword of 55D ₁₆ RC
	SEC8LA	* 97th word 0001 ₁₆ checkword 2nd sector after zero padding 55D ₁₆ RC
	SEC8M	* All words of buffer floating one Checkword of 486 ₁₆ RC

SECTION 9

HEAD AND SECTOR ADDRESS TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC9	Set passcount to 2
	S9X1	Select low limit
	S9X2	Build one track buffer (\$AEO words) in increments of \$60 with data pattern equal to disk address. Position disk. Do 1 track write * RC
	S9X6	Repeat for next head if selected
	S9X4	Repeat for fixed disk if selected
	S9X10	Select low limit
	S9X112	Generate 1 sectors data (\$60 words) of sector address. Position disk Do 1 sector read Verify data * RC Repeat for each sector until end of surface. Repeat if fixed disk is also selected

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	S9X20	Set low limit Execute 1 word write from location 0 * RC Increment buffer length X\$10 (left sliding 1). Repeat to S9X20 until all bits of buffer length have been used (1G)
	S9X22	Set low limit Set buffer length to \$60 Set buffer FWA to 1 Initiate write Reposition disk to low limit \$10 word read
U933	S9X26	Verify data against data written Repeat incrementing buffer FWA X\$10 until all 15 or 16 bits have been tested
	S9X28	* RC * RS * Next Disk

SECTION 11 MAXIMUM TIME TO POSITION TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC11	Set up random positions Convert to legal addresses Preset some addresses to high and low extreme Set time for correct computer 1784-900 or 1784-600 Clear controller
	SEC11T1	* Initialize millisecond count and move one cylinder
	SEC11T0	Measure time till end of position Verify less than 8 milliseconds Check for end of file
UB37	S11T3	Report excessive time
	S11T4	Repeat condition to S11T1
	SEC11A	Move up new address Momentarily jump to monitor

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
UB1C	SC11D	*	Position to new address Measure time to busy drop RC Next iteration to SC11A Repeat section

SECTION 12 AUTOLOAD CHECK

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC 12		Set section passcount to one Set disk to address 0
	S12A		Move copy of program to buffer area Write 2784 ₁₀ location onto first track
	S12B		Wait for not busy Change one location in low core STOP - operator must press autoload
UC1D	S12D		Compare autoload data Repeat section (In case of multiple errors, set Stop/ Jump parameter bit 11)

SECTION 13 CHECKWORD CHECK OF ENTIRE SURFACE

<u>Error Code</u>	<u>Program Tag Name</u>		<u>Description of Program</u>
	SEC13		Set section passcount to one Initialize first and last address Clear controller
	S13F	*	Set attempt counter
UD31 UD32	S13A		Load address Execute checkword check Make 10 attempts if alarms set-Jump S13A RC Increment until end of disk jump to S13F Check if fixed disk present; if yes, jump to S13F RC Repeat section

SECTION 14

PROTECT CIRCUITS TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>	
0001	SEC14	Set pass count to 1 Message to clear PROGRAM PROTECT switch	
	S1400	Set program protect bits in test	
	S1400A	Clear program protect bits in protect test output driver	
000F		Message to set PANEL PROTECT switch	
	S1401	Status selected drive Save protect status Message to operator if drive is protected	
	S1402	Generate two sector buffer at \$5555 via protect driver	
	S14BLN	Position drive to high range buffer length Initiate buffer write Check statuses for no alarm Verify, status 2, 5, and 3	
	S1410	Clear read buffer 96 word protect bit Reposition drive Initiate read	
	S1411	Drive protected; verify all statuses	
	S1412	Verify all statuses	
	S1415	RC Message; CLEAR PROTECT SWITCH RS	
			Go to next drive
	UD50	PROPLY	Reply received if drive protected Report error
UD60	PROREJ	Reject received report error if drive is not protected - re-execute sequence via protected I/O	
UD61	PROIRJ	Internal reject. Report error re-execute sequence via protected I/O	

SECTION 15

CROSSTRACK TEST

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	SEC15	Clear subroutine flag for write or compare Generate random addresses

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
		Convert to legal addresses
		Clear controller
		Set section passcount to 5
		Set buffer output to all ones
	SEC15B	* Clear count
		Get 3 consecutive tracks alternately at high and then at low range limits
		Set number of random positions count
		Write first track with all one's
		Write 3rd track with all one's
0F34	SEC15A	Write random data on 2nd track
		Random position
		Return to SEC15A for 20 times
		Compare outer tracks for correct data
		RC
		Next iteration jump SEC15B
		Repeat section

C. SUB-PROGRAM DESCRIPTION

Some major programs (subroutines) are contained in this section and ordered alphanumerically by call name (that is, the entry address tag to the subroutine is the call name of the subprogram).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
XX21	ADPRINTP	Routine to position under interrupt control Select interrupt Position Wait for interrupt Check for errors during interrupt processing Check cylinder register status Exit
	ADSR	Routine to compute difference to get to a new address
XX12	BUSYPRES	Routine to wait for busy to drop and to return control to monitor as required
XX26	CBINTP	Routine to compare under interrupt control
	C DFA	Routine to compare true cylinder and cylinder register status

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	CLRCON	Clear controller routine Execute clear controller function Input director status Wait for on cylinder to drop, then wait for on cylinder to come back up Exit
XX27	CNFE	Routine to compare cylinder register sta- tus with a predicted value after an oper- ation
XX14	COMPARE	Compare write buffer with read buffer internally by computer
	CONALARM	Routine to check for EOP and for absence of all alarms
	CONV	Routine to convert random numbers to legal addresses
	CSCY	Compute expected cylinder status using buffer length for anticipated operation
XX23	CWACOMP	Add buffer length to FWA and check CWA after operation
	CWINTP	Execute checkword check under interrupt control
	IECHECK	Check for any errors during an interrupt
	INC	Routine will cause an increment of values to check bit positions in a 16 bit register
	INCREMEN	Routine to sequentially increment addresses by sector or by tracks (used in Section 7)
	INTPROC	Interrupt processor Stores Q Input status Output clear interrupt Input status Verify both statuses and set appropriate flags Store return address Load Q Exit

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description of Program</u>
	NEXTSECT	Routine to select sections of test
	READ	Position and read one sector under interrupt control
	ROUT 1	Routine to position. Enter routine with Q = to buffer length and A = to new address Store Q and A Check if address is in bad track table (except Section 7 which assigns new bad tracks) Checks for fixed disk and limit addresses as a result of presence or absence Executes ADSR routine Outputs buffer length Executes position Predict address after contemplated operation (CSCY) Exit
	ROUT 2	Routine to read, write, and compare Enter routine with A = FWA and Q = to function Store A in CWACOMP routine Execute operation Wait not busy Check alarms
XX27		Execute CNFE routine
XX26		Execute CDFA routine
XX23		Execute CWACOMP routine Exit
	WRITE	Position and write one sector under interrupt control

VI. APPLICATIONS

A. Suggestions for manufacturing test in the use of this diagnostic test:

An acquaintance with the SMM Reference Manual will enable an operator in better use of SMM tests to aid in resolution of errors and easy maintenance of device being tested.

If possible, a partial debug of controller should be made using the maintenance test panel that is available for this device. However, it is possible to run if clear controller and director status input functions have been debugged. A short, hand-punched program such as the following can be used.

E000		LDQ
0X00	or	OX01
0B00		NOP
02FE		INPUT
0000		STOP

Load SMM test number 7A Cartridge Disk Drive test (MDC). Set Stop/Jump parameter to 49_{16} . Select each test individually. Set range limits if applicable. Assure correct interrupt line is selected.

Attempt sections in following order:

Section 1

Section 3

Section 2 If error 33 occurs, abort test and continue until Section 4 is verified.

Section 4

Section 7 Run until first surface error, then abandon and go to Section 4. (This effectively puts data on entire surface of disk so as to avoid unrecoverable checkword check errors).

Section 4 If an error occurs, you may limit range to as little as one cylinder. By setting repeat condition at proper time and with range limit set to one cylinder, you can debug read, write, compare, or checkword check on only one cylinder. If repeat subsection is selected, you can do all four previously mentioned operations all on one cylinder.

NOTE

The advantage of doing an operation on one cylinder avoids unnecessary positioning time.

Sections 5 and 9 These two tests are similar to test 4 but using interrupt control.

The remaining sections can be run in any order.

B. Explanation of an error and an example of how to repeat an error.

Example of error typeout:

A	Q	A	Q	A	Q	A	Q
7A48	0049	U41E	017F	0009	C801	0000	0205
(IDENT)	(STOP/JUMP)	(SEC/ERR)	(RET.ADD)	VARIABLE		DATA(either 2 or 4 words)	

The first word of the error typeout is the identifier. The second word is the Stop/Jump parameter. The third word contains the section number and the error code. For example, 041E means Section 4 had an end of operation failure. That is, EOP status bit did not set as expected. The fifth word, according to the error explanation, is the director status. The sixth word is the cylinder address that the error occurred at. The seventh word is the status at the instant of an alarm. (Since no alarm is present, this status is not applicable.) The eighth word contains the function code of the last output that was attempted before the error.

At this point, several options are available to the operator:

1. Check if the error is repetitive. Set repeat condition and check for same error again. If error is the same and operator determines that debug will be attempted at this point, a disable typeout can also be set in Stop/Jump parameter and selective stop removed and test will cycle on error.
2. If operator is not sure of the operation being performed at the time of the error, he may want to look at the test description and determine what was being attempted. The operator should proceed as follows:

Go to Section 4 description and look for error code; if error code is not listed, it indicates that it was not the major test performed in this section. Then the operator should use the error information that tells the last function attempted and look for this function in the Section 4 description. The test description shows that a compare function is executed in Section 4E (0205 indicates compare function). By scanning the entire section description, the operator can determine the sequence of events being attempted and determine how many of these will be repeated when he selects repeat condition. A closer detailed observation of the section can be obtained by looking at the listing for this test.

In some types of errors, the fourth word of the typeout or return jump address can point directly to the section where the error occurred.

- C. Suggestions for running test for maintenance of a unit known to have been operating previously.

Load SMM test number 7A Cartridge Disk Drive test (MDC). Set Stop/Jump parameter to 49₁₆. If sectors containing bad surfaces are known, enter an A on fourth parameter stop. If bad areas are known, test would be initiated as follows:

At first stop, set Q = to Stop/Jump of 49₁₆. Hit run and at second stop leave A set to normally selected sections and check Q for correct range limits. Hit run and at third stop set A and Q to correct interrupt line. Hit run and at fourth stop set A = to track number of bad sector. Hit run and at stop enter next bad track address or clear to zero and run and test will execute. If address of bad sectors are unknown, test will have to be initiated as suggested for a manufacturing operation.

VII. PHYSICAL REQUIREMENTS

- A. STORAGE REQUIREMENTS - approximately 8K
- B. TIMING - N/A
- C. EQUIPMENT CONFIGURATION:
1. 1784-X Computer with 8K memory
 2. Interrupt Data Channel
 3. 1 Cartridge Disk Drive 1733-2
 4. Device for loading SMM tests into computer

APPENDIX A

DICTIONARY OF TAG NAMES AND ABBREVIATIONS

<u>Name</u>	<u>Definition</u>
* (Asterisk)	See definition of RC.
Cylinder Register Status	This phrase refers to the contents of the register only and does not always indicate the head position (see true cylinder status).
True Cylinder Status	This status gives the actual cylinder address as read from the disk when a read, write, or compare operation is attempted (only upper eight bits are used).
CWA	Current word address.
Function Code	Refers to equipment code and director bits.
Difference	A 16 bit value consisting of eight lower bits which are absolute and eight upper bits indicating the number of cylinders forward or backward (as determined by bit 5) required to move in order to get to a new address.
RC	Repeat condition, if selected go back to statement marked *.
EOP	End of operation.
DSA	Direct storage access.
FWA	First word address.
Position	Execute a load address difference function to get to a new address.
Range	Selectable parameter entry which limits the area to be written on cartridge portion of drive only.
Compare	Defined by the type of error received. An error with a 14 code indicates an internal compare of read and write data by a computer. A 15 code indicates an error detected when a compare function was executed.
Bad Track	Entire track of 29 sectors labeled as bad by software when any sector or portion of the track will not verify all data checks.
#	See RSC.
RSC	Repeat subsection, if selected go back to statement marked #.

APPENDIX B

FUNCTION CODES

<u>Dir Bits Q Register</u>	<u>Output From A</u>	<u>Input to A</u>
0	Load buffer length	Clear controller
1	Director function	Director status
2	Cylinder register status	Load address difference
3	Write	CWA status
4	Read	Checkword status
5	Compare	True cylinder status/seek complete
6	Checkword check	
7	Write address tag	

DIRECTOR STATUS

XXX1 - Ready	X1XX - Checkword error
XXX2 - Busy	X2XX - Lost data
XXX4 - Interrupt	X4XX - Address error
XXX8 - On cylinder	X8XX - Seek error (cont)
XX1X - EOP	1XXX - Not used
XX2X - Alarm	2XXX - Storage parity
XX4X - No compare	4XXX - Protect fault
XX8X - Protected	8XXX - Seek error (drive)

DIRECTOR FUNCTIONS

XXX2 - Clear Interrupt
XXX4 - Next Ready and Not Busy Interrupt Request
XXX8 - EOP Interrupt Request
XX1X - Alarm Interrupt Request

1745-1746/211 DISPLAY STATION
(DDC040 Test No. 40)

I. INTRODUCTION

A. IDENTIFICATION

1. Title 1745-1746/210 Display Station Test (Test number 40)
2. Type of Program Diagnostic test under 1700 System Maintenance Monitor (SMM17)
3. Computer CONTROL DATA 1700

B. PURPOSE

The display station test operates under the control of the 1700 System Maintenance Monitor to verify all of the operating features and data handling capabilities of either the 1745 or 1746 controller.

NOTE

It does not check any features pertaining to the typewriter.

C. CAUTION TO USER

The timing is done by counting the number of returns to SMM17. All wait times were calculated by the 1745-1746/210 Test running alone. Therefore, when operating in a system mode these times can be greatly increased.

II. PARAMETER ENTRY

Each time the test is entered, either during the initialization or on restart, the test will identify itself by typing.

1745-1746/210

After this typeout, the computer will halt four times.

- A. STOP 1. Displays in A the number and in Q the Stop/Jump parameter.
- B. STOP 2. Enters into the A register the equipment address necessary for a direct input or output (i. e. W = 0, 2, 7, or C; E = equipment address; S = 0; and D = 0).

Enters into the Q register the interrupt line (i. e. bit 7 implies the 1745/1746 is on interrupt line 7).

- C. STOP 3. Enters into the A register the subtest to be executed (See Section 3). i. e. bit 3 implies execute test 3.

Enter into Q the stations to be tested, (i. e. bits 1 and 2 imply stations 1 and 2 are to be tested).

- D. STOP 4

Enter into the A register

0050₁₆ If the screen size is 13 x 80 or

0032₁₆ if the screen size is 20 x 50

Enter into the Q register

000D₁₆ If the screen size is 13 x 80 or

0014₁₆ if the screen size is 20 x 50

- E. STOP/JUMP WORD

Bit 00 must be set to enter parameters.

Bit 02 must be set to stop at end of test.

Bit 03 must be set to type out errors.

III. SUBTEST EXPLANATION

If the multistation controller (1745) and more than one station is being tested, the testing is started with the highest station number (i. e. stations 1 and 2 defined for testing, station 2 will be functioned then station 1).

The timing is done by counting the number of returns to SMM17. All wait times were calculated by the 1745-1746/210 Test running alone. Therefore, when operating in a systems mode these times can be greatly increased.

- A. TEST 0 REJECT

Purpose: This test verifies the various reject no-reject capabilities of the display subsystem.

The "reject Code" (see paragraph 5 for error typeouts) defines the sequence of operations in which an error was found.

Method:

<u>Reject Code</u>	<u>Procedure</u>	<u>Expected Result</u>
0	Copy Status Check Protect Status	Error No 2E if protected. Error No 2D if not protected.
0	Select All Possible Stations Station Numbers 1 through 15 Deselect all Stations	Type Station Numbers that could be selected, (see error Code 2F).
1	Issue Director Function of 3	Internal Reject
2	Set A = 0 Issue D. F. of 2	No Reject
3	Select Station	No Reject
4	Select Station Set Active	No Reject
5	Select Station Clear Active	No Reject
6	Deselect Station	No Reject
7	Deselect Station Set Active	No Reject
8	Deselect Station Clear Active	No Reject
9	Clear A Issue D. F. 1	No Reject
A	Select End of Operation Interrupt	No Reject
B	Select Station Interrupt	No Reject
C	Deselect Station Alert	External Reject
D	Select End of Print Interrupt	No Reject
E	Clear Interrupt Enables	No Reject
F	Deselect Station Clear Screen Wait for Not Busy	External Reject

<u>Reject Code</u>	<u>Procedure</u>	<u>Expected Result</u>
10	Deselect Station Reset Wait for Not Busy	External Reject
11	Select Station Set Active Alert	No Reject
12	Select Station Set Active Reset Wait for Not Busy	No Reject
13	Select Station Set Active Clear Screen Wait for Not Busy	No Reject
4	Clear Controller	No Reject

B. TEST 1. STATION SELECT

Purpose: This test assures that the station selected is the one that data will be transmitted to.

Method:

1. Clear Controller
2. Reset all stations selected for testing.
3. Select Station.
4. Set Active.
5. Write screen (full screen each character position containing the station number). Wait a minimum of 2 seconds.
6. Repeat steps 3 through 5 for all defined stations.
7. Reset all stations.
8. Select Station.
9. Read full screen. Wait a minimum of 2 seconds.
10. Verify data
11. Repeat steps 5 through 10 for all defined stations
12. Clear screen for all stations

C. TEST 2. END OF OPERATION INTERRUPT ON END OF MESSAGE
PURPOSE: THIS TEST VERIFIES THAT THE END OF MESSAGE CHARACTER IS READ

Method:

1. Clear controller.
2. Reset all defined stations.
3. Select station.
4. Set Active.
5. Write the end of message character.
6. Deselect station.
7. Repeat steps 3 through 6 for all defined stations.
8. Reset all defined stations.
9. Select station.
10. Set Active.
11. Enable End of Operation interrupt.
12. Read data.
13. Wait a minimum of 50 ms for Interrupt.
14. Verify Interrupt status.
15. Deselect station.
16. Verify data.
17. Repeat steps 9 through 16 for all defined stations.
18. Steps 2 through 17 are repeated until the end of message character has been written in all screen positions starting with the last character and ending with the first (Total of 1000 outputs for the 20 x 50 option or 1040 outputs for the 13 x 80 option).

D. TEST 3. PATTERN TEST

Purpose: This test verifies that the delay line will accept various bit patterns without losing or retaining bits.

Method:

1. Clear controller.
2. Reset all defined stations.

3. Select station.
4. Set active.
5. Write full screen; wait a minimum of 2 seconds.
6. Clear active.
7. Deselect station.
8. Repeat steps 2 through 7 for all defined stations.
9. Reset all defined stations.
10. Select station.
11. Set active.
12. Read full screen; wait a minimum of 2 seconds.
13. Deselect station.
14. Clear active.
15. Verify data.
16. Repeat steps 10 through 15 for all defined stations.
17. Clear screen for all defined stations.
18. Repeat steps 2 through 17 until all patterns are written, read, and verified.

PATTERNS USED IN TESTING

<u>Pattern Number</u>	<u>ASCII Characters</u>	<u>Octal Codes</u>	<u>Expected Displayed Data</u>
1	2041	0001	bA
2	3F3E	7776	?
3	2020	0000	bb
4	3F3F	7777	??
5	4747	0707	GG
6	3838	7070	88
7	5555	2525	UU
8	2A2A	5252	**

E. TEST 4. ALL CHARACTERS IN ALL POSITIONS

Purpose: This test verifies that all characters can be written in each screen position (the carriage return, 0D, is not used). The test further verifies that all illegal characters are transformed into delete codes (7F). All 256 ASCII characters are outputted for all screen positions, as defined by Figure 1.

Method:

1. Clear Controller.
2. Reset all defined stations.
3. Select station.
4. Set active.
5. Write full screen.
6. Clear active.
7. Deselect station.
8. Repeat steps 3 through 7 for all defined stations.
9. Reset all defined stations.
10. Select station.
11. Set active.
12. Read full screen.
13. Clear active.
14. Deselect station.
15. Verify data.
16. Repeat steps 10 through 15 for all defined stations.
17. Repeat steps 2 through 16 until all characters have been written, read, and verified for all screen positions. Steps 2 through 16 are repeated a total of 256 times thereby using the complete ASCII symbol set.

CHARACTER POSITION

LINE	1	2	3	4	5	6	7	8
1	00	01	02	03	04	05	06	07
2	01	02	03	04	05	06	07	08
3	02	03	04	05	06	07	08	09
4	03	04	05	06	07	08	09	0A
5	04	05	06	07	08	09	0A	0B

ASCII Symbols Outputted - First Output

CHARACTER POSITION

LINE	1	2	3	4	5	6	7	8
1	01	02	03	04	05	06	07	08
2	02	03	04	05	06	07	08	09
3	03	04	05	06	07	08	09	0A
4	04	05	06	07	08	09	0A	0B
5	05	06	07	08	09	0A	0B	0C

Figure 1. ASCII Symbols Outputted - Second Output

F. TEST 5. CARRIAGE RETURN

Purpose: This test verifies that carriage returns can be written, properly interpreted, read, and written over.

The pattern used is:

LINE 1 LINE 2 LINE 4 LINE 7 LINE 11b*

Method:

1. Clear controller.
2. Reset all defined stations.
3. Select station.
4. Set active.

Note: *implies carriage, b implies blank.

5. Write full screen of periods; wait a minimum of 2 seconds.
6. Clear active.
7. Deselect station.
8. Repeat steps 3 through 7 for all defined stations.
9. Reset all defined stations.
10. Select station.
11. Set active.
12. Write pattern (21 words); wait a minimum of 2 seconds.
13. Clear active.
14. Deselect station.
15. Repeat steps 10 through 14 for all defined stations.
16. Reset all defined stations.
17. Select station.
18. Set active.
19. Read data (21 words); wait a minimum of 2 seconds.
20. Clear active.
21. Deselect station.
22. Verify data.
23. Repeat steps 17 through 22 for all defined stations.
24. Reset all defined stations.
25. Select station.
26. Set active.
27. Write full screen of apostrophies; wait a minimum of 2 seconds.
28. Clear active.
29. Deselect station.
30. Repeat steps 25 through 29 for all defined stations.
31. Reset all defined stations.
32. Select station.
33. Set active.

34. Read full screen; wait a minimum of 2 seconds.
35. Clear active.
36. Deselect station.
37. Verify data.
38. Repeat steps 32 through 37 for all defined stations.

G. TEST 6. READY AND NOT BUSY INTERRUPT

Purpose: This test verifies that the Ready and Not Busy interrupt will be returned for a reset, clear screen, read, and write.

Method:

1. Clear controller.
2. Select station.
3. Sect active.
4. Issue reset.
5. Select Ready and Not Busy interrupt.
6. Wait a minimum of 50 ms.
7. Verify interrupt status.
8. Write one word (AB).
9. Select Ready and Not Busy interrupt.
10. Wait a minimum of 50 ms.
11. Verify status.
12. Repeat steps 8 through 11 until the full screen has been outputted.
13. Issue reset - clear loop count.
14. Select Ready and Not Busy interrupt.
15. Wait a minimum of 50 ms.
16. Verify status.
17. Read full screen minus loop count.
18. Select Ready and Not Busy interrupt.
19. Wait a minimum of 50 ms.

20. Verify status.
21. Verify data.
22. Increment loop count .
23. Repeat steps 17 through 21 until loop count equals number of words necessary to fill the screen.
24. Repeat steps 2 through 23 for all defined stations.
25. Select station.
26. Set active .
27. Select clear screen .
28. Select Ready and Not Busy interrupt.
29. Wait a minimum of 50 ms.
30. Verify status.
31. Clear active .
32. Deselect station .
33. Repeat steps 25 through 32 for all defined stations .

H. TEST 7. STATION INTERRUPT

Purpose: This test verifies that the station interrupt will occur for each defined station.

Method:

1. Clear controller.
2. Select station.
3. Set active .
4. Enable End of Operation interrupt.
5. Select clear screen .
6. Wait for interrupt .
7. Read full screen .
8. Verify .
9. Clear active .
10. Deselect station .
11. Repeat steps 2 through 10 for all defined stations .

12. Select station,
13. Set active,
14. Write the message.
CLEAR
ENTER MESSAGE
SEND
15. Clear active,
16. Deselect station,
17. Repeat steps 12 through 16 for all defined stations,
18. Enable station interrupt,
19. Wait for station to interrupt (minimum wait time 5 minutes),
20. When the interrupt is received - verify interrupt status,
21. Select station ,
22. Set active,
23. Read screen,
24. Clear active ,
25. Deselect station,
26. Search input buffer for, EOM,
27. Place station number directly behind EOM,
28. Select station,
29. Set active,
30. Write message - number of words to first EOM,
31. Clear active,
32. Deselect stations ,
33. Repeat steps 18 to 32 until all defined stations have been accounted for.

CAUTION

If the multi-station controller (1745) and more than one station is being tested, the error "send request status not cleared after a read" (Error 27) may be generated if two or more stations interrupted (send request) at about the same time.

I. END OF TEST

Purpose: This is not a test and cannot be selected or deselected by the operator. Its purpose is to write the message,

END OF TEST

on the screen of each station. Any errors encountered in this test will be indicated as belonging to test 8.

Method:

1. Clear controller.
2. Clear screen (no verify).
3. Select station.
4. Set active.
5. Write the message.
6. Write the message.
7. Deselect station.
8. Repeat steps.
9. Go to SMM to check for End of Test stop.
10. Go back and repeat all selected subtests.

IV. ROUTINES USED BY TEST

The following is a list of routines common to all subtests. They are presented so that the user may follow the sequence of operation of each subtest.

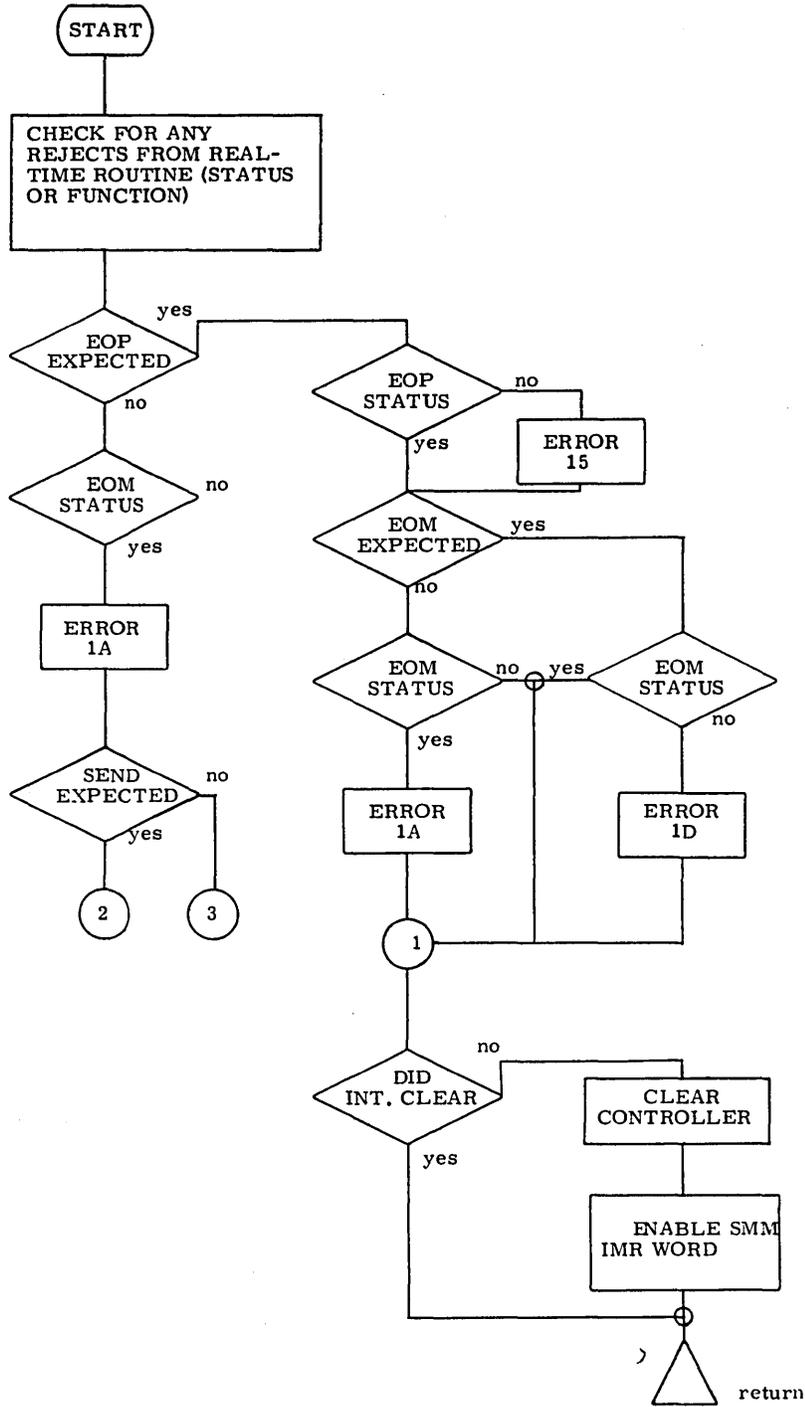
A. CLEAR ACTIVE ROUTINES

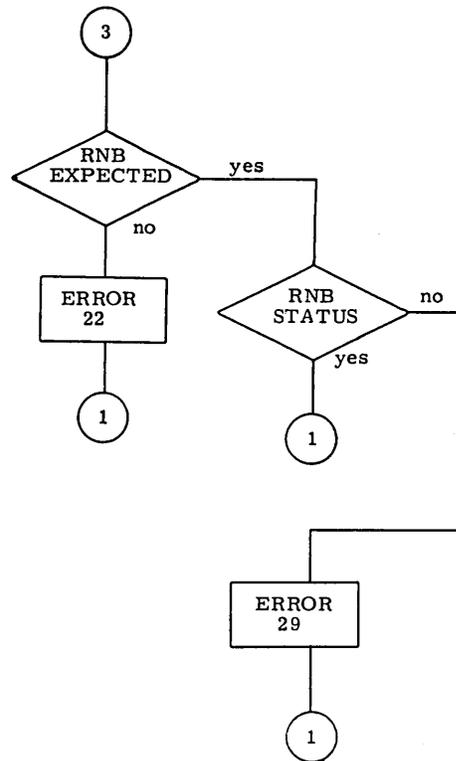
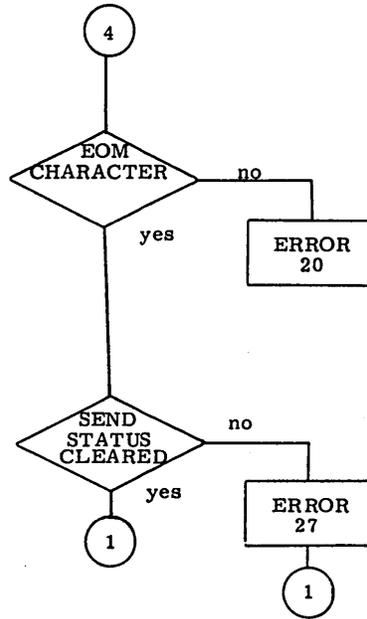
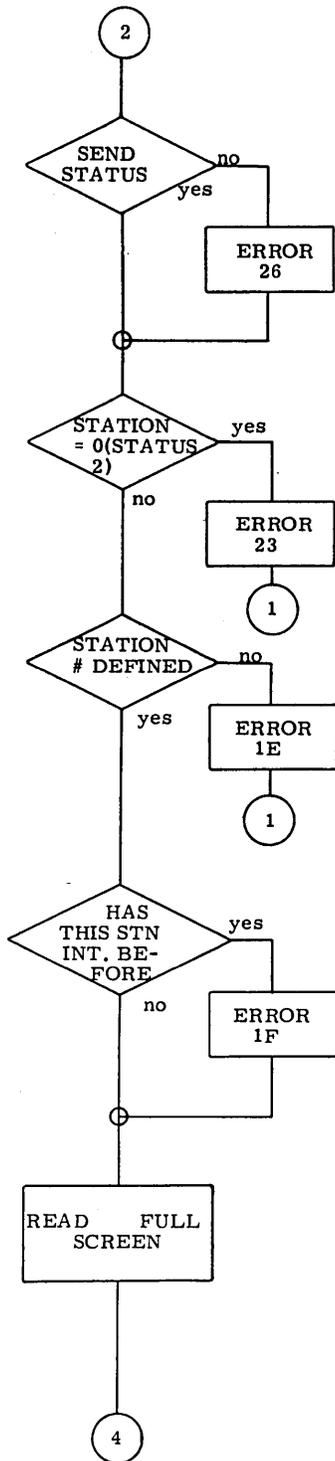
Purpose: This routine attempts to clear the station active condition.

Method:

1. Issue the clear active function.
2. Check status for no active bit.

NON REAL-TIME INTERRUPT PROCESSOR





B. CLEAR SCREEN ROUTINE

Purpose: This routine issues a clear screen function specifying the end of operation interrupt.

Method:

1. Select station.
2. Set active.
3. Select End of Operation interrupt.
4. Wait for interrupt (minimum of 50 ms).
5. Verify interrupt status.
6. Read and verify full screen, if not end of test (see paragraph 3.9).
7. Repeat steps 1 through 6 for all stations defined.

C. DESELECT STATION

Purpose: This routine attempts to deselect a previously selected station.

Method:

1. Issue a deselect station function.
2. Check status for no active bit.

D. FUNCTION ROUTINES

Purpose: These routines issue either a director code 1 or director code 2. Any rejects that are detected are immediately typed, control is then returned without reissuing the command.

E. NON REAL-TIME INTERRUPT PROCESSOR

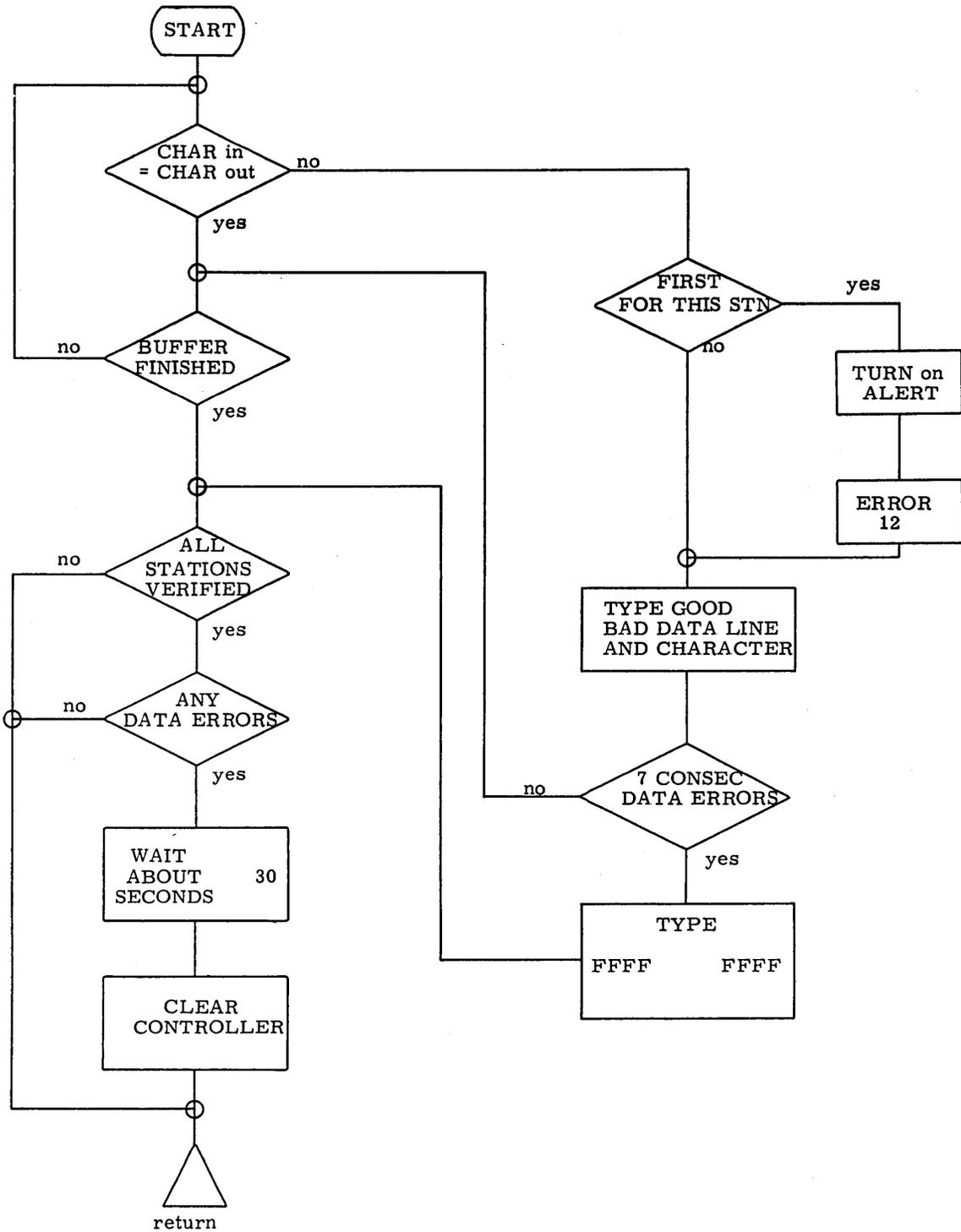
Purpose: This routine processes all non-real-time interrupts. It verifies the status received against the status expected.

Method: (See Flowchart)

F. NON REAL-TIME STATUS ROUTINE

Purpose: This routine inputs and stores both director status 1 and director status 2.

If any rejects occur, either internal or external, an error message will be typed along with the contents of A and Q when the reject occurred. After the error has been typed the routine will attempt to input the status again and will continue to do so until the reject condition disappears.



Method:

1. Input director Status 1
2. Input director Status 2
3. If no rejects, return
4. If rejects type error and repeat steps 1 through 3

G. READ ROUTINE

Purpose: This routine is used to input data from the selected station. The read routine will maintain maximum input rate provided it is not interrupted. Any internal rejects that occur will be typed immediately. Any external rejects will be allowed to continue for approximately 25 ms. When an external reject has been continuous for 25 ms, the status is sensed to see whether active has dropped. If active has dropped an error message will be typed, active will be enabled. If active has not dropped an external reject error message will be typed.

In the event a reject error message, internal, active dropped, or external, inputting will continue with the pair of characters in which the reject occurred.

H. READ-TIME INTERRUPT PROCESSOR

Purpose: This routine attempts to clear all interrupts while in an interrupt state condition.

Method:

1. Input and save status 1 and 2.
2. Issue a Clear Interrupt function.
3. Input and save status 1 and 2.
4. If the interrupt did not clear, disable the mask bit from both the interrupt save area and from SMM enable interrupt mask word.
5. Return to SMM interrupt processor.

I. REAL-TIME STATUS ROUTINE

Purpose: This routine inputs status 1 and status 2 while in an interrupt state condition.

Any rejects that occur are flagged so that they may be processed non real-time. If a reject occurs, status 1 is set up to show an interrupt is present and status 2 is set zero.

J. RESET ENTRY MARKER

Purpose: This routine issues a reset function, specifying the End of Operation interrupt.

Method:

1. Select station.
2. Set active.
3. Select End of Operation interrupt.
4. Issue reset.
5. Wait for interrupt (minimum of 50 ms).
6. Verify interrupt status.
7. Repeat steps 1 through 6 for all defined stations.

K. SET ACTIVE ROUTINE

Purpose: This routine attempts to activate a selected station.

Method:

1. Issue the set active function.
2. Check status for active bit.

L. VERIFY ROUTINE

Purpose: To verify the data inputted against that expected.

Method: (See Flowchart)

M. WRITE ROUTINE

Purpose: This routine is used to output data from the selected station. The write routine will maintain maximum output rate, provided it is not interrupted. Any internal rejects that occur will be typed immediately. Any external rejects will be allowed to continue for approximately 25 ms. When an external reject has been continuous for 25 ms, the status is sensed to see whether active has dropped. If active has dropped, an error message will be typed, the station selected and active re-enabled. If active has not dropped, an external reject error message will be typed.

In the event a reject error message, internal active dropped, or external, the outputting will continue with the pair of characters in which the reject occurred.

DIRECTOR STATUS 1

<u>Bit</u>	<u>Purpose</u>
00	Ready
01	Busy
02	Interrupt
03	Ready and not busy
04	End of operation interrupt
05	Not used
06	Not used
07	Protected
08	Not used
09	Station Print Print Request
10	Station Printing
11	End of Message
12	Active
13	Send Request
14	Printer Printing
15	Print complete interrupt

DIRECTOR STATUS 2

Bits 6 through 9 indicate the station that issued the send request interrupt; all other bits are not used.

V. ERROR CODES

Error Typeouts are of the following type:

```
1745-1746/210
TEST t STN ss ERROR ee
ST1 _____ ST2 _____
AAAA BBBB CCCC DDDD*
```

Where:

t is the subtest number
ss is the station number in which the error occurred
ee is the error code
ST1 is director status 1
ST2 is director status 2

Note:* This contains additional information about the error. Refer to the error code table for the information contained.

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
00	No end of operation interrupt on a clear screen function. Minimum wait time 50 milliseconds.	None
01	External reject on director status 1.	AAAA contents of the A register. BBBB contents of the Q register. CCCC see reject code, if error occurred in test 0, for sequence leading to the error.
02	Internal reject on director status 1.	See error code 01.
03	External reject on director status 2.	See error code 01.
04	Internal reject on director status 2.	See error code 01.
05	External reject on director function 1.	See error code 01.
06	Internal reject on director function 1.	See error code 01.
07	External reject on director function 2.	See error code 01.
08	Internal reject on director function 2.	See error code 01.
09	External reject on output of data, the reject has been continuous for more than 25 milliseconds.	AAAA = contents of A reject. BBBB = contents of Q reject.
0A	Internal reject on input of data.	See error code 09.
0B	External reject on input of data, the reject has been continuous for more than 25 milliseconds.	See error code 09.
0C	Internal reject on input of data.	See error code 09.

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
0D	An internal reject was expected but none occurred.	See error code 01.
0E	An external reject was expected but none occurred.	See error code 01.
0F	An unexpected external reject was defected (test 0 only).	See error code 01.
10	An unexpected internal reject was defected (test 0 only).	See error code 01.
11	The active status bit is not set following a set active command. (The station has previously been selected.)	None
12	Data verify error. The alarm will be turned on for the station that is in error and will remain on for a period of not less than 30 seconds following the verification of the data read from the last station. If no error occurred, the information will be displayed for a period of not less than 2 seconds.	<p>AAAA = Expected data (lower 8 bits).</p> <p>BBBB = Data received (lower 8 bits).</p> <p>CCCC = The line in which the error occurred (starting with line 1).</p> <p>DDDD = The character which is in error (starting with character 1).</p> <p>Up to 7 such errors will be typed until it is assumed that the data block is bad. At this point, the verify will be aborted. This is signified by typing:</p> <p>AAAA = FFFF</p> <p>BBBB = FFFF</p> <p>CCCC = blank</p> <p>DDDD = blank</p>
13	The interrupt status bit is still set following a clear interrupt command.	None

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
14	The station active bit is set following a clear active command.	None
15	The end of operation status bit is not set following an end of operation interrupt.	None
16	The controller has been busy for more than 50 milliseconds.	None
17	No end of operation interrupt has occurred for a reset command, minimum wait time 50 milliseconds.	None
18	No end of operation interrupt has occurred for a data input containing an end of message character. Minimum wait time 50 milliseconds.	None
19	Active status dropped while outputting data (continuous external rejects for 25 milliseconds before status is checked).	None

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
1A	Unexpected end of message status has been detected.	None
1B	Active status dropped while inputting data (continuous external rejects for 25 milliseconds before status is checked).	None
1C	Unexpected end of operation status has been detected.	None
1D	No end of message status is detected following the end operation interrupt for an end of message character minimum wait time 50 milliseconds.	None
1E	An unexpected send request interrupt has been detected. Bits 6 through 9 of director status 2 contain a station address that was not defined in parameter entry.	AAAA = The station address that gave the unexpected interrupt. BBBB = 0.
1F	A send request interrupt has been detected from a station that has already given a send request interrupt.	See error code 1E.
20	No end of message character can be found in the input buffer following a read on send request interrupt.	None
21	No send interrupt(s) have been detected in the past 5 minutes (minimum time).	AAAA = the bits represents the stations that have not replied with a send interrupt.

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
22	An unidentified interrupt has occurred.	AAAA = Interrupt that was expected. 00 = End of operation on clear screen. 17 = End of operation on reset. 18 = End of operation on end of message. 21 = Send Interrupt.
23	Director status 2, bits 6 through 9 are zero, following a send request interrupt.	None
24	Not Used	
25	Send request status is present when no send interrupt is expected.	None
26	The send request status is not present for an expected send interrupt.	None
27	Send request status not cleared after a read. Also see caution for test 7.	None
28	No ready and not busy interrupt after a write. Minimum wait time 50 milliseconds.	None
29	Ready and not busy status is not present on a ready and not busy interrupt.	None
2A	The ready and not busy interrupt did not occur after a read. Minimum wait time 50 milliseconds.	None
2B	The ready and not busy interrupt did not occur after a reset minimum wait time 50 milliseconds.	None

<u>Error Number</u>	<u>Explanation</u>	<u>Additional Information</u>
2C	The ready and not busy interrupt did not occur after a clear screen. Minimum wait time 50 milliseconds.	None
2D	This is not an error condition. It defines the position of the PROTECT switch through the status. The PROTECT switch is not on. Also see test 0.	AAAA Not Used BBBB Not Used CCCC Zero
2E	This is not an error condition. It defines the position of the PROTECT switch. The PROTECT switch is on. Also see test 0.	See 2D
2F	This is not an error condition. It defines the stations that could be selected.	AAAA Not Used BBBB Not Used CCCC Zero DDDD Contains the stations that could be selected (i. e., bit 2 set implies station 2 could be selected). Also see test 0 (paragraph 3.1).

1745-2/211-3 DISPLAY STATION TEST

(DDT01D Test No. 1D)

I. REQUIREMENTS

A. HARDWARE

The following equipment will be required to properly execute this test:

1. 17X4 Basic Computer
2. 17X5 Interrupt Data Channel
3. 1745-2 Display Station Controller
4. A maximum of (12) 211-3 Display/Entry Stations
5. Basic, Edit, or no keyboard associated with 211-3

B. SOFTWARE

This test is designed to run under the following software system:

1700 Systems Maintenance Monitor.

II. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Hardware

The 1745-2 display station does not check any features pertaining to a typewriter station.

2. Software

Interface between the 1745-2 display station test and the 1700 system maintenance monitor is established whenever a time out is required. Therefore, when operating in a system mode, the run time of a successful pass is increased in proportion to the number of tests referenced.

B. LOADING PROCEDURES

1. The test is loaded in accordance with 1700 SMM directives.
2. The test may be re-started at initial address.

C. PARAMETERS

Parameters are entered at the beginning of the test or if bits 0 and 10 are set, re-entered after completion of a test pass.

Parameter entry requires four stops.

Stop 1 - (A) = ID Word (Overflow is lit)

(Q) = Stop-Jump Parameter

Stop 2 - (A) = Equipment address for direct input of Status 1 (W = 0, 2, 7, or

C--E = Equipment address--S = 0--D = 1)

(Q) = Interrupt Line Number

(Bit 4 = Line 4, Bit 7 = Line 7, etc.)

Stop 3 - (A) = Section/s to Run

(Bit 1 = Section 1, Bit 2 = Section 2, etc. up to Bit 13) (Bit 0 - Not used)

(Q) = Station Address/es to Test

(Bit 1 = Station 1, Bit 2 - Station 2, etc., up to Bit 12) (Bit 0 - Not used)

Stop 4 - (A) = 50 (If the number of character per line is 80_{10})

32 (If the number of character per line is 50_{10})

(Q) = D (If the number of lines is 13_{10})

= 14 (If the number of lines is 20_{10})

D. MESSAGES

Each time the test is entered, the test will identify itself by typing:

DDT01D, 1745-2 Display Test

IA = XXXX, FC = XX

III. TEST DESCRIPTION

A. GENERAL

Sections are executed in numerical order, beginning with the lowest numbered section selected. All selected sections are executed to one station prior to execution to other selected stations.

Stations are tested with the lowest numbered selected station, progressing to the highest numbered selected station.

B. SECTION EXPLANATION

1. Section 1 - Reject-Reply Run Time - L. T. 1 Sec.

This section verifies the various reject . . . No reject capabilities of the display sub-system. A function is sent to a selected/de-selected station after which a reply or a reject to the function is expected. When a reply is expected, a status check is done to ensure the function was performed except for End of Operation, Station, and Data interrupts.

The various test sequences and expected result are listed as follows:

<u>Operation</u>	<u>Expected Result</u>
a. Clear controller	Reply
b. Director Function 2 - No Function	External Reject
c. Select station	Reply
d. Clear Memory - Re-set	External Reject
e. Re-set marker	External Reject
f. Clear controller	Reply
g. Select station	Reply
h. Set station active	Reply
i. De-select station	Reply
j. Set station active	External Reject
k. Clear controller	Reply
l. Director Function 1 - No Function	Reply
m. Enable End-of-Operation interrupt	Reply
n. Enable Station interrupt	Reply
o. Write Terminate	Reply
p. Enable Data interrupt	Reply
q. Clear Interrupt Enables	Reply
r. Alert	External Reject
s. Clear Memory - Re-set entry marker	External Reject
t. Re-set entry marker	External Reject
u. Select station	Reply

<u>Operation</u>	<u>Expected Result</u>
v. Set station active	Reply
w. Re-set entry marker	Reply
x. Clear memory - Re-set	Reply
y. Clear Active	Reply
z. Clear controller	Reply
2. Section 2 - Station Addressing Run Time = L. T. 1 Sec.	
<p>This section verifies that the station selected is the one that data will be transmitted to and from. The station is selected, a full screen is written with the selected station number, and the screen is then read and verified.</p> <p>The following sequence is used in this test section:</p>	
<ul style="list-style-type: none"> a. Set up full screen data buffer with station address + space/EOM. b. Clear controller. c. Select station. d. Set station active. e. Re-set the entry marker to the first character position. f. Output complete buffer using direct I/O transfer. g. De-select station. h. Select station. i. Set station active. j. Re-set entry marker. k. Read a full screen of data using direct I/O transfer. l. De-select station. m. Compare data received with data transmitted. n. Delay for visual verification. o. End section. 	
3. Section 3 - Interrupts Run Time = L. T. 2 Minutes	
<p>This section is used to check the interrupt system under normal data transfer conditions.</p>	

To verify the End-of-Operation interrupt End-of-Message characters are written in every screen position, the EOP interrupt is enabled and the EOM is read in every character position.

The following sequence is used to test this section:

- a. Set up data buffer consisting of blank codes until EOM required.
 - b. Clear controller.
 - c. Select station.
 - d. Set station active.
 - e. Reset the entry marker to the first character position.
 - f. Output Data Buffer.
 - g. De-select station.
 - h. Enable End-of-Operation interrupt.
 - i. Select station.
 - j. Set station active.
 - k. Re-set entry marker.
 - l. Read data until EOM character position.
 - m. Process interrupt.
 - n. Enable End-of-Operation interrupt.
 - o. Send Write Terminate.
 - p. Process interrupt.
 - q. Repeat entire sequence until EOM written and read in every character position.
 - r. End section.
4. Section 4 - Delay Line Pattern Run Time = L. T. 1 Second

This section verifies that the delay line will accept various bit patterns without dropping or picking up bits. The delay line patterns used are as follows.

<u>ASCII Code (HEX)</u>	<u>Alpha-numeric Display</u>	
2041	Space	A
3F3E	Question Mark	Greater Than
2020	Space	Space
3F3F	Question Mark	Question Mark
4747	G	G
3838	8	8
5555	U	U
2A2A	*	*

The following sequence is used in this test section:

- a. Set up full screen data buffer with delay line pattern.
- b. Clear controller.
- c. Select station.
- d. Set station active.
- e. Re-set the entry marker to the first character position.
- f. Output complete data buffer using direct I/O transfer .
- g. De-select station .
- h. Select station .
- i. Set station active.
- j. Re-set entry marker .
- k. Read a full screen of data using direct I/O transfer.
- l. Repeat K 10 times per pattern.
- m. De-select station,
- n. Compare data received with data transmitted .
- o. Delay for visual inspection.
- p. Repeat the entire sequence until all patterns have been written, read and verified.
- q. End section .

5. Section 5 - All Characters in all Positions Run Time = 2 Minutes

This section verifies that almost all characters may be written in all screen positions. Special characters such as the new line code, special edit characters, and other similar characters are not written on the screen.

NOTE

Each character is written as a full data buffer.

The following sequence is used for each character:

- a. Set up a full screen data buffer with current character + space/EOM.
- b. Clear controller.
- c. Select station.
- d. Set station active.
- e. Re-set the entry marker to the first character position.
- f. Output complete data buffer using direct I/O transfer.
- g. De-select station.
- h. Select station.
- i. Set station active.
- j. Re-set entry marker.
- k. Read a full screen of data using direct I/O transfer.
- l. De-select station.
- m. Compare data received with data transmitted.
- n. Delay for visual inspection.
- o. Repeat the entire sequence until all characters have been used.
- p. End section.

6. Section 6 - New Line Run Time = L. T. 1 Second

This section verifies that new line codes can be written, properly interpreted, read, and written over again. The pattern used is:

Line b1 * Line b2** Line b4*** Line b7**** Line b11

* Implies a new line code

b Implies a space code

The following sequence is used in this test section:

- a. Set up full screen data buffer consisting of periods.
 - b. Clear controller.
 - c. Select station.
 - d. Set station active.
 - e. Re-set the entry marker to the first character position.
 - f. Output complete data buffer using direct I/O transfer .
 - g. De-select station.
 - h. Select station.
 - i. Set station active .
 - j. Re-set entry marker.
 - k. Read a full screen of data using direct I/O transfer.
 - l. De-select station.
 - m. Compare data received with data transmitted.
 - n. Delay for visual verification.
 - o. Set up data buffer with new line pattern.
 - p. Repeat steps b through n.
 - q. Set up data buffer consisting of exclamation points .
 - r. Repeat steps b through n.
 - s. End section .
7. Section 7 - Echo Test Run Time = Up to 5 Minutes

This section verifies the capability of each station to generate a station interrupt, interpret an end-of-message code on a send request, and correct receipt of operator initiated messages. The operator clears the screen on command, enters any message from the keyboard, and depresses the send key.

The computer responds to the send interrupt by reading the screen, clearing the screen, and writing back the message entered by the operator.

The following sequence is used in this test section:

- a. Set up data buffer containing operator message .
- b. Clear controller .

- c. Select station.
- d. Set station active.
- e. Re-set the entry marker to the first character position.
- f. Output Data Message.
- g. De-select station.
- h. Enable station interrupt.
- i. Wait for interrupt to occur.
- j. Process Station interrupt.
- k. Select station.
- l. Set station active.
- m. Re-set entry marker.
- n. Read a full screen of data.
- o. Check for EOM code.
- p. Clear memory and re-set entry marker.
- q. Delay for verification.
- r. Write message received.
- s. Delay for verification.
- t. End section.

8. Section 8 - Re-set/Skip With Escape Run Time = L. T. 1 Second

This section writes a buffer of escape codes followed by re-set and skip codes in an order which will put escape, re-set, and skip codes in each of the four character positions in the interface buffer.

The buffer of data written is as follows:

ERES ESES 1ERE SES2 ERER ES3E R4ER

E - Implies Escape Code

S - Implies Skip Code

R - Implies Re-set Code

This data is displayed on the screen as: 4321, with the entry marker at the re-set position.

- a. Set up data pattern consisting of re-set/skip/escape codes.
- b. Clear controller.
- c. Select station.
- d. Set station active.
- e. Re-set entry marker to first character position.
- f. Output complete data buffer consisting of direct I/O transfer.
- g. De-select station.
- h. Select station.
- i. Set station active.
- j. Re-set entry marker.
- k. Read a full screen of data using direct I/O transfer.
- l. De-select station.
- m. Compare data to 4321 pattern.
- n. Delay for visual inspection.
- o. End section.

9. Section 9 - Line Skip Function With Escape Run Time = L, T, 1 Second

This section will check the Line Skip edit function feature, by sending successive line skip codes preceded by escape codes until the entry marker is at the re-set position. Two characters (1W) precede the edit characters. When a Read is performed after the Write, the Read buffer should read the first two characters sent.

The following sequence is in this test section:

- a. Set up data buffer with two characters and line skips/escapes.
- b. Clear controller.
- c. Select station.
- d. Set station active.
- e. Re-set entry marker to first character position.
- f. Output complete data buffer using direct I/O transfer.
- g. De-select station.
- h. Select station.

- i. Set station active.
- j. Read two characters of data using direct I/O transfer .
- k. De-select station.
- l. Compare data to 1W (Output Word) .
- m. Delay for visual inspection.
- n. End section.

10. Section 10 - Carriage Return Without Escape Run Time = L. T. 1 Second

This section verifies that carriage return codes, not preceded by an escape may be written on the screen in all character positions.

A full screen of carriage return codes, except for a CR in the first two positions is sent.

The following sequence is used in this test section:

- a. Set up data buffer with two characters (CR) and carriage return codes .
- b. Clear controller .
- c. Select station .
- d. Set station active .
- e. Re-set the entry marker to the first character position .
- f. Output complete data buffer using direct I/O transfer .
- g. De-select station .
- h. Select station .
- i. Set station active .
- j. Re-set entry marker .
- k. Read a full screen of data using direct I/O transfer .
- l. De-select station .
- m. Compare data received with data transmitted .
- n. Delay for visual verification .
- o. End section .

11. Section 11 - Status Switches Run Time = Not more than 5 Minutes

This section verifies that the four status switches may be set and properly interpreted by the computer. This section will require operator action for proper execution.

Each pass through this section instructs the operator to set a status switch and depress the send key when completed.

The operator message used is:

```
CLEAR SCREEN
SET STATUS SWITCH 0X (X = SWITCH NUMBER)
SEND
```

The following sequence is used in this test section:

- a. Set up data buffer containing operator message.
- b. Clear controller .
- c. Select station.
- d. Set station active .
- e. Re-set the entry marker to the first character position.
- f. Output data message .
- g. De-select station.
- h. Enable Station interrupt.
- i. Wait for interrupt to occur .
- j. Process Station interrupt .
- k. Select station.
- l. Set station active .
- m. Re-set entry marker .
- n. Read a full screen of data using direct I/O transfer .
- o. Ensure data buffer contains all blank codes .
- p. Check status 2 for proper switch set .
- q. Update status switch number .
- r. Repeat entire sequence for each status switch .
- s. End section .

12. Section 12 - Tab Access/Tab Protect Run Time = L. T. 1 Second

This section verifies that the Tab Access and Tab Protect function codes are properly interpreted on Read and Write operations. A portion of the screen is protected and then given an access code for attempted Write screen operations. The data is then read for comparison.

The following sequence is used in this test section:

- a. Set up data buffer containing asterisk codes.
- b. Clear controller.
- c. Select station.
- d. Set station Active.
- e. Re-set the entry marker to the first character position.
- f. Output full screen buffer.
- g. De-select station.
- h. Set up start tab buffer as follows:
Escape/Line Skip
Escape/Line Skip
A/Start Tab
C/C
C/C
End Tab/D
- i. Output start tab buffer.
- j. Repeat steps b through e.
- k. Set up tab access buffer as follows:
Asterisk/Escape
Line Skip/Escape
Line Skip/Tab Access
- l. Output tab access buffer.
- m. Repeat steps b through e.
- n. Read buffer indicated in step h.
- o. Compare data.

p. Set up tab protect buffer as follows:

Asterisk/Escape
Line Skip/Escape
Line Skip/Tab Protect

q. Output tab protect buffer .

r. Repeat steps b through e.

s. Read data .

t. Compare buffer to following:

A/Tab Protect
End Tab/D
Clear Screen

u. End section .

13. Section 13 - Troubleshoot Section Run Time = N/A

This section provides small loops for function, status and data transmission for use with a monitoring device such as an oscilloscope. The operator, after selecting the section, enters parameters as follows:

NOTE

Only one stop may contain data.

Stop 1 - Write A = Data Character/s

 Screen Q = Station Address (Bit 2 = Station 2, etc.)

- 1) Ensure A and Q registers clear if data loop not desired.
- 2) Enter into the A registers any data desired for transmission.
- 3) Enter into the Q register the station address associated with the binary bit.
- 4) The segment will continually output the data in the A register.
- 5) Exit from the section is accomplished by clearing the A and Q register and enabling Run mode.

Stop 2

Function

A = Any Function Code

Q = The equipment address plus director bits
for outputting the function.

1. Ensure A & Q registers clear if function loop not desired.
2. Enter into the A register any valid function code (function 1 or 2).
3. Enter into the Q register the equipment address necessary for outputting the function from the A register.
4. The segment will continuously output the function code in A. Status is not performed.
5. A count of the number of rejects encountered is available at location specified by mnemonic REJ13OUT for external rejects and mnemonic REJ131N for internal rejects.
6. Exit from this section is accomplished as stated in Stop 1, Step 5.

Stop 3

Status

A = Enter any value greater than zero

Q = Equipment address for input of status
plus director bits

1. Ensure A & Q registers cleared if status loop not desired.
2. Set A register non-zero
3. Enter into the Q register the equipment code necessary to input to A the status 1 or 2 code.
4. The section will continually input the controller status into A.
5. The status word is stored at location specified by mnemonic Act 13.
6. Exit from this section is accomplished as stated in Stop 1, Step 5.

Stop 4

Read Screen

1. Ensure A and Q registers cleared if read loop not desired.
2. Center into the A register the character/s to read.
3. Center Q register binary station address
4. The section will continually input the character/s written on the screen.
5. Exit from this section is accomplished as stated in stop 1, Step 5.

IV. ERROR

A. Messages

Error messages are standard SMM17 format.

A	Q	A	Q	A Q - A Q
1DX8	STOP/JUMP	YYZZ	RTN Address	Data

X = Number of Stops

YY = Section Number

ZZ = Error Number

Data = Addition Information

The section number and return address give the approximate location in the test where the error occurred.

B. Error Codes

<u>Error Code</u>	<u>Meaning</u>	<u>Additional Information</u>
02	Not Used	
03	External Reject on Director function	A = Function Error occurred on Q = Equipment Address
04	Internal Reject on Director function	Same as Error 03
05	Reply on Director function (Expected external reject)	Same as Error 03
06	Internal Reject on Director function	Same as Error 03
07	Busy does not drop after a reset function	None
08	Status (1) error NOTE: (Status is checked after most functions are performed -if a bit remains set/or does not set, a status error results, --this is the only <u>error condition associated with function/status outside of rejects and interrupts.</u>)	A = Expected Status Q = Received Status
09	External Reject on Director Status 1	A = Expected Status Q = Zero
0A	Internal Reject on Director Status 1	Same as Error 09
0B	External Reject on output	A = Output character/s Q = Zero

<u>Error Code</u>	<u>Meaning</u>	<u>Additional Information</u>
0C	Internal Reject on output	Same as Error 0B
0D	External Reject on input	A = Input Character/s Q = Zero
0E	Internal Reject on input	Same as Error 0D
0F	An expected interrupt did not occur	A = 00X x = Number corresponding to non-received interrupt 1 = No Data interrupt 2 = No EOP interrupt 3 = No EOP on EOM interrupt 4 = No Station interrupt
10	The interrupt was set but no interrupt occurred	Same as Error 0F
11	Status 2 error (see Note Error 8)	Same as Error 08
12	External Reject on Director Status 2	Same as Error 09
13	Internal Reject on Director Status 2	Same as Error 09
14	Data received did not agree with data expected	A = Expected Character/s Q = Received Character/s A = Address of Expected Character Q = Address of Received Character
15	An end-of-message code was not read on input data after a Send request	None
16	An interrupt occurred but the interrupt bit (Bit 02) was not set	A = Expected Interrupt Status Q = Received Status Interrupt
17	The interrupt bit remained set after a clear interrupt function	Same as Error 16
18	An interrupt occurred that was not selected or expected	Same as Error 16

<u>Error Code</u>	<u>Meaning</u>	<u>Additional Information</u>
19	Data was not read from a protected area after a tab access performed	
20	Data read from a protected area, a tab access was not performed, prior to the read operation	

1700/8000 DATA TRANSFER BUFFER,
8049 DISPLAY CONTROLLER, 211 DISPLAY STATION
(DTBA10 Test No. 10)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. The test must be run alone. It does not return control to SMM.
2. The interrupt lines selected at the parameter stop must match the physical connections of the interrupt cables.
3. The SEND key on the display station keyboard must be pressed in sections 3 and 5 of the test.
4. The CLEAR and SEND keys should not be pressed during sections 1, 2, 4, and 6.
5. The SEND key must be pressed five times in section 3, but section 5 may be terminated by entering two periods as the first two characters of the input message. Otherwise, the SEND key must be pressed twenty times in section 5.
6. The patterns output in sections 4 and 6 should appear stationary except for the motion of the entry marker. If the patterns move or one of these sections hangs, data is being lost upon output probably due to a bad Not Reject card in the DTB.

B. LOADING PROCEDURE

1. Call as external test number 10 under SMM17.
2. Test can be restarted from initial address after loading.

C. PARAMETERS

If bit 0 of the SMM stop/jump word is set at the start of the test, three stops occur.

1. First stop, A = 1031, Q = stop/jump word.
2. Second stop, A = 007E, Q = 0038. The bits in A specify the sections to be executed (pre-stored parameter specifies sections 1, 2, 3, 4, 5, and 6). Q is the symbol code of the symbol to be output in section 6 (pre-stored parameter specifies H).

3. Third stop, A = 4000, Q = 8000. The bit in A specifies the 1700/8000 DTB End of Operation interrupt line, i. e., connection of J20 cable (pre-stored parameter specifies interrupt line 14). The bit in Q specifies the Interrupt 40 line, i. e., connection of J40 cable (pre-stored parameter specifies interrupt line 15).

D. MESSAGES

No timeouts occur if bit 8 of the stop/jump word is set.

1. Test title and initial address timeout

DTBA10, 1700/8000, 8049-A, 211 DISPLAY TEST
IA = XXXX, FC = XX

XXXX is the initial address of the test

2. Start of section 3 (this message is output on the display screen, not the typewriter).

PRESS SEND KEY

3. Start of section 5 (output on display, not typewriter)

ECHO TEST

4. End of test (typed out)

A	Q	A	Q
1024	Stop/Jump Word	Pass Number	Return Address

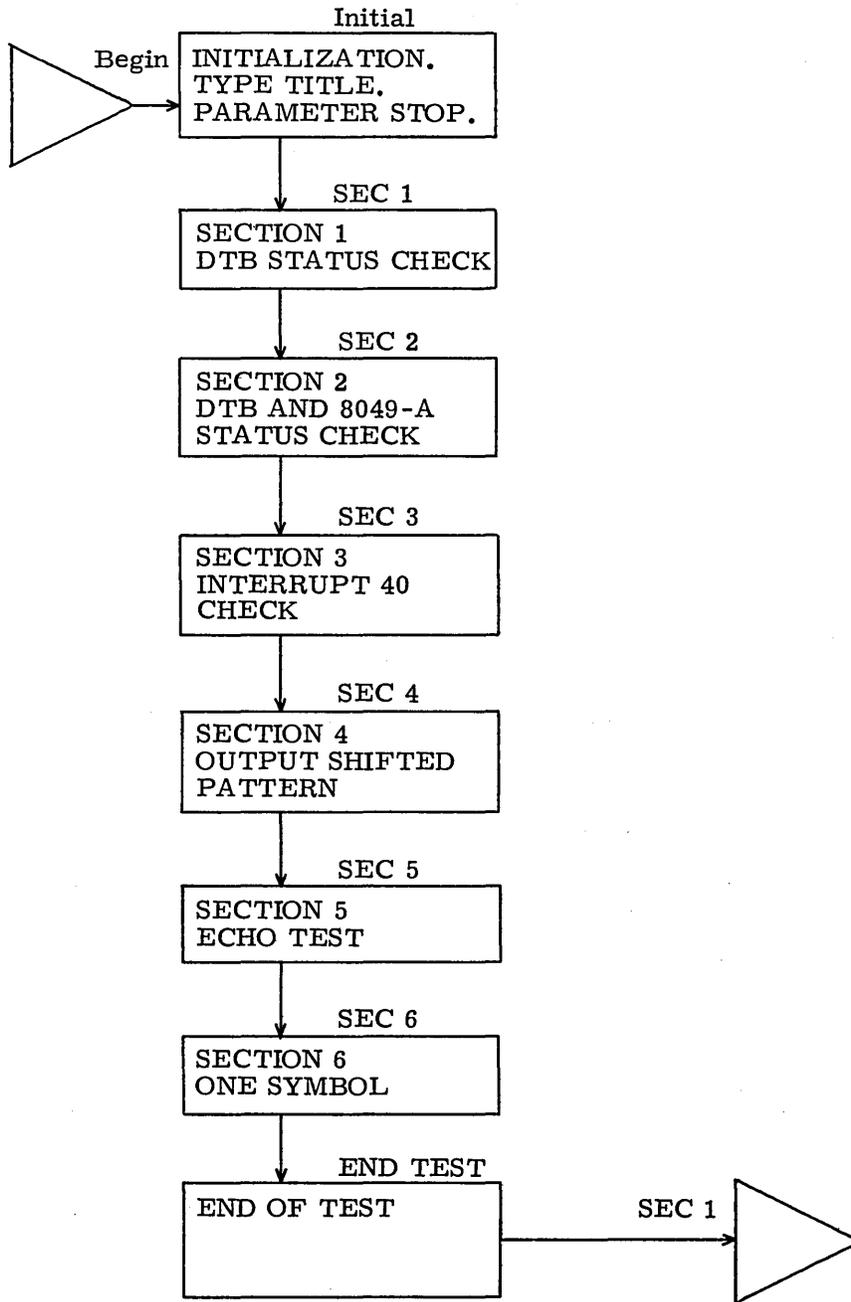
E. ERROR MESSAGES

All error messages are in the SMM17 format. The return address tells where the error occurred.

<u>Error Code</u>	<u>Meaning</u>
01	Insufficient memory for test.
02	Equipment address error (operator error). Test must be called again.
03	Parameter error (operator error). Parameters must be selected again.
04	Unexpected internal reject.
05	Unexpected external reject.

II. DESCRIPTION

A. BLOCK DIAGRAM



B. DETAILED TEST DESCRIPTION

0. Initialization

- a. (INITIAL). Inhibit interrupts.
- b. Determine initial address. Type title and initial address.
- c. Determine whether equipment address is legal. Error code 2 if not.
- d. (INITA). Determine whether memory is large enough for test. Error code 1 if not.
- e. Parameter stop. Error code 3 if parameter error.

1. Section 1 - DTB STATUS CHECK

- a. Section 1, Loop 1
 - 1) (SEC1). Input status.
 - 2) Expect reply (hang on reject), Error code 4 (internal reject) or 5 (external reject) if not.
 - 3) (S11A). Expect zero status, Error code 6 (unexpected DTB status) if not.
 - 4) (S11B). Loop to 1) 100 times. Continue looping if Stop/Jump bit 4 is set.
- b. Section 1, Loop 2
 - 1) (LOOP12). Clear controller.
 - 2) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 3) (S12A). Get DTB status.
 - 4) Expect zero status, Error code 6 if not.
 - 5) (S12B). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- c. Section 1, Loop 3
 - 1) (LOOP13). Clear interrupt.
 - 2) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 3) (S13A). Get DTB status.
 - 4) Expect zero status, Error code 6 if not.
 - 5) (S13B). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.

- d. Section 1, Loop 4
 - 1) (LOOP14). Print.
 - 2) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 3) (S14A). Get DTB status.
 - 4) Expect zero status, Error code 6 if not.
 - 5) (S14B). Print.
 - 6) Expect external reject, Error code 4 or 7 (unexpected reply) if not.
 - 7) Get DTB status.
 - 8) Expect zero status, Error code 6 if not.
 - 9) (S14C). Delay 75 microseconds.
 - 10) Print.
 - 11) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 12) (S14D). Delay 75 microseconds.
 - 13) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- e. Section 1, Loop 5
 - 1) (LOOP15). Print, hang on reject.
 - 2) Clear controller.
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S15A). Print.
 - 5) Expect external reject, Error code 4 or 7 if not.
 - 6) Get DTB status.
 - 7) Expect zero status, Error code 6 if not.
 - 8) (S15B). Delay 75 microseconds.
 - 9) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- f. Section 1, Loop 6
 - 1) (LOOP16). Set all bits in A except 0, 1, and 7. Set Director bit in Q.
 - 2) Output from A (undefined functions in A).
 - 3) Expect external reject, Error code 4 or 7 if not.
 - 4) Get DTB status.

- 5) Expect zero status, Error code 6 if not.
 - 6) (S16A). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- g. Section 1, Loop 7
- 1) (LOOP17). Set Director bit in Q and bit 1 in Q.
 - 2) Input to A.
 - 3) Expect external reject, Error code 4 or 7 if not.
 - 4) Get DTB status.
 - 5) Expect zero status, Error code 6 if not.
 - 6) (S17A). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
 - 7) Repeat steps 1) through 6) with each of bits 2 through 6 set in Q (instead of bit 1 in Q).
- h. Section 1, Loop 8
- 1) (LOOP18). Set all bits in A. Set director bit in Q.
 - 2) Output (all functions).
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S18A). Repeat steps 1) through 3).
 - 5) (S18AA). Set Director bit and Continue bit in Q.
 - 6) Input to A (DTB status input).
 - 7) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 8) (S18AB). Expect zero status, Error code 6 if not.
 - 9) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- i. Section 1, Loop 8A
- 1) (LUP18A). Set Q01, clear Q00. Clear A. Set interrupt mask for EOP interrupt. Enable interrupts.
 - 2) Output (to connect to peripheral device number 00).
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S18A1). Get DTB status.
 - 5) Expect Busy status, Error code 6 if not.
 - 6) Delay 39 microseconds.
 - 7) Expect no EOP interrupt, Error code 8 if interrupt.

- 8) (S18A2). Clear controller.
 - 9) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 10) (S18A3). Get DTB status.
 - 11) Expect Busy status, Error code 6 if not.
 - 12) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- j. Section 1, Loop 9
- 1) (LOOP19). Initialize EOP interrupt (set interrupt mask, enable interrupts).
 - 2) Output from A with Q00 and Q01 set (to set equipment select flip-flop).
 - 3) Expect external reject (hang on reply or internal reject), Error code 4 or 7 if not.
 - 4) Set Q15 and Q01.
 - 5) Output.
 - 6) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 7) (S19A). Get DTB status.
 - 8) Expect busy, Error code 6 if not.
 - 9) (S19B). Delay 30 microseconds.
 - 10) Expect no EOP interrupt, Error code 8 if interrupt.
 - 11) (S19C). Get DTB status.
 - 12) Expect busy, Error code 6 if not.
 - 13) (S19D). Clear interrupt.
 - 14) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 15) (S19E). Get DTB status.
 - 16) Expect Busy, Error code 6 if not.
 - 17) (S19EA). Set Q15 and Q02.
 - 18) Output.
 - 19) Expect external reject, Error code 4 or 7 if not.
 - 20) (S19EB). Set Q15 and Q01.
 - 21) Output.
 - 22) Expect external reject, Error code 4 or 7 if not.

- 23) (S19F). Clear controller.
 - 24) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 25) (S19G). Get DTB status.
 - 26) Expect Busy, Error code 6 if not.
 - 27) (S19H). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- k. Section 1, Loop 9A
- 1) (LUP19A). Set Q01. Load A with 700 hex (=3400 octal).
 - 2) Output (connect 8049 and select input mode).
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S19A1). Delay 30 microseconds.
 - 5) Set Q15 and Q02.
 - 6) Output (request input of status from 8049).
 - 7) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 8) (S19A2). Delay 30 microseconds.
 - 9) (S19A3). Clear Q00.
 - 10) Input (8049 status).
 - 11) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 12) (S19A4). Set Q15 and Q02.
 - 13) Output (request input to cause disconnect).
 - 14) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 15) (S19A5). Delay 30 microseconds (to give Disconnect FF in 8049 time to set).
 - 16) Clear controller (to clear Input FF in DTB, thus dropping input request signal and clearing Disconnect FF in 8049).
 - 17) Clear controller (to clear Interrupt FF and Disconnect FF in DTB).
 - 18) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- l. Section 1, Loop 10
- 1) (LOOP1A). Initialize EOP interrupt.
 - 2) Set Q00 and Q01
 - 3) Input (to set Equipment Select FF).

- 4) Expect external reject (hang on reply or internal reject), Error code 4 or 7 if not.
- 5) Set Q15 and Q02.
- 6) Output (request input).
- 7) Expect reply (hang on reject), Error code 4 or 5 if not.
- 8) (S1AA). Get DTB status.
- 9) Expect busy, Error code 6 if not.
- 10) (S1AB). Delay 30 microseconds.
- 11) Expect no EOP interrupt, Error code 8 if interrupt.
- 12) (S1AC). Get DTB status.
- 13) Expect busy, Error code 6 if not.
- 14) (S1ACA). Set Q15 and Q01.
- 15) Output.
- 16) Expect external reject, Error code 4 or 7 if not.
- 17) (S1ACB). Set Q15 and Q02.
- 18) Output.
- 19) Expect external reject, Error code 4 or 7 if not.
- 20) (S1AD). Clear controller.
- 21) Expect reply (hang on reject), Error code 4 or 5 if not.
- 22) (S1AE). Get DTB status.
- 23) Expect Busy, Error code 6 if not.
- 24) (S1AF). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.

m. Section 1, Loop 11

- 1) (LOOP1B). Set Equipment Select FF.
- 2) Set Q15 and Q02.
- 3) Output (input request).
- 4) Expect reply (hang on reject), Error code 4 or 5 if not.
- 5) (S1BA). Get DTB status.
- 6) Expect Busy, Error code 6 if not.
- 7) (S1BB). Clear Q00.

- 8) Input (8049 status).
 - 9) Expect external reject, Error code 4 or 7 if not.
 - 10) Clear controller.
 - 11) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 12) (S1BC). Get DTB status.
 - 13) Expect busy, Error code 6 if not.
 - 14) (S1BD). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- n. Section 1, Loop 12
- 1) (LOOP1C). Set Q01. Load A with 700 hex (-3400 octal).
 - 2) Output (connect to 8049).
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S1CA). Get DTB status.
 - 5) Expect Busy, Error code 6 if not.
 - 6) (S1CB). Delay 30 microseconds.
 - 7) (S1CC). Get DTB status.
 - 8) Expect Interrupt status and Not Busy, Error code 6 if not.
 - 9) (S1CD). Clear controller.
 - 10) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 11) (S1CE). Get DTB status.
 - 12) Expect zero, Error code 6 if not.
 - 13) (S1CF). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- o. End of Section 1
- 1) Clear controller.
 - 2) Stop if Stop/Jump Bit 1 is set.
 - 3) Repeat Section 1 if Stop/Jump bit 5 is set.
2. Section 2 - DTB AND 8049-A STATUS
- a. Section 2, Loop 1 (and Loop 2).
- 1) (SEC2). Initialize section 2, Loop 1 to select Output mode on 8049.
 - 2) (LOOP21). Initialize EOP interrupt.

- 3) Connect to 8049 and select Output mode (or Input mode in Loop 2).
- 4) Expect reply (hang on reject), Error code 4 or 5 if not.
- 5) (S21B). Get DTB status.
- 6) Expect Busy, Error code 6 if not.
- 7) Delay 30 microseconds.
- 8) Expect EOP interrupt, Error code 9 if not.
- 9) (S21D). Get DTB status.
- 10) Expect interrupt and Not Busy, Error code 6 if not.
- 11) (S21E). Clear interrupt.
- 12) Expect reply (hang on reject), Error code 4 or 5 if not.
- 13) (S21F). Get DTB status.
- 14) Expect zero, Error code 6 if not.
- 15) (S21G). Initialize EOP interrupt.
- 16) Expect no EOP interrupt, Error code 8 if interrupt.
- 17) (S21H). Set Q15 and Q02.
- 18) Output (request input of 8049 status).
- 19) Expect reply (hang on reject), Error code 4 or 5 if not.
- 20) (S21I). Initialize EOP interrupt.
- 21) Expect EOP interrupt, Error code 9 if not.
- 22) (S21J). Get DTB status.
- 23) Expect data, interrupt, Busy Status, Error code 6 if not.
- 24) (S21K). Clear Q00.
- 25) Input 8049 status.
- 26) Expect reply (hang on reject), Error code 4 or 5 if not.
- 27) Expect 8049 status to be 701 hex (3401 octal) if Output mode was selected (Loop 1). Expect 8049 status to be 700 hex (3400 octal) if Input mode was selected (Loop 2). Error code A if not.
- 28) (S21M). Get DTB status.
- 29) Expect zero, Error code 6 if not.
- 30) (S21MA). Attempt 2nd input from 8049.

- 31) Expect external reject, Error code 4 or 7 if not.
- 32) (S21N). Initialize EOP interrupt.
- 33) Expect no EOP interrupt, Error code 8 if interrupt.
- 34) (S21O). Set Q15 and Q02.
- 35) Output (request input of data).
- 36) Expect reply (hang on reject), Error code 4 or 5 if not.
- 37) (S21P). Initialize EOP interrupt.
- 38) If Loop 1 (Output mode), go to 62) (S21AA).
- 39) Expect EOP interrupt (upon disconnect).
- 40) (S21Q). Clear interrupt.
- 41) Expect reply (hang on reject), Error code 4 or 5 if not.
- 42) (S21R). Initialize EOP interrupt.
- 43) Expect interrupt, Error code 9 if not.
- 44) (S21S). Get DTB status.
- 45) Expect Disconnect, Interrupt, Busy, Error code 6 if not.
- 46) (S21U). Attempt input from 8049 after disconnect.
- 47) Expect internal reject, Error code 5 or 7 if not, unless DTB is on 1706 or 1716 (W non-zero).
- 48) If DTB is on 1706 or 1716 expect external reject and expect 1706 status of Busy, not device reply, not device reject. Error code E if unexpected BDC status. If W is non-zero, perform terminate buffer on 1706 and go to 51) (S21W).
- 49) (S21V). Connect to 8049.
- 50) Expect internal reject, Error code 5 or 7 if not.
- 51) (S21W). Clear controller.
- 52) Expect reply (hang on reject), Error code 4 or 5 if not.
- 53) (S21X). Get DTB status.
- 54) Expect Disconnect, Interrupt, Not Busy status, Error code 6 if not.
- 55) Get DTB status.
- 56) Expect interrupt and not Disconnect status, Error code 6 if not.

- 57) (S21Y). Clear interrupt.
 - 58) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 59) (S21Z). Get DTB status.
 - 60) Expect zero, Error code 6 if not.
 - 61) Go to 66) (S21AB).
 - 62) (S21AA). Expect no EOP interrupt.
 - 63) Get DTB status.
 - 64) Expect Busy status, Error code 6 if not.
 - 65) Clear controller.
 - 66) (S21AB). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- b. Section 2, Loop 2
- 1) (LOOP22). Set up Section 2, Loop 1 to select Input mode instead of Output mode.
 - 2) Go to 2. a. 1) (LOOP21) unless Input mode has been used.
- c. Section 2, Loop 3
- 1) (LOOP23). Initialize EOP interrupt.
 - 2) Connect to 8049 station 2.
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S23A). Get DTB status.
 - 5) Expect Busy, Error code 6 if not.
 - 6) Delay 30 microseconds.
 - 7) Expect EOP interrupt, Error code 9 if not.
 - 8) (S23B). Request input from 8049.
 - 9) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 10) (S23C). Get DTB status.
 - 11) Expect Data, Interrupt, Busy Status, Error code 6, if not.
 - 12) (S23D). Input 8049 status.
 - 13) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 14) (S23E). Expect 8049 status to be 712 hex (Busy bit set), Error code A if not.

- 15) Get DTB status.
 - 16) Expect zero, Error code 6 if not.
 - 17) (S23F). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- d. Section 2, Loop 4
- 1) (LOOP24). Initialize EOP interrupt.
 - 2) Connect to 8049, select Output mode.
 - 3) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 4) (S24A). Clear controller.
 - 5) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 6) (S24B). Delay 30 microseconds.
 - 7) Expect no EOP interrupt, Error code 8 if interrupt.
 - 8) (S24C). Get DTB status.
 - 9) Expect Busy status, Error code 6 if not.
 - 10) (S24D). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- e. Section 2, Loop 5
- 1) (LOOP25). Initialize EOP interrupt.
 - 2) Connect to 8049, select Output mode, hang on reject.
 - 3) (S25A). Wait for EOP interrupt.
 - 4) (S25B). Clear controller, hang on reject.
 - 5) Get DTB status.
 - 6) Expect zero, Error code 6 if not.
 - 7) (S25C). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- f. Section 2, Loop 6
- 1) (LOOP26). Initialize EOP interrupt.
 - 2) Connect to 8049, Select mode, hang on reject.
 - 3) (S26A). Wait for EOP interrupt.
 - 4) (S26B). Initialize EOP interrupt.
 - 5) Request input from 8049, hang on reject.
 - 6) (S26C). Wait for EOP interrupt.

- 7) (S26D). Clear controller, hang on reject.
- 8) Get DTB status.
- 9) Expect zero, Error code 6 if not.
- 10) (S26E). Initialize EOP interrupt.
- 11) Request input from 8049, hang on reject.
- 12) (S26F). Wait for EOP interrupt (due to disconnect).
- 13) (S26G). Clear interrupt.
- 14) Expect reply (hang on reject), Error code 4 or 5 if not.
- 15) (S26GA). Get DTB status.
- 16) Expect Disconnect, Interrupt, Busy status, Error code 6 if not.
- 17) Clear controller, hang on reject.
- 18) Clear interrupt, hang on reject.
- 19) Get DTB status.
- 20) Expect Disconnect, Interrupt, and Not Busy status, Error code 6 if not.
- 21) Get DTB status again.
- 22) Expect Interrupt and not Disconnect status, Error code 6 if not.
- 23) Clear interrupt, hang on reject.
- 24) Get DTB status.
- 25) Expect zero status, Error code 6 if not.
- 26) (S26H). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.

g. Section 2, Loop 7

- 1) (LOOP27). Initialize EOP interrupt.
- 2) Connect to 8049, select Output mode, hang on reject.
- 3) (S27A). Wait for EOP interrupt.
- 4) (S27B). Initialize EOP interrupt.
- 5) Request input from 8049, hang on reject.
- 6) (S27C). Wait for EOP interrupt.
- 7) (S27D). Input 8049 status, hang on reject.
- 8) (S27DA). Initialize EOP interrupt.

- 9) Output data (blanks) to 8049.
 - 10) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 11) (S27E). Clear controller (hang on reject).
 - 12) Expect no EOP interrupt, Error code 8 if interrupt.
 - 13) (S27F). Get DTB status.
 - 14) Expect Busy, Error code 6 if not.
 - 15) (S27G). Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- h. Section 2, Loop 8
- 1) (LOOP28). Connect to 8049, select Output mode, reset entry marker.
 - 2) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 3) (S28A). Get DTB status.
 - 4) Expect Busy, Error code 6 if not.
 - 5) (S28B). Wait Not Busy.
 - 6) (S28C). Expect Interrupt status when busy drops, Error code 6 if not.
 - 7) (S28D). Request input from 8049.
 - 8) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 9) (S28E). Get DTB status.
 - 10) Expect Data, Interrupt, and Busy status, Error code 6 if not.
 - 11) (S28F). Input 8049 status.
 - 12) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 13) (S28G). Expect 8049 status to be 701 hex (3401 octal), Error code A if not.
 - 14) (S28H). Initialize EOP interrupt.
 - 15) (S28HA). Output data to 8049.
 - 16) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 17) (S28I). Get DTB status.
 - 18) Expect Busy, Error code 6 if not.
 - 19) (S28J). Delay 40 milliseconds.
 - 20) Get DTB status.
 - 21) Expect Interrupt status, Error code 6 if not.

- 22) Expect EOP interrupt, Error code 9 if not.
 - 23) Loop to 14) (S28H) to output word 25 which contains EOM code.
 - 24) Loop to 1) if Stop/Jump bit 4 is set.
- i. Section 2, Loop 9
- 1) (LOOP29). Connect to 8049, select Output mode, reset entry marker, hang on reject.
 - 2) Request input from 8049, hang on reject.
 - 3) (S27A). Wait for Interrupt status.
 - 4) Expect Data, Interrupt, Busy status, Error code 6 if not.
 - 5) (S29AA). Set Q15, clear Q00, set Q01 through Q06.
 - 6) Input (8049 status).
 - 7) Expect reply (hang on reject), Error code 4 or 5 if not.
 - 8) (S29B). Expect 8049 status to be 701 (3401 octal), Error code A if not.
 - 9) Loop to 1) 100 times and until Stop/Jump bit 4 is clear.
- j. Section 2, Loop 10
- 1) (LOOP2A). Connect to 8049, select Output mode hang on reject.
 - 2) Request input from 8049, hang on reject.
 - 3) Input status from 8049, hang on reject.
 - 4) (S2AA). Output data (blanks), hang on reject.
 - 5) Output data (blanks) again, hang on reject.
 - 6) Wait Not Busy.
 - 7) Expect Interrupt status when Not Busy, Error code 6 if not.
 - 8) Output data (blanks), hang on reject.
 - 9) Output data (blanks) again, hang on reject.
 - 10) Wait for Interrupt status.
 - 11) Expect Not Busy status with Interrupt status, Error code 6 if not.
 - 12) Loop to 4) (S2AA) for total of 500 words.
 - 13) (S2AB). Loop to 1) if Stop/Jump bit 4 is set.

- k. End of Section 2
 - 1) Clear controller.
 - 2) Stop if Stop/Jump bit 1 is set.
 - 3) Repeat Section 2 if Stop/Jump bit 5 is set.

3. Section 3 - INTERRUPT 40 CHECK

- a. Section 3, Loop 1
 - 1) (SEC3). Connect to 8049, select Output mode, reset entry marker, hang on reject.
 - 2) (S31A). Wait Not Busy.
 - 3) (S31B). Request input, hang on reject.
 - 4) Input 8049 status, hang on reject
 - 5) (S31C). Output 500 blank words (to clear screen).
 - 6) (S31F). Output message "PRESS SEND KEY" followed by EOM code.
 - 7) (S31H). Initialize interrupt 40.
 - 8) (S31HA). Connect to 8049, select Input mode, hang on reject.
 - 9) Request input, hang on reject.
 - 10) Input 8049 status, hang on reject.
 - 11) Loop to 7) (S31H) until interrupt 40 occurs or until one or both of 8049 status bits 0 and 5 are set.
 - 12) (S31I). If one or both or 8049 status bits 0 and 5 are set, expect 8049 status to be 721 hex (3441 octal), Error code A if not.
 - 13) (S31IA). Expect interrupt 40, Error code B if not.
 - 14) Go to 19) (S31L).
 - 15) (S31J). If interrupt 40 occurs, connect to 8049 and get 8049 status.
 - 16) Expect 8049 status to be 721 hex (3441 octal), Error code A if not.
 - 17) (S31K). Initialize interrupt 40.
 - 18) Expect no interrupt 40, Error code C if interrupt 40 occurs.
 - 19) (S31L). Initialize EOP interrupt.
 - 20) Request input (of data).
 - 21) Delay 20 milliseconds.

- 22) (S31M). Get DTB status.
- 23) (S31N). Go to 36) (S31T) if Disconnect status is set.
- 24) Expect data, Interrupt, Busy status, Error code 6 if not.
- 25) Expect EOP interrupt, Error code 9 if not.
- 26) (S31O). Input data from 8049.
- 27) Expect reply (hang on reject), Error code 4 or 5 if not.
- 28) (S31P). Get DTB status.
- 29) Expect zero, Error code 6 if not.
- 30) Loop to 19) (S31L) if not EOM code.
- 31) (S31Q). Request input, hang on reject.
- 32) Delay 30 microseconds for disconnect to set in 8049.
- 33) (S31R). Get DTB status.
- 34) Expect Disconnect, Interrupt, Busy, Error code 6 if not.
- 35) Go to 37) (S31U).
- 36) (S31T). Disconnect status occurred on DTB, EOM code was not found, Error code D.
- 37) (S31U). Clear controller.
- 38) Clear controller again.
- 39) Loop to 1) five times and until Stop/Jump bit 4 is clear.

b. End of Section 3

- 1) Clear controller.
- 2) Stop if Stop/Jump bit 1 is set.
- 3) Repeat Section 3 if Stop/Jump bit 5 is set.

4. Section 4 - OUTPUT SHIFTED PATTERN

a. Section 4, Loop 1 (Ripple Test)

- 1) (SEC4). Connect to 8049, select Output mode, reset entry marker, hang on reject.
- 2) (LOOP41). Set up buffer area for first line of pattern (store all codes in buffer area in ascending order except EOM code and Carriage Return code).

- 3) (S4E). Connect to 8049, select Output mode, do not reset entry marker, hang on reject.
 - 4) Request input of status from 8049, hang on reject.
 - 5) Input status from 8049, hang on reject.
 - 6) (S4F). Get data in A.
 - 7) (S4G). Output data, hang on reject.
 - 8) Increment word count, and loop to 6) (S4F) for 24 words.
 - 9) (S4GB). Form last word with EOM code, and loop to 7) (S4G) to output word 25.
 - 10) (S4H). Loop to 3) (S4E) if Stop/Jump bit 4 is set.
 - 11) Shift buffer area, increment line count, and loop to 3) (S4E) for 20 lines (fill the screen).
 - 12) Loop to 2) (LOOP41) 20 times and until Stop/Jump bit 4 is clear.
- b. End of Section 4
- 1) Clear controller.
 - 2) Stop if Stop/Jump bit 1 is set.
 - 3) Repeat Section 4 if Stop/Jump bit 5 is set.
5. Section 5 - ECHO TEST
- a. Section 5, Loop 1
- 1) (SEC5). Output message "ECHO TEST" in upper left of display screen and fill rest of screen with blanks.
 - 2) (S5E). Initialize interrupt 40.
 - 3) (S5F). Wait for interrupt 40.
 - 4) (S5G). Connect to 8049, select Input mode, hang on reject.
 - 5) Request input from 8049, hang on reject.
 - 6) Input status from 8049, hang on reject.
 - 7) Expect 8049 status to be 721 hex (3441 octal), Error code A if not.
 - 8) (S5I). Request input, hang on reject.
 - 9) Input data from 8049, hang on reject, and store data in buffer area.
 - 10) Loop to 8) (S5I) until EOM code or word 500 is input.

- 11) (S5J). Request input, hang on reject.
 - 12) Delay 15 milliseconds for disconnect to set in 8049.
 - 13) Clear controller to clear disconnect.
 - 14) Connect to 8049, select Output mode, do not reset entry marker, hang on reject.
 - 15) Request input, hang on reject.
 - 16) Input 8049 status, hang on reject.
 - 17) Output carriage return on 8049.
 - 18) If first two characters of input message were periods, go to end of section (S5M).
 - 19) (S5K). Output data thru EOM code.
 - 20) (S5L). Delay 2 seconds for operator to view display.
 - 21) Loop to 1) 20 times and until Stop/Jump bit 4 is clear.
- b. End of Section 5 (S5M).
- 1) Clear controller.
 - 2) Stop if Stop/Jump bit 1 is set.
 - 3) Repeat Section 5 if Stop/Jump bit 5 is set.
6. Section 6 - ONE SYMBOL
- a. Section 6, Loop 1
- 1) (SEC6). Connect to 8049, select Output mode, reset entry marker, hang on reject.
 - 2) Request input, hang on reject.
 - 3) Input, hang on reject.
 - 4) (S6A). OUTPUT 999 identical symbols (the symbol code was chosen at the parameter stop).
 - 5) (S6C). OUTPUT EOM code.
 - 6) (S6D). Loop to 1) (SEC6) 20 times and until Stop/Jump bit 4 is clear.
- b. End of Section 6
- 1) Clear controller.
 - 2) Stop if Stop/Jump bit 1 is set.
 - 3) Repeat Section 6 if Stop/Jump bit 5 is set.

7. End of Test
 - a. End of test timeout.
 - b. Stop if Stop/Jump bit 2 is set.
 - c. Test will be repeated.
 - d. Re-enter parameters if bits 0 and 10 of stop/jump word are set.

III. PHYSICAL REQUIREMENTS

- A. SPACE REQUIRED - approximately 1700 locations.
- B. TIMING
- C. EQUIPMENT CONFIGURATION
 1. 1704 Computer
 2. 8049 Display Controller
 3. 211 Display Station

1744/274 DIGIGRAPHICS SYSTEM

(DIGA4F Test No. 4F)

The following information contains the procedure for performing each of the Digigraphics test programs. Test program 2 relates to alignment of the 274 Console. This procedure illustrates the method for stepping through each test phase of the console alignment; it does not include the alignment procedure. The user must still refer to the 274 Digigraphics Console Reference/Customer Engineering Manual (Pub. No. 60279100) for specific information on how adjustments are to be performed.

OPERATIONAL PROCEDURE

A. HARDWARE REQUIREMENTS

1. 1704 or 1774 Computer
2. 1744 Digigraphic Controller
3. 274 Display Console
4. 1706 Channel (optional)

B. SOFTWARE REQUIREMENTS

1. Test operates under control of SMM 17.
2. Test is a stand-alone test.
3. Test is approximately $2A70_{16}$ locations in length.
4. Bit 5 of the SMM parameter must be set to run the test (NON-interrupt mode).

C. LOADING PROCEDURE

1. The test must be loaded under SMM 17 as test number 4F.
2. The test may be restarted from Initial Address.

D. PARAMETERS

Once the test has been loaded the following procedure is applicable.

1. Teletype types: Interrupt Line 1 to F.
2. Enter interrupt line; 1 to \$F.

3. Depress carriage RETURN key.
4. Teletype types: DATA CHANNEL.
5. Type: 0 (if 1706 BDC not used)
or
1 (if 1706 BDC used)
6. Teletype types: EQUIP NO.
7. Enter equipment number; 1 to \$F
8. Depress carriage RETURN key.
9. Teletype types: TYPE TEST NUMBER.
10. Check that all computer console lever switches are in center position.
11. Type test number: X where X = 1-9.
(For test 6 go to step 12 and skip step 11.)
12. Go to test program procedure to be performed.
13. Repeat steps 10 through 12 for each test.

NOTE

If at the completion of any test program, the 274/1744
Maintenance Test is to be exited, return to System
Maintenance Monitor Control:

- a. Depress and release SELECTIVE SKIP lever switch.
- b. Teletype types: TYPE TEST NUMBER.
- c. Type: E
- d. Depress and release carriage RETURN key.

E. TEST PROGRAMS

1. Test 1: Core Test Program
 - a. Phases 1 and 2.
 - 1) Set SELECTIVE STOP lever switch to up position. (Switch must remain in this position for the normal execution of the Core Test Program.)
 - 2) Teletype types: ENTER MEMORY SIZE 4 or 8.
 - 3) Type: 4 (if 1744 core memory = 4K)
or
8 (if 1744 core memory = 8K)

- 4) Depress carriage RETURN key.
- 5) Teletype types: 1744 CONTROLLER MEMORY
MODULE ADDRESS ACTUAL DESIRED

NOTE

Phase 1 and phase 2 of core test are now in progress (test requires 1 to 2 minutes for execution). If both phases are performed without error, teletype will print message indicated in Phase 3, step 1). This signifies entry into phase 3 of core test. If test fails, an error type-out will be printed conforming to the format above.

b. Phase 3.

- 1) Teletype has typed: ENTER TEST PATTERN IN A REG-RUN.
- 2) Depress REGISTER SELECT button.
- 3) Depress display register CLEAR button.
- 4) Using the display register buttons, enter the test pattern to be written into 1744 core (this pattern will also be read and verified).
- 5) Momentarily set RUN/STEP lever switch to RUN position and release.
- 6) Teletype types: XXXX HEX TEST PATTERN SELECTED.
(XXXX = test pattern selected, in hexadecimal).
- 7) If you previously designated that the 1744 has an 8K memory, perform steps a) through c); with a 4K memory, omit these steps.
 - a) Teletype types: TYPE 0 OR 1 TO SELECT MODULE.
 - b) Type: 0 (if you desire Module 0 to be exercised)
or
1 (if you desire Module 1 to be exercised)
 - c) Depress and release carriage RETURN.

NOTE

Module 1 or 2 is currently being exercised. It takes approximately 1 minute to complete the Read, Write and Verify operation. If no errors occur, the operation will continually be recycled. If an error is detected, the teletype will print out the error information.

- 8) To exit phase 3, press and release teletype MANUAL INTERRUPT button.

c. Phase 4.

- 1) Teletype has typed: R or W.
- 2) Type: W (if you want a continuous write operation performed)
or
R (if you want a single write operation followed by a continuous read)
- 3) Teletype types: ENTER TEST PATTERN IN A REG-RUN
- 4) Press REGISTER SELECT button.
- 5) Press display register CLEAR button.
- 6) Set the display register buttons to reflect the pattern to be used for the continuous read or write operation.
- 7) Momentarily set RUN/STEP lever switch to RUN position and release.
- 8) Teletype types: XXXX HEX TEST PATTERN SELECTED
(XXXX = test pattern selected, in hexadecimal).
- 9) If you previously designated that the 1744 has an 8K memory, perform steps a) through c); with a 4K memory, omit these steps.
 - a) Teletype types: TYPE 0 or 1 TO SELECT MODULE.
 - b) Type: 0 (if you wish the continuous read or write operation performed with Module 0)
or
1 (if you wish the continuous read or write operation performed with Module 1)
 - c) Depress and release carriage RETURN key.

NOTE

The continuous read or write operation is now in progress. There is no verification during this phase. The program will continually loop until user desires to manually exit test.

- 10) To exit from Core Test Program:
 - a) Set SELECTIVE STOP lever switch to center position.
 - b) Press REGISTER SELECT button.
 - c) Press and release SELECTIVE SKIP lever switch.
 - d) Teletype types: TYPE TEST NUMBER
 - e) Go to next test program.

2. Test 2: 274 Console Test Program

NOTE

The following procedure enables the user to step through all the phases of the console test program. It is intended to supplement the current console alignment procedure in the Digigraphics console customer engineering manual. The user must still refer to the alignment procedure for complete and accurate guidance.

a. Teletype types: NUMBER

b. Choose one of the following:

If user desires only to step through the high voltage on checks (phases 15-18, see Table 1), perform the following:

- 1) In reply to the teletype message, NUMBER, type: 15
- 2) Press carriage RETURN. (Test phase is now in progress; 274 Console displays square type pattern).
- 3) Omit steps c through f. and go directly to step g.

OR

If user desires to step through each test phase, see Table 1, and proceed to step c.

c. Turn off the 274 Console high-voltage power supply.

CAUTION

Console test phases 1 through 14 should be performed with the console high voltage turned off. Failure to turn off high voltage may cause burn spots on the Console CRT screen.

NOTE

If user attempts to enter console test phases 1 through 14 with high voltage on, teletype types: TURN OFF HIGH VOLTAGE. The proper response to this message is:

- 1) Turn off 274 Console high-voltage power supply.
- 2) Wait until type-out stops.
- 3) Depress and release teletype MANUAL INTERRUPT pushbutton.
- 4) Teletype types: NUMBER
- 5) Go to step h.

Remove the 274 Console preamplifier cards at locations J43 and J66.
(Turn console off while cards are being removed or inserted).

CAUTION

Console test phases 1 through 12 should be performed with the console preamplifier cards at jack locations J43 and J66 removed. Failure to remove cards will cause the console deflection amplifiers to overheat. Make certain that preamplifier cards are replaced before turning high voltage back on.

- d. In reply to the teletype message, NUMBER, type: 1.
- e. Press carriage RETURN.

NOTE

Phase 1 of console test is now in progress.

TABLE 1. CONSOLE TESTS

CAUTIONS

High voltage off for phases 1-14.
Do not turn high voltage back on until phase 15 is executed.
Preamplifier cards out for phases 1-12, replace after entering phase 13.
Never turn high voltage on while preamplifier cards out.
Turn console off when cards are being removed or inserted.
Refer to Digigraphics console customer engineering manual for exact sequencing of items above.

<u>Phase</u>	<u>Console Test</u>
1	Receiver check
2	Bit 2 D/A Alignment
3	Bit 3 Alignment
4	Bit 4 Alignment
5	Bit 5 Alignment
6	Bit 6 Alignment
7	Bit 7 Alignment
8	Bit 8 Alignment
9	Bit 9 Alignment
10	Bit 10 Alignment
11	Bit 11 Alignment
12	S&H Delay and Time Constant
13	Preamplifier and Deflection Ampl. Alignment

TABLE 1. CONSOLE TESTS (Cont'd)

<u>Phase</u>	<u>Console Test</u>
14	XY Velocity and Vector Sum Adj.
15	Test Square Displayed
16	Three Test Squares Displayed
17	Test Square Displayed
18	Five Dot Pattern Displayed

- f. To progress through remainder of console test, choose one of the following procedures:
- 1) Teletype Advance Procedure. (Procedure enables user to advance through test sequentially or to jump to any desired test phase.)
 - a) Depress teletype MANUAL INTERRUPT button.
 - b) Teletype types: NUMBER
 - c) Type in number in PHASE column (see Table 1) corresponding to specific console test you wish to perform.
 - d) Press carriage RETURN key. (Selected console test phase is now in progress.)
 - e) Repeat steps a through d to advance test.
 - 2) Light Pen Switch Advance. (Procedure enables user to sequentially advance through test phases 1-15).
 - a) Press and release light pen switch.
 - b) Teletype types: N = XX
(XX = console test phase initiated; see Table 1.)
 - c) Repeat steps a and b to advance test.
 - 3) Maintenance Switch Card Advance. (Procedure enables user to sequentially advance through test phases 1-18. Test phase 18 advances to phase 1.)
 - a) Press and release switch on maintenance card (location J16) in the 274 Console logic rack.
 - b) Teletype types: N = XX
(XX = console test phase initiated; see Table 1.)
 - c) Repeat steps a and b to advance test.

- 4) Light Pen Strike Advance. (May be used to advance program sequentially only when light is present on screen; i. e., phases 15-18. Test phase 18 advances to phase 1.)
 - a) Press Light Pen switch and pick light from the 274 Console display.
 - b) Teletype types: N = XX
(XX = console test phase initiated; see Table 1.)
 - c) Repeat steps a and b to advance test.
 - h. To exit 274 Console Test Program:
 - a) Press and release SELECTIVE SKIP lever switch.
 - b) Teletype types: TYPE TEST NUMBER
 - c) Go to next test program.
3. Test 3: X, Y and S Transfer and ID Read Test Program
- a. Internal/Computer Display Check

NOTE

If test 3 is in progress and any interrupt other than Priority or Light Pen occurs, the teletype will print out an error message (Ghost Interrupt):

GI
HHHH*

- 1) Observe that:
 - a) Teletype does not print error message.
 - b) The display on the 274 Console conforms to the following illustration (Dots are internally displayed; cross is computer-displayed.)

*HHHH = Status of 1744 in hexadecimal

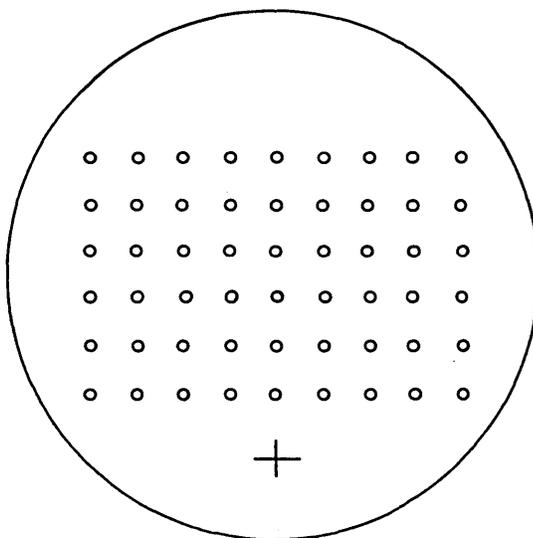


Figure 1. Dot-Cross Display

b. ID Error Check.

- 1) Using the light pen, choose one of the displayed dots. Observe that:
 - a) Next dot in sequence disappears while choice is being made.
(Dot sequence: left to right, starting at bottom row)
 - b) There is no teletype ID error (IDERR) message printout.

NOTE

An ID error printout (in hexadecimal) will resemble the following format:

IDERR

$X_4 X_3 X_2 X_1$ $Y_4 Y_3 Y_2 Y_1$ $S_4 S_3 S_2 S_1$
 00 $X_4 X_3$ 00 $X_2 X_1$ 00 $Y_4 Y_3$ 00 $Y_2 Y_1$ 00 $S_4 S_3$ 00 $S_2 S_1$ 00VR* 00HR**

* Vertical row number of dot chosen.

**Horizontal row number of dot chosen.

Top row of numbers reflects actual X, Y and S register status at time of light pen strike. Bottom row reflects ID bytes associated with chosen dot. Two low-order characters of each ID byte identify dot parameters.

c. Forced Printout Feature.

- 1) Using the light pen, choose one of the displayed dots (next dot in sequence disappears when choice is made).
- 2) Using the light pen, choose the cross.
- 3) Observe that the teletype prints a message conforming to the following format (information relates to chosen dot, not cross):

CROSS

$X_4 X_3 X_2 X_1$ $Y_4 Y_3 Y_2 Y_1$ $S_4 S_3 S_2 S_1$

$00X_4 X_3$ $00X_2 X_1$ $00Y_4 Y_3$ $00Y_2 Y_1$ $00S_4 S_3$ $00S_2 S_1$ OOVR OOHR

d. Intensity Levels Check.

- 1) Set SELECTIVE STOP lever switch to up position.
- 2) Depress REGISTER SELECT button.
- 3) Depress the display register CLEAR button.
- 4) Enter $OF77_{16}$ (0000111101110111_2) into the display register.
- 5) Set SELECTIVE STOP lever switch to center position.
- 6) Momentarily set the RUN/STEP lever switch to RUN position and release.
- 7) Observe that:
 - a) Each previously displayed dot has been replaced with a 45-degree line, approximately 1 inch in length.
 - b) The lines at the left third of the display are of a dim intensity; center third, medium intensity; and right third, bright intensity.

e. Increment Byte Entry Feature.

- 1) Set SELECTIVE STOP lever switch to up position.
- 2) Depress REGISTER SELECT-A button.
- 3) Depress display register CLEAR button.
- 4) Enter desired increment byte into display register. Use the following guide.

Display Register	15 14 13 12	11	10 9 8	7	6 5 4	3	2 1 0
Increment Byte	Set to 0's	1 = Beam on 0 = Beam off	Scale Factor 010, 011, 100, 101, 110 or 111 only	Sign X 0 = + 1 = -	X enter in comple- ment form if sign neg.	Sign Y 0 = + 1 = -	Y enter in comple- ment form if sign neg.

- 5) Set SELECTIVE STOP lever switch to center position.
- 6) Momentarily set RUN/STEP lever switch to RUN position and release.
- 7) Observe that 274 Console displays the new increment byte.

NOTE

To enter another increment byte, repeat previous seven steps.

- f. To exit from X, Y and S Transfer and ID Read Test Program:
 - 1) Depress REGISTER SELECT-P button.
 - 2) Depress and release SELECTIVE SKIP lever switch.
 - 3) Teletype types: TYPE TEST NUMBER
 - 4) Go to next test program.

4. Test 4: Command Test Program.

- a. Observe that 274 Console displays the following:

SSSSSSSSSSMMMMMMMMMMMMPPPPPPPPPPRRRRRRRRRRRE

NOTE

S's signify successful execution of an S Jump command;
M's, Macro Call; P's, P Jump; R's, Return to Main;
E's - decoding of an End of Display byte.

- b. To Exit Command Test Program:
 - 1) Depress and release SELECTIVE SKIP lever switch.
 - 2) Teletype types: TYPE TEST NUMBER
 - 3) Go to next test program.

5. Test 5: Memory Dump Program.
 - a. Teletype types: FWA
 - b. If only one dump is desired and the dump program is to be exited at the completion of that dump, set and leave the SELECTIVE SKIP lever switch in the up position. To remain in dump program, check that switch is in the center position.
 - c. In reply to teletype message "FWA", type, in hexadecimal, the First Word Address of memory dump (0 to FFF in 4K system; 0 to 1FFF in 8K system).
 - d. Depress and release carriage RETURN key.
 - e. Teletype types: NWDS
 - f. Type, in decimal, the number of words desired in dump. (Maximum: 100_{10}).
 - g. Depress and release carriage RETURN key.
 - h. Observe that teletype prints out the memory dump requested (typeout is in hexadecimal).
 - i. Choose one of the following:
 - 1) If SELECTIVE SKIP lever switch is in the center position:
 - a) At the completion of the dump, teletype types: FWA
 - b) Repeat steps 5b through 5h to obtain another dump.
 - 2) If SELECTIVE SKIP lever switch is in the up position:
 - a) At the completion of the dump, the teletype types: TYPE TEST NUMBER.
 - b) Set SELECTIVE SKIP lever switch to center position.
 - c) Go to next test program.
6. Test 6: Variable Function and Alphanumeric Keyboards Test Program.
 - a. Check that all computer console lever switches are in the center position.
 - b. Perform the appropriate keyboard checkout procedures: 1) Variable Function Keyboard Checkout and/or 2) Alphanumeric Keyboard Checkout.
 - 1) Variable Function Keyboard Checkout:
 - a) Prior to initiating Test 6, depress and release Keyboard ON/OFF pushbutton several times. Observe that the pushbutton illuminates and extinguishes. Leave pushbutton in extinguished condition.

NOTE

Keyboard ON/OFF lamp extinguished indicates deactivated keyboard.

- b) Teletype has previously typed: TYPE TEST NUMBER
- c) Type: 6
- d) Depress carriage RETURN.
- e) Observe that keyboard ON/OFF pushbutton illuminates.
- f) Check that all pushbuttons, except ON/OFF, are extinguished or can be extinguished by depressing pushbuttons.
- g) With all keyboard pushbuttons, except ON/OFF, extinguished, observe that the 274 Console display surface is blank.
- h) Depress and hold keyboard Reject (red) button. Observe that the button is illuminated and "00" is displayed on the 274 Console.
- i) Release Reject button.
- j) Depress and hold keyboard Accept (green) button. Observe that the button is illuminated and "01" is displayed on the 274 Console.
- k) Release Accept button.
- l) Depress and latch each latching button (those other than Accept, Reject, and ON/OFF). Observe that as each button is latched, the bit position associated with the button is displayed.
- m) Depress and release the On/OFF button.
- n) Note that all keyboard button lamps extinguish and the 274 Console screen is blank.
- o) To exit from Variable Function Keyboard portion of test program:
 - (1) Depress and release SELECTIVE SKIP lever switch.
 - (2) Teletype types: TYPE TEST NUMBER
 - (3) Choose one of the following:
 - Go to Alphanumeric Keyboard Checkout
 - or
 - Go to any other 274/1744 Maintenance Test programs to be performed
 - or
 - Exit 274/1744 Maintenance Test and return to SMM 17 control by:

- (a) In reply to teletype message TYPE TEST NUMBER,
type: E
 - (b) Depress and release carriage RETURN key.
- 2) Alphanumeric Keyboard Checkout.
- a) Prior to initiating Test 6, depress and release keyboard ON/OFF button several times. Observe that the button illuminates and extinguishes. Leave button in illuminated condition.

NOTE

Keyboard ON/OFF lamp illuminated indicates keyboard activated.

- b) Teletype has previously typed: TYPE TEST NUMBER
- c) Type: 6
- d) Depress and release carriage RETURN.
- e) Observe that keyboard ON/OFF pushbutton extinguishes.
- f) Depress and release keyboard on/off pushbutton and observe that it illuminates.
- g) Using Table 2 as a guide, depress and release keyboard key and observe that the 274 Console displays the data indicated.

NOTE

Certain key characters are uppercase symbols and require that the SHIFT or CTRL keys be depressed (dep) while selection is being made.

NOTE

The 274 Console will display any portion of "07 06 05 04 03 02 01 00" depending on which key is depressed. A "07 03 00" would indicate that the 1744 Controller is sending a logical 1 in bit positions 07, 03, and 00 to the computer. The 06, 05, 04, 02, and 01 bit positions would be logical 0's.

- h) To exit from Alphanumeric Keyboard portion of test program:
 - (1) Depress and release SELECTIVE SKIP lever switch.
 - (2) Teletype types: TYPE TEST NUMBER.

(3) Choose one of the following:

Go to any other 274/1744 Maintenance Test programs to be performed

or

Exit 274/1744 Maintenance Test and return to SMM 17 control by:

(a) In reply to teletype message TYPE TEST NUMBER, type: E

(b) Depress and release carriage RETURN key.

7. Test 7: SPARE (Not used)

8. Test 8: Scissoring Test

a. Observe that the 274 Console displays the form described under Test 8 in the TEST PROGRAMS DESCRIPTION section.

b. To exit the scissoring test program:

1) Depress and release SELECTIVE SKIP lever switch.

2) Teletype types TYPE TEST NUMBER.

3) Go to next test program.

9. Test 9: Velocity Compensation Test

Same as above, except for the display. See the discussion under TEST PROGRAM DESCRIPTIONS.

TEST PROGRAMS DESCRIPTION

TEST 1: CORE TEST PROGRAM

PURPOSE

The core test program checks the ability of the 1744 Controller to have data written into and read out of its buffer memory, and it ensures that the transfer is unaffected by cross talk. The worst test patterns are used to thoroughly exercise the logic circuitry.

PROCEDURAL DESCRIPTION

General

Test 1 is subdivided into four test phases. Phases 1 and 2 are executed sequentially without operator intervention. Pre-selected test patterns using varied combinations of $FFFF_{16}$, 0000_{16} , 5555_{16} and $AAAA_{16}$ bytes are used. Phase 3 enables the user to exercise buffer memory with any 16-bit word combination so desired. In phases 1, 2 and 3, the selected bytes are written into core, read out and verified. If the test phase fails, the teletype will print out a message defining the failure. The fourth phase is a continuous read/write feature, whereby the user specifies a 16-bit word pattern and calls for a read or write operation.

Phases 1 and 2

Upon entering test 1 the teletype prints out ENTER MEMORY SIZE 4 or 8. This is a request for the user to enter, via the teletype, the current size of the 1744 buffer memory, 4 or 8, as applicable for a 4K or 8K system. When the core size information is entered, the teletype prints:

```
1744 CONTROLLER MEMORY
MODULE ADDRESS ACTUAL DESIRED
```

This typeout signifies that phase 1 of the core test has been initiated. Phase 2 will automatically be entered at the successful completion of phase 1. Should either test phase fail, the teletype will print out an error message in hexadecimal conforming to the format heading above. The typeout in the MODULE column will be either 1 or 0, indicating the memory module in which the failure occurred. The ADDRESS column will contain the 1744 S-Register count at which the error occurred. The ACTUAL column specifies the byte that was read

back to the computer (i. e., the byte that is in error). DESIRED column indicates the true byte being exercised by the test program. The successful completion of phases 1 and 2 is signaled by: no error message typeout; and teletype message, ENTER TEST PATTERN IN A REG-RUN.

Phase 3

The last typeout signified entry into phase 3 of the core test; it is also a request for the user to enter a test pattern in the A register of the computer, via the computer console display register pushbuttons. The program will stop at this point only if the SELECTIVE STOP lever switch had previously been set to the up position. After the pattern is entered, the teletype will print XXXX HEX TEST PATTERN SELECTED; XXXX is the test pattern entered in the A register.

If operator previously designated that the 1744 had an 8K memory, the teletype will request that the number of the module to be exercised is entered with the message, TYPE 0 OR 1 TO SELECT MODULE. Type 0 or 1 to make this selection. This typeout will not occur if a 4K memory had previously been indicated.

Phase 3 test will continually be repeated until: an error occurs and the teletype prints out that error message; or the test is to be manually exited.

Phase 4

Depressing the teletype MANUAL INTERRUPT pushbutton while phase 3 is in progress will cause the test program to advance to phase 4.

Entry into phase 4 is indicated by the teletype message R OR W. Type R if a continuous read operation is to be performed or W if a continuous write operation is to be performed. The teletype will print ENTER TEST PATTERN IN A REG RUN. This is a request for the user to enter the test pattern to be used for the operation into the A register operation of the computer. After the pattern is entered, the teletype will print XXXX TEST PATTERN SELECTED; XXXX is the test pattern selected in hexadecimal.

If an 8K memory had previously been indicated, the teletype will print TYPE 0 OR 1 TO SELECT MODULE. The user replies by typing 0 or 1, depending on the module to be exercised. The request for module selection will not be printed out if a 4K buffer memory had previously been indicated.

Phase 4 execution will begin with the input of the data above. It will continually be repeated until the user desires to exit the core test program by depressing the SELECTIVE SKIP lever switch.

TECHNICAL DESCRIPTION

General

Figure 3 illustrates, on a basic block level, the data transfer path used during the core write operation. Each interconnecting line represents a 16-bit transfer path.

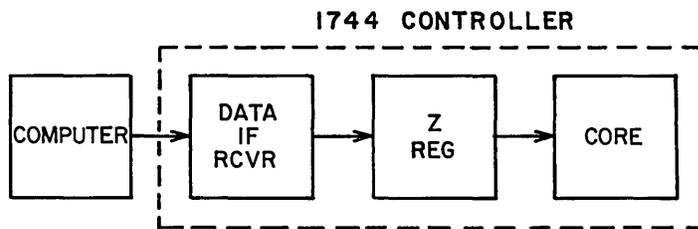


Figure 3. Core Write-Data Transfer for Path

Figure 4 is an example of the data transfer logic used during a core write operation. The logic unique to the transfer of bit 03 is illustrated.

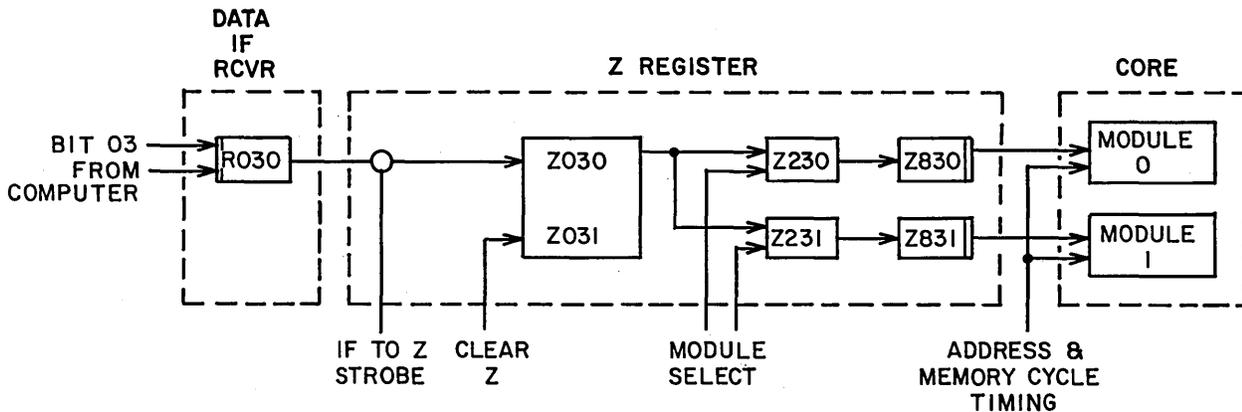


Figure 4. Core Write - Bit 03 Logic Circuit

Additional inhibited gates and loads are not shown in the figure; they are not used for data transfer during core write. Though they are not used, they may be a probable trouble area for this operation.

The basic block diagram of the core read data transfer path is illustrated in Figure 5.

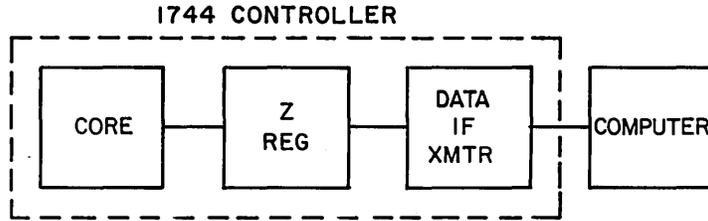


Figure 5. Core Read - Data Transfer Path

Figure 6 illustrates the data path associated with transferring a bit during the core read operation on a logic circuit level. Bit 03 is used as an example.

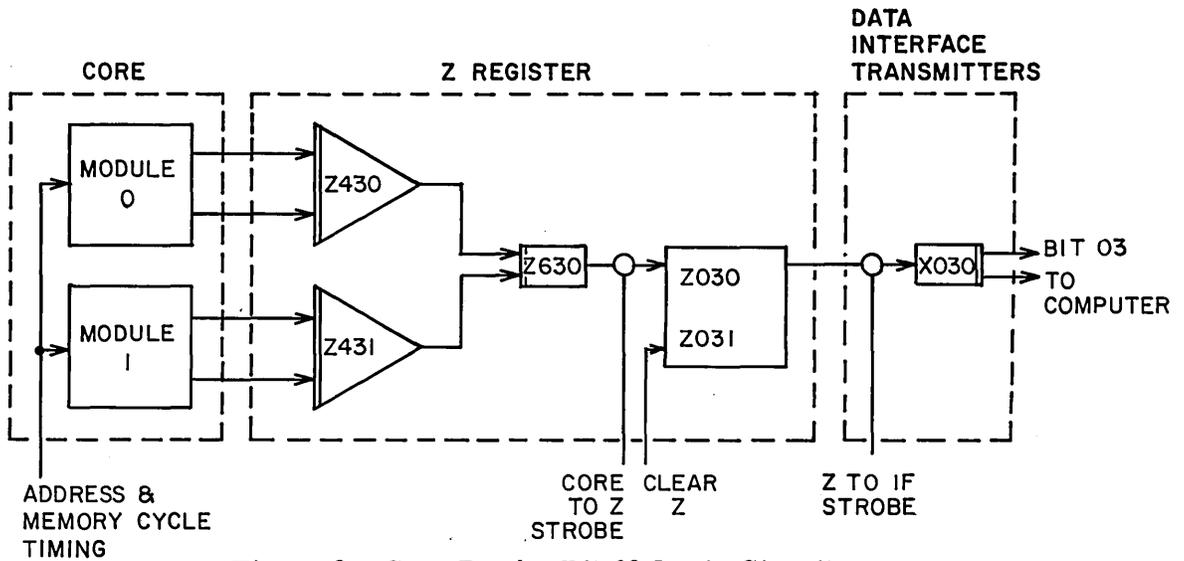


Figure 6. Core Read - Bit 03 Logic Circuit

Although the Z-register flip-flops shown in Figures 4 and 6 illustrate only two of the Z-register set inputs, the 13 low-order flip-flops have additional set inputs from the status selector circuits. These inputs are inhibited during a buffer memory read or write operation, but would present problems if the input gate was enabled due to a malfunction. This also applies to an additional OR input to transmitter X030 in Figure 6.

Phase 1: During phase 1, the 1744 core read/write logic is exercised with 16-bit $FFFF_{16}$ and 0000_{16} bytes. The exact sequencing is described below:

- 1) $FFFF_{16}$ bytes written into every location in Module 0; read and verified.
- 2) Alternate 0000 and $FFFF_{16}$ bytes written into every location in Module 0; read and verified.

If 1744 has an 8K memory, steps 3 and 4 are performed:

- 3) $FFFF_{16}$ bytes written into every location in Module 1; read and verified.
- 4) Alternate 0000 and $FFFF_{16}$ bytes written into every core location in Module 1; read and verified.
- 5) Steps 1 through 4 (1 and 2 in 4K system) repeated ten times.

The test patterns may be expressed in hexadecimal, octal or binary form:

Hexadecimal	$FFFF_{16}$	0000_{16}
Octal	177777_8	000000_8
Binary	$1111\ 1111\ 1111\ 1111_2$	$0000\ 0000\ 0000\ 0000_2$

Phase 1, therefore, exercises buffer memory with 16-bit words containing either all logical 1's or all logical 0's. This test checks the ability of the core read/write logic to process both 1's and 0's and to switch between the two at 600 kc rate. It is also a good check of all the strobing terms used during the buffer memory operations. (See Figures 4 and 6.)

Phase 2: Phase 2 is entered without operator intervention at the completion of phase 1. The test phase exercises the buffer memory Read/Write circuits with 16-bit $AAAA_{16}$ and 5555_{16} bytes. The test sequence is described below:

- 1) A 64-word block of alternate 5555_{16} and $AAAA_{16}$ bytes written into Module 0.
- 2) A 64-word block of alternate $AAAA_{16}$ and 5555_{16} bytes written into Module 0.
- 3) Steps 1 and 2 repeated until Module 0 filled.
- 4) Contents of Module 0 read and verified.
- 5) A 64-word block of alternate $AAAA_{16}$ and 5555_{16} bytes written into Module 0.
- 6) A 64-word block of alternate 5555_{16} and $AAAA_{16}$ bytes written into Module 0.
- 7) Steps 5 and 6 repeated until Module 0 filled.
- 8) Contents of Module 0 read and verified.
- 9) Steps 1 through 8 re-cycled ten times.
- 10) Steps 1 through 9 repeated for Module 1 if 1744 has an 8K memory.

The test patterns may be expressed in hexadecimal, octal or binary form:

Hexadecimal	5555 ₁₆	AAAA ₁₆
Octal	052525 ₈	125252 ₈
Binary	0101 0101 0101 0101 ₂	1010 1010 1010 1010 ₂

Phase 2 exercises the core Read/Write circuits with 16-bit words consisting of alternate logical 1's and 0's, with the 1's and 0's being shifted in successive words. In terms of crosstalk problems, this presents a worst-case test pattern for the memory module and transmission lines. If a crosstalk problem is likely to occur, this test phase will provide every opportunity.

Phase 3: Entry into phase 3 of the core test program (i. e., successful completion of phase 1 and 2) is signaled by the teletype message, ENTER TEST PATTERN IN A REG RUN. This is a request for the user to enter, via the teletype, the test pattern to be exercised.

The selected test pattern is written into every location in buffer memory, read and verified. A failure is indicated by a teletype message defining the error.

Phase 4: Phase 4 is normally entered by depressing the teletype MANUAL INTERRUPT pushbutton while phase 3 is in progress.

The test aids in troubleshooting because it enables the user to select a 16-bit test pattern and have this pattern either continually written into buffer memory or continually read out after a single write operation.

TEST 2: 274 CONSOLE TEST PROGRAM

PURPOSE

Test program 2 generates all the different byte streams necessary to enable the customer engineer to align the 274 Console.

PROCEDURAL DESCRIPTION

The program consists of 18 test phases. The test phases may be advanced using either the teletype or the light pen or a maintenance card located in the 274 Console logic rack. Each technique has its advantages and limitations.

Using the teletype, the operator depresses the MANUAL INTERRUPT pushbutton whenever one test phase is to be changed to another. The teletype types NUMBER, to which the user responds by typing in the new test phase number. With this procedure the user may jump to any test phase so desired; the disadvantage is that the user must leave the console and approach the teletype whenever a test phase is to be changed. The teletype may or may not be in close proximity to the console.

The test phases may be advanced sequentially with the light pen by either of two methods. Depressing the Light Pen switch will advance tests 1 through 14 (tests with high voltage off). Depressing the light pen switch and picking light from the 274 console screen will advance tests 15 through 18 (tests with high voltage on). These are quick and convenient methods for advancing the console tests; the only minor limitation is that tests can only be advanced sequentially.

Each console test phase may be advanced from the rear of the console through use of the maintenance card at location J16. Depressing the momentary switch on the card will sequentially advance the test. The teletype will print out the new phase test number.

The user must determine which of the possible ways of advancing the 274 Console test program is most advantageous to use under a given set of circumstances.

To exit test 2, the SELECTIVE SKIP lever switch is depressed.

The procedure for performing all adjustments associated with each test phase is described in the 274 Digigraphic Console Reference/Customer Engineering Manual, Pub. No. 60279100.

TEST 3: X, Y and S TRANSFERS and ID READ

PURPOSE

The X, Y and S Transfers and ID Read test checks the ability of the 274/1744 to perform computer and internal display, and to time-share between both in one display frame. The test checks the ability of the hardware to respond to and process Read S, Read X, Read Y and Search for ID Byte function code commands. It also checks the ability of the hardware to detect and process the following command bytes: End of Display, Reset, Increment, and ID.

PROCEDURAL DESCRIPTION

Test 3 consists of five major checks. Upon entering the test program, the user performs the Internal/Computer Display check. A dot-cross pattern display on the 274 Console is examined to determine whether it is correct.

The second check is the ID Error check. Several of the displayed dots are chosen with the light pen and the user observes that the teletype does not print an ID error message.

The Forced Printout check is next. A displayed dot is chosen with the light pen. It is immediately followed by a cross choice. A teletype message is printed out defining location parameters associated with the chosen dot. This printout is examined.

To perform the Intensity Levels check, the user enters a preselected Increment byte into the A register of the computer. He then observes the 274 Console for a given display pattern with several intensity levels.

The last check is the Increment Byte Entry feature. The operator enters an Increment Byte of his own choosing into the A register of the computer and observes that the 274 Console displays the byte.

Return to the control program may be accomplished by depressing the SELECTIVE SKIP lever switch on the computer console.

TECHNICAL DESCRIPTION

Internal/Computer Display Check

Upon entering test 3 the console will display the dot-cross pattern illustrated in Figure 7 below.

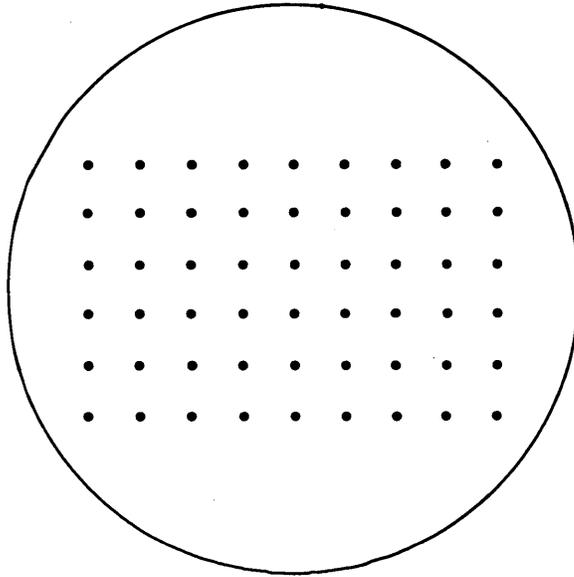


Figure 7. Dot-Cross Pattern Display

All dots are displayed from buffer memory, and the cross is computer displayed. Internal display is initiated by a Function Code 0 (i. e., Command Field = 0), Write command with bit 12 (Start Internal Display Bit) set to 1. Dots are sequentially displayed, left to right, starting at the bottom row.

It is necessary that the user know what command bytes are used to generate the display to better understand what aspects of the hardware are checked during this test. The following describes the byte stream used to generate two consecutive dots. Specific dots are identified by the S register count associated with the Increment byte producing the dot (see Figure 8). As an example, the dot at the bottom left of the display would be identified as Dot 00E. Illustrated below is the byte stream used to produce Dot 01D and Dot 02C.

TABLE 1. BYTE STREAM-DOT 01D AND DOT 02C

	Byte	Purpose
Hexadecimal Character	Type	
841	RESET	Key 1744 logic that next two bytes are new X and Y coordinates; enable light pen sense; and set dim intensity.
C54	X COORDINATE	Horizontal position for dot 01D.
AFF	Y COORDINATE	Vertical position for dot 01D.
FB	ID }	Contain X position data for dot 00E.
1B	ID }	
FA	ID }	Contain Y position data for dot 00E.
FF	ID }	
0	ID }	Contain S register count of increment byte producing dot 00E.
0E	ID }	
0	ID	Contains vertical row count for dot 00E.
0	ID	Contains horizontal row count of dot 00E.
C00	NOP - BEAM ON	Displays dot 01D.
200	NOP	No operation byte, turns beam off.
200	NOP	No operation byte (beam off).
200	NOP	No operation byte (beam off).
841	RESET	Key 1744 logic that next two bytes are new X and Y coordinates; enable light pen sense; and set dim intensity.
D94	X COORDINATE	Horizontal position for dot 02C.
AFF	Y COORDINATE	Vertical position for dot 02C.
FC	ID }	Contain X position data for dot 01D.
5B	ID }	
FA	ID }	Contain Y position data for dot 01D.
FF	ID }	
0	ID }	Contain S register count of increment byte producing dot 01D.
ID	ID }	

TABLE 1. BYTE STREAM-DOT 01D AND DOT 02C

	Byte	Purpose
Hexadecimal Character	Type	
1	ID	Contains vertical row count of dot 01D.
0	ID	Contains horizontal row count of dot 01D.
C00	NOP - BEAM ON	Display dot 02C
200	NOP	No operation byte, turns beam off
200	NOP	No operation byte, (beam off)
200	NOP	No operation byte, (beam off)

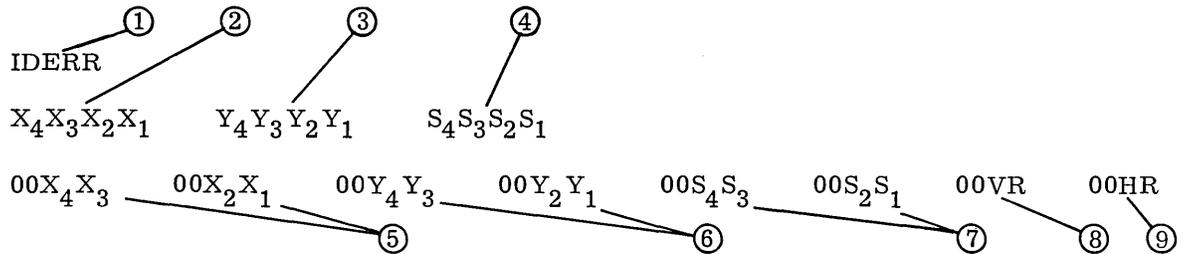
The last byte in the internal display byte stream is an End of Display byte. When decoded, it will set the Priority Interrupt FF, causing the Interrupt line to come up. Sensing an interrupt, the computer will initiate a Function Code 0 Read command to read 1744 status. Having determined that the Priority Interrupt was enabled, the computer will initiate a Function Code 4 Write (computer display) command. The byte stream for the cross is now sent over from the computer and the cross is displayed. This sequence of events is repeated every 25 ms, providing for a 40 frame per second display rate.

ID Error Check

One of the capabilities of test 3 enables the user to check the light pen light detection and interrupt circuitry, X, Y, and S register transfer circuitry, and ID byte detection. When the user chooses a dot with the light pen, the following sequence of events occur:

- a. User chooses dot with light pen.
- b. Light pen amplifier/power supply detect the light, changing it to a logic level.
- c. Light Pen strike logic level transmitted from console to controller where it sets Light Pen (LP) Interrupt FF.
- d. LP Interrupt FF causes 1744 interrupt line to come up. X, Y, S registers frozen.
- e. Computer detects interrupt, comes back with a Function Code 0 Read to determine which interrupt FF was set.
- f. Computer detects light pen has caused interrupt.
- g. Computer initiates a Function Code 4 Read command (Read X). The X register contents represent the X coordinate of the light pen strike.

- h. Computer initiates a Function Code 5 Read command (Read Y). The Y register contents represent the Y coordinates of the light pen strike.
- i. Computer initiates a Function Code 2 Read command (Read S). The S register contents represent core address at time of the light pen strike.
- j. Computer initiates a Function Code 6 Read (Search for ID bytes). The controller starts sequentially addressing and reading core locations, starting from the freeze location. The data bytes read from each core location are placed on the controller data interface transmitter lines. A non-ID byte is accompanied by a Reject signal; ID byte, Reply signal. The ID byte carries the identification parameters associated with the dot that was struck. These parameters include: true X and Y dot location coordinates; true S register count of Increment byte producing dot; and true horizontal and vertical row count.
- k. Computer goes through a verify routine. It compares the X, Y and S register contents associated with the light pen strike to the X, Y and S dot location parameters in the ID byte. If the values differ by a given amount, the teletype will print out an ID error message. The typeout is in hexadecimal.



- ① Indicates typeout is result of ID error.
- ② Contents of X register at time of freeze.
- ③ Contents of Y register at time of freeze.
- ④ Contents of S register at time of freeze.
- ⑤ Two ID bytes; two low-order characters of each, when combined, identify true X coordinate of dot chosen; should be equal to ② .
- ⑥ Two ID bytes; two low-order characters of each, when combined, identify true Y coordinate of dot chosen; should be equal to ③ .
- ⑦ Two ID bytes; two low-order characters of each, when combined, define true S register count (Core address) of increment byte generating chosen dot; should be within three counts of ④ .

- ⑧ ID byte, two low-order characters identify vertical row count of chosen dot.
- ⑨ ID byte, two low-order characters identify horizontal row count of chosen dot.

NOTE

X_4 and/or Y_4 in the ID bytes will be "F" characters (-0) if chosen dot is in negative quadrant.

When an ID error printout occurs, it may have been caused by an error relating to the X, Y or S transfers or by an error unique to ID byte processing or both. To aid in isolating a trouble to a given area, refer to Figure 8. It illustrates all the dots displayed on the CRT and their X and Y coordinates, and S register count. By relating the ID error printout to the figure, the user can more easily categorize a trouble.

Forced Printout Check

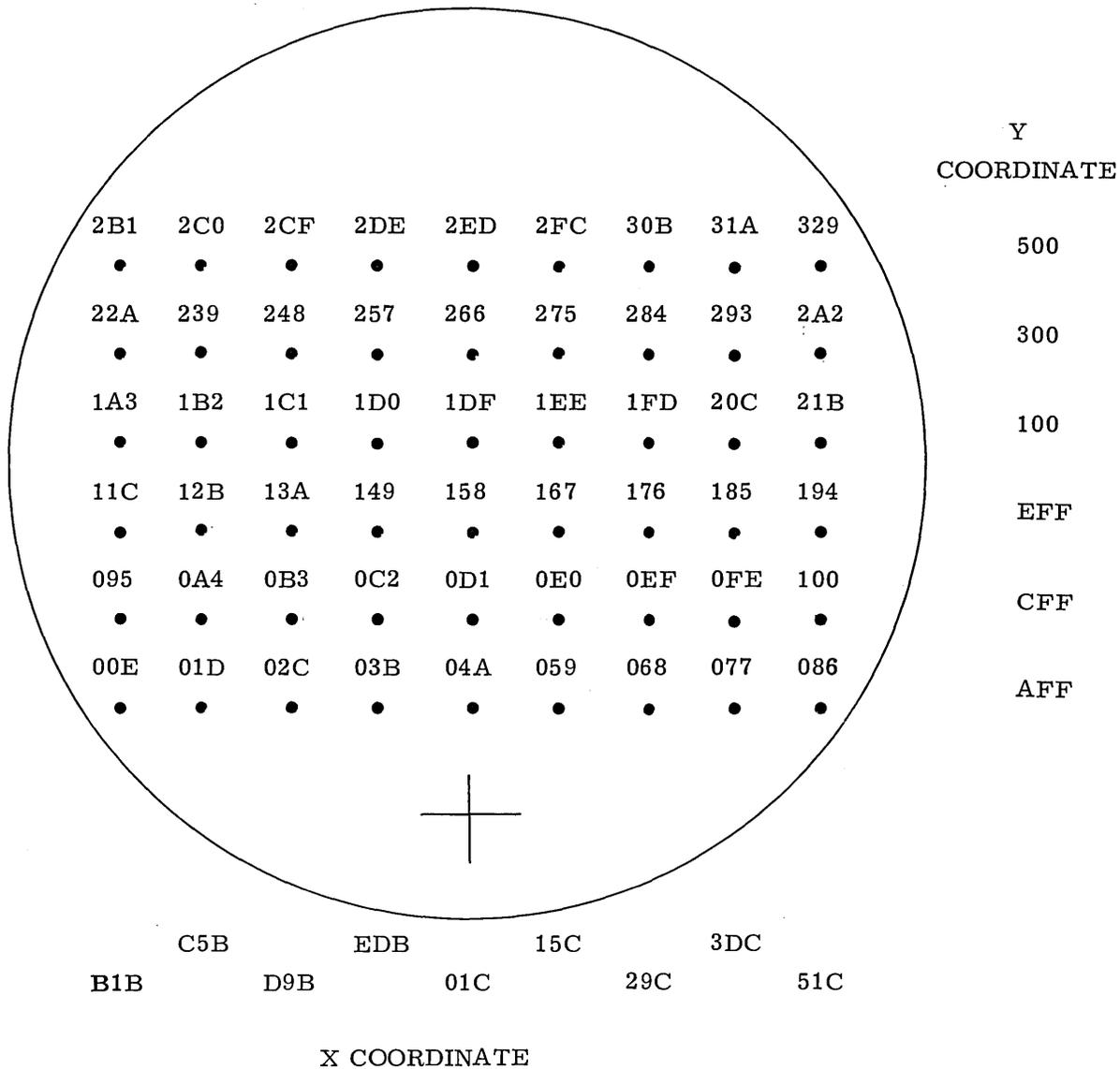
The forced printout check enables the user to have the identification parameters associated with any selected dot printed out on the teletype. To exercise the test, the user picks one of the displayed dots. It is important to note that the next dot in sequence goes out. This verifies that the choice has been made. The user then chooses the cross. Upon choosing the cross, the teletype will print out the following message:

```

C R O S S
X4X3X2X1   Y4Y3Y2Y1   S4S3S2S1
00X4X3  00X2X1  00Y4Y3  00Y2Y1  00S4S3  00S2S1  00VR  00HR

```

The term "CROSS" signifies this printout was a result of a dot-cross choice. The remainder of the printout format is described in the ID Error Check. The Figure 9 typeout was obtained by choosing each dot in the bottom row.



1. All numbers in hexagon.
2. Numbers above dots represent S register counts of byte producing dot.

Figure 8. Dot Location Diagram

```

CROSS
0B1B 0AFF 000E
00FB 001B 00FA 00FF 0000 000E 0000 0000
CROSS
0C5B 0AFF 001D
00FC 005B 00FA 00FF 0000 001D 0001 0000
CROSS
0D9B 0AFF 002C
00FD 009B 00FA 00FF 0000 002C 0002 0000
CROSS
0EDB 0AFF 003B
00FE 00DE 00FA 00FF 0000 003B 0003 0000
CROSS
001C 0AFF 0049
0000 001C 00FA 00FF 0000 004A 0004 0000
CROSS
015C 0AFF 0059
0001 005C 00FA 00FF 0000 0059 0005 0000
CROSS
029C 0AFF 0068
0002 009C 00FA 00FF 0000 0068 0006 0000
CROSS
030C 0AFF 0076
0003 00DC 00FA 00FF 0000 0077 0007 0000
CROSS
051C 0AFF 0086
0005 001C 00FA 00FF 0000 0086 0008 0000

```

Figure 9. Dot-Cross Typeout - Bottom Dot Row

Note that whenever a dot lies in a negative quadrant, the ID bytes defining that coordinate parameter are prefixed with an F character, rather than a 0.

Intensity Levels Check

The intensity levels check enables the user to check the ability of the 1744 and 274 to detect, decode, and process dim, medium and bright intensity commands. The byte stream producing the dots in test 3 contained the three intensity levels, but with only dots displayed, it is difficult to distinguish different intensity levels. With the intensity levels check, the user enters an increment byte in the computer A register with a scale factor of 7, and delta X and delta Y equal to +7. This produces a series of 45 degree lines on the console display, replacing the dots. The lines at the left one-third of the display are of a dim intensity, center one-third, medium intensity, and right one-third, bright intensity.

Increment Byte Entry Feature

Test 3 has an option which enables the user to enter any desired increment byte into the A register of the computer. The increment will then be displayed at each previous dot location. This feature is a useful tool to the customer engineer because all the logic circuitry associated with processing of varied increment bytes can be checked. The 274/1744 logic associated with processing the following byte characteristics can be checked:

- a. Beam on/off.
- b. Scale factors 2 through 7.
- c. All combination of positive and negative delta X and delta Y values.

TEST 4: COMMAND TEST PROGRAM

PURPOSE

The command test program checks the ability of the hardware to execute all 1744 jump commands (i. e., S Jump, Macro Call, P Jump and Return to Main). It checks that the hardware can detect and process the following bytes: End of Display, Reset, and Increment.

PROCEDURAL DESCRIPTION

There is only one test phase in the command test program. When the test is entered, the user observes the 274 Console for a given display. A correct display indicates successful execution of test 4.

TECHNICAL DESCRIPTION

Upon entering the test program, the appropriate commands are sent from the computer to the controller to enable the sorting of all bytes used in this test into buffer memory. An execute internal display command is initiated and the console presentation is controlled by the jump commands. The display conforms to the following pattern:

SSSSSSSSSMMMMMMMMMMPPPPPPPPRRRRRRRRRRE

The letters in proper number and sequence convey the following information:

- 10 S's successful execution of S Jump
- 10 M's successful execution of Macro Call
- 10 P's successful execution of P Jump
- 10 R's successful execution of Return to Main
- 1 E detection of End of Display byte (10 E's indicate failure to detect byte)

To better understand how the display is generated, refer to Chronological Description, Command Test. The chart at the left represents buffer memory locations of Module 0 (location 0 through 4096₁₀ or 0 through 1000₁₆). Data in the chart identifies the bytes or byte streams used; hexadecimal characters defining the byte structure are also shown.

CHRONOLOGICAL DESCRIPTION, COMMAND TEST

	MODULE 0 CONTENTS	Location (Hex)
① Reset beam to coordinate DA7 in X and 258 in Y; set medium intensity level.	① RESET (802) X COORDINATE (DA7) Y COORDINATE (258)	0
② S JUMP CMD detected; S register incremented by 1.	② S JUMP CMD (1C8)	
③ S JUMP ADDRESS read out of core; strobed to Z register, to S buffer, to S register and addresses core.	③ S JUMP ADDRESS (300)	
④ S JUMP location; contains the byte stream for displaying the letter S; S byte stream repeated ten times.	* END OF DISPLAY (1F8's) (many)	
⑤ MACRO CALL CMD detected; S register incremented by 1.	⑦ M's (10 times)	0100
⑥ MACRO ADDRESS read out of core; strobed to Z register, to S buffer, to S register and addresses core; core location of MACRO ADDRESS stored in P register.	⑧ P JUMP CMD (1D8)	
⑦ MACRO Location; contains the byte stream for displaying the letter M; M byte stream repeated ten times.	* END OF DISPLAY (1F8's) (many)	
⑧ P JUMP CMD detected; location stored in P register, i. e., 6 incremented by 1 and strobed into the S register addressing core at this location.	⑩ P's (10 times)	0200
⑨ P JUMP ADDRESS read out of core; strobed to Z register, to S buffer, to S register, and addresses core at this location, core location of P JUMP ADDRESS stored in P register.	⑪ RETURN TO MAIN CMD (1FA)	
⑩ P JUMP location; contains the byte stream for displaying the letter P; P byte stream repeated ten times.	* END OF DISPLAY (1F8's) (many)	
⑪ RETURN TO MAIN CMD detected; location stored in P, i. e. 9 incremented by 1 and strobed into the S register addressing core at this location.	④ S's (10 times)	0300
⑫ Location contains byte stream for displaying the letter R; R byte stream repeated ten times.	⑤ MACRO CALL CMD (1E8)	
⑬ S JUMP CMD detected; S register incremented by 1.	⑥ MACRO ADDRESS (100)	
⑭ S JUMP ADDRESS read out of core; strobed to Z register, to S buffer, to S register and addresses core.	⑨ P JUMP ADDRESS (200)	
	⑫ R's (10 times)	037B
	⑬ S JUMP CMD (1C8)	
	⑭ S JUMP ADDRESS (D00)	
	* END OF DISPLAY (1F8's) (many)	
	⑮ E -	0D00
	⑯ END OF DISPLAY (1F8)	
	** E's (9 times)	
	* END OF DISPLAY (many) (1F8's)	1000
	⑮ Locations contain the byte stream for displaying the letter E, once.	
	⑯ END OF DISPLAY byte detected, display is terminated, will be repeated once every 25 ms.	

*Each * represents many locations. End of Display bytes fill all of these locations. If one of them is addressed due to a malfunction, display will be terminated for the remainder of the display frame.

**Locations contain the byte stream for displaying the letter E; E byte stream repeated nine times. If the END OF DISPLAY byte at 16 is not decoded these will be displayed.

The byte stream used for generating a single letter M is illustrated below. It is typical of the byte streams used to display the other letters because it consists only of beam on and off Increment bytes of varying magnitudes.

BYTE STREAM FOR LETTER M

<u>Hexadecimal Character</u>	<u>Type</u>
D04	Increment byte with beam on
D02	Increment byte with beam on
D39	Increment byte with beam on
4C4	Increment byte with beam off
D34	Increment byte with beam on
4CB	Increment byte with beam off
D0B	Increment byte with beam on
D0D	Increment byte with beam on
522	Increment byte with beam off
4D0	Increment byte with beam off

To determine how test 4 would respond to different troubles, the Set and Clear outputs of each command flip-flop were alternately grounded (simulating a logical 0 at the ground point) and the display recorded. These are the results:

TROUBLE	CONSOLE DISPLAY
Set Output Grounded:	
S Jump - B710/711	•
Macro Call - B750/751	SSSSSSSSSRRRRRRRRRRE
P Jump - B730/731	SSSSSSSSSMMMMMMMMMM
Return to Main - B770/771	SSSSSSSSSMMMMMMMMMM
	PPPPPPPPP
Term Internal Display - B772/773	SSSSSSSSSMMMMMMMMMM
	PPPPPPPPRRRRRRRRRRR
	EEEEEEEEEE

Clear Output Grounded:
Any above flip-flop Console screen blank

An analysis of the contents of buffer memory during test 4 will illustrate why specific results were obtained. The only result that is not readily obvious by examining core contents is the blank display obtained when any one of the Clear outputs of the flip-flops was grounded. Under these conditions, the Set output is forced to a logical 1. The Set outputs of all jump command flip-flops are applied to inverter B405.

The B405 term is needed to enable the Set input AND gate at E200/201 in the Byte Processing Timing Circuits. Under these conditions, the gate is inhibited by B405 and consequently, the console screen is blank.

TEST 5: MEMORY DUMP PROGRAM

PURPOSE

The memory dump program enables the user to have the contents of the 1744 Controller memory printed out on the teletype. He has the option of selecting the first word address and the number of words in the dump. Hardware must be capable of processing S register Write and Read Core commands before test 5 can be executed.

PROCEDURAL DESCRIPTION

There is only one test phase in the memory dump program: the dump itself. When the program is entered, the teletype prints FWA. This is a request for the operator to enter, via the teletype, the first word address of the transfer. He replies by entering this information in hexadecimal. The teletype will then request the number of words desired in the transfer, with the message, NWDS. This information should be entered in decimal. With the last input, the program takes over and executes the dump, printing out the information, in hexadecimal, on the teletype.

TECHNICAL DESCRIPTION

With the input of the necessary information to perform a dump, the hardware executes an S register Write command (Function Code 2, Write). This command enables 13 bits to be transferred from the computer A register to the 1744 data interface receivers through the S buffer to the S register. The address entered into the S register is the one the user specified by his reply to the teletype message, FWA. The computer next performs a Read Core operation (Function Code 1, Read). Bytes are sequentially read out of 1744 core, routed through the Z register, to the data interface transmitters to the computer. A new core location is read and outputted every 1.67 μ sec. A reply accompanies each byte transfer.

The computer outputs the received data to the teletype where it is recorded.

TEST 6: KEYBOARDS TEST PROGRAM

PURPOSE

The Variable Function and/or Alphanumeric keyboards are checked out during test 6. The ability of the keyboards to be activated or deactivated under program and manual control is checked along with the ability of the computer to recognize which of the keyboard keys have been depressed.

PROCEDURAL DESCRIPTION

Test 6 contains a separate checkout procedure for the Variable Function and Alphanumeric keyboards. Assuming both are to be checked, begin with the Variable Function keyboard.

Prior to entering the test, activate and deactivate the keyboard manually. Leaving the keyboard deactivated, enter test 6 and observe that the test program could activate it. Depress the keyboard keys and observe that the keys illuminate and that the 274 Console displays the bit number associated with the key. After completing the above checks, manually deactivate the keyboard and exit test 6.

To check out the Alphanumeric keyboard, manually activate and deactivate the keyboard prior to re-entering test 6. Leaving the keyboard in the activated state, enter test 6 and observe that the program deactivates the keyboard. At present, the program has the ability of activating only the Variable Function keyboard. Manually activating the Alphanumeric keyboard, systematically depress each key and observe that the 274 Console displayed the proper bit numbers associated with the keyboard 8-bit ASCII code.

Depressing the SELECTIVE SKIP lever switch exits test 6.

TECHNICAL DESCRIPTION

When either keyboard is manually activated, a logical 0 is generated by the ON/OFF. The activate command is routed through the 274 Console to the 1744 Controller, where it is processed. In the controller, there is logic circuitry that is unique to the ON/OFF status of each keyboard. This circuitry will be affected by the momentary signal generated by the switch, and it will change the signal to an activate hold signal for the activated keyboard and a deactivate signal for the other. The outputs are transmitted to the 274 Console to light driver

cards in the keyboard logic. The light driver cards associated with the activated keyboard will generate a ground to that keyboard. This ground will activate the keyboard, illuminating the ON/OFF lamp. During manual activation, this is the only way that the lamp can be illuminated. The ON/OFF lamp on the non-selected keyboard will either become extinguished or remain extinguished depending on its previous state.

With the current program, only the Variable Function keyboard can be activated by the test program. This is accomplished by a Function Code 7, Write Command.

After a keyboard has been activated, any key that is depressed will generate a delta keyboard signal. This signal will be directed through the 274 Console to the controller. Upon receipt of this input, the controller will generate an interrupt. The computer, in turn, will read controller status (Function Code 0, Read). Having determined that a keyboard interrupt has occurred, the computer will read keyboard status (Function Code 7, Read). The status of the activated keyboard will be placed on the A register lines. The computer will examine the bit positions associated with the keyboard status input. If it detects a logical 1 in a specific bit position, it will send a byte stream over to the digigraphics to display the bit position character(s). The display will be all or part of: 07 06 05 04 03 02 01 00.

On the Variable Function keyboard, the Accept and Reject (green and red) keys are momentary switches and must be held in the down position to display their respective bit position. The remaining keys, associated with bits 02 through 15, are latching switches, and need only be latched in the down position.

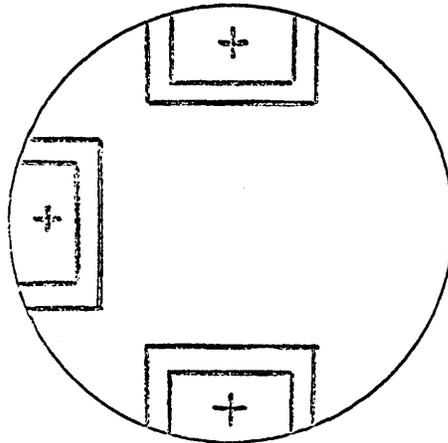
The Alphanumeric keyboard utilizes an 8-bit ASCII code to identify a depressed key. The high-order bit is an Even Parity bit. All the keys activate momentary switches. Unlike the Variable Function, the key does not have to be held in the depressed position to obtain a display, because the outputs are strobed into eight flip-flops in the console keyboard logic. The ASCII code of the last depressed key is stored at these flip-flops. The contents are changed whenever a new key is depressed.

It is significant that the keyboard and 274 Console outputs reflect the negated version of the bit or bits associated with the depressed key.

TEST 7: SPARE (NOT USED)

TEST 8: SCISSORING TEST PROGRAM

Improper scissoring will result in the deformation of the display, which takes the following form:



TEST 9: VELOCITY COMPENSATION TEST PROGRAM

PURPOSE

The velocity test pattern permits adjustments of the 274 console for improved velocity compensation when W09, Rev D and W07, Rev G are inserted in the console. This test is for use on the 1744/274, both old and new resets, and on the 3344/274.

DESCRIPTION

Three groups of diagonal lines are displayed, each group representing one of the three available intensity levels. All three groups have the same byte structure, except for the intensity bit in the increment bytes.

Each diagonal line is made up of repeated vectors of a single scale factor and increment size, representing one of the 42 possible combinations available (6 scale factors X 7 increment factors).

A brief review of the structure of the increment byte is useful here. It has the format.

b f f f (ΔX) (ΔY)

where:

- b = intensity
- fff = scale factor = 2, 3, 4, 5, 6, or 7
- (ΔX) = X-increment (4 bits, with sign)
- (ΔY) = Y-increment (4 bits, with sign)

Whenever an increment byte is encountered, the contents of the X and Y interface registers are incremented as follows:

$$X^1 = X + (\Delta X) \cdot 2^{fff - 2}$$

$$Y^1 = Y + (\Delta Y) \cdot 2^{fff - 2}$$

The multipliers are 2^0 , 2^1 , 2^2 , 2^3 , 2^4 , and 2^5 ; i.e., 1, 2, 4, 8, 16, and 32. Since ΔX and ΔY are four signed bits, then the total number of distinct (positive) increments is $6 \times 7 = 42$. The maximum change in either interface register is therefore $0111_2 \times 32 = 7 \times 32 = 224$.

Each set of 42 lines is generated by 42 separate reset bytes, followed by calls to the same basic set of macros. (Recall that beam intensity is established by the reset sequence.) Each line macro consists of a single type of increment byte (with positive and equal ΔX and ΔY), repeated enough times to give a line approximately 2 inches long, on the diagonal.

The length of lines can be computed from the increment bytes, using the beam-lag factor which is built into the 274 Console; i.e., whenever one of the interface registers is incremented, the corresponding beam coordinate is inhibited from changing by more than half of the difference between the new register value and the old beam coordinate, during the remainder of the current clock cycle (1.67 microseconds).

For example, consider the case of maximum ΔX and ΔY, obtained by using scale factor 7 (multiplier 32) and increments of 32 in both X and Y. The increment byte for this would be:

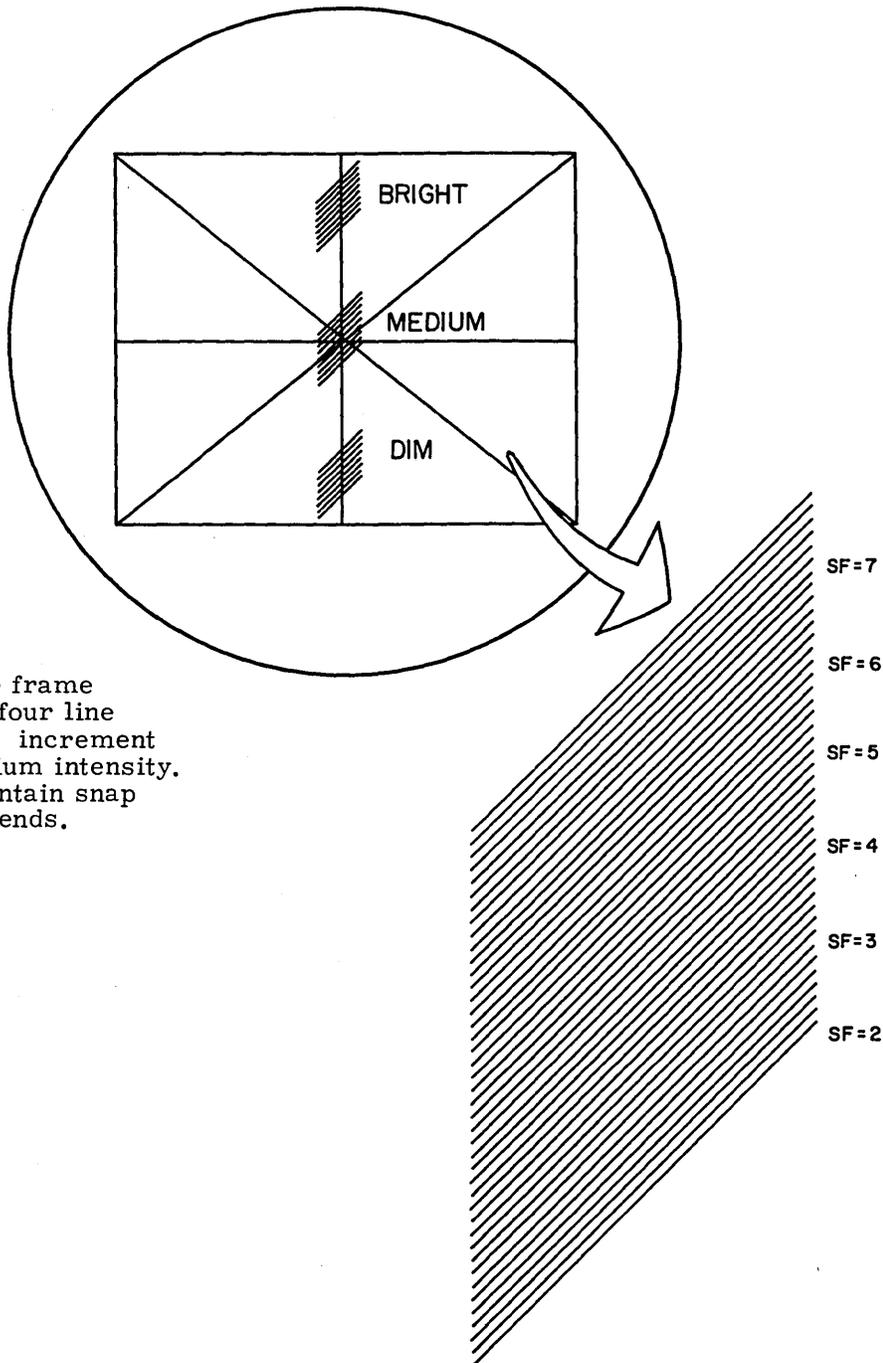
1 1 1 1 0 1 1 1 0 1 1 1
b f f f ΔX ΔY

This increment byte causes the X and Y interface register to be increased by 224, each time the byte is processed. If several such bytes are processed in succession, starting with $X_0 = Y_0 = 0$ in the registers, the register values and follow-up beam coordinates can be represented as follows:

<u>Cycle</u>	<u>Register Values</u>	<u>Beam Coordinates at End of Cycle</u>	<u>Change in Beam Coord. (ΔH & ΔV)</u>
0	0	0	0
1	224	112	112
2	448	$(448-112)/2 + 112$ = 280	168
3	672	$(672-280)/2 + 280$ = 476	196
4	896	686	210
5	1120	903	217
		.	
		.	
		.	

It can be seen that ΔH and ΔV will approach the maximum of 224 display grid units, which is the maximum change in the interface registers. Therefore, the upper limit on beam movement for a single increment byte is approximately $(224/200) \times 1.4$ inches = 1.57 inches on the diagonal. For this case ($fff = 7$ and $\Delta X = \Delta Y = 32$), two increment bytes are used, giving a line $(280/200) \times 1.4 = 1.96 \approx 2$ inches.

The display pattern is illustrated in the figure below. A line of medium intensity surrounds the three patterns, as shown:



NOTE: The frame consists of four line segments 7, increment 7, and medium intensity. All lines contain snap back at the ends.

5-21A-E000 H

KEY	Upper Case Keys		274 CONSOLE DISPLAY						
	SHIFT	CTRL							
1			07	05	04				00
2			07	05	04			01	
3				05	04			01	00
4			07	05	04		02		
5				05	04		02		00
6				05	04		02	01	
7			07	05	04		02	01	00
8			07	05	04	03			
9				05	04	03			00
0				05	04				
:				05	04	03		01	
-				05		03	02		00
Q			07	06		04			00
W			07	06		04	02	01	00
E			07	06			02		00
R			07	06		04			01
T			07	06		04		02	
Y				06		04	03		00
U				06		04	02		00
I			07	06			03		00
O			07	06			03	02	01
P				06		04			
LINE FEED							03		01
RE-TURN			07			03	02		00
A				06					00
S				06		04			01
D				06			02		
F			07	06			02	01	
G				06			02	01	00
H				06			03		
J			07	06			03		01
K				06			03		01
L			07	06			03	02	
;			07		05	04	03		01
RUB OUT			07	06	05	04	03	02	01
OUT			07	06	05	04	03	02	01

5-4-E04

TABLE 2. ALPHA NUMERIC KEYBOARD CHART

KEY	Upper Case Keys		274 CONSOLE DISPLAY						
	SHIFT	CTRL							
Z				06		04	03		01
X			07	06		04	03		
C			07	06					01
V				06		04		02	01
B				06					01
N				06				03	02
M								03	02
,			07		05		03	02	
.					05		03	02	01
/			07		05		03	02	01
!	dep				05				00
,,	dep				05				01
#	dep		07		05				01
\$	dep				05			02	
%	dep		07		05			02	00
&	dep		07		05			02	01
,	dep				05			02	01
{	dep				05			03	
}	dep		07		05			03	00
*	dep		07		05			03	01
=	dep		07		05	04	03	02	00
WRU		dep						02	00
TAPE		dep				04			01
TAPE		dep				04		02	
TAB		dep						03	00
←	dep			06		04	03	02	01
@	dep		07	06				-	
X OFF		dep	07			04			01
EOT		dep	07					02	
RU		dep						02	01
BELL	dep		07					02	01
VT	dep		07				03		01
FORM		dep						03	02
+	dep				05			03	01
	dep		07	06		04	03	02	01
<	dep				05	04	03	02	
>	dep		07		05	04	03	02	01
?	dep				05	04	03	02	01

1744/274 DIGIGRAPHICS DISPLAY SYSTEM
(DG406F Test No. 6F)

I. INTRODUCTION

A. IDENTIFICATION

1. Type of Program - Diagnostic test under 1700 System Maintenance Monitor (SMM17)
2. Computer - CONTROL DATA 1700/SC17

B. PURPOSE

The digigraphics display system test operates under the control of the 1700 System Maintenance Monitor to verify all of the operating features and graphics display capabilities of the 1744 Digigraphics Controller and the 274 Digigraphics Display Console. It also provides graphic patterns for alignment. The test consists of 8 sections (0-7) selected by corresponding bits set in test parameter. Sections are executed sequentially beginning with the lowest number selected.

C. RESTRICTIONS

1. Minimum core requirements - 12K.
2. The test is designed for compatibility with either the 1700 or SC17 processor. Bit 2 of SMM parameter must be set if running on an SC17 processor.
3. Operator intervention is required in the following sections:
 - a. Section 05 - Pattern Alignment Test (PALTST)
(if alignment is necessary)
 - b. Section 06 - Scale Factor Test (SCLTST)
(when scale factors are maladjusted)
 - c. Section 07 - Keyboard Test (KYBTST)
(to check correct functioning of AN/KB and /or VFKB, keys must be depressed by operator)

D. SPECIAL FEATURES

The following special features are implemented by selectable parameters in test parameter word 1:

1. Test may run either buffered (1706 BDC) or unbuffered.
2. Flexible running time - long or short test implies cycling through 5 times (45 sec) for short or 15 times (1 min. 45 sec) for long (Memory test).
3. The current section being run may be terminated and the next selected section started by light pen picking of the displayed word "NEXT" located at lower center of CRT (coordinates X = \$F69, Y = \$900).
4. Display of error message on 274 console. This feature provides for display of the first 9 words of the error message on the console, in addition to the normal error reporting, via A/Q or Teletypewriter.
5. Optional short error message feature terminates error message after 5 stops. Long error message provides 10 stops to include applicable register contents.

II. REQUIREMENTS

A. HARDWARE

1. Minimum Configuration

17X4 Mainframe
17XX Storage Increment
17X5 Interrupt Data Channel
1744 Digigraphic Controller (4K)
274 Digigraphic Display Console

2. Target Configuration

The minimum configuration expanded to include:

1706 Buffered Data Channel
274 Digigraphic Display Console with optional:

Alphanumeric Keyboard
Variable Function Keyboard

1711/12/13 Teletypewriter

3. Maximum Configuration

The target configuration expanded to include:

An additional 4K memory module for the 1744 Digigraphic Controller

III. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test must be loaded under the standard SMM17 loading procedures as test number 6F.

B. PARAMETERS

1. Stop 1

A	Q
6F31	Stop/Jump

A = Test Number, Number of Stops, Type of Stop

Q = Stop/Jump

- Bit 0 = Stop to Enter Parameters
- Bit 1 = Stop at End of Test Section
- Bit 2 = Stop at End of Test
- Bit 3 = Stop on Error
- Bit 4 = Repeat Condition
- Bit 5 = Repeat Section
- Bit 6 = Repeat Test
- Bit 7 = Not Used
- Bit 8 = Omit Typeouts
- Bit 9 = Bias Return Address Display
- Bit 10 = Reenter Parameters
- Bit 11-15 = Not Used

2. Stop 2

A	Q
Testing Modes	Interrupt Line No.

A = Testing modes in following format:

- Bit 0 = Long Test
- Bit 1 = Buffered Data Control
- Bit 2 = 274 Console Section Selection
- Bit 3 = 274 Console Error Message Display
- Bit 4 = Variable Function Keyboard (VFKB)
- Bit 5 = Alphanumeric Keyboard (AN/KB)
- Bit 6 = Short Error Message
- Bit 7 = Run in Memory Stack 1
- Bit 8-15 = Not Used

Q = Interrupt Line

The interrupt line is selected by setting the bit corresponding to interrupt line number desired, e.g.: Bit 7 set, interrupt line 7 is selected. This parameter should not be changed after the initial parameter stop.

3. Stop 3

A	Q
Test Sections	OPR. SEL. Test Pattern

A = Test Sections

The desired test sections to be executed will be selected by setting bits corresponding to the section numbers, e.g.: Bit 0 = Section 0. An optional method may be used to select the next section using light pen picking from the word "NEXT" displayed on the console.

Q = Operator Selected Test Pattern

The operator may select a bit configuration of his choice as the final memory test pattern. If no selection is made, the final memory test pattern will be \$01F8.

C. MESSAGES

Message timeout will not occur if bit 8 of Stop/Jump word is set.

1. Test title and initial address typeout:

DG406F 1744/274 Digigraphic Test. IA = XXX, FC = XX
--

XXX is the initial address of the test.
XX is the frequency count.

2. Section running typeout:

Running Section X

X is section number.

3. End of Section.

A	Q	A	Q
6F22	Stop/Jump Word	Section/ Number	Return Address

4. End of Test.

A	Q	A	Q
6F24	Stop/Jump	Pass Count	Return Address

D. ERROR MESSAGES

All errors are in SMM17 format. The return address indicates the origin of the error reported. The error code is divided into two hexadecimal digits, the lower order digit indicates the error condition while the next significant digit indicates the error type. The uppermost two hexadecimal digits will be the section number, (XXYZ).

Where XX = Section Number

Y = Type of Error

Z = Error Condition Code

For specific error code and maintenance aids, see Appendix A.

1. Definition of error types:

<u>Type</u>	<u>Definition</u>
0	Buffered data channel input
1	Buffered data channel output
2	Direct A/Q channel input

<u>Type</u>	<u>Definition</u>
3	Direct A/Q channel output
4	Controller status data (0-7)
5	Controller status data (8-15)
6	Not used
7	Input and output command/function
8	Data compare
9	Register content
A	Not used
B	Interrupt

2. Error conditions defined by types:

Type 0 - Buffered Data Channel Input

<u>Code</u>	<u>Condition</u>
0	Not used
1	External reject on status input (1706)
2	Internal reject on status input (1706)
3	Not used
4	External reject on buffered data input
5	Internal reject on buffered data input
6-9	Not used
A	Un-terminated buffer transfer
B	External reject on 1706 function
C	Internal reject on 1706 function
D	Buffered data channel input failure

Type 1 - Buffered Data Channel Output

<u>Code</u>	<u>Condition</u>
0	Not used
1	Buffered data channel output failure
2	Probable memory failure (RUN MEMTSX)
3	Not used
4	External reject on buffered data output
5	Internal reject on buffered data output

Type 2 - Direct A/Q Channel Input

<u>Code</u>	<u>Condition</u>
0	External reject on controller status input
1	Internal reject on controller status input
2	External reject on direct data input
3	Internal reject on direct data input
4	External reject on S-reg input
5	Internal reject on S-reg input
6	External reject on P-reg input
7	Internal reject on P-reg input
8	External reject on X-reg input
9	Internal reject on X-reg input
A	External reject on Y-reg input
B	Internal reject on Y-reg input
C	External reject on ID byte search input
D	Internal reject on ID byte search input
E	External reject on KYBD status input
F	Internal reject on KYBD status input

Type 3 - Direct A/Q Channel Output

<u>Code</u>	<u>Condition</u>
0	External reject on controller function output
1	Internal reject on controller function output
2	External reject on direct data output
3	Internal reject on direct data output
4	External reject on S-reg address output
5	Internal reject on S-reg address output
6	External reject on terminate computer display
7	Internal reject on terminate computer display
8	External reject on computer display
9	Internal reject on computer display
A	External reject on KYBD function output
B	Internal reject on KYBD function output

Type 4 - Controller Status Data 0-7

<u>Code</u>	<u>Condition</u>
0	Unexpected status
1	Console power off (disabled)
2	KYBD interrupt did not enable

Type 5 - Controller Status Data (Keyboard)

<u>Code</u>	<u>Condition</u>
0	Variable function keyboard did not activate
1	Variable function keyboard did not deactivate
2	Alphanumeric keyboard did not activate
3	Alphanumeric keyboard did not deactivate

Type 6 - Not Used

Type 7 - Input/Output Command/Function

<u>Code</u>	<u>Condition</u>
0	Status data input not functioning
1	Input data command not functioning
2	S-Reg input not functioning
3	P-Reg input not functioning
4	X-Reg input not functioning
5	Y-Reg input not functioning
6	Search ID byte not functioning
7	Keyboard status data input not functioning
8	Reject on clear controller function
9	Output data command not functioning
A	Starting I/O address output not functioning

Type 8 - Data Compare

<u>Code</u>	<u>Condition</u>
0	Memory address error - content incorrect
1	Incorrect storage word content
2	Not used
3	Parity plane test storage error

Type 9 - Register Content

<u>Code</u>	<u>Condition</u>
0	S-register content error
1	P-register content error
2	X-register content error
3	Y-register content error

Type A - Not used

Type B - Interrupt Errors

<u>Code</u>	<u>Condition</u>
0	Not used
1	Internal reject status input
2	External reject status input
3	Internal reject KB status input
4	External reject KB status input
5	Internal reject CLR INTRPT output
6	External reject CLR INTRPT output
7	Internal reject CLR KB INTRPT output
8	External reject CLR KB INTRPT output
9	Interrupt failed to CLR
A	Internal reject - status input after CLR
B	External reject - status input after CLR
C	Unexpected interrupt
X	Reject code stored here for register input
E	PRI failed to occur
F	PRI FF failed to enable

3. Error Message Formats

Parameter entry permits the operator to select long or short error message formats. All console displayed errors will be short format. Error display will not appear on console for sections 2, 3, and 4. Short message format:

Stops 1		2		3		4		5	
A	Q	A	Q	A	Q	A	Q	A	Q
6F58	S/J	SS/XY	RTA	ACT	FUNCT	EXP	DASTA	KBSTA	MEMADR

Long Message format:

Stops 1		2		3		4		5	
A	Q	A	Q	A	Q	A	Q	A	Q
6FA8	S/J	SS/XY	RTA	ACT	FUNCT	EXP	DASTA	KBSTA	MEMADR

Stops 6		7		8		9		10	
A	Q	A	Q	A	Q	A	Q	A	Q
S-EXP	S-ACT	PEXP	P-ACT	X-EXP	X-ACT	Y-EXP	Y-ACT	ID-EXP	ID-ACT

For reject codes stop 3 is the contents of A and Q register.

Glossary:

- S/J = Stop/Jump word
- SS/XY =
 - SS = Section
 - X = Error type
 - Y = Error condition
- RTA = Return address
- ACT = Actual word received
- FUNCT = Function code to be performed
- EXP = Expected word
- DASTA = Data status word
- KBSTA = KYBD status word
- MEMADR = Memory address (1744) or incorrect status bits for status errors
- S-EXP = Expected S-register contents, if applicable
- S-ACT = Actual S-register contents, if applicable
- P-EXP = Expected P-register contents, if applicable
- P-ACT = Actual P-register contents, if applicable
- X-EXP = Expected X-register contents, if applicable
- X-ACT = Actual X-register contents, if applicable
- Y-EXP = Expected Y-register contents, if applicable
- Y-ACT = Actual Y-register contents, if applicable
- ID-EXP = Expected ID byte
- ID-ACT = Actual ID byte

E. SECTION DESCRIPTION INDEX

The following is an index of section descriptions:

<u>Tag Name</u>	<u>Section Name</u>	<u>Section No.</u>	<u>Page</u>	<u>Running Time</u>
CMDTST	Command Test	00	14	
BDC TST	Buffered Data	01	15	
	Channel Test			
MEMTS0	Memory Test (Stack 0)	02	16	Long-1 min. 45 sec. Short- 45 sec.
MEMTS1	Memory Test (Stack 1)	03	19	Long-1 min. 45 sec. Short -45 sec.
JMPTST	Jump Test	04	19	
PALTST	Pattern Alignment Test	05	20	
SCLTST	Scale Factor Test	06	28	
KYBTST	Keyboard Test	07	30	

IV. DESCRIPTION

A. GENERAL

1. The diagnostic test consists of 8 individually selectable test sections, designed to test the controller and its associated display console for proper operating condition. Hardware failures and malfunctions will be reported as errors using the previously described error message formats. Error message display on the console is an optional parameter selection, except for Sections 2, 3, and 4.
2. The selection of 1744 controller memory stack is determined by memory test section selected (Sections 2 and 3) as follows:

Memory Test	Testing Stack
MEMTS0 (Sec 02)	Stack 0
MEMTS1 (Sec 03)	Stack 1

The memory stacks will be tested by writing predetermined patterns in the selected stacks, reading each location and comparing its contents for correct pattern.

3. Graphic patterns will be displayed on the console for visual checking of definition and error triangles. Graphic patterns will also be used for alignments.
4. Common subroutines are provided to satisfy SMM requirements and for use by test sections as required.
5. Special features are included that provide console display of the number of the test section running, except for memory tests which are displayed on the typewriter. The word "NEXT" is displayed at the lower center of the display screen which allows the operator to select the next sequential test section previously selected to be executed.

B. SECTION DESCRIPTION

Each section except 2 and 3 will store alphanumeric macros in upper memory locations of running stack unless previously stored. The stack is selected by bit 7, testing mode parameter.

1. Test Section 00 - Command Test (CMDTST).

Commands and functions of the 1744 Controller except internal jumps, are executed in this section. Responses, storage or register contents are checked to determine if properly executed. Incorrect responses, register contents or malfunctions will result in an error being reported. The test pass frequency is determined by parameter selection for long or short (long - 10 passes; short - 5 passes). A group of clear/disable functions are performed to clear the controller, clear and disable all Interrupt flip-flops (FF), and deactivate all keyboards. Store each memory location with its own address. The capability of setting a starting address in the S register is checked by setting the S register to each value 000 to FFF and reading its contents subsequent to each setting for accurate comparison to its own value. Data transfer commands are exercised by transferring data pattern \$AAAA to the controller and reading same from controller memory, and comparing for accuracy. Numerous status inputs are done and bits checked throughout the section. Reset functions are performed to provide known X and Y values which permit X and Y registers input and comparison. Keyboard activation, interrupt FF, enabling, and start display functions are also accomplished by this section.

Any malfunction, incorrect data, or status during the performance of the above commands/functions will cause an appropriate error code to be reported.

2. Test Section 01 - Buffered Data Channel Test (BDCTST)

This section verifies the proper functioning of the I/O channels. If the Buffered Data Channel (BDC) is used, data is transferred via BDC to the 1744 Controller, and read back via BDC and compared. If an error occurs, the same data is read back via A/Q channel and compared. If this comparison is error free, a BDC input error is reported. In the event it is not error free, the data is again transferred to the 1744 via A/Q channel and read back via A/Q channel and compared. If this comparison is error free, a BDC out error is reported. However, if an error still exists, a memory malfunction error will be reported. Therefore, the memory test should be selected and executed.

When test Section 01 is selected and it is determined that the BDC is not in the system, control passes to the end of section.

3. Test Section 02 - Memory Stack 0 Test (MEMTS0)

This section exercises the 1744 Memory Stack 0, utilizing the following patterns:

- Pattern 0 - Zeros
- Pattern 1 - Ones
- Pattern 2 - Address Test
- Pattern 3 - A-5, Pattern Test
- Pattern 4 - Worst Pattern Test
- Pattern 5 - Parity Plane Test
- Pattern 6 - Operator Selectable Pattern

(Contents of Q register at last test parameter Stop 4)

The patterns will be sequentially selected and stored in the memory stack under test, the stack will be read and the contents of each cell compared for accuracy. Any unexpected variation of the patterns will be reported as an error to include the address of the failing cell in Q of Error Stop 5. The long/short test parameter selection will cause the section to be repeated 5 times for short or 15 times for long test.

- a. Pattern 0 - This pattern ensures that the stack will successfully hold zeros (\$0000) in each location. Each location is read and compared for accuracy.
- b. Pattern 1 - This pattern ensures that the stack will successfully hold ones (\$FFFF) in each location. This is verified by reading and comparing each location.
- c. Pattern 2 - This pattern determines if the stack under test will hold its own address and additionally ensures that the 1744 S register can be successfully incremented.
 - 1) Beginning with the first location of the stack each location is filled with its own address, e.g. (stack 0 = \$0000 - \$0FFF) (stack 1 = \$1000 - \$1FFF).
 - 2) Verification is assured by reading and comparing each location's contents with its address.
- d. Pattern 3 - The A-5 pattern test ensures that the stack is capable of holding a pattern of \$AAAA and \$5555 in adjacent memory locations. This is accomplished by filling the stack with alternate \$AAAA and \$5555, reading and comparing each location's contents for accuracy.
- e. Pattern 4 - This pattern determines if the memory stack will hold the worst pattern which is defined as: \$AAAA, \$0000, \$5555, \$FFFF in 64 adjacent locations and \$FFFF, \$5555, \$0000, \$AAAA in the next 64 adjacent locations, and continuing this sequence through the last location of the stack.
 - 1) The pattern is developed by filling 4 locations with \$AAAA, \$0000, \$5555, \$FFFF and repeating this pattern sequence until 64 locations are filled.
 - 2) Fill the next 4 locations with \$FFFF, \$5555, \$0000, \$AAAA and repeat this pattern sequence until 64 locations are filled.
 - 3) Repeat 1) and 2) above until the entire memory stack is filled.
 - 4) After reading and comparing each location, repeat 1) through 3) above except use the complement of indicated patterns.

- f. Pattern 5 - Parity Plane test ensures that the parity plane of the stack will hold zero and one while the rest of the plane holds the worst pattern.
- 1) Fill the stack with the complement of the worst pattern, except for plane zero which is masked to zeros. This causes worst pattern to be generated in the parity plane.
 - 2) Each location is read and compared for accuracy.
 - 3) Fill the stack with the worst pattern, except for plane zero which is masked to zeros. This causes the complement worst pattern to be generated in the parity plane.
 - 4) Repeat step 2) above.
- g. Pattern 6 - This pattern is pre-stored as \$01F8 and may be changed by the operator during parameter entry. To change the pattern the operator will enter the desired pattern in Q - register at parameter stop 4.

4. Test Section 03 - Memory Test Stack 1 (MEMTST1)

This section is identical to test Section 02, except the 1744 Memory Stack 1 will be tested.

5. Test Section 04 - Jump Test (JMPTST)

This section ensures the proper performance of the S - Jump, P - Jump, Macro Call, and Return to Main functions.

The S - Jump is checked by storing the S - Jump byte (\$1C8) followed by the Jump address, with all other locations filled with \$1F8 end of display byte. Upon executing the jump, an end of display will be detected causing the generation of a priority interrupt. Input S register and compare to determine if S register is equivalent to jump address. Execute for 11 addresses, \$0800, \$0400, \$0200, \$0100, \$0080, \$0040, \$0020, \$0010, \$0008, \$0004, \$0002.

The P - Jump, Macro Call, and Return to Main is checked by restoring macros in 1744 memory and executing macro calls to display "S - Jump, P - Jump, and M - Jump. The value of the P register will be checked for errors. Visual check should be made on display console.

The number of repetitions may be varied by the long/short parameter selection (long - 10 times; short - 5 times).

6. Test Section 5 - Pattern Alignment Test (PALTST)

This section generates and displays graphic patterns for visual scrutiny by the operator to determine display quality and correct alignment.

a. The following three graphic pattern, byte stream groups are sequentially generated in the 1700 processor and transferred to the 1744 controller memory for display on the 274 console:

1) 5 Dot Pattern

2) D/A Bit Switching Pattern

3) Composite Graphics Pattern (boxes, circles, crosses, diagonals, alphanumerics, intensity variations, blinking, and non-blinking functions)

b. The patterns are displayed sequentially as listed above. However, the operator may terminate a pattern and cause the next sequential pattern to be displayed by depressing the light pen switch. To extend the period of pattern display, the repeat section (bit 5) of the Stop/Jump parameter should be set.

c. Pattern Description

1) The 5 - Dot Pattern (Figure 1) consists of 5 small dots displayed. A hardware adjustment has been made on most 1744 digigraphics systems to cause the outer dots to be just visible. This adjustment causes graphic dimensions on the console to be slightly less than the binary equivalence. For example, binary representation of a 14 inch line is graphically displayed as approximately 13 inches. This adjustment was made to satisfy the standard software package design.

CAUTION

If only the center dot is visible, determine whether the hardware has been adjusted to display inch for inch; if so, visibility of the center dot only is correct.

2) D/A Switching Pattern (Figure 2) is a diagonal line from lower left to upper right with X and Y bit switching markers beside the line. The line adjacent to the markers should be straight. A marked variation appearing on the line opposite the markers indicates maladjustment of the associated D/A amplifier. To correct this condition, adjust D/A amplifiers until the line adjacent to the markers is straight.

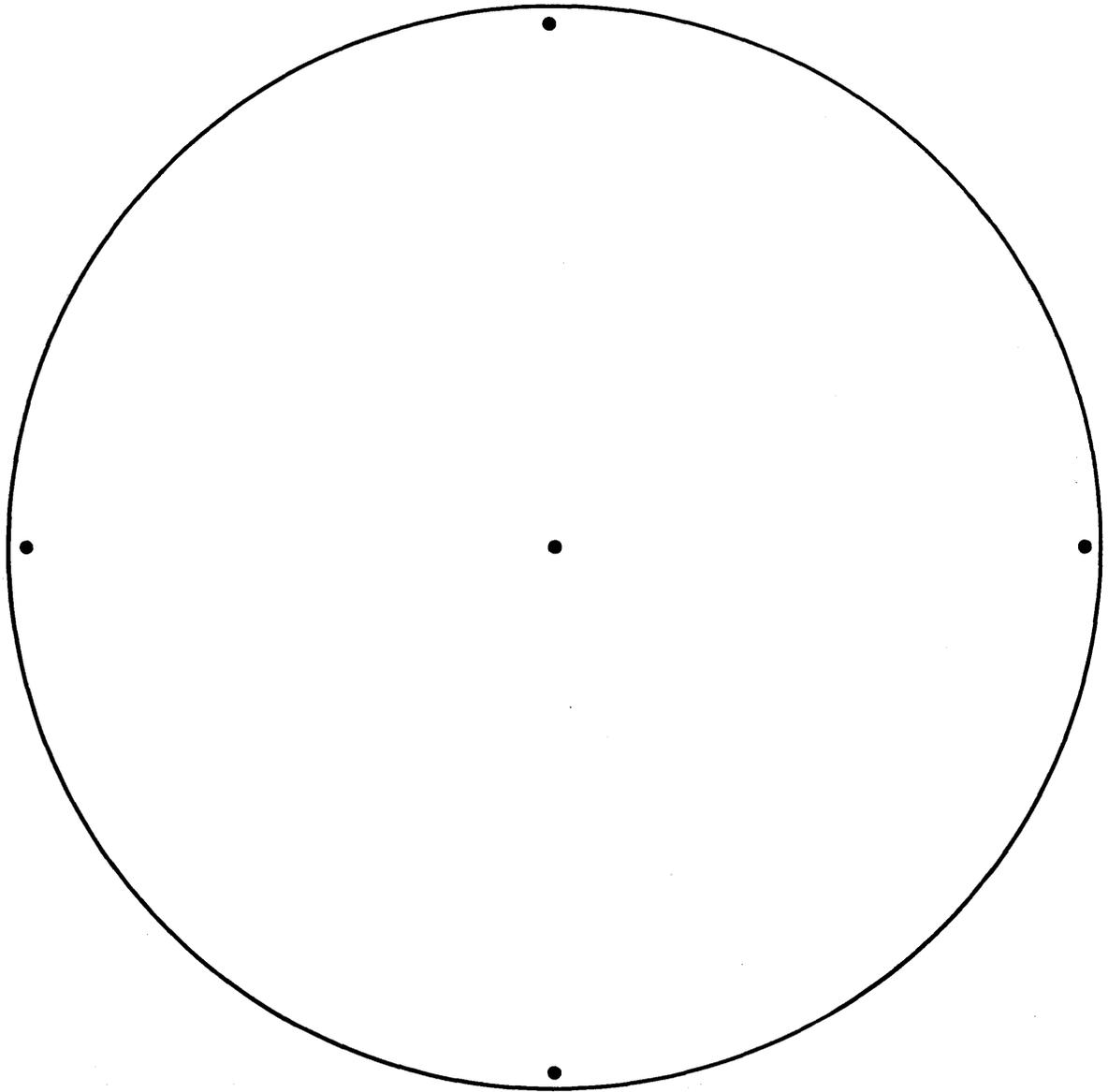


Figure 1. 5 Dot Pattern

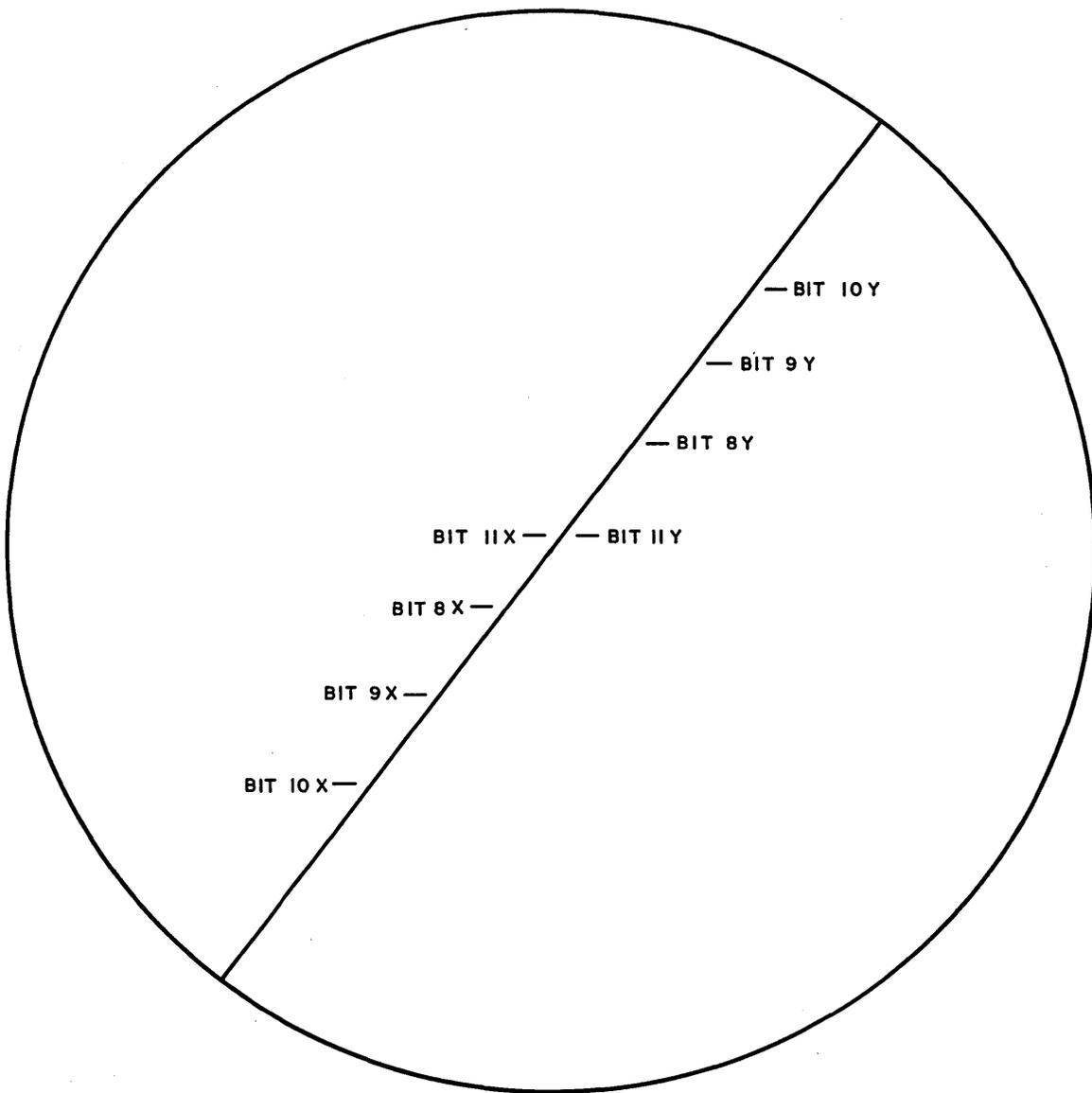


Figure 2. D/A Switching Pattern

3) The Composite Graphics Pattern (Figure 3) consists of three square boxes (14 x 14, 12 x 12 and 7 x 7 inches), four circles 1/2 inch diameter, four circles 2-1/2 inches diameter, two diagonal lines intersecting at the center and with the corners of the two inner boxes and terminating at the four corners of the 14 inch box, two perpendicular lines terminating at the edges of the 14 inch box and forming four right angles at the center, intensity, blinking and nonblinking functions indicated in upper half of pattern, and with alphanumeric characters on both sides. Some incorrect patterns are shown in Figure 4 which indicates malalignment.

7. Test Section 6 - Scale Factor Test (SCLTST)

This test section ensures that each scale factor (2 - 7) will provide the proper unit variation (Figure 5). A horizontal line will be drawn for each scale factor using the same number of incremental byte of equal value. A visual examination should determine if correct variation is attained.

8. Test Section 7 - Keyboard Test (KYBTST)

This test section consists of two subsection described below, each of which requires operator intervention to be effectively completed. The subsections desired must be selected in the test parameter by setting bit 4 for VFKB or bit 5 for AN/KB, or both for dual keyboard configuration. The section, however, will exit after a time out period in the event no further action is taken by the operator.

a. Alphanumeric Keyboard Subsection

The subsection displays as follows:

"HIT RANDOM KEY"

At this time the operator activates a key at random, causing the corresponding character to be displayed. This character should be visually checked against the selected key for match. Continue in this manner until all 64 ASCII subset characters are checked. Upon completion of this subsection, it advances to the variable function keyboard subsection after time out period. If variable function keyboard is not in the system, it advances to the end of section.

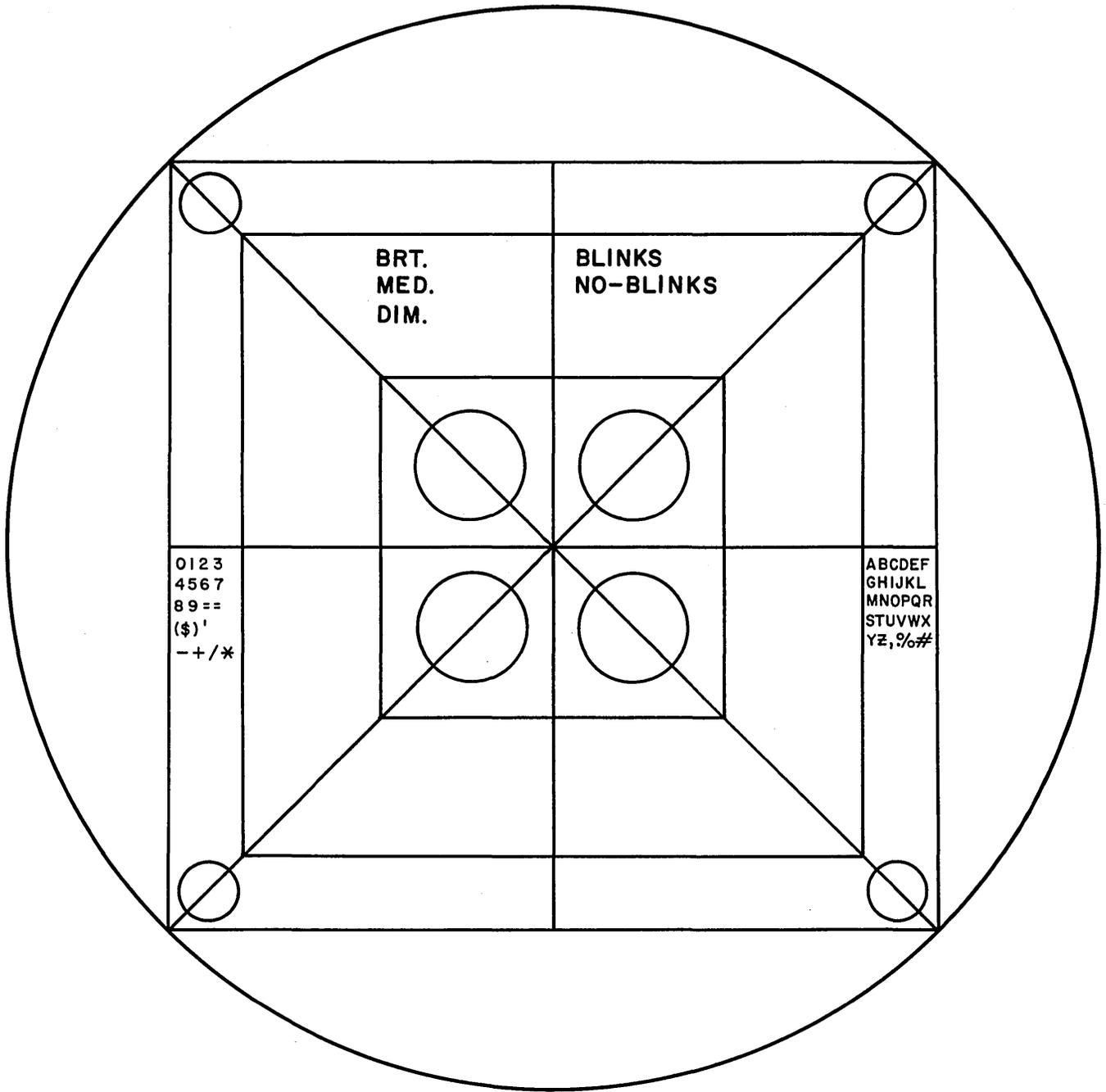


Figure 3. Composite Graphics Pattern

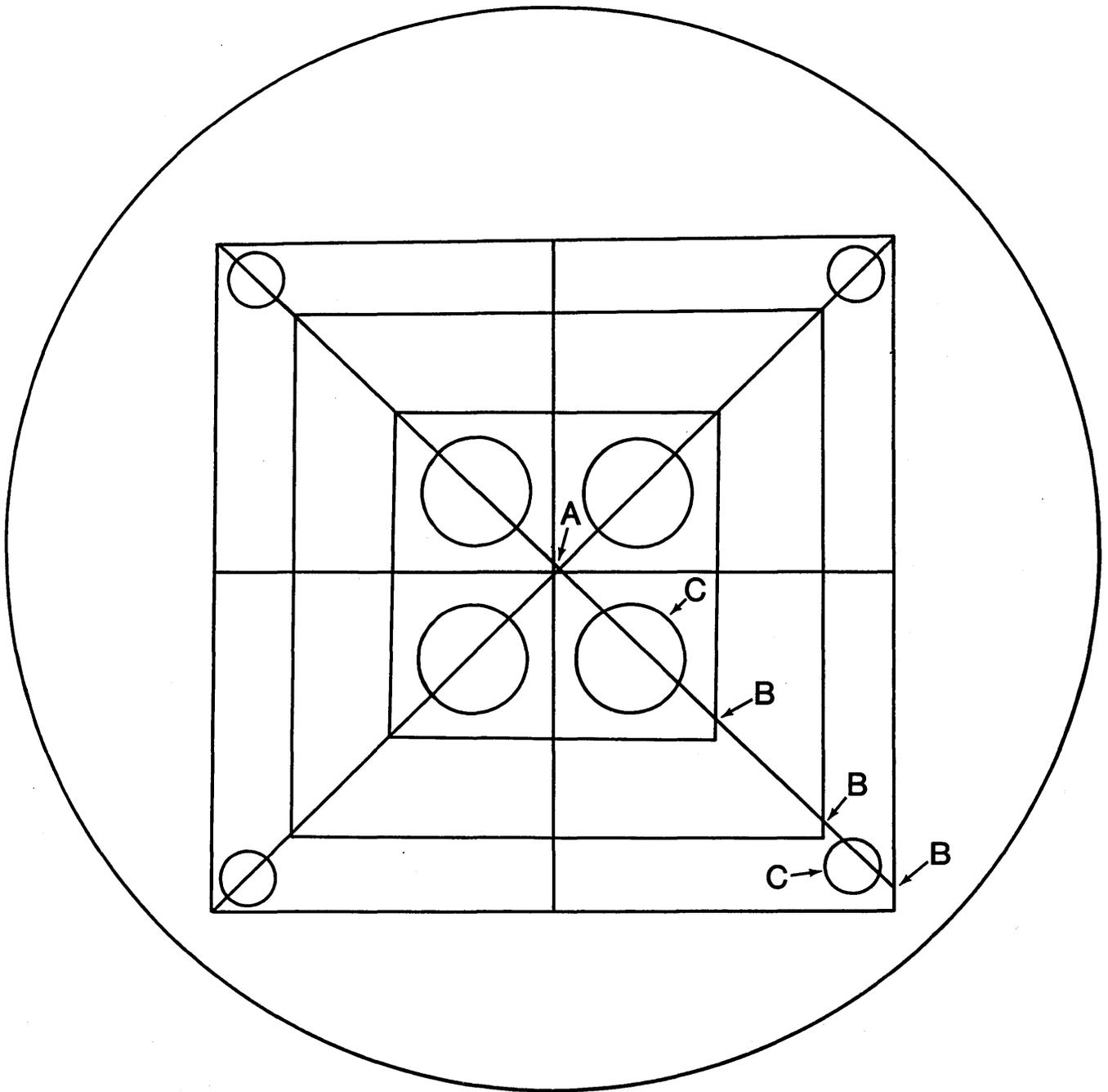


Figure 4. Malaligned Composite Pattern

- A. Error Triangle
- B. Diagonal not through Corner
- C. Diagonal not through Center of Circles

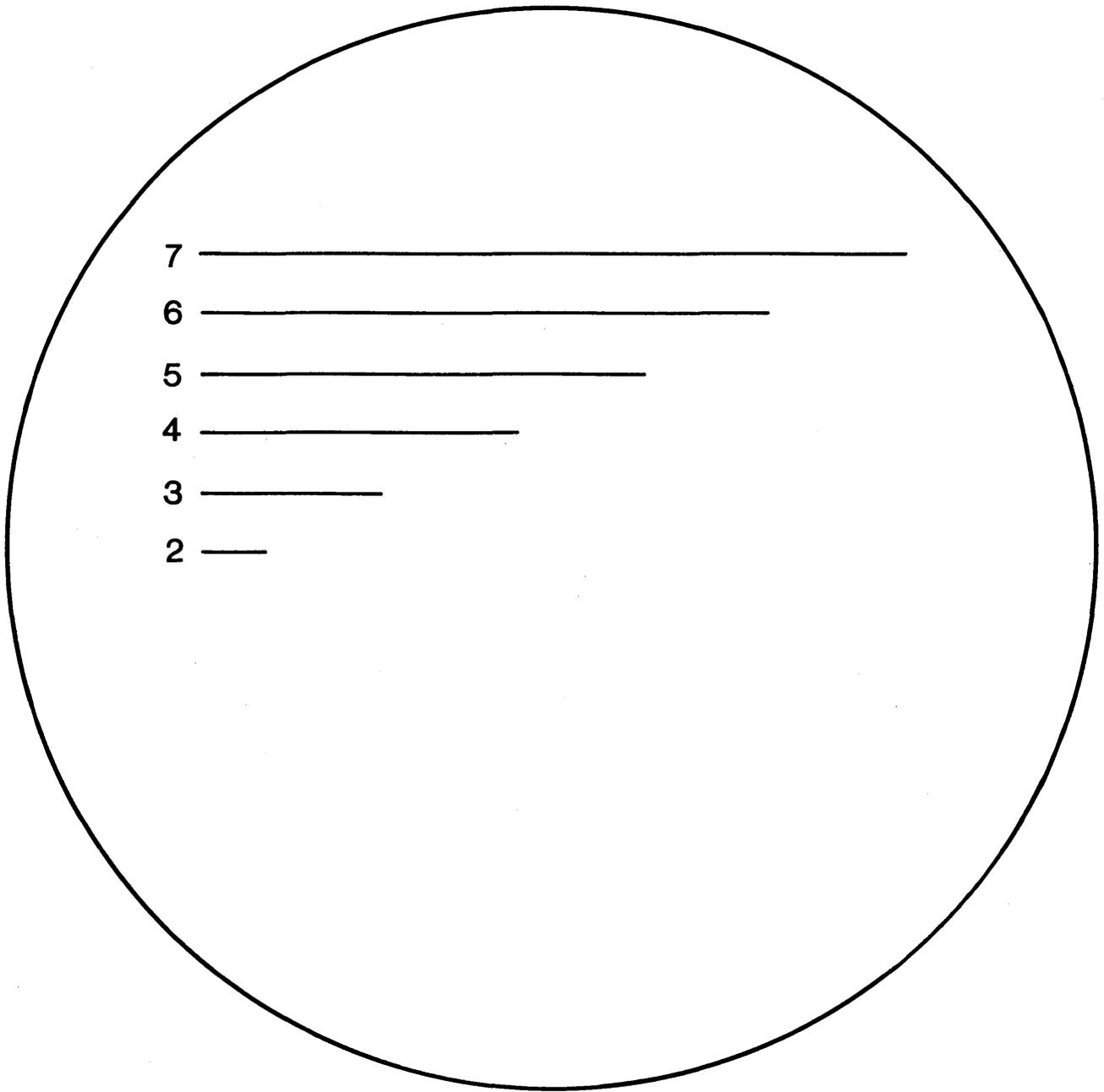


Figure 5. Scale Factor Pattern

b. Variable Function Keyboard Subsection

The keyboard activation is accomplished by the section. After keyboard is activated, the keyboard interrupt is enabled which allows the operator to randomly select one or more keys.

Upon key selection, depress the Accept key (keyboard interrupt is generated) which will cause the keyboard pattern (Figure 6) to be displayed with a blinking "X" appearing in the corresponding key position, including the Activate key. All keys other than the Accept and Reject keys are latching type and will remain activated until released. The release of latching keys followed by depressing the Accept/Reject key will cause the removal of the blinking "X" in the next pattern display for all released keys. Non-selection by operator will cause exit to next section after time out.

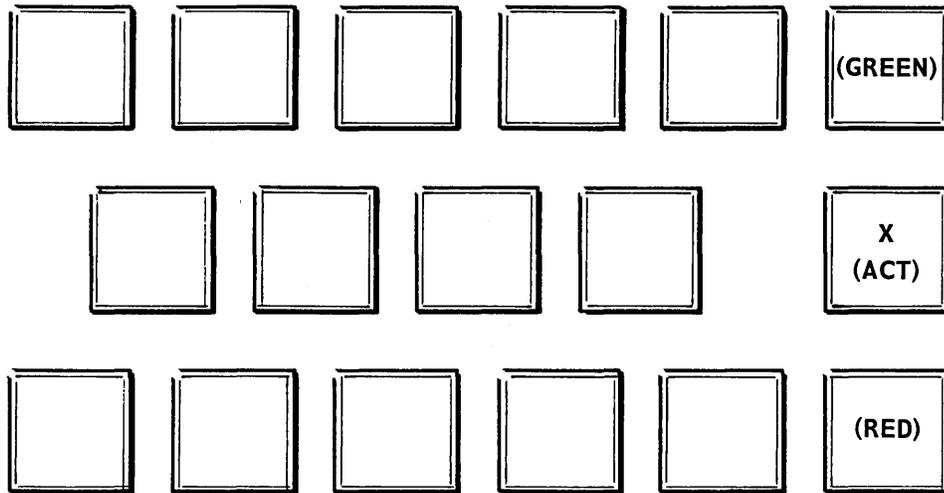


Figure 6. Variable Function Keyboard Display Pattern
(blinking "X" indicates keys activated)

APPENDIX A

I. MAINTENANCE ROUTINES

A. 1744 DIGIGRAPHIC CONTROLLER MEMORY DUMP

This routine reads the contents of the 1744 Memory Stack (2048) and stores it in the buffer area. It also passes control to the line printer or teletypewriter dump routine for printout.

1. Call - Set P register to IA + \$10,

Set A register bit 15 = 1, for teletypewriter, or bit 15 = 0 for line printer output. Set bit 12 = 0 for stack 0 or bit 12 = 1 for stack 1.

Set Q register to \$0 for memory location 0-2047, or set Q register to \$800 for memory locations 2048-4096.

2. Execute - RUN/STEP Switch to Run

To dump the complete stack 0 two runs must be made, one for each Q register setting. To dump the complete stack 1 (same as above) with bit 12 of A register set.

B. TELETYPEWRITER DUMP

This routine prints the contents of the computer memory on the teletypewriter from the address specified in the A register to the address specified in the Q register.

1. Call - Set P register to IA + 9.

Set A register to FWA.

Set Q register to RUN.

2. Execute - RUN/STEP Switch to Run.

C. LINE PRINTER DUMP

This maintenance routine prints the computer memory contents specified by A and Q registers on the line printer.

1. Call - Set P register to IA + \$E.

Set A register to FWA.

Set Q register to LWA.

2. Execute - RUN/STEP Switch to Run.

II. ERROR CODES

Error Code is prefixed with section number (XX) when displayed.

<u>Code</u>	<u>Definition</u>
XX01	Ext. Reject - Status Input (BDC)
XX02	Int. Reject - Status Input (BDC)
XX04	Ext. Reject - Data Input (BDC)
XX05	Int. Reject - Data Input (BDC)
XX0A	Un-Terminated BFR Transfer
XX0B	Ext. Reject - BDC Function
XX0C	Int. Reject - BDC Function
XX0D	Input Failure (BDC)
XX10	Input Data Error (BDC)
XX11	Output Failure (BDC)
XX12	Probable Memory Failure (Suggest running memory test)
XX14	Ext. Reject - Data Output (BDC)
XX15	Int. Reject - Data Output (BDC)
XX20	Ext. Reject - Controller Status Input (1744)
XX21	Int. Reject - Controller Status Input (1744)
XX22	Ext. Reject - Direct Data Input
XX23	Int. Reject - Direct Data Input
XX24	Ext. Reject - S Register Input
XX25	Int. Reject - S Register Input
XX26	Ext. Reject - P Register Input
XX27	Int. Reject - P Register Input
XX28	Ext. Reject - X Register Input
XX29	Int. Reject - X Register Input
XX2A	Ext. Reject - Y Register Input
XX2B	Int. Reject - Y Register Input
XX2C	Ext. Reject - ID Byte Input
XX2D	Int. Reject - ID Byte Input
XX2E	Ext. Reject - Keyboard Status Input
XX2F	Int. Reject - Keyboard Status Input
XX30	Ext. Reject - 1744 Function Output
XX31	Int. Reject - 1744 Function Output
XX32	Ext. Reject - Direct Data Output
XX33	Int. Reject - Direct Data Output

<u>Code</u>	<u>Definition</u>
XX34	Ext. Reject - S Register Output (ADDR)
XX35	Int. Reject - S Register Output (ADDR)
XX36	Ext. Reject - Terminate Computer Display
XX37	Int. Reject - Terminate Computer Display
XX38	Ext. Reject - Computer Display
XX39	Int. Reject - Computer Display
XX3A	Ext. Reject - Keyboard Function Output
XX3B	Int. Reject - Keyboard Function Output
XX40	Unexpected Status
XX41	Console Power Off
XX42	KB Interrupt FF Did Not Enable
XX50	VFKB Did Not Activate
XX51	VFKB Failed to De-activate
XX52	AN/KB Did Not Activate
XX53	AN/KB Failed to De-activate
XX70	Controller Status Data Incorrect
XX71	Input Data Command Failed
XX72	S Register Input Failed
XX73	P Register Input Failed
XX74	X Register Input Failed
XX75	Y Register Input Failed
XX76	Search ID Byte Failed
XX77	Keyboard Status Input Failed
XX78	Reject on Clear Controller Function
XX79	Output Data Command Failed
XX7A	S - Register Output Failed
XX80	Memory Location - Wrong Address/Bad Compare
XX81	Memory Error - Incorrect Compare
XX83	Parity Plane Test - Storage Error
XX90	S Register Content Error
XX91	P Register Content Error
XX92	X Register Content Error
XX93	Y Register Content Error
XXB1	Int. Reject - Status Input (Interrupt processor)
XXB2	Ext. Reject - Status Input (Interrupt processor)
XXB3	Int. Reject - Keyboard Status Input (Interrupt processor)
XXB4	Ext. Reject - Keyboard Status Input (Interrupt processor)

<u>Code</u>	<u>Definition</u>
XXB5	Int. Reject - Clear Interrupt
XXB6	Ext. Reject - Clear Interrupt
XXB7	Int. Reject - Clear KB Interrupt
XXB8	Ext. Reject - Clear KB Interrupt
XXB9	Interrupt Failed to Clear
XXBA	Int. Reject - Status Input (after clear interrupt)
XXBB	Ext. Reject - Status Input (after clear interrupt)
XXBC	Unexpected Interrupt
XXBE	PRI Int. Failed to Occur
XXBF	PRI Int. FF Failed to Enable

VALIDATA KEY ENTRY STATION TEST
(KEY 060 Test No. 60)

I INTRODUCTION

This diagnostic will test the validata unique components.

II REQUIREMENTS

A. HARDWARE TESTED

970-8	Key Entry Station Controller
970-8	Key Entry Distribution Unit
970-32	Key Entry Station (CRMT)
970-380	Key Entry Station (CRVT)

B. SOFTWARE

This diagnostic is designed to operate under control of the SMM17 Monitor.

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The diagnostic is loaded using the standard SMM17 monitor test loading procedure.

NOTE

The equipment code used must be the address of the controller supplying the interrupt.

B. PARAMETERS

The diagnostic is set to run with a prestored set of parameters. No parameter changes are required if the prestored list of parameters are valid for the stations to be tested. To alter the prestored parameters, follow the directions stated in SMM17 Reference Manual.

The parameter stops are as follows:

First stop (overflow light on)

(A) = 6031 - test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Sections to run (prestored as 0027)

(Q) = Interrupt line - interrupt line 7 = bit 7, etc. (prestored as 0100)

Third stop

(A) = Number of controllers to be tested (prestored as 0001) (maximum of 8)

(Q) = Not used

The number of remaining stops is dependent on the number of controllers to be tested. The format of the remaining stops is as follows:

(A) Bits 8 through 15 = stations to be tested, where:
 Bit 8 = Station 0, etc.

(A) Bits 0 through 7 = stations containing 480 character terminals.

Example: If station 5 is a 480 character terminal, set bit 5 in the A register.

(Q) = Equipment code of the controller to be tested.

The previous stop will continue until all controllers have been entered.

C. SECTION DESCRIPTION INDEX

Section 0	Controller Test
Section 1	Output Worst Pattern
Section 2	Output All Characters
Section 3	Input from Keyboard and Display
Section 4	Input from One Station Output to Another
Section 5	Plasma Matrix Check

IV OPERATION COMMUNICATION

A. MESSAGE FORMATS

1. Error Messages

All error message displays use the standard SMM17 error message format:

A	Q	A	Q	AQ.....AQ
60X8	Stop/Jump Parameter	Section/ Error	Return Address	(See Individual Error Message)

B. MESSAGE DICTIONARY

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Message</u>
Entry Error		
01	PARENT	Parameter entry error, retry A3 = Sections Q3 = Interrupt line A4 = Stations to test Q4 = Stations containing 480 character displays

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Message</u>
Reject Error		
02	INTPRO IO	Internal reject on input A3 = A register contents Q3 = Q register contents A4 = Address of calling program Q4 = Not used
Reject Error		
03	INTPRO IO	External reject on input A3 = A register contents Q3 = Q register contents A4 = Address of calling program Q4 = Retry count
Reject Error		
04	INTPRO IO	Internal reject on output Same as 02
Reject Error		
05	INTPRO IO	External reject on output Same as 03
Status Error		
06	SEC0	Status error A3 = Actual status Q3 = Expected status
Status Error		
07	SEC0	Clock status did not clear when clear controller was executed
Data Error		
08	INPCHK	Input word not equal to expected word A3 = Actual data Q3 = Expected data A4 = Not used Q4 = Equipment number
Parity Error		
09	IO	Parity error A3 = Input word Q3 = Equipment Address A4 = Line address Q4 = Character address

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Message</u>
Character Lost		
0A	IO	Character lost A3 = Input word Q3 = Equipment address A4 = Line address Q4 = Character address
Break		
0B	IO	Break condition detected A3 = Input word Q3 = Equipment address A4 = Line address Q4 = Character address
Status Error		
0C	INTPRO	Interrupt received, clock status not set
Status Error		
0D	INTPRO	Clock status did not clear with clear interrupt
False Interrupt		
0E	INTPRO	Clock interrupt occurred when disabled
Time Out		
0F	SEC0	Controller time out. No clock status
Status Error		
10	IO	No character request status
	SEC2	A3 = Input word Q3 = Equipment address

V DESCRIPTIONS

A. GENERAL

The diagnostic performs various tests on the Validata Key Entry Controller and Stations. The test sections to be run are selected via the parameter entry routine. Common subroutines include: parameter entry, section select, end of test, repeat test, repeat section, repeat conditions, error reporting, interrupt processing, and the input/output driver.

B. SECTION DESCRIPTIONS

1. Section 0 - Controller Test

This section checks the operation, status, and functions of the controller.

Controller status is read and the protect status is checked. A message is printed on console teletype and all selected stations if protected.

The clock status is then checked. If it is not set, program waits 20 milliseconds for clock status to set. If clock does set in the prescribed time, ERROR "F" is generated. When clock status is detected, a clear controller is attempted (no rejects expected). ERROR "7" is generated if clock status does not clear when clear controller is attempted. ERROR "6" is generated if any status other than protected or clock is received.

2. Section 1 - Output Worst Pattern

This section outputs the U*U* pattern as a worst condition test. The operator must observe the pattern displayed to determine proper operation. One page is sent to all selected stations using character positioning. A 480-character buffer is built at INIT. The clear command is issued to all selected stations and the I/O driver is scheduled.

Re-entry is performed after completion of buffer and repeat section is tested.

3. Section 2 - Output All Characters

This section will transmit the alphanumeric repertoire. The first page is written using character positioning. The second page uses the self sequencing mode of operation. On 480 character type displays the second page is in the inverse video mode and uses the erase line feature to clear the screen upon completion. It will be necessary for the operator to monitor the display to determine proper operation. Repeat conditions are checked between pages.

A 480 character buffer is built at INIT. The clear command is issued to all selected stations and the I/O driver is scheduled. Upon completion, start inverse video command is issued to all selected 480 type stations. The character buffer is then transmitted using the self sequencing mode. End inverse video commands are issued to all 480 type stations, and erase line functions are performed bottom to top.

4. Section 3 - Input from Keyboard and Display

This section requires the operator to exercise the keyboard. Characters received will be returned and displayed. The operator must determine proper operation. Operating the "INT" key will terminate the section.

The "Input" message buffer is scheduled for the I/O driver. Upon completion, the input word table is monitored for data received. When data is received it is checked to determine code type. The alphanumeric repertoire is saved in a single character buffer. Special key codes will generate the appropriate message

buffer. The "INT" key will terminate the section. All buffers, when generated, will schedule the I/O driver.

5. Section 4 - Input from One Station Output to Another

This section receives data from any station and will display the data on any other station. The first two characters received will determine the station to which the data will be sent. Operating the "INT" key will terminate this section.

The message "THIS IS XX OUTPUT TO" is scheduled for the I/O driver. Upon completion, the input word table is monitored for data received. The first two characters received will be saved in the routing table which will be used as the destination station for data received from this station. When data is received it is checked to determine code type (same as Section 3). The "INT" key will terminate the section. All buffers, when generated, will schedule the I/O driver.

6. Section 5 - Plasma Matrix Check

This section will print characters which will use all matrix positions of the plasma display. One page each of the characters H, I, and number sign will be printed. Each page is terminated by the "INT" key.

A 480-character buffer is built at INIT. The clear command is issued to every selected station. The I/O driver is scheduled with the first page. When the "INT" character is received the next page is scheduled until the three pages are complete. Repeat condition is checked after each page.

C. SUBPROGRAM DESCRIPTION

The subprograms used by this diagnostic, with the exception of the I/O driver, are used primarily for interface to SMM17.

1. PARENT

The parameter entry routine allows the operator to select the tests which are applicable to his system and situation. Failure to select at least one section, an interrupt line, and at least one controller will result in error code 1 being reported. After the error is reported, the routine will initialize and return for a retry.

2. SECSEL

The section select routine will transfer control to the selected sections, one at a time, until all sections have been completed. After completion of all sections, control is given to the end test routine.

3. ENDTES

The end of test routine will check the stop at end of test parameter. If bit 2 of the Stop/Jump word is set, a stop will occur in accordance with SMM17 requirements. After the stop, bit 6 will be tested to determine if repeat test is desired.

4. REPTES

The repeat test routine will reinitialize the section select routine and check the Stop/Jump word for re-enter parameters (bit 10) and stop to enter parameters (bit 0). If both set a parameter stop will occur.

5. REPSEC

The repeat section routine will stop at the end of a section if bit 1 of the Stop/Jump word is set. If not set, control is given to the next section via the section select routine.

6. REPCON

The repeat conditions routine will check bit 4 of Stop/Jump word. If set, the previous conditions will be repeated.

7. ERRRPT

The error reporting routine reports all errors detected by the diagnostic. Errors are reported in accordance with SMM17 procedures. This routine also contains the error data table (ERRDAT).

8. INTPRO

The interrupt processor will read and save controller status. The clock enable flag is checked, and ERROR E is reported if clock was not enabled when the interrupt occurred. The I/O driver is entered via the return address (IA+5). The exit from this routine will be to the exit interrupt handler located in SUMMIT.

9. IO

The input/output driver is completely interrupt driven and performs all data transfers in the character positioning mode. This routine is scheduled by the various sections via the enable interrupt routine and is entered when the interrupt is received by the interrupt processor (INTPRO).

The driver reads station status from all selected stations. The status word is saved in the status word table, and character ready status is checked. If character ready is set, parity error, character lost, and break status is examined. These errors are then reported, if present, as ERROR 9, ERROR A, and ERROR B respectively. The output word table is checked for activity. If the

output buffer is active, the driver will send the line address from LAD, the character address from CAD, and one word from the data buffer. The line address, character, and buffer addresses are updated. First word and last word addresses are compared. If addresses are equal, OUTWD is cleared (not active). Exit is accomplished by enabling interrupts and returning to the monitor.

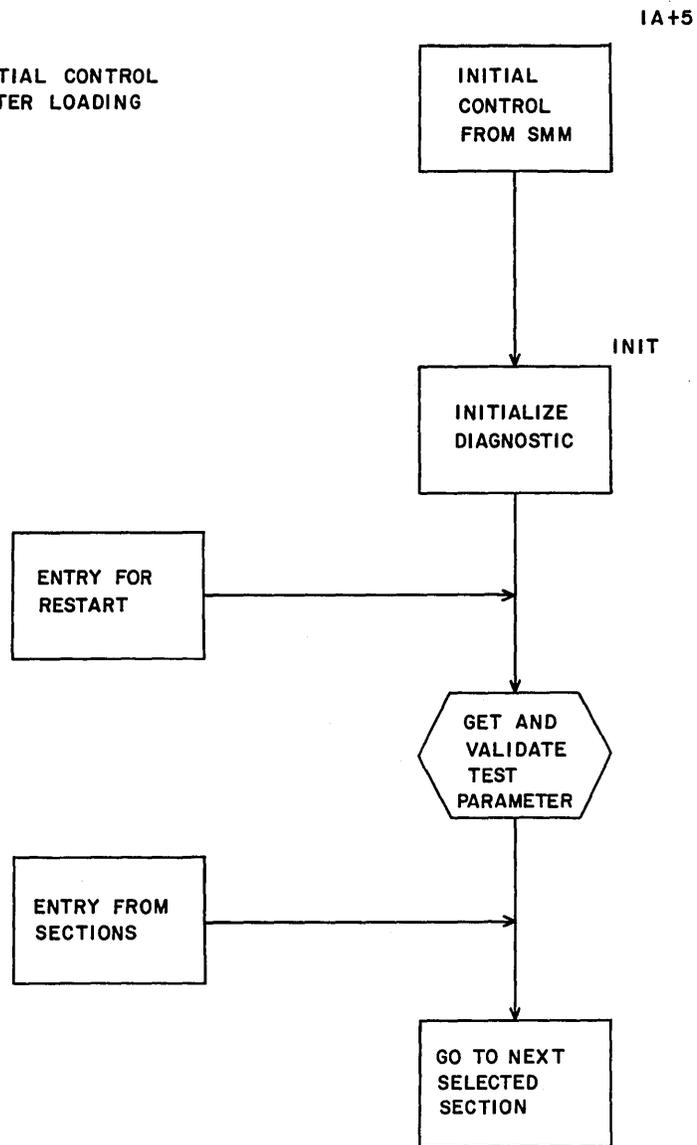
VI APPLICATIONS

A. HUNG CONDITIONS

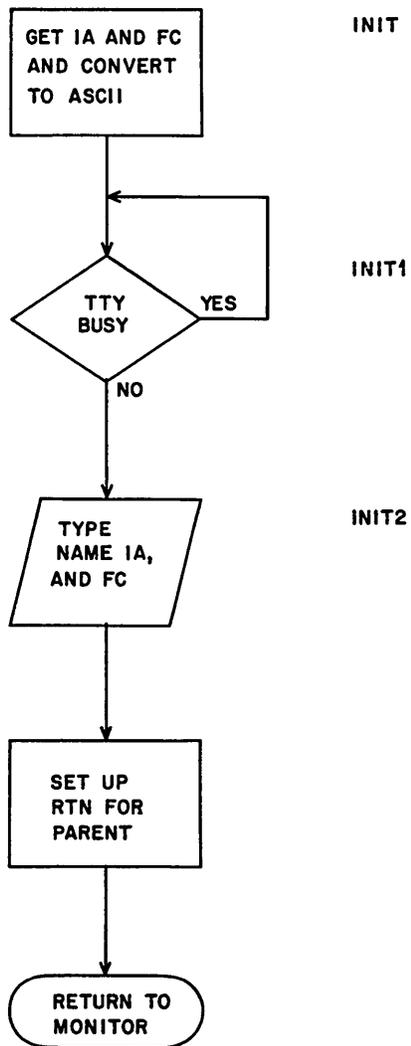
This diagnostic is entirely interrupt driven, therefore, interrupt failure will cause a hung condition waiting for I/O to complete.

Failure of the character ready status to clear will cause a hung condition at program tag DUMIN. A dummy input is performed to clear character ready status. If this status does not clear, the diagnostic continues to try.

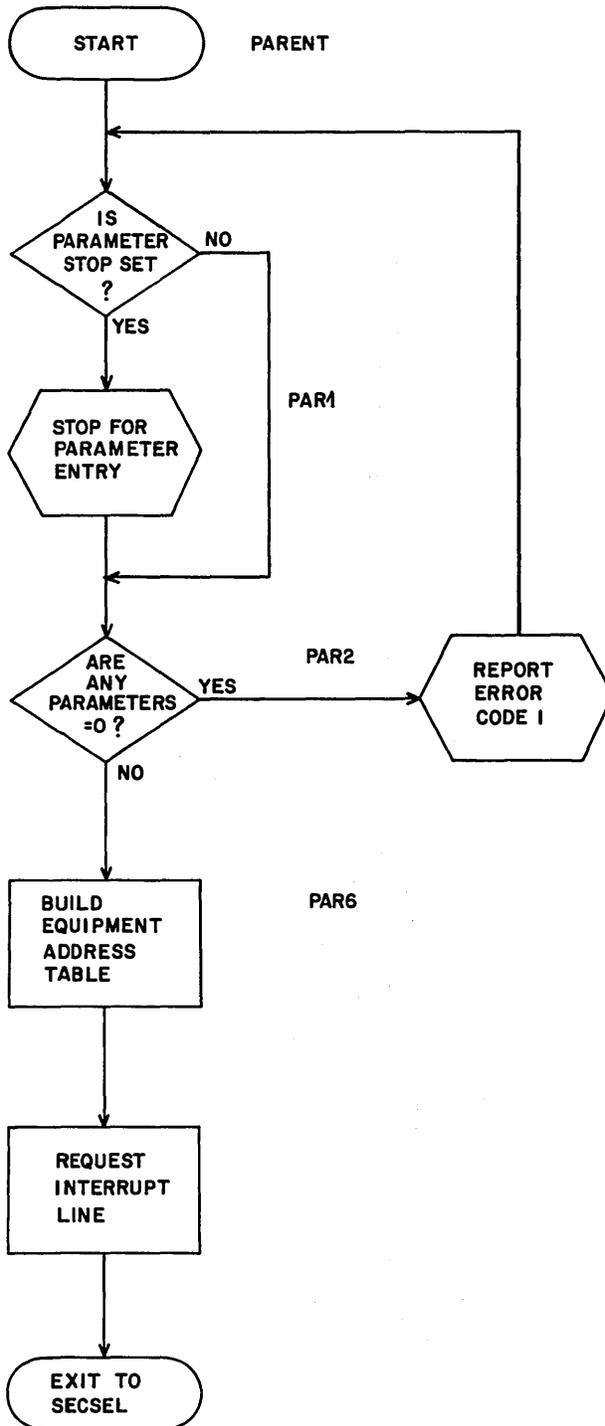
INITIAL CONTROL
AFTER LOADING



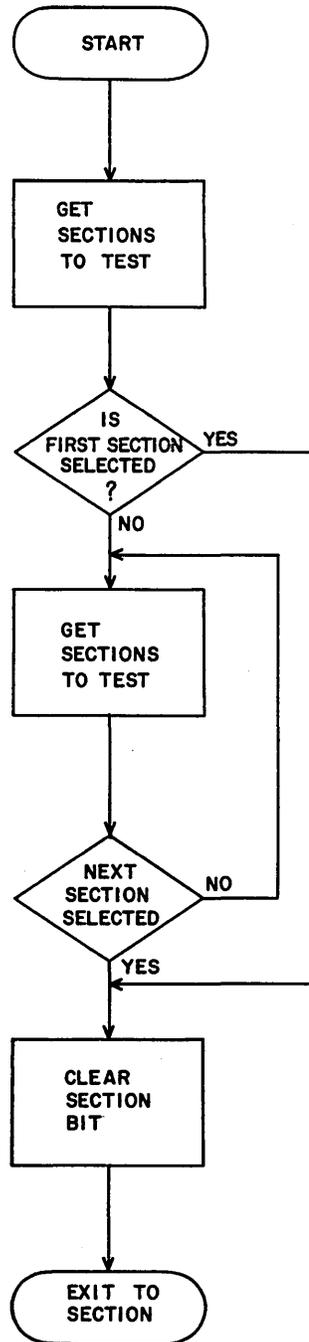
INITIALIZE ROUTINE (INIT)



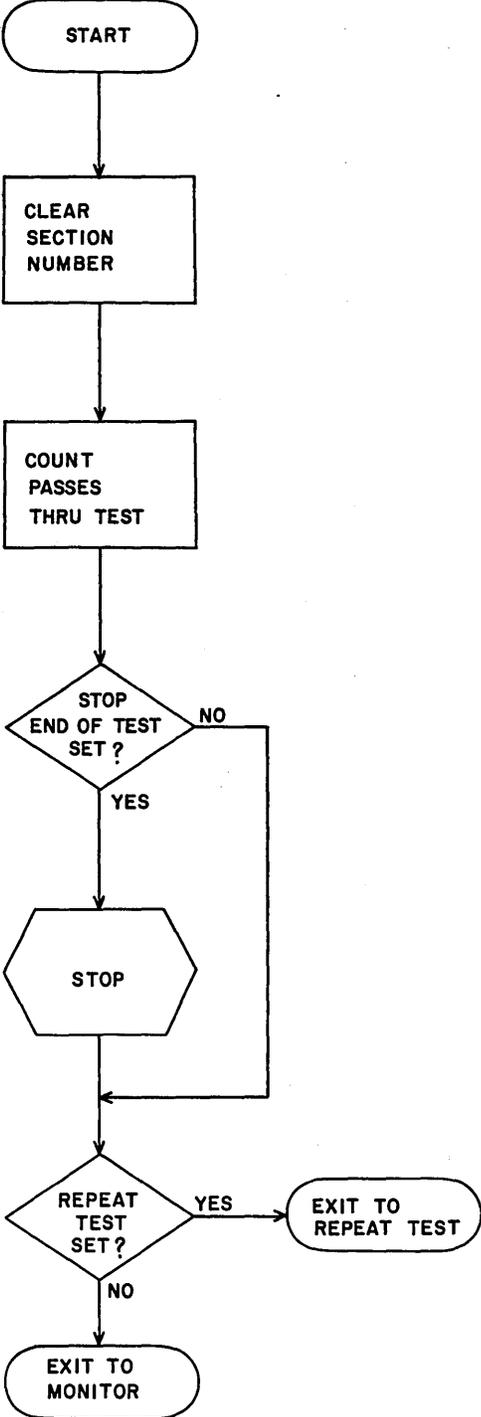
PARAMETER ENTRY ROUTINE (PARENT)



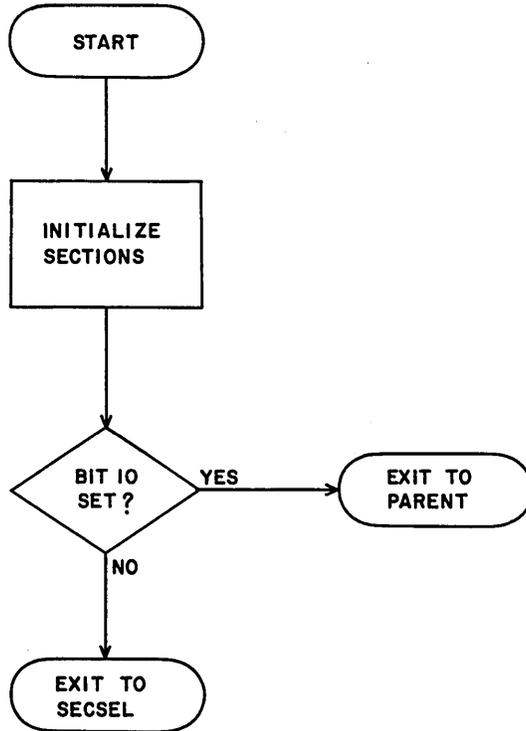
SECTION SELECT ROUTINE (SECSEL)



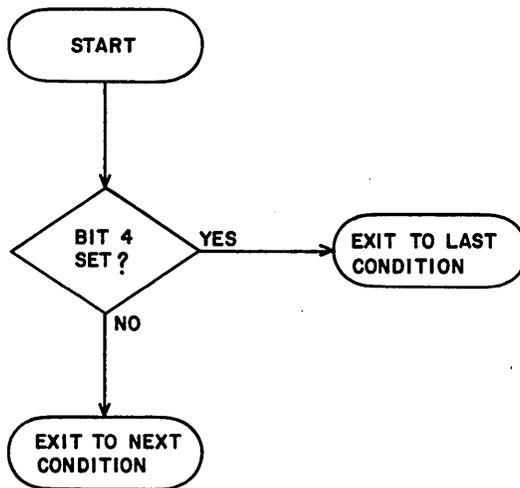
END OF TEST ROUTINE (ENDTES)



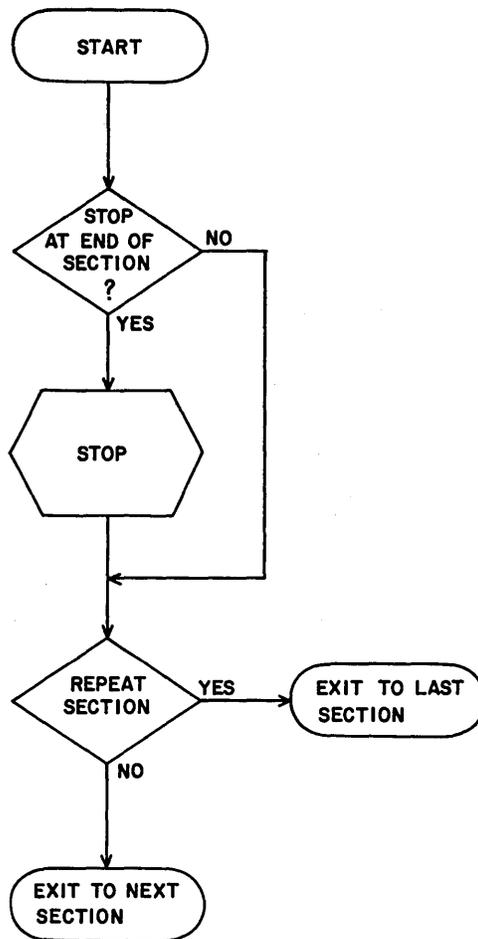
REPEAT TEST ROUTINE (REPTES)



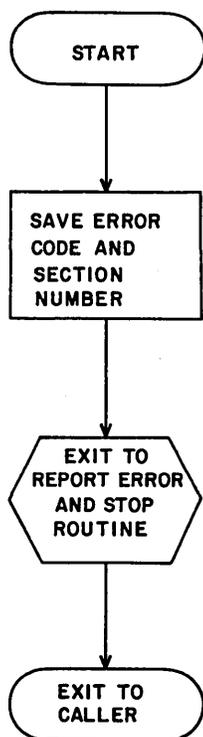
REPEAT CONDITIONS ROUTINE (REPCON)



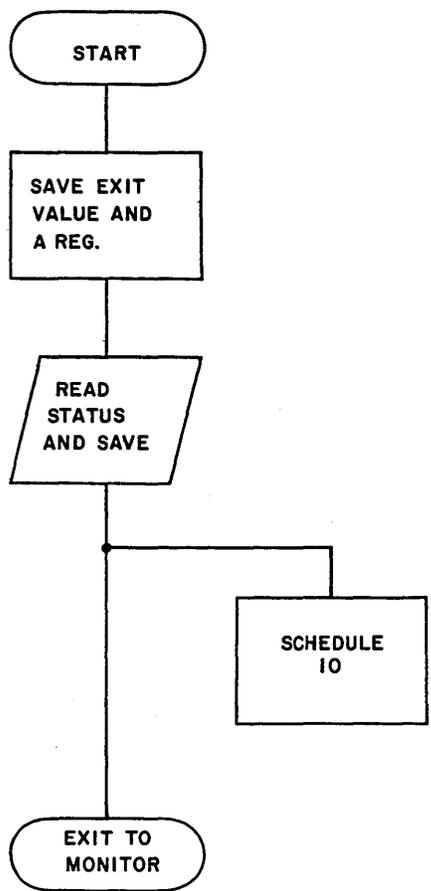
REPEAT SECTIONS ROUTINE (REPSEC)



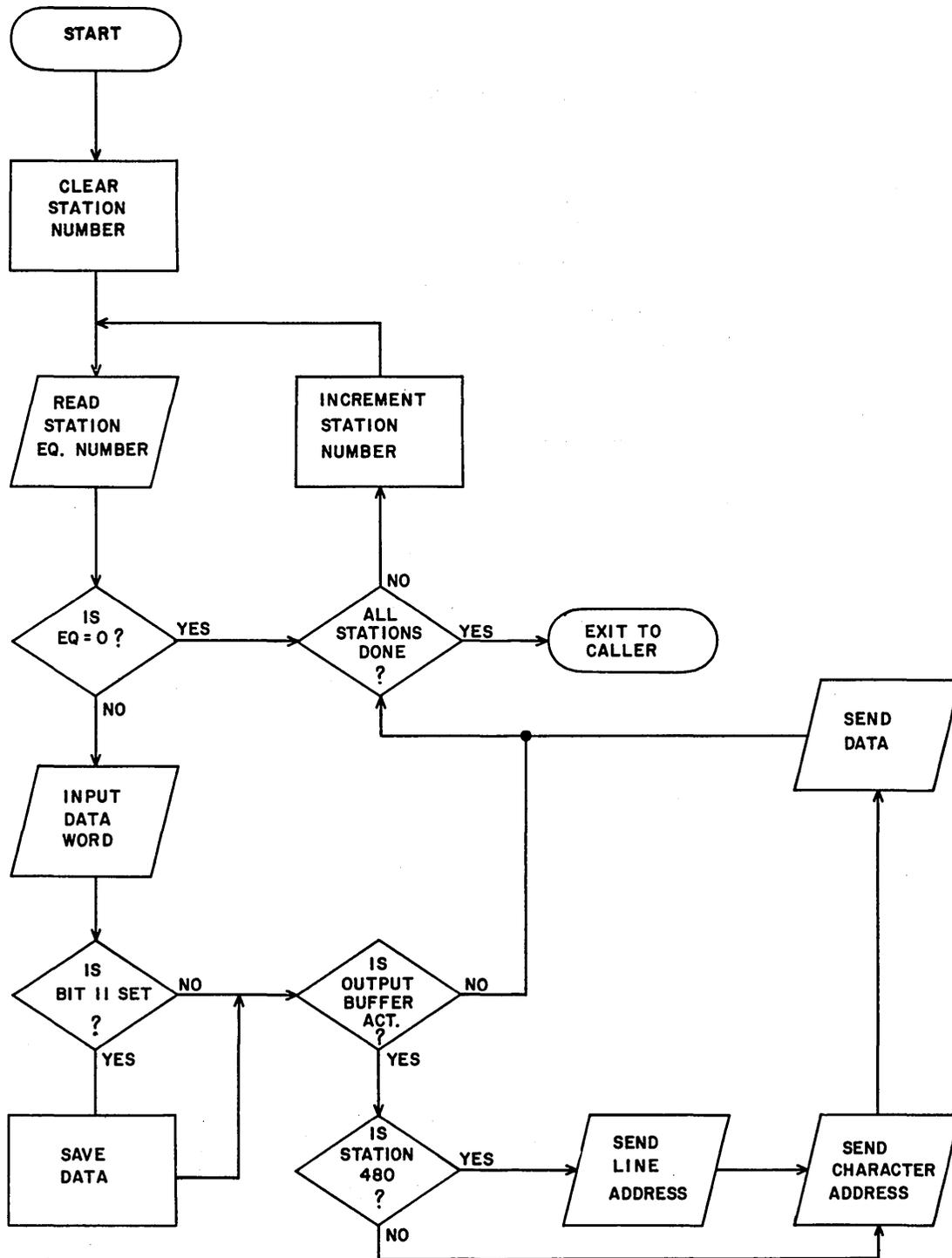
ERROR REPORTING ROUTINE (ERRRPT)



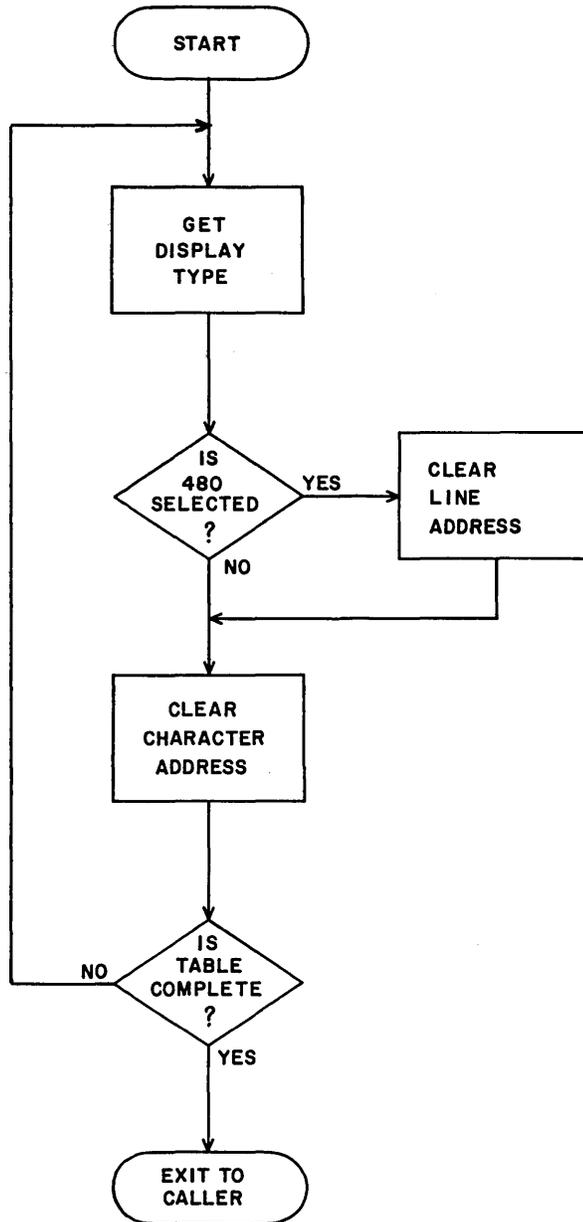
INTERRUPT PROCESSOR (INTPRO)



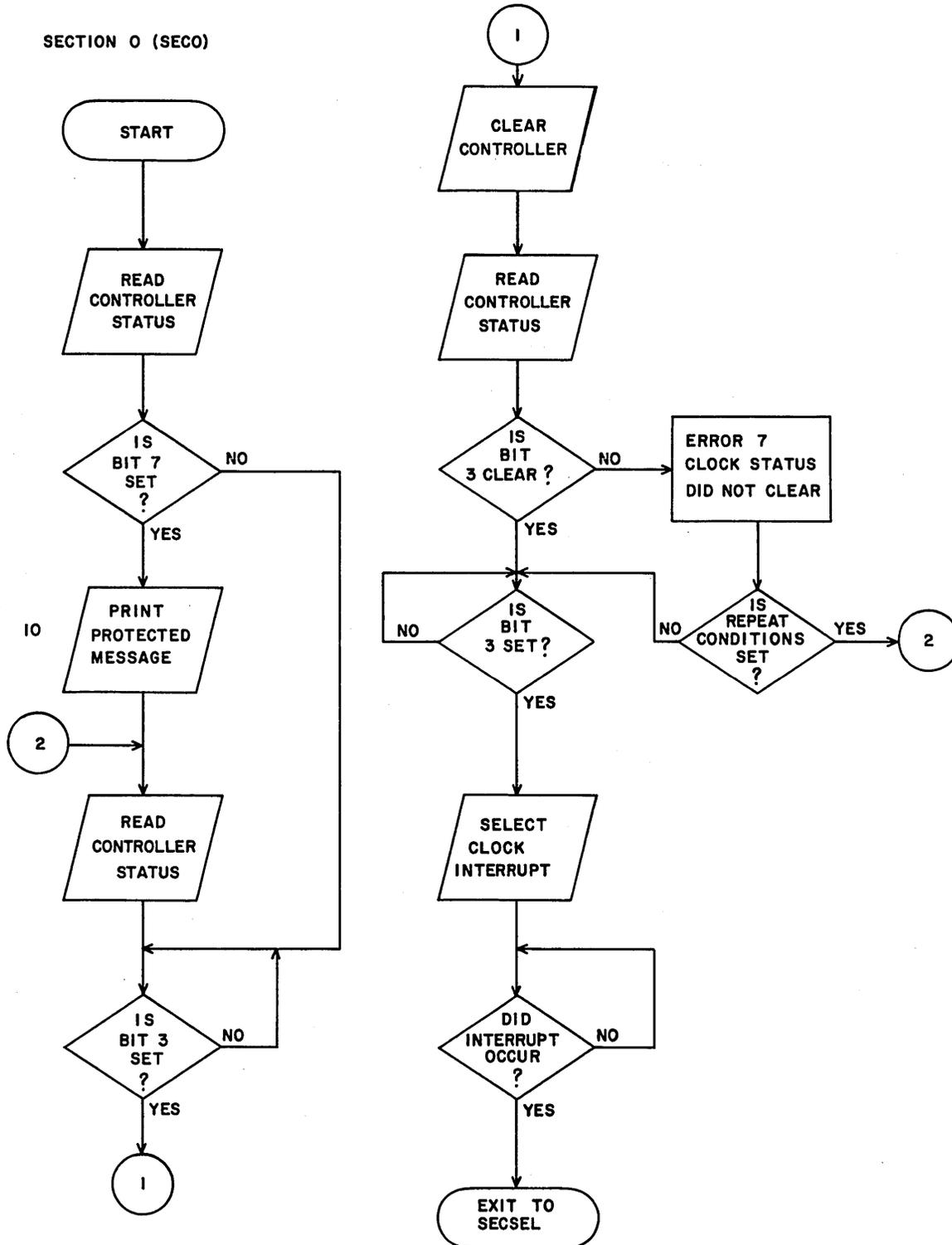
INPUT/OUTPUT DRIVER (10)



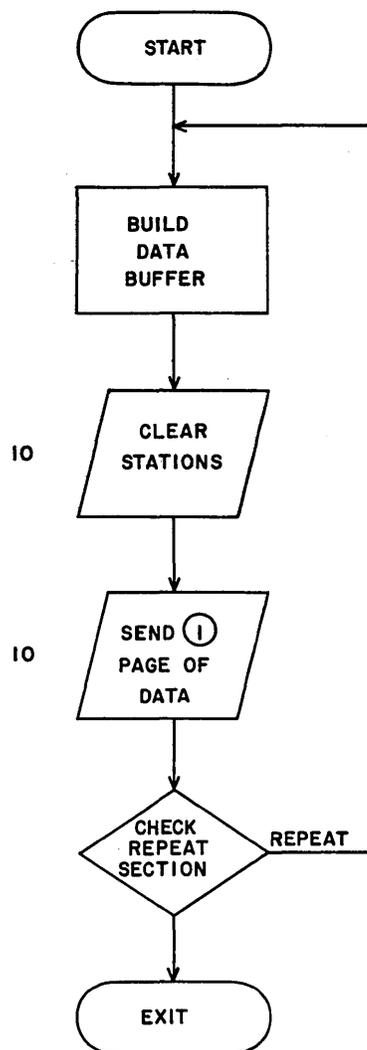
CLEAR TABLE ROUTINE (TABCLR)



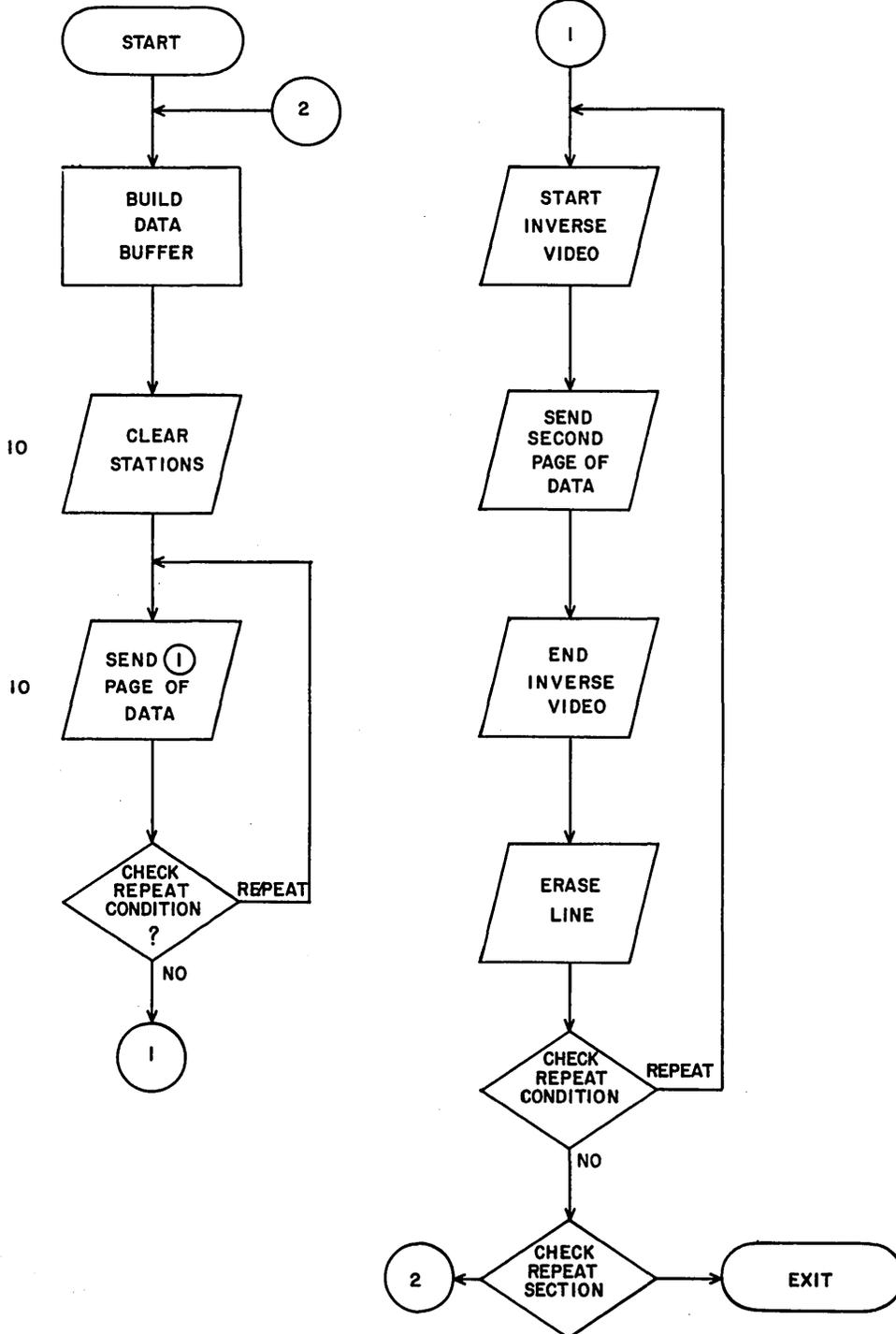
SECTION 0 (SECO)



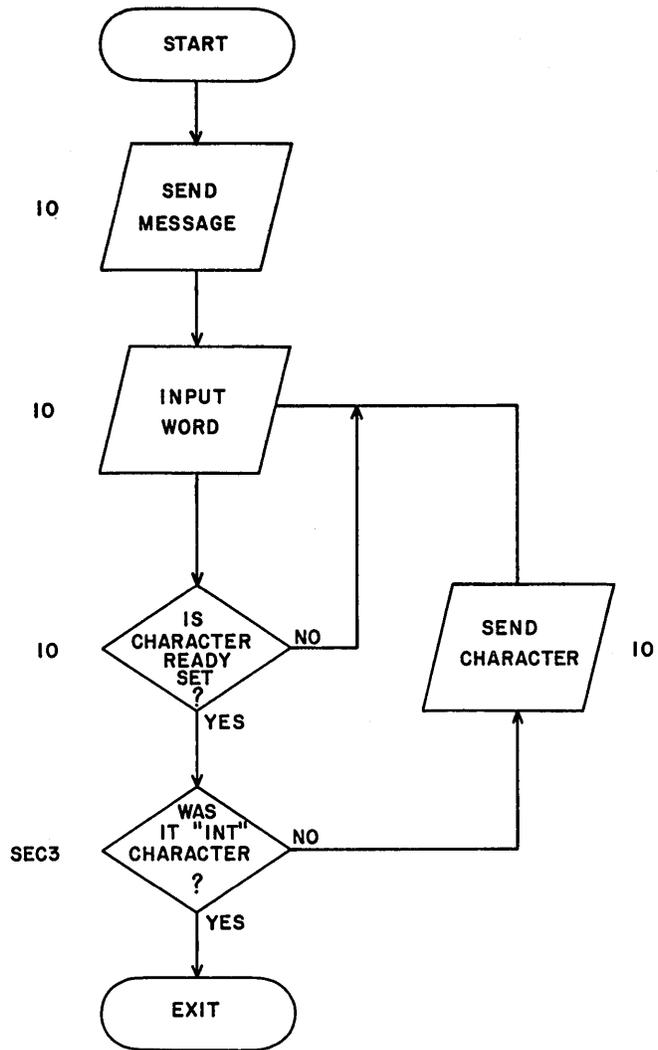
SECTION I (SECI)



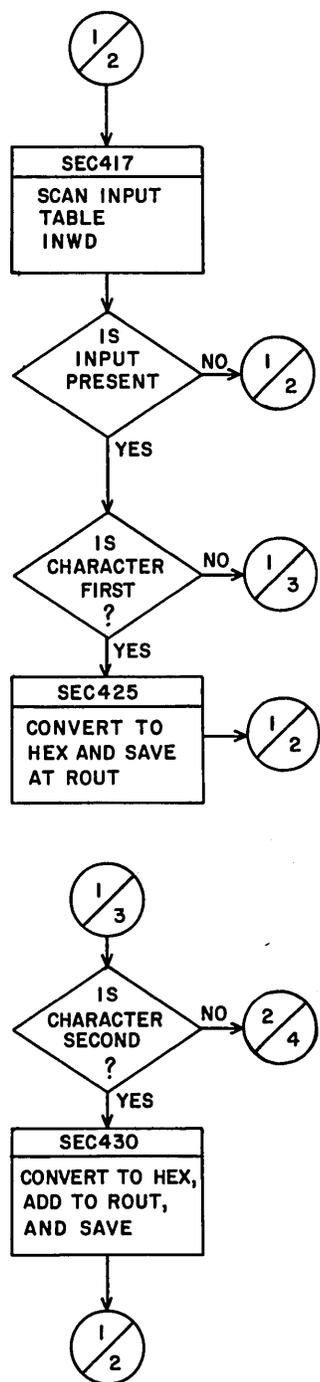
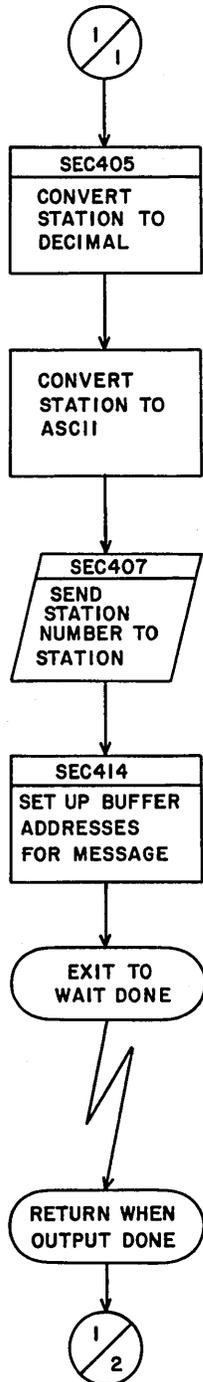
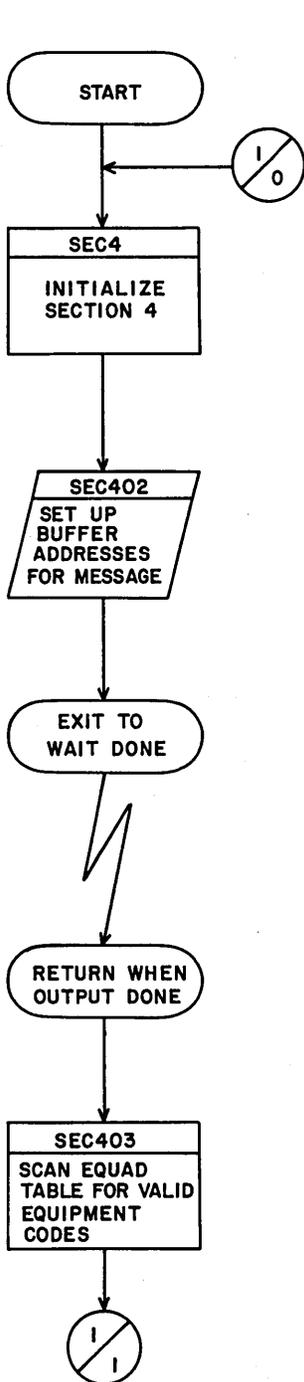
SECTION 2 (SEC2)



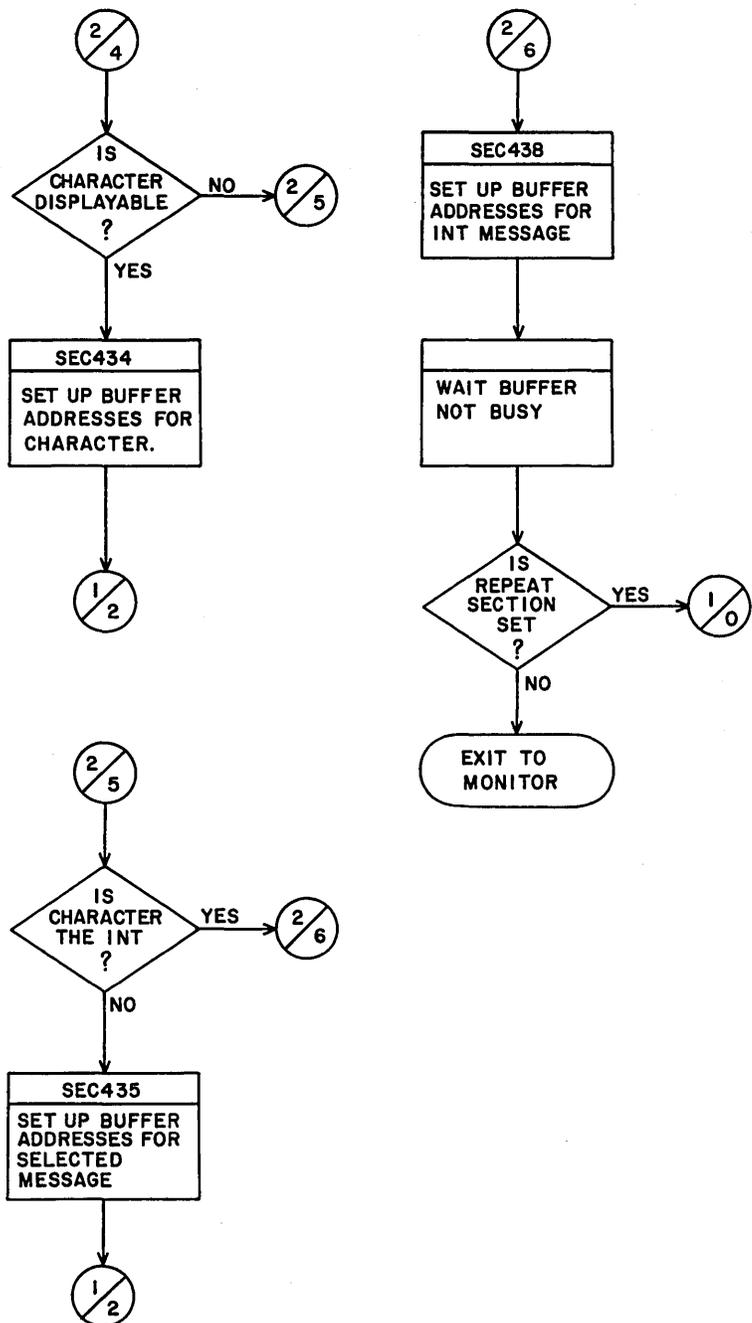
SECTION 3 (SEC3)



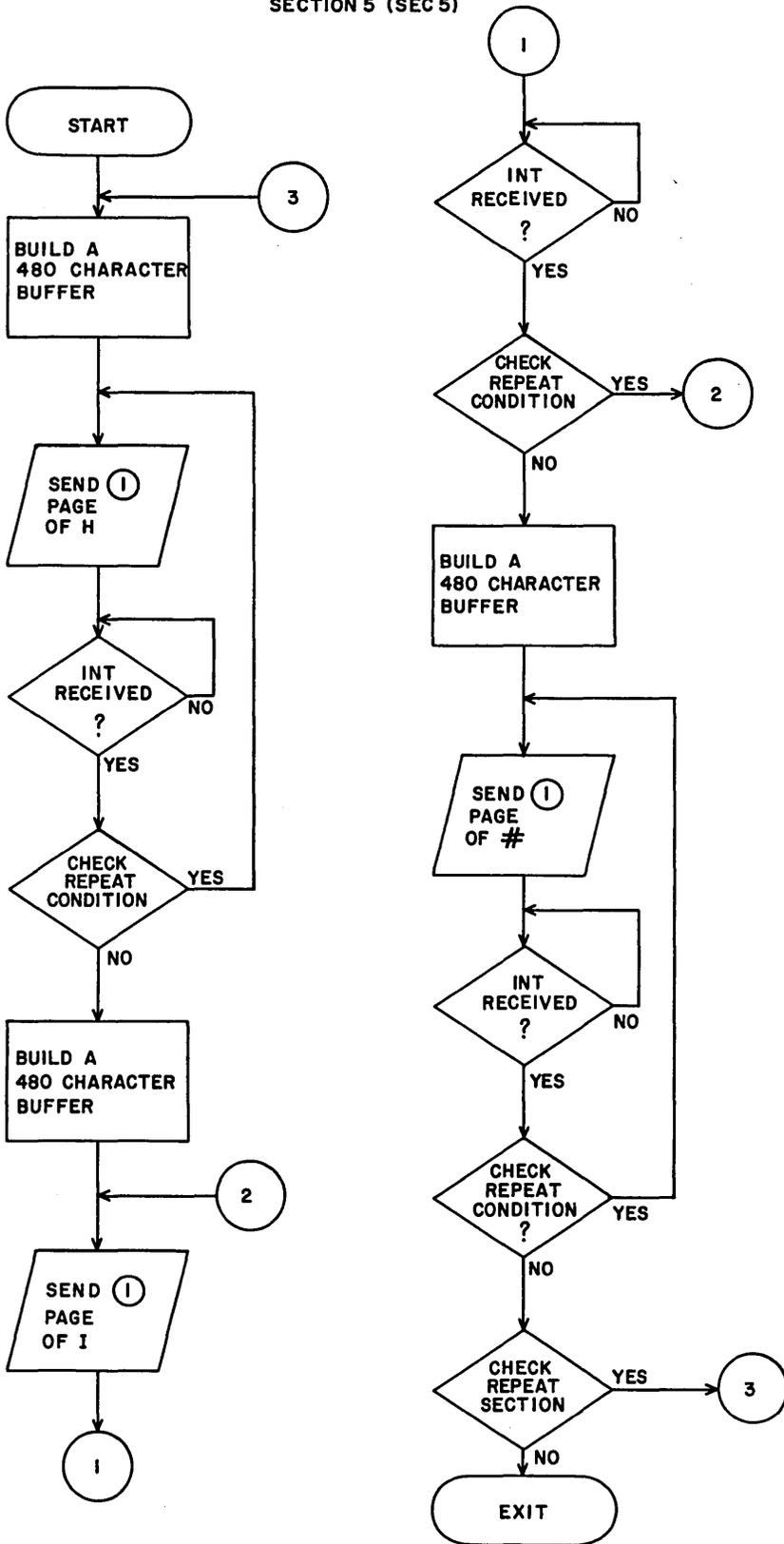
SECTION 4 (SEC 4)



SECTION 4 (SEC4)



SECTION 5 (SEC 5)



GENERAL PURPOSE GRAPHICS TERMINAL (GPGT)

I. INSTRUCTION MACROS

The macros described in this section are used to generate the GPGT Display Code Interpreter (DCI) instructions in tests GT0, GT1, GT2, GT3, and GT6. Some of the macros appear in a different form from one test to the next. The macro definition in the front of each test designates which form of a macro is used by that test. All changes made to the tests mentioned above must use these macro instructions to generate DCI instructions. Macros designated with an asterisk (*) to the left should not be used. Their macro definitions are to be deleted from the tests in a future revision.

A. GPGT DISPLAY FILE

1. Null Instruction
 NULL No parameters required
2. Relative Jump
 JMPR A (where A is the relative address tag)
3. Indirect Jump
 JMPI A (where A is the indirect address tag)
4. Direct Subroutine Entry
 SRED A (where A is the direct address tag)
5. Indirect Subroutine Entry
 SREI A (where A is the indirect address tag)
6. Relative Subroutine Exit
 SRXR A (where A is the relative address tag)
7. Indirect Subroutine Exit
 SRXI A (where A is the indirect address tag)
8. Execute Instruction
 EXCI A (where A is the indirect address tag)
9. Control Word
 CW A, B, S, W
 where A is the relative address tag
 B is the blink bit (0 or 1)
 S is the enable scissor bit (0 or 1)
 W is the execute scissor bit (0 or 1)

10. Move Beam Delta X
 MBX X (where X is the number of raster units)
11. Move Beam Delta Y
 MBY Y (where Y is the number of raster units)
12. Draw Vector Delta X
 DVX X (where X is the number of raster units)
13. Draw Vector Delta Y
 DVY Y (where Y is the number of raster units)
14. Draw Vector Delta X, Delta Y
 DVXY X, Y
 where X is the number of raster units on X
 Y is the number of raster units on Y
 The type bit and the delta intensity are forced to zero.
- * DVXY X, Y, I3
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I3 is the delta intensity value
 The type bit is forced to zero.
- DVXYT X, Y, I3
 where X is the number of raster units in X
 Y is the number of raster units in Y
 I3 is the delta intensity value
 The type bit is forced to one.
- DVXYI X, Y, I3
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I3 is the delta intensity value
 The type bit is forced to zero.
- DVXYIT X, Y, I3, T
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I3 is the delta intensity value
 T is the type bit
15. Short Vector Mode
- * DVSM S, I4, T
 where S is the scale field
 I4 is the delta intensity value
 T is the type field
- * XY X, Y, I1, I0
 where X is the number of raster units in X
 Y is the number of raster units in Y
 I1 is the upper bit of the delta intensity
 I0 is the lower bit of the delta intensity

SVM S
 where S is the scale field
 The delta intensity value and the type field are forced to zero.

SVMI S, I4
 where S is the scale field
 I4 is the delta intensity value
 The type field is forced to zero.

SVMIT S, I4, T
 where S is the scale field
 I4 is the delta intensity value
 T is the type field (DASH2 for .2 inch or
 DASH4 for .4 inch)

XY X, Y
 where X is the number of raster units in X
 Y is the number of raster units in Y
 The delta intensity value is forced to zero.

XYI X, Y, I
 where X is the number of raster units in X
 Y is the number of raster units in Y
 I is the delta intensity value

SVMEX No parameters required
 The delta X is forced to all ones.
 The delta Y and the delta intensity value are forced to zero.

16. 16-Bit Relative Vector

* DVR X, Y, I4, T
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I4 is the delta intensity value
 T is the type field

DVR X, Y
 where X is the number of raster units on X
 Y is the number of raster units on Y
 The delta intensity value and type field are forced to zero.

DVRI X, Y, I4
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I4 is the delta intensity value
 The type field is forced to zero.

DVRIT X, Y, I4, T
 where X is the number of raster units on X
 Y is the number of raster units on Y
 I4 is the delta intensity value
 T is the type field (DASH2 for .2 inch or
 DASH4 for .4 inch)

17. 16-Bit Absolute Beam Movement

- * MBA X, Y, I4, T
where X is the number of raster units on X
Y is the number of raster units on Y
I4 is the delta intensity value
T is the type field
- MBA X, Y
where X is the number of raster units on X
Y is the number of raster units on Y
The delta intensity value if forced to all ones.
The type field is forced to zero.
- MBAI X, Y, I4
where X is the number of raster units on X
Y is the number of raster units on Y
I4 is the delta intensity value
The type field is forced to zero.
- MBAIT X, Y, I4, T
where X is the number of raster units on X
Y is the number of raster units on Y
I4 is the delta intensity value
T is the type field (DASH2 for .2 inch or
DASH4 for .4 inch)

18. 16-Bit Negative Relative Beam Movement

- MBNR X, Y, I4, T
where X is the number of raster units on X
Y is the number of raster units on Y
I4 is the delta intensity value
T is the type field
- MBNRI X, Y, I4
where X is the number of raster units on X
Y is the number of raster units on Y
I4 is the delta intensity value
The type field is forced to zero.

19. Symbol Mode-Fixed Spacing

- * CMFS S, I4, V, K
where S is the size field
I4 is the intensity value
V is the 90 degree orientation bit
K is the italics bit
- CMFS S
where S is the size field
The intensity value, the 90 degree orientation bit, and the
italics bit are forced to zero.

CMFSI S, I4
 where S is the size field
 I4 is the intensity value
 The 90 degree orientation bit and the italics bit are forced to zero.

CMFSIT S, I4, TC
 where S is the size field
 I4 is the intensity value
 TC is the type code (IT for italics, OR for 90 degree orientation, or ITOR for 90 degree orientation of italics)

CMEX No parameters required
 A symbol mode exit character is forced into the upper ASCII character. The lower character is zero.

20. Symbol Mode-Variable Spacing

* CMVS X, Y, S, I4, V, K
 where X is the number of raster units on X spacing
 Y is the number of raster units on Y spacing
 S is the size field
 I4 is the intensity value
 V is the 90 degree orientation bit
 K is the italics bit

CMVS X, Y, S
 where X is the number of raster units on X spacing
 Y is the number of raster units on Y spacing
 S is the size field
 The intensity value, the 90 degree orientation bit, and the italics bit are forced to zero.

CMVSI X, Y, S, I4
 where X is the number of raster units on X spacing
 Y is the number of raster units on Y spacing
 S is the size field
 I4 is the intensity value
 The 90 degree orientation bit and the italics bit are forced to zero.

CMVSIT X, Y, S, I4, TC
 where X is the number of raster units on X spacing
 Y is the number of raster units on Y spacing
 S is the size field
 I4 is the intensity value
 TC is the type code (IT for italics, OR for 90 degree orientation or ITOR for 90 degree orientation of italics)

CMEX No parameters required
 A symbol mode exit character is forced into the upper ASCII character. The lower character is zero.

21. Plot Symbol Mode

- * CMPL S, I4, C, V, K
 where S is the size field
 I4 is the intensity value
 C is the hex value for the ASCII character
 V is the 90 degree orientation bit
 K is the italics bit
- CMPL S, C
 where S is the size field
 C is the hex value for the ASCII character
 The intensity value, the 90 degree orientation bit, and the
 italics bit are forced to zero.
- CMPLI S, C, I4
 where S is the size field
 C is the hex value for the ASCII character
 I4 is the intensity value
 The 90 degree orientation bit and the italics bit are forced
 to zero.
- CMPLIT S, C, I4, TC
 where S is the size field
 C is the hex value for the ASCII character
 I4 is the intensity value
 TC is the type code (IT for italics, or for 90 degree
 orientation or ITOR for 90 degree orientation of
 italics)
- CMPLEX No parameters required
 A plot symbol mode instruction is generated. A symbol mode
 exit character is forced into the ASCII plot character field.
 This size field, intensity value and type code are forced to
 zero.

22. Conditional Control Instruction

All conditional control instruction macros follow the format:

- Jtcf Parameters (if any)
 where J always appears to designate a jump
 t is the type of jump
 1 - jump over next word
 2 - jump over next two words
 S - jump to start of item
 E - jump to end of item
 c is the condition or inversion of the jump
 O - jump if condition (true)
 N - jump if not condition (false)
 E) used only in jump on
 G) zoom level
 f is the function tested
 HIT - jump on light pen hit
 SW - jump on light pen switch
 W11 - jump on 11-bit window
 W12 - jump on 12-bit window
 CCR - jump on conditional control register
 EQ - cyclic jump
 ZL - jump on zoom level

23. Jump on Light Pen Hit
 JtcHIT No parameters required
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump on hit or N for jump on no hit)
24. Jump on Light Pen Switch
 JtcSW No parameters required
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump if switch closed or N for jump
 if switch open)
25. Jump on 11-Bit Window
 JtcW11 No parameters required
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump if beam is on window or
 N for jump if beam is off window)
26. Jump on 12-Bit Window
 JtcW12 No parameters required
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump if beam is on window or
 N for jump if beam is off window)
27. Jump on Conditional Control Register
 JtcCCR B
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump if the bit is a one or
 N for jump if the bit is a zero)
 B is the bit position to be tested
28. Cyclic Jump
 JtcEQ V, C
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (O for jump if value and count are equal or
 N for jump if value and count are not equal)
 V is the constant that is compared against the count
 C is the count that gets incremented
29. Jump on Zoom Level
 JtcZL L
 where t is the type of jump (1, 2, S, or E)
 c is the condition or inversion of the jump
 (G for jump if the current zoom level would draw a
 picture larger than would be drawn at a zoom level
 equal to the operand; or E for jump if the current
 zoom level would draw a picture the same size or
 smaller than would be drawn at a zoom level equal
 to the operand)
 L is the operand used in the decision described above

30. Parameter Word 1

PAR1 I, C1, L, C2, NZ
where I is the absolute intensity value
C1 is the light pen enable bit (1 enables)
L is the light pen on bit (1 turns on)
C2 is the zoom enable bit (1 enables)
NZ is the zoom on bit (1 turns on)

* PAR1 I, CL, L, CZ, Z
where I is the absolute intensity value
CL is the light pen enable bit (1 enables)
L is the light pen on bit (1 turns on)
CZ is the zoom enable bit (1 enables)
Z is the zoom off bit (1 turns off)

31. Parameter Word 2

PRGINT No parameters required
The function field is forced to zero, selecting a program interrupt.

W11 No parameters required
The function field is forced to 2, selecting an 11-bit window.

W12 No parameters required
The function field is forced to 3, selecting a 12-bit window.

PENON No parameters required
The function field is forced to 4, providing the second level of light pen enable.

PENOFF No parameters required
The function field is forced to 5, providing the second level of light pen disable.

* EOF No parameters required
The function field is forced to 6, marking an end of frame.

SOF No parameters required
The function field is forced to 6, marking an end of frame.

32. Load Register

All load register instruction macros follow the format:

Lr A

where L always appears to designate a load
A is the relative address tag
r is the register name

The following register names are legal:

PADR - P Address (00)
DATUM - DATUM (01)
SADR - Execute Instruction Address (02)
LVADR - Last Vector Address (03)
CWADR - Control Word Address (04)
HIT - Light Pen Hit Address (05)

HITX - Light Pen Hit X Position (06)
 HITY - Light Pen Hit Y Position (07)
 WLOCX - Window Location X Position (08)
 WLOCY - Window Location Y Position (09)
 HITC - Symbol/Short Vector Count (0A)
 CCR - Conditional Control Register (0B)
 SPAR1 - Spare Register (0C)
 SPAR2 - Spare Register (0D)
 ZL - Zoom Level (18)
 WLIM - Window Limits (19)
 INTEN - Interrupt Enable (1A)
 INTIN - Interrupt Disable (1B)

33. Unload Registers

All unload register instruction macros follow the format:

Ur A

where L always appears to designate an unload
 A is the relative address tag
 r is the register name

The following register names are legal:

PADR - P Address (00)
 DATUM - DATUM (01)
 SADR - Execute Instruction Address (02)
 LVADR - Last Vector Address (03)
 CWADR - Control Word Address (04)
 HIT - Light Pen Hit Address (05)
 HITX - Light Pen Hit X Position (06)
 HITY - Light Pen Hit Y Position (07)
 WLOCX - Window Location X Position (08)
 WLOCY - Window Location Y Position (09)
 HITC - Symbol/Short Vector Count (0A)
 CCR - Conditional Control Register (0B)
 SPAR1 - Spare Register (0C)
 SPAR2 - Spare Register (0D)
 BPOSX - Beam Position X (10)
 BPOSY - Beam Position Y (11)

GENERAL PURPOSE GRAPHICS TERMINAL (GPGT) TROUBLESHOOTING PROGRAM
(GT0 Test No. 70)

I. INTRODUCTION

The purpose of this program is to aid the customer engineer and checkout technician in generation and execution of his own display file for the GPGT. To accomplish this, the operator must type the hexadecimal codes for the GPGT instructions at the GPGT keyboard. This program also includes a core dump to the display console.

II. REQUIREMENTS

A. HARDWARE

1. Minimum Configuration
1700

1705 Interrupt Data Channel
CC104A/B/C GPGT Console
CA122A Keyboard
Input device for SMM17

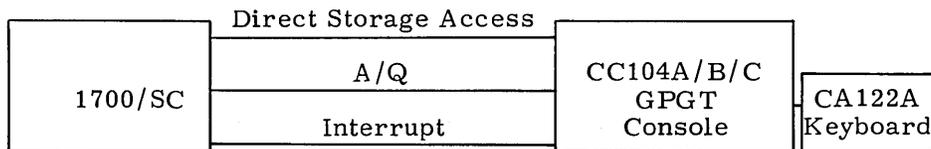
System Controller (SC)

1772 Magnetic Core Memory Module
1775 A/Q Interrupt Data Channel
1773 Direct Storage Access Channel
CC104A/B/C GPGT Console
CA122A Keyboard
Input Device for SMM17

2. Core Requirements

The minimum amount of core required is 4K.

3. Equipment Configuration



B. SOFTWARE

The program operates under control of the SMM17 monitor.

C. ACCESSORIES

None.

III. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The program is loaded as test number 70 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First Stop (overflow light on)

(A) = 7021 - test ID stop

(Q) = Stop/Jump parameter

Second Stop

(A) = Interrupt line for display code interpreter

(Prestored as 0004-bit 2 designating interrupt line 2)

This parameter must not be changed after the initial parameter stop.

(Q) = Not Used

2. DCI Switch Setting

DCI instruction/clock control switches must be UP.

The DCI PROTECT switch must be in UNPROTECTED.

The DCI SENSE REFRESH FAULT switch must be UP.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters

1 - Not sensed by this program

2 - Not sensed by this program

3 - Not sensed by this program

4 - Not sensed by this program

5 - Not sensed by this program

6 - Not sensed by this program

7 - Not used

8 - Omit typeout

9 - Bias return address display

10 - Not sensed by this program

11 - Not sensed by this program

12 - Not sensed by this program

13 - Not sensed by this program

14 - Not sensed by this program

15 - Run this program alone

(This bit should be set when two or more tests in the test list use the same display code interpreter equipment number. This allows the tests to be run consecutively, since they cannot be multiplexed.)

C. SECTION DESCRIPTION INDEX

Not applicable

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization.

GT0 (No. 70) GPGT TROUBLESHOOTING TEST

IA = XXXX

2. Normal Display Console Message
Displayed at the console after teletype message.

```

FUNCT-
LOC   0 1 2 3 4 5 6 7 8 9 A B C D E F

```

3. Error Messages
No error messages are used. Illegal keyboard codes and illegal operations are ignored.

B. MESSAGE DICTIONARY

Not applicable

V. DESCRIPTION

A. GENERAL

This program allows the selection of four functions: dump core to the display, make changes to the core image on the display, store these changes back into core, and run a display file. These four functions are controlled from the display console keyboard. Key depression controls a cursor on the display or inserts a symbol at the cursor position. Initially the display is as follows:

```

FUNCT-
LOC   0 1 2 3 4 5 6 7 8 9 A B C D E F

```

Lower case on the keyboard must be selected. Upper case codes from the keyboard are ignored. Although lower case on the keyboard is used, display of letters is in upper case to be compatible with normal hexadecimal A-F notation.

To enable selection of a function, type an R, S, or T depending upon which function is desired. This brings the last core dump (if any) and places the cursor following the FUNCT. If an error is made while typing in the function selection, depress BACKSPACE and correct your error. Illegal keys are ignored. Illegal functions are discarded and the cursor replaced following the FUNCT. No error messages are given.

1. Dump Core to Display (Read Core)

Type: RCnnnn (ETX)
where nnnn is the starting address
(leading zeros need not be typed)

Core is displayed in 16 lines with 16 locations to each line. The starting address of each line is an even multiple of 10_{16} . The starting address of each

line is displayed to the left under the heading LOC. The cursor is placed at the upper hexadecimal digit of the first location.

CORE IS READ ONLY ONCE FOR EACH RC COMMAND.
IT IS NOT READ CONTINUOUSLY.

2. Change the Core Image

First follow the procedure to dump core to display.

Then move the cursor to the location to be changed. Type the desired change. An asterisk (*) is displayed to the left of each location changed.

NOTE

Only the display is changed. No changes occur in memory. To change memory follow the procedure to store into core.

Legal cursor moves are as follows:

SKIP	- advances cursor one hexadecimal digit bypassing spaces between locations
BACKSPACE	- backspaces cursor one hexadecimal digit bypassing spaces between locations
LINE DOWN	- advances cursor one line
LINE UP	- moves cursor back one line
NEW LINE	- advances cursor to start of the next line
RESET	- moves cursor to upper hexadecimal digit of the first location

3. Store into Core (Transfer into Core)

First follow the procedure to dump core to display and to change the core image.

Then type: T C (ETX)

Each location with an asterisk (*) to its left is stored into memory. The asterisks are cleared.

4. Run A Display File (Start Display)

If a display file must first be generated, follow the procedure to dump core to display, to change the core image, and to store into core.

Then type: SDnnnn (ETX)

where nnnn is the starting address of the display file
(leading zeros need not be typed)

NOTE

To avoid burning the CRT, ensure that the display file contains a refresh instruction and a jump back to the beginning. Also set beam defocus.

5. Terminate the Program

Type: ETX with no function given.

B. SECTION DESCRIPTIONS

Not applicable.

C. SUBPROGRAM DESCRIPTIONS

Not applicable.

VI. APPLICATIONS

Only a few types of DCI instructions are used in this program. However, if one of them is failing, generation and execution of a display file with this program may be impossible. The DCI instructions used in this program are as follows:

- Control Word
- Parameter Word 1
- Parameter Word 2 (12-Bit Window and End of Frame)
- Absolute Beam Movement
- Character Mode-Fixed Spacing
- Move Beam X
- Relative Jump

The control word instructions are used only to allow the cursor to blink and could be eliminated.

GENERAL PURPOSE GRAPHICS TERMINAL (GPGT) DISPLAY CODE
 INTERPRETER COMMAND TEST
 (GT1 Test No. 71)

I. INTRODUCTION

The purpose of this test is to verify the operation of the Display Code Interpreter (DCI). This test checks the A/Q channel functions, interrupts, and clock/instruction stepping of DCI instructions. During clock stepping after each clock pulse, the entire TV monitor is read and compared against a table of expected changes. After the instruction has been completed, the parameter registers are also read and compared against a table of expected changes. After an instruction step, both the TV monitor and the parameter registers are read and compared against a table of expected changes.

II. REQUIREMENTS

A. HARDWARE

1. Minimum Configuration

1700

1705 Interrupt Data Channel
 CC104A/B/C GPGT Console
 Input Device for SMM17

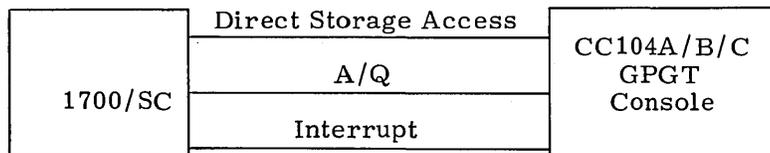
System Controller (SC)

1772 Magnetic Core Memory Module (12K)
 1775 A/Q Interrupt Data Channel
 1773 Direct Storage Access Channel
 CC104A/B/C GPGT Console
 Input Device for SMM17

2. Core Requirements

The minimum amount of core required is 12K.

3. Equipment Configuration



B. SOFTWARE

The test operates under control of SMM17 monitor.

C. ACCESSORIES

None.

III. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 71 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First stop (overflow light on)

- (A) = 7131 test ID stop
- (Q) = Stop/Jump parameter

Second stop

- (A) = First group of section selection bits
(prestored as $FFFE_{16}$)

- Bit 0 = Not used
- Bit 1 = Section 1 - A/Q functions
- Bit 2 = Section 2 - Load/unload instructions (clock step)
- Bit 3 = Section 3 - Load/unload instructions (instruction step)
- Bit 4 = Section 4 - Jump instructions (clock step)
- Bit 5 = Section 5 - Jump instructions (instruction step)
- Bit 6 = Section 6 - Parameter word instructions (clock step)
- Bit 7 = Section 7 - Parameter word instructions (instruction step)
- Bit 8 = Section 8 - Move beam instructions (clock step)
- Bit 9 = Section 9 - Move beam instructions (instruction step)
- Bit 10 = Section A - Conditional control instructions (clock step)
- Bit 11 = Section B - Conditional control instructions (instruction step)
- Bit 12 = Section C - Draw vector instructions (clock step)
- Bit 13 = Section D - Draw vector instructions (instruction step)
- Bit 14 = Section E - Control word instructions (clock step)
- Bit 15 = Section F - Control word instructions (instruction step)

- (Q) = Second group of section selection bits
(prestored as $002F_{16}$)

- Bit 0 = Section 10 - Character mode instructions (clock step)
- Bit 1 = Section 11 - Character mode instructions (instruction step)
- Bit 2 = Section 12 - Execute instruction (clock step)
- Bit 3 = Section 13 - Execute instruction (instruction step)
- Bit 4 = Not used
- Bit 5 = Section 15 - Start/stop and interrupt

Third stop

- (A) = Interrupt line for display code interpreter
(prestored as 0004_{16} - bit 2 designating interrupt line 2)
This parameter must not be changed after the initial parameter stop.

- (Q) = Power line frequency
(prestored as 0060_{16})

For 60-cycle input power, set to 0060_{16} .

For 50-cycle input power, set to 0050_{16} .

2. DCI and Display Console Switch Setting

The DCI instruction/clock control switches must be up.
 The DCI PROTECT switch must be in the UNPROTECTED position.
 The DCI SENSE REFRESH FAULT switch must be DOWN.

NOTE

To avoid burning the CRT, ensure that the BEAM DEFOCUS switch on the display console is set.

3. Stop/Jump Parameter Word

- Bit 0 - Stop to enter parameters
- Bit 1 - Stop at end of section
- Bit 2 - Stop at end of test
- Bit 3 - Stop on error
- Bit 4 - Repeat condition
- Bit 5 - Repeat section
- Bit 6 - Repeat test
- Bit 7 - Not used
- Bit 8 - Omit typeouts
- Bit 9 - Bias return address display
- Bit 10 - Re-enter parameters
- Bit 11 - Set audible alarm on error
- Bit 12 - Not sensed by this test
- Bit 13 - Not sensed by this test
- Bit 14 - Not sensed by this test
- Bit 15 - Run this test alone
 (This bit should be set when two or more tests in the test list use the same display code interpreter equipment number. This allows the tests to be run consecutively, since they cannot be multiplexed.)

C. SECTION DESCRIPTION INDEX

<u>Number</u>	<u>Name</u>	<u>Run Time (Seconds)</u>
0	Not Used	
1	A/Q Functions	2
2	Load/Unload Instructions (clock step)	41
3	Load/Unload Instructions (instruction step)	4
4	Jump Instructions (clock step)	3
5	Jump Instructions (instruction step)	1
6	Parameter Word Instructions (clock step)	3
7	Parameter Word Instructions (instruction step)	1
8	Move Beam Instructions (clock step)	22
9	Move Beam Instructions (instruction step)	2
A	Conditional Control Instructions (clock step)	21
B	Conditional Control Instructions (instruction step)	4
C	Draw Vector Instruction (clock step)	40
D	Draw Vector Instruction (instruction step)	2
E	Control Word Instructions (clock step)	2
F	Control Word Instructions (instruction step)	1
10	Character Mode Instruction (clock step)	100
11	Character Mode Instruction (instruction step)	8
12	Execute Instruction (clock step)	1
13	Execute Instruction (instruction step)	1
14	Not Used	
15	Start/Stop and Interrupt	1
		Total run time 260

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization

GT1 (No. 71) GPGT DCI TEST

2. Stop at End of Section

First stop (overflow light on)

(A) = 7122 - test ID stop

(Q) = Stop/Jump parameter

Second Stop

(A) = Section number

(Q) = Return address

3. Stop at End of Test

First Stop (overflow light on)

(A) = 7124 - test ID stop

(Q) = Stop/Jump parameter

Second Stop

(A) = Pass number

(Q) = Return address

4. Stop on Error

All error message displays use basically the standard SMM17 error message format. The format of the first two stops is the same for all types of errors. The format of the third, fourth, and fifth stops is determined by the type of error. The format for the first and second stops is as follows:

First Stop (overflow light on)

(A) = 71X8 - test ID stop

where X is the number of stops

(Q) = Stop/Jump parameter

Second Stop

(A) = XXYZ where XX = Section number

Y = Condition (or subsection)

Z = Error type

(Q) = Address pointer to where within a condition the error occurred.

This pointer is not the same as the return address found in other SMM17 tests. The address points to where execution stopped when the error occurred, but not to where execution will continue after the error. Where execution continues after the error is determined by the repeat condition bit of the Stop/Jump parameter. If the repeat condition bit is set, execution will continue at a backward marker (a recovery point to repeat the condition designated in (A) of this second stop). If the repeat condition bit is not set, execution will continue at a forward marker (a recovery point to skip around the remainder of the condition designated in (A) of this second stop).

B. MESSAGE DICTIONARY

The upper hexadecimal digit of the two-digit error message code designates the condition (or subsection) that failed. The lower digit is the error type. This message dictionary describes the error types.

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X1	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive internal reject A = I/O instruction Q = Q register function code
X2	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive external reject A = I/O instruction Q = Q register function code
X3	FNER STER	FNI230 STI220	RESPONSE, expect external reject, receive internal reject A = I/O instruction Q = Q register function code
X4	FNER STER	FNI200 STI200	RESPONSE, expect external reject, receive reply A = I/O instruction Q = Q register function code
X5	CMPALL	CMI030	TV monitor has unexpected display A = First word of DCI instruction being stepped Q = YYYY Where X is the current DCI word number (0, 1, or 2) and YYY is the clock pulse number. A pseudo word number of 4 is used to desig- nate when start draw has occurred. The clock pulse number then refers to LDU clocks. When the instruction is completed Q is FFFF ₁₆ . A = Actual TV display Q = Expected TV display A = Failing TV word number Q = Previous TV display
X6	CMPALL	CMI030	REGISTER, parameter register has unexpected contents A = First word of DCI instruction being stepped Q = FFFF A = Actual register contents Q = Expected register contents A = Failing register number Q = Previous register contents

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X7	CKCORE	CKI020	STORAGE, core location has unexpected contents A = First word of DCI instruction being stepped Q = FFFF ₁₆ A = Actual location contents Q = Expected location contents A = Failing location address (Biasing is determined by bit 9 of Stop/Jump parameter) Q = Not used
X8	WAIT	WAI050 WAI060	TIME, interrupt did not occur within expected time limits A = First word of DCI instruction being stepped Q = FFFF ₁₆ A = Lower limit (milliseconds) Q = Upper limit (milliseconds) A = Actual time (milliseconds) Q = Expected interrupt (bit corresponding to register 20 ₁₆)
X9	DCIPRO	DCI002	INTERRUPT, internal reject during interrupt state A = I/O instruction Q = Q register function code
XA	DCIPRO	DCI002	INTERRUPT, external reject during interrupt state A = I/O instruction Q = Q register function code
XB	RINT	RIT010	INTERRUPT, missing A = First word of DCI instruction being stepped Q = FFFF ₁₆ A = Actual interrupts (bits corresponding to register 20 ₁₆) Q = Expected interrupts (bits corresponding to register 20 ₁₆)
XC	DCIPRO	DCI020	INTERRUPT, no interrupt status bit set when an interrupt occurred A = First word of DCI instruction being stepped Q = XYYY Where X is the current DCI word number (0, 1, or 2) and YYY is the clock pulse number. When the instruction is completed Q is FFFF ₁₆ . A = 0000 (actual status) Q = Expected interrupts (bits corresponding to register 20 ₁₆)

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
XD	DCIPRO	DCI030	<p>INTERRUPT, unexpected</p> <p>A = First word of DCI instruction being stepped</p> <p>Q = XYYY</p> <p>Where X is the current DCI word number (0, 1, or 2) and YYY is the clock pulse number.</p> <p>When the instruction is completed Q is FFFF₁₆.</p> <p>A = Actual interrupts (bits corresponding to register 20₁₆)</p> <p>Q = Expected interrupts (bits corresponding to register 20₁₆)</p>
XE	DCIPRO	DCI060	<p>INTERRUPT, unable to clear interrupt status</p> <p>A = First word of DCI instruction being stepped</p> <p>Q = XYYY</p> <p>Where X is the current DCI word number (0, 1, or 2) and YYY is the clock pulse number.</p> <p>When the instruction is completed Q is FFFF₁₆.</p> <p>A = Actual interrupt status after attempted clear (bits corresponding to register 20₁₆)</p> <p>Q = Expected interrupt status after attempted clear (bits corresponding to register 20₁₆)</p> <p>A = Function used to attempt clear interrupt status</p> <p>00 = Cleared when interrupt status or keyboard register unloaded</p> <p>1A = Load interrupt enable register</p> <p>1B = Load interrupt disable register</p> <p>30 = Reset</p> <p>Q = Not used</p>

V. DESCRIPTION

A. GENERAL

Sections which step DCI instructions are arranged in section pairs. The even numbered section clock steps the instruction and the odd numbered section instruction steps the instruction. Both sections of a section pair use the same routine, but the routine is entered with a different parameter in the Q register (0, even or 1, odd).

Each condition (or subsection) begins with a reset function and ends with a check of the repeat condition bit of the Stop/Jump parameter. Most conditions are executed a pre-determined number of counts. When the repeat condition bit is set, this count is not advanced.

Unexpected interrupts are enabled in Sections 4-15.

B. SECTION DESCRIPTIONS

1. Section 1 - A/Q Functions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCAQ	Condition 0 - scratchpad, all ones
0101	P1I010	Reset. Expect reply.
0102		
0105		Read TV interrupt enable. Expect 0000.
0101		Load all scratchpad registers with FFFF.
0102		Expect reply.
0101		Unload all scratchpad registers. Expect reply.
0102		
0106		Verify that scratchpad registers contain FFFF. Check repeat condition stop/jump bit. Do 16 times.
	POI000	Condition 1 - scratchpad, all zeros
0111	POI010	Reset. Expect reply.
0112		
0115		Read TV interrupt enable. Expect 0000.
0111		Load all scratchpad registers with 0000.
0112		Expect reply.
0111		Unload all scratchpad registers. Expect reply.
0112		
0116		Verify that scratchpad registers contain 0000. Check repeat condition stop/jump bit. Do 16 times.
	S1I000	Condition 2 - scratchpad, shifted one
0121	S1I010	Reset. Expect reply.
0122		
0125		Read TV interrupt enable. Expect 0000.
0121		Load all scratchpad registers with one bit (start with 0001 and shift one bit position left each pass).
0122		Expect reply.
0121		Unload all scratchpad registers. Expect reply.
0122		
0126		Verify that scratch registers contain the value loaded. Check repeat condition stop/jump bit. Do for each bit position.
	S0I000	Condition 3 - scratchpad, shifted zero

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0131	SOI000	Reset. Expect reply.
0132		
0135		Read TV interrupt enable. Expect 0000.
0131		Load all scratchpad registers with all bits except one (start with FFFE and shift one bit position left each pass). Expect reply.
0132		
0131		Unload all scratchpad registers. Expect reply.
0132		
0136		Verify that scratchpad registers contain the value loaded. Check repeat condition stop/jump bit. Do for each bit position.
	SRI000	Condition 4 - scratchpad, register number
0141	SRI010	Reset. Expect reply.
0142		
0145		Read TV interrupt enable. Expect 0000.
0141	SRI020	Load all scratchpad registers with its register number. Expect reply.
0142		
0141	SRI016	Unload all scratchpad registers. Expect reply.
0142		
0146		Verify that scratchpad registers contain the value loaded. Check repeat condition stop/jump bit. Do 16 times.
	UZI000	Condition 5 - zoom level
0151	UZI010	Reset. Expect reply.
0152		
0155		Read TV interrupt enable. Expect 0000.
0151		Load zoom level register (use levels 7, 0...6). Expect reply.
0152		
0151		Read TV zoom level. Expect reply.
0152		
0155		Verify that zoom level register contains the value loaded. Check repeat condition stop/jump bit. Do for each zoom level.
	UWI000	Condition 6 - window limits
0161	UWI010	Reset. Expect reply.
0162		
0165		Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0161 0162		Load window limits registers (use FFFF, 0000, AAAA, 5555). Expect reply.
0161 0162		Read TV window limits. Expect reply.
0165		Verify that window limits register contains the value loaded. Check repeat condition stop/jump bit. Do for four values.
	UEI000	Condition 7 - interrupt enable
0171 0172 0175	UE010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0171 0172		Load interrupt enable register (use EF9F, 0000, AA8A, 4515). Expect reply.
0171 0172		Read TV interrupt enable. Expect reply.
0175		Verify that interrupt enable register contains the value loaded. Check repeat condition stop/jump bit. Do for four values.
	UDI000	Condition 8 - interrupt disable
0181 0182 0185	UDI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0181 0182	UDI020	Load interrupt enable register with EF9F. Expect reply.
0181 0182		Read TV interrupt enable. Expect reply.
0185		Verify that interrupt enable register contains EF9F.
0181 0182		Load interrupt disable register (use 0000, EF9F, 2515, CA8A). Expect reply.
0181 0182 0185		Read TV interrupt enable register. Expect reply.
0185		Verify that interrupt enable register contains expected contents (EF9F, 0000, CA8A, 2515). Check repeat condition stop/jump bit. Do for four values.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	URI000	Condition 9 - write limits
0191 0192 0195	URI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0191 0192		Load write limits register (use FFFF, 0000, AAAA, 5555). Expect reply.
0191 0192		Read TV write limits. Expect reply.
0195		Verify that write limits register contains the loaded value. Check repeat condition stop/jump bit. Do for four values.
	ILI000	Condition A - illegal functions
01A1 01A2 01A5	ILI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
01A3 01A4		Attempt illegal output function (use all illegal functions through 7F). Expect external reject.
01A3 01A4		Attempt illegal input function (use all illegal functions through 7F). Expect external reject. Check repeat condition stop/jump bit. Do for all illegal functions.
	CSI000	Condition B - clock step
01B1 01B2 01B5	CSI010	Reset. Expect reply. Read TV interrupt enable. Expect reply.
01B1 01B2 01B6		Load and unload P register. Expect reply.
01B1 01B2 01B5 01B6		Clock step a Null instruction. Check repeat condition stop/jump bit. Do 16 times.
	ISI000	Condition C - instruction step
01C1 01C2 01C5		Reset. Expect reply. Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
01C1 01C2 01C6		Load and unload P register. Expect reply.
01C1 01C2 01C5 01C6		Instruction step a Null instruction.
		Check repeat condition stop/jump bit. Do 16 times.

2. Section 2 and 3 - Load and Unload Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCREG	Condition 0 - scratchpad, all ones
0201/0301 0202/0302 0205/0305	R1I010	Reset. Expect reply.
0201/0301		Read TV interrupt enable. Expect 0000.
0201/0301		Load and unload P register. Expect reply.
0202/0302 0206/0306		
0201/0301 0202/0302 0205/0305 0206/0306	R1I020	Clock/instruction step a load register instruction.
0201/0301 0202/0302 0205/0305		Load write limits register so unload instruction is within limits. Set all protect bits in the write limits area except the location into which the unload instruction will write.
0201/0301 0202/0302 0205/0305 0206/0306	R1I030	Clock/instruction step an unload register instruction.
0207/0307		Verify that FFFF was written into core by the unload instruction.
		Check repeat condition stop/jump bit. Do for each scratchpad register except P.
	R0I000	Condition 1 - scratchpad, all zeros
0211/0311 0212/0312 0215/0315	R0I010	Reset. Expect reply.
		Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0211/0311 0212/0312 0216/0316		Load and unload P register. Expect reply.
0211/0311 0212/0312 0215/0315 0216/0316	R0I020	Clock/instruction step a load register instruction.
0211/0311 0212/0312 0215/0315		Load write limits register so unload instruction is within limits. Set all protect bits in the write limits area except the location into which the unload instruction will write.
0211/0311 0212/0312 0215/0315 0216/0316	R0I030	Clock/instruction step an unload register instruction.
0217/0317		Verify that 0000 was written into core by the unload instruction. Check for repeat condition stop/jump bit. Do for each scratchpad register except P.
	TAI000	Condition 2 - scratchpad, AAAA
0221/0321 0222/0322 0225/0325	TAI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0221/0321 0222/0322 0226/0326		Load and unload P register. Expect reply.
0221/0321 0222/0322 0225/0325 0226/0326	TAI020	Clock/instruction step a load register instruction.
0221/0321 0222/0322 0225/0325		Load write limits register so unload instruction is within limits. Set all protect bits in the write limits area except the location into which the unload instruction will write.
0221/0321 0222/0322 0225/0325 0226/0326	TAI030	Clock/instruction step an unload register instruction.
0227/0327		Verify that AAAA was written into core by the unload instruction. Check for repeat condition stop/jump bit. Do for each scratchpad register except P.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	T5I000	Condition 3 - scratchpad 5555
0231/0331 0232/0332 0235/0335	T5I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0231/0331 0232/0332 0236/0336		Load and unload P register. Expect reply.
0231/0331 0232/0332 0235/0335 0236/0336	T5I020	Clock-instruction step a load register instruction.
0231/0331 0232/0332 0235/0335		Load write limits register so unload instruction is within limits. Set all protect bits in the write limits area except the location into which the unload instruction will write.
0231/0331 0232/0332 0235/0335 0236/0336	T5I030	Clock/instruction step an unload register instruction.
0237/0337		Verify that 5555 was written into core by the unload instruction. Check for repeat condition stop/jump bit. Do for each scratchpad register except P.
	TRI000	Condition 4 - scratchpad, register number
0241/0341 0242/0342 0245/0345	TRI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0241/0341 0242/0341 0246/0346		Load and unload P register. Expect reply.
0241/0341 0242/0342 0245/0345 0246/0346	TRI020	Clock/instruction step a load register instruction.
0241/0341 0242/0342 0245/0345		Load write limits register so unload instruction is within limits. Set all protect bits in the write limits area except the location into which the unload instruction will write.
0241/0341 0242/0342 0245/0345 0246/0346	TRI030	Clock/instruction step an unload register instruction.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0247/0347		Verify that the register number was written into core by the unload instruction. Check for repeat condition stop/jump bit. Do for each scratchpad register except P.
	VZI000	Condition 5 - zoom level
0251/0351 0252/0352 0255/0355	VZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0251/0351 0252/0352 0256/0356		Load and unload P register. Expect reply.
0251/0351 0252/0352 0255/0355 0256/0356	VZI020	Clock/instruction step a load zoom level instruction (use 7, 06). Check repeat condition stop/jump bit. Do for eight values.
	VWI000	Condition 6 - window limits
0261/0361 0262/0362 0265/0365	VWI010	Reset. Expect reply Read TV interrupt enable. Expect 0000.
0261/0361 0262/0362 0266/0366		Load and unload P register. Expect reply.
0261/0361 0262/0362 0265/0365 0266/0366	VWI020	Clock/instruction step a load window limits instruction (use FFFF, 0000, AAAA, 5555). Check repeat condition stop/jump bit. Do for four values.
	VEI000	Condition 7 - interrupt enable
0271/0371 0272/0372 0275/0375	VEI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0271/0371 0272/0372 0276/0376		Load and unload P register. Expect reply.
0271/0371 0272/0372 0275/0375	VEI020	Clock/instruction step a load interrupt enable instruction (use EF9F, 0000, AA8A, 4515). Check repeat condition stop/jump bit. Do for four values.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	VII000	Condition 8 - interrupt disable
0281/0381 0282/0382 0285/0385	VII010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0281/0381 0282/0382 0286/0386		Load and unload P register. Expect reply.
0281/0381 0282/0382	VII016	Load interrupt enable register with EF9F. Expect reply.
0281/0381 0282/0382		Read TV interrupt enable. Expect reply.
0285/0385		Verify that interrupt enable register contains EF9F.
0281/0381 0282/0382 0285/0385 0286/0386		Clock/instruction step a load interrupt disable instruction (use 0000, EF9F, 4515, AA8A). Check repeat condition stop/jump bit. Do for four values.

3. Section 4 and 5 - Jump Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCBR	Condition 0 - relative jump
0401/0501 0402/0502 0405/0505	JRI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0401/0501 0402/0502 0405/0505		Load interrupt enable register with EE8F. Read TV interrupt enable. Expect EE8F.
0401/0501 0402/0502 0406/0506		Load and unload P register. Expect reply.
0401/0501 0402/0502 0405/0505 0406/0506	JRI020	Clock/instruction step a relative jump instruction (use 0AAA, 0555). Check repeat condition stop/jump bit. Do for two jump addresses.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	J1I000	Condition 1 - indirect jump (one word)
0411/0511	J1K010	Reset. Expect reply.
0412/0512		
0415/0515		Read TV interrupt enable. Expect 0000.
0411/0511		Load interrupt enable register with EE8F.
0412/0512		Expect reply.
0415/0515		Read TV interrupt enable. Expect EE8F.
0411/0511		Load and unload P register. Expect reply.
0412/0512		
0416/0516		
0411/0511		Load and unload DATUM register (address of
0412/0512		start of section). Expect reply.
0416/0516		
0411/0511	J1I020	Clock/instruction step a one-word indirect jump
0412/0512		instruction (use indirect addresses AAAA, 5555).
0415/0515		
0416/0516		Check repeat condition stop/jump bit.
		Do for two indirect addresses.
	J1I000	Condition 2 - indirect jump (two-word)
0421/0521	J2I010	Reset. Expect reply.
0422/0522		
0425/0525		Read TV interrupt enable. Expect 0000.
0421/0521		Load interrupt enable register with EE8F.
0422/0522		Expect reply.
0425/0525		Read TV interrupt enable. Expect EE8F.
0421/0521		Load and unload P register. Expect reply.
0422/0522		
0426/0526		
0421/0521		Load and unload DATUM register (address of
0422/0522		start of section). Expect reply.
0426/0526		
0421/0521	J2I020	Clock/instruction step a two-word indirect jump
0422/0522		instruction (use indirect addresses AAAA, 5555).
0425/0525		
0426/0526		Check repeat condition stop/jump bit.
		Do for two indirect addresses.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	XRI000	Condition 3 - relative subroutine exit
0431/0531 0432/0532 0435/0535	XRI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0431/0531 0432/0532 0435/0535		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0431/0531 0432/0532 0436/0536		Load and unload P register. Expect reply.
0431/0531 0432/0532 0436/0536		Load and unload DATUM register (address of start of section). Expect reply.
0431/0531 0432/0532 0435/0535 0436/0536	XRI020	Clock/instruction step a relative subroutine exit instruction (use link addresses 2AAA, 5555). Check repeat condition stop/jump bit. Do for two direct addresses.
	X1I000	Condition 4 - indirect subroutine exit (one word)
0441/0541 0442/0542 0445/0545	X1I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0441/0541 0442/0542 0445/0545		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0441/0541 0442/0542 0446/0546		Load and unload P register. Expect reply.
0441/0541 0442/0542 0446/0546		Load and unload DATUM register (address of start of section). Expect reply.
0441/0541 0442/0542 0445/0545 0446/0546		Clock/instruction step a one-word indirect subroutine exit instruction (use link addresses 2AAA, 5555). Check repeat condition stop/jump bit. Do for two link addresses.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	X2I000	Condition 5 - indirect subroutine exit (two word)
0451/0551 0452/0552 0455/0555	X2I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0451/0551 0452/0552 0455/0555		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0451/0551 0452/0552 0456/0556		Load and unload P register. Expect reply.
0451/0551 0452/0552 0456/0556		Load and unload DATUM register (address of start of section). Expect reply.
0451/0551 0452/0552 0455/0555 0456/0556	X2I020	Clock/instruction step a two-word indirect subroutine exit instruction (use link addresses 2AAA and 5555). Check repeat condition stop/jump bit. Do for two link addresses.
	D1I000	Condition 6 - direct subroutine (one-word)
0461/0561 0462/0562 0465/0565	D1I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0461/0561 0462/0562 0465/0565		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0461/0561 0462/0562 0466/0566		Load and unload P register. Expect reply.
0461/0561 0462/0562 0466/0566		Load and unload DATUM register (address of start of section). Expect reply.
0461/0561 0462/0562 0465/0565		Load Write Limits register so that the location to be written by the direct subroutine entry instruction is within limits. Set all protect bits within the write limits except the location to be written by the direct subroutine.
0461/0561 0462/0562 0465/0565 0466/0566	D1I020	Clock/instruction step a one-word direct subroutine entry instruction.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0467/0567	D1I021	Verify that the core location written by the subroutine entry instruction contains the correct link address. Check repeat condition stop/jump bit.
	D2I000	Condition 7 - direct subroutine entry (two-word)
0471/0571 0472/0572 0475/0575	D2I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0471/0571 0472/0572 0475/0575		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0471/0571 0472/0572 0476/0576		Load and unload P register. Expect reply.
0471/0571 0472/0572 0476/0576		Load and unload DATUM register (address of start of section). Expect reply.
0471/0571 0472/0572 0475/0575		Load Write Limits register so that the location to be written by the direct subroutine entry instruction is within limits. Set all protect bits within the write limits except the location to be written by the direct subroutine entry.
0471/0571 0472/0572 0475/0575 0476/0576	D2I020	Clock/instruction step a two-word direct subroutine entry instruction.
0477/0577	D2T021	Verify that the core location written by the subroutine entry instruction contains the correct link address. Check repeat conditions stop/jump bit.
	I1I000	Condition 8 - indirect subroutine entry (one-word)
0481/0581 0482/0582 0485/0585	I1I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0481/0581 0482/0582 0485/0585		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0481/0581 0482/0582 0486/0586		Load and unload P register. Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0481/0581 0482/0582 0486/0586		Load and unload DATUM register (address of start of section). Expect reply.
0481/0581 0482/0582 0485/0585		Load Write Limits register so that the location to be written by the indirect subroutine entry instruction is within limits. Set all protect bits within the write limits except the location to be written by the indirect subroutine entry.
0481/0581 0482/0582 0485/0585 0486/0586	I1I020	Clock/instruction step a one-word indirect subroutine entry instruction.
0487/0587	I1I021	Verify that the core location written by the subroutine entry instruction contains the correct link address. Check repeat condition stop/jump bit.
	I2I000	Condition 9 - indirect subroutine entry (two-word)
0491/0591 0492/0592 0495/0595	I2I010	Reset. Expect reply. Read TV interrupt enable. Expect reply.
0491/0591 0492/0592 0495/0595		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0491/0591 0492/0592 0496/0596		Load and unload P register. Expect reply.
0491/0591 0492/0592 0496/0596		Load and unload DATUM register (address of start of section). Expect reply.
0491/0591 0492/0592 0495/0595		Load Write Limits register so that the location to be written by the indirect subroutine entry instruction is within limits. Set all protect bits within the write limits except the location to be written by the indirect subroutine entry.
0491/0591 0492/0592 0495/0595 0496/0596	I2I020	Clock/instruction step a two-word indirect subroutine entry instruction.
0497/0597	I2I021	Verify that the core location written by the subroutine entry instruction contains the correct link address. Check repeat condition stop/jump bit.

4. Section 6 and 7 - Parameter Word Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCPW	Condition 0 - parameter word 1 - set intensity
0601/0701 0602/0702 0605/0705	I4I010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0601/0701 0602/0702 0605/0705		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0601/0701 0602/0702 0606/0706		Load and unload P register. Reply.
0601/0701 0602/0702 0605/0705 0606/0706	I4I020	Clock/instruction step a parameter word 1 instruction (use absolute intensity of F, 0...E). Check repeat condition stop/jump bit. Do for each absolute intensity value.
	PXI000	Condition 1 - parameter word 1 - change zoom ability
0611/0711 0612/0712 0615/0715	PZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0611/0711 0612/0712 0615/0715		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0611/0711 0612/0712 0616/0716		Load and unload P register. Expect reply.
0611/0711 0612/0712 0615/0715	PXI020	Clock/instruction step a parameter word 1 instruction (use zoomable and nonzoomable). Check repeat condition stop/jump bit. Do for zoomable and nonzoomable.
	BWI000	Condition 2 - 11/12-bit window
0621/0721 0622/0722 0625/0725	BWI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0621/0721 0622/0722 0625/0725		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0621/0721 0622/0722 0626/0726		Load and unload P register. Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0621/0721 0622/0722 0625/0725 0626/0726	BWI020	Clock/instruction step a parameter word 2 instruction (select 12-bit window).
0621/0721 0622/0722 0625/0725 0626/0726	BWI030	Clock/instruction step a parameter word 2 instruction (select 11-bit window).
		Check repeat condition stop/jump bit. Do two times.
	PII000	Condition 3 - program interrupt
0631/0731 0632/0732 0635/0735	PII010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0631/0731 0632/0732 0635/0735		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0631/0731 0632/0732 0636/0736		Load and unload P register. Expect reply.
0631/0731 0632/0732 0635/0735 0636/0736 0639/0739 063A/073A 063C/073C 063D/073D 063E/073E	PII020	Clock/instruction step a parameter word 2 instruction (program interrupt).
063B/073B		Verify that program interrupt occurred. Check repeat condition stop/jump bit. Do two times.

5. Section 8 and 9 - Move Beam Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCMB	Condition 0 - absolute beam movement (nonzoomable)
0801/0901 0802/0902 0805/0905	BNI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0801/0901 0802/0902 0805/0905		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0801/0901 0802/0902 0806/0906		Load and unload P register. Expect reply.
0801/0901 0802/0902 0806/0906		Load and unload window location X with 7FFF. Expect reply.
0801/0901 0802/0902 0806/0906		Load and unload window location Y with 7FFF. Expect reply.
0801/0901 0802/0902 0805/0905		Load zoom level register with 7. Expect reply. Read TV zoom level. Expect reply.
0801/0901 0802/0902 0805/0905 0806/0906	BNI016	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0801/0901 0802/0902 0805/0905 0806/0906	BNI020	Clock/instruction step an absolute beam movement instruction (use positions AAAA, 5555, AAAA, 5555, and 1 random position for both X and Y). Check repeat condition stop/jump bit. Do for each of the five sets of operands.
	BZI000	Condition 1 - absolute beam movement (zoomable)
0811/0911 0812/0912 0815/0915	BZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0811/0911 0812/0912 0815/0915		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0811/0911 0812/0912 0816/0916		Load and unload P register. Expect reply.
0811/0911 0812/0912 0816/0916		Load and unload window location X and Y (use locations FFFF, 0000, 0000, FFFF, AAAA, 5555, 5555, AAAA, and 1 random location for both X and Y).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0811/0911 0812/0912 0815/0915		Load zoom level register with a random zoom level. Expect reply. Read TV zoom level. Expect reply.
0811/0911 0812/0912 0815/0915 0816/0916	BZI016	Clock/instruction step a parameter word 1 instruction (enable zoomability).
0811/0911 0812/0912 0815/0915 0816/0916	BZI020	Clock/instruction step an absolute beam movement instruction (use positions FFFF, 0000, FFFF, 0000, AAAA, 5555, AAAA, 5555, and 1 random position for both X and Y). Check repeat condition stop/jump bit. Do for each of the nine sets of operands.
	RZI000	Condition 2 - negative relative beam movement
0821/0921 0822/0922 0825/0925	RZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0821/0921 0822/0922 0825/0925		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect reply.
0821/0921 0822/0922 0826/0926		Load and unload P register. Expect reply.
0821/0921 0822/0922 0825/0925 0826/0926	RZI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0821/0921 0822/0922 0825/0925 0826/0926	RZI016	Clock/instruction step an absolute beam movement instruction (use position 0000 for both X and Y).
0821/0921 0822/0922 0825/0925 0826/0926	RZI020	Clock/instruction step a negative relative beam movement instruction (use deltas AAAA and 5555 for both X and Y). Check repeat condition stop/jump bit. Do for each of the two operands.
	XZI000	Condition 3 - move beam delta X
0831/0931 0832/0932 0835/0935	XZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0831/0931 0832/0932 0835/0935		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0831/0931 0832/0932 0836/0936		Load and unload P register. Expect reply.
0831/0931 0832/0932 0835/0935 0836/0936	XZI016	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0831/0931 0832/0932 0835/0935 0836/0936	XZI018	Clock/instruction step an absolute beam movement instruction (use positions FFFF, 0000, FFFF, 0000, AAAA, 5555, AAAA, 5555, and 1 random position for both X and Y).
0831/0931 0832/0932 0835/0935 0836/0936	XZI020	Clock/instruction step a move beam delta X instruction (use deltas FFFF, 0000, 0000, FFFF, FAAA, 0555, 0555, FAAA, and 1 random delta for X).
		Check repeat condition stop/jump bit. Do for each of the nine sets of operands.
	YZI000	Condition 4 - move beam delta Y
0841/0941 0842/0942 0845/0945	YZI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0841/0941 0842/0942 0845/0945		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0841/0941 0842/0942 0846/0946		Load and unload P register. Expect reply.
0841/0941 0842/0942 0845/0945 0846/0946	YZI016	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0841/0941 0842/0942 0845/0945 0846/0946	YZI018	Clock/instruction step an absolute beam movement instruction (use positions FFFF, 0000, FFFF, 0000, AAAA, 5555, AAAA, 5555, and 1 random position for X and Y).
0841/0941 0842/0942 0845/0945 0846/0946	YZI020	Clock/instruction step a move beam delta Y instruction (use deltas FFFF, 0000, 0000, FFFF, FAAA, 0555, 0555, FAAA, and 1 random delta for Y).
		Check repeat condition stop/jump bit. Do for each of the nine sets of operands.

6. Section A and B - Conditional Control Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCCC	Condition 0 - jump on zoom level (true)
0A01/0B01 0A02/0B02 0A05/0B05	ZTI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A01/0B01 0A02/0B02 0A05/0B05		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A01/0B01 0A02/0B02 0A06/0B06		Load and unload P register. Expect reply.
0A01/0B01 0A02/0B02 0A05/0B05		Load zoom level register with 7. Expect reply. Read TV zoom level. Expect reply.
0A01/0B01 0A02/0B02 0A05/0B05 0A06/0B06		Instruction step a parameter word 1 instruction (enable zoomability).
0A01/0B01 0A02/0B02 0A05/0B05 0A06/0B06	ZTI020	Clock/instruction step a conditional control instruction (jump over 1 word if the zoom level is equal to or greater than the operand - use operands 7, 06) expect jump. Check repeat condition stop/jump bit. Do for each zoom level as operand.
	ZFI000	Condition 1 - jump on zoom level (false)
0A11/0B11 0A12/0B12 0A15/0B15	ZFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A11/0B11 0A12/0B12 0A15/0B15		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A11/0B11 0A12/0B12 0A16/0B16		Load and unload P register. Expect reply.
0A11/0B11 0A12/0B12 0A15/0B15 0A16/0B16		Instruction step a parameter word 1 instruction (enable zoomability).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0A11/0B11 0A12/0B12 0A15/0B15 0A16/0B16	ZFI020	Clock/instruction step a conditional control instruction (jump to start of item if the zoom level is equal to or greater than the operand, use operands 7-1). Expect no jump (zoom level equal 0 from reset). Check repeat condition stop/jump bit. Do for zoom levels 7-6 as operands.
	CTI000	Condition 2 - jump on CCR (true)
0A21/0B21 0A22/0B22 0A25/0B25	CTI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A21/0B21 0A22/0B22 0A25/0B25		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A21/0B21 0A22/0B22 0A26/0B26		Load and unload P register. Expect reply.
0A21/0B21 0A22/0B22 0A26/0B26	CTI016	Load and unload condition control register with a single one bit (use 8000, 0001....4000). Expect reply.
0A21/0B21 0A22/0B22 0A25/0B25 0A26/0B26	CTI020	Clock/instruction step a conditional control instruction (jump to end of item if the designated CCR bit is not set. Use operands F, 0....E). Expect no jump. Check repeat condition stop/jump bit. Do for each bit position in conditional control register.
	CFI000	Condition 3 - jump on CCR (false)
0A31/0B31 0A32/0B32 0A35/0B35	CFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A31/0B31 0A32/0B32 0A35/0B35		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A31/0B31 0A32/0B32 0A36/0B36		Load and unload P register. Expect reply.
0A31/0B31 0A32/0B32 0A36/0B36		Load and unload conditional control register with all bits set except one (use 7FFF, FFFE...BFFF). Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0A31/0B31 0A32/0B32 0A35/0B35 0A36/0B36	CFI020	Clock/instruction step a conditional control instruction (jump over two words if the designated CCR bit is not set. Use operands F, O...E). Expect jump. Check repeat condition stop/jump bit. Do for each bit position in conditional control register.
	HFI000	Condition 4 - jump on light pen hit (false)
0A41/0B41 0A42/0B42 0A45/0B45	HFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A41/0B41 0A42/0B42 0A45/0B45		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A41/0B41 0A42/0B42 0A46/0B46		Load and unload P register. Expect reply.
0A41/0B41 0A42/0B42 0A45/0B45 0A46/0B46	HFI020	Clock/instruction step a conditional control instruction (jump over 2 words if a light pen occurred). Expect no jump. Check repeat condition stop/jump bit. Do two times.
	SFI010	Condition 5 - jump on light pen switch (false)
0A51/0B51 0A52/0B52 0A55/0B55	SFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A51/0B51 0A52/0B52 0A55/0B55		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A51/0B51 0A52/0B52 0A56/0B56		Load and unload P register. Expect reply.
0A51/0B51 0A52/0B52 0A55/0B55 0A56/0B56	SFI020	Clock/instruction step a conditional control instruction (jump over 1 word if the light pen switch is not set). Expect jump. Check repeat condition stop/jump bit. Do two times.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	ETI000	Condition 6 - jump if outside 11-bit window (true)
0A61/0B61 0A62/0B62 0A65/0B65	ETI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A61/0B61 0A62/0B62 0A65/0B65		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A61/0B61 0A62/0B62 0A66/0B66		Load and unload P register. Expect reply.
0A61/0B61 0A62/0B62 0A65/0B65 0A66/0B66	ETI017	Instruction step a parameter word 1 instruction (disable zoomability).
0A61/0B61 0A62/0B62 0A65/0B65 0A66/0B66		Instruction step an absolute beam movement instruction with a shifting single bit set in the positions (use 0400....8000 first in X position and then in Y position).
0A61/0B61 0A62/0B62 0A65/0B65 0A66/0B66	ETI020	Clock/instruction step a conditional control instruction (jump over two words if the beam is not inside the 11-bit window). Expect jump. Check repeat condition stop/jump bit. Do for each single bit position outside the 11-bit window in X and then in Y position.
	EFI000	Condition 7 - jump if outside 11-bit window (false)
0A71/0B71 0A72/0B72 0A75/0B75	EFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A71/0B71 0A72/0B72 0A75/0B75		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A71/0B71 0A72/0B72 0A76/0B76		Load and unload P register. Expect reply.
0A71/0B71 0A72/0B72 0A75/0B75 0A76/0B76		Instruction step a parameter word 1 instruction (disable zoomability).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0A71/0B71 0A72/0B72 0A75/0B75 0A76/0B76		Instruction step an absolute beam movement instruction (X and Y positions 0000).
0A71/0B71 0A72/0B72 0A75/0B75 0A76/0B76	EFI020	Clock/instruction step a conditional control instruction (jump to end of item if the beam is not inside the 11-bit window). Expect no jump. Check repeat condition stop/jump bit. Do two times.
	TTI000	Condition 8 - jump if outside 12-bit window (true)
0A81/0B81 0A82/0B82 0A85/0B85	TTI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A81/0B81 0A82/0B82 0A85/0B85		Load interrupt enable with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0A81/0B81 0A82/0B82 0A86/0B86		Load and unload P register. Expect reply.
0A81/0B81 0A82/0B82 0A85/0B85 0A86/0B86	ETI017	Instruction step a parameter word 1 instruction (disable zoomability).
0A81/0B81 0A82/0B82 0A85/0B85 0A86/0B86		Instruction step an absolute beam movement instruction with a shifting single bit set in the positions (use 0800...8000 first in X position and then in Y position).
0A81/0B81 0A82/0B82 0A85/0B85 0A86/0B86	ETI020	Clock/instruction step a conditional control instruction (jump over two words if the beam is not inside the 12-bit window). Expect jump. Check repeat condition stop/jump bit. Do for each single bit position outside the 12-bit window in X and then in Y position.
	TFI000	Condition 9 - jump if outside 12-bit window (false)
0A91/0B91 0A92/0B92 0A95/0B95	TFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0A91/0B91 0A92/0B92 0A95/0B95		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0A91/0B91 0A92/0B92 0A96/0B96		Load and unload P register. Expect reply.
0A91/0B91 0A92/0B92 0A96/0B96		Load and unload control word address register with the address of a control word instruction. Expect reply.
0A91/0B91 0A92/0B92 0A95/0B95 0A96/0B96		Instruction step a parameter word 1 instruction (disable zoomability).
0A91/0B91 0A92/0B92 0A95/0B95 0A96/0B96		Instruction step an absolute beam movement instruction (X and Y positions 0).
0A91/0B91 0A92/0B92 0A95/0B95 0A96/0B96	TFI020	Clock/instruction step a conditional control instruction (jump to end of item if beam is inside 12-bit window). Expect jump. Check repeat condition stop/jump bit. Do two times.
	YTI000	Condition A - cyclic jump (true)
0AA1/0BA1 0AA2/0BA2 0AA5/0BA5	YTI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0AA1/0BA1 0AA2/0BA2 0AA5/0BA5		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0AA1/0BA1 0AA2/0BA2 0AA6/0BA6		Load and unload P register. Expect reply.
0AA1/0BA1 0AA2/0BA2 0AA6/0BA6		Load and unload control word address register with the address of a control word instruction. Expect reply.
0AA1/0BA1 0AA2/0BA2 0AA5/0BA5		Load write limits register so that the location to be written by the conditional control instruction is within limits. Set all protect bits within the write limits except the location to be written by the conditional control instruction.
0AA1/0BA1 0AA2/0BA2 0AA5/0BA5 0AA6/0BA6	YTI020	Clock/instruction step a conditional control instruction (jump to start of item if the operand is equal to count. Use operands 1-F with counts O-E). Expect jump.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0AA7/0BA7		Verify that the core location written by the conditional control instruction contains 0000. Check repeat condition stop/jump bit. Do for operands 1-F with counts O-E.
	YFI000	Condition B - cyclic jump (false)
0AB1/0BB1 0AB2/0BB2 0AB5/0BB5	YFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0AB1/0BB1 0AB2/0BB2 0AB5/0BB5		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0AB1/0BB1 0AB2/0BB2 0AB6/0BB6		Load and unload P register. Expect reply.
0AB1/0BB1 0AB2/0BB2 0AB5/0BB5		Load write limits register so that the location to be written by the conditional control instruction is within limits. Set all protect bits within the write limits except the location to be written by the conditional control instruction.
0AB1/0BB1 0AB2/0BB2 0AB5/0BB5 0AB6/0BB6	YFI020	Clock/instruction step a conditional control instruction (jump over one word if the operand is equal to the count). Use operands E, E, O-D with counts F, O, 1-E. Expect no jump.
0AB7/0BB7		Verify that the core location written by the conditional control instruction contains the starting count incremented by one. Check repeat condition stop/jump bit. Do for operands E, E, O-D with counts F, O, 1-E.

7. Section C and D - Draw Vector Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCDV	Condition 0 - draw vector X (from off window to on window)
0C01/0D01 0C02/0D02 0C05/0D05	AXI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.

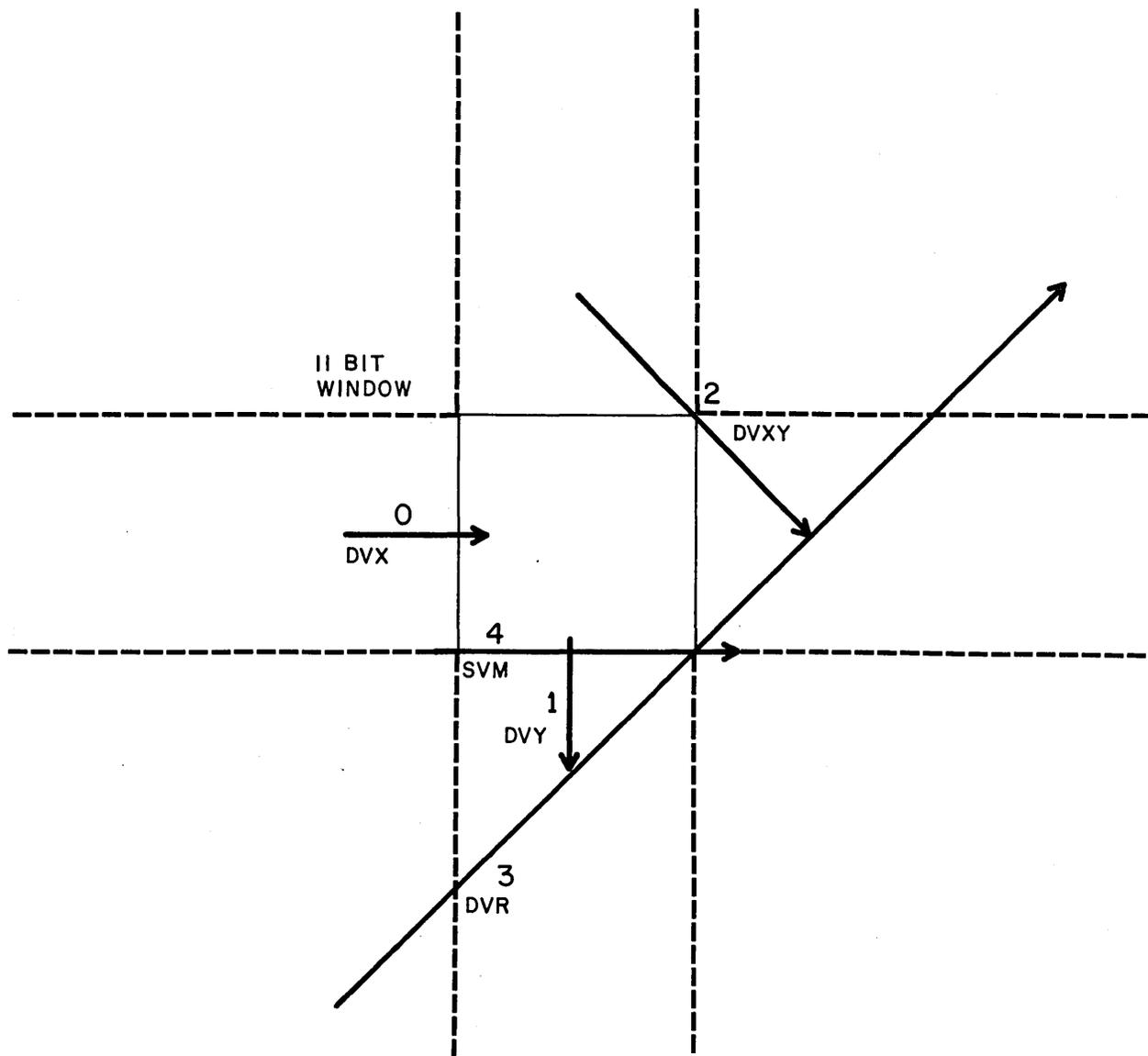
<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0C01/0D01 0C02/0D02 0C05/0D05		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0C01/0D01 0C02/0D02 0C06/0D06		Load and unload P register. Expect reply.
0C01/0D01 0C02/0D02 0C05/0D05 0C06/0D06	AXI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0C01/0D01 0C02/0D02 0C05/0D05 0C06/0D06	AXI016	Clock/instruction step an absolute beam movement instruction (use position FA00 for X and 0000 for Y).
0C01/0D01 0C02/0D02 0C05/0D05 0C06/0D06	AXI020	Clock/instruction step a draw vector X instruction (use delta X of 0240_{16}).
		Check repeat condition stop/jump bit. Repeat five times.
	AYI000	Condition 1 - draw vector Y (from on window to off window)
0C11/0D11 0C12/0D12 0C15/0D15	AYI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0C11/0D11 0C12/0D12 0C15/0D15		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect reply.
0C11/0D11 0C12/0D12 0C16/0D16		Load and unload P register. Expect reply.
0C11/0D11 0C12/0D12 0C15/0D15 0C16/0D16	AYI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0C11/0D11 0C12/0D12 0C15/0D15 0C16/0D16	AYI016	Clock/instruction step an absolute beam movement instruction (use position 0000 for X and FC40 for Y).
0C11/0D11 0C12/0D12 0C15/0D15 0C16/0D16	AYI020	Clock/instruction step a draw vector Y instruction (use delta Y of FDBF).
		Check repeat condition stop/jump bit. Repeat five times.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	ABI000	Condition 2 - draw vector XY (from off Y window to off X window)
0C21/0D21 0C22/0D22 0C25/0D25	ABI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0C21/0D21 0C22/0D22 0C25/0D25		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0C21/0D21 0C22/0D22 0C26/0D26		Load and unload P register. Expect reply.
0C21/0D21 0C22/0D22 0C25/0D25 0C26/0D26	ABI016	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0C21/0D21 0C22/0D22 0C25/0D25 0C26/0D26	ABI018	Clock/instruction step an absolute beam movement instruction (use position 0000 for X and 07FE for Y).
0C21/0D21 0C22/0D22 0C25/0D25 0C26/0D26	ABI020	Clock/instruction step a draw vector XY instruction (use delta X of 07FE and delta Y of F801). Check repeat condition stop/jump bit. Repeat five times.
	ARI000	Condition 3 - relative vector (from off X and Y windows, across X and Y window limits, to off X and Y windows)
0C31/0D31 0C32/0D32 0C35/0D35	ARI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0C31/0D31 0C32/0D32 0C35/0D35		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0C31/0D31 0C32/0D32 0C36/0D36		Load and unload P register. Expect reply.
0C31/0D31 0C32/0D32 0C35/0D35 0C36/0D36	ARI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0C31/0D31 0C32/0D32 0C35/0D35 0C36/0D36	ARI016	Clock/instruction step an absolute beam movement instruction (use position F801 for X and F003 for Y).
0C31/0D31 0C32/0D32 0C35/0D35 0C36/0D36	ARI020	Clock/instruction step a relative vector instruction (use a delta X of 17FA and a delta Y of 17FA). Check repeat condition stop/jump bit. Repeat five times.
	ASI000	Condition 4 - short vector mode (from off X window, across entire X window, to off X window)
0C41/0D41 0C42/0D42 0C45/0D45	ASI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0C41/0D41 0C42/0D42 0C45/0D45		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0C41/0D41 0C42/0D42 0C46/0D46		Load and unload P register. Expect reply.
0C41/0D41 0C42/0D42 0C45/0D45 0C46/0D46	ASI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
0C41/0D41 0C42/0D42 0C45/0D45 0C46/0D46	ASI016	Clock/instruction step an absolute beam movement instruction (use position FBC0 for X and FC00 for Y).
0C41/0D41 0C42/0D42 0C45/0D45 0C46/0D46	ASI020	Clock/instruction step a short vector mode instruction (use a scale factor of 7 with a delta X of 0011 ₁₆ and a delta Y of 0000). Check for repeat condition stop/jump bit. Repeat five times.

8. Section E and F - Control Word Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCCW	Condition 0 - no skip, no automatic scissoring to window enabled



VECTORS DRAWN IN CONDITIONS
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<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0E01/0F01 0E02/0F02 0E05/0F05	SAI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0E01/0F01 0E02/0F02 0E05/0F05		Load interrupt enable register with EE870. Expect reply. Read TV interrupt enable. Expect EE87.
0E01/0F01 0E02/0F02 0E06/0F06		Load and unload P register. Expect reply.
0E01/0F01 0E02/0F02 0E05/0F05 0E06/0F06	SAI020	Clock/instruction step a control word instruction (S and W bits set). Expect not draw item and not skip item. Check repeat condition stop/jump bit. Do two times.
	SMI000	Condition 1 - no skip, no S/W bit
0E11/0F11 0E12/0F12 0E15/0F15	SBI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0E11/0F11 0E12/0F12 0E15/0F15		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0E11/0F11 0E12/0F12 0E16/0F16		Load and unload P register. Expect reply.
0E11/0F11 0E12/0F12 0E15/0F15 0E16/0F16	SBI020	Clock/instruction step a control word instruction (use S bit not set/W bit set and S bit set/W bit not set). Expect not draw item and not skip item. Check repeat condition stop/jump bit. Do for S bit not set/W bit set and S bit set/W bit not set.
	SCI000	Condition 2 - skip
0E21/0F21 0E22/0F22 0E25/0F25	SCI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0E21/0F21 0E22/0F22 0E25/0F25		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0E21/0F21 0E22/0F22 0E26/0F26		Load and unload P register. Expect reply.
0E21/0F21 0E22/0F22 0E26/0F26	SCI020	Clock/instruction step a control word instruction (S and W bits set). Expect not draw item and skip item. Check repeat condition stop/jump bit. Do two times.
	CNI000	Condition 3 - draw item, W clear/not correct
0E31/0F31 0E32/0F32 0E35/0F35	CNI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0E31/0F31 0E32/0F32 0E25/0F25		Load interrupt enable with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
0E31/0F31 0E32/0F32 0E36/0F36		Load and unload P register. Expect reply.
0E31/0F31 0E32/0F32 0E35/0F35 0E36/0F36	CNI020	Clock/instruction step a control word instruction (W bit not set and S bit set). Expect not draw item and not skip item. Load and unload P register with the address of the previously stepped control word instruction. Expect reply.
0E31/0F31 0E32/0F32 0E35/0F35		Load write limits register so that the location to be written by the control word instruction is within limits. Set all protect bits within the write limits except the location to be written by the control word instruction.
0E31/0F31 0E32/0F32 0E35/0F35 0E36/0F36	CNI030	Clock/instruction step the same control word instruction previously stepped (W bit not set and S bit set). Expect draw item and W bit clear/not correct (store bit 15 into control word).
0E31/0F31 0E32/0F32 0E35/0F35 0E36/0F36	CNI040	Clock/instruction step the rest of the control word instruction. P decremented during draw item (W bit now set and S bit set). Expect not draw item and skip item.
0E37/0F37		Verify that the W bit is set in the control word instruction. Check repeat condition stop/jump bit. Do two times.

9. Section 10 and 11 - Character Mode Instructions

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCCM	Condition 0 - character mode fixed spacing
1001/1101	SHI010	Reset. Expect reply.
1002/1102		
1005/1105		Read TV interrupt enable. Expect 0000.
1001/1101		Load interrupt enable register with EE8F.
1002/1102		Expect reply.
1005/1105		Read TV interrupt enable. Expect EE8F.
1001/1101		Load and unload P register. Expect reply.
1002/1102		
1006/1106		
1001/1101	SHI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
1002/1102		
1005/1105		
1006/1106		
1001/1101	SHI016	Clock/instruction step an absolute beam movement instruction (use position F800 for X and 07FF for Y).
1002/1102		
1005/1105		
1006/1106		
1001/1101	SHI020	Clock/instruction step a character mode fixed spacing instruction (an exit symbol and one other character is used at sizes A and B alternately).
1002/1102		
1005/1105		
1006/1106		
		Check repeat condition stop/jump bit. Repeat, in reverse order, for all characters between ASCII code 20 ₁₆ and 7E ₁₆ .
	SZI000	Condition 1 - character mode variable spacing
1011/1111	SZI010	Reset. Expect reply.
1012/1112		
1015/1115		Read TV interrupt enable. Expect 0000.
1011/1111		Load interrupt enable register with EE8F.
1012/1112		Expect reply.
1015/1115		Read TV interrupt enable. Expect EE8F.
1011/1111		Load and unload P register.
1012/1112		Expect reply.
1016/1116		
1011/1111	SZI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
1012/1112		
1015/1115		
1016/1116		

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
1011/1111 1012/1112 1015/1115 1016/1116	SZI016	Clock/instruction step an absolute beam movement instruction (use position F800 for X and 07FF for Y).
1011/1111 1012/1112 1015/1115 1016/1116	SZI020	Clock/instruction step a character mode variable spacing instruction (an exit symbol and two other characters are used at size A with spacing 0F on X and F0 on Y). Check repeat condition stop/jump bit. Repeat, in reverse order, for all character pairs between ASCII codes A0B0 and AFBF.
	LRI010	Condition 2 - enter plot character mode
1021/1121 1022/1122 1025/1125	LRI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
1021/1121 1022/1122 1025/1125		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
1021/1121 1022/1122 1026/1126		Load and unload P register. Expect reply.
1021/1121 1022/1122 1025/1125 1026/1126	ERI014	Clock/instruction step a parameter word 1 instruction (disable zoomability).
1021/1121 1022/1122 1025/1125 1026/1126	LRI016	Clock/instruction step an absolute beam movement instruction (use position F800 for X and 07FF for Y).
1021/1121 1022/1122 1025/1125 1026/1126	LRI020	Clock/instruction step an enter plot character mode instruction (a backspace symbol at size A is used). Check repeat condition stop/jump bit.

10. Section 12 and 13 - Execute Instruction

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCEXC	Condition 0 - execute control word
1201/1301 1202/1302 1205/1305	CWI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
1201/1301 1202/1302 1205/1305		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
1201/1301 1202/1302 1206/1306		Load and unload P register. Expect reply.
1201/1301 1202/1302 1206/1306	CWI014	Load and unload DATUM register (address of start of section). Expect reply.
1201/1301 1202/1302 1205/1305 1206/1306	CWI020	Clock/instruction step an execute instruction (indirect address points to a control word instruction).
1201/1301 1202/1302 1205/1305 1206/1306	CWI030	Clock/instruction step a control word instruction in execute mode. Expect immediate exit.
		Check repeat condition stop/jump bit.

11. Section 15 - Start/Stop

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	CYCRUN	Condition 0 - start/reset
1501 1502 1505	ESI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
1501 1502 1505		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
1501 1502 1506		Load and unload P register (address of a load P register instruction - loading its own address). Expect reply.
1501 1502		Start DCI at address in P register. Expect reply.
1503 1504		Attempt to load one scratchpad register (use registers 0F - 01). Expect external reject.
1503 1504		Attempt to unload one scratchpad register (use registers 0F-01). Expect external reject.
1501 1502	ESI020	Reset. Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
1501 1502	ESI030	Unload one scratchpad register (use registers 0F-01). Expect reply. Check repeat condition stop/jump bit. Do for scratch register 0F-01.
	INI000	Condition 1 - start/finish
1511 1512 1515	INI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
1511 1512 1515		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
1511 1512 1516		Load and unload P register (address of a load P instruction, loading its own address). Expect reply.
1511 1512		Start DCI at address in P register. Expect reply.
1513 1514		Attempt to load interrupt enable register. Expect external reject.
1513 1514		Attempt to load interrupt disable register. Expect external reject.
1511 1512		Finish current instruction and stop. Expect reply.
1511 1512		Load interrupt enable register with EE8F. Expect reply. Check repeat condition stop/jump bit. Do two times.
	OFI000	Condition 2 - Start/end of frame interrupt
1521 1522 1525	OFI010	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
1521 1522 1525		Load interrupt enable register with EE8F. Expect reply. Read TV interrupt enable. Expect EE8F.
1521 1522 1526		Load and unload P register (address of display file containing an end of frame instruction and a load P register instruction, loading its own address). Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
1521		Start DCI at address in P register.
1522		Expect reply.
1528	OFI020	Verify that the end of frame interrupt occurs in 19-21 milliseconds. No interrupt time error (type 8) will occur if the interrupt is timed to be less than 19 milliseconds and this test is being multiplexed.
1529		
152A		
152C		
152D		
152E		
152B		Report missing interrupt if end of frame interrupt has not occurred after waiting 100 milliseconds.
1521		Load zoom level register. Expect reply.
1522		
		Check repeat condition stop/jump bit. Do for each method of clearing the interrupt (re-enable, disable, and reset).
	RGI000	Condition 3 - start/program interrupt
1531	RGI010	Reset. Expect reply.
1532		
1535		Read TV interrupt enable. Expect 0000.
1531		Load interrupt enable register with EE8F.
1532		Expect reply.
1535		Read TV interrupt enable. Expect EE8F.
1531		Load and unload P register (address of a display file containing a program interrupt instruction and load P register instruction, loading its own address). Expect reply.
1532		
1536		
1531		Start DCI at address in P register.
1532		Expect reply and program interrupt.
1539		
153A		
153C		
153D		
153E		
153B		Verify that the program interrupt occurred.
1531		Load write limits register. Expect reply.
1532		
		Check repeat condition stop/jump bit. Do for each method of clearing the interrupt (re-enable, disable, and reset).

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	L1I000	Condition 4 - start/program failure 1 interrupt (write limits)
1541	L1I010	Reset. Expect reply.
1542		
1545		Read TV interrupt enable. Expect 0000.
1541		Load interrupt enable register EE8F.
1542		Expect reply.
1545		Read TV interrupt enable. Expect EE8F.
1541		Load and unload P register (address of a display file containing an unload P register and a load P register instruction). Expect reply.
1542		
1546		
1541	L1I030	Load write limits register (use limits above/below the location to be written by the unload P register instruction). Expect reply. Clear the protect bit for the location to be written by the unload P register instruction.
1542		
1545		
1541		Start DCI at address in P register. Expect reply and program failure 1 interrupt (attempted write outside write limits).
1542		
1549		
154A		
154C		
154D		
154E		
154B		Verify that program failure 1 interrupt occurred.
1547		Verify that the location of the attempted write remained unchanged.
1541		Load write limits register. Expect reply.
1542		
1545		
		Check repeat condition stop/jump bit. Do two times.
	B1I000	Condition 5 - Start/program failure 1 interrupt (protect bit)
1551	B1I010	Reset. Expect reply.
1552		
1555		Read TV interrupt enable. Expect 0000.
1551		Load interrupt enable register with EE8F.
1552		Expect reply.
1555		Read TV interrupt enable. Expect EE8F.
1551		Load and unload P register (address of a display file containing an unload P register instruction and a load P register instruction, loading its own address). Expect reply.
1552		
1556		

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
1551 1552 1555		Load write limits register so that the location to be written by the unload P register instruction is within limits. Expect reply. Set the protect bit for the location to be written by the unload P register instruction.
1551 1552 1559 155A 155C 155D 155E		Start DCI at address in P register. Expect reply and program failure 1 interrupt (attempted write into a protected location).
155B		Verify that the program failure 1 interrupt occurred.
1557		Verify that the location of the attempted write remained unchanged.
1551 1552		Unload all the unload only registers. Expect reply. Check repeat condition stop/jump bit. Do two times.
	TCI000	Condition 6 - real time clock interrupt
1561 1562 1565	TCI010	Reset. Expect reply. Read interrupt enable. Expect 0000.
1561 1562 1565		Load interrupt enable register with FF8F. Expect reply. Read TV interrupt enable. Expect FF8F.
1568 1569 156A 156C 156D 156E	TCI020	Verify that first real time clock interrupt occurs in 0-17 milliseconds if line frequency is 50 cycle. No interrupt time error (type 8) will occur if the interrupt is timed to be less than the lower limit and this test is being multiplexed.
156B		Report missing interrupt if the real time clock interrupt has not occurred after waiting 100 milliseconds.
1568 1569 156A 156C 156D 156E	TCI030	Verify that second real time clock interrupt occurs either in 16-17 milliseconds if line frequency is 60 cycle or in 19-21 milliseconds if line frequency is 50 cycle. No interrupt time error (type 8) will occur if the interrupt is timed to be less than the lower limit and this test is being multiplexed. This second interrupt is cleared with a reset.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
156B		Report missing interrupt if the real time clock interrupt has not occurred after waiting 100 milliseconds.
1561		Read TV interrupt enable. Expect 0000. Check repeat condition stop/jump bit. Do two times.
1562		
1565		

C. SUBPROGRAM DESCRIPTION

CKCORE

This subroutine compares one core location against a masked expected value.

Enter with: Q = Expected value
A = Mask
call +1 = Unbiased core address

Exit to: Marker if error type 7
Call +2 if no error

CMPALL

This subroutine compares actual DCI register contents against expected contents.

Enter with: A = First register number to compare
Q = Last register number +1

Exit to: Call +1 (if error type 5 or 6 occurs, the subroutine calling CMPALL will exit to marker)

Three table pairs are used by this subroutine. The first table of each pair is for the parameter registers; the second is for the TV monitor. The pairs are as follows: mask tables RMT000/TMT000, expected tables RXT000/TXT000, and actual tables RGT000/TVT000 or RGT100/TVT100. Pointer RAP000 alternately designates RGT000/TVT000 or RGT100/TVT100 as the current actual tables. Pointer RPP000 designates the previous actual tables. When a compare error occurs, this subroutine calls the error subroutine, but does not exit to marker. Instead, this subroutine stores the address of marker in the calling subroutine's return address and that subroutine will exit to marker. This operation allows all register compare errors to be reported before going to the forward or backward marker.

DCIPRO

This subroutine processes all DCI interrupts.

Enter and exit with: Q = Interrupt exit value

Exit to: Call +1 (if error types 9, A, C, D, or E occurs the error is flagged but cannot be reported until the monitor has exited interrupt state)

This subroutine unloads the interrupt status register to determine which interrupt occurred, flags the expected interrupts as being received for the RINT recognize interrupt subroutine, flags the interrupt as no longer expected, and clears the interrupt from the interrupt status register. If an error occurs in the interrupt processor, the error is flagged. Then the address of the marker routine is stored in the error routine return address and the address of the error routine +1 is stored in the interrupt return address. Thus, the next time this test gets control, the error will be reported and control will go to the forward or backward marker.

FNER

This subroutine attempts to output a function, but expects an external reject.

Enter with: Q = Equipment address and command

Exit to: Marker if error type 3 or 4
Call +1 if no error

FNRP

This subroutine outputs a function expecting a reply.

Enter with: Q = Equipment address and command
A = Data for load register operations

Exit to: Marker if error type 1 or 2 and not in interrupt state
Call +1 if no error
Call +2 if error type 1 or 2 during interrupt state

GETRCT

This subroutine fetches register change times and change table control words from a change table. A change table is used by STEPER stepping subroutine to predict parameter register and TV monitor contents during clock and instruction stepping. The change table format is as follows:

11WW	WSSS	SSSS	SSSS	Word control word
				S = Number of clock steps
				W = DCI instruction word number
				000 word 0
				001 word 1
				010 word 2
				100 line drawing

1000	0111	1111	1111	Table subroutine entry or exit
0AAA	AAAA	AAAA	AAAA	Unbiased address of the portion of table out of sequence or 0 to exit back to main table
1000	0CCC	CCCC	CCCC	Register change time (a register is expected to change at this time) C = clock pulse number of change
00MM	MMMM	ORRR	RRRR	TV register expected to change R = TV register number (40-5F) M = modifier code for TV register data
DDDD	DDDD	DDDD	DDDD	Unmodified expected contents of TV register
1111	0000	0000	0000	Instruction done 1 control word (signals the start of parameter register changes; STEPER starts here during instruction stepping)
00MM	MMMM	ORRR	RRRR	Parameter register expected to change R = parameter register number M = modifier code for parameter register data
DDDD	DDDD	DDDD	DDDD	Unmodified expected contents of parameter register
1111	1111	0000	0000	Instruction done 2 control words (signals the end of parameter register changes; STEPER exits here in clock step)
0AAA	AAAA	AAAA	AAAA	Unbiased address of start of change table for clock stepping (STEPPER uses this address to pick up TV changes after instruction step)
1111	1111	1111	1111	Terminate instruction step

RINT

This subroutine checks for a missing interrupt.

Enter with: Q = Bit in interrupt enable register corresponding to expected interrupt

Exit to: Marker if error type B
 Call +1 if no error

STEPPER

This subroutine clock steps and instruction steps DCI instructions.

Enter with: Call +1 = unbiased address of change table (clock stepping and instruction stepping use different addresses)

Exit to: Call +2

This subroutine uses a change table (described under GETRCT subroutine) to predict parameter register and TV monitor contents during clock and instruction stepping. When clock stepping, the entire TV monitor is compared against the predicted after each clock phase. After the final clock phase, the parameter registers are compared against the predicted. When instruction stepping, the parameter registers are compared against predicted after the obey one instruction. Then a new table is built from the entries in the clock stepping portion of the change table. Since this new table contains only the final entry for each TV monitor word, it is then used to predict the TV monitor contents after instruction stepping.

STER

This subroutine attempts to unload a register, but expects an external reject.

Enter with: Q = Equipment address and command

Exit to: Marker if error type 3 or 4
Call +1 if no error

STRP

This subroutine unloads a register expecting a reply.

Enter with: Q = Equipment address and command
Call +1 = number of times to loop on an external reject

Exit with: A = parameter register data or TV monitor word

Exit to: Call +2 if no error
Call +3 if error type 1 or 2 during interrupt state

X1I096

This subroutine compares parameter registers and TV monitor words against expected contents. The input parameters to the X1TCW subroutine determine which registers are compared and which ones are not compared. This subroutine is actually just a part of the X1TCW subroutine, but it was made into a subroutine to allow checking all registers before going to the forward or backward marker on an error.

X1TCW

This subroutine does the actual instruction stepping and clock stepping for the STEPER subroutine.

Enter with: A = Minus to instruction step
 0 to use subroutine to compare only
 1 to clock step 1 phase at a time
 5 to clock step 5 phases at a time (line drawing)
 Q = 1 to read and compare only parameter registers
 2 to read and compare only TV monitor

Exit to: Call +1

WAIT

This subroutine waits for an interrupt to occur within time limits.

Enter with: A = Lower time limit in milliseconds
 Q = Upper time limit in milliseconds
 Call +1 = Number of milliseconds after which interrupt is considered
 missing

Exit to: Marker if error type 8
 Call +2 if no error

VI. APPLICATIONS

A. GENERAL

If for some reason the operator wishes to stop after each clock pulse during clock stepping, he may set the system controller breakpoint to location X1I036 of the X1TCW subroutine. Also, he may wish to eliminate any register or TV monitor compare errors at this time. This is accomplished by storing a no-op (0B00) in location X1I090 of the X1TCW subroutine.

The backward marker of each condition (or subsection) normally points to the start of that condition and the forward marker points to the start of the next condition. The operator may change these markers by changing the two addresses following the RTJ to CINIT near the start of each condition. The first of the two addresses is the backward marker; the second is the forward marker. The address that the operator stores must be the listing address rather than the core address.

If the operator wishes to stop the system controller when an interrupt occurs, he may set the system controller breakpoint to DCI000 of the interrupt processor DCIPRO. The A register contains the interrupt status at the breakpoint stop.

B. HUNG CONDITIONS

If the test hangs or seems to be lost, the system controller and the display code interpreter should be stepped to halt all action. The computer registers, TV monitor and certain program locations should be observed to help define the problem.

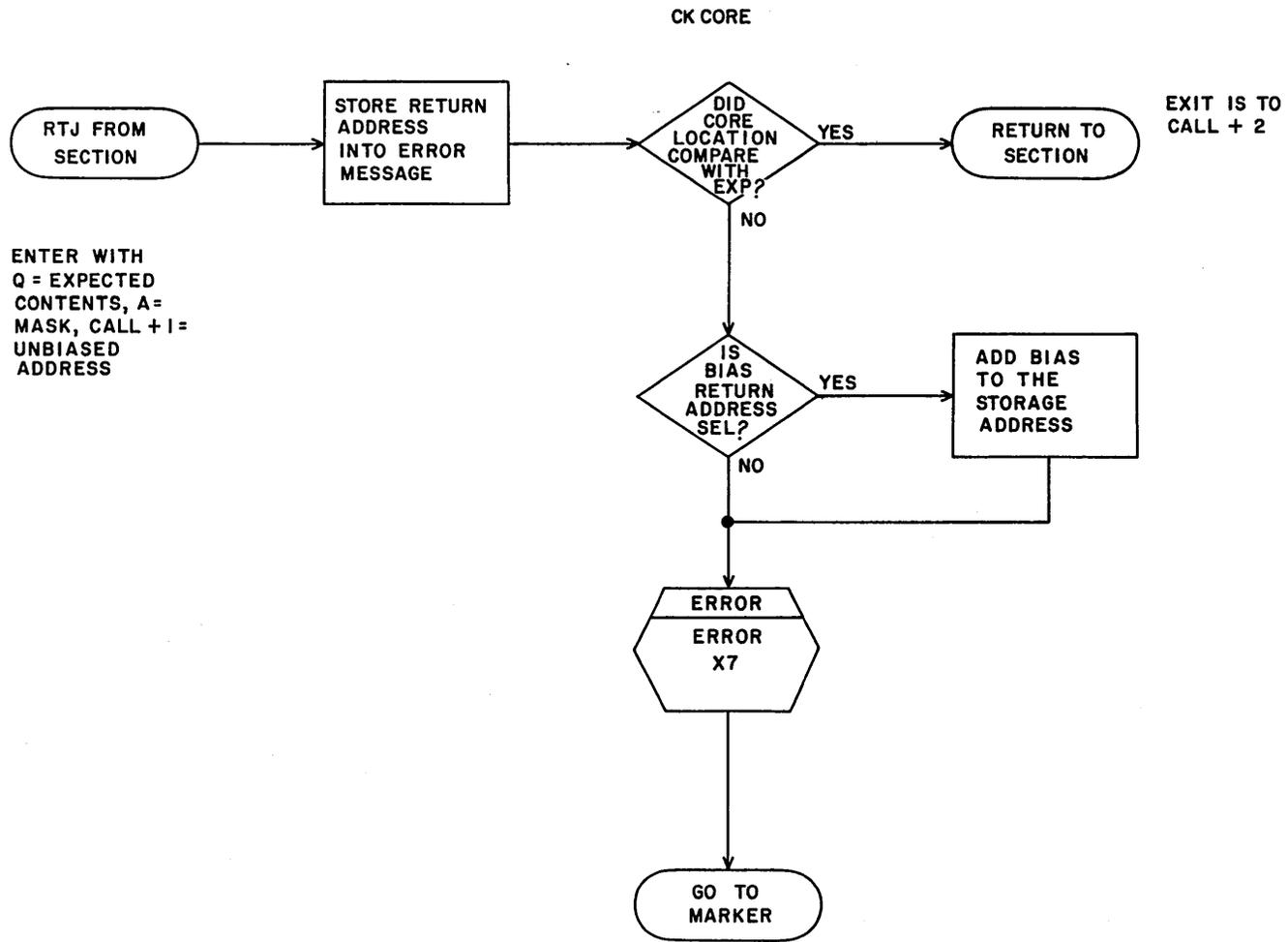
NOTE

Do not master clear the computer. If the computer is master cleared, much of the TV monitor information will also be cleared. Memory locations may be observed without master clearing. This is done by clearing P with the register clear button, setting P to the desired address, placing ENTER/SWEEP switch to SWEEP, stepping the RUN/STEP switch once, and observing the X register.

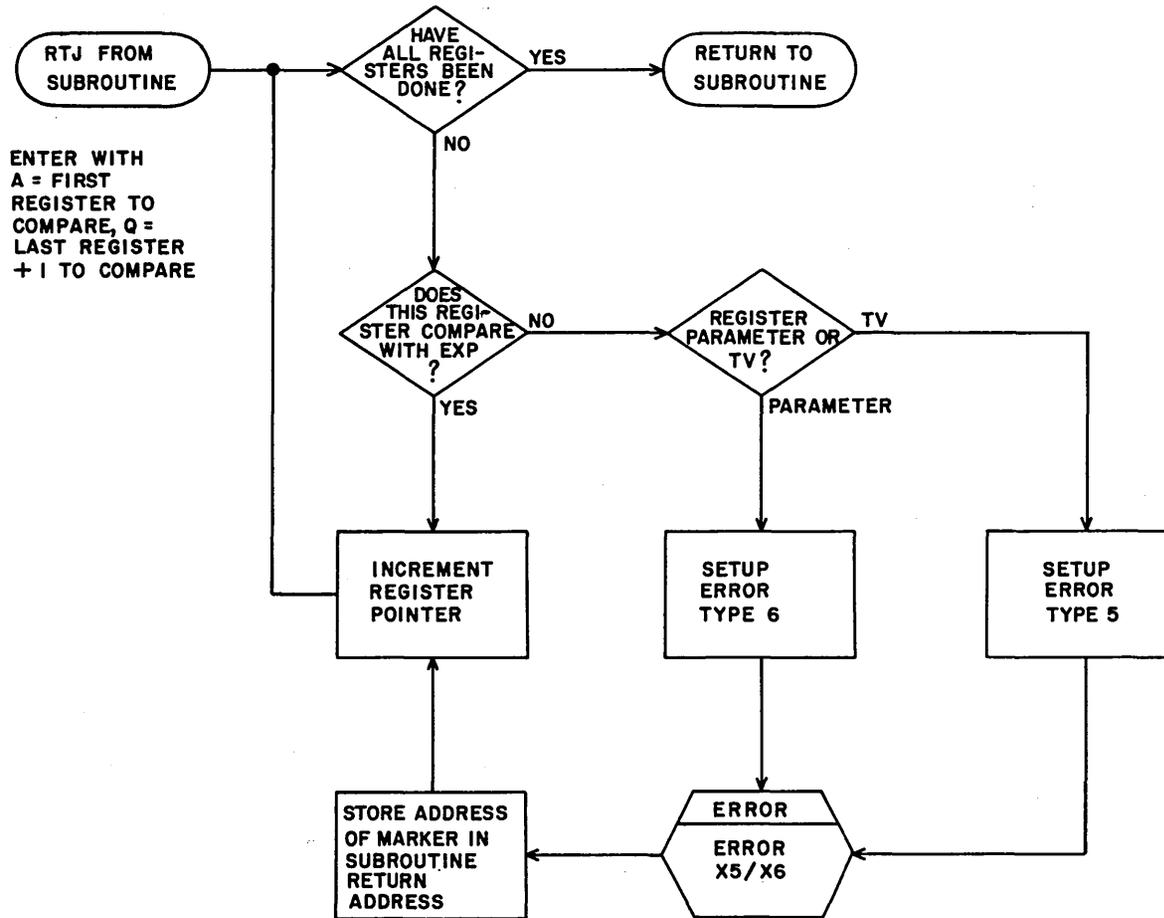
The test's section number, condition number, and return address are found in locations BET120, A2B, and Q2 respectively. These three locations point to where within the test section something went wrong.

The last DCI P register address loaded from the A/Q channel is saved in location LDT150.

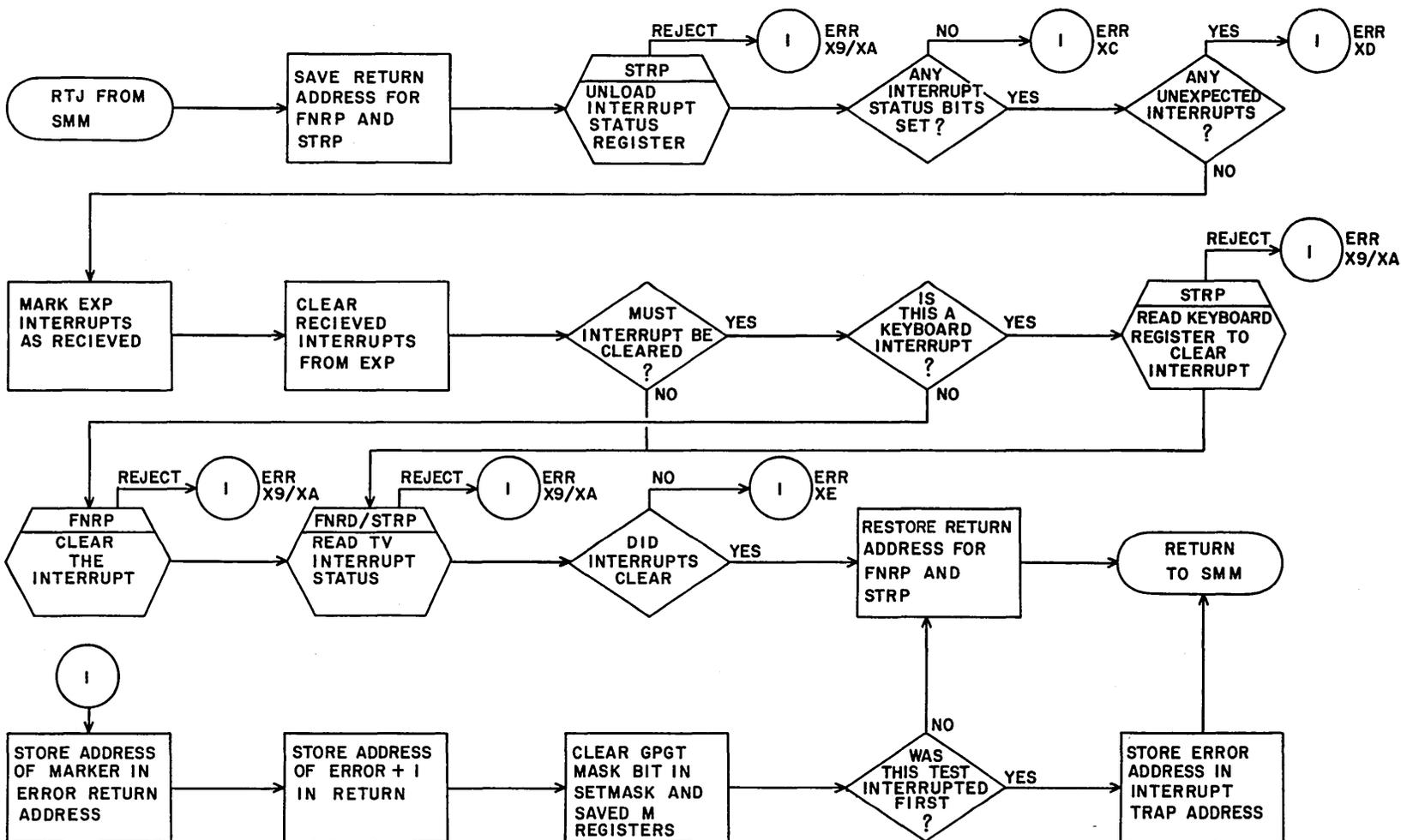
The computer M register may point to an interrupt problem if the mask bit for the DCI interrupt line is clear. If an interrupt problem is suspected, the expected interrupts and the received interrupts are saved in locations EXPINT and EXPREC respectively. The bits in these two locations correspond to bits in the Interrupt register 20_{16} in the DCI.



CMPALL



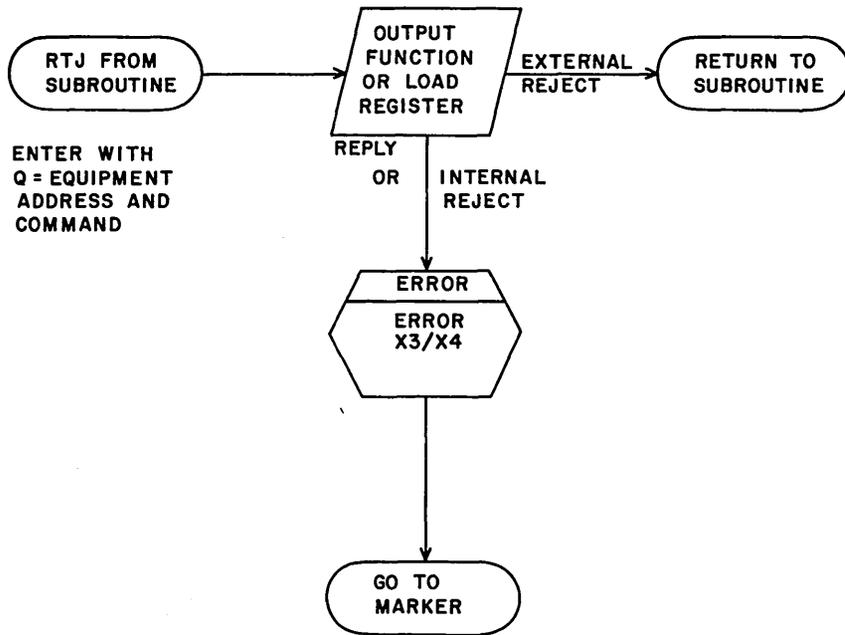
DCIPRO



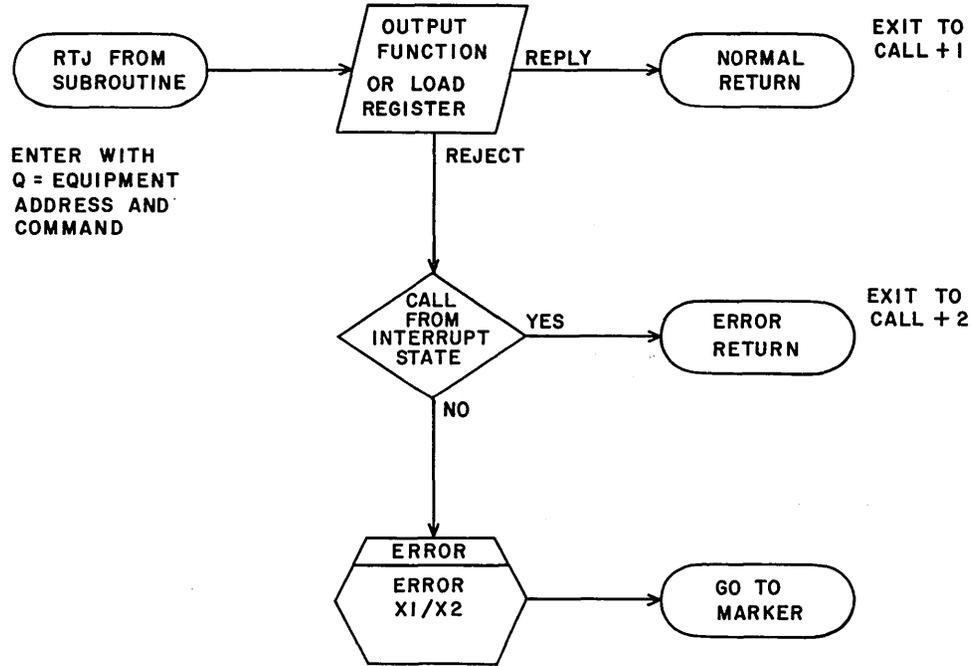
60182000 L

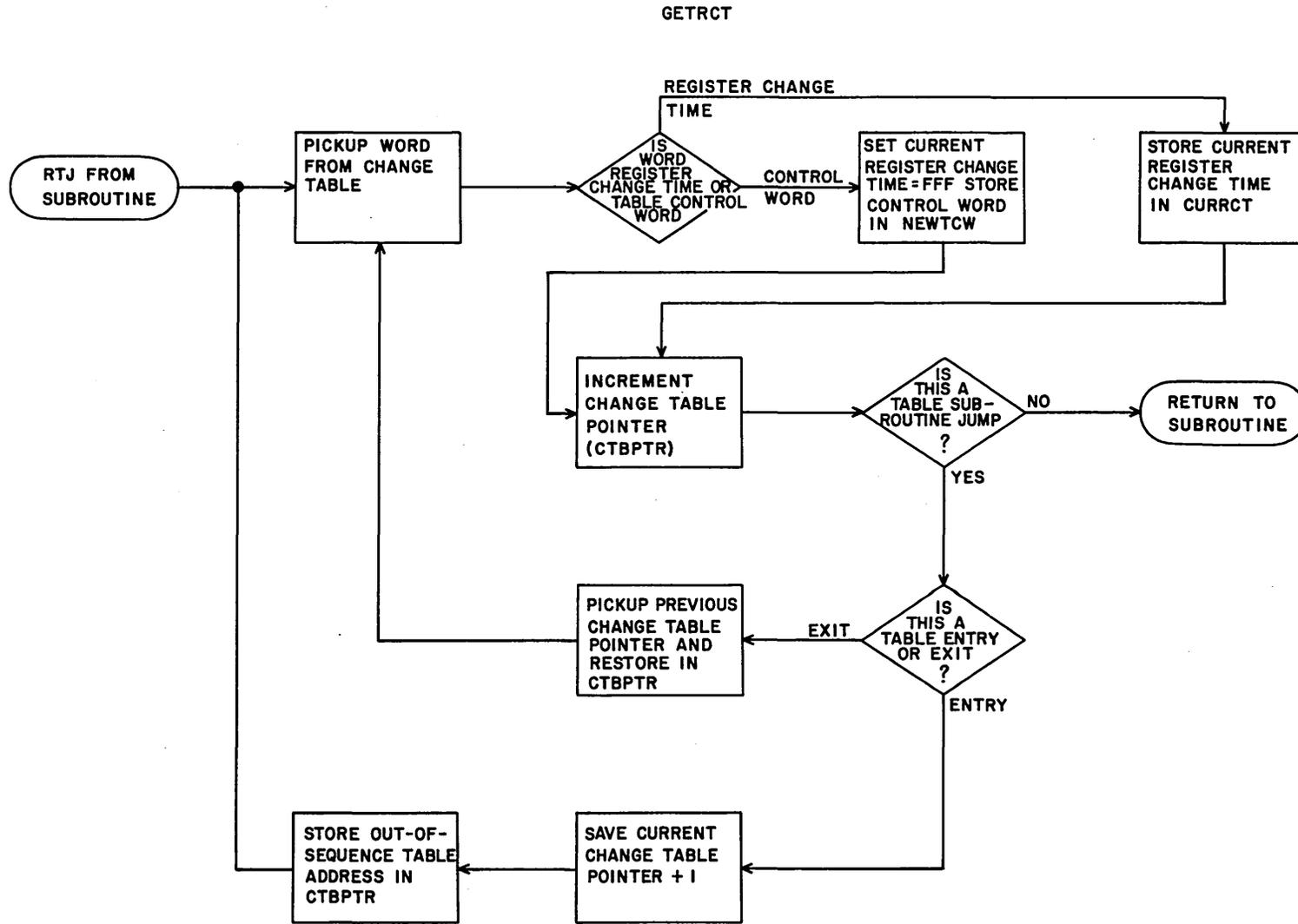
612-55

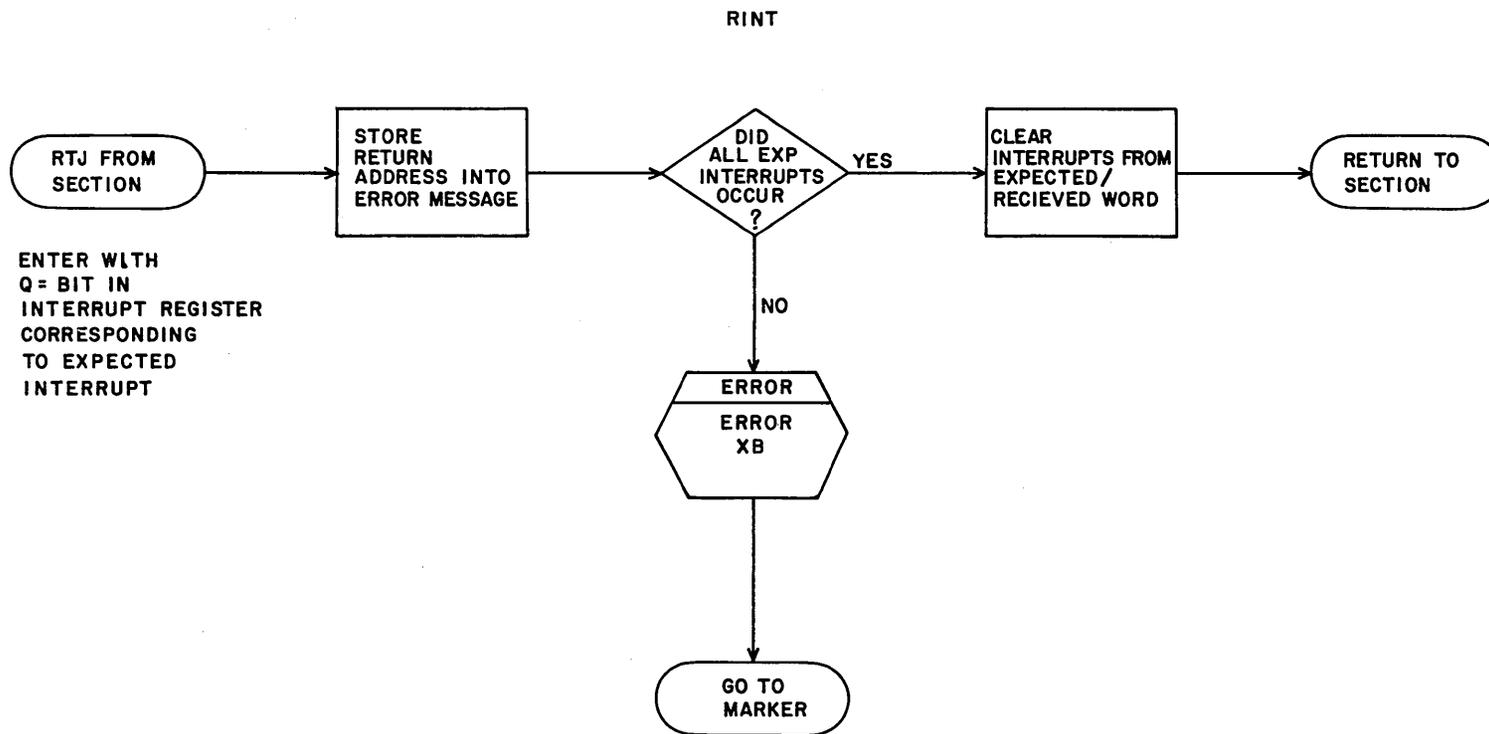
FNER



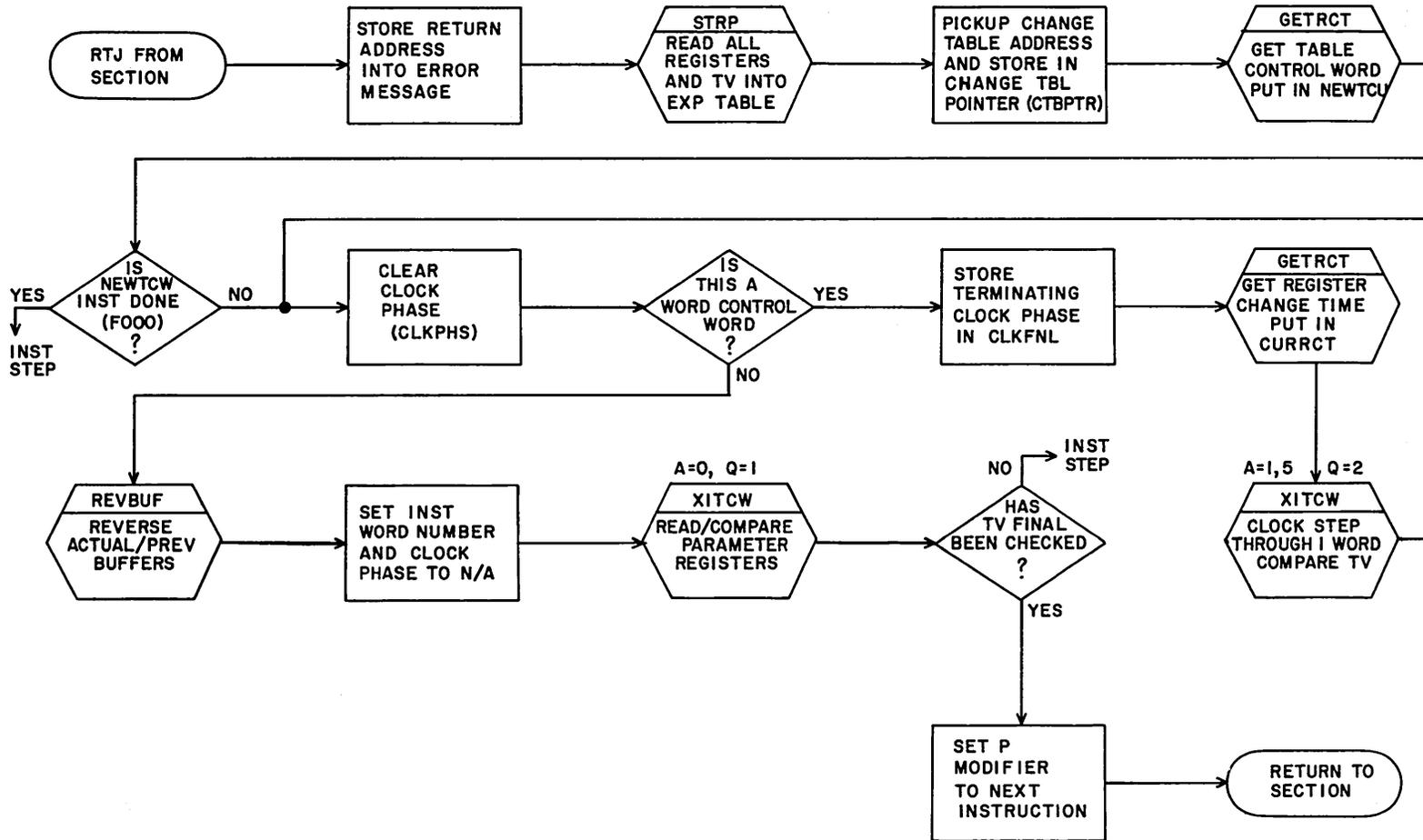
FNRP



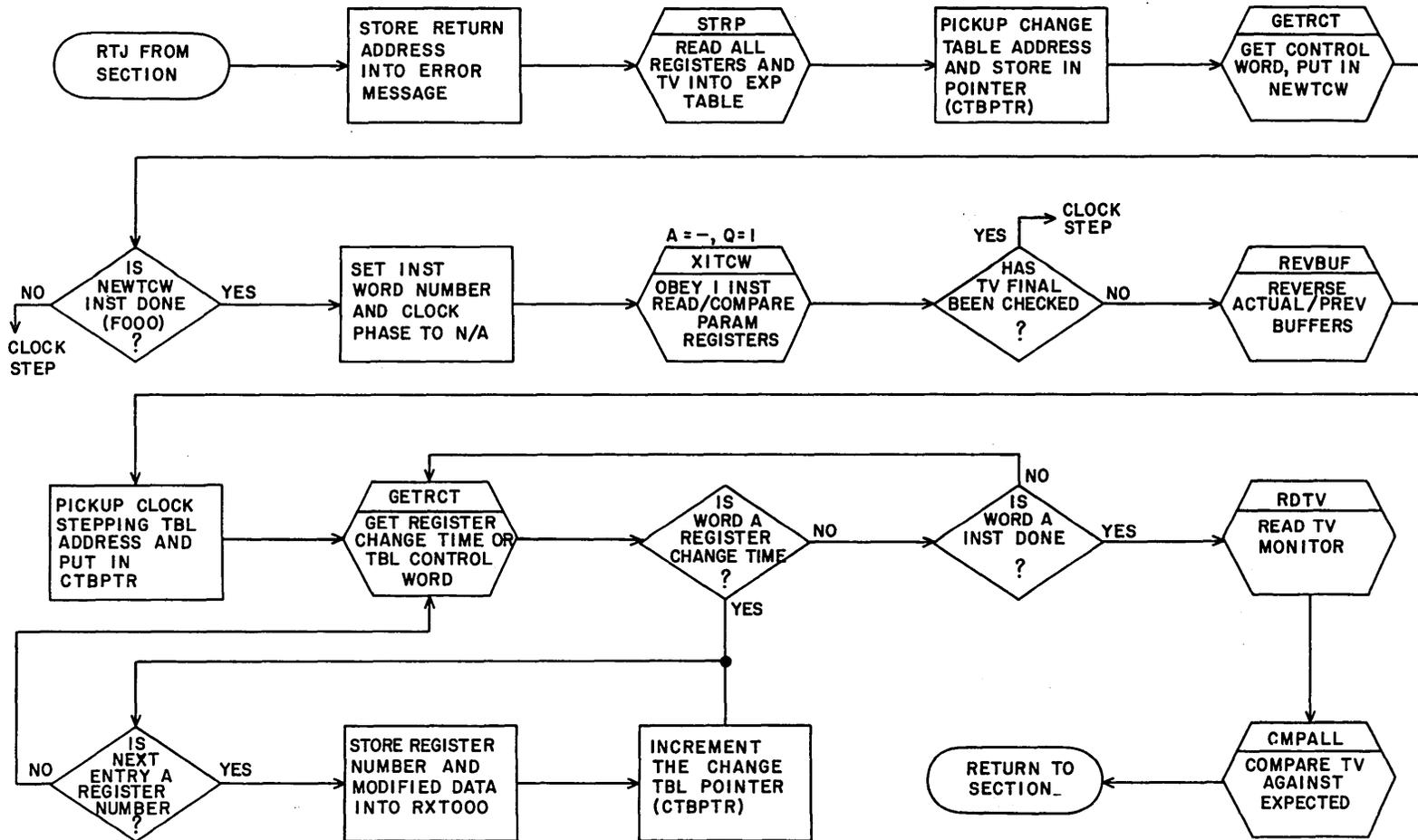




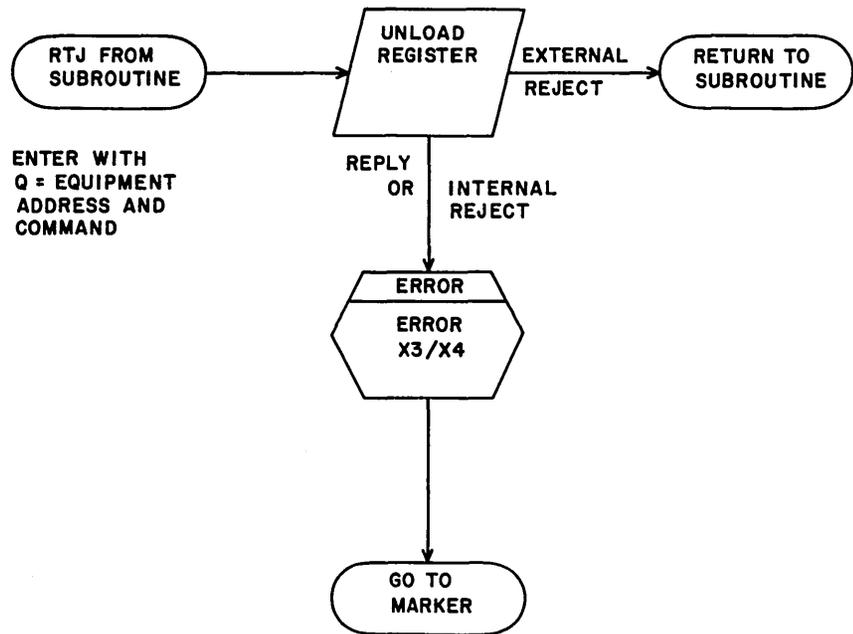
STEPPER (CLOCK STEP)



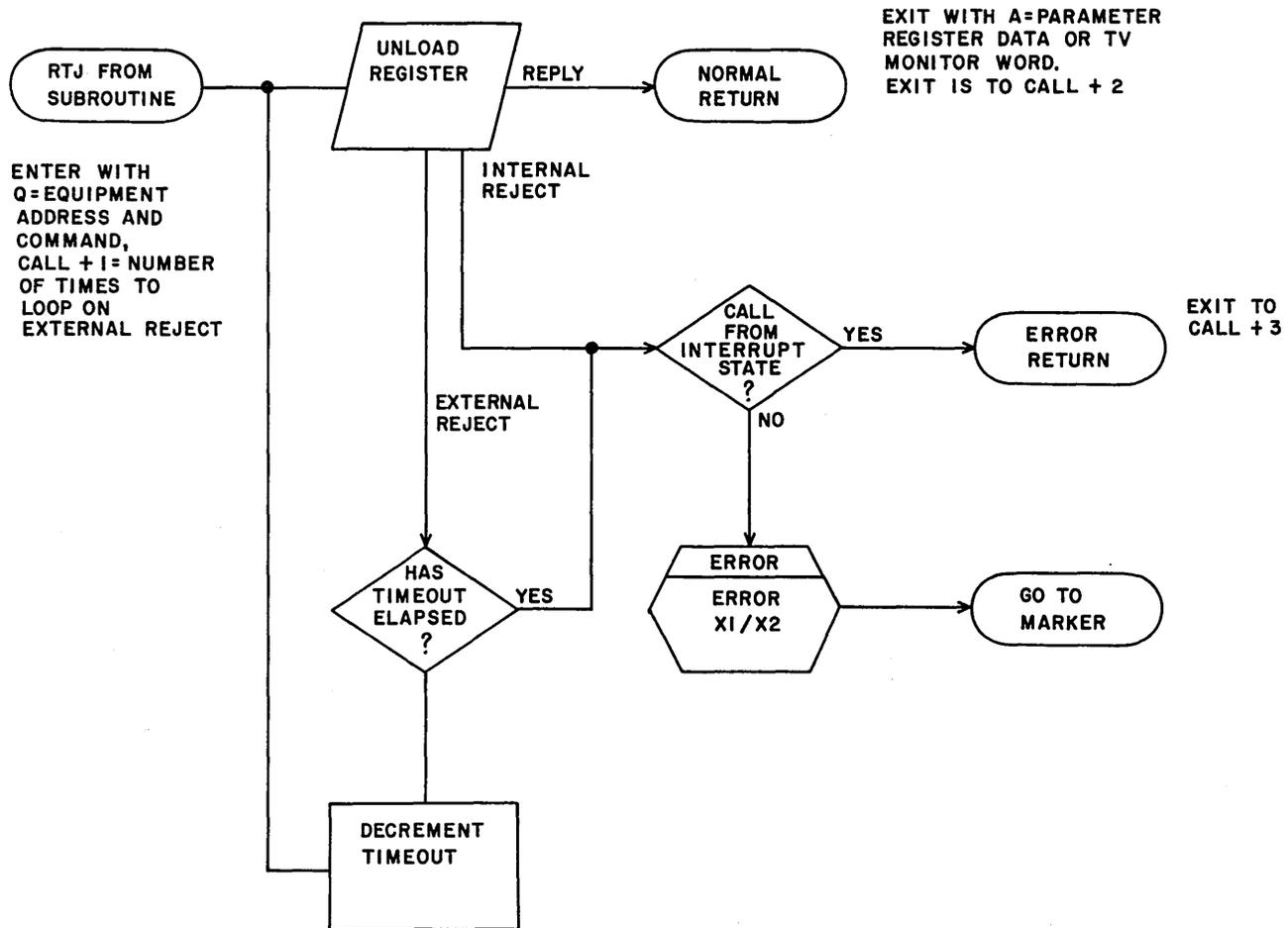
STEPPER (INSTRUCTION STEP)



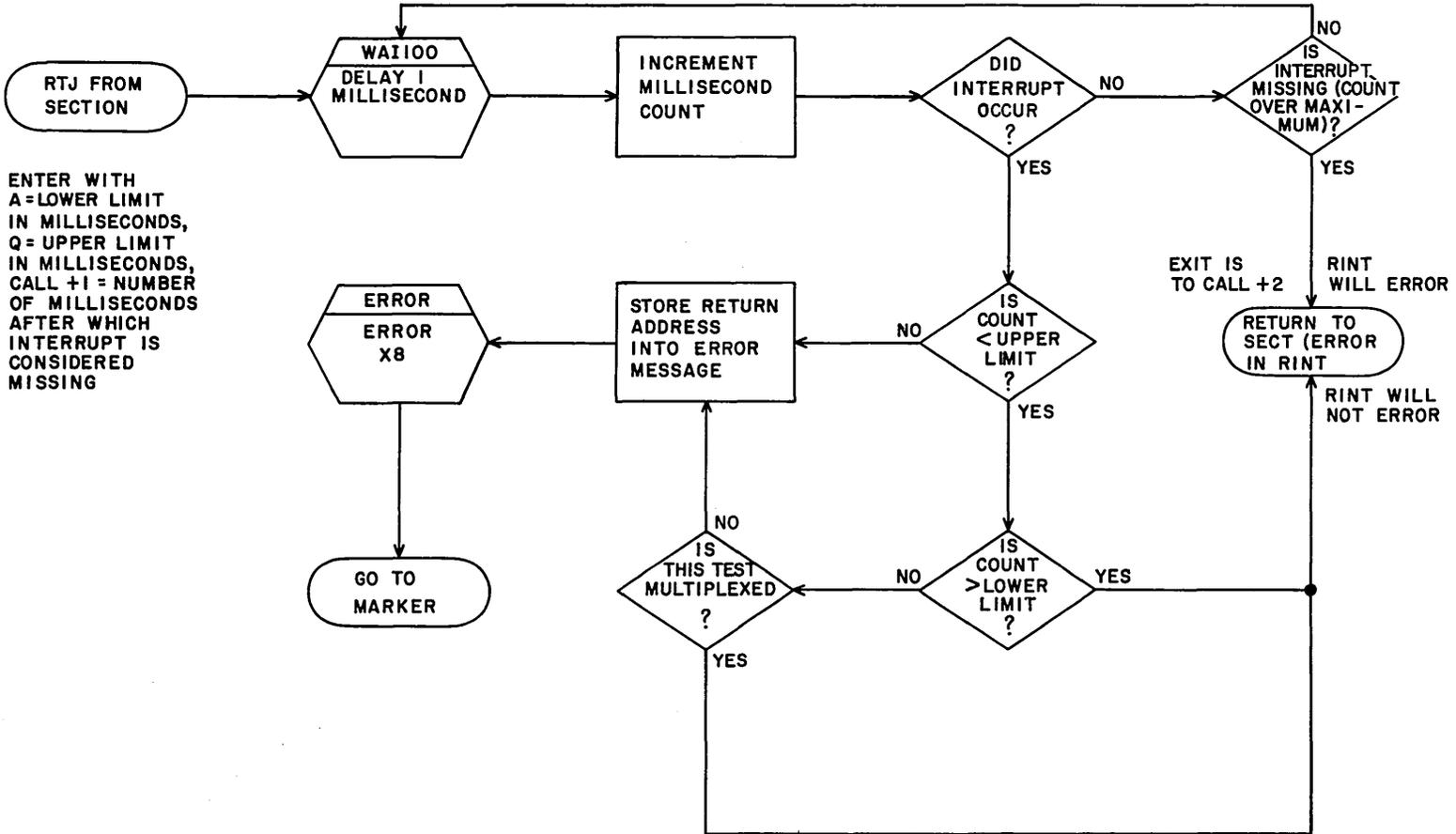
STER



STRP

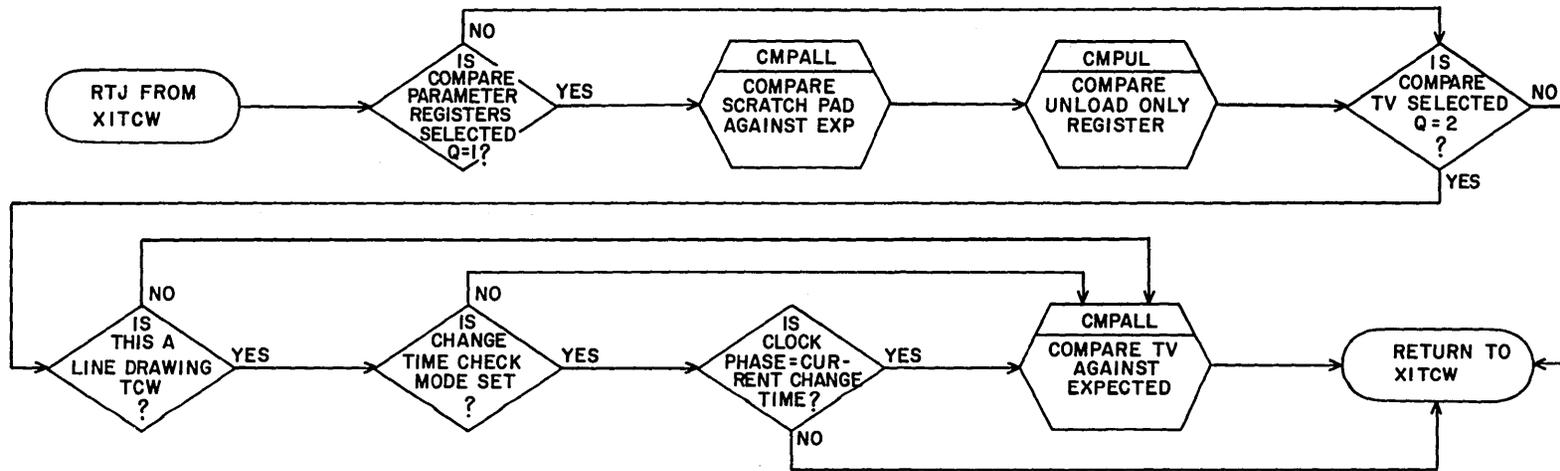


WAIT

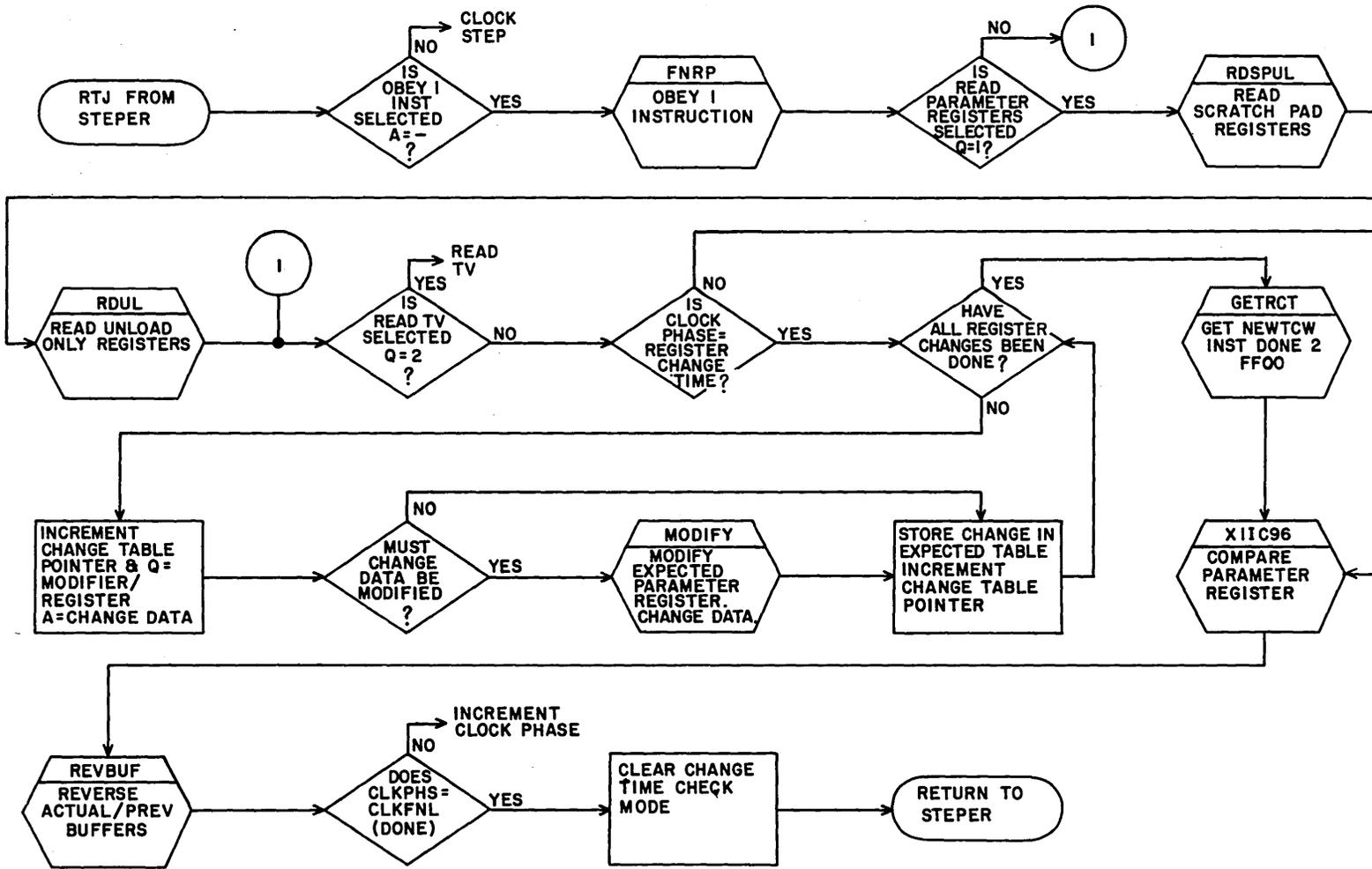


ENTER WITH
A=LOWER LIMIT
IN MILLISECONDS,
Q= UPPER LIMIT
IN MILLISECONDS,
CALL +1 = NUMBER
OF MILLISECONDS
AFTER WHICH
INTERRUPT IS
CONSIDERED
MISSING

XI I096

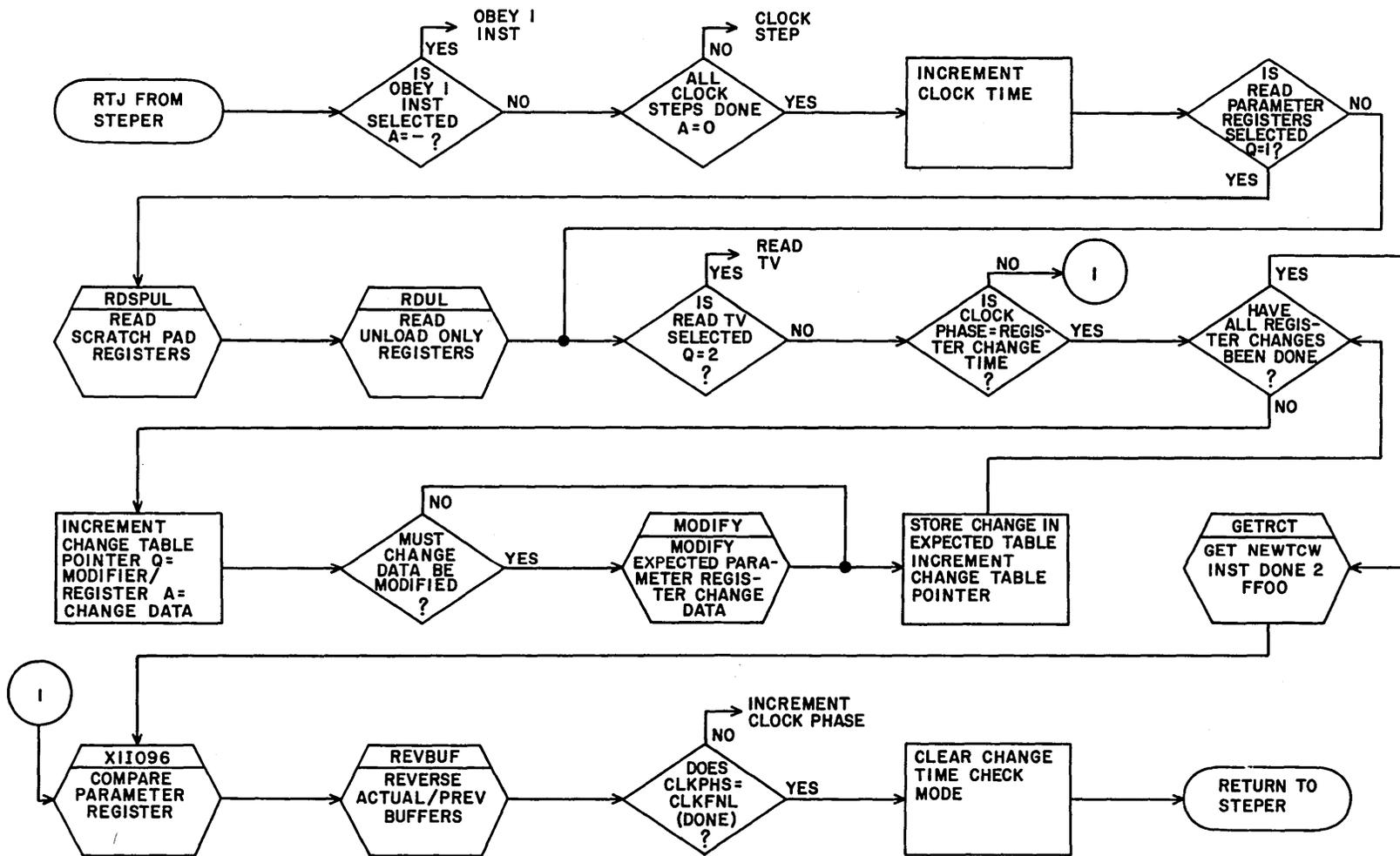


XITCW (A=-,Q=1)



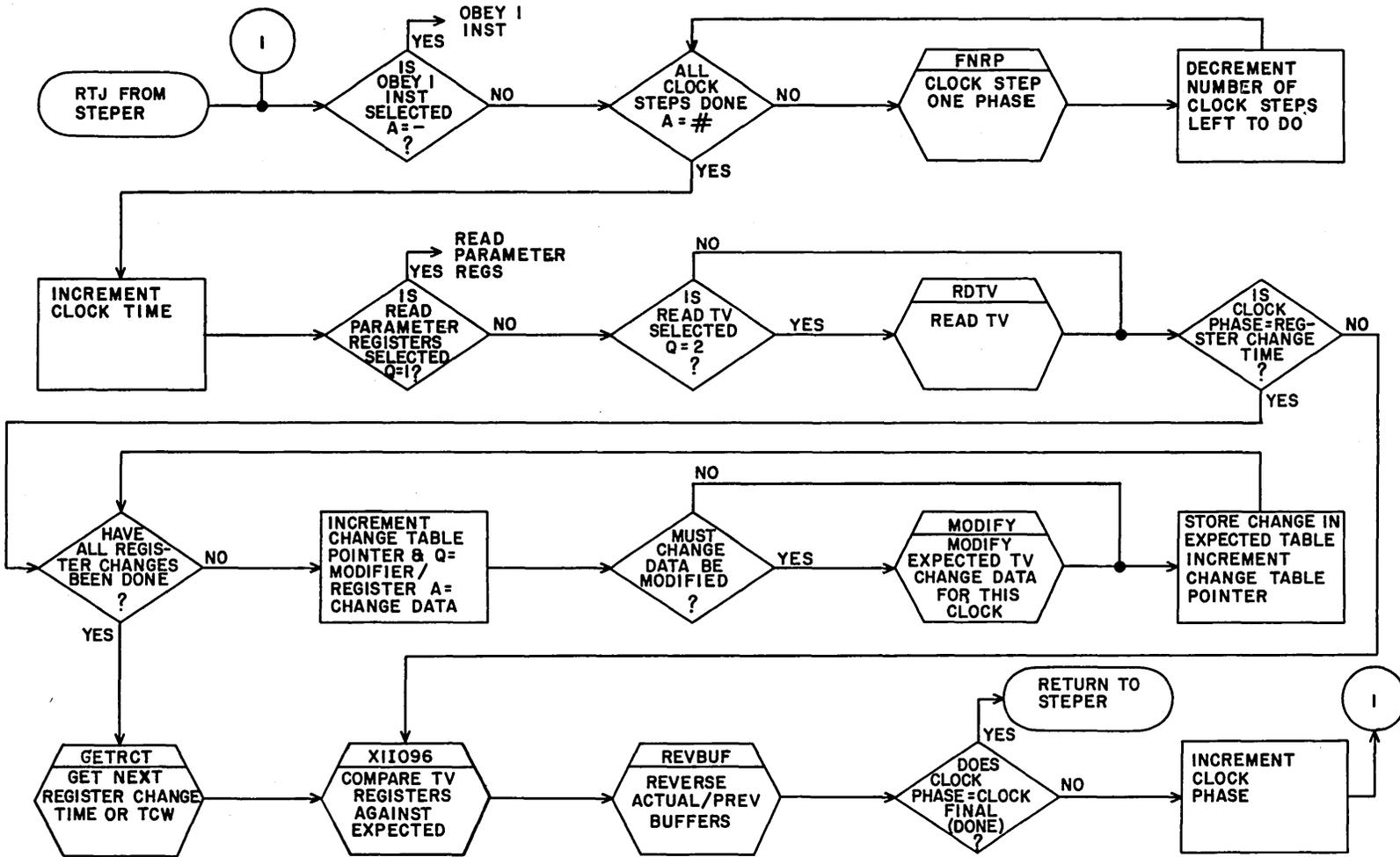
XITCW (A=0, Q=1)

60182000 L



612-67

XITCW (A=1, Q=2)



III. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 72 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First stop {overflow light on}

{A} = 7221 test ID stop
{Q} = Stop/Jump parameter

Second stop

{A} = Interrupt line for Display Code Interpreter
{Prestored as 0004-bit 2 designating interrupt line 2}
This parameter must not be changed after the initial parameter stop.
{Q} = Not used

2. DCI Switch Setting

DCI instruction/clock control switches must be UP.
The DCI PROTECT switch must be in UNPROTECTED.
The DCI REFRESH FAULT switch must be UP.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters
1 - Not sensed by this test
2 - Not sensed by this test
3 - Stop on error
4 - Not sensed by this test
5 - Not sensed by this test
6 - Not sensed by this test
7 - Not used
8 - Omit typeouts
9 - Bias return address display
10 - Re-enter parameters
11 - Not sensed by this test
12 - Not sensed by this test
13 - Not sensed by this test
14 - Not sensed by this test
15 - Run this test alone

{This bit should be set when two or more tests in the test list use the same display code interpreter equipment number. This allows the tests to be run consecutively since they cannot be multiplexed.}

C. PATTERN DESCRIPTION INDEX

Since the patterns in this test are used in the alignment procedure for the display console, a detailed description of the patterns is

located in the GPGT On-Site Maintenance Manual (Publication Number 82165000).

<u>Number</u>	<u>Name</u>
1	Quick Look
2	Focus {Vectors}
3	Pincushion
4	Text
5	Drift
6	Intensity
7	Focus {Dots}

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization.

```
GT2 {No. 72} GPGT DISPLAY QUALITY TEST  
IA = XXXX
```

2. Normal Display Console Message

Displayed at the console after the teletype message, during pattern selection, and during pattern manipulation.

```
PATTERN NUMBERS 1 = QUICKLOOK 2 = FOCUS....  
TO SELECT PATTERN, TYPE PTN/pattern number ETX  
FUNCT _
```

3. Stop on Error

All error message displays use basically the standard SMM17 error message format. The format of the first two stops is the same for all types of errors. The format of the third and fourth stops is determined by the type of error. The format for the first and second stops is as follows:

First stop {overflow light on}

```
{A} = 72XB test ID stop  
       where X is the number of stops  
{Q} = Stop/Jump parameter
```

Second stop

```
{A} = XX0Z where XX = Pattern number  
       Z = Error type  
{Q} = Address pointer to where within the  
       pattern setup the error occurred
```

This pointer is not the same as the return address

found in other SMM17 tests. The address points to where execution stopped when the error occurred, but not to where execution will continue after the error. Execution after the error continues from the beginning of the pattern setup.

B. MESSAGE DICTIONARY

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
01	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive internal reject A = I/O instruction Q = Q register function code
02	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive external reject A = I/O instruction Q = Q register function code
05	CMPALL	CMIO30	TV monitor has unexpected contents A = Actual TV display Q = Expected TV display A = Failing TV word number Q = Previous TV display
06	CMPALL	CMIO30	REGISTER, parameter register has unexpected contents A = Actual contents Q = Expected contents A = Failing register number Q = Previous contents
09	DCIPRO	DCIO02	INTERRUPT, internal reject during interrupt state A = I/O instruction Q = Q register function code
0A	DCIPRO	DCIO02	INTERRUPT, external reject during interrupt state A = I/O instruction Q = Q register function code
0B	RINT	RIIO10	INTERRUPT, missing A = Actual interrupts {bits corresponding to register 20 ₁₆ } Q = Expected interrupts {bits corresponding to register 20 ₁₆ }

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
0C	DCIPR0	DCIO20	<p>INTERRUPT, no interrupt status bit set when an interrupt occurred</p> <p>A = 0000 {actual status} Q = Expected interrupts {bits corresponding to register 20₁₆}</p>
0D	DCIPR0	DCIO30	<p>INTERRUPT, unexpected</p> <p>A = Actual interrupts {bits corresponding to register 20₁₆} Q = Expected interrupts {bits corresponding to register 20₁₆}</p>
0E	DCIPR0	DCIO60	<p>INTERRUPT, unable to clear interrupt status</p> <p>A = Actual interrupt status after attempted clear {bits corresponding to register 20₁₆} Q = Expected interrupt status after attempted clear {bits corresponding to register 20₁₆}</p> <p>A = Function used to attempt clear interrupt status 00 = Cleared when interrupt status or keyboard register unloaded 1A = Load interrupt enable register 1B = Load interrupt disable register 30 = Reset Q = Not used</p>

V. DESCRIPTION

A. GENERAL

This test allows the selection and manipulation of alignment patterns. These patterns are called and controlled by typing functions on the display console keyboard. Initially the display is as follows:

```
PATTERN NUMBERS 1 = QUICKLOOK 2 = FOCUS....
TO SELECT PATTERN, TYPE PTN/pattern number ETX
FUNCT ___
```

NOTE

Lower case on the keyboard must be selected. Upper case codes from the keyboard are ignored. Although lower case on the keyboard is used, display of letters is in upper case to be compatible with normal hexadecimal A-F notation.

Depressing the first key of a function type-in causes any previous pattern to stop being displayed and the function display with cursor to be displayed instead. That first symbol is displayed following the FUNCT and the cursor is advanced one space. Each symbol of the type-in is displayed and the cursor advanced until an ETX terminates the type-in. If you make an error while typing the function, depress BACKSPACE and correct your error. Illegal keys are ignored. Illegal functions are discarded and the cursor replaced following the FUNCT.

1. Display a Pattern {PTN/}

Type: PTN/n (ETX)
where n is the pattern number

The selected pattern is displayed using prestored parameters for window limits, zoom level, mask, conditional control register bits, and 11/12-bit window selection. Since each pattern has its own set of parameters, it is necessary to select a pattern before any pattern parameters are typed.

NOTE

The test ignores pattern parameters that are typed before a pattern number has been selected.

2. Change Window Location {8/ or 9/}

Type: 8/nxxx (ETX) for window location X
or 9/nxxx (ETX) for window location Y
where nxxx is the window location
{leading zeros need not be typed}

3. Change Zoom Level {18/}

Type: 18/n (ETX)
where n is the zoom level

4. Change Window Limits {19/}

Type: 19/wxyz (ETX)
where w is x upper limit
x is y upper limit
y is x lower limit
z is y lower limit

5. Change 11/12-Bit Window {PAR/}

Type: PAR/nn (ETX)
where nn is 11 for an 11-bit window
or 12 for a 12-bit window

6. Change CCR {B/}

Type: B/nnnn (ETX)
where nnnn is the value to be placed in the
conditional control register

NOTE

The conditional control register bits
are not sensed by all patterns. When
the CCR bits are sensed, they may have
different meaning from one pattern to
the next.

7. Terminate the Test {END/}

Type: END/ (ETX)

B. PATTERN PARAMETER DESCRIPTION

1. Quick Look

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	0
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	Not Used

2. Focus {vectors}

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	0
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	Not Used

3. Pincushion

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	0
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	Not Used

4. Text

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	6000
Window location Y {9}	9800
Zoom level {18}	3
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	0001

The Conditional Control register is used to select 1 or 16 paragraphs of text. If bit 0 of the CCR is set, one paragraph is displayed. If bit 0 is clear, 16 paragraphs are displayed.

5. Drift

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	4
Window limits {19}	0000
11/12-bit window	12
Conditional control	0101

The Conditional Control register is used to select either the vertical or horizontal drift test and also the wait time at each edge of the CRT. The CCR bits are assigned as follows:

Drift Test Selection

- Bit 8 - Horizontal drift test
- Bit 9 - Vertical drift test

Wait Time

- Bit 0 - 0 milliseconds
- Bit 1 - 20 milliseconds
- Bit 2 - 40 milliseconds
- Bit 3 - 80 milliseconds
- Bit 4 - 160 milliseconds
- Bit 5 - 320 milliseconds
- Bit 6 - 640 milliseconds
- Bit 7 - 640 milliseconds

b. Intensity

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	4
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	0001

The Conditional Control register is used to select quadrants of the intensity pattern. The CCR bits are assigned as follows:

- Bit 0 - All quadrants
- Bit 1 - Quadrant 1
- Bit 2 - Quadrant 2
- Bit 3 - Quadrant 3
- Bit 4 - Quadrant 4

7. Focus {Dots}

<u>Parameter</u>	<u>Prestored</u>
Window location X {8}	0000
Window location Y {9}	0000
Zoom level {18}	4
Window limits {19}	0000
11/12-bit window	12
Conditional control {B}	0001

The Conditional Control register is used to select the displayed symbol. The CCR bits are assigned as follows:

- Bit 0 - No symbol displayed {beam movements only}
- Bit 1 - Points
- Bit 2 - H's

C. PATTERN SETUP DESCRIPTION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
XX01 XX02	KEI001	Finish current instruction and stop. Expect reply.
XX01 XX02	KEI002 KEI003	Read TV DCI stopped bit. Expect reply. Return control to SMM. Wait for DCI stopped.
XX01 XX02 XX05	KEI004	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
XX01 XX02 XX05		Load write limits register. Expect reply.
XX01 XX02 XX06		Load and unload P register. Expect reply.
XX01 XX02 XX06		Load interrupt enable register with AF9F. Expect reply. Read TV interrupt enable. Expect AF9F.
XX01 XX02	KEI008	Start display. Expect reply {selected pattern or function display}.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
XX09 XX0A XX0C XX0D XX0E	KEI020	Return control to SMM. Wait for keyboard interrupt.
XX0B	KEI030	Verify that keyboard interrupt occurred. Store symbol into display file and update cursor position. If symbol is an (ETX), do the designated function. If END (ETX) has been typed, exit test.

GENERAL PURPOSE GRAPHICS TERMINAL {GPGT} LIGHT PEN AND KEYBOARD TEST
{GT3 Test No. 73}

I. INTRODUCTION

The purpose of this test is to verify the operation of the GPGT light pen and keyboard. The two modes of light pen operation, picking and tracking, are checked. Light pen picking is checked using vectors, points, symbols and combinations of vectors, points, and symbols. Light pen tracking is checked using basically the same tracking routine as used by the GPGT software system. The keyboard is checked by depressing keys in a random sequence and visually checking the resultant display. A symbol key results in displaying that symbol; a control key results in the indicated function or displaying the character sequence shown on that key.

II. REQUIREMENTS

A. HARDWARE

1. Minimum Configuration

1700

1708 Storage Increment
1705 Interrupt Data Channel
CC104A/B/C GPGT Console
CA122A Keyboard
CA203A/CA202A Light Pen
Input device for SMM17

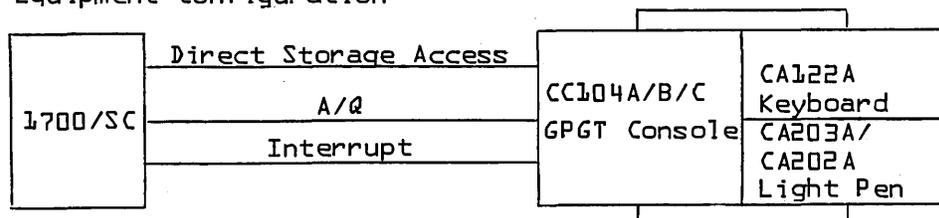
Systems Controller {SC}

1772 Magnetic Core Memory Module {8K}
1775 A/Q Interrupt Data Channel
1773 Direct Storage Access Channel
CC104A/B/C GPGT Console
CA122A Keyboard
CA203A/CA202A Light Pen
Input device for SMM17

2. Core Requirements

The minimum amount of core required is 8K.

3. Equipment Configuration



B. SOFTWARE

The test operates under control of the SMM17 monitor.

C. ACCESSORIES

None.

III. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 73 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First stop {overflow light on}

{A} = 7321 test ID stop
{Q} = Stop/Jump parameter

Second stop

{A} = Section selection bits {prestored as 0007}
Bit 0 = Section 0 - Light pen picking check
Bit 1 = Section 1 - Light pen tracking check
Bit 2 = Section 2 - Keyboard check
{Q} = Interrupt line for display code interpreter
{prestored as 0004-bit 2 designating interrupt line 2}
This parameter must not be changed after the initial parameter stop.

2. DCI Switch Setting

DCI instruction/clock control switches must be UP.
The DCI PROTECT switch must be in UNPROTECTED.
The DCI SENSE REFRESH FAULT switch must be UP.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters
1 - Stop at end of test section
2 - Stop at end of test
3 - Stop on error
4 - Repeat condition
5 - Repeat section
6 - Repeat test
7 - Not used
8 - Omit typeouts
9 - Bias return address display
10 - Re-enter parameters
11 - Not sensed by this test
12 - Not sensed by this test
13 - Not sensed by this test
14 - Not sensed by this test
15 - Run this test alone
{This bit should be set when two or more tests in the test list use the same display code interpreter equipment number. This allows the tests to be run consecutively, since they cannot be multiplexed.}

C. SECTION DESCRIPTION INDEX

<u>Number</u>	<u>Name</u>
0	Light pen picking
1	Light pen tracking
2	Keyboard

IV. OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization.

```
GT3 {NO. 73} GPGT LIGHT PEN/KEYBOARD TEST  
IA = XXXX
```

2. Normal Display Console Message

Displayed at the console during the keyboard check section.

```
KEYBOARD TEST-TERMINATE WITH RESET, E, N, D, ETX
```

3. Stop at End of Test Section

First stop {overflow light on}

```
{A} = 7322 - test ID stop  
{Q} = Stop/Jump parameter
```

Second stop

```
{A} = Section number  
{Q} = Return address
```

4. Stop at End of Test

First stop {overflow light on}

```
{A} = 7324 - test ID stop  
{Q} = Stop/Jump parameter
```

Second stop

```
{A} = Pass number  
{Q} = Return address
```

5. Stop on Error

All error message displays use basically the standard SMM17 error message format. The format of the first two stops is the same for all types of errors. The format of the third and fourth stops is determined by the type of error. The format for the first and second stops is as follows:

First stop {overflow light on}

{A} = 73XB - test ID stop
where X is the number of stops
{Q} = Stop/Jump parameter

Second stop

{A} = XYZ where XX = Section number
Y = Condition {or subsection}
Z = Error type
{Q} = Address pointer to where within a condition the error occurred.

This pointer is not the same as the return address found in other SMM17 tests. The address points to where execution stopped when the error occurred, but not to where execution will continue after the error. Where execution continues after the error is determined by the repeat conditions bit of the Stop/Jump parameter. If the repeat condition bit is set, execution will continue at a backward marker, a recovery point to repeat the condition designated in {A} of this second stop. If the repeat condition bit is not set, execution will continue at a forward marker, a recovery point to skip around the remainder of the condition designated in {A} of this second stop.

B. MESSAGE DICTIONARY

The upper hexadecimal digit of the two-digit error message code designates the condition {or subsection} that failed. The lower digit is the error type. This message dictionary describes the error types.

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X1	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive internal reject

A = I/O instruction
Q = Q register function code

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X2	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive external reject A = I/O instruction Q = Q register function code
X5	CMPALL	CMIO30	TV monitor has unexpected display A = Actual TV display Q = Expected TV display A = Failing TV word number Q = Previous TV display
X6	CMPALL	CMIO30	REGISTER, parameter register has unexpected contents A = Actual register contents Q = Expected register contents A = Failing register number Q = Previous register contents
X8	WAIT	WAI050 WAI060	TIME, interrupt did not occur within expected time limits A = Lower limit {in milliseconds} Q = Upper limit {in milliseconds} A = Actual time {in milliseconds} Q = Not used
X9	DCIPRO	DCIO02	INTERRUPT, internal reject during interrupt state A = I/O instruction Q = Q register function code
XA	DCIPRO	DCIO02	INTERRUPT, external reject during interrupt state A = I/O instruction Q = Q register function code
XB	RINT	RIIO10	INTERRUPT, missing A = Actual interrupts {bits corresponding to register 20 ₁₆ } Q = Expected interrupts {bits corresponding to register 20 ₁₆ }
XC	DCIPRO	DCIO20	INTERRUPT, no interrupt status bit set when an interrupt occurred A = 0000 {actual status} Q = Expected interrupts {bits corresponding to register 20 ₁₆ }

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
XD	DCIPR0	DCIO30	<p>INTERRUPT, unexpected</p> <p>A = Actual interrupts {bits corresponding to register 20₁₆}</p> <p>Q = Expected interrupts {bits corresponding to register 20₁₆}</p>
XE	DCIPR0	DCIO60	<p>INTERRUPT, unable to clear interrupt status</p> <p>A = Actual interrupt status after attempted clear {bits corresponding to register 20₁₆}</p> <p>Q = Expected interrupt status after attempted clear {bits corresponding to register 20₁₆}</p> <p>A = Function used to attempt clear interrupt status</p> <p>00 = Cleared when interrupt status or keyboard register unloaded</p> <p>1A = Load interrupt enable register</p> <p>1B = Load interrupt disable register</p> <p>30 = Reset</p> <p>Q = Not used</p>

V. DESCRIPTION

A. GENERAL

Since Section 0 requires the operator to execute conditions in a sequential manner, standard SMM17 error messages are provided when an unexpected result occurs. Sections 1 and 2 have no required sequence and thus, expected results must be verified visually. However, unexpected interrupts are always enabled and an error is reported if any unexpected interrupt is received.

B. SECTION DESCRIPTIONS

1. Section 0 - Light Pen Picking

Each condition in Section 0 follows the same sequence of operations. Two DCI drawing instructions {vector and/or symbol} are executed in each condition. Light pen hits are enabled on

the first and disabled on the second. The operator must pick the one that is enabled. If a vector is to be picked, it must be picked at its end nearest the disabled vector or symbol. This is necessary to check the light pen hit beam position registers 06 and 07. The vector and/or symbol combinations for five conditions in this section are as follows:

<u>Condition Number</u>	<u>Light Pen Hit Enabled</u>	<u>Light Pen Hit Disabled</u>
0	Long Vector	Short Vector
1	Long Vector	Point Symbol
2	Point Symbol {on the left}	Point Symbol {on the right}
3	Dollar Sign	Point Symbol
4	Point Symbol	Short Vector

To execute the picking operation in each condition, the operator must perform the operations as follows:

- a. Begin with the light pen switch off.
When the light pen switch is off, the vector and/or symbol combination is drawn and the alarm is sounded.
- b. Press the tip of the light pen against the face of the CRT so that the light pen is over the disabled vector or symbol and the light pen switch is depressed.
When the lightpen switch is depressed, the audible alarm is silenced. No light pen hit should occur.
- c. Move the tip of the light pen so that it is over the enabled vector or symbol, keeping the light pen switch depressed.
When the light pen hit occurs, the vector and/or symbol combination is no longer drawn.
- d. When the vector and/or symbol combination disappears, release the light pen switch.
When the light pen switch is released, the next condition is displayed, unless the repeat condition stop/jump bit is set.

Operations 1 - 4 are repeated for each condition. When all conditions have been completed, the next selected section is executed.

The sequence of operations is the same for all conditions {subsections} of Section 0. Therefore, only one detailed description is necessary.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
00X1 00X2 00X5	LSI000	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
00X1 00X2 00X6		Load and unload P register. Expect reply.
00X1 00X2		Clear audible alarm. Expect reply.
00X1 00X2	LSI010	Read TV interrupt status. Expect reply. Return control to SMM. Wait for light pen switch off status.
00X1 00X2 00X5	LSI020	Load interrupt enable register. Expect reply. Read TV interrupt enable. Expect 2EAF.
00X1 00X2	LSI028	Unload all scratchpad registers. Expect reply.
00X1 00X2		Start display. Expect reply.
00X1 00X2		Set audible alarm. Expect reply.
00X9 00XA 00XC 00XD 00XE	LSI030	Return control to SMM. Wait for light pen switch interrupt.
00XB	LSI040	Verify that light pen switch interrupt occurred.
00X1 00X2 00X5		Read TV interrupt status. Expect light pen switch on.
00X1 00X2		Clear audible alarm. Expect reply.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
00X1 00X2		Finish current instruction and stop. Expect reply.
00X1 00X2	LSI041 LSI41A	Read TV DCI stopped bit. Expect reply. Return control to SMM. Wait for DCI stopped.
00X5	LSI042	Verify that DCI stopped bit is set.
00X1 00X2	LSI043	Load interrupt disable register. Expect reply.
00X1 00X2		Start display. Expect reply.
00X9 00XA 00XC 00XD 00XE	LSI044	Return control to SMM. Wait for light pen hit interrupt.
00XB	LSI046	Verify that light pen hit interrupt occurred.
00X1 00X2		Unload all scratchpad registers. Expect reply.
00X1 00X2		Unload the unload only parameter registers Expect reply.
00XB	LSI060	Verify that scratchpad registers have expected contents.
00X1 00X2		Load interrupt enable register with light pen switch interrupt bit. Expect reply.
00X9 00XA 00XC 00XD 00XE		Wait 5 seconds for light pen switch interrupt.
00XB	LSI090	Verify that the light pen switch interrupt occurred.
00XB		Verify that light pen switch status bit is off. Check repeat condition stop/ jump bit.

2. Section 1 - Light Pen Tracking

The tracking routine is basically the same program used by the GPGT software system. To execute the tracking routine, the operator must perform the operations as follows:

- a. Begin with the light pen switch off.
When the light pen switch is off, a small diamond with a point at its center is drawn on the display.
- b. Press the tip of the light pen against the face of the CRT so that the light pen switch is depressed.
When the light pen switch is depressed, tracking is activated. The diamond is replaced by the tracking symbol of six points.
- c. Move the tip of the light pen randomly across the face of the CRT, keeping the light pen switch depressed.
The tracking symbol should follow the light pen wherever the light pen is moved. If the tracking system loses the light pen, a search pattern will scan the entire screen until the light pen is found again.
- d. When it is desired to terminate the tracking section, release the light pen switch.
When the light pen switch is released, the next selected section is executed, unless the repeat condition or repeat section stop/jump bits are set.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0101 0102 0105	Track	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0101 0102 0106		Load and unload P register. Expect reply.
0101 0102 0106		Load and unload conditional control register with 0001. Expect reply.
0101 0102	TRIO10	Read TV interrupt status. Expect reply. Return control to SMM. Wait for light pen switch status bit to be off.
0101 0102 0105	TRIO20	Load interrupt enable register. Expect reply. Read TV interrupt enable. Expect AEBD.
0101 0102 0105		Load write limits. Expect reply. Read TV write limits. Expect reply.
0101 0102		Start display. Expect reply Diamond is displayed.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0109 010A 010C 010D 010E	TRIO30	Return control to SMM. Wait for light pen switch interrupt.
0108	TRIO40	Verify that light pen switch interrupt occurred.
0101 0102 0105		Read TV interrupt status. Expect light pen switch on.
0101 0102		Finish current instruction and stop. Expect reply.
0101 0102	TRIO41 TRIO41A	Read TV DCI stopped bit. Expect reply. Return control to SMM. Wait for DCI stopped.
0105	TRIO42	Verify that DCI stopped bit is set.
0101 0102	TRIO43	Load interrupt enable register. Expect reply.
0101 0102 0106		Load and unload conditional control register with 0000. Expect reply.
0101 0102		Start display. Expect reply. Tracking symbol is displayed.
0109 010A 010C 010D 010E	TRIO50	Return control to SMM. Wait for light pen switch interrupt.
0108	TRIO60	Verify that light pen switch interrupt occurred.
0101 0102 0105		Read TV interrupt status. Expect light pen switch off. Check repeat condition stop/jump bit.

3. Section 2 - Keyboard Operation

To execute the keyboard section, the operator must perform the operations as follows:

- a. The section begins with a display of a cursor and the message as follows:

KEYBOARD TEST - TERMINATE WITH RESET, E,N,D, ETX

- b. Randomly depress the keyboard keys.

When a key is depressed, it results in one of the following:

- 1} The symbol for that key is displayed at the cursor position and the cursor is advanced one space.
- 2} The character sequence shown on that key is displayed and the cursor advanced the number of spaces in the character sequence. {F1,F2,F3,F4,F5, F6,F7,F8,F9,F10, SUPERSCRIP^T, SUBSCRIP^T, NORMAL TEXT, INT, and ETX}
- 3} A function is executed as specified by any of the keys as follows:

SKIP - advance cursor one space

BACKSPACE - backspace cursor one space

LINE DOWN - advance cursor one line

LINE UP - move cursor back one line

NEW LINE - move cursor to start of next line

RESET - move cursor to start of first line

LINE CLEAR - clear all symbols to the right of cursor and move cursor to start of next line

CLEAR - clear all symbols and move cursor to start of first line

- 4} If an illegal code is received, the two digit hexadecimal code is displayed in a message as follows:

XX ILLEGAL CODE {XX = code}

The cursor is advanced 15 spaces.

- c. When it is desired to terminate the keyboard section, type the following:

RESET END **ETX**

THE E, N, and D MUST BE UPPER CASE.

When the above is typed, the section is terminated,

unless the repeat condition or repeat section stop/jump bits are set.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0201 0202 0205	Key	Reset. Expect reply. Read TV interrupt enable. Expect 0000.
0201 0202 0206		Load and unload P register. Expect reply.
0201 0202 0205		Load interrupt enable register. Expect reply. Read TV interrupt enable. Expect BE&F.
0201 0202		Start display. Expect reply.
0209 020A 020C 020D 020E	KEI020	Return control to SMM. Wait for keyboard interrupt.
0208	KEI030	Verify that keyboard interrupt occurred. Store symbol(s) into display file and update cursor position. If (RESET) END (ETX) has not been typed, go back and wait for another keyboard interrupt. If (RESET) END (ETX) has been typed, check repeat condition stop/jump bit.

GENERAL PURPOSE GRAPHICS TERMINAL (GPGT)
 (16-BIT) COMMUNICATIONS INTERFACE TEST
 (GT4 Test No. 74)

I. INTRODUCTION

The purpose of this test is to verify the operation of the GPGT communications interface. The test operates in link around mode in which the receiver is connected to the output of the transmitter. Since this mode of operation is selected by a software function, no hardware alteration is necessary. The modem interface drivers and receivers are not included in the link around data path.

II REQUIREMENTS

A. HARDWARE

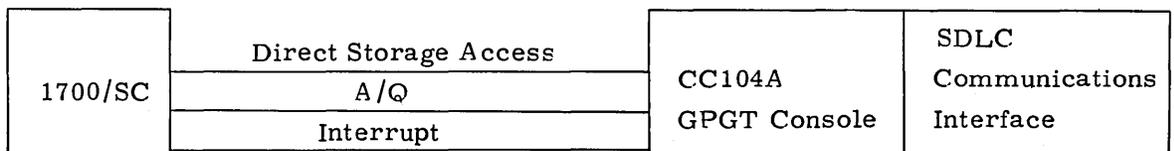
1. Minimum Configuration

<u>1700</u> 1705 Interrupt Data Channel CC104A GPGT Console Input device for SMM17	<u>System Controller (SC)</u> 1772 Magnetic Core Memory Module (4K) 1775 A/Q Interrupt Data Channel 1773 Direct Storage Access Channel CC104A GPGT Console Input device for SMM17
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2. Core Requirements

The minimum amount of core required is 4K.

3. Equipment Configuration



B. SOFTWARE

The test operates under control of the SMM17 monitor.

C. ACCESSORIES

None

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 74 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First stop (overflow light on)

(A) = 7431 test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Section selection bits (prestored as 03FF)

Bit 0 = Section 0 - Zeros

1 = Section 1 - Ones

2 = Section 2 - Shifting zeros

3 = Section 3 - Shifting ones

4 = Section 4 - Compliments

5 = Section 5 - Doubling lengths

6 = Section 6 - Random

7 = Section 7 - Buffer overflow

8 = Section 8 - Buffer unfilled

9 = Section 9 - Protect failure

(Q) = Interrupt line for communications interface (prestored as 0008-bit 3
designating interrupt line 2)

Third stop

(A) = Station address (in bits 0-4)

(prestored as 0000)

(Q) = Not used in link around

2. Data Terminal Switch Setting

The DATA TERMINAL IN switch must be UP.

The PROTECT switch must be DOWN.

The PRIORITY switch must be DOWN.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters

1 - Stop at end of test section

2 - Stop at end of test

3 - Stop on error

4 - Repeat condition (buffer)

5 - Repeat section

6 - Repeat test

7 - Not used

8 - Omit typeouts

- 9 - Bias return address display
- 10 - Re-enter parameters
- 11 - Use QSE10358/QSE6873 driver in place of link-around driver
(See supplement A)
- 12 - Not sensed by this test
- 13 - Not sensed by this test
- 14 - Not sensed by this test
- 15 - Not sensed by this test

C. SECTION DESCRIPTION INDEX

<u>Number</u>	<u>Name</u>	<u>Run Time</u>
0	Zeros	
1	Ones	
2	Shifting Zeros	
3	Shifting Ones	
4	Complements	
5	Doubling Lengths	
6	Random	
7	Buffer Overflow	
8	Buffer Unfilled	
9	Protect Failure	

IV OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization.

GT4 (No. 74) GPGT COMMUNICATIONS TEST
IA - XXXX

2. Stop at End of Test Section

First stop (overflow light on)

(A) = 7422 - test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Section number

(Q) = Return address

3. Stop at End of Test

First stop (overflow light on)

(A) = 7424 - test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Pass number

(Q) = Return address

4. Stop on Error

All error message displays use basically the standard SMM17 error message format. The format of the first two stops is the same for all types of errors. The format of the third and fourth stops is determined by the type of error. The format for the first and second stops is as follows:

First stop (overflow light on)

(A) = 74X8 - test ID stop; where X is the number of stops

(Q) = Stop/Jump parameter

Second stop

(A) = XXYZ where XX = Section number

Y = Buffer number (0-F)

Z = Error type

The buffer designated in Y is actually the same buffer repeated 16 times.

(Q) = Address pointer to where within the communications driver the error occurred.

This pointer is not the same as the return address found in other SMM17 tests. The address points to where execution stopped when the error occurred, but not to where execution will continue after the error. Where execution continues after the error is determined by the repeat condition bit of the Stop/Jump parameter. If the repeat condition bit is set, execution will continue at a backward marker, a recovery point to repeat the buffer designated in (A) of this second stop. If the repeat condition bit is not set, execution will continue at a forward marker, a recovery point to ignore the remainder of the current buffer sequence and to advance to the next buffer.

B. MESSAGE DICTIONARY

The upper hexadecimal digit of the two-digit error message code designates the buffer number that failed. (Each section transfers 16 buffer numbered 0-F). The lower digit of the error message code is the error type. This message dictionary describes the error types.

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X1	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive internal reject A = I/O instruction Q = Q register function code
X2	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive external reject (A) = I/O instruction (Q) = Q register function code
X5	CMPST	CMI010	STATUS, word has unexpected contents A = Actual status Q = Expected status A = Q register function code Q = Previous status
X6	CMPST	CMI010	FWA, first word address register has unexpected contents A = Actual address Q = Expected address A = Q register function code Q = Previous address
X7	CKCORE	CKI130	DATA does not match expected data A = Actual data Q = Expected data A = Word number in buffer (words numbered from 1) Q = Not used
X9	DCIPRO	DCI002	INTERRUPT, internal reject during interrupt state A = I/O instruction Q = Q register function code
XA	DCIPRO	DCI002	INTERRUPT, external reject during interrupt state A = I/O instruction Q = Register function code

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
XB	RINT	RII010	<p>INTERRUPT, end of operation interrupt missing</p> <p>A = Actual interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p> <p>Q = Expected interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p>
XC	DCIPRO	DCI020	<p>INTERRUPT, no interrupt status bit set when an interrupt occurred</p> <p>A = 0000 (actual interrupts)</p> <p>Q = Expected interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p>
XD	DCIPRO	DCI030	<p>INTERRUPT, unexpected</p> <p>A = Actual interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p> <p>Q = Expected interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p>
XE	DCIPRO	DCI069	<p>INTERRUPT, unable to clear interrupt status</p> <p>A = Actual interrupts after attempted clear interrupts Bit 0 for receiver EOP Bit 1 for transmitter EOP</p> <p>Q = 0000 (expected interrupts after attempted clear interrupts)</p>

V DESCRIPTION

A. GENERAL

All sections of this test transmit and receive 16 buffers (numbered 0-F) in link around mode. Each section uses a common driver, but the routine is entered with different patterns prestored and different buffer lengths selected. The first eight bits of each buffer contains the site address. Each buffer sequence (or condition) begins with a

clear function and ends with a check of the repeat condition bit of the Stop/Jump parameter. When the repeat condition bit is set, the buffer number is not advanced.

Both receiver and transmitter end of operation interrupts are enabled.

B. BUFFER LENGTH AND PATTERN DESCRIPTION

The upper eight bits (0X) of the first word of each buffer contains the GPGT site address as defined by a set of address switches located within the display code interpreter.

<u>Number</u>	<u>Transmitter Buffer Length</u>	<u>Receiver Buffer Length</u>	<u>Transmitter Buffer Prestored Pattern</u>
0	1	1	0X00 (zeros)
1	1	1	0XFF (ones)
2	16 ₁₀	16 ₁₀	0X01, 0002, 0004... (one shifted left)
3	16 ₁₀	16 ₁₀	0XFE, FFFD, FFFB... (zero shifted left)
4	256 ₁₀	256 ₁₀	0XAA, 5555, AAAA... (alternate A's/5's)
5	2, 4, 8... 512, 2, 4, 8... 64 (doubling)	2, 4, 8... 512, 2, 4, 8... 64 (doubling)	0X01, 0002, 0003... (word number)
6	Random (maximum of 512 ₁₆)	Same lengths as transmit buffers	Random
7	4, 8, 16... 1024, 4, 8, 16... 128 (doubling-2 times receive buffer)	2, 4, 8... 512, 2, 4, 8... 64 (doubling)	0X01, 0002, 0003... (word number)
8	2, 4, 8... 512, 2, 4, 8... 64 (doubling)	4, 8, 16... 1024 4, 8, 16... 128 (doubling-2 times transmit buffer)	0X01, 0002, 0003... (word number)
9	2	Second word with protect bit set	0XFF, FFF

C. LINK AROUND DRIVER DESCRIPTION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description</u>
	ECHODR	Echo driver
	ECT015	Store BADA throughout receive buffer
	ECI016	Go to common I/O routine
	INOUT	Common I/O routine
XXX1	ECI020	Function receiver clear and link around-
XXX2		expect reply
XXX1		Function transmitter clear and expect reply
XXX2		
XXX5		Input all status and expect receiver status 0001 and transmitter status 0001
XXX1	ECT030	Write receiver FWA and expect reply
XXX2		
XXX1	ECT050	Write receiver LWA and expect reply
XXX2		
XXX1	ECT070	Write transmitter FWA and expect reply
XXX2		
XXX1	ECT080	Write transmitter LWA and expect reply
XXX2		
XXX1	ECT081	Function receiver start, select end of operation interrupt and link around; expect reply
XXX2		
XXX5	ECT090	Input all status and expect receiver status 0003, transmitter status 0001, receiver FWA 0823 plus bias and transmitter FWA 061B plus bias
XXX6		
XXX1		Function transmitter start and select end of operation interrupt and expect reply
XXX2		
XXX9	ECI110	Return control to SMM; wait several seconds for both end of operation interrupts to occur
XXXA		
XXXC		
XXXD		
XXXE		
XXX5	ECI054	Input all status; expect transmitter status 0001 in all sections and receiver status 0001 in all sections except 0401 in Section 7 and 1001 in Section 9
XXX6		
XXXB		Verify that both end of operation interrupts occurred.

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Description</u>
XXX7		Exit common I/O routine
		Compare receive data against transmit data and expect compare
	ECI190	Check repeat condition stop/jump bit

VI QSE10358/QSE6873 DRIVER

Selecting this driver causes the test to write patterns into the QSE6873 Station Buffer Unit (SBU) memory and to read these patterns back to the GPGT memory.

The hardware required to use this driver consists all the hardware required for the link around driver, plus the equipment as follows:

<u>QSE6873</u>	<u>QSE10358</u>
FV241A Station Buffer Unit (SBU)	GG115A Display Code Interpreter with
FV472A SBU Remote Interface (RSBUI)	QSE10358 Communications Interface
DJ156A Five Megabit Modems	

A. OPERATION

Sections 0, 1, 7, 8, and 9 cannot be run using this driver.

Section 10, SBU memory addressing, may be selected by setting bit 10 of the A register during the second stop of a parameter stop. This section writes each SBU memory location with its address, in 512 word blocks.

The PRIORITY switch must be UP when using this driver.

Setting bit 4 (repeat condition) of the Stop/Jump parameter causes the entire section to be repeated.

During an error stop, the contents of A of the second stop is the format XXYZ:

Where XX = Section number

Y = I/O cycle code (instead of buffer number)

6 for SBU reset sequence number

D for SBU write

5 for SBU

Z = Error type

Y does not designate the buffer number as it did in the link around mode of testing.

One additional error type is used by this driver:

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X8	CKRES	CK1210	SBU response word does not match expected A = Actual SBU response word Q = Expected SBU response word A = Command word Q = Not used The following responses are used: XX1X = Accept XX9X = Accept followed by data XX3X = Reject

B. DRIVER SEQUENCE

<u>Error Code</u>	<u>Subroutine Tag Name</u>	<u>Description</u>
	QSEDR	QSE driver
XX61	INOUT	Send SBU resent sequence number and
XX62		read reply (see common I/O routine
XX65		for details
XX66		
XX69		
XX6A		
XX6B		
XX6C		
XX6D		
XX6E		
XX68	CKRES	Check SBU response and expect XX10
	PRESTO	Store BADA throughout receiver buffer
XXD1	INOUT	Send SBU write function followed by data and
XXD2		read reply (see common I/O routine for
XXD5		for details
XXD6		
XXD9		
XXDA		
XXDB		
XXDC		

<u>Error Code</u>	<u>Subroutine Tag Name</u>	<u>Description</u>
XXDD		
XXDE		
XXD8	CKRES	Check SBU response and expect XX1X
XX51	INOUT	Send SBU read function and read response
XX52		followed by data (see common I/O routine
XX55		for details)
XX56		
XX59		
XX5A		
XX5B		
XX5C		
XX5D		
XX5E		
XX58	CKRES	Check SBU response and expect XX1X
XX57	CKCORE	Compare receive data against transmit data and expect compare Repeat SBU write and SBU read 16 times Check repeat condition and repeat section stop/jump bits; repeat section if set

GENERAL PURPOSE GRAPHICS TERMINAL (GPGT)
 COMMUNICATIONS TEST (12-BIT INTERFACE)
 (GT5 Test No. 75)

I INTRODUCTION

The purpose of this test is to verify the operation of the GPGT communications interface. The test operates in link around mode in which the receiver is connected to the output of the transmitter. Since this mode of operation is selected by a software function, no hardware alteration is necessary. The modem interface drivers and receivers are not included in the link around data path. An echo mode may also be selected. In this mode, data is turned around after the modem. On the 358-3 modem, this is accomplished by reversing the loop test connector J2. Also, bit 12 of the Stop/Jump parameter must be set to enable echo mode.

II REQUIREMENTS

A. HARDWARE

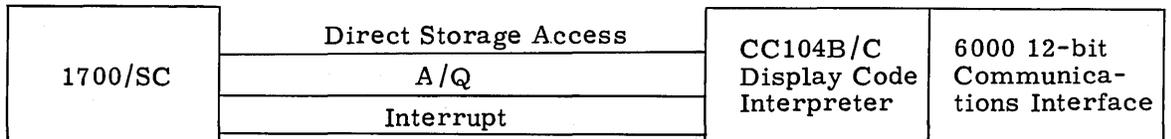
1. Minimum Configuration

<u>1700</u>	<u>System Controller (SC)</u>
1705 Interrupt Data Channel	1772 Magnetic Core Memory Module (4K)
CC104B/C GPGT Console	1775 A/Q Interrupt Data Channel
Input device for SMM17	1773 Direct Storage Access Channel
	CC104B/C GPGT Console
	Input device for SMM17

2. Core Requirements

The minimum amount of core required is 4K.

3. Equipment Configuration



B. SOFTWARE

The test operates under control of the SMM17 monitor.

C. ACCESSORIES

None

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 75 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

First stop (overflow light on)

(A) = 7521 test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Section selection bits (prestored as 003F)

Bit 0 = Section 0 - Zeros

1 = Section 1 - Ones

2 = Section 2 - Shifting one

3 = Section 3 - Shifting zero

4 = Section 4 - Complements

5 = Section 5 - Random

6 = Section 6 - Protect/parity error/CRC character check

7 = Section 7 - Terminate buffer

8 = Section 8 - Test mode

(Q) = Interrupt line for communications interface (prestored as 0008)

2. Data Terminal Switch Setting

The DATA TERMINAL IN switch must be UP.

The PROTECT switch must be DOWN (except during portions of Section 6).

The PRIORITY switch must be DOWN.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters

1 - Stop at end of test section

2 - Stop at end of test

3 - Stop on error

4 - Repeat condition (buffer)

5 - Repeat section

6 - Repeat test

- Bit 7 - Not used
- 8 - Omit typeouts
- 9 - Bias return address display
- 10 - Re-enter parameters
- 11 - Communicate with 1700 host
- 12 - Echo through modem
- 13 -
- 14 -
- 15 -

Bits 11 and 12 must not be set at the same time.

C. SECTION DESCRIPTION INDEX

<u>Section Number</u>	<u>Name</u>	<u>Run Time</u>
0	Zeros	Less than 1 second
1	Ones	Less than 1 second
2	Shifting one	Less than 1 second
3	Shifting zero	Less than 1 second
4	Complements	Less than 1 second
5	Random	Less than 1 second
6	Protect	Less than 1 second
7	Terminate buffer	Less than 1 second
8	Test mode	Less than 1 second

IV OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Messages

Program identification during test initialization.

GT5 (No. 75) GPGT COMMUNICATIONS TEST
IA = XXXX

Section 6 Instructions Typeout

Stop Q = 61, Set 1700 PROTECT switch

Stop Q = 62, Set EQUIPMENT PROTECT switch

Stop Q = 63, Clear PROTECT switches

Stop Q = 6E, Clear PROTECT switches to report error

Section 8 Instructions Typeout

Set test mode switches

Clear test mode switches

2. Operator Intervention Stops

An operator intervention stop is identified by an ID word of 751F in the A register. The Q register contains a code to designate what operation the operator must perform.

(A) = 751F - Test ID word

(Q) = 0061 - Operator must place the 1700 PROTECT switch to the PROTECT position

(A) = 751F - Test ID word

(Q) = 0062 - Operator must place the PROTECT switch on the communications interface to the PROTECT position

(A) = 751F - Test ID word

(Q) = 0063 - Operator must place the 1700/communications PROTECT switches to the NON-PROTECT positions

(A) = 751F - Test ID word

(Q) = 006E - Operator must clear the 1700/communications PROTECT switches and hit RUN. An error stop, if selected, will follow this stop

(A) = 751F - Test ID word

(Q) = 0081 - Operator must place both TEST MODE switches on the communications interface to a position other than OFF

(A) = 751F - Test ID word

(Q) = 0082 - Operator must place both TEST MODE switches on the communications interface to the OFF position

3. Stop at End of Test Section

First stop (overflow light on)

(A) = 7522 - Test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Section number

(Q) = Return address

4. Stop at End of Test

First stop (overflow light on)

(A) = 7524 - Test ID stop

(Q) = Stop/Jump parameter

Second Stop

(A) = Pass number

(Q) = Return address

5. Stop On Error

All error message displays use basically the standard SMM17 error message format. The format of the first two stops is the same for all types of errors. The format of the third and fourth stops is determined by the type of error. The format for the first and second stops is as follows:

First stop (overflow light on)

(A) = 75X8 - Test ID stop

Where X is the number of stops

(Q) = Stop/Jump parameter

Second stop

(A) = XXYZ where XX = Section number

Y = Buffer number (Sections 0-5)

Z = Error type

The buffer designated in Y is actually the same buffer repeated 16 times in Sections 0-5. In Sections 6-8, Y is always zero except for several special cases of error type 6 and 7.

(Q) = Address pointer to where within the communications driver the error occurred.

This pointer is not the same as the return address found in other SMM17 tests. The address points to where execution stopped when the error occurred, but not to where execution will continue after the error. Where execution continues after the error is determined by the repeat condition bit of the Stop/Jump parameter. If the repeat condition bit is set, execution will continue at a backward marker, a recovery point to repeat the buffer designated in (A) of this second stop. If the repeat condition bit is not set, execution will continue at a forward marker, a recovery point to ignore the remainder of the current buffer sequence and to advance to the next buffer.

B. MESSAGE DICTIONARY

The upper hexadecimal digit of the two-digit error message code designates the buffer number that failed in sections 0-5. (Sections 0-5 transfer 16 buffers numbered 0-F.) In Sections 6-8, the upper hexadecimal digit is always zero except for several special cases of error type 6 and 7. The lower digit of the error message code is the error type. This message dictionary describes the error types including the special cases of error type 6 and 7.

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
X1	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive internal reject A = I/O instruction Q = Q register equipment address
X2	FNRP STRP	FNI110 STI100	RESPONSE, expect reply, receive external reject A = I/O instruction Q = Q register equipment address
X3	FNRP STRP	FNI230 STI220	RESPONSE, expect external reject, receive internal reject A = I/O instruction Q = Q register equipment address
X4	FNRP STRP	FNI200 STI200	RESPONSE, expect external reject, receive reply A = I/O instruction Q = Q register equipment address
X5	CMPST	CMI010	STATUS, word has unexpected contents A = Actual status Q = Expected status A = Q register equipment address Q = Previous status
X6	CMPST	CMI010	FWA, first word address register has unexpected contents A = Actual address Q = Expected address A = Q register equipment address Q = Previous address
Special case of error type 6 in Section 7.			
0716	S7I150 S7I170	S7I005	FWA register out of expected range after terminate buffer A = Actual address Q = Q register station and director bits A = Starting address of buffer Q = Last word address plus one of buffer
X7	CKCORE	CKI130	DATA does not match expected data A = Actual data Q = Expected data A = Word number in buffer (words numbered from 1) Q = Not used

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
Special cases of error type 7 in Section 6.			
0617	PPI220	PPFAIL	PROTECTED location altered by receive operation when 1700 PROTECT switch is on and command is not protected A = Actual data Q = Expected data (OBAD) A = Word number in buffer Q = Not used
0627	PPI250	PPFAIL	CRC received incorrect A = Actual CRC Q = Expected CRC A = Word number in buffer (0065) Q = Not used
X8	CKCORE	CKI140	DATA stored beyond receive buffer LWA A = Data stored in location following the end of the receive buffer Q = Address of buffer overflow
X9	DCIPRO	DCI002	INTERRUPT, internal reject during interrupt state A = I/O instruction Q = Q register function code
XA	DCIPRO	DCI002	INTERRUPT, external reject during interrupt state A = I/O instruction Q = Q register function code
XB	RINT	RII010	INTERRUPT, missing A = Actual receiver interrupts (bits corresponding to receiver status bits) Q = Expected receiver interrupts (bits corresponding to receiver status bits) A = Actual transmitter interrupts (bits corresponding to transmitter status bits) Q = Expected transmitter interrupts (bits corresponding to transmitter status bits)

<u>Code</u>	<u>Subroutine Name</u>	<u>Subroutine Tag Name</u>	<u>Message and Description</u>
XC	DCIPRO	DCI020	<p>INTERRUPT, no interrupt status bit set when an interrupt occurred</p> <p>A = Actual receiver status when interrupt occurred</p> <p>Q = Expected receiver interrupts (bits corresponding to receiver status bits)</p> <p>A = Actual transmitter status when interrupt occurred</p> <p>Q = Expected transmitter interrupts (bits corresponding to transmitter status bits)</p>
XD	DCIPRO	DCI030	<p>INTERRUPT, unexpected</p> <p>A = Actual receiver status when interrupted</p> <p>Q = Expected receiver interrupts (bits corresponding to receiver status bits)</p> <p>A = Actual transmitter status when interrupt occurred</p> <p>Q = Expected transmitter interrupts (bits corresponding to transmitter status bits)</p>
XE	DCIPRO	DCI069	<p>INTERRUPT, unable to clear interrupt status</p> <p>A = Actual receiver status after attempted clear interrupts</p> <p>Q = 0000 (expected interrupts after attempted clear interrupts)</p> <p>A = Actual transmitter status after attempted clear interrupts</p> <p>Q = 0000 (expected interrupts after attempted clear interrupts)</p>

V DESCRIPTION

A. GENERAL

Sections 0-5 of this test transmit and receive 16 buffers (numbered 0-F) in link around mode or echo mode. Sections 0-5 use a common driver, but the routine is entered with different patterns prestored. Each buffer sequence (or condition) begins with a terminate buffer and ends with a check of the repeat condition bit of the Stop/Jump parameter. When the repeat condition bit is set, the buffer number is not advanced. Both receiver and transmitter end of operation interrupts are enabled.

Sections 6-8 test portions of the communications interface are not necessarily required in normal data transfers. Section 6 and 8 require manual operations to be performed by the operator. Sections 6 and 7 may generate special cases of error types 6 and 7.

B. BUFFER LENGTH AND PATTERN DESCRIPTION

<u>Section Number</u>	<u>Transmitter Buffer Length</u>	<u>Receiver Buffer Length</u>	<u>Transmitter Buffer Prestored Pattern</u>
0	100	100	0000 (zeros)
1	100	100	0FFF (ones)
2	100	100	0001, 0002, 0004 (one shifted left)
3	100	100	0FFE, 0FFD, 0FFB (zero shifted left)
4	100	100	0AAA, 0555, 0AAA (alternate A's/5's)
5	100	100	Random
6	100	101	0FFE, 0FFD, 0FFB.... (zero shifted left)
		(first word with protect bit set and last word CRC character)	
7	100 (buffer is terminated)	100 (buffer is terminated)	0000, 0001, 0002 (incrementing count)
8	No data is transferred		

C. LINK AROUND/ECHO DRIVER DESCRIPTION (used by Sections 0-5)

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	ECHODR	Start of driver
	ECT015	Store 0BAD throughout receive buffer
	ECI016	Go to common I/O routine (INOUT)

	INOUT	Start of common I/O routine
XXX1	INI010	Terminate receive buffer-expect reply
XXX2		
XXX1	INI020	Terminate transmit buffer-expect reply
XXX2		

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
XXX1	INI030	Function receive clear (and select link around if
XXX2		Stop/Jump bits 11 and 12 equal zero). Expect reply
XXX1	INI040	Function transmitter clear and expect reply
XXX2		
XXX1	INI050	Input all status and compare against expected
XXX2		
XXX5		
XXX6		
XXX1	INI160	Function receiver end of operation interrupt select.
XXX2		Expect reply
XXX1	INI170	Write receiver FWA and expect reply
XXX2		
XXX1	INI180	Write receiver LWA and expect reply
XXX2		
XXX1	INI190	Write transmitter FWA and expect reply
XXX2		
XXX1	INI200	Write transmitter LWA and expect reply
XXX2		
XXX1	INI210	Input all status and compare against expected
XXX2		
XXX5		
XXX6		
XXX1	INI220	Function receiver end of operation interrupt select, alarm
XXX2		interrupt select and start. Expect reply
XXX3	INI230	Attempt function receiver clear. Expect external reject
XXX4		
XXX1	INI240	Input all status and compare against expected
XXX2		
XXX5		
XXX6		
XXX1	INI250	Function transmitter end of operation interrupt,
XXX2		alarm interrupt, and start. Expect reply
XXX9	INI260	Wait for transmitter and receiver EOP interrupts
XXXA		
XXXC		
XXXD		
XXXE		

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
XXX1	INI290	Input all status and compare against expected
XXX2		
XXX5		
XXX6		
XXXB	INI300	Verify that both transmitter and receiver end of operation interrupts occurred EXIT INOUT (return to ECHODR)

XXX7	CKCORE	Compare receive data against transmit data
XXX8		
	ECI190	Check repeat condition stop/jump bit

D. SECTION 6 DESCRIPTION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	PPI020	Store shifting zero bit pattern into transmit buffer
	PPI024	Store 0BAD into receive buffer. Set protect bit of first word of receive buffer
0601	PPT030	Write receiver FWA and expect reply
0602		
0601	PPT040	Write receiver LWA and expect reply
0602		
0601	PPT050	Write transmitter FWA and expect reply
0602		
0601	PPT060	Write transmitter LWA and expect reply
0602		
0601		Function receiver link around (if stop/jump bits 11 and 12 equal zero). Expect reply
0602		
	PPI070	Typeout Section 6 operation instructions and stop with A = 751F and Q = 0061 Operator must place 1700 PROTECT switch in the PROTECT position and place the RUN/STEP switch to RUN
0601	PPI080	Function receiver start and expect reply
0602		
0601	PPI090	Function transmitter start and expect reply
0602		
	PPI200	Wait receiver not busy

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
0601	PPI110	Input all status and compare against expected
0602		
0605		
0606		
	PPI150	Stop with A = 751F and Q = 0062 Operator must place the communications interface PROTECT switch in the PROTECT position and place the 1700 RUN/STEP switch to RUN
0601	PPI160	Input all status and compare against expected
0602		
0605		
0606		
0603	PPI180	Attempt unprotected function receiver clear.
0604		Expect external reject
0603		Attempt unprotected function receiver write FWA.
0604		Expect external reject
0603		Attempt unprotected function receiver write LWA.
0604		Expect external reject
0603		Attempt unprotected function transmitter clear.
0604		Expect external reject
0603		Attempt unprotected function transmitter write FWA.
0604		Expect external reject
0603		Attempt unprotected function transmitter write LWA.
0604		Expect external reject
0617	PPI220	Check if protected location was altered by receive operation when 1700 PROTECT switch on and command not protected
0627	PPI250	Check for correct CRC character received
	PPI290	Stop with A = 751F and Q = 0063 Operator must place both the 1700 and communication interface PROTECT switches in the non-protect position and place the 1700 RUN/STEP switch in RUN
	PPI310	Check repeat condition Stop/Jump parameter bit

E. SECTION 7 DESCRIPTION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	S7I005	Store incrementing count in each location of transmit buffer
	S7I024	Store 0BAD throughout read buffer
0701	S7I030	Function receiver write FWA and expect reply
0702		
0701	S7I040	Function receiver write LWA. Expect reply
0702		
0701	S7I050	Function transmitter write FWA. Expect reply
0702		
0701	S7I060	Function transmitter write LWA. Expect reply
0702		
0701		Function receiver link around (if Stop/Jump parameter bits 11 and 12 equal zero). Expect reply
0702		
0701	S7I064	Function receiver start. Expect reply
0702		
0701	S7I090	Function transmitter start. Expect reply
0702		
	S7I110	Wait a short delay to approximately midpoint of buffers
0701	S7I120	Function receiver terminate buffer. Expect reply
0702		
0701	S7I126	Function transmitter terminate buffer. Expect reply
0702		
0701	S7I128	Input all status and compare against expected
0702		
0705		
0706		
0716	S7I150	Check that receiver FWA is within expected range after terminate buffer
0716	S7I170	Check that transmitter FWA is within expected range after terminate buffer
0708	S7I190	Check that data is not stored beyond receive buffer LWA
	S7I200	Check repeat condition Stop/Jump parameter bit

F. SECTION 8 DESCRIPTION

<u>Error Code</u>	<u>Program Tag Name</u>	<u>Program Description</u>
	S8I005	Typeout SET TEST MODE switches and stop with A= 751F and Q = 0081 Operator must place both communications interface TEST MODE switches to a position other than OFF and place the 1700 RUN/STEP switch to RUN
0801		Input all status and compare against expected
0802		
0805		
0806		
0803		Attempt function receiver clear. Expect external reject
0804		
0803		Attempt function transmitter clear. Expect external reject
0804		
	S8I105	Typeout CLEAR TEST MODE switches and stop with A = 751F and Q = 0082 Operator must place both communications interface TEST MODE switches to the OFF position and place the 1700 RUN/STEP switch to RUN
	S8I200	Check repeat condition Stop/Jump parameter bit

VI APPLICATIONS

A. GENERAL

In Sections 0-5, all buffers are set up for 100 words. However, if buffers of varying lengths are needed, the desired buffer lengths may be manually entered into 16 consecutive locations starting at the address tag called LTBL. The buffer lengths must be in the range 1-100 decimal (or 1-64 hexadecimal). Care should be taken to ensure that the 17th word from LTBL remains a zero. The word of zeros terminates the table of buffer lengths. Without the word of zeros, false errors will occur.

B. HUNG CONDITIONS

If the test hangs or seems to be lost, the 1700 should be stepped to halt all action. Then, the computer registers, TV monitor, and certain program location should be observed to help define the problem.

NOTE

Do not master clear the computer. If the computer is master cleared, much of the TV monitor information will also be cleared. Memory locations may be observed without master clearing. This is done by clearing P with the register clear button, setting P to the desired address, placing the ENTER/SWEEP switch to SWEEP, stepping the RUN/STEP switch once, and observing the X register.

The test's section number is found in location BET120. If Sections 0-5 were running, locations BFRNUM and CURL will contain the current buffer number (0-F) and the current buffer length respectively. The starting address of the receive buffer is stored in location ADRBUF and the starting address of the transmit buffer is stored in location ADWBUF.

The last two copies of receiver status, transmitter status, receiver current word address, and transmitter current word address are stored in word pairs at locations ST0, ST1, FWA0, and FWA1 respectively. To determine which of the word pair is the most recent, location RAP000 must be examined. If RAP000 equals 0000, the first word of the word pair is the most recent. If RAP000 equals 0001, the second word of the word pair is the most recent.

GENERAL PURPOSE GRAPHICS TERMINAL (GPGT)
 DESIGN SPECIFICATION VERIFICATION TEST
 (GT6 Test No. 76)

I INTRODUCTION

The purpose of this test is to verify that the GPGT meets certain design specifications. This test checks vector volume, character volume, light pen field of view, and light pen tracking rate. Patterns are selected on the keyboard.

II REQUIREMENTS

A. HARDWARE

1. Minimum Configuration

1700

1705 Interrupt Data Channel
 CC104A/B/C GPGT Console
 CA122A Keyboard
 Input device for SMM17

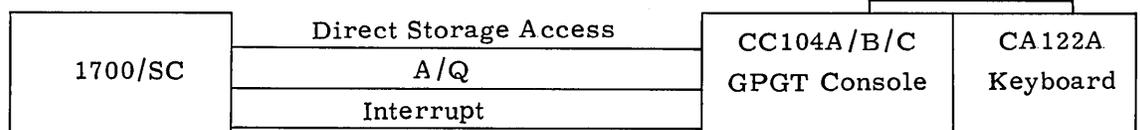
System Controller

1772 Magnetic Core Memory Module (8K)
 1775 A/Q Interrupt Data Channel
 1773 Direct Storage Access Channel
 CC104A/B/C GPGT Console
 CA122A Keyboard
 Input device for SMM17

2. Core Requirements

The minimum amount of core required is 8K.

3. Equipment Configuration



B. SOFTWARE

The test operates under control of SMM17 monitor.

C. ACCESSORIES

None

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The test is loaded as test number 76 using standard SMM17 loading procedure.

B. PARAMETERS

1. Parameter Stops

Parameters cannot be changed after the initial parameter stop.

First stop (overflow light on)

(A) = 7621 test ID stop

(Q) = Stop/Jump parameter

Second stop

(A) = Interrupt line for display code interpreter (prestored as 0004-bit 2 designating interrupt line 2)

(Q) = Power line frequency (prestored as 0060_{16}) For 60-cycle input power, set to 0060_{16} . For 50-cycle input power, set to 0050_{16} .

2. DCI Switch Setting

DCI instruction/clock control switches must be UP. The DCI PROTECT switch must be in UNPROTECTED. The DCI SENSE REFRESH FAULT switch must be DOWN.

3. Stop/Jump Parameter Word

Bit 0 - Stop to enter parameters

1 - Not sensed by this test

2 - Not sensed by this test

3 - Not sensed by this test

4 - Not sensed by this test

5 - Not sensed by this test

6 - Not sensed by this test

7 - Not used

8 - Omit typeouts

9 - Not sensed by this test

10 - Not sensed by this test

11 - Not sensed by this test

12 - Not sensed by this test

13 - Not sensed by this test

14 - Not sensed by this test

15 - Not sensed by this test

C. PATTERN DESCRIPTION INDEX

<u>Number</u>	<u>Name</u>
1	Short Vector Mode 1/2 Inch Vector Volume

<u>Number</u>	<u>Name</u>
2	Short Vector Mode 2 Inch Vector Volume
3	Short Vector Mode 8 Inch Vector Volume
4	Two Word 1/2 Inch Vector Volume
5	Two Word 2 Inch Vector Volume
6	Two Word 8 Inch Vector Volume
7	Three Word 1/2 Inch Vector Volume
8	Three Word 2 Inch Vector Volume
9	Three Word 8 Inch Vector Volume
10	Symbol Volume
11	Light Pen Field of View
12	Light Pen Tracking Rate

IV OPERATOR COMMUNICATIONS

A. MESSAGE FORMATS

1. Normal Teletype Message

Program identification during test initialization.

GT6 (No. 76) GPGT SPEC VERIFICATION TEST
IA = XXXX

2. Normal Display Console Message

Displayed at the console after the teletype message and during pattern selection.

PATTERN NUMBERS 1 = SVM HALF INCH VECTORS,
2 = SVM TWO INCH VECTORS.

TO SELECT PATTERN, TYPE PTN/pattern number ETX FUNCT _____

3. Error Messages

No error messages are used. Displays must be visually checked.

B. MESSAGE DICTIONARY

Not applicable.

V DESCRIPTION

A. GENERAL

This test allows the selection of specification verification patterns. These patterns are called by typing pattern numbers on the display console keyboard. Initially the display is as follows:

PATTERN NUMBERS 1 = SVM HALF INCH VECTORS, 2 = SVM TWO INCH VECTORS.....

TO SELECT PATTERN, TYPE PTN/pattern number ETX FUNCT—
LOWER CASE ON KEYBOARD MUST BE SELECTED.

Upper case codes from the keyboard are ignored.

Depressing the first key of a pattern selection type-in causes any previous pattern to stop being displayed and the pattern selection display with cursor to be displayed instead. That first symbol is displayed following the FUNCT and the cursor is advanced one space. Each symbol of the type-in is displayed and the cursor advanced until an ETX terminates the type-in. If an error is made while typing the function, depress BACKSPACE and correct the error. Illegal keys are ignored. Illegal pattern selections are discarded and the cursor replaced following the FUNCT.

B. DISPLAY A PATTERN (PTN/)

Type: PTN/n ETX
Where n is the pattern number

C. SELECT A NEW SYMBOL FOR PATTERN 10 (SYM/)

Type: SYM/s ETX
Where s is the desired symbol

D. TERMINATE THE TEST (END/)

Type: END/ETX

CAUTION

This termination procedure is necessary to ensure the proper execution of other GPGT tests to be run. Locations changed in SMM are restored to their proper values.

E. PATTERN DESCRIPTIONS

1. Short Vector Mode 1/2 Inch Vector Volume

This pattern is used to calculate the number of 1/2 inch vectors that can be drawn in one refresh time using short vector mode draw instructions. The result is displayed to the left of the vector pattern. Approximately 7 percent is added to the result to cover overhead time used in the display file and in setting up the display file.

2. Short Vector Mode 2 Inch Vector Volume

This pattern is used to calculate the number of 2 inch vectors that can be drawn in one refresh time using short vector mode draw instructions. The result is displayed to the left of the vector pattern. Approximately 5 percent is added to the result to cover overhead time used in the display file and in setting up on the display file.

3. Short Vector Mode 8 Inch Vector Volume
This pattern is used to calculate the number of 8 inch vectors that can be drawn in one refresh time using short vector mode draw instructions. The result is displayed to the left of the vector pattern.
4. Two-Word 1/2 Inch Vector Volume
This pattern is used to calculate the number of 1/2 inch vectors that can be drawn in one refresh time using two-word (DVXY) draw instructions. The result is displayed to the left of the vector pattern. Approximately 1 percent is added to the result to cover overhead time used in the display file and in setting up the display file.
5. Two-Word 2 Inch Vector Volume
This pattern is used to calculate the number of 2 inch vectors that can be drawn in one refresh time using two-word (DVXY) draw instructions. The result is displayed to the left of the vector pattern.
6. Two-Word 8 Inch Vector Volume
This pattern is used to calculate the number of 8 inch vectors that can be drawn in one refresh time using two-word (DVXY) draw instructions. The result is displayed to the left of the vector pattern. Approximately 1 percent is added to the result to cover overhead time used in the display file and in setting up the display file.
7. Three-Word 1/2 Inch Vector Volume
This pattern is used to calculate the number of 1/2 inch vectors that can be drawn in one refresh time using three-word (DVR) draw instructions. The result is displayed to the left of the vector pattern.
8. Three-word 2 Inch Vector Volume
This pattern is used to calculate the number of 2 inch vectors that can be drawn in one refresh time using three-word (DVR) draw instructions. The result is displayed to the left of the vector pattern.
9. Three-Word 8 Inch Vector Volume
This pattern is used to calculate the number of 8 inch vectors that can be drawn in one refresh time using three-word (DVR) draw instructions. The result is displayed to the left of the vector pattern.
10. Symbol Volume
This pattern is used to calculate the number of symbols that can be drawn in one refresh time. The result is displayed to the left of the symbol pattern. A percentage is added to the result to cover overhead time used in the display file. This percentage varies from symbol to symbol. The prestored symbol pattern contains the symbol A (code 41).

11. Light Pen Field of View

This pattern is used to examine the field of view of the light pen. The pattern consists of two small squares. On the left the larger square is formed by hundreds of short vectors illuminating its entire area. On the right the smaller square is formed by four .1287-inch perimeter vectors. To examine the field of view, the light pen is brought near the larger square. Each vector sensed by the light pen is also drawn at the right near the smaller square. Thus, an exact image of what the light pen sees appears over the smaller square. When the field of view is correct, the image should fit within the smaller square.

12. Light Pen Tracking Rate

This pattern is used to calculate the light pen tracking rate at which the light pen is lost. After selecting this pattern from the keyboard, the light pen switch must be depressed to activate light pen tracking. To force a tracking rate calculation, the light pen must first be lost. The light pen is considered lost when the tracking routine enters into a full screen raster search. Speedy light pen motions with sudden changes in direction are necessary to lose the light pen. When the light pen is lost, the rate at which it was moving is displayed near the top of the screen. If the light pen switch was released during the loss of the light pen, the switch must be depressed to again activate tracking and to display the rate at which the light pen was lost.

CAUTION

Tracking rates displayed as a result of a released light pen switch should be considered inaccurate.

1735/915 OPTICAL CHARACTER READER TEST
(OCR035 Test No 35)

I. OPERATING INSTRUCTIONS

A. RESTRICTIONS

1. Bit 2 of SMM Parameter must be set if running on an SC1700.
2. Due to timing differences between computer mainframes, any message indicating a 1735/915 timing problem may be a mainframe fault. In cases where timing is critical the test does not attempt to interpret the error. Rather an informative message is displayed.
3. All sections of the test except Section 6 will run with only the system interrupt line connected. To run Section 6, both the system interrupt line and the manual interrupt line must be connected.
4. Sections 4 and 6 require manual intervention and are not normally selected.
5. In Section 6, change the reader from Ready to Not Ready by alternately pressing the Start and Stop switches with a document at the Document Ready operation.
6. In Section 4, two stops will occur after typeouts. After setting or clearing the proper switches the computer must be placed in RUN to continue testing.
7. Test requires minimum of 8K to run.

B. LOADING PROCEDURE

1. Call as external test number 35 under SMM17.
2. The following documents are required to run the test:
 - a. Section 0. Two documents of any type are required.
 - b. Section 1. Seven documents of any type are required.
 - c. Section 2. Thirty documents of any type are required.
 - d. Section 3. One document of any type is required.
 - e. Section 4. One document of any type is required.
 - f. Section 5. Six documents, Pub. No. 60217516, are required. These documents are of nominal stroke width, pitch and skew. Spacing is six lines per inch.

- g. Section 6. One document of any type is required.
- h. Section 7. One document of any type is required.
- i. Section 8. This is the general read routine. The machine should be capable of reading any of the following documents.

Pub. No.

- 1) 60217502
- 2) 60217503
- 3) 60217504
- 4) 60217505
- 5) 60217506
- 6) 60217507
- 7) 60217508
- 8) 60217509
- 9) 60217510
- 10) 60217511
- 11) 60217512
- 12) 60217513
- 13) 60217514
- 14) 60217515

See the General Specifications of test documents (Pub. No. 60217500) for a description of the above documents. Eighteen documents are required for one pass of Section 8.

- j. Section 9. Sixteen documents of Pub. No. 60217511 are required.
- k. Section A. Two documents having Line Locate bars along the left margin are required.
- l. Section B. Two documents having Line Locate bars are required.

C. PARAMETERS

If bit 0 of the SMM Stop/Jump parameter is set at the start of the test, a parameter stop occurs. If bits 10 and 0 are set, parameters may be re-entered at the end of each section and at the end of a pass through the test.

1. First Stop, A = 3541, Q = Stop/Jump parameter.

The Stop/Jump parameter may be changed if desired.

2. Second Stop, A = 079F₁₆, Q = 21₁₆. The bits in the A register specify the pre-selected sections to run; bit 0 implies section 0, bit 1 implies section 1, bit 10 implies section A, etc. The sections selected may be changed as desired.

The bits in Q are a word count parameter prestored as 21₁₆.

If the 915 has a serial number below 100 and has not been modified to read the entire Rabinow character set, this parameter must be changed to 1F₁₆.

3. Third stop, A = 0040, Q = 0080. The bit in the A register specifies the system interrupt line (data, end-of-operation and alarm). The bit in the Q register specifies the manual interrupt line. Both the system and manual interrupt lines must be connected to run Section 6. All other sections will run with only the system interrupt line connected. These interrupt line bits may be changed if desired.
4. Fourth stop, A = BA29₁₆, Q = 0000. The A register contains the read coordinates used by the test.

D. MESSAGES

No typeouts occur if bit 8 of the Stop/Jump parameter is set.

1. Test title and initial address of the test.

1700/SC - 1735/915 OCR035 TEST

IA = XXXX

XXXX is the starting address where the test is loaded in memory.

2. Low-Speed Mirror Timing is typed out in Section 3 as follows:

MIRROR FWD TIMING

AVERAGE = 0316, MAXIMUM = 0320, MINIMUM = 0305

* MIRROR REVR TIMING**

AVERAGE = 0083, MAXIMUM = 0086, MINIMUM = 0081

Given times are in decimal. The average forward time should be 316₁₀ milliseconds $\pm 4\%$ (acceptable limits: 304₁₀ MS \leq FWRD Time \leq 330 MS).

The average reverse time should be 81_{10} MS $\pm 4\%$ (Acceptable limits: 77_{10} MS \leq REVRS Time 85_{10} MS). Forward time is computed based on $F0_{16}$ is started with the mirror already moving.

WARNING

The 1700 and SC1700 do not have internal clocks and, therefore, all computed times are based on instruction cycle times. A "slow" 1700 will shorten the above times; a "fast" 1700 will lengthen the above times. All average times outside the above limits should be investigated. (The test takes into account the longer cycle times of an SC1700.)

3. Actual data and expected data typeouts in case of data compare errors. This typeout may be omitted by setting bit 7 of the Stop/Jump parameter. This typeout may occur in Sections 5, 8, 9 or C.

A. D* yyyyyyyyyyyy
 Where yyyy is the actual data read.

E. D* zzzzzzzzzzzz xxx zzz \backslash ss \backslash
 Where zzzz zzz is the expected data pattern.
 xxxx specifies those cases where expected data cannot be predicted;
 e. g., when reading the entire character set in Alpha mode, the numeric characters may be read as rejects or as some alpha character.

\backslash is current printer character for a field mark (DC_{16}). Where SS indicates space codes. (Spaces in A. D* line are actual spaces.)

4. Section 4. These typeouts instruct to operator to Set or Clear the Protect switches.

SET PROTECT SWITCH ON 1735
 SET 1704 PROTECT SWITCH - RUN
 CLEAR 1704 AND 1735 PROTECT SWITCHES - RUN

5. Section 6. These typeouts are used when checking the End-of-File status, manual interrupt and alarm interrupt.

SET AND CLEAR EOF SWITCH 10 TIMES.
 Sets EOF status and causes manual interrupt.
 PRESS START, THEN STOP SWITCH 10 TIMES.
 Sets alarm status and causes alarm interrupt.

6. End of Test Timeout

A	Q	A	Q
35X4	S/J Parameter	Pass Number	Return Address

X = Number of stops

7. Error Messages

a. All error messages are in the format specified by SMM17:

A	Q	A	Q
35X8	S/J Parameter	0yzz	Return Address

x = Number of stops (if any) or number of pairs of words typed (if any)

y = Section number

zz = Error code

Additional information is given, depending on the type of error, if X (number of stops) is greater than 2. See description of error codes below.

b. Error Codes

An error code is displayed in the lower two digits of the A register on the second stop of all error stop sequences. A description of the error codes used and the additional information displayed on each error is described below.

<u>Error Code (Hex.)</u>	<u>Description</u>
01	Ready status not set A = Equipment status Q = 0000
02	Busy status not set A = Equipment status Q = 0000
03	An interrupt occurred but the interrupt status bit is not set A = Equipment status Q = 0000

<u>Error Code (Hex.)</u>	<u>Description</u>
04	The time required to sort one document exceeded 1800 ms. A = Sort time in ms Hex. Q = 0000
05	Incorrect equipment status A = Actual status Q = Expected status
06	Incorrect mirror status A = Actual status Q = Expected status
07	An interrupt occurred. Interrupt status bit was set but none of the following were set - data, end of operation, alarm or manual interrupt. A = Equipment status Q = 0000
08	An interrupt occurred which had not been selected. A = Equipment status Q = Interrupt select bits for selected interrupts
09	A clear interrupt function did not clear the interrupt status bit. A = Equipment status Q = 0000
0A	Line Locate did not occur within 300 ms A = Actual status Q = Expected
0B	The character read was "out of mode." Example: Reading in alpha mode and a numeric character is read. A = Number of "out of mode" characters in the line just read Q = 0000

<u>Error Code (Hex.)</u>	<u>Description</u>
0C	External reject on a status input A = 0000 Q = Equipment address
0D	Internal reject on a status input A = 0000 Q = Equipment address
0E	External reject of a function A = Function code(s). Q = Equipment address
0F	Internal reject of a function A = Function code(s) Q = Equipment address
10	Stop read function did not clear busy status A = Equipment status Q = 0000
11	Space code-field mark data compare error. Expected 7 spaces 2 field marks and a fill character. Actual and expected data type-out follows error message. A = Number of errors (i. e. , number of characters not found) Q = 0000
12	Protect switches were set but a reply was received to a nonprotected 1735/915 function. A = Function code Q = 0000
13	An incorrect equipment code or interrupt line parameter was entered. Run to re-enter parameters.

Error Code (Hex.)

Description

14	<p>Incorrect mirror coordinate. After mirror motion the mirror coordinate was not the one expected.</p> <p>A = Actual mirror status Q = Expected mirror coordinate</p>
15	<p>Mirror compare failed. After mirror motion, mirror compare status was not set.</p> <p>A = Actual mirror status Q = Expected mirror coordinate</p>
16	<p>Coordinate drift. The coordinate at which the character was read was not within \pmtwo of the expected coordinate.</p> <p>A = Actual coordinate Q = Expected coordinate</p>
17	<p>Selected interrupt did not occur.</p> <p>A = Function bits for selected interrupt Q = Function bits for actual interrupt</p>
18	<p>Reject of a protected function. Protect switches set on 1735 and 1704.</p> <p>A = Function code Q = 0000</p>
19	<p>Data compare error. Data read did not match expected data.</p> <p>A = Number of data compare errors detected in the line just read (See I.D.2 for data typeouts.) Q = 0000</p>
1A	<p>Reader Ready - should not be. To start Section 6, the reader must be in a not ready condition.</p>

<u>Error Code (Hex.)</u>	<u>Description</u>
1B	End of File status did not set when End of File switch was pressed. A = Equipment status Q = 0000
1D	Mechanical counter Busy status did not set after a counter function. A = Counter function Q = 0000
1E	Page advance error and/or mirror coordinate error occurred after executing a page advance function. Could not find the expected character or could not find line after page advance. (Note: Odd page advance functions are executed twice.) A = 000X Where X is the number of lines the page was advanced prior to the error (1FX is odd 2X). Q = 00YY Where YY as the coordinate at which it expected to find a character.

E. ERROR STOPS

Stops occur upon errors if bit 3 of the Stop/Jump parameter is set. At least two stops occur. Additional stops may occur depending upon the type of error.

II. DESCRIPTION

A. INITIALIZATION

1. Calculate and store bias value
2. Type test title
3. Store last address of test in SMM
4. Enter parameters if selected in Stop/Jump word
5. Bias address of interrupt processing routine

6. Request interrupt lines from SMM
7. Go to control routine and start test

Section 0 (S0). Check for a reply to 1735/915 functions. Status must be Ready and Not Busy. Error if internal or external reject.

B. OPERATING MODE FUNCTION (D = 1)

1. Clear controller
 2. Clear interrupts
 3. Data interrupt request
 4. End of operation interrupt request
 5. Alarm interrupt request
 6. Stop read
 7. Manual interrupt request
 8. Increment mechanical counter No. 1
 9. Increment mechanical counter No. 2
 10. Increment mechanical counter No. 3
 11. Clear mechanical counter No. 1
 12. Clear mechanical counter No. 2
 13. Clear mechanical counter No. 3
- Repeat from (A) 1, 000 times

C. DATA MODE FUNCTIONS (D = 2)

1. Clear controller
 2. Clear interrupt
 3. Data interrupt request
 4. End of operation interrupt request
 5. Alarm interrupt request
 6. Manual interrupt request
 7. Assembly mode
 8. Scan mode
 9. Read mode
- (Repeat from c 1, 000 times)

D. POSITIONING FUNCTIONS (D = 3)

1. Page advance
2. Page advance - small step
3. Position mirror forward.
4. Position mirror reverse.
Repeat from (D. 1) 24 times.

E. MECHANICAL ACTION FUNCTIONS - Except Mechanical Action Code (D = 4)

1. Clear interrupt.
2. End of operation interrupt request.
3. Alarm interrupt request.
Repeat from (D. 1) 1,000 times.

F. READ MODE FUNCION (D = 5)

1. Read function.
2. Zero mirror.
Repeat from (F. 1) 24 times.

Section 1. Check Page Advance (normal and mini-step) and End of Operation Interrupt After Page Advance.

A. PAGE ADVANCE - Normal and Mini-step.

1. Sort to primary hopper
2. Advance page the specified increment. Normal step.
3. Repeat A. 2 until increment equals $0F_{16}$.
4. Repeat from A. 1 if Repeat Conditions is selected.
5. Repeat from A. 1 for mini-step.

B. END OF OPERATION INTERRUPT AFTER PAGE ADVANCE

1. Sort to primary hopper.
2. Advance page the specified increment. Normal step.
3. Select End of Operation interrupt.
4. Check for interrupt. Error if interrupt did not occur.
5. Repeat from B. 2 until page advance increment equals $0F_{16}$.
6. Repeat from B. 1 if repeat conditions is selected.

7. Repeat from B. 1 for mini-step.
8. Repeat from B. 1 if Repeat Conditions is selected.
9. End of section. Repeat from A. 1 if Repeat Section is selected.

Section 2 (S2). Check Document Sorting, Sort Timing and End of Operation Interrupt After Sorting.

A. SORT TO ALTERNATE HOPPERS

1. Set counter.
2. Wait Not Busy.
3. Sort to primary hopper.
4. Sort to secondary hopper.
5. Repeat from A. 3 four times.
6. Control to SMM
7. Repeat from A. 1 if Repeat Conditions is selected.

B. SORT TIMING

1. Set counter
2. Wait Not Busy.
3. Advance document to end of page.
4. Sort to primary.
5. Compute the time in ms that Busy status remains set during sort operation.
6. Error stop if sort time exceeds 1800 ms.
7. Repeat from B. 2 nine times.
8. Control to SMM
9. Repeat from B. 1 if Repeat Conditions is selected.

C. END OF OPERATION INTERRUPT AFTER SORT

1. Set counter.
2. Sort to primary hopper and select End of Operation interrupt.
3. Wait Not Busy.
4. Check for E. O. P. interrupt. Error if interrupt did not occur.
5. Repeat from C. 2 if Repeat Conditions is selected.

6. Sort to secondary hopper.
7. Select End of Operation interrupt.
8. Check for interrupt. Error if it did not occur.
9. Repeat from C. 6 if Repeat Conditions is selected.
10. Repeat from C. 2 four times.
11. End of Section stop. Repeat from A. 1 if Repeat Section is selected.

Section 3 (S3). Check Mirror Motion, Status, Coordinates, Timing and Interrupts.

A. MIRROR MOTION TO FAR FORWARD AND FAR REVERSE AND CORRECT STATUS.

1. Set counter.
2. Zero mirror.
3. Check for Ready and Mirror Far Reverse status.
Error if status not correct.
4. Move mirror to Far Forward position. Check Equipment status for End of Operation, Ready and Mirror Far Forward status.
Error if status not correct.
5. Check Mirror status for Mirror Far Forward and Compare.
Error if status is not correct.
6. Move mirror to Far Reverse position.
7. Check Equipment status for End of Operation, Ready and Mirror Far Reverse.
Error if status is not correct.
8. Check Mirror status for Mirror Far Reverse and Compare.
Error if status not correct.
9. Repeat from A. 2 twenty-four times.
10. Repeat from A. 1 if Repeat Conditions is selected.

B. COMPARE AND COORDINATE STATUS AT EACH COORDINATE FROM ZERO TO FAR FORWARD. COMPARE BUT NOT COORDINATE STATUS FROM MIRROR FAR FORWARD TO MIRROR FAR REVERSE.

1. Set coordinate flag to one.
2. Zero mirror.
3. Move mirror forward to coordinate selected.
4. Check Mirror status for Compare and correct Coordinate.
Error if status not correct.

5. Update coordinate by one and repeat from B. 2 until coordinate reaches FF_{16} .
 6. Decrease coordinate flag by one.
 7. Move mirror reverse to selected coordinate.
 8. Check Mirror status for Compare only. Error if status not correct.
 9. Move mirror to Far Forward position.
 10. Repeat from B. 6 until coordinate reaches zero.
 11. Repeat from B. 1 if Repeat Conditions is selected.
 12. Clear controller
- C. END OF OPERATION INTERRUPT AFTER FORWARD AND REVERSE MIRROR MOTION CHECK
1. Set counter
 2. Zero mirror
 3. Move mirror forward to coordinate 40_{16} .
 4. Select End of Operation interrupt.
 5. Check for interrupt. Error if interrupt did not occur.
 6. Repeat from C. 2 if Repeat Conditions is selected.
 7. Move mirror to coordinate $F0_{16}$.
 8. Zero mirror
 9. Select End of Operation interrupt.
 10. Check for interrupt. Error if it did not occur.
 11. Repeat from C. 7 if Repeat Conditions is selected.
 12. Repeat from C. 2 twenty-four times.
- D. END OF OPERATION INTERRUPT ON MIRROR FAR REVERSE AFTER A CLEAR CONTROLLER FUNCTION
1. Set counter
 2. Zero mirror
 3. Move mirror to Far Forward position.
 4. Clear controller
 5. Wait Not Busy
 6. Check for Mirror Far Reverse status. Error if not set.
 7. Select End of Operation interrupt.

8. Check for interrupt. Error if interrupt did not occur.
 9. Repeat from D. 2 twenty-four times.
 10. Repeat from D. 1 if Repeat Conditions is selected.
- E. COMPUTE MIRROR TIMING - FORWARD AND REVERSE
1. Clear minimum, maximum and average time flags.
 2. Zero mirror
 3. Start mirror forward to coordinate OA_{16} .
 4. Wait for Busy to drop
 5. Start Read from OF_{16} to FO_{16} .
 6. Wait for Busy.
 7. Determine the time in ms that Busy status remains set during mirror motion.
 8. Update minimum, maximum and average time flags.
 9. Repeat from E. 1 fourteen times.
 10. Determine average of the fifteen times.
 11. Convert results to decimal.
 12. Print message giving average minimum and maximum mirror forward time.
 13. Repeat from 1 if Repeat Section is selected.
 14. Clear minimum, maximum and average time flags.
 15. Zero mirror
 16. Move mirror to coordinate FO_{16} .
 17. Wait Not Busy
 18. Start mirror motion toward zero.
 19. Determine the time in ms that Busy status remains set during mirror motion.
 20. Update minimum, maximum and average time flags.
 21. Repeat from E. 14 nine times.
 22. Determine average of 15 times.
 23. Convert results to decimal.
 24. Print message giving average, maximum and minimum times.
 25. Repeat from 14 if Repeat Section selected.

F. ALARM INTERRUPT ON ILLEGAL MIRROR MOTION CHECK

1. Set counter
2. Zero mirror
3. Move mirror forward to coordinate $F0_{16}$.
4. Attempt to move mirror forward to coordinate 80_{16} .
5. Select alarm interrupt.
6. Check for interrupt. Error if interrupt did not occur.
7. Repeat from F. 2 twenty-four times.
8. Repeat from F. 1 if Repeat Conditions is selected.
9. End of Section 3. Repeat from A. 1 if Repeat Section is selected.

Section 4. Protect Test

A. PROTECT STATUS FROM 1735 CHECK

1. Get SMM parameter, save and set bit 5. (This causes TTY to type out in Character mode which is necessary when using the Protect feature.)
2. Set counter
3. Type out message: SET PROTECT SWITCH ON 1735
4. Input Equipment status.
5. Check for Protect status bit.
6. Repeat from A. 4 if not set.
7. Repeat from A. 4 forty-nine times.
8. Repeat from A. 2 if Repeat Conditions is selected.

B. REPLY TO PROTECTED 1735/915 FUNCTIONS CHECK

1. Set protect bits in all of memory.
2. Type message: SET 1704 PROTECT SWITCH - RUN
3. Stop. Wait for operator to set PROTECT switch on console and place computer in Run.
4. Set counter.
5. Output all function bits, one at a time, from 0 through 15.
Error if a reject is received.
6. Repeat from B. 5 twenty times.

C. REJECT TO NONPROTECTED 1735/915 FUNCTIONS CHECK

1. Set counter.
2. Clear Protect bits in core.
3. Output all function bits, one at a time, from 0 through 15.
Expect a reject. Error if a reply is received.
4. Repeat from C. 3 nineteen times.
5. Type message: CLEAR 1704 AND 1735 PROTECT SWITCHES - RUN.
6. Clear all Protect bits in core.
7. End of section. Repeat from A. 1 if Repeat Section is selected.
8. Restore original SMM Parameter.

Section 5. Check Window Operation and Space Code Field Mark Generation

A. READ NOMINAL TEST DOCUMENTS IN ALPHANUMERIC MODE - SCAN 2

1. Set document count.
2. Set up alphanumeric pattern for data checking.
3. Sort to primary hopper.
4. Set line count.
5. Advance page two lines.
6. Jump to A. 8.
7. Advance page one line.
8. Clear buffer.
9. Zero mirror.
10. Clear error counters.
11. Select Scan 2 mode.
12. Read one line.
13. Check actual data against expected data. Update error count if not the same.
14. Error stop if any Data Compare errors occurred in this line.
15. Check End of Data Line for seven spaces, two field marks (DC) and a fill character (DB).
16. Error stop if any space code - field mark errors.
17. Print actual and expected data.

18. Repeat from A. 7 fifty-five times.
19. Repeat from A. 3 four times.
20. Repeat from A. 1 if Repeat Conditions is selected.
21. Wait Not Busy.
22. Sort to primary.
23. End of Section 5. Repeat from A. 1 if Repeat Section is selected.

Section 6. Check End of File Status, Manual Interrupt and Alarm Interrupt.

- A. CHECK END OF FILE STATUS AND MANUAL INTERRUPT, LOAD A DOCUMENT TO THE DOCUMENT READY POSITION, BUT DO NOT PRESS THE START SWITCH TO STORE THIS SECTION
 1. Check Equipment status for Not Ready. Error if Ready status is set.
 2. Type message: SET AND CLEAR END OF FILE SWITCH 10 TIMES.
 3. Set counter.
 4. Select manual interrupt.
 5. Check for interrupt. Error if interrupt did not occur.
 6. Check for End of File status. Error if not set.
 7. Repeat from A. 4 nine times.
 8. Repeat from A. 3 if Repeat Conditions is selected.
- B. CHECK ALARM INTERRUPT WHEN GOING FROM READY TO NOT READY
 1. Type message: PRESS START THEN STOP SWITCH 10 TIMES.
 2. Set counter.
 3. Select alarm interrupt.
 4. Check for interrupt. Error if interrupt did not occur.
 5. Repeat from B. 3 nine times.
 6. Repeat from B. 2 if Repeat conditions is selected.
 7. End of Section 6. Repeat from A. 1 if Repeat Section is selected.

Section 7. Check Mechanical Counters

- A. CLEAR AND INCREMENT COUNTERS INDIVIDUALLY
 1. Clear each counter separately.
 2. Increment counter No. 1 fifty times.

3. Increment counter No. 2 fifty times.
 4. Increment counter No. 3 fifty times.
 5. Control to SMM.
 6. Repeat from A. 2 if Repeat Conditions is selected.
 7. Delay approximately 1 second.
 8. Clear each counter separately.
 9. Repeat from A. 8 if Repeat Condition is selected.
- B. INCREMENT COUNTERS 1, 2, AND 3 FIFTY TIMES SIMULTANEOUSLY
1. Set counter.
 2. Increment all counters fifty times.
 3. Delay approximately 1 second.
 4. Repeat from B. 2 if Repeat Conditions is selected.
 5. Clear all counters simultaneously.
- C. SIMULTANEOUSLY SET AND CLEAR ALL COUNTERS AS FOLLOWS:
1. Clear 3 - increment 1 and 2 ten times.
 2. Clear 2 - increment 1 and 3 ten times.
 3. Clear 1 - increment 2 and 3 ten times.
 4. Increment 1, 2 and 3 ten times.
 5. Final contents of counter = 10, 20, 30.
 6. Repeat from C. 1 if Repeat Conditions is selected.
 7. Delay approximately 1 second.
 8. Clear all counters.
 9. End of Section 7. Repeat from A. 1 if Repeat Section is selected.

Section 8. Check Read in Scan 3

- A. READ AND CHECK DATA IN ALPHANUMERIC MODE
1. Set document count.
 2. Set up alphanumeric pattern for data checking.
 3. Sort to primary hopper.
 4. Set line count.

5. Advance page to first line.
6. Jump to A. 8.
7. Advance page two lines.
8. Clear input buffer.
9. Zero mirror.
10. Clear error flag.
11. Read line.
12. Check data, one word at a time (two characters), update error count if data word read does not match expected data.
13. Error stop if data compare errors occurred in line just read. (See I. D. 2.)
14. Repeat from A. 7 thirty-seven times (one page).
15. Repeat from A. 3 four times.
16. Repeat from A. 1 if Repeat Conditions is selected.

B. READ AND CHECK DATA IN ALPHA MODE

1. Set up alpha pattern for data checking.
2. Set document count.
3. Wait Not Busy.
4. Sort to primary hopper.
5. Set line count.
6. Advance page to first line.
7. Jump to A. 10.
8. Wait Not Busy.
9. Advance page two lines.
10. Clear input buffer.
11. Zero mirror.
12. Clear error flag.
13. Select Alpha mode.
14. Read line.
15. Check for "Out of Mode Characters". See Error code 0B.

16. Check data. (See Section 8, step 12.)
17. Error stop if data compare errors occurred in line just read. (See I. D. 2.)
18. Repeat from B. 8 thirty-seven times (one page).
19. Repeat from B. 3 four times.
20. Repeat from B. 1 if Repeat Conditions is selected.

C. READ AND CHECK DATA IN NUMERIC MODE

1. Generate numeric pattern for data checking.
2. Set document count.
3. Wait Not Busy.
4. Sort to primary.
5. Set line count.
6. Advance page to first line.
7. Jump to A. 10.
8. Wait Not Busy.
9. Advance page two lines.
10. Clear input buffer.
11. Zero mirror.
12. Clear error flag.
13. Select numeric mode.
14. Read line.
15. Check for "Out of Mode Characters." See I. D. 6. b. Error code 0B.
16. Check data. (See Section 1, step 12.)
17. Error stop if data compare errors occurred in the line just read. See I. D. 2.
18. Repeat from C. 8 thirty-seven times (one page).
19. Repeat from C. 3 four times.
20. Repeat from C. 1 if Repeat Conditions is selected.

D. CHECK DATA INTERRUPT

1. Set counter.
2. Wait Not Busy.

3. Sort to primary.
 4. Advance page to first line.
 5. Wait Not Busy.
 6. Zero mirror.
 7. Start read.
 8. Select Data interrupt.
 9. Check for interrupt. Error if interrupt did not occur.
 10. Repeat from D. 5 twenty-four times.
 11. Repeat from D. 1 if Repeat Conditions is selected.
- E. CHECK FOR END OF OPERATION INTERRUPT AFTER A READ
1. Wait Not Busy.
 2. Sort to primary.
 3. Set counter.
 4. Zero mirror.
 5. Read a line.
 6. Check for Mirror Compare status. Error if not set.
 7. Select End of Operation interrupt.
 8. Check for interrupt. Error if interrupt did not occur.
 9. Repeat from E. 4 twenty-four times.
 10. Repeat from E. 1 if Repeat Conditions is selected.
- F. CHECK ALARM INTERRUPT ON LOST DATA
1. Sort to primary hopper.
 2. Advance page to first line.
 3. Set counter.
 4. Zero mirror.
 5. Start Read but do not input data. Forces Lost Data.
 6. Wait Not Busy.

Section 9. Check the ability of the reader to maintain registration within reading limits during a series of constant page advance functions of increments of (1, 2, 3 F_{16}).

Stop read function and coordinate counter drift are also checked.

1. Set page advance increment equal to one.
2. Sort to primary hopper.
3. Clear error flag.
4. Set up alphanumeric pattern for data checking.
5. Clear input buffer.
6. Advance page to first line and read first line three times.
7. Check data read against expected data. Update error count if any data words (two characters) are not correct.
8. Error stop if data compare errors occurred in the line first read. (See I. D. 2.)
9. Repeat from 1 if Repeat Conditions is selected.
10. Set iteration counter for this column.
11. Select alphanumeric and scan 3.
12. Advance page the specified increment.
13. Repeat 12 if page increment is an add number.
14. Zero mirror.
15. Start Read.
16. Check for Data Ready, if not go to 21.
17. Input Data Word.
18. Check for expected character.
19. Go to 16 if not expected character.
20. Go to 25 if expected character.
21. Check for mirror compare i. e., EOP.
22. Not mirror compare go to 16.
23. Mirror compare, error stop: Expected character not found, or page advance error.
24. Go to 28.
25. Stop Read when expected character is read.

26. Get Mirror status.
27. Check that the expected character was read at the expected coordinate plus or minus two.
28. Repeat from 12 the number of times specified for this column.
29. Update page advance increment and repeat from 2 until increment equals $0F_{16}$.
30. Wait Not Busy.
31. Sort to primary hopper.
32. End of Section. Repeat from 1 if Repeat Section is selected.

Section A₁₆. Check Line Locate function and interrupts.

A. CHECK LINE LOCATE AND LINE LOCATE FAILURE

1. Set counter.
2. Inhibit interrupts.
3. Sort to primary hopper.
4. Zero mirror.
5. Move mirror to coordinate 25.
6. Line Locate. Expect Line Locate Failure and Alarm status within 300 ms. Error if status does not occur within this time.
7. Repeat from A. 4 twenty-four times.
8. Set counter.
9. Zero mirror.
10. Advance page two lines.
11. Move mirror to coordinate 25.
12. Line Locate. Expect End of Operation status within 300 ms. Error if status does not set within this time.
13. Repeat from A. 9 thirty-six times.

B. CHECK ALARM INTERRUPT ON LINE LOCATE FAILURE

1. Sort to primary hopper.
2. Set counter.
3. Zero mirror.
4. Move mirror to coordinate 25.

5. Line Locate. Expect Line Locate Failure and Alarm status within 300 ms. Error if status does not set within this time.
6. Select Alarm interrupt.
7. Check for interrupt. Error if interrupt did not occur.
8. Repeat from B. 3 twenty-four times.
9. Repeat from B. 2 if Repeat Conditions is selected.

C. CHECK FOR END OF OPERATION INTERRUPT AFTER LINE LOCATE

1. Set counter.
2. Zero mirror.
3. Advance page two lines.
4. Move mirror to coordinate 25.
5. Line Locate. Expect End of Operation status within 300 ms. Error if status does not set within this time.
6. Select End of Operation interrupt.
7. Check for interrupt. Error if interrupt did not occur.
8. Repeat from C. 2 thirty-six times.
9. Repeat from C. 1 if Repeat Conditions is selected.
10. End of Section A. Repeat from A. 1 if Repeat Section is selected.

Section B. Check Marking Function

A. CHECK MARKING FUNCTION

1. Set counter.
2. Sort to primary hopper.
3. Advance page two lines.
4. Mark page.
5. Check for Busy status. Error if not busy.
6. Wait Not Busy.
7. Repeat from A. 3 thirty-six times.
8. Repeat from A. 1 if Repeat Conditions is selected.

B. CHECK FOR END OF OPERATION INTERRUPT AFTER MARKING

1. Sort to primary hopper.
2. Set counter.
3. Zero mirror.
4. Advance page two lines.
5. Move mirror to coordinate 25.
6. Line Locate.
7. Mark page.
8. Wait Not Busy.
9. Select End of Operation interrupt.
10. Check for interrupt. Error if interrupt did not occur.
11. Repeat from B. 3 thirty-six times.
12. Repeat from B. 1 if Repeat Conditions is selected.
13. End of Section B. Repeat from A. 1 if Repeat Section is selected.

1700/935-2 READ TRANSPORT TEST

(OC2A52 Test No. 52)

I. OPERATIONAL PROCEDURE

A. DOCUMENTS REQUIRED

1. No. 48705208
2. No. 48705209

B. RESTRICTIONS

Requires a minimum 8K system

C. LOADING PROCEDURE

1. Standard SMM17 call
2. Call test no. 52

D. PARAMETERS

1. Fixed
 - a. All document dimensions
 - b. Data read definition
 - c. Leading edge detector distance to lens 2
 - d. Lens 2 to lens 1 and 3 distance
2. Manual

On a manual interrupt, control is transferred to "ENTER PARAMETERS" routine. If phase 1 of the program is complete (see I. D. 3), changes to parameters can be made by typing in one of the following control.

<u>Control Code</u>	<u>Routine</u>
A	Autoload a block entry*
C	Load the controller
DD	Request shift register dump device
DR	Data receive from the FF406*
DS	Data send to the FF406*
E	End Test

*Maintenance aids

<u>Control Code</u>	<u>Routine</u>
I	FF406 Interrupt Line
L	Shift register dump parameter
P	Output device
Q	FF406 equipment code
R	Read (lens data)
T	Document size
X	Execute test
Ø	Oscillator frequency request
B	Bias read coordinate

3. Forced (Automatic) Requests

- a. Should anything happen to prevent the normal flow of the program before a series of required entries are made, the program will re-start its list of automatic parameter calls. The following is a list of those calls. (See I. D. 2 for control code meeting).

"ENTER PARAMETERS"

The sequence that follows is:

Q, I, C, O, R, T

Until this sequence is completed, manual selection of series will not be allowed.

(For further information see Section II messages).

4. STOP/JUMP Parameter

Fourbits of the Stop/Jump parameter are used. They can be displayed in A register for a change if the SKIP switch is on just after an entry in the "ENTER PARAMETER" routine. The bits are:

Bit 8 = 1 = suppress error message output

Bit 12 = 1 = Suppress automatic document repositioning

Bit 5 = 1 = Repeat Execution after zone error

Bit 13 = 1 = Full, dump when listing image

E. OPERATING INSTRUCTIONS

1. Load OC2 via SMM17 operation instructions.

2. Respond with the correct entry on the teletype to the requests (see I. D. 3).
3. Manual parameter entries may be made after (I. E. 2) is complete.

If no further parameters are requested, other than "X" for execute test, the remaining entries are prefixed at:

P = 1 = teletype

DD = 1 = Dump Image to standard output device

L = 2 = Shift register dump on error

The Data will be output to the selected dump device (See II. B. 3) as 400, 80 CHTR lines to the Printer or Lister, or 400, 60 CHTR lines to the teletype. (The upper and lower 10 columns are truncated.) If bit 13 of the Stop/Jump parameter is not Set, the All Zero columns of the printout will be suppressed and tallied if on the standard output device. Upon receiving a column with data in it, this column count will be printed as:

ZC = XXXX where XXXX = the decimal count of suppressed columns.

II. MESSAGES

A. NORMAL MESSAGES

1. BEGIN OC2 READ TRANSPORT TEST IA = XXXX

Initial typeout where XXXX = the initial address of the program.

2. END OC2 READ TRANSPORT TEST

Final message of test in response to control code (E).

3. XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

This is the format after a (DRYYYY) command where XXXX represents 4 hexadecimal digits of 8 FF406 words. The command is DATA RECEIVE and YYYY = the address of the FF406 at which the dump request is to start. The data is output after a line feed, and carriage return. The string continues if another YYYY is entered again followed by a line feed, carriage return, YYYY forms the new address to start the string. Exit from this command by MANUAL INTERRUPT.

B. COMMAND MESSAGES

1. LENS NO. = X SIZE = Y

In response to code (R)*

X = Desired lens number and Y = its size

X = 1, 2 or 3, Y = 6 for 60 mm and 8 for an 80 mm lens. The program continues with:

HORR POS = XXXX. VERT POS = YYYY.

If lens 2 is requested, part 1 of this message is omitted. XXXX and YYYY are the horizontal and vertical positions of the requested lens respectively. Terminate each entry with a period.

2. S/R DUMP PARAMETER = X

In response to code (L),

X = 1 = no dump = 2 = dump on error = 3 = demand shift register dump.

An input of 3 will not disturb a previous entry of 1 or 2. An input of a 3 will not produce 2 dump to the output device if no black data was detected during the read if bit 13 of STJP is not set.

3. S/R DEVICE = X

In response to code (DD),

X = 1 = dump to standard output device = 2 = dump to lister. This is an output director.

4. NORMAL OUTPUT DEVICE = X

In response to code (P),

X = 1 = teletype, = 2 = 1742 printer. If a 2 is entered, the program continues with:

1742 EQUIPMENT = X

Where X = 0→F as the printer equipment number. The program continues with:

OCR DRUM = 1, 8156-2 = 2 = Y

Where Y = 1 = USASI font, 2 = standard print drum.

5. FF406 EQUIPMENT = X

In response to code (Q), *

X = 0→F = the FF406 equipment number.

*These entries are force called up on initialization of the program (See I. D. 3).

6. FF406 INT. LINE = X

In response to code (I), *

X = 2 → F = the FF406 interrupt line.

7. DOCUMENT SIZE = X

In response to code (T), *

X = 0 for Doc. No. 48705208 (5 1/2" X 8 1/2")

X = 1 for Doc. No. 48705209 (2 1/4" X 3")

8. SIGN = S

In response to code (B),

A = 2 → F as the MT interrupt line.

S = + or - = direction of bias

If "F" is entered and lens 2 is selected the leading edge detector is compensated by the amount of error present and control is automatically transferred to message (II B1). The computer continues with:

BIAS = NNNN.

NNNN = the decimal number of columns to move the image register pattern.

The entry is terminated with a period and overflow is possible. This quantity is accumulative in both the positive or negative direction.

9. OSC = X

In response to code (0), *

X = 1 - slow oscillator = 2 = fast oscillator

The transport must be running during this parameter selection.

10. MT, W, X, Y, Z, = A B C D

In response to code (C), *

A = 2 → F as the MT interrupt line.

Enter B = 0 → F for the converter number C = 0 → F for the equipment number and D = 0 → 7 for the unit number of the mag tape containing the "Aux. Tape".

The program will now autoloading the FF406.

The FF406 controller is test No. 1 and is located in location 1 of the program.

A possibility of 6 errors can occur on Loading which are II. C. 4 → II. C. 9.

11. ENTER PARAMETERS

In response to manual interrupt, See I. C. 2 (Manual entry of parameters).

*These entries are force called up on initialization of the program (See I. D. 3).

C. ERROR MESSAGES

1. HDIAL = XXXX

Horizontal dial setting does not agree with that supplied by operator, or, new setting after bias is added or subtracted. Used only for lens 1 or 3. Tolerance = ± 1.5 percent.

2. LEDT = SX . XX

Gives leading edge detector variation from the expected value in inches, also as above on a bias change. Lens 2 only. S shows direction of movement for corrective action. Tolerance = ± 1.5 percent.

3. VDIAL = XXXX

Vertical dial setting does not agree with that supplied by operator. Not effected by bias. Tolerance = ± 1 percent.

4. NO RESPONSE FROM BC

Self explanatory

5. BC CHECKSUM ERROR XXXX

A checksum error has occurred while loading the BC XXXX - The reflected word count in hex. This error message will occur if the transport is OFF during AUTOLOAD.

6. MT X STATUS ERROR

X = The MT unit number.

7. NO BC INT.

.5 seconds have elapsed and no interrupt has been received from the BC as expected on auto loading.

8. PROGRAM NOT ON TAPE

The OCL control wave was not on the unit specified.

9. NO RESPONSE FROM MT X

X = The Mag tape unit number.

10. TTMG FAIL

Transport timing failed or was in error.

11. MECH. FAIL

A mechanical fail status was received.

12. TRANS. CK OR LOST DOC.

PCA =
ABCDE

A transport check/lost document status was received. The photocell on Side A (Feed side) of the transport where 1 = light or 0 = dark at the time the error was detected where: A = feed check A, B = feed check B, C = feed check C, D = doubles sense, and E = LEDT.

13. SORT CK

PCB =
ABCDE

A Sort Check status was received. The photocells on Side B (stacker side) were 1 = light or 0 = dark at the time the error was detected where: A = sort check 1, B = sort check 2, C = sort check 3, D = sort station 1 and E = sort station 2.

14. LIST FAIL

LST =
ABCDZ

A Lister Fail status was received. The Lister status bits were 0 = not present, 1 = condition present where the conditions were: A = busy, B = paper low, C = out of paper and D = Lister ready, Z = 0.

15. NO FEED

A status response indicating that feed failed.

16. FF406 HANGUP

The FF406 failed to respond to a command in the allowed amount of time.

17. OSC. ERR.

There was an illegal response to an oscillator frequency request.

18. CLOCK ERR. XXXX/YYYY

The clock versus tack pulse distance is computed by two methods and disagree by more than 2 percent. If they disagree by less than 4 percent, YYYY will be compensated by 25 percent of the difference, the document position recomputed and, at the end of the evaluation pass, message II. C. will be output. (See II. C. 23 for further information).

19. MAG. FACTOR = X.XX

The computed magnification factor disagrees with the expected magnification factor by more than 2 percent. The slew rates for the horizontal and vertical dials are computed from the magnification factor. If there is an error of more than 2 percent and less than 4 percent, the computed magnification will be used for this. Otherwise, the expected factor will be used.

20. TAN. SKEW = S.0XXXX

The skew exceeded its allowed tolerance for the document size specified. The document rotation (S) was + = counterclockwise or - = clockwise. The degrees of skew can be looked up in the tangent table.

21. ZONE QUALITY - X, X, X, X, X

One or more of the 5 zones has a quality of less than 5. All zones start with a quality of 9 and are reduced by one or more of the following factors:

<u>Demerits</u>	<u>Zones</u>	<u>Cause</u>
-1	ALL	*Quantizing ± from expected more than 250
-2	All	*Quantizing ± from expected more than 500
-4	All	*Quantizing ± from expected more than 1000
-1	All	A false zone with Z-2 characteristics
-5	All	No Zone 4
-9	1	Zone 2 first in table
-9	1	Zone 2 less than .310" from doc. leading edge
-9	5	Zone 2 third in table
-9	5	Zone 2 more than .460" from doc. leading edge

22. CHECKS NOT PERFORMED

- Mag.
- Skew
- Vert. Pos.
- Hor. Pos.
- Clock

Due to a zone quality of less than 5 or another stated cause, the units listed below the message were not performed. Other causes for not performing a check follow:

*A count of 211 block bits in read area (see read area in Figure 1).

- a. If zones 2 or 4 are less than 5, no checks will be performed.
- b. If zone 1 is less than 5, magnification and skew will not be performed.
- c. If zone 3 is less than 5, horizontal and vertical position will not be performed.
- d. If zone 5 is less than 5, skew will not be performed.

The following is a list of additional conditions for not checking:

- e. Magnification - less than 3 bars, ≥ 5 and ≤ 15 light pipes high, or a negative or zero magnification factor.
- f. Horizontal position - a document is to be repositioned.
- g. Skew - Less than 2 bars, ≥ 5 and ≤ 15 light pipes high or less than 2 end bars, but with nomatch with the same qualifications in zone 1, or no good find within 9 bars.

23. DOCUMENT REPOSITIONED

As the result of a clock error more than 2 percent and less than 4 percent.

The document was repositioned if the bit 12 of the STOP/JUMP parameter is Clear and the sum of the zone qualities for zone 2 and 4 are equal to or more than 14.

D. ERROR STOPS

None

E. MAINTENANCE AIDS

Three of the manual entries are present as maintenance aids and are as follows:

- a. In response to code (A), up to 2K words can be sent to the FF406. The data to be autoloading is typed in via teletype in hexadecimal format, each word being followed by a "line feed," and "carriage return." The data block is transferred after a final entry of N "line feed," carriage return." Control is then returned to "enter parameters". Up to eight words may be autoloading without harm to the OC2 controller. Thus, a dispatch to a certain portion of the controller or another program may be entered by this method.
- b. In response to code (DR), data can be received from the FF406 and typed on the teletype. See message (II. A. 3) for explanation.

- c. In response to code (DS), data can be sent to a particular location(s) of the FF406. This allows the entry of small programs without destroying the OC2 controller as is the case in autoloading a program of more than eight locations. When one wishes to exercise that program, a one word jump to the desired location could be autoloaded. Due to the command structure of the program, any entry from "enter parameters" requiring the use of the OC2 controller could automatically return control to the controller when the command is issued. Data is sent to the FF406 as follows: Manual interrupt terminates entries.

EX: DS102, AAAA LF CR*
 ,BBBB LF CR
 105, CCCC LF CR
 0, DDDD LF CR
 5, EEEE LF CR
 MI*

From the preceding, the following would result in the FF406:

<u>Locn</u>	<u>Contents</u>	<u>Remarks</u>
102	AAAA	
103	BBBB	No address causes seg. entry
104	XXXX	Remains untouched
105	CCCC	
106	DDDD	0 = no address
005	EEEE	

*LF CR represent "line feed" and "carriage return"
 MI represents "manual interrupt"

III. DESCRIPTION

A. INITIALIZATION

1. Set brush back roller, doubles level and feeder.
2. Load the 935 with documents and set the stackers to the proper length.

B. OPERATION

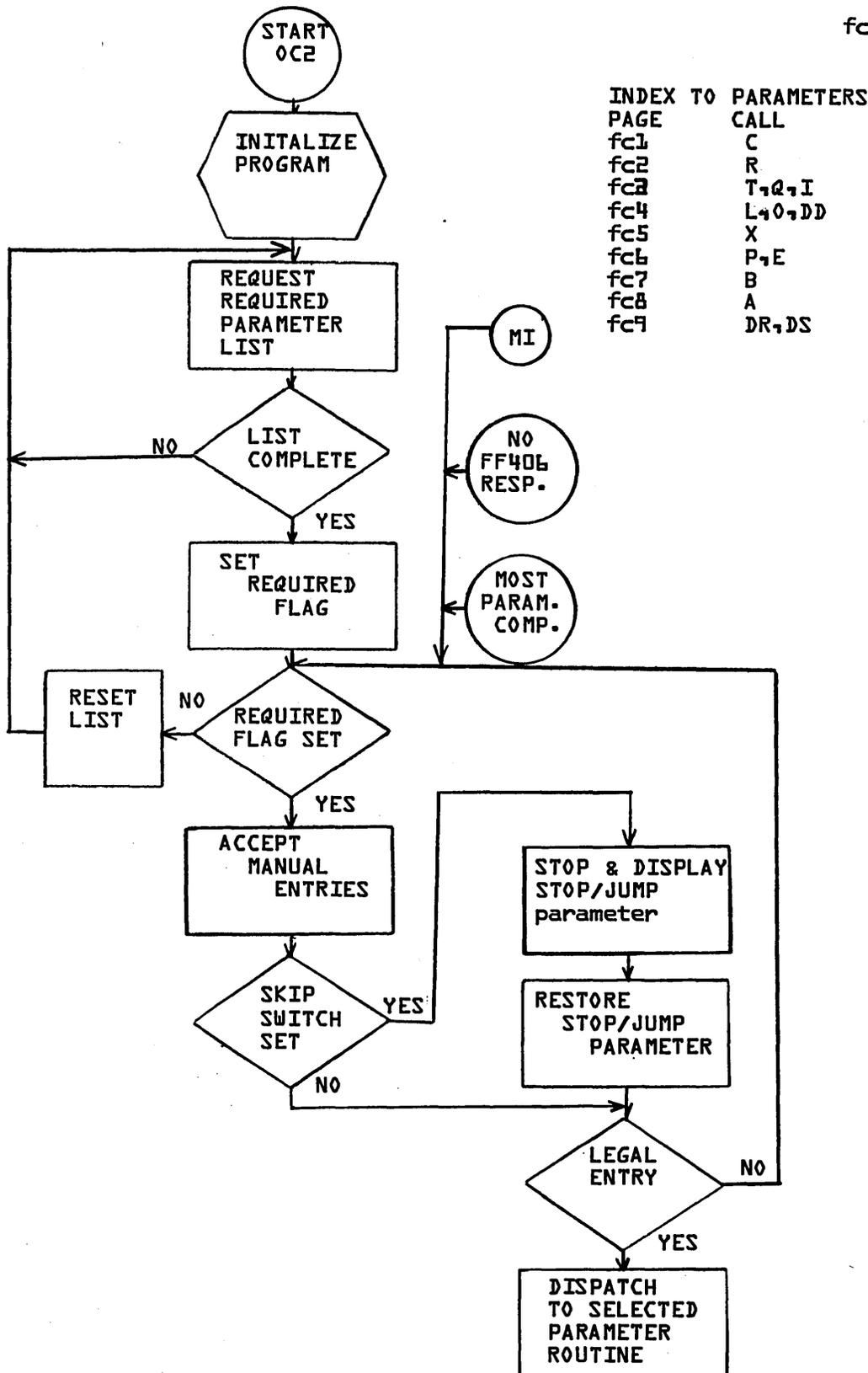
1. Purpose
 - a. To test the calibration of 60 and 80 mm lenses.
 - b. To check the document skew for small and large documents.
 - c. To check the magnification factors of 60 and 80 mm lenses.

- d. Find the slow and fast clock rates.
- e. Allow viewing of the Image register.
- f. Provide some maintenance aids for checking the buffer controller.

2. Procedure

The attached flow charts outline the procedure in detail.

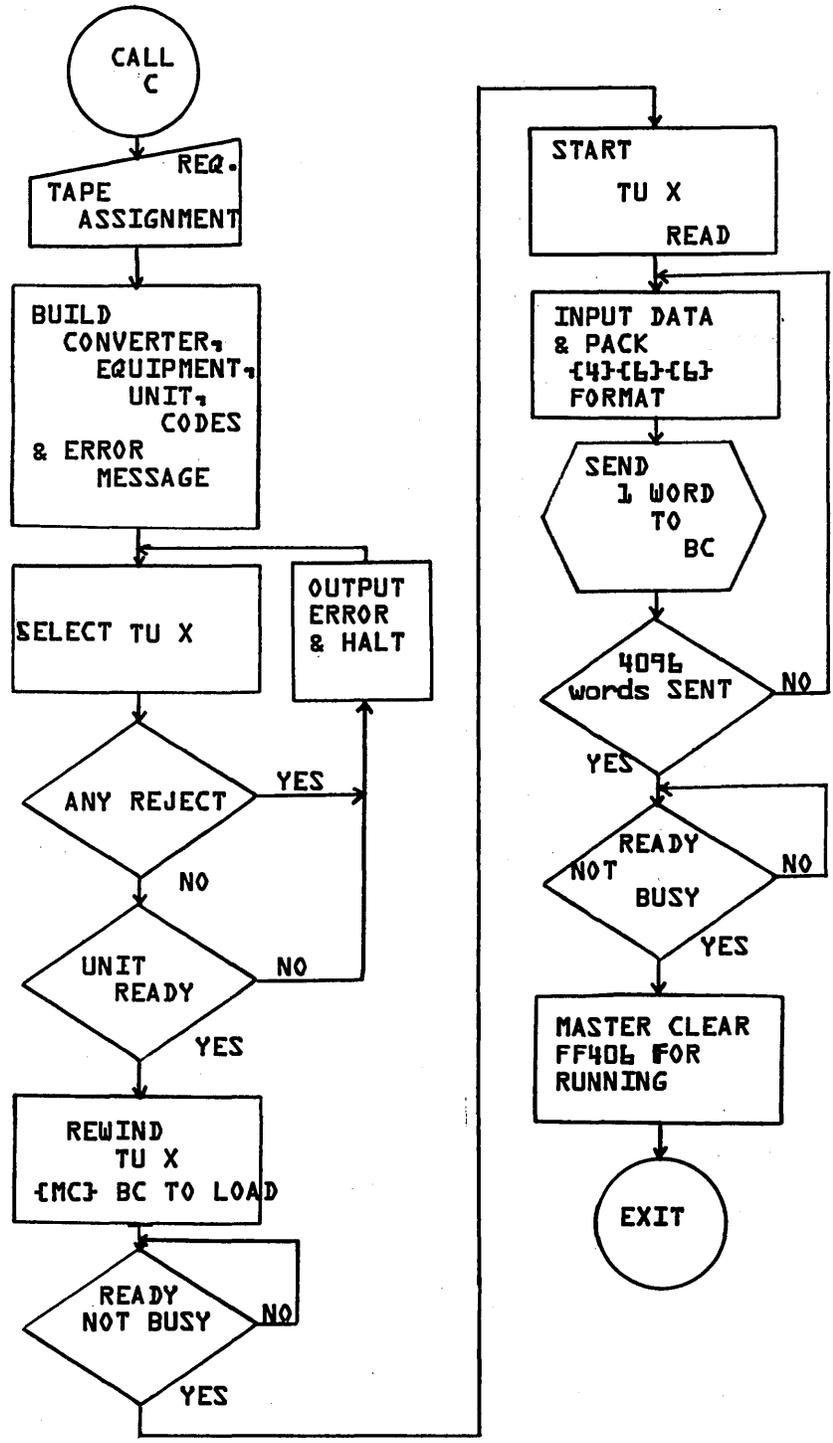
fc0



INDEX TO PAGE	PARAMETERS CALL
fc1	C
fc2	R
fc3	T, Q, I
fc4	L, O, DD
fc5	X
fc6	P, E
fc7	B
fc8	A
fc9	DR, DS

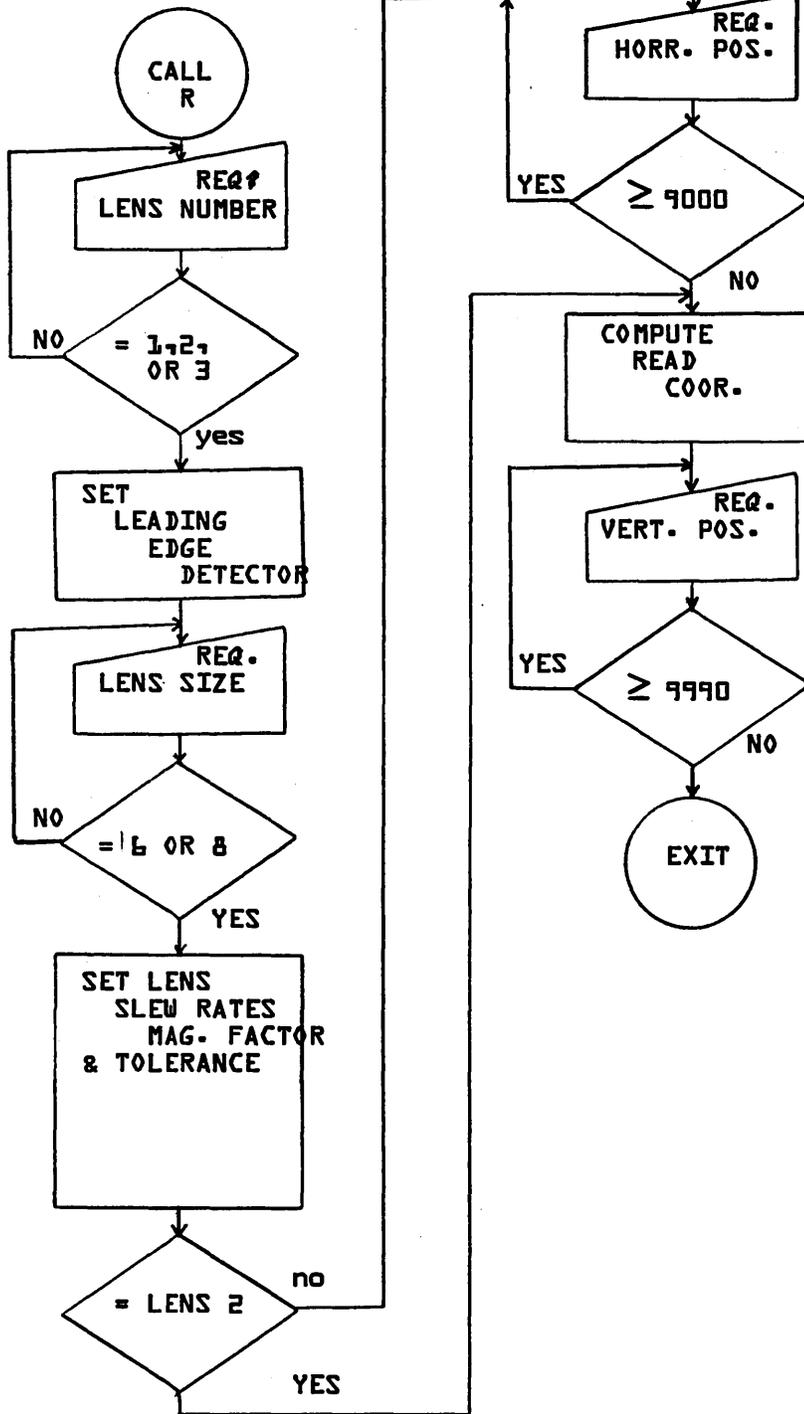
AUTO LOAD THE BC

fcl

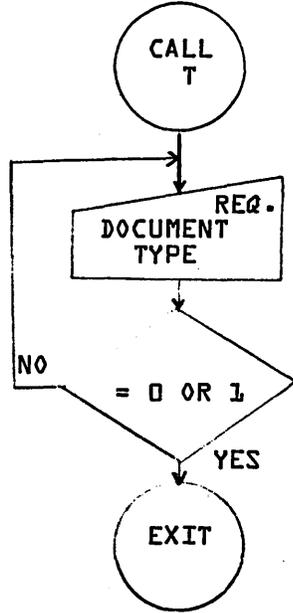


READ PARAMETERS

fc2

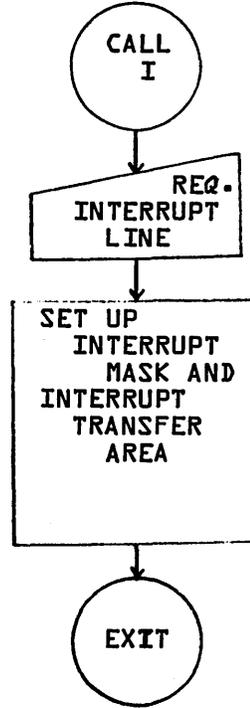


DOCUMENT TYPE

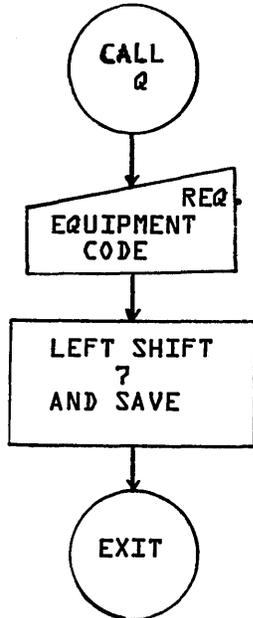


FF406 INT. LINE

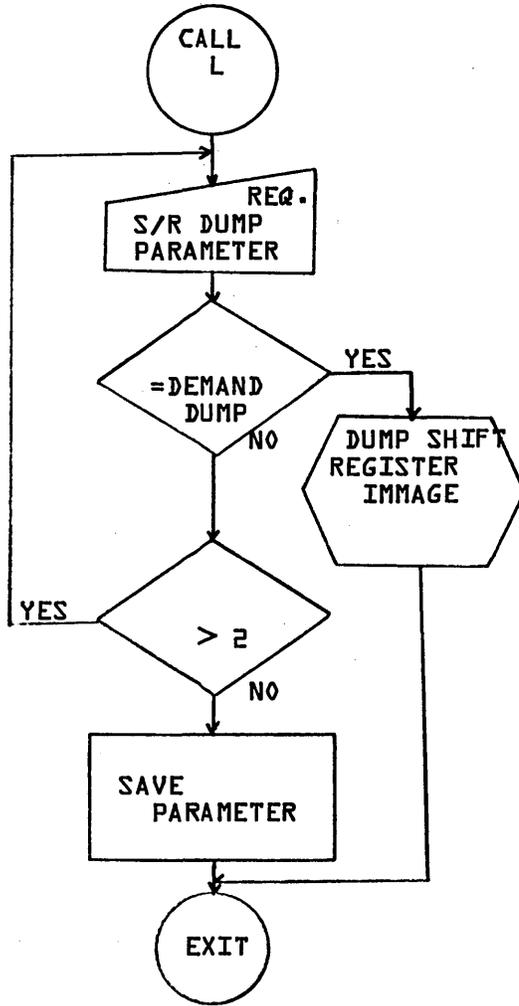
fc3



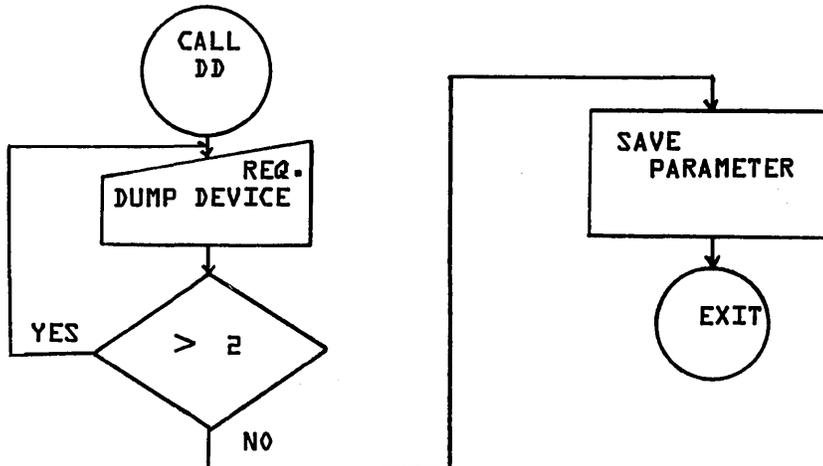
FF406 EQUIPMENT CODE



S/R DUMP PARAMETERS

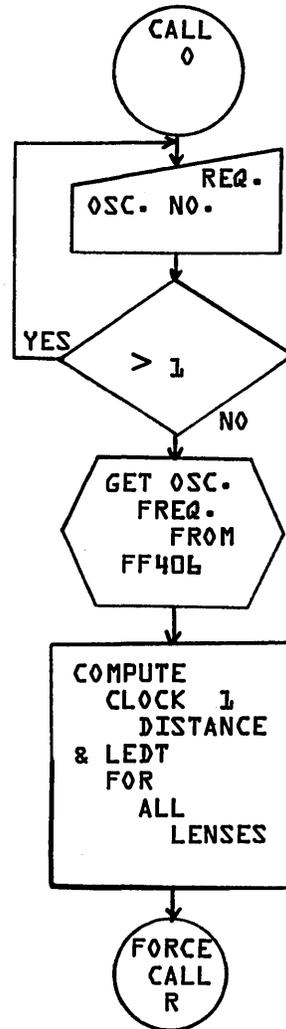


S/R DUMP DEVICE



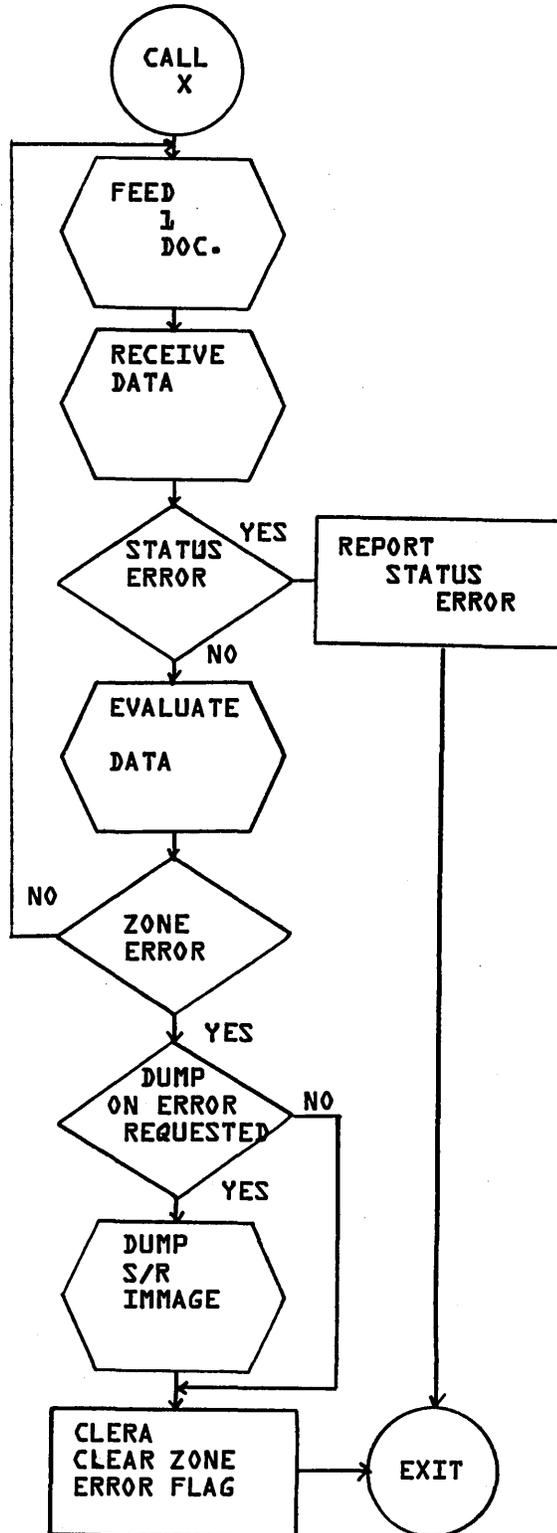
SELECT OSCILLATOR

fc4



EXECUTE TEST

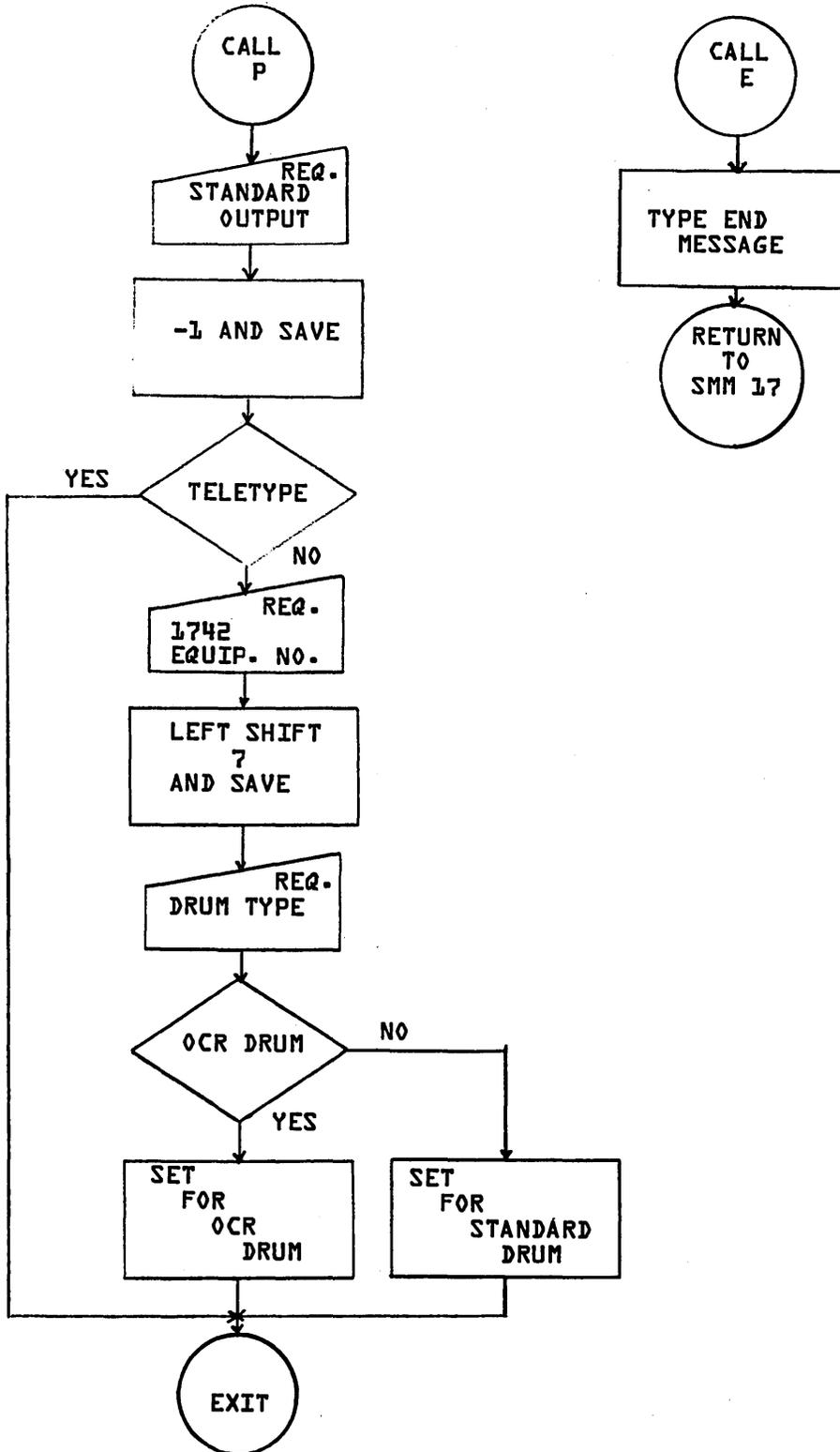
fc5



STANDARD {ERROR} OUTPUT

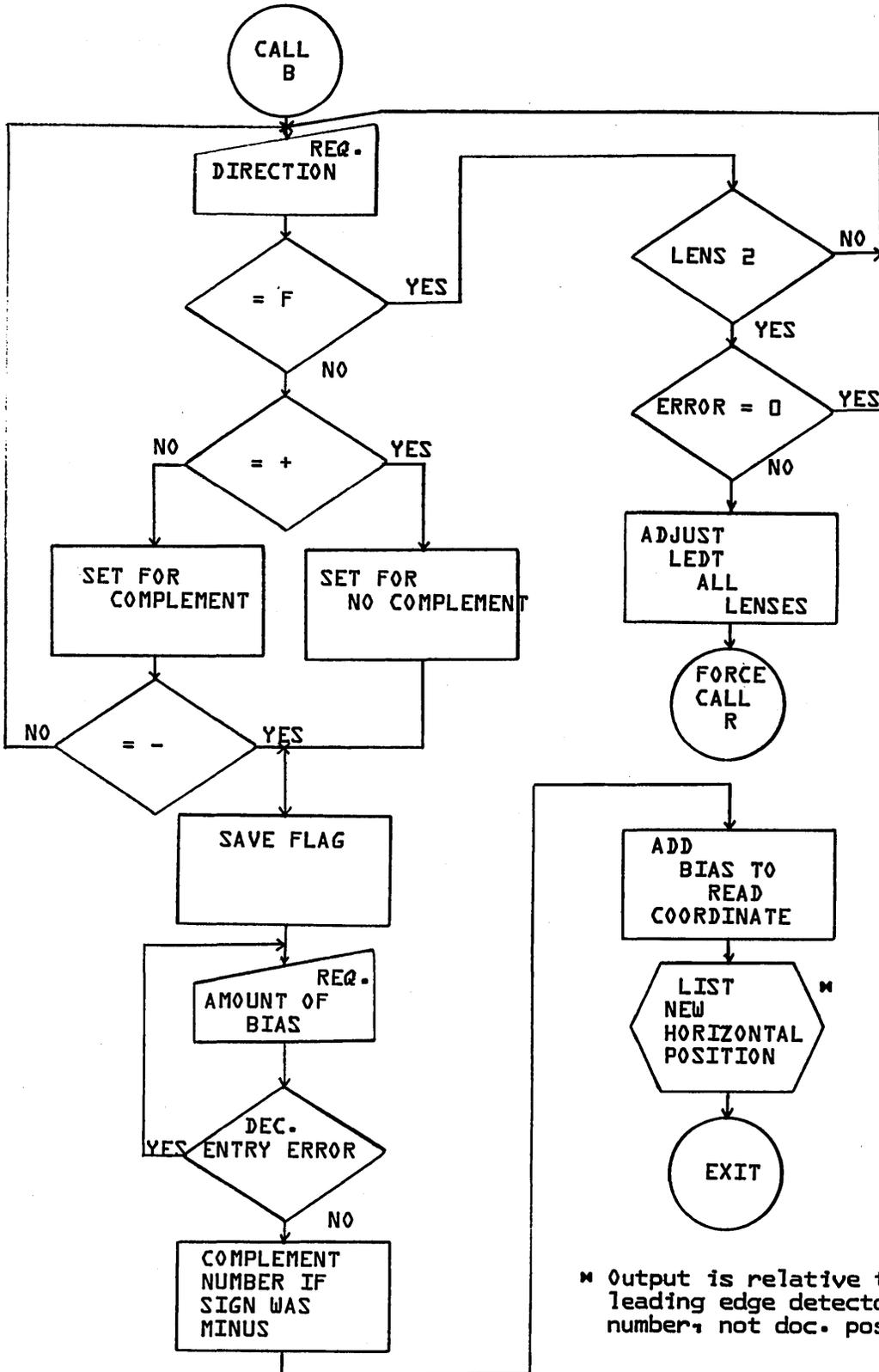
END TEST

fcb



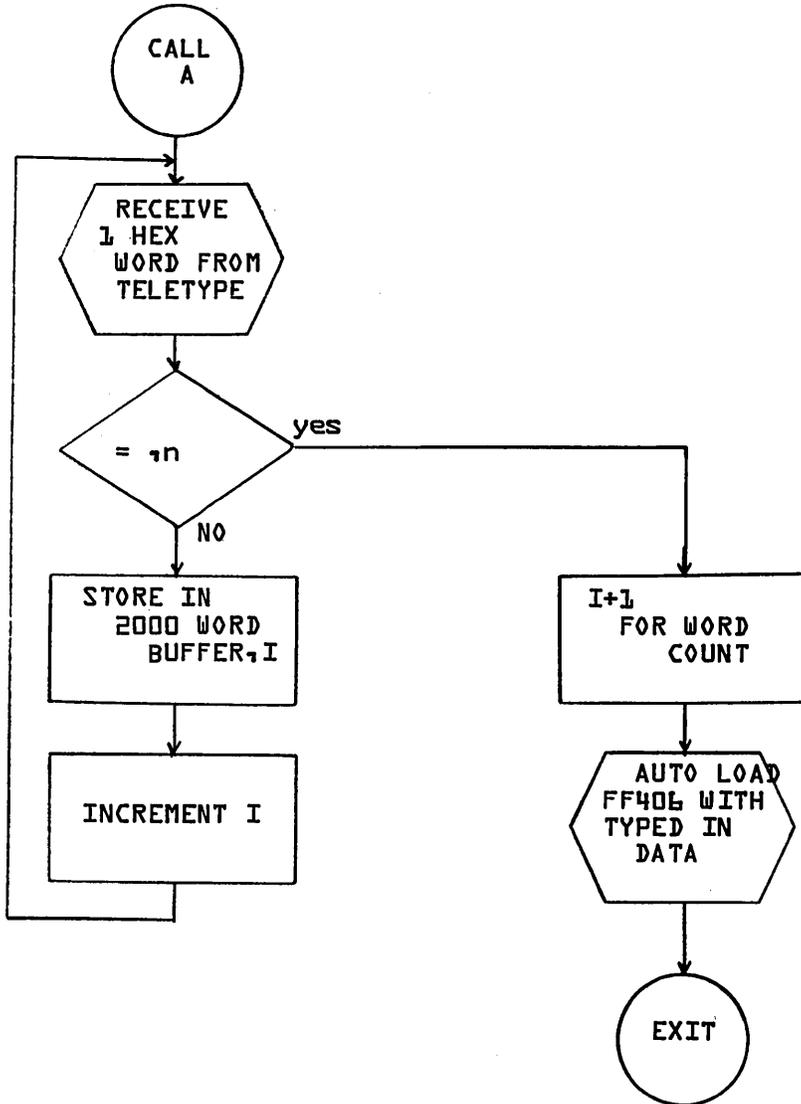
BIAS READ COORDINATE

fc7

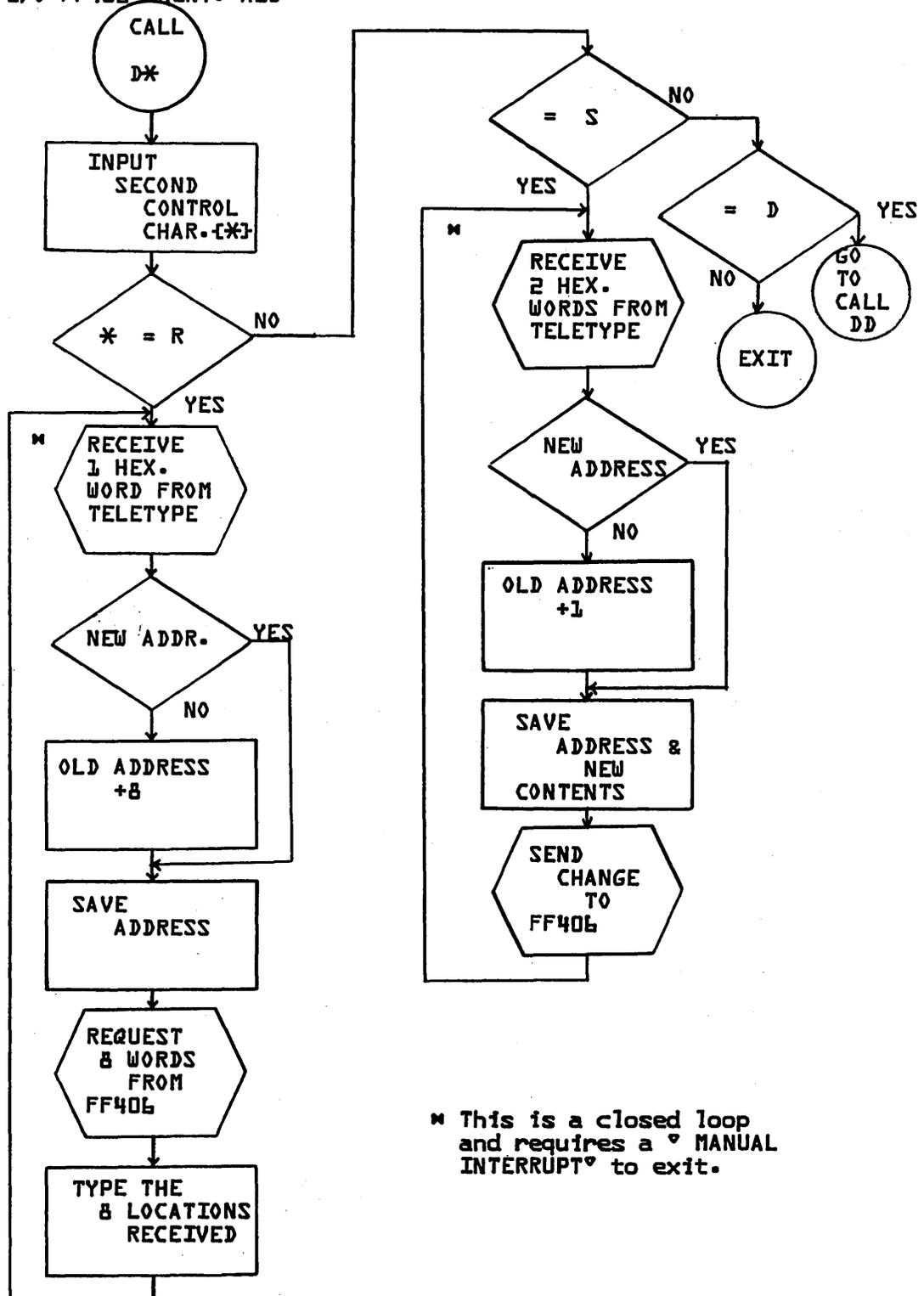


* Output is relative to leading edge detector number, not doc. pos.

AUTO LOAD MAINT. AID



I/O FF406 MAINT. AID



* This is a closed loop and requires a MANUAL INTERRUPT to exit.

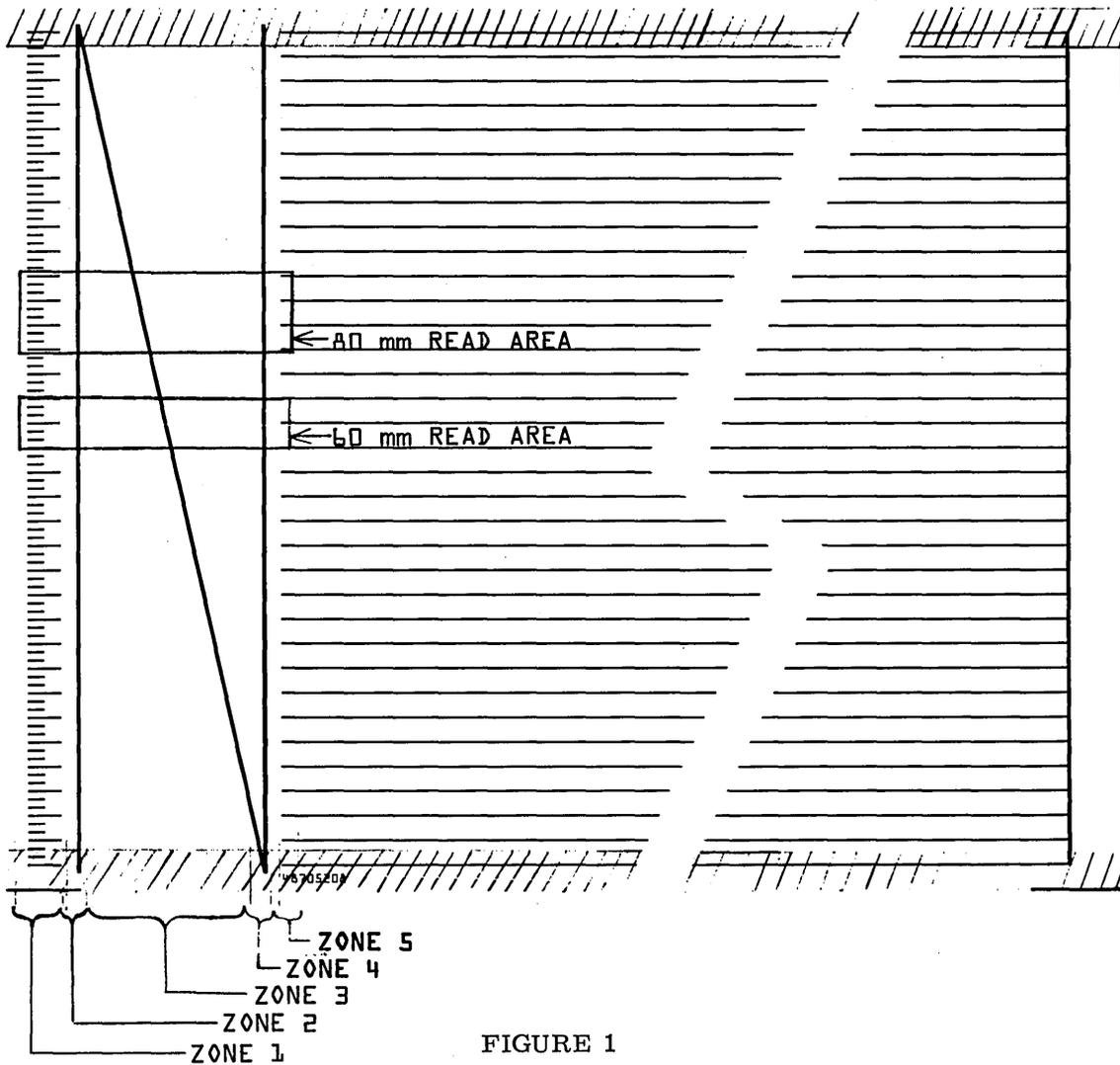


FIGURE 1

NOTE

If any of the crosshatched area appears in the read area, evaluation will not be performed.

Read areas are marked off for fast clock and low density selected.

To select low density, set locn. 5 in the B. C. = 0.

TABLE 1

Zone	Characteristic Checked
1	MAGNIFICATION, SKEW
2	CLOCK, VERT. POS.
3	VERT. POS.
4	CLOCK, VERT. POS.
5	SKEW

TANGENT TABLE

	0°	1°	2°	3°	4°	5°
0	.00000	.01746	.03492	.05241	.06993	.08749
2	.00058	.01804	.03550	.05299	.07051	.08807
4	.00116	.01862	.03609	.05357	.07110	.08866
6	.00175	.01920	.03667	.05416	.07168	.08925
8	.00233	.01978	.03725	.05474	.07227	.08983
10	.00291	.02036	.03783	.05533	.07285	.09042
12	.00349	.02095	.03842	.05591	.07344	.09101
14	.00407	.02153	.03900	.05649	.07402	.09159
16	.00465	.02211	.03958	.05708	.07461	.09218
18	.00524	.02269	.04016	.05766	.07519	.09277
20	.00582	.02328	.04075	.05824	.07578	.09335
22	.00640	.02386	.04133	.05883	.07636	.09394
24	.00698	.02444	.04191	.05941	.07695	.09453
26	.00756	.02502	.04250	.05999	.07753	.09511
28	.00815	.02560	.04308	.06058	.07812	.09570
30	.00873	.02619	.04366	.06116	.07870	.09629
32	.00931	.02677	.04424	.06175	.07929	.09688
34	.00989	.02735	.04483	.06233	.07987	.09746
36	.01047	.02793	.04541	.06291	.08046	.09805
38	.01105	.02851	.04599	.06350	.08104	.09864
40	.01164	.02910	.04658	.06408	.08163	.09923
42	.01222	.02968	.04716	.06467	.08221	.09981
44	.01280	.03026	.04774	.06525	.08280	
46	.01338	.03084	.04833	.06584	.08339	
48	.01396	.03143	.04891	.06642	.08397	
50	.01455	.03201	.04949	.06700	.08456	
52	.01513	.03259	.05007	.06759	.08514	
54	.01571	.03317	.05066	.06817	.08573	
56	.01629	.03376	.05124	.06876	.08632	
58	.01687	.03434	.05182	.06934	.08690	

1700/FF406/935 MODULE TESTS

(OC3A53 Test No. 53)

I. OPERATING PROCEDURE

A. RESTRICTIONS

1. The diagnostic interface to SMM17 only for loading.
2. The diagnostic requires a 12K 1700 system, a teletype, and a mag. tape (601,608,609,659).
3. Test parameters are accepted only from teletype.
4. SMM17 Mag. Tape must be mounted on Unit No. 0, Equipment No. 7.
5. Module tests may not be run in an off-line mode unless a 211 display is available.

B. OC3 LOADING PROCEDURE

Standard SMM17 call as test number 53.

Restart at P=047B.

C. PARAMETERS

1. Automatic (A)

Upon selection of the automatic parameter, the program will set up the I/O table for the selected module as follows:

Loading Device	= Mag. Tape (601,608,609)
Unit Number	= 1
Equipment Number	= 7
Interrupt Line	= 3
Converter Code	= 0
Output Device	= TTY
Output Level	= Normal
BC Equipment No.	= E
BC Interrupt Line	= 2

2. Manual

Following the initial test typeout the program will list all the manual parameters available as follows:

COMMON PARAMETERS

A = Automatic
B = 659 Tape Transport
C = Load Module to FF406
I = F F406 Interrupt Line
K = Off-Line
P = Program Output
Q = FF406 Equipment Code
X = Execute Test
Z = Reselect Module

ELECTRONIC READ AND VERIFY

D = Define Data
G = Quick Look
N = Image File Number
R = Read Parameters
T = Error Totals
U = Recirculate Character

LISTER TEST

L = Lister
M = Subtest

DOCUMENT HANDLING

F = Feed Parameters
M = Subtest
S = Sort Parameters
T = Error Totals

H. P. Electronic Read and Verify

Same Parameters as Module 1

Select Module = 1, 2, 3, 4, 5 =

The operator should now enter the number of the module tests to be run,
where:

Module Test 1 = Electronic Read and Verify

Module Test 2 = Lister Test

Module Test 3 = Document Handling Test

Module Test 4 = Operator Panel Test

Module Test 5 = H. P. Electronic Read and Verify

NOTE

The parameter list typeout above is divided into four groups. The parameters termed "Common" applies to any module test. Those listed after module test "Electronic Read and Verify" apply to module 1 and module 5. Those listed after module tests titled Lister Tests and Document Handling Tests apply to only that test. Note also that the above printout may be suppressed by depressing the MI on the teletype.

Once a module test has been selected, the program will solicit parameter selection by typing:

ENTER PARAMETER

Once a specific parameter has been selected, the program may request more information pertinent to the selected parameter.

Refer to Table 1 for Common Parameters

Refer to Table 2 for Module 1 and 5

Refer to Table 3 for Module 2

Refer to Table 4 for Module 3

D. AUTOLOAD MODULE PROCEDURE

1. Using Automatic Parameters

- a. Select automatic parameter (A).
- b. Select B parameter if tape transport = 659.
- c. Select C parameter.

See Table 1 for more information.

2. If Automatic Parameters Not Selected

- a. Specify BC interrupt line (I).
- b. Specify BC equipment code (Q).
- c. Select B parameter if tape transport = 659.
- d. Select C parameter (see Table 1).

E. MODULES' OPERATING PROCEDURE

1. Module 1. "Electronic Read and Verify"

Skip step a and b if the automatic (A) parameter was selected and there is no desire to change them.

- a. Specify output level and output device (P).
- b. Specify repetitions (M).

Skip step c if the read parameters have already been specified and there is no desire to change them.

- c. Specify Read Parameters (R). See Table 2.
- d. Specify File Number (N). See Table 6.
- e. Define Data (D). See Table 2.
- f. Execute Test (X).

QUICK LOOK TEST OPERATING PROCEDURE

Skip step a if the automatic parameter has been selected and there is no desire to change the output level or the output device.

- a. Specify output level and output device (P).

NOTE

Output level should be normal.

- b. Specify repetitions (M).

NOTE

For quick look repetition, count cannot be 0.

Skip step c if read parameters have already been specified and there is no desire to change them.

- c. Specify read parameters (R). See Table 2, Section 2.
- d. Select parameter G (see Table 2) and specify last file number to be tested. See Table 6 for file number selection.
- e. Select parameter D and enter 3 in response to = typeout.
- f. Execute test (X).

NOTE

The test must not be interrupted until the program displays on the output device the "End of Test" message.

2. Module 2. "Lister Tests"

- a. Specify lister or listers to be tested (L). See Table 3, Section 1.
- b. Specify subtest and repetitions (M). See Table 3, Section 2.
- c. Execute test (X).

3. Module 3. "Document Handling Tests"

- a. Specify subtest and repetitions (M). See Table 4, Section 2.
- b. Specify feed parameters (F). See Table 4, Section 1.
- c. Specify sort parameters (S). See Table 4, Section 3.
- d. Execute test (X).

4. Module 4. Operator Panel Test

- a. Execute test (X).

5. Module 5. "Handprint Electronic Read and Verify"

Skip step a and b if automatic parameter (A) has been selected and there is no desire to change the output or the repetitions.

- a. Specify output level and output device (P). See Table 1, Section 5.
- b. Specify repetitions (M).

Skip step c if the pitch has already been specified.

- c. Specify pitch (R). See Table 2, Section 4.

NOTE

MI (manual interrupt) after the pitch has been specified.

- d. Specify file number (N). See Table 2, Section 3. Refer to Table 6 for handprint file number selection.
- e. Define data (D). Enter 3 in response to D = .
- f. Execute test (X).

QUICK LOOK TEST OPERATING PROCEDURE

Skip step a if automatic parameter (A) has been selected and there is no desire to change the output device.

- a. Specify output device and output level (P).

NOTE

Output level should be normal. See Table 1, Section 5.

- b. Specify repetitions (M) (Range 1 - FFFF).
- c. Specify pitch (R). See Table 2, Section 4.

NOTE

MI after the pitch has been selected.

- d. Select G parameter. See Table 2, Section 2. Refer to Table 6 for last file number selection.
- e. Specify initial file number (N). See Table 2, Section 3. Refer to Table 6 for file number selection.
- f. Select D parameter and enter 3 in response to D = .
- g. Execute test (X).

NOTE

Do not interrupt (MI) the test until the program displays on the output device the "End of Test" message.

TABLE 1. COMMON MANUAL PARAMETERS

1. (B) 659 TAPE TRANSPORT

The program will type "=" in response to B entry.

Select the 3518 Equipment Code (1-6). If not selected, the program assumes Equipment Code 1.

2. (C) LOAD MODULE TO FF406

The program will type "=" in response to C entry. Define loading device: 1 = Mag. Tape, 2 = Paper Tape. If this is the first time the FF406 is being loaded with a module and automatic parameters were not selected, the program will type:

MT W, X, Y, Z = Where

W = Interrupt Line

X = Converter Code

Y = Equipment Code

Z = Unit Number

3. (I) FF406 INTERRUPT LINE

The program will type "=" in response to I entry. Define the interrupt line (2-F).

4. (K) OFF-LINE

The program will type:

ØC3, MOD X, Y OFF-LINE

Indicating that module test X is to run off-line on FF406 equipment number Y.

5. (P) PROGRAM OUTPUT

The program will type:

NORMAL = 1, SUPPRESS =2=

Entry of a 1 enables the program to output all error messages as they occur.

Entry of a 2 disables all output messages except for End of Test. Once the output level is selected the program will type:

LP = 1, TTY =2=

If the output device has already been selected, depress the MI (Manual Interrupt)

button, otherwise select the output device. If a 1 is entered, the program will type:

ØCR DRUM = 1, 8156-2=2=

If a 1 is entered, the program will convert data to match the ØCR Drum.

6. (Q) FF406 EQUIPMENT CODE

The program will type "=" in response to Q entry. Define the Equipment Code (3-F).

7. (X) EXECUTE TEST

Upon selection, the program transfers to the module residing in the FF406, the parameters required to run the test and the test begins. While the test is in progress, the operator may change or select parameters by using the MI.

8. (Z) RESELECT MODULE

The program will type:

MODULE SELECT = 1, 2, 3, 4, 5=

1 = Electronic Read and Verify Test

2 = Lister Tests

3 = Document Handling Tests

4 = Operator Panel Test

5 = Handprint Electronic Read and Verify Test

TABLE 2. MODULE 1 AND MODULE 5 MANUAL PARAMETERS

1. (D) DEFINE DATA

The program will type "=" in response to "D" entry. Select one of the following options:

DEFINE DATA ENTER 1

DEFINE SUBSET ENTER 2

LOAD ENTIRE FONT ENTER 3

If a 1 is entered, the program will type:

CHARACTER =

The operator may now enter up to 60 characters to define the set and sequence of characters of the previously selected font which he desires to test.

NOTE

1. A comma typeout following a character entry indicates a legal character.
2. If no comma typeout occurs, the entry is illegal (does not belong to the selected font). The program will ignore it and the operator may continue with the selection.
3. If a valid entry is made which the operator wishes to change, enter a "Rub-Out" followed by the change.
4. Data definition is terminated with a CR (Carriage Return) entry.

If a 2 is entered, the program will type:

X =

The operator should now enter the first character of the subset he wishes to test.

The program will respond:

SUBSET LENGTH =

The number of characters following the first which is to form the subset is entered as two hexadecimal digits.

If a 3 is entered, the program will load the entire selected image file to the FF406.

2. (G) QUICK LOOK TEST

The program will type "=" in response to G entry. The operator should now define the file number of the last font to be tested as two hexadecimal digits.

3. (N) IMAGE FILE NUMBER

The program will type "=" in response to N entry. The operator should now define the image file number as two hexadecimal digits or one hexadecimal digit followed by a CR.

4. (R) READ PARAMETERS

The program will type:

PITCH = 1, 2, 3, 4 =

The operator should now select one or more of the following options:

- 1 = Nominal Pitch (3 clear columns)
- 2 = Minimum Pitch (0 clear columns)
- 3 = Maximum Pitch (7 clear columns)
- 4 = Define Pitch

Entry of a 1 will cause the image to be passed through the 935 Shift register on a 22 column center.

Entry of a 2 will cause the image to be passed through the 935 Shift register on a 19 column center.

Entry of a 3 will cause the image to be passed through the 935 Shift register on a 26 column center.

Entry of a 4 will cause the program to type:

PITCH (0-F)=

The operator should now specify from 0 to F (-15) clear columns to be inserted between each character image as it is passed through the 935 Shift register.

NOTE

If more than one option is selected, the program will test each font for all the options selected before terminating the test.

EXAMPLE:

PITCH = 1, 2, 3, 4= 1 2 3 (CR)

The selected font will be tested for nominal, minimum, and maximum pitch.

After the pitch has been selected, the program will type:

OSC =

The operator should now specify the Oscillator as a 1 hexadecimal digit.

For more information refer to Table 3.

After the Oscillator has been selected the program will type:

CHAR-GROUP (0-6) =

If the character group have already been selected, enter (CR). Otherwise the operator should now select the 935 character groups to be enabled during the testing of the selected font. Terminate character group selection with a (CR) entry.

5. (T) ERROR TOTALS

The program will display the following summary on your selected output device

CHAR-READ WWWWWWW ERROR - CHAR = XXXXXXXX
 ERROR = YYYYYYYY REJECT = ZZZZZZZZ
 REF LINE =

Where W is the total number of characters read. X is the total number of characters which were either rejected or substituted. Y is the total number of characters substituted and Z is the total number of characters rejected. The Ref. Line will indicate which characters are being read.

6. (U) RECIRCULATE CHARACTER IMAGE

The program will type:

CHARACTER =

The operator should now enter the character which is to be recirculated through the 935 Shift register.

TABLE 3. OSCILLATOR SELECTION

Entry	Select
0	HFB
1	HFC
2	HFC
3	HFD
4	HFA
5	HFD
6	---
7	---
8	HFB
9	HFB
A	HFB
B	HFB
C	HFA
D	---
E	HFB
F	HFB

Type	Location	Function	Pitch	Frequency	Time / Column
HFA	C43	ØSCA	10/IN	2.74 MHz	60.6 Microseconds
HFB	C44	ØSCC	7/IN	1.92 MHz	86.7 Microseconds
HFC	C45	ØSCB	8/IN	2.19 MHz	75.7 Microseconds
HFD	C46	ØSCD	9/IN	2.47 MHz	67.3 Microseconds

TABLE 4. LISTER TEST MANUAL PARAMETER

1. (L) LISTER NUMBER

The program will type "=" in response to L entry. The operator should now define the lister or listers to be tested. Terminate selection with a (CR).

2. (M) SUBTEST AND REPETITIONS SELECTION

The program will type:

SELECT SUBTEST = 0, 1, . . . , 6 =

Entry of a 0 will cause subtest 1-5 to be executed once. If subtest 6 is selected, the program will type:

ENTER LISTER PATTERN =

The operator should now enter the lister print pattern. Sixteen entries are required and only valid lister characters are accepted.

VALID LISTER CHARACTERS = 0 1 2 3 4 5 6 7 8 9 \backslash C N S T

Once the lister print pattern has been specified or if a subtest other than 6 was selected, the program will type:

RIPPLE = 1, NON-RIPPLE=2=

Entry of a 1 will cause the lister print pattern to be left shifted end around one character per print.

If either subtest 1, 2, 3, 4, 5, or 6 was selected, the program will type:

RE=

The operator should now define the subtest repetition count. Hexadecimal Range 1 - FFFF. Terminate selection with a CR.

TABLE 5. DOCUMENT HANDLING MANUAL PARAMETERS

1. (F) FEED PARAMETERS

The program will type:

DOCUMENT LENGTH =XX=

The operator should now define the document length in tenths of an inch as two hexadecimal digits.

The program will type:

INTERDOCUMENT GAP =XX=

The operator should now define the interdocument gap in tenths of an inch as two hexadecimal digits.

The document length and interdocument gap determine the document throughput rate per the following equation:

$$T = \frac{.9 (75)}{L + 1}$$

Where T is the throughput in documents/second; L is the document length in inches; 75 is the transport speed in inches/second; .9 is the system efficiency; and 1 is the minimum document gap in inches.

2. (M) SUBTEST AND REPETITIONS SELECTION

The program will type:

SELECT SUBTEST = 0, 1, . . . , 8 =

The desired subtest is now entered. The program will continue by typing:

RE=

The operator should now define the subtest repetition count in hexadecimal. Terminate selection with a CR.

Range 1-FFFF.

3. (S) SORT PARAMETERS

The program will type "=" in response to S entry. The operator may now specify the sort pockets by number (1-2-3) in the sequence desired. Three entries are required.

4. (T) ERROR TOTALS

The program will display the following summary on the selected output device.

ERROR TOTALS C = XXXX LEDT = XXXX SST = XXXX

SCK = XXXX GAP = XXXX

Where in each case XXXX represents the total velocity or gap errors detected at the indicated photocell during the previous run.

TABLE 6. CHARACTER FONT IMAGES

Font	Number of Images	File Number	Stroke Width	Clock Enable
ASA	65	6	THIN	A or C
ASA	65	7	NOMINAL	A or C
ASA	65	8	THICK	A or C
407-1	14	9	THIN	A
407-1	14	A	NOMINAL	A
407-1	14	B	THICK	A
12F	14	C	THIN	A
12F	14	D	NOMINAL	A
12F	14	E	THICK	A
1428E	14	F	THIN	C
1428E	14	10	NOMINAL	C
1428E	14	11	THICK	C
1428	15	12	THIN	A
1428	15	13	NOMINAL	A
1428	15	14	THICK	A
7B	14	15	THIN	C
7B	14	16	NOMINAL	C
7B	14	17	THICK	C
7B INV.	14	18	THIN	C
7B INV.	14	19	NOMINAL	C
7B INV.	14	1A	THICK	C
407E-1	14	1B	THIN	D
407E-1	14	1C	NOMINAL	D
407E-1	14	1D	THICK	D
OCR-B	16	1E	THIN	A
OCR-B	16	1F	NOMINAL	A
OCR-B	16	20	THICK	A
E13B	14	21	THIN	B
E13B	14	22	NOMINAL	B
E13B	14	23	THICK	B

NOTE

See Appendix A for character image description.

TABLE 7

Font Name	Number of Images	File No.	Contents
ENCODER	21	1	0123456789@CSTX@+ -/= @
HP0	4	2	0000
HP1	10	3	1111111111
HP2	7	4	2222222
HP3	23	5	3333333333333333333333
HP4	10	6	4444444444
HP5	9	7	555555555
HP6	15	8	666666666666666
HP7	10	9	7777777777
HP8	19	A	8888888888888888888
HP9	12	B	9999999999999
HPC	4	C	CCCC
HPS	3	D	SSS
HPT	9	E	TTTTTTTTTT
HPX	12	F	XXXXXXXXXXXXXX
HPZ	5	10	ZZZZZ
HP+	13	11	+++++
HP-	1	12	-
HP=	2	13	==
N Rejects	21	14	
A Rejects	1	15	
S Rejects	2	16	
USA@	3	17	
HPE1	6	18	111111
HPE7	6	19	777777
Black Goodies	6	1A	222222
Features	16	1B	
Splits/Joins	27	1C	
Flats/Slopes	8	1D	

II. ERROR MESSAGES

A. COMMON ERROR MESSAGES

1. MT FAILED

The program received an internal or external reject while attempting to connect the tape driver.

Hint: Verify equipment code, unit number, and ready.

2. MT * PE

Mag. Tape parity error.

Hint: Verify selected density.

3. ILLEGAL AUX. TAPE

The program has detected that the module's record length is not 14 computer words as expected.

Hint: Make sure that your tape is positioned to the load point where there is the auxiliary tape.

4. ILLEGAL FILE NUMBER

The specified image file number is illegal. Refer to Table 6 for standard and optional fonts. Refer to Table 7 for Handprint fonts.

5. ENTRY ILLEGAL

The parameter entry is not in the \emptyset C3 library.

6. NO RESPONSE

The BC never replied with an interrupt to begin checksum operation after the module had been autoloaded.

Hint: Verify BC interrupt line.

7. CHECKSUM ERROR

The checksum computed on the module at the time it was autoloaded from mag. tape, is not equal to the checksum computed on the module while it was being transferred from the BC to the 1700.

Hint: Attempt autoload one more time, should it fail again, run BC2.

B. MODULE 1 ERROR MESSAGES

All error messages are prefaced by \emptyset C3, MOD X, Y:

Where X is the module test number and Y is the equipment number being tested.

1. NO DATA READY RESPONSE TO X

The image of the character X was not responded to by the 935 data ready within 10 columns after the image was centered in the matrix.

Hint: Verify specified character groups parameter.

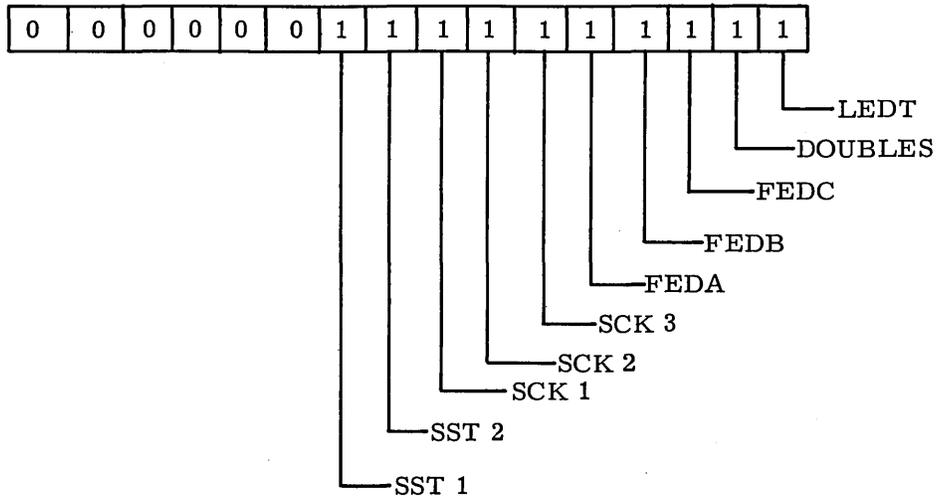
2. CHSREAD = XXXXXXXX ERT = XXXXXXXX ER = XXXXXXXX RE =
XXXXXXX
RE=RRR. . .
=EEE. . .
Printer Output Format.

C. MODULE 2 ERROR MESSAGES

1. EXP Y REC Z MSK F
A status error has occurred on lister X. Y represents the four-bit hexadecimal status expected, Z the status received, and F is the mask applied to the lister status word. The four-bit status word is broken down as shown below:
0001 (1) = READY
0010 (2) = LISTER PAPER LOW
0100 (4) = LISTER OUT OF PAPER
1000 (8) = LISTER BUSY

D. MODULE 3 ERROR MESSAGES

1. TTMG OFF
No change in the state of the 935 transport clock has been sensed within 2.0 msec.
2. STATIC TTMG ACT = XXX EXP = 667
The 935 transport clock is changing state, but it is not within 1 percent of 667 usec. per transition.
3. LIGHT PHOTOCCELL STATUS ACT XX EXP 03FF
Under static conditions (no document in the 935 system) a status error, indicating dark photocells has been detected. A description of the EXP status word is given below. A "0" bit in the ACT status represents a dark photocell.
4. DARK PHOTOCCELL STATUS ACT XXX EXP YYY
Status error detected when a document was entered into the system and photocells indicated by XXX have not gone dark by the time the document has reached a sort pocket. The description of the status word is the same as II. D.3.



5. TIME ON LEDT ACT XXX. XXX EXP YYY. YYY (MSEC)
The velocity at leading edge detector, computed from the document length specified by the operator, is not within 1 percent of 75 ips.
6. LOADED TTMG ACT XXX EXP 667
The transport clock is not changing within 1 percent of 667 μ sec when the transport is loaded with documents.
7. DVEL FAST/SLOW
The document velocity at Photocell C is fast (slow) as computed by comparing the specific document length to the length of time in TTMG pulses which photocell C is covered.
8. LEDTV FAST/SLOW
Same as II. D 7 but computed at leading edge detector.
9. SST X VEL FAST/SLOW
Same as II. D 7 but computed at sort station X photocell.
10. SCK X VEL FAST/SLOW
Same as II. D 7 but computed at sort check X photocell.
11. GAP ERROR
The interdocument spacing at leading edge detector in TTMG pulses is more than 0.5 inch smaller than specified by the GAP parameter.
12. STKR X FULL
The program has detected a stacker full condition at pocket X.
13. JAM AT SST X
The program has detected a jam condition at sort check X photocell.

14. JAM AT SCK X

Same as II. D . 13 but sort check at X photocell.

15. NO FEED

The program has not seen a document reach photocell B within 13.3 msec after pulsing the feeder vacuum.

16. FEED CHK

The program has detected a jam at photocell C.

17. TRANSCHK 1

The program has detected that the leading edge photocell has been covered for the duration of 1 1/2 document lengths.

18. TRANSCHK 2

The program has detected that a document which passed leading edge did not reach sort station 1 photocell within 557 msec.

19. XXXX DOCUMENTS FED IN YYYY MINUTES

Documents throughput rate since the last execute test command.

E. MODULE 4 ERROR MESSAGES

1. STOP SET

The program was expecting the START switch to be depressed and sensed apparent depression of the STOP switch.

2. START SET

The program was expecting STOP to be depressed and sensed apparent depression of the START switch.

3. END OF TEST

The program sensed apparent depression of the EOF switch.

F. MODULE 5 ERROR MESSAGES

1. CHAR-READ = XXXXXXXXX E=XXXXXXXX S=XXXXXXXX R=XXXXXXXX

REFERENCE LINE =

NUMERIC LINE =

ALPHA LINE =

SYMBOL LINE =

NOTE

- (1) The symbol indicates reject.
- (2) An E in the Numeric, Alpha, and Symbol line indicates ERROR.
- (3) An N in the Numeric, Alpha, and Symbol line indicates that the 935 did not generate a character data ready.

III. TEST DESCRIPTION

A. INITIALIZATION

Type beginning test typeout and parameter list and stop to receive parameters.

B. OPERATION

The diagnostic consists of six distinct programs. Five run in a selected FF406 and the other is a 1700 program which loads the FF406 programs and communicates normal and error messages to the operator. The diagnostic will run up to 15 935/FF406 stations simultaneously.

1. Module Test 1 - Electronic Read and Verify

a. Purpose

Test the 935 read logic electronics.

b. Procedure

The block diagram in Figure 1 indicates the portions of the 935 being tested here:

Basically, the program sends the character images to the 935 Load register via the FF406 special channel and tests for proper recognition by examining the character codes sent out by the 935 character encoder. A detailed description of the FF406 program operation is presented below prefaced by a discussion of FF406 special channel operation.

Execution of the FF406 OUT instruction causes one 16-bit word to be transferred from the FF406 memory to the special channel X register. All FF406 operation ceases at this point until the special channel responds to the FF406 with a RDYRES signal. The special channel awaits a CSYN (column sync) signal from the 935 and then sends one X register bit with each subsequent 935 Odd Clock signal until all 16 bits have been sent. The special channel data are received at the bottom of the 935 Load register and are vertically shifted upwards in the Load register during 935 even clock times. When all 16 X register bits have been sent to the 935 the special channel sends a RDYRES signal to the FF406. An immediate transfer from the FF406 memory to special channel X register occurs and the X register contents are again sent bit by bit to the 935. When the second 16 bit word has been sent to the 935, the special channel sends another RDYRES signal to the FF406 and forces white data to be sent to the 935 for the remaining 50 vertical shift clocks (until the next CSYN time).

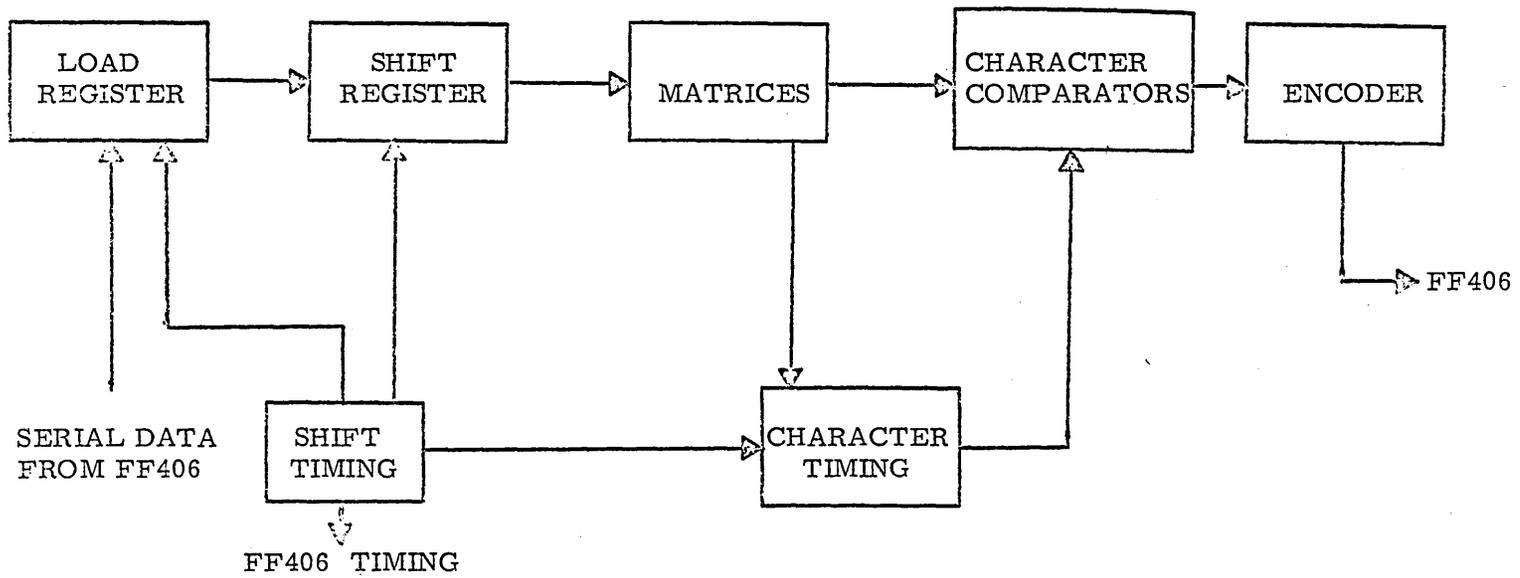


Figure 1. Block Diagram

The FF406 program is initialized with a group of character images prior to execute time. Each image requires 38 words of FF406 core storage. The set of ASCII character codes representing the images are also sent by the 1700 program to the FF406. At execute time the FF406 program begins to output the images by performing a series of two word outputs to the special channel. Each two word output transfers one vertical column of character data to the 935. During the latter 50 vertical shifts of the 935 Shift register, the FF406 tests for a Data Ready signal from the 935. If present, the program inputs the state of the 935 character encoder, translates the character code to ASCII, and performs various housekeeping functions before initiating the two word output for the next column. When all the images have been outputted the program compares the two sets of ASCII codes, updates character, reject and error counters and tests for End of Test conditions. In the event of a read error (reject or substitution) or End of Test, the FF406 sends the counters, the ASCII reference line, and the characters read in error on the previous pass to the 1700 for presentation to the operator.

The program provides great flexibility with regard to simulating the reading of virtually any character field. In addition to the sets of character images available, detailed in Appendix A, the operator may define the set and sequence of the character images, their stroke widths, and horizontal pitch.

2. Module Test 2 - Lister Tests

a. Purpose

Test 935 Lister(s)

b. Procedure

The Lister tests are divided into six subtests. If a subtest "0" is selected by the operator during initialization, the first five subtests described below are performed in order as one test.

1) Subtest 1

The first portion of this subtest prints the following pattern 256 times. Each line should appear legibly as shown.

0123456789 CNST

The second portion performs a 256 line rippleprint on the same character pattern.

2) Subtest 2

This test is designed to enable the operator to detect poor hammer response and tendency of the lister paper to skew. The pattern below is printed 256 times.

01 000000

The pattern is then reversed as shown below and again printed 256 times.

000000 01

Note should be taken that the print quality of the '1' in the above patterns is not significantly different than that of the '0's.

3) Subtest 3

This test exercises the lister data register with a worst case bit pattern. The line below is rippleprinted 256 times.

5C5C5C5C5C5C5C5C

4) Subtest 4

The following print sequence is repeated 32 times.

0000000000000000
1111111111111111
2222222222222222
3333333333333333
4444444444444444
5555555555555555
6666666666666666
7777777777777777
8888888888888888
9999999999999999
NNNNNNNNNNNNNNNN
SSSSSSSSSSSSSSSS
TTTTTTTTTTTTTTTT
CCCCCCCCCCCCCCCC
.....
XXXXXXXXXXXXXXXXXX (X's = single line space)

5) Subtest 5

This test is designed to determine the maximum lister print rate. The data pattern below is sent to the lister.

0123456789 CNST

The program then sends a print command to the lister whenever lister Not Busy status is detected. Using the 935 TTMG pulses for timing, this process is repeated for 1 minute, at the end of which, the program spaces the lister paper four lines and prints:

CNT XXXX

Where XXXX is the number of print commands sent to the lister during the minute. This number should not be less than 1800. Also, the actual number of lines printed shall be the same as XXXX.

6) Subtest 6

Subtest 6 is performed only if selected by the operator. This test prints the operator defined character pattern 256 times for each selected repetition.

With the exception of subtest 5 the FF406 program block diagram is as shown in Figure 2. If the lister status differs from that expected, the actual status is communicated to the 1700 for presentation to the operator.

3. Module Test 3 - Document Handling Tests

a. Purpose

To test the 935 document handling mechanics and electronics.

b. Procedure

The document handling tests are divided into eight subtests. If subtest "0" is specified by the operator, the subtests described below are performed in the order listed.

1. Subtest 1

The program first senses for a transition of the 935 TTMG signal. If no change occurs within 2.0 msec an error message indicating same is sent to the 1700 and the FF406 program halts. If the TTMG signal is switching, the program monitors the time between transitions. The time between transitions is sent to the 1700 when it is not within 1 percent of 667 μ sec and the FF406 program will halt.

2. Subtest 2

All of the document path photocells are tested for a light condition (not covered). The FF406 program will indicate to the 1700 program the status of the photocells in the event any are in an incorrect state. The FF406 program will not continue unless all photocells are in the proper state.

3. Subtest 3

The program feeds one document and sorts to pocket 1. As the document passes through the system the photocells are monitored for a light to dark transition. When the document is in the sort pocket the photocells are then tested for a light condition. Photocells not demonstrating a light to dark transition are sent to the 1700 for presentation to the operator.

4. Subtest 4

Same as III. B. 3. b. 3 above except the document is sorted to Pocket 2.

5. Subtest 5

Same as III. B. 3. b. 3 above except the document is sorted to Pocket 3.

6. Subtest 6

The program feeds one document and waits for leading edge detector to cover. Using the document length information specified by the feed parameters, the document velocity is calculated. A velocity not within 1 percent of 75 in/sec will cause the actual time the document covered leading edge to be sent to the 1700. The program will repeat this velocity check on 10 documents.

7. Subtest 7

The program feeds 16 documents at a 0.5 inch gap and waits for 5 of these documents to pass leading edge. With transport in this loaded state, the program monitors 935 TTMG. Again, the actual time between TTMG transitions is sent to the 1700 if it is not within 1 percent of 667 μ sec.

8. Subtest 8

This subtest is a general feed/sort routine. The feed rate and sort sequence are specified by the operator during initialization. After the execute test command is performed via the teletype, the FF406 program will await the depression of the 935 START switch before feeding any documents. As documents are moving through the system, the FF406 program performs the following checks:

Document velocity is monitored at photocell C (FEDC), leading edge detector (LEDT), sort station photocells (SST X), and at the sort check photocells (SCK X). Since the test uses 935 TTMG pulses and document length information for velocity calculations,

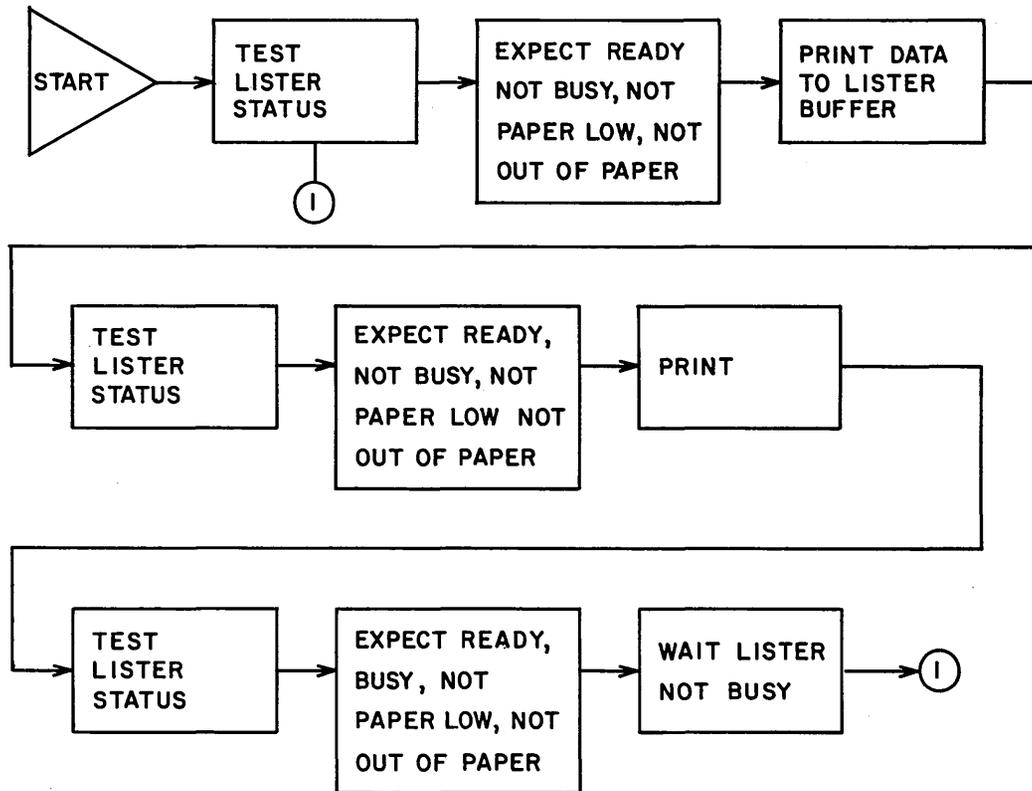


Figure 2. FF406 Program Block Diagram

the testing accuracy is only qualitatively sufficient. For example, if the document length is 3 inches and the document covers LEDT for 58 TTMG pulses, the program only knows that the velocity is more than 1 percent faster than 75 in/sec and indicates same with the message LEDTV FAST.

The program also monitors the interdocument gap at LEDT. A gap error is recorded if the gap becomes more than 0.5 inch less than that specified by the operator.

The program constantly monitors the document throughput rate by counting the documents fed and using the 935 TTMG pulses to update a minute clock.

All jams, doubles and no feeds are counted by the program and sent to the 1700 as they are detected.

With normal output selected, any error conditions detected by the above checks are presented as they occur to the operator via the selected output device. If for some reason, the 1700 has taken all existing error messages, the program will then start feeding again without any operator intervention.

In some cases, especially if a teletype is the only available output device, it will be more efficient to run this test with suppressed output. The operator may still obtain totals of the error conditions above through the "T" parameter at the end of test time.

In the event of a jam, the FF406 program will turn off 935 transport power and force a Stop condition. To restart, the operator must clear the jam conditions, turn on transport power, and depress the START switch. When a No Feed occurs, the program will light the NO FEED indicator and force a Stop condition. To continue, the operator must depress the START switch.

4. Module Test 4 - Operator Panel Test

a. Purpose

To test the 935 operator panel switches and indicators.

b. Procedure

After the execute test command is performed by the operator, the FF406 program awaits the depression by the operator of the 935 START switch. Once depressed, the program will light the START indicator and the NO FEED indicator. The program will now await the depression of the STOP switch. When depressed the program turns off the NO FEED indicator and turns on the STOP indicator. By repeating this START/STOP switch sequence, the program will turn a different operator panel indicator on and off each time. The order in which the indicators are lighted is as follows:

NO FEED
STACKER FULL
READER READY*
LISTER READY*
LISTER PAPER
FEED CHECK
TRANSPORT CHECK
SORT CHECK
LISTER CHECK

Depression of the EOF switch should cause it and all of the above indicators to light and also terminate the test with an end of test message. The error messages for this test, described above, are self explanatory.

NOTE

*The READER READY and LISTER READY indicators are located on the 935 maintenance panel.

5. Module Test 5 - Handprint Electric Read and Verify

a. Purpose

Test the 935 Handprint read logic electronics.

b. Procedure

Basically the program sends the character images to the 935 Load register via the FF406 special channel and tests for proper recognition by examining the character codes sent out by the 935 character encoder. A detailed description of the FF406 program operation is presented below prefaced by a discussion of FF406 special channel operation.

Execution of the FF406 OUT instruction causes a 16-bit word to be transferred from the FF406 memory to the special channel X register. All FF406 operation ceases at this point until the special responds to the FF406 with a RDYRES signal. The special channel awaits a CSYN *column Sync signal from the 935 and then sends one X register bit with each subsequent 935 Odd Clock signal until all 16 bits have been sent. The special channel data are received at the bottom of the 935 Load register and are vertically shifted upwards in the Load register during 935 even clock times. When all 16 X register bits have been sent to the 935, the special channel sends a RDYRES signal to the FF406. An immediate transfer from the FF406 memory to special channel X register occurs and the X register contents are again sent bit by bit to the 935. When 935, the special channel sends another RDYRES signals to the FF406 and forces white data to be sent to the 935 until the next CSYN time.

The FF406 program is initialized with a group of character images prior to execute time. Each image requires 38 words of FF406 core storage, except 50 words of FF406 core storage. The set of ASCII character codes representing the images are also sent by the 1700 program to the FF406. At execute time the FF406 program begins to output the images by performing a series of two word outputs to the special channel. Each two word output transfers one vertical column of character data to the 935. Between each column output, the FF406 tests for a Data Ready signal for the 935. If present, the program inputs the state of the 935 character encoder and performs various

housekeeping functions before initiating the two word output for the next column. When all the handprint images have been outputted the program stops reading. If the handprint images consist of FLATS SLOPES and SPLITS/JOINS, it will return to read otherwise, the program will monitor the Error bit in the Data Ready word and if present it will not attempt to translate the numeric alpha and symbol handprint code into ASCII. The program now compares the set of expected ASCII codes with received. Updates CHARS READ, ERROR, SUBSTITUTION, and REJECT counter and test for a read error (error, reject, or substitution) the program monitors the output level parameter, if suppressed it will return to read, else the FF406 sends the counters, the ASCII reference line, and the in error on the previous pass to the 1700 for presentation to the operator.

APPENDIX A

I. CHARACTER IMAGE DESCRIPTION

The character patterns used by Module Test 1 are designed to be contained within a 19 X 32 bit grid. The image for the ASA "E" character is shown in Figure 1. Different symbols are used to describe black portions of the image to enable differentiation of the nominal, thick and thin stroke width images. The thin stroke width image is represented by plus (+) symbols, the nominal by the plus and asterisk (*) symbols and the thick stroke width image by the plus, asterisk and slash (/) symbols.

Each image occupies one record on mag tape. The image information is stored on a column basis, the bit of Row 1, Column 1 occupying the first bit of the record and that of Row 32, Column 19 occupying the last. As the image is read in from mag tape, it is packed into 16 bit words, each column of the image requiring two (2) 16 bit words. Each image requires a total of thirty-eight 16 bit words (19 columns) of core.

II. IMAGE FILE DESCRIPTION

The 935 character fonts for which sets of images have been constructed are shown in Table 6. To enable greater testing flexibility, each font has images of nominal, max and min stroke width for each character. Table 1 below describes the mag tape library of character images giving file number, number of images, image stroke width and character font.

The order in which the images for each font are stored on mag tape is described below:

ASA - ABCDEFGHIJKLMNOPQRSTUVWXYZ0123456789

Δ ! * & : \$ = - () % . + ? / ' * ,) # ' (; () /

407-1 0123456789)-
12F 0123456789H-
1428E 0123456789-+
1428 0123456789H-.
7B 0123456789EP
7B INV 0123456789EP/
407E-1 0123456789-)/
OCR-B 0123456789+ (#- /
E13B 0123456789! "&-

/ FIELD MARK

COLUMN # 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

ROW #

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
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1700/935 SYSTEM TEST

(0C4A55 Test No. 55)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. 4K of memory is required to run the test.
2. SMM17 acts as the loading vehicle and receives control only at test termination.
3. The standard "AQAQ" message is replaced by descriptive error messages.
4. The user of this test must be familiar with the system controlware specifications.
5. ASCII mode must be selected in the read parameter mode word(s) for character reading.

B. LOADING PROCEDURE

Standard SMM17 call as test number 55.

C. PARAMETER

1. Fixed (none)
2. Manual

On receiving a manual interrupt, control is transferred to the "ENTER PARAMETERS" routine. If Phase I of the program is complete (see I. C. 3.), by typing in one of the following control characters, the appropriate routine is entered.

<u>Code</u>	<u>Routine</u>	<u>Description</u>
R	Accept read parameters	II. B. 3
X	Execute the test	II. B. 14
N	Select error printout level	II. B. 9
Y	Select error detection type	II. B. 8
TT	Print error totals	II. C. 2
TC	Print reference line	II. A. 3
F	Select feed parameters	II. B. 4
D	Select data definition method	II. B. 10
V	Do character Deletion/Addition	II. B. 15

<u>Code</u>	<u>Routine</u>	<u>Description</u>
Q	Select B. C. equipment code	II. B. 1
I	Select B. C. interrupt line	II. B. 2
L	Select Lister parameters	II. B. 7
S	Select Sort parameters	II. B. 5
P	Select Error output device	II. B. 11
C	Load B. C. controlware	II. B. 16
U	Unload MT output to new output device	II. B. 11, 17
E	End test	II. A. 2
M	Move sort char. position	II. B. 6

3. Forced (Automatic) Requests

- a. The program requests a list of standard calls. Should anything happen to prevent the normal flow of the program before the series is complete, the program will restart the list. The list is as follows:

Q, I, R, F, S, L, Y, N, D

- b. Until this sequence is complete, random selection of parameters will not be allowed.

4. STOP/JUMP Parameter Switch

The STOP/JUMP parameter can be changed in the "ENTER PARAMETERS" routine. It will be in "A" when the computer stops, just after a parameter entry if the SKIP switch is on. To change the switch, change "A" and run. The program makes use of the following bits:

<u>Bit</u>	<u>Function</u>
4	Repeat execution after error.
5	Master clear the B. C. and ship all parameters and execute after an error.
8	Suppress error output.
11	On autoloading, stop for a controller number change in "Q".

NOTE

If switch bits 4 and 5 = 0, the program will turn control over to the "ENTER PARAMETERS" routine after having issued a stop feed, if a status error occurs.

E. OPERATING INSTRUCTIONS

1. Load 0C4A55 via SMM17 operating instructions.
2. Respond with the correct entry via teletype.
3. Manual entries may now be made. If no other entries (other than X) are made, the following is assumed:
 - a. Teletype is to be the error output device.
 - b. The controller has been previously loaded.

"SAMPLE PARAMETER SET"

The following is a list of parameters to acquaint the beginner with the program operation. They are for a lens 2 Read on document numbers 48705201, 2, or 3. The height of lens 2 should be set to center one of the lines of the document in the optics.

READ PARAMETERS

CC9F	Mode word
0F04	Open shutter 2 at 0F0
1065	Start Read at 106
19E0	Close shutter 2 and stop Read at 19E
0000	Terminal parameters code

FEED PARAMETERS

00E	Demand Feed, 7.5" to 8.5" Document
-----	------------------------------------

PRINT LEVEL

- 1 Error totals, Reference line, and Error line.

DATA DEFINITION

- 1 Receive data Reference line via 935 Read.

ERROR DETECTION LEVEL

- 2 Character Rejects and substitutions.

II. MESSAGES

A. NORMAL MESSAGES

1. BEGIN 0C4A55 SYSTEM TEST IA = XXXX

Initial typeout where XXXX = the initial address of the program.

2. END 0C4A55 TEST

Final message of test in response to code (E). Error totals are printed automatically with this call just prior to this message.

3. ABC X ←

In response to code (TC), as well as other programmed controls, the Comparison (REFERENCE) line is output with an End of Field (record) code mark. The End of Document code is not output.

B. COMMAND MESSAGES

(All entries are in hexadecimal via the teletype unless other wise stated.)

1. TYPIN EQUIPMENT = X

In response to code (Q)*,
X = 0 → F = the FF406 equipment number.

2. INTERRUPT LINE = X

In response to code (I)*,
X = 2 → F = the FF406 interrupt line.

3. SELECT CONTROLLER READ TABLE

XXXX
YYYY
.
.
NNNN
0000

In response to code (R)*,
XXXX → NNNN = the read parameter table and XXXX itself = the initial mode selection. Regardless of one's position of entry, a rubout will erase the last full entry in the table and place the next entry back to that point.

*These entries are force called upon initialization of the program (See I. C. 3.)

NOTE

Sequential rubouts will cause sequential deletions but will never underflow position XXXX in the table. An all zero entry will terminate the list.

4. ENTER FEED FUNCTION XYZ = AAB

In response to code (F)*,

AA = The desired document gap in tenths of inches (HEX). 00 = demand feed.

B = The document size where:

2 = 2.5" → 3.5"

4 = 3.5" → 4.5"

6 = 4.5" → 5.5"

8 = 5.5" → 6.5"

A = 6.5" → 7.5"

C = 7.5" → 8.5"

NOTE

All entries not mentioned are illegal.

5. NO SORT = X

REJECT = Y

SORT DEFINITION = DZ N

In response to code (S)*,

X = the no sort stacker entry 1 → C

Y = the reject character stacker entry 1 → C

If D → N = 1 → C, then D → N = the sequential stacker sort order. A carriage return, or 30 entries, will terminate the entry.

If D = D, then Z → N is in alpha-numeric and represents the character from the read line (see next message) to be sorted to stackers 1 → B respectively. A (?) will delete that sequential pocket from use for data sorting. A carriage return or 11 entries will terminate entry. The stacker following the last defined stacker becomes the undefined character sort pocket. The computer will continue with:

*These entries are force called upon initialization of the program. (See I. C. 3.)

6. CHAR. POS. = NN

Also in response to code (M),

NN = 00→FF and defines the position of the character in the read line from which to do sorting.

NOTE

If data comparison or print mode (see X = 2 or 3 of message II. B. 8) is selected, documents not matching the reference line are sorted to the reject character stacker. To avoid this, (see X = 2 of message II. B. 10) define a no data reference line. This, however, deletes the following test.

A test is made to ensure more reliable sorting by comparing the length of the reference line against that of the read line. If the reference line is longer, that document will be sent to the character reject stacker. It will not be tallied as an error.

EXAMPLE:

NO SORT = 1

REJECT = 2

SORT DEFINITION = D??ABC? (cr)

CHAR. POS. = 01

The above specifies the following:

<u>Stacker</u>	<u>Collects</u>
1	No sort documents
2	Character and line length reject documents
3	A's
4	B's character position 01 =
5	C's second character of Read buffer
6	not used
7	All other documents

7. ENTER 1 = LIST, 2 = NO LIST, = X

In response to code (L)*,

X = 2 = Suppress Lister operation.

X = 1 = Use lister and the computer continues with:

LISTER UNITS = X N

LISTER DATA = Y N

LISTER LINES/DOC. = Z

ENTER 1 = RIPPLE, 2 = NO RIPPLE, = A

X → N = 1 → C indicating the listers to use in that sequential order. A carriage return or 12 entries terminates entry.

Y → N = 0000000000000000 → FFFFFFFFFFFFFFFF

is the data to output to all listers. Sixteen entries terminate this entry.

Z = 1 → F = The number of lines to print on each lister for each document feed.

A = 1 = Rotate the lister pattern from right to left one position for each print on that lister.

A = 2 = Maintain the pattern entered.

The following applies for data entries:

TELE	LIST	TEL	LIST	TELE	LIST	TELE	LIST
0 → D	9 = 0 → 9 C	A E	N .	B F	S SPACE	C	T

*These entries are force called upon initialization of the program. (See I. C. 3)

8. TYPEIN 1 = REJECT, 2 = ERROR, 3 = PRINT = X

In response to code (Y)*,

X = 1 = Tally only rejects and use level 1 or 2 for error output (see II. B. 9.).

X = 2 = Tally all errors and use level 1 or 2 for error output (see II. B. 9.).

X = 3 = Tally all errors and print all read data.

NOTE

All documents, having errors under the above conditions, will go to the selected reject stacker.

9. TYPEIN LEVEL = 1, 2 = X

In response to code (N)*,

X = 1 = yield error message II. C. 1 on detected errs.

X = 2 = yield error message II. C. 2 on detected errs.

10. TYPIN 1 = DOCUMENT, 2 = OPERATOR = X

In response to code (D)*,

X = 1 = Take reference line from document when execution takes place.

X = 2 = Enter the reference line via teletype and the computer continues with:

DEFINE DATA. TERMINATE FIELD DEF BY CR

The operator now enters the reference line via teletype and terminates each field with a carriage return and end of document with an additional carriage return. The error output device now receives the entire reference line as defined and includes each end of record termination code (see II. A. 3.).

NOTE

To define a no character reference line, enter only a double carriage return. Mark sense and hand print data can be defined by option 1 only.

11. ENTER 1 = TELETYPE, 2 = PRINTER, 3 = MT = X

In response to code P, (or U) see II. B. 17 for explanation, the error output device =

X = 1 = Teletype,

X = 2 = Printer and continues from II. B. 12,

X = 3 = Magnetic tape and continues from II. B. 13.

*These entries are force called upon initialization of the program. (See I. C. 3.)

12. 1742 EQUIPMENT = X

OCR DRUM = 1, 8156-2 = Y

X = 0 → F = the printer equipment number.

Y = 1 = Convert ASCII to the special code for the OCR type drum

Y = 2 = Standard print drum format.

13. MT = WXYZ = ABCD

A = 2 → F = Mag tape int. line.

B = 0 → 2 = Converter number. (Zero = No Converter)

C = 0 → F = Equipment number.

D = 0 → F = Unit number.

If this message is in response to code P, the characters NO are written to tape to space off of load point and identify the field start. If in response to code C, controller loading proceeds.

14. TYPIN 1 CLEAR TOTAL, 2 = NO CLEAR = X

In response to code X,

If X = 1, Totals are cleared,

If X = 2, Totals remain unchanged,

In either case, 1700/1736/935 operation begins. If define via document

X = 1 in message II. B. 10) the following message will be output after the first document is fed, read, sent to the no sort stacker, and normal message II. A. 3. is output.

ENTER 1 TO REPEAT, 2 TO GO = X

If X = 1, Another document is fed as above.

If X = 2, The last document read is used as the reference line and continuous execution begins. Execution will halt on the following conditions:

- a. A 1736 status error (see note below)
- b. A manual interrupt.
- c. No data is read from the document.

NOTE

If switch bits 4 or 5 are set, (see I. C. 4) execution will occur until a manual interrupt occurs. If both bits are clear, the 1700 will issue a stop read before going to the "ENTER PARAMETERS" routine.

15. ENTER CHTR DELETIONS

CHTR 00, 02, , NN =

In response to code V,

You can now delete characters from checking and the reference line. To do this, enter the hexadecimal position of that character. A carriage return ends the list of deletions and the computer continues with:

ENTER CHTR ADDITIONS

CHTR 01A, 00C, , NNB =

Characters can now be added to the reference line by typing its hexadecimal position and the character to add. A carriage return will end the list of additions. The computer will then output message II. A. 3.

16. LOAD CONTROLLER

In response to code C,

The system controlware should be loaded on a tape drive. The computer will follow this message with message II. B. 13.

On completion of the tape assignment, the following occurs:

- a. The tape will be rewound.
- b. A search for the controlware begins. *
- c. The controlware is loaded and checksummed.
- d. The controlware is reflected and checksummed.
- e. The checksums are compared.

*The controlware number is $100_{(10)}$ and is located in location 0001 of the program. If a different program number is needed, set bit 11 in the switch word. Before entering the tape parameters, set the SKIP switch. After the MT entry is made, the computer will stop. At this time, enter the test number into "Q" bits 00 → 07 (zero is illegal) and run.

A possibility of six errors can occur on loading which are II. C. 3 → II. C. 8.

17. When a code U is entered, an End of File is written on mag tape to mark the end of list. The request is then made (II. B. 11) to determine the dump device. When this is complete, the tape will be rewound and dumped to that device. This device now becomes the new error output device. Only one attempt is allowed to dump the tape. The format is 4-6-6 and Odd parity for every two ASCII characters.

C. ERROR MESSAGES

1. FLD A DOC B EDOC C CHTR D ERRS E REJT F

1A. ABCDEFGH←

1B. A _ I ←

A → F of line 1 represents the field number (two digits) and eight digits for the following: document count, error documents, character count, error characters (substitutions), and rejected character count respectively.

Line 1A represents the reference line and line 1B represents the errors placed directly below that character for which the error occurred.

On demand feed, all of the above will print out. On continuous feed, line 1 will be eliminated, line 1A will preprint once for all errors and line 1B will print with each error. All numbers are in decimal. Certain character conditions exist and are as follows:

- a. A space in error is represented by a printer underscore.
- b. A delete character symbol will strike out the two preceding characters in the Read buffer.
- c. Character checking is done only to the earliest End of Field symbol regardless of which line it occurs on. (Reference or Read.)
- d. Reject character sorts are done as soon as the first error is detected.
- e. Data or sequential sorts are done at the end of all character checking but prior to error message output.
- f. Hand print and mark sense have the same format, but each character is output as four hexadecimal digits followed by two spaces each and the End of Record codes are not printed.

2. DOC A EDOC B CHTR C ERRS D REJT E

In response to code (TT), or program demand, this is a truncation of message 1.

3. NO RESPONSE FROM BC

Self explanatory.

4. BC CHECKSUM ERROR XXXX

A checksum error has occurred while loading the B.C. XXXX = the reflected word count in hex.

5. NO RESPONSE FROM MT X
X = the MT unit number.
6. MT X STATUS ERROR
X = the MT unit number.
7. NO BC INT.
Five seconds have elapsed and no interrupt has been received from the B. C. as expected on autoloading.
8. PROGRAM NOT ON TAPE
The B. C. controlware was not on the unit specified.
9. NO DATA READ
Only an End of Record and End of Document were received as data. A forced status output follows.
10. ABNORMAL INT.
A call "F" was received from the B. C. The forced status, which follows, shows this.
11. NO B. C. INT. FUNC = XXXX
Five seconds of operation have elapsed with no interrupt from the B. C. as expected. XXXX = the last function request made. A forced status follows this message.
12. CONTROLLER REJECT XXXX
The B. C. has rejected the function XXXX.
13. STATUS ERROR XXXX

YYYY	RCS	(Read control status)
.	FCS	(Feed control status)
.	SSS	(Sort station status)
.	SFS	(Stacker full status)
.	SCS	(Sort check status)
.	SLX	(Lister select status)
ZZZZ	LRS	(Lister ready status)

XXXX = The system status which is in error or forced.

YYYY → ZZZZ are sub unit status followed by the code for that unit they represent. Any, all, or none may follow any system status message. Only those showing errors are printed.

14. LOST DATA SET

The lost data bit was set in the End of Document word from the B.C. The document will be sent to the reject stacker. If any data was read, it will be tallied.

III. DESCRIPTION

A. INITIALIZATION

1. Set brush back roller, doubles level, and feeder.
2. Load the 935 with documents and set the stackers for proper document length.

B. OPERATION

1. Purpose
 - a. To determine system operability.
 - b. To determine operability using customer parameters.
 - c. To isolate general problem areas for further testing using more comprehensive diagnostics.
2. Procedure

See attached flow charts for detailed operation procedure.

TABLE 1. DATA FORMAT

HAND PRINT

NUM	ALF	SPC	err	fdr	N	U	M	A	L	F	S	P	C	0	1	1	1
0	C	+			0	0	0	0	0	0	0	0	0				
1	S	-			0	0	0	1	0	0	1	0	0	1			
2	T				0	0	1	0	0	1	0	0	1	0			
3	X	=			0	0	1	1	0	1	1	0	1	1			
4	Z				0	1	0	0	1	0	0						
5					0	1	0	1									
6	sp.	sp.			0	1	1	0	1	1	0	1	1	0			
7	rej.	rej.*			0	1	1	1	1	1	1	1	1	1			
8					1	0	0	0									
9					1	0	0	1									
	sp.				1	1	0	0									
	rej.				1	1	1	1									

* rej. = code reject for respective group only.

err = read error Ex. shift register bit dropping.

fdr = character too high or low for recognition.

} both cause a character reject.

CHARACTER DATA

A	A	A-B	0	0	0	0	rej	0	0	0						
---	---	-----	-----	-----	-----	-----	-----	-----	---	---	---	---	-----	---	---	---

Where A represents ASCII code and B represents External BCD code.

MARK SENSE 10 and 12

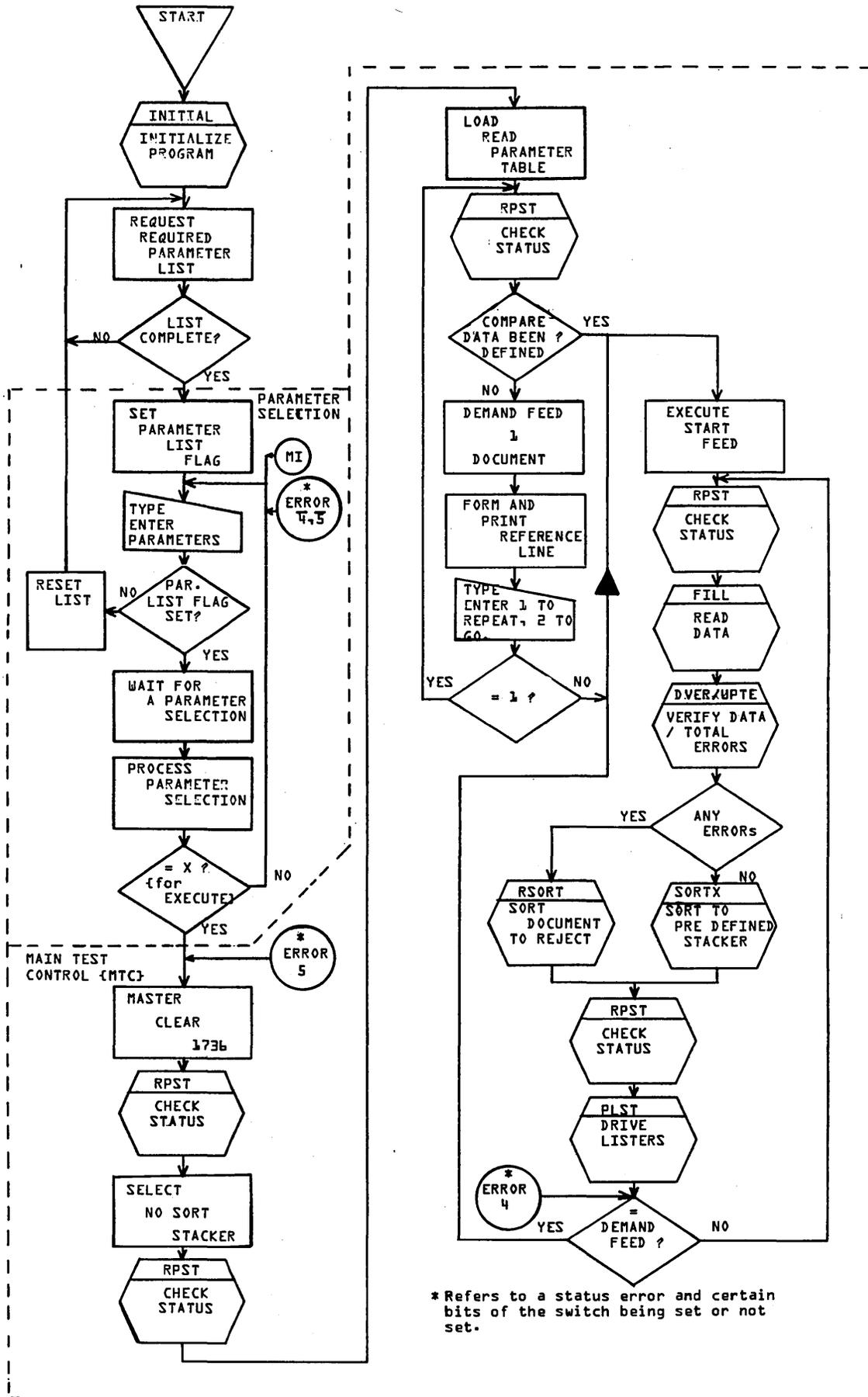
12	11	00	01	02	03	04	05	06	07	08	09	rej	0	1	1
----	----	----	----	----	----	----	----	----	----	----	----	-----	---	---	---

The digits 12 → 09 represent the bits position relative to a hollerith code position. Bits 12 and 11 are in mark sense mode 12 only.

HEX 935 TELE PRINT HEX 935 TELE PRINT HEX 935 TELE PRINT HEX 935 TELE PRINT

20	sp.	sp.	sp.	30	0	0	0	40	rej	@	@	50	P	P	P
21	!	!	!	31	1	1	1	41	A	A	A	51	Q	Q	Q
22	"	"	"	32	2	2	2	42	B	B	B	52	R	R	R
23	#	#	#	33	3	3	3	43	C	C	C	53	S	S	S
24	\$	\$	\$	34	4	4	4	44	D	D	D	54	T	T	T
25	%	%	%	35	5	5	5	45	E	E	E	55	U	U	U
26	&	&	&	36	6	6	6	46	F	F	F	56	V	V	V
27	'	'	'	37	7	7	7	47	G	G	G	57	W	W	W
28	{	{	{	38	8	8	8	48	H	H	H	58	X	X	X
29	}	}	}	39	9	9	9	49	I	I	I	59	Y	Y	Y
2A	*	*	*	3A	:	:	:	4A	J	J	J	5A	Z	Z	Z
2B	+	+	+	3B	;	;	;	4B	K	K	K	5B		{	{
2C	,	,	,	3C	4	<	<	4C	L	L	L	5C		\	\
2D	-	-	-	3D	=	=	=	4D	M	M	M	5D	△	}	}
2E	.	.	.	3E	#	>	>	4E	N	N	N	5E	—	†	^
2F	/	/	/	3F	?	?	?	4F	0	0	0	5F	eor	←	—

This table is arranged so as to accelerate troubleshooting for gained or dropped bits in the data transfer between equipments on the system. Going down, one looks for NX where N is known and X is suspect. Going across, one looks for XN.



1700/FF406/1700-I/O INTERFACE TEST

(BC1054 Test No. 54)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Sections 1 and 2 are primarily "go-no-go" tests. The error printouts obtained are not necessarily meaningful and indeed may not occur after an error because of a program "blow-up" in the FF406.
2. The diagnostic does not completely interface to SMM17. It will, however, permit time-sharing of the 1700 with other tests. Following is a list of SMM17 features which are not used.
 - a. Repeat Test Option (the tests repeat unconditionally).
 - b. Stop On Error.
 - c. Stop At End of Section.
 - d. Messages are not reported via the normal A, Q, A, Q sequence.
3. A 1700 with 8K of memory is required to load and run the diagnostic. (The FF406 programs are constant blocks in the diagnostic resident memory.)
4. Parameters are accepted only from the teletype (they may be re-entered at any time by setting the "re-enter parameter" bit in the SMM17 Stop/Jump word).

B. LOADING PROCEDURE

Standard SMM17 call as test number 54.

C. PARAMETERS

1. Automatic
None.
2. Manual

Manual parameters must be entered following the beginning test typeout. The program will type:

BC1 FF406 EQUIP =

One character, 0-F₁₆ must now be entered via teletype designating the FF406 equipment number.

After this entry the program continues:

BC1 X FF406 INTERRUPT LINE =

The FF406 interrupt line number 2-F₁₆ must now be entered. X is equipment number previously defined.

The program then continues:

BC1 X ENTER SECTION =

Desired test sections to be run must now be selected by means of a code 1-7. Bits 0, 1, and 2 of this hexadecimal digit correspond to sections 1, 2 and 3 and must be set to select the test section. Thus, an entry of 1, 2 or 4 would select respectively, section 1, 2 or 3. A 7 entry selects all three sections.

After the entry, the program continues:

BC1 X ENTER CR TO RUN =

A carriage return should now be entered to begin execution of the test. If a carriage return is not entered, the program re-requests manual parameters.

II. MESSAGES

A. NORMAL MESSAGES

1. BC1054 BEGIN FF406 TEST IA = XXXX

Beginning test typeout where XXXX is the test initial address.

2. BC1 FF406 EQUIP =

Parameter typeout requesting equipment code selection.

3. BC1 X FF406 INTERRUPT LINE =

Parameter typeout requesting interrupt line selection. X is the equipment number selected and is present on all typeouts after the select.

4. BC1 X PASS YY

Pass YY₁₆ though the test has completed.

5. BC1 X SECTION ZZ RUNNING
Section ZZ = 01-03 is currently executing.
6. BC1 X ENTER CR TO RUN =
Teletype carriage return entry request.

B. ERROR MESSAGE

1. BC1 X FF406 COMMAND ERROR ADDRESS YYYY
An error has occurred while executing the command test (Section 2). Address YYYY in the command test listing must be referenced to obtain information regarding the error.
2. BC1 X FF406 MEMORY
S REGISTER ERROR EXPECTED YYYY RECEIVED ZZZZ
Self-explanatory.
3. BC1 X FF406 MEMORY ERROR
ADDRESS AAAA EXPECTED YYYY RECEIVED ZZZZ
Self-explanatory.
4. BC1 X ECHO ERROR
EXPECTED YYYY RECEIVED ZZZZ
An error has occurred in section 3 while testing the 1700 I/O interface. YYYY is the word sent to the FF406 and ZZZZ the word received.
5. BC1 X FF406 NO RESPONSE
The FF406 has not responded with an interrupt within 6 seconds to a 1700 output in Section 3. The firmware is likely in an error hangup loop.
6. BC1 X AUTOLOAD EXTERNAL REJECT XXXX
The FF406 has externally rejected an autoloader output command. XXXX is the Q-word used.
7. BC1 X AUTOLOAD REPLY XXXX
Same as II, B. 6 except that the FF406 has replied to the autoloader output.
8. BC1 X INTERNAL REJ ON INPUT
A normal input from the FF406 was internally rejected.
9. BC1 X EXTERNAL REJ ON INPUT
An external reject was received following an input.

10. BC1 X INTERNAL REJ ON OUTPUT

Same as II. B. 8 except the command was an output.

11. BC1 X EXTERNAL REJ ON OUTPUT

Same as II. B. 9 except the command was an output.

III. TEST DESCRIPTION

A. INITIALIZATION

Type beginning test typeout and stop to receive parameters.

B. OPERATION

The diagnostic consists of 4 distinct program. Three run in the FF406 and the other is a 1700 program which primarily is used to load the FF406 programs and to communicate normal and error messages to the operator.

1. Section 1 (Memory Test)

a. Purpose:

Test the FF406 Memory and the S-Register.

b. Procedure:

1) Memory Test

The memory is checked in 1K increments beginning with upper memory. Four "worst" memory patterns are used.

Pattern 1:

<u>Address</u>	<u>Contents</u>
P	0000
P+1	FFFF
P+2	FFFF
P+3	0000
P+4	FFFF
P+5	0000
P+6	0000
P+7	FFFF
P+8	0000
P+9	FFFF
P+10	FFFF
P+11	0000
etc.	etc.

Pattern 2:

Complement of Pattern 1.

Pattern 3:

<u>Address</u>	<u>Contents</u>
P	0000
P+1	0000
P+2	FFFF
P+3	FFFF
P+4	FFFF
P+5	FFFF
P+6	0000
P+7	0000
P+8	0000
P+9	0000
etc.	etc.

Pattern 4:

Complement of Pattern 3.

Note

The addresses containing all zeros are "disturbed" periodically with non-zero quantities.

2) S Register Test

The S register is tested by writing 0XXX at memory address 0XXX, and verifying the address expression.

2. Section 2 (Command Test)

a. Purpose:

Test most* FF406 instruction commands.

b. Procedure:

Execute the following 23 sub-tests.

1) Unconditional jump

2) Non-zero jump (1 of 2).

*Input/Output instructions are not tested.

- 3) Positive jump.
- 4) Shift left.
- 5) Add/Subtract.
- 6) Load/Store.
- 7) Load/Store indirect.
- 8) Replace add one.
- 9) Non-zero jump (2 of 2)
- 10) Random non-zero jump.
- 11) Random add.
- 12) Random subtract.
- 13) Random logical product.
- 14) Random left shift.
- 15) Random exclusive or.
- 16) Random right shift.
- 17) Random odd parity jump.
- 18) Random skip A.
- 19) Random overflow skip.
- 20) Skip A lower.
- 21) Non-zero jump indirect.
- 22) Positive jump indirect.
- 23) Odd parity jump indirect.

3. Section 3 (1700 I/O Interface Test)

a. Purpose:

Test the I/O Interface Package and the 1700/FF406 transmission lines.

b. Procedure:

This test section consists of a 1700 program which autoloads a program to the FF406. The 1700 then outputs one word (a counter which ranges from 0000 - FFFF) to the FF406, waits for an interrupt, reads the FF406 and verifies that the data word output is the same as the word read. Two FF406 programs may be used. The program normally loaded is the "Comprehensive Echo Test". This is a FF406 program which monitors the I/O

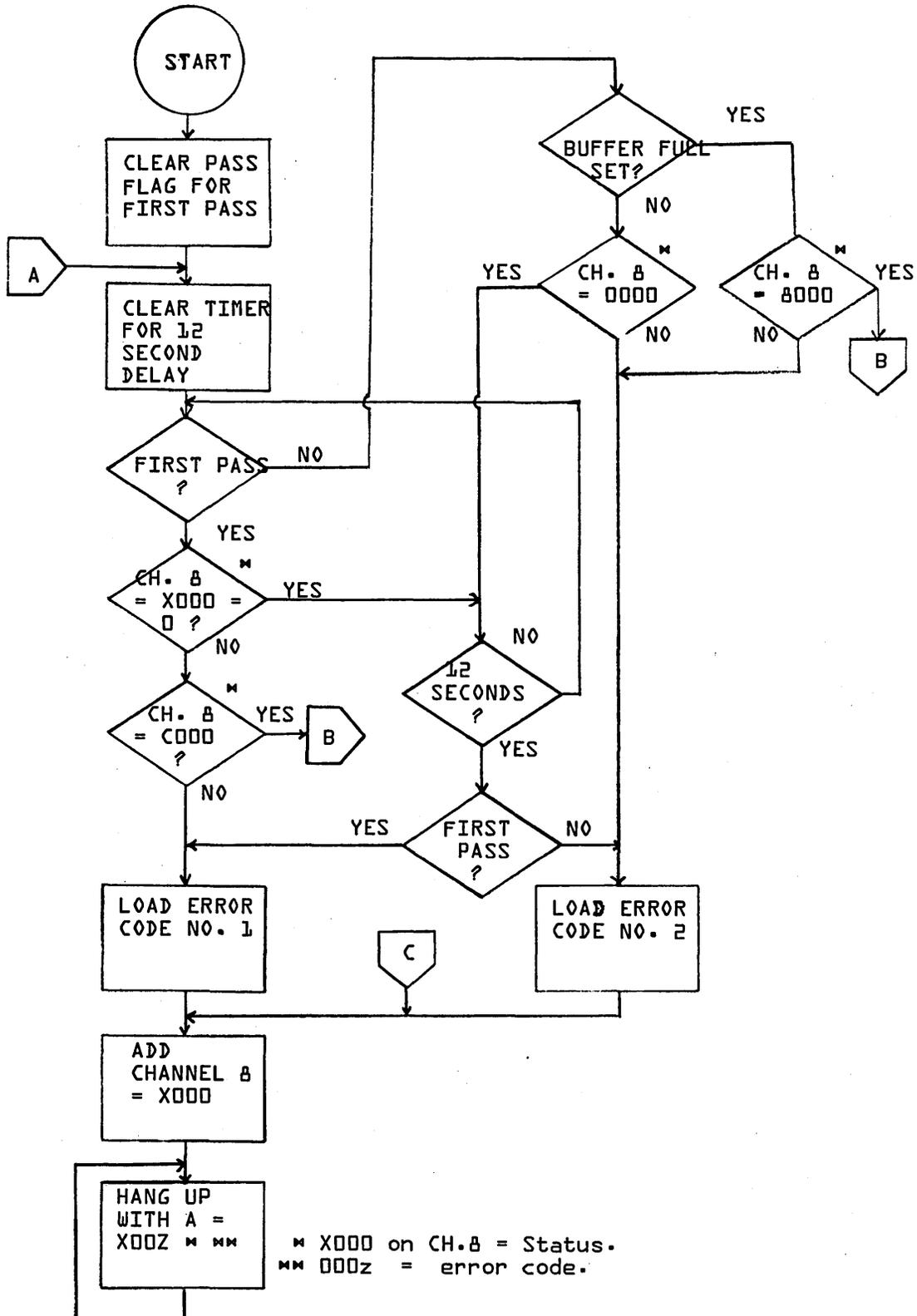
Interface Package flip-flops expecting a certain state at a given time. It will hang up displaying an error message in the A register if an error occurs. If the repeat condition bit of the SMM17 Stop/Jump word is set, the diagnostic loads the FF406 "Simple Echo Test". This program is similar to the "comprehensive version" but will not hang in an error loop and thus allows operation in FF406 "Step Mode" or permits the use of an oscilloscope to isolate a problem. See pages 227-8 and 227-10 for flow charts of the two programs.

Below is a description of the 1700/FF406 interaction. The numeric steps are 1700 operations and the asterisked steps that of the FF406.

- 1) Autoload FF406 with Echo Program. (comprehensive version)
- 2) Initialize data word counter to zero.
- 3) Output data word to FF406.
- *) Input data word, output data word, and set interrupt.
- 4) Wait 6 seconds for interrupt. If interrupt occurs, go to 8.
- 5) Type BC1 X FF406 NO RESPONSE.
- 6) If repeat condition bit is set, go to 14.
- 7) Go to 6.
- 8) Read FF406 and compare data word sent with data word received. If an incompare exists, type:

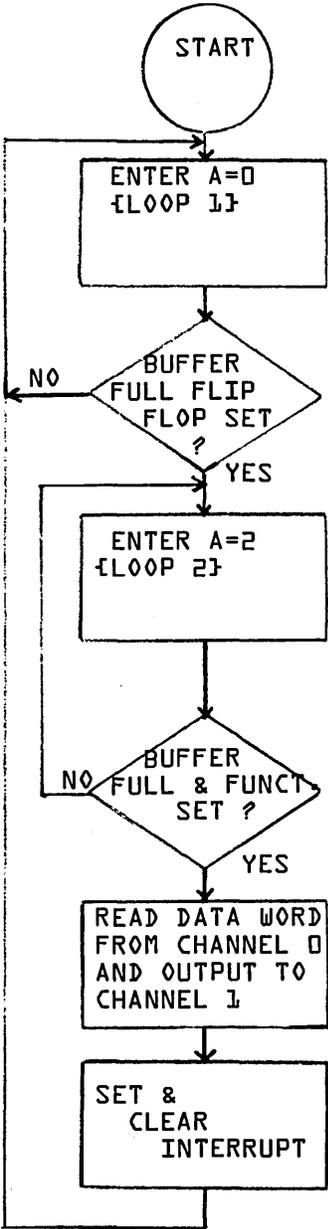
BC1 X ECHO ERROR
EXPECTED YYYY RECEIVED ZZZZ
- 9) Update data word + 1.
- 10) If data word = FFFF, go to 12.
- 11) Go to 3.
- 12) Repeat from 2 for two passes.
- 13) Exit section.
- 14) Autoload FF406 with Echo Program (simple version).
- 15) Go to 2.

FF406 ECHO PROGRAM (COMPREHENSIVE VERSION) fcd



FF406 ECHO PROGRAM
(SIMPLE VERSION)

fc2



1700/FF406 I/O Interface Test

	LDN	0	CLEAR PASS	000	C000
	STD	PASSCNT	COUNTER	1	0071
TIMER	LDN	0	CLEAR	2	C000
	STD	TIME	TWO WORD	3	0074
	STD	TIMER1	TIMER	4	0075
TIMER1	LDD	PASSCNT	TEST PASS COUNTER	5	1071
	NJN	TIMER3	GO TO BUFRFULL TEST	6	9020
	IAN	8	TEST	7	F108
	LPD	ETHOU	BUFRFULL,FUNCTION,RNI	8	4077
	STD	CHNL8		9	0072
	NJN	TIMER2	JUMP ONE SET	A	900C
	UJN	TIMER2A	CONTINUE TIME OUT TEST	B	8014
TIMER2	IAN	8	SAVE	C	F108
	LPD	ETHOU	CHANNEL 8	D	4077
	STD	CHNL8		E	0072
	LMD	CTHOU	TEST JUST BUFRFULL,FUNCTION	F	5076
	NJN	ERR1	GO TO ERROR #1	010	9051
	UJN	CHKOUT	EXIT THIS LOOP	1	802D
	LDN	0	*FILLER*	2	C000
	LDN	0	*****	3	C000
TIMER2A	A0D	TIME	TEST	4	7074
	LMD	OVERFLW	FOR	5	5079
	NJN	TIMER1	TIMER	6	9005
	A0D	TIMER1	OVERFLOW	7	7075
	LMD	FIVE		8	5078

	NJN	TIMER1	CONTINUE TIME TEST	019	9005
	IAN	&	SAVE	A	F108
	LPD	ETH0U	CHANNEL	B	4077
	STD	CHNL&	& AND	C	0072
	LDD	PASSCNT	G0 T0	D	1071
	NJN	ERR2	ERROR #2	E	9053
	UJN	ERR1	OR ERROR #1,	F	8051
TIMER3	IAN	&	TEST	020	F108
	LPD	BIT0	BUFRFULL	1	407C
	NJN	TIMER4	SKIP IF SET	2	902B
	IAN	&	TEST	3	F108
	LPD	SIXTH0U	FUNCTION	4	407E
	STD	CHNL&	RNI SET	5	0072
	NJN	ERR2	JUMP IF ERROR #2	6	9053
	UJN	TIMER2A	CONTINUE TIME TEST	7	8014
TIMER4	IAN	&	SAVE	8	F108
	LPD	ETH0U	CHANNEL &	9	4077
	STD	CHNL&		A	0072
	LMD	BIT0	TEST ONLY BUFRFULL SET	B	507C
	NJN	ERR2	G0 T0 ERROR #2	C	9053
CHK0UT	LDN	/FFF	0UTPUT	D	CFFF
	0AN	1	ALL 0NES	E	F601
	IAN	&	TEST	F	F108
	LPD	ETH0U	F0R N0	030	4077
	LDM	CHNL&	CHANGE	1	5072

	NJN	ERR3	GO TO ERROR #3	032	9055
	IAN	0	INPUT	3	F100
	STD	DATA	DATA	4	0070
	LMD	MASK1	TEST = FFFE	5	5078
	NJN	CHKIN		6	9038
	A0D	PASSCNT	UPDATE PASS COUNT	7	7071
CHKIN	IAN	8	TEST	8	F108
	LPD	ETH0U	CHANNEL	9	4077
	STD	CHNL8	8 CLEAR	A	0072
	NJN	ERR4	GO TO ERROR 4	B	905A
	LDD	DATA	OUTPUT	C	1070
	0AN	1	DATA WORD	D	F601
	IAN	8	TEST	E	F108
	LPD	ETH0U	CHANNEL 8	F	4077
	STD	CHNL8	STILL CLEAR	040	0072
	NJN	ERR5	GO TO ERROR #5	1	905C
	LDD	BIT0	SET	2	107C
	0AN	9	AND	3	F609
	LDN	0	CLEAR	4	C000
	0AN	9	INTERRUPT	5	F609
	IAN	8	TEST	6	F108
	LPD	ETH0U	RNI	7	4077
	STD	CHNL8	SET	8	0072
	LMD	BIT2		9	507D
	NJN	ERR6	GO TO ERROR #6	A	905E

	LDN	0	DELAY	04B	C000
	STD	MSDLY	96	C	0073
MILLS	A0D	MSDLY	US	D	7073
	LMD	DLYCT	F0R	E	507A
	NJN	MILLS	1700	F	904D
	UJN	TIMER	T0 RESP0ND	050	8002
ERR1	LDN	1	L0AD	1	C001
	UJN	ERRSTP	ERR0R	2	805F
ERR2	LDN	2	C0DE	3	C002
	UJN	ERRSTP	AND	4	805F
ERR3	IAN	8	ADD	5	F108
	LPD	ETH0U	CHANNEL	6	4077
	STD	CHNL8	8 AND	7	0072
	LDN	3	G0 T0	8	C003
	UJN	ERRSTP	ST0P 0N	9	805F
ERR4	LDN	4	ERR0R	A	C004
	UJN	ERRSTP		B	805F
ERR5	LDN	5		C	C005
	UJN	ERRSTP		D	805F
ERR6	LDN	6		E	C006
ERRSTP	ADD	CHNL8		F	2072
	UJN	*	STOP DISPLAYING ERROR CODE		
	BSS	15	& CHNL 8	060	8060

DATA	BSS	1	070	0
PASSCNT	BSS	1	1	0
CHNL8	BSS	1	2	0
MSDLY	BSS	1	3	0
TIME	BSS	1	4	0
TIME1	BSS	1	5	0
CTH0U	C0N	/C000	6	C000
ETH0U	C0N	/E000	7	E000
MASK1	C0N	/FFFE	8	FFFE
0VERFLW	C0N	/FF00	9	FF00
DLYCT	C0N	/0010	A	0010
FIVE	C0N	/000A	B	000A
BIT0	C0N	/8000	C	8000
BIT2	C0N	/2000	D	2000
SIXTH0U	C0N	/6000	E	6000

1700 / FF104 / 955 SYSTEM TEST

(RX1A30 Test No. 30)

I. OPERATING PROCEDURES

A. RESTRICTIONS

1. Requires a minimum of 8K 1700 with a 608 or 609, and a teletype.
2. The diagnostic interfaces to SMM17 only for loading.
3. Test parameters are accepted only from the teletype.
4. Complete control is given to the RX-1 monitor.
5. All entries are in hexadecimal.
6. The standard "A,Q,A,Q," error messages are not used. All errors are typed on the teletype or line printer.

B. LOADING PROCEDURE

1. The standard SMM17 call for 8K is test number 30.

C. PARAMETERS

1. Automatic
 - a. A standard I/O table is used by the RX-1 Monitor. All I/O parameters are defined in the Standard I/O Table (Table 1).
2. Manual
 - a. The Manual Interrupt button can be depressed at any time. All operations are stopped and control is transferred to the RX-1 Monitor. The monitor will type:

NEXT JOB

I

Entry by teletype can be accomplished only after the monitor has typed "Next Job", "I", and rings a bell. The monitor will wait for an input to be typed and then a carriage return. It is not necessary to type spaces. All entries are right justified.

To repeat the last entry, type 2 carriage return.

Teletype input formats are:

- 1) W
- 2) A, B or
 A(Z), B or
 A, B(Z) or
 A(Z), B(Z)
- 3) C, D(X)=Y

where:

W =

E = Output error totals (reference line not included).

S = Dump standard I/O table.

A = TTY = Teletype (in).

MT_x = Mag tape unit x (in).

PTR = Paper tape reader.

OCR = 955 Page Reader.

B = TTY = Teletype (out).

MT_x = Mag tape unit x (out).

PTP = Paper tape punch.

LPR = Line printer.

ABC = Autoload buffer controller.

C = C = Change standard I/O table.

D = TTY = Teletype input/output.

MTI = Mag tape input.

MTO = Mag tape output.

PTR = Paper tape reader.

PTP = Paper tape punch.

LPR = Line printer.

OCR = 955 Page Reader.

X = EQ = Equipment number.

INT = Interrupt line number.

MOD = Data handling mode.

FIL = Mag tape file number.

TFM = Mag tape format for each 16 bit 1700 word.

MRD = Mark document.

CV = Converter number.

CCC = Line printer carriage control characters.

PAR = TTY parity select.

OLC = Drive on-line character correction option.
SEL = Paper tape reader terminator selector.
DPA = Document ready page advance.
BSC = Buffer scan control.
POS = Mirror position.
ADV = Line stepping.
LCT = Line count/page.
EOL = Line terminate symbol.
ESP = Line terminate space count.
BLC = Blank line coordinate.
RSC = Line rescan count (on rejects).
CC = Cancel character.
DL = Delete character.
QL = Quantizing level.
SN2 = Scan mode.
KRL = Keep reference line.
IOT = Inhibit output.
SLL = Suppress line locate.

X = CMP = Comparison mode.
DCC = De-select cancel character.
DDL = De-select delete line character.
CPV = Character peak voltage.
HLT = Horizontal line thickening.
VLT = Vertical line thickening.
IMC = Initial mirror coordinate.
TMC = Terminal mirror coordinate.
FF_w = Field/font word w = 0 → 7.
IC_w = Initial field coord. w = 0 → 7.
TC_w = Terminal field coord. w = 0 → 7.

Y = _____ = A value for X. See I.C.2.c. for acceptable values.

Z = One of the temporary modes in the table below.

- b. The following is an option association table that goes with the format A(Z),B(Z). Any input device "A" in its allowable temporary mode (Z) can be output to any output device "B" in its temporary mode (Z).

A	(Z)	B	(Z)
OCR	PDM Packed data mode	MTx	BCD, BIN, ASC
	UCD Unpacked chtr data	TTY	BCD, BIN, ASC*
	SDM Servo data mode	PTP	BCD, BIN, ASC
	CPV Chtr peak voltage	LPR	BCD, BIN, ASC*
MTx	BCD, BIN, ASC	ABC	-----
TTY	ASC	* While ASCII is the only real mode, these entries will cause conversion to show representative data.	
PTR	BCD, BIN, ASC		

- c. The following is an association table that goes with format C,D(X)=Y; where C indicates a change in the standard I/O table is requested, D = the device to change, (X) = the unit to change, and Y = the actual change.

D	X	Y	Range	INIT.
OCR	EQ	Equipment no.	0 → F	A
	INT	Interrupt line no.	1 → F	7
	LCT	Lines/page	0 → FF	21
	ADV	Stepping increment/line	TABLE 2	2
	DPA	Units of .008" after doc. ready	0 → 3FF	2A
	POS	Mirror retrace position	00 → FF	10
	IMC	First coor. where read can start	00 → FF	28
	TMC	Terminating mirror coordinate	00 → FF	C0
	FFw	Font selection for field w.	TABLE 5	0
	ICw	Initial read coord. for field w.	00 → FF	0
	TCw	Terminal read coord for field w.	00 → FF*	0
	RSC	Rescan count/line (on reject)	0 → 7	0
	EOL	Line terminate symbol	ASCII chtr. in HEX	0
	ESP	Line terminate space count	0 → 7	2

*If a third digit ,=8, is added here, end of field codes are added.

D	X	Y	Range	INIT.
OCR	BLC	Blank line coord.	00 FF	50
	CC	Cancel character	ASCII chtr. in HEX	00
	DL	Delete line symbol	ASCII chtr. in HEX	00
	QL	Quantizing level	00 FF	80
	SN2	Scan mode	0 = Scan3, 1 = Scan2	0
	CMP	Compare mode	D = Print all, disable err. ck. E = Print all, enable err. ch. A = Print all errors only. R = Print all errors when rej. only. S = Print all errors when sub. only.	A
	DCC	De-select cancel chtr. selection		
	IOT	Inhibit output	Y = Yes, N = No	N
	SLL	Suppress Line Locate	Y = Yes, N = No	N
	KRL	Keep reference line	Y = Yes, N = No	N
	DDL	De-select delete line chtr. selection		
	CPV	Adjust chtr. peak reference	0 F	A
	HLT	Adjust horizontal line thickening	00 3F	30
	VLT	Adjust vertical line thickening	0 1	0
	MRD	Mark document on chtr. reject.	0 = No Mark, 1 = Mark	0
	BSC	Buffer scan control	TABLE 9	0
	OLC	Drive OLCC option	Y = Yes, N = No	N
LPR	EQ	Equipment no.	0 F	F
	MOD	ASC, BIN, BCD		ASC
	CCC	Carriage control characters	Y = Yes, N = No	N
MTI				
MTO	EQ	Equipment no.	0 F	7
	INT	Interrupt line no.	1 F	3
	CV	Converter no.	0 F	0
	MOD	ASC, BIN, BCD		BCD
	FIL	Mag. tape file no.		1
	TFM	Mag. tape format/1 1700 word		6
TTY	PAR	Parity select	1 = Even, 2 = Odd	
PTR	SEL	PTR terminator selector		

D. OPERATING INSTRUCTIONS

1. Set up the parameters for the desired operation via the format in (I. 0. 2. 1. 1).
(See I.D.5. for std. par.)

EXAMPLE 1: C,OCR(EOL)=4B

This would change the existing EOL symbol from a + to a K.

EXAMPLE 2: C,MTO(MOD)=BIN

This will change the output mag. tape mode to binary.

EXAMPLE 3: C,MTI(EQ)=3

This will change the input mag. tape equipment number to 3.

2. Execute the operation via the A(Z),B(Z) format in I. 0. 2. a. 2)

EXAMPLE 1: OCR(CPV),LPR

This will cause the 955 to read according to preset parameters and direct the output to go to the line printer. Character peak voltages will also be output.

EXAMPLE 2: MT1,LPR

This will cause the contents of mag. tape unit 1 to dump to the line printer. It is recommended that the tape would have been written in the ASCII mode to avoid time consuming conversion which may force the tape to hang up on slow systems.

3. The Reference Line

When operating the OCR in a reference mode (CMP = A, E, R, or S), a reference line will be read from the first line in the optics and output to the teletype for examination. To request that this line not be accepted, depress the rubout on the TTY and another attempt will be made to get a reference line from the 955. If the reference line is acceptable, a carriage return will put that line in the reference buffer as is. If corrections to that line are desirable, the following rules apply.

- a. Space to the undesired character and type in an * to delete checking that character or, type a character to substitute for it.
- b. When all correcting has been completed, a carriage return will cause the acceptance of the remainder of the reference line as is.
- c. When correcting hand print characters, the character input via TTY, determines the type of character to read. For example, if an alpha character is typed in, that character will always compare against the alpha extraction from the data read and the alpha portion of the read line will be output from now on for that character.

- d. Upon completion of the reference line, it will be output to the teletype in its corrected form and the requested operation will begin.

NOTE

In an error output only mode, the reference line will be output for every fifth error line.

A blank (space) character substitution error will appear as an underscore in the teletype error message.

- 4. Autoloading the FF104
 - a. MT^x, ABC
- 5. Standard (Preset) Parameters.
 - a. The parameters are initially set to allow execution of autoload from MT^x and running using the standard series of USASI test documents.
 - b. To review the standard parameters, see the column marked INIT of the table at I.C.2.c.
- 6. Character Peak/Servo Data
 - a. Character peak is a number representing the peak voltage at chtr. recognition time. It's value ranges from 0 through F. Ideally it should always = F. It's output format is the same as that for servo data.
 - b. Servo data represents the number of shifts in a vertical plane required to shift the character upward to the point of recognition. It is sent to the 1700 as a complemented value and has a range of 0 through 37 hex. The 1700 divides this number by 4, complements and outputs it following the character data in the following manner.

```

ABCDEFGHIJKLMN-----Z
77776666555444443333-----1*

```

The above values were used to illustrate the method of output and show the servo data in a possible skew situation. The right hand side would be higher in the optics than the left.

* A false indication is given when the character is rejected; as, a value is given where none was generated, i. e., the register is not cleared. The above values were used to illustrate the method of output and show the servo data in a possible skew situation. The right hand side would be higher in the optics than the left.

- c. In the FF104, servo data is used to determine topless and bottomless data and as a guide to the degree and direction of servo necessary to line locate. Zone 5 (see chart) is ideal positioning for the FF104. This falls into zones 3 and 4 of the RX1 output.

7. Hand Print

- a. In RX1, a code is used to determine the data for extraction on each hand-print character. It is initially set for all numeric data and can be changed when building a reference line. The basic hand-print data to the 1700 is as follows:

$2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$

1	0	0	CODE	NUMERIC	ALPHA	SYMBOL
---	---	---	------	---------	-------	--------

VALUE		C			
		N	A	S	O
		U	L	Y	D
		M	F	M	E
0	0	C	+		
1	1	S	-	L	
2	2	T		E	
3	3	X	=	I	
4	4	Z	R	H	
5	5	R	I	B	
6	6			I	
7	7	@	@	I	
8	8				
9	9				
A	R				
B	I				
C	I				
D	I				
E					
F	@				

where:

- E = Error
- I = Illegal
- L = Low
- H = High
- R = Controller Reject
- B = High and Low
- @ = Reject

b. To run using hand print, change the following parameters to:

(ADV)=0
(DPA)= (see Table 2)
(IMC)=2A
(TMC)=D4
(FF0)=7
(LCT)=0

These entries will allow continuous reading of the same line. The reference line for lines F and H must be modified at the teletype to the correct alpha or symbol as the basic mode of extraction is numeric.

c. On Line Character Correction Option

The OLCC option may be driven by entering the parameter C, OCR (OLC) = Y. *Each Reject Read will then be displayed on the tube. To continue test after each display, depress a rubout character. Actual character correction of rejected character is beyond the scope of RX1.

II. MESSAGES

A. NORMAL MESSAGES

1. BEGIN RX1A30 V2.0, IA = XXXX V3.1, CP03.

Initial typeout where XXXX = the initial address of the program.

2. NEXT JOB

I

The computer is waiting for an input.

3. THE B/C IS LOADED

The FF104 has been loaded correctly.

4. EOF

The end of file has been depressed on the 955. Normal message 5 will be output to the standard output device.

5. LINES = A CHTRS. = B SUB. = C REJ. = D

In response to command E or an EOF from the 955, the above message will output where, A,B,C, and D are 8 digit decimal numbers noting the number of lines read, characters read and compared, substitution errors, and reject errors respectively.

6. END OF RX-1

In response to command T, the RX1 test is terminated.

* A handprint reject typed and not displayed on OLCC indicates that not all extractions are rejected.
60182000 L

B. COMMAND MESSAGES

1. MANUAL INTERRUPT

The manual interrupt has been depressed. Message II. A. 2. will now be output.

2. READY OR EOF

In response to the 955 going not ready. If the end of file is depressed, see message II. A. 5. If the system is made ready (EOF not depressed) normal operation will continue.

3. CLEAR SKIP SWITCH

The SKIP switch is set while autoloading the buffer controller. Clear the SKIP switch.

C. ERROR MESSAGES

1. ILLEGAL ENTRY

Self-explanatory.

2. MT CHECKSUM ERROR FILE NO. XX.

The output checksum does not match with the input checksum. XX = the tape file number.

3. B/C CHECKSUM ERROR

A checksum error occurred while loading the FF104.

4. B/C FAILED TO RESPOND

The FF104 generated an external reject to a director function.

5. MT DOES NOT RESPOND

The mag tape externally rejected a function.

6. CHECK FF104 CONV. AND EQUIPMENT NUMBER

The 1700 internally rejected when trying to function the FF104.

7. Q REG. VALUE = XXXX

The value in the Q register at the time of a reject.

8. SYSTEM STATUS = XXXX

The 955 system status after an error.

17. BLANK LINE
Taken from 955 system status (lost data).
18. DOCUMENT NO SORT
Taken from 955 system status.
19. TRANSPORT FAULT OCCURRED THIS LINE
Taken from 955 system status.
20. LOST DATA
Taken from 955 system status.
21. LINE LOCATE AND DATA SKEW
Taken from 955 system status.
22. BLK.CH.FAIL, RUN BC2
One of 3 possible conditions exists and control is returned to the teletype.
The conditions are:
 - a. A reject when the status says that data is ready.
 - b. A reject before the data transfer is complete.
 - c. No reject when extra data is requested.
23. MT FORMAT ERROR
Mag tape format = 0.
24. UNDEFINED ALARM STATUS
An alarm status was received from the FF104 but, the remaining status does not indicate the error.
25. PRINTER ALARM
Self-explanatory.
26. AUTOLOAD REQUIRED
Taken from 955 system status.

III. TEST DESCRIPTION

A. INITIALIZATION

1. Load the standard set of test documents.
2. Put the 955 in a ready condition.

B. OPERATION

1. Purpose

- a. Determine the system operability.
- b. Isolate general problem areas for further testing using the more comprehensive diagnostics.

2. Procedure

- a. Execute the test using the A(Z), B(Z) commands.
EX: Read and print using the standard test documents. (See special considerations for hand-print I.D.7.b.) simply type:
OCR, LPR
- b. See attached flow charts for a detailed flow of OCR testing.

TABLE 1
STANDARD I/O EQUIPMENT TABLE

```

*****
EQUIPMENT *   7   *   7   *   F   *   A   *
INTERRUPT  *   3   *   3   *   -   *   7   *
MODE       *   1   *   1   *   3   *   3   *
FORMAT     *   6   *   6   *   -   *   -   *
CONVERTER  *   0   *   0   *   0   *   0   *
FILE       *   1   *   1   *   1   *   1   *
*****

```

NOTE

Mode = 1 = BCD, 2 = BIN, 3 = ASCII
Format = The frame arrangement in each
1700 word. Example: 66 would represent
12 bits or 2 frames in each 1700 16-bit word.

TABLE 2. PAGE ADVANCE

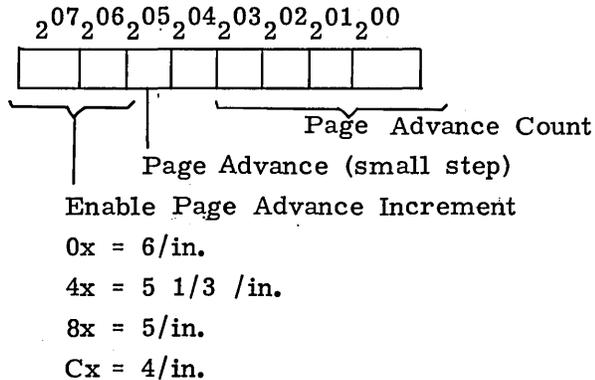


TABLE 3. 955 TRANSPORT STATUS

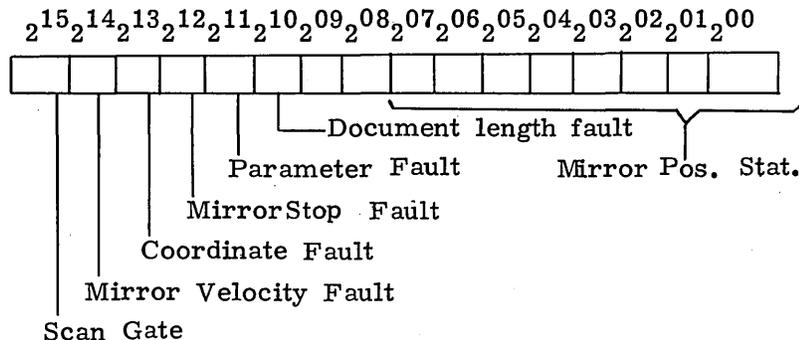
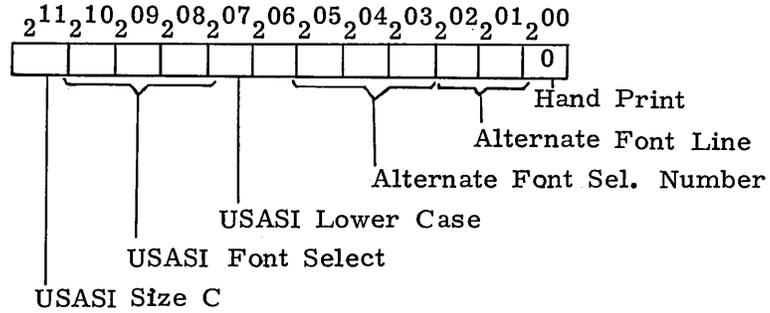


TABLE 4. ALTERNATE FONT (FF_w) w = 0 → 7



In Table 4, if $2^0 = 1$, the remaining bits change their meaning as follows:

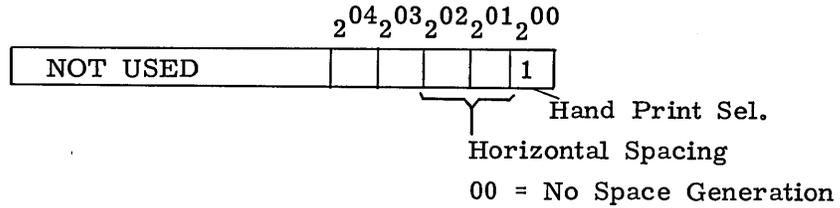


TABLE 5. ALTERNATE FONT LINE NUMBER (A02, A01)

Alternate Font Line	A02	A01
No Selection	0	0
Alternate Font Line 1	0	1
Alternate Font Line 2	1	0
Alternate Font Line 3	1	1

TABLE 6. ALTERNATE FONT HORIZONTAL CHARACTER PITCH (A05, A04, A03)

Font	Pitch	Size	A05	A04	A03
No Select	-----	-----	0	0	0
1403	10/in.	A	0	0	1
1428	10/in.	A	0	1	0
12F	10/in.	A	0	1	1
7B	7/in	C	1	0	0
N0F	10/in.	C	1	0	1
E13B	8/in.	A	1	1	0
OCR-B	10/in.	A	1	1	1

TABLE 7. ALTERNATE FONT HORIZONTAL CHARACTER PITCH (A04, A03)

Pitch	A04	A03
10/in.	0	0
8/in.	0	1
7/in.	1	0
Undefined	1	1

TABLE 10. READER AND CHARACTER CODES

Bit Position			7 6 5 4	# 0 0	# 0 1	# 0 1 0	# 0 1 1	# 1 0 0	# 1 0 1	# 1 1 0	# 1 1 1
3	2	1	0								
0	0	0	0			SP	0	REJ	P		p
0	0	0	1			Δ	1	A	Q	a	q
0	0	1	0			∇	2	B	R	b	r
0	0	1	1			#	3	C	S	c	s
0	1	0	0			\$	4	D	T	d	t
0	1	0	1			%	5	E	U	e	u
0	1	1	0			&	6	F	V	f	v
0	1	1	1			"	7	G	W	g	w
1	0	0	0			(8	H	X	h	x
1	0	0	1)	9	I	Y	i	y
1	0	1	0			* ↗	:	J	Z	j	z
1	0	1	1			+	;	K	unused	k	
1	1	0	0			,	=	L			
1	1	0	1			-	.	M		m	
1	1	1	0			.	/	N		n	
1	1	1	1			/	?	O	‡	o	

Column	Scan 3	Scan 2
45		
46		
47	B	<u>Topless</u>
48		
49		
50	C	1
51		
52		
53		
54	D	
55		
00		<u>Topless</u>
01		
02	0	2
03		
04		
05		
06	1	
07		
08		
09		
10	2	
11		
12		
13		
14	3	
15		
16		
17		
18	4	
19		
20		
21		
22	5	
23		
24		
25		
26	6	
27		
28		
29		
30	7	
31		
32		
33		
34	8	Bottomless
35		
36		
37		
38	9	
39		
40		
41		
42	A	<u>Bottomless</u>
43		
44		

Figure 1. Servo Data (RX1 VRS FF104)

(DPA) =

```
32   A_4 8 7 6 4 1 0 0
5C   B_1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 7 7 7 7 7 7
86   C_4 4 4 4 4 4 4 4 4 5 5 5 5 5 5 6 6 6 6 6 6 6 6 6 9 9 9 9 9 9 9
B0   D_0 0 0 0 0 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 0 1 2 3 4 5 6 7 8 9
DA   E_
104  F_C C C C C C S S S S S S T T T T T T X X X X X Z Z Z Z Z
12E  G_
158  H_+ + + + + + - - - = = = = = | | |
182  I_
1AC  J_0 1 2 3 4 5 6 7 8 9 0 0 1 1 2 2 3 3 4 4 5 5 6 6 7 7 8 8 9 9 | |
1D6  K_3 2 1 0 5 6 2 1 3 1 5 1 1 2 3 4 5 6 7 8 9
```

Figure 2. Hand Print Document as Seen in RX1 Reference Line

NOTE

Line K is shown as reading without space generation. If space generation is used, many controller rejects are to be expected. R type.

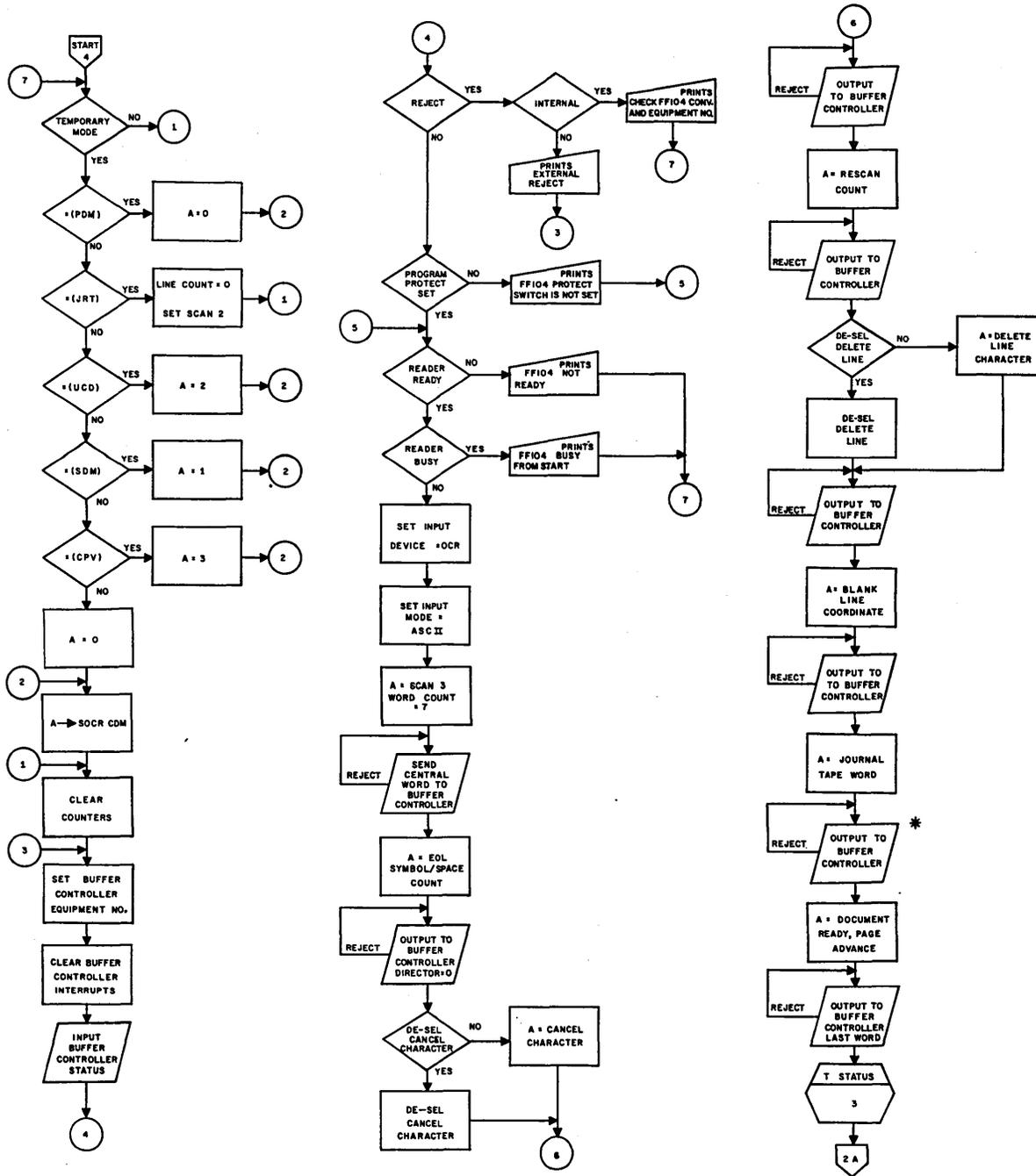


Figure 3. Flow Chart of RX-1 System Test (Sheet 1 of 5)

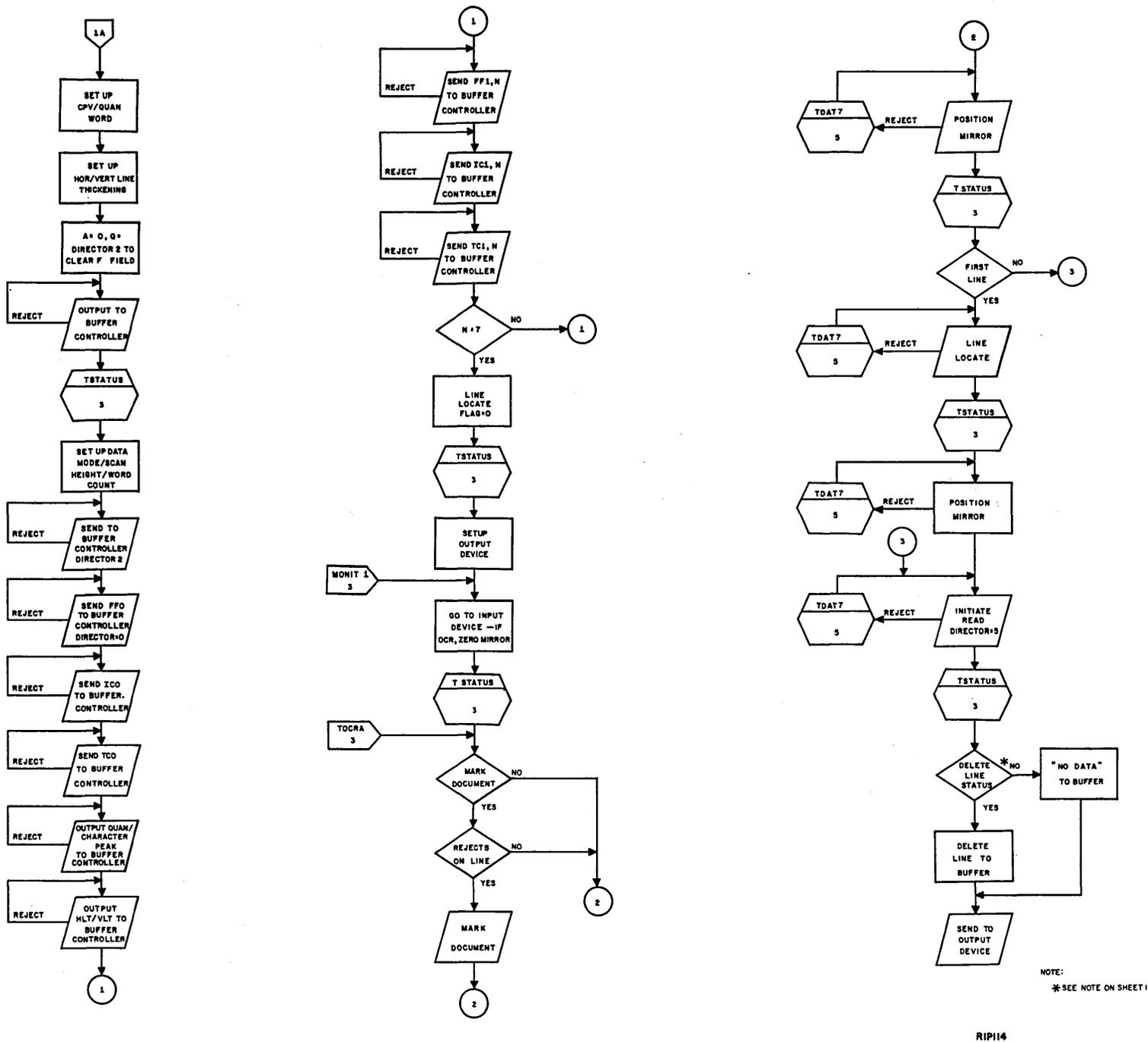
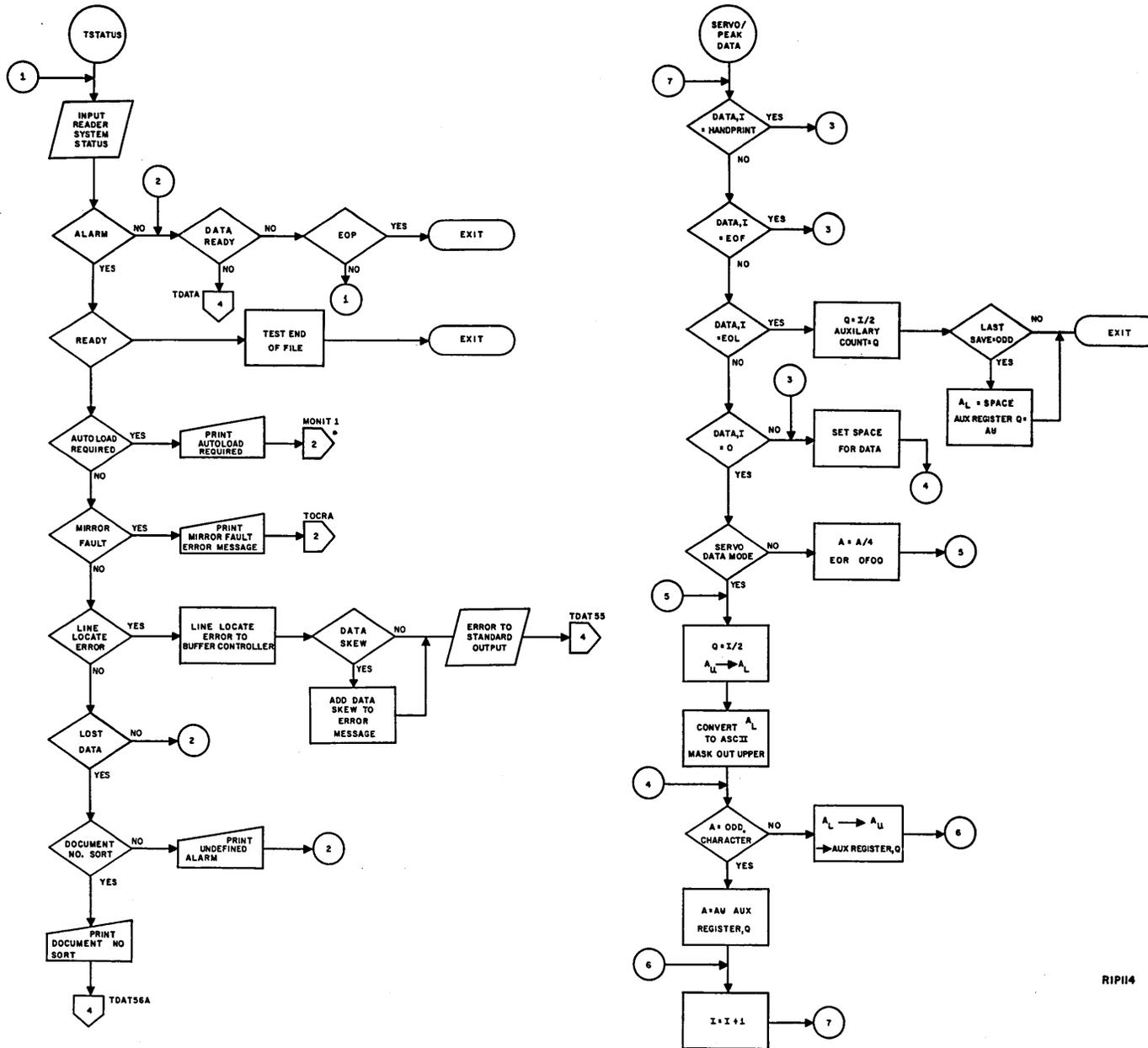


Figure 3. Flow Chart of RX-1 System Test (Sheet 2 of 5)



RIPII4

Figure 3. Flow Chart of RX-1 System Test (Sheet 3 of 5)

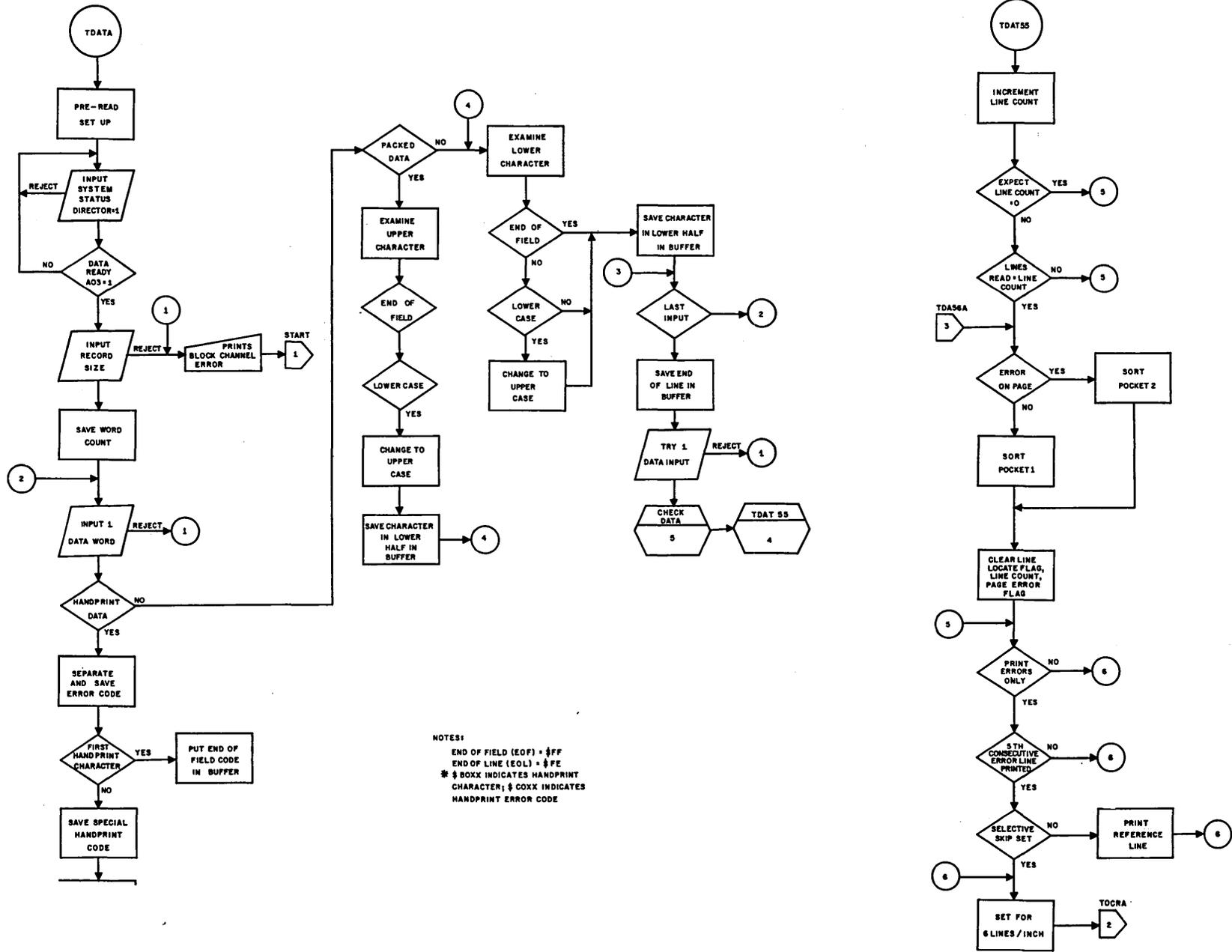


Figure 3. Flow Chart of RX-1 System Test (Sheet 4 of 5)

SC/1700/955 MODULE TEST
(LDRA32 Loader and RX3A33 Test No. 33)

I. OPERATING PROCEDURE*

A. RESTRICTIONS

1. Requires an 8K 1700 with a 609 or 608 MT and a teletype.
2. The diagnostic interfaces to SMM17 only for loading.
3. Test parameters are accepted only from teletype.
4. Manual parameters must be terminated with the BC equipment code.
5. Entries performed after a parameter request must be terminated with a CR.
6. Module tests may not be run in an off line mode unless the system includes a maintenance console.

B. LOADING PROCEDURE

The standard SMM17 calls as test number 32. See Appendix A for loading procedure. Following the initial test typeout [BEGIN RX -3 1700/FR101/955 MODULE TESTS (IA=XXX)] the program will request module selection by typing:

SMX=Y

The operator should now define the BC equipment code (X) before selecting the desired module (Y).

- Module Number 1 = Electronic Read and Verify Test
- Module Number 2 = Page and Document Handling Test
- Module Number 3 = Operator Panel Test
- Module Number 4 = Mirror Test
- Module Number 5 = Handprint Electronic Read and Verify

NOTE

Modules 1-4 are on auxiliary 1 tape and module 4 is
on auxiliary 2 tape.

After module selection the program will request the BC interrupt line by typing:

BIX=Y

Where X = the buffer controller equipment number and Y = its interrupt line.

*A more detailed procedure can be found in the CJ122 Maintenance Manual Volume, 48430080.

C. AUTOLOADING MODULE PROCEDURE

1. Select Automatic Parameter (AP)

Upon selection, the program will set up the Standard I/O Equipment Table (see Table 1)** and the Automatic Parameter Table to run the selected module. See Table 2 for Electronic Read and Verify and Table 3 for Page and Document Handling Automatic Parameters.

The Standard I/O Equipment Table and the Automatic Parameter Table assigned to the selected module may be changed at any time by using the Manual Interrupt button on the teletype. The program upon sensing the Manual Interrupt button depressed will complete the function currently in progress and return program control to the monitor. The monitor will type:

ENTER PARAMETER

The operator should now define a parameter.

See Table 4 for Common Manual Parameters

See Table 5 for Electronic Read and Verify

See Table 6 for Page and Document Handling

See Table 7 for Mirror Test

NOTE

If the mag. tape driver is a 659, select TD parameter. (See Appendix B Section 28.)

2. Select autoloader parameter (AL*). See Appendix B.

D. MODULE 1 OPERATING PROCEDURE

1. Electronic Read and Verify***

If using the automatic parameters:

a. Define font (DF*). See Table 9.

b. Define data, subset, or font (DD*, SS*, LF*). See Appendix B, Section B.

c. Execute test (EX*).

*Buffer controller equipment code.

**Tables begin at the end of this test.

***For sync purpose, use general sync 1 or read.

If not using the automatic parameters (see Appendix B, Section B):

- a. Define image position and read mode (IP*)
 - b. Define read parameters (RP*)
 - c. Define repetitions (RE*)
 - d. Define output device (OT*, OP*, OM*)
 - e. Define font (DF*)
 - f. Define data (DD*, SS*, LF*)
 - g. Execute test (EX*)
2. Recirculate Image Test (RI)***
- a. Define image to be recirculated.
3. Load and Shift Register Test (SR)**
- a. Select data pattern no. (see Table 11).
 - b. Set 955 DUMP switch to INPUT.
 - c. Press 955 READY switch.

The Load Register Test is now in progress. To terminate the Load Register Test and begin the Shift Register Test do the following:

- a. Press 955 STOP switch.
- b. Set 955 DUMP switch to OUTPUT.
- c. Press 955 READY switch.

To terminate the S/R test press STOP switch.

4. Quick Look Test (QL*)

a. Purpose

To obtain a quick summary of the 955 electronic reading capabilities on standard and optional fonts.

b. Restrictions

Repetition parameter may not be zero since zero repetitions means to read the selected font indefinite.

*Buffer controller equipment code.

**For sync purpose use general sync 2 or read.

***For sync purpose use general sync 2.

- c. Operating Procedure
 - 1) Define repetitions (RE*).
 - 2) If optional fonts are going to be tested and this is the first time, define font enable lines (RP*).
 - 3) Select quick look parameter. (QL*). See quick look specifications in Appendix B under Electronic Read and Verify Manual Parameters.
- 5. OLCC (On Line Character Correction) Test (LC*)
 - a. Purpose

To align and troubleshoot the OLCC device.
 - b. Operating Procedure
 - 1) Autoload Module 1 (AL*).
 - 2) Select LC* parameter.

In response to "LC*=" enter (CR) or A (CR). (CR) leaves all parameters unchanged and begins the test. A (CR) sets up the following automatic parameters and begins the test.
 - c. OLCC Automatic Parameters
 - 1) Font = ANSI medium
 - 2) Character images A through E
 - 3) Image position = bottom
 - 4) Character pitch = 7 clear columns
 - 5) Dino time = 2 seconds (see Appendix B, Section B-11) (DT*)
 - 6) Column count = 35 (see Appendix B, Section B-12) (CC*)

NOTE

Change any of the automatic parameters specified above at any time.

EXAMPLE 1: Character images changed from A-E to F-J.

- a. MI (Manual Interrupt)
- b. Select SS* parameter and define F-J subset
- c. Enter LC* (CR)

*Buffer controller equipment code.

EXAMPLE 2: The Dino time changed to 5 seconds.

- a. MI (Manual Interrupt)
- b. DT* = 5000 (CR)
- c. LC* (CR)

NOTE

Change all the parameters back to automatic at any time as follows:

- a. MI (Manual Interrupt)
 - b. LC * A (CR)
- d. Theory of Operation.

The RX3 module 1 upon receiving the command to start the test, begins to load the images (one column at a time) to the Shift register. When the program detects that the column just loaded to the Shift register is equivalent to the column count (CC*) parameter, it sets the Dino signal and continues to output the remaining character images. After the last column of data has been outputted the program checks the Dino time (DT*) parameter. If it is set to zero, the program will leave the Dino signal set and goes into an idle loop where it awaits new instructions from the operator. If the Dino time is set to non zero, the program will leave the Dino signal up for the duration of the Dino time parameter before dropping the Dino signal and repeating the test.

6. Servo Data Test

a. Purpose

The purpose of the Servo Data Test is:

- 1) Verify the accuracy of the Servo Data Count in determining the accurate position of an image within the Shift register.
- 2) Check Topless logic.
- 3) Check Top Scrub logic.
- 4) Check Bottomless logic.

*Buffer controller equipment code.

b. Operating Procedure

- 1) Autoload module 1 to BC (AL*).
- 2) Define Servo Data Test font (DF*=SDTST).
- 3) Define repetitions (RE*=100).
- 4) Execute Test. (EX*).

c. Theory of Operation

The RX3/Module 1 upon receiving the command to begin the Servo Data Test, will read the Servo Data Image Font, which consists of 39 character images. After the 39 images have been read, the RX3/Module 1 transfers to the RX3/1700 monitor the Character Voltage, Character Data, and Servo Data. The RX3/1700 monitor performs the Topless check, the Top Scrub check, Servo Data check, and Bottomless check. Any failure will now be reported with an appropriate message. The Servo Data Test will be performed 100 times. Upon completion the RX3/1700 monitor will display the End of Test message.

E. MODULE 2 OPERATING PROCEDURE

1. Light Sensor Test

- a. Select subtest number 1 (ST*)
- b. Define repetition (RE*)
- c. Execute test (EX*)

2. Dark Sensor Test (Sort of Pocket 1)

- a. Select subtest number 2 (ST*)
- b. Define repetitions (RE*)
- c. Execute test (EX*)
- d. Put one document on the feed-up table
- e. Press 955 READY switch
- f. Wait for STOP indicator to set
- g. Repeat from step d

*Buffer controller equipment code.

3. Dark Sensor Test (Sort of Pocket 2)
 - a. Select subtest number 3 (ST*)
 - b. Define repetition (RE*)
 - c. Execute test (EX*)
 - d. Put one document on the feed-up table
 - e. Press 955 READY switch
 - f. Wait for STOP indicator to set
 - g. Repeat from step d
4. Transport Speed Test (Check points RZ and SST1)
 - a. Select subtest number 4 (ST*)
 - b. Define repetitions (RE*)
 - c. Define feed parameters (FP*)
 - d. Execute test (EX*)
 - e. Put one document on the feed-up table
 - f. Press 955 READY switch
5. Transport Speed Test (Check points RZ and SST2)
 - a. Select subtest number 5 (ST*)
 - b. Define repetitions (RE*)
 - c. Define feed parameters (FP*)
 - d. Execute test (EX*)
 - e. Put one document on the feed-up table
 - f. Press 955 READY switch
6. Transport Slippage Test (Not Available)

*Buffer controller equipment code.

7. 955 Feed and Sort Exerciser
 - a. Select Subtest number 7 (ST*)
 - b. Define feed parameters (FP*)
 - c. Define sort parameters (SP*)
 - d. Execute test (EX*)
 - e. Place documents in the hopper
 - f. Press 955 READY switch

F. MODULE 3 OPERATING PROCEDURE

- a. Execute Test (EX*)

The Indicator Test is now in progress. The operator should now observe the indicators flashing sequence. The flashing sequence is Top to Bottom, Left to Right.

To terminate the indicator test and begin the 955 Switch Test, perform step b.

- b. Press the EOF (End of File) Switch

All the indicators should now be on and they should remain on for as long as the EOF switch is depressed. Upon release of the EOF switch, all the indicators should clear and the Switch Test begins.

The module will now begin to flash one of the switches to be tested. The operator should now press that switch. The indicator corresponding to the switch which is being tested, will continue to flash if the module does not detect the switch depressed. If the module detects the switch depressed, it will light the indicator and leave it on for as long as the operator holds the switch down. Upon release of the switch under test, the module begins to flash the next switch to be tested. Upon completion of the Switch Test the module repeats the test all over again.

*Buffer controller equipment code.

G. MODULE 4 OPERATING PROCEDURE

1. Define mirror coordinates (MC*).

The operator should define only the Forward coordinate if the mirror must be reversed with a Zero Mirror command. This is accomplished by entering a (CR) when the RX3/1700 monitor requests the REVMC.

2. Execute test (EX*).
3. Press 955 READY switch.

H. MODULE 5 OPERATING PROCEDURE

1. If using the automatic parameters:

- a. Define Handprint font (DF*) (see Table 13)
- b. Define Data, Subset or Load font (DD*, SS*, LF*)
- c. Execute test (EX*)

Automatic parameters for module 5 are as follows:

- a. On-Line Mode
- b. Standard Output Device (TTY)
- c. Normal Output Level
- d. Character Pitch = 3
- e. Test Is Set To Run Indefinite

2. If not using the automatic parameters:

- a. Select the output device (OT*, OP*, OM*)
- b. Define character pitch (RP*)
- c. Define repetitions (RE*)
- d. Define Handprint font (DF*) (see Table 13)
- e. Define Data, Subset or Load font (DD*, SS*, LF*)
- f. Define the output level (EO*, SO*)

*Buffer controller equipment code.

3. Quick Look Operating Procedure

- a. Define repetitions (RE*) number range 1-65000.
- b. Select Quick Look parameter (QL*). See Quick Look Specifications in Appendix B, under Electronic Read and Verify.

II. MESSAGES

A. NORMAL MESSAGES

1. BEGIN RX-3 1700/FR101/955 MODULE TESTS IA-600

Initial typeout. 600 is the initial address of the program.

2. ENTER PARAMETER

The RX-3 monitor has control and is awaiting an input from teletype.

3. THE BC IS LOADED

The selected module has been loaded to the FR101 and the checksums are correct.

4. END OF TEST

B. COMMON ERROR MESSAGES

1. ONA (Option Not Available)

2. MT DOES NOT RESPOND

The program received an external reject while trying to connect the MT. Verify MT equipment code and unit number.

3. MT STATUS ERROR

The program has detected a parity error.

4. ILLEGAL AUX. TAPE

5. BC/X FAILED TO REPLY ON FUNCTION RELOAD BC/X

The 1700 program is unable to communicate to BC/X. The program requests that BC/X be reloaded.

NOTE

Verify BC interrupt line.

*Buffer controller equipment code.

6. CHECKSUM ERROR

The checksum computed on the module while being loaded to the FR101 is not equal to the checksum computed during the transfer of the module from the FR101 to the 1700 program.

7. INCORRECT REPLY FROM BC/C RELOAD BC/X

The module residing in BC/X has lost control. It is not sending the correct reply to the 1700 program.

C. ELECTRONIC READ AND VERIFY ERROR MESSAGES

All error messages are prefaced by RX-3 MOD/Y/X; where X is the BC equipment code, and Y the module number.

1. NO DATA RDY RESP. ON X

The image of the character X was not responded by the 955 DATA READY switch in the time in which the image was centered in the matrix. (Make sure that the switch on the 955 is SIMULATED DATA and not on OPTICAL DATA.)

2. CONTINUOUS DATA READY X

The image of the character X generated more than one data ready. (The operator should now suppress character data ready (SD) in order to be able to continue with the test and determine cause of data ready failure.)

3. CHARS-READY = XXXXXXXXX ERR = YYYYYYYY REJ = ZZZZZZZZ

REF. LINE=
ERR. LINE=
VOLT. LINE=

The above printout occurs whenever images are misread or rejected. (X) is the total number of images read including those which are either misread or rejected. (Y) is the total number of images misread. (Z) is the total number of images rejected.

The characters contained in the error line corresponding to the reference line represent the images which were either rejected or misread. Those which were rejected are indicated with a character typeout. A question mark (?) in the error line may indicate that the 955 generated an illegal character code (not an ANSCI code) on the image indicated by the character in the reference line.

4. L/R FAILED

EXP PATRN=XXXXXXXXXXXXXXXX*XXXXXXXXXXXXXXXX*Y
XXXXXXXXXXXXXXXX*XXXXXXXXXXXXXXXX*Y

The pattern as indicated above is divided into four groups of 14 bits (X).
Each group is separated by (*Y) where Y is the control code.

5. S/R FAILED

EXP PATRN=XXXXXXXXXXXXXXXX*XXXXXXXXXXXXXXXX*Y
XXXXXXXXXXXXXXXX*XXXXXXXXXXXXXXXX*Y

REC PATRN=(SAME AS ABOVE)

6. COLUMN READY FAILED

The Column Ready signal from the reader to the BC is not changing state.
It is constant zero.

7. TOPLESS, NO REJECT

The reader has not generated a Reject on a Topless condition.

8. REJECT, NO TOPLESS

The reader has not generated Topless condition status.

9. NO TOPLESS, NO REJECT

The reader has neither generated a Topless condition nor a Reject.

10. TOP SCRUB LOGIC FAILED

The reader failed to scrub the black data from the Top Scrub image and
in consequence, the image was not read as a space.

11. BOTTOMLESS, NO REJECT

The reader has not generated the reject on a Bottomless condition.

12. REJECT, NO BOTTOMLESS

The reader has not generated Bottomless Status condition.

13. NO BOTTOMLESS, NO REJECT

Neither Reject nor Bottomless Status was generated.

14. SERVO DATA = 50000000011111111122222222223333333
EXPECTED = 723456789012345678901234567890123456

SERVO DATA =
RECEIVED =

The servo data received is not equal to the Servo Data expected.

D. PAGE AND DOCUMENT HANDLING TEST ERROR MESSAGES

All error messages are prefaced by RX-3, MOD/X/Y/Z where (X) is the module test number, (Y) is the BC equipment code, and (Z) is the subtest number.

1. Subtest Number 1 Error Message

955 SENSOR STATUS XXXX EXP X REC Y

The underscored portion specifies the sensor being tested.

RZ = READ ZONE

SE = SORT ENTRY

DD = DOUBLE DETECTOR

SST1 = SORT STATION 1

SST2 = SORT STATION 2

SPF1 = SORT POCKET FULL 1

SPF2 = SORT POCKET FULL 2

2. Subtest Number 2 Error Messages

Subtest number 2 messages are the same as those in subtest number 1. Subtest number 2 however, feeds and sorts a document in the primary pocket checking Read Zone, Sort Entry, and Sort Station 1 for an uncovered to covered and uncovered condition.

3. Subtest Number 3 Error Messages

Subtest number 3 messages are the same as those used in subtest number 1. Subtest number 3 however, feeds and sorts a document in the secondary sort pocket checking Read Zone, Sort Entry, Sort Station 1, and Sort Station 2 for an uncovered to covered and uncovered condition.

4. Subtest 4 Error Messages

a. DOC. VEL. AT RZ EXP XX.XX REC XX.XX INCHES/SEC.

b. DOC. VEL. AT SST1 EXP 75.00 REC XX.XX INCHES/SEC.

5. Subtest 5 Error Messages
 - a. DOC. VEL. AT RZ. EXP XX.XX REC XX.XX INCHES/SEC
 - b. DOC. VEL. AT SST2 EXP 75.00 REC XX.XX INCHES/SEC
6. Subtest 6 Error Messages
 - a. FWD SLIPPAGE XX CONVEYOR COUNTS
 - b. REV SLIPPAGE XX CONVEYOR COUNTS
 - c. TRANS-MOTION = FSTOP = XX FPNZV=XX FDWELL=XX
RSTOP = XX RPNZV=XX RDWELL=XX

FSTOP (forward stop) is the transport coordinate or conveyor counts recorded from the time read zone sensor was covered by a document. The transport speed was changed to 5 IPS and allowed to drop to 5 IPS and finally the forward motion was stopped.

FPNZV (forward page near zero velocity) is the difference between the FSTOP coordinate and FPNZV representing the number of conveyor counts elapsed since forward motion was stopped, until PNZV was sensed.

FDWELL (forward dwell) is the difference between FPNZV and FDWELL coordinates representing the number of conveyor counts in which the transport moved from the time PNZV was sensed until after a 5 second delay.

RSTOP (reverse stop) is the transport coordinate or conveyor counts in which the document was reversed before motion was stopped.

RPNZV (reverse page near zero velocity) is the difference between Stop and RPNZV coordinates representing the number of conveyor counts elapsed since reverse motion was stopped until PNZV was sensed.

RDWELL (reverse dwell) is the difference between RPNZV and RDWELL coordinates representing the numbers of conveyor counts in which the transport moved from the time RPNZV was sensed until after a 5 second delay.

The above message will be presented to the operator whenever the program detects document slippage and the difference between either FSTOP and FDWELL or RSTOP and RDWELL is less than or greater than 4.

Example: FSTOP=40 FPNZV=42 FDWELL=45 means that 40 conveyor counts after read zone was seen covered forward motion was stopped. Two counts later PNZV was sensed, and during the 5 seconds dwell time the transport moved three more counts forward.

7. Procedure To Recover From System Shutdown (Subtest 7)

a. Hopper Empty

- 1) Press the EOF (end of file) switch.

The END OF TEST message will now be displayed on the output device. The system will now be idling until a new EX command is performed. The throughput rate may now be requested by using the (ET) manual parameter.

b. Transport Check Or Misfeed

- 1) Remove document which caused the jam.
- 2) Remove documents from feed-up table.
- 3) Press READY switch.
- 4) Wait for STOP indicator to light.
- 5) Replace documents in the feed-up table.
- 6) Press READY switch.

c. Sort Check

- 1) Remove all documents from sort area.
- 2) Press READY switch.

d. Sort Pocket Full

- 1) Empty sort pockets.
- 2) Press READY switch.

e. Doubles

- 1) Remove double documents.
- 2) Remove documents from feed-up table.
- 3) Press READY switch.
- 4) Wait for STOP indicator to light.
- 5) Replace documents on the feed-up table.
- 6) Press STOP switch and READY switch.

E. MODULE 3 ERROR MESSAGES

Module 3 being strictly an off-line test does not have error messages.

F. MODULE 4 ERROR MESSAGES

1. MNZV NOT GENERATED WITHIN 10 MSEC FOLLOWING STOP COMMAND.
2. MIRROR COUNT OR VELOCITY FAULT XXXX (XXXX=STATUS)
1000= mirror velocity fault and 0020= mirror count fault.
3. ENCODER COUNT EXP 00 REC XX
The Encoder was expected to be zero when the mirror was out of Scan Gate. XX is the actual status.
4. FWD MIRROR COUNT FAULT
Mirror count fault detected after the mirror reached the forward coordinate.
5. FWD COORD ACT=XXXX MNZV=YYYY DWELL=ZZZZ
The mirror moved more than three coordinates from the time Scan Forward command was dropped until after the Dwell time.
6. SCAN FWD MIRROR SPEED * EXP 75.00 REC XX.XX INCHES/SEC.
7. REV. MIRROR COUNT FAULT
Mirror count fault detected after the mirror reached the reverse coordinate.
8. REV. COORD MDPNT=WWWW ACT=XXXX MNZV=YYYY DWELL=ZZZZ
The mirror moved more than three coordinates following Stop command.
9. REV. PULSES REC. IN FWD. MOTION X-Y
Encoder generated reverse pulses while the mirror was scanning forward. X is the ENCODER status before reverse pulses were detected and Y after.
10. ENCODER COUNT OUT OF SEQUENCE (FWD) X-Y
Encoder count incremented by more than 1. X is the encoder status before it went out of sequence and Y after.
11. FWD. PULSES REC. IN REV. MOTION X-Y
Encoder generated forward pulses while the mirror was in a reverse motion. X is the encoder status before the forward pulses occurred and Y after.
12. ENCODER COUNT OUT OF SEQUENCE (REV) X-T
Encoder count decremented by more than 2. X is the encoder status before it went out of sequence and Y after.

G. MODULE 5 ERROR MESSAGES

1. NO DATA RESP. ON X

The image indicated by X was not responded by the 955 data ready within the time in which the image was centered in the matrix*.

2. CONTINUOUS DATA READY X

The image indicated by the character X generated more than one data ready. To restart and determine data ready failure, suppress data ready (SD*).

3. RX3/MOD/5/X: HANDPRINT REV. X. Y

CHARS READ=XXXXXXXXX ERR=XXXXXXXXX SUB=XXXXXXXXX REJ=XXXXXXXXX

REF. LINE=

NUMERIC=

ALPHA=

SYMBOL=

The above printout occurs whenever an error, substitution, or reject is detected. Use manual parameter (SO*) to suppress printout.

4. COLUMN READY FAILED

The column ready signal from the reader to the BC is not changing state. It is either a constant 1 or a constant 0.

III. OFF LINE MODE OPERATING PROCEDURE

A. ELECTRONIC READ AND VERIFY ERROR HALTS

If the SELECTIVE STOP switch on the maintenance console is set, the module will come to a halt under six conditions. This is determined by examining the contents of the A register on the maintenance console.

1. End of Test A Register = 0000

The module has read the selected set of images the requested number of times. To repeat the test the operator should now enter in A register the number of repetitions (zero for indefinite) and press the GO button.

*Verify SIM/OPT switch on the 955 back panel, it should be on SIM.

2. Continuous Data Ready A Register = XX40

The 955 is generated more than one character data ready for every image being read. XX is the number of character data ready generated. To continue enter in the A register 0001 to suppress character data ready and 0000 to enable character data ready. Press the GO button.

3. No Data Ready Response A Register = 00XX

The 955 has failed to give out the ASCII code on the image indicated by XX ASCII code. To restart the module press GO.

4. Character Image Rejected A Register = XX40

The image indicated by XX ASCII code was rejected by the 955. To continue press GO.

5. Character Image Misread A Register = XXYY

The 955 misread the image indicated by ASCII code. YY is the ASCII code given out by the 955.

6. Load Register Test Failed A Register = 00C0

The Load register failed to give out the same pattern. To verify the expected pattern press the GO button four times. Press the Go button four more times to verify the pattern received. To repeat the test press go.

7. Shift Register Test Failed A Register = 01C0

The pattern changed while going through the Shift register. Press the GO button four times to verify the expected pattern. Press four more times to verify the pattern received.

B. PAGE AND DOCUMENT HANDLING TEST ERROR HALTS

***** NOT DEFINED *****

C. OPERATOR PANEL TEST ERROR HALTS

***** NONE *****

D. MIRROR TEST ERROR HALTS

If the SELECTIVE STOP switch on the maintenance console is not set, the program will bypass all mirror failures which might occur. If the switch is set, the program upon detecting a mirror fault will come to a halt displaying in the A register the error halt number. Additional information on some of the error halts are obtained by pressing the GO button and observing the contents of A.

1. ERROR HALT NUMBER 0 = SCAN FORWARD SPEED FAULT

The mirror speed was not 75 inches per second as expected. Press the GO button A=expected msec count. Press it again A=actual msec count in which the Scan Forward command was up.

2. ERROR HALT NUMBER 1 = MNZV FAILED

Mirror near zero velocity was not generated within 10 msec following Stop Mirror command.

3. ERROR HALT NUMBER 2 = MIRROR COUNT OR VELOCITY FAULT

Mirror status error. Press GO; A= mirror status, 1000=mirror velocity fault, 0020=mirror count fault.

4. ERROR HALT NUMBER 3 = MIRROR ENCODER FAILED

Press GO. A will contain the ENCODER status.

If A=000X The ENCODER count was not zero as expected when mirror was out of Scan Gate. X=Encoder Count.

If A=01XV Reverse pulses were received in forward motion. X=Encoder count status before reverse pulses occurred and Y after.

If A=02XY Encoder count out of sequence (FWD). The encoder incremented by more than 1. X=Encoder count status before it went out of sequence and Y after.

If A=03XY Forward pulses were received in reverse motion. X=Encoder count before forward pulses were detected, and Y after.

If A=04XY Encoder decremented by more than 1. X=Encoder status before it went out of sequence and Y after.

5. ERROR HALT NUMBER 4 = FWD MIRROR COUNT FAULT

Mirror count fault detected after the mirror reached the forward coordinate.

6. ERROR HALT NUMBER 5 = FWD COORDINATE FAULT

The mirror moved more than three coordinates from the Time Scan Forward command was dropped until after the dwell time.

Go A = Forward Coordinate

Go A = MNZV Coordinate

Go A = Dwell Coordinate

7. ERROR HALT NUMBER 6 = REV MIRROR COUNT FAULT

Mirror count fault detected after the mirror reached the reverse coordinate.

8. ERROR HALT NUMBER 7 = REVERSE COORDINATE FAULT

The mirror went behind the reverse coordinate by more than three coordinates following Stop command.

Go A = Midpoint Coordinate

Go A = Reverse Coordinate

Go A = MNZV Coordinate

Go A = Dwell Coordinate

E. HANDPRINT ELECTRONIC READ AND VERIFY ERROR HALTS

All error halts will be bypassed if the SELECTIVE STOP switch on the maintenance console is not set.

1. NO DATA READY RESPONSE A = 00XX

Where XX is the ASCII code corresponding to the image which failed to generate Data Ready. To suppress data ready clear A register. Press GO button.

2. CONTINUOUS DATA READY A = 0140

To suppress Data Ready, clear A register. Press GO button.

3. ERROR, SUBSTITUTION OR REJECT DETECTED

A register = 00XX (Expected ASCII code) Press GO

= 00XX (NUMERIC code) Press GO

= 00XX (ALPHA code) Press GO

= 00XX (SYMBOL code) Press GO

TABLE 1. STANDARD I/O EQUIPMENT TABLE

Equipment*	*	MTI 7	*	MTO 7	*	TTY -	*	LP F
Interrupt	*	3	*	3	*	2	*	5
Mode	*	B	*	B	*	A	*	A
Format	*	466	*	466	*	8	*	16
Converter	*	0		0	*	0	*	0
Unit Number	*	1		2	*	-	*	-
Drum	*	-		-	*	-	*	*

Common Automatic Parameters

Output Device = TTY

Output = Normal

Repetitions = Zero or Indefinite

TABLE 2. ELECTRONIC READ AND VERIFY AUTOMATIC PARAMETERS

Character Pitch = 7

Read Mode = Normal

Character Peak = 12

Font Enable = ANSI

Character Data Ready Enabled

Image Position = TOP

TABLE 3. PAGE AND DOCUMENT HANDLING AUTOMATIC PARAMETERS

Document Length = 13 Inches
Transport Speed = 20 Inches/Sec.
Sort Sequence = Primary - Secondary
Subtest = 7

TABLE 4. COMMON MANUAL PARAMETERS

AL* = Autoload Module to FR101
AP* = Automatic Parameters
BD* = Buffer Controller Dump
BE* = Buffer Controller Equipment
BI* = Buffer Controller Interrupt
DR* = Data Receive From Controller
DS* = Data Send to Controller
EC* = Enable Controller Communication (On Line Mode)
EO* = Enable Controller Output
EX* = Execute Module
ME* = Mag Tape Equipment
MI* = Mag Tape Interrupt
OM* = Output to Mag Tape
OP* = Output to Printer
OT* = Output to Teletype
PC* = Punch From Core
PD* = Printer Drum
PE* = Printer Equipment
PI* = Printer Interrupt
RE* = Repetitions
SC* = Suppress Controller Communication
SM* = Select Module
SO* = Suppress Controller Output
TC* = Mag Tape Converter
TM* = Terminate Module
TN* = Mag Tape Unit Number
XT* = Exit From Test to SMM17
TD* = Tape Driver Select

*Buffer controller equipment code.

TABLE 5. ELECTRONIC READ AND VERIFY MANUAL PARAMETERS

DD* = Define Data
DF* = Define Font
ED* = Enable Character Data Ready
ET* = Error Totals
IP* = Image Position And Read Mode
LF* = Load Font
QL* = Quick Look Test
RI* = Recirculate Image
RP* = Read Parameters
SD* = Suppress Character Data Ready
SR* = Shift Register Test
SS* = Select Subset

TABLE 6. PAGE AND DOCUMENT HANDLING MANUAL PARAMETERS

ET* = Error Totals
FP* = Feed Parameters
SP* = Sort Parameters
ST* = Subtest

TABLE 7. MIRROR TEST MANUAL PARAMETERS

MC* = Mirror Coordinates

*Buffer controller equipment code.

TABLE 9. IMAGE FONT SELECTION

Type the full name of the font desired.

ANSI Thin	7B Thin
ANSI Medium	7B Medium
ANSI Thick	7B Thick
RABINOW Thin	12F Thin
RABINOW Medium	12F Medium
RABINOW Thick	12F Thick
1428 Thin	NOF Thin
1428 Medium	NOF Medium
1428 Thick	NOF Thick
1403 Thin	OCR-B71 Thin
1403 Medium	OCR-B71 Medium
1403 Thick	OCR-B71 Thick
E13-B Thin	Lower Case Medium
E13-B Medium	
E13-B Thick	SDTST (Servo Data Test)

TABLE 12. 955 TRANSPORT MODULE SUBTESTS

1. Light Sensor Status Test
2. Dark Sensor Status Test (Sort Station 1)
3. Dark Sensor Status Test (Sort Station 2)
4. Transport Speed Test (Sort Station 1)
5. Transport Speed Test (Sort Station 2)
6. Document Slippage Test
7. Feed - Sort Throughput Rate

TABLE 13. HANDPRINT IMAGES FONT LIBRARY LIST

Font Name	Contents
ENCODER (complete HP set)	0123456789@ CSTXZ@ +- +HEL@
HP0 (0 char. set)	0000
HP1 (1 char. set)	1111111111
HP2 (2 char. set)	22222
HP3 (3 char. set)	3333333333333333333333
HP4 (4 char. set)	444444
HP5 (5 char. set)	55555555
HP6 (6 char. set)	66666666666666
HP7 (7 char. set)	7777777777
HP8 (8 char. set)	888888888888888888
HP9 (9 char. set)	99999999999999
HPC (C char. set)	CCCC
HPS (S char. set)	SSS
HPT (T char. set)	TTTTTTTTTT
HPX (X char. set)	XXXXXXXXXXXXXX
HPZ (Z char. set)	ZZZZZ
HP+ (+ char. set)	+++++
HP- (- char. set)	-
HP= (= char. set)	==
HPM (char. set)	(field mark)
N REJECTS	
A REJECTS	
S REJECTS	
HPE1	
HPE7	
USA@	
GOTHIC	
BLACK GOODIES	
SUPER GOODIES	
FEATURES	
FLATS/SLOPES	
SPLITS/JOINS	

NOTE

1. When selecting font, spell full name as it appears in the font list.
2. Except for the ENCODER, font selection of a specific character image or subset is illegal. Use (LF*) manual parameter.

APPENDIX A

A. Manually load the following bootstrap.

1FC0 = 681B	1FCD = 02FE
1FC1 = E000	1FCE = 0FCC
1FC2 = 0382	1FCF = 7C0C
1FC3 = C000	1FD0 = 02FE
1FC4 = 0404	1FD1 = 0FC6
1FC5 = 03FE	1FD2 = BC09
1FC6 = 09FB	1FD3 = 7C08
1FC7 = 0DFE	1FD4 = 02FE
1FC8 = 03FE	1FD5 = BC06
1FC9 = 0F42	1FD6 = 6C05
1FCA = 03FE	1FD7 = D804
1FCB = 0DFE	1FD8 = 0101
1FCC = 0A00	1FD9 = 18F2

B. Set SELECTIVE STOP and SELECTIVE SKIP switches.

C. Set P = 1FC0

D. Run and set up stopping.

First Stop: Q = 0205 and Run

Second Stop: A = 08B0 Q = 0381 Run

The TTY will reply by typing:

SMM17 ED. 2.3

BUILD TEST LIST

Third Stop: A = 3201 Q = 0381. Run.

Fourth Stop: Clear A register and SELECTION SKIP switch. Run.

APPENDIX B

A. COMMON MANUAL PARAMETERS SPECIFICATIONS

1. AL* = Select autoload mode (H=Hardware, S=Software)
2. AP*
3. BD*
4. BE* = Change BC equipment code (1-F)
5. BI* = Define BC interrupt line (1-F)
6. DR* = The monitor will type:
FWA = (Define FR101 dump starting address)
The monitor will type:
LWA = (Define FR101 dump terminating address)
7. DS* = The monitor will type:
ADR = (Define core location to be changed)
The monitor will type:
XXXX = (Define FR101 change)
Terminate change with a comma (,) for sequential store and with
a period (.) for single store.
To terminate update type STOP.
8. EC*
9. EO*
10. EX*
11. ME* = Select MT equipment code (1-F)
12. MI* = Select MT interrupt line (1-F)
13. OM* = Define file number (1-F)
14. OP*
15. OT*
16. PC*
17. PD* = Select printer drum (O=OCR, S=Standard)
18. PE* = Select printer equipment code (1-F)
19. PI* = Select printer interrupt line (1-F)

*Buffer controller equipment code.

- 20. RE* = Define repetition (0-65, 500)
- 21. SC*
Upon selection the program changes from On-Line Mode to Off-Line Mode and the test is restarted.
- 22. SM* = The operator should now select a module (1-5)
- 23. SO*
Upon selection the program changes the output level to suppress and the test is restarted. No error messages will now be displayed.
- 24. TC* = Select MT converter code (O-F)
- 25. TM* = (Not Defined)
- 26. TN* = Select MT unit number (0-7)
- 27. XT* = Call SMM17 loader

NOTE

SELECTIVE SKIP and SELECTIVE STOP switches must be set prior to selecting this parameter.

- 28. TD* = Select tape driver (608, 609, or 659)
If a 659 is selected, the program will request the equipment code for the 3518 by typing:
3518 # =

NOTE

3518 equipment code is set to 1 if not selected.

B. ELECTRONIC READ AND VERIFY MANUAL PARAMETERS

- 1. DD* =

The operator may now enter as many as 60 characters to determine the set and sequence of the previous Py is rested by the program for validity and if valid the program will respond with a comma (,) typeout. If the entry is illegal (does not belong to the selected font), the program ignores it and the operator may continue.

If a valid entry is made, which the operator wishes to change, he should now enter a RB (Rubout) followed by the change.

Data definition is terminated with a (CR).

*Buffer controller equipment code.

2. DF* =

For standard and optional fonts refer to Table 9 for font selection.

If the font which is to be tested was generated with the 955 optical data, an * (asterisk) must precede the name.

3. ED*

This parameter instructs the RX3/module 1 to read normal without suppressing character data.

4. ET*

The following summary will be displayed on the output device.

CHARS - READ = XXXXXXXX ERR = YYYYYY REJ = ZZZZZZZZ
REF. LINE =
ERR. LINE =
VOLT. LINE =

5. IP*

The operator should now define where and how he wishes to read the images.

WHERE OPTIONS

- T (top) most significant 28 bits of the Load register
- C (center) middle 28 bits of the Load register
- B (bottom) least significant 28 bits of the Load register

HOW OPTIONS

- 0 (Normal) $\begin{array}{|c|} \hline \text{F} \\ \hline \end{array}$
- 1 (Upside Down) $\begin{array}{|c|} \hline \text{E} \\ \hline \end{array}$
- 2 (Shift Reverse Normal) $\begin{array}{|c|} \hline \text{7} \\ \hline \end{array}$
- 3 (Upside Down Shift Reverse) $\begin{array}{|c|} \hline \text{J} \\ \hline \end{array}$

Examples:

- a. Top + Normal = IP*T, 0 (CR) or (IP*T (CR)
- b. Center + Upside Down = IP*C, 1 (CR)
- c. Bottom + Shift Reverse Normal = IP*B, 2 (CR)

NOTE

- 1. These options are not available for handprint images or captured video data.
- 2. Following IP* define DD, SS, or LF.

*Buffer controller equipment code.

6. LF*

All the images contained in the defined font will now be transferred to the BC.

7. QL* =

For font name and sequence, see Table 9 for standard and optional fonts. See Table 13 for handprint. If the fonts desired to test are in sequence, enter:

```
QL*=FIRST - LAST (CR           WHERE
      FIRST = Initial font name and
      LAST  = Last font name to be tested
```

If the fonts are not in sequence, enter

```
QL*=FONT NAME,
```

The program will now perform an (LF) + (CR). Define the next font. Terminate with a (CR) last font name.

```
Example 1:  QL*=ANSI THIN - ANSI THICK (CR)
             QL*=ENCODER - BLACK GOODIES (CR)
```

```
Example 2:  QL*=ANSI THIN,
             1428 MEDIUM,
             E13-B THICK,
             7B THIN (CR)
```

8. RI* =

Define image to be recirculated.

9. RP*

The program will type:

```
CHAR - PITCH =      (Range 0-13)
```

Enter a (CR) if the pitch has already been defined, otherwise specify the number of clear columns to be inserted between the images as they are read.

The program will type:

```
FONT ENABLE =
```

If the font line for the font or fonts which are about to be tested have already been defined, enter (CR). Otherwise, enter font name (see Table 9) followed by an = (equal sign) and the font line number or numbers. Refer to the table below for font line number selection.

*Buffer controller equipment code.

NOTE

For handprint font name use *HP=

Example 1: Font line selection for one font

Font Enable = E13-B=X (CR)

Font Enable = ANSI = 0123456 (CR)

Example 2: Font line selection for multi fonts,

Font Enable = 1428=X, 1403=Y, RABINOW=Z(CR)

Example 3: Font line selection for fonts generated by RX4 Optical
Dump program

Font Enable = *NAME=X(CR)

After the font line selection the program will type

CHAR-PEAK = Enter a (CR) if character peak has already been defined.

FONT LINE SELECTION TABLE

Line Number	Font Enabled
0	USASI Mark Sense
1	USASI Numeric
2	USASI Control
3	USASI Alpha "5"
4	USASI Alpha "21"
5	USASI Punctuation 1
6	USASI Punctuation 2
7	Optical Scaling (Size C)
8	Alternate Font Line 1
9	Alternate Font Line 2
A	Alternate Font Line 3

10. SD*

Upon selection of this parameter the program instructs the RX3-module 1 to begin the electronic read test and suppress character data. In other words, the BC program will not verify the character data generated by the 955.

NOTE

It is illegal to request totals when the SD* parameter is selected. The BC program is not accumulating any totals in this mode.

*Buffer controller equipment code.

11. DT* OLCC DINO TIME (DEFINE TIME IN MILLISECONDS)

This parameter represents the duration of the Dino signal from the time the last column of data has been outputted. If the Dino Time is set to zero the Dino signal will get set at the requested column count, and it will remain set until interrupted.

12. CC* = COLUMN COUNT WHERE THE DINO SIGNAL MUST BE SET

The column count is computed as follows:

$I + P + I + P \dots\dots\dots$ WHERE

I = Image width (column count)

P = Character pitch (clear columns)

Example:

Character images = A through E

Character pitch = 7

Image width = 15

Dino signal on the first column of D.

$A + p + B + p + C + p + D1$ (D1 = First Column of D)

$15 + 7 + 15 + 7 + 15 + 7 + 1 = 67$ Answer

C. PAGE AND DOCUMENT HANDLING MANUAL PARAMETERS

1. ET*

The program upon selection of this parameter will display the following summary on the output device.

XXXXXX DOCUMENTS FEED IN XX MIN. YY SEC. XX DBLS XX JAMS

2. FP* The monitor will type

DL =

Define the document length in tenths of inches. After selection the program will request the transport speed by typing:

TS = (options 5, 10, 20, 40)

3. SP* = DEFINE SORT SEQUENCE (P=Primary, S=Secondary)

4. ST* = SELECT SUBTEST (See Table 12)

*Buffer controller equipment code.

D. MIRROR TEST MANUAL PARAMETERS

1. MC* The monitor will type:
FWDMC = (Define forward mirror coordinate)
The monitor will type:
REVMC = (Define reverse mirror coordinate)
The monitor will type:
DWELL TIME = (Define dwell time)

*Buffer controller equipment code.

SC 17/1700 - FR101 MEM/COMM/IFP TEST (BC2A56)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Requires an 8K 1700.
2. Requires a (TF201-A01) FR101 Maintenance Console.
3. The 1700 does not give error messages detected by the command and memory tests.
4. SMM17 is used for overlay loading.

B. LOADING PROCEDURE

1. Standard SMM call.
2. Test number 56.

C. PARAMETERS

1. Automatic (none)
2. Manual

- a. On receiving a "MANUAL INTERRUPT (MI)", control is transferred to the "ENTER PARAMETERS" routine (see flow chart fco). If initialization is complete (see I.C.3.), parameters can now be entered. An "ONA" response to an entry indicates that the option is not available. The following is a list of options.

<u>Code</u>	<u>Task</u>	<u>Reference</u>
AL = n	Autoload test n	II. B. 14
BD	Buffer controller dump	II. B. 15
BE	Select buffer equipment no.	II. B. 5
BI	Select buffer interrupt line	II. B. 6
DL	Delete autoloading	II. B. 10
EL	Enable autoloading	II. B. 11
EX = n	Execute test n with program loading	II. B. 12
OP	Select printer for error output	II. B. 1
OT	Select teletype for error output	II. B. 2
PD	Select printer drum type	II. B. 3
PE	Select printer equipment no.	II. B. 4
PL	Punch program boot loader	II. B. 13
PP	Punch program	II. B. 16
TB	Select upper and lower transfers	II. B. 9
TL	Select lower transfers	II. B. 9
TU	Select upper transfers	II. B. 9
XT	Exit from test to SMM17	II. A. 2

3. Forced (Automatic) Requests

- a. Should anything happen to prevent the normal flow of the program before a series of required entries are made, the program will re-start its list of automatic calls. The following is a list of those calls.

ENTER PARAMETERS

BE = Requesting buffer equipment no.

BI = Requesting buffer int. line.

4. Stop/Jump Parameter

- a. The parameter can be displayed in A for a change, just after an entry in the enter parameters routine if the SKIP and STOP switches are set. The used bits are:

Bit 8 = 1 = Suppress Error Message Output

D. OPERATING INSTRUCTIONS

1. Load BC2 via SMM17 operating instructions.
2. Respond with the correct entry on the teletype to the request (see I.C.3.).
3. After I.D.2 is complete, manual entries can now be made. If no other entries (other than to execute test) are made, the following is assumed in the program:
 - a. OT, PD = S, PE = F, EL, and TB.

II. MESSAGES

A. NORMAL MESSAGES

1. BEGIN BC2 FR101 TEST IA = XXXX

Initial typeout where XXXX = the initial address of the program. Rerun from P = IA.

2. END BC2 TEST

In response to code (XT), the test is terminated and control is returned to SMM17.

B. COMMAND MESSAGES

1. OP
Request error output to go to printer.
2. OT
Request error output to go to teletype.

3. PD = X
Request printer drum type where X = S = standard and = O = OCR.
4. PE = X
Request printer equipment where X = 0 → F.
5. BE = X*
Requesting buffer controller equipment number where X = 0 → F.
6. BI = X*
Requesting buffer controller interrupt line where X = 2 F.
7. ENTER PARAMETERS

In response to a manual interrupt or on an entry completion, entries may now be made via teletype (see I. C. 2).
8. PROGRAM X WAITING FOR PARAMETERS

In response to codes (EX or AL), this message denotes that text X has been loaded and is waiting for manual intervention at the Maintenance Console. Master clear the BC and run the test according to the procedures for that test. The tests are as follows:

<u>Test</u>	<u>Remarks</u>	<u>BC2 Listing Page</u>
1 = BCQ	Quick Look Program	50
2 = BCCOM	Buffer Controller COM Test	70
3 = MEM	2 1/2D Memory Test (750 nanoseconds)	178
4 = MM1	Memory Test (1.1 microseconds)	236
5 = MM2	Memory Test (1.1 microseconds)	265
6 = MY1	Memory Test	288
7 = MY2	Memory Test (200 nanoseconds)	316
8 = BCM (Y4)	Memory Test	341

9. TX

Where X = U for upper, = L for lower, and = B for both upper and lower. This command modifies the program boot loader, henceforth referred to as PBL, accept data on only that specified portion(s) of the block transfer channel as valid data. TU and TL will disable autoloading the PBL. If DL (see II. B. 10) has not been entered, a jump to the PBL will be autoloaded. If EL (see II. B. 11) is entered, the modified boot will be autoloaded. TB will re-enable PBL loading. See Figure 2 for combinations.

* These entries are force requested at initialization.

10. DL

This option will delete the autoloading of the PBL and a jump to it. It is assumed that a boot is in at \$F6F. The BC must be set to that address and run before execution takes place. (See EX at II. B. 12 and Figure 2.)

11. EL

This option enables autoloading of the PBL in its existing configuration. (Cancel DL option and TU/TL boot loading restrictions.) (See Figure 2.)

12. EX = x

This option begins the program controlled loading of text x and does an interface coupler check (Figures 1 and 2). It begins by autoloading the PBL if not restricted by TU, TL, or DL options. It next runs an interface check and finally loads the program (see fc1, 2, 3, and 4).

13. PL

If the 1700 has a paper tape punch, this option will generate a paper tape of the PBL in its current configuration. It should be loaded and run at P = 0000 on the Maintenance Console.

14. AL = x

Autoloads program x (Figure 2).

15. BD

FWA = XX0 LWA = YYF

This option will cause the 1700 to autoload a small boot into the first 15 locations and dump XX0 YYF to the selected error output device. If locations 000 00F are important, they should be written down before execution of this option begins. F is not actually printed but should be understood.

16. PP

Punches the last program executed onto paper tape in console loading format.

C. ERROR MESSAGES

1. ONA

Notes that the requested option is not available.

2. AUTOLOADING LOADER FAILED

Five attempts to load the FR101 Loader (or a jump to it) were made but an initial interrupt response from the loader was not received.

3. CH X FAILED SET = XXXX CLR = YYYY

Some of the channel bits have failed to be as expected, either solidly or intermittently. Those that failed to set are in (CLR = YYYY) and those that failed to clear are marked in (SET = XXXX). Possible channels are 0, 1, and B (for block transfer channel). The 1's in either word mark the bit in error.

4. FR101 PROGRAM LOADING FAILED

After a required amount of time without a data interrupt or five consecutive errors on the same transfer, program loading is aborted and the above message is output.

5. NO BC INT. X

In the required amount of time, an interrupt was not received during program loading.

X = 1 = No controlware alarm and end of operation.

= 2 = No data interrupt during interface check.

= 3 = No data interrupt during actual program load.

6. INTERNAL REJ. ON INPUT DIRECTOR = X

The computer internally rejected on an attempt to input using director X.

7. EXTERNAL REJ. ON INPUT DIRECTOR = X

The buffer controller rejected the 1700 on an attempt to input using director X.

8. INTERNAL REJ. ON OUTPUT DIRECTOR = X

The computer internally rejected on an attempt to output using director X.

9. EXTERNAL REJ. ON OUTPUT DIRECTOR = X

The buffer controller rejected the 1700 on an attempt to output director X.

10. COUPLER STATUS E= XXXX A= YYYY S= NN

While all directors were being exercised, the coupler status was collected by the buffer controller and later sent to the 1700 for analysis. The ones output were found to be in error. E = expected and A = actual (see Figure 1) NN = the status position in the table.

11. SMM OVERLAY LOADING FAILED

Self explanatory

III. DESCRIPTION

A. INITIALIZATION

1. Clear the buffer controller via the Maintenance Console.
2. Set the Maintenance Console STOP switch.

B. OPERATION

1. Purpose

- a. Check all directors.
- b. Check all data lines.
- c. Check all interrupts.
- d. Check coupler status.
- e. Check system status.
- f. Check the BC memory.
- g. Check the BC instructions.

2. Procedure

- a. See flow charts for execution flow.
- b. Load one of the tests via AL or EX options.
- c. When the test is loaded, examine all errors in the priority order given:
 - 1) Coupler status errors (Figure 1)
 - 2) System status (channel 0 errors)
 - 3) Interrupt errors
- d. From the Maintenance Console, run the test just loaded, according to the following procedures.

FR101 BC QUICK LOOK COMMAND AND MEMORY TEST

Operating Procedure

Restrictions

The SLS instruction must be operational to flag a UJR error and when the CE assembly option is selected.

The Jump instructions must be operational to flag most other instruction failures and when the HANG assembly option is selected.

The SCB instruction must be operational to flag errors when the BUZZ assembly option is in use.

At least one of the assembly options must be selected.

1. CE - Stop on an SLS instruction at the failing routine.
2. HANG - Hang on a Jump instruction at the failing address.
3. BUZZ - Alert buzzer upon errors and hang.

One direct cell must be available for testing purposes. (COMQL) is preset to a 2 for this. The original contents are reset at the end of a pass.

Channel instructions are not tested.

The loading address through the loading address +100 is not tested in the memory test.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console.

Type "AL = 1" for autoloading or,
"EX = 1" for controlled loading.

Using the Maintenance Console, clear and start the test at P = 0000.

Parameters

None - except for the assembly options: CE, HANG, BUZZ, COMQL, (LWATEST) = the last memory test address.

Messages

The failing address (observe P by use of the Maintenance Console) must be compared with a listing of BCQ to determine the failure.

(B1) = Failing memory address in memory test.

Significant Locations

Direct cell COMQL is preset to a 2 for direct testing.
(LWATEST) = FFF to test 4K.

Description

Command Test

Execute at least one of each format one instructions and check the results. Stop if any errors.

Execute at least one of each format two instructions and check the results. Stop if any errors.

Memory Test

Set the address into the first available location after BCQ.

Continue setting and checking each location with its address until the (LWATEST) is reached. (Preset to test 4K.)

On errors

- a. (B1) = Failing address.
- b. (B1) = Expected data.

End of Pass

Reset address COMQL to original data.

Exit to loading address +3 to restart test.

The test will keep looping if no error is encountered.

Comments

The UJR instruction is tested first and if a failure occurs, BCQ will stop on an SLS instruction and alert buzzer if selected.

All other Jump instructions are tested next and if a failure occurs, BCQ will stop on an SLS instruction (if CE enabled) or hang on a UJR 0 instruction (if HANG is enabled).

All other instructions follow in logical order.

(BCORST) approximately = 70 may be set to 0 for an end of pass SLS.

Timing

The test takes less than 1 second to run the command test.

The memory test takes less than 1 second to test 4K of memory.

One complete pass is equal to the command test time plus the memory test time.

BUFFER CONTROLLER COMMAND TEST (BCC)
(Formerly BCCOM)

Operating Procedure

Restrictions

The Input/Output tests will require a strap to shunt output channels to a corresponding input channel for test purposes.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console.

Type "AL = 2" or,
"EX = 2"

Master Clear and Channel Clear the Maintenance Console.

Run from location 0000.

Parameters

Five programmed stops occur in the I/O instructions test of Section 4. The action required for each of the stops is as follows:

Stop 1 - Set a not equal to zero to bypass the block transfer test.

Stop 2 - Set a not equal to zero to bypass the normal channel test.

Stop 3 - Set A to designate the initial hexadecimal numbers of the output channel-bit and the corresponding input channel-bit to be tested.

<u>Output</u>		<u>Input</u>	
CH	BIT	CH	BIT
A = XXXX	XXXX	XXXX	XXXX

Each channel and bit number is to be designated by one hexadecimal digit 0 through F.

Stop 4 - Set A to designate the number of successive channels (M) and bits (N) to be tested starting with the I/O channel-bit numbers specified in stop 3.

Channels (M)		Bits (N)	
A = XXXX	XXXX	XXXX	XXXX

The normal channel test will loop through the instruction test sequence N- times, one loop for each consecutive increment of both input and output bit numbers designated in stop 3. The input-output channel numbers do not change. Upon

completion of the bit incrementing loop both input and output channel numbers are incremented and the bit sequence test repeated. Upon completion of M times N loops through the normal channel test the program will exit to stop 5. If A is not changed during stop 4, the normal channel test makes one pass to test the I/O channel-bit combination specified in stop 3 and exits to stop 5.

At stop 4 the test operator can insert the hexadecimal digits 01, 02, . . . , 0E, 0F, through 10 to represent from 1 to 16 channels and from 1 to 16 associated bits to be tested.

Stop 5 - (A) is initially set at 1 by parameter flag RPTFLAG. Clear (A) to zero in order to exit from the normal channel test. Else, the program will return to stop 3 for repeating the normal channel test.

Error Stops and General Information

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working. No programmed stop will occur in test sections 1, 2, or 3 unless a failure is encountered.

The encounter of an error stop requires the test operator to review the series of assembled instructions (see listing) leading up to the SLS Stop instruction (error). In most cases the operator would only have to look at the instructions contained within one or two SLS instructions just prior to the error stop. The instruction under test would be similar to an elementary test sequence out of the overall command test and separated from other instructions under test by SLS stops. Error stops are designated by EEEEE in the rightmost portion of the assembly listing.

Instructions being tested are noted by ***** in the rightmost portion of the assembly listing comment field.

BC Core Locations of Interest (with Maintenance Console)

Specific Locations

Start of Program	Address - 0000
Restart	Address - 0F48
Stop 1 - Bypass Block Transfer Test	Address - 0E4D
Stop 2 - Bypass Normal Channel Test	Address - 0E52
Stop 3 - Normal Channel I/O Setup	Address - 0E56
Stop 4 - Normal Channel Counter	Address - 0E5B
Stop 5 - Repeat Normal Channel Test	Address - 0EFA

Section Description

Basic Command Test Sequence

This test is divided into four different sections based upon the number of storage reference cycles of the instruction. The sections are arranged in the following order:

Section 1 - One Storage Cycle

Direct Jumps

No Address

Condition Jumps

Relative Address Test

Condition Bit Test

Shift Test (see Table 1)

Scale Test (see Table 1)

Adder Test (see Table 2)

Select Bits in A

Enter Instructions

The following instructions are tested in this order:

Direct Jumps

UJD - Unconditional Jump

ZJD - Zero Jump

NJD - Non-Zero Jump

PJD - Positive Jump

MJD - Minus Jump

No Address

LDN - Load

ADN - Add

SBN - Subtract

LMN - Logical Minus

LPN - Logical Product

LCN - Load Complement

Condition Jumps

FJD - False Jump Direct

TJD - True Jump Direct
FJR - False Jump Relative
TJR - True Jump Relative

Relative Address Test

ADR - Add Relative
SBR - Subtract Relative
LCR - Load Complement Relative

Condition Bit Tests

TOV - True on Overflow
TOP - True on Odd Parity
TAB - True on Bit of A
INT - True on "OR" of Internal tests

Shift Test (Table 1)

SRC - Shift Right Circular
SLC - Shift Left Circular
SRO - Shift Right Open

Scale Test (Table 1)

SCA - Scale A to A

Adder Test (Table 2)

Select Bits in A

SAB - Set Bit in A
CAB - Clear Bit in A
MAB - Complement Bit in A

Enter Instructions

EN1 - Enter Index 1 Direct
ENA - Enter A Direct
EN2 - Enter Index 2 Direct
IN1 - Increase Index 1
EI1 - Enter and Increment Index 1
EI2 - Enter and Increment Index 2

IN2 - Increase Index 2
TA1 - Transfer A to Index 1
TA2 - Transfer A to Index 2

Section 2 - Two Storage Cycles

Memory References Direct
Load Bytes
Clear
Loads and Enters
Indirect Addressing Test
Indirect Jump Test
Index 1 Tests
Index 2 Tests

Section 3 - Three and Four Storage Cycles

Destructive Load
Replaces Test
Four Storage Cycle

Section 4 - I/O Instructions

Normal Channel Tests

SCB - Set Channel Bit
IAN - Input From Channel to A
CCB - Clear Channel Bit
TCB - Test Channel Bit
OAN - Output From A to Channel
OSN - Set Channel for Ones in A
OCN - Clear Channel for Zeros in A

Block Transfers

OTD - Output
IND - Input

General Notes on Section 4

Program Stops (with Maintenance Console)

Two program stops (SLS) (stop 1 and stop 2) are found at the start of the I/O instructions test. These stops allow the test operator to bypass either the normal channel test and/or the block transfer test. The bypass parameter flags "CHKBLOK" and "CHKNORM" are initialized during their respective stops and remain in effect for all subsequent passes through the command test. The bypass parameters can be reset by setting (P) to location "CBSTOP" and processing the stop 1 and stop 2 test operator options.

Three program stops (SLS) (stop 3, stop 4, and stop 5) are contained within the normal channel test. Stop 3 allows the test operator to select an input/output channel and bit combination for use as operands in the instruction test sequence. Stop 4 is used as a counter to designate the number of channels and number of bits that are to be tested. The initial value of the counter contains a channel count of 1 and a bit count of 1. Stop 5 occurs at the end of the normal channel instruction test sequence. This stop allows the test operator the option to either continue the normal channel test or to exit from the test.

Following an initial pass through the program stops in Section 4, the command test executes a series of parameter initializing instructions. These instructions allow the test to restart and provide a jump to the start of the command test. Assuming no error stop will occur, the command test will continuously loop through the entire program (including the I/O tests if previously selected).

Restart - Restart of Test

Assembler instructions for command test restart.

TABLE 1. SHIFT/SCALE TESTS

The following are the Shift/Scale network operands used in the BC Command Test.

A-Register	Correct Result	Bit 8	Shift Count	Input Number
0000	0000	0	0	0
0000	0000	1	1	1
0000	0000	1	2	2
0000	0000	1	4	3
0000	0000	1	8	4
0000	0000	1	F	5
FFFF	FFFF	1	0	6
FFFF	FFFF	1	1	7
FFFF	FFFF	1	2	8
FFFF	FFFF	1	4	9
FFFF	FFFF	1	8	10
FFFF	FFFF	1	F	11
4020	4020	1	0	12
0001	0002	1	F	15
FFFE	FFFE	1	0	16
AAAA	5555	1	1	17
AAAA	AAAA	1	0	18
5555	5555	1	0	19
5555	AAAA	1	1	20
CCCC	3333	1	2	21
CCCC	CCCC	1	0	22
3333	3333	1	0	23
3339	4CCE	1	2	24
F0F0	0F0F	1	4	25
0F4F	F0F4	1	4	26
FF00	00FF	1	8	27
00FF	FF00	1	8	28
FF00	7F80	0	1	29
FF00	FF00	0	0	30
F0F0	F0F0	1	0	31
00FF	00FF	1	0	32
000F	0000	0	4	33
0003	0000	0	2	34
0001	0000	0	1	35
00FF	0000	0	8	36
FF00	3FC0	0	2	37

TABLE 1. SHIFT/SCALE TESTS (Cont'd)

A-Register	Correct Result	SCALE	Input Number
FFFF	0000	SCALE	38
0000	0010	SCALE	39
8000	0000	SCALE	40
4000	0001	SCALE	41
2000	0002	SCALE	42
1000	0003	SCALE	43
0800	0004	SCALE	44
0400	0005	SCALE	45
0200	0006	SCALE	46
0100	0007	SCALE	47
0080	0008	SCALE	48
0040	0009	SCALE	49
0020	000A	SCALE	50
0010	000B	SCALE	51
0008	000C	SCALE	52
0004	000D	SCALE	53
0002	000E	SCALE	54
0001	000F	SCALE	55
F7FF	0000	SCALE	56
1FFF	0003	SCALE	57
00FF	0008	SCALE	58
00F7	0008	SCALE	59
00F3	0008	SCALE	60
40F3	0001	SCALE	61
42F3	0001	SCALE	62
02F3	0006	SCALE	63
0273	0006	SCALE	64
4273	0001	SCALE	65
4233	0001	SCALE	66
80C0	0000	SCALE	67
800C	0000	SCALE	68
0030	000A	SCALE	69
8010	0000	SCALE	70
8001	0000	SCALE	71
C001	0000	SCALE	72
E001	0000	SCALE	73

TABLE 1. SHIFT/SCALE TESTS (Cont'd)

A-Register	Correct Result	SCALE	Input Number
F001	0000	SCALE	74
F801	0000	SCALE	76
7FFF	0001	SCALE	
07FF	0005	SCALE	
007F	0009	SCALE	
0007	000D	SCALE	

TABLE 2. ADDER TESTS

The following are the adder operands used in the BC Command Test.

A-Register	Memory	Correct Result	G349	Adder General Bit	Input No.
Logical Product					
0000	0000	0000	0	X	0
FFFF	0000	0000	0	X	1
0000	FFFF	0000	0	X	2
FFFF	FFFF	FFFF	1	X	3
Exclusive OR					
0000	0000	0000	0	X	4
FFFF	FFFF	0000	0	X	5
FFFF	0000	FFFF	0	X	6
0000	FFFF	FFFF	0	X	7
Add					
0000	0000	0000	0	0	8
FFFF	0000	FFFF	0	0	9
0000	FFFF	FFFF	0	0	10
0001	FFFF	0000	1	1	11
FFFF	FFFF	FFFE	1	1	12
1111	1111	2222	0	0	13
2222	2222	4444	0	0	14
4444	4444	8888	0	0	15
8888	8888	1110	1	1	16
Subtract					
0000	0000	0000	1	1	17
FFFF	0000	FFFF	1	1	18
8888	8888	0000	1	1	19
CCCC	5555	7777	1	1	20
Add					
3333	AAAA	DDDD	0	0	21
Subtract					
0000	0001	FFFF	0	0	22
Add					
FFFF	0001	0000	1	1	23

TABLE 2. ADDER TESTS (Cont'd)

A-Register	Memory	Correct Result	G349	Adder General Bit	Input No.
Subtract					
FEFE	EFEF	0F0F	1	1	24
Add					
6666	5555	BBBB	0	0	25
9999	5555	EEEE	0	0	26
Subtract					
FDFD	DFDF	1E1E	1	1	27
F7F7	7F7F	7878	1	1	28
Add					
DFDF	0202	E1E1	0	0	29
EFEF	0101	F0F0	0	0	30
Subtract					
9999	5555	4444	1	1	31
FBFB	BFBF	3C3C	1	1	32
Add					
7F7F	0808	8787	0	0	33
1111	3333	4444	0	0	34
Subtract					
CCCC	AAAA	2222	1	1	35
Add					
BFBF	0404	C3C3	0	0	36
1111	7777	8888	0	0	37
Subtract					
815F	5555	2C0A	1	1	38
D52A	5555	7FD5	1	1	39
Add					
1111	BBBB	CCCC	0	0	40
3333	7777	AAAA	0	0	41
0707	0A0A	1111	0	0	42

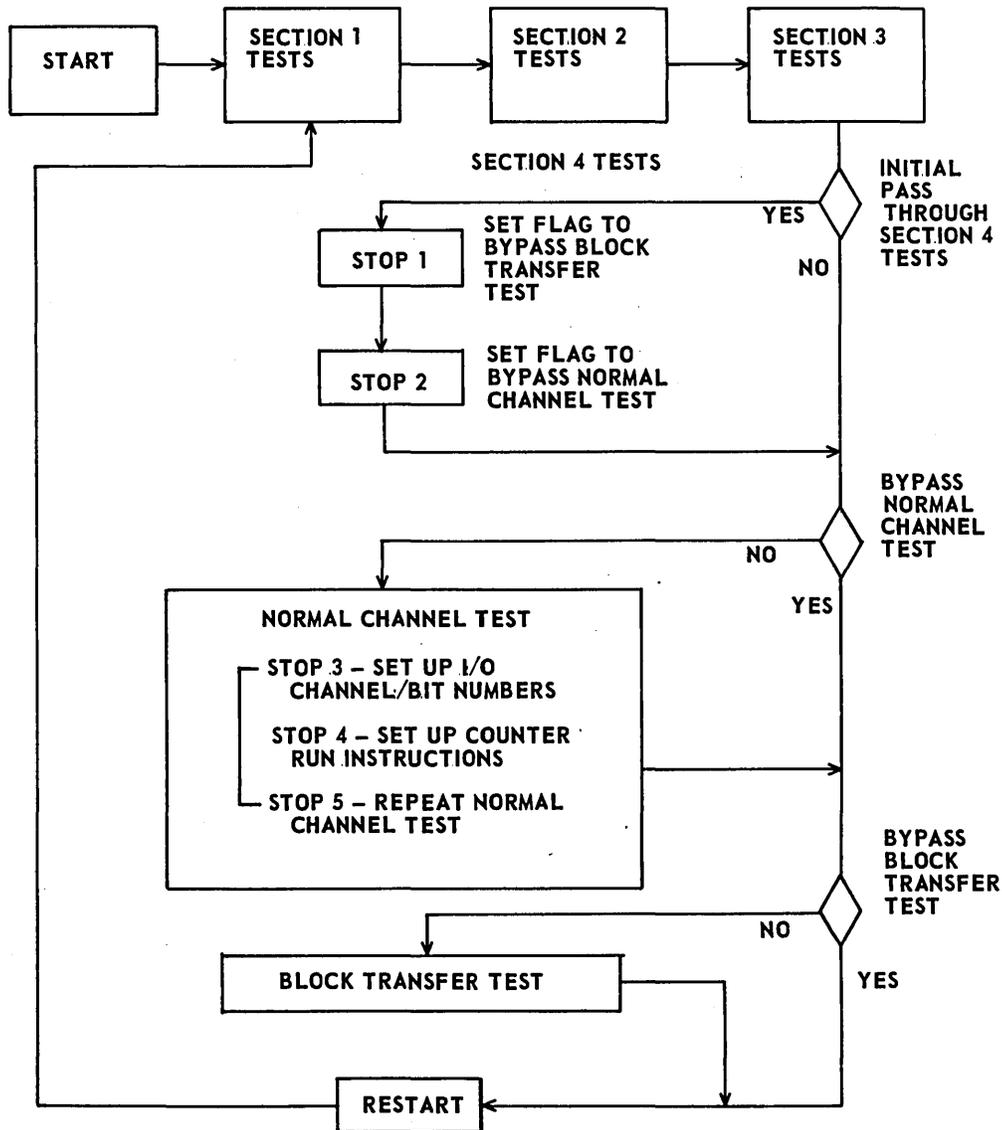
TABLE 2. ADDER TESTS (Cont'd)

A-Register	Memory	Correct Result	G349	Adder General Bit	Input No.
Subtract					
7070	5F5F	1111	1	1	43
0000	0100	FF00	0	0	44
0000	0010	FFF0	0	0	45
0C0C	AAAA	6162	0	0	46
F59F	5555	A04A	1	1	47
5555	AAAA	AAAB	0	0	48
8888	5555	3333	1	1	49
C0C0	AAAA	1616	1	1	50
Add					
0C0C	5555	6161	0	0	51

INDEX TO ADDER ANALYZER

Primary Inputs		Tested Instruct-ions	Correct Answer	Page	Primary Inputs		Tested Instruct-ions	Correct Answer	Page
M	A				M	A			
0000	0000	LP	0000	6	3333	1111			120
		LM		37	4444	4444		8888	90
		ADD		72	5555	OCOC		6161	137
		SUB		93		6666		BBBB	108
	FFFF	LP		15		815F	SUB	2COA	124
		LM	FFFF	59		8888		3333	135
		ADD		73		9999	ADD	EEEE	109
		SUB		95			SUB	4444	117
FFFF	0000	LP	0000	25	5555	CCCC	SUB	7777	97
		LM	FFFF	71		D52A		7FD5	125
		ADD		74		F59F		A04A	133
	FFFF	LP		29	5F5F	0707		1111	129
		LM	0000	53	7777	1111	ADD	8888	123
		ADD	FFFE	82		3333		AAAA	127
	0001		0000	75	7F7F	F7F7	SUB	7878	112
0001	0000	SUB	FFFF	103	8888	8888	ADD	1110	91
	FFFF	ADD	0000	104			SUB	0000	96
0010	0000	SUB	FFF0	131	AAAA	OCOC		6162	132
0100			FF00	130		3333	ADD	DDDD	101
0202	DFDF	ADD	E1E1	113		5555	SUB	AAAB	134
	EFEF		F0F0	116		C0C0		1616	136
0404	BFBF		C3C3	122		CCCC		2222	121
0808	7F7F		8888	119	BBBB	1111	ADD	CCCC	126
0A0A	0707		1111	128	BFBF	FBFB	SUB	3C3C	118
1111	1111		2222	87	DFDF	FDFD		1E1E	110
2222	2222		4444	89	EFEF	FEFE		0F0F	105

BLOCK DIAGRAM



BUFFER CONTROLLER MEMORY TEST (MEM)
(Formerly MEMORY)
(2 1/2D, 750 Nanoseconds Memory)

Operating Procedure

Restrictions

None

General Information

The memory test starts at location 0 upon completion of test loading and master clear.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console.

Type "AL=3" or "EX=3".

Master Clear and Channel Clear the Maintenance Console.

Run from location P = 0000.

Parameters

The operator may view/change the test parameters by enabling breakpoint on instruction at location X0080. There are two consecutive stops:

First Stop

B2 = 0000

B1 = Test number + section

A = Pseudo switches (preset to 0200)

Bit 0 - Not used	8000
1 - Stop at end of test/bank	4000
2 - Stop at end of pass	2000
3 - Stop at end of section	1000
4 - Stop at end of condition	0800
5 - Not used	0400
6 - Stop on error	0200
7 - Repeat test in same stack	0100
8 - Repeat test in same test area	0080
9 - Not used	0040
10 - Repeat pass	0020

Bit 11 - Repeat section	0010
12 - Repeat condition	0008
13 - Not used	0004
14 - Not used	0002
15 - Not used	0001

Second Stop

B2 = 0000

B1 = Test number + section

A = Sections (preset to FFC0)

Bit 0 = Section 0 - Addressing test

1 = Section 1 - Zeros test

2 = Section 2 - Ones test

3 = Section 3 - Checkerboard test

4 = Section 4 - Worst pattern test

5 = Section 5 - Sliding 1 then 0 - bit

6 = Section 6 - Sliding 1 then 0 - word

7 = Section 7 - Disturb test

8 = Section 8 - Worst pattern disturb

9 = Section 9 - Random

Normal Stops

B2 = 0000 - Parameter Stop

First Stop - B1 = Test number + section

B2 = 0000

A = Pseudo switches

Second Stop - B1 = Test number + section

B2 = 0000

A = Sections

B2 = 0800 - Condition Stop

First Stop - B1 = Test number + section

B2 = 0800

A = 0000

Second Stop - B1 = 1111

B2 = 2222

A = 0000

B2 = 1000 - End of Section Stop

First Stop - B1 = Test number + section

B2 = 1000

A = 0000

Second Stop - B1 = 1111

B2 = 2222

B2 = 2000 - End of Pass Stop

First Stop - B1 = Test number + section

B2 = 2000

A = 0000

Second Stop - B1 = 1111

B2 = 2222

A = 0000

B2 = 4000 - End of Test Stop

First Stop - B1 = Test number + section

B2 = 4000

A = 0000

Second Stop - B1 = 1111

B2 = 2222

A = 0000

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working.

On error stops, the following is displayed:

B2 = 0200 - Error

First Stop - B1 = Test number + section

B2 = 0200

A = Error code

Second Stop - B1 = Actual data

B2 = Expected data

A = Failing address

Third Stop - B1 = 1111

B2 = 2222

A = 0000

Section Description

Section 0 (Bit 0) - Addressing Test

Each address contains its own address.

1. Write up, read up, and check.
2. Write down, read down, and check.
3. Write up, read down, and check.
4. Write down, read up, and check.

Section 1 (Bit 1) - Zeros Test

1. Fill test areas with zeros, read, and check.
2. Repeated ten times.

Section 2 (Bit 2) - Ones Test

1. Fill test areas with ones, read, and check.
2. Repeated ten times.

Section 3 (Bit 3) - Checkerboard Test

1. Fill test areas with alternating 1 + 0, read, and check.
2. Repeated ten times.
3. Fill test areas with alternating 0 + 1, read, and check.
4. Repeated ten times.

Section 4 (Bit 4) - Worst Pattern Test

1. Fill test areas with worst pattern.
2. Read, and store all words on this word line.
3. Read, complement, and store all words on this word line.
4. Test all words on this word line.
5. Repeat from 2 on all word lines in test areas.
6. Check all word lines in test areas.

Section 5 (Bit 5) - Sliding 1 Then 0 on Bit Line

1. Fill test areas with zeros.
2. Slide a 1 down the bit line, test, and restore to zero.
3. Repeat from 2 for all bit lines.
4. Fill test areas with all ones.
5. Slide a 0 down the bit line, test, and restore to zero.
6. Repeat from 2 for all bit lines.

Section 6 (Bit 6) - Sliding 1 Then 0 On Word Line

1. Fill test areas with zeros.
2. Slide a 1 across the word line, test, and restore to zero.
3. Repeat from 2 for all word lines.
4. Fill test areas with all ones.
5. Slide a 0 across the word line, test, and restore to one.
6. Repeat from 2 for all word lines.

Section 7 (Bit 7) - Disturb Test

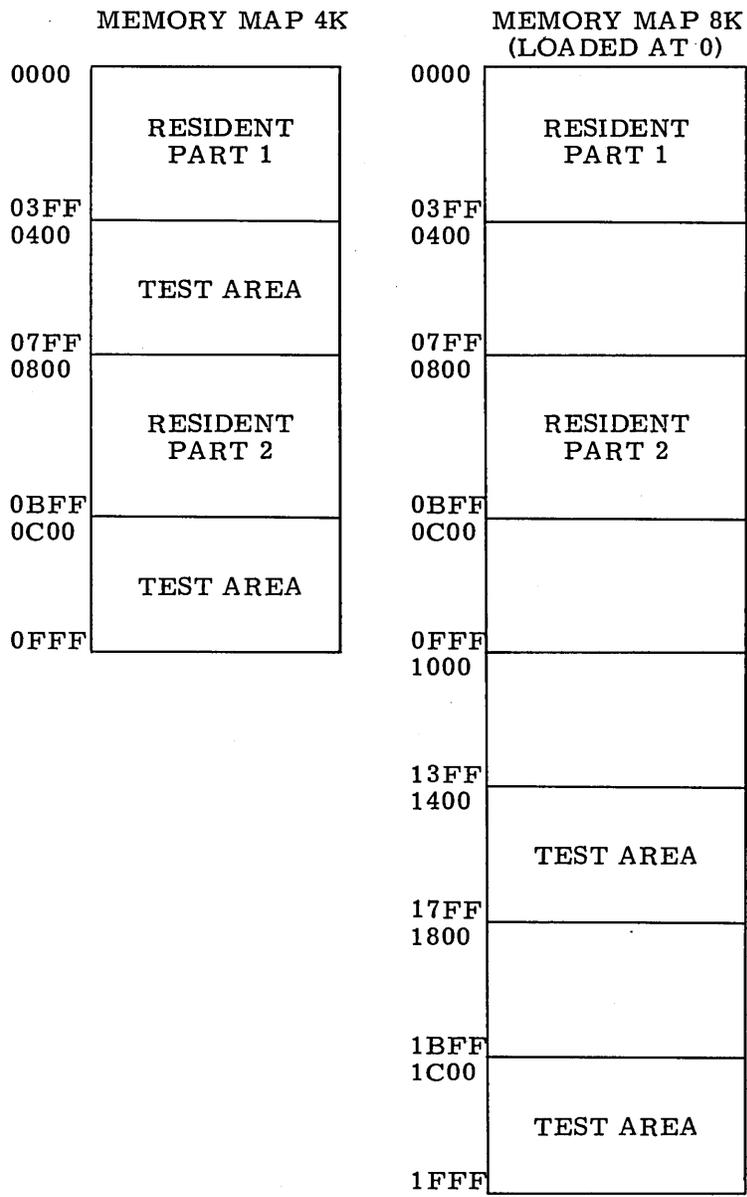
1. Fill test areas with all ones.
2. Store zeros in word to be tested.
3. Store a word of all ones 100 times above, below, and on either side of test cell.
4. Check test cell.
5. Repeat from 3 for all words in test area.
6. Perform 100 loads above, below, and on either side of test cell.
7. Check test cell.
8. Repeat from 6 for all words in test area.

Section 8 (Bit 8) - Worst Pattern Disturb

1. Fill test areas with worst pattern alternately reversing the current direction on the X line.
2. Read and verify the test areas.

Section 9 (Bit 9) - Random Test

1. Randomly write addresses in their address in test areas.
2. Repeat random sequence in 1 above verifying addresses.
3. Randomly generate code to execute a load, store, or no operation (TOV) sequence on a randomly generated address using random data.
4. Execute the generated code.
5. Verify the data.
6. Repeat 4096 times.



The test resident and test areas move end around within their respective stacks until all sections have run on all quarters. The resident then moves to the next stack if 8K or to address 0000 if 4K.

BUFFER CONTROLLER MEMORY TEST (MM1)
(Formerly MEMT1)
(FR101/BB104, 1.1 Microsecond)

Operating Procedure

Restrictions

Do not master clear unless the test is in low core and a restart is desired.

General Information

The memory test starts at location 0 upon completion of test loading and master clear.

Loading Procedure

Set the SELECTIVE STOP switch to ON.

Type "AL = 4" or, "EX = 4".

Master Clear and Channel Clear at the Maintenance Console.

Run from location 0000.

Parameters

Test selections and control parameters can be inserted by starting at location 0000 with the A register not equal to zero.

Parameters are preset to run all tests and repeat the section. Halts will occur only on detection of errors.

Procedure

After loading Master Clear, set the HALT on PARITY ERROR switch. If no parameter changes are to be made, run. If parameters are to be entered, set any bit in the A register.

Run. The program will halt at location 0004E. Setting the indicated bits in the A register will select the following:

Bit 15	Test 6 selected
Bit 14	Test 7 selected
Bit 7	Halt at end of section
Bit 6	Halt at end of test
Bit 5	Repeat selected test
Bit 4	8K memory option

After setting bits, run.

NOTE: When selecting the repeat test option, select only one test.

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working.

Two error routines are incorporated in MEMT1: Disturb Error Analysis and Error Analysis.

Disturb Error Analysis

When an error is encountered during a Disturb cycle, this routine is used to display the pertinent data. Two halts take place in this routine. Depending on where the program is resident, X will equal 0 for lower core and 8 for upper core. Z will equal the bank number.

First error halt at location P - ZX96

Register contents:

- B1 - Correct word
- B2 - Error data
- A - Address of error cell

Second error halt at location P - ZX98

- A - Current test number

Error Analysis

When an error occurs while reading data, this routine is used to display pertinent data.

First error halt at location P - ZX76

Register contents:

- B1 - Correct data
- B2 - Error data
- A - Address of error cell

Second error halt at location P - ZX84

Register contents:

- B1 - Test resident area*
- B2 - Testing area*
- A - Current test number

NOTE: The error data located in B2 is the logical difference between the correct data word and the incorrect data word. This represents bits picked up or dropped. Therefore, it is possible to determine the incorrect word as follows:

Example:	FFFF	CORRECT DATA	(B1)
	0100	ERROR DATA	(B2)
	EXC. OR	----	
	FEFF	ERROR WORD	(IN CORE)

* Lower core - 1; upper core - 2.

Memory parity errors cannot be detected by the software. If the PARITY ERROR switch is in the HALT position, a halt will occur and the operator can manually inspect the following registers.

S - Contains the address of the error cell

X - Contains the error data

To resume testing after a parity error halt, clear the parity error indication and run.

Section Description

This memory test consists of two segments labeled MEMT2 and MEMT1.

MEMT1 contains two comprehensive worst pattern tests.

Test 6 - Parity Plane Test

Tests the ability of each core in the parity plane to hold zero and one while the rest of the plane holds worst pattern and complement worst pattern.

Test 7 - Worst Pattern Test

Tests the ability of each location in the test area to hold worst pattern and complement worst pattern while the remainder of the test area holds worst pattern. Each location is tested to hold complement worst pattern and worst pattern while the remainder of the test area holds complement worst pattern.

Both tests use the following disturb method.

Disturbs are accomplished by reading a combination of locations (Y1) and (Y2).

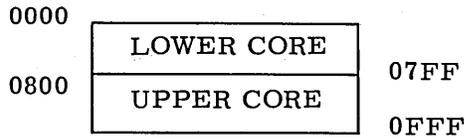
(Y1) is a location that contains all zeros and is in the same inhibit group as location (X) but not on a common drive line with (X). (Y2) has the same specification as (Y1) except that it is on a common drive line with location (X).

Philosophy

The tests in MEMT1 are designed to reside in and test a 4K memory stack. An option is provided to test two 4K stacks or 8K of memory. This option can be expanded to test any number of 4K stacks of the same memory. However, testing will remain the same as if each stack were an individual memory. All tests use a common relocation and error routine. Additional tests can be added provided they conform to the existing concepts, parameters, etc.

Method

The 4K stack is divided into two sections referred to as lower core (0000-07FF) and upper core (0800-0FFF). When the test resides in lower core, upper core will contain the pattern and be tested. The test is then relocated to upper core and then lower core will contain the pattern and be tested.



BUFFER CONTROLLER MEMORY TEST (MM2)
 (Formerly MEMT2)
 (FR101/BB104, 1.1 Microsecond)

Operating Procedure

Restrictions

After an error stop, do not Master Clear unless test is resident in quadrant zero, and a restart is desired.

General Information

The memory test starts at location 0 upon completion of test loading and master clear.

Loading Procedure

Set the SELECTIVE STOP switch to ON on the Maintenance Console.

Type "AL = 5" or "EX = 5".

Master Clear and Channel Clear on the Maintenance Console.

Run from location 0000.

Parameters

Test selection and control parameters can be inserted by starting at location 0000 with the A register not equal to zero. Parameters are preset to run all tests and repeat the section. Halts will occur only upon detection of errors.

Procedure

After loading Master Clear, set HALT on PARITY ERROR switch. If no parameter changes are to be made, run. If parameters are to be entered, set any bit in the A register.

Run. The program will halt at location 002C. Setting the indicated bits in the A register will select the following.

NOTE: The 8K memory option must be selected when 8K is available.

Bit 15 Test 1 selected

Bit 14 Test 2

Bit 13 Test 3

Bit 12 Test 4
 Bit 11 Test 5
 Bit 7 Halt at end of section
 Bit 6 Halt at end of test
 Bit 5 Repeat selected test
 Bit 4 8K memory option

After the A register is set up as desired, run.

NOTE: When selecting the repeat test option, select only one test to run, otherwise the first test selected will be repeated.

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working.

Error Analysis

Upon detection of an error the first of two error halts will occur at location ZX57 (x - 0, 4, 8 or C depending on the quadrant the test resides in at the time and Z - bank number). Pertinent data is displayed in the following registers.

First error halt at location P - ZX57

- B2 - Error data
- B1 - Correct data
- A - Location of error cell

Second error halt at location P - ZX6E

- B2 - Number of test quadrant
- B1 - Number of quadrant test resides in
- A - Number of test running

NOTE: The error data located in B2 after the first halt is the logical difference between the correct data word and the incorrect data word. This represents bits picked up or dropped, therefore, it is possible to determine the incorrect word as follows:

Example 1	012F	Correct data
	EXC. or 1001	Error data (B2)

	112E	Error word (in core)
Example 2	FFFF	Correct data
	EXC. or 0100	Error data

	FEFF	Error word (in core)

After the first halt, returning the switch to RUN will result in the second halt. After the second halt, returning the switch to RUN will resume the testing where it left off.

CAUTION: Do not Master Clear unless test is resident in quadrant 0 and you desire to start over.

NOTE: Error data displayed in B2 represents bits dropped or picked up (failing bits).

A memory parity error indication cannot be sensed by the program. If the PARITY ERROR switch is in the HALT position, a halt will occur on a parity error and the operator can manually inspect the following registers:

S register	Contains the error cell address
X register	Contains the error data

After a parity error halt, clear the parity error and run.

Section Description

This memory test will consist of two segments labeled MEMT2 and MEMT1.

MEMT2 contains five memory quick check tests.

Test 1 - Zeros Test

Tests the ability of locations to hold all zeros.

Test 2 - Ones Test

Tests the ability of all locations to hold all ones.

Test 3 - Address Test

Tests the S register and the ability of each cell, in the test stack, to hold its own address.

Test 4 - Shifting Zeros

Tests the ability of each plane to hold all zeros while the rest of the planes hold all ones.

Test 5 - Shifting Ones

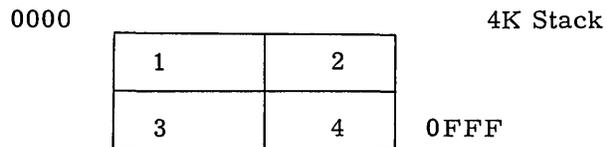
Tests the ability of each plane to hold all ones while the rest of the planes hold all zeros.

Test Philosophy

The tests in MEMT2 are designed to reside in and test a 4K memory stack. An option to test two 4K stacks or 8K of memory is provided. However, testing will remain the same as if each stack were an individual memory. All tests use a common relocation and error routine and all testing is done on a quadrant basis.

Method

The 4K stack is divided into four sections referred to as quadrants. When the test is resident in quadrant 1 a pattern will be written into quadrants 2, 3, and 4. Quadrant 4 will be tested. The test will then be moved to quadrant 2, a pattern will be written into quadrants 1, 3, and 4 and quadrant 3 will be tested; and so on in this manner until all quadrants are tested.



BUFFER CONTROLLER MEMORY TEST (MY1)
(Formerly BCMY1)
(FV156, 200 Nanosecond Memory)

Operating Procedure

Restrictions

None

General Information

The memory test starts at location 0 upon completion of test loading and master clear. Restart of the test following any stop is accomplished by setting the (P) to location 0.

NOTE: Location 0 may be at 0, 200 hex, 800 hex or at A00 hex depending on where the test is residing at the time it is stopped.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console

Type "AL = 6" or "EX = 6".

Master Clear and Channel Clear the Maintenance Console.

Run from location 0000.

Parameters

The operator may select certain parameters by enabling SELECTIVE STOP. There are two consecutive parameter stops at which point the operator can select parameters.

The First Stop

(A) = 00XX - 0001 initially
= 00X1 - Stop on error
= 00X2 - Stop at end of section
= 00X4 - Stop at end of test
= 00X8 - Repeat section

The Second Stop

(A) = XXXX - F860 initially
= 8XXX - Addressing test

- (A) = 4XXX - Zeros test
- = 2XXX - Ones test
- = 1XXX - Checkerboard test
- = X8XX - Odd parity pattern test
- = XX4X - Random data test
- = XX2X - Random addressing test

Parameters can also be changed at end of test stop same as in 1 and 2 above.

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working. No programmed stop will occur in test sections 1, 2, 3, or 4 unless a failure is encountered.

On error stops, the following is displayed:

First Stop

- A = Address of tested location
- B1 = Correct data
- B2 = Actual data

Second Stop

- A = (PARM001)
- B1 = FWA of parameters
- B2 = Section number

Section Description

NOTE: All referrals to complemented data are one's complement.

Addressing Test (each location holds its own address)

1. Write up, read up, and check.
2. Write down, read down, and check.

Zeros Test

1. Write zeros in all locations.
2. Read each location three times checking data on the third read.

Ones Test

1. Write ones in all locations.
2. Read each location three times checking data on the third read.

Checkerboard Test

1. Write alternate word lines of AAAA, AAAA, AAAA, AAAA and 5555, 5555, 5555, 5555.
2. Read each location three times checking data on the third read.
3. Complement the pattern and repeat 1 and 2.

Odd Parity Pattern Test (special parity pattern)

1. Write pattern in memory.
2. Read each word three times and check data on the third read.

Random Data (a pass number is available to change the random data generated)

1. Generate and store random data.
2. Read and check data.

Random Addressing

1. Each location has its own address written into it.
2. A group of 32 addresses are formed, read, and checked.
3. Repeat 1 and 2 1000 times.

Sample of Sliding One On Bit Line

```

00100000000000000010
00100000000000000010
00100000000000000010 Across is word line
00100000000000000010
00100000000000000010
00100000000000000010
00100000000000000010
00100000000000000010

```

Up is bit line

Sample of Sliding One On Word Line

```

00000000000000000000
00000000000000000000
00000000000000000000 Across is word line
00000000000000000000
11111111111111111111
00000000000000000000
00000000000000000000
00000000000000000000

```

Up is bit line

Test Layout

Test resides respectively in:

1. Area marked "RES1", testing area marked "TEST1"
2. Area marked "RES2", testing area marked "TEST2"
3. Area marked "RES3", testing area marked "TEST3"
4. Area marked "RES4", testing area marked "TEST4"

SEG1	SEG2	SEG3	SEG4	
03FF	07FF	0BFF	0FFF	Memory Plane 1
RES3	RES3	RES4	RES4	
TEST2	TEST2	TEST1	TEST1	
0200	0600	0A00	0E00	
01FF	05FF	09FF	0DFF	Memory Plane 0
RES1	RES1	RES2	RES2	
TEST4	TEST4	TEST3	TEST3	
0000	0400	0800	0C00	

BUFFER CONTROLLER MEMORY TEST (MY2)
(Formerly BCMY2)
(FV156, 200 Nanosecond Memory)

Operating Procedure

Restrictions

None

General Information

The memory test starts at location 0 upon completion of test loading and master clear.

Restart of the test following any stop is accomplished by setting the (P) to location 0.

NOTE: Location 0 may be at 0, 200 hex, 800 hex or at A00 hex depending on where the test is residing at the time it is stopped.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console.

Type "AL = 7" or "EX = 7".

Master Clear and Channel Clear the Maintenance Console.

Run from location 0000.

Parameters

There are two consecutive parameter stops at which point the operator can select parameters.

On the First Stop -

- (A) = 00XX - 0001 initially
 - = 00X1 - Stop on error
 - = 00X2 - Stop at end of section
 - = 00X4 - Stop at end of test
 - = 00X8 - Repeat section

On the Second Stop -

- (A) = XXXX - 0780 initially
 - = X4XX - Sliding one, then zero on bit line
 - = X2XX - Sliding one, then zero on word line
 - = X1XX - Disturb test
 - = XX8X - Disturb complement test

Parameters can also be changed at end of test stop same as in 1 and 2 above.

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working. No programmed stop will occur in test sections 1, 2, 3, or 4 unless a failure is encountered.

On error stops, the following is displayed:

First Stop

A = Address of tested location
B1 = Correct data
B2 = Actual data

Second Stop

A = (PARM001)
B1 = FWA of parameters
B2 = Section number

Section Description

NOTE: All referrals to complemented data are one's complement.

BCMY2 Test Sections

Sliding One, Then Zero on Bit Line Test

Sliding One

1. One of the 16 bit lines of a word on a word line is set to one, the other bits in that word are set to zero.
2. The same pattern is repeated for the other three words on the word line and throughout the portion of memory being tested.

3. Read data and check it.
4. Shift pattern to other 15 bit positions and repeat 1, 2, and 3

Sliding One, Then Zero on Word Line

Sliding One

1. The portion of memory being tested is set to all zeros.
2. Set one entire word line to all ones.
3. Read word line of all ones and check data.
4. Repeat 1, 2, and 3 with next word line set to all ones.

Sliding Zero (same as sliding one with complement data)

Disturb Test (each location X is tested as follows)

1. Write X with all ones, 1000 times.
2. Write (X-1) and (X+1) locations with zeros 1000 times each alternating between the two.
3. Write X with zeros.
4. Write (X-1) and (X+1) with ones, 1000 times alternating between the two.
5. Location X is quickly read out and checked.

Disturb Test Complement

Same as Disturb Test with complemented data.

BUFFER CONTROLLER MEMORY TEST (BCM)
(Formerly BCMY4)

Operating Procedure

Restrictions

None

General Information

The memory test starts at location 0 upon completion of test loading and master clear.
Restart of the test following any stop is accomplished by setting the (P) to location 0.

NOTE: Location 0 may be at 0, 200 hex, 800 hex or A00 hex depending on where the test is residing at the time it is stopped.

BCM is the same as BCMY4 the Word Organized Memory Test.

Loading Procedure

Set the SELECTIVE STOP switch on the Maintenance Console.

Type "AL = 8" or "EX = 8".

Master Clear and Channel Clear the Maintenance Console.

Run from location 0000.

Parameters

Parameters start at address 2:

PARM001 Preset to 4600 Hex

- Bit 1 = Stop at end of test (4XXX)
- Bit 3 = Stop at end of section (1XXX)
- Bit 5 = Stop on error (X4XX)
- Bit 6 = Run 8K on second pass (X2XX)
- Bit 11 = Repeat section (XX1X)

PARM002 Preset to 7800 Hex

- Bit 0 = Not used
- Bit 1 = Section 1 (digit noise)
- Bit 2 = Section 2 (sliding one, then zero)
- Bit 3 = Section 3 (add one, FFFF times)
- Bit 4 = Section 4 (word line disturb)

Error Stops

The SELECTIVE STOP switch must be set before running the test. The Selective Stop instruction (SLS) is used for error stops and is assumed to be working. No programmed stop will occur in test sections 1, 2, 3, or 4 unless a failure is encountered.

When running from SMM 6000 or 7000, the section counter will stop incrementing when an error occurs.

On error stops, the following is displayed:

First Stop

A = Address of tested location
B1 = Correct data
B2 = Actual data

Second Stop

A = (PARM001)
B1 = FWA of parameters
B2 = Section number

Section Description

NOTE: All referrals to complemented data are one's complement.

BCM Test Sections

Digit Noise Test (Attempt to generate noise on digit current turnoff, thereby causing a failure on the next Read operation.)

1. Store all ones in memory portion to be tested.
2. Store all zeros in same memory segments but in the other memory plane.
3. Store all zeros in memory word (X).

4. Store Load A (X) instruction on the same word line as (X).
5. Jump to Load instruction stored in 4 above, read and check data.
6. When each location has been tested, repeat 1 through 5 using complemented data.

Sliding One, Then Zero in One Word Test -

1. Store all zeros in memory.
2. Store all in location (X).
3. Read and write location (X) three times (check data on last read).
4. Shift data left one place in location (X).
5. When each location has been tested, repeat 1 through 4 using complemented data.

Add One, FFFF times, to each location. No data check is done. Parity error stop is expected if a memory problem exists.

Word Line Disturb Test

1. Write all ones in the first test segment.
2. Write all ones in the corresponding non-test segment.
3. Write the first test location 100 times using the same pattern of step 1.
4. Store the complement of step 3 at the test location.
5. Disturb memory by performing a 2-instruction loop 100 times.
6. Read and check the test location.
7. Restore the test location with the original pattern.
8. Repeat steps 3 through 7 for each of 200 hex test locations.
9. Repeat steps 3 through 8 with the complement patterns.
10. Calculate the word line address. Use the address of the store instruction of step 4 to define a corresponding location within the non-test segment.
11. Store the complement of the contents of the word line address at the word line address.
12. Repeat steps 3 through 9.
13. Repeat steps 1 through 12 using the following patterns for steps 1 and 2.

Step	Test Segment Pattern	Non-Test Segment Pattern
A	All Ones	All Zeros
B		

<u>Step</u>	<u>Test Segment Pattern</u>	<u>Non-Test Segment Pattern</u>
A	All Zeros	
B		All Ones
A	All Zeros	
B		All Zeros

14. Repeat steps 1 through 13 for the second segments.
15. Relocate test.

Sample of Sliding One On Bit Line

```

00100000000000000010
00100000000000000010
00100000000000000010   Across is word line
00100000000000000010
00100000000000000010
00100000000000000010
00100000000000000010
00100000000000000010
00100000000000000010

Up is bit line

```

Sample of Sliding One On Word Line

```

00000000000000000000
00000000000000000000
00000000000000000000   Across is word line
00000000000000000000
11111111111111111111
00000000000000000000
00000000000000000000
00000000000000000000

Up is bit line

```

Test Layout

Test resides respectively in:

1. Area marked "RES1", testing area marked "TEST1"
2. Area marked "RES2", testing area marked "TEST2"
3. Area marked "RES3", testing area marked "TEST3"
4. Area marked "RES4", testing area marked "TEST4"

SEG1	SEG2	SEG3	SEG4	
03FF	07FF	0BFF	0FFF	
RES3 TEST2	RES3 TEST2	RES4 TEST1	RES4 TEST1	Memory Plane 1
0200	0600	0A00	0E00	
01FF	05FF	09FF	0DFF	
RES1 TEST4	RES1 TEST4	RES2 TEST3	RES2 TEST3	Memory Plane 0
0000	0400	0800	0C00	

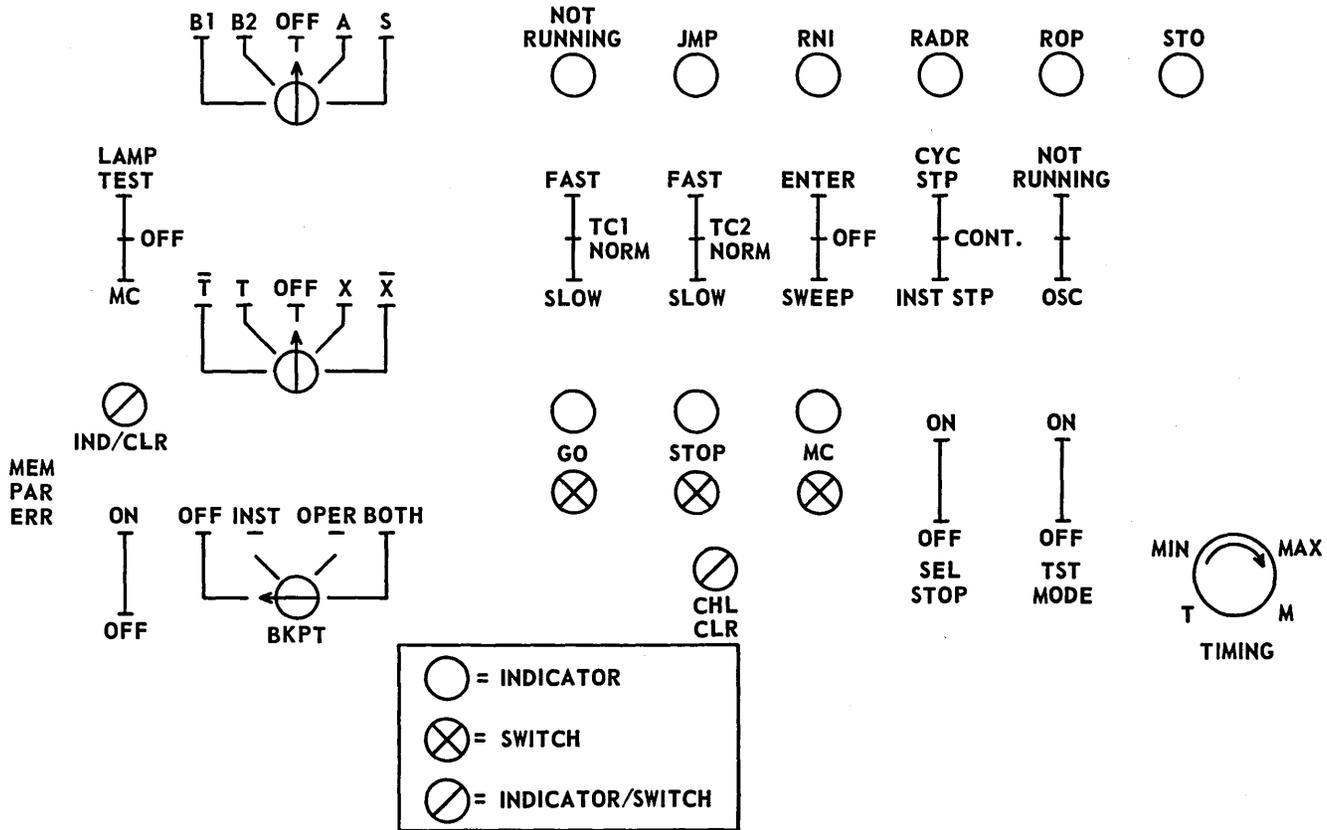
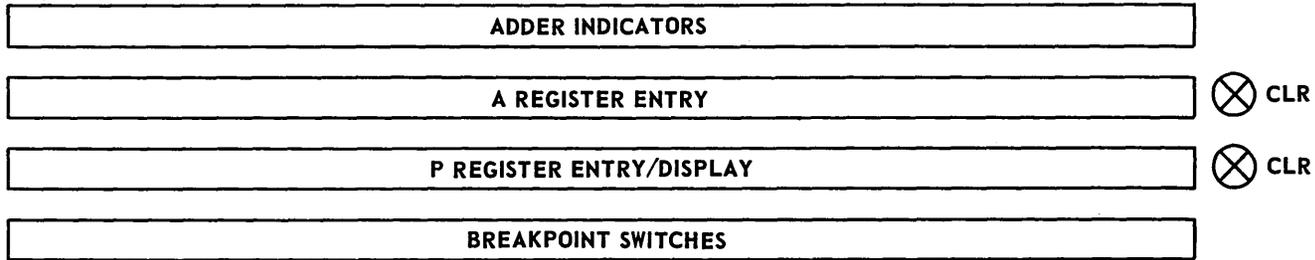
<u>S No.</u>	<u>Stored In BC At*</u>	<u>1700 Expects</u>	<u>Comments</u>
	000		Number of captured status words in the BC
01	001	FF80	First capture depicting coupler not ready
02	002	FF89	Coupler ready/data time out
03	003	FF81	Coupler ready, data time out cleared
04	004	FF80	Coupler ready cleared
05	005	FF84	Director 1 A = 1 causing clear coupler status
06	006	FF80	Clear above
07	007	FFA3	Director 2 A = 1 clear coupler
08	008	FF80	Clear above
09	009	FFB3	Director 3 A = 1/clear coupler
10	00A	FF80	Clear above
11	00B	FFC3	Director 4 A = 1/clear coupler
12	00C	FF80	Clear above
13	00D	FFD3	Director 5 A = 1/clear coupler
14	00E	FF80	Clear above
15	00F	FFE3	Director 6 A = 1/clear coupler
16	010	FF80	Clear above
17	011	FFF3	Director 7 A = 7/clear coupler
18	012	0000	Status extension area
19	013	0000	Status extension area
20	014	0000	Status extension area

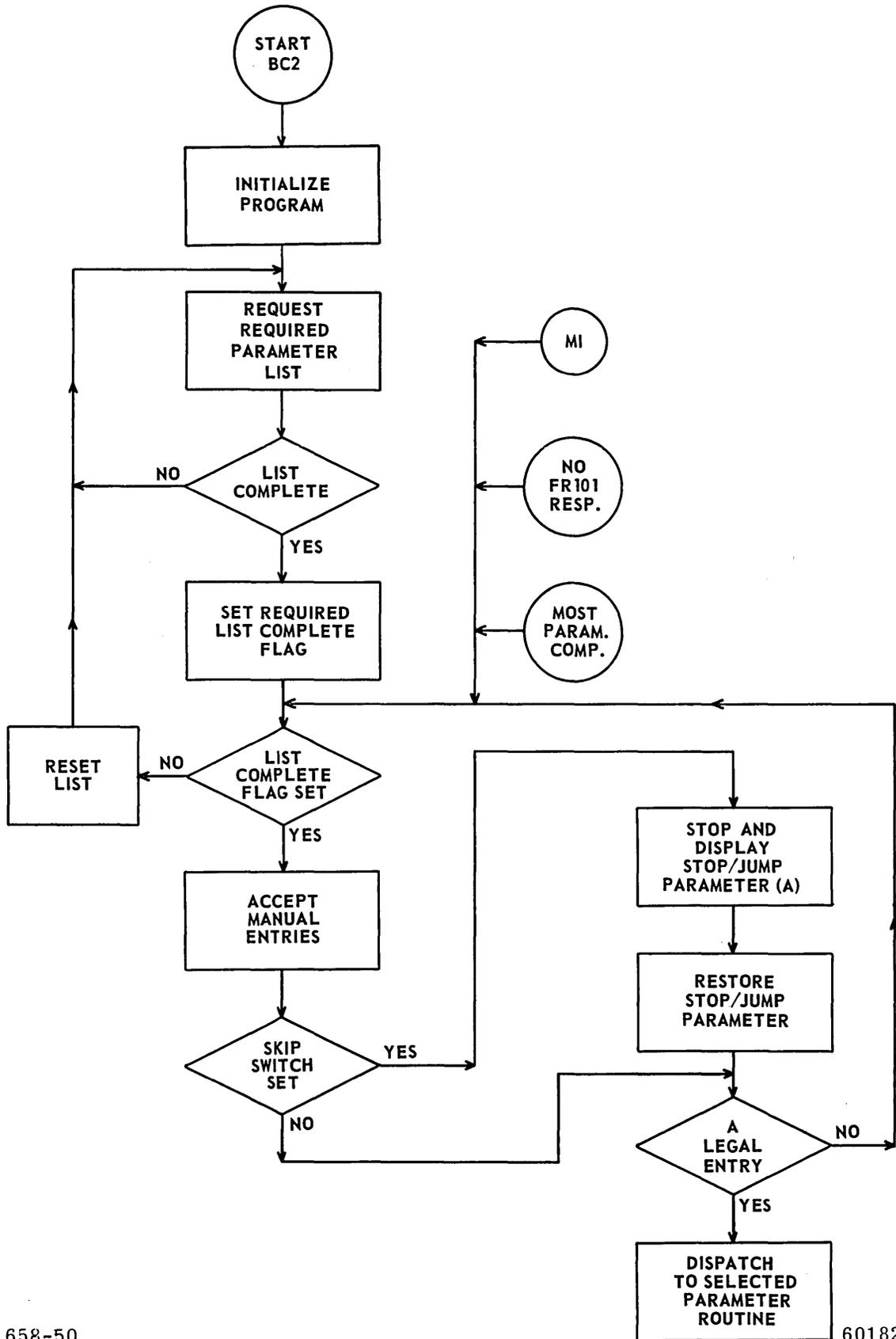
* The actual status may be examined in the buffer controller should it not be transferred to the 1700. Three conditions can cause the data not to be shipped back to the 1700:

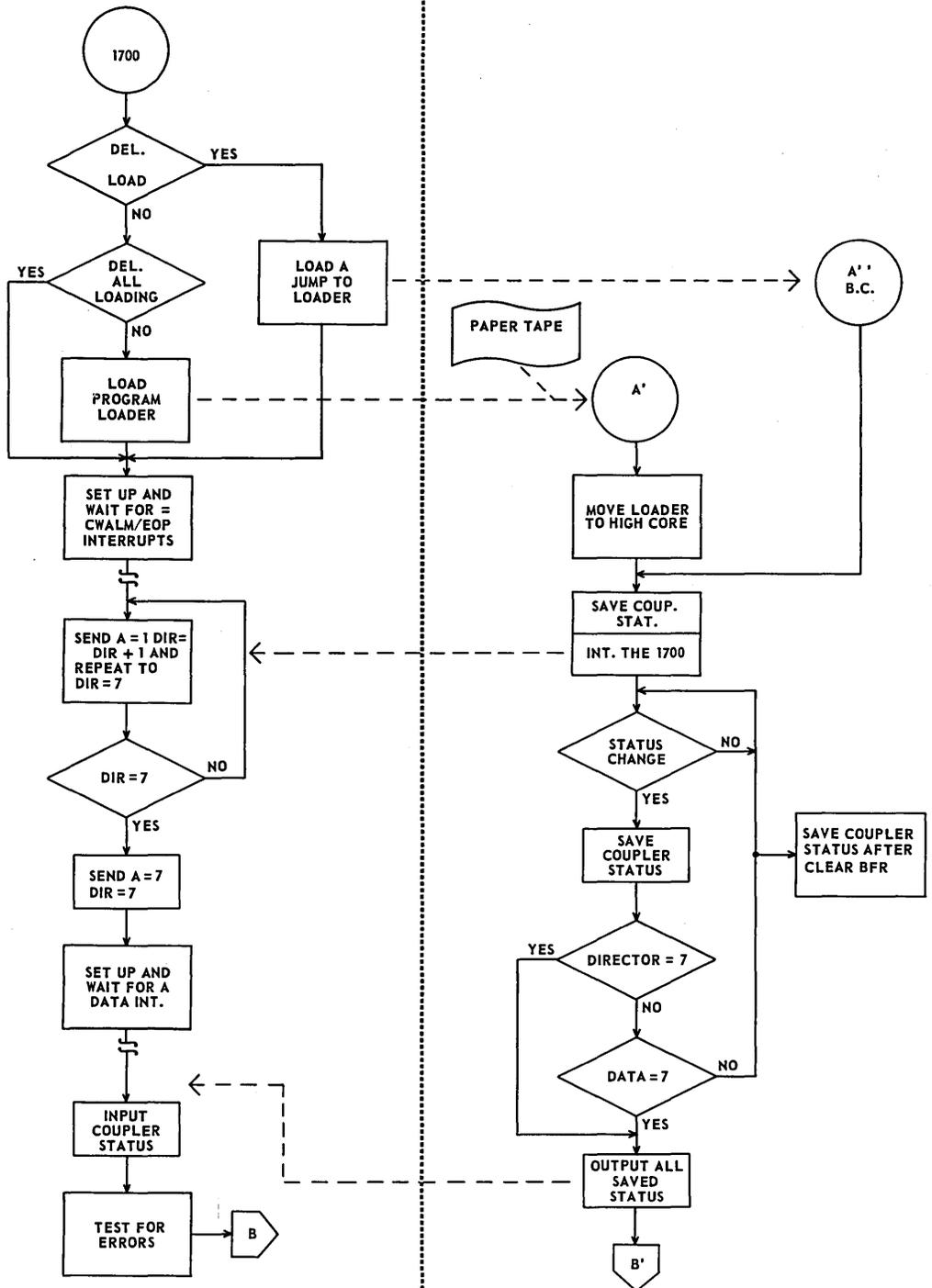
1. The EOP/Alarm interrupts did not issue to the 1700 (step the 1700 and status the coupler via Director 1) or coupler busy did not set on Director 2 in the 1700. Both of these conditions will not give any coupler status (junk at 02 - 14).
2. A Director 7 with A = 7 was never received (coupler status list incomplete).
3. The status was taken and an attempt to ship was made but the Data interrupt failed.

** A Director 7 or A = 7 is sufficient to terminate the coupler status collection and force the return of the status to be 1700.

Figure 1. Coupler Status





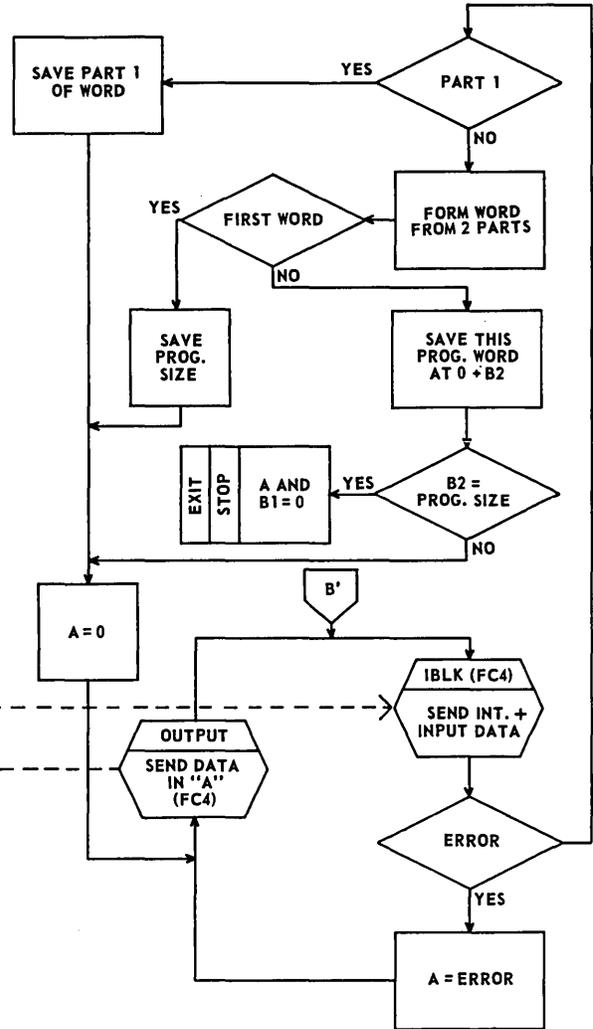
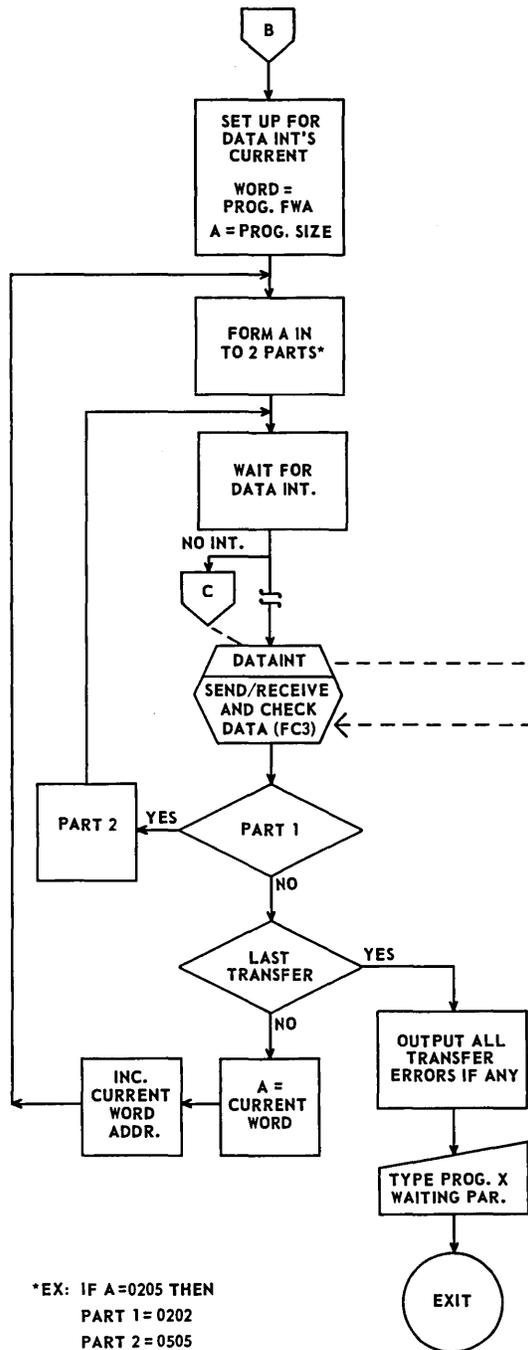


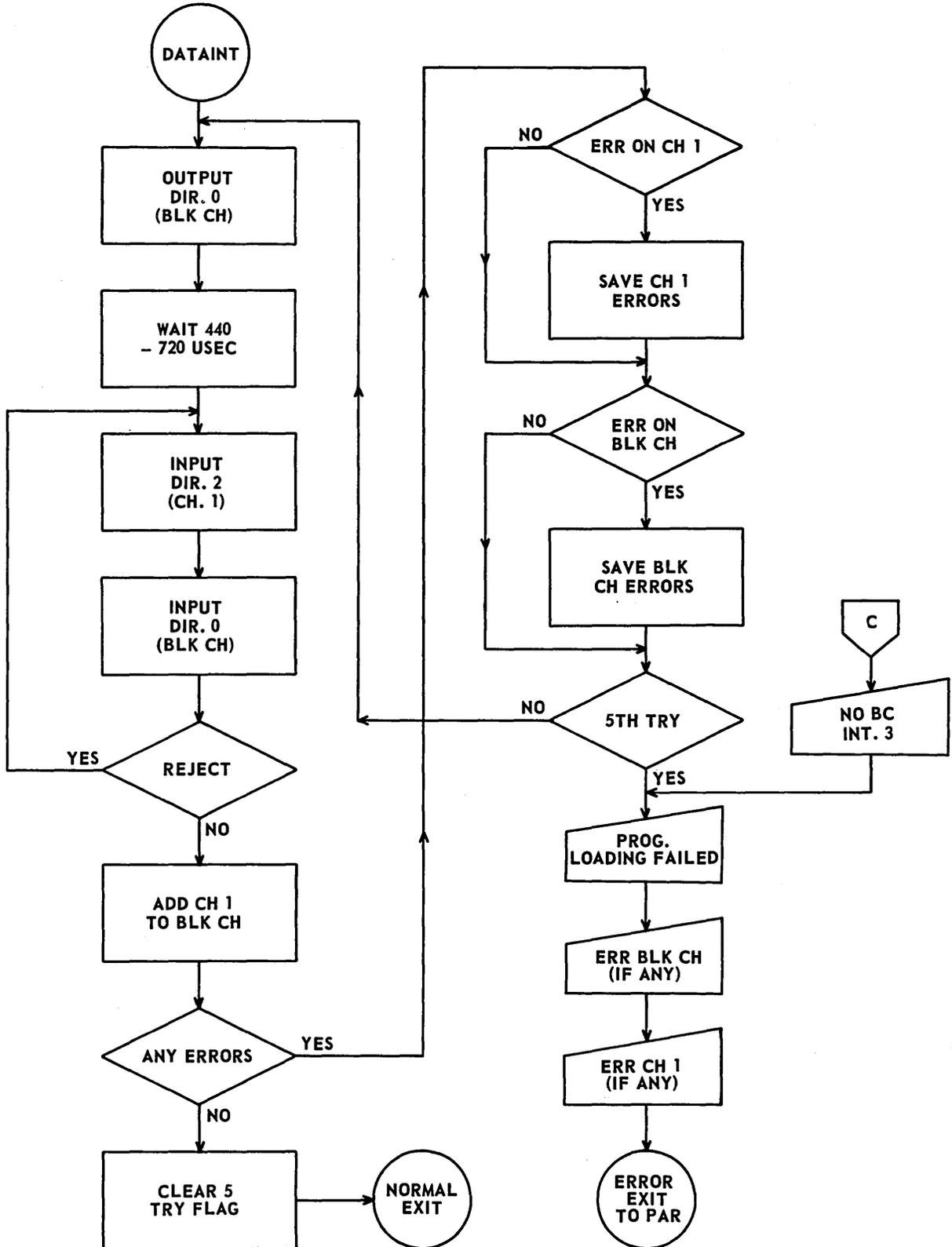
1700

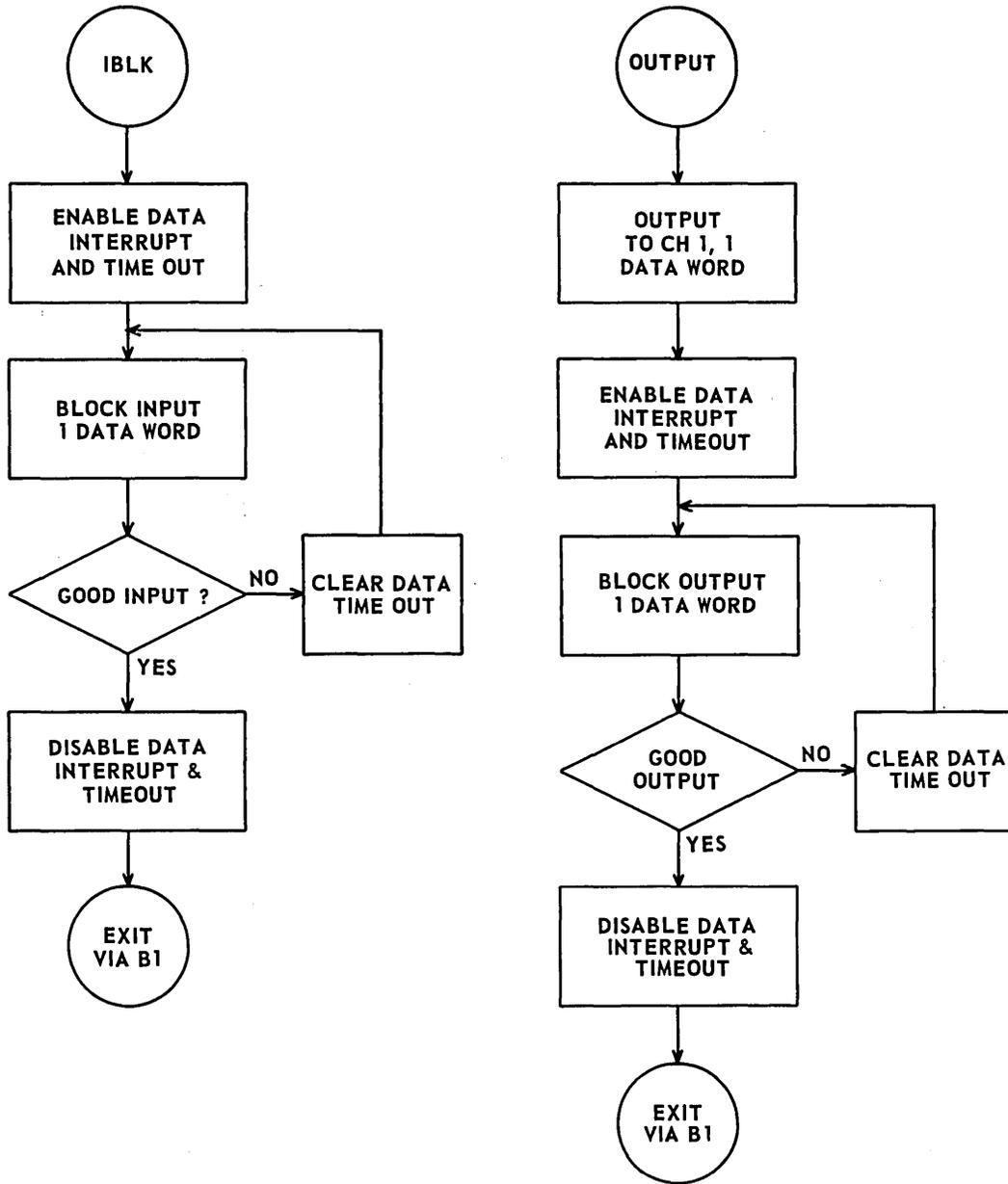
LOAD PROGRAM (2 OF 2)

B.C.

FC2







1700/FR101/955 TRANSPORT TEST

(RX4A34 Test No. 34)

I. OPERATING PROCEDURE

A. RESTRICTIONS

1. Requires an 8K 1700 with a 608 or 609 MT and a TTY.
2. The diagnostic interfaces to SMM17 only for loading.
3. Test parameters are accepted only from TTY.
4. Manual parameters must be terminated with the BC equipment code.
5. Entries performed after a parameter request must be terminated with a CR.
6. The test may not be run in an off-line mode unless the system includes a maintenance console.

B. RX4 LOADING PROCEDURE

The standard SMM17 calls as test number 34. See Table 1 for loading procedure. Following the initial test typeout (begin RX4/1700/FR101/955 Transport Test IA = XXX, Rev. X.X.) the program will request module selection by typing:

SMX=Y

The operator should now define the BC equipment code (X) before selecting the desired module (Y).

Module 1 = Optical Dump and Stepping Accuracy Test

Module 2 = Undefined

After module selection the program will request the BC interrupt line by typing:

BIX = Y

The operator should now define the interrupt line (Y) for the BC X.

TABLE 1. RX-4 STANDARD LOADING PROCEDURE

Step	Procedure
1	<p style="text-align: center;">NOTE</p> <p>Manual parameter entries following the "=" sign at the TTY must be terminated by a carriage return. The asterisk (*) equals buffer controller equipment code selected.</p> <p>Ensure that system is energized.</p>
2	<p>Set EQUIPMENT SELECT switches at rear of buffer controller to selected equipment code (1 to F).</p>
3	<p>Open rear door of tape controller and set EQUIPMENT switch to 7.</p>
4	<p>At tape transport, set UNIT SELECT switch to 0. Mount SMM17 controlware maintenance tape and position to load point.</p>
	<p style="text-align: center;">NOTE</p> <p style="text-align: center;">Perform step 5 only if two tape transports are available. If only one tape transport is available, proceed to step 6.</p>
5	<p>At second tape transport, set UNIT SELECT switch to 1. Mount SMM17 auxiliary test tape and position to load point.</p>
6	<p>Set CLEAR. Press P REGISTER SELECT pushbutton. Set 1FCO (0001 1111 1100 0000) into Display register.</p>

TABLE 1. RX-4 STANDARD LOADING PROCEDURE (Cont'd)

Step	Procedure
7	<p>Press X REGISTER SELECT pushbutton. Set ENTER. Set SELECTIVE STOP. Enter SMM17 bootstrap program instructions (see SMM17 Reference Manual) as follows:</p> <ol style="list-style-type: none"> a. Set instruction into Display register b. Set STEP c. Press CLEAR pushbutton d. Repeat until all instructions are entered.

TABLE 1. RX-4 STANDARD LOADING PROCEDURE (Cont'd)

Step	Procedure
	<p>Set ENTER SWEEP switch to center position. Set CLEAR.</p>
8	<p>Press P REGISTER SELECT pushbutton. Set 1FCO (001 1111 1100 0000) into Display register. Set SELECTIVE STOP and SELECTIVE SKIP switches. Set RUN.</p>
9	<p>Press Q REGISTER SELECT pushbutton. Set 0205 (0000 0010 0000 0101) into Display register. Set RUN.</p>
10.	<p>Press AQ REGISTER SELECT pushbutton. Set 30B0 0011 0000 1011 0000) into Display register. Set SELECTIVE SKIP switch to center position. Set RUN.</p>
11.	<p>TTY prints SMM17 ED 3.0 ,</p>
12.	<p>Press A REGISTER SELECT pushbutton. Set 3401 (0011 0100 0000 0001) into Display register. Set RUN.</p>
13.	<p>Press A REGISTER SELECT pushbutton. Set 0000 (0000 0000 0000 0000) into Display register. Set RUN.</p>

TABLE 1. RX-4 STANDARD LOADING PROCEDURE (Cont'd)

Step	Procedure
14.	TTY prints BEGIN RX-4 1700/FR101/955 TRANSPORT TEST IA-XXX. Prints SM*. Type selected buffer controller equipment code (1 to F).
15.	TTY prints =. Type number of module test to be performed (1 to 2).
16.	TTY prints BI*= Type interrupt line for selected buffer controller (1 to F).
17.	TTY prints ENTER PARAMETER. Type AP*.
18.	TTY prints ENTER PARAMETER.
<p>NOTE</p> <p>Perform step 19 only if SMM17 auxiliary test tape is not loaded. If two tape transports are available and SMM17 auxiliary test tape is already loaded (step 5), proceed to step 20.</p>	
19.	At tape transport, set UNIT SELECT switch to 1. Mount RX4 auxiliary test tape and position to load point.
20.	If the tape transport is a 659: Type TD* TTY prints = Type 659 TTY prints 3518 #= Type 3518 equipment number (1-7).
21.	Type AL*.
22.	TTY prints =. Type H (hardware) or S (controlware). Program autoloads selected module to buffer controller.

TABLE 1. RX-4 STANDARD LOADING PROCEDURE (Cont'd)

Step	Procedure
23.	TTY prints THE BC IS LOADED if autoloading was successful. If autoloading failed, TTY prints CHECKSUM ERROR, or BC does not respond.

NOTE

RX-4 standard loading procedure complete.
 Proceed to appropriate module test operating procedure as follows:

Module 1 - Section I. D.
 Module 2 - Undefined

C. MODULE AUTOLOAD PROCEDURE

1. Select Automatic Parameter (AP*)

Upon selection the program will set up the standard I/O equipment table (see Table 2) and the automatic parameter table for the selected module. See Table 3 for module 1.

The standard I/O equipment table and the automatic parameter table assigned to the selected module may be changed at any time by using the MI (Manual Interrupt) button on the TTY. The program upon sensing the MI button depressed will respond with:

NEXT

The operator should now define a parameter.
 See Table 4 for common manual parameters.
 See Table 5 for module 1 manual parameters.

2. Select autoloading parameter (AL*). See Table 5. The program will now autoloading the selected module to the BC and will respond with an appropriate message to informing the autoloading status.

TABLE 2. STANDARD I/O EQUIPMENT TABLE

MTI	E= 7, I = 3, M= B, F = 466, C= 0, U = 1.
MTO	E= 7, I = 3, M= B, F = 466, C= 0, U = 2.
LP	E = F I = 5

Common Automatic Parameters

Output Device = TTY

Output Level = Normal

Repetitions = Zero (Run test indefinite)

E = Equipment

I = Interrupt

M = Mode

F = Format

C = Converter

U = Unit

TABLE 3. MODULE 1 AUTOMATIC PARAMETERS

a.	Black fill disabled	(BF**=0)
b.	Character peak = A	(CP**=A)
c.	Document position = 500 mils	(DP**=500)
d.	Dwell time = 32 milliseconds	(DT**=32)
e.	Final coordinate = 50	(FC**=50)
f.	Font enable = ANSI	(FE**=FE00)
g.	Forward step = 1/3 inch or 336 mils	(FS**=336)
h.	Horizontal line thicken = disabled	(HT**=0)
i.	Initial read coordinate = 2A	(IC**=2A)
j.	Character image width = 22 columns	(IW**=22)
k.	Optical dump mode = reject	(OD**=R)
l.	Quantize level = 78	(QL**=78)
m.	Steps per page = 32	(SP**=32)
n.	Subtest number 5 optical dump	(ST**=5)
o.	Transport speed = 20 IPS	(TS**=20)
p.	Vertical line thicken = 30	(VT**=30)

* Buffer controller equipment code.

TABLE 4. COMMON MANUAL PARAMETERS

1. AL* = Autoload module to FR101
2. AP* = Automatic parameters
3. BD* = Buffer controller dump
4. BE* = Buffer controller equipment
5. BI* = Buffer controller interrupt
6. DR* = Data receive from controller
7. DS* = Data send to controller
8. EC* = Enable controller communication
(On-line mode)
9. EO* = Enable output
10. EX* = Execute test
11. ME* = Mag. tape equipment
12. MI* = Mag. tape interrupt
13. OM* = Output to mag. tape
14. OP* = Output to printer
15. OT* = Output to TTY
16. PD* = Printer drum
17. PE* = Printer equipment
18. PI* = Printer interrupt
19. RE* = Repetitions
20. SC* = Suppress communication (Off-line mode)
21. SM* = Select module
22. SO* = Suppress controller output
23. TC* = Mag. tape converter
24. TN* = Mag. tape unit number
25. XT* = Call SMM17 loader
26. LI* = List captured video data images from mag. tape
27. ID* = Dump captured video data images from mag. tape

* Buffer controller equipment code. For more detailed information see Table 6.

TABLE 5. MODULE 1 MANUAL PARAMETERS LOOK UP TABLE

1.	BF*	Black fill
2.	CP*	Character peak
3.	DP*	Document position
4.	DT*	Dwell time
5.	FC*	Final read coordinate
6.	FE*	Font enable
7.	FS*	Forward step
8.	HT*	Horizontal line thicken
9.	IC*	Initial read coordinate
10.	IW*	Image width
11.	OD*	Optical dump
12.	QL*	Quantize level
13.	RS*	Reverse step
14.	SP*	Steps per page
15.	ST*	Subtest select
16.	TS*	Transport speed
17.	VT*	Vertical line thicken
18.	ER*	Electronically read captured video data

NOTE

Refer to Table 7 for more detailed information.

*Buffer controller equipment code.

TABLE 6. COMMON MANUAL PARAMETERS SPECIFICATIONS

Step	Procedure
1.	AL* = Select Autoload mode (H=hardware, S=controlware).
2.	AP* = Upon selection, the program will set up the automatic parameters and returns to the monitor.
3.	BD* = Buffer controller core dump.
4.	BE* = Change BC equipment code (code range 1-F).
5.	BI* = Define BC interrupt line (range 1-F).
6.	DR* = Any section of the FR101 memory is to be dumped on the output device by defining FWA (first word address) and LWA (last word address).
7.	<p>DS* = Modify, insert, or delete any section of the FR101 memory. Upon selection, the program will type:</p> <p>ADR =</p> <p>Define BC core location address. Terminate with a (CR) define operand. Terminate operand with a comma (,) for sequential store and with a period (.) for single store. To terminate update enter "STOP (CR)" in response to ADR =</p>
8.	EC* = Upon selection, the program changes the mode of operation from off-line to on-line and the test is restarted.
9.	EØ* = The program sets the output level to normal and the test is restarted.
10.	EX* = Send to the FR101 module the parameter table and execute the test.
11.	ME* = Select mag. tape equipment code (range 1-F).
12.	MI* = Select mag. tape interrupt line (range 1-F).
13.	<p>OM* = Enter (CR) to output on mag. tape, the video data in a listing format. Enter font name or file name to dump on mag. tape the video data in auxiliary format.</p>
14.	OP* = The program selects the line printer for the output device.
15.	OT* = The program selects the TTY for the output device
16.	PD* = Select printer drum (O-OCR, S=standard).
17.	PE* = Select printer equipment code (range 1-F).
18.	PI* = Select printer interrupt line (range 1-F).

TABLE 6. COMMON MANUAL PARAMETERS SPECIFICATIONS (Cont'd)

Step	Procedure
19.	<p>RE* = Define repetitions (number range 0-65500₁₀). This parameter corresponds to the number of pages to be processed.</p>
20.	<p>SC* = Change output mode from on-line to off-line and restart the test.</p>
21.	<p>SM* = Select module.</p>
22.	<p>SO* = Change the output level so that all error messages will be suppressed and restart the test.</p>
23.	<p>TC* = Select mag. tape converter (range 0-F).</p>
24.	<p>TN* = TN* = Select mag. tape unit number (range 0-7).</p>
25.	<p>XT* = Call SMM17 loader from MTO.</p>
26.	<p style="text-align: center;">NOTE</p> <p>SELECTIVE STOP and SELECTIVE SKIP switches must be set prior to the selection of this parameter.</p>
	<p>LI* = Define file number in decimal. To dump all the files, enter 0 (zero). Dump on the selected output device the summary and the video data captured on mag. tape in a listing format.</p> <p style="text-align: center;">NOTE</p> <p>Select output device (OT or OP) before selecting LI* parameter.</p>
27.	<p>ID* = This parameter allows character images captured on mag. tape to be dumped in auxiliary tape format. Dump any one of the fonts captured. Dump only those characters which there is concern with. Here are some examples on how to dump these fonts.</p> <p>Example 1: (SINGLE FILE DUMP) ID* = File name (CR) Dump all the images contained in the request file.</p>
	<p style="text-align: center;">NOTE</p> <ol style="list-style-type: none"> 1. Refer to the typeout or printout for file name selection. The typeout or printout was given at the time the data was captured on mag. tape. 2. Select the output device prior to the selection of ID* parameter.

TABLE 6. COMMON MANUAL PARAMETERS SPECIFICATIONS (Cont'd)

Step	Procedure
	<p>Example 2: (MULTI FILES DUMP * SEQUENTIAL) ID* = File Name A, File Names (CR) Dump file name A, file name B, file name C, and file name D.</p> <p>Example 3: (MULTI FILE DUMP * RANDOM) ID* = File name B, file name D (CR) Skip file name A, dump file name B, skip file name C, dump file name D.</p> <p>Example 4: (SINGLE FILE DUMP * PARTIAL RANDOM) ID* = File name A (1,5,14,16) Looking at the Error Line below, character position 1, 5, 14, and 16 correspond to A, E, N, and P, respectively. The images A, E, N, and P will be displayed on selected output device.</p> <p>Example 5: (SINGLE FILE DUMP * PARTIAL SEQUENTIAL) ID* = File name B (5-7) Looking at the Error Line below, character position 5, 6, and 7, correspond to E, F, and G, respectively. The images E, F, and G, will be displayed on output device. ERR. LINE = ABCDEFGHIJKLMNOP CHARACTER = 0000000011111111 POSITION = 1234567890123456</p>

TABLE 7. MODULE 1 MANUAL PARAMETERS SPECIFICATIONS

1. BF* = Black fill 0 = Disable 1 = Enable.
2. CP* = Character peak reference (range 1-F).
3. DP* = Document position or document ready. Enter in mils the distance from the leading edge of the document to the center line of the first line to begin reading.
4. DT* = Dwell Time (millisecond range 1-65000₁₀).
This is a time delay performed after every step and upon sensing page near zero velocity.
5. FC* = Final read coordinate (range 1-FC).
6. FE* = Font enable for selection, refer to BC channel 5 output. For ANSI enter FE00.
7. FS* = Forward step (distance in mils from centerline to centerline).
8. HT* = Horizontal line thicken 0 = disable 1 = enable.
9. IC* = Initial read coordinate (range 6-FA).
10. IW* = Character image width (column count).
11. OD* = Optical dump mode respond with A, R, or S where:
A = Absolute dump
R = Dump on reject only
S = Dump on substitutions or rejects
If S is selected, the program will type REF LINE =
Define the reference line.
12. QL* = Quantize level (range 1-FF).
13. RS* = Reverse step (distance in mils).
14. SP* = Steps per page (steps to be performed on one page).
15. ST* = Subtest Select 1, 3, or 5 where:
1 = Forward Stepping Accuracy Test
3 = Troubleshooting Stepping Test
5 = Optical Dump Test
16. TS* = Transport speed; 5, 10, 20, 40, (IPS).
17. VT* = Vertical line thicken (range 1-3F).

* Buffer controller equipment code.

18. NR* = Number of rescans (range 1=65000).

This parameter specifies the number of times each line must be read.

19. ER* = Electronically read captured video data from the optics. After selection of this parameter perform the following steps:

- a. Set the 955 SIM/OPT switch to SIM.
- b. Press 955 READY switch.

The RX4/Module 1 Firmware is now circulating the character images captured from the optics during live read.

An EX* command will terminate Electronic Read and initiates live read.

- NOTE: 1. Character Data Ready are not verified during Electronic Read.
2. Character images captured from the optics and residing in the buffer controller, can be modified for study purposes while they are being read electronically. The procedure is as follows:

PROCEDURE TO MODIFY CHARACTER IMAGES.

SAMPLE OF VIDEO DATA DUMP

	Column
.....*****.....	1
.....*****.....	2
.....*****.....	3
.....*****.....	4
.....*****.....	5
.....*****.....	6
.....*****.....	7
.....*****.....	8
.....*****.....	9
.....*****.....	10
.....*****.....	11
.....*****.....	12
.....*****.....	13
.....*****.....	14
.....*****.....	15

CW=15 IA=BFD

BINARY DATA EQUIVALENT FOR THE IMAGE LISTED ABOVE

ADR	Data	Column
BFD	= 0003 1FFE FC01 0000	15
C01	= 0003 3FFE FC01 0000	14
C05	= 0003 3FFE FC01 0000	13
C09	= 0003 3C02 0001 0000	12
C0D	= 0003 1E02 0001 0000	11
C11	= 0003 0F02 0001 0000	10
C15	= 0003 07C2 0001 0000	9
C19	= 0003 03C2 0001 0000	8
C1D	= 0003 03C2 0001 0000	7
C21	= 0003 0702 0001 0000	6
C25	= 0003 0E02 0001 0000	5
C29	= 0003 1C02 0001 0000	4
C2D	= 0003 3E82 0001 0000	3
C31	= 0003 3FFE FC01 0000	2
C35	= 0003 3FFE FC01 0000	1

If we wish to delete the bit circled in column 3 and add the two bits in column 6, perform the following steps:

1. MANUAL INTERRUPT RX4
TTY PRINTS : NEXT
2. TYPE DS*
TTY prints
3. ADR = C2E (CR)
TTY prints
C2E = 3E02.
TTY prints
4. ADR = C22 (CR)
TTY prints
C22 = 07C2
TTY prints
5. ADR = STOP (CR)
TTY prints
NEXT

- NOTE:
1. Four computer words are required for every column of data.
 2. Only the most significant 14 bits of a computer word represent data, the least significant two bits (bit 2/0 and bit 2/1) is a code which specifies the position in the L/R (Load/Register) where the 14 bits of data must be loaded.

CONTROL CODE 3 = Upper 14 positions of L/R

2 = Upper middle 14 positions of L/R

1 = Lower middle 14 positions of L/R

0 = Lower 14 positions of L/R

3. Referring to step 3, the period (.) after 3E02 implies that the next change is not sequential. For sequential store use comma (,) instead of period (.).
4. Step 5 return control to RX-4 monitor.

D. OPERATING PROCEDURE

1. Forward Stepping Accuracy Test *

a. Select subtest number 1 (ST*=1).

Upon selection, the program will set up the following parameters for subtest number 1, section 1.

Section 1 Automatic Parameters

Initial read coordinate	= 2A
Terminal read coordinate	= 50
Transport speed	= 20 IPS
Step length	= 1/3 inch
Steps per page	= 25
Document position	= 500 mils
Quantize level	= 78
Font enable	= ANSI
Pages to be processed	= 40
Dwell time	= 50 milliseconds
Tolerance	= 30 mils

b. Place at least 40 documents in the hopper.

c. Verify that on maintenance panel OPTICAL/SYM switch is set to OPTICAL.

d. On the Operator's Control Panel press READY switch. Section 1 is now running. Section 1 will perform 1000 1/3-inch steps at 20 IPS. Upon completion, the RX4/1700 program will inform the operator whether or not the test is accepted, and sets up the following parameters to run Section 2.

Section 2 Automatic Parameters

Initial read coordinate	= 2A
Terminal read coordinate	= 50
Transport speed	= 40 IPS
Step length	= 1 inch
Steps per page	= 10
Document position	= 500 mils
Quantize level	= 78
Font enable	= ANSI
Pages to be processed	= 40
Dwell time	= 50
Tolerance	= 42 mils

* Use document number 60217511A, 60217512A, or 60217513A.

The operator should now do the following:

- 1) Place at least 40 documents in the hopper.
- 2) On Operator's Control Panel press READY switch.

Section 2 is now running. Section 2 will perform 400/1-inch steps at 40 IPS. Upon completion, the RX4/1700 will inform the operator whether or not the test is accepted.

Theory of Operation for Section 1

The RX4 controlware performs a document ready and positions the first line on the document at servo data 16+3. A 1/3-inch step (336 mils) is now performed at a speed of 20 IPS. The controlware scans between coordinate 2A and 50 capturing the first four characters and compares it to the average servo data obtained on the first line. If the difference is greater than 30 mils, the controlware will inform the RX4/1700 monitor that a stepping error has been detected and transfer the following information to the RX4/1700 monitor:

- 1) Page count
- 2) Line count
- 3) Servo data average of the first line
- 4) Servo data average after stepping
- 5) Transport coordinates

The RX4/1700 monitor processes the page count and line count by transferring their respective values to a print picture, analyzes the transport coordinates and determines transport drift. A forward (+) drift of a 3-conveyor count is accepted and a reverse (-) drift of 1-conveyor count is also accepted. If there is any drift the program transfers the conveyor count to the print picture. By analyzing the servo data, the program determines if the amount of error is greater than 48 mils ($X|X > 48$ mils). This is considered a fatal error and the test will be rejected. The program will display the following message:

SECTION 1 FAILED

If the error is greater than 30 mils but less than or equal to 48 mils, the program will register the error incrementing a counter. Upon completion of Section 1 the program will monitor this counter. If the total number of errors is greater than 5 percent, the program will display the following message:

SECTION 1 FAILED

If the total number of errors is less than or equal to 5 percent, the program displays the following message:

SECTION 1 PASSED

Section 2 Theory of Operation

The theory of operation described in Section 1 applies also to Section 2. The only difference is that the tolerance is greater and the number of steps is 400 instead of 1000.

Upon completion of Section 2, the program will display one of the following messages:

SECTION 2 PASSED

SECTION 2 FAILED

2. Troubleshooting Stepping Test (Subtest #3)

The following parameters are required:

- a. Transport speed (TS*)
- b. Forward step length (FS*)
- c. Dwell time (DT*)
- d. Number of steps (RE*)

The above parameters are already set to automatic (see Table 5), however change any of them as desired.

Perform the following steps:

- a. Execute test (EX*)
- b. On Operators Control Panel press READY switch to begin test.

3. Optical Dump Test (Subtest #5)

The following parameters are required:

- a. Initial read coordinate (IC*)
- b. Final read coordinate (FC*)
- c. Forward step length (FS*)
- d. Document position (DP*)
- e. Quantize level (QL*)
- f. Font enable (FE*)
- g. Steps per page (SP*)
- h. Dwell time (DT*)
- i. Number of pages (RE*)
- j. Transport speed (TS*)
- k. Optical dump mode (OD*)
- l. Character width (CW*)

The preceding parameters are already set to automatic (see Table 5); change any of them as desired.

Perform the following steps:

- a. Execute test (EX*)
- b. Place documents in the hopper
- c. On Operators Control Panel press READY switch

II. MESSAGES

A. NORMAL MESSAGES

1. Begin RX4 1700/FR101/955 Transport Test IA=XXX (REV X.X).
2. NEXT

The RX4 monitor has control and is awaiting on an input from TTY.

3. THE BC IS LOADED

The selected module has been loaded to the FR101 and the checksums are correct.

4. END OF TEST

B. COMMON ERROR MESSAGES

1. ONA (option not available)
2. MT DOES NOT RESPOND

The program received an external reject while trying to connect the MT. Verify MT equipment code and unit number.

3. MT STATUS ERROR

The program has detected a parity error.

4. ILLEGAL AUX. TAPE

5. BC/X FAILED TO REPLY ON FUNCTION RELOAD BC/X

The 1700 program is unable to communicate to BC/X. The program requests that BC/X be reloaded.

6. CHECKSUM ERROR

The checksum computed on the module while being loaded to the FR101 is not equal to the checksum computed during the transfer of the module from the FR101 to the 1700 program.

7. INCORRECT REPLY FROM BC/X RELOAD BC/X

The module residing in BC/X has lost control. It is not sending the correct reply to the 1700 program.

C. MODULE 1 ERROR MESSAGES

1. Subtest Number 1 Normal and Error Messages

SECTION 1 PASSED

The RX4 controlware has performed the 1000 1/3-inch steps and the number of steps in error does not exceed 5 percent.

SECTION 1 FAILED

Either a fatal error just occurred or the number of steps in error at the completion of the test is not within 5 percent. Fatal error ($X|X > 48$ mils).

SECTION 2 PASSED

The RX4 controlware has performed the 400/1-inch steps and the total number of steps in error is within 5 percent.

SECTION 2 FAILED

Either a fatal error just occurred or the number of steps in error at the completion of Section 2 is not within 5 percent. Fatal error = ($X|X > 60$ mils).

EXPSD---ACTSD---MILS OFF--DRIFT-LC--PC--EID

XX X X + XX + X XX XX XXX

The preceding message is displayed whenever a stepping error is detected.

EXPSD:

Average servo data obtained from the first line of the document.

ACTSD:

Average servo data obtained after the step was performed.

MILS OFF

Difference between the EXPSD and ACTSD multiplied by 6.

1 light pipe = 6 mils.

+ XXX indicates overstepping - XXX indicates understepping.

DRIFT:

Number of conveyor counts which the transport moved from the time the Stop Motion command was executed until after the 50-millisecond dwell time.

Drift of +3 and -1 is accepted.

+X indicates a forward drift greater than 3.

-X indicates a reverse drift greater than $|-1|$.

LC: Line count

PC: Page count

EID: Error identification

FSE = Forward stepping error

TLD = Topless data

BLD = Bottomless data

2. Subtest Number 5 Error Messages

a. VIDEO DATA OUT OF SEQUENCE EXP. 3.2.1.0 Rec W.X.Y.Z

As each column of video data comes out of the Dump register (1 column = 4 words) the first word should have a control code of 3 (bit 14 and 15 set), the second word should have a 2 (bit 14 set), the third word should have a 1 (bit 15 set), and the fourth word should have a 0 (bit 14 + 15 clear).

The 1700 program prior to dumping a column of data will monitor these codes and if it detects that they are out of sequence, it will display the above message.

b. MAXIMUM CHARACTER Width Exceeded (37 columns)

The program has detected that the width of an image (black data only) is greater than 37 columns. This exceeds the size of the buffer which holds the black video data. Change the optical dump mode to Absolute (OD*A) in order to obtain a video data dump. In Absolute mode the program dumps one column at a time without looking for transition.

NOTE

1. PC (page count) refers to the document count in the secondary packet.
 2. The symbol @ indicates character reject.
 3. Character substitutions are not detected in this mode.
 4. CW (character width) is the number of black columns the character image is made up of.
 5. IA (initial address) refers to the buffer controller initial address of the image displayed.
 6. The rejected character is always preceded by the numbers 1 through 56, which correspond to the light pipes.
 7. Anything less than four columns of black data will be considered as dirt by the RX4.
 8. Character images have been inverted for easier reading.
- j. Magnetic Tape Video Data Dump (Listing Format)

The purpose of this option is to save time. On most systems video data dumps are performed on TTY which takes a very long time. If a line printer should be available elsewhere in the plant, video data could then be captured on magnetic tape and listed on the line printer available.

NOTE:

1. Data is written on MT in the format described in the previous figures.
 2. Data is written on MT in BCD.
 3. Use manual parameter LI* to dump video data from magnetic tape.
 4. A tape mark is written at the end of each dump.
- k. Magnetic Tape Video Data Dump (Auxiliary Tape Format)

The following summary will be displayed on the line printer if one is available; otherwise the summary will be displayed on the TTY.

Example:

```
PC = XXXX      LC = XXXX  FN = FONT NAMED
REF.  LINE = ABCD . . . (If in Reference mode)
ERR.  LINE =
VOLT  LINE = FXFF
SERVO      = 1X11
          DATA = 7X67
```

NOTE:

1. Data is written on magnetic tape in 466 binary.
2. Density, whichever is selected.

3. "Font Name" is the name which is defined.
The program assigns the letters A-Z in order to make the name unique for every dump performed.
4. Character images recorded on magnetic tape in auxiliary tape format can be listed by using manual parameter ID*.
5. The first record of every dump on magnetic tape consists of Name Mask (sum of the ASCII codes describing the name) reference line ASCII codes if in Reference mode. If in Reject or Absolute mode, the reference line consists of the ASCII codes generated by the 955 Reader.
6. All the video data corresponding to the character read will be recorded on magnetic tape. The program does not attempt to separate the bad images from the good ones, since this could affect the end result when the images are read electronically with the RX3 module 1.
7. A tape mark will be written at the end of each dump.

1. Handprint Optical Dump Specifications

1) Restrictions

- Optical dump in Reject mode is illegal.
- The program will not handle leading ANSI characters.
- A rescan parameter is available. However, this parameter allows the same line to be read any number of times. It does not allow the errors occurred in the first scan to be corrected.

The above restrictions are necessary if the program is to be effective. The more sophisticated the program, the less useful it becomes. In other words, if the amount of core storage available for capturing video data is too small, the diagnostic would become obsolete.

2) Theory of Operation

a) Absolute Mode

In Absolute mode the program upon sensing the READY switch depressed will bring a document to the read zone and position it 1 inch past read zone plus the amount of mils specified with the document position parameter. It scans between the specified read coordinates and reports to the operator the information obtained from the scan. (Refer to the preceding figures.)

If a forward step has been specified (FS*), the program performs the step ignoring high and low characters and once again reports the information to the operator.

b) Reference Mode

In Reference mode the program upon sensing the READY switch depressed, brings a document to the read zone and positions it 1 inch past read zone sensor plus the amount of mils. Specified with the document position parameter. It scans only the character data. At this point the program monitors the first 3-character data ready words for high and low signals. If both high and low are detected, the program will reject this document and bring up a new one. If more than one high signal is detected, the program performs a 64 mils reverse step. If more than one low signal is detected, the program performs a 64 mils forward step. Once again, the program scans between the read coordinates and checks for high and low signals. If within six attempts the program does not succeed to get rid of high or low signals, the document will be rejected.

Upon succeeding in positioning the line, the program scans the line one more time capturing character data and video data.

Character data is now analyzed and compared to the reference line. If rejects or substitutions are detected, the program will report the information to the operator. (Refer to the preceding figures.)

If more lines must be read from the same document, the program will perform the forward step specified with the FS* parameter, check for high or low signals, and adjust the line if more than one signal is up, and return one again to capture character data and video data.

Hand Print Operating Procedure to Simulate Controlware

1. Parameters for Initial Scan

OD*=S (Optical dump = Reference mode)
FE*=4 (Enable hand print font line)
HT*=0 (Disable horizontal line thicken)
VT*=30 (Vertical line thicken = 30)
QL*=78 (Quantize level = 78)
BF*=0 (Disable black fill)
DP*= (Total mils (in decimal) from leading edge of document to the center
of the line you wish to read)
FS*= (Forward step length (total mils in decimal))
NOTE: FS*=0 for stationary read.
SP*= (Steps per page or number of lines that you wish to read)
EX* Execute test
Press 955 READY switch

If no substitutions or rejects are detected, change the following parameters to perform the first rescan.

2. First Rescan

VT*=21 (Vertical line thicken = 21)
BF*=1 (Enable black fill)
EX* (Execute test)
Press 955 READY switch

If no substitutions or rejects are detected after the first rescan, change the following parameters to perform the second rescan.

3. Second Rescan

QL*=80 (Quantize level = 80)
BF*=0 (Disable black fill)
EX* (Execute test)
Press 955 READY switch

If no substitutions or rejects are detected after the second rescan, change the following parameters to perform the third and final rescan.

4. Third Rescan

VT*=12 (Vertical line thicken = 12)
BF*=1 (Enable black fill)
EX* (Execute test)
Press 955 READY switch

NOTE: If no errors (substitutions or rejects) are detected during the three rescans, hand print errors were possibly caused by skew in the document.

To test this theory perform the following steps:

FS*=0 (Stationary read)

EX* (Execute test)

Press 955 READY switch

Manually move the document as the program is performing stationary read.

NOTE: Skew of ± 1.5 degree is normal.

Sample of Error Printout on the Forward Stepping Accuracy Test

EXPSD	ACTSD	MILS OFF	DRIFT	LC	PC	EID
15	2	+ 78		1	1	FSE
15	4	+ 66		2	1	FSE
15	5	+ 60		3	1	FSE
15	6	+ 54		4	1	FSE
15	5	+ 60		5	1	FSE
15	5	+ 60		6	1	FSE
15	6	+ 54		7	1	FSE
15	5	+ 60		8	1	FSE
15	7	+ 48		9	1	FSE
15	4	+ 66		10	1	FSE
15	4	+ 66		11	1	FSE
15	4	+ 66		12	1	FSE
15	3	+ 72		13	1	FSE
15	4	+ 66		14	1	FSE
15	5	+ 60		15	1	FSE
15	4	+ 66		16	1	FSE
15	6	+ 54		17	1	FSE
15	3	+ 72		18	1	FSE
15	5	+ 60		19	1	FSE
15	6	+ 54		20	1	FSE
15	6	+ 54		21	1	FSE
15	5	+ 60		22	1	FSE
15	7	+ 48		23	1	FSE
15	5	+ 60		24	1	FSE
15	6	+ 54		25	1	FSE
18	3	+ 90		1	2	FSE
18	8	+ 60		2	2	FSE
18	9	+ 54		3	2	FSE
18	9	+ 54		4	2	FSE
18	8	+ 60		5	2	FSE

NOTE

1. The above error printout was forced by defining a forward step of 400 mils instead of 336 mils (1/3 inch) which is the actual spacing between lines on the document.
2. No values are listed under drift, because it was within tolerance.

2. Subtest Number 5 Optical Dump

a. Absolute Mode

RX4 module 1, upon sensing the READY switch depressed, will initiate 40 IPS speed and wait for a document to be sensed at read zone. If a document is already covering read zone sensor at the time the READY switch is depressed, the program will bypass it and wait for a new one. As soon as a document is sensed at read zone, the program will allow the document to move 1 inch (distance from read zone sensor to read area) plus the number of mils specified with the document position parameter (DP*).

Since this is an absolute dump, the program will not attempt to line locate. The program will now perform a zero mirror and position the mirror to the initial read coordinate (IC*). Character peak reference, font lines, and read will now be enabled.

Due to the high frequency in which the video data comes out of the Dump register, the program will not terminate the scan when the mirror reaches the final read coordinate (FC*). This is due to the fact that having to capture video data, character data, servo data, and character voltage, the program cannot monitor the mirror encoder without losing video data. Therefore, the scan will be terminated, based on a video data word count.

The formula to compute the video data word count is:

$$\begin{aligned} & ((FC - IC)/2) \quad (IW \times 4) \\ FC & = \text{Final read coordinate} \\ IC & = \text{Initial read coordinate} \\ IW & = \text{Image width (column count)} \end{aligned}$$

EXAMPLE:

$$IC = 2A, \quad FC = 50, \quad IW = 22$$

Converting IC and FC from hexadecimal to decimal;

$$IC = 42 \quad FC = 80$$

Using the formula

$$\begin{aligned} & ((80-42)/2) (22 \times 4) \\ & = 38/2 \times 88 \\ & = 19 \times 88 \\ & = 1672 \end{aligned}$$

After 1672 video data words have been taken, the program will drop Scan Mirror Forward command and execute a Stop Mirror command. The firmware will now inform the 1700 program that the video data is ready for output. The 1700 program will request page count, line count, line read, servo data, and character voltage and displays them on the output device.

The 1700 program will now request the BC to transfer one column of video data (four words), checks the four words for proper control codes sequence and if they are in sequence, display the column of data. This process will continue until 1672 words or 418 columns of video data have been listed. The 1700 program will now instruct the BC program to continue with the test.

The BC program will now monitor the forward step (FS*) parameter. If it is set to zero, it will perform another scan on the same line. This is known as stationary read. If the step is not set to zero, the program will perform the step specified (FS*) before executing the next scan. This process continues until the specified number of steps have been executed on a single document. After the requested number of steps have been executed, a new document will be brought into the read area and the test starts over again.

NOTE

Stepping in Absolute mode may cause either bottomless or topless. This is because the program in Absolute mode does not adjust the step using servo data, it actually performs an absolute step without any adjustments whatsoever. This mode will allow you to test how accurate the transport can step without using servo data.

b. Reject of Reference Mode

The BC program, upon sensing the READY switch depressed, will initiate a 40 IPS speed and wait for a document to be sensed at read zone. If a document is already covering read zone sensor at the time the READY switch is depressed, the program will ignore it. As soon as a document is sensed at read zone sensor, the program will allow the document to move 1 inch (distance from read zone sensor to read area) plus the number of mils specified with the document position parameter. The program will now line locate and position the line at servo data $16 + \frac{3}{2}$ ($16 = \text{center}$). The mirror will now be positioned at the initial read coordinate. Character peak reference, font lines, and

read are now enabled. The program will now begin to capture video data, character data, servo data, and character voltage. When the computed number of video data words have been captured, the program will drop the Scan Forward Mirror command and bring up Stop Mirror command. If this is a dump on reject only, the program will analyze the character data, and if any rejects are detected, the program informs the 1700 program. If this is a dump on Reference mode, the characters generated by the reader are compared against the reference line and if any substitutions are detected, the program informs the 1700. The 1700 program, upon notification that either rejects or substitutions have been detected, will request the BC program to transfer page count, line count, character data, character voltage, and servo data and displays all the information on the selected output device. The 1700 program will now begin to request 1 column of video data (four words) at a time. Checks the four words for proper control code sequence (EXP. = 3.2.1.0) and if they are found to be out of sequence, the operator will be informed, the program checks to see if this is a clear column (all 56 bits clear). If it is a clear column, a clear column count will be incremented by 1 and a test is performed to determine if a black to white transition just occurred. If no transition occurred, more video data will be requested. If the column of data contains black data, the program transfers the four words to the video data buffer and tests for an overflow (37 columns of black). If an overflow is detected, the program informs the operator and no other action is taken.

Upon a transition from white to black, the program determines if the image residing in the video data buffer must be listed. The program will list the image if so determined and checks to see if there are any more to be listed.

If there are no more images to be listed, the program instructs the BC program to continue with the test. The BC program will now monitor the forward step parameter and if set to zero will rescan the same line (stationary read); otherwise the program will test to see if the specified number of steps have been performed on this page. If not, the program performs the specified step making the necessary adjustments (by using servo data) so that the next line will be as close as possible in the center of the optic. When the specified number of steps have been executed on a page, a new page is brought in the read area and the test is repeated all over again.

SC/1700/FR101/FR113 INTERFACE TEST

(BC3A59 Test No. 59)

(Non-Supported Class III Test)

I. OPERATING PROCEDURE

A. RESTRICTIONS

1. Requires an 8K 1700 system with a 608 or 609 MT and a TTY.
2. The diagnostic interfaces to SMM17 only for loading.
3. BC interrupt line must be on 4 or 7.

B. LOADING PROCEDURE

Manually enter the appropriate bootstrap (see SMM17 Reference Manual) starting at address \$1FC0.

1. Set SELECTIVE STOP and SELECTIVE SKIP switches.
2. Set P = 1FC0 and run.
3. First halt, run.
4. Second halt.
 - a. Computer halts with A=3080, Q=0381.
 - b. Clear SELECTIVE SKIP switch.
 - c. Add 30 to A (30B0).
 - d. Run.
5. TTY prints.

SMM17 ED. 3.0
BUILD TEST LIST
6. Third halt.
 - a. Set A = 5901 (BC3 Test Number 59).
 - b. Set Q = 0381.
 - c. Run.
7. Fourth halt.
 - a. Clear A register.
 - b. Run.

8. TTY prints BC3 internal printout message.

C. BC3 TEST FUNCTIONS

1. Section 1 Functions 'Control Lines Test'
 - a. Director 1 write, expect reply.
 - b. Director 2 read, expect reply.
 - c. Director 2 write, expect reply.
 - d. Director 1 write, expect internal reject.
2. Section 2 Functions 'Autoload Test'
 - a. Verify Autoload status bit.
 - b. Verify that it is possible to autoload 4K words to the BC with no hang-ups.
 - c. Verify data autoloading to the BC.
 - d. Verify data received from the BC.
3. Section 3 Functions 'Status + Interrupts Test'
 - a. Program Protect Switch Status test.
 - b. Director 1 Status test.
 - c. Director 2 Status test.
 - d. Data Interrupt + Status test.
 - e. EOP Interrupt + Status test.
 - f. Alarm Interrupt + Status test.
 - g. Lost Data Interrupt + Status test.
4. Section 4 Functions 'Directors + Functions Test'
 - a. Starting with Director 2 through 7, verify that the coupler decodes the correct director.
 - b. Verify that the BC receives the correct function with each director.
5. Section 5 Functions 'Block Transfer ECO Test'
 - a. Starting with one word and continuing up to 4K, verify that the BC always accepts and transmits the correct number of words.

SECTION 1. BC CONTROL LINES TEST

NOTE: To bypass this section set the SELECTIVE SKIP switch on the 1700 Console.

TTY types: Section 1 Running.

TTY types: Set BC Equipment to X.

Enter CR after setting the BC equipment switch to X.

Functions performed in Section 1:

1. Director 1 Write, Expect Reply
2. Director 2 Read, Expect Reply
3. Director 2 Write, Expect Reply
4. Director 1 Write E ≠ X Expect Internal Reject
5. Director 1 Write W ≠ 0 Expect Internal Reject

If the responses to the functions listed above are correct, the program will request that the BC equipment number be changed to a different combination and the test repeated.

Combinations 2, 4, 8, F, and A are tested:

At the completion of the section the program types: END OF SECTION 1.

Section 1 Error Message

EXP = AA REC=BB F=X D=Y E=Z W=XX WHERE

EXP = AA

AA is the expected response on the function performed. AA takes the form of RE (Reply), IR (Internal Reject), or ER (External Reject).

REC = BB

BB is the actual response received. BB takes the form of RE (Reply), IR (Internal Reject), or ER (External Reject).

F = X

X is the function performed. X takes the value of R (Read) or W (Write).

D = Y

Y is the director used in the function.

E = Z

Z is the equipment number used in the function. Z = 2, 4, 8, F, or A.

W = XX

XX is the converter number used in the function. XX = 0-10

After typing the above error message, the program types ACTION (C, R) =.

The operator should now select C to continue or R to repeat the same function.

NOTE: If an R is entered in response to ACTION(C, R)= the program will re-execute the same function for as long as the function fails. In other words, it will repeat on error only. To repeat the same function unconditionally, set the SELECTIVE SKIP switch on the computer before entering R. To exit from this unconditional loop, clear the SELECTIVE SKIP switch. The program will now start processing the next function.

SECTION 2 AUTOLOAD TEST

TTY types: Section 2 Running.

Clear SKIP switch if it was set to skip Section 1.

Section 2 Error Messages

AUT BIT NOT SET

ACTION (C, R)=

Following a DIR 9 write, the autoload status bit was not a "1".

Enter R in response to ACTION (C, R)=. The program will perform a DIR 9 continually until the problem is solved. The program will inform the operator by ringing the TTY bell when it receives the proper status response.

AUT HANG UP. WC=XXXX (XXXX Range = 1 - 1000₁₆)

EXP=RE REC=IR F=W D=8 E=A W=0

During the 4K Autoload Test, the program received an Internal Reject on a Director 8 at WC (word count) XXXX.

Since no other section can be processed unless the autoload works properly, enter R in response to ACTION (C, R)=.

The program will perform the autoload continually until it succeeds to perform a 4K autoload.

AUT. BIT NOT CLR

ACTION (C, R)=

Following a Director 1 Write (Master Clear BC), the autoload status bit was not a "0". Enter R in response to ACTION (C, R)=.

AUTOLOAD TO BC FAILED

ACTION (C, R)=

The data autoloaded to the BC is incorrect.

Enter C in response to ACTION (C, R)=

TTY types: Data=.

Define the data to be autoloaded to the BC as four hexadecimal digits or less, terminate DATA selection with a (CR).

The program will now continually autoloading the data defined until the operator presses the TTY manual interrupt button. The program upon sensing the TTY interrupt will request a new data word.

To terminate, enter STOP in response to DATA=.

BLOCK TRANSFER FAILED

ACTION (C, R)=

The word count received from the BC is incorrect.

Section 5 will check Data Block Transfer Logic. We cannot jump to Section 5 at this time because D1 and D2 status and interrupts have not been checked yet. Enter C in response to:

ACTION (C, R)=, after the status is checked the cause of Data Block Transfer Failure will be determined.

INCORRECT DATA FROM BC EXP=XXXX REC=YYYY

The data coming from the BC is incorrect.

If no errors are detected during the autoloading test, the TTY types END OF SECTION 2.

SECTION 3 DIRECTOR 1 AND DIRECTOR 2 STATUS CHECK

DATA, EOP, ALARM AND LOST DATA INTERRUPTS CHECK

NOTE: BC interrupt line must be on interrupt line 4 or 7.

TTY types: Section 3 Running.

Section 3 Error Messages for D1 and D2 Status

EXP BIT 2/X SET DY

REC BIT 2/X CLR DY

ACTION (C, R)=

OR

EXP BIT 2/X CLR DY

REC BIT 2/X SET DY

ACTION (C, R)=

Where X is the bit being tested and Y the director.

See tables below for D1 and D2 status bits specifications.

If an R is entered in response to ACTION (C, R)=, the program will set and clear continually the status bit in error. Should the CE correct the status bit in error, the program will ring the TTY bell, and proceed to test next status bit.

Interrupt Failure Error Messages

1. NO DATA INTERRUPT
2. NO EOP INTERRUPT
3. NO ALARM INTERRUPT
4. NO LOST DATA INTERRUPT

NOTE: Additional information will be displayed if the status is incorrect.

Expected status before BC generates Data interrupt.

READY (Bit 2/0 set)

BUSY (Bit 2/1 set)

Expect status after BC generates Data interrupt:

READY (Bit 2/0 set)

BUSY (Bit 2/1 set)

INT. (Bit 2/2 set)

DATA (Bit 2/3 set)

Expected status before BC generates EOP interrupt:

READY (Bit 2/0 set)

BUSY (Bit 2/1 set)

Expected status after BC generates EOP interrupt:

READY (Bit 2/0 set)

INT. (Bit 2/2 set)

EOP (Bit 2/4 set)

Expected status before BC generates Alarm interrupt:

READY (Bit 2/0 set)
BUSY (Bit 2/1 set)

Expected status after BC generates Alarm interrupt:

READY (Bit 2/0 set)
BUSY (Bit 2/1 set)
INT. (Bit 2/2 set)
ALARM (Bit 2/5 set)

Expected status before BC generates Lost Data interrupt:

READY (Bit 2/0 set)
BUSY (Bit 2/1 set)

Expected status after BC generates Lost Data interrupt:

READY (Bit 2/0 set)
BUSY (Bit 2/1 set)
INT. (Bit 2/2 set)
ALARM (Bit 2/5 set)
LOST DATA (Bit 2/6 set)

DIRECTOR 1 STATUS

CHANNEL 0

<u>Bit Position</u>	<u>Status Function</u>
2/0	READY
2/1	BUSY
2/2	INTERRUPT
2/3	DATA
2/4	EOP (END OF OPERATION)
2/5	ALARM
2/6	LOST DATA
2/7	PP (PROGRAM PROTECT)
2/8	AUTOLOAD
2/9	LINE DELETE
2/10	CHARACTER REJECT
2/11	LLF (LINE LOCATE FAILURE)
2/12	EOF (END OF FILE)
2/13	TRANSPORT STATUS FAULT
2/14	DOCUMENT NO SORT
2/15	DATA SKEWED

DIRECTOR 2 STATUS

CHANNEL 1

Bit Position

Status Function

2/0 - 2/7	MIRROR POSITION STATUS
2/8	UNUSED
2/9	UNUSED
2/10	DOCUMENT LENGTH FAULT
2/11	PARAMETER FAULT
2/12	MIRROR STOP FAULT
2/13	COORDINATE FAULT
2/14	MIRROR VELOCITY FAULT
2/15	SCAN GATE

SECTION 4

Starting with Director 2 through 7 the BC3 program will perform two functions for every director.

Example:

Function number 1 = Director 2, A = 0000

Function number 2 = Director 2, A = FFF8

Theory of Operation

The BC upon receiving the Director function, transfers back to the BC3 monitor the actual director decoded by the coupler and the function. BC3 monitor will verify that the coupler decoded the correct director and that the correct function was received by the BC.

Error Messages

BC DECODE WRONG DIRECTOR EXP=DX REC=DY

Where DX is the expected director and DY is the director actually decoded by the coupler.

BC RECEIVED INCORRECT FUNCTION ON DX EXP=XXXX REC=YYYY

BC3 monitor after it displays one of the above error messages requests operator's action by typing:

ACTION(C, R)= Where

C = Continue

R = Repeat on error only

NOTE: To repeat the same Director function unconditionally, set the SELECTIVE SKIP switch before entering R in response to ACTION(C, R).

After Directors 2 through 7 have been verified, the BC3 monitor types END OF SECTION 4.

SECTION 5 ECO TEST

Data Block transfer to and from the BC, starting with a data block of one word up to 4000. Each time the program verifies that the BC accepts only as many words as instructed to, and transfers back the same number.

Error Messages

BC HANG UP ON DATA INPUT

During a Data Block transfer of X words ($x \mid 1 \leq x \leq 4000_{10}$) to the BC, the BC failed to generate EOP interrupt.

BLOCK TRANSFER FAILED

FROM 1700 TO BC

EXP=XXXX ACT=YYYY

The BC accepted more or less than XXXX data words than instructed. XXXX is the number of words the BC should have accepted before generating an EOP interrupt. YYYY is the number of words the BC actually accepted.

LOST DATA STATUS

FROM 1700 TO BC

EXP=XXXX ACT=YYYY

During a Data Block transfer of x words from the 1700 to the BC, the BC generated Lost Data status.

This is a fatal error. Once the 1700 initiates a data transfer to the BC it does not terminate data output to the BC unless the BC generates an EOP interrupt or the 1700 detects timeout on data transfer.

ILLEGAL LOST DATA STATUS

FROM 1700 TO BC

EXP=XXXX ACT=YYYY

The BC accepted as many words as instructed to, yet the BC generated a Lost Data Status condition.

NOTE: Under normal conditions, that is: following a successful Data Block transfer, the condition bit in the BC should be true, if it is false the BC program will generate a Lost Data status.

BC HANG UP ON DATA OUTPUT

During a Data Block transfer of x words from the BC to the 1700, the BC has failed to terminate the data transfer with an EOP interrupt. Data transfer has been terminated by the 1700 upon detecting timeout on data transfer.

BLOCK TRANSFER FAILED

FROM BC TO 1700

EXP=XXXX ACT=YYYY

The BC has failed to transfer the correct number of words.

NOTE: On any one of the above messages, the BC3 types:

ACTION (C, R) = Where

C = Continue

R = Repeat on error only

NOTE: To repeat the same function unconditionally, set the SELECTIVE SKIP switch before entering R in response to ACTION(C, R). To exit from this unconditional loop clear the SELECTIVE SKIP switch.

If no errors are detected in the Block Transfer ECO Test, the BC3 will type:

END OF SECTION 5

END OF TEST

ACTION(C, R)=

Enter R if the entire test is to be re-run.

COMMENT SHEET

MANUAL TITLE CONTROL DATA® 1700 SYSTEM MAINTENANCE MONITOR (SMM17

Volume 2 Reference Manual

PUBLICATION NO. 60182000 REVISION L

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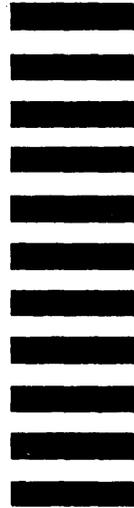
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