# BUS INTERFACE PRODUCTS CHASSIS PRODUCTS



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SILKSCREEN



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#### 1.0 Introduction

This manual describes the operation of the Bit 3 Model 406 PC/AT-VMEbus Adaptor. The Adaptor consists of one PC/AT circuit board and one 6U VMEbus board. The two cards are connected with a round EMIshielded cable.

This chapter gives the specifications of the Adaptor boards and a general description of their features. Chapters Two and Three give detailed descriptions of the jumpering required to use the Adaptor correctly. Chapter Four is an installation guide. Chapter Five describes the control registers on the Adaptor.

# 1.1 Board Specifications

Bus Communication Specifics:

The Adaptor permits the PC/AT to act as a bus master on the VME bus, allowing memory references to it to pass to the VMEbus chassis. A dual-port memory option allows VMEbus masters to pass data to and from the PC/AT. Addressing from the PC/AT to the VMEbus is A32, A24, or A16; data accesses are D16 or D8. Addressing from the VMEbus to optional dual-port memory is A32 or A24; data accesses are D32, D16, or D8.

Bus Arbitration: Release-On-Request (ROR)

Access Times and Data Rates:

PC/AT read/write access to remote RAM: 2.0 usec PC/AT read/write access to dual-port RAM: 1.6 usec VMEbus read/write access to dual-port RAM: 500 nsec

Interrupt Passing:

The Adaptor can pass any of seven VMEbus interrupts (IRQ7-IRQ1) to the PC/AT chassis. The PC/AT is also able at any time to pass a programmed interrupt to the VMEbus chassis by a write to an Adaptor I/O register.

Read-Modify-Write:

Read-modify-write is simulated by a bus-lock control bit in an Adaptor control register.

Interrupt Acknowledgement:

PC/AT acknowledgement of VMEbus interrupts (and VMEbus vector passing) is provided through an Adaptor card control register.

Power Requirements:

The VMEbus Adaptor card draws 3.5 A at 5 V. The PC/AT Adaptor card draws 3.0 A at 5 V.

#### Environment:

Temperature:	0	to	60 C operating; -15 to 85 C storage
Humidity:	0	to	90% non-condensing

Adaptor Functions

#### 1.2 Operation

The Bit 3 PC/AT to VMEbus Adaptor enables an IBM PC/AT device to directly address resources on a VMEbus system as though they were local to the PC/AT. It allows the user the ability to pass blocks of data, I/O commands, and even interrupts between the two systems. The Adaptor can also act as the lone bus controller in a remote VMEbus chassis -- in effect, extending a single PC/AT device across two different backplanes.

Direct address mapping (direct mode) permits a PC/AT system to address the other chassis as if it were local memory, via randomaccess memory reads or writes. There is no need to pass data through intermediate software drivers, and the PC/AT processor can even execute code from memory on the VMEbus system. The Adaptor provides a flexible interface permitting random-access eight-bit and sixteenbit transfers to a remote system at speeds comparable to reads and writes to local memory.

As an alternative, paged memory accesses (page mode) are also possible. A page register on the VMEbus Adaptor card combines its contents with the lower sixteen address bits on the PC/AT bus to allow access to all four gigabytes of VMEbus memory through a much smaller PC/AT address window.

VMEbus I/O can be directly addressed by a PC/AT processor so that memory reads or writes within an Adaptor window (combined with an I/O address modifier) are translated into I/O operations on the VMEbus.

Finally, the two systems can be linked with a dual-port memory -- RAM available to both systems. Accessing this memory from either bus does not use bandwidth on the other bus, and random accesses to this memory appear to either system as local reads and writes.

Interrupts can be passed between the two chassis. Any one of the seven VMEbus interrupts may be passed to a PC/AT system where that system's processor can handle the interrupt. It is also possible to pass programmed interrupts in either direction by writing to an I/O register on an Adaptor card.

It is important to note that the Bit 3 Adaptor is not merely a simple repeater-type connection linking the timing of both buses together (so that activity on either bus slows down the other). Instead, the Bit 3 Adaptor permits each bus to operate independently. The two buses are linked only when a memory or I/O reference is made to an address on the PC/AT system that translates to a reference on the VMEbus system.

# 1.2.1 Bus-to-Bus Mapping

The 406 Adaptor works by mapping a portion of memory space in the VMEbus chassis into memory space on the PC/AT chassis. The configuration process takes <u>unused</u> memory space in the PC/AT chassis and converts accesses within that space into memory or I/O accesses on the VMEbus. These windows appear to a PC/AT processor as though they were present in that chassis and behave just as if they were local memory.

# 1.2.2 Dual-Port Memory

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The dual-port RAM is an optional memory board that attaches to the VMEbus Adaptor card and looks to both systems as simply more memory. The address of the dual-port RAM is independently set on each Adaptor card, and may be set to respond to one address range in one system and a different range in the other. Both systems can access the memory at the same time, and the VMEbus Adaptor card housing the dual-port RAM arbitrates simultaneous accesses by the two systems. Several different sizes of dual-port RAM are available.

Use of the dual-port RAM allows data passing from the VMEbus to the PC/AT under the control of a VMEbus processor.

#### 1.2.3 Notes on Memory Ranges

The Intel microprocessor in the PC/AT has two modes of operation: real address mode and protected address mode. In real address mode, only the first 1M byte of memory is directly addressable. In protected address mode, all 16M bytes of physical address space is addressable. MS/DOS only directly supports real address mode; UNIX and OS/2, on the other hand, can use real and protected-mode addresses. Support software for developing applications in protected mode on Intel 80386-type machines is available from several thirdparty houses.

If you are using the PC/AT in real address mode, there are only a few large blocks of RAM available. Memory space from 080000 to 0A0000 (128K) and from 0D0000 to 0E0000 (64K) is often free. On some compatibles, the space from 0E0000 to 0F0000 (64K) may also be used.

The PC/AT to VMEbus Adaptor does not permit VMEbus masters to directly access memory or I/O devices on the PC/AT bus. (The dualport RAM option allows indirect VMEbus access to PC/AT memory space.) The PC/AT can co-exist with and share the resources available to any other bus master in the VMEbus chassis.

# 1.2.4 Notes on PC/AT Bus Speeds

The Bit 3 PC/AT-VMEbus Adaptor works with most IBM-compatible AT machines as long as the expansion slot bus speed is 8 MHz.

Many IBM-compatible machines run their microprocessor at 25 MHz or faster; however, the speed of the expansion slot bus in most of these machines is still 8 MHz. The Bit 3 Adaptor should operate properly in these machines.

# 1.2.5 System Controller Operation

The Bit 3 Adaptor has the ability to act as a link between a PC/AT chassis and a VMEbus chassis even when the VMEbus chassis has no system controller present. This form of operation is called "system controller" mode.

System controller mode is selected on the VMEbus Adaptor card. This card is configured in the SYST jumper block to drive the system clock and bus arbitration signals. The Bit 3 VMEbus Adaptor card may be configured to be a single-level bus arbiter on VMEbus level three.

# 1.2.6 Adaptor I/O Operation

The Adaptor requires a minimum of 32 bytes of VMEbus I/O space and 16 bytes of PC/AT I/O space for Adaptor control and status functions. The PC/AT user also has the ability to access VMEbus I/O space by using the PC/AT remote RAM window in combination with a VMEbus "short I/O address modifier".

# 1.2.7 Write Pipelining

Write operations from the PC/AT to remote RAM or dual-port RAM are pipelined -- the Adaptor releases the PC/AT "READY" signal once it has captured the address and data from the PC/AT bus, and the PC/AT is able to proceed with another instruction while the Adaptor is completing the write operation to the VMEbus or dual-port RAM.

If the PC/AT invokes a second read or write operation to the Adaptor before the first has been completed, the Adaptor holds the "READY" so that the second operation does not begin until the first is complete.

Read operations are not pipelined since the PC/AT must wait for the requested data before a new PC/AT bus cycle can occur.

# 1.2.8 Interrupt and Error Handling

To pass the different types of interrupts from one card to another, several jumper pins marked "cable interrupt" or "CINTx" in the following diagrams will be used. A cable interrupt is the latched representation of whatever interrupt the user wishes to pass across the cable -- backpanel or programmed interrupts.

For example, if the user wishes to have VMEbus interrupt IRQ6 passed to PC/AT interrupt IRQ15, he or she would choose any of the four CINT cable lines to carry the interrupt. Two connections are required -on the VMEbus board, from the IRQ6 pin to the chosen CINTx line, and on the PC/AT board, from the CINTx line with the same name to the IRQ15 interrupt pin. The diagrams of the interrupt jumper blocks in the jumper select sections will demonstrate the use of the CINTx lines.

There are three possible sources of interrupts from the Bit 3 Adaptor card:

- (1) Interrupts from the VMEbus chassis to the PC/AT.
- (2) Interface error interrupts.
- (3) Programmed interrupts in either direction.

# 1.2.8.1 Backpanel Interrupts

Up to four of the seven VMEbus interrupts (IRQ1-IRQ7) may be passed to the PC/AT backplane. VMEbus interrupts are passed across the cable interrupt lines to become one of the seven PC/AT interrupts (IRQ3-5, IRQ10-12, and IRQ15) supported by the Adaptor.

# 1.2.8.2 Interface Error Interrupt

The PC/AT interface error interrupt pin (ERR INT) is active when any of the three status error bits (timeout, parity error, or bus error) are active, and is cleared with a "reset status error" command. The interface error interrupt and status bit are meaningful only if the Adaptor card initiates communication over the cable to the other Adaptor. The jumper pin is found in the PC/AT INT jumper block, and may be wire-wrapped or jumpered to any of the seven PC/AT interrupts (IRQ3-5, IRQ10-12, and IRQ15) supported by the Adaptor.

# 1.2.8.3 Programmed Interrupts

Two types of programmed interrupts may be exchanged: (1), programmed interrupt to PC/AT, and (2), programmed interrupt to VMEbus.



PROGRAMMED INTERRUPT TO PC/AT

The pin designated PT in the TINT jumper block on the VMEbus Adaptor card becomes active when the "programmed interrupt to PC/AT" flipflop is set by a VMEbus processor card. This interrupt can be sent from the VMEbus Adaptor board to the PC/AT board IRQ jumper pad over one of the four CINTx lines.

Programmed interrupts to PC/AT work as follows:

- 1. A VMEbus processor writes to the VMEbus Adaptor local node command register and sets the "programmed interrupt to PC/AT" flip-flop on the VMEbus Adaptor card.
- 2. The flip-flop is jumpered to a cable interrupt (CINTx) line which sends the interrupt to the PC/AT Adaptor card.
- 3. The CINTx interrupt passes through a second jumper in the PC/AT IRQ jumper block to become a PC/AT bus interrupt.
- 4. When the PC/AT processor sees this programmed interrupt, it clears the flip-flop by doing a write over the cable to a remote command register located on the VMEbus card.

The programmed interrupt is jumpered to a cable interrupt line in the TINT jumper block to go across the cable; the same-name CINT line at the other end of the cable is jumpered in the PC/AT Adaptor card IRQ jumper block. All interrupts into the PC/AT are edge-sensed (not level-sensed).



#### PROGRAMMED INTERRUPT TO VMEbus

The PGMD-TO-VME interrupt pin (in the RINT jumper block on the VMEbus Adaptor card) becomes active when the "programmed interrupt to VMEbus" flip-flop is set by the PC/AT. This pin can be jumpered directly to VMEbus interrupt line IRQ1 or IRQ2 to cause a VMEbus interrupt.

Programmed interrupts to VMEbus work as follows:

- 1. A PC/AT processor writes over the interface cable to the VMEbus Adaptor card and sets the "programmed interrupt to VMEbus" flip-flop on the VMEbus card.
- 2. The programmed interrupt on the VMEbus Adaptor card activates either IRQ1 or IRQ2 on the VMEbus backplane.
- 3. When the VMEbus processor detects the programmed interrupt, it clears it by doing a local write to the VMEbus Adaptor card.

The "programmed interrupt to VMEbus" is jumpered in the VMEbus RINT jumper block to allow it to pass to the VMEbus backplane. The interrupt to the VMEbus is level-sensed.

# 1.2.9 IACK Read Operation

A PC/AT processor can instruct the VMEbus Adaptor card to perform an interrupt acknowledge on the VMEbus by reading from the Adaptor "IACK READ" register. The Adaptor converts a read of this register into an interrupt acknowledge cycle on the VMEbus. The VMEbus interrupt vector is returned to the PC/AT as data from the read.

# 1.2.10 Page Mode Operation

A PC/AT application may need to access a larger VMEbus address space than the remote RAM window available in the PC/AT permits. The Adaptor provides the means to access any address on a VMEbus system through a much smaller window in PC/AT memory.

In direct addressing mode, remote RAM (VMEbus RAM) is addressed by setting a "window" in remote bus address space as large as the block of RAM to be addressed. For example, if the user wished to address 512K bytes of memory in the VMEbus, he or she would set the PC/AT remote RAM jumpers for a 512K byte window. Page mode, however, permits addressing of all remote RAM locations through a variablesize window in PC/AT address space. The upper sixteen VMEbus address bits in page mode are provided by a sixteen-bit page register located on the VMEbus card. The remaining sixteen lower address bits are provided by the address offset in the PC/AT remote RAM window. It is also possible to use both direct and paged modes and switch between them under program control.

Page mode also controls PC/AT paging to dual-port RAM. When page mode is selected for access to dual-port RAM, address bits A16 through A23 to the dual-port RAM are provided by the value in the page register; address bits A24 through A31 are ignored.

The <u>size</u> of the page may also be varied under program control. A page size register (located on the VMEbus card) allows page size to be selected from the PC/AT in increments from 64K bytes to 1M byte.

# 1.2.11 Address Biasing

When a PC/AT processor <u>directly</u> addresses memory in the VMEbus chassis, it does so by using the remote RAM address range selected on the PC/AT Adaptor card. This address may be convenient for the PC/AT card, but might not be the same as the absolute address that the processor wants to use in the VMEbus chassis. The address bias jumpers on the VMEbus Adaptor card permit the user to offset a PC/AT address into a different VMEbus address on the VMEbus chassis.

Biasing applies only to remote RAM accesses. It does not apply to dual-port RAM accesses.

") ignored in page mode

#### Adaptor Functions

# 1.2.12 Handshake Mode Operation

The user should note that some VMEbus devices can maintain control of the VMEbus for long periods of time -- up to several microseconds or more. If a PC/AT system makes an access to a VMEbus system with a device holding the bus for longer than 15 microseconds, bus timeout errors will occur on the PC/AT Adaptor card. To avoid this problem, data may be transferred in either of two ways -- by transfer through the optional dual-port RAM card or by use of the Adaptor "handshake mode" function.

Handshake mode provides a means for a PC/AT processor to communicate with very slow VMEbus devices. When the handshake mode bit is set, the Adaptor always responds immediately with a reply to the processor without waiting for a reply from the VMEbus. This circumvents the PC/AT timeout, but before the processor can issue the next read or write to the remote bus, it must check the handshake mode READ/WRITE DONE status bit to verify that the first operation has actually been completed.

If the operation was a read from the VMEbus, the data returned from the read is stored in the HANDSHAKE DATA register on the PC/AT Adaptor card. This data register can be read by the processor once it detects that the "handshake mode done" status bit is set. The status bit is set when the VMEbus operation has been completed and is automatically reset at the beginning of a read or write operation.

Note that most transfers from the PC/AT to the VMEbus will be completed in two microseconds or less. Usually, there is no need to use handshake mode.

# 1.2.13 Adaptor Programmed Awaken

The PC/AT automatically checks on initialization (power up or altctrl-del) for the maximum amount of memory available to the system. If the jumpers for the Bit 3 PC/AT board are configured so that remote RAM or dual-port RAM is contiguous with the end of memory in the PC/AT chassis, the PC/AT <u>ordinarily</u> would detect that there is more memory in the system (the Bit 3 board) than it thinks it should have, and it would inform you that the PC/AT has not been configured correctly. To prevent this from happening, the Adaptor card has been designed to not respond to any memory requests after initialization until after an I/O read of the PC/AT Local Node Status Register takes place (register I/O + 2). This one-time "board awaken" is automatic upon reading the status register and enables all memory references to the Adaptor until the PC/AT is reset.

YOU MUST RUN SETUP OR EXECUTE A PC/AT LOCAL NODE STATUS READ TO ENABLE MEMORY ACCESSES THROUGH THE ADAPTOR AFTER POWER-UP OR AFTER AN ALT-CTRL-DEL RESET.

# 1.3 Unpacking

The Adaptor package contains the following items. Please identify each item and notify Bit 3 if any items are missing:

*	One PC/AT circuit board:	Model 406-201
*	One VMEbus circuit board:	Model 406-202
*	One "Utilities Diskette":	Model 400-802
*	This manual:	Model 406-901

- \* An I/O cable to connect the two cards (purchased separately)
- \* A warranty card (please complete and mail)

The Adaptor boards are shipped in static-safe packages to protect the components on the board. It is important for the user to observe static-safety precautions to prevent damage to the board during configuration and installation.

#### 1.4 Adaptor Cables

Standard shielded cables to connect the two Adaptor boards are available in eight foot and twenty-five foot lengths. Microcoax cables are available in fifty foot lengths. Custom-length cables are also available from Bit 3.

All cables are purchased separately.

# 1.5 Configuration Checklists

Before any Adaptor board is installed, determine how each board will be accessed <u>and then</u> configure the Adaptor accordingly. The checklist on this page will greatly simplify this operation; information on each item is found in the sections noted.

CONFIGURATION ITEMS	PC/AT CARD	VMEbus CARD
a) Is there a processor in this chassis, or is the Bit 3 board to operate as system controller? (sections 1.2.5, 3.1.1)	NOT APPLICABLE TO PC/AT CARD	
b) What interrupt level(s) should each Adaptor card activate on an interrupt from the other card? (sections 2.1.6, 3.1.2, 3.1.3)		
c) What unused I/O space do you wish to use for Adaptor I/O? (sections 2.1.4, 3.1.5)	(16 bytes only)	(32 bytes only)
d) What unused address space (in 64K increments) do you wish to map as dual-port RAM, if any? (sections 2.1.6, 3.1.6)		
e) What OTHER unused address space (in 64K increments) will you wish to be mapped over to the other chassis (Remote RAM), if any? (section 2.1.5)		NOT APPLICABLE TO VMEbus CARD
f) What fixed byte and word swaps are desired, if any? (section 2.1.1)		NOT APPLICABLE TO VMEbus
<pre>g) Do you wish to bias addresses received from the other chassis to a <u>different</u> range of address space? If so, what range? (section 3.1.8)</pre>	NOT APPLICABLE TO PC/AT CARD	

# CHAPTER TWO -- PC/AT ADAPTOR BOARD CONFIGURATION

#### 2.0 Introduction

This chapter gives the detailed descriptions of the jumper blocks on the PC/AT Adaptor card and instructions for their configuration. It is important that the user understand how each of the features are configured in order to use the Adaptor correctly, and that the user follow the checklist in section 1.5.

Jumpers are actually inskalled as shown here.

# 2.1 PC/AT Adaptor Board Jumper Blocks

This section describes the jumper blocks on the PC/AT Adaptor board.

#### 2.1.1 System Jumpers

Find the SYS jumper block at location F2 on the PC/AT card. The block is shown here with no jumpers, as the board is shipped:

SYS

- o o 1 jumper if you want to select byte swap
- o o 2 o o 3 jumper if you want to select word swap
- there should never be a jumper on these pins
- 0 0 4 jumper if you are using a IBM PC/RT computer

The "byte swap" and "word swap" jumpers shown above allow the user to control the order of data passing through the Bit 3 Adaptor. This control is most useful when dealing with different types of microprocessor families -- an Intel 80x86, for example, differs from a Motorola 680x0 in that each mandate their own order of bytes within a word or words within a long-word when eight, sixteen, or thirty-two bits of data are moved from one location to another.

These swap options are also available from the PC/AT local node command register at address (I/O + O); setting these options in either place will enable the swap.

The fourth jumper position in this block is jumpered if the Adaptor card is used in an IBM PC/RT machine.

# 2.1.2 Remote RAM Jumpers

The REM RAM HI and LO jumpers select the address range (memory window) that a bus master on the PC/AT bus will reference in its address space when it wants to read from or write to VMEbus memory. An address in the 16M byte PC/AT bus address range may be described as a hex value in the range 00xxxx-FFxxxx.

Accesses from the PC/AT to the VMEbus through the remote RAM window may become A32, A24, or A16 addresses through the use of the VMEbus Adaptor card BIAS, ADDRESS MODIFIER, and ADDRESS PAGE registers.

Set the REM RAM LO jumpers to the first two digits of the six-digit hex PC/AT address for the block of addresses to be mapped to VMEbus memory and to an address that is an even multiple, starting from address zero, of the desired window size. (See section 2.1.4.) Assume that the remaining four digits of the hexidecimal address are all zeros. Set the REM RAM HI jumpers to the first address after the end of the memory to be mapped to the VMEbus. PC/AT address space equal to or greater than the REM RAM LO setting and less than the REM RAM HI setting is mapped to the VMEbus. There <u>must</u> <u>not</u> be any other PC/AT RAM or dual-port RAM at the addresses assigned for remote RAM, since there would then be two memories addressed at the same time and neither card could work properly.

Note that the microprocessor in the PC/AT has two modes of operation: real address mode and protected address mode. In real address mode, only the first megabyte of address space is directly addressable; protected addressing permits access to all 16M bytes of physical address space. MS/DOS only supports real address mode.

Memory space from 080000 to 0A0000 (128K) and from 0D0000 to 0E0000 (64K) is often free. On some compatibles, the space from 0E0000 to 0F0000 (64K) may also be used.

Address ranges 00xxxx-07xxxx, 0Fxxxx, FExxxx, and FFxxxx MUST NOT be used for remote RAM -- these are reserved by the PC/AT processor.

Find the REM RAM HI and LO jumper block at PC/AT card location **D**3. The factory setting shown below for the remote RAM range is for REM RAM LO set to 08 and REM RAM HI set to 0A (hex) -- thereby enabling a 128K byte remote RAM window from 080000 to 09FFFF. The jumper table in section 2.1.4 describes the REM RAM space in hex notation.

		23	22	21	20	19	18	17	16	PC/AT ADDRESS BITS
	ΗI	0	ο	0	0	о	0	ο	ο	
							挈			
REM		Ο	Ο	0	0	0	ò	0	0	Jumper in: bit is "O"
RAM		0					ο	ο		Jumper out: bit is "1"
									1	
	$\mathbf{LO}$	ò	ò	ò	ò	ο	Ő	Ó	Ö	

If you do not wish to use the REM RAM function, set the REM RAM LO and HI jumpers to the same value (the minimum 64K byte window) and locate the REM RAM window somewhere in unused 16M byte address space.

#### 2.1.3 Dual-Port RAM Jumpers

The Dual-Port RAM card is an optional memory board that attaches to the VMEbus Adaptor card and looks to both systems as simply more memory. The address of the dual-port RAM is set by range jumpers on each Adaptor card, and may be set so that the dual-port RAM may respond to one address range in the PC/AT system and to a different range in the VMEbus system.

Both systems may access dual-port memory at the same time. The Adaptor arbitrates conflicts that occur if both systems try to use the memory at the same instant.

If dual-port RAM is used, the minimum range is 64K bytes and the maximum range is 16 megabytes. Dual-port range should be set to match the size of your dual-port memory and to an address that is an even multiple, starting from address zero, of the desired window size. (See section 2.1.4.) If your dual-port memory card is a 32K byte card, set the range to 64K bytes. There <u>must not</u> be any other PC/AT RAM or remote RAM at the addresses assigned for dual-port RAM, since there would then be two memories addressed at the same time and neither card addressed could work properly.

Note that the microprocessor in the PC/AT has two modes of operation: real address mode and protected address mode. In real address mode, only the first megabyte of address space is directly addressable; protected addressing permits access to all 16M bytes of physical address space. MS/DOS only supports real address mode.

Set the DUAL PORT LO jumpers to the first two digits of the six-digit hex PC/AT address for the block of memory to be mapped to the dualport memory. (See section 2.1.4.) Assume that the remaining four digits of the hexidecimal address are all zeros. Set the DUAL PORT HI jumpers to the first address after the end of the memory to be mapped to the dual-port RAM. PC/AT address space equal to or greater than the DUAL PORT LO setting and less than the DUAL PORT HI setting is mapped to Dual-Port memory. Remote RAM may not overlap this space.

Memory space from 080000 to 0A0000 (128K) and from 0D0000 to 0E0000 (64K) is often free. On some compatibles, the space from 0E0000 to 0F0000 (64K) may also be used.

Addresses 00xxxx-07xxxx, 0Fxxxx, FExxxx, and FFxxxx MUST NOT be used for dual-port RAM -- these are reserved by the PC/AT processor.

If you do not wish to use the PORT RAM function, set the PORT RAM LO and HI jumpers to the same value (the minimum 64K byte window) and locate it somewhere in unused 16M byte address space.

Dual-port RAM <u>cannot</u> be accessed through a REM RAM address window -for example, an access from the PC/AT through the REM RAM window, out onto the VMEbus and back into the VMEbus PORT RAM window (loopback). PORT RAM may be accessed ONLY through its own window. Find the DUAL PORT HI and LO jumper block at PC/AT card location F3. The factory setting shown below for the dual-port RAM range is for DUAL-PORT HI and DUAL-PORT LO both set to 1D (hex) -- thereby enabling a 64K byte dual-port RAM window from 1D0000 to 1DFFFF.

		23	22	21	20	19	18	17	16	PC/AT ADDRESS BITS
	HI	Õ	ò	ò	0	0	ο	ò	ο	
		狎								
PORT		0	0	0	0	0	0	0	0	Jumper in: bit is "0"
RAM		o 貄	0 	0 	0	0	0	0 	0	Jumper out: bit is "1"
	$\mathbf{LO}$	0	0	0	0	0	0	0	0	

The jumper table in section 2.1.4 describes the DUAL-PORT space in hex notation. An address in the 16K byte PC/AT bus address range may be described as a hex value in the range 00xxxx-FFxxxx.

#### 2.1.4 PORT RAM/REM RAM Jumper Table

This table describes the jumper positions for both the DUAL-PORT and REM RAM address spaces explained in sections 2.1.2 and 2.1.3. An address in the 16K byte range on the PC/AT bus may be described as a hex value in the range 00xxxx-FFxxxx.

				PC/AT PORT RAM or REM RAM ADDRESS
A23	A22	A21	A20:	FIRST HEX DIGIT
A19	A18	A17	A16:	SECOND HEX DIGIT
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	Α
OFF	ON	OFF	OFF	В
OFF	OFF	ON	ON	С
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

NOTE: For whatever window size used, the dual-port and remote RAM windows must start at an address that is an even multiple, starting from address zero, of the selected window size. Thus, for a 64K byte window size, the window must start on a 64K byte address in the address space; for a 128K byte window, the window must start on a 128K byte address, and so on.

# 2.1.5 I/O Range Jumpers

The PC/AT Adaptor card uses a minimum of sixteen bytes of I/O space - eight to access control and status registers on the PC/AT card, and eight for control and status registers on the VMEbus card. The I/O jumper block selects the address range that a PC/AT bus master will use when it wants to read from or write to I/O space on the Adaptor cards.

Find the I/O jumper block at location E<sup>®</sup> on the PC/AT card. The jumpers are shown here as the board is shipped, configured for a sixteen-byte I/O range of 200-20F (hex):

		9	8	7	6	5	4	PC/AT ADDRESS BITS
				-	o	-	-	
	HI		•	•	•		•	
I/O		ο	ο	0	ο	0	0	Jumper present: bit is "O"
					O			Jumper out: bit is "1"
	$\mathbf{LO}$							
		ο	ο	Ο	ο	Ο	0	Always set I/O LO equal to I/O HI

The Adaptor I/O range starts on a sixteen-byte boundary from address zero and is sixteen bytes long. (To insure this, there are no I/O jumpers for address bits 0-3, and the I/O LO and the I/O HI jumpers are to be set to exactly the same value.) Also note that the PC/AT Adaptor card only decodes I/O address bits 0-9, even though sixteen I/O address bits are present on the address bus.

Some PC/AT I/O addresses are reserved by the internal requirements of the PC/AT and cannot be used by the Adaptor. Also, be sure to choose an I/O address NOT used by another I/O card already in the PC/AT, since two cards would be addressed at the same time and neither would work. I/O locations reserved for PC/AT cards that are not installed may be used for Adaptor I/O. Pre-assigned PC/AT I/O locations are:

000 - OFF	reserved for internal PC/AT use
1FO - 1F8	Fixed Disk
200 - 20F	Game Control
278 - 27F	Second parallel printer port
2F8 - 2FF	Second Async port
300 - 31F	Prototype Card
378 - 37F	Printer port
380 - 38C	SDLC Communications
380 - 389	BI-SYNC Communications secondary
3AO - 3AF	BI-SYNC Communications primary
3BO - 3BF	Monochrome Display/Printer
3D0 - 3DF	Color/Graphics
3F0 - 3F7	Diskette
3F8 - 3FF	Async Communications (primary)

PC/AT Adaptor Board Configuration

Bit 3 notes that the ranges 200-20F and 300-30F (hex) are often left unused. Also note that the Bit 3 SETUP Utility on the Utilities Diskette is written to operate at I/O 200-20F.

A PC/AT processor wishing to access VMEbus I/O (remote bus I/O) may do so by writing a "short address modifier" (address modifiers 29 or 2D) to the ADDRESS MODIFIER register and then addressing VMEbus I/O space (short address space) through the PC/AT remote RAM window.

The following table describes the Adaptor I/O space in hex notation. An address in the 1024-byte PC/AT I/O range may be described as a hex value in the range 00x-3Fx.

		A9	A8	PC/AT I/O ADDRESS FIRST HEX DIGIT
<u>A7</u>	A6	A5	Α4	PC/AT I/O ADDRESS SECOND HEX DIGIT
ON	ON	ON	ON	0
ON	ON	ON	OFF	1
ON	ON	OFF	ON	2
ON	ON	OFF	OFF	3
ON	OFF	ON	ON	4
ON	OFF	ON	OFF	5
ON	OFF	OFF	ON	6
ON	OFF	OFF	OFF	7
OFF	ON	ON	ON	8
OFF	ON	ON	OFF	9
OFF	ON	OFF	ON	A
OFF	ON	OFF	OFF	B
OFF	OFF	ON	ON	С
OFF	OFF	ON	OFF	D
OFF	OFF	OFF	ON	E
OFF	OFF	OFF	OFF	F

# 2.1.6 Interrupt Jumpers

The interrupt jumper block on the PC/AT Adaptor card establishes which of the four possible interrupts coming across the cable from the VMEbus card (cable interrupts) will go out to the PC/AT bus as an interrupt request. A fifth pin also allows an error on the Bit 3 PC/AT card to become a PC/AT interrupt request. Up to four of the seven VMEbus (IRQ1-IRQ7) interrupts and/or the error interrupt may be passed to one of the seven uncommitted PC/AT interrupt lines (IRQ03-IRQ05, IRQ10-IRQ12, and IRQ15).

Note that unused PC/AT interrupt lines must be selected for VMEbus interrupts; PC/AT interrupts cannot be "wire-ORed" because the PC/AT interrupt controller looks for the low-to-high edge of the interrupt. The Adaptor inverts the VMEbus interrupt signals before sending them to the PC/AT to insure that the leading (rising) edge of a VMEbus interrupt will be detected by the PC/AT.

Cable interrupt pins (labeled CINT1-CINT4 on the diagram below) are the latched representation of whatever interrupts the user chooses to pass across the cable to the PC/AT card. If the user, for example, wishes to have VMEbus interrupt IRQ1 cause a PC/AT interrupt IRQ12, he or she would choose one of the four CINT lines to carry the interrupt and then make two connections -- from the IRQ1 pin on the VMEbus card to the chosen CINTx line, and, on the PC/AT card, from the CINTx line with the same name to the PC/AT interrupt IRQ12.

The ERR INT pin (error interrupt) is pulled low when any of several interface error conditions (interface parity error, remote node bus error, or interface timeout) occur on the PC/AT Adaptor card, and is cleared with a "reset status error" command. The ERR INT pin may be wire-wrapped or jumpered to a PC/AT interrupt line in the same manner as any of the cable interrupts.

Find the IRQ jumper block at location G6 on the PC/AT Adaptor card. The block is shown here with no jumpers, as the card is shipped:

		о З	PC/AT IRQO3 -	These
		o 4	PC/AT IRQ04	seven
These four	ERR INT	00 0 5	PC/AT IRQ05	lines
cable lines	- CINT4	4 o o 10	PC/AT IRQ10	connect to
carry VMEbus	CINT3	30011	PC/AT IRQ11	the PC/AT
interrupts	CINT2	20012	PC/AT IRQ12	backpanel
to the PC/AT	- CINT1	1 o o 15	PC/AT IRQ15 -	interrupts

Any of the four cable interrupt lines may be connected from the VMEbus to the PC/AT bus, as long as the user remembers that their use requires two connections -- one on the PC/AT card and one on the VMEbus card. The lines may be jumpered or wire-wrapped. The PC/AT card interrupt pins may NOT be "wire-ORed".

Several of the PC/AT interrupt lines are pre-assigned in a normally configured PC/AT. Other option cards in the PC/AT may already use an interrupt line that you are thinking of using. <u>Check for this before assigning VMEbus interrupts to the PC/AT</u>.

The PC/AT interrupts accessible by the Bit 3 Adaptor are listed here in order of descending priority:

INT10 ---- NOT CURRENTLY ASSIGNED
INT11 ---- NOT CURRENTLY ASSIGNED
INT12 ---- NOT CURRENTLY ASSIGNED
INT15 ---- NOT CURRENTLY ASSIGNED
INT3 ---- ALTERNATE COMM CARD, SDLC CARD or BI-SYNC CARD
INT4 ---- PRIMARY COMM CARD, SDLC CARD or BI-SYNC CARD
INT5 ---- FIXED DISK

Note that this chapter covers PC/AT Adaptor card configuration; since one connection must be made on each Adaptor board to pass an interrupt, the user is also referred to section 3.1.2 for jumpering interrupts through the VMEbus Adaptor card.

# 2.1.7 Other PC/AT Adaptor Board Jumpers

The jumpers at location B5 are timing jumpers which are preset at the factory and are not to be changed by the user. The typical setting for these jumpers is shown below.

HI	1	2	3	4	4	3	2	1	$\mathbf{LO}$	
	ο	o	Ο	ο	ο	0	ο	ο		
										TIMING JUMPERS
	ο	ο	ο	ο	0	Ο	ο	ο		

# 2.2 PC/AT Adaptor Card Factory Settings

The PC/AT Adaptor card is configured as follows when shipped:

PC/AT REMOTE RAM RANGE	080000 - 09FFFF (hex)
PC/AT DUAL-PORT RAM RANGE	1D0000 - 1DFFFF (hex)
PC/AT ADAPTOR I/O RANGE	200 - 20F (hex)
PC/AT INTERRUPT JUMPERS	none
PC/AT SYSTEM JUMPERS	none

#### CHAPTER THREE -- VMEbus ADAPTOR BOARD CONFIGURATION

#### 3.0 Introduction

This chapter gives the detailed descriptions of the jumper blocks on the VMEbus Adaptor card and instructions for their configuration. It is important that the user understand how each of the features are configured in order to use the Adaptor correctly, and that the user follow the checklist in section 1.5.

# 3.1 VMEbus Adaptor Board Jumper Blocks

This section describes the jumper blocks on the VME Adaptor board.

Jumpers are actually installed as shown here.

#### 3.1.1 System Jumpers

Find the SYS jumper block at location J7 on the VMEbus Adaptor board. The block is shown here as the board is shipped:

1	00	there should always be a jumper on these pins
2	0 0 S	
3	оо Ү	there should always be a jumper on these pins
4	oo s	
5	00	jumper if this card will drive VME SYSRESET
6	00	jumper if this card will detect bus timeouts
7	0 0	there should never be a jumper on these pins

VME SYSCLK DRIVE: This jumper allows the Adaptor board to supply the VMEbus SYSCLK signal to its VME backplane. The board is to drive this signal (jumper IN) when it is the VMEbus system controller and no other device is driving SYSCLK. THERE MUST BE ONE SYSCLK PRESENT FOR THE ADAPTOR TO FUNCTION. See section 1.2.5.

VME SYSRESET DRIVE: This jumper allows the Adaptor board to supply VMEbus SYSRESET to its VME backplane, which may be either a power-on reset or a programmed reset from the PC/AT bus. See section 1.2.5.

VME BUS TIMEOUT: This jumper allows the Adaptor board to drive the VMEbus BERR (bus error) signal to its VME backplane if any transfer on the bus exceeds 48 microseconds (bus timeout). The board is usually jumpered to detect bus timeout (jumper IN) also when it is the VMEbus system controller. See section 1.2.5.

# 3.1.2 Transmitted Interrupt Jumpers

Find the TINT jumper block at location  $\clubsuit$ 3 on the VMEbus Adaptor card. The block is shown here with no jumpers, as the board is shipped:

These seven	_	VMEbus	IRQ1	о	о	1	CINT1 - These cable
lines		VMEbus	IRQ2	ο	ο	2	CINT2   lines carry
connect to		VMEbus	IRQ3	ο	ο	3	CINT3 interrupts
the VMEbus		VMEbus	IRQ4	ο	ο	4	CINT4 - to the PC/AT
backpanel		VMEbus	IRQ5	ο	ο	5	not used
interrupts		VMEbus	IRQ6	ο	ο	6	not used
	·	VMEbus	IRQ7	ο	ο	7	not used
					ο	РТ	PGMD-TO-AT INTERRUPT
				Т-	INT		(only to CINTx line)

This group of jumpers permits selection of interrupts to go across the cable to the remote Adaptor card. The pins in the left column are the possible choices for VMEbus interrupts to go out across the cable to the PC/AT bus. The CINT pins in the right column are the four cable interrupt lines that allow the left-column signals to pass to the PC/AT bus. The PGMD-TO-AT INTERRUPT pin is the programmed interrupt signal described in section 1.2.8.3 above. The pins may be jumpered STRAIGHT ACROSS from the left column pins to the right (or from the PT pin to one of the CINTx pins).

#### 3.1.3 Received Interrupt Jumpers

Find the RINT jumper block at location J6 on the VMEbus Adaptor card. The block is shown here as the board is shipped:

PGMD-TO-VME INTERRUPT 3 0 VME IRQ1 4 0 0 not used not used 5 0 R-INT

The PGMD-TO-VME INTERRUPT pin is a programmed interrupt from the PC/AT chassis to the VMEbus processor. Pins 1 and 5 in the left column and the two pins in the right column are not used.

The PGMD-TO-VME interrupt may be asserted as VME IRQ1 or VME IRQ2 through this jumper pad. IRQ1 and IRQ2 may be jumpered or wire-wrapped to the PGMD-TO-VME pin to permit this interrupt source to cause an IRQ1 or IRQ2 interrupt on the VMEbus backplane.

As an example, a user wishing to have IRQ2 asserted when a PC/AT processor invokes a "programmed interrupt to VMEbus" would place a jumper between the IRQ2 and PGMD-TO-VME pins.

# 3.1.4 Bus Grant and Bus Request Jumpers

Find the bus grant (BGO-BGI) jumper block at location M2 and the bus request (BR) jumper block at location L7 on the VMEbus Adaptor card. These blocks establish the Adaptor card bus grant and request levels.

If there is a bus arbiter in the VMEbus system, the Adaptor card can be configured to use any of the four bus request/ bus grant levels. If there is no bus arbiter in the VMEbus system, the Bit 3 Adaptor can be set to become a single-level arbiter on level 3. (In singlelevel bus arbitration mode, the VMEbus Adaptor card is the highest priority bus master; it will respond to bus requests on level 3 and will activate the level 3 bus grant line when the Adaptor does not need the bus.)

**CAUTION** -- VME backplanes have jumpers to connect the daisy-chained bus request, bus grant and interrupt acknowledge signals around unused card locations. Make sure that these jumpers are removed for the Adaptor card's VMEbus slot.

If the VMEbus Adaptor card is to be the bus arbiter (on level 3), configure the jumpers as follows:

	BGO-BGI								
	0-	-0		BA	0	ο	ο		
_		0 0-			1	ο	ο		
$\rightarrow$	ο	00	ο	2	2	ο	ο		
	ο	00	ο	1	3	0-	-0		
	ο	00	ο	0		в	R		

The following table summarizes the four configuration options for the VMEbus Adaptor card if the VMEbus chassis does have another bus arbiter. Note that in all four of these cases, the "bus request" level will always match the "bus grant daisy chain" level.

BGO-BGI		BGO-BGI	
O O BA	000	O O BA	000
00 00 3	1 o o	o oo o 3	1 o o
o oo o 2	200	00 00 2	2 00
o oo o 1	3 00	o oo o 1	300
0 00 0 0	BR	0 00 0 0	BR
BUS REQUES	r 3	BUS REQUES	Г 2
BGO-BGI		BGO-BGI	
O O BA	000	O O BA	0 00
o oo o 3	1 00	o oo o 3	1 o o
o oo o 2	200	o oo o 2	20 O
00 00 1	300	o oo o 1	30 O
0 00 0 0	BR	00 00 0	BR
BUS REQUEST	r 1	BUS REQUES	r 0

VMEbus Adaptor Board Configuration

# 3.1.5 I/O Range Jumpers

Find the I/O jumper block at VME card location G2. This jumper block is used to set the range of the Adaptor card in VMEbus I/O space.

The VMEbus Adaptor uses 32 bytes of I/O space. The first eight bytes are used for miscellaneous control registers on the VMEbus Adaptor card; the next twenty-four bytes are reserved by the Adaptor. I/O LO is always set equal to I/O HI.

15	00	00	A15 -	VMEbus ADDRESS BITS
14	00	00	A14	
13	0 0	0 0	A13	Jumper out: bit is "1"
12	00	00	A12	Jumper in : bit is "O"
11	00	00	A11	-
10	00	00	A10	
9	00	00	A09	Always set I/O LO equal
8	00	00	A08 – '	to I/O HI
	HI	LO		
	I/	/0		

A jumper present causes the address bit to be a "zero". A jumper off causes the address bit to be a "one". The I/O range factory setting is 2000-201F (hex). I/O LO is always to be set equal to I/O HI.

A15 A11 ON ON ON ON ON OFF OFF OFF	A14 A10 ON ON ON OFF OFF OFF ON ON ON ON OFF	A13 A09 ON OFF OFF ON OFF ON OFF ON OFF ON	A12: A08: ON OFF ON OFF ON OFF ON OFF ON OFF ON OFF ON	VME VME 0 1 2 3 4 5 6 7 8 9 A B C	•	ADDRESS ADDRESS		
		-						
OFF	OFF	ON	OFF	D				
OFF	OFF	OFF	ON	E				
OFF	OFF	OFF	OFF	F				

The Adaptor I/O range logic responds to short I/O address modifiers "29" and "2D".

#### 3.1.6 Dual-Port RAM Jumpers

Find the DUAL PORT HI and LO jumper block at VME card location L4.

The DUAL PORT HI and LO jumpers select the address range that a bus master on the VMEbus will reference when it wants to read or write to the dual-port RAM. The DUAL PORT LO jumper block sets the starting VMEbus address and the DUAL PORT HI selects the ending address. One additional jumper (marked "A32") selects whether the board will respond to 24-bit address space or 32-bit space.

The minimum range is 64K bytes and the maximum range is 4 gigabytes. Set the range to match the size of your dual-port memory. If the dual-port memory is less than 64K bytes, set the range to 64K bytes. There cannot be any other VMEbus RAM or remote RAM at the addresses assigned for dual-port RAM, since there would then be two memories addressed at the same time; neither card could work properly.

Set the DUAL PORT LO jumpers to the first four digits of the eightdigit hex VMEbus address for the block of memory to be mapped to the dual-port memory. Assume that the remaining four digits of the hexidecimal address are all zeros. Set the DUAL PORT HI jumpers to the first address after the end of the memory to be mapped to the dual-port RAM. VMEbus address space equal to or greater than the DUAL PORT LO setting and less than the DUAL PORT HI setting is mapped to Dual-Port memory.

If you want to disable the PORT RAM function, or if you do not install the PORT RAM option, set the PORT RAM HI jumpers to a value less than the PORT RAM LO jumpers.

If the user wishes to access only 24-bit address space, leave the "A32" jumper out when configuring the board. Jumpers 24-31 are ignored when the "A32" jumper is not present.

In 32-bit mode, the Adaptor Dual-Port RAM will respond to address modifiers "09", "0A", "0D", and "0E". In 24-bit mode, Adaptor Dual-Port RAM will respond to address modifiers "39", "3A, "3D", and "3E".

The dual-port RAM module is able to respond to eight-bit, sixteenbit, and thirty-two-bit data transfers from the VMEbus.

Note that for whatever window size used, the dual-port window must start at an address that is an even multiple, starting from address zero, of the selected window size. Thus, for a 64K byte window size, the window must start on a 64K byte address in the address space; for a 128K byte window, the window must start on a 128K byte address, and so on.

DUAL	-PORT			
00	0 0	31	A31	-
00	00	30	A30	Jumper in : bit is "zero"
00	00	29	A29	Jumper out: bit is "one"
00	00	28	A28	
00	00	27	A27	
00	00	26	A26	
00	00	25	A25	
00	00	24	A24	VMEbus ADDRESS
00	00	23	A23	BITS
00	00	22	A22	
00	00	21	A21	
00	00	20	A20	
00	00	19	A19	
00	00	18	A18	
00	00	17	A17	
00	00	16	A16	-
00	A32		24-bi	t/32-bit SWITCH (IN = 32-bit)
HI	LO			

The factory setting for the remote RAM range is for DUAL-PORT HI set less than DUAL-PORT LO -- thereby disabling the dual-port RAM window.

The jumper table below describes the DUAL-PORT space in hex notation. An address in the 4G byte VMEbus address range may be described as a hex value in the range 0000xxxx-FFFFxxxx.

A31 A27 A23 A19 ON ON ON ON ON ON ON OFF OFF OFF OFF	A30 A26 A22 A18 ON ON ON OFF OFF OFF OFF ON ON ON ON ON ON OFF	A29 A25 A21 A17 ON OFF OFF ON OFF ON OFF ON OFF ON OFF ON ON ON ON	A28: A24: A20: <u>A16:</u> ON OFF ON OFF ON OFF ON OFF ON OFF ON OFF ON OFF	FIRST HEX DIGIT SECOND HEX DIGIT THIRD HEX DIGIT FOURTH HEX DIGIT 0 1 2 3 4 5 6 7 8 9 A B C D	-   VMEbus   DUAL PORT - ADDRESS
OFF OFF	OFF OFF	ON OFF	OFF ON	D E	
OFF	OFF	OFF	OFF	F	

· •

# 3.1.7 Unused Remote RAM Jumpers

Find the REM RAM HI and LO jumper block at VME card location L6.

The REM RAM jumpers on the VMEbus Adaptor card ARE NOT USED WITH THE MODEL 406 ADAPTOR. These jumpers exist ONLY for the use of the Bit 3 VMEbus Adaptor card in OTHER applications. These jumpers are set at the factory to a "disabled" setting, which is shown below:

REM	RAM			
00	0 0	31	A31	-
00	00	30	A30	Jumper in : bit is "zero"
00	00	29	A29	Jumper out: bit is "one"
00	00	28	A28	
00	00	27	A27	
00	00	26	A26	
00	00	25	A25	
00	00	24	A24	VMEbus ADDRESS
00	00	23	A23	BITS
00	00	22	A22	
00	00	21	A21	
00	00	20	A20	
00	00	19	A19	
00	00	18	A18	
00	00	17	A17	
00	00	16	A16	-
00	A32		24-bi	it/32-bit SWITCH (IN = 32-bit)
HI	LO			

The factory setting for the remote RAM range is for REM RAM HI set less than REM RAM LO -- thereby disabling the REM RAM window.

PLEASE DO NOT USE THIS WINDOW.

VMEbus Adaptor Board Configuration

# 3.1.8 Address Bias Jumpers

When a PC/AT device addresses VMEbus remote RAM through its remote RAM window, the lower sixteen address lines are passed on "as is" to the remote backpanel. This establishes the minimum contiguous block of remote addresses as 65K bytes in VMEbus memory (sixteen address bits = 65K). The user may position this 65K byte block anywhere in VMEbus address space so long as the target address starts on a 65K byte boundary (from address zero). In direct mode, the BIAS jumpers allow three choices for the remaining high-order address lines:

- (1) Set the VMEbus address bit to a "ZERO".
- (2) Set the VMEbus address bit to a "ONE".
- (3) Extend VMEbus address range by passing more address bits from the PC/AT to the VMEbus.

The VMEbus Adaptor cards are set at the factory to access VMEbus RAM starting at VMEbus address zero. If the user wishes to re-position the address in VMEbus memory, the jumpers will have to be changed.

	Transmitter		I	Receiver	VMEbus
PC/AT				>	> address
bus		I/O CABLE			bits 15-01
>	>	address>	>		
		(24 bits)			VMEbus
				BIAS>	> address
	· · · · · · · · · · · · · · · · · · ·			· · · · · · · · · · · · · · · · · · ·	bits 31-16

Note that THE BIAS JUMPERS ADJUST THE ADDRESSES COMING FROM ACROSS THE CABLE -- not the addresses local to the Adaptor board. Also note that the bias jumpers are ignored when page mode is selected. (In page mode, the upper sixteen VMEbus address bits are supplied by a page register on the remote Adaptor card. See section 1.2.10.)

Connecting cable address line A16 to VMEbus address line A16 will cause the Adaptor to address a 128K byte VMEbus block. Connecting cable address A17, A18, A19, A20, A21, A22, and A23 to VMEbus address lines A17, A18, A19, A20, A21, A22, and A23 extends the range to 256K, 512K, 1M, 2M, 4M, 8M, and 16M bytes, respectively.

Once the range has been established, the remaining higher VMEbus address bits must be jumpered to ground or left open to establish the VMEbus starting address. A bit left unjumpered appears as a "one" on the target VMEbus address lines. A bit jumpered to a ground pin appears as a "zero" on the target VMEbus address lines.

Note that for whatever window size used, the dual-port and remote RAM windows (jumper-selected on each card) must start at an address that is an even multiple, starting from address zero, of the selected window size. Thus, for a 64K byte window size, the window must start on a 64K byte address in the address space; for a 128K byte window, the window must start on a 128K byte address, and so on.

Be sure to not set the bias jumpers such that an access from the PC/AT chassis to the VMEbus maps through the VMEbus Adaptor card and back into the Adaptor (loopback into dual-port RAM space, for example). This would cause an Adaptor conflict and cannot work.

NOTE: The user may also use the card in page mode, where the upper sixteen VMEbus address bits are supplied by a page register on the VMEbus Adaptor card. See section 1.2.10.

Find the BIAS jumper block at location E1. The middle column pins connect through a buffer to drive the VMEbus address lines A31-A16. The right column pins are all grounded. The left column pins 16-23 are the address bits from the PC/AT. THE LEFT COLUMN PINS 24-31 MUST BE LEFT UNUSED.



The jumper positions shown are the factory jumper settings, with all addresses from the PC/AT biased to zero.

VMEbus Adaptor Board Configuration

#### 3.2 VMEbus Adaptor Board Factory Settings

The VMEbus Adaptor card is configured as follows when shipped:

VMEbus DUAL-PORT RAM RANGEdisabledVMEbus ADDRESS BIASSTART AT VMEbus ADDRESS ZEROVMEbus ADAPTOR I/O RANGE2000 - 201F (hex)VMEbus RINT JUMPERSnoneVMEbus TINT JUMPERSnoneVMEbus IRQ LEVELnone

VMEbus card NOT driving VME SYSCLK VMEbus card NOT driving VME SYSRESET VMEbus card NOT driving VME bus timeout (BERR)

#### 3.3 VMEbus Adaptor Board LEDs

Find the three LEDs at location K12 on the VMEbus Adaptor card.

The green LED on the Adaptor card labeled "READY" is on when the logic arrays on the card have been successfully loaded after poweron. The green LED must be on for the card to operate.

The red LED on the Adaptor card labeled "REMOTE" is on when the card is processing a command from the PC/AT Adaptor card.

The red LED on the Adaptor card labeled "LOCAL" is on when that card is being addressed by its local VMEbus chassis. The LED will be on if the Adaptor card recognizes a VMEbus address even if there is no active cycle (address strobe) in process.

#### CHAPTER FOUR -- INSTALLATION

#### 4.0 Installing Adaptor Cards

The Adaptor cards are shipped in static-safe packages to protect the components on the card. It is important for the user to observe static-safety precautions to prevent damage to the cards. ALSO -- BE SURE POWER IS OFF IN BOTH CHASSIS BEFORE INSTALLING ADAPTOR CARDS!

The PC/AT Adaptor card may be installed in any unoccupied dualconnector slot in the PC/AT. Locate a vacant slot and remove the metal plate covering the cable exit in the rear of the chassis. Insert the card into the connector and secure it with the same screw.

The VMEbus Adaptor card may be installed in any unoccupied 6U slot in the VME card cage. (If the VME Adaptor card is to operate as the system controller in the VME cage, it must be installed in slot 1.)

The cable connectors mate with the I/O cable ordered separately. Match the "A/B" label on the cable connector to the label above the VME Adaptor card faceplate. The connectors are keyed so that the cables cannot be installed incorrectly. Connect the cable shield wire lug to the VMEbus chassis. (When removing the connectors, use the pull tabs -- DO NOT pull on the cable.) Plug the cable connector into its mate on the PC/AT Adaptor card and secure it with the two screws on the cable connector body.

The VMEbus has a bus priority scheme that permits other bus masters to use other cards on the VMEbus. Before a VME bus master can talk to other VME cards, it must first gain control of the bus. A VMEbus functional module called the "bus arbiter" grants VME cards permission to use the VMEbus, and is located either on a separate system controller board or integrated into a processor card. It is beyond the scope of this manual to describe VMEbus arbitration, but it is essential that the user understand how it works. The <u>VMEbus</u> <u>Specification Manual</u> (see below) describes the VMEbus and the bus arbiter in detail. Experience shows that a common problem that VMEbus users encounter is an inability to communicate with other VME cards because the bus arbiter has been incorrectly configured.

The Adaptor can be configured with jumpers to work with an alreadyinstalled system controller board containing a bus arbiter. If necessary, the Adaptor can provide the system controller function of driving the system clock and can be a single level bus arbiter on level 3. In single-level bus arbitration mode, the Adaptor is the highest priority bus master, will respond to bus requests on level 3 from other masters, and will activate the level 3 bus grant line when the Adaptor does not need the VMEbus. The Adaptor operates in release-on-request mode unless the Adaptor bus lock flip-flop is set.

The <u>VMEbus Specification Manual</u> is available from VITA (VMEbus International Trade Association), 10229 N. Scottsdale RD., Suite E, Scottsdale, Az. 85253. The VMEbus standard is also available as <u>IEEE Standard 1014</u> from The Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, NJ 08855-1331.

Installation
#### CHAPTER FIVE -- SOFTWARE CONSIDERATIONS

#### 5.0 Introduction

This section describes both the PC/AT and the VMEbus Adaptor card control and status registers. These registers are accessed through I/O space selected by the I/O range jumpers on each card.

The first eight bytes of the PC/AT Adaptor I/O space are for a PC/AT processor to control and check status of the Adaptor card in its chassis -- eight bytes called "Adaptor local node registers". The following eight bytes of the Adaptor I/O space are for a PC/AT processor to talk to the <u>remote</u> (VMEbus) Adaptor card registers -- eight bytes called "Adaptor remote node registers".



In the same context, the first eight bytes of the VMEbus Adaptor card's I/O space are for a VMEbus processor to talk to <u>its</u> Adaptor local node registers. However, the following twenty-four bytes of I/O are reserved by the Adaptor and must not be accessed.

The following tables show the destination of Adaptor I/O accesses:

	DESTINATION Local node I/O - on PC/AT Adaptor card Remote node I/O - on VME Adaptor card
VME     I/O     ADDR     RANGE (hex)       I/O     LO     +     0     -     I/O     LO     +     7:       I/O     LO     +     8     -     I/O     LO     +     1F:	DESTINATION Local node I/O - on VME Adaptor card Reserved addresses - DO NOT USE

## 5.1 PC/AT Adaptor Local Node Registers

These registers are located on the local (PC/AT) Adaptor card and are addressed by processors on the PC/AT bus.

PC/AT I/O ADDR	WRITE FUNCTION	READ FUNCTION
I/O LO + O	LOCAL COMMAND REGISTER	LOCAL COMMAND REGISTER
I/O LO + 1	reserved	reserved
I/O LO + 2	reserved	LOCAL STATUS REGISTER
I/O LO + 3	reserved	reserved
I/O LO + 4	reserved	HANDSHAKE MODE DATA REG
I/O LO + 5	reserved	HANDSHAKE MODE DATA REG
I/O LO + 6	reserved	reserved
I/O LO + 7 (hex)	reserved	reserved

#### 5.1.1 Local Node Command Register

The local node command register is a read/write register.

BIT	FUNCTION
7	"1" = Clear PC/AT status reg errors (one shot)
6	"1" = Select byte swap "0" = Deselect
5	"1" = Select word swap "0" = Deselect
4	not defined - must be O
3	not defined - must be O
2	not defined - must be O
1	not defined - must be O
0	"1" = Select handshake mode "0" = Deselect

CLEAR STATUS REGISTER ERRORS (BIT 7): Communication between the two systems is monitored for (1) cable parity errors, (2) VME bus error, and (3) interface timeouts (the VMEbus system takes too long to respond). These errors sets their corresponding error bit in the local node status register. The error bit flip-flop stays set until cleared by writing a "1" to bit 7 of the local node command register.

SWAP SELECTS (BITS 6 and 5): The byte swap and word swap options are <u>identical</u> to the swap options provided by the PC/AT Adaptor card byte swap and word swap jumpers. These bits provide in-process switching of swapping (just as the jumpers provide constant swapping.)

If byte swap is enabled, PC/AT data bus bits 0-7 are mapped to VMEbus data bits 8-15 and PC/AT data bus bits 8-15 are mapped to VMEbus data bits 0-7. The byte swap occurs on references from the PC/AT to the VMEbus or to dual-port RAM but not on references to the command and status registers on the Adaptor boards.

If word swap is enabled, PC/AT address bit A01 is inverted on references to the VMEbus or to the dual-port RAM, but not on references to the I/O registers on the Adaptor boards.

SELECT HANDSHAKE MODE (BIT 0): The user sets this bit to "1" when handshake mode operation is desired. A "0" returns the Adaptor to normal operation.

Software Considerations

## 5.1.2 Local Node Status Register

The local node status register is a read-only register.

BIT		FUNCTION
7	"1" =	Interface parity error
6	"1" =	VMEbus error on PC/AT-VMEbus transfer
5		reserved for future use
		reserved for future use
3	"1" =	Handshake Mode selected
2	"1" =	Interface timeout
1	"1" =	Handshake Mode data ready
		Remote bus power off or $1/0$ cable is off

LOCAL NODE STATUS REGISTER bit 7 is a "1" if an interface parity error has occurred on a PC/AT-to-VMEbus transfer. This bit is cleared by "clear status register".

LOCAL NODE STATUS REGISTER bit 6 is a "1" if a VMEbus bus error has occurred. This bit is cleared by "clear status register".

LOCAL NODE STATUS REGISTER bit 3 is a "1" when handshake mode has been selected in the local node command register.

LOCAL NODE STATUS REGISTER bit 2 is a "1" if an interface timeout occurred. The Adaptor waits 15 microseconds for a response to a read or write command on the VMEbus, and if the Adaptor cannot complete the operation in that time, the interface timeout status bit is set and the operation is terminated.

LOCAL NODE STATUS REGISTER bit 1 is a "1" when the VMEbus Adaptor card indicates that a handshake operation has been completed. This bit is automatically reset at the beginning of a read or write operation. If the operation was a remote bus read, the data from the read is stored in the HANDSHAKE DATA register.

LOCAL NODE STATUS REGISTER bit 0 is a "1" if the VMEbus chassis power is off or if the I/O cable is not connected. If this bit is a "1", there is no point in trying to communicate with the remote bus since only timeout errors will result.

YOU MUST RUN SETUP OR EXECUTE A READ OF THE PC/AT LOCAL NODE STATUS REGISTER TO ENABLE MEMORY AFTER POWER-ON OR AN ADAPTOR RESET.

### 5.1.3 Handshake Data Register

This local read-only register holds the data received from the VMEbus when handshake mode is selected for a read operation and when the "handshake mode data ready" status bit is set.

#### 5.2 PC/AT Adaptor Remote Node Registers

These eight registers are controlled by processors on the PC/AT bus, but are located on the REMOTE (VMEbus) Adaptor card.

PC/AT I/O ADDR	WRITE FUNCTION	READ FUNCTION
I/O LO + 8	REMOTE COMMAND REG 1	REMOTE NODE STATUS REG
I/O LO + 9	REMOTE COMMAND REG 2	REMOTE COMMAND REG 2
I/O LO + A	ADDRESS PAGE LOW REG	ADDRESS PAGE LOW REG
I/O LO + B	ADDRESS PAGE HIGH REG	ADDRESS PAGE HIGH REG
I/O LO + C	reserved	reserved
I/O LO + D	REMOTE ADDRESS MODIFIER	REMOTE ADDRESS MODIFIER
I/O LO + E	reserved	IACK READ LOW REG
I/O LO + F (hex)	reserved	IACK READ HIGH REG

#### 5.2.1 Remote Node Command Register 1

Remote node command register 1 is a write-only register.

BIT	FUNCTION
7	"1" = reset VMEbus card (one shot, allow 1 sec)
	"0" = clear "reset" status in remote node status reg
б	"1" = clear PGMD-TO-AT interrupt FF on VMEbus card
	"0" = no action
5	"1" = set PGMD-TO-VME interrupt FF on VMEbus card
	"0" = reset interrupt
4	"1" = LOCK VMEbus
	"0" = UNLOCK VMEbus
3	"1" = use address page register
	"0" = use address bias jumpers
2	IACK READ MODE ADDRESS BIT 2 (VME address bit 3)
1	
0	IACK READ MODE ADDRESS BIT 0 (VME address bit 1)

RESET REMOTE ADAPTOR BOARD (BIT 7): The VMEbus Adaptor card has a power-on-reset circuit that resets the the card when power is applied to the chassis. This reset may also be activated from the remote chassis by writing a "1" to bit 7 of the REMOTE NODE COMMAND REGISTER. After triggering the reset, your program should wait one second before starting another remote access or VMEbus cycle.

If the SYSRESET jumper in the SYS jumper block is installed, this reset will also drive the VMEbus global reset signal (section 2.1.1.)

Writing a "O" to this bit will clear bit 7 of the REMOTE NODE STATUS REGISTER, which is set when RESET REMOTE ADAPTOR BOARD or any VMEbus global reset occurs.

CLEAR PGMD-TO-AT INTERRUPT ON VMEbus CARD (BIT 6): If a VMEbus processor has set the "programmed to PC/AT" interrupt flip-flop on the Adaptor card in its chassis, a PC/AT processor can clear it by writing a "1" to bit 6 of the REMOTE NODE COMMAND REGISTER.

SEND PGMD-TO-VME INTERRUPT TO VMEbus CARD (BIT 5): If a PC/AT processor wants to send a "programmed to VMEbus" interrupt to the VMEbus chassis, it does so by writing a "1" to bit 5 of the REMOTE NODE COMMAND REGISTER. Writing a "0" will clear the interrupt.

LOCK VMEbus (BIT 4): Writing a "1" to bit 4 in the REMOTE NODE COMMAND REGISTER sets the LOCK BUS flip-flop. If the LOCK BUS flipflop is set, the address strobe signal on the VMEbus will remain active after the first PC/AT access to the VMEbus. This prevents any other VMEbus master from using the VMEbus and permits the PC/AT to convert a read operation followed by a write operation into an atomic read-modify-write on the VMEbus. To use this function, the PC/AT should should set the LOCK BUS flip-flop, then perform a VMEbus read followed by a VMEbus write (to the same address), and then, as quickly as possible, clear the bus lock flip-flop.

This function is useful in a multi-processor application where it is common for processors to signal availability of a resource through an indivisible read-modify-write semaphore operation.

The LOCK BUS flip-flop may also be used by the PC/AT to make PC/AT accesses to dual-port RAM indivisible.

Read-modify-write operations (such as TEST and SET) from the VMEbus to dual-port RAM are automatically indivisible.

USE ADDRESS PAGE REGISTER (BIT 3): Bus masters may address VMEbus RAM or dual-port RAM through either of two techniques: direct mode or page mode. In direct addressing mode, dual-port RAM or VMEbus RAM are addressed by setting a "window" in address space as large as the block of RAM to be addressed. Page mode, however, permits addressing of all dual-port and VMEbus RAM locations through a variable-size window in PC/AT address space. The upper sixteen VMEbus address bits in page mode are provided by an sixteen-bit page register located on the VMEbus Adaptor card. The remaining sixteen lower address bits are provided by the address offset in the PC/AT memory window.

If the PAGE MODE bit is set, address bits A16 through A31 to the dual-port RAM or VMEbus RAM are provided by the PAGE REGISTER. Direct mode operation occurs if the PAGE MODE bit is a zero. The address bias jumpers are ignored if PAGE MODE is selected.

IACK READ MODE ADDRESS BITS (BITS 2-0): When a PC/AT processor wishes to acknowledge an interrupt on the VMEbus backplane using the IACK READ feature of the Adaptor, it must also present to the VMEbus backplane a three-bit address with the same value as the interrupt level (1-7) being acknowledged. IACK READ MODE ADDRESS BITS 2-0 are a three-bit register which the PC/AT writes to before performing an IACK READ. The contents of these three register bits are gated to VMEbus address lines A03, A02, and A01 during the IACK READ cycle.

See the information on IACK READ in section 5.2.6.

## 5.2.2 Remote Node Command Register 2

Remote node command register 2 is a read/write register.

BIT	FUNCTION
7	not defined - must be 0
6	not defined - must be 0
5	not defined - must be 0
4	not defined - must be 0
3	PAGE SIZE SELECT BIT 3
2	PAGE SIZE SELECT BIT 2
1	PAGE SIZE SELECT BIT 1
0	PAGE SIZE SELECT BIT O

This register controls the size of the page window (when PAGE MODE is selected) on the Adaptor card. The default page window size (after the Adaptor card is reset) is 64K bytes. The page size select bits are set as follows:

Page Size Select Bit:	3	2	1	0	Page Size
	0	0	0	0	64K byte
	0	0	0	1	128K byte
	0	0	1	1	256K byte
	0	1	1	1	512K byte
	1	1	1	1	1M byte

NOTE: For whatever page size used, the dual-port and remote RAM windows (jumper-selected on each card) must start at an address that is an even multiple, starting from address zero, of the selected page window size. Thus, for a 64K byte page window size, the window must start on a 64K byte address in the address space; for a 128K byte page window, the window must start on a 128K byte address, and so on.

#### 5.2.3 Remote Node Status Register

The remote node status register is a read-only register.

BIT	FUNCTION
	"1" = VMEbus was reset
6	
5	"1" = PGMD-TO-VME interrupt flip-flop on VME card is set
4	"1" = LOCK BUS not set (this is the inverted
	state of the lock bus flip-flop)
3	"1" = use address page register
	IACK READ MODE ADDRESS BIT 2
1	"1" = PGMD-TO-AT interrupt flip-flop on VME card is set
0	IACK READ MODE ADDRESS BIT 0

REMOTE NODE STATUS REGISTER bit 7 is a "1" when any VMEbus reset or VMEbus Adaptor card reset has occurred. The bit may be cleared by writing a "0" to bit 7 of the REMOTE NODE COMMAND REGISTER.

REMOTE NODE STATUS REGISTER bit 5 is a "1" when the "programmed to VMEbus" interrupt flip-flop on the VMEbus Adaptor card is set.

REMOTE NODE STATUS REGISTER bit 4 shows the <u>inverted</u> state of the LOCK BUS flip-flop controlled by bit 4 of the REMOTE NODE COMMAND REGISTER.

REMOTE NODE STATUS REGISTER bit 3 shows the state of the USE ADDRESS PAGE REGISTER bit (bit 3) in the REMOTE NODE COMMAND REGISTER.

REMOTE NODE STATUS REGISTER bit 1 is a "1" when the "programmed to PC/AT" interrupt flip-flop on the VMEbus Adaptor card is set.

REMOTE NODE STATUS REGISTER bits 2, 6, and 0 show the state of the IACK READ MODE ADDRESS BITS 2-0 written to the REMOTE NODE COMMAND REGISTER. These bits are scrambled only to maintain compatibility with previous Adaptor models.

## 5.2.4 Remote Node Page Registers

The remote node page registers are read/write registers that may be accessed together as a word or individually as bytes.

BIT 7 6 5 4 3 2 1 0	VMEbus VMEbus VMEbus VMEbus VMEbus	ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS	BIT BIT BIT BIT BIT BIT	30 29 28 27 26 25	_	ADDRESS	PAGE	HIGH
7 6 5 4 3 2 1 0	VMEbus VMEbus VMEbus VMEbus VMEbus	ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS ADDRESS	BIT BIT BIT BIT BIT BIT	22 21		ADDRESS	PAGE	LOW

These registers are gated to the address bus on remote bus cycles when the USE ADDRESS PAGE REGISTER command bit is set. The two registers together provide the upper sixteen address bits of a 32-bit dual-port or remote RAM address. The ADDRESS PAGE LOW REGISTER provides address bits A16-A23 when accessing memory in 24-bit or 32bit mode; the ADDRESS PAGE HIGH REGISTER provides address bits A24-A31 when accessing memory in 32-bit mode, and is ignored in 24-bit mode.

# 5.2.5 Remote Address Modifier Register

VMEbus addresses consist of 16, 24, or 32 address bits and a six-bit address modifier. The address modifier is a code designating the type of access (short, standard, or extended; non-privileged or supervisory) to occur on the VMEbus. VMEbus devices must receive their correct address modifier as well as the correct address or they will not respond to an access.

The REMOTE ADDRESS MODIFIER REGISTER is a read/write register that allows a local processor to set or change the address modifier for all accesses through the Adaptor to the VMEbus backplane.

BIT	FUNCTION
7	not defined - must be 0
6	not defined - must be O
5	VMEbus ADDRESS MODIFIER BIT 5
4	VMEbus ADDRESS MODIFIER BIT 4
3	VMEbus ADDRESS MODIFIER BIT 3
2	VMEbus ADDRESS MODIFIER BIT 2
1	VMEbus ADDRESS MODIFIER BIT 1
0	VMEbus ADDRESS MODIFIER BIT 0

Definitions for the various address modifiers may be found in any published VMEbus specification. See section 4.

## 5.2.6 IACK READ Register

A PC/AT processor can instruct the Adaptor to perform an interrupt acknowledge cycle on the VMEbus by reading from the IACK READ REGISTER. The Adaptor converts a read from these registers (in the PC/AT chassis) into a remote interrupt acknowledge cycle (on the VMEbus chassis), activating the VMEbus IACK line and presenting a three-bit IACK code corresponding to the interrupt level being acknowledged. When the VMEbus interrupting device sees the acknowledgement, it posts an interrupt vector on the VMEbus which is returned to the PC/AT processor performing the IACK READ (as data from that read) in the IACK READ REGISTER.

The IACK READ REGISTER is a read-only register that may be addressed as a word or as two bytes. However, note that two IACK READs would cause two IACKs to occur; the second read would induce a VME bus error.

The three-bit IACK code presented by the VMEbus Adaptor card may be modified by writing to the REMOTE NODE COMMAND REGISTER 1 bits 2-0. See section 5.2.1.

## 5.3 VMEbus Adaptor Board Registers

The following table shows the location and definition of the I/O registers on the VME Adaptor card. These registers are addressed by processors on the VMEbus.

VMEbus I/O ADDR	WRITE FUNCTION	READ FUNCTION
I/O LO + O (hex)	reserved	reserved
I/O LO + 1	LOCAL NODE COMMAND REG	LOCAL NODE COMMAND REG
I/O LO + 2	reserved	reserved
I/O LO + 3	reserved	LOCAL NODE STATUS REG
I/O LO + 4	reserved	reserved
I/O LO + 5	reserved	reserved
I/O LO + 6	reserved	reserved
I/O LO + 7	INTERRUPT VECTOR REG	INTERRUPT VECTOR REG

I/O addresses (I/O LO + 8) through (I/O LO + 1F) are reserved and the user must not attempt to access these addresses.

I/O LO + 8 through reserved reserved I/O LO +1F (hex)

#### 5.3.1 Local Node Command Register

The VMEbus local node command register is a read/write register.

BIT			FUNCTION
			not defined - must be 0
6	"1"	=	clear PGMD-TO-VME interrupt flip-flop
	"0"	=	no action
5	"1"	=	set PGMD-TO-AT interrupt flip-flop
	"0"	=	clear PGMD-TO-AT interrupt flip-flop
4			not defined - must be O
3			not defined - must be O
2			not defined - must be O
1			not defined - must be O
0			not defined - must be 0

CLEAR PGMD-TO-VME INTERRUPT (BIT 6): Writing a "1" to this bit clears the "programmed to VME" interrupt flip-flop. Writing a "0" to this bit has no effect.

SET PGMD-TO-AT INTERRUPT (BIT 5): Writing a "1" to this bit sets the "programmed to PC/AT" interrupt flip-flop. Writing a "0" to this bit will clear the flip-flop.

## 5.3.2 Local Node Status Register

The local node status register is a read-only register.

BIT		FUNCTION
7		not defined - reserved for future use
6		not defined - reserved for future use
5	"1" =	PGMD-TO-VME interrupt flip-flop is set
4		not defined - reserved for future use
3		not defined - reserved for future use
2		not defined - reserved for future use
1	"1" =	PGMD-TO-AT interrupt flip-flop is set
0	"1" =	Remote bus power off or I/O cable is off

LOCAL NODE STATUS REGISTER bit 5 is a "1" when the "programmed to VME" interrupt flip-flop has been set by the PC/AT.

LOCAL NODE STATUS REGISTER bit 1 is a "1" when the "programmed to PC/AT" flip-flop on this Adaptor card is set.

LOCAL NODE STATUS REGISTER bit 0 is a "1" if the PC/AT power is off or if the I/O cable is not connected.

# 5.3.3 Interrupt Vector Register

This read/write register holds the interrupt vector transmitted to a VMEbus processor when that processor acknowledges an interrupt from the VMEbus Adaptor card. This vector is the response to a VMEbus IACK cycle initiated by a "programmed interrupt to VMEbus".

The INTERRUPT VECTOR REGISTER is preset to "FF" at power-on time.

This register is read from and written to by a VMEbus processor --NOT by any PC/AT processor. PC/AT interrupt acknowledgement on the VMEbus is performed with the IACK READ command (see section 5.2.6).

## 5.4 Setup Sequence

If your application uses the Adaptor card status or control registers, it is necessary to execute a simple setup procedure to initialize the card. The program would use the following sequence:

- (1) DO A PC/AT I/O READ from the local node status register to awaken the PC/AT Adaptor card. Disregard the data.
- (2) DO A PC/AT I/O READ from the remote node status register to flush interface errors caused by the power-on transition.
- (3) DO A PC/AT I/O READ from the local node status register to test if the VMEbus chassis has power on.
- (4) DO A PC/AT I/O WRITE with data "80" (hex) to the local node command register to clear status register power-on errors.
- (5) DO A PC/AT I/O WRITE with data "3D"(hex) (or whatever other address modifier required) to the remote address modifier register to prepare the VMEbus Adaptor card for PC/AT remote RAM accesses.
- (6) DO A PC/AT I/O READ from the local node status register to see that no interface errors occurred and that the preceding steps were successful.

## 5.5 Testing the Adaptor

The debug or monitor facilities provided with many processors may be useful to test the Adaptor link between the two systems. You should be able to display memory and modify memory in the other system just as though it were memory on the local system chassis. This is a good way to initially test the Adaptor cards and the configuration jumpers. Another good test is to execute a memory diagnostic in the PC/AT chassis that tests memory in the VMEbus chassis.

### APPENDIX -- PROGRAM LISTING

BASIC PROGRAM LISTING

10 ATCMD=512:REM 512 = HEX 0200, THE FACTORY I/O LO VALUE 20 ATSTAT=ATCMD+2 30 VMECMD=ATCMD+8 40 VMESTAT=ATCMD+8 50 VMEPAGE=ATCMD+10 60 VMEAM=ATCMD+13 70 VMEIACK=ATCMD+14 100 REM SETUP THE ADAPTOR CARDS 110 STATO=INP(ATSTAT): REM TURN ON THE Bit 3 CARD 120 STATO=INP(VMESTAT): REM FLUSH ANY POWER UP ERRORS 125 STATO=INP(ATSTAT):REM TEST FOR VME POWER ON 130 IF (STATO AND 1) <> 0 THEN PRINT "POWER IS OFF OR CABLE DISCONNECTED": END 140 OUT ATCMD, 128: REM RESET ANY STATUS REGISTER ERRORS 150 OUT VMEAM, 61:REM LOAD ADDRESS MODIFIER 3D 160 STATO=INP(ATSTAT):REM READ AT STATUS AGAIN 170 IF (STATO AND 197) <> 0 THEN PRINT "SETUP STATUS ERROR":GOTO 300 180 REM THE ABOVE LINE TESTED FOR STATUS BITS 7,6,2,AND 0. 190 PRINT "SETUP OK" 200 END 300 IF (STATO AND 128) <> 0 THEN PRINT "INTERFACE PARITY ERROR" 310 IF (STATO AND 64) <> 0 THEN PRINT "VME BUS ERROR" 320 IF (STATO AND 4) <> 0 THEN PRINT "INTERFACE TIMEOUT" 330 IF (STATO AND 1) <> 0 THEN PRINT "POWER IS OFF OR CABLE DISCONNECTED" 340 END

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2		PAGE
3	TITLE SETUP	
4	;	
5	;	
6	SUBTIL DEFINI	TIONS OF MACROS
7		.SALL
;Don't expand macros		
8	;	
9	;	
10	DISPLAY	MACRO TEXT
11		MOV
DX,OFFSET TEXT ; Point to message to p	print	
12		MOV AH,9
;Function selected = console output		
13		DOSCALL
;Invoke DOS to display message		
14		ENDM
15	;	
16	DOSCALL	MACRO
17		INT 21H
Request DOS service, id in AH		
18		ENDM
19	;	
20	;	
21	SUBTTL DESCRI	PTION OF THE
STACK SECMENT 22		
	;	
23 0000 STACK 'STACK'	STACK	SEGMENT PARA
24 0000 40 [		<b>DD</b> (4
DUP('STACK ')		DB 64
25 53 54 41 43		
26 4B 20 20 20		
27 ¥2 20 20 20		
28		
29 0200	STACK	ENDS
30	;	
31	, SUBTTL DESCRIP	TION OF THE
data workarea		
32	;	
33 0000	WORKAREA	SEGMENT PARA
PUBLIC 'DATA'		
34	;	
35 0000 ????		DW ?
SCRATCH PAD LOCATION FOR STATUS		
36	;	
37 0002 53 45 54 55 50 2		O DB
SETUP OK '		
38 4F 4B 20		
39 OOOB OD		DB ODH
;CR		0//
•		

Appendix

:LF     41   000 24   DB '\$'     :Terminator   2   :     42   :   .     43   000 0 4F 57 45 52 20   MSG01   DB     'POWER IS OFF OR THE I/O CABLE IS DISCONNECTED'   .   .     44   49 53 20 4F 46 46   .   .     45   20 4F 52 20 54 48   .   .     46   45 20 49 2F 4F 20   .   .     47   43 41 42 4C 45 20   .   .     48   49 53 20 44 49 53   .   .     49   43 4F 4E 4E 45 43   .   .     50   54 45 44 20   .   .     51   003c   0D 0A   DB     0DH, OAH   .   .   .     52   003E 24   .   .   .     53   .   .   .   .     54   .   .   . <th>40</th> <th>000C</th> <th>QA</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th>DB</th> <th>OAH</th>	40	000C	QA								DB	OAH
: Terminator     42   :     43   000E   50   4F   57   45   52   20   MSG01   DB     'POWER IS OFF OR THE I/O CABLE IS DISCONNECTED '     44   49   53   20   4F   66     45   20   4F   52   20   54   48     46   45   20   4F   49   53   48   49   53   20   44   49   53     47   43   41   42   42   45   20   48   49   53   20   44   49   53     48   49   53   20   44   49   53   44   49   53     49   43   4F   4E   45   43   50   51   003c   0D   0A   DB     51   003c   0D   0A   DB   DB   '\$'     52   003E   24   D   DB   '\$'	;LF											
42   ;     43   000E   50   4F   57   45   52   20   MSG01   DB     'POWER   IS   OFF OR THE   I/O   CABLE IS DISCONNECTED '     44   49   53   20   4F   46   46     45   20   4F   52   20   54   48     46   45   20   4F   50   47   43   41   42   42   45   20     48   49   53   20   44   49   53   44   49   53     49   43   4F   4E   45   43   50   54   45   43     50   54   45   44   20   51   003C   0D   0A   DB     0DH, OAH   E   52   003E   24   DB   '\$'	41	000D	24								DB	'\$'
43   000E   50   4F   57   45   52   20   MSG01   DB     'POWER IS OFF OR THE I/O CABLE IS DISCONNECTED '   44   49   53   20   4F   56   45     44   49   53   20   4F   46   46   45     45   20   4F   52   20   54   48   46   45   20   47   43   41   42   42   45   20   48   49   53   20   44   49   53   44   49   53   44   49   53   44   49   53   44   49   53   44   49   53   44   49   53   44   49   53   44   49   53   50   54   45   44   20   51   003C   0D   0A   DB   0H   0H   1H   <	;Termina	tor										
'POWER IS OFF OR THE I/O CABLE IS DISCONNECTED'     44   49 53 20 4F 46 46     45   20 4F 52 20 54 48     46   45 20 49 2F 4F 20     47   43 41 42 4C 45 20     48   49 53 20 44 49 53     49   53 4F 4E 4E 45 43     50   54 45 44 20     51   003C   0D     003L   DB     52   003E 24   54	42							;				
44   49   53   20   4F   46     45   20   4F   52   20   54   48     46   45   20   49   2F   4F   20     47   43   41   42   45   20     48   49   53   20   44   49   53     49   43   4F   4E   45   43     50   54   45   44   20   51     51   003c   0D   0A   DB     0DH, OAH   DB	43	000E	50	4 F	57	45	52	20		MSG01		DB
45   20   4F   52   20   54   48     46   45   20   49   2F   4F   20     47   43   41   42   42   45   20     48   49   53   20   44   49   53     49   43   4F   4E   45   43     50   54   45   44   20   DB     51   003c   0D   0A   DB     ODH, OAH   DB< '\$'	'POWER IS	SOFFO	x The	: 1/0	CAR	BLE IS	S DIS	CONNECT	ED '			
46   45   20   49   2F   4F   20     47   43   41   42   42   45   20     48   49   53   20   44   49   53     49   43   4F   4E   45   43     50   54   45   44   20     51   003C   0D   0A   DB     ODH, OAH   DB< '\$'	44		<b>49</b> 53	20	4F 4	6 46						
47   43   41   42   42   45   20     48   49   53   20   44   49   53     49   43   4F   4E   45   43     50   54   45   44   20   DB     51   003c   0D   0A   DB     0DH, OAH   DB	45		20 4F	52	20 5	54 48						
48   49   53   20   44   49   53     49   43   4F   4E   45   43     50   54   45   44   20     51   003C   0D   0A   DB     ODH, OAH   DB     52   003E   24   DB   '\$'	46		45 20	49	2F 4	F 20						
49   43 4F 4E 4E 45 43     50   54 45 44 20     51   003C   0D 0A     0DH, 0AH   DB     52   003E 24   DB '\$'	47		43 41	. 42	4C 4	5 20						
50 54 45 44 20   51 003c 0D 0A DB   ODH, OAH 52 003E 24 DB '\$'	48		49 53	20	44 4	9 53						
51     003C     0D     DB       ODH, OAH     DB     '\$'	49		43 4F	' 4E	4E 4	5 43						
ODH, QAH 52 003E 24 DB '\$'	50		54 45	44	20							
52 003E 24 DB '\$'	51	003C	c	D	0A							DB
· · · · ·	odh, qah											
;Terminator	52	003E	24								DB	'\$'
	;Terminat	tor										
53 ;	53							;				

The IBM Personal Computer MACRO Assembler 05-29-86 PAGE 1-2 SETUP

DESCRIPTION OF THE DATA WORKAREA

.

54			PAGE	
55	003F	49 4E 54 45 52 46	MSG02	DB
INTERFA	ce par	ITY ERROR ', ODH, OAH		
56		41 43 45 20 50 41		
57		52 49 54 59 20 45		
58		52 52 4F 52 20 OD		
59		QA.		
60	0058	24	DB	'\$'
61		;		
62	0059	56 4D 45 20 42 55 MSG03	DB	'VME
BUS ERRC	R',OD	1, OAH		
63		53 20 45 52 52 4F		
64		52 20 0D QA		
65	0069	24	DB	'\$'
66		;		
67	006A	<b>49 4E 54 45 52 46</b>	MSG04	DB
' INTERFA	CE TIM	20UT', ODH, QAH		
68		41 43 45 20 54 49		
69		4D 45 4F 55 54 OD		
70		QA		
71	007d	24	DB	'\$'
72		;		
73	007E	53 45 54 55 50 20	MSG05	DB
'SETUP S	TATUS	ERROR ', ODH, OAH		
74		53 54 41 54 55 53		
75		20 45 52 52 4F 52		
76		20 OD OA		
77	0093	24	DB	'\$'
78		;		
79	0094	WORKAREA	ENDS	

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The IEM Personal Computer MACRO Assembler 05-29-86 PAGE 1-3 SETUP

DESCRIPTION OF THE DATA WORKAREA

80		DAGE	
81		PAGE	
82	; SUBTTL	MAIN I	TATE
PROGRAM	308111	PRIN I	1146
83			
84 0000	; CSEG	CEVMENT	r Para
PUBLIC 'CODE'	CSEG	DEAD-IEIV.	
85	;		
86 0000	, START	PROC	FAR
87	SIARI	FRAC	ASSUME
CS:CSEG, DS:NOTHING, SS:STACK, ES:NOTHING			ASSUME
88	•		
89 = 0200	; PCPORT		EQU
00200H ;ADAPTOR I/O PORT ADDRE			FÕO
90 =	ATCMD	FOU	
PCPORT ; THE AT COMMAND REGISTE		EQU	
91 = 0202	ATSTAT		FOU
PCPORT + 2 ; THE AT STATUS REGISTER			EQU
92 = 0208	VMECMD		FOU
PCPORT + 8 ; THE VME COMMAND REGIST			EQU
		m	FOU
	VMESTA	T	EQU
PCPORT + 8 ;THE VME STATUS REGISTE		_	
94 = 020A	VMEPAG	E	EQU
PCPORT + OAH ; THE VME ADDRESS PAGE RI			
95 = 020D	VMEAM		EQU
PCPORT + ODH ; THE VME ADDRESS MODIFIN			
96 = 020E	VMEIAC	ĸ	EQU
PCPORT + OEH ; THE VME LACK READ ADDRI			
97	;		~
98 0000 1E		PUSH	DS
;Set return segment addr to stack 99 0001 2B CO		SUB	NY NY
		505	AX,AX
;Clear a reg 100 0003 50		THE KMI	736
		PUSH	AX
;Put zero return addr to stack			MON
101 0004 B8 R			MOV
AX, WORKAREA			DO 31
102 0007 8E D8		MOV	DS,AX ASSUME
103			ASSUME
DS:WORKAREA	_		
104	;		
105	;		NOT
106 0009 BA 0202	_		MOV
DX,ATSTAT ;Setup to enable adaptor	7		
107 000C EC		IN	AL, DX
;Enable adaptor			
108	;		1007
109 000D BA 0208			MOV
DX, VMESTAT ; Setup to do I/O to flus	ai power up erro:		AL DY
110 0010 EC		IN	AL, DX
;Flush power up errors			

Appendix

111 ; 0011 BA 0202 MOV 112 DX,ATSTAT ;Setup to test for power on 0014 EC IN AL, DX 113 ;read AT status 114 0015 24 01 AND AL,01H ;Test for power off bit 115 0017 74 OA JZ START1 ;Continue if power on 116 DISPLAY MSG01 ;Display power off message 0020 EB 61 90 117 JMP EXIT ; and quit 118 ; 119 0023 BA 0200 START1: MOV DX,ATCMD ;Setup to reset status errors 120 0026 B0 80 MOV AL,080H ; Reset status errors bit 121 0028 EE OUT DX,AL ; Reset status errors 122 ; 123 0029 BA 020D MOV DX,VMEAM ;Setup to load address modifier code 124 002C BO 3D MOV AL,03DH ; address modifier code = 3D 125 002E EE OUT DX, AL ; load the address modifier 126 ; 127 002F BA 0202 MOV DX,ATSTAT ;Setup to read AT status IN 128 0032 EC AL, DX ; Read AT status 129 0033 24 C5 AND AL, OC5H ; test for errors 130 0035 74 45 JZ START2 ; exit if no errors 131 ;

The IBM Personal Computer MACRO Assembler 05-29-86 PAGE 1-4 SETUP

MAIN LINE PROGRAM

122			
132		PAGE	
133 0037 A3 0000 R STATUS.AX :save status			MOV
STATUS,AX ;save status 134			_
;Display status error message		DISPLAY MSGC	5
135 0041 A1 0000 R			
AX, STATUS ; recover STATUS			MOV
136 0044 24 80			
AL,080H ;Test for Parity e	m		AND
137 0046 74 07		JZ ERR	1
;Jump if no parity error			-
138		DISPLAY MSGO	2
;Display parity error message		DIGLINI (1960	6
139 004F A1 0000 R	ERR1:	MOV	
AX,STATUS ;recover status			
140 0052 24 40			AND
AL,040H ;Test for bus erro	r		
141 0054 74 07		JZ ERR	2
;Jump if no buss error			-
142		DISPLAY MSGO	3
;Display bus error message			
143 005D A1 0000 R	ERR2:	MOV	
AX,STATUS ; recover status			
144 0060 24 04			AND
AL,04H ;Test for Timeout			
145 0062 74 07		JZ ERR3	3
;Jump if no timeout error			
146		DISPLAY MSG04	ł
;Display timeout error message			
147 006B A1 0000 R	ERR3:	MOV	
AX,STATUS ;recover status			
148 006E 24 01			AND
AL,01H ;test for power of:	f		
149 0070 74 11		JZ EXIT	•
;Exit			
150		DISPLAY MSG01	
;Power must be off			
151 0079 EB 08 90		JMP EXIT	
152	;		
153 007c	START2:	DISPLAY MSGOO	•
;Display setup ok message			
154 0083 св	EXIT:	RET	
FAR RET TO DOS			
155 0084	START	ENDP	
156 0084	CSEG	ENDS	
157		END START	

The IBM Personal Computer MACRO Assembler 05-29-86 PAGE Symbols-1

SETUP

#### Macros:

Name										Length				
DISPLAY.	•		•	•		•		•	•	•	•		0005	
DOSCALL.		•			•	•			•		•		0002	

#### Segments and groups:

Name	Size	align	combine class
CSEG	0084	PARA	PUBLIC
STACK	0200	PARA	STACK
'STACK' WORKAREA	0094	PARA	PUBLIC

#### Symbols:

.

Name	Туре	Value	Attr	
ATCMD	Alias	PCPORT		
ATSTAT	Number	0202		
ERR1	l near	004F	CSEG	
ERR2	l near	005d	CSEG	
ERR3	l near	006B	CSEG	
EXIT	l near	0083	CSEG	
MSG00	L BYTE	0002	WORKAREA	
MSG01	L BYTE	000E	WORKAREA	
MSG02	L BYTE	003F	WORKAREA	
MSG03	L BYTE	0059	WORKAREA	
MSG04	L BYTE	006a	WORKAREA	
MSG05	L BYTE	007E	WORKAREA	
PCPORT	Number	0200		
START	F PRC	c	0000	CSEG
Length =0084				
START1	l near	0023	CSEG	
START2	l near	007C	CSEG	
STATUS	L WORD	0000	WORKAREA	
VMEAM	Number	020D		
VMECMD	Number	0208		
VMEIACK	Number	020E		
VMEPAGE	Number	020A		
VMESTAT	Number	0208		

Warning Severe

Errors Errors

0 0

Appendix