American National Standard

for information systems – interface between rigid disk drive(s) and host(s)

ANSI X3.101-1984

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X3.101-1984

American National Standard for Information Systems – Interface between Rigid Disk Drive(s) and Host(s)

Secretariat

Computer and Business Equipment Manufacturers Association

Approved October 17, 1983

American National Standards Institute, Inc

Abstract

Strict mechanical, electrical, and functional specifications are defined for attaching disk drive(s) to their host(s). Certain capabilities are defined as extensions. This interface will facilitate the interconnection of disk drive(s) to the host(s) and thus provide a common interface specification for both.

American National Standard

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Foreword (This Foreword is not part of American National Standard X3.101-1984.)

This standard was developed to specify a common interface definition and to enumerate common optional features and specify connector pin assignments and functional protocols of these options. Physical characteristics of the disk, recording methods, and formats for interchange are beyond the scope of this standard.

Development of the rigid disk drive standard began in mid-1979 at the urging of several drive manufacturers.

Public announcements were made and letters were sent out to disk drive/host manufacturers and users to form a substantial membership body to write the standard. The participants on the committee were drawn from many sectors of the industry: drive manufacturers, host manufacturers, government, users, and systems houses. The observers, whose number approached 150, received a full mailing after each meeting and some even participated in the working discussions via mail presentations.

The standard was drafted in a relatively short time due to the clear objectives, the force of the market, and the strong commitment of the large active membership. The group not only met for the usual bimonthly meetings, but added working meetings in between.

The resultant interface standard is an original design by the committee based upon proven techniques. The standard was developed with a minimum mandatory set of requirements for low cost. It also includes a well-defined, but optional, set of extensions for future drives and current drives with enhanced features.

While work was in progress, a 5-1/4-inch rigid disk drive was announced. The committee decided to drop the words, *8 inch,* from the title because they believed that this new standard was ideal for all sizes of rigid disk drives.

The document was approved by the Task Group X3T9.3 on Device-Level Interfaces in October 1980. At that time, about six manufacturers of drives and hosts had announced that they intended to use the interface as their standard.

The trade press has done an excellent job of keeping the industry informed about the committee and its work. It has also been helpful in encouraging a professional interest in the committee's work, thus facilitating the progress of the development of the standard.

Suggestions for improvement of this standard will be welcome. They should be sent to the Computer and Business Equipment Manufacturers Association, 311 First Street, NW, Suite 500, Washington, D.C. 20001.

This standard was processed and approved for submittal to ANSI by American National Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not necessarily imply that all committee members voted for its approval. At the time it approved this standard, the X3 Committee had the following members:

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Task Group X3T9.3 on Device-Level Interfaces, which developed this standard, had the following members:

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American National Standard for Information Systems - Interface between Rigid Disk Drive(s) and Host(s)

1. Scope

This standard applies to rigid disk drive(s) and defines the necessary functional and electrical requirements (including logic signals) and the mechanical requirements of the interface for connection of conforming rigid disk drive(s) to host system(s). This standard is distinct from a specification in that it delineates a minimum set of requirements consistent with compatibility and interchangeability at the interface level.

This standard will facilitate the interconnection of rigid disk drive(s) to host system(s) by a user that has available the technical capabilities to verify and test performance up through the functional level. The user should have the capability to specify the overall system hardware and software that will be unique for a particular device and host combination.

This standard by itself does not guarantee plug compatibility of devices meeting this standard. To obtain total interchangeability of devices an operational specification must be defined. Neither the operating specification nor the power requirements are defined by this standard.

This standard was developed for the 8-inch rigid disk drive, but its use is not limited to 8-inch rigid disk drives.

This standard does not apply where no clear separation exists between the device and the host.

This standard does not prescribe the magnetic encoding or decoding method, the recording techniques, nor the format used to write or read data, but allows the reporting of all of the above. Unique characteristics offered by a vendor are allowed where specified in the standard.

The design of this interface:

(1) Provides addressability of up to eight devices

(2) Provides capability for both variable and fixed sector sizes

(3) Provides transfer of data across the interface at up to 10 megabits per second

(4) Provides daisy-chain configuration utilizing a 50-wire flat ribbon cable

(5) Supports a radial attention and selection capability through the daisy chain bus

(6) Permits self-configuration of the system and self definition of the individual devices

(7) Provides extensive error reporting and status information

(8) Allows for the capability of enhancement beyond the current range of known devices

(9) Includes a command set that has been divided into mandatory and optional functions to allow for different levels of implementation

This standard is intended for low-cost implementations and offers a high degree of flexibility.

2. Definitions

mandatory. The functions labeled mandatory shall be included in all devices and hosts. They shall be implemented as defined in this standard.

optional. The features labeled optional may be implemented in the host, the device, or both, as defined in this standard. If the feature is included but the implementation can not be exactly the same as defined in this standard, then the feature shall be considered vendor unique. (See definition.)

state nomenclature. The nomenclature used to define voltage levels and signal states on the interface and used to define logical states internally to the device and their correlation is defined in Table 1.

vendor unique. The features labeled vendor unique may be defined by each vendor as required. Caution should be exercised in defining and using these features since they are not standard between vendors nor have they been adopted as American National Standards.

Table 1

State Nomenclature

Interface			Internal		
Voltage Level		Signal State	Logical State		Logical Transition
Single Ended	Differential		Tables	Text	
LOW	+ line ≥ - line	Active	1	ONE	SET = X to ONE
HIGH	- line > + line	Inactive	0	ZERO	RESET = X to ZERO

3. Physical Characteristics

This interface standard defines the configuration classes that cover the use of cable types and line driver/receiver types as summarized in Table 2. The classes are defined in response to perceived application requirements for the wide range of applications within which this interface is expected to be used.

Unless otherwise indicated, all values of impedance, voltage or current in this section are specified with a tolerance of +/- 5 percent.

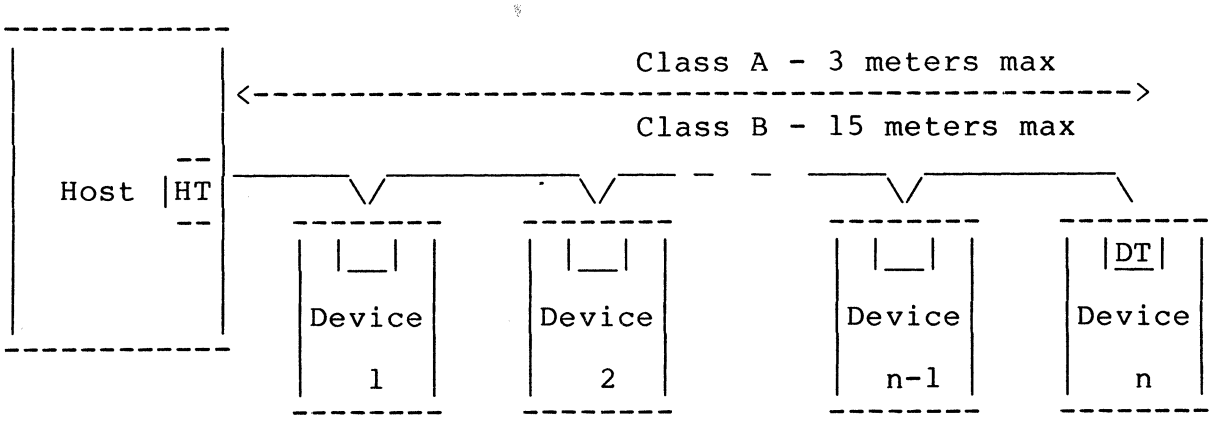
3.1 Cabling Configuration. A maximum of eight units shall be connected to the host by a daisy-chain signal cable configuration as shown in Figure 1.

Delivery of primary power (ac, dc, or both) shall not be accomplished on the interface cable. A separate dc common (ground) may be provided. Specifications for power supply cabling and grounding requirements are not a subject of this standard. Refer to vendor specifications for power/ground information.

Table 2

Interface Configuration

Cable Type	Connection Type	Driver/Receiver Type	Maximum Length (meters)	Configuration Class
Flat ribbon	2x25 Pin header	Three-state and open collector driver TTL receiver with hysteresis	3	A
Flat ribbon	2x25 Pin header	Transceiver with open collector driver and high-threshold receiver	15	B



NOTE: HT = Terminator installed at the host;
DT = Terminator installed at the last device.

Figure 1

Interface Configuration

The configurations permitted by this standard are intended to permit selection of the most cost-effective alternative for different market environments.

3.1.1 Class A Configuration. A 50-conductor flat ribbon cable for use internal to the equipment cabinets shall be used. The maximum accumulated cable length from host to terminator in the last unit shall be 3 meters.

3.1.2 Class B Configuration. A 50-conductor flat ribbon cable for use internal to the equipment cabinets shall be used.

For use external to the equipment cabinets, a shielded flat ribbon cable jacket is needed to meet EMI/RFI requirements. The shielded flat ribbon cable jacket shall be connected at both the host and the device end to pin number one.

The maximum accumulated cable length from host to terminator in the last unit shall be 15 meters.

3.2 Connector Specification. The connector type shall be the 50-pin, two-row inline, flat-ribbon rectangular connector illustrated in Figures 2 and 3 with the dimensions as specified in those figures.

Pin assignments and signal nomenclature are illustrated in Table 3. Termination of the individual cable lines shall be at the host and at the last device according to the electrical requirements of 3.4 and 3.5.

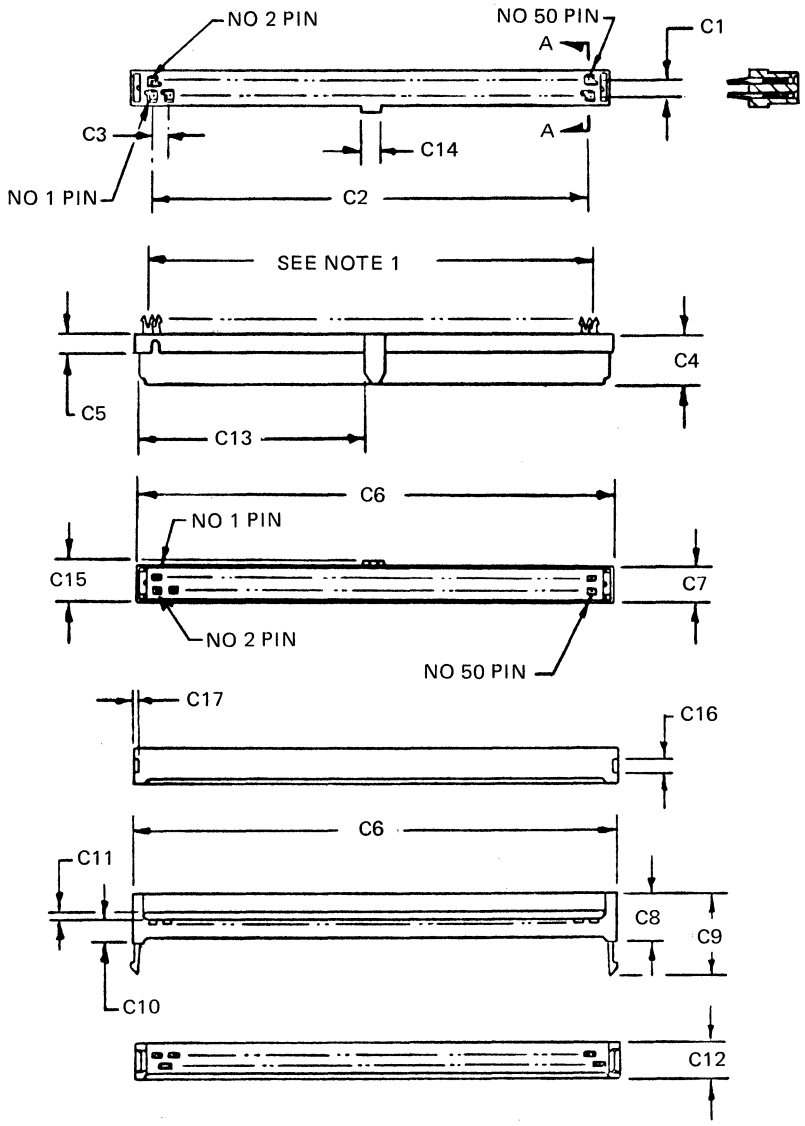
The cable plug (Figure 2) shall be polarized and polarization shall be done with a center top tab.

3.3 Cable Characteristics. The flat ribbon cable or equivalent shall consist of 50 conductors of 28 AWG. The characteristic impedance of the lines shall be 100 ohms +/- 10 percent. Conductor spacing shall be 1.27 millimeters (0.050 inch) center-to-center to provide for mechanical termination. Additionally, the flat ribbon cable shall be marked in such a way as to identify line number one (pin 1).

If the cable contains a shield ground, it shall be connected to pin number one of the interface connector.

3.4 Electrical Characteristics, Class A Configuration

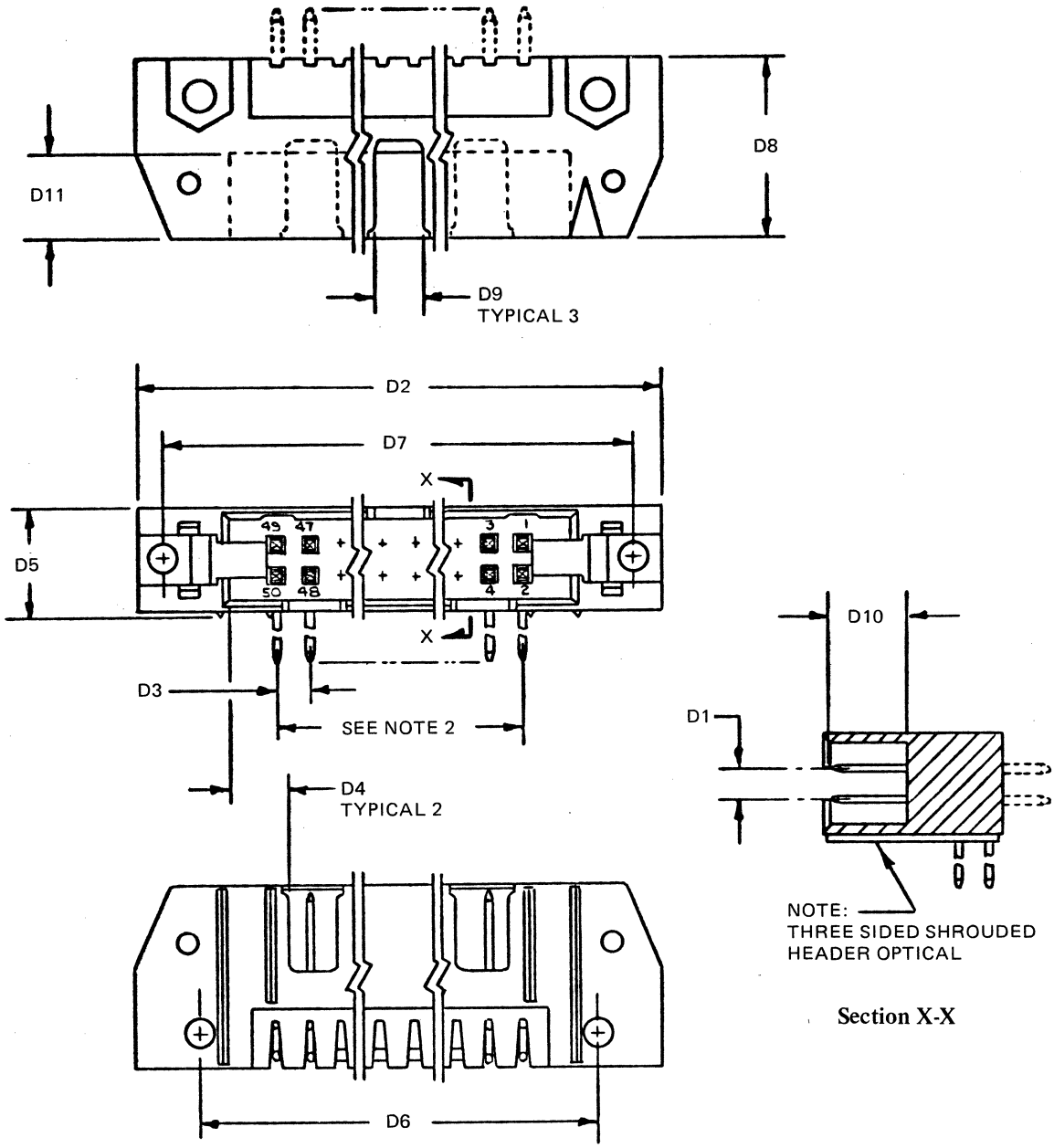
3.4.1 Bidirectional CONTROL BUS Lines. The bidirectional CONTROL BUS is used in the daisy-chain mode and the radial mode.



Dimensions	Millimeters	Inches
C1	2.54	0.100
C2	60.96	2.4
C3	2.54	0.100
C4	8.357	0.329
C5	3.3025	0.130
C6	68.072	2.680
C7	6.096	0.240
C8	8.153	0.321
C9	13.487	0.531
C10	3.81	0.150
C11	1.27	0.050
C12	6.096	0.240
C13	32.385	1.275
C14	3.302	0.130
C15	7.493	0.295
C16	2.667	0.105
C17	1.625	0.064

NOTES:
(1) Fifty contacts on 1.27 mm (0.050 inch) staggered spacing = 63.23 mm (3.450 inch).
(2) Tolerances ± 0.127 mm (± 0.005 inch) noncumulative.

Figure 2
Interface Cable Plug



Dimensions	Millimeters	Inches
D1	2.54	0.100
D2	83.80	3.260
D3	2.54	0.100
D4	4.83	0.190
D5	8.51	0.335
D6	72.64	2.860
D7	78.74	3.100
D8	13.94	0.549
D9	4.19	0.165
D10	6.09	0.240
D11	6.60	0.260

NOTES:
(1) Fifty contacts on 2.54 mm (0.100 inch) spacing = 60.96 mm (2.40 inch).
(2) Tolerances ± 0.127 mm (± 0.005 inch) noncumulative.

Figure 3
Interface Cable Receptacle

In the daisy-chain mode, eight bits of information and an optional parity bit shall be transferred between the host and the selected device.

In the radial mode, each of the eight CONTROL BUS lines shall be used separately for communication with one specific device. In this way, one bit of information is transferred to or from all devices simultaneously. Each device shall have provisions (jumper, switches, etc) to connect the radial line to any one of the eight CONTROL BUS lines. The optional control bus parity bit shall not be used in the radial mode. The configuration of the bidirectional CONTROL BUS lines is shown in Figure 4.

3.4.1.1 CONTROL BUS Drivers. The bus drivers for the parallel information shall be either three-state or open collector. The driver for the radial signal in the device shall be open collector.

All bus driver outputs for LOW level shall sink 24 milliamps minimum. The LOW level output voltage shall be 0.5 volt maximum. Driver outputs for HIGH level shall have a HIGH level output voltage of 2.4 volts minimum, 5.25 volts maximum. A 10-milliamps source current is provided by the 470-ohm terminator discussed in 3.4.1.3.

The leakage current in the high impedance state (OFF state for open collector drivers) shall not exceed 0.25 milliamp for either HIGH or LOW level on the CONTROL BUS.

The total number of drivers connected to any CONTROL BUS line shall not exceed ten (one in the host, one in each of the eight devices for the parallel lines, and one in a single device for the radial line).

3.4.1.2 CONTROL BUS Receivers. The maximum LOW level input current shall be -400 microamps. The maximum HIGH level input current shall be 80 microamps. The maximum LOW level input voltage shall be 0.9 volt. The minimum HIGH level input voltage shall be 2.0 volts.

The total number of receivers connected to any CONTROL BUS line shall not exceed ten (one in the host, one in each of the eight devices for the parallel lines, and one in a single device for the radial line).

3.4.1.3 CONTROL BUS Termination. A 470-ohm resistor, +/- 10 percent shall be installed at the host end of all CONTROL BUS lines (control bus bits 0 to 7 and control bus parity) connected to +5 volts, +/- 5 percent. See Figure 4.

3.4.2 Single-Ended Lines. The cable configuration of the single-ended lines shall be as shown in Figures 5 through 7.

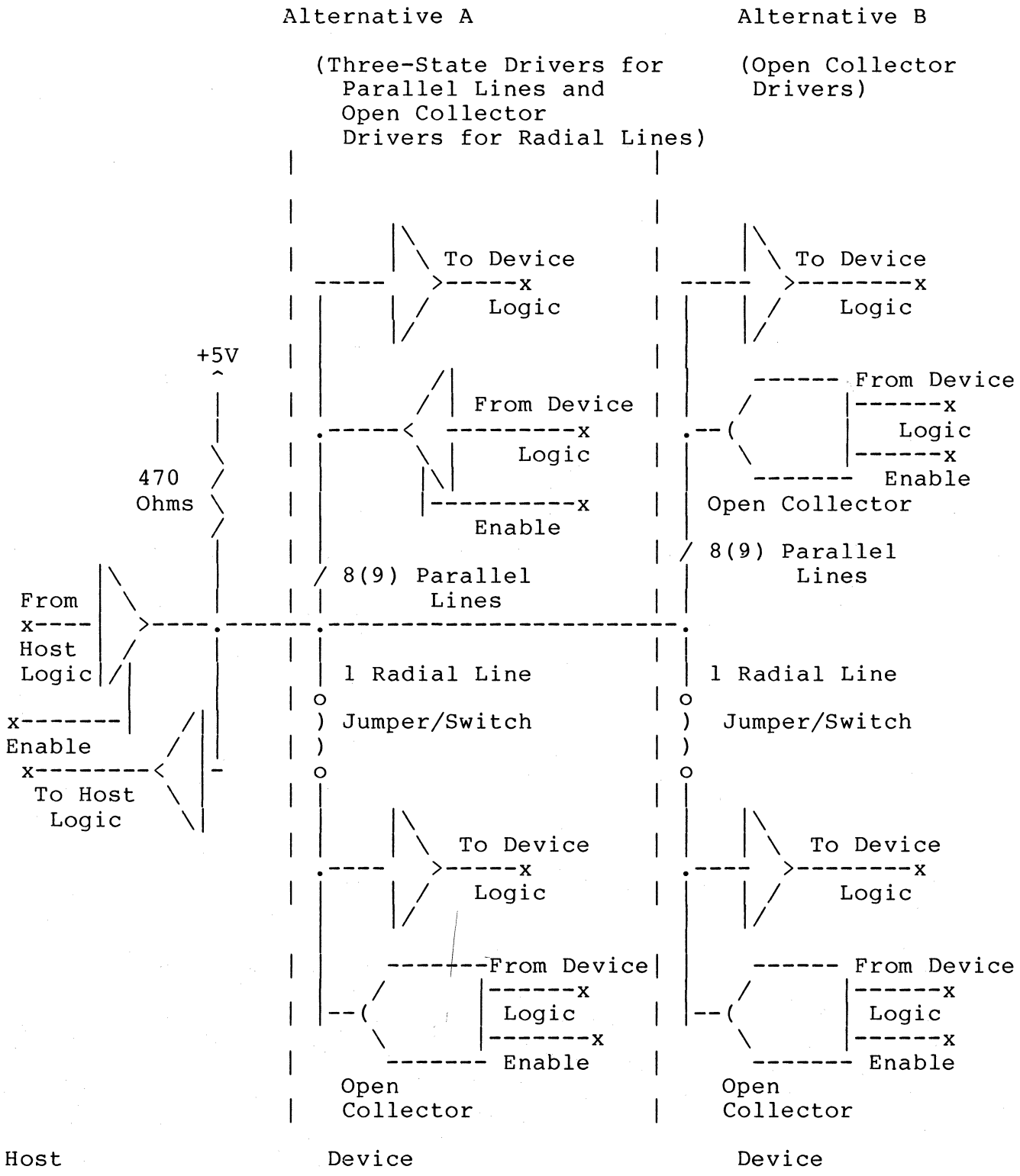


Figure 4

Class A Cable Configurations for Bidirectional CONTROL BUS Signals

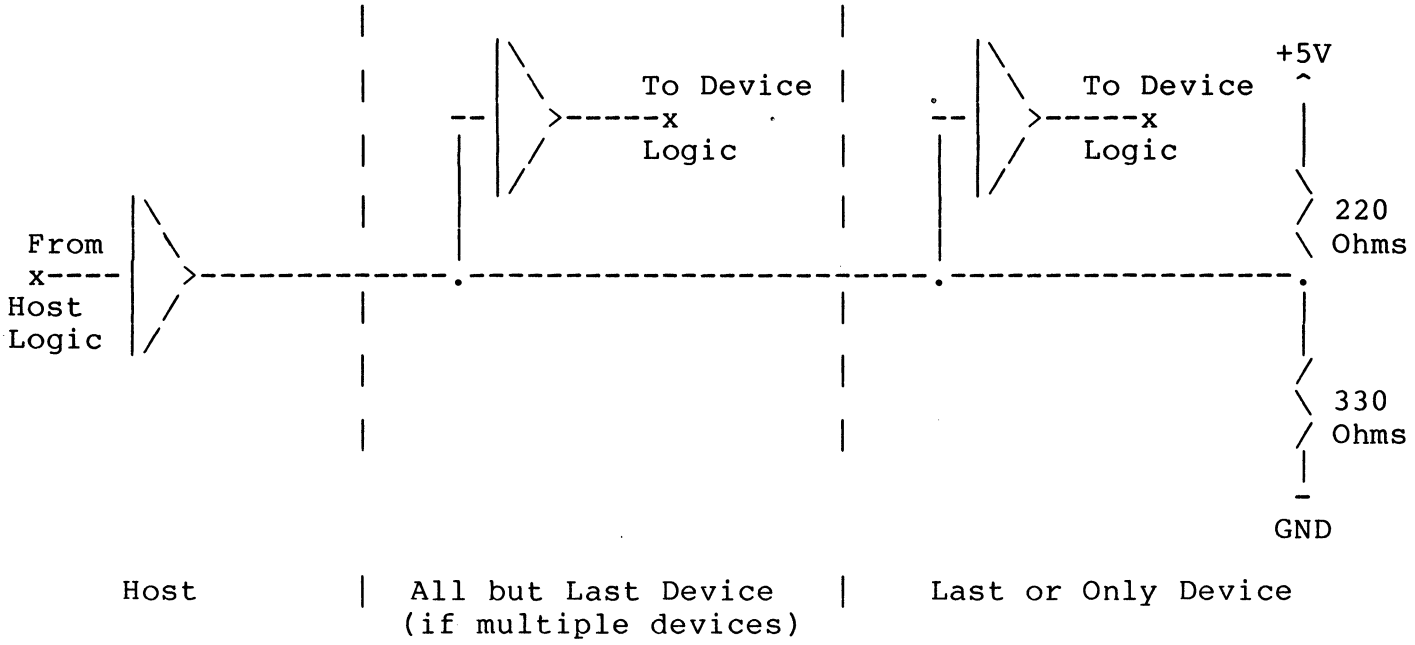


Figure 5

Class A Cable Configuration for Unidirectional Single-Ended Lines from Host (Except PORT ENABLE)

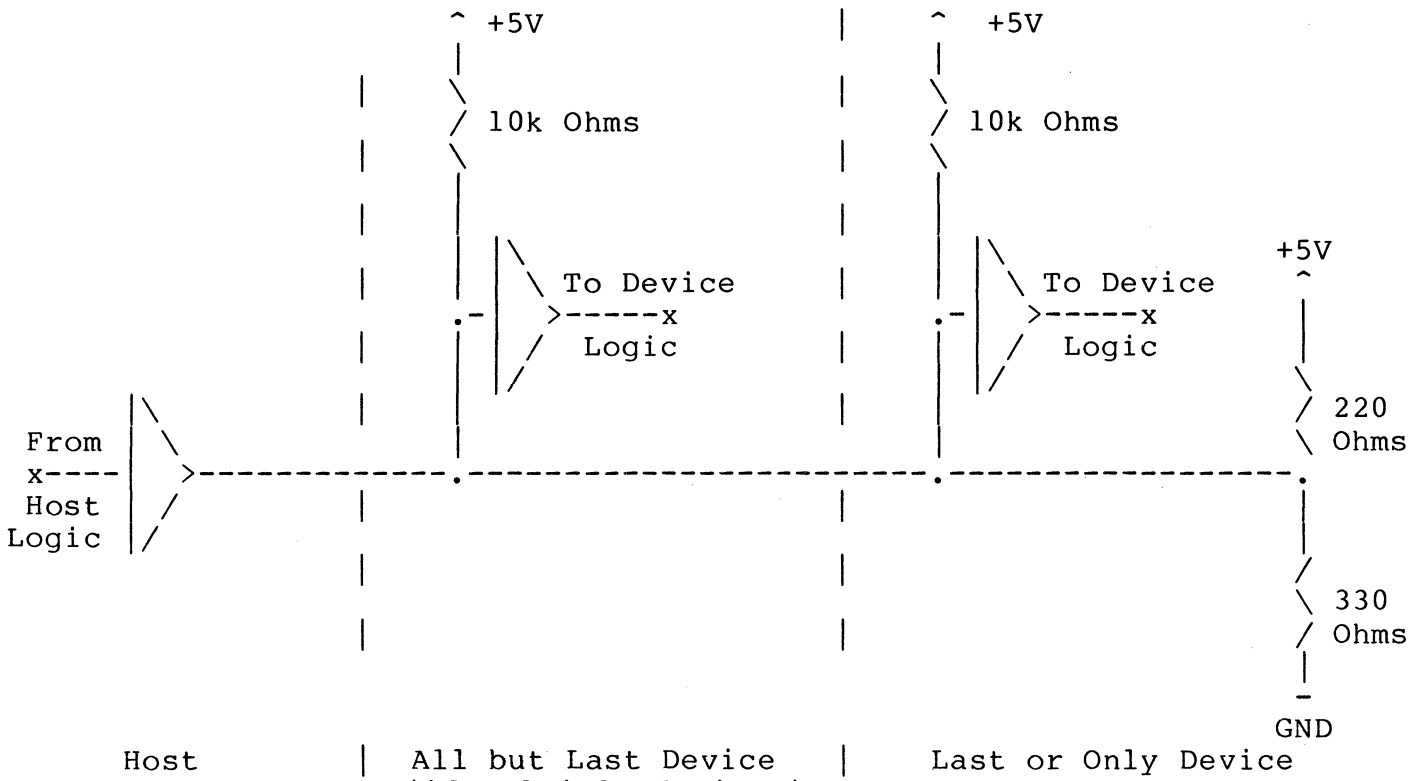


Figure 6

Class A Cable Configuration for PORT ENABLE

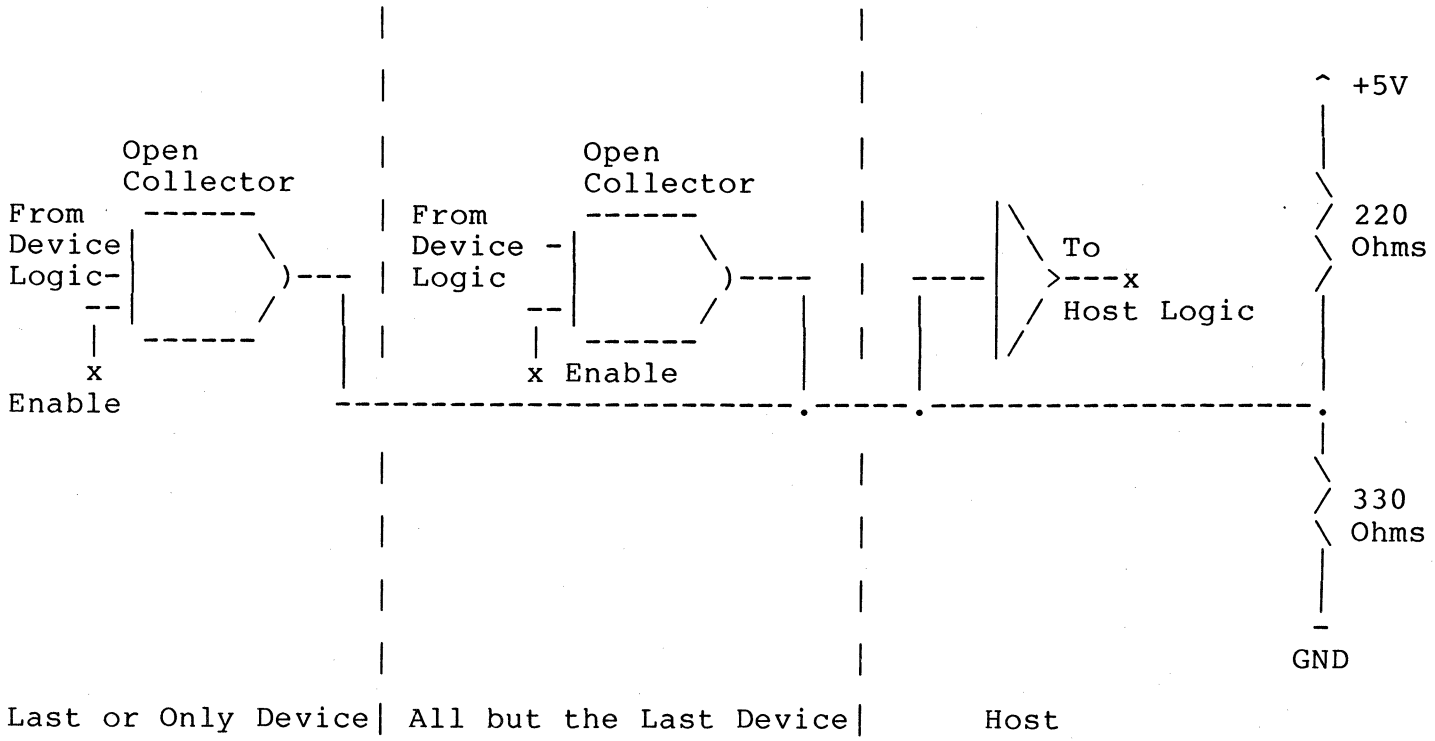


Figure 7

Class A Cable Configuration
for Unidirectional Single-Ended Lines from Device

3.4.2.1 Single-Ended Line Drivers. The drivers shall have open collector outputs capable of sinking 40 milliamps at LOW levels. LOW level output voltage shall not exceed 0.4 volt. The high level leakage current shall not exceed 250 microamps.

3.4.2.2 Single-Ended Line Receivers. The receivers shall accept TTL logic levels. For noise immunity, the receivers shall have an input hysteresis of 0.4 volt minimum, with a positive-going threshold voltage between 1.4 and 2.0 volts and a negative-going threshold voltage between 0.5 and 1.1 volts. LOW level input current shall be -1.2 milliamps or less. The HIGH level input current shall be 40 microamps maximum.

3.4.2.3 Single-Ended Line Termination. All single-ended lines originating at the host shall be terminated at the last device with 330 ohms, +/- 5 percent, to ground and 220 ohms, +/- 5 percent, to +5 volts. All single-ended lines originating at the devices shall be terminated in the same way at the host.

3.4.2.4 PORT ENABLE Termination. A pullup resistor of 10 kilohms +/- 10 percent to +5 volts shall be added to the PORT ENABLE line in each device to generate an inactive signal state whenever the device is not connected (see Figure 6).

3.4.3 Differential Lines. The differential line drivers and receivers shall operate from a single + 5-volt supply. They shall operate to 10 MHz and shall be capable of meeting the timing requirements of 6.3 and 6.4 while operating the recommended terminated cable configuration.

The cable configuration of the differential lines shall be as shown in Figures 8 and 9.

An active signal state is defined as the plus (+) line being equal or more positive than the minus (-) line. An inactive signal state is defined as the minus line being more positive than the plus line.

3.4.3.1 Differential Line Drivers. The differential line drivers shall have a three-state output and be capable of sinking or sourcing a minimum of 20 milliamps in the active state. In the inactive or high-impedance state, leakage current shall not exceed +/- 20 microamps.

3.4.3.2 Differential Line Receivers. The common mode input range capability of the receivers shall be at least +7 to -7 volts. The differential input voltage shall be -0.2 volt minimum and +0.2 volt maximum. The input hysteresis should be 140 millivolts +/- 70 millivolts minimum.

3.4.3.3 Differential Line Termination. Each line of all pairs of differential lines shall be terminated with 100 ohms, +/- 10 percent, to ground both at the host and the last device.

3.5 Electrical Characteristics, Class B Configuration. This class uses open collector drives and high-threshold receivers for the bidirectional CONTROL BUS and the single-ended lines. Refer to Figures 10 through 13.

3.5.1 Line Drivers. The maximum LOW level output voltage shall be 0.45 volts. At LOW level, the driver output shall sink 100 milliamperes minimum. At HIGH level, the driver output shall source 300 milliamperes maximum.

3.5.2 Line Receivers. The maximum LOW level input voltage shall be 1.8 volts. The minimum HIGH level input voltage shall be 2.3 volts. At LOW level, the input current shall be -100 microamperes maximum. At HIGH level, the input current shall be 300 microamperes maximum.

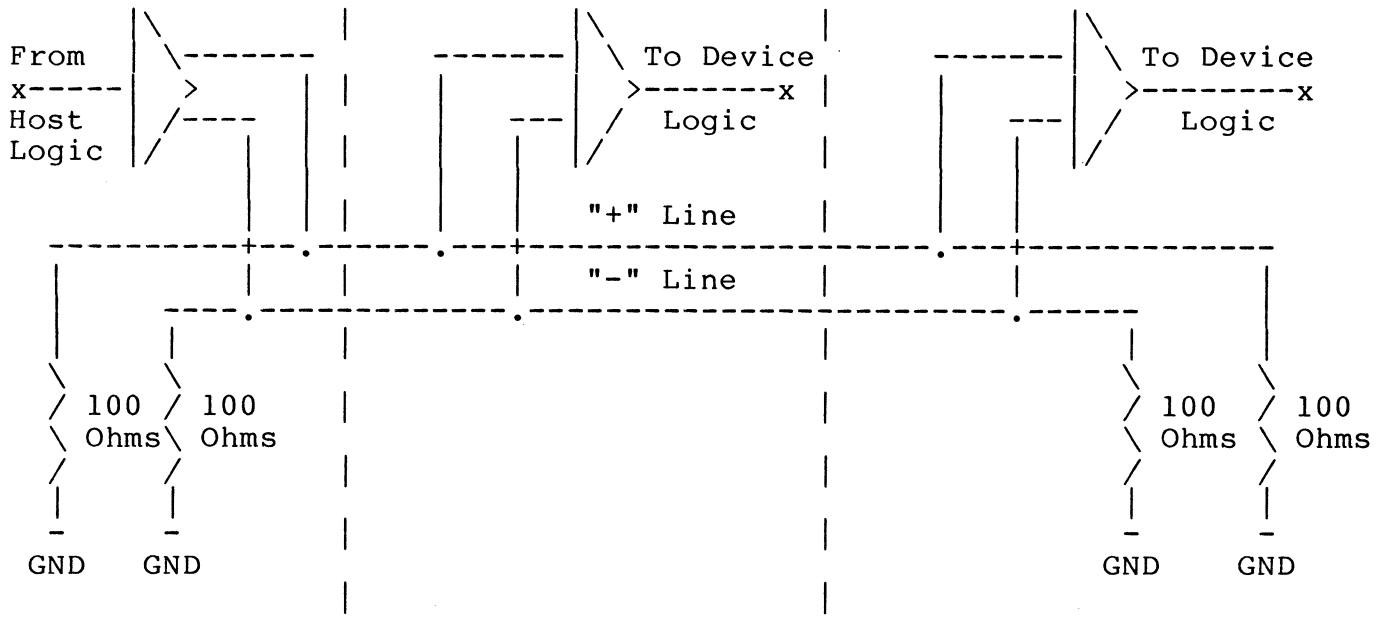


Figure 8

Class A or B Cable Configuration for Differential Lines from Host

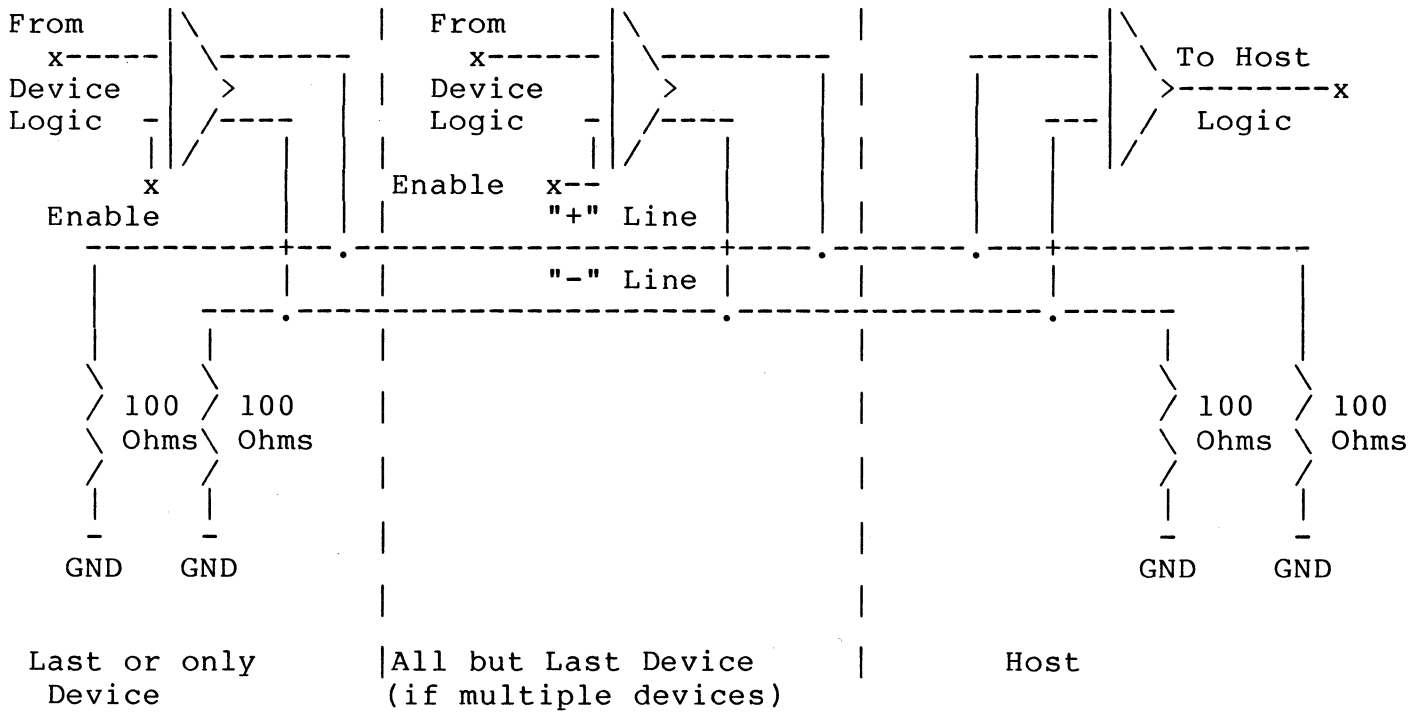


Figure 9

Class A or B Cable Configuration for Differential Lines from Device

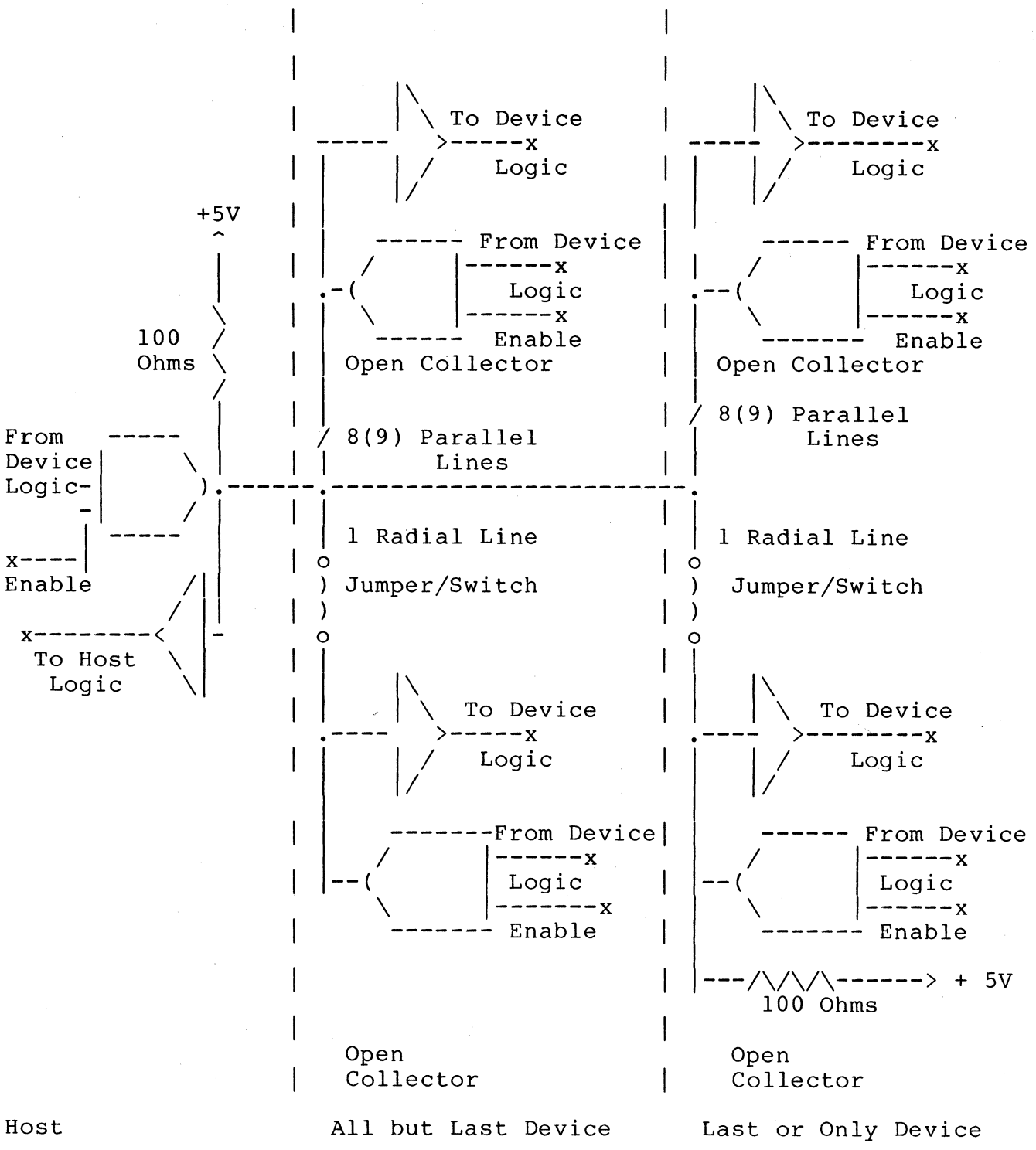


Figure 10

Class B Cable Configuration for Bidirectional CONTROL BUS Signals

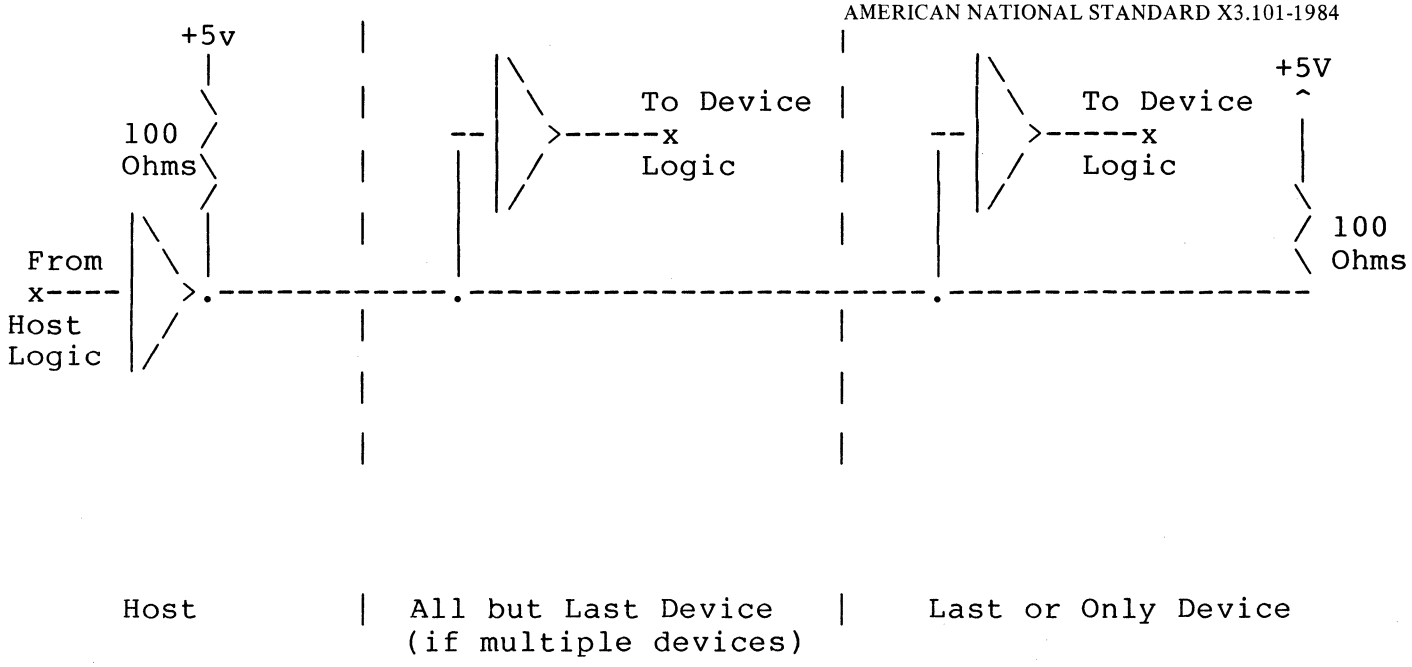


Figure 11

Class B Cable Configuration for Unidirectional Single-Ended Lines from Host (except PORT ENABLE)

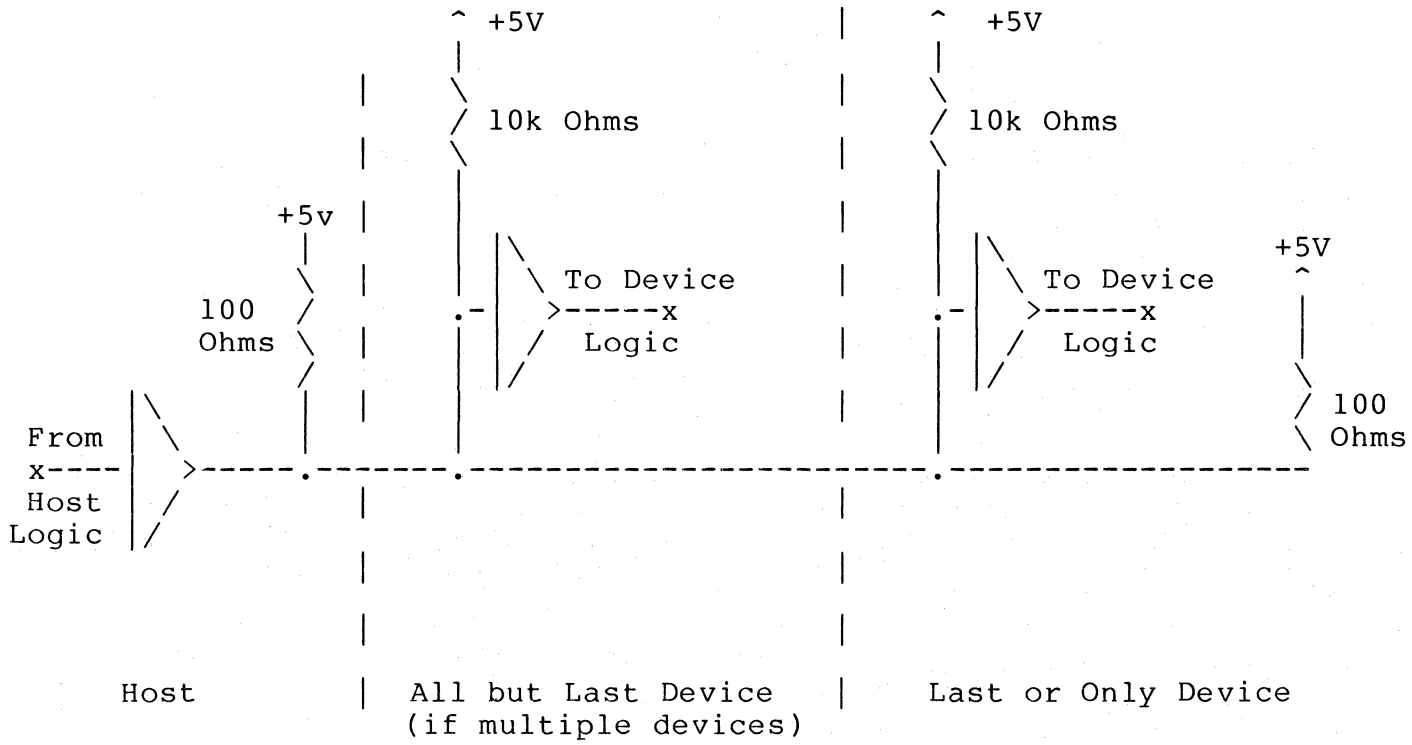


Figure 12

Class B Cable Configuration for PORT ENABLE

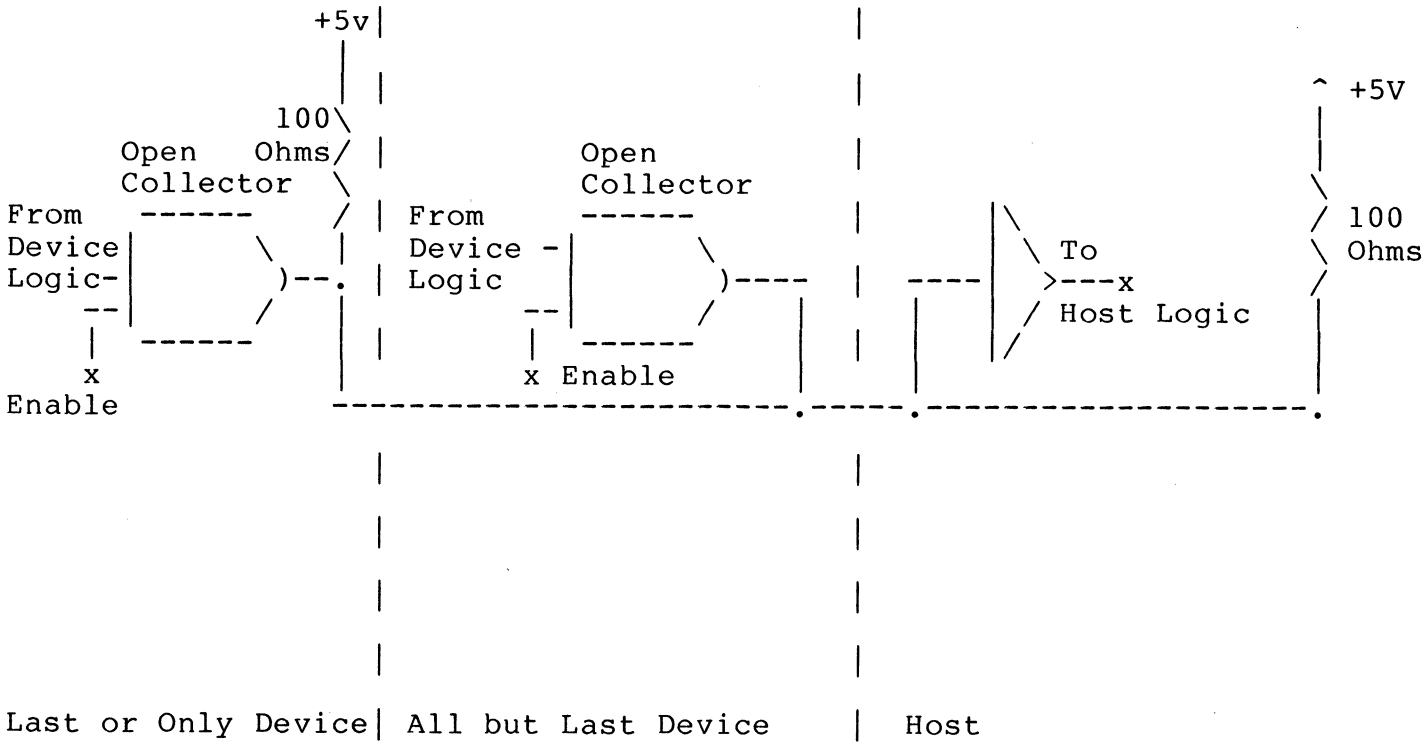


Figure 13

Class B Cable Configuration

for Unidirectional Single-Ended Lines from Device

3.5.3 Line Termination. Each signal shall be terminated by installing a 100-ohm resistor from signal to + 5 volts at both the host and the last unit on the cable.

3.5.4 PORT ENABLE. A pullup resistor of 10 kilohms +/- 10 percent to +5 volts shall be added to the PORT ENABLE line in each device to generate an inactive signal state whenever the device is not connected (see Figure 12).

3.5.5 Differential Lines. The differential line drivers and receivers shall operate from a single +5-volt supply. They shall operate to 16 MHz and shall be capable of meeting the timing requirements of 6.3 and 6.4 while operating the recommended terminated cable configurations.

The cable configurations of the differential lines shall be as shown in Figures 8 and 9.

An active signal state is defined as the plus line being equal or more positive than the minus line. An inactive signal state is defined as the minus line being more positive than the plus line.

3.5.5.1 Differential Line Drivers. The differential line drivers shall have a three-state output and be capable of sinking or sourcing 40 milliamps in the active state. In the inactive or high impedance state, leakage current shall not exceed +/- 20 microamps.

3.5.5.2 Differential Line Receivers. The common mode of input range capability of the receivers shall be at least +7 to -7 volts. The differential input voltage shall be -0.2 volt minimum and +0.2 volt maximum. The input hysteresis should be 140 millivolts +/-70 millivolts minimum.

3.5.5.3 Differential Line Termination. Each line of all parts of differential lines shall be terminated with 100 ohms, +/- 10 percent to ground both at the host and the last device.

4. Signal Definitions

This section provides signal definitions and their intended operation, status, or both. Relative signal timing and tolerance is defined in Section 6.

NOTE: The timing diagrams of Section 6 shall take precedence over all other timing definitions.

4.1 CONTROL BUS. The CONTROL BUS shall be used for bidirectional transfer of information. The direction of transfer shall be determined by the BUS DIRECTION OUT signal.

The electrical characteristics of the CONTROL BUS signals are defined in 3.4.1. The CONTROL BUS lines shall be LOW for an active signal state and shall be HIGH for an inactive signal state.

Throughout the specification of this interface, the host shall be in control of the CONTROL BUS. All communications between the host and the selected device shall be determined by the host.

The CONTROL BUS is used in two modes. When SELECT OUT/ATTENTION IN STROBE is active, the CONTROL BUS shall be in the radial mode. When the COMMAND REQUEST, PARAMETER REQUEST, or BUS ACKNOWLEDGE is active, the CONTROL BUS shall be in the daisy-chain mode.

4.1.1 Radial Mode. Each device shall be assigned a unit number 0 to 7 by radially attaching to one SELECT/ATTENTION DEVICE (0-7) line in accordance with Table 3.

Table 3

Pin Assignment

Signal Pin	Ground Pin	Signal Name	Signal Source
1		Ground	---
		CONTROL BUS	
2	10	Bit 0, Select/Attn Device 0	Host/Device
3	10	Bit 1, Select/Attn Device 1	Host/Device
4	10	Bit 2, Select/Attn Device 2	Host/Device
5	10	Bit 3, Select/Attn Device 3	Host/Device
6	10	Bit 4, Select/Attn Device 4	Host/Device
7	10	Bit 5, Select/Attn Device 5	Host/Device
8	10	Bit 6, Select/Attn Device 6	Host/Device
9	10	Bit 7, Select/Attn Device 7	Host/Device
11	12	Parity (optional)	Host/Device
13	14	SELECT OUT/ATTN IN STROBE	Host
15	16	COMMAND REQUEST	Host
17	18	PARAMETER REQUEST	Host
19	20	BUS DIRECTION OUT	Host
21	22	PORT ENABLE	Host
23	24	ADDRESS MARK CONTROL (optional)	Host
25	26	READ GATE	Host
27	28	WRITE GATE	Host
29	30	BUS ACKNOWLEDGE	Device
31	32	INDEX	Device
33	34	SECTOR/ADDRESS MARK DETECTED	Device
35	36	ATTENTION	Device
37	36	BUSY	Device
39	38	READ DATA +	Device
40	38	READ DATA -	Device
42	41	READ/REFERENCE CLOCK +	Device
43	41	READ/REFERENCE CLOCK -	Device
45	44	WRITE CLOCK +	Host
46	44	WRITE CLOCK -	Host
48	47	WRITE DATA +	Host
49	47	WRITE DATA -	Host
	50	Ground	---

4.1.1.1 Select Out Mode. When both BUS DIRECTION OUT and SELECT OUT/ATTENTION IN STROBE are active, each radial line shall transfer the selection information to the corresponding device.

4.1.1.2 Attention In Mode. When BUS DIRECTION OUT is inactive and SELECT OUT/ATTENTION IN STROBE is active, each device shall gate its internal ATTENTION condition onto its corresponding CONTROL BUS line.

4.1.2 Daisy-Chain Mode. When in the daisy-chain mode, all CONTROL BUS transfers shall consist of a two-byte sequence. The transfer is asynchronous and controlled with a handshake protocol. The first byte is transferred using a handshake between the COMMAND REQUEST signal and the BUS ACKNOWLEDGE signal. The second byte is transferred using a handshake between the PARAMETER REQUEST signal and the BUS ACKNOWLEDGE signal. Refer to Section 5 for the command definitions.

4.1.2.1 Command Out. When both the BUS DIRECTION OUT and COMMAND REQUEST are active, the host shall transfer a command byte to the selected device.

When bit 6 in the command code (first byte) is ONE, the second byte shall be parameter out (see 4.1.2.2 and Table 4).

When bit 6 in the command code (first byte) is ZERO, the second byte shall be parameter in (See 4.1.2.3 and Table 5).

When the state of the BUS DIRECTION OUT signal for the transfer of the parameter (second byte) does not comply with the definition of bit 6 of the command code, this condition shall set the ATTENTION condition and the control bus error bit in the general status byte (see 5.4.1.2).

The condition of the BUS DIRECTION OUT signal being inactive and the COMMAND REQUEST signal being active is a violation of protocol and may optionally set the ATTENTION condition and the control bus error bit in the general status byte (see 5.4.1.2).

4.1.2.2 Parameter Out. When both BUS DIRECTION OUT and PARAMETER REQUEST are active, the host shall transfer a parameter byte to the selected device (see Table 4).

4.1.2.3 Parameter In. When the BUS DIRECTION OUT signal is inactive and the PARAMETER REQUEST signal is active, the host is requesting a parameter byte (status) to be transferred from the selected device (see Table 5).

Table 4
Commands with Parameters Out

Function	Command Code	Parameter Out
ATTENTION CONTROL	40 Hex	Bit 7 0 = ENABLE ATTENTION 1 = DISABLE ATTENTION
WRITE CONTROL	41 Hex	Bit 7 1 = WRITE ENABLE 0 = WRITE DISABLE
SET UPPER CYLINDER ADDRESS	42 Hex	MSB of cylinder address
SET LOWER CYLINDER ADDRESS	43 Hex	LSB of cylinder address
SELECT MOVING HEAD	44 Hex	Head number
SELECT MOVING HEAD *	45 Hex	Head number
LOAD ATTRIBUTE NUMBER	50 Hex	Address byte
LOAD DEVICE ATTRIBUTE	51 Hex	Information byte
SELECT FIXED HEAD	52 Hex	Head address
READ CONTROL	53 Hex	Bits 7,6 0X = Nominal strobe 10 = STROBE EARLY 11 = STROBE LATE
OFFSET CONTROL *	54 Hex	Bits 7,6 0X = No offset 10 = OFFSET FORWARD 11 = OFFSET REVERSE
SPIN CONTROL *	55 Hex	Bit 7 1 = SPIN-UP 0 = SPIN-DOWN
LOAD BYTES PER SECTOR HIGH	56 Hex	MSB of bytes per sector
LOAD BYTES PER SECTOR MEDIUM	57 Hex	MedSB of bytes per sector
LOAD BYTES PER SECTOR LOW	58 Hex	LSB of bytes per sector
LOAD SECTOR PULSES PER TRACK HIGH	59 Hex	MSB of SECTOR pulses per track
LOAD SECTOR PULSES PER TRACK MEDIUM	5A Hex	MedSB of SECTOR pulses per track
LOAD SECTOR PULSES PER TRACK LOW	5B Hex	LSB of SECTOR pulses per track
LOAD READ PERMIT HIGH	6B Hex	MSB of cylinder address
LOAD READ PERMIT LOW	6C Hex	LSB of cylinder address Read enabled only on cylinder equal to or greater than the above
LOAD WRITE PERMIT HIGH	6D Hex	MSB of cylinder address
LOAD WRITE PERMIT LOW	6E Hex	LSB of cylinder address Write enabled only on cylinder equal to or greater than the above
LOAD TEST BYTE	6F Hex	Test byte

NOTES:

(1) Commands with codes 40 Hex through 4F Hex are mandatory commands, whereas, commands with codes 50 Hex to 6F Hex are optional.

(2) The code range of 70 Hex through 7F Hex is reserved for unique vendor applications. All unused bits in parameters shall be zero.

* These commands are time-dependent commands that generate an ATTENTION condition upon completion.

Table 5

Commands with Parameters In

Function	Command Code	Parameter In
REPORT ILLEGAL COMMAND	00 Hex	General status
CLEAR FAULT	01 Hex	General status
CLEAR ATTENTION	02 Hex	General status
SEEK *	03 Hex	General status
REZERO *	04 Hex	General status
REPORT SENSE BYTE 2**	0D Hex	Sense byte 2
REPORT SENSE BYTE 1**	0E Hex	Sense byte 1
REPORT GENERAL STATUS**	0F Hex	General status
REPORT DEVICE ATTRIBUTE	10 Hex	Device attribute byte
SET ATTENTION *	11 Hex	General status
RESERVE DEVICE	12 Hex	General status
RELEASE DEVICE	13 Hex	General status
SELECTIVE RESET *	14 Hex	General status
SEEK TO LANDING ZONE *	15 Hex	General status
PARTITION TRACK *	16 Hex	General status
REPORT CYLINDER HIGH	29 Hex	MSB of cylinder address
REPORT CYLINDER LOW	2A Hex	LSB of cylinder address
REPORT READ PERMIT HIGH	2B Hex	MSB of cylinder address
REPORT READ PERMIT LOW	2C Hex	LSB of cylinder address
REPORT WRITE PERMIT HIGH	2D Hex	MSB of cylinder address
REPORT WRITE PERMIT LOW	2E Hex	LSB of cylinder address
REPORT TEST BYTE	2F Hex	Echo byte

NOTES:

(1) Commands with codes 00 Hex through 0F Hex are mandatory commands, whereas, commands with codes 10 Hex to 2F Hex are optional.

(2) The code range of 30 Hex through 3F Hex is reserved for unique vendor applications. All unused bits in parameters shall be ZERO.

* These commands are time-dependent commands that set an ATTENTION condition upon completion.

** Events reported in these status and sense bytes can set an ATTENTION condition even without a preceding command.

4.1.3 CONTROL BUS Bits 0-7, SELECT/ATTENTION Device 0-7. The eight CONTROL BUS signals, 0 to 7, shall be used for communication between the host and the device as defined in 5.1.1 and 5.1.2. Control bus bit 0 shall be the least significant bit.

4.1.4 CONTROL BUS PARITY (optional). When the CONTROL BUS is used in daisy-chain mode, the bidirectional control bus parity bit shall be odd parity (odd number of ONEs) of the eight control bus bits and the control bus parity bit.

When the CONTROL BUS is used in the radial mode, the CONTROL BUS PARITY signal is not used and shall be inactive.

If CONTROL BUS PARITY is implemented in either the host or the device but not in both, the CONTROL BUS shall function without an error condition.

4.2 Control Interface. This group of signals is unidirectional in nature. The electrical characteristic of the CONTROL INTERFACE lines is defined in 3.4.2. All CONTROL INTERFACE lines shall be LOW for an active signal state and HIGH for an inactive signal state.

4.2.1 PORT ENABLE. This signal is normally held active by the host. When this signal is active all devices attached to the interface shall respond to the interface protocol as described by this standard.

This signal may be used to disable all devices when host power is lost, or as a programmed reset, or both. If the interface cable is being disconnected from a device, the device shall be reset by the active-to-inactive transition on this line. (See 4.2.2.3 for multiported drives.)

When this signal changes from active to inactive, all devices shall be deselected within 20 milliseconds maximum except for the write circuitry in each device, which shall be disabled within 1 microsecond maximum. The device shall remain deselected while PORT ENABLE is inactive.

Upon detecting PORT ENABLE going inactive, each device shall go to its initial state as defined below (also see the vendor specification). After PORT ENABLE changes from inactive to active and after the initial state is reached the device shall set the ATTENTION condition.

The initial state is the state a device shall reach after being powered up, PORT ENABLE has become active, or a SELECTIVE RESET command has been received.

The conditions are:

(1) The device shall be deselected.

(2) The device shall respond to the SELECT OUT/ATTENTION IN STROBE signal.

(3) All parameters of commands with parameters out in Table 4 shall be reset to ZERO (except SPIN CONTROL - see 5.1.2.6).

(4) The device attribute table, if implemented, shall be set to its initial value (see 5.3).

(5) All resettable error conditions shall be reset. If the cause of the error still exists, it shall set the error conditions again.

(6) The initial state bit in sense byte 2 shall be set.

4.2.2 BUS DIRECTION OUT. The BUS DIRECTION OUT signal is transferred from the host to all attached devices. BUS DIRECTION OUT controls the direction of transfer on the CONTROL BUS. When the BUS DIRECTION OUT signal is active, this defines a transfer from the host to the device.

4.2.3 SELECT OUT/ATTENTION IN STROBE. This signal is transferred from the host to all attached devices. It has two different functions depending on the state of the BUS DIRECTION OUT signal.

When the BUS DIRECTION OUT signal is active, the signal is SELECT OUT STROBE.

When the BUS DIRECTION OUT signal is inactive, the signal is ATTENTION IN STROBE.

4.2.3.1 SELECT OUT STROBE. Only one device shall be selected at any one time. When the BUS DIRECTION OUT signal is active, the active-going edge of the SELECT OUT STROBE signal is used for selecting or deselecting the device.

When any CONTROL BUS signal is active and SELECT OUT STROBE transitions to active, the device connected to that specific CONTROL BUS line shall become selected.

When any CONTROL BUS signal is inactive and SELECT OUT STROBE transitions to active, the device connected to that specific CONTROL BUS line shall become deselected.

When all CONTROL BUS signals are inactive and the SELECT OUT STROBE transitions to active, all attached devices shall become deselected.

4.2.3.2 ATTENTION IN STROBE. When the BUS DIRECTION OUT signal is inactive, the ATTENTION IN STROBE shall be used to gate the device's internal ATTENTION condition (see 4.2.8) onto the corresponding CONTROL BUS line connected to that device (see Appendix A).

4.2.4 COMMAND REQUEST. This signal initiates the handshake control from the host to the selected device. The active state of this signal signifies the transfer of the first byte of each two-byte transfer. Until the receipt of BUS ACKNOWLEDGE, the COMMAND REQUEST signal shall remain active.

4.2.5 PARAMETER REQUEST. This signal is also a handshake control line from the host to the selected device. The active state of this signal for a PARAMETER OUT command indicates that the output parameter byte is valid on the CONTROL BUS. The active state of this signal for a PARAMETER IN command requests the selected device to place the parameter byte on the CONTROL BUS. Until the receipt of BUS ACKNOWLEDGE, the PARAMETER REQUEST signal shall remain active.

4.2.6 BUS ACKNOWLEDGE. This signal is returned from the selected device to the host. The BUS ACKNOWLEDGE signal has two functions.

When the CONTROL BUS is used in the radial mode (SELECT OUT/ATTENTION IN STROBE active), the selected device shall make the BUS ACKNOWLEDGE signal active to acknowledge its selection.

When the CONTROL BUS is used in daisy-chain mode, the BUS ACKNOWLEDGE signal performs the asynchronous handshake with the COMMAND REQUEST signal or the PARAMETER REQUEST signal.

4.2.7 BUSY. This signal shall be held active by the selected device if the selected device is unable to accept additional commands. The BUSY signal shall change to the active state before the active-going edge of the BUS ACKNOWLEDGE of a time-dependent command (see Section 5) that causes the device to become busy. The BUSY condition could occur during power-up sequencing, seeking, or execution of diagnostics. The BUSY signal shall not be made active if the device can accept commands.

The busy-to-not-busy transition within the device shall set the ATTENTION condition within the device (see 4.2.8).

If COMMAND REQUEST becomes active when the BUSY signal is already active, the device will not respond with BUS ACKNOWLEDGE before the function is completed and BUSY is made inactive.

NOTE: The BUSY interface signal is different from the busy executing status bit (see 5.4.1.7).

4.2.8 ATTENTION. This signal is a party line signal ("wired OR") from all devices to the host, independent of the selection of a device.

The ATTENTION signal shall be made active by a device, if the device's internal ATTENTION condition is set to ONE, and if ATTENTION is enabled (see ATTENTION CONTROL command, 5.1.1.1). The ATTENTION condition shall be set if the device requires service from the host. The detailed conditions to set the ATTENTION condition are defined in Section 5.

The ATTENTION condition of the selected device shall only be reset by the CLEAR ATTENTION command or the CLEAR FAULT command. Issuing the CLEAR FAULT command shall reset only those error status bits and the resulting ATTENTION condition if the error condition can be reset. A CLEAR ATTENTION command shall reset the ATTENTION condition independent of error conditions.

4.2.9 INDEX. INDEX is a signal that indicates to the host that a reference point or index area is passing under the heads of the selected device. One INDEX pulse shall be generated by the selected device per revolution of the recording media.

Whenever the device is ready and the head carriage is not in motion, a valid INDEX signal shall be transferred from the selected device to the host. When the head carriage is in motion or the device is not ready, the INDEX signal may or may not be valid (see vendor specification).

4.2.10 SECTOR/ADDRESS MARK. The SECTOR signal establishes rotational reference points on the recording surface. Each track may be divided into sectors with the initial sector (Zero) starting coincident with the INDEX pulse. All subsequent sectors start coincident with the active-going edge of a Sector pulse. When the INDEX pulse is activated, the SECTOR pulse is omitted.

ADDRESS MARK, which is an optional signal, indicates device detection of a previously recorded ADDRESS MARK when READ GATE and ADDRESS MARK CONTROL are both active. Only one inactive-to-active transition of ADDRESS MARK is made for each assertion of an ADDRESS MARK CONTROL signal that is active when the READ GATE signal is active.

Whenever the device is ready and the head carriage is not in motion, a valid SECTOR/ADDRESS MARK signal shall be transferred from the selected device to the host. When the head carriage is in motion or the device is not ready the SECTOR/ADDRESS signal may or may not be valid (see vendor specification).

4.2.11 READ GATE. The READ GATE signal is transferred from the host to the selected device.

The READ GATE signal enables and synchronizes the read circuitry to transfer the serialized data information on the READ DATA lines from the recording medium. If the address mark option is utilized, READ GATE and ADDRESS MARK CONTROL shall enable the device to search for a previously recorded ADDRESS MARK.

4.2.12 WRITE GATE. The WRITE GATE signal is transferred from the host to the selected device.

The WRITE GATE signal enables the write circuitry in the device to transfer the serialized information on the WRITE DATA lines to the recording medium. If the address mark option is implemented, the device shall record an ADDRESS MARK on the medium when WRITE GATE and ADDRESS MARK CONTROL are active.

NOTE: A write operation shall not take place unless a WRITE ENABLE condition has been established by a previous WRITE CONTROL command.

4.2.13 ADDRESS MARK CONTROL (optional). The ADDRESS MARK CONTROL signal is transferred from the host to the selected device.

ADDRESS MARK CONTROL is used in conjunction with READ GATE or WRITE GATE, for the detection of or writing of an ADDRESS MARK on the data surface.

The ADDRESS MARK CONTROL signal shall be inactive if the address mark option is not used or not implemented. Devices that do not use the address mark option shall still provide the specified terminating resistors.

4.3 READ/WRITE Signals. This section describes the signals used when transferring data to and from the host. These signals are only valid if a device is selected. All of these signals are driven differentially (see 3.4.3). All data sent to the device or host shall be Non-Return-to-Zero (NRZ).

4.3.1 READ DATA. When READ GATE is active, the READ DATA lines transfer the serial NRZ read data from the selected device to the host. This data is synchronized with READ CLOCK. The READ DATA signal shall be static when READ GATE is not active.

4.3.2 READ/REFERENCE CLOCK. The READ/REFERENCE CLOCK is transferred from the selected device to the host. This signal shall transfer READ CLOCK when READ GATE is active. READ CLOCK shall be synchronous with the serial NRZ read data. This signal shall transfer the REFERENCE CLOCK at all other times.

4.3.3 WRITE DATA. When WRITE GATE is active, the WRITE DATA lines shall transfer the serial NRZ write data from the host to the selected device for recording. The serial write data shall be synchronized to the WRITE CLOCK. This signal shall be held static at all times except when WRITE GATE is active.

4.3.4 WRITE CLOCK. WRITE CLOCK shall be used by the selected device to properly phase the WRITE DATA lines while recording. WRITE CLOCK shall be generated in the host by returning the REFERENCE CLOCK signal back to the selected device at the same frequency with an unspecified but constant shift in phase. This signal shall be held static at all times except when used to precede the active-going edge of WRITE GATE by at least one bit cell but not more than 16 bit cells and when WRITE GATE is active.

5. Command Structure

All command, status, and parameter information passed between the selected device and the host shall be transferred via the CONTROL BUS and shall conform to the command protocol defined in this standard.

The command protocol requires that each command sequence consists of a two-byte transfer. The first byte, the command byte, shall always be transferred from the host to the selected device. The second byte, the parameter byte, may be transferred from the host to the selected device or from the selected device to the host. The direction of the transfer of the parameter byte is determined by the state of the BUS DIRECTION OUT signal.

Command codes 80 Hex to FF Hex are reserved for commands outside the scope of this standard. It is desirable that this device-dependent level interface operates with an as yet undefined higher level interface. By reserving the most significant bit of the command code, a simple check can identify commands that are either executed or passed on by such a higher level interface. If a reserved command is received, the device shall set the ATTENTION condition and the illegal command bit in the general status byte.

The command byte, therefore, indicates the particular function that the selected device is to perform. This may include functions such as accepting parametric information from the host, performing requested head motion, or reporting specific status conditions. The command byte also conditions the device as to the direction of the transfer of the parameter byte portion of the command sequence.

The parameter byte completes the command sequence by providing the parameter or status information demanded by the command byte. In cases where the command byte is sufficient to

indicate the complete nature of the command, the general status byte is transferred as parameter byte to complete the command sequence.

In the following paragraphs all defined command sequences are specified. They are divided into two groups: One that requires the parameter byte transferred to the device (parameter out) and one that requires the parameter byte transferred to the host (parameter in). Note that there is a further subdivision in each group. There are certain mandatory commands that shall be implemented in all devices conforming to this standard. There is a second class of commands that are defined but may or may not be implemented in a particular vendor's device. In a third class of commands, vendors may implement unique commands that are not defined in this standard.

There are two kinds of commands: immediate commands and time-dependent commands.

For immediate commands, the active-going edge of the second BUS ACKNOWLEDGE shall not be generated until the required action has been performed. In the case that action is not performed, ATTENTION condition shall be set prior to the active-going edge of the BUS ACKNOWLEDGE signal that is returned as a response to PARAMETER REQUEST.

For time-dependent commands, the ATTENTION condition shall be set when the action for the time-dependent command is completed. The resetting of the ATTENTION condition by the immediate command, CLEAR FAULT or CLEAR ATTENTION, completes the time-dependent command.

All commands, once in progress, shall proceed to completion utilizing parameters established prior to the issuance of the command. While a time-dependent command (denoted in Tables 4 and 5 by an asterisk(*)) is in progress (signaled in the general status byte by the busy executing bit (Bit 6)) and if the device is not busy, as denoted by the BUSY signal at the interface (see 4.2.7), a new time-dependent command is issued. The new time-dependent command shall be rejected by setting the ATTENTION condition and the command reject bit in sense byte 1.

A new time-dependent command may be issued only after the current time-dependent command has completed and the busy executing bit of the general status byte has been cleared.

Also, while a time-dependent command is in progress (signaled in the general status byte by the busy executing bit (Bit 6)), the device shall accept immediate commands if not busy, as denoted by the BUSY signal at the interface (see 4.2.7).

Although all commands are defined individually, there are logical groupings of commands that represent functional operations. For example, the loading of parameter information

(cylinder address) and the execution of a particular operation (SEEK). Unusual command sequences within such groupings may result in violations of an implied protocol and will cause responses that are implementation dependent and will vary among vendors.

It should be noted that in some implementations such violations may cause a loss of data or functional error with or without an error indication. The user is urged to consult vendors' specifications to determine what results, if any, are defined for such command sequences.

5.1 Commands with Parameter Out. All commands defined in this section require a parameter byte to be transferred to the device. These commands are summarized in Table 4.

5.1.1 Mandatory Commands. All commands defined in this section shall be implemented in all devices.

5.1.1.1 ATTENTION CONTROL (Command Code 40 Hex). This command shall condition the selected device to enable or disable its attention circuitry based on the value of the parameter byte as shown in Figure 14.

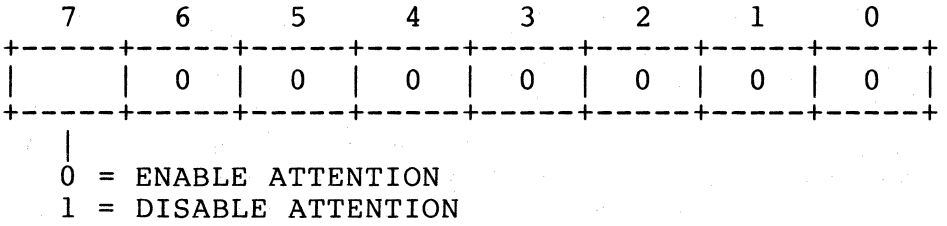


Figure 14
Parameter Byte for ATTENTION CONTROL

This command allows the host to selectively ignore attention requests from certain devices on the interface. This might be done in response to a device that generates spurious attention requests due to a malfunction.

The ENABLE ATTENTION command shall cause the selected device to gate its internal ATTENTION condition onto the party line (wired OR) ATTENTION signal. The DISABLE ATTENTION command shall cause the selected device to disable the gating of the internal ATTENTION condition onto the party line ATTENTION signal. This command shall have no impact on the function of the radial status returned with the ATTENTION IN STROBE signal (see 4.2.3.2)

Devices shall be initialized with the attention circuitry enabled.

5.1.1.2 WRITE CONTROL (Command Code 41 Hex). This command shall condition the selected device to enable or disable its write circuitry based on the value of the parameter byte as shown in Figure 15.

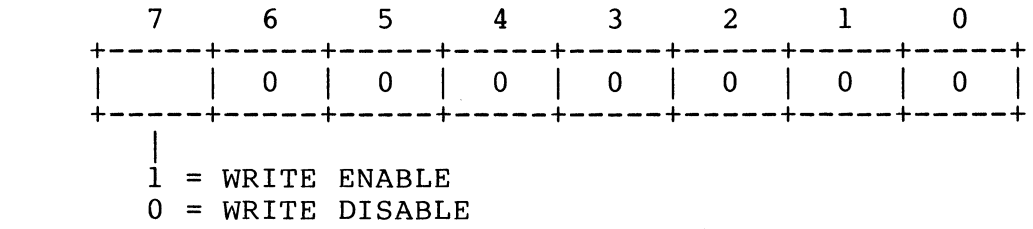


Figure 15

Parameter Byte for WRITE CONTROL

This command is used in conjunction with the WRITE GATE signal and therefore merely enables the write circuitry, while the WRITE GATE signal activates the circuitry at the proper time. An active WRITE GATE signal, while the device's write circuitry is disabled, shall result in no data being recorded.

Devices shall be initialized with the write circuitry disabled.

A WRITE CONTROL command executed during a write operation is a violation of protocol.

5.1.1.3 SET UPPER CYLINDER ADDRESS (Command Code 42 Hex). This command shall condition the selected device to accept the parameter byte as the most significant byte of a cylinder address.

This command is used in conjunction with the SEEK command (see 5.2.1.4) and therefore is a means of supplying the most significant byte of a target cylinder address.

This command shall not cause any head motion. Loading a cylinder address outside the range of a device shall not cause an error unless a subsequent SEEK command is issued to that illegal cylinder.

Devices shall be initialized with the target cylinder address equal to ZERO.

5.1.1.4 SET LOWER CYLINDER ADDRESS (Command Code 43 Hex). This command shall condition the selected device to accept the parameter byte as the least significant byte of a cylinder address.

This command is used in conjunction with the SEEK command (see 5.2.1.4) and therefore is a means of supplying the least significant byte of a target cylinder address.

This command shall not cause any head motion. Loading a cylinder address outside the range of a device shall not cause an error unless a subsequent SEEK command is issued to that illegal cylinder.

Devices shall be initialized with the target cylinder address equal to ZERO.

5.1.1.5 SELECT MOVING HEAD. There are two SELECT MOVING HEAD commands, one is time dependent, the other is immediate (NOT time dependent). It is mandatory that at least one SELECT MOVING HEAD command be implemented.

This command shall condition the selected device to accept the parameter byte as the binary address of the head selected for read or write operations. This command shall enable the moving heads and shall disable the fixed heads.

A SELECT MOVING HEAD command issued during a read or write operation is a violation of protocol.

The device shall set the ATTENTION condition and the illegal parameter bit in the general status byte upon receipt of a head address outside the head address range of the device.

Devices shall be initialized with moving head zero selected.

5.1.1.5.1 SELECT MOVING HEAD (Immediate)(Command Code 44 Hex). This command shall be used when the time to select a moving head is less than the normal command cycle of the interface.

5.1.1.5.2 SELECT MOVING HEAD (Time Dependent)(Command Code 45 Hex). This command shall be used when the time to select a moving head is longer than the normal command cycle of the interface.

This command is in effect a SEEK command and as such shall set the ATTENTION condition upon the completion of the select operation.

This SELECT MOVING HEAD command is a time-dependent command and as such shall set the busy executing bit in the general status byte (see 5.4.1.7) while command execution is in process. Also, the device shall exercise appropriate control over the BUSY signal at the interface (see 4.2.7).

5.1.1.6 Reserved Mandatory Commands. Command codes 46 Hex through 4F Hex are reserved for future mandatory parameter out commands.

5.1.2 Optional Commands. Commands defined in this section may or may not be implemented in a particular device. Individual vendor's specifications should be consulted.

Issuance of an optional command to a device in which it is not implemented shall set the ATTENTION condition and the illegal command bit in the general status byte.

5.1.2.1 LOAD ATTRIBUTE NUMBER (Command Code 50 Hex). This command shall condition the selected device to accept the parameter byte as the number of a device attribute as defined in Table 6. This command prepares the device for a subsequent LOAD DEVICE ATTRIBUTE command or REPORT DEVICE ATTRIBUTE command (see 5.1.2.2 and 5.2.2.1). This command may be issued at any time.

5.1.2.2 LOAD DEVICE ATTRIBUTE (Command Code 51 Hex). This command shall condition the selected device to accept the parameter byte as the new value of a device attribute. The number of the device attribute shall have been previously defined by the LOAD ATTRIBUTE NUMBER command (see 5.1.2.1).

5.1.2.3 SELECT FIXED HEAD (Command Code 52 Hex). This command shall condition the selected device to accept the parameter byte as the binary head address of the fixed head to be accessed during a read or write operation. This command shall enable the fixed heads and shall disable the moving heads. (See Figure 16.)

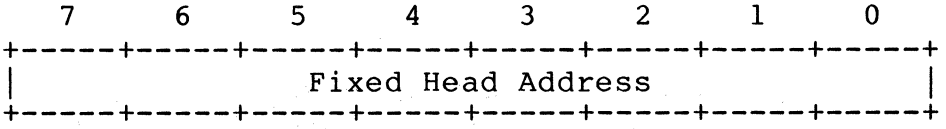


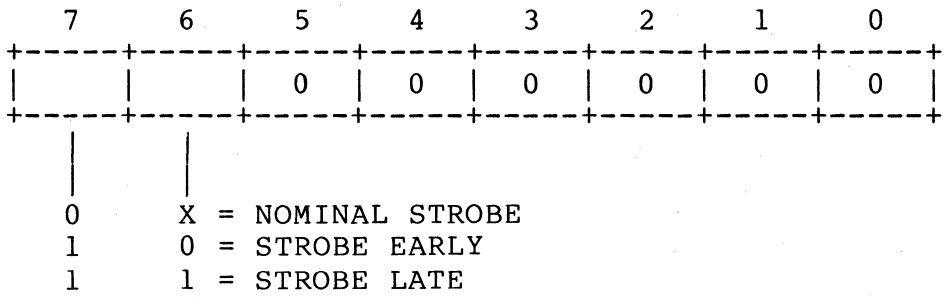
Figure 16
Fixed Head Address

Any head selection command issued during a read or write operation is a violation of protocol.

The device shall set the ATTENTION condition and the illegal parameter bit of the general status byte upon receipt of a head address outside the head address range of the device.

Devices shall be initialized with the fixed heads disabled.

5.1.2.4 READ CONTROL (Command Code 53 Hex). This command shall condition the selected device to modify its read timing. The modification of the timing is defined by the value of the parameter byte as shown in Figure 17.



NOTE: X = Don't care.

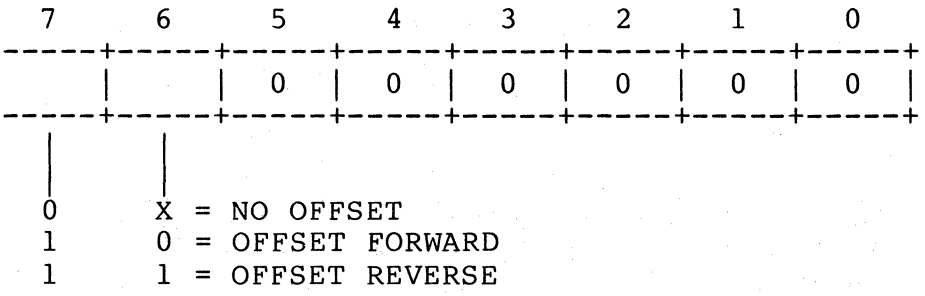
Figure 17

Parameter Byte for READ CONTROL

When set, the READ CONTROL shall remain in the one state and will only return to the nominal strobe state by a new READ CONTROL command, REZERO command or initial state.

The device shall be initialized with nominal strobe timing.

5.1.2.5 OFFSET CONTROL (Command Code 54 Hex). This command shall condition the selected device to modify the position of the moving head(s). The offset modification is defined by the value of the parameter byte as shown in Figure 18.



NOTE: X = Don't care.

Figure 18

Parameter Byte for OFFSET CONTROL

The OFFSET CONTROL shall be reset to no offset positioning by every SEEK command, REZERO command, or initial state.

Furthermore, the setting of any offset has the effect of disabling the write circuitry and any write operation attempted shall set the ATTENTION condition and the command reject bit in sense byte 1.

The OFFSET CONTROL command is in effect a SEEK command and as such shall set the ATTENTION condition upon the completion of the offset operation.

The OFFSET CONTROL command is a time-dependent command and as such shall set the busy executing bit in the general status byte (see 5.4.1.7) while command execution is in process. Also, the device shall exercise appropriate control over the BUSY signal at the interface (see 4.2.7).

The device shall be initialized with no offset.

5.1.2.6 SPIN CONTROL (Command Code 55 Hex). This command shall condition the selected device to enter a spin-up or spin-down cycle based on the value of the parameter byte as shown in Figure 19.

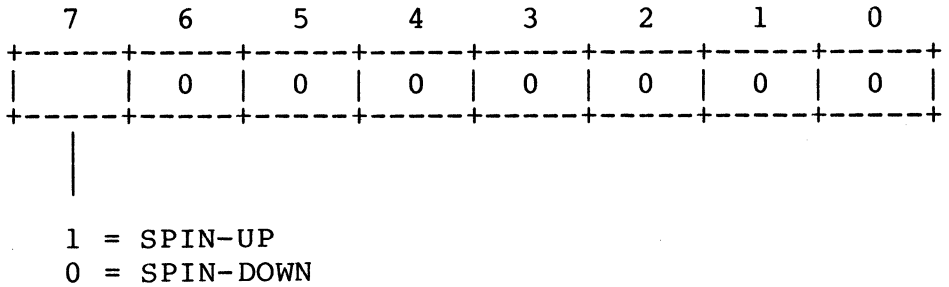


Figure 19

Parameter Byte for SPIN CONTROL

A spin-up cycle shall consist of starting the rotation of the spindle. A spin-down cycle shall consist of stopping the rotation of the spindle.

Upon completion of a spin control cycle, the device shall set the ATTENTION condition. Issuing a SPIN-UP command to a device in which the spindle is already at full speed, or issuing a SPIN-DOWN command to a device in which the spindle has already stopped, shall also set the ATTENTION condition.

The SPIN CONTROL command is a time-dependent command and as such shall set the busy executing bit in the general status byte

(see 5.4.1.7) while command execution is in process. Also, the device shall exercise appropriate control over the BUSY signal at the interface (see 4.2.7).

See vendor specification for initial state of the SPIN CONTROL.

5.1.2.7 LOAD BYTES PER SECTOR HIGH (Command Code 56 Hex). This command shall condition the selected device to accept the parameter byte as the most significant byte of a 24-bit number that represents the total number of bytes that will occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the most significant byte of the bytes per sector value.

Upon completion of the execution of the PARTITION TRACK command the contents of this byte shall be set into the bytes per sector high attribute (13 Hex). See Table 6 and 5.3.12.

This command functions in conjunction with the LOAD BYTES PER SECTOR MEDIUM and LOW commands (see 5.1.2.8 and 5.1.2.9) and operates in the same way.

5.1.2.8 LOAD BYTES PER SECTOR MEDIUM (Command Code 57 Hex). This command shall condition the selected device to accept the parameter byte as the medium significant byte of a 24-bit number that represents the total number of bytes that will occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the medium significant byte of the bytes per sector value.

Upon completion of the execution of the PARTITION TRACK command, the contents of this byte shall be set into the bytes per sector medium attribute (14 hex). See Table 6 and 5.3.13.

This command functions in conjunction with the LOAD BYTES PER SECTOR HIGH and LOW commands (see 5.1.2.7 and 5.1.2.9) and operates in the same way.

5.1.2.9 LOAD BYTES PER SECTOR LOW (Command Code 58 Hex). This command shall condition the selected device to accept the

Table 6
Device Attributes

Attribute	Number	Parameter
User ID	00 Hex	User defined
Model ID High	01 Hex	Vendor defined
Model ID Low	02 Hex	Vendor defined
Revision ID	03 Hex	Vendor defined
Device Type ID	0D Hex	Device dependent
Table Modification	0E Hex	Action dependent
Table ID *	0F Hex	Vendor defined
Bytes per Track High	10 Hex	MSB of number of bytes
Bytes per Track Medium	11 Hex	MedSB of number of bytes
Bytes per Track Low	12 Hex	LSB of number of bytes
Bytes per Sector High	13 Hex	MSB of number of bytes
Bytes per Sector Medium	14 Hex	MedSB of number of bytes
Bytes per Sector Low	15 Hex	LSB of number of bytes
Sector Pulses Per Track High	16 Hex	MSB of number of SECTOR pulses
Sector Pulses Per Track Medium	17 Hex	MedSB of number of SECTOR pulses
Sector Pulses Per Track Low	18 Hex	LSB of number of SECTOR pulses
Sectoring Method	19 Hex	Sectoring method
Number of Cylinder High	20 Hex	MSB of number of cylinders
Number of Cylinder Low	21 Hex	LSB of number of cylinders
Number of Moving Heads	22 Hex	Number of heads
Number of Fixed Heads	23 Hex	Number of heads
Head Select Mode	24 Hex	Selection mode
Encoding Method #1	30 Hex	Encoding method
Preamble #1 Length	31 Hex	Number of bytes
Preamble #1 Pattern	32 Hex	Preamble pattern
Sync #1 Pattern	33 Hex	Sync pattern
Postamble #1 Length	34 Hex	Number of bytes
Postamble #1 Pattern	35 Hex	Postamble pattern
Gap #1 Length	36 Hex	Number of bytes
Gap #1 Pattern	37 Hex	Gap pattern
Encoding Method #2	40 Hex	Encoding method
Preamble #2 Length	41 Hex	Number of bytes
Preamble #2 Pattern	42 Hex	Preamble pattern
Sync #2 Pattern	43 Hex	Sync pattern
Postamble #2 Length	44 Hex	Number of bytes
Postamble #2 Pattern	45 Hex	Postamble pattern
Gap #2 Length	46 Hex	Number of bytes
Gap #2 Pattern	47 Hex	Gap pattern

NOTES:

(1) The range of numbers E0 Hex through FF Hex is reserved for unique vendor applications. All other unused numbers are reserved for future standardization.

(2) All unused bits in parameters shall be ZERO.

* See 5.3.8 for validity of this byte.

parameter byte as the least significant byte of a 24-bit number that represents the total number of bytes that will occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the least significant byte of the bytes per sector value.

Upon completion of the execution of the PARTITION TRACK command, the contents of this byte shall be set into the bytes per sector low attribute (15 Hex). See Table 6 and 5.3.14.

This command functions in conjunction with the LOAD BYTES PER SECTOR HIGH and MEDIUM commands (see 5.1.2.7 and 5.1.2.8) and operates in the same way.

5.1.2.10 LOAD SECTOR PULSES PER TRACK HIGH (Command Code 59 Hex). This command shall condition the selected device to accept the parameter byte as the most significant byte of a 24-bit number that represents the total number that will control the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the most significant byte of the sector pulses per track value.

Upon completion of the execution of the PARTITION TRACK command the contents of this byte shall be set into the sector pulses per track high attribute (16 Hex). See Table 6 and 5.3.15.

This command functions in conjunction with the LOAD SECTOR PULSES PER TRACK MEDIUM and LOW commands (see 5.1.2.11 and 5.1.2.12) and operates in the same way.

5.1.2.11 LOAD SECTOR PULSES PER TRACK MEDIUM (Command Code 5A Hex). This command shall condition the selected device to accept the parameter byte as the medium significant byte of a 24-bit number that represents the total number that will control the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the medium significant byte of the sector pulses per track value.

Upon completion of the execution of the PARTITION TRACK

command, the contents of this byte shall be set into the sector pulses per track medium attribute (17 Hex). See Table 6 and 5.3.16.

This command functions in conjunction with the LOAD SECTOR PULSES PER TRACK HIGH and LOW commands (see 5.1.2.10 and 5.1.2.12) and operates in the same way.

5.1.2.12 LOAD SECTOR PULSES PER TRACK LOW (Command Code 5B Hex). This command shall condition the selected device to accept the parameter byte as the least significant byte of a 24-bit number that represents the total number that will control the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices when a PARTITION TRACK command (see 5.2.2.6) is executed.

This command is used in conjunction with the PARTITION TRACK command and is a means of supplying the least significant byte of the sector pulses per track value.

Upon completion of the execution of the PARTITION TRACK command the contents of this byte shall be set into the sector pulses per track low attribute (18 Hex). See Table 6 and 5.3.17.

This command functions in conjunction with the LOAD SECTOR PULSES PER TRACK HIGH and MEDIUM commands (see 5.1.2.10 and 5.1.2.11) and operates in the same way.

5.1.2.13 LOAD READ PERMIT HIGH (Command Code 6B Hex). This command shall condition the selected device to accept the parameter byte as the most significant byte of a 16-bit cylinder address defining a programmable read permit area on the device.

The device shall allow read operations to occur only on cylinders with an address equal to or greater than the cylinder address programmed in the device via this command.

Issuing this command while READ GATE is active is a violation of protocol.

The device shall initialize read permit high to ZERO.

5.1.2.14 LOAD READ PERMIT LOW (Command Code 6C Hex). This command shall condition the selected device to accept the parameter byte as the least significant byte of a 16-bit cylinder address defining a programmable read permit area on the device.

This command functions in conjunction with the LOAD READ PERMIT HIGH command (see 5.1.2.13) and operates in the same way.

The device shall initialize read permit low to ZERO.

5.1.2.15 LOAD WRITE PERMIT HIGH (Command Code 6D Hex). This command shall condition the selected device to accept the parameter byte as the most significant byte of a 16-bit cylinder address defining a programmable write permit area on the device.

The device shall allow write operations to occur only on cylinders with an address equal to or greater than the cylinder address programmed in the device via this command.

Issuing this command while WRITE GATE is active is a violation of protocol.

The device shall initialize write permit high to ZERO.

5.1.2.16 LOAD WRITE PERMIT LOW (Command Code 6E Hex). This command shall condition the selected device to accept the parameter byte as the least significant byte of a 16-bit cylinder address defining a programmable write permit area on the device.

This command functions in conjunction with the LOAD WRITE PERMIT HIGH command (see 5.1.2.15) and operates in the same way.

The device shall initialize write permit low to ZERO.

5.1.2.17 LOAD TEST BYTE (Command Code 6F Hex). This command shall condition the selected device to accept the parameter byte as a special test byte that shall be returned to the host as part of the REPORT TEST BYTE command (see 5.2.2.13).

This command pair allows the host to test the integrity of data transfer over the CONTROL BUS.

5.1.2.18 Reserved Optional Commands. Command codes 5C Hex through 6A Hex are reserved for future optional parameter out commands.

5.1.2.19 Vendor Unique Commands. Command codes 70 Hex through 7F Hex are reserved for commands with parameter out that may be defined solely by the individual vendor. Particular device specifications should be consulted.

5.2 Commands with Parameter In. The commands defined in this section require a parameter byte to be transferred to the host. These commands are summarized in Table 5.

5.2.1 Mandatory Commands. All commands defined in this section shall be implemented in all devices.

5.2.1.1 REPORT ILLEGAL COMMAND (Command Code 00 Hex). This command shall force the illegal command bit to be set in the general status byte (see 5.4). The general status byte, with the illegal command bit equal to ONE, is returned to the host by the parameter byte of the command sequence.

5.2.1.2 CLEAR FAULT (Command Code 01 Hex). This command shall cause all fault status bits of the selected device to be reset, provided the FAULT condition has passed. If the FAULT condition persists, the appropriate status bit shall continue to be equal to ONE. The general status byte, cleared of previous fault status, shall be returned by the parameter byte of the command sequence.

The CLEAR FAULT command shall also reset the ATTENTION condition caused by the FAULT condition, again only if the FAULT condition no longer exists.

5.2.1.3 CLEAR ATTENTION (Command Code 02 Hex). This command shall cause the ATTENTION condition to be reset in the selected device. The general status byte shall be returned by the parameter byte of the command sequence.

If the error or other condition that caused the ATTENTION condition persists, the ATTENTION condition shall not be set again. If, however, the condition is reset and then the error reoccurs, the ATTENTION condition shall be set again.

5.2.1.4 SEEK (Command Code 03 Hex). This command shall cause the selected device to seek to the cylinder identified as the target cylinder by the LOAD CYLINDER ADDRESS commands (see 5.1.1.3 and 5.1.1.4). The general status byte shall be returned to the host by the parameter byte of the command sequence with the busy executing bit set (see 5.4.1.7).

The SEEK command shall set the ATTENTION condition and the illegal parameter bit in the general status byte if the target cylinder address is outside the cylinder address range of the device.

Upon the completion of any SEEK (including a ZERO-LENGTH SEEK), the device shall clear the busy executing bit in the general status byte and set the ATTENTION condition.

This command shall reset the OFFSET CONTROL to no offset.

5.2.1.5 REZERO (Command Code 04 Hex). This command shall cause the selected device to position the moving head(s) over cylinder zero and reset READ CONTROL to nominal strobe and the OFFSET CONTROL to no offset. The general status byte shall be

returned to the host by the parameter byte of the command sequence with the busy executing bit set (see 5.4.1.7).

Upon the completion of the positioning of the moving head(s) over cylinder zero, the device shall clear the busy executing bit in the general status byte and set the ATTENTION condition.

5.2.1.6 REPORT SENSE BYTE 2 (Command Code 0D Hex). The command shall cause the selected device to return sense byte 2 by the parameter byte of the command sequence. No other action shall be taken in the device.

5.2.1.7 REPORT SENSE BYTE 1 (Command Code 0E Hex). This command shall cause the selected device to return sense byte 1 by the parameter byte of the command sequence. No other action shall be taken in the device.

5.2.1.8 REPORT GENERAL STATUS BYTE (Command Code 0F Hex). This command shall cause the selected device to return the general status byte by the parameter byte of the command sequence. This command shall not perform any other function in the device and acts as a "no-op" in order to allow the host to monitor the device's general status byte without changing any device condition.

5.2.1.9 Reserved Mandatory Commands. Command codes 05 Hex through 0C Hex are reserved for future mandatory parameter in commands.

5.2.2 Optional Commands. Commands defined in this section may or may not be implemented in a particular device. Individual vendor's specifications should be consulted.

Issuance of an optional command to a device in which it is not implemented shall set the ATTENTION condition and the illegal command bit in the general status byte.

5.2.2.1 REPORT DEVICE ATTRIBUTE (Command Code 10 Hex). This command shall cause the selected device to return a byte of information that is the device attribute, the number of which was defined in the LOAD ATTRIBUTE NUMBER command (see 5.1.2.1). The contents of the byte is defined by Table 6 and 5.3.

5.2.2.2 SET ATTENTION (Command Code 11 Hex). This command shall cause the selected device to set the ATTENTION condition. No other action shall be caused.

The general status byte shall be transferred to the host by the parameter byte of the command sequence.

5.2.2.3 Multiported Devices. The following two commands, RESERVE DEVICE and RELEASE DEVICE, shall be valid only with devices that have more than one port.

Reserving a device shall cause it to act upon commands from the reserving port only and either disregard all other ports (for example, alternate ports) by making BUSY active or only respond to STATUS REQUEST and FORCED RELEASE commands from the alternate ports.

A device may be implicitly or explicitly reserved to a port thereby limiting a device's activity with respect to the alternate ports.

A device shall be implicitly reserved to a port whenever it has been selected from that port and remains reserved until it has been deselected.

A device shall be explicitly reserved by a RESERVE DEVICE command and remains reserved until explicitly released by a RELEASE DEVICE command from the same port or a FORCED RELEASE from an alternate port.

Multiported devices shall have two types of status reporting: common status and port-specific status. Common status shall be-reported to all ports while port-specific status shall be only-reported to the port that issued the command when the status was set. Port-specific status shall only be cleared by the port to which it is port specific. Common status, unless self-clearing, shall be cleared individually by each port.

A forced release shall occur if a device is reserved and there is a detection of port enable transition from the active to the inactive state and all CONTROL BUS BIT 0 - 7 lines are active. A FORCED RELEASE shall cause the device to release the reserved port, set the forced release bit in sense byte 2 and set the ATTENTION condition to the port that was previously reserved.

In a multiported device, the inactive state of the PORT ENABLE signal on one port shall not cause other ports to become disabled.

Errors are only reported to the port where the error occurred or the port that initiated the operation.

Powering down a device shall release the reserved port.

5.2.2.3.1 RESERVE DEVICE (Command Code 12 Hex). This command shall cause the selected device to be reserved to the port through which this command was received.

Bit 4 of sense byte 2 of the alternate ports shall be set, and bit 2 of sense byte 2 of the reserving port shall be set.

The device may then either (at the discretion of the vendor) make BUSY active on the alternate ports or accept a REPORT GENERAL STATUS command, REPORT SENSE BYTE 1 command, or REPORT SENSE BYTE 2 command. If the latter approach is used only these commands are valid. All other commands shall be rejected by setting the ATTENTION condition and the command reject bit in sense byte 1.

5.2.2.3.2 RELEASE DEVICE (Command Code 13 Hex). This command shall cause the selected device to be released. Bit 4 of sense byte 2 of the alternate ports shall be reset and bit 2 of sense byte 2 of the reserving port shall be reset.

After deselection the device shall then be available for either implicit or explicit reserving by any port.

5.2.2.4 SELECTIVE RESET (Command Code 14 Hex). This command shall cause the selected device to reach initial state (see 4.2.1). This is a time-dependent command and, as such, shall set the busy executing bit prior to the assertion of the acknowledge to PARAMETER REQUEST and shall be reflected in the returned general status byte. Upon completion of the parameter byte transfer, the device shall go to the initial state and all reset. When the initial state is reached bit 0 of sense byte 2 will be set. (This causes the setting of the ATTENTION condition).

5.2.2.5 SEEK TO LANDING ZONE (Command Code 15 Hex). This command shall cause the selected device to seek to a defined landing zone. The general status byte with not ready bit set shall be returned to the host by the parameter byte of the command sequence.

Upon completion of the positioning of the moving head(s) over the landing zone, the device shall set the ATTENTION condition. If the device cannot successfully seek to the landing zone, it shall set the ATTENTION condition and set bit 0 of sense byte 1.

The SEEK TO LANDING ZONE command is a time-dependent command and, as such, shall set the busy executing bit in the general status byte (see 5.4.1.7) while command execution is in process. Also, the device shall exercise appropriate control over the BUSY signal at the interface (see 4.2.7).

5.2.2.6 PARTITION TRACK (Command Code 16 Hex). This command shall cause the selected device to reconfigure the arrangement of SECTOR pulse generation according to parameters

received via the LOAD BYTES PER SECTOR command, the LOAD SECTOR PULSES PER TRACK commands, or both, (see 5.1.2.7 to 5.1.2.12). The general status byte shall be returned to the host by the parameter byte of the command sequence.

The PARTITION TRACK command is a time-dependent command and, as such, shall set the busy executing bit in the general status byte returned by this command (see 5.4.1.7) and it is to remain set while this command execution is in process. Also, the device shall exercise appropriate control over the BUSY signal at the interface (see 4.2.7).

Upon the completion of execution of this command, the bytes per sector and the sector pulses per track will be updated in the attribute table (Table 6) and also bit 6 of attribute byte 0E Hex will be cleared and this shall set the ATTENTION condition.

The PARTITION TRACK command shall set the ATTENTION condition and the illegal parameter bit in the general status byte if the bytes per sector, the sector pulses per track, or both create a set that is outside the range of the device.

Issuing this command while READ GATE or WRITE GATE is active, or activating READ GATE or WRITE GATE while this command is executing, is a violation of protocol.

5.2.2.7 REPORT CYLINDER HIGH (Command Code 29 Hex). This command shall cause the selected device to return a byte of information that is the most significant byte of a 16-bit number that indicates the cylinder address of the current position of the moving heads. This number shall not reflect the most recent cylinder address set by the SET CYLINDER ADDRESS commands (see 5.1.1.3 and 5.1.1.4) unless there has been an intervening SEEK command completed (see 5.2.1.4).

If executed during a seek operation, the information returned shall be ascertained by the vendor specification.

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.8 REPORT CYLINDER LOW (Command Code 2A Hex). This command shall cause the selected device to return a byte of information that is the least significant byte of a 16-bit number that indicates the cylinder address of the current position of the moving heads. This number shall not reflect the most recent cylinder address set by the SET CYLINDER ADDRESS commands (see 5.1.1.3 and 5.1.1.4) unless there has been an intervening SEEK command completed (see 5.2.1.4).

If executed during a seek operation, the information returned shall be ascertained by the vendor specification.

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.9 REPORT READ PERMIT HIGH (Command Code 2B Hex). This command shall cause the selected device to return a byte of information that is the most significant byte of a 16-bit number that indicates the minimum cylinder address accessible for read operations. This number is programmed by the LOAD READ PERMIT commands. (See 5.1.2.13 and 5.1.2.14.)

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.10 REPORT READ PERMIT LOW (Command Code 2C Hex). This command shall cause the selected device to return a byte of information that is the least significant byte of a 16-bit number that indicates the minimum cylinder address accessible for read operations. This number is programmed by the LOAD READ PERMIT commands. (See 5.1.2.13 and 5.1.2.14.)

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.11 REPORT WRITE PERMIT HIGH (Command Code 2D Hex). This command shall cause the selected device to return a byte of information that is the most significant byte of a 16-bit number that indicates the minimum cylinder address accessible for write operations. This number is programmed by the LOAD WRITE PERMIT commands. (See 5.1.2.15 and 5.1.2.16.)

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.12 REPORT WRITE PERMIT LOW (Command Code 2E Hex). This command shall cause the selected device to return a byte of information that is the least significant byte of a 16-bit number that indicates the minimum cylinder address accessible for write operations. This number is programmed by the LOAD WRITE PERMIT commands. (See 5.1.2.15 and 5.1.2.16.)

The information shall be transferred by the parameter byte of the command sequence.

5.2.2.13 REPORT TEST BYTE (Command Code 2F Hex). This command shall cause the selected device to return a copy of the test byte transferred to the device via the LOAD TEST BYTE command. (See 5.1.2.17.)

The test byte shall be transferred by the parameter byte of the command sequence.

5.2.2.14 Reserved Optional Commands. Command codes 17 Hex through 28 Hex are reserved for future optional parameter in commands.

5.2.2.15 Vendor Unique Commands. Command codes 30 Hex through 3F Hex are reserved for commands with parameter in that may be defined solely by the individual vendor. Particular device specifications should be consulted.

5.3 Device Attribute Commands. These optional commands allow the host to manage the device's mass memory configuration. The host can interrogate each device on the daisy-chain bus to determine each device's attributes. The host may then modify the attributes of the devices to optimize parameters of the subsystem. Device type, model IDs, etc. are also provided.

The device attribute commands are: LOAD ATTRIBUTE NUMBER, LOAD DEVICE ATTRIBUTE, and REPORT DEVICE ATTRIBUTE. They are used to load or report device attributes, or to do both, but they do not cause any operation that effects the characteristics of the device. All device attribute commands are optional.

The parameter byte transferred with the LOAD ATTRIBUTE NUMBER command is used as a number to select a device attribute. This number remains valid for all subsequent load device attribute commands and report device attribute commands until changed by another LOAD ATTRIBUTE NUMBER command. If, for a received number, no attribute is assigned or the function is not implemented in the particular device, the ATTENTION condition and the illegal command bit in the general status byte shall be set.

The LOAD DEVICE ATTRIBUTE command shall set the selected attribute to the value transferred with the parameter byte. If the selected attribute can be read only and not be altered, the ATTENTION condition and the illegal command bit in the general status byte shall be set. If an illegal value is loaded, the ATTENTION condition and the illegal parameter bit in the general status byte shall be set.

The REPORT DEVICE ATTRIBUTE command shall cause the selected device to return the current value of the selected attribute. The REPORT DEVICE ATTRIBUTE command shall work for all implemented attributes.

5.3.1 User ID (Number 00 Hex). This attribute is a user-settable and -readable byte that can be used for any purpose. It is intended to be used to identify the characteristics of the device with which the host is communicating.

5.3.2 Model ID High (Number 01 Hex). This attribute is a read-only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify a particular device model.

5.3.3 Model ID Low (Number 02 Hex). This attribute is a read-only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify a particular device model.

5.3.4 Revision ID (Number 03 Hex). This attribute is a read-only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify the revision level of a particular device.

5.3.5 Reserved (Number 04 to 0C Hex). These attributes are reserved for future standardization.

5.3.6 Device Type ID (Number 0D Hex). This attribute is a read-only byte that identifies the device as defined as follows:

Value	Type
00 Hex	Not used
01 Hex	Nonremovable disk
02 Hex	Removable disk
03 Hex	Combination removable and nonremovable disk
04 to FF Hex	Reserved for future standardization

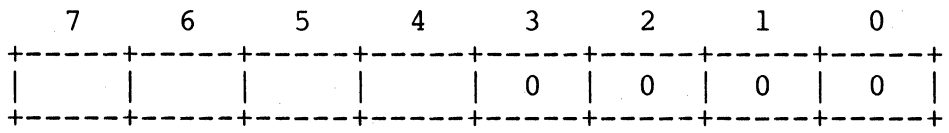
5.3.7 Attribute Table Modification (Number 0E Hex). The purpose of this attribute is to permit an orderly modification of the attribute table (see Table 6).

When the device goes to initial state, bit 7 of this attribute is set. After or during the initial state generation, the device initializes the attribute table. When the table is initialized by the device, bit 7 is reset and bit 6 is set. A host may at its option modify any byte and, if it does, the device shall reset bit 6. After all bytes have been modified, the host shall set bit 5.

When any subsequent byte, except number 0E Hex, is modified, bits 5 and 6 shall be reset and bit 4 shall be set. After a host has modified the byte(s), it shall execute a LOAD DEVICE ATTRIBUTE command with number 0E Hex selected. This shall reset bit 4 and set bit 5.

When either bit 6 or bit 5 is equal to ONE, the table is safe to use. As long as bit 6 remains set, the table contains the initial values set by the device.

This attribute is defined as shown in Figure 20.



Bit 7 = 1 — The attribute table is being modified by the device. This bit is set by the device and is reset by the device upon completion of the modification process.

Bit 6 = 1 — The initial device attribute values have not been modified. This bit is set by the device upon attaining the initial state and is reset when any LOAD DEVICE ATTRIBUTE command (except to number 0E Hex) is executed or the PARTITION TRACK command is executed.

Bit 5 = 1 — This bit, which is set by a host, is used to signify that the attribute table is complete and ready for use. This bit is reset on any LOAD DEVICE ATTRIBUTE command except to number 0E Hex. This bit can be set only by executing a LOAD DEVICE ATTRIBUTE command to number 0E Hex.

Bit 4 = 1 — This bit is set by the device after a LOAD DEVICE ATTRIBUTE command is executed after bit 5 was equal to a ONE. This bit can only be reset by executing a LOAD DEVICE ATTRIBUTE command to number 0E Hex.

The setting of this bit causes bit 5 of sense byte 2 to be set.

Bits 0,1,2,3 = 0 — These bits shall be ZERO.

Figure 20

Attribute Table Modification

5.3.8 Table ID (Number 0F Hex). This attribute defines the meaning of numbers 10 Hex to FF Hex.

When the value of this attribute is equal to 01 Hex, then see 5.3.9 to 5.3.39 for the definitions of the attributes for numbers 10 Hex to FF Hex.

When the value of this attribute is equal to FF Hex, see vendor specifications for meaning of numbers 10 Hex to FF Hex.

When the value of this attribute is equal to 00 Hex, the values of all table numbers are undefined.

All other values of this attribute are reserved for future standardization.

5.3.9 Bytes per Track High (Number 10 Hex). This attribute is the most significant byte of a 24-bit number that represents the total number of unformatted bytes that occur between active-going edges of INDEX pulses.

5.3.10 Bytes per Track Medium (Number 11 Hex). This attribute is the medium significant byte of a 24-bit number that represents the total number of unformatted bytes that occur between active-going edges of INDEX pulses.

5.3.11 Bytes per Track Low (Number 12 Hex). This attribute is the least significant byte of a 24-bit number that represents the total number of unformatted bytes that occur between active-going edges of INDEX pulses.

5.3.12 Bytes per Sector High (Number 13 Hex). This attribute is the most significant byte of a 24-bit number that represents the total number of bytes that occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse.

5.3.13 Bytes per Sector Medium (Number 14 Hex). This attribute is the medium significant byte of a 24-bit number that represents the total number of bytes that occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse.

5.3.14 Bytes per Sector Low (Number 15 Hex). This attribute is the least significant byte of a 24-bit number that represents the total number of bytes that occur between active-going edges of SECTOR pulses, and between the active-going edge of the INDEX pulse and the active-going edge of the first SECTOR pulse.

5.3.15 Sector Pulses per Track High (Number 16 Hex). This attribute defines the most significant byte of a 24-bit number that indicates the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices. The

SECTOR pulses are used to divide a track into sectors. The length of the sectors (distance between SECTOR pulses) is defined by the bytes per sector attribute.

5.3.16 Sector Pulses per Track Medium (Number 17 Hex). This attribute defines the medium significant byte of a 24-bit number that indicates the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices. The SECTOR pulses are used to divide a track into sectors. The length of the sectors (distance between SECTOR pulses) is defined by the bytes per sector attribute.

5.3.17 Sector Pulses per Track Low (Number 18 Hex). This attribute defines the least significant byte of a 24-bit number that indicates the number of SECTOR pulses between (but excluding) INDEX pulses generated by hard-sectored devices. The SECTOR pulses are used to divide a track into sectors. The length of the sectors (distance between SECTOR pulses) is defined by the bytes per sector attribute.

5.3.18 Sectoring Method (Number 19 Hex). This attribute defines the sectoring method used in the device. The attribute may allow either loading and reporting if the device provides two or more sectoring methods that are selectable by the host or it may allow reporting only if the device provides only one sectoring method. The sectoring methods are defined as follows:

Value	Sectoring Method
00 Hex	Invalid
01 Hex	Hard sectoring
02 Hex	Soft sectoring with dc-erased address marks
04 Hex	Soft sectoring with address marks with missing clocks
08 to EF Hex	Reserved for future standardization
F0 to FF Hex	Unique vendor methods

NOTE: Combinations of the above Hex codes are valid.

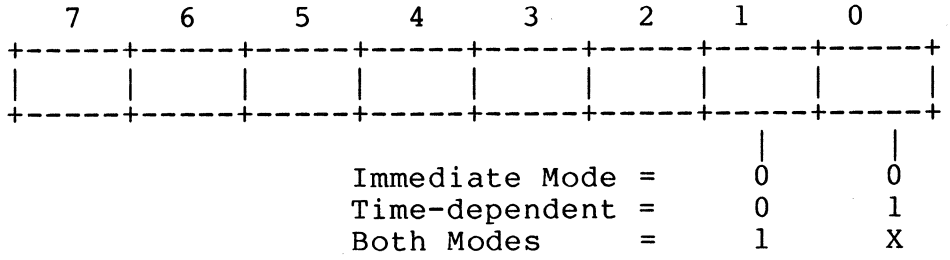
5.3.19 Number of Cylinders High (Number 20 Hex). This attribute is the most significant byte of a 16-bit number that represents the number of cylinders implemented in the device. This number is one greater than the maximum allowable cylinder address that can be addressed.

5.3.20 Number of Cylinders Low (Number 21 Hex). This attribute is the least significant byte of a 16-bit number that represents the number of cylinders implemented in the device. This number is one greater than the maximum allowable cylinder address that can be addressed.

5.3.21 Number of Moving Heads (Number 22 Hex). This attribute represents the number of moving heads implemented in the device. This number is one greater than the maximum allowable moving head address that can be addressed.

5.3.22 Number of Fixed Heads (Number 23 Hex). This attribute represents the number of fixed heads implemented in the device. This number is one greater than the maximum allowable fixed head address that can be addressed.

5.3.23 Head Select Mode (Number 24 Hex). This attribute defines the mode of selecting heads implemented in this device. See Figure 21 and 5.1.1.5.



NOTE: Bits 2 through 7 shall be ZERO.
X = (don't care).

Figure 21

Head Select Mode

5.3.24 Header Encoding Method #1 (Number 30 Hex). This attribute represents the header encoding method used for all fields labeled #1 in the device and is defined as follows:

Value	Encoding Method
00 Hex	Modified frequency modulation (MFM)
01 Hex	Group code recording (GCR)
02 Hex to EF Hex	Reserved for future standardization
F0 Hex to FF Hex	Unique vendor method

The definition of formatting requirements as defined by commands 30 Hex to 47 Hex is based on one of the formats in Figure 22.

5.3.25 Preamble #1 Length (Number 31 Hex). This attribute represents the minimum number of header preamble bytes required by the device.

5.3.26 Preamble #1 Pattern (Number 32 Hex). This attribute represents the pattern to be recorded in the header preamble bytes. The pattern shall be recorded starting with the most significant bit.

5.3.27 Synchronization #1 Pattern (Number 33 Hex). This attribute represents the pattern to be recorded in a one byte header synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit.

5.3.28 Postamble #1 Length (Number 34 Hex). This attribute represents the minimum number of header postamble bytes required by the device. A value of zero indicates that no postamble is required.

5.3.29 Postamble #1 Pattern (Number 35 Hex). This attribute represents the pattern to be recorded in the header postamble bytes. The pattern shall be recorded starting with the most significant bit.

5.3.30 Gap #1 Length (Number 36 Hex). This attribute represents the minimum number of bytes in the header gap (splice area) between postamble and the next preamble.

5.3.31 Gap #1 Pattern (Number 37 Hex). This attribute represents the pattern to be recorded in the header gap bytes. The pattern shall be recorded starting with the most significant bit.

5.3.32 Data Encoding Method #2 (Number 40 Hex). This attribute represents the encoding method used for all fields labeled, #2, in the device and is defined as follows:

Value	Encoding Method
00 Hex	Modified frequency modulation (MFM)
01 Hex	Group code recording (GCR)
02 Hex to EF Hex	Reserved for future standardization
F0 Hex to FF Hex	Unique vendor method

The definition of formatting requirements as defined by commands 30 Hex to 47 Hex is based on one of the formats in Figure 22.

5.3.33 Preamble #2 Length (Number 41 Hex). This attribute represents the minimum number of preamble bytes required by the device.

5.3.34 Preamble #2 Pattern (Number 42 Hex). This attribute represents the pattern to be recorded in the preamble bytes. The pattern shall be recorded starting with the most significant bit.

5.3.35 Synchronization #2 Pattern (Number 43 Hex). This attribute represents the pattern to be recorded in a one-byte synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit.

5.3.36 Postamble #2 Length (Number 44 Hex). This attribute represents the minimum number of postamble bytes required by the device. A value of zero indicates that no postamble is required.

5.3.37 Postamble #2 Pattern (Number 45 Hex). This attribute represents the pattern to be recorded in the postamble bytes. The pattern shall be recorded starting with the most significant bit.

5.3.38 Gap #2 Length (Number 46 Hex). This attribute represents the minimum number of bytes in the gap (splice area) between postamble and the next preamble.

5.3.39 Gap #2 Pattern (Number 47 Hex). This attribute represents the pattern to be recorded in the gap bytes. The pattern shall be recorded starting with the most significant bit.

5.4 Status Reporting

5.4.1 General Status Byte. See Table 7.

5.4.1.1 Bit 0 - Not Ready. The not ready bit shall be set if the device is unable to perform any head motion or read/write operation.

INDEX, SECTOR/ADDRESS MARK DETECTED, and READ/REFERENCE CLOCK are invalid when the device is not ready.

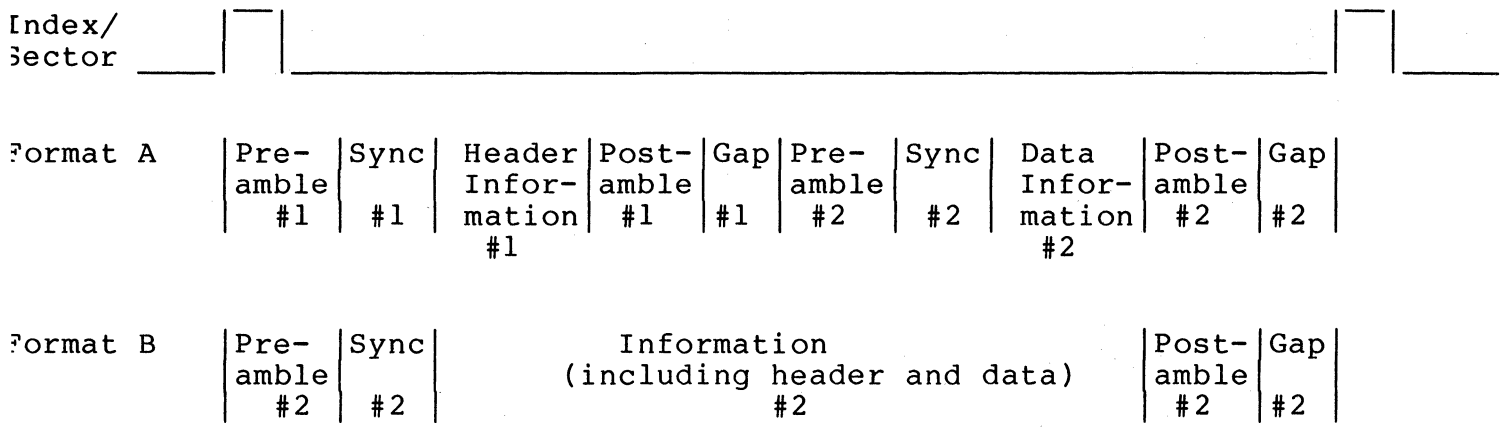


Figure 22

Sector Formats for Attributes 30 Hex to 47 Hex

Table 7

General Status Byte

Bit Number	Multiport (common/ specific)	Meaning	Mandatory /Optional	Method of Clearing
0	C	Not ready *	M	Self-clearing
1	S	Control bus error **	M	CLEAR FAULT command
2	S	Illegal command **	M	CLEAR FAULT command
3	S	Illegal parameter **	M	CLEAR FAULT command
4	C/S	Sense byte 1 ***	M	***
5	C/S	Sense byte 2 ***	M	***
6	C	Busy executing	M	Self-clearing
7	C	Normal complete **	M	CLEAR ATTENTION command

* The ready-to-not-ready and not-ready-to-ready transition shall set the ATTENTION condition.

** A ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

*** See sense byte 1 (5.4.2 and Table 9) and sense byte 2 (5.4.3 and Table 10).

Table 8
Command Busy/Not Ready Relationships

Function	Busy Signal	Not Ready Status	Busy Executing Status
No power	D*	N/A	N/A
Spinning up **	D	1	1
Spinning down **	D	1	1
Motor stopped	0	1	0
Idle condition	0	0	0
Missing media	0	1	0
Seeking **	D	0	1
Offsetting **	D	0	1
Power fault ***	0	0	0
Diagnostic	D	D	1
Read/Write operation	D ****	0	0

* D indicates device vendor-dependent state.

** Time-dependent operations.

*** Status is as indicated for noncatastrophic power faults. Catastrophic power faults result in undefined state for the three signals.

**** WARNING: If a device allows a command transfer during a read or write operation, data errors may result.

NOTE: In a multiport device, when the device is explicitly reserved, the above table does not apply to alternate ports. Resultant status may be vendor dependent.

Table 9
Sense Byte 1

Bit Number	Multiport (common/ specific)	Meaning	Mandatory /Optional	Method of Clearing
0	S	Seek error *	M	CLEAR FAULT command
1	S	Read/write fault *	M	CLEAR FAULT command
2	C	Power fault *	O	CLEAR FAULT command
3	S	Read/write permit violation*	O	CLEAR FAULT command
4	C	Speed error *	O	CLEAR FAULT command
5	S	Command reject *	M	CLEAR FAULT command
6	C/S	Other errors *	O	CLEAR FAULT command
7	C/S	Vendor unique errors*	O	CLEAR FAULT command

* A ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

Table 10
Sense Byte 2

Bit Number	Multiport (common/ specific)	Meaning	Mandatory /Optional	Method of Clearing
0	C	Initial state *	M	CLEAR ATTENTION command
1	C	Ready transition *	M	CLEAR ATTENTION command
2	S	Device reserved to this port	O	Self Clearing
3	S	Forced release *	O	CLEAR ATTENTION command
4	S	Device reserved to alternate port	O	Self Clearing
5	C	Device attribute table modified *	O	CLEAR ATTENTION command
6	C	Positioned within write protected area	M	Self Clearing
7	C/S	Vendor unique attentions *	O	CLEAR ATTENTION command

NOTE: If option is not implemented or undefined, its bit value must be ZERO.

* A ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

The not ready bit shall be reset when the device becomes ready.

The ready-to-not-ready and not-ready-to-ready transition shall set the ATTENTION condition.

See Table 8 for busy/not ready relationship.

5.4.1.2 Bit 1 - Control Bus Error. This bit shall be set if the device detects a protocol or parity error during the transfer of a command or parameter such as:

(1) CONTROL BUS PARITY error (if implemented)
(2) COMMAND REQUEST and BUS DIRECTION OUT inactive
(3) The level of the BUS DIRECTION OUT signal for the transfer of the parameter byte does not comply with the command code

(4) Two consecutive parameter cycles
(5) Two consecutive command cycles

The device shall not act upon the command transferred during a command/parameter cycle resulting in a control bus error. If the BUS DIRECTION OUT signal is inactive for the second byte and a control bus error has been detected, the device shall return the general status byte.

The control bus error bit shall be reset by the CLEAR FAULT command.

The detection of a control bus error shall set the ATTENTION condition.

5.4.1.3 Bit 2 - Illegal Command. This bit shall be set if the device detects an illegal command such as:

(1) The command received is not implemented in the device
(2) The device detected a parity error in the command byte, that will also set the control bus error bit

This error may occur because of a hardware or software error, during a self-configuring process or when receiving the REPORT ILLEGAL COMMAND command.

The illegal command bit shall be reset by the CLEAR FAULT command.

This error shall set the ATTENTION condition.

5.4.1.4 Bit 3 - Illegal Parameter. This bit shall be set if the device tests for and detects an illegal parameter or part of a parameter such as:

(1) The parameter is an address and exceeds the valid range (e.g. illegal head address)
(2) Any other illegal parameter value
(3) The device detected a parity error in the parameter byte, which will also set the bus error bit

The illegal parameter bit shall be reset by the CLEAR FAULT command.

This error shall set the ATTENTION condition.

5.4.1.5 Bit 4 - Sense Byte 1. This bit shall be generated by an OR function of all bits in the sense byte 1 status byte. The sense byte 1 bit shall be reset if all bits of the sense byte 1 are ZERO.

5.4.1.6 Bit 5 - Sense Byte 2. This bit shall be generated by an OR function of all bits in the sense byte 2 status byte. The sense byte 2 bit shall be reset if all bits of the sense byte 2 are ZERO.

5.4.1.7 Bit 6 - Busy Executing. This bit shall be set during the execution of all time-dependent commands and shall be set prior to the return of general status for those commands with parameters in that return the general status as the parameter (see Tables 4 and 5, and 5.2).

NOTE: This status bit is different from the BUSY interface signal (see 4.2.7).

5.4.1.8 Bit 7 - Normal Complete. This bit shall be set if the device has successfully completed the execution of a time-dependent command. (See Tables 4 and 5).

The normal complete bit shall be reset by the CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2 Sense Byte 1

5.4.2.1 Bit 0 - Seek Error. The seek error bit shall be set if a head positioning command (SEEK, REZERO, SEEK TO LANDING ZONE, or OFFSET) cannot be completed successfully.

If a REZERO command is required for recovery, a successful rezero operation shall reset this bit. If no REZERO command is required, the CLEAR FAULT command shall reset this bit.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.2 Bit 1 - Read/Write Fault. This bit shall be set if the device is not able to execute a READ command or a WRITE command or detects a fault during reading or writing. Two kinds of faults are distinguished:

(1) Bit 1 and Bit 5 shall be set if the execution of a read/write function requested by making READ GATE or WRITE GATE active is prevented by one of the following conditions:

(a) WRITE GATE active and writing disabled with a WRITE CONTROL command (see 5.1.1.2)
(b) WRITE GATE active and heads offset (see 5.1.2.5)

(2) Bit 1 only shall be set if the device detects a fault in its read/write section, for example:

(a) Simultaneous selection of more than one head
(b) WRITE GATE active but no write current

Optionally, the bit may be set if the device detects READ GATE and WRITE GATE active simultaneously.

The read/write fault bit shall be reset by the CLEAR FAULT command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.3 Bit 2 - Power Fault. This bit shall be set if the device tests for and detects a failure such as overvoltage or undervoltage in one of its supply voltages.

This bit shall be reset by the CLEAR FAULT command if the power failure no longer exists.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.4 Bit 3 - Read/Write Permit Violation. This bit shall be set if writing to the currently accessed track is not permitted (see 5.1.2.15 and 5.1.2.16) and WRITE GATE is active. This bit shall be set if reading from the currently accessed track is not permitted (see 5.1.2.13 and 5.1.2.14) and READ GATE is active.

This bit shall be reset by the CLEAR FAULT command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.5 Bit 4 - Speed Error. This bit shall be set if the device tests for and detects that the spindle speed is not within the tolerances specified by the device vendor.

This bit shall be reset by the CLEAR FAULT command if the spindle speed is within the specified tolerance.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.6 Bit 5 - Command Reject. This bit shall be set if the device received a command that it cannot execute at this time because of some interlocking condition or command sequence error.

This status bit may be set in combination with another status bit that defines the reason why the command was rejected. For example, the device is not ready and has received a command that cannot be executed (such as, SEEK when the disk is not rotating).

The command reject bit shall be reset by the CLEAR FAULT command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.7 Bit 6 - Other Errors. This bit shall be set if the device detects an error that is not covered by error status bits 0 through 5 or 7.

This bit shall be reset by the CLEAR FAULT command if the error no longer exists.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.2.8 Bit 7 - Vendor Unique Errors. This bit shall be set as defined by the device vendor.

This bit shall be reset by the CLEAR FAULT command if the error no longer exists.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.3 Sense Byte 2

5.4.3.1 Bit 0 - Initial State. This bit shall be set if an initialize procedure has been entered and the procedure has been completed.

The initial state bit shall be reset by a CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.3.2 Bit 1 - Ready Transition. This bit shall be set if a ZERO-to-ONE or a ONE-to-ZERO transition of the not ready bit (see 5.4.1.1) has occurred.

The ready transition bit shall be reset by a CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.3.3 Bit 2 - Device Reserved to This Port. This bit is used for multiport devices. It shall be set when the device is explicitly reserved to the port requesting sense byte 2.

This bit shall be reset when the device is released.

5.4.3.4 Bit 3 - Forced Release. If bit 2 of sense byte 2 was cleared by a FORCED RELEASE (see 5.2.2.3), then this bit shall be set. (This bit shall be set if the device previously reserved to the port requesting sense byte 2 has been released due to a FORCED RELEASE).

This bit shall be reset by a CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.3.5 Bit 4 - Device Reserved to Alternate Port. This bit is used for multiport devices. It shall be set when the device is explicitly reserved to a port other than the one requesting sense byte 2.

This bit shall be reset when the device is released.

5.4.3.6 Bit 5 - Device Attribute Table Modified. This bit shall be set if bit 4 of the table modification attribute number 0E Hex is set to a ONE (see 5.3.7).

This bit shall be reset by a CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

5.4.3.7 Bit 6 - Positioned within Write Protected Area. This bit shall be set by the device whenever WRITE CONTROL (see 5.1.1.2) has placed the device in the write disable state.

This bit shall be set by the device whenever the head is positioned within an area that has been defined as write protected (see 5.1.2.15 and 5.1.2.16) and the device is write enabled.

Any means that write-protects an area of the device shall be reflected in this bit.

This bit shall be cleared whenever the head(s) is positioned outside of the write protected area.

This bit is not defined during head movement.

5.4.3.8 Bit 7 - Vendor Unique Attentions. This bit shall be set as defined by the vendor.

This bit shall be reset by a CLEAR ATTENTION command.

The ZERO-to-ONE transition of this bit shall set the ATTENTION condition.

6. Timing Specification

The timing characteristics described in the following paragraphs are referenced to the signals at the device interface connector. The host timing shall be designed to accommodate cable delays and signal skew within the cable.

NOTE: This section takes precedence, with respect to actions and timing, over all preceding sections. All waveforms in the timing diagrams show the voltage levels of the signals. A minus (-) in front of a signal name indicates a LOW-active, HIGH-inactive signal. A plus (+) in front of a signal name indicates a HIGH-active, LOW-inactive signal.

6.1 CONTROL BUS Timing

6.1.1 SELECTION Timing. The active-going edge of the SELECT OUT/ATTENTION IN STROBE shall be used to clock the select information on the dedicated CONTROL BUS line into the device. A successful selection shall be acknowledged by making BUS ACKNOWLEDGE active. In the host, the inactive-going edge of the SELECT OUT/ATTENTION IN STROBE signal shall be used to sample the BUS ACKNOWLEDGE signal. If BUS ACKNOWLEDGE is not active within the specified time, the host shall assume that the desired device does not exist or is inoperable. The state of the BUSY signal indicates to the host if the selected device will accept commands and respond to the CONTROL BUS handshake.

Deselecting all devices shall be accomplished by an active-going edge of SELECT OUT/ATTENTION IN STROBE with none of the CONTROL BUS lines active.

The SELECTION timing is defined in Figure 23.

6.1.2 ATTENTION Timing. In general the timing of the party line ATTENTION signal (see 4.2.8) is asynchronous to the CONTROL BUS signals. However, if a command error or parameter error is detected, the ATTENTION condition shall be set and, if enabled, the ATTENTION signal shall be made active prior to the active-going edge of BUS ACKNOWLEDGE, which is returned as a response to the PARAMETER REQUEST. All other events (completion or errors) shall make ATTENTION active (if enabled) immediately, when they occur.

ATTENTION shall be made inactive prior to the active-going edge of the BUS ACKNOWLEDGE, which is returned as a response to the PARAMETER REQUEST of a CLEAR ATTENTION command or CLEAR FAULT command. ATTENTION shall not be made inactive by a CLEAR FAULT command if the error that caused ATTENTION to be made active still exists.

To determine which one of the attached devices has caused the party line ATTENTION signal to be active, the host polls all devices simultaneously by making the BUS DIRECTION OUT signal inactive and changing the SELECT OUT/ATTENTION IN STROBE from inactive to active. Each device shall then immediately gate its internal ATTENTION condition onto its dedicated CONTROL BUS line. Additionally, the selected device, if any, shall make the BUS ACKNOWLEDGE signal active.

The ATTENTION timing is defined in Figure 24.

6.1.3 CONTROL BUS Handshake Timing. The CONTROL BUS handshake is performed by three interface signals: COMMAND REQUEST, PARAMETER REQUEST, and BUS ACKNOWLEDGE.

The CONTROL BUS handshake timing is defined in Figures 25 and 26.

6.2 INDEX and SECTOR Timing. The timing of the INDEX signal and the SECTOR signal for hard-sectored devices is shown in Figure 27. There is one and only one INDEX pulse per revolution. The SECTOR pulses are used to divide a track into sectors. The device inhibits the SECTOR pulse during the INDEX pulse such that a SECTOR pulse is not transmitted at INDEX.

The INDEX signal and SECTOR signal are enabled with device selection. The INDEX signal and SECTOR signals shall not be considered valid until at least 500 nanoseconds after the active-going edge of the SELECT OUT/ATTENTION IN STROBE signal that caused the selection of the device.

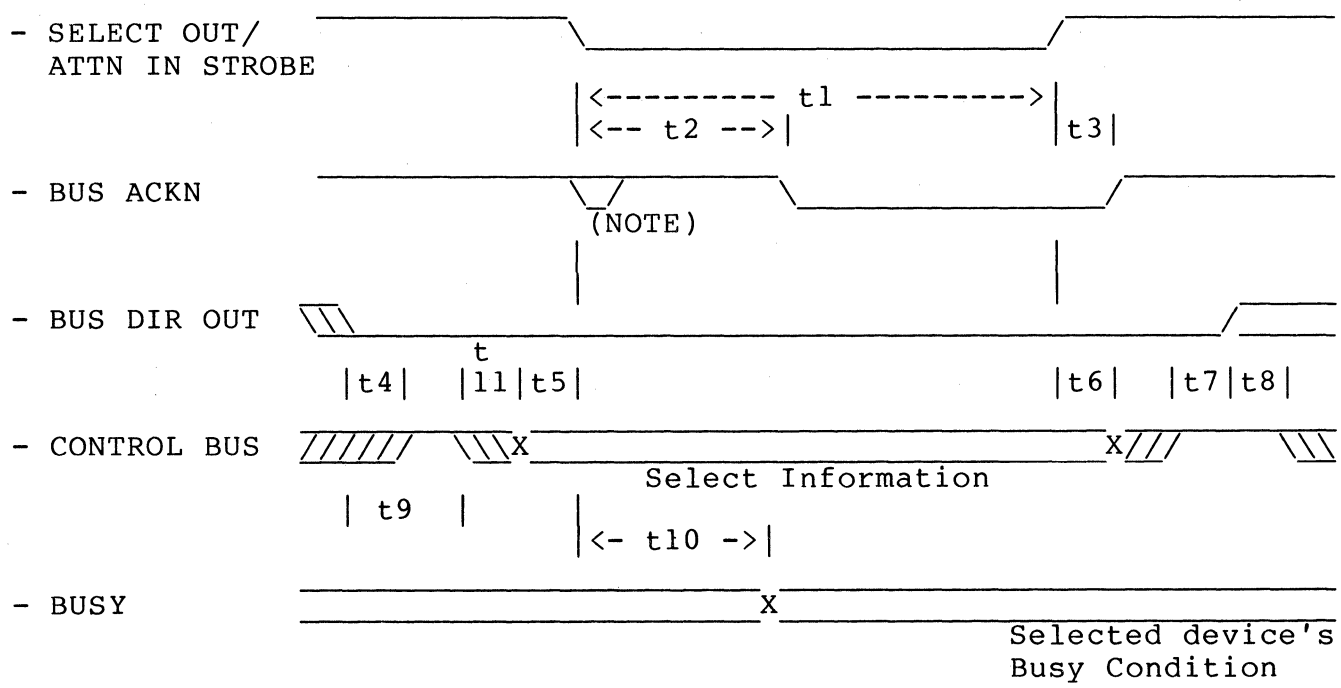
6.3 REFERENCE CLOCK Timing. The REFERENCE CLOCK timing is defined in Figure 28.

6.4 READ Timing. The READ timing is defined in Figure 29.

6.5 WRITE Timing. The WRITE timing is defined in Figure 30. The WRITE CLOCK shall be generated in the host from the REFERENCE CLOCK. The delay time from the REFERENCE CLOCK to WRITE CLOCK is a function of cable length and circuit delays. The phase difference between the two signals shall be constant during the complete write operation. The WRITE DATA signal and the WRITE

CLOCK signal shall be synchronized as defined in Figure 30. The READ DATA signal is undefined during a write operation.

6.6 ADDRESS MARK Timing (optional). The READ ADDRESS MARK timing is defined in Figure 31. The WRITE ADDRESS MARK timing is defined in Figure 32.

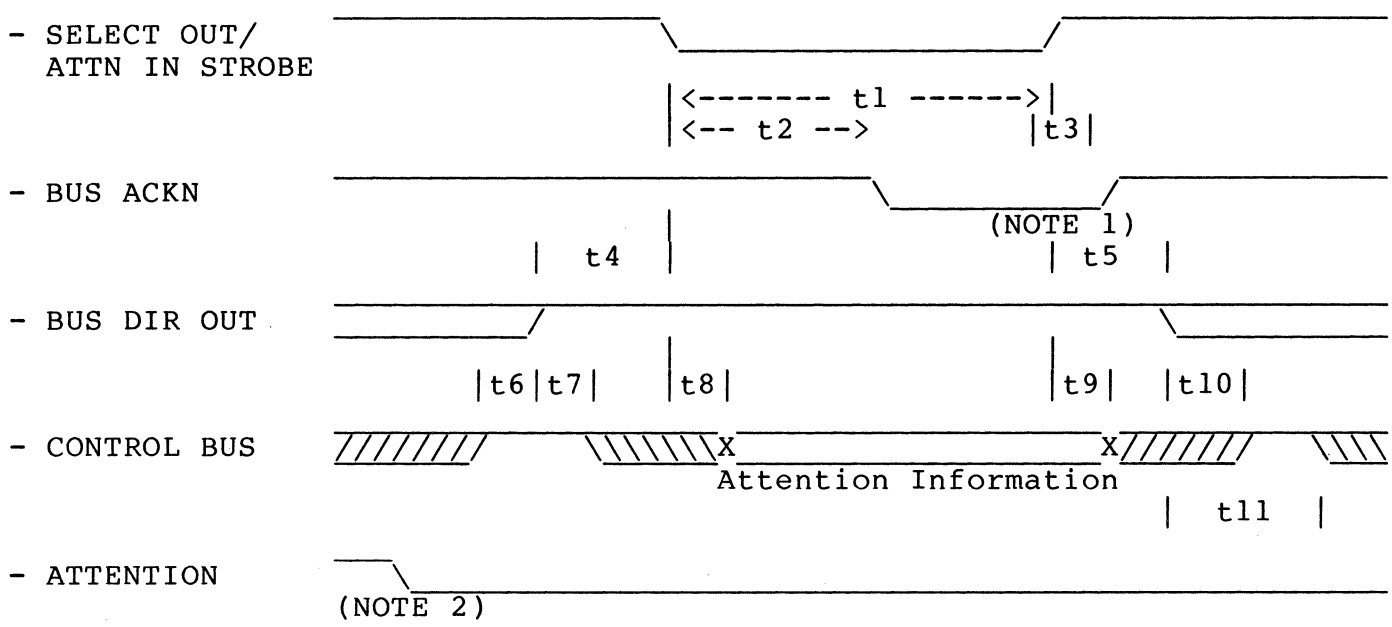


Label	Description	Min.	Max.	Units
t1	SELECT/ATTENTION STROBE width	500	---	Nanoseconds
t2	BUS ACKNOWLEDGE invalid	0	300	Nanoseconds
t3	BUS ACKNOWLEDGE hold time	0	100	Nanoseconds
t4	Device - CONTROL BUS release time	0	100	Nanoseconds
t5	CONTROL BUS - Data setup time	100	---	Nanoseconds
t6	CONTROL BUS - Data hold time	0	---	Nanoseconds
t7	Host - CONTROL BUS release time	100	---	Nanoseconds
t8	Device - CONTROL BUS access time	0	---	Nanoseconds
t9	Host - CONTROL BUS access time	100	---	Nanoseconds
t10	BUSY invalid	0	300	Nanoseconds
t11	Device-to-Host transition	0	---	Nanoseconds

NOTE: Glitch possible due to previously selected device. To avoid glitch, deselect all devices and then select.

Figure 23

SELECTION Timing



Label	Description	Min	Max	Units
t1	SELECT/ATTENTION STROBE width	500	---	Nanoseconds
t2	BUS ACKNOWLEDGE invalid (NOTE 1)	0	300	Nanoseconds
t3	BUS ACKNOWLEDGE hold time	0	100	Nanoseconds
t4	BUS DIRECTION OUT - Setup time	100	---	Nanoseconds
t5	BUS DIRECTION OUT - Hold time	0	---	Nanoseconds
t6	Host - CONTROL BUS release time	100	---	Nanoseconds
t7	Device - CONTROL BUS access time	0	---	Nanoseconds
t8	ATTENTION information invalid	0	100	Nanoseconds
t9	ATTENTION information hold time	0	---	Nanoseconds
t10	Device - CONTROL BUS release time	0	100	Nanoseconds
t11	Host - CONTROL BUS access time	100	---	Nanoseconds

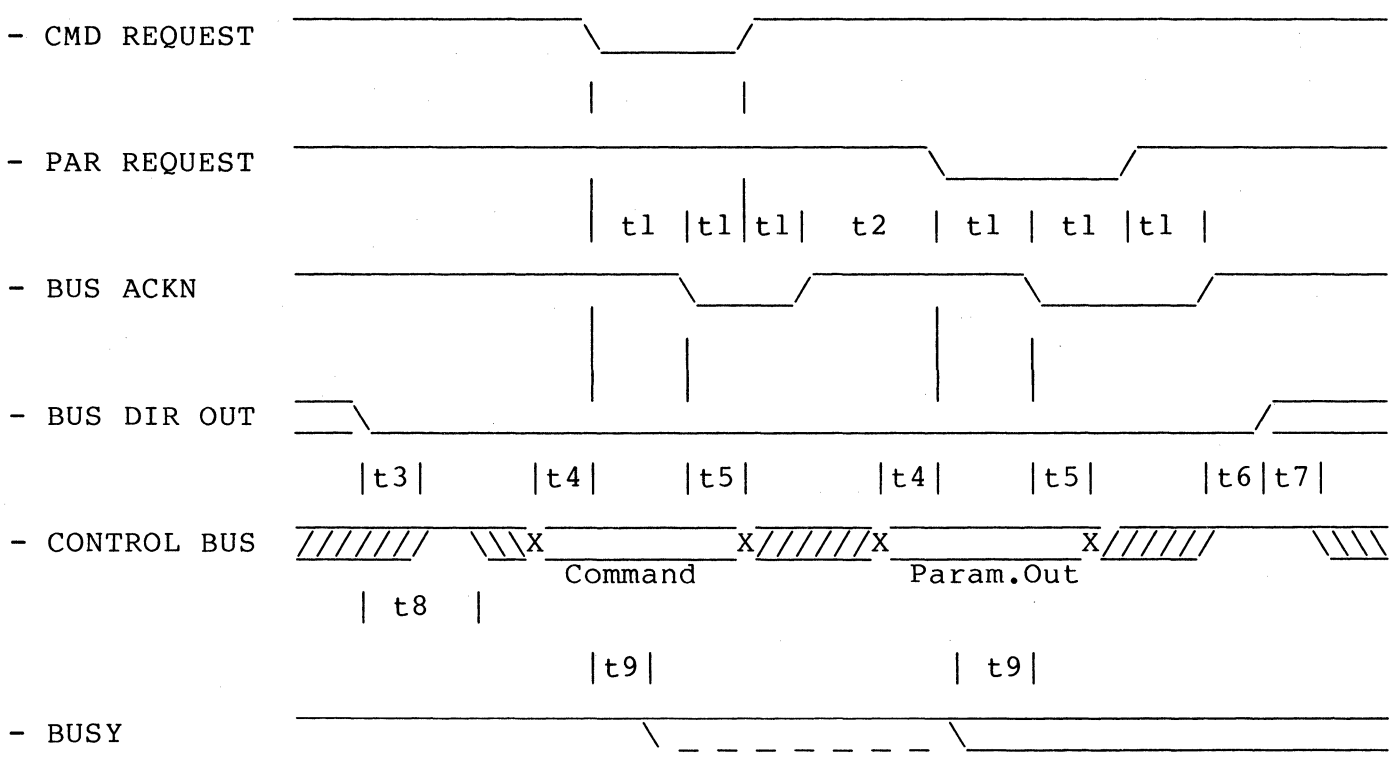
NOTES:

(1) Active only if there is a previously selected device, inactive if all devices are deselected.

(2) Some devices may have ATTENTION active causing the host to perform the ATTENTION timing sequence.

Figure 24

ATTENTION Timing

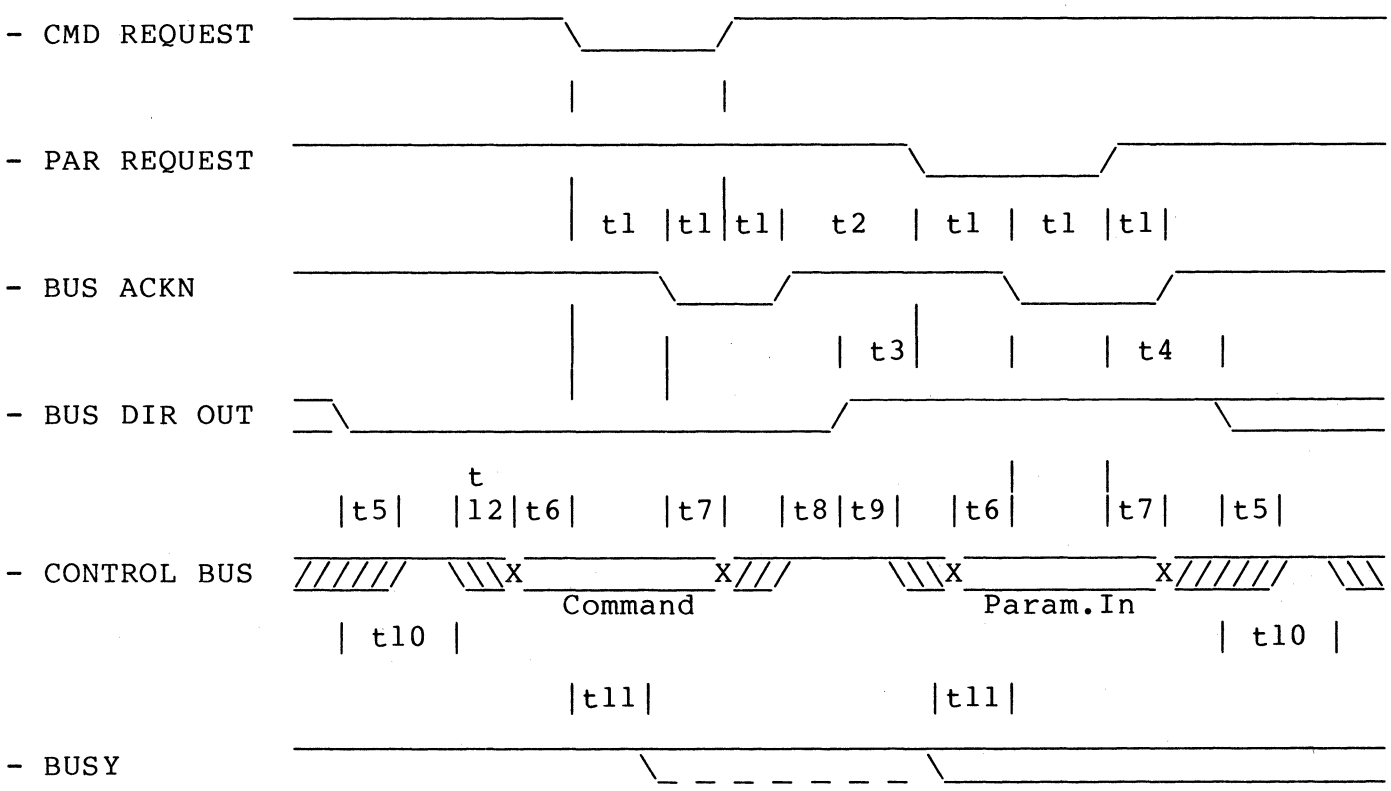


Label	Description	Min	Max	Units
t1	Handshake response time	0	10*	Milliseconds
t2	Spacing	0	10*	Milliseconds
t3	Device - CONTROL BUS release time	0	100	Nanoseconds
t4	CONTROL BUS - Data setup time	100	---	Nanoseconds
t5	CONTROL BUS - Data hold time	0	---	Nanoseconds
t6	Host - CONTROL BUS release time	100	---	Nanoseconds
t7	Device - CONTROL BUS access time	0	---	Nanoseconds
t8	Host - CONTROL BUS access time	100	---	Nanoseconds
t9	BUSY setup time	0*	---	Nanoseconds

* This value is valid only if the BUSY signal is not active at beginning of sequence.

Figure 25

Command/Parameter Out Sequence

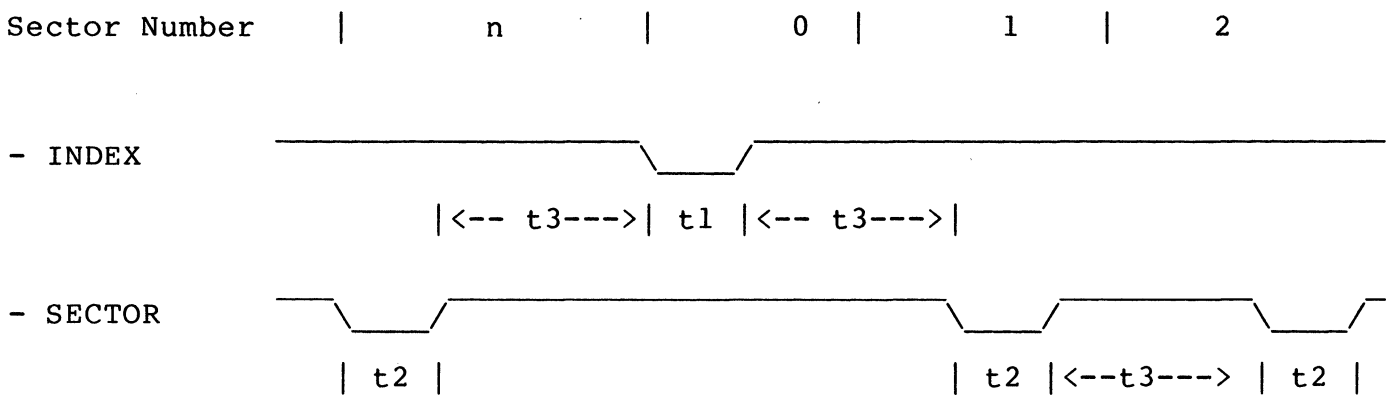


Label	Description	Min	Max	Units
t1	Handshake response time	0	10*	Milliseconds
t2	Spacing	0	10*	Milliseconds
t3	BUS DIRECTION OUT - Setup time	100	---	Nanoseconds
t4	BUS DIRECTION OUT - Hold time	0	---	Nanoseconds
t5	Device - CONTROL BUS release time	0	100	Nanoseconds
t6	CONTROL BUS - Data setup time	100	---	Nanoseconds
t7	CONTROL BUS - Data hold time	0	---	Nanoseconds
t8	Host - CONTROL BUS release time	100	---	Nanoseconds
t9	Device - CONTROL BUS access time	0	---	Nanoseconds
t10	Host - CONTROL BUS access time	100	---	Nanoseconds
t11	BUSY setup time	0*	---	Nanoseconds
t12	Device-to-Host transition	0	---	Nanoseconds

* This value is valid only if the BUSY signal is not active at beginning of sequence.

Figure 26

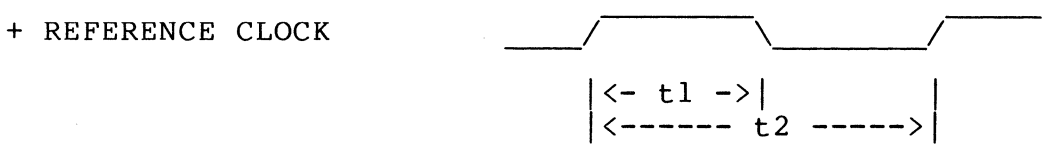
Command/Parameter In Sequence



Label	Description	Min	Max	Units
t1	INDEX pulse width	0.5	---	Microseconds
t2	SECTOR pulse width	0.5	---	Microseconds
t3	Interpulse spacing	0.5	---	Microseconds

Figure 27

INDEX/SECTOR Timing (Hard Sectoring)

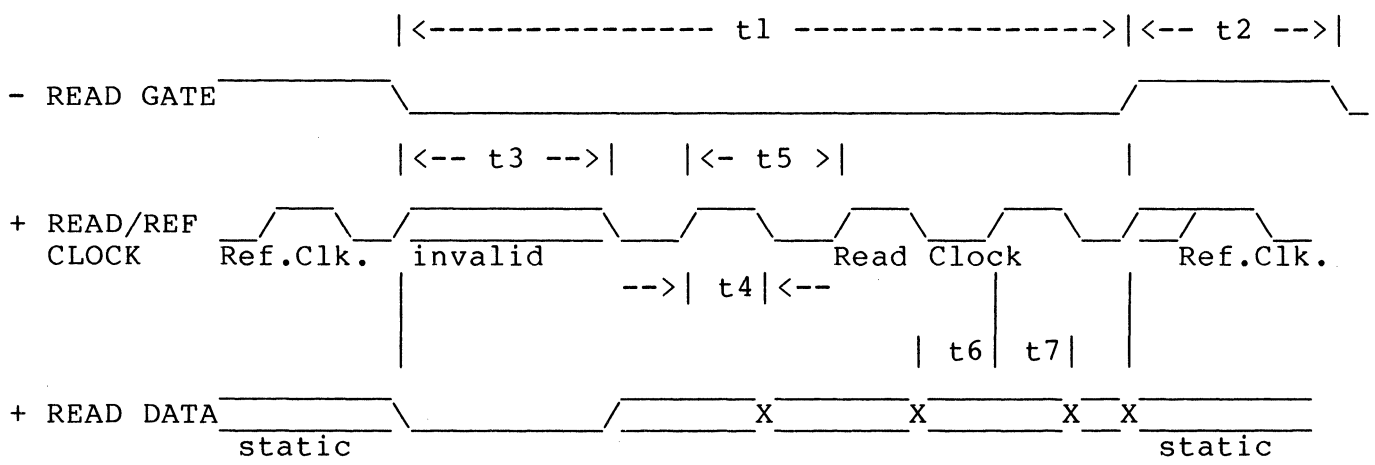


Label	Description	Min	Max
t1	REFERENCE CLOCK active time	0.4*tp	0.6*tp
t2	REFERENCE CLOCK period	0.95*tp	1.05*tp

* = Multiply; tp = Nominal REFERENCE CLOCK period.

Figure 28

REFERENCE CLOCK Timing

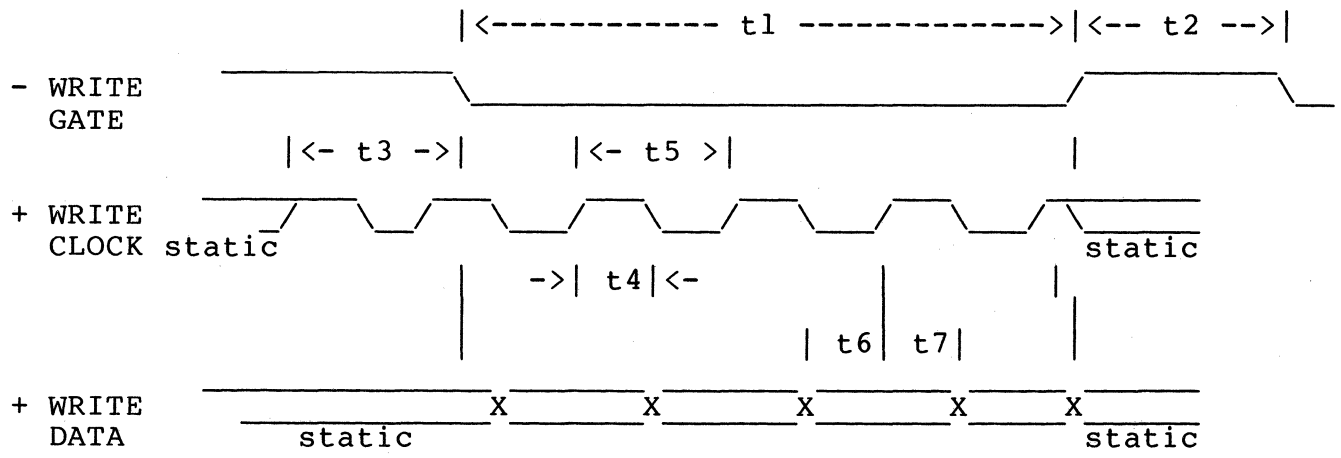


Label	Description	Min	Max
t1	READ GATE active	0	---
t2	READ GATE inactive	2*tp	---
t3	READ GATE to valid READ DATA and READ CLOCK	See vendor specifications	
t4	READ CLOCK active time	0.4*tp	0.6*tp
t5	READ CLOCK period	0.95*tp	1.05*tp
t6	READ DATA setup time	0.25*tp	---
t7	READ DATA hold time	0.25*tp	---

* = Multiply; tp = Nominal REFERENCE CLOCK period.

Figure 29

READ Timing

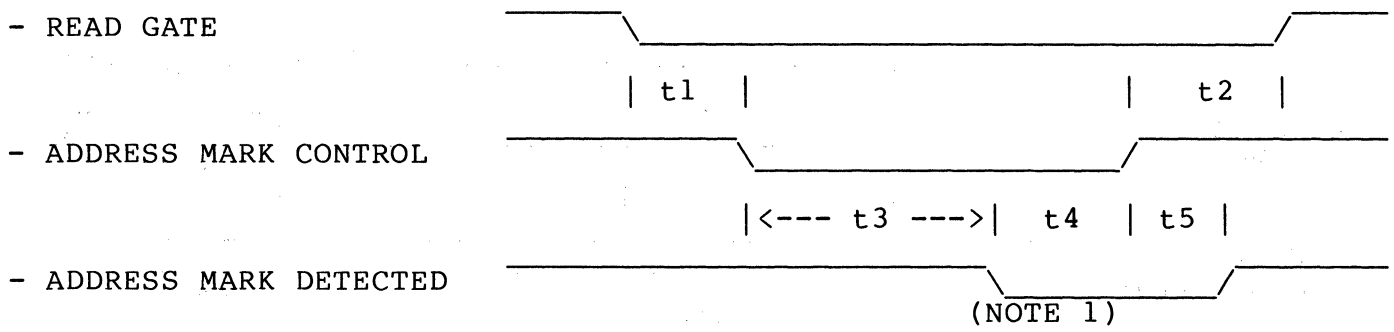


Label	Description	Min	Typ	Max
t1	WRITE GATE active	0	---	---
t2	WRITE GATE inactive	0	---	---
t3	WRITE CLOCK valid	tp	---	16*tp
t4	WRITE CLOCK active time	0.4*tp	---	0.6*tp
t5	WRITE CLOCK period	---	tp	---
t6	WRITE DATA setup time	0.25*tp	---	---
t7	WRITE DATA hold time	0.25*tp	---	---

* = Multiply; tp = Nominal REFERENCE CLOCK period.

Figure 30

WRITE Timing



Label	Description	Min	Max	Units
t1	READ GATE setup time	0	---	Nanoseconds
t2	READ GATE hold time	0	---	Nanoseconds
t3	ADDRESS MARK Control setup time	24*tp	---	---
t4	ADDRESS MARK CONTROL hold time	0	---	Nanoseconds
t5	ADDRESS MARK DETECTED hold time (NOTE2)	0	100	Nanoseconds

* = Multiply; tp = Nominal REFERENCE CLOCK period.

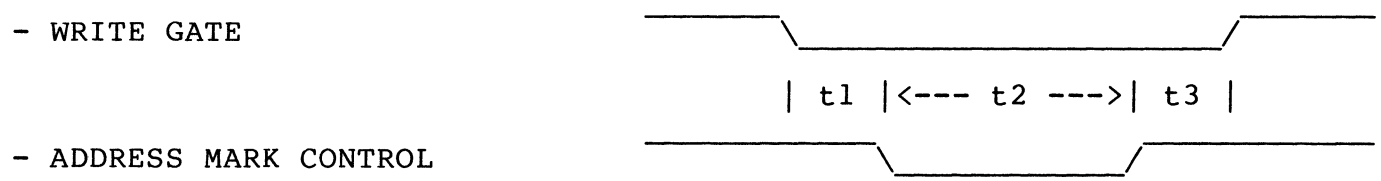
NOTES:

(1) This hold time applies to the earliest loss of READ GATE or ADDRESS MARK CONTROL.

(2) This edge implies the trailing edge of the address mark has been passed.

Figure 31

READ ADDRESS MARK Timing



Label	Description	Min	Max	Units
t1	WRITE GATE setup time	0	---	Nanoseconds
t2	ADDRESS MARK CONTROL width	24*tp	---	---
t3	WRITE GATE hold time	0	---	Nanoseconds

* = Multiply; tp = Nominal REFERENCE CLOCK period.

Figure 32

WRITE ADDRESS MARK Timing

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American National Standards for Information Processing Systems

X3.1-1976 Synchronous Signaling Rates for Data Transmission
X3.2-1970 (R1976) Print Specifications for Magnetic Ink Character Recognition
X3.3-1970 (R1976) Bank Check Specifications for Magnetic Ink Character Recognition
X3.4-1977 Code for Information Interchange
X3.5-1970 Flowchart Symbols and Their Usage
X3.6-1965 (R1973) Perforated Tape Code
X3.9-1978 Programming Language FORTRAN
X3.11-1969 General Purpose Paper Cards
X3.14-1983 Recorded Magnetic Tape (200 CPI, NRZI)
X3.15-1976 Bit Sequencing of the American National Standard Code for Information Interchange in Serial-by-Bit Data Transmission
X3.16-1976 Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the American National Standard Code for Information Interchange
X3.17-1981 Character Set for Optical Character Recognition (OCR-A)
X3.18-1974 One-Inch Perforated Paper Tape
X3.19-1974 Eleven-Sixteenths-Inch Perforated Paper Tape
X3.20-1967 (R1974) Take-Up Reels for One-Inch Perforated Tape
X3.21-1967 Rectangular Holes in Twelve-Row Punched Cards
X3.22-1983 Recorded Magnetic Tape (800 CPI, NRZI)
X3.23-1974 Programming Language COBOL
X3.24-1968 Signal Quality at Interface between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission
X3.25-1976 Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in the American National Standard Code for Information Interchange
X3.26-1980 Hollerith Punched Card Code
X3.27-1978 Magnetic Tape Labels and File Structure
X3.28-1976 Procedures for the Use of the Communication Control Characters of American National Standard Code for Information Interchange in Specified Data Communication Links
X3.29-1971 Specifications for Properties of Unpunched Oiled Paper Perforator Tape
X3.30-1971 Representation for Calendar Date and Ordinal Date
X3.31-1973 Structure for the Identification of the Counties of the United States
X3.32-1973 Graphic Representation of the Control Characters of American National Standard Code for Information Interchange
X3.34-1972 Interchange Rolls of Perforated Tape
X3.36-1975 Synchronous High-Speed Data Signaling Rates between Data Terminal Equipment and Data Communication Equipment
X3.37-1980 Programming Language APT
X3.38-1972 (R1977) Identification of States of the United States (Including the District of Columbia)
X3.39-1973 Recorded Magnetic Tape (1600 CPI, PE)
X3.40-1983 Unrecorded Magnetic Tape (9-Track 800 CPI, NRZI; 1600 CPI, PE; and 6250 CPI, GCR)
X3.41-1974 Code Extension Techniques for Use with the 7-Bit Coded Character Set of American National Standard Code for Information Interchange
X3.42-1975 Representation of Numeric Values in Character Strings
X3.43-1977 Representations of Local Time of the Day
X3.44-1974 Determination of the Performance of Data Communication Systems
X3.45-1982 Character Set for Handprinting
X3.46-1974 Unrecorded Magnetic Six-Disk Pack (General, Physical, and Magnetic Characteristics)
X3.47-1977 Structure for the Identification of Named Populated Places and Related Entities of the States of the United States for Information Interchange
X3.48-1977 Magnetic Tape Cassettes (3.810-mm [0.150-Inch] Tape at 32 bpmm [800 bpi], PE)
X3.49-1975 Character Set for Optical Character Recognition (OCR-B)
X3.50-1976 Representations for U.S. Customary, SI, and Other Units to Be Used in Systems with Limited Character Sets
X3.51-1975 Representations of Universal Time, Local Time Differentials, and United States Time Zone References
X3.52-1976 Unrecorded Single-Disk Cartridge (Front Loading, 2200 BPI) (General, Physical, and Magnetic Requirements)
X3.53-1976 Programming Language PL/I
X3.54-1976 Recorded Magnetic Tape (6250 CPI, Group Coded Recording)
X3.55-1982 Unrecorded Magnetic Tape Cartridge, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase encoded
X3.56-1977 Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase Encoded
X3.57-1977 Structure for Formatting Message Headings Using the American National Standard Code for Information Interchange for Data Communication Systems Control
X3.58-1977 Unrecorded Eleven-Disk Pack (General, Physical, and Magnetic Requirements)
X3.59-1981 Magnetic Tape Cassettes, Dual Track Complementary Return-to-Bias (CRB) Four-States Recording on 3.81-mm (0.150-Inch) Tape
X3.60-1978 Programming Language Minimal BASIC
X3.61-1978 Representation of Geographic Point Locations
X3.62-1979 Paper Used in Optical Character Recognition (OCR) Systems
X3.63-1981 Unrecorded Twelve-Disk Pack (100 Megabytes) (General, Physical, and Magnetic Requirements)
X3.64-1979 Additional Controls for Use with American National Standard Code for Information Interchange
X3.66-1979 Advanced Data Communication Control Procedures (ADCCP)
X3.72-1981 Parallel Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase Encoded
X3.73-1980 Single-Sided Unformatted Flexible Disk Cartridge (for 6631-BPR Use)
X3.74-1981 Programming Language PL/I, General-Purpose Subset
X3.76-1981 Unformatted Single-Disk Cartridge (Top Loading, 200 tpi 4400 bpi) (General, Physical, and Magnetic Requirements)
X3.77-1980 Representation of Pocket Select Characters
X3.79-1981 Determination of Performance of Data Communications Systems That Use Bit-Oriented Communication Procedures
X3.80-1981 Interfaces between Flexible Disk Cartridge Drives and Their Host Controllers
X3.82-1980 One-Sided Single-Density Unformatted 5.25-Inch Flexible Disk Cartridge (for 3979-BPR Use)
X3.83-1980 ANSI Sponsorship Procedures for ISO Registration According to ISO 2375
X3.84-1981 Unformatted Twelve-Disk Pack (200 Megabytes)(General, Physical, and Magnetic Requirements)
X3.85-1981 1/2-Inch Magnetic Tape Interchange Using a Self-Loading Cartridge
X3.86-1980 Optical Character Recognition (OCR) Inks
X3.88-1981 Computer Program Abstracts
X3.89-1981 Unrecorded Single-Disk, Double-Density Cartridge (Front Loading, 2200 bpi, 200 tpi) (General, Physical, and Magnetic Requirements)
X3.91M-1982 Storage Module Interfaces
X3.92-1981 Data Encryption Algorithm
X3.93M-1981 OCR Character Positioning
X3.95-1982 Microprocessors — Hexadecimal Input/Output, Using 5-Bit and 7-Bit Teleprinters
X3.96-1983 Continuous Business Forms (Single-Part)
X3.98-1983 Text Information Interchange in Page Image Format (PIF)
X3.99-1983 Print Quality Guideline for Optical Character Recognition (OCR)
X3.100-1983 Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment for Packet Mode Operation with Packet Switched Data Communications Network
X3.101-1983 Interfaces Between Rigid Disk Drive(s) and Host(s)
X3.102-1983 Data Communication Systems and Services — User-Oriented Performance Parameters
X3.103-1983 Unrecorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in)
X3.104-1983 Recorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in), Phase Encoded
X3.105-1983 Data Link Encryption
X3.106-1983 Modes of Operation for the Data Encryption Algorithm
X3.110-1983 Videotex/Teletext Presentation Level Protocol Syntax
X3.114-1984 Alphanumeric Machines; Coded Character Sets for Keyboard Arrangements in ANSI X4.23-1984 and X4.22-1983
X11.1-1977 Programming Language MUMPS
IEEE 416-1978 Abbreviated Test Language for All Systems (ATLAS)
IEEE 716-1982 Standard C/ATLAS Language
IEEE 717-1982 Standard C/ATLAS Syntax
IEEE 770X3.97-1983 Programming Language PASCAL
IEEE 771-1980 Guide to the Use of ATLAS

MIL-STD-1815A-1983 Reference Manual for the Ada Programming Language

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