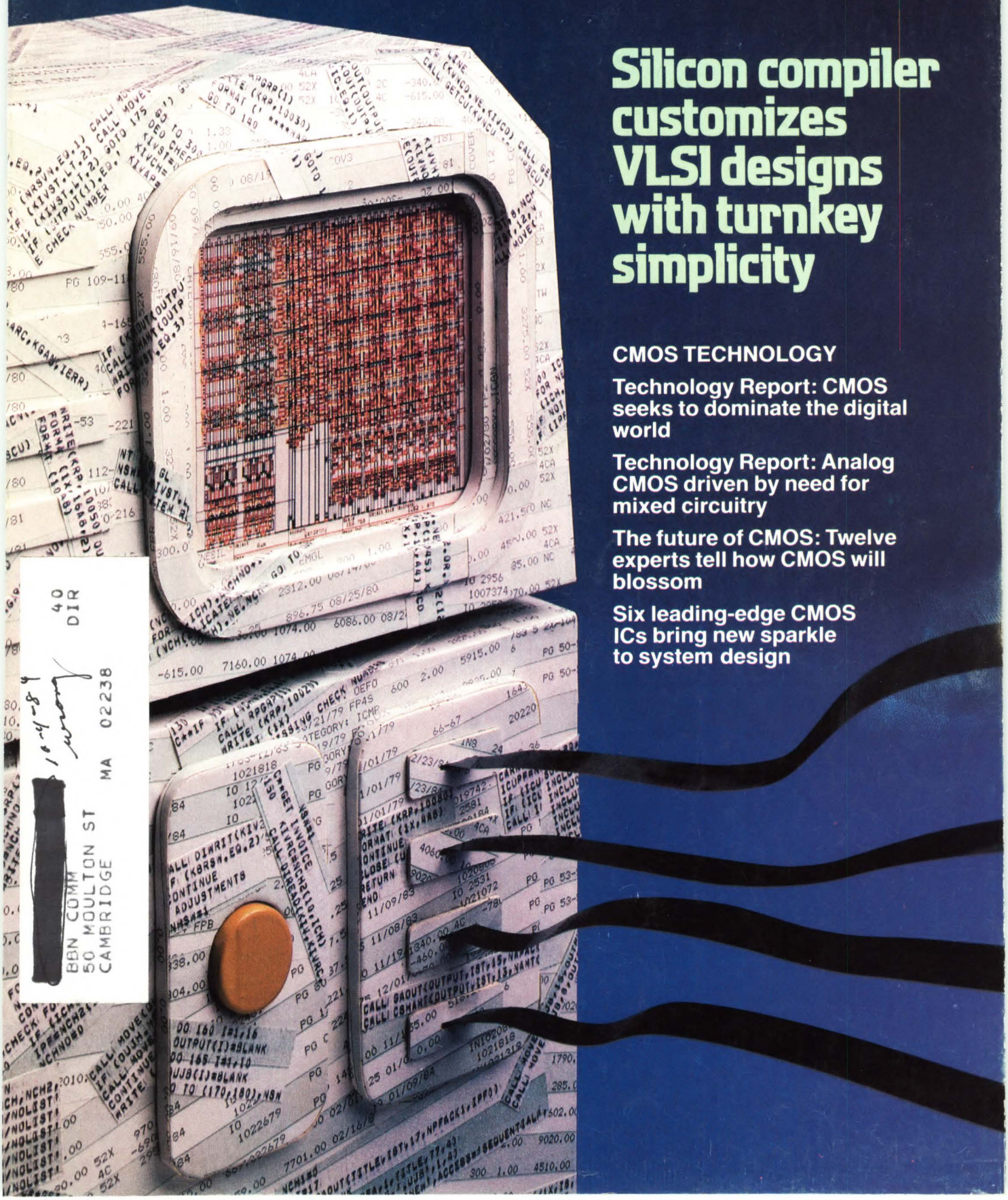
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OCTOBER 4, 1984



Silicon compiler customizes VLSI designs with turnkey simplicity

CMOS TECHNOLOGY

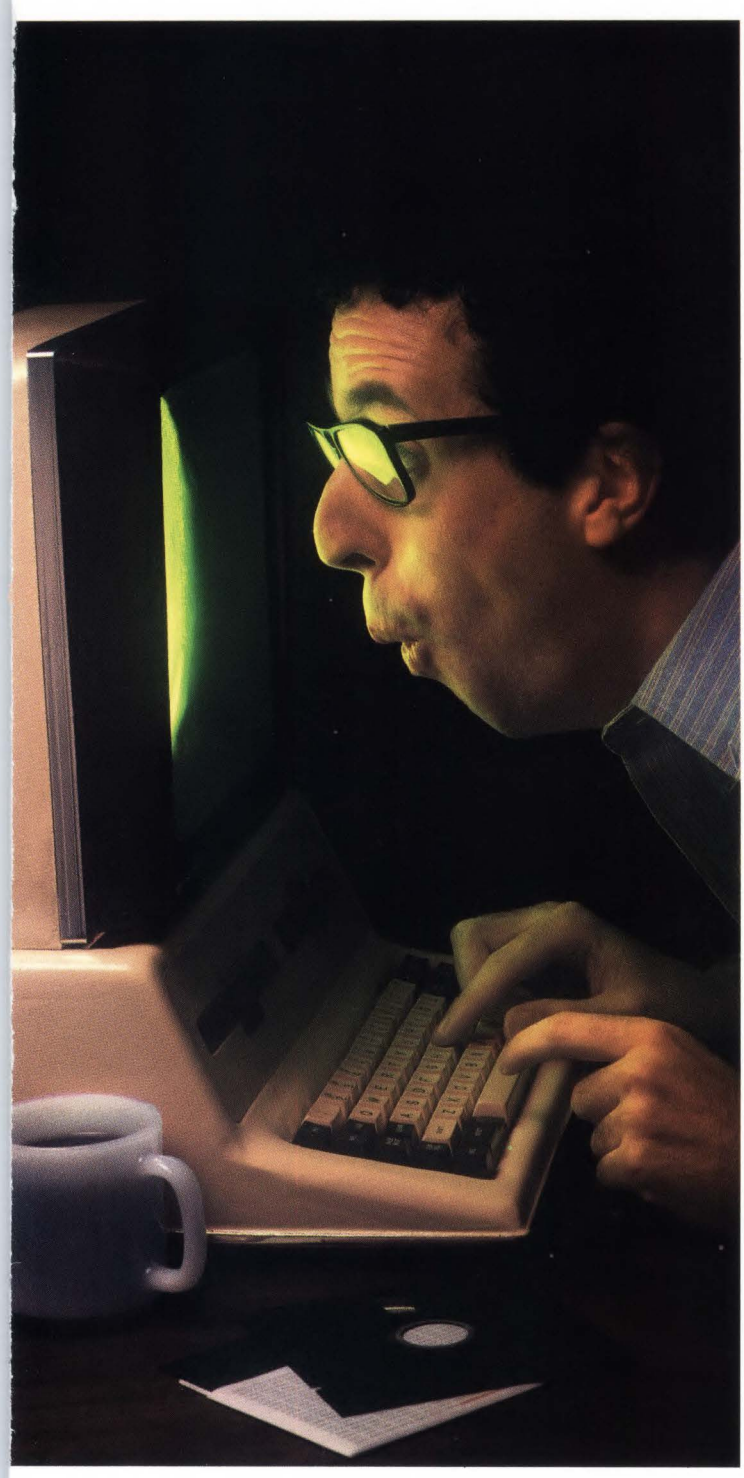
Technology Report: CMOS seeks to dominate the digital world

Technology Report: Analog CMOS driven by need for mixed circuitry

The future of CMOS: Twelve experts tell how CMOS will blossom

Six leading-edge CMOS ICs bring new sparkle to system design

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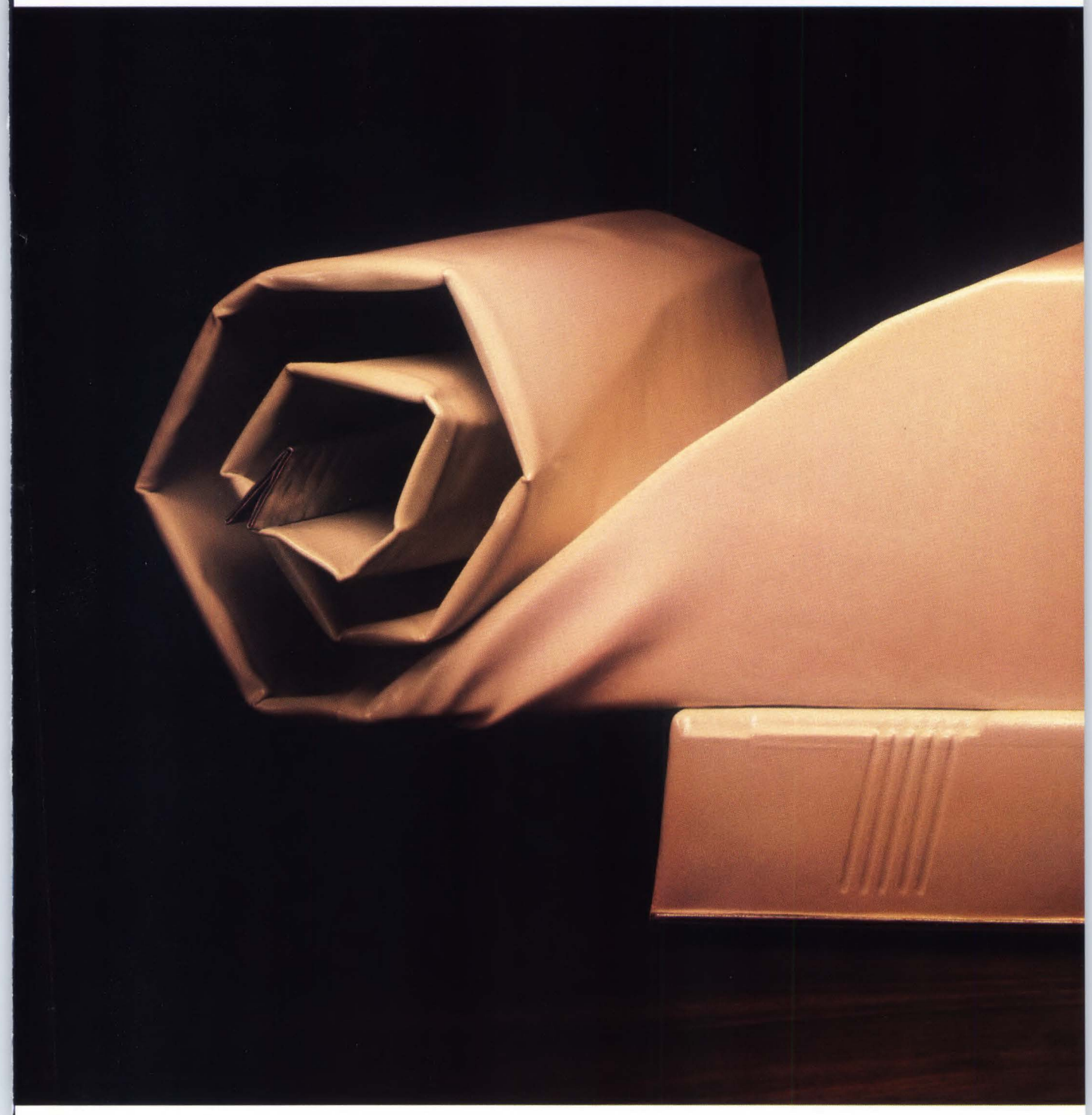
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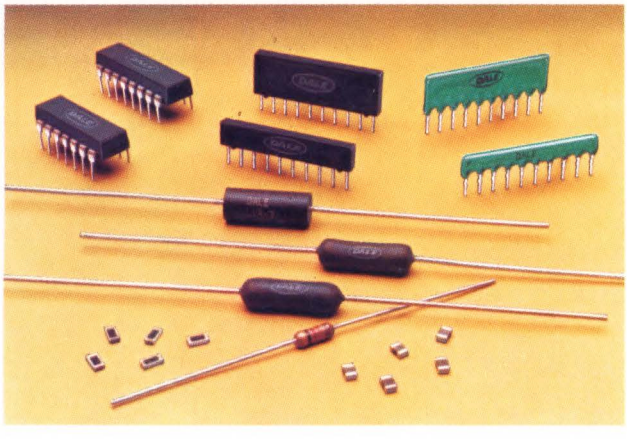
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CIRCLE 3

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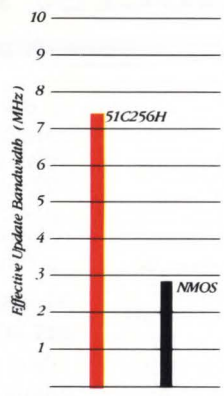
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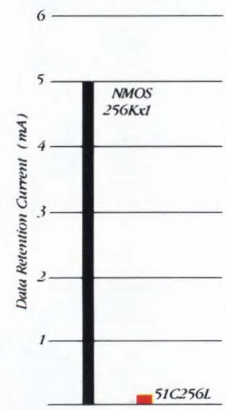
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BEHIND THE COVER

Put it in writing" could be Stephen Johnson's battle cry. For that was exactly what he did on becoming Silicon Compilers' new vice president of engineering a year ago. With the position came the assignment to produce the company's—and the world's—first commercial turnkey silicon compilation system.

The massive software project meant distilling the company's two years of success in producing fully laid-out VLSI chips from only their architectural descriptions. And that entailed being "as systematic about developing the software as the system is about designing chips," says Johnson.

So, before letting designers write a single line of code, he and others first produced a corporate specification that set rigid and detailed programming standards for structuring the software. And since the software was written in C, a language that, as Johnson puts it, "lets you hang yourself," the standards went so far as to outlaw certain constructs.

Enter vice president Dave Johannson, silicon-compiler veteran and protégé of VLSI pioneer Carver Mead (Johannson and Mead were two of the company's three founders). He and Johnson next condensed all the ideas and concepts of the company's past two years into a 455-page functional system specification. It even included a chapter-and-verse description of how the system would look to the user. This specification, Johnson points out, "had a tremendous leveling effect" on the design team, bringing everyone's ideas into harmony. That, however, was only the beginning.

There followed a marathon effort to come up with a top-down design of the actual system. In a few weeks, a 3000-page document was produced, describing every software routine, its role, and its interfaces. About 2600 separate functions, in all, had to be coded into routines. Next came the equally meticulous and exhaustive scheduling sessions and the bottom line on development time: one year.

Is this any way to develop software? Johnson thinks so. And he's not alone: the company met its schedule to within a week. Exactly what it produced is the subject of this issue's three-part cover story (p. 167) written by Stan Mazor and, of course, Stephen Johnson.

ElectronicDesign
October 4, 1984 • Vol. 32 No. 20

DEPARTMENTS

3 Behind the Cover
6 Contents Spotlight
11 On Reflection
15 Reader Feedback
23 U.S. Meetings
27 Personally Speaking
95 International Meetings
345 Index of Advertisers
346 Reader Service Card

CMOS TECHNOLOGY

102 Introduction

Technology Report

104 Before reaching its potential, CMOS faces some thorny problems
How well CMOS can strengthen its foothold depends on solutions to latch-up, device isolation, and limited interconnections.

121 Analog CMOS marches on, but it steps to the beat of a different drummer
First because it makes excellent switches and input devices, then because it allows the easy addition of digital functions, and always because it dissipates little power, CMOS takes over the analog world.

135 A dozen experts see CMOS in your future

Design Entries

185 Advanced clock controller cuts power needs, size of static CMOS systems
With a one-chip controller-generator running a static CMOS system in three minimal-frequency modes, power consumption plummets.

195 Charge-nulled CMOS switch lets op amps tackle precision analog tasks
A dual DPDT switch aimed at switched-capacitor designs ushers in new instrumentation amps, analog multipliers, and v-f converters.

209 Image signal processor computes fast enough for gray-scale video
Handling millions of computations per video frame, a pipelined chip attains system speeds 1000 times those of 16-bit processors.

217 Multiplier-accumulator derives high performance from 1-μm CMOS
With a 1-μm effective channel length, a chip fits in a pin-grid array with enough pins for nonmultiplexed outputs—an asset for many digital signal-processing tasks.

TECHNOLOGY NEWS

31 Newspulse

Newsfront

41 32-bit chip set follows 250 instructions, uses static NMOS circuits

44 Computer's voting architecture protects industrial process control

46 Parallel-processing mainframe welcomes Unix to a new home

48 Serial bus carries multiple-channel or fast data

Conference Preview

55 GaAs, superconducting, optical ICs spearhead government conference

67 Ever more complex, VLSI chips spur testing from within and without

75 ICCD will heat up with gallium arsenide, AI, and supercomputers

Viewpoint

81 Digital scopes will emerge as the standard tools for hardware designers

82 Testing and servicing suffer at the hands of throwaway design methods

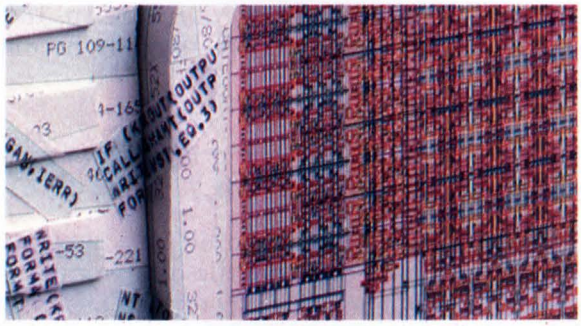
92 International Newsfront

229 With built-in specialties, CMOS microcontrollers take aim at diverse tasks
Designers need not add extra devices to their systems. A microcontroller family may well incorporate most of the necessary circuits.

245 Dense static RAM speeds data access in memory-intensive systems
Because slow RAM will not do in graphics and other fast signal-processing jobs, dense static devices are making a bid to replace sluggish dynamic parts.

DESIGN ENTRIES

167 Cover: Silicon compiler lets system makers design their own VLSI chips
Despite powerful tools, designing custom VLSI circuits is slow and inefficient. A turnkey silicon compiler now streamlines the job, making the task a comparative snap.



259 Multiple display schemes make their mark on smart graphics stations
With attention paid to command structures and windowing, a series of workstations affords speed, high-level drawings, and interactivity.

275 Design Solutions

NEW PRODUCTS

Analog

291 Monolithic 12-bit ADCs need only 5 V and convert in 100 μs

294 Op amp chips remain stable at a 40-MHz unity-gain bandwidth

296 Sense-and-hold hybrid captures pulse peaks as narrow as 100 ns

Computer Systems

298 Compact Lisp machine fits under a desk; develops and runs AI programs

Instruments

302 Frequency standard holds drift to 10^{-11}/day, can use 2 external references

Power

306 Switching power supplies occupy 6 in.^{3} yet deliver 7.5 W

315 Components
318 Packaging & Production
325 Communications
327 Product News
330 Application Notes
331 New Literature

IN THE NEXT ISSUE

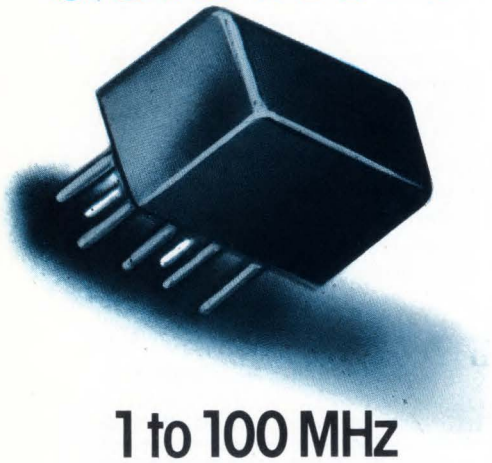
Instruments Technology: an in-depth examination of emulators . . . An advanced view of what's coming at Wescon plus a look at products to be introduced at the conference . . . Progress in oscilloscopes, logic testing, checking out mass-storage devices.

Cover photograph by Steve Eisenberg

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CIRCLE 5

CONTENTS SPOTLIGHT

CMOS Technology 102

The impact that CMOS has had on all areas of electronics defies quantification. Besides the well-known advantage of low power consumption, it opens doors to higher density and performance. Digital CMOS circuitry, the subject of our first Technology Report (p. 104), typifies some of the stubborn problems encountered with the technology—latch-up, inadequate device isolation, limited interconnections. The analog world, too, is shifting toward CMOS, pushed by the frequent mixing of digital and analog circuitry on one chip. Naturally, analog circuits cannot sacrifice quality or speed, forcing designers to consider extremely different factors, as our second Technology Report explores (p. 121).

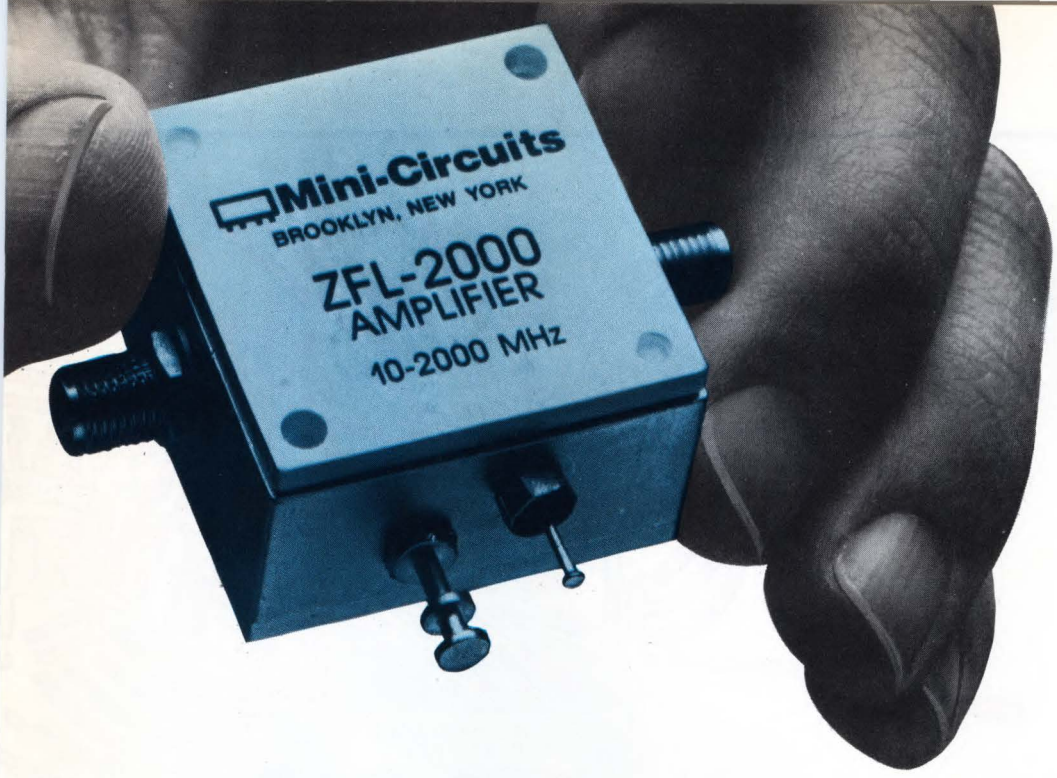
Following the reports, a dozen industry leaders present their views on CMOS and predict its future (p. 135). Not surprisingly, all agree that CMOS is quickly becoming the technology of the 1980s.

Cover: Silicon compiler 167

Just as software language compilers relieve programmers of the minute details of a computer's native instructions, the silicon compiler promises not only to lift a pile of details from IC designers' shoulders but also to turn system designers into VLSI chip makers. A powerful silicon compiler is the first development tool that lets designers translate a VLSI block diagram into a chip and then test the design before committing it to silicon. Our coverage of the silicon compiler, presented here in three parts, explores the general principles behind it, the specifics of the actual system, and a detailed application.

Preview: International Test Conference 67

At today's extremely high level of integration, device testing becomes a critical matter. The International Test Conference, to be held later this month in Philadelphia, tackles testability in general, through self-testing facilities or through sophisticated testers. Even expert systems are making an entrance, diagnosing the problems of the testers.



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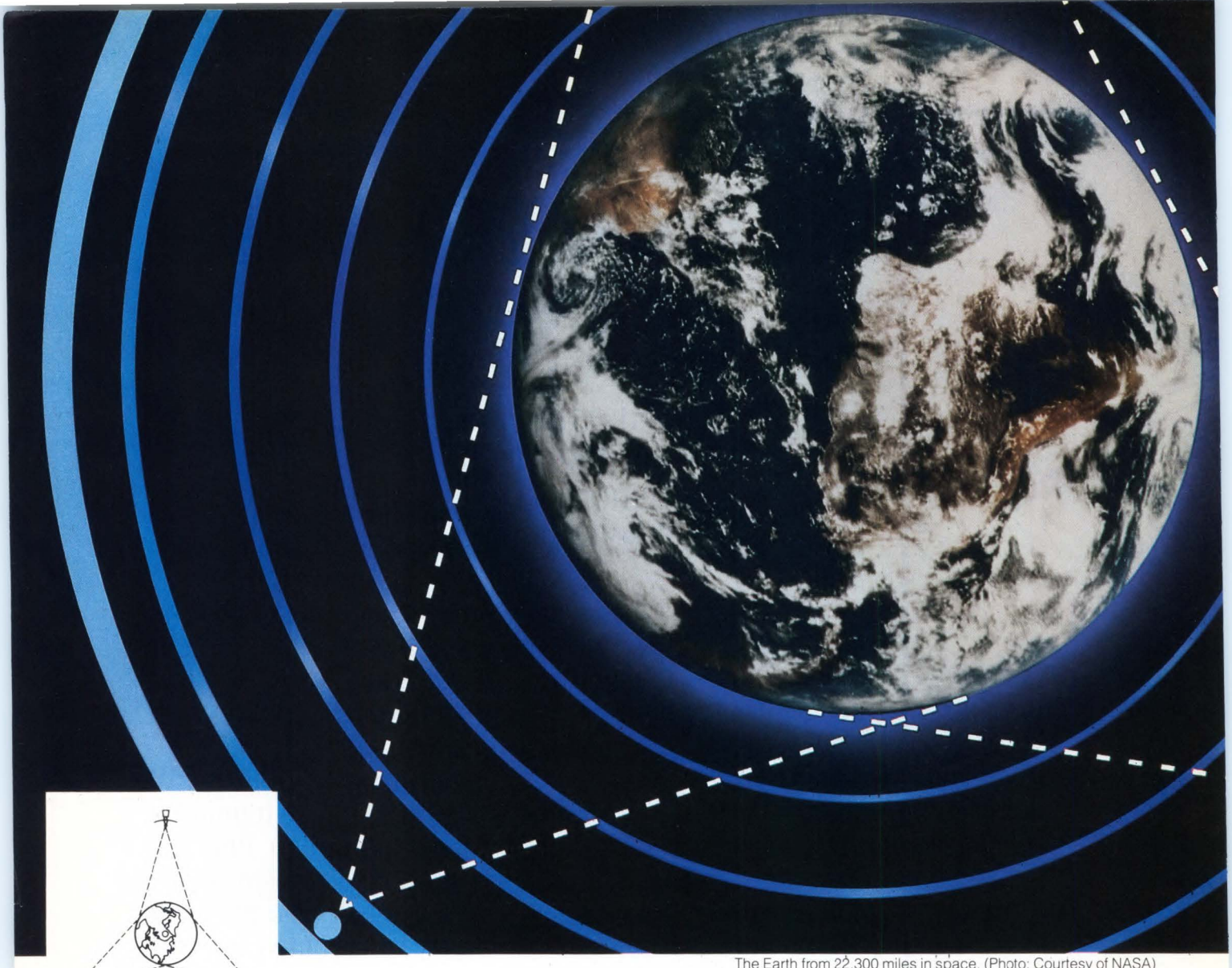
National offers a fully integrated CAD system. With comprehensive training and logic simulation. Plus fault grading for design checking and testing. And 100% auto-place and route capabilities.

So next time the talk turns to CMOS gate arrays, remember National. We're not just talking about it. We're doing it.

For a copy of our micro-CMOS brochure, contact us at 2900 Semiconductor Drive, MS 23200, Santa Clara, California 95051.

National Semiconductor
We're doing it.

CIRCLE 140



The Earth from 22,300 miles in space. (Photo: Courtesy of NASA)

Clarke's proposed
3-satellite system.

FINDING NEW WAYS...

In 1945, Arthur C. Clarke—a British mathematician, wireless operator and creative science fiction writer found a better way to beam communications signals around the world. He theorized that an artificial satellite, carried by a rocket to an orbit 22,300 miles above the earth's equator and traveling at 6879 mph (the speed at which the earth rotates on its axis), would appear motionless to an observer on earth. From that height, Clarke reasoned, a radio relay station could cover one-third of the earth's surface; three such satellites, placed in geosynchronous orbit around the equator could provide worldwide communications. In 20 years, advances in electronics, miniaturization and rocketry made Clarke's dream a reality and gave the world improved communications capability.

Likewise, in 1969, Mini-Circuits made its total commitment to serve the emerging communications market . . . by replacing expensive, custom RF signal-processing components with low-cost, catalog units with unparalleled reliability.

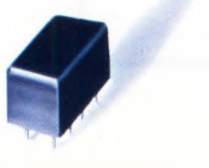
Our dream, like Clarke's, has come true. Over 1,000 catalog items available with such Mini-Circuits innovations as our exclusive HTRB burn-in testing, the world's only 3-year guaranteed mixers, computer-automated performance data (CAPD) to eliminate design guesswork . . . just to name a few.

Mini-Circuits' products have become the industry standard. We are actively dedicated to the pursuit of further improvements in product cost/performance, quality and reliability for more effective worldwide communications.

finding new ways . . .
setting higher standards

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CIRCLE 142

F79 Rev. Orig.

ON REFLECTION



Making the most of optical disks depends on accurate retrieval

One of our dreams is to replace all the clutter and paper on our desks and in our files with a system that easily stores the information in a compact chassis. Rather than shuffling through stacks of paper, we could pull out a page of information merely with the touch of a key and then display it in a window on a screen.

With gigabyte optical disks, we at last have the vast memory we would need to do that. For instance, one system can practically replace 800 standard filing cabinets. Another optical disk can hold 1 terabyte—at an amazing 80¢ a megabyte. Optical disks rely on a laser beam to burn holes into a tellurium alloy; each hole represents one bit. In that way, the disks can hold billions of bits of permanent data, none of which is affected by light, magnetic fields, or sound.

Having so much memory at hand is an ideal situation for a system designer. Yet one question remains: Has the technological advance actually preceded practical use? The problem revolves around organization, not capacity. Consider how desks and files are organized: Some filing is alphabetical, some chronological, some topical; others are arranged by priority or by guess. In fact, with the fairly random nature of the typical filing system it is a miracle that we can find a piece of paper at all. Nevertheless, we seem able to reach into the right file or drawer and retrieve the correct document—if not immediately, then within one or two tries. Conventional computers cannot do that.

Perhaps the solution lies in artificial intelligence. Because human beings think through association, AI machines are programmed to "think" that way, too. The similarity stops there, however: Human beings can think in a disorganized manner, computers do not have that facility. However, the presence of huge-capacity optical memories virtually mandates that computers be able to retrieve randomly organized information.

A good definition of goals and techniques—especially in terms of artificial intelligence—would go a long way toward structuring data retrieval for the coming generation of optical disks. Otherwise, those devices may end up collecting reams of paperwork—with no way of calling up the information easily. Unless we pay closer attention to ways of organizing information, we may resort to using a nice icon—the wastebasket—for all data.

Heather Bryce

Heather Bryce

Gould AMI... Innovation and Quality in Semiconductors

The double-metal answer to sluggish gate arrays.



What are you waiting for? Move into the world of 1 to 3 ns gate delays.

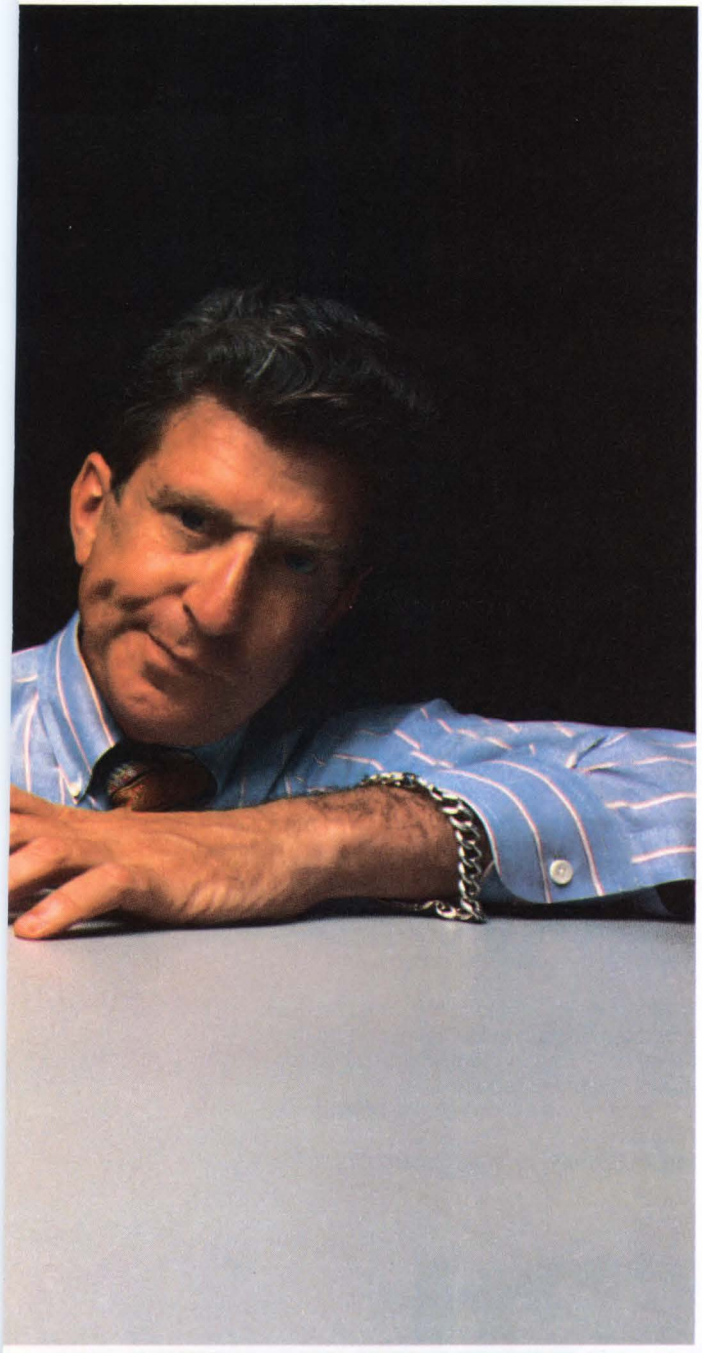
Gould AMI 3μ double-metal HCMOS technology opens up applications once considered too fast for CMOS gate arrays. Now, you can have low cost and power consumption without giving up speed.

Fast circuit design and delivery.

These double-metal arrays don't just work faster—they're designed faster. One reason is Gould AMI's growing library of macro cells. Over 100 popular functions—predefined and pretested—allow you to avoid wasting time and money reinventing the wheel.

Also, Gould AMI's fully integrated CAD software places and routes each programmable level automatically. More than fast, it can utilize over 98% of available gates!

Gould AMI offers 3μ double-metal arrays from 1100 to 4000 gates. (Later this year, our 2μ family will provide up to 10,000 gates.) Delivery in production quantities takes just 5 to 7 weeks from prototype approval.



Service just as fast and flexible.

We can do everything from design through fabrication—or any part of the job you wish. Gould AMI CAD software runs on Prime® and VAX™ computers. Our macro cells are available on major workstations. We can train your designers. And there's second sourcing, of course.

You're invited to find out more about the Gould AMI gate array program. Call us at 408-554-2311, or return the coupon. Because if the job is making CMOS gate arrays faster, Gould AMI is right for the job.

Prime® is a registered trademark of Prime Computer, Inc.
VAX™ is a trademark of Digital Equipment Corporation.

Yes, I want faster gate arrays—fast!
Tell me all about Gould AMI's:

- ☐ Complete gate array line.
- ☐ Complete standard cell line.
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- ☐ Macro cell libraries.
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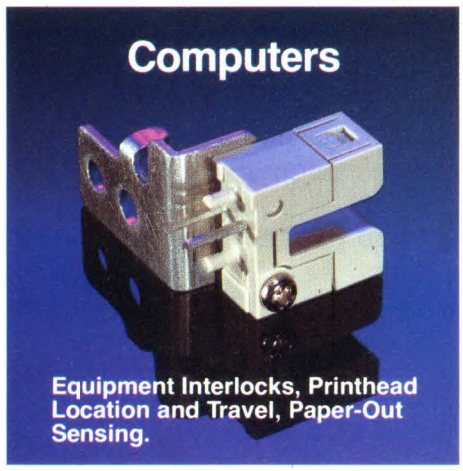
Mail to: Gould AMI Semiconductors
Gate Arrays Marketing
3800 Homestead Road
Santa Clara, CA 95051

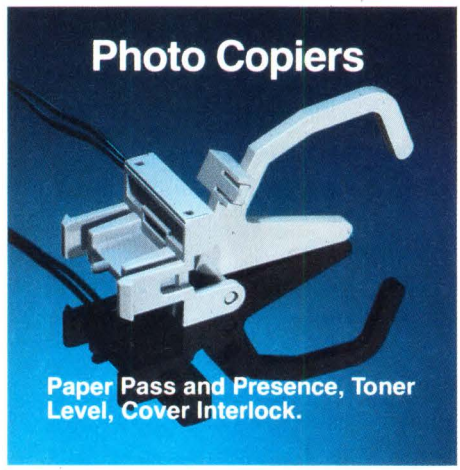
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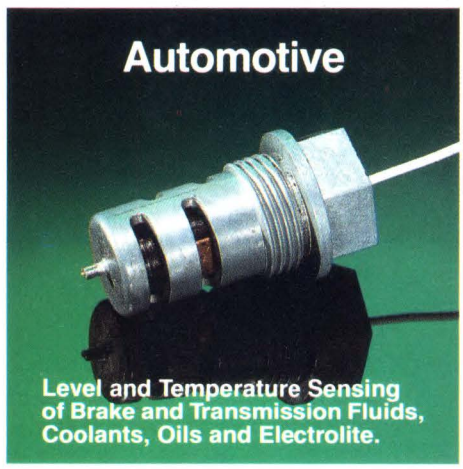
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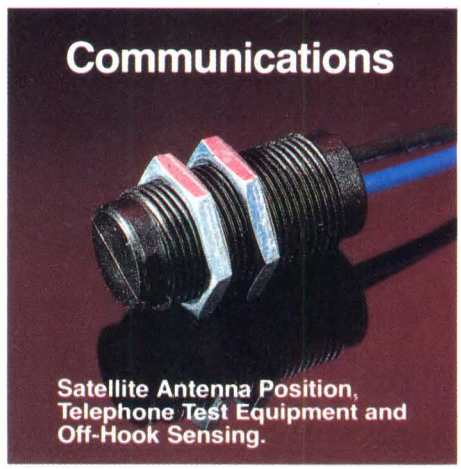
AMI Semiconductors

Q. Whose Magnetic Sensors Are The Big Companies Turning To? A. Aleph International, That's Who!









The top "Fortune 500" companies like IBM, Xerox, AT&T, Toyota, and Honda, just to name-drop a few, are turning to Aleph International for innovative magnetic sensors in all sizes and shapes.

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We're set up to respond to your needs quickly. And to produce a high volume of MagneSensors in a short time. Built to your exacting specifications.

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CIRCLE 6

READER FEEDBACK

Where's the info?

I looked forward to reading your July 12 cover article, "Low-Voltage FETs Slash On-Resistance to Boost Power Density" [p. 125]. In five pages the only concrete information concerns decreasing the die size and therefore the cost of manufacture. At the least the authors could have given data on one particular unit of the series. No one could design from this article, and there isn't even a reference for further information.

The article should have given capacitances, which determine driving current; input breakdown voltage; input voltage for minimum forward resistance; thermal resistance with actual numbers; and an output family from which to determine how closely the devices approach the ideal pentode curves with horizontal and vertical output lines and how sharp the transition is from vertical to horizontal.

The fact that this information is omitted makes me wonder whether it's because it isn't too good.

Name witheld

Even faster

Reader R. E. Pickvance is mistaken in stating that Texas Instruments' TMS 320 digital signal-processing chip requires 1.9 ms for a 64-complex-point FFT [July 12, p. 15].

Indeed, TI did list that time for a radix-2, *looped* 64-complex-point transform (ELECTRONIC DESIGN, Aug. 19, 1982, p. 154). But it also noted in the article that an in-line code version would take 783 μs, the unacceptable penalty being that 3722 of the 4906 program memory locations are required.

However, DSPS Inc. has been offering a 580-μs 64-complex-point FFT for the TMS 320 since December 1982. The key to the speed and the reasonable memory requirements (2700 locations, leaving more than twice the *total* memory of the competing NEC 7720 for non-time-critical control) is a superior algorithm architecture (radix 4). The program was created through automated code generation techniques.

DSPS's latest benchmarks for standard TMS 320s (with 4 kbytes of ROM) are 535 μs, 2.4 ms, and 6.2 ms for 64-, 128-, and 256-complex-point FFTs, respectively—including bit reversal. The latter two are program-memory-to-program-memory times and allow for double buffering. That is, data is collected into one buffer while the other is transformed.

The TMS 320 has a deceptively simple architecture and is capable of some relatively astonishing results.

L. Robert Morris
President
DSPS Inc.
Ottawa, Canada

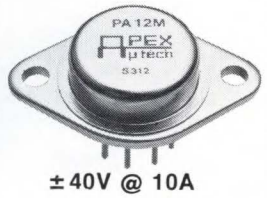
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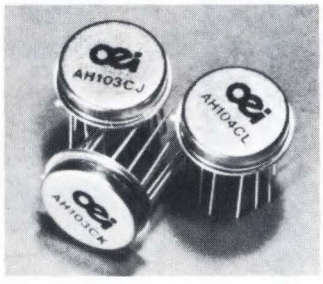
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CIRCLE 7

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CIRCLE 8



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LXD

CIRCLE 9

READER FEEDBACK

Left out

We would like your readers to know that the directory of manufacturers you published in your June 28 Focus on Switching Power Supplies [p. 301] is incomplete. For one, it omitted our company.

Scotty Wallace
Vice President, Sales and Marketing
Teapo Electronic Corp. of America
Norcross, Ga.

Add the smallest to the list

I have just come across your very interesting Focus on Subminiature Switches in the Aug. 23 issue [p. 301]. Since our company was not mentioned, I feel that your readers might be interested to know that Schurter offers the smallest pushbutton switch family (alternate and momentary action) with built-in LED and mechanical indicator in the world.

Bruno H. Schurter
President
Schurter Inc.
Petaluma, Calif.

Correction

The Aug. 23 New Products story on Western Digital's WD2400 chip set for tape control and formatting (p. 283) should have referred to the SASI throughout (rather than to the SCSI). Also, the present schedule calls for the chip set to be available early in 1985.

Win Exciting Prizes!

enter Mini-Circuits'

Design Contest



IBM® PC Personal Computer,
dual disk-drives, printer, software
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A complete system . . . **a $4,000 VALUE!***

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electronic tuning . . . including 6 tapes
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IBM is a registered trademark of International Business Machines Corporation.
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F 93-A REV. ORIG.

Design Contest

MICROWAVE JOURNAL OFFICIAL JUDGES

It's Easy to Enter

Do you have a clever design idea or application involving IF/RF/microwave signal-processing components—mixers, power splitter/combiners, attenuators, RF transformers, directional couplers, amplifiers or RF switches? Or perhaps a versatile setup for testing them or a novel approach to enhance their performance.

If you have an original idea, enter Mini-Circuits Design Contest now. Type or legibly print your submissions. Start with a brief abstract describing the key point of your idea (cost saving, improved performance, simplified testing, etc.). List RF signal processing components used. Then proceed with the detailed explanation. Make schematics and block diagrams clear; include values of circuit components. Be sure to include performance data and curves; judges' scores will be based on content, multiplicity of products involved and thoroughness.

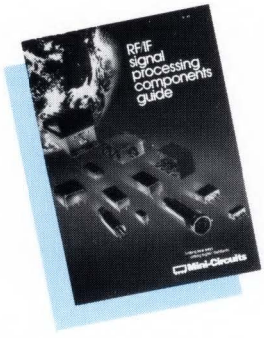
Contest Rules

1. Submit as many entries as you wish.
2. Ideas should be original and non-proprietary.†
3. Entries will be judged by the editorial staff of Microwave Journal and their decisions will be final. The top 25 winning entries will be published in Microwave Journal.
4. All entries become the property of Mini-Circuits Laboratory and must be received by December 31, 1984.
5. Employees of Mini-Circuits Laboratory, Microwave Journal and their sales representatives, are not eligible.
6. Contest void where prohibited by law.
7. Make sure to include your business address and phone number. In addition, for non-U.S. entries, indicate AC power line voltage and frequency.
8. Send your entries to:
   Mini-Circuits' Design Contest
   P.O. Box 137
   Brooklyn, NY 11235

†Winners may be asked to sign an affidavit of eligibility & release.

Good Luck, and Thanks.

The Mini-Circuits Design Contest, with its competitive excitement and fabulous prizes, is our way of thanking all of the designers worldwide whose staunch customer support has been responsible for our continuing growth.



Free 64-page RF/IF Signal Processing Components Guide

For an up-to-date review of Mini-Circuits' IF/RF/Microwave product line, refer to EEM, EBG, Gold Book or Microwaves Directory. Or call/write our factory or any of our 45 worldwide sales offices for our 64-page RF Signal-Processing Components Guide.



Free fact-filled Question/Answer Series on RF Signal-Processing Components

Since Mini-Circuits is the world's largest manufacturer of mixers and RF signal-processing components, it's natural for us to receive hundreds of questions from engineers on these products. How to test them, how to make the right selection, how to optimize a circuit design ... questions with answers not found in textbooks or reference manuals.

So we've put together a series of Q & A (question/answer) booklets on most-frequently asked questions on mixers, phase detectors and power splitter/combiners. They are loaded with application-oriented tips, ready to solve a problem you may be facing. The set is free ... just call or write us or any of our 45 worldwide sales representatives.

F 93-B REV. ORIG.

send your entries to:

Mini-Circuits' Design Contest
P.O. Box 137,
Brooklyn, New York 11235

EXAMPLE 1:

Low-cost, high performance Image-Rejection Mixer.

KEY COMPONENTS; mixers, power splitters.

Many telecommunications systems require a mixer arrangement that delivers the desired IF and sharply rejects the other image frequency.

An effective, low-cost solution makes use of Mini-Circuits' TFM-2 mixers and it's 2-way, 0° PSC-2 and 2-way, 90° PSCQ-2-90 power splitter/combiners as shown in the diagram.

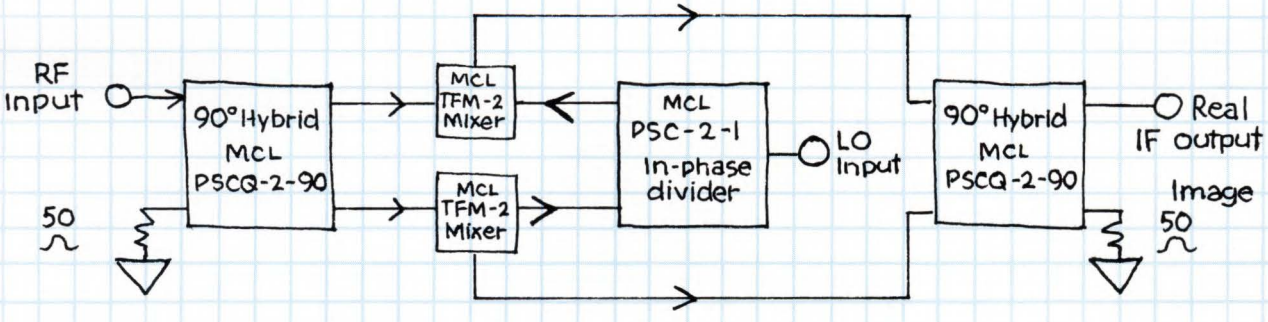
The key to an efficient image-rejection, such as shown in the block diagram, is the use of double-balanced mixers with well-matched amplitude and phase characteristics and high isolation. However, poor hybrid phase characteristics, differences in the output amplitudes of the hybrids and non-symmetrical external circuits will also reduce image-rejection performance. The effects on sideband suppression caused by unequal mixer amplitude and phase shift are shown in Tables 1 and 2.

Table 1
Amplitude Unbalance vs. A, dB

Unbal, dB	A, dB
0.3	35
0.9	27
1.5	22
2	13
3	15

Table 2
Phase Unbalance A, dB

Phase Unbal, degree	A, dB
3	33
9	22
15	18
20	15
30	12



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Engineering Dept.,
Alphaomega Corp.,
11 Madison Street
Key Biscayne, Florida 33149

finding new ways...
setting higher standards
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EXAMPLE 2:

Improving two-tone, third-order IM measurements.

KEY COMPONENTS; power splitters, attenuators, amplifiers

Two-tone, third-order intermodulation (IM) expresses the degree of non-linearity of an amplifier or mixer. This parameter is generally not included on data sheets because it is dependent upon operating frequencies, terminating impedance and input levels; it must be measured under specific design performance conditions.

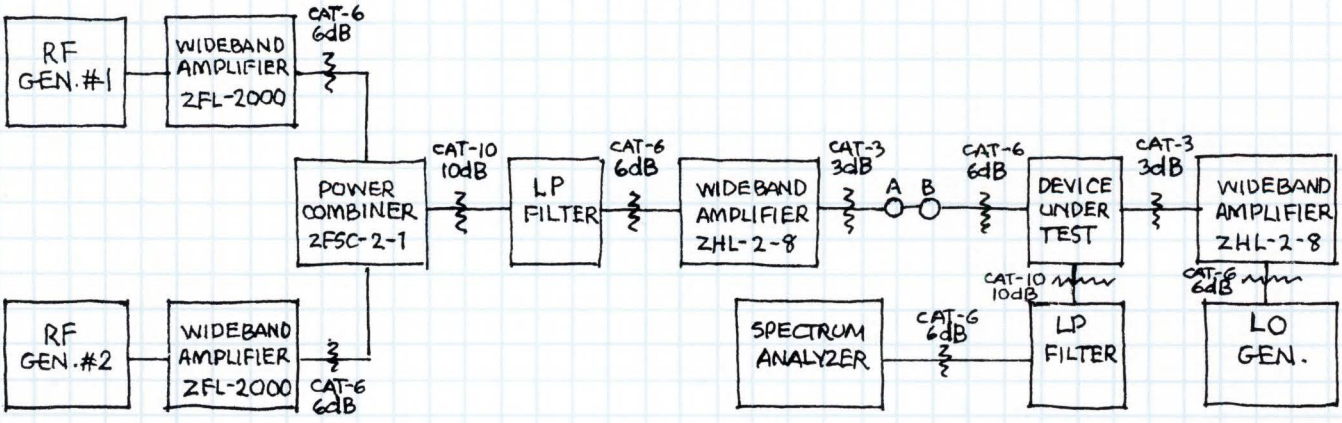
Two common errors in these measurements are (1) failure to provide adequate isolation between input signal generators and proper impedance matching and (2) insufficient filtering of the two input test signals.

A proper test setup for measuring two-tone, third order IM distortion is shown. Note the use of two amplifiers and 6dB pads for input generator isolation and proper 50 ohm matching. A practice of simply using a Tee-connector between generators developes mismatches, producing undesired harmonics which dramatically affect accuracy.

Two-tone, third-order IM distortion is only meaningful when the input levels to the device-under-test are defined.

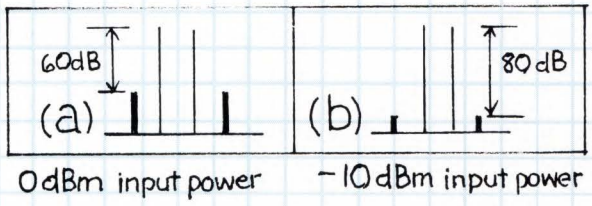
Examine the spectrum analyzer display for a ZAY-1 double-balanced mixer. Notice the significant difference in two-tone, third-order component with an input level of -10dBm for each tone (b) compared with 0 dBm input level for each tone (a).

Also, the amount of two-tone, third-order must be specified relative to either the RF input or desired IF output; the desired IF output is more meaningful.



GENERAL NOTES

1) All Mini-Circuits products have model numbers shown.
2) 0dBm input, A-B connected as shown
   -10dBm input, insert CAT-10, 10dB between A-B



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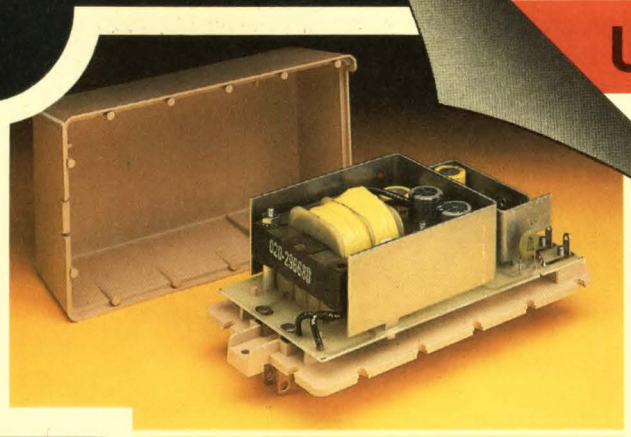
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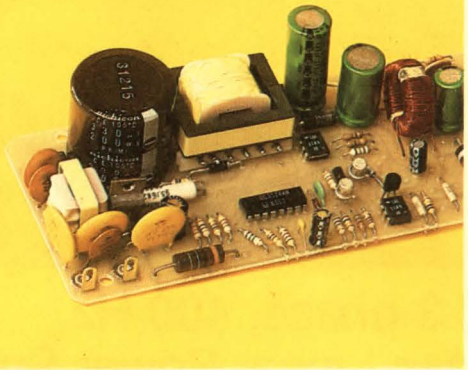
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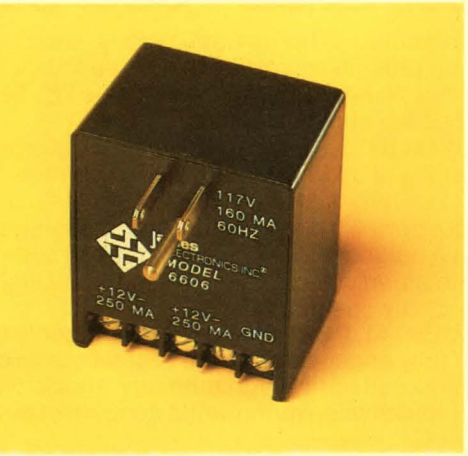
MADE IN USA

Why James is the leader

in telecommunication transformers and power supplies.







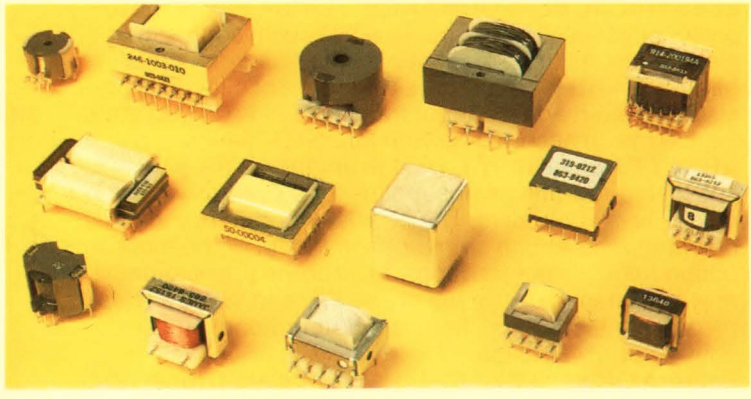
James advanced CAD/CAM designed transformers and power supplies have become the standard for quality and performance in the telecommunications industry. Here's why James is most often specified . . .

- We're a U.S. equipment manufacturer. That means on-time deliveries without the hassle of letters-of-credit, off-shore expediting or expensive shipments.
- We know what "telephone" quality means. We build it into every product . . . and inspect for it in every shipment.
- Innovative engineering has kept our product lines competitively priced . . . with performance assured to rigid industry and MIL-grade QC standards!

James supplies telecommunications transformers for all signal and power applications. Our power supply line includes plug-in, wall-mount and floor models . . . both linears and high efficiency switchers in the 2-100 watt range. They're all designed to meet FCC (Part 68) and UL requirements.

Write for complete technical specifications. You'll find our engineering consulting services for custom designs very price-competitive, too!

CIRCLE 10



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For demanding airborne applications, such as acoustic data processing, electronic surveillance and countermeasures equipment, Abbott's new WL Series of compact power supplies deliver:

MORE POWER IN LESS SPACE. WL Models provide power densities of up to 3.67 watts per cubic inch, with a maximum case height of just 2.5 or 2.75 inches, depending on output power. This permits a space savings of up to 60%, since a balanced ac power distribution system can now be maintained without resorting to three single-phase supplies or costly custom designs.

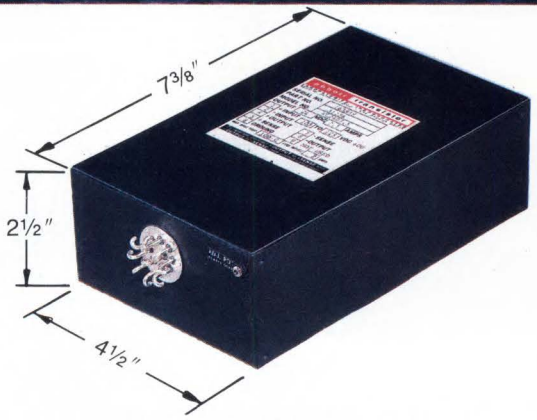
ENVIRONMENTAL PERFORMANCE. Ruggedly built WL Models are fully encapsulated and hermetically sealed to protect against salt spray, high humidity, shock, vibration and other applicable environmental conditions defined in MIL-STD-810C.

ELECTRICAL PERFORMANCE. The low EMI of these power supplies ensures compatibility with sophisticated electronics. All units meet applicable requirements of MIL-STD-461B for emissions and susceptibility. They are also protected against input transients of up to 180 Vrms for 100 ms, in accordance with MIL-STD-704.

ABBOTT RELIABILITY. Design engineers have been specifying Abbott power supplies for 23 years...whenever reliability is imperative. The consistent performance that has made the Abbott single-phase Model W the most popular 400 Hz power supply in airborne applications is now available in our new 3-phase WL and WWL Series. Please contact Abbott Transistor Laboratories, Inc., Power Supply Division.

Eastern Office: (201) 461-4411. **Southwest Office:** (214) 437-0697. **Western Office:** (213) 936-8185.

Call or send for Specs and Full Line Catalog



- Input: 105-125 Vrms, 380-420 Hz, 3-phase "delta" std. 3-phase "Wye" input optional
- Single and dual outputs, 5-28 Vdc
- Output power 48 to 420 Watts
- Low ripple of 5 mVrms, peak-to-peak 25 mV
- High 55% efficiency
- Load regulation: 0.1% from no-load to full-load
- Operating temperature range −55°C to +100°C

HIGH RELIABILITY:
MTBF CALCULATED PER MIL-HDBK-217D

	Standard	ER Version
Ground benign	164,406 hours	883,580 hours
Air-inhabited	25,633 hours	94,956 hours

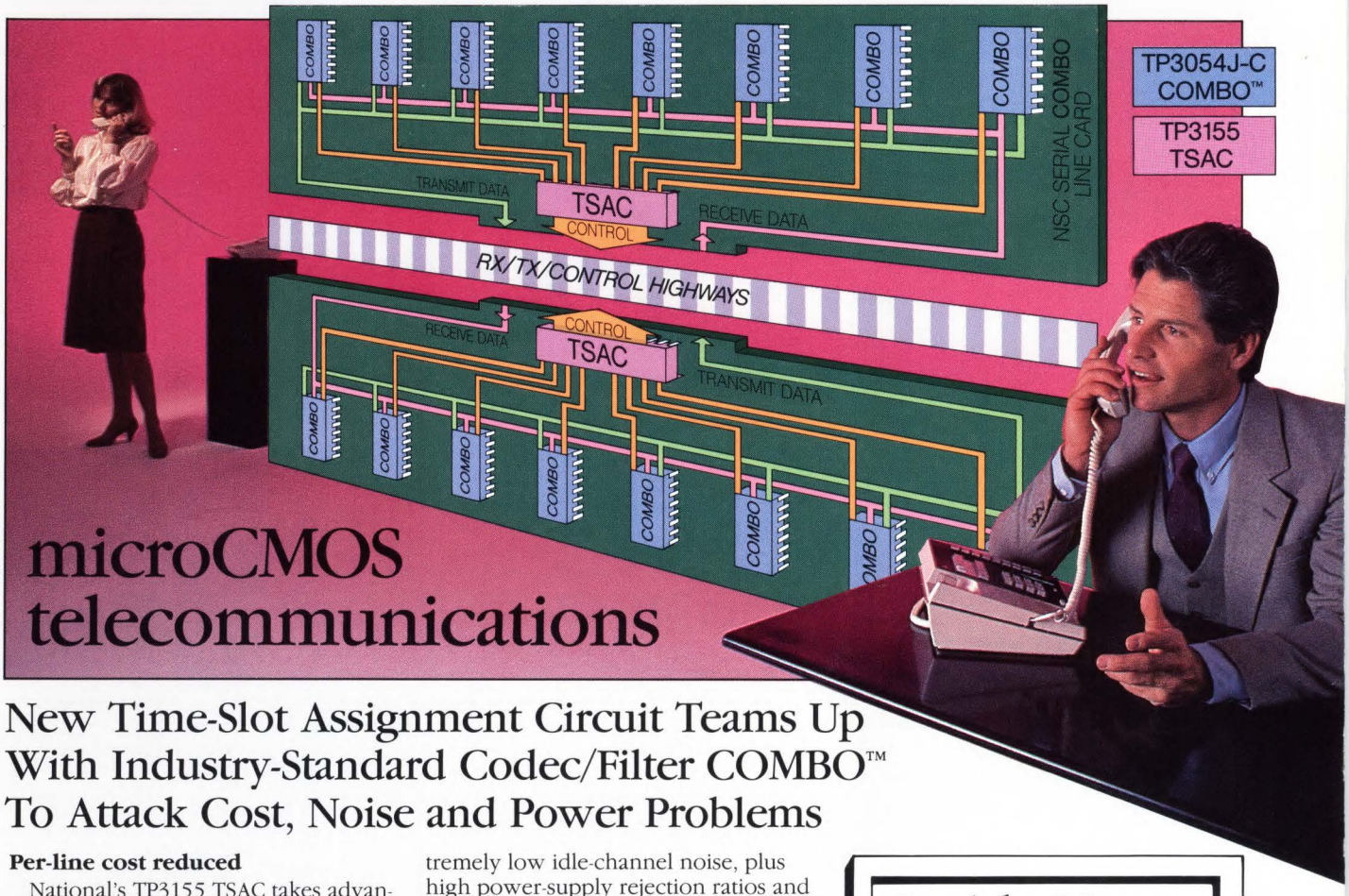
abbott

MILITARY POWER SUPPLIES

CIRCLE 11

NATIONAL ANTHEM®

Technology News From National Semiconductor 54



New Time-Slot Assignment Circuit Teams Up With Industry-Standard Codec/Filter COMBO™ To Attack Cost, Noise and Power Problems

Per-line cost reduced

National's TP3155 TSAC takes advantage of microCMOS density to provide a low-cost, single-chip replacement for expensive, conventional discrete logic and software.

One TSAC can be shared over four COMBO lines in a bidirectional system, and eight COMBO lines in a unidirectional format. This spreads the already-low TSAC cost over a large number of subscriber lines.

In addition to lowering per-line costs, the TP3155 offers design-in ease and flexibility, by providing a serial control interface compatible with the popular TP3020/2910 codecs. The new circuit features a 4.096MHz clock rate, independent transmit and receive time slots, and up to 64 time slots per frame.

Noise problems silenced by TP3054/57J-C COMBOs

Noise, the most important consideration in designing a line card, is effectively reduced by National's workhorse TP3054/57J-C COMBOs, which use microCMOS technology to deliver extremely low idle-channel noise, plus high power-supply rejection ratios and high stability.

These COMBOs perform the complete range of codec/filter functions, including those of transmit highpass/lowpass filters with prefiltering, and receive lowpass filters with post filtering. This capability further ensures low noise characteristics and maximum cost effectiveness.

Low power requirements

With PBX and Central-Office systems tending to provide higher and higher line capacities, both the TP3155 TSAC and TP3054/57J-C fully utilize the ultra-low power supply current offered by microCMOS technology.

Specifications in the low 'milliwatt' area guarantee minimal line-card and system current drain, expanding cost benefits still further.

Lower line costs, less noise, lower power needs—these features and more make the team of National's TSAC/COMBO a very difficult act to follow.

For complete information, check box ***S7*** *on the back page of this Anthem.*

Inside News

CMOS

2-Micron gate array software.

New display drivers handle all technologies—LED, LCD, VF.

NS32000

The ultimate UNIX machine.

New Products

Serial communications at no extra cost.

Programmable logic analysis software for Apple-DOS

Hard-disk design gets cost-effective separator/synchronizer chips.

Advanced FM IF circuits for low-distortion stereo.

5V-Only EEPROM offers fast read access.

New bipolar gate arrays replace low power Schottky.

National's 15ns PALS—industry's fastest!

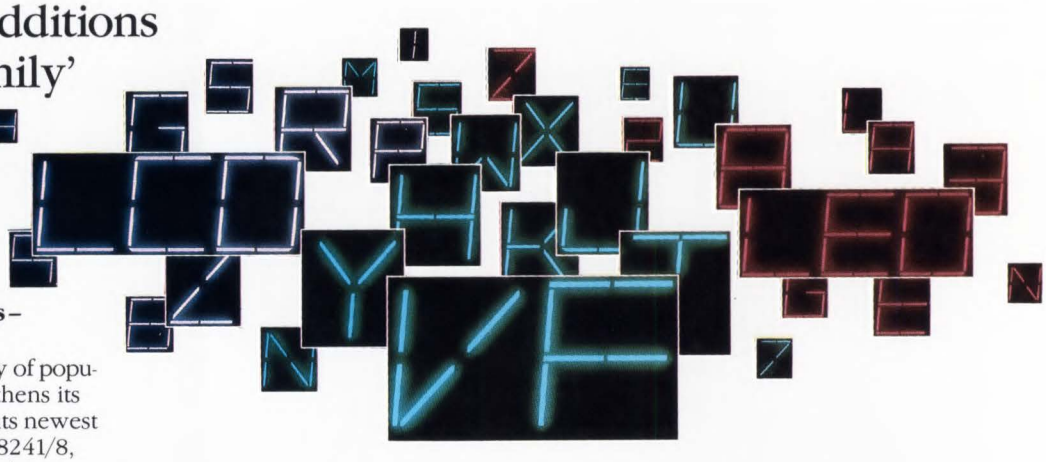
Tape-and-Reel. National's new industry standard.

Quality

Ship-to-Stock program reflects customer confidence.

National Semiconductor

Versatile New Additions To the 'First Family' Of CMOS Display Drivers



For all display technologies – LED, LCD and VF

National's broad-based family of popular display drivers now strengthens its leadership position by adding its newest VF and LCD drivers – the MM58241/8, MM58341/8 and the MM58538/9, MM58540/8 respectively.

Unrivaled compatibility

Each driver in this comprehensive 22-member family offers function-similar features – a simple serial data-input channel, a 31- to 35-bit shift register, latches, and buffer/drivers for direct interface to respective LED, LCD or VF displays. This compatibility provides users with true design flexibility in selecting display technology.

VF products: direct microprocessor interface plus full features

High-voltage MM58241/8 (up to 60V) and MM58341/8 (up to 35V) VF drivers furnish a direct, simple interface from microprocessor to display. In addition, they offer on-chip pull-down resistors, direct serial data and clock interface, on-chip brightness and blanking control, and data-out for easy cascading. Each is ideal for driving multiplexed VF displays such as 5 x 7 dot-matrix character arrays.

Equally important, the new VF drivers fit a wide scope of customer applications, from sophisticated instrumentation to automotive dashboard readouts and word-processor text displays.

With industry-first metal gate CMOS and full software compatibility, National's VF display drivers become instant favorites with both hardware and software engineers.

Unique flexibility in multiplexed 32/34-bit LCD drivers

Socket-equivalent to the HLCD0538 series, National's innovative MM58538 family provides full TTL compatibility plus alphanumeric, dot-matrix, and bar graph display capabilities.

Advanced features like these bring engineers of microprocessor-based systems the true flexibility necessary to maintain their competitive edge.

Traditional quality and performance

The new VF and LCD driver family members are carrying on an all-important National tradition of high-performance, first-quality drivers offered at a reasonable cost – for all popular display technologies.

*Check box **S3** on the back page of this Anthem to receive National's display driver family brochure.*

Now, 2-Micron Gate Array Software For Daisy, Mentor

Semicustom technology on the move

National continues to set the pace in semicustom technology with its gate array workstation support package.

This advanced software permits development of National's 2-micron microCMOS ICs on such leading computer-aided engineering workstations as Daisy and Mentor.

Now, for the first time, design engineers can take advantage of National's advanced gate array design tools – plus its industry-leading 2-micron processing technology – without ever having to leave their home facility.

Facilitates fast, accurate design

Designers simply breadboard a circuit on the workstation screen by using the new software package – then interface with National's mainframe to develop semicustom ICs. Circuit design time is reduced, while design accuracy and reliability sharply improve.

Fully supporting Daisy and Mentor, the software provides the complete range of semicustom development functions, including schematic capture, design verification, and auto-place-and-route.

Powerful design verification tools – graphically built in

With the new software, basic and complex logic building blocks, in addition to critical timing data, are built into the workstation and displayed graphically.

Timing parameters – including worst-case intrinsic gate delays, wiring capacitance delays, fanout, loading, etc. – let designers quickly simulate logic functions, and accurately estimate circuit performance. As a final check, actual delay calculations can be back-annotated after placement and routing is completed.

Complete IC design control

With National's workstation support software, users have total start-to-finish design control – control that dramatically improves designer productivity and reduces system costs.

*For more information, check box **S6** in coupon on the back page of this month's Anthem.*



National's Series 32000 – The Ultimate UNIX Machine

The Best UNIX micro

If your system design calls for UNIX™, industry experts have called the Series 32000™ "the best for UNIX".

National's GENIX,™ featuring optimized Demand Paged Virtual Memory support, is available today in source form for OEM adaption. The next generation of GENIX, with Ethernet™ support, is in test now. National has also delivered the Series 32000 version of UNIX System V (release 2.0) to AT&T for validation.

National's Series 32000 software catalog gives OEMs an opportunity to select from a wide variety of software, including offerings from independent software vendors.

True 32-bit architecture with Demand Paged Virtual Memory and Floating Point support

The word "complete" just took on new meaning in the world of 32-bit performance. National's Series 32000 microprocessor family includes the only commercially available 32-bit microprocessors offering it all – Demand Paged Virtual Memory, fast Floating Point, and efficient High Level Language support.

The Series 32000 is the only microprocessor family to offer true two address architecture. A detail which is a must when it comes to efficient high level language support. The Series 32000 is the most complete family of 32-bit CPUs, slave processors, peripherals, development systems and software on the market. Second place isn't even close.

Fast, compact compiler cuts code costs

National's CPU instruction set supports fast, highly compact C compiler code which, in turn, requires less RAM – significantly improving performance and lowering system costs. As the implementation language for UNIX, efficient C compiler support directly contributes to efficient system performance. National's C compiler fully supports all the architectural features of the Series 32000 family.

Powerful NS32082 MMU provides Demand Paged Virtual Memory

Thanks to National's advanced Memory Management Unit (MMU), the NS32082, Series 32000 micros are the only μPs in use today offering Demand Paged Virtual Memory.

This industry first not only brings you fast on-chip address translation, but full UNIX operating system support – making the Series 32000 the perfect choice for UNIX design environments.

Floating Point Unit heightens performance

The Floating Point Unit (FPU), the NS32081, allows operating speed up to 100 times faster than software emulation only, is easily designed into any 32- or 16-bit system.

FPU instructions can be used with any addressing mode, any operand length – and use any general purpose register. In addition, memory-to-memory operations are performed automatically.

Total Compatibility

Series 32000 CPUs offer total compatibility across the entire line, making it possible to develop a variety of systems with all the benefits of 32-bit software performance.

The same software can be incorporated in all systems within the family – a unique and all-important benefit for programmers and system designers.

Full 32-bit architecture – a systems solution approach

An elegant 32-bit architecture is the cornerstone of the Series 32000, and is implemented in all Series 32000 CPUs. This is 32-bit architecture from the top down.

Collectively, the features of the innovative Series 32000 – fast, space-saving compiler code, hardware floating point support, the only Demand Paged Virtual Memory offered in a microprocessor, total software compatibility, and immediate availability – assure you the speed, flexibility and cost-efficient performance you need for your system, particularly if your work centers around UNIX.

*For more information on Series 32000, check box **R7** in this Anthem's coupon.*



National's 15ns PAL Devices

Industry's fastest offer programmability at advanced Schottky speeds

With the introduction of the industry's fastest PAL® devices, National now offers design engineers an economical, high-performance replacement for costly Schottky logic.

The set of four high-density chips—the PAL16L8B with active low output, and the PAL16R8B, PAL16R6B and PAL16R4B with registered outputs—are manufactured with National's advanced OXISS™ bipolar process. This process produces logic devices with ultra-fast 15ns maximum access time.

Multiple, customized applications

Full programmability at advanced Schottky speeds gives systems engineers the design flexibility necessary for a broad range of customized logic applications without sacrificing performance. These include address coding, multiplexing, microprogrammed control store, arbitration, high-speed random gating, and many more.

Lower system costs

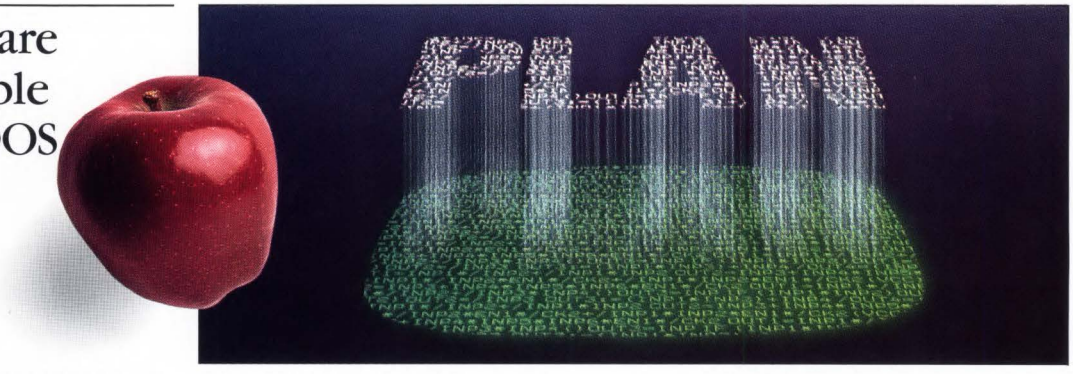
Complete integration and space-saving 20-pin ceramic or plastic dual-in-line packaging permit significant chip-count reduction and a corresponding cut in system cost.

Additionally, the new logic devices feature TRI-STATE™ outputs (which can be acted upon by input variables), and typical power dissipation of just 600mw.

No need for additional power combined with programmable design and the fastest access time available, make National's new 15ns PAL devices the cost-effective choice over any of the advanced Schottky logic families.

*For more information, check box **R9** on the back page of this Anthem.*

PLAN Software Now Available For Apple-DOS



Create disk files for multiple hardware options

PLAN™ (Programmable Logic Analysis by National) software gives systems designers using programmable logic devices a set of powerful interactive design and development tools.

Available for CP/M®-80, and MS®-DOS operating systems, PLAN software is now also available for Apple®-DOS.

Automatic device selection

Three PLAN programs—PLUS, SERV, and PROG—permit the creation and editing of disk files to provide a broad scope of hardware solutions.

PLUS, a Boolean equation entry/editing program, features algorithmic programmable device selection that includes pin-out assignment. The program automatically chooses the most efficient device—the one with the fewest fuses and registers.

With PLUS, systems designers can quickly find the most cost-effective hardware solutions. All error and time-waste associated with determining hardware requirements are eliminated.

Flexible design-in

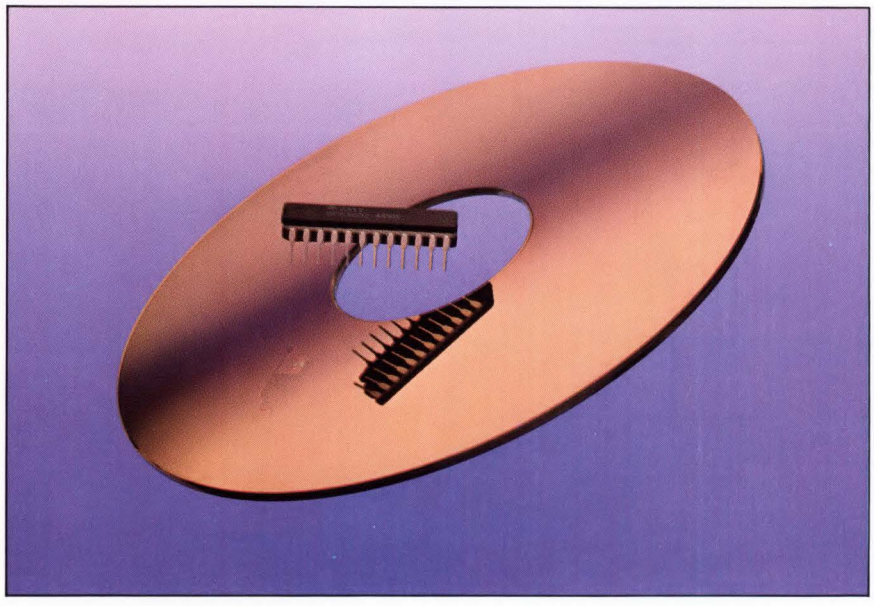
SERV offers optional device selection and pin-out editing as well as a documentation utility. In the edit mode, the SERV program allows editing of the pin-out assignment within the limits of the given equations and the selected device. In the documentation mode, SERV permits users to output equations, pin-out diagrams and fuse maps.

Taking the equation file created by PLUS and altered by SERV, the PROG routine generates the formatted programming data for the device. The program directs the formatted data, including optional user-defined test vectors, to a data file disk, system printer port, or CRT.

Broad logic applications

Designed expressly for 64K microcomputers, PLAN software has wide-range applications wherever logic is used—especially in computer processing, control systems and copiers. And with the new Apple-DOS version of PLAN software, even more systems engineers can take advantage of National's comprehensive logic design software.

*For more information on PLAN software, check box **S4** on the back page of this Anthem.*



The DP8460/8450 Data Separator/ Synchronizer ICs: Low-Cost Solutions to Disk Controller Design

With the introduction of the DP8460/8450 data separator/synchronizer chips, National continues its tradition of providing the disk industry with innovative, cost-effective design solutions.

The advanced LSI/VLSI circuits are user-programmable, making them design-appropriate for hard disks and high-density floppies that employ a host of codes and data rates.

No more external potentiometers

Performing the read-data synchronization PLL function, the DP8460 also features on-chip decoding circuitry for separating NRZ data and clock from MFM encoded data.

Additionally, the on-chip design frees board space for additional disk data path electronics.

Equally important, the DP8460 Data Separator offers an improved error rate by reducing window error and simplifying production testing with fixed external Rs and Cs.

DP8450 with synchronization only

Like the DP8460, the DP8450 Data Synchronizer chip performs basic PLL/synchronization—but produces only synchronized data and VCO Clock waveforms derived from the incoming encoded bit stream.

With a small pin-count of 20 (the DP8460 has 24), the DP8450 is quite cost effective. The high performance and high reliability characteristics, of course, are the same for both devices.

Applicable to workstations, communications networks and computers of all sizes, National's industry-first LSI/VLSI separator/synchronizer chips offer the disk controller designer an unrivaled pair of cost-lowering, space-saving design tools.

For additional information on these high-economy separator/synchronizer circuits, check box ***S5*** *on the back page of this Anthem.*

Advanced FM IF System With Low-Distortion, Single-Tuned Quadrature Coil

LM1865/1965

Market pressure for improved FM performance has paralleled the trend toward electronic tuning in car and home stereo systems.

National's new generation of FM intermediate frequency (IF) circuits, the LM1865/1965, gives radio/stereo designers the tools to ensure high performance while substantially reducing system cost.

Multi-feature ICs for quality receivers

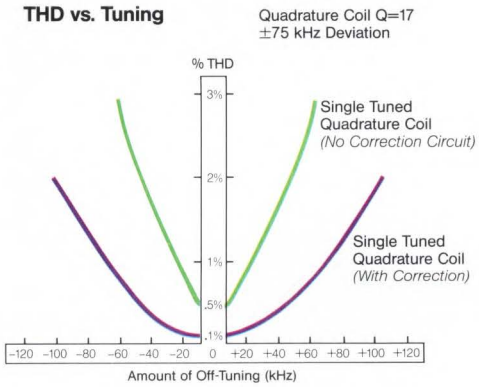
The LM1865/1965 system contains all active circuitry—from RF tuner output to stereo decoder input. The LM1865 provides sophisticated stop-detection circuitry for electronic tuning, while mechanical tuning is served by the deviation and signal-level mute function in the LM1965 version.

A new-design quadrature detector in both versions compensates for non-linearity, allowing high performance with a single-tuned coil. This compensation eliminates production adjustments of double-tuned coils, and guarantees low distortion.

First to incorporate ultrasonic noise detection

The LM1865/1965 is the first integrated-circuit implementation of ultrasonic noise detection for determining valid stop (or mute) conditions.

This feature, in conjunction with signal-strength detection and automatic fine tuning, means that a receiver will not stop on a noisy station, or between two strong adjacent signals.

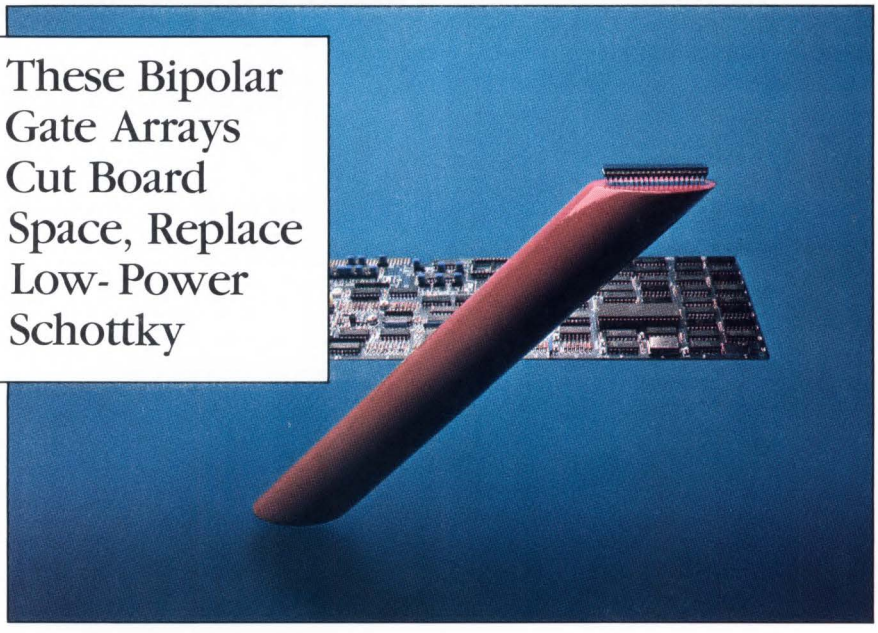


Additionally, the system is the first FM IF to provide a dual-threshold, automatic gain control (AGC). The AGC automatically detects the presence or absence of strong adjacent signals—and selects a high or low AGC threshold, allowing the best possible reception in all conditions.

These versatile FM IF circuits are appropriate in a broad range of design applications—from car, home and TV stereo receivers to satellite sound systems.

For more information, check box ***T1*** *in this Anthem's coupon.*

These Bipolar Gate Arrays Cut Board Space, Replace Low-Power Schottky



Available now

National's newest additions to its bipolar gate array family—the MCA500ALS and MCA1300ALS—provide design engineers with two more cost-cutting tools for custom LSI and VLSI circuit development.

Available now, the new macrocell arrays replace hard-to-find low-power Schottky while significantly reducing board space. And smaller boards mean smaller, less costly systems.

High performance, low power

Both MCA500ALS and MCA1300ALS are fabricated with National's advanced OXISS™ process. They internally employ emitter-coupled logic macrocell circuit technology and are TTL compatible to the outside world. Typical gate delay is 2.5 ns and power dissipation is approximately 1 watt per package.

Simple design-in

Producing LSI and VLSI designs with the new array devices is easy. Designers simply select the appropriate macrofunctions from the library, then define how to interconnect these functions to realize their design. Samples are delivered six weeks after the design has been completed. National also offers a design service converting circuit diagrams into fully functioning parts (turnkey design).

The MCA1300ALS uses the same macrocell concept as the MCA500ALS array. Each macrocell contains 54 transistors and ample resistors to create the necessary logic functions. The MCA500ALS has 77 macrocells equivalent to 533 gates. The MCA1300ALS offers 140 macrocells equalling 1280 gates.

National's macro library presently contains more than 80 logic functions. Designers can create these arrays on a workstation, or by accessing National's mainframe through user terminals.

Low power consumption, high reliability

Replacing low-power Schottky components with bipolar gate arrays reduces power consumption, allowing a smaller power supply, smaller system size and lower system cost.

Gate arrays pack many components into one piece of silicon, allowing systems with fewer soldering pins and less connectors—substantially increasing system reliability.

Many applications

National's new MCA500ALS and MCA1300ALS have broad-range applications in minicomputers, instrumentation, test and control equipment, and telecommunications. Wherever design engineers need a cost-reducing, high-performance replacement for low-power Schottky, National's new bipolar gate arrays are ready to fit the bill.

*For additional information, check box **S8** on the back page of this Anthem.*

National's NMC9817 EEPROM Reacts Fast For Home Alarm Systems

National's high-performance NMC9817 complements its full line of EEPROMs. Fast read-access time of 200 ns and fast write time of 10 ms maximum make these 16k EEPROMs compatible with high-performance microprocessor applications, such as home security/intrusion and fire alarm systems.

Dedicated microprocessor operation eliminated

Complete self-timing and AUTO ERASE before WRITE allows an efficient RAM-like write cycle. This frees the microprocessor to tend to other I/Os. The READY/BUSY signal on pin 1 notifies the microprocessor when the programming cycle is complete. During the 10-ms ERASE/WRITE operation, the CPU is freed.



Bus contention eliminated

Two-line control architecture eliminates bus contention in your system environment.

Parts count reduced

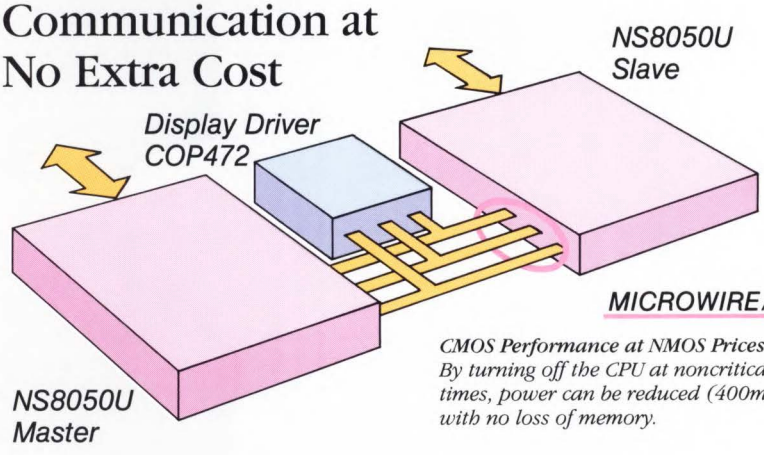
On-chip V_{pp} generation during ERASE/WRITE allows 5V-only operation in all modes, while on-board addresses and on-board latches completely eliminate the requirement for external circuitry.

Easier application design

The NMC9817 offers ease-of-design. It's ideal for storage of user-defined functions, calibration constants, configuration parameters, and accumulated totals.

*For more information, check box **P7** on the coupon shown on the last page.*

National's New NS8050U Microcontroller—Now Serial Communication at No Extra Cost



CMOS Performance at NMOS Prices
By turning off the CPU at noncritical times, power can be reduced (400mW,+4mW) with no loss of memory.

National's new NS8050U microcontroller offers multiprocessing and distributed processing capabilities via MICROWIRE/PLUS™ serial communications.

MICROWIRE/PLUS is an advanced three-wire serial communications protocol that makes it easy to communicate between two or more CPUs and to such MICROWIRE™ peripherals as A/Ds, EEROMs, display drivers, frequency generators and more.

Saves I/O lines

With MICROWIRE/PLUS, the lines needed by typical eight-bit controllers for data exchange with other processors and peripherals, are reduced from eight to three. This frees up I/O lines so designers can add more features and functions to their systems.

Serial communications reduces necessary pc board space, and markedly lowers system cost. Nicest of all, the NS8050U costs no more than a standard 8050.

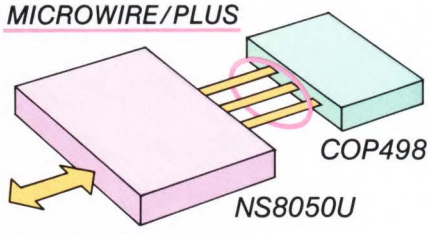
Straightforward design-in

Design-in is simple. The 8050U utilizes the familiar 8048 instruction set, plus two new instructions (XCHM and XCHS) required for serial communications.

Code generation and device emulation are fast and easy using National's MOLE™ development system. And, after developing the appropriate code, designers can use the NS8040U (ROMless version) controller to substantiate their design.

Rich feature mix allows multiple uses

Features like 256 x 8 RAM, programmable master/slave functions, and piggy-back emulation allow the new controller a diverse range of applications in such fields as automotive, telecommunications, home security systems, and more.



MICROWIRE/PLUS
Serial communication between two CPUs or multiple National MICROWIRE peripherals.

For any applications where eight-bit microcomputer systems require several peripherals—or where design engineers wish to upgrade an 8050-based system at no extra cost—the I/O-efficient 8050U microcontroller outshines the field.

*Check box **S9** on the back page of this Anthem for complete information.*



National Sets Standard For Surface-Mount Tape-and-Reel

As electronics manufacturers automate production lines and adopt surface-mount technology to lower manufacturing costs, a better way is needed to handle the high volume of chips used in surface-mount assembly.

National's new Surface-Mount Tape-and-Reel offers the perfect component-handling complement to these advanced manufacturing operations.

Less handling, more savings

With Tape-and-Reel, the assembly process is streamlined. Surface-mount components are held, during shipment and machine loading, in cavities of conductive plastic tape. Pick-and-place equipment automatically removes the components in sequence, placing them on the pc board quickly and accurately.

Because a Tape-and-Reel package holds 10 to 25 times as many components as a rail, the result is simplified device handling and sharply reduced labor costs.

Packaging technology of the future

Made from conductive PVC material, the tape resists static charge buildup, and each Tape-and-Reel carries a bar-code label for automated, error-free inventory management.

National's Tape-and-Reel is compatible with all surface-mount devices. These include small-outline transistors, small-outline ICs, plastic chip carrier ICs, and (coming soon) ceramic leadless chip carriers.

In addition, Tape-and-Reel specifications fully meet proposed EIA standard RS-481 (Taping of Surface-Mounted Components for Automatic Placing) to guarantee compatibility with all surface-mount pick-and-place systems in use today.

*For more information on the industry's leading Tape-and-Reel packaging, check box **T2** in this Anthem's coupon.*

Quality/Reliability is a matter of policy

National's Ship-to-Stock Program Reflects Customer Confidence

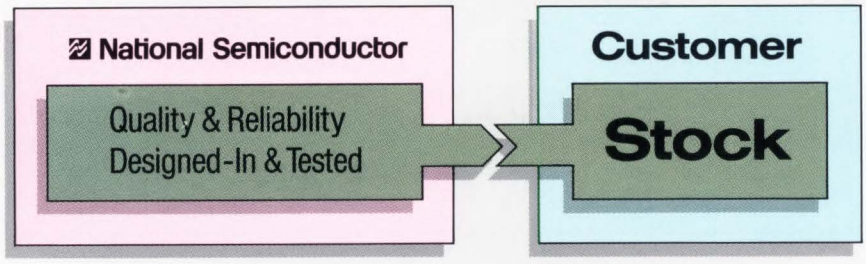
National is moving ever closer to its quality goal—a zero defect rate. In the past six years, the company's IC rejections have dropped from 8000 parts per million to an industry low of just 119 ppm.

That dramatic improvement in product quality has helped contribute to the strong success of National's innovative Ship-to-Stock Program.

Under the program, product is shipped directly to customer stock, eliminating the need for further electrical testing at customer sites. That's quite a vote of confidence for National's strict quality and reliability testing procedures.

Reduced manufacturing costs

The subsequent reduction in test equipment, inventory space, and labor hours means major cost savings for the manufacturer. Under the Ship-to-Stock Program, all elements are in place to help customers improve product quality—at board, subsystem, and system levels.



Broad-scale tracking and service resources

National's rigorous in-house test and assembly procedures ensure superior ICs. Continuous worldwide component tracking and reporting provide customers with up-to-the-minute reports on outgoing ppm levels.

Finally, National's Ship-to-Stock Program relies on the experienced engineers of the company's Quality Engineering Group to maintain top-line support—support that strengthens the quality of each customer's product line.

With effective, fully implemented programs like National's Ship-to-Stock, more and more customers are discovering the truth to the old adage "Quality begets quality."

News From Your National Library

M5 ☐ microCMOS Brochure
P7 ☐ NMC9817 Datasheet
R7 ☐ In Search of the Best UNIX Machine Brochure
R9 ☐ C.L.A.S.S. Brochure
S3 ☐ Display Driver Family Folder
S4 ☐ PLAN Product Bulletin
S5 ☐ DP8460 Family Folder—Disk Data Path Electronics
S6 ☐ Semi-Custom Workstation Support Information
S7 ☐ TP3155 Time-Slot Assignment Circuit Datasheet
S8 ☐ ECL/ALS Gate Array Family Application Guide
High Performance TTL Compatible Macrocell Array Application Guide
S9 ☐ NS8050U Information
T1 ☐ LM 1865/1965 Datasheet
T2 ☐ Surface Mount Tape and Reel Datasheet

M7 ☐ 1984 CMOS Databook $12.00
P0 ☐ Linear Supplement Databook 1984 $7.00
P1 ☐ Data Conversion/Acquisition Datebook 1984 $12.00
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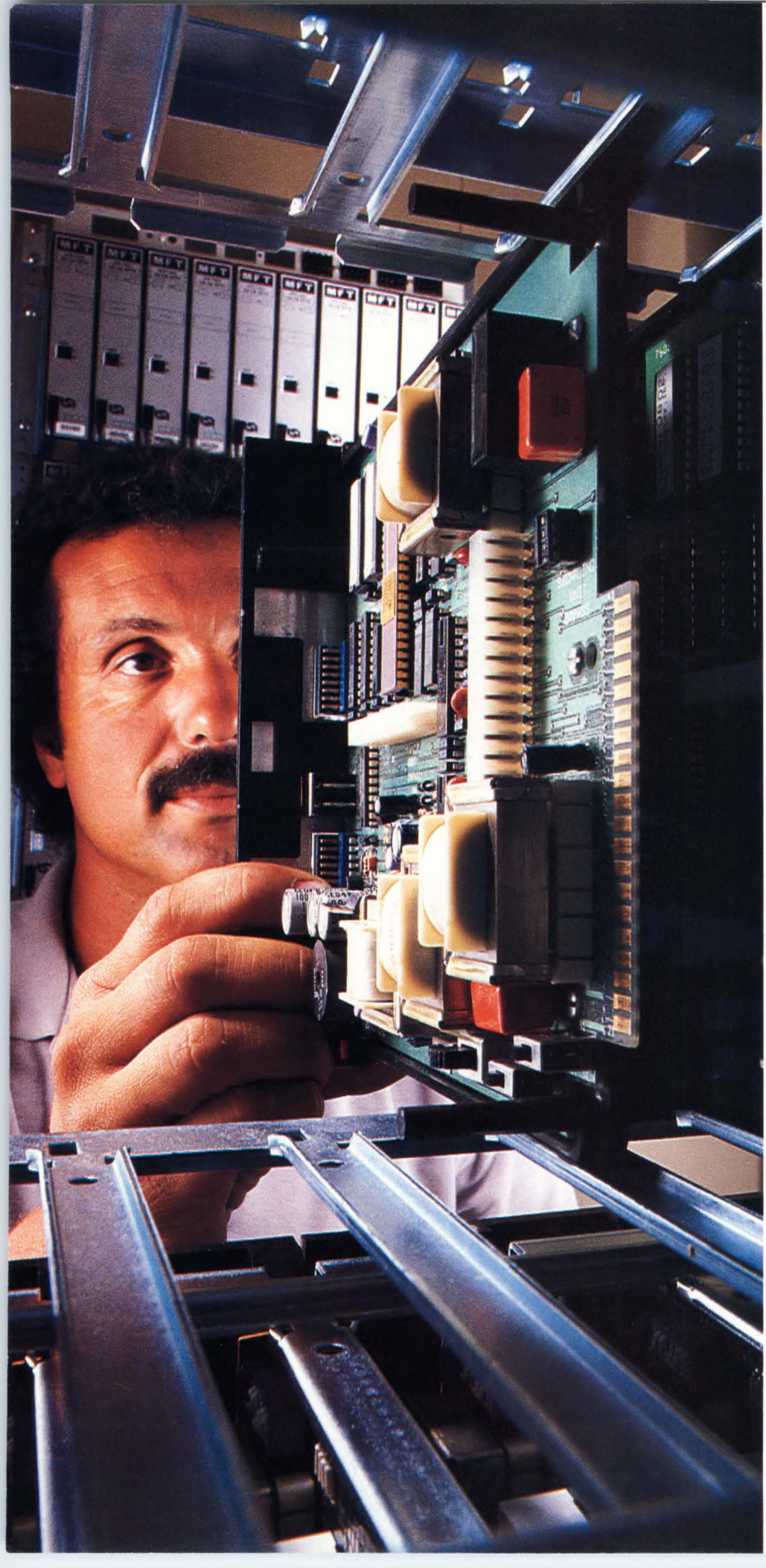
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Texas Instruments digital signal processor helps Lear Siegler Inc. make your message loud and clear...from anywhere.

- **TI's single-chip, high-performance TMS32010** digital signal processor (DSP) assures highest quality telephone transmission *(Page 2)*.
- **TMS320 DSPs from TI** support high-speed and numeric-intensive applications from communications to seismic processing *(Page 3)*.
- **Complete development support** for TI digital signal processors includes hardware, software, documentation, and application workshops *(Page 4)*. ▶



TI digital distortion

When you're depending on the telephone to get your message through, you don't need "singing" on the line. A standard two-wire circuit "sings" when signals traveling in opposite directions are insufficiently isolated in a repeater. To eliminate this problem, Lear Siegler, Inc., manufacturer of repeaters used worldwide, relies on the Texas Instruments TMS32010 digital signal processor (DSP). And cuts setup time for each repeater from hours to minutes.

In the unique VFR-7608 repeater, TI's TMS32010 performs all the functions of analog equalizers, filters, and amplifiers (see diagram opposite). It compensates automatically for line impedance 8,000 times per second. Completely isolates the opposing signal streams. Puts an end to "singing."

TMS32010 eliminates reflections "by the numbers"

The standard solution to "singing" is an analog network designed to cancel out reflected signals on the line. But even with expensive "precision" hybrids, the best solution is a compromise that limits usable bandwidth and gain.

Digital signal processing with the TMS32010 balances the circuit across the entire frequency band every 125 μs. Because the repeater adapts continuously, the circuit *cannot* "sing" at any frequency, and its gain can be fully utilized.

DSP cuts setup time to minutes

Tuning each analog repeater is an hours-long, trial-and-error procedure for a highly skilled technician. Using a comprehensive history of each circuit, he must set 68 switches in an analog repeater. TI's TMS32010 in Lear Siegler's new digital repeater eliminates 65 of those switches. Ends the need to keep detailed circuit histories. And the small, affordable plug-in unit is interchangeable with older repeaters.

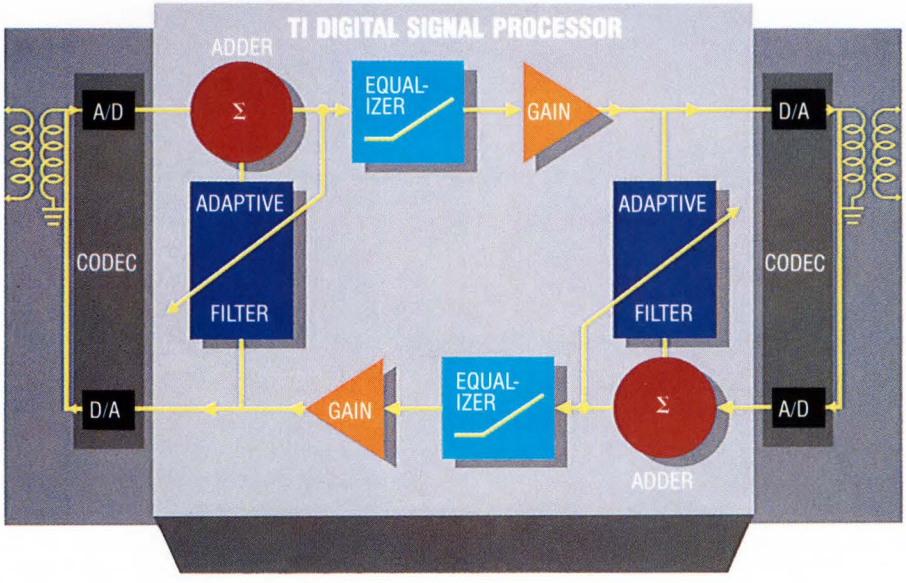
So your message can always come through—loud and clear.

◀ **Setup is as simple as 1-2-3** with Lear Siegler's adaptive telephone repeater using TI's TMS32010 DSP. Whereas manual adjustment of an analog repeater can take many hours, only three simple switch settings are required to assure rock-stable, "sing"-free performance from the digital repeater.

27-4973

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signal processor squelches in unique adaptive repeater.



Heart of the adaptive repeater is TI's single-chip, 16/32-bit TMS32010 digital signal processor. All the functions shown are achieved in real time through software operating on signals digitized by conventional single-chip codecs.

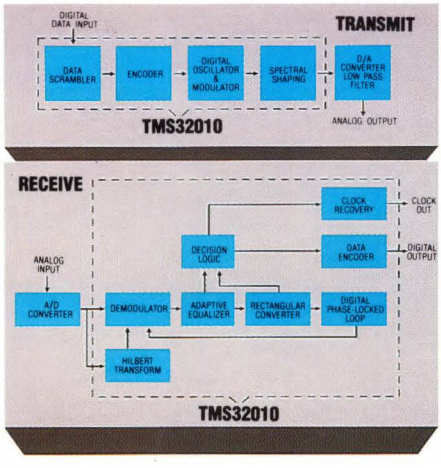
The TMS320 family from Texas Instruments: "Workhorse of digital signal processing."

The TMS32010, first member of the TMS320 DSP family, is TI's trailblazing contribution to an important new technology. A Lear Siegler engineer who has been following the progress of digital signal processing from its inception says, "The TMS32010 is the first device that can reliably do what we need. It's a real workhorse: The '8080' of DSP."

TI's TMS320 DSPs excel at high-speed, numeric-intensive applications

High-performance TMS320-family DSPs from Texas Instruments will find widespread use in many fields where large volumes of high-speed computation are required. In telecommunications, they can also be used to build high-speed modems with data-transmission rates up to 9,600 baud. They can make speech recognition, analysis, and synthesis practical. Speed image processing and pattern recognition. Facilitate high-speed process control and instrumentation. Process radar, sonar, and seismic signals. And furnish the multiple functions often required for a single application.

For example, a TMS320 DSP could enable an industrial robot to synthesize and recognize speech, sense objects and their orientation, and perform mechanical operations through digital servo-loop computations.



High-speed modem functions are effectively performed by TI's TMS32010, as well as such expanded functions as auto-dial/answer, dial-tone verification, busy-signal detection, and self-test routines.

The TMS320 family, with its extensive development support *(see page 4)*, can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, fast Fourier transforms—performing a 64-complex-point FFT in only 550 μs. And for seismic processing involving very low frequencies which only a digital system can implement.

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features and perform template comparisons for optical character recognition.

A one-chip alternative to bit-slice processing

TI's 16/32-bit TMS320 DSPs offer an inexpensive alternative to multichip bit-slice processors. They combine the flexibility of a high-speed controller with the numerical capability of an array processor—on a single chip, in one 40-pin DIP.

Highly pipelined architecture and a comprehensive instruction set give the TMS320 the speed to execute five million instructions per second with 32-bit precision: More than fast enough, for example, to handle the 40 additions and 40 multiplications necessary for realtime voice-frequency processing within the 125-μs sampling interval. A conventional microprocessor, operating at 8 MHz, would require 900 μs, and quickly become bogged down in the signal stream.

Now in three versions

The TMS32010 microprocessor has 288 bytes of on-chip data RAM, and can address up to 8K bytes of off-chip memory at full speed.

The TMS320M10 microcomputer is identical to the TMS32010, but it also includes 3K bytes of on-chip mask-programmed ROM.

The military version, SMJ32010JDS, is processed to the extended temperature range requirements of MIL-STD-883B.

To learn more about the many applications and available development support for TMS320-family DSPs, return the coupon on the following page.

See back page for more information.



In-depth support for the TMS320 family of TI DSPs includes a host-independent development system, an evaluation module, emulator and analog interface board, as well as assembler/linkers and simulators that can run on a variety of host computers and PCs. Documentation is extensive and thorough.

Develop your own DSP applications with comprehensive support from TI.

Texas Instruments has assembled an extensive group of development-support packages for the TMS320 family of VLSI digital signal processors *(see table)*. Included are all the hardware, software, and documentation you need to utilize the power and speed of TMS320 DSPs in your designs. A rapidly growing volume of third-party support is also available.

Use your own PC as a TMS320 development station

The latest addition to TI's development-support software is the TMS32010 Digital Filter Design Package developed by Atlanta Signal Processors Inc. It makes your Texas Instruments Professional Computer or IBM PC a cost-effective, easy-to-use, digital-filter design station. With it you can produce the TMS32010 source module. Then you can assemble the code and simulate it in software on the PC. Later you can download the code into the hardware-development system for realtime emulation.

Two versions are now available: **DFDP-TI001** for the Texas Instruments Professional Computer, and **DFDP-IBM001** for the IBM PC.

TMS32010 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
TI990	DX10	TMDS3240120-08
DEC VAX	VMS	TMDS3240210-08
DEC VAX	Berkeley UNIX 4.1	TMDS3240220-08
DEC VAX	Berkeley UNIX 4.2	TMDS3240230-08
IBM	MVS	TMDS3240310-08
IBM	CMS	TMDS3240320-08
TI/IBM PC	MS-DOS	TMDS3240810-02
Simulators		
DEC VAX	VMS	TMDS3240211-08
TI/IBM PC	MS-DOS	TMDS3240811-02
Hardware		
Evaluation Module (EVM)		RTC/EVM320A-03
Analog Interface Board (AIB)		RTC/EVM320B-06
Emulator		TMDS3262210

Learn in TI workshops

Texas Instruments supplies comprehensive documentation with each device. A growing library of application reports will also assist you in the design of digital signal processing circuits using TI's TMS320 DSPs.

Three-day DSP workshops, including extensive hands-on experience, are conducted periodically at Texas Instruments Regional Technology Centers. For registration information, call the Regional Technology Center nearest you: Atlanta, (404) 452-4686; Boston, (617) 890-4271; Chicago, (312) 228-6008; Dallas, (214) 680-5096; Northern California, (408) 980-0305; Southern California, (714) 660-8164.

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Please send me information about:

PR 22 ☐ TI's TMS320 family of Digital Signal Processors.
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IEEE International Conference on Computer Design (ICCD 84), Oct. 7–11. Rye Town Hilton, Port Chester, N.Y. Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

1984 ACM Annual Conference, Oct. 8–10. Hilton Hotel, San Francisco, Calif. Alexander Roth, 9900 Main St., Suite 303, Fairfax, Va. 22031; (703) 385-0211.

Electronics Manufacturing Technologies & Systems 84 (EMTAS 84), Oct. 9–11. North Carolina State University, Raleigh, N.C. Gerri Andrews, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500.

Circuit Expo '84, Oct. 16–18. Centrum, Worcester, Mass., Worldwide Convention Management Co., Box 159, Libertyville, Ill. 60048; (312) 362-8711.

Fifth Annual Assembly Technology Expo, Oct. 16–18. O'Hare Expo Center, Rosemont, Ill. Richard Lewis, Assembly Technology Expo, 2400 East Devon Ave., Suite 205, Des Plaines, Ill. 60018; (312) 299-3131.

Maecon/84, Oct. 16–18. Cervantes Convention Center, St. Louis, Mo. Ohmcom/Maecon, PO Box 699, Utica, Miss. 48087; (313) 731-4551.

Nepcon Northwest, Oct. 16–18. San Mateo Exposition Center, San Mateo, Calif. Jerry Carter, Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

International Test Conference 1984, Oct. 16–19. Franklin Plaza Hotel, Philadelphia, Pa. Harry Hayman, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

Unix Expo, Oct. 16–18. Sheraton Centre Hotel, New York, N.Y. National Expositions Co., Inc., 14 West 40th St., New York, N.Y. 10018; (212) 391-9111.

1984 Conference on Electrical Insulation and Dielectric Phenomena, Oct. 21–24. Wilmington Hilton Hotel, Calyton, Del. Steven Boggs, Ontario Hydro Research, 800 Kipling Ave., Toronto, Canada M8Z 665; (416) 231-4111, ext. 6735.

Convergence '84, Oct. 22–24. Hyatt Regency Hotel, Dearborn, Mich. Bruce McCristal, General Motors Corp., 10-263 General Motors Bldg., Detroit, Mich. 48202; (313) 556-2025.

International Symposium for Testing and Failure Analysis (ISTFA), Oct. 22–26. Los Angeles Airport Hilton, Los Angeles, Calif. Doug McCormac, ISTFA, PO Box 4110, Torrance, Calif. 95010; (213) 217-4310.

ISA '84, Oct. 22–25. Houston Astrohall, Houston, Texas. Elinor Munsch, 67 Alexander Drive, PO Box 12277, Research Triangle Park, N.C. 27709; (919) 549-8411.

The International Telemetering Conference (ITC), Oct. 22–25. Riviera Hotel, Las Vegas, Nev. Michael D. Lloyd, The Judith-Michaels Agency, 1108 Celis St., San Fernando, Calif. 91340; (818) 365-6986.

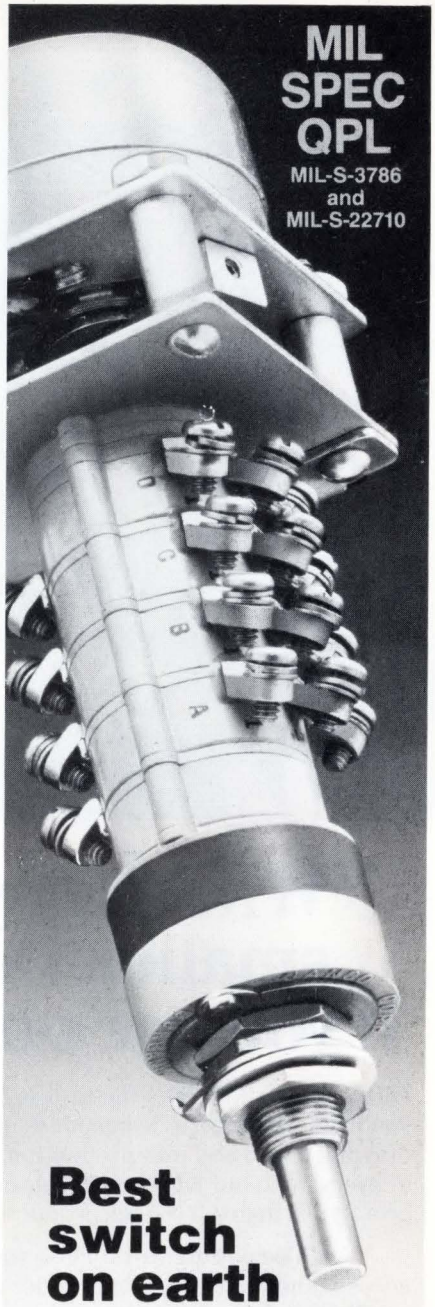
Indycon '84, Oct. 23–24. Indiana Convention Center and Hoosier Dome, Indianapolis, Ind. Elise Ogden, H. V. "Hank" Oakwood, 5160 E. 65th St., Suite A, Indianapolis, Ind. 46220; (317) 842-3024.

Fourth Annual International Electronics Packaging Conference, Oct. 29–31. Omni International Hotel, Baltimore, Md. Evelyn Ashman, IEPS, PO Box 333, Glen Ellyn, Ill. 60137; (312) 260-1044.

The Third Annual Pacific Northwest Computer Graphics Conference, Oct. 29–30. Hult Center for the Performing Arts and Eugene Conference Center, Hilton Hotel, Eugene, Ore. Third Annual Pacific Northwest Computer Graphics Conference, Continuation Center, 333 Oregon Hall, University of Oregon, Eugene, Ore. 97403; (503) 686-4231.

Wescon '84, Oct. 30–Nov. 2. Anaheim Convention Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

(continued on p. 25)



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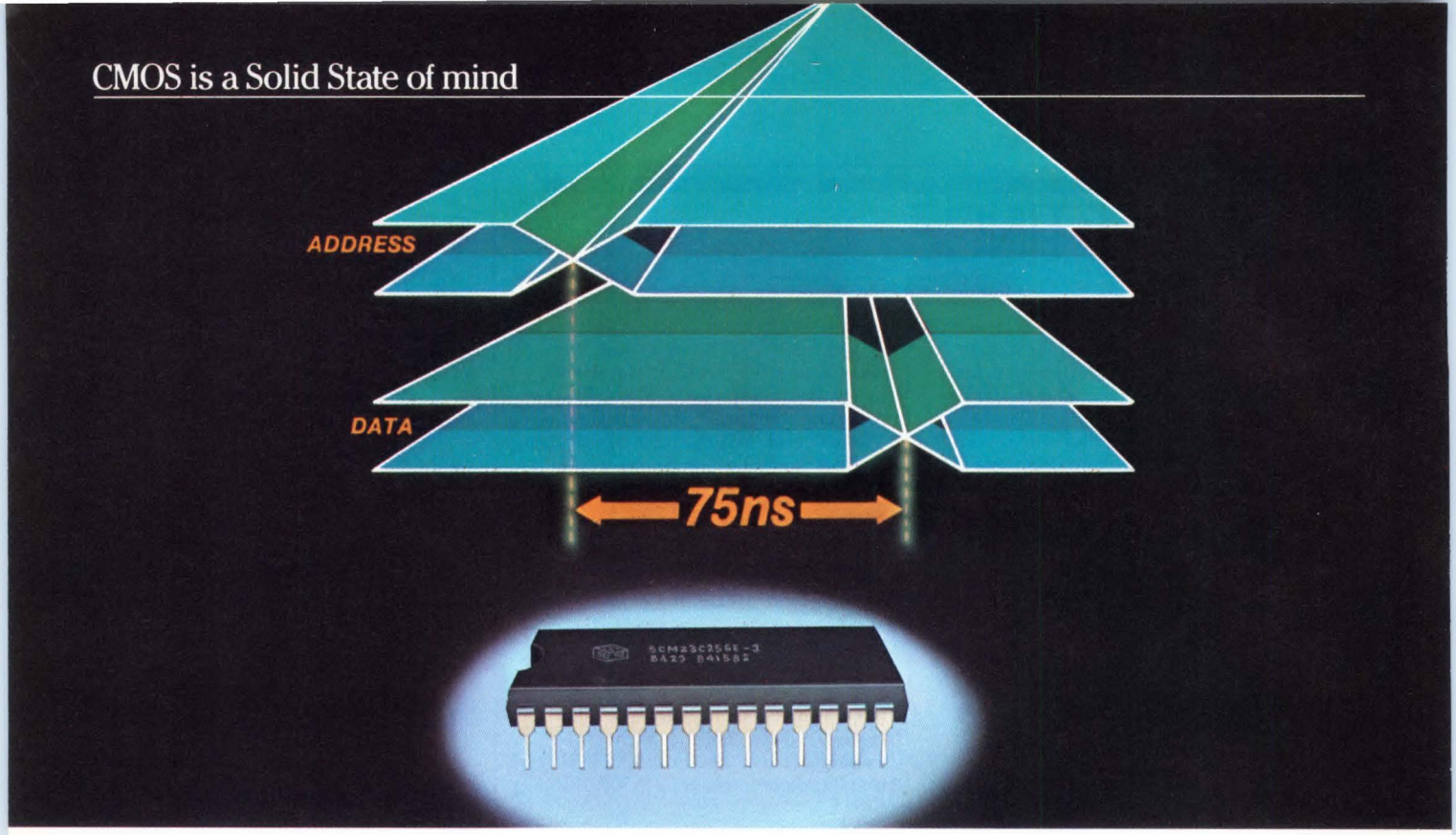
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CIRCLE 13

U.S. MEETINGS

(continued from p. 23)

Intellec '84, Nov. 4–7. New Orleans Hilton Hotel, New Orleans, La. R. R. Garreau, AT&T Technology Systems, Gateway II, Room 1806, Newark, N.J. 07102; (201) 468-5493.

Lasers in Graphics, Nov. 4–8. Hyatt Regency, New Orleans, La. Dunn Technology Inc., 749 E. Vista Way, Vista, Calif. 92083; (619) 758-9460.

The Second International Congress on Advances in Non-Impact Printing Technologies, Nov. 4–8. Stouffer's Concourse Hotel, Arlington, Va. Robert H. Wood, SPSE, 7003 Kilworth Lane, Springield, Va. 22151.

Autotestcon '84, Nov. 5–7. Washington, D.C. Autotestcon, 1725 Jefferson Davis Highway, Suite 704, Arlington, Va. 22202.

Federal Office Automation Conference, Nov. 6–8. Washington Convention Center, Washington, D.C. Federal Office Automation Conference, PO Box 322, Wayland, Mass. 01788; (617) 358-5301.

Government Microcircuit Applications Conference (GOMAC '84), Nov. 6–8. Riviera Hotel, Las Vegas, Nev. John Bart, Rome Air Development Center/RB, Griffiss AFB, N.Y. 13441; (315) 330-3064.

International Conference on Computer-Aided Design (ICCAD '84), Nov. 12–15. Santa Clara, Calif. John Domiter, AT&T, Room 4K523, Holmdel, N.J. 07733; (201) 949-6675.

Automation '84, Nov. 13–14. Stanford Holiday Inn, Palo Alto, Calif. Lori Savate, Semi, 625 Ellis St., Suite 212, Mountain View, Calif. 94043; (415) 964-5111.

Interface I, Nov. 13–15. Conrad Hilton Hotel, Chicago, Ill. Marie Curcio, American Production and Inventory Control Society, 500 W. Annandale Road, Falls Church, Va. 22046; (703) 237-8344.

Power Conversion Products Council International (PCPCI), Nov. 13–14. Sheraton International, O'Hare, Rosemont, Ill. Betsy Bevington, PCPCI, Box 637, Libertyville, Ill 60048; (312) 362-3201.

Fallcon '84, Nov. 14–15. Stouffer's Five Seasons Hotel, Cedar Rapids, Iowa. H. L. Jim Hanson, IEEE, Cedar Rapids Section, PO Box 451, Marion, Iowa 52302; (319) 395-3505.

Comdex/Fall, Nov. 14–18. Las Vegas, Nev. Peter Young, The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

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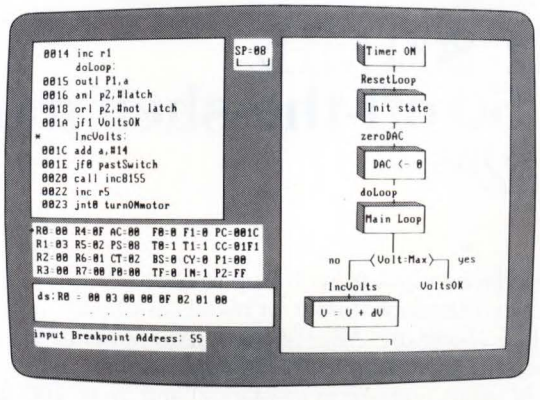
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PERSONALLY SPEAKING



32-bit systems take on a host of functions, playing catch the VAX

Even as 32-bit chip families compete for the attention of system designers, another battle is shaping up, this time among the new systems being designed with the latest off-the-shelf processors. Although they may differ widely in looks and in applications, they have one common goal—to approach the performance of the popular VAX family. Thus engineering workstations, sophisticated CAD tools, and some personal computers are all incorporating features with that end in mind.

Systems designed with 32-bit chips such as the 32032 and the 68020 are able to handle multiple users or multiprocessing, consequently adding traditional minicomputer functions like memory management and protection. Their operating systems are protected as well, reducing the possibility of the systems going down. One shining example is the recently introduced 32-bit computer from Sequent Computer Systems Inc. (Portland, Ore.). It shares its load among up to 12 architecturally identical processors.

In another area, the new processor chips are making fault-tolerant computers much more prevalent. Further, although the ability to execute floating-point arithmetic was available at 16 bits, its true value will become apparent with the wider data buses—and faster data transfers—of 32-bit CPUs. Equally important, virtual memory—already available for 16-bit processors—will become absolutely necessary for 32-bit systems to handle their inherently larger programs.

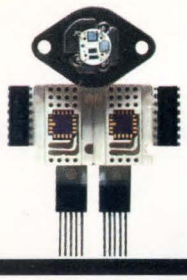
Another reason behind the move to systems built with standard processors is that such chips can be produced at dramatically lower costs than many of the older minicomputers. Those still rely on bit-slice processors, custom chips, or multiple boards to accomplish floating-point processing and memory management. The difference in cost could widen further as the semiconductor manufacturers go into large-volume production on their processor families. Unbelievably, some estimates see 32-bit engineering workstations sporting bargain-basement price tags of between $8000 and $12,000. In comparison, minicomputers go for $100,000 or more. To force costs even lower, semiconductor manufacturers are gearing up to offer board-level subsystems.

The plunging price of VAX-like machines is only part of the story: Incredibly, system designers are now asking for more advanced 32-bit processors. These devices are already on the drawing boards and will boast higher processing speeds, increased integration, and—with CMOS's help—lower power consumption than their predecessors.

The ultimate aim remains unchanged: Create a multiprocessor system by 1987 that matches the performance of the recently introduced VAX 11/785. To keep things interesting, Digital Equipment is already working on more powerful versions of its VAX based on proprietary 32-bit chips. To catch up, system designers will have to be pretty fast on their feet—they're chasing a moving target.

Martin Gold

Martin Gold

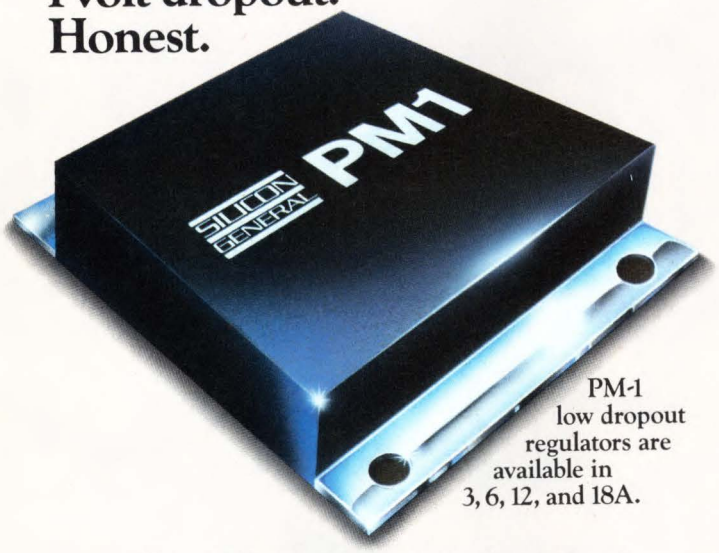


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Imagine getting 5V of clean power from a regulator that requires only 5.2 to 6.0V input. That approaches the theoretical.

Such high performance makes these products ideally suited for any high rel, low noise application; for example, instrumentation, telecommunications, mass memory, portable battery-operated equipment, analog I/O and microprocessor/interface applications.

An entire product family.

Our PM-1 regulator family covers a fairly broad range of standard currents and voltages.

Products are available in 3, 6, 12, and 18A. And in standard voltages of 5, 12, 15, 18, and 24V.

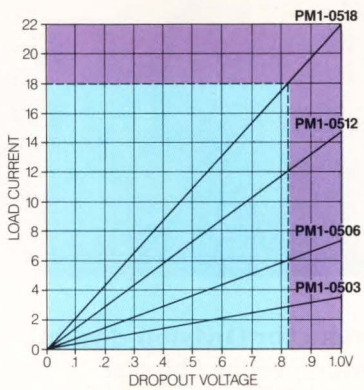
That's 20 standard products right there.

We also do customs and specials. We'll design you a product from 1A to 18A and with voltage ratings between 1.2 and 24V.

A few more interesting specs.

These regulators come with three standard terminals, plus two additional pins used for remote sensing.

The thermally efficient modular package is designed to bolt directly onto the user's heat sink or PC board. It's completely self-contained and includes an output power stage, built in current limiting and associated control electronics.



DROPOUT CHARACTERISTICS

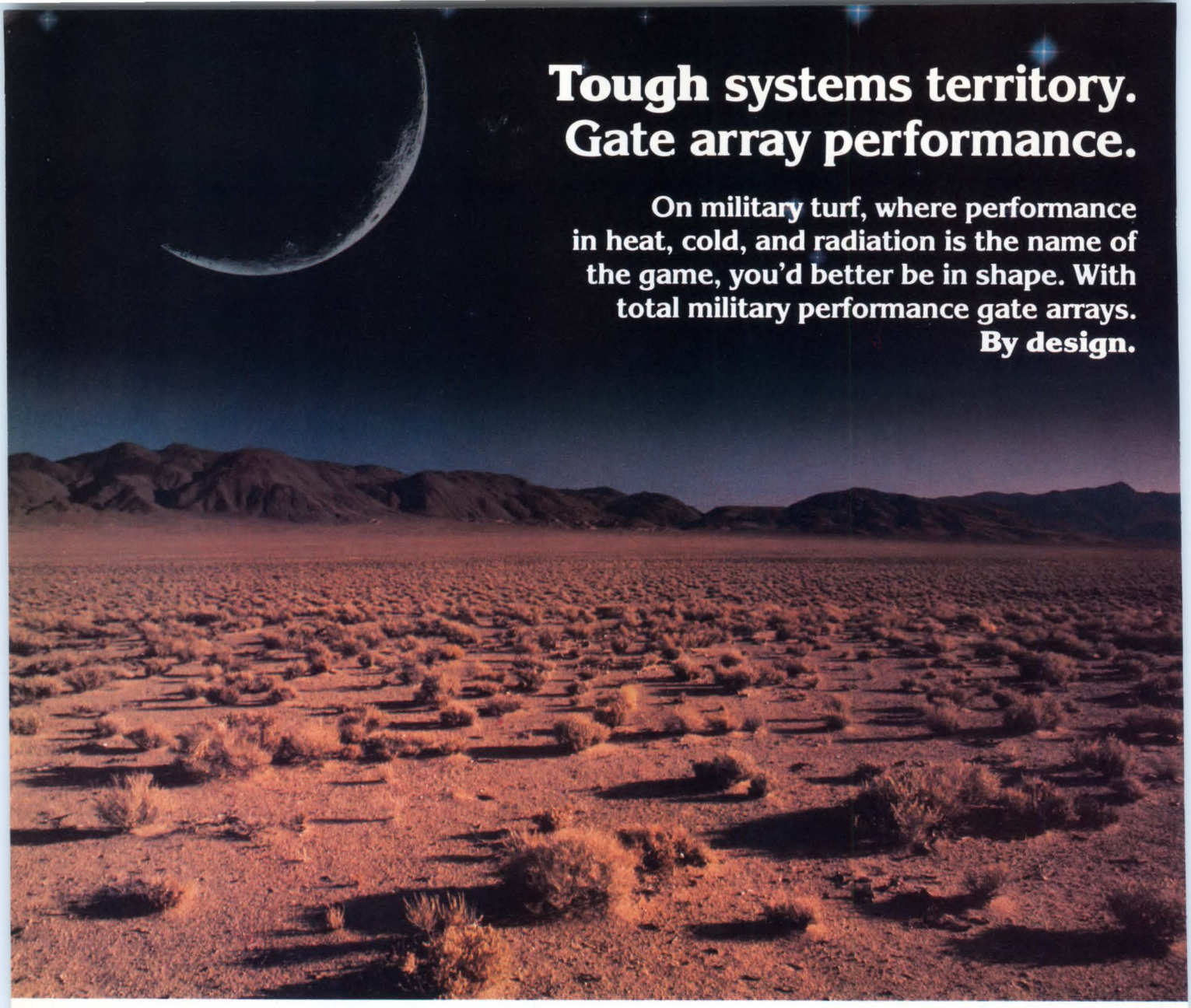
For more than 10 years Silicon General has been the innovator in power control IC design. We've made our mark with supervisory circuits, motor drives, PWM's, linear voltage regulators and power op amps. As you can see, with our new family of ultra-high-efficiency regulators we still haven't lost our touch.

For details, send in the bingo. For specific questions, call Dan Loyer at Silicon General, Power Products Group, 940 Detroit Avenue, Concord, CA 94518. (415) 686-6660. TWX: 910-481-9477.

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CIRCLE 17



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☐ **Credentials:** Trident II, Milstar, F-111, F-15, F-16, F-18, B-1, SICBM, JTIDS, AIM-7M, Patriot, ALQ 135 and other programs.

☐ **Advanced technology:** Five array densities from 800 to 2400 gates. Efficient Integrated Schottky Logic (ISL) bipolar technology. 2.3nS, 350μW (typ) gate performance . . . for 0.8pJ speed-power product. Selective enhancement to 1.8nS.

☐ **Call Raytheon Semiconductor Division:** Specifications, application notes, technical and cost proposal for your application. **415/966-7716.**

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Access to the Right Technology

CIRCLE 18

NEWSPULSE

Accelerator and workstation break simulation record

A test that simulated the equivalent of 292,000 two-input NAND gates proved to be the largest benchmark test ever run on a workstation, with that machine capturing the schematic and uploading the resulting net list. The entire test took just 10 minutes, with a hardware accelerator spending only 17 seconds of that actually simulating the circuitry. Conducted at Westinghouse Co.'s Defense Electronic Center (Baltimore, Md.), the test teamed up the Model 2000 workstation from CAE Systems Inc. (Sunnyvale, Calif.) with the LE 1008 data-flow hardware accelerator from Zycad Corp. (Arden Hills, Minn.). Aside from the 17 seconds, the remaining time was given to uploading the net list to the accelerator and downloading the simulation results to the workstation.

SPICE models MOSFETs, minimizing breadboard testing

Precise SPICE models of power MOSFETs will simplify the design of switching-power supplies and power-control circuits containing these high-speed transistors, thereby shortening the prototyping cycle. In the past, the models could only emulate low-power units (up to 1 or 2 W). The new models, developed by RCA Corp.'s Solid State Division (Mountain Top, Pa.), will handle units of any size or power rating. To represent the MOSFETs in a circuit, a designer will only have to enter data-sheet specifications or a few simple measurements into the model.

Connectorless tapping cuts fiber-optic bus losses

Tapping an optical-fiber bus directly rather than through connectors and couplers reduces excess losses from about 3 dB to less than 0.2 dB. Direct tapping was accomplished by chemically stripping two plastic-clad silica fibers with 200-μm diameter cores and twisting the fibers together. To ensure maximum coupling, the optical power output of the fibers was monitored while the fibers were being twisted. Afterward, the fibers were reclad and joined with epoxy. Scientists at Bell Communications Research Inc. (Murray Hill, N.J.) developed the technique, successfully testing it on a multimode fiber with 5 dB/km of attenuation and a bandwidth of 20 MHz-km.

IBM tips scales in favor of Virtual Device Interface

VDI, which is currently being considered by ANSI as an industry standard for personal computer graphics software, got a big boost when IBM Corp. (Armonk, N.Y.) endorsed its use for personal computers with medium- and high-resolution screens. A standard driver would simplify the job of application program developers, who would no longer have to produce different versions of their products for each kind of computer and CRT. The Virtual Device Interface, developed by Graphic Software Systems Inc. (Wilsonville, Ore.) is a simplified version of the powerful Graphical Kernel System (GKS) and works like an operating system for graphics. Already widely used, it is one step closer to being the de facto industry standard as a result of IBM's support.

NEWSPULSE

212A modem chip packs more funtions on board

One of the most complete 212A modem chips has a switched-capacitor modulator and a digital coherent demodulator, as well as switched-capacitor filters. The on-chip filters isolate channels, shape spectrums, and equalize the signals in high- and low-speed modes. Additionally, the receiver filter can operate as the front end for a smart dialer. Now in the final stages of development at the Linear Division of Fairchild Corp. (Mountain View, Calif.), the modem operates at a full 1200 or 300 bits/s, as set by the Bell 212A standard. The modem needs only a microcontroller and a line interface circuit. The CMOS modem will draw just 75mW when powered by ± 5V.

Software package tracks pc boards' service history

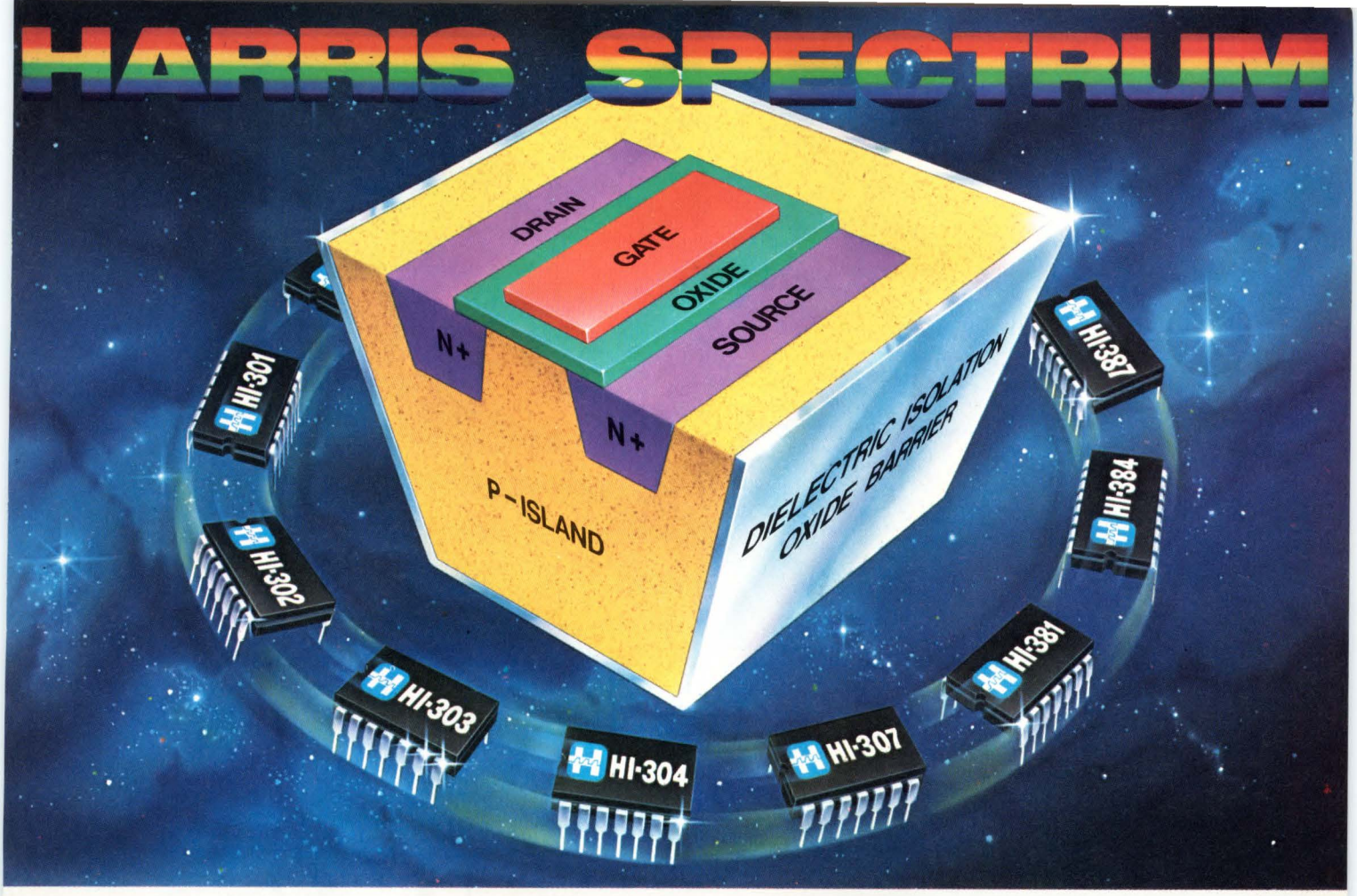
Manufacturers of printed circuit boards have long been plagued by hidden inventories that loop endlessly between testing and repair stations. Fortunately, forthcoming software promises to keep track of those boards, linking repair data to a relational data base that records a board's chronological failure and repair history. In fact, the package, created by Zehntel Inc. (Walnut Creek, Calif.), compares tester-generated diagnostic information with the action taken at the repair station, alerting service personnel to discrepancies between the test and the remedy. Dubbed IRIS, for Integrated Rework Information System, the software will be unveiled at the International Test Conference, Oct. 16–19 in Philadelphia.

MAP controllers link wide μP buses

Factory networking takes another step toward reality with the announcement of the first token-passing bus controller chips to conform to the Manufacturing Automation Protocol, conceived by General Motors Corp. (Detroit). The chips, which are expected to be sampled sometime next year, will allow all popular 8- and 16-bit microprocessor buses to communicate. Further, they will be able to handle both MSB- and LSB-first transmissions. The controllers are the work of Motorola Semiconductor Products Inc. (Phoenix, Ariz.) and Concord Data Systems Inc. (Waltham, Mass.). Motorola's version is also being designed to work with its 32-bit microprocessor, the 68020.

Alternative-source pact leads to standard-cell library

System designers will soon be able to draw on a broad CMOS standard-cell library of 3-μm—and eventually 2.3-μm—SSI and MSI chips, following a recent alternative-source agreement among Texas Insturments Inc. (Dallas), Philips Export BV (Eindhoven, the Netherlands), and Signetics Corp. (Sunnyvale, Calif.). According to the pact, TI will contribute 150 SSI, MSI, and I/O cells, whereas Signetics and its parent Philips will contribute 40 complex MSI cells. At the 2.3-μm level, Philips and Signetics will prepare an additional 80 MSI cells. The library's cells will be compatible with design-automation systems from Daisy, Mentor, FutureNet, P-CAD and Valid Logic.



Harris CMOS Precision Analog Switches:

the dielectric difference.

Astute specifiers of the precision 30X/38X switch series—the industry standard—are turning on to the advantages of Harris CMOS Analog 30X/38X Switches.

They know that only Harris CMOS Analog Switches are fabricated by the exclusive Harris Dielectric Isolation (DI) process that results in highest performance:

- The lowest leakage current: 40 pA
- The lowest charge injection: 3 mV
- The lowest ON resistance: 35 ohms
- A standard maximum power supply voltage of 44 V

Harris 30X/38X Analog Switches are available in 12 pin-compatible models to replace whatever precision to general-purpose device you're now using in your military and industrial applications.

The switch is to superior Harris CMOS technology.

Get it on!

CIRCLE 19

Harris 30X/38X Product Summary

FUNCTION	DEVICE	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$(NA) (TYP)	$t_{(ON)}$(NS) (TYP)	$t_{(OFF)}$(NS) (TYP)	P_D(mW) (TYP)
2 x SPST	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1

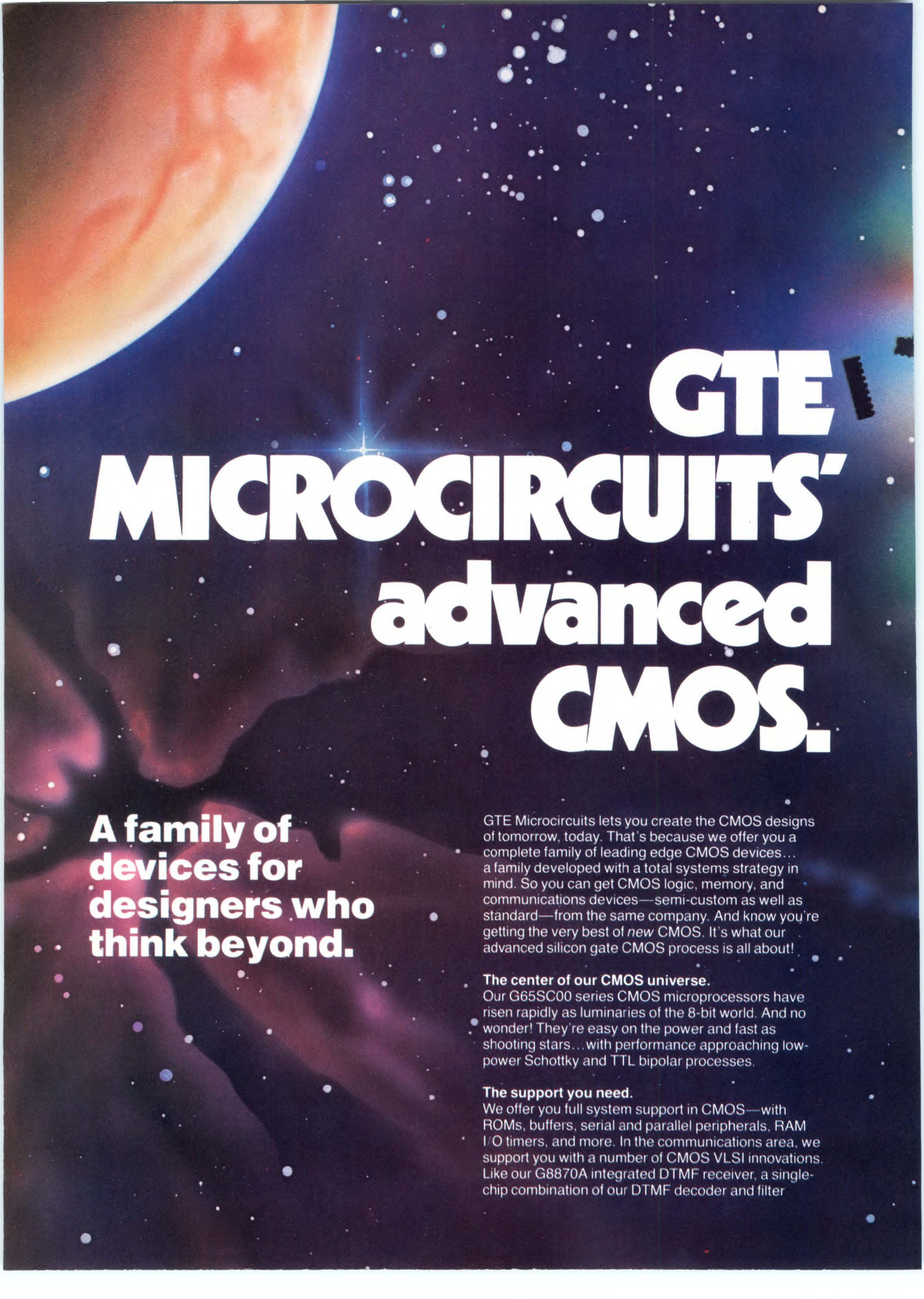
For your information, our name is Harris.

For more information, write: Harris Semiconductor Analog Products Division, P. O. Box 883, MS 53-035, Melbourne, Florida 32902-0883.

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HARRIS



A family of devices for designers who think beyond.

GTE Microcircuits lets you create the CMOS designs of tomorrow, today. That's because we offer you a complete family of leading edge CMOS devices... a family developed with a total systems strategy in mind. So you can get CMOS logic, memory, and communications devices—semi-custom as well as standard—from the same company. And know you're getting the very best of *new* CMOS. It's what our advanced silicon gate CMOS process is all about!

The center of our CMOS universe.
Our G65SC00 series CMOS microprocessors have risen rapidly as luminaries of the 8-bit world. And no wonder! They're easy on the power and fast as shooting stars...with performance approaching low-power Schottky and TTL bipolar processes.

The support you need.
We offer you full system support in CMOS—with ROMs, buffers, serial and parallel peripherals, RAM I/O timers, and more. In the communications area, we support you with a number of CMOS VLSI innovations. Like our G8870A integrated DTMF receiver, a single-chip combination of our DTMF decoder and filter



devices. Or our G65SC150 communications terminal unit: an 8-bit CPU, ROM, RAM, timer, I/O and sine wave generator…all on a single chip!

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Want to personalize your design with semi-custom? No problem. Our G50000 series gate arrays let you convert the most complex SSI/MSI logic into a single IC with up to 2,500 gate-equivalent functions. And, thanks to our state-of-the-art Automated Logic Integration System (ALIS), you'll get super fast turnaround on our semi-custom devices. They're all implemented in our leading edge silicon gate CMOS process—a process also available to you through our customer-furnished tooling program.

Your CMOS master source.
We're already galaxies ahead in CMOS. And it's only the start. In the future we'll be announcing several new CMOS products…like a 16-bit microprocessor, LAN controller, Codec combo, and more. As a major force in advanced CMOS, we've established ourselves among the ranks of the major semiconductor companies in the marketplace…with a full commitment to meeting your present and future needs for leading edge products.

Launch your all-CMOS design today!
For complete information about our advanced CMOS family, write us on your letterhead. If you can't wait to blast off, call us right away. GTE Microcircuits, Marketing Services, 2000 West 14th Street, Tempe, AZ 85281, Tel: (602) 968-4431, TWX: 910-951-1383. For the name of your nearest GTE Microcircuits distributor, call: WEST—(714) 855-9901; CENTRAL—(312) 259-1112; EAST—(516) 724-8300; EUROPE (Munich, W. Germany)—Tel: 089/1 78 20 31, TLX 528452 GTEMC D.

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CIRCLE 20

DISPELLING THE MYTH ABOUT SINGLE CHIP MICROCOMPUTERS.

This is the first in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.



Single chip microcomputers are marvels of advanced electronic technology. Going beyond even the tiny architectures of today's general-purpose microprocessors, they combine the functions of multiple chips to form a single-device solution. Indeed, they are awesome machines.

But after their introduction, myths grew up around MCU's. Designers believed that they were difficult to design with; that there wasn't sufficient hardware and software support for them; that those who selected them would get a Sisyphus Complex. Sisyphus, you remember, is the character in ancient Greek mythology who was condemned forever to push a rock up a hill. Just as the rock reached the top, it escaped Sisyphus and rolled back to the bottom.

Some MCU's, no doubt, deserve the stigma of this myth. But one definitely does not. Zilog's Z8® MCU Family. For there is more than enough evidence to prove that the Z8 chip is not only the fastest MCU around, but it's the easiest to work with, too. In fact, it should be the chip of choice for any dedicated control applications that must get to market on time—even if you need large quantities of them to fill your needs. Because the Z8 device is available now for off-the-shelf delivery.

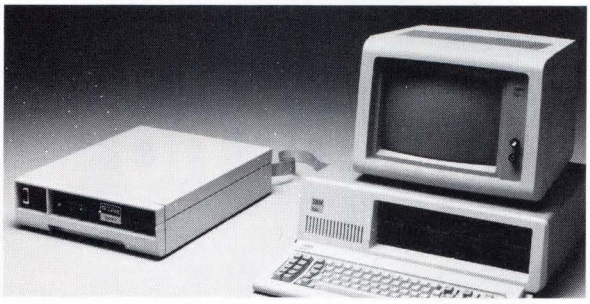
But what does ease of design mean to you? What do you look for when you select a chip? What do you need to make your job easier? Whatever it is, you'll find Zilog provides everything you need, and more:

- Hardware and software development tools
- An existing software base
- Factory and field sales support
- Preproduction parts supplies

Z-SCAN™ 8 PROVIDES REAL-TIME EMULATION CAPABILITIES.

Zilog's Z-SCAN 8 is an in-circuit Emulator with a combination of hardware and sophisticated software that gives you efficient, interactive emulation of the entire family of Z8 microcomputers. By the simple exchange of target devices, the selected Z8 MCU can be emulated in a real-time mode that gives you the ability to inspect and control the

tested environment. It also gives you real-time trace speed up to 12 MHz, two breakpoints, single-step capability and extensive mappable memory. All to ensure that you get an accurate simulation of your Z8 operating environment.



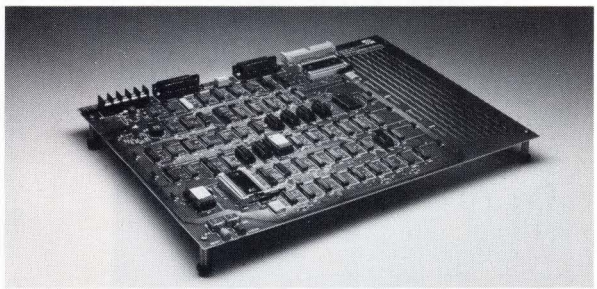
The Z-SCAN 8 Emulator is a combination of hardware and firmware that allows efficient, interactive emulation of the Z8 MCU. When hooked to an IBM PC software host, Z-SCAN 8 provides real-time, in-circuit development system capabilities. The Z-SCAN 8 will connect easily to other PC's making it a highly versatile unit.

The Z-SCAN 8 operates with both Zilog systems and other 8-bit development systems running CP/M® and/or other operating systems. Its standard RS-232 serial link makes it particularly useful with the IBM PC and other CRT terminals. Hardware and software debugging is fast and convenient. Two screens display the status of the Z-SCAN 8 monitor and Z8 MCU target resources. Target memory can be displayed and modified in a scrollable window. Moreover, the Z-SCAN 8 is interactive and easy to use. Commands are selected from menus and command arguments are self-prompting.

The set-up procedure and initialization for the Z-SCAN 8 is done for you—a unique feature in itself. The Z-SCAN 8 is designed to reduce design time. But it's not the only time-saving device Zilog provides for the Z8 MCU.

THE Z8 MCU DEVELOPMENT MODULE CUTS HARDWARE AND SOFTWARE DEVELOPMENT TIME.

The Z8 Development Module (DM) features two 4K Z8 devices on a single-board microcomputer. It's designed to assist you in the development and evaluation of hardware and software designs based on the Z8 MCU. With it, you can easily build a prototype using the Z8 prototyping device, and then develop code that will eventually be mask-programmed onto the Z8 on-chip ROM.



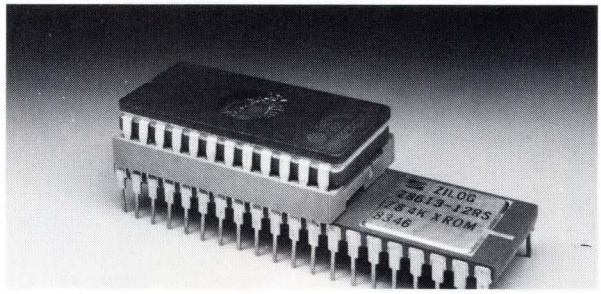
The Z8 Development Module allows you to build a prototype using the Z8 prototyping device, thereby developing code that will eventually be mask-programmed into the Z8 on-chip ROM. The Module is a single-board microcomputer system designed to develop and evaluate hardware and software designs based on the Z8 family.

The Development Module connects to the CRT terminal and host system through two on-board RS-232 serial ports. So the DM fits between the CRT and host. A simple command makes the DM transparent in the serial path, which allows software to be developed on the host-resident assembler without disconnecting the DM from the CRT and host.

The DM has a range of features to make Z8 designs easier than you ever thought possible: • 4096 bytes of static RAM for convenient creation and debugging of user code; • an on-board socket that tests user code in a 2716 or 2732 EPROM; • up to 4096 hardware breakpoints on address compare that can cover the entire internal ROM space; • a wire wrapped area for prototyping; and much more.

Z8 MCU DEVELOPMENT SOFTWARE SPEEDS UP DESIGN TIME.

Zilog also provides you with a growing library of sample programs and convenient assembler packages to help you get started testing your Z8 MCU designs. In our Subroutine Library, for example, there's our arithmetic subroutine, an I/O subroutine and a general control subroutine. What's more, there are several versions of the Z8 device: a 2K and 4K ROM version; a ROMless version; and a Protopak for prototyping. Each offers different memory addressing structures. Zilog is developing more all the time. Plus, there's an existing software base for all the Z8 MCU's. We can provide you with samples of designs currently in use.



The Z8613 MPE is used for prototype development and preproduction of mask-programmed applications. The Protopack is a ROMless version of the standard Z8611, housed in a pin-compatible 40-pin package.

SERVICE AND SUPPORT AT EVERY LEVEL FOR YOUR Z8 MCU DESIGNS

From the factory to the field, Zilog provides support at every level. A worldwide field sales network stands ready to help you with both hardware and software support. And you can get all the Z8 MCU's you need right now. Yields for the device are up 40%, and price reductions reflect our new supplies. What's more the upcoming Z8 Super 8™ promises a smooth migration path for today's Z8 MCU family.

Zilog's Z8 single chip microcomputer. Believe the myths. Or get the facts. If bringing your product to market is important to your business, then design with the part that does more for success than any other. The Z8 MCU makes getting over the design hill and into production a lot easier than you might think.

For more on the Z8 MCU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call (408) 370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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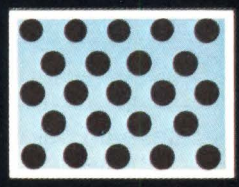
CIRCLE 101

TEK 4115B COMPUTER DISPLAY TERMINAL

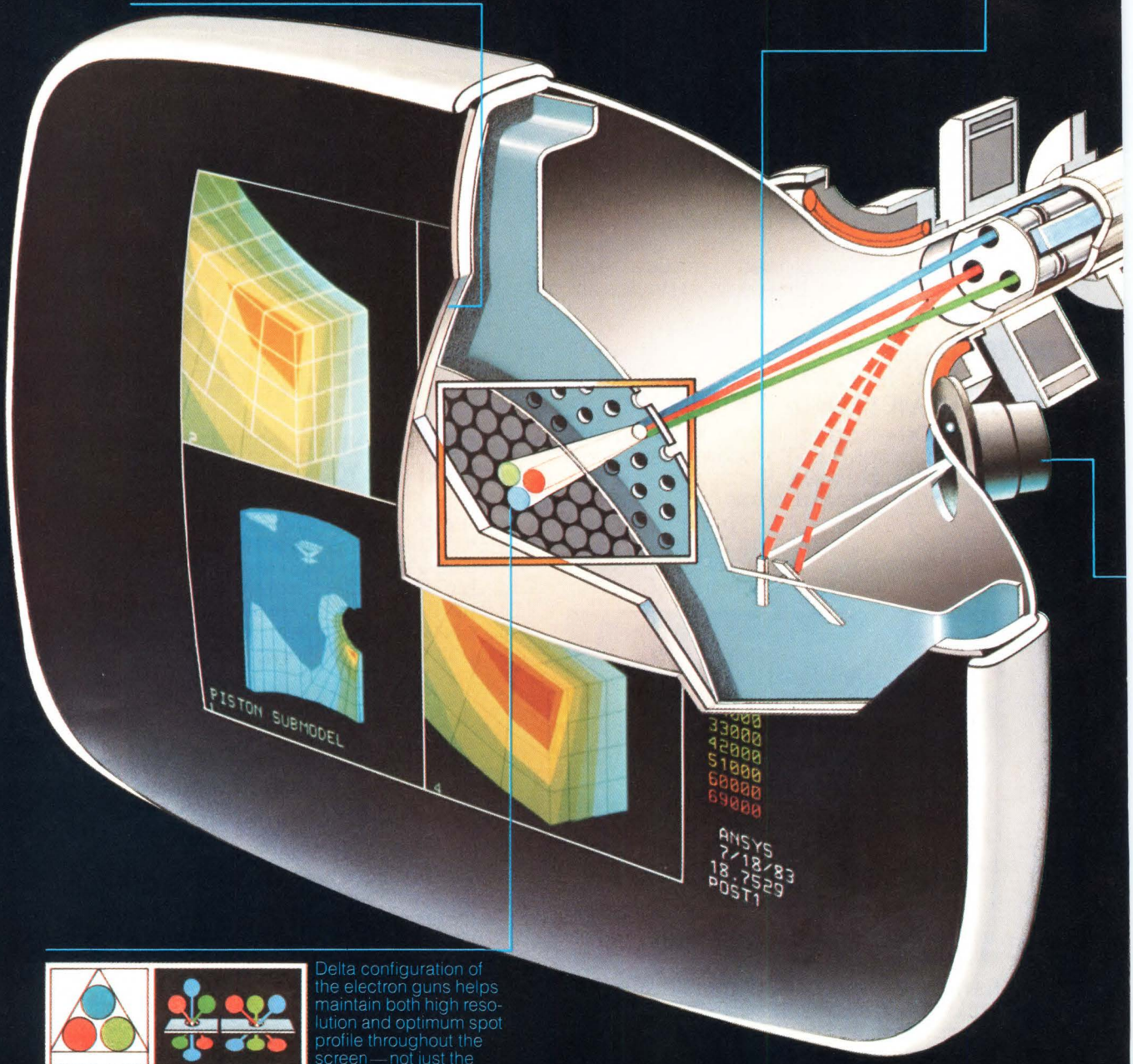
Who solves the misconvergence problems no one else will talk about?



An aluminum layer between the shadow mask and the screen reflects light from the phosphor dots out toward the viewer and at the same time prevents errant screen light from reaching the photodetector.



The 4115B's patented AutoConvergence is accomplished by applying non-parallel indexing phosphors at precise angles and positions at the rear of the CRT shadow mask, detail at left.



Delta configuration of the electron guns helps maintain both high resolution and optimum spot profile throughout the screen—not just the center.

*Display courtesy of Swanson Analysis Systems, Inc. Copyright © 1984, Tektronix, Inc. All rights reserved. GST-355

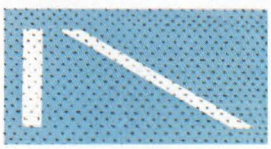
Tektronix.

The higher the visual resolution of a color display, the more difficult it becomes to converge the color beams at a precise point.

Yet, without precise control of convergence, productivity gains promised by high resolution graphics simply can't be realized.

That's why Tek designed the 4115B with AutoConvergence as our engineering prerequisite.

The engineering work environment is tough on high resolution displays. A shift in display angle for better viewing. Mild vibration from a stray elbow. Minor temperature change. Circuit drift. Tube aging. The earth's magnetic field.



A photodetector picks up light from the indexing phosphors. A microcomputer then compares instantaneous beam positions with factory specifications. Convergence corrections are generated to make the two coincide.

They all can cause the color line blurring effects commonly called *misconvergence*.

Loss of detailed information, especially in corners. Fuzzy, fringed colors. And visual ambiguity. All of which can lead to user fatigue, error and loss of productivity.

Until the 4115B, manual reconvergence was typically up to an hour-long task for a service technician—resulting in even more lost time.

No wonder most display manufacturers won't talk about the problem. But Tek will. Because we solved it with our exclusive AutoConvergence.

Push one button on the 4115B and all three electron guns are converged automatically. In 20 seconds. Not just in the screen center but from corner to corner.

Convergence accuracy is within .25mm, as compared to the 0.3mm to 1.0mm achievable by manual or other techniques. There's no interruption to work, so there's no loss of productivity.

The 4115B's high performance doesn't stop with AutoConvergence. It just begins there. You can apply its 60 Hz noninterlaced, 1280 x 1024 display, 50,000 vector/second redraw speed and user selectable 32-bit coordinate space to optimize productivity on any application.

Large area fills are accomplished at 125 million pixels per second. Standard host communications is 19.2K baud.

So if you want to start with the highest resolution and work at your best all day, every day, call your Tek Sales Engineer. For literature or the location of your local Tek sales office, call toll-free: 1-800-547-1512. In Oregon, 1-800-452-1877.

Call Tek



Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 21

BOB, CAROL, TED & ALICE



How Four Innovative Design Engineers Found Happiness Using The New DASH-1™ Schematic Design System.

BOB: "DASH-1 keeps me under budget and ahead of schedule..."

"DASH-1 has freed my designers from the drudgery of manual schematic design and documentation. Now, we can knock out complex designs in a fraction of the time it used to take. Using the huge DASH-1 parts library (on disk) we can instantly call up any symbols we need — all with pinouts and pin functions. With DASH-1's amazing options, we can generate Net Lists, Lists of Materials, Design Check Reports and other critical documents. I'm a hero in my company now, with productivity at an all-time high."

CAROL: "DASH-1 helped save our CAD Systems..."

"My company has a big investment in large CAD systems. But for a long time I noticed our engineers were frustrated. They'd send in schematic sketches only to get back drawings and documents that were completely different. The poor engineers would spend hours checking, changing and red-lining. DASH-1's family of CAD translators, to front-end all of our large systems, has changed all this. And back annotation is easy. DASH-1 has provided our engineers easy access to those previously difficult-to-use and inaccessible CAD tools."

TED: "Imagine! Simulation right at my desk..."

"I'm even more sold on my DASH-1 with its new simulator. After I complete my schematic, I have a closely coupled logic and fault simulator that I can run at my desk. I can analyze my designs much faster — and put them into production without delay. FutureNet calls it the DASH-1 CADAT.™ I call it a miracle because I can handle designs as large as 10,000 gates right at my desk, and up to 100,000 gates using a FutureNet CAD translator. Thanks to DASH-1, simulating is stimulating!"

ALICE: "DASH-1 keeps growing — as we do..."

"Ours was a start-up company — but it's growing fast. One of our first investments was a DASH-1 (about the price of an IBM PC or XT system) to speed up schematic design and documentation. Since then, FutureNet has added all kinds of low-cost enhancements. Things like CAD translators; direct-connections to most computers; the STRIDES hierarchical package with 99 levels of structured design nesting; the powerful CADAT simulator, pen plotter options, and hot new features, like Rubber Banding, Tag and Drag, and Snap. We're with FutureNet... for now and the future."

FutureNet, DASH-1 and STRIDES are trademarks of FutureNet Corporation. IBM is a registered trademark of the IBM Corporation. CADAT is a trademark of HHB Softron, Inc.
DASH-1 CAD Translators (Partial List): APPLICON, CADAM, CADAT, CALAY, CALMA, CBDS, COMPUTERVISION, GERBER, RACAL-REDAC, SCICARDS, TEGAS.

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Productivity of the Future... today.

CIRCLE 22

NEWSFRONT

32-bit chip set follows 250 instructions, uses static NMOS circuits

Working with NMOS static circuitry lets the instructions of a 32-bit microprocessor be stepped through individually for testing.

The latest 32-bit microprocessor chip set is marked by an impressive quartet of firsts. At 250 members, its instruction set overshadows the 100 to 125 instructions typically run by most of its counterparts. Further, it is the first 32-bit device to go with fully static NMOS circuitry, which enables its clock to operate from dc to 8 MHz and its instructions to be tested.

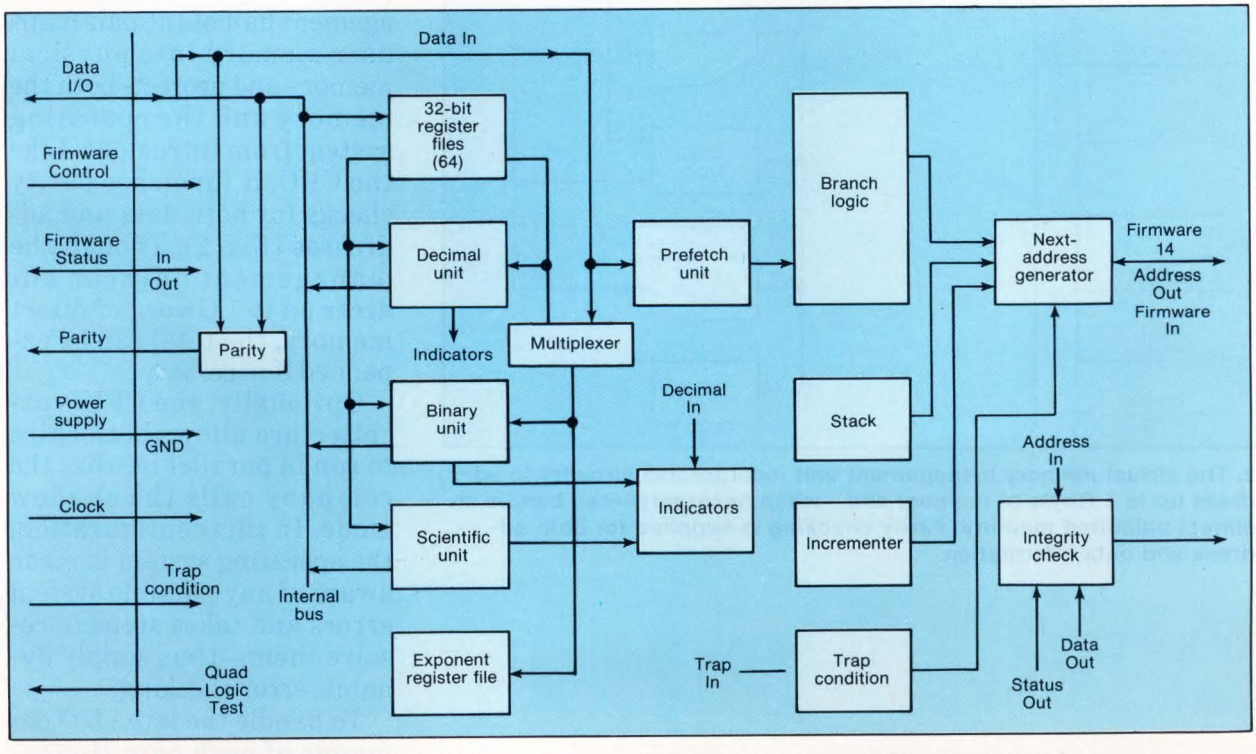
The set also carries its decimal, binary, and arithmetic logic units on chip. Finally, the microprocessor boasts 64 working-register files, each able to store 32 bits.

The chip pair comprises a CPU and a virtual memory management unit. Their architecture is specifically oriented for multiple users.

Gary Elinoff

Putting it together

In assembling the microprocessor set, the Small Systems and Terminal Division of Honeywell Information Systems Inc. (Billerica, Mass.) elected not to include

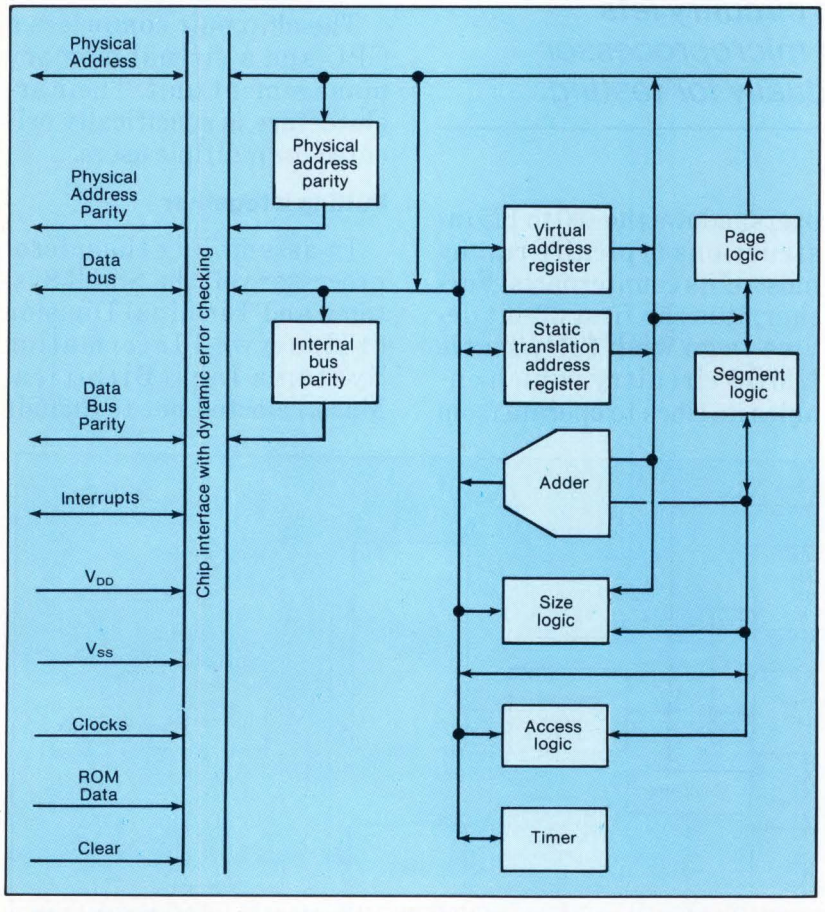


1. Honeywell's 32-bit microprocessor includes a CPU with separate decimal, binary, scientific, and exponential logic units, all working in conjunction with an on-chip multiplexer. Parity checking is done both for transfers between internal registers and for transfers off chip.

control ROM on chip. (Typically, firmware can occupy as much as 85% of a die.) Instead, it used the freed-up real estate to enlarge the instruction set, which includes both diagnostics and Fortran and Cobol instructions that eliminate the need for external compilers.

The chips are fabricated with 2-μm NMOS using arrays of cross-coupled transistors for the logic circuitry, making all of the logic and the registers static. That permits the set to operate from dc up to its maximum clock speed and also allows instructions to be stepped through one at a time for testing and debugging.

Arithmetic instructions are speeded by an on-board hardware-based 64-bit shift register. Also contributing to speed are logic units that handle binary and decimal arithmetic, a scientific unit that performs trigonometric and scientific calculations, and an exponent register file (Fig. 1). All are managed by an on-chip multiplexer.



2. The virtual memory management unit incorporates circuitry to address up to 1 Gbyte of memory and—when necessary—can handle an almost unlimited memory. Parity checking is supplied for both address and data information.

Checking in

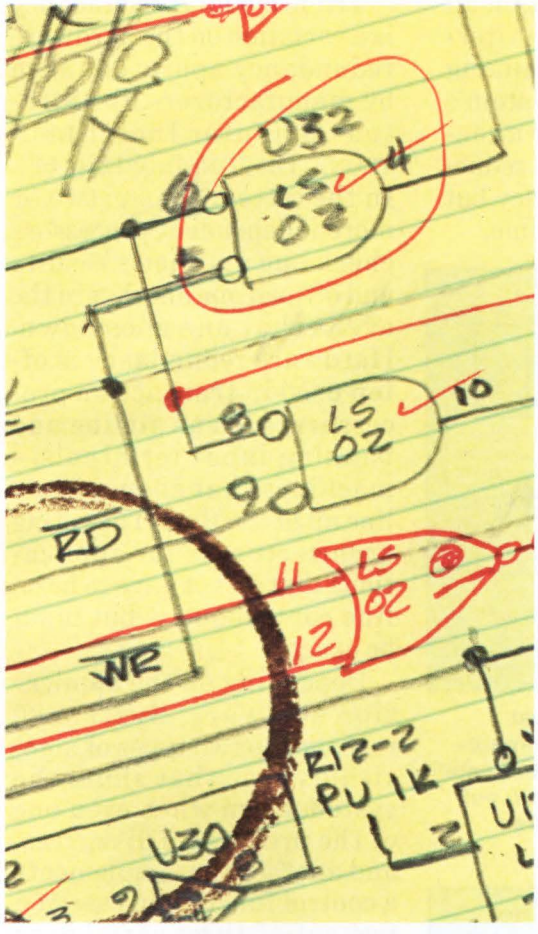
In the I/O portion of the CPU, parity checking is used for transfers within registers on the chip as well as transfers to and from other devices. Of the device's 64 dual-port working registers, over 40 are accessible through software.

The virtual memory management half of the pair maps user memory into physical memory and protects both the memory and the operating system from intrusions. Like the CPU, it furnishes parity checks for both data and addresses (Fig. 2). Though the management unit can address up to 1 Gword of direct memory, the total can be expanded if necessary.

Optionally, the CPU's architecture allows both chips to run in parallel in what the company calls the shadow mode. In this configuration, the operating system is made aware of any possible system errors and takes steps to resolve them—thus supply dynamic error checking.

To handle the large I/O demands of each chip Honeywell houses them in 132-pin grid arrays.

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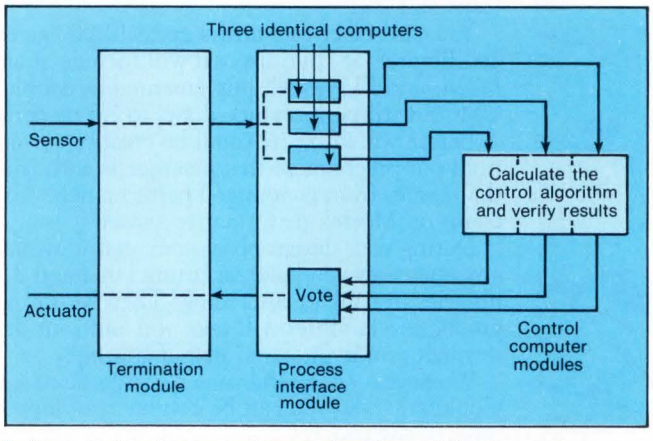
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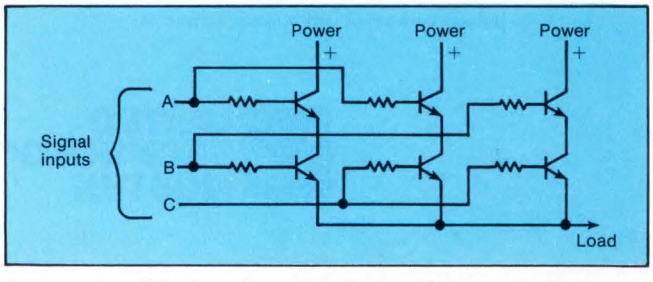
Voting architecture protects industrial process control

A voting architecture for a fault-tolerant computer designed for industrial process control does more than traditional hardware redundancy schemes to ensure the accuracy of control outputs. In the architecture, several independent microprocessors handle identical inputs and compare their results before giving the go-ahead for a control action.

For environments where precision is critical, such as nuclear power, chemical, or gasoline plants, the system can be programmed to shut down unless the outputs of all the processors agree. Alternatively, agreement among the majority of the system's processors can trigger a control output, potentially reducing the system's accuracy but increasing its on-line time.



1. In a redundancy scheme developed by August Systems, three independent process-control computers analyze input data, compare their results, and vote on an outcome. No action is triggered unless two out of three or (with different code) three out of three computers have matching results.



2. In a simplified voting circuit, transistor switches control the circuit paths between the power and the load. At least two of the signal inputs must be valid (two sets of switches must be on) to make one complete signal path.

System 30, from August Systems Inc. (Tigard, Ore.), allows data to be voted on while it is being entered, during computation, and at the end of processing (Fig. 1). Called triple modular redundancy, the architecture is implemented with three identical microcomputers.

Triple modular redundancy is a variation on the hardware redundancy approach taken by manufacturers like Stratus Computer Inc. (ELECTRONIC DESIGN, July 12, p. 62). In the latter scheme, two or more independent processors check one another's results and offload one another in the event that one goes down. Hardware redundancy is often used in transaction processors, such as airline and banking input terminals—machines that should be on line all of the time. The voting architecture is for applications that do not have to be on line continuously, but must be exact.

Depending on the application software, System 30 responds to two types of algorithms: One that shuts the system down when even one of the processors disagrees, and another that implements a control function in case of a two-out-of-three vote. In the latter, repeated discrepancies are reported to the operator as a need for maintenance. Though the voting process may slow the system's response to specific sensor input conditions, it ensures that the response is correct. A similar type of voting architecture, involving five microprocessors, is used on the

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space shuttle.

The majority voting mechanism is analogous to a switching circuit in which two out of three switches must be on to make a complete path, although it may not matter which two switches (Fig. 2).

Like the straightforward hardware redundancy approach, a two-out-of-three voting architecture will make sure the system is usually running. Unlike the hardware redundancy approach, voting algorithms give double or triple protection against errors.

The System 30 chassis includes a motherboard with 3 redundant power supplies, 4 serial ports for communicating with other computers, up to 14 I/O process monitor boards, and 3 separate computer boards—each residing on its own bus. Each control computer board contains an 8086-2 microprocessor and an 8087-2 math processor.

Stephan Ohr

Parallel-processing mainframe gives Unix a new home

A new day has dawned for Unix: The popular operating system can run in real time on a parallel-processing mainframe, thus gaining speed and minimizing context switching to trim overhead. The OS is a version of Unix System III, devised by Denelcor Inc. (Aurora, Colo.) for use with its heterogeneous element processor (HEP).

HEP Unix, as the operating system is known, was completely rewritten from C into the native machine code of its associated mainframe. A third layer was added between the kernel and the shell that make up most Unix systems. Dubbed the supervisor, it links the other two layers and puts unneeded portions of the kernel to rest, picking them up when they are called into play by the user. Since the operating system and the application packages are stored in different memory locations, temporarily dropping a portion of the OS does not interfere with processing.

Helping out the boss

The supervisor also works in conjunction with scheduling hardware to speed throughput. When a task must be stopped to wait for data—say, an I/O search to a disk—the interrupted instructions are transferred to a passive interface. Other tasks are then transferred to the available processor, keeping the processing rate at HEP's full 10 million instructions/s. When the data becomes available, the supervisor and the scheduling module shift the instruction back into the processing cycle.

Further, the revision incorporates the file-sharing portion of the Berkeley 4.2 version of Unix. Despite that addition, the operating system remains compatible with most application packages written for Unix System III.

Since HEP processors always operate at full speed, the system's throughput is much higher than traditional com-

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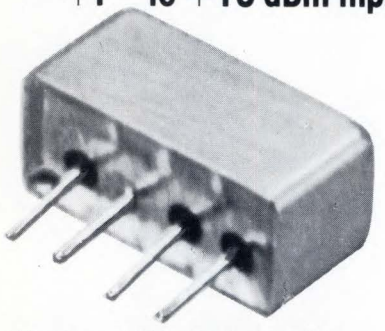
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Spurious Harmonic Output, dB	TYP.	MIN.
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200-600 MHz F1	−25	−20
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puters with similar operating speeds. Also, the mainframe's parallel structure, which processes up to 50 instructions at once, eliminates much of the software overhead required in von Neumann machines.

Because tasks are carried out in parallel, the code for handling interrupts as single-element processors switch between jobs is minimized, as is the time needed to perform these tasks. In fact, rather than the 35% to 40% overhead required for most Unix operating systems, HEP Unix only ties up about 5% of the processor's time and power.

The context switching normally required during changeovers from user to user is performed in parallel with the processing of the data, so throughput is not hampered. The amount of switching also drops, since several tasks can be tackled at once. Finally, the 50 data paths of any processor can be divided among seven assignments. *Terry Costlow*

Serial bus carries multiple-channel or high-speed data

One of the first serial buses that allows a user to choose between more channels and higher bandwidths also conforms to the proposed Integrated Services Digital Network (ISDN) standard. The twisted-pair ST-Bus, from Mitel Corp. (Kanata, Ont., Canada), connects voice-data components, microprocessors, and peripherals and gives a system designer much more flexibility than do traditional buses with fixed numbers of channels and predetermined data rates.

The ST-Bus ties together the company's family of telecommunications chips (ELECTRONIC DESIGN, Aug. 23, p. 303), which meet the specifications of the International Consultative Committee on Telegraphy and Telephony (CCITT). Working with the system, the bus can transmit over as many as 32 multiplexed channels, each operating at 300 bits/s to 64 kbits/s. Each channel carries digital data integrated with toll-grade pulse-code-modulated voice signals.

For high-speed communications, the bus operates over a single channel at 2.048 Mbits/s; alternatively, the system designer can set combinations in between. Regardless of their configuration, the 8-bit-wide channels are governed by a 125-μs clock cycle.

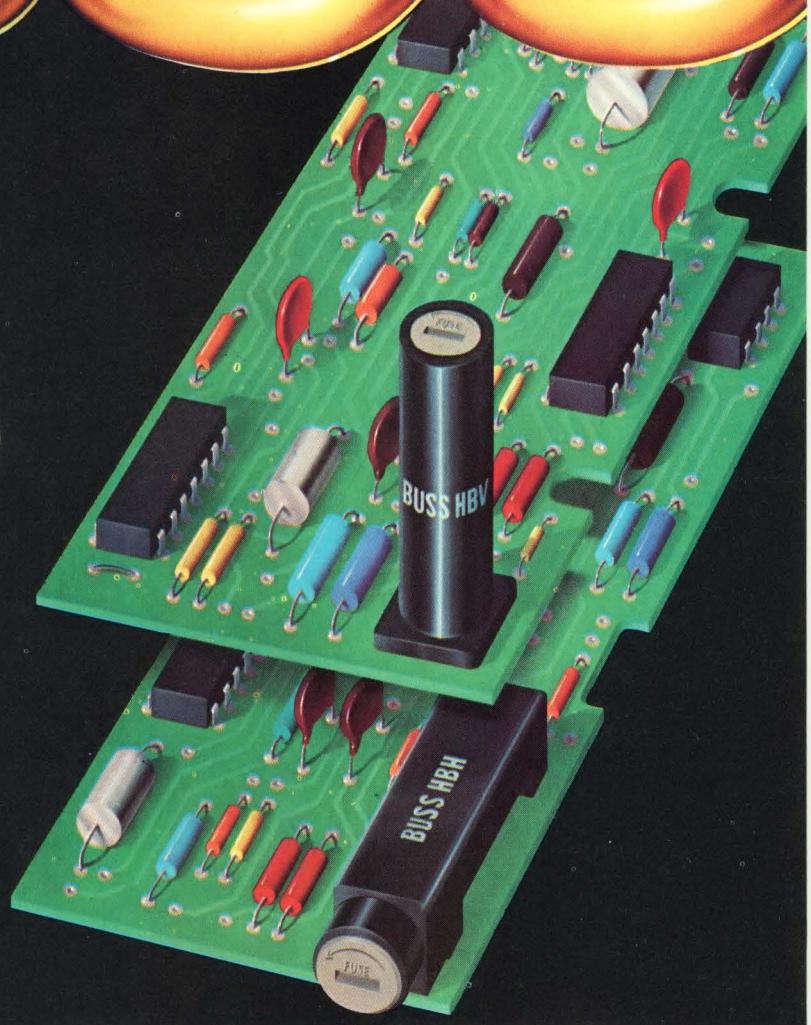
When used in general data and control applications, the bus is even more versatile—it can be divided into as many as 256 channels, each operating at 8 kbits/s. Higher bandwidths can be reached by arranging several buses in parallel.

Because the bus itself transmits data serially rather than in parallel, it needs few circuit pins. As a result, it considerably reduces pc board, backplane and packaging complexities.

Roger Allan

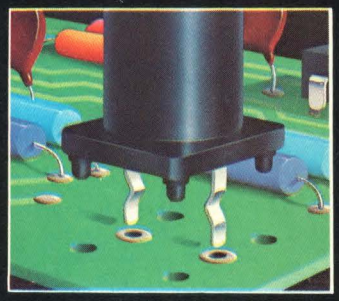
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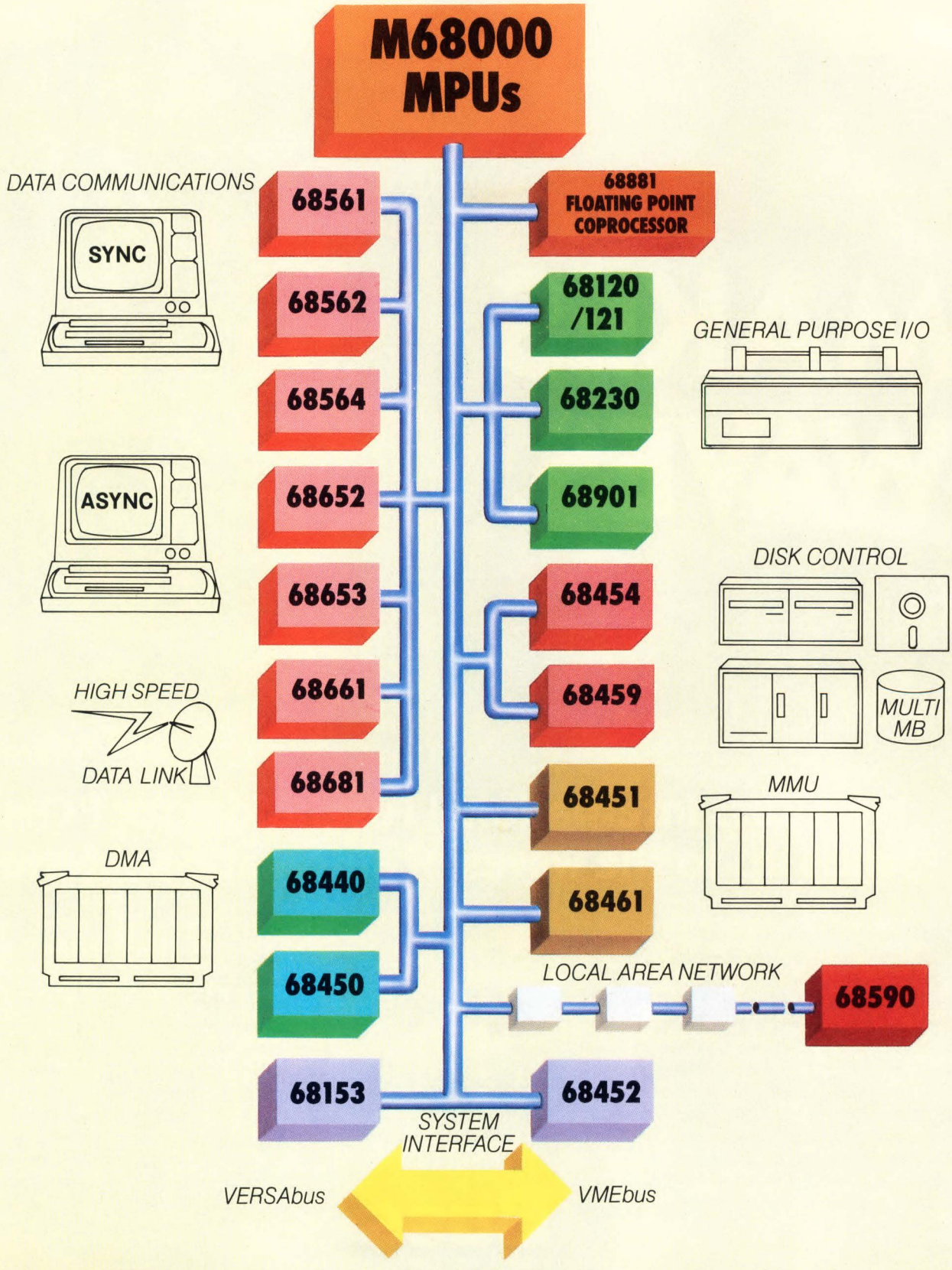
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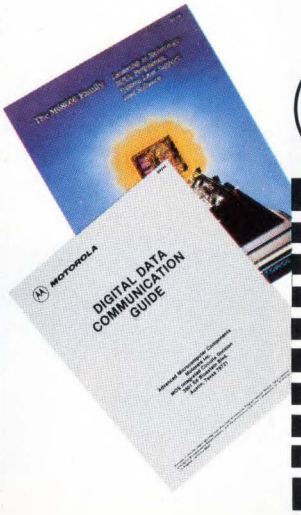
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32-bit Virtual Memory Microprocessor	MPU	68020
Floating Point Coprocessor	FPC-P	68881
Dual Direct Memory Access	DDMA	68440
Direct Memory Access Controller	DMAC	68450
Multi-Protocol Communications Controller	MPCC-2	68561†
Dual Universal Serial Communications Controller	DUSCC	68562
Serial I/O	SIO	68564†
Multi-Protocol Communications Controller	MPCC	68652
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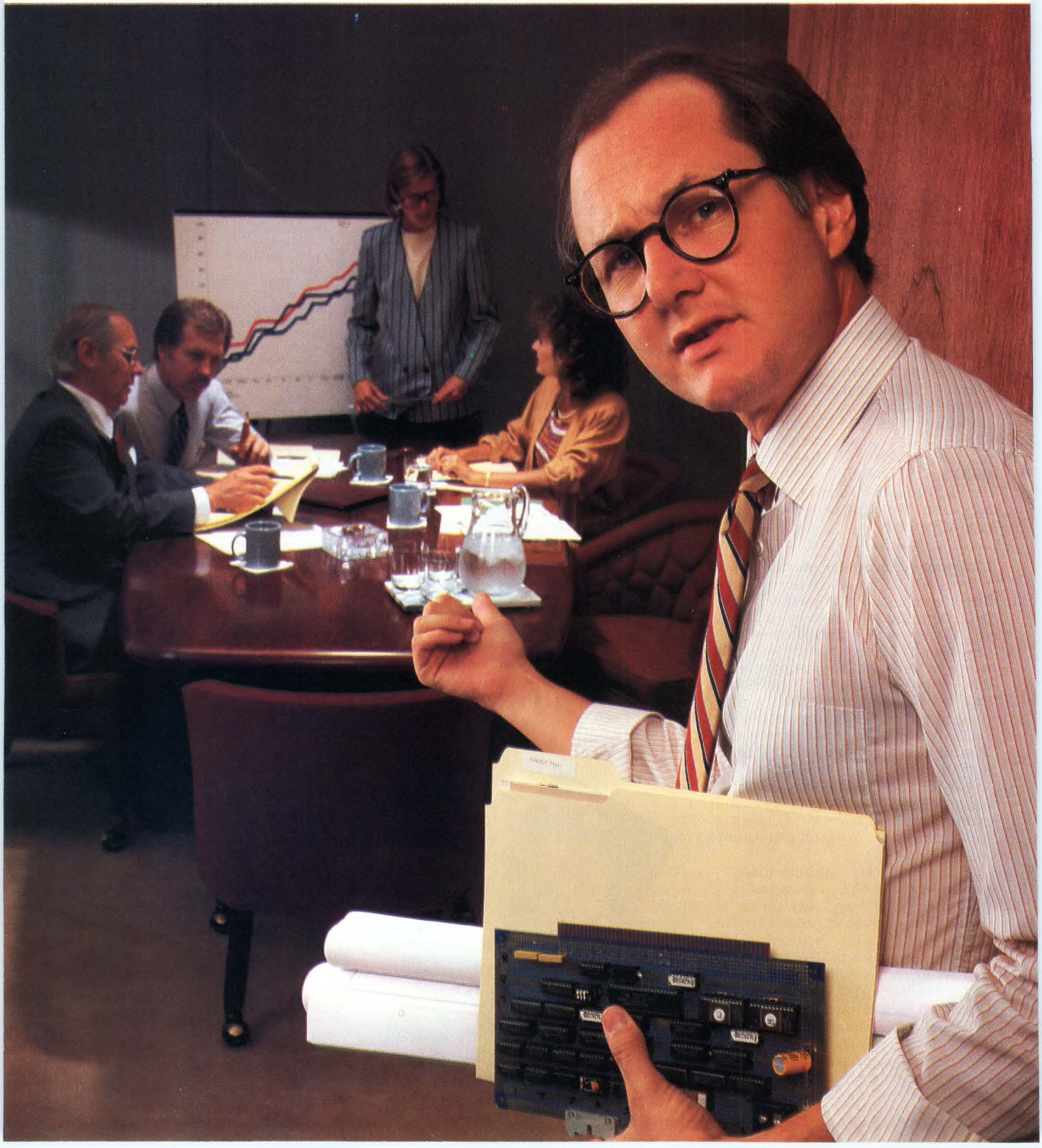
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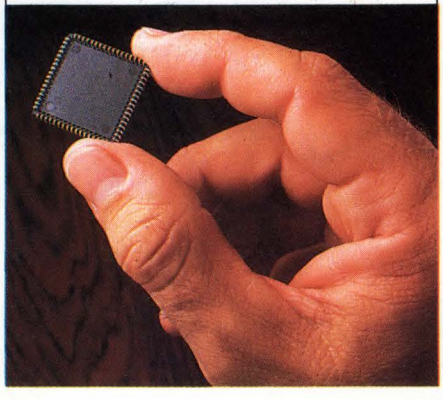
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7 Stage Counter	10G065	3 GHz

NAME	PART NUMBER	SPEED
Variable Modulus Divider	10G070	2 GHz
7 Stage Divider	11G566	4 GHz
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Diode Array	16G011	675 GHz
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Dual Gate FET Array	16G021	15 GHz
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CIRCLE 28

CONFERENCE PREVIEW

GaAs, superconducting, and optical ICs spearhead government conference

High-speed communications circuitry, VHSIC progress, and analog microwave systems are draws at conference.

Digital ICs made from gallium arsenide, superconducting and optically coupled analog-to-digital converters, and other new semiconductors for sophisticated tactical communications systems will be the hot topics at the Government Microcircuit Applications Conference (GOMAC), to be held Nov. 6-8 in Las Vegas. Also under review will be the VHSIC program; in particular, progress in fabricating high-speed, high-density CMOS circuits for signal processing. In conventional analog communications, monolithic ICs for microwave work will be examined in detail.

Cooking with GaAs

Gallium arsenide technology is making the jump into digital applications. No wonder, since the 1-μm geometries now developing give these digital chips speed and power advantages, radiation hardness, and an operating temperature range that rivals competing technologies. The material's ultimate impact on military systems will be significant, to be seen first, perhaps, in higher-speed radars and more precise early-warning systems.

Improvements in a-d and d-a converters, perhaps the most important part of digital processing systems, will extend their reach to the uhf region. Shift registers, dividers, and gate arrays that can handle signals up to 5 GHz also show progress.

Most of that circuitry is employed in one of the first digital rf memory subsystems. A hybrid from Rockwell International Corp. (Anaheim, Calif.) uses a monolithic GaAs sample-and-hold input stage and a following a-d converter to sample incoming data at rates of up to 1 GHz. Its digital output resolves to 4 bits.

After passing through several shift registers on the same chip, the data moves into a four-page (8 bits/page) static RAM that contains all the control circuitry to link the system to a microprocessor. The third stage has ECL parallel-to-serial converters and a latched d-a converter that recover the stored data. The GaAs components directly drive the ECL devices and vice versa; no logic-level translators are required. Rockwell hopes to produce an all-GaAs digital memory module in the not-too-distant future.

Indeed, work on GaAs-based memories is proceeding on several fronts. Texas Instruments Inc. (Dallas) will shortly fabricate a 1-kbit RAM. The company also uses enhancement-mode MESFETs in a 64-bit device that has an access time of 1.5 ns.

TI selectively dopes heterojunction transistors with GaAs/GaAlAs on silicon to build pn junctions with higher mobility. The company should thus get faster functions on large, 1000-gate arrays.

These selectively doped transistors go into frequency dividers made from single-gate FETs that can toggle at 5.5 GHz at room temperature. Developed by AT&T Bell Laboratories (Murray Hill, N.J.) the dividers reach a record operating frequency—10.1 GHz at 77K.

Superconducting devices represent the next wave of high-speed conversion, because they promise high resolution, sensitivity, and linearity and extremely low power dissipation. Already at hand is a 6-bit a-d converter from

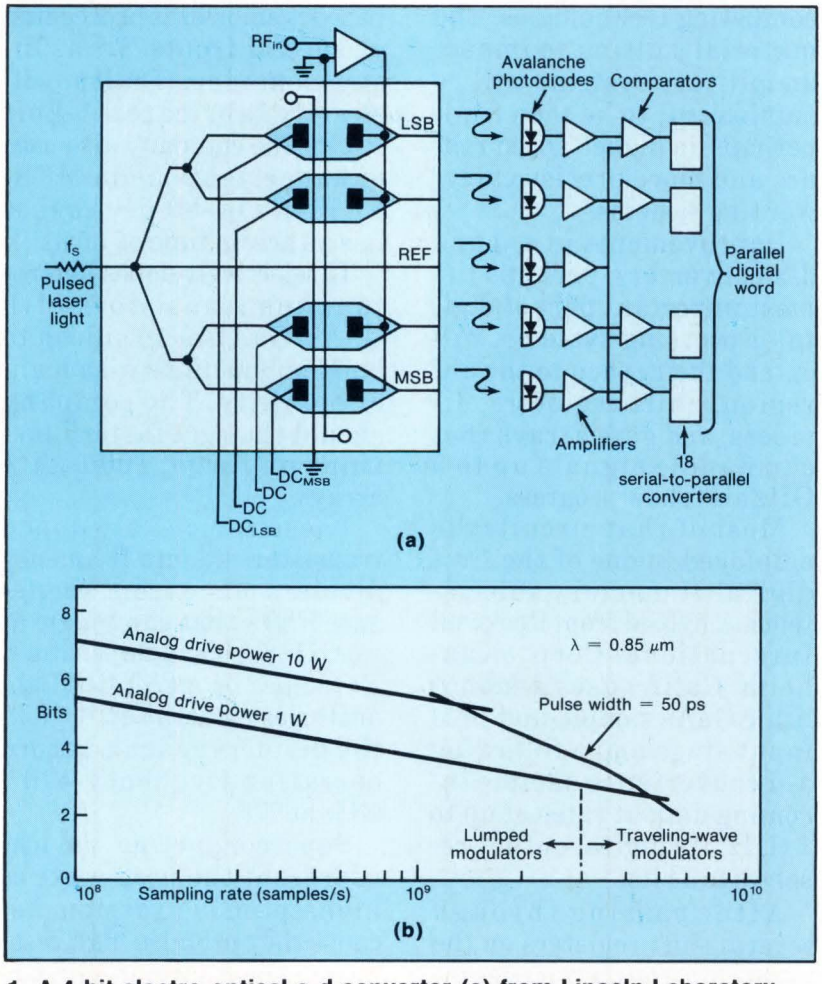
Vincent Biancomano

CONFERENCE PREVIEW

the National Bureau of Standards (Boulder, Colo.) that works at up to 4 Gsamples/s and a 1-bit unit from TRW Inc. (Redondo Beach, Calif.).

Crucial to NBS's device are six comparators made from superconducting quantum-interference device (Squid) structures. These use a magnetically controlled, lead-alloy technology and consume only 1 mW. As for TRW, it estimates that it will shortly be able to build a 12-bit, 10-Msample/s converter that draws only 10 μW.

Other promising methods for processing data at high speeds include so-called guided-wave a-d converters. A 4-bit device (Fig. 1a) under development at Massachusetts Institute of Technology's Lincoln Laboratory (Lexington, Mass.) uses an interferometer-laser system to sample data at 1 GHz. This optical technique could build multiple-bit converters that have rates equaling or exceeding those of most technologies (Fig. 1b).



1. A 4-bit electro-optical a-d converter (a) from Lincoln Laboratory uses a guided-wave interferometer to analyze input amplitudes. The bit-sampling rate attainable (b) with this technique depends on input drive power and, at the higher rates, the laser's pulse width.

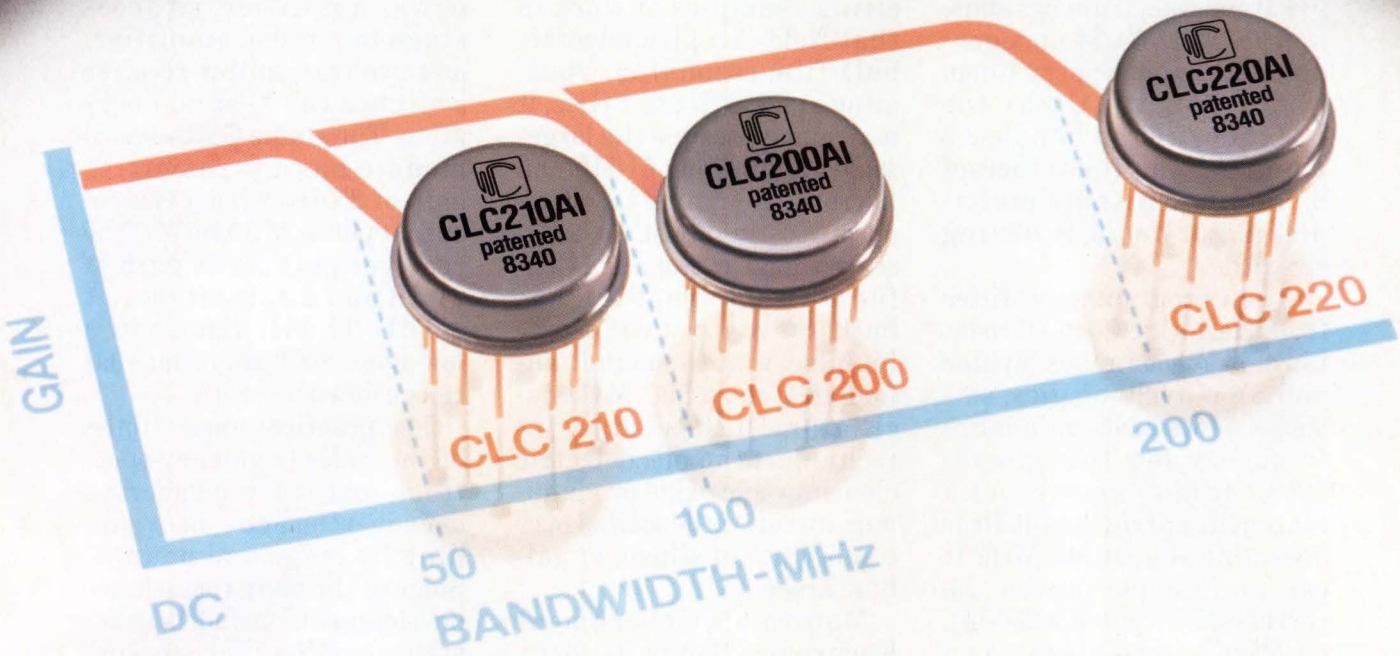
The growing role of optics in signal processing is also demonstrated by an adaptive system for canceling multipath distortion from laser-type radars (Fig. 2). Developed by General Electric Co.'s Military Electronics System (Syracuse, N.Y.), such a circuit provides weighting for both the spatial and the temporal domain without the large antenna arrays required by the former systems or delay lines of the latter.

Efforts are continuing to equip weapon systems with high-performance data processing, radar, and communications circuits within the VHSIC timetable. Among the military program's most exciting developments is a radiation-hardened, Schottky ROM. The 73-kbit device from Honeywell Inc.'s Systems and Research Center (Minneapolis, Minn.) is arranged as 192 words by 96 bits. It has an access time of only 15 ns and a power drain of 5 mW.

A late development in memories for VHSIC comes from Motorola Inc. (Phoenix, Ariz.), which uses 0.5-μm technology to produce the largest CMOS static RAM to date— 1 kbit.

CMOS's operating frequency range is also being extended in a programmable divider chip for a 250-MHz frequency synthesizer. It draws as little as 35 mW. The device, from GTE Communications Systems Division (Needham Heights, Mass.), operates in 400-MHz systems with prescaling circuits. Its

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CIRCLE 29

CONFERENCE PREVIEW

power dissipation comes to about 120 mW.

CMOS technology has found yet another application in spread-spectrum systems, in a 25-MHz VLSI encoder-decoder. From Sperry Corp. (Salt Lake City, Utah), the 16-bit device can handle 2.5 Mbits/s or multiples thereof by adding suitable multiplexing or demultiplexing circuitry.

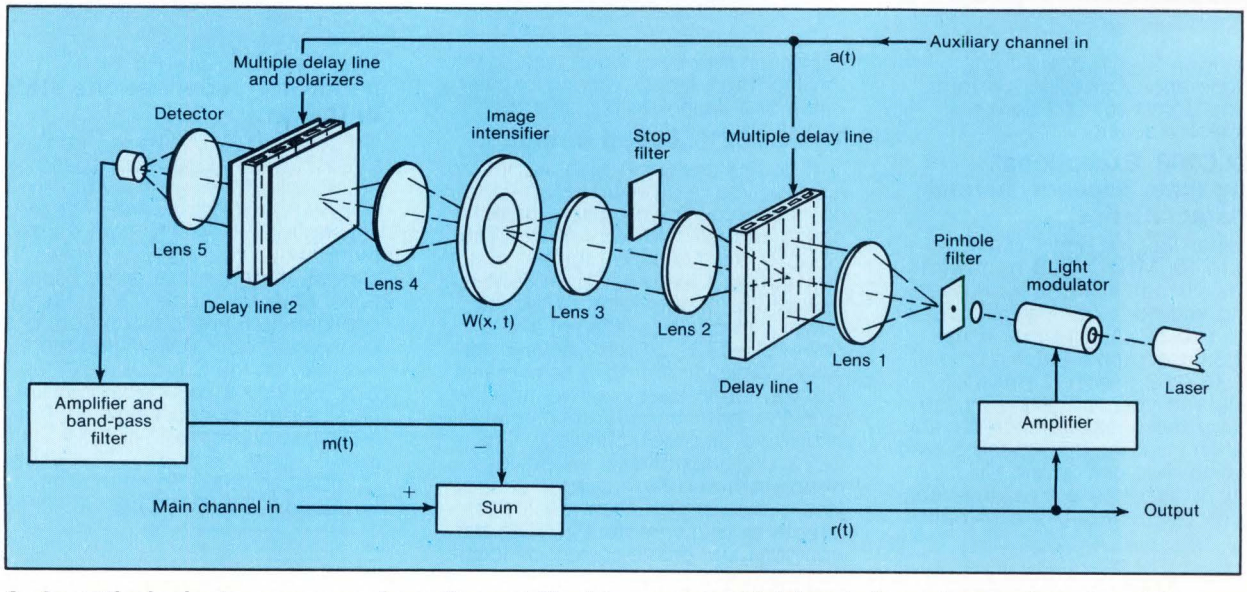
A new programmable filter from Hazeltine Corp. (Greenlawn, N.Y.) combines bipolar and SAW technologies, setting a new standard in high-frequency, low-cost spread-spectrum systems. As a matched, narrowband filter operating at up to 300 MHz, it can, for example, provide the correlated output of a 256-bit, 64-Mbit/s input signal. As a 96-tap transversal filter, it can supply a 6- to 60-dB shape factor of 1.5 and a center frequency that is programmable from 55 to 65 MHz.

Analog microwave systems continue to attract interest. Among the most exciting examples of work in that field is a piezoelectric bulk film resonator. Operating at 200 MHz to 1 GHz, it may make possible the large-scale integration of UHF and microwave circuits. Its developer, Westinghouse Co.'s Research and Development Center (Pittsburgh, Pa.), has built resonators with very high (several thousand) unloaded Q for a 500-MHz oscillator. In the company's technique, the piezoelectric element (zinc oxide or aluminum nitride) is deposited over a substrate of silicon or gallium arsenide.

Motorola's Government Electronics Group (Gilbert, Ariz.) is already developing amplifiers, voltage-controlled oscillators, and multipliers in GaAs for future integration in more complex monolithic circuits.

Other advances come from TI, which integrated a low-power amplifier, a three-stage low-noise amplifier, and two transmitter-receiver switches for X-band operation. The stable GaAs-based module has a transmitter gain of 25 dB (with a typical output power of 350 mW). The receiver path has a gain of 21 dB and a noise figure of 4.3 dB. TI will also show a low-noise FET amplifier that can go down to 2.6 dB.

The practical upper limits of the radio frequency spectrum—only a few gigahertz a decade or so ago—is expanding by leaps and bounds. Some of the more remarkable developments include a solid-state amplifier that can work at 44 GHz. The three-stage cavity-type device from Raytheon Co.'s Research Division (Lexington, Mass.) uses seven



2. An optical adapter processor from General Electric cancels sidelobes in laser-type radars. Special optoacoustical delay lines cross-correlate (modulate) radar signal m(t) with interfering samples contained in a(t) and provide suitable spatial and temporal weighting functions so that offending signals can be eliminated at the output.

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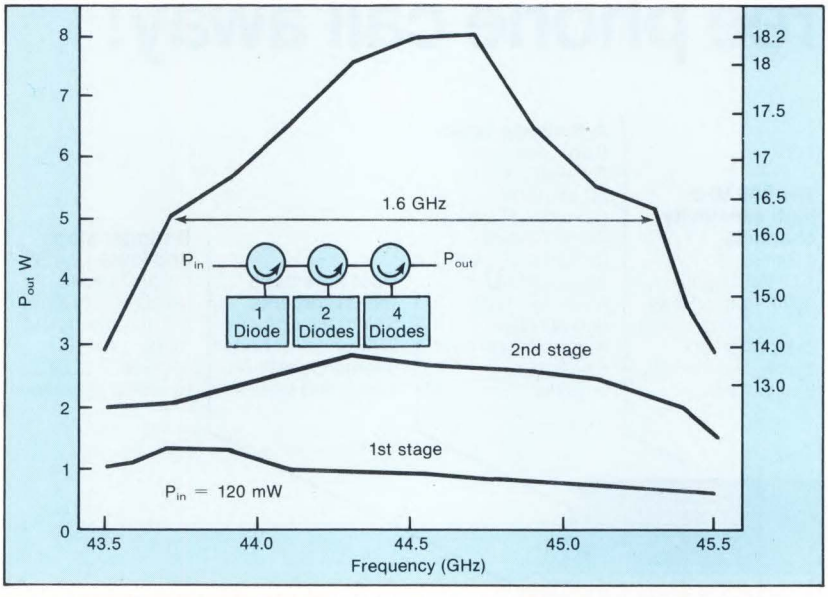
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CONFERENCE PREVIEW



3. A three-stage amplifier using Impatt diodes generates 5 W at 44 GHz. The cavity-type amplifier has a nominal gain of 16 dB and a bandwidth of 1.6 GHz.

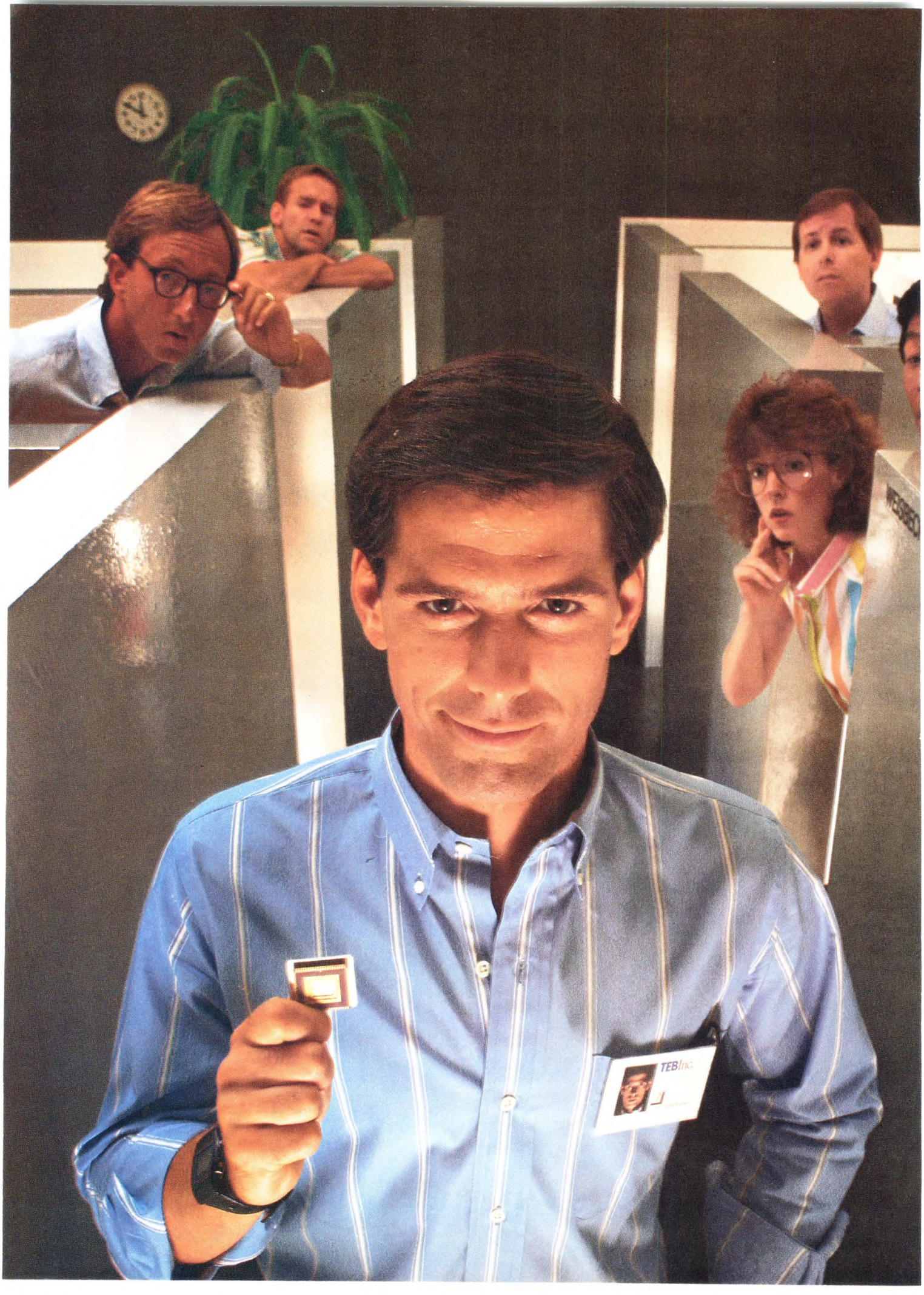
of the company's 2-W GaAs Impatt diodes to generate 5 W (Fig. 3). The amplifier has a nominal gain of 16 dB and a bandwidth of 1.6 GHz.

At the receiving end, Lincoln Laboratory has already started to integrate various circuits on monolithic structures. They have thus far combined balanced mixers and i-f amplifiers using GaAs planar-diode technology for a 32-GHz receiver. They have also fabricated antennas monolithically on the same GaAs wafer to eliminate the high-precision wave-guide circuits that are otherwise required at the receiver's front end. Conversion losses of these input networks can be held to below 4 dB.□



CIRCLE 30

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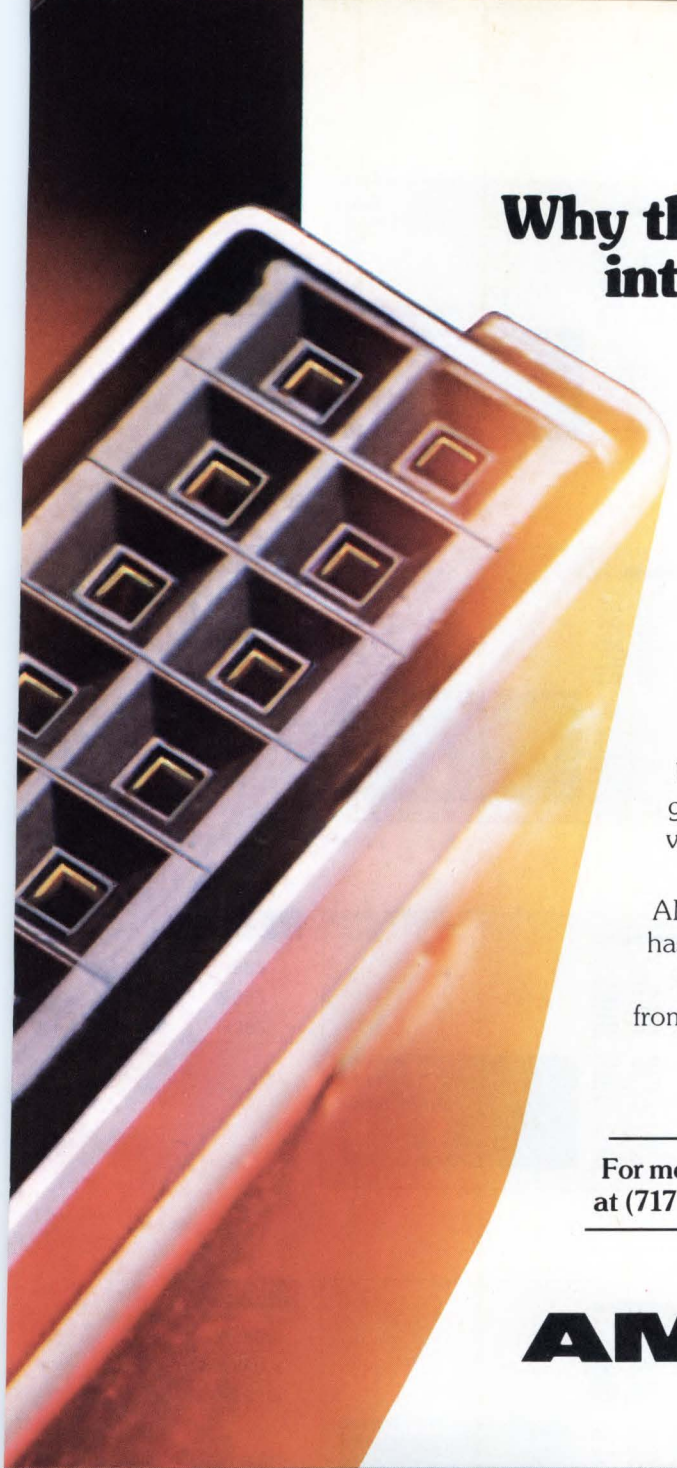
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CIRCLE 31



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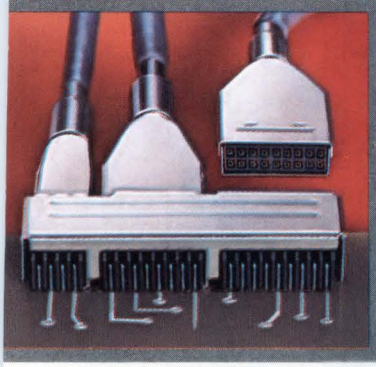
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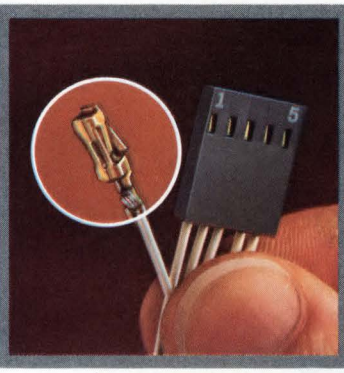
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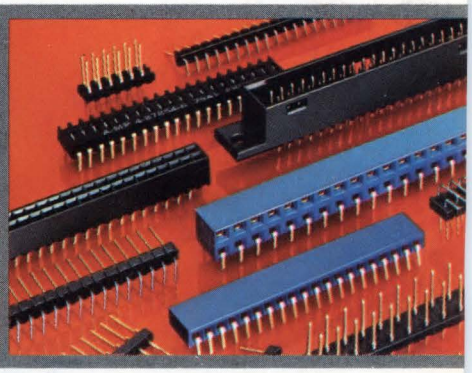
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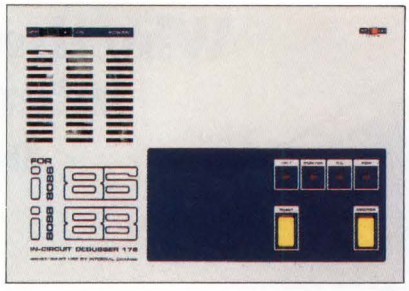
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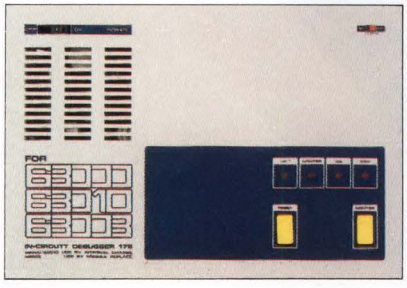


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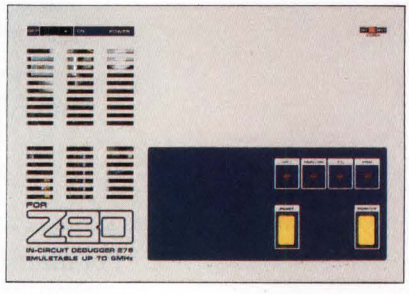
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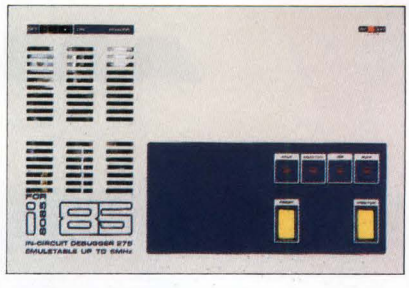
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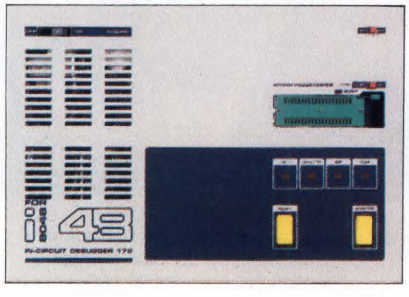
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CIRCLE 32

CONFERENCE PREVIEW

Ever more complex, VLSI chips spur testing from within and without

Testability stands out as key design issue, and AI, visual, and thermographic methods earn high marks at test conference.

The testing of VLSI devices and the systems they operate in has not kept pace with the industry's ability to design and fabricate them. Building circuits that are testable, as well as ones that are self-testing, are two solutions to this problem. Creating sophisticated testers is another.

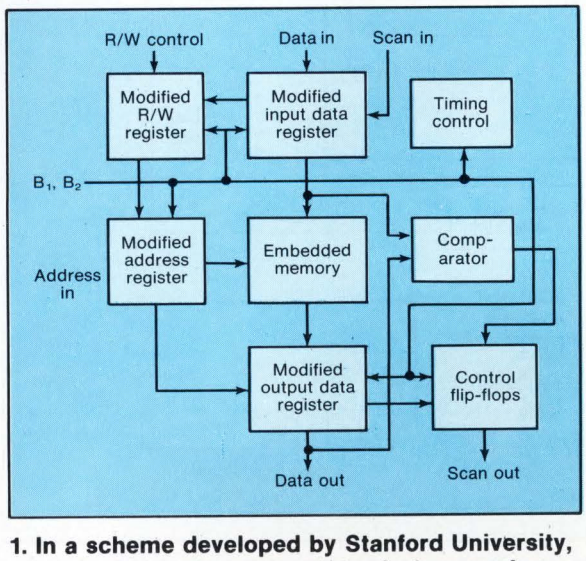
Ironically, as VLSI testers become more complex, their own failures are being diagnosed by expert systems. Along with these systems, advanced techniques like automatic visual scanning and high-sensitivity thermography will be examined at the International Test Conference, to be held Oct. 16–19 in Philadelphia, Pa.

Geared toward making designing for testability simpler, a circuit proposed by Logical Solutions Inc. (Campbell, Calif.) links the control and visibility points of a unit under test to a standard bus called the Testability Bus. Dubbed TORINO (totally-universal reset, initialization, and nodal observation), the circuit is easily incorporated as a standard cell in VLSI devices, as a gate array, or using standard MSI components.

One of the circuit's advantages is that with only a few hundred gates it can access up to 32 visibility and control points. Gate count for the circuit goes up only linearly as the number of access points increases, keeping the total area of the chip down.

One result of the growth in VLSI technology has been the integration of both logic circuits and memories on the same chip, creating special problems for testing. For instance, single-chip microcomputers often do not connect the address, data, and read/write control lines of their on-board RAM to the I/O pins. Checking these so-called embedded RAMs by feeding test patterns directly to the I/O pins is difficult.

To get around the problem, embedded RAMs can be checked through a combination of self-testing and scanning. The technique, from Stanford University (Calif.), requires that the address, input and output data, and read/write control registers associated with the memory be modified, and an on-board comparator and control flip-flops be added (Fig. 1). Two control lines, B_1 and B_2, select from among the memory's



1. In a scheme developed by Stanford University, an embedded memory operates in four modes: normal, scanning, self-testing and single stepping. Made up of modified registers, a scan path shifts in test patterns and out test results. During self-testing, the address, input data, and read/write control generate a march test pattern.

Bob Milne

CONFERENCE PREVIEW

four operating modes: normal, scanning, self-testing, and single stepping.

Under normal conditions, the memory functions as a regular RAM. Alternatively, its registers and flip-flops make up a scan path to shift test patterns in and test results out. Scanning detects failures like bridging faults between data lines and stuck-at faults in the memory.

March through memory

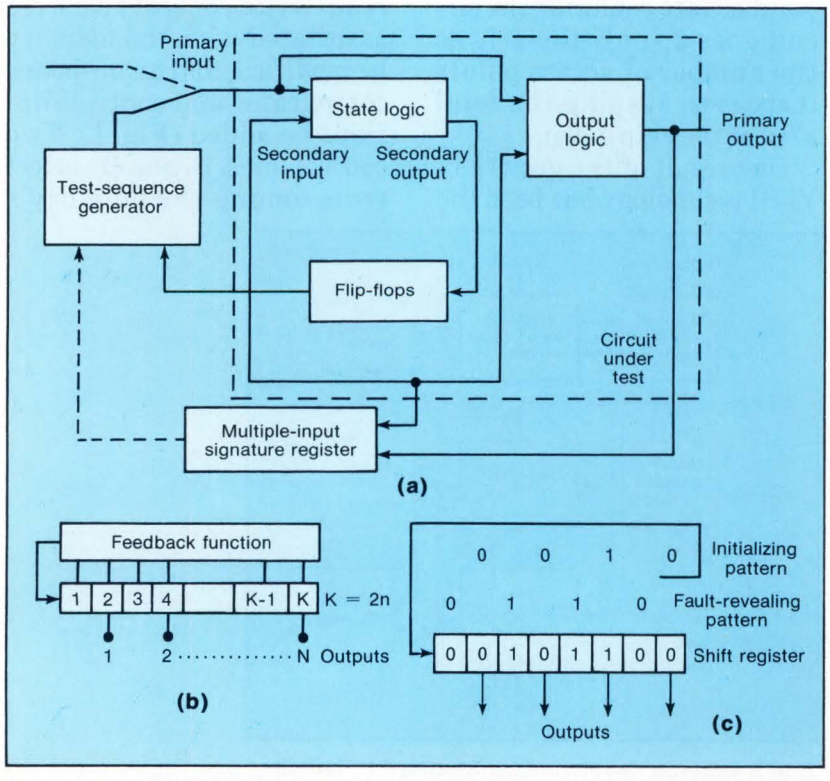
In the self-testing mode, the circuit's address, input data, and read/write control registers generate a simple march test pattern to check the memory. An engineer can interrupt self-testing to inspect, scan out, and analyze an intermediate result by single-stepping the memory.

Self-testing is also being implemented in CMOS logic through two hardware test-generation techniques. Developed at the University of Hannover (West Germany), one is for a sequential circuit, the other for a combinatorial one.

In the first, a multiple-input signature register evaluates test information; a test-sequence generator can be controlled by the circuit itself or in conjunction with the signature register (Fig. 2a). Compared with designs in which the test generator works independently, this technique reduces the number of generator flip-flops and the amount of state logic.

For combinatorial CMOS circuits, which become sequential in the presence of stuck-at-open faults, a second test-sequence generator has been developed. Here, a pair of patterns tests each fault. The first pattern initializes the circuit to a known state, and the second pattern reveals the fault to the circuit outputs. Test patterns are generated with a nonlinear feedback shift register—a technique often employed in checking combinatorial circuits. The difference is that in this case the shift register is twice as long as the number of outputs (Fig. 2b).

Both the initializing pattern and the fault-revealing pattern are merged into a single-state vector by alternately shifting in bits from each (Fig. 2c). After the shift is complete, the initializing pattern appears at the register outputs. One more shift generates the fault-revealing pattern.



2. A sequential CMOS circuit, designed by West Germany's University of Hannover, controls a test-sequence generator and has a multiple-input signature register to evaluate the test results (a). For testing a combinatorial CMOS circuit, a nonlinear feedback shift register (b) alternately shifts in bits from initializing and fault-revealing patterns (c), forming a single-state vector.

Get an expert

As VLSI devices get more complex, the systems that test them have to follow suit. Consequently, artificial-intelligence systems are surfacing as diagnostic aids to service personnel.

One such system that detects and diagnoses faults within VLSI testers is made up of six elements: a test engine, system hardware, a test knowledge data base, a diag-

DDC NEWS

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ILC Data Device Corporation (DDC) is proud and pleased to announce that it is the very first company to have its facilities fully certified under the new MIL-STD-1772. Official certification was issued by the Defense Electronics Supply Center (DESC) on September 14th. This new standard, which effectively complements and extends MIL-M-38510 and MIL-STD-883, will have a profound impact on the way military hybrid microcircuits are manufactured and procured. Under the new requirements, hybrid manufacturing lines and process qualification methods will now be audited according to a uniform code of procedures. A hybrid manufacturer must now have a MIL-STD-1772 certified facility to be able to claim or mark its hybrids as being processed to MIL-STD-883.

In the past, some problems occurred when variations in hybrid quality were allowed to enter the military procurement system. Consequently, Rome Air Development Center (RADC) and the Joint Electron Device Engineering Council (JEDEC) sought to relieve the problem by issuing MIL-STD-1772 on May 15, 1984.

Briefly stated, MIL-M-38510, Appendix G, will now require hybrid manufacturers to have their facility certified by DESC. MIL-STD-1772 is the governing document and accordingly, defines the quality assurance provisions that must be adhered to. Certification requires extensive preparation in the form of test and evaluation of manufacturing processes with strict process control—(i.e., no changes to process or material without re-audit, certification and/or approval). In addition, a detailed MIL-M-38510 Product Assurance Appendix A Program Plan must be submitted to DESC for approval prior to the actual audit.

Two special teams from DESC conducted an in-depth audit at DDC in recent months. This entailed checking the Company's facility, equipment, work instructions, documentation, revision control systems and the qualifications of its personnel. The favorable results and subsequent certification are a tribute to DDC's long-standing commitment to quality and customer satisfaction.

DDC supports the new standard in the belief that it can only result in a major upgrade of manufacturing discipline in the military hybrid world. Benefits to the user will be in the form of more reliable products and to the manufacturers, more equitable competition in the marketplace. DDC will remain the leader. **First in MIL-STD-1772, First in Quality and First in Mil-Spec Hybrids!**

If your program requirements include MIL-STD-883, Revision C, and MIL-M-38510F, Appendix G, please call DDC at one of the telephone numbers below for a quotation on your hybrid components or sub assemblies. □

CIRCLE 34 FOR LITERATURE

CIRCLE 35 FOR SALES CONTACT

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CONFERENCE PREVIEW

nostic rule data base, causal maps, and an inference engine. From Teradyne Inc. (Woodland Hills, Calif.), the machine for intelligent diagnosis, or MIND, is "taught" by an experienced human troubleshooter.

Initially, the instructor's experience in test-system repair is translated for the system. Next, as failures are simulated, the instructor critiques the diagnostic paths taken by the system. This feedback allows MIND to learn from the instructor.

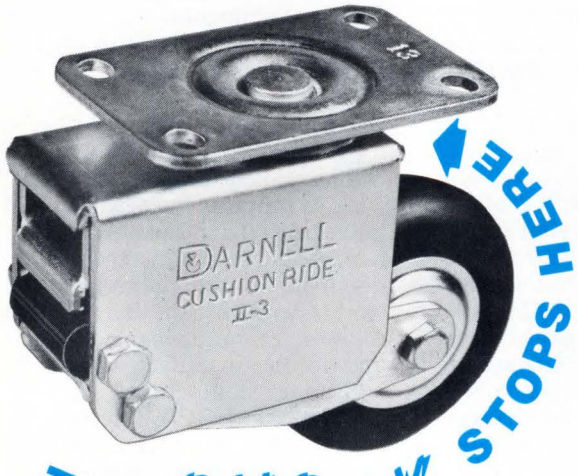
Look at the birdie

Printed-circuit board testing also is benefiting from automation. After a board is assembled, one of the first checks it usually gets is a person looking it over. A comparative study by the Cognex Corp. (Needham, Mass.) makes a strong case for having a camera capture the board's image and transmit it to a computer.

The computer checks the board for visible assembly defects. Thanks to advanced pattern-recognition techniques, the computer detects 99% of such defects, and when used with a shorts tester, eliminates the need for in-circuit testing.

A different approach to checking pc boards, high-sensitivity thermography, has been analyzed by the UTI Instruments Co. (Sunnyvale, Calif.). Because the system does not require any thermal connections to the device under test, a designer can get a true thermal profile of the die components and interconnections of VLSI and hybrid circuits.

Wed to bed-of-nails testing, thermography enhances diagnostic power. For instance, the tester may detect a short between two nodes on a printed-circuit board, but it will not tell the operator the exact location of the short. If power is applied to the shorted nodes, however, thermography will pinpoint the location of the short as a hot spot on the thermogram.□



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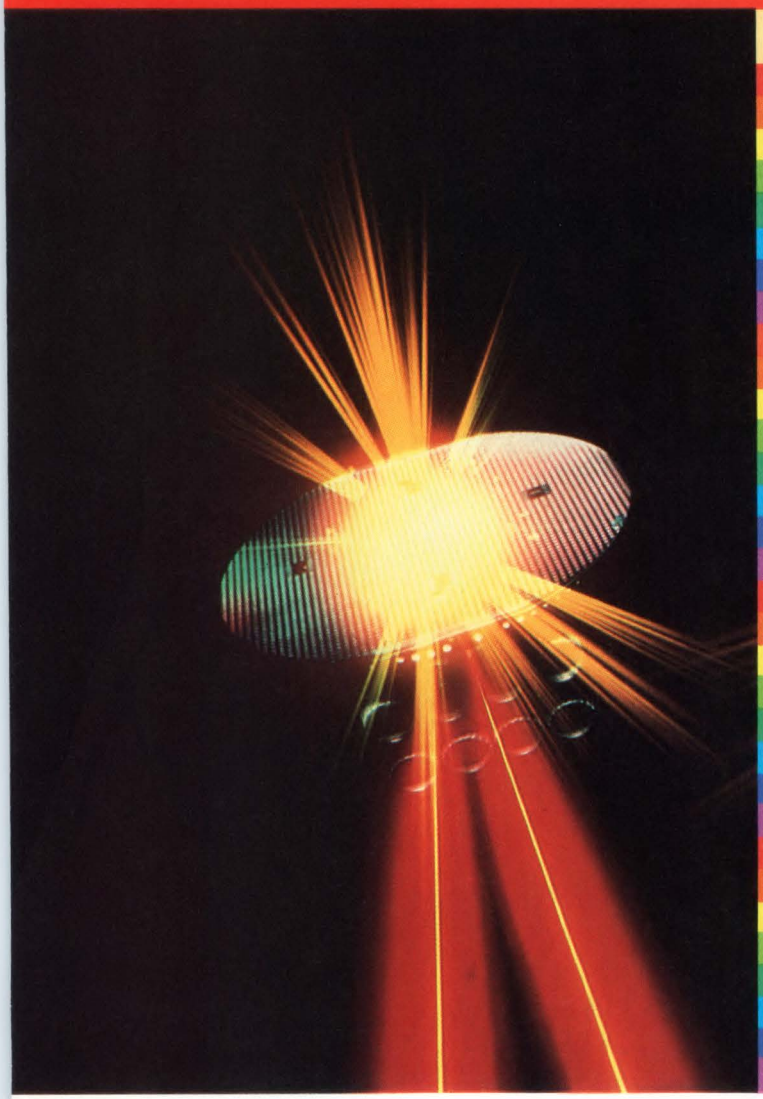
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CIRCLE 36

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HC/HCT366*	Hex Buffer/Line Driver; 3-State; Inverting
HC/HCT367*	Hex Buffer/Line Driver; 3-State
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting
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HC/HCT174	Hex D-Type Flip-Flop with Reset
HC/HCT175	Quad D-Type Flip-Flop with Reset
HC/HCT273	Octal D-Type Flip-Flop with Reset
HC/HCT374*	Octal D-Type Flip-Flop; 3-State
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting
HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting
LATCHES	
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HCT533*	Octal Transparent Latch; 3-State; Inverting
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HC/HCT158	Quad 2-Input Multiplexer; Inverting
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HC/HCT154	4-to-16-Line Decoder/Demultiplexer
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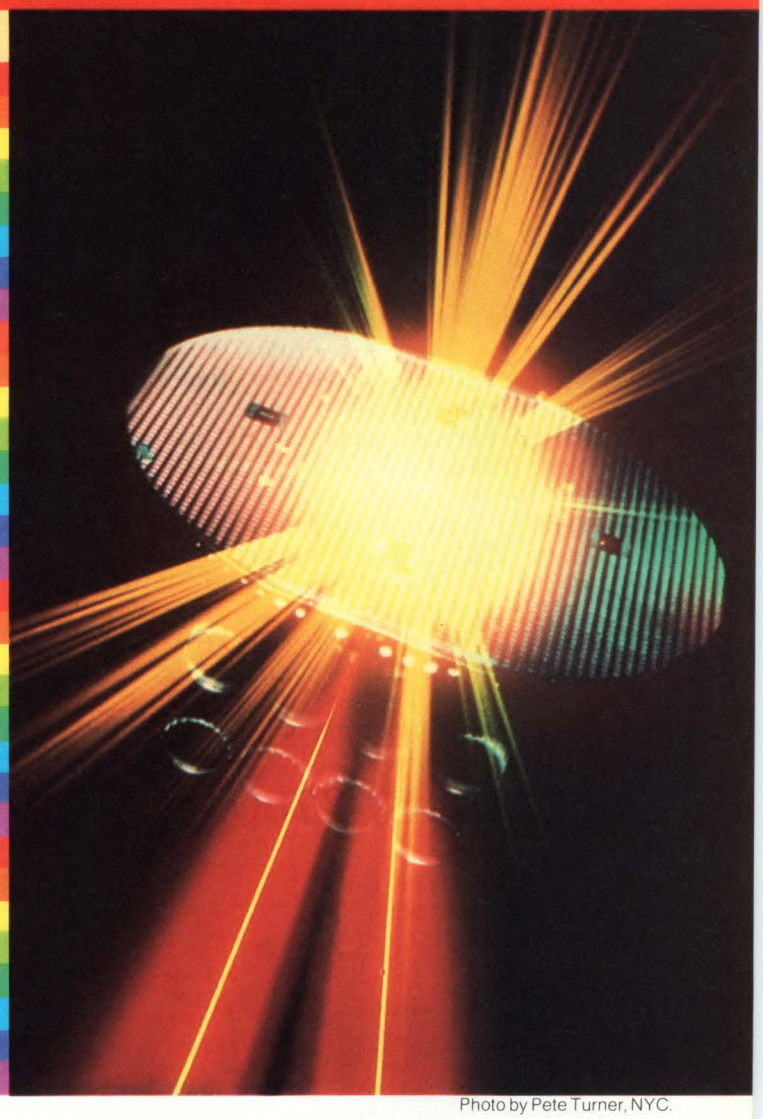


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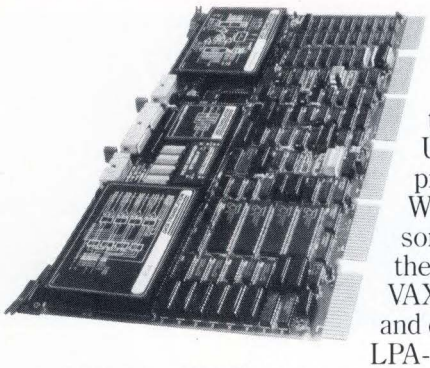
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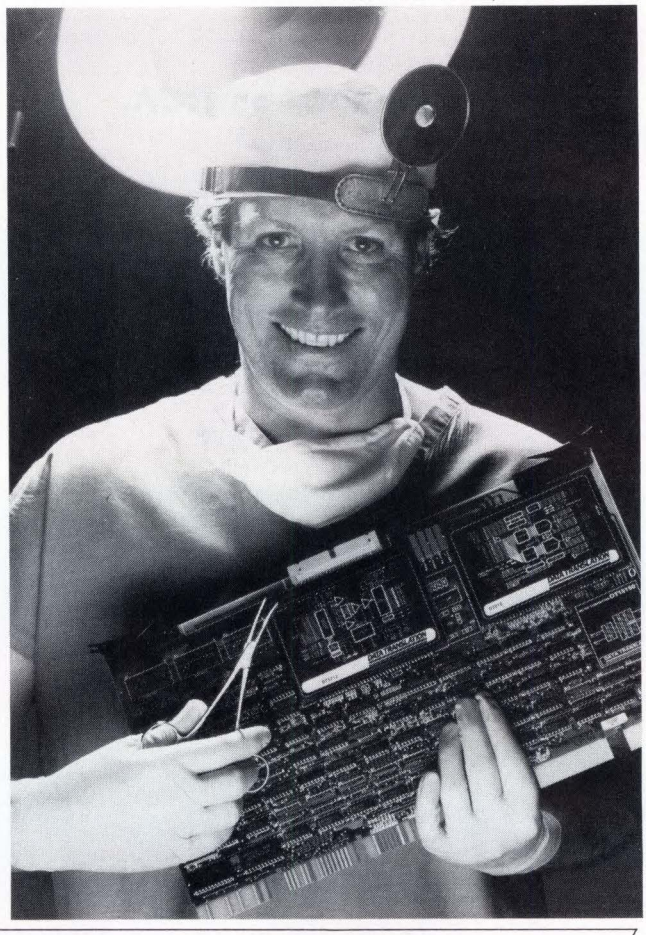
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CIRCLE 37

CONFERENCE PREVIEW

ICCD will heat up with gallium arsenide, AI, and supercomputers

The International Conference on Computer Design will take a close look at the crucial issues affecting VLSI in computers.

Gallium arsenide devices may hold out the promise of blazing speed and extremely low power consumption, but they still have a long road to travel before they pose any threat to silicon as the primary VLSI technology. That is just one of the beliefs revealed at this year's International Conference on Computer Design.

The gathering, whose theme is VLSI in computers, will examine many of the critical aspects related to that subject. The move to artificial intelligence to simplify CAD will also be of great concern, as will the fifth-generation supercomputers that are achieving breathtaking speeds by working with specialized vector-processing architectures. The meeting will be held in Rye, N.Y., on Oct. 8–12.

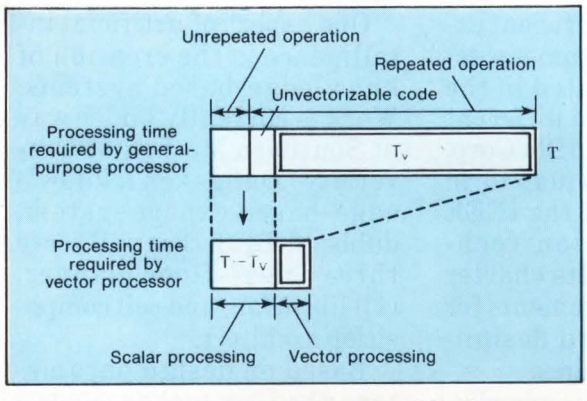
GaAs is emerging as a high-speed, low-power material that may eventually overtake silicon. At its present stage of development, though, it is not ready to step into its predecessor's shoes.

One of the chief obstacles in gallium arsenide's path is the difficulty involved in designing large-scale arrays that are of comparable complexity to those built with silicon. The largest integration thus far reported is a 4-kbit static RAM that employs about 25,000 active devices.

Production problems have also blocked progress in GaAs technology. Interestingly, improving production controls yields little increase in the percentage of good chips in any run. As the Defense Advanced Research Projects Agency notes, random defects are a major stumbling block in GaAs fabrication.

According to DARPA, the reason for the shortfall is that GaAs manufacturing facilities are not operated at the level of their silicon counterparts. Once equally tight controls over factors such as particle contamination are in place and rigorous schedules and substantial throughput are instituted, yields should begin to improve. Further, it is hypothesized that once these steps are taken, a learning curve—similar to that of silicon will be seen with GaAs.

Although companies are pushing for GaAs integration on a scale comparable with that of silicon, it may be more fruitful to treat GaAs chips as a separate class of processors rather than as a potential replacement for silicon. Over the short term, GaAs devices will not approach the complexity of silicon, so more ICs



Vector processing—as implemented in the Japanese supercomputers—dramatically reduces the time needed to handle vectorized variables. T represents the time required for program implementation by a scalar processor; T_V the time for execution of the vectorized calculation. As can be seen, no advantage is realized in the time required for scalar processing.

Mark Brownstein

CONFERENCE PREVIEW

will have to do the job handled by a silicon processor.

GaAs shines in settings where speed is the primary concern, like video processing, data encryption, and biomedical applications requiring transient event detection. It is even more valuable when high speed must hook up with low power consumption.

As is evident at ICCD '84, CAD will be among the primary tools for future VLSI circuitry. With the increasing intricacy of circuits, plus the complexity of design tools, design data itself will become increasingly complicated. Hence, a language will be needed to simplify specifying component features and chip performance.

Speak my language

One approach to the issue of languages breaks them into two areas: a design language that permits an engineer to communicate with design tools and a description language that allows efficient exchanges to be made among design centers—located in the same company or at different ones. That tack led IBM Corp. (Manassas, Va.) to help form a subcommittee of the IEEE Design Automation Technical Committee. Its charter is to develop requirements for industry-standard design-automation languages.

The problem of standardizing design languages is thrown into sharp relief as various languages emerge. One, jointly developed by Tektronix Inc. (Beaverton, Ore.) and National Semiconductor Corp. (Santa Clara, Calif.), is known as the Electronic Design Interface Format. EDIF targets gate-array and semicustom ICs. It derives from a number of earlier languages, including the Common Interchange Description Format and the Gate Array Interface Language. EDIF already has the backing of many of the major design and silicon manufacturing companies, including Daisy Systems Inc., Motorola Inc., and Texas Instruments Inc. With that kind of support, the industry may ultimately see the evolution of more than one "standard."

Nothing artificial about it

Artificial intelligence is emerging as a key concern in CAD. Its immediate goals are to furnish a user-friendly interface, on-line tutorials, and help facilities. Ultimately, AI may be able to produce a circuit design once a user feeds all the needed specifications into a system.

One aspect of artificial intelligence is the creation of knowledge-based systems. Work is currently under way at Southern Methodist University (Dallas) on a knowledge-based expert system, dubbed KBES, that will serve three roles—floor planner, cell librarian, and cell composition architect.

Based on design parameters, the first tool develops a high-level plan of a chip layout. The system breaks a chip into a number of design regions, or functional blocks, that can be integrated into the larger design.

The cell librarian serves as a data base containing VLSI design cells. The library is functionally independent and free to carry out certain logical operations. Once developed, a floor plan can be filled in by cells stored in the library that most closely match particular requirements.

On the eastern front

A great deal of attention has been given to Japan's so-called supercomputers. These machines are aiming at a performance of about 10 billion floating-point operations/s. Currently, the fastest computer is the S-810, from Hitachi Ltd. (Kokubunji), which is capable of performing 630 million floating-point operations/s. Another entry, the SX-2 is expected sometime soon, from NEC Corp. (Tokyo), and will run at roughly 1.3 billion floating-point operations/s.

Such speeds are obtained by using sophisticated architectures that primarily enhance a computer's ability to process vectors (see the figure). In general, high vector performance is achieved by using a number of pipelined ALUs operating in parallel. In addition, the effective application of main storage and buffers ensures the rapid transfer of data.

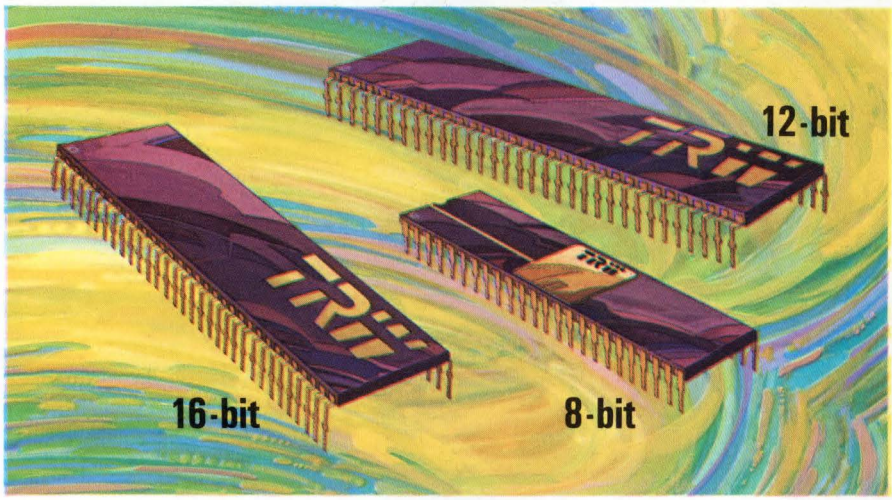
Additionally, ICCD '84 will explore other areas of interest, including logic simulation, systolic arrays, gate-array layouts, and machine architecure. Finally, emphasis will be placed on wafer-scale technology and parallel processing.□

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TMC2008	8-bit	19-bit	100 ns	See footnote (1)	TDC1008	48-lead DIP or 68-pin contact or leaded chip carriers

(1) Worst case: Static dissipation 50 mW; dissipation changes approx. 50 mW/MHz. *All packages are pin-compatible with Bipolar equivalent.

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CIRCLE 38

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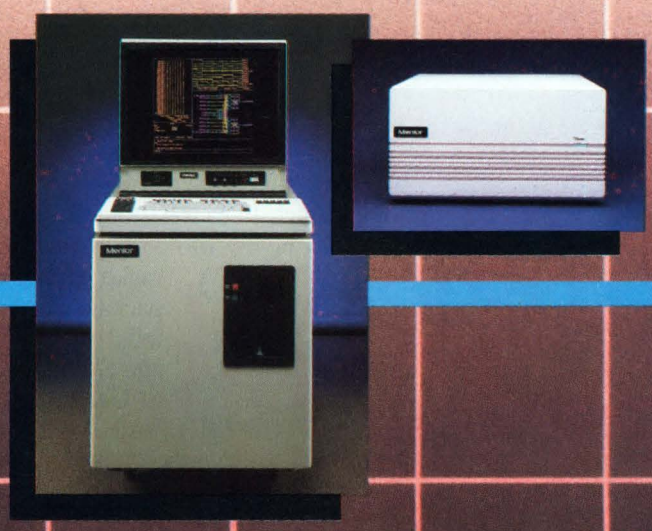
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VIEWPOINT

Digital scopes will emerge as the standard tools for hardware designers

William G. Parzybok Jr.
Vice President and
General Manager
Design Systems Group
Hewlett-Packard Co.
Fort Collins, Colo.

Oscilloscope technology has always been driven by the measurement needs of the user. As William G. Parzybok Jr. predicts, "If you could step forward to the end of the decade and look at a digital designer's bench, chances are you're not going to see a 100-MHz analog oscilloscope. In its place will be a sophisticated digital scope."

When working with high-speed logic, for instance, an engineer is concerned with the very small differences in time intervals between signals that significantly affect a circuit's performance. Because a digital scope uses a crystal oscillator for its time base, notes Parzybok, these intervals can be measured very accurately.

Another advantage that digital instruments offer is their ability to work with what is known as negative time. Parzybok explains: "In the digital world, if you're going to measure a signal, it's very important to know what preceded it. If there's a glitch in the system, the designer needs to look back in time and see what happened.

"Besides that, narrow pulses with low repetition rates are pretty hard to catch with an analog scope. With a digital instrument the measurement is easily made."

This comparison, Parzybok points out, illustrates a basic difference between analog and digital scopes. "In an analog scope, the CRT itself is directly involved in the measurement process. The CRT on a digital oscilloscope, in contrast, is simply a computer graphics display." Consequently, the emphasis in digital scopes has shifted from the CRT to front-end technology.



In his 16 years with HP, William G. Parzybok Jr. held a host of positions before being appointed general manager of the company's Electric Measurements Group. That section's 11 divisions account for roughly two-thirds of HP's instrument business. He was promoted to his current position earlier this year.

"In the digital realm," he continues, "the push is on for faster analog-to-digital converters and speedier memories." Right now, in fact, the a-d converter is one of the limiting factors in the performance of digital scopes.

Parzybok foresees breakthroughs that will affect the front ends of digital instruments. "A lot of work is being done around the world in microwave semiconductors."

Parzybok brings up an interesting point concerning digital scope profiles. "I think it will be important to the designer to access a large number of points easily without moving probes all over the place. In other words—multiplexed probes."

One question that always comes up concerning digital scopes is whether they will

Bob Milne

VIEWPOINT

become part of a "universal" instrument. Parzybok does not think so, even though their architecture (a-d converter, memory, and display) resembles that of spectrum analyzers and data acquisition systems. "I think we're a long way from realizing a universal instrument. You have to optimize a piece of equipment around what the user is doing with it—for instance, a-d performance and memory speed. In the case of the scope, it has to be tailored to digital hardware design. "Equally important," he concludes, "the trend is toward scopes that work in harmony with other instruments, like logic analyzers, to form what will be known as the complete electronic workbench."

Testing and servicing suffer at the hands of throwaway design methods

John Harnett
Director of Planning and Development
TRW Inc.
Customer Service Division
Fairfield, N.J.

Designers and manufacturers of high-technology products are leaning toward the same "throwaway" mentality as consumer electronics manufacturers, who churn out ever-new gadgetry to titillate a fickle consumer. "Manufacturing is being driven to least-cost design by the forces of competition," says John Harnett. "Test and repair beyond the requirements of the manufacturing line are often omitted from designs—usually for cost reasons."

There is a general movement toward surface-mounting techniques at the expense of field engineering. OEMs who integrate assemblies, printed circuit boards, and similar devices may be more aware of servicing demands than someone who walks into his corner Computerland to buy a personal computer—but they have been unable to influence manufacturers on consumers' behalf.



John Harnett has come up with some novel solutions to the problem of repairing high-technology devices. Before joining TRW, he held a management position with Singer. A graduate of St. Peter's College in New Jersey, he also holds an MBA from the University of Pennsylvania's Wharton School of Business.

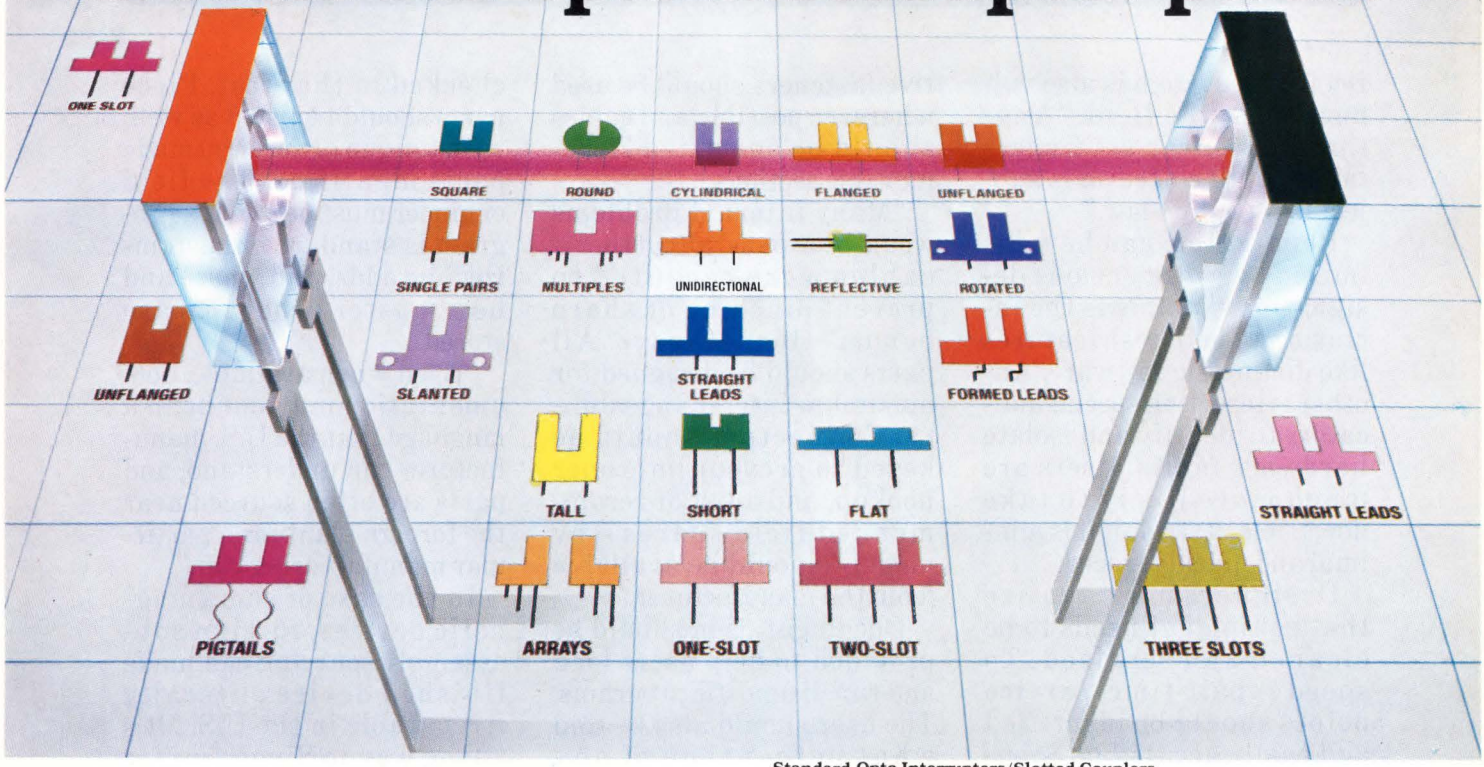
On the one hand, Harnett notes, there have been some great advances in both the circuit density and reliability of devices. Statistically, this presents a strong case for minimizing rarely used test points, saving that space for new features that appeal to designers and users.

"But until the day arrives when all the elements of a computer are really manufactured at throwaway prices," he warns, "ignoring these same test points and sockets will take its toll in user satisfaction."

"Statistics don't mean a lot when the device that you own fails," he points out. "No matter how good the quality control, 1 in 10 systems manufactured this year will need

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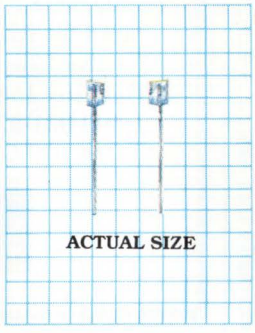
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repair." A system is also vulnerable in the field. "Anything a user can get fingers into or spill coffee on is subject to Murphy's law."

Repair time can be minimized by conscientious design. One example is the inclusion of self-test features like diagnostic software. Another is inserting special indicators to identify and isolate hardware faults. Users are much more likely to take downtime in stride if it is minimal and quickly traced.

Designers must realize that equipment needs to be cleaned and serviced. To speed repair time, service points should be identified and easily accessible. Standard quick-release and captive fasteners should be used wherever possible and cables should be specified in removable sections.

"Many internal problems would be avoided altogether if cables were rerouted to prevent pinching or sharp bends," Harnett says. All parts should be designed for maximum interchangeability. Connectors should be keyed to prevent improper hookup, and a list of recommended field spares—by model—should be available from the manufacturer.

Documentation should be provided to help users load and run diagnostic programs. The user should also be told what percentage of any system is actually being checked in that test. Piece parts should be listed as well, with unique or foreign-made parts identified. The field engineer must be told if a program is standard or customized, he adds, and where and how master programs are stored.

"Even when available, documentation may not be in a language that the U.S. manufacturer can understand, and parts are often sourced near the foreign plant for a particular manufacturing run."

In the case of some magnetic devices, foreign subassembly sourcing can make finished devices literally irreparable in the U.S. "It's a long way to Singapore for components," says Harnett.□

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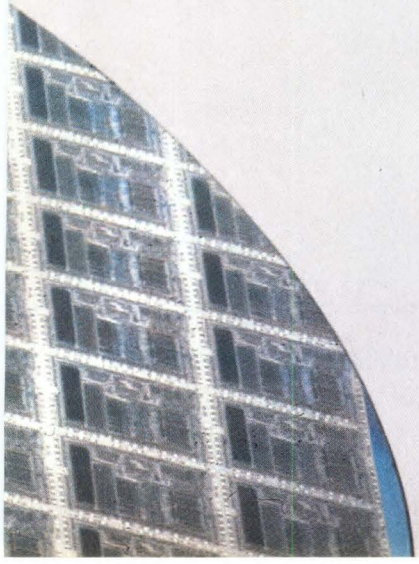
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Holographic 'backplane' aims to swell throughput of multiprocessors

Replacing masses of switches with spatial holograms may permit processors to communicate at over 10^{14} bits/s.

Currently limited by poor interconnection schemes, multiprocessing promises to take off with a holographic system that will employ light beams to transmit more than 10^6 channels at 10^8 bits/s. That throughput far exceeds the rates possible with massive crossbar switches or hierarchical architectures.

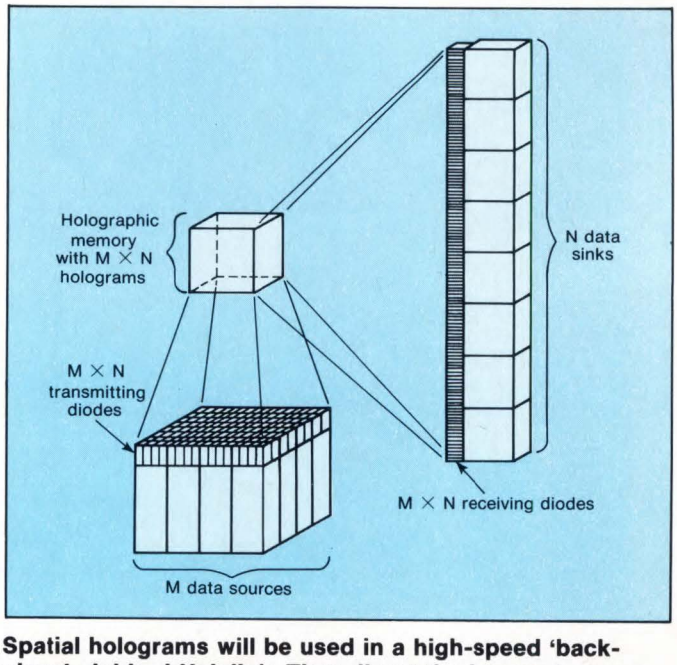
At Fraunhofer Gesellschaft (Karlsruhe, West Germany), Europe's largest nonprofit organization for applied research, scientists want to connect all of a computer's processors and nodes together with a holographic system, dubbed Hololink.

Let there be light

In Hololink, spatial holograms serve as a kind of backplane wiring system that remains constant as long as the computer configuration does not change. Consequently, although it is based on the concept of holographic memories, Hololink does not depend on the still unrealized ability to rewrite a spatial hologram.

In operation, signals originating in M data sources (e.g., processors) are sent to N data sinks (e.g., nodes) over M×N light-emitting diodes (see the figure). The holographic coordinator routes the light beams to the same number of photosensitive diodes distributed over the input devices. Thanks to the high angular resolution of spatial, or volume, holograms, more than 10^6 channels can be transmitted, collision free, at 10^8 bits/s. The resultant 10^{14} bits/s far exceeds the bandwidth of any electrical linking system.

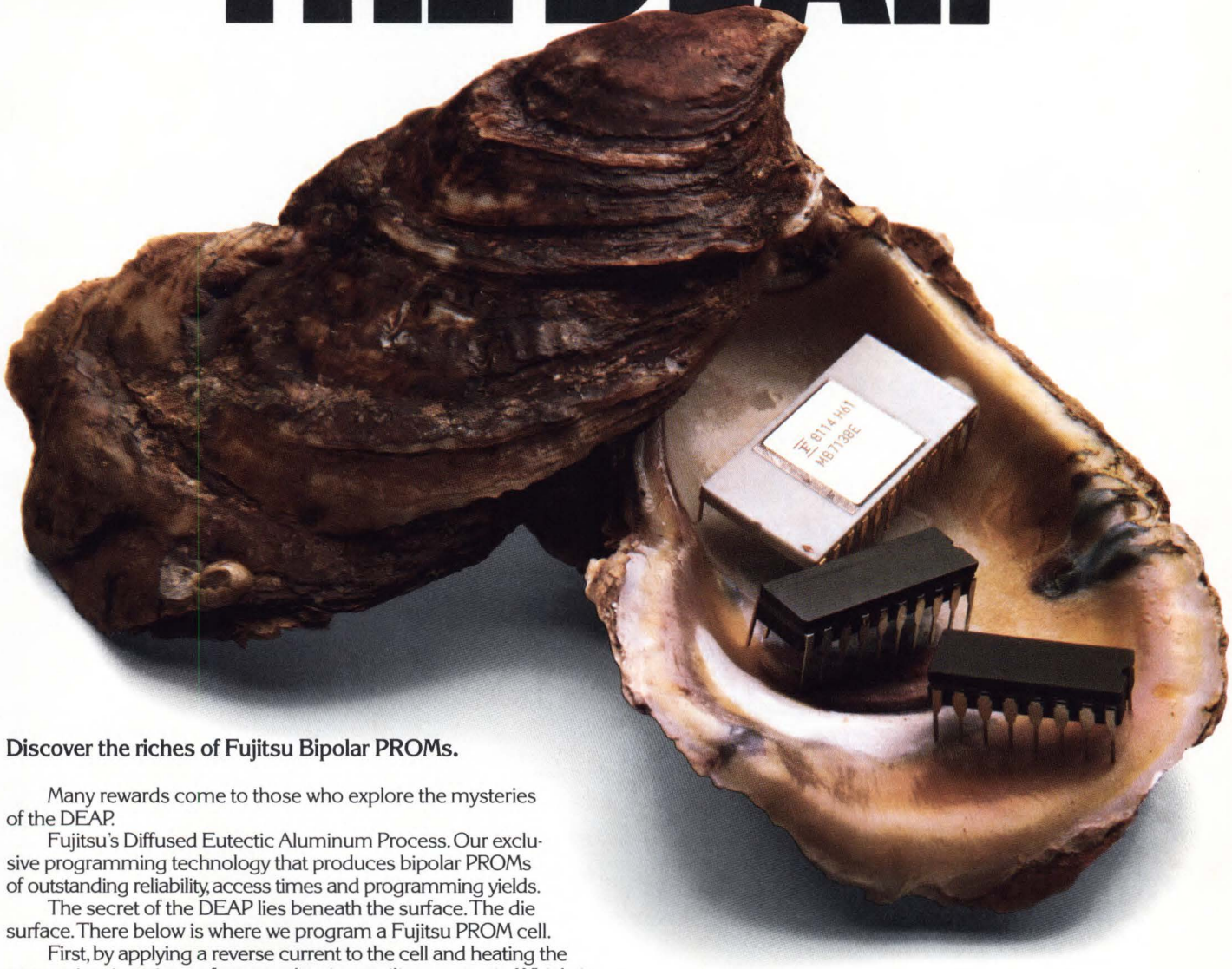
Although the bit streams do not interfere, several transmitters may wish to simultaneously address the same receiving node. The researchers propose inserting a communications processor before each node to manage input queues. Non-von-Neumann architectures, optimized for a Hololink network, should eventually lead to still higher efficiency.



Spatial holograms will be used in a high-speed 'backplane', dubbed Hololink. They direct the beams from an array of transmitting diodes, so they are routed to the proper receivers.

Max Schindler

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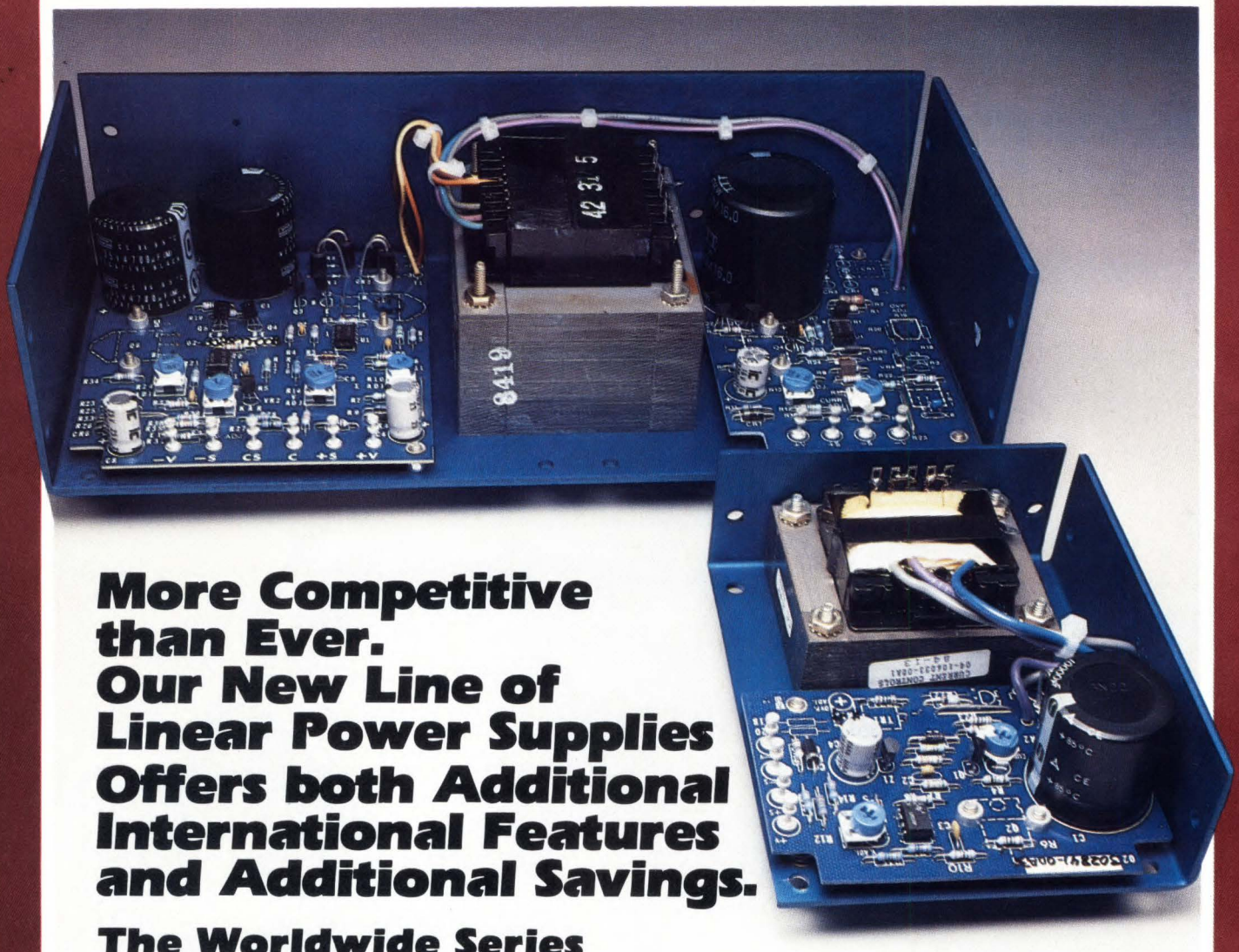
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INTERNATIONAL MEETINGS

Taiwan Electronics Show, Oct. 5–11. Taipei Sungshan Airport, Taiwan. China External Trade Development Council, Taipei Sungshan Airport, Taiwan.

Computer Graphics '84, Oct. 9–11. Conference and Exhibition, London, England. Online Conferences Ltd., Pinner Green House, Ash Hill Drive, Pinner, Middlesex HA5 2AE; (01) 868-4466.

Machine Intelligence '84, Oct. 9–10. Novotel London Hotel, Hammersmith, England. Bob Tracy, Industrial & Trade Fairs, Ltd., Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG; (01) 940-6065.

1984 APL users Meeting, Oct. 15–17. Westin Hotel, Toronto, Canada. Rosanne Wild, I. P. Sharp Associates Ltd., 2 First Canadian Place, Suite 1900, Toronto, Ont., Canada M5X 1E3; (416) 364-5361.

International Symposium on Electromagnetic Compatibility (EMC '84), Oct. 16–18. Hotel Pacific, Tokyo, Japan. Prof. Takagi, EMC '84/Tokyo, Tohoku University, Department of Commerce, Sendai, Japan; 0222-22-1800, ext. 4266.

Internepcon '84, Oct. 16–18. Metropole Exhibition Centre and Brighton Centre, Brighton, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

Software Productivity, Oct. 22–24. Kurhaus Hotel, Scheveningen, the Netherlands. CAM-1, Newfoundland House, Poole Quay, Poole, Dorset BH15 1HJ, England; (0202) 670717.

Orgatechnik Cologne, Oct. 25–30. Cologne, West Germany. Messe- und Ausstellungs-Ges.m.b.H, Koln, Postfach 21 07 60, 5000 Koln 21 (Deutz) (0221) 821-2574.

Comdex/Europe, Oct. 29–Nov. 1. RAI Congress and Exhibition Centre, Amsterdam, the Netherlands. The Interface Group, 300 First Ave., Needham, Mass. 02194; (617) 449-6600 or Riverstaete, Amsteldijk 166, PO Box 7000, 1007 MA, Amsterdam, the Netherlands; (31) 20 460201.

Fairex '84, Oct. 29–Nov. 2. RAI Exhibition Centre, Amsterdam, the Netherlands. RAI Gebouw bv., Europaplein, 1078 GZ Amsterdam, the Netherlands; (0) 20-5411 411.

International Conference on computer Communication, Oct. 30–Nov. 2. Sidney, Australia. P. Davidson, ICCC '84, GPO Box 2367, Sydney, NSW 1001, Australia.

International Test and Measurement Exhibition and Conference '84 (ITAME), Oct. 30–Nov. 1. Olympia 2, London, England. Network Events Ltd., Printer Mews, Market Hill, Buckingham MD18 1JX, England; (0280) 815226.

London Sensors '84, Oct. 30–Nov. 1. Wembley Conference Centre, London, England. Trident International Exhibitions Ltd., 21 Plymouth Road, Tavistock, Devon PL19 8AU; 0822 4671.

Custom Electronics and Design Techniques Show, Nov. 6–8. Heathrow Penta Hotel, London, England. Prodex Ltd., 79 High St., Turnbridge Wells, Kent, England TN1 1XZ; (0892) 39664.

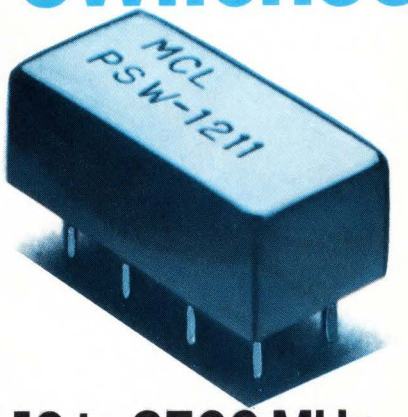
DAK/DAP '84, Nov. 6–9. Info-Rama Centre, Sandvika, Norway. Tor Rustad, Messebyrået AS. Sandviksvn. 184, Info-Rama. Postboks 530, N-1301 Sandvika; 02-39 27 04.

Ergodesign '84, Nov. 6–9. Montreaux, Switzerland. Ergodesign '84, PO Box 122, CH-1820 Montreaux, Switzerland. (021) 63 48 48.

5th Generation Computer Systems, Nov. 6–9. Tokyo, Japan. FGCS '84, Institute for New Generation Computer Technology, Mita Kokusai Bldg., 21F, 1-4-28 Mita, Minato-ku, Tokyo 108 Japan; 03-456-3195.

Computer Peripheral and Small Computer Systems (Compec), Nov. 13–16. Olympia, London, England. Reed Exhibitions, Surrey House, 1 Throwley Way, Sutton, Surrey, England; (01) 643-8040.

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CIRCLE 47

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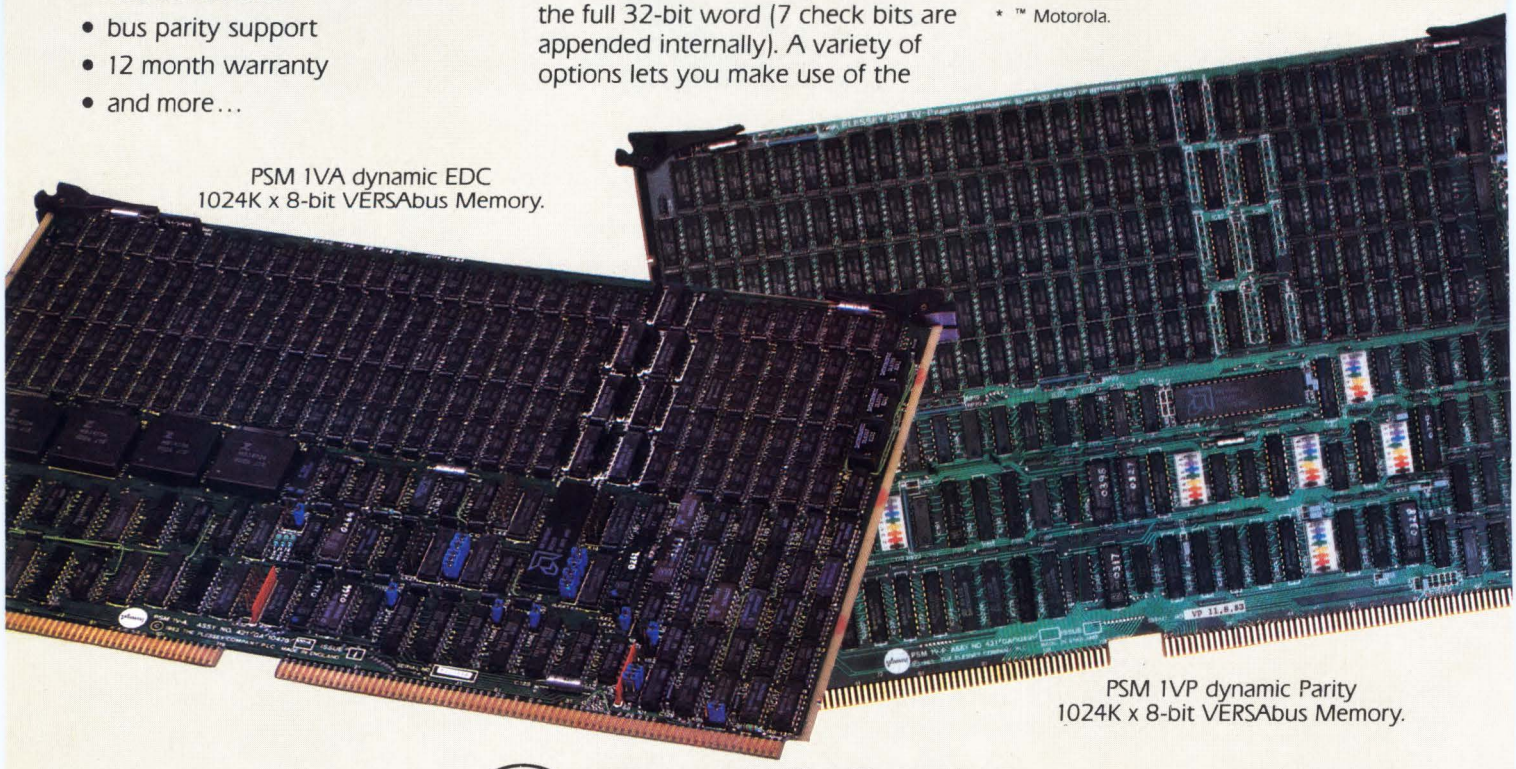
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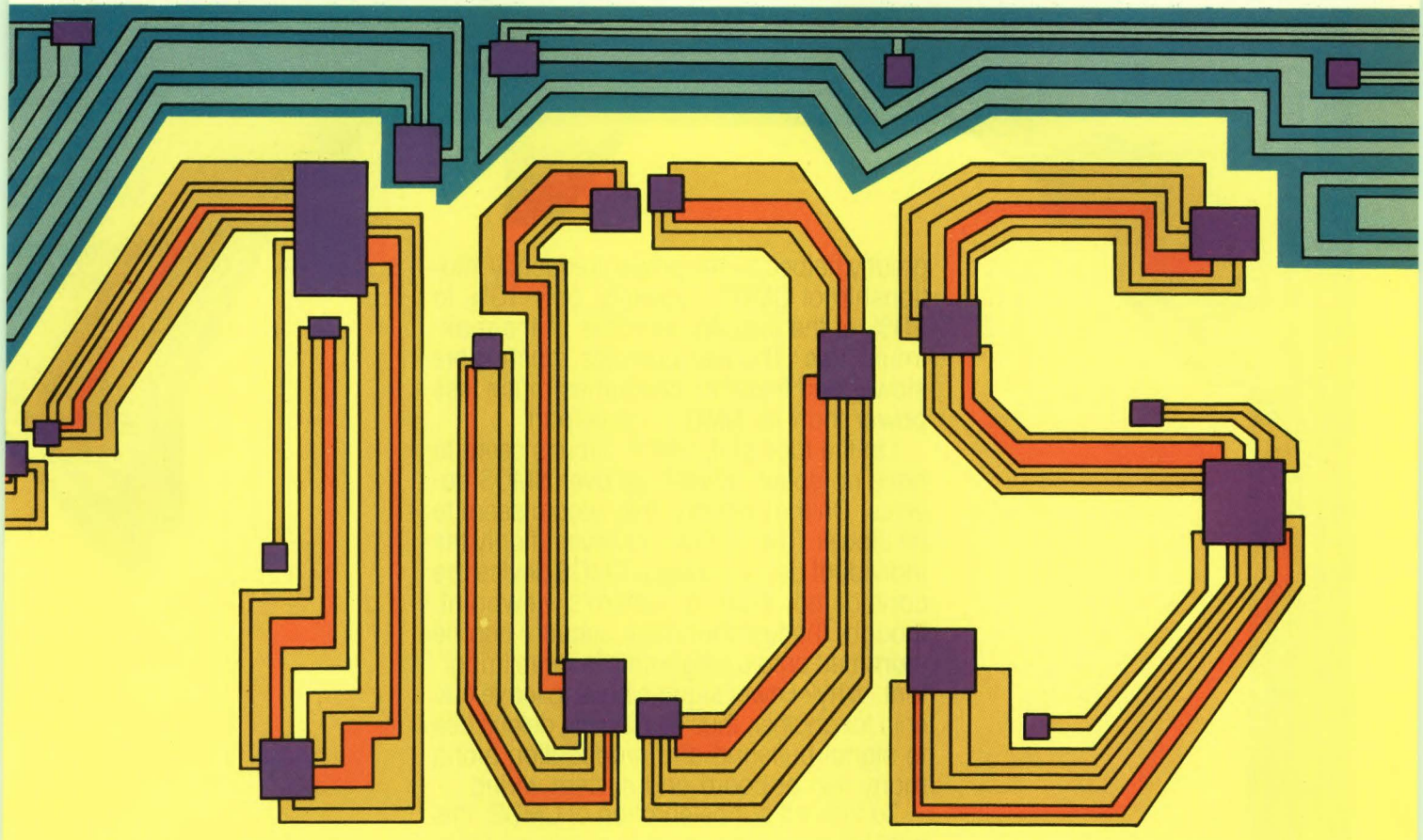
CIRCLE 57



The great takeover: CMOS catches NMOS, prepares to move on

Thanks to its low power consumption, CMOS has come of age – realizing circuit densities too hot for the others to handle. The technology may also prove faster than NMOS because of its density.

Mike Riezenman



CMOS is taking over. Exactly when and exactly how the use of complementary pairs of NMOS and PMOS transistors will become the dominant IC technology is tough to say, but there is no doubt that the mainstream approach for both analog and digital integrated circuits over the short- and medium-term is CMOS.

Although much has been written about why CMOS will take over, it all boils down to one main fact: CMOS uses very little power. In fact, it is almost true that digital CMOS circuitry uses no power at all except when changing states. The importance of low power consumption is obvious in the design of battery-operated portable equipment. It is just as meaningful, although not quite as apparent, in the design of almost everything else.

Briefly, IC fabrication techniques have reached the point where it is possible to squeeze several hundred thousand transistors onto a chip. Bipolar and NMOS chips with that many active devices dissipate several watts of power, which rules out housing them in inexpensive plastic packages and necessitates going with expensive ceramics (see the figure). CMOS chips of equivalent complexity, though, may only consume 500 mW — a comfortable level for many low-cost packages. Moreover, as chip complexity continues to rise, even standard ceramic packages will prove inadequate, leaving CMOS as the only economically sensible alternative.

Actually, at least for digital CMOS, power consumption depends on the frequency at which the circuit operates — the lower the frequency, the lower the power.

As a result of the relationship between power consumption and frequency, manufacturers tend to minimize operating frequencies whenever they can. In a real-time clock, for example, a time base of about 32 kHz is often used to keep the active power consumption to just a few microwatts.

Even a complex circuit like a microprocessor with a multimegahertz oscillator is

greatly helped by the power-frequency relationship of CMOS. Typically, only 10% to 20% of the circuitry switches at the maximum rate. The rest operates much more slowly and therefore consumes much less power than its NMOS counterpart.

On the face of it, CMOS circuits seem to have no speed advantage over NMOS devices. On the contrary, they would seem to be slower. That is true, however, if only the individual delays of each CMOS device are considered. From a system's viewpoint, though, the fact that more circuitry can be crammed onto a single chip is more important. Why? Fewer signals have to leave one chip for another, thus eliminating delays due to signal buffering and propagation along many feet of board and system wiring.

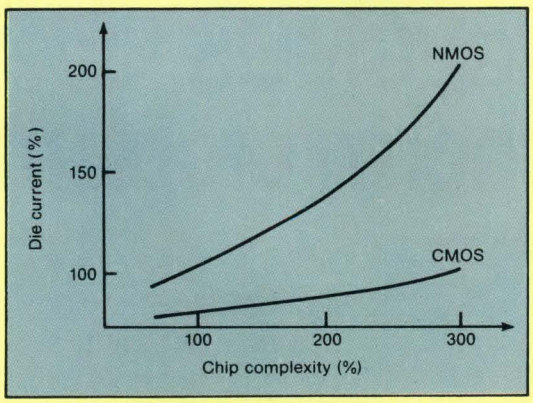
To kick off our celebration of CMOS, this special issue begins with a pair of Technology Reports, one on digital circuitry, the other on analog. These reports focus in on the technological barriers that are keeping CMOS from reaching its potential and discuss what various manufacturers around the world are doing to overcome them.

Twin-well processes, which allow the individual p- and n-channel devices to be optimized independently of each other, are a major trend, as is the use of refractory-metal gates. These are made of such metals as tungsten and molybdenum and combine the advantages of conventional aluminum-gate technology with that of silicon gates — namely, low resistance and the ability to withstand high-temperature processing. The result: self-aligned metal-gate structures with the unique combination of low resistance, high density, and low parasitic capacitance.

To get a personal perspective on the fu-

ture of CMOS and of CMOS-based products, our technology package includes interviews with a dozen movers and shakers in the world of CMOS, some of whom have been there since the early days. Although these people all agree on the great importance of CMOS technology, their beliefs are not based on identical reasoning. Some emphasize its low power consumption, some its excellent noise immunity, and others its ability to easily integrate analog and digital functions on one chip. Some talk about its applicability to memories, some to data converters, and some to the booming area of telecommunications. They do hold one thing in common, however: important as it already is, CMOS will be even more important just a short way down the road.

Rounding out our CMOS special is a collection of six Design Entries, each of which introduces a new CMOS product. These include both analog and digital devices and both mixed and straight CMOS circuits. They range from a clock controller to a digital signal processor and from an analog switch to a static RAM.



As circuit complexity increases, NMOS power consumption rises to levels that will eventually prevent further growth. In contrast, CMOS power consumption increases only slightly as chip size increases.

The controller enhances the attractiveness of static CMOS systems by supplying three operating modes: slow, stop clock, and stop oscillator and clock. These allow system designers to take advantage of CMOS's power-frequency relationship to save power by either slowing down or shutting down selected portions of their circuitry. The technique is, of course, only applicable to static circuitry, which can operate down to dc without losing data.

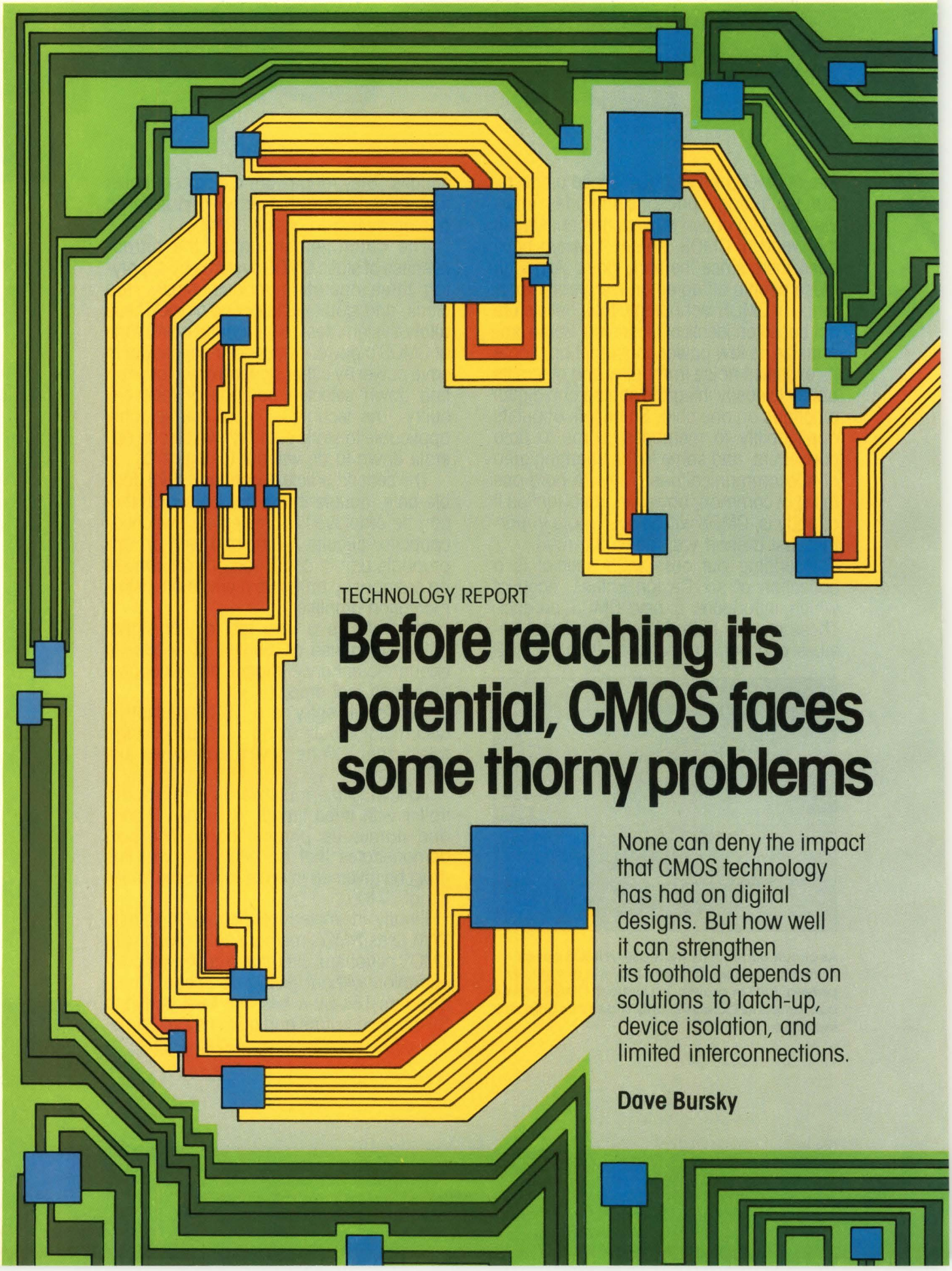
The second article describes a dual double-pole, double-throw analog switch that can be employed to implement switched-capacitor circuits. Combined with an appropriate pair of capacitors, it can convert an ordinary op amp into a precision instrumentation amplifier.

Next comes a very fast digital signal processor aimed at robotics. It is speedy enough to enhance images and recognize objects in real time.

Our fourth entry is a 16-bit multiplier-accumulator built using 1.25-μm design rules. The 100-ns device consumes just 400 mW.

Following the multiplier is a microcontroller with three timers, a serial I/O port, and numerous parallel ports. The part demonstrates that no bells and whistles must be given up in order to reap the benefits of CMOS.

Finally, the mixed-technology 64-k static RAM uses NMOS memory cells along with CMOS peripheral circuitry to cut power consumption without giving up speed. Organized as 16k-by-4 bits, the RAM boasts a 35-ns access time and a 55-ns cycle time.

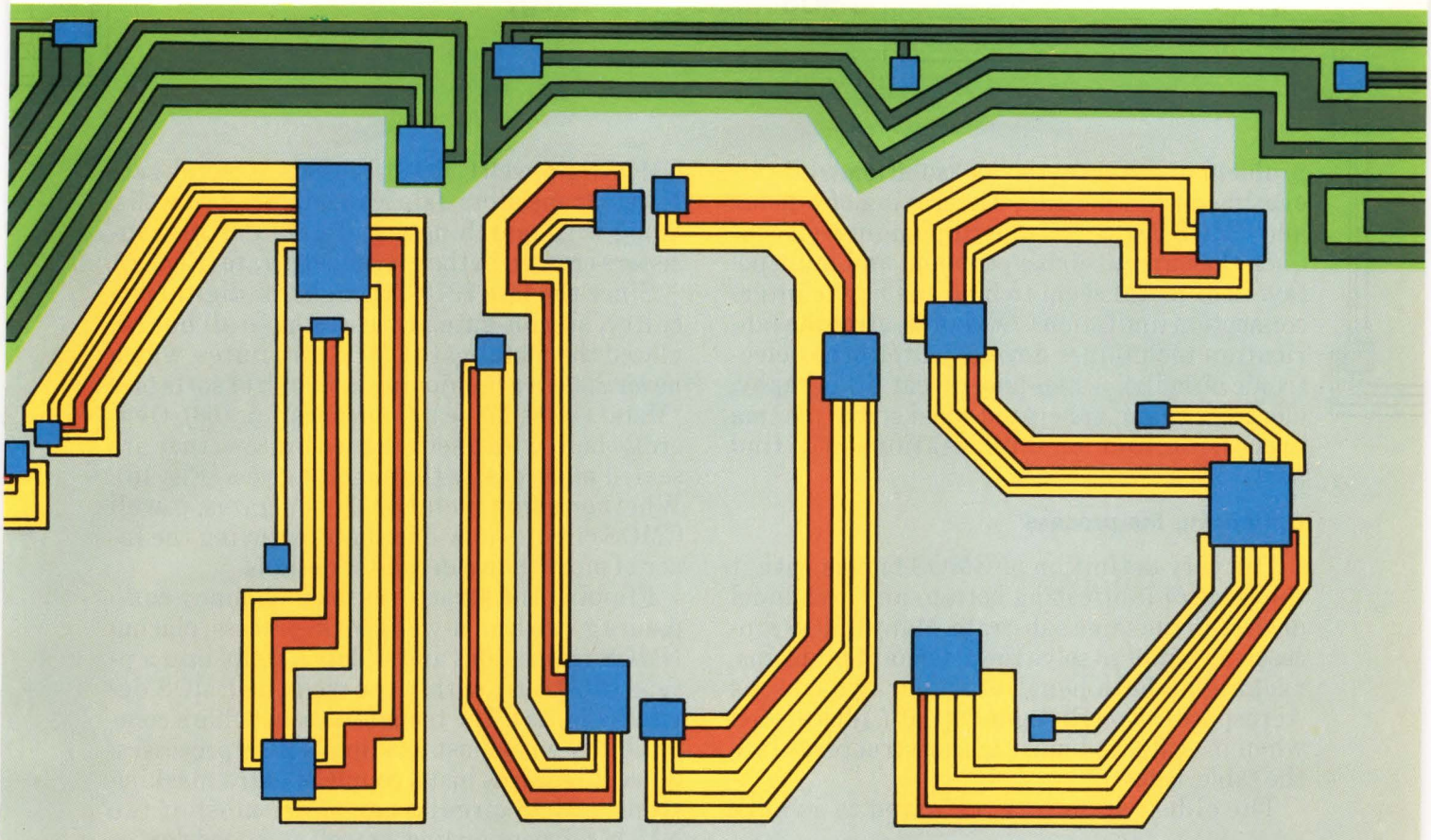


TECHNOLOGY REPORT

Before reaching its potential, CMOS faces some thorny problems

None can deny the impact that CMOS technology has had on digital designs. But how well it can strengthen its foothold depends on solutions to latch-up, device isolation, and limited interconnections.

Dave Bursky



Over the past years digital CMOS technologies have emerged that now rival the performance and density of NMOS-only fabrication processes. But while NMOS now faces a heat-dissipation barrier that may limit its future density growth, CMOS jumps right over that obstacle — thanks to its low power consumption. As a result, CMOS circuits like 256-kbit dynamic and static RAMs, 16- and some 32-bit microprocessors, and random logic circuits with 10,000 gates are making their debut.

So confident are manufacturers that the technology will dominate the digital logic arena that many have stated for the record that they plan no more NMOS-only circuits. Future designs will be either all-CMOS or mixed-MOS, in which CMOS circuits are sprinkled strategically (in the higher-power portions of the circuitry) throughout a mostly NMOS design.

Yet, even in the bright land of CMOS, all is not perfect. Some problems remain to be solved.

- The fundamental nature of CMOS circuitry — a combination of n- and p-channel transistors — means that the manufacturing process is less than optimum for one of those device types.
- Latch-up, the unwanted triggering of intrinsic pnpn structures, must be dealt with.
- Inadequate isolation of adjacent devices threatens to worsen as densities climb.
- The output current-drive capability of a CMOS circuit is often insufficient when compared with that of NMOS and especially bipolar devices.
- Higher densities demand greater numbers of interconnections. The ability to wire together the devices on a chip will supplant the concern with fitting all the devices onto the chip.

Of course, these difficulties must be surmounted if CMOS is to fulfill its promise of being the mainstream digital technology of the late 1980s. Already, many laboratories around the world are addressing those problems, with twin-well designs responding to transistor optimization and with epitaxial layers on wafers and retrograde well structures tackling the issue of latch-up. Various forms of silicon-on-insulator and trench isolation — teamed with a finer-line lithography — are cracking the

problem of adjacent device isolation while elevating circuit density. The mixing of bipolar and CMOS devices on one chip might well conquer the current-drive problem, and multiple layers of metal seem to hold the key to interconnection limitations. Of course, all of the fabrication techniques developed for other electronic circuitry—step-and-repeat lithography, electron-beam-generated masks, dry plasma processing, and ion implantation—will find new work as well.

Optimizing the process

The very definition of CMOS brings with it the issue of fabricating both p- and n-channel devices in the same substrate. Many CMOS processes attempt to solve the attendant problems, racking up both benefits and drawbacks, as Aerospace Corp. (El Segundo, Calif.) discovered when it evaluated most major structures (see the table, below).

The oldest structure, referred to as bulk CMOS (or p-well CMOS), consists of metal-gate NMOS transistors, fabricated in p-doped wells, along with matching metal-gate PMOS transistors created in the n-type substrate (Fig. la).

Since the late 1970s, though, for digital circuitry, silicon-gate processes have all but replaced the metal-gate CMOS structures, which nevertheless are enjoying a rebirth of sorts (see "Metal Gates Make a Comeback," p. 108). Generally built with a self-aligned process, they are scaled more easily than metal gates (Fig. lb). Whether using metal or silicon gates, p-well CMOS circuits now dominate, enjoying the favor of more than a decade of designs.

Flipping the structures around, many companies go with an n-well CMOS process, placing NMOS transistors and n-doped wells into a p-type substrate; within the wells lie PMOS devices (Fig. 2a). The technique boasts high compatibility with most existing NMOS processes: Since it requires just a couple of extra masking steps, CMOS circuits can share most of the NMOS fabrication line, as well as a good deal of the processing advances applied to NMOS structures.

How CMOS technologies stack up

Generic features	Circuit density	Process simplicity	Speed	Radiation hardness: Latch-up	Radiation hardness: Transient	Radiation hardness: Soft error	Radiation hardness: Total dose
Bulk							
P well, metal gate	1	3	2	1	1	1	3
P well, polysilicon gate	2	2	1	1	1	2	1
P well, polysilicon gate, oxide isolated	3	2	2	1	1	2	1
N well, polysilicon gate*	2	2	1	1	2	2	2
Twin-well, polysilicon gate, epitaxial*	1	1	2	2	3	3	2
Thin film							
Silicon on sapphire	3	3	3	3	3	3	2
Silicon on insulator**	3	2	3	3	3	3	2

Approximate relative merit, 3 = high, 1 = low. Special designs strongly affect merit values, particularly with regards to radiation hardness.

* Only one variant each of n-well and twin-well technologies is categorized; other variants are similar to p-well variants.

** Still experimental; scores represent expectation.

Source: Aerospace Corp.

Two tubs are better than one

In either the p- or the n-well CMOS process, one transistor type is less than optimum because of tradeoffs made during fabrication. A third method—called twin tub, twin well, or dual well—optimizes both transistor types, since it embeds precisely doped p and n wells in an n-type substrate and then implants ions to create the best doping for the drain and source (Fig. 2b). Twin-well processing is more complex than the p- and n-well processes but pays off in its greater immunity to alpha particles and its better noise margins.

The strong immunity to alpha particle strikes comes about because each transistor sits in its own well, protected against electrons that are being scattered by alpha hits elsewhere on the chip. Similarly, having each device sitting in its own well isolates the devices from substrate noise.

Twin-well and n-well CMOS structures will prevail for the next few years. Both structures will benefit from their compatibility with existing, highly refined NMOS processes. Not only

will they be dense as a result, they will be fast too, lending themselves to building logic devices and microprocessors with on-chip memory. The twin-well structure, in particular, promises extremely high packing densities, as it eliminates the need for the oversized p-channel devices that normally compensate for less-than-optimum doping.

Many industry experts expect that the separate twin-well and n-well processes will merge by the late 1980s. However, neither structure is invulnerable to the failings of the older processes—latch-up and device isolation remain concerns.

Catching up with latch-up

With structures plunging below 2-μm and devices being squeezed closer together, the gain of the incidental, between-the-well pnpn structures increases. Noise or unexpected voltage transients can cause the pnpn structures to turn on and stay on (latch), enabling large currents to flow and possibly burn out the circuit.

Minimizing the number and the gain of the incidental devices can avoid latch-up. But it may not be enough, especially when high voltages are present on a chip's I/O lines or are being generated on chip for programming purposes, as in the case of EPROMs and EEPROMs.

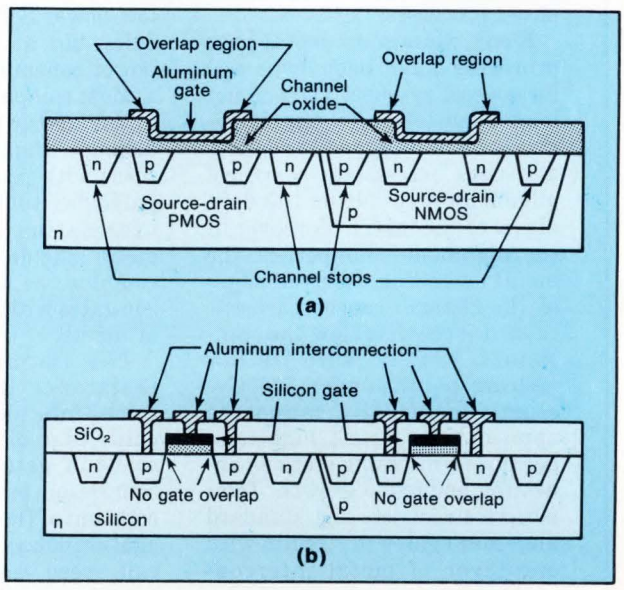
Several alternatives reduce the likelihood of latch-up. One in particular forms retrograde well structures using deep boron implants. In the technique, developed by TRW Inc.'s LSI Products Division (La Jolla, Calif.), boron defines the regions for the n-channel transistors and also serves as a field-isolation guard band that minimizes leakage between transistors (ELECTRONIC DESIGN, Sept. 6, 1984, p. 37). Furthermore, the process cuts the current gain of the pnpn structures by a factor of 10 compared with conventional p-well processes.

Strong showing for epitaxial layers

As the strongest remedy for latch-up headaches, almost every company hedges its bets by preparing a process that builds wells in an epitaxial silicon layer on the wafer (Fig. 3). Since the epitaxial layer is of very high purity, its resistivity is high, lowering the gain of the pnpn structures. Moreover, that high resistivity permits a low resistivity substrate material to pave a good path to ground for noise. The powerful duo—low gain and good grounding—prevents anything but extraordinarily high voltages from triggering latch-up in pnpn structures.

Improved hardness to radiation is another benefit of the use of epitaxy. In a technology development program Sandia Laboratories (Albuquerque, N.M.), developed a radiation-hard epi-based CMOS process, and recently transferred it to the Semiconductor Group of Harris Corp. (Melbourne, Fla.). Along with the process, Sandia developed a CMOS version of the Intel 8085 and its set of peripheral support chips (ELECTRONIC DESIGN, Aug. 9, 1984, p. 46). The parts can withstand radiation dose levels of up to 10^5 rads.

Once a manufacturer goes with epitaxy to avoid latch-up, a natural next step might be to exploit the epitaxial layer for better adjacent-device isolation. How? By growing the layer over selected portions of the wafer instead of



1. The oldest CMOS structure, the p-well aluminum gate process places aluminum over the channel oxide to form the transistor gate (a). However, the metal cannot be easily aligned with the channel when dimensions shrink. Most manufacturers have since substituted polysilicon, which can be deposited using a self-aligned process to create extremely small features (b).

over the entire surface. The process is extremely difficult, however, since it often requires high temperatures to form the epitaxial layer, and no epi layer should grow atop the oxide-protected regions. To deal with these problems, RCA Corp.'s Solid-State Division (Somerville, N.J.) is now looking at multiple growth and partial etch-back cycles to create isolated epitaxial silicon islands. The process is in the early experimental stages and will not likely become commercially viable until the early 1990s.

Another technique, which bears some resemblance to what RCA is doing, sequentially deposits silicon dioxide on a wafer, opens windows in the oxide, caps the wafer with silicon nitride, and re-etches the window regions, thus leaving regions of silicon dioxide protected by silicon nitride sidewalls. Epitaxial silicon can grow in the areas between the protected regions, which isolate the epitaxial islands. NEC Corp. (Kanagawa, Japan) has applied the process to some simple CMOS gate structures in which the epitaxial layer houses not only an n-

Metal gates make a comeback

New digital designs rarely opt for the original form of metal-gate CMOS. The process has given way to a higher-performance but higher-resistance technique that uses silicon gates. Nevertheless, new forms of metal gates are appearing, including refractory metals and refractory-metal silicides, as well as low-temperature aluminum-based processes.

Early aluminum metal-gate processes have been bypassed for several reasons: They do not lend themselves to the fabrication of self-aligned structures and thus necessitate a critical alignment step during the definition of the metal. Moreover, if the alignment is not perfect, the metal extending over the edges of the channel causes parasitic capacitances that slow the transistors. Finally, with its low melting point—under 500°C—aluminum usually cannot be applied before such high-temperature processing steps as annealing and oxide growth. Temperature restricts the standard aluminum gates to circuits with one layer of metal interconnections and thus limits its use to relatively low-density circuits.

To solve part of the problem, one company—Zytrex Corp. (Sunnyvale, Calif.)—combines a proprietary two-level aluminum-based process with low temperatures and 2-μm feature sizes. The technique builds CMOS logic circuits that have I/O delays rivaling those of low-power Schottky bipolar circuits, but at a fraction of the power consumption.

Most companies, however, are attacking the limitations of traditional aluminum-gate structures with refractory metals or polycides (polysilicon with an overcoating of a refractory-metal silicide). These materials combine the advantages of silicon gates with the low resistance of metal.

The importance of low-resistance interconnections comes into play with the VLSI chips that boast tens of thousands of gates and long interconnection paths. The RC time constant of the path causes propagation delays that limit the circuit speed more than does the actual switching speed of the transistors.

Because of their high melting points, refractory metals can survive subsequent processing steps that bring temperatures up to 700°C. Steps for self-alignment and silicon-on-insulator structures can now be readily added to the manufacturing process.

The metal silicides and pure metals are being put to work as contact barriers for the shrinking source and drain regions of VLSI circuits. A barrier serves two purposes: First, it lowers the contact resistance of the shallow junction; second, it protects against aluminum spikes, which might diffuse through the junction and short-circuit the overlying aluminum interconnection to the substrate. In addition, new designs of silicide or pure metal-gate structures are now lowering the gate contact resistance.

Which of these metal or silicide combinations will be the winner is anyone's guess. Most of the materials are all good candidates. The choice depends on which one will be most compatible with a manufacturer's fabrication process.

channel device but also a p-channel device resting in an n-well.

Perhaps the best news of all about epi layers comes from Fujitsu Laboratories Ltd. (Atsugi, Japan), which is growing epitaxial silicon at 630°C—a relatively low temperature compared with the 1000°C now commonly needed. The technique combines disilane gas (Si_2H_6) and high-power ultraviolet light, but the layer now grows far too slowly (0.001 μm/minute) to be of commercial interest.

SOS to the rescue

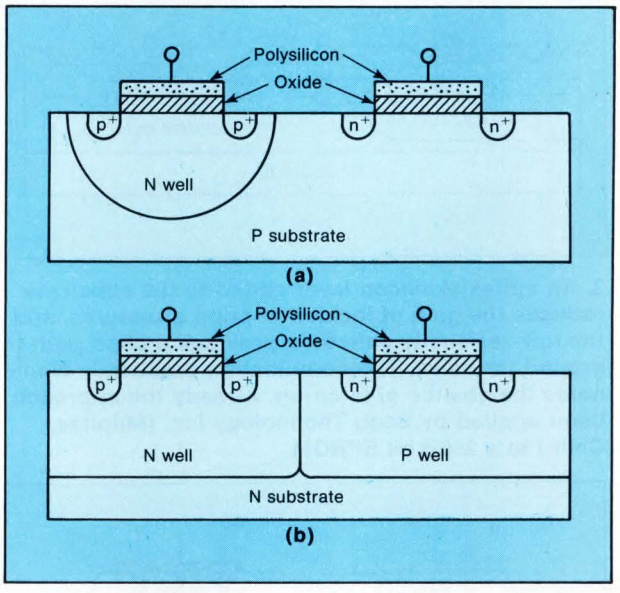
For more than a dozen years, epi layers on sapphire substrates have been protecting against latch-up and providing adjacent-device isolation (Fig. 4). However, the high cost of producing the sapphire substrates and manufacturing losses have kept volume relatively low. Generally speaking, an insulating substrate like sapphire helps reduce transistor and circuit parasitic capacitances and raises the level of radiation hardness (to more than 10^7 rads). That combination renders silicon on sapphire (SOS) suitable for extremely fast military and aerospace system applications.

To improve the silicon-sapphire interface, increase electron mobility, and cut back reverse leakage currents, Hughes Aircraft Co. (Newport Beach, Calif.) is battling lattice mismatching with recrystallization. In a customary SOS structure, the lattice between the silicon and the sapphire is mismatched, a fact that diminishes electron mobility and hikes leakage current.

Hughes first grows a thin epitaxial layer of silicon on the sapphire, then converts the monocrystalline silicon into amorphous form by implanting silicon ions in it. Afterward it cultivates a second epitaxial layer on the amorphous silicon. As the new epi layer grows, the amorphous silicon is annealed. Hughes finds that it can match lattices almost perfectly and raise mobilities to within 10% of those achieved with bulk silicon. Moreover, the lattice matching slashes reverse leakage currents by 50% to 100% over previous SOS endeavors. Still experimental, Hughes hopes to transform the technique into a production-viable process for the Department of Defense's VHSIC project.

The continued refinement of SOS technology not withstanding, many experiments are producing active devices in silicon layers that are subsequently deposited atop other insulating materials—spinel or silicon dioxide, for instance. Other techniques either place an insulating layer below the surface layer of the silicon or create device-quality silicon above an insulator. With the same benefits as SOS, these oxide techniques offer the potential of a much lower chip cost—if the production problems can be licked.

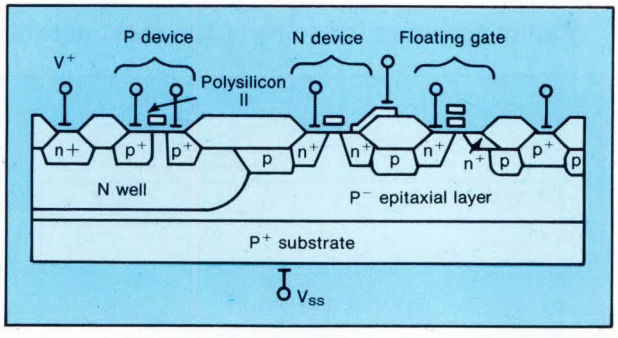
Japan accounts for some of the most notable



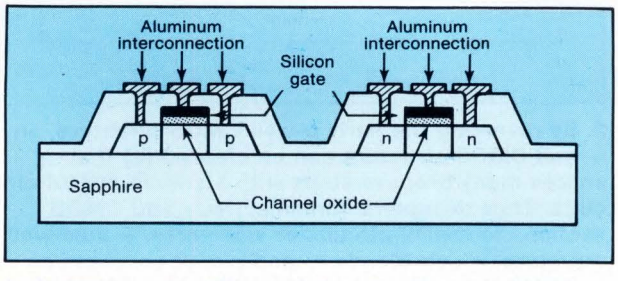
2. By reversing the early p-well CMOS structure, an n-well CMOS structure can be created (a) that shares many process steps with standard NMOS circuits. Thus designers can selectively add CMOS sections to NMOS circuits or vice versa. A dual-well structure, which blends n- and p-well concepts on one chip (b), can optimize both transistor types and thus raise the circuit performance.

work. At NEC Corp. Researchers have grown a double hetero-epitaxial structure in which spinel grows on a silicon wafer, then silicon atop the spinel. Hitachi Ltd. (Kokubunji), Fujitsu Laboratories Ltd. (Atsugi), and Nippon Telegraph and Telephone Public Corp. (Atsugi) have developed processes that form insulating silicon-dioxide layers beneath the transistor regions.

NEC's approach indicates that for 3-μm-thick silicon layers, the spinel insulator produces higher-mobility channel electrons than possible through SOS. In addition, better matching of the crystal structures puts little if any stress on the epitaxial silicon layer. By the time the process makes it out of the lab—several years at least—the processing must be sufficiently streamlined to deposit the spinel, oxidize the silicon through it, and then grow the layer of epitaxial silicon in an acceptably short length of time.



3. An epitaxial silicon layer added to the substrate reduces the gain of incidental pnpn structures, and the low-resistivity substrate provides a good path to ground for noise. The combination practically eliminates the chance of latch-up. Already the approach been applied by Seeq Technology Inc. (Milpitas, Calif.) to a 256-kbit EPROM.



4. Covering a sapphire substrate with an epitaxial silicon layer eliminates many of the parasitic capacitances found in CMOS circuits. The structure, pioneered by RCA, consumes very little operating power and affords good hardness to radiation—two desirable features for military and aerospace applications.

Fujitsu's process depends on the high powered implantation of oxygen ions in the substrate, followed by an annealing cycle that permits the ions to combine with the silicon, thus forming a silicon-dioxide layer beneath the transistor region. The scheme is now limited by the lack of high-power machines that can shoot the oxygen ions into the silicon.

Texas Instruments (Dallas) has a similar process (Fig. 5) with which it has developed an experimental 4-kbit static RAM. The memory, built with 2.5-μm design rules, can access data in just 55 ns.

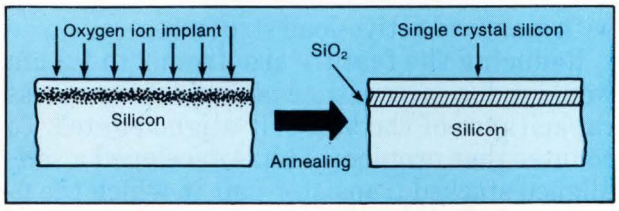
Oxygen gives fast results

The route taken by NTT differs somewhat. The company chemically alters selected areas on the silicon's surface layer, turning them into porous regions that are subsequently exposed to oxygen, which is absorbed easily. The material surface is then treated to remove its porosity, thereby trapping the oxygen under the surface. The oxygen blends with the silicon to form silicon dioxide; thus, devices fabricated in the surface regions are isolated from the substrate.

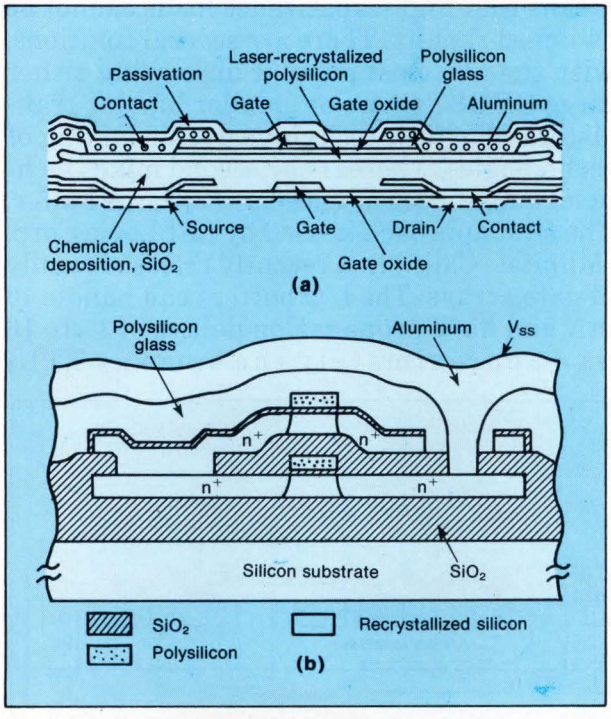
The process, dubbed Simox (for separation by implanted oxygen), has built a 1-kbit static RAM that boasts a 12-ns chip-selection time and consumes just 45 mW. Both features can be attributed to the high-quality silicon placed above the buried oxygen layer and the reduced parasitic capacitance of the pn junction. The process also proves valuable for high isolation voltages: It has produced an analog CMOS chip that can handle as much as 60 V.

Lasers are favored

Of the experimental thermal techniques for producing silicon-on-insulator circuits, laser annealing has been the most thoroughly



5. If oxygen atoms are propelled with sufficient force into a silicon substrate, they can form a submerged layer of silicon dioxide after annealing. The formed layer separates the surface from the rest of the substrate, so that transistors can be built in an isolated region.



6. Three-dimensional ICs are coming closer to reality. Mitsubishi puts one layer of transistors in the substrate, then covers the devices with silicon dioxide and polysilicon (a). The polysilicon is then laser-annealed and another layer of active devices created in the annealed silicon. Using a different approach, Fujitsu first coats the substrate with silicon dioxide to isolate the next, polysilicon layer (b). After annealing, transistors are fabricated, and the process repeats to form a second layer of active elements.

studied and is the most widely used. Some laser-annealed circuits could well work twice as fast as similar ones made with standard processes.

In an advanced experiment, researchers at Mitsubishi Electric Co. Ltd. (Itami, Japan), have created a silicon-on-insulator structure with two independent stacked layers (Fig. 6a). The first layer of active devices holds n-channel transistors, which are fabricated in the substrate and then interconnected with phosphorous-doped polysilicon instead of aluminum so that they can withstand the heating when the next layer is annealed. After the polysilicon layer is laid down, silicon dioxide, polysilicon, and silicon nitride are sequentially deposited; the nitride is then etched into long stripes. Those stripes create a coating that controls the thermal profile while the underlying polysilicon is laser-annealed into single-chrystal form in 15-μm-wide stripes. In the single-crystal regions, n- and p-channel transistors can then be created.

Preliminary results reveal that the crystal quality of the silicon-on-insulator is the same as that of the substrate, and even more important, that the performance of the lower-layer transistors does not degrade during processing. To check the performance, a comparison of a 31-stage NMOS ring oscillator in the substrate with a CMOS equivalent in the silicon-on-insulator was carried out. The CMOS inverters yielded propagation delays of about 500 ps and dissipated about 1 mW; the NMOS units were about 200 ps slower and consumed about five times the power.

Entering another dimension

Similar work—with a twist—is under way on three-dimensional gate arrays. Fujitsu Ltd. (Kawasaki, Japan) lays down oxide and polysilicon on the bare substrate, recrystallizes the polysilicon with a laser, and afterward creates standard CMOS structures in the annealed single-crystal material. Following that, it deposits another layer of oxide and polysilicon, anneals it again, and creates a second set of devices with independent gates (Fig. 6b).

The annealing conditions for the lower and upper layers are quite different—the lower layer uses an 11- to 12-W continuous-beam argon

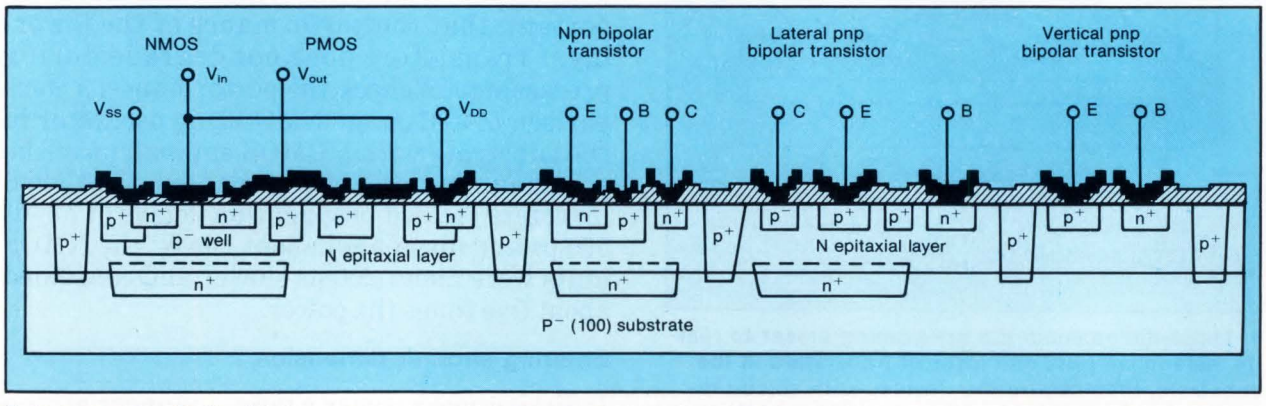
laser and a 450°C substrate temperature, giving a melt width of 60 to 80 μm. The upper layer works with lower power levels—just 5 to 6 W—to reduce thermal stress on the buried CMOS circuits and a 300°C substrate temperature, yielding a melt width of 30 to 60 μm. To demonstrate the technique's effectiveness, a ring oscillator built with two-input NAND cells and 2-μm minimum features exhibited propagation delays of only 420 ps per stage.

To date, the largest circuit yet fabricated in stacked CMOS is a 64-kbit static RAM from Texas Instruments. The memory uses active loads, which reduces its susceptibility to soft errors. Fabricated with 2-μm features, it can be accessed in just 85 ns and consumes a low 350 mW.

The memory's p-channel load transistors were fabricated in polysilicon above the n-channel transistors, resulting in a non-self-aligned structure with a cell size of 307 μm^2—comparable to that of cells fabricated with polysilicon loads. Moreover, the memory performance comes close to that of units built with standard active-load structures.

Reducing the feature size from 2 to 1.5 μm would reduce access time because of the excess capacitance of the non-self-aligned gates. To counter that problem, TI has developed a self-aligned stacked transistor pair in which the p-channel load devices are fabricated on the sidewall of the self-aligned transistors.

Despite this work on stacked structures and other means for increasing packing density, the problem remains of what to do when signals must go off the chip. CMOS's low-power nature means that high-capacitance loads cannot be switched rapidly. There are several solutions, with the two most popular ones using either large CMOS drivers or smaller bipolar transistors. The first technique avoids mixing of technologies, whereas the second mixes technologies but does not need a very large buffer. The first approach is used by LSI Logic Corp. (Milpitas, Calif.) in a recently released family of gate arrays. The I/O buffers can handle 10 mA and have propagation delays of 11 to 16 ns—approximately the same as TTL-



7. In response to the high output-current drive needed in circuits that combine logic and power, Ricoh created a structure that mixes CMOS with vertical npn transistors, as well as with lateral and vertical pnp devices, thus permitting the designer to pick the best circuit approach. Ricoh uses the bipolar-CMOS technique to drive thermal print heads.

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compatible bipolar drivers.

Taking the second approach, Ricoh Co. Ltd. (Osaka, Japan) combines lots of logic with some high-power transistors for driving the elements of a thermal print head. The technique merges an epitaxial-based p-well structure for the logic with isolated vertical npn and both lateral and vertical pnp transistors, which withstand the high currents and voltages—20 to 40 mA at between 15 and 20 V—that heat up the printing elements (Fig. 7). N^+ buried layers improve the characteristics of both the n-channel MOS transistor and the vertical npn and the lateral pnp transistors.

A good mix

From another angle comes Motorola Inc. (Mesa, Ariz.), which combines bipolar and CMOS circuitry but without an epitaxial layer. Workers at the company's Research Labs take advantage of an n-well double-metal CMOS process and 2-μm feature sizes (Fig. 8). The bipolar device incorporates a walled-emitter structure with polysilicon emitters and very shallow base and emitter junctions.

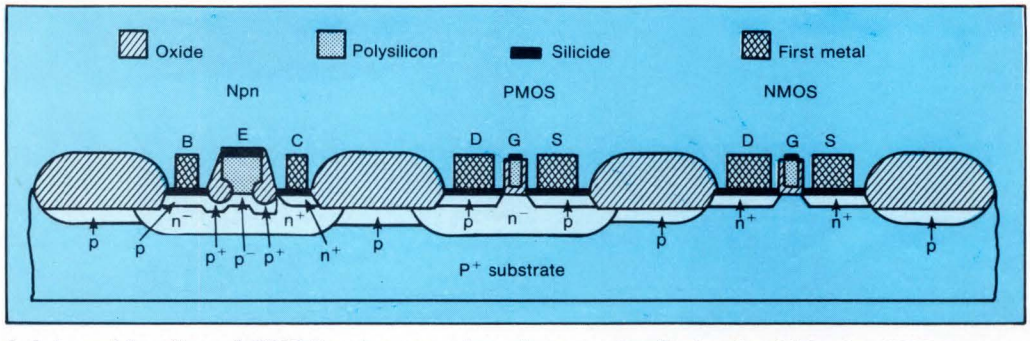
Mixing the bipolar transistors with CMOS logic structures shortens propagation delays considerably and permits internal functions to have higher fan-outs without slowing down. For contrast, consider that the propagation delay of a CMOS inverter degrades about 1.3 ns per picofarad of load whereas that of the bipolar-CMOS inverter degrades just 0.35 ns.

Mixed cells cut power

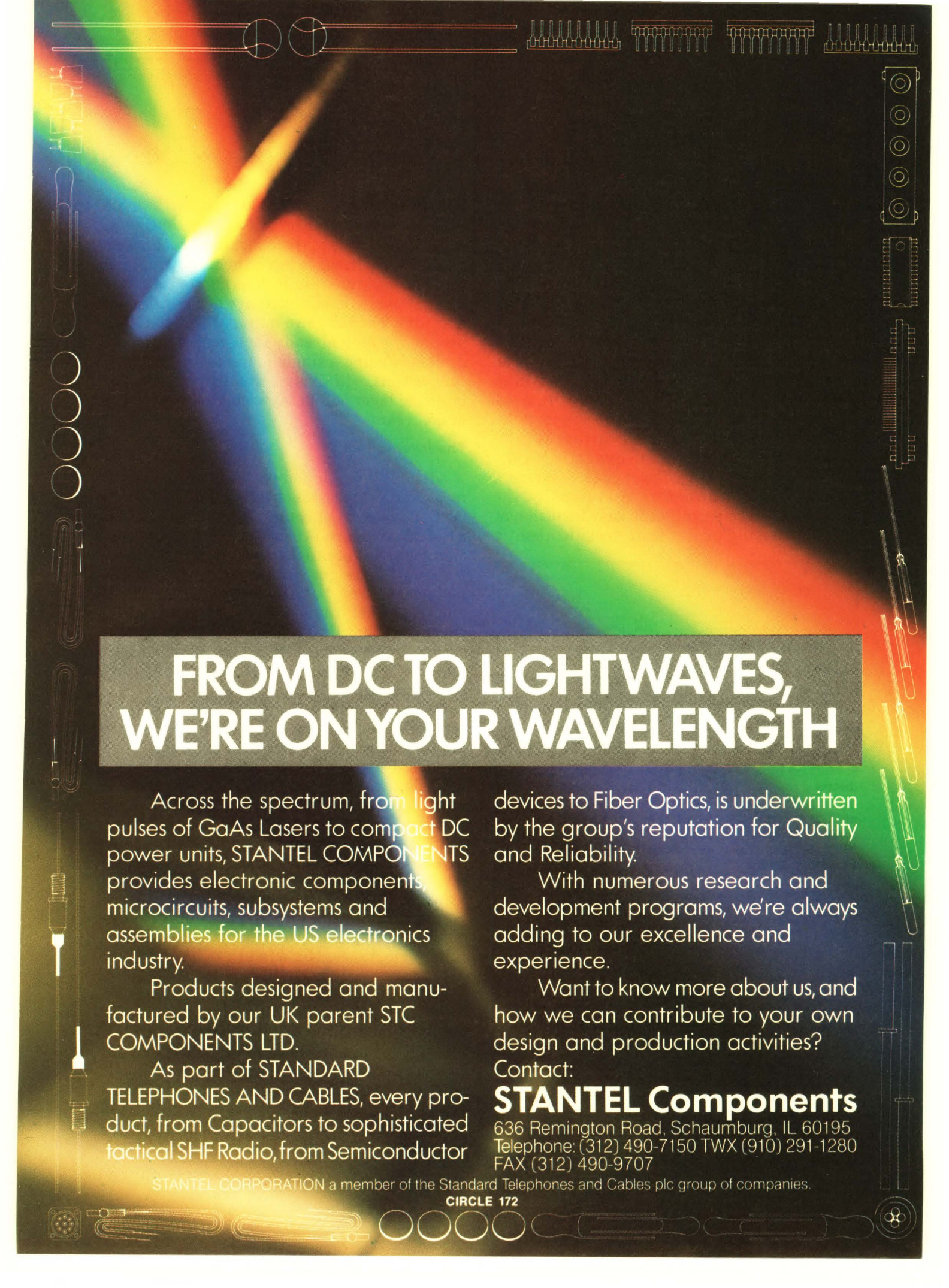
Yet a third bipolar-CMOS process, this one from Hitachi, aims at high-speed static memories, producing a low-power memory cell and a high-speed driver circuit (Fig. 9). The memory cell combines cross-coupled p- and n-channel FETs with emitter-follower npn transistors; it dissipates only 1 nW and accesses data in 50 ns. Read current flows only through the selected cell—that is, the one connected to both the selected word line and the selected digit line. In most standard CMOS RAMs, read current flows through all the cells connected to the selected word line. Thus the operating power of the bipolar-CMOS array is significantly lower than that of a CMOS array.

When maximum speed is the issue, however, the CMOS RAM to look at is a 1024-bit unit from Cypress Semiconductor Corp. (San Jose, Calif.). Built with an n-well process and 1.2-μm features, the RAM has an access time of 15 ns and a power consumption of 400 mW.

Valuable as it is for static memories, CMOS is ready to become the technology of choice for dy-



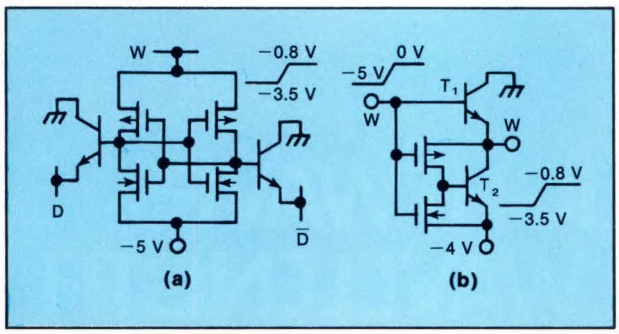
8. Internal loading of CMOS gates can slow down a circuit. A mixed bipolar CMOS process comes to the rescue. In Motorola's structure, bipolar transistors merge with gate logic to handle large internal fan-outs.


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CIRCLE 172

namic RAMs beyond 256 kbits. The reason is clear: As cell sizes shrink, they need greater protection from alpha particle strikes—protection afforded by twin-well CMOS technology.

This technology also permits building high-voltage structures, so that charge-boosting techniques can be used to boost the number of electrons stored in the capacitor—a critical problem as scaling reduces the capacitor size.

In its 64- and 256-kbit dynamic RAMs, Intel Corp., Memory Products Div. (Aloha, Ore.), put CMOS structures to work in the support circuits that surround the memory array. As compared with standard NMOS dynamic RAMs, the new devices use 65% fewer clock generators and 30% fewer transistors. Additionally, the CMOS structure permits the easy inclusion of new addressing modes that provide about a four-time improvement in the speed with which data can be read from or written to the memory.



9. With its bipolar CMOS process, Hitachi has produced a memory cell (a) and a word driver (b) for high-speed static RAMs. The memory cell has an area of about 450 μm^2 and consumes about 1 nW at 5 V and 20 MHz. The word driver occupies about 3000 μm^2 and consumes about 3 mW under the same conditions.

RAMs, becuase of their regular structure, do not pose a critical interconnection problem. Random-logic circuits such as microprocessors and gate arrays, however, are often interconnection-, rather than density-limited. The problem, which already faces semicustom IC designers using a single metal layer for interconnections, will likely become less critical as multiple layers of metal wiring move into the mainstream.

The layered look

Although n^+-doped polysilicon pervades most NMOS processes as a first-level interconnection material, it cannot be used throughout a CMOS structure, because it forms diode junctions when it contacts the p-doped regions. Mixed-MOS designs go with polysilicon for the n-channel array, but use metal between the p- and n-channel transistors in the surrounding circuitry. That limitation on the use of polysilicon is one reason CMOS circuits need a second metal layer as part of the strategy for achieving high density.

Despite that, polysilicon remains a viable interconnection material. One or two layers are found in various memory and logic products, and an 8-bit CMOS processor family, the NSC800, is fairly typical of how polysilicon and metal cooperate. The chips, developed by National Semiconductor Corp. (Santa Clara, Calif.), employ two polysilicon and one metal layer. The extra polysilicon layer is used to form high-resistance load elements, and the others serve as interconnections. National Semiconductor does not expect double polysilicon to be a panacea and has developed a two-layer metal process for a family of high-density gate arrays.

More recently, advanced CMOS processors have started to appear. The only commercially available one at the 32-bit level is Motorola's MC68020, which is not a fully CMOS design. Instead it uses a mixed-MOS approach: about 80% of the chip is made up of n-channel transistors, while the remaining 20% uses CMOS logic to do what it does best: keep power consumption down.□

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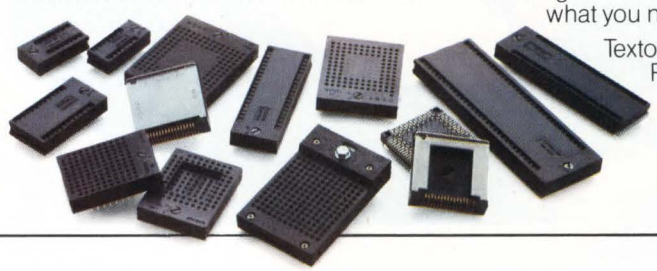
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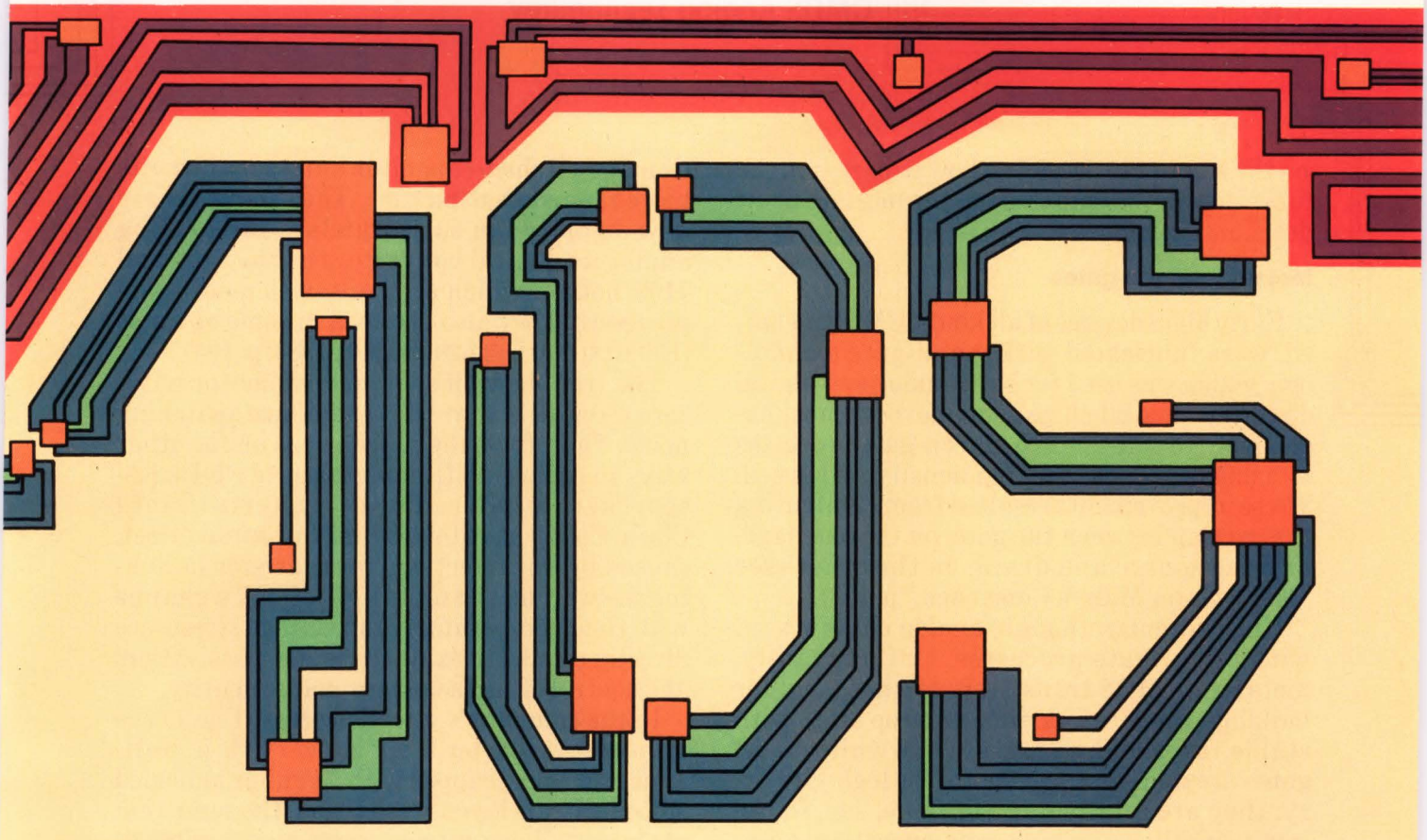


TECHNOLOGY REPORT

Analog CMOS marches on, but it steps to the beat of a different drummer

First because it makes excellent switches and input devices, then because it allows the easy addition of digital functions, but always because it dissipates little power, CMOS takes over the analog world as well.

Frank Goodenough



Like digital ICs, analog circuits have been moving from bipolar to CMOS construction at an ever-increasing pace in recent years. Until recently, the move was in response to forces completely independent of those driving the digital world. Lately, however, the need to mix analog and digital circuitry on the same chip has been a major motivating factor behind the move to analog CMOS.

At first, analog functions moved to CMOS for two major reasons: CMOS builds nearly perfect switches for handling analog signals without distortion and it creates pairs of transistors with very high input impedances. The switches made it possible to build precise converters, and the transistors allowed precise op amps to be fabricated.

Today, as manufacturers seek to increase the number of functions of their devices, it is often necessary to add significant amounts of analog circuitry to digital chips, and vice versa. Of course, the analog functions are expected to be of ever-increasing quality — high resolution, good linearity, and low noise — and both the digital and the analog circuitry is meant to be fast.

How do the designers of analog CMOS ICs meet these sometimes contradictory goals? The way they always have, by making trade-offs. Specifically they have to decide whether to use:

- Metal-gate or silicon-gate transistors
- P-well or n-well construction
- Double or single layers of polysilicon or metal
- Ion-implanted, diffused, or thin-film resistors
- Metal or polysilicon (or both) for capacitor electrodes

Of course, they are forced to make a major trade-off between speed and accuracy in determining the IC's minimum feature size. (The smaller the feature, the faster the circuit. At the same time, small features lower the voltage rating and therefore degrade the ability to accurately handle signals with wide dynamic ranges.)

Finally, in many cases designers find it necessary to combine CMOS and bipolar circuitry

on the same chip. Deciding how to partition the functions on the chip is often the most difficult decision of all.

Metal vs silicon gates

Early MOS devices of all kinds, CMOS included, were fabricated with metal-gate technology, which was used for both analog and digital circuitry. Digital chips soon moved almost exclusively to self-aligned silicon-gate processes to achieve greater packing density and speed. These improvements resulted from eliminating the overlap between the gate, on the one hand, and the source and drain, on the other (see "Metal Gates Make a Comeback," p. 108).

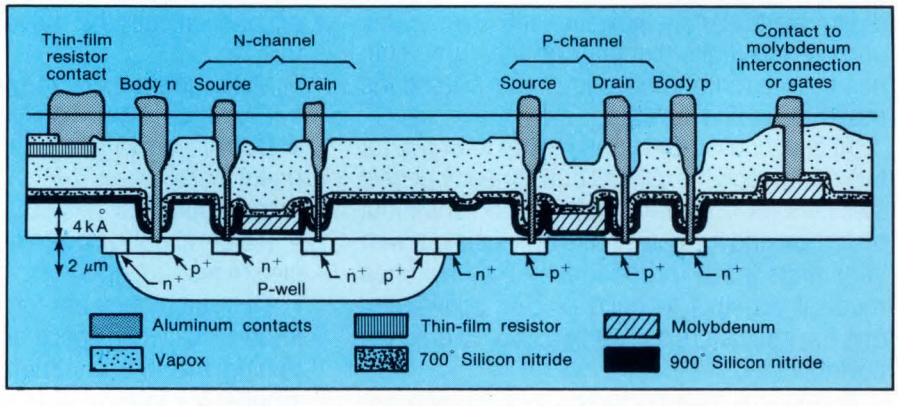
Until recently, though, analog chips stayed with metal-gate processes. Unfortunately, metal-gate MOS transistors are not ideal for building comparators, timers, or op amps with stable threshold voltages. Thus while metal gates are more than adequate for logic circuitry, they are totally unacceptable, say, in the input circuitry of a high-gain operational amplifier.

Analog designers have dealt with this problem by ensuring that they create almost all of their threshold-sensitive circuitry with bipolar technology. Recently, however, the introduction of switched-capacitor auto-zero circuits has changed that picture. These circuits are now employed in such standard integrating analog-to-digital converters as the 7106 and 7109, both of which are built with metal-gate processes. They also are used in some op amps (ELECTRONIC DESIGN, Sept. 6, 1984, p. 104).

The trouble with switched-capacitor auto-zero circuits is that they introduce switching noise. Therefore, the search goes on for other ways to reduce drift in metal-gate FETs. Researchers at Micro Power Systems (Santa Clara, Calif.) have found that the initial offset, caused by imperfections in transistor matching, as well as the metal-gate FET's change with time, temperature, and voltage stress, are directly related to oxide thickness, passivation, and control of surface-state charge density.

In the company's p-well process (Fig. 1) the transistors are built with a very thin, well-annealed oxide, capped with a similar annealed silicon-nitride layer. In addition, the same thin oxide and silicon-nitride sealer also minimizes the typical metal-gate noise problem caused by surface trapping sites and high charge density in the gate dielectric. The resulting transistors are said to be almost as quiet as JFETs.

Of course, the most popular way of dealing



1. A metal-gate, CMOS p-well process from Micro Power Systems can achieve the threshold voltage stability and density of silicon gate processes because molybdenum is used for the gate material.

with the shortcomings of metal-gate devices has been to substitute silicon for the metal. The big problem with standard silicon-gate MOS, however, is that silicon has higher resistivity than metal. The main remedy, for analog CMOS as for digital, has been to add a layer of refractory-metal silicide to the silicon gate to lower its resistivity.

Disagreement over wells

As for the question of wells, there appears to be little agreement as to which is best—p or n.

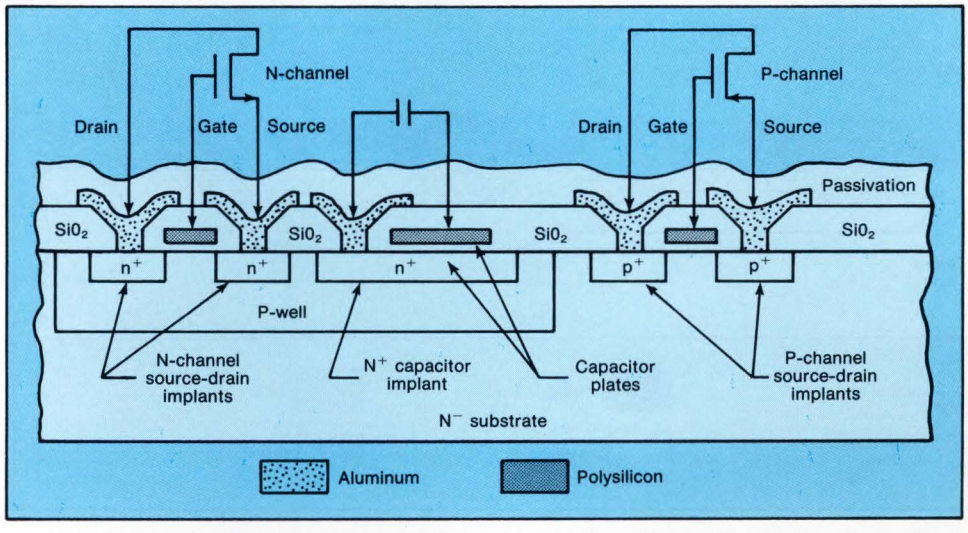
At present, p-well predominates for analog CMOS processes, perhaps because it has been around longer. Moreover, several new p-well processes have recently become available for analog circuits.

One major advantage of p-well technology is that the p- and n-channel transistors made with it will, if the transistors are of the same size, have similar speed and transconductance. Threshold voltages of transistor pairs therefore can be closely matched to minimize the offset voltage of op amps and comparators. For this reason, Linear Technology Corp. (Milpitas, Calif.) chose p-well for its analog CMOS process (Fig. 2). Its analog switch with low offset voltage (see the Design Entry, p. 195) is built with it. Like most analog p-well processes, it also makes use of the substrate npn transistor in op amps and band-gap references.

The manufacturers of a second new analog CMOS structure (Fig. 3) have also chosen p-well construction for superior transistor matching. The chip, from precision Monolithics Inc. (Santa Clara, Calif.), uses oxide isolation to reduce parasitic capacitance. It was first used to build a 6-μs, 10-bit a-to-d-converter (ELECTRONIC DESIGN, Sept. 6, 1984, p. 191).

A second advantage of p-well, according to American Microsystems Inc., (Santa Clara, Calif.), is lower susceptibility to power supply noise in the substrate. For example, in most high-gain amplifiers, the n-channel device in the p-well is used for the input gain stage. It is shielded from the substrate noise by the p material in the well.

On the other hand, Texas Instruments Inc. (Dallas) believes n-well is better for analog circuits. TI has developed a family of analog CMOS processes and has used them to build op amps, comparators, a-to-d converters and a variety of telecommunications chips. It chose n-well primarily because of the superior mobility of n-type silicon devices. (ELECTRONIC DESIGN, Sept. 1, 1983, p. 134). However, it used this mo-



2. A p-well silicon gate process from Linear Technology puts its voltage-insensitive capacitors between a layer of polysilicon and a p^+ diffusion in the well. P-well is used to permit well-matched n and p channel transistors.

bility to build very small n-channel transistors in the p substrate.

For example, an n-channel device of a given size will have three to four times the gain of a p-channel transistor the same size. With maximum use of these tiny NMOS transistors, very small, high-gain op amps are built. The mobility of n-type devices can also be used to build faster circuits. In fact, an upcoming comparator from TI is both fast and precise. Its response time for a 100-mV step with 5-mV overdrive is just 0.65 μs. The offset drift is less than 1 μV/°C. These are better than bipolar specifications, and the bias current is 1000 times lower.

A second reason for using n-well is its similarity to digital NMOS processes. As a result, the logic designs in converter, telecom, and other mixed-function chips can be easily transferred from NMOS to CMOS. TI, for example, has chosen p-well for its digital chips to obtain well matched transistors. Most other manufacturers use p-well for logic to get the optimized, mobile n-type devices.

Twins that get along

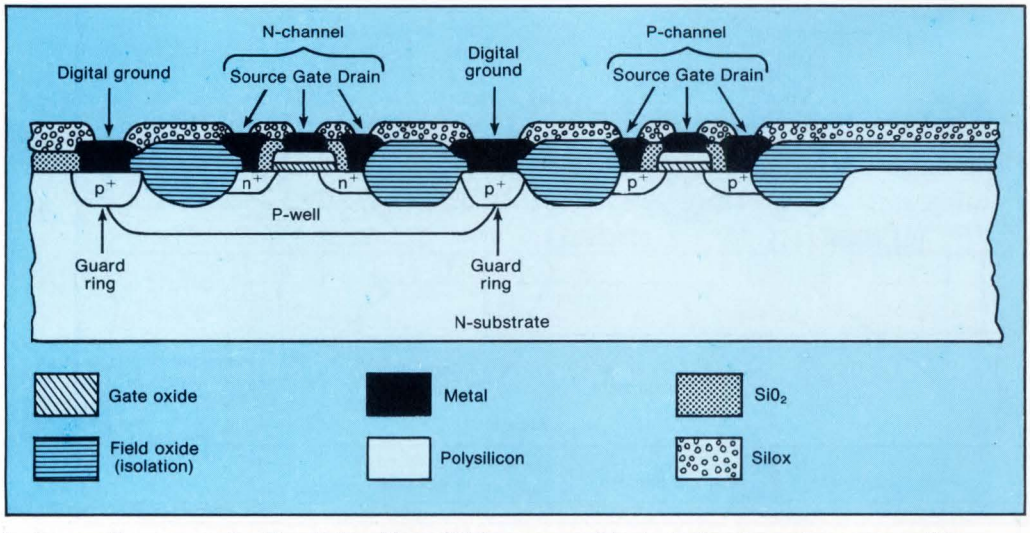
In adjacent wells on the same chip, p- and n-channel devices work well together. At present this twin-well process under development by NCR (Fort Collins, Colo.) is little used for analog functions, except by AT&T Bell Laboratories (ELECTRONIC DESIGN, June 14, 1984, p. 158). However, this trend may change; many semiconductor makers are studying the process.

In a twin-well process under development by NCR (Fort Collins, Colo.) (Fig. 4), a p-substrate, with or without a p-epitaxial layer, contains pairs of ion-implanted wells, one p and one n. Each well contains its respective n- or p-channel MOSFET. This structure permits precise control of individual transistor characteristics. Both wells can be optimized for resistivity and their transistors for threshold voltage, matching, gain and minimum parasitic capacitance.

There is virtual unanimity in the semiconductor industry that twin-well structures are mandatory when feature sizes get much below 2 μm.

A vicious circle

The designer striving for process improvements to increase the speed or bandwidth of analog chips—particularly in CMOS—finds himself in the same predicament as a dog chasing its tail. To increase speed, feature size must be reduced. If feature size is reduced, the supply voltage must be lowered to prevent both break-



3. A p-well process by Precision Monolithic uses oxide isolation to reduce parasitic capacitance and thus increase speed. It has been used to build a 10-bit, 6-μs a-d converter.

down and latch-up from parasitic bipolar devices. If supply voltage is lowered, maximum signal voltage must be reduced, even though CMOS handles signals almost to the rails. However, input signals do not decrease and if anything, the smaller transistors are noisier. To top it off, unlike transistors for digital circuits, MOS transistors for analog circuits do not scale. As a result, accuracy and dynamic range drop.

For example, as the feature size shrinks below 2 μm, the usual sharp breakdown of MOS transistors becomes soft and leakage current rises. Likewise, the transistors no longer turn on and off sharply. While both of these problems can be handled in logic circuits by careful design (although noise immunity may drop), linear performance is degraded significantly. In addition, because drain and source are closer together, punch-through can occur and parasitic capacitance is greater. Moreover, these smaller transistors make poor current sources, and threshold voltages and capacitors are hard to match. Finally, because of channel-length modulation, the gain drops.

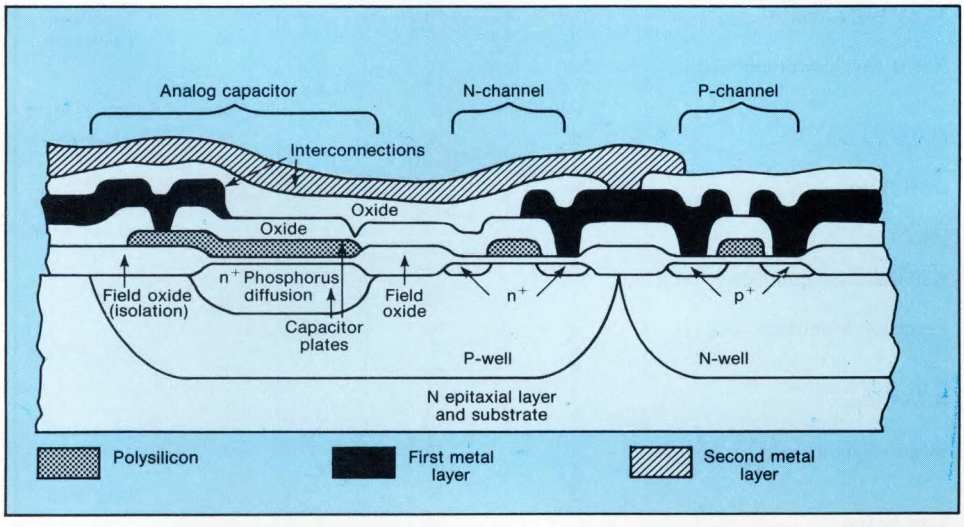
Process engineers and chip designers are hard at work on a bag of tricks to overcome these problems (see the table, p. 126). In particular, major efforts are aimed at averting latch-up. They include the placing of an epitaxial layer between the substrate and wells, new design rules, and the use of twin wells.

One circuit trick for solving the problem of reduced dynamic range is the use of switched-capacitor techniques to convert input signals to differential form, thereby essentially doubling the dynamic range. This approach with a 2-μm, p-well process has been used to build a switched-capacitor filter operating on NTSC and PAL video signals. This first-order filter, from Hitachi Ltd. (Tokyo), operates at a clock rate of over 14 MHz. The signal-to-noise ratio for a dc-to-5-MHz bandwidth is 70 dB, and the differential output signal is 6 V pk-pk. (Fig. 5).

Supply voltages to climb, too

But analog CMOS cannot count on a future of ever higher speed, lower voltages, and potentially limited accuracy. Researchers are obtaining higher voltages by trading off some of the speed. If the high speed is not needed, a 40-V process cannot be beat for accuracy. As a result, at least four companies have such processes under development, and several others are considering it.

One objective will be to replace bipolar de-



4. Twin-well processes such as this 2-μm design from NCR optimize the characteristics of both n- and p-channel transistors. The capacitor is built with the oxide dielectric between polysilicon and an n^+ diffusion in the p-well.

vices across the board. Such a process could build an op amp that would be priced like a 741 and have the input impedance, low bias current and speed of a biFET.

The choice of n- or p-well will probably be along the lines already established, so both will probably be used. The new chips will have feature sizes in the 3-to-4-μm range, some will use epitaxy, all will provide switched-capacitor capability, and some will have thin-film resistors. One contender, Telmos Inc. (Sunnyvale, Calif.), may scale down its 200-V linear DMOS-CMOS process to handle the breakdown problems and incidentally provide high output current.

Learn your R's and C's

The interface between the real and the digital world requires a d-to-a and a-to-d converters. To build these, not only are op amps, comparators and switches needed, but also precise, stable resistors and capacitors. Thus, a good analog CMOS process must build one or both of these latter components. Diffused and ion-implanted resistors are easily capable of 6-bit accuracy and, with care, 8 or 10. However, for real precision, thin-film nichrome or sichrome resistors must be used, and many of the present processes have them. They are usually fabricated just prior to passivation.

Switched-capacitor circuits, of course, require precise, stable, voltage-insensitive capacitors. And it might well be said that if silicon dioxide did not make a good capacitor dielectric, there would be no switched-capacitor circuits—on-chip or off. Moreover, even bipolar ICs would not be as advanced, because these oxide capacitors stabilize them.

Although only one dielectric material is available, the choice of what kind of electrodes it is sandwiched between varies widely from

Analog CMOS processes feature size vs voltage rating

Company	Feature size (μm)	Voltage rating (V)	Status		Comments
			Now	Future	
American Microsystems Inc.	3	10	X		
	1 1/4	5		X	Epitaxial layer
Analog Devices Inc.	4-5	30	X		Merged
	6	10	X		
AT&T Bell Laboratories	3 1/2	10	X		Twin well
	2	5		X	Twin well
Harris Semiconductor Group	5-7	30	X		
	3-4	10	X		
	2-2 1/2	5		X	Epitaxial layer
Motorola Inc.	2	5		X	Merged
	3	30-40		X	
NCR Corp.	10	4	X		
	2	5-10		X	Twin well and epitaxial layer
National Semiconductor Corp.	4-5	5	X		
	4	40		X	
Precision Monolithic Inc.	9	15	X		
	5	5	X		
	3	5		X	
RCA Corp.	7	20	X		
	3	10	X		
Silicon Systems Inc.	4	12		X	
	3	5	X		
	2	5		X	Twin well
Telmos Inc.	4-6	30	X		
	3	10	X		
	N.a.	40		X	
Texas Instruments Inc.	6-9	20	X		
	3-5	10	X		
	2-3	5	X		
	N.a.	40		X	



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process to process. If NCR puts a layer of thin oxide below a layer of polysilicon and above a heavily doped n^+ ion-implanted phosphorous diffusion in the p-well (ELECTRONIC DESIGN, Dec. 8, 1983, p. 108). This same type of capacitor is used by Linear Technology in its p-well process made with a single polysilicon layer. A process with two layers of polysilicon, one for gates and one for interconnections, can place the oxide between the two, eliminating the need for the n^+ diffusion.Other approaches place the oxide between polysilicon and a metal layer or between two layers of metal.

Nitride won't do

Precision Monolithics discovered almost by accident just how good a capacitor made of silicon dioxide is. Unlike most makers of monolithic op amps, it uses silicon-nitride capacitors rather than oxide to stabilize its op amps. Its dielectric constant, k, is three times larger than that of oxide, so it needs only one-third as much silicon. However, when the silicon-nitride was tried in switched capacitor circuits, it suffered from dielectric adsorption, or memory, just as paper and Mylar capacitors do. (This effect may be caused by charge trapping rather than dielectric adsorption—a polarizing phenomenon.) This problem does not occur with oxide. Thus the company's CMOS process, like all others, must use oxide for its precise, voltage-insensitive capacitors.

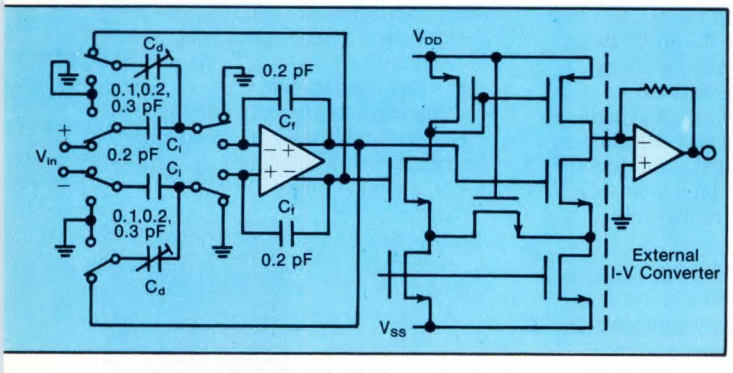
If CMOS is so great for analog and digital circuits, why the move to merged bipolar/CMOS processes? Because for a number of circuit jobs, while CMOS transistors are adequate, bipolar devices are better. For example, a simple operation like getting a fast digital signal off a chip and down a line requires 10 to 30 times more silicon with CMOS transistors than with bipolar devices to obtain similar low output impedances from a line-driving stage. As a result, even most high-speed digital CMOS chips use the parasitic, or substrate, transistor as an emitter follower for line driving and similar functions.

However, the real weakness of CMOS for analog functions is the large amount of silicon needed to build matched input transistor pairs with low noise for op amps. Probably the best to be expected in the near future is 741-type performance, not CMOS OP-27. On the other hand, some designers predict that by taking advantage of the switched-capacitor auto-zero circuits, manufacturers will build CMOS op amps that have noise and offset voltage characteristics as good as those in bipolar units—and that are more stable. That would be a race to watch. Other designers believe that process refinements alone will lead to CMOS op amps that are as good as bipolars.

An additional problem with basic CMOS processes is that they do not lend themselves easily to building references. Without a buried layer, making buried zeners is difficult (although Telmos has put them in the p-wells of its silicon gate process). Band-gap references can be built, but for best performance, even they should use the substrate transistor. The best band-gap references in CMOS have been built with switched-capacitor techniques.

The ultimate advantage of merged processes is access to highly mobile, high-transconductance, isolated npn transistors. When maximum speed and gain are needed, a good npn transistor beats an n-channel transistor hands down. Other devices available from various merged processes include JFETs, lateral pnp transistors, and even fast, high-gain vertical pnp devices.

The first and most successful merged process is RCA's metal-gate, p-well BiMOS technique introduced over 10 years ago. Since then it has



5. This video-bandwidth, switched-capacitor filter operates on both NTSC and PAL video signals. It is built with a 2 μm, p-well process. By using a differential signal, dynamic range is doubled, permitting a 6-V p^k-p^k output signal.

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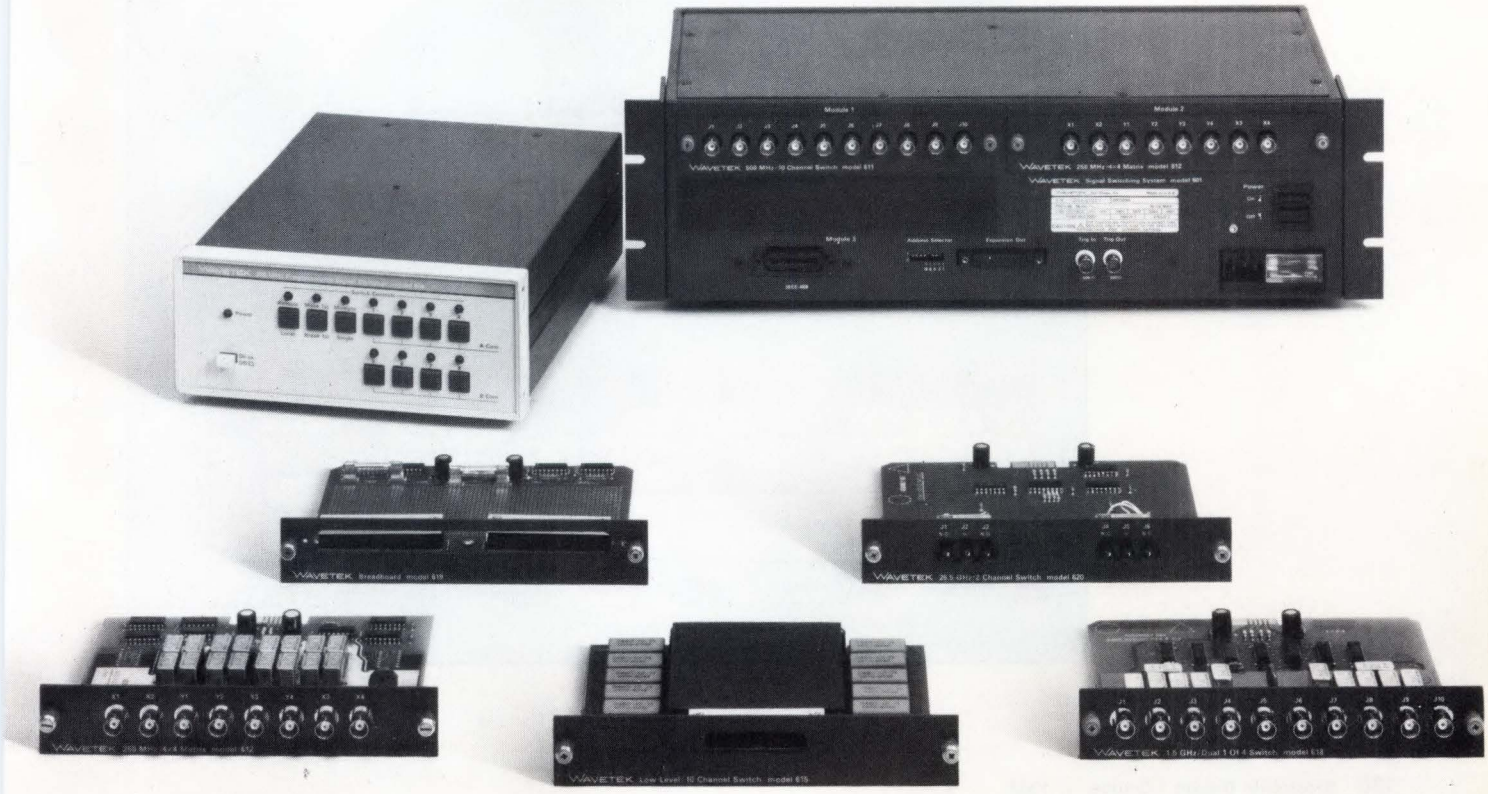
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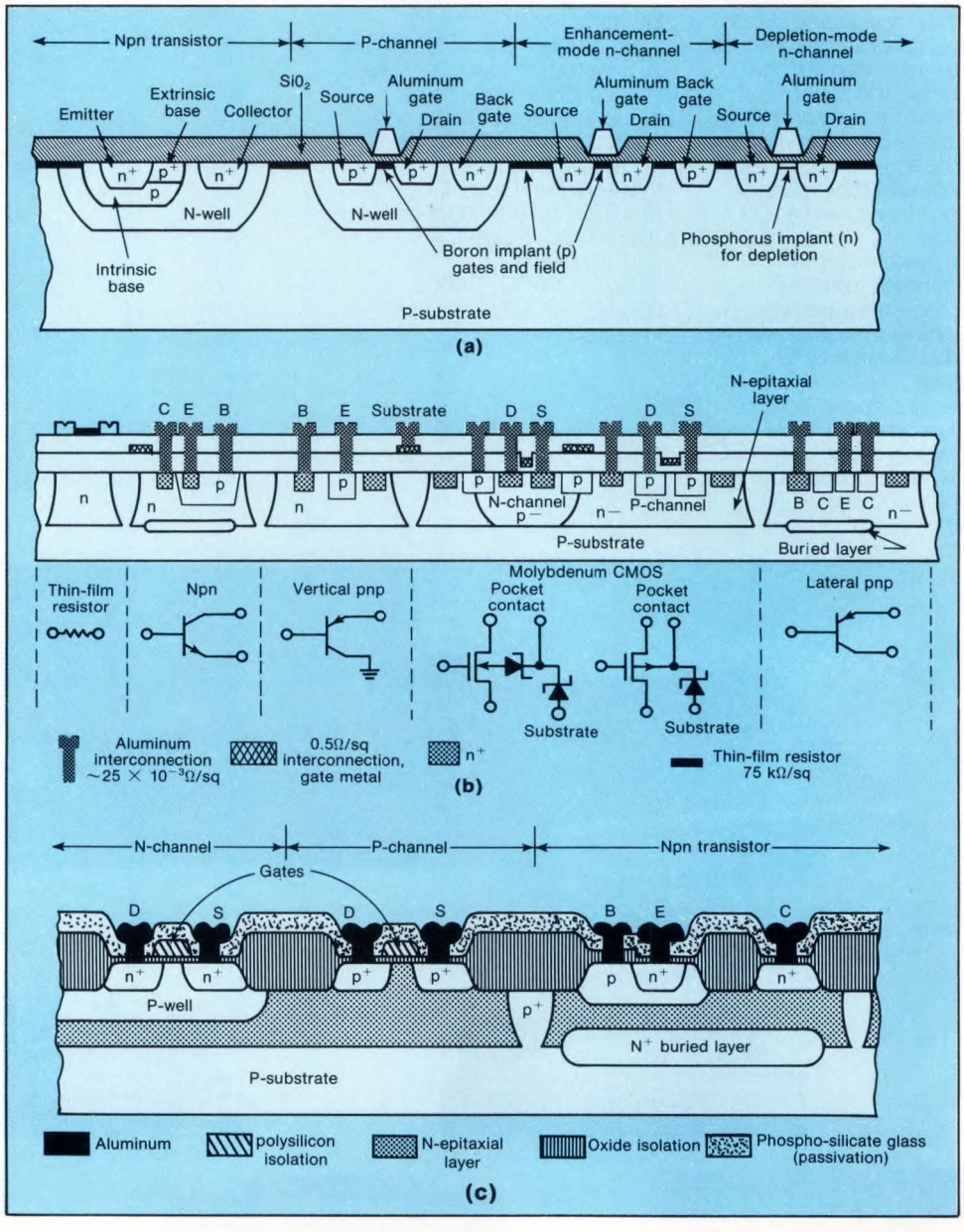


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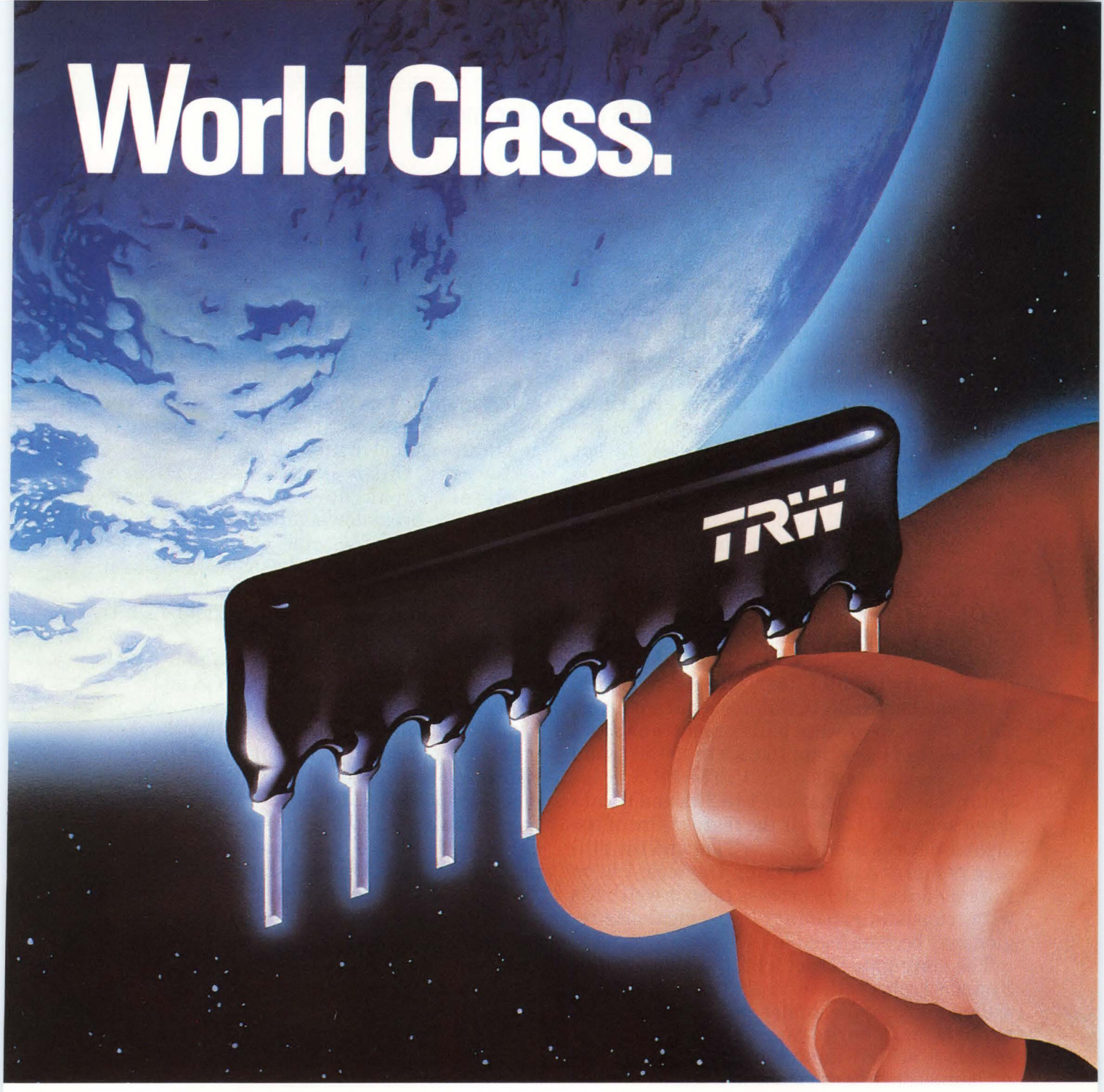
been used in a broad line of popular op amps. The MOS transistors have provided high input impedance, as well as low bias current in all stages, for current sources and loads, and they have been used in output stages that can swing to the rails. In each op amp design, MOS transistors are mixed with bipolar, with each doing what it does best. For example, for lowest offset voltage and noise, bipolar transistors are used in the input stage.

But if the tradeoffs needed to develop a high-performance analog CMOS process are great, they are virtually infinite for a merged process. Here the wide selection of bipolar processes must be multiplied by the processes used for CMOS. An indication of this structural diversity is shown in four recently developed bipolar/CMOS processes. Two use metal gates (Fig. 6a, b) and two silicon gates (Fig. 6c, Fig. 7). The first process is n-well, the second and third



6. Merged bipolar/CMOS processes such as these three make possible fast or precision devices. Analog Devices uses n-well in order to build the best possible npn transistors (a). Micro Power Systems uses a p-well and get good npns by building them in pockets of an n-type epitaxial layer (b). That process also makes good vertical pnp transistors and precision thin-film resistors. Hitachi's fast p-well process (c) has been used to build FM audio filters for VCRs.

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CIRCLE 51

p-well, and the fourth n-well.

Although the first process was only recently incorporated in a product, a 16-bit one-chip d-to-a converter (ELECTRONIC DESIGN, June 14, 1984, p. 173), the developer, Analog Devices (Norwood, Mass.), is already converting the process from metal-to silicon-gate.

The second process is not a plain metal gate either, but rather a merged version of Micro Power System's moly-gate process. While not yet used to build any standard products, it has turned up in a number of custom chips, particularly in the medical field. Pacemakers, for example, are taking advantage of the minimum power needs of CMOS.

Analog Devices chose n-well to gain access to a high-gain, fast, isolated npn transistor. The basic bipolar process is triple-diffused and similar to a process used by TRW (La Jolla, Calif.) for years to build flash a-to-d converters. With neither an epitaxial nor a buried layer, this 4-to-5-μm process builds npn transistors with betas of more than 100, f_t's to 400 MHz and breakdown voltages of 20 V. The MOS transistors have gate delays of 1 to 2 ns and breakdown voltages of 30 V. If the feature size of the bipolar devices is dropped to 2 μm and the process is merged with Analog Devices' 1.5- to 2.5-μm digital CMOS process (also n-well), ICs with transistor capability in the gigahertz region may become feasible.

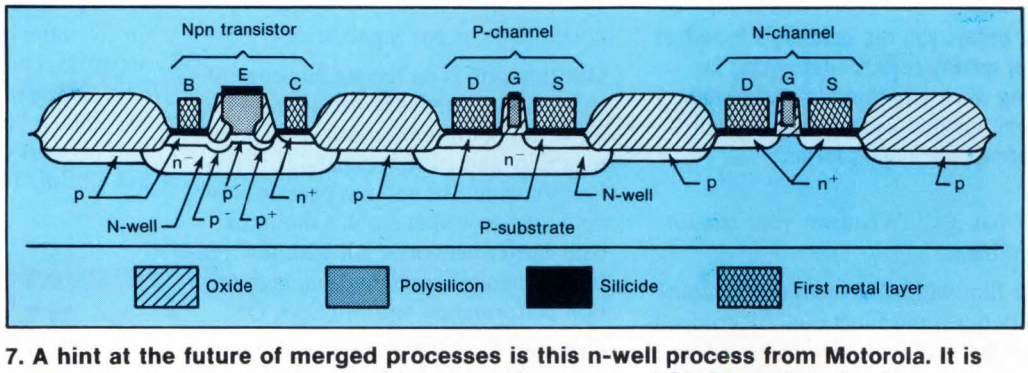
The moly-gate structure from Micro Power Systems builds both vertical npn and pnp transistors and also p-channel devices in an n^- epitaxial layer. A buried layer is added to the npn section to achieve minimum on-resistance. The n-channel devices are made in diffused p-wells, and similar material is used for isolation. This process, like the previous one, also builds precision thin-film resistors.

The third structure is a silicon-gate circuit, but its npn transistors are fabricated somewhat the same way as in the second process: The transistors are made in an n-type epitaxial layer, and they have a buried n^+ layer. The p-channel transistors are in the epitaxial layer and the n-channel in a p-well.

However, this 5-μm process by Hitachi (Takasaki, Japan) does not make pnp transistors. The breakdown voltage of the bipolar transistor is 21 V, the beta 100, and the f_t is 400 MHz. The transistor has been used in ICs for video cassette recorders (including an FM audio filter), a switching power supply, and a white balancer.

The fourth merged structure under development is for high-speed CMOS logic, and it is a true glimpse of the future. Up to now, the designers of high-speed CMOS have for the most part been content to use the substrate npn transistors solely for output drivers. But the process being developed by Motorola (Phoenix, Ariz.) is used to build isolated npn transistors for on-chip circuits. The circuits are at the output of gates or inverters to provide large fan-outs. The 2-μm process can be used just as well to build analog circuits, and the npn transistors have an f_t of 2 GHz.

An n-well process, it uses all the latest high-speed process techniques, such as metal silicide contacts, oxide isolation, and polysilicon walled emitters. The next generation of the process will have an epitaxial layer to reduce latch-up, Motorola says.□



7. A hint at the future of merged processes is this n-well process from Motorola. It is now under development for on-chip use as the output of CMOS digital circuits.

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A DOZEN EXPERTS SEE CMOS IN YOUR FUTURE

Semiconductor industry executives are unanimous in the opinion that the penetration of CMOS—which began more than a decade ago in hand-held calculators and digital timepieces—is on the roll. It is rapidly becoming the favored process from discrete logic, microprocessors, and memories to data converters and dedicated telecommunications ICs. If the predictions made by a dozen industry experts come true, the well-established NMOS and bipolar technologies will be forced to take a back seat virtually across the board.

R. GARY DANIELS
Motorola Inc.

SUNLIN CHOU
Intel Corp.

DARRELL MAYEUX
TRW Inc.

MIKE EVANS
National Semiconductor Corp.

PETER PERRY
Mitel Corp.

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RCA Corp.

JAMES TOWNSEND
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WILLIAM WAGNER
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RICHARD BLANCHARD
Siliconix Inc.

DOUG GRANT
Analog Devices Inc.

TOM SPRUNGER
Texas Instruments Inc.

EDWARD ROSS
Signetics Corp.

At the core of this optimism is the belief that only CMOS will make it possible to move up to the next generation of crucial circuits. The power barriers now facing alternative semiconductor processes indicate that only CMOS will allow chip makers to capitalize on the density that can be achieved with gate arrays and standard cells. The same holds true for digital signal processors and microprocessors in general.

Nevertheless, many technical hurdles still must be cleared. In data converters, for instance, CMOS by itself has neither the speed nor the resolution demanded by 16-bit analog-to-digital circuits. CMOS is thus being married to bipolar linear processes, offering a blend of digital and analog circuitry on the same chip—an essential feature for the coming telecommunications ICs.

Additionally, a CMOS design cannot yet match the execution time of some specialized bipolar chips, say, a 45-ns multiplier. In fact, a 16-by-16-bit CMOS multiplier built with 2-μm design rules works roughly half as fast as similarly designed bipolar chips.

In terms of speed, CMOS discrete logic is not nearly as fast as the advanced forms of bipolar logic. That gap will be closing over the next two years, as line widths continue to shrink from 3 to 2 μm.

Once, maybe twice a decade the electronics industry encounters a force that affects not only the way circuits are physically designed but also the way the industry thinks. CMOS is just such a force. It has opened doors to new processes, but more importantly, it has opened the mind to new possibilities.

R. GARY DANIELS

Vice President, Technical Staff
Motorola Inc., Microprocessor Products Division

One of the most interesting aspects of CMOS is that it answers different needs in various applications. Every device, be it a microprocessor, memory, or dedicated telecommunications chip, is affected differently by the use of the process, and enhancements will likewise influence specific areas differently. The technology's background illustrates that fact.

The pioneers in CMOS—working in 1969—concentrated on applications such as timepieces, where tiny batteries made low power consumption an obvious requirement. I felt then that CMOS had much greater potential for the future, and my feelings proved right during the 1970s, when a lot of refinements in geometries and processing equipment opened the frontier for CMOS.

NMOS was still necessary largely because of the density and cost advantages it held. Even so, CMOS was likely to come into its own sooner or later because of its lower power dissipation and its speed.

Through the years, CMOS came into use more and more, reaching out to battery-backed microcomputers and certain telecommunications devices. I wondered when microprocessors would have to take that step.

My concern was unfounded, because as it turned out, the decision was made for me. CMOS happened to microprocessors because there was no other choice. It wasn't a matter of cost or performance tradeoff. If we had not implemented present-generation microprocessors in CMOS, we couldn't have gotten the power out of the chips with reasonable packaging techniques.

> "CMOS happened because there was no choice; it was not a matter of cost or performance."

Within the microprocessor area, there are two separate classes that require CMOS. One is characterized by great chip complexity and high performance. Dissipating 5 to 6 W in NMOS and only 1 W in CMOS, these chips must be built in the second to operate at all. On the other side are the single-chip microcomputers, often used as controllers. Running in the milliwatt range in CMOS, they are ideal for battery applications.

Of those two classes, one has to be built with CMOS or heat dissipation will burn up its circuitry. The simpler, battery-powered chip needs CMOS for its low power. The whole range of processors benefit, and in fact depend on the process.

Memories, though, need CMOS for com-

R. Gary Daniels joined Motorola in 1965, working for five years in the Central Research Laboratory and for another five at the Timepiece Electronics Division. The rest of his career at Motorola has been spent working in the Microprocessor Division.



pletely different reasons. Heat is not a problem here. We never run our memories up to the 1-W range, because clocks are internally generated upon an address transition. Also, a lot of dynamic circuitry prevents the entire device from being on at once, so it runs cooler.

The best argument for CMOS memories is the process's lower power dissipation, crucial for system reliability. At static RAM densities, HMOS memories pull 120 mA active current; the same chip in CMOS draws 50 mA. The system implications for memories are phenomenal when you realize that there may be thousands of memory ICs in a system.

The rapidly moving telecommunications area has another clear and continuing need for CMOS. The standard phone of the future will be digital, and its power source comes from a twisted-pair loop. Power considerations are paramount here, since the entire system must run at under 1 W. As they continue to offer more and more features, the complex chips that perform those operations will continue to be built with CMOS.

Analog devices pose another challenge—altogether greater and greater voltage swings. Bipolar still wins on that, but for applications that depend on CMOS, this specification must still be met. Even though there have been great strides made in CMOS to supply analog functions, the best solution here may be combining of technologies on one chip.

The structure of CMOS itself will see some changes over the next few years; the most obvious will of course be device size. We are presently at 2 μm. The step to 1.5 μm will be made easily in the next few years.

As device geometries shrink, however, voltage breakdown becomes a concern. So power supply requirements will probably drift away from the present 5-V to 3-V supplies.

At the transistor level, we're now at the 200,000-plus mark. We expect half a million transistors on silicon by 1987.

CMOS must also become more rugged. All CMOS devices have an inherent SCR built in to them—in other words, a pnpn junction. If the voltage on one of the output pins gets too high, the pin latches up. This problem is continually being worked on.

One possible cure may be to coat the bare wafer with an epitaxial layer of a lower-resistivity silicon. In that way, rather than trying to grow low resistivity, we add a coat of it. But this method could catch on in the future. We presently don't use it on all products because it adds about a dollar per square inch to the cost of the wafer.

I would add, though, that CMOS will not replace other processes overnight. For very cost-sensitive applications, the job—at least over the next five years—can still be done quite effectively with NMOS. NMOS suffices wonderfully today for moderately complex microprocessors. I definitely believe, however, that in the next fifteen to twenty years, everything will be in CMOS.

SUNLIN CHOU

Director, Portland Memory
Technology Group Intel Corp.

Designers building dynamic RAMs with CMOS technology are now discovering that this approach—rather than NMOS—will enable them to store more data, access that information in much less time, and protect it from soft errors.

Two reasons to turn to CMOS is to solve the problem of punch through and to eliminate the hot-electron effect. Both result directly from reducing the device geometries of the transistors used in dynamic RAMs. As these transistors are made smaller—with the hope of achieving greater densities—their source-to-drain spacings shrink as well. In turn, the materials separating each will not be able to withstand the electric field that can lead to a short from the source to the drain—a difficulty which is known as punch through.

Even if that does not occur, there is still the possibility of the strong electric field generating spurious electrons, dubbed the hot-electron effect, that can cause a shift in the threshold voltage and may ultimately lead to the circuit malfunctioning.

The pair of difficulties, though, are much less severe at lower supply voltages. In fact, lowering the voltage down to 3.3 V will sufficiently reduce the electric field so that geometries can be shrunk for another decade before these problems arise again. CMOS can easily operate at such low voltages, but the complexity of the design needed to make NMOS work at these levels might prove prohibitive.

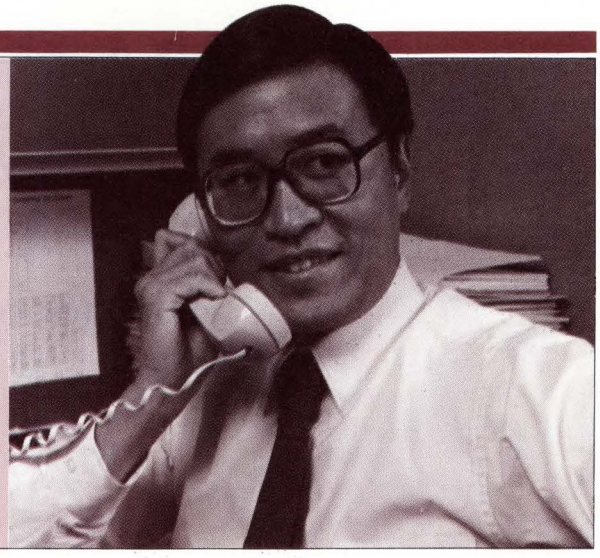
In addition to being the technology of choice for increasing the density of dynamic RAMs, CMOS will also improve the access time of such memories. Today, the access times for both NMOS and CMOS devices come in around 100 ns.

> "At 1Mbit and beyond, CMOS may be the only way to design chips with tolerable alpha-particle failure rates."

CMOS does offer a way to cut that time by employing static-column decoding. Typically, data in a dynamic RAM is stored in a two-dimensional array. An individual bit is accessed by selecting a particular column and row, and access delay is a function of the time it takes to do so.

Static-column decoding, on the other hand, can shorten the time involved in this process by allowing one column to remain selected as each bit located in it is randomly accessed by applying the appropriate row address.

This technique, however, demands static random logic, and implementing such a structure in NMOS would yield a circuit that would draw an enormous amount of power. CMOS is perfect for static columns, since it lends itself



Sunlin Chou is responsible for dynamic RAM process and product development at Intel in Portland, Ore. He has been with the company since 1971. Earlier, he carried out research in device physics at Fairchild. He holds a BS and MS from MIT and a PhD in Electrical Engineering from Stanford.

readily to static random logic.

Dynamic RAMs built with CMOS static columns have access times in the neighborhood of 55 ns, which translates into a data rate of about 20 MHz. Further, the shrinking geometries expected over the next three years will drop access times to 30 ns. Static-column decoding will considerably enhance the performance of, say, graphics systems, which will require higher data rates in order to write screens more rapidly.

The lower refresh rate of CMOS—compared with that of NMOS—may prove to be critical to building dynamic RAMs with densities greater than 8 Mbits—a development that may be seen in the next five years. At such levels, data that was formerly stored on several chips will be contained on one, in turn meaning more accesses to that particular IC. The chance of one of those accesses colliding with a refresh access would be very high with an NMOS device, slowing down the effective read and write access times. A CMOS design, with its lower refresh rate, would yield fewer collisions and thus speed up the access.

As designers miniaturize dynamic memories, alpha particle strikes will interfere to a greater degree with a circuit's operation. Indeed, soft errors cause 64-kbit NMOS dynamic memories to lose a single bit every million hours. CMOS circuits, on the other hand, are 10 to 100 times more resistant than their NMOS counterparts, since their capacitors are sunk into n wells and are thus protected from alpha particle bombardment.

Soft errors become even more severe as density increases: any 256-kbit dynamic RAMs that are designed using NMOS will require expensive die coatings or larger capacitors, in turn making for a larger die. At 1 Mbit and beyond, CMOS may be the only way to design chips with tolerable alpha-particle failure rates.

Until now, there have been two major problems that have blocked the widespread acceptance of CMOS, but they are both being solved. The first, latch-up, is being done away with through carefully selected substrate resistances and adherence to design rules.

The second difficulty with CMOS was that its complexity demanded up to 14 masking steps. NMOS designs, however, have grown more complicated over the years and now require up to 12 masking steps. Thus the difference in cost between CMOS and NMOS is much smaller.

The advantages of CMOS far outweigh any of its problems, though. Consequently, many of the 256-kbit dynamic RAMs just being introduced are built with it. Indeed, some manufacturers have elected to build all their future dynamic memories using CMOS. Others will find CMOS the easiest way to create the 1-Mbit dynamic RAMs that are expected in 1986. Further, 90% of the 4-Mbit dynamic RAMs that should be introduced by 1990 will probably be fabricated with CMOS.

DARRELL MAYEUX

Director of Marketing
TRW Inc., LSI Products Division

The use of digital signal processors is growing at an explosive rate, thanks largely to CMOS. Without it, such processors would run into a power barrier that would severely limit the complexity of future chips.

CMOS puts a feast on the digital signal-processing table. Its circuit speeds approach bipolar's, and its circuit densities make possible a big jump in the integration of signal-processing functions. Since CMOS evolved in high-capacity memories, it can simplify adding fast memories to specialized chips. Not only that, it remains stable over a range of temperatures and tolerates fluctuations in supply voltages.

> "With CMOS, we can create digital signal processors more powerful than anything around."

Digital signal processing requires extremely high speeds—in the area of subnanosecond gate delays. Pushed by 2-μm design rules, CMOS chips will reach that speed before the end of next year. I predict that the industry will be working at rules nearing 1 μm in a few years. Today's geometries fall in the 2- to 3-μm range.

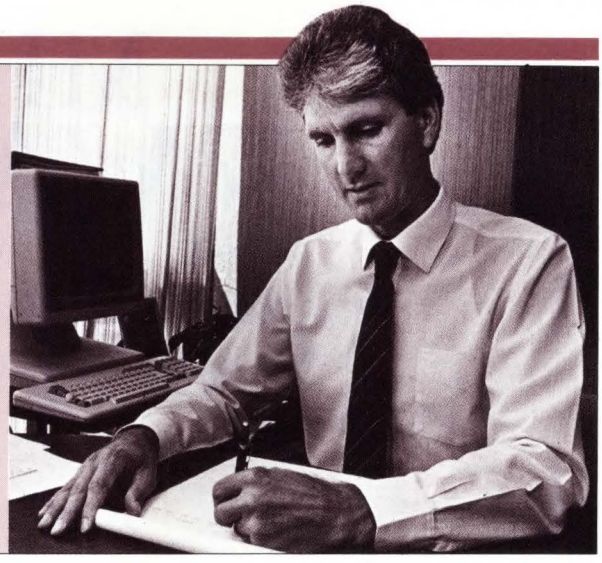
For the immediate future, bipolar will lead CMOS in raw speed; however, it is already straining the power limits of packaging. For instance, a bipolar 16-by-16-bit multiplier can carry out its job in 45 ns, but it dissipates 4 W. Today, we could theoretically fit four of these circuits on one chip, but we could not come close to handling the resultant 16 W. CMOS, on the other hand, delivers not only the necessary circuit densities but does so at a far lower power draw, as well. The equivalent CMOS multiplier would consume only tenths of a watt.

The CMOS design cannot match the 45-ns execution time of the bipolar multiplier. Using the 16-by-16-bit design as a starting point, 2-μm CMOS can crack 100 ns but not 50. Typically, CMOS trails bipolar digital signal processors, performing about half as fast as a bipolar chip using the same design rules. I expect that CMOS will reach the 50-ns mark when design rules fall to 1 μm.

Plastic packages will reduce the cost of many CMOS digital signal processors. Packaging, in fact, now makes up one-third a unit's cost. Bipolar usually consumes too much power for plastic packages, which are one-tenth as expensive as ceramic packages. A high-power bipolar chip housed in a ceramic package could cost about $10 in parts alone; its plastic CMOS counterpart, less than a dollar.

Faced with CMOS's advantages in power densities and packaging, bipolar will be relegated to high speeds, medium-complexity dig-

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ital circuits, and fast converters. Everything else will fall to CMOS.

With that technology, we can add a greater number of functions to chips, creating processors that are far more powerful than anything currently around. We'll see more specialized chips, like floating-point and FFT processors, special multipliers and arithmetic processors, sample-and-hold circuits, digital correlators, sequencers, and accelerators. Beyond those will be general-purpose digital signal processors, as well as bit- or word-slice devices.

Nevertheless, the process is not the best choice for all functions or applications. Take analog-to-digital and digital-to-analog converters. Bipolar remains king of the hill for video-speed flash converters simply because its inherent accuracy towers far above that of CMOS. I don't see CMOS changing that in the next two or three years. It's adequate for successive-approximation converters and lower-end flash converters, but high-performance flash converters demand a number of different but precise voltages—a level of precision that cannot easily be implemented in CMOS.

Several problems continue to plague the technology. For instance, I doubt that we'll get much standardization in the next generation of digital signal processors. True, several low-level functions have already been agreed upon, but the high-level functions and processors will initally be customized, typically through custom or semicustom arrangements.

One requirement for viable custom or semicustom IC design is a technology base that can be alternatively sourced. Bipolar digital signal processor technology is so specialized and varies so greatly in technique that other sources can rarely be found. CMOS, being far more universal, lends itself to second sources.

I think that digital signal processors will follow the example set by telecommunications chips. Individual customers will want an in-house advantage, prompting more specialized chips to be designed into their systems. Furthermore, the complexity of future chips—functional integration, that is—will demand cooperation between the manufacturer and the end user. I expect to see a lot of custom and semicustom relationships being forged to develop complex processing functions in CMOS.

Radiation hardening poses another problem for CMOS. Exposure to high radiation bursts can cause the CMOS circuits to latch up, so that only a power-down releases them. Latch-up in general is a less critical problem for normal CMOS usage. We've solved it by taking certain precautions in our CMOS circuit design and processes. We use a retrograde p-well structure and an ion implant, which consumes about 10% more area.

In the next few years, CMOS will serve even video-speed converters. The thing to remember is that digital signal processing is just now getting started—a lot of analog signal processing has yet to be digitized.

MIKE EVANS

Applications Manager, Logic Group
National Semiconductor Corp.

As the data communications speeds increase, standard and popular processes like NMOS and HMOS will give way to CMOS, even though for a given function, the CMOS IC will likely take up slightly more space.

NMOS and HMOS processes present the designer with an upper constraint—power dissipation. He or she must work backwards from this barrier, limiting gate dimensions and hence chip speeds for a given number of gates per chip.

No such restrictions exist with the CMOS process. Transistor gate dimensions can be tailored to the task at hand. In parallel data communications networks that transmit single-byte or multibyte digital information, CMOS chips have been shown to operate effectively at relatively high date rates of up to 25 to 30 Mbits/s.

One can certainly achieve data rates of 50 Mbits/s and higher quite easily with bipolar ICs. But at such speeds, power dissipation and thermal management problems force a multichip solution, which is economically very unattractive. For a given data rate, a CMOS IC will dissipate about one tenth the power of its bipolar counterpart.

The inherent nature of CMOS (i.e., the fact that only a few of a CMOS transistors' gates are toggling at the chip's maximum data rate) ensures that power dissipation levels of less than 1 W can be maintained at rates as high as 50 Mbits/s.

Even complex data communications chips like high-speed disk controllers dissipate no more than 1 W and less than 1 mW in the chip's quiescent state. And because of the nature of such communication—short bursts of packets—1 W would not prove intolerable for short intervals.

> "Power dissipation levels under 1 W can be maintained at rates as high as 50 Mbits/s."

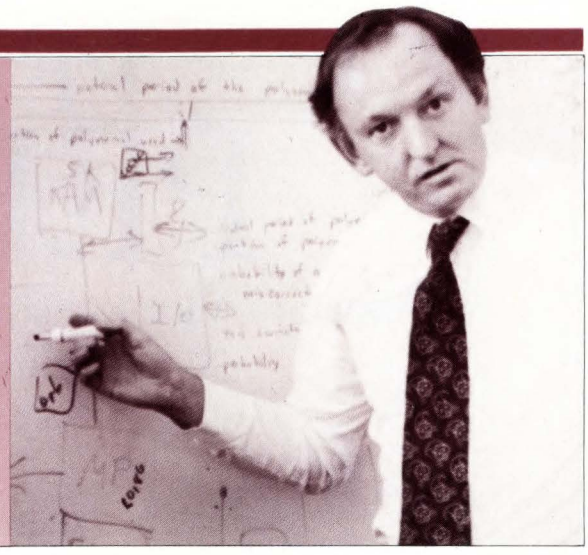
We can expect CMOS to be the process of choice in future monolithic controller chips for high-speed networks handling data transfers of tens of Mbits/s.

CMOS ICs are under consideration for the controller and buffer-management functions of the FDDI (fiber-distributed data interface), for example. This proposed token-passing ring-topology network standard from ANSI (American National Standard Institute) is designed to handle very high-speed data transfers of up to 100 Mbits/s.

Though that speed may not be reached by the end of this decade, we can expect CMOS to reach the 50-Mbit/s mark, and possibly a little higher, within the next few years.

CMOS ICs will also play an important role

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in the controllers of parallel communications systems like local high-speed computer buses. Bipolar devices will still be necessary for high-speed serial communications functions, like those performed by codecs and serial interface adapters.

Eventually, mixed process improvements will lead to single-chip solutions that include both CMOS and bipolar transistors. This trend is certainly starting with lower-speed devices like line drivers and receivers, and can be expected to continue to more complex monolithic functions over the next few years. It is only a matter of time before experiences gained with processing will permit us to have single-chip devices made of both CMOS and bipolar processes.

As data rates rise to the tens-of-Mbit/s range, the advantages of low power consumption begin to take on system-level implications. For one thing, CMOS with its single-supply and low-power-dissipation operating characteristics will allow an overall reduction in the size of the required power supply, saving significant space and energy when compared to NMOS or HMOS devices. For another, heat-management problems on the PC board are considerably simplified.

That simplification means that a greater number of small-outline CMOS packages will be surface-mounted on high-density PC boards. Because of their small size such packages are popular for surface mounting, but they cannot withstand as much heat as conventional dual in-line packages. But with less power dissipation to contend with, thermal-management problems are considerably simplified.

Of course, for truly low power dissipation at very high data rates, gallium-arsenide technology may eventually overtake CMOS. But despite its impressive performance, GaAs technology is far from maturity, and cannot soon be expected to compete with CMOS and bipolar ICs in the high-speed data communications' arena.

The low power dissipation of CMOS ICs will also propel the development of a multitude of remote data communications applications and will enhance the use of portable equipment in the field. CMOS circuits operating from small batteries will become possible.

CMOS modem chips are one reason for this optimism. We're already witnessing 300-baud CMOS modem chips in remote telemetry and dial-up metering applications, and can expect higher speeds, possibly up to 9600 baud by the end of this decade. More functions will be added onto single-chip CMOS modem chips. Incidentally, the switched-capacitor filter circuits of these modem chips are best made with the CMOS process.

We're also using 300-baud modem chips for remote readings of gas, electric, and water meters. Because these chips are made in CMOS, they can be powered directly from the telephone line, without any concern for the ac powerline.

PETER PERRY

Assistant Vice President, Component Design
Mitel Corp.

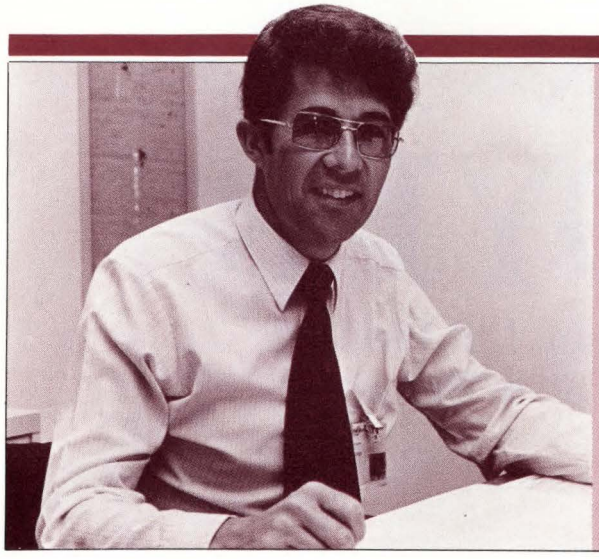
The next generation of telecommunication ICs will demand the integration on one CMOS chip of ever more complex digital circuits and simple but elegant analog functions. The trend toward mixing technologies began just a few years ago with codecs and dual-tone multifrequency receivers and now continues in the digital line interfaces emerging for the Integrated Services Digital Network (ISDN), a standard for end-to-end digital telecommunications at 144 kbits/s issued by the International Telecommunications Union's CCITT (International Consultative Committee on Telegraphy and Telephony). These chips, which link the subscriber's telephone to the central office over twisted-pair wiring, contain an ever larger number of functions, including analog switched-capacitor transmitting and receiving filters, a digital-to-analog converter, a phase-locked loop, and line drivers and receivers. Accompanying those circuits are digital signal processors for adaptive echo cancellation.

> "CMOS circuits will make it feasible to transfer video, speech, and data over narrowband telephone lines."

For some telecommunication circuits—such as those that incorporate battery feeding, overvoltage protection, ringing, supervision, and testing, the cooperation of bipolar and CMOS processes is essential before a successful monolithic version can appear. For now the functions are satisfied only with multiple chips and thick-film hybrids. The bipolar process affords the several hundred volts of isolation needed by the line interface, a measure that protects the circuit from lightning and transient signals. But this will change, when monolithic bipolar-CMOS versions appear over the next few years.

Through the rest of the decade, a 3-μm double-polysilicon, double-metalization process will be the workhorse CMOS process. Two layers of polysilicon remain an important ingredient for elegant switched-capacitor circuits of filters and codecs. Double metal layers are becoming increasingly popular for design automation. That field will become more critical as chip densities rise and intricate circuits move on chip.

CMOS processes will shrink line geometries to 2 μm to accommodate a number of high-performing telecommunication circuits such as the powerful signal processors that will lead to more intelligent telephones. Speech recognition and synthesis chips, some already appearing in systems, will proliferate. CMOS



Peter Perry has been with Mitel in Kanata, Ontario, since 1980. Previously he worked with telecommunication circuits at Plessey Semiconductor. He attended the College of Electronics of Britain's Royal Signals Research Establishment and is a member of the British Institute of Electrical Engineers.

circuits—specifically, bandwidth compressors—will make it feasible to transfer video, speech, and data signals through the narrowband confines of voice-grade telephone lines. Future telephone subscribers can look forward to sending their voice, video image, and even scratchpad information over their telephones.

With bandwidth-compression CMOS devices as their spark, low-power cameras for telephones will take off. Such cameras will combine monolithic imaging arrays of charge-coupled devices with CMOS signal-processing elements. We're already witnessing such cameras being used in robotics and factory inspection.

Higher chip densities and adequate speeds, along with the traditionally low power consumption of CMOS, virtually guarantee the technology a leading position in the switching architecture of private branch exchange networks. CMOS digital crosspoint switches are already satisfying a wide range of telephone-system needs, from a few dozen lines to several hundred. In the future, PBXs will handle several thousand telephone lines, with complex CMOS switching matrices at their center.

CMOS ICs will elevate the status of PBXs from voice-signal carriers to true digital data carriers, advancing the cause of office automation in the process. Only a handful of CMOS ICs will be required for a PBX to act as a local area network.

As switching bandwidths increase, CMOS will be called on for higher switching speeds, with gate lengths and channels widths both shrinking.

By the beginning of the 1990s, the 0.5-μm channel widths of CMOS ICs may no longer suffice; instead gallium-arsenide devices may be asked to fulfill the switching function. Over the next few years, the combination of GaAs diodes and CMOS transistors—as demonstrated by Japanese researchers—may well be the answer to high-speed fiber-optic interface circuits.

Latch-up is, of course, CMOS's Achilles' heel. It could be eradicated, but that would exact a heavy price in process complexity, die size, and ultimately cost-competitiveness. Latch-up threatens to worsen as CMOS IC line widths decrease and chip densities increase. Still, the phenomenon is well understood and should be remedied through improved periphery layouts, retrograde p wells, and epitaxial and oxide-isolation techniques.

If current threshold levels climb to 5 or 10 times those of CMOS chip output-drive currents, then the current overshoots arising from unterminated buses and stray coupling between buses will be far below the levels that can cause latch-up. Alternatively, if the latch-up threshold voltage rises to the same level as the digital signal voltage swings, latch-up may also be contained. Aside from that, care must be taken with power-supply sequencing, but that does not seem a heavy burden.

JON SHROYER

Division Vice President, LSI Products
RCA Corp., Solid-State Division

There is no reason why CMOS logic should not be fully competitive with the advanced forms of its bipolar logic. Today, CMOS discrete logic competes fairly well with Schottky TTL and low-power Schottky equivalents when performing a function. Nevertheless, advanced bipolar processes still win out when comparing raw gate speed.

I see this situation changing over the next 18 months. The gap will be closed by step-and-repeat lithography equipment, dry plasma etching, and the proliferation of the 2-μm CMOS technology that has already been developed for 64-kbit static RAMs, 256-kbit dynamic RAMs, and some semicustom chips.

> "With 2-μm line widths, CMOS discrete logic will begin squeezing out bipolar TTL."

Not only will CMOS discrete logic begin to squeeze out bipolar TTL, I also expect it to start crowding out ECL in some of its traditional applications like mainframe computers. For now, however, it looks like CMOS will capture the bulk of the low- and medium-performance applications while ECL will still dominate the high end of the spectrum.

One of the biggest problems in replacing TTL with CMOS is coming up with a TTL interface. TTL has become almost like a plug in the wall. CMOS will have to be able to fit into that outlet.

As CMOS moves further into bipolar territory, there will be some changes in the present spectrum of discrete logic devices. Semicustom CMOS logic and standard-cell designs in particular will grow in importance.

There will be fewer discrete logic circuits for system designers. With large logic blocks such as standard-cell-based chips and gate arrays available, the broad product lines of older logic families or even the new HC/HCT series will become unnecessary.

What discrete circuits remain will tend to specialize in MSI functions such as line drivers, line receivers, and interface octals, as well as very-high-current drive circuits and some analog functions. That trend, though, depends upon packages with high pin counts becoming readily available for semicustom logic circuits. Currently, a pin-grid array for high-density CMOS semicustom circuitry is much more costly than the conventional dual-in-line package used for discrete logic circuits.

Packaging itself, in fact, will lead the innovations in discrete logic. Eight gates will be integrated into new octal circuits. Thanks to CMOS's low power consumption, more functions can be crowded into a single package.



Jon Shroyer is based in Somerville, N.J. His responsibilities include the engineering and manufacturing of microprocessors and microcomputers. Before joining RCA in 1982, he was general manager of the Semiconductor Division of Data General.

CMOS standard cells—and this would eventually include silicon-compiled circuits—will become a very important form of CMOS logic. Especially at 2-μm to 3-μm line widths, there will be a big savings in silicon area.

Using standard cells will make it possible to incorporate large dedicated islands such as core microprocessors and ROMs and RAMs with variable heights, widths, and pitches. The marriage of CMOS and standard-cell technologies will permit very-high-density functions with extremely low power dissipation.

Another logic device which could emerge as a winner in CMOS is the field-programmable logic array (FPLA), which has primarily been offered in bipolar. The major question will be whether the industry can develop a real cost-effective way of using them. If so, FPLAs could eventually become as popular as the EPROM. Fuses, as used in the conventional bipolar array, would not be an economical approach. Then there is also the issue of testing it. If it could be programmed at a reasonable voltage, like EPROMs and EEPROMs, the CMOS FPLA could be a real winner.

It's still not totally clear what specific techniques will dominate the coming generations of CMOS logic. I don't see standardization around n-well, p-well, or even twin-tub approaches. Looking far enough down the road, there will probably be a tendency to standardize on something that resembles the twin tub.

As for CMOS-on-sapphire, it has its specialities, but its range of applicability has narrowed. We now see it for radiation-hardened and very-high-speed functions. It can compete with high-speed ECL without the latter's power problems and at the 1.5-μm level, it could be cost-competitive with bulk CMOS. But, the success of silicon-on-sapphire will depend on whether companies make an investment in equipment and people.

As of now, the alternatives for 1-μm CMOS and below are bulk CMOS or CMOS-on-insulator. It continues to be the old cost and performance tradeoff issue. The approach that supplies the most cost-effective solution will be the one that wins out. The industry will be making geometries smaller, junctions shallower, and voltages lower.

JAMES TOWNSEND

Strategic Marketing Manager
Toshiba America Inc.

Static RAM capacities and speeds are keeping pace with fast-moving dynamic RAMs; CMOS processes are the reason. As design rules approach 1 μm, fast-switching CMOS lays the foundation for new static RAMs with densities 64 and 256 kbits and beyond and adds the bonus of low power consumption.

The story of CMOS involves reducing parasitic capacitances and increasing packing densities. Furthermore, CMOS static RAMs have been designed to minimize the soft errors that increasingly occur at higher densities—the incorrect data values that result from alpha particles.

> "By next year, more than half of the MOS static RAMs will be produced in CMOS."

Present CMOS static RAMs deliver access speeds as fast as 35 ns. Their capacities range up to 64 kbits. A number of companies are readying 256-kbit devices for next year, and some of these memories will shoot for access in the 50-ns range. Today's techniques are even being extended to deliver 1-Mbit static RAMs—with comparable speeds—by 1988.

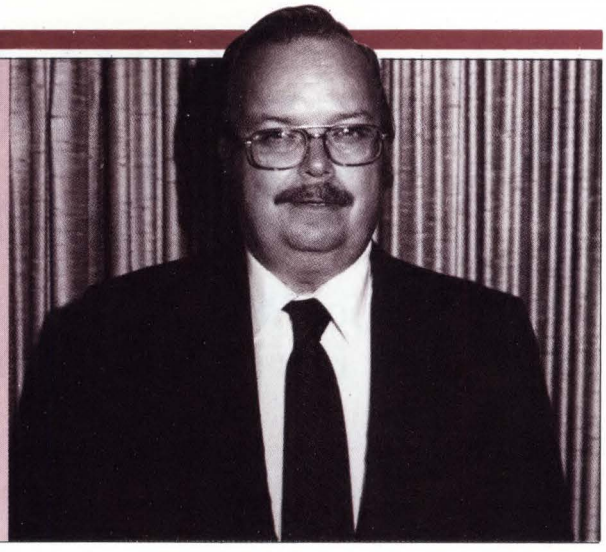
It is in power consumption that CMOS technology truly shines. The operating and standby power of the 64k static RAM are as low as 28 mW and 110 μW, respectively. The 256k versions are projected to consume 30 mW while active and 10 μW in standby. The ratings for a 256-kbit NMOS dynamic RAM, in contrast, are 275 mW and 25 μW.

Static RAMs hold their memory values; they don't require external circuitry to dynamically refresh their memory cells. Dynamic RAMs, because they have simpler processes and memory cells, are cheaper and now lead the advances in memory capacities. However, as their cells shrink in size, they become increasingly vulnerable to false charges induced by alpha particle bombardment. The 1-Mbit level may very well turn out to be the limit for MOS dynamic RAMs, and CMOS static devices may take up the challenge from there.

Static CMOS RAMs are not as susceptible to soft errors—their memory cells are stable because they consist of symmetrically cross-coupled gates in a flip-flop configuration. It takes a lot more charge to change their values than it would in dynamic RAMs. Also, CMOS's p-well structure adds another measure of immunity against alpha particles.

There is a simple relationship between the chip densities of dynamic RAMs and CMOS static RAMs. In general, the densities of CMOS static memories will be one-quarter that of their dynamic counterparts. Today, the

James F. Townsend is strategic marketing manager at Toshiba America, in Tustin, Calif., where his primary responsibilities are product definition and long-term planning. He held various marketing positions at Harris and has been a member of JEDEC's committee on memory standardization.



256k dynamic RAMs are now out and so are the 64k static RAMs; 1-Mbit dynamic memories are in the wings, as are 256k static memories. This relationship will hold for the future.

Both static and dynamic RAMs are dominated by MOS technology; mixed-MOS combinations (CMOS control and NMOS memory cells) and full CMOS predominate. NMOS has the simplest process and therefore the lowest cost. It will always be around as a cheaper alternative to CMOS.

Mixed MOS brings power down significantly, while remaining fairly close to NMOS in cost. In the mixed-MOS devices, two transistors of the CMOS memory cell are replaced by high-value polysilicon resistors, cutting the number of transistors from six to four.

Historically, CMOS static RAMs were much more expensive and slower than their NMOS counterparts. CMOS technology was less developed than that of n-channel, resulting in inferior chip densities and die sizes. Many earlier CMOS designs were copies of n-channel or p-channel and, as such, less than optimum for the new process. As CMOS has matured, chip size, circuit complexity, and speed have improved; CMOS is now closing in on NMOS pricing and performance.

The initial CMOS circuitry was an even balance between p-channel and n-channel transistors. A p-channel transistor, however, requires more space to deliver the same charge because the p-channel holes are less dense than the n-channel electrons. Therefore, as CMOS matures, more n-channel devices are used to save real estate. In some of the newer chips, high impedance polysilicon resistors (1 GΩ) replace the upper p-channel transistors in the last memory cell—delivering higher circuit densities at the cost of increased current. In the future, we'll see more modifications of the basic CMOS circuitry as designers seek higher memory densities.

Latch-up, an earlier CMOS problem, has been brought under control by paying careful attention to horizontal currents in the layout. A number of techniques, ranging from the use of guard rails to process methods, have been successfully adopted to eliminate the problem.

By next year, more than half of the MOS static RAMs will be produced in CMOS. NMOS will not go away—there is room for another NMOS generation. But CMOS will be the most important technology for static RAMs.

We are now entering the next evolutionary stage in CMOS technology; the normal incremental process of enhancement and scaling down to reduce circuit dimensions. Lithography tools are improving, and circuit design techniques are being optimized for CMOS characteristics. Some of the newer techniques incorporate dynamic circuits to reduce operating power, input translation detection to generate timing on the chip, circuit precharging for internal dynamic operation, high resistance polysilicon resistors, and redundant memory.

WILLIAM WAGNER

Vice President, Microprocessor Products
Harris Corp., Semiconductor Sector

The latest generation of microprocessors does not need CMOS simply for low power or high performance; rather it needs it merely to exist. The upcoming 32-bit microprocessors and highly integrated microcomputers cannot continue to evolve without it. Furthermore, since static circuitry in general consumes the least amount of power, it will team up with CMOS for the future devices.

As soon as we crossed the 100,000 transistor level, CMOS became a necessity. Highly integrated microcomputers dissipate far too much heat in NMOS. As a result of this heat, devices are more prone to failure. Reliability is recovered with CMOS circuits, which can run at 5°C over ambient temperature. They don't heat up, and if designed properly, could be inherently more reliable than NMOS designs.

"High-performance microprocessors prove that CMOS has conquered the speed problem."

A few fundamental differences exist between the complex 32-bit microprocessors and the existing smaller ones. The former chips have 32-bit address and data buses, as well as a lot of metal running throughout the package. When going from a 16-bit bus to a 32-bit one, the area quadruples; bringing it down to the size requires shrinking the transistor. For that reason, many 32-bit microprocessors will be built with 1- and 1.5-μm features, instead of the 2- and 3-μm rules for 16-bit devices.

Nevertheless, 32-bit microprocessors will be large even with shrinkage. For instance, one popular 16-bit CMOS chip is about 70,000 mils^2, nearly 50% larger than the equivalent NMOS chip. By the time 32-bit chips move into full swing, they should be about 100,000 to 120,000 mils^2.

The large and extremely complex devices can be built only with CMOS, especially if combined with static circuitry, which dissipates much less power than dynamic circuitry. Static structures can work with clock rates of 5 to 8 MHz and go all the way down to dc. Without even a bootstrap, the system remains fully functional and ready to continue. A static CMOS chip drops from milliamperes to microamperes with no problem—an essential trait for most battery-backup purposes.

Some manufacturers are treading a middle ground—CMOS with dynamic circuits. That combination has the reliability of static CMOS but not the same low power rating, nor can it retain data when power shuts down. Dynamic CMOS chips can only go down to 2 MHz, meaning that a battery backup will not work



William Wagner joined Harris's Semiconductor Sector last year, bringing with him extensive experience in the industry. He previously worked at RCA Solid-State and ITT Semiconductors. He has a BSEE from the University of Illinois.

for very long. And because so many systems need portability and reliability, I doubt that dynamic CMOS will become a viable technology for widespread use—except, perhaps, for cost-sensitive applications.

Portable computers will be the biggest beneficiary of static CMOS, as their most critical operating parameter focuses on power requirements. The new Hewlett-Packard 110, for instance, is fully static and weighs 8½ lb. With a 16-bit CMOS CPU, it sacrifices nothing in performance. These days any lightweight machine demands a CMOS CPU.

In the past CMOS has encountered two main difficulties—speed and cost. High-performance microprocessors prove that CMOS has conquered the speed problem; we can now jump into high-demand areas needing fast execution. The issue of cost is a relative one and should be considered in terms of tradeoffs in the power supply, heat sinks, and the total enclosure—all important concerns in factory automation and military high-reliability and industrial systems. Static CMOS is about 24% to 30% more expensive than NMOS. However, the overall system cost is lower, even though the internal components are 30% higher.

Yet, these percentages are changing. Though CMOS has traditionally required almost double the number of process steps as NMOS, the latest generations of NMOS such as HMOS, now require almost as many mask steps as CMOS. As development of NMOS continues, geometries shrink, and further layers of interconnection are required to tie together the 100,000 plus devices needed for the newer designs, further processing and more mask steps will be required. While this will be true, to some extent also with CMOS, many of these additional layers are already part of today's CMOS processes.

Though CMOS will never totally replace NMOS microprocessors, it will be used for the large, highly integrated devices. The real challenge is deciding what level of integration should be brought to the new generation of CMOS microprocessors.

As for the present limitations of CMOS in building microprocessors, I don't think that there are any from a practical standpoint. From now on, CMOS can only strengthen its hold as the technology of choice for highly complex chips.

RICHARD BLANCHARD

Vice President, Design and Engineering
Siliconix Inc.

Three challenges facing high-voltage CMOS are likely to be met within the next five years: One primarily concerns integrating low-voltage (5- to 20-V) CMOS logic with high-voltage (90-V and up) DMOS, using self-isolation between devices on the same substrate. We call this intelligent, or smart, power, using CMOS logic to control high-current, high-voltage DMOS output devices.

The two other contests are closer to traditional power semiconductor processes used to build high-voltage and high-current switching devices: lateral n-channel, p-well CMOS with junction-isolated vertical DMOS outputs, and a four-layer power device with junction-isolated MOS gates.

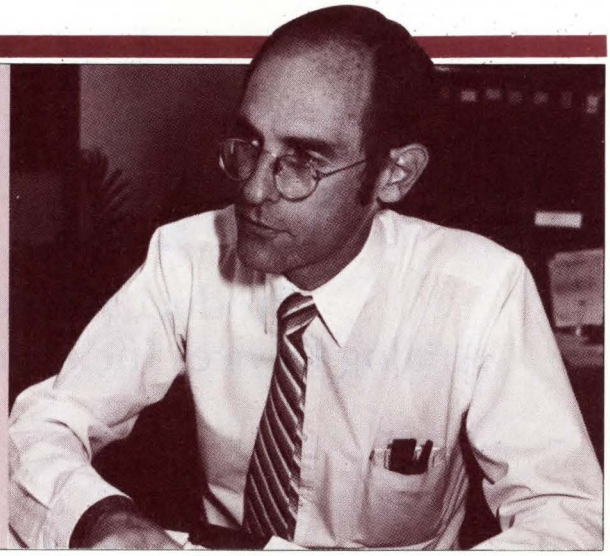
> "Five years down the road, devices may be isolated on a substrate by implanting oxygen at high currents."

The smart power approach is similar to that taken with lateral n-channel MOS structures that employ a modified n-channel transistor for the power device. The technology used for the logic section of these power ICs, evolved originally from metal-gate CMOS, is a high-density oxide-isolated CMOS with an operating voltage in the range of 5 to 20 V. It is also possible to use a 20- to 30-V process that is not as dense, though it has other advantages. It could go into a variety of linear devices such as precision band-gap references, op amps, and comparators for traditional linear applications. In addition to increases in logic speed (beyond the 5- to 8-MHz switching frequencies currently available), density, and finer geometries, other areas for development include mixing analog and digital functions on the same IC.

This self-isolated technology might be well applied to power supplies, telecommunication parts, or semicustom ICs constructed with standard cells. Another use might be electroluminescent display drivers requiring output voltages in the range of 150 to 200 V.

The n-channel output junction-isolated process has the advantage of allowing other structures, like conventional bipolar transistors, to occupy the same substrate as CMOS devices. This process, in addition, allows isolation in the range of 90 to 150 V, and 400 to 500 V for n-channel output devices. It counts among its applications high-voltage multiplexers, display drivers, and voltage regulators in power supplies.

The four-layer junction isolation will supply breakdown voltages only up to 200 V, but furnishes some very high current—up to 20 A with approximately 1 Ω on-resistance. You can



Richard Blanchard has written two books on semiconductors and contributes regularly to technical journals. Before joining Siliconix, in Santa Clara, Calif., he was vice president and founder of Supertex. He holds a PhD in electrical engineering from Stanford.

also get 200-A pulse peaks. The obvious use for this is high-speed power switching. At low currents you can switch within 20 to 100 ns, though higher currents require closer to like 200-ns. This is still a full order of magnitude faster than bipolar devices. These circuits lend themselves to over-voltage protection and high-current ac driving.

Other technologies—like dielectric isolation or silicon-on-insulator—may not prove as useful. One factor is the high cost ($60 to $100) of starting wafers. Currently, CMOS wafers can be processed for a finished cost of $150 to $200 each. Wafer lapping and other insulating techniques would more than double that price.

Five years down the road, devices may be isolated on a substrate by implanting oxygen at very high currents. That would create isolated islands of silicon dioxide in a field of pure silicon. The dosage would have to be in the vicinity of 10^{18} atoms of oxygen for every square centimeter of silicon. To do that, you need very large—100-mA—focused beam currents. The concept is well understood, but the equipment just isn't there. People are experimenting with technology, doing things like 20-hour implants simply to see what happens. Though it's still in its infancy, this kind of process has the potential of making dielectric isolation much cheaper than wafer lapping.

Both the junction and self-isolated high-voltage CMOS processes are limited by the power dissipation of their packages. For intelligent devices, we need more leads than are currently provided by TO-3 and other traditional power packages and more creative ways of dissipating the heat.

Power-integrated circuits and CMOS devices usually trail discrete device technology by about five years. For example, we can now build 100-V/20-A and 400-V/3A power FETs on an IC substrate. That was something that required metal-gate vertical DMOS transistors five years ago. Similarly, we can now put depletion-mode devices on ICs, as well as many traditional linear devices whose precision is ordinarily difficult to control on an IC substrate. These include thin-film resistor ladders (with 10- and 12-bit accuracies before trimming), band-gap references, and precision zeners.

The trick here is to control n^+ and p materials precisely within the context of a DMOS structure. In the future, some of the conductivity-modulated devices that are now appearing only as discretes may be integrated into four-layer IC structures.

One avenue for speculation, in this regard, is the appropriate inputs for power ICs. So much of our work is currently geared toward controlling substantial voltages on the output of circuits that perhaps we need to consider what the real world gives us for inputs. Does it make sense to build photo-optical sensors in CMOS? What about magnetic sensors or pressure transducers? The possibilities are as endless as the applications, and we can be almost sure that work here will reap large rewards.

DOUG GRANT

Product Marketing Manager
Analog Devices Inc., Semiconductor Operation

If one needs both high speed and high resolution in a data converter, CMOS by itself is not the answer. Although practical standard CMOS devices have approached bipolar speeds, attaining gate delays on the order of 1 ns, there are still formidable obstacles to all-CMOS data conversion.

For one thing, it is very difficult to build precisely matched CMOS transistors in volume. What we get are noisy operational amplifiers of limited accuracy, which are unacceptable for high-precision converters.

That is not to say that it is totally impossible to get around the noise and matching problems of CMOS technology. Huge CMOS input transistors will furnish a cure. In that solution, though, the designer loses what is probably the single most important reason for turning to CMOS in the first place: chip density. This obviously can't be maximized if half of the chip is then taken up with input transistors.

Other earlier problems associated with CMOS, such as sodium contamination have been reduced to the point where manufacturers can consistently turn out reliable products at respectable yields.

To delegate analog and digital tasks to their best advantage, the combined talents of two technologies are needed: bipolar for the high-resolution analog comparisons and CMOS for the manipulation of digitized data. The two are most promisingly teamed on the same chip.

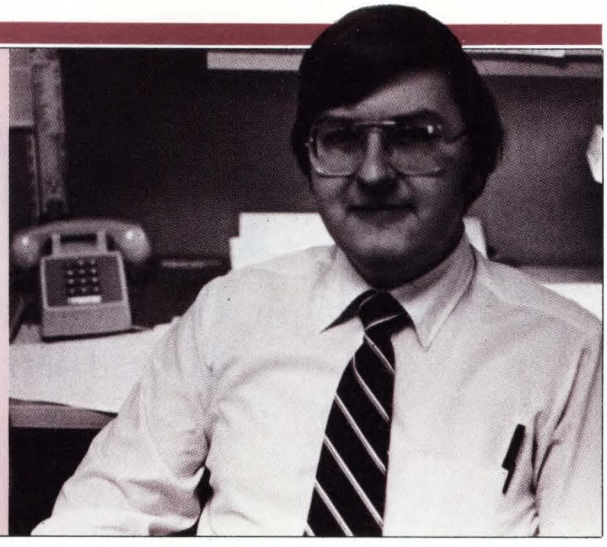
This partnership makes a 16-bit monolithic analog-to-digital converter a very real possibility. The comparator and all other critical analog circuitry are built with a bipolar process, and the components that are intrinsically digital in character, such as switches for the precision resistors, would be configured in CMOS.

> "Data conversion CMOS devices can include endless varieties of on-chip interface logic."

Hybrids have been popular for quite some time now. Yet their fabrication costs give manufacturers pause. Chips for hybrids must be made separately, bonded onto the device substrates, and electrically connected. Furthermore, they take up a lot of pc board real estate.

Due to the very real limitations of analog CMOS, it is difficult to envision all-CMOS successive-approximation data converters with a resolution of more than 12 bits. Bipolar converters will retain this charter for some time yet.

There are, however, many applications of data conversion—in automotive, consumer, and factory automation, for instance—that



Doug Grant is product marketing manager for data converters at Analog Devices's Semiconductor Operation in Wilmington, Mass., a post he has held for the past two years. He joined the company in 1976 as a design engineer for data converters and for microprocessor-based data acquisition systems.

simply do not require high resolution. Here, bipolar's inherent constraints—high current consumption and excessive heat generation—throw CMOS's relative strengths into sharp relief.

Because it is an extremely low-power technology, individual devices can be crammed closely together on the chip with little risk of problems associated with heat dissipation. Additionally, a given digital function can then be configured in CMOS with fewer transistors than an equivalent bipolar device would call for.

Technological advances such as self-aligned gates have helped to lower on-chip capacitances and have therefore improved speed. There are now a number of commonly used CMOS a-d converters that sport conversion rates of up to 30 MHz.

The self-aligned process is another factor that has led to smaller device geometries, increasing density without a commensurate decline in yield. That density, in turn, has spawned a whole new area of multiconverter designs. Multiple converters on a single chip reduce board space requirements and packaging and assembly costs.

It is possible to envision entire families of data conversion CMOS devices that include endless varieties of on-chip interface logic. CMOS switches can be used to build digital systems consisting of registers, controllers, microprocessor data-bus interfaces, or even complete protocol generators.

As a by-product of the CMOS process technology, any number of small-valued capacitors, accurate to within about 0.1%, can be made available to designers at little extra cost. These versatile devices, called switched-capacitors, can be used in lieu of more expensive precision resistors in digital-to-analog converters, if accuracy is not an overriding concern. The accuracy of an all-switched-capacitor data converter is limited by the accuracy of the capacitor, which for practical purposes, cannot be laser-trimmed.

An all-CMOS data converter based on switched-capacitor technology is a good bet for low-resolution applications (under 10 bits).

Another very real future for switched capacitors lies in filters, necessary in certain a-d converters for anti-aliasing or band selection and rejection. Using bipolar-based op amps, engineers will be able to configure these on one chip.

The sample-and-hold amplifier is another candidate for monolithic technology. Switched capacitors, as well as any and all interface logic, no matter how complex, may be fabricated in CMOS. The amplifier would be left to bipolar processes.

What we see, then, is that for low resolution applications, there is simply no limit to what can be done entirely in CMOS. For those applications requiring higher resolution, BiMOS-type monolithic devices can replace what today takes entire printed circuit boards.

TOM SPRUNGER

Manager, Operational Amplifier Products
Texas Instruments Inc.

The benefits of silicon gates have brought CMOS technology to formerly bipolar linear circuits and applications. They have accomplished this by fulfilling two critical requirements that frustrated the process in the past: a stable threshold voltage and a wide voltage range.

A bipolar circuit optimized for stability may have a variation of only 1 μV/°C, but at a great sacrifice in speed; typical bipolar circuits have an offset voltage instability of 10 μV/°C. A silicon-gate linear CMOS circuit can have a 1- to 3-μV/°C change, which is quite an improvement over the unstable threshold voltages that went along with metal gates.

Time variations have made impressive gains, too. Linear CMOS op amps drift only 1 μV/month, half as much as bipolar units. As for voltage drift, a linear CMOS silicon-gate circuit shows a drift of 12.5 mV/V. By this specification, we really see that linear CMOS has arrived; it is almost as stable as low-drift bipolar and biFET devices, which came in at 0.04 mV/V.

With silicon-gate CMOS, we can now consider all linear devices potential targets for CMOS. Each kind of linear IC type may need specific refinements in the technology, but there are some definite areas that can be improved upon to enhance the entire collection of devices.

CMOS will broaden its horizons by widening its voltage range still further. Although it can now furnish a voltage swing of 18 to 20 V, many applications demand a swing of more than 30 V in range. This will come within two to three years and will be used in some of the existing ±15- or +12-V sockets.

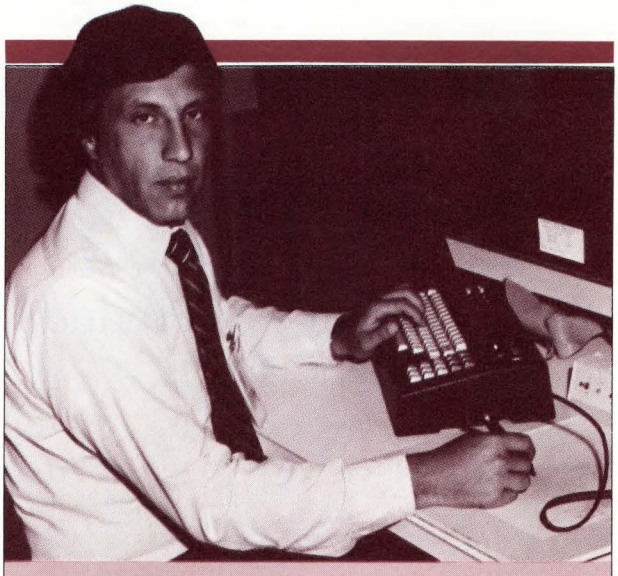
> "With silicon-gate CMOS, we...consider all linear devices potential targets for CMOS."

To extend that voltage range, the drain and source must be spaced to allow for the depletion that is generated at high voltages. P-channel devices have rather long channels now, in excess of 10 μm. However, n-channel components are typically 5- to 7-μm—that should be increased to the 7- to 10-μm range.

At the same time, guard ring structures will be changed somewhat by lowering the doping concentration and narrowing the spacing. That will minimize parasitic transistor action.

Finally, by thickening the field oxide beyond the current 10,000 Å, parasitic transistor action at higher voltages will be lessened. A word of caution is in order here, though: Too much thickness will be a cause of junction problems.

Speed, as well as voltage range, will certain-



Tom Sprunger has been with Texas Instruments in Dallas since graduating from Purdue University in 1972 with a BSEE. He has held several semiconductor design positions in the automotive, photographics, video game, and radiation-protection areas.

ly see improvement. Through new circuit design techniques and changes in geometries to reduce capacitance in key areas, CMOS will make the 4-to-5 MHz range in the foreseeable future. It will compete favorably with today's very fast biFETs, and find applications in data acquisition, telecommunications of high bandwidth, and industrial controls.

Although noise is not a major problem today, we'll see some quieter parts. Most importantly, the current at the input stage will be changed from 1 mA to 2 in the high-bias mode. Thinning the gate oxide and enlarging the width of a device will also lessen noise.

Currently, CMOS op amps have an input noise voltage density of about 30 nV/$\sqrt{\text{Hz}}$, the same as typical biFET parts. Both bipolar and metal-gate CMOS perform more quietly at 10 to 15 nV/$\sqrt{\text{Hz}}$, and silicon-gate CMOS should get from 10 to 12 nV/$\sqrt{\text{Hz}}$ in the next few years. Any precision instrumentation stands to gain from those advances. Bipolar super beta parts are now being used for such small-signal applications; in the future, CMOS will answer those needs.

Lower offset voltages will be a concommitant requirement with higher precision and low noise. CMOS's current 2-mV voltage offset will be improved to under 0.5 mV, probably by trimming the devices at the probe. Trimming resistors will be fabricated into the device to attempt a perfect match. That would theoretically obtain a zero offset, desirable for any op amp.

Still further out, the output current capability will be boosted. This will demand a direct tradeoff with die size. Eventually, designers will put bipolar transistors on the outputs to increase the drive. This, however, will greatly add to the complexity of the process and to the cost of the wafer.

Keep in mind that there is no such thing as the ideal op amp, and there never will be. Perfection notwithstanding, linear CMOS has opened up a complete group of products that were not possible in CMOS, only in bipolar.

Finally, even though silicon-gate CMOS is not optimized for digital circuits, it builds very respectable digital devices. So digital and analog functions may be combined on the same chip. A good candidate for that would be the data acquisition function, combining dense logic with switched-capacitor filters.

EDWARD ROSS

Vice President, LSI Products
Signetics Corp.

Let's go beyond the obvious benefits of low-power CMOS in hand-held devices: The real advantage of CMOS in consumer applications is its ability to integrate complex analog and digital circuit functions on the same chip. CMOS is turning out to be the technology of choice for the kind of system-level integration that once required a mixture of semiconductor approaches—bipolar for speed, NMOS for density (especially in memories and digital circuits), and specialized processes such as thin-film deposition.

The particular advantages of each of these is satisfactorily combined in CMOS. Consequently, it is very clear that much of the electronics world will be coming around to this approach.

Although this trend is most evident in microcomputer and memory components, it will be true for consumer ICs as well. Bipolar and NMOS circuits now being developed and used for digital television applications, for example, are good candidates for conversion in years to come. There are, in fact, strong similarities in the processes used to manufacture memories and consumer linear ICs. Both memory and linear circuits require up to 12 or 14 masking steps, which produce ICs with 3-μm or smaller line widths and multiple-level interconnection schemes.

But this is only the current state of the art—some of the best consumer uses for CMOS have barely been conceptualized.

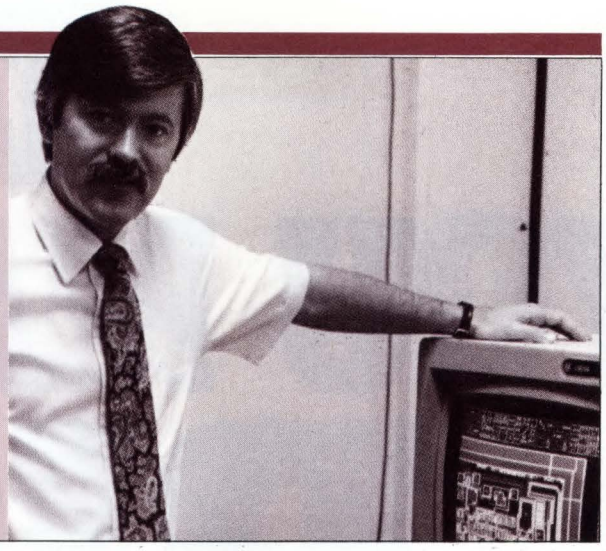
Try to imagine the kinds of devices to be built five years down the road with 1-μm geometries. Picture, if you can, circuits so dense that a microprocessor occupies only one segment of a combined linear and digital chip. With 6- or 8-in. wafers, chips with more than 100,000 transistors can be made cheaply enough to be used in high-volume consumer applications.

> "Some of the best consumer uses for CMOS have barely been conceptualized now."

Another factor to be considered will be automated design processes. Silicon compilers and standard-cell technology are currently being applied to digital design, but they are likely to have a major impact on consumer devices as well. A large portion of consumer circuits is now developed from custom circuits, but the engineering-intensive design processes have been time-consuming and costly and have frequently limited the kinds of projects that a semiconductor company undertakes.

In the future, silicon compilers—the flexible standard-cell concept applied to consumer linear circuit design—will speed up that process. On an engineering workstation, key elements can be called out from a library of pre-

As vice president and general manager of Signetics's Linear LSI division, Edward C. Ross is responsible for marketing consumer and linear circuits developed by Signetics and Philips International. Previously, he directed National Semiconductor's CMOS facility in Scotland. Ross holds a PhD from Princeton.



viously digitized circuits. Linear system design then begins to resemble a cut-and-paste routine that can be frequently accomplished by a junior engineer. That will not only ensure extremely high levels of system integration with very rapid turnaround and low cost, it will also increase the number and varieties of consumer CMOS circuits.

In this context, let me give you some flavor of the kind of circuits we're likely to see in the near future. In cellular radio applications, portable radio-telephones will be among the first devices to benefit from CMOS technology. You need density to shrink complex circuit elements, such as telephone dialers and rf transmitters and receivers, into LSI parts. You need low power consumption for portability. You need speed for rf applications. And you need built-in intelligence to identify which of hundreds of cell locations is actually being used.

Smart telephone" features—automatic dialing, automatic answering, automatic retry and many others—will benefit from CMOS-based components that not only must be able to generate tones or pulse codes, but also must include memory to store and recall previously dialed numbers. In addition, there are on-board oscillators and control and address logic, which provide good examples of the kind of mixed analog and digital functions that must be performed by the same chip. Future generations of ICs will include more RAM, ROM, and intelligence for expanded features.

There will be new radio circuits that use digital signal-processing (DSP) techniques. In automotive radio applications, for example, linear input signals will be digitized by an analog-to-digital converter on the DSP chip. The signal will then be manipulated by a dedicated digital processor and finally reconverted by an on-chip digital-to-analog converter. The analog output will be presented to an audio amplifier, which in turn will drive a low-impedance speaker. With the amplifier included on the DSP chips, the same technology can be applied to hand-held and pocket-style radios, as well.

LCD and LED display drivers and CMOS microcontrollers (80C48 and 80C51 types) will also contribute to automotive circuitry in a much bigger way. In fact, a big feature of automotive electronics in years to come will be the ability to control not just the radio but the passenger's environment and the engine control system as well.

Also on the horizon, energy-management systems for homes and offices will use low-power devices to monitor and control power consumption without presenting substantial loads themselves. Lighting, for example, can be controlled to match weather conditions, dimming on sunny days or automatically brightening on overcast ones. The potential cost of energy management in CMOS control systems stacks up very favorably next to the potential savings in electricity for an office skyscraper.

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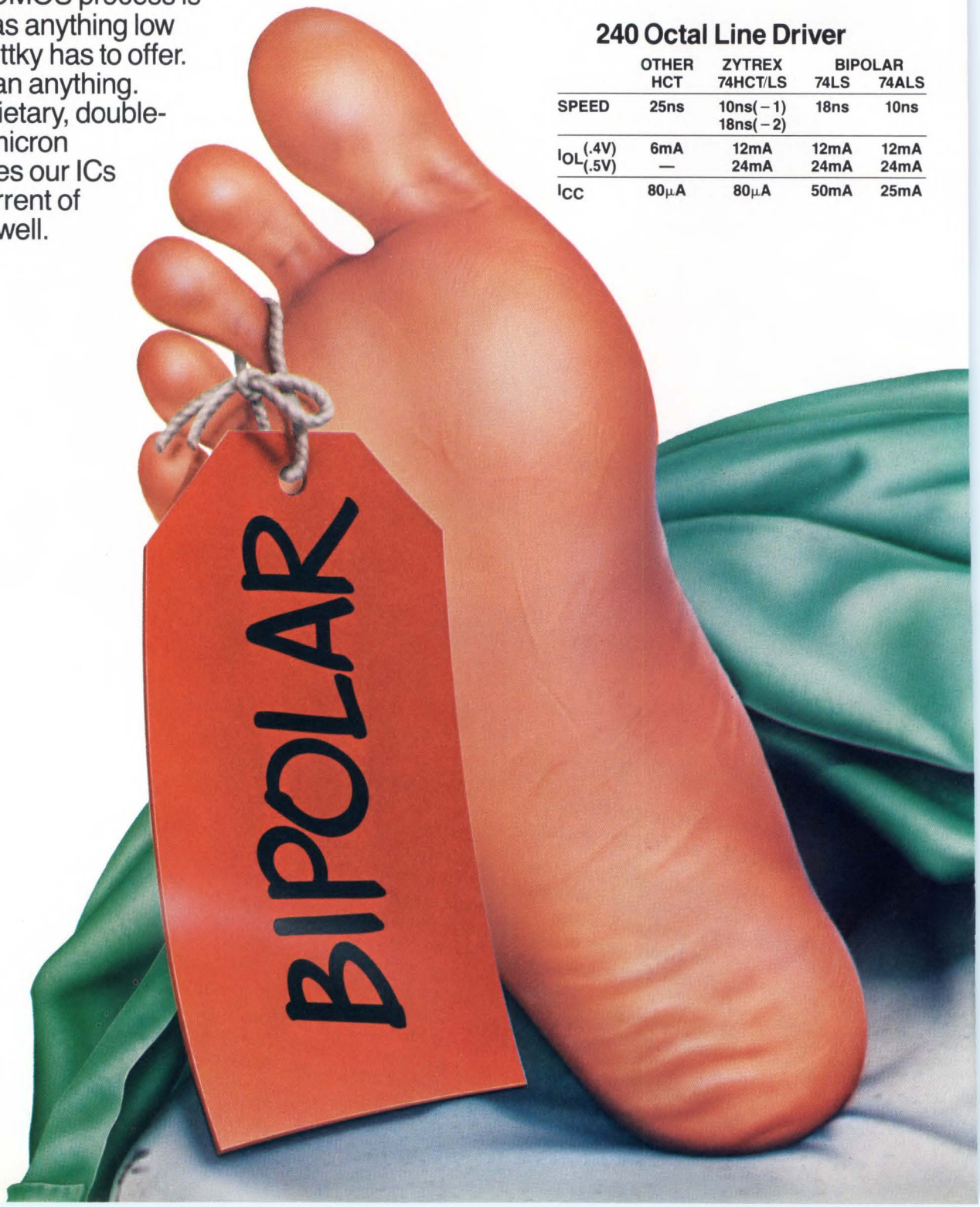
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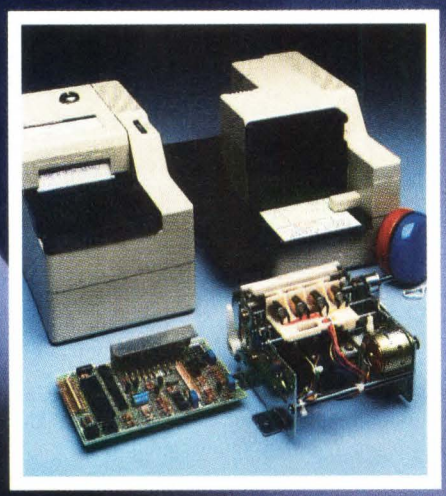
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Silicon compiler lets system makers design their own VLSI chips

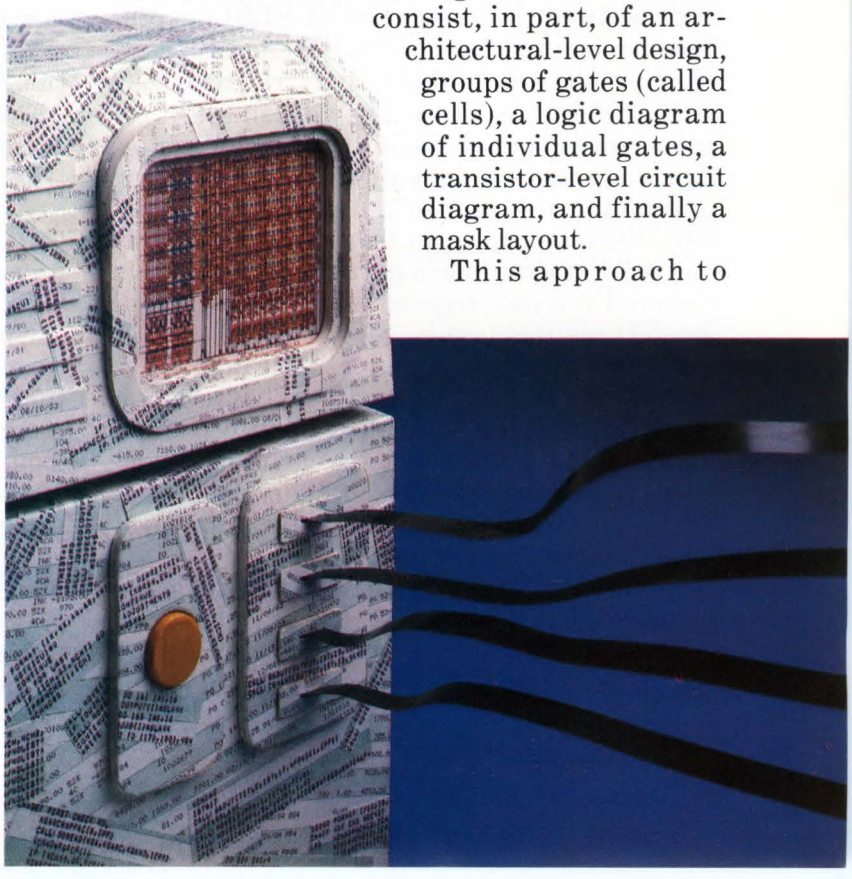
Despite powerful tools, designing custom VLSI circuits is slow and inefficient. A turnkey silicon compiler now streamlines the job, making the task comparatively a snap.

The promise of VLSI technology has always been a little brighter in theory than in practice. Until system designers are able to develop circuits that meet their exact needs quickly, easily, and at a reasonable cost, they will have to compromise their best ideas. When those who build systems can themselves design custom chips for the job, they will no longer have to settle for less than optimal designs pieced together from standard chips.

Relief from this limitation is now appearing in the form of silicon compilers. Just as software language compilers freed programmers from attending to the minute details of the native instructions of a computer, silicon compilers promise to remove a mountain of details from the shoulders of IC designers. More important, they will open the door to VLSI design for system designers themselves. Silicon compilers even make it practical to try out different architectures and find the best one before going on to complete the project.

Despite twenty years of IC design and the help of increasingly sophisticated CAD tools, the IC design process has changed very little. It remains a task of decomposing, designing, and verifying an idea through at least five levels of abstraction and increasing detail. These levels consist, in part, of an architectural-level design, groups of gates (called cells), a logic diagram of individual gates, a transistor-level circuit diagram, and finally a mask layout.

This approach to



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Cover: Silicon compiler

VLSI design is inherently inefficient because the designer must commit to a specific architecture and fully verify it at one level before moving on to the next. After the laborious job of coding a cell-level design into a logic simulation model, and the weeks or months spent getting it to work, a designer must start over at the gate level and often again at the transistor stage. Designed this way, an integrated system of 60,000 transistors might require 15 technical experts, three years and several million dollars. Such tremendous outlay demands that chips be made in large quantities, forcing IC makers away from custom designs and toward standard products. Yet this entire state of affairs is inconsistent with the needs of system manufacturers. These are under intense competitive pressures to implement low-cost designs with fast turnaround times, sometimes with only a year allowed between a project's conception and shipment.

VLSI design semantics

The chip design situation is analogous to that of the computer industry less than thirty years ago, before the advent of high-level languages and the software compilers that translate them into machine language. A silicon compiler is also a computer program, one that understands the semantics of VLSI design. That understanding is possible because all VLSI circuits are designed from structures that can be categorized into a few dozen families. Each family represents a high-level abstraction, such as a shift register, a FIFO, or an arithmetic and logic unit. A particular structure within a family, in turn, is called an "instance." For example, a parallel loaded, 16-bit up-and-down shift register is one instance from the shift register family.

Within the silicon compiler, those families of structures are used as operators that accept a user's inputs as operands and generate a tailor-made instance at the geometry or timing-model levels. In this way, the VLSI details that are below the architectural, or block diagram, level are invisible to the designer.

Building a silicon compiler starts with developing accurate models for each family of structures required to design and verify ICs. These models must address factors such as functionality (to facilitate simulation), performance (to make a timing analysis) and layout. Once developed, these models are encoded as synthesis rules in one or more computer programs.

The silicon structure instance generated, or synthesized, by a compiler is called a block; the synthesized model for the structure's function is called the block functional model. The corresponding model for timing is, not surprisingly, called the block timing model. In all, the programs for generating the blocks are called block compilers. Since as many as 50 different families of structures are involved, and the synthesis rules for each set must be capable of generating hundreds of thousands or more varieties of each type flawlessly, the block compilers, as well as the tools to verify the overall design, are difficult to create.

A silicon compiler has intrinsic functional simulation and timing verification capabilities that operate directly from the models synthesized by the block compilers. Compare this with the traditional verification method. There a VLSI circuit's performance and functionality is predicted by extensive simulation at the more primitive gate, switch, and (with the help of circuit analysis programs such as Spice) transistor levels. In this case the designer translates the circuit's gate-level design into a simulator language and applies test vectors. While the simulation confirms the design's function at this point, timing can only be estimated.

Only when the layout is complete can the designer use sophisticated CAD programs to extract an electrical model of the entire circuit, and draw hard conclusions about timing. At that point, problems are revealed, and corrective action to modify the layout can take weeks or even months.

On the other hand, a silicon compiler performs a functional simulation at the architectural level and a static timing analysis based on a model of the final layout. The functional simulation, sometimes called register-transfer level (RTL) simulation, models a circuit using those few dozen structures defining the architecture. Compare this to other techniques, which typically must model many thousands. With the appropriate block-compiler algorithms, the compiler can synthesize a functional model (for functional testing) and an elec-

trical model (for static timing analysis) for any block or collection of blocks.

Silicon compilation promotes more efficient designs by simplifying architectural exploration. A designer requires critical feedback about his circuit's functionality, power, performance and cost. If the designer can quickly make "trial" architectures and then receive such feedback on the entire circuit or any portion of it, his ability to explore alternative architectures and to converge quickly on an optimum final architecture is considerably enhanced. Silicon compilation techniques include estimation and prediction algorithms that, in combination with the intrinsic functional simulation and timing analysis model synthesis, complete the entire suite of modeling required to perform VLSI design.

If the procedures followed by experienced VLSI designers are implanted carefully enough into the silicon compiler, the results can equal that of "hand-crafted" circuits in less time, and most importantly, they can be achieved by those 99% of engineers who have no direct experience designing silicon.

Finally, silicon compilation overcomes two other problems of traditional VLSI design. When using custom VLSI circuits, system manufacturers usually have to give up the safeguard of a second source, because such circuits are typically designed for one particular IC vendor's fabrication line. Moreover, the pace of technology can quickly make any custom circuit obsolete. A silicon compiler, on the other hand, can be recalibrated to generate optimal layouts and accurate timing information for an entire range of processes within a major family, like 2-to-5-μm, single-layer NMOS.

To achieve its goal of almost instant design and verification, a silicon compilation system must include a functional simulator, a static timing analysis system, and an effective user interface. Such a system contains all the components of VLSI design and, unlike traditional methods, it is usable by any engineer comfortable with architectural-level design.

One-stop VLSI design comes in a system that allows tests, refinements

A system that turns a designer's block diagram into a mask for producing a VLSI chip is a powerful tool. Yet even it cannot ensure that the chip will work, let alone embody the best approach to an application, unless it can also test a design before committing it to silicon.

The first such development tool, called the Genesil system, is made up of a powerful silicon compiler, including circuit-simulation software that runs on a substantial complement of hardware: a VAX 11/750 with 4 Mbytes of main memory and a 450-Mbyte Winchester disk drive, four 1k-by-768-bit color graphics terminals with mouse pointers, and an 800- and 1600-bit/in. magnetic tape drive (Fig. 1).

Stephen Johnson, Silicon Compilers Incorporated

A system maker's system

The Genesil system is for those electronic system manufacturers that could benefit from integrating their designs, but have been stymied by the high cost and complexity of creating a VLSI circuit specific to their application. It lets system engineers, using what they know about design, develop fully custom VLSI circuits without resorting to compromise measures such as gate arrays and standard cells. In other words, the development system elimi-

nates the need for what could be called VLSI literacy. Significantly, it opens the door to exploring and refining a system at the architectural level.

Moreover, because the performance and density of the circuits it produces rivals those of hand-crafted designs, the system is equally well suited for use by IC manufacturers.

Many functions

As a tool for designing and implementing VLSI, the IC development system encompasses a wide range of functions. It lets the engineer specify a design and then compile the separate blocks, modules, and even chip-level structures that make it up. The system then simulates the design's function and analyzes its timing in order to verify that it will work when built. Once a designer is satisfied with the chip's performance, the system generates a mask manufacturing tape, which is used to create the actual device. Beyond these essential tools, the system has a hierarchical data base manager and, finally, a unique style of data entry that makes specifying and changing the structure of a design as easy as filling out a simple form.

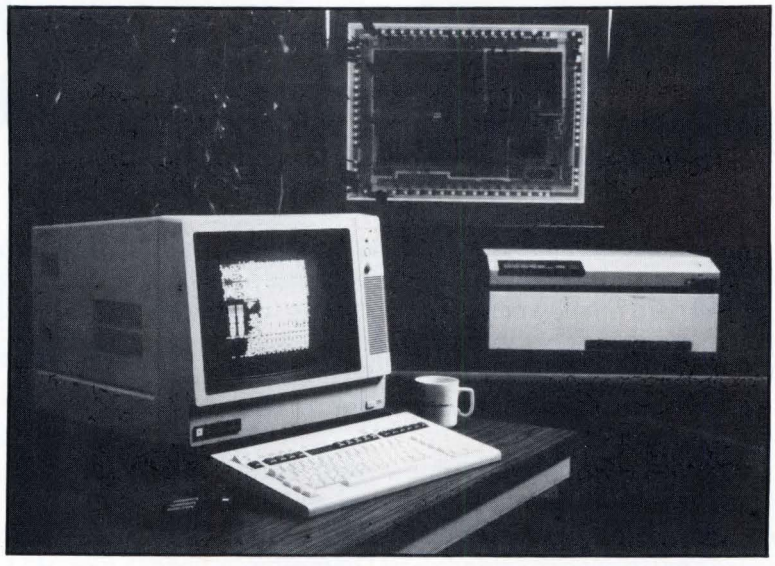
An engineer can adopt a top-down, bottom-up, or mixed style of design using just three fundamental structural elements of the VLSI development system—blocks, modules, and chips. Blocks are the most primitive of these three objects, yet are actually complex structures, like an ALU, synthesized by the system's block compilers at the user's request. Modules, in turn, are composed of blocks and other modules.

For example, a part of a particular VLSI design might consist of RAM, data buses with latches and multiplexers, and an ALU, each of which is considered an individual structural block. If the designer found it convenient to identify these blocks and their interconnections as a bit slice, he could treat such a traditional unit as a module and invoke it as such throughout the remaining design.

Finally, the highest level of architectural definition is a chip, which is nothing more than a module that has bonding pads.

Families of functions

The development system includes block generators that synthesize a nearly unlimited number of blocks from several dozen structure families, called functions. These families go by meaningful names like ALU, Barrel Shifter, Dual-Port RAM, Programmable Logic Array,



1. The Genesil System translates an architectural-level VLSI design directly into a mask generation tape. It runs software for silicon compilation, including functional testing verification, and timing analysis on a VAX 11/750, 4 Mbytes of main memory, and its associated hardware.

Interface, FIFO, Read-Only Memory, and Random Logic.

The process of synthesizing a particular block, for instance, of a function begins when the designer specifies block characteristics by filling out a form displayed on the workstation's screen. From these particulars, the development system creates the custom circuit layout, simulation model, timing model, and a timing data sheet. The synthesis portion of the development system is rule-based and generates the correct models and an efficient layout for the particular fabrication line and semiconductor process that is targeted to produce the actual silicon. Moreover, the synthesized block is completely self-contained: its internal "wiring" is automatically generated, as are the locations of all external signal connectors (the external signal points of a block or module).

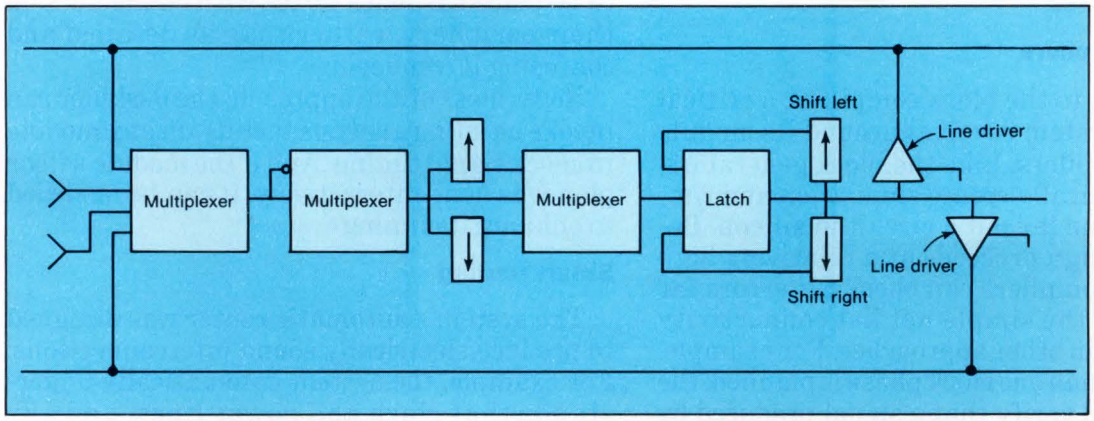
Net list now or later

When two or more blocks or modules are to be connected, the designer is given two options for entering the net list that interconnects them: implicit and explicit net list entry. The first calls for the designer to supply the names of signals for each connector to the block generator at the same time that the rest of the block is being specified. For example, when entering the specification for an Interface block, the designer might request a two-way multiplexer to route data from one of two buses; the system would then recognize the need for a multiplexer control signal and immediately give the designer an opportunity to enter a name for that signal. If the designer chooses a name at that time, it is automatically connected to all signal lines with the same name on any other module or block within the chip.

In contrast, the explicit net list option lets the designer defer the naming of signals for a particular block until that block and its surrounding structures are fully specified. Then the designer enters a net list explicitly, in terms of the surrounding blocks and modules. Explicit net listing makes sense when the block being generated is to be shared with other designers or used throughout a design—in other words, when the context for names does not become clear until later in the design process.

Display reflects changes

As a designer completes the input specification of a particular block, the system responds by automatically displaying a color-coded block diagram of the system (Fig. 2). To aid the de-



2. As the designer specifies the details of each structural block of a VLSI architecture, the system displays corresponding color-coded representations. If, in the course of refining his or her ideas, the designer changes the details of a block, the display automatically reflects these changes and flags any errors.

signer in exploring different architectures, a block adjusts to reflect changes as they are entered. Also, any semantical or syntactical errors made in specifying a block will prompt error messages to appear, as well as a visual indication locating the source of the error. By making such checks, the system determines if all the options of a block will work together, and that all the required information has been entered. Moreover, when it comes time to compile a block and generate its layout, the system will not produce a block that violates any layout, electrical, or logical design rules.

The development system yields layouts and models from even sketchy information for the purpose of planning and estimating the outcome of a design. As the user gains insight and fills in the details, they are reflected in the circuit models and layouts. In this way, the design proceeds in a natural, iterative style that is not possible with other approaches to VLSI. Also, a design's layout geometry and its models for functional simulation and timing analysis are tightly coupled to one another so that the designer can verify the behavior and performance of an idea interactively. This is done without the inconvenience of shifting to other tools or converting to different data formats or operating procedures.

Watchful compilers

In addition to the block compilers, a critical part of the system revolves around its module and chip compilers. Like the block generators, they automatically create simulation and timing models and lay out a circuit in silicon. Because the design proceeds at a relatively high level, these compilers can check for errors far subtler than the simple net list connectivity checks found in other approaches. For example, where more than one clock phase is planned, the compilers will verify that a signal produced by one module meets the clock phase requirements of each module that it feeds.

To help save time and effort, wherever possible, connections inside modules occur automatically, a feature called intrinsic routing. Modules with intrinsic routing, typically those that are made up of registers, ALUs and output logic, have their constituent blocks automatically interconnected. Here the designer has and needs no control over the floor plan (placement) of the blocks. The compiler therefore eliminates the biggest source of a VLSI chip's cost—the channels through which interconnections run.

Designer's judgment

In cases where modules are composed of blocks from functionally unrelated families, extrinsic routing is used. In this mode of operation, the designer interactively specifies every module's floor plan and the net list for its blocks. But the actual routing is still completely automatic.

Interactive floor planning is entirely feasible and even desirable for the designer on the Genesil system since, even in a very complex chip, the total number of modules is usually between 10 and 50 and handled better by the designer. In contrast, even simple gate-array and standard-cell layouts have thousands of elements to be placed, a task that requires automation and suffers from its associated inefficiency.

Interactive graphics expedites the floorplanning, and special net list entry commands direct the fully automatic routing. The interactive graphics shows the blocks and modules to be placed as black boxes with connectors on their periphery, rather than as detailed and confusing IC renderings.

Regardless of the approach, the designer can invoke a timing analysis facility on any module to check signal timing. And if the module's floor plan was done interactively, it can be modified to enhance its timing.

Smart routing

The system's automatic router was designed to produce electrically sound interconnections. For example, the system automatically understands that clock and power lines, and any signals identified by the user, have a high priority and routes them accordingly. Moreover, it sizes those lines to ensure that each maintains the proper current density and a suitable signal level. In fact, the designer never sees, edits, or need directly influence any module or chip routing. Once the function of a module is verified, then its actual laid-out and automatically routed version will also be correct, since the

functional simulation model and the interconnections come from the same internal data (the designer's input specification) for the module.

Several other features, or subsystems, of module and chip editors make a designer's life easier. A full plotting feature displays or prints out block diagrams, floor plans, package pinout drawings, and bonding diagrams. The information for both package pinouts and bonding diagrams comes from the user during the chip specification phase of the design. (Also, although never needed during the design process, the system produces scaled, color drawings of the final geometric layout).

In addition, the designer need only indicate a chip's I/O pins in terms of package pin numbers, rather than through the error-prone task of specifying IC bonding pads. This is because the system "knows" about different packages through its built-in (and expandable) package library and, during compilation, attempts to place die bonding pads in accordance with industry-standard or user-defined rules.

Functional modeling important

A designer using the new system experiences unprecedented flexibility in refining an idea and therefore ensuring its success. Consider that, ultimately, the key to a successful VLSI design lies in an accurate functional simulation, and hence verification, before the chip is actually built. Recognizing this, the development system's creators have made it possible to progress in seconds from specifying a design to verifying it.

With a comprehensive functional test sequence set up, a designer can apply it as any change, large or small, is made to a module. What's more, the system's functional simulation is fast and effective because it generates models at a high level of abstraction, never at the gate or switch level. A model's function is guaranteed by the compilation process to be correct.

By incorporating an instrumentation package, the system's functional simulator appears to the designer like a logic analyzer. To use the package, the designer, with the help of a setup facility, creates test patterns or even entire test programs, with breakpoints, loops, case statements, and conditional executions. Then he or she defines unique sets of screen formats, which tests can be stored for later use. These formats determine how the simulation will appear on the display and are "painted" with commands like ARRAY, INDEX, VALUE, LABEL, HISTORY, and TIMING (see the table).

Poking around

The instrumentation package also lets a designer interactively insert signals into a simulated module or an entire chip. Using commands like BIND, ASSERT, and PROPAGATE, the effects of different logic values can be studied. A designer can also insert a value into a model by simply typing a new value over the old one displayed on the screen. Additional commands like QUERY, CHECK, and PRINT help the designer to determine the results of a simulation.

Finally, the simulator's setup mode changes the state of a simulation globally. For example, it enables the designer to define or delete all clocks, vectors, and mnemonics; to issue resets;

Commands invoking the instrumentation package

Command	Action
ARRAY	Displays address and contents of array-oriented devices such as RAMs, ROMs, and PLA's
INDEX	Defines an input field when an address entered returns the corresponding contents
VALUE	Translates data into any radix or mnemonic
LABEL	Marks display areas with helpful remarks
HISTORY	Scrolls through current and recent vectors
TIMING	Draws signal-timing waveforms
BIND	Holds a node at a constant value
ASSERT	Initializes a node to a value
PROPAGATE	Propagates asserted values through logic
QUERY	Returns the state of a vector
CHECK	Compares a vector with a mask
PRINT	Produces a hard copy output

to load and clear the contents of RAM, ROM, and PLA arrays; and to halt the simulation at a certain point, called a checkpoint.

Timing tested, too

Beyond functional simulation, a critical phase of a chip's development is an analysis of the timing relationships among its many signal paths. In a classically designed VLSI, timing performance is derived by extracting all the parameters of the layout and inserting them into a switch- or gate-level simulator model. The new development system, however, separates its timing analysis from the process of simulation. As a result, it is fast, about 2000 transistors/min; accurate to within 10% of a Spice analysis; and exhaustive, although it requires no test vectors to be generated.

The timing analysis is done from a timing model that is synthesized whenever a block or module is compiled. The model consists of accurate circuit representations at the transistor level and includes all intrinsic resistance and capacitance values, as well as those parasitic elements contributed by the interconnection network. Moreover, the model resolves all signal flow directions and classifies transistors into about half a dozen types, like precharging, discharging, and pull-up. In addition, the timing of a block is based on the system's built-in knowledge of the chip's most important parameters, from which the system creates a timing data sheet, similar to that found in a typical component data sheet.

Tailored to a fabrication line

Timing analysis also accounts for a particular manufacturer's specific fabrication line, allowing the designer to compare the performance of a circuit made by several manufacturers by simply changing the associated parameters and recompiling the design.

Also, an approximate timing analysis can be performed on any block, module, or chip without the time-consuming routing that must ultimately be done between each block or module. Instead, a fast routing estimator gives a quick indication of a design's timing performance. The most accurate timing analysis, however, must account for the effects of the interconnection impedances and therefore requires that the connections be already routed.

Once the routing is complete, the system's timing analyzer examines every possible path through a block or module to determine the worst-case timing delays. It then produces three reports for the designer: a timing report, a node-delay report, and a delay-path report.

The timing report identifies those paths that establish the minimum clock periods and duty cycles, and it gives their values. It lists these paths, in order, from worst to best. It also gives the total cycle time for each module, displays the set-up and hold times for various signals, and calculates how long after a clock transition a signal will be available. The second report displays the maximum and minimum delay time for a given node with respect to a clock, and the delay-path report lists those paths that set the maximum and minimum delay between any two nodes.

Since the timing analysis might report paths that would never occur in practice, the designer can filter out such unwanted and illogical results with the help of the system's set-up feature. This feature allows nodes to be bound to fixed values, forcing a particular direction of signal flow on bidirectional lines. It also lets the designer flag nodes be ignored and can hold constant the delay between two points. In addition, external models representing devices from the "outside world" can be attached to the circuit.

Design time well spent

The major steps in designing a chip with the new development system (namely, block and module compilation, functional simulation, and timing analysis) take only a few seconds or minutes, even for complex ICs. As a result, designers can spend most of their time exploring and improving the design of the chip's component structures, the blocks and modules, and their interaction. Since VLSI design is a structured, hierarchical problem, the user interface developed for the new VLSI development system conforms by making a trivial task of defining and frequently modifying hierarchical circuit definitions.

For example, movement within the hierarchy is done with a SELECT command that picks the objects—blocks, modules, and chips—

a designer wishes to work on. A SPECIFY command allows details to be added. The hierarchy can then be modified with the commands ATTACH and DETACH, and the results checked with VERIFY.

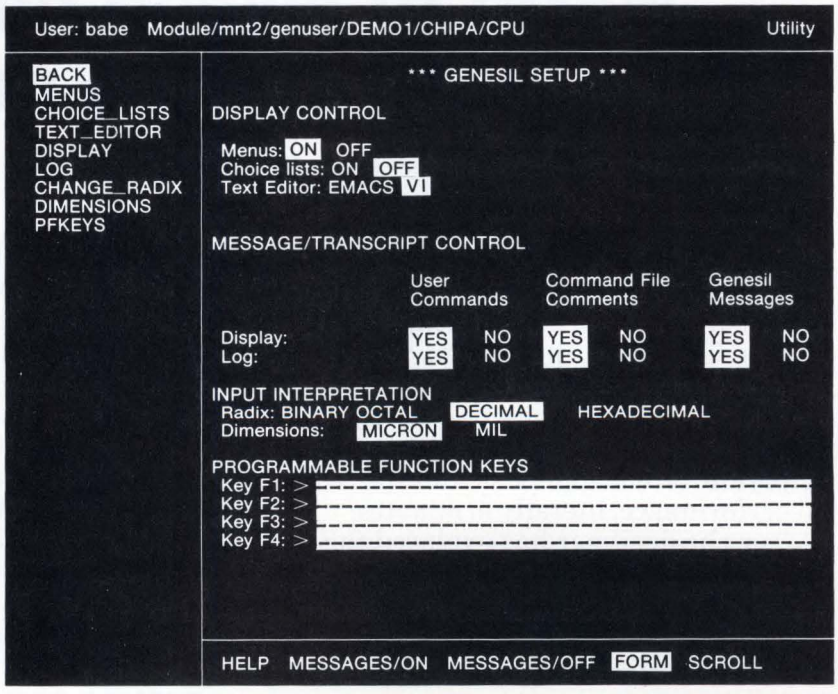
A menu presents these commands, to be selected either by mouse or keyboard. In the latter case, a command's abbreviation is accepted. Menus are hierarchical; in other words, one choice in a menu can bring up submenus, containing additional selections based on the original decision. Finally, the display is a partitioned window system, the partitions being permanently assigned to certain functions.

An appealing form

Input specifications, which include details for creating and modifying blocks, net lists, connectors, or even the user interface, are entered through displayed forms (Fig. 3). Forms consist of descriptive text, selectable and highlighted key words, and text-entry fields. Their use is easily learned—everyone has filled out a form of some kind—and they automatically document the designer's actions and intentions. Unlike programming languages, forms involve no complex syntax or particular entry sequence. Experience has shown that, with one exception, chips, modules, and blocks are specified at least three times faster with a well-constructed form than with schematic approaches to data entry.

The exception to this rule pops up when specifying the states of PLAs and ROMs. For these devices, the development system provides a PLA mnemonic language that includes I/O declarations, state assignments, cases, case vectors, and finite state-machine operators. Where necessary, the system accepts source-file specifications and net lists in the proprietary design language format.

To help smooth the design process still fur-



3. The specifications for blocks, modules, chips, and even the user interface are entered by means of displayed forms. Consisting of descriptive text, selectable keywords, numeric and text entry fields, forms are easy to learn, self-documenting, and eliminate the need to remember a complex syntax.

ther, a site manager can partition a job into password-controlled accounts, each of which is write-protected and can even be read-protected from the others. The development system also allows batch operation as well as interactive macro-command files. Extending Unix's powerful concept to chip design, the system's entire command structure is tied to a subset of the C language so the designer can create design macros that access such data as an object's size, power dissipation, and simulation states. When a user requests an operation like routing or simulation, the system checks to see if a block, module, or chip has been modified without having been recompiled. If that is the case, it recompiles that object from the bottom of the hierarchy up, before proceeding further with the operation.

The outcome

When finally a design is complete, the development system supplies the data optimized for a particular fabrication line, to its tape drive. In addition to the tape, the system produces a report on the data and manufacturing instructions. Finally, the test data used during the design's simulation is available for production test systems, as is various other information such as net lists, truth tables, and even a log of every design session's interactions.

Data path design shows worth of silicon compiler to VLSI system makers

System engineers now can build their own custom VLSI circuits with a turnkey silicon compiler, simulation, and analysis system. The most important virtue of the Genesil System (see p. 169) is not just that it lets designers turn their system ideas into silicon, but that it lets them first refine their ideas and compare different approaches for the best price and performance, literally in minutes.

After the designer has explored the possibilities and settled on a block diagram, the system verifies the behavior of the chosen architecture, establishes the floor plan, routes the connection between circuit blocks and modules, and creates a tape from which a particular foundry will make the actual silicon parts.

To illustrate, consider the exploratory phase of designing the data path section of a 9-bit-wide magnetic tape controller chip. Note that the whole chip's design would be divided into two sections—the control logic and the data path. In a typical approach to full chip design, the data path would be specified first, followed by descriptions of the control logic, using flow charts, state diagrams, and Boolean equations. The control section would most likely be implemented with a ROM or programmable logic array (PLA). When both sections were complete, the system could estimate the control section's area, power consumption, and speed even before the exact control equations were formulated.

The data-path section of the chip is similar to that of many bit-slice ICs. With the new

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Stan Mazor is Silicon Compilers' applications manager, providing technical support to customers and sales staff. Before joining the Los Gatos, Calif., company in May, he had 14 years at Intel, where he helped invent the microprocessor. Mazor shares patents on the MCS-4 and 8080 microprocessors, has lectured on microelectronics internationally, and published over 30 articles and technical papers. He is also a senior member of the IEEE.

system, its elements are particularly easy to enter and manipulate, since they can all be found as predefined blocks in the development system's library.

The starting point

Exploration for the best data-path architecture starts when the designer analyzes the required data flow and makes a first try at a block diagram (Fig. 1). Since this controller is for a 9-track magnetic tape drive, the registers in the data path need to be 9 bits wide. Moreover, previous experience tells the designer that five registers are needed to store characters for the header, control words, and check sums. A three-port RAM serves the function of these registers.

Next, the RAM's read ports must drive two data buses containing latches and multiplexers. The multiplexers, in turn, feed a multifunction ALU whose output ultimately feeds back around to the data-in port of the RAM. An advantage of this configuration is that it allows the input data to two registers to be simultaneously selected from two address buses, A and B. In addition, once the ALU operates on the data, it can be put back into the RAM where B was previously stored.

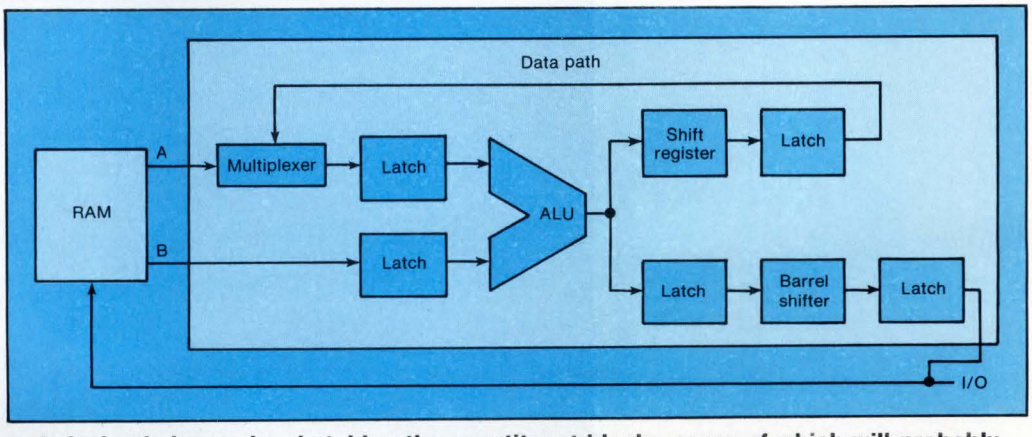
The designer must decide how to shift the output data, or more specifically, whether to use a barrel shifter or a shift register. A barrel shifter is fast, performing multiple bit-shifts in one clock time, but it occupies a relatively large amount of chip area. On the other hand, the simple shift register takes one clock pulse for each shift it makes, but consumes less area and so produces a more economical design.

Choosing from a menu

The registers, multiplexers, shifters, ALUs, and buses are picked from the development system's families of functions and refined in detail with the help of the displayed menus (Fig. 2). Each component's data path can be serial or of any desired bit width; the designer has full control of these details and can choose the options that maximize a design's efficiency.

With the displayed data-input form as a guide, the designer easily specifies the blocks for the data path module. As blocks are chosen, the form changes to offer only those subsequent options that are valid for a selection. This spares the designer from having to consider extraneous choices and focuses attention on the best options.

Under the heading "Fabline" (for fabrication



1. A design is begun by sketching the constituent blocks, many of which will probably be available from the development system's library and simply need fine-tuning to conform to the circuit's needs. Here, the data path of a 9-bit magnetic tape drive controller is taking shape.

line), the first section of the form accepts the choice of foundry for producing the chip. The compiler then generates the correct output files for that fabricator and optimizes the layout for the associated process. If the designer chooses a different foundry later, recompiling the design is the only step needed to create the files for the new choice.

Next, the designer enters the data-path width, in this case nine bits. This sets a default value for all registers and buses, but this figure can be overridden where a smaller width slice is desired.

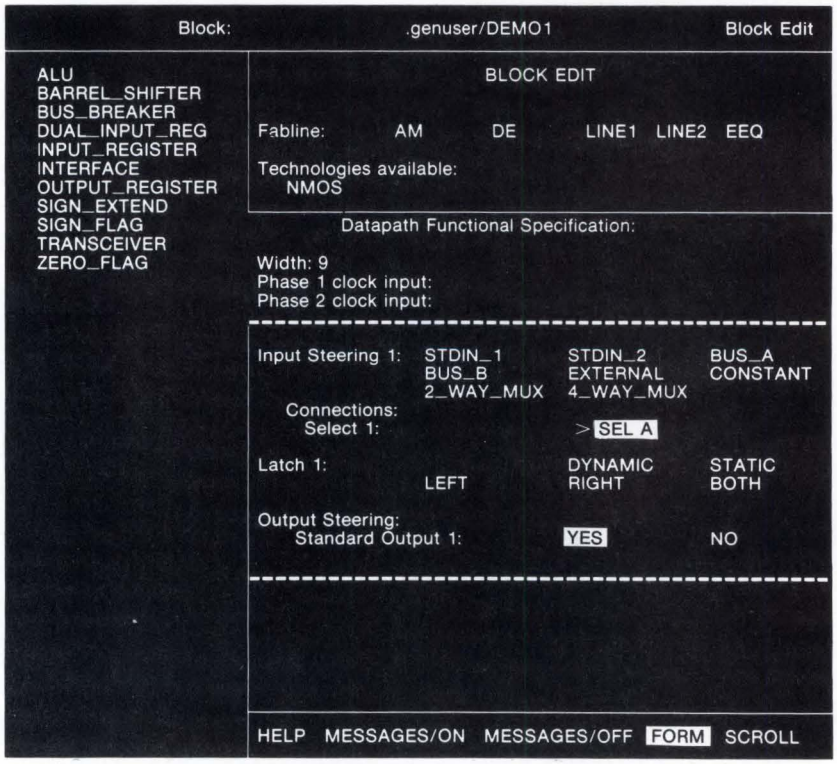
Steering toward the right design

The first element in the block diagram (after the RAM) is a two-way multiplexer. This block is picked from the nine choices listed under the heading Input Steering. The next element in the data path is a latch; here the form offers five choices: dynamic, static, shift right, shift left, or shift right and left. The remaining elements in the data path are similarly picked by making menu selections from presented options; the whole form-filling process takes about five minutes.

Once the block diagram is completed, control-signal names are keyed in or assigned automatically: The system chooses from a list of default names, such as "sel A," in the case of the two-way multiplexer.

For the sake of accuracy, the system checks its input specification form for syntactical and semantical errors. Errors in logic design are noted, as are simple entry mistakes such as dangling outputs or undefined inputs.

The system will go so far as to flag timing errors that arise from signals based on different



2. A displayed input form accepts the designer's specifications, starting with a particular fabrication line and technology (top). On the left are the components selected by the designer, who works down the form selecting the different options available for each one.

clocks—a common characteristic of MOS designs. In two-phase MOS logic it is important not to mix signals that are valid during opposite clock phases. The system remembers which clock is used in a register and identifies data-bus transfer times. When potential timing errors crop up, the system's compiler issues a warning message.

Another way to identify possible timing errors is to issue a VIEW command to request a compiler-generated block diagram of the design (Fig. 3). It shows the blocks and data-flow paths, color-coding them to identify the clock phase used by each.

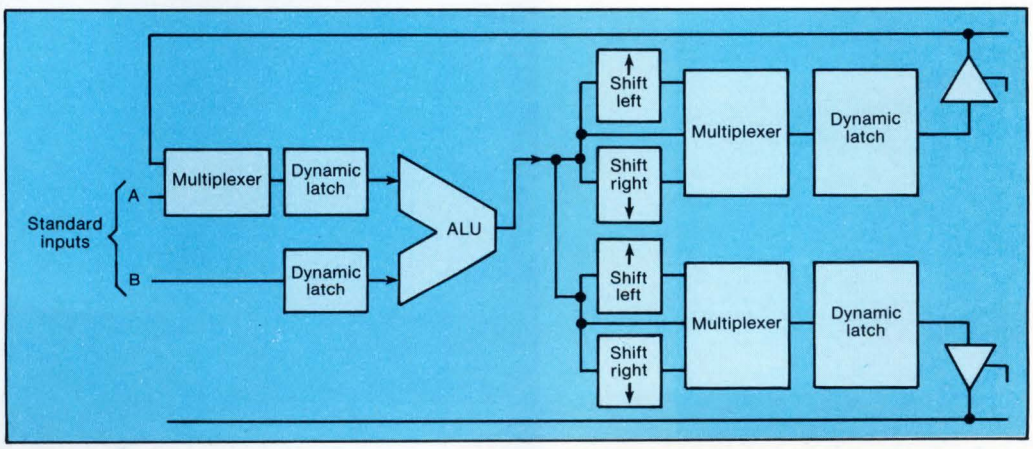
Making a test run

When the designer is satisfied with the block diagram, he or she can instruct the system to generate the layout and verification models for the specified process. In less than a minute, the system compiles a typical module and reports the portion of chip area used. If additional blocks and modules are added, the system figures in their sizes so the designer can monitor the chip's overall cost as the design proceeds.

At some point in the design of a complex chip, it becomes necessary to analyze the ac timing in order to calculate the circuit delays and maximum operating frequency. The system performs this evaluation, taking into account the particulars of the particular foundry and process selected.

By following all the logic paths and calculating the accumulated delays within a block or module, the system's timing analyzer will find the longest delay path. This path establishes the clock duty cycles, which in turn fixes the minimum clock period. When several blocks or modules are merged, the system combines these periods to give a chip-wide maximum operating frequency.

A block or module's setup and hold time can also be analyzed for all input and output signals in order to compare the performance of different architectures. For this, the system generates a table (Fig. 4). Moreover, a designer can find the rise and fall times along any path and compare it to one of those that set the operating frequency. Working in conjunction with this option, a Flag menu identifies any node whose



3. Once the components are selected and their details specified on the input form, the designer can request a system-generated block diagram of the compiled circuit. When a design uses two nonoverlapping two-phase clocks, the system color-codes the blocks to identify them with particular clock phases and therefore helps the designer avoid mixing the signals associated with each.

Cover: Silicon compiler

delay time is above an assigned threshold.

If a chip's performance does not meet the designer's expectations, there are two options: change the process or restructure the design. Since any timing analysis is based on a particular foundry process, the designer can explore the alternatives by selecting a faster process and recompiling, a matter of a few minutes.

Options for improvement

In the second option, the designer can modify the architecture to improve performance. The choices involved are typical ones, familiar to system designers, and avoid esoteric IC techniques like tweaking transistors. Some examples: using adders instead of counters, using two separate adders where one is used twice, or opting for barrel shifter instead of a simple shift register. Another technique is to replace large arrays with distributed elements, or to add bus buffers to reduce loading-related delays.

Simulation in parts

Once the delays are brought within tolerable limits, the designer can evaluate the circuit's behavior with the development system's built-in functional simulator. The simulator's screen handles a wide variety of data formats. In the design example, the upper portion of the screen shows the 9-bit inputs to the tape controller's ALU, while the lower portion shows some of that data as timing waveforms (Fig. 5).

Min time from rise of Ph 1 to fall of Ph 1: 25.7ns
Min time from rise of Ph 2 to fall of Ph 2: 82.8ns

Min time from rise of Ph 1 to rise of Ph 2: 50.3ns
Min time from rise of Ph 2 to rise of Ph 1: 86.9ns

Total Cycle Time 137.2ns

Setup and Hold Times (ns)

Signal Name	Phase 1 setup	Phase 1 hold	Phase 2 setup	Phase 2 hold
SE	2.1 (f)	−1.1 (f)	23.3 (f)	−4.4 (f)
INTER2_DRA1	6.1 (r)	---	2.2 (f)	−1.2 (f)
INTER2_DRB2	6.1 (r)	---	2.2 (f)	−1.2 (f)
INTER2_SE1	2.2 (f)	0 (f)	24.5 (f)	−1.1 (f)
INTER2_SE2	2.2 (f)	0 (f)	16.7 (f)	−3.1 (f)
INTER2_SL1	5.5 (f)	−1.3 (f)	28.7 (f)	−4.6 (f)
INTER2_SL2	5.5 (f)	−1.3 (f)	20.9 (f)	−6.6 (f)
INTER2_SLI1	0 (f)	0 (f)	13.4 (f)	−2.8 (f)
INTER2_SLI2	0 (f)	0 (f)	12.6 (f)	−2.7 (f)
INTER2_SRI1	0 (f)	0 (f)	20.1 (f)	−2.8 (f)
INTER2_SRI2	0 (f)	0 (f)	12.3 (f)	−2.7 (f)
ALU1_CIN	0 (f)	0 (f)	−0.6 (r)	7.3 (f)
ALU1_F[0]	0 (f)	0 (f)	17.0 (r)	---
ALU1_F[1]	0 (f)	0 (f)	15.1 (r)	---
ALU1_F[2]	0 (f)	0 (f)	16.9 (r)	---
ALU1_F[3]	0 (f)	0 (f)	15.0 (r)	---
ALU1_F[4]	0 (f)	0 (f)	18.1 (r)	5.6 (f)
ALU1_F[5]	0 (f)	0 (f)	18.1 (r)	5.6 (f)
ALU1_F[6]	0 (f)	0 (f)	15.0 (f)	---

Output Timing

Signal Name	Phase 1 rise	Phase 1 fall	Phase 2 rise	Phase 2 fall
INTER2_SLO1	---	---	68.5 ns	75.4 ns
INTER2_SLO2	---	---	73.8 ns	81.2 ns
INTER2_SRO1	---	---	33.7 ns	40.7 ns
INTER2_SRO2	---	---	60.2 ns	67.6 ns
ALU1_COUT	---	---	68.9 ns	61.9 ns
ALU1_OVF	---	---	---	---

BUF: XXYY FILE: XXYY Normal Bottom

4. The system's timing analyzer creates a report of the setup and hold times for all of the input and output signals for the circuit's two clock phases.

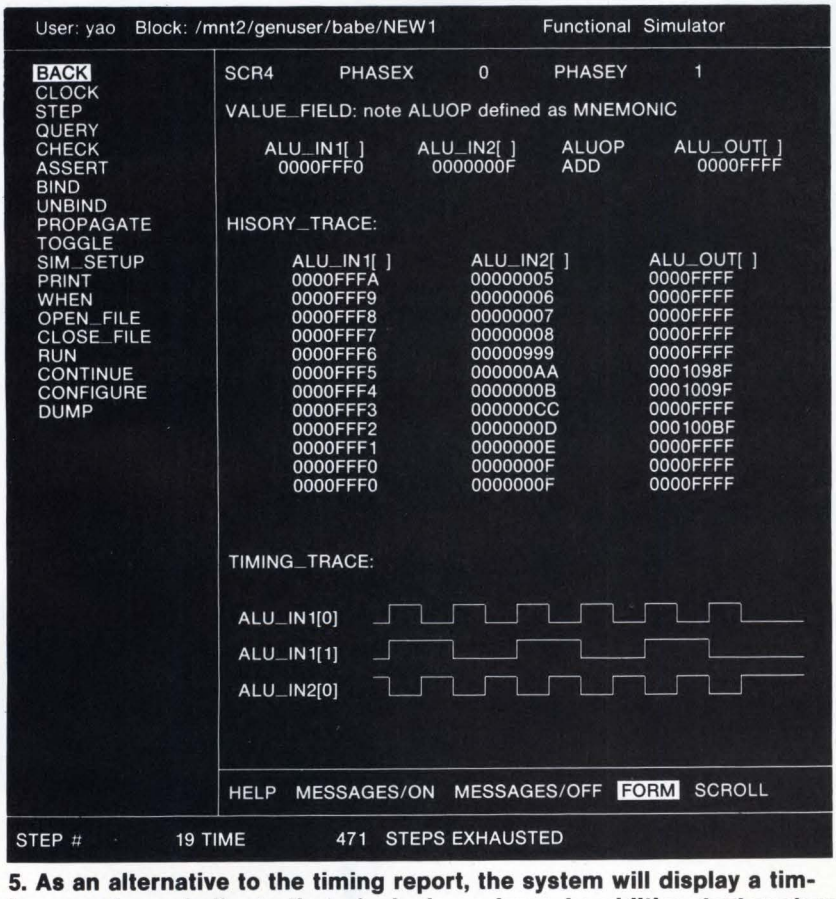
In addition, test vectors can be input directly from the system's terminal or from a batch file. The circuit's response to each vector can be stored, in turn, for eventual comparison to the actual ICs.

Final touches

In this example, because the data path module consists of pre-designed blocks, the circuit requires little simulation to check its function. Once the designer has conducted a preliminary circuit test, he or she would begin designing the chip's control logic. That done, the full circuit could be simulated again to test the combined functioning of data path and control logic.

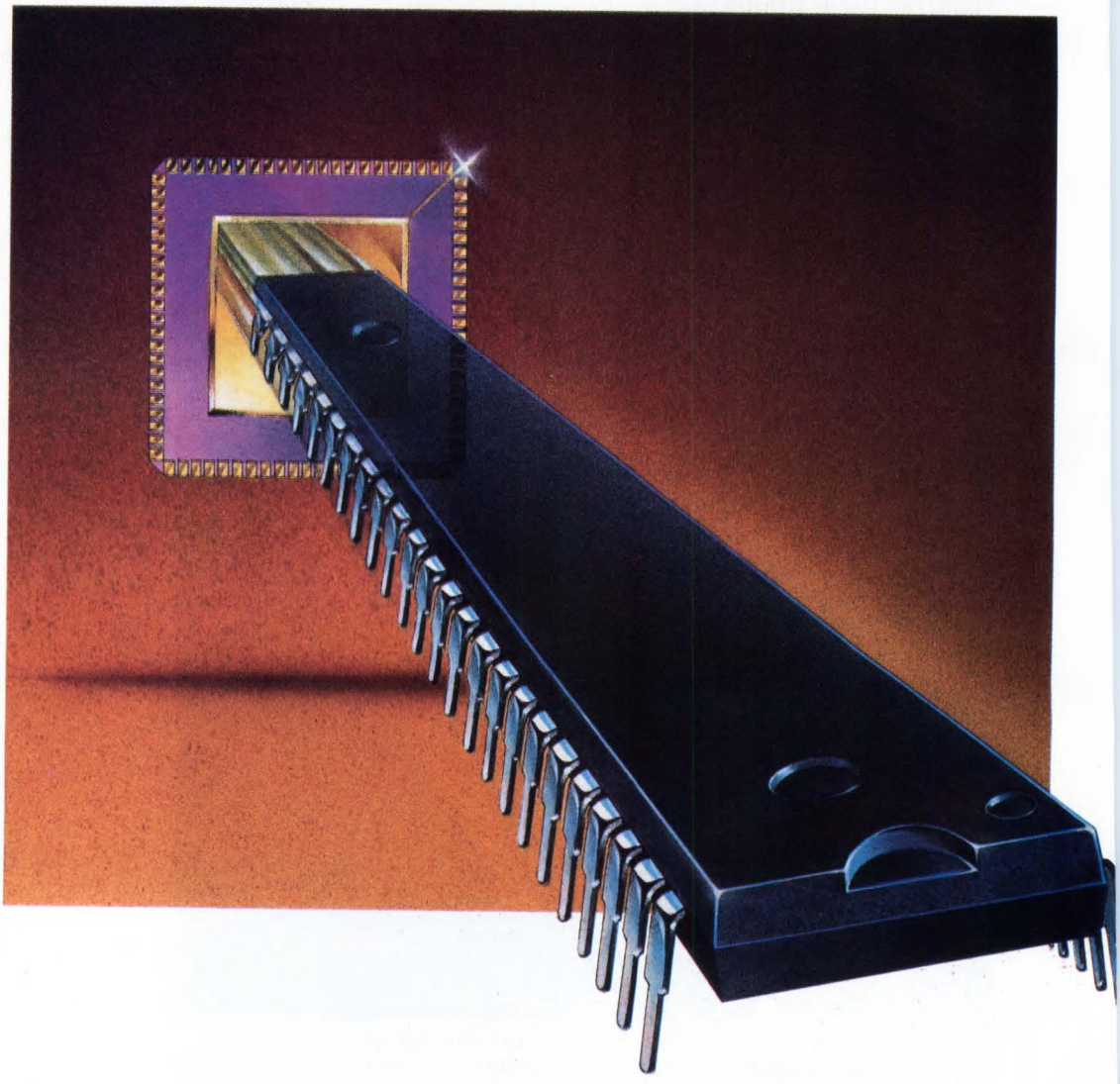
After the compiler generates a layout of the controller, the designer can get a multicolored hard copy to inspect the results. Eventually, however, as the designer becomes more confident of the system's ability to generate silicon artwork automatically, the need for plotted layouts will diminish.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543



5. As an alternative to the timing report, the system will display a timing waveform similar to that of a logic analyzer. In addition, test vectors can be entered at the keyboard or in a batch mode, and the simulated circuit's output can be collected for eventual correlation with the behavior of the actual silicon part.

DOUBL



E DUTY

Introducing the MK68200 16-bit microcomputer/microprocessor.

Unlike any other 8- or 16-bit single-chip microcomputer, the new Mostek MK68200 performs equally well as a single-chip microcontroller and as a peripheral I/O controller. In the latter type of application, the MK68200 can provide local intelligence required to handle typical computer system I/O functions. Without tying up the host processor. In addition, it can transfer data to and from system memory using a software DMA function. So, as an example, it's ideal as a front-end processor for handling complex serial I/O protocols.

Actually, the 16-bit MK68200 gives you a whole new dimension of system control. One that enables you to monitor, measure, regulate, sense, and interconnect with more precision than ever before.

The operative word is more. More speed. More powerful instructions. More I/O functions. More efficiency. More versatility. All of which mean more application opportunities. For robotics. Engine control. Pattern recognition. And real-time measurements and control – as a stand-alone device, or in tandem with other microprocessors as an intelligent peripheral controller.

First, consider speed. Using the 6 MHz instruction clock rate, the MK68200 can execute a 16-bit multiply as fast as a 3.5μs; a 32 x 16 divide in 3.8μs; and a 16-bit add/subtract in as little as 500ns. In other words, it's faster than any other general-purpose, single-chip micro currently available.

One reason for this faster speed is code efficiency; most MK68200 instructions are just one word. That not only saves code space, it also improves execution speed. And the powerful instruction set incorporates more than 50 instruction types which operate on both byte and word operands.

Next, look at the available versions. The MK68200 comes in a 48-pin DIP with 0 or 4K bytes of ROM and 256 bytes of RAM. It is expandable to address a full 64K byte address space externally. And finally, an 84-pin LCC version (with no ROM), is available for system development or for multiple bus applications.

For single-chip applications, up to 40 pins of the 48 pins are available for I/O to include two 16-bit parallel ports. Plus a full-duplex USART with double-buffered transmit and receive capable of operating at data rates up to 1.5Mbps (using a 6MHz instruction clock).

The MK68200 offers extensive interrupt capabilities. One non-maskable interrupt input is provided as well as 14 maskable interrupt sources. In addition, all 14 independently vectored interrupts are user-assignable in software for any priority scheme. And to enhance serial communications, there's also an innovative wake-up interrupt on the serial channel.

As for support, there's a powerful Macro Cross Assembler, along with a host of other software tools. As well as RADIUS™, a very cost-efficient remote development station. And to expand the MK68200 family, plans include higher performance versions with denser memory and faster throughput. Plus power-conserving CMOS.

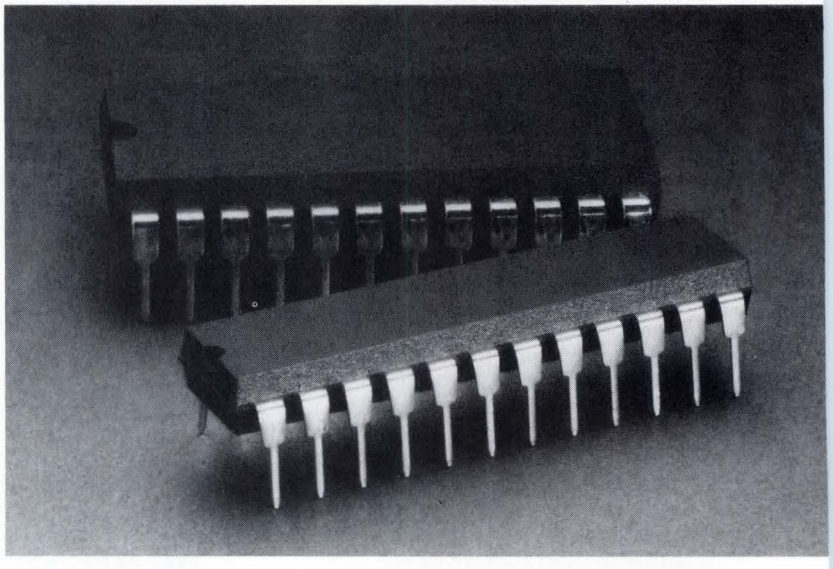
Look beyond the limits of conventional single-chip systems into the realm of ultimate control. It's yours with the MK68200. For more information, contact Mostek, 1215 W. Crosby Road, MS2205, Carrollton, TX 75006, (214) 466-6000. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5-681157-9.

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CIRCLE 63

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CIRCLE 64

Advanced clock controller cuts power needs, size of static CMOS systems

With a one-chip controller-generator running a static CMOS system in any of three minimal-frequency modes, power consumption will drop to a trickle.

The faster a CMOS system runs, the more power it consumes. Consequently a natural way to reduce power consumption is to run the system at a minimal frequency or even stop it whenever full speed is unnecessary. That possibility is open only to static CMOS circuits—those capable of running at anything from dc to their maximum frequency—and not to dynamic ones, which lose data below a certain clock frequency.

The 82C85 clock-signal generator and controller chip ensures that a static CMOS system will dissipate the least power possible (see "Lowering Power Consumption in CMOS Systems," p. 186). The chip can run the system in four modes, which are, in the order of most to least power savings:

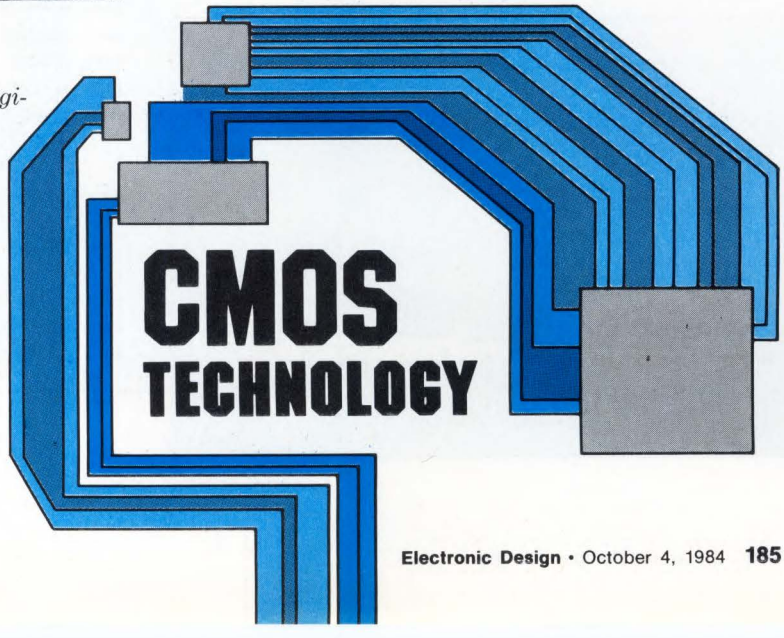
- The stop-oscillator mode, in which both the control chip's oscillator and the system CPU's clock stop.
- The stop-clock mode, in which only the CPU clock stops (to make it faster to restart the system).
- The slow mode, at much less than the system's maximum frequency. Here, power dissipation approaches standby leakage current levels, yet the CPU can still tackle such functions as periodically polling external sources and collecting data from them or sensing low battery conditions.
- The fast mode, at the system's maximum frequency.

The Static Clock Controller-Generator, as the 82C85 is formally called, has separate

Curtis A. Mroz and **Walt Niewierski**
Harris Corp.

Curtis Mroz works as head applications engineer for the microprocessor applications group of Harris's Semiconductor Digital Products Division, Melbourne, Fla. Previously, he was a design engineer at Honeywell and OAK Industries. He has a BSEE from Purdue University.

Walt Niewierski, who holds a BSEE from the University of Michigan, is technical marketing engineer for the Harris division. Before joining the company, he designed microprocessor-based test equipment at Ford Motors.



signals for stopping and starting its oscillator or for blocking and unblocking an external frequency input. It can produce any clock frequency up to its maximum of 8 MHz, plus 1/256 of that frequency for its slow mode. Besides a crystal-controlled oscillator and clock generation logic, the chip contains ready synchronization and reset logic, as well as halt and decode restart logic. It comes in a slim-line DIP with 24 pins on 0.3-in. centers.

To guarantee crystal-controlled operation at 24 MHz, the chip uses a parallel, fundamental-mode crystal and two small-load capacitors. It generates both system and peripheral clock signals and for increased system flexibility, produces edge-synchronized 33% (CLK) and 50% (CLK_{50}) duty-cycle clock signals. Both of the latter are available simultaneously. Moreover the device can synchronize its clocks with 82C84A clock generator-driver ICs and with other 82C85s for use in multiprocessor systems. All of its inputs except three (X_1, X_2, and RES) are TTL-compatible over three temperature ranges—commercial, industrial and military—and the outputs are both CMOS- and TTL-compatible.

For ease of use with the 80C86/88 CMOS microprocessor family, the new chip is manu-

Lowering power consumption in CMOS systems

Only when static CMOS components are designed into a system can power consumption and package size be truly minimized. Consequently, as CMOS chips take over in architectures formerly built with NMOS devices, the distinction between static and dynamic circuitry takes on new importance.

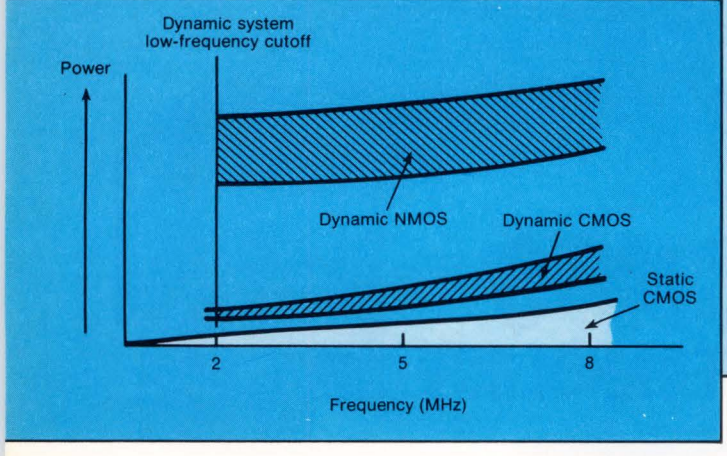
Dynamic CMOS systems usually dissipate more power than static systems, in both the operating and the standby mode (see the figure). Even when their power dissipation seems the same for such operating conditions as maximum frequency and worst-case voltage, other factors tilt the balance in favor of the static device. A static circuit can run on any frequency from dc to its maximum. In contrast, if the clock frequency of a dynamic circuit falls below a specified minimum, data in the CPU or a peripheral is lost or altered. Therefore true standby operation (with the clock stopped) can occur only with a static CMOS design.

A static microprocessor system, like one based on the 80C86 or 80C88 CMOS devices, can be put in a standby mode by simply stopping the clock signals. The 80C86/80C88 family, for example, has an operating frequency range of dc to 5/8 MHz and retains data even if the external clock is stopped indefinitely. The system restarts when the CPU clock signal resumes.

But a static system design calls for several prerequisites. First, it requires static CMOS microprocessors and support circuits, which can operate and maintain data from standby (dc) to the maximum frequency of operation. Another need is for care in defining power-down situations, in which the processor and system clock frequencies can be controlled. Standby and operating modes should not be considered separate entities. Opportunities to stop the system clock must be evaluated carefully, as should transitions from the operating mode to standby and back again. Standby, low-frequency, and high-frequency operations then become complementary states, and the result is lower system power dissipation.

By anticipating circumstances in which the system can be stopped or run more slowly, the engineer can ensure that the proper standby and low-frequency hardware and software get into the initial system design and are not treated merely as afterthoughts. This increases efficiency and lowers the cost of implementing a static design. The degree to which the system's operating characteristics are altered is based on power, performance, and response requirements.

Because a static design results in lower power consumption, the system needs fewer supportive elements. For instance, fans and heat sinks can be eliminated, power-supply requirements reduced, and smaller enclosures used.

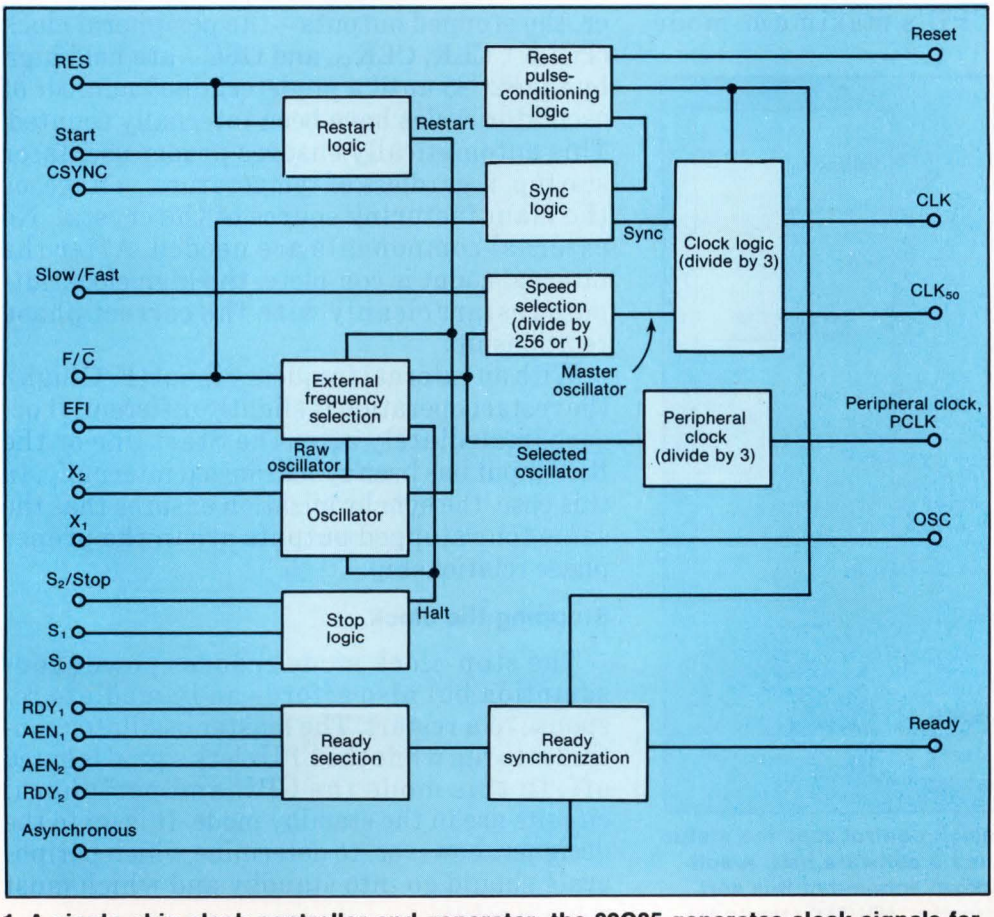


factured with the same CMOS process—a self-aligned junction-isolated process called scaled SAJI IV. However, it can be used with any static microprocessor or peripheral device. Its pinout is a superset of that of the 82C84A: pins 1 through 9 and 16 through 24 are compatible with pins 1 through 9 and 10 through 18, respectively. To emulate the 82C84A, pins 11 through 15 are tied high.

If power consumption must be held as low as possible and response times of 1 to 3 ms are acceptable, the device should be operated in the stop-oscillator mode. In this case, the chip gates off the system clock and then stops the crystal oscillator circuit. The External Frequency Input line (EFI) can be used instead of the oscillator by driving the Frequency-Control line ($F/\overline{C}$) line high.

With a 15-MHz crystal, which is needed for the operating frequency of a 5-MHz 80C86/88 system, the total operating current for the oscillator circuit ranges from 15 to 30 mA. Without those 15-MHz transitions in the oscillator circuit, the typical standby current falls to less than 50 μA (100 μA, worst case). A typical 80C86/80C88 system draws from 1 to 2 mA in standby.

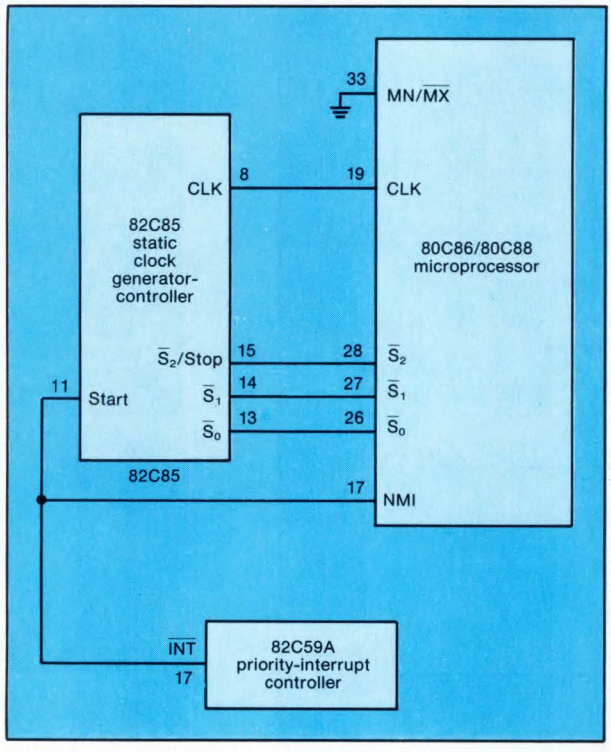
Stopping the controller-generator is a simple



1. A single-chip clock controller and generator, the 82C85 generates clock signals for a microprocessor and its peripherals. Designed for static CMOS systems, the device controls system frequency to reduce power consumption.

matter. Its three status lines—S_2/Stop, S_1, and S_0—are sampled on the rising edge of the CLK signal (Fig. 1). When these three lines enter the logic 011 state after a 111 state and when the Start line is also low, either the chip's oscillator will be stopped synchronously or its external frequency source will be turned off synchronously. In other words, the CLK and CLK_{50} outputs each stop in a logic 1 state after two additional complete cycles of the clock signal. The operation can occur in either the slow or the fast mode.

The 011 condition after a 111 on the three status pins indicates a software halt in the 80C86/80C88. This condition can be used in conjunction with the CPU's maximum-mode status lines—S_2, S_1, and S_0—to activate a software-controlled power-down that requires no external circuitry (Fig. 2).



2. A simple method for clock control uses the status lines of the 82C85 to detect a software halt. A software-controlled, power-down scheme of this sort requires no additional circuitry. MN/MX stands for Maximum mode.

If a power-down hinges on conditions other than a software halt, the device's S_2/Stop input can be used as a stand-alone command to stop the crystal operation. To do this, the S_0 and S_1 pins are connected to V_{CC}, and the S_2/Stop line is controlled through external logic.

Once the oscillator stops or is committed to stop, its restart sequence begins on either a high level on the Start input or a low level on the Reset input ($\overline{RES}$). A high level applied to the Start input disables the Stop input and overrides a Stop command in all instances. However, the stopped outputs—the peripheral clock (PCLK), CLK, CLK_{50}, and OSC—are held high by the 82C85 until a predetermined number of oscillator cycles have been internally counted. This automatically ensures proper oscillator startup, regardless of temperature, voltage, or the manufacturing source of the crystal. No external components are needed. After the internal count is complete, the high clock outputs restart cleanly with the correct phase relationship.

With an external frequency input (F/C high), the restart operation is slightly different. It occurs immediately after the Start line or the $\overline{RES}$ input has been synchronized internally. In this case, the synchronization ensures that the same four stopped outputs are in the proper phase relationship.

Stopping the clock

The stop-clock mode reduces power consumption but also affords an immediate response to a restart. The master oscillator continues to run while the CPU clock signal is gated off. In this mode the CPU and peripheral circuits are in the standby mode. It is up to the designer, however, to determine which peripherals should go into standby and which must remain active.

The stop-clock mode can be achieved with the 82C85. Here the OSC output connects to the EFI input, and the device is operated in the EFI mode, with F/$\overline{C}$ high. In other words, the chip's own crystal oscillator serves as the "external" frequency source. The S_2/Stop input gates the clock signal in the EFI mode, allowing the oscil-

lator to continue to run. When Start is enabled, system restart begins immediately with the resumption of the CLK output. The clock can also be restarted by a reset or external interrupt.

The mode's primary advantage is that the system clock can be restarted within microseconds after it is enabled, thereby permitting an immediate response to interrupts or other signals that indicate a change in system activity. The clock signal is always active, and there is no waiting for oscillator stabilization.

Of course, the penalty for such instant response is higher power dissipation (Fig. 3). This dissipation comes from current drawn by the crystal oscillator circuit. Clock generator ICs like the 82C84A and 82C85 typically consume 1 to 2 mA/MHz when the crystal is in operation. With a 15-MHz crystal, the total operating current for the oscillator circuit ranges from 15 to 30 mA.

Slow clock cuts power

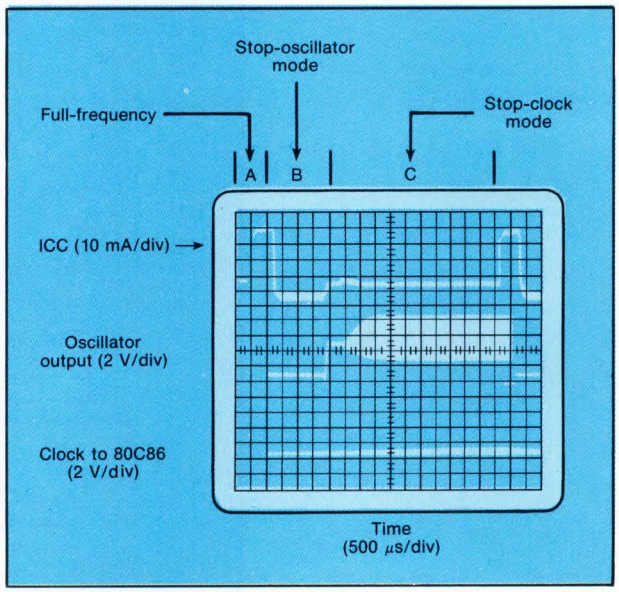
When continuous operation is critical but power consumption remains a concern, the controller-generator can put the system into the slow, low-frequency mode, which retards most operations and thus reduces the total power required. Data continues to flow properly, and the system responds to interrupt requests much faster than it would in the stop-oscillator mode.

The low-frequency divide-by-256 mode offers continual operation and performance of critical functions with a drastic reduction in power. The main oscillator continues to run, but the clock signal is divided by 256. The Slow and Fast input (SLO/FST) controls the frequency of the CLK and CLK_{50} outputs. When the line is high, the two outputs run at full speed—at one-third the crystal or external frequency. When the line is low, the frequencies of the two outputs are divided by 256. The PCLK output, however, remains at a constant frequency of one-sixth the oscillator or external frequency.

To be recognized by the controller-generator, SLO/FST must stay low for at least 195 oscillator or external frequency pulses—13 μs at a 15-MHz oscillator frequency. Otherwise glitches or noise spikes could cause undesirable frequency changes. To eliminate glitches on CLK and CLK_{50}, SLO/FST is synchronized to the high or low transitions of PCLK. To guarantee transition to full frequency, SLO/FST must be held high for at least three oscillator or external frequency pulses.

In the low-frequency mode, a 15-MHz system can be returned to full speed in 1 microsecond—a half PCLK cycle of 800ns plus 200 ns for three OSC or EFI cycles. The total delay in returning to full frequency operation is 50.2 μs. These times depend on the system's operating frequency, and they vary with the main oscillator frequency.

At a 5-MHz system clock—15-MHz crystal—the final CPU clock frequency in the slow mode is approximately 20 kHz. At that reduced speed,



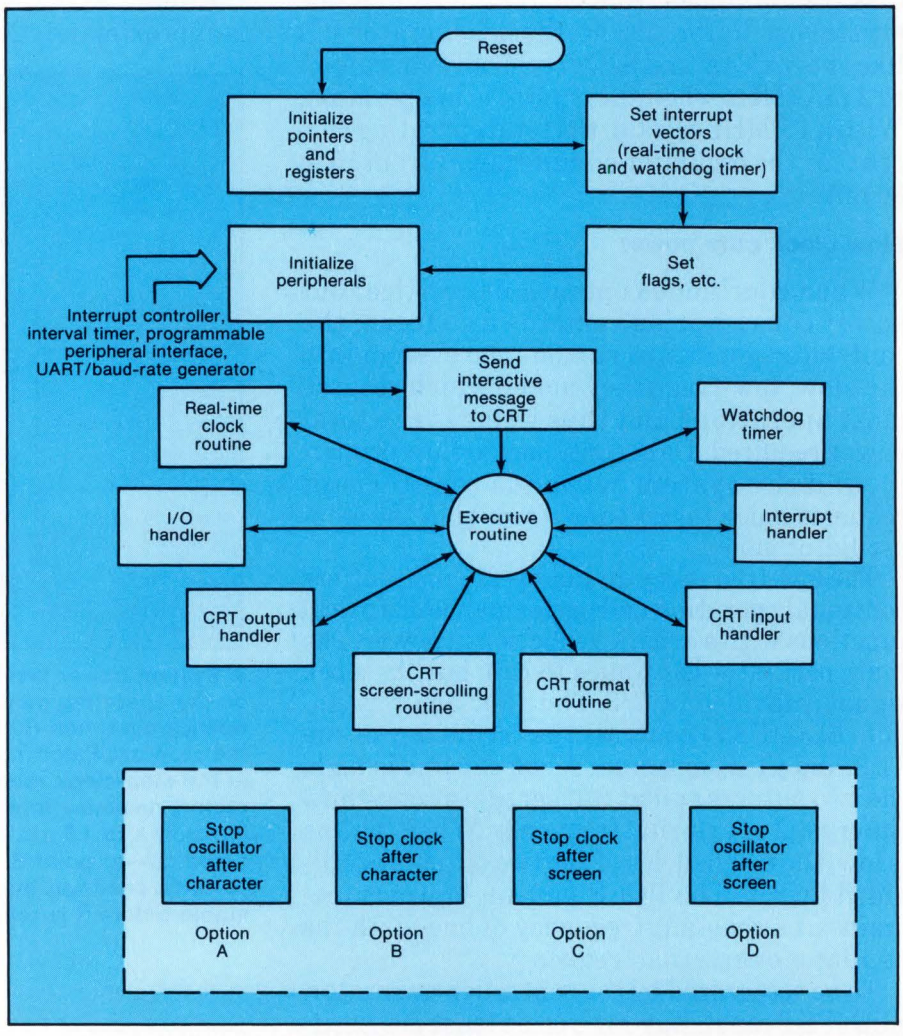
3. System power levels vary significantly, depending on the operating mode of the clock. From full frequency operation (point A), dissipation is lowest in the stop-oscillator mode (point B) and next lowest in the stop-clock mode (point C). Note the differing restart response times. The crystal start-up time is typically 1 to 1.5 ms, and the CPU clock signal is gated on—at point B—after the crystal oscillator restarts, ensuring that the oscillator frequency is stable before it is reapplied to the CPU.

the power dissipation of the CPU and peripheral circuits is very close to that drawn under standby current conditions and results in nearly the same power reduction as in the stop-clock operation.

Since the frequency of PCLK is not reduced when the 82C85 is in the slow mode, a real-time clock can be implemented with an 82C54 programmable interval timer driven by PCLK. Chip count falls, because no need exists for a stand-alone real-time clock circuit. Further, no additional crystal oscillator is needed for a UART, since it can run from PCLK.

CPU dissipation is reduced in the low-frequency mode. The operating power for 80C86/80C88 microprocessors, for example, is 10 mA/MHz of clock frequency. At 20 kHz, the average operating current of these microprocessors drops to 200 μA. Adding 500 μA of standby current brings the total current to 700 μA—a sharp contrast with 50 mA at a 5-MHz operating frequency. However, the controller-generator will still run with a high-frequency crystal that consumes between 15 and 30 mA.

Low-frequency operation is a compromise between the stop-oscillator mode and full-speed operation. It requires a minimum of



4. In a CRT control flowchart, the executive routine can select either the stop-clock or the stop-oscillator mode, depending on the system's power and response requirements. If power consumption is the primary consideration, using the stop-oscillator mode to halt the CPU proves the best choice.

hardware and offers a reasonable tradeoff between power requirements and speed of response.

Power-down through software

In an interrupt-driven system—for example, one for updating information on a CRT—the software executive idles most of the time while waiting for an interrupt from an external source. When it recognizes the interrupt, it allows the task to be completed and then returns to the idle state to await the next sequence. With the controller-generator and the proper software, power in such a system can be regulated. In addition the user gets software and hardware options not previously available.

The system and CPU can be stopped periodically at intervals based on the data transmission rate (Fig. 4). While data travels to the screen over a serial channel, the system can drop into a power-down state until more data can be loaded from the CPU. The major concerns are how often to stop the operation and the impact on power and performance.

Two options significantly affect power and performance: stopping the system after each character is transmitted or stopping the system after each screen refresh. If power consumption is paramount, the choice is to stop the processor on the main loop of the executive routine. This allows the CPU to enter the stop-oscillator mode after a character is sent to the CRT. An interrupt—one indicating that the transmitter buffer register in the UART is empty—takes the system out of the stop mode and restarts the oscillator. After the crystal oscillator stabilizes and the clock is restored to the CPU, the interrupt is serviced.

How the clock oscillator start-up time affects display performance

Baud rate (baud)	Data transmission time (ms)	Oscillator start-up time (ms)	Nominal impact on transmission time per character (ms)
19,200	0.52	3	−2.48
9600	1.04	3	−1.96
4800	2.08	3	−0.92
2400	4.17	3	+1.17 (no speed impact)
1200	8.33	3	+5.33 (no speed impact)

Such a system requires a separate crystal oscillator for the UART and for a hardware real-time clock if periodic scrolling is required. That approach consumes less power than stopping the system after each screen refresh. With the main system oscillator stopped, the only power dissipation is in the UART's crystal circuit—typically 1 to 2 mA.

Nevertheless low power comes at the expense of response time. Since the crystal oscillator must be stabilized before the CPU can restart, data cannot be transmitted between the time the interrupt for more data occurs and the oscillator becomes stable. The start-up time for crystal circuits can be from 1 to 2 ms or longer, but each application should be evaluated individually.

The oscillator start-up time affects the data transmission time. A fixed start-up time of 3 ms is assumed for various baud rates. As the baud rate increases, the start-up time slows the effective transmission rate (see the table). For standard rates above 2400 baud, data transmission is completed well before new data is loaded, resulting in varying degrees of so-called system dead time.

The second option—stopping the oscillator after each screen refreshing—has no effect on the system's response time. With the oscillator and system clock running constantly while the screen is being updated, the CPU can respond immediately to requests for more data. This method, however, dissipates more power because the oscillator runs longer.

If scrolling is called for, a much higher current is needed, since the oscillator must continue to deliver a clock signal to the real-time clock or other circuit used for watchdog timing functions.□

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546

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Charge-nulled CMOS switch lets op amps tackle precision analog tasks

A dual DPDT switch aimed at switched-capacitor designs ushers in a new age of instrumentation amplifiers, analog multipliers and v-f converters.

Converting differential signals into single-ended form is an essential ingredient of analog signal processing. However, accurately extracting those single-ended signals in the presence of a large common-mode potential proves a tough job. Though several types of amplifiers have been assigned the job, they serve as stopgap measures.

On the one hand, instrumentation amplifiers can afford the necessary degree of precision, but are relatively expensive. Isolation amplifiers, on the other hand, can allow desired signals to be extracted in the presence of large common-mode voltages; however, their relatively large gain drift and inherent nonlinearity limit their ultimate precision.

A CMOS chip housing two double-pole, double-throw (DPDT) switches, designated the LTC1043, virtually eradicates those difficulties. When accompanied by two standard small-signal capacitors, each of its two sections (Fig. 1) turns a high-performance op amp into an instrumentation amplifier that rivals or beats the performance of today's chips or hybrids.

The value of the switch does not stop at instrumentation amplifiers. Instead it extends to high-accuracy analog designs like multiplier-dividers, voltage-to-frequency and frequency-to-voltage converters, and voltage inverters.

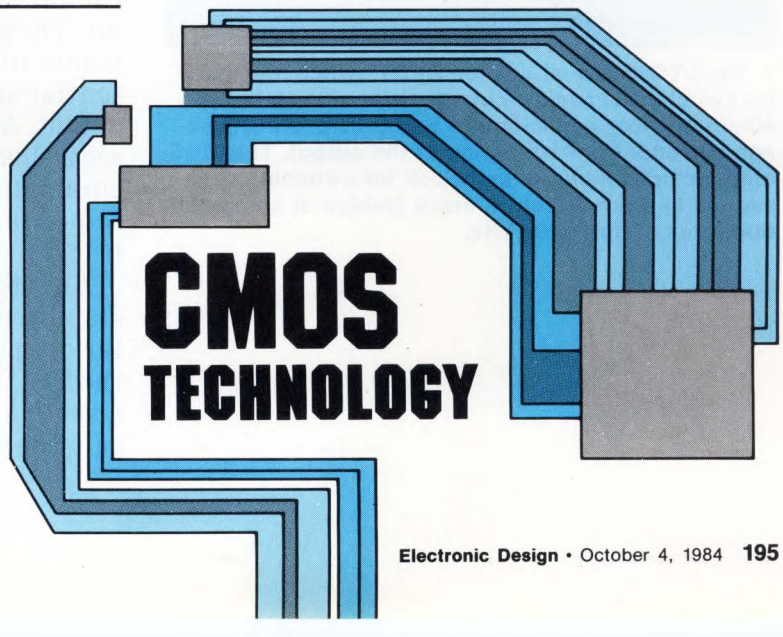
Reining in the charge

The switch's appeal lies in its ability to prevent leakage currents from appearing at the output, thereby minimizing sampling errors (see "Compensating for the Errors," p. 197). It

Nello Sevastopoulos and **Jim Williams**
Linear Technology Corp.

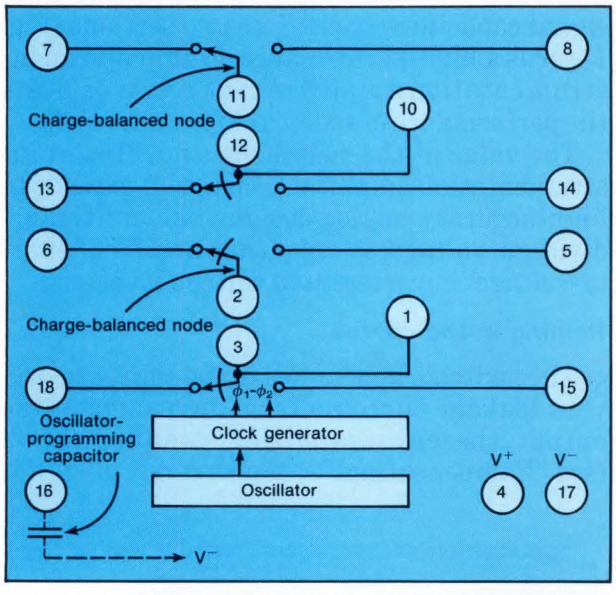
Nello Sevastopoulous runs the analog MOS design group at Linear Technology Corp. Previously he was head of the MOS IC design section at National Semiconductor. He holds an MSEE degree from Santa Clara University.

Jim Williams is a staff scientist at Linear Technology, specializing in analog circuit design. Before that, he was the applications manager for linear ICs at National and a consulting engineer for the Massachusetts Institute of Technology.



essentially serves as the front end for a switched-capacitor instrumentation amplifier. Although its on-resistance is not notably superior to that of existing CMOS switches, its charge-balancing circuitry dampens the effects of stray capacitance. Thus the device meets its primary objective: transferring charge with precision.

Based on a flying-capacitor technique, the DPDT switch helps create an economical circuit for converting differential into single-ended signals. In that type of configuration, a sampling capacitor, C_S, alternately switches between the output of a balanced bridge that represents the signal source and a holding capacitor, C_H. (Alternate arms of the bridge are connected to the positive rail and ground.) After a number of commutation cycles, the voltage across C_H equals that across C_S. Any common-mode component is removed.



1. The LTC1043 dual-section DPDT switch, designed for switched-capacitor circuits, is compensated to eliminate stray capacitances and thus prevent leakage currents from appearing at the output. The MOS chip includes a two-phase clock for switching each section in a break-before-make fashion at commutation rates of up to 200 kHz.

Controlling the break-before-make action of each switch is an internal oscillator, which drives a two-phase nonoverlapping clock generator working at a free-running frequency of 200 kHz. The rate can be adjusted from several hertz to 200 kHz with an internal capacitor. The oscillator also can be disabled and the switch driven by an external clock, if desired.

Meeting the specs

To demonstrate its prowess with analog tasks, consider the LTC1043's role in building an instrumentation amplifier for a transducer-fed system (Fig. 2). The simple configuration matches the best hybrid or monolithic amplifier in its low offset, low gain drift, high common-mode rejection ratio, and high linearity. Key performance specifications vary with the output instrumentation amplifier chosen (see the table, p. 198).

The stage gain is set by resistors R_1 and R_2. Capacitor C_F determines the roll-off (frequency) response of the amplifier, the control of which conventional instrumentation amplifiers cannot achieve with external components. The highest precision is obtained through a low oscillator frequency, typically 300 to 1000 Hz. That rate minimizes the number of switch transitions, reducing the effects of charge-injection residues. Typically, the charge transfer accuracy will be within a few parts per million. The maximum linearity error is about 2000 ppm at a sampling frequency of 200 kHz.

Note that the switch chip behaves like a switched capacitor low-pass filter, with the commutation frequency controlling the roll-off. The stage thus filters the acquired signal before it is amplified, thereby preventing potential nonlinearities from appearing at the output. Additionally, ac common-mode signals see a short circuit at the input and will thus be eliminated from the output if the input source impedances are balanced (as in a transducer bridge).

An expansion of that idea employs a chopper-stabilized amplifier (the LTC1052) that has better dc specifications than current units. Half the DPDT switch is set up with a diode to create a small negative voltage drop (Fig. 3). As a result, the amplifier is biased in class A, allowing

Compensating for the errors

A proprietary silicon-gate process deserves much of the credit for the dual DPDT switch's ability to manipulate charges without introducing significant errors. The process, which makes the gate structure retain its symmetry with respect to source and drain, ensures that the overlap capacitance between the gate and the drain and between the gate and the source of identical p- and n-channel transistors forming a CMOS switch is virtually identical. As a result, hold-step errors become dependent only on the amount of charge injected into the channel. Also, errors are virtually canceled when the sample differential voltage is nearly zero (see B). Such a technique gives the chip a common-mode rejection ratio that approaches infinity at low frequencies and has nearly ideal gain linearity. Additionally, it requires no external precision capacitors.

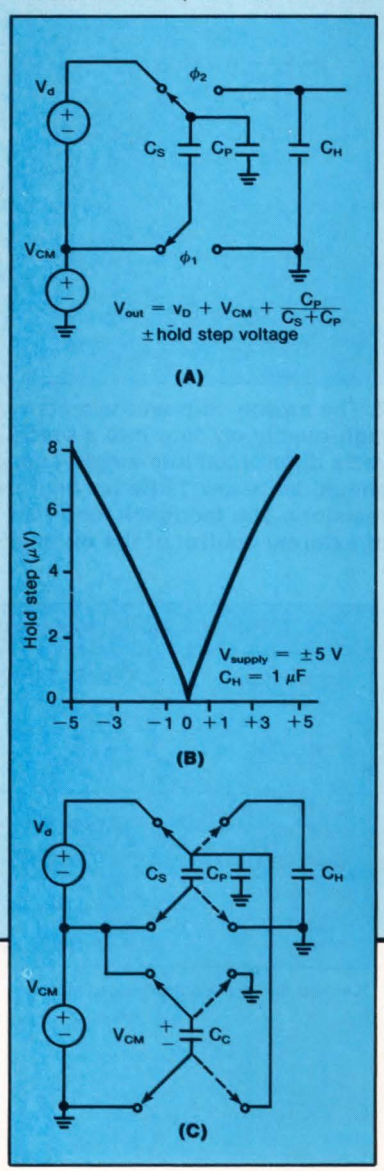
It is virtually impossible to build a high-accuracy flying-capacitor circuit with conventional switches, which are prone to two basic sources of error. First, consider the error associated with measuring differential voltages. During the sampling mode (see A), the charge placed on sampling capacitor C_S is equal to $C_S V_d$. The switch's parasitic capacitance, C_P, however, charges to the sum of the common-mode voltage (V_{CM}) and the differential voltage (v_D). (Note that one end of C_P is virtually grounded.) The excess charge placed on C_P is thus equal to $C_P V_{CM}$ and is shared equally by C_P and C_S during charge-transfer phase. Initially, then, the voltage placed on hold capacitor C_H is:

$$V_D + V_{CM}[C_P/(C_S + C_P)] \pm \text{hold-step voltage}$$

A second error voltage is added when the switches toggle (off-state to on-state) to again sample the differential voltage. During that interval, an additional error occurs that is similar to the hold-step error observed in sample-and-hold circuits. In conventional CMOS switches, this error is due mainly to the mismatch of the gate-to-drain/source overlap capacitance. Additionally, the channel charge injected into the drain/source during a switch's turn-off contributes to the hold-step error.

Parasitic capacitances are not easy to cancel, since they are essentially the sum of error capacitances of various sources. The most important ones to consider are the junction capacitances of the switches. By means of special MOS transistor geometries, however, the internal junction capacitance of the switches is made almost constant, permitting internal compensation of C_p with capacitor C_C (see C). This (internal) capacitor's value is equal to that of the switch's junction capacitance C_P and virtually cancels the V_{CM} error. (The V_{CM} term becomes $[V_{CM}(C_P - C_C]/[C_S + (C_P - C_C)] = 0$.) During the circuit's sampling mode, C_C samples the common-mode voltage. Then, during the charge-transfer mode, C_C's polarity reverses. Because C_C is essentially connected in parallel with the switch's junction capacitance, the newly negative charge on C_C cancels the positive charge on C_P.

As for the interpin capacitances within the dual in-line package, they are not canceled but their effects are eliminated with a dummy pin, which places any additional capacitance across the nonprecision sampling capacitor C_S. The pc board's stray capacitances are also referenced in parallel with C_S by adding a shield under the sampling capacitor and tying it to the dummy pin.



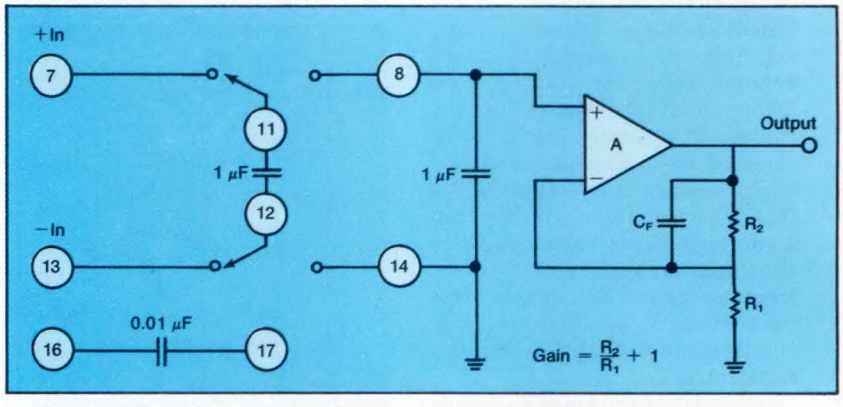
its output to swing fully to zero. As for the performance of the circuit, input offset is less than 3 μV. Drift is below 0.05 μV/°C, and common-mode rejection ratio goes beyond 120 dB from dc to 20 kHz.

Measuring small signals

The LTC1043 also makes an excellent choice in transducer signal conditioning (Fig. 4). Here, the thermistor network is offset with respect to 0°C so that it can work as an accurate subtraction device. Thus, 0°C corresponds to a voltage of 0 V at the output.

Turning a differential signal into a single-ended one, the switch chip extracts the difference between thermistor T's output and a scaled reference voltage. The output amplifier provides calibrated gain, so that the circuit's output voltage will correspond directly to temperature.

Calibration is easy. First the potentiometer is set for a voltage of 1.068 V at pin 7 of the switch chip. Next, pin 13 is shorted directly to the reference's output and the 100°C trim potentiometer is set for an output voltage of 0.2527 V. The circuit is accurate to ±0.25°C over



2. The switch chip and two standard signal-handling capacitors turn a high-quality op amp into a precision instrumentation amplifier that converts differential into single-ended signals. The commutating frequency should be below 1 kHz for best performance. Stage gain is set by two resistors. The feedback loop that includes capacitor C_F gives a degree of external control of the op amp's roll-off characteristics.

Worst-case performance of instrumentation amp

Parameter	LT1001/LT1002	LT1012	LT1013/LT1014
E_{OS}	15 μV	35 μV	150 μV
$E_{OS}/\triangle TC$	0.6 μV/°C	1.5 μV/°C	2 μV/°C
I_B	2 nA	100 nA	20 nA
Common-mode rejection ratio	> 120 dB	> 120 dB	> 120 dB
Gain drift	1 ppm/°C typ*	1 ppm/°C*	1 ppm/°C*
Linearity	1 ppm	1 ppm	1 ppm
Power supply	±5 to +15 V, GND	±5 to +15 V, GND	+5 V, GND to ±15 V

*Limited by gain-controlling-resistors

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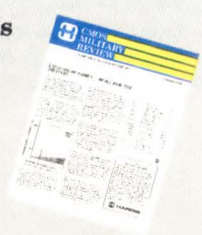
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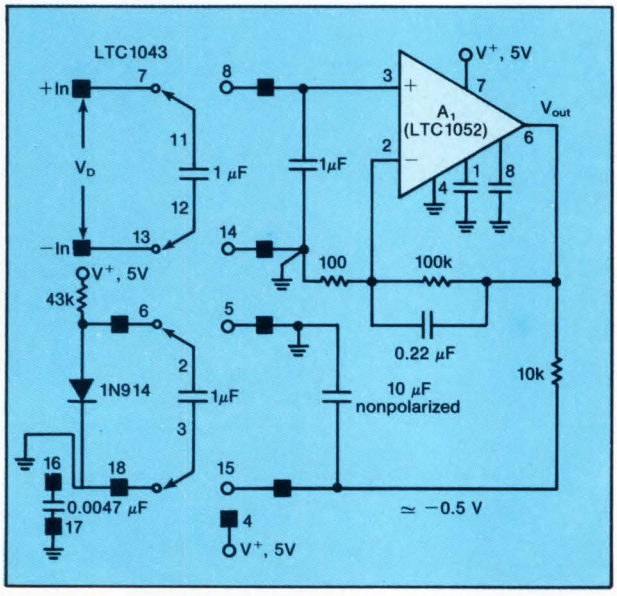
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CIRCLE 66

CMOS Technology: Dual switch chip



3. For especially good performance down to dc, a chopper-stabilized circuit fills the bill. Half the DPDT switch and a diode develop a small negative voltage that biases the amplifier, thereby permitting the circuit's output to swing fully to zero.

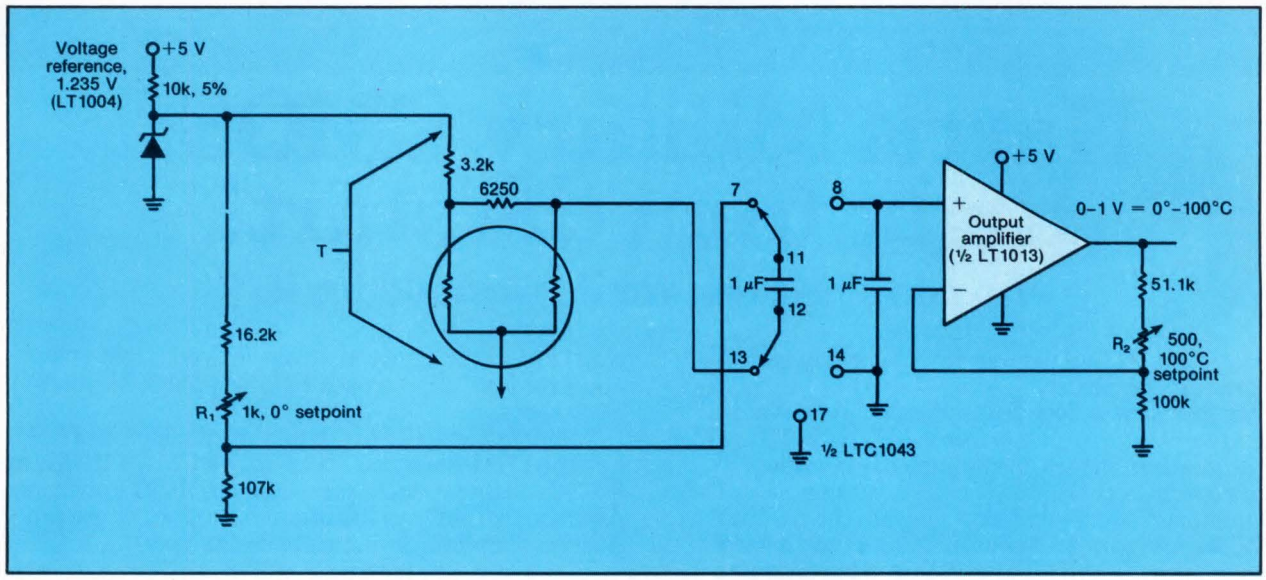
a temperature range of 0° to 100°C.

The LTC1043 can also fit into a voltage-controlled current source having both source and load referred to ground (Fig. 5). A simpler and more precise circuit than the commonly employed Howland configuration, it requires only one precision component—the load resistor. Moreover, it can drive transducers and current-loop transmitters in industrial control systems.

Better power sources

The amplifier in the configuration drives current into the grounded load through the 100-Ω resistor. The 0.68-μF capacitor and the 1-kΩ resistor form a dominant feedback loop that is unconditionally stable. If desired, the remaining section of the DPDT chip can be placed ahead of the amplifier, creating a fully differential voltage-controlled input.

A scheme like that proves handy for offsetting the amount of current in the loop or when the control voltage is not referred to



4. The DPDT switch chip is well-suited to use in low-level transducer circuits. Here a voltage-subtraction circuit permits a thermistor network to deliver a voltage that is directly proportional to the temperature in degrees Celsius. Each easily calibrated unit is accurate to within ±0.25°C over 0° to 100°C.



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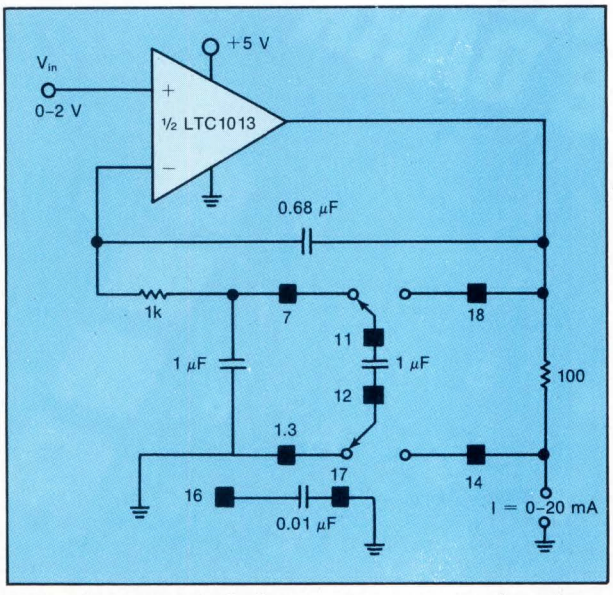


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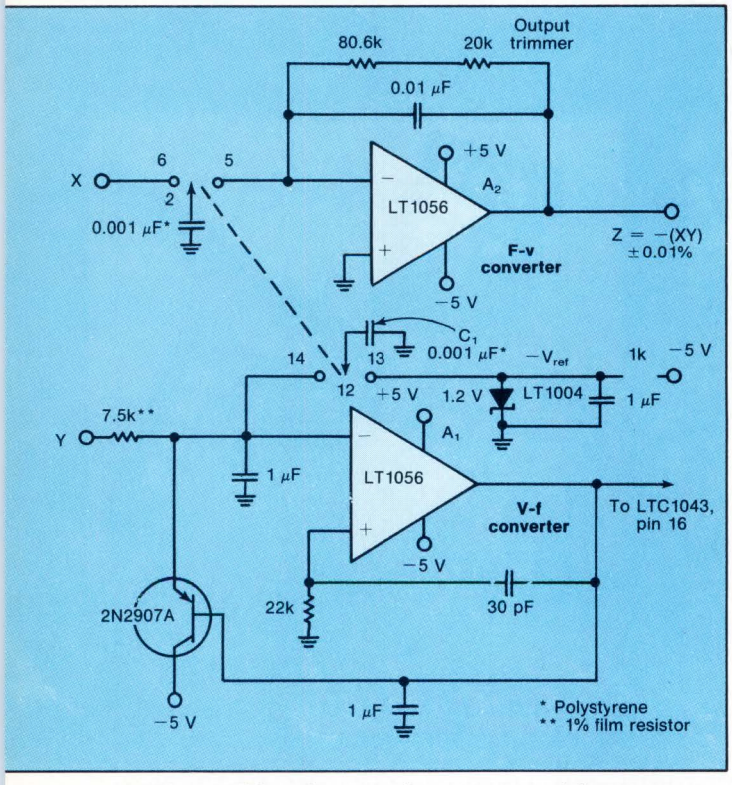
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CIRCLE 67

CMOS Technology: Dual switch chip



5. A voltage-controlled current source needs only one precision component—a load resistor. The circuit is unconditionally stable for input voltages between 0 and 2 V, delivering an output of 0 to 20 mA.



6. Along with voltage-to-frequency and frequency-to-voltage converters, the LTC1043 helps build an analog multiplier that is accurate to 0.01% over the input range of −5 to +5 V. Linearity is 0.005%, and gain drift is 20 ppm/°C.

ground. The accuracy and stability of the circuit is almost entirely dependent upon the characteristics of the 100-Ω resistor.

Voltage-to-frequency and frequency-to-voltage converters capitalize on the LTC1043's ability to manipulate charge, as in an analog multiplier with 0.01% accuracy (Fig. 6). Since the circuit is more accurate than any commercially available analog multiplier, it could be put to work linearizing a bridge or transducer. In fact, it is extremely useful in all but the most stringent applications.

Making an easy conversion

In this circuit, the v-f portion is biased from the Y input. The X input establishes a voltage reference for the f-v portion. Thus the value of X controls the signal path's attenuation from the Y input to the Z output.

In operation, the X and Y input voltages produce a summing current at the input to A_2. Assume that Y is initially zero, and A_1's inverting input is below ground. Therefore the output of A_1 is high. As a result, the switch's oscillator is enabled, and pin 12 of the switch is connected to pin 13. Thus the 0.001-μF capacitor, C_1, charges to $-V_{ref}$. When the inverting input rises above ground, A_1's output flips, driving the switch's clock pin low (the transistor circuit is a start-up loop that ensures switching).

That action connects C_1 to pin 14, pulling charge from the 1-μF capacitor connected at A_1's input and lowering A_1's input voltage. The RC network at A_1's noninverting input provides hysteresis to allow complete charging of the 0.001-μF capacitor at pin 12. The process repeats, with the frequency of oscillation of this loop being directly proportional to the voltage at the Y input (i.e., the discharge time of C_1). As for performance, this circuit provides 0.005% linearity. Scale drift is 20 ppm/°C.

To calibrate the conversion, the X and Y inputs should be shorted, 0.7321 V applied, and A_2's output trimmer adjusted for an output voltage of exactly 3 V. □

How useful?	Circle
Immediate design application	547
Within the next year	548
Not applicable	549

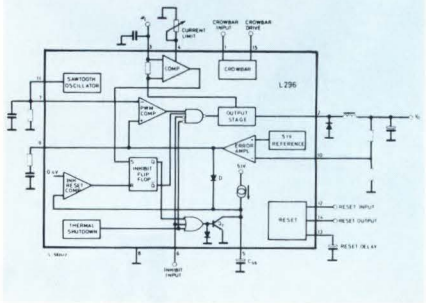


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In fact, all necessary circuitry to build a complete switchmode power supply is housed in the IC's cost-saving plastic Multiwatt® package.

In addition, the L296 includes more control/protection functions, while requiring fewer external circuits. For example, only one capacitor and one resistor are needed for the device's reset circuit to provide a signal to the microprocessor. Plus, with most other switching regulators, an external current limiter must be added; this function is standard in the L296. Soft-start, internal precision reference and overload output protection are also part of the high performance L296 package.

To date, millions of L296 switching regulators are on the job in a host of products including monitors, printers, personal computers and typewriters. The SGS device is in demand because of its exceptional power and its proven track record. In short, the L296 is simply the logical choice for engineers who can't afford to gamble on their power supply design.

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Ripple Rejection	f = 120Hz	60dB

L296 evaluation kit now available from SGS.

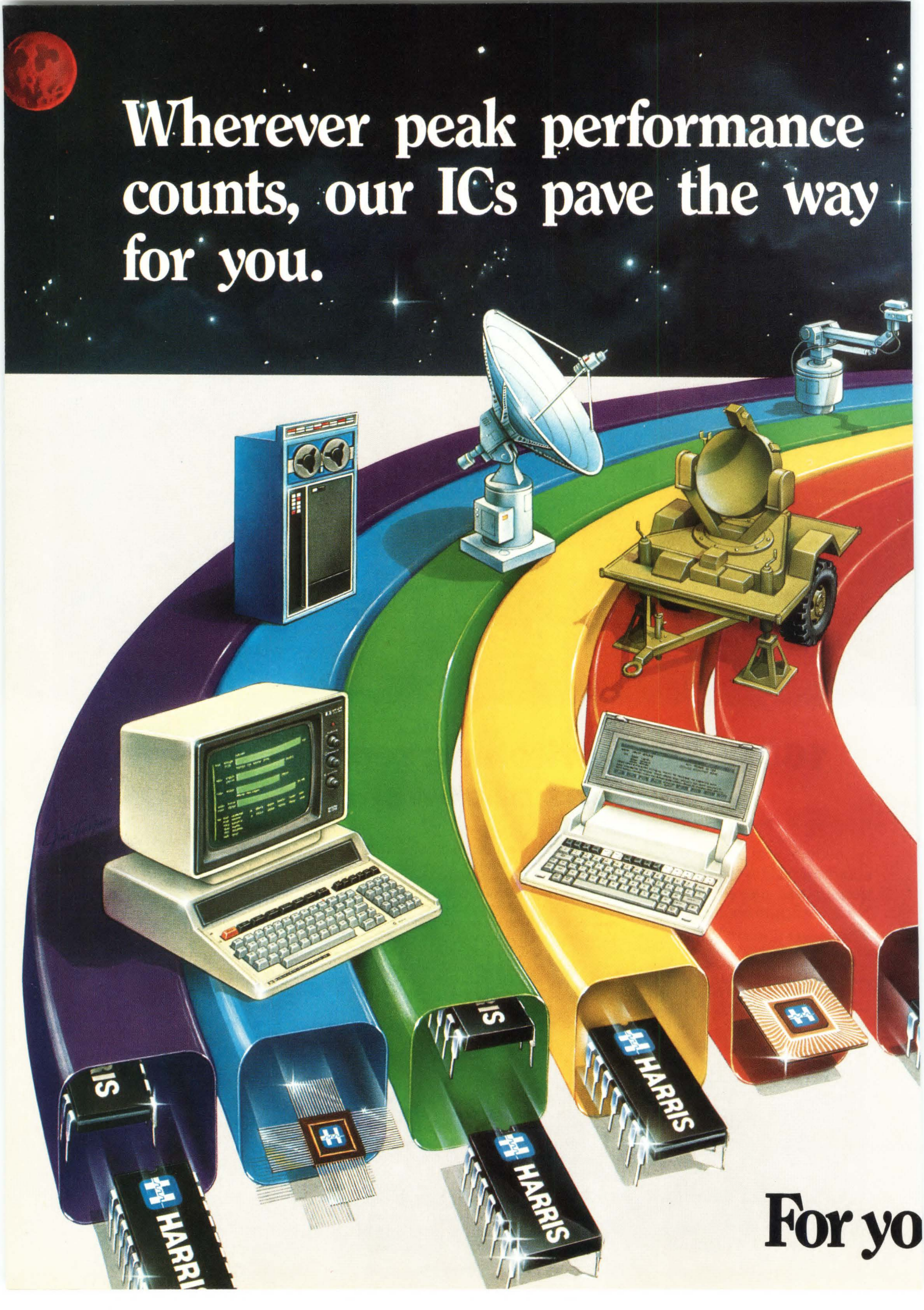
The kit, which is available for immediate shipment, includes an L296, PC board and layout information as well as detailed application notes. To order, send a $10 check to SGS Semiconductor Corporation, Product Marketing, 1000 E. Bell Road, Phoenix, AZ 85022. Or call 602/867-6262.

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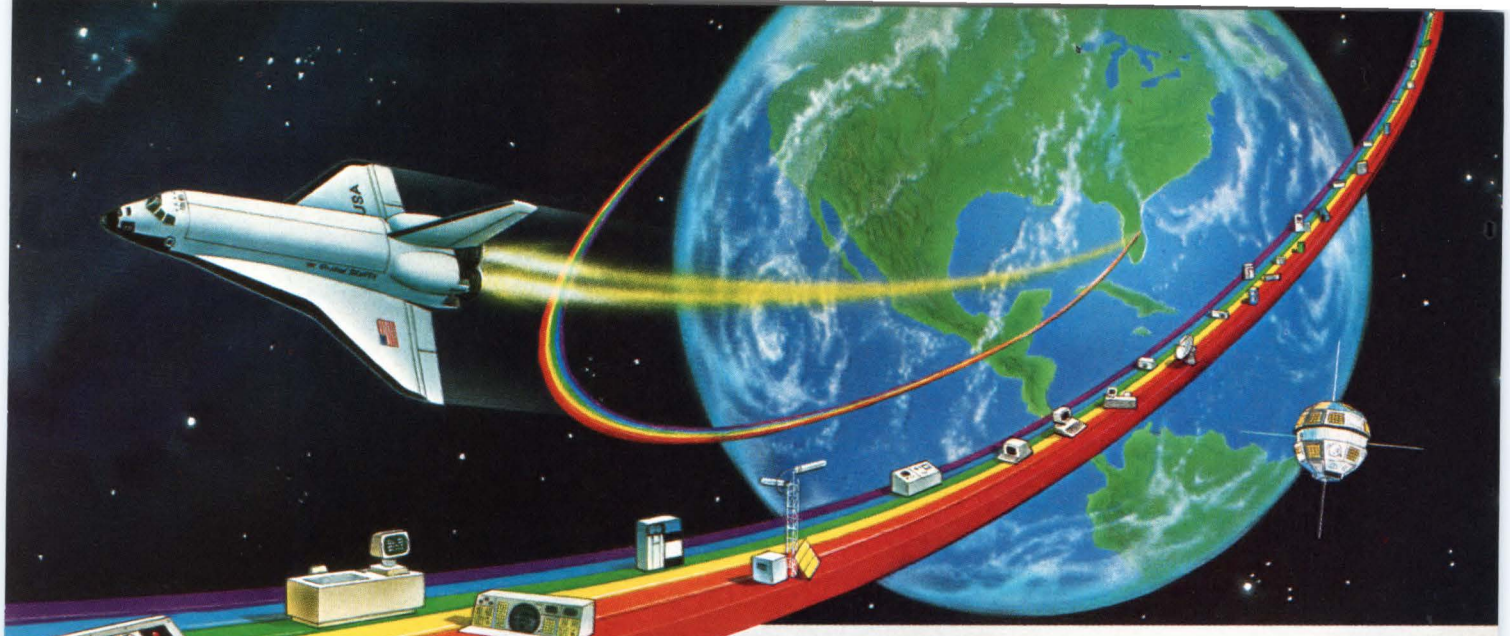
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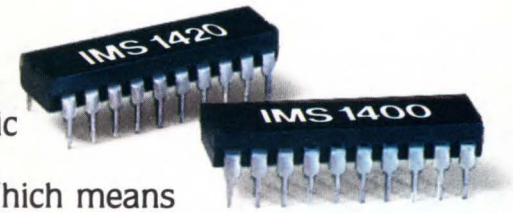
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	55	660	110	IMS1400-55
	70	495	83	IMS1400-70L
	100	495	83	IMS1400-10L
4Kx4	45	605	165	IMS1420-45
	55	605	165	IMS1420-55
	70	495	83	IMS1420-70L
	100	495	83	IMS1420-10L

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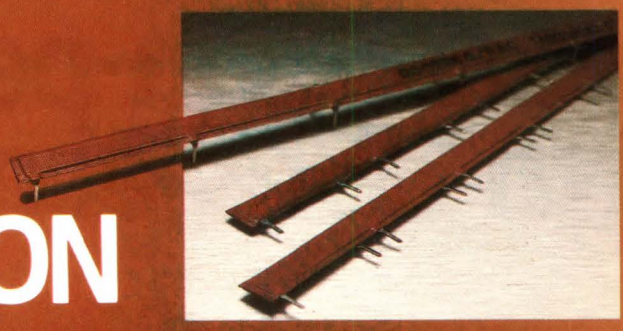
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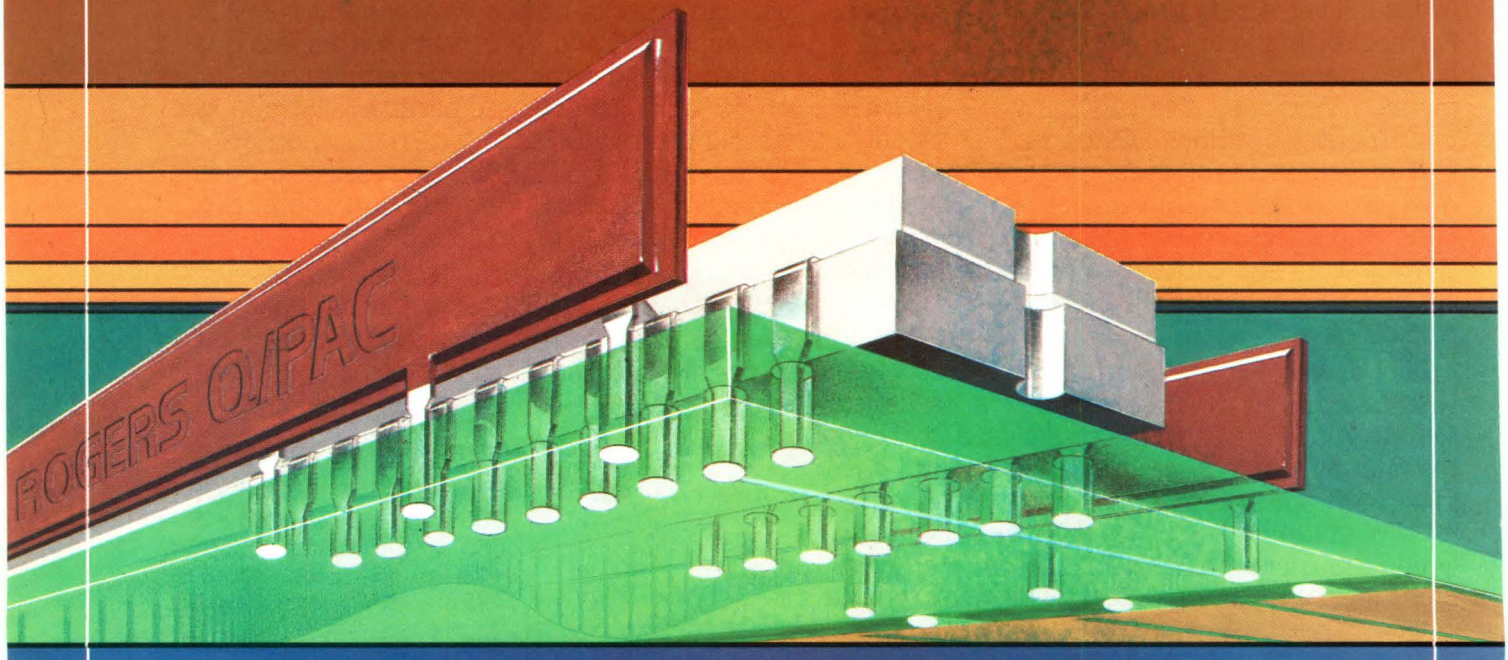
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CIRCLE 71

Image signal processor computes fast enough for gray-scale video

Handling millions of computations per video frame, a pipelined, dedicated chip attains system speeds 1000 times those of 16-bit microprocessors.

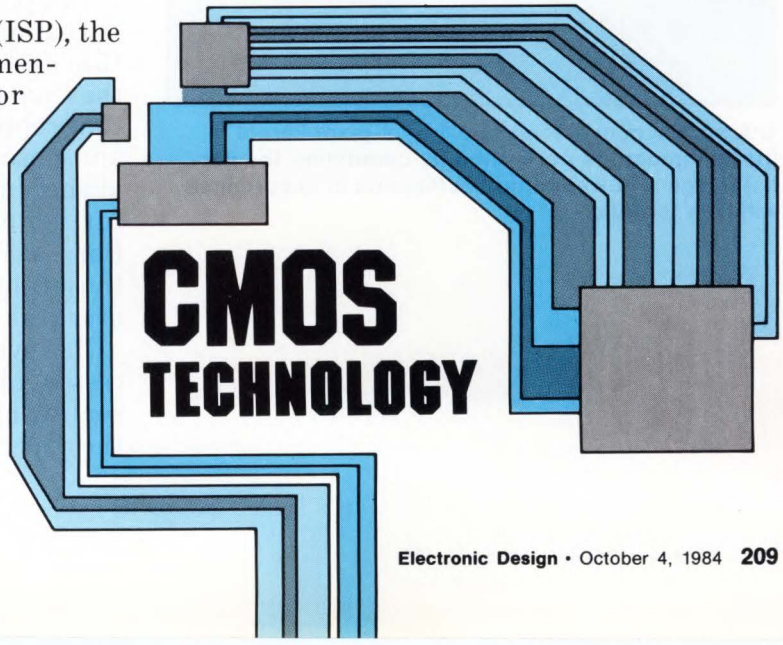
Object recognition in robotics and image enhancement in document processing require tremendous processing power. Millions of multiplications and additions must be done at speeds high enough to meet the real-time needs of the production line. That requirement, in turn, has limited the application of image-processing techniques to monochromatic (and hence binary) images and to either very simple real-time applications or off-line processing, in which speed is not critical.

Now, however, single-instruction multiple-data-stream processing and pipelining combine in a specialized processor chip to yield system speeds 1000 times faster than those of systems based on 16-bit microprocessors and 100 times faster than many 32-bit superminicomputers.

Dubbed an image signal processor (ISP), the circuit performs most of the two-dimensional image processing needed for gray-scale video images consisting of 256 by 256 picture elements. The chip can also be made to handle both color and monochromatic images. Thus its gray-scale capability opens up such new image-processing applications as automatic inspection systems (for detecting defects like cracks, smears, spots, and uneven color) and vision systems for moving robots, enabling them to recognize the ends of walls or the border between a wall and the floor.

The chip, designated the HD6184OR, holds over 60,000 transistors in an area somewhat over 7 by 8 mm. It is fabricated with a 3-μm CMOS process and will come in a 64-pin dual in-line package.

Image processing, in general, is accomplished in five consecutive steps: observation, sampling and quantizing, preprocessing, fea-



Tadashi Fukushima, Hitachi Ltd.

Tadashi Fukushima is a researcher in digital signal and image processing, pattern recognition, computer vision, and VLSI hardware implementations at Hitachi Research Laboratory, Hitachi Ltd., Hitachi, Japan. He holds a 1977 BE in electrical engineering from Kyoto University and a 1979 MSCC in computer science from the University of Illinois.

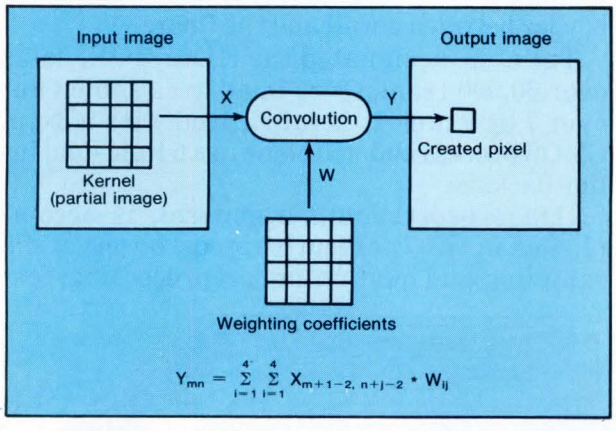
CMOS Technology: Image signal processor

ture extraction, and object recognition. In an industrial application, the desired object is usually first observed with a video camera, and the photographic image is then digitized.

Since camera characteristics and light reflection typically introduce random noise and shading into the digitized image, preprocessing is used to remove the unwanted elements. Next, various features are extracted from the smoothed image, and finally, the extracted features are used by the system to identify the defined object.

A long time

The preprocessing and feature extraction stages consume the most time, since both must handle the huge digital data base that represents an image. For example, mask operations of a 3-by-3-pixel kernel (the number of input pixels used to compute one new pixel) are powerful processing functions for these steps, but even they require several seconds on a superminicomputer. However, a dedicated image signal processor chip can reduce the computational task to a few milliseconds, so that real-time gray-scale image processing becomes cost-effective.



1. A spatial convolution of a 4-by-4-pixel kernel (partial image) is performed by combining the partial image and weighting coefficients in accordance with the formula.

Optimized for noninterlaced 256-by-256-pixel images, the image signal processor performs all the basic calculations, representing each pixel with an 8-bit word. Multiple processor chips can expand the number of computations in the X, Y, and Z directions, handling larger displays or improving the throughput of single tasks. A system based on this chip can process a 256-by-256-pixel gray-scale image in just 10.9 ms—fast enough to handle the video frames produced by a TV camera.

The computational kernel performed by the chip can be extended in two ways. In the first, the designer simply adds more chips, while in the second, the circuit or circuits are time-shared. For high throughput, the first method is best, since throughput can be maintained for a small increase in hardware. The second approach keeps hardware costs down but reduces throughput.

Repeated operations do spatial convolution

Spatial convolution is one of the most basic computations used in gray-scale image processing. It consists of many repeated arithmetic operations—a made-to-order problem for the image signal processor chip. For example, in a simple 4-by-4-pixel spatial convolution (Fig. 1), 16 weighting coefficients are used with the pixel data. First, the 16 adjacent pixels of the 4-by-4 region are removed from the image data. The 8-bit data word representing each pixel is multiplied by one of the weighting coefficients, and the 16 products are finally summed to form a single output word representing the convolved pixel.

That process, totaling 16 multiplications and 15 additions, must be repeated for every pixel in the final image. For a 256-by-256-pixel image, that represents over 1 million multiplications and close to a million additions—to be accomplished in just 10.9 ms for one video frame. That further extrapolates to 200 million computations/s. Typical general-purpose computers do those calculations sequentially and thus run far over real-time deadlines.

In a system that uses four image signal processor chips and delay elements, the data representing an unprocessed image is scanned from the upper-left corner to the lower right, just as

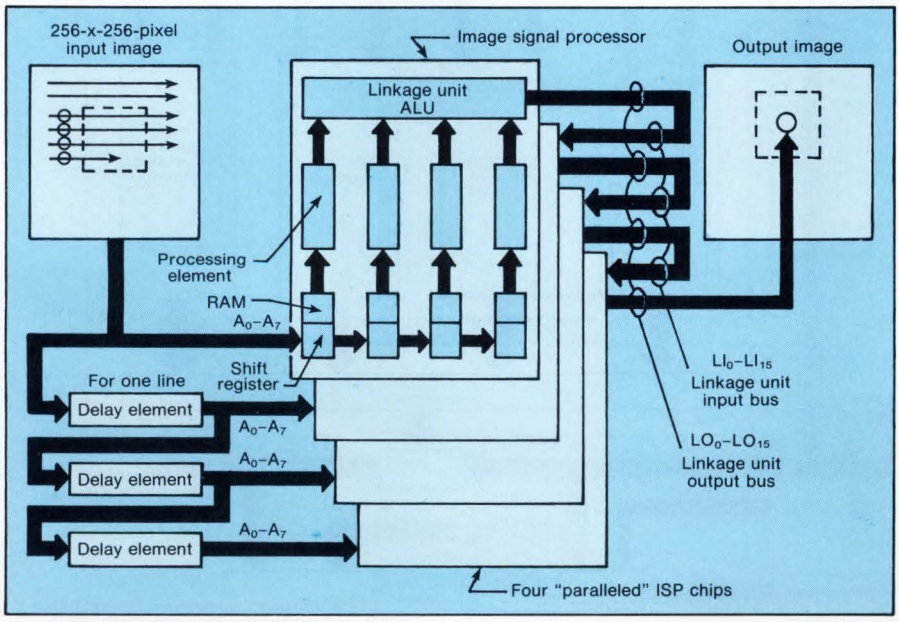
TV images are scanned (Fig. 2). The words representing the pixels in each of the four scan lines are then sent through the delay elements to all except the first processor. The first chip in the pipeline receives its four words directly, needing no delay in this combinative process. Each delay element (typically an adjustable shift register) must hold the pixel word for as long as it takes its preceding processor to convolve one full line of image data. Thus at any time, a set of four words can be sent to the four-chip array.

Since each chip contains four 8-bit shift registers, the four processors can together "freeze" a 16-pixel data packet. In another part of the chip, the weighting coefficients are stored on small RAMs prior to the computation. The chip then multiplies all four words at once by the four data coefficients in its corresponding processing elements (one for each word). Those products are sequentially summed in the final arithmetic and logic unit and sent out to the system image memory (Fig. 3). In this sequence, all the processing elements on the chips operate in parallel and the full arithmetic operation is done in pipelined fashion.

Each image signal processor works on four data words in parallel, its four identical processing elements simultaneously executing the same operations. Each processing element comprises an 8-bit ALU followed by an 8-by-8-bit parallel multiplier. In addition to those elements, the chip contains five other sections: the data, memory, linkage, evaluation, and control units.

The data unit includes the string of four 8-bit shift registers and supplies the processor unit with the partial image data. Each register obtains that data from the left and transfers it both to its associated processor element and to the register to the right. That double data transfer is one of the keys to the system's architectural flexibility, permitting performance enhancement or cost reduction through the addition or subtraction of chips.

The memory unit holds the weighting coefficients for spatial convolution in its four 16-word-by-8-bit RAMs. (In other applications, it might hold templates for pattern matching, for example.) Each RAM can be addressed via external signals (the memory register address lines MRA_0-MRA_3), with all four RAMs being



2. Four image signal processors are interconnected by feeding the pixels from four scan lines into each chip and cascading the linkage units so the results of the upper chip are fed into the one below. In this way, a 4-by-4-pixel partial image can be convoluted fast enough to permit the entire 256-by-256-pixel image to be processed in just 10.9 ms.

addressed in parallel—the four data words in the matching locations of each RAM are accessed simultaneously and sent to the corresponding processor element.

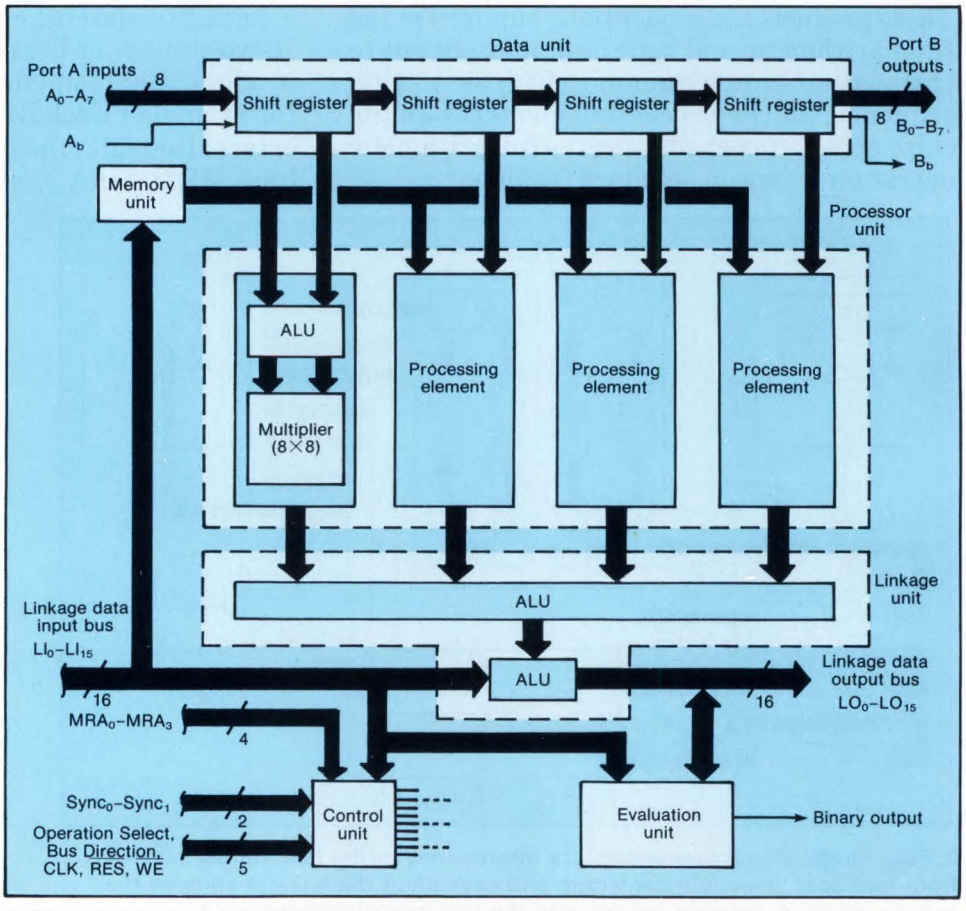
The four processing elements feed their 16-bit outputs to the linkage unit, a four-input ALU whose resultant 16-bit output becomes one of the two inputs for a two-input ALU that also delivers a 16-bit sum. The two-input ALU can get its other operand from a variety of sources—possibly the external system, another weighting coefficient, or the output of another image processor chip.

The evaluation unit

The evaluation unit contributes binarization and clustering toward the final results of the linkage unit. Binarization is the term for producing a binary image from a gray-scale one by assigning the chip two fixed- or floating-point threshold values. Clustering in this context describes the chip's ability to partition a color image into several clusters, each of which has as its standard color three gray values of green, blue, and red. Every color pixel of the input image has its color distance from the standard colors calculated and is classified into that cluster to which it is closest.

Two 16-bit comparators and some other circuits make up the processor's evaluation unit. Each comparator possesses one rewritable comparison register to allow both fixed- and floating-point binarization. The comparators also control a binary counter (not shown in Fig. 3) that creates the cluster numbers.

The control unit's four 16-bit registers hold the setup commands that determine how the chip responds to incoming data. Those reg-



3. The six basic subsections of the image signal processor are the data memory, processor, linkage, evaluation, and control units. The heart of the chip, though, is the processor unit, consisting of four subsections called processor elements.

isters, typically set up prior to processing, are the key to implementing various image-processing algorithms.

Multiple input and output buses and control lines bring the pin count of the image signal processor up to at least 64. The chip contains a four-line address bus; ten signal, control, and power lines; and four data buses. Two of the buses are 8 bits wide and have a ninth control line. The ninth line of the 8-bit A and B buses (Ab and Bb) provides an active-high Data Valid signal. The other two bases are 16 bits wide.

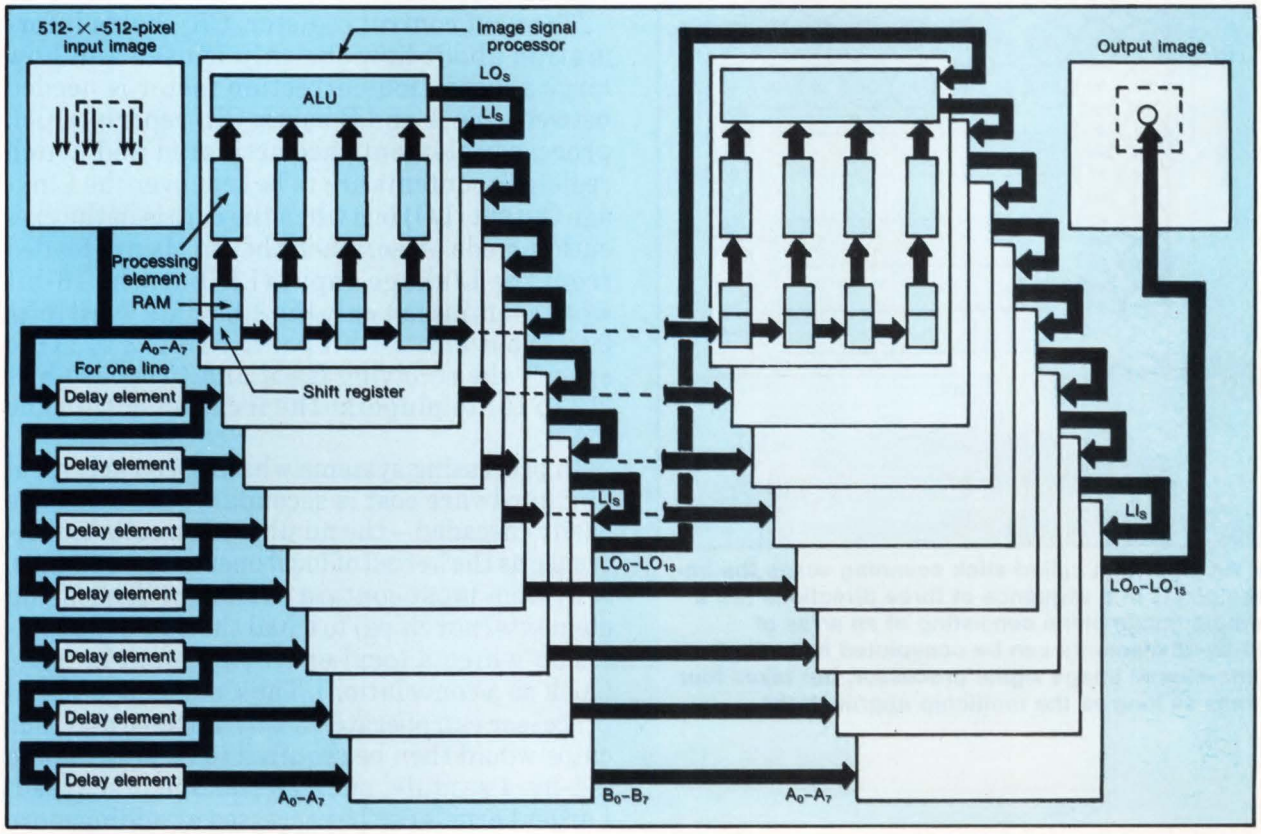
The A bus only accepts data, while the B bus either accepts or sends it. The Bus Direction signal (BD) controls the direction of data flow on the B bus—when BD is low, data flows out of the chip; when it is high, data flows in and permits the chip to "back up" the data stream if necessary. (The Bb line, though, validates data only when the chip is sending.) When several image processor chips are used in a system, one architectural scheme permits the B outputs of one chip to feed the A inputs of the next.

The A bus would typically accept 8-bit words that represent either one gray-scale pixel or eight monochromatic (binary) pixels. Also, for gray-scale data words, the data can be represented in either two's complement or in binary magnitude code.

The one-way 16-bit buses handle linkage input and output. The first feeds either chip initialization data or interim (partially processed) data to the image signal processor. The linkage output bus delivers the contents of the linkage, evaluation, or control units to external systems or other processors.

Choosing operations

What the chip does with the delivered 16 bits is determined by the state of the Operation Select signal (OPS). When OPS is low, data is sent to the internal memory or to evaluation or control units; when it is high, data flows into the second port of the final ALU in the linkage unit where it is combined with the 16-bit result from the four-port ALU. The resulting 16-bit

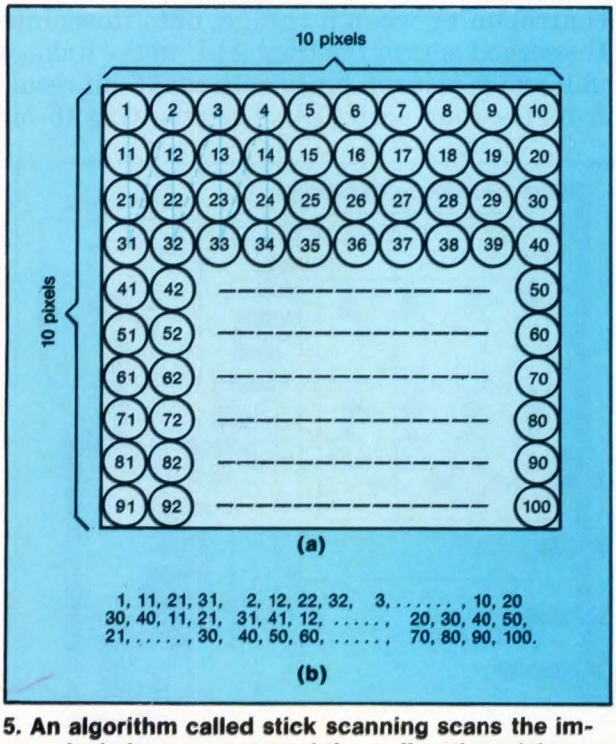


4. To handle an 8-by-8-pixel partial image, 16 image signal processors can be interconnected along with seven delay elements. They perform the full image convolution in just 43.7 ms.

word is represented in two's complement form.

The OPS state and the initialization of the control registers together determine which unit sends its contents out through the linkage output bus. Besides sending the results off chip, the linkage unit also sends the 16-bit word to the evaluation unit to receive some further processing for clustering or binarization; the result is finally sent out either through the linkage output bus or the single Binary output (BNR).

Four memory register address lines, MRA_0–MRA_3, permit the user to select one of the 16 RAM locations (the same one simultaneously in all four RAMS) when OPS is high. When the line is low, the address lines select one of the control registers. The chip also contains a reset signal that can clear all registers before loading data. For general system and data input timing, there are two synchronization signal inputs ($Sync_0$, $Sync_1$) and a system clock input. The clock signal can reach a maximum 6 MHz—the same rate used by most TV scanning systems.



5. An algorithm called stick scanning scans the image pixels in a sequence of three directions (a); a simple image plane consisting of an array of 10-by-10 elements can be convoluted by a single time-shared image signal processor, but takes four times as long as the multichip approach (b).

Register setup prepares the chip

Before the image-processing chip can be used, it must be put into a setup mode with OPS so that the control registers and RAMs can be loaded. An occasional third step can be taken to initialize two comparison registers in the evaluation unit. After that, OPS switches the chip into the execution mode, and an external controller supplies the control signals needed to sequence the chip through the desired algorithm.

All 16 bits in control register 0 (CR_0) and the first 9 bits in CR_1 define the functions performed by the various ALUs and the evaluation unit. Six of the remaining 7 bits in CR_1 define the image data type on the A and B buses, image data flow control, and linkage data flow control. The last bit on CR_1 is reserved for future use.

The next control register, CR_2, holds information about how the chip is used and how large a distortion-correction factor is needed between the A and B buses. CR_3 reports which processor elements are activated and which register's contents are to be sent over the Linkage Output (LO) bus when the chip is in the execution mode. Also, when the RAMs are loaded from the Linkage Input (LI) bus, the 16-bit word contains not only the 8-bit data word (bits 0 to 7) but also a 4-bit pointer (bits 8 to 11) to specify the receiving RAM and 4 encoded bits (12 to 15) to pinpoint the location within the RAM.

In processing systems where speed is critical and hardware cost is secondary, the chips are easily cascaded—the number of circuits can increase as the kernel of local operations expands. A system must contain sufficient processing elements (not chips) to equal the number of pixels on which a local operation must be done (such as a convolution). Thus, one image signal processor can operate on 1 by 4 pixels, and four chips would then be required to rapidly handle a 4-by-4 sample, such as the one discussed. Larger kernels can be processed by adding more processors, both vertically and horizontally.

For instance, an 8-by-8-pixel system requires 16 processors and 7 one-line delay elements (Fig. 4). Further expansion to a 16-by-16-pixel kernel would require 64 processors and 15 delay elements to process the data in real time.

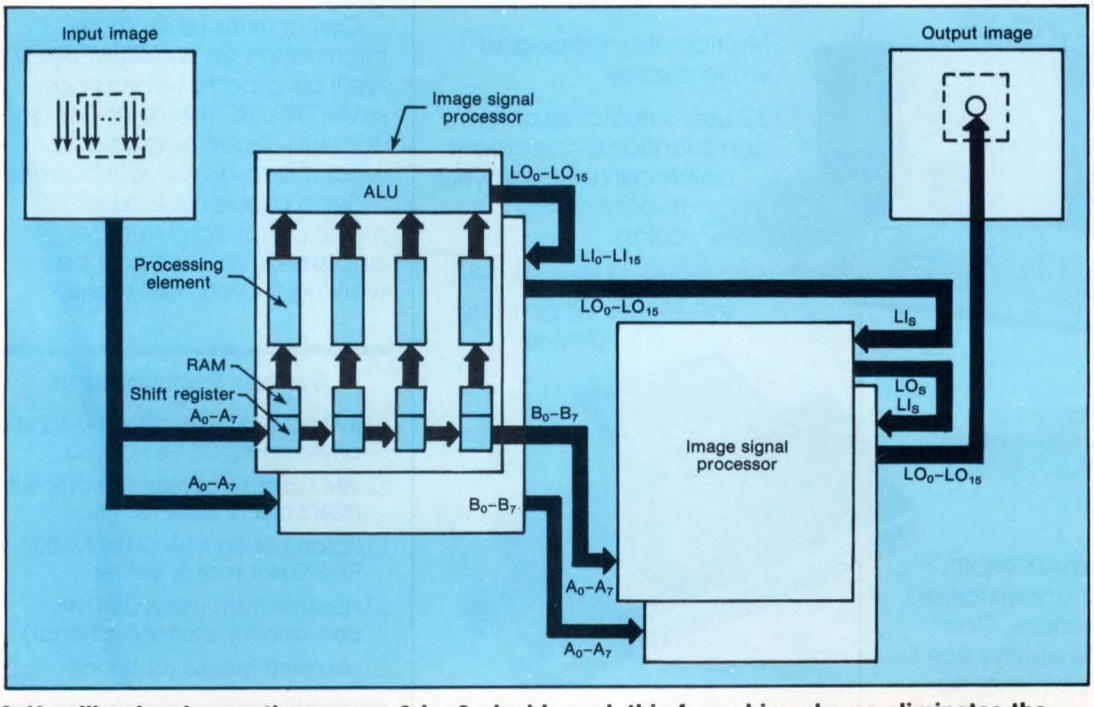
Time-sharing keeps hardware minimal

If hardware has to be minimized, the processor can be multiplexed and the number of chips can be cut by 75%, as compared with the previous approach. A different scanning scheme, called stick scanning, requires no delay elements and involves scanning the data array in three directions: from top to bottom, from left to right, and again from top to bottom.

In this approach, a set of pixels scanned in the first direction is called a stick; the number of pixels in one stick defines the stick length. Thus, if local operations for a 4-by-4-pixel sample of a simple 10-by-10-pixel image (Fig. 5a) are done with one processor, the stick scanning length must be four, and the pixels must be scanned in the sequence shown (Fig. 5b). Time-sharing the processors sets the delay step of the internal shift register to four, whereas in the other technique the delay was set to one. However, processing takes four times as long, since one chip must do the work of four.

If the time-sharing concept is expanded to a larger system, four image signal processors can carry out the local operations on an 8-by-8-pixel subset (Fig. 6). In that scheme, the image data is alternately sent to the two left-most processors to eliminate the line delay elements. The time-shared approach extends the time of a 256 by-256-pixel convolution from 10.9 to 43.7 ms; a 512-by-512-pixel image slows from 43.7 to 174.8 ms.□

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



6. Handling local operations on an 8-by-8 pixel kernel, this four-chip scheme eliminates the delay elements and 75% of the processor chips used in the approach of Fig. 5, but pays a speed penalty—it takes four times as long to do the computations.

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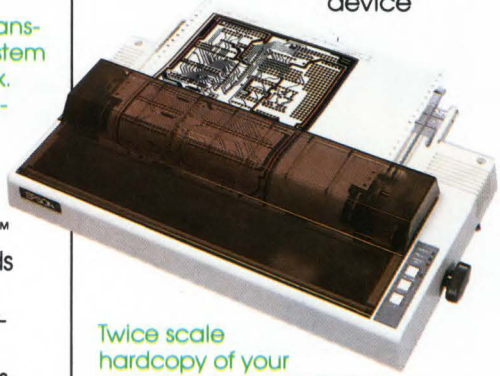


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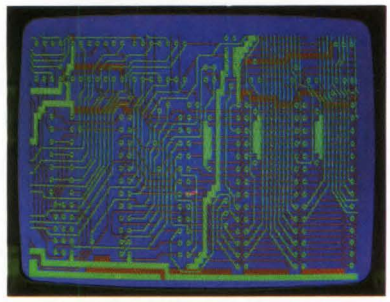
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- ☐ Houston Instrument DMP-41 pen-and-ink plotter (optional)
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Multiplier-accumulator derives high performance from 1-μm CMOS

With a 1-μm effective channel length, the chip fits in a pin-grid array with enough pins for nonmultiplexed outputs—an asset for many digital signal-processing tasks.

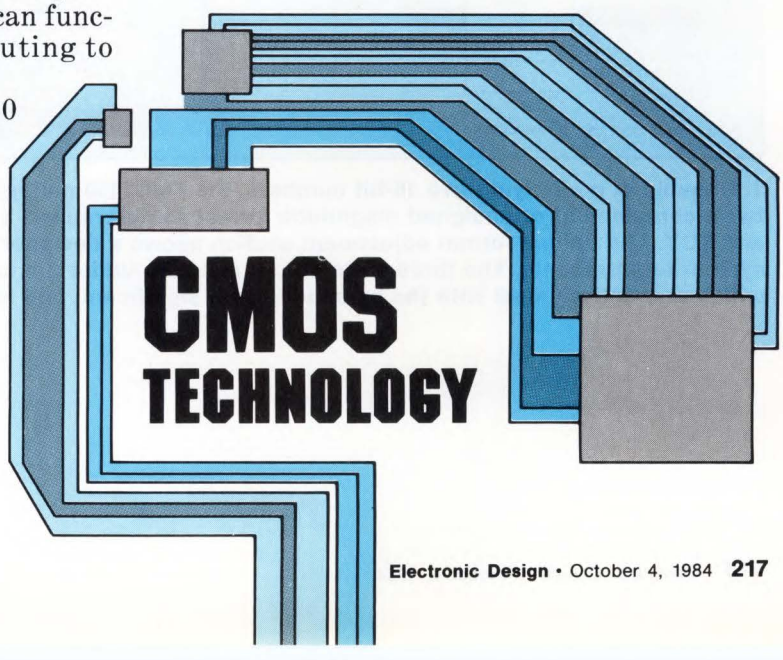
Continually shrinking features promise a land of plenty for virtually every aspect of electronics, with digital signal processing marked as a chief beneficiary. Chip architecture and packaging share some credit, but fine-line lithography deserves the bulk of it. Though it is not uncommon to hear of 2- and 3-μm designs, until now no standard production line has seen a chip that attains a 1-μm effective channel length.

With that process, a CMOS multiplier-accumulator scores some impressive points in speed, size, and architectural improvements. The same process that compresses the chip also enables it to squeeze into a pin-grid array that is smaller and has more pins than a 64-pin DIP. With extra control lines at hand, no outputs need be multiplexed; instead they all can function simultaneously, again contributing to speed.

In fact, the monolithic TMC2160 multiplier-accumulator operates at twice the speed of current bipolar devices. That performance permits wider-bandwidth digital signal processing than can be attained with current multiplier-accumulators or else greater resolution in digital filtering and spectrum analysis.

The device's 88-lead pin-grid array package lets it make all output bits available at one time—a so-called "broadside" output that is needed for block floating-point FFT butterfly operations and integer arithmetic in Fortran multiplication. Also, because of its CMOS construction, the TMC2160 reduces system power consumption, making it a candidate for use in battery-powered equipment or systems in which thermal management is a problem (see "Behind the CMOS Process," p. 219).

Previous generations of multiplier-accum-



Fred Williams, TRW Inc.

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CMOS Technology: Multiplier-accumulator chip

ulators were limited by pin count in the number of control lines that could be employed. The TMC2160's nine control lines (excluding clock enables) give it greater flexibility than the older devices.

Two of the control leads, for example, are independent two's complement lines that make possible a true double-precision function. A format adjustment line allows a designer to position the binary point to best match system requirements. Such features were always available on multiplier devices, but not on multiplier-accumulators.

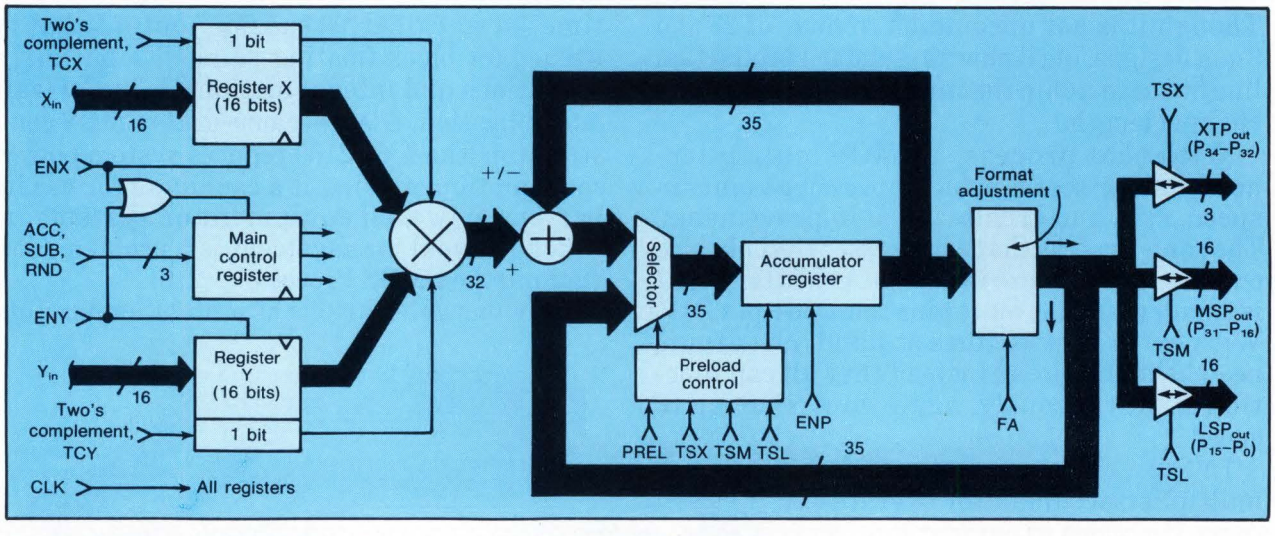
Rapid growth in microprogramming as a design tool has influenced the chip's design. Previously, it was usual to rely on signal edges to initialize operations. As an alternative way of handling control operations, microprogramming encourages the use of one master-clock with on-chip enabling circuitry—an approach adopted by the TMC2160.

In a broad realm of applications, digital signal processing can replace analog methods because of its improved stability, higher performance, and programmability. The decision to use it is determined not only by bandwidth and performance considerations, but by economic concerns as well. As a cost-effective, high-performance device, the multiplier-accumulator extends the applications to which digital signal processing applies.

Three buses maximize speed

The chip is well suited to widely used three-bus digital signal processor architectures. In such system, one input port connects the multiplier-accumulator to the data memory bus while another port connects it to the coefficient or operand memory bus. Its output port sends results back to data memory over an output bus. Usually, all three buses can be kept fully loaded, maximizing system throughput.

The chip's control signals must be produced by the designer in two different ways: through random logic or microprogrammed control. In a simple system, random logic, such as hard-wiring control lines either high or low and using gates and counters, is sufficient. For instance,



1. Capable of multiplying two 16-bit numbers, the TMC2160 multiplier-accumulator accepts inputs in either two's complement or unsigned magnitude format as determined by its two's complement control lines, TCX and TCY. The unique format adjustment section allows a designer to position the binary point to match system requirements. The three-state output lines are under the control of the TSX, TSM and TSL inputs, which respectively deal with the extended, most significant, and least significant products.

finite impulse response (FIR) filters usually require only two control lines on the multiplier-accumulator—its Accumulate (ACC) and Round (RND) controls.

When control lines do not operate on a simple cycle, microcoding becomes a reasonable alternative. In its simplest form, a ROM can be addressed by a counter and other circuitry to generate the control line sequence. If a multiplier-accumulator is added to a microcoded system, control signals can be stored directly in the program ROM or RAM.

A TMC2160 user sees a device that has two input registers that accept numbers. After loading, the chip multiplies the numbers, selectively accumulates or subtracts them, and places the result in an output register.

Operating details

Register loading occurs on the rising edge of the master clock when the Product Enable command is asserted. Three-state output drivers send out the result on command. The device can operate on two's complement numbers, un-

Behind the CMOS process

A 1-μm CMOS process depends on a retrograde p well to define n-channel transistors. In a retrograde p well, the doping density is lower at the surface than farther down, setting up an effective barrier to the currents responsible for latch-up. No other isolation areas are needed, so the process yields a high packing density.

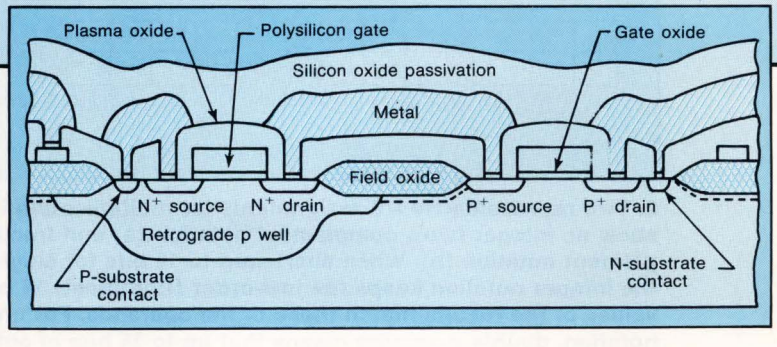
Full-wafer optical stepper photolithography and plasma and reactive ion etching team up to precisely control critical device dimensions. This type of CMOS consumes significantly less power—an order of magnitude less—than the conventional version, entailing higher reliability than possible with CMOS, NMOS, and bipolar. High performance is due to the effective channel length of just 1 μm.

The starting substrate is conventional n-type <100> single-crystal silicon (see figure). A local oxidation process grows the field oxide, which is followed by the formation of the retrograde p well. That well is created by a boron implantation that defines a region for the n-channel transistor. In addition, boron deep beneath the field oxide serves as a field-isolation guardband in the p well, preventing interdevice leakage.

A retrograde well effectively reduces the vertical parasitic npn bipolar transistor current gain by about an order of magnitude compared with conventional p well processes. As a result, chips have both a high immunity to latch-up and high packing density.

A wet-oxidation technique grows a thin gate oxide, a step that gives both n and p devices intrinsically high transconductance. After depositing a thin film of polysilicon, the layer is photomasked to delineate the gate electrode area and anisotropically etched. Next the polysilicon gate is defined, and self-aligned arsenic and boron implants are used to form the shallow source and drain regions for the n- and p-channel devices, respectively. All is done in two independent masking steps, followed by a short annealing cycle. An oxide layer is deposited as a dielectric between polysilicon and metal, and etching opens the contact windows to the n and p polysilicon areas.

To ensure good contact with the chip, three metal layers—platinum, titanium-tungsten, and aluminum—are applied to the wafer, a structure that prevents aluminum spiking in the shallow source-drain region. Finally, low-pressure chemical vapor deposition lays down a film of silicon nitride at low temperature as a passivation layer. Etching that layer provides a contact-pad area for external connections and also permits chips to be assembled in plastic packages.



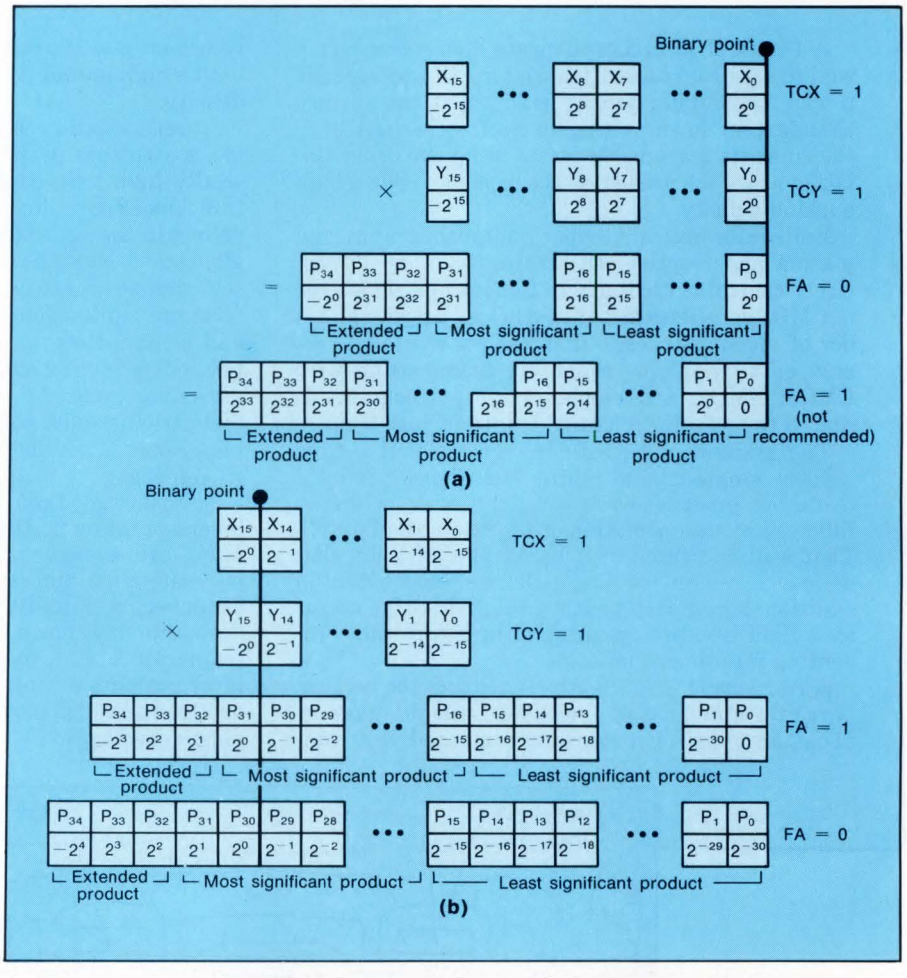
CMOS Technology: Multiplier-accumulator chip

signed magnitude numbers, or one of each type.

The multiplier array uses a modified form of Booth recoding. In conventional multipliers, groups of AND gates generate partial products from each bit of the multiplicand. The idea behind Booth recoding is to generate partial products from more than 1 bit of the multiplicand at a time. If the multiplicand is considered 2 bits at a time, the partial product will be 0, 1, 2, or 3 times the multiplier. Multiplication by 0 or 1 proceeds in the conventional manner, with AND gates. Multiplication by 2 is merely a one-position shift left, and multiplication by 3 is a two-position shift left followed by a subtraction of the original operand. This concept can obviously be extended to 3 or more bits at a time.

Generating internal partial products is, of course, only half the task. The other half is adding up all the partial products. Accordingly, the TMC2160 incorporates a special fast-carry adder circuit along with carry look-ahead and conditional sum adders (Fig. 1).

Other features of the multiplier-accumulator include a patented configuration of drivers, buffers, and registers that permits the output port to be used for preloading a constant into the output register. This feature increases the bus bandwidth for multiplication-addition



2. Two representative I/O assignments for multiplication in a 32-bit format show an integer two's complement notation (a) and fractional two's complement notation (b). When shortened to 16 bits for single-precision systems, the integer notation keeps the low-order (rightmost) 16 bits, so that the place values of the results match those of the operands. For unsigned fractional notation, double-precision means that up to 35 bits of output are available.

$(A \times B + C)$ operations. Internal ½-LSB rounding is also available, and this is coordinated with the format adjustment to retain as much precision as possible in the output signal.

Choosing a number format

When a sequence of numbers represents a signal, the largest number should be smaller than the largest signal expected, to avoid distorting the signal. Many designers find it easier to work with normalized values where the signal ranges from -1 to $+1$ LSB less than a value of $+1$. Others prefer viewing the signal as an integer value. The binary point can be placed anywhere within the bit field, which in practice means anywhere within a 16-bit word. The choice of normalized or integer values is arbitrary from a mathematical standpoint, but has practical consequences.

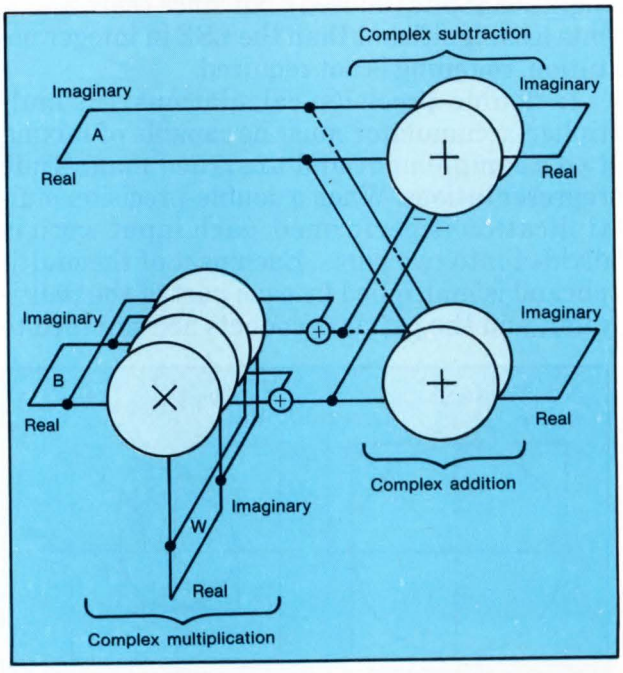
The first consideration is that coefficients, unlike signal values, cannot be scaled arbitrarily if feedback exists anywhere in a system. Even if a signal is represented as an integer value, a system with feedback must work properly for fractional-valued coefficients.

The product of two 16-bit numbers can have up to a 32-bit product. But increasing the word size with each calculation is undesirable, so results are usually rounded to the basic word size of the system—16 bits in most cases. To maintain the modularity of a system, designers like to use the output of one process to drive the next (this is important in obtaining the lowest noise response of an infinite impulse response, or IIR, filter). This requires that the binary point be in the same position for each number. Designers therefore use mostly fractional numbers or integers; mixed numbers are used very seldom.

A numerical representation problem arises with two's complement notation when fractional numbers are represented. That is, -1 can be expressed, but $+1$ can not. Since the product of -1 and -1 is $+1$, errors can occur in conventional systems.

The previous versions of multiplier-accumulators have had difficulties dealing with problems of fractional-valued coefficients, binary point positioning, and fractional two's complement notation. The TMC2160 is the first device of its type to address all three problems. For example, conventional multiplier-accumulators can handle the $-1 \times -1 = +1$ two's complement condition, but they produce a net shift right if the sign bit is kept. Multiplier-only devices offer a left-shifting format that overflows on -1×-1, giving an erroneous result of -1. When a multiplier-accumulator solves problems such as these, the entire design of a digital signal-processing system becomes much simpler.

Two basic approaches are involved in numeric scaling: fractional and integer notation. In addition, numbers can be either signed (two's complement is the notation of choice) or unsigned (magnitude only). This gives four com-

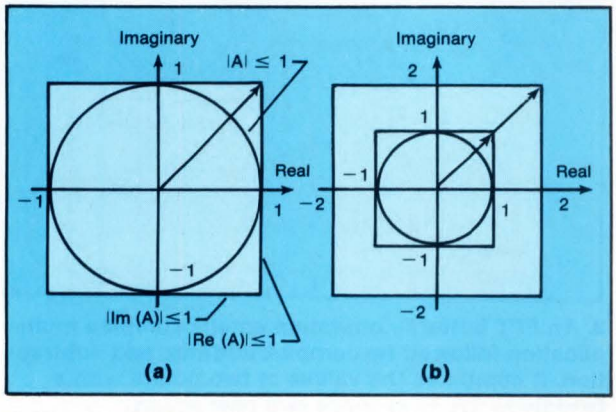


3. An FFT butterfly operation entails complex multiplication followed by complex addition and subtraction. It combines the values of two points with a twiddle factor to produce two new points.

monly used formats: fractional two's complement, fractional unsigned magnitude, integer two's complement, and integer unsigned magnitude.

Fractional and integer notations are described as left-justified and right-justified, respectively. With the multiplier-accumulator, when assignments of bits have a 32-bit format, results must be shortened to 16 bits in single-precision systems (Fig. 2). For integer notation, the low-order (right-most) 16 bits are kept, so that the place values of the results match the place values of the operands. Rounding keeps as much information as possible about the least significant bits (unused); but since there are no bits less significant than the LSB in integer notation, rounding is not required.

In double-precision calculations, the multiplier-accumulator must be capable of mixing two's complement and unsigned magnitude representations. When a double-precision multiplication is performed, each input word is divided into two parts. Each part of the multiplicand is multiplied by each part of the multiplier, and the partial products are summed to obtain the final result. However, only the most significant words of the multiplicand and the multiplier have sign information. Therefore, inputs that come from the least significant word must be treated as unsigned numbers. In double-precision work, the multiplier-accumulator is much more efficient than previous parts.



4. Word growth occurs when two complex numbers are worked on by a butterfly function (a). The vector magnitude of the two can be as high as $\sqrt{2}$. If two other complex numbers are added to these, the final value can be as high as 2 $\sqrt{2}$, or 2.82 (b).

The chip follows the classic method of rounding, taking the round number nearest the number to be rounded. A one is added to the position to the right of the last rounded digit, and the result is truncated. This provides nearly unbiased rounding. The only sticky point occurs when a prerounded value is exactly halfway between two results. If the full 16 bits of precision are used in each input, the chance of landing halfway between two values is only about one part in 2^{16}, so the remaining bias is only about one part in 2^{17} relative to the LSB of the rounded result.

A flexible control structure

The circuit includes separate lines for each bit in both inputs—16 bits each for the multiplier, X, and the multiplicand, Y. The output totals 35 lines for a total I/O count of 67 pins. Inputs can be individually designated as two's complement or unsigned magnitude, as determined by the TCX and TCY controls.

The output appears in two's complement format if either of the two inputs is in two's complement format or if a subtraction operation is invoked. A single master clock (CLK) with separate enable controls for each of the three sets of registers is provided (ENX and ENY for the input registers, ENP for the product register). As in previous multiplier-accumulators, the accumulator does not have a separate Clear line—that is, an accumulation cycle begins with the Accumulate control line unasserted during the first multiplication. This places the first product in the product register, after which ACC is asserted for the remaining cycles. Similarly, the previous result can be subtracted from the present product by asserting the control line SUB.

The output format can be selected for either integer or fractional notation and the selected result can be rounded if desired. A format adjustment does not affect the number in the



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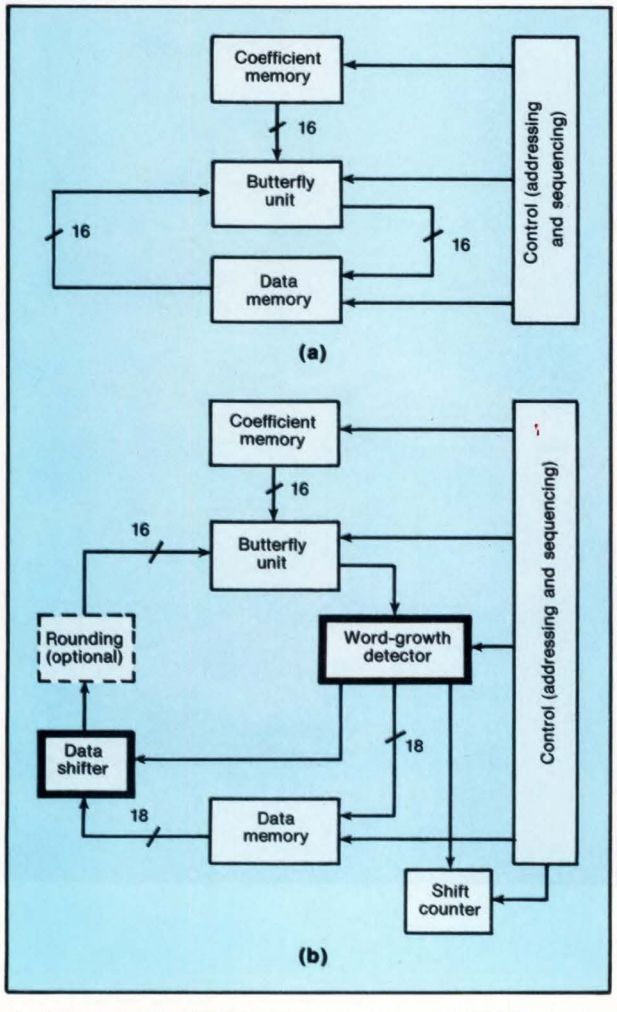
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product register; it affects only the result applied to the output buffers. However, the format adjustment affects the placement of the rounding bit. For example, computing a vector dot product (a sum of products) progresses through four steps:

- Selecting the desired output format;
- Computing the first product with RND, if desired, but with ACC = 0;
- Computing the remaining products with RND = 1 (rounding disabled) and ACC = 1 (accumulation enabled);
- Starting the next dot product at step 2.



5. A fixed-point FFT processor (a) may be converted into a block floating-point one (b) by adding a word-growth detector and data shifter. If word growth occurs on any pass, the inputs to every butterfly are shifted 1 or 2 bits to the right on the next pass.

All outputs are three-state and are controlled by the TSX, TSM and TSL inputs. These control the extended product (XTP), the most significant product (MSP), and the least significant product (LSP), respectively.

The TMC2160's wide output format permits a designer to locate the coefficient binary point anywhere in the field. It is then possible to read out those 16 bits of the product that align with the original 16 data bits, thereby maintaining proper normalization. All bits above the 16 become overflow bits and all those below become guard bits. This is an extension of the right- and left-shifting concept used in fractional two's complement format vs fractional unsigned magnitude notation (binary point left of operand). For integers, the LSP field becomes output, there are no guard bits, and the entire MSP field becomes extension or overflow.

Slowing down word growth

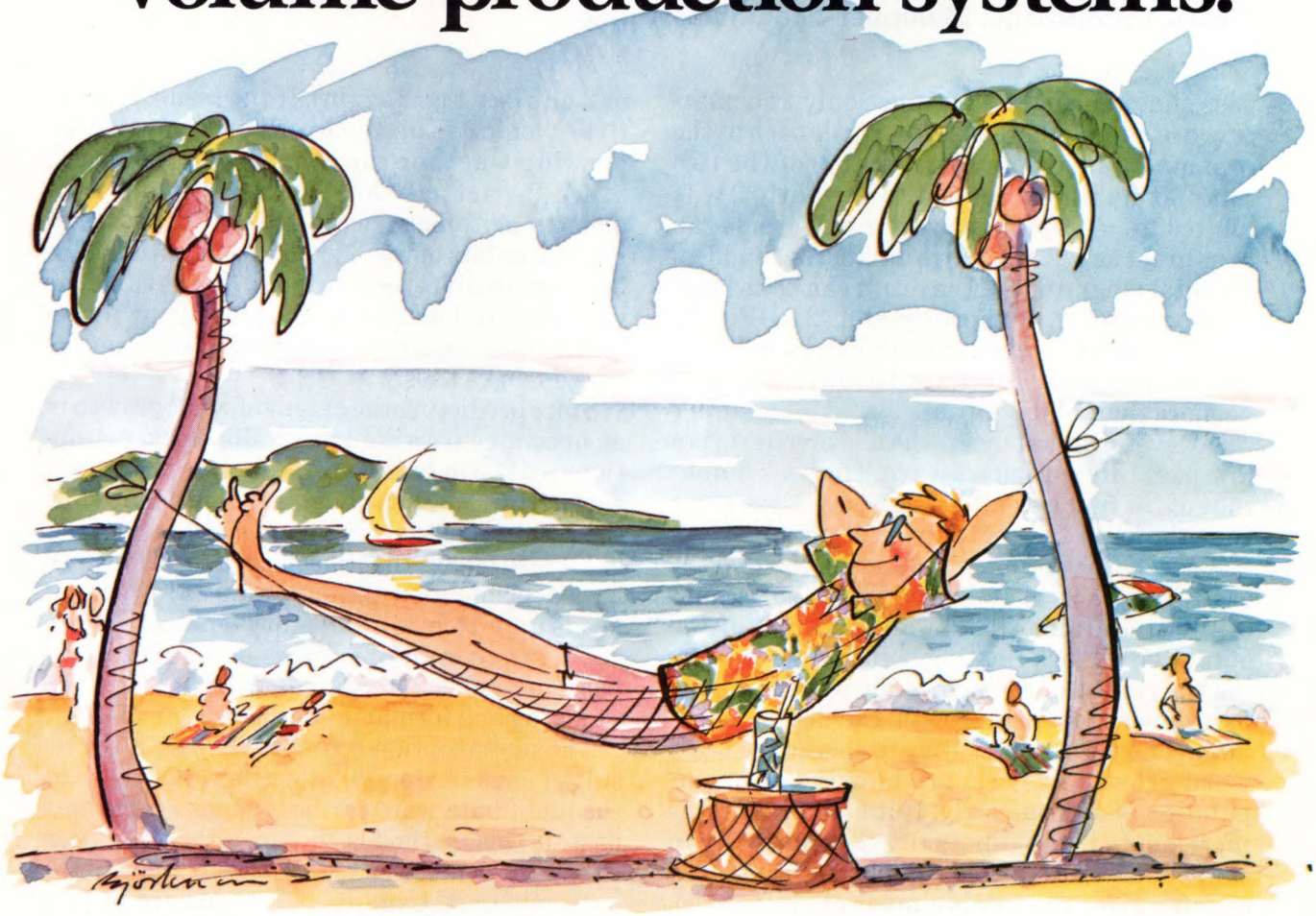
In various forms of the Fourier transform (the FFT and others), the result is the sum of many numbers. If a signal is centered in a frequency bin or is matched to a filter, the result is a sum of many positive numbers. Thus the number of digits increases.

If no extra bits are used to cope with the increase, one of two things occurs: either the FFT analyzer overloads for some input signals or the output signal-to-noise ratio is reduced because of input level restrictions. A way of preventing overload is to divide the results by 2 or 4 at each pass. Unfortunately, every division makes fewer bits available, thereby degrading the output signal-to-noise ratio. The longer the filter or transform, the worse the problem.

One solution to word-growth problems with the FFT is the so-called block floating point, which originates from a careful analysis of the overflow problem. The butterfly operation combines the values of two points with a "twiddle factor" to generate two different points (Fig. 3). Each input value ranges from −1 to +1 if the analyzer operates on normalized numbers.

Seemingly, just one bit of word growth per

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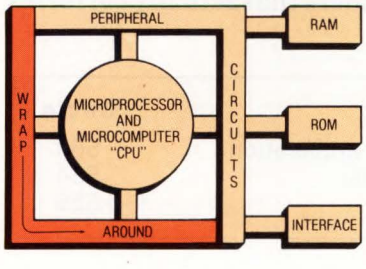


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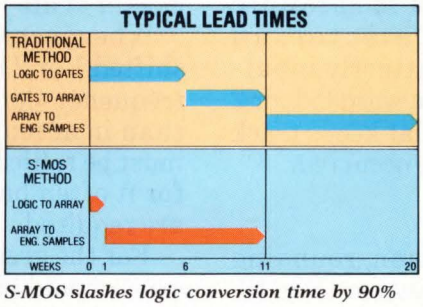
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pass should be necessary since only two numbers are added—but not here. While each of the components (real and imaginary) of the two complex numbers applied to the butterfly is limited to -1 to $+1$, the vector magnitude can be as great as $\sqrt{2}$. Since two numbers are added, the total magnitude of the result can be as large as two times $\sqrt{2}$, or approximately 2.82 (Fig. 4). This means that word growth can be 0, 1, or 2 bits at each pass. Total word growth averages no more than 1 bit per pass.

A waveform that meets the above criteria is a low-pass filtered square wave. The peak amplitude of the fundamental is significantly greater than the amplitude of the overall signal.

A block floating-point operation for FFTs is easily implemented with the TMC2160 because of the simultaneous availability of all of the output bits. Block floating point works by storing the results of each butterfly with two extra bits allowed for word growth. During the calculation of a pass, the results are checked to see if word growth has occurred during the computation of any butterfly. If it has, a counter is incremented, and inputs to every butterfly in the next pass are shifted right by 1 or 2 bits. The counter gives the total number of shifts used, thus preserving information about the scale of the output results.

To implement this algorithm in hardware requires a word-growth detector; an 18-bit-wide data memory; a butterfly input-data shifter that shifts the entire word 0, 1, or 2 bits to the right; and circuitry that keeps track of the number of shifts that have occurred.

Rounding for precision

To obtain the greatest precision, rounding circuitry can be added to the system (Fig. 5). Since information shifts in a data-dependent manner, the rounding-bit location also shifts. This location is the one to which a logic 1 is added before truncation.

Word growth or overflow into the extended product (XTP) can occur in a positive or negative direction and can be either one or two bits. It is caused by a carry into the extended product if in the positive direction and a borrow from it if in the negative direction. If the result is positive, a logic 1 is placed in either the P_{32} or P_{33} bit position, depending whether the growth was 1 or 2 bits (see Fig. 2 again). If the result is negative, a logic 0 is placed in either P_{32} or P_{33}, depending whether the growth was 1 bit or 2. Since P_{34} acts as the sign bit in two's complement arithmetic, word growth has occurred if all three bits of the XTP are not identical. The bit that is different indicates whether the growth was 1 or 2 bits. The word growth detector must retain the largest growth that occurs during a pass.

Since predicting the extent of word growth in an upcoming pass is an impossible task, two options exist: Go back and recompute the pass if word growth occurs, but this time down-shift the results. Not only is this method inefficient, but it also makes the time needed to perform an FFT dependent on the data input. However, it needs only 16 bits of memory—not a big concern, since memory chips are quite inexpensive—and supports the TMC2160's built-in rounding and format adjustment controls.

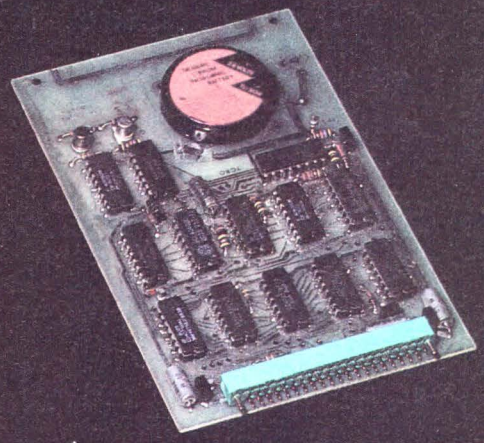
The second option is to store 18 bits of the result of each butterfly, selecting 16 of these as the input data word for butterflies on the next pass. If this method is chosen, a three-position data shifter must be placed at the input to the butterfly unit. Usually, it is composed of four input multiplexers. The scale factor selection should be changed only at the beginning of a pass, if at all.

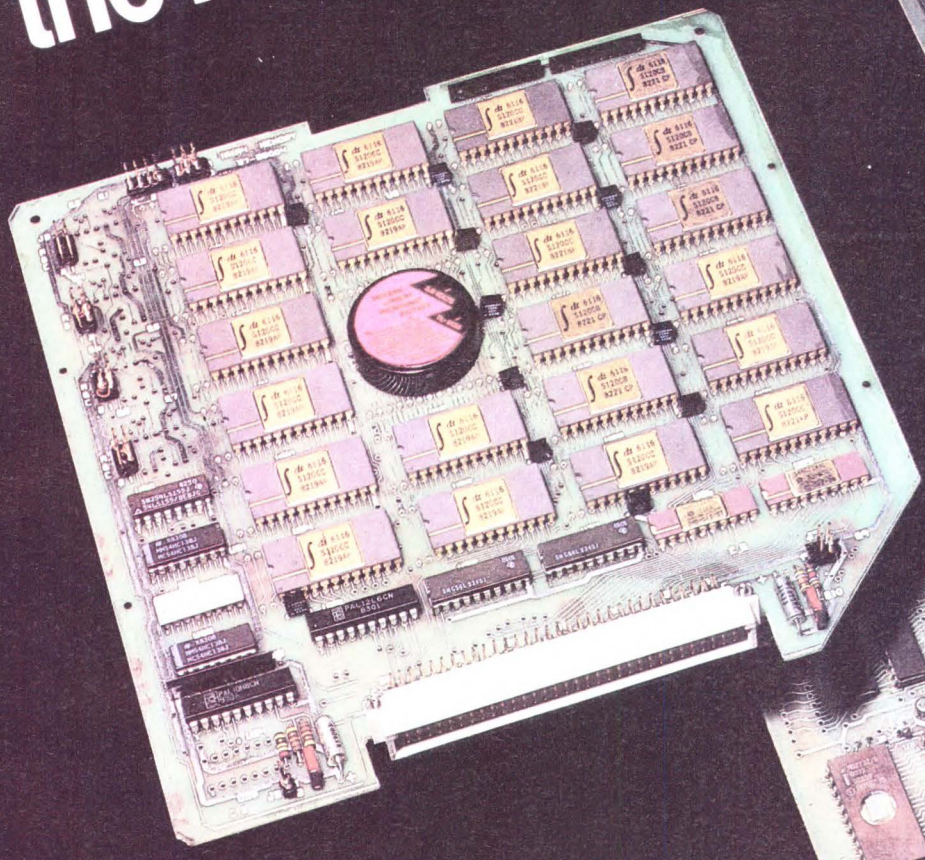
Whenever word growth occurs, all data is shifted 1 or 2 bits to the right. Because of this, frequency-domain amplitudes appear smaller than in actuality. The number of downshifts must be tallied to keep track of the scale factor, for it often happens that absolute amplitudes are required.

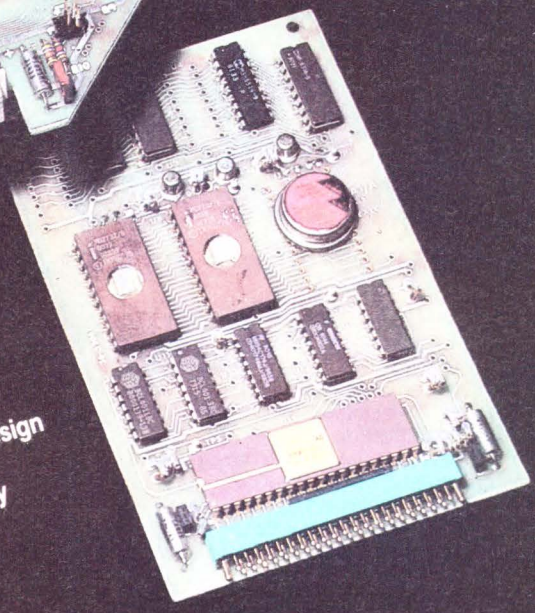
For the greatest accuracy, the results of each pass should be rounded rather than truncated. But which 16 bits will be selected cannot be determined until a pass is completed. Thus the numbers must be rounded before reaching the butterfly section, with the data shifter's output applied to a set of adders that actually performs the rounding.□

How useful?	Circle
Immediate design application	553
Within the next year	554
Not applicable	555

Here's to the memory







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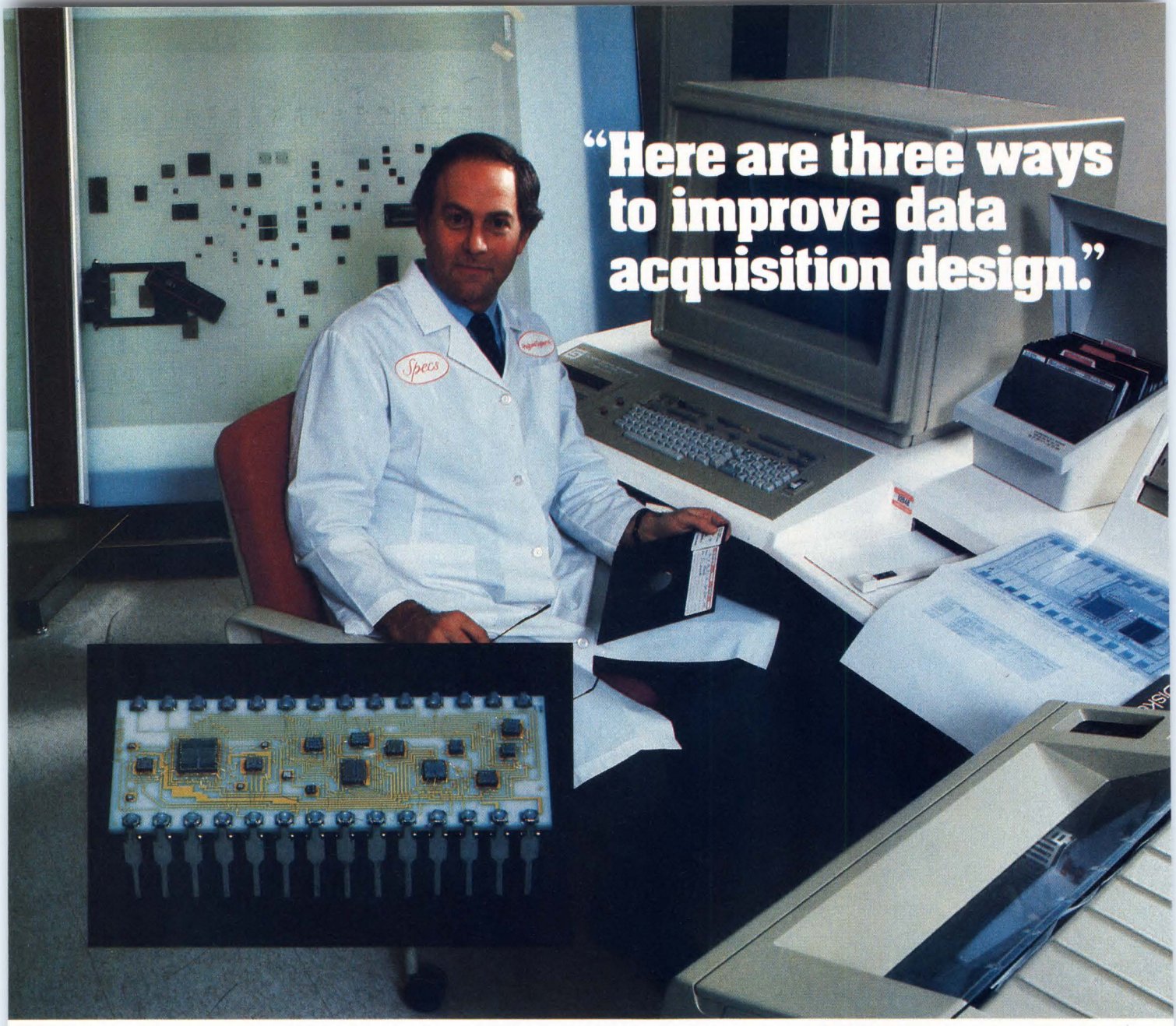
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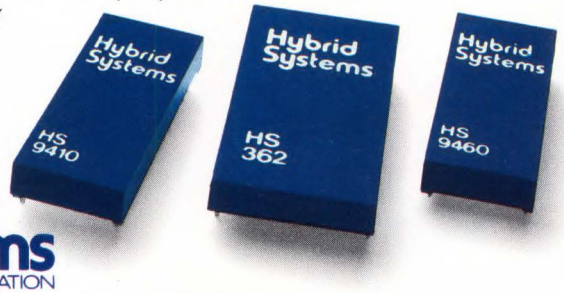
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CIRCLE 79



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With built-in specialties CMOS microcontrollers take aim at diverse tasks

Designers need not spend time completing their systems with extra devices. A chip from a microcontroller family may well incorporate most of the necessary circuits.

CMOS microcontrollers are rapidly rising to new challenges in factory and office automation, portable telecommunications, and other areas that demand functional integration and extremely low power consumption. Their software is generally compatible with that of standard CMOS microprocessors, yet special software enhancements and some extra hardware features increasingly target the microcontrollers for specific purposes.

With today's sophisticated microcontrollers, designers can breathe more easily. No longer need they waste time choosing separate chips to enhance addressing, memory, I/O, and timing capabilities. Many chips incorporate some if not all of those functions, and others supplement them with built-in custom circuits.

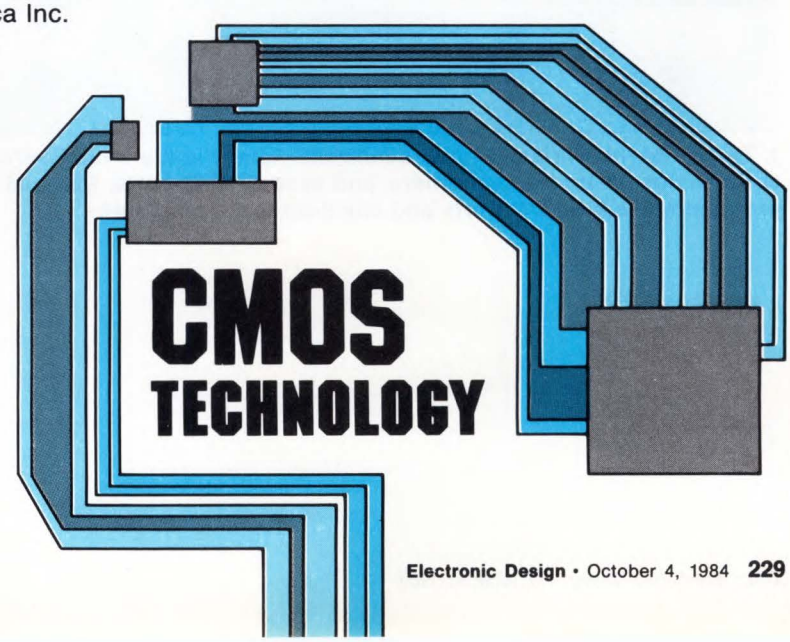
Packing more special functions than normally expected, the Series 740 of 8-bit CMOS microcontrollers is geared specifically for low-power systems that can sacrifice neither functions nor board space. All boast a powerful instruction set that, when combined with such on-chip circuits as serial I/O ports, a UART, analog-to-digital converters, and high-voltage output ports, make them ideal for many different systems. Furthermore, since all of the chips reside in shrink DIPs or flat packages, they occupy up to 50% less board space than conventional packages.

The instruction set of the 740 series is upwardly compatible with that of the familiar 6502. It holds 69 machine-language instruc-

I. Saeed, Mitsubishi Electronics America Inc.
N. Yamauchi, Mitsubishi Electric Corp.

Iftikhar Saeed serves as an applications engineering manager for Mitsubishi's microprocessor products in Sunnyvale, Calif. Before joining the company last year, he developed local-area network controllers at Advanced Micro Devices. Saeed has a BSEE from the University of Peshawar in Pakistan and an MSEE from the University of Tennessee.

Naoki Yamauchi is a senior engineer at Mitsubishi Electric, near Osaka, Japan. For nine years he has worked with microprocessor designs, concentrating now on CMOS controllers. He holds a BSEE from Osaka University.

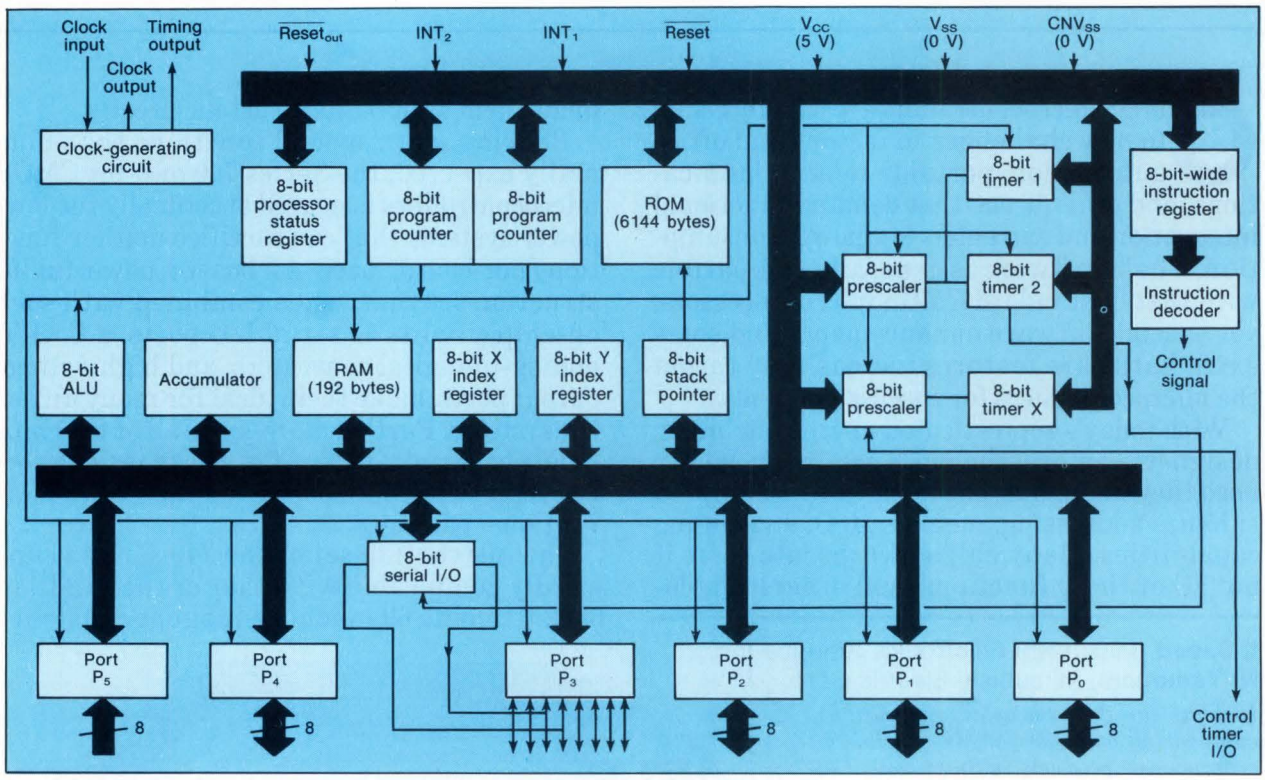


tions and responds to 17 addressing modes. Various entries manage and manipulate bits in the accumulator, the memory, or the I/O ports. Still another address indexes for table references. Arithmetic, logic, and decimal operations proceed between memory locations and I/O ports or between I/O ports directly—without passing through the accumulator.

Support available

Development support for the microcontrollers comes from cross-assemblers and dynamic debugging tools that run on the IBM PC personal computer, Intel's microprocessor development systems, or all computers using the CP/M-86-based operating system. Low-cost emulator boards and piggyback chips can be had for trial programming.

Examining one microcontroller in the 8-bit family lays sufficient groundwork for understanding how the remainder of the series can fit into high-performance, low-power designs. The M50745 contains 6 kbytes of mask-programmable ROM, 192 bytes of RAM, three 8-bit interval timers, a built-in serial I/O port, five 8-bit programmable parallel I/O ports, and one 8-bit input port (Fig. 1). Designed with a 3-μm n-well silicon-gate CMOS process, the microcontroller operates with a V_{CC} of 5 V, dissipating only 6 mA maximum (at 4 MHz) in the



1. Typical of the Series 740 microcontroller family is the 8-bit M50745, which has 6 kbytes of ROM, 192 bytes of RAM, three 8-bit interval timers, and assorted I/O ports. External communication is handled through five programmable 8-bit I/O ports and one 8-bit input-only port.

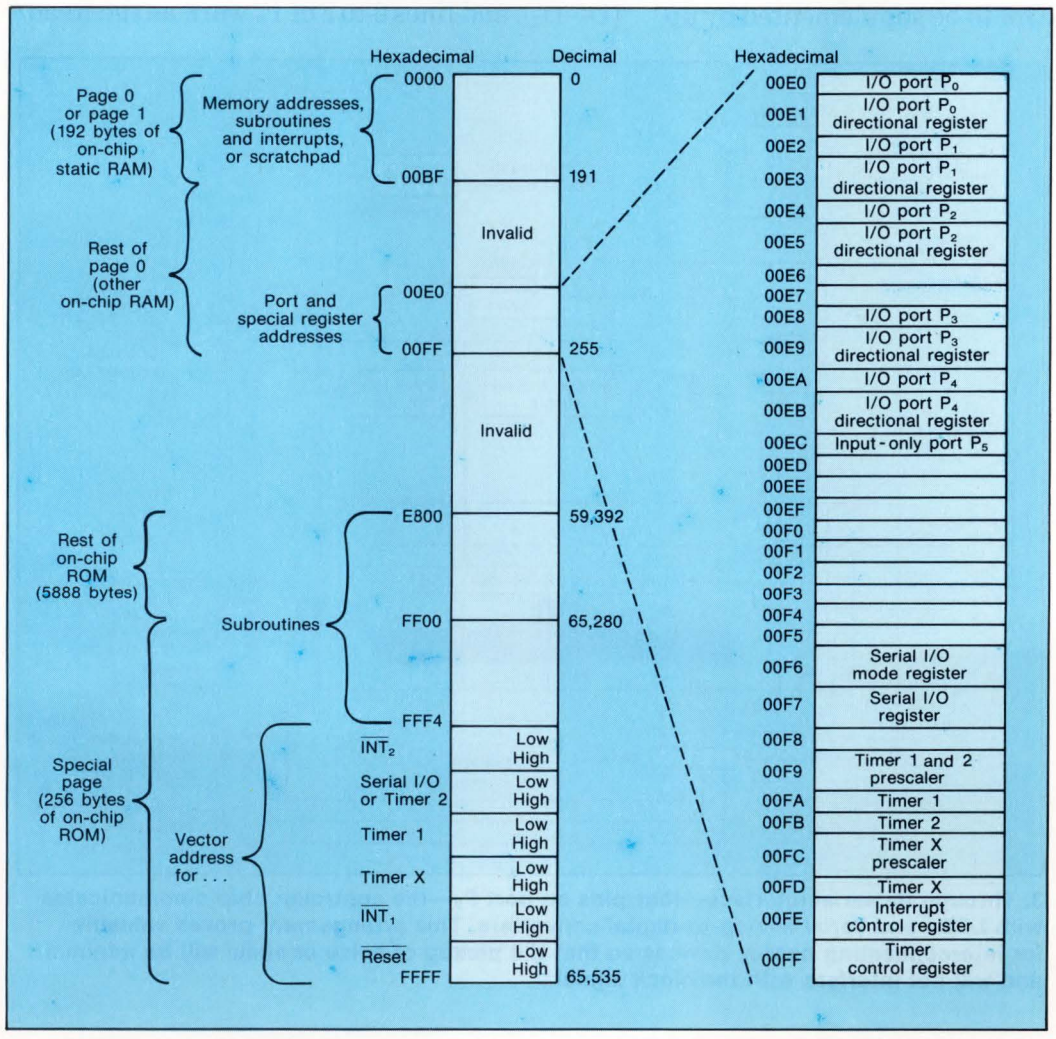
active mode and just 10 μA on standby. A low-voltage version uses a V_{CC} of 3 V $\pm$10% and consumes one-third the current of the 5-V version. Each version is housed in a 64-pin shrink DIP or a 60-pin flat package and is fully software-compatible with all other members of the series.

Register and memory space

The microcontroller addresses ROM, RAM, I/O ports, and special registers through the same memory map. The total memory area is nominally 64 kbytes. The first and last 256 bytes are address spaces called, respectively, page 0 and the special page (Fig. 2).

Page 0 is accessed through the zero-page addressing modes plus two-word instructions. The last 32 bytes of the page hold the addresses of all I/O ports, timers, and special registers. The first 192 bytes of the page hold internal RAM addresses and occupy the on-chip static RAM. Since this RAM is also used as the stack area for subroutines or interrupt calls, it is in fact selectable to either page 0 or page 1.

The special page is reached similarly—that is, by using the special-page addressing modes plus two-word instructions. Its last 12 bytes (words) hold reset and interrupt-vector addresses. Its other 244 bytes hold subroutines. The special page is stored in the last 256 bytes of



2. A memory map identifies the addressable ROM, RAM, I/O ports, and special registers in the microcontroller. The map contains the actual addresses that access each area within the chip.

address space $FF00_{16}$ through $FFFF_{16}$, which occupy the on-chip ROM, organized as 6144 words by 8 bits.

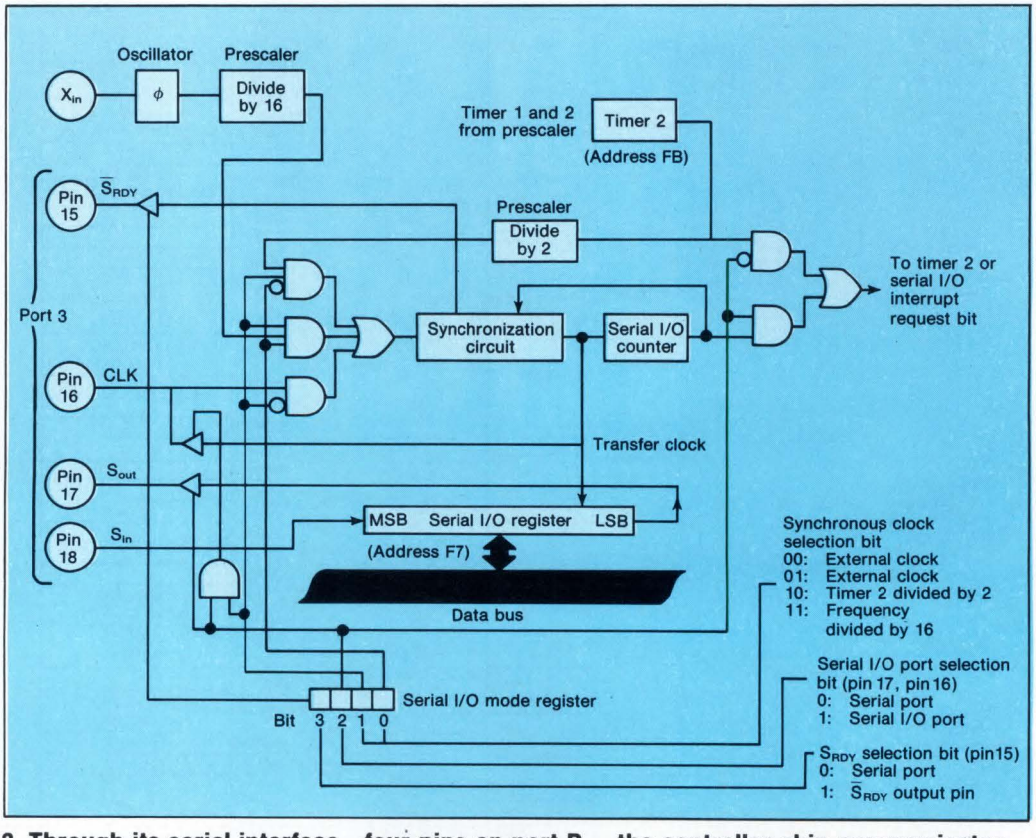
Reaching full potential

In addition to its potential as a single-chip microcomputer, the M50745 can be programmed as a microprocessor or as an expanded memory-based microcontroller system. The processor mode flag—bits 0 and 1 of address $00FF_{16}$—sets altogether four operating modes.

When that flag reads 00, the M50745 starts in the single-chip mode after being reset, and ports P_0 through P_3 function as I/O ports. For the memory expansion mode, the flag is set to 01 and the CNV_{SS} pin is tied to V_{SS}, allowing the on-chip 6-kbyte ROM to be supplemented by up to 64 kbytes of external memory. (The CNV_{SS} pin helps program the chip for different operating modes.)

For the evaluation chip mode, the flag is set to 11, and 10 V is applied to the CNV_{SS} input pin. In this state the chip's internal memory is disabled by forcing all instructions fetches to use external memory. This mode is useful for evaluating a program before committing it to the final ROM code.

Finally, in the microprocessor mode, the controller can be programmed as a microprocessor by connecting the CNV_{SS} input to V_{CC} and programming the processor mode flag to logic 10. In this mode, ports P_0 and P_1 are used as the 16-bit address bus, P_2 becomes the data bus (D_0–D_7), and lines 0 to 2 of P_3 work as the Read/



3. Through its serial interface—four pins on port P_3—the controller chip communicates with LCDs and serial analog-to-digital converters. This arrangement proves valuable for interconnecting nearby devices so that the pickup of noise or skew will be minimal and will not interfere with the clock signal.

Write (R/W), Sync, and Ready (RDY) signals. (The original functions of these three I/O ports are lost—except for the input functions.)

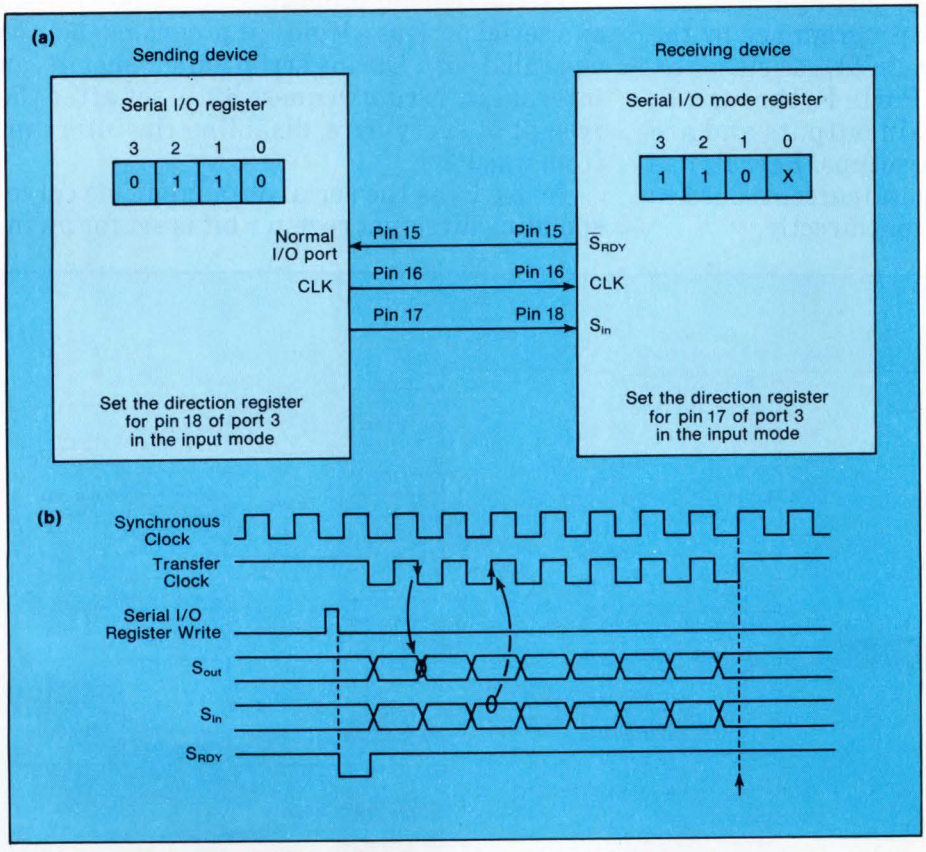
The M50745 supplies a variety of timing and counting functions through its timer 1, timer 2, and timer X. The 8-bit counter-timers have reload registers and prescalers (timer 1 and timer 2 use the same prescaler). All three timers count down with 8-bit latches. The timer latch is reloaded immediately after the counter reaches zero. The address space $00F9_{16}$ through $00FD_{16}$ is allocated to the timers and prescalers.

Timer X works in four different ways, as determined by the two mode-selection bits (bits 2 and 3 at address FF_{16}) of the timer control register. In the timer mode, the oscillator frequency (one-sixteenth the clock frequency) is counted, the interrupt request bit is set, and the timer contents are reloaded when the timer reaches a count of zero. In the pulse output mode, the M50745's control (CNTR) pin is programmed as an output, whose level is inverted each time the timer reaches a zero count.

The event-counting mode is the same as the control timer mode, except that the microcontroller's CNTR pin supplies the counted input. In the final mode, the timer can measure the pulse width (the time between low levels) of any input to the CNTR pin.

Interrupt control

Six sources may interrupt the microcontroller. All are vectored interrupts, and their priorities are fixed by the chip's internal logic. How-



4. When port P_3 acts as the serial data input, a bit in the direction register that corresponds to a particular line is programmed as an input (set to logic 0) and the devices are connected as shown (a). The Synchronous Clock signal can be taken from either an internal or external source (b).

ever, various priority schemes can be executed with the interrupt control registers (address FE_{16}) and the timer control register (address FF_{16}). The M50745 interrupt control has a request flag, an enable flag, and a mask flag, which controls the efficiency of the interrupt. All the flags can be handled by the chip's bit-manipulation instructions.

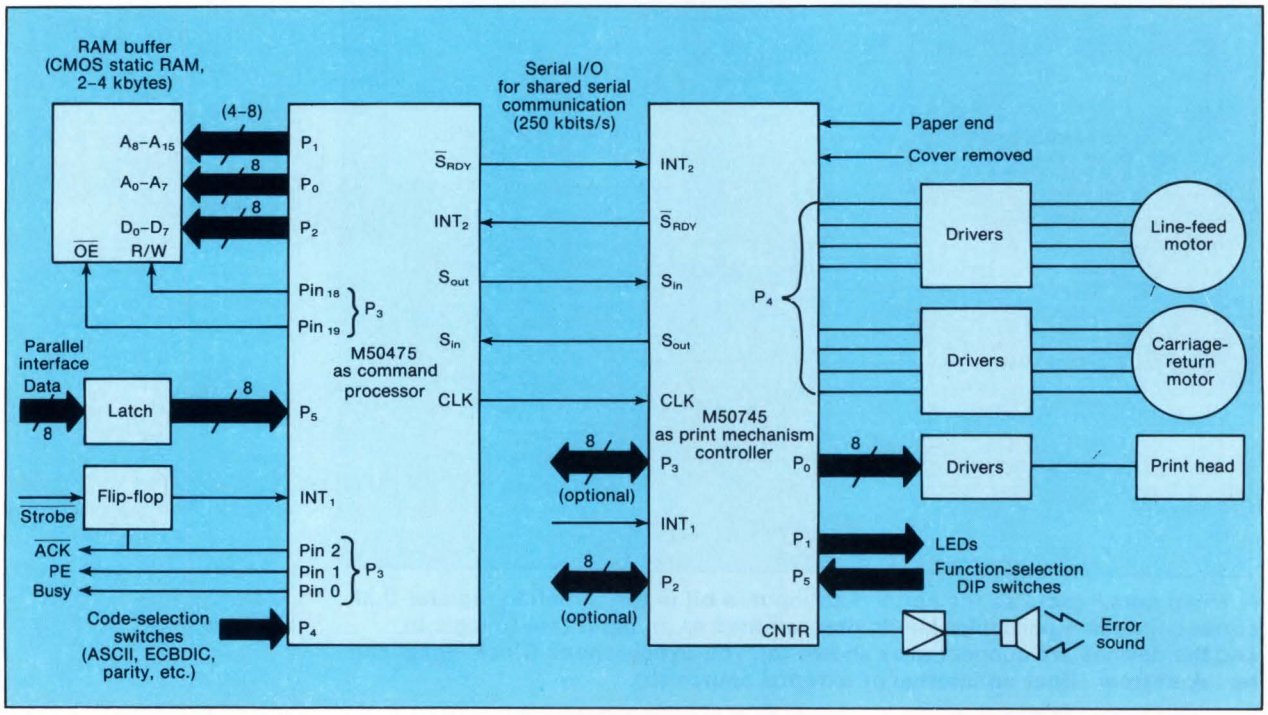
Exits and entrances

Like the other 740 microcontrollers, the chip has a broad selection of I/O facilities, including five parallel ports (P_0 through P_4) and one input-only port, P_5. A direction register assigned to each port configures the individual bits for input or output. The M50745's memory-mapped I/O is assigned to the last 32 words of page 0 (Fig. 2 again). For example, port P_0 is accessed at address $E0_{16}$ and can be programmed by the direction register at address $E1_{16}$ as either an input or an output port. Ports P_0 through P_3 have n-channel open-drain outputs and are suitable for current-sink setups. Port P_4 has p-channel open-drain outputs (current sources) that can drive npn transistors directly.

The chip's simple serial interface exchanges information with such devices as LCD drivers, serial analog-to-digital converters, and master-slave peripherals. As a three-wire synchronous serial interface (Fig. 3), it needs separate wires for data and clock signals. The interface generally interconnects devices in proximity with one another, usually on the same pc board. (Distances must be restricted, otherwise noise or skew might interfere with the clock signal, resulting in a loss of synchronization.)

Four pins of port P_3 constitute the serial interface: Serial Data Input (S_{in}), Serial Data Output (S_{out}), Synchronous Clock (CLK), and Serial I/O Ready ($\overline{S}_{RDY}$). The serial I/O function is configured by a 4-bit serial I/O mode register (address $F6_{16}$). When set to logic 1, bit 2 of the I/O serial register programs four pins of port P_3 as a serial port; as a logic 0, it programs them as a parallel port. During serial data transfers, an internal interrupt request bit is set after the receipt of every byte, disabling the interrupt from timer 2.

To use P_3 as the serial data input, its corresponding direction register bit is set for an in-



5. Two chips are pulled into duty controlling a dot-matrix printer. One acts as the command processor, decoding host commands, arranging data into a page format, and placing it in a page buffer. The second microcontroller runs the print mechanism, supplying the details needed for the printing actions.



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put (logic 0). Bit 3 of the serial I/O register allows P_3 to be used as a normal I/O port or as an output for $\overline{S}_{RDY}$, which goes low after the data flows to the serial I/O register (Fig. 4a).

A low level on $\overline{S}_{RDY}$ means that the chip is ready to receive external serial data (Fig. 4b), and it goes high at the next falling edge of the transfer clock. The synchronous clock can be selected from either an external or an internal source, with the internal one derived either from a programmable rate selected from timer 2 or from a 250-kHz clock derived from the internal 4-MHz oscillator.

Power down and standby

The M50745's two power-down modes are controlled by software. The first mode stops only the clock to the internal logic and the chip's CPU and is programmed by the Wait instruction. When Wait is executed, the internal clock stops on a logic high. The purpose behind halting only the clock is to allow an immediate restart, since the oscillator is left running and needs no start-up time.

In the second option, initiated by the Stop instruction, the oscillator stops and the entire system falls into a standby (quiescent) state. When Stop is executed, the internal oscillator halts in the high state and the values FF_{16} and 01_{16} are loaded into prescaler X and timer X, respectively. Also, the clock (internal oscillator frequency divided by 16) is forcibly connected to the prescaler, a connection that is cleared when timer X overflows or the system is reset.

Mastering a dot-matrix printer

A dot-matrix printer demonstrates how the M50745 and other microcontrollers in the family can simplify the design and boost the efficiency of a peripheral. Like any other printer controller, it must handle several disassociated operations; thus it draws heavily on its extensive I/O capability, its versatile timer system, and its on-chip ROM.

The printing algorithm resides in the chip's 6-kbyte ROM, as do the dot-pattern tables. The memory-mapped I/O structures—plus its 192 bytes of RAM, its page 0 and page 1 stacks, and its bit-manipulation instructions—lend extra flexibility to the control programming. In addition, the three programmable timers, a six-level priority interrupt structure, and the 48 I/O ports combine to make the chip ideal for controlling the dot-matrix printer.

Many sophisticated printers today incorporate multiple processors for handling commands, text and graphics, and the print mechanism. For this application, two microcontrollers do the jobs (Fig. 5). The command processor not only transfers data between the host CPU and the printer but also decodes the commands, arranges the print data into a page format, and places the data in a page buffer. The other chip actually coordinates the printing action, controlling both the stepper motors for the horizontal print head and paper feeder and the operator control functions.

The command processor talks to the host through a conventional Centronics interface, with port P_5 serving as an 8-bit data bus and with port P_3 (bits 0, 1, and 2) and INT_1 handling handshaking signals. The RAM buffer stores about a page of data (2 to 4 kbytes). If the printer needs more buffer space, the upper bits of port P_1 can be decoded to address a larger RAM area.

Port P_4 of the printing-action controller drives the stepper motors through line drivers, and ports P_1 and P_5 control LED monitors and DIP switches that select functions. Both chips communicate directly through the software-efficient serial interface. Together they have 12 kbytes of program ROM and 384 bytes of RAM—ample space for an on-chip control program.

Since each M50745 contains three 8-bit timers, timer 2 on each chip is assigned the serial I/O functions, leaving four on-chip timers free for other duties. Two of those timers serve as the main units for the dot-matrix printer, one controlling the stepping speed of the printer carriage and the other looking after dot density and positioning. The final two timers work with the host-printer interface, or generate a real-time clock during automatic power-down of the printer.□

How useful?	Circle
Immediate design application	556
Within the next year	557
Not applicable	558

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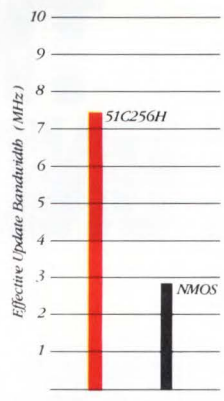
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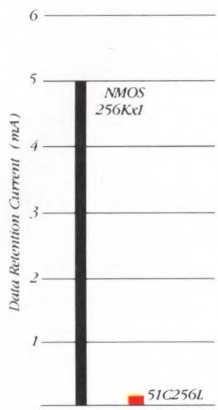
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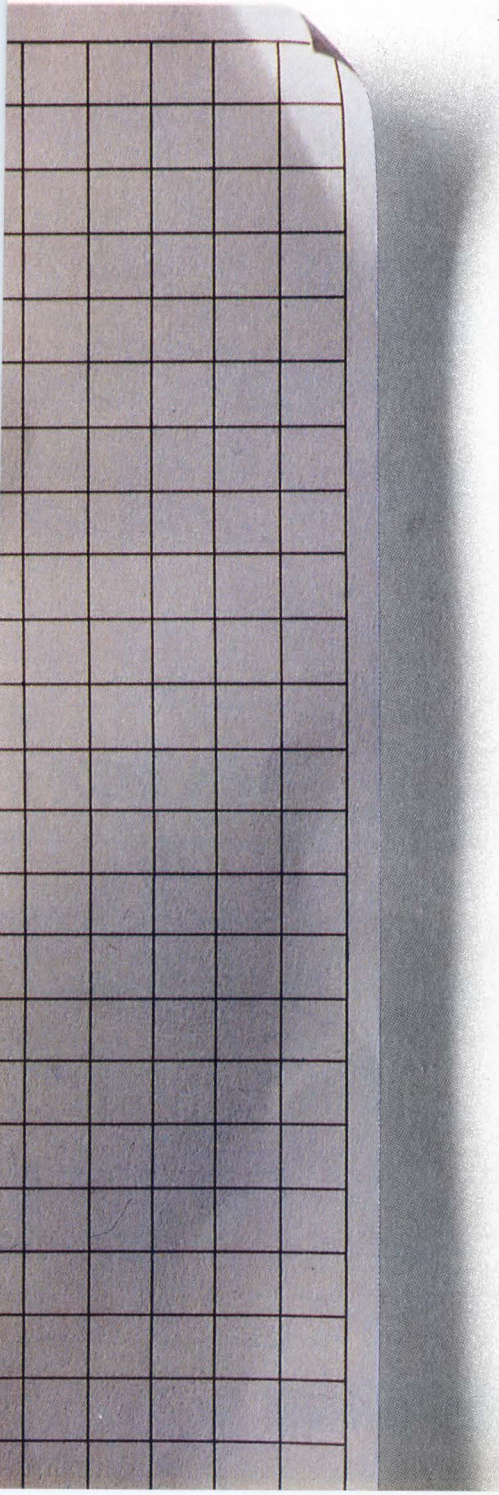
The 80C51 is based on Intel's revolutionary CHMOS technology. Achieving the high performance and high integration of HMOS, with the low power advantages of CMOS.

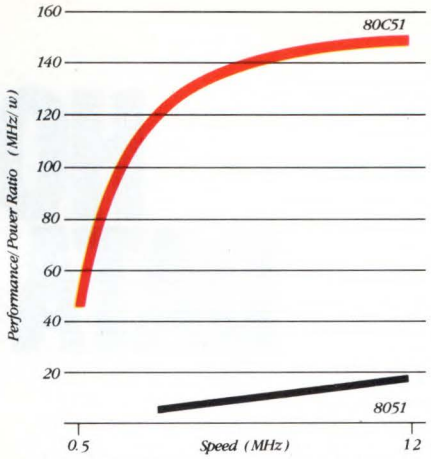
The result is an 8051 pin-compatible microcontroller with the most powerful eight-bit CPU and the highest level of integration available. The 80C51 runs on an incredible 11mA at 8MHz clock frequency. Average power dissipation can be lowered into microamp range, by using one of two new software programmable power control modes. In the power down mode, current drain is 50 microamps.

On the performance side, the 80C51 has a maximum clock rate of 12MHz. The fastest data throughput of any CMOS microcontroller.

Its high integration capabilities include 4K byte ROM and 128 byte RAM, a Boolean Processor able to manipulate 256 individually addressable bits, a versatile serial port and a pair of 16-bit counter/timers.

All this helps to make the 80C51 ideal for high end eight-bit applications ranging from hand-held instruments

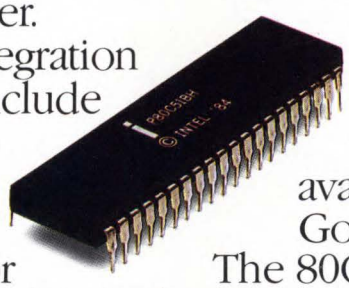




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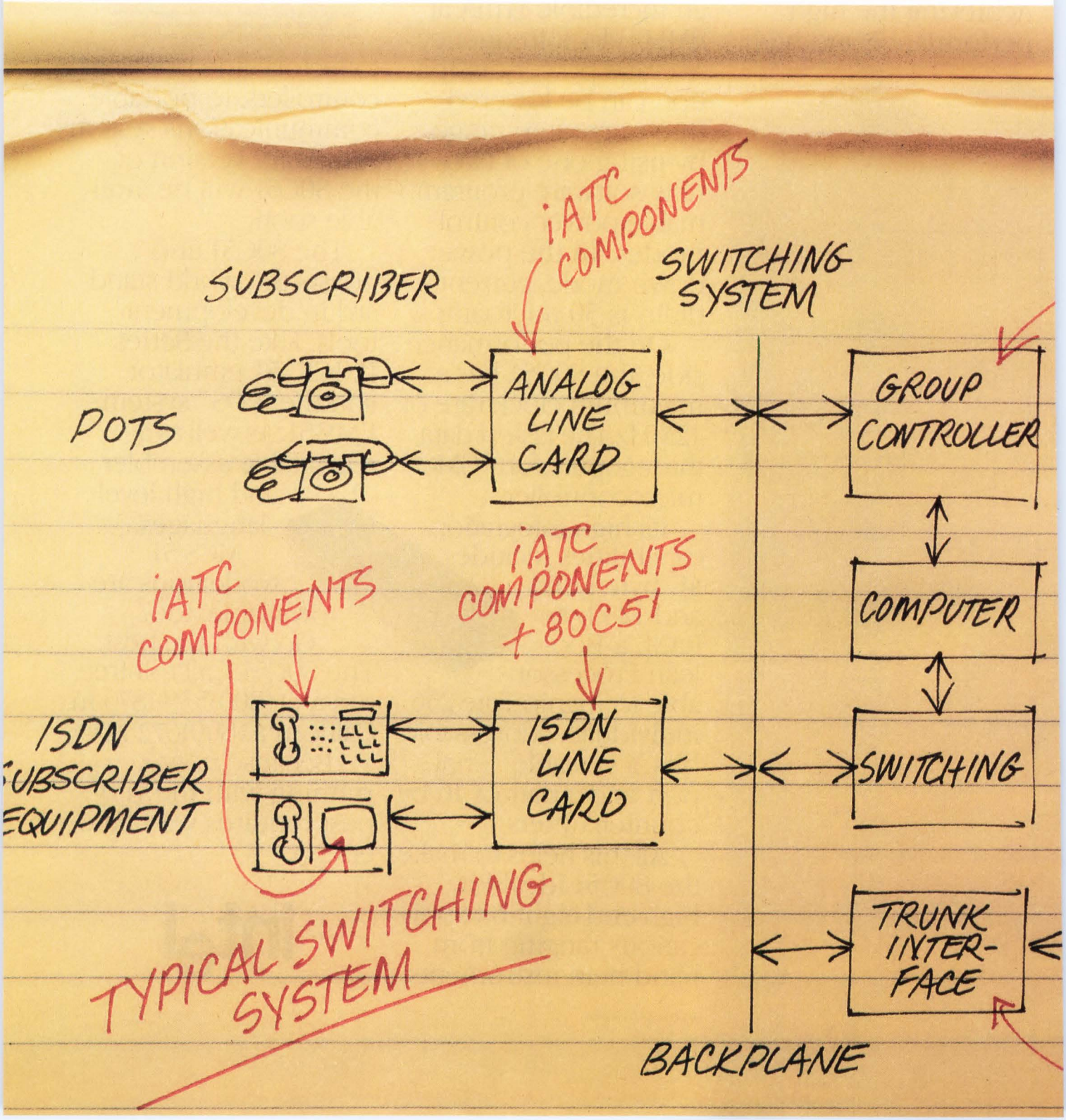
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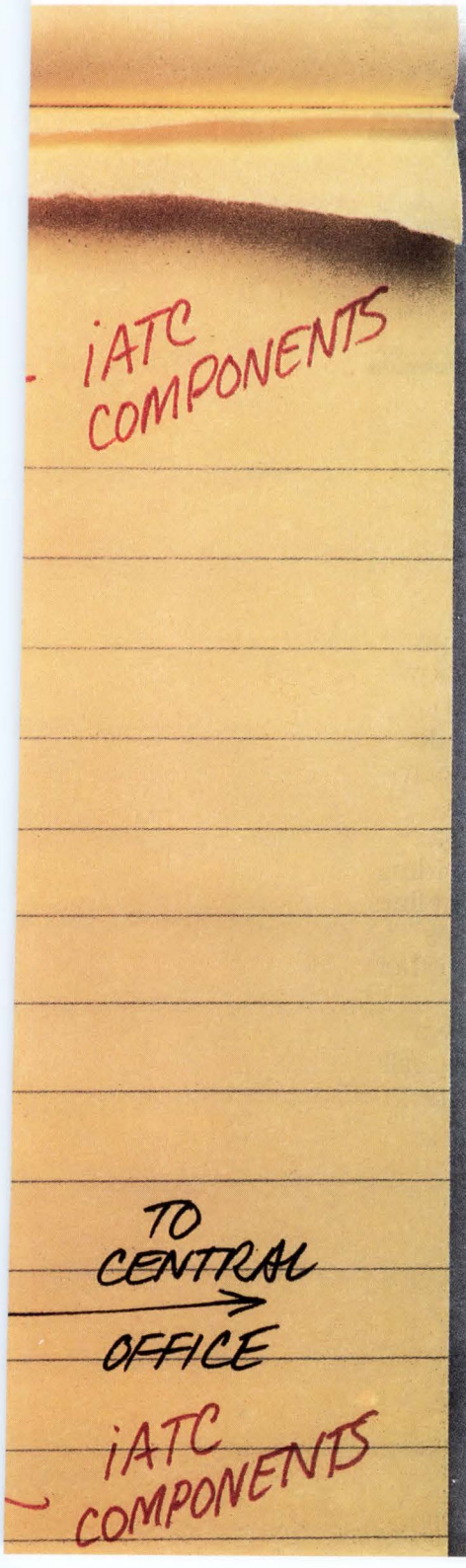
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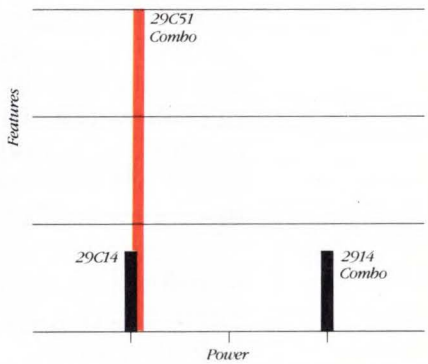
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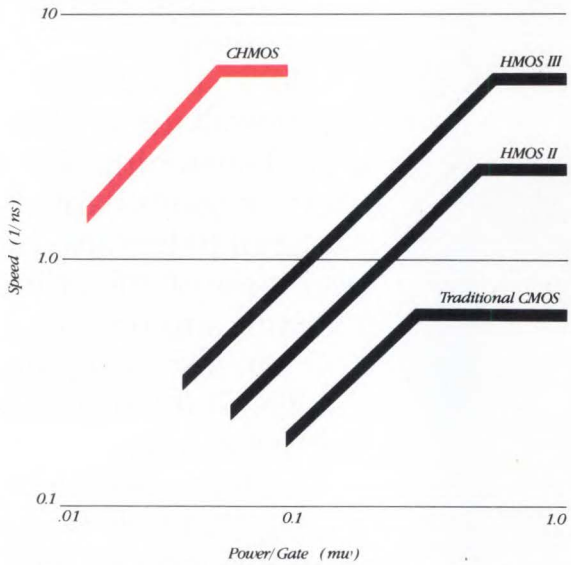
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Dense static RAM speeds data access in memory-intensive systems

Because slow RAM won't do in graphics and other fast signal-processing jobs, dense static devices are making a bid to replace more sluggish dynamic parts.

Fast static RAMs are far from unseating dynamic RAMs in all memory applications. In digital signal-processing, however, where high performance does not take a back seat to other design goals, their speed is very appealing, particularly in conjunction with their lower power consumption.

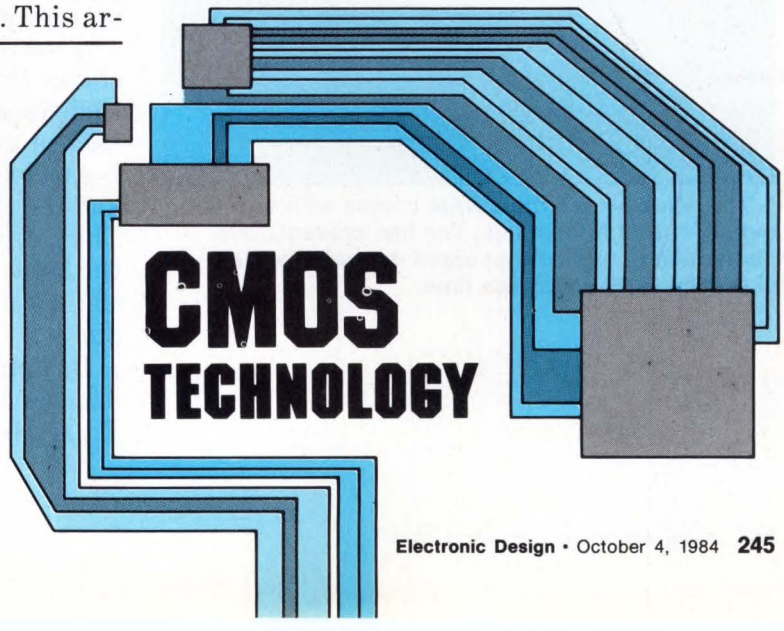
A new, very fast 64-kbit static RAM slashes access times to just 35 ns and reduces power consumption to 100 mA active and 20 mA standby. The mixed technology of its fabrication process, UltraMOS, combines the speed of an NMOS memory array with the low power consumption of a CMOS periphery. The nibble-wide 16k-by-4-bit organization also helps conserve power at the system level.

The RAM's data pins each function as either inputs or outputs, matching the bidirectional data buses of MOS microprocessors. This arrangement saves the microprocessor bus from having to demultiplex for memory devices with separate I/0. Because of the RAM's fast access times, an Output Enable ($\overline{OE}$) line has been included to prevent problems with bus turnaround, select, and deselect timing, as well as system skewing. Those problems can be troublesome in pipelined or interleaved system architectures. Contributing still further to system productivity, the RAM includes a bulk-write mode and uses a standard JEDEC pinout.

While fast static RAMs always benefit writeable control storage, cache, high-speed buffer memories, and the local memory of bit-slice microprocessors, the new RAM's bit capacity is high enough to present attractive alternatives to dynamic RAMs in high-performance bit-

William H. Righter
Lattice Semiconductor Corp.

William H. Righter, as technical marketing manager for Lattice Semiconductor, is responsible for the CMOS static RAM, EEPROM, and CMOS multiplier product lines. He is also developing the architectural specifications for the Portland, Ore., company's second-generation memory products. Previously, Righter worked as a senior applications engineer at Intel, specializing in CMOS dynamic RAMs. He has studied computer engineering at the University of Portland.



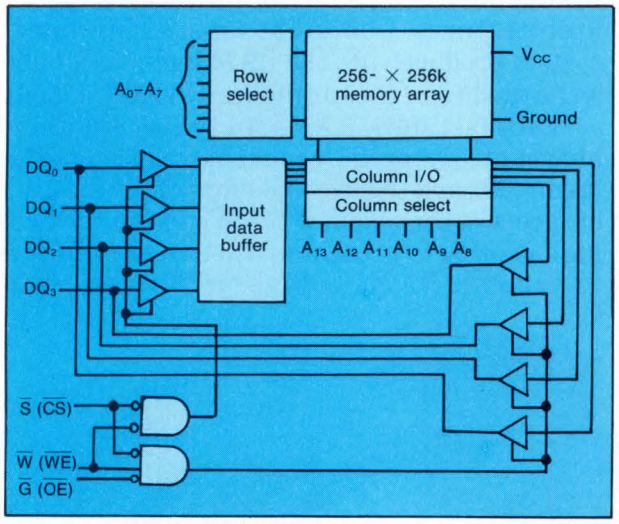
CMOS Technology: 16k-by-4 CMOS static RAM

mapped graphics displays. Its 16-kbit-by-4-bit organization is the right depth and width, and its fast cycle times provide the bandwidth required by such graphics systems. In addition, the static RAM comes in leadless chip carriers that permit construction of high-density modules for such memory-intensive applications.

Besides graphics, other demanding roles are open to the static RAM in array processing, radar and sonar systems, speech recognition and generation, and digital filtering. The memory's 35-to-45-ns accesses provide a good bandwidth match to the new high-speed 45-ns multipliers being developed for digital signal-processing systems.

With or without $\overline{OE}$

The RAM comes in two versions (Fig. 1): one with an Output Enable line (SR64E4) and one without (SR64K4). Access and cycle times range from 55 to as short as 35 ns—more the result of proper circuit design and device layout than any complex technology. However, because the design is optimized for speed, no low-power CMOS standby mode is specified. Yet the standby power consumption is 110 mW when the inputs and internal clocks are not in transition. In contrast, maximum power use is about 550 mW when the RAM is active.



1. The 16k-by-4-bit static RAM comes with or without an Output Enable line. The line prevents bus contention problems that could degrade the device's 35- to 55-ns access time.

Address transition detectors reduce the device's access time without compromising low-power performance. A rather recent innovation, the detectors operate despite address skews, slow rise and fall times, high-frequency transitions, glitches, and non-TTL or floating levels on the inputs. Also cutting access times are single-sided row decoders and bit-line-equilibrated, high-gain sense amplifiers.

An internal substrate bias generator allows 5-V operation, affords greater tolerance of negative overshoots on the inputs, and improves access times by reducing stage delays due to bulk silicon capacitance.

The Output Enable line is included in the output buffer to avoid bus contention and thus preserve fast access times. This feature is typical of many high-performance memory systems, permitting them to take advantage of a common-I/O RAM's speed. It is especially important for banked, interleaved, or pipelined systems, where skews, bus turnaround time, data buffering, and multiplexing prevent system cycle times from approaching device cycle times.

Bus contention occurs in an interleaved memory architecture (Fig. 2a). Because the data on the first device remains on the bus for some finite period after the device is deselected, data may overlap with that of the next selected device. Such contention causes considerable system noise by coupling current spikes through the V_{CC} line. For this reason, pipelining is not feasible and extra time must be added between cycles, thereby stretching the effective system cycle time (Fig. 2b).

A second control line—Output Enable—solves the bus contention problem. With two such lines (Fig. 2c), device cycles can run back to back or even slightly overlap. The overlap time is approximately the difference between the $\overline{CE}$ and the $\overline{OE}$ access times of the device, or 15 ns. Thus, consecutive reads can be pipelined with the help of the Chip Enable line while access to the bus is controlled through the Output Enable pin.

Bus turnaround is also difficult to accommodate within the cycling time frame of a 35-ns RAM. Here, too, the $\overline{OE}$ helps. Contention oc-

curs during a write cycle when there is insufficient time to switch the direction of the data bus before the read data arrives from the device output buffers (Fig. 3a). The data, however, must be held valid until the trailing edge of the write- OR Chip Enable ($\overline{CE}$) signal. The only alternative to a $\overline{CE}$-controlled part is increasing the system cycle time.

If a RAM is equipped with an Output Enable pin, back-to-back or overlapping pipelined cycles can occur (Fig. 3b). Controlling $\overline{OE}$ during a read cycle makes it possible to generate an early $\overline{CS}$ to start an internal data access. Then, a properly timed Output Enable signal will activate the data output buffers when the bus is available.

By-4 benefits

In addition to the Output Enable function, the 64k RAM benefits from its 4-bit-wide organization, which lets it add memory to a system in 16k increments. The advantages are clearest in the wide, shallow memory organization typical of mainframe processor cache or local memory, as well as in writable control storage.

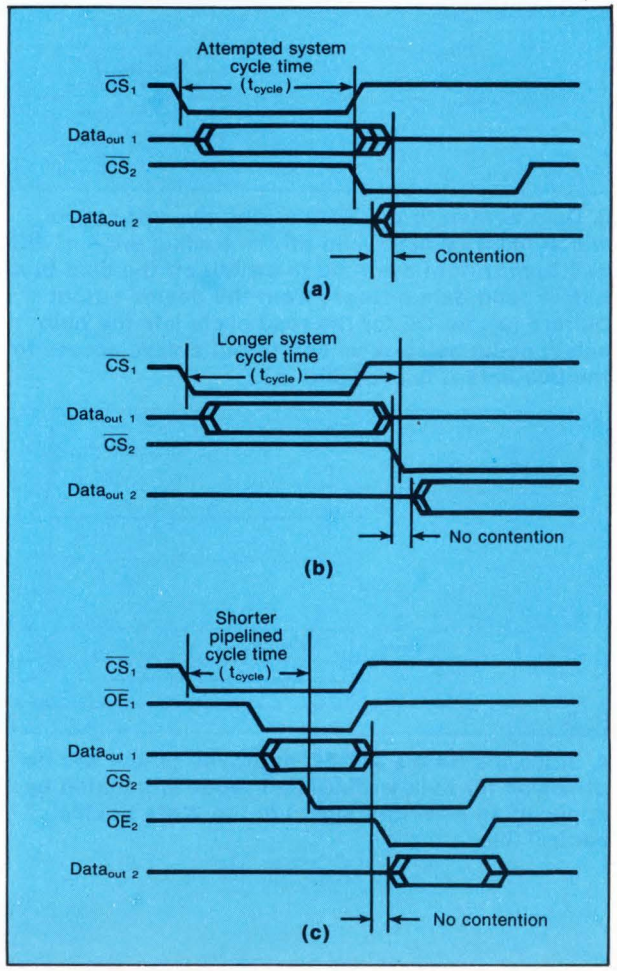
Memory arrays using 16k-by-4-bit static RAMs consume much less power than similar systems built with 64k-by-1 devices. The by-4 architecture means that for any given word width, fewer devices are selected and consume power. For example, a 64k-by-64-bit memory system built with 64k-by-1-bit RAMs consumes 2.5 times as much power as the same array built with by-4 devices, assuming both RAMs have similar I_{CC} characteristics. In general, the wider the word width, the greater the power savings.

The by-4 device is also the better choice for systems where circuit board real estate is at a premium. A by-1 system needs extra space for two separate input and output buses as well as an extra pair of address lines through the memory array. In addition to preventing a dense board layout, the by-1 RAM may actually mandate the use of a more costly multilayer pc board.

The bulk-write mode

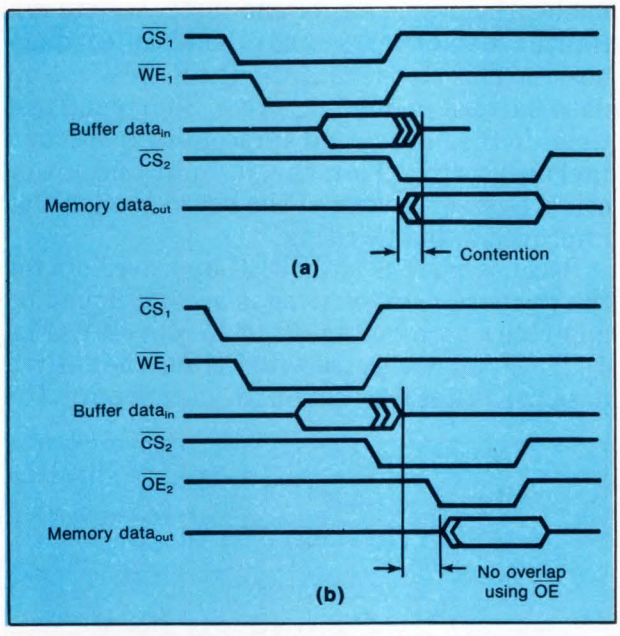
For the manufacturer or for incoming-test and quality-assurance groups, the bulk-write mode provides an easier and faster way to initialize a memory array and to conduct test diagnostics. This mode initializes the RAM to a 4-bit data pattern in one 1-μs cycle. Shortened test times in the factory and at incoming inspection increase production throughput and lower costs. System testing at the board level is also improved by bulk writing.

Because there is no JEDEC-approved pin for the purpose, bulk writing is accomplished by applying a high-voltage (8-to-15-V) to $\overline{WE}$ (Fig. 4). The RAM is selected with $\overline{CE}$ and the desired data pattern is then set on the data inputs. The

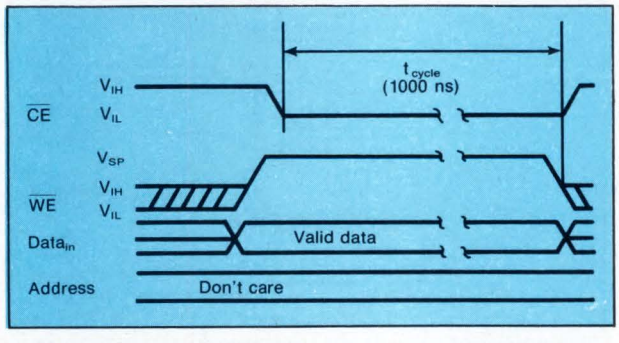


2. Bus contention results when data from one deselected RAM remains on the bus for some time after another RAM is already selected. Data overlap is the result (a). Adding time between cycles solves the problem but stretches the effective cycle time (b). A second control signal from the Output Enable pin allows back-to-back operation of devices without contention (c).

CMOS Technology: 16k-by-4 CMOS static RAM



3. Data written to the RAM during the write cycle, which must be held valid till the trailing edge of $\overline{WE}$ or $\overline{CE}$, may not have time to switch off the data bus before read data appears from the device output buffers (a). An $\overline{OE}$ for the read cycle lets the chip select occur as early as before but delays access to the bus until it is available (b).



4. Since the RAM's JEDEC-approved pinout has no provision for bulk writing, that mode is initiated by applying an 8-to-15-V signal to the Write Enable control line.

pattern must be held valid for 1 μs. If the data is altered at any time during the writing cycle, a new cycle begins, and the 1-μs timing period starts from that point.

Although intended primarily for testing, there are other useful system applications for the bulk-write feature. For example, very rapid screen clearing or background color painting is possible when the RAMs store displays in a bit-mapped graphics system.

The performance advantage of fast memory initialization is maintained even in memory systems that perform parity checking. Some multiuser operating systems, such as Unix, also require rapid clearing of user-allocated memory space before allowing access to the memory. Other benefits are cache-memory clearing and computer self-diagnostic routines, working more quickly with the one-cycle bulk-write mode.

The static RAMs show their performance edge especially well in three-dimensional imaging systems, such as computer-aided design stations used in machine design.

Large amounts of high-performance memory are required in the bit map and, to a lesser extent, in the display list (Fig. 5). Also, small yet fast storage is needed within the image processor itself. Without it, bottlenecks can develop between the display list and the image processor or within the image processor itself. Moreover, operations on the random-access side of the bit map suffer because high data rates on the display side can absorb memory bandwidth, thus limiting the vector generator's updates.

The display list occupies a dual-port configured RAM that stores the three-coordinate end points of each display vector. The RAM also provides a communication channel between the main processor and the image development circuitry, or graphics engine. Together, the three system parts must handle a highly animated display—perhaps a detailed engineering diagram of a machine part as it rotates, spins, or moves rapidly across the screen. That level of movement requires a worst-case image update rate of 16 frames/s, not to mention sufficient display-list RAM to store a complex image of 100,000 vectors.

Six words are required to transfer one vector

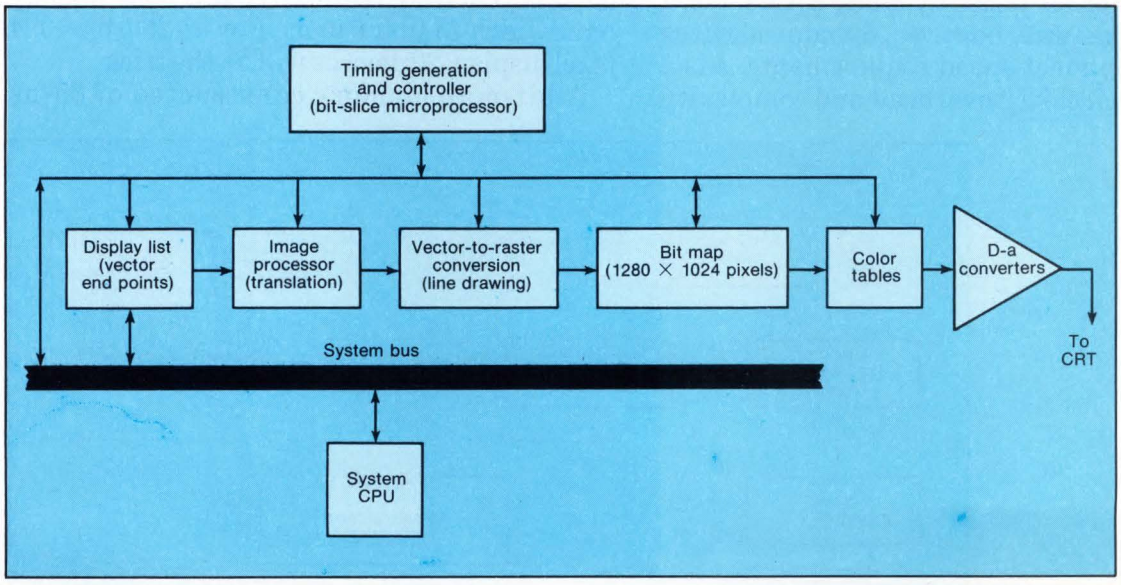
from the display-list RAM. Processing a complete image 16 times/s mandates a 9.6-MHz rate, or a 104-ns cycle time, on just one side of the dual port. For best performance, the system processor should have asynchronous access to the other side of the dual port. That implies that the RAM should cycle twice as fast as the rest of the system and also allow overhead time for access request arbitration and system skews. To meet those combined performance specifications, a 35-ns static RAM is needed.

An image processor's demand

The image processor transforms displayed images—that is, it moves an image from one place to another; rotates or turns an image about one of the three dimensional axes; scales, or sizes an image up or down in each coordinate direction; clips, or cuts an image to fit on a display; and, in a process called perspective transformation, projects all visible points of a 3D image onto a plane, usually the display screen (Fig. 6). All such transformations require some pixel data processing, which in turn involves a data array or matrix multiplication to translate data on a vector-by-vector basis. A matrix multiplication may also be needed to change global coordinates to the clipping coordinates of the viewing system.

Because of the large number of multiplications, transformation processing is a very time-consuming step in image display. Even high-speed bit-slice circuitry can noticeably slow system performance when multiplication is performed in software. To minimize delays, a CMOS multiplier-accumulator with a 45-ns multiply time should be used as the core of the processor.

Linked to the multiplier are several shallow memories that temporarily store partially pro-



5. Three-dimensional imaging systems require considerable amounts of fast RAM for the bit map, display list, and image processor.

cessed image data, matrix coefficients, and output data. Because the multiplier cycles at the system level in less than 70 ns, fast RAM is needed to provide matching data storage. The wide, shallow organization of the l6k-by-4 RAM makes it a good fit with the l6k-by-16 organization of the memory bank. Also required is a FIFO at the input of the image processor in order to uncouple input data bursts from the display list memory and thus eliminate stage-to-stage synchronization.

The bit-map is a large (1280-by-1024-pixel) 3D memory array in which final image data is stored. Systems of this size are commonly eight bit planes deep to simultaneously display 256 colors. More than 1.3 Mbytes of memory are required for such a system.

Implementing the bit map

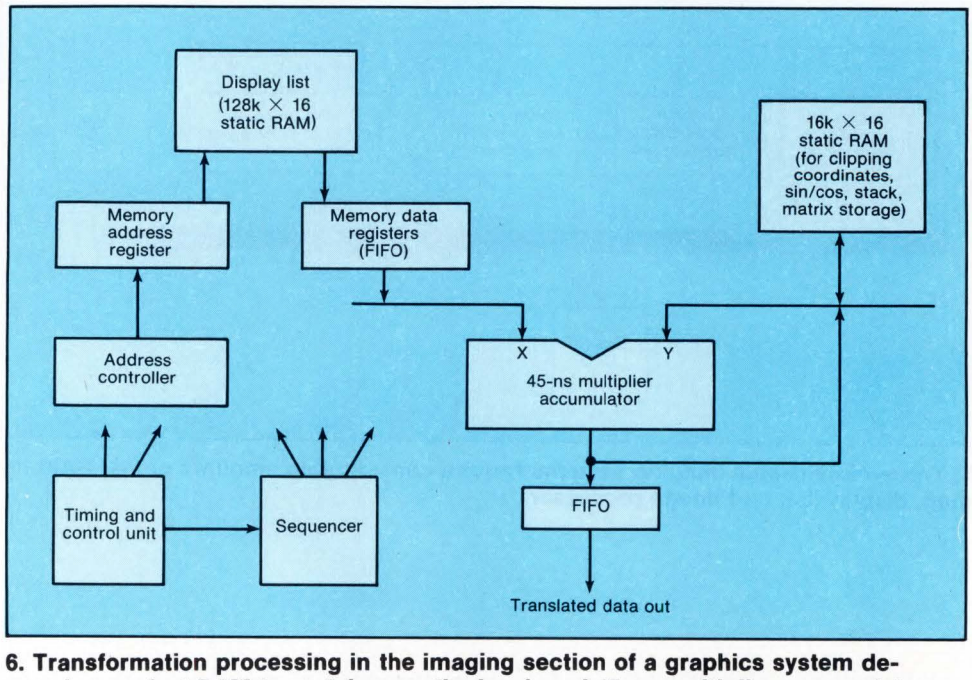
To fill this tall order, graphics designers usually opt for bit-dense dynamic RAMs. For a display of that size, however, dynamic devices do not easily meet speed requirements. Also, the control circuitry overhead and complexity typically impinge on performance as well.

The bit-map specification and the blanking times of the display monitor determine the speed requirements of the memory system. Thus, for a 1280-picture-element-by-1024-line display operating at 60-Hz frame rate, each frame requires 16.667 ms. The total blanking time is the combined vertical and horizontal blanking intervals times the number of lines. For instance, a 650-μs vertical and a 5.4-μs horizontal interval take 6.18 ms just for blanking.

That figure, subtracted from the 16.667-ms frame time, leaves 10.49 ms to display 1,310,720 pixels, or 8 ns/pixel. The inverse of that number—125 MHz—is the instantaneous bandwidth requirement of the display memory in the bit map.

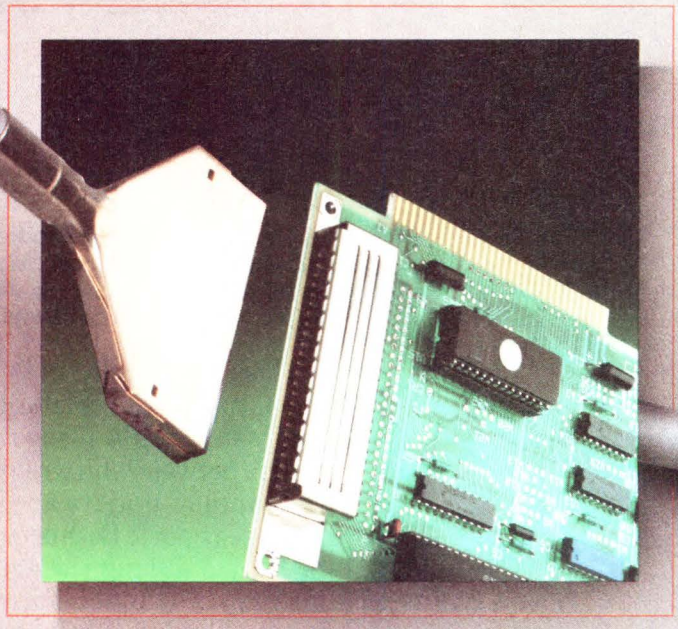
That appears to be beyond the cycling capability of a 35-ns RAM. However, connecting 16k-by-4 RAMs in parallel (Fig. 7) reduces the device cycle time required to meet the display bandwidth to just 640 ns. For a 1280-by-1024 pixel display, 20 devices will do the trick.

A bit-map memory constructed of 35-ns



6. Transformation processing in the imaging section of a graphics system demands very fast RAM to match recently developed 45-ns multiplier-accumulators.

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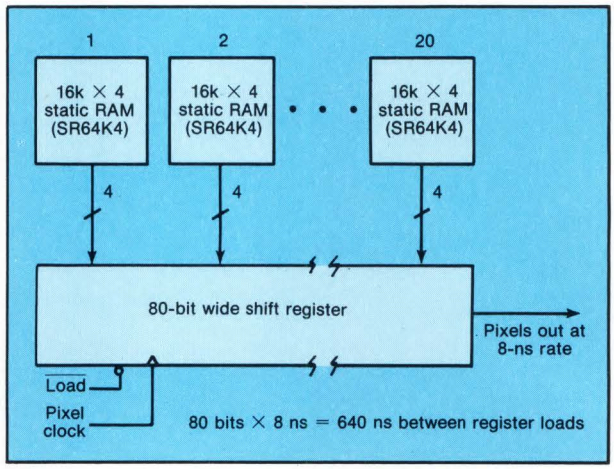


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CIRCLE 85

16k-by-4 CMOS static RAM



7. Device cycle time is reduced by connecting 16k-by-4-bit RAMs in parallel. For a 1280-by-1024-pixel graphics display, 20 devices are required to meet the 125-MHz bandwidth requirements.

RAMs can be cycled in 70 ns at the system level. An output shift register can then be loaded using just a single 70-ns memory cycle; the 570 ns left between shift-register loads can be used for random update accesses from the image processor port. Because the register need only be loaded during the actual display time, the bit-map is available for random updating during the blanking periods.

The maximum number of pixel updates must be determined to get a measure of the bit-map performance. Dividing the 6.18-ms composite blanking time by the 70-ns cycle time yields 88,285 updates during the blanking period. Also, 8 updates can occur between each of the 16 shift register load cycles per line, for a total of 128. Multiplying 128 by the 1024 displayed lines yields 131,072 possible updates during the display time.

Combining the two update numbers and multiplying by the 60-Hz frame rate shows 13.16 million updates per second. If the vector-to-raster line drawing circuitry produces pixels at a maximum 100-ns rate, the frame buffer provides an adequate bandwidth with a comfortable margin.□

How useful?	Circle
Immediate design application	559
Within the next year	560
Not applicable	561

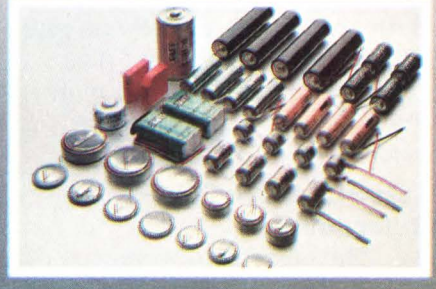


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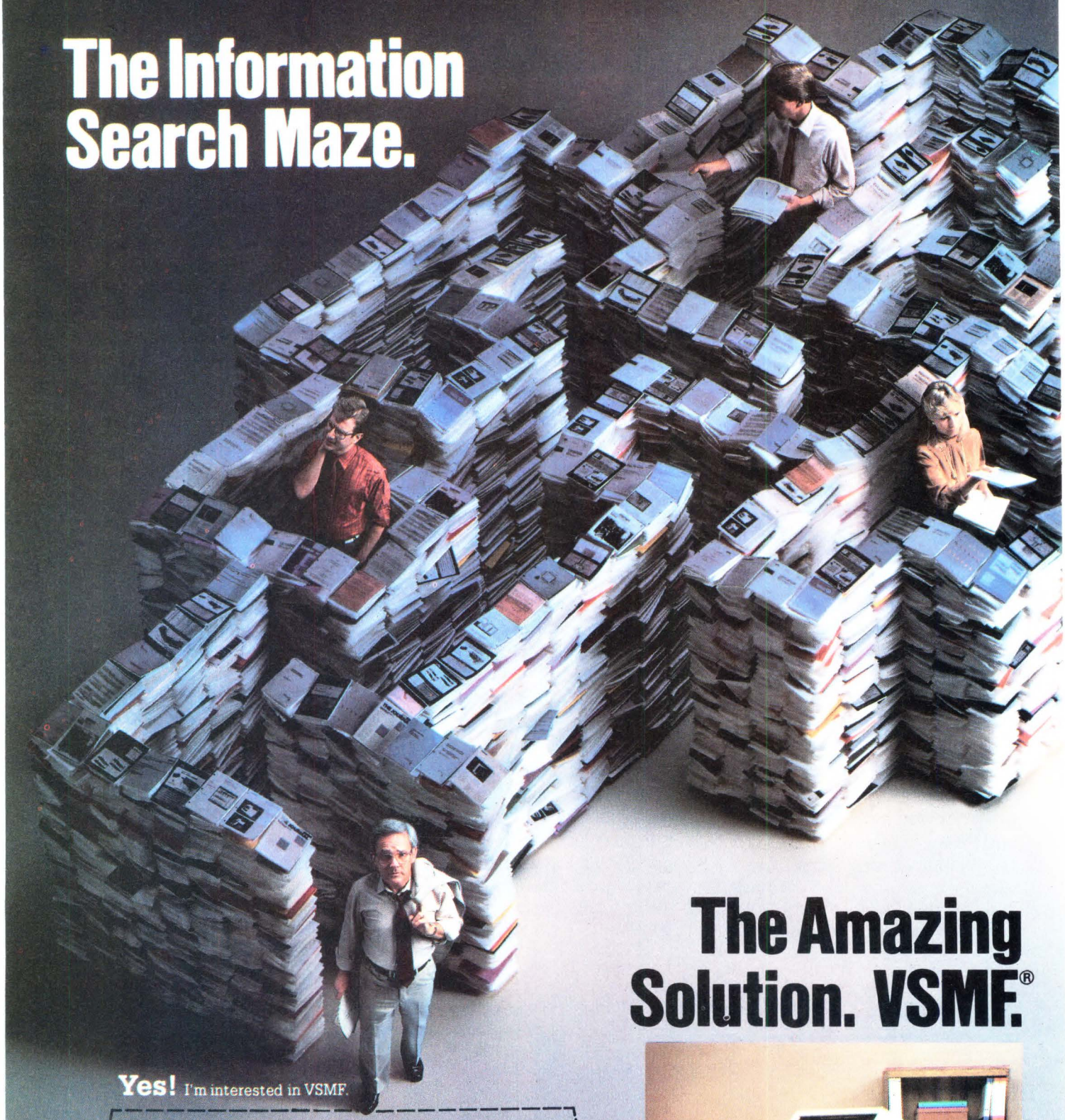
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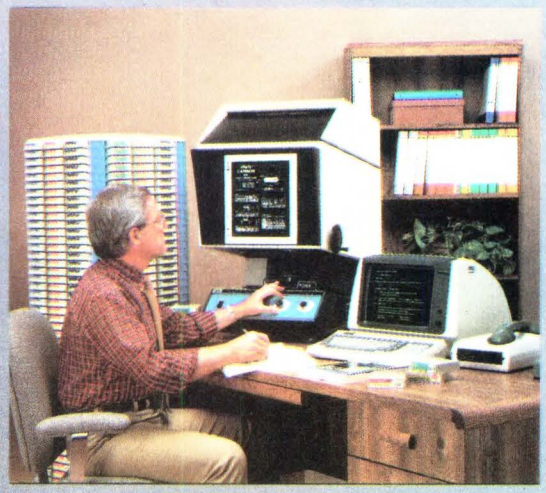
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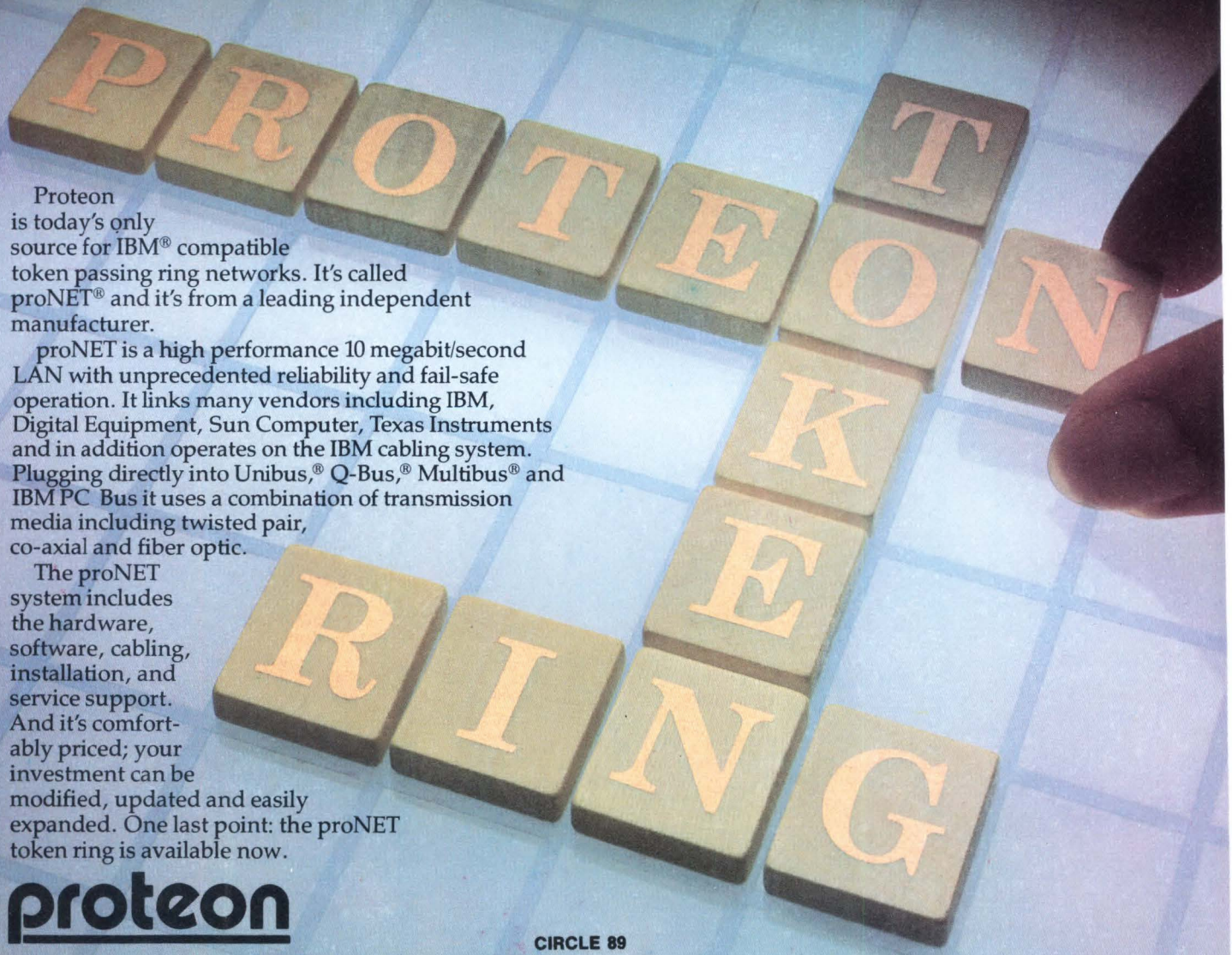
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Multiple display schemes make their mark on smart graphics stations

With close attention paid to command structures and windowing, a series of graphics workstations gives engineers speed, high-level drawings, and interactivity.

The second in a series, this article focuses on the sophisticated display facilities of an intelligent graphics workstation family. The first part, which appeared in the Sept. 20 issue (p. 161), outlined the hardware; future articles will cover specific applications.

Computer graphics are no longer a luxury; rather they have become a necessity within the engineering world. In fact, it is virtually inconceivable today that workstations should appear without the menus, windows, and mice that have become commonplace and without the bit-manipulation, text, and modeling capabilities that an interactive design environment demands.

Putting all those features into one system does not mean simply adding software to an existing computer—not if fast responses and real-time operation are essential. Instead, the command structure becomes critical. Low-level display commands specially designed for generating and manipulating windows hasten the system's response. A bit-manipulation primitive like BitBLT (Block Logical Transfer), which was developed by Xerox Corp.'s Palo Alto Research Center, is well suited to windows and bit-mapped graphics but falls short in demanding CAD/CAM programs. Those applications often must transform detailed geometric models through complex actions like translation, scaling, and rotating. A new standard, the Graphical Kernel System (GKS), gives CAD/CAM a firm foundation, since it generates vector-style graphics that prove essential to engineering tasks (see "A Quick Look at GKS," p. 260)

One collection of intelligent graphics workstations, the 6000, packs it all—an interactive user interface, GKS and BitBLT graphics primitives, and a broad range of output formats—into two series (see the table, p. 261). Both series incorporate the same user interface and the same display subsystem architecture and software. But the systems diverge when they interpret display-list commands and send them to the display hardware.

With similar user interfaces, engineers running the same application program on either system essentially see no difference except in response time and screen resolution. Through the windowed interface, they can select desired operations from a pop-up menu and then move from one window to another, working on sev-

George Reis and **Don Zurstadt**, Tektronix Inc.

Don Zurstadt, ECS display systems software architect, joined Tektronix's Engineering Computer Systems Division last November. Before that, he worked for Autotrol Technology. He has a BA in physics from the University of Colorado.

George Reis, ECS display systems section manager, has been with Tektronix for 11 years, coming aboard directly from 3M. He holds an AAS in electronic technology and a BS in electrical engineering, both from Iowa State University.

eral applications during one sitting. For instance, an engineer may draw a schematic by picking components from a library parts window and moving them into a work-space window. Later, subassemblies can be placed in simulation windows for testing, and finally a documentation window can compile a parts list and a technical description.

The entire 6000 family runs under the Unix operating system, which is not known for its real-time abilities or its fast interactive response. To remedy that, the specially designed display subsystem is given the responsibility of the user interface, thereby freeing the workstations' primary CPU for application programs. The display software is designed for real-time work.

In addition to the display subsystem's hardware and software, two components added to the Unix-based operating system run on the workstations' primary CPU: a display subsystem server and a display subsystem TTY device driver (Fig. 1). The display subsystem server handles requests for activating the device driver; for initiating the subsystem; for managing software routine accesses to the display subsystem; and for creating windows and initiating associated Unix processes. The server also handles requests from the display subsystem, say, for creating and accessing Unix files.

The TTY device driver treats the console and log-in window as a standard ANSI terminal. Standard Unix I/O streams through the driver, which also sends any other associated I/O traffic through the terminal emulator pathways.

Opening a window

Once a window and subwindows are created, they can be accessed directly by application programs. To create a window, application management subroutines get information from the display subsystem server and then make requests directly to the screen-management software. Once created, application programs access terminal emulator windows through the TTY device driver.

The workstations' display subsystem software (Fig. 2) comprises three groups of subroutines—one each for the screen, window frames, and windows—and the display operating system. (A group of subroutines is alternately called a process, and handles a particular set of operations.) The screen subroutines are responsible for all window-management functions and set up the user interface. These are actuated when the user desires to create, move, bury, delete, or collapse a window.

A quick look at GKS

The Graphical Kernel System (GKS), now recognized as an international standard, specifies high-level graphics functions for application programs. Its device-independent primitives can draw lines, display text, and fill areas on a hardware display, plotter, or other peripheral. To communicate with a GKS program, the user enters a point, a real number, a menu choice, a stream of points, a string of text, or a segment—all while the program is running.

Segments are graphics data structures that can be named, transferred to a workstation, displayed, and geometrically transformed (rotated, translated, scaled). With segments, users can organize frequently needed shapes and use them repeatedly.

The GKS structure also can permanently capture graphics through the metafile facility. A programmer sends graphics to the metafile and later uses them for a separate program. For example, the symbols used in a schematic drafting program could reside in a metafile.

The 6000 family of engineering graphics workstations comply with GKS's level 2c for both Fortran 77 application programs and C. Currently, GKS makes no provisions for three-dimensional graphics, nor does it permit editing of segments. An extension to the standard will enable the workstations to edit segments and refer to others through a segment hierarchy. This increases the flexibility and versatility of application programmers.

The window frame subroutines—one group for each window frame of the screen—monitor any data exchanges with the window frames. The window subroutines—here again, one group is assigned to each window or subwindow in a frame—display the borders and handle any data traffic with the windows. A window is a representation of a page of data, while a window frame is the outerdimension of the window.

The display operating system performs many services for the subroutines; for instance, it gives them access to files through the display subsystem server. Files are used for loading text fonts and for calling up nonresident window subroutines. If an engineer makes a selection from the menu, the display operating system senses a mouse movement or a pressed key. The input router passes these asynchronous input events on to the active window subroutines, which then call up the application program through the workstation's primary CPU. The screen and window subroutines communicate with the display operating system synchronously, in contrast to asynchronous user input events.

Display lists key to screen output

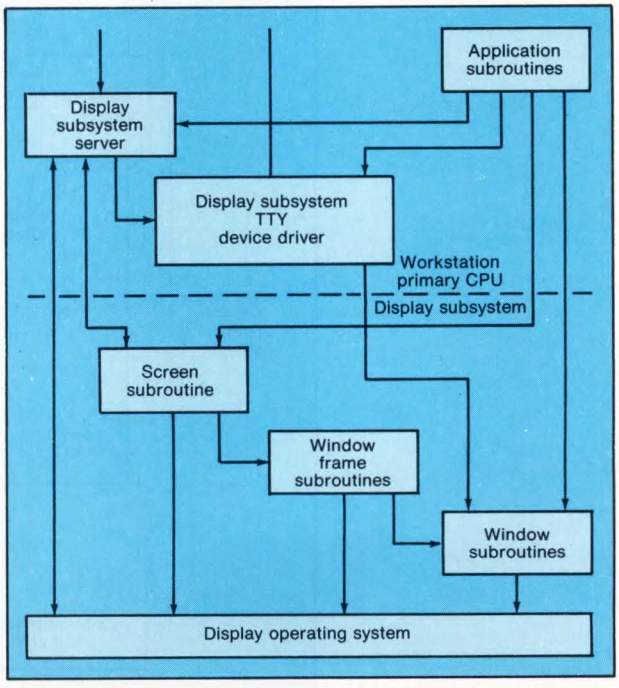
Output to the screen is accomplished by building up display list structures within the screen, window frame, and window subroutines and then executing them. Display lists are a simple framework for ordering text and graphics primitives. Each window can have one or more display list structures, based on input from application programs that use a GKS general-purpose graphics library. The structure facilitates GKS-style organization of text and graphics primitives; BitBLT operations can be mixed in the same list.

Each display list is processed in the context of another data structure, called a display state, that maintains the parameters (such as screen position) within which the graphics and text primitives are interpreted. For example, a GKS polyline function is described by a line type whose attributes (dashed, long dashed, solid, and so forth) are stored in the display-state structure. Similarly, text characters are stored with their font, size, position, and orientation.

The workstation series differ in the way they

A display of salient characteristics

	6100 series	6200 series
Display processor	32000 series, up to 1 Mbyte of local memory	32000 series, floating-point processor, bit-slice display-list microengine; up to 2 Mbytes of local memory (expandable)
Display Features	13-in. color, 15-in. monochromatic; 640 by 480 pixels; 16 simultaneous colors from a 64-color palette	19-in. color, 20-in. monochromatic; 1024 by 768 pixels; 16 or 256 simultaneous colors from a palette of 16.7 million colors
Display subsystems	Supports only one	Supports multiple subsystems
Standard input devices	Keyboard and three button mouse	Keyboard and three button mouse



1. The display subsystem server interfaces with the primary CPU and handles requests for Unix services. The TTY device driver makes the terminal emulator windows operate transparently.

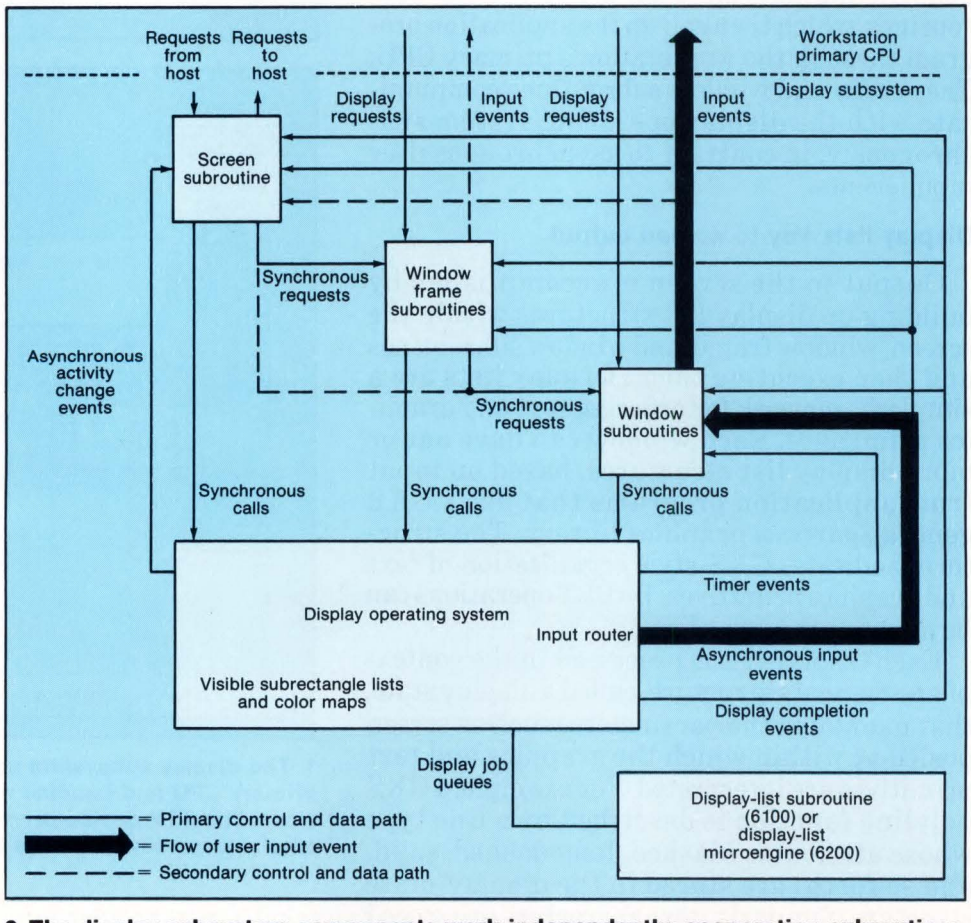
execute the display-list commands, a difference that also accounts for varying screen performance. In the 6100 series, software interprets the commands and converts them into pixel data for the frame buffer. The arrangement streamlines hardware, so that all the display circuitry can fit on the board. In contrast, the high-performance 6200 series executes the display-list commands in a hardware microengine.

The Unix-based operating system executes on the primary CPU for the display system. The 6100 display processor board interfaces with the primary CPU through the external bus. The board runs the display subsystem software, including the display-list manager.

The primary CPU communicates with the display subsystem through common RAM, which stores not only the subsystem software, but also interprocess communication and display-list data structures. The bus interface circuitry buffers information and arbitrates between the external bus and the workstations' CPU. Display lists, control and status information, and user inputs enter the common RAM.

The 6100's frame buffer RAM stores the 640-by-480-pixel bit-mapped data. A monochromatic display is backed up by one 64 kbyte plane, whereas the color display addresses 64kbytes for each of the four planes. Any remaining part of that plane memory may be put to use holding data for text fonts. With the help of the CRT controller, the frame buffer synchronizes the conversion of pixels into serial data for the monitor. The controller itself generates blanking and vertical and horizontal sync signals.

A state machine built into the display sub-



2. The display subsystem components work independently; cooperating subroutines provide high-level window management. Asynchronous and synchronous communication separate internal display signals from those of the main processor.

system hardware keeps track of pixel states (on or off); it also takes advantage of a row destination counter to increase scrolling performance and screen filling.

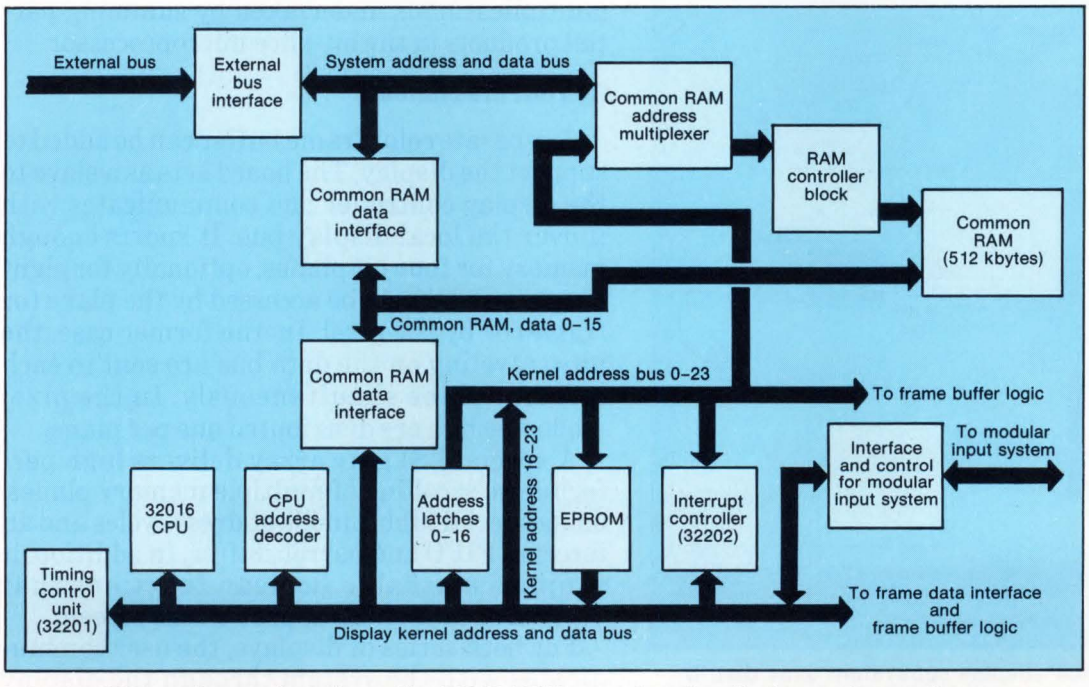
Scrolling is controlled by software, so that the display can move in increments of pixel or character rows. The width and height of the area being filled or scrolled is also under software control. An index generator can convert a monochromatic pixel pattern (mainly for generation of text) into color by adding a prestored color index value to the text signal. In that way, character fonts can be stored as monochromatic fonts and then converted into the desired color for display.

In contrast, the high-performance 6200 series assigns display-list and pixel-processing needs to a set of dedicated processing units (Fig. 3). That distribution scheme furnishes the necessary performance for the more demanding tasks that will run on these workstations, each of which can handle multiple display subsystems.

Be it resolved

For the 6200's monochromatic and color subsystems, displaying 1024 by 768 pixels, a second computing engine operates as the display processor unit (Fig. 4). Like other subsystems in the 6200, the board ties into the global bus, with its own local buses handling display system internal communication. A display controller board, based on the Am29116 bit-slice microprocessor and incorporating a display-list microengine, further boosts performance.

The display controller interprets and executes instructions from the display processor unit, while the display-list microengine con-



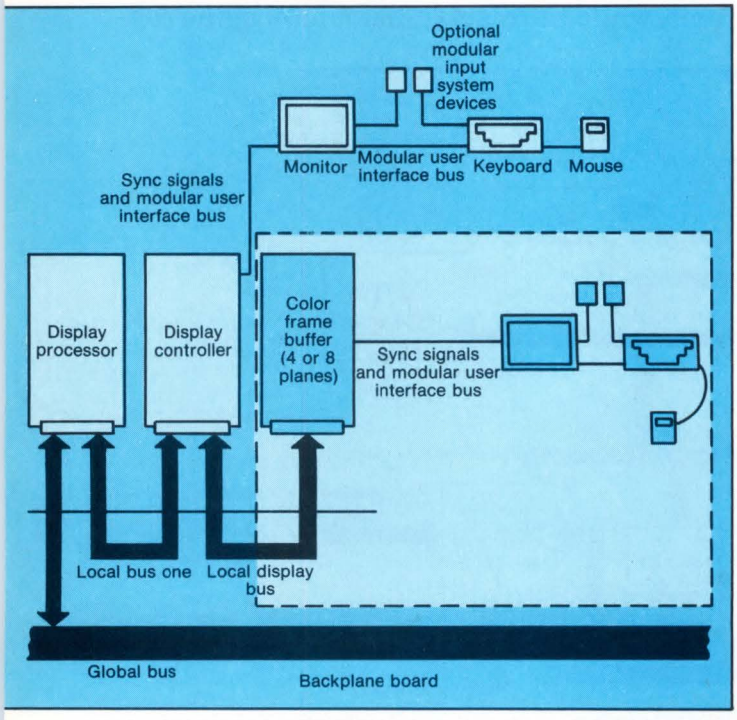
3. In the 6100 series workstations, the 32016 CPU executes the display system software, processes the display list, and puts data into raster form. A signal enters the display subsystem through the external bus.

verts the commands into raster form and sends them to the frame buffers.

The Am29116 microprocessor is extremely fast, has the support of a family of compatible ICs, and fits into a 64-bit-wide parallel processor. With one 64-bit instruction, it can simultaneously control branches, move scratchpad data into a multiplier, add a register value to the internal accumulator, start a bus transfer, and so forth. The parallel processing leads to extremely fast performance on the workstation screen.

A 2910A microsequencer in the display controller board selects the address of the next instruction, which is loaded into the pipeline register and then sent to the bit-slice microprocessor, the microsequencer, and bus logic.

All microcode from the display processor unit flows over the local bus, serially enters into the pipeline register, and goes to the microcode RAM (Fig. 5). When the display-list microengine must swap a page of microcode, it interrupts the processor, which stops the microengine's internal clock and loads the requested page into the register. Two address bytes precede each 64 bits of microcode and are sent to the microcode address register. After the microcode is completely loaded, the microsequencer is reinitialized and the internal clock restarted.



4. The 6200 series' display subsystem uses distributed processing to produce graphics. The display processor accepts signals from the global bus, and then sends them over the local bus one to the display controller. In a monochromatic display, the video and synchronization signals travel to the monitor over the modular user interface bus (MUIB), through which the keyboard, mouse, and optional devices communicate. For a color display, display control signals flow over the local display bus to the color frame buffer board, which works with four or eight bit planes.

When configured for parallel processing, the Am29116 has limited register space, necessitating 8 kbytes of scratchpad RAM. That fast static RAM is accessed by the microprocessor, the multiplier chip, and other internal circuitry. The 16-by-16 bit multiplier performs the 32-bit external coordinate transformations, used by GKS in particular. A 32- and 48-bit multiplication is undertaken by summing partial products in the bit-slice microprocessor.

Roll out the planes

A separate color frame buffer can be added to support the display. The board acts as a slave to the display controller and communicates with it over the local display bus. It sports enough memory for four bit planes, optionally for eight bit planes and may be accessed by the plane (or frame) or by the pixel. In the former case, the bits traveling on the data bus are sent to each memory plane simultaneously. In the pixel mode, the bits are distributed one per plane.

A special LSI gate array delivers high performance scrolling of multiple memory planes, using special nibble mode address cycles and an internal FIFO and barrel shifter. In addition, it supplies maskable Boolean functions that determine how pixels appear on the screen.

For both series of displays, the user communicates with the system through the display processor's modular input system, which can be configured for daisy-chaining of keyboards, mice, and other input devices. For example, a mechanically integrated keypad can be attached to either end of the keyboard or can be used as a detached device.

A remote universal peripheral interface controller, Intel's 8044 RUPI, coordinates the interaction between the display processor and

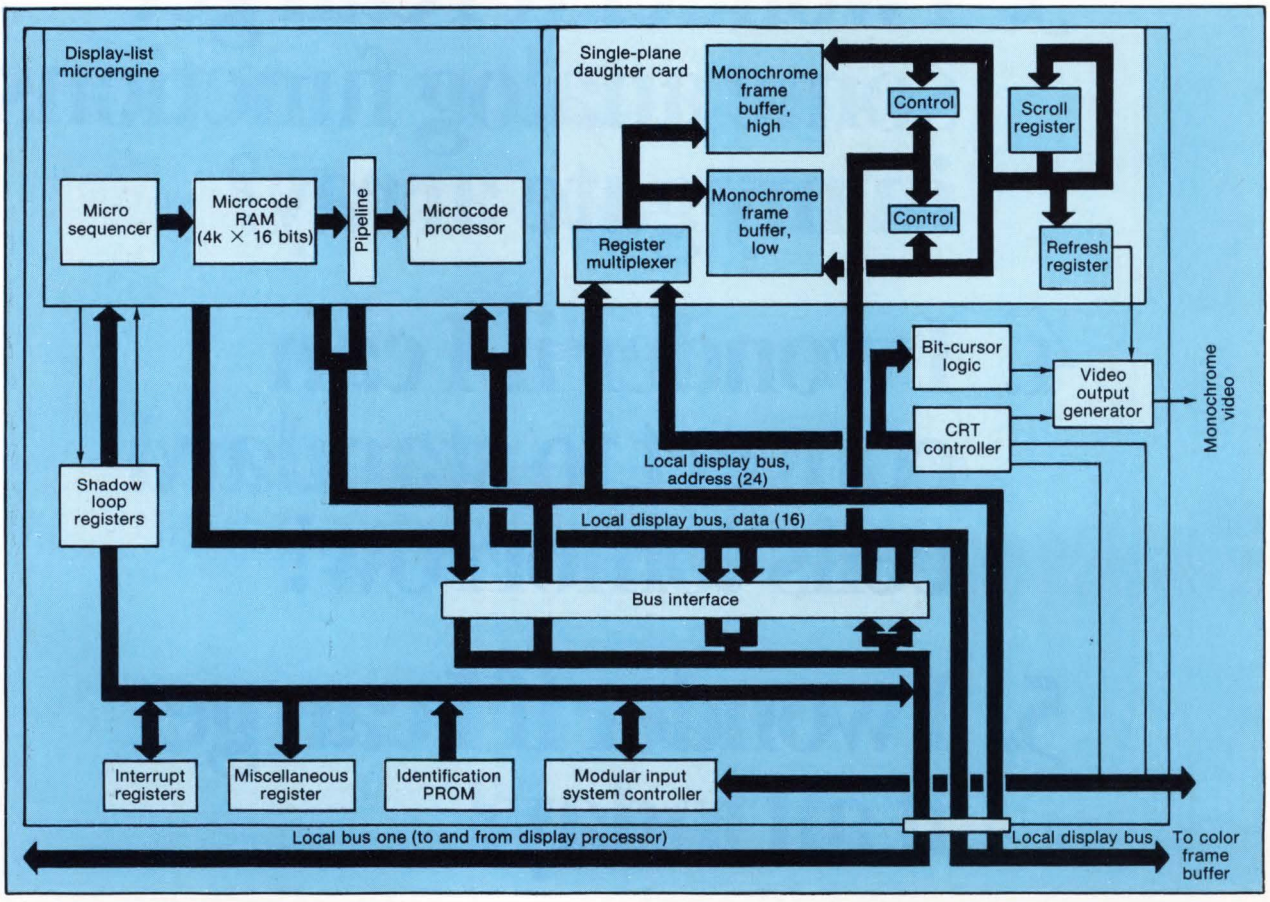
every input device. The controller in the main board receives data from peripheral controllers through a simple two-wire path, with the main controller acting as a master and the others as slaves. The keyboard adheres to the SDLC protocol. During power-up and configuration, each chip identifies itself by a two-field code that contains type of device and an ID number.

Following a GKS polyline

As a demonstration, suppose that an engineer working on a 6200 runs a Fortran 77 GKS program that includes a call to the polyline routine. First, the program initializes the GKS environment, then opens and activates a GKS logical workstation. Appropriate internal state lists and other data structures are created in the workstation's computing engine, after which GKS requests a window through the display subsystem server. The polyline routine creates a display list with the coordinate points being drawn and transfers it to the proper window subroutines in the display subsystem.

The display list microengine, constantly monitoring the command queue in the display processor memory, sees a display list ready for execution. The microcode engine executes the display-list commands, even clipping the graphics primitives against the window border if requested. The 16-by-16-bit multiplier in the display-list microengine quickly transforms the segments of the polyline.□

How useful?	Circle
Immediate design application	562
Within the next year	563
Not applicable	564



5. The 6200 display controller manages many internal signals. A signal enters local bus one en route to the display processor unit, which internally produces a video output for the monochromatic display or for the color frame buffer.

1. I wonder if I can get 13,000 gates?

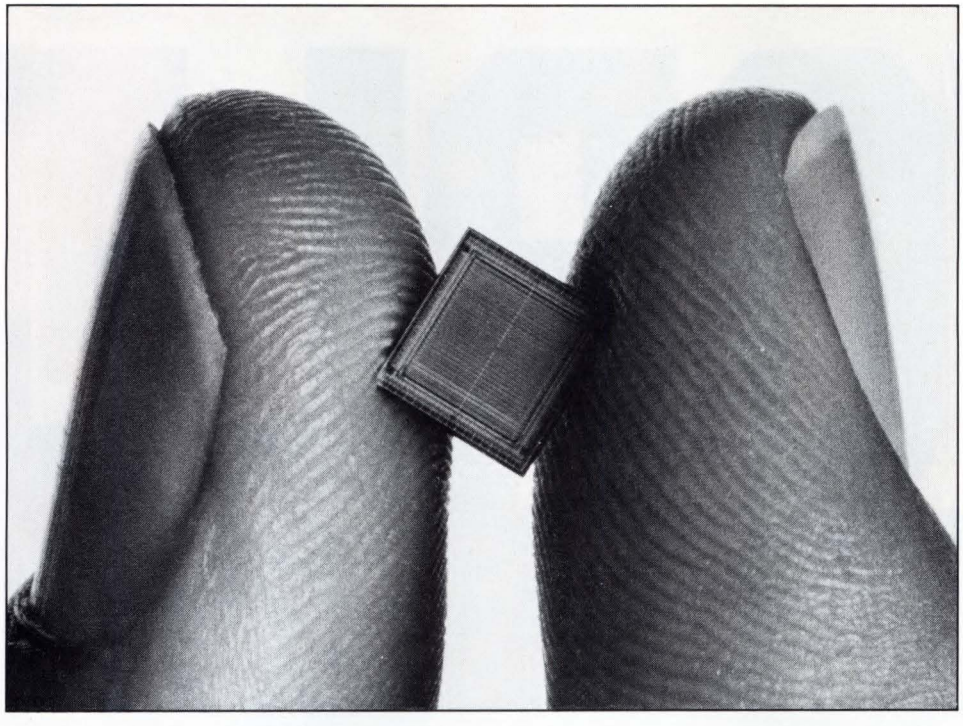
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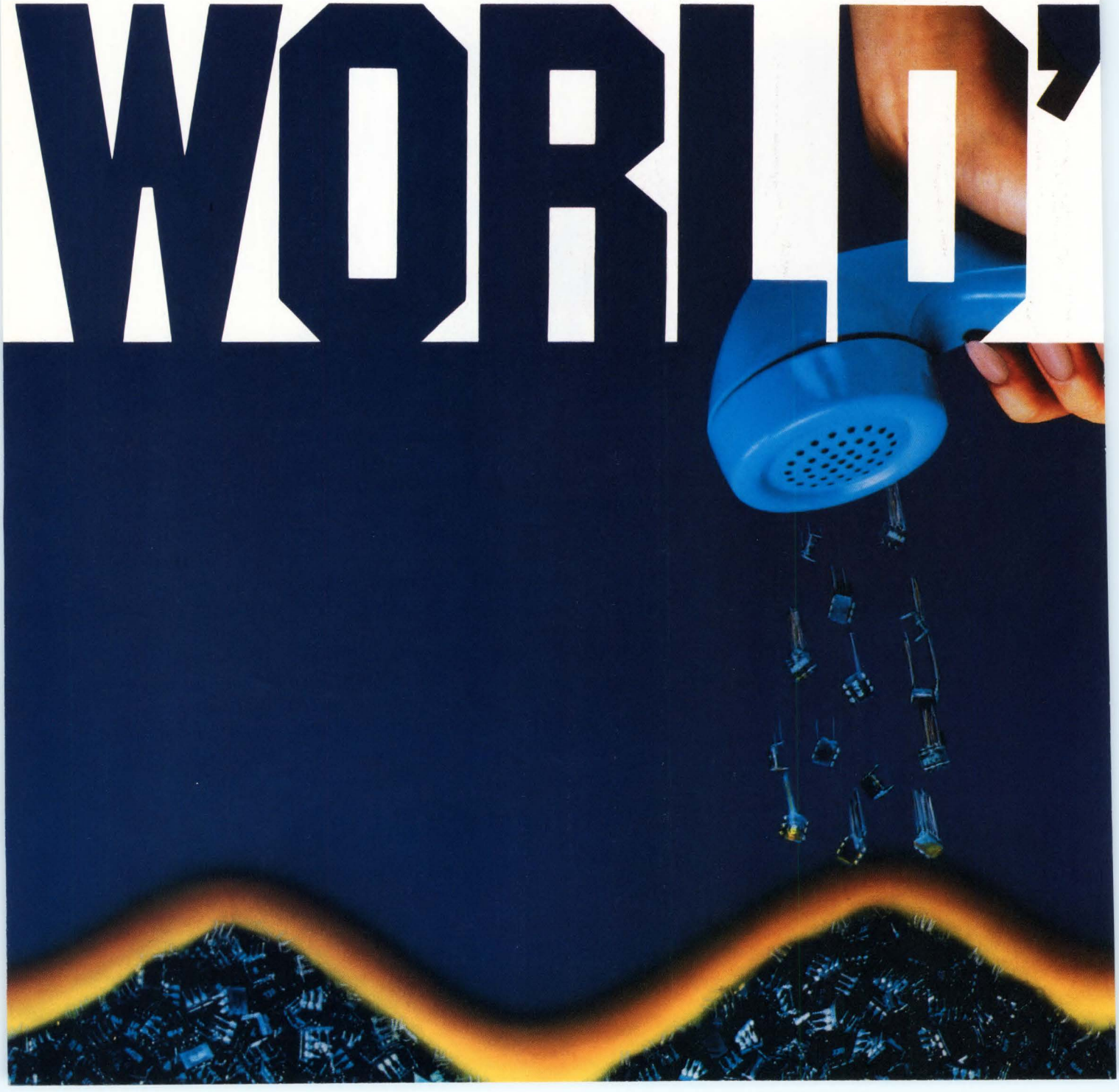
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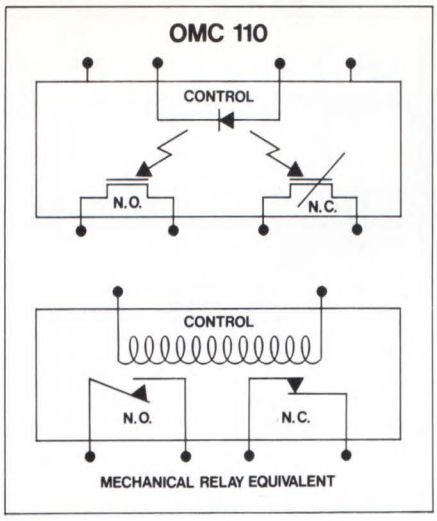
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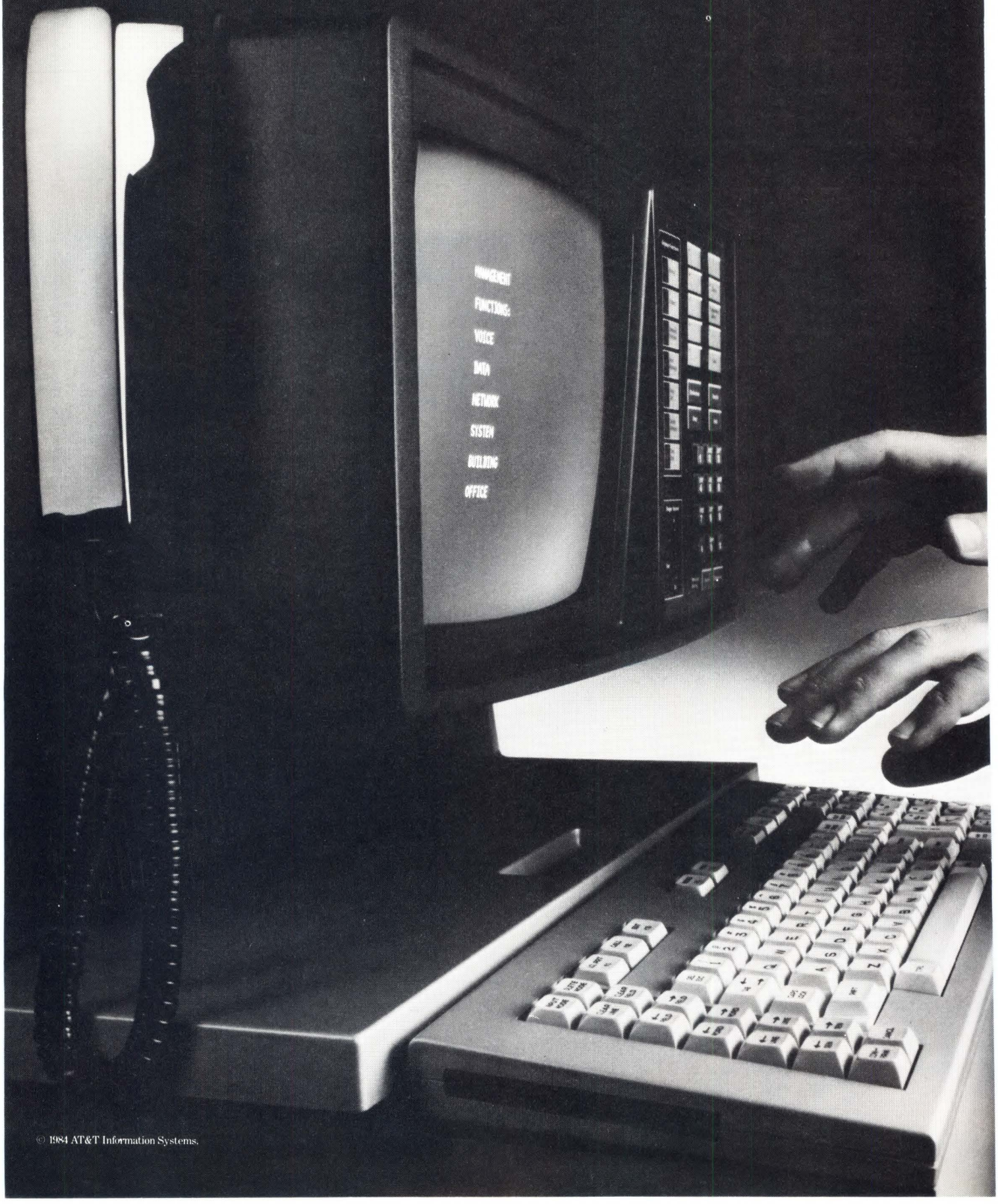
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3	●	●■	●	●
4	●			
5	●			
6	●	●■	●	●
7	●			
8	●			
9	●			
10	●	●■	●	●
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PROM and octal latch make a simple, versatile 7-bit counter

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A novel idea for designing a counting circuit uses a PROM instead of the usual up-down counter. The PROM, when teamed with an octal latch, yields a streamlined, versatile 7-bit counter.

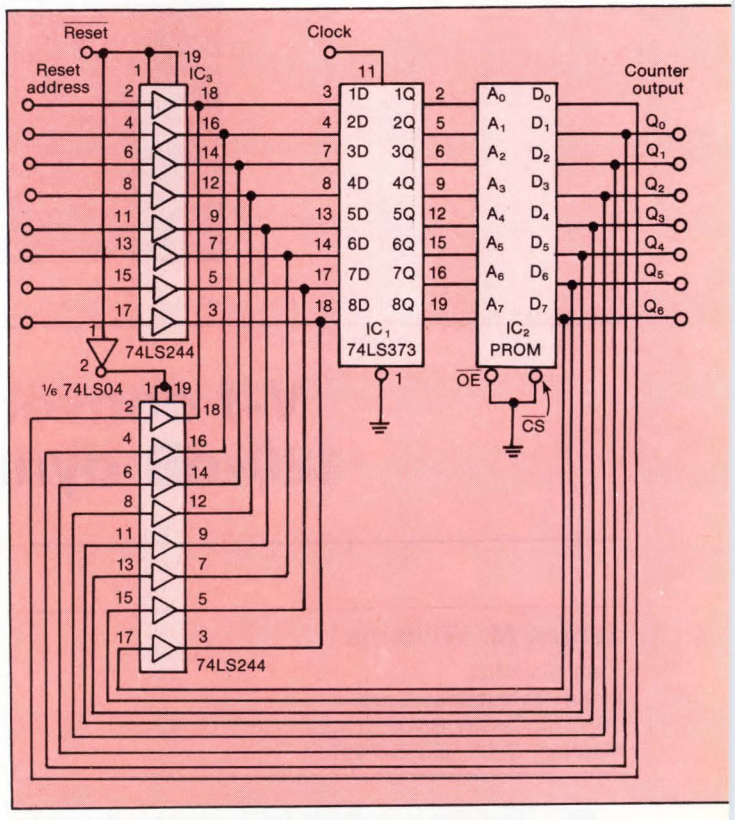
The circuit (see the figure) handles complex counting jobs. For example, for the first pulse, the counter might set to 5 and for the second pulse, to 7. Next, it might set to 3 and then to 1 for the fourth pulse. A conventional counter performing that task would need many more ICs than the PROM-based circuit and would additionally require that its logic gates be changed as the counting sequence is varied.

The PROM circuit has another edge over the conventional design. The latter's counting speed is limited by the delays encountered when signals pass through logic gates. Since the PROM circuit has no gates, the counting speed is limited only by the access time of the PROM.

A clock signal is applied to a 74LS373 octal latch, IC_1, to capture data previously acquired by the PROM, IC_2, through an octal driver, IC_3. The PROM uses the latched data as an address to obtain succeeding data for the next clock cycle. The resulting counter steps through a predetermined sequence on the arrival of each clock pulse.

In general, the data from the PROM at the N−1 clock pulse forms the address for the memory chip at the N clock pulse, the data at the N clock pulse forms the address at the N+1 pulse, and so on. In that manner, the data fed back forms a new address and the PROM and latch create a counting logic circuit. Whenever two identical states must be stepped through, the D_0 bit in the PROM is used as a control bit to arbitrate (see the table).

Any type of PROM can be used, but attention should be paid to access time. For example, a



PROM data, held in an octal latch, forms the address information in this counterless counter circuit. The circuit is especially adept at nonsequential counting.

16-kbit NMOS PROM such as the 2716 has a 350-ns access. A 10-ns bipolar device can considerably increase the counter's speed.

The counter is reset by applying a pulse on the Reset line for a period longer than one clock pulse. The address to the PROM will then come from IC_3, rather than from the PROM's output. The circuit will also reset for the next incoming clock pulse if data from the PROM matches the address set at IC_3.

Programming data for counterless counter

State	Counter output required Q_0	PROM address A_0	PROM data to be burned	Control bit D_0	Remarks
1	000 0000	0000 0000	0000 000	1	
2	000 0010	0000 0001	0000 010	1	
3	000 0001	0000 0101	0000 001	1	
4	000 0011	0000 0011	0000 011	1	
5	000 0010	0000 0111	0000 010	0	States 2 and 5 are the same
6	000 0100	0000 0100	0000 100	1	
7	000 0011	0000 1001	0000 011	0	States 4 and 7 are the same
8	000 0101	0000 0110	0000 101	1	
9	000 0100	0000 1011	0000 100	0	States 6 and 9 are the same
10	000 0110	0000 1000	0000 110	1	
11	000 0101	0000 1101	0000 101	0	
12	000 0111	0000 1010	0000 111	1	
13	000 0110	0000 1111	0000 110	0	States 10 and 13 are the same
14	000 1000	0000 1100	0001 000	1	
15	000 0111	0001 0001	0000 111	0	States 12 and 15 are the same
16	000 1001	0000 1110	0001 001	1	
17	000 1000	0001 0011	0001 000	0	States 14 and 17 are the same
18	000 1010	0001 0000	0001 010	1	
19	000 1001	0001 0101	0001 001	0	States 16 and 19 are the same

V-f converter offers 120-dB dynamic range

James M. Williams
Staff Scientist
Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, Calif. 95035-7487

Although it is built with several discrete devices, a voltage-to-frequency converter offers a wider dynamic range—120 dB—than monolithic devices. The circuit offers an output of 1 Hz to 1 MHz for a 0-to-10-V input. The circuit's operation hinges on a control loop that uses the output frequency to balance the input current.

Op amp IC_1 integrates a positive input voltage in a negative direction. When its output crosses zero, the output of op amp IC_2 switches low. That causes the diode bridge, built around a 2.5-V reference, to limit at −3.7 V (the reference minus the forward voltage). As a result, a



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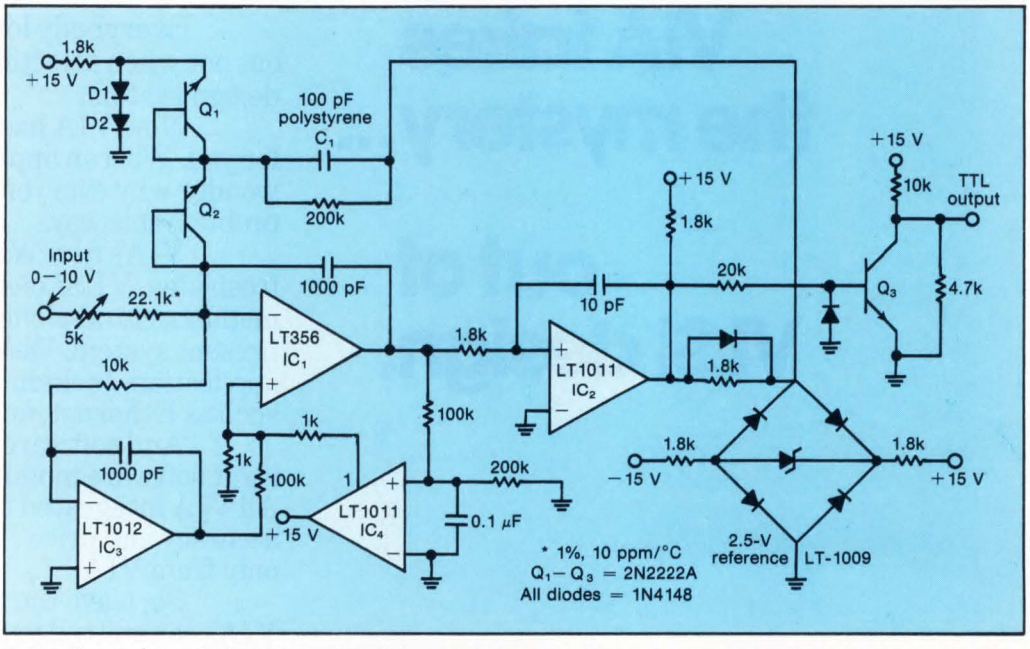
charge is pulled from IC_1's summing junction via C_1, a 100-pF capacitor.

Next, the output of IC_1 goes positive, switching IC_2 and limiting the diode bridge to +3.7 V. The 100-pF capacitor charges, IC_1's summing junction recovers, and the entire cycle repeats. In that manner, the circuit output oscillates at whatever frequency is required to keep IC_1's summing junction at zero.

Diodes D_1 and D_2 compensate the diodes in the bridge. Transistor Q_1, connected as a diode, compensates another transistor, Q_2, which is used as a steering diode. Transistors are used instead of diodes because they provide lower leakage.

Other contributing circuit elements include a precision op amp, IC_3, which stabilizes IC_1 without introducing any additional bias current error. Op amp IC_4 is in the circuit to guard against circuit latch-up—a possible problem due to the ac-coupled feedback loop. If the circuit latches, the output from IC_1 goes to the negative rail and stays there. That causes the output of IC_4 to go high and the output of IC_1 to head positive, initiating normal circuit operation. Since the output of IC_4 is used in an emitter-follower mode, its output is taken from pin 1.

To trim the circuit, precisely 10 V must be applied to the input and the 5-kΩ potentiometer adjusted until the measured output is 1 MHz. Because of IC_3's low offset, there is no need for zero trimming. In fact, the zero-point drift is less than 0.1 Hz/°C. The circuit will maintain linearity to within 0.05% and will typically exhibit 25 ppm/°C drift over its range. The output is TTL compatible.



A feedback loop helps the output frequency control the input current in a 1-Hz-to-1-MHz voltage-to-frequency converter. The circuit offers a 120-dB dynamic range that surpasses those offered by currently available monolithic devices.



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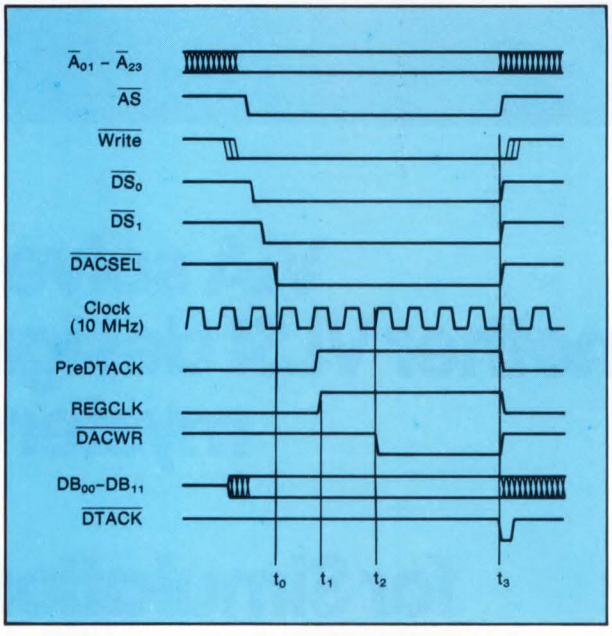
Timing generator controls DAC data transfer to block digital noise

Eduardo Lipiansky
Electronic Design Engineer
Varian Associates, Instruments Division
2700 Mitchell Drive
Walnut Creek, Calif. 94598
(Also with the University of California Extension, Berkeley)

Feedthrough of digital signals can be a problem for high-resolution digital-to-analog converters when they are connected directly to a microprocessor bus. Digital feedthrough is the change in the analog output caused by data being switched on the d-a converter's input lines when the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$) control lines are inactive (both high). It also can occur when the inputs are toggled when the converter is in its transparent mode ($\overline{CS}$ and $\overline{WR}$ both low) and its analog input reference is at 0 V.

A solution that is much less costly than delay lines but equally effective requires the use of external octal latches, which temporarily hold data, and a timing generator, which renders the converter's input lines inactive except when they are needed. In a representative circuit (see the schematic), a Data Transfer Acknowledge (DTACK) generator retimes VERSAbus asynchronous control signals to facilitate sequential data transfer to a pair of 74LS374 octal D-type flip-flops. The writing sequence is timed so that the data lines will be quiet when data is being transferred.

The DTACK generator must produce three signals—DTACK, PreDTACK, and D-a Converter Write (DACWR). When the converter is addressed by system software, the d-a converter Select line ($\overline{DACSEL}$) is asserted, and the 74LS393 counter starts running at 100



The timing diagram of a write cycle shows the 74LS393 counter enabled at t_0. At t_1, the data (DB_{00} through DB_{11}) is clocked into the latches. From t_2 to t_3, the d-a converter is transparent. At t_3, data previously held in the latches enters the converter.

Winner for September 6, 1984

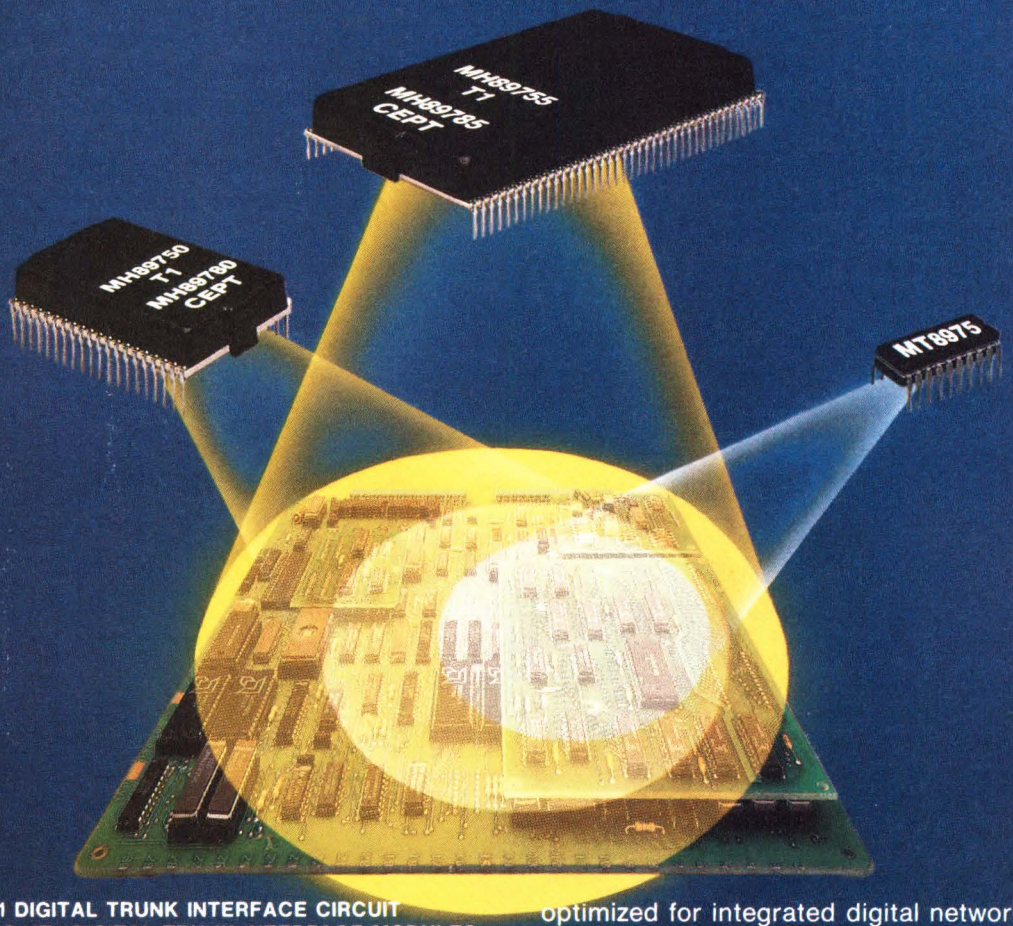
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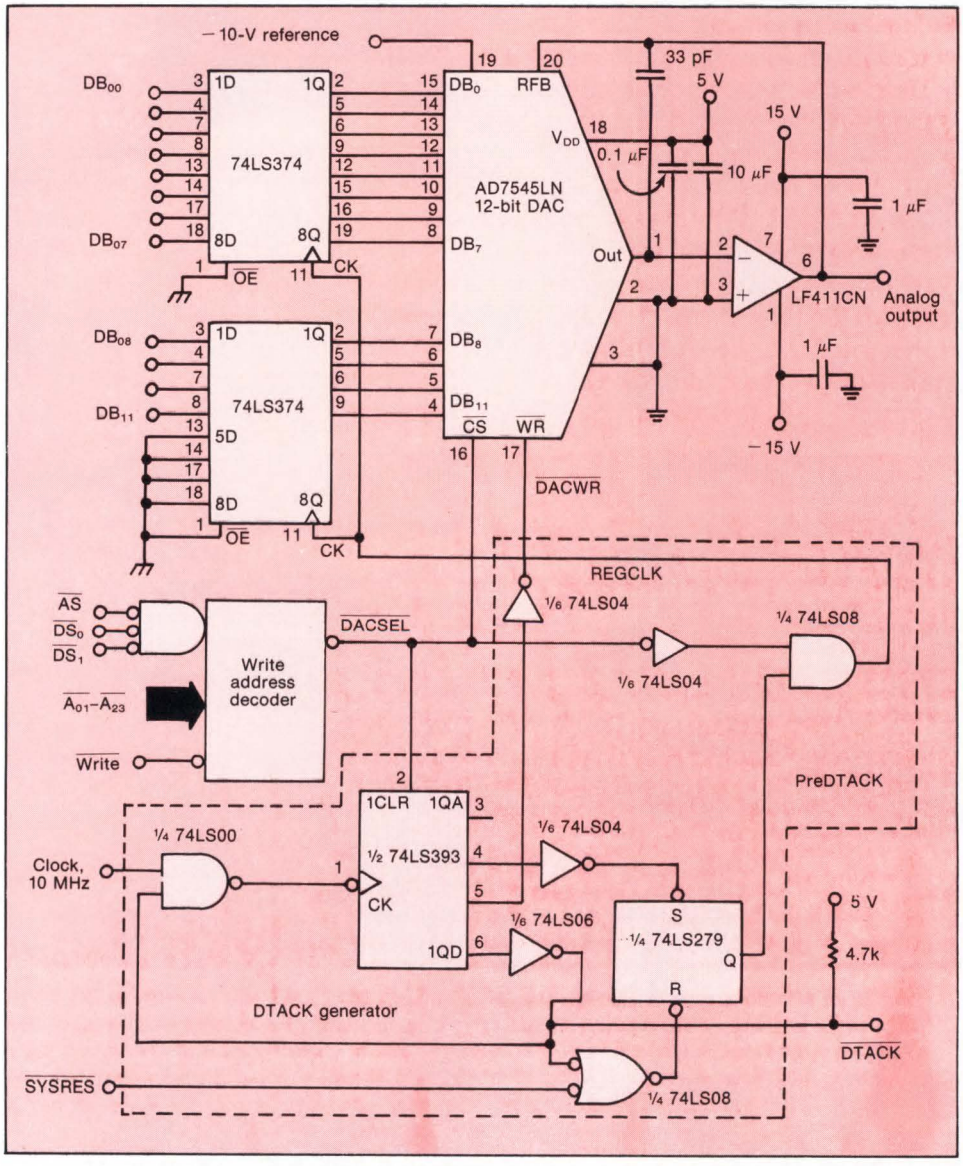
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ns/state (see the timing diagram). The Pre-DTACK line goes high, 100 to 200 ns after DACSEL is asserted, allowing a lengthy setup time before data is clocked into the flip-flops.

Some 200 ns after the rising edge of the Pre-DTACK signal, the DACWR goes low and stays low for 400 ns. During that time the converter is in its transparent mode, that is CS and WR are low and the data lines are inactive. At the eighth transition of the 74LS393 counter, DTACK is asserted, negating DACWR, Pre-DTACK, and DACSEL. Data previously held in the latches is then latched into the d-a converter on the rising edge of DACWR.

The DTACK generator will serve several I/O devices, providing that the appropriately decoded I/O select signal is connected to the counter's Clear line. Also, a different clock frequency or other counter outputs can be used if varied timing requirements are necessary.



A Data Transfer Acknowledge (DTACK) generator controls the movement of information through a digital-to-analog converter to prevent feedthrough of digital signals to the analog output. Data is clocked into a pair of octal flip-flops that are controlled by the timing generator.

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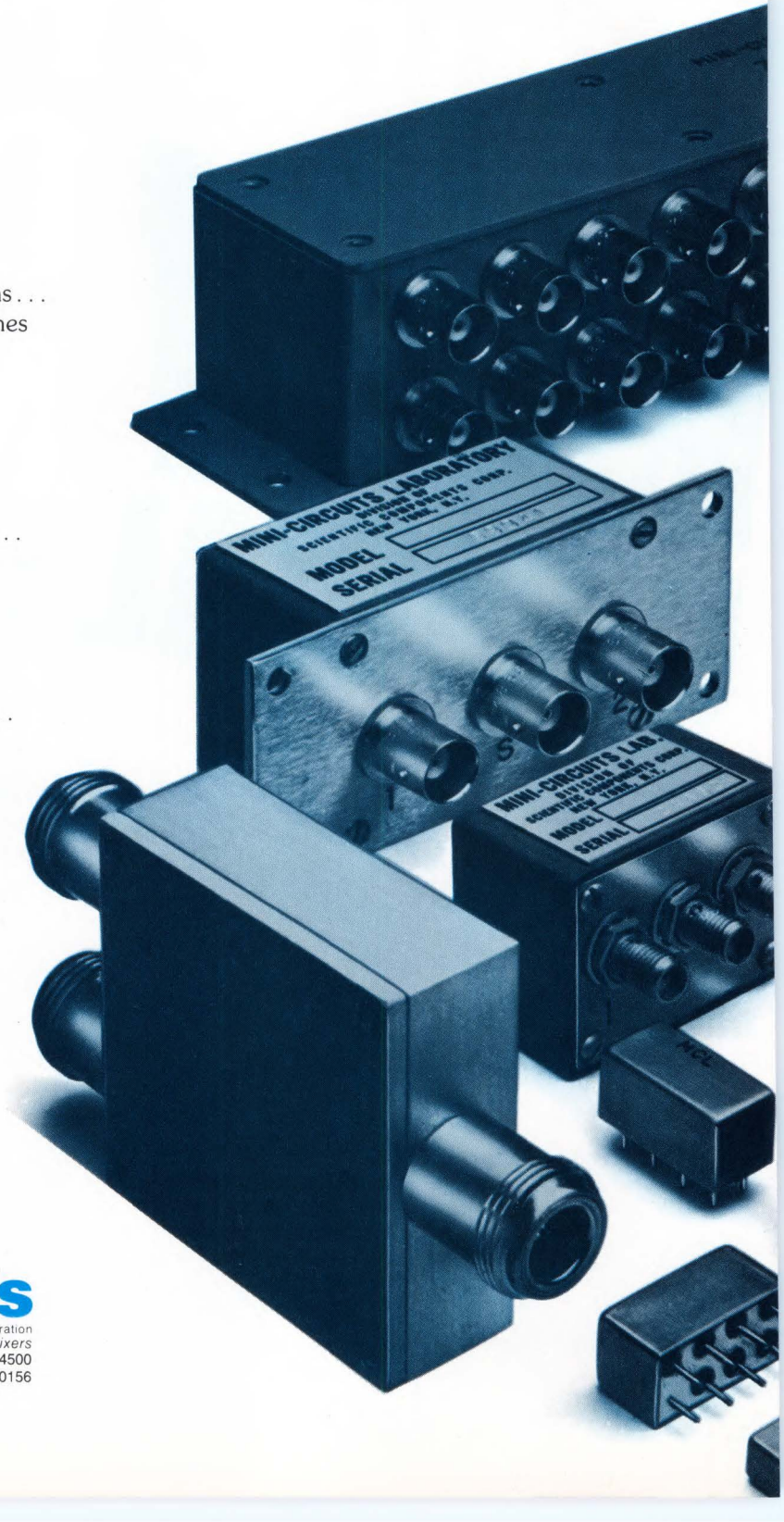
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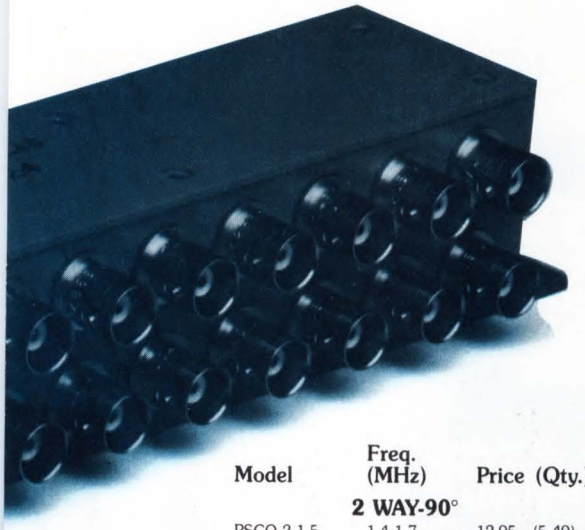
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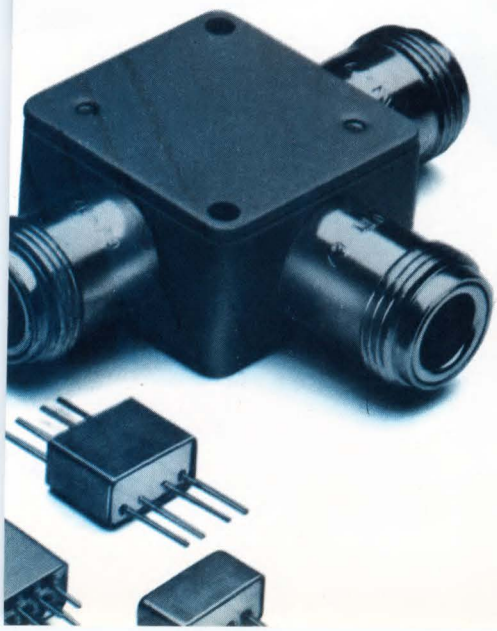
C73-1 REV. ORIG.

combiners

covering 2 KHz to 4.2 GHz from $9.95



Model	Freq. (MHz)	Price	(Qty.)
2 WAY-90°			
PSCQ-2-1.5	1.4-1.7	12.95	(5-49)
PSCQ-2-3.4	3.0-3.8	16.95	(5-49)
PSCQ-2-6.4	5.8-7.0	12.95	(5-49)
PSCQ-2-7.5	7.0-8.0	12.95	(5-49)
PSCQ-2-10.5	9.0-11.0	12.95	(5-49)
PSCQ-2-13	12-14	12.95	(5-49)
PSCQ-2-14	12-16	16.95	(5-49)
PSCQ-2-21.4	20-23	12.95	(5-49)
PSCQ-2-50	25-50	19.95	(5-49)
PSCQ-2-70	40-70	19.95	(5-49)
PSCQ-2-90	55-90	19.95	(5-49)
PSCQ-2-120	80-120	19.95	(5-49)
PSCQ-2-180	120-180	19.95	(5-49)
PSCQ-2-250	150-250	19.95	(5-49)
PSCQ-2-400	250-400	19.95	(5-49)
PSCQ-2-450	350-450	19.95	(5-49)
ZAPDQ-2	1000-2000	59.95	(1-9)
ZAPDQ-4	2000-4200	59.95	(1-9)
ZMSCQ-2-50	25-50	49.95	(4-24)
ZMSCQ-2-90	55-90	49.95	(4-24)
ZMSCQ-2-180	120-180	49.95	(4-24)
ZSCQ-2-50	25-50	39.95	(4-24)
ZSCQ-2-90	55-90	39.95	(4-24)
ZSCQ-2-180	120-180	39.95	(4-24)
2 WAY-180°			
PSCJ-2-1	1-200	19.95	(5-49)
PSCJ-2-2	0.01-20	29.95	(5-49)
ZFSCJ-2-1	1-500	49.95	(4-24)
ZFSCJ-2-3	5-300	39.95	(4-24)
ZMSCJ-2-1	1-200	47.95	(4-24)
ZMSCJ-2-2	0.01-20	57.95	(4-24)
ZSCJ-2-1	1-200	37.95	(4-24)
ZSCJ-2-2	0.01-20	47.95	(4-24)



Model	Freq. (MHz)	Price	(Qty.)
2 WAY-0°			
LPS-109	10-500	15.95	(5-24)
PSC-2-1	0.1-400	9.95	(6-49)
PSC-2-1W	1-650	14.95	(6-49)
PSC-2-2	0.002-60	19.95	(6-49)
PSC-2-4	10-1000	19.95	(6-49)
■ PSC-2375	55-85	19.95	(6-24)
■ PSC-2-1-75	0.25-300	11.95	(6-49)
MSC-2-1	0.1-450	16.95	(5-24)
MSC-2-1W	2-650	17.95	(5-24)
TSC-2-1	1-400	13.95	(5-24)
ZFSC-2-1	5-500	31.95	(4-24)
■ ZFSC-2-1-75	0.25-300	32.95	(4-24)
ZFSC-2-1W	1-750	35.95	(4-24)
ZFSC-2-2	10-1000	39.95	(4-24)
ZFSC-2-4	0.2-1000	44.95	(4-24)
ZFSC-2-5	10-1500	49.95	(4-24)
ZFSC-2-6	0.002-60	36.95	(4-24)
■ ZFSC-2-6-75	0.004-60	38.95	(4-24)
ZMSC-2-1	0.1-400	37.95	(4-24)
ZMSC-2-1W	1-650	42.95	(4-24)
ZMSC-2-2	0.002-60	47.95	(4-24)
ZSC-2-1	0.1-400	27.95	(4-24)
ZSC-2-1W	1-650	32.95	(4-24)
ZSC-2-2	0.002-60	37.95	(4-24)
ZSC-2-4	10-1000	37.95	(4-24)
■ ZSC-2375	55-85	37.95	(4-24)
■ ZSC-2-1-75	0.25-300	29.95	(4-24)
	GHz		
ZAPD-1	0.5-1.0	39.95	(1-9)
ZAPD-2	1.0-2.0	39.95	(1-9)
ZAPD-4	2.0-4.2	39.95	(1-9)
ZAPD-21	0.5-2.0	49.95	(1-9)
3 WAY-0°			
PSC-3-1	1-200	19.95	(5-49)
PSC-3-1W	5-500	29.95	(5-49)
PSC-3-2	0.01-30	29.95	(5-49)
■ PSC-3-1-75	1-200	20.95	(5-49)
■ PSC-3-1-75-2	10-300	22.95	(5-49)
PSC-3-13	1-200	24.95	(5-49)
ZFSC-3-1	1-500	39.95	(4-24)
ZFSC-3-1W	2-750	41.95	(4-24)
ZFSC-3-13	1-200	39.95	(4-24)
ZMSC-3-1	1-200	47.95	(4-24)
ZMSC-3-2	0.01-30	57.95	(4-24)
ZSC-3-1	1-200	37.95	(4-24)
ZSC-3-2	0.01-30	47.95	(4-24)
■ ZSC-3-1-75	1-200	38.95	(4-24)
■ ZSC-3-2-75	0.02-20	48.95	(4-24)
	GHz		
ZA3PD-1	0.5-1.0	79.95	(1-9)
ZA3PD-1.5	0.75-1.5	79.95	(1-9)
ZA3PD-2	1-2	79.95	(1-9)
ZA3PD-4	2-4.2	79.95	(1-9)

■ Denotes 75 ohm models

Performance over the entire frequency range is approximately less than 1 dB insertion loss, greater than 20 dB isolation, less than 0.5 dB amplitude unbalance and less than 3 degree phase unbalance.

For complete specifications, please refer to our new 64 page RF Signal Processing Components Guide.

C73-2 REV. ORIG.

CIRCLE 144

Model	Freq. (MHz)	Price	(Qty.)
4 WAY-0°			
PSC-4-1	0.1-200	28.95	(6-49)
■ PSC-4-1-75	1-200	24.95	(6-49)
PSC-4-3	0.25-250	23.95	(6-49)
PSC-4-6	0.01-40	29.95	(6-49)
PSC-4A-4	10-1000	49.95	(6-49)
ZFSC-4-1	1-1000	89.95	(1-4)
ZFSC-4-1W	10-500	74.95	(1-4)
ZFSC-4-3	10-300	69.95	(1-4)
■ ZFSC-4375	50-90	89.95	(1-4)
ZFSC-4-2-75-1	200-800	74.95	(1-4)
ZMSC-4-1	0.1-200	56.95	(4-24)
ZMSC-4-2	0.002-20	69.95	(4-24)
ZMSC-4-3	0.25-250	53.95	(4-24)
ZSC-4-1	0.1-200	46.95	(4-24)
■ ZSC-4-1-75	1-200	46.95	(4-24)
ZSC-4-2	0.002-20	69.95	(4-24)
ZSC-4-3	0.25-250	43.95	(4-24)
	GHz		
ZA4PD-2	1-2	79.95	(1-9)
ZA4PD-4	2-4.2	79.95	(1-9)
ZB4PD-42	1.7-4.2	99.95	(1-9)
ZB4PD-4	3.7-4.2	89.95	(1-9)
5 WAY-0°			
PSC-5-1	1-300	59.95	(1-5)
■ PSC-5-1-75	1-300	59.95	(1-5)
6 WAY-0°			
PSC-6-1	1-175	68.95	(1-5)
■ PSC-6-1-75	1-300	78.95	(1-5)
ZFSC-6-1	1-175	89.95	(1-4)
■ ZFSC-6-1-75	1-200	89.95	(1-4)
8 WAY-0°			
PSC-8-1	0.5-175	68.95	(1-5)
■ PSC-8-1-75	0.5-175	69.95	(1-5)
PSC-8-6	0.01-10	79.95	(1-5)
PSC-8A-4	5-500	89.95	(1-4)
■ PSC-8A4-75	1-300	79.95	(1-4)
ZFSC-8-1	0.5-175	89.95	(1-4)
■ ZFSC-8-1-75	0.5-175	90.95	(1-4)
■ ZFSC-84-75	1-300	119.95	(1-4)
■ ZFSC-8375	50-90	119.95	(1-4)
ZFSC-8-4	5-700	129.95	(1-4)
ZFSC-8-43	30-1000	139.95	(1-4)
ZFSC-8-6	0.01-10	109.95	(1-4)
	GHz		
ZB8PD-2	1-2	149.00	(1-9)
ZB8PD-4	2-4.2	149.00	(1-9)
12 WAY-0°			
	MHz		
ZFSC-12-1	1-200	174.95	(1-4)
ZFSC-12-11	10-300	174.95	(1-4)
16 WAY-0°			
ZFSC-16-1	0	174.95	(1-4)
ZFSC-16-3	1-[illegible]	174.95	(1-4)
■ ZFSC-16-675	0.01-25	189.95	(1-4)
ZFSC-16-12	0.1-200	189.95	(1-4)
24 WAY-0°			
ZFSC-24-1	0.2-100	264.95	(1-4)
ZFSC-24-11	1-200	274.95	(1-4)
ZFSC-24-6	0.025-50	274.95	(1-4)
48 WAY-0°			
ZFSC-48-1	10-300	595.00	(1-4)
■ ZFSC-48-1-75	10-300	595.00	(1-4)

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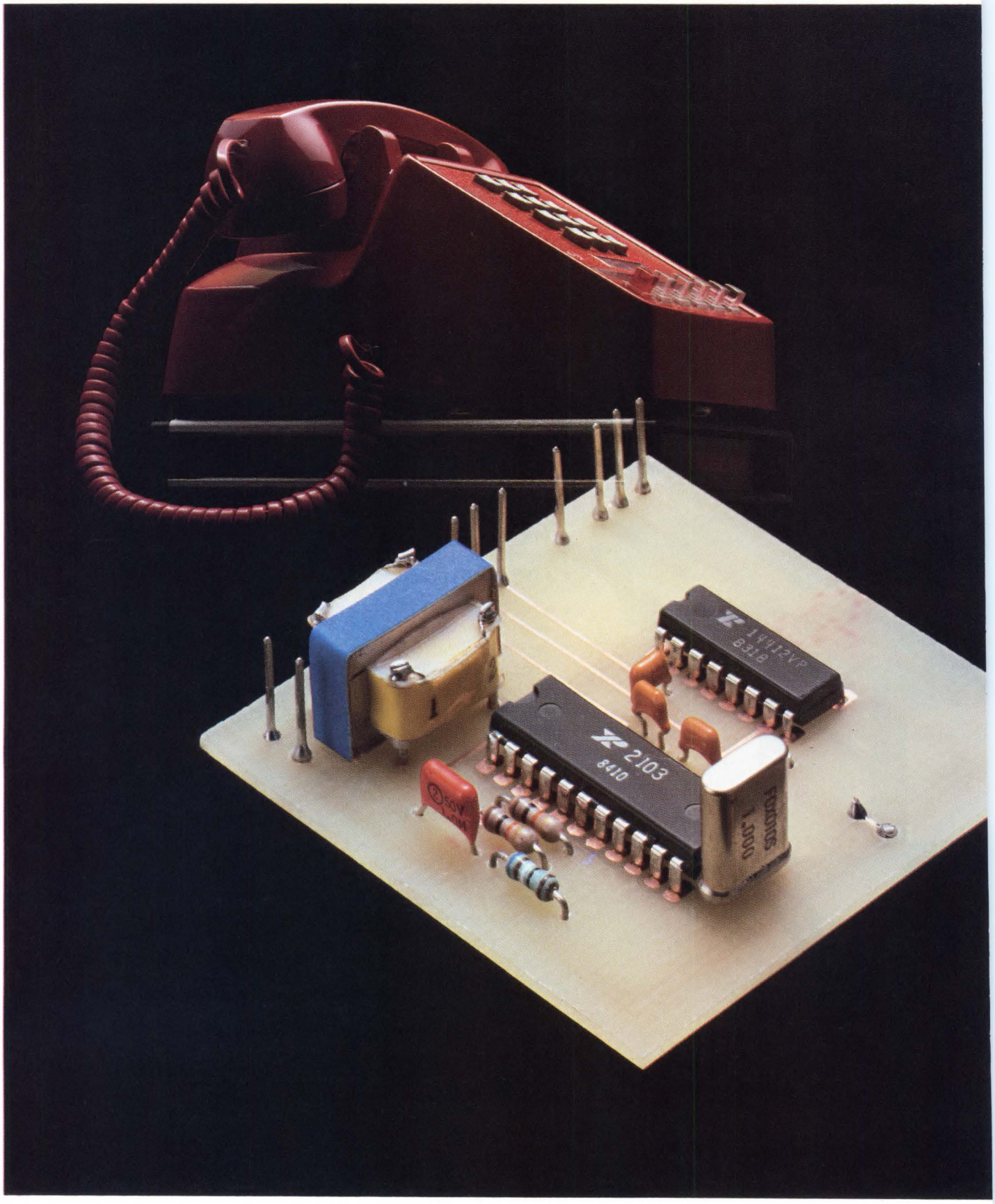
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Design Problems? The Answer is EXAR.

Now EXAR has come up with yet another solution: the XR-2103 Monolithic Switched-Capacitor Filter. Designed specifically to perform the complete filtering function for a Bell 103-type (300 BPS) compatible modem, the XR-2103 is meant to be used in conjunction with the XR-14412 Modulator/Demodulator. A complete, stand alone two-chip modem is the result.

How We Made It Makes a Difference.

The XR-2103 is actually two six-pole bandpass filters (centered at 1170Hz and 2125Hz respectively) providing you with both transmit and receive filter functions. Multiplexers route these signals into and out of the correct filter. Direct interface to the XR-14412 is taken care of by a built-in, auto-zeroing limiter that converts the received carrier to digital levels. Also built in is a carrier detection circuit providing you with a typical sensitivity of −48dBM plus a built-in 2dB hysteresis. To further enhance the solution, the XR-2103 shares the same crystal with the XR-14412.

You Have Three Choices. This One's the Right One.

What's the alternative to our XR-2103 solution? You could use our XR-14412 combined with a number of discrete filters. But you'd spend a lot of time tuning and counting components. Or you could spend up to twice as much money on a single chip approach and a lot of time justifying the cost.

That's why your best choice is the XR-2103. It's reliable, inexpensive, easy to use, and offers you a low external part count. And better still, we can provide you with a modem evaluation kit to minimize your 103 modem design task.

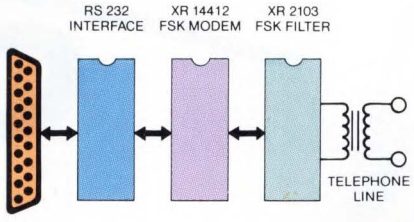
It All Adds Up to EXAR.

When you consider that the XR-2103 filter also features CMOS technology for low power consumption (enabling line-powered capabilities), complete on-board output active filters, programmable input receive gain to boost weak signals, and an oscillator circuit that gives you the option of either an independent 4.0 MHz crystal or shared 1.0 MHz crystal operation, the XR-2103 adds up to a truly elegant solution.

Features and Applications

Features: single 5-volt operation; 4.0 MHz/1 MHz clock input; complete on-board output active filters; low supply current; internal answer/originate mode switching; programmable input receive gain.

Applications: Bell 103 transmit/receive filtering complement to XR-14412 or other modulator/demodulators.



103 Compatible Modem

The Solution is Just a Call or Coupon Away.

If it sounds like we can help you with your design, give us a call or cut out the coupon and get the whole story. We'll send you everything you'll need including our Modem Design Handbook, a thorough compilation of modem design and technical data. Once you see what we have to offer, you'll see why we say "EXAR goes one step further."



EXAR, I'd Like Your Help!

☐ Send me the **EXAR Modem Design Hand Book.**

☐ Also, send me more information about the Modem Design Kit.

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INTENDED APPLICATION_____

The EXAR Family of Filters and Modems.

Device	Application	Type	Speed (BPS)	Tech-nology	Features
(Filters)					
XR-2103 XR-2120	Bell 103 Bell 212A	FSK PSK	300 300/1200	CMOS CMOS	Low Power, 5V Low External Part Count, Versatile
(Modems)					
XR-14412	CCITT V21 Bell 103 Mod/Demod	FSK	300/600	CMOS	Low Power 5V
XR-2211	Adjustable Demod	FSK	0-1M	Bipolar	Wide Speed Range
XR-2206 XR-2207	Adjustable Mod	FSK	0-1M	Bipolar	Wide Speed Range
XR-2123	Mod/Demod	PSK	1200/2400	CMOS	2400bps Half Duplex 1200bps Full Duplex
XR-210	Mod or Demod	FSK	0-10M	Bipolar	Wide Speed Range, Adjustable

As our chart indicates, we have a wide variety of solutions for a wide variety of modem applications (with even more filters on the way). And, to complete your design, there are EXAR's RS-232 line drivers and receivers for interfacing, as well as a wide range of op amps for amplification and signal conditioning functions. Still not satisfied? Then contact us about an EXAR custom-designed product for your special application.

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CIRCLE 99

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In October, Electronic Design has something extra for career-minded engineers

Career Extra is the industry's only recruitment newspaper for 118,000 professional engineers. Our career-oriented articles and interviews with leading Personnel Managers give readers a complete assessment of employment trends and opportunities.

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Monolithic 12-bit ADCs need only 5 V and convert in 100 μs

The first one-chip 12-bit successive-approximation a-d converters to work from a single 5-V supply have arrived. From National Semiconductor, the CMOS ADC1205 and ADC1225 convert in just 100 μs.

Furthermore, when a −5-V supply is added, they become 13-bit converters by adding a sign bit to their two's complement output code. (Virtually all successive-approximation devices lose 1 bit of resolution when operated in a bipolar configuration.)

In the unipolar mode the input signal can run from −0.05 to +5.05 V when the reference and V_{CC} are at +5 V. Bipolar signals under similar conditions can run between −5.05 and +5.05 V.

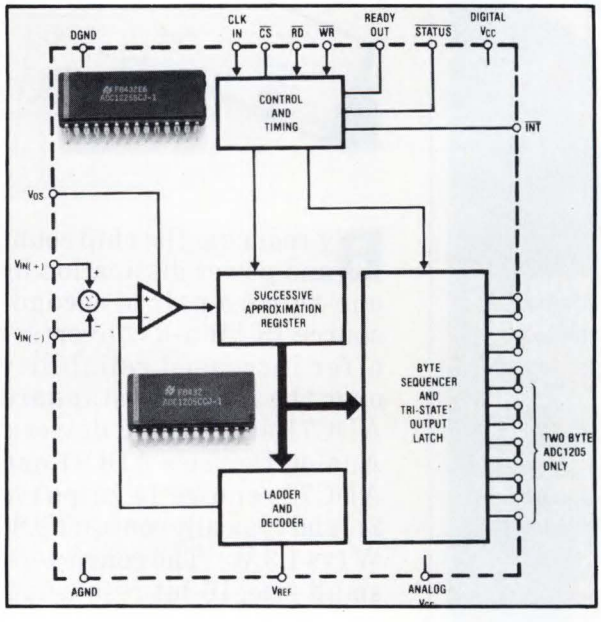
One major difference separates the 1205 from the 1225: It puts out a 13-bit data word in two bytes, high byte first, and thus fits into a 24-pin DIP, whereas the 1225 puts out a 13-bit word broadside for direct interfacing with a 16-bit bus and therefore requires a 28-pin DIP.

All versions guarantee an unadjusted zero error on both the unipolar and bipolar input ranges of ±2 LSBs. This error varies just 1.5 ppm/°C. Unadjusted positive and negative full-scale error for unipolar and bipolar operation is ±30 LSBs, but external adjustments bring that ±½ LSB for unipolar signals and ±1 LSB for bipolar. Moreover the gain temperature coefficient is under 15 ppm/°C.

The nonlinearity is ±½ LSB for the upper grade of both chips and ±1 LSB for the lower grade. In addition there are two temperature ranges for each grade, for a total of eight models (see the table).

The converters also boast a differential input circuit—that is, the full-scale input voltage at both inputs can sit above ground; any error is within ±½ LSB. This input circuit, a feature not seen on many units, whether monolithic or hybrid, also acts as a buffer so that input signals from high-impedance sources do not disturb the converter.

Since the chips are made with a CMOS process, they consume just 25 mW. That

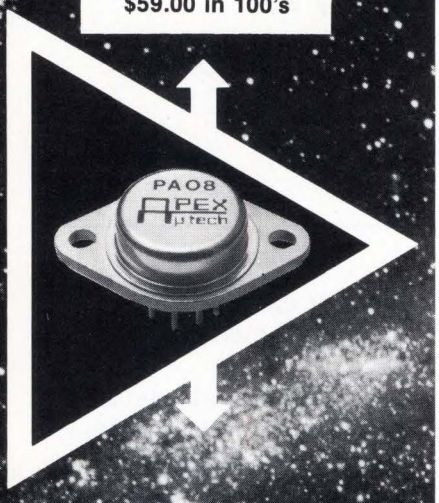


Frank Goodenough

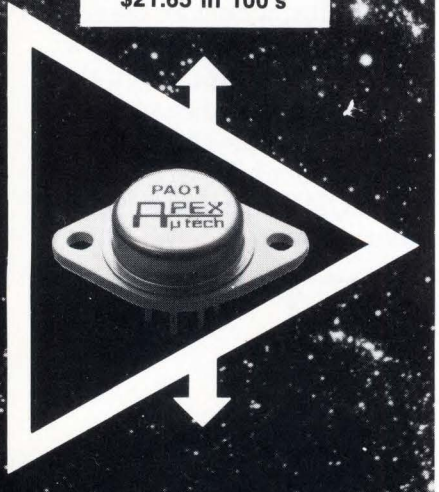
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CIRCLE 102

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ANALOG

Model	Operating temperature range (°C)	Package (no. of pins)	Unit price in hundreds ($)
ADC1205BCJ-1	0 to 70	24	29.95
ADC1205CCJ-1			19.95
ADC1225BCJ-1		28	29.95
ADC1225CCJ-1			19.95
ADC1205BCJ	−40 to +85	24	45.00
ADC1205CCJ			35.00
ADC1225BCJ		28	45.00
ADC1225CCJ			35.00

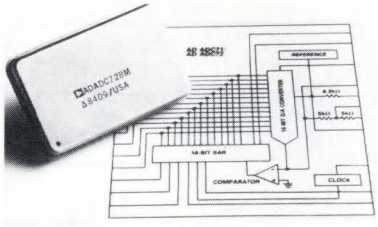
Notes: Specifications are guaranteed over the full operating temperature range.
V_{CC} = 5 V.

represents only 5 mA from the 5-V supply. The minus supply used for converting bipolar signals needs a mere 100 μA additional.

Furthermore, the devices get on and off the bus fast, too: Access time is just 350 ns. The chips have a unique architecture, combining charge-balancing, or sampled data, comparators with a switched-capacitor network for the MSBs and resistors for the LSBs.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; Al Tremain, (408) 721-5226. **CIRCLE 307**

16-bit ADCs reduce power consumption

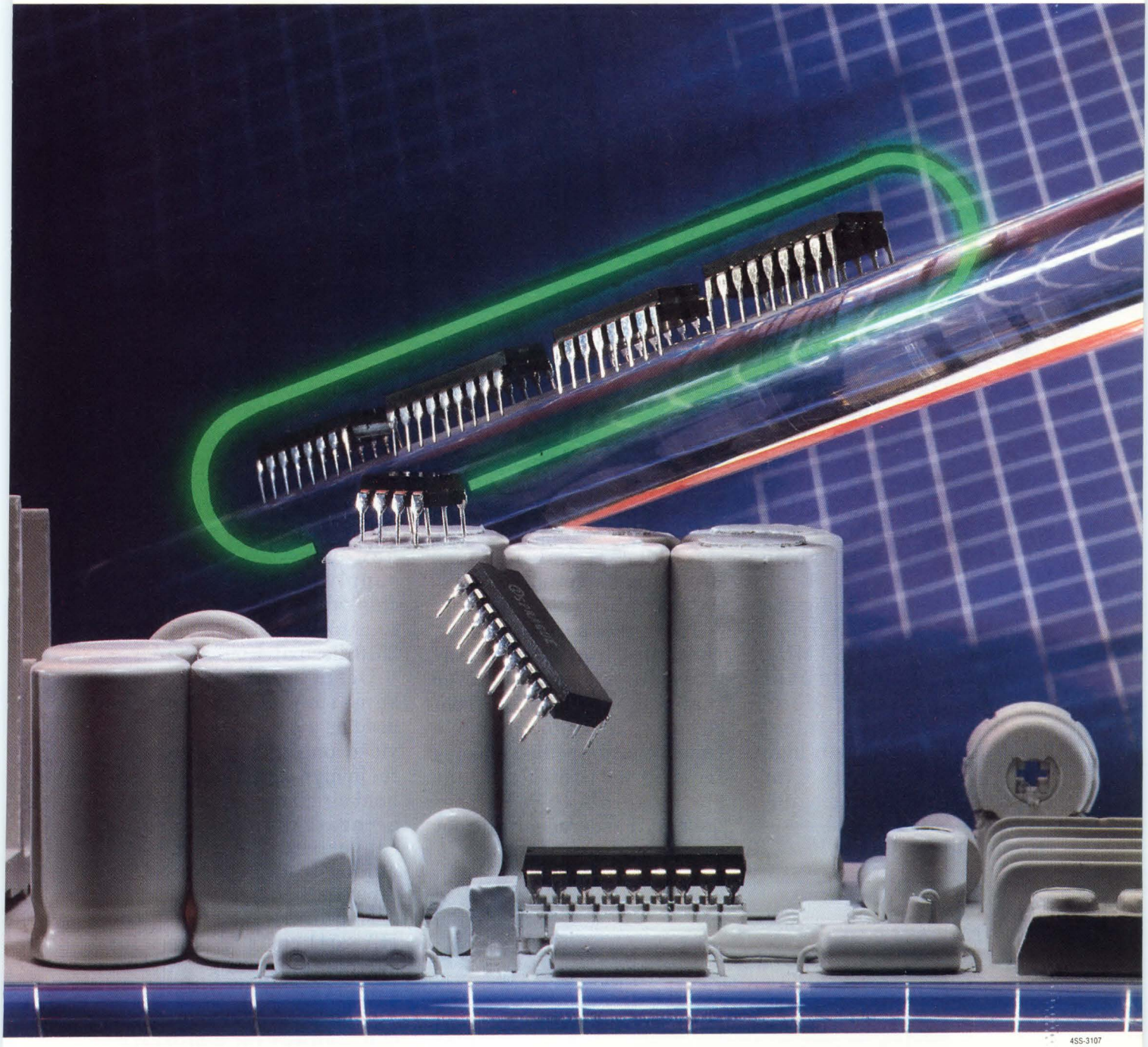


By reducing the chip count and power dissipation by one-third, a pair of second-source 16-bit a-d converters offer increased reliability over the industry-standard ADC71 and ADC72 devices. Analog Device's ADC71 and ADC72 require 14 chips (vs 21) and typically consume 0.85 W (vs 1.3 W). The converters' small size, 16-bit resolution, and 14-bit accuracy make them useful in such applications as data acquisition, ATE, and industrial robots.

Specifications for the devices include a maximum nonlinearity of ±0.003% (±0.006% for the J and A grades), a 50-μs maximum conversion time short-cycled to 14 bits, and no missing codes for the K and B versions to 14 bits from 10° to 40°C. All digital inputs and outputs are TTL-compatible. Internal thin-film resistors allow analog ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V, and 0 to +20 V.

Analog Devices Inc., 804 Woburn St., Wilmington, Mass. 01880; (617) 935-5565. Starting at $140 (100 units); six to eight weeks. **CIRCLE 309**

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CIRCLE 103

ANALOG

Op amp chips remain stable at a 40-MHz unity-gain bandwidth

The first monolithic optional amplifier to be stable at a unity-gain bandwidth of 40 MHz finally permits the use of op amps as general-purpose video amplifiers—even in a follower (buffer) configuration. Until now, wideband operation with stable unity gain has been the domain of hybrid ICs.

The full-power bandwidth of the HA-2541 from Harris is an equally impressive 3 MHz, and it is guaranteed over ±10-V output swing. Moreover, it slews at a guaranteed 250 V/μs. (The extremely high slew rate is responsible for the chip's full-power bandwidth.)

Heather Bryce

In contrast, its predecessor, the HA-2510, until now the fastest monolithic op amp available, slews at only 50 V/μs and has unity-gain and full-power bandwidths of 12 and 1 MHz, respectively.

Also, the 2541 settles to within 0.1% of final value in a mere 90 ns, (typical) for a 10-V output step vs 250 ns for the HA-2510.

To get that speed, however, the input bias current increases by a factor of 150 over that of the earlier unit, from 200 nA to 30 μA. At the same time, input impedance drops from 50 MΩ to 50 kΩ. But at the op amp's 40-MHz frequency, these tradeoffs do not cause significant errors.

Nor are dc specifications sacrificed to achieve the higher speeds. The op amp's offset voltage is 2 mV maximum and its offset voltage drift is 20 μV/°C. The common-mode rejection ratio is 70 dB, and the open-loop gain is 80 dB.

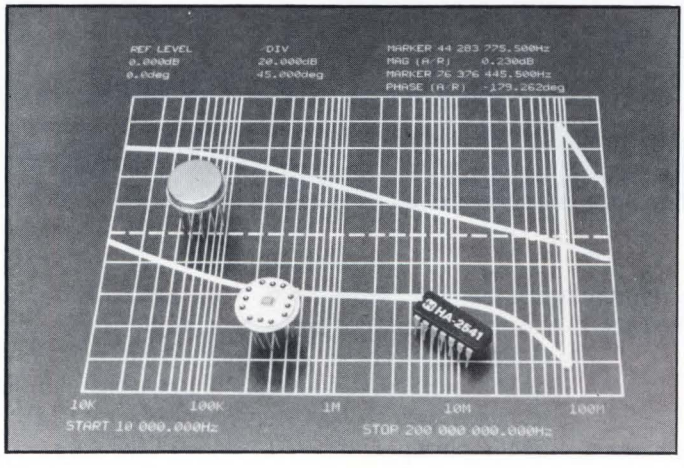
These impressive specifications do impose a penalty, however—higher power-supply requirements: The chip draws 45 mA from a ±5- to ±15-V power supply. (The 2510 dissipates only 6 mA.)

Despite the power consumption, the 2541 can be used as a pulse, wideband, or video amplifier. It is also useful in high-speed sample-and-hold circuits, fast and highly accurate digital-to-analog converters, and high-speed analog-to-digital converter input buffer circuits.

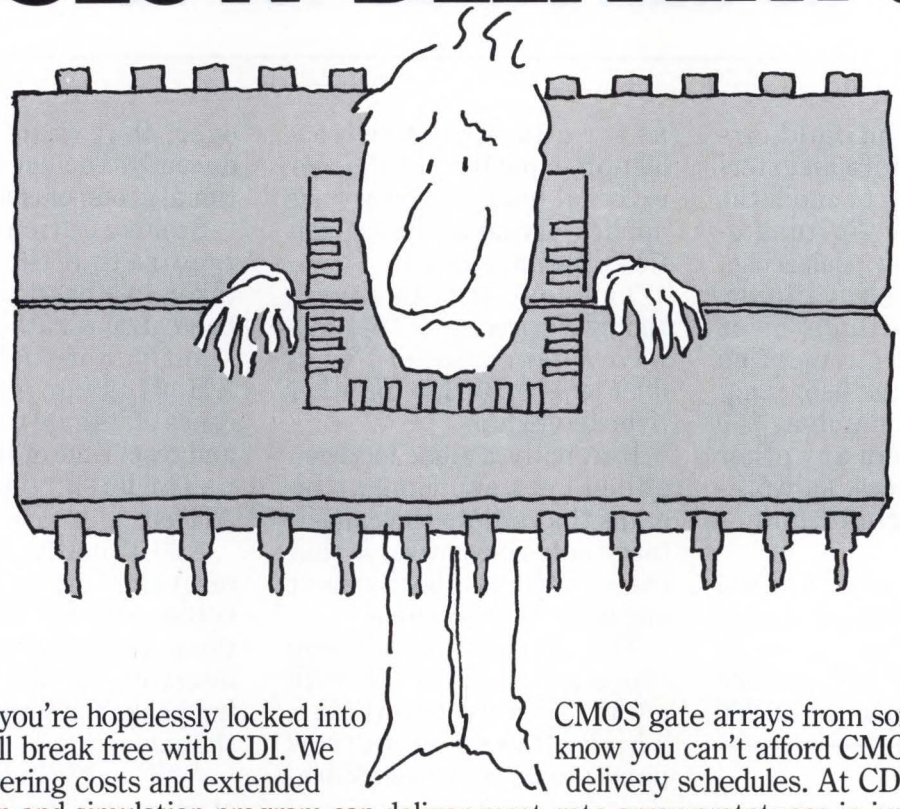
In quantities of 100, the HA-2541 costs $6 apiece for the commercial grade in a 14-pin Cerdip (0° to 75°C), $9 for the same grade in a TO-8 can, and $24 for a military-grade unit in a TO-8 can. Small quantities are available from stock.

Harris Corp., PO Box 883, Melbourne, Fla. 32901; Gloria Simpson, (305) 724-7418.

CIRCLE 306



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CIRCLE 104

ANALOG

Sense-and-hold hybrid captures pulse peaks as narrow as 100 ns

Sample-and-hold circuits require an external device to catch the maximum value. Fortunately, there are a few peak sense-and-hold devices available. Now, two thin-film hybrids from Optical Electronics find the peak value and hold it automatically as much as 150 times faster than any other commercial peak sample-and-hold hybrid or monolithic IC.

The AH503 and AH504 peak sense-and-hold circuits capture pulses as narrow as 100 ns for a 1-V pulse with a 100-pF hold capacitor or 200 ns for a 10-V pulse with a 300-pF capacitor. (As larger external hold capacitors are applied, of course, the acquisition time increases.)

The cost of this speed, though, is precision: The units have a gain error of 1%, vs 0.1% or even 0.01% for other hybrids or chips.

Internally, a diode has been added between the two op amps that allows the capacitor to only go positive, so that the circuits can both detect and hold the peak value.

The hybrids have a droop rate of less than 1 mV/μs with a 330-pF hold capacitor, which allows very narrow pulses to be captured. Moreover, that value can be reduced by the use of an additional group of components.

Some applications may require that the sample be taken in a particular narrow band of time rather than constantly. For such cases the AH504 is appropriate, because of its gate time of 250 ns and reset time of 100 ns, vs 400 ns for both times for the AH503.

Additionally, the shorter reset time makes the AH504 better not only for capturing the peak during specific time intervals, but also for capturing peaks for several units at the same time.

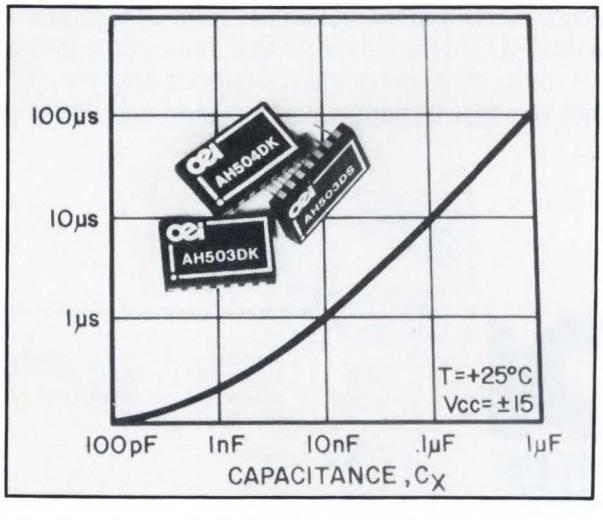
A "K" suffix indicates operation over 0° to 70°C, and an "S" −55° to +125°C. (At 125°C, however, the droop rate increases to 7 mV/μs maximum.) Circuits with a "D" suffix come in a dual in-line package.

All models are available from stock. In 100-unit quantities, the prices are $88.10 apiece for the AH503DK and $127.40 each for the AH504-DK and AH503DS.

Optical Electronics Inc., PO Box 1140, Tucson, Ariz. 85734; (602) 624-8358.

CIRCLE 304

Heather Bryce



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PART NO.	ORGANIZATION	SPEED (COM'L MAX)	POWER (TYP) OPERATING	STANDBY
IDT6167	16Kx1	45ns	125mW	10μW
IDT6168 IDT7168 1/2*	4Kx4	45ns	225mW	10μW
IDT6116	2Kx8	~~70ns~~ 55 NS	200mW	20μW

*Separate Data I/O

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IDT7M164	64Kx1	70ns	250mW	40μW
IDT7M464	16Kx4	55ns	500mW	40μW
IDT7M864	8Kx8	85ns	325mW	80μW

DIGITAL SIGNAL PROCESSING. Our 16x16 multiplier applies all of the advantages of our CEMOS technology to DSP systems. The superior capabilities of our multiplier allow the use of high speed DSP designs in new applications such as video, robotics, speech synthesis and voice recognition. This is the first of a family of high performance CEMOS DSP circuits.

PART NO.	ORGANIZATION	SPEED (COM'L MAX)	POWER (TYP) OPERATING	STANDBY
IDT7216/ IDT7217	16x16 Multiplier	65ns	150mW	500μW

MEMORY SUPPORT LOGIC. Our new high speed memory support logic offers low power Schottky speeds at CMOS power levels. The first decoder products are in production now. A whole logic family will be available this year.

PART NO.	ORGANIZATION	SPEED (MIL MAX)	POWER (TYP) OPERATING	STANDBY
IDT54HCT138/ IDT72T338*	1-of-8 Decoder	20ns	15mW	5μW
IDT54HCT139/ IDT72T339*	Dual 1-of-4 Decoder	17ns	15mW	5μW

*Additional $\overline{CS}$ pins and select indicator output.

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COMPUTER SYSTEMS

Lisp machine fits under a desk; develops, runs AI programs

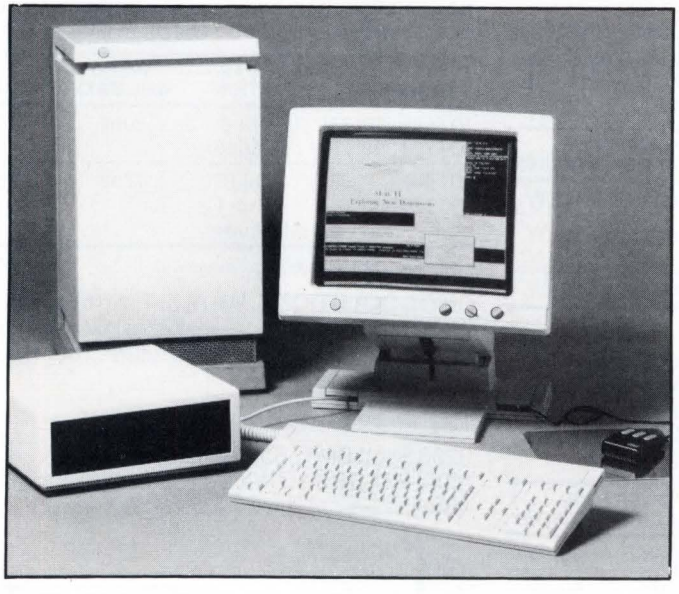
The full power of a Lisp machine to develop and run artificial-intelligence software has been shrunk down to fit under a desk. The 32-bit Explorer, from Texas Instruments, is a compact system standing a mere 25 in. high, 13 in. wide, and 18 in. deep, with seven slots for the various functional boards—namely, the processor, system interface, memory, and mass-storage controller, as well as an optional Ethernet controller.

Aside from the standard Lisp features, the Explorer has additional hardware for high-speed symbolic processings, such as bit-field circuitry for manipulating complex data structures; hardware-assisted memory management; and a 128-Mbyte virtual address space.

Heather Bryce

The processor board contains 16k 56-bit words of writable control store microprogrammed for rapid and efficient Lisp processing.

The system interface board contains a fiber-optic link to the monitor, keyboard, optical mouse, microphone, and headset. The display receives data from the system interface at 68 Mpixels/s. The board also contains graphics control logic that uses a 1-Mbit bit map built with 100-ns RAM. Included as well are a parallel printer and RS-232-C ports, clocks, timers, and power failure protection logic.



The first memory board to be offered holds 2 Mbytes of dynamic RAM; future boards will use 256-kbit RAMs to provide 8 Mbytes each. The access time is under 300 ns, and the complete system can accommodate 16 Mbytes.

One of the Explorer's two buses is TI's NuBus, a full 32-bit processor-independent bus with a 37.5-Mbyte/s transfer rate. A second 32-bit bus for fast movement of data between the processor, main memory, and the graphics bit map frees the NuBus for system-wide operations.

The user interface hardware is designed to be compact, as well as easy to use. For one, the 60-Hz noninterlaced monochrome screen is adjustable for height and tilt; it displays 1024 pixels horizontally by 808 vertically and is only about 15 by 12 in.

The keyboard has 111 keys,

COMPUTER SYSTEMS

including the standard typewriter, Lisp-specific, and cursor control keys. The optical mouse contains three buttons, primarily for menu selection and to move the cursor.

Since the console equipment leads to the chassis via a fiber-optic link, they may be placed up to 200 ft apart, allowing the user to more conveniently position the units.

Powerful software aids the user both in program development and in run-time operation. A help facility completes partially entered commands and make suggestions about next steps.

Program development tools include a ZMACS editor, which is both real-time and window oriented. Another tool, called a Lisp listener, facilitates direct user interaction with the interpreter, and compiler and debugging facilities are also included.

The stand-alone development model, the XP-7222, costs $61,000 and comes with the chassis, processor, system interface, mass-storage controller, a 2-Mbyte memory board, keyboard, monitor, two 112-Mbyte Winchester disk drives, and a 60-Mbyte cartridge tape backup.

The model XP-7212, not recommended for development, includes all the same hardware, except that it has only one 112-Mbyte Winchester drive. It costs $52,500.

Shipments are scheduled to start at the beginning of 1985.

Texas Instruments Inc., Data Systems Group, PO Box 402430, Dallas, Texas 75240; (800) 527-3500. **CIRCLE 303**

IBM's newcomer rivals PC's performance



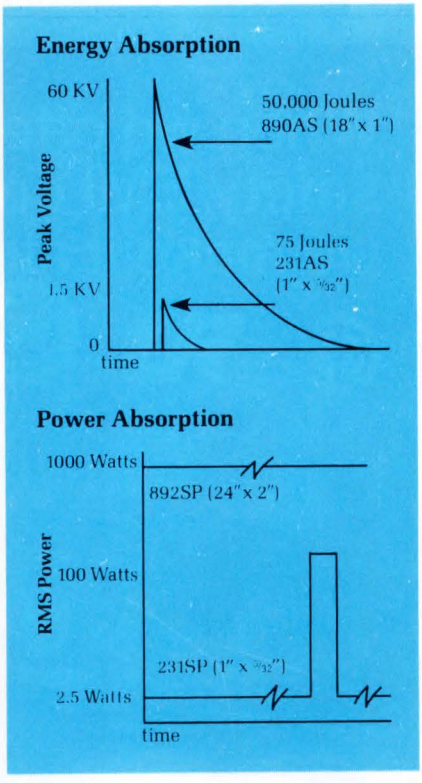
Boasting almost five times the user memory and more than twice the information storage capacity of the IBM PC, the top-of-the-line PC AT offers up to 3 million characters of dynamic RAM and 41.2 million characters of on-line storage. Moreover, in most cases, system performance is two to three times faster. Compatible with most existing IBM PC hardware and software, the 80286-based PC AT can be used as a single-user system or shared by up to three users. It can also be used with IBM's token-passing ring network, which can link up to 72 PCs.

The system is available in two configurations. A $3395 model includes 256 kbytes of RAM and a 1.2-Mbyte diskette drive. The second model, priced at $5795, offers 512 kbytes of RAM, a 1.2-Mbyte diskette drive, and a 20-Mbyte fixed-disk drive. Both models have an 84-key keyboard and eight expansion slots.

IBM Corp., Entry Systems Division, PO Box 1328, Boca Raton, Fla. 33432; (305) 241-7614. **CIRCLE 310**

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CIRCLE 106

COMPUTER SYSTEMS

Q-bus-based μC uses fast storage subsystem

Targeted at multi-user and data-base-intensive markets, the Q-bus-based MicroVIP combines an LSI-11/73 CPU (or a MicroVAX) with a fast storage architecture to provide optimum performance and capacity in a rack-mounted package only 5¼-in. high. The VIP mass-storage subsystem, based on a 190-Mbyte Winchester disk drive with a 128-kbyte adaptive cache control unit, offers an average access time of less than 18 ms. An optional 512-kbyte cache reduces access times to below 10 ms. Backing up the disk is a 100-Mbyte cartridge tape transport.

U.S. Design Corp., 5100 Philadelphia Way, Lanham, Md. 20706; (301) 577-2880. From $15,900. **CIRCLE 311**

Second member joins MicroPDP-11 family

Significant performance improvements and compatibility with the Micro PDP-11 are just two of the numerous features of the family's newest member, the MicroPDP-11/73. Based on the J-11 microprocessor chip set, the computer offers CPU performance comparable to the fastest 16-bit micros available today. In fact, CPU performance is three to five times greater than that of the MicroPDP-11.

The Q-bus-based computer supports all of the major PDP-11 operating systems, including the MicroRSX implementation of RSX-11-Plus and the Ultrix-11 implementation of Unix. It also features the same system packaging as the MicroPDP-11 and MicroVAX I to enable system configurations without repackaging.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754; (617) 264-1669. From $7800 (rack-mounted version) and from $15,140 (packaged systems); 60 days. **CIRCLE 312**

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CIRCLE 107

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SOLAREX

CIRCLE 108

INSTRUMENTS

Frequency standard holds drift to 10^{-11}/day, can use 2 external references

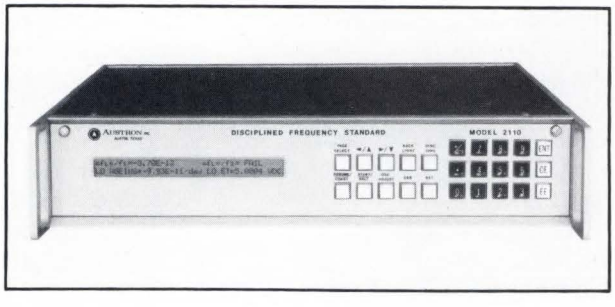
The first microprocessor-controlled frequency standard automatically locks the frequency of its ovenized quartz-crystal oscillator onto an externally applied reference of 1, 5, or 10 MHz (100 kHz optional) and drifts no more than 1 part in 10^{11} per day without an external reference.

Because it is microprocessor-controlled, the unit, called the 2110 disciplined frequency standard by its maker, Austron, offers several unique features. Probably the most important is the optional ability to make use of two references at the same time. Others are a third-order servo oscillator control system, an eight-character liquid-crystal display, continuous correction after the reference is removed, and an IEEE-488 interface.

Heather Bryce

By being able to handle two references at once, the 2110 ensures greater reliability than other frequency standards, since its ability to deal with noise is enhanced. For example, the primary/secondary mode uses the primary reference until a fault is perceived, at which time the 2110 will lock onto the secondary reference. In the statistical combination mode, both references are used at all times and statistical computations determine by weight which reference should be followed more closely. These modes also increase the overall reliability of the system.

Thanks to its highly precise ovenized crystal-controlled oscillator, the standard also has impressive open-loop performance. Its guaranteed drift rate of 1 part in 10^{11} per day after the external reference fails or is removed contrasts sharply with a guaranteed rate of less than 5 parts in 10^{11} per day for other units.



The microprocessor performs third-order integration, creating a third-order servo oscillator control system. Other systems stop at first- or second-order integration control. (This system accuracy is the key to continuous correction of the oscillator frequency even with the external reference removed.)

The LCD, which replaces the traditional meter, shows such information as statistical measurement and status parameters, making it easy to detect a failure. It also prompts the user for the inputs required and shows multiple pages that the user may scroll up and down. Function switches and a front-panel keyboard program the display.

The frequency standard is available in 120 days and costs $8700. The dual-reference input costs $1300, and the 100-kHz sine-wave output option $1000.

Austron Inc., PO Box 14766, Austin, Texas 78761; (512) 251-2313. **CIRCLE 308**



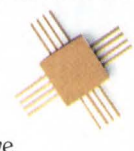
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☐ 5 INPUT NAND/AND GATE: HMD-11104-2
☐ 5 INPUT NOR/OR GATE: HMD-11101-2
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For your information our name is Harris.

HARRIS

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Because it is the first erasing system designed to remove both lead and ink lines from paper and film!

The new Koh-I-Noor 2800 Electric Erasing System is the only eraser designed to provide engineers, drafters and artists with the means to cleanly remove graphite lines from most drawing papers and ink or polymer lead lines from polyester-base films.

The system consists of eraser unit with replaceable collet, three #287 white strips for graphite and two #285 imbibed yellow strips for ink. The package sells itself, too! Unit may be used to power a precision lead pointer attachment available as an optional accessory.

The maintenance-free motor is quiet, air-cooled and designed with a hollow shaft to accept full 7″ eraser strips from either end. White Lexan® case, with broad finger-tip switch, needs no grounding.

For details, contact your Koh-I-Noor dealer, or write to Koh-I-Noor for more information and the names of dealers in your area.

Koh-I-Noor Rapidograph, Inc.
Bloomsbury, NJ 08804
(201) 479-4124
In Canada: 1815 Meyerside Dr.
Mississauga, Ont. L5T 1G3
(416) 671-0696



KOH-I-NOOR
RAPIDOGRAPH®

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CIRCLE 110

INSTRUMENTS

Two-channel synthesizer generates independent dc-to-13-MHz signals



For applications requiring two signal sources spanning dc to 13 MHz, the HP 3326A delivers two independent signals, two signals related in phase or frequency, or one coordinated signal. By combining two synthesizers, flexible modulation, and control circuitry into a single instrument, the HP 3326A can replace custom test systems comprising several instruments.

Each channel of the HP 3326A produces sine and square waves with independent control of amplitude and dc offset. Two-phase, two-tone, and pulsed signals are generated from the instrument's front panel. A harmonic distortion of −80 dBc for signals below 100 kHz (less than −65 dBc for signals in the range of 100 kHz to 1 MHz) is the result of the HP 3326A's frequency-offset tracking, internal signal combining, and amplitude and phase modulation capabilities.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303; call local sales office. $9200; 10 weeks.

CIRCLE 313

Hardware-software kit transforms IBM PC into data-line monitor

With the use of a hardware-software package, the IBM PC can assume the role of a programmable data-line monitor. The package—Metascope-PC—permits real-time data/status recording to diskette, line monitoring to 19,200 bits/s, external or internal synchronous clocking from 75 to 19,200 bits/s, automatic baud detection, pre- and post-triggering, trigger event counting, and idle suppression. In addition, data may be displayed in ASCII,

INSTRUMENTS

EBCDIC, hexadecimal, baudot, or other user-defined formats. The computer can be programmed to trigger on pattern match or on change of signal state, to split channel speeds, and to monitor and display the more commonly used EIA signals. The Metascope-PC, which includes a printed circuit board, documentation, and all of the necessary software, can also emulate a host computer to simulate line traffic.

Metatek Inc., 410 93rd Ave. NW, PO Box 33129, Minneapolis, Minn. 55433; (612) 786-8253. $2500 (fall). **CIRCLE 314**

Instrument measures both radiant energy and luminance



Finding application in such areas as laser-power and optical-transmission measurements, the Model S360 autoranging radiometer/photometer is capable of making linear and logarithmic measurements over a spectral range of 200 to 1800 nm. The instrument has a sensitivity of 10^{-12} W, −90 dBm, with automatic ambient/zero compensation and built-in calibration verification. Its four different calibration settings are selected via push buttons on the front panel to permit fast switching among the various units of power and luminance.

The Model S360 also features analog and digital outputs, a voltage comparator, and a backlit 3½-digit LCD readout. Powered by rechargeable batteries, the meter is particularly convenient for use in portable applications. The instrument is compatible with a line of photodetectors, including UV-enhanced detectors for measurements down to 200 nm and germanium detectors for measurements up to 1800 nm.

United Detector Technology, 12525 Chadron Ave., Hawthorne, Calif. 90250; (213) 978-0516. **CIRCLE 315**

Why is the new KOH-I-NOOR® 285 not like other eraser strips?



Because it is specially imbibed for erasing ink and polymer lead from drafting film — a KOH-I-NOOR exclusive!

The new Koh-I-Noor 285 Imbibed Yellow Eraser Strip is manufactured with microscopic drops of erasing fluid imbibed throughout the molecular structure of a vinyl base. Erasing action releases fluid to soften ink and polymer lead lines, then lifts residue without ghosting or marring film surface.

The 285 Imbibed Yellow Eraser Strip makes possible faster, cleaner updating of original drawings for high-quality reproduction, and is especially useful for softening and removing hard-set ink to make changes on long-stored drawings. Strips are available in boxes of 10 each, and are also included with each Koh-I-Noor 2800 Electric Eraser as part of an exclusive, total lead/ink erasing system. Strips will fit most other types of electric erasers.

For details, contact your Koh-I-Noor dealer, or write to Koh-I-Noor for more information and the names of dealers in your area.

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Bloomsbury, NJ 08804
(201) 479-4124
In Canada: 1815 Meyerside Dr.
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CIRCLE 111

POWER

Switching power supplies occupy 6 in.^{3} yet deliver 7.5 W

Two extremely low-power switching power supplies, one putting out 5 W and the other 7.5 W, come in exceptionally compact packages: 4.36 by 2.16 by 0.64 in.

The two units, from Theta-J, operate at a switching frequency of 300 kHz, the highest ever employed by off-the-shelf supplies. This switching frequency is the principal contributor to the supplies' small size, since it allows for a shrinking in the filter components.

The 5-W unit, the P5AG, has two floating outputs, 5 and 26 V; the 7.5-W P5ADD, three outputs, +5 and ±12 V, with a common ground. Both devices, members of the MicroSwitch mode series, provide 1500-V peak input-to-output isolation and are rated at a minimum efficiency of 70%. The ac input voltage is 90 to 130 V ac, 47 to 440 Hz, and an internal 3-A ac line filter is provided.

Gary Elinoff

The P5AG provides 5 V at 0.25 to 1.0 A and 26 V at 0.01 to 0.1 A. For all allowable line and load variation, as well as setting tolerance, the maximum deviation is ±5% for the 5-V output and −5% to +20% for the 26-V output. The combined ripple and noise is 100 mV and 300 mV pk-pk maximum, for the respective outputs.

The P5ADD is rated at 0.25 to 1.0 A at 5 V and at 0 to 0.1 A on both its 12-V outputs. The maximum deviation for all conditions is ±5% on all three outputs. The combined ripple and noise is 100 mV and 50 mV pk-pk maximum on the 5-V and the 12-V outputs, respectively.

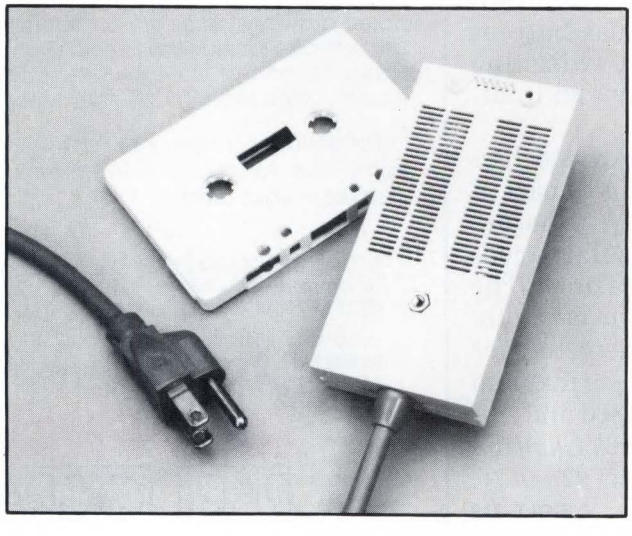
Both units incorporate RFI filtering meeting both conducted and radiated FCC Class A requirements. Additionally, they are UL-recognized and CSA-certified.

The power supplies are fully enclosed in plastic, with a 6-ft ac line cord attached; both units can be mounted on a pc board or in a frame. Output voltages are available from an output connector designed for plugging in to a board-mounted socket.

In lots of 1000, the P5AG costs $27.50 and the P5ADD $29.95. Delivery is in six to eight weeks for moderate production quantities.

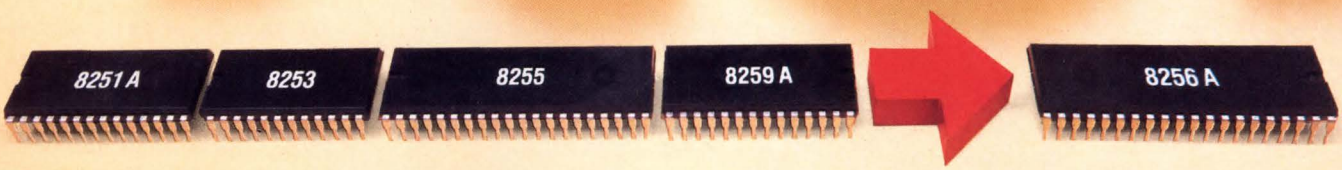
Theta-J Corp., 8 Corporate Place, 107 Audobon Road, Wakefield, Mass. 01880; Jim Emergy, (617) 246-4000.

CIRCLE 301



SIEMENS

4 to 1



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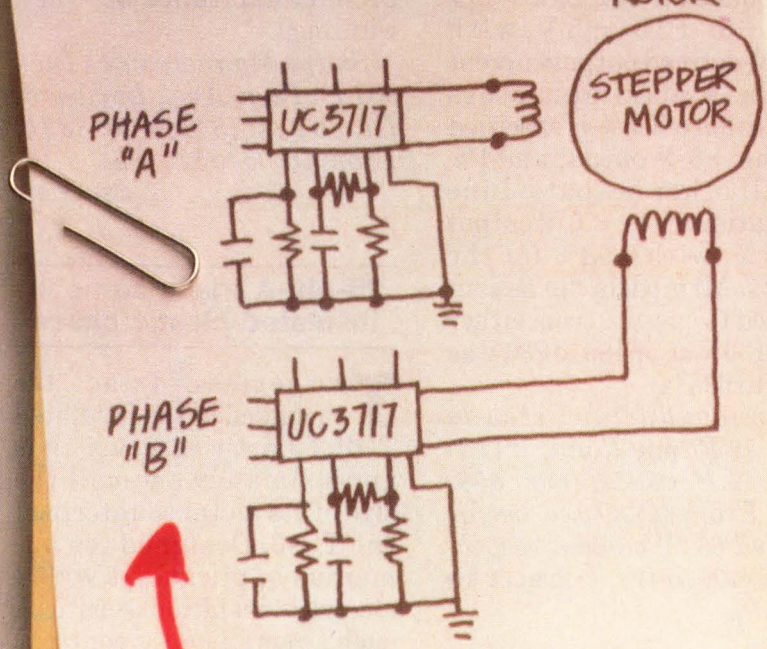
All the difference in the world

Registry: British

CIRCLE 139

To Joe: Great! New Stepper Motor Drive IC from Unitrode

HERE'S HOW IT WORKS—
Two UC3717's and a few external components form a complete control and drive unit for LST, TTL or microprocessor controller stepper motor systems.



Problem

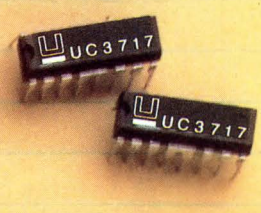
Find a complete stepper motor drive IC that runs cool, improves efficiency, operates up to 1 amp and is cost-effective.

Solution:

Unitrode's new UC3717 is the answer. This IC has built in schottky clamping diodes, a wide range of current - up to 1 amp and can be used for 1/2 step and full step applications.

PS. U.S. supplier, too!

— Ron



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Samples and data sheets available from the following Unitrode Field Offices: Boston 617-245-3010; New York 516-271-3110; Tampa 813-932-5807; Chicago 312-394-5240; Dayton 513-294-1364; Dallas 214-231-8700; Los Angeles 213-705-8085; 714-730-1077; San Jose 408-294-4210.

POWER

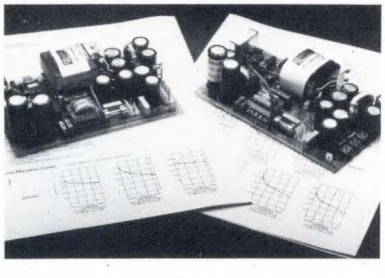
Thyristors handle 100 to 1300 A

Delivering symmetrical blocking voltages of up to 2000 V, the DK and TF series of thyristors cover a range of current ratings from 100 to 1300 A. The fast-switching thyristors are designed for industrial use in motor controls, inverters, converters, and in high-frequency welding and related applications. The devices have turn-off times as low as 40 μs when blocking 2000 V. Furthermore, the high performance is achieved while obtaining reductions in unit size, weight, and cost. The thyristors are available in both stud and hockey-puck housings and, in quantities of 100, are priced from $44 per unit for the lower-current models.

Thomson Semiconductors, Discrete Components Group, 6660 Variel Ave., Canoga Park, Calif. 91303; (818) 887-1010. Sixteen weeks.

CIRCLE 316

Switchers feature MTBF of > 100,000 hours



A family of 50- and 65-W switching power supplies, with triple and quad outputs, offers ten models that boast a verified minimum MTBF of 100,000 hours. An operating efficiency of 75% over the entire input range further enhances the CF series' reliability.

Fixed voltage output combinations include triples of +5/±12 V and +5/±15 V and quads of +5/±12/−5 V and +5/±15/−5 V, with model-defined output current levels. A maximum cross regulation of 0.5% is specified for the +5-V output and 1% for all other outputs. Line regulation of the +5-V output is 0.1%, with 0.03% for the others. All models can be configured to operate from either 90 to 130 V ac or 180 to 230 V ac at 47 to 63 Hz.

Semiconductor Circuits Inc., 49 Range Road, Windham, N.H. 03087; (603) 893-2330. From $44.30 and $58 for 50- and 65-W models, respectively (100 units). CIRCLE 317

Unit conditions 3-phase power lines

The Z-Phase Line Tamer, a computer power conditioner, brings the low cost and high performance of ferroresonant transformers to three-phase applications for both line-to-line and line-to-neutral loads. To eliminate oscillation between phases, the unit shares the load among all three transformers in the three-phase system. Typically, only two transformers are used. The Line Tamer's design precisely matches inductance and capacitance to prevent oscillation from reaching shutdown levels.

The standard product is designed for loads from 7.5 through 74 kVA. Line-to-line regulation is ±5% over a regulating range of +10%, −20%, with load unbalances of up to 30% of the average total load. Isolation is 0.001 pF of capacitance between windings.

Shape Magnetronics Inc., 901 DuPage Ave., Lombard, Ill. 60148; (312) 620-8394. From $3400 to $24,000.

CIRCLE 318

25-/40-A triacs come in insulated plastic cases

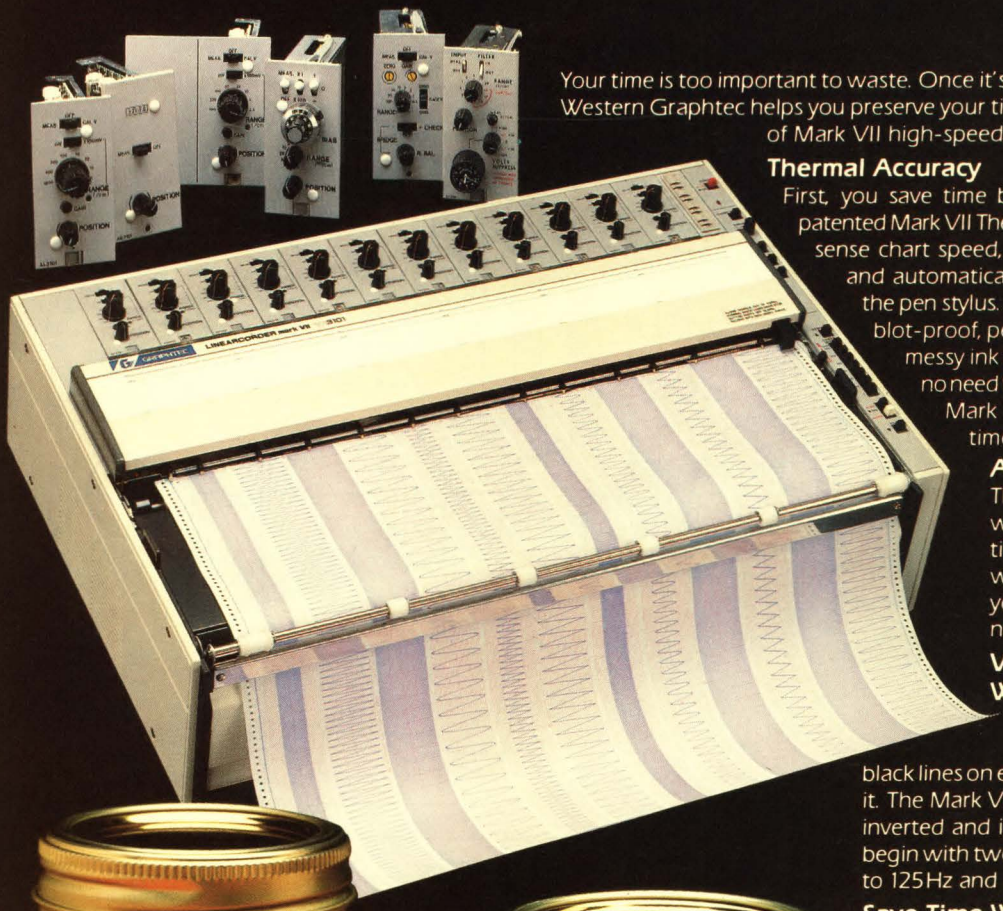
Two series of triacs are packaged in the insulated TOP 3 plastic case, which is approximately one-half the size of its metal counterpart the TO-3. Designed for numerous applications where electrical isolation is critical, such as small motor controls, the units offer a compact, low-cost alternative to triacs housed in the noninsulated TO-3 case. The BTA 26 and BTA 41 series triacs feature a copper frame that provides a thermal resistance of less than 1°/W.

The BTA 26 and BTA 41 each feature a voltage range of 200 to 700 V at 25 and 40 A, respectively, and can handle high current surges. The 25-A triac withstands a peak current surge of 300 A; the 40-A device handles 400 A peak.

Thomson Semiconductors, Discrete Components Group, 6660 Variel Ave., Canoga Park, Calif. 91303; (818) 887-1010. $3.36 (100 units).

CIRCLE 319

Preserve Your Time With Our Thermal Line



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First, you save time by getting sharper, cleaner lines with our patented Mark VII Thermal Pen. Its microprocessor patented circuits sense chart speed, signal velocity, and ambient temperature, and automatically regulate the current that goes through the pen stylus. This guarantees you sharp, constant density, blot-proof, permanent presentations of charted data. No messy ink smears. No time-consuming clean-up. And no need to re-run your data. With Western Graphtec's Mark VII oscillographs you get it right the first time. And that saves you time.

Automatic Digital Annotation

The Mark VII preserves your time in more ways than one. Its automatic Digital Annotation records the data and time for you, along with the record number and chart speed. So you never have to go back and waste time noting them yourself.

Versatility When and Where You Need It

Fourteen, highly accurate, push-button chart speeds give you sharp, clean blue or black lines on either roll or Z-fold charts wherever you need it. The Mark VII can be operated vertically, horizontally or inverted and is not motion or altitude sensitive. You can begin with two channels and field install up to 12, from DC to 125Hz and choose from a wide range of pre-amplifiers.

Save Time With Western Graphtec

You save time by choosing the right equipment with the help of Western Graphtec. Highly skilled design engineers will talk over your exact specifications and match your specific needs with our wide range of instrumentation devices. Save time with built-in, pre-tested reliability. But, should you ever need service, save time with our free "loaner" while our Service department provides prompt service.



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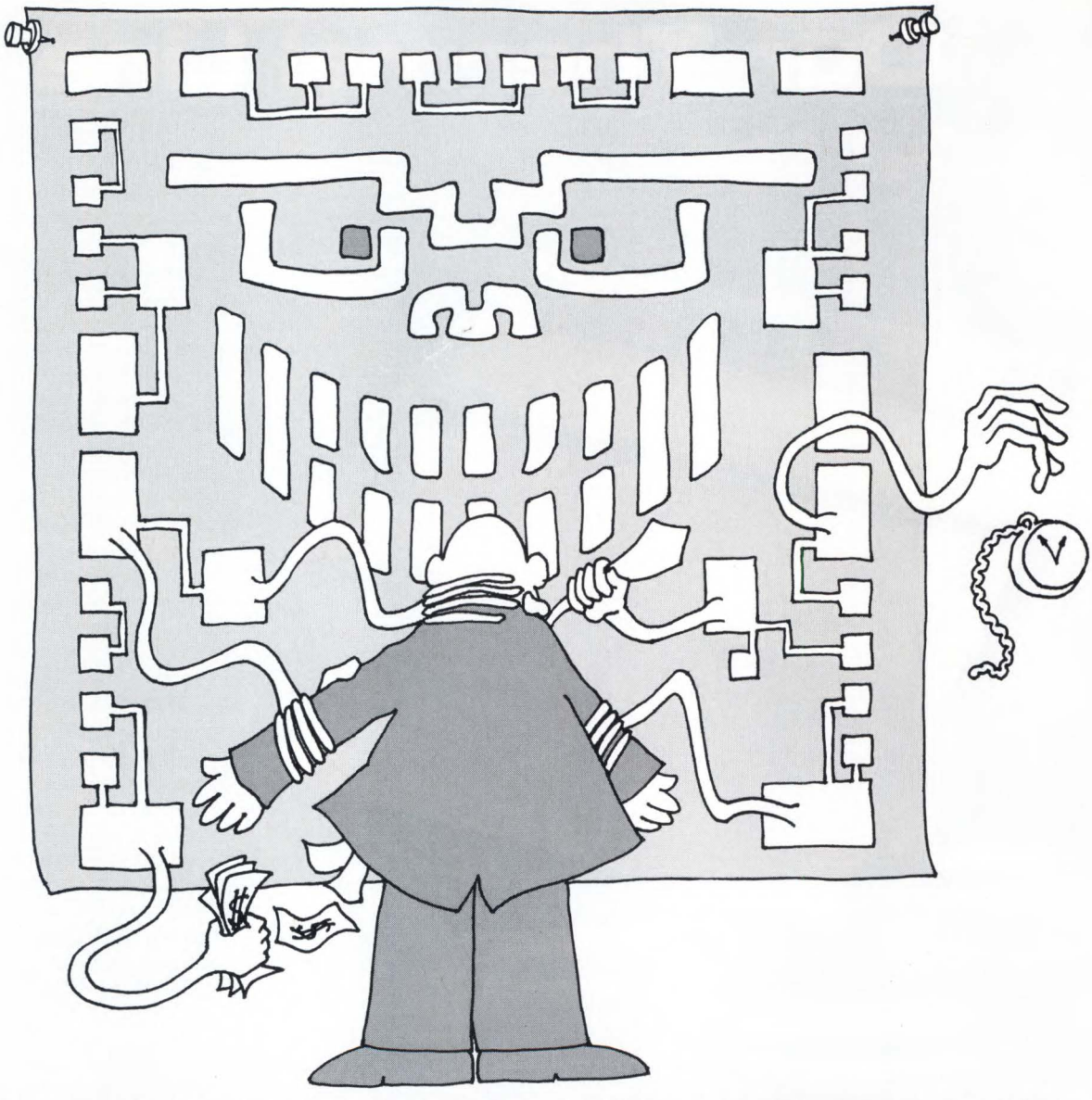
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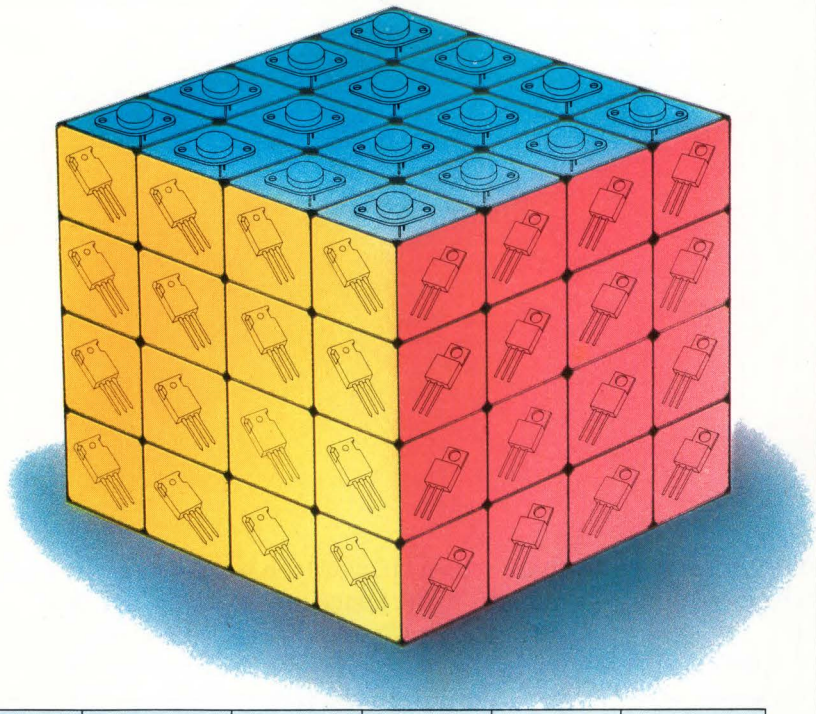
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CIRCLE 114

General Instrument solves the most puzzling power supply problems.

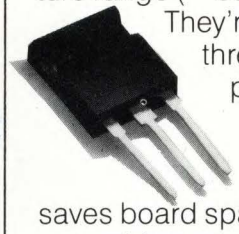


Part Number	V_{RM} Volts	$I_{F(AV)}$ Amperes	t_{rr} N sec	VF Volts	Package Type*
FE8	50-200	8	35	.95	TO220
	300-600	8	35	1.20	
FE16	50-200	16	35	.95	TO220
	300-600	16	35	1.20	
FEP30	50-200	30	35	.95	TO3P
	300-600	30	35	1.20	
FE30	50-200	30	35	.95	TO3
	300-600	30	35	1.20	

*Available in negative center tap and doubler configurations.

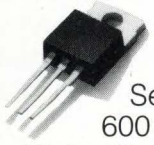
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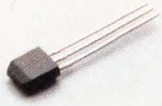
For detailed literature, samples and applications engineering information write or call General Instrument Corporation, Discrete Semiconductor Division, 600 W. John Street, Hicksville, NY 11801 (516) 933-3713.

General Instrument Corporation: Our continued attention to rectifier development has made us an industry leader in high voltage ultra fast switching devices.

GENERAL INSTRUMENT

CIRCLE 115

When you order a Hall effect sensor, is this all you get?



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If you want to purchase only a basic sensor—or want to package the complete sensor yourself—you could choose a product such as the one above. Or you can select from our wide variety of sensor packages like those shown below which we can modify to your designs. We'll change the size of the ceramic substrate. Provide a holder for the sensor. Attach leadwires. Form terminals. Give you multiple sensor packages. To name a few.

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So talk with the Sensor Consultants at MICRO SWITCH. After all, you should get a sensor that's ready to work. Instead of one that's ready to work on.

For more information on our Hall effect products and customization capabilities, or the location of a sales office or Authorized Distributor near you, call 815-235-6600. Or write MICRO SWITCH, Freeport, IL 61032.



Together, we can find the answers.

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CIRCLE 116

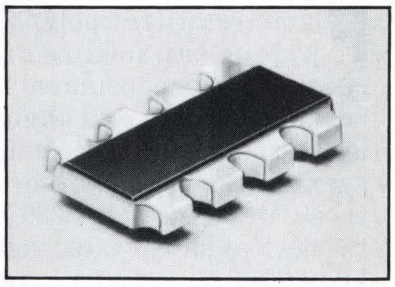
COMPONENTS

Resistor array hybrid saves board space

The first surface-mountable resistor array puts as many as eight resistors in less space than that needed for a single standard component. Rohm's hybrid IC consists of a leaded set of two-, four-, or eight-resistor arrays.

The package is designed for reflow (infrared or vapor-phase) soldering and features a notched spacing between the leads to prevent bridging, a common problem. It can also be wave-soldered.

The resistors, available as individual surface-mountable chips, are built up on an alumina substrate by successive



coatings of ruthenium oxide, laser-trimmed, and then glass-passivated.

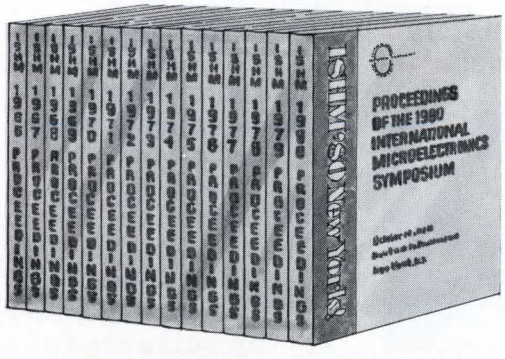
Highly reliable, the arrays have a defect rate of less than 20 ppm. Their resistance values run from 100 Ω to 330 kΩ, with tolerances to +5%; dissipation is 1/32 W at 70°C and 12 V. They operate between −10° and +125°C and have a temperature coefficient of ±200 ppm/°C.

The CRA8 eight-resistor pack is 10.7 mm long, 3.2 mm wide, and 0.55 mm high. The others differ only in length: the two-resistor CRA2 is 2.7 mm, the four-resistor CRA4 is 5.2 mm.

Mechanical samples are available now, electrical samples will be ready in December, and deliveries are set for the first of the year. The CRA8 unit costs 80¢ apiece in quantities of 1000.

Rohm Corp., 8 Whatney, Irvine, Calif. 92718; (714) 855-2131. **CIRCLE 305**

THE MOST PRACTICAL REFERENCE GUIDE TO MICROELECTRONICS



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For the first time the International society for Hybrid Microelectronics (ISHM) will make available its Annual Symposium Proceedings for each year going back to 1966. That's 15 Annual Proceedings. You can buy the 1980. Each of the last 2 years. 3 years. 4 years. Etc. Or a complete set of the last 15 years.

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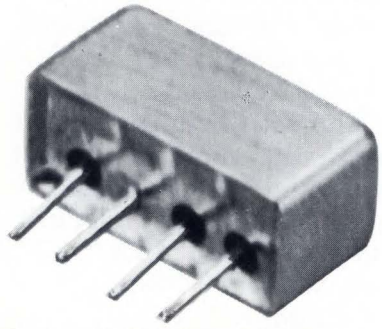
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hi level (+17 dBm LO)



5 to 1000 MHz
only $31.95 (5-24)

IN STOCK . . . IMMEDIATE DELIVERY

- **micro-miniature, pc area only 0.5 x 0.23 inches**
- RF input up to +14dBm
- guaranteed 2 tone, 3rd order intermod 55 dB down at each RF tone 0dBm
- flat-pack or plug-in mounting
- low conversion loss, 6.2dB
- hi isolation, 40 dB
- MIL-M-28837/1A performance*
- one year guarantee

*Units are not QPL listed

TFM-2H SPECIFICATIONS

FREQUENCY RANGE, (MHz)			
LO, RF	5-1000		
IF	DC-1000		
CONVERSION LOSS, dB		TYP.	MAX.
One octave from band edge		6.2	7.0
Total range		7.0	10.0
ISOLATION, dB		TYP.	MIN.
low range	LO-RF	50	45
	LO-IF	45	40
mid range	LO-RF	40	30
	LO-IF	35	25
upper range	LO-RF	30	20
	LO-IF	25	17

SIGNAL 1 dB Compression level +14 dBm min

finding new ways . . .
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
World's largest manufacturer of Double Balanced Mixers
2625 E. 14th St. B'klyn, N.Y. 11235 (718) 769-0200

C 82-3 REV.B

CIRCLE 118

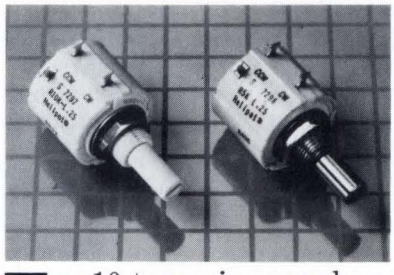
COMPONENTS

Capacitors resist humidity and chemicals

Flame-retardant polypropylene capacitors are epoxy-resin encapsulated to resist humidity and chemicals, especially such cleaning agents as Freon and Chlorothene. Designated as B33074, the devices have a rated voltage of 100 V dc and a rated capacitance of 2200 pF. They are also specified for operation over the temperature range of −40° to +85°C. The axial-leaded capacitors are suitable for use in rf tuned circuits, particularly i-f and carrier-frequency filters for telecommunications. The capacitors are also useful in printed circuit board applications.

Siemens Components Inc., 186 Wood Ave. S., Iselin, N.J. 08830; (201) 321-4842. Approximately $0.20 (1000 units); 12 to 14 weeks. **CIRCLE 320**

10-turn potentiometers are economical



Two 10-turn wirewound potentiometers pack high performance levels and low cost in a convenient 3/4-in.-long, 7/8-in.-diameter package. The Model 7296, which has a metal shaft and bushing, and the Model 7297, which has a plastic shaft and bushing, offer standard resistances of 100 Ω to 100 kΩ and a +5% resistance tolerance. The power rating for each device is 2 W, with an independent linearity of ±0.25%. A life expectancy of 1 million shaft revolutions and an ambient temperature range of −55° to +125°C further enhance the parts.

Beckman Industrial Corp., Electronic Technologies Division, 2500 Harbor Blvd., Fullerton, Calif. 92634; (714) 773-8080. $5.53 (7296) and $5.08 (7297) in quantities of 100; stock. **CIRCLE 321**

Keyboard switch is illuminated

Designated the SMK 0700, a conductive rubber switch for use in keyboards is illuminated with a long-life 5-V, 60-mA incandescent lamp. The component offers tactile feedback, with an operating stroke of 0.020 in. and a maximum operating force of 6.6 oz. The momentary-action switch has a life span of 5 million cycles (at no load) and is rated for 5 V dc at 10 mA. Contact resistance is 200 Ω maximum. The operating temperature range is specified from −10° to +50°C. Sporting an acrylic keytop suitable for hot-stamped or engraved legends, the SMK 0700 switch body is constructed of Noryl, the base of PBT, and the terminals of gold-plated phosphor bronze.

Shelly Associates Inc., 2942 Dow Ave., Tustin, Calif. 92680; (714) 544-9970. $1.94 (100 units); stock. **CIRCLE 322**

COMPONENTS

Relays come in SIPs, DIPs, DDIPs

Utilizing industry-standard in-line pinouts, a line of ac solid-state relays is available in SIP, DIP, and double-wide DIP configurations. With the new packaging, CAD/CAM designers can now include SSRs in their software libraries. Not only does the in-line-packaged device afford a cost savings over standard relays, but the solid-state relay offers a tenfold life expectancy as well. They also provide greater design flexibility for specialized applications in robotics and industrial process control. To encourage new applications in these markets, the SSR line is available in a variety of designs, including ac or dc inputs and normally open or normally closed, 60- and 400-Hz ac outputs.

Electronic Instrument & Specialty Corp., 42 Pleasant St., Stoneham, Mass. 02180; (617) 438-5300. **CIRCLE 323**

LED connector eliminates hard wiring

To solve the problems that arise from wiring panel-mounted LEDs—such as damaged or broken leads from soldering or wire wrapping—the Conxrite solderless connector makes a positive press-fit connection with either a Cliplite lens-mounted or a clip-and-ring-mounted LED. It also supports the LED leads to relieve the stress and vibration experienced during transport. The connector's molded plastic body contains an interchangeable 1/4-W resistor, which eliminates the need for an external resistor. It can be used on circuits requiring from 3 to 28 V, and its wiper-type contacts compensate for varying sizes of LED leads.

Visual Communications Co., PO Box 986, El Segundo, Calif. 90245; (213) 822-4727. $0.34 (10,000 units); stock to two weeks. **CIRCLE 324**

Teltone IC's

Covering the full spectrum of your telecommunications needs.

Solve your telecommunications design problems with Teltone's complete family of telecom IC's. You'll find innovative, up-to-the-moment single-chip and hybrid generators, detectors, receivers and relays — all backed by Teltone's commitment to performance, reliability and quality.



Leading the industry in DTMF technology. Consider the M-957, a monolithic 22-pin CMOS DTMF receiver. It needs fewer support components, so designs can be simple and use a minimum of space. The new M-958 is a hybrid PCM-compatible DTMF receiver that is dial tone immune and packs μ-Law or A-Law PCM input at up to 3 MHz into a single 22-pin package.



Designing the *first* call progress IC's. Need to monitor for or generate dial tone, circuit or station busy, audible ringing and other call routing tones? Take a look at our exciting 8-pin CMOS M-980 Call Progress Tone Detector or our unique new 14-pin CMOS M-991, the only Call Progress Tone *Generator* on the market. If you require *precise* detection of the four common call progress tones (350, 440,480 and 620 Hz), Teltone has a 22-pin CMOS solution for you called the M-982.



A reputation for telecom innovations. Rounding out our complete family of telecommunications components are the M-949 Line Sense Relay and the M-959 Dial Pulse Counter and Hook Status Monitor. The M-949 is a small PWB-mount loop current detector that, when connected to the tip and ring voice pair of an ordinary telephone line, responds to currents of 18-125 mA with a 1 form A relay closure. The low-cost, low-power CMOS M-959 features independent hook status monitoring and includes time-guarded dial pulse counting and pin-selectable dialing speeds of 10 or 20 PPS.

For more information on components from the leader in telecom technology, call Teltone today: **1-800-227-3800, ext. 1130.**

TELTONE®

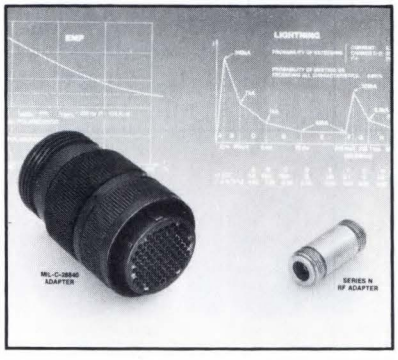
Teltone Corporation, the telecommunications company. P.O. Box 657, Kirkland, WA 98033. In the east call: Teltone Corporation, (904) 262-6910. In Canada, contact: Teltone Ltd., 183 Amber Street, Markham, Ontario L3R 3B4, (416) 475-0837.

CIRCLE 119

Connector knocks out EMP

An arrestor for coaxial and multileaded transmission lines protects sophisticated telecommunications equipment from electromagnetic pulses (EMP) caused by anything from static discharges to lightning and nuclear blasts.

At the heart of ITT Cannon's transient voltage suppressor is a junction diode that is an integral part of each connector pin, not a wired-in add-on component, as is usually the case. (The device suppresses pulses by being forced from a standby condition into an avalanche condition.) As a result, lead inductances are drastically reduced and transients are shunted through the diodes to the connector's housing in less than 1 ns.



The arrestor can dissipate an instantaneous pulse power of 500 W at 25°C. It is available in a MIL-C-28840 adapter or in an n-type rf connector.

Pricing is a function of the pin configuration; the typical cost is $3 per contact for orders of 1000 units or more.

ITT Cannon, 2801 Airlane, Phoenix, Ariz. 85034; (602) 275-4792. **CIRCLE 302**

Unit tests memory and gate performance



Suitable for incoming inspection and production testing, the Model AT700 access-time tester measures the access times of static RAMs, ROMs, and PROMs and the propagation times of PALs, gates, and cables. The unit features 1-ns resolution over the entire measurement range of 0 to 390 ns. Absolute accuracy is within ±2 ns from 0 to 60 ns and within ±5 ns from 61 to 390 ns. Test mode, pass/fail limits, check sum values, memory size, and other parameters are entered via the front-panel keyboard and may be stored in nonvolatile memory. Although the easy setup and low cost of the portable tester make it ideal for small-quantity testing, an RS-232-C interface is available to accommodate high-volume applications.

Hilevel Technology Inc., Irvine Technology Center, 18902 Bardeen Way, Irvine, Calif. 92715; (800) 445-3835 or (714) 752-5215. $2850; 30 days. **CIRCLE 355**

Vision system frees pc board inspectors

Relieving workers from the tedious task of inspecting printed circuit boards, the IRI PCB256 vision system's single camera scans a 24-by-36-in. work area at 20 in./s—five to ten times faster than its human counterpart. The machine inspects 100 lead insertions per second, covers 4^2 in./s per image, identifies board serial numbers at 20 char/s, inspects hole registration at 100 ms/hole, and inspects part orientation, presence, and absence at 50 ms/part (with four to 16 features per part).

Two terminals monitor and control the inspection system: a control panel and display and a parts-file access terminal. Software includes the Q-See inspector program and a parts-file data manager. The latter enables the operator to input parts data and allows the system to make use of enhanced gray-scale capabilities.

International Robomation/Intelligence, 2281 Las Palmas Drive, Carlsbad, Calif. 92008; (619) 438-4424. $4800.

CIRCLE 356



NOW THOUSANDS OF CALIFORNIA OEM'S AND SYSTEMS INTEGRATORS FOCUS ON JUST ONE SHOW.

And so can you...on Mini/Micro West.

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CIRCLE 120



New From TRW Microwave . . .

Extremely Fast Switching, Low Barrier Schottky Diodes

- Low Capacitance – < 1.0 pF @ 0V
- Low Barrier – < .30 V @ 1 mA
- Low Leakage – < 100 nA @ 10V
- Guard-Ring Protected
- Very Fast – < 100 psec lifetime

TRW Microwave offers new guard-ring, fast switching Schottky diodes for wave shaping, A/D converting, clamping, and general purpose switching. These replace A2S835 (HP 5082-2835), 1N5711/12.

PART NUMBER	CASE	V_{BR} VOLTS	C_{TO} pF	1 mA V_F max VOLTS	I_F min @ 1V, mA
A2S830	Glass	20	1.1	0.32	50
A2S836	Glass	10	1.0	0.34	50
A2S832	Glass	15	3.5	0.30	200
A2S032	Chip	20	1.2	0.32	50
A2S033	Chip	10	0.9	0.34	50
A2S035	Chip	15	4.0	0.30	200

Also from TRW Microwave's Semiconductor Group . . .

- Schottky chips and glass package diodes –1N5711, 1N5712, 1N5165
- PIN Diodes – 1N5719, equivalent to HP 5082-3188
- Planar Back and Tunnel Diodes
- JAN, JANTX also available

TRW Microwave, 825 Stewart Drive, Sunnyvale, CA 94086. Telephone: 408.732.0880
TWX: 910-339-9207

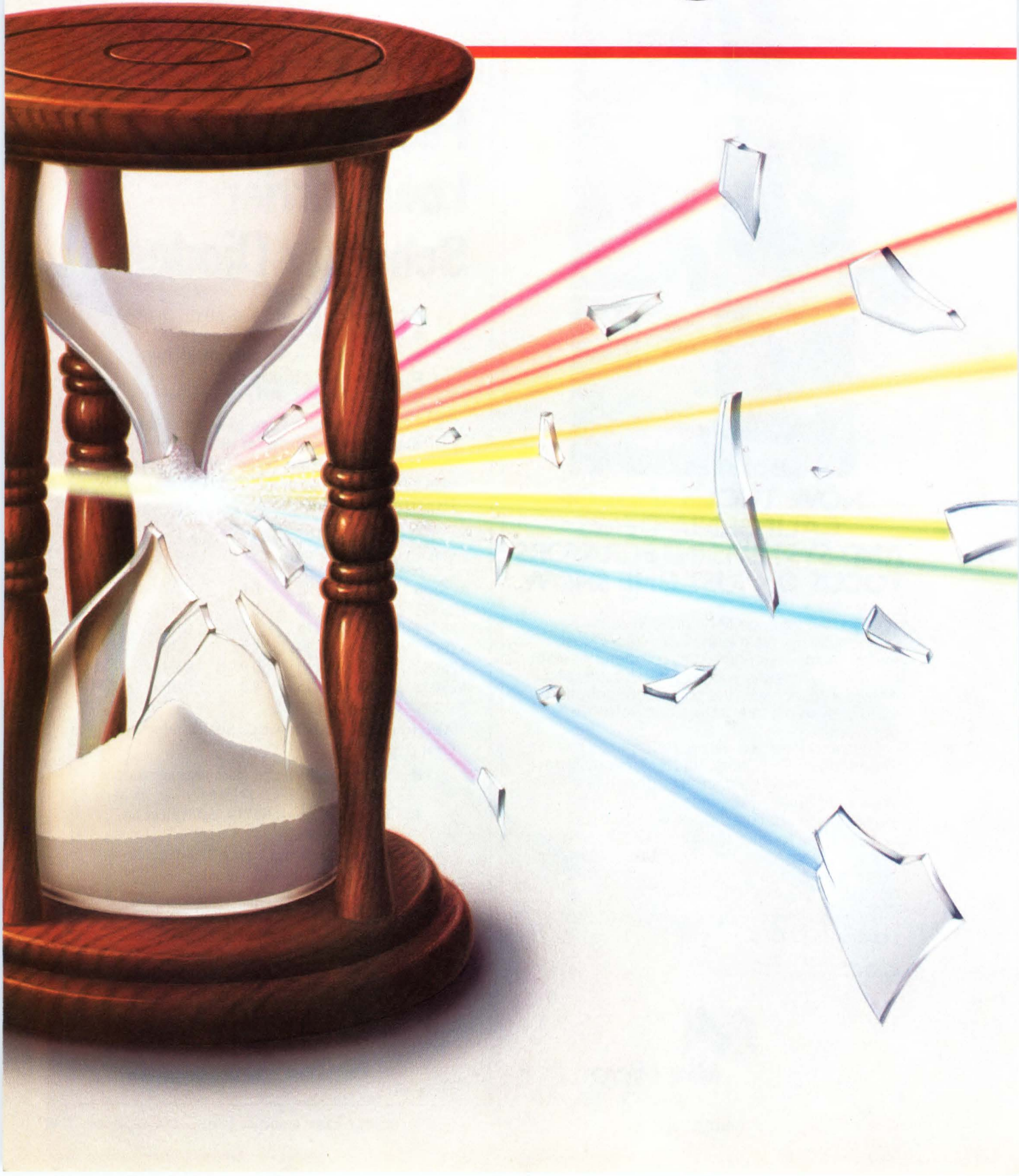
TRW

TRW Microwave

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CIRCLE 123

ZYCAD
Break Through The



Logic Evaluators™ Simulation Bottleneck

Today's complex I.C.s demand increasingly sophisticated engineering designs. These in turn call for increasingly complex design simulation and verification. And until now, that has meant lost time, expensive product reruns and lost marketing opportunities — in short, a product development bottleneck.

Your Fastest Source For Logic Simulation. By Up To 1000 Times.

Zycad's series of Logic Evaluators are not workstations or software simulators. They are dedicated, simulation hardware processors that eliminate the compute-intensive bottleneck. The Logic Evaluators have established new standards in simulation performance, verifying complex I.C. designs at speeds up to 1000 times faster than anything else available.

*EPS is the number of output state changes processed in one second.

Zycad Logic Evaluator Performance and Features

SPEED RANGE

Events Per Second-
200,000 upgradable to
16,000,000

Gate Evaluations Per Second-
500,000 upgradable to
40,000,000

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Number of Gates-
25,000 upgradable to
1,600,000

- Event-Driven
- Switch Level Simulation
- Gate Level Simulation
- Functional Simulation
- Assignable Gate Delays

Enhance Your CAD Investment.

A Zycad Logic Evaluator will interface with your existing system to provide benefits you've never before achieved through simulation:

- IMPROVED SPEED - Verify designs in seconds rather than hours with supercomputer pipeline architecture and parallel processing to 16 million events per second (EPS)*.
- IMPROVED CAPACITY - Verify a single chip, components or an entire system.
- IMPROVED FLEXIBILITY - Utilize any combination of switch, gate or functional modeling levels.
- IMPROVED COST-EFFICIENCY Obtain the lowest available cost per unit of speed.
- IMPROVED PRODUCTIVITY - Streamline the product development cycle while increasing product quality.

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We're tapping the limits of today's technology to meet the design needs of tomorrow.



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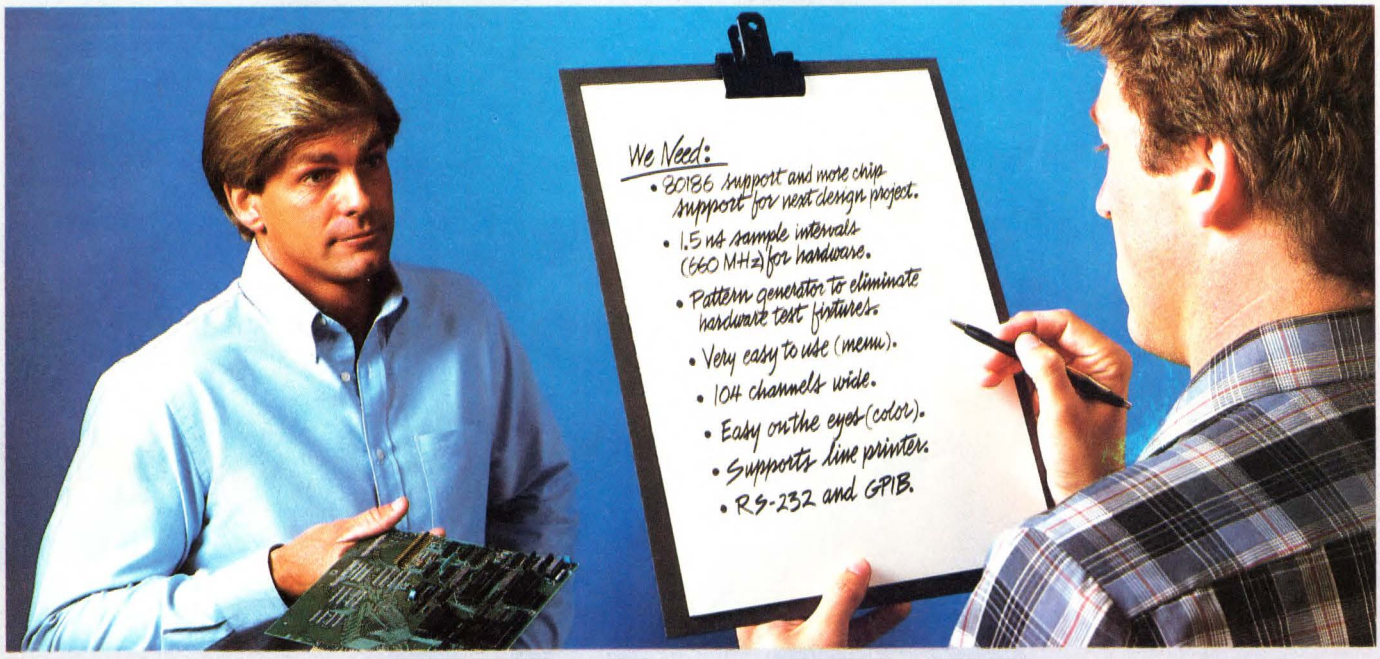
CIRCLE 121

TEK 9100 DIGITAL ANALYSIS SYSTEM

We don't design this.



You do.



The DAS gives you a choice.

Who needs limits — on your capability to solve a problem, or on the value of your investment? That's why we built the DAS. You configure it. You upgrade it. So you fit the solution to the problem. Without the limits imposed by monolithic instruments.



Configure your own.

Choose from six different data acquisition modules and two pattern generator modules. You can combine up to six modules to design your own analysis system.

You decide – 96 channels for software analysis. General purpose 25 MHz software and hardware analysis. 100 MHz hardware analysis. High-speed hardware analysis – 330 MHz or 660 MHz. Pattern generation. And add GPIB, RS-232, tape drive, line printer and hard copy support if you want.

Microprocessor support? None better.

The best in the business. You can design your own custom disassembly, using our Extended Define Mnemonics firmware, or choose from our support packages:

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We've got color.

Nobody else does. Color makes the DAS the easiest design tool on the market to view, to use, to understand. You work faster because you spot hardware and software errors faster.

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Call your Tektronix sales engineer and talk about your applications. We'll help you design your DAS.

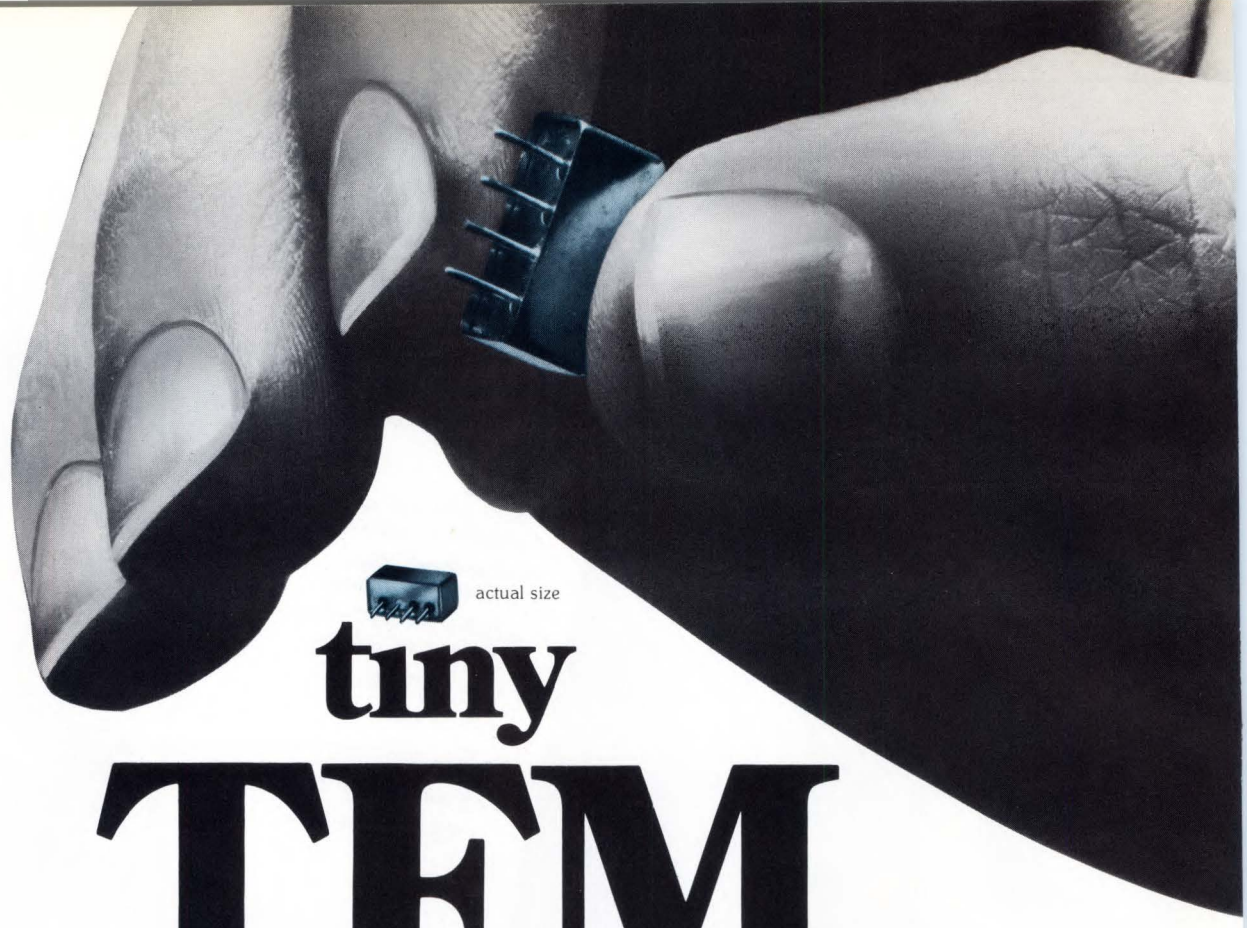
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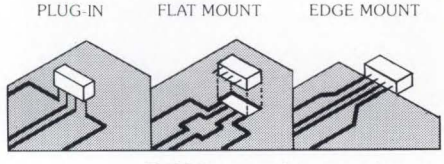
tiny TFM

the world's smallest hermetically-sealed mixers from $11.95
40 KHz to 3 GHz, MIL-M-28837 performance*

Increase your packaging density, and lower your costs... specify Mini-Circuits miniature TFM Series. These tiny units 0.5" x 0.21" x 0.25" are the smallest, off-the-shelf Double Balanced Mixers available today.

Requiring less PC board area than a flat-pack or TO-5 case, the TFM Series offer greater than 45 dB isolation, and only 6 dB conversion loss.

Manufactured to meet the requirements of MIL-M-28837*, the tiny but rugged TFM units have become the preferred unit in new designs for military equipment.



E-Z Mounting for circuit layouts
Use the TFM series to solve your tight space problems. Take advantage of the mounting versatility—plug it upright on a PC board or mount it sideways as a flatpack.

MODEL	FREQUENCY, MHz		CONVERSION LOSS dB, TYPICAL		ISOLATION dB, TYPICAL						PRICE	
					Lower Band Edge		Mid Range		Upper Band Edge			
	LO/RF	IF	1 Octave from Band Edge	Total Range	LO-RF	LO-IF	LO-RF	LO-IF	LO-RF	LO-IF	$ EA.	QTY.
TFM-2	1-1000	DC-1000	6.0	7.0	50	45	40	35	30	25	11.95	(1-49)
TFM-3	.04-400	DC-400	5.3	6.0	60	55	50	45	35	35	19.95	(5-49)
TFM-4	5-1250	DC-1250	6.0	7.5	50	45	40	35	30	25	21.95	(5-49)
•••TFM-11	1-2000	5-600	7.0	7.5	50	45	35	27	25	25	39.95	(1-24)
•••TFM-12	800-1250	50-90	—	6.0	35	30	35	30	35	30	39. 95	(1-24)
▪▪TFM-15	10-3000	10-800	6.3	6.5	35	30	35	30	35	30	49.95	(1-9)
▪▪TFM-150	10-2000	DC-1000	6.0	6.5	32	33	35	30	35	30	39.95	(1-9)

•••If Port is not DC coupled
▪▪+10 dBm LO, +5 dBm RF at 1dB compression
*Units are not QPL listed

For complete specifications and performance curves refer to the Goldbook, EEM, EBG, or Mini-Circuits catalog

CAPO now available! computer-automated performance data

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CIRCLE 145

C68 REV C

COMMUNICATIONS

Multitone ringer is mask-programmable

Replacing the electromechanical bell in telephones, a mask-programmable ringer fulfills almost all of the tone frequency, impedance, and input voltage frequency requirements of the major European postal and telecommunications authorities (PTTs). The ability to produce customized melodies allows the PCD3360 to be used in all countries, irrespective of the melody required by the relevant PTT. Tones include 533, 600, 667, 800, 1000, 1067, and 1333 Hz, with the interval between tones selected at 15, 30, 45, or 60 ms. The ringer offers three selectable impedances of approximately 7, 10.5, and 17.5 kΩ and is equipped with a frequency descriminator circuit, which permits the incoming enable signal to be anything between 16 and 50 Hz.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.

Signetics Corp., 811 E. Arques Ave., Sunnyvale, Calif. 94086; (408) 739-7700.

CIRCLE 328

Ethernet controllers ride popular buses

Intelligent Ethernet controllers for Unibus-, Q-bus-, and Multibus-based systems—the NP100, NP200, and NP300, respectively—offload the host from protocol processing to provide higher throughput and greater CPU availability. Each board has a dedicated 80186 processor. For high-performance Ethernet applications, an on-board Xerox Network Systems Internet Transport Protocol (XNS/ITP) package is available, as well as a DOD-compatible Transmission Control Protocol/Internet Protocol (TCP/IP) package.

Interlan Inc., 3 Lyberty Way, Westford, Mass. 01886; (617) 692-3900. **CIRCLE 329**

The STD Bus Language: ROBASIC™

FAST - ROBASIC is a ROM-based language that runs up to 50 times faster than Basic, without compiling. **With ROBASIC, you may never need Assembly Code again!**

EASY - ROBASIC is easy like Basic. But with multi-tasking plus special measurement and control commands. Because ROBASIC is part of an integrated hardware/software system, it replaces expensive development systems. ROBASIC makes everyone a programmer.

ROBASIC - now on the Octagon 880 Multifunction CPU card.



- 2 RS-232C serial ports
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- Real time clock
- 16 parallel I/O channels
- 9 prioritized interrupts
- 8088 processor - IBM-PC compatible
- ROBASIC on board in 16K ROM

ROBASIC and the 880 give you a powerful tool for real time control. Connect a 5V supply and a CRT or personal computer and write ROBASIC programs the same day - guaranteed.

Hardware and software products and support are available.

CALL Robert Schlesinger for details: (303) 426-9780

OCTAGON SYSTEMS CORPORATION
6501 W 91st Ave., Westminster, Co. 80030 (303) 426-8540

CIRCLE 124

Celesco means: position measurement

From two to 500 inches and beyond, Celesco transducers measure the position or displacement of anything that moves. Whether it be the position of a gate or damper door, feedback for servo systems or programmable controllers, hydraulic or pneumatic ram displacement, Celesco provides critical data, increases productivity and gives you control.

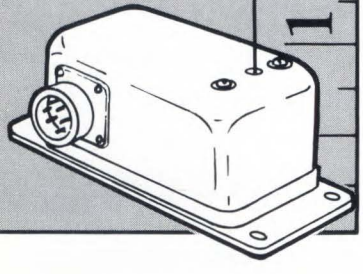
A stainless steel cable is attached to the moving object and the transducer to a fixed surface. An electrical signal proportional to the extension of the cable is provided for display, recording, feedback or input to a controller.

The transducer is available in a sealed version for use underwater or in other hostile environments. Celesco also provides velocity and combined position/velocity transducers.

So if your problem is position measurement, consider the simplicity and accuracy of a Celesco transducer. For more information, call: 800-423-5483 (213-884-6860 in Calif.); or write: Celesco Transducer Products, Inc., 7800 Deering Ave., P.O. Box 1457, Canoga Park, CA 91304.

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Means Measurement

Subsidiary of HCC Industries



CIRCLE 126

NEW PRODUCTS

COMMUNICATIONS

Fiber-optic modem works with PDP-11, VAX

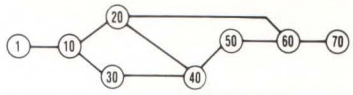


Compatible with VAX and PDP-11 minicomputers, as well as DEC-compatible peripheral devices, the DC100 fiber-optic modem permits interconnections (up to 3300 ft) of DR11-W and DR11-B communications interfaces using a small duplex fiber-optic cable. Using the DC100 to link DEC and DEC-compatible devices eliminates many of the communications problems associated with large, multiconductor coaxial cables, including distance limitations, electromagnetic interference, grounding problems, and signal radiation. The DC100 is also transparent to software, converting the parallel DEC DR11-W or DR11-B interface into a 60-Mbit/s serial optical bit stream—which is reconverted into parallel electrical signals at the far modem end.

The DC100 system consists of two small modems: the DC100/C at the central processor and the DC100/U at the user's location. Each modem is equipped with remote loop-back diagnostics.

Artel Communications Corp., PO Box 100, West Side Station, Worcester, Mass. 01602; (617) 752-5690.

CIRCLE 330



WE DARE YOU TO COMPARE *ANY* PROJECT MANAGEMENT SYSTEM TO PMS-II

FEATURES:
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- Super- and Sub-Networking
- Budget and Actual Cost Control
- True and Free Float
- Runs on Most Microcomputers
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REPORTS:
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- Complete Bar Charting
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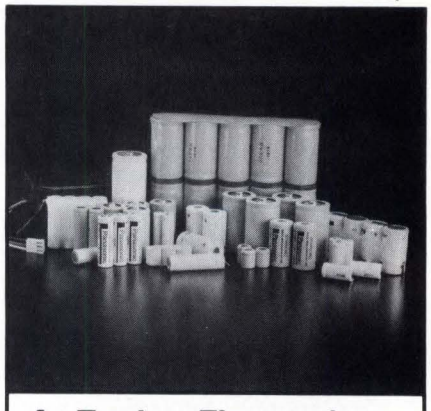
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CIRCLE 127



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CIRCLE 128

PRODUCT NEWS

PROM programmer gets universal adapter

The 256DI UPM adapter enables the Model 256DI PROM programmer, from **Dynatec International Inc. (Salt Lake City, Utah),** to program virtually any programmable device, including EPROMs, PALs, PROMs, IFLs, FPLAs, EEPROMs, and microprocessors. The adapter, which costs $485, is compatible with most industry-standard protocols, such as Intel Hex, Motorola S-code, Tektronix Hex, and the JEDEC Standard 3. Each pin of the adapter's two sockets (a standard 40-pin and a 28-pin with 0.03-in. spacing) is programmable by selecting a two-number code, which is contained in the programmer's EPROM, for the device that is to be programmed.

CIRCLE 331

Diagnostic card tests mass-memory system

Designed specifically for the MK8200 family of general-purpose mass-memory systems, **Mostek Corp. (Carrollton, Texas)** is offering a diagnostic card, which verifies that the system is fully functional before it is placed on-line. In the event of a subsystem failure, the MK8151 card also assists the operator in identifying and isolating the system problems to the RAM and card levels. The MK8151 features a test processor capable of executing up to 12 different diagnostic algorithms and reporting any failures to its built-in log. In addition, user-selectable scope loop tests are available to further assist in isolating system problems. The single-unit price of the card is $6500.

CIRCLE 332

Logic analyzers meet diverse needs

By reconstructing its previous line of logic analyzers, **Nicolet Paratronics Corp. (Fremont, Calif.)** has introduced five new machines that can be configured for almost every application and budget. The five models that comprise the 800 series include the NPC-800A, a complete logic analysis system that offers 32 channels of state analysis and 16 channels of timing analysis. The NPC-800B, which has a 48-channel state analyzer and a 16-channel timing analyzer, features 8- and 16-bit microprocessor analysis capability, while the NPC-800C offers 200-MHz timing. The top-of-the-line NPC-800D also features 200-MHz timing, along with sophisticated 48-channel state analysis. Finally, the NPC-800E is for users who require 200-MHz timing analysis but do not need a state analyzer.

CIRCLE 333

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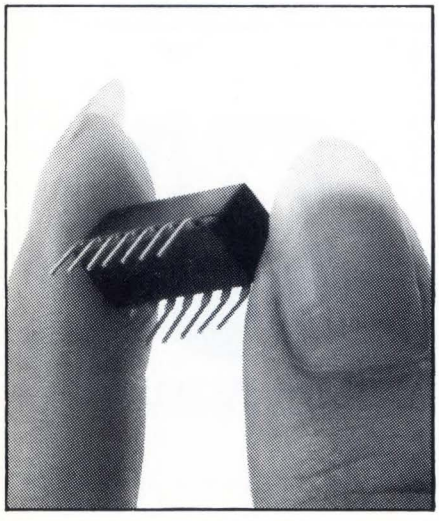
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CIRCLE 130

PRODUCT NEWS

HP 9000 family welcomes two additions

Hewlett-Packard Co. (Palo Alto, Calif.) has added two new models to its HP 9000 Series 200 line of desktop engineering workstations. Users now have 14 models from which to choose, ranging in price from approximately $5000 to $100,000. The Model 217 engineering workstation uses an 8-MHz 68010 processor and features a 14-in. monitor and 512 kbytes of RAM (expandable to 4 Mbytes). Based on a 68000 processor running at 12.5 MHz, the Model 237 graphics workstation includes a high-resolution 17-in. monitor, a mouse, and 512 kbytes of RAM (expandable to 7 Mbytes). Basic and Pascal operating systems, as well as the Unix-derived HP-UX operating system, permit a growth path across the entire line.

CIRCLE 334

VLSI test system is more flexible

A software upgrade for the J941 VLSI test system has released by **Teradyne Inc. (Woodland Hills, Calif.)** to speed load time and expand the system's flexibility. The improved software, Version 5.0, also makes program generation, calibration, and operation easier and faster. One enhancement to the system's Master Operating Program (MOP) and Pascal-T compiler enables vector compression. File size is automatically reduced by up to 30% and without having to redesign existing programs. Other features automatically calibrate the system or halt testing if calibration cannot be performed. To simplify the testing of two different devices in the same system, the job relocation function automatically manages memory resources used by the two concurrently loaded device test programs.

CIRCLE 335

Euroboard manufacturer comes to U.S.

Encouraged by the growing acceptance of the Euroboard form factor by American manufacturers of board-level microcomputer products, the Switzerland-based Gespac S.A. has opened a subsidiary in the U.S. known as **Gespac Inc. (Mesa, Ariz.).** The company manufactures microcomputer boards in the single-height Euroboard format (100 by 160 mm) and supports all of the popular microprocessors, such as the 6809, Z80, 8085, 68000, 8088, 16032, and J11. It also carries an extensive range of compatible memories, interfaces, controllers, converters, transducer boards, and accessories. All of the boards are compatible with the G-64 bus, the de facto standard in most European countries. In order to support G-64 users in their design efforts, the company also offers a variety of development systems and software packages.

CIRCLE 336

PRODUCT NEWS

Schottky rectifier line gains 3-A devices

Unitrode Corp. (Lexington, Mass.) is expanding its Schottky rectifier line with the addition of the 1N5820 through 1N5822 series of 3-A axial devices. These Schottky barrier rectifiers are suitable for use as free-wheeling diodes, as polarity-protection diodes, and as rectifiers in low-voltage, high-frequency inverters. The series offers reverse voltages of 20, 30, and 40 V. Maximum forward-voltage drops at 3 A are 0.475, 0.500, and 0.525 V. In quantities of 1–99, the 1N5820, 1N5821, and 1N5822 are priced at $1.04, $1.22, and $1.60, respectively. **CIRCLE 337**

Digital filter program supports TI's DSP

Signix Corp. (Wayland, Mass.) has announced that its Dispro v1.0 software system now supports digital filtering applications on Texas Instrument Corp.'s TMS32010 digital signal processor. The software, which runs on the IBM PC, provides a total environment for the design and performance evaluation of digital filters. Features include functional testing of filter operation through simulated fixed-point arithmetic and generation of assembly language instructions to implement digital filters on the TMS32010. **CIRCLE 338**

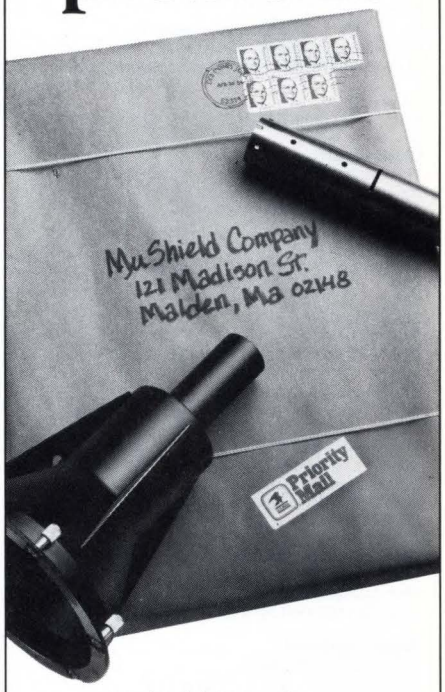
PDP-11 talks to 70 dissimilar computers

Enabling PDP-11 series computers running under the RSX operating system to communicate with 70 different vendor's computers (including minis, micros, and mainframes) is a version of BLAST communications software. The product of **Communications Research Group Inc. (Baton Rouge, La.)**, BLAST—for Blocked Asynchronous Transmission—allows the error-free transfer of any binary data files, text files, or commands between RSX-based systems and any other computer running the BLAST software, regardless of differences in the operating systems. **CIRCLE 339**

D flip-flops are fabricated in QMOS

RCA Corp.'s Solid State Division (Somerville, N.J.) has added two versions of the popular quad D-type flip flop with complementary outputs to its QMOS family of high-speed CMOS logic devices. The CD54/74HC175 flip-flops are intended for new high-speed CMOS designs, while the CD54/74HCT175 flip-flops can directly replace low-power Schottky TTL logic devices in existing systems. The latter flip-flops are speed-, function-, and pin-compatible with the LSTTL devices. **CIRCLE 340**

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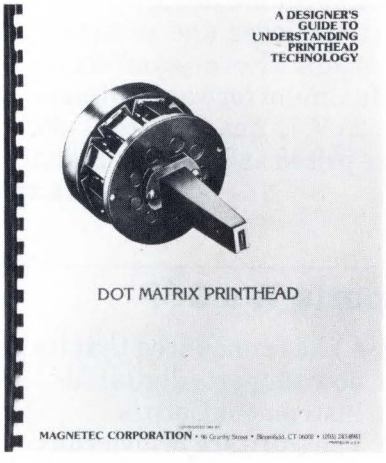
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APPLICATION NOTES

Evaluating, applying dot-matrix printheads



A designer's guide to understanding dot-matrix printhead technology provides a general introduction to the design, application, and use of dot-matrix impact printheads. The information contained is applicable to most rotating armature- or clapper-type printheads, in particular those of the ballistic type. Some of the topics discussed include basic operating principles, electronic drivers, print quality, and printhead evaluation.

Magnetec Corp., 96 Granby St., Bloomfield, Conn. 06002.

CIRCLE 341

Applying CMOS d-a converters

The use of CMOS d-a converters in microprocessor-based systems is the subject of a note that details the circuit techniques available to designers when only a single +5-V supply is available. Specific topics of discussion include single-supply operation in the voltage-switching or current-switching mode, the selection of amplifiers, and interfacing the converter to the microprocessor. A useful chart of popular op amps details their expected performance when used with CMOS d-a converters in single +5-V applications.

Analog Devices Inc., Route 1 Industrial Park, PO Box 280, Norwood, Mass. 02062.

CIRCLE 34

Proximity switches in process control

A booklet serves as a guide to the use of electronic proximity switches in machine- and process-control applications. The guide concentrates on units that operate a load directly through a solid-state output circuit and points out their advantages over mechanical limit switches. It also explains the difference between inductive and capacitive sensors and discusses the application considerations of two- and three-wire configurations. In addition, the literature covers mounting arrangements and such parameters as detection range, hysteresis, attenuation range, and speed.

Automatic Timing & Controls Co., 201 S. Gulph Road, King of Prussia, Pa. 19406.

CIRCLE 343

NEW LITERATURE

Metallized film capacitors

Electrical, mechanical, and environmental characteristics are provided in a 33-page catalog for metallized film capacitors of molded-box construction. Capacitor selection criteria, typical properties of dielectric materials, and a metric conversion table are also included, along with numerous performance curves and outline drawings.

Evox Inc., 2345 Waukegan Road, Suite S-150, Bannockburn, Ill. 60015.

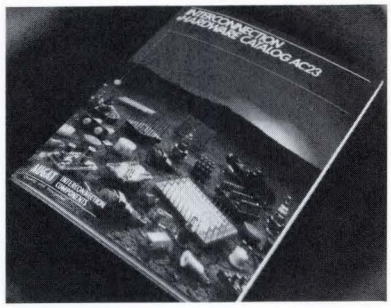
CIRCLE 344

Electronic test accessories

Hundreds of time-saving solutions to common testing, hook-up, and assembly applications are offered in a 114-page catalog of electronic test accessories. Specifications, configuration diagrams, and application examples are given on such products as DIP testing accessories, continuity and voltage testers, multilead assemblies, jumpers, probes and patch cords, components and adapters, coaxial test accessories, cables, and connectors. Over 12,000 styles, sizes, and color-coded variations are available to suit virtually any use or special design requirements.

Tektest Inc., E-Z Hook Division, PO Box 450, Arcadia, Calif. 91006. **CIRCLE 345**

Interconnection hardware



Featured in this 96-page catalog (AC23) are adapters, programming devices, test jacks, transistor sockets, crystal relay sockets, Holtite products, tools, and socket and pin terminals. Each product is described and identified by part number listings, photographs, specifications, and engineering drawings.

Augat Inc., Interconnection Components Division, 33 Perry Ave., PO Box 1037, Attleboro, Mass. 02703.

CIRCLE 346

Controllers, timers, and solid-state relays

Physical and operational specifications are presented in a 25-page booklet for process control instrumentation and components. Offerings include programmable logic controllers, electronic timing modules, solid-state relays, monitoring relays, proximity switches, and sensors.

Automated Controls and Systems, Station Road, Whittlesford, Cambridge CB2 4NL, England. **CIRCLE 347**

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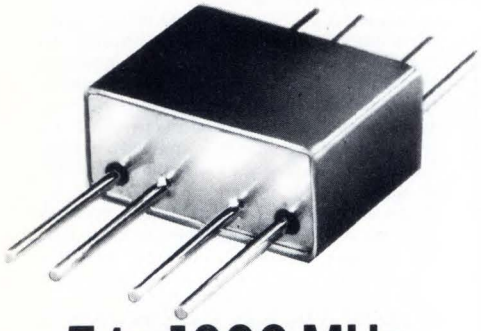
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one octave from band edge			6.2	7.0
total range			7.0	8.0
ISOLATION, dB			TYP.	MIN.
5-50	MHz	LO-RF	50	45
		LO-IF	45	40
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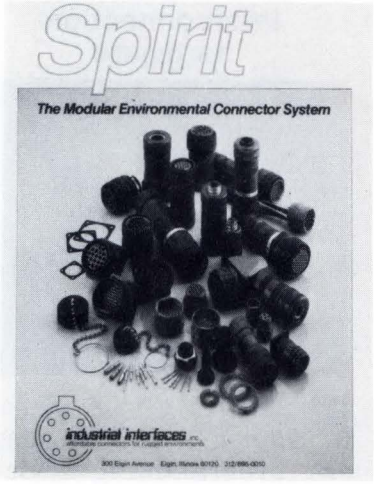
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CIRCLE 132

NEW LITERATURE

Heavy-duty industrial connectors



The Spirit series of connectors, for use in harsh industrial environments, is the subject of a 16-page brochure. The literature presents device features, photos, line drawings, specifications, performance data, cable diameters, and ordering information. The Spirit series consists of a few standard modular components that allow for 18,000 unique connector variations.

Industrial Interfaces Inc., 300 Elgin Ave., Elgin, Ill. 60120. **CIRCLE 348**

Rf and microwave components

A 440-page catalog provides detailed definitions and illustrations of an updated product line for next-generation rf and microwave systems. With more than 34 new products, the line includes rf switches (single and multithrow); biphase, quadraphase, and vector modulators; digital attenuators; rf logarithmic and thin-film amplifiers; microwave and termination-insensitive mixers; doublers that operate up to 6 GHz; and 90° flat-pack hybrids. Also featured are GaAs FET amplifiers, which cover the range of 150 MHz to 5.2 GHz in a single drop-in unit.

Adams-Russell Co., Anzac Division, 80 Cambridge St., Burlington, Mass. 01803. **CIRCLE 349**

Switch-mode, linear, hybrid power supplies

Fifteen power supply families are described and specified in a 20-page publication. Supply types include switch-mode, linear, and hybrid. Also included are dc-input power supplies, switching regulators, and converters.

Coutant Electronics Ltd., Kingsley Ave., Ilfracombe, Devon EX34 8ES, England. **CIRCLE 350**

Monochrome video monitors

A bulletin presents 9-, 12-, 15-, 17-, and 23-in. video monitors with standard P4 white phosphor screens. Specifications are given for each type, along with photographs, outline drawings, options, and customized specials.

Electrohome Ltd., 250 Wales Ave., Tonawanda, N.Y. 14150.

Electrohome Ltd., 7 Civic Way, South Wirral, Cheshire L65 0AX, England. **CIRCLE 351**

NEW LITERATURE

Semiconductor development equipment

Scanning electron microscopes and equipment specifically designed to meet the requirements of semiconductor development and production provide the major focus of this 14-page brochure. Examples of the equipment described are depicted with color photographs and brief explanations of the applications and the more significant capabilities of each.

Cambridge Instruments Inc., 40 Robert Pitt Drive, Monsey, N.Y. 10952. **CIRCLE 352**

Dc servomotors, tachometer generators

Rotating components are the subject of a colorful 32-page booklet, which includes dc tachometer generators, dc servomotors, motor generators, custom products, options, accessories, speed-indicating systems, and dc servo control systems. The fully illustrated literature discusses features and advantages and lists specifications and dimensions for each of the product lines.

Servo-Tek Co. Inc., 1086 Goffle Road, Hawthorne, N.J. 07506. **CIRCLE 353**

Infrared-filter wall chart

An 18-by-24-in. wall chart presents the design parameters and environmental conditions affecting infrared filters. The four-color chart includes atmospheric absorption spectra, substrate transmission for ten frequently used substrate materials in the infrared region (out to 24 μm), specification criteria including angle and temperature effects, standard equations, and a glossary of commonly used terms.

Optical Coating Laboratory Inc., 2789 Northpoint Pkwy., Santa Rosa, Calif. 95401. **CIRCLE 354**

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CIRCLE 134

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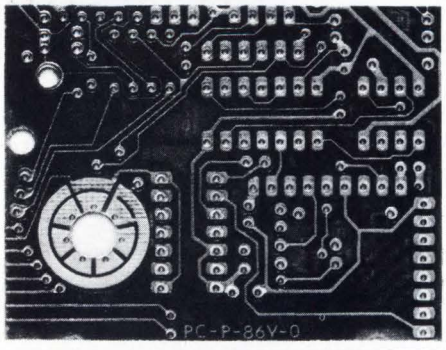
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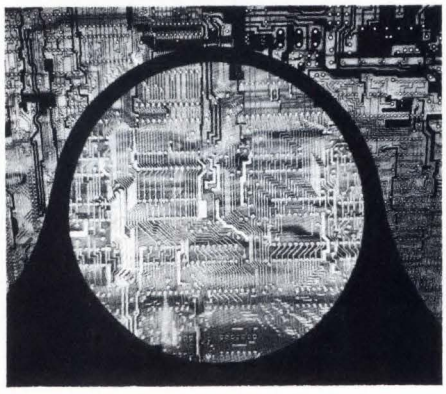
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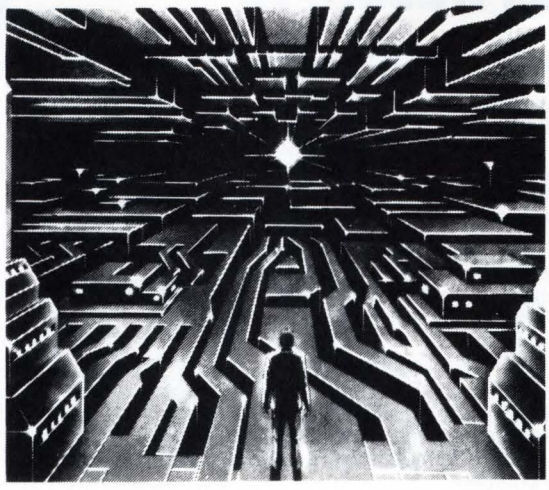
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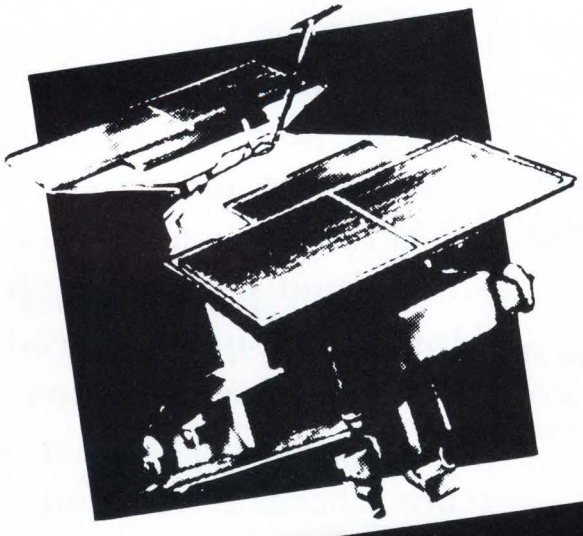
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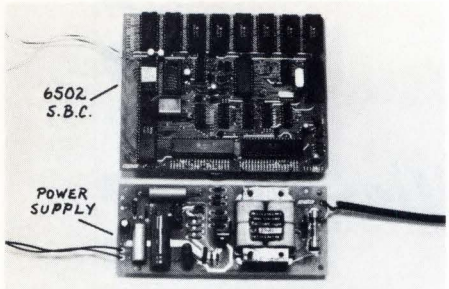
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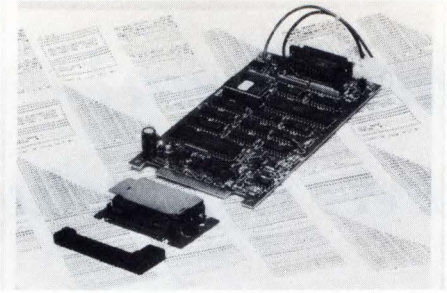
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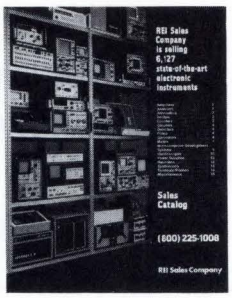
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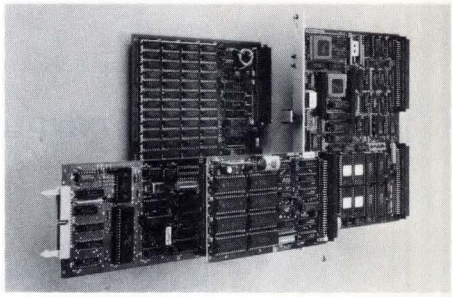
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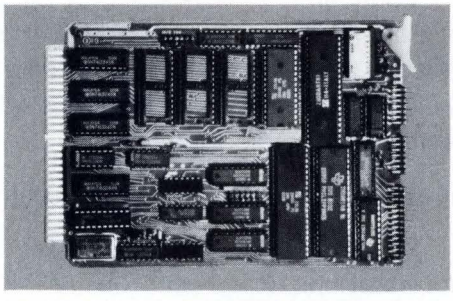
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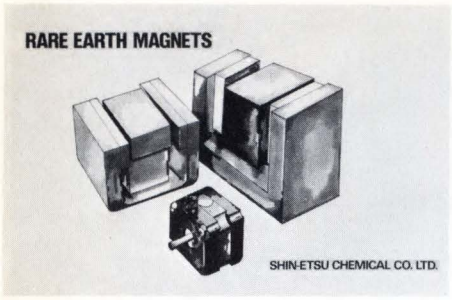
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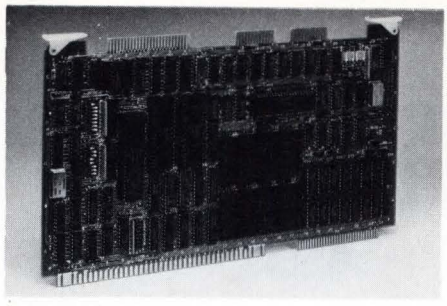
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RARE EARTH MAGNETS **259**



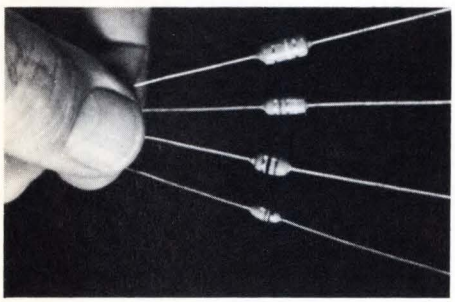
Z8000™ MULTIBUS™ SBC. Z8001 or Z8002 16-bit CPU (6 MHz); 32K or 128K DRAM (upgradable to 512K); up to 48K static RAM or EEPROM; up to 128K EPROM; 2 RS-232 ports (Z8030 SCC); 40 parallel I/O lines, six 16-bit counter-timers (Z8036 CIOs); vectored interrupts. EPROM Debug Monitor, MICRO CONCURRENT PASCAL, C, FORTH, VRTX. Dev. Z8000 software on IBM PC, PDP-11, Intel MDS, Olivetti M20 or 8080/Z80 CP/M system. Z8000™ Zilog, Multibus™ Intel Corp. SINGLE BOARD SOLUTIONS, 7669 Rainbow Dr., Cupertino, CA 95014. 408-253-0181.

SINGLE BOARD SOLUTIONS **260**



The NEW OMEGA SLC-II is a "stand-alone" computer voice simulator. The SLC-II will monitor any RS232C data stream, analyze the information and route it through any of 16 possible outputs to a data bank, computer terminal, or even call & brief you directly via the phone. Eighty-five actions can be stimulated over the phone. Programming is done in BASIC. For information in a RUSH, call (203) 359-7874. OMEGA ENGINEERING, INC., P.O. Box 4047, Stamford, CT. 06907.

SLC-II TALKING MONITOR **261**



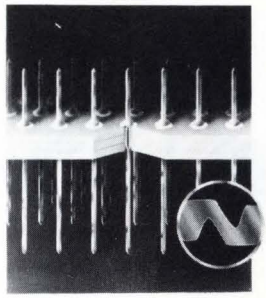
CONFORMAL COATED INDUCTORS ... Manufactured to the same high quality standards as MIL-SPEC molded chokes ... **at considerable savings** ... epoxy resin coated inductors withstand severe environmental conditions ... standard values from .1 uH to 1,000 uH ... custom winding on special order ... 40-page industrial inductors catalog on request. J. W. MILLER DIVISION of Bell Industries, 19070 Reyes Ave., P.O. Box 5825, Rancho Dominguez, CA 90224. (213) 537-5200.

INDUCTORS **262**

Logic Simulation System

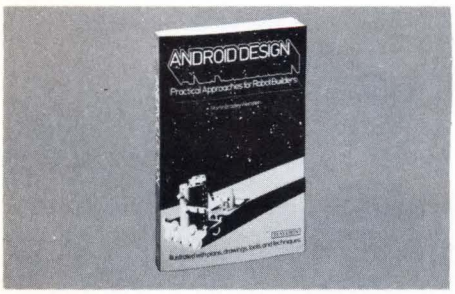
Interactive Logic Simulation System. A four state unit delay simulator. (1, 0, unknown, hi-z.) Standard ASCII files or keyboard entry. User defined macros, signal sources, patterns. Output is timing diagram (screen or printer) loading report (fanout). Circuit, macros and externals. Signal sources are periodic and aperiodic, user defined. It is easy to use and handles errors gracefully. Full documentation is provided. For microcomputers running CP/M or MS-DOS. Price: $175.00. Tatum Labs, P.O. Box 698, Sandy Hook CT 06482, 203-426-2184.

SIMULATION SYSTEM **263**



FEED-THROUGH COMPLIANT PIN Eliminates damage to plated-through holes in printed circuit backplanes. The compliant section has an elastically deformable "Z" cross-section which is designed to provide a high-retention-force, gas-tight joint with no hole damage even after multiple insertions. Mil-C-28859 QPL listed, the pin is available in .025" feed-through wrap-post or DIN configurations. Custom tooled pins also available. INTERCONICS, P.O. Box 64223, St. Paul, MN 55164.

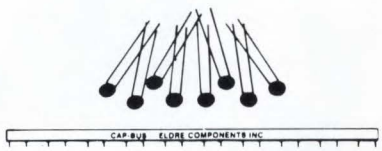
COMPLIANT PIN **264**



ANDROID DESIGN: Martin Bradley Weinstein, Build your own android with the tools and techniques presented in this easy-reference instruction manual. **Fully illustrated.** Send $15.95 plus $2.00 to cover postage & handling to Hayden Book Company, 10 Mulholland Dr., Hasbrouck Hts., NJ 07604. Reference number 5192 must be included on your check or money order. If not satisfied, return the book undamaged, within 10 days for refund.

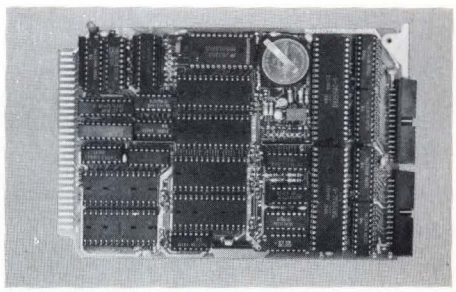
ANDROID DESIGN **265**

ELIMINATE DECOUPLING CAPACITORS



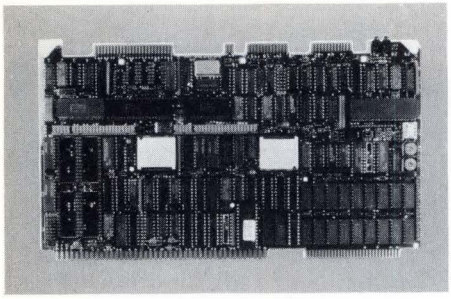
CAP-BUS® CAPACITOR/BUS BAR Eliminate the decoupling capacitors and the power and ground traces from your PCB for more reliability. CAP-BUS® has distributed capacitance of .05 micro-farads per lin. in., at 50 VDC with low inductance and low impedance. The capacitor and the bus bar have been joined together for CAP-BUS®; a more efficient capacitive decoupled power distribution system, increasing IC density on a two sided board. **ELDRE COMPONENTS, INC.,** 1500 Jefferson Rd., Rochester, NY 14623 (716) 244-2570

BUS BAR CAPACITOR **266**



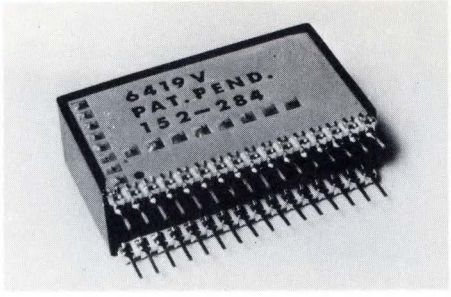
STD CLOCK, MEMORY, I/O BOARD, The RSD-7758 features a battery backed, 14 digit real time clock w/prog. interrupt, six 28 pin bytewide memory sockets, 48 buffered parallel I/O lines. Available options: up to 48K bytes battery backed RAM and 32 high current open collector drivers for parallel I/O. Board is memory mapped and decodes either 16,17 or 20 address lines. Consult factory for other available configurations. ROBOTROL CORP., 16100 B Caputo Drive, Morgan Hill, CA 95037, (408) 778-0400.

STD CLOCK, MEMORY, I/O **267**



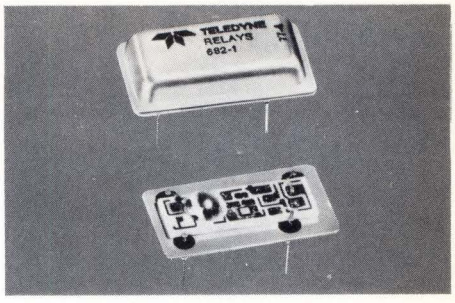
ZX-186/30 80186 SINGLE BOARD COMPUTER On IEEE-796 BUS ... 8 MHz 80186 ... 128K/256K/512K/1MB on-board, dual-ported zero-wait-state RAM w/ parity. Up to 128KB EPROM. (1) RS-232C serial port/(1) RS-232C or RS-422 serial port. Bit Sync capability. (2) DMA channels. 24 parallel I/O lines. (2) iSBX connectors. (6) 16-bit timers. (10) vectored interrupt levels. iSBC-86/30 compatibility. Vol. Discounts. **ZENDEX CORP.** 6700 Sierra Ln., Dublin, CA 94568 (415) 828-3000. TWX 910 389 4009. iSBC, iSBX TM of Intel Corp.

SINGLE BOARD COMPUTER **268**



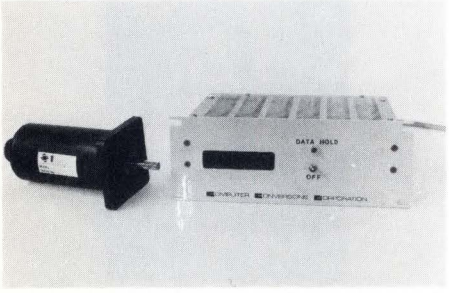
HPI-6418V/25618V 64kb/256 kilobyte dynamic RAM module reduces required PC board space by 70% compared to conventional memory modules. This memory module offers lower distributed capacitance, higher speeds & fewer support components. The module operates at a lower temp. & has higher speeds & reliability factor. The HPI-6418V operates on +5 volts & is ideal for computer/telecommunication applications. Units 100% tested. Pricing starts at $125.00 in 100 piece lots. Hy-Pac Inc., 760 San Aleso, Sunnyvale, CA 94086. (408) 745-0950.

DYNAMIC RAM MODULE **269**



MIL SOLID STATE RELAYS Teledyne 682 AC relay features load rating of 1 amp at 250VRMS, over a frequency of 45 to 440Hz. Zero voltage turn-on assures low EMI. Optical isolation is 1500VRMS. Control range is 3.8 to 32VDC @13mA. Operating temp is −55°C to 100°C. Qualified to MIL-R-28750. $36 ea for 500 pcs. Assembly to MIL-883B & 38510A available at additional cost. Model 683 is the DC version. Teledyne Solid State Products, 12525 Daphne Ave., Hawthorne, Ca. 90250. (213) 777-0077.

RELAYS **270**



SWITCH SCALEABLE ABSOLUTE ENCODER ±1 part in 3600 system accuracy, electromagnetic transducer & L.E.D. display, BCD output for P.C., micro-interface, field programmable scale factor (0-9999) & preset (range adjust). Hi-noise immunity, zero offset, Nema 12 Explosion proof transducer avail., rack, panel or PC card electronics. Price less than $995/axis. Other products: Multiturn Encoders, S/D & D/S Converters & Limit Switches. Send for free catalog/application notes. Computer Conversions Corp., 6 Dunton Ct., East Northport, N.Y. 11731 516/261-3300.

ABSOLUTE ENCODER **271**

INTRODUCING TELTONE'S NEW MULTIFREQUENCY TONE RECEIVER

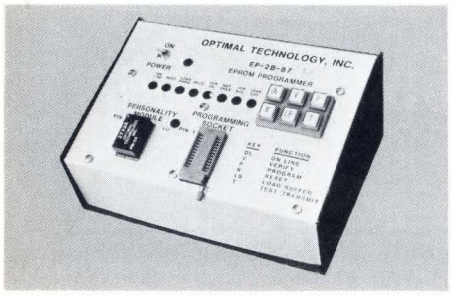
Teltone's high performance M-985 Multifrequency Receiver detects multitone trunk address signals. Compatible with North American standards and international CCITT recommendations, it detects tones at 700, 900, 1100, 1300, 1500 and 1700 Hz, using a single 12V supply. It joins Teltone's complete telecommunications family of generators, detectors, receivers and relays. **1-800-227-3800, ext. 1130. Teltone Corporation, P.O. Box 657, Kirkland, WA 98033.**

TELTONE **272**



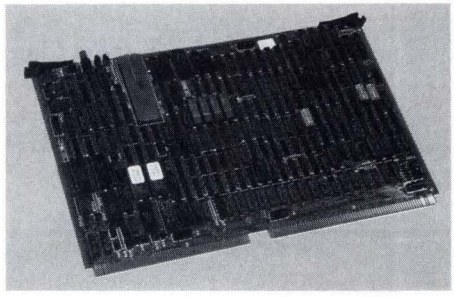
8048 IN-CIRCUIT EMULATOR E232-48 emulates Intel compatible 8048, 8049, 8050 microcomputers and their ROMless, EPROM and CMOS versions in real time at their maximum rated speeds. It offers complete debugging facilities including inline assembly, disassembly, hardware breakpoints and single stepping. E232-48 connects to any host computer via RS-232 serial port. Price: $1795. IBM-PC, CP/M cross assemblers $99.50. SIGNUM SYSTEMS, 726 Santa Monica Blvd., Santa Monica, CA. 90401, 213/451-5382.

EMULATOR **273**



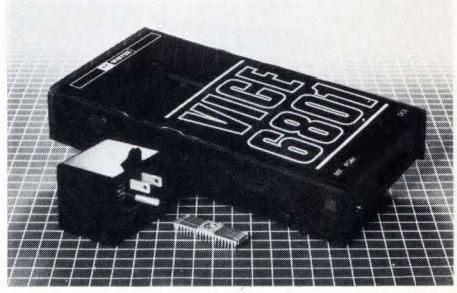
EPROM PROGRAMMER. Model EP-2B-87 comes with RS-232 and 20 Ma. current loop. Programs 2708, 2716, 27C16, TMS2716, 2732, 27C32, 2732A, 2532, 2764, 2764A, 27C64, 27128, 27128A, 27256, 2564, MCM68764 EPROMS; 2816A 2864 EEPROM; 8751, 38E70 MPU. Intel, Motorola, and Tektronix formats. Stand alone copy, edit, 17 RS-232 commands. Price, $575 for 8K buffer. Personality modules $18 to $36. Optimal Technology, Earlysville, Va. 22936. 804-973-5482.

EPROM PROGRAMMER **274**



PT-VBS100. MAIN FRAME PERFORMANCE NOW AVAILABLE ON VERSABUS A general purpose VERSAbus processing element yeilding high-end minicomputer processing power in compact, cost effective package. Combines high performance 12.5 Mhz 68000 16-bit microprocessor, high speed memory management facility & very fast 2K byte cache memory. Executes memory resident programs w/ an 80% one-half wait state hit rate. Performance Technologies, Inc., 300 Main St., E. Rochester, New York 14445 (716) 586-6727.

VERSABUS BOARD **275**



6801 Test Bed and Programmer. Virtual In-Circuit Emulator (VICE) develops single-chip microcomputer programs for the 6801/68701 and programs on-board EPROM. A cost and time effective way to progam the 6801/68701 for $695. Wintek Corporation, 1801 South Street, Lafayette, IN 47904-2993. (317) 742-8428.

V.I.C.E. **276**

INDEX OF ADVERTISERS

AMP 64-65
AT&T Information Systems ... 270-271
Abbott Transistor Laboratories 22
Advanced Micro Devices ..... Cover II Gatefold
Aleph International 14
Ampere Inc. 342
Apex Microtechnology 15, 292

Brown Boveri & Cie ..... 100L†
Bussman 49

Calay Systems 286, 287
California Devices, Inc. 295
Carborundum 299
Career Extra 290
Celesco 326
Celm ..... 92E†
Comdial 161, 283
Comlinear Corp. 57
Computer Conversions, Inc. 344
Control Data Corp. 235
Custom Programming Group Inc. .. 342
Cybernetic Micro Systems 25
Cypress Semiconductor 184

Dale Electronics 2
Darnell Corp Ltd. 70
Data Translation 74
Dexpo 192, 193-194
Digelec (Wavetek-Digelec) 115
Digitec 84

ENI 327
ERSO 342
ESAN USA 328
Elantec 133
Eldre Components 343
Electrochem Industries 60, 315
Electronic Concepts 84
Electronic Conventions 319
Enertec Schlumberger 1000*
Exar 288-289

Fag SA Lausanne 100I*
Ferranti Electronics 100H*
Filter Concepts 70
Fujitsu Microelectronics 93*
FutureNet 40

GE Intersil 266-267
GTE Microcircuits 34-35
General Instrument, Discrete Semiconductor 313*
General Instrument, Microelectronics Div. ..... Cover IV
Genstar Rental Electronics 342
Gigabit Logic 54
Gold Book 272-273
Gould AMI 12-13
Gould Ltd. ..... 100E†
Grayhill 201

Harris Microwave 303
Harris Semiconductor, A Div. of Harris Corp. 33, 199, 204-205
Hayden Book Co. 343
Hitachi America Ltd. 90-91*
Holt Integrated Circuits 312*
Hughes Connecting Devices 89*
Hybrid Systems 228
Hy-Pac, Inc. 344
ILC Data Device Corp. 69

Information Handling Services 256-257
Inmos 206-207
Integrated Device Technology 297
Intel Corp. 134, 237-344
Interconics, Inc. 343

James Electronics 21
Janco Corp. 23

Keltron Corp. 342
Koh-I-Noor Rapidograph, Inc. 304*, 305*

Language Resources 127
Linear Technology 254-255
LXD, Inc. 16

Marconi Instruments 333
Mentor Graphics 78-79
Micrografx 101
Micro Power Systems 273
Microswitch, a Div. of Honeywell 98-99*, 314*
Mietec ..... 96E-97E†
J.W. Miller Div./Bell Industries ... 343
Mini-Circuits Laboratory, a Div. of Scientific Components Corp. 6, 7, 10, 17-20, 26, 48, 95, 272, 284-285, 316, 324, 332
Mitchell Electronics 342
Mitel 281
Molex ..... Cover III
Monolithic Memories, Inc. 61-63
Mostek Corp. 43, 182-183
Motorola Semiconductor Products, Inc. ..... 50-51, 83, 96-97*, 100J-100K†
MuShield Corp./Div. Bomco 329
3M Corporate 223
3M Electronic Products, Textool ... 119

NCR Board Level Products 251
NCR Power Supply 300
NCR Printer 166
NEC Electronics ..... 100R†
National Semiconductor Corp 8-9
North America Mica 326

Octagon Systems 325
Omega Engineering 343
Optical Electronics 16
Optimal Technology 344

Pace Electronic Products 252
Pacific Microcircuits 160
Performance Technologies, Inc. 344
Plessey Microsystems 100*
Plessey Semiconductor ..... 98E-99E†
Powertec, Inc. 85-88*
Precision Monolithics 46, 47
Princess Cruises 308
Proteon 258

RCA Solid State Division 71-73
Radiometrics Midwest Corp. 342
Raytheon Co. 30
Robotrol 343
Rockwell International 1
Rogers Corp 208, 342
Rohde & Schwarz ..... 100S†

SGS 203*
SGS-ATES ..... 100M-100N†
S-MOS 225
SAFT America, Inc. Advanced Battery Div. 253
Shin-etsu Chemical Co. 343
Siemens 307*
Signetics 164-165
Signum Systems 344
Silicon General 28-29
Single Board Solutions 343
Solarex 301
Solid State Scientific 24
Solutionware Corporation 342
Sprague Electric Co. 80, 293
Stag Microsystems 346
Standard Power 94*
Stantel Components 117

TRW/LSI Products Div. 77
TRW Microwaves 319
TRW Resistive Products Div. 131
Tadiran 227
Tatum Labs 343
Tauber Electronics 326
Tektronix 38-39, 59, 322-323
Teledyne Semiconductor 45
Teledyne Solid State Products 344
Teltone 317, 344
Texas Instruments 52-53
Theta-J 268-269
Thomson CSF ..... 90E-91E†
Triplett Corp. 274

Unitrode 309*

VIA Systems 277, 279

Wavetek San Diego 129
Western Graphtec 311*
Wintek Corp. 216, 344

Zax 66
Zendex 344
Zilog 36-37
Zycad 320-321
Zytrex 162-163

Recruitment

Access Engineering Corporation ... 338
Atomic Personnel 338
Ball Aerospace 339
Career Opportunities, Inc. 340
CCPO-Crystal City 341
Charles A. Binswanger 340
CLEO 338
Cochran, Cochran, & Yale 338
Department of Defense 340
Harris Corporation 338
Intel Corporation 335
Martin Marietta-Orlando Aerospace 337
Photocircuits 334
Riker Personnel 338
Search Northwest 340
Southwest Technical 340
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The First Logic Programmer dedicated to PAL* and IFLs.



Stag ZL30. The Next Logical Development

The new Stag ZL30 is the most cost-effective **programmable logic development system** available. Capable of programming and vector-testing all current 20, 24 and 28-pin PAL* and IFLs, without the need for plug-in modules, the ZL30 can also be used as an aid in the development of fuse patterns. New devices will be catered for by simple firmware changes.

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Stag worked hand-in-hand with all major semiconductor manufacturers throughout the development, resulting in an approved product with future capability to meet the rapidly changing technology.

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As part of a high-level development system, ZL30 can be remotely controlled via a choice of interfaces – RS232C or IEEE 488. In addition, this advanced Stag unit features a universal handler interface for driving any standard automatic device handler.

To find out more about the ultimate programmable logic development system, contact:

stag

Stag Micro Systems Inc,
528-5 Weddel Drive, Sunnyvale, CA 94089
Tel: (408) 745-1991
Telex: 910-339-9607

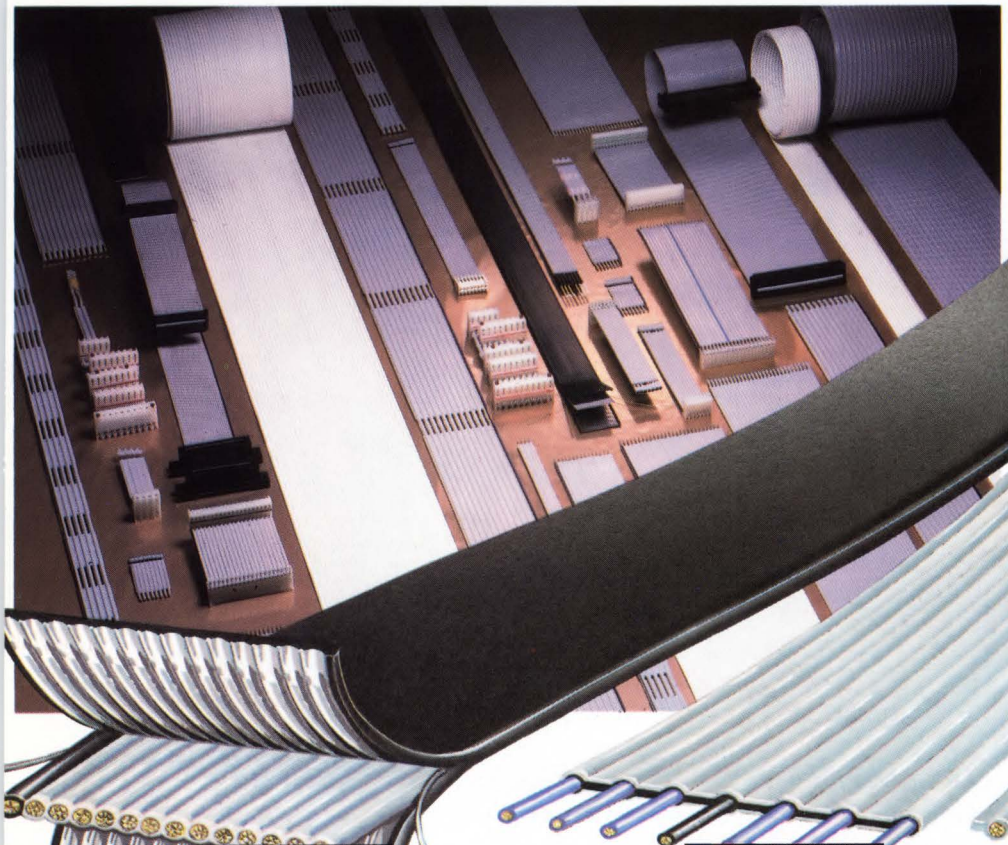


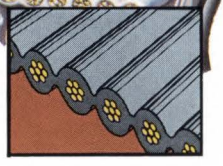
"*PAL is a registered trademark of Monolithic Memories Inc."

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CIRCLE 133

Molex cable: Our best kept secret is out!

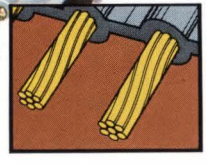




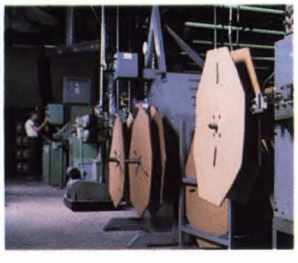
.050″Foil Shielded/ Foil Ground Plane Cable with zip-lines for fast, easy jacket removal.



.100″ and .156″ Poly-shield Cable. The unique shielding can be stripped in one simple step.



.050″, .098″ (2,0mm), .100″ and .156″ PVC insulated ribbon cable. Available with solid, stranded and top-coated conductors.



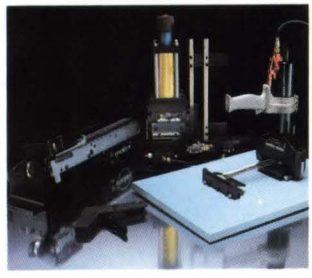
The word is out. Molex now makes over 20 types of planar cable on .050″, .098″ (2,0mm), .100″ and .156″ centers. Today our growing line of cable products extends from solid and stranded-conductor flat cable to our latest foil shielded cable for longer distance, high frequency EMI/RFI shielding applications. All are available in bulk quantities for the high volume cable user.

To accompany these cable products, Molex also offers a broad range of compatible connector products and application tools.

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To find out how Molex can lower the applied costs of your interconnection system, contact the Molex office nearest you.



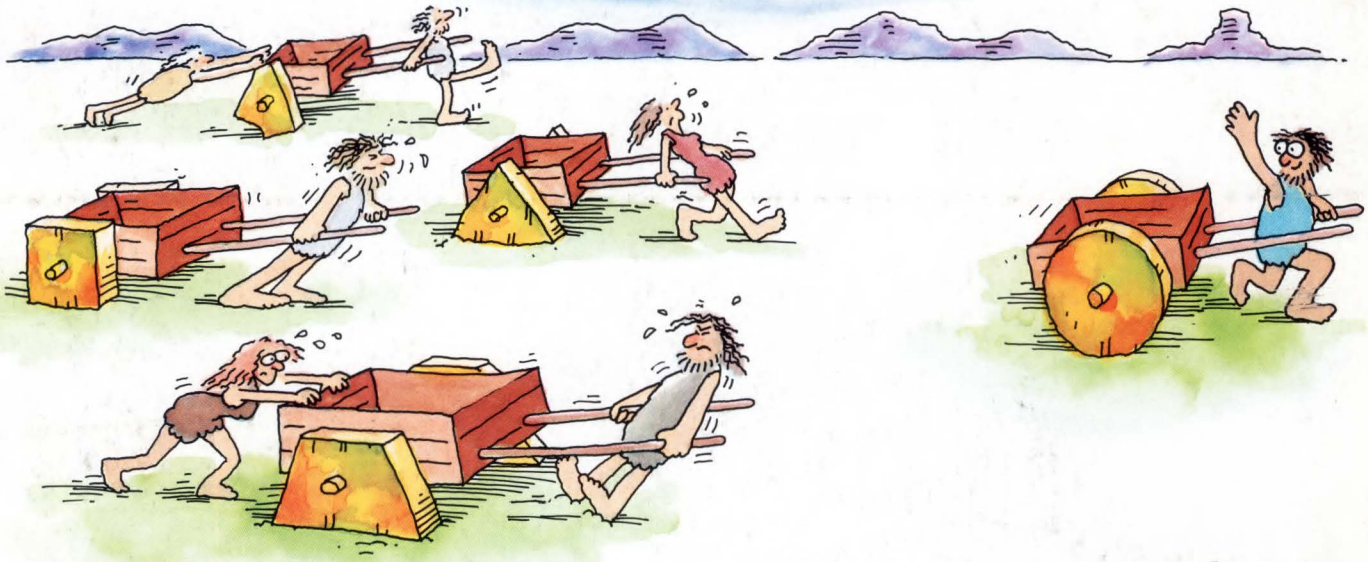
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Far Eastern Headquarters: 5-4, 1-Chome, Fukami-Higashi, Yamato-Shi, Kanagawa Pref., Japan 242 Phone: 462-614500 Telex; 781-03872486

CIRCLE 132

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*Licensing Agreement, ZyMOS Corporation.

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CIRCLE 133