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FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

SEPTEMBER 6, 1984

Multiprocessing 32-bit computer dynamically reassigns tasks for each added CPU

ANALOG TECHNOLOGY

Technology Report:
Converters push toward the ideal

A-d chip works with 8- or 16-bit micros

Anti-aliasing filter shares a-d converter chip

Single chip monitors five power lines

Floating-point converter widens dynamic range

Analog I/O boards team up with VAX

Clocked v-f converter lifts performance specs

Product Report:
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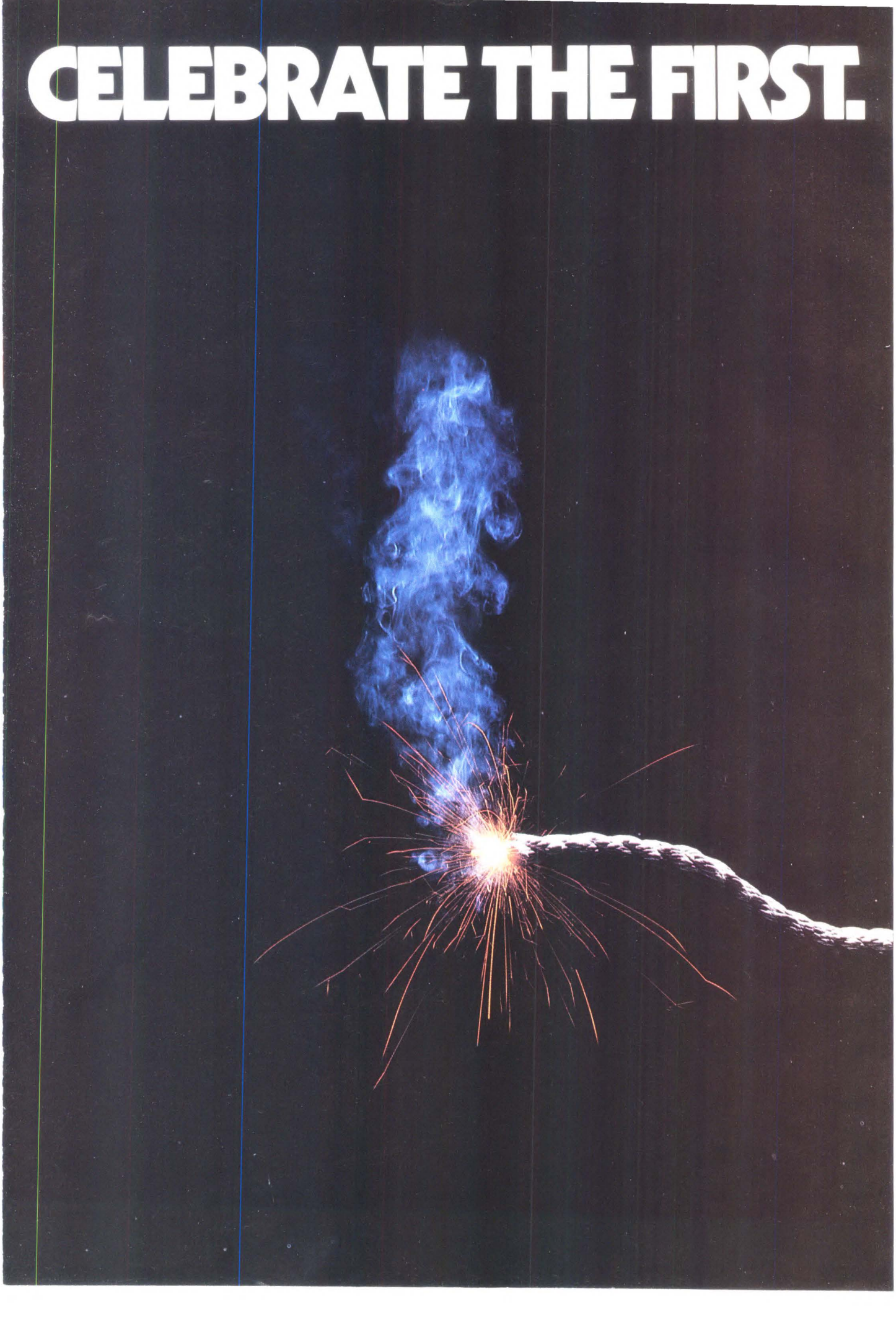

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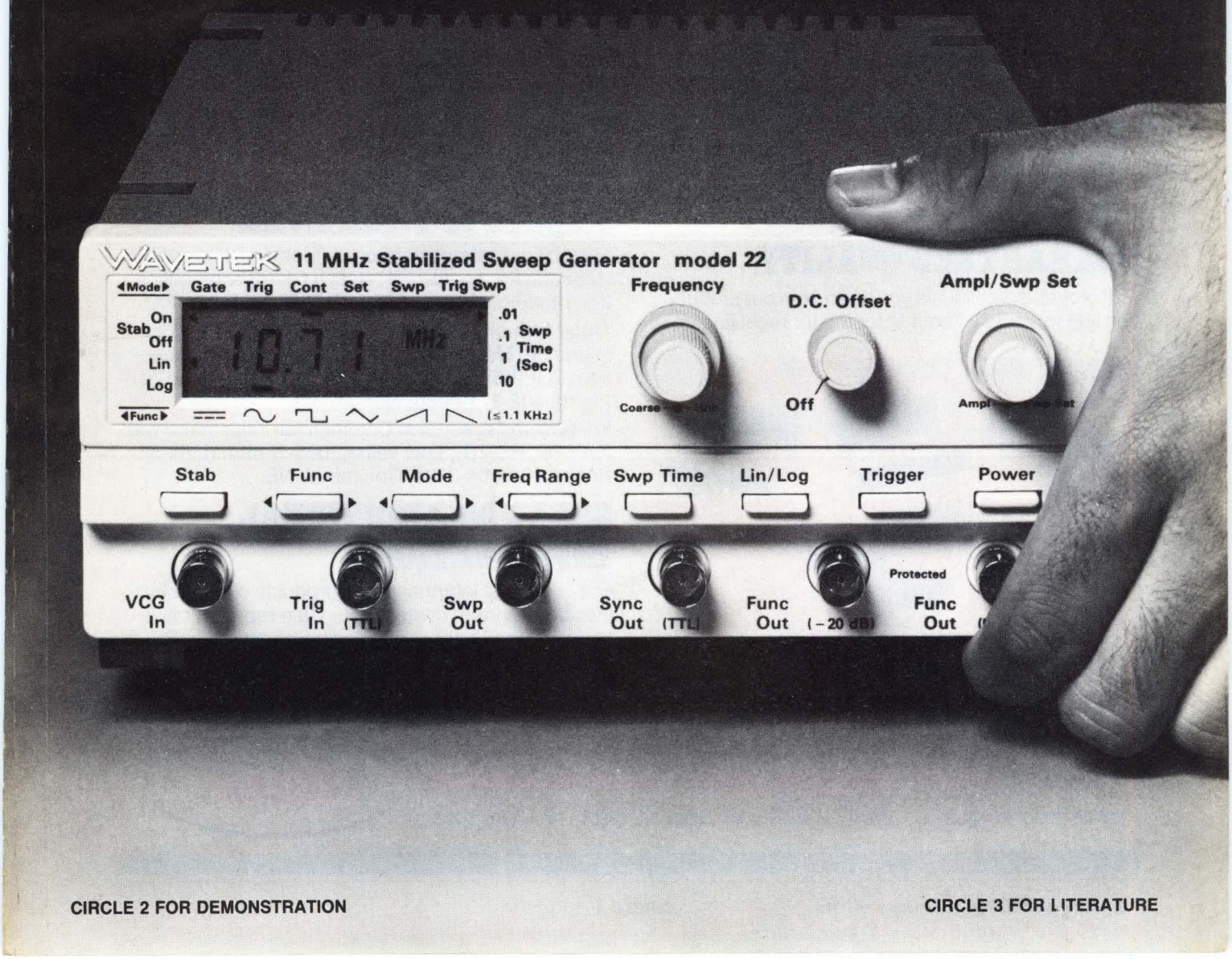

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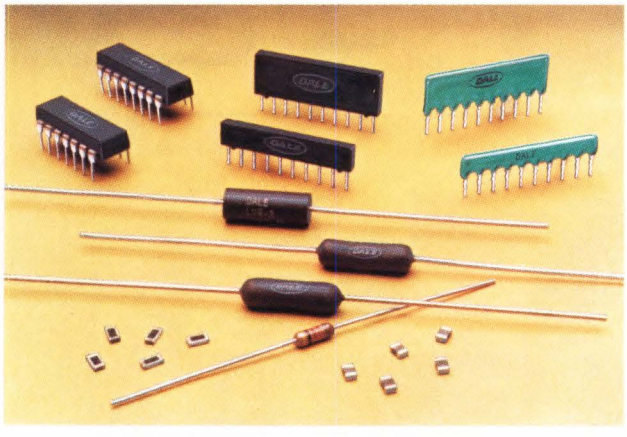

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BEHIND THE COVER

A designer's creative juices flow best in an atmosphere that promotes, rather than restricts, new ideas—where, as Dave Rodgers puts it, "you don't have to battle with people who say no just because something has never been done a certain way before." It was just such an atmosphere that the 18 founders of Sequent Computer Systems Inc. hoped to foster. So strong was the drive to work unencumbered that the team of engineers, administrators, and marketers got together in January, 1983, with no particular preconceptions about a product.

After three months of brainstorming and analyzing industry trends, it became clear that there was a bright future for a general-purpose multiprocessing computer—one that would fit the OEM's need for performance and configurability. That decided, one immediate goal was to hire Rodgers, who had helped design the VAX-11/780. And now he and Gary Fielland, whom he calls the "intellectual father" of the Balance 8000, have written this issue's cover story (p. 153) about that multiprocessing machine.

To be sure, it was Fielland's extensive background in system architectures and his grasp of the problems involved in synchronizing multiple microprocessors that led to the Balance 8000—a machine that automatically distributes its processing load evenly and continuously among up to 12 independent processors, runs Unix-based software, and automatically reconfigures itself as extra processors, memory controllers, and I/O modules are added to it. Further, it was Fielland who came up with the idea for the system link and interrupt controller chip, which manages the computer's global interrupt system, controls its cache semaphores, and forms the core of a packet-based communication system.

The new company's willingness to take risks was also a factor in getting the complex design up and running exactly a year from its inception. In Rodgers' understated way of speaking, it was "a much more rapid cycle than I was used to."

Today, though its engineers now number 45, Sequent still maintains its air of adventure. To Fielland, it brings the joy of seeing his ideas fleshed out and working. To Rodgers, it means "having a measurable impact on the company, seeing how you personally have changed it."

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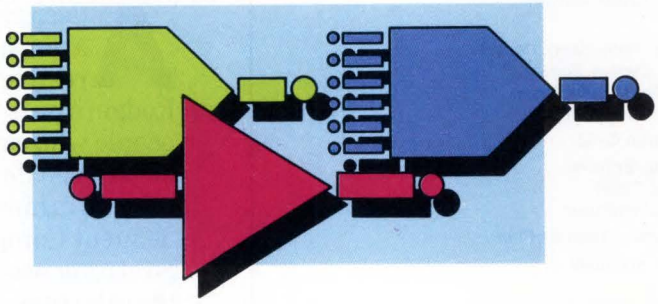

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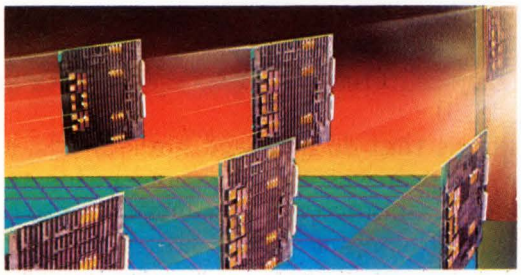

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Cover illustration by Jim Kinstrey

136,810 copies of this issue printed

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published biweekly with one additional issue in February, May, October and December and two additional issues in August by Hayden Publishing Company, Inc., 10 Mulholland Dr., Hasbrouck Heights, N.J. 07604. Subscription rates are $45 per year U.S. (foreign rates available upon request). James S. Mulholland Jr., President. Printed at Brown Printing Co., Waseca, Minn., Somerset Publishing Co., Somerset, N.J., and Wisconsin Cuneo Press, Milwaukee, Wis. Second-class postage paid at Hackensack, N.J. 07602 and at additional mailing offices.
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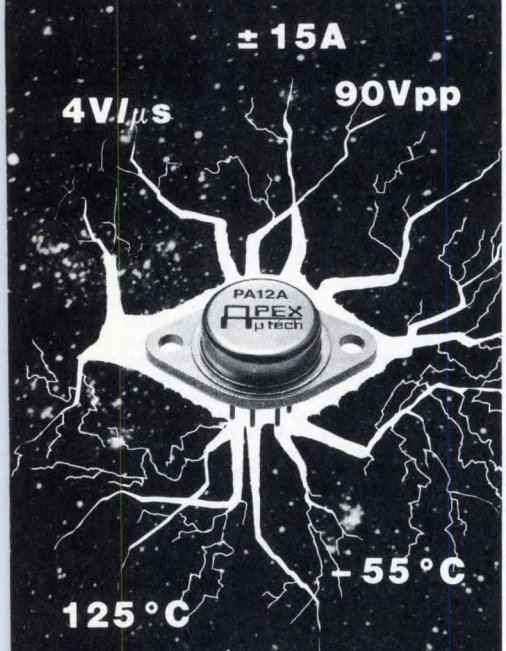

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Designers who work with data converters may have found the land of milk and honey—a land filled with more functions per package, higher performance, and both CMOS and merged CMOS-bipolar processes. Just how far these devices and their sample-and-hold companions have gone is the subject of this issue's Technology Report (p. 106), which is backed up with a diverse selection of contributed articles.

Leading the coverage are three analog-to-digital converters: a floating-point version that reaches a 20-bit dynamic range (p. 175), one that shares its chip with a microprocessor interface (p. 191), and another that teams up with an anti-aliasing filter for digital signal processing (p. 205). For sampling data, an analog I/O board supplies the speed and accuracy required by a VAX-based data acquisition system (p. 219).

For those applications that do not need high speeds, a voltage-to-frequency chip proves an able stand-in for an a-d converter (p. 235). Rounding out the contributed articles is a power-line monitoring chip that safeguards digital systems (p. 249).

Cover: Dynamic load-sharing computer 153

Twelve architecturally identical microprocessors can do the heretofore impossible for a multiprocessor computer: deliver twelve times the processing power of one CPU. Incremental expansion without degradation or bus contention is made possible by a 32-bit system that dynamically redistributes its processing tasks in order of priority and uses one copy of a Unix-based operating system.

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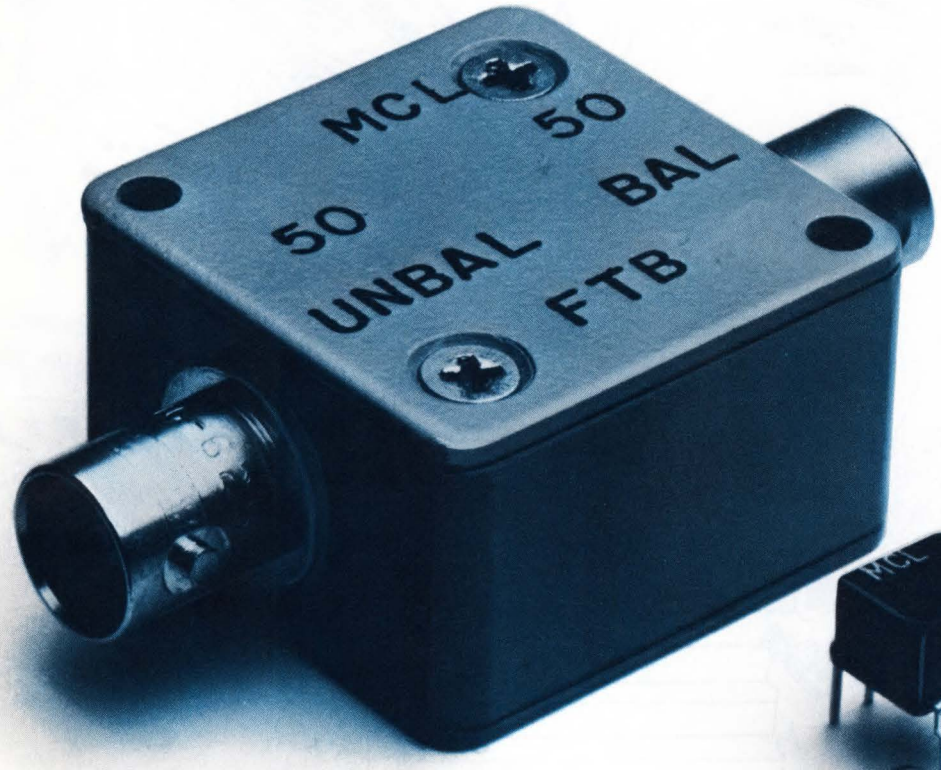

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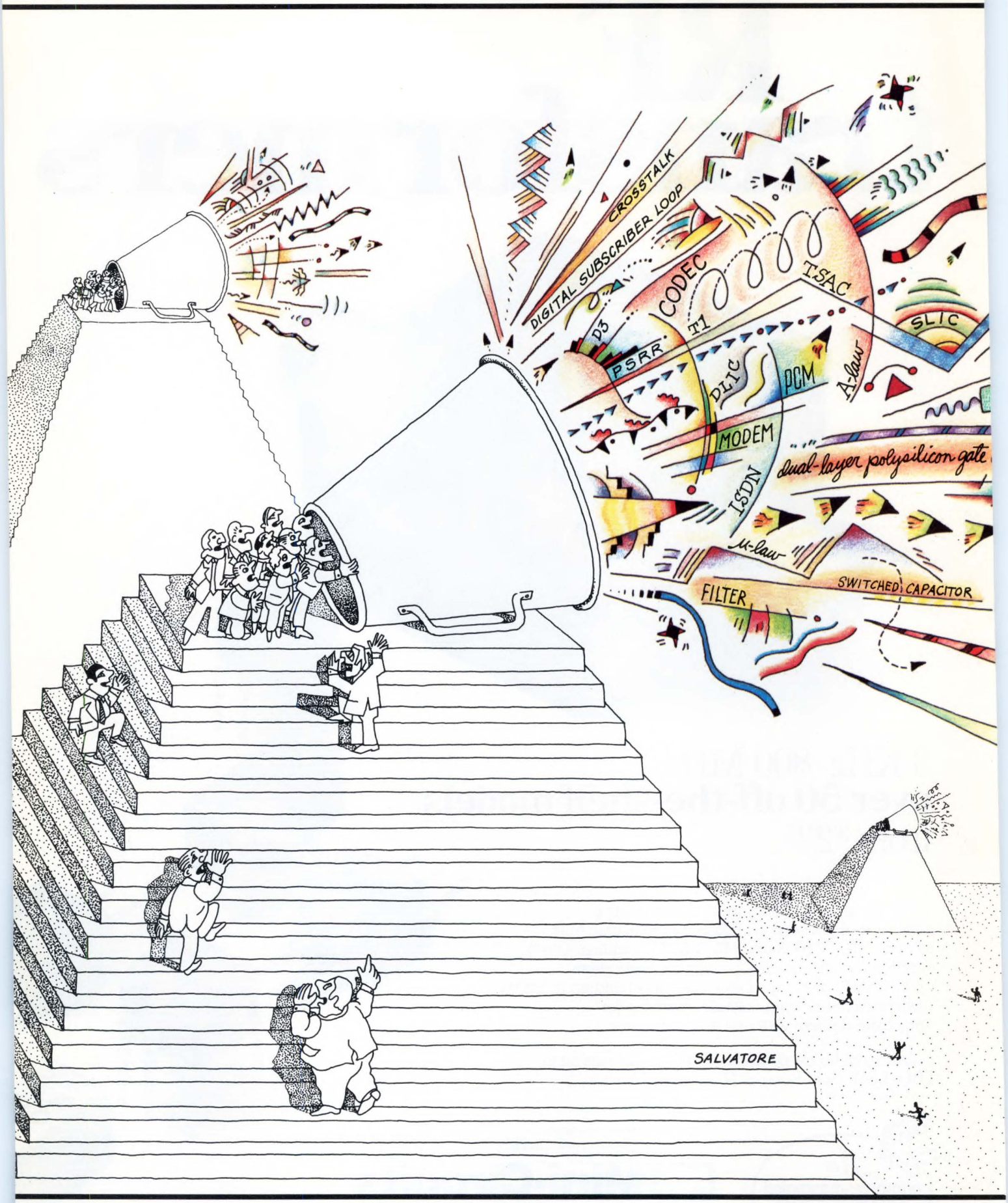
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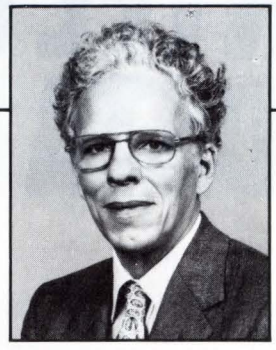

Digital designers need a crash course in analog technology

As keepers of the analog faith have long warned, digital designers are quickly facing a day of reckoning. It will soon become mandatory that digital designers not only be able to understand analog technology but also be able to operate in what is to them a nebulous and inexplicable world. A world, for example, in which industrial control systems often must handle fast nanovolt and kilovolt signals in close proximity without interference and to within 0.0015% accuracy.

In addition to pure physics, two other reasons will force the digital designer to learn the analog trade: a demand for top functionality in one package and the obvious shortage of analog specialists.

With logic speeds reaching for the microwave region, parasitic capacitances and inductances will soon turn sharp pulses into near sine waves.

Those degraded pulses must not be further distorted by logic inverters or gates, which are actually nonlinear amplifiers. Although the pulses start out reasonably large, if they travel any distance, attenuation also occurs, making the interference in noisy environments a critical factor.

Even in moving magnetic memories, the signals coming off the read heads are truly linear and must be processed carefully to determine whether they are logic 1s or logic 0s. Moreover, if these pseudopulses emanate from the latest hard-disk drives, they demand amplifier bandwidths of 50 to 100 MHz. To complicate the matter, the signals, which are extremely small to start with, could suffer from the noise of spindle motors.

Designers of circuits handling fast high-voltage or high-current pulses face similar pseudo-analog problems. For instance, a 100-A power MOSFET can turn off in less than 1 μs. However, the di/dt effects in parasitic pc-board and package-lead inductances may turn them on again. Pc-board wiring resistance, as well as source-drive impedance and current output, must be minimized for guaranteed turn on and turn off. The high input capacitance of 15,000 pF also must be charged from the source—through the resistance—in under 1 μs.

Squeezing more functions into one package has prompted strong interest in putting digital and analog functions on one chip and their diverse signals on the same board. As a result, digital designers are being asked to handle analog signals, as well as the more familiar digital ones. Frequently, the digital designers determine which op amps, comparators, or converters should be used.

Those designers may think that trusty analog engineers will be as helpful in designing the new boards as they have been in the past. That luxury may not exist much longer—the shortage of experienced analog designers is significantly more acute than that of their colleagues.

Digital designers, dust off your original analog computer—your slide rule—get out your trusty handbook, and pay heed to the real world. It's later than you think.

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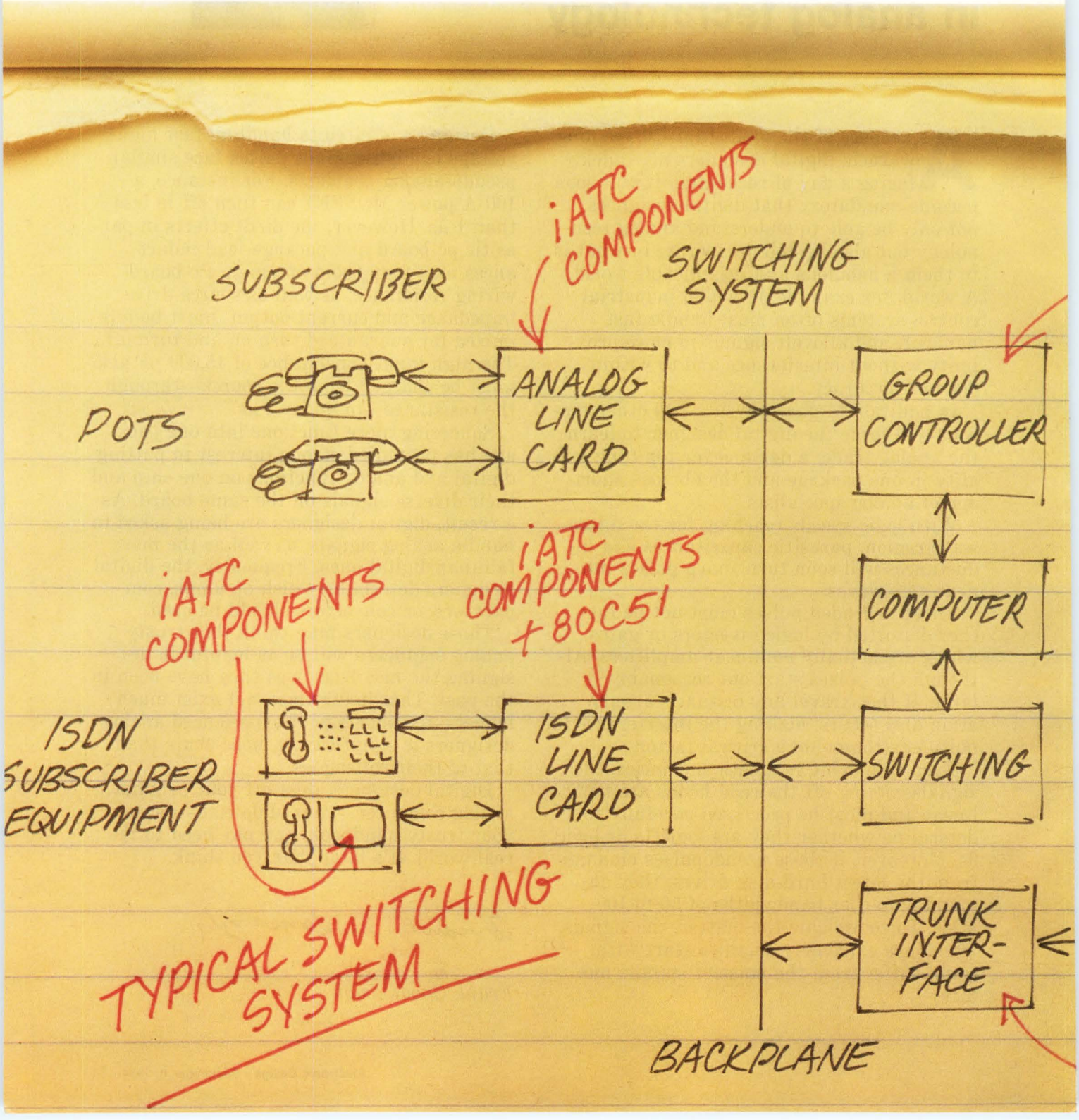

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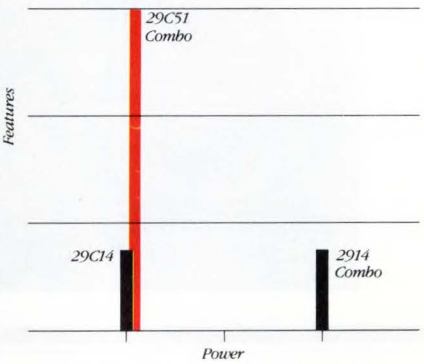
Developed for use with the 29C51, the 2952 Line Card Controller provides the bridge to ISDN upgrades.

It can control up to 16 subscriber lines at once, plus manage all voice and data transfers between the backplane and the line circuits. This includes matching time slots on PCM highways and intelligent interface to a control highway.

Although the 2952 can interface with just about any part of your system it's optimized for use with Intel's 80C51 microcontroller and the Intel iAPX family of microprocessors.



The high performance 29C51 offers the benefits of low power with more features than conventional NMOS.

Which means your telecommunication system design can be virtually unlimited in scope.

Together, the 29C51 and 2952 will work with every other iATC component. Now. And in the future.

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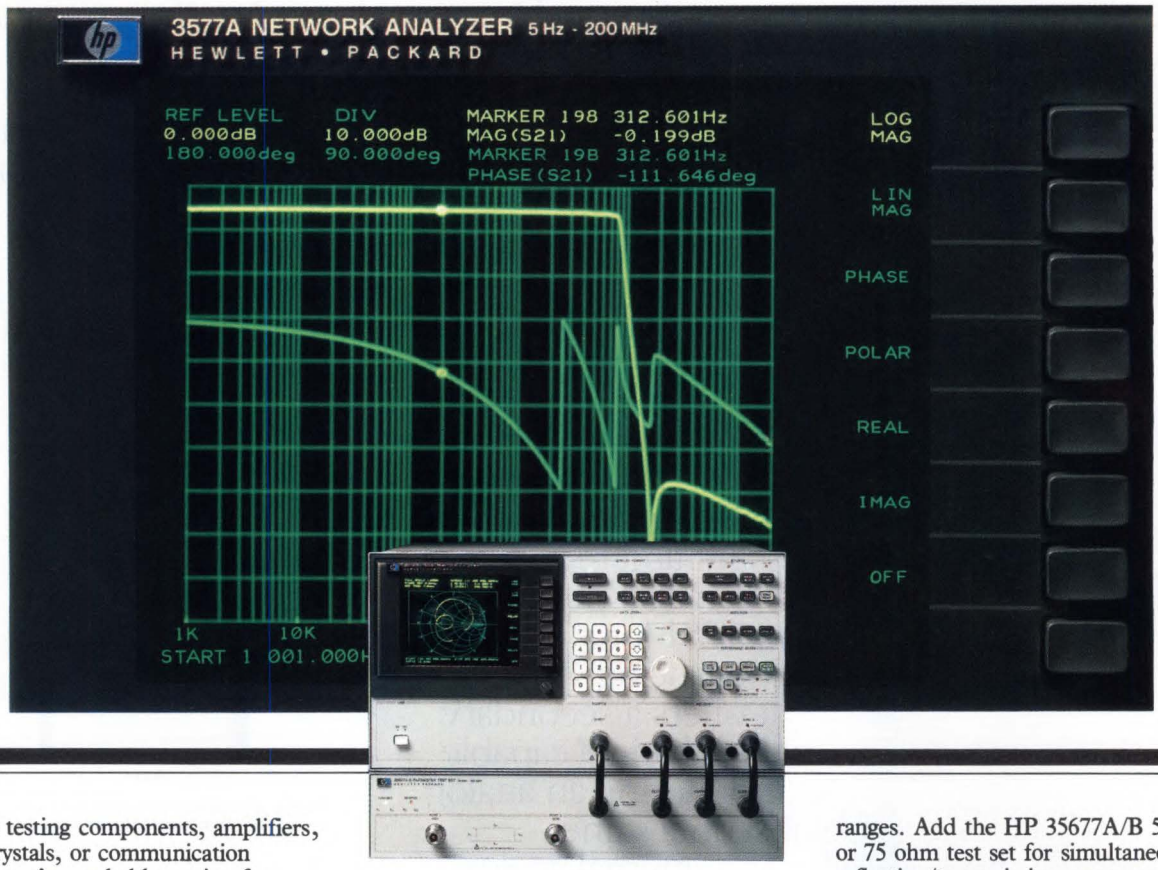
Finally, high-performance network analysis from 5 Hz to 200 MHz ...for only $23,500*.



If you're testing components, amplifiers, filters, crystals, or communication systems, you're probably paying for bandwidth you don't need. Or you're getting significantly less performance than you really want. But not any more. Because with the HP 3577A Network Analyzer, you get precision measurements from 5 Hz to 200 MHz at an affordable price.

Swept Frequency Coverage. The HP 3577A's internal synthesized source lets you sweep as narrow as 10 milliHz or as broad as 200 MHz. With accurate and stable start, stop, and CW frequency selection to 0.001 Hz resolution.

Magnitude/Phase Accuracy and Resolution. With three independent receiver inputs, the HP 3577A can make accurate magnitude and phase measurements over a 100 dB dynamic range. Sensitivity is -115 dBm in a 1 kHz BW. Better than -130 dBm in a 1 Hz BW. Plus, you can resolve to 0.001 dB magnitude and 0.005 degree phase.

Versatile Group Delay Measurements. Swept group delay measurements are yours to 1 ps resolution. Selectable frequency aperture between 0.5% to 16% of span lets you optimize each measurement for the situation at hand.

Introducing the HP 3577A Network Analyzer

But that only scratches the surface. You can display measured data in rectangular, polar, Smith, or log (Bode) formats. Perform arithmetic on trace data, use the autoscale function for bringing a measurement on scale quickly, get hardcopy output using the direct HP-IB plotter control. Plus true vector averaging, electronic line stretch, and selectable input impedances.

Price, performance, and convenience... they combine to make the HP 3577A the ideal solution.

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Disc Manufacture. With data rates pushing higher all the time, traditional digital logic and read/write amplifiers require precision analog-type testing. The HP 3577A is the perfect choice for designing, verifying, and optimizing such circuits.

Put the HP 3577A to work on your design problem. The right bandwidth. Exceptional accuracy. Superior resolution. And low price. For complete details, contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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CIRCLE 10

A101302

READER FEEDBACK

Track record speaks for itself

I'm happy that your fine Newsfront story "1/4-in. Cartridge Drive Doubles Track Density to Store 134 Mbytes" [July 12, p. 44] recognizes data cartridges for what they are—a tremendously powerful, reliable, and cost-effective method of backing up computer systems.

A clarification is warranted, because of the assertion that our DC 600 data cartridge lacks mechanical precision. Nothing could be further from truth. In fact, the DC 600 has a four-year track record of excellent data exchange and reliability in the HCD-75 drive and the HP-7900 series of tape subsystems. In these systems, the cartridge supports one of the highest areal densities (640,000 bits/in.^{2}) in the business. At 64 tpi and 10,000 bpi, one cartridge can store 67 Mbytes formatted.

Peter N. Holste
Public Relations Department
3M Co.
St. Paul, Minn.

Establishing the right connections

I read with interest the Design Solution in your June 28 issue ["Dual-Mode Power Supply Works Either Linearly or as a Switcher," p. 294]. This is my area, and an innovative circuit interests me. Unfortunately, a number of typographical errors appeared to have crept into the schematic.

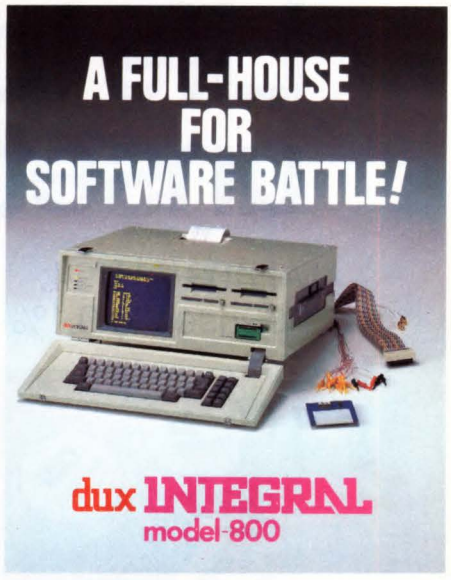
The catching diode, type MR851, is on the wrong side of the choke, so it won't catch the inductive kick. Since the diode is in the wrong place, switch S_{1A} also must be in the wrong location. Further, the 15-V zener diode in the lower left-hand corner of the circuit is also connected wrong.

Robert Bruce
Senior Engineer
AIL Division of Eaton Corp.
Deer Park, N.Y.

The author replies: *I appreciate the opportunity to make the corrections Mr. Bruce suggests. On the schematic, the intersection of the catching diode, and the inductor should indicate a connection. A node should also be shown at the intersection of the 15-V zener diode and the base of the 2N2222 transistor. Incidentally, to handle a greater output current, two 2N3970 transistors can be used in parallel for the Darlington pair.*

On the right wavelength

The tough stance taken by Vincent Biancomano in his June 28th On Reflection [p. 11] may anger a few readers, but I think it hits the mark squarely. Even though the merits of regulation vs deregulation can be argued ad infinitum, the evidence thus far presented clearly confirms that when



INTEGRAL 800 is a complete package for software development, built around a Z80B, 6MHz CPU with 64KB RAM and using the CP/M™ operating system. Incorporating keyboard, twin 3.5" floppy disk drive, in-circuit emulator, display screen, PROM programmer and eraser, printer and multiple connection ports into a carrying case the size of a large briefcase, the INTEGRAL 800 is truly profitable for emulation, logic analysis and debugging that requires real-time and hardware tracing. Most importantly, the INTEGRAL provides a wide variety of utilities that allow the user to communicate with the VAX 11 (DEC), MDS (Intel) etc.. Also, 8 inch floppy disk drives can be connected to expand the system. (option)
There's no short cut to good software, but the dux INTEGRAL makes the job a whole lot easier.

Brief specifications:

CPU:	Z80B, 6MHz
Disk drives:	Twin 3.5" micro floppies, each with 720 KB storage
Display:	7" non-glare, amber CRT with 24 lines of 80 characters each
Keyboad:	ASCII plan with function keys
Printer:	40 columns on thermal paper
PROM programmer	Supports 2716, 2732, 2732A, 2764, 2764A, 27128, 27128A, 27256 and 27C256 with read, write and verify functions
PROM eraser:	UV with 10 min. timer
Target CPU:	Z80, Z80A, Z80B and C-MOS with clock up to 6MHz
Dimensions:	19.3(W) x 6.7(H) x 15.0(D) in 490(W) x 170(H) x 380(D) mm
Weight:	33 lb (15 kg)

Power requirements AC 115/230V, 50/60 Hz
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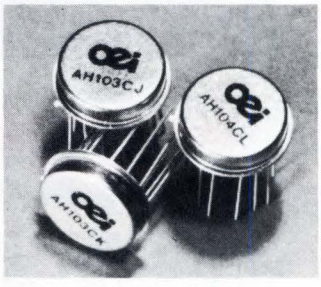

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CIRCLE 13
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READER FEEDBACK

deregulation is instituted, all hell breaks loose. Unfortunately, it is going to be very difficult for engineers to demand reestablishment of standards as long as FCC officials are nontechnical bureaucrats, content to make decisions that are compatible with economic factors. To clear up the problem, engineers may have to fight for better qualified and more even-handed decision makers, a virtually hopeless task.

Name withheld

Corrections

In the Aug. 9 cover article [p. 153], a regrettable but unforeseeable concatenation of errors eliminated or misnamed the hatching of elements in three figures. In Fig. 3, the ellipse at the extreme right should be cross-hatched. In Fig. 4, p. 163, the uppermost row of four ellipses should be dotted and the ellipse within the oblong should be cross-hatched. In Fig. 5, page 166, the circle labeled "sensor usage violations" should show blue lines.

Apologies to Energetec Systems Inc. (Lisle, Ill.), whose name we misspelled in our August 9 letters column while we were trying to correct a goof in our June 28 Product Report on switching power supplies. The perpetrator is now writing "I will not misspell Energetec Systems" 500 times on his editing terminal.

ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 8031 AND 8051 ALTERNATIVES.

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RAM (x8)	192	192	192	64	64
I/0 Lines	32	32	56	32	23
Serial Comm.	UART	UART	UART	—	—
Counters	2 x 16	2 x 16	2 x 16	1 x 16	1 x 16
Expansion Bus	65K	16K	16K	—	4K
Interrupts External Internal Host	6 4 —	6 4 —	6 4 —	3 1 —	4 1 2
Standby RAM (mW)	12	12	12	35	—
Package	64-pin QUIP	40-pin DIP	64-pin QUIP	40-pin DIP	40-pin DIP
Replaces	8031	8051		8048/49	8041

Our R6501Q microprocessor provides an alternative to the 8031. This "super microprocessor" device extends the R6500 family with four new bit manipulation instructions, and offers 192 bytes of RAM, two 16-bit counters, a serial (UART) port, 32 I/O lines, plus a full 65K address bus.

In addition, the R6500/11 or R6500/12 microcomputers can end your search for an 8051 alternative. The R6500/11 has all the features of the R6501Q, plus 3K of ROM, 32 I/0 lines—or 56 I/0 lines with the R6500/12—and address expansion to 16K is available.

If you're looking for an 8048/49 replacement, look into our R6500/1 microcomputer—its in over half the world's 5" hard disks. With 2K ROM, 64 bytes of RAM, a 16-bit counter and 32 I/0 lines, it's ideal for moderate sized jobs.

And if you're waiting for an 8041 to off-load tasks from your central CPU, look at the R6500/41. It has 1.5K ROM, 64 bytes of RAM, a 16-bit counter, multiplexed address expansion to an additional 4K and a host bus that talks 8050/Z80 or 6500/6800.

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U.S. MEETINGS

Defense Computers-Graphics '84, Sept. 10–13. Convention Center, Washington, D.C. Dorothy Bomberger, DCG '84, 2033 M Street, N.W., Suite 333, Washington, D.C. 20036; (202) 775-9556.

EASCON '84, Sept. 10-12. Shoreham Dunfey Hotel, Wash., D.C. Larry Whicker, LRW Assoc., 1218 Balfour Drive, Arnold, Md. 21012; (301) 765-7264.

1984 Symposium on VLSI Technology, Sept. 10–12. Vacation Village, San Diego, Calif. Dr. Lewis M. Terman, IBM T.J. Watson Research Center, PO Box 218, Yorktown Heights, N.Y. 10598; (914) 945-2029.

10th Annual Advanced Control Conference, Sept. 10-13. Fowler Hall, Stewart Center, Purdue Univ., W. Lafayette, Ind. Edward Kompass, Control Engineering, 1301 S. Grove Ave., PO Box 1030, Barrington, Ill. 60010; (312) 381-1840.

Electronic Imaging '84, Sept. 11–13. Westin Hotel, Copley Place, Boston, Mass. Electronic Imaging '84, 2 Park Ave., New York, N.Y. 10016-5667; (212) 340-9780.

Midcon/84 and Mini/Micro Midwest/84, Sept. 11–13. Dallas Convention Center, Dallas, Tex. Nancy Hogan, Electronic Conventions, Inc., 8110 Airport Boulevard, Los Angeles, Calif. 90045; (213) 772-2965.

UNIX Systems Expo/84, Sept. 11–14. Convention Center, Los Angeles, Calif. Sally Nestler, Computer Faire, Inc., 181 Wells Avenue, Newton, Mass. 02159; (617) 965-8350.

Voice Input/Output Systems Applications Conference '84, Sept. 11–13. Marriott Crystal Gateway Hotel, Arlington, Va. Leon Lerman, AVIOS, PO Box 60940, Palo Alto, Calif. 94306; (408) 742-2539.

1984 ASM Materials Science Seminar, Sept. 15–16. Westin Hotel, Detroit, Mich. Prof. B.W. Wessels, Technological Institute, Northwestern University Evanston, Ill. 60201; (312) 492-3219.

The Solid Modeling Revolution, Oct. 15–16. The Sheraton Tara Hotel, Farmington, Mass. Lorraine Mazza, Management Roundtable, Inc., 824 Boylston St., Chestnut Hill, Mass. 02167; (617) 232-8080.

Compcon Fall '84, Sept. 16–20. Hyatt Regency/Crystal City, Arlington, Va. Gerrie Katz, Small Computer (R)evolution, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

DataStorage 84, Sept. 17–19. Fairmont Hotel, Denver, Colo. Terri Noble, Cartlidge & Assoc. Inc., 4030 Moorpark Avenue, Suite 205, San Jose, Calif. 95117; (408) 554-6644.

FOC/LAN 84, Sept. 17–21. MGM Grand Hotel, Las Vegas, Nev. Michael O'Bryant, Information Gatekeepers Inc., 138 Brighton Ave., Boston, Mass. 02134; (617) 787-1776.

1984 International Microelectronics Symposium, Sept. 17–19. Loews Anatole, Dallas, Texas. Glenn Dowler, International Society for Hybrid Microelectronics, PO Box 3255, Montgomery, Ala. 36109; (205) 272-3191.

Federal Computer Conference, Sept. 18–20. Washington Convention Center, Washington, D.C. Dallas Kinney, Conference Communications, PO Box 368, Wayland, Mass. 01778; (800) 225-5926 or (617) 358-5181.

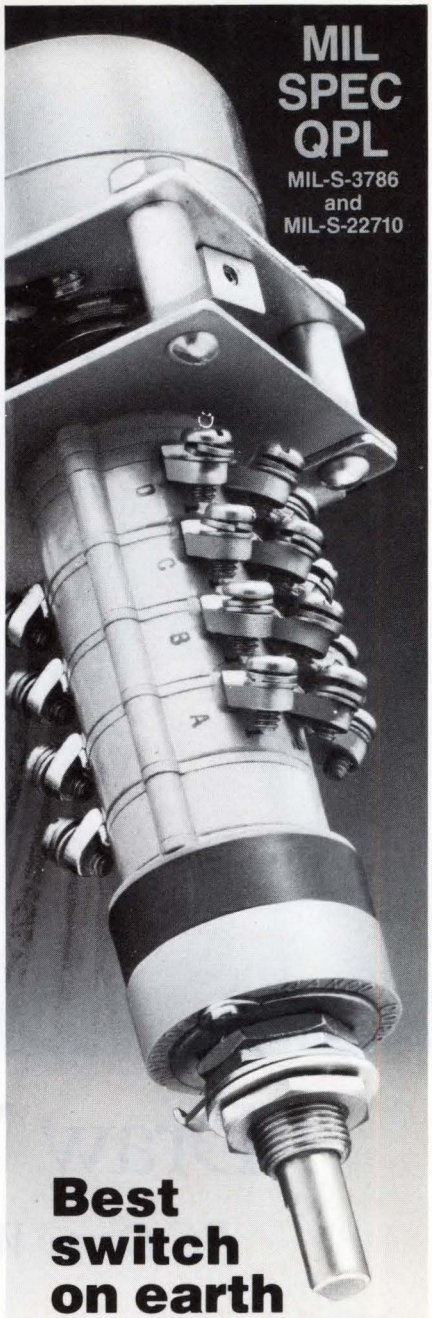
17th Annual Connectors and Interconnections Symposium, Sept. 19–21. Disneyland Hotel, Anaheim, Calif. Jim Pletcher, Electronic Connector Study Group, Inc., PO Box 167, Fort Washington, Pa. 19034; (215) 279-7084.

13th Annual Conference North American Thermal Analysis Society, Sept. 24–26. Marriott Hotel, Philadelphia, Pa. Hal Ferrari, Lederle Laboratories, Bldg. 65B, Pearl River, N.Y. 10965; (914) 735-5000, ext. 3443.

World Conference on Ergonomics in Computer Systems, Sept. 24–25, Los Angeles; **Sept. 25–26,** Dallas, Texas; **Sept. 26–27,** Chicago, Ill.; **Sept. 27–28,** New York, N.Y. Robert Baily, Computer Psychology Inc., 54 E. Main St., PO Box 16, Mendham, N.J. 07945; (201) 543-9009.

International Industrial Controls Conference and Exposition, Sept. 25–27. Philadelphia Civic Center, Philadelphia, Pa. Tower Conference Management Co., 331 Wesley St., Wheaton, Ill. 60187; (312) 668-8100.

Annual Convention and Exhibition Showcase of the North American Telecommunications Association (NATA), Oct. 1–4. NATA, 200 M St., N.W., Washington, D.C. 20036; (202) 296-9800. *(continued on p. 21)*



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CIRCLE 17

U.S. MEETINGS

(continued from p. 19)

AUTOFACT 6 Conference and Exposition, Oct. 1–4. Anaheim Convention Center and Disneyland Hotel, Anaheim, Calif. SME's Public Relation Dept., One SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-0777.

Information Management Exposition & Conference (INFO '84), Oct. 1–4. INFO '84, 999 Summer St., Stamford, Conn. 06905; (203) 864-0000.

Northcon 84 and Mini/Micro Northwest 84, Oct. 2–4. Seattle Center Flag Pavilion, Seattle, Wash. Nancy Hogan, Electronics Convention Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

IEEE International Conference on Computer Design (ICCD 84), Oct. 7–11. Rye Town Hilton, Port Chester, N.Y. Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

1984 ACM Annual Conference, Oct. 8–10. Hilton Hotel, San Francisco, Calif. Alexander Roth, 9900 Main St., Suite 303, Fairfax, Va. 22031; (703) 385-0211.

Electronics Manufacturing Technologies & Systems 84 (EMTAS 84), Oct. 9–11. North Carolina State University, Raleigh, N.C. Gerri Andrews, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500.

Circuit Expo '84, Oct. 16–18. Centrum, Worcester, Mass., Worldwide Convention Management Company, Box 159, Libertyville, Ill. 60048; (312) 362-8711.

Fifth Annual Assembly Technology Expo, Oct. 16–18. O'Hare Expo Center, Rosemont, Ill. Richard lewis, Assembly Technology Expo, 2400 East Devon Ave., Suite 205, Des Plaines, Ill. 60018; (312) 299-3131.

Maecon/84, Oct. 16–18. Cervantes Convention Center, St. Louis, Mo. Ohmcom/Maecon, PO Box 699, Utica, Miss. 48087; (313) 731-4551.

Unix Expo, Oct. 16–18. Sheraton Centre Hotel, New York, N.Y. National Expositions Co, Inc., 14 West 40th Street, New York, N.Y. 10018; (212) 391-9111.

International Test Conference 1984, Oct. 16–19. Franklin Plaza Hotel, Philadelphia, Pa. Harry Hayman, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

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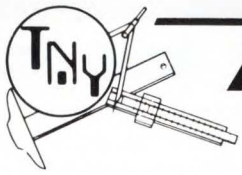

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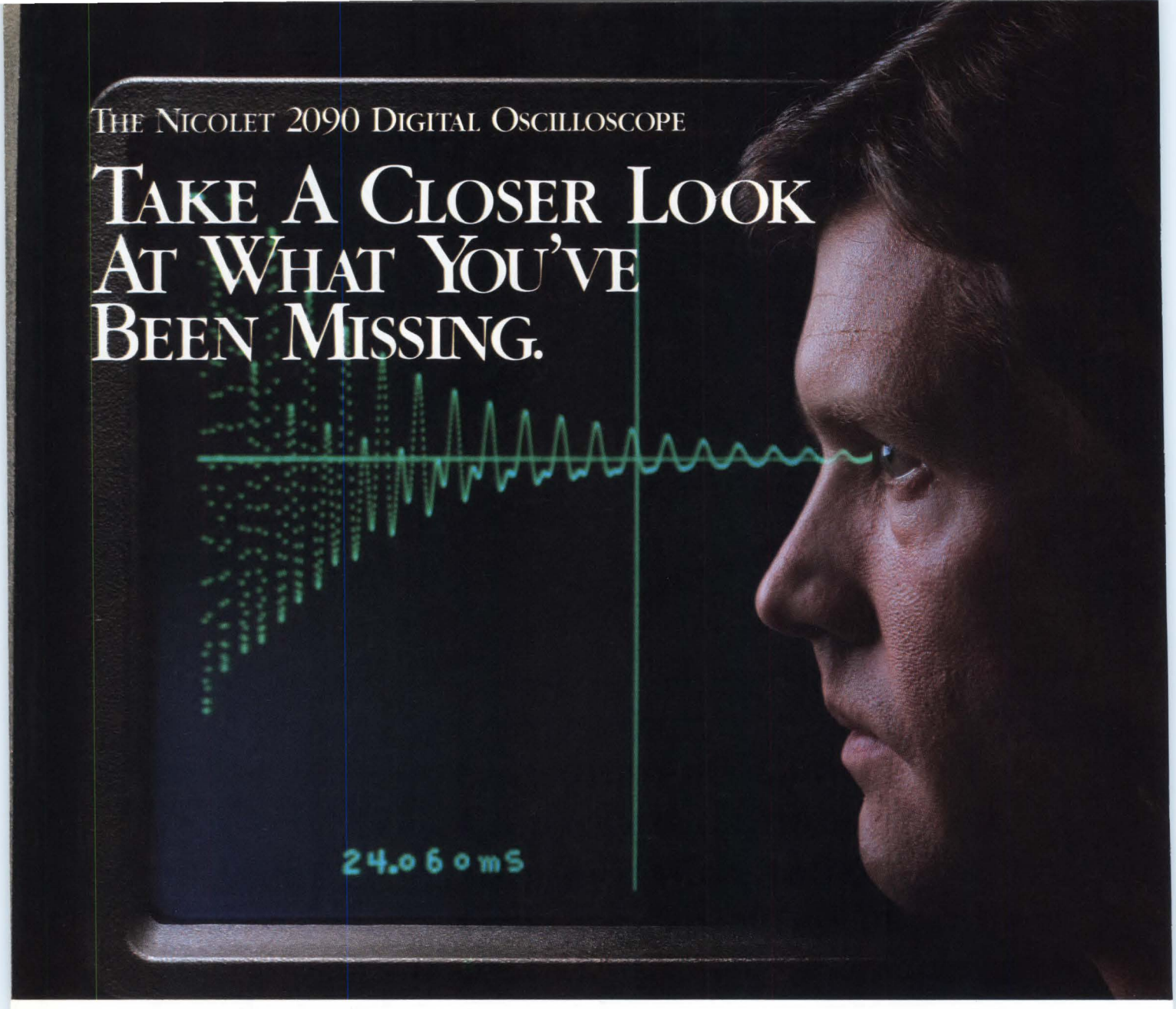

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the 2090 scope can be the front end of an entire analysis system. Not only that, the 2090's modular design allows you a choice of *four different plug-ins.* Pick the digitizer that's designed for your present application, and add other plug-ins to fit your expanding needs in the future.

SEE FOR YOURSELF.

Let us show you how easy the 2090 is to use. It's time *you* started benefiting from the tremendous digital advantage. Call us: **(608) 273-5008.** Or write: Nicolet Oscilloscope Division, 5225 Verona Road, Madison, WI 53711.

BRINGING DIGITAL PRECISION TO AN ANALOG WORLD

Nicolet

CIRCLE 24 FOR MORE INFORMATION

PERSONALLY SPEAKING

Semicustom circuits usher in new concerns about IC packaging

Just as gate arrays and standard cells have revolutionized logic technology, so will they affect packaging. The dual in-line package, the acknowledged industry standard for preceding generations of logic circuits, cannot keep pace with the explosion of semicustom logic chips, which command pin counts far beyond 64 pins. Though packaging issues are often placed on the back burner, this case is particularly hot, since it could well influence the success with which arrays and cells are designed into a system.

Fortunately, standardization efforts and concentrated developments in plastic leaded chip carriers and pin-grid arrays are keeping packaging in the forefront. JEDEC has already given standardization a top priority. For over a year, representatives from the semiconductor and chip packaging industries have been trying to hammer out the first specifications. A document for chip carriers will likely be completed later this month and will spell out a square-shaped package with as many as 144 pins, center spacings of 50 mils, and J-form leads that are rolled under the package.

Early next year, JEDEC plans to iron out the specifications for grid arrays with as many as 400 pins. Ten different families are in the offing, ranging from an array with 121 pins configured in 11 rows and columns to one with 400 pins arranged in 20 rows and columns. All will be based on 100-mil center spacings.

The need for a standardized pin count will squarely hit semicustom circuit users who are currently or are on the verge of investing huge sums into the test systems and specialized equipment needed for handling complex chips. To cope with the testing issue, several chip manufacturers are pushing for uniform placement of power-supply and ground pins, a move that would undoubtedly simplify testing while eliminating many costly testing fixtures.

Large capital investments are further pressing semiconductor makers to drop the cost of semicustom packages, particularly for arrays of 3000 to 10,000 gates and for standard cells with even greater gate complexity. Not surprisingly, plastic is emerging as the economical alternative to ceramic packages. The less-expensive circuit is set upon a small pc board, and then encapsulated in a high-temperature plastic mold. Plastic would also eliminate much of the gold found in ceramic packages. Altogether, system designers might expect to find a 4000-gate pin-grid array, housed in plastic, dropping in price from $55 to $37 in large quantities. Equally impressive, those savings might become a reality as early as next year.

Unless pin count and other packaging-related problems are resolved, system designers may take a wait-and-see attitude before moving head on into gate arrays and standard cells. Surely, the semiconductor industry has enough pull to prevent that from happening.

Martin Gold

Martin Gold

Introducing the newest member of

The HP 1630G...65 channels and maximize 16-bit system

First came the HP 1630A and the HP 1630D. One, a low-cost general purpose logic analyzer suited to the needs of the full development cycle. The other, with 16 channels of timing analysis and 27 of state, an invaluable tool for the hardware design engineer. Now Hewlett-Packard introduces the HP 1630G. With up to 65 channels of state analysis, it is the new standard for software design engineers working on complex new 16-bit microprocessor-based products. Plus, the ability to configure 8 of those lines for 100 MHz timing analysis gives you a logic analyzer system with investigative power and versatility for virtually all your needs.

Three new software overview modes let you nonintrusively monitor software performance and hardware/software interactions in real time.

The HP 1630G significantly expands on the software performance capabilities already introduced in the HP 1630A/D family members. In addition to time histograms that show execution-time distribution, and label histograms that show address activity, the HP 1630G gives you three new modes: program flow, time positional, and linkage measurements. *Program flow measurement* lets you monitor program activity based strictly on opcode accesses. This can help resolve confusions which may occur when histogramming by address, especially if the program generates inline code or if memory blocks are interspersed between sections of the program. *Time positional measurement* lets you measure the number of occurrences of an event per unit time. Use this to better understand the behavior of your system under a time-varying load. *Linkage measurement* measures the relative frequency of the activity between specific software modules. You'll find this mode invaluable when you want to monitor the transfer activity between a main program and a series of subroutines, for example. Take advantage of all these software performance analysis modes to rapidly

HP-IL

DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

HP 1630D

HP 1630A

HP's logic analyzer family.

advanced software analysis help you performance.

discover if your system is resource-limited or if, for example, poorly chosen program segmentation is causing too much time-consuming disc-to-memory swapping.

Time tagging gives you added insights into system functions.

In the state analysis mode, time tagging measures the time elapsed between each stored state. Make detailed absolute time measurements between states and known physical events. Or, use the mode to measure the total time from the trigger point to a particular state. Because time tagging is a single-pass activity, it is well suited to helping you identify inline sections of code that take longer to execute than anticipated.

Floppy disc interface and popular 16-bit microprocessor support.

On-board non-volatile memory keeps one instrument setup and your current disassembler instantly available at power-up. For even greater storage, the HP 1630G features direct compatibility with a number of HP disc drives such as the HP 9121S/D (the HP 9121D is illustrated). In one convenient 3 1/2" floppy you can now store data, state listings, timing diagrams, alternate disassemblers, and instrument setup configurations. For added flexibility, the HP 1630G supports all popular 8-bit, as well as the following 16-bit microprocessors: 68000, 8086, 8088, 80186, 80286, Z8001 and Z8002.

Our HP 1630G upgrade kit protects your previous HP investment.

If you've already invested in an HP 1630A or HP 1630D, but you feel you need the added capabilities of the HP 1630G, you'll be glad to know that an upgrade kit is available.

Compare the HP 1630G. At $12,100* it's even HP-IB programmable for fully automated measurements. To find out more about the HP 1630G or its companions the HP 1630A/D, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

* U.S.A. list price only.

HP 1630G

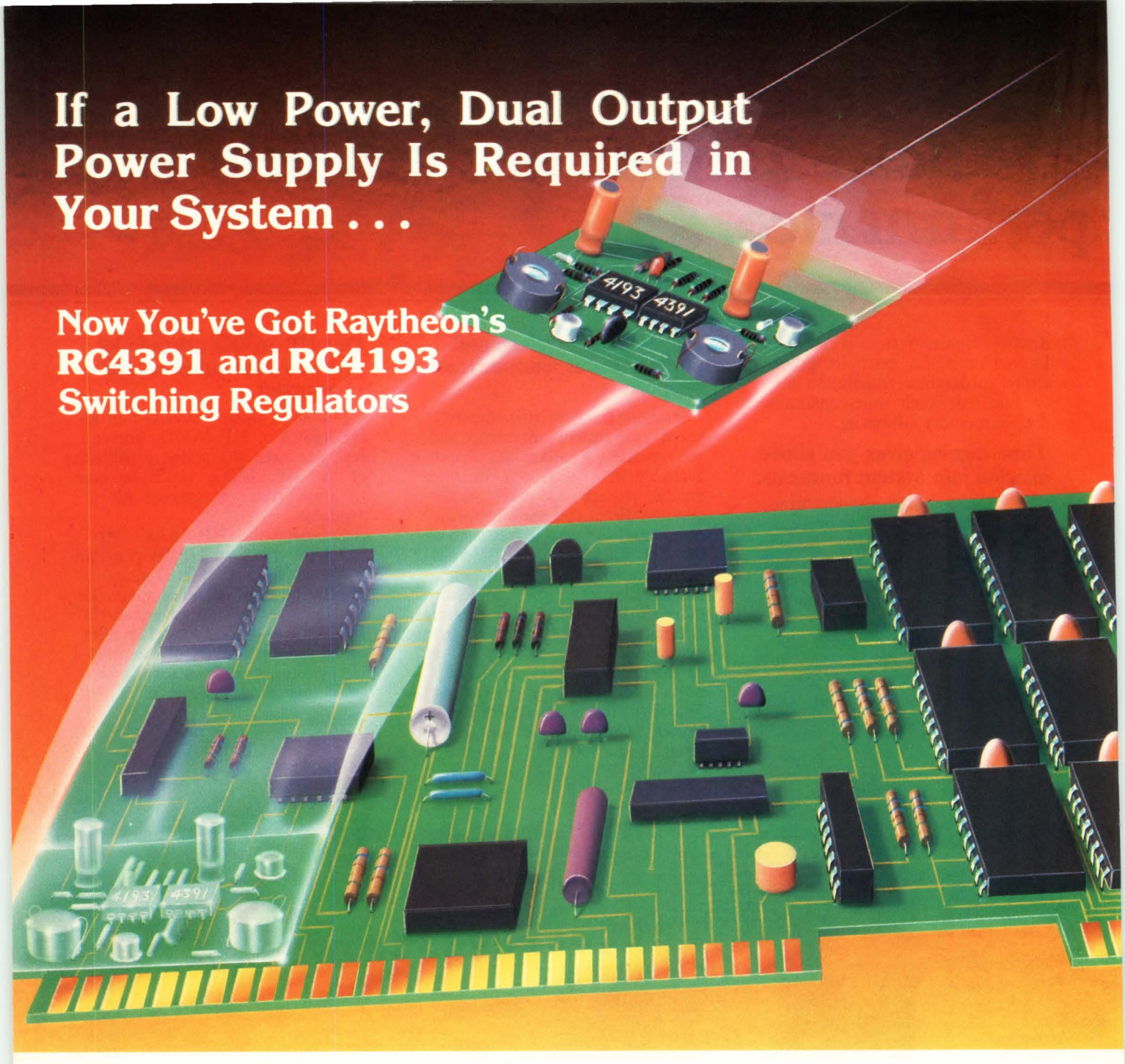
HEWLETT PACKARD

0801403

CIRCLE 20

If a Low Power, Dual Output Power Supply Is Required in Your System . . .

Now You've Got Raytheon's RC4391 and RC4193 Switching Regulators



The **RC4391** and **RC4193** are switch mode regulators each containing all of the active circuitry you need to build a switching regulator circuit.

You Get Flexibility: With Raytheon's **RC4391** inverting regulator and **RC4193** configured in the step-up mode, the designer can take an existing "on-card" voltage (typically 5.0 Volts or from a battery), and add just two inductors, transistors, steering diodes, and some passive components to configure an adjustable dual output power supply.

You Get Efficiency: No need for additional positive and negative "on-card" three-terminal regulation (typically required when using an external power supply). With the **RC4391** and **RC4193** the designer can achieve electrical efficiencies up to 70%. And both devices draw 135μA of quiescent current, are adjustable, and have internal circuitry to provide line and load regulation of less than 0.5% of the output.

You Get The Facts: Raytheon has data sheets on each product including theory of operation and a complete application note on a dual tracking power supply using the **RC4391** and **RC4193**.

Raytheon Company
Semiconductor Division
350 Ellis Street
Mountain View, CA 94043
(415) 966-7716

RAYTHEON
Semiconductor Division

CIRCLE 21

NEWSPULSE

Solid-state ceramic display competes head on with LCDs

The ubiquitous liquid-crystal display is going to face some sharp contention from an electro-optical ceramic display that outperforms LCDs in operating temperature range, response time, and viewing angle. The solid-state ceramic display, dubbed SCD, is built with a lanthanum-doped material called polycrystalline lead zirconate titanate (PLZT), which enables the ceramic display to work over −40° to +85° C without the heaters required by LCDs. Over that entire range, the SCD responds in 500 μs and affords a wide viewing angle of 160°. Developed by Motorola Inc.'s Ceramic Products Division (Albuquerque, N.M.), the display can be built with reflective, transreflective, and transmissive characteristics, thanks to the PLZT. Furthermore, it can change colors as a function of the operating voltage's amplitude. The material was originally developed at Sandia Laboratories (Albuquerque) for the Air Force.

Matchmaking efforts between software, hardware giants pay off

The HILO-2 software package has found a hardware home on the 32-bit HP 9000 Series 500 computer. The agreement between GenRad Inc.'s Engineering Test Products Group (Santa Clara, Calif.) and Hewlett-Packard Co. (Palo Alto, Calif.) calls for GenRad to also participate in HP's software supplier program, known as HP Plus. HILO-2 is a high-speed logic simulation package that has been running on a number of powerful 32-bit computers including those from IBM Corp. (Armonk, N.Y.), Apollo Inc. (Chelmsford, Mass.), and Digital Equipment Corp. (Maynard, Mass.). It also runs on advanced engineering workstations from Computervision Corp. (Bedford, Mass.), CAE Systems Inc. (Sunnyvale, Calif.), Metheus Corp. (Hillsboro, Ore.), and Valid Logic Systems Inc. (Mountain View, Calif.).

IBM broadband communications system joins 1000 PCs

Linking more than 1000 personal computers, a network announced by IBM Corp. (Armonk, N.Y.) is the first of its kind to operate over broadband channels. The PC Network uses the CSMA/CD arbitration scheme, as well as the localNet/PC protocol developed by Sytek Inc. (Mountain View, Calif.). With coaxial cable as the transmission medium, it handles 2 Mbits/s. Hardware consists of a network adapter, associated translators, and retransmitters. The network adapter itself has an 80188 microprocessor, an 82586 communications controller, a broadband rf modem, a BIOS (basic I/O system) ROM, and related circuitry.

EIA chooses standard for consumer electronics bus

A technical steering committee of the Electronics Industries Association meets this week to consider proposals for a standard consumer electronics bus. Buses of this kind link appliances to electronic systems, managing control, status, data, voice, and wideband analog signals. Contending for acceptance will be a digital small-area network codeveloped by Signetics Corp. (Sunnyvale, Calif.) and its parent

company, Philips International BV (Eindhoven, the Netherlands); HomeNET from General Electric Co. (Fairfield, Conn.); and a proprietary scheme from BSR Inc. (Blauvelt, N.Y.).

Philips and Signetics have announced a CMOS controller for their network that they hope will weigh the committee's decision in the favor of their bus. Combining two chips, the controller not only links different appliances but also allows ICs within equipment to rapidly share data.

Adaptable head substrate marks magnetic printer

A thin-film head, placed on a flexible substrate, opens the door to a new generation of nonimpact magnetic printers that can conceivably challenge laser-based printers. Developed by Ferix Corp. (Fremont, Calif.), the flexible head can conform to the many shapes of an adaptable drum; as a result the magnetic page printer that uses the head is—unlike laser units—virtually unaffected by flaws in the drum's surface and variations in inks and paper thickness. Thin-film recording coils that are sputter-deposited on the flexible substrate project the magnetic flux lines through the head, thereby magnetizing the drum's surface. As with other magnetic printers, a toner containing metal particles is attracted to the drum's surface and rolled out onto the paper. The Ferix printer lays down 240 dots/in. and produces about 10 pages a minute.

Smallest LAN interface satisfies military standards

The smallest local-area network interface yet for MIL-STD-1553 systems squeezes all required military functions into a single, 1.9-by-2.1-in. package. The BUS-65112 device, developed by ILC Data Device Corp. (Bohemia, N.Y.), has two fully redundant identical buses. Screened to meet MIL-STD-883 as well, the 78-pin hybrid owes its compactness to a monolithic chip design using proprietary gate arrays.

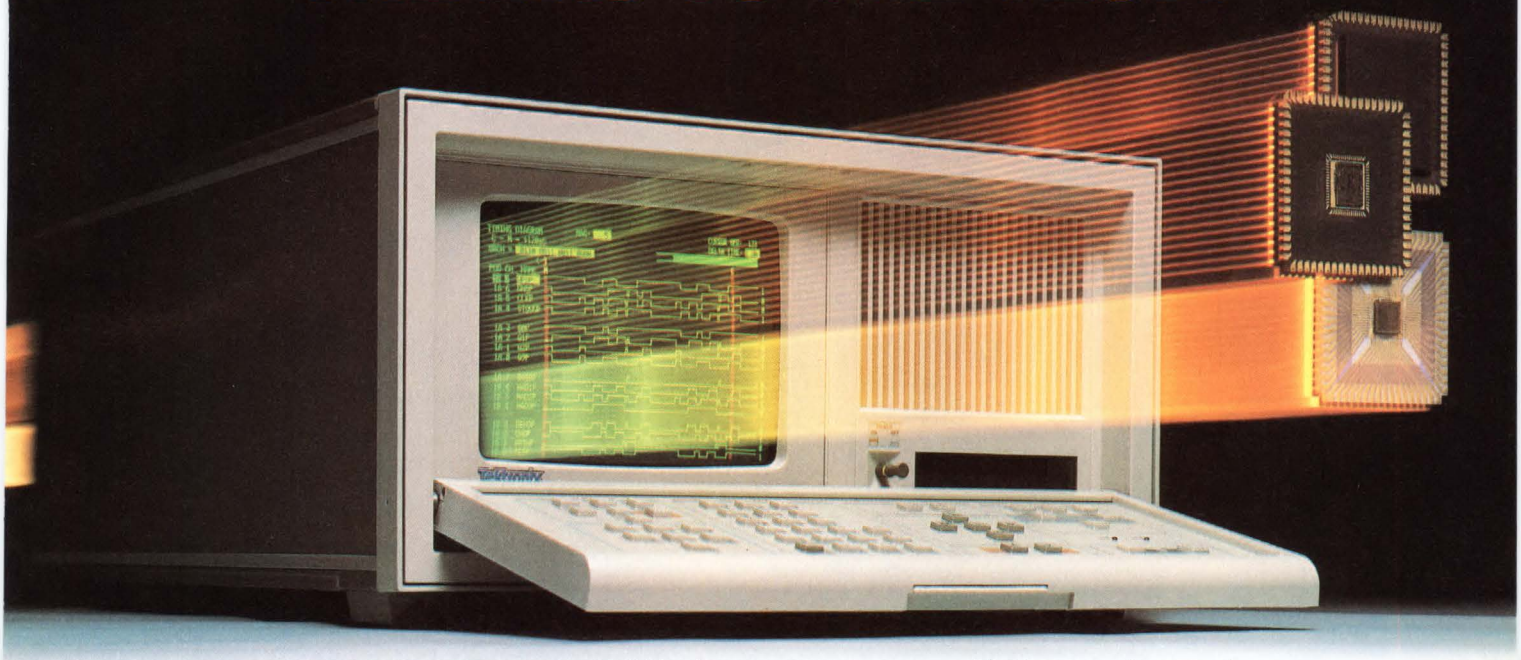
New PC-compatible computer uses 80286 processor

The first personal computer to use Intel's 80286 processor chip puts it to work supporting multiple users with a CSMA/CD communications protocol. The Personal Computer AT from IBM Corp. (Armonk, N.Y.) also works with an 8087 math coprocessor, as well as the familiar PC series of software, peripherals, and expansion cards.

Although the AT's internal data bus is 16 bits wide, provisions have been made on the motherboard's eight expansion slots to accept adapter cards from the older IBM PC family, which were developed for the 8088 processor and an 8-bit data bus. The computer additionally uses what is called a high-capacity 5¼-in. floppy-disk drive. The 80-track drive is double-sided, recording at 96 tpi and 9646 bpi.

TEK DESIGNLINK™ VLSI VERIFICATION SOFTWARE

VLSI VERIFICATION: NOW YOU CAN REALLY PUT THE DAS TO THE TEST!



If you thought the DAS 9100 was a powerful logic analyzer before, wait til you see what it can do now: VLSI prototype testing!

Tek's new 91DVV DesignLink™ VLSI Verification Software Package ties the DAS to a VAX computer to let you do interactive functional testing right at your benchtop.

Only the DAS, with its unique channel width and stimulus capability, could develop into this kind of personal test station.

91DVV software converts test vectors used by your simulator into a compressed DAS pattern generator program, then downloads to the DAS for stimulation of the prototype. Resultant outputs are automatically acquired and uploaded to the host, where 91DVV compares actual to simulator-predicted responses and displays the differences.

When it comes to VLSI prototype testing, DesignLink software now lets you bring the test to your bench. Call us today for all the facts on the first VLSI personal test station: 1-800-547-1512. In Oregon, 1-800-452-1877.

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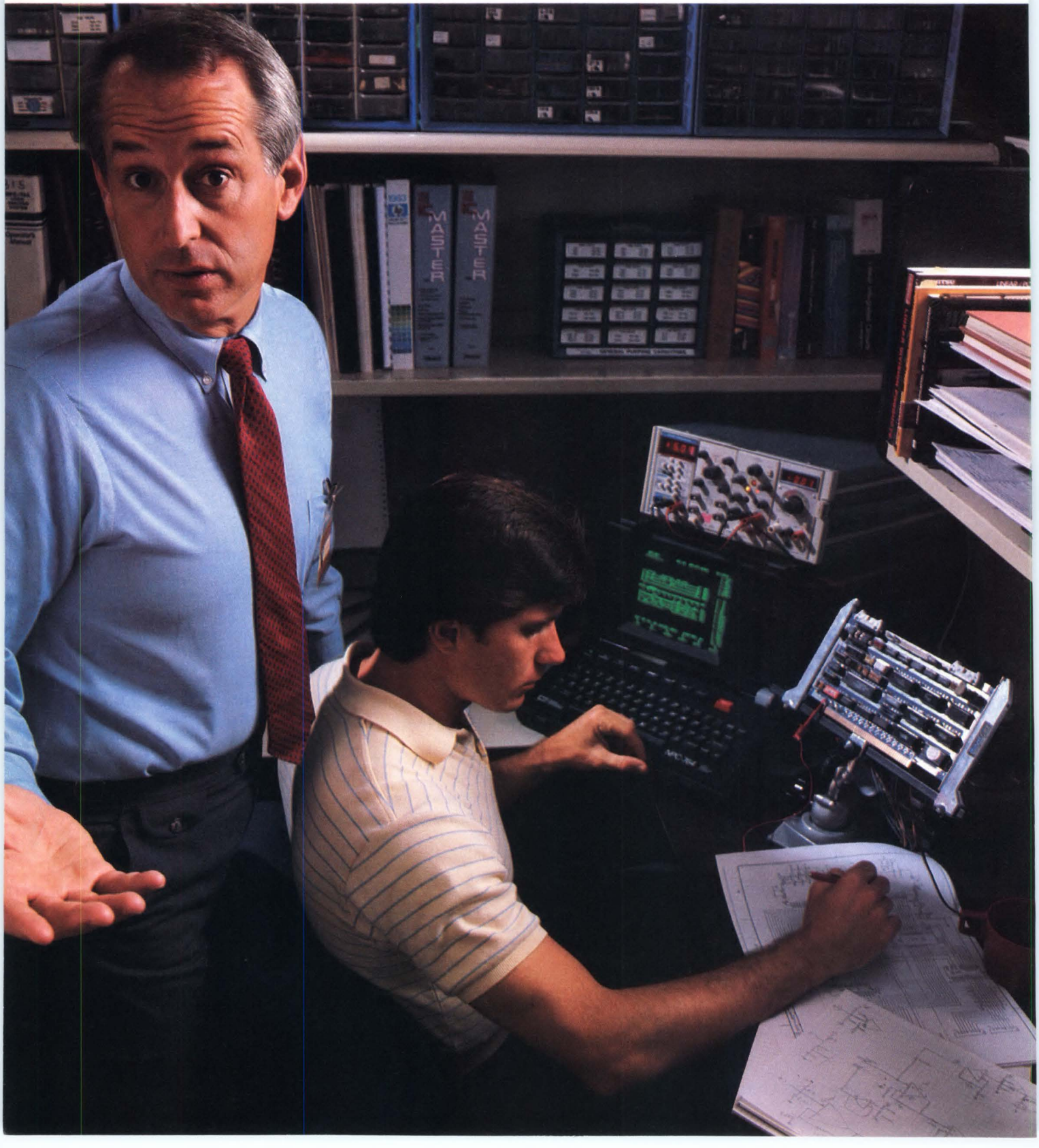
CIRCLE 72 FOR LITERATURE

CIRCLE 73 FOR SALES CONTACT

"Standard-cell but I don't know



ICs sound good, how to design them."

With Texas Instruments, you do.

The TTL design techniques you are thoroughly familiar with are the basis for TI's Standard Cell Integration System. Put simply, designing with TI's standard cells is much like arranging standard TTL logic packages on a printed-wiring board. And you not only have the standard digital functions to design with but also RAM, ROM, PLA, ALU, and linear functions.

Using TI's 3-μm CMOS technology requires only minimum effort on your part to achieve an affordable semicustom chip.

Getting started is easy

You can get your design started by bringing us your hand-drawn schematic or, better yet, a schematic generated by an engineering work station. When you use a work station, TI will supply the cell library and translation software for automatic generation of the TI design-description language. TI's standard-cell library is supported on many industry-standard work stations, including Daisy, Mentor, and Valid, as well as on several PC systems.

We deliver to specs

TI's Standard Cell Integration System, with its systematic step-by-step procedure, gives your design its best assurance of first-pass success. TI commits to deliver chips that perform to your specifications.

After your logic design is complete, simulation, testability analysis, test generation, and test-pattern grading are performed either by you or by TI. And then double-checked by TI.

Next, TI will develop a computer-aided layout of your design which is thoroughly verified for accuracy. Or you can do the chip layout, and TI will supply the specifications you need.

A final simulation becomes, upon your approval, the conformance specification against which prototypes are produced and measured. Prototypes are then shipped to you for in-system evaluation and a "go" decision.

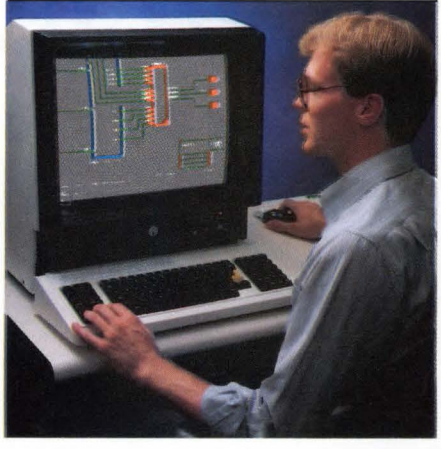
Your Regional Technology Center is nearby to help

All of the IC design resources and expertise of Texas Instruments are available to you through your nearest Regional Technology Center.

Each Center is staffed with a team of standard-cell specialists who will work closely with you to meet your design goals and product schedule.

Your Regional Technology Center can provide quick answers to technical questions as well as provide training in standard-cell design procedures. Here you will receive assistance in design optimization and test development as well as in creating the data-base description of your chip design. Here are engineering work stations for your use and the software tools and the computers needed to complete the logic design and perform simulation and verification.

State-of-the-art design tools speed TI standard-cell design process, help minimize development costs.



TI's standard cells are cost-effective

Texas Instruments offers a full spectrum of logic alternatives—semicustom, including standard cells and gate arrays, advanced bipolar logic, and HCMOS logic. Thus, we at TI are in a unique position to help you weigh all the factors concerning each to determine which alternative is best for your application.

In the case of standard-cell ICs, we'll analyze how you intend to use them and how they will impact your overall system, including performance and cost.

One standard-cell IC can contain the equivalent of hundreds of individually packaged chips. It can dramatically reduce the number of individual parts needed to implement a system. It can significantly cut weight, size, and power consumption while increasing system quality, reliability, and capability.

Then, too, TI standard-cell chips are the lowest cost alternative when produced in mid to high volumes.

Call 1-800-232-3200, Ext. 111

You already know the TTL design rules, so you're well on your way to tailoring logic more precisely to your performance requirements using TI standard-cell technology. For our brochure, pocket selection guide, sample data sheets, and a more detailed description of the design flow, call the telephone number above or circle the Reader Service Card number. Or write Texas Instruments Incorporated, Dept. SRSØ13E1 , P.O. Box 809066, Dallas, Texas 75380-9066.

TEXAS INSTRUMENTS

Creating useful products and services for you.

CIRCLE 23

27-4778

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For six years we've been telling you about the benefits of Programmable Array Logic.

And for six years you've refused to leave asynchronous logic behind.

OK, you win.

Here's the first PAL® circuit for asynchronous logic designs.

The PAL 20RA10.

It has everything you need to put your design on silicon in a hurry. While you chase as many as a dozen TTL parts off your board.

A guaranteed 30ns clock-to-output time.

20 inputs.

10 outputs that can be clocked separately. Each with programmable asynchronous set and reset.

Programmable registers. Each with an independent transparent mode.

Programmable output polarity, so you won't even need an inverter circuit.

The whole thing sits in a sleek 24-pin SKINNYDIP® package.

And the programming is a snap.

Using PALASM,™ our enhanced CAD software, and a standard PAL programmer, you can design and program an asynchronous PAL circuit in just hours.

You can build a prototype in seconds.

And when your design is stable, you can crank out as many PAL circuits as you need. Or you can convert to our mask-programmed HAL® circuits.

So you win.

You get the profound benefits of programmable array logic.

Without leaving your asynchronous logic behind.

Call your Monolithic Memories representative or franchised distributor for our PAL 20RA10 data sheet and an applications packet.

Or write Monolithic Memories, 2175 Mission College Blvd., Mail Stop 9-14, Santa Clara, CA 95054.

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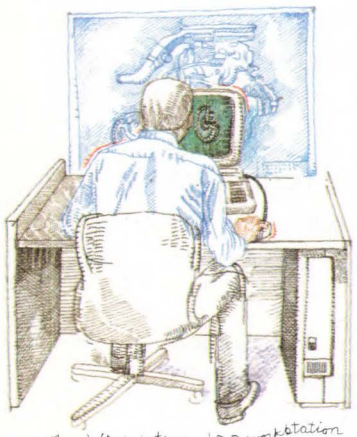
Monolithic Memories MMI

CIRCLE 25

PRESENTING VAXSTATION 100. A COMPREHENSIVE TOOL FOR THE TECHNICAL PROFESSIONAL.

While others have been busy designing computing systems for the technically naive, Digital has been busy designing them for the technically astute.

The welcomed result: the VAXstation 100™ workstation terminal. Connected to a VAX™ host computer by fiber optic cable, VAXstation 100s make full use of the VAX/VMS™ operating system, its layered products and the range of its office automation, networking and applications software.



The VAXstation 100 workstation terminal: graphics processor, monitor, keyboard and mouse.

The workstation terminal's comprehensive design demands that you now reconsider what is possible with computer assistance. From filling polygons to filing reports, it enables you to automate every step of a technical project. Whether in engineering, education, research, or science. Whether your need is text manipulation, numerical calculation, graphics processing – or all three.

To be sure, the VAXstation 100 workstation terminal will be the envy of every technical professional who now sits before a computer dedicated to doing one or two things well at the expense of doing anything else.

THE FRIENDLIEST INTERFACE IN TECHNICAL CIRCLES.

The VAXstation 100 workstation terminal mirrors the latest trends in desktop computing with a complete assortment of end-user niceties. They include all-English commands, helpful pop-up menus, descriptive icons and convenient pointing devices.

Powerful screen management software presents the user with an endless array of overlapping applications windows and the means to move easily between them.

With this friendly interface you can simultaneously display and interrelate any combination of tasks. You can work with equal facility in words, numbers, or pictures. You can work concurrently on parts of different jobs. Or on different parts of the same job.

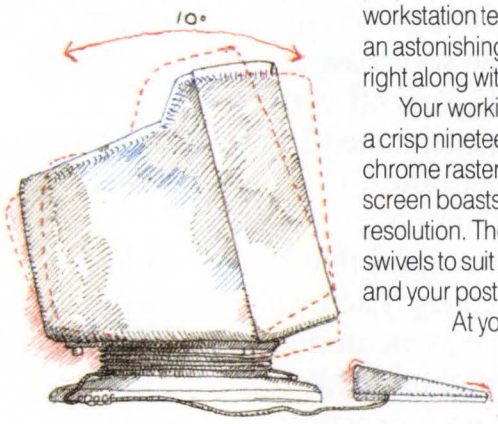
Each application window remains active whether on display or not. Like papers on a desk, windows can be moved at will, allowing you to always maintain a "clean" working environment.

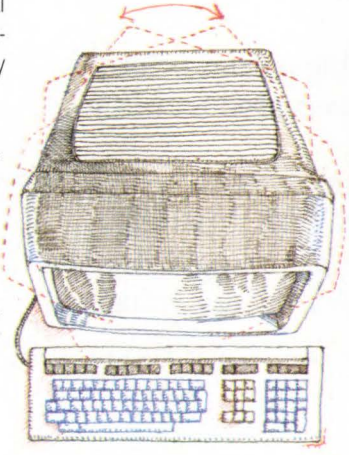
DRAWING ON THE POWER AND VERSATILITY OF VAXSYSTEMS.

The VAXstation 100 workstation terminal can be added to any existing UNIBUS™ VAX computer, from the 11/725 to the 11/785.

This makes VAXstation 100 the most versatile add-on workstation of its kind. It capitalizes on your installed base of software by executing the thousands of programs written by Digital and third parties for the VT100™ terminal series, as well as those applications written for the popular Tektronix 4014™ terminal. And in almost every case, it executes them without modification.

While scaled-down subsystems compromise the performance of micro-based workstations, the VAXstation





100 presents no such barriers. With virtual memory management, your program size is defined by the virtual address space of the VAX computer – some two billion bytes. You also get the complete set of VMS operating system facilities and utilities that have made it a world-famous development environment.

Plus, there's a wide choice of high-level languages important to technical professionals, including industry-standard versions of FORTRAN and Pascal and artificial intelligence languages like VAX LISP.

No matter what you're working on, or how demanding your project is, the VAXstation 100 workstation terminal possesses an astonishing capacity to work right along with you.

Your working surface is a crisp nineteen-inch monochrome raster display. The screen boasts 864 x 1088 pixel resolution. The monitor tilts and swivels to suit your environment and your posture.

At your disposal is both the CORE Graphics Library (based on the CORE graphics standard) and the VAXstation Subroutine Library. Both are callable from a high-level language, and between them you are guaranteed full creative freedom throughout the design and simulation phases.

A powerful MC68000™ microprocessor running at 10MHz has been completely dedicated to screen management and graphics processing. Its accelerator enhances raster operations. This allows you to move large pixel blocks quickly and slide windows across the screen without erasing them. You can even process multiple applications on the screen simultaneously.

Whether you are working on circuit design, seismographic studies, CAD/CAM, or financial

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modeling, whether you are executing familiar technical tasks or dabbling on the edge of engineering exotica, you'll run out of practically everything before you run out of VAX software.

MAINSTREAMING THE TECHNICAL PROFESSIONAL.

VAXstation 100 workstation terminals can be configured with ease. Whether you network them via Ethernet throughout a hierarchy of VAX/VMS systems, or cluster several around a single processor, communications remain streamlined. Each station can access the full range of VAX information management and office automation tools. In this way, the data and programs in general company use can be incorporated into technical projects. Conversely, the highly technical results in a single applications window can be mainstreamed throughout the corporation.

VAXstation 100 workstation terminals let you and your coworkers share and swap information readily. Extrapolate results quickly. Draw conclusions confidently. They rescue the technical professional from tiresome commuting between single-function workstations. They declare war on errors and lost time attributable to manual conversions.

This is the state-of-the-art in distributed computing. VAXstation 100s will not just help project managers increase productivity some day – they will do so immediately.

DIGITAL'S COMMITMENT TO THE WORKSTATION MARKET.

The first add-on workstation terminal for VAX systems, the VAXstation 100 is also the first in a family of new workstation products from Digital. Each reflects Digital's dedication to providing integrated computing solutions.

The workstation terminal provides a truly comprehensive and cost-effective way to coordinate the work of engineers, scientists and researchers. It is unmatched in its ability to accommodate the fluid and unpredictable nature of highly technical projects. And it does so elegantly, whether in response to a momentous change in direction or to a momentary change of heart.

Each VAXstation 100 system comes backed by full Digital service and support from coast to coast and in 44 foreign countries. Each carries with it Digital's enviably high reputation for quality and engineering excellence.

BEST ENGINEERED MEANS ENGINEERED TO A PLAN.

The VAXstation 100 workstation terminal, like every Digital hardware and software product, is engineered to conform to an overall product plan. This means Digital systems work together easily and expand economically. Only Digital provides you with a single, integrated computing strategy direct from desktop to data center.

Configured with graphics processor, monitor, keyboard, mouse, fiber optic cable and interface, the VAXstation 100 workstation terminal can be added onto an existing VAX/VMS system inexpensively.

For the new VAXstation 100 product brochure, call 1-800-DIGITAL, extension 250. Or write: Digital Equipment Corporation, Media Response Manager, 200 Baker Avenue, West Concord, MA 01742.

THE BEST ENGINEERED COMPUTERS IN THE WORLD.

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BOB, CAROL, TED & ALICE

How Four Innovative Design Engineers Found Happiness Using The New DASH-1™ Schematic Design System.

BOB: "DASH-1 keeps me under budget and ahead of schedule..."

"DASH-1 has freed my designers from the drudgery of manual schematic design and documentation. Now, we can knock out complex designs in a fraction of the time it used to take. Using the huge DASH-1 parts library (on disk) we can instantly call up any symbols we need — all with pinouts and pin functions. Also, our amazing DASH-1's automatically generate Net Lists, Lists of Materials, Design Check Reports and other critical documents. I'm a hero in my company now, with productivity at an all-time high."

CAROL: "DASH-1 helped save our CAD Systems..."

"My company has a big investment in large CAD systems. But for a long time I noticed our engineers were frustrated. They'd send in schematic sketches only to get back drawings and documents that were completely different. The poor engineers would spend hours checking, changing and red-lining. DASH-1's family of CAD translators, to front-end all of our large systems, has changed all this. And back annotation is easy. DASH-1 has provided our engineers easy access to those previously difficult-to-use and inaccessible CAD tools."

TED: "Imagine! Simulation right at my desk..."

"I'm even more sold on my DASH-1 with its new simulator. After I complete my schematic, I have a closely coupled logic and fault simulator that I can run at my desk. I can analyze my designs much faster — and put them into production without delay. FutureNet calls it the DASH-1 CADAT.™ I call it a miracle because I can handle designs as large as 10,000 gates right at my desk, and up to 100,000 gates using a FutureNet CAD translator. Thanks to DASH-1, simulating is stimulating!"

ALICE: "DASH-1 keeps growing — as we do..."

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CIRCLE 28

NEWSFRONT

Fine-line CMOS process will soon be trimming feature sizes to 1 μm

A CMOS technique ultimately aimed at 1-μm features uses retrograde p-well structures to give 2-μm circuits speed and low power.

An advanced CMOS process, now successfully producing circuits with 2-μm feature sizes, will soon cut that figure in half. The savings in chip area, power, and speed will permit the process's developer, TRW Inc.'s LSI Products Division (La Jolla, Calif.), to build chips like 16-bit parallel multipliers that operate at less than 50 ns and consume only a few hundred milliwatts.

Though TRW originally wanted to go directly with 1-μm features and extremely tight metal-to-metal pitches—4 μm with 1-μm spaces—it has backed off slightly, opting for 2-μm features until it wrings the quirks out of the process—by the end of the year.

The structure is all

To bring such small design rules into the realm of possibility, the company developed a retrograde p-well transistor structure—the key to defining the n-channel transistors. That structure's doping profile calls for a lower boron density at the surface, increasing in density deeper in the material.

The dopant concentrations represent a tradeoff between device switching speed and latch-up immunity. The transistors are so fast, however, that the circuit speed is limited by interconnection capacitances and not by gate delays.

Start with deep implants

The retrograde structure starts with a deep boron implant that defines the region for the n-channel transistor. The boron region within the p well also serves as a field-isolation guard band, preventing interdevice leakage.

The process reduces the current gain of parasitic vertical npn bipolar transistors by a factor of 10 as compared with conventional p-well processes. Consequently, circuits built with the retrograde p well have high latch-up immunity.

This process replaces more conventional forms of device isolation such as guard rings, making possible very high packing densities. For example, a 16-bit CMOS multipliers has been fabricated with 1-μm design rules; its area—just 180 mils^2—is about 30% smaller than the bipolar counterpart, also built with a 1-μm process.

Second implant

After the boron has been deeply implanted, the polysilicon gate structures are formed, followed by a second boron implant (self-aligned to the gate) that creates the source and drain regions of the n-channel devices. A similar arsenic implant defines the p-channel transistor's source and drain regions.

Next, the regions are annealed and an oxide layer deposited on top to insulate the previously deposited polysilicon from the next metal interconnection layer. Contact windows are opened in the oxide to permit access to the n, p, and polysilicon areas, and then platinum, titanium-tungsten, and aluminum are sequentially deposited.

The platinum and titanium-tungsten layers form silicided barriers in the contact regions, which prevent aluminum spikes from passing through those shallow regions and contacting the substrate, shorting the drain or source. And, to house the chips in plastic packages, TRW uses a silicon nitride passivation coating that is

Dave Bursky

deposited via low-pressure chemical vapor desposition.

Single-level metal circuits with 2-μm features are now moving into production, and 1-μm metal devices should be released as samples later this year. Additional process development, though, is already under way to add a second layer of metal interconnections.

Designers are experimenting with forms of low-temperature reflow glass to act as the planarizing intermediate insulating material between metal layers. Although the more complex double-level metal process might result in losses in yield, it will produce a more compact layout that will more than compensate for the loss in yield since almost twice as many chips will fit on a wafer. Samples of the double-level metal circuits are slated to appear early next year.

Internal floating-point processor further boosts RISC machine speed

With a floating-point accelerator built directly into its execution path, a reduced-instruction-set computer pushes its streamlined operation ever upward in speed, performing floating-point arithmetic faster than a VAX.

Designated the 32 CX by designers at Ridge Computers Inc. (Santa Clara, Calif.), the RISC microcomputer eliminates the three or four additional machine clock cycles ordinarily required by floating-point processors for addressing and accessing memory. With a 125-ns clock, the machine saves 375 or 500 ns, a significant amount for computationally intensive tasks like solids modeling, interactive IC design, logic simulation, and design rule checks.

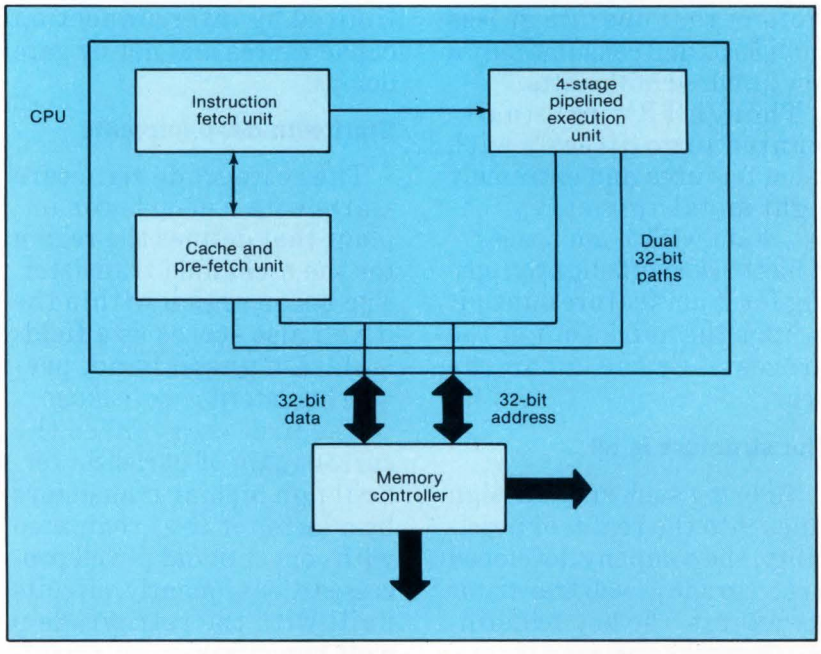
With the floating-point processor built directly into its execution path, the CPU does not care whether the instruction being executed is an integer addition, comparison, or a double-precision floating-point operation.

A full 64-bit floating-point addition can be done in 0.750 μs on the 32CX, compared with 1.4 μs on a VAX 11/780, which uses an add-on floating-point accelerator. A multiplication—the most time-consuming operation since it comprises successive addition cycles—can be done in 3.5 μs vs 4.25 μs for the VAX, and a division takes 7.375 μs compared with 8.0 μs.

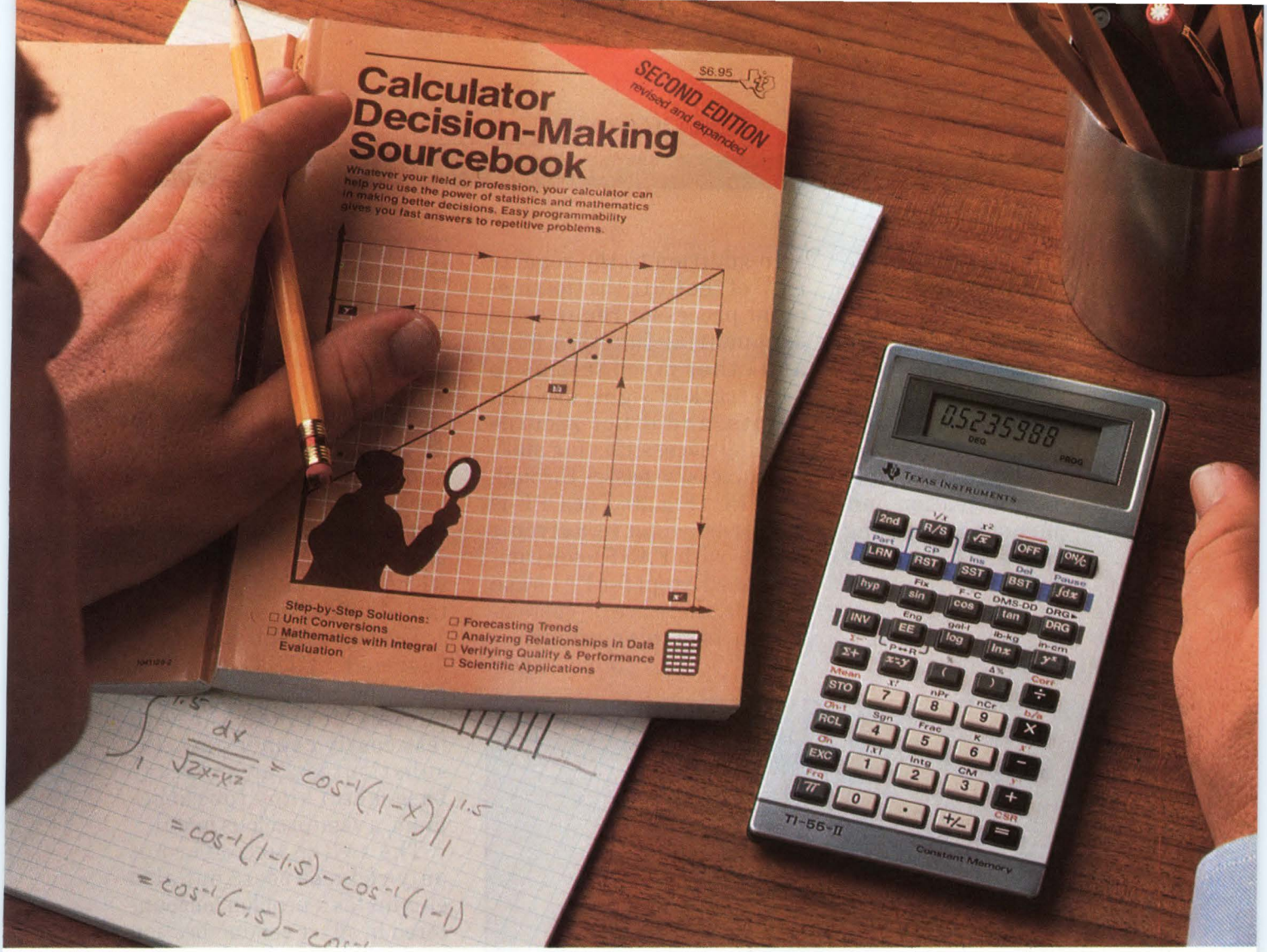
Calculating RISCs

Unlike conventional microcomputers with generalized instruction sets, RISC machines (using an architecture developed at the University of California at Berkeley) spend absolutely no time interpreting their limited instructions.

The Ridge 32CX supplements that with a "pipelined" architecture, meaning that it does no work finding instructions; a separate mechanism rapidly loads instructions and



1. In the CPU of Ridge Computers' reduced-instruction-set computer, memory access and instruction loads are accomplished simultaneously with execution.



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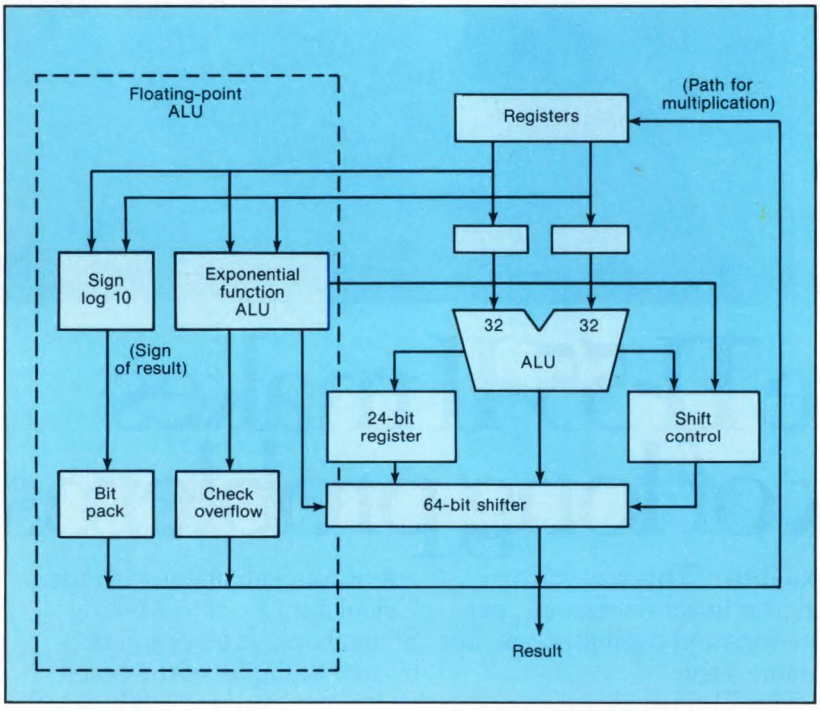
operands. With virtually no memory-addressing overhead needed to pull instructions into the CPU, the microcomputer attains great speeds.

For floating-point operations, all instructions are indexed in advance and pipelined into the execution unit (Fig. 1); memory addressing and accessing take place simultaneously. In other words, the loading and execution functions of the CPU are performed at once.

In addition to the regular ALU of the CPU, the floating-point processor requires an exponential-function ALU and other mechanisms to keep track of signs, decimal points, and other record-keeping necessities for making successive passes through the CPU (Fig. 2). The CPU is constructed on two circuit boards with FAST logic components. Except for PALs and PROMs, there are no customized parts in this machine.

Stephan Ohr



2. The 32CX includes a floating-point processor within the execution path of its instruction execution unit. With most memory fetch cycles eliminated for floating-point operations, the machine's performance proves superior to that of a VAX 11/780.

Base metals replace precious ores to cut resistor network cost

A thick-film process opts for base metals in place of the precious and semiprecious ores now used in resistor networks, sharply slashing cost and improving aging characteristics without diminishing important standards.

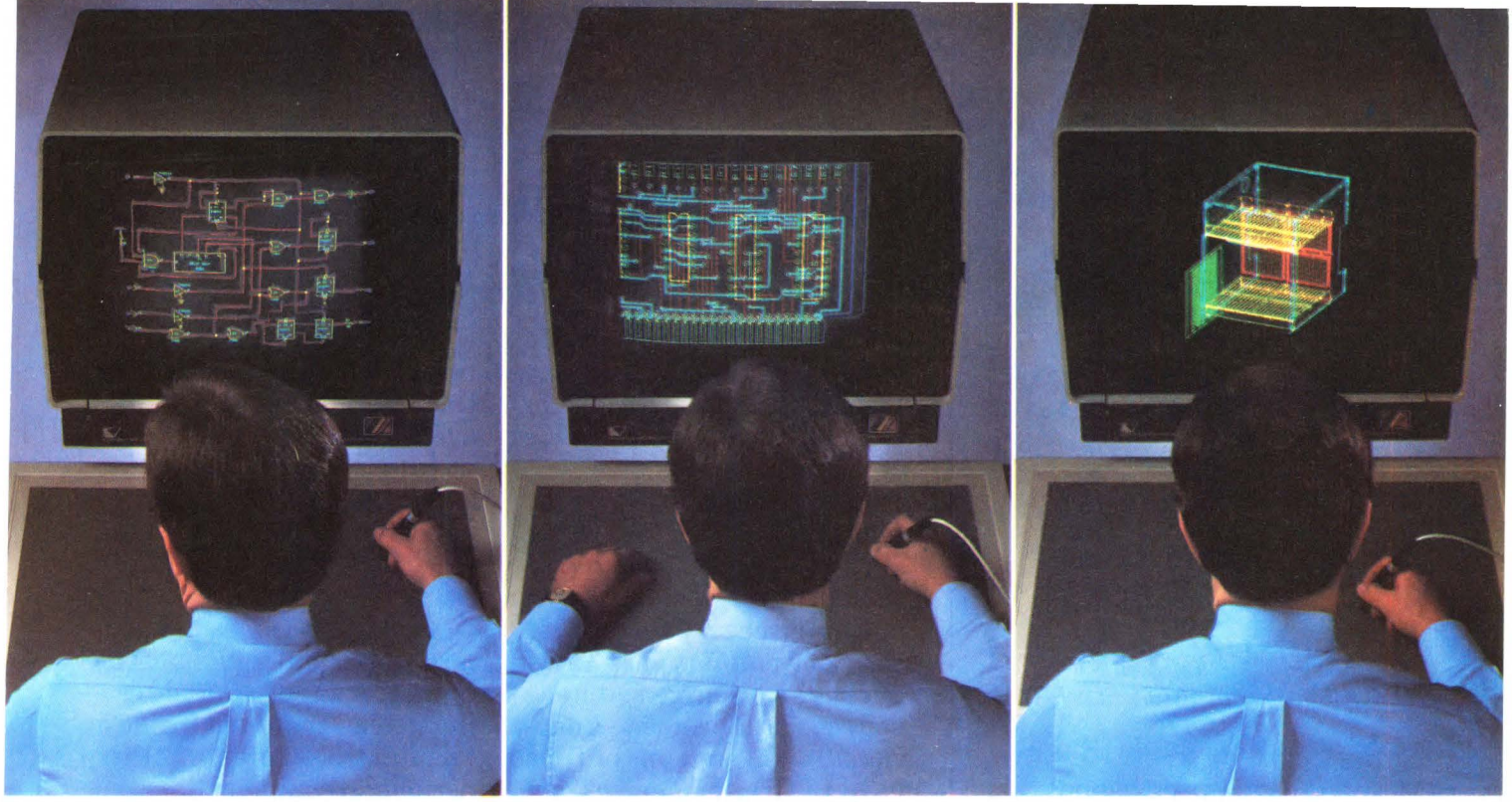
The new resistor technique, devised by CTS Corp. (Elkhart, Ind.), replaces the common silver conductor with less costly copper and also substitutes a proprietary base metal alloy for ruthenium, a semiprecious metal.

The switch to copper not only reduces costs but also eliminates a problem encountered in silver conductors: ion migration. Silver is more susceptible to ion movement when moisture is present.

Although other ruthenium substitutes have been rejected because of their poor noise characteristics, the proprietary alloy compares favorably. The noise constants of the base material range from −3 dB for the lowest noise to 20 dB for components with looser specifications.

The resistors can be used over a wide resistance range, from 10 Ω/square to 1 MΩ/square. The thermal coefficient of resistance remains within ±100 ppm/°C.

The metal also holds up well under the repeated firings frequently used when manufacturing resistors. After the component is assembled, fired, and laser-



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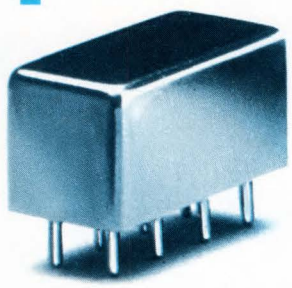

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CIRCLE 39

trimmed, it will hold to within ±0.2% of its trimmed value through subsequent heat treatments. The thick-film resistors have a typical value of ±0.5%.

A drawback to the technique is that both the copper and resistive element must be fired in nitrogen ovens, which are more costly to operate than conventional ones. However, gas or infrared heat sources can be used. Additionally, the amount of time used to fire the devices can vary widely without adversely affecting the materials or the stability of the parts.

Terry Costlow

Chip capacitors and leaf springs yield compact connector

Using chip capacitors in a filtered connector instead of the traditional tubular components not only lowers the EMI/RFI emissions of the connector but also bolsters its performance and durability while cutting package size. To those benefits, add another: The capacitor is held in place with a leaf spring, considerably lowering—if not actually eliminating— the piezoelectric interference encountered with the more common contact method of soldering.

By going with chip capacitors instead of the tubular, axial-leaded components, Allied Corp.'s Amphenol Products (Oak Brook, Ill.) racked up several benefits. For one, the capacitor chips are significantly smaller than the regular components, making the filtered connector package no larger than the one for unfiltered devices. Tubular capacitors, in contrast, are usually curved around the pins, meaning that their packages must be much wider. Size becomes particularly important in light of the connector's typical final resting place—mounted inside a terminal, a printer, or other peripheral equipment.

Springing to life

The chip capacitors, furthermore, are well suited to leaf-spring mounting, a technique that presses the chip against both the housing shell for grounding and the connector pins while it lends a large degree of stress isolation. In the traditional approach, solder holds the capacitor to the connector pin; unfortunately, vibrations caused by, say, a cooling fan, can stress the joint, creating piezoelectric interference.

In contrast, leaf springs virtually eradicate the risk that a device designed to filter noise will instead become a source. Not only that, they strengthen durability, since the stress isolation absorbs some of the shock when the part is dropped or jarred. To ensure a long and secure life for the connector-pin contact, the capacitors are fitted into the recesses of the housing, reducing the chance that the connection might break.

With filtered connectors mounted inside the various peripheral cabinets, EMI/

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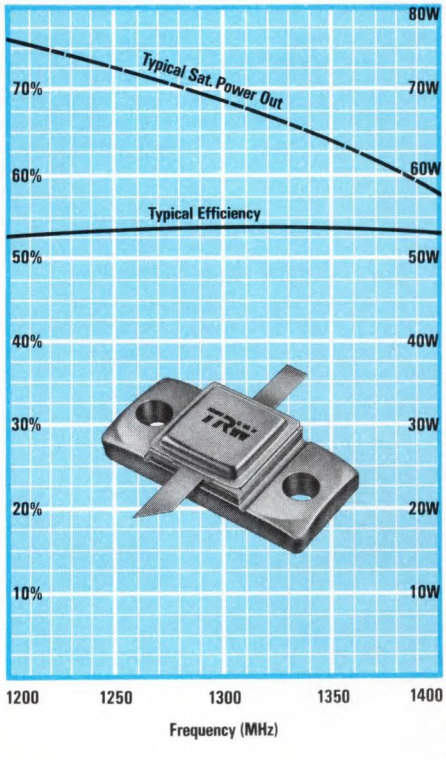

The MRA1214 is only the first of a whole new generation of RF Devices we'll be announcing during the next year. Keep your eye on TRW RF Devices.

For information and data sheets on the MRA1214-55H, contact your local TRW/ECG Field Sales Office or RF Devices Division, TRW Electronics Group, 14520 Aviation Blvd., Lawndale, California 90260, phone 213.536.0888.

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CIRCLE 32

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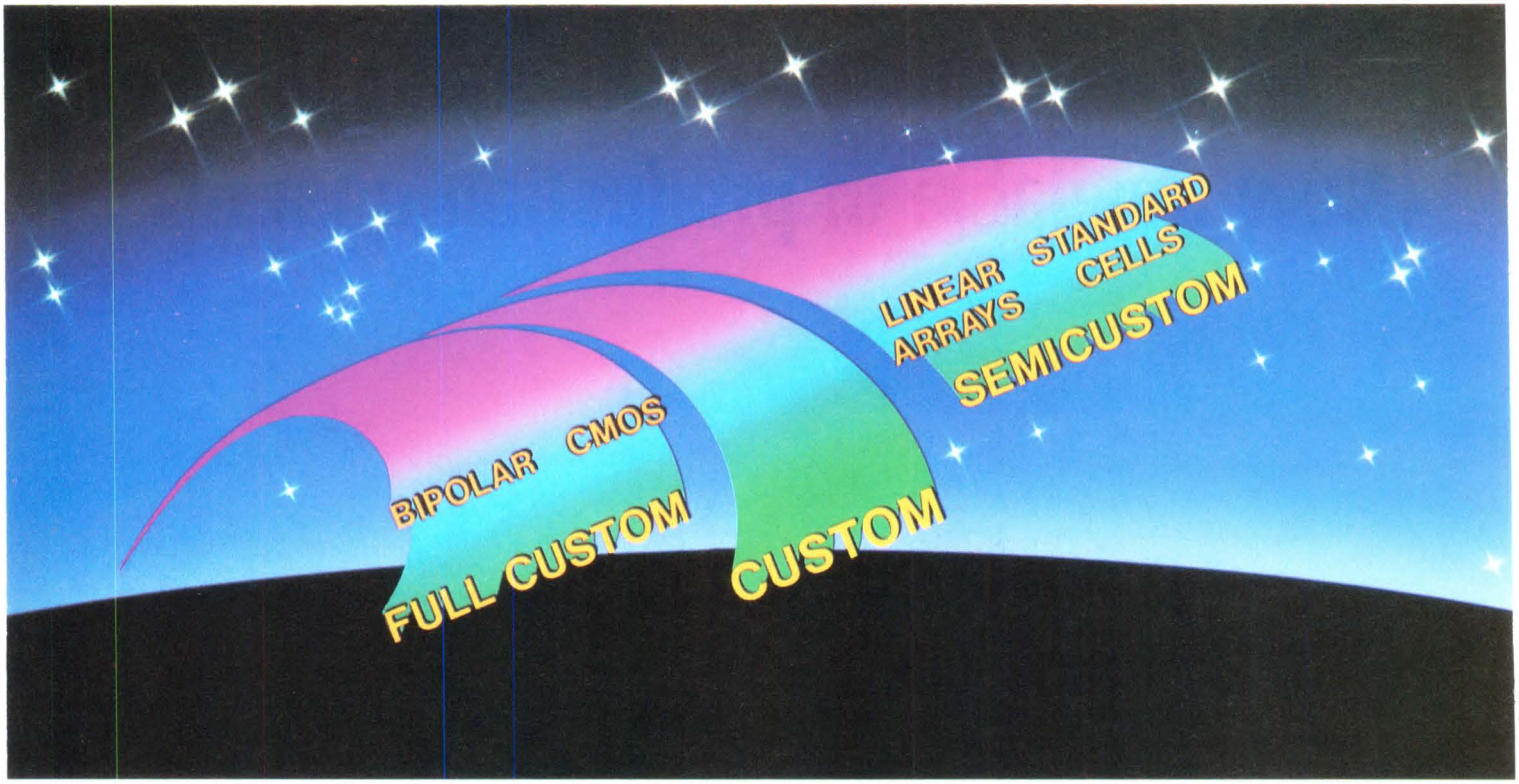

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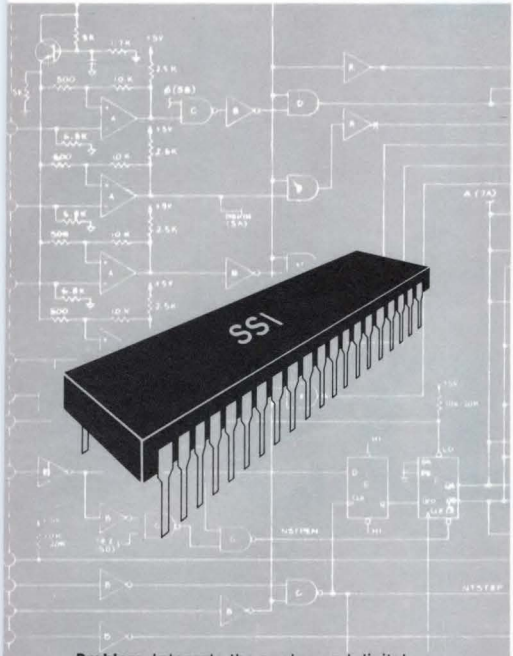

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CIRCLE 33

NEWSFRONT

RFI emissions fall to lower levels than could be possible with shielding. Filtering noise before it leaves the peripheral's enclosure removes any concern that noise will be transferred from one peripheral to another. Beyond that, it eliminates the need for shielding the connector and the full cable.

The capacitance values in the filtered connector range from 100 pF to 47,000 pF, depending on the signal level of the peripheral. However, variations in system parts and applications make it extremely difficult to quantify the decrease in noise emissions afforded by the filtered connector. *Terry Costlow*

MESFET technique shrinks power needs of GaAs chips

A MESFET process yields gallium arsenide ICs with power consumption below 1 mW per gate, even on dense circuits. Two high-speed devices, a divider and a ring oscillator, have demonstrated the technique's success.

At a 1-GHz clock frequency, the divide-by-4 chip dissipates only 0.172 mW per gate, or 4.79 mW for the entire circuit (see the table). The ring oscillator operates as fast as 30 ps, with power consumption falling within the 1-mW/gate range.

Relative speed vs supply voltage and power dissipation

Voltage (V)	Power (mW)	Frequency (GHz)
0.84	3.47	0.5
1.00	4.79	1.0
1.83	11.9	1.5
6.6	59.4	2.0

The fabrication technique from Honeywell Inc.'s Physical Sciences Center (Bloomington, Minn.), makes use of normally off, self-aligned gate MESFETs. Refractory metal-silicide gates are formed by combining a dielectric-assisted lift-off process for the first two metal layers. This permits addition of a third interconnection level needed in complex ICs. The metal levels have a 4-μm pitch and nonoverlapping vias between layers.

Across the entire 3-in. wafer, threshold voltage typically varies from 50 to 70 mV, with variations as low as 10 mV over smaller areas.

The divider chip makes especially good use of gallium arsenide's speed: It operates as high as 2.5 GHz. The equivalent gate delay at the maximum clock frequency is about 100 ps. *Terry Costlow*

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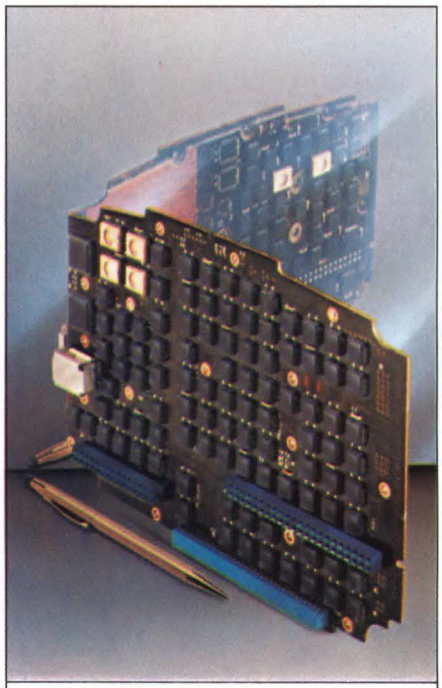
Texas make

As Collins Avionics and Singer-Kearfott developed JTIDS*, the new communications system for the F-15 fighter, Texas Instruments helped solve a severe circuitry packaging problem.

The new system utilizes the most advanced chip packaging technology, the

*Joint Tactical Information Distribution System



Successful application of high-density packaging was achieved in the PC boards of the F-15's new communications equipment. TI's clad metal system solved thermal expansion mismatch. This mirror-reflection photo shows how ICs were mounted on both sides of the PC boards.

leadless chip carrier. Design objectives called for 191 components to be surface mounted on both sides of a 6″ × 8.5″ printed circuit (PC) board—and to dissipate up to 40 watts of power.

But, during thermal cycling tests, the difference in the thermal coefficient of expansion (TCE) between the ceramic chip carriers and the conventional PC

◀ **Improved reliability** in the F-15's new communications system (JTIDS) is achieved with TI's copper-clad Invar used to prevent solder joint breakage on densely populated PC boards. TI teamed up with Collins Avionics and Singer-Kearfott to meet the demanding packaging requirements of the fighter's receiver/transmitter.

Instruments and Collins Avionics dense circuit reliability soar.

board caused the solder joints attaching the components to the board to break.

TI's solution: A composite metal core of low-TCE Invar that is clad on both sides with copper. Thin, polyimide-glass, multilayer boards were bonded to each side of the metal, to provide the circuitry function.

With a TCE match between the board and the chip carriers, the PC boards easily passed the exacting thermal cycling tests.

And the metal core in the board dramatically improved thermal conductivity and overall rigidity.

Solves thermal mismatch problems

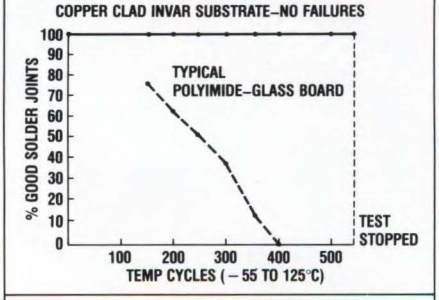
As Collins Avionics discovered, the advantage of using chip carriers to achieve high-density, high-performance circuitry also imposes stringent demands for increased thermal management, structural integrity, as well as TCE compatibility—demands met by Texas Instruments copper-clad Invar.

By combining TCE compatibility with high lateral thermal conductivity. And mechanical rigidity.

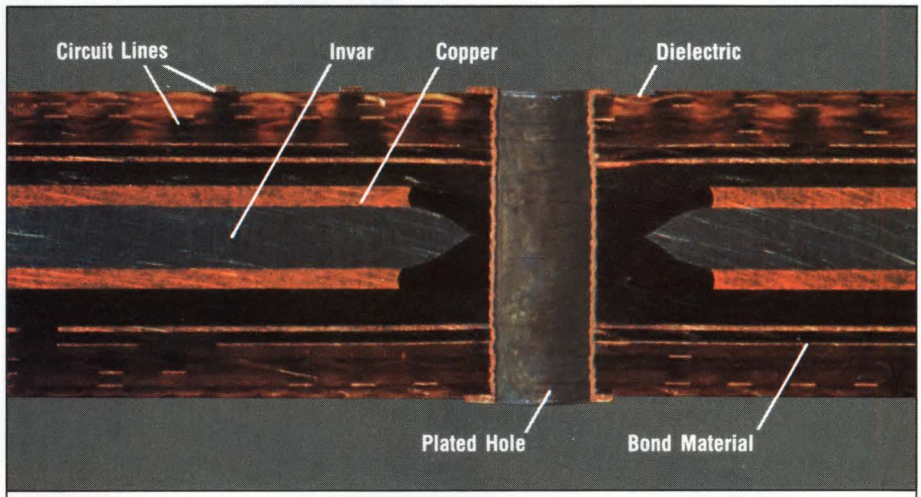
All at lower cost than alternate approaches. ■

The solution is a trilayer metal.

TI's process involves roll bonding copper foil to Invar—a 36% nickel/64% iron



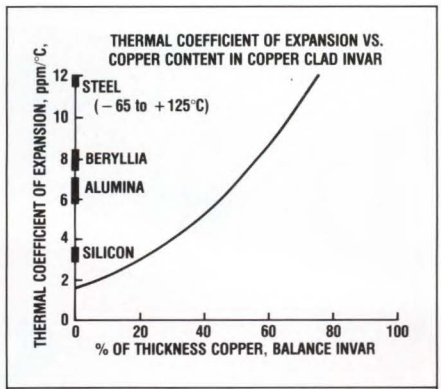
After 540 thermal cycles from −55° to 125°C failed to break chip carrier solder joints, Collins Avionics halted tests of PC board used in F-15 communications system. Reliability goals had been surpassed by a wide margin.



Effective thermal management is achieved with a copper-clad Invar core that acts as a support for circuitry in the PC board. Heat dissipation characteristics of the copper are excellent, and the Invar contributes rigidity and strength.

alloy. The bonding to each side of the Invar is accomplished by the same process used to make thermostat metal and coins. No adhesives or brazing alloys are required to achieve a permanent bond.

By varying the ratios of the high thermal conductivity copper to the ultra-low TCE Invar, the TCE of the clad metal can be tailored to match that of silicon, alumina, or beryllia.



Matching the TCE of the metal core of a PC board to chip carrier ceramic is accomplished by bonding the correct ratio of copper to Invar.

This material is available in thicknesses from 5 to 62 mils (.13 to 1.57 mm). You can get it in widths up to 24 inches (610 mm).

Copper-clad Invar is being developed for many other applications: From ground and power planes in multilayer boards, to heat sinks and covers for multichip ceramic modules, and more.

A clad remedy to packaging challenges

TI's innovative clad metal solutions can solve your circuitry packaging problems—with a variety of materials.

You can get copper-cored electron tube materials; nickel-clad stainless steel transistor can materials; copper-clad stainless steel lead frame materials; precious metal, aluminum, and solder selective cladding on base metals for lead frame and connector applications; copper-clad steel, aluminum, and Alloy 42 wire products; and high-speed precision stamping and assembly.

In fact, TI—the world's leading clad metals manufacturer—can help you develop a clad metal solution to many electronic materials problems.

For information, contact Texas Instruments Incorporated, Dept. MMJ9Ø3E1 , P.O. Box 401560, Dallas, TX 75240. 1-800-341-5202.

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CONFERENCE PREVIEW

Fiber-optic radio link makes waves at connector conference

Ways of reducing EMI, measuring shielding effectiveness, and designing high-density connectors for VLSI computers share the bill.

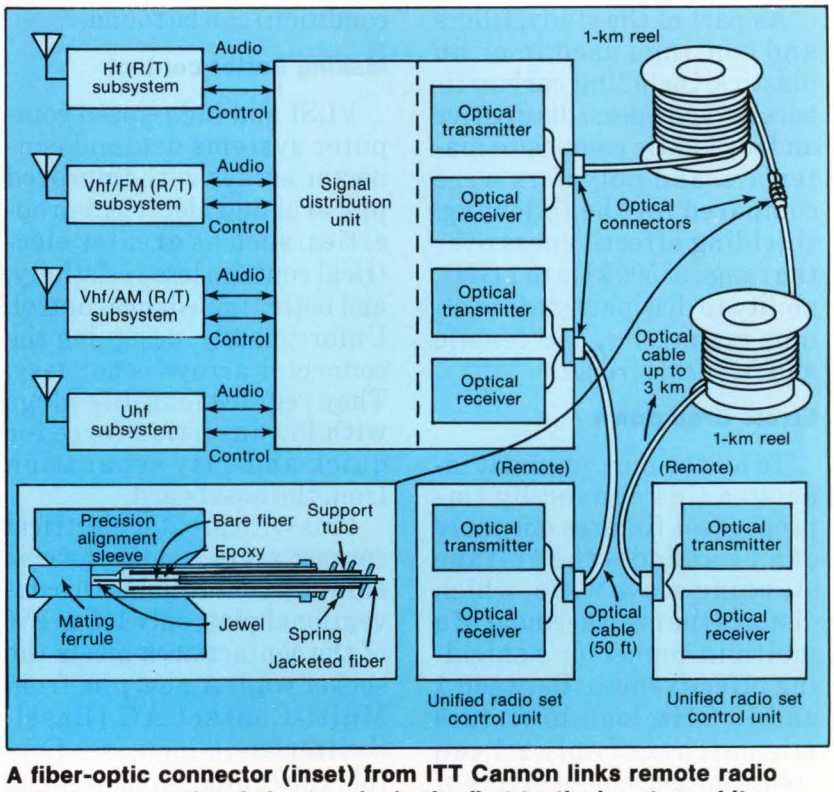
How to apply relatively new fiber-optic techniques to conventional rf systems in military settings will be the main topic at the 17th Annual Connectors and Interconnection Technology Symposium, held in Anaheim, Calif., Sept. 19–21. Several companies have also devised better ways to reduce EMI in hard-wired systems and to measure shielding effectiveness. Finally, at the low (dc) frequencies, high-density connectors are improving the performance of VLSI systems.

Military communications systems have begun to transmit over fiber-optic cables. Optical transmission reduces the risk of eavesdropping. Furthermore, optical cables cost less and are less bulky than metallic cables, in addition to having a higher bandwidth.

In all fiber-optic systems, alignments must be precise. A connector for linking an rf system to optical fibers must also be rugged enough for army life. A fiber-optic connector, developed by ITT Cannon Electric's Military Aerospace Division (Santa Ana, Calif.), meets the optical performance requirements of military specifications 1344A, 5015, and 202E for shock, vibration, mating durability, submersion and corrosion.

The connector itself aligns a 50-μm fiber cable by means of a jewel ferrule-and-guide sleeve (see figure). Its average coupling loss is 1.65 dB over $-40°$ to $+68°$C in the infrared spectrum.

The connector is being used to link a Magnavox AN/GRC-206 hf/vhf/uhf radio set to forward observer units up to several kilometers away. Magnavox Government and



A fiber-optic connector (inset) from ITT Cannon links remote radio units to conventional rf networks in the first tactical system of its kind. The key to the connector's excellent optical performance—an average insertion loss of 1.65 dB—and its mechanical reliability is a precision jewel ferrule-and-guide sleeve.

Vincent Biancomano

CONFERENCE PREVIEW

Industrial Electronics Co. (Fort Wayne, Ind.) has extensively analyzed the interaction of the connector and radio, as well as the possibility of system loss, in fiber-optic links of this kind.

Get the static out

Static discharge and EMI continue to disrupt systems that have plastic-based connectors. Through experiments, LNP Corp. (Malvern, Pa.) can relate the electrostatic voltages produced on a plastic surface to relative humidity and to the source of the static electricity. The company's results have helped determine which materials are best for a given application.

As part of the study, fillers and coatings used in or on plastics, including carbon fibers and powders, dissipative and antistatic composite materials, and polymers were compared for the following: shielding effectiveness over the range of 500 kHz to 1 GHz, ability to dissipate static, volume resistivity, and tensile and flexural strength.

Errors drop down

To all the measurement inaccuracies caused by improper test fixtures one more can be added—the voltage standing-wave ratio, which distorts the measurement of a multipin connector's shielding effectiveness. Between 1 and 10 GHz, load-to-fixture mismatches of only 2:1 can create measurement errors of about ±3 dB. Often the mismatches are much greater, as are the resulting measurement errors.

A noted expert in making accurate mode-stirred measurements on connectors, Allied/Amphenol Products' Bendix Connector Operations (Sidney, N.Y.) suggests revisions that would tighten the standard measurement procedures for systems, basing the suggestions on a coaxial transmission line. These revisions will benefit triaxial, radiation, and mode-stirred test schemes.

Among the experimental changes proposed is to substitute a short circuit for the matched load termination in a "nominally matched" test fixture, so that the worst-case figure (which varies a known 6 dB from a perfectly matched condition) can be found.

Making better contact

VLSI and high-speed computer systems demand connector arrays with improved physical and electrical properties, such as greater electrical contact, less resistivity, and better impedance control. Unfortunately, designing the connector arrays is not easy: They require long-life plugs with low insertion force for quick and easy separation from the host board.

Pins with greater electrical contact areas reduce the risk of faulty connections. On conventional pins, only 1% to 2% of the contact area meets the socket wall. A new pin, from Multi-Contact AG (Basel, Switzerland), increases fivefold the contact area between pin and socket by welding the pin onto a springlike metal band. The flexible band also minimizes insertion stress.

A flexible pin may well solve the problem of out-of-tolerance hole sizes on pc boards. Developed by Bihler of America Inc. (North Branch, N.J.), a one- to four-piece welded spring made of phosphor-bronze or beryllium-copper asserts a uniform force on the walls of the hole. The spring permits better electrical contact and allows the pin to work in a hole with a larger than nominal diameter.

Massing for the attack

In addition to the general developments in pin technology, high-density connectors are meeting the ever-growing need for mass termination. One such connector, introduced by Advanced Circuit Technology Inc. (Nashua, N.H.), has 40 contacts per inch. Called SNAP for sustained necessary applied pressure, the six-part clamp-type connector has a zero insertion force.

Better interconnecting designs for leaded chip carriers are also coming. A pin array, from ITT Cannon's Commercial Interconnect Division (Fountain Valley, Calif.), uses an externally activated contact technique to mate up to 1000 contacts to the carrier. Its pins have diameters of 16 to 20 mils and are spaced 75 mils apart. Its greatest advantages are its controlled impedance characteristics (a standing-wave ratio of less than 1.2 at 3 GHz), zero insertion force, automatic alignment, and lifetime of 10,000 cycles.□

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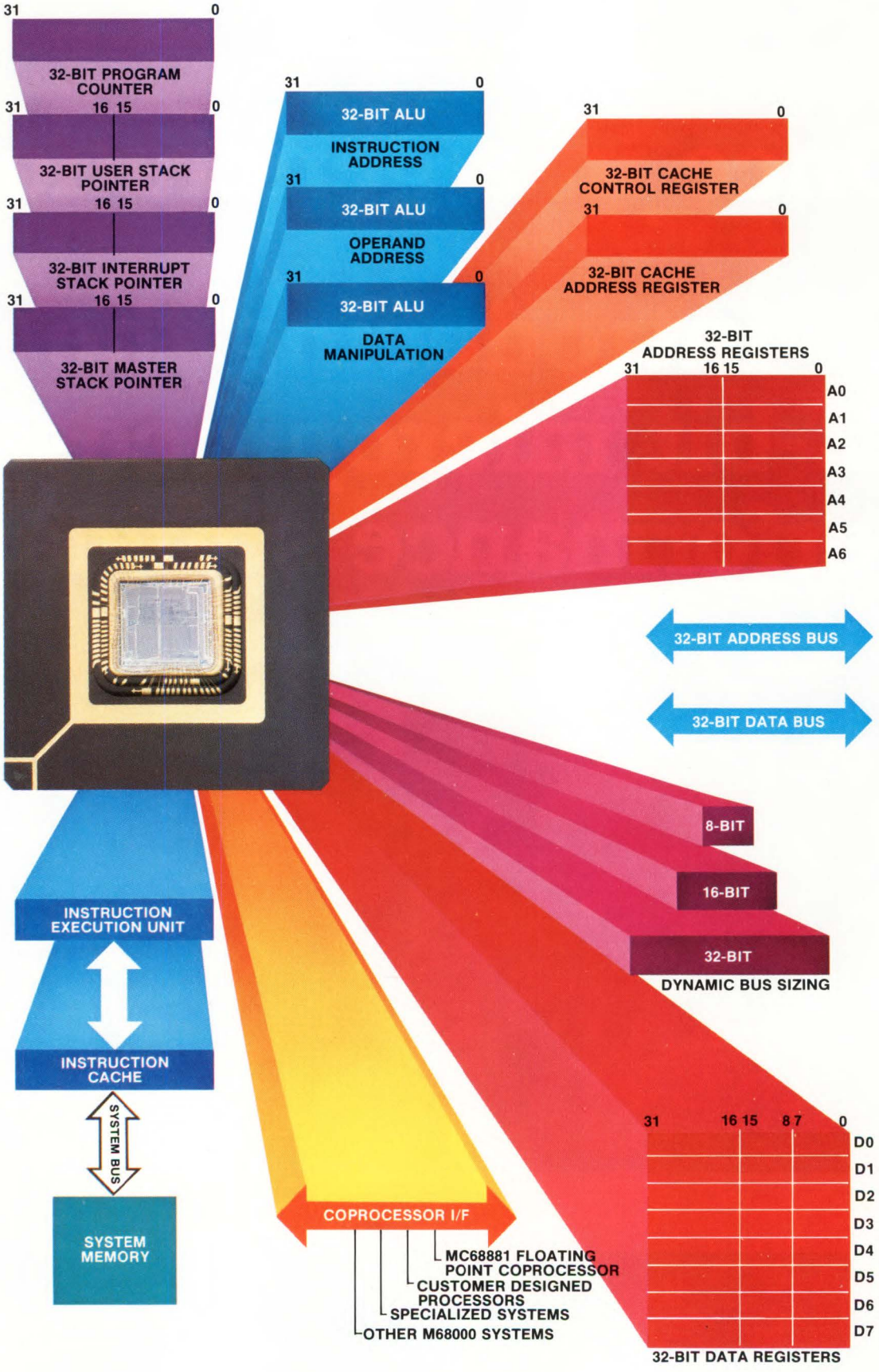

new system with the MC68020: microprocessor.

The new performance standard.

Motorola's new MC68020 performs at speeds typically 400% of the established standard of comparison, the MC68000. It's up to ten times faster in dedicated 32-bit applications.

No other 32-bit MPU makes this extensive a leap in performance improvement. At 16.67 MHz the MC68020 typically runs at 2.5 MIPS for integer processing. MIPS rates several times typical are achievable in dedicated 32-bit applications.

The advanced two-micron HCMOS manufacturing technology which allows this unparalleled performance also results in very low power dissipation. In fact, the MC68020 consumes less power in a system than the original MC68000.

The MC68020 creates opportunities you've never had before--opportunities to unleash the full potential in your 32-bit MPU-based systems because it sets the standard for 32-bit microprocessors. And, because it's the first complete 32-bit microprocessor available, more than just a 16-bit design on a data bus stretched to 32 bits. A detailed look at the architecture reveals this totality.

A fully compatible M68000 Family member.

Yes, the MC68020 has features new to the M68000 Family to maximize its true 32-bit capabilities.

Yes, it's an all new design built with advanced, highly manufacturable HCMOS technology.

And, yes, it's a fully-compatible member of the M68000 Family of MPUs and peripherals. All user object code written for previous M68000 Family MPUs executes without revision. In fact, MC68020 enhancements allow it to run more than three times faster.

Family compatibility is further enhanced by dynamic bus sizing, which supports the use of 8-, 16- and 32-bit ports in 68020-based systems. In fact, the MC68020 can be used in existing 8- or 16-bit systems.

New features enhance 32-bit architecture.

The MC68020 design is new, however its architecture is based on the proven M68000 Family 32-bit register set. And, the MC68020 is highly enhanced.

On-board instruction cache speeds operation and provides increased multiprocessing efficiency. The coprocessor interface allows direct expansion of the architecture off the MC68020 chip to coprocessors or customer-specified processing systems.

New addressing modes, new instructions and a 32-bit barrel shifter support new capabilities. Operating system efficiency is improved with a 32-bit program counter.

These enhancements and more optimize the MC68020 for 32-bit operations.

Design support brings projects together, fast.

Making the most of your new 32-bit design opportunities with the MC68020 is simple and effective with the backing of powerful new hardware and software support from Motorola.

The Benchmark 20™ evaluation system has been developed as a maximum environment testbed for resultant software. For initial software development, cross-support packages under both the UNIX™-derived System V/68™ and the real-time VERSAdos™ operating systems run on standard Motorola VME/10™ and EXORmacs® hosts.

You'll find MC68020 designs a breeze with Motorola's advanced development tools--real time emulation and bus-state analysis with the HDS400 development system.

Move up to the MC68020.

The opportunity to design new-generation systems around the MC68020 and the M68000 Family is yours today. Marketplace attention will be focused directly on the growth-oriented companies that take advantage of this opportunity. Motorola's sales engineers and field applications specialists are available and equipped to assist you in moving up to the new 32-bit microprocessor performance standard. Contact one of them today.

Additional technical information is available by writing or sending the completed coupon to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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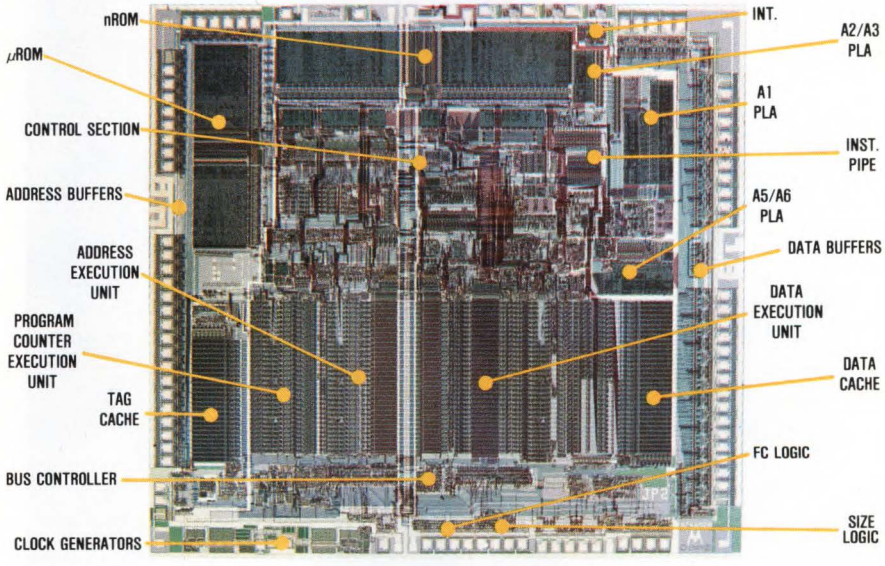

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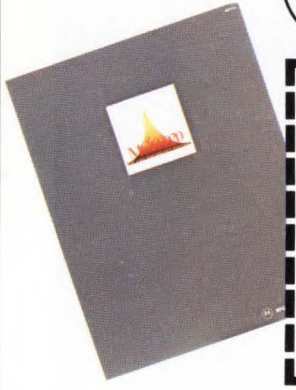

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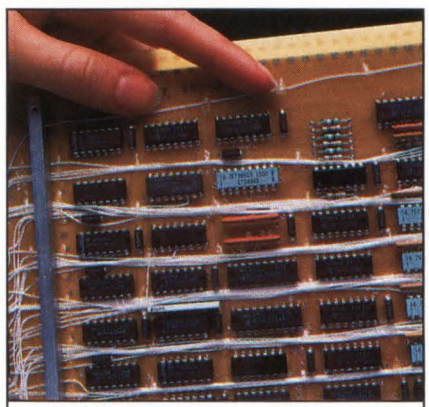
A Texas Control

Months ahead of the market, Control Data is delivering the DDC (Director-to-Device Controller) interface on its 33800 Disk Storage Subsystem. It's an extremely compact, high-speed, large-capacity unit. Most important, it is the only available mass-storage subsystem plug compatible with the new-generation IBM DDC. What helps give Control Data this competitive edge? The SN75174 line driver from Texas Instruments.



Only TI's SN75174 line driver could provide the drive capability vital to Control Data's new 33800 disk storage subsystem featuring DDC interface.

No choice but TI

Only TI's SN75174 could provide sufficient differential current drive through Control Data's special compensation circuit to deliver proper signals in the DDC interface cable.

And Control Data will be able to stay current with future market developments because of the minimum active-high drive (40 mA) capability of the '174.

Forty-two '174s are used in a fully configured 33800 disk storage subsystem.

TI's SN75126 and SN75127 are also used in the new storage subsystem. These circuits meet the IBM 360/370 specifi-

◀ **Leading the market,** Control Data is shipping the first non-IBM storage subsystem that's plug compatible with the IBM Director-to-Device Controller interface. Use of TI's new SN75174 line driver not only made the Control Data design feasible but also minimized design time, component count, board size, and power requirements.

27-4812
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Instruments line driver drives Data to market faster.

cation, providing fault protection and power up/power down protection, as well as enable and fault flags.

Performance as specified

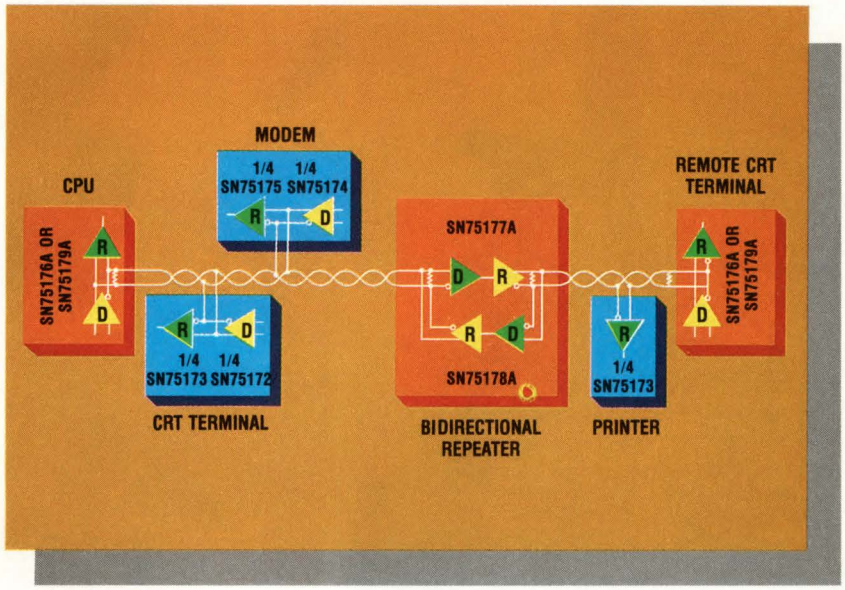
Control Data engineers learned about the '174 early on. Moving quickly, they evaluated and designed it in, counting on it to perform to very exacting specifications. It did . . . perfectly.

The alternative? Greater costs

Control Data engineers estimate that a discrete-component alternative would have resulted in at least a 15% increase in board area to accommodate the necessary additional components.

As it turned out, the SN75174 driver contributed important system savings to the design, improved reliability, helped Control Data get to market faster. ■

Get on the party line faster with eight new line circuits from Texas Instruments.



Hooking 32 driver-receiver pairs on a single bus to achieve party-line communication is possible with TI's full family of line circuits.

Now, eight new line drivers, receivers, and transceivers from Texas Instruments allow you to implement party-line applications on a single bus efficiently.

SN75176A
Half-duplex Transceiver

This new circuit wraps the capability to send or receive data over a single twisted pair in a compact, 8-pin package. It saves board space and cuts component cost.

SN75179A
Full-duplex Transceiver

Also available in a space-saving, 8-pin package, the SN75179A can send and receive data simultaneously, and requires two twisted pairs.

SN75177A/SN75178A
Bus Repeaters

These two differential ICs are identical except for complementary enable inputs. The SN75177A is active high and the SN75178A is active low. This allows you to pair the two back-to-back for improved bidirectional communication when extending cable distance.

SN75172/SN75174
Quad Drivers, SN75173/SN75175
Quad Receivers

The two quad drivers operate from a single +5 V supply, yet maintain a high-impedance output over a common-mode range from −7 V to +12 V with power on or off. Without sacrificing speed. Both drivers have maximum delay times of 50 ns, rise and fall times of less than 80 ns. They allow data rates up to four megabaud.

The major difference between the two drivers is the enable scheme. And this increases design flexibility. All four drivers in the SN75172 are enabled at once, whereas they are enabled in pairs in the SN75174.

The two quad receivers are similar to existing RS-422 devices but have higher input impedance and extended common-mode range, from ±7 V to ± 12 V. Sensitivity is ±200 mV over −12 V to +12 V common-mode range.

All other standards covered, too

In addition to offering these new devices that meet RS-422 and other party-line applications, TI offers the industry-standard ICs you need to meet the EIA RS-485, RS-232-C, and RS-423 standards, as well as IEEE 488.

In fact, with its wide selection of general-purpose line circuits, TI fields the industry's broadest line of line circuits. Results: Component compatibility, design flexibility, and immediate availability.

For details on TI's broad family of line circuits, write Texas Instruments Incorporated, Dept. SLL053E1, P.O. Box 809066, Dallas, Texas 75240.

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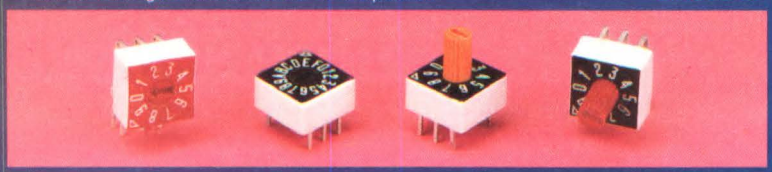
CIRCLE 37



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CONFERENCE PREVIEW

Midcon/84 addresses refinements in speech recognition and synthesis

As testing improves voice recognition, speech synthesis gets a push from CMOS. Meanwhile, chip makers tackle the ISDN.

Testing the accuracy of speech recognition systems has enabled researchers to improve the systems' hit rates. Results of the tests will be a hot item at this year's Midcon, which will be held in Dallas, Sept. 11-13. In addition, extra registers and memory have improved the quality of sound and the vocabulary of speech synthesizers. Finally, in what is still unconquered territory in the U.S., semiconductor manufacturers have introduced complete families of chips to support voice-and-data networks based on the Integrated Services Digital Network (ISDN).

A system that monitors its own speech recognition process helped researchers discover is the best parameter of speech for successful recognition. The Interactive Laboratory System (ILS) from Signal Technology Inc. inspects individual speech parameters as it goes through the basic steps of voice recognition—digitization, segmentation, labeling, feature extraction, template generation, recognition, and performance analysis.

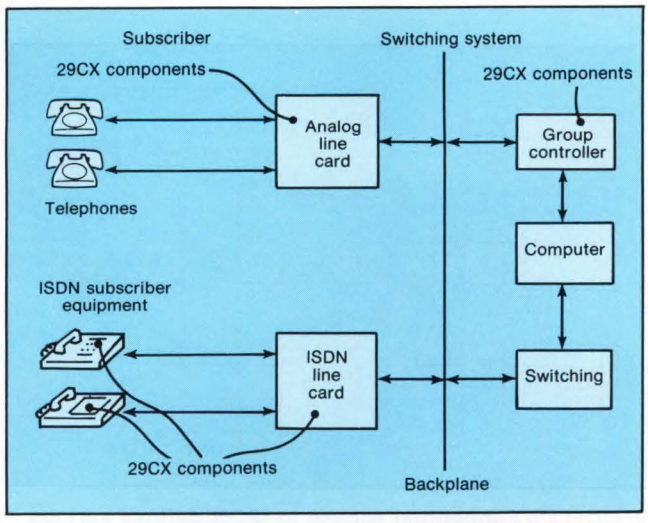
To create templates that could identify words without regard to syntax (and consequent inflection change), experimentors embedded words in a variety of sentences and syntactic positions. The ILS analyzed each word for a number of different speech characteristics. Reference templates were constructed from all of these parameters.

Words that were spoken into the system after the templates were created were broken down and compared with all of the templates. The word was identified by the template whose coefficients it most closely matched. Words that had similar sounds were confused—for instance, the words "keep" and "heat." Results showed that a 95% hit rate could be obtained using a measurement parameter that looked at frequencies below 1 KHz linearly and those above logarithmically.

Generic system

A simpler speech recognition system restricts entry into a secured area by verifying identity. It consists of a self-contained 6800-based voice recognition system. Authorized individuals must record samples of their speech for the machine to recognize.

Developed by Interstate Voice Products (Orange, Calif.), the system can be imi-



1. In a typical switching sytem, an analog line card digitizes voice interformation for backplane switching and routing. The ISDN line card interfaces analog and digital ISDN subscribers with the backplane.

Heather Bryce

CONFERENCE PREVIEW

tated with standard voice recognition hardware. Requirements for the generic system include a voice digitizer, memory for storing reference patterns, a microprocessor for implementing the pattern recognition algorithm, and an input channel. In the generic system, as in the self-contained system, the voice input is analyzed and compared with reference patterns. If the voice matches a reference pattern, the speaker is allowed entry.

Interstate Voice Products set up the system for 25 male and 25 female speakers and determined that 3.5% to 4.5% of the time the system failed, admitting imposters and rejecting true speakers.

In another area, small-geometry CMOS parts and greater on-chip capabilities have improved speech synthesis technology. Texas Instruments Inc. (Dallas) developed the TMS50C40, the CMOS version of an earlier speech synthesis chip. A pitch-fractional register that supplements the standard pitch-period register raises the quality of the chip's speech by allowing it to record more points along a sound wave. The chip uses linear predictive coding to expand the compressed speech. On earlier models, a set number of bits—at most six—were defined for various reflection coefficients (pitch and energy, for example). With the TMS50C40, the user can select up to eight bits, trading off better sound for added memory.

Further, thanks to a mask-programmable option, the user can set keys of a 4-by-4 matrix to generate responses for up to 16 keys on a pad. Formerly, software was required for this type of programming. Enhancements on the TMS50C40 include a 64-kbit ROM that stores 25 seconds of speech and a microprocessor that handles both 4- and 8-bit buses with few interface chips.

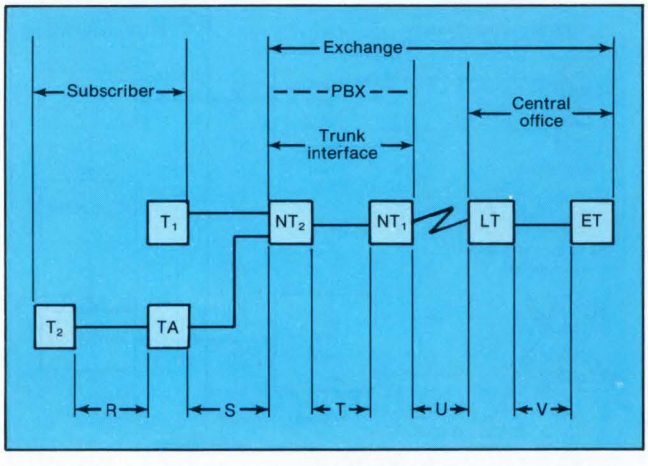
Gould AMI, too, has a basic speech synthesizer that uses linear predictive coding. It shrank a 5-μm CMOS chip with a 3-μm CMOS process and then made the chip into a macrocell, ready to be customized to users' needs.

As the macro core of a chip, the synthesizer lies between a back end (output) and a front end (input logic and timing) and allows either end to be modified. Some of the most popular customizations are likely to be an internal memory for speech or a keyboard interface. Other features, as well, may be embedded in the Gould AMI macrocell.

Switching over

Front-runners in the field, U.S. researchers are trying new approaches toward speech recognition and synthesis. In contrast, the U.S. lags somewhat behind Europe in the area of voice-data networking. To catch up, some U.S. semiconductor manufacturers have implemented the ISDN approaches in their products.

A group of advanced telecommunication components called the iATC 29CX family effect the ISDN protocol in a typical switching system (Fig. 1). Of the components, which were developed by Intel Corp. (Santa Clara, Calif.), the iATC is the intelligent line-card controller, as well as the time-division multiplexer for the network. It interfaces both analog and digital subscribers with the backplane, interleaves signals (on smaller systems), directs



2. CCITT's conceptual access to ISDN defines various interfaces (R through V) within a voice-and-data network. Only the S interface has been fully defined: It interfaces the PBX with the subscriber. Intel's 29C53 four-wire transceiver serves as the interface.

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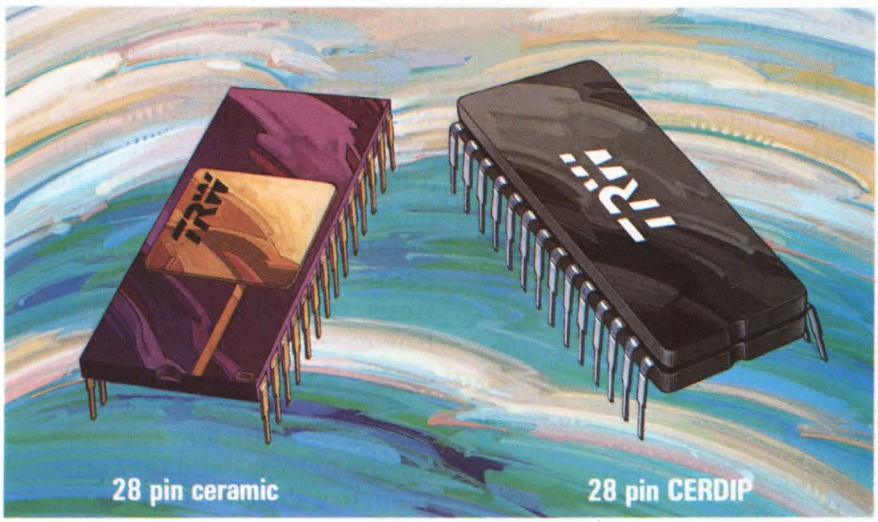

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CIRCLE 38

group signals over dedicated highways, and manages transmissions over serial or parallel highways.

The subscriber interface scheme realized by the 29CX family is the subscriber line data link. This serial protocol, adopted by more than eight manufacturers, is a simple approach that requires only three leads per subscriber. Thus all information can be sent with a 512-kHz data clock, an 8-kHz directional signal, and a bidirectional data link.

Interface travels

A four-wire transceiver, the 29C53, will be the network's S interface, as defined by the CCITT standard (Fig. 2). The transceiver interfaces with the line-card controller through the subscriber line data link. A microprocessor port is planned that will send unformatted data to the 29C53.

Further, a two-wire transceiver link, the 29C55, is being developed together with the 29C53. The link will be a completely separate physical layer capable of 144-kbit/s echo canceling.

Also tackling the ISDN model, Motorola Inc. (Austin, Texas) built a family of universal digital loop transceivers (UDLTs) that integrate voice and data into a single network with a PBX (Fig. 3). The system works with an analog line card that contains the traditional logic functions, a time-slot assignment circuit, a filter-codec, and a subscriber line interface circuit (SLIC) for two-to-four-wire conversions.

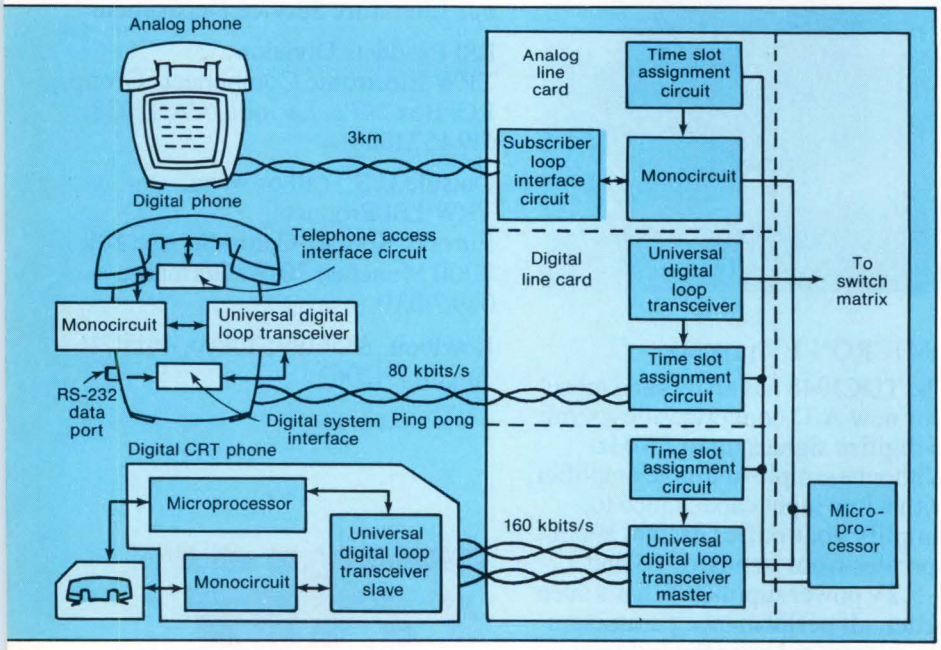
On the analog line card, pulse-code modulation circuits code and decode voice signals using stored voltage references.

Five circuits make up the "monocircuit" family. The 14400 and 14401 work with a transformer interface and a solid-state interface, respectively. With the 14402, the most complex of the circuits, clock speed and volume can be adjusted. Two simpler circuits, the 14403 and 14404, are for synchronous transmission, and the 14405 can run on a variable data clock. The circuits support both line cards and digital phones.

Three time-slot assignment chips direct the signals in a single-party telephone line circuit. The most advanced chip, the 14418, assigns variable time slots for digital switching.

A digital line card that also can be plugged into the network replaces the pulse-code modulator and the SLIC with a master UDLT. Since the pulse-code modulator and the master UDLT perform the same backplane I/O functions, the analog and digital line cards are interchangeable in the PBX.

A master UDLT on the digital line card formats signals for the network and forwards them to a slave UDLT that resides on a remote telephone set. The two transfer data at 80 kbits/s over 26 gauge wire and over larger twisted-pair cables for distances up to 2 km. Even when remote, the circuit can still have high-speed data access to the PBX facility. Using a ping-pong technique, the master and slave UDLTs send and receive voice data at 64 kbits/s and digital signals at 16 kbits/s. □



3. A voice-and-data PBX system from Motorola includes a line-card control for both analog and digital phones.

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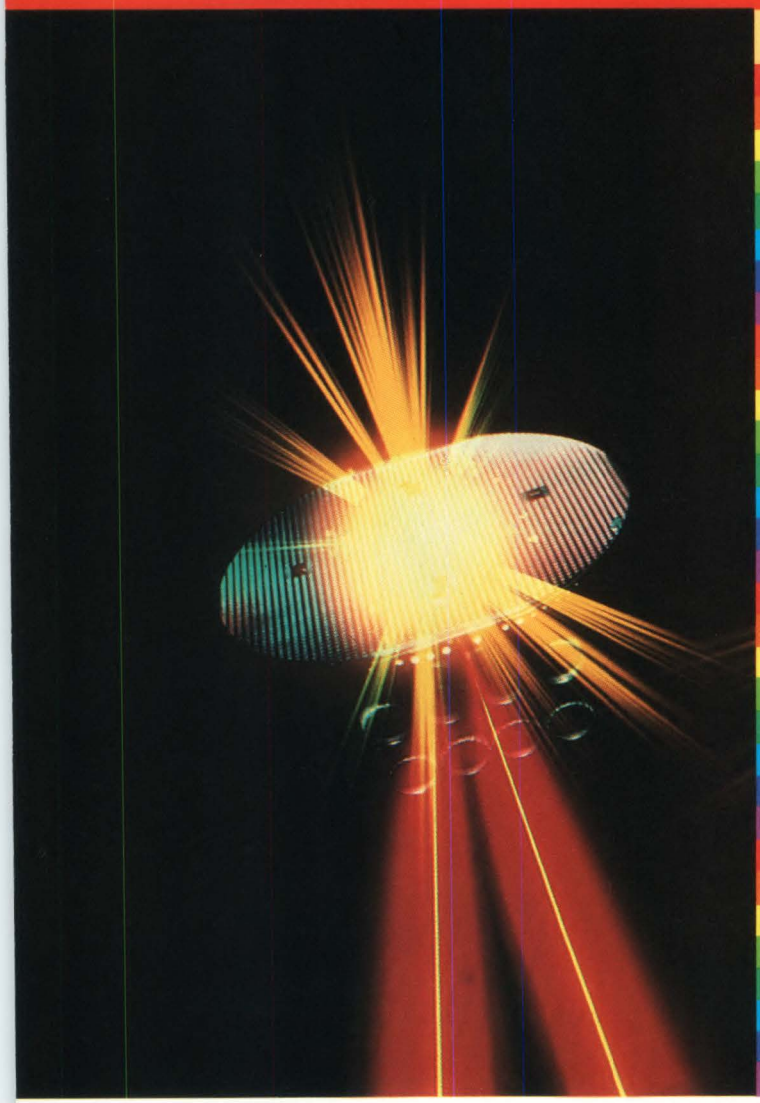
RCA has true low-power drop-in replacements for LSTTL.



97 High speed CMOS types:

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HC/HCT00	Quad 2-Input NAND Gate
HC/HCT10	Triple 3-Input NAND Gate
HCT20	Dual 4-Input NAND Gate
AND GATES	
HC/HCT08	Quad 2-Input AND Gate
HC/HCT11	Triple 3-Input AND Gate
INVERTERS/BUFFERS/BUS DRIVERS	
HC/HCT04	Hex Inverter
HC/HCT365*	Hex Buffer/Line Driver; 3-State
HC/HCT366*	Hex Buffer/Line Driver; 3-State; Inverting
HC/HCT367*	Hex Buffer/Line Driver; 3-State
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting
HC4049	Hex Inverting HIGH-to-LOW Level Shifter
HC4050	Hex HIGH-to-LOW Level Shifter
FLIP-FLOPS (POSITIVE-EDGE TRIGGERS)	
HC/HCT74	Dual D-Type Flip-Flop with Set and Reset
HCT173*	Quad D-Type Flip-Flop; 3-State
HC/HCT174	Hex D-Type Flip-Flop with Reset
HC/HCT175	Quad D-Type Flip-Flop with Reset
HC/HCT273	Octal D-Type Flip-Flop with Reset
HC/HCT374*	Octal D-Type Flip-Flop; 3-State
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting
HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting
LATCHES	
HC/HCT373*	Octal Transparent Latch; 3-State
HCT533*	Octal Transparent Latch; 3-State; Inverting
HC563*	Octal Transparent Latch; 3-State; Inverting
HC/HCT573*	Octal Transparent Latch; 3-State
SHIFT REGISTERS	
HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register
HC/HCT166	8-Bit Parallel/Serial-In/Serial-Out Shift Register

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HC/HCT161	4-Bit Binary Counter; Asynchronous Reset
HC/HCT162	BCD Decade Counter; Synchronous Reset
HC/HCT163	4-Bit Binary Counter; Synchronous Reset
COUNTERS	
HC/HCT4020	14-Stage Binary Ripple Counter
HC4024	7-Stage Binary Ripple Counter
HC/HCT4040	12-Stage Binary Ripple Counter
HC/HCT4518	Dual Synchronous BCD Counter
HC/HCT4520	Dual 4-Bit Synchronous Binary Counter
HC/HCT40102	8-Bit Synchronous BCD Down Counter
HC/HCT40103	8-Bit Binary Down Counter
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HCT157	Quad 2-Input Multiplexer
HC/HCT158	Quad 2-Input Multiplexer; Inverting
HC/HCT251	8-Input Multiplexer; 3-State
HC/HCT257*	Quad 2-Input Multiplexer; 3-State
DECODERS	
HC/HCT138	3-to-8-Line Decoder/Demultiplexer; Inverting
HC/HCT139	Dual 2-to-4-Line Decoder/Demultiplexer
HC/HCT154	4-to-16-Line Decoder/Demultiplexer
HC/HCT238	3-to-8-Line Decoder/Demultiplexer
HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latches
HC/HCT4515	4-to-16-Line Decoder/Demultiplexer with Input Latches
BUS TRANSCEIVERS	
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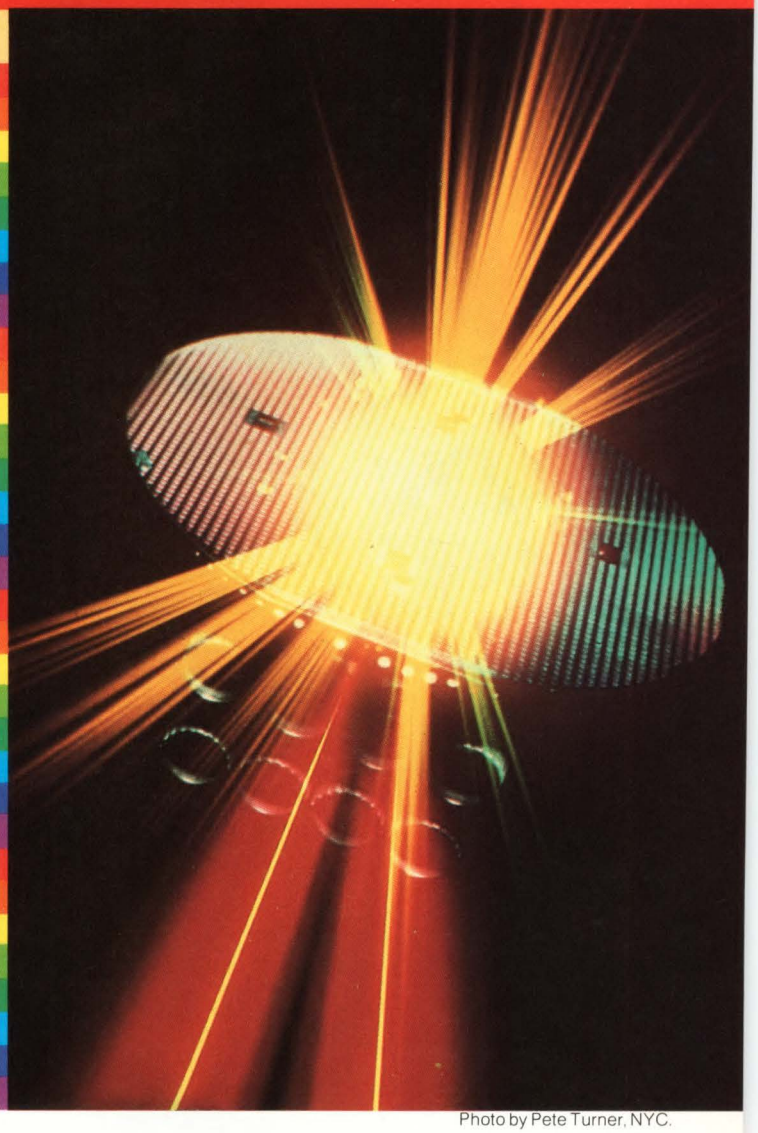
HC/HCT243*	Quad Bus Transceiver; 3-State
HC/HCT646*	Octal Bus Transceiver/Register; 3-State

*Types with a bus driver output stage.



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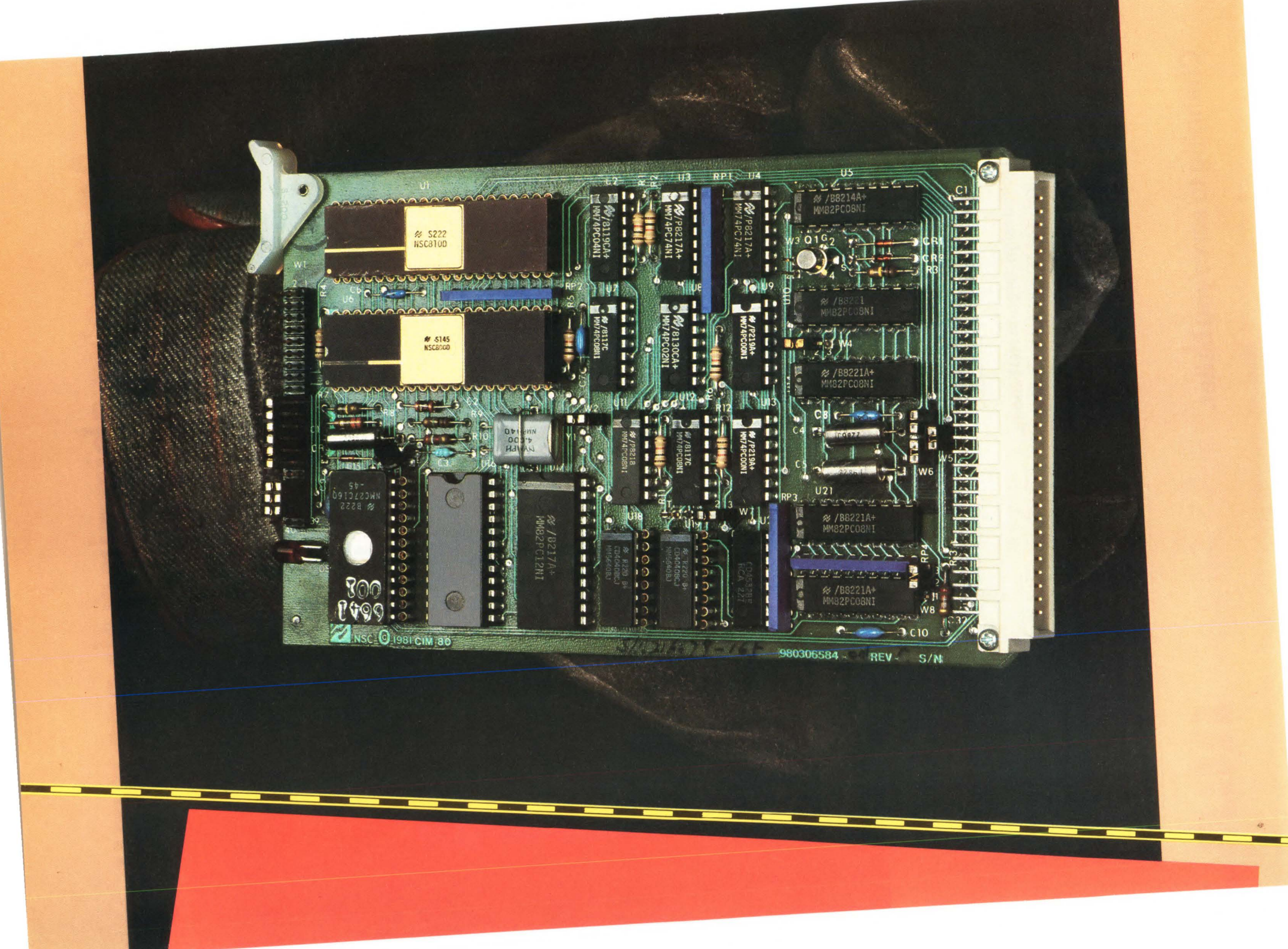
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S222
NSC810D
U6
S145
NSC800D
U3
RP1
U4
U5
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MM82PC08NI
/B8217A+
MM74PC74NI
/B8221A+
MM82PC08NI
/B8217A+
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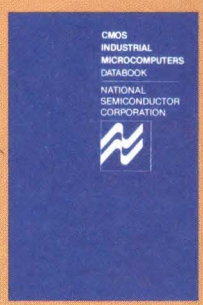

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CIRCLE 45

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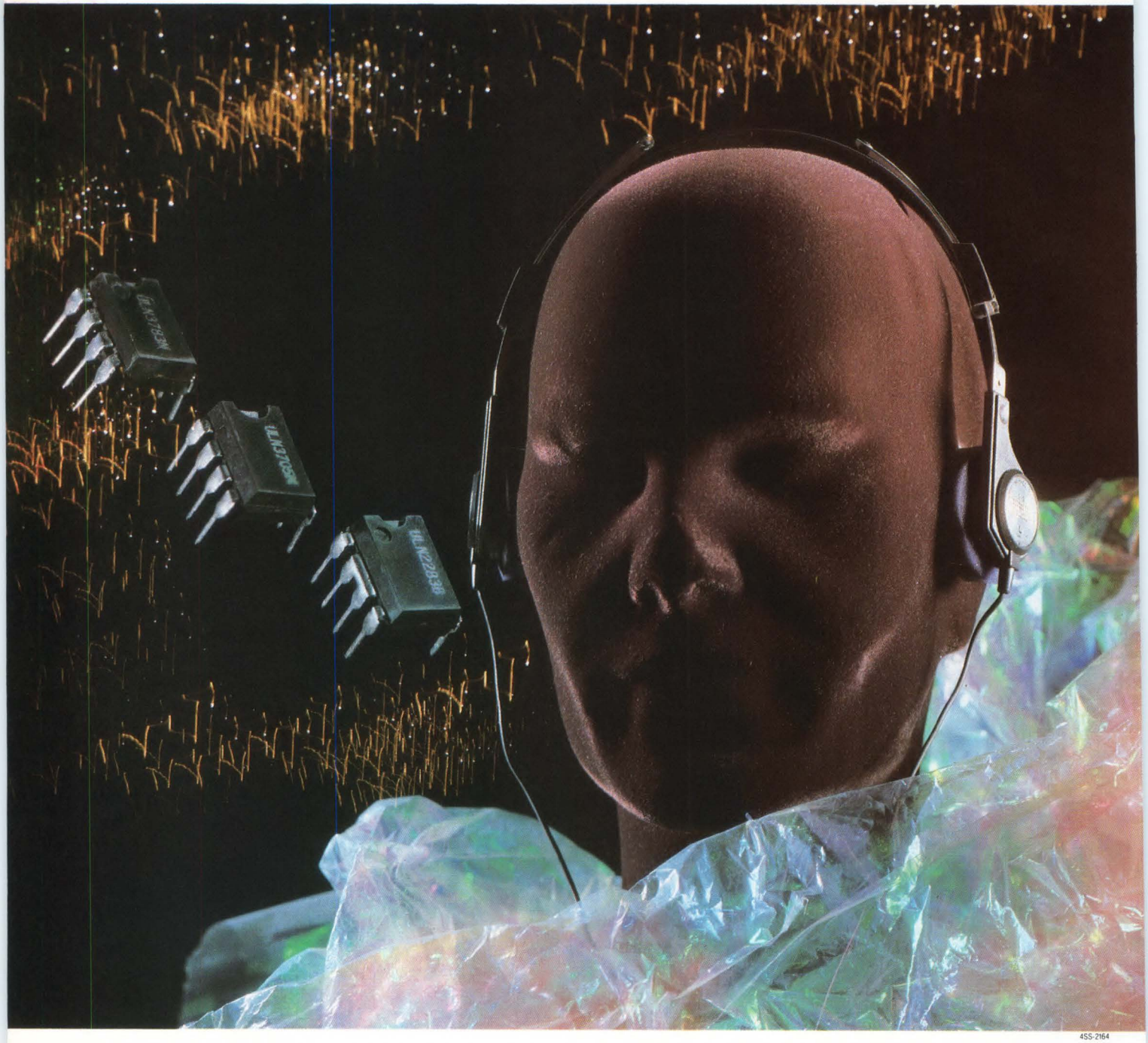

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CIRCLE 102

VIEWPOINT

Functional testing gains importance as boards become more complex

Bob Bergstrom
Marketing Manager
Automated Systems
John Fluke Manufacturing Co. Inc.
Everett, Wash.

As printed circuit boards incorporate more and more LSI and VLSI devices, a greater number of faults remain hidden unless these parts are tested in concert. "Those dynamic faults," says Bob Bergstrom, "will call increasingly for functional testing." Riding close behind this area's return to prominence is a new emphasis on testability and better links between the design and test disciplines.

According to Bergstrom, in-circuit testing, which excels at finding individual component and manufacturing faults in isolation, does not have high enough yield to be relied upon alone. "The problem," he explains, "is that in-circuit testers cannot diagnose dynamic functional faults."

Although functional defects, such as cumulative timing and tolerance buildups, have typically accounted for only 10% of board problems, the picture is changing.

"It's no secret," Bergstrom points out, "that American companies are following the lead of the Japanese in demanding higher-quality parts from their suppliers. As a result, fewer parts are discovered dead or out of tolerance, and functional faults assume a larger proportion of the total."

The growing concentration on functional testing will demand a solution to that method's major drawback—lengthy programming time. In-circuit checks can still help by screening out the majority of board faults first.

Bob Bergstrom's 13 years with Fluke have seen him in a variety of marketing and engineering roles, including the automation of that company's testing operations. Previously, he dealt with Martin Marietta's line of avionics automated test equipment.

Another solution, Bergstrom suggests, involves designing the test stimulus into the board itself. Of course, that will not complete the troubleshooting job. "That is where the functional tester comes in," he adds. "It will ride piggyback on the built-in self-testing routines and perform the diagnostics."

He also sees more and more functional testers making use of bed-of-nails fixtures. "It is extremely important to gain access to the microprocessor and other critical areas of a board without going from the card-edge connector through layers of logic—not only to control the board but for measurements as well."

Bergstrom also believes that comparing a test board with a reference (a known-good board)—a technique that has been around for a while—still has a lot to offer in functional testing. "To test a board you have to have a model of it some place. It can be modeled in software or in hardware. But if you have a

Bob Milne

known-good board as a model, you cannot create a software model that is better than the board itself."

Finally, Bergstrom considers the communications link between test and design engineers equally important, as is the physical link between CAE tools and testers.

"Five years ago a designer probably didn't know anything about his company's ATE equipment. What's more, he did not care. If a divide-by-counter on a pc board provided no easy way for a tester to initialize it, that was not the designer's problem. The test engineer had to spend a lot of time trying to find a solution." Fortunately, says Bergstrom, the heightened emphasis on testability will continue to strengthen a dialogue between design and test engineers.

More memory, at lower cost, will radically alter the way computers operate

Harry Garland
President
Cromemco Inc.
Mountain View, Calif.

The revolution in computer technology will be furthered not so much by microprocessors as by cheaper high density semiconductor memory," says Harry Garland.

In all computer architectures, optimum engineering is constrained by limited memory. "This," he adds, "is increasingly true as computers are called upon to simultaneously handle multiple users and perform multiple tasks." Even a 68000 microprocessor that can address 16 Mbytes is limited by the partitioning of this space for simultaneous tasks.

Engineers waste a lot of time prioritizing memory space assignments and making choices about which tasks must return to disk for their completion. Plentiful and inexpensive memory, Garland suggests, would simplify the assignment of memory spaces, so that engineers will be able to concentrate on better designs for existing applications and even for new applications instead of allocating relatively scarce memory. CPUs will also be freed from having to keep track of as many program instructions and operands scattered throughout memory.

Harry Garland cofounded Cromemco in 1976. While in the electrical engineering department at Stanford University, he helped define the S-100 bus used in the original Altair computers. He holds a PhD in biophysics from Stanford and a BA from Kalamazoo College.

As for improved designs, "A 1-Mbyte work space provides one way of solving a problem, a 16-Mbyte space provides a completely different set of possible solutions." As an example, advanced computer tasks like speech or visual pattern recognition currently utilize algorithms to calculate values that only approximate digitized inputs. It would be much easier and faster to find matching values for spoken words or visual

Stephan Ohr

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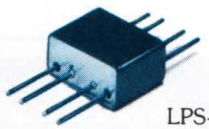
PSC-2-1W
PSC-2-2
PSC-2-4

MSC-2-1



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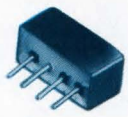

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PSC-2-2		0.002-60	0.3	0.3	0.6	27	30	27	2.0	3.0	4.0	0.15	0.2	0.3	19.95	(6-49)
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CIRCLE 47

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inputs on a memory table and bypass calculations entirely.

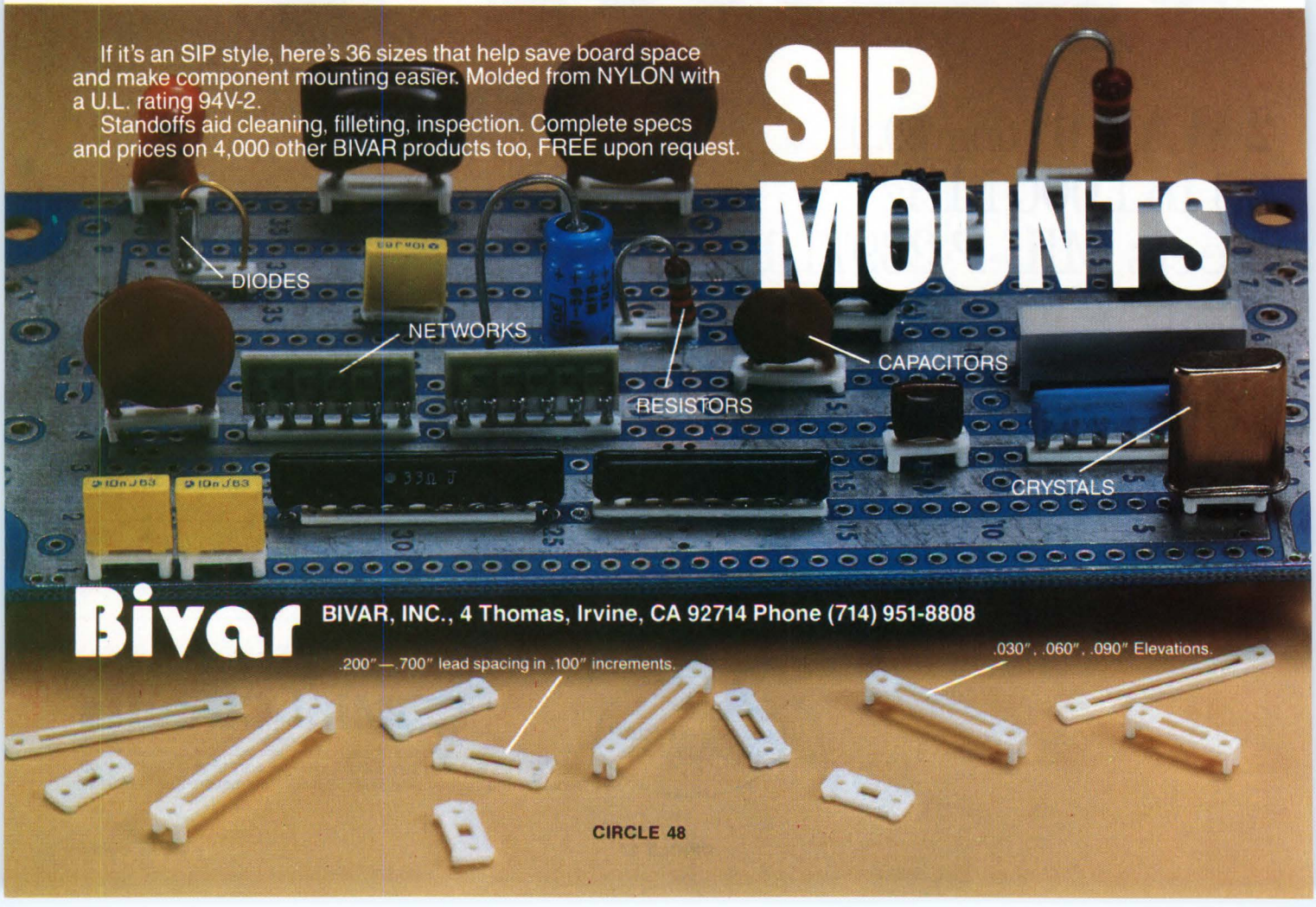
Memory will make a difference in the approach to speech synthesis, as well. The use of phonemes and predictive coding algorithms, says Garland, are compression schemes designed to construct speech when memory is limited. Unlimited memory will allow full digitizing of voice inputs fostering much higher quality of synthesized speech than is possible today.

Matrix inversions, as another example, require frequent returns to disk memory because of limited work space. A 16-Mbyte RAM space speeds up matrix inversions by a factor of 10 without any changes in the computational program.

Computer graphics and digital imaging are other memory-intensive applications. Reproducing one frame of a simple low-resolution television screen, notes Garland, takes more than 256 kbytes of memory. Furthermore, to feel comfortable to the human eye, which is very discriminating, a high-resolution display requires at least a megabyte.

Memory management units can only be a short-term solution. Management schemes can improve how a limited amount of memory is used, but not sufficiently to revolutionize the way computers handle processing. What is required is not more management but virtually unlimited, high-speed semiconductor memory.

The new generation of 256-kbit chips will free computers somewhat from memory restraints, as will the 1-Mbit devices on the horizon. Even more promising is the use of CMOS for RAMs with both lower power and shorter access times. Not only will the cost of the devices be less, but also the attendant expenses of power supplies and cooling. In addition, these chips will reduce the need for other peripheral circuitry by including more housekeeping functions. □

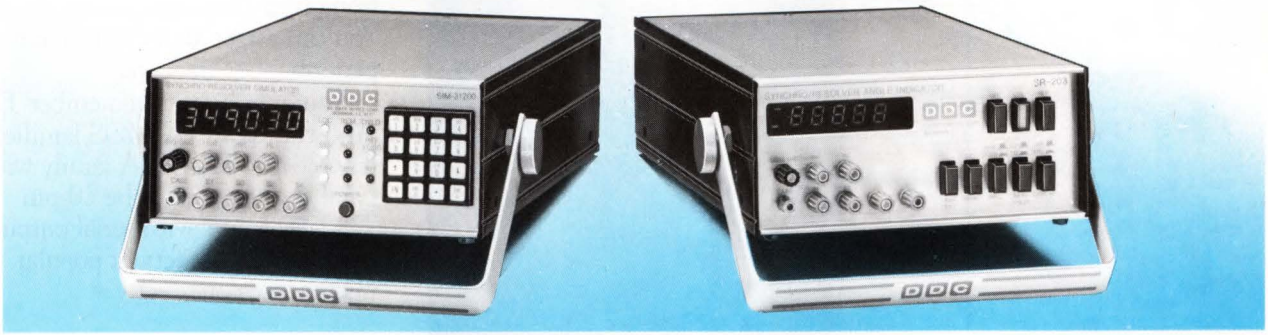


DDC NEWS

ABOUT SYNCHRO-CONVERSION • HIGH-SPEED, HIGH ACCURACY D/A & A/D CONVERSION • DATA BUS DEVICES

PUBLISHED BY **ILC DATA DEVICE CORPORATION** SEPTEMBER 1984

SYNCHRO / RESOLVER TEST INSTRUMENTS COMBINE HIGH ACCURACY WITH SUPERIOR PERFORMANCE



When accuracy and performance are required by your synchro or resolver test application, DDC's **SIM-31200 simulator** and **SR/HSR-203 angle indicators** are unexcelled.

The **SIM-31200 simulators** are broadband (47Hz to 11KHz) synchro and resolver simulators, which incorporate microprocessor control of digital input multiplexing, front panel display, and status/fault flag outputs. An internal converter provides resolution of .001° BCD or .00034° binary, with accuracy up to ± .003° (10 arc seconds). The angle input may be entered locally via the front keyboard, or remotely through the rear panel connector. The remote input format (BCD or binary) is selectable via a rear panel switch. An optional IEEE-488 interface is available.

The outputs are transformer isolated synchro or resolver signals programmable to 11.8, 26, or 90V rms line-to-line.

In addition, the microprocessor works in conjunction with a non-volatile memory and a counting circuit to measure the reference frequency which is used to generate a digital correction and calibration scheme. The instrument is powered by 115V or 230V rms, and has internal EMI/RFI filtering. Bench top and rack mounted configurations with or without front panel keyboard or display are available.

Applications for the **SIM-31200 Series** include production testing, quality control inspections and laboratory instrumentation.

The **SR/HSR-203** are high quality angle indicators used in precision synchro and resolver test equipment. They accept synchro or resolver signals from a front panel input channel or either of two rear connector input channels. Both models are enclosed bench-type instruments, with a carry handle, which may be used as a tilt stand.

Control functions, such as input channel select, input type, bandwidth, unipolar/bipolar, lamp test and inhibit, may be controlled either manually by front panel switches or remotely via the rear connector. An internal IEEE-488 data bus interface is available as an option. The **SR/HSR-203** instruments differ only in their accuracy and resolution. The **SR-203** is accurate to ±0.03°, while the **HSR-203** is accurate to ±.005°. Resolution for the devices is ±0.01° and ±0.001° respectively.

Because they can accept a broad range of voltages and frequencies, without programming, and signal to reference phase shifts of ±50° (max), the **SR/HSR-203** are ideal for situations where a variety of inputs must be quickly accommodated. There can be no hangup 180° away from the input angle. A fault indicator shows when the unit is not tracking the input signal, and an ambiguity indicator shows when the output data is changing.

The **SR/HSR-203,** in addition to serving as high performance bench instruments, can be used wherever accurate angle information is required for display, control, testing purposes, or computation.

Full particulars on DDC's high accuracy instruments are readily available. Circle one of the numbers shown below on the readership service card or call the nearest DDC office for immediate attention. □

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CIRCLE 250 FOR SALES CONTACT

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Plan your LinCMOS

High speed, exceptionally low power consumption, and multipurpose analog and/or digital inputs—new LinCMOS™ microprocessor-controlled data-acquisition systems from Texas Instruments deliver all! You can forget about traditional performance "tradeoffs."

You only have to remember TI. And two new LinCMOS families: The 28-pin TLC532A family with parallel output, and the 20-pin TLC540 family with serial output for interface to a variety of popular microprocessors.

One-chip data-acquisition system

Both families provide an entire data-acquisition system, from analog multiplexer to digital data bus, on one chip. You treat the IC as a simple plug-in component, replacing a board of parts.

Eliminating external components also reduces total system costs. And the chip itself is less costly than many metal-gate CMOS ICs having only an A/D converter function.

One potential application for the new LinCMOS peripherals is environmental control. An array of these A/D peripherals could sense room temperatures throughout a building and feed them to a microprocessor that instructs the heating/cooling system to direct air where it is needed.

Result: Energy bills could be slashed by a simpler, more cost-effective system.

◀ **Moving energy costs down** by moving air around—that's how TI's new LinCMOS A/D peripherals could work in a large building. These ICs could take multiple readings of each room's temperature for a microprocessor that quickly determines where warmer or cooler air is needed.

™Trademark of Texas Instruments Incorporated

Photo taken at Plaza of the Americas, Dallas, Texas.

27-5077 A

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control system with TI's new microprocessor-controlled A/D ICs.

DATA-ACQUISITION EVOLUTION

	1979-83	1981-85	1983-1990s
Technology:			
Process:	Metal-gate CMOS	Metal-gate CMOS	Si-gate LinCMOS
Circuit:	Resistor ladder	Switched capacitor	Switched capacitor
Converter:			
Part types:	ADC0808, 0809N	TL520, 521, 522N	TLC532A, 533A
Size:	8,000 mil²	1,700 mil²	500 mil²
Components:	256 resistors 511 switches	9 capacitors 26 switches	9 capacitors 26 switches
Features:			
Bar size:	29,000 mil²	21,000 mil²	15,000 mil²
Speed:	10k samples/sec.	14k samples/sec.	67k samples/sec.
Error:	±0.75 LSB	±0.75 LSB	±0.5 LSB
Inputs:	8 analog	8 analog	11 analog*

*Includes six multipurpose inputs.

Major speed improvements, more inputs, smaller size—the evolution to LinCMOS products from metal-gate technology reflects big performance boosts and operational advantages, creating a bright linear future.

Up to 71,000 samples per second

Dramatic speeds are available—as fast as 71,000 samples per second. With power requirements as low as 6.0 mW.

This allows noise canceling and precise control of blower motors or heating elements. While virtually eliminating bulky power supplies.

Exceptional stability over a wide temperature range

Both the TLC532A family and the TLC540 family offer excellent temperature-range stability—total output error is within ±0.5 least significant bit (LSB) over a wide temperature range—from −40° to 85°C.

Military versions, also available, are stable within ±0.5 LSB over a −55° to 125°C temperature range.

Handle up to 11 inputs

Each LinCMOS A/D peripheral family allows a processor to monitor up to 11 analog signals. Six signals can be digital, if preferred, allowing keyboard or switch-position sensing.

These devices feature a built-in sample-and-hold circuit (software-controlled on the TLC540) that holds a "snapshot" of the input signals to reduce the effects of noise and random spikes.

Immediate availability

All of these LinCMOS A/D peripherals are TTL, MOS, and CMOS compatible. And all are available now. With performance that will change the way you look at linear.

Environmental control is only one possibility. These LinCMOS peripherals offer many opportunities in test equipment, automotive instrumentation, industrial controls, robotics, toys, home computers, signal processing, and other applications.

For more information on TI's A/D converters, op amps, and the LinCMOS process that creates them, call your authorized TI distributor or nearest TI sales office. Or write Texas Instruments Incorporated, Dept. SLAØ43E1, P.O. Box 809066, Dallas, Texas 75380-9066.

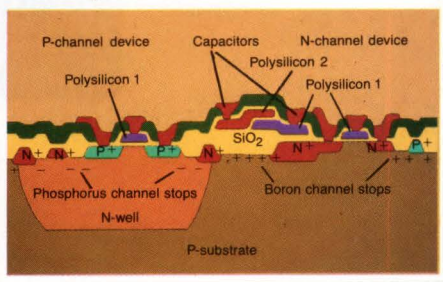
TI is first with silicon-gate CMOS for linear.

The key to a successful combination of CMOS and bipolar capabilities: Phosphorus doping of the silicon gates that effectively halts and binds sodium ions—the main cause of threshold voltage shifts in MOS-based technologies.

For enhanced carrier mobility, NMOS transistors are placed in a p-type substrate and the PMOS transistors in an n-well. This increases carrier mobility of the NMOS transistors to about 3.7 times that of the PMOS transistors, enhancing speed.

The LinCMOS process also provides a gate-to-drain capacitance about one-seventh that of metal-gate CMOS. This performance stems from gate formation, which is accomplished in the same step that forms the transistor source and drain. The source, gate, and drain are all self-aligned, boosting speed and enhancing the bandwidth even further.

And the final result: A built-in speed advantage that greatly enhances AC performance and makes possible the 20X speed improvement of the TLC532A over its pin-compatible metal-gate TL532 predecessor.



TEXAS INSTRUMENTS

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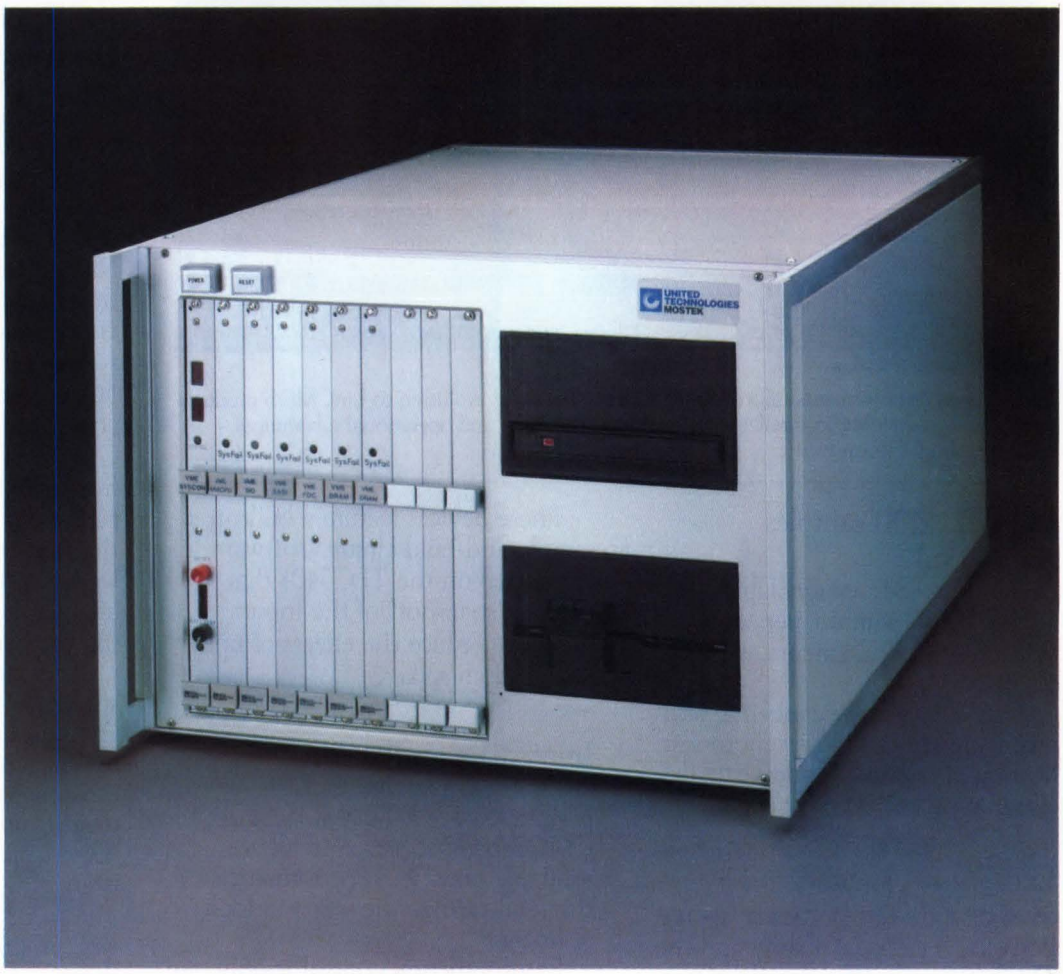
CIRCLE 29

VMEbus + UN



IX™+MOSTEK

Add the above together, and what do you get? The Mostek Matrix 68K™. It combines a multi-user, 16-bit microcomputer system based on the VMEbus architecture – plus a UNIX operating system. The result is a powerful and cost-effective tool for system integrators.

The Matrix 68K is also a high performance tool. It's modular. Structured. Flexible. And easily expandable for future application requirements. What's more, it can lower your development costs, and get your product to the market faster.

This new system in its base configuration features 640KB of expandable main memory, a 36MB Winchester disk, 1MB of floppy disk storage, serial RS-232 interfaces for five users, a standard parallel printer interface, and three open slots for expansion.

The heart of the system is the VME-MMCPU board with its 16-bit processor. The VMEbus-based modular board designs meet today's 16-bit needs. And permit fast, easy reconfiguration for 32-bit applications in the future. So, you won't have to develop another architecture as more powerful hardware becomes available.

The flexibility of VMEbus architecture is further enhanced by the powerful UniPlus +™ operating system (UNIX System III with Berkley enhancements). It provides you with a flexible, expandable operating system that's well suited to program development, text preparation, and general purpose processing. Its supported languages include "C," Fortran, and Pascal.

Another big plus is Mostek's ongoing development of new cards for the VMEbus: a one megabyte DRAM, SMD disk controller, and Intelligent I/O boards will soon be available. With the reconfiguration software package, UNIX can easily be expanded to use these and many more VMEbus boards.

With the Matrix 68K, you get high performance. Full VMEbus compatibility. Transportable software. Flexibility. And unusual value. Because it's all you need today. And tomorrow.

Get in on VMEbus + UNIX + all the future applications. Contact Mostek, 1215 W. Crosby Road, MS2205, Carrollton, Texas 75006, (214) 466-8801. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5-681157.

UNIX is a trademark of Bell Laboratories. UniPlus + is a trademark of UniSoft Systems. UniPlus + is derived from UNIX System II under license from AT&T. Matrix 68K is a registered trademark of Mostek Corp.

What a performance! Seven new data acquisition and control boards for your IBM PC.™

Encore! Encore!

Data Translation has done it again. Our first two analog and digital I/O boards for IBM personal computers received rave reviews.

So we extended our product line to seven ... starting at $295 for quantity purchasers.

While most of the personal computer world focused on home and office applications, we lifted the curtain on two other key areas. Laboratory data acquisition and industrial control.

Now, no matter what you need for your IBM PC, we have it. Each board is a complete data acquisition and control system. With A/D, D/A, digital I/O, and a programmable clock. You simply choose the board offering the speed and resolution you need most. Just plug it into your PC's backplane and it's showtime.

With on-board intelligence, all seven are software compatible and supported by Data Translation's PCLAB software package.

Price (U.S. $)	Class	Model	A/D Resolution (bits)	A/D No. of Channels	A/D Speed (KHz)	D/A Resolution (bits)	D/A No. of Channels	D/A Speed (KHz)	Digital I/O Channels	Programmable Clock
295 (OEM) 495	Low Cost	DT2808	10	16SE	3.3	8	2	10	16	yes
1195	General Purpose	DT2801	12	16SE or 8DI	13.7	12		16		
1345	High Speed	DT2801-A	↓	↓	27.5	|	|	33	|	|
2170	High Resolution	DT2801/5716	16	8DI	2.5	|	|	16	|	|
1295	Low Level	DT2805	12	|	13.7	|	|	|	|	|
2270	Low Level, High Resolution	DT2805/5716	16	↓	2.5	|	|	↓	|	|
1695	Simultaneous S/H	DT2818	12	4	27.5	↓	↓	33	↓	↓

NOTES: 1. PCLAB software supports all models. 2. Programmable gain is standard for all DT2801 and DT2805 models.
3. Screw terminal and signal conditioning panels available for connection of all I/O signals.

Data Translation is playing the leading role in personal computer data acquisition and control. Find out how we can help your performance today.

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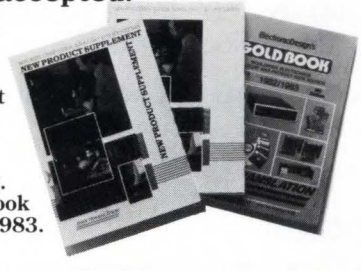

See our new 192 pg. product supplement in Gold Book 1984, Vol. III, and our 336 pg. catalog/handbook in Gold Book 1983.

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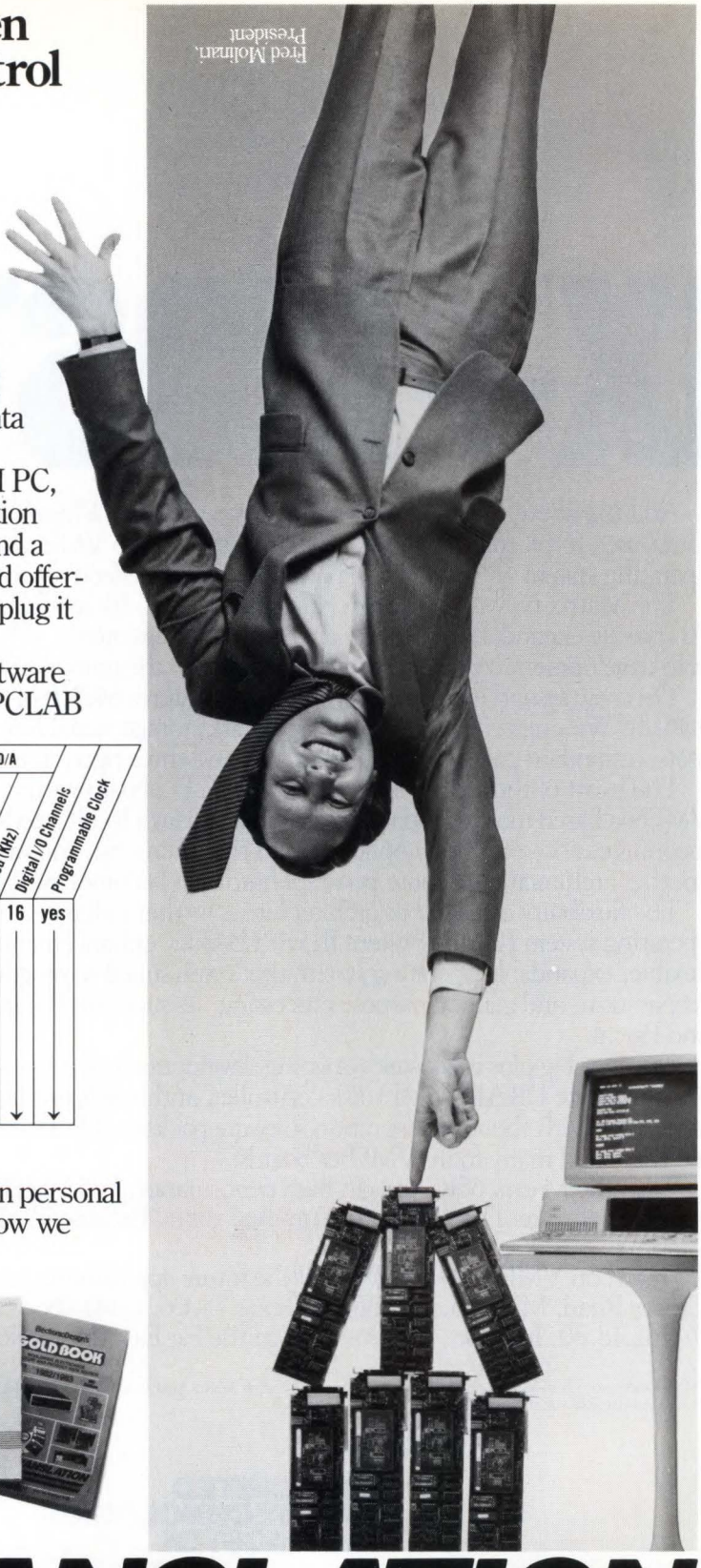

DATA TRANSLATION

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CIRCLE 26

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IBM® PC Personal Computer,
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A complete system . . . **a $4,000 VALUE!***

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electronic tuning . . . including 6 tapes
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F 93-A REV. ORIG.

Design Contest

MICROWAVE JOURNAL OFFICIAL JUDGES

It's Easy to Enter

Do you have a clever design idea or application involving IF/RF/microwave signal-processing components—mixers, power splitter/combiners, attenuators, RF transformers, directional couplers, amplifiers or RF switches? Or perhaps a versatile setup for testing them or a novel approach to enhance their performance.

If you have an original idea, enter Mini-Circuits Design Contest now. Type or legibly print your submissions. Start with a brief abstract describing the key point of your idea (cost saving, improved performance, simplified testing, etc.). List RF signal processing components used. Then proceed with the detailed explanation. Make schematics and block diagrams clear; include values of circuit components. Be sure to include performance data and curves; judges' scores will be based on content, multiplicity of products involved and thoroughness.

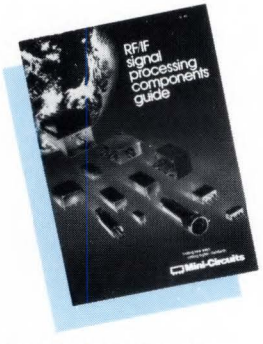
Contest Rules

1. Submit as many entries as you wish.
2. Ideas should be original and non-proprietary.†
3. Entries will be judged by the editorial staff of Microwave Journal and their decisions will be final. The top 25 winning entries will be published in Microwave Journal.
4. All entries become the property of Mini-Circuits Laboratory and must be received by December 31, 1984.
5. Employees of Mini-Circuits Laboratory, Microwave Journal and their sales representatives, are not eligible.
6. Contest void where prohibited by law.
7. Make sure to include your business address and phone number. In addition, for non-U.S. entries, indicate AC power line voltage and frequency.
8. Send your entries to:
   Mini-Circuits' Design Contest
   P.O. Box 137
   Brooklyn, NY 11235

†Winners may be asked to sign an affidavit of eligibility & release.

Good Luck, and Thanks.

The Mini-Circuits Design Contest, with its competitive excitement and fabulous prizes, is our way of thanking all of the designers worldwide whose staunch customer support has been responsible for our continuing growth.



Free 64-page RF/IF Signal Processing Components Guide

For an up-to-date review of Mini-Circuits' IF/RF/Microwave product line, refer to EEM, EBG, Gold Book or Microwaves Directory. Or call/write our factory or any of our 45 worldwide sales offices for our 64-page RF Signal-Processing Components Guide.

Free fact-filled Question/Answer Series on RF Signal-Processing Components

Since Mini-Circuits is the world's largest manufacturer of mixers and RF signal-processing components, it's natural for us to receive hundreds of questions from engineers on these products. How to test them, how to make the right selection, how to optimize a circuit design ... questions with answers not found in textbooks or reference manuals.

So we've put together a series of Q & A (question/answer) booklets on most-frequently asked questions on mixers, phase detectors and power splitter/combiners. They are loaded with application-oriented tips, ready to solve a problem you may be facing. The set is free ... just call or write us or any of our 45 worldwide sales representatives.

F 93-B REV. ORIG.

send your entries to:

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P.O. Box 137,
Brooklyn, New York 11235

EXAMPLE 1:

Low-cost, high performance Image-Rejection Mixer.

KEY COMPONENTS; mixers, power splitters.

Many telecommunications systems require a mixer arrangement that delivers the desired IF and sharply rejects the other image frequency.

An effective, low-cost solution makes use of Mini-Circuits' TFM-2 mixers and it's 2-way, 0° PSC-2 and 2-way, 90° PSCQ-2-90 power splitter/combiners as shown in the diagram.

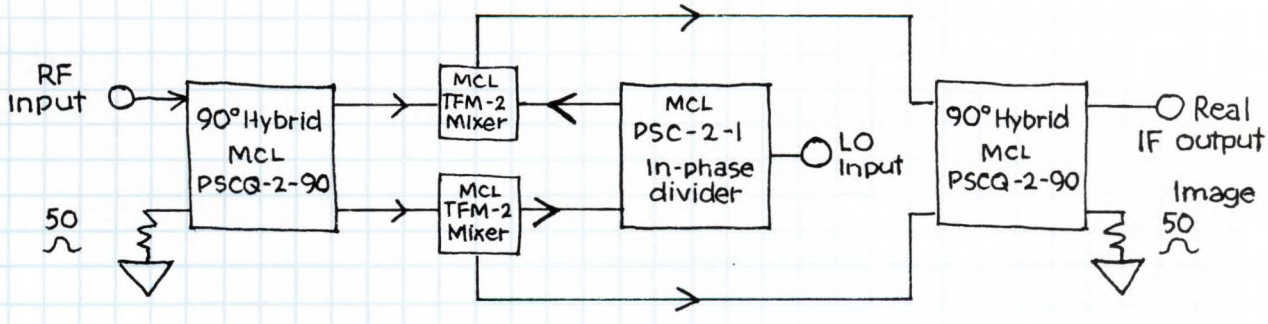
The key to an efficient image-rejection, such as shown in the block diagram, is the use of double-balanced mixers with well-matched amplitude and phase characteristics and high isolation. However, poor hybrid phase characteristics, differences in the output amplitudes of the hybrids and non-symmetrical external circuits will also reduce image-rejection performance. The effects on sideband suppression caused by unequal mixer amplitude and phase shift are shown in Tables 1 and 2.

Table 1
Amplitude Unbalance vs. A, dB

Unbal, dB	A, dB
0.3	35
0.9	27
1.5	22
2	13
3	15

Table 2
Phase Unbalance A, dB

Phase Unbal, degree	A, dB
3	33
9	22
15	18
20	15
30	12



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Engineering Dept.,
Alphaomega Corp.,
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setting higher standards
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A Division of Scientific Components Corporation
World's largest manufacturer of Double Balanced Mixers
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EXAMPLE 2:

Improving two-tone, third-order IM measurements.

KEY COMPONENTS; power splitters, attenuators, amplifiers

Two-tone, third-order intermodulation (IM) expresses the degree of non-linearity of an amplifier or mixer. This parameter is generally not included on data sheets because it is dependent upon operating frequencies, terminating impedance and input levels; it must be measured under specific design performance conditions.

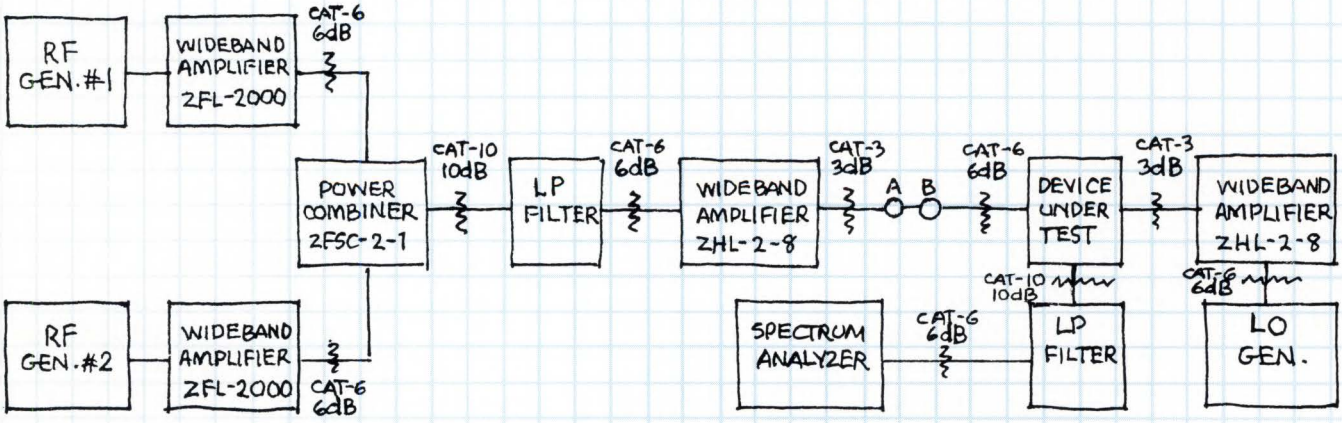
Two common errors in these measurements are (1) failure to provide adequate isolation between input signal generators and proper impedance matching and (2) insufficient filtering of the two input test signals.

A proper test setup for measuring two-tone, third order IM distortion is shown. Note the use of two amplifiers and 6dB pads for input generator isolation and proper 50 ohm matching. A practice of simply using a Tee-connector between generators developes mismatches, producing undesired harmonics which dramatically affect accuracy.

Two-tone, third-order IM distortion is only meaningful when the input levels to the device-under-test are defined.

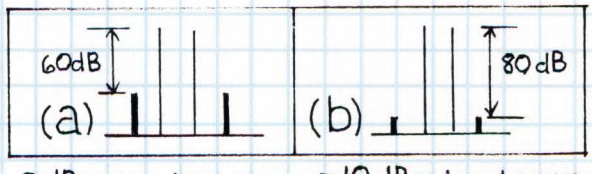
Examine the spectrum analyzer display for a ZAY-1 double-balanced mixer. Notice the significant difference in two-tone, third-order component with an input level of -10dBm for each tone (b) compared with 0 dBm input level for each tone (a).

Also, the amount of two-tone, third-order must be specified relative to either the RF input or desired IF output; the desired IF output is more meaningful.



GENERAL NOTES

1) All Mini-Circuits products have model numbers shown.
2) 0dBm input, A-B connected as shown
   -10dBm input, insert CAT-10, 10dB between A-B



0dBm input power -10dBm input power

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CIRCLE 49

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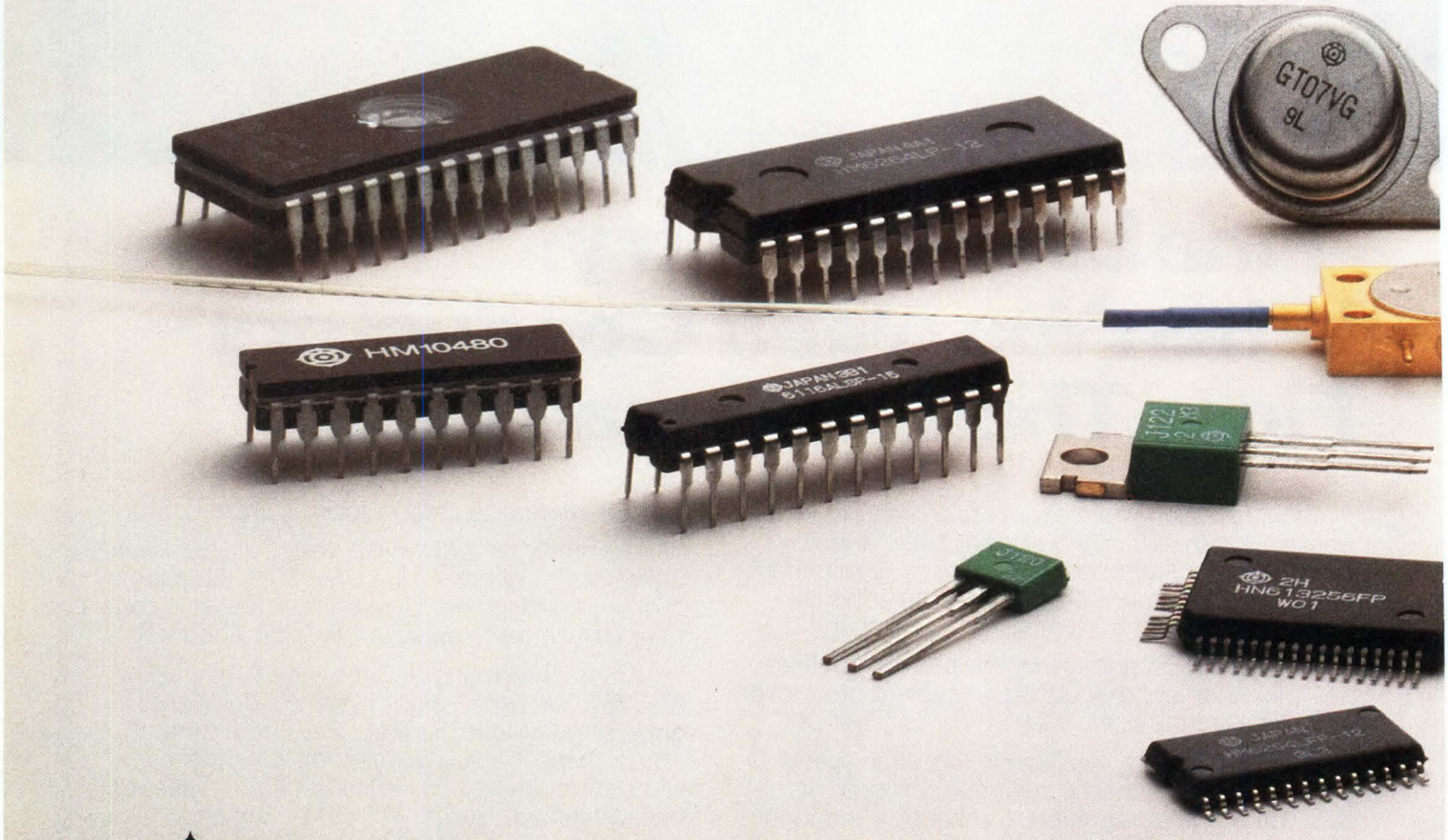

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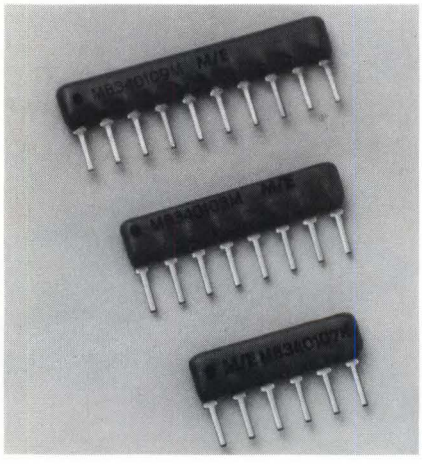

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Low Profile Resistor Networks

- Mil qualification approval per MIL-R-83401 in all pin styles, /07 (6-pin), /08 (8-pin), /09 (10-pin)
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CIRCLE 50

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- Offered in PCB mounting configuration or with std. screw terminals
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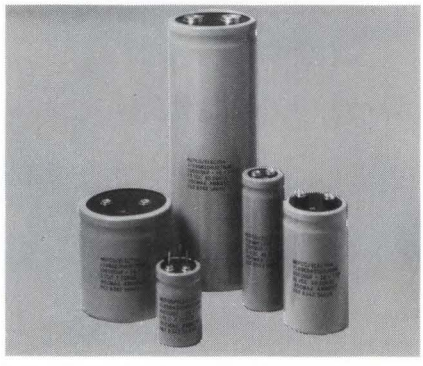
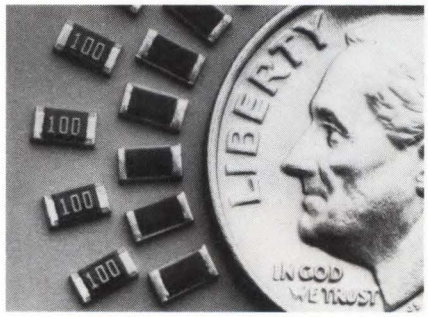
CIRCLE 51





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- Provides dramatic reduction of PCB real estate in new designs
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%	Ω	PPM/°C
±1	10 to 1M	±100
±5	10 to 1M	±200
±10	1.2M to 10M	±200

Zero ohm unit is also available

- Bulk or tape and reel packaging

CIRCLE 52

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Digital signal processing makes the headlines at European conference

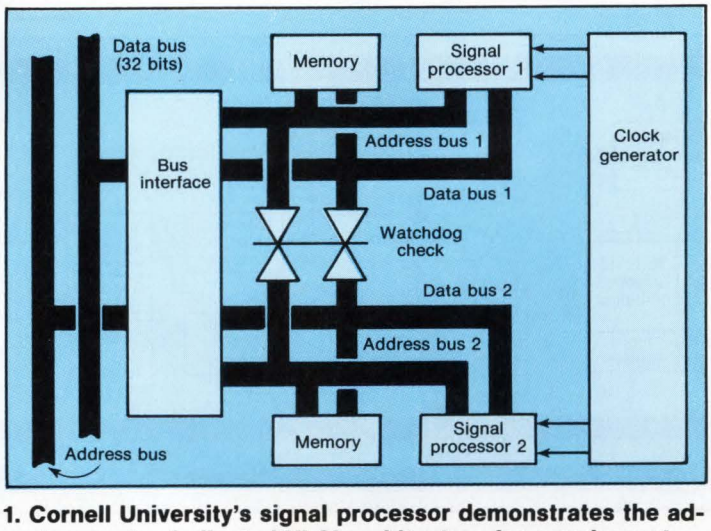
High-speed CMOS signal processors garner their share of glory at the conference; NMOS and bipolar are not left out in the cold.

Finer design rules and tighter chip layouts have yielded CMOS chips that rival the speeds of their NMOS and bipolar counterparts, opening the floodgates to the era of CMOS digital signal processors. These devices are very much in evidence at this year's European Solid-State Circuits Conference. Nevertheless, neither NMOS nor bipolar chips are overshadowed at ESSCIRC '84—architectural and process developments are putting both to work in faster and denser devices. The meeting, which will be held in Edinburgh (Sept. 19–21), will also take a close look at the progress in computer-aided design.

An essential ingredient of many digital signal-processing systems is a circuit for performing fast Fourier transforms. The speed that CMOS is clocking in at can be seen in a processor that computes 1024-point FFTs on complex inputs in a mere 1.4 ms and also executes a staggering 15.4 million multiplications/s. The 2.5-μm bulk-CMOS processor (Fig. 1), developed by Cornell University (Ithaca, N.Y., U.S.), contains 61,000 transistors and uses serial multipliers and adders. Intended for radar and sonar signal processing, the device's serial registers are distributed throughout the arithmetic section so that signals can propagate rapidly between stages.

A bit-slice 2-μm CMOS chip will form the number-crunching core of a Harvard-architecture digital signal processor. The IC, from Philips International BV's Research Laboratories (Eindhoven, the Netherlands), carries 18,600 transistors and connects to other functional blocks within the signal processor through two 16-bit data buses and a control bus (Fig. 2).

Operands for the multiplier's accumulator come from outside the core via the buses or are stored locally in a three-port register file. Addressing two operands in the register file, putting them onto the buses, multiplying both, and storing the result in the product register takes one processor cycle. The device's expected cycle time—about



1. Cornell University's signal processor demonstrates the advantages of a dedicated VLSI architecture for carrying out complex digital signal processing. The chip capitalizes on its ability to be connected with other identical ICs to form a fault-tolerant array.

Mitch Beedie

100 ns—will suit it to speech recognition and similar applications.

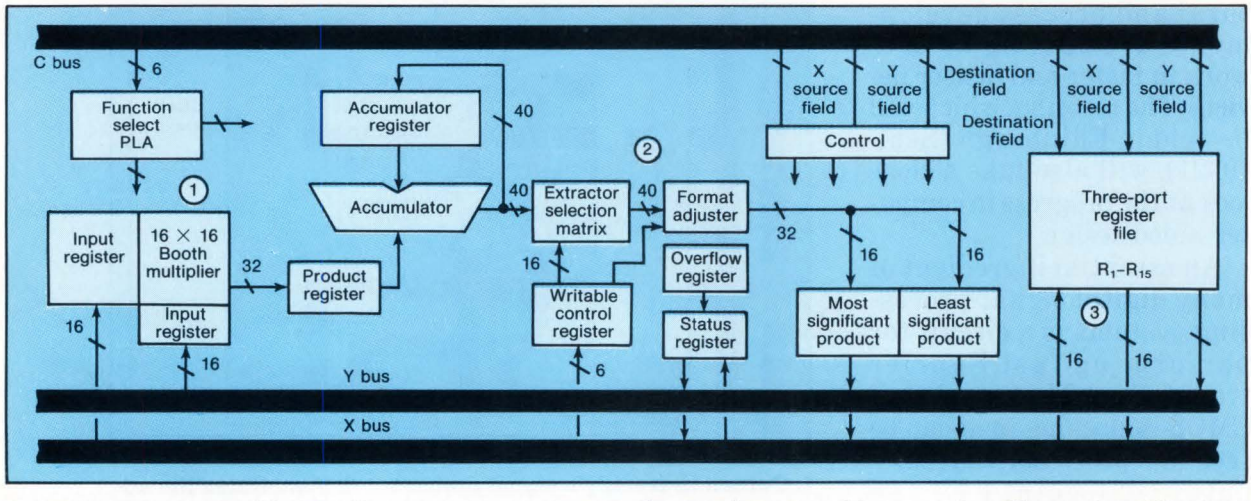
A CMOS chip that is laid out with 3-μm rules features both programmable echo canceling and gain setting. The processor, developed by Bell Telephone (Antwerp, Belgium), shapes speech signals to CCITT specifications and serves as a control link between a subscriber line interface circuit (SLIC) and a line card controller. The 23,000-transistor chip receives line-control data in 8-byte packets from the card controller, and SLIC control data is exchanged through a 256-kHz full-duplex link.

Though impressive performances are being turned in by CMOS chips, NMOS technology is holding its own. A systolic processor for digital video-matrix operations, for example, runs at 13.5 MHz and reverse-transforms luminance and color-difference video signals into RGB signals. The 3.15-μm NMOS peripheral processor is part of an experimental video decoder for 108-Mbit/s wideband digital TV. The chip, from CCETT (Cesson-Sevigné, France), carries 35,000-transistors and is equipped with three processors, each of which carries out linear functions XA+YB+ZC (where X, Y, and Z are 8-bit coded constants). During each 13.5-MHz clock cycle, three bytes are pipelined into the processor from a 24-bit input bus; the result emerges 13 clock cycles later at the outputs.

For document analysis, an optical recognition circuit can search text—at the rate of 500 char/s—for a given string of characters. The full-custom IC, from the University of Louvain (Louvain-la-Neuve, Belgium), links to a 68000 microprocessor over the VMEbus and also can be used for coding graphics and images (Fig. 3). The bit-slice IC is programmable and runs many of the highly repetitive algorithms associated with document analysis. In operation, the microprocessor sequences an algorithm at a high level, and the custom IC handles segmentation. The chip contains 10,000 transistors, is built with a 6-μm NMOS process, and has a 4-MHz clock frequency.

Twice is nice

Virtually doubling the speed of existing converters, a 6-bit analog-to-digital converter samples at 200 MHz. The bipolar device shuns the parallel operation that is the norm for high-speed a-d converters and uses instead rapid master-slave comparators that are arranged in four blocks, with three encoding stages. The chip, from the Entwicklungszentrum für Mikroelektronik (Villach, Austria), has no missing codes and a signal-to-noise ratio as high as 37 dB at fre-



2. A microprogrammable bit-slice processor serves as the number-crunching core in a Harvard-architecture device. From Philips Research Laboratories, the chip is fabricated in 2-μm CMOS and features three buses. The X and Y buses handle the operands and products, and the C bus takes care of control functions.

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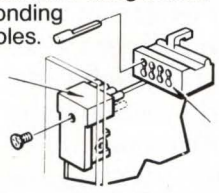

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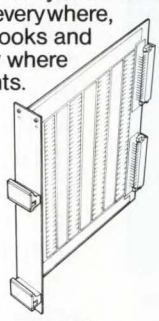
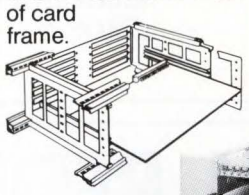


Horizontal Mounting Kit

Horizontal Mounting Kit accommodates any size of PCB within width of card frame.



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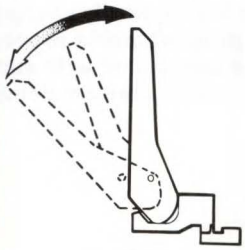

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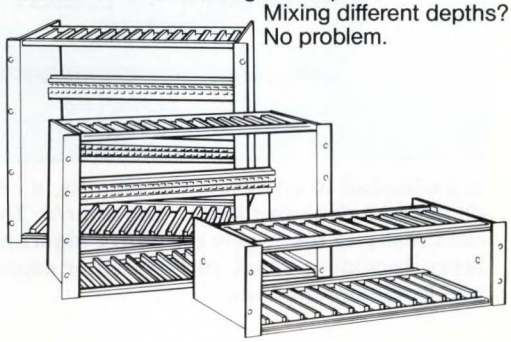

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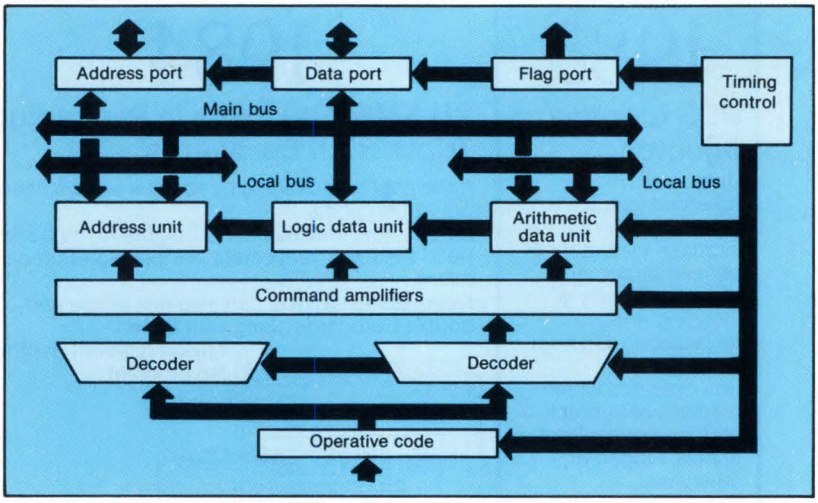

3. Dedicated to analyzing documents, a chip that optically recognizes characters can scan text at 500 char/s. The programmable processor runs many of the highly repetitive algorithms associated with such tasks, including block and character segmentation, contour detection, and Boolean functions.

quencies up to its Nyquist limit of 100 MHz.

One approach to digital signal processing actually falls under the CAD portion of the conference, since the elements of a bit-serial digital signal processor have been created with a silicon compiler. Researchers at the Wolfson Microelectronics Institute at the University of Edinburgh have produced a cell library that consists of addition, subtraction, multiplication, multiplexing, and other processing functions—including a mixture of dynamic and static logic. The ICs operate at 20 MHz and are fabricated with 2.5-μm bulk-CMOS.□

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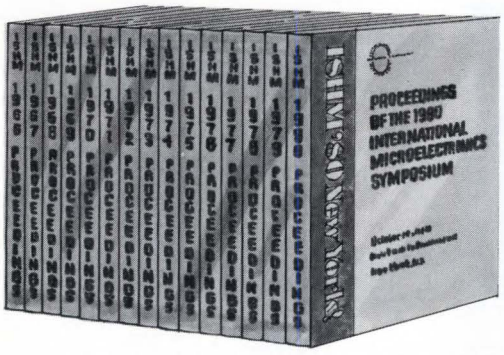

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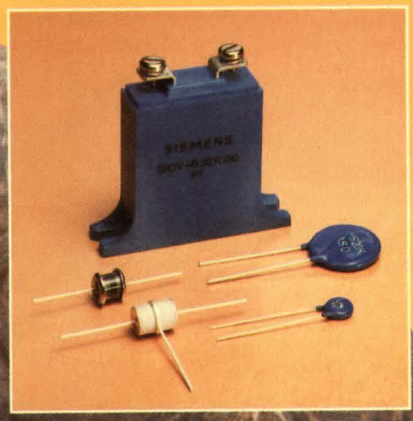

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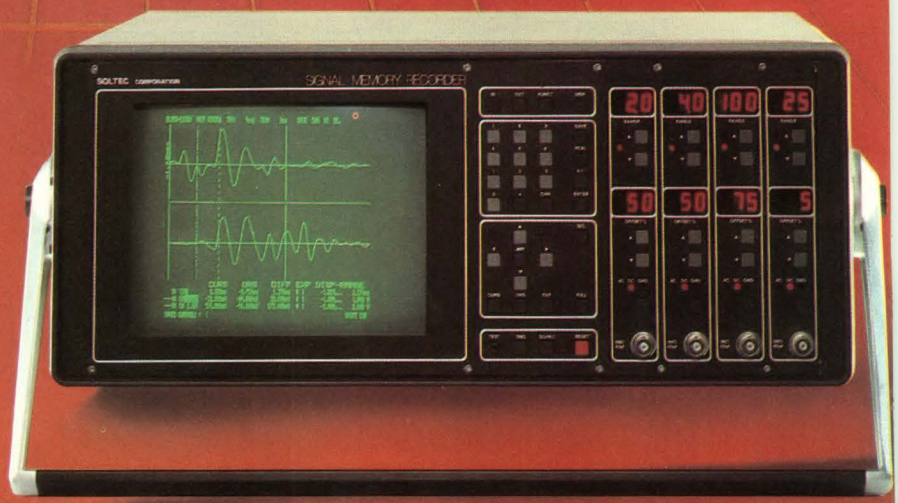

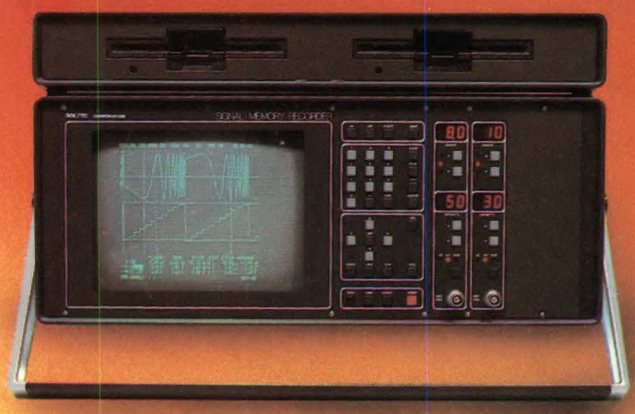

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INTERNATIONAL MEETINGS

Third International Conference on Flexible Manufacturing Systems, Sept. 11–13. Stuttgart, West Germany. IFS (Conferences) Ltd., 35-39 High St., Kempston, Bedford MK42 7BT England; (0234) 853605.

Exhibition with Congress on Technology Innovation in Power Electronics, Motors, Drives & Motion Control, Sept. 18–20. Geneva, Switzerland. Incom Zieroth & Partner, Kleinreuther WEG58 D8500, Nuremberg 10, West Germany.

Tenth European Solid-State Circuits Conference (ESSCIRC '84) Sept. 19–21. Edinburgh. ESSCIRC '84 Secretariat, CEP Consultants Ltd., 26 Albany St., Edinburgh EH1 3QH, Scotland; (031)-557 2478.

Unix Systems '84, Sept. 19–21. Kelsey Kerridge Hall, Cambridge, England. Network Events Ltd., Printer Mews, Market Hill, Buckingham MK18 1JX, England; (0280) 815226.

Design Engineering Show, Sept. 25–28. NEC, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59-61 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

Sama/Swissdata/Autofact Europe '84, Sept. 25–29. Swiss Industries Fair, Basel, Switzerland. Leslie Hossack, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-0023.

Semiconductor International Exhibition, Sept. 25–27. NEC, Birmingham, England. Cahners Exhibition Ltd., Chatsworth House, 59-61 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

Eurocon '84, Sept. 26–28. Brighton, England. Conference Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; 01-240 1871, ext. 222.

Symposium on Electrostatics, Sept. 26–28. Southhampton, England. Oyez Scientific and Technical Services, Booth House, 3rd floor, 56 Holborn Viaduct, London EC1, England; (01) 236 4080.

International Symposium on Industrial Robots (ISIR), Oct. 1–4. Gothenberg, Sweden. Patricia Van Doren, RI/SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 369.

World Conference on Ergonomics in Computer Systems, Oct. 1–2, London, England; Oct. 3–4, Dusseldorf, West Germany; Oct. 4–5, Helsinki, Finland. Robert W. Bailey, Computer Psychology Inc., 54 E. Main St., PO Box 16, Mendham, N.J. 07945; (201) 543-9009.

Automatic Testing and Test Instrumentation Conference and Exhibition, Oct. 2–4. Paris, France. Network Events Ltd., Printer Mews, Market Hill, Buckingham MK18 1JX England; (0280) 815226.

Infomatics '84, Oct. 2–4. Hyatt Regency, Singapore. Infomatics '84, PO Box 34404, Bethesda, Md. 20817; (301) 983-0604.

Toronto Tool & Manufacturing Engineering Conference & Exposition, Oct. 2–4. International Centre, Toronto, Ontario. Tom Reichert, Expositions Division, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 323.

Japan Electronics Show, Oct. 4–9. Harumi International Fair Ground, Tokyo, Japan. Japan Electronics Show Assn. Tokyo Chamber of Commerce Building, 3-2-2, Marunouchi, Chiyoda-ku, Tokyo, Japan.

Taiwan Electronics Show, Oct. 5–11. Taipei Sungshan Airport, Taiwan. China External Trade Development Council, Taipei Sungshan Airport, Taiwan.

Computer Graphics '84, Oct. 9–11. Conference and Exhibition, London, England. Online Conferences Ltd., Pinner Green House, Ash Hill Drive, Pinner, Middlesex HA5 2AE; (01) 868-4466.

Machine Intelligence '84, Oct. 9–10. Novotel London Hotel, Hammersmith, England. Bob Tracy, Industrial & Trade Fairs, Ltd., Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG; (01) 940 6065.

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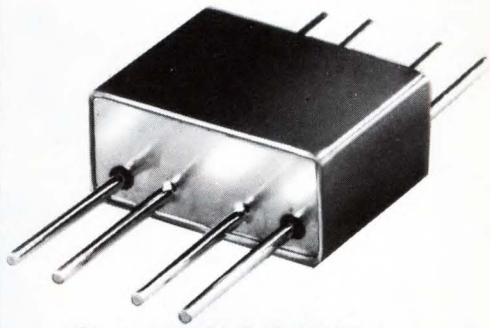

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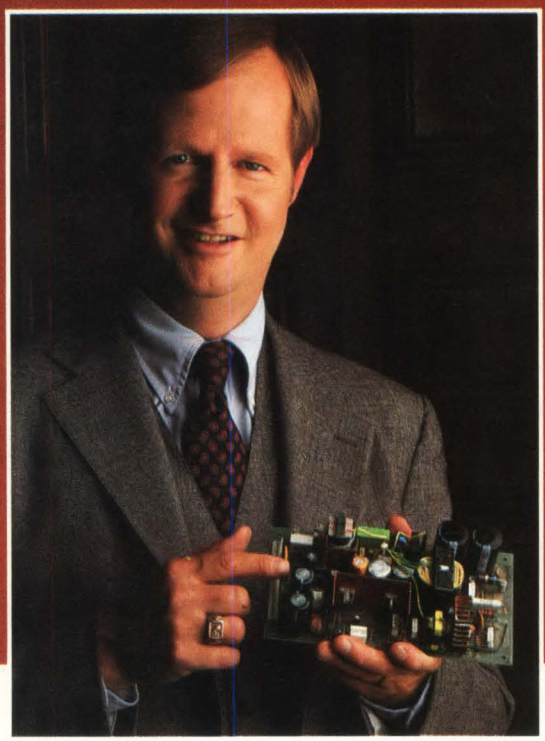

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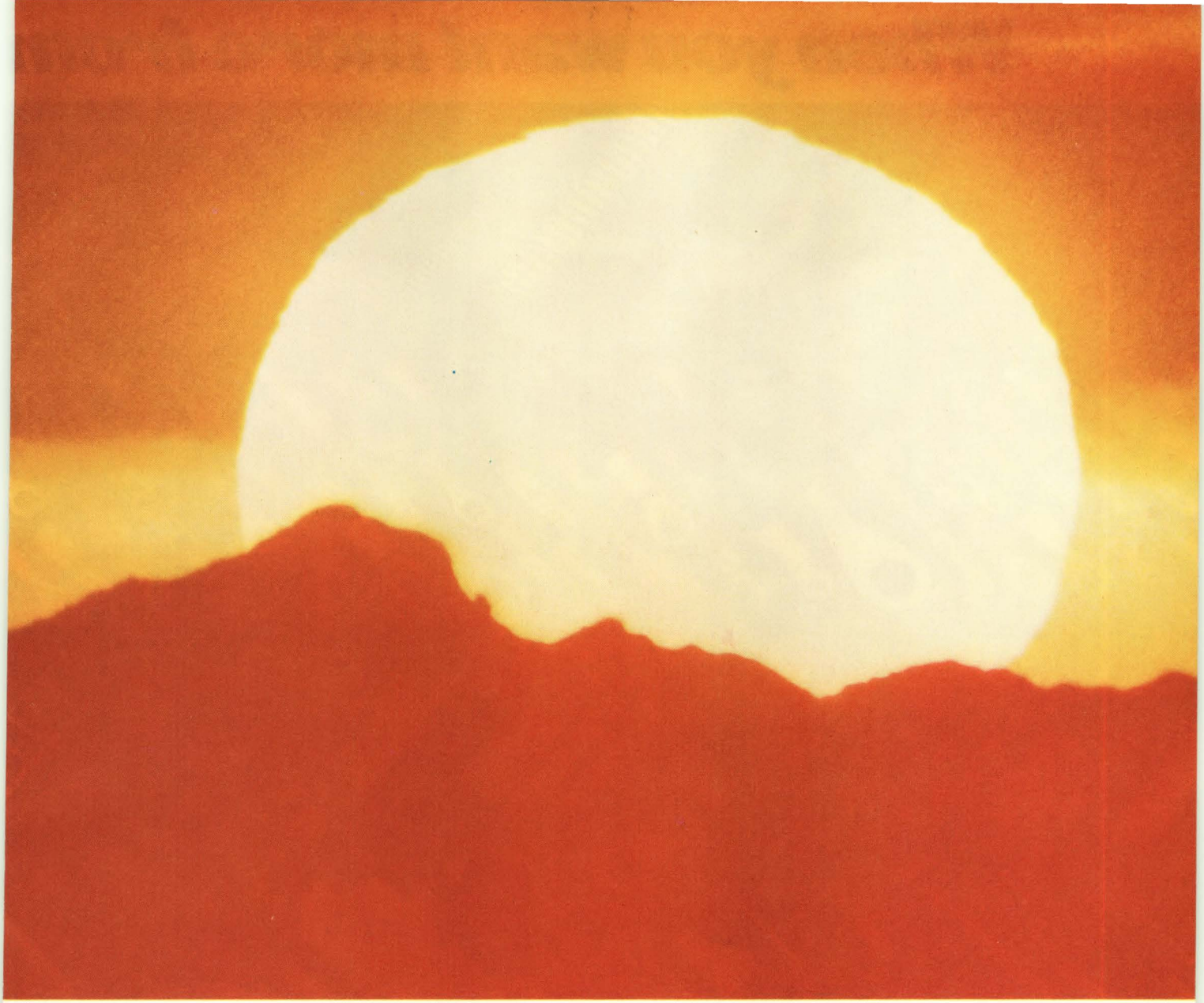

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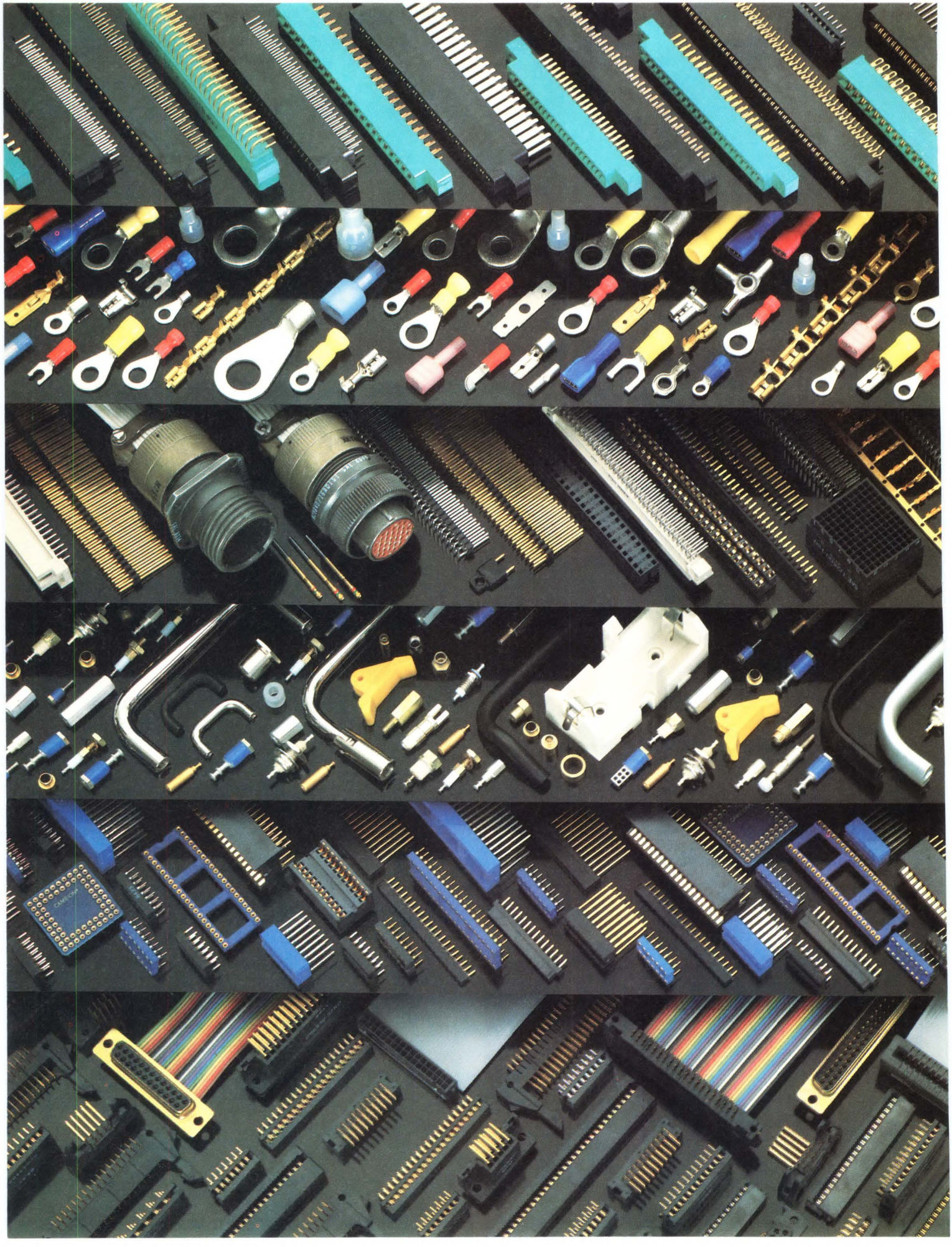

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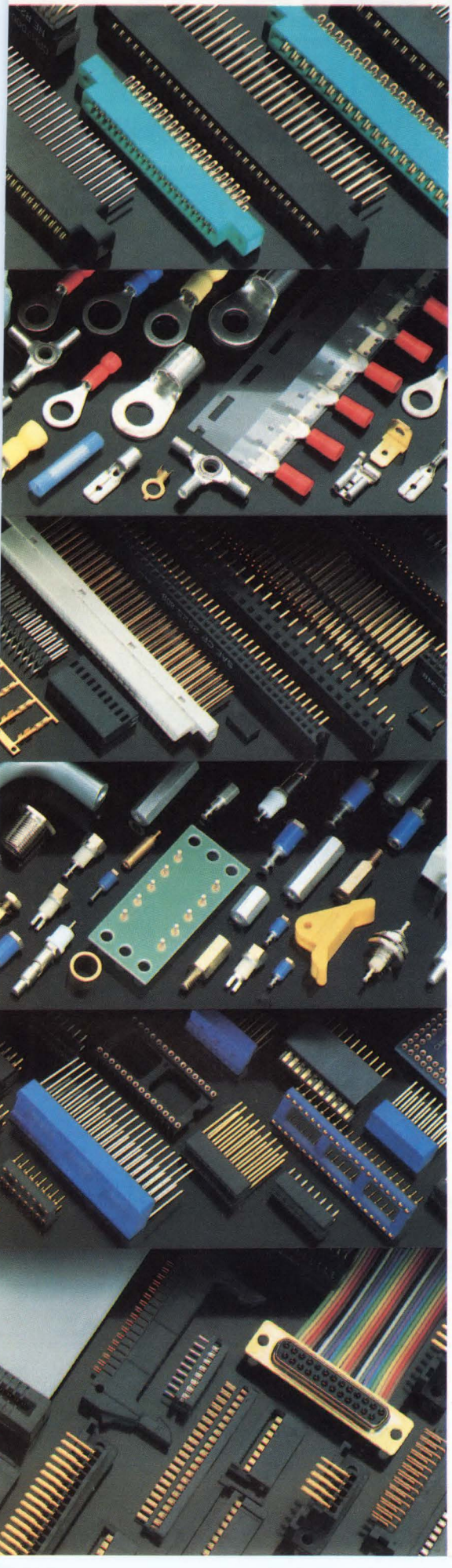

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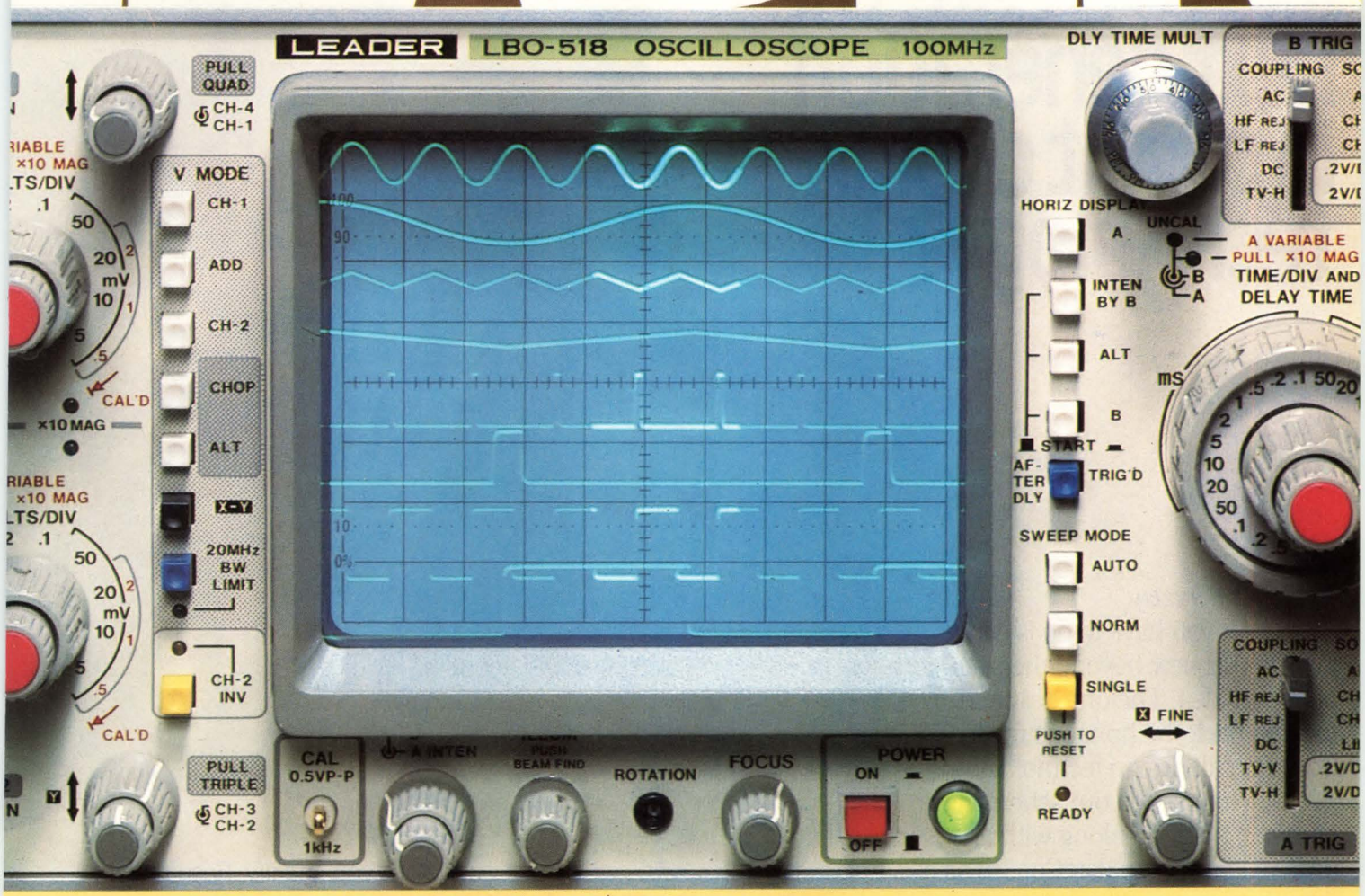

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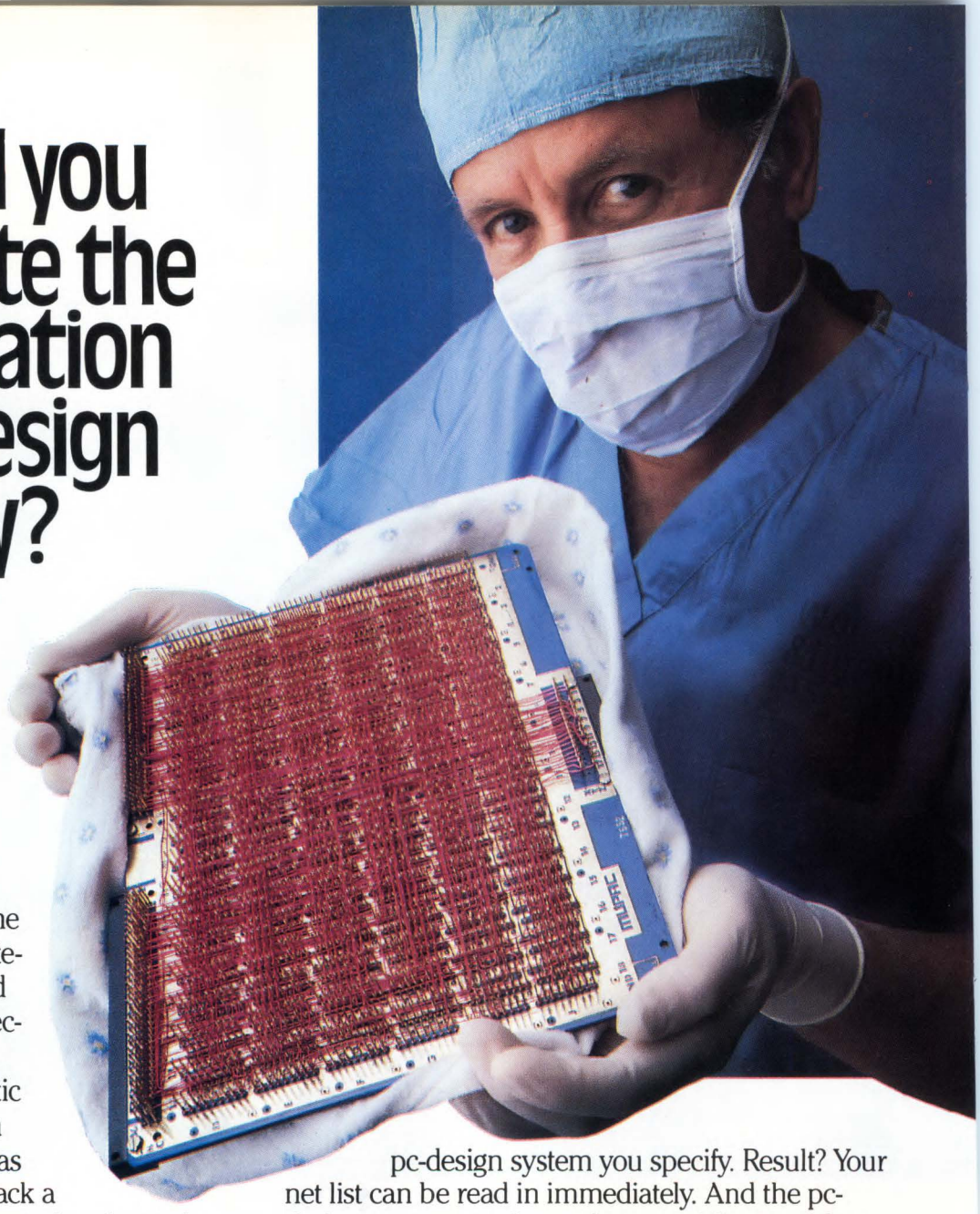

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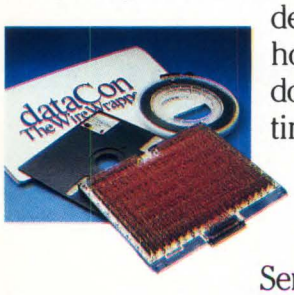

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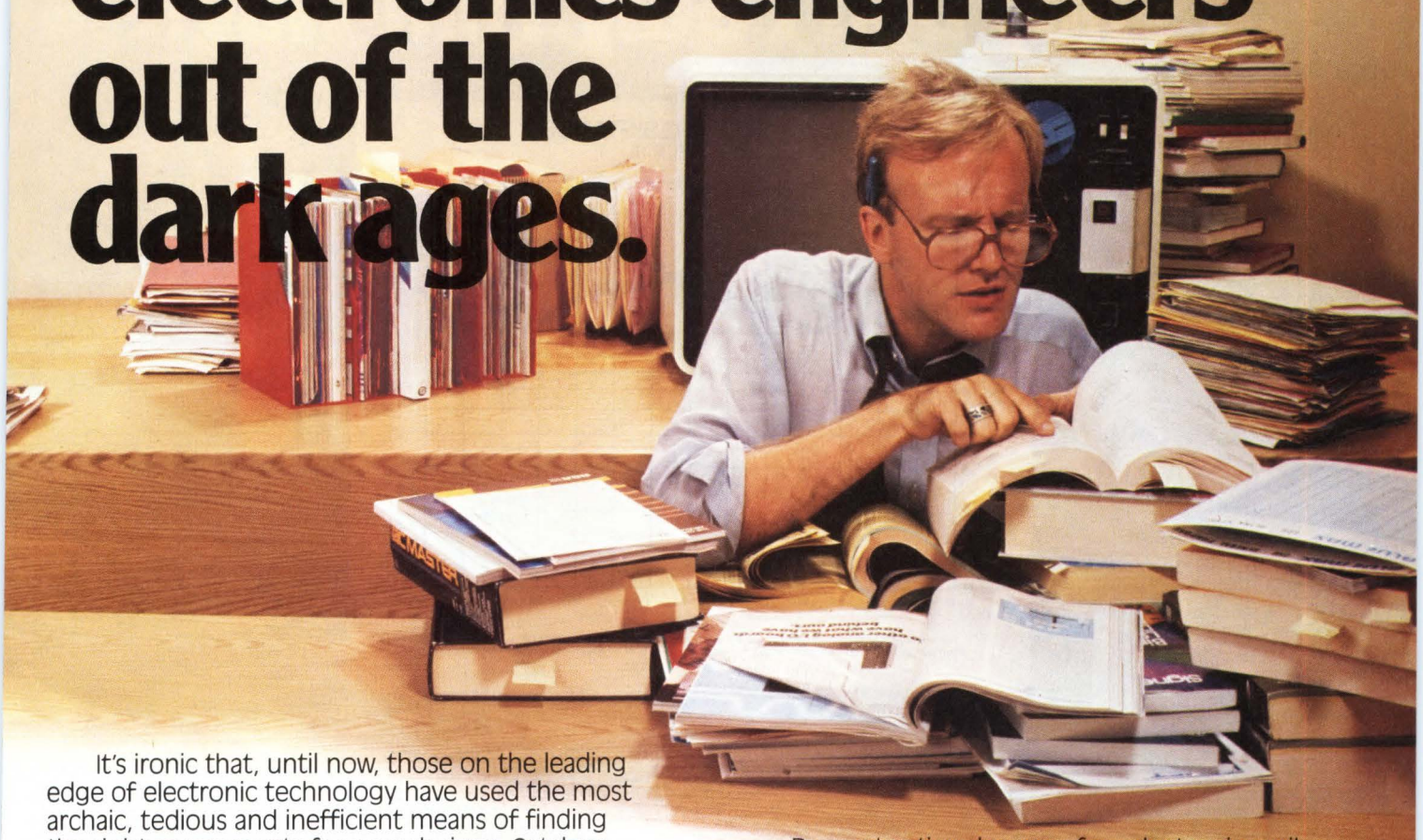

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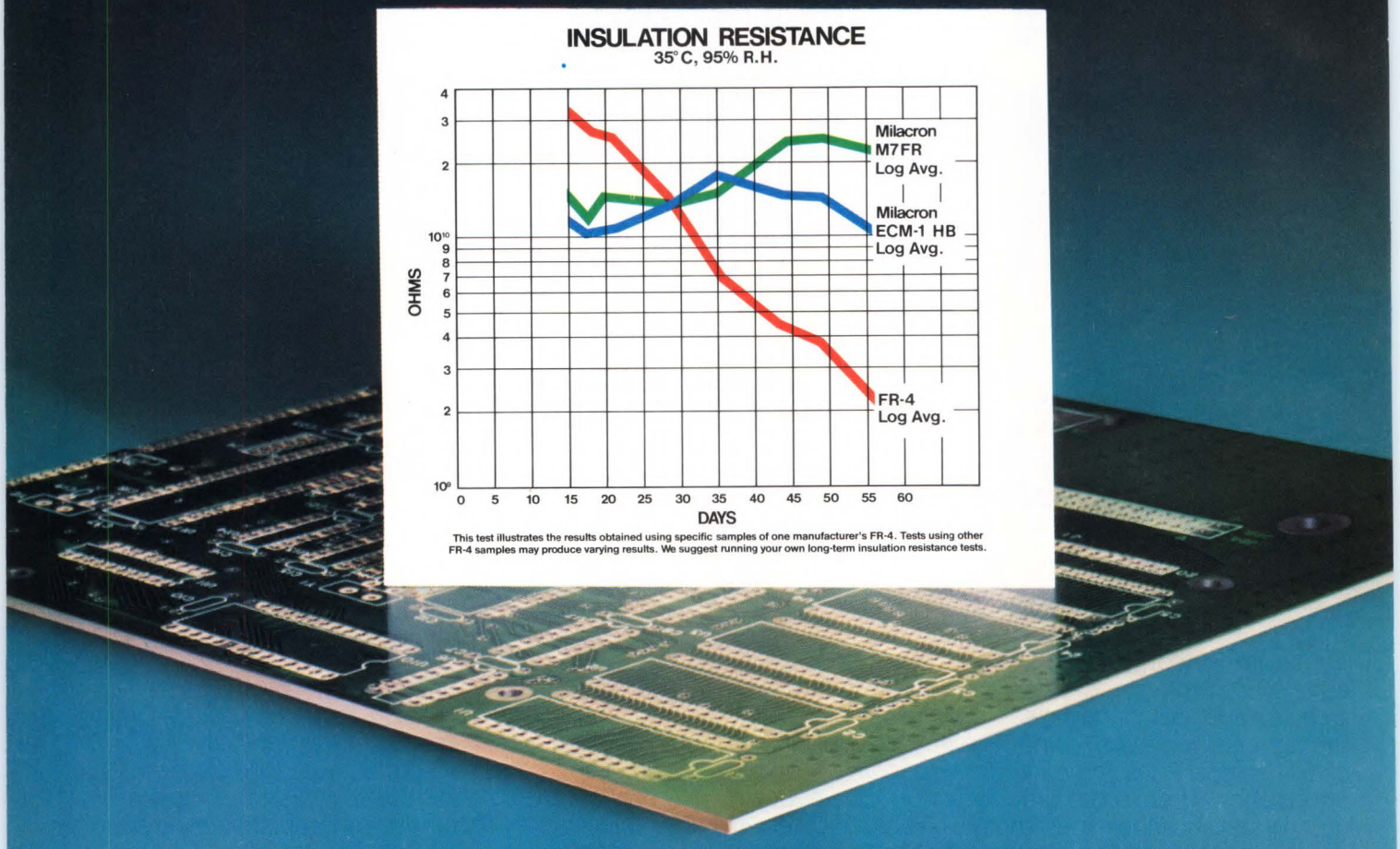

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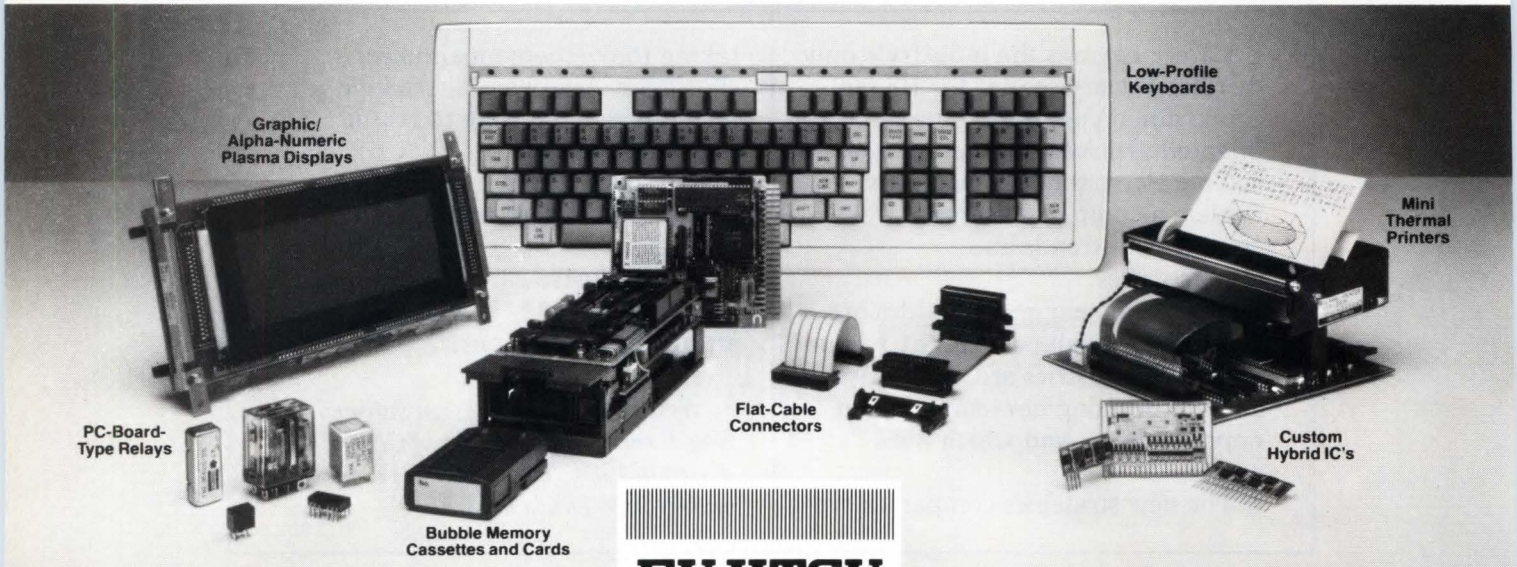

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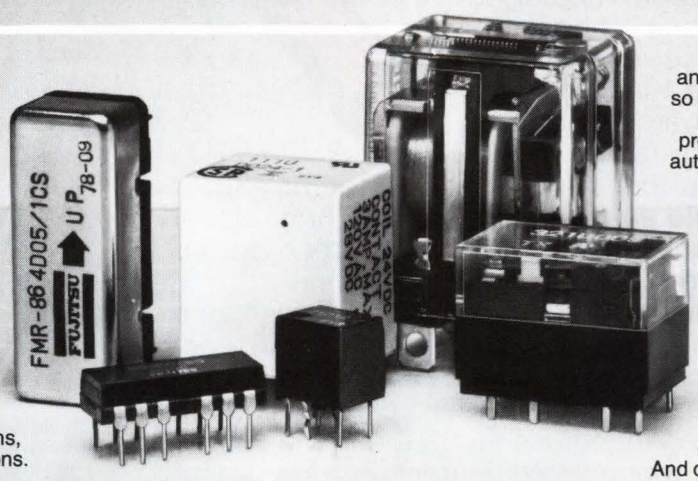

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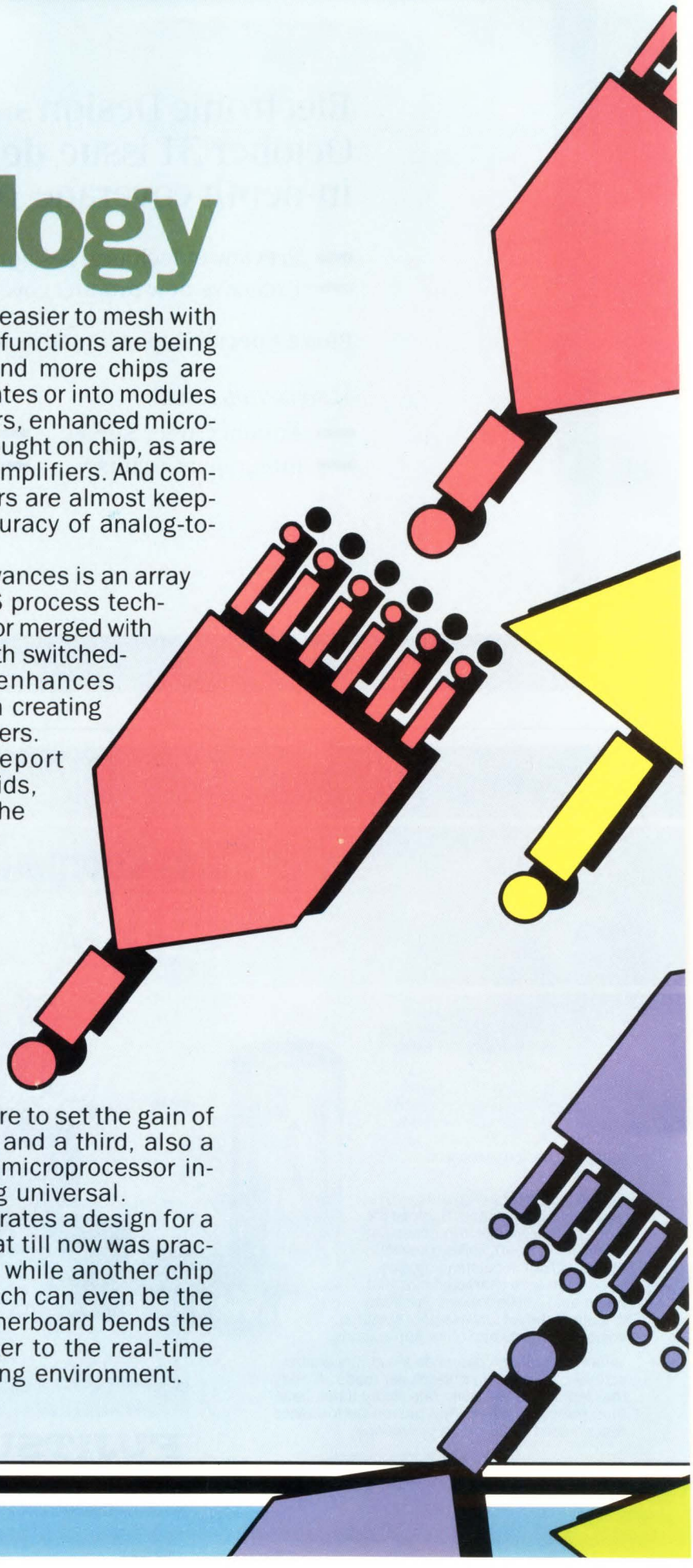
Analog Technology

Computing power has never been easier to mesh with the world of analog signals. More functions are being crammed into individual chips and more chips are being crowded onto hybrid substrates or into modules than ever before. In data converters, enhanced microprocessor interfaces are being brought on chip, as are filters and low-noise operational amplifiers. And companion sample-and-hold amplifiers are almost keeping pace with the speed and accuracy of analog-to-digital converter chips.

Underpinning most of these advances is an array of ever more sophisticated CMOS process technologies, either used on their own or merged with bipolar elements. Compatibility with switched-capacitor techniques further enhances the versatility of CMOS, notably in creating sampling digital-to-analog converters.

The following Technology Report discusses the latest chips, hybrids, modules, and boards to meet the digital needs of everything from graphics processors to panel meters. Then a half-dozen Design Entry articles home in on the newest advanced devices. Three of these involve analog-to-digital converters: a 10-bit device brings anti-aliasing filters on chip to increase the integration of analog subsystems; another attains a 20-bit dynamic range by using hardware rather than software to set the gain of its programmable gain amplifier; and a third, also a 10-bit device, boasts an on-chip microprocessor interface that comes close to being universal.

As for the others, one chip integrates a design for a voltage-to-frequency converter that till now was practical only in discrete device form, while another chip monitors five voltages, one of which can even be the ac line. Finally, an ingenious motherboard bends the power of a VAX superminicomputer to the real-time exigencies of the signal-processing environment.



TECHNOLOGY REPORT

Analog converters, sample-and-hold amps lead the way to a world of ideal design parameters

The system designer who works with analog-to-digital and digital-to-analog converters — and their sample-and-hold companions — may have found the land of milk and honey. They have access to alternatively sourced single-chip d-a converters that remain accurate to 12 bits even over the military temperature range. These are complemented by hybrid 12-bit a-d converters — with low chip counts — that do not miss any code over their operating temperatures. What's more, a single-chip device is on the way. To put the finishing touches on this earthly paradise, monolithic sample-and-hold amplifiers with a guaranteed accuracy of 12 bits are starting to arrive.

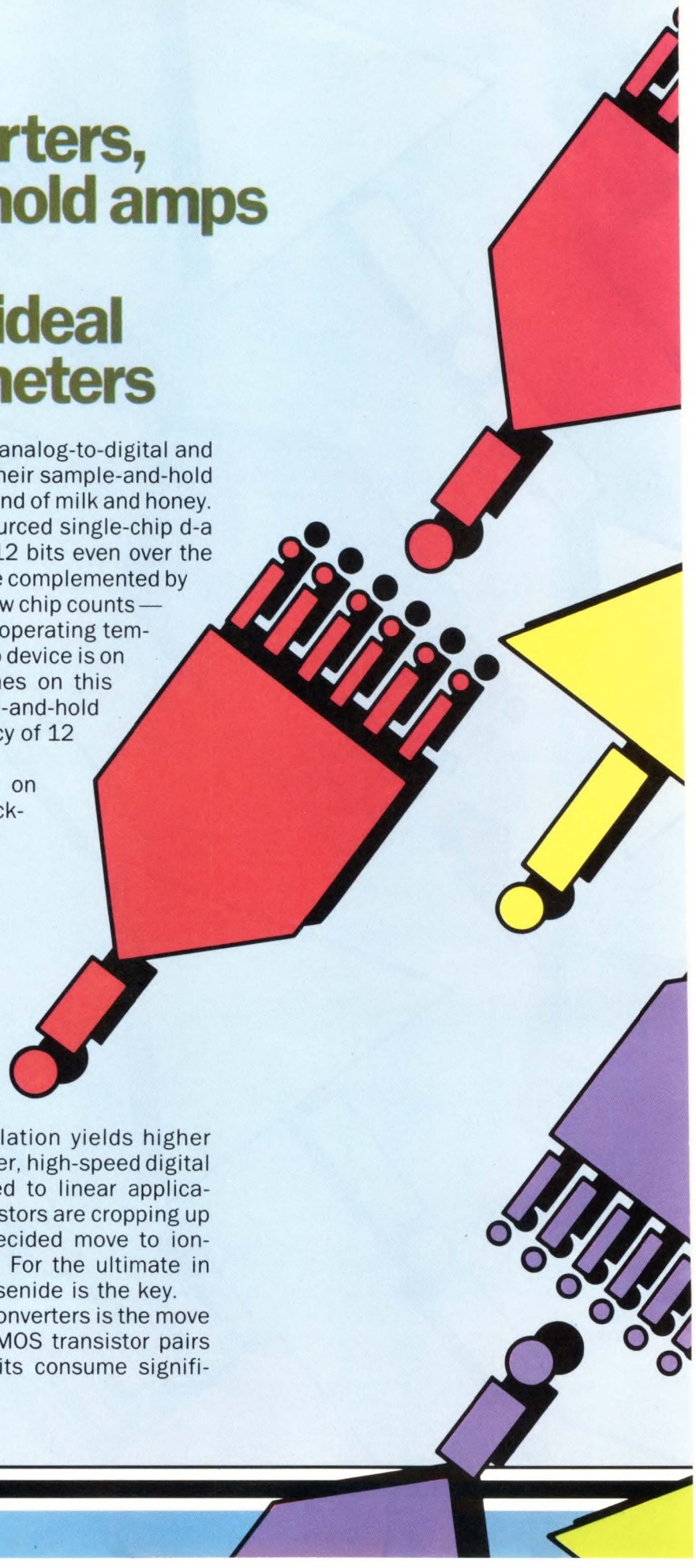
This brave new world is founded on three ideals: more functions to a package, higher performance, and the use of both CMOS and merged CMOS-bipolar processes.

The move to more functions takes into account four aspects of a designer's requirements: completeness, single-supply operation, versatility, and the need to house a number of similar chips in one package. The first two ensure that devices are easy to use. The second pair broadens a unit's range of functions.

The greater use of dielectric isolation yields higher speeds and lower bias currents. Further, high-speed digital bipolar processes are being adapted to linear applications. At the same time, thin-film resistors are cropping up in more settings, and there is a decided move to ion-implanted and polysilicon resistors. For the ultimate in converter speed, though, gallium arsenide is the key.

The main process trend in analog converters is the move to CMOS. As in the digital world, CMOS transistor pairs build dense logic, and CMOS circuits consume signifi-

FRANK GOODENOUGH



ficantly less power. Until recently, however, CMOS devices were limited to noisy op amps (with a tendency to drift), 8-bit a-d converters, and 12-bit current-output d-a converters with thin-film resistors. Although built without references, the last often demanded complex interface logic.

CMOS, in particular, puts switched-capacitor techniques into the designer's hands. It also makes possible a number of new converter architectures, as well as automatic zeroing and calibrating. It is found across the board, from slow dual-slope devices to flash converters and on to sample-and-hold and operational amplifiers.

The trend to CMOS is split along two paths: so-called linear processes, aimed mainly at building high performance chips, and merged processes that combine the best of CMOS and bipolar technologies (see "CMOS and Bipolar: The Twain Shall Meet," below).

CMOS and bipolar processes: The twain shall meet

Most bipolar processes build high-gain, fast npn transistors, as well as slow pnp transistors. These devices can be matched in pairs to furnish low offset, and their input noise is close to the theoretical minimum. Thus they create good op amps. Add ion implantation and they make JFETs possible. The processes also can fabricate low-drift buried zener references and band-gap references. Further, they can yield voltage-insensitive capacitors that serve for stabilizing amplifiers and act as the hold capacitor in sample-and-hold amplifiers. Despite all that is in their favor, though, they make very poor analog switches and do not lend themselves to low-power logic that is both dense and fast.

CMOS processes, on the other hand, build good analog switches, good capacitors, and very dense logic. In addition, they can create npn transistors, which can be employed as emitter followers.

Initially, CMOS transistor pairs were noisy and difficult to match. Also, their offset voltages changed over time, at different temperatures, and with varied input voltages—significantly more than that of bipolar transistors. However, by changing from metal-gate to silicon-gate CMOS, and through innovative circuit design, analog circuits fabricated with CMOS transistors are approaching and may equal the performance of circuits based on bipolar transistors.

As a result, two strong trends are emerging: a move to silicon gate and a shift to merged CMOS-bipolar technologies for fabricating high-performance converters and other analog chips. Two other secondary, or support, processes should be mentioned, since they also improve the performance of converter circuits—dielectric isolation and thin-film resistors. The first adds speed by minimizing parasitic and coupling capacitances, and it also minimizes leakage current to the substrate for op amp inputs. Thin-film resistors make possible on-chip precision to 16 bits. Since both are compatible with CMOS and bipolar technologies, they are either being incorporated into existing processes or considered for future ones.

More functions to the package save space and design time

Driven hard by the cost of design, testing, and assembly time, as well as by the price of pc board real estate, the number of functions squeezed into a single package is rapidly increasing. That rise holds true even if the package contains a single chip, is a multichip hybrid (holding from two to dozens of components), or is itself a module.

Importantly, in most cases, neither the package size nor the number of chips or devices in a housing is climbing with the increase in functionality. There are three reasons for this: For one thing, packages can hold even the largest chips. Second, hybrids are taking advantage of the boost in functionality to be seen in standard and semicustom ICs. Finally, modules and boards are themselves using specially constructed hybrids.

The move to more complete devices dominates the world of converters, with versatility running a close second. In comparison, the trend toward mounting multiple identical devices in a package and the ability to operate from a single power supply are just beginning to show up. Nonetheless, whether discussing the increase in functionality of a particular device or a greater number of devices in a package, such improvements always start with 6- and 8-bit devices and then move on to higher-resolution converters.

The past year has seen the arrival of a variety of digital-to-analog converters that are true portents of the future. For example, the first monolithic 8-bit quad d-a converter appeared (Fig. 1). The AD7226, from Analog Devices Inc. ((Norwood, Mass.) is fabricated in CMOS. Additionally, the set of latches on its eight inputs and on its 2-bit address word both crams the chip into a 20-pin DIP and simplifies the interface to virtually any microprocessor.

Like most CMOS converters, the quad chip has no reference. However, the linear CMOS process with which it is built uses the substrate npn transistor common to all MOS transistor processes to supply each converter with an output op amp that sports a bipolar output stage. The converter also exemplifies the trend toward single supplies, although a split supply improves performance when the output voltage is close to zero. The coming year should welcome several other chips with similar capabilities, including one from Precision Monolithics Inc. (Santa Clara, Calif.).

Harnessing hybrids

Designers who need to put more general-purpose 12-bit (rather than 8-bit) d-a converters in less space must go with hybrid units. One such device is Analog Devices' AD390, which squeezes four 12-bit converters into a 28-pin double-width (0.6-in.) DIP. Its single set of 12 digital inputs is more versatile than the 7226's. Each of the package's four d-a chips is an AD567—a current-output 12-bit device with a pair of cascaded input latches. The use of cascaded latches in the hybrid illustrates the way that double buffering permits several converters, riding a common bus, to be sequentially loaded with data (into the first latch) and have their outputs change simultaneously when the four new words are concurrently strobed into the second set of

latches. The quad converter is also complete with a reference, and an op amp is connected between each 567 and its output pin.

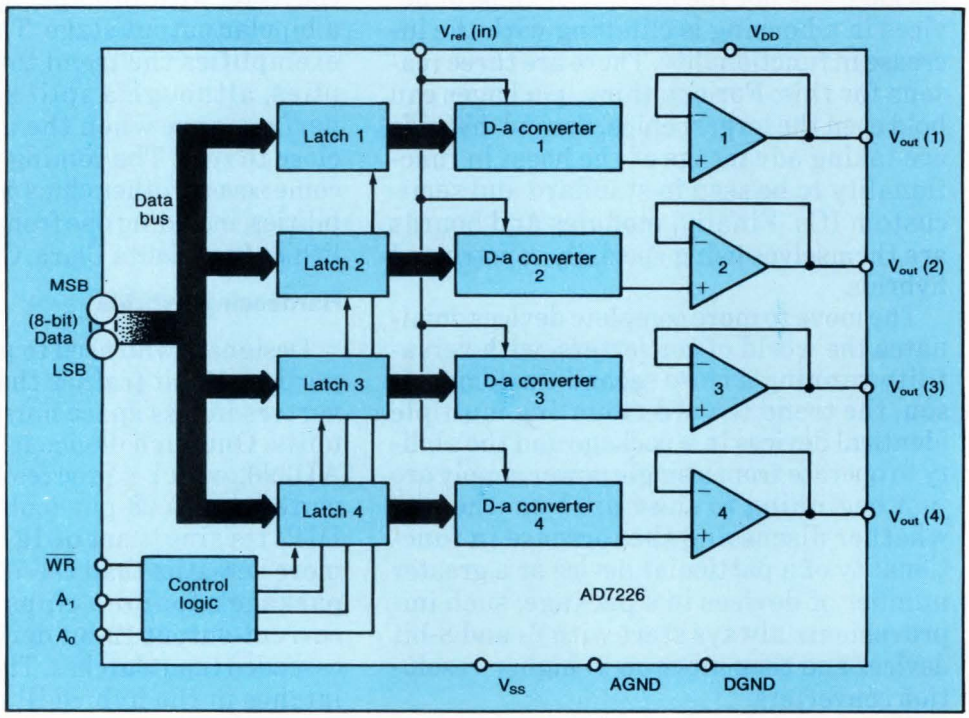
Just how the number of d-a converters housed in a DIP will rise is interesting: Not only will there be more chips in each hybrid, but there will also be more converters to a chip. In fact, a monolithic dual 12-bit converter is expected within a year. Made possible by dense CMOS logic, it will be a referenceless current-output device.

Flexible inputs

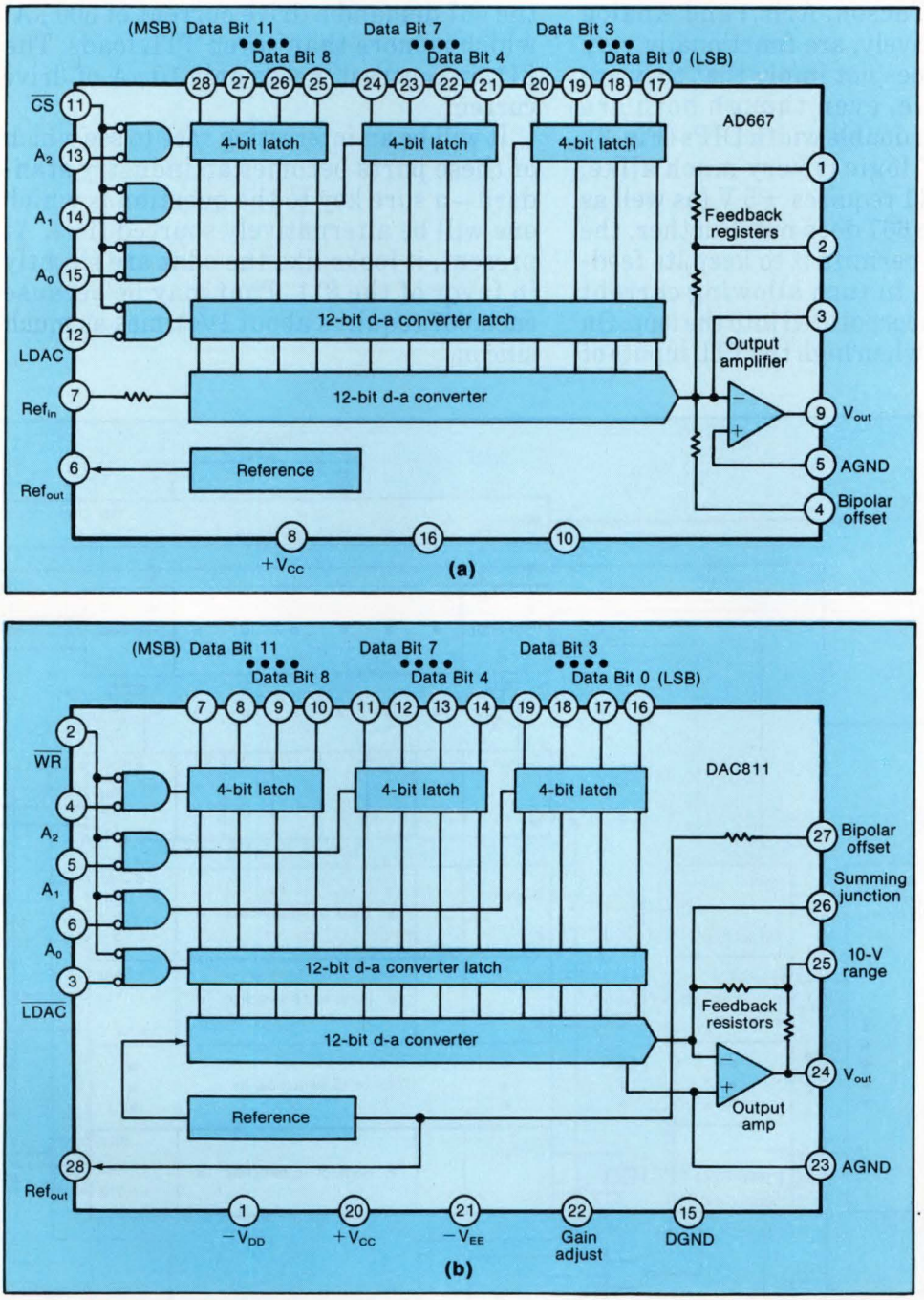
The ultimate versatility for a d-a converter's input logic combines double buffering with the ability to take an input word in two or more subwords (bytes or nibbles), allowing connections to be made to a host of microprocessor buses. For example, the 567's architecture takes input words in any combination of left- or right-justified nibbles (MSB or LSB first). If connected to a 12-bit bus, it can handle all 12 bits at once, as can the AD390. If linked to an 8-bit bus, it first accepts the 4 MSBs and then the 8 LSBs (or vice versa). On a 4-bit bus, the data word is read in three sequential nibbles.

The 567 and a referenceless CMOS partner both lack output op amps. But units with such op amps are not unavailable. Bursting on the scene early this year, virtually simultaneously, came a pair of one-chip voltage output devices (ELECTRONIC DESIGN, March 8, 1984, p. 197, and March 22, 1984, p. 262).

The DAC811 and the AD667, from Burr-



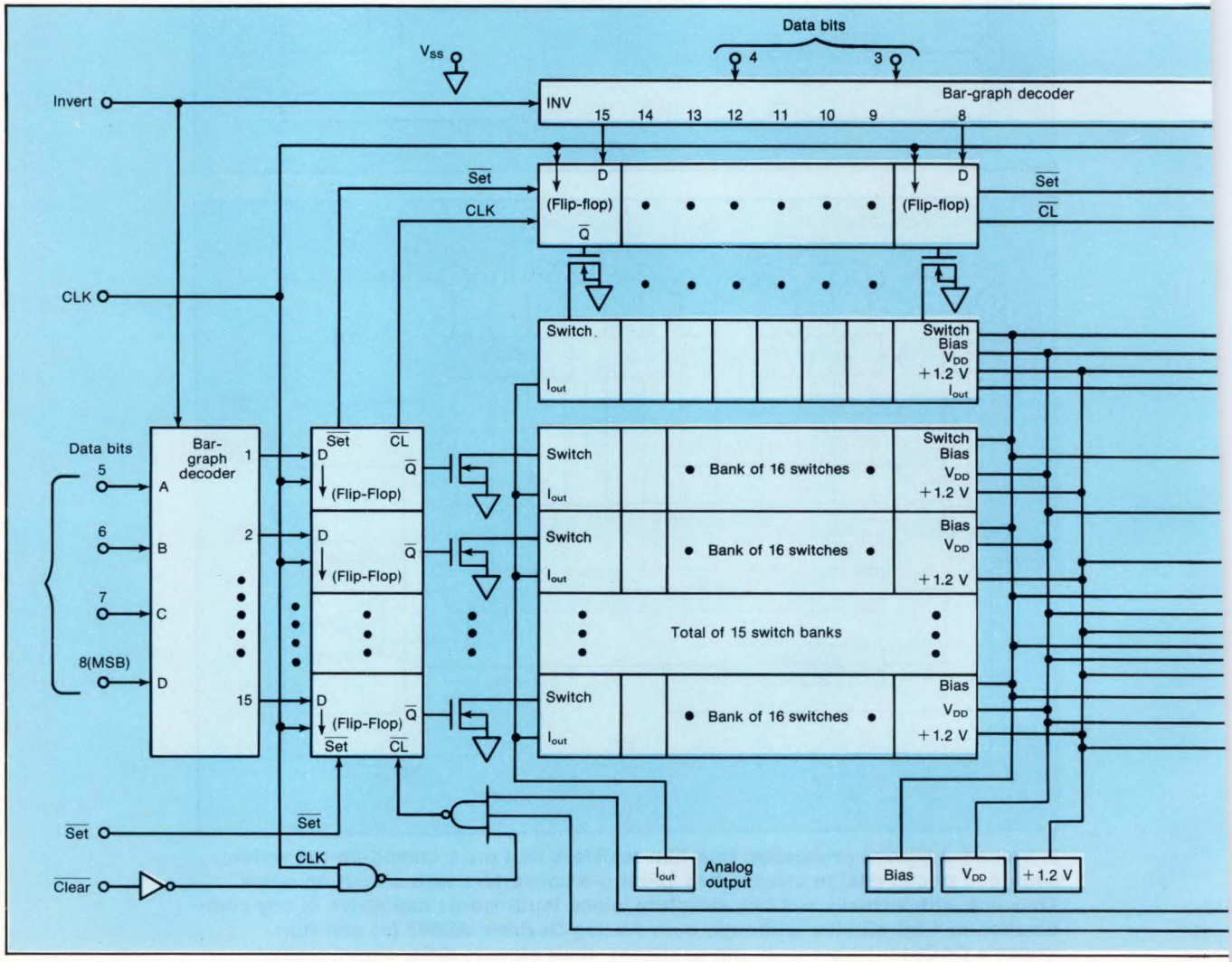
1. Four d-a converters are squeezed into a 20-pin DIP. Moreover, these 8-bit chips from Analog Devices ensure a true voltage output. The AD7226's ability results from an advanced linear CMOS process combined with an innovative circuit design, including reverse-connected d-a converters buffered by voltage-output op amps. The process permits the substrate npn transistors to be used as the amplifier output transistors and also builds the dense logic required for bus data inputs.



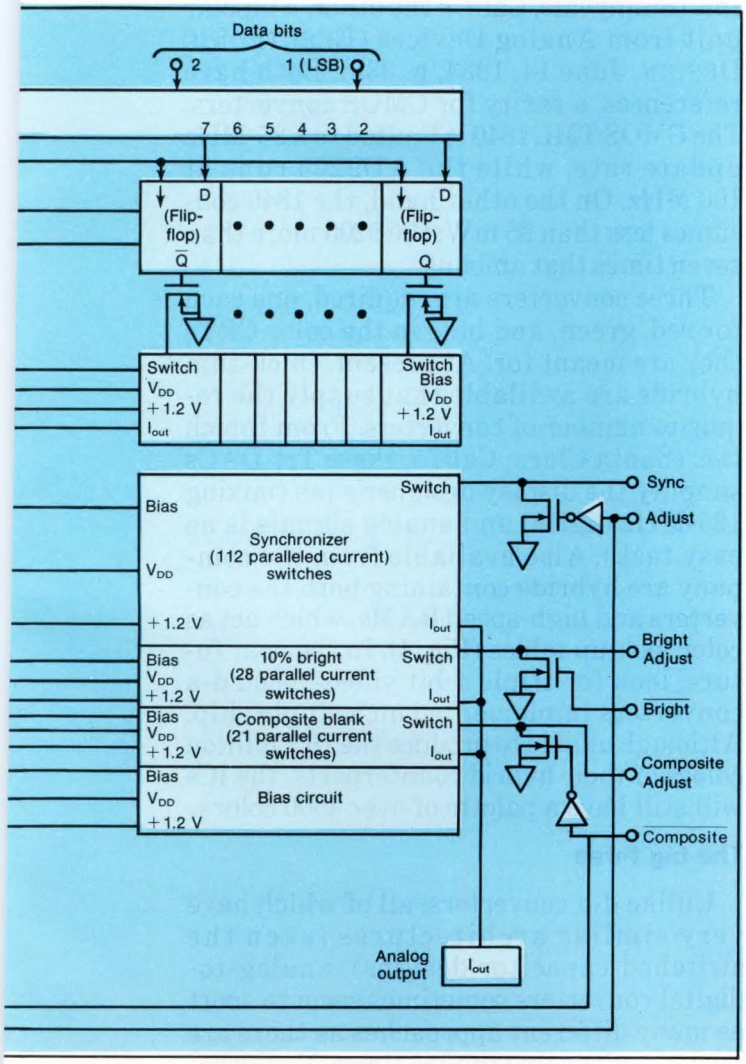
2. Standard bipolar processes, thin-film resistors that are trimmed on the wafer, and good circuit design creates two 12-bit d-a converters with output op amps. They link with virtually any bus structure, since input words can arrive in any combination of 4-bit nibbles. Although both Analog Devices' AD667 (a) and Burr-Brown's DAC811 (b) are in 28-pin packages, their pinouts differ significantly.

Brown Corp. (Tucson, Ariz.) and Analog Devices respectively, are functionally very similar. That does not imply that they are pin-compatible, even though both are housed in 28-pin double width DIPs (Fig. 2). The two chips' logic is very much alike. However, the 811 requires +5 V (as well as ±15 V) and the 667 does not. Further, the 667's extra pin permits it to keep its feedback loop open, in turn allowing current boosters to be incorporated into the loop. On the other hand, when high the TTL inputs of the 667 demand a drive current of 300 μA, which is more than seven TTL loads. The 811, in contrast, needs only 10 μA of drive current.

It will be an interesting race to see which of these parts becomes an industry standard—a sure key to the question is which one will be alternatively sourced first. At present, it looks like the odds are slightly in favor of the 811. That may be because each 667 requires about 1½ times as much silicon.



Several monolithic 14-bit CMOS d-a converters, without references or output op amps, can be had with double buffering. At 16 bits, a two-chip double-buffered hybrid supplies a simple microprocessor interface. (In large volumes, a two-chip hybrid built on an automated assembly line costs only a little more to put together than a one-chip device.) From Burr-Brown, the hybrid comprises an analog 16-bit d-a converter and a gate array. It comes in two versions: the DAC709 voltage-output unit and the DAC708, current-output unit. Both are mounted in double-width 24-pin DIPs and accept data in two bytes (ELECTRONIC DESIGN, March 8, 1984, p. 141.) In addition, to minimize the number of interface lines, both can take in the input word one bit at a time. The serial input also permits simple opto-isolation between digital inputs and analog outputs.



Double the buffer

Also pointing the way to 16 bits is a single-chip multiplying d-a converter with double buffering and a voltage output. Fabricated with a new high-performance bi-MOS process, it uses a pair of cascaded resistor strings in a circuit somewhat similar to a Kelvin Varley divider. Since the AD569, from Analog Devices, is a multiplying converter, it does not contain a reference. That is not much of a surprise, though, since building a reference stable enough to maintain 16-bit accuracy over temperature is no mean feat—even on its own chip—let alone putting it on a complicated monolithic chip, along with a variety of other digital and analog circuits (ELECTRONIC DESIGN, June 14, 1984, p. 273).

A ticket to ride

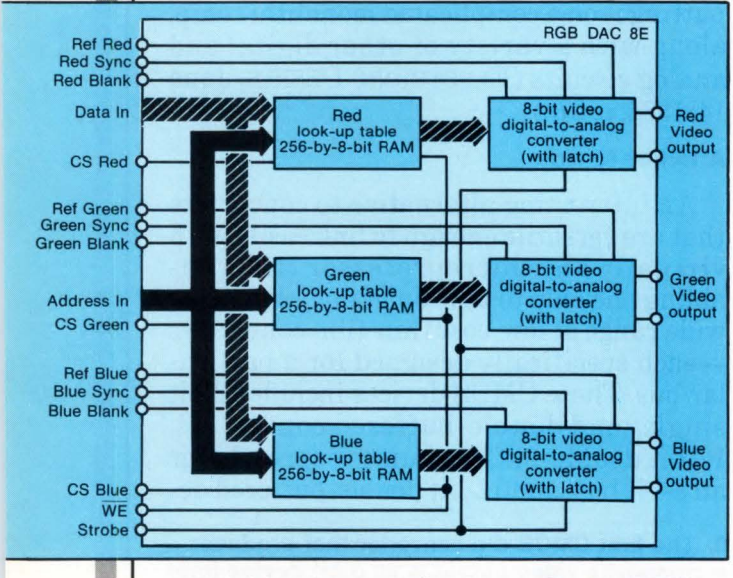
An interesting alternative to converters that are versatile enough to link easily with virtually any microprocessor (thus enabling one chip to take on many jobs) is the wide range of low-cost thin-film converters —each specifically designed for a particular bus. These CMOS devices include 12-bit single- and double-buffered converters, 12-bit double-buffered units expressly for an 8-bit bus, and 12-bit double-buffered de-

3. The first CMOS d-a converter that produces a composite video output is an 8-bit device from Telmos that operates at up to 25 MHz. Its architecture takes advantage of the high packing density of CMOS to use bar-graph decoding. It employs over 256 current sources to ensure monotonicity and to minimize glitches.

vices with a serial input.

Another peek into the future reveals that 12-bit CMOS d-a converters with references and output op amps—some chopper-stabilized at that—will be on the scene within a year. The same period should also see some 12- to 16-bit devices with deglitching circuits built into the op amp.

The drive for better and lower-cost color graphics has—over the past five years—seen video speeds jump from 20 to 125 MHz and d-a converters move from modules, through thick-film hybrids, to CMOS and bipolar ICs. These 4- to 8-bit devices produce a composite video signal that is compatible with international standards RS-170 or RS-343. Virtually all of them use a single input buffer register to minimize the glitches caused by time skews in the arriving information. When all the digital data has been received, the latches are strobed and the analog output changes cleanly.



4. Hybrid technology shoehorns three 100-MHz d-a converters and three high-speed 256k-by-8-bit RAMs in a single package only 2 in. square. The result is Intech's color-mapped red-green-blue composite video converter that can paint over 16 million colors on a raster-scan CRT.

Additional digital inputs produce outputs such as a full-scale reference white, whiter than white, and blacker than black. The first single chip for the job arrived about a year ago. A bipolar device, the TDC1018 from TRW Inc. (La Jolla, Calif.) lacks a reference. However, it operates at 100-MHz word rate.

Two on the town

Two additional 8-bit chips have made their debut within the last three months. One is a CMOS device (Fig. 3), from Telmos Inc. (Sunnyvale, Calif.); the other, a bipolar unit from Analog Devices (ELECTRONIC DESIGN, June 14, 1984, p. 332). Both have references, a rarity for CMOS converters. The CMOS TML 1840 is limited to a 25-MHz update rate, while the AD9200 runs at 100 MHz. On the other hand, the 1840 consumes less than 85 mW, the 9200 more than seven times that amount.

Three converters are required, one each for red, green, and blue in the color CRTs they are meant for. At present, thick-film hybrids are available that supply the requisite number of converters. From Intech Inc. (Santa Clara, Calif.), these Tri-DACs simplify the display designer's job (mixing 125-MHz digital and analog signals is no easy task). Also available from the company are hybrids containing both the converters and high-speed RAMs, which act as color look-up tables (Fig. 4). In the near future, look for triple 4-bit video-speed d-a converters implemented on a single chip. Although unable to produce the 16.7 million colors of their hybrid counterparts, the ICs will still have a palette of over 4000 colors.

The big three

Unlike d-a converters, all of which have very similar architectures (even the switched-capacitor designs), analog-to-digital converters sometimes seem to sport as many different approaches as there are trick circuits using the 555 timer. Neverthe-

less, three designs dominate—and a fourth is coming on fast. The major three are the usually slow multislope integrating converter, the general-purpose midspeed successive-approximation converter, and the typically high-speed flash converter. The relative newcomer (dubbed, for want of a better name, the multistep converter) puts two or more of those three basic circuits to work in sequence.

For example, to build a 10-bit multistep converter, a 4-bit flash converter might handle the 4 MSBs and could be followed by a 6-bit successive-approximation circuit. Currently, converters using this architecture run the gamut from chips to boards and use a pair of flash circuits or employ the same flash twice. Mixed pairs, like the aforementioned, and designs using more than two steps are being reinvestigated for the future.

Increased functionality dominates the realm of a-d converters as much as it does that of d-a converters. In a general sense, it does so in much the same way; more analog capability on the input and more digital capability on the output.

Come the evolution

The increase in digital ability has been evolutionary, as it has in its d-a counterparts. Fueled by advances in microprocessors, the movement has been from plain TTL outputs, through three state outputs, up to multibyte outputs. The last reduces the number of lines and pins and simplifies the interface with microprocessor buses.

In addition, control circuits have been developed that minimize bus-access time (the time needed to transfer data to a bus when a conversion is complete). Also, clock circuits have been added to converters. They may prove to be an anachronism, though, since devices are now used with a microprocessor or a microprocessor-based system and must be synchronized with the system clock. What's more, the outputs of integrating converters aimed at digital panel meters and digital voltmeters have moved from BCD-encoded outputs to multiplexed lines for driving seven segment displays.

In a sense, as sample-and-hold amplifiers are showing up on their front ends, a-d converters are finally becoming true sampling devices rather than just encoders or digitizers. This revolutionary increase in functionality is found in chips, modules, and boards and is the result of many interrelated causes. The basic motivating factor is that if the input to an a-d converter changes during a conversion, regardless of its architecture (even if it is an integrating or a flash device), an error may occur. The right sample-and-hold amplifier in front of it, though, eliminates the problem.

Coming soon

In the near future, hybrid technology will wed a 574 with a sample-and-hold amplifier—all in a 574 package and pinout. Following it in a year or so, using merged processes, a single-chip device can be expected.

Nonetheless, as the speed and resolution of converters climb, the capability of these sampling amplifiers has not risen at the same rate. Rather, it has remained the weak link in sampled-data systems. Moreover, optimizing the performance of a high-speed or high-resolution converter, or both, with a companion sample-and-hold amplifier (if one can be found) is not easy: Timing and wiring are critical. In high-speed, high-resolution, two-step converters, incorporating a sample-and-hold amplifier is mandatory, since the input must remain constant throughout the conversion.

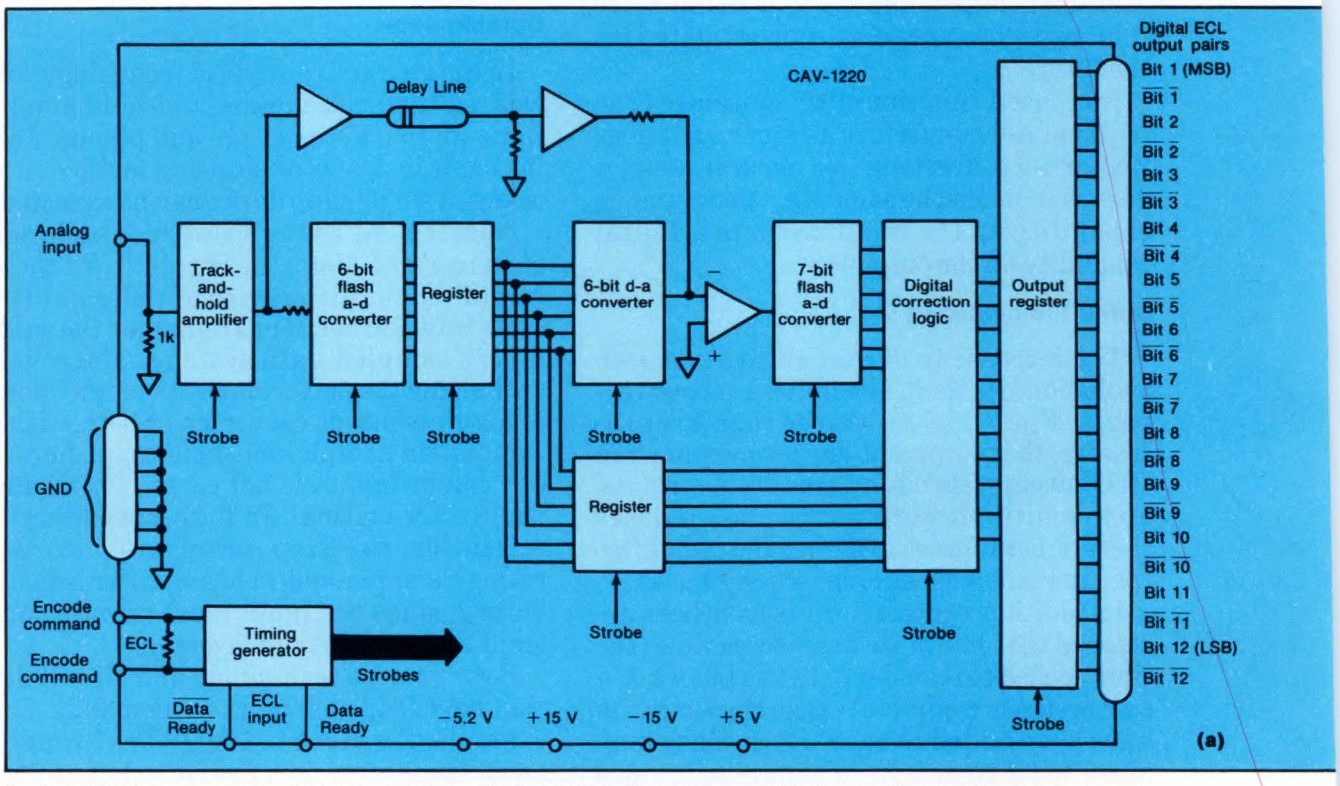
Both process technology and circuit design have helped meet these demands. For example, the move to CMOS has brought about converters using switched-capacitor circuits that in many cases inherently supply the ability to sample and hold signals.

Building an a-d converter that is truly accurate to 16 bits is no easy task. Demanding

that it first sample a signal to that accuracy in under 1 μs and then carry out a conversion in under 2 μs only complicates matters. Yet that is exactly what the Adam-826 from Analogic Corp. (Wakefield, Mass.) can do, with a throughput of 435,000 conversions/s. The module, which stands 3.0 by 5.0 by 0.44 in., adapts to various bus interfaces by using three-state outputs. Its performance is attributable to innovative circuit design, which employs precision, high-speed discrete devices.

Indicative of the need for these 16-bit sampling converters (and ones that work at 14 and 15 bits, regardless of their speed) is a trio of 16-bit modules from Analog Devices. The throughput of the DAS1157, DAS1158, and DAS1159 (14 to 16 bits) may only be 18 MHz, but on the other hand their maximum power consumption is just 650 mW. (Adam, for instance, needs about five times that.) The low power draw is achieved with CMOS thin-film d-a converters. Two sets of three-state output buffers allow data to be taken either in one byte or in two.

The two-step converter, probably more than any other type, demands a sample-and-hold amplifier ahead of it, since the only reason for its existence is speed. An example of such a device is a member of a family of board-level converters. The CAV-1210 (Fig. 5a), from Analog Devices, is about 5 by 6.5 in. and combines two flash-converter stages, a d-a converter, an error amplifier, and several other components in a manner that allows the second (7-bit) stage to cor-



5. A multistep circuit architecture is the design of choice when resolution and speed must be wed in an a-d converter. It uses one or more flash a-d converters, as well as d-a converters. Some multistep circuits like Analog Devices' CAV-1220 (a) and Micro Networks' MN5245 (b) use digital correction logic to ensure accuracy. The board-level CAV-1220 supplies 12-bit digital words at a 20-MHz rate; the MN5245, a hybrid, the same number of bits at over 1.1 MHz.

rect for inaccuracies in the first (6 bits).

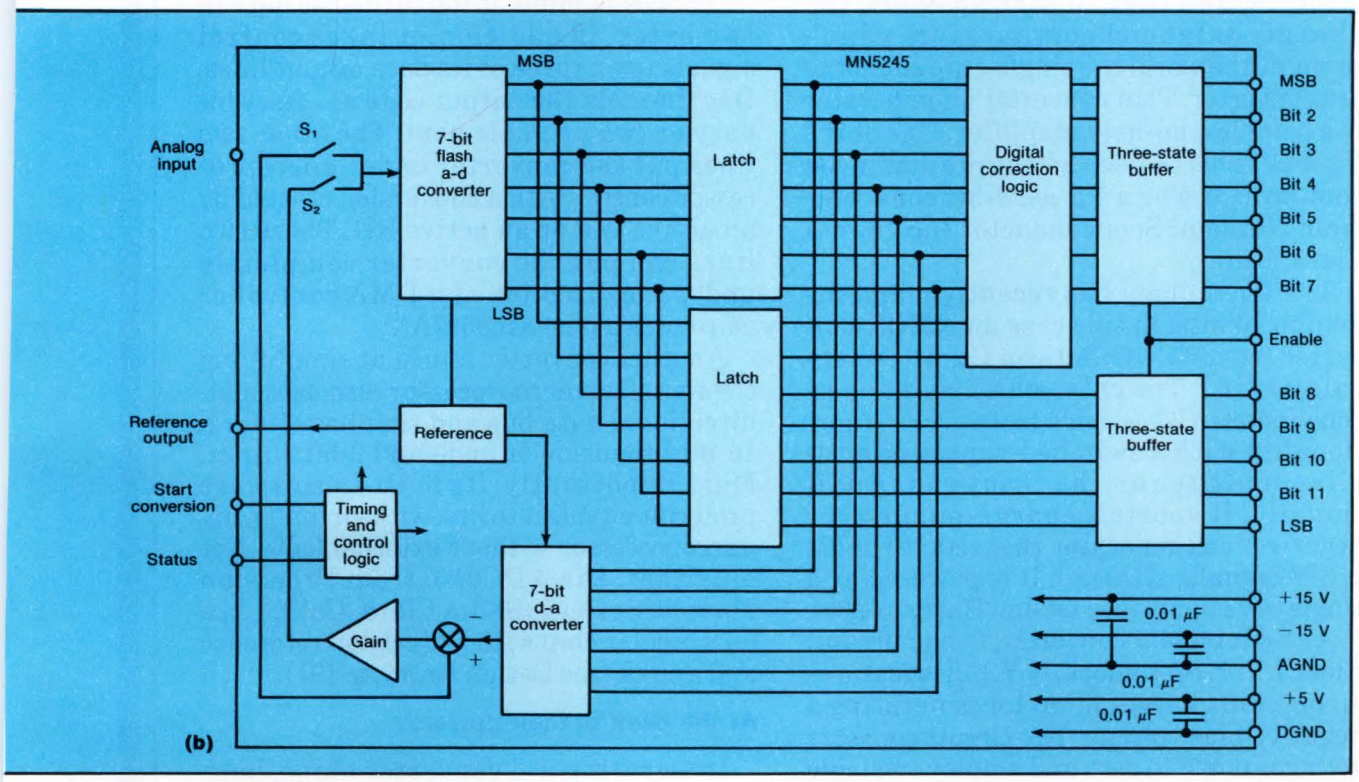
The analog input is digitized by the first stage, and 6 bits of digital information are applied to the digital correction logic circuits. They will eventually become bits 1 through 6 of the output. These same bits are also reconstructed as an analog signal in the 6-bit d-a converter and subtracted from the original input. The difference between the two is an error signal that is amplified and applied as an analog input to the second flash converter.

If both stages and all components were perfect, another 6-bit converter could be used for the second stage. The two outputs could then be added for the desired 12-bit output. Digitally corrected subranging takes the imperfections of the practical world into account by resolving the error signal, instead, into seven bits.

The seventh bit

The additional bit ensures that the output is twice as accurate as would have to be if every part were flawless. The digital correction logic can then use the output to compensate for various errors in the first stage, the d-a converter, the internal track-and-hold amplifier, and the difference amplifiers.

The value of the MSB of the 7-bit output determines whether the 6-bit output of the first stage is passed as is or if 1 should be added to it. Bits 2 through 7 of the second stage become bits 7 through 12 in the output of the CAV-1210's a-d converter. In the next



6 to 18 months, this approach should yield a 40-MHz 10-bit sampling converter and a 20-MHz 12-bit unit.

The same technique—in hybrid form—will be used to build families of general-purpose sampling converters with resolutions from 12 to 16 bits and conversion times in the submicrosecond range. In many cases, they will use a simpler form of digitally corrected subranging, with a single flash converter used twice. Such an approach is taken in the MN5245 from Micro Networks (Worcester, Mass.), which adds a sample-and-hold amplifier to the device's front end (Fig. 5b).

Turn, turn again

CMOS made possible switched-capacitor circuits, and they in turn spawned the charge-balanced comparator, which brought the world the single-chip sampling a-d converter. That converter's comparator is a sample-and-hold amplifier. One of the first devices to use the charge-balanced comparator was a 1.5-μs, 8-bit converter from National Semiconductor Inc. (Santa Clara, Calif.).

The technology has recently made the leap to 10 bits, in this case an NMOS converter from EG&G Reticon Corp. (Sunnyvale, Calif.). The chip, which performs a conversion in 24 μs, adds to its overall functionality with a switched-capacitor antialiasing filter on the front end. Additionally, it sports a charge-pump-type negative bias generator that lets it handle $\pm$5-V signals, although it is powered by a single 6-V supply (see Design Entry, p. 205).

An 8-bit bipolar converter, from Ferranti Electric Inc. (Commack, N.Y.), also features an on-chip charge-pump for generating a negative bias voltage. The circuit converts voltages down to zero and employs a single supply. Unlike the MOS devices, it needs an external capacitor for the pump and also has its own precision 2.5-V reference.

The next few months could see the arrival of two more CMOS a-d converters with sample-and-hold amplifiers at their front ends. One will be a 12-bit, 100 μs unit from National Semiconductor—the first 12 bit converter to operate from a single +5-V supply.

Pulling double duty

Most of these chips have enhanced analog capabilities, and many also mate more easily with different processors. For example, National's 12-bit chip is available in two versions: as a 28-pin DIP it carries a broadside 12-bit three-state output, as a 24-pin DIP it supplies two bytes on eight pins.

Also at 12 bits is the Am6112 from Advanced Micro Devices Inc. (Sunnyvale, Calif.). Specifically designed with processor interfaces in mind, it too furnishes data in two bytes. In addition, it takes control signals in on three of its data output lines. One line sets the output code at offset binary or two's complement. The other two lines put the converter under microprocessor control with a conversion started by an active $\overline{WR}$ or an active $\overline{RD}$. Those two lines can put the converter completely under the direction of a DMA controller chip (such as the Am9517A).

Another converter aimed at simplifying the link to a microprocessor also uses a bidirectional data bus and supplies either a 10-bit broadside or an 8- and 2-bit output. More importantly, its built-in software protocols enable it to link with virtually any microprocessor without external logic. Not only that, the ADC910, from Precision Monolithics Inc. (Santa Clara, Calif.), is a 6-μs bipolar chip with a precision reference and a clock (see Design Entry, p. 191).

At the peak of their powers?

Integrating a-d converter chips, both those with BCD outputs for DPMs and DVMs and those with binary outputs for data acquisition, might be considered to have reached their zenith. The first drive

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CIRCLE 66

seven-segment LCDs; the latter work closely with processors. However, within the next few months, two U.S. manufacturers plan to unveil a pair of 3½-digit autoranging converters designed for hand-held multimeters. Unlike autoranging chips from Japan, the U.S. versions need only 20 to 30 external components as compared with over 100.

The ultimate in autoranging and in analog front-end functionality must reside in an a-d converter module with the ability to handle a signal with a dynamic range of a million to one (20 bits/120 dB) to an accuracy of 12 bits (see Design Entry, p. 175). Moreover, it operates at over 300 kHz. Earlier autoranging converters that combined a software-programmable gain amplifier with a successive-approximation a-d converter were slow. Further, they tied up the microprocessor while it iteratively increased or decreased the gain of the amplifier until the optimum level was found. That approach might be called negative feedback. In comparison, the MN5420 uses a feed-forward technique.

At the module's input is a sample-and-hold amplifier, followed by a flash converter that measures the approximate level of the input signal. The digital output of the flash converter then sets the programmable gain amplifier: The signal is amplified, sampled again, and a 12-bit conversion made in 1 μs. The 4-bit output of the flash converter and the 12-bit output of the second a-d converter, when combined, furnish a reading accurate to 12 bits of any signal to 160 kHz over a 120-dB dynamic range.

A different drummer

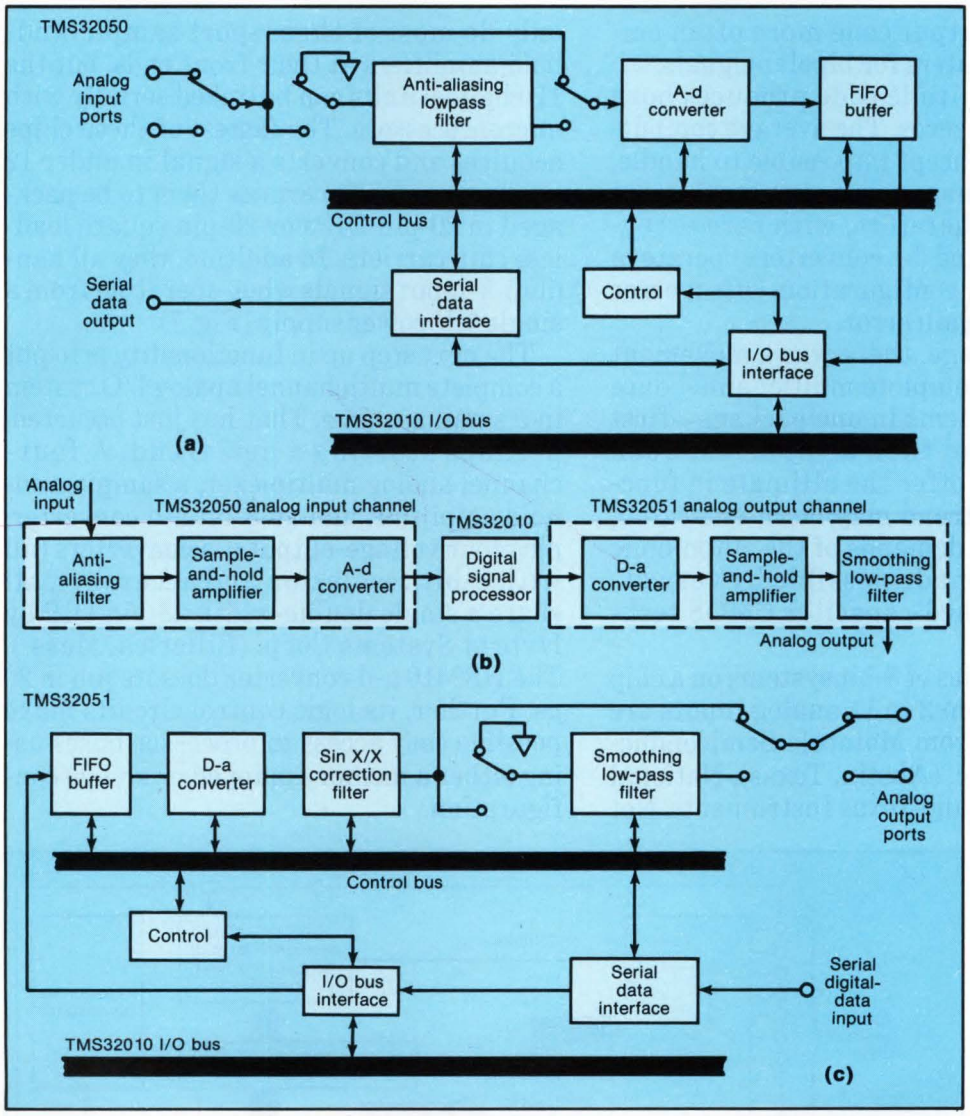
Another interesting route to increased functionality is the development of matched pairs of a-d and d-a converters. Two of these have surfaced recently, each aimed at quite different tasks. One pair is built around hybrids; the other, chips. Both sets incorporate many of the architectural features mentioned earlier and both represent high-resolution systems.

The hybrids are from Analog Devices and are 14-bit units designed for frequency-division multiplexing and time-division multiplexing systems. They can, however, be employed in other types of data transmission, as well as in their own right as stand-alone devices. The a-d converter, designated the HAS-1409, is a two-step device with a sample-and-hold amplifier on the front end. It operates at a minimum throughput rate of 112 kHz, and its three-state output is available as a single 14-bit word or in two bytes. Its mate, the HDD-1409 also accepts its input either way. Thus both can operate from an 8- or a 16-bit bus. The 1409 runs at a guaranteed update rate of 200 kHz, and its output swings ±5 V.

The second duo was designed to permit a digital signal-processing chip, the TMS320 from Texas Instruments Inc. (Houston), to connect its inputs and outputs to the real analog world (ELECTRONIC DESIGN, May 17, 1984, p. 243). The architecture of each chip virtually mirrors that of the other (Fig. 6). The only difference is the addition of the (sin x)/x correction filter in the d-a half of the pair. The low-pass anti-aliasing filter in the a-d converter is identical to the low-pass smoothing filter in the d-a converter.

Switching and sampling

These NMOS chips work with switched-capacitor techniques, so the sample-and-hold function is easy to implement for all of the analog circuits. Their resolution, differential linearity, and monotonicity are a full 16-bits, but integral linearity (accuracy) drops to 10 bits. Both devices operate at a throughput rate of 16 kHz. A quick glance shows that the a-d converter is similar to the Reticon converter in many ways. For example, they both handle a +5-V signal and minimize errors in the vicinity of zero by generating their code in sign-magnitude form and then converting it to the two's



6. Switched-capacitor converters built with NMOS permit a pair of mirror-image chips to contain all the analog and digital circuits needed to link a digital signal processor chip to the outside world. The TMS32050 analog IC (a), from Texas Instruments, contains a 16-bit a-d converter, an anti-aliasing filter, a FIFO memory, and control and serial I/O logic. It works in a system (b) with the output d-a converter chip, designated the TMS32051 (c). Both converters are 16-bit devices with 10-bit integral linearity. The capacitors in both are monotonic to 16 bits, ensuring no missing codes in the input chip and low distortion in the output device.

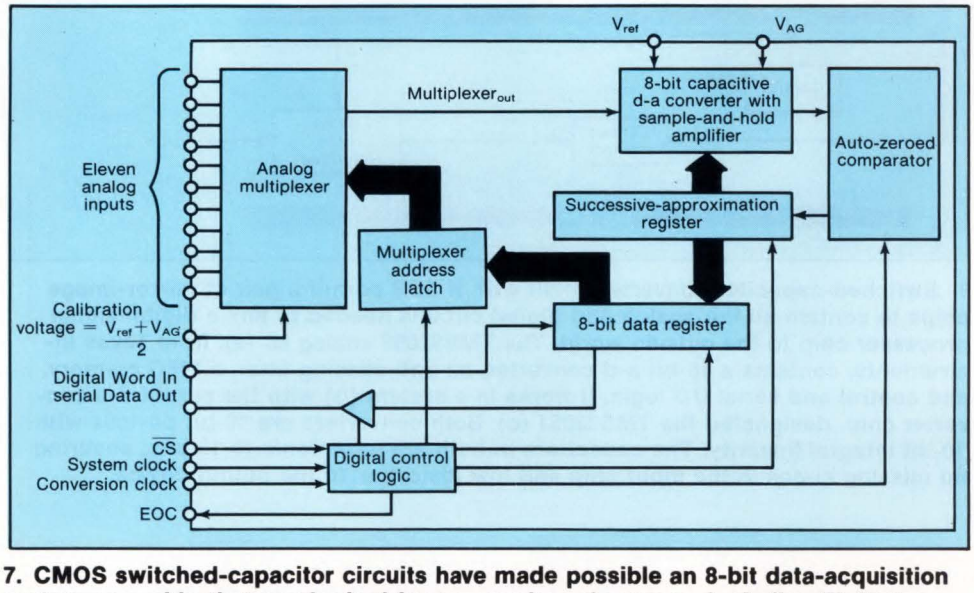
complement output code more often employed by computers for bipolar signals.

A sign-magnitude code produces both plus and minus zeros. The average computer finds that concept impossible to handle, so an offset binary or two's complement code is used. Therefore, with rare exceptions, both a-d and d-a converters operate in an offset binary configuration. Offset error is a function of gain error.

A few years ago, there was a movement afoot to build complete multichannel data acquisition systems in one package—first as modules and then as hybrids. Such systems would offer the ultimate in functionality. The trend may be re-emerging, powered by the demands of the automobile industry and made possible by very affordable switched-capacitor CMOS technology.

In fact, families of 8-bit systems on a chip that handle from 2 to 11 analog inputs are now available from Motorola Semiconductor Products Inc. (Austin, Texas), National Semiconductor and Texas Instruments. Not only do most of them sport sample-and-hold amplifiers at their front ends, but the 11-channel units can be linked serially with microprocessors. The fastest of these chips acquires and converts a signal in under 12 μs. The serial I/O permits them to be packaged in 20-pin DIPs or 20-pin square leadless chip carriers. In addition, they all handle 5-V input signals when operating from a single 5-V power supply (Fig. 7).

The next step up in functionality is to put a complete multichannel analog I/O system in a small package. That has just occurred, perhaps starting a new trend. A four-channel analog multiplexer, a sample-and-hold amplifier, and an 8-bit a-d converter, plus four voltage-output d-a converters (all with 8-bit resolution and accuracy), all share a single double-width 28-pin DIP by Hybrid Systems Corp. (Billerica, Mass.). The HS9410 a-d converter does its job in 20 μs. Further, its logic control circuits make possible easy access to processor buses using either a memory mapped or an I/O configuration.



7. CMOS switched-capacitor circuits have made possible an 8-bit data-acquisition system on a chip that can be had from a number of sources, including TI, Motorola, and National. It samples 11 analog inputs, and a 12th input calibrates it; conversion times approach 12 μs.

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CIRCLE 67

Can IC technology keep pace with converters' demands?

Can semiconductor technology continue to meet the demand for one-chip converters that possess ever-greater resolution, accuracy, and speed? Answering this question from the available evidence and from the devices that are planned does not yield a clear-cut reply. On the one hand, d-a converters appear to be moving quite successfully in the directions indicated. On the other, advances in monolithic a-d converters appear to have stopped dead in their tracks.

The last two years have seen a steady gain in the performance of d-a converters. The period began with a one-chip voltage-output version of the industry-standard bipolar DAC80, from Harris Corp. (Melbourne, Fla.). That device was soon second-sourced by Analog Devices, which improved the circuit by eliminating the need for a +5-V supply. Now, by using its bipolar dielectrically isolated process, Harris has spawned a DAC80 that is four times as fast as the original. Its output op amp settles to within 0.01% in 1 μs. These d-a converters, as well as the 811 and 667, are laser-trimmed on the wafer and use thin-film resistors. Some make use of them in an R-2R network, others turn to an R-2R network on the LSBs and go with segmented current sources for the MSBs. The next six months should see a 12-bit CMOS converter from GE-Intersil (Cupertino, Calif.) with an auto-zeroed output op amp.

About the same time that the monolithic DAC80 arrived, a 16-bit bipolar (current-output) converter with a reference came on the scene. This Harris chip appeared at the same time that 16-bit CMOS (multiplying) current-output converters, which also used thin-film resistors, arrived from GE-Intersil, Micro Power Systems Inc. (Santa Clara, Calif.) and Hybrid Systems. All of these are so-called 16/14-bit converters. (They resolve 16 bits and are accurate to 14 bits.) Except for the Intersil unit, all use some form of segmentation combined with an R-2R network, and none are laser-trimmed. The Intersil device has an on-chip correcting d-a converter that is activated during postassembly testing by blowing an on-chip PROM.

Next, following in the footsteps of the 16/14-bit converters came a family of chips with a reference and an output op amp, the DAC700 series from Burr-Brown. It is built with a bipolar process, and employs thin-film resistors that are trimmed on the wafer. The resultant chip has 14-bit integral linearity and is monotonic to within 14 bits over temperature. For a 16-bit converter, the settling time to 14 bits is typically 4 μs for a 10-V step.

Eight equal segmented current sources supply the 700's 3 MSBs; nine more current sources—used with a modified R-2R ladder—take care of the next 9 bits, and area ratioing along with a continuation of the R-2R ladder handle the four LSBs (ELECTRONIC DESIGN, March 17, 1983, p. 14).

Steady as she goes

A monotonicity of 16 bits over the temperature range has just recently come on the scene with the aforementioned AD569 voltage-output converter. Its unique architecture makes possible the monotonicity but limits integral linearity to 12 bits

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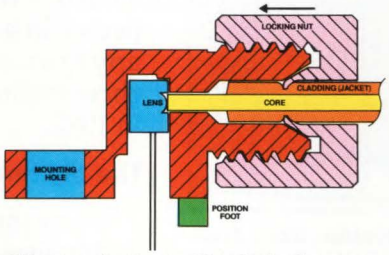

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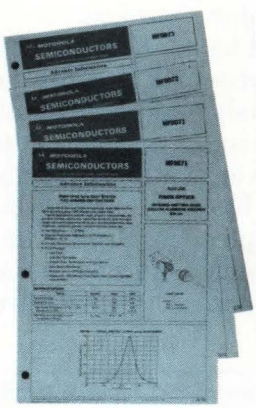

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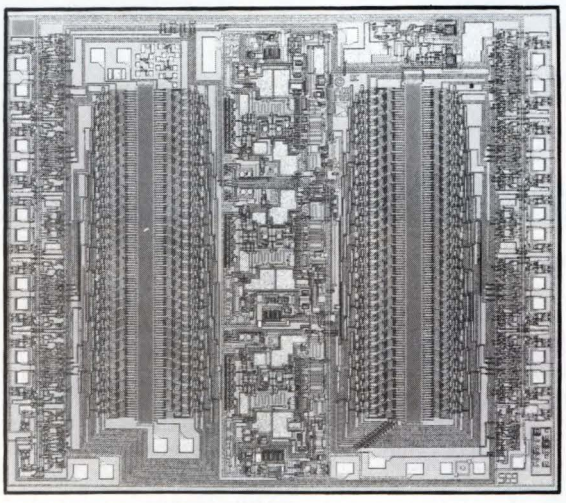
(Fig. 8). Nonetheless, its output settles to within ±½LSB (of 15 bits) of its final value in under 5 μs for a 10-V step.

How long will the wait be to the next step: a 16-bit d-a converter with both integral linearity and monotonicity over temperature guaranteed to the full 16 bits? At minimum, it will be two or three years, since such devices are only now being considered. One proposed approach would trim and keep



8. The one-chip AD569 d-a converter, from Analog Devices, has a resolution and a monotonicity over temperature to 16 bits. The pair of thin-film resistor strings (256 resistors apiece) that make this performance possible dominate the chip. Decoding logic runs along the left- and right-hand edges, and three 16-bit fast-settling op amps lie between the resistor strings.

trimmed the equality of the segments in either voltage- or current-segmented converters.

As advanced merged processes (bipolar plus CMOS) come on stream, it should be possible to automatically zero and automatically calibrate circuits continuously (or as required), thus correcting the accuracy of a device. Until that time, however, system designers will have to use 16-bit hybrids and modular converters. For example, one hybrid uses just two chips, an 18-bit CMOS switch set, and a thin-film network with the 4 MSBs segmented and the remaining 12 LSBs in an R-2R network. The HS9331, from Hybrid Systems, is paired with the HS9377, which adds a reference and output op amp. Thus the evolution of a true 16-bit unit will be slow. Along with greater functionality, significant gains in speed are expected but only incremental increases in accuracy and stability are to be hoped for.

If there is to be a true 16-bit monolithic a-d converter, regardless of conversion time, it is a long way off. By definition, such a device would present no missing codes over its operating temperature range and would exhibit 16 bits of terminal linearity. In fact, the benchmarks set by one-chip converters in 1982 still stand today and none of the devices have been second-sourced—yet. In order to gauge the enhancements expected in a-d chips over the next few years, any frame of reference must include the three major achievements that took place in 1982.

The big three

These include the appearance of the first 14-bit successive-approximation converter with a conversion time of 40 μs (the GE-Intersil ICL7115). The year also marked the arrival of a 12-bit successive-approximation device that converted signals in only 3 μs (the AMD Am6112). These were the first two fast monolithic a-d converters with 12 or more bits of resolution. Both are just now becoming available, and the conversion time of the second has dropped to 7 μs.

The third hallmark of 1982 was the first 1.5-μs 8-bit converter priced at less than $10. Moreover, it performed the sample-and-hold function. The ADC0820, from National Semiconductor, is still the fastest low-cost 8-bit converter available.

Since that time, no other monolithic successive-approximation a-d converters have appeared with 12 or more bits of reso-

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lution, and no 10-bit devices can yet touch the speed of the Am6112. In fact, until now monolithic 10-bit converters were few and far between and their conversion times were in the 30- to 100-μs range.

Stranger than fiction

It was unimaginable that a one-chip 16-bit voltage output d-a converter would show up before a monolithic version of the two-chip 574 a-d converter. Yet that is just what has happened. The device, which was considered imminent two years ago should be available as a stocking stuffer this December—and in plastic at that.

During the two-year waiting period, though, there has been no shortage in activity surrounding the 574. It has become the industry standard for general-purpose 12-bit a-d converters (using two to seven chips) and can be had from multiple sources. As an aside, a primary factor making possible those multiple sources has been the availability of multiple sources for the 565 bipolar 12-bit d-a converter. That high-speed, thin-film converter—with its precision reference—has, in the shadow of the DAC80, become a ubiquitous component with six (going on eight) manufacturers. Their growing popularity signifies that laser trimming thin-film resistors at the wafer level is now widely spread.

These multiple-chip 574s meet the unit's primary speed and accuracy specifications over temperature (35 μs maximum conversion time, bus access in 250 ns, no missing codes, 12-bit accuracy) and are functionally identical as well—but they are not clones. To optimize performance, each divides up its functions differently. The original 574 uses the bipolar 565s plus a second bipolar chip that contains the clock, precision comparator, successive-approximation register, and control logic (I^2L), which permits bus interfaces that handle one or two bytes. The offset voltage of its comparator is trimmed by zener zapping to an impressively low 1/10 LSB.

A five-chip version, from Hybrid Systems, uses a custom CMOS chip for its clock, successive-approximation registers, switches, and decoding and control logic. A bipolar chip that provides a comparator and a reference and a three-chip thin-film resistor network (high bits, segmented; low bits, R-2R) completes the device. What's more, by the end of the year, it should turn up on two-chips, with the thin-film registers divided between them.

Picking up speed

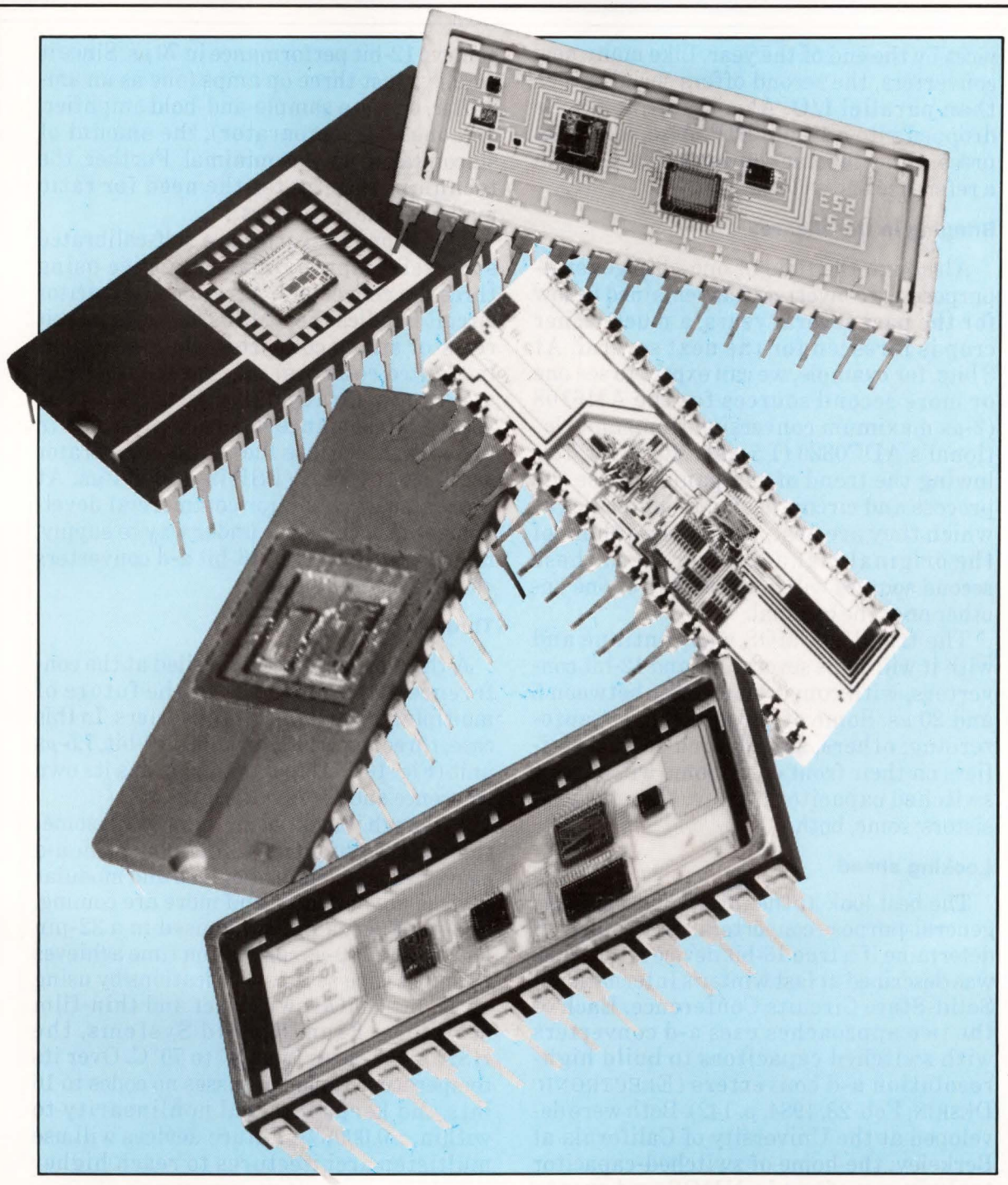
Still another two-chip configuration of the 574 adds the comparator to the bipolar 565 and uses a CMOS chip for logic. However, the analog bipolar IC is built with a dielectrically isolated process that increases its speed significantly. So much so, in fact, that Harris Semiconductor has just announced the HI-674A, which drops guaranteed conversion time to 15 μs and bus access time to 15 ns. All other specifications remain the same. The 674 can be dropped directly into a 574 socket to upgrade a system (Fig. 9).

Within six months, a further drop in conversion time—to 6 or 7 μs—is predicted, putting it in the same range as the 6112. From a system's point of view, as conversion time drops, so must bus access time.

Although very slow, the soon-to-be-announced 12-bit monolithic converters, from National Semiconductor, will certainly be in the running to be a future standard. Even at 100 μs, they are still 100 to 1000 times faster than integrating converters, and even though they are referenceless, they require fewer parts.

Ten bits is suddenly a very popular number, as evidenced by the pair of converters just announced by PMI and EG&G Reticon.

A CMOS chip is expected from RCA Corp.'s Solid State Division (Somerville, N.J.) and a bipolar unit (with a conversion time of 30 μs) is expected from Analog De-



9. The industry-standard 574 a-d converter, originally introduced as a two-chip device, is now built with up to seven chips. A single-chip version of the 12-bit converter should be out by the end of the year. Although the first device used a pair of bipolar chips, the converter is now available from multiple sources, some of which use a combination of CMOS and bipolar ICs.

vices by the end of the year. Like many new converters, the second offers serial rather than parallel I/O. As a result, it can be dropped into a 14-pin DIP. Also, like most present-day bipolar converters, it has both a reference and a clock.

Bringing in the sheaves

Although the field of one-chip general-purpose a-d converters has remained fallow for the past several years, a much richer crop is foreseen for the next several. At 8 bits, for example, we can expect to see one or more second sources for the AM6108 (2-μs maximum conversion time) and National's ADC0820 (1.5-μs). Moreover, following the trend of companies to use the process and circuit design technologies at which they are best, rather than those of the original manufacturer, both these second sources will not be clones of one another or of the original.

The trend to CMOS will continue and with it will come several 10- and 12-bit converters, with conversion times between 5 and 20 μs. Some of these will sport autozeroing; others, sample-and-hold amplifiers on their front ends. Some will employ switched capacitors; some, thin-film resistors; some, both.

Looking ahead

The best look at the future of monolithic general-purpose converters, particularly to determine if a true 16-bit device is possible, was described at last winter's International Solid-State Circuits Conference. Each of the two approaches uses a-d converters with switched capacitors to build high-resolution a-d converters (ELECTRONIC DESIGN, Feb. 23, 1984, p. 142). Both were developed at the University of California at Berkeley, the home of switched-capacitor techniques—first in NMOS and now in CMOS.

One of the converters uses an algorithmic, successive-approximation circuit to achieve 12-bit performance in 70 μs. Since it employs just three op amps (one as an amplifier, one as a sample-and-hold amplifier, and one as a comparator), the amount of silicon taken up was minimal. Further, the technique eliminates the need for ratio matching the capacitors.

The second converter is a self-calibrated successive-approximation device using three d-a converters. A switched-capacitor circuit handles the 9 MSBs, a 5- and a 7-bit resistor string converter (built with ion-implanted resistors) take care of the LSBs and the calibration, respectively. True 16-bit performance has been obtained in under 20 μs because the CMOS comparator settles out to $\pm$ ½ LSB in under 1 μs. At present, several major commercial development programs are under way to supply, in a year or two, true 16-bit a-d converters using these techniques.

Three to go

A third development unveiled at the conference gives a glimpse of the future of multiple step monolithic converters. In this case, three were used to build a 10-bit, 1.5-μs unit (Fig. 10). A bipolar chip, it has its own reference and three-state output.

Although it looks as if there is still something of a wait for true 16-bit monolithic a-d converters, a variety of hybrid and modular devices are available and more are coming. For instance, a hybrid housed in a 32-pin DIP with a 100-μs conversion time achieves an impressive set of specifications by using an 18-bit CMOS switch set and thin-film resistors. From Hybrid Systems, the HS9516 operates from 0° to 70°C. Over its temperature range, it misses no codes to 16 bits and keeps integral nonlinearity to within $\pm$0.0008%. Future devices will use multistep architectures to reach higher speeds.

The slowest and the fastest a-d converters have at least one major point in common: They are almost exclusively

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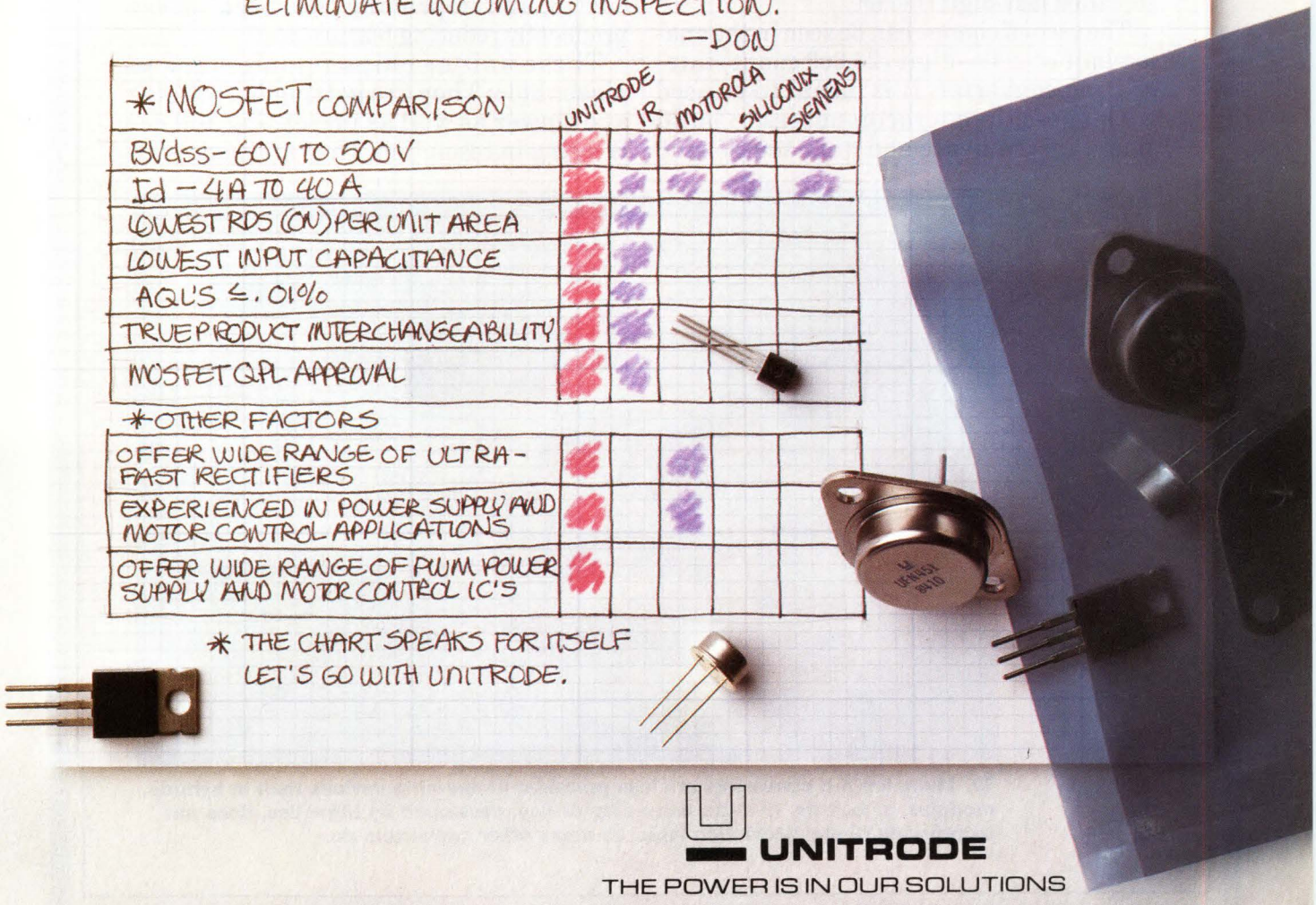

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monolithic. In fact, flash converters did not become practical until they could be put on one chip. Interestingly, the same is true for switched-capacitor circuits.

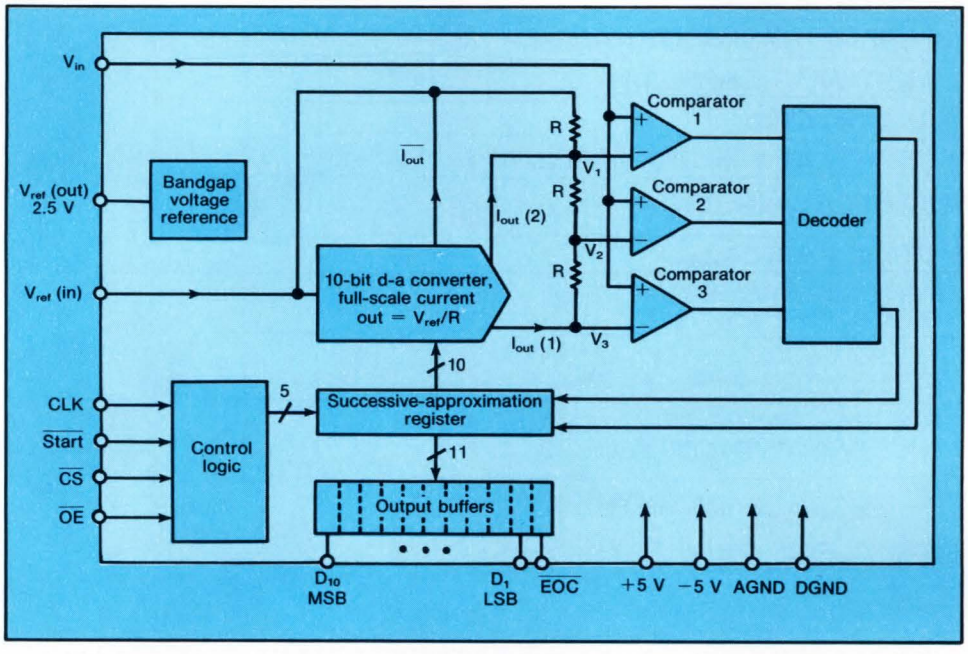
With metal-gate CMOS technology, the integrating chips have reached a resolution of 4½ digits and an accuracy of 15 bits. Currently, there is neither the driving force nor the technology to increase resolution to 5½ digits or to 18 bits. However, two developments are on tap. The first represents a move from aluminum-gate to molybdenum-gate CMOS for a 4½-digit integrating a-d converter from Micro Power Systems. The process change brings the input noise of the pre-amplifier to a new low. As a result, the device can resolve 10 μV and thus eliminate so-called last-digit flicker.

The second change can be seen in the analog half of a 4½-digit (20,000 count) integrating converter. It is meant to be used with one-chip microcomputers to build smart instruments and data acquisition systems. The chip, from Teledyne Semiconductor (Mountain View, Calif.) contains the integrating op amp, comparator, and automatic zeroing circuits (Fig. 11). The computer controls the chip's timing, creates its output code, and processes measurement results. It could, say, linearize thermocouples, perform cold junction compensation, and calculate flow by taking the square root of the value of a differential pressure measurement.

The ways to go

There are only three discernible trends in flash a-d converters: increasing proliferation in kind and number, an attempt to decrease power requirements by switching to CMOS, and improving the speed-power product by reducing feature size.

These unique chips remain hard to pigeonhole: They are getting both faster and slower as well as increasing and decreasing in resolution. They are made with



10. Multistep a-d converters are less prevalent in one-chip devices than in hybrids, modules, or boards. A 10-bit three-step device, developed by Signetics, does not incorporate digital correction logic, as many other converters do.

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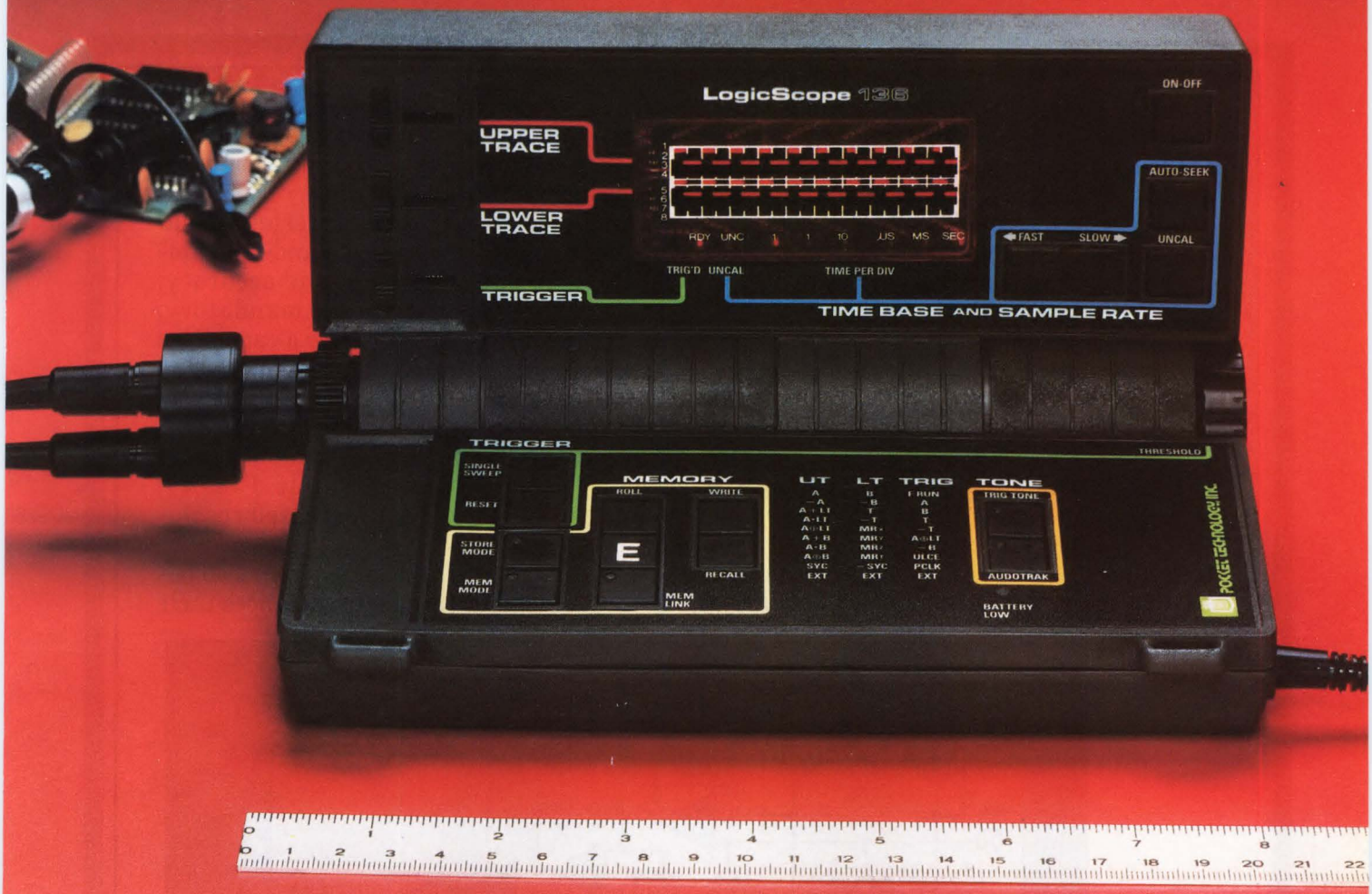

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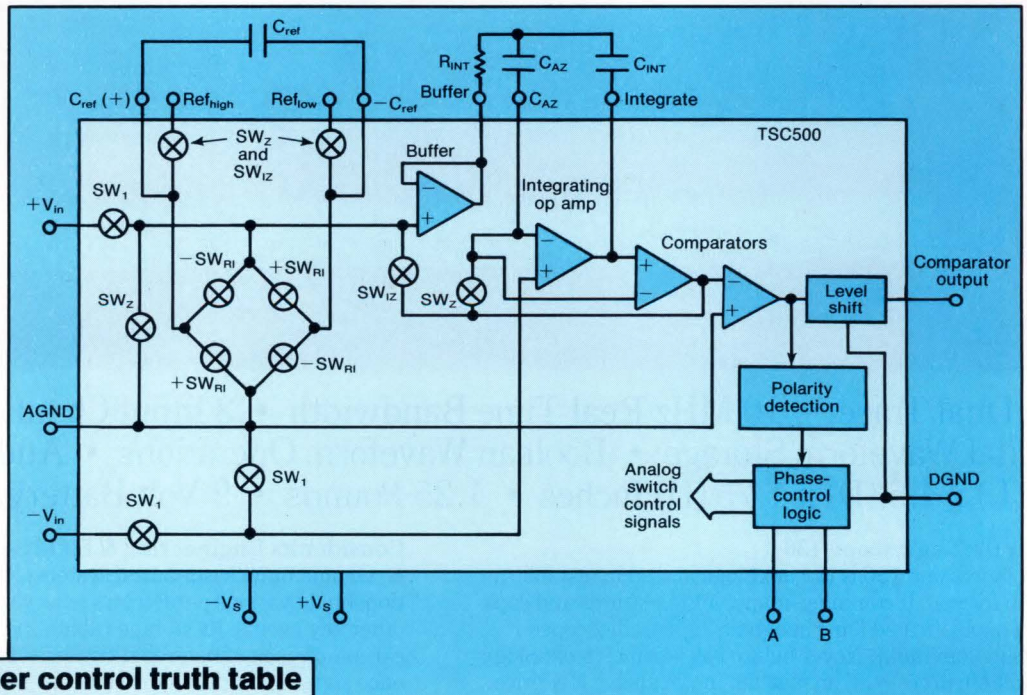
Not so fast

Flash converters should be the easiest converters to use: Simply hook them up to the signal, supply a clock and a reference, and the answer is always there. Despite their apparent simplicity, in most applications they are operating at blinding speed, and a practical knowledge of video or rf techniques is required. In addition, several have to be clocked continuously to maintain an answer; all must be clocked to find a new answer. Some require positive signals, others demand negative, and some handle bipolar inputs.

At the same time, such converters would appear not to require sample-and-hold amplifiers. To optimize speed and accuracy, though, these amplifiers are mandatory, and they must be able to drive a capacitive load, which is usually changing as fast as the signal does. The converter's eccentricities do not stop here: some are pipelined, others are not; some consume a great deal of power, some very little. Finally, some can be stacked for increased resolution.

These converters do suffer from two potential problems. In certain instances their



Converter control truth table

Converter phase	A	B
Zero output of integrator	0	0
Auto-zeroing circuit	0	1
Integrate signal	1	0
De-integrate	1	1

11. The ultimate adaptation of an analog chip to microprocessor compatibility is an a-d converter that will not work without a processor. Fabricated in metal-gate CMOS, by Teledyne Semiconductor, it represents the analog portion of a 20,000-count (4½-digit) integrating converter. A microprocessor does the rest.

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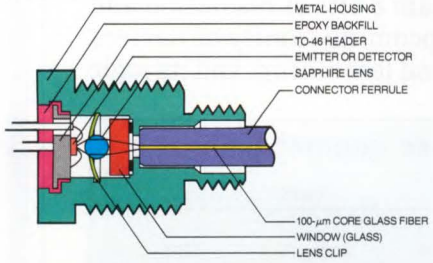

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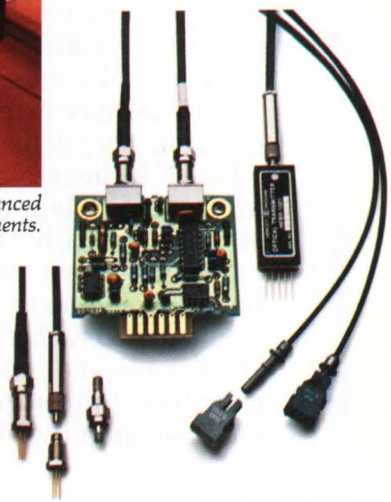

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input bandwidth is not up to the specified sampling rate. Also, they have a tendency to miss a code every few billion conversions. The first difficulty shows up as an inability to digitize a sine wave of half the rated sampling frequency (its Nyquist frequency) to the specified resolution and accuracy. For example, an 8-bit converter that samples at 100 MHz may only supply 6 bits of accuracy when encoding a 50-MHz sine wave. An accuracy of 8 bits may be obtained at only 15 MHz.

The second problem may seem insignificant until it is realized that such an error may occur several times a minute when a converter is sampling at 100 MHz. The error is particularly troublesome, as well as being difficult to locate, when a flash converter is used to build a two-step device.

All flash converters do have one thing in common: they demand 2^N-1 comparators, where N is the resolution in bits. Within the approaching legion of flash devices are several monolithic two-step, or half-flash parts. These require a mere $2(2^{N/2}-1)$ comparators. Thus an 8-bit converter, say, would use 30 rather than 255 comparators. If a sample-and-hold function is not implicit in its architecture, it must use a sample-and-hold amplifier between the signal and the input.

Flash converters' move to less power has been made possible by advances in process geometry (Table 1). Such work has been one of the converns over the past two years of TRW Inc.'s LSI Products Division (La Jolla, Calif.). Its main intention has been to drop the minimum feature size of its triple-diffused bipolar process from 2 μm to 1 μm and to go with double metal interconnects. The first device was a 6-bit, 100-MHz chip (the TOC1029) that arrived about two years ago (ELECTRONIC DESIGN, Sept. 16, 1982, p. 89).

The drop in feature size is accompanied by an increase in speed/power ratio which permits chips to either sample faster at the same power or consume less power than was previously needed at a specific speed. In addition, input capacitance drops, making the converters easier to drive.

By moving from a 5-μm bipolar ECL process to a 1-μm linear MOSAIC process, Motorola Inc.'s Semiconductor Products Division (Phoenix, Ariz.) hopes to increase the sampling rate of its 7-bit flash converter from 15 to 25 MHz, enabling 10-MHz 1-V signals to be encoded to 8 bits of accuracy. Two of these 7-bit converters can then be stacked to obtain 8 bits of resolution and accuracy. The upcoming family of devices uses less power and less silicon, and its logic

Table 1. Improvements in flash converters as process geometry shrinks

		2 μm			1 μm		
Maximum signal bandwidth (MHz)	Resolution (bits)	Power dissipation (W)	Sampling rate (Msamples/s)	Input capacitance (pF)	Power dissipation (W)	Sampling rate (Msamples/s)	Input capacitance (pF)
50	6	Not practical			2.0	100	20
12	8				3.8	50	160
7	6	1.1	25	75	0.6	20	30
	8	2.7	20	250	1.4	20	100
	7	—	—	—	1.0	20	60
5	9	4.7	18	280	—	—	—

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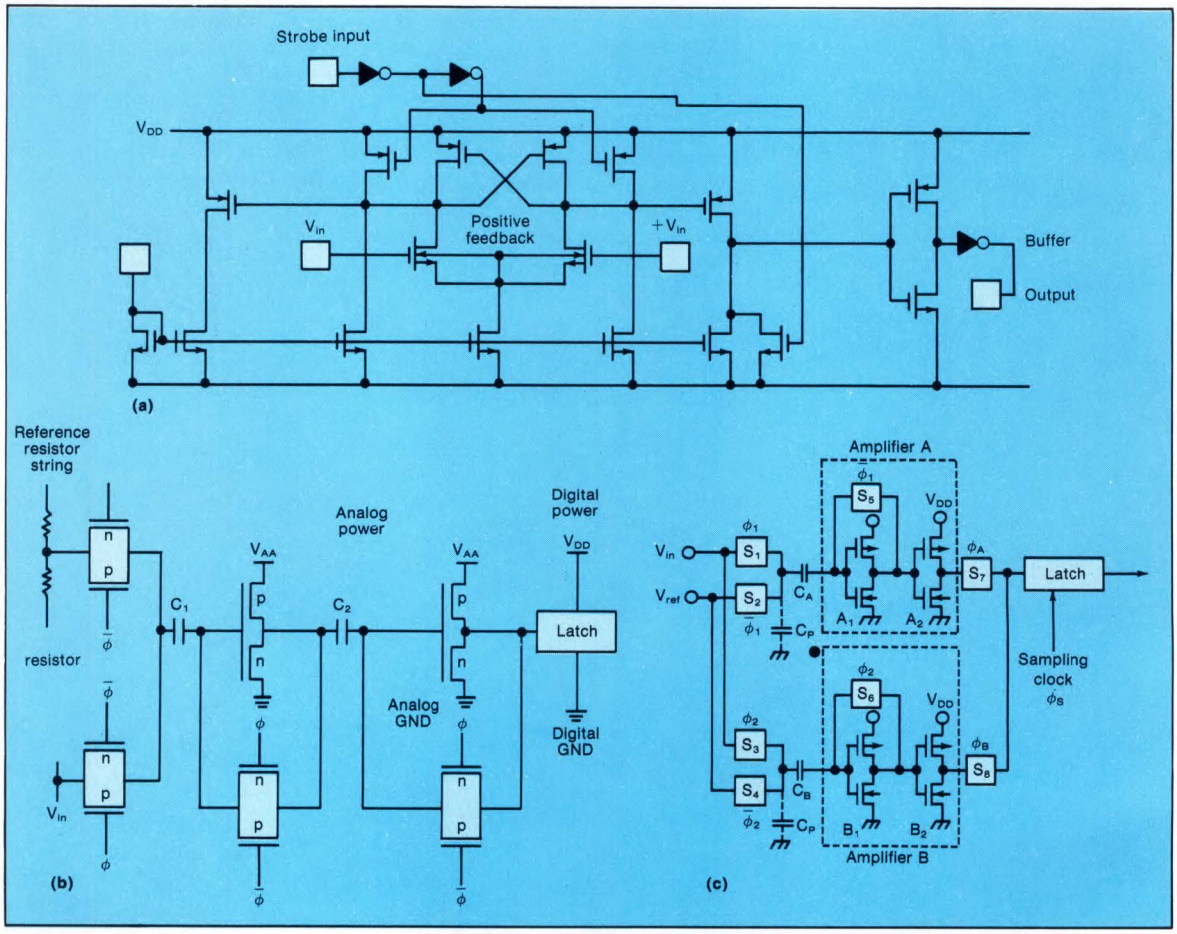
CIRCLE 71

will be TTL-compatible.

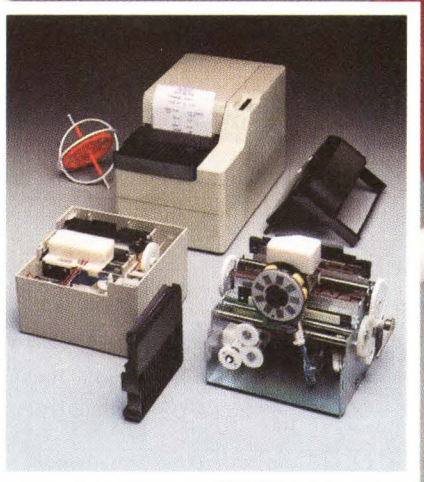
Today's variety of flash converters is staggering. Even a limited overview of these devices shows the dramatically lower power requirements of CMOS converters (Table 2), which use a number of different comparator circuits (Fig. 12). Most, but not all, take advantage of the switches and capacitors made possible by the CMOS process, which uses automatic zeroing to eliminate offset voltage errors.

As for the future, four of the seven a-d converters unveiled at February's ISSCC were flash units. Heading the list, a 400-MHz 6-bit converter from Hewlett-Packard Laboratories (Palo Alto, Calif.), proves quite clearly that silicon is not limited to 100 MHz. It takes advantage of a bipolar process that builds 5-GHz transistors and a circuit architecture that carries out two bits of analog encoding ahead of the clocked comparators (Fig. 13).

Another silicon flash converter is an 8-bit, 120-MHz unit from Matsushita Cen-



12. A variety of comparators are used for CMOS flash converters. Most use switched-capacitor circuits to perform automatic zeroing. When a pair of the RCA circuits (a) are cascaded, 8-bit, 15 MHz converters can be built. Rather than autozeroing, a differential circuit is used by Telmos (b) to eliminate the offset voltage errors. It builds 7-bit, 10-MHz units. Combining both techniques is Toshiba's differential, autozeroed comparator, which builds an 8-bit, 20-MHz CMOS converter—the fastest CMOS unit around.



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tral Research Laboratory (Osaka, Japan), which uses a 1-μm bipolar process. Completing the list are an 8-bit, 100-MHz device from Sony Corp. (Kanagawa, Japan) and a 20-MHz, 7-bit bulk CMOS converter from Toshiba Microelectronics Center (Kawasaki, Japan). The first is the fastest 8-bit unit to date; the second, the fastest 7-bit bulk CMOS device (ELECTRONIC DESIGN, March 22, 1984, p. 75).

Also on the horizon are converters ranging from 4-bit, 15-MHz silicon CMOS chips to 4-bit, 1-GHz gallium arsenide ICs. Tektronix Inc. (Portland, Oregon) is also working with gallium arsenide and has achieved 5- and 6-bit performance; the company will continue experimenting until it reaches the required 8 bits of resolution. At present, surface states cause hysteresis in the depletion-mode MESFETs, limiting their resolution.

Over the past few years, the speed, resolution, and accuracy of monolithic and hybrid successive-approximation a-d converters have increased. Sample-and-hold amplifiers, on the other hand, have witnessed increases, but not at the same pace as their successive-approximation brethren. Help is arriving. It should be noted that even the first device (the Harris HA-2420) was aimed at 12-bit a-d converters.

Defining perfection

The ideal sample-and-hold amplifier requires a set of specifications that in no way degrades or hinders the performance of

Table 2. Comparing flash converters

Resolution (bits)	Sampling rate (MHz)	Power dissipation (mW)	Signal voltage (V)	Supply voltage (V)	Process	Model number	Manufacturer	Comments
10	20	1800	0 to −2	−5.2	Bipolar	AN6859	Panasonic	Highest resolution; high speed
8	50	3700	0 to −2	−5.2	Bipolar	TDC1025	TRW	See Table 1
8	20	900	0 to −2	−5.2	Bipolar	MB40508	Fujitsu	
8	5	75	3 to 8	5 to 8	CMOS	MP7683	Micro Power	Two-step circuit
7	14.5	1100	±2	+5, −5.2	Bipolar	MC10315L	Motorola	Can be stacked
7	20	400	0 to +2.5	+5, +12	NMOS	PNA7507C	Phillips	Uses high-impedance reference resistor string
7	8	150	±3.2	±5	CMOS	TML1070	Telmos	
7	1	9	±3.2	±5	CMOS	TML1072	Telmos	
6	12 to 19	200	2.4 to V_{cc}	5 to 8	CMOS/SOS	CA3300	RCA	CMOS on sapphire, must be clocked
6	110	500	±2.5	+5, −5.2	Bipolar	SDA5200	Siemens	
4	100	1200	±2.6	+5, −5.2	Bipolar	AM6688	AMD	May not be available

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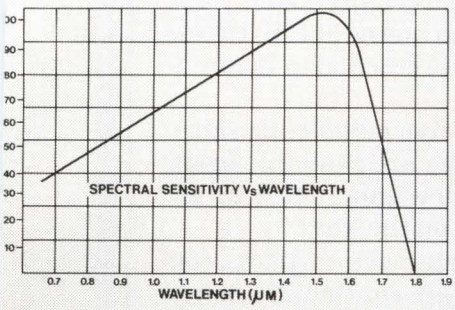

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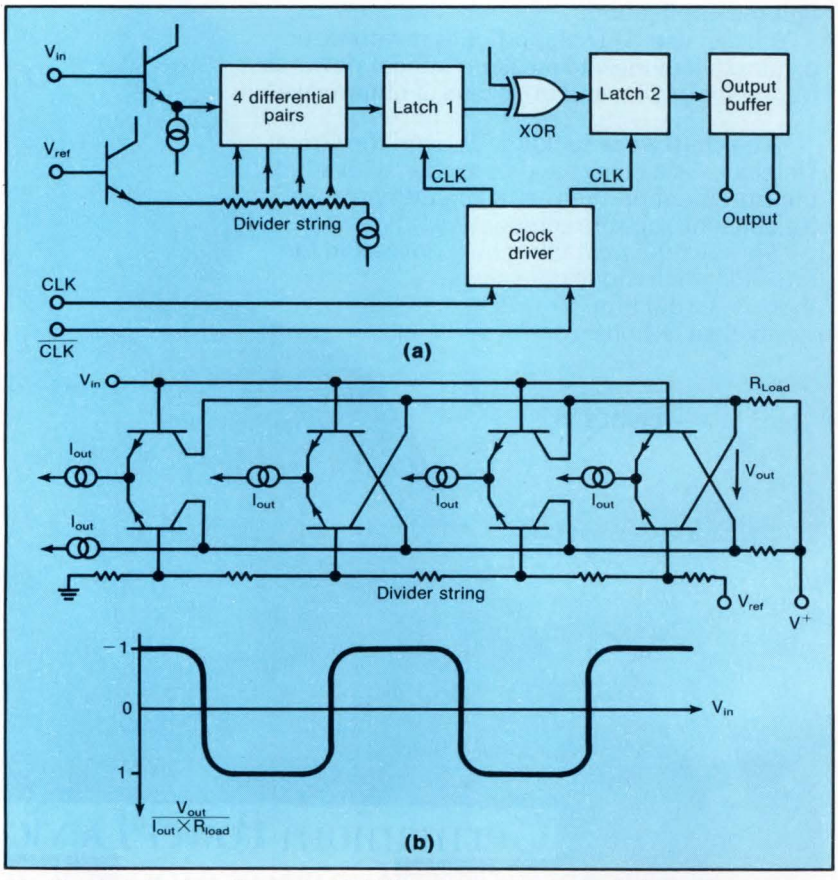
the converter. The following relationships must exist: First, the time needed to acquire a full-scale signal (to within ± ½ LSB of the converter's resolution) should be less than one-tenth of the conversion time. Second, the aperture uncertainty time, or jitter, should be short enough to allow the converter to accurately sample complex waveforms with sinusoidal frequency components up to half its maximum throughput rate (at the system's Nyquist rate).

Third, all other errors, both dc and dynamic (such as charge transfer, feedthrough, offsets, and droop) must represent less than ± ½ LSB of the converter's resolution in bits. In earlier modular sample-and-hold amplifiers, there was often a tradeoff between acquisition time and droop. However, in most of today's units—regardless of their construction—the required hold time (conversion time) is no more than 10 times the acquisition time; thus droop is not a problem.

At last count, only five monolithic sample-and-hold amplifiers are available from four suppliers. Three new units, one from an additional source, are on the way.

Unlike their converter counterparts, for which new processes are continually being developed or old ones refined and upgraded,



13. Hewlett-Packard's 6-bit, 400-MHz flash converter (a) reaches very high speed by performing 2 bits of analog encoding with differential transistor pairs (b) ahead of the latched comparators. As a result, only 17 rather than 63 comparators are needed.

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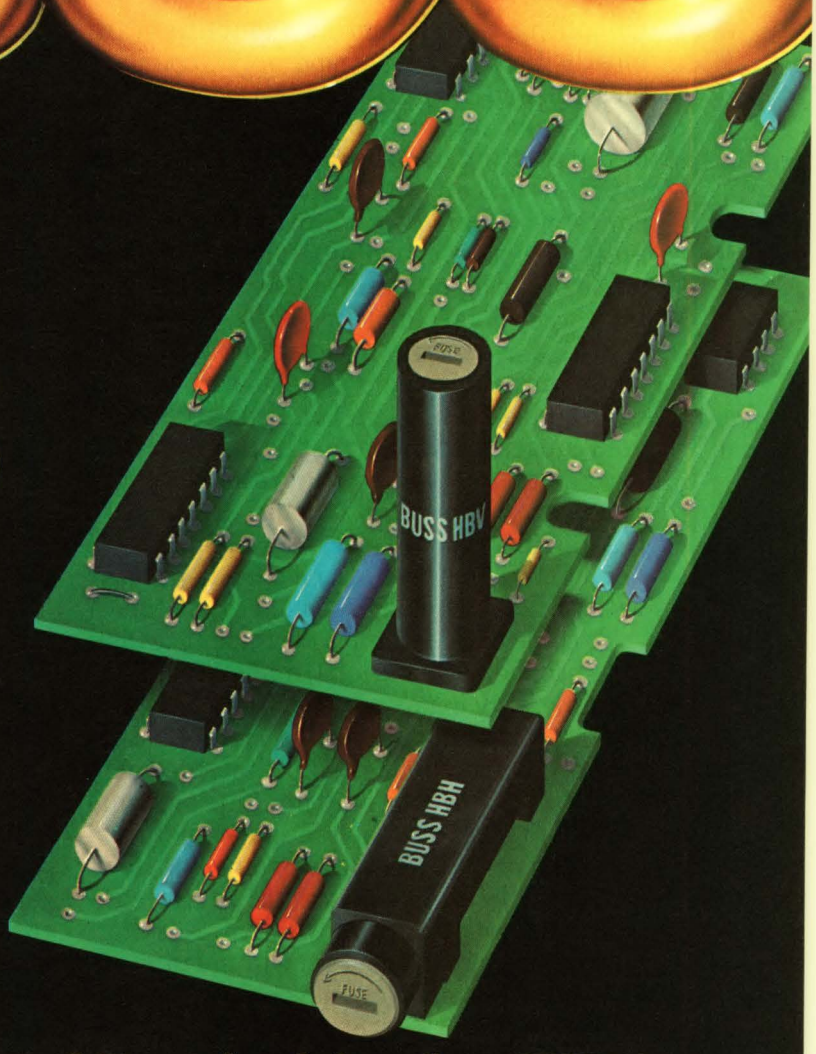

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monolithic sample-and-hold amplifiers are mostly limited to existing process technologies. Although CMOS or biMOS processes might seem natural for this application, all of the existing and the planned devices are bipolar—except for the HA-2420, which contains a pair of p-channel MOSFETs built with a modified bipolar process. The latest of the bipolar units have taken advantage of biFET technology.

Still, a seemingly minor process change made just a few years ago has had significant consequences on functionality: The hold capacitor, which must be insensitive to voltage and also have a low dielectric absorption, was brought on chip. In Harris's HA-5320, that capacitor is a 100-pF MOS device, but the rest of the chip is bipolar with JFETs buffering the hold capacitor.

To some extent, higher performance (and thus broader applications) made the change possible, which may appear to be a paradox. The acquisition time of the HA-2420 was dropped from 5 to 1 μs. (Thus it needed only a 100-pF capacitor). Although hold time needed to meet a droop requirement with a 12-bit accuracy is ordinarily somewhat lower, since the 5320 is aimed at faster converters, droop is not a problem. Further, Harris has just made a very important upgrade of the relatively new chip—acquisition time to 0.01% is now guaranteed to be under 1 μs worst case. Previously, that figure was a typical specification.

Across the spectrum

The solutions to the problem of fast analog sampling represent the wide diversity of circuit design technology. The 2420 (Fig. 14a) uses an input op amp that charges the external hold capacitor (C_H) located between its output and ground. A MOSFET input buffer op amp limits the capacitor's discharge while it is holding. The device may be connected as an inverter or follower. External resistors set the gain at unity or greater. (Most sample-and-hold units are used as unity-gain followers.)

The AD582 (Fig. 14b) may appear similar, but its external hold capacitor (C_H) is charged as a true integrator in the feedback loop of the output op amp. The 5320 is similar except that the hold capacitor, as mentioned, is on chip and low-noise JFETs rather than MOSFETs minimize droop. Using a circuit somewhat similar to that of the 2420 but internally connected as a unity-gain buffer, the LF198, from National Semiconductor, also uses low noise JFETs to replace the MOSFETs (Fig. 14c).

Another switch

All of these units use a low-leakage bipolar switch between their input op amps and their hold capacitors. Another kind of switch circuit, a diode bridge, is used in an internally connected unity-gain buffer sample-and-hold amplifier, the SMP-10, from PMI (Fig. 14d). It uses a third amplifier, called a supercharger, to drive the external hold capacitor, which, like those on the 2420 and the 198, are connected to ground. The SMP-10 was the first one-chip sample-and-hold amplifier to guarantee acquisition time to 0.01%—in this unit just 5 μs. Rather than JFETs, it uses low bias current superbeta bipolar transistors to minimize droop.

Three upcoming sample-and-hold amplifiers each offer something different. A circuit similar to that of the 5320, with an on-chip 100-pF capacitor and working with JFETs, adds a pair of laser-trimmed thin-film resistors to set the gain (Fig. 14e). The AD585, from Analog Devices, is not as fast as the dielectrically isolated 5320, but at 2.5 μs, it will still guarantee acquisition to 0.01%.

The second chip to arrive—and none too soon—is aimed at 14- and even 16-bit converters. It operates at an inverting gain of 1, uses JFETs, an on-chip capacitor in an interesting circuit, and a third amplifier. The last is located between the input and the

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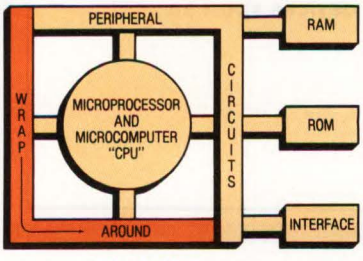

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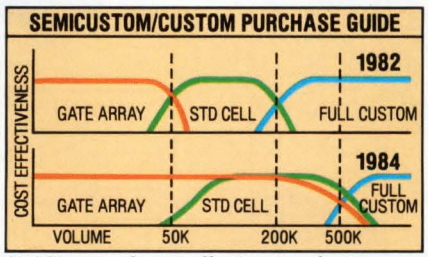

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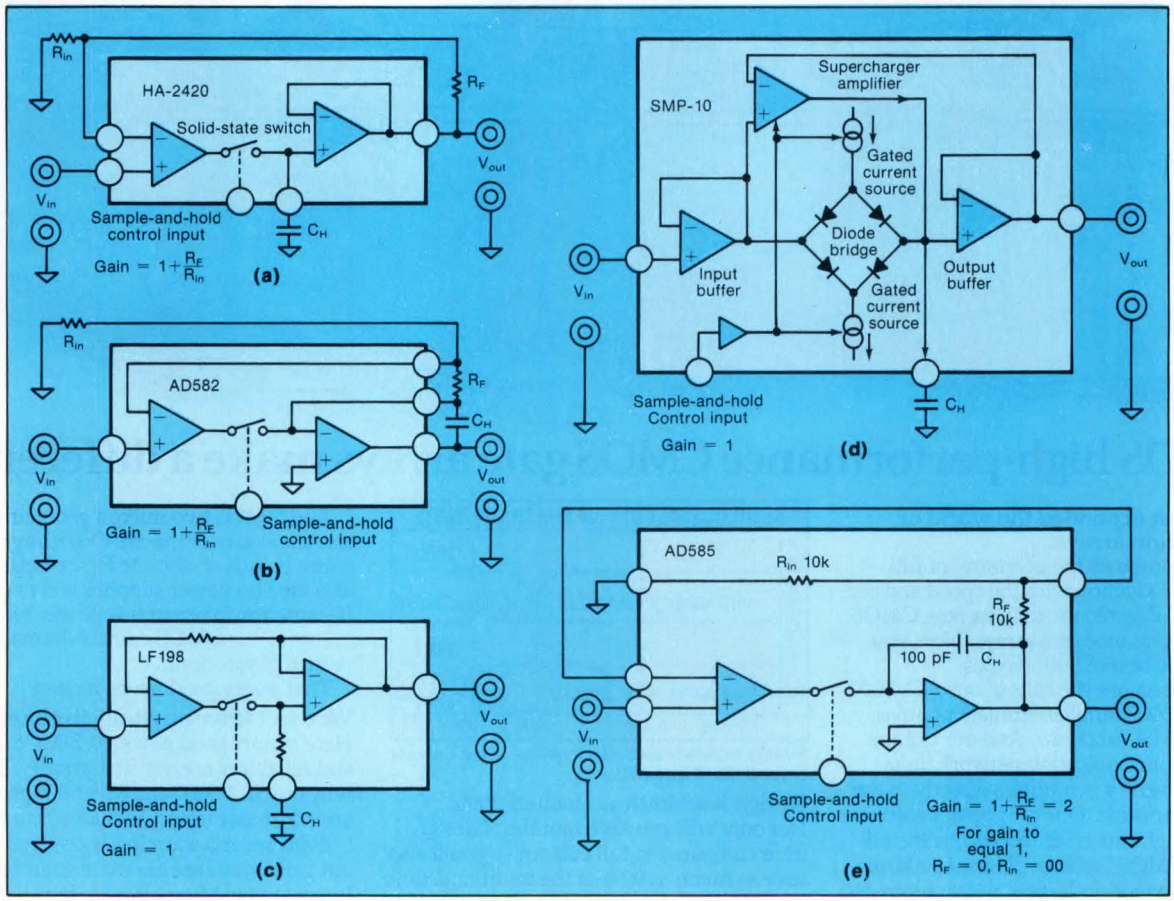
switch, to charge the capacitor. It can acquire a new sample of 0.001% accuracy in 2 μs. From Signetics Corp. (Sunnyvale, Calif.), the output of TDA1535 slews at 100 V/μs and it easily samples 20-kHz sine waves. The third chip, slated to arrive from Harris, some time next year, will move 12-bit sampling time to under 0.5 μs.

When faster or higher accuracy sampling amplifiers are required, the user must turn to hybrids and modules. Designers of such devices have the luxury of picking devices from any process to minimize errors and maximize performance. For example, high-speed MOSFET switches can be combined with fast, low-offset bipolar amplifiers using gigahertz-bandwidth transistors. In addition, great care can be taken in laying out the unit, thus minimizing coupling between high-speed digital and analog circuits. □



14. Monolithic sample-and-hold amplifiers, the few around, all are built on bipolar processes. However, their architectures and functions differ. Some can operate in both inverting and follower configurations and with variable gains (a, b), while others can only operate as unity-gain followers (c). Most use bipolar switches, but one uses a diode bridge (d). The newest devices sport an on-chip hold capacitor (e).

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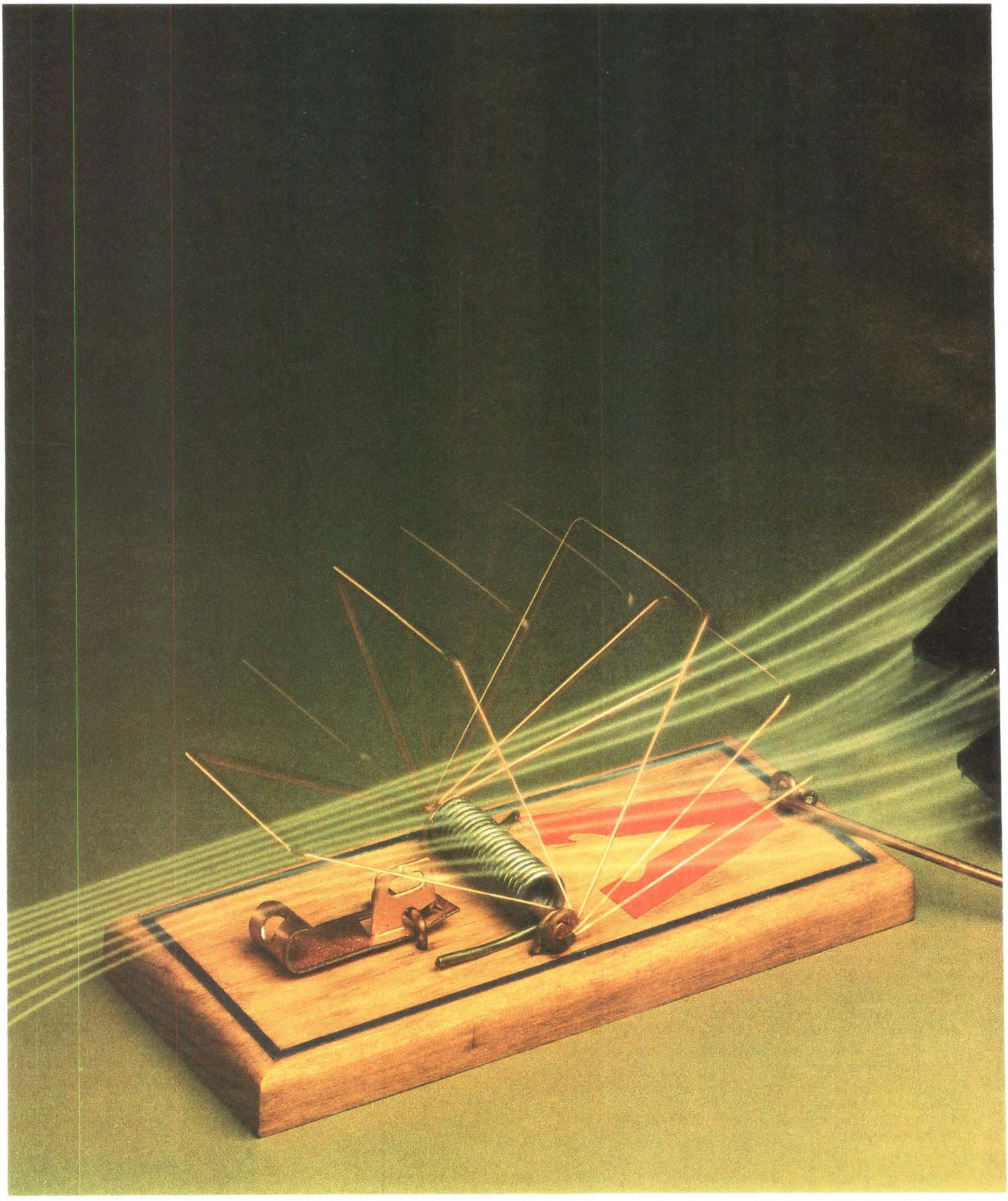

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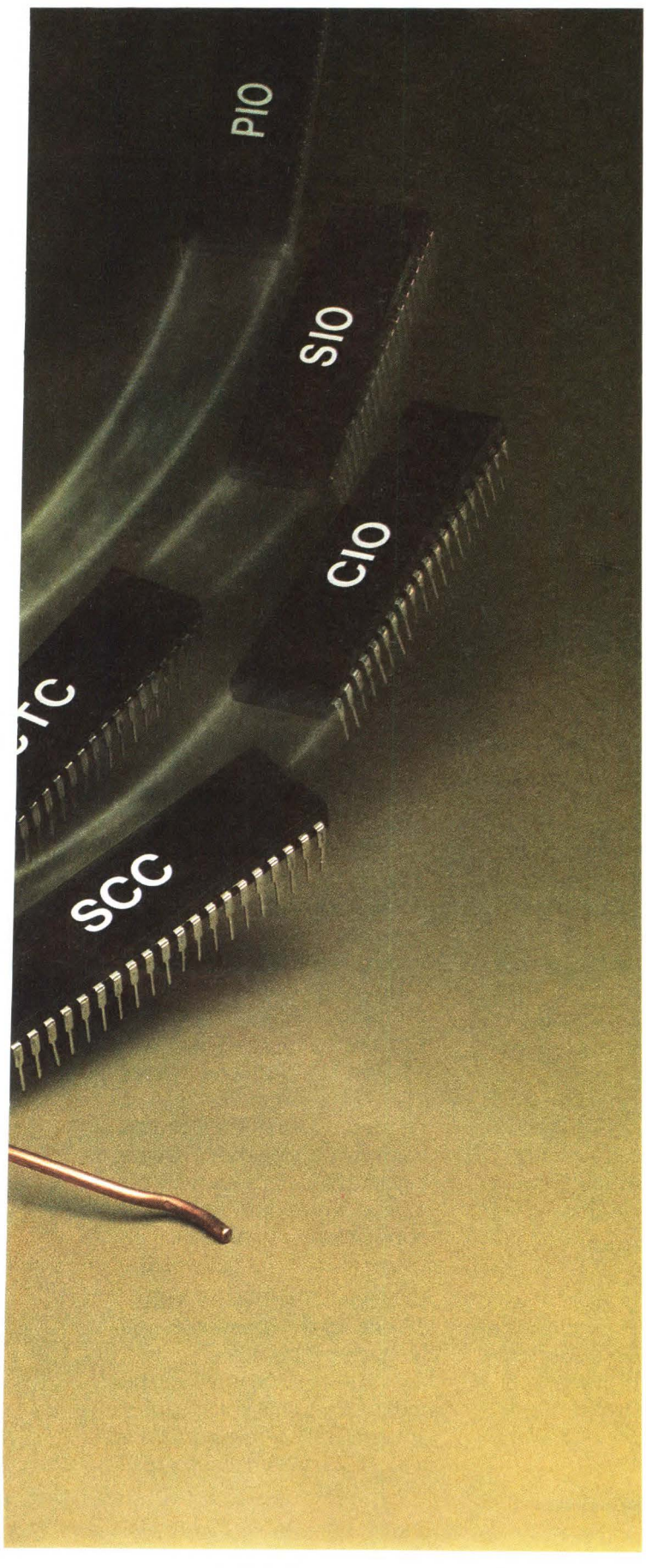

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This regulator has guarantees of 1% initial voltage tolerance, 0.015%/V line regulation, and 0.02%/W thermal regulation.

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LT1001 The Lowest Offset Voltage And Drift General Purpose Op Amp

Useful for low-level signal processing and high accuracy data acquisition applications. Has performance features of 15μV max. offset voltage, 0.6μV/°C max. offset voltage drift, and 2.0nA max. bias current. For similar performance in a dual with guaranteed matching specifications, the LT1002 is available.

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LT1003 5 Volt/5 Amp Voltage Regulator

The LT1003 is ideal for on-card regulation and laboratory supplies where more current is needed than the LM323 can provide. It has a 2% initial tolerance output voltage guarantee.

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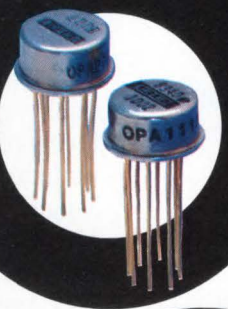

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32-bit computer system shares load equally among up to 12 processors

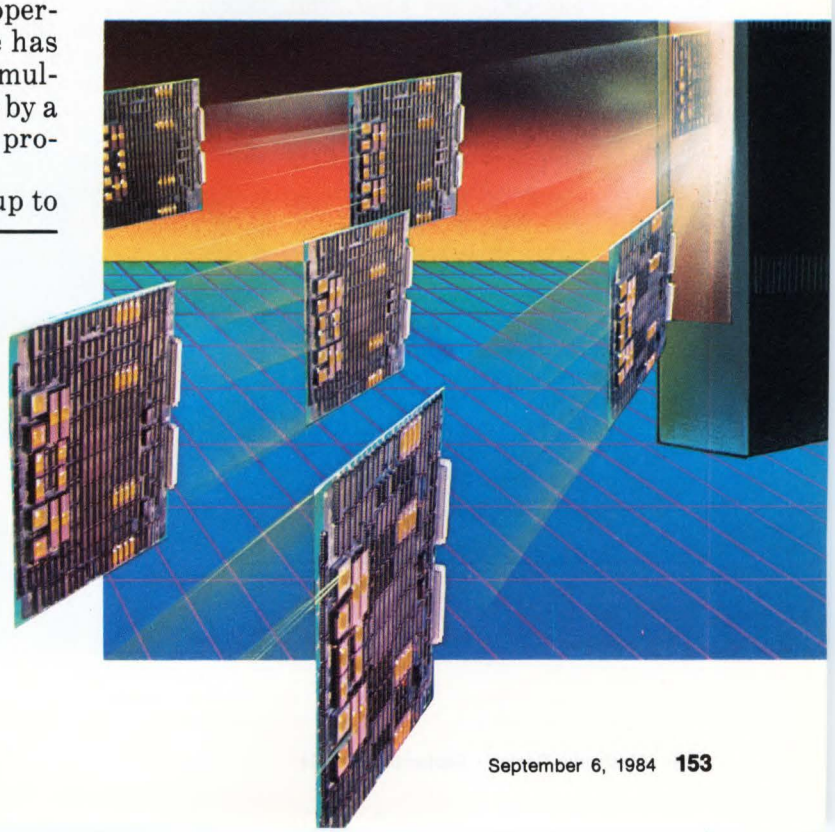
A multiprocessor computer automatically redistributes the work load and lets the user add more CPUs, employing one modified copy of the Unix operating system.

The performance of microprocessors has steadily increased as the demand for computer power has continued to spiral upward. What would seem to be the most powerful outcome of these trends—a computer that uses multiple processors—has run afoul of the law of diminishing returns in several ways.

Traditionally, it has been necessary to call for extensive changes when more processors are added to a system. Those additions, in turn, invite memory contention and overworked buses and require multiple copies of expensive operating systems. Furthermore, experience has shown that adding a processor to a system multiplies that system's and computing power by a factor of only 0.8, making each successive processor less effective.

By sharing its processing load among up to 12 architecturally identical microprocessors and employing a single copy of a Unix-based operating system, a new computer eliminates the barriers associated with multiprocessor systems. Called the Balance 8000, it delivers up to 5 million instructions/s (MIPS). Its power grows almost linearly when more processors—32-bit NS32032s plus floating-point and memory management units—are added (see "More is Better, Finally," p. 154).

To make the most efficient use of its multi-



Gary Fielland and **Dave Rodgers**
Sequent Computer Systems Inc.

Gary Fielland, director of advanced development at Sequent, worked at Intel for nine years, mostly in its OEM Systems operation, before joining the Portland, Ore., company. He holds a BSME and a master's degree in electrical engineering and computer science from the University of Florida.

Dave Rodgers is vice president of engineering at Sequent. He worked at Digital Equipment Corp. for 10 years, where he was instrumental in the design of the VAX 11/780. He holds a BSEE from Carnegie-Mellon University.

processing power, the system dynamically balances its load; in other words, it automatically and continuously assigns tasks to run on any processor that is currently idle or busy with a lower-priority task. This process is carried out transparently; neither the user nor the programmer need be aware that the system sports multiple processors.

Easy to extend

At the same time, the computer is easily extensible. The user can add CPUs, memory, and I/O subsystems within a node, or more nodes within a distributed network, or more distributed and local-area networks—all with no changes in software (Fig. 1). Moreover, if the machine's assigned tasks do not run quickly enough, the user can add two more processors by simply plugging in a single circuit board.

The new computer is the first of a family to implement a processor pool architecture (see "Getting Everyone Into the Pool," p. 156). The system consists of a pool of 2 to 12 processors, a high-bandwidth bus, up to 28 Mbytes of primary storage, a diagnostic processor, up to four high-performance I/O channels, and up to four IEEE-796 (Multibus) bus couplers. It is managed by a version of the Unix 4.2 BSD operating system, enhanced to make the multiprocessor base appear invisible to any application program.

Each processor in the pool is a subsystem

More is better, finally

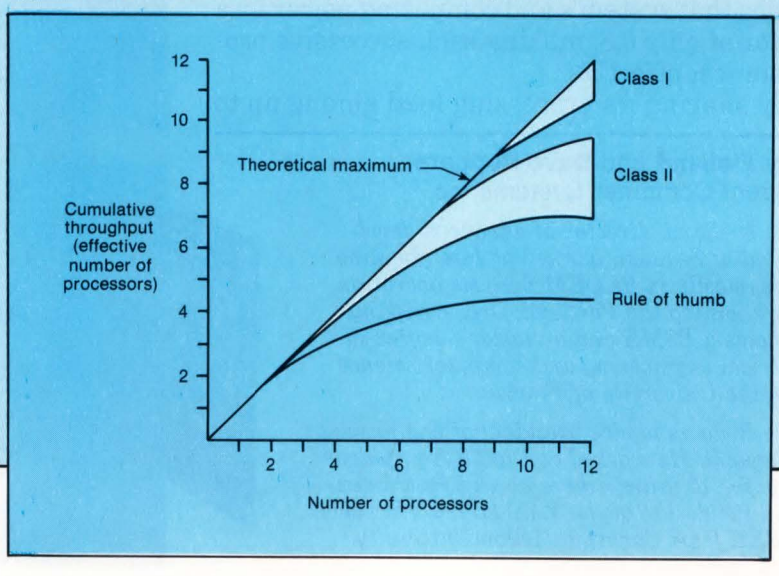
The Balance 8000, with its scalable processor pool architecture, lets OEMs easily set the number of processors to match an application. It does so in spite of a well-known saturation curve reflecting the performance of tightly coupled multiprocessors—a rule of thumb that says that each additional processor adds only 80% of the power of the one previously added. Under this rule, no matter how many CPUs are added, the maximum effective computing power does not surpass the equivalent of only five processors.

Worse, the rule only predicts the effective computing power and not an additional processor's effect on a particular application, which in many ways could actually degrade that program's performance. Therefore, this rule is best taken strictly as a measure of hardware performance.

Two classes of simple benchmarks were used to test the rule against Balance 8000: One class (Class I, in the figure) consists of traditional benchmarks like binary sort and Whetstone programs. The second (Class II) consisted of so-called pathological benchmark programs like cache busters and memory saturation generators to push the machine to its limits. All the tests are concentrated on the computer itself and produce negligible I/O activity.

Overall system performance is N times the ratio t_1/t_2, where t_1 is the run time for executing a single copy of a benchmark and t_2 is the run time for executing N copies simultaneously. The results show how the new computer's performance stacks up against the rule-of-thumb prediction and the theoretical maximum.

Clearly, the cached machine is well suited for running the Class I tests. It achieves a nearly linear improvement in performance (up to eleven effective processors when twelve are applied). With the same number of processors, the Class II tests show a much wider spread, but still yield an effective range of more than six to nine processors. And in all cases, the benchmarks show a much better performance than the rule of thumb predicts.

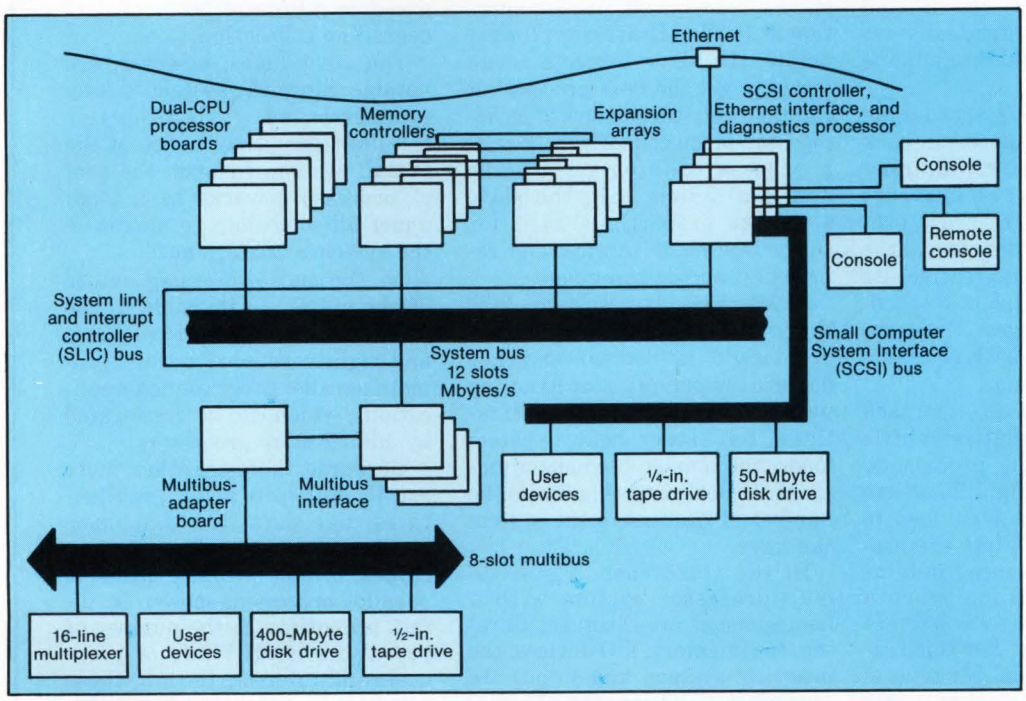


containing three VLSI parts: a 32-bit CPU, a hardware floating-point accelerator, and a paged virtual memory management unit. Two such subsystems are on one circuit card (Fig. 2). The fully 32-bit CPU and the floating-point accelerator suit technical applications, which tend to stress 32-bit operations and address calculations. The paged memory management, which handles a fully associative translation look-aside buffer and a two-level page table, accesses up to 16 Mbytes of virtual memory space for each process.

Each processor also contains a cache memory for near-zero wait states and minimized bus traffic. The two-way set-associative cache consists of 8 kbytes of very high-speed memory and stores recently accessed instructions and data. In this way, subsequent requests for the same data are satisfied from the cache, rather than main memory, to conserve bus and memory bandwidth. The cache takes in 8 bytes, a trade between hit rate and bus traffic that affords an effective hit rate of 95%.

Cache takes brains

Designing a cache for a processor pool architecture is difficult for several reasons. Since data in each cache represents a copy of some data in the primary memory, it is important that all copies and the original remain the same, even when a cache is updated. To ensure that, the new computer employs a write-



1. An extensible multiprocessor computer, the Unix-based Balance 8000 centers on a high-speed 26.7-Mbyte/s bus. Plugged into the bus are one to six dual-NS32032 processor boards, at least one memory controller, and at least one I/O controller.

Cover story: Multiprocessor computer

Getting everyone into the pool

The concept of multiprocessing embraces a full spectrum of structures that range from loosely to tightly coupled (see the figure).

Multicomputers, or specialized-function multiprocessors, encompass I/O controllers or data-acquisition subsystems whose processor boards often include special-purpose hardware. But the term "multiprocessor" may more classically be applied to general-purpose systems consisting of two or more processors of equal capability. This definition, however, covers at least three different structures: coordinated job scheduling, master and slave scheduling, and homogeneous scheduling.

In coordinated job scheduling, a loosely coupled approach, each processor is relatively autonomous. Each has its own interrupt system and storage. Each processor also has its own copy of the operating system and receives its job load from a centralized scheduling-policy manager. Once assigned, a job stays with the same processor until it ends.

One advantage of this approach is that there is relatively little coupling among the processors, simplifying the design. But there are significant disadvantages to this approach, too. First, the processing load is balanced only at the beginning of a job, when a user logs on, making the balance relatively inflexible. For this reason, it is not unusual for several users to experience poor response even when a processor within the group sits idle.

Other short-term resource imbalances are also possible, such as a memory shortage occurring in one processor while a neighboring processor has memory to spare. Also, it is not possible to employ processors concurrently to speed up a single application, as is often needed for technical tasks.

In a master and slave scheduling, a tightly coupled approach, all memory is accessible to all processors, but one processor is distinguished (usually by the software) as a master while all the others are slaves. The master maintains all of the system structures and schedules the work of all the slaves. Slaves, however, are limited to executing only user code while the master handles both user and supervisory code.

In a dual-processor, master-slave, Unix-based implementation at Purdue University, for example, the slave inspects a run queue to get the next process but can take only those marked as being user-mode code. Even then, if a process running on a slave makes a system call, the slave stops the process, marks it for supervisor mode service, and reinserts it on the run queue.

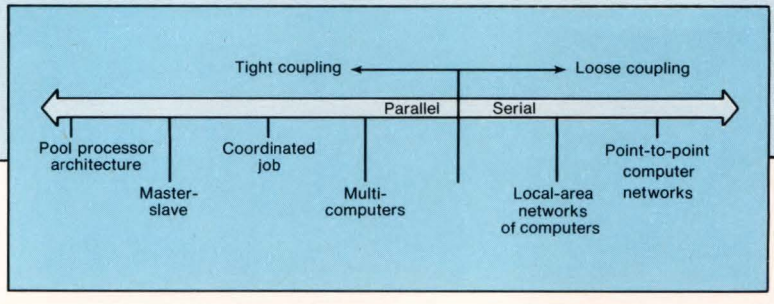
Master and slave systems, like the previous approach, are relatively easy to implement, and they do have the potential for handling parallel-programmed applications. But under heavy system loads, the master becomes a major bottleneck, and this limits the number of processors the system can have.

In the third case, a general multiprocessor system with a homogeneous architecture, all resources (memory, I/O devices, the interrupt system, and so on) are accessible to all processors. Resources are dynamically assigned to processes and not hard-wired rigidly to a processor. In this form of tightly coupled multiprocessing, a process scheduler assigns processors from a pool, earning it the name of processor pool architecture. Also, if the number of processors may be changed at need, it then is known as a scalable processor pool architecture.

The principal drawback of this approach is the difficulty of implementing it. The operating system must be carefully designed to ensure that mutual access is properly synchronized and, where necessary, excluded. In addition, the hardware must be carefully balanced to minimize performance-degrading contention.

The advantages, however, are notable. Since the system is fully symmetric, no single processor can limit the performance of the overall system. Instead, the pool of processors works as a team under all conditions to maximize the system's performance.
Also, the multiprocessing nature of the system is invisible to the user, while its shared resources and tightly coupled nature promote parallel programmed applications, which can be accelerated by adding more processors.

Of course, there are other, more exotic multiprocessor architectures, like data-flow machines, transputers, and inference machines, which promise massive parallel processing power in direct proportion to the number of processors used. While of great academic interest, though, these machines suffer from revolutionary architectures that are incompatible with existing von Neumann-based software.



through mechanism, in which each write cycle goes through to the bus and memory, in addition to updating the appropriate cache.

In this way, the write-through mechanism keeps the primary memory up to date with the caches on each processor. But what keeps the individual caches consistent among themselves? If two processors have both recently read the same data into their respective caches, and one of them updates its cache, what will keep the second processor from using its now stale data?

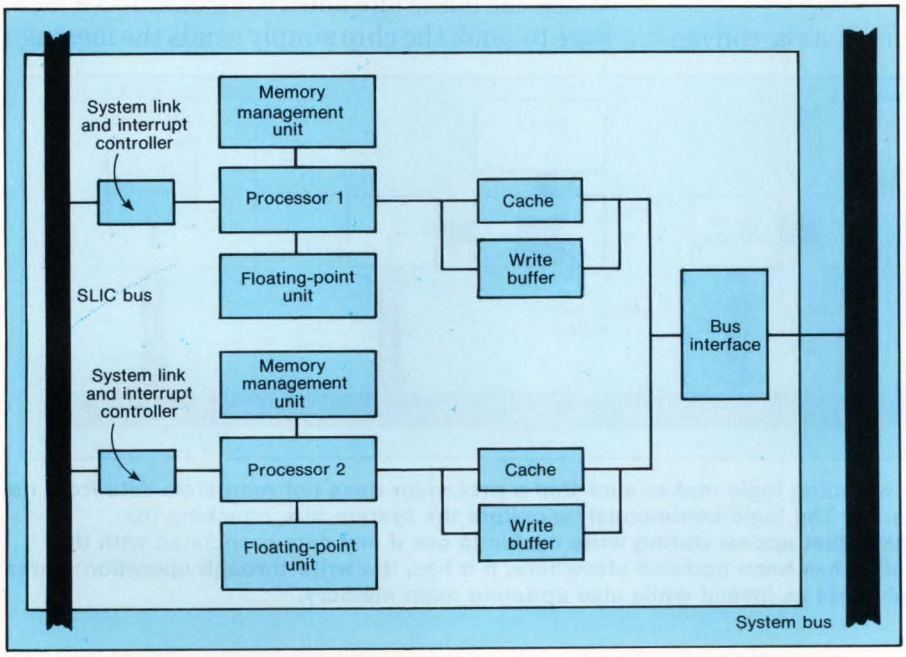
The answer is found in each cache's bus-watching logic (Fig. 3). This logic continuously monitors all write cycles on the bus and compares addresses with those in its own cache to see if any writes affect its own contents. When such an address appears, the cache invalidates the entry in question.

Also, although write cycles typically make up only 10% to 15% of the processor cycles, a processor could still waste precious time waiting for the completion of a write cycle. To avoid needless waiting, a write buffer relieves the processor of the write operation's address and data, letting it proceed while the buffer waits for the memory cycle to complete.

A SLIC chip

The last component of the processor subsystem is a custom IC, the System Link and Interrupt Controller, or SLIC. A SLIC appears with every processor in the system, as well as on every memory controller, I/O channel, and bus controller board. Communication between SLICs is accomplished with a simple command-response packet carried over a dedicated bus.

The controller serves several functions. First, it is the key element of the system's global interrupt system. Device interrupts are broadcast over the controller's bus as a packet. When that happens, the chips arbitrate among



2. Each processor in the pool is a subsystem containing three VLSI components: a 32-bit CPU, a hardware floating-point accelerator, and a paged virtual memory management unit.

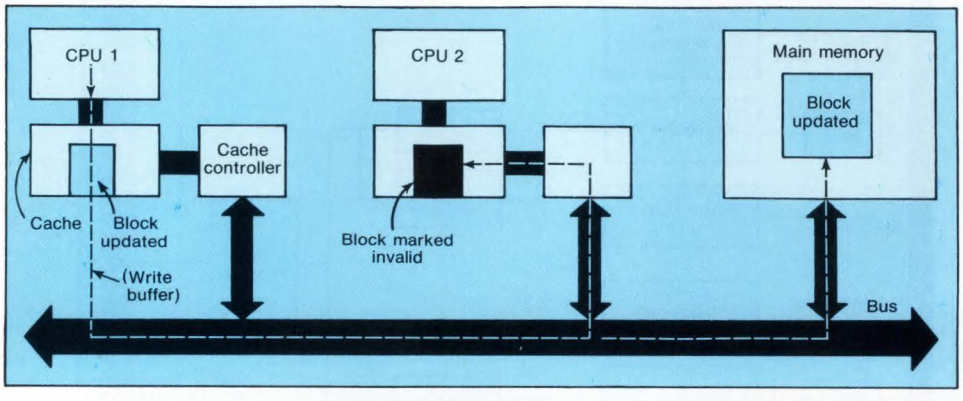
themselves on the basis of the priority of the processes running on their companion processors. The SLIC whose processor is executing the lowest-priority job at the time transforms the packet into an interrupt for its processor. With this mechanism, neither device interrupt signals nor device drivers are bound to particular processors, and only the lowest-priority processes are ever interrupted.

Cache of semaphores

A second function of the controller is to manage a cache of single-bit unit-semaphores. Such semaphores exclude access to a processor; in fact, all high-level exclusion and synchronization facilities involving the operating system are based on this function. Moreover, since each processor's SLIC is on the local bus, access to the chip does not incur any system bus cycles. As a result, spin-locks, which repeatedly request access from a SLIC semaphore, never waste bus or memory cycles.

Finally, the controller serves as a convenient communication path among modules. For example, system diagnostics and debugging routines take modules on and off line using the SLIC bus, which carries error management information. Also, the controllers note the power-up codes of modules and record their presence in an auto-configuration table accessed by the operating system. As a result, when the user plugs in a new circuit board, the system automatically reconfigures itself to include the new board without switches, wire-wrap stakes, or jumpers.

The circuit combines the functions of a serial receiver, a contention resolver, a transmitter, an interrupt controller, a semaphore cache, parallel I/O ports, and a processor interface (Fig. 4). It is implemented using a 3-μm CMOS process with gate-array technology and comes in a pin-grid array. The SLIC bus is a two-wire, bit-serial wired-OR bus that facilitates the distributed self-arbitrating access mechanism. When the bus is idle and a controller has a message to send, the chip simply sends the message



3. Bus-watching logic makes sure that a processor does not read stale data from its own cache. The logic continuously monitors the system bus, checking the addresses that appear during write cycles to see if any data associated with its own cache has been updated elsewhere. If it has, the write-through operation marks the stale data as invalid while also updating main memory.

over the bus. If it collides with another message, the lowest-priority one backs off to try again later.

A bus's burden

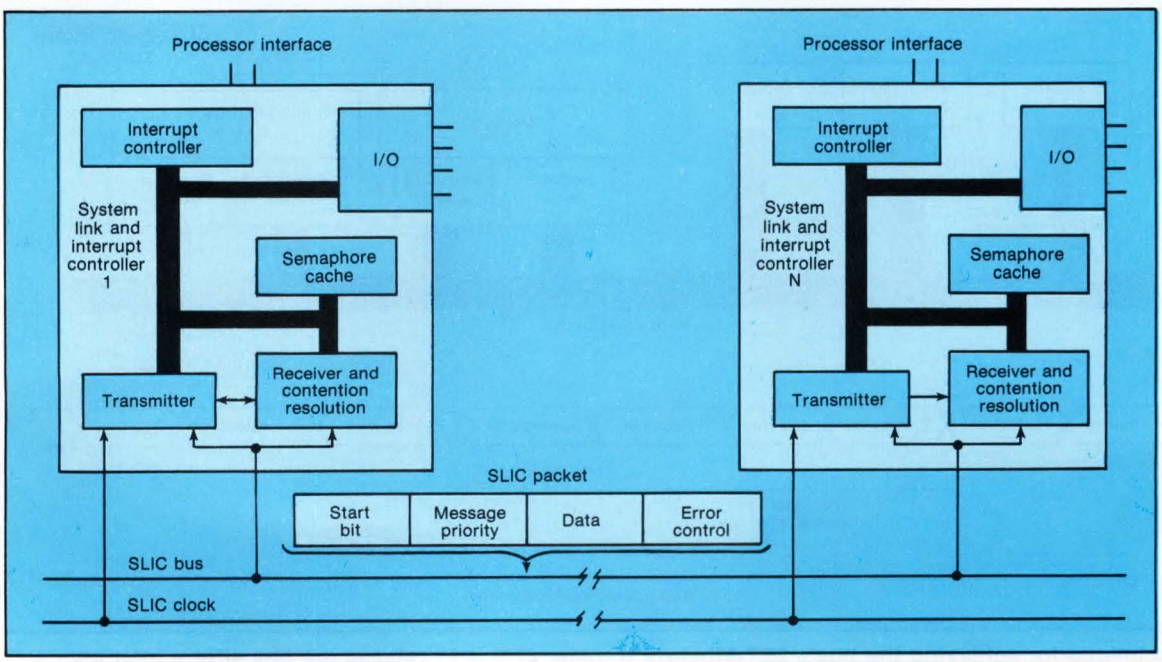
Obviously, the system bus for a scalable processor pool architecture machine is a critical element. It must provide software-transparent, symmetrical access between all processors and the system resources, including I/O subsystems of widely varying access times. And it must do so with careful regard to the high bandwidth required by the 32-bit CPUs. Yet, for the sake of economy, it must also have minimal interface complexity.

The Balance 8000's system bus achieves these goals through a combination of techniques. For example, a single, global 10-MHz synchronous bus that interconnects all processors to all other resources supplies the required symmetry. The bus yields the necessary performance with a 32-bit parallel time-multiplexed address and data path, as well as a set of control paths. The combination of time-multiplexing and Fast TTL circuits helps keep the bus interface circuitry, including transceivers, to fewer than 20 ICs.

A multiple pipeline protocol with multiple 4- or 8-bit fixed-length packets up to 8 bytes long helps to maintain the bus's bandwidth. To spare the primary storage pipelines from the possible long latency of serving relatively slow I/O buses such as Multibus, separate pipelines have been assigned to serve reading, writing, and I/O requests.

As a result, the protocol splits responses from requests so that the bus is only tied up for those cycles needed to transmit the request and response information. The storage access itself causes no bus delays and instead occurs in parallel with the traffic from other requests and responses. Moreover, the write response has its own dedicated set of wires on the bus and so happens "out of band." This frees the main 32-bit data path for more traffic.

As an example of the bus's parallelism, sup-



4. A SLIC (System Link and Interrupt Controller) chip accompanies each processor, memory controller, I/O channel, and bus coupler in the system. It provides a global interruption system, manages the cache semaphores, and establishes a packet-based communication link among the system's modules.

pose that processor P_1 sends a 1-byte request destined for the Multibus (Fig. 5). It takes only one 100-ns cycle to transmit and enqueue the request on the Multibus coupler. Next, processors P_2 and P_3 both transmit 8-byte read requests to the primary storage in the following bus cycles, after which the bus is again free for traffic.

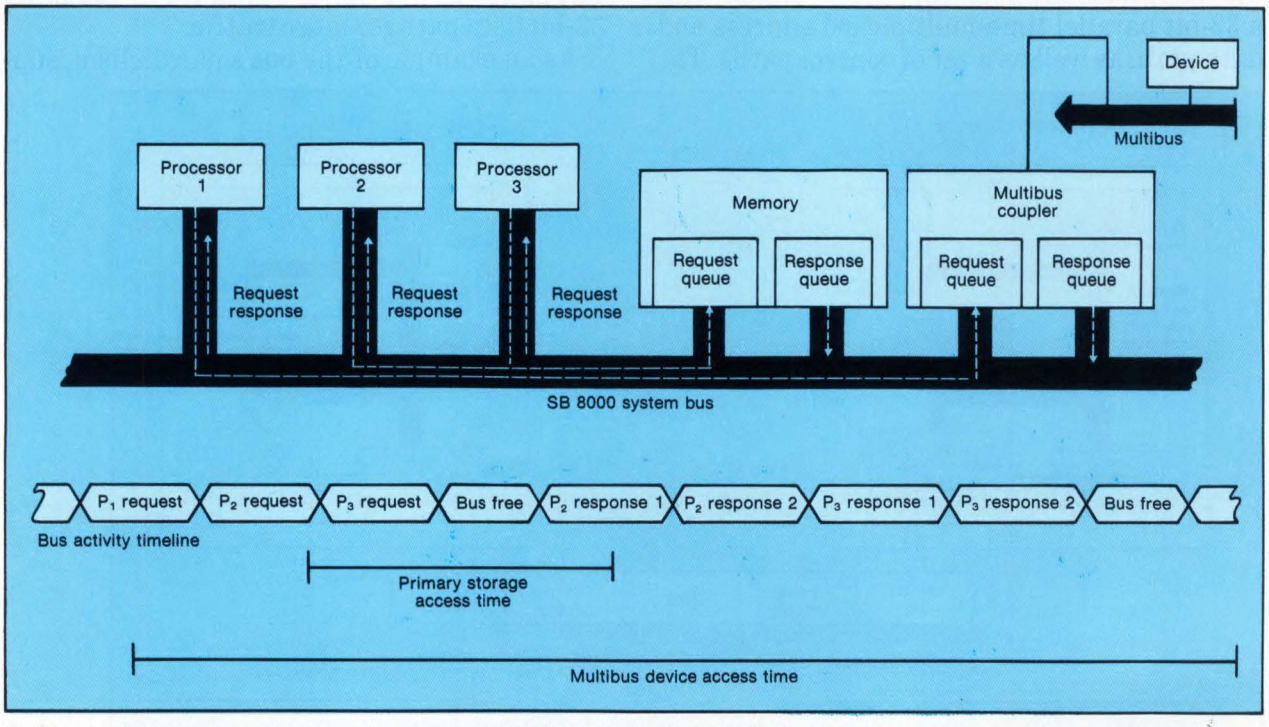
Then, when the 8 bytes of data requested by P_2 are available, the storage controller takes two bus cycles to return those 8 bytes of data to P_2, followed immediately by the two bus cycles needed to return 8 bytes to P_3. The bus is then free again until some time later when, depending on the speed of the addressed Multibus device, the Multibus coupler obtains its data from the device and uses the bus to respond to processor P_1.

Since the bus traffic is decoupled from the main-storage access, the bus can be accessed with the most efficiency. This decoupling, along with the fact that the memory controllers can be interleaved, results in a sustainable bandwidth of 26.7 Mbytes/s out of a theoretical maximum of 40 Mbytes/s.

Resolving problems

Beyond bandwidth considerations are the issues of bus arbitration, congestion, and control of and recovery from errors. To address these problems, the system employs a central multi-level arbiter. It has multiple priority levels to serve mechanical mass storage devices whose performance would suffer if their data transfers were not accepted in real time.

All processors share a given priority level as well, and within that level the arbitration circuit guarantees fairness. This is important because it ensures that, even under a very heavy load, there is no condition that would deprive a



5. One technique for achieving the bus's 26.7-Mbyte/s transfer rate is to release the bus after a memory request without waiting for a response, so that the bus is occupied only for the cycles needed to transmit requests and response information. Requests and responses are queued until the bus is free.

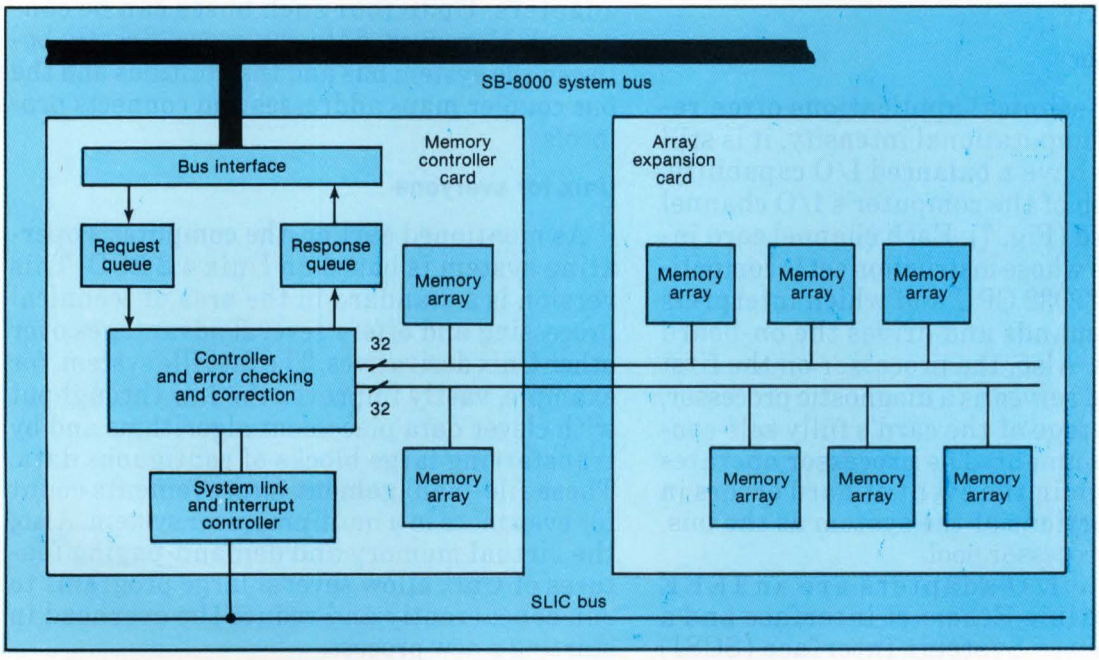
given processor of bus access. This in turn prevents deadlocks or intolerable degradation in performance.

A related issue for split-response protocol is that of managing congestion and controlling the flow of queue requests. Instantaneous heavy loads on the bus can fill up the request queues of the responders. In some systems, the flow control mechanism uses a negative acknowledge (NAK) response to keep those queues from overflowing. However, such a system can degrade from excessive request and NAK cycles. In the Balance 8000, however, each requester stores status information about each relevant queue. Requests are not propagated onto the system bus unless they are guaranteed a slot in the address queue. Therefore, even under heavy loads, each and every bus cycle is used productively.

Controlling and recovering from errors is always a difficult issue, but even more so in a multiprocessor system where there are many contenders for the bus and a high degree of concurrency. The system's bus checks for parity and uses other error-checking schemes. Whenever a serious error occurs, the hardware records the identity of each party involved and then freezes the bus so that the error does not create further trouble. Next, a diagnostic processor takes control and, through the link and interrupt controller chips, investigates the problem. Typically, recovery software will reset the computer, run selected confidence tests, disable the faulty module, and reboot the system on the remaining hardware.

Memory matters

In a scalable processor pool architecture, the single global memory is the center of the universe. It stores all resident code and data and



6. A pipelined packet bus and 8-byte transfers help maintain the high bandwidth needed by the global memory in the multiprocessor system. Requests arrive from the bus interface and are stored in the request queue, while responses queue up and await access to the bus. At the same time, the controller cycles the 64-bit-wide arrays to access data and check errors.

must satisfy all requests that are not met by the local caches. Therefore, a high bandwidth for the memory is critical.

To do its job, the central memory uses a pipelined operation and a memory controller, which together sustain a data transfer rate of 8 bytes every 300 ns (Fig. 6). Memory requests arrive from the bus interface and are stored in the request queue. At the same time, the controller can cycle the 64-bit arrays to access the data and generate and check error-correction codes. Also in parallel is the response queue which returns responses to previous requests.

In addition, the SLIC circuit on the memory controller card is used to report any error information and identify a memory module and its configuration to the auto-configuration software. It also allows that software to set attributes on a memory controller card, like a base address and the number of controllers to be interleaved.

I/O reaches out

Although technical applications often require sheer computational intensity, it is still important to have a balanced I/O capability. This is the job of the computer's I/O channel processor card (Fig. 7). Each channel card includes a 32016 whose instruction set is compatible with the 32032 CPU and which interprets channel commands and drives the on-board I/O adapters. Also, the processor on the first channel board serves as a diagnostic processor, taking advantage of the card's fully self-contained environment. The processor operates normally even in the event of hard errors in such vital portions of the system as the bus, memory, or processor pool.

Among the I/O adapters are an IEEE 802.3-compatible Ethernet interface and a Small Computer Systems Interface (SCSI) mass storage bus. This emphasis on industry standard interfaces makes it easy for the OEM to mix and match from among the growing set of compatible mass storage devices. The system's software device driver also benefits, accommodating a wide range of disks without modifications.

In order to peak the I/O's throughput, the system employs individual FIFO "surge" buffers and direct memory access controllers that are designed for 8-byte transfers. Using surge buffers instead of a conventional RAM to buffer bursts of data from an I/O device minimizes the delay between the data's arrival and its updating of the main memory.

The I/O channel processor board is designed to sustain both (Ethernet and SCSI) adapters at once. Its high transfer rate and ability to gather scattered data into consecutive memory locations make it an excellent match for the large disk transfers used in Unix 4.2 BSD's fast file system. Since the system supports up to four such I/O channel boards, the designer has the capability to balance the I/O bandwidth to match the computational bandwidth for a given application.

The computer system's IEEE-796 (Multibus) bus conveniently obliges an OEM who wants to add custom hardware or put in one of the many Multibus-compatible, special-purpose I/O adapters. Up to four such buses can be connected. Moreover, data can move directly between the system bus and the Multibus and the bus coupler maps addresses and connects protocols.

Unix for everyone

As mentioned earlier, the computer's operating system is based on Unix 4.2 BSD. This version is a standard in the area of technical processing and offers several advantages over other Unix derivatives. The fast file system, for example, vastly improves the I/O throughput with clever data placement algorithms and by transferring large blocks of contiguous data. These file-management improvements count for even more in a multiprocessor system. Also, the virtual memory and demand-paging features of Unix allow several large programs to run concurrently and reduce the overhead in starting a new process.

In addition, the 4.2 BSD version takes advantage of the proven DARPA (Defense Advanced Research Projects Agency) standard TCP/IP (Transmission Control Protocol/Internet Protocol) to facilitate integrated and heterogeneous network services. Some examples are remotely transferring files, logging on, or executing commands.

Much of the power and elegance of Unix is in its concise syntactical notation and support for

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TI TMS 320 DSP MICROCHIP

consists of a 500 page, tutorially-orientated text and programming/users' manual; more than 50 tested FORTRAN, MACRO-11, and TMS 320 programs in machine readable DEC or MS/PC-DOS source floppy format; and a powerful TMS 320 cross assembler. Of course, all TMS 320 cross assemblers can assemble TMS 320 code! But, only *DSPS-Macro*, because it runs under *MACRO-11* or *Microsoft Macro*, allows the user to invoke the powerful *repeat* [.REPT], *concatenation* ['], and *numeric conversion* [\] operators for *user* macros. The following examples vividly demonstrate what these capabilities buy you in terms of ease of generation of time-efficient '320 code such as DSPS' FFT's, with 64/128/256 complex point transforms executing in 0.53/2.4/6.1 msec.

128'th Order FIR Filter: Only two short macros and a 5-line repeat sequence generate the complete nucleus of a 128'th order, 400 nsec-per-tap, finite impulse response filter, assuming that a file containing COEF 1,*c*1; COEF 2,*c*2; . . . COEF 128,*c*128 (where the *c*'s are scaled, 13-bit integers) has been generated by any high level language filter design package, such as those in the *IEEE Programs for DSP* book:

```
.MACRO COEF I,J          .MACRO TAPGEN I          I = 128.
CF'I = J                 LTD  *-                  .REPT 128.
.ENDM                    MPYK  CF'I               TAPGEN  \I
                         .ENDM                    I = I-1
                                                  .ENDR
```

What could be simpler?

Variable Shift of a 32-bit Integer, plus Exponent Adjustment: In TI's *Floating-Point Arithmetic* DSP Application Report, the 30 required subroutines occupy about 10 pages of code (over 400 source lines) vs. only 1 page of code (about 50 lines) required for *DSPS-Macro*. Although both programs assemble into the same amount of object code, the compact DSPS approach is easier to write, debug, and maintain, and results in a much smaller and thus more readable source program.

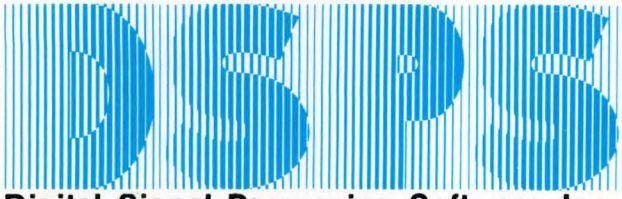
10'th Order Leroux-Gueguen LPC Matrix Inversion (included in our package): The lack of indexed data addressing on the TMS 320 makes our *autogen* technique both attractive and realistic for programming "non-array-like", looped algorithms involving indexed data access. In the L-G program, about 60 lines of clear, readable, "looped" code — which reflect the structure of the original FORTRAN prototype program — generate about 600 lines of TMS 320 in-line code which execute in 300 *u*sec (including 10 calls to divide): nearly 3x faster than a leading $50,000 floating-point array processor. The alternative, a "looped-at-run-time" version, would execute more than twice as slowly. *And, writing a correct in-line version manually would be very difficult indeed, and totally inappropriate in view of the power of DSPS-Macro.* Similarly, in our 535 *u*sec *64 complex-point FFT (DSPS-2)*, about 150 source statements — which again echo the structure of the FORTRAN prototype — expand into 2900 lines of object code, with all control, addressing, and trig coefficients absorbed into the code at assembly time.

And, **DSPS-Macro** allows use of other powerful features such as conditional assembly, macro nesting, and macro calls within macro definitions (including recursion). Finally, while we guarantee that *DSPS-Macro* assembles TMS 320 code correctly, DEC and Microsoft guarantee the long-term support, stability and availability of the *MACRO-11* and *Microsoft Macro* "supervisors".

BOOK CONTENTS/REVIEW

• Digital Signal Processing Algorithms & General Purpose Computers • PDP-11 & Macro-11 Assembler • Structures For Control, Data Access & Data Manipulation • Compilers, Computers, & High-Level DSP Software • Systematic DSP Programming & DSP Systems Programming • TMS 320 DSP Microchip: Architecture: instruction set; address modes; page, pointer, and data manipulation. Arithmetic sequence programming: data and coefficient scaling; addressing and instruction ordering strategies; utilities. Modular programming: subroutines and argument passing, case branch, threaded code, interrupt service routines, memory overlays. Input/output. Data and coefficient scaling techniques. Time/space tradeoffs via *autogen*. DSP case studies: A/D, D/A, *u*law mapping, windowing, FFT butterfly, convolution, biquad filter, modems, square root, software sine & divide. LPC: limited-memory, 32-bit autocorrelation (3 msec for 200 point, 10 lag); L-G matrix inversion (300 *u*sec for 10'th order); lattice speech synthesis (20 *u*sec/point, 10'th order); pitch detection. Comparative performance: TI vs. Fujitsu vs. J-11. Software development systems: Software emulators. MACRO-11 and MS-DOS cross assemblers; TI EVM board/host communication. Next generation TMS 320. **A Tale of Two Architectures: PDP-11 vs TMS 320 • The Future: New Technologies •**

The reviews are now in on our DSPS-3 package; in the Jan/Feb 1984 issue of *Speech Technology*, Dr. E. Randolph Cole at the Information Sciences Institute, U. of S. California, states: "People developing software for the TMS 320 . . . should not be without this book and the accompanying software",** "the software is a bargain for those who can use it", "the techniques of real-time software writing are the strength of the book", and "we're talking about powerful real-time software here", and "this is the clearest, most concise tutorial on the TMS 320 I have seen anywhere". We appreciate Dr. Cole's remarks, and we know that the hundreds of copies of the DSPS-3 book and software now in the field have easily saved their owners the purchase price in the first week or two of software development on the TI TMS 320.



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CIRCLE 82

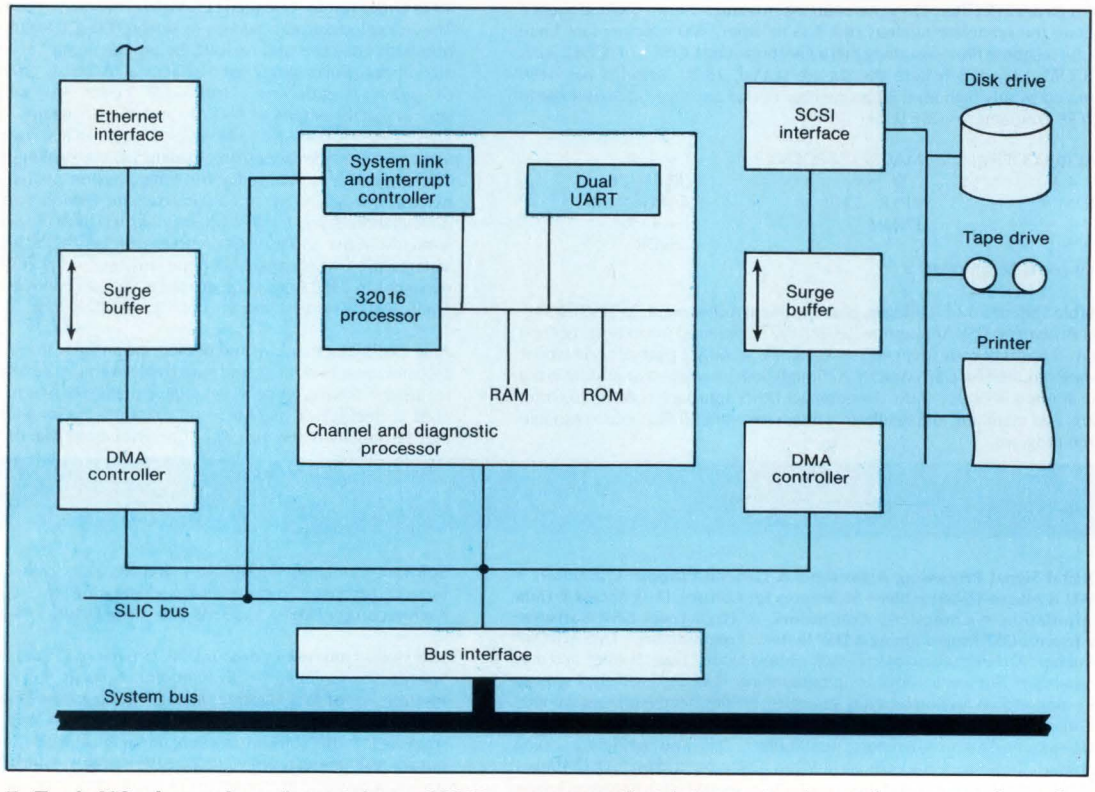
multiprogramming. Unix encourages the programmer to construct applications by piecing together collections of smaller programs; these are interconnected by a simple inter-process communications (IPC) facility: the pipe. A pipe connects the output of one program to the input of a second, whose output goes to the input of a third program, and so on.

The IPC facilities of Unix 4.2 BSD extend to include a so-called socket-based message-passing mechanism. Rather than doing everything in a large monolithic program, this philosophy advocates smaller, simpler, and easily reused programs all communicating through the IPC facilities.

Unix also encourages multiprogramming at the human level. With the simple shell command-language syntax, a user can invoke one or more processes and have them run in the background simply by terminating the command with an ampersand (&). Alternatively, the user can invoke several communicating process simultaneously by using the pipe syntax "½."

Done with mirrors

On a single-processor computer, apparent concurrency is not real, since the processes are multiplexed (time-sliced) through a single processor. However, on a multiprocessor system with a processor pool architecture, the pool of symmetrical processors will execute the pro-



7. Each I/O channel card contains a 32016 processor that interprets channel commands and drives the on-board I/O adapters. The processor on the first channel board also serves as a diagnostician; it can operate normally even if hard failures befall the system bus memory or processor pool.

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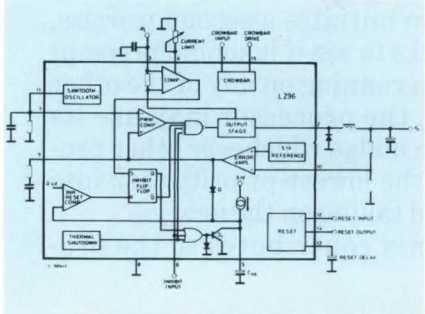

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In addition, the L296 includes more control/protection functions, while requiring fewer external circuits. For example, only one capacitor and one resistor are needed for the device's reset circuit to provide a signal to the microprocessor. Plus, with most other switching regulators, an external current limiter must be added; this function is standard in the L296. Soft-start, internal precision reference and overload output protection are also part of the high performance L296 package.

To date, millions of L296 switching regulators are on the job in a host of products including monitors, printers, personal computers and typewriters. The SGS device is in demand because of its exceptional power and its proven track record. In short, the L296 is simply the logical choice for engineers who can't afford to gamble on their power supply design.

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Characteristic	Rating	
Input Voltage	V_i = 7.5 to 50V	
Line Regulation	V_i = 10V to 40V Io = 2A	60dB
Load Regulation	V_i = 20V Io = 0.3A to 4A	60dB
Ripple Rejection	f = 120Hz	60dB

L296 evaluation kit now available from SGS.

The kit, which is available for immediate shipment, includes an L296, PC board and layout information as well as detailed application notes. To order, send a $10 check to SGS Semiconductor Corporation, Product Marketing, 1000 E. Bell Road, Phoenix, AZ 85022. Or call 602/867-6262.

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CIRCLE 83

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cesses in true concurrency, resulting in a multiplicative improvement in throughput.

This architecture, then, combines the benefits of Unix's existing application set with the scalable power of multiple processors. Simply adding or deleting processors changes the level of performance without a single software change.

Some changes needed

However, although the Unix philosophy is based on multiprogramming, the standard implementation is still based on a single-processor architecture. By implication, that would limit the operating system functions to one process at a time. In contrast, a processor pool architecture often accommodates several simultaneous processes executing within the kernel on several processors. For this the kernel needs to be fully sharable by multiple, concurrently executing processors.

The version of Unix ported to the Balance 8000, called Dynix, required modifications in four major areas: mutual exclusion, interrupt distribution, virtual memory management, and process scheduling.

On a single-processor system, mutual exclusion of processes from the operating system is achieved simply by disabling processor interrupts, therefore guaranteeing that no other process will get control until the interrupts are enabled. However, this technique is not enough to guarantee mutual exclusion for a processor pool multiprocessor, since other processors may be simultaneously executing processes via the kernel. The Dynix kernel, therefore, incorporates a more robust model of exclusion based on three mechanisms: gates, locks, and counting semaphores.

Gates and locks

A gate, the lowest-level mechanism, is implemented in the SLIC circuit and used only for routines where time is critical, since there are only a limited number of them available. A lock is a software version of a simple, non-queueing unit semaphore built over the gate mechanism; it is used when the requesting process cannot afford to "sleep" (lapse until notified) while waiting.

The highest-level exclusion mechanism is the counting semaphore, consisting of a counter and a waiting queue. Semaphores completely replace the conventional sleep-and-wakeup mechanism, providing more structure and eliminating unnecessary context switching. Semaphores are used by processes to avoid waiting for events or to hold the sought resource for a long time.

In a conventional Unix system, a single processor receives all device-interrupt signals. However, in a processor pool architecture, any processor can accept any interrupt signals. The resulting decrease in interruption latency is another improvement over single-processor systems.

If necessary, however, device drivers can avail themselves of the kernel lock and semaphore mutual-exclusion mechanisms to protect critical data. There is also a mode that emulates a single-processor system to simplify the porting of existing monoprocessor drivers to the new multiprocessor machine. Moreover, Dynix supports configuration at the object-code level, so users can add drivers and rebuild the kernel without the source code.

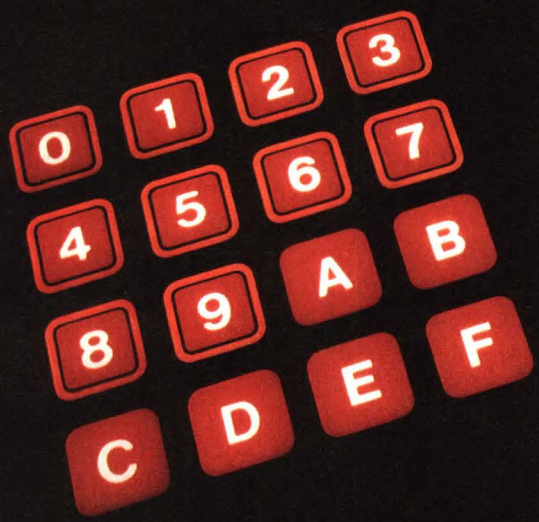
Spreading the work around

Process scheduling in Dynix is conceptually quite similar to that of conventional Unix. There is a single, priority-oriented run queue; since the system is fully symmetrical, any process can execute on any processor, whether in supervisory or user mode. As for priorities, the basic scheduling philosophy is to always run the highest-priority, ready-to-run processes first.

Dynix's global visibility minimizes the number of context switches that will result from system events. It works this way: a periodic interrupt causes the processor accepting it to determine if there is a process running that should be preempted by a higher-priority one in the run queue. Similarly, when one currently executing program initiates a second process, the processor checks to see if it should preempt any other program running on any of the other processors. If so, the processor may use its SLIC's software to nudge whichever other processor is running the lowest-priority task into rescheduling it and taking on the new job.

Obviously, Dynix contributes to the pro-

KEYBOARDS THAT GLOW IN THE DARK



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cessor pool architecture's ability to balance loads dynamically. As already mentioned, this is a function of the fact that all processors are identical and all code and data are equally accessible to all processors. There is no rigid binding of processes to processors, and there are no restrictions limiting the ability of processes to execute on any of the processors. In short, any process in an executable state can run on any processor.

To get down to specifics, the Dynix scheduler continuously monitors the set of ready-to-run processes and dynamically schedules the highest-priority ones so that each processor is always working on the most important job as long as there is work to be done.

Many applications

A computer of this kind opens up new application possibilities, the breadth of which is exemplified by two extremes: a multi-user, multipurpose network server, and a single-user, application-specific workstation.

At the first extreme, technical OEM applications require a broad range of distributed and centralized computing power, but the overriding requirement is that each user have full access to all the system's resources. In part, this means that a computer's files be fully available to dumb terminals, personal computers, and workstations alike.

A network server fits well into this scheme because it can manipulate the contents of a data base for the workstation, offer files and computing power to the personal computer, and provide all but display services to the dumb terminal. Moreover, the computational power required of the server depends on the size of the network. Here the scalable pool idea is a natural fit.

The multiple users will undoubtedly generate a large number of independent processes that will be transparently and dynamically scheduled by Dynix to run in order of priority on the available set of processors. Therefore, an increased throughput attributed to the two or more processors is available without the application designer expending any extra effort.

With this approach, the OEM can create a "product line in a box," offering a basic configuration that processors can be added to or subtracted from to meet the particular needs of the network. Similarly, the installed base of systems can be upgraded in the field, without software changes, by the simple addition of a processor card.

Workstation potential

At the other extreme, some individual applications are so computationally intensive that they justify the expense of their own dedicated, single-user workstations. Here the OEM needs to offer a low-cost starter system and the opportunity to add processing power later. In addition, the workstation must fit into a network with other, and probably different, computer systems, in order to conveniently share data bases.

One example has an image server as one node, a high-resolution film recorder as another, and a workstation demanding high-quality graphics. Here again, the pooled processor system is a powerful solution. The OEM can configure a low-cost starter system with only 2 processors, while offering to upgrade it to 12 as needed. And the high-performance graphics subsystem is easily connected to one of the industry standard I/O ports, like the SCSI bus; for the highest possible performance, it could go directly on the system bus.

In addition, most computationally intensive technical applications have a great deal of inherent parallelism that can exploit the power of the multiprocessor computer by making simple changes to a program originally intended for a one-processor computer. The ray-tracing algorithm used to realistically model and shade three-dimensional solids is a good example. The parallel computational paths are easily separable; a typical algorithm can be so modified in less than a man month. In many cases, the algorithm can even be designed to dynamically adapt to the number of available processors, thereby providing the convenience of self-configuring software, even at the application level.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543

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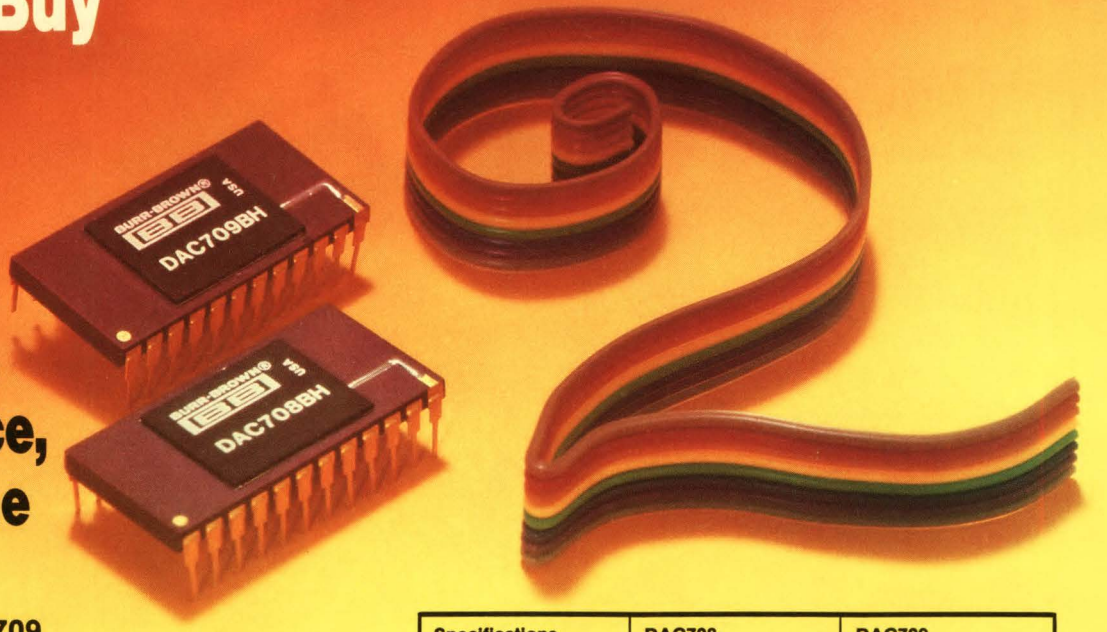

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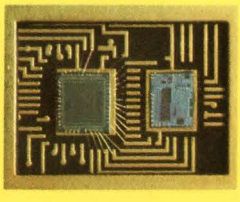

Specifications	DAC708	DAC709
Resolution	16 bits	16 bits
Bus Compatibility	8-bit parallel or serial	8-bit parallel or serial
Linearity error (max, over spec temp)	±0.003% FSR	±0.003% FSR
Monotonicity (min, over spec temp)	14 bits	14 bits
Gain Drift, max: BH KH	±15ppm/°C ±25ppm/°C	±15ppm/°C ±25ppm/°C
Settling to ±0.003% FSR	8μsec, max	8μsec, max
Output Range: Unipolar Bipolar	 0 to −2mA ±1mA	 0 to +10V ±10V, ±5V
Package	Hermetic 24-pin DIP	Hermetic 24-pin DIP
Price (100s): BH KH	$54 $44	$54 $44

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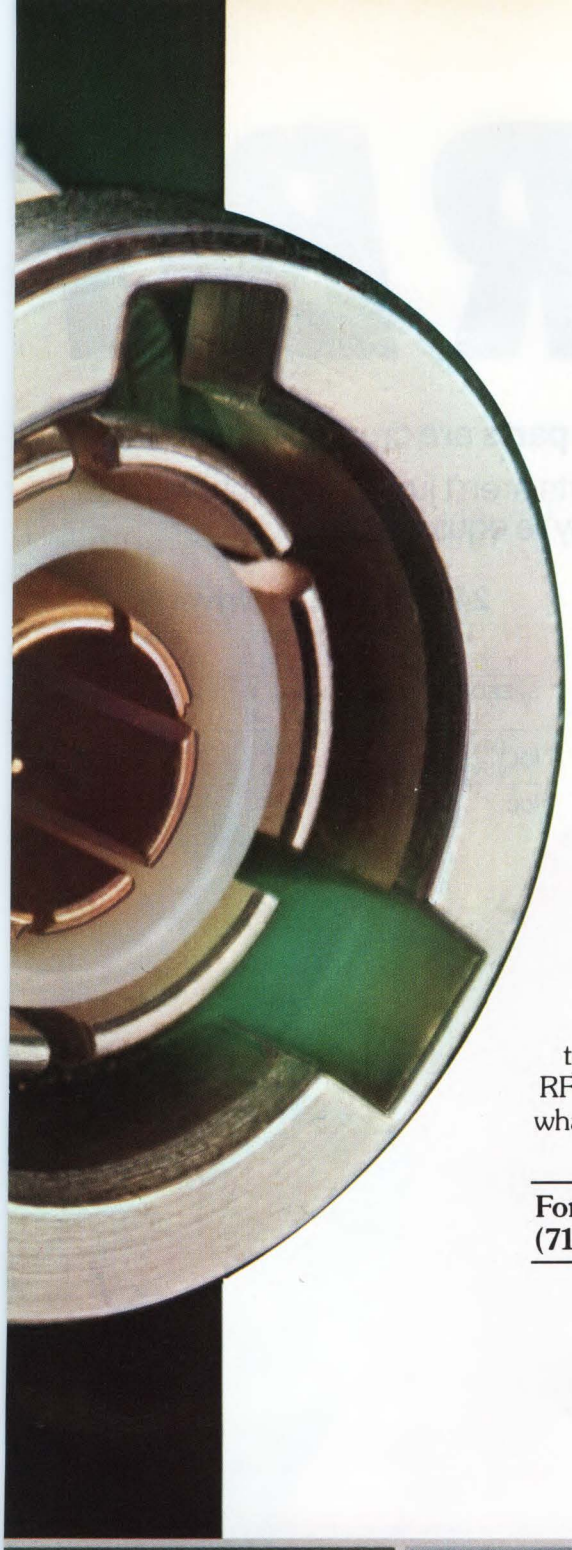

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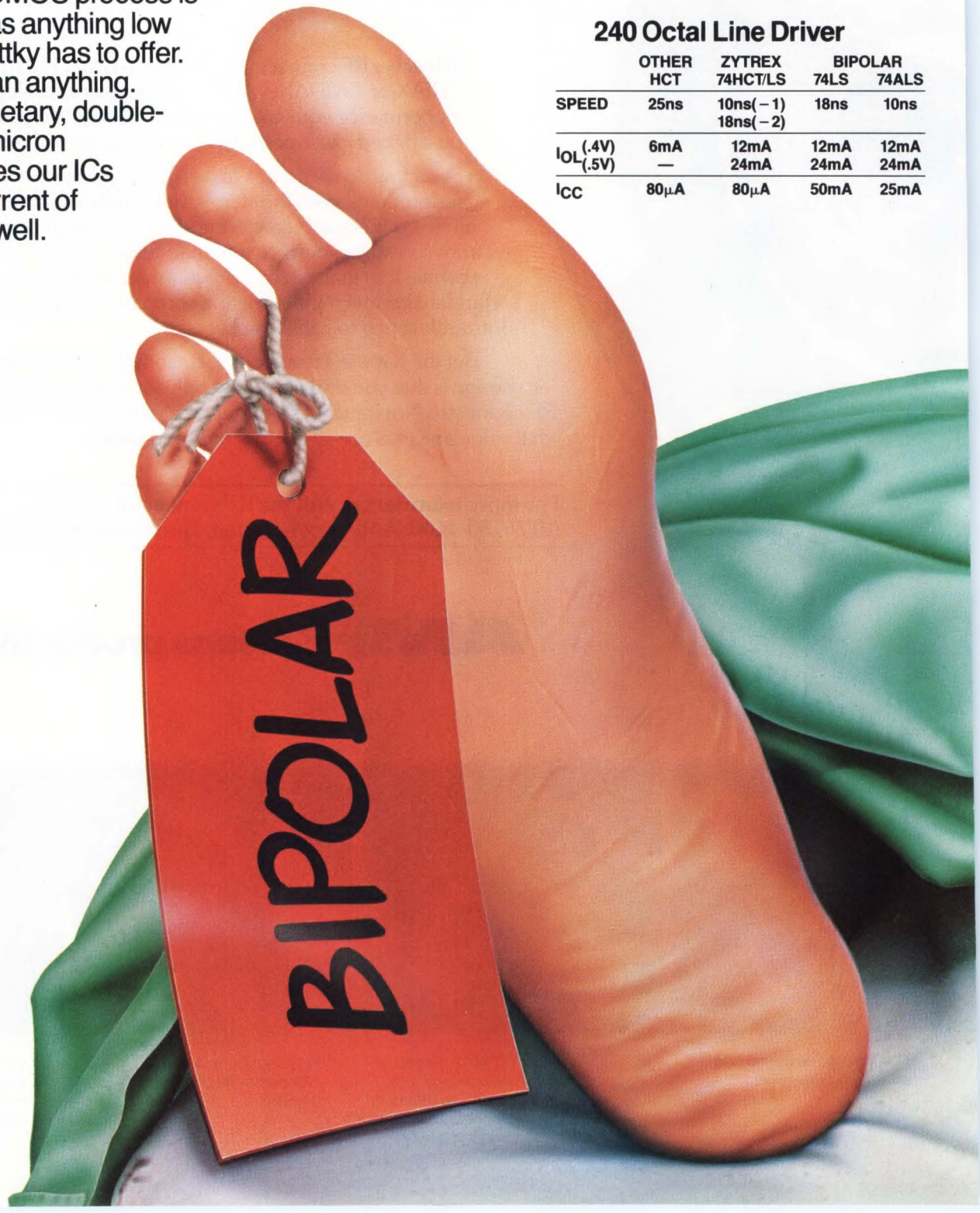
SPEED	25ns	10ns(−1) 18ns(−2)	18ns	10ns
I_{OL} (.4V)	6mA	12mA	12mA	12mA
I_{OL} (.5V)	—	24mA	24mA	24mA
I_{CC}	80μA	80μA	50mA	25mA



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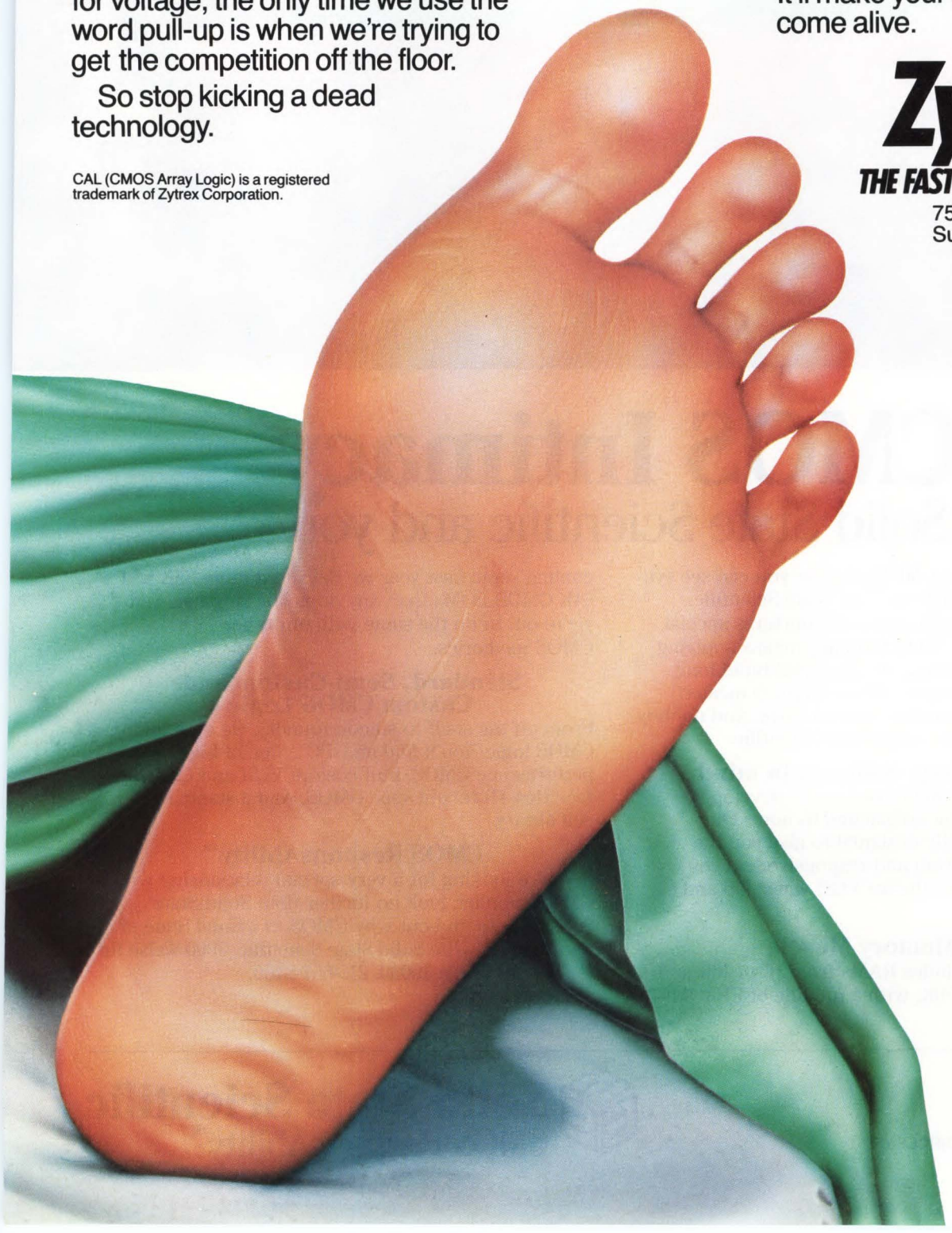
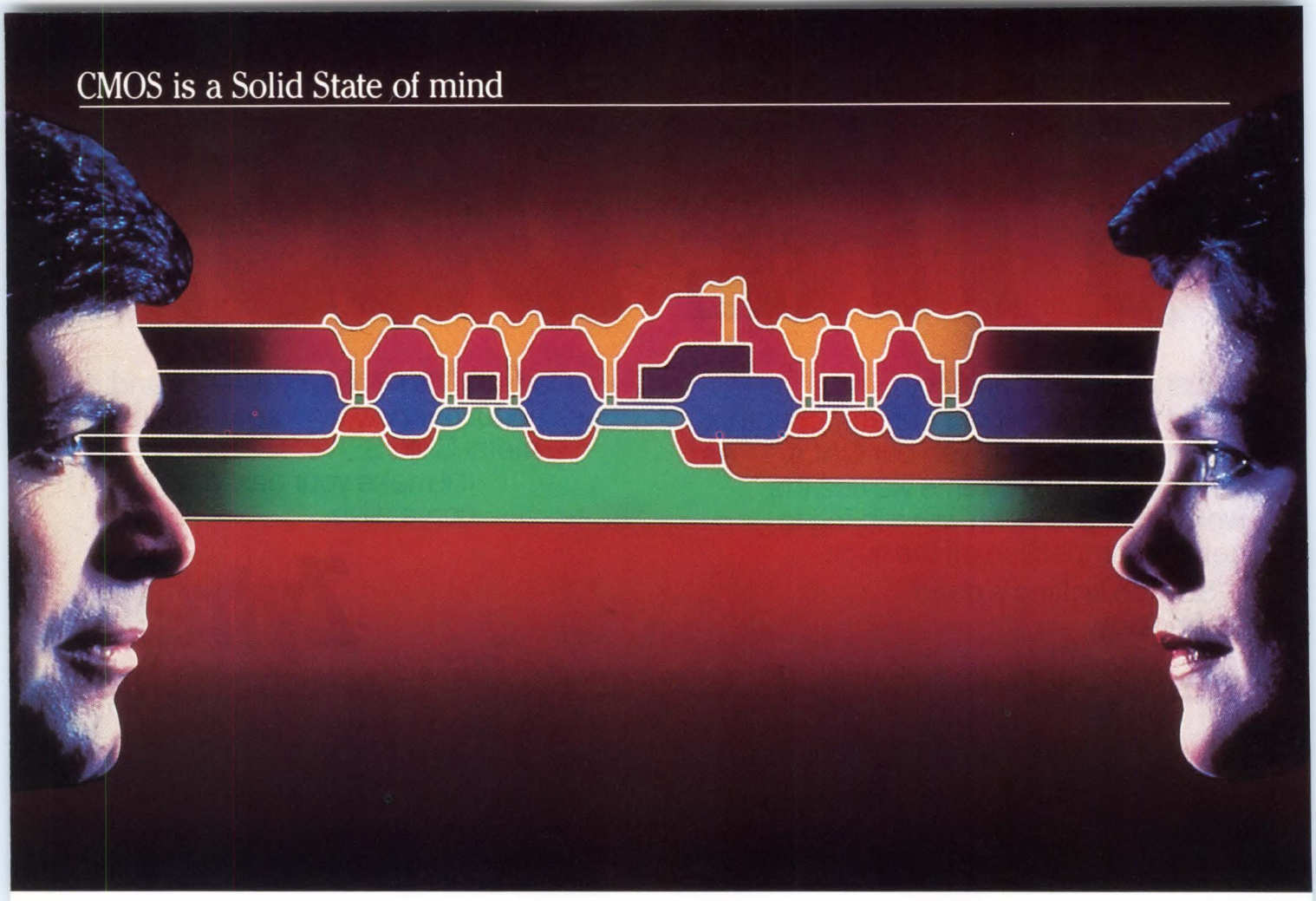


CMOS is a Solid State of mind



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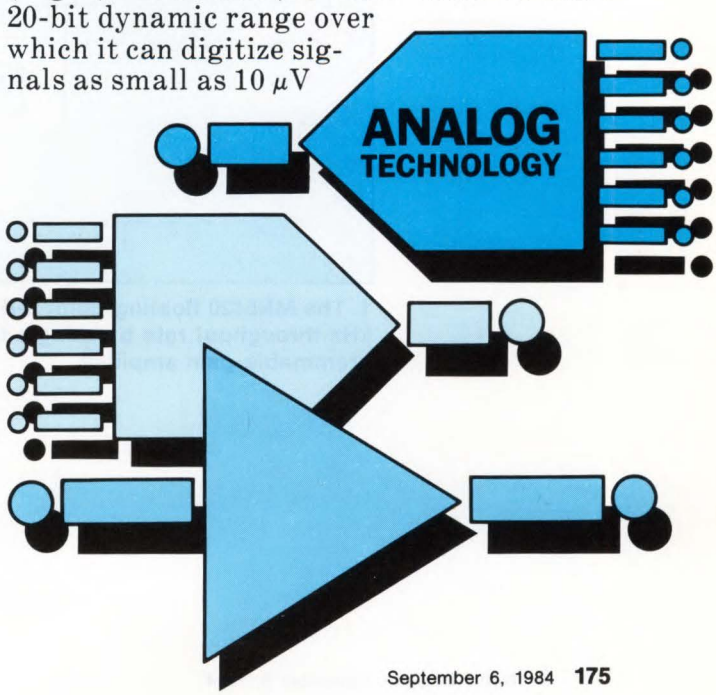
Floating-point converter uses hardware to get a 20-bit dynamic range

With hardware setting the gain of a programmable-gain amplifier, an analog-to-digital converter samples full-scale signals from ±20 mV to ±5 V at 320 kHz.

Digital signal-processing applications like radar and sonar systems often demand more of analog-to-digital converters than those devices can provide unaided. The signals not only span a wide dynamic range but their conversion may need resolutions of 16 to 22 bits at throughput rates approaching 1 MHz. Preconditioning circuitry, inserted between the signal source and the converter, is needed to adjust the signal to a converter's limitations with respect to aliasing effects, sampling rate, and dynamic range.

Nor do the difficulties end there. Although analog filters satisfy aliasing requirements, sampling, which is a function of conversion time and dynamic range limitations, is not as straightforward. Automatic gain control and software autoranging techniques, which have been used in the past to build floating-point a-d converters, have always compromised either sampling rate, or dynamic range, or both. The result is usually a loss of information.

The MN5420 floating-point converter solves those problems. It eliminates the need for preconditioning essentially by incorporating components like anti-aliasing filters and a programmable-gain amplifier (PGA) in the same module as a high-speed, 12-bit a-d converter (Fig. 1). As a result, it achieves an effective 20-bit dynamic range over which it can digitize signals as small as 10 μV



Richard Burrier and **Ross Mangiapane**, Raytheon Co.
Jesse Rhodes, Robert Duris, and **Chuck Sabolis**, Micro Networks

Richard W. Burrier and Ross Mangiapane are both principal engineers at the Bedford Laboratories of the Missile Systems Division of Raytheon Co. in Bedford, Mass. Each has made a significant contribution to the advancement of continuous-wave radar technology.

Chuck Sabolis, Robert Duris and Jesse Rhodes work for Micro Networks (a division of Unitrode Corp.) in Worcester, Mass. As manager of strategic planning, Sabolis is responsible for new product and long-range business planning. Duris joined the company in 1976 and currently manages the Advanced Engineering Development group. Jesse is a senior design engineer who has been with the company since 1981; his area of concentration is high-speed analog design.

Analog Technology: 20-bit a-d converter

and as large as ±5 V at a 320-kHz conversion rate (see "Floating-Point Dynamic Range Explained," opposite).

Two-part output

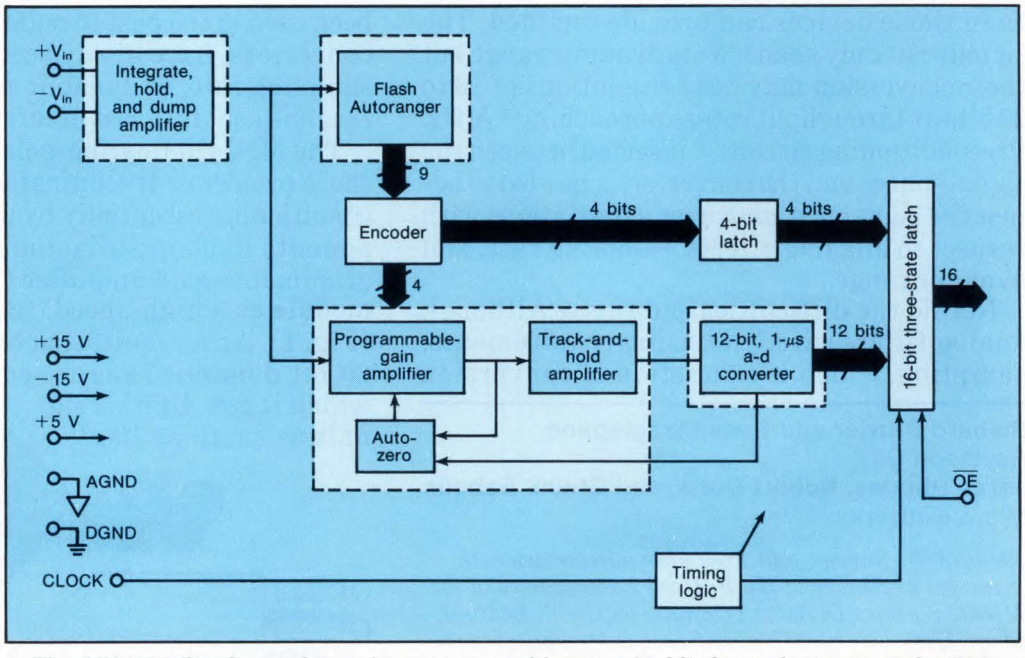
Like other floating-point converters, the MN5420 produces a two-part output consisting of a mantissa and an exponent. The amplifier's gain provides the exponent, and conversion at that gain provides the mantissa. But whereas other such converters use software to control the amplifier's gain, this one uses hardware (a 4-bit flash converter) to scale itself instantaneously to one of nine input-voltage ranges.

In contrast, a typical software-based scheme employs a microprocessor to observe the converter's output and adjust the amplifier's gain, ensuring optimal usage of the converter's full-scale range. It is an iterative process and often ties up both converter and processor for several conversion cycles.

Moreover, the MN5420 is designed to minimize spurious noise pickup, hysteresis (memory of previously encoded signals), gain-switching errors, and self-generated wideband noise. For all gain ranges, it has an absolute noise floor of below 50 μV rms and maintains a 66-dB signal-to-noise ratio (rms value of the input signal in relation to any spurious signal in the noise floor).

Do it the hardware way

In addition to timing, control, and logic circuits, the hardware-controlled floating-point converter contains five major blocks—a pair of track-and-hold amplifiers, a 4-bit geometric flash a-d converter or autoranger, a nine-range programmable-gain amplifier, and a fast (1-μs conversion time) two-step a-d converter with 12-bit accuracy—that is, no missing codes at 12 bits. The first track-and-hold amplifier (called an integrate, hold, and dump circuit) acquires



1. The MN5420 floating-point a-d converter achieves a 20-bit dynamic range and a 320-kHz throughput rate by using a flash converter on the front end to set the gain of a programmable-gain amplifier.

the input signal in about 1 μs (Fig. 2). It then passes into the hold mode and applies the held voltage simultaneously to the flash converter and the PGA.

The flash converter quantizes the input signal coarsely. Its output word both sets the PGA's gain and is latched into the three-stage output as the exponent. The PGA amplifies the held input signal and the second track-and-hold amplifier simultaneously acquires the amplified signal—the two events taking approximately 1.3 μs. The second track-and-hold amplifier simultaneously subsequently goes into the hold mode, and the 12-bit converter completes its task in approximately 1 μs. The total cycle time for a complete conversion is 3.125 μs.

The floating-point converter is designed to handle bipolar signals, and the 12-bit a-d converter produces an offset binary output word that is converted into a two's-complement word for the 12-bit mantissa. The flash converter, on the other hand, is an absolute-value circuit and produces its 4-bit output regardless of signal polarity.

Integrate, hold, and dump

What is the rationale for using a seemingly new circuit function on the front end of the MN5420, rather than a readily available high-speed hybrid or monolithic track-and-hold amplifier? Answer: the integrate, hold, and dump amplifier (Fig. 3) enhances the floating-point application with several unique features.

In conventional fast amplifiers, frequency components outside the band of interest can add unwanted in-band information. In one of its most important roles, the integrate, hold, and dump amplifier filters the input signal with a sin X/X function during integration. That action, similar to that performed by a single-pole, low-pass filter, desensitizes the a-d converter to high-frequency input noise and

Floating dynamic range explained

The term dynamic range, when used to describe a-d converters, has a number of definitions. In its simplest form, it is the ratio of the smallest signal it can detect (the value of its least significant bit, or LSB) to its full-scale input range, or FSR. A typical 12-bit a-d with a 10-V input range (0) to +10 V or ±5 V) has an LSB value of 2.44 mV, as shown by the equation:

$$1\,\text{LSB} = \text{FSR}/2^N = 10\,\text{V}/4096 = 2.44\,\text{mV}$$

where FSR = 10 V and N = 12 bits. Thus its dynamic range (DR) in dB is:

$$\text{DR} = 20 \log \frac{10\,\text{V}}{2.44\,\text{mV}} = 72.4\,\text{dB}$$

However, the MN5420 floating-point a-d converter has, when operating at the highest gain, an LSB equal to 9.5 μV:

$$\text{LSB} = \text{FSR}/\text{Gain}/2^N = 10\,\text{V}/256/4096 = 9.5\,\mu\text{V}$$

Its dynamic range in decibels according to this definition, based on a 10-V full-scale input range, is:

$$\text{DR} = 20 \log \frac{10\,\text{V}}{9.5\,\mu\text{V}} = 120\,\text{dB}$$

All a-d converters have inherent quantization noise equal to ± ½ LSB. In digital signal-processing applications, a more appropriate expression of dynamic range may be in terms of signal-to-noise ratios (SNR).

For sinusoidal signals $v(t) = A \sin \omega t$, where A is equal to half the full scale range (pk-pk) of the converter, the rms value of the signal is represented as:

$$\frac{A}{\sqrt{2}} = \frac{\text{FSR}/2}{\sqrt{2}} = \frac{\text{FSR}}{2\sqrt{2}}$$

For quantization noise (uncertainty) of ± ½ LSB, pk-pk quantization noise = 1 LSB. Rms quantization noise is:

$$\frac{1\,\text{LSB}}{\sqrt{12}} = \frac{\text{FSR}/2^N}{\sqrt{12}} = \frac{\text{FSR}}{2^N\sqrt{12}}$$

If N = the number of bits of resolution, then SNR is:

$$\text{SNR} = \frac{\text{rms signal}}{\text{rms noise}} = \frac{\text{FSR}/2\sqrt{2}}{\text{FSR}/2^N\sqrt{12}} = 2^N\sqrt{3/2}$$

$$\text{SNR (in dB)} = 20 \log (2^N\sqrt{3/2})$$

$$\text{SNR} = 20\,(N \log 2 + \log \sqrt{1.5})$$

$$\text{SNR} = 20\,(0.301 + 0.09)$$

$$\text{SNR} = (6.02N + 1.8)\,\text{dB}$$

Using this equation, the maximum signal-to-noise ratio for 8-to-16-bit converters runs linearly from 49.8 to 97.8 dB.

Because of the MN5420's floating-point architecture, it merits two dynamic range specifications. Its "scaled dynamic range" is the 120 dB defined earlier. Its "instantaneous dynamic range" is the ratio of its instantaneous LSB to its instantaneous input voltage range and is effectively the number of bits (12) in the mantissa a-d converter. This instantaneous dynamic range (72 dB) "floats" over a 48-dB dynamic range, as determined by the MN5420's PGA gain (from ×1 to ×256).

Analog Technology: 20-bit a-d converter

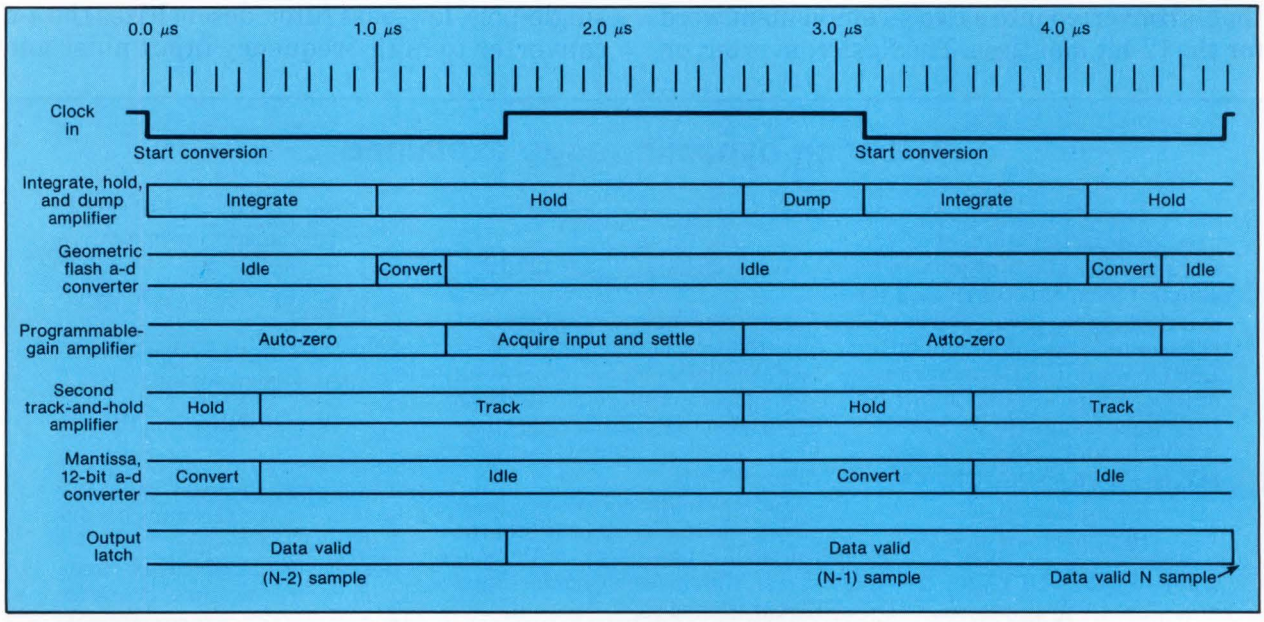
spurious signals that would otherwise be aliased into the signal spectrum by the sampling function. As an added feature, the sin X/X characteristic provides nulls in the input spectrum at frequencies having an integral number of cycles over the integrated period.

In addition, the integrate and dump function reduces the converter's sensitivity to high-frequency FM sidebands and jitter on the arrival of the input encode command. Thus the rejection of high-frequency noise on the signal input and the rejection of FM noise on the encode signal is performed at the very input to the a-d converter module. (In fact, the integrate, hold, and dump amplifier in the MN5420 produces less than 100 μV of rms noise, while the MN375 wideband, 12-bit linear track-and-hold hybrid yields approximately 320 μV of rms noise, and a widely used fast monolithic device produces 190 μV).

The dump portion of the cycle completely discharges the hold capacitor, thus ensuring that "memory" of a previously held voltage will not produce an error.

Current, not voltage

In a departure from usual sampling techniques, the integrate, hold, and dump amplifier uses a current rather than a voltage to charge the hold capacitor, C_H. A Howland current pump provides a current that is proportional to the differential input voltage. Given the system's wide dynamic-range requirement, this near-ideal, high-compliance current source is a necessity. In a conventional voltage-driven scheme, the input DMOS FETs' (S_1 and



2. In the conversion of an analog signal, the integrate, hold, and dump amplifier acquires (integrates) the signal for 1 μs and holds it for 1.6 μs while the programmable-gain amplifier settles. It then dumps the signal on the hold capacitor (to eliminate memory, or hysteresis) while the second track-and-hold amplifier holds the signal to the a-d converter constant. The complete cycle takes 3.125 μs.

S_2) on-resistance is dependent on the input voltage and would thus give rise to intolerable errors. Current drive, of course, completely eliminates on-resistance effects.

In the circuit (see Fig. 3 again), S_1 shunts the current source's output to ground when S_2 is open. That step prevents the Howland circuit's op amp from swinging wildly to the rails when the current output is interrupted. In the integrate step, S_1 and S_3 are open, and S_2 is closed. The input current charges C_H for 1 μs. In the hold period, S_1 closes and S_2 opens for about 1.6 μs. Finally, in the dump operation, S_3 closes to discharge C_H in approximately 500 ns.

The compensation block minimizes errors arising from charge transfer and feedthrough. Charge transfer, or hold pedestal, arises because the transitions of the switches' control logic couple to the hold capacitor through S_2's gate-drain capacitance. The compensation circuit provides a similar capacitance from the logic to the op amp's noninverting terminal; the net result is a common-mode signal that cancels the pedestal. Feedthrough occurs because the input signal couples to the hold capacitor when S_2 is off; the culprit in this case is the FET's source-to-drain capacitance. The compensation again provides a like capacitance from the input to a capacitor equal to C_H at the noninverting terminal.

Geometric flash converter

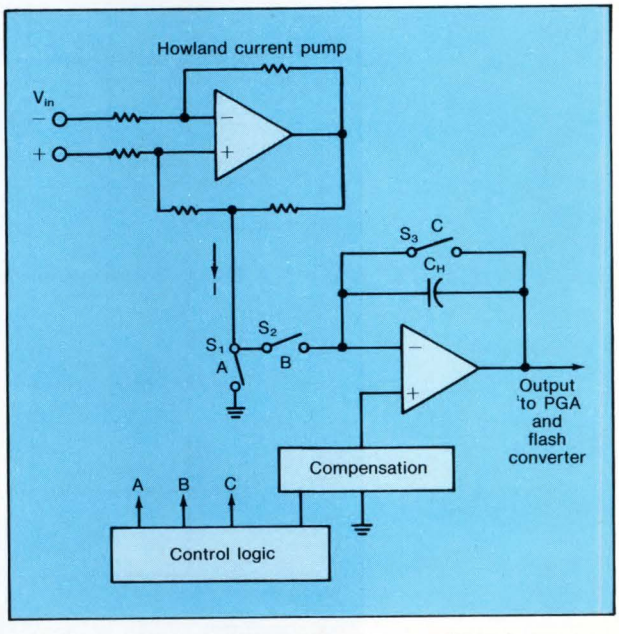
The major contributor to the speed of this floating-point machine is its flash converter, which sets the PGA's gain. Not a typical flash, it operates on a geometric rather than a linear basis to maximize speed, minimize the parts count, and handle bipolar signals (Fig. 4).

In a conventional (linear) flash converter, the resistor network that generates the reference voltage for the comparators consists of a string of equal resistors. In contrast, this converter uses a pair of R-2R networks, one for each signal polarity.

For example, a linear converter with eight comparators would divide the 5-V full-scale reference into eight equal increments of 0.625 V each; transitions would then take place at 0.625, 1.250, 1.875, 2.500, 3.750, and 4.375 V. This covers a dynamic range of only 8 to 1, or 18 dB. Linear techniques would require a flash converter with about a million comparators.

However, by using the geometric technique implemented by the R-2R network, a mere eight comparators can cover the 120-dB dynamic range. In actuality, 16 comparators are used, eight (even-numbered) for positive signals and eight for negative signals. The transition voltage for each level is shown.

At first glance, the circuit might appear somewhat strange—for example, the ladder has only six pick-off points for each polarity as opposed to the theoretical eight. Observing the positive polarities only, comparators 6 and 10 obtain their reference inputs from the same point as do comparators 8 and 12. Because the signal input to comparators 10 and 12 (and 14 and 16) is four times that applied to the higher-order comparators (as a result of the 4:1 signal

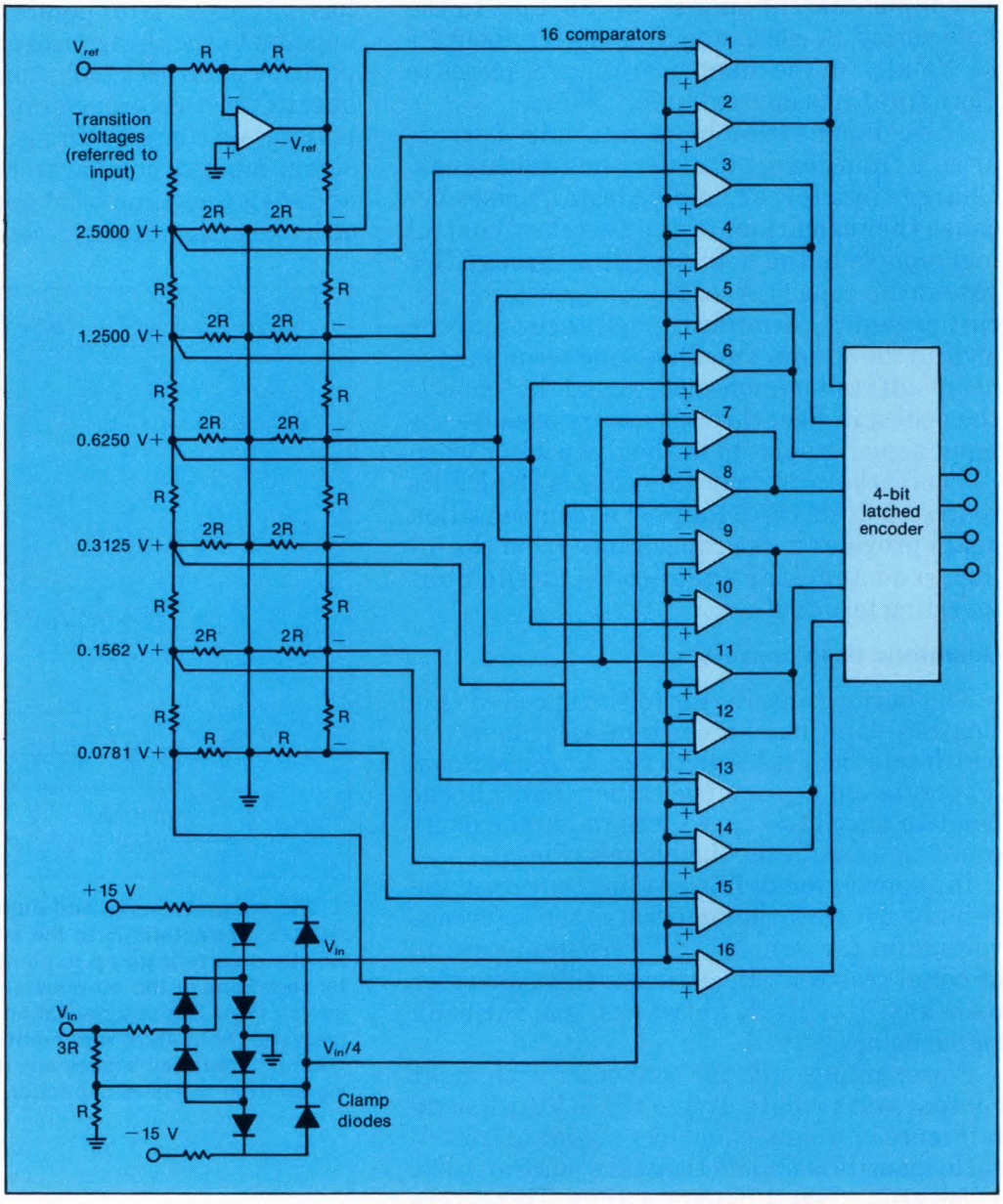


3. The integrate, hold, and dump amplifier imparts a sin X/X characteristic to the analog signal. It uses a Howland current pump to eliminate errors caused by variations in the on-resistance of the input FET switch (S_2). The compensation circuitry minimizes pedestal (hold step) and feedthrough errors; the "dump" operation erases any memory of a previous signal from the hold capacitor.

divider circuit), the net result is the same as that obtained with a ladder having eight pick-off points. This circuit reduces the size of the resistor network and eliminates two wire bonds and some laser trimming. The situation is symmetrical for negative polarities.

The input to the higher-order comparators is divided by four to reduce the maximum differential input voltage to these ICs. Further, this step holds the inputs to a level where simple diode clamping can prevent input-circuit degradation caused by large input excursions. To this end, the clamping-diode circuit limits all comparator input voltages to two or three diode drops (± 1 to ± 2 V).

Finally, to avoid exceeding the 12-bit a-d converter's range, the actual implementation of the autoranging flash converter



4. An absolute-value, geometric flash-converter sets the gain of the PGA and provides the 4-bit exponent portion of the digital output word. It uses just 16 comparators to handle a 48-dB bipolar dynamic range signal.

scales the transition points slightly below those shown in the schematic. For example, instead of the indicated +2.5 V (referred to input) for the most-significant-bit (MSB) transition, the trip point is actually set at +2.0 V; the lower-order transitions are scaled accordingly.

Pseudo-PGA

Once the autoranging flash converter has set the optimum gain for the PGA, the amplifier does its job of presenting the highest level input possible to the 12-bit a-d converter. However, this PGA accomplishes that without variable gain. Rather, to achieve maximum bandwidth (minimum settling time), it uses a programmable attenuator followed by a fixed-gain amplifier pair, A_1 and A_2 (Fig. 5). Attenuation factors run in binary steps of 1, 2, 4 . . . 64, 128, 256 to match the outputs of the geometric flash converter. The inverting amplifier has a gain of 128.

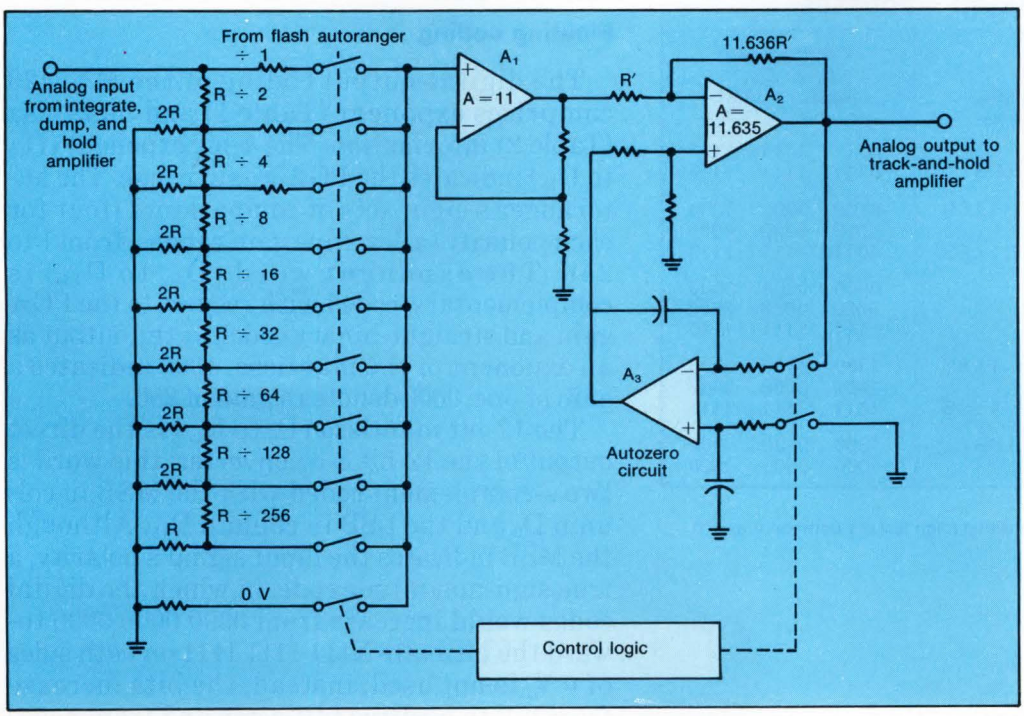
The attenuator-amplifier pair thus yields gains of 0.5, 1, 2, 4, 8, 16, 32, 64 and 128. Gains range from 0.5 to 128 instead of 1 to 256 because the analog input ranges for the MN5420 is ±5 V, while its 12-bit a-d converter input range is ±2.5 V, thus contributing a "gain" of two. This halved-gain requirement further improves the amplifier's offset and settling time.

Since an LSB is approximately 10 μV, the amplifier is equipped with an autozero circuit, in effect making it a chopper-stabilized amplifier. This circuit also maintains a constant offset for all ranges. Without zeroing, the offset would appear to change when the output mantissa was divided by the exponent.

The autozeroing function takes about a third of each conversion cycle. The control logic closes the associated switches, applying 0 V to amplifier A_3 and causing the autozero circuit to force 0 V at the output of the second op-amp stage, A_2.

Broad bandwidth demands

The floating-point converter contains three more major circuit blocks: the second track-and-hold amplifier, the 12-bit 1-μs a-d converter, and a 16-bit, three-state output latch. The transient and settling times required by



5. A programmable attenuator followed by a fixed-gain amplifier provides a settling time that does not change over a range of gains from 0.5 to 128. The a-d converter that follows provides an additional gain of 2.

Analog Technology: 20-bit a-d converter

the high-speed flash a-d converter and the PGA demand broad bandwidths from these two circuits.

To prevent their internally generated broadband noise from reaching the second track-and-hold amplifier, a filter is inserted before it. This amplifier permits the signal to be passed through a two-stage, or pipelined, process; the signal is first amplitude-scaled and resampled and then resampled. During the second portion of the next encoding interval, the signal is encoded through the 12-bit mantissa-generating a-d converter.

This two-stage pipelined architecture allows time for filtering before the second sampling. That filtering, in turn, reduces the wideband thermal noise generated by the PGA that would otherwise be aliased into the second sampling amplifier. It also reduces the requirements on the timing of the hold command to the second amplifier. That traditional "closed-loop" track-and-hold circuit acquires a 5-V signal with ±0.01% accuracy in less than 1 μs, while the PGA is settling.

The 12-bit a-d converter is a hybrid circuit using a 7-bit flash-converter chip in a subranging configuration that includes digital error correction. Its analog input drives the flash converter to determine the seven MSBs. The flash converter's output drives a precision d-a converter whose output is subtracted from the input signal. The residue is recirculated to the flash a-d converter to determine the five LSBs of the digital output, leaving the two extra MSBs to correct any inaccuracies in the seven MSBs of the first conversion.

Table 1. Floating-point converter's 4-bit exponents

Programmable-gain amplifier code (D_{12}–D_{15})	Gain	Input voltage
1 0 0 0	1	2.5 V<|V_{in}|<5 V
0 1 1 1	2	1.25 V<|V_{in}|<2.5 V
0 1 1 0	4	0.625 V<|V_{in}|<1.25 V
0 1 0 1	8	0.3125 V<|V_{in}|<0.625 V
0 1 0 0	16	0.15625 V<|V_{in}|<0.3125 V
0 0 1 1	32	0.078125 V<|V_{in}|<0.15625 V
0 0 1 0	64	0.039063 V<|V_{in}|<0.078125 V
0 0 0 1	128	0.019531 V<|V_{in}|<0.039063 V
0 0 0 0	256	0 V <|V_{in}|<0.019531 V

Table 2. Floating-point converter's 12-bit mantissas

Analog input	Output code $D_0 \rightarrow D_{11}$ (MSB → LSB)
+ F.S.*	0111 1111 1111
+ F.S. − 1 LSB	0111 1111 111Ø**
+ ½ F.S. + 1 LSB	0100 0000 000Ø
+ ½ F.S.	0ØØØ ØØØØ ØØØØ
+ ½ F.S. − 1 LSB	0011 1111 111Ø
+ 1 LSB	0000 0000 000Ø
0.0000 V	ØØØØ ØØØØ ØØØØ
− 1 LSB	1111 1111 111Ø
− ½ F.S. + 1 LSB	1100 0000 000Ø
− ½ F.S.	1ØØØ ØØØØ ØØØØ
− ½ F.S. − 1 LSB	1011 1111 111Ø
− F.S. + 1 LSB	1000 0000 000Ø
− F.S.	1000 0000 0000

*F.S.—full scale
**Ø denotes a transition (digit flickers between 0 and 1).

Floating coding

The digital-output coding of the MN5420 comprises exponent (Table 1) and mantissa (Table 2) information. The 4-bit exponent (D_{12} to D_{15}) indicates the PGA's gain range. The autoranger's eight sets of comparators (four for each polarity) allow nine gain ranges, from 1 to 256. The exponent word (D_{12} to D_{15}) is complementary-coded with respect to the PGA gain and straight-binary coded at the output as an exponent of the mantissa. 1000 indicates a gain of one; 0000 denotes a gain of 256.

The 12-bit mantissa (D_0 to D_{11}) is the direct output of the 12-bit a-d converter; this word is two's-complement coded with the MSB in column D_0 and the LSB in column D_{11}. Although the MSB indicates the input signal's polarity, a true sign-magnitude code, in which the digital codes would increase from 0000 0000 0000 toward the ultimate X111 1111 1111 on both sides of 0 V, is not used; instead, the bits increase from 0 V to positive full-scale and from negative full-scale to 0 V.

The analog input voltages shown (see Table 2

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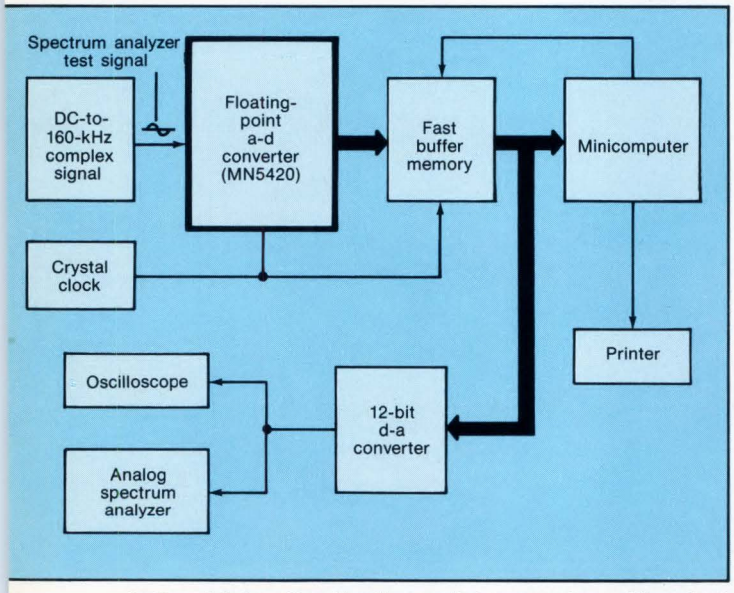
again) are the theoretical values of the digital-output transitions indicated. In an ideal situation, with the converter continuously operating, the output bits indicated as "0" will change from a 1 to a 0 (or vice versa) as the input voltage passes through the level indicated. If the converter is driving a bank of LEDs, those voltages will cause the pertinent lamps to flicker.

The coding is perhaps most easily understood if the device is viewed as nine 12-bit a-d converters, each with an input-voltage range half that of the previous one. For example, with an exponent of 1000, the converter has a ±5-V input range. If the exponent is 0111, however, the unit's effective range is ±2.5 V. Note that the LSB size is the input range (total span) divided by 4096, the total number of codes resolvable by a 12-bit converter.



6. Combining the floating-point converter with a fast buffer memory and a minicomputer produces a spectrum analyzer that can handle fast, complex signals with a wide dynamic range in real time.

Employment opportunity

The floating-point a-d converter finds a major application as the front end of a real-time spectrum analyzer for analog signals with a wide bandwidth and wide dynamic range. In this usage, the output of the converter is fed to a high-speed buffer memory and then to a high-performance minicomputer. The computer, using fast Fourier transforms (FFTs), performs feats ranging from detecting continuous wave radar signals deeply embedded in noise to interpreting the complex waveforms obtained from seismic sensors searching for slippery hydrocarbons.

The MN5420 floating-point converter becomes the heart of a spectrum analyzer (Fig. 6) capable of handling complex signals with frequency components to 160 kHz, the Nyquist frequency of the 320-kHz throughput converter. The amplitude of these signals can range from 10 μV to 10 V pk-pk. Although it handles these signals, the analyzer is best demonstrated by being fed an ultrapure 5-kHz sine wave. Its amplitude is set at various levels over the full 120-dB dynamic range of the instrument, and a number of conversions are made at each level.

In this application, the converter runs continuously, initiating conversions on the falling edge of each clock pulse and strobing data from the previous conversion into the three-state output latches on the clock's rising edge.

At the start of the demonstration program, the minicomputer enables the fast buffer memory; the memory then acquires a preset number of successive samples produced by the converter. This sample sequence can range in length from 256 to 2048 16-bit words.

The data is read from the buffer into the minicomputer's memory; the computer applies a Hanning windowing function to the sample sequence and performs the FFT. The computer then analyzes the resulting spectrum to determine the signal-to-noise ratio, which, when measured over the full dynamic range, is a basic indication of analyzer performance. The result-

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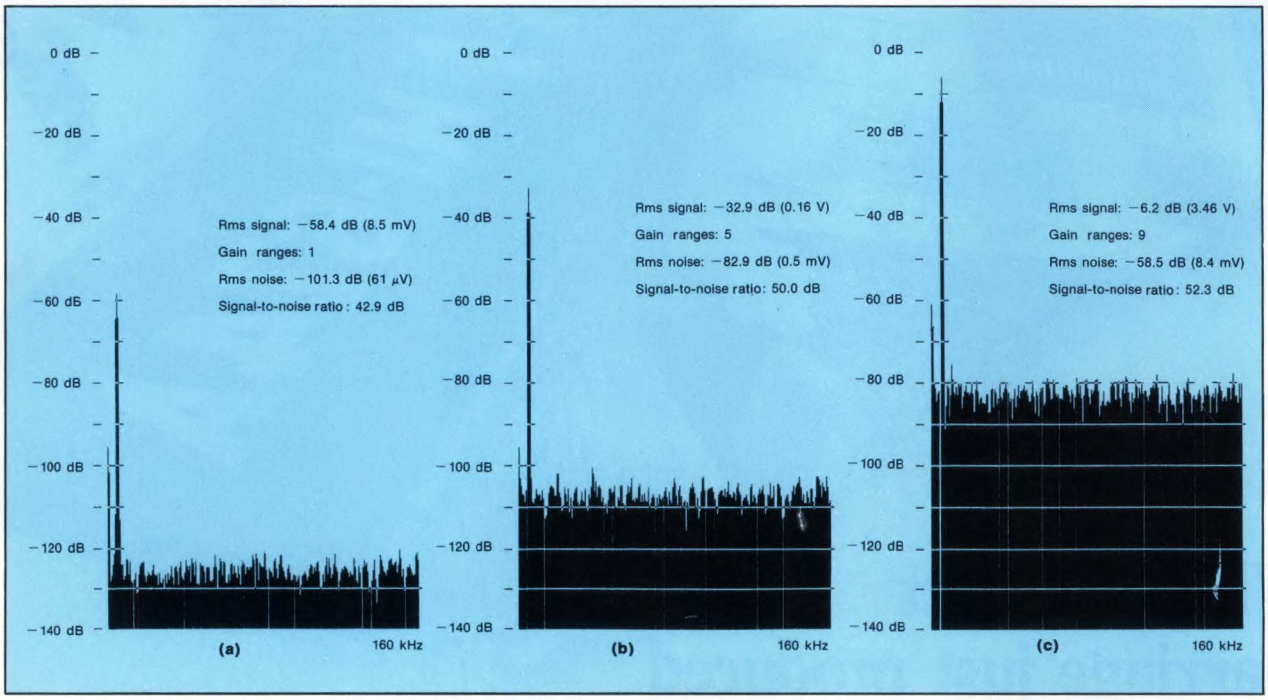
ing data is sent to a dot-matrix printer. If desired, the system can take as many as 256 spectra in succession and average them.

The plotted results of 512-point FFT analyses at three input signal levels are shown (Fig. 7). Each represents the average of four spectra. Note that the signal-to-noise ratios represent the rms noise produced by the converter at various input levels—that is, the square root of the sum of the squares of all frequency bands excluding a band around the input signal, the spike on the left of each at 5 kHz. The ratio of the input signal peak to any particular spurious peak is greater than 55 dB in all cases. □

Acknowledgments

The authors would like to acknowledge the contributions to the MN5420 made by section manager Don Miller, of Raytheon Co., and of Tom Borski and Joe Wronski, both of Micro Networks.

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546



7. A spectrum analyzer built from the floating-point converter is tested with an ultrapure, 5-kHz sine wave. The input level of the sine wave is set at the maximum input voltage for each of three gain ranges of the converter between 1 and 256, and a spectrum analysis is run at each setting. Each analysis is a 512-point FFT made with a Hanning windowing function applied to the digital data. The sampling rate is 320 kHz. Regardless of the input signal amplitude, the signal-to-noise ratio is more than 66 dB.

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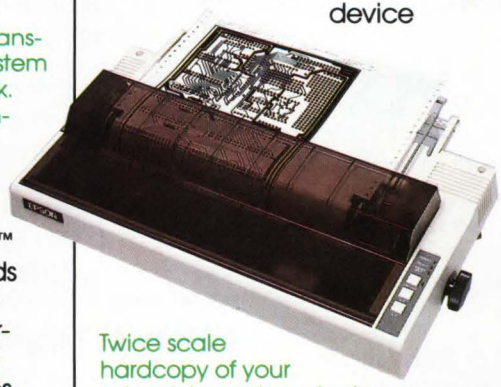

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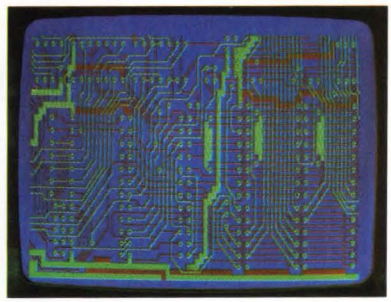

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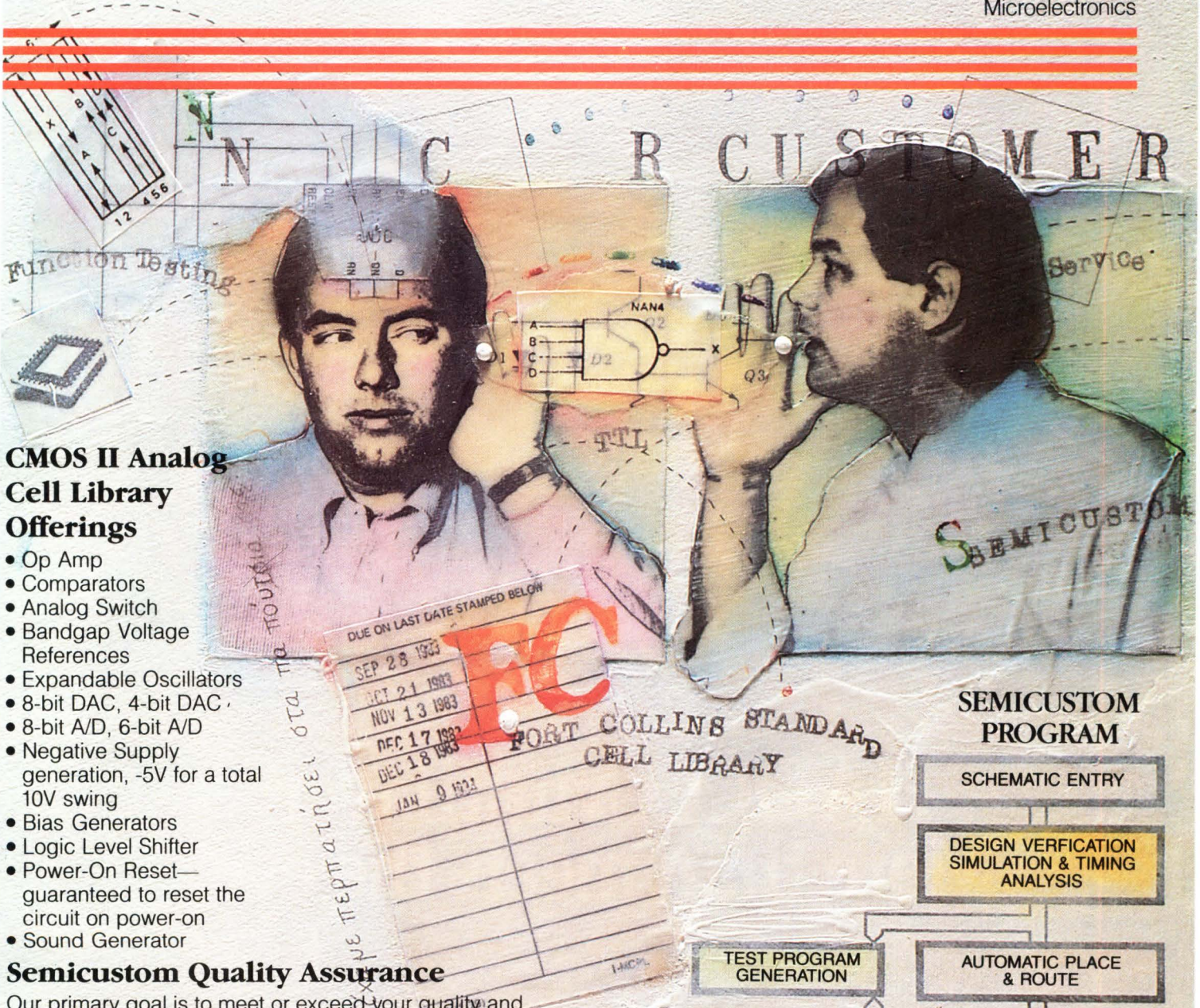

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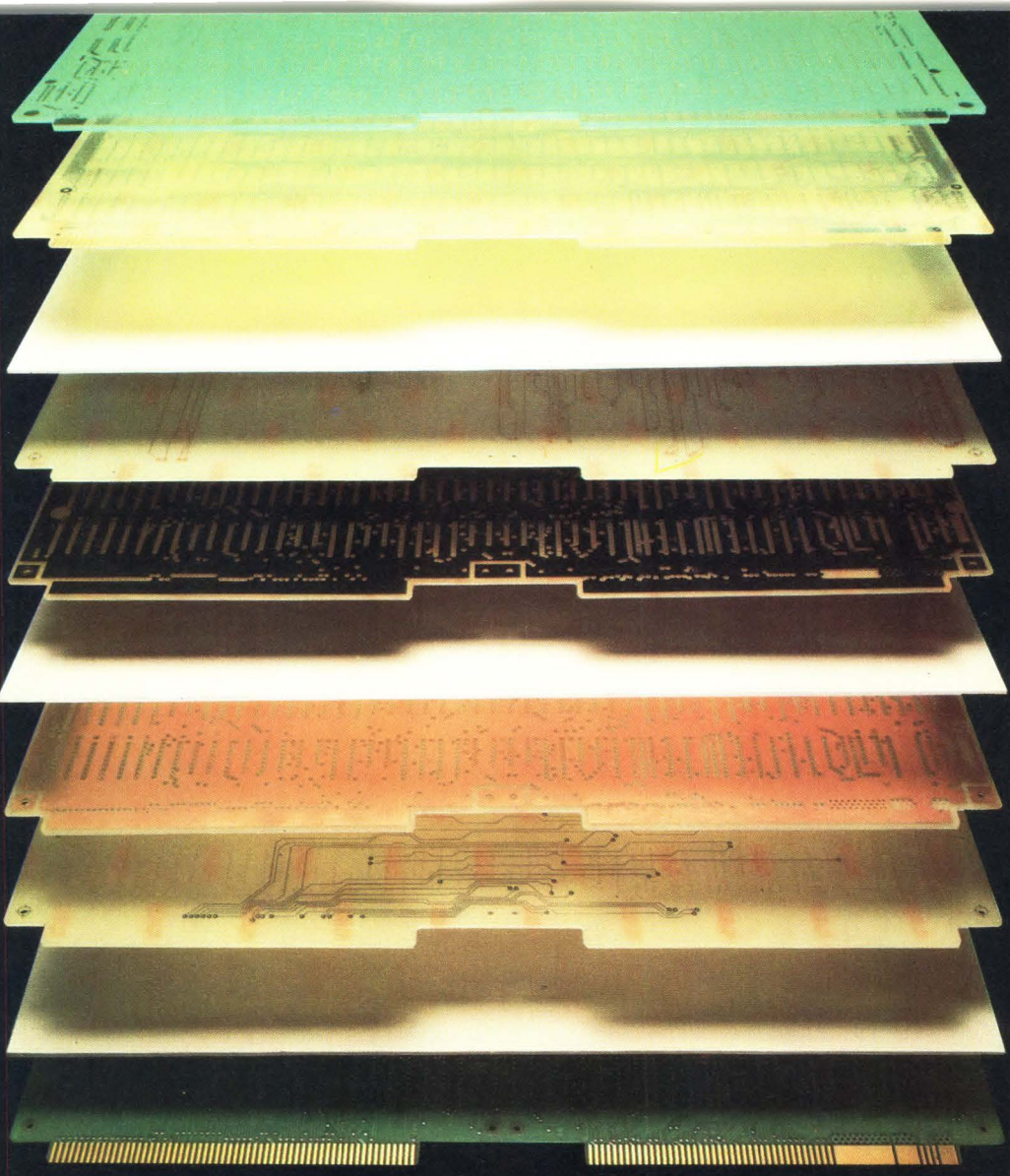

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Monolithic a-d converter interfaces directly with most microprocessors

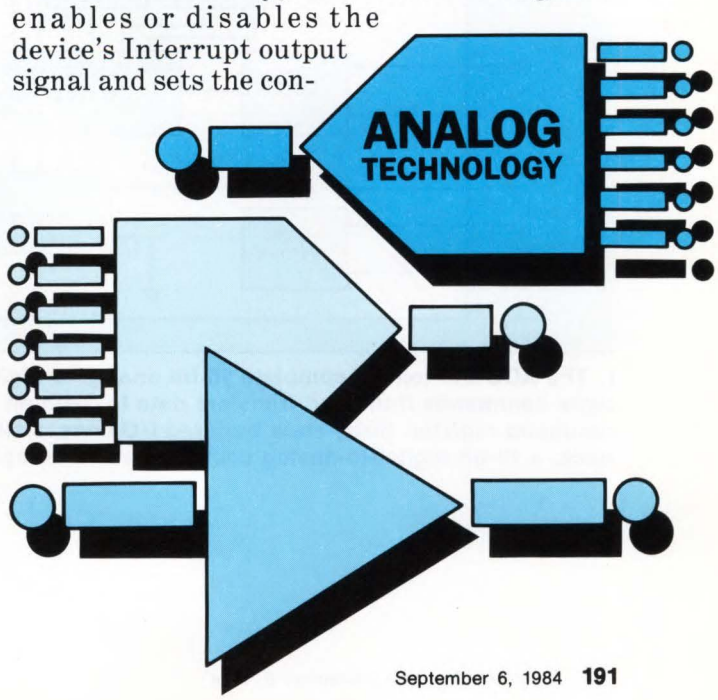
Accepting and delivering data over an 8- or 16-bit bus, a one-chip analog-to-digital converter is accurate to 10 bits and handles a conversion in a mere 6 μs.

A microprocessor interface is a natural partner for an analog-to-digital converter. Until now, however, that partnership has never been completely established on a single chip, for it demands precise analog and compact digital circuits that no combination of logic structure and IC process has been capable of creating.

A specially designed logic structure and bipolar process have overcome that hurdle, yielding a converter that is accurate to 10 bits and that operates under the control of either an 8- or a 16-bit microprocessor. The device also formats digitized data for and accepts software commands from both. What's more, the chip carries out a conversion in only 6 μs.

Having a complete interface on board the converter reduces the parts count in microprocessor-based systems. Moreover, the converter is three times as fast as any other monolithic 10-bit device. It thus boosts the data-handling rate and the system bandwidth in precise real-time operations such as digital signal processing applications.

From a microprocessor's point of view, the ADC-910 is designed to resemble a peripheral interface adapter, transferring data bidirectionally and under software control. For example, the converter's command register, which controls the choice of functions, accepts a Start of Conversion command directly from a data bus through the chip's bidirectional three-state buffers. Similarly, the command register enables or disables the device's Interrupt output signal and sets the con-



Stephen Moore and **Steve Pietkiewicz**
Precision Monolithics Inc.

Stephen Moore is a senior product marketing engineer at Precision Monolithics in Santa Clara, Calif., and is responsible for its bipolar data converters. Before joining the company, he served as an application engineer for data conversion products at Siliconix and as a design engineer for a number of Silicon Valley companies. He holds a BSEE from the University of California at Berkeley.

Steve Pietkiewicz, a senior design engineer, has worked at the company for three years on bipolar data acquisition and linear IC designs. He also holds a BSEE from the University of California at Berkeley.

Analog Technology: A-d converter

verter for either unipolar or bipolar input voltages (Fig. 1).

The same three-state buffers also send converted data to the microprocessor bus. The information is either transmitted 10 bits at a time or sent in two successive bytes: a high-order byte and a low-order byte that includes the remaining 2 bits. A status word sent out by the converter indicates when a conversion is complete and if the input voltage is out of range (see the table, opposite).

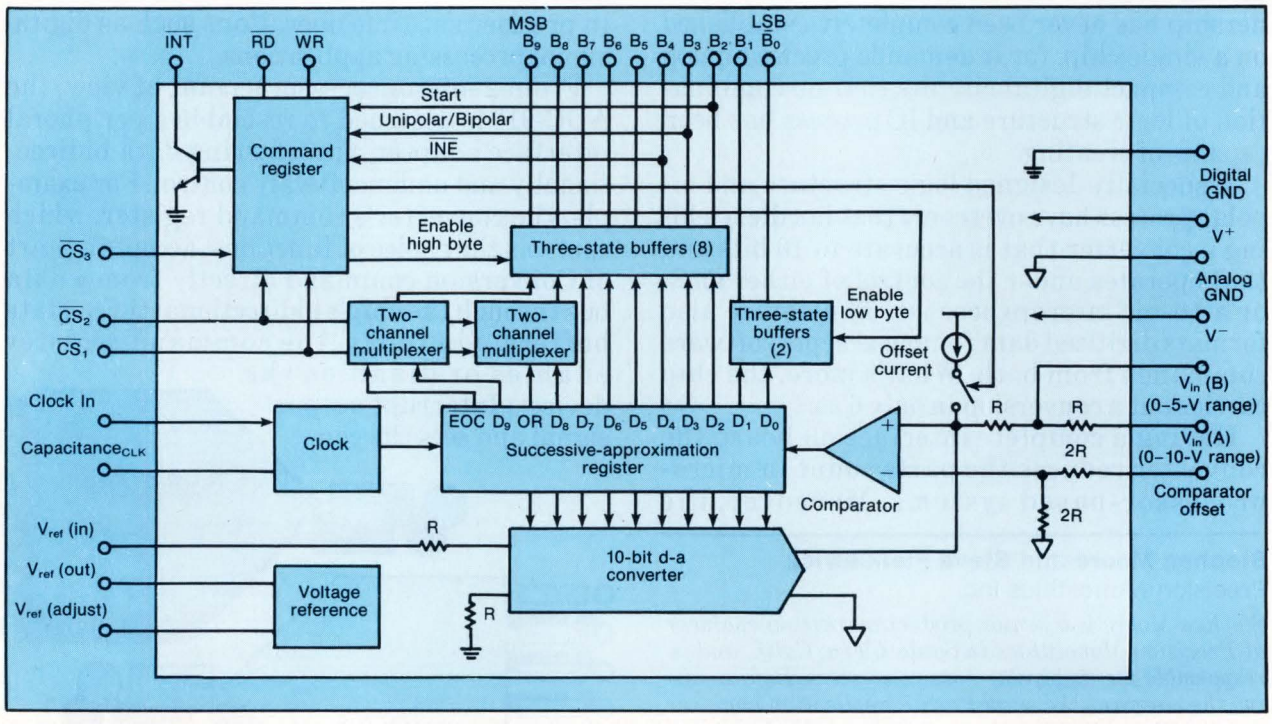
The chip contains all the elements needed for a complete a-d converter. It includes a voltage reference that is stable to within 25 ppm/°C (see "Attending to Analog Elements Ensures Accuracy," p. 200), a successive-approximation register, a 10-bit digital-to-analog converter, a high-speed comparator, and a clock. Further, unlike its slower CMOS counterparts, the converter is not easily damaged by static discharges.

In all, through a combination of pin and software programming, the converter accepts up to four input-voltage ranges. They are 0 to 10, 0 to 5, ±5, and ±2.5 V dc.

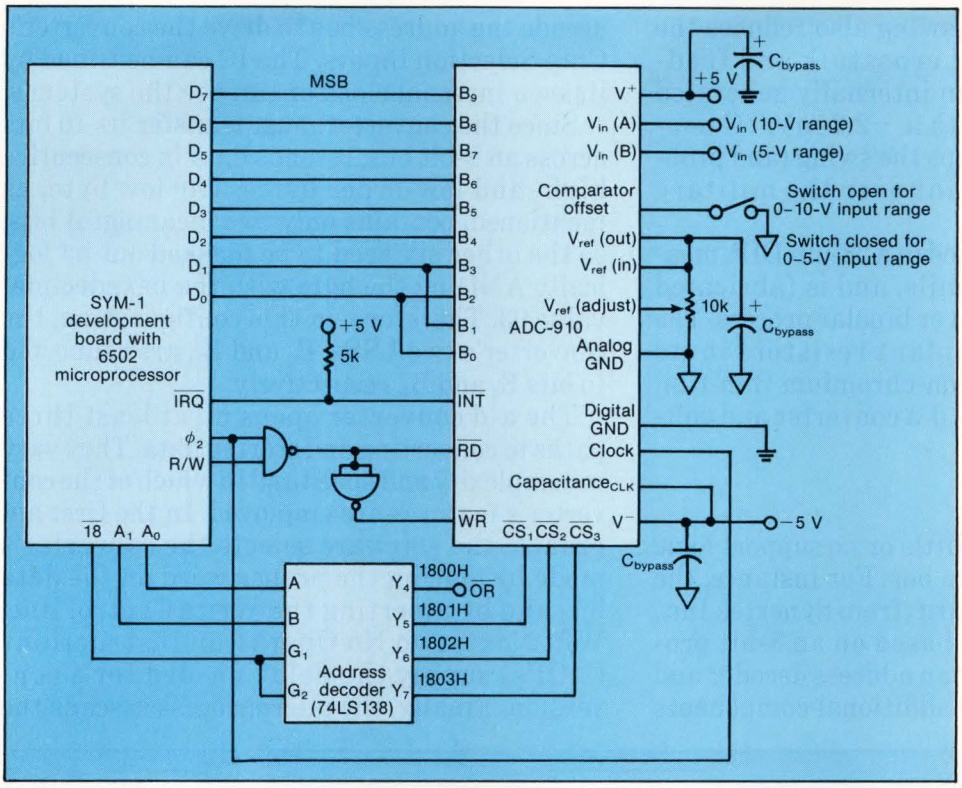
Finally, so-called zener-zap trimming eliminates the need for laser trimming and ensures long-term stability and an integral nonlinearity of no more than ½ LSB over the full military temperature range. (The zener-zapping technique trims by turning on small-value current sources.)

In order to integrate the large amount of circuitry needed in the converter, its designers worked with a proprietary logic circuitry, known as linear differential logic. LDL, a nonsaturating form of logic similar to emitter-coupled logic, was chosen largely for its simple and compact gate structure, as well as for its low power consumption.

LDL is self-biasing and—with its 150-mV logic swing—works well alongside precise ana-



1. The ADC-910 joins a complete 10-bit analog-to-digital converter with a microprocessor interface that accepts commands from, and transfers data to, both an 8- and a 16-bit bus. It counts among its elements a command register, three-state buffered I/O lines, a successive-approximation register, a voltage reference, a clock, a 10-bit digital-to-analog converter and a comparator.



2. Only two logic chips are needed to connect the converter to an 8-bit microprocessor development board. The address decoder and the inverter IC fulfill all of the converter's addressing requirements. For an 8-bit bus, the converter transfers its 10 bits in a low- and high-order format.

Reading and writing for the 10-bit converter

Read/Write	Chip Select	Bit position and meaning										Explanation
		B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	
$\overline{WR}$ = low	$\overline{CS_3}$ = low	Don't care					Interrupt, 1=Disable 0=Enable	1=Unipolar 0=Bipolar	1= Start conversion	Don't care		Start conversion and select operating mode
$\overline{RD}$ = low	$\overline{CS_1}$ = low	Data								High-impedance		Read high-order byte
	$\overline{CS_2}$ = low	High-impedance								Data		Read low-order byte
	$\overline{CS_3}$ = low	1 = busy 0 = End of Conversion	1 = over-range 0 = within range	Don't care						High-impedance		Read status

log circuitry. Its small swing also reduces the chances of chip-level crosstalk and feedthrough. In addition, an internally generated logic supply voltage with a −2.2-mV/°C temperature coefficient keeps the swing (and propagation delay) constant over the military range.

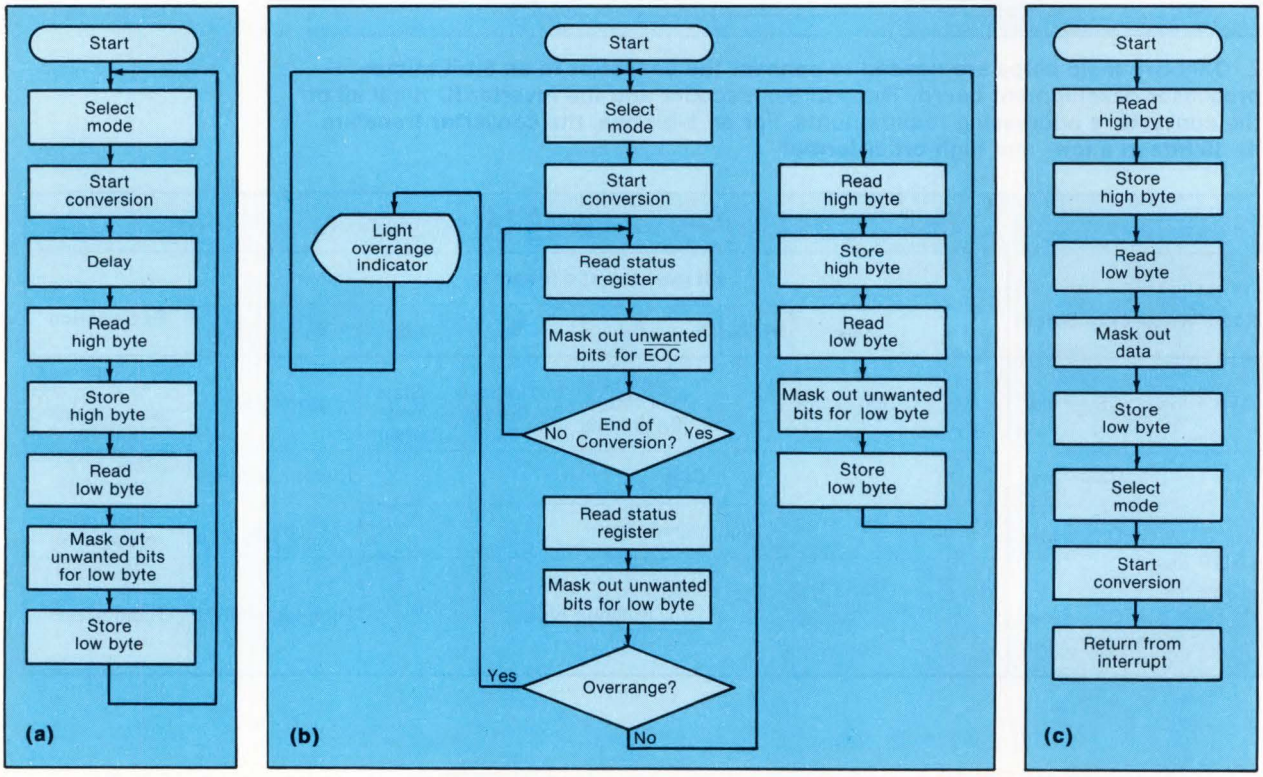
The chip itself is housed in a 28-pin DIP, measures 222 mils by 132 mils, and is fabricated with a 7-μm epitaxial layer bipolar process. The circuit contains p-implant resistors in its digital portion and silicon-chromium thin-film resistors throughout its d-a converter and voltage reference sections.

Transfer by bus

The converter needs little or no support logic to link it to an 8-bit data bus. For instance, the SYM-1 development board (from Synertek Inc., Santa Clara, Calif.) is based on an 8-bit processor and calls for only an address decoder and inverter (Fig. 2). Those additional components decode the address bus to drive the converter's Chip Selection inputs. The IC can be timed by its own internal clock or can use the system's.

Since the converter must transfer its 10 bits across an 8-bit bus, it sends data in consecutive high- and low-order bytes. The low byte, as mentioned, contains only two meaningful bits, so the other six need to be masked out by logically ANDing the byte with the hexadecimal value 03. Therefore, in this configuration, the converter's two LSBs, B_0 and B_1, are connected to bits B_3 and B_4, respectively.

The a-d converter opens up at least three paths to converting and storing data. They vary in complexity and speed and in which of the converter's features are employed. In the first approach, the software selects the converter's mode by placing the proper word on the data bus and by asserting the Write Control line, $\overline{WR}$. Next, two No Operation instructions (NOPs) supply the delay needed for a conversion. Finally, the microprocessor scans the



3. A designer can take at least three different tacks for converting and storing data. The simplest is to start the conversion and delay the data reading operation with No Operation instructions (a). The second takes advantage of the chip's End of Conversion and Overrange bits (b), and the third uses the converter's Interrupt output signal to initiate a service routine in the program (c).

reads and stores the converter's high- and low-order bytes (by asserting its Chip Select lines, $\overline{CS_1}$ and $\overline{CS_2}$, respectively) in separate memory locations (Fig. 3a).

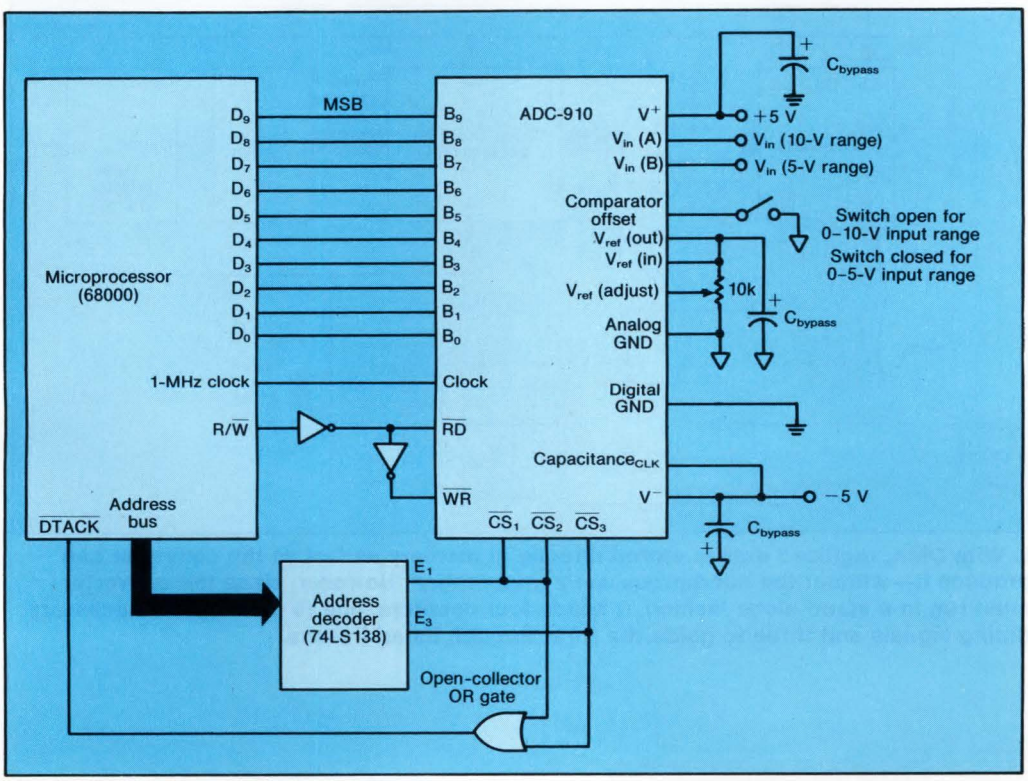
A second approach puts the converter's status register to work checking whether a conversion is complete or an input voltage is out of range (Fig. 3b). To do so, the microprocessor first polls the status register, by sending low its Chip Select input ($\overline{CS_3}$), until the register's Busy bit goes low, which indicates that a conversion is complete. The microprocessor then reads the status register again, this time for its Overrange bit. If the input is within range, the data is read and stored in memory.

Excuse my interruption

In the third scheme, a designer can use the converter's Interrupt output signal ($\overline{INT}$) to drive the microprocessor's Interrupt Request line (IRQ). The software first sets the processor's interrupt vector and then holds the device in a loop, waiting to be interrupted by the converter. When an interrupt signal is sent, the program goes to an interrupt service routine, which reads and stores the data, restarts the conversion process, and then reenters the loop at the point it exited (Fig. 3c).

The converter can be dropped into another 8-bit system, the SDK-85 development kit (from Intel Corp., Santa Clara, Calif.), without any additional parts. As in the previous examples, the converter transfers its data in high and low bytes and accepts commands over a multiplexed address and data bus, using its read and write control lines. Here, however, a 1-of-8 decoder supplied with the kit drives the converter's Chip Select inputs.

For a 16-bit processor like the 68000, the converter's 10 three-state I/O buffers connect to the 10 least significant bits of the 16-bit data bus (Fig. 4). In this case, an address decoder drives the converter's Chip Select lines, as well as a two-input open-collector OR gate that



4. In a 16-bit system, all 10 bits of converted data are placed on the bus at once. An address decoder generates the converter's Chip Select inputs and the Data Acknowledge signal required by the microprocessor.

Analog Technology: A-d converter

sends a Data Acknowledge signal ($\overline{\text{DTACK}}$) back to the microprocessor. Finally, the signals to control any reads and writes between the converter and the processor come directly from the processor's Read/Write output (R/$\overline{\text{W}}$).

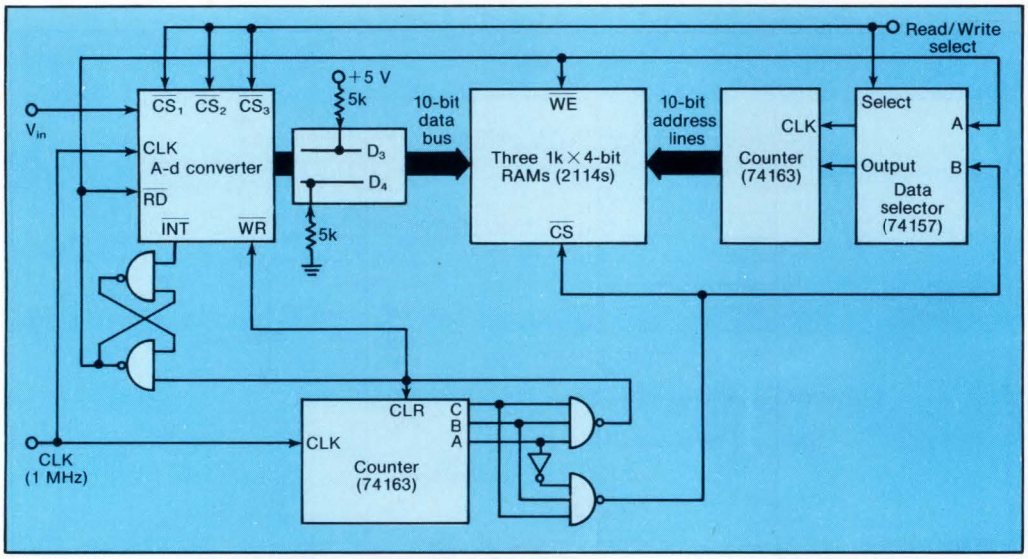
Quick as a wink

In some applications, DMA is needed to take full advantage of the converter's high speed. With direct memory access, digitized samples are stored in memory without the microprocessor's intervention. Since there is no longer a delay caused by the microprocessor's cycle time, samples are stored as fast as the converter can produce them. Once the data is stored, the program can process it at a later time. However, since DMA operations disable the microprocessor, the converter must operate as a stand-alone unit (Fig. 5). In order for the converter to access the data bus without the microprocessor, each of the converter's Chip Select lines must be linked together.

In the circuit, a counter starts the conversion process every eight cycles by asserting the chip's Write input. When a conversion is finished, the converter's Interrupt output line goes low (active) and resets a set/reset latch. That in turn holds the chip's Read input active and puts all 10 bits of converted data onto the data bus. The next Write pulse resets the latch and initiates the following conversion cycle.

Once the digitized data is available, it can be stored directly in memory. For example, three 1k-by-4-bit RAMs linked in parallel will store up to 1024 bytes before needing the microprocessor's intervention. A 10-bit counter addresses the RAM and decodes the common Chip Select lines, which signals the start of a conversion. In addition, the memory's Write Enable input connects directly to the converter's Read input.

Pull-up or pull-down resistors select the de-



5. With DMA, digitized data is stored directly in memory as fast as the converter can produce it—without the microprocessor's intervention. However, since the converter must run in a stand-alone fashion, it needs four counters: one to develop the necessary timing signals and three to guide the RAM through its addresses.

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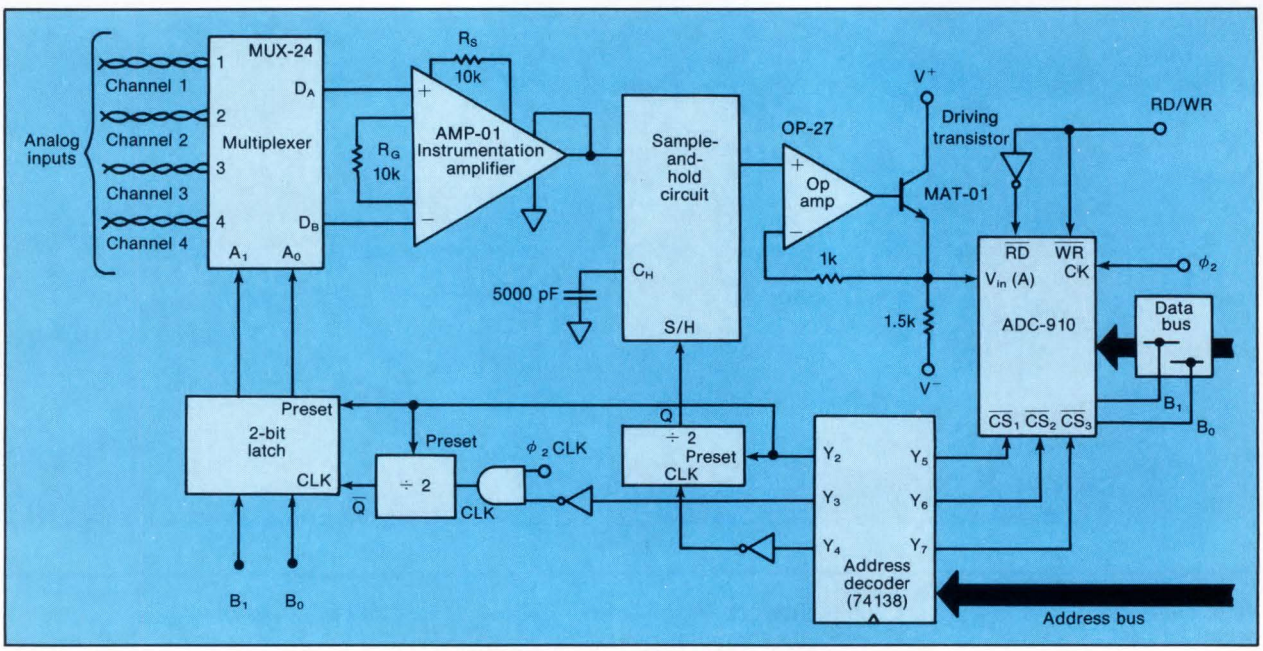
sired operating mode by setting the command word to the desired state when the Write signal is applied. To enable the Interrupt output, as is necessary in this example, and select a unipolar input range, the fourth data bit would be tied to ground and the third data bit to +5 V dc—each through a 5-kΩ resistor.

Given the converter's simple microprocessor interface, the device can serve as the building block for a data acquisition system that is composed of only a handful of ICs (Fig. 6). In one such system, an 8-bit microprocessor selects the channels, controls the sample-and-hold timing, and converts and stores the data. The microprocessor can be used to process the data as well, making decisions based on input values and controlling actuators in a manufacturing or a processing operation.

Input signals enter the system through a four-channel differential analog multiplexer, which selects one of four balanced twisted-pair lines connected to such sensing devices as pressure transducers, thermocouples, strain gauges, or other process-monitoring equipment.

The multiplexer's differential output drives an instrumentation amplifier, which boosts the output and strips it of common-mode noise. The amplifier's single-ended output, in turn, drives a sample-and-hold circuit with a 50-ns aperture time. That narrow aperture allows the converter to sample waveforms with slew rates up to 200 mV/μs accurately enough to match the converter's full 10-bit capacity.

In sampling a waveform the chip's successive-approximation algorithm modulates the input current at a 1-MHz rate. At this frequency the output impedance of most op amps is too



6. A handful of components can construct a digital data acquisition system around the converter. An analog multiplexer selects the input channel, whose signal is amplified and stripped of common-mode noise by an instrumentation amplifier. Next, a sample-and-hold circuit samples the signal, which is then buffered and fed to the converter.

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high to preserve the chip's 10 bits of accuracy. For example, given the chip's 5-kΩ input, a 5-Ω output impedance causes an error of 1 LSB. Therefore, a low-impedance, high-frequency driving source is constructed using a high-speed operational amplifier driving an emitter-follower circuit.

Finally, an address decoder supplies the timing from the system's address bus. The bus addresses the multiplexer's inputs, and a 2-bit latch holds these locations after the data passes from the bus. In addition, the address decoder, in conjunction with the microprocessor, defines the sample-and-hold circuit's timing and controls the Chip Enable input lines to the converter. Obviously, the data bus also carries the converted data, employing the high- and low-order format, when the bus is only 8 bits wide.□

How useful?	Circle
Immediate design application	547
Within the next year	548
Not applicable	549

Attending to analog elements ensures accuracy

Three sections of the ADC-910 analog-to-digital converter are essential to its accuracy. They are the resistive ladder in its digital-to-analog converter section, the bipolar offset-current source, and the voltage reference.

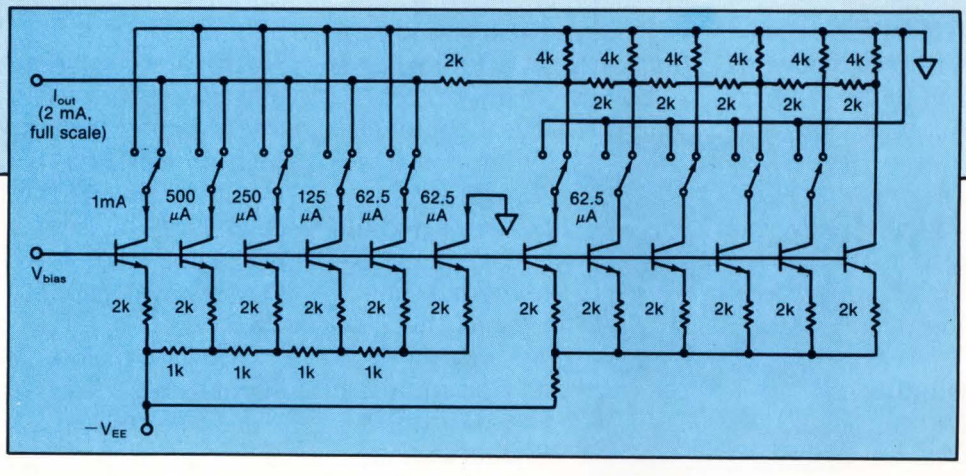
The ADC-910's resistive ladder is unique. Whereas other chips use a master-slave arrangement and current division in their emitter circuit only, the new chip's d-a section has a standard R-2R ladder for its five most significant bits and a ladder for its five least significant bits (see figure). This configuration allows the section to operate with as little as −4.5 V dc applied to its negative supply line.

One requirement for a d-a converter of this type is that the output of the inverted ladder must be at exactly ground potential in order for the bit currents to be scaled properly. That is no problem because the chip's successive-approximation algorithm inherently drives the summing node (I_0) to ground in the conversion process.

As for trimming, the second, third, and fourth MSBs are trimmed by zener-zapping them in ½-LSB increments. What's more, those d-a converters that initially fall within 0.2% of their intended value can be trimmed in ¼-LSB increments by zener-zapping one additional diode.

The bipolar offset-current is switched in and out of the summing node by a pair of diodes (during the unipolar mode this current shunted to the negative supply). The current source is trimmed during the wafer-sorting stage to equal the MSB current. In addition, an on-chip capacitor supplies compensation to stabilize the current source and ensure fast settling.

The voltage reference, which delivers 2.5 V dc at up to 5 mA, is based on the popular bandgap technique but incorporates a novel curvature correction scheme to achieve its 25-ppm/°C stability. A correction current source delivers a temperature-dependent current, which cancels temperature-induced curvature in the bandgap voltage and yields a constant output voltage. As with other analog portions of the converter, the critical thin-film resistors in the voltage reference are trimmed during the wafer-sorting stage to eliminate the effect of process variations and minimize the temperature coefficient.



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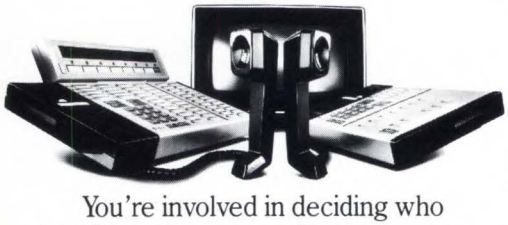

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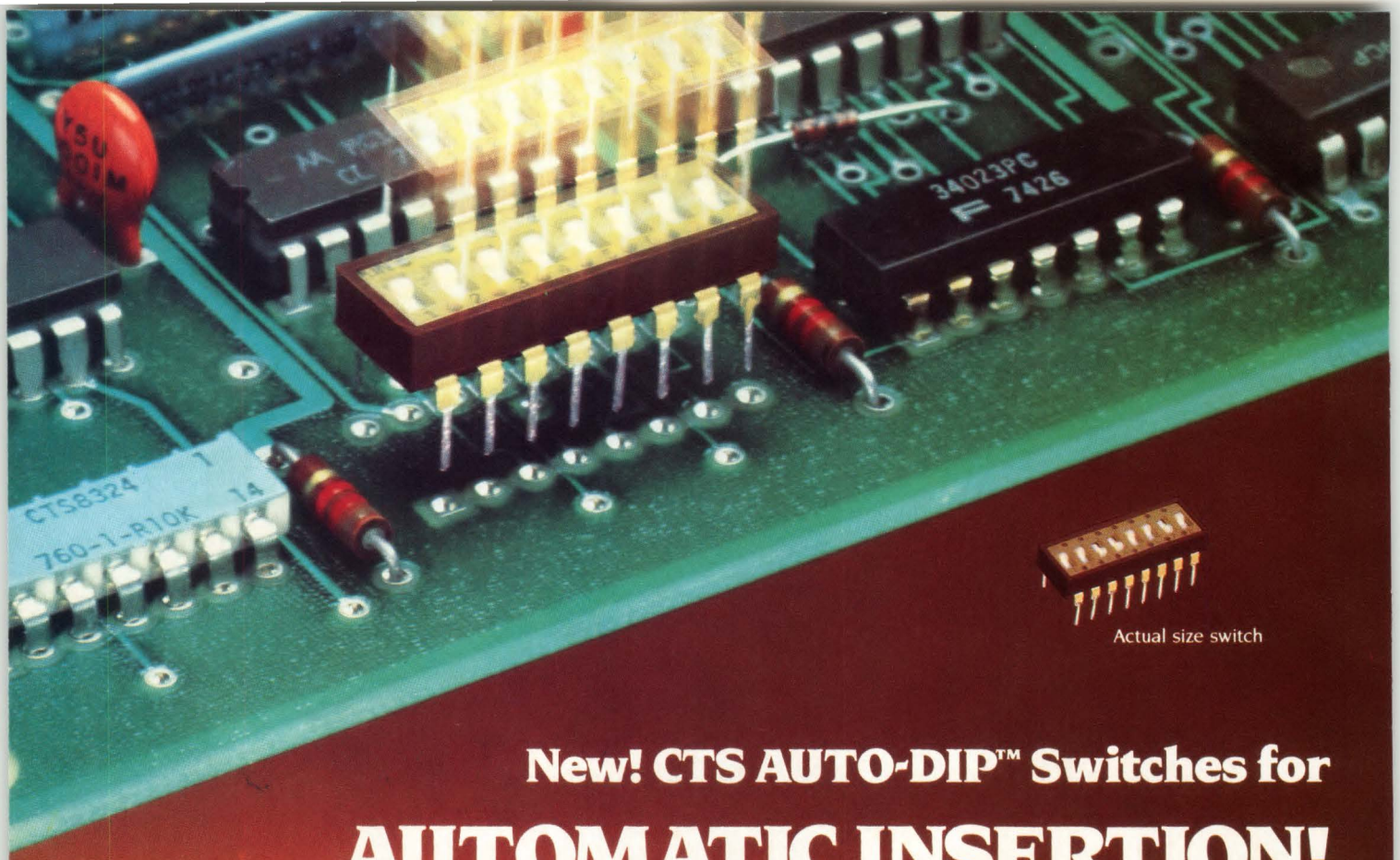

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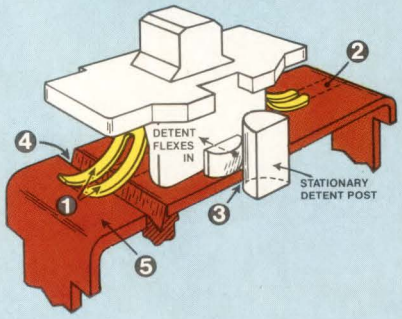

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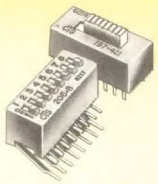

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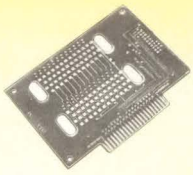

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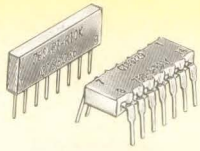

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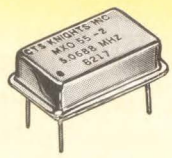

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A-d converter-filter chip serves as front end for digital signal processing

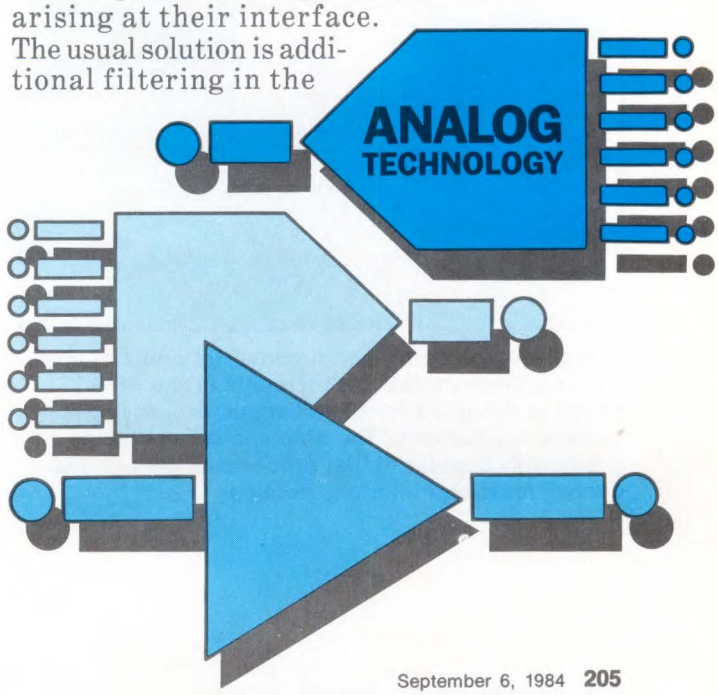
An analog-to-digital converter and an anti-aliasing filter based on switched capacitors form the analog front end for digital signal processors.

These days, almost all of the complex signal processing required in speech recognition, high-speed modems, biomedical instrumentation, and sonar systems is done by 8- and 16-bit microprocessor chips over the audio frequency range of 0 to 20 kHz. That kind of analog input is usually oversampled to minimize the anti-aliasing filtering requirements. But monolithic microprocessors need as low an input rate as possible because of their limited signal-processing bandwidth.

These contradictory requirements are reconciled in a monolithic device that combines a 10-bit analog-to-digital converter with a high-performance anti-aliasing tracking filter. Called the R5640, the chip serves as a complete front end for digital signal processors. It therefore exemplifies the increasing extent to which analog subsystems are becoming integrated.

The latest switched-capacitor filter technology enables the R5640 chip to integrate an economical voice-band anti-aliasing filter in a high-density MOS process. With the filtering problem thus solved, it becomes feasible to use low-cost, low-speed MOS a-d conversion. In fact, the chip is fabricated with a high-performance double-polysilicon NMOS process (see "Double-Polysilicon Processing Proves its Versatility," p. 207).

Since the filter and the converter are both sampled-data systems, they need synchronization to prevent an aperture problem from arising at their interface. The usual solution is additional filtering in the



Tsung D. Mok and **John R. Ambrose**
EG&G Reticon

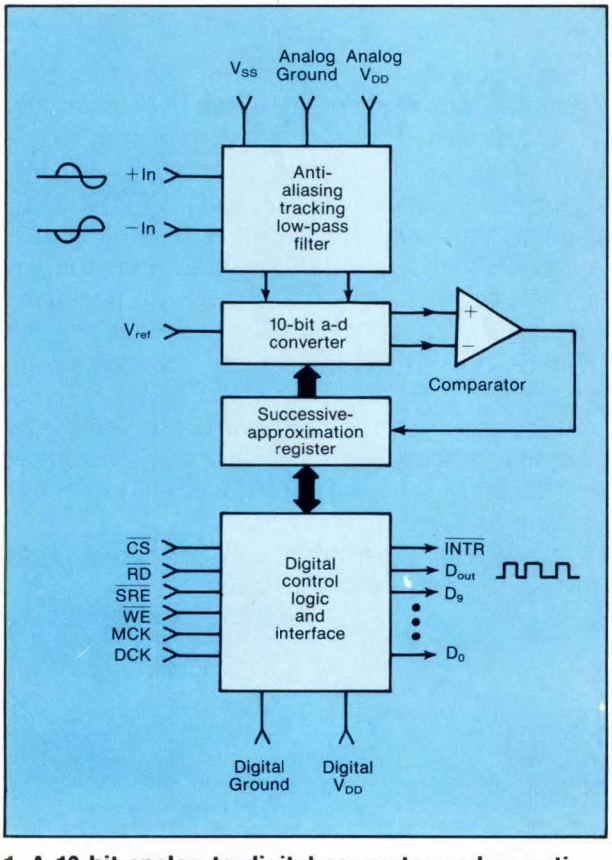
In 1981 Tsung D. Mok joined EG&G Reticon in Sunnyvale, Calif., as a design section head, after serving as a project manager for Intel's telecommunications group. His team designs and develops switched-capacitor filters and digital signal processors. He holds a PhD in electrical engineering from the University of Toronto.

The holder of an AA degree in electronics technology, John R. Ambrose is now pursuing his BS in electrical engineering at San Jose State University. He joined EG&G Reticon in 1979, where he helps develop signal processors and image sensors.

Analog Technology: Converter-filter duo

form of a continuous-time filter at the converter's input. That addition is no longer necessary when an anti-aliasing filter and converter are combined on one chip, because the circuit's internal sampling processes can now be carefully synchronized. Moreover, the device's total dynamic range is improved by the absence of the extra filter.

In summary, the integration of the entire a-d front end on one chip improves reliability, reduces component count, and saves silicon real estate. Moreover, designers can take advantage of the inherent programmability of switched-capacitor technology to realize far greater flexibility than afforded with nonmonolithic analog front-end devices.



1. A 10-bit analog-to-digital converter and an anti-aliasing filter are the key elements in the R5640, which is designed for digital signal-processing system applications. The chip can communicate easily with popular digital processors through the control logic and interface section.

The R5640 consists of an anti-aliasing tracking low-pass filter, an a-d converter with its associated comparator and successive-approximation register, and a digital control and interfacing section (Fig. 1). At the input of the chip is the anti-aliasing filter, a seventh-order elliptical low-pass filter implemented with switched-capacitor techniques. The filter feeds into the 10-bit a-d converter, which executes a successive-approximation algorithm using binary-ratioed capacitors. Both the filter and the converter employ an advanced differential analog signal-processing technique that increases the dynamic range by 6 dB and the power-supply rejection ratio by more than 20 dB compared with single-ended amplifier techniques.

The basic switched-capacitor filter employs two sets of sampling and integrating capacitors (Fig. 2). The effective time constant (R_EC_I) can be shown to be equal to $C_I(C_Sf_S)$, which depends only on the capacitor ratio C_I/C_S and the sampling clock frequency, f_S.

To maximize the useful dynamic range of the 10-bit a-d converter, the anti-aliasing filter has been given a pass-band ripple of less than 0.2 dB and a stop-band rejection of at least 60 dB. The sharp roll-off of the low-pass filter—20 dB attenuation at a frequency 1.15 times the corner frequency, f_o—allows the pass band to be precisely defined, a very useful feature for voice recognition and spectral analysis.

A maximum corner frequency of 20 kHz can be achieved at a corresponding digitization rate of more than 40 kHz, which covers the requirements of a range of diverse signal-processing applications.

Eliminating signal aliases

Since the anti-aliasing switched-capacitor filter and the a-d converter are driven by one master clock (MCK), they are internally synchronized. The corner frequency of the filter has a fixed relationship to the master clock, permitting a user to program the filter's pass band by selecting an appropriate frequency for the master clock. The nominal value of the clock-to-corner ratio (f_{MCK}/f_o) is 140 to 1.

With the ratio between the a-d conversion rate and the switched-capacitor filter's corner frequency (f_{ADC}/f_o) at 2.69 to 1, the attenuation

of the filter at half the conversion rate—that is, the Nyquist frequency—is greater than 60 dB, so that any aliased (unwanted) signal caused by the converter's sampling action is smaller than the inherent quantization noise associated with the converter.

Aliasing, or the translation of a signal from one frequency band into another, can be caused by the sampling process if the input spectrum's bandwidth is not properly limited (anti-aliased) or if the sampling rate is too low. Anti-aliasing remedies can be avoided by sampling at a rate much higher than the input-signal spectrum. However, that alternative is expensive since it requires a very fast converter and wastes signal-processing bandwidth.

Instead, the aliasing effect is minimized by using a low-pass filter for limiting the bandwidth. Sufficient signal rejection—here, a matter of 60 dB—must be provided in the stop band to keep any residual aliased signal to at most the same order of magnitude as the converter's quantization noise.

Since the switched-capacitor filter is itself a sampled-data device, a simple external bandwidth-limiting filter—half the former's sampling rate, $f_{MCK}/8$—may be required in certain applications. Often, the switched-capacitor filter's sampling rate is much higher than the bandwidth of the signal source, making extra anti-aliasing unnecessary.

The chip's anti-aliasing filter has truly dif-

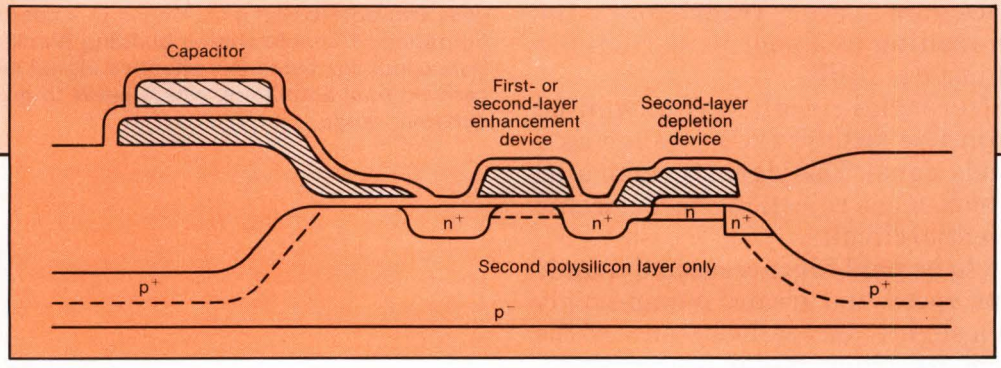
Double-polysilicon processing proves its versatility

An industry-proven technology, double-polysilicon n-channel MOS produces fast, high-performance analog and digital circuits. Moreover, it can build double-polysilicon capacitors, an essential ingredient of analog circuitry. Careful optimization of the process makes it extremely suitable for mixed analog-digital circuitry, as well. Diffusion depths and oxide thicknesses, for instance, are appropriate for high-voltage (20-V) analog circuits, as well as for high-speed digital circuits.

Double polysilicon puts three types of active devices at the disposal of an IC designer. An unimplanted enhancement-mode transistor can be fabricated in the first layer, and both an enhancement- and a depletion-mode transistor in the second layer (see the figure). The transistor in the first layer is designed to exhibit minimal 1/f noise (flicker noise), which together with an ability to handle large analog signals could give a wide dynamic range to an input stage. The transistors in the second polysilicon layer make possible the construction of high-density op amps and of comparators with sufficiently high gain.

A double-polysilicon structure sandwiching a thin dielectric layer of silicon dioxide creates a stable high-quality capacitor with very low temperature and voltage coefficients. Since the uniformity of thermally grown silicon and the area ratio of the polysilicon layers can be precisely controlled, the ratios of double-polysilicon capacitors can be matched to better than 0.1%, making it possible for designers to combine high-performance precision integrated MOS components with analog circuits. In switched-capacitor technology, capacitor ratios produce RC time constants that determine the filter characteristics. (The switched-capacitor filter techniques and the a-d conversion methods found in the R5640 depend on those accurate capacitor ratios. Binary-ratioed capacitor arrays generate the decision levels in the converter.)

Compared with bipolar analog circuits, double-polysilicon NMOS is denser and also more reliable, as current consumption follows a negative temperature-coefficient curve.



ferential inputs and accepts single-ended, as well as differential, input signals. Common-mode rejection is better than 50 dB, a useful parameter in applications involving bridge-type sensors with some common-mode bias. In single-ended operation, either the positive input (+In) or the negative input (−In) should be connected to analog ground. The other one can be used for offset nulling in critical applications by applying an opposite offset voltage at the terminal.

To meet the demands of some high-performance applications, the converter-filter can apply differential processing to analog signals and thereby overcome the limitations in dynamic range and power-supply rejection of earlier switched-capacitor filter designs. The technique takes advantage of the differential I/O nature of a basic NMOS analog building block (Fig. 3).

In a conventional single-ended NMOS operational amplifier, a differential-to-single-ended stage delivers the single-ended output; that arrangement adds complexity to the amplifier design and contributes to noise. But because the fully differential op amp needs no such conversion, its design is simpler and exhibits lower noise.

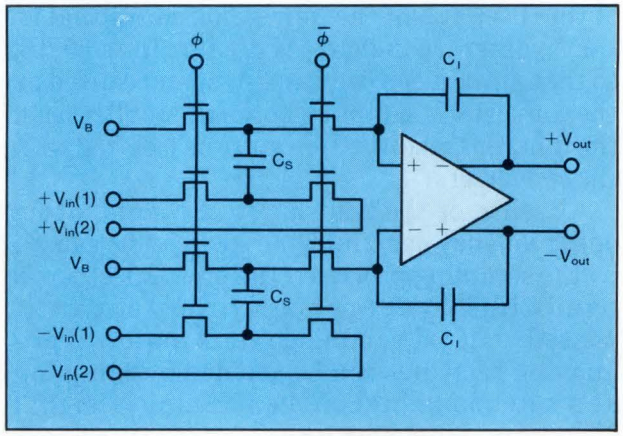
Twice the swing

The differential approach produces an internal signal swing that is double that of a conventional single-ended design. Thus the effective dynamic range is increased by a factor of two, or by more than 6 dB in the case of the R5640 converter.

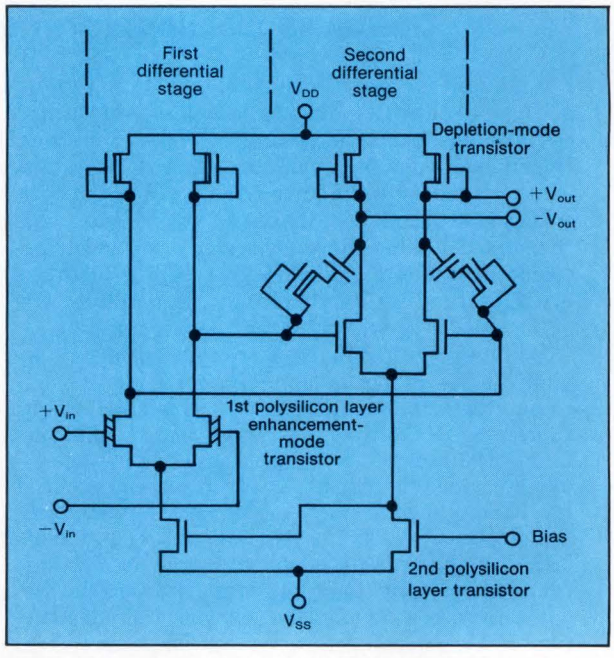
Other benefits of the simpler design are greater speed and superior power-supply rejection. In a conventional design, the substrate acts as a back gate to every transistor on the chip, often leading to a poor power-supply rejection of just 0 to 10 dB.

In the differential circuit, any unwanted signal from the substrate appears as a common-mode signal. This signal is eliminated by the common-mode rejection characteristic of the differential circuits.

The price to be paid for increased dynamic range, higher speed, and greater power-supply rejection is a slightly larger die because of the dual arrays of capacitors. However, in most de-



2. A basic differential switched-capacitor filter element is a differential integrator whose RC time constant is determined by both a capacitor ratio and the sampling rate of the switched capacitor.



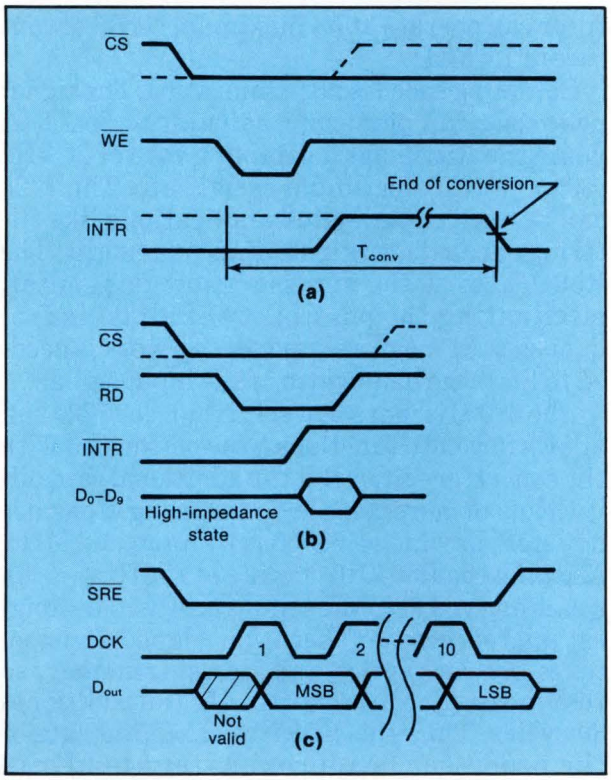
3. The converter filter's fully differential op amp uses two differential gain stages in a cascaded configuration. A simple analog building block of this type produces twice the effective signal swing of conventional amplifiers, which leads to greater dynamic range.

signs, the die is only 30% larger, an increase that is easily justified by the improvement in converter performance.

Profile of the converter

The a-d converter contains its own sample-and-hold circuit. All timing required for the successive-approximation logic and microprocessor interface is generated on chip. A precision voltage generator produces the negative reference voltage, which is required by the fully differential converter.

The user must provide a positive reference voltage to establish the full-scale conversion range. However, the reference voltage input (V_{ref}) can be used to implement an automatic gain control (agc) function—for instance, V_{ref} can be varied according to the maximum code being encoded by the converter.



4. When interfacing the R5640 with a microprocessor, the device can be treated as an address in memory space. Control signals CS and WE initiate a-d conversion (a), and the combination of CS and RD read the parallel output ports, D_0–D_9 (b). The serial output port is enabled by SRE and the 10 serial output bits are synchronized with DCK, an externally supplied data clock signal (c).

The 10-bit linear converter offers bipolar performance in a sign-magnitude coding, a format that has the best resolution around the origin and is the most suitable for examining low-level signals in high-performance applications. The technique also simplifies certain signal-processing operations, such as rectification, integration, and correlation. But for mathematical operations like multiplication and scaling, the most efficient method is to first convert—through a simple software routine—the sign-magnitude codes into two's complement.

The digital interface is compatible with the address and data bus structures of most popular microprocessors. Five control inputs are on the chip: Chip Select (CS), Write Enable (WE), Read Enable (RD), Serial Read Enable (SRE), and Interrupt Status (INTR). Those control lines allow a microprocessor to communicate easily with the R5640 either to initiate an a-d conversion or to read the converted code.

The device has 10 parallel three-state data outputs (D_0 through D_9) and a serial output port (D_{out}). The master clock line (MCK) runs both the filter and converter. An external serial data clock, which can be asynchronous, is used for the serial output.

From analog to digital

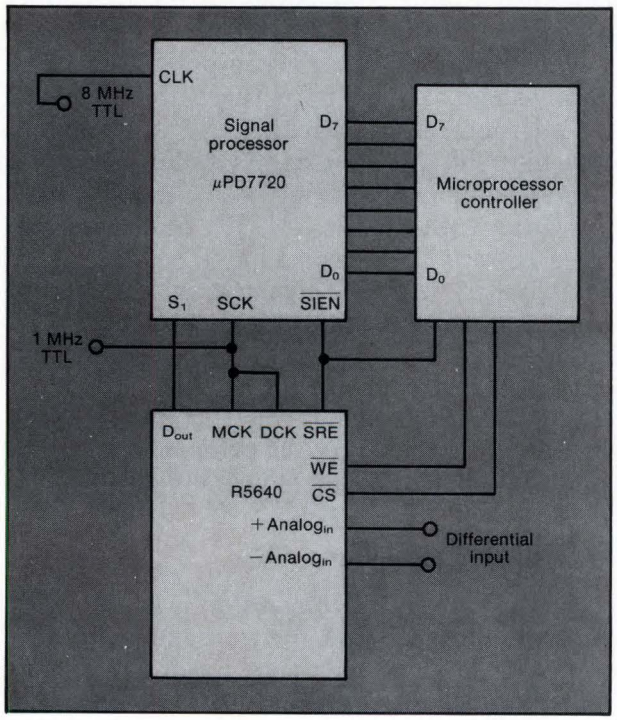
Analog-to-digital conversion is initiated by control inputs CS and WE going low simultaneously (Fig. 4), which occurs when the controlling microprocessor performs a write operation to the appropriate memory space. The minimum conversion time is typically 24 μs and takes a minimum of 52 master clock cycles to complete.

At the end of the conversion process, the output signal on INTR goes low, and the digital code corresponding to the analog input is available at both the parallel and serial output ports. Control signals RD and SRE are normally set high to hold the data output ports in a high-impedance state, so that the ports can be con-

nected directly to the data lines of a microprocessor-based system.

To activate the parallel ports, $\overline{CS}$ and $\overline{RD}$ must be set low by having the microprocessor perform a read operation. Serial output port D_{out} is enabled by bringing $\overline{SRE}$ low. Then the entire 10-bit code can be clocked out of the serial port on the falling edges of the first 10 externally supplied pulses to the serial data clock pin (DCK). If fewer than 10 bits are required, a burst of the appropriate number of data clock pulses can be applied. All read and write operations—that is, start conversion—can be performed asynchronously. To prevent possible aperture jitter, however, $\overline{WE}$ should be synchronized with the master clock.

The R5640's digital control and interfacing



5. Data flows smoothly between the R5640 and the NEC μPD7720 digital signal-processing microcomputer, since the converter-filter's serial output connects directly to the microcomputer's asynchronous serial input. Both devices can share a common clock signal.

section allows the device to connect to a special signal-processing microcomputer such as the NEC μPD7720 or to a general-purpose microprocessor such as the 68000.

Microprocessor interfacing hints

Interfacing the chip with the signal processor is fairly straightforward (Fig. 5). Its serial output is simply connected to the microcomputer's asynchronous serial input (S_1). The converter-filter's master clock signal is shared with the serial clock of the signal processor, so that the microcomputer can operate at its maximum clock rate of 8 MHz and the converter-filter can operate at its maximum serial output rate of 1.4 MHz.

Sampling speed is not a limitation. The signal processor can perform a calculation in 1.6 μs while the R5640 has a sampling rate of 20 kHz (50 μs) at the maximum serial rate. The 7720 can be used in dedicated applications like filtering or calculating instantaneous energy. The R5640 acts as the necessary low-pass filter, eliminating the possibility of aliasing frequencies. At most, a simple RC network is needed to limit the bandwidth of the input signal.

The 68000 is more powerful than the 7720 and allows far more functions to be performed with the converter-filter. But the additional capability leads to more complex interfacing. Consider a system in which a 68000 is running at 8 MHz, allowing the R5640 to operate at 2 MHz (Fig. 6), a rate arrived at in the following way. The longest microprocessor operation, signed division, takes 150 clock cycles, and accessing memory so that the result can be stored takes an additional 30 cycles. Thus the effective sampling rate of the processor is approximately 40 kHz (8 MHz/180).

Simply dividing the 68000's clock by four lets the converter-filter use the same clock. However, the R5640's serial output cannot be used. Instead, parallel outputs are more effective: Since the 68000 has 16 parallel data lines, no multiplexing is required for low- and high-order bytes, as in other microprocessors.

All inputs and outputs in the 68000 application are treated as memory locations, through the technique known as memory mapping. A particular I/O device can be decoded by using a multiple-input AND gate with select inputs in-

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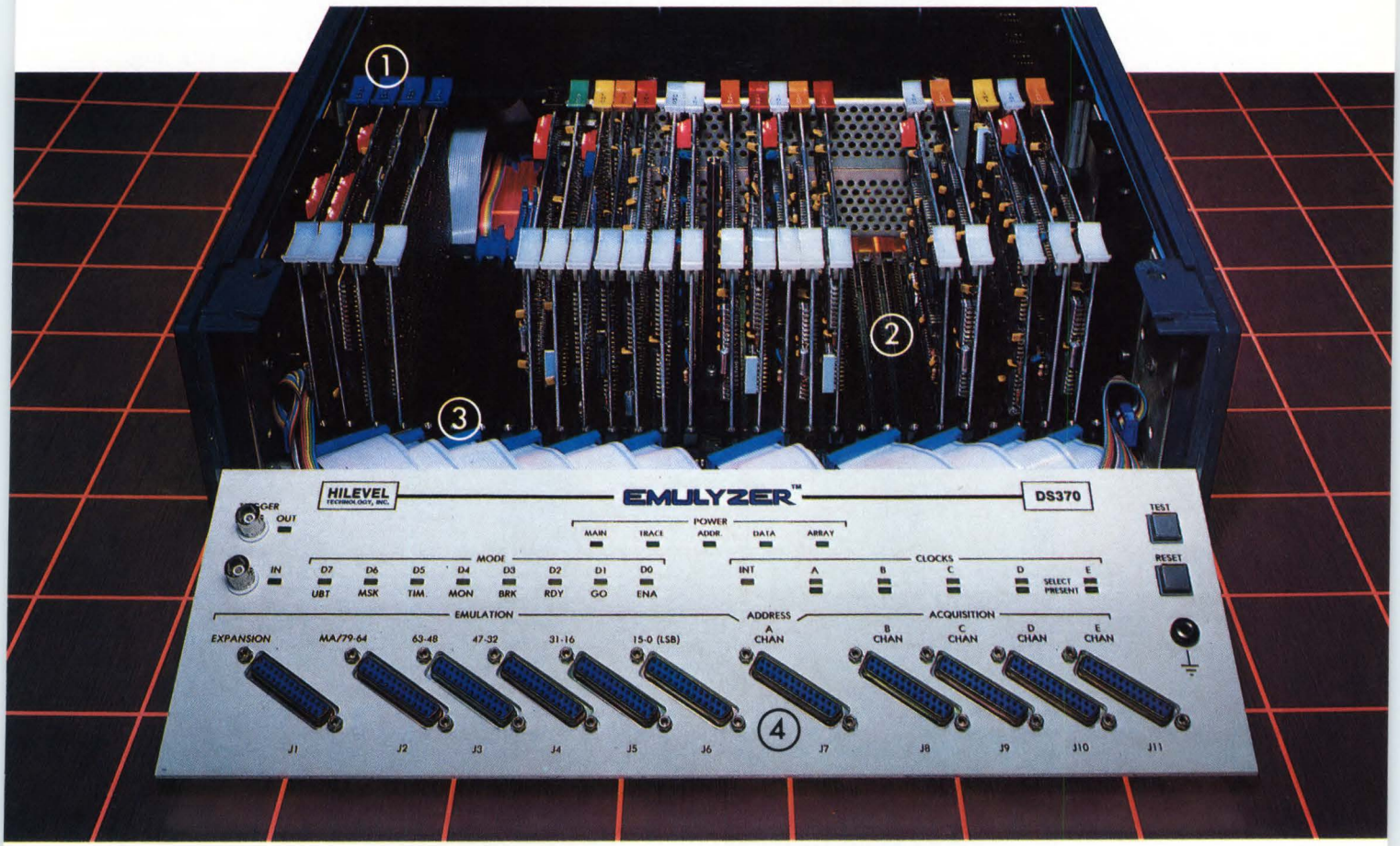

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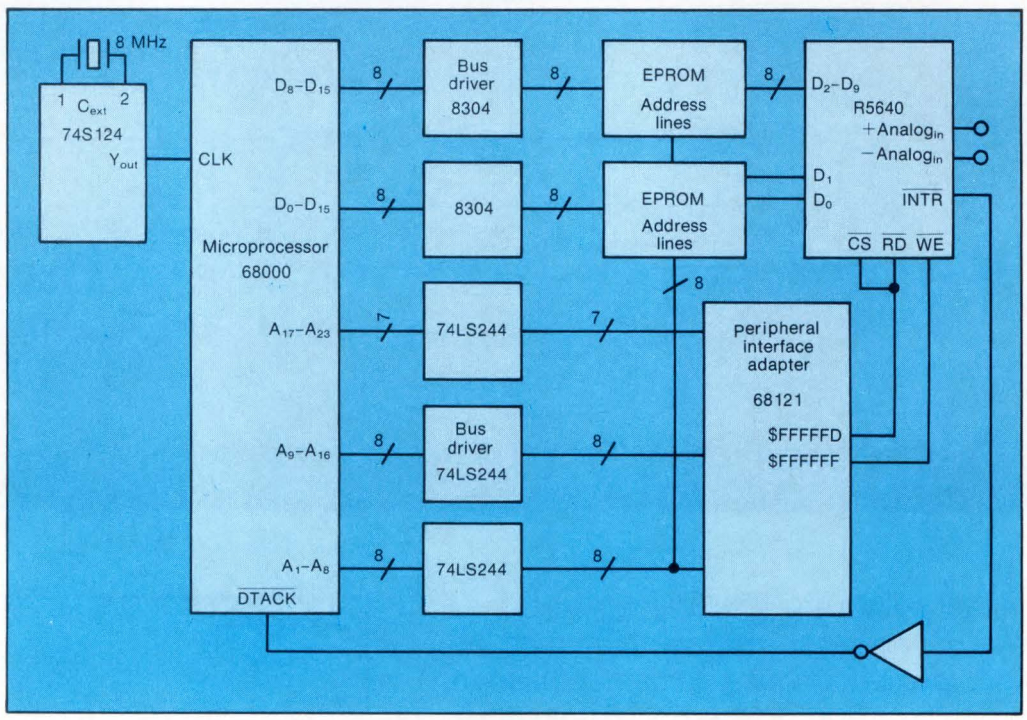
verted. In that way, any I/O locations can serve as the R5640 parallel output port. Usually, address line A_{23} is used for I/O selection; when any I/O device is desired, A_{23} is pulled high. Together with the AND-gate decoding for port selection, that step constitutes I/O selection for the R5640.

Address line A_{23} can also serve as a control line on the $\overline{CS}$ pin to stop the conversion process when it is not needed. The $\overline{RD}$ line is controlled by ANDing the R/$\overline{W}$ signal of the 68000 with the $\overline{INTR}$ signal of the R5640.

For simple startup of the converter, it is best to use the reset vector of the 68000, which starts from memory location 0. On reset, the program counter loads the supervisor stack pointer with the first two words and is then loaded with the next two words from low-order memory. It jumps to that location immediately to execute the next command. Under that setup, a fixed polling method can be created so that the program accesses the R5640, reads a word, processes it, and sends the results to system RAM or another I/O device.□

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



6. The powerful 68000 16/32-bit microprocessor treats the R5640 as a memory location. With the chip's three-state parallel output ports, converted code can be sent to the host processor using a simple read operation.

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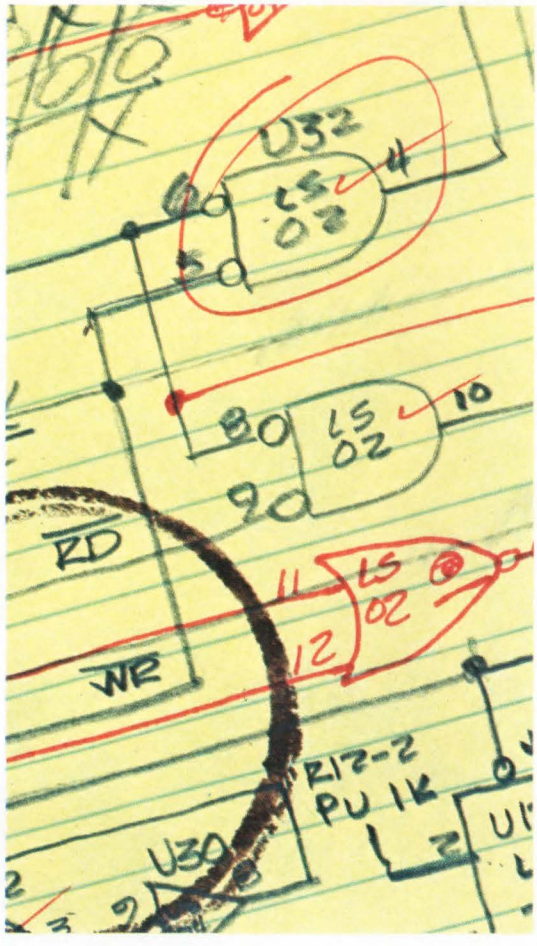

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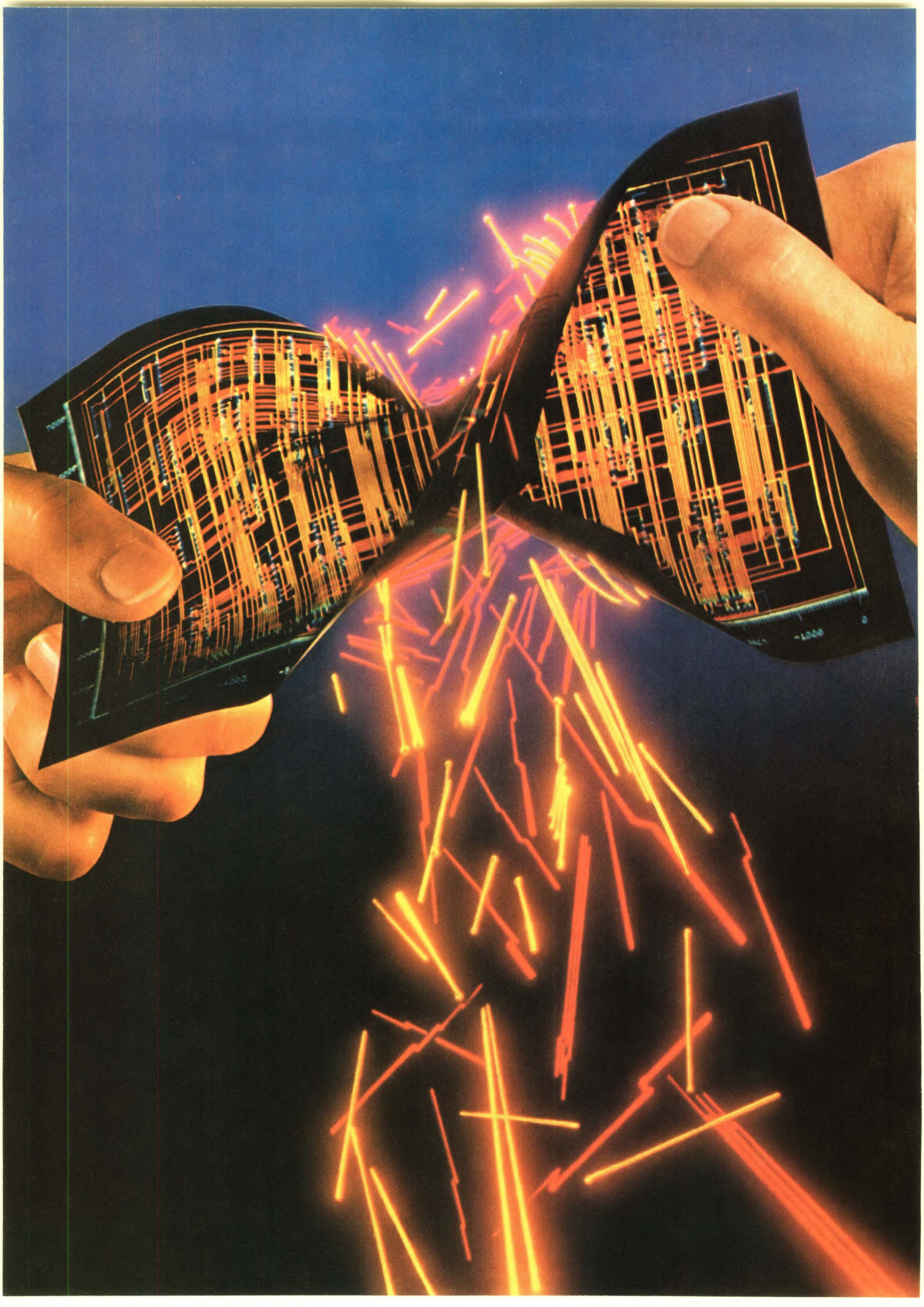

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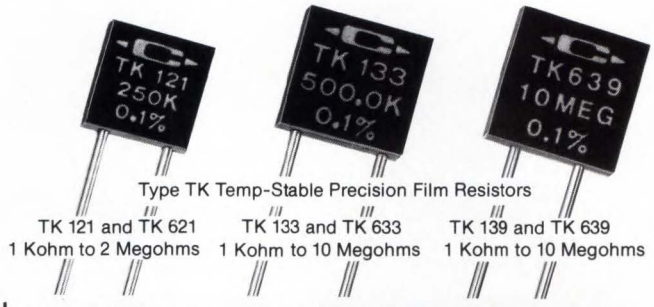

Type TK Temp-Stable Precision Film Resistors

TK 121 and TK 621
1 Kohm to 2 Megohms

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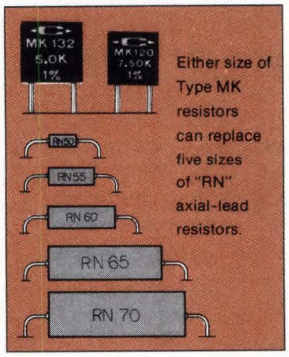
• Resistance Tolerance	±1.0% is standard, to ±0.1% on special order, depending on value and model.			
• Wattage	0.5 Watt	—	0.75 Watt	—
• Voltage	200 V	200 V	400 V	400 V
• Temperature Coefficient	50 PPM/°C	80 PPM/°C	50 PPM/°C	80 PPM/°C
	Temp Range: −15°C to +105°C, ref. +25°C.			
• Package Size	.250" square, .100" thick		.300" square, .100" thick	



Either size of Type MK resistors can replace five sizes of "RN" axial-lead resistors.

These full-size photos comparing the Type MK resistors to "RN" style axial-lead resistors show that the largest Type MK, which is rated at 3/4 watt, requires less board space than the 1/20 watt "RN 50".

And within their voltage ratings, both sizes of Type MK resistors can replace five sizes of "RN" resistors, including the 1/2 watt "RN 70" which requires 10 times the board space of the MK 132 !

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Type TK Temp-Stable Precision Film Resistors provide a combination of performance advantages that are unique in a miniature resistive component:

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- **Precision Tolerances:** ±1.0% is standard, and tolerances as close as ±0.05% are available on special order.
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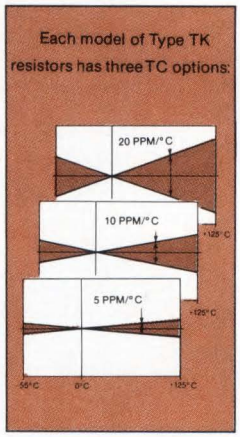
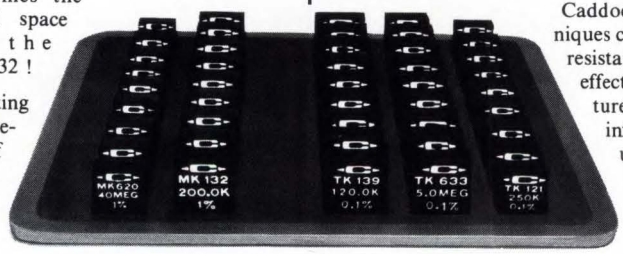
- **Two Power Ratings:** .2 watt and .3 watt.



The Model TK 121, TK 133 and TK 139 precision film resistors have demonstrated performance which meets the requirements of Mil-R-55182/9 for thermal shock, moisture resistance, shock and vibration, dielectric withstanding voltage and low temperature operation.



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HIGH PERFORMANCE FILM RESISTORS

CIRCLE 105

Analog I/O boards ensure speed and accuracy in VAX-based data acquisition

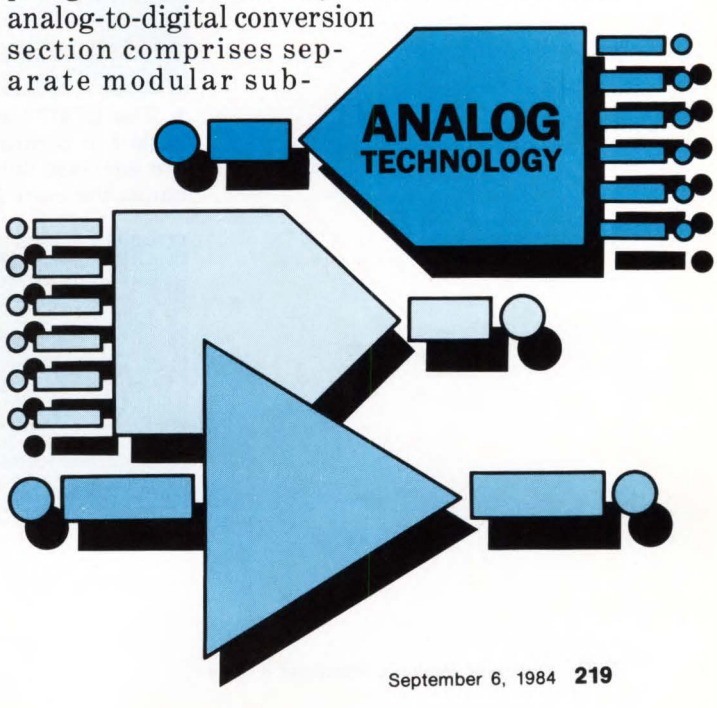
A bit-slice controller and a 64-kword FIFO buffer compensate for slow host systems, allowing data transfer at 250,000 samples a second.

The movement of minicomputers and superminicomputers out of a central computer room and into individual departments and laboratories promises to bestow much more computer power on those who most need it—the scientists and engineers involved in research and development. These users will probably want to apply the machines as single-user, single-experiment workstations dealing with real-world phenomena. In other words, the computers will need extremely fast and accurate analog I/O interfaces, preferably smart enough to free both system and user from involvement in real-time hardware management.

The target of the DT1771 series of analog interface boards is the computer most widely used by the OEM design community—Digital Equipment's VAX, running under the Unix or VMS operating system or under the VAXElan run-time executive. The boards also serve the needs of users who continue to work with the PDP-11 and the process RSX operating system.

Developing a really fast and accurate analog I/O interface for VAX systems has pushed data-acquisition system design to new limits. The DT1771 series depends on an intelligent, buffer-based architecture (Fig. 1) to achieve 12-bit sampling rates of up to 250 kHz—data transfer rates beyond the capabilities of simple programmed I/O. It also avoids the subtle but devastating timing errors that can plague unwary users of purely DMA types of interface, and the process is totally transparent to the user.

The key elements are a dedicated bit-slice control processor and a tightly coupled 64-kword ring buffer that overcomes the crippling effects of host system latencies. The analog-to-digital conversion section comprises separate modular sub-



Andrew Davis, Data Translation Inc.

Andrew Davis, vice president of marketing and sales, joined Data Translation in Marlborough, Mass., four years ago. Prior to that, he was involved with product marketing at Data General. He holds a BSEE and an MSEE from Cornell University and an MBA from Harvard University.

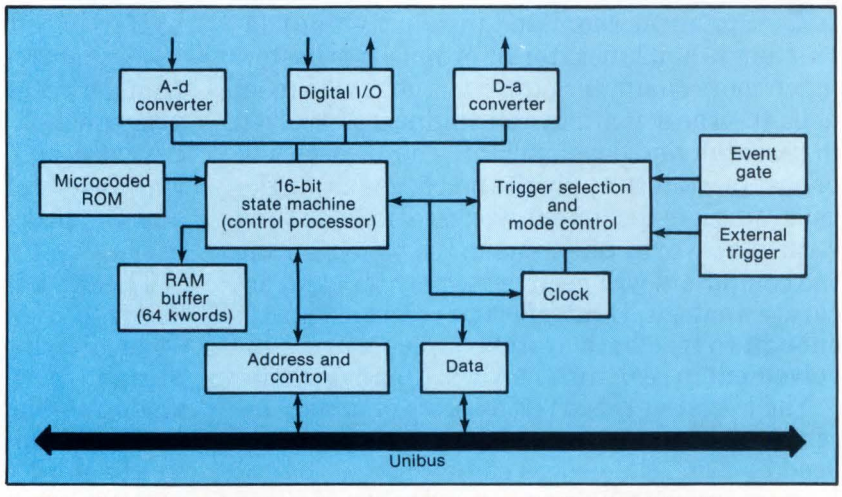
systems that enable users to specify different analog input characteristics (see the table, below).

Doing up to 24 MIPS

The control processor handles the analog subsystems, the on-board time base, and the interface with the Unibus of a VAX or DPD-11 system (see "Adapting Unibus to the VAX," opposite). Implemented as a 16-bit state machine, the bit-slice control processor is nominally specified for an execution rate of 8 million instructions/s. The processor employs multiple levels of parallelism in its design, so that it can simultaneously execute more than one operation per instruction. In effect, that design can push the aggregate execution rate to between 16 and 24 million instructions/s. To VAX systems, none of which is rated for more than 2 million instructions/s, the control processor appears to respond instantly.

An analysis of the control path of the state machine (Fig. 2) underscores the breadth of its power and capabilities. The state machine is microprogrammed with a 48-bit-wide, 512-word control store PROM and has a 125-ns cycle time. The output of the machine's 48-bit-wide instruction register controls the data-path reader and writer, the on-board memory, the Unibus interface, clocking and triggering, and analog functions. Furthermore, it determines the selection of a single condition code reflecting the results of the most recent ALU operation, Unibus function, program mode, or analog service request. Both the condition code and an encoded branch control field are sent to a branch PROM, which controls selection of the next program address.

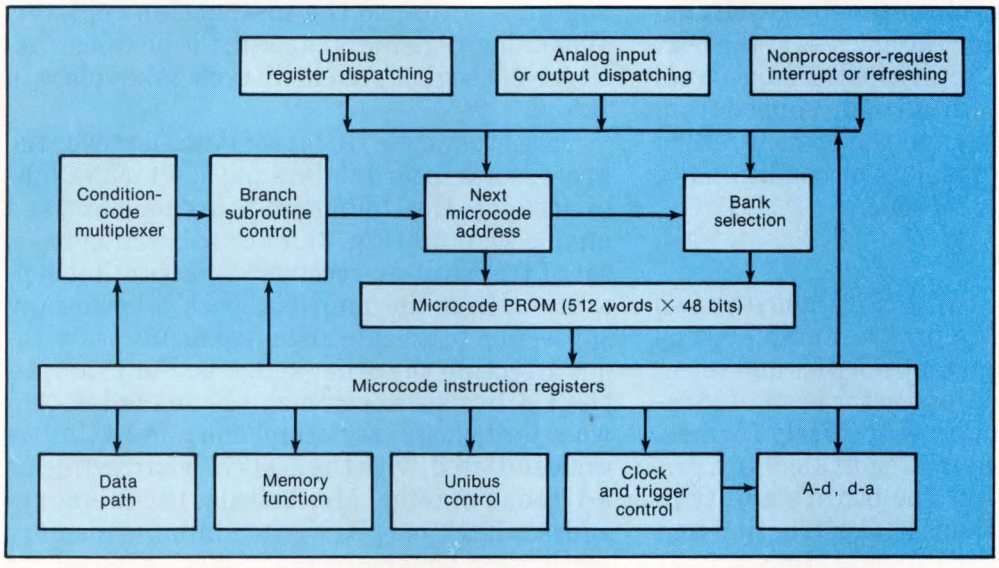
That program address may simply be the next sequential location. On the other hand, the



1. The DT1771 analog interface boards use a dedicated bit-slice processor to control the analog subsystems, the on-board time base, and the interface with a VAX's Unibus. Implemented as a 16-bit state machine, the control processor can execute 8 million instructions/s.

A-d modules for the analog interface series

Class	Analog input channels	Full-scale range (V)	Model
12-bit converter, 250 kHz	16 single-ended or 8 dual	1.25, ±1.25, 2.5, ±2.5, 5, ±5, 10, ±10	DT1771
12-bit simultaneous sample-and-hold converter, 100 kHz	4 single-ended	10, ±10	DT1778
16-bit converter, 100 kHz	4 dual	±10	DT1777



2. The 16-bit state machine controls the board's functions through a microprogrammable 48-bit-wide instruction register, which receives its code from a 512-word control store PROM.

Adapting Unibus to the VAX

The Unibus is a hardware developer's primary link to a VAX computer. An asynchronous bidirectional bus, it lets medium- and low-speed peripheral devices communicate with VAX systems and also affords the simplest VAX access port for custom devices. Although the Unibus is used in both VAX and PDP-11 systems, each computer addresses it differently, the VAX encoding addresses in hexadecimal form and the PDP-11 in octal form.

VAX computers contain a Unibus adapter that connects the computer to the bus subsystem. Through the adapter, the processor can access registers on the Unibus, and devices on the bus can conduct DMA transfers with VAX memory and also interrupt the processor. The adapter breaks the sequential addresses that are broadcast by Unibus devices into noncontiguous 512-byte blocks for the VAX physical memory. (Under the VAX architecture, addresses that are contiguous in virtual memory are allowed to be noncontiguous in physical memory on 512-byte boundaries.) Since Unibus devices can address only 256 kbytes, the adapter expands these addresses to give access to the VAX's full physical address space.

The DT1771 analog interface board uses a block-mode DMA technique to transfer data over the Unibus at the highest allowable rate. In the absence of conflicting requests from other nonprocessor requesting devices (dubbed NPRs in Unibus terminology), the interface board will transfer 16 words over Unibus, relinquish the bus for at least one cycle so that the CPU or other users can access the bus, and then become bus master for another 16-word transfer. The board defers to requests from other NPR devices on the bus but only after transferring at least two words. The peak rate of block transfers is 1 Mbyte/s, a significant percentage of the Unibus's maximum rate (1.5 Mbits/s). By using the bus bandwidth efficiently during block transfers, the interface minimizes its total time on the Unibus and thus helps to preserve host system response.

Bus use and throughput are further improved by providing high-speed synchronization through metastable-hardened registers. A metastable condition arises when an active clock edge hits any flip-flop just as the input is changing state; the event can cause the cross-coupled latch at the flip-flop output to reach a balanced, symmetrical state, which it holds for several microseconds before returning to either state. A two- or three-stage register could reduce the probability of the condition occurring but would add delays to throughput. Improved circuitry in the metastable-hardened registers not only reduces the probability of entering a metastable condition but can also resolve this occurrence in only 6 ns—nonhardened devices average 60 ns.

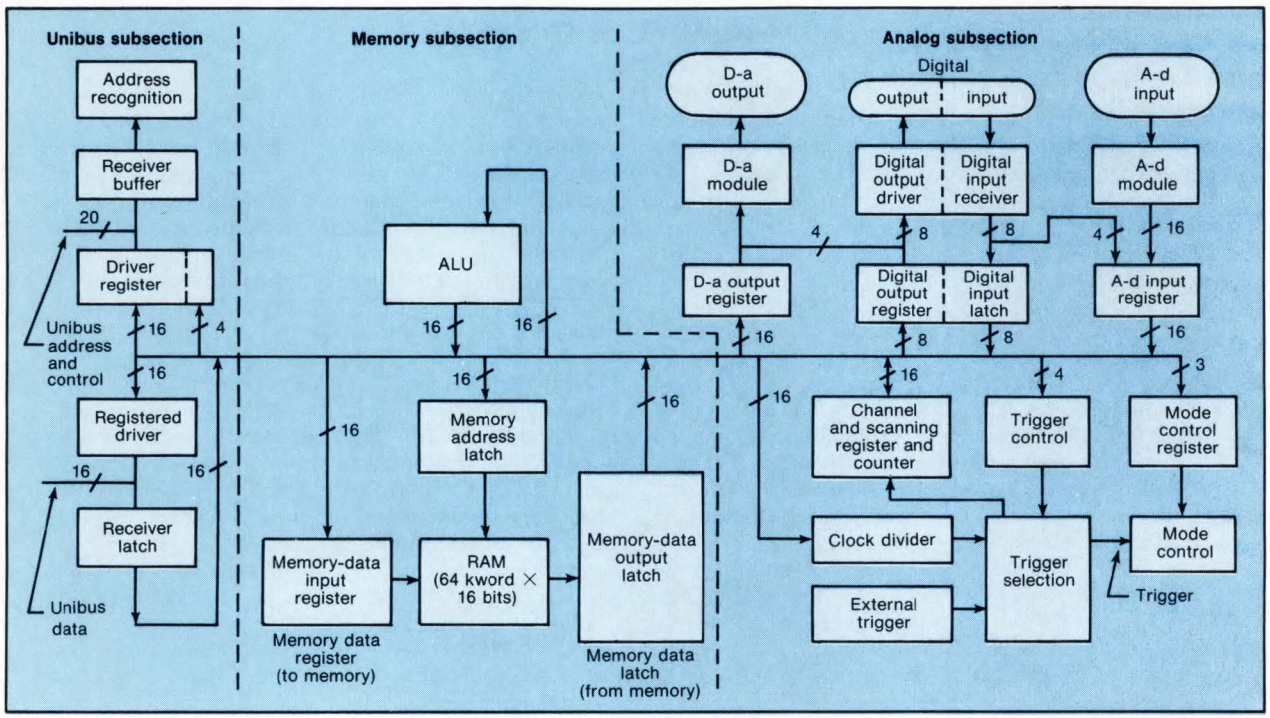
microcode can call a subroutine by specifying its address and stacking the address of the next sequential location. A return instruction allows the next microcode address to be popped from the stack. Both the call and the branch-return instructions may be absolute or conditionally dependent on the selected code.

Branching addresses

A special branch or call facility, aided by two external PROMs and a programmable array logic (PAL) circuit, can set priorities and select the next microcode address on the basis of 18 inputs. That arrangement essentially forms a high-speed decision matrix, equivalent to a priority multiway branch. The board's ability to recognize precisely the right instruction and prepare it for execution in real time is what makes the state machine so efficient and fast.

At this point the next microcode address is sent to the control store PROM, which presents the instruction to the instruction register. When that register is clocked, the next instruction cycle begins. An entire cycle takes place in 125 ns.

Once every cycle, 16 bits of data flow over the processor's internal data path, which is subdivided into the Unibus, on-board memory, and analog sections (Fig. 3). Each subsection has a set of transmitter-receiver registers that separates it from the main data path, allowing any subsection to execute an on-going process without affecting the other sections. For example, the Unibus subsection can be loaded with a word for transfer to host memory and a Unibus cycle initiated, with the DT1771 board acting as a Unibus master. Meanwhile, the memory-address latch may be written into the memory section and a memory-read function issued. At the same time, data from the analog-to-digital converter may be arriving at the holding register in the analog section. That highly parallel



3. One reason for the control processor's high performance is the independent transmitter-receiver registers of the Unibus, memory, and analog subsections. While one subsection is executing a process, the internal data path is free for use by the other subsections.

architecture deserves the credit for the processor's extremely high performance.

Of course, the difficulties virtually any general-purpose computer has in sampling analog signals at rates over a few kilohertz are due primarily to host system latencies and unpredictability. Present a-d converters can acquire and convert hundreds of thousands or even millions of samples a second, but the computer's response can be blocked by its process management activity or by peripheral devices. As a result the computer might miss some data points, with its file of converted data then having random discontinuities. To date, the most common "solution" to this problem—time stamping all data points, or collectively storing timing and conversion data—proves more useful for detecting than preventing discontinuities.

The board's architecture overcomes that problem by isolating data acquisition from the host system interface. A 64-kword ring buffer delivers the elastic coupling necessary to synchronize the analog interface and the host system (Fig. 4).

All data transfers go through this buffer in a first-in, first-out (FIFO) fashion. The data from the a-d converter enters the buffer location designated by the input address pointer, which is incremented after the data has been stored. Similarly, data is removed from the FIFO location designated by the output address pointer. Both address pointers increment in the same direction.

As a ring buffer, the FIFO buffer has no beginning and no end. Whenever a pointer reaches the end of the buffer, it is automatically reset to the beginning; thus both pointers follow each other continuously—without collision—around the buffer's address space. The distance between the pointers varies as host system latencies affect data transfers over the host bus.

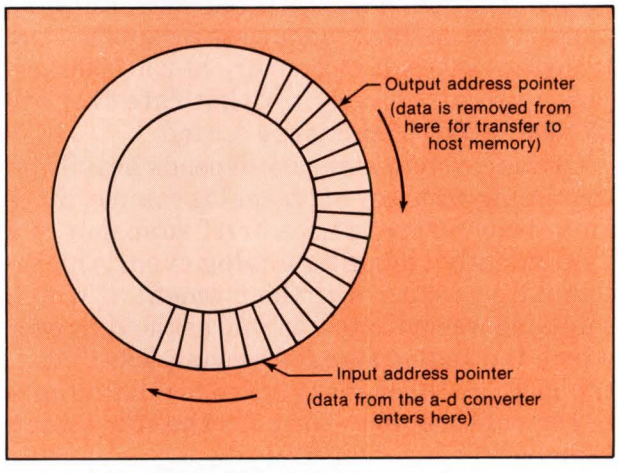
Data 'round the ring

The configuration of the buffer, 64k by 16 bits, allows even the fastest a-d converter—the 12-bit, 250-kHz multichannel input module—to be synchronized with the Unibus. That 12-bit module streams conversion data into the ring buffer at a rate of 4 μs/word, yet the buffer's size gives the host system up to 250 ms (64k $\times$ 4 μs) to define and initiate a DMA buffer transfer.

The wide speed matching of the ring buffer not only yields high performance but also reduces host system overhead significantly. The timing compliance of the ring buffer makes interfacing with the I/O board appear simple to the operating system; thus complex tasks like double buffering or buffer look-ahead are avoided.

What Unix needs

That simplicity merely increases the efficiency with which a host system runs under the VMS or RSX operating systems, but it is essential for Unix-based systems. Until now, the only way standard Unix could serve real-time interface applications was through custom extensions. The analog interface board can continuously sample data and transfer it to disk at



4. A 64k-by-16-bit FIFO ring buffer synchronizes the transfer of data between the analog interface and a host computer. Even though data can stream in at a rate of 4 μs/word, the buffer is sufficiently large to give the host computer 250 ms to define and initiate a DMA transfer.

100 kHz; though the rate is limited primarily by existing disk technology, it is virtually unheard of for standard Unix applications.

When it comes to the maximum continuous throughput to host memory, the real-time performance difference between VMS and Unix is easy to explain. Whereas VMS sets fixed real-time priorities and uses a queued I/O system, making it relatively predictable, Unix dynamically assigns process priorities inversely with respect to the time the CPU requires to execute it. Thus Unix can initially assign data acquisition and other I/O-intensive processes a high priority, but when they require CPU time, Unix brings them to a lower priority. Though that feature maintains an acceptable system response to multiple interactive users, it renders system response unpredictable in real-time applications.

Unix also lines up interrupt requests by types, so that a real-time I/O request may be queued behind less critical requests. Running under VMS or RSX, the fastest a-d module can transfer data to host memory at 250,000 samples a second; under Unix that rate drops to 150,000 or 200,000 samples a second.

Overall system accuracy depends heavily on the timing accuracy of an analog sample. Since an a-d converter takes a brief snapshot of a dynamically changing analog event, the information concerning the moment at which sampling was initiated, as well as the time over which the analog signal was sampled (that is, the aperture time), is as critical to relating data to the real-world event as is the conversion value.

On-board timing

An on-board pacer clock generates the timing necessary for critical data-acquisition applications. Accurate to within 100 ppm over 0° to 70°C, the clock can be programmed for more than 65,000 frequencies ranging from 1 Hz to 1 MHz, with jumper-selected primary frequencies of 16 MHz, 1 MHz, and 62.5 kHz. An external trigger initiates simple a-d and d-a functions, whereas an external gate is used for sophisticated sampling activities like signal averaging. An End of Conversion output from the a-d board may serve as a successive trigger for burst-mode sampling.

Simple data acquisition is the most elementary sampling mode, triggered internally or externally. Here the user specifies the number of the first analog channel, the triggering mode, whether the process will require single or multiple channels, and the value of the optional programmable gain amplifier. Users may also opt for one conversion per trigger or multichannel scanning at each trigger. The internal triggering rate is controlled by a user-selected clock frequency. For burst sampling, conversions occur at the maximum speed of the a-d subsystem.

When data is being acquired continuously, the control processor transfers conversion data to the on-board ring buffer and subsequently to a buffer area in the host memory, according to the starting address and length of the buffer, both specified by the user. Additional data can be gathered by simply providing new data buffers in host memory.

With the ring buffer synchronizing the data-acquisition and memory-transfer rates, the flow of data never breaks at buffer switches. Only a ring buffer overflow or underflow can interrupt continuous data acquisition. Both these error conditions can be avoided, however, as the ring buffer allows at least 250 ms for buffer switching, even with the fastest a-d conversion module.

Before and after the fact

Two powerful modes developed for data acquisition applications are pre- and post-gate sampling. In the former mode, data is collected before and after a gating event. The user selects the number of pre-gate samples to be retained and initiates conversions. The acquired data is cycled in the FIFO buffer. When an external gating event occurs, the most recent pre-gate samples are transferred from the FIFO buffer to the host memory, and sampling continues. That sampling scheme proves valuable when the conditions leading up to an event, as well as those occurring during and after the event, are of interest.

Post-gate sampling allows a specified number of samples to be collected and transferred to main memory after the event occurs. The countdown mode, which is related to post-gate sampling, does not depend on external events to

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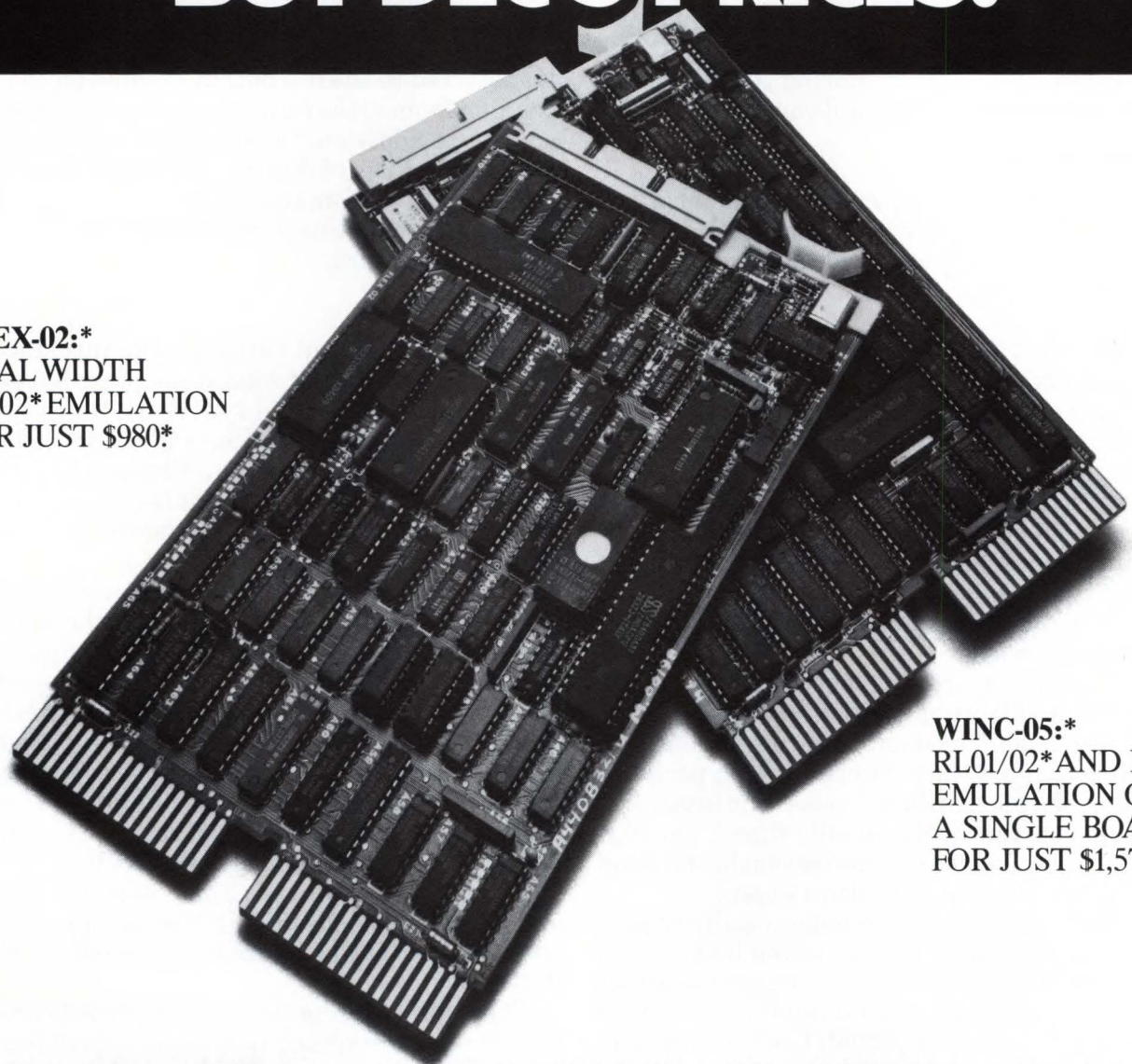

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CIRCLE 106

collect a specified number of samples.

For more sophisticated requirements, on-board histogramming can be used to analyze unknown classes of phenomena. In that case, the board's local memory is configured as a multibin accumulator, storing the number of occurrences of a unique a-d conversion value.

Plenty of room

The width of each accumulator determines the number of stored occurrences and is dictated by the resolution of the a-d converter. For example, a 12-bit board has 4096 (2^{12}) unique conversion values, but a 16-bit a-d converter has 65,536 (2^{16}) values. Since the local-memory complement is 64k by 16 bits, a single-channel histogram collected with a 16-bit a-d converter is limited to 16 bits in each accumulator, for a maximum of 65,536 occurrences of any single conversion value. A 12-bit a-d may be assigned 32-bit accumulators, which can compile a histogram of more than 4.2 billion occurrences of one value before overflowing. Histograms for up to eight channels of 12-bit data can be compiled simultaneously.

For signal averaging, periodic phenomena are repeatedly sampled to improve the signal-to-noise ratio. The number of conversions performed during the synchronization period—that is, the phenomenon's repetition interval—is kept constant and critically timed. The conversions performed during one synchronization period are collectively called a sweep.

Signal-averaging techniques usually trigger a sweep through a phase-locked loop, which ensures that each conversion trigger has an accurate phase angle and minimal jitter within the synchronization period. Users can specify up to 16,384 conversions in a sweep, with the results of each current sweep stored in the first 16 kwords of local memory. The remainder of the local memory is organized into 16,384 accumulators, each 32 bits wide and each holding the results of the same numbered conversion in each sweep. In other words, accumulator 1 holds the sum of the first conversions in each sweep, and so forth. That action, combined with the simultaneous sample-and-hold a-d module, can average the signals of four channels, all sampled within 10 ns of each other.

When needed, d-a conversion outputs can be driven continuously either through the host's memory or through the on-board ring buffer. In a pre-gating d-a conversion mode, an external event initiates data transfers.

During continuous d-a operation, data can be transferred to the d-a output module on each trigger from either an internal or external source. In addition, the interface board provides eight lines of digital I/O, which may be read exclusive of analog I/O activity. Four of those lines can be used in conjunction with a 12-bit analog word.

Creating speech

Just how fast and versatile the interface board is comes to light when a computer is used for speech analysis and synthesis. Since the board adds direct acquisition and output capabilities to the computer, data files can be analyzed as soon as the experiment is completed or even reviewed while the experiment is in progress.

In the system, the DT1771 interfaces with a VAX-11/730 under VMS. It records the input speech waveform and then plays back the output file, which contains the synthesized speech pattern. Only six of the eight analog channels are used (Fig. 5); the remaining two are grounded to minimize input noise. With the aggregate sampling rate across the six channels being 150,000 samples a second and the experiment lasting 1 minute, the board collects 9 million data words, or 18 Mbytes. That volume of data cannot be stored directly in host memory; instead, it is stored on a disk connected to the Unibus.

The application program that records and synthesizes the speech is split into three segments. The first acquires the data and transfers it to disk; the second extracts the data from the disk, analyzes it, synthesizes the new speech pattern, and returns the results to the disk; the last segment transfers the disk data to the d-a subsystem of the DT1771 and sends it to the audio amplifier and the display unit. Segments 1 and 3 operate in real time, segment 2 does not.

A subroutine library called VMSLIB greatly simplifies the writing of the real-time segments of the program. Thanks to the library, an application program written in any language under VMS needs only a simple set of subrou-

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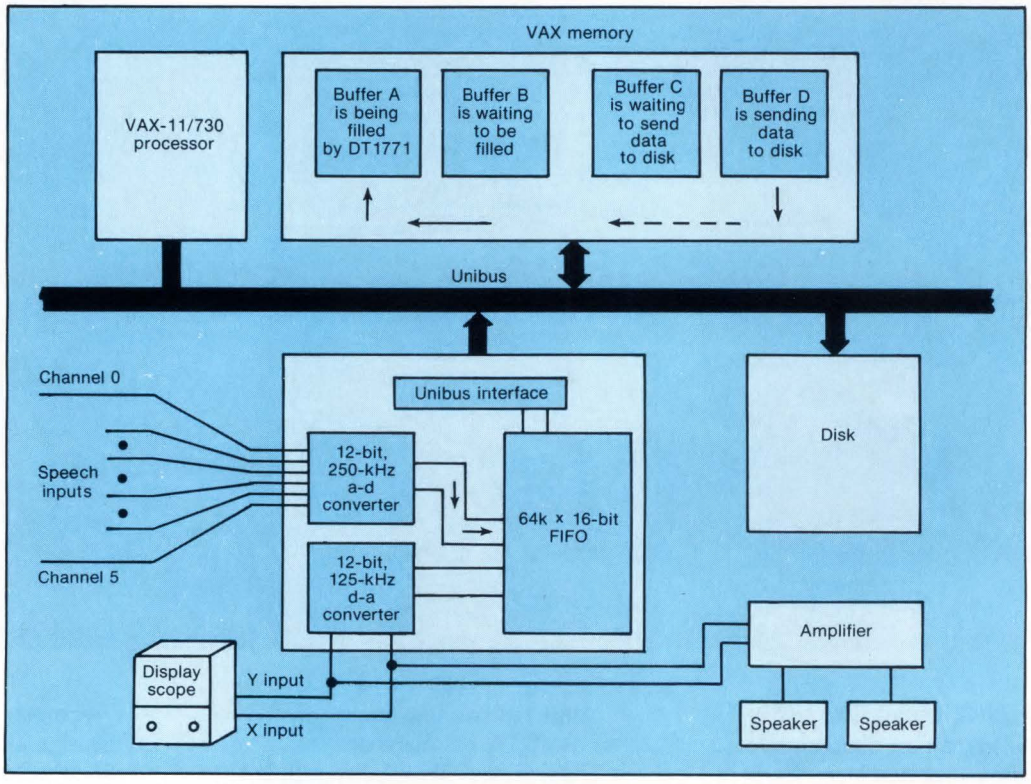
tine calls to set the functions of the board and to control the disk transfer operation.

The program listing for Segment 1 (p. 230) shows the subroutine calls under Fortran that acquire the data that will be sent to disk. For the sake of clarity, the library's error-checking procedures are not shown.

The board is set up for continuous data acquisition with on-board clock triggering and a scanning operation for each trigger. At 40-μs intervals, the clock generates a trigger, the six channels are scanned sequentially, and six words of data are collected. The board then resets its multiplexer to channel 0 and waits for the next trigger. Data from the a-d converter flows into the FIFO, where it awaits transfer to the host memory. For its part, the host can take as long as 420 ms to respond before a single data point is lost. Each time the board gains control of the bus, it transfers a block of 2 to 16 words before relinquishing control. The data-acquisition process continues indefinitely until the board is halted by the application program.

Through VMSLIB, the application program creates four 2096-word buffers in the host. Those buffers are filled by the DT1771 device driver and then released to the disk-transfer routine. After a buffer has been emptied, it is given back to the driver, which refills it, and the cycle continues. At any given time, one buffer is being filled, one is being emptied, and two are waiting to pick up the slack (see Fig. 5 again).

After being collected and transferred to disk, the data is analyzed and displayed under the



5. When the board is recording and synthesizing speech, six analog input channels acquire the speech waveforms and two analog output channels synthesize the speech patterns. To handle the data collected—about 18 Mbytes—four buffers are created in the VAX memory. While one buffer is being filled, another is transferring data to disk. Two other buffers are always on standby.

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control of segment 2 of the program. If the desired result of the analysis is an analog waveform, the board's continuous-performance d-a output can synthesize waveforms to 0.01% accuracy at update rates of 125 kHz.

The output of the four d-a channels on the DT1771 board can be played back through a stereo amplifier. Alternatively, it can be used to drive the X and Y channels of an oscilloscope. The board's display refreshing permits the use of a nonstorage oscilloscope. The programming required to control the d-a output in segment 3 resembles that of segment 1, the data-acquisition control section.□

How useful?	Circle
Immediate design application	553
Within the next year	554
Not applicable	555

The first step toward acquiring and transferring data

```
C   Device-initialization section
    CALL DTDEV (IDCB, LUN, IDEVNM)          !Ask for device specification
    CALL DTISCN (IDCB, ISTRT, NCHAN, ITRIG) !Specify the start channel, the number
C                                           of channels to be scanned, and the
C                                           triggering mode
    CALL DTCLK (ICTRLB, IDIV)               !Specify the clock divisor that will give
C                                           the sampling frequency
    CALL SPMSW (IDCB, MSCB, LULNMS, NRECS)  !Opens a file on the disk with a specified
C                                           number of records
    CALL SPMB (IDCB, IBCB, NBUFS, IBFSIZ)   !Specify the number of buffers and their size
    CALL MSRWN (IDCB)                       !Rewind the data file
    CALL MBDR (IDCB, IDTBUF, NBUFS, IBFSIZ) !Define each buffer and release it to the
C                                           device driver
C   Data-acquisition section
    CALL DTMBR (IDCB)                       !Start filling the buffers with data
C                                           from the DT1771
100 IF (IDCB(1). EQ. ISNNE) GO TO 1040      !If required number of records has been
C                                           written, exit the loop
    IF (IR .EQ. IW) GO TO 120               !If the event flag for a read
    CALL WFLOR (IR, IW)                     !operation is set, go to the segment
    CALL READEF (IR, IDS)                   !that writes the buffer.
    IF (IDS .NE. 2) GO TO 140               !If the write event flag is set, go to the
C                                           subsection that releases the buffer to
C                                           the device driver
C   Writing subsection
120 CONTINUE
    CALL DTMBWB (IDCB, IR)                  Verify that the buffer is filled
    CALL MSMBW (IDCB, IR)                   Write the buffer to disk
    IR = NXTBUF (IR, NBUFS)                 !Increment the number of buffers filled
    GO TO 100
C   Releasing subsection
140 CONTINUE
    CALL MSMBWB (IDCB, IW)                  !Verify that the buffer has been emptied
    CALL DTMBRB (IDCB, IW)                  !Release the buffer to be filled
    IW = NXTBUF (IW, NBUFS)                 !Increment the number of buffers emptied
    GO TO 100
1040 END
```

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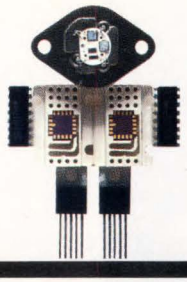

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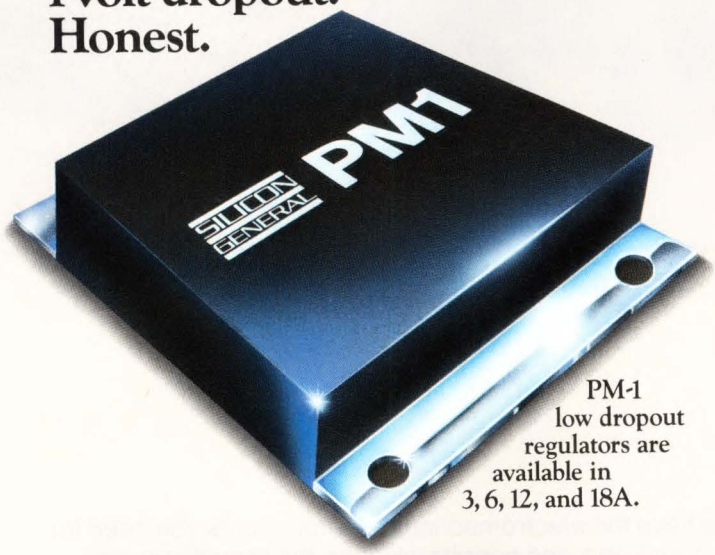

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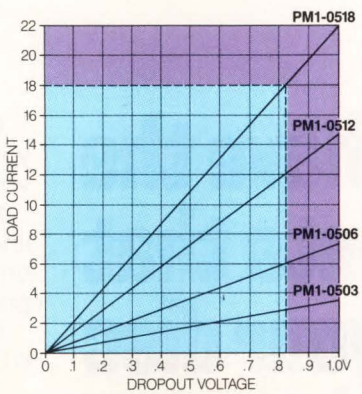

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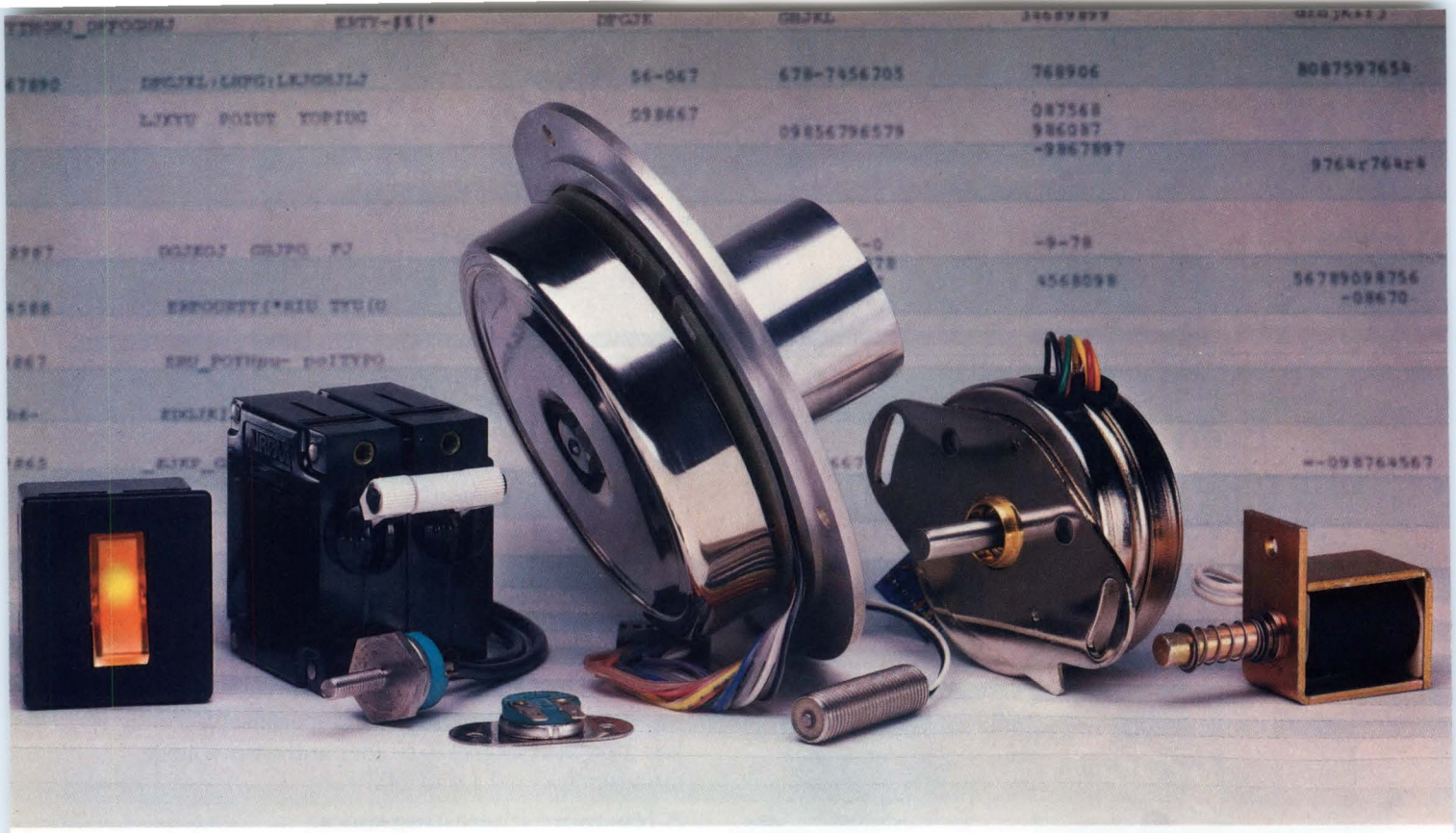

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CIRCLE 111

Clocked v-f converter tightens accuracy and raises stability

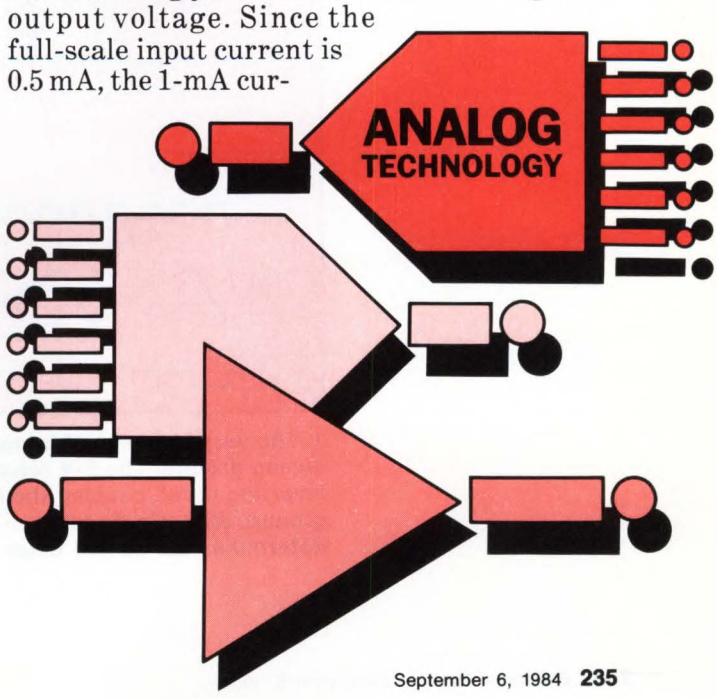
Replacing sensitive external components with a clock input, a voltage-to-frequency converter experiences less gain drift over temperature.

When very high speed is not critical, voltage-to-frequency converters make efficient and accurate analog-to-digital converters, largely because of their integrating characteristics, low nonlinearity, inherent monotonicity, and serial output. Present monolithic versions, though, require precision external capacitors and resistors, which make their gain vulnerable to temperature change.

A new clocked v-f converter chip circumvents that vulnerability with a technique previously implemented only with discrete components. A clock input controls the device's output frequency, an approach that not only produces an initial accuracy of 0.5% with an excellent temperature stability of ±20 ppm/°C but also simplifies system design, since fewer external parts are required.

The clocked, or synchronous, device is a different breed of v-f converter, though it employs the conventional and well-proven technique of charge balancing. An input voltage connected to the internal input register, R_{in}, creates a current, I_{in}, that charges the external integrating capacitor, C_1 (Fig. 1). The integrator then produces a linear voltage ramp with a negative slope as its output. When the ramp crosses the comparator's input threshold, the falling edge of the clock pulse enables the clocked logic.

The next rising clock edge initiates both an output pulse and an integrator reset period. In more detail, it causes the open-collector output transistor to saturate, producing an active-low output pulse. At the same time, current I_1 switches from the output of the integrator to the summing junction to reset the integrator output voltage. Since the full-scale input current is 0.5 mA, the 1-mA cur-



T. Anderson and **B. Trump,** Burr-Brown Corp.

Tom Anderson joined Burr-Brown in Tucson, Ariz., in 1977 and is currently a design engineer of analog products. He holds a BSEE from the University of Arizona.

Bruce Trump, who holds an Iowa State University BSEE, is a product manager at Burr-Brown, which he joined in 1979. He holds two patents in consumer electronic equipment, and he and Anderson have another patent pending.

Analog Technology: V-f converter chip

rent pulled from the summing junction always reverses the direction of the integrator ramp.

The next positive clock edge ends the reset period, switching current I_1 back to the output of the integrator and thus maintaining a constant current load at the integrator output. The integrator reset period thus lasts one complete cycle of the clock input. At this point, the integrator output voltage resumes its negative slope and ramps downward through the comparator threshold. Once the threshold is reached, the next falling and rising clock sequence initiates another output pulse and another integrator reset period.

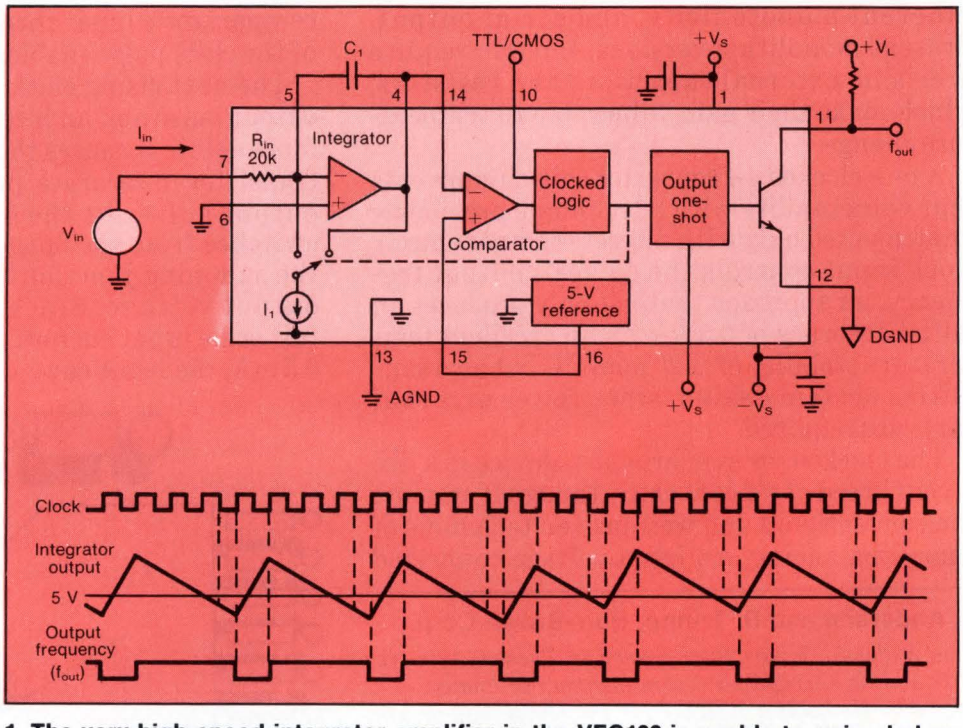
If V_{in} is greater than 10 V, the output frequency remains at half the clock frequency. Although such an overrange input frees the integrator output to trip the comparator continuously, the converter's internal logic allows output pulses to occur only on alternate clock cycles. That character is useful in system design, where the most positive valid input voltage can be scaled to less than 10 V and a frequency output of $F_{clock}/2$ used as an input overrange indication.

The value of integrating capacitor C_1 depends on the full-scale operating frequency required. Essentially, C_1 must become larger as the full-scale frequency falls; otherwise the integrating amplifier will saturate.

The capacitor's value affects the amplitude but not the frequency of the integrator waveform; thus a wide range of values (10:1) can be chosen for a given application. Accurate integration does, however, require good dielectric absorption, which is a measure of the capacitor's ability to retrace a given q/V slope regardless of that slope's polarity. Polycarbonate, polystyrene, and Teflon make good dielectrics for the integrating capacitor.

Clock frequency sets full-scale frequency

At full scale, the difference current in the capacitor ($I_{in} - I_1$) during the reset period is equal to the full-scale input current but flows in the opposite direction. As a result, the ramp-up



1. The very high-speed integrator amplifier in the VFC100 is unable to swing below analog ground. The 5-V reference voltage is used to offset the comparator's noninverting input, causing the integrator waveform to reach a plateau 5 V above ground. With pin 9 tied to $+V_S$, the output one-shot is disabled and the clock logic determines the output pulse width.

and ramp-down times for the integrator are each equal to one clock period, and the output frequency is half the clock frequency. Thus if V_{in} falls between 0 and 10 V, the transfer function for the clocked v-f converter is:

$$F_{out} = (V_{in}/20\ V) \cdot F_{clock}$$

In contrast, the transfer function for the standard charge-balancing converter is:

$$F_{out} = V_{in}/(V_{ref} \cdot R_{in} \cdot C_T)$$

where C_T is a one-shot timing capacitor that determines the integrator reset period. Both C_T and R_{in} must have a low temperature coefficient to minimize the gain error and drift they introduce into standard v-f converters. Since the initial gain accuracy of these converters is typically specified to within only 5% to 10% —even with so-called ideal external components—each circuit must be individually calibrated so that the gain error and the tolerance of actual external components can be taken into account.

Maintaining a low temperature coefficient on an input resistor with a wide adjustment range is a challenge. Because the total gain drift of the system is the sum of the individual components' temperature coefficients, low-drift, low-cost systems have been difficult to build.

The clocked v-f converter uses a precision

A look inside the VFC100

Integrated circuit technology has achieved many impressive feats but a resistor with zero temperature drift is not among them. Accurate resistor matching, however, is a strong point of IC technology and has been used extensively in the VFC100 voltage-to-frequency converter chip to cancel the effects of temperature drift of many internal circuit elements.

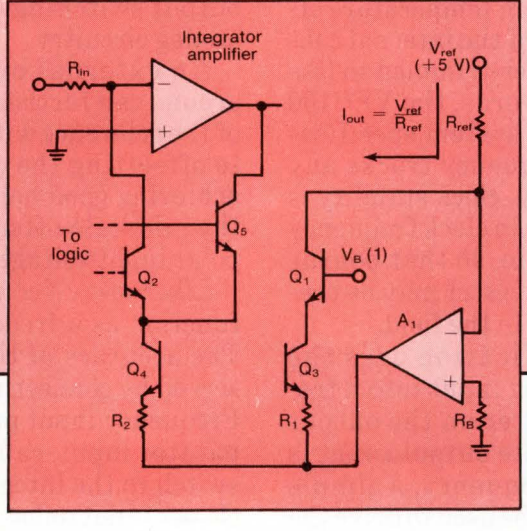
The device's input resistor, R_{in}, has excellent initial accuracy. However, only if its temperature coefficient is canceled do its advantages remain intact (see the figure).

Amplifier A_1 together with a current mirror (Q_1 through Q_4), derives the integrator's reset current, I_1, from the 5-V reference. With the noninverting input of A_1 at ground, the summing junction is also at ground potential (the amplifier's offset is laser-trimmed). Thus when R_{ref} is connected between V_{ref} and the summing junction, current I_{ref} flows in the resistor and the feedback path. Resistor R_B is laser-trimmed to cancel the offset voltage created by the amplifier's input bias current flowing in R_{ref}.

Feedback current comes from Q_1 and Q_3. Q_1 has a bias voltage, $V_B(1)$, connected to its base, and A_1 drives the voltage on R_1 so that Q_1's collector current is equal to I_{ref}. Q_3 and Q_4 have the same base bias voltage, and Q_4 has four times the emitter area of Q_3. R_1 is exactly four times the value of R_2, so Q_4 has a collector current exactly four times that of Q_3.

Q_2 and Q_5 are the switching transistors that steer I_1 to either the summing junction of the integrator amplifier or its output. The voltages on its base control the switching, and these voltages are centered around $V_B(1)$, the base bias for Q_1. This causes Q_3 and Q_4 to have the same collector-base voltage for the best possible match. Q_1 also compensates for the base current error of Q_2 and Q_5.

The result is that I_1 has the same temperature coefficient as R_{ref} (plus the smaller temperature coefficient of V_{ref}). Since the temperature coefficient of the v-f converter's input resistor is matched to that of R_{ref}, the converter's input current also has the temperature coefficient of R_{ref}. With the converter input and reset currents having the same temperature coefficient, their effects cancel and the drive of V_{ref} (laser-trimmed to 20 ppm/°C) controls temperature effects.



thin-film resistor as R_{in} to set the 10-V full-scale sensitivity. That resistor's temperature coefficient tracks other internal circuitry for excellent temperature stability (see "A Look Inside the VFC100," p. 237). Besides eliminating an external component, the arrangement allows the initial gain error to be laser-trimmed to 0.5%; thus, in most applications, the user need not calibrate gain. Of course, the user may adjust that 0.5% gain error to zero—now only a minimal adjustment—rendering the effect of temperature drift of any external trim components negligible. Since the clock frequency controls the integrator's reset period, no precision timing capacitor adds expense and error to the system.

Counting the output

Output pulses can occur only on the positive edge of a clock pulse, locking the instantaneous output frequency to a subharmonic of the clock frequency. The input voltage is represented by the ratio of the converter's output pulses (N) to the clock pulses (M), or $V_{in} = (N/M) \cdot 20$ V. To convert to a numerical value, simply count the output pulses. The key is to use a counter gate period determined by the same clock frequency. The duration of the gate (that is, its number of clock cycles) then determines the available resolution. For example, counting for 4000 clock cycles gives a measurement resolution of 1 part in 2000 since the counting period could contain no pulses or as many as 2000 converter pulses.

Since no external components affect the transfer function, total system temperature effects are limited to the drift of the internal converter circuitry, which is laser-trimmed to less than 20 ppm/°C. In other words, the VFC100 specifications are complete system specifications. Since the output frequency tracks any variations in clock frequency, clock stability is not critical. Small variations in clock frequency do not change the N/M ratio, so that boards built with the clocked v-f converter may be precalibrated and interchanged in the field.

A common system application uses the VFC100 to convert an analog input into a frequency with a simple counter on the output (Fig. 2). Because the ultimate output count is insensitive to the clock frequency, a simple RC-controlled oscillator can be used to drive the converter's clock input and to generate the counter gate period. An increase in clock frequency, for instance, would be accompanied by a proportional increase in the v-f converter's output frequency. Since the counter gate period derives from the same clock, it would be correspondingly shorter, thus producing the same number, N, of accumulated converter counts.

In actual practice, a system might contain a clock that is, in fact, quite accurate. But the insensitivity to the actual frequency allows a single input circuit to function in a variety of system designs without recalibration. An accurate clock is not without benefits, however. The v-f converter has a fully integrating input, and the integration period is equal to the counting gate period. For best noise rejection, it is best to integrate for multiples of the period of the most likely interfering signal. Therefore, multiples of 1/60 second and 1/50 second are usually chosen to reject ac-line frequency noise.

A voltage reference, too

In addition to bringing clocked operation and pretrimmed gain to the party, the v-f converter offers an excellent on-chip 5-V reference to the designer. This bandgap reference is laser-trimmed to within 0.5% and a 20-ppm/°C temperature drift. The high-gain, high-bandwidth amplifier in the voltage reference provides low output impedance (1 Ω) and the excellent transient rejection required in a digital signal environment. Separate analog and digital grounds aid in maintaining accuracy by isolating digital output switching currents from the sensitive analog circuitry.

An external bypass capacitor to analog ground can further enhance the noise rejection of the reference with external loads. In addition to offsetting the comparator input and thus achieving good noise rejection, it can establish the midscale offset required for handling bipolar input voltages.

Like most v-f converters, the VFC100 can also function as a frequency-to-voltage converter. The accuracy of the transfer function is preserved by connecting R_{in} as a feedback resistor. Frequency input pulses are applied to the comparator input, causing reference current I_1 to switch to the integrator input for one clock cycle per input pulse. The current pulses are aver-

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Analog Technology: V-f converter chip

aged by C_1 to create a voltage output, $V_{out} = 20\ V \cdot f_{in}/f_{clock}$.

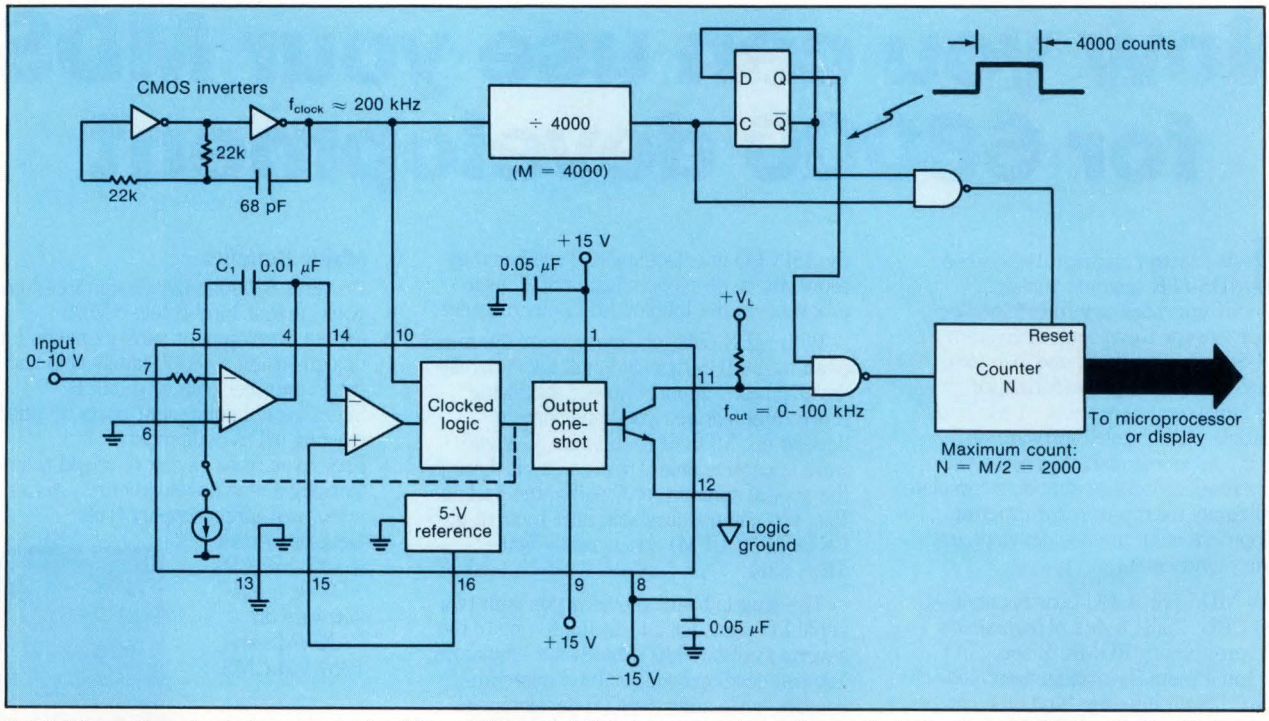
The design of the internal logic causes the input frequency information to be loaded on the falling edge of the clock signal—a convenience when interfacing a v-f converter with an f-v converter. Since both comparator inputs are free, the digital input can be directly coupled, avoiding the cumbersome capacitive coupling circuitry required with previous designs. The analog voltage output (that is, the integrator amplifier output) can easily drive a 10,000-pF load, so that long coaxial lines can be driven directly.

An isolated system

The chip can serve equally well as a voltage-to-frequency and as a frequency-to-voltage converter, say, in moving an analog signal across an optically isolated barrier (Fig. 3). That technique is useful not only for ensuring safety in the presence of high voltages but also for improving noise rejection in industrial environments. A common clock frequency again adds significantly to accuracy. A clock on the output side is optically coupled to the v-f converter, giving the two converters the same transfer function and also minimizing errors.

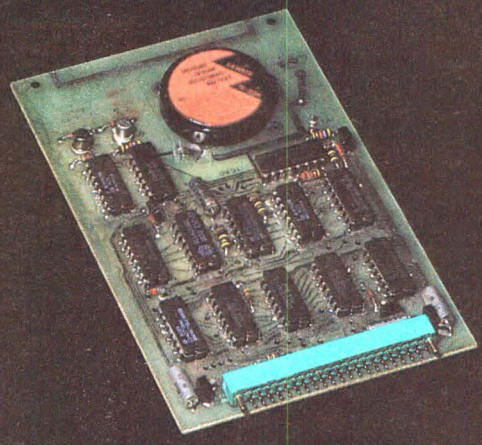
The output one-shot circuit facilitates optical coupling of the frequency data. To accommodate the slow turn-off time of optical couplers, the active-low output pulse (normally lasting one clock cycle) can be shortened by connecting C_2 to pin 9. The one-shot, which is normally disabled when pin 9 connects to a positive voltage, enables C_2 to vary the duration of an output pulse from as short as 200 ns to as long as one clock cycle. The timing diagram (see Fig. 3 again) reveals how the accumulated delay of both optical couplers might create too long an input pulse to the chip working as an f-v converter, VFC_2: an input pulse remaining low during two falling clock edges (dotted lines) would be interpreted as two input pulses.

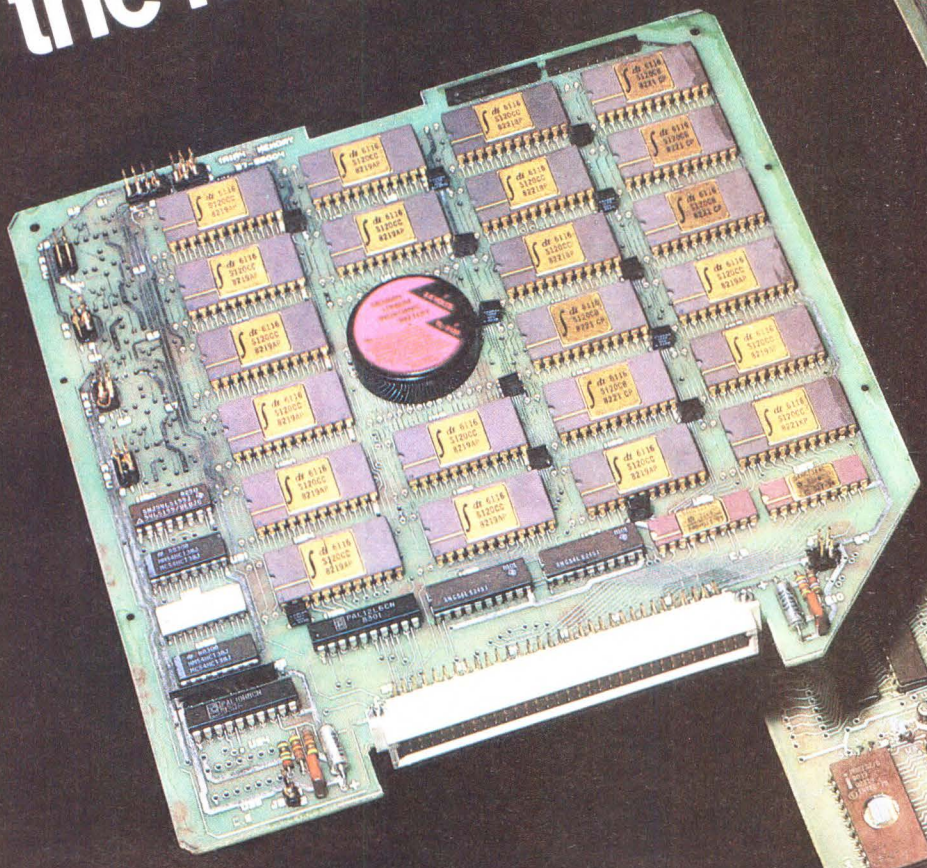
The ripple voltage existing in the output of the f-v converter section is more effectively filtered if a minimum operating frequency is established. Since the basic operating mode of the

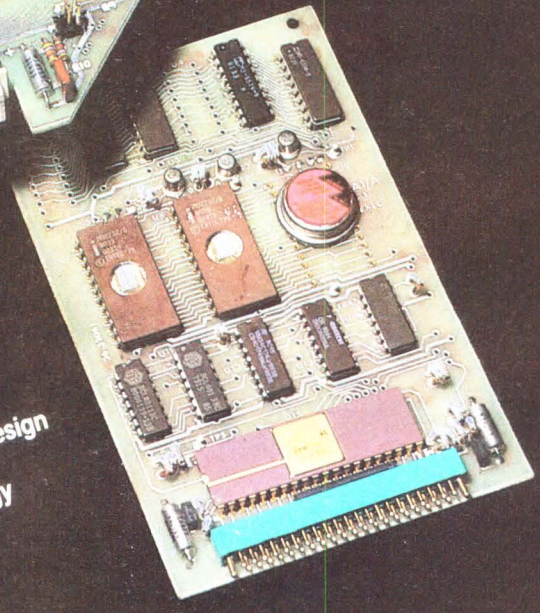


2. Dividing the clock frequency by M = 4000 establishes a counter gate period. An input of 0 to 10 V will then produce 0 to 2000 counts in the N counter. The count will stay the same even if the clock frequency drifts.

Here's to the memory







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"VISIT BOOTH #304 AT MIDCON"

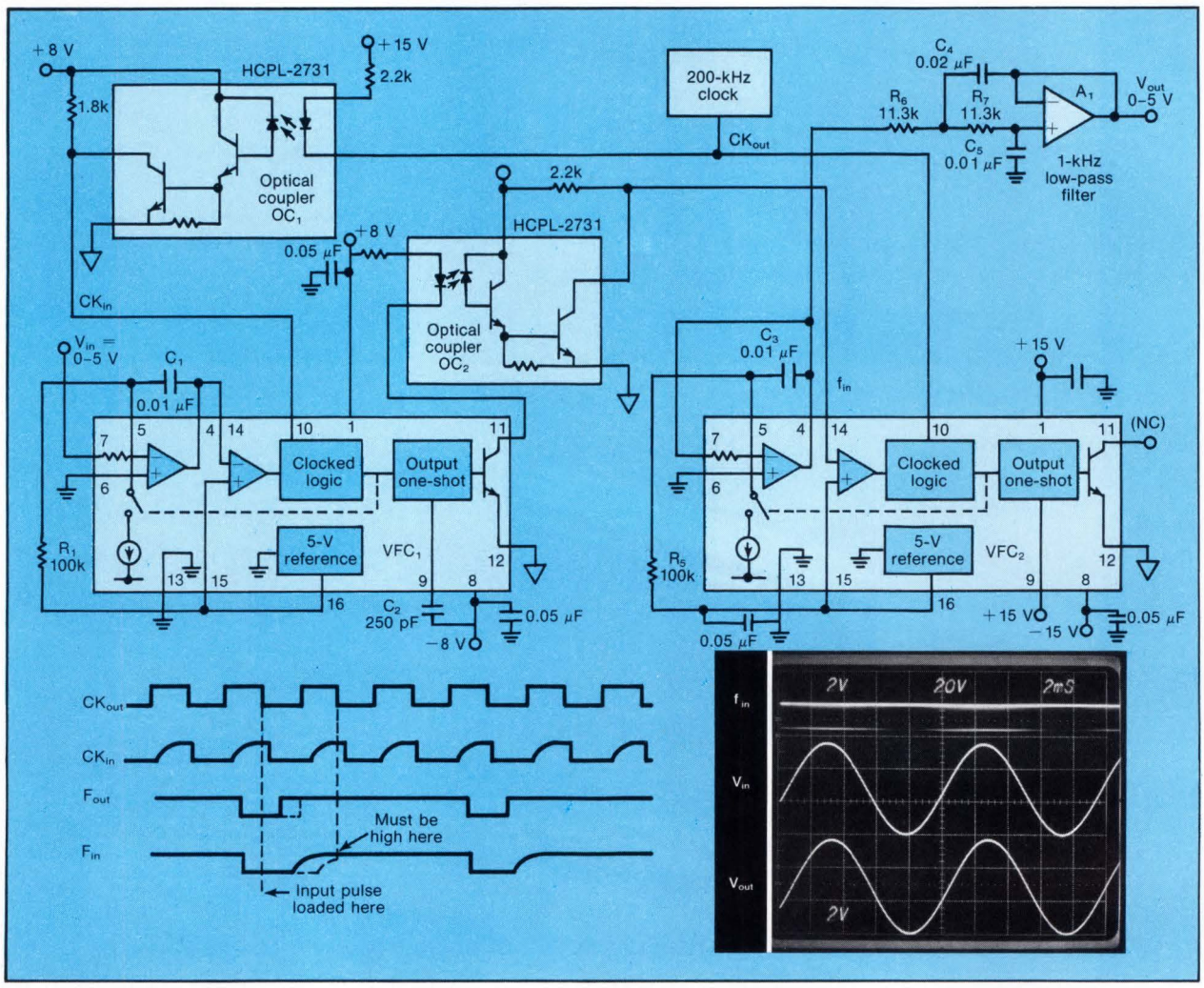
Analog Technology: V-f converter chip

v-f converter (see Figs. 1 and 2 again) produces zero output frequency for a 0-V input, a small circuit change is required. R_1 is simply connected to the reference, adding a constant 50-μA offset current to the input current. An input of 0 V now produces a 10-kHz output.

Given the same offsetting value, R_5 subtracts a matching offset in the frequency's conversion back into a voltage. A second-order 10-kHz low-pass filter, A_1, further reduces the ripple voltage at the integrator's output. Although the same results could be obtained by using a larger integrator capacitor, C_3, the low-pass filter yields a more favorable tradeoff between output ripple and settling time.

More resolution

Intrinsic to the synchronized v-f converter is an instantaneous output frequency that is quantized. Since output pulses must always align with the nearest clock pulses, they appear to have a phase jitter, an effect that can be min-



3. An offset of 10 kHz introduced by R_1 helps achieve a ripple-free output voltage (see the schematic). The offset is removed with R_5 in the frequency-to-voltage section, VFC_2. Using the internal one-shot in the output section and controlling it with C_2 shortens the output pulse (lower left). This ensures that f_{IN} rises before the next falling edge, despite optical coupler delay. The clean output possible after low-pass filtering (shown at lower right) illustrates the performance of the overall system.

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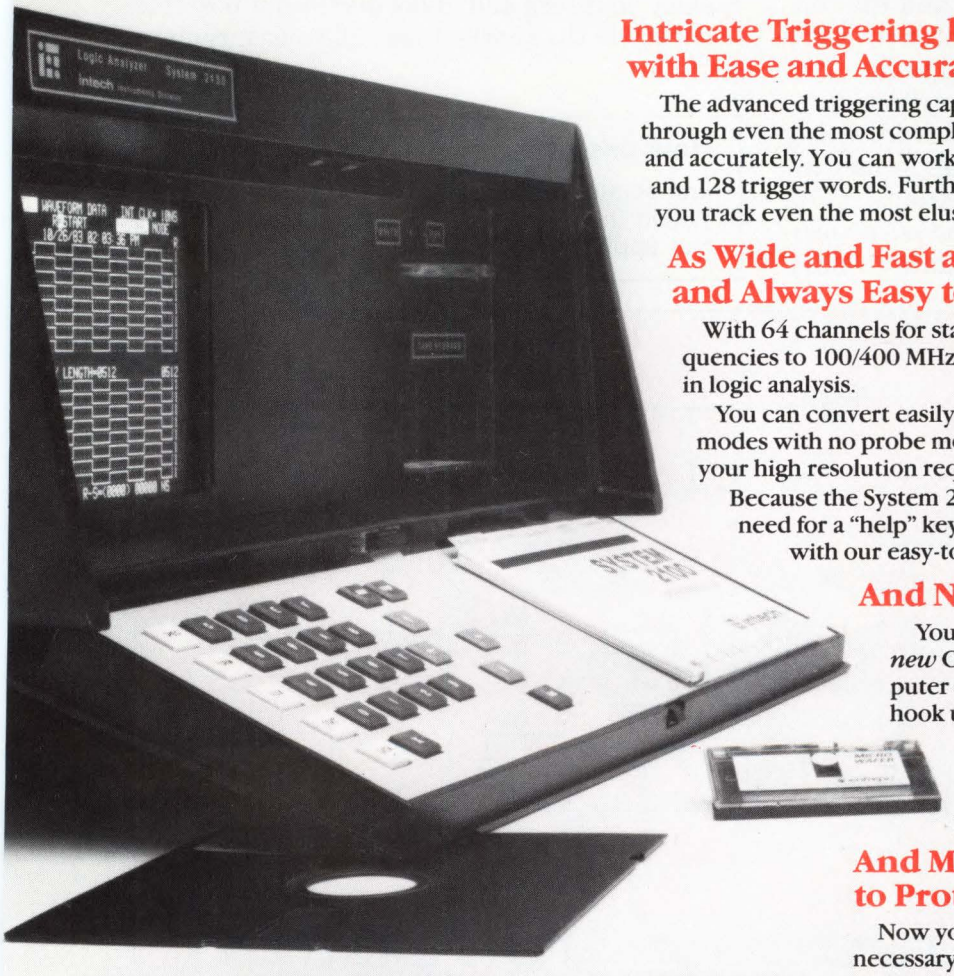

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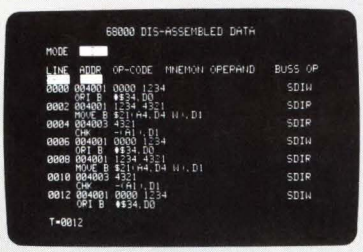

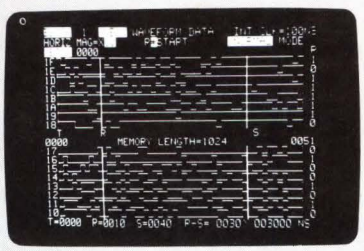

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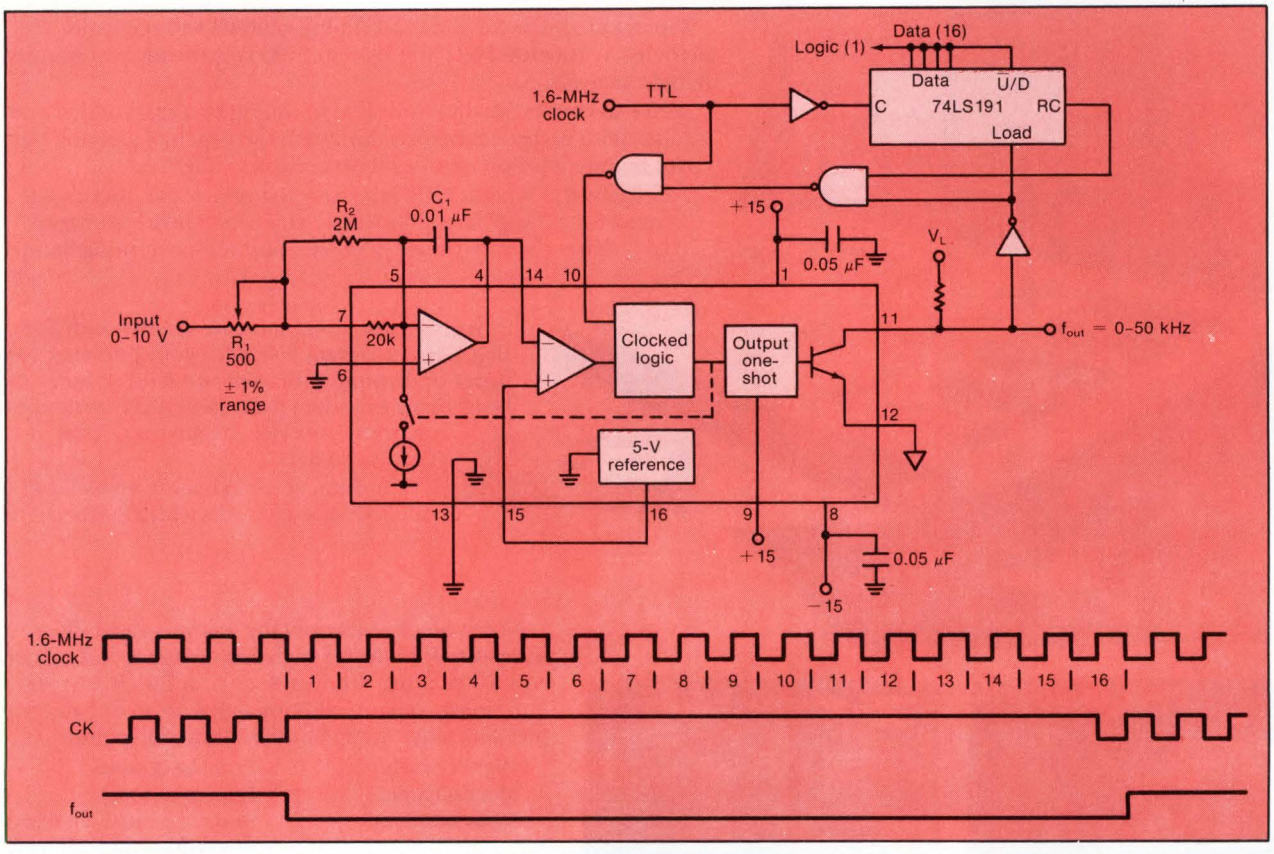
Analog Technology: V-f converter chip

imized with a high-speed clock, that makes clock edges available more frequently. Normally that high-speed clock sould be accompanied by a correspondingly high full-scale frequency, but there is an alternative approach (Fig. 4). Here, a 1.6-MHz clock affords excellent resolution in output pulse timing; but the full-scale frequency is set at a much lower 50 kHz by using a counter triggered by the v-f converter's output pulse.

The converter's 1.6-MHz clock input held high when the comparator trips and the converter's output goes low. The counter circuitry delays the next rising edge applied to the clock input for 16 clock cycles. Since the critical integrator reset period is determined from rising edge to rising edge at the converter's clock input, the effective clock frequency is $f_{clock}/16$. Other full-scale frequencies can be set by programming the appropriate load data (binary 2 to 16) on the counter.

With output pulses now able to align with 16 times the resolution, the output has far lower phase jitter. Clock frequencies of up to 3 MHz, in conjuntion with larger counters, can achieve a wide range of full-scale frequencies and resolutions. The output now lends itself to ratiometric counting techniques, where the period of many v-f converter cycles is measured and the frequency computed. This frequency measurement technique is used in many laboratory frequency counters and gives maximum possible accuracy in the shortest possible measurement periods. □

How useful?	Circle
Immediate design application	556
Within the next year	557
Not applicable	558



4. Conventional logic functions can supply a low-frequency output synchronized to a much higher-frequency clock. The reduced phase jitter resulting from this high-speed clocking means that 16 times more resolution is available in the output signal's period. Conversion speed can now be improved by using ratiometric counting techniques.

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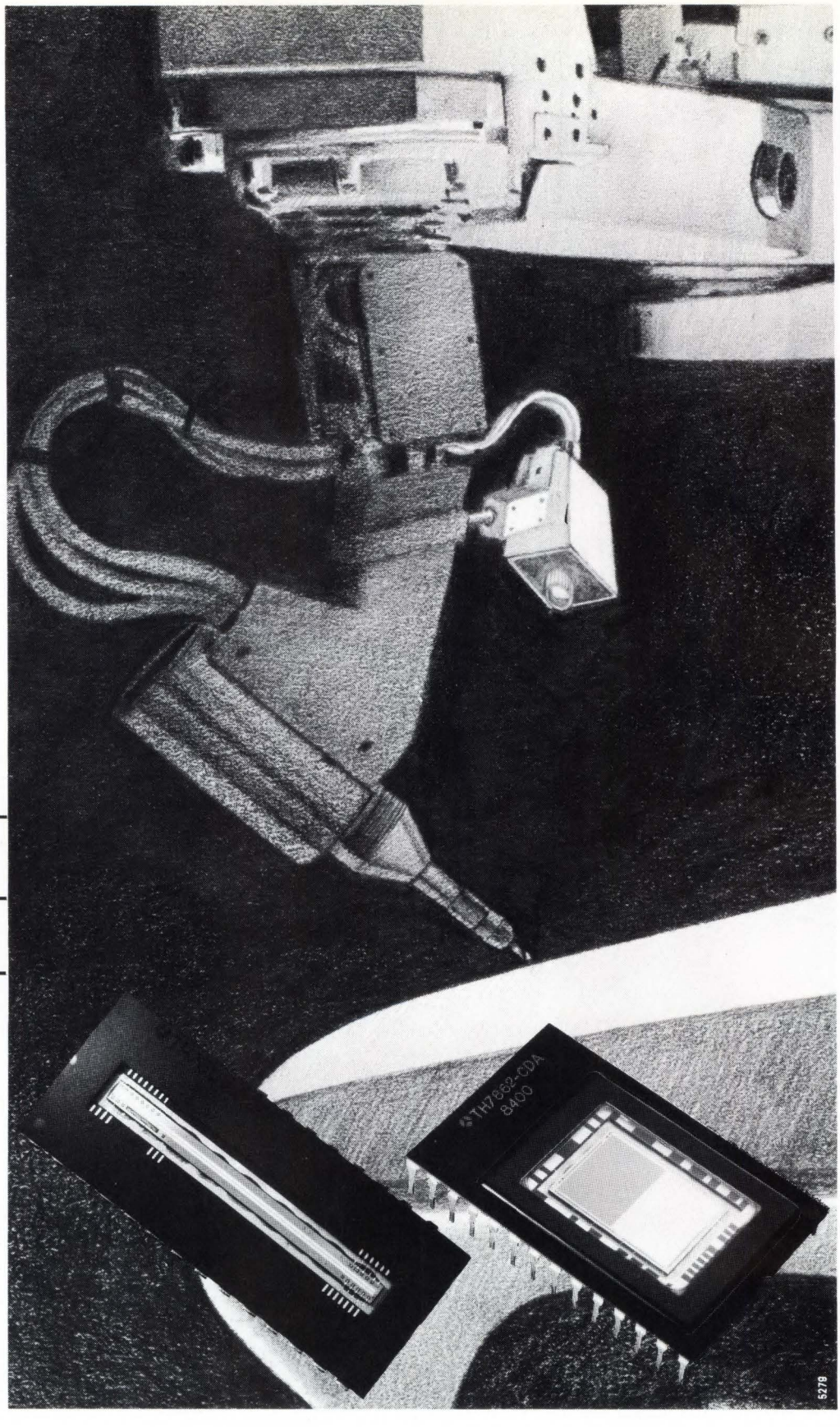

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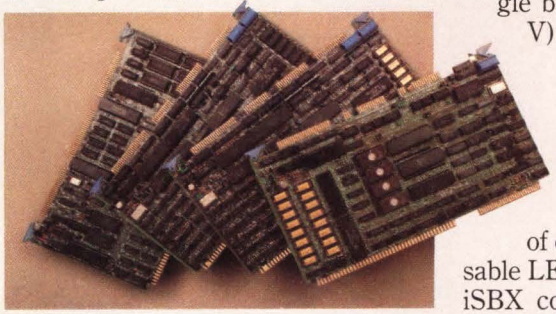

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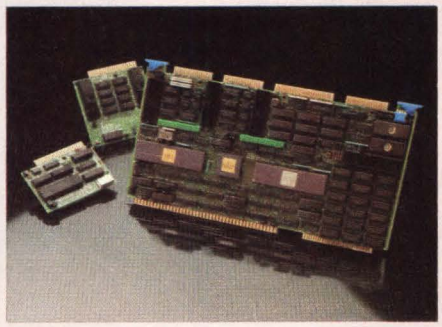

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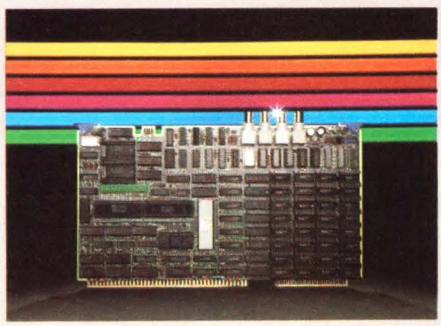

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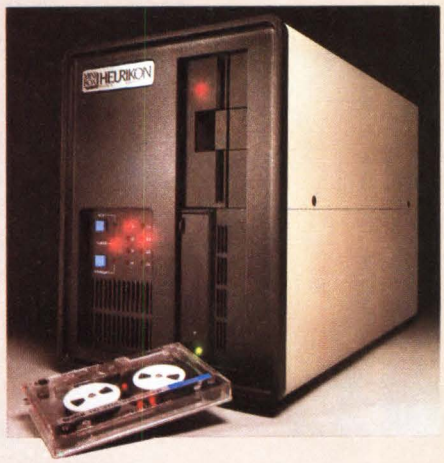

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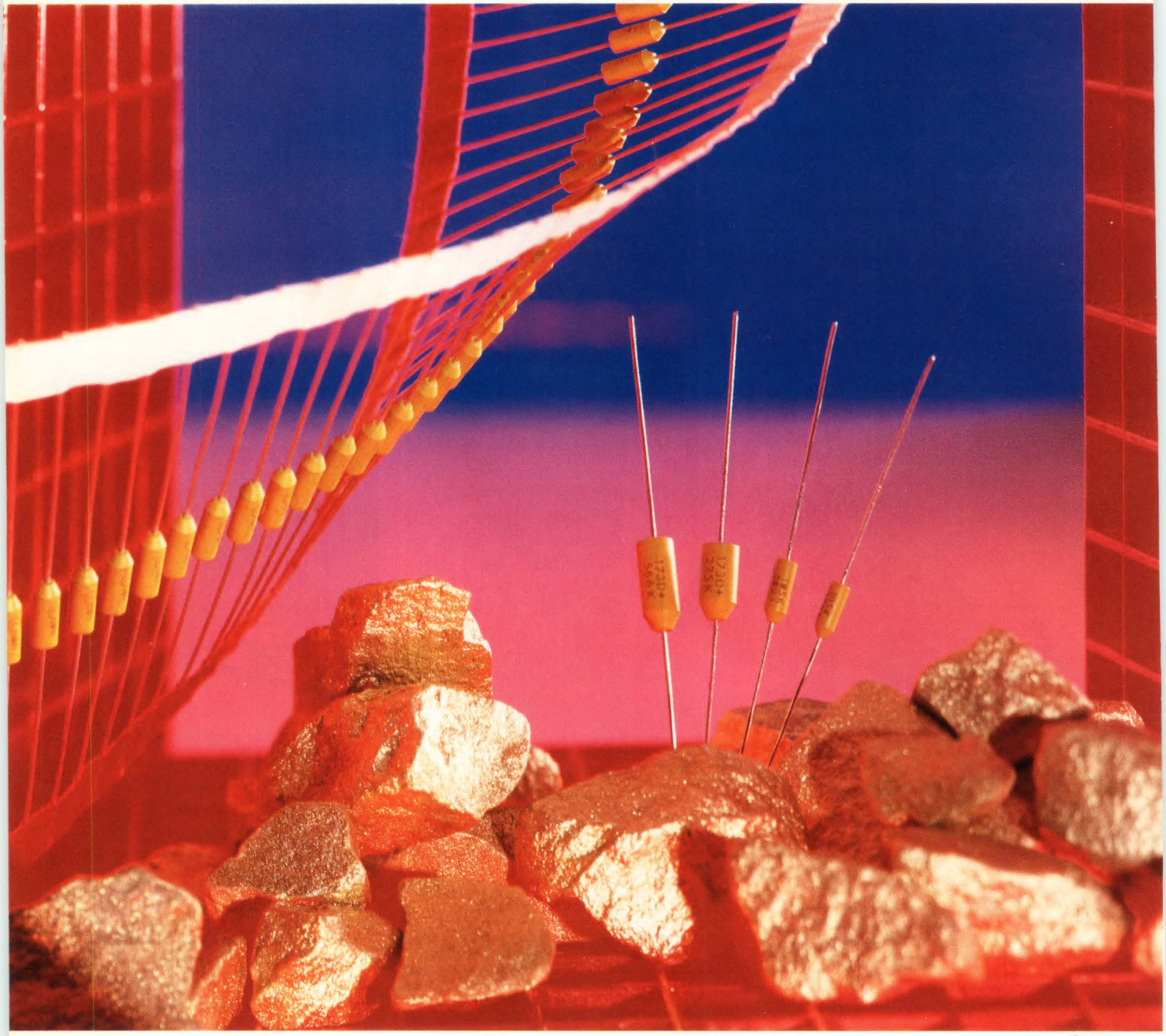

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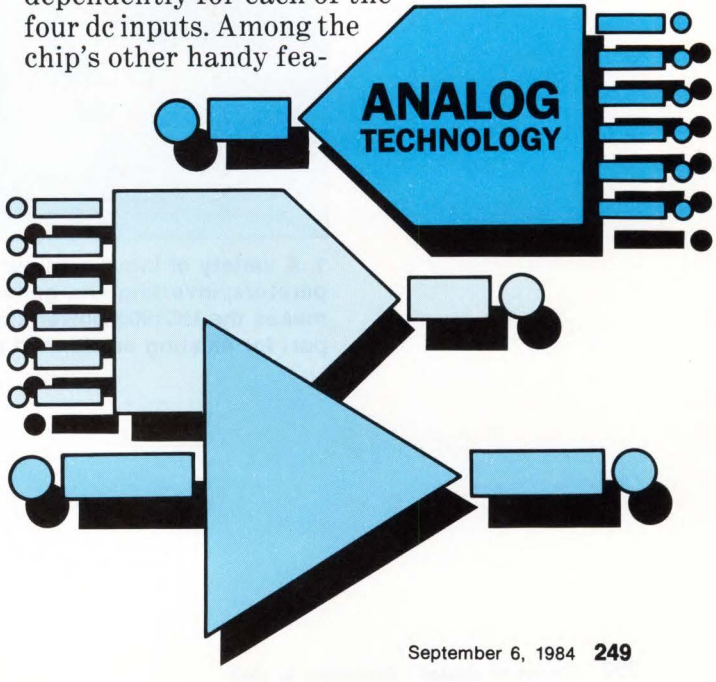
Even simple power supplies had required a host of components for the supervisory function, including operational amplifiers, comparators, precision resistors, and a precise reference. Multiplied by the number of outputs—up to four in a typical supply for a microprocessor system—supervision grew large and costly.

Now, a single integrated circuit, the UC1903, not only monitors four dc outputs over a very wide range of programmable tolerances, but also keeps tabs on the incoming ac line (Fig. 1). Under- and over-voltage faults, with limits set by the user, are reported by means of two open-collector outputs; a third output responds to any fault, making its off state a "Power OK" indicator.

To suit the majority of standard and custom power supplies, the chip's inputs can be configured for combinations of negative and positive voltages. One on-board op amp is dedicated to sensing negative voltages; a general-purpose op amp can be strapped to sense a second negative input, boost input voltages that are below the 2.5-V reference level, or set tolerance levels.

The reference itself is brought out to a pin for external use or to scale fault tolerance levels independently for each of the four dc inputs. Among the chip's other handy fea-



Rich Valley, Unitrode Integrated Circuits Corp.

Rich Valley designs power management ICs for Unitrode Integrated Circuits in Lexington, Mass. As senior design engineer, he plans such power circuit support chips as pulse-width modulators, regulators, and supervisory circuits. Before joining Unitrode, Valley worked as a research engineer for Motorola Communications and Electronics. He holds a BSEE from the University of Michigan and an MEE from the University of Texas at Arlington.

Analog Technology: Monitor chip

tures is a start-up circuit, called a starting latch, that prevents false trouble indication before the power supply has stabilized. An input-supply under-voltage sense circuit also prevents an erroneous fault indication under low-supply conditions.

The operating points of the four dc inputs can be set with just a handful of resistors that scale the inputs to 2.5 V. The scaled supply levels are compared with precisely defined upper- and lower-voltage thresholds at the sense inputs.

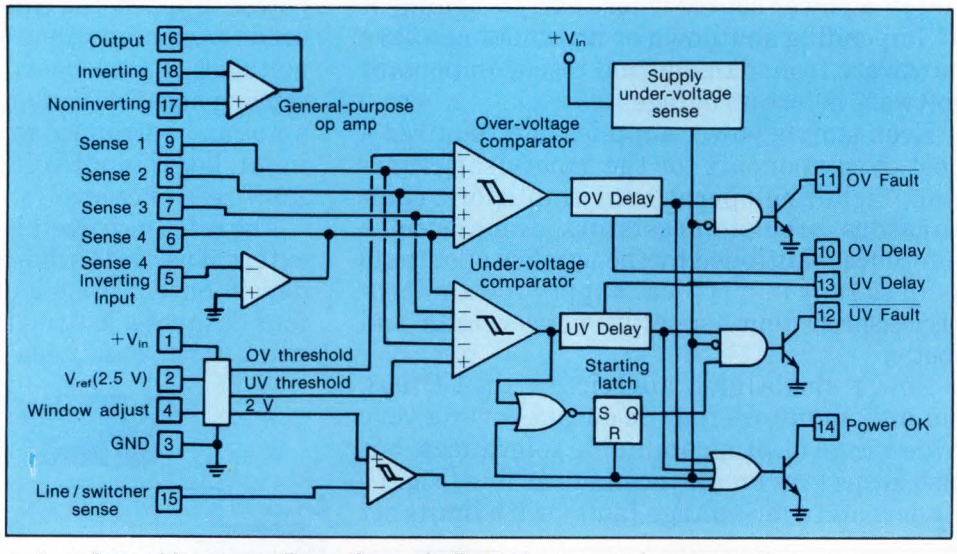
The user selects the proper tolerance using the Window Adjust pin, which simultaneously adjusts all four sense inputs from ±5% to ±25%. The fifth input, for the incoming ac line, is monitored for an under-voltage condition through comparision with a fixed 2-V level. A failure caught at the ac line gives the system its best chance for an orderly shutdown before power is completely lost, the rescue time depending on the size of the power supply's filter capacitors.

The chip's outputs are open-collector npn transistors that can sink in excess of 30 mA, and therefore are easily interfaced with many different types of alarm or emergency systems. Both the over- and under-voltage outputs are active low only when a fault occurs at any of the four sense inputs. But to accommodate the problems of the real world—say, transients and other types of noise—delays can be programmed into the detection paths.

A system status indicator

The Power OK output differs from the others, since it indicates a fault condition anywhere in the supply, be it the input or output. The active-low state signifies over- and under-voltage faults at the four sense inputs, a low-input supply line at the $+V_{in}$ terminal of the IC, or a low condition at the line sense input. Thus, the off state of that output (or a high state if an external pull-up resistor is used) indicates that no problem exists.

The value of separate fault indicators for the dc supply outputs and the incoming ac line are



1. A variety of input configurations, dedicated over- and under-voltage comparators, inverting and general-purpose op amps, and open-collector outputs makes the UC1903 power supply and line monitor a flexible add-on or integrated part for existing or planned power supplies.

obvious. However, in many cases, a supervisory system will take the same action regardless of the fault's cause. For those cases, the Power OK output alone suffices to initiate action. If line problems call for a unique response, however, the three fault outputs can be logically combined externally to distinguish that condition from other faults.

A typical application demonstrates the simplicity of the controller's design (Fig. 2). There, four power-supply outputs ±5, +12, and +15 V—must be monitored to ensure that they stay within ±10% of their nominal values. The outboard hardware for the circuit consists mostly of the resistive dividers used to scale the nominal outputs to 2.5 V, which represents the center of the tolerance windows.

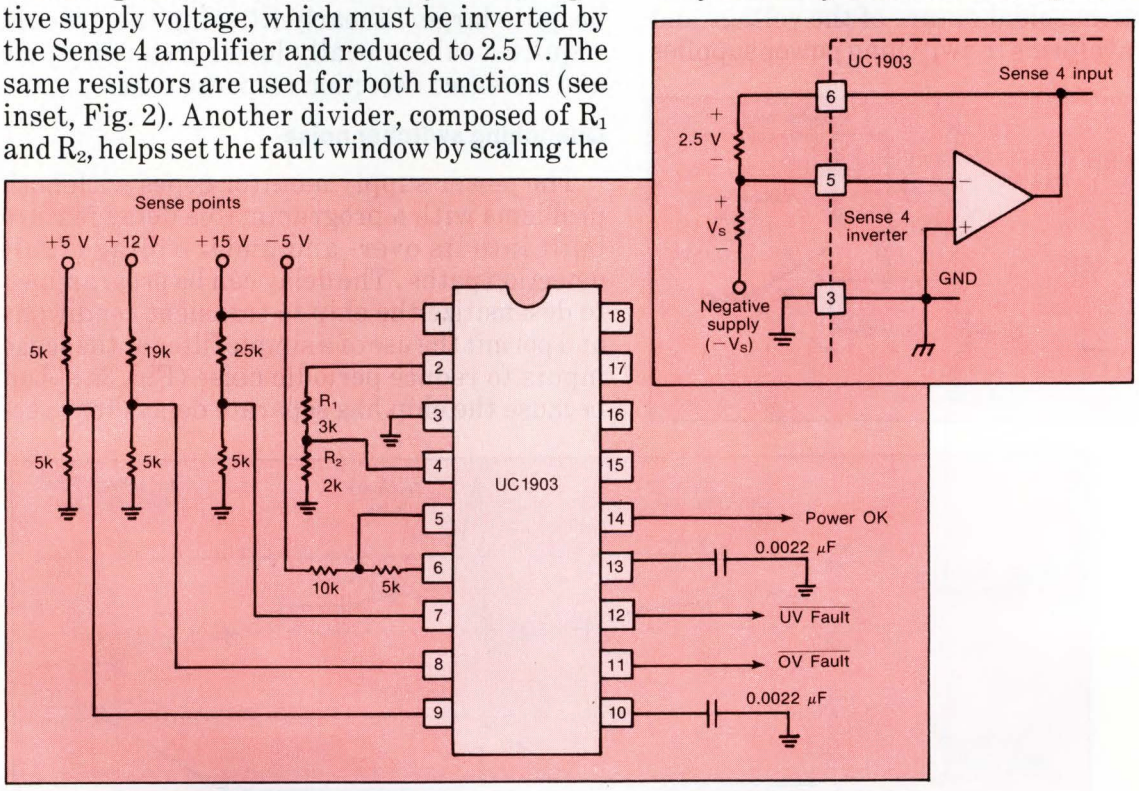
Scaling resistors do double duty for the negative supply voltage, which must be inverted by the Sense 4 amplifier and reduced to 2.5 V. The same resistors are used for both functions (see inset, Fig. 2). Another divider, composed of R_1 and R_2, helps set the fault window by scaling the 2.5-V reference at pin 2 to 1 V for the Window Adjust input at pin 4, according to the formula:

$$\text{Fault window}\,(\%) = V_S \pm (10 \times V_{ADJ})\,\%$$

where V_S is the nominal level of the voltage being monitored and V_{ADJ} is the voltage at the Window Adjust input.

If the fault window is not symmetrical, that is, the nominal supply voltage will range X% below the overvoltage point and Y% above the minimum, the divider values are selected so that $V_s(1+[(x-y)/(2\times100)]$ scales to 2.5V. In such a case, V_{ADS} would be set to (X+Y)/20 V.

Although threshold hysteresis will reduce a comparator's susceptibility to noise, too much impairs the circuit's resolution. For that reason, the power supply monitor's hysteresis is very carefully chosen to reach just the amount



2. In a simple hook-up, the chip monitors four supply levels for over- and under-voltage conditions. In addition to a built-in inverter for negative supply voltages, the chip includes a general-purpose op amp that can be configured to monitor a second negative supply (inset).

of resolution required for clean, glitch-free performance.

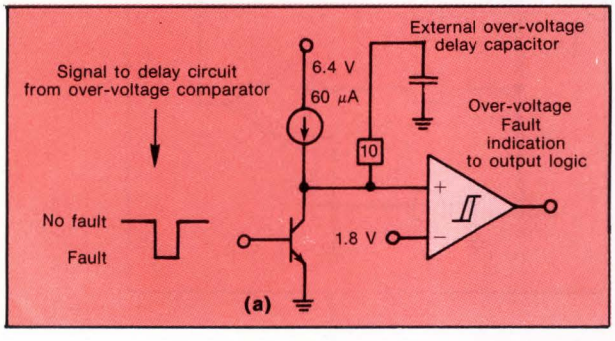
Both the over- and under-voltage comparator thresholds are set at the sense inputs of the controller for a hysteresis that is always 8% of the window magnitude. For example, ±10% fault windows have a hysteresis of 0.8%, or 20 mV at the sense inputs.

If a supply must be monitored to within ±5%, the fault window at the sense inputs would be ±125 mV. In that case, 50 mV would be too much hysteresis but 10 mV would not. On the other hand, if a supply is checked to within ±25%—that is, ±625 mV at the sense inputs—then the 50 mV of resulting hysteresis would not be too much. In fact, the increased hysteresis may be desirable, since the supply would more likely be noisy due to its poor regulation.

The nonsinusoidal nature of the voltage and current waveforms in switching power supplies causes substantial amounts of residual switching noise and ripple on the outputs. Also, the limited bandwidth of the switcher—about one half of the switching frequency—and the large output inductors used to reduce ripple combine to limit transient response. All three factors require that the monitoring circuit be able to reject periodic noise as well as normal transient excursions.

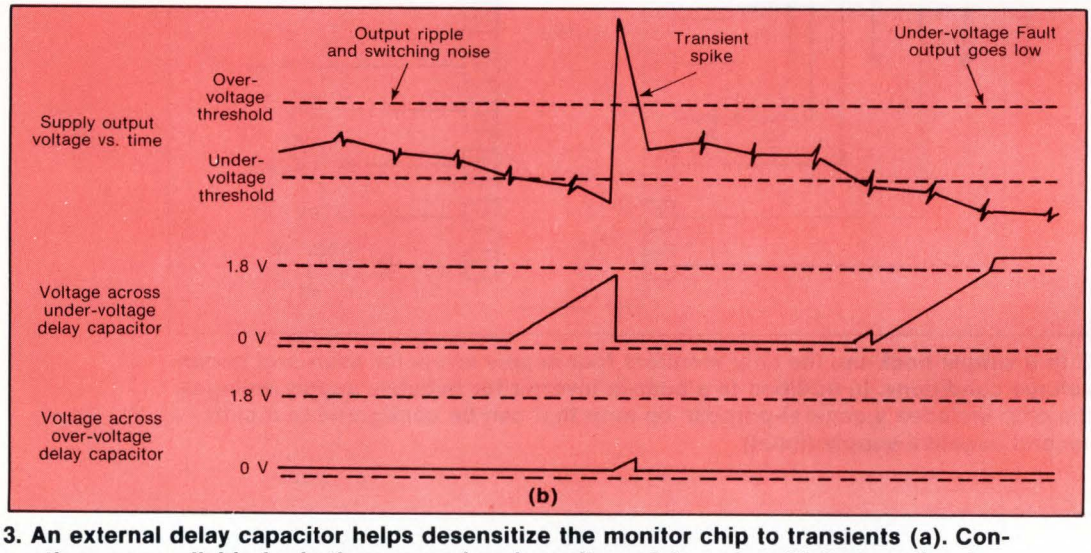
The monitoring circuit's tolerance is effectively reduced by the peak noise amplitude. Filters can be used but they can cause an undesirable delay that prevents fault detection before damage is done.

Ripple noise is the least of the problems, since its amplitude is limited. Transient spikes are not as easy to handle, since their amplitude, (energy content) is not as predictable and can be quite large. Linearly filtering them would require a substantially lower frequency pole and increased detection response time.



Quenching switcher noise

The power supply monitor copes with both problems with a programmable delay feature built into its over- and under-voltage fault detection paths. The delay can be programmed to desensitize the chip to transient conditions and permit the use of a simple filter at the sense inputs to reduce periodic noise (Fig. 3a). And because the chip has separate delays for over-



3. An external delay capacitor helps desensitize the monitor chip to transients (a). Connections are available for both over- and under-voltage delays. Sensitivity to spikes is reduced but definitive action results from a true under-voltage condition (b).

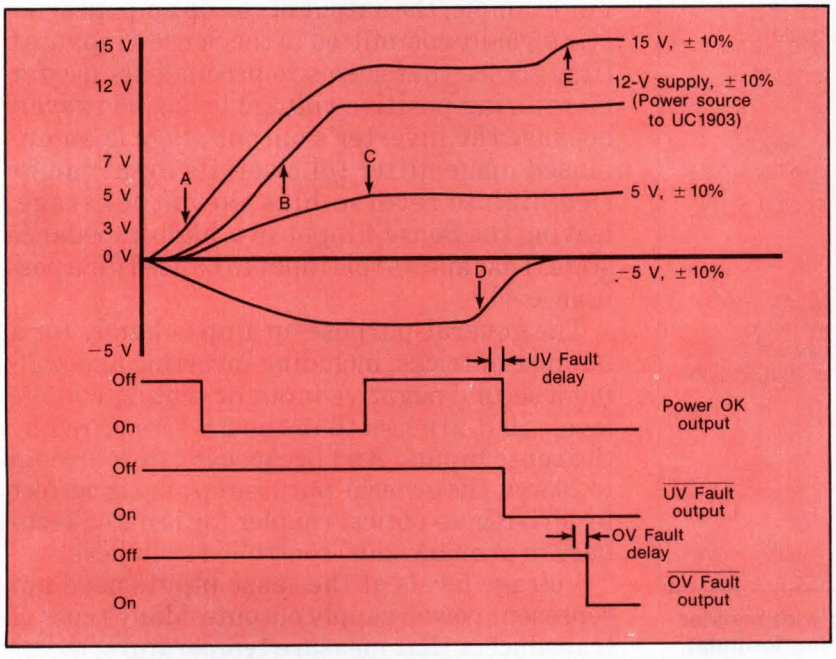
and under-voltage conditions, plus fast decay of the delay capacitor's charge (Fig. 3b), it can sidestep a drawback of combining quad fault capabilities onto a single chip. That is, if several noisy inputs are near a fault threshold simultaneously, the fault delay will not be effectively shortened.

A minimum fault delay of about 50 μs is adequate to effectively reject transient spikes in a typical switcher. The UC1903 has a nominal fault delay of 30 ms/μF of delay capacitance. Thus for a 50-μs wait, a delay capacitance of 1.7 nF is required. Accordingly, the 2.2 nF shown (see Fig. 2 again) is adequate for nominal fault delays of 66 μs.

Getting things started

A couple of irksome power supply problems can confuse a supervisory circuit at start-up. In a multiple-output supply, the various outputs do not necessarily come up to proper levels at the same rate. Indeed, in some instances the outputs are intentionally staggered. Also, if the biasing for the reference levels, or comparators, is not adequate when the chip receives power, the over-voltage trip levels may be artificially low at the sensing points. As a consequence, the monitoring circuit may sense fast-rising dc inputs as over-voltage conditions. That is an especially critical problem if hard-wired shutdown or crowbar circuits are tripped. Both problems can lead to an erroneous indication of under-voltage faults if the start-up condition is not sensed.

To cope with these problems, the input-supply under-voltage sense circuit of the UC1903 monitors the internal bias supply to all other circuits within the chip. When the input supply is not adequate to sustain proper internal bias levels, the over- and under-voltage

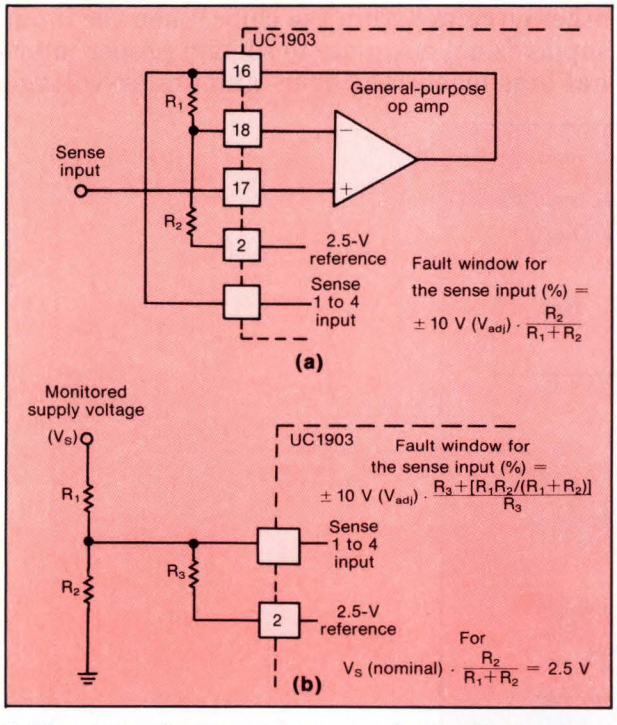


4. The starting latch and the input-supply sense circuitry ensure predictable fault response during start-up and low input-supply conditions.

fault outputs are disabled. Typically, an input supply of 7 V is required before the disabling signal from the under-voltage sense circuit is removed.

The chip's starting latch recognizes a start-up condition through the under-voltage sense signal, and is reset when a low input-supply condition occurs. The output of the latch disables the under-voltage fault output and continues to maintain that condition as long as the latch remains reset.

The end of a start-up sequence is recognized when all four sense inputs exceed the under-voltage threshold. At that point, the starting latch is set, enabling the under-voltage fault output to go low if any of the sense inputs drop below the under-voltage threshold.



5. The general-purpose op amp, along with resistor values (determined by the accompanying formula), tightens the fault window of one sense input independently of the others (a). For a wider window, one resistor must be added to the resistive divider (its value found by the formula) and connected between the sense input and the 2.5-V reference (b).

In a representative start-up sequence (Fig. 4), the supervisory chip's own power supply has reached 3 V and the Power OK output becomes active at point A. The over- and under-voltage outputs are disabled. At B, the chip's supply has exceeded 7 V, the over-voltage output is enabled, the under-voltage output remains disabled (by virtue of the starting latch), and the Power OK output remains low. The last supply has reached the under-voltage threshold at point C and the Power OK output has gone high. In addition, the under-voltage output is enabled. At point D, the −5-V supply starts to rise and the under-voltage output, after a suitable delay, goes low. An over-voltage fault in the +15-V line causes the appropriate warning at point E.

Versatility is the key

The supervisory chip's strength lies in its adaptability to a variety of monitoring chores. For example, the output of the op amp inverter is internally committed to the Sense 4 input. At first glance that seems to preclude its use for monitoring positive voltage levels. However, because the inverter's output stage is an unbiased npn emitter follower, its input can be tied high to reverse-bias the output stage, leaving the Sense 4 input in a high-impedance state. That allows this input to be used for a positive level.

The general-purpose op amp is handy for a number of tricks, including inverting and scaling a second negative input or scaling voltage levels that are less than the 2.5 V required by the sense inputs. And because it can source up to 20 mA, the general-purpose op amp is perfect for driving an optical coupler for isolated feedback in primary-side-controlled switchers.

Voltage levels at the sense inputs need not represent power-supply outputs. Many types of transducers that measure temperature, motor speed, air flow, and other variables produce current outputs that can be converted, if necessary, by the op amp to the required 2.5-V level.

The fault tolerance windows of the monitor chip, with the help of the reference output pin and the general-purpose op amp, can be individually scaled to accommodate the practical need for a variety of output tolerances within a single multioutput power supply. To narrow a win-

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dow, the hook-up must be used to amplify the output's deviation from its midrange, or nominal value (Fig. 5a). Because the middle point of the fault window at the sense inputs is always 2.5 V, the op amp can compare the divided supply voltage with 2.5 V and then boost the deviation.

Just one extra resistor is needed to widen the fault window (Fig. 5b). In that case, the deviations of an output are simply divided by tying a resistor from the 2.5-V reference to the output of the supply divider.

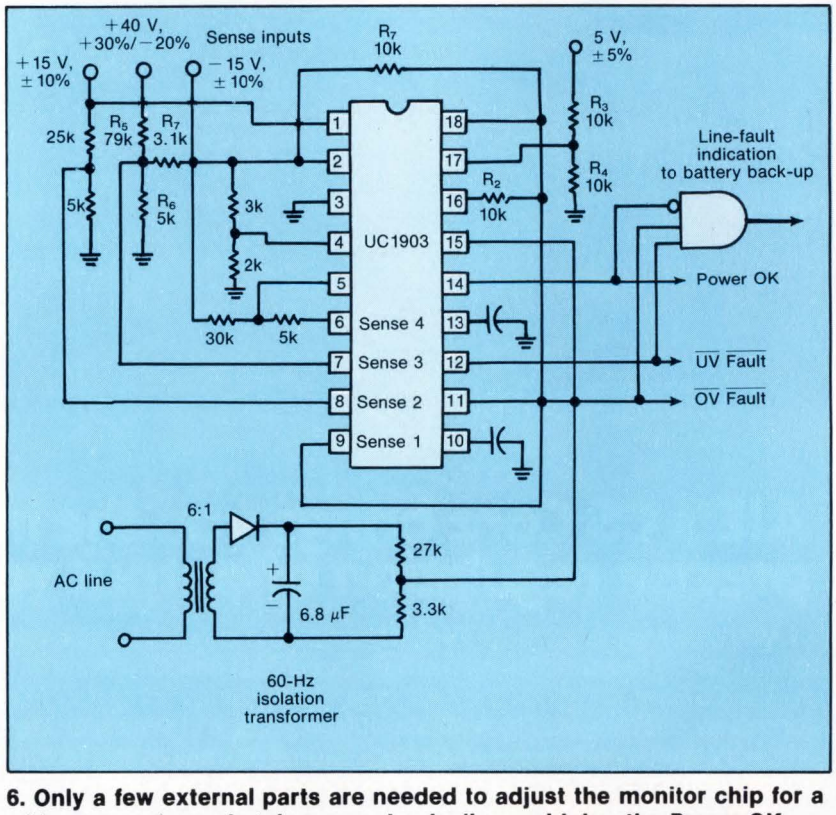
The diversity of circuit configurations possible with the supervisory chip is well illustrated by a four-supply example: 5V, ±5%, ±15 V, ±10%; and 40 V, which must not vary more than −30% or +20% (Fig. 6). In addition to the monitored supplies, the logic system attached to the power supply has a battery backup that requires an early warning of line failures.

Although the monitoring job is quite complex, the circuitry is not. The few external parts required are mostly scaling resistors. The Window Adjust voltage is set to 1 V by a divider tied to the reference. The ±10% windows for the 15-V supplies are set by simple scaling and, in the case of the negative supply, by inversion to a 2.5-V level.

The general-purpose op amp is enlisted to monitor the 5-V supply's strict tolerances. To do so, resistors R_1 and R_2 set a gain of 2 between the output of the R_3/R_4 divider and the Sense 1 input. The noninverting input of the op amp then references the sense level to 2.5 V.

To monitor a 40-V supply, the R_5/R_6 divider is centered in the middle of the operating range—42 V. The fault window is widened from ±10% to ±25% by resistor R_7, which is placed between the reference and the Sense 3 input.

To sense the line voltage, a small-signal 60-Hz transformer both steps down the line level and isolates the line from the chip. The



6. Only a few external parts are needed to adjust the monitor chip for a wide range of supply tolerances. Logically combining the Power OK, under-voltage and over-voltage outputs generates a reliable line-fault indication for an external battery back-up system.

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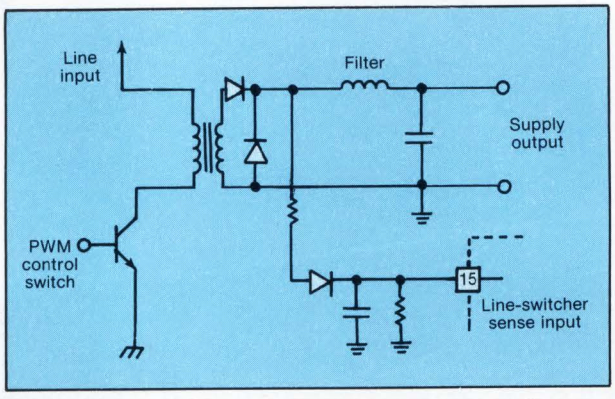

7. The line-switcher sense input catches faults in the switching power-train early enough to ensure an orderly system shutdown before a complete outage. In the hookup for a primary-side–controlled switching power supply, the headroom is limited to the hold-up time of the switcher's output filter.

output of the transformer is rectified, filtered, and divided down to a lower voltage for application to the line-switcher sense input. That input, with a 2-V threshold, has a hysteresis of 175 mV. Thus the rectification filter network is designed for a pk-pk ripple at the line-switcher input of 150 mV during low-line conditions. In that way, detection time will be fast but the hysteresis will prevent "stuttering" during a soft brownout.

Switching power supplies present a unique additional problem: A failure in the switching power train cannot be detected until an undervoltage condition occurs at the supply outputs. Proper connections within the switcher, however, can extract an early warning of power train failures (Fig. 7). Although the headroom is limited to the hold-up time of the supply's output filters, the delay time through the line-switcher sense input to the Power OK output is typically just 500 ns. In addition, the comparator hysteresis in that circuitry will minimize overdrive requirements. Thus the very fast indication of an impending power failure will provide the few milliseconds of warning that will prevent loss of data stored in volatile memories.□

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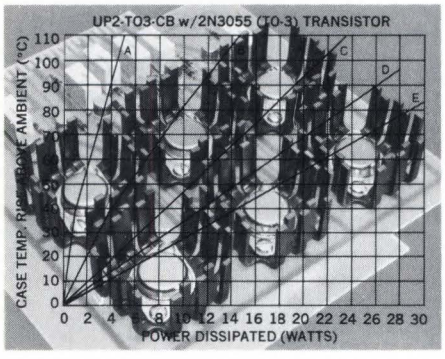

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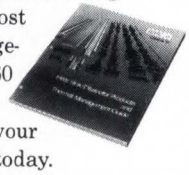

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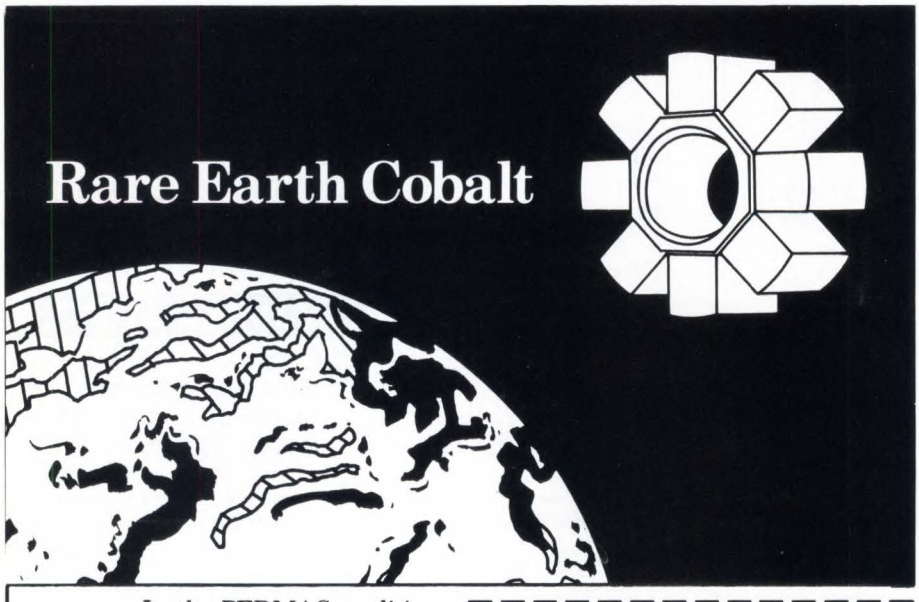

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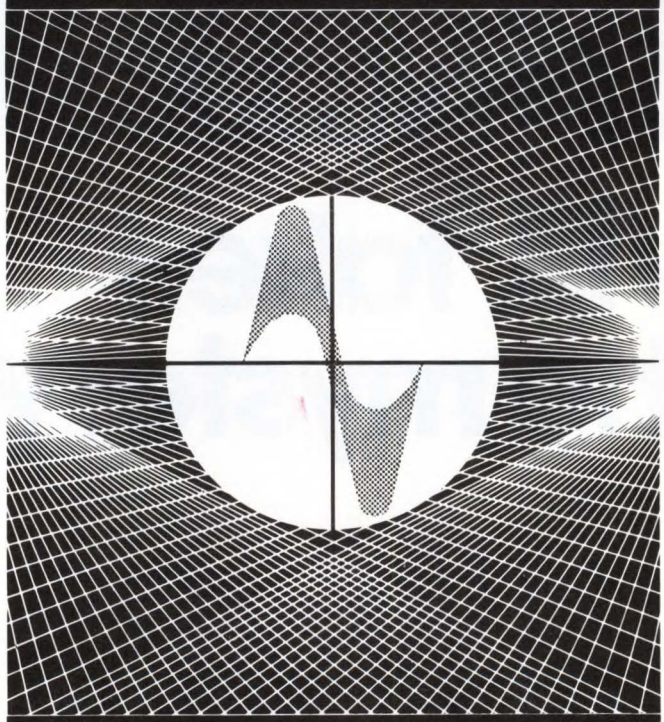

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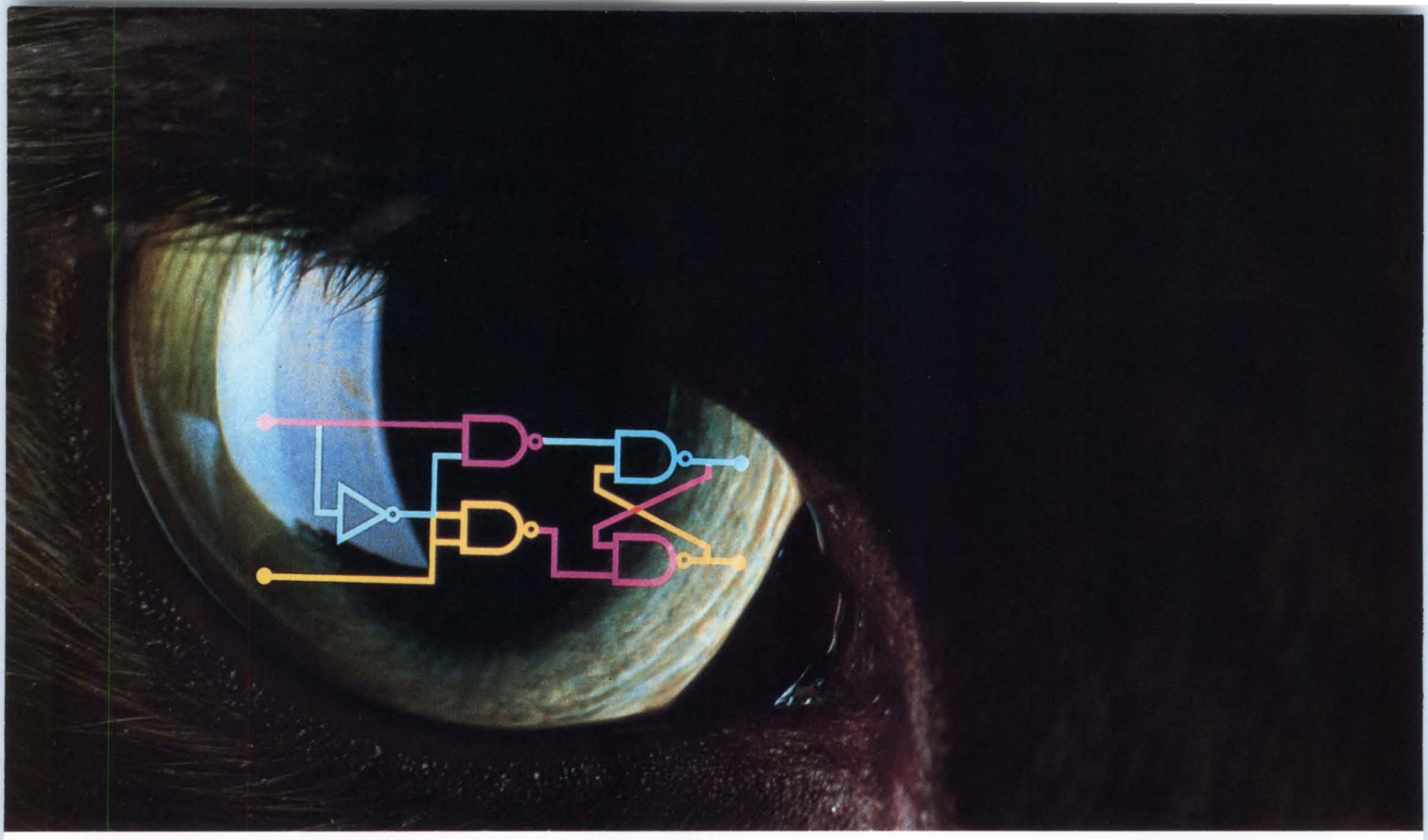

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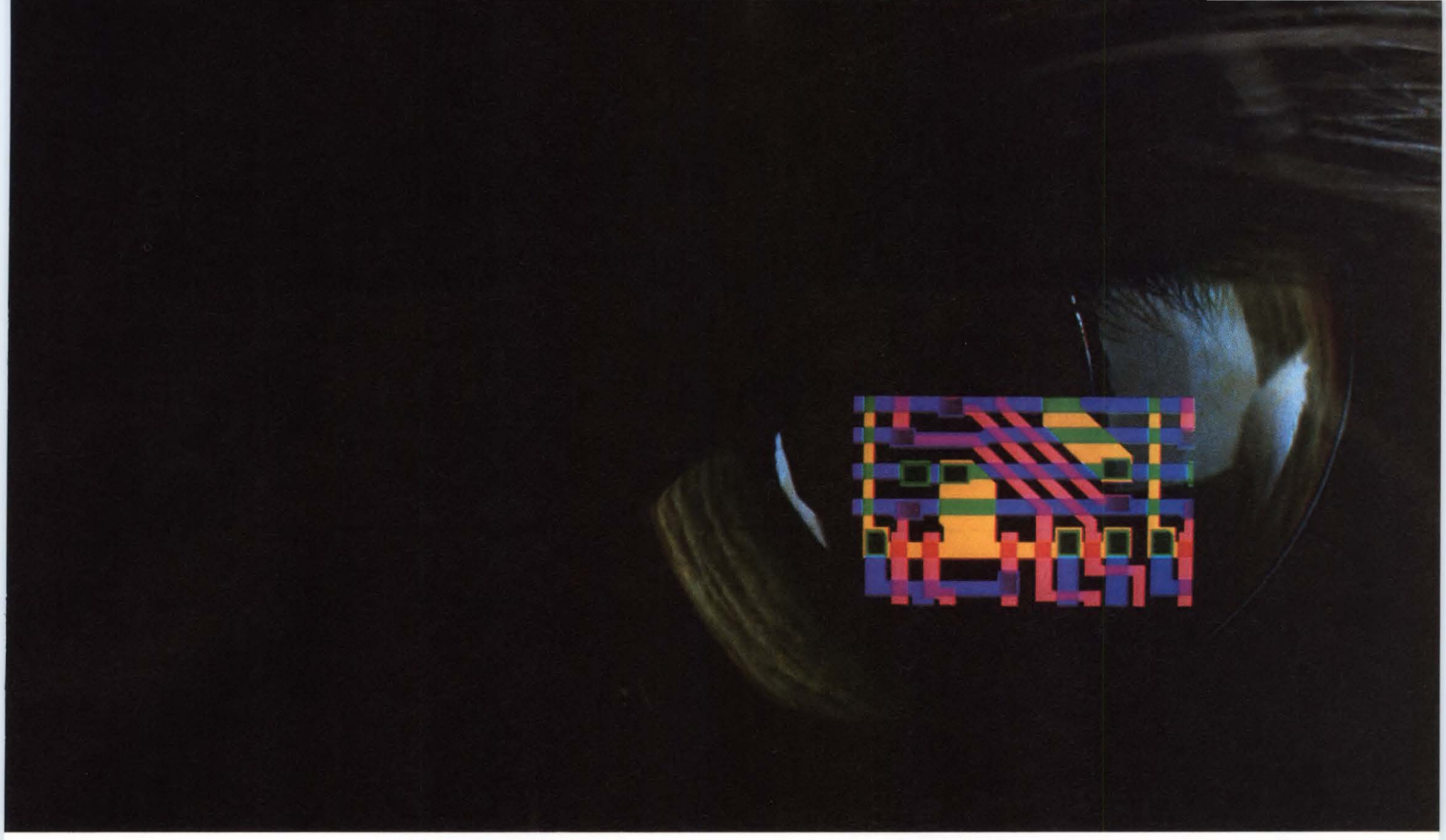

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DESIGN SOLUTIONS

Forth word simplifies numeric data entry

Jeffrey Anthony
Computer Scientist
Corby Industries Inc.
2747 MacArthur Road
Whitehall, Pa. 18052

Though numeric parameters can be passed to a Forth word using the stack, before that definition is invoked, a numerical value must often be obtained from an input device during program execution. Since many versions of Forth supply only character-string input words, numeric input definitions must be written using previously defined words (see the program).

Entering the value itself is quite straightforward. The word INPUT obtains the string number to be entered with the EXPECT word and then places it in the buffer designated by the contents of STRBUF. The definition STOI attempts to convert the string number to a single-precision integer value, leaving a True flag (1) if successful or a False flag (0) if the value is overrange. Those values are left on the stack.

The INPUT word alters only the top of the stack. It can, of course, be used in conjunction with any other Forth word.

The definition STOI converts a string number to a single-precision integer by transforming each of the string's characters to a digit, multiplying that digit by its corresponding power of 10, and summing the result. It handles negative numbers by multiplying the result by −1. Such numbers are designated by a negative sign appearing as the first character in the string.

The Forth word ** is used to calculate X^N, where X and N are the arguments of the definition. It recognizes X^0 and X^1 as special cases: the former because of its unique mathematical def-

Forth word for entering numeric data

```
( LEN---Calculate length of string in given buffers)
: LEN                           ( Buffer base address---length.)
    DUP  DUP                    ( Save buffer base address; make copies for)
                                ( memory pointer.)
    BEGIN
        C@ 0= 0=                ( Null character?)
    WHILE
        1+ DUP                  ( Increment memory pointer.)
    REPEAT
    SWAP — ;                    ( Calculate length; subtract buffer base)
                                ( address from final memory pointer value.)
                                ( Leave result on stack.)

( **--raise X to the n power)
: **                            ( X, N---X^N.)
    DUP 0= IF                   ( N = 0?)
        DROP DROP 1             ( Leave X^0 on stack.)
    ELSE
        DUP 1 = IF              ( N = 1?)
            DROP                ( LeaveX^1 on stack.)
        ELSE
            OVER SWAP 1 —           ( Set up stack for iterative multiplication.)
            0 DO
                OVER *          ( Multiply Previous result * X.)
            LOOP
            SWAP DROP           ( Leave result on stack.)
        THEN
    THEN ;
( Set string buffer to 1000H or whatever)
1000 CONSTANT STRBUF
( Set maximum number of input characters)
0006 CONSTANT MAXCHARS
( Define MINUS sign ASCII character)
002D CONSTANT MINUS
( Define TRUE and FALSE flags)
 0001 CONSTANT TRUE
 0000 CONSTANT FALSE
( STOI--Convert string number to single precision integer value;)
(       leave False flag if overrange, else leave True flag.)

: STOI                          ( ---N, flag.)
    STRBUF C@ MINUS = IF        ( String number negative?)
        −1 00                   ( Use −1 later to correct sign.)
                                ( Set sum to 0.)
        STRBUF LEN 1            ( Set string traversal range for)
                                ( characters 1 to LEN −1.)
    ELSE
        1 00                    ( Use 1 later to correct sign.)
                                ( Set sum to 0.)
        STRBUF LEN 0            ( Set string traversal range for)
                                ( characters 0 to LEN.)
    THEN
    DO                          ( Traverse string.)
        STRBUF I + C@ OF AND    ( Get numeric equivalent of)
                                ( ASCII character)
        0A STRBUF LEN I — 1 —   ( Multiply by appropriate power of 10)
        ** * +                  ( and sum.)
    LOOP
    DUP 8000 AND 0= 0= IF       ( Overrange?)
        DROP DROP 00 FALSE      ( Leave False flag and zero result.)
    ELSE
        * TRUE                  ( Leave True flag and correct sign.)
    THEN ;                      ( Leave result on stack.)
( INPUT -- Input string number and convert to single precision integer value;)
(          leave False flag if overrange, else leave True flag)
: INPUT                         ( ---N, flag.)
    STRBUF MAXCHARS EXPECT      ( Get input string.)
    STOI ;                      ( Convert string to integer.)
                                ( Leave result on stack.)
```

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inition and the latter because of the post-test structure of the DO loop used to calculate all other powers of X. For powers of X greater than 1, the word multiplies X by itself N times.

The LEN definition assumes that a string is ended by the null character ØØH. It counts from the beginning of the string specified by the value on the top of the stack to the character.

Wide-range oscillator operates above 20 MHz

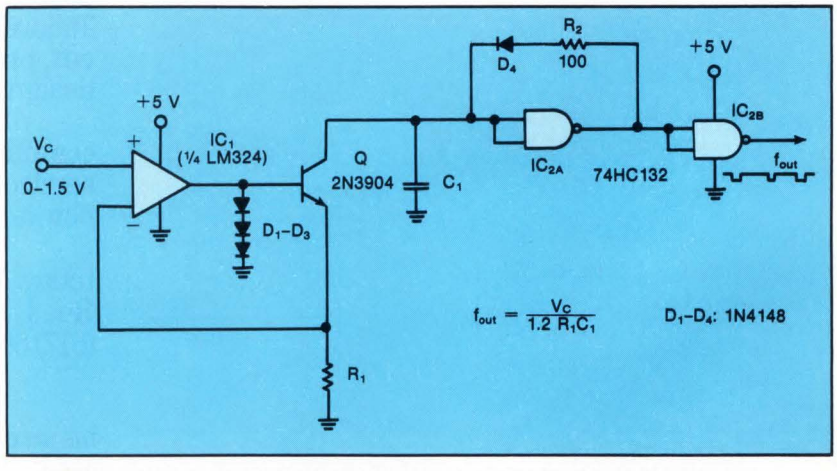
Einar Abell
Research Associate
Physics Department
University of Vermont
Burlington, Vt. 05405

The addition of several components to an HCMOS Schmitt trigger creates a voltage-controlled oscillator with a sweeping range of greater than 100,000:1 and an upper limit in excess of 20 MHz. The circuit is especially well suited to building frequency synthesizers that employ a phase-locked loop.

The circuit (see the figure) replaces single-chip designs that have a control range of more than 1000:1 but that cannot work above a few megahertz. Circuits that work at higher frequencies have a restricted range.

Circuit operation is simple: When the output of NAND gate IC_{2A} is high, capacitor C_1 charges rapidly through diode D_4 and resistor R_2 until the upper threshold is reached. Then, the gate's output goes low. Also, C_1 discharges to the low threshold by passing its current through a sink formed by transistor Q, resistor R_1, and op amp IC_1. That action creates a series of pulses whose spacing is a function of the input voltage, V_C. Diodes D_1 to D_3 clamp the voltage across R_1 to less than 1.5 V, since oscillation would cease if IC_2's lower threshold were exceeded.

The oscillation frequency can be calculated fairly accurately if it is considered the inverse of the discharge time of C_1. Thus starting with the formula $dV/dt = I/C$ and substituting V_C/R_1 for I and 1.2 (the difference between the upper and lower thresholds) for dV, the output



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*SPECIFICATIONS

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	Zero Center Scale	±.4%
	Set Point	±.2% of Full Scale

Input Impedance: 1 Million Ohms @ 50 mV. Standard milliamp units have a 50 mV compliance voltage drop across the input. Suppressed units have a 62.5 mV compliance voltage drop across the input.

Annunciator Interface: Open Collector Output.
V_{CEO} = 30 V
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Ic (max) = 300 mA

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frequency becomes $f_{out} = V_C / 1.2R_1C_1$.

The circuit's operation is linear to within 1% for a V_C of less than 0.1 V. Nonlinearity increases to about 20% at 1 V, since the charge time of C_1 becomes an increasing portion of the total oscillation cycle. Another limiting factor is the delay time of the Schmitt trigger, which holds the frequency to below 30 MHz.

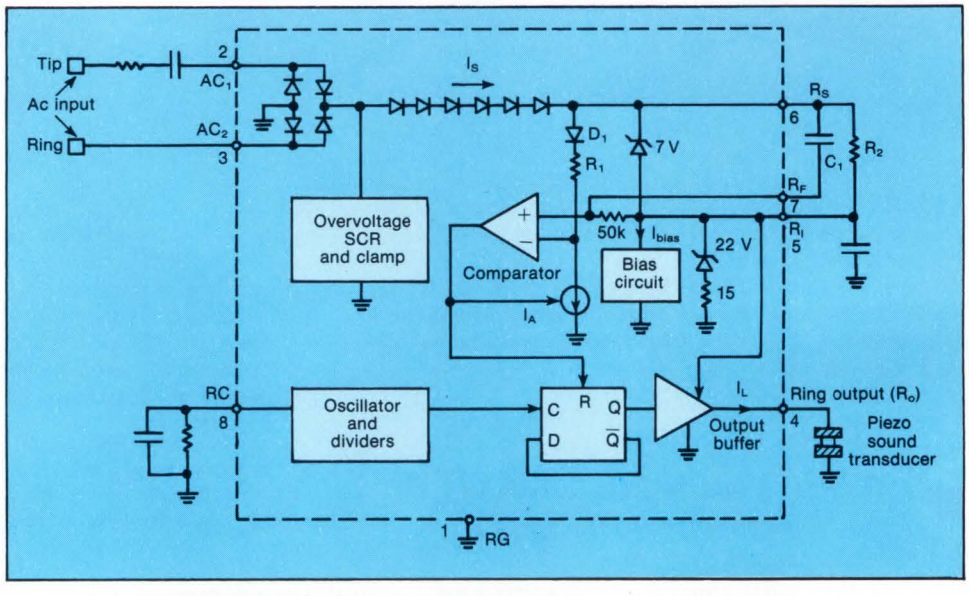
The op amp's positive offset can prove troublesome since the voltage across R_1 never drops to zero, thus reducing the frequency sweep to as few as two decades. The problem can be solved by an op amp with a negative offset or one that can have its offset driven negative or trimmed to zero if the output frequency must be zero for a 0-V input.

Tone-ringer circuit drives telephone-signal counter

Dennis Morgan
Applications Engineer
Motorola Inc.
Semiconductor Products Sector
7402 S. Price Road
Tempe, Ariz. 85283

Although it was developed to replace bulky electromechanical bell assemblies in conventional telephone sets, the MC34012 electronic tone ringer does a good job connecting a telephone line to a sequential ring-signal counter. The counter not only sounds a piezoelectric transducer after a selectable number of ringing pulses, it also has an auxiliary output that can turn on a variety of accessories, such as a modem or an answering machine.

In the tone ringer (Fig. 1), a full-wave bridge rectifies a ringing voltage and passes it through a string of diodes that provide the high input impedance required by telephone systems at low voltages. A small portion of the current



1. A comparator in the MC34012 tone ringer connect an oscillator to a piezoelectric transducer after detecting the incoming ringing voltage.

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CIRCLE 130

flowing through the diodes is diverted through diode D_1 and resistor R_1 to set the voltage at the inverting input of the comparator to 1.5 V below the voltage at pin 6.

The majority of the current, I_S, flows through resistor R_2. Capacitor C_1 and an internal 50-kΩ resistor filter the voltage generated across resistor R_2 before applying it to the comparator's noninverting input.

When the input voltage increases sufficiently to drop the voltage at the noninverting input to 1.5 V below that at pin 6, the comparator's output goes low, allowing the oscillator's signal to reach the sound transducer.

The output drives type 4N35 opto-isolator whose output, in turn, drives a 4017 decade counter through a pair of 4093 Schmitt triggers (Fig. 2). The counter outputs become active sequentially with each cycle of the ringing signal. When the selected output is active, the 4013 flip-flop changes state and drives the second 4N35 opto-isolator, providing the ground path that turns on the piezo sound transducer. The Q output of the flip-flop drives various accessories.

Circuit values are based on a typical ringing cadence of 2 seconds on, 4 seconds off. The counter and the flip-flop automatically reset when the ringing signal stops. Two separate grounds must be used to isolate the telephone line from the remaining circuit.

If the sound transducer's output is a bit high for comfort, the sound level can be adjusted by placing a 10-kΩ potentiometer in series with the transducer.

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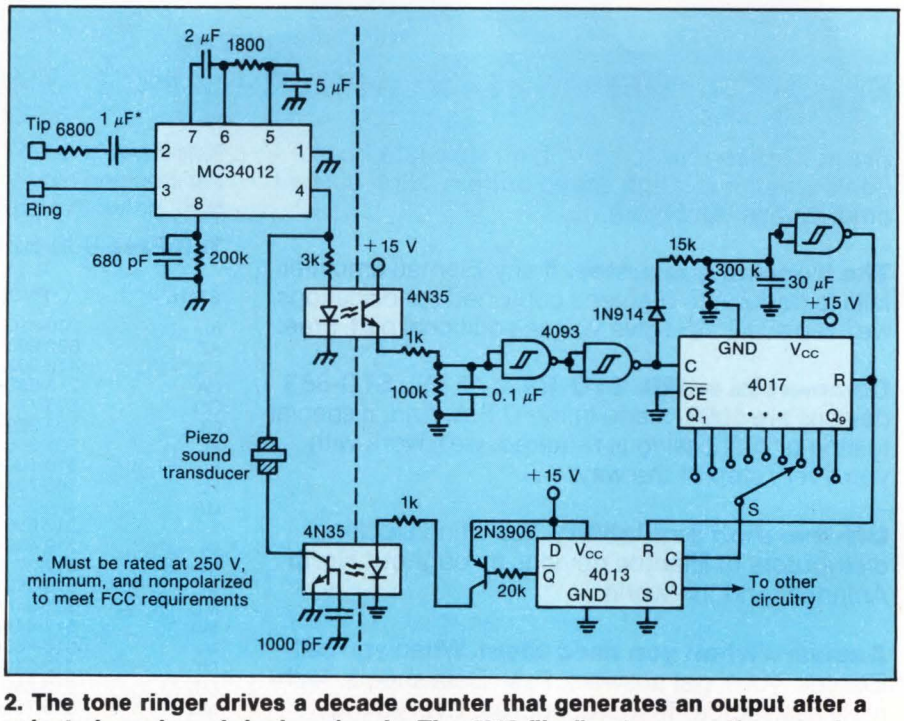

2. The tone ringer drives a decade counter that generates an output after a selected number of ringing signals. The 4013 flip-flop turns on the sound transducer and also provides an output to accessories, such as a modem.

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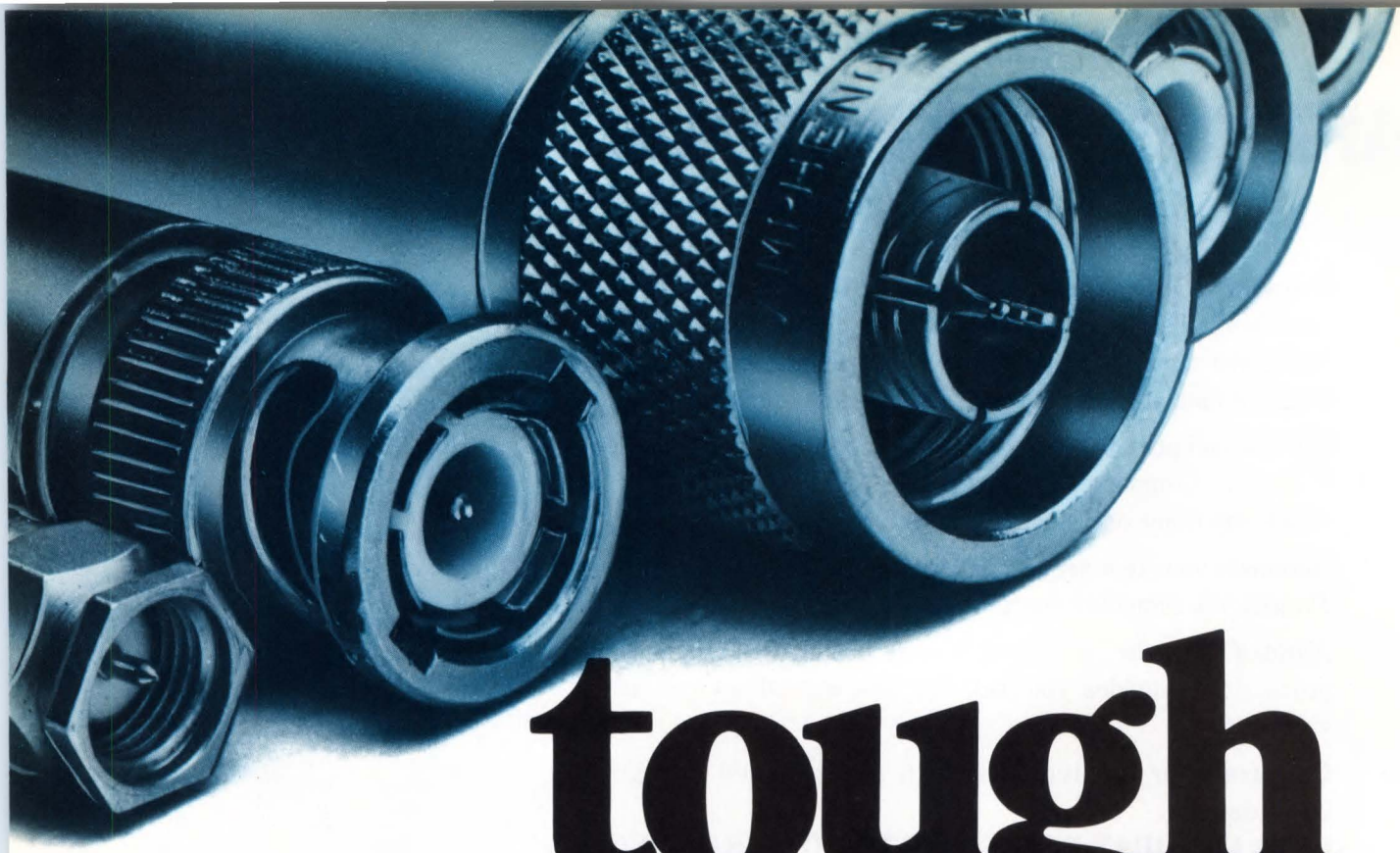

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7	●			
8	●			
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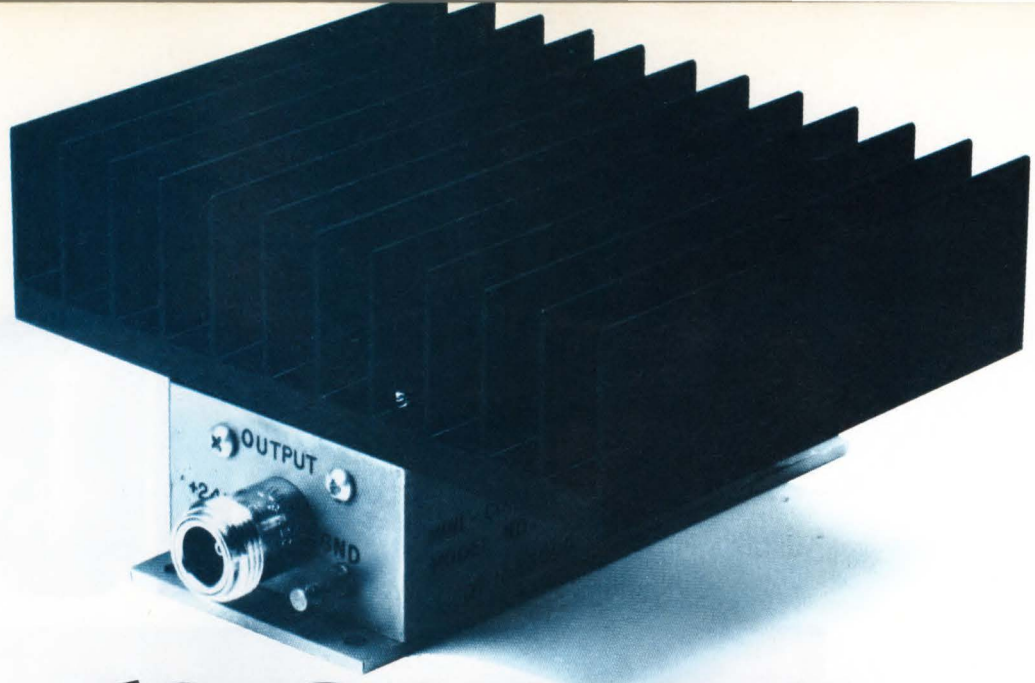

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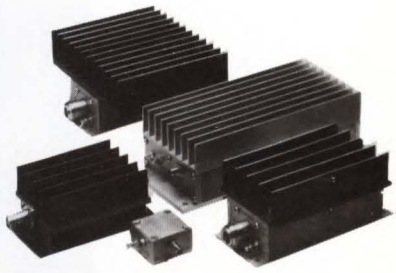

Model No.	Freq. MHz	Gain dB	Gain Flatness dB	Max. Power Output 1dBm Compression	Noise Figure dB	Intercept Point, Typ. 3rd Order	DC Power Voltage	DC Power Current	Price $ Ea.	Price Qty.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 dBm Min.	18 Typ.	+38 dBm	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.65A	474.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.75A	599.00	(1-9)
ZHL-1-2W	5-500	29 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+44 dBm	+24V	0.9A	495.00	(1-9)
ZHL-42	700-4200	30 Min.	±1.0 Max.	+29 dBm Min.	7.5 Typ.	+38 dBm	+15V	0.69A	895.00	(1-9)
ZHL-7-2W	600-800	28 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+43 dBm	+24V	0.9A	525.00	(1-9)
ZFL-2000	10-2000	20 Min.	±1.5 Max.	+17 dBm Min.	7 Typ.	+30dBm	+15V	0.1A	179.00	(1-9)

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C70 REV. B

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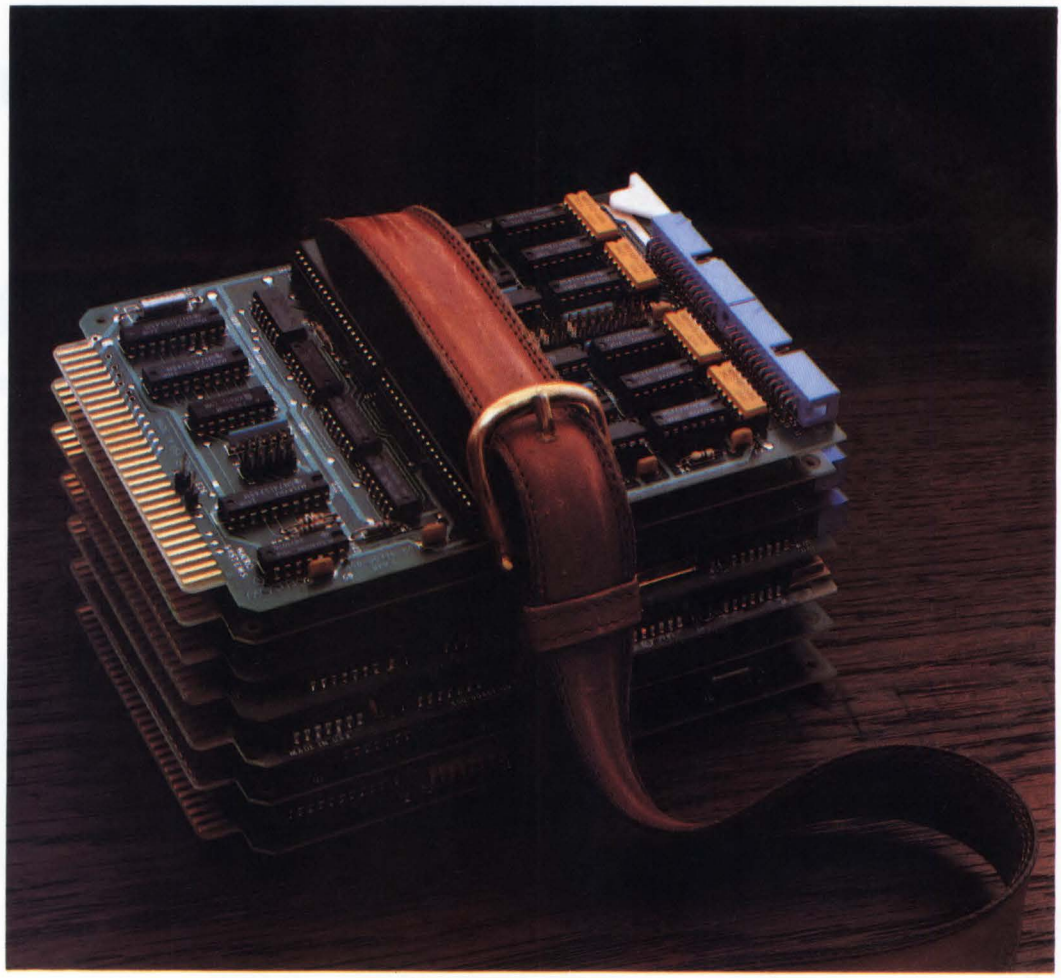

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CIRCLE 138

PRODUCT REPORT

FOCUS ON PORTABLE SCOPES

Even as they drop in size, portable oscilloscopes are adding new talents to their repertoire and meeting the user more than half way in ease of operation.

1. The LogicScope 136 is one of the smallest scopes, weighing just 1.25 lb. The 10-MHz miniature, from Pocket Technology, folds in half to just 1.75 by 4.5 by 8.25 in.

Like their benchtop counterparts, portable oscilloscopes are taking on more tasks while becoming easier to use. In addition, because portability is their main selling point, the already lightweight, compact devices are continuing to shrink.

Whereas just a few years ago a scope coming in at less than 15 lb was thought to be a featherweight, today there are a number of scopes under 5 lb. These can be tucked into a briefcase, often with room to spare. The somewhat larger portables have grown in power without putting on any weight or bulk.

Regardless of their size, portables are moving to higher frequencies and adding functions that previously required separate devices. By combining screen readings with deflection factors and multipliers, some scopes compute desired waveform parameters and display them on a digital readout or on the CRT itself. At the same time, many screens are obligingly becoming larger and brighter.

Even calibration, another time-consuming task, is now often handled (with unprecedented accuracy) by internal microprocessors. Benefiting from such control, a user can quickly check calibration whenever the scope has been tossed into a car trunk or thrown around by baggage handlers.

Digitization is another major trend in portable scopes, allowing manipulation of data that previously could only be viewed or stored. That storage, in fact, has gained a much longer life through digitization, eliminating the fading associated with tube storage.

Digital storage permits both the capture of transients during unattended operation and the comparison of real-time waveforms with reference models held in memory. What's more, the data from a digital scope can be permanently stored on a floppy disk or bubble memory for later processing. The only way to store analog data displayed on a CRT is to photograph it, a lengthy process that forces the user to carry yet another piece of equipment.

Finally, like digital benchtop scopes, digital

Terry Costlow

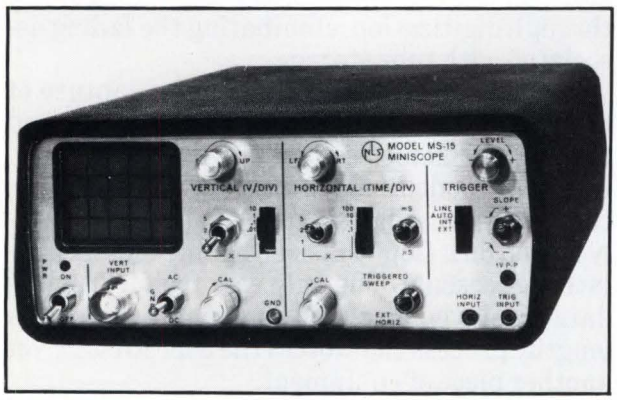
Focus on portable scopes

portables have extended their data reach to personal computers adding, RS-232 or IEEE-488 ports.

As these advances come into play, the need for portable scopes continues to rise. Field service users, a growing breed, increasingly are demanding lightweight personal scopes, rather than sharing a limited number between the service representatives of a base site. With automation assuming more tasks in the factory, scopes also are becoming more common in industrial environments, offering more flexibility and begging little floor space.

The push toward the much-discussed "scope on a chip" appears to be moving at a good pace. Custom chips, hybrid circuits, and alternative display technologies are helping to squeeze scopes into shirt pockets. Indeed, many scopes now comprise a single circuit board.

2. Hand-held scopes like North American Soar's Model 1000 shun bulky cathode-ray tubes for flat panels. The 1000 uses a liquid-crystal display with a 128-by-160-pixel matrix.



3. A traditional hand-held scope from Non-Linear Systems uses a small CRT to conserve space. The MS-15 has a 15-MHz bandwidth.

The incredible shrinking scope

One of the smallest to date weighs just 1.25 lb (Fig. 1) and folds in half when not in use, taking up just 8.25 by 4.5 by 1.75 in. Called LogicScope 136, the dual-trace device from Pocket Technology has a real-time bandwidth of 10 MHz, although with a front-end option, it captures pulses down to 50 ns. To fit into a package this small, the scope has shunned the traditional CRT display, using instead an array of LEDs that eliminates the depth requirements of the tubes. The LEDs, in four parallel rows, are spaced approximately 0.15 in. apart. Each pair of rows displays a single trace with a crudely digitized version of the waveform. Storing up to two dozen 128-bit waveforms in RAM, the battery-powered scope uses four custom chips (a display controller, a synchronization and trigger circuit, a master timing circuit, and a keyboard and memory controller) to help keep its size down.

A different substitute for the large CRT bottle is found in North American Soar's hand-held Model 1000, which uses an LCD with 128-by-160-pixel resolution. The display, which measures 6 by 7.5 in., helps keep the overall instrument size down to 10 by 7⅜ by 2⅞ in. The screen is viewed from the top, not the front as with most scopes (Fig. 2). The 3.5-lb device can be powered either by batteries or an ac adaptor.

More conventional-looking products in this lightweight class are somewhat heavier, but still remain below 5 lb. One hand-held battery-powered scope family goes up to 30 MHz, yet weighs only 3.5 lb. Non-Linear Systems' MS line comes in 15- and 30-MHz models, both triggered either internally or externally. Their screen size is 1 by 1.25 in., with a 4-by-5-division graticule (Fig. 3). When their lead-acid batteries are fully charged, the units can operate for about 45 min. Using ac power, they consume 50 W; the batteries will recharge in 16 hours.

Ballantine's 1020 series of single- or dual-trace scopes weighs 4.25 lb. Unlike many other portables, which take as much as 4 kV to drive the CRT with sufficient brightness, the 1020 drives the 1.5-by-2-in. screen using just 1 kV,

minimizing the space and weight required by the power supply. The low power consumption also keeps heat low, so no fan is needed. Cooling vents are also dispensed with, improving durability by giving dust no entrance. The family comes in 15- and 25-MHz versions.

Digital scopes gain momentum

The outgoing nature of digital portable scopes makes them especially popular. They communicate with hosts, plotters, or other devices without the need for any special interface. The reason behind this ease, of course, is that the most critical part of the interface—analog-to-digital conversion—has already been performed by the scope.

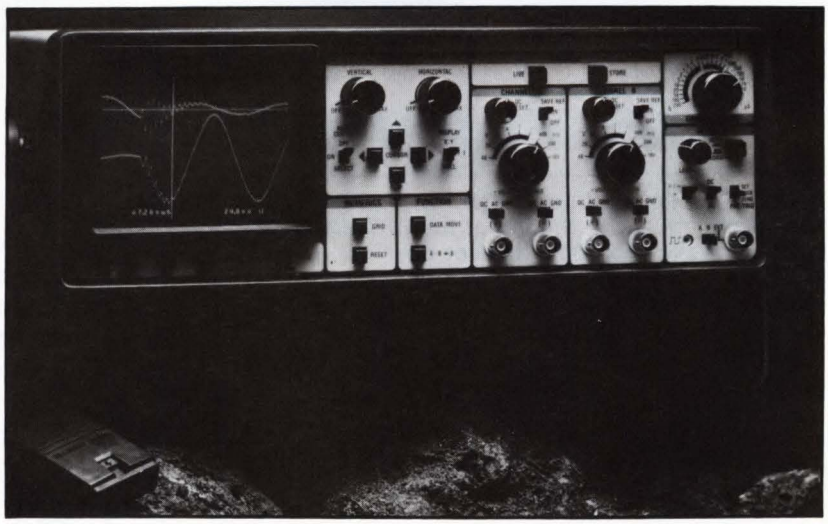
4. Digital scopes are moving in on higher frequencies, where analog now holds sway. The Philips PM3311 goes up to 60 MHz, with single-shot capabilities of 150 MHz.

The scope's a-d converter is simultaneously its strongest and its weakest point. It makes possible all of the features that make digital scopes so attractive, yet it also limits their bandwidths. Although most digital scopes use off-the-shelf flash a-d converters, some manufacturers have taken other routes for speeding up conversion rates while awaiting faster a-d chips. Philips Test & Measuring Instruments, for example, has combined a track-and-hold circuit and what the company calls a profiled peristaltic charge-coupled device on a single chip. The P^2CCD gathers and stores analog data, then holds it while a successive-approximation converter digitizes it.

That technology is implemented in Philip's PM3311 60-MHz scope with single-shot capabilities up to 150 MHz. The dual-trace scope has 8-bit resolution and can sample sequential signals at 200-ps (5-GHz) intervals. The 23-lb scope has a 3-by-4-in. screen (Fig. 4).

Another high-speed digital scope is the Sony/Tektronix 336, weighing in at only 11 lb. It can measure periodic signals with a bandwidth of up to 50 MHz, storing up to 1024 words of 8 bits in memory. In the nonstorage mode, the dual-trace unit also works up to 50 MHz.

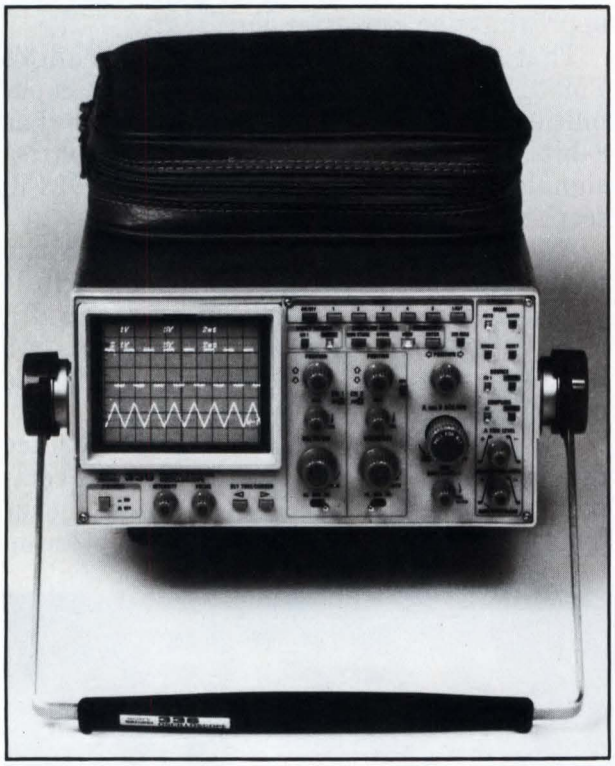
The 336 offers an optional GPIB interface that lets users transmit data to a personal computer for long-term storage or analysis. The interface option also includes memory to store up



5. Nicolet's 3091 digital scope lets users store waveforms permanently with a bubble memory cartridge, which holds five 4k-by-12-bit records (left).

to 18 waveforms, with battery backup to preserve the memory when power is turned off.

A large, flexible memory gives the Gould DSO 4040 the edge over many competitors. The memory, holding up to 5000 bytes, can be dedicated to a single channel or split between two or four. The scope has a sampling rate of 10 MHz when the storage mode is used, with a real-time rate of 25 MHz. It can freeze a waveform, then let the user scroll it across the screen as if unrolling a strip chart printout. When it is being scrolled, the waveform can be expanded up to 20 times during calibration or up to 50 times if calibration is not needed. The scope is on the heavy end of the portable spectrum, weighing 36.3 lb.



6. Digital readouts of parameters and other measurements appear at the top of the CRT display on the Sony/Tektronix 336. The user does not have to look away from the screen at settings or count the number of divisions.

Nicolet's 3091 offers digital storage but goes one step further by using a bubble memory to store data permanently. The small bubble cartridges, which plug into the side of the scope, can be removed, letting users capture a number of waveforms for processing in a lab (Fig. 5). The cassette also lets users grab one waveform, then go quickly on to other tasks.

Five 4k-by-12-bit records or ten 2k-by-12-bit records can be stored on a single bubble cassette. The scope has a 5-in. screen for high-quality display, as well as 12-bit resolution to ensure accuracy and reading ease. With a 300-kHz bandwidth, the 20-lb scope samples at rates of up to 1 MHz. An RS-232 port is standard, and an IEEE-488 connector has just been added as an option.

Simplifying use

Along with the addition of new features, the incorporation of microprocessors into portable scopes is making the devices simpler to work with. Analog and digital scopes are streamlining both setup and standard applications by automating tasks previously handled by the user. Some let a remote computer handle the setup, while others minimize the number of steps needed.

The analog Sony/Tektronix 336 simplifies setup with CRT-displayed menus. The user can choose from among the parameters given, instead of searching through many front-panel controls. These parameters are then displayed on the screen with the waveforms, so that users can interpret the screen without glancing at the control panel to see where dials are set (Fig. 6).

Another easy-to-use analog scope, the 100-MHz Hitachi V-1100, features a CRT readout in addition to a waveform display. A built-in microprocessor permits digital display of such measurements as the voltage value between ground level and the reference cursor or the time difference between two points. The scope determines and displays the panel settings, as well. The four-channel instrument weights 22 lb.

The SC61 from Sencore also simplifies the user's chores by displaying waveform measure-

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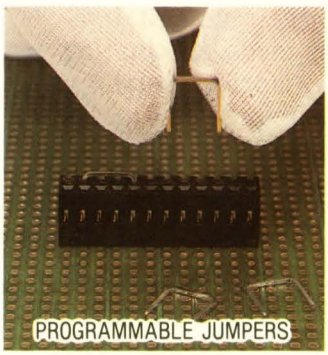
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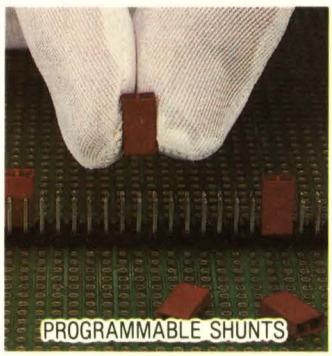
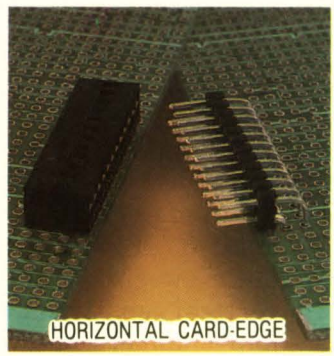

PROGRAMMABLE SHUNTS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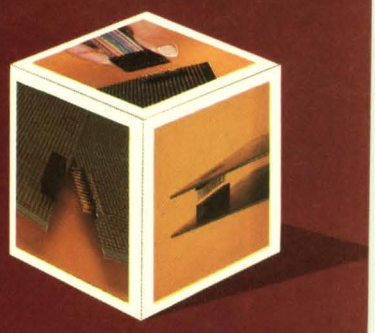

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CIRCLE 139

Product Report: Focus on portable scopes

ments digitally. When the desired waveform appears and a Display button is pressed, its measurements are shown on a six-digit LCD located directly above the CRT. The 60-MHz scope, weighing 31 lb, is compatible with the IEEE-488 bus, letting a computer handle setup while the user performs other tasks.

Speed kings

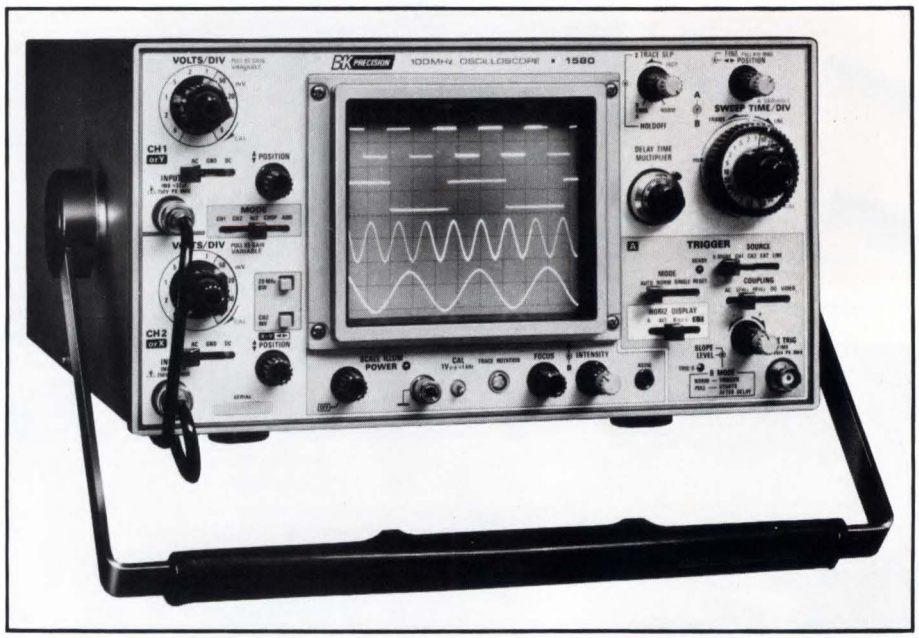
It is tough enough to build a really fast a-d converter without trying to keep its size and power consumption down. Really high-frequency portables, therefore, are still basically analog scopes. However, they do take advantage of digital technology, in the form of microprocessors, to enhance their performance and ease of use.

One of the highest-frequency portables is the Tektronix 2465, a 300-MHz scope. It has a maximum sweep speed of 500 ps per division, with a vertical sensitivity of 2 mV per division. The four-channel scope, weighing 20.5 lb, also offers waveform cursors with digital readout, making it simpler to use. A new option, which cannot be retrofitted to existing scopes, is an IEEE-488 connection. With that interface, users can program the 2465 using a personal computer. However, since the analog scope has no digitizer, it cannot transmit waveforms back to the host.

Hewlett-Packard has a family of scopes which can handle frequencies up to 275 MHz. The 1725A, 1726A, and 1727A all fall into this category. The 1727A boasts variable-persistence phosphors, which let users freeze a signal on the display for temporary storage. LED indicators display the operating mode, eliminating lost signals resulting from improper settings.

The smallest of the high-frequency scopes is the 4150 from Vu-Data. This 14.5-lb device has a bandwidth of 150 MHz yet has dimensions of just 8.75 by 15.1 by 4.25 in. The scope's predecessor, the 4100, is a 100-MHz unit of similar size.

Unlike many other manufacturers, Vu-Data does not use custom chips to shrink sizes. Instead, the company uses smaller components. For example, a smaller CRT with 8 by 10 di-



7. Scopes with 100-Mhz bandwidths like the B&K Precision 1580 are becoming increasingly common. The 1580 weighs 19.3 lb.

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CIRCLE 140

visions, each measuring 0.25 in. However, smaller dot size and high brightness ensure good resolution and readability.

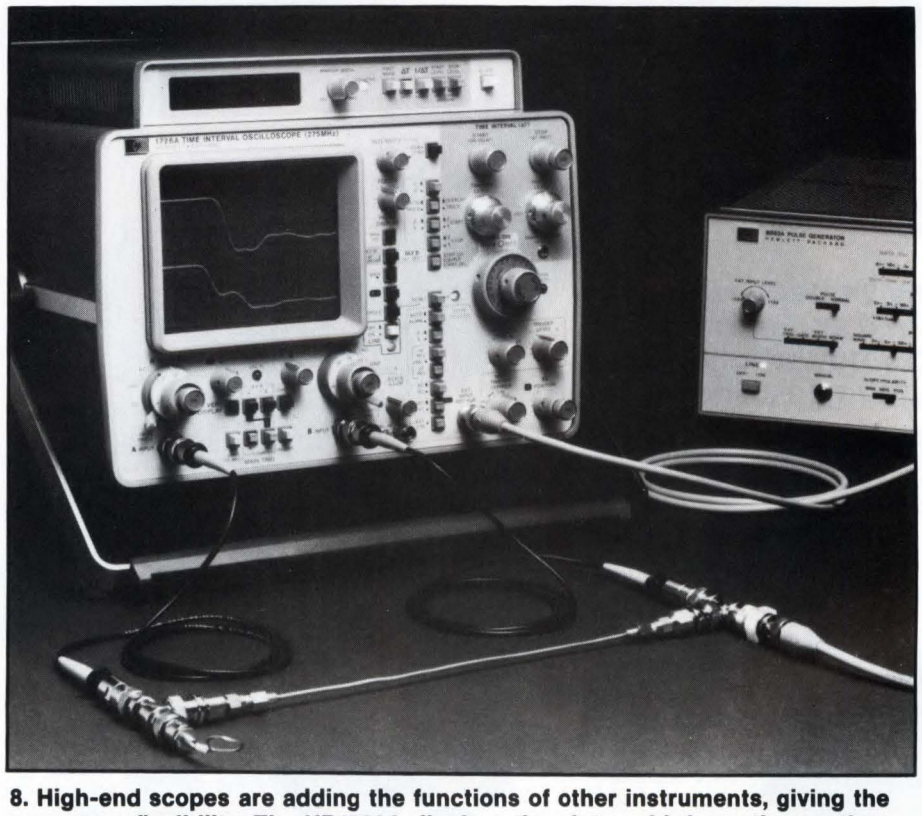
Although 100 MHz was previously a lofty bandwidth for portables, a host of manufacturers have now unveiled 100-MHz devices. Typical of these is B&K Precision's 1580, a 19.3-lb scope with dual-trace and dual-time capabilities (Fig. 7). Standard features include bandwidth limiting, 23 calibrated sweeps, and sweep magnification of up to 10 times normal size.

Adding functions

In addition to the move toward higher speeds and greater operating ease, many scopes are adding functions that previously required a second device. For instance, as timing becomes increasingly important, given the high clock speeds of computers and communications devices, scope users will encounter more and more timing measurement operations. Take Hewlett-Packard's 1726A high-speed scope: the timing portion of the scope monitors any repetitive signal that the instrument displays. It achieves 10-ps resolution and ±50-ps accuracy. The timing information is displayed on an LED readout (Fig. 8). Time interval operations can be performed in two modes, overlapped or triggered.

A counter, timer, and multimeter are built into Tektronix's 2236 100-MHz scope. The vertical, horizontal, and triggering systems of the scope are used to acquire data for these devices; their outputs are shown on a four-character vacuum fluorescent display.

The multimeter, which has side inputs, is a 5000-count autoranging unit. The scope uses



8. High-end scopes are adding the functions of other instruments, giving the user more flexibility. The HP1726A displays time interval information on the readout atop the device.

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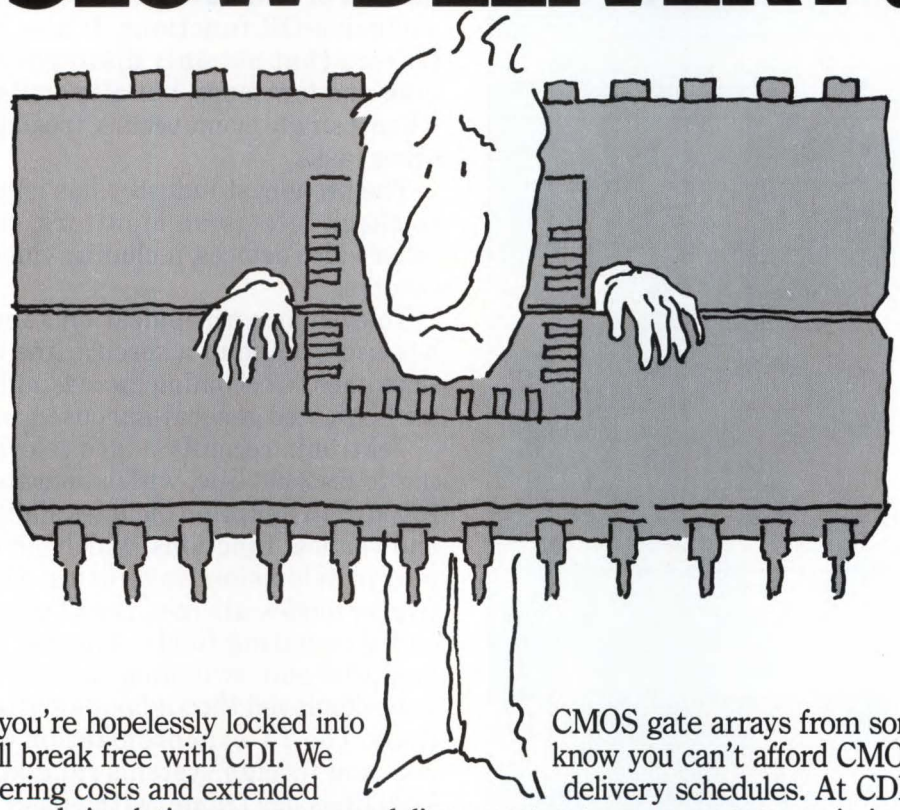

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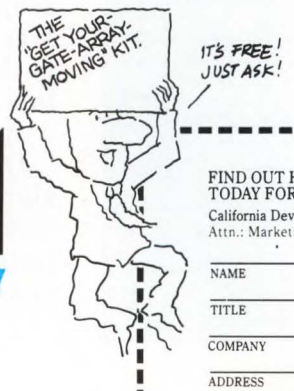

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CIRCLE 141

Product Report: Focus on portable scopes

Directory of portable oscilloscope manufacturers

	Under 100 MHz	100 MHz and over	Under 10 lb	Analog	Digital	Circle
B&K Precision, Dynascan Corp. Chicago, Ill. (312) 889-8870	★	★		★		451
Ballantine Laboratories Inc. Boonton, N.J. (201) 335-0900	★		★	★		452
Dumont Oscilloscope Laboratories Inc. West Caldwell, N.J. (201) 575-8666	★	★		★		453
Gould Instruments Ltd. Hainault, Ilford Essex, U.K. 01-500-1000	★				★	454
Heath Co. Benton Harbor, Mich. (616) 982-3443	★			★		455
Hewlett-Packard Co. Colorado Springs, Colo. (303) 590-1900	★	★		★		456
Hitachi Denshi America Ltd. Woodbury, N.Y. (516) 921-7200	★	★		★		457
Hung Chang Products U.S.A. Ltd. St. Petersburg, Fla. (813) 577-9010	★			★		458
Kikushi International Corp. Gardena, Calif. (213) 515-6432	★			★		459
Leader Instruments Corp. Hauppauge, N.Y. (516) 231-6900	★			★		460
Nicolet Instrument Corp. Madison, Wis. (608) 271-3333	★				★	461
Non-Linear Systems, Kaypro Corp. Solana Beach, Calif. (619) 481-3954	★		★	★		462
Norland Corp. Fort Atkinson, Wis. (414) 563-8456	★				★	463
North American Soar Corp. Cherry Hill, N.J. (609) 488-1060	★		★	★		464
Philips Test & Measuring Instruments Inc. Mahwah, N.J. (201) 529-3800	★	★		★	★	465
Pocket Technology Inc. Columbia, Md. (301) 730-5500	★		★		★	466
Sencore Inc. Sioux Falls, S.D. (605) 339-0100	★			★		467
Simpson Electric Co. Elgin, Ill. (312) 697-2260	★			★		468
A. W. Sperry Instruments Inc. Smithtown, N.Y. (800) 645-5398	★			★		469
Tektronix Inc. Beaverton, Ore. (503) 627-7111	★	★	★	★	★	470
Vu-Data Corp. San Diego, Calif. (619) 279-6572	★	★		★		471

the same probe for its multimeter as for the analog scope measurements, reducing circuit loading and minimizing the number of necessary attachments. This can be especially valuable when testing high-density circuits, where fitting in two probes can be a real problem.

Pocket Technology's lightweight LogicScope has some logic analyzer functions in addition to its scope capabilities. These include the comparison of two waveforms with AND, OR and exclusive-OR functions. It also has an audio feature that not only distinguishes between high and low tones, but also emits a tone itself when a single event occurs, freeing the user for other tasks.

The broadcast industry has long used scopes to check television monitors, cameras, and other video devices, including video cassette recorders.

Television synchronization, therefore, which lets users pinpoint a specific line within a TV's scan lines, is becoming increasingly popular for sophisticated general-purpose scopes.

Tektronix recently added television triggering to its 2400 line, which operates at 150 and 300 MHz. The option includes additional trigger and vertical functions, which simplify the display of television waveforms. There are four trigger modes: all lines, field 1 lines, field 2 lines and alternating fields. Another feature, preamplifier gain switching, allows flat waveform to be displayed throughout all attenuator positions. The TV synchronization option serves U.S. and foreign systems ranging from 525 to 1280 lines per frame, with either 50- or 60-Hz interlaced or noninterlaced scanning.

Simpson's Model 454, a 15-MHz scope weighing 13 lb, provides TV synchronization on either of its two channels. Sencore also has added that capability to its SC61.

In the more traditional areas, many analog scopes eschew additional functions and high frequencies to provide low-cost, easy-to-use packages. B&K Precision's 1405, for example, has a bandwidth of just 5 MHz and displays only a single trace.

Other scopes go up to 60 MHz but are designed for the low-end user. Often these units remain unchanged for years, giving the user a reliable scope at the cost savings typically associated with mature products. □

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CIRCLE 142

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Speed? It reads up to over 400 measurements/s. Its 2ns real-time clock gives higher resolution and speed than others."

ability count just as much as quality and price."

enough for over 20 hours of line voltage-independent stabilization.

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High-resolution frequency counting, period and time-interval measurements are supplemented by valuable extra facilities like: PHASE, BURST and RPM.

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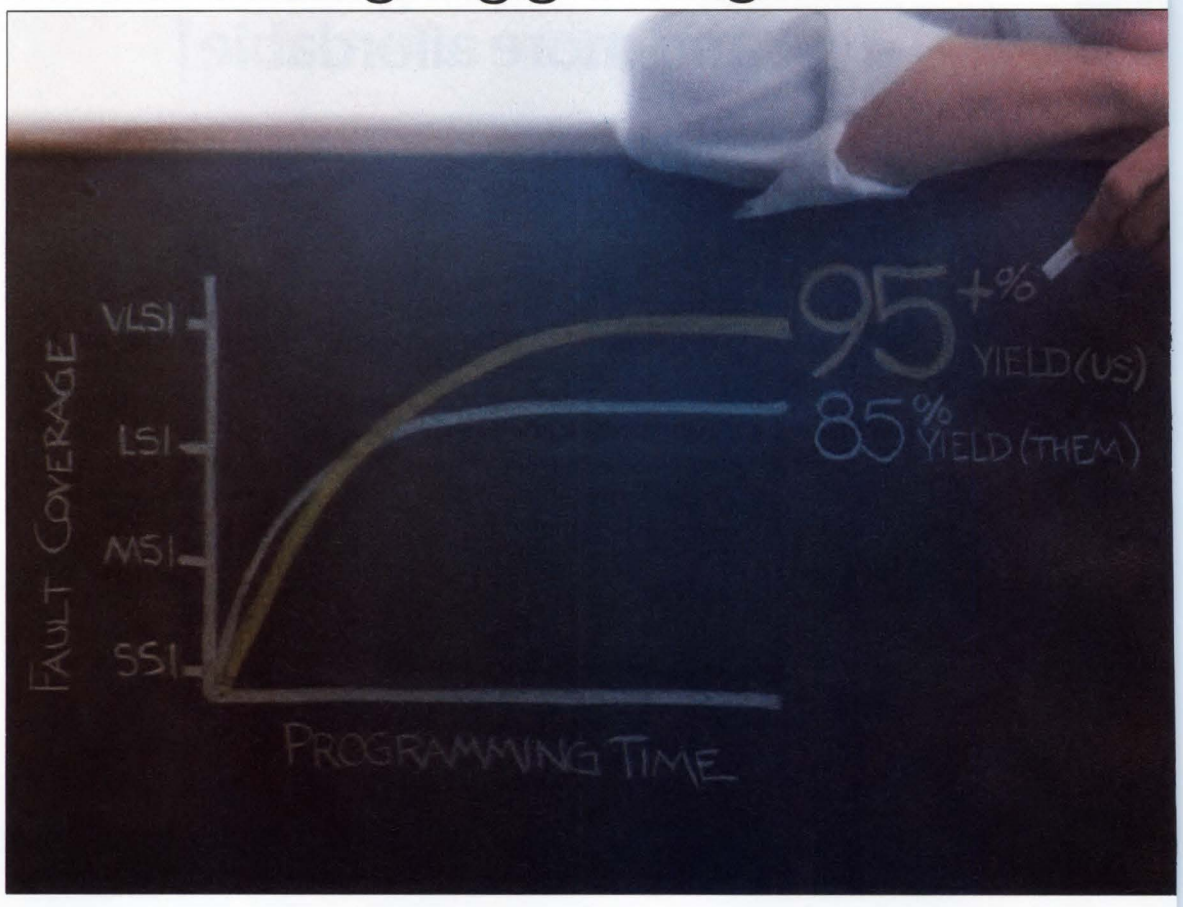
PHILIPS

CIRCLE 143

The L200 Board Test System. For when the going gets tough.



Consider the L200 Board Test System by Teradyne. Combining both in-circuit and functional testing capabilities, it's absolutely the best system available to tackle today's complex designs.

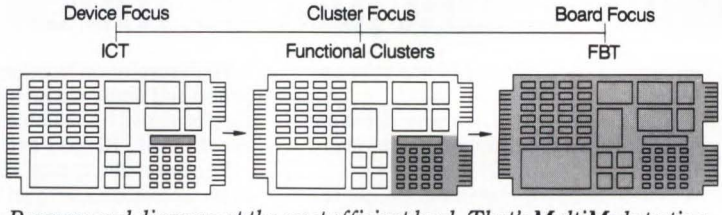
We call this unique integration MultiMode™ testing. It's a Teradyne invention already working on over 100 machines turning out sophisticated electronics. Our competition hooted at first. Now they're scrambling to catch up. Why?

Because the L200 delivers yields of some 95% plus at system test on modern VLSI boards. On average, that's a full 10% higher than any of our competitors. Nobody does it better. Here's how it works.

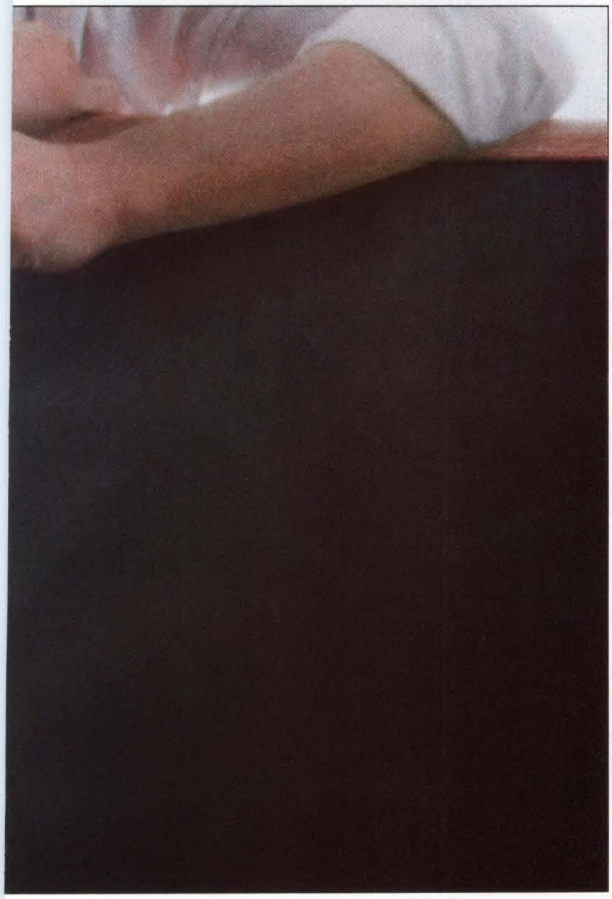
The Three P's of MultiMode.

Partitioning. Patterns. Performance. This is what you need to get good yields. With MultiMode testing, the L200 gives you all three.

Partitioning. The L200 gives you precision functional test capability with overdrive on every channel. That means you can test at the most effective level—device, cluster or board.



Program and diagnose at the most efficient level. That's MultiMode testing.



Partition your boards into easily programmable segments. Quickly and accurately diagnose faults at any level with our software's advanced diagnostic algorithms for in-circuit and functional fault isolation.

Patterns. You need to apply lengthy pattern sets to get high fault coverage on today's VLSI boards. And the L200 is up to the task.

It comes with a powerful computer, up to 4 megabytes main memory and high capacity disk storage. So you can store even the largest job plans.

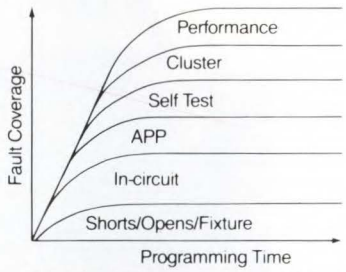
Then the L200 can apply millions of unique patterns at a high effective test rate. So you can do more testing in a controlled period of time than ever before. A custom Digital Command Processor quickly transfers patterns to test channel memory. There, they're stored efficiently and burst at pattern rates up to 10 MHz to boards under test.

And at the 10 MHz rate, with microprogrammable APP hardware, you can algorithmically generate complex memory test patterns continuously.

Performance. The L200's hardware formatting, multiple phases, and ability to change timing on the fly with 1 ns resolution, let you easily emulate complex waveforms. And that sort of precision in the time domain lets you really test the limits of board performance.

A Smart Job Plan.

The L200's software lets you efficiently build one MultiMode program for all tests using a common data base. Take patterns from all available sources—including in-circuit pattern libraries, design data bases, LASAR™ software, and self test.



Take test patterns from a variety of sources to optimize fault coverage in the shortest programming time possible.

Get going quickly by generating the easiest tests first. Then add test segments to maximize fault coverage. As volume builds you'll be driving up yields at system test.

A Tough Tool for a Tough Job.

We all know that programming modern VLSI boards is hard work. But we've built a machine and developed a strategy that makes the task practical. And you successful.

If you're going to build VLSI boards, MultiMode on the L200 is the only way to go. And the rewards will be great.

You'll be driving up yields at system test. And that can save your company a fortune.

For more information, call Teradyne today, (617) 482-2700. Or write Teradyne, 321 Harrison Avenue, Boston, MA 02118.

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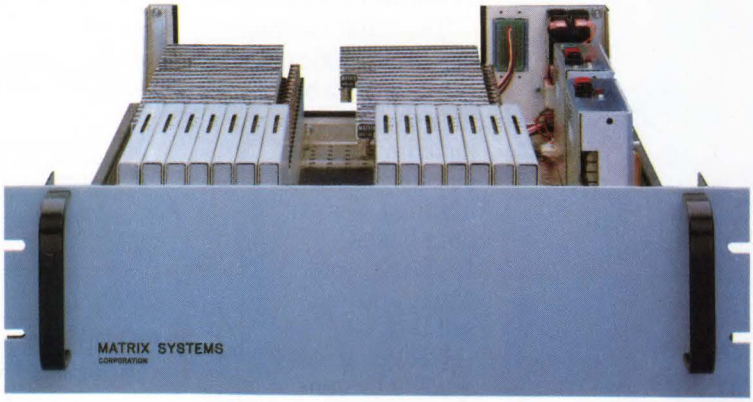

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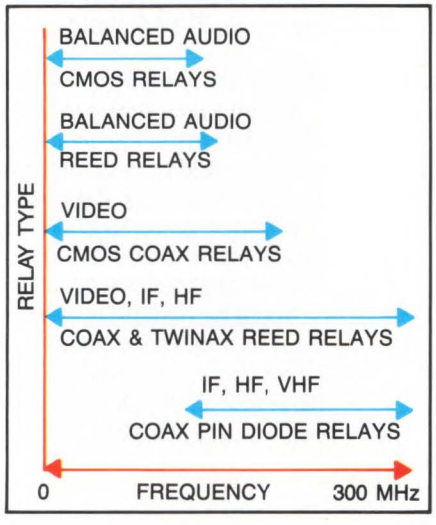

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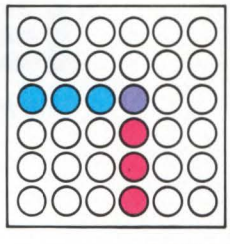

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CIRCLE 147

Circuit compiler cuts chip area 25% to 40% over standard cells

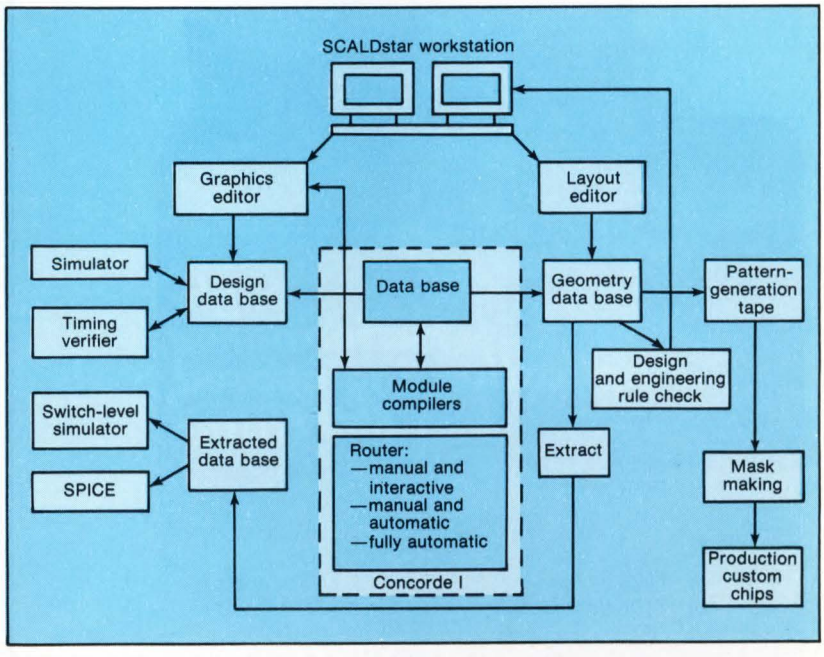
The Concorde I, one of the first commercial silicon compilers, designs circuits that are 25% to 40% more silicon-efficient than those composed of standard cells. The software, written by Seattle Silicon Technology Inc. (Bellevue, Wash.), was modified by Valid Logic for use on its SCALDstar workstation and is available as either an add-on or as part of a complete hardware-software package.

Using the Concorde I, which consists of more than half a dozen subprograms that interface with SCALDstar's CAD software (see the figure), designers can enter a schematic, compile subsections as modules, simulate and test the modules, connect them automatically or interactively, and then simulate and lay out the chip.

The key subprograms are the module compilers, which are tailored to the logic functions desired for a particular design—gates, RAM, ROM, or programmable logic arrays, for example. When a designer specifies a detail to be added to a schematic—say, a gate or a flip-flop—he or she triggers an interactive process. A set of menus appears in a window, permitting the user to define such factors as loading or the number of inputs (or bits, in the case of a counter) and immediately get an estimate of speed, power consumption, and area.

As circuits are stored by the workstation's schematic capture program, the system compiles the subelements: Each gate, flip-flop, counter, RAM block, and so on is designed from the transistor level to the top-most mask, permitting very efficient circuit layout. In contrast, standard cells are predesigned and merely interconnected to make larger cells.

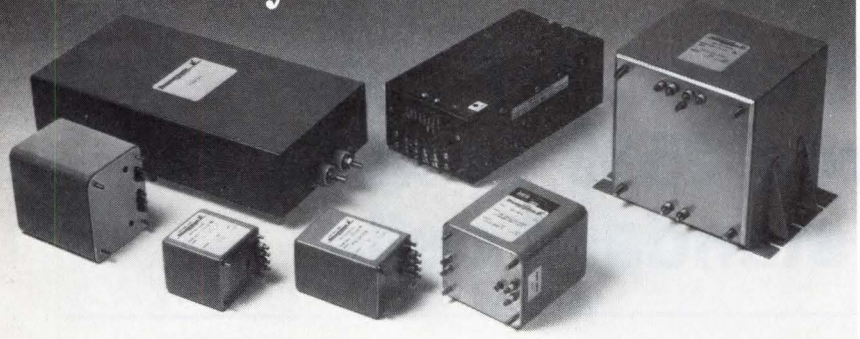
Some of the circuits that



Able to merge right into an existing SCALDstar workstation, the Concorde I silicon compiler connects the design data base to the geometry data base. The software produces circuits 25% to 40% smaller than those patched together with standard cells.

Dave Bursky

The New Technipower Modular/Switching Power Supplies... You'll Think They're Custom Built!



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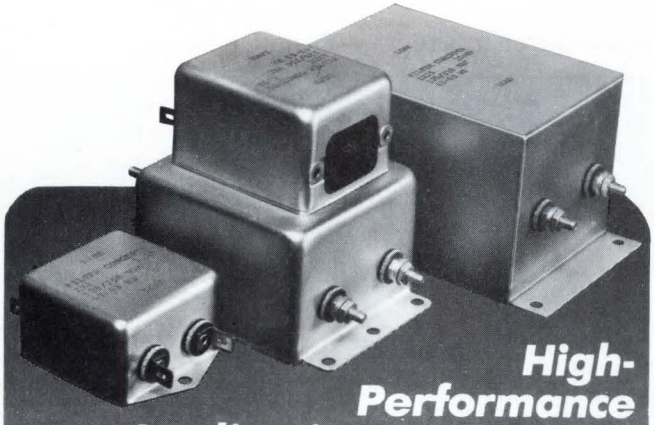
CIRCLE 148



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CIRCLE 149

SOFTWARE

can currently be compiled include MSI-level devices like counters, registers, shifters, arithmetic elements, encoders and decoders, and clock generators.

The compiler works with any 3-μm p-well CMOS process. The first step in using the package is to put the parameters of the fabrication process into the data base to define the transistors, spacing distances, diffusions, and the like. This procedure alone may take a few weeks, since test structures must be made on the fabrication line to verify the process.

Optional software for the Concorde I includes an analog-module compiler that creates various amplifiers, a-d and d-a converters, switched-capacitor filters, and analog switches. Another compiler handles complex circuits such as microcomputers, and a routine called a packaging editor generates diagrams of the optimum yet physically feasible bonding and helps the designer select the best package for the circuit.

The Concorde I software costs $25,000; a combination hardware-software system runs about $100,000. The optional analog-module and complex-function compilers cost $10,000 each; the packaging editor, $5000. The software is currently going out for beta-site testing and will be available in November.

Valid Logic Inc., 1395 Charleston Road, Mountain View, Calif. 94043; Don Ritzman, (415) 940-4000.

CIRCLE 309

SOFTWARE

Simulator for 8048 shows six windows, runs on IBM PC

Software that runs on the IBM personal computer displays six windows as it simulates and helps debug programs for the full 8048 family of microcontrollers. The software, the first such multiple-window package for the 8048 to run on the IBM PC, is estimated to cut program development time by a factor of 10.

The SIM-8048 program, developed by Cybernetic Micro Systems, fills the six windows simultaneously with the source and assembly code, the register and flag values, the program counter value and the contents of some memory locations, the pointer and stack values, the actual program flow in flow-chart form (in a large window), and commands specified by the user. Additionally, the software can simulate a counter-timer, including its reactions to interrupts, and even an 8155 external RAM chip.

Each of the simulator's 50 commands consists of an alphabetical or a control character. The commands cover operations like register value declaration; trap and breakpoint specification; single-step, automatic-step and fast execution; and even immediate control of the I/O pins.

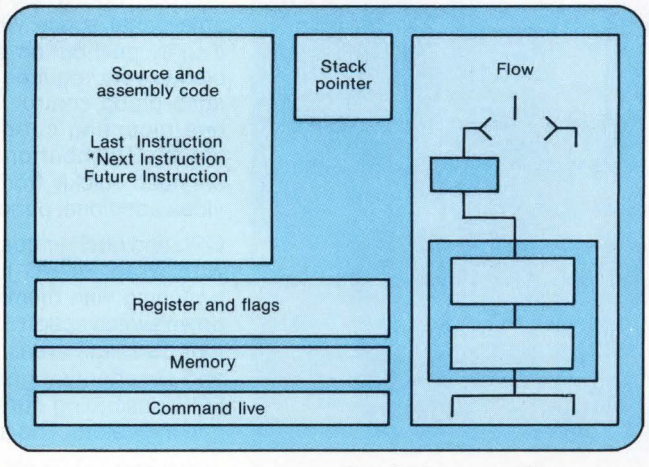
The simulator displays both the symbolic name and the numerical value for all instructions. Using on-line help, a programmer can review commands and procedures even while the program execution is being simulated. Program execution is simulated at approximately 1% of the speed of the 8048 processors.

The IBM PC must have a single disk and a minimum of 128 kbytes of RAM to run the SIM-8048. After software has been developed on the SIM-8048, the company's CYS-8049 cross-assembler compiles the actual program code for the 8048 microcontroller and then saves it in the form of a hexadecimal file.

The SIM-8048 program costs $395, and an evaluation disk and manual are available for $39.50. Delivery is from stock.

Cybernetic Micro Systems, PO Box 3000, San Gregorio, Calif. 94074; Ed Klingman, (415) 726-3000. **CIRCLE 310**

Dave Bursky



With the SIM-8048 program, six windows on the screen of an IBM PC show the full simulation of any processor in the 8048 family. Source code and assembly mnemonics appear in one window and an execution flow graph in another, for example.

SOFTWARE

Design tools run on PC-based workstation

Two computer-aided engineering programs, for use on the IBM PC-based CAD 1000 and CAD 2000 workstations, are well suited for system-level design, as well as pc board and semicustom IC design. Simulog is a nine-state, event-driven logic simulator with a set of 20 logic primitives. It permits the simulation of circuits using both TTL and MOS integrated circuit technologies. The Symgraph schematic capture system allows the user to enter logic designs as multiple-sheet schematic diagrams and extract a complete netlist, which can be used for simulation, as a verification of the accuracy of the physical layout, or as an interface with physical layout tools.

Simulog is priced at $2500 per copy, while Symgraph is an integral part of Chancellor's high-resolution color graphics subsystem.

Chancellor Computer Corp., 1101 San Antonio Road, Mountain View, Calif. 94043; (415) 969-5000.

CIRCLE 311

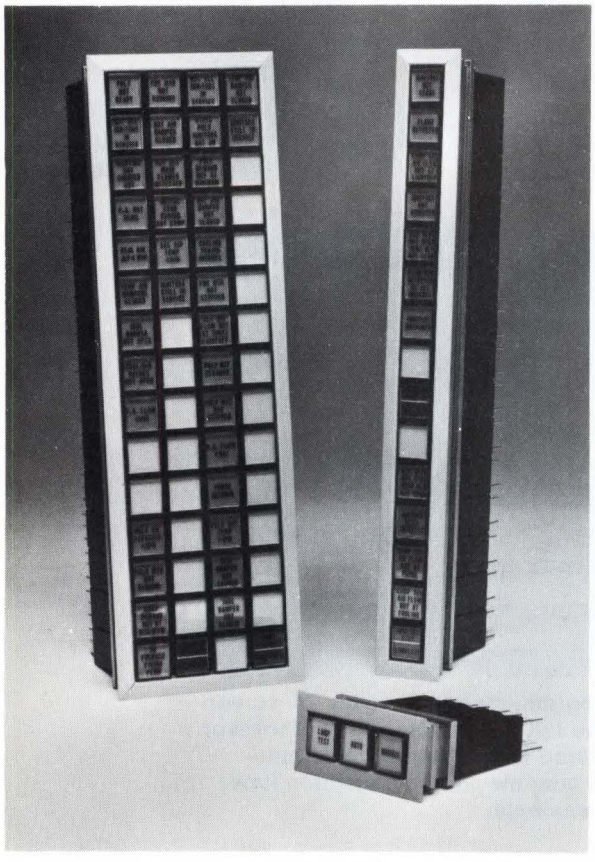
Binary object module supports 80186/80188

Beneficial to design engineers developing applications for the 80186, 80188, 8086, and 8088 microprocessors is a binary object module that converts symbolic object-module files from BSO format into Intel format. Currently, FMTCNV converts absolute BSO hex object modules into binary Intel-type object modules. Any of BSO's languages can be used in conjunction with the FMTCNV module.

FMTCNV operates in any VAX environment running under VMS. Generated object modules may be transmitted to the dedicated Intel emulator for the final hardware/software integration and PROM programming.

Boston Office Systems, 496 Moody St., Waltham, Mass. 02254; (617) 894-7800.

CIRCLE 312



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CIRCLE 150

SOFTWARE

Real-time executive works with NS16000

Compatible with all NS16000 family CPUs and development boards, the NS-EXEC operating system kernel monitors and controls, in real time, multiple external events that occur asynchronously. The ROMable executive performs task and event management, intertask communication, interrupt handling, memory-pool management, and timer management.

Written in NS16000 assembly language, the NS-EXEC executes faster and occupies less space than would be expected of an executive written in a high-level language. Requiring only 2 kbytes of RAM and 4 kbytes of ROM, the software executes at a speed of 50 μs, measured at the time of interrupt to first user-defined instruction. Up to 256 logical channels for task communication and up to 256 levels of task priority can be dynamically assigned.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $1000 (one-time source license fee).

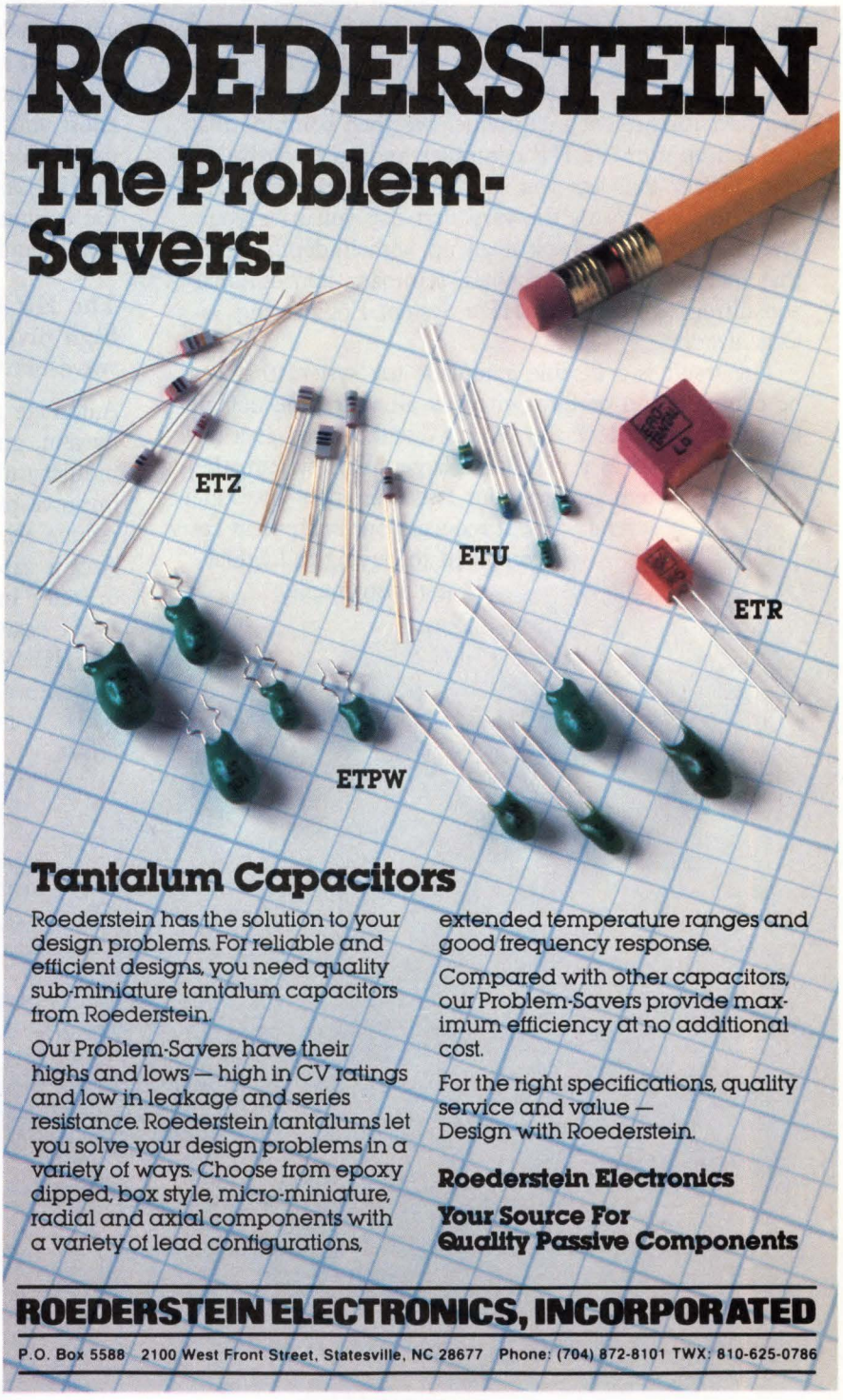
CIRCLE 313

Design tool aids IFL programming

An interactive software package aids in the functional-level programming of Signetics' proprietary IFL circuits. The menu-driven program, called AMAZE—Automatic Map and Zap Equation Entry—manipulates Boolean equations, truth tables, state diagrams, or flowcharts to create the binary fuse map that is needed to program the IFL devices. The AMAZE software operates on the VAX 11/780 computer under VMS.

Signetics Corp., 811 E. Arques Ave., Sunnyvale, Calif. 94086; (408) 739-7700. $100.

CIRCLE 314



CIRCLE 181

The HP 1980 Time Domain Measurement System...

Speed production throughput and by automating your time-domain

The HP 1980 System combines key test instruments with powerful computers, flexible software, and comprehensive support for a total test solution.

The modular HP 1980 Time Domain Measurement System integrates four essential test instruments — a fully programmable oscilloscope, a waveform digitizer, a universal counter, and analog comparators — into a single, compact instrument mainframe. We then combine that with an appropriate HP computer and an extensive software library that lets you start making measurements of many test waveforms the very first day you have your system. Finally, we back it all up with in-depth support that includes application notes, seminars, and optional consulting services from HP's System Engineering Organization.

The result is a flexible automatic test system that can be configured to perform virtually all your time domain measurements below 100 MHz. Whether used as a total test solution, or as a core for a larger ATE system, the HP 1980 System reduces your test equipment investment several ways. It reduces your equipment costs compared to buying individual test instruments.

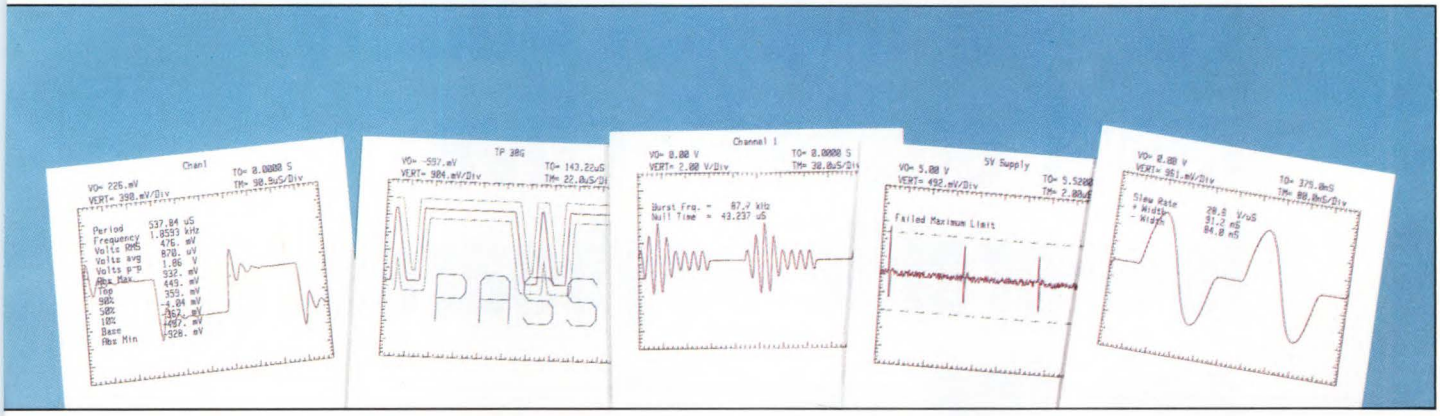
It eliminates or greatly reduces the time you spend in system integration effort and software development. And the HP 1980 reduces test equipment space requirements.

The HP 1980 System saves test time and assures high product quality through consistent waveform comparison and characterization.

Automate production measurements with the HP 1980 System, and tackle two of the biggest problems facing industry today...how to reduce manufacturing costs and improve product quality. This system can significantly reduce test time and increase production throughput. And it can virtually eliminate errors associated with operator interaction, interpretation, and fatigue.

For example, in waveform comparison measurements, the HP 1980 can quickly compare a waveform under test with a stored limit waveform and provide a pass/fail indication within seconds. It eliminates the problems of waveform positioning, parallax, and judgement so

improve product quality measurements.



you get consistently accurate results. Comparison measurements with the HP 1980 are orders of magnitude faster than manual testing. For example, parametric tolerance tests, such as comparing peak amplitude to preset limits, can be performed within several hundred milliseconds.

Waveform characterizations that used to be difficult and time consuming are now performed quickly and accurately with the HP 1980. For total waveform characterization, there's a first-day measurement program in the software library that automatically determines peak-to-peak voltage, frequency, period, pulse width, rise time, and fall time on repetitive signals. For specific applications, you can use the subprograms contained in the software library to determine the fundamental frequency or period of a waveform, count events, and, with the HP 1980's flexible gating capability, measure the time between bursts.

The HP 1980 Time Domain Measurement System. When you want a complete, low-cost waveform measurement solution that goes right to work.

Perhaps you've felt that ATE was out of reach. Then this is the system that can make low-cost automated test a reality.

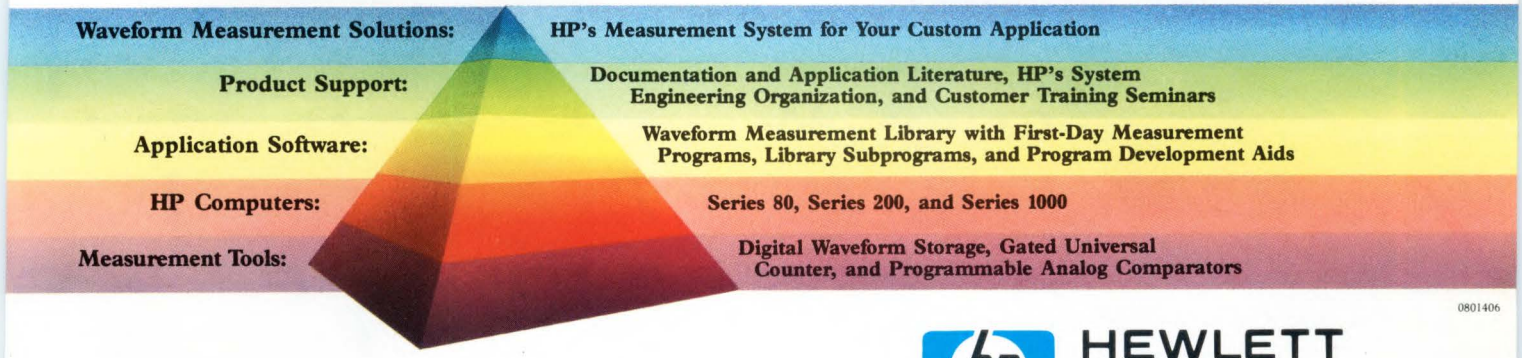
If you need a more sophisticated test system, now or in the future, the HP 1980 can be a powerful core system that you can easily expand via HP-IB. HP can even provide consulting assistance through our System Engineering Organization.

As you plan for the future, the HP 1980 will dovetail with your long-term networking objectives. As a part of HP's Manufacturing Productivity Network, the HP 1980 allows you to integrate production test data with information from other manufacturing operations. The ability of various departments to access a timely, accurate, integrated data base can have far-reaching impact on productivity, manufacturing costs and product quality.

Whether you're concerned with today's testing needs, tomorrow's manufacturing network, or both, the HP 1980 can make a valuable contribution toward improving your company's product quality and manufacturing productivity. To find out more, contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.



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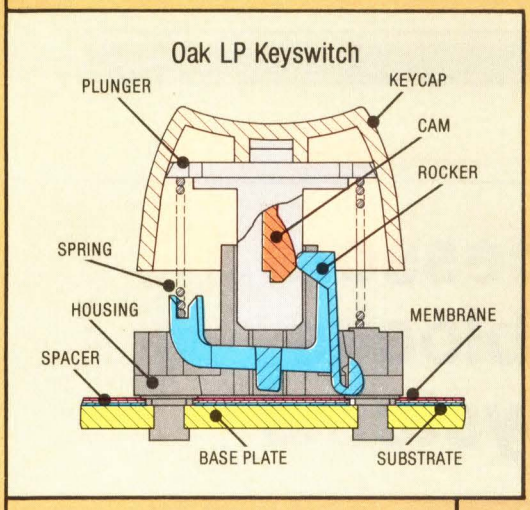
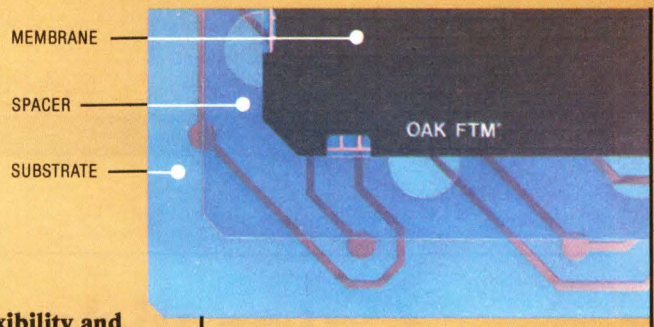
For engineering excellence . . . ask OAK





Introducing the low-profile, DIN compatible keyboard with the features you've been searching for — **Oak's Low-Profile FTM® Keyboard.** Designed especially for high speed data entry systems, where long life and operator comfort are paramount, Oak low-profile FTM keyboards feature a patented keyswitch design. Now, finally, you can specify the "feel" your customers want . . . from standard linear to fall-through tactile.

For design flexibility and savings . . . ask OAK

Simple design, coupled with advanced manufacturing, spells maximum design flexibility and savings for you. Oak keycaps are made of durable, lightweight, non-glare polyester and feature a comfortable cylindrical industry standard design. Sublimation printing provides for a wide variety of printing options — quadrant printing, multicolors, front legending, and custom legends — order whatever you need. And, there are a host of available options to fill most any special design requirement — LED indicators, EMI/RFI/ESD shielding, standard or custom encoding electronics, variable operating forces and more!

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Oak is the recognized leader in full travel membrane technology, a technology that provides proven performance features, benefits and cost savings not available with other keyboard designs ● high reliability ● long life of 50 million cycles ● elimination of double-sided, plated-through hole printed circuit boards ● environmental protection by design ● light weight . . . just a few of the many features designed to help enhance the performance of your product.

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Oak remains dedicated to staying in the forefront of keyboard technology. To providing a superior quality product, in the quantities you need, on time, at the right price. **To see how the new Low-Profile FTM Keyboard can go to work for you . . . ask OAK.**

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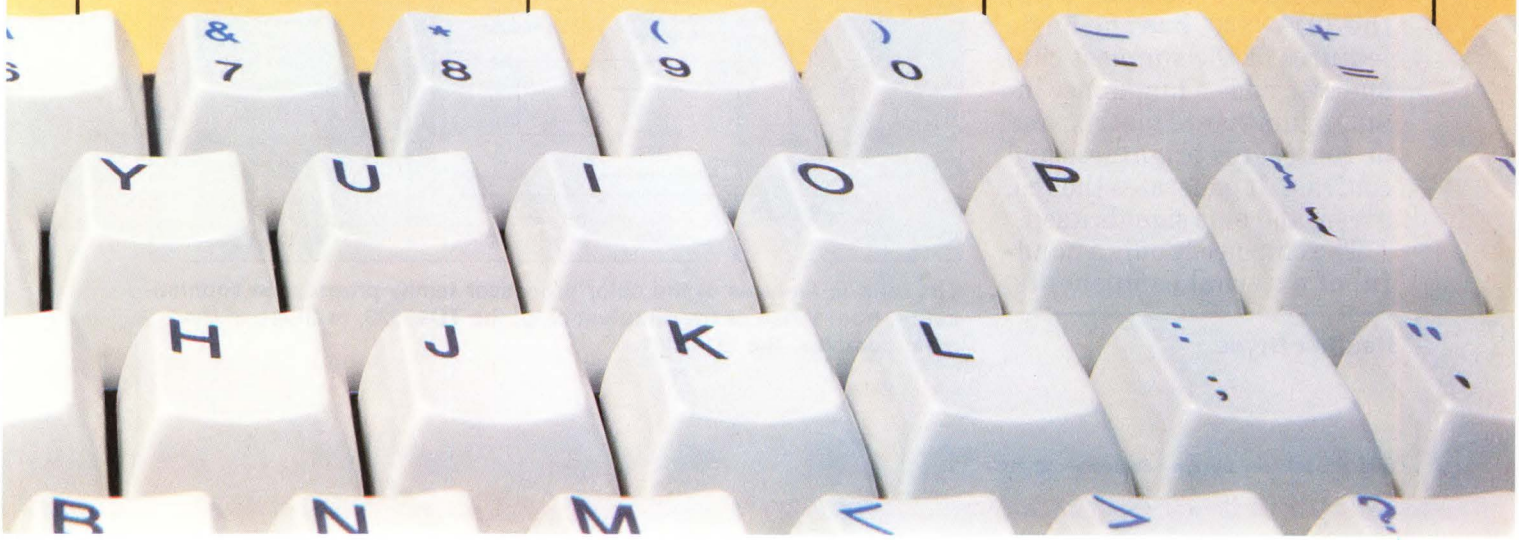
CIRCLE 183



Color video processors act as building blocks for PAL, NTSC systems

A series of three color processor chips from Motorola accept either European PAL or United States NTSC composite video signals and generate the appropriate signals for a TV receiver or a monitor.

The chips all are based on a color-difference demodulator, the TDA3333, which blends three functions on one chip (see the figure). It targets video systems that can supply their own luminance and green signals (Y and G) but that need a separate circuit to generate the R−Y (red minus luminance) and B−Y (blue minus luminance) signals. When the chip is used with a tube that reverses the matrix of signals, no additional circuits are required to deliver the full red, green, blue, and luminance signals.

The next processor chip, the TDA3330, has the basic features of the simplest chip and also adds a luminance input, a luminance matrix, and dc control for brightness and contrast. It generates the red, green, and blue signals itself.

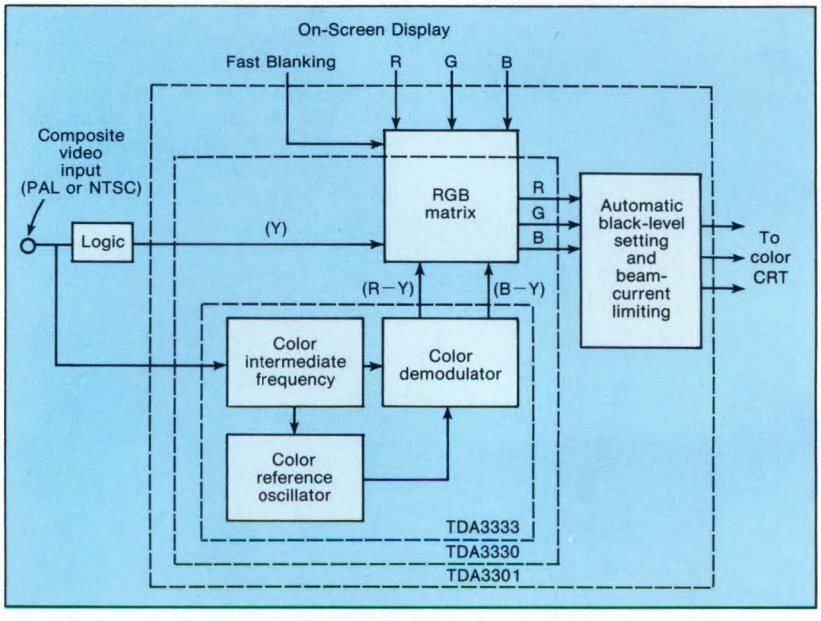
The chip needs only a handful of external components, including an inexpensive 4.43- or 3.58-MHz crystal, a delay line, a chroma bandpass filter, and one 12-V supply. With this chip, a separate driver acts as the interface with the picture tube.

At the top of the line is the TDA3301, which not only generates all the RGB signals but also accepts an On-Screen Display signal from a character or graphics generator.

The high-end chip also can automatically sense the beam level and set up RGB levels for true black, thereby eliminating the need for manual adjustments.

In quantities of 100 to 999, the basic TDA3333 sells for $2.12 each, the intermediate TDA3330 sells for $3.08, and the most sophisticated TDA3301 goes for $5.14. Delivery is from stock.

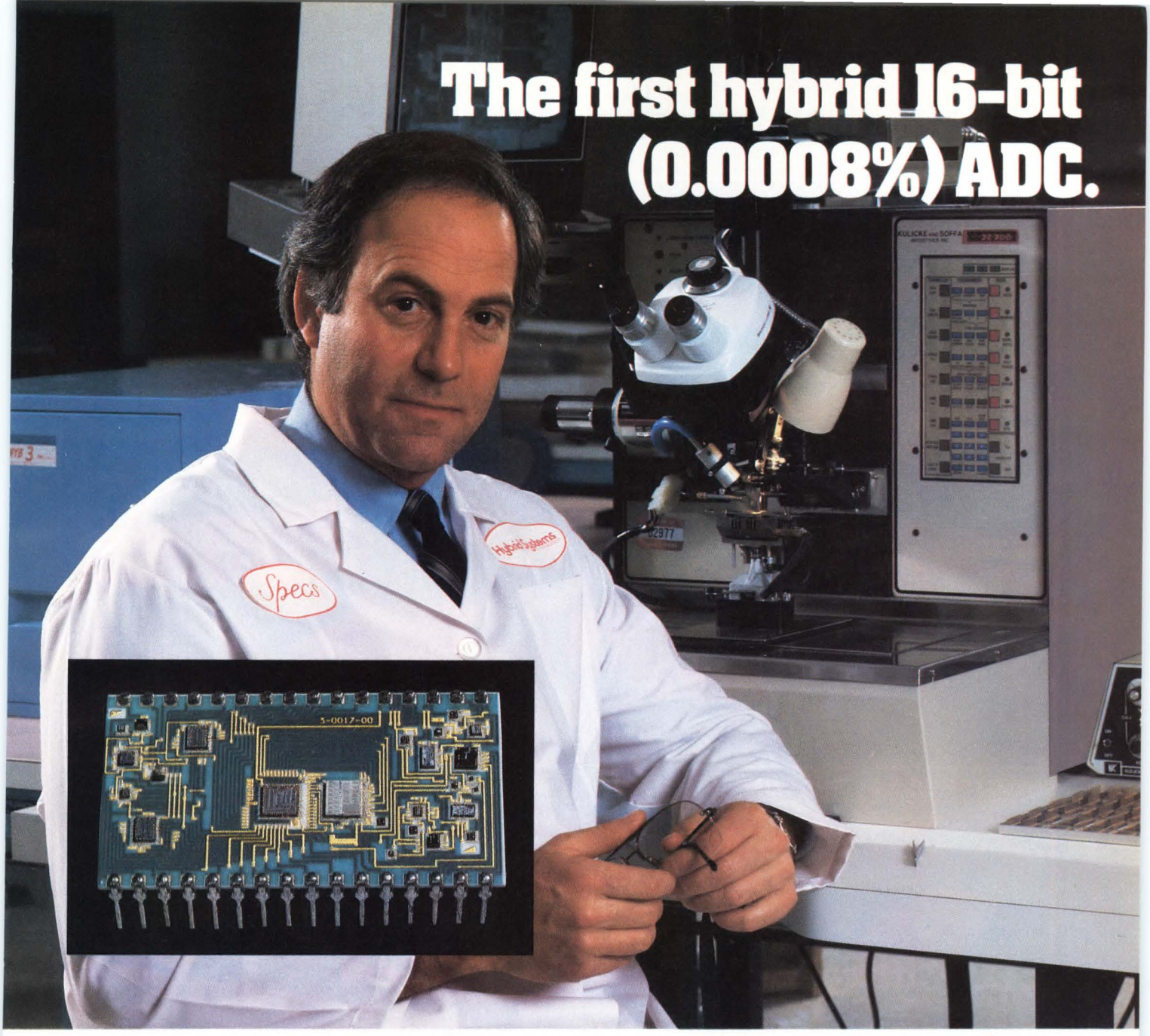
Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 897-3874. **CIRCLE 304**



The built-in features of the color processor family progress in sophistication from those of the simplest chip, the TDA3333, to those of the most complex, the TDA3301.

Heather Bryce

The first hybrid 16-bit (0.0008%) ADC.



"To get accuracy that good, you have to be committed to excellence."

"My name is Bob Spector. Because I'm a fanatic about component performance, my friends here at Hybrid Systems call me 'Specs.'

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"Take the HS 9516-6, for example. We have created the industry's first ADC with true 16-bit (0.0008%) linearity.

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"I don't mind being called 'Specs,' because I help Hybrid deliver the features and performance you need in your design. And the reliability, too. That's why we're the leader in precision data converters, hybrid data acquisition systems, and thin-film products.

"So you can call me 'Specs.' Or better yet, just call me. Hybrid's here to help."

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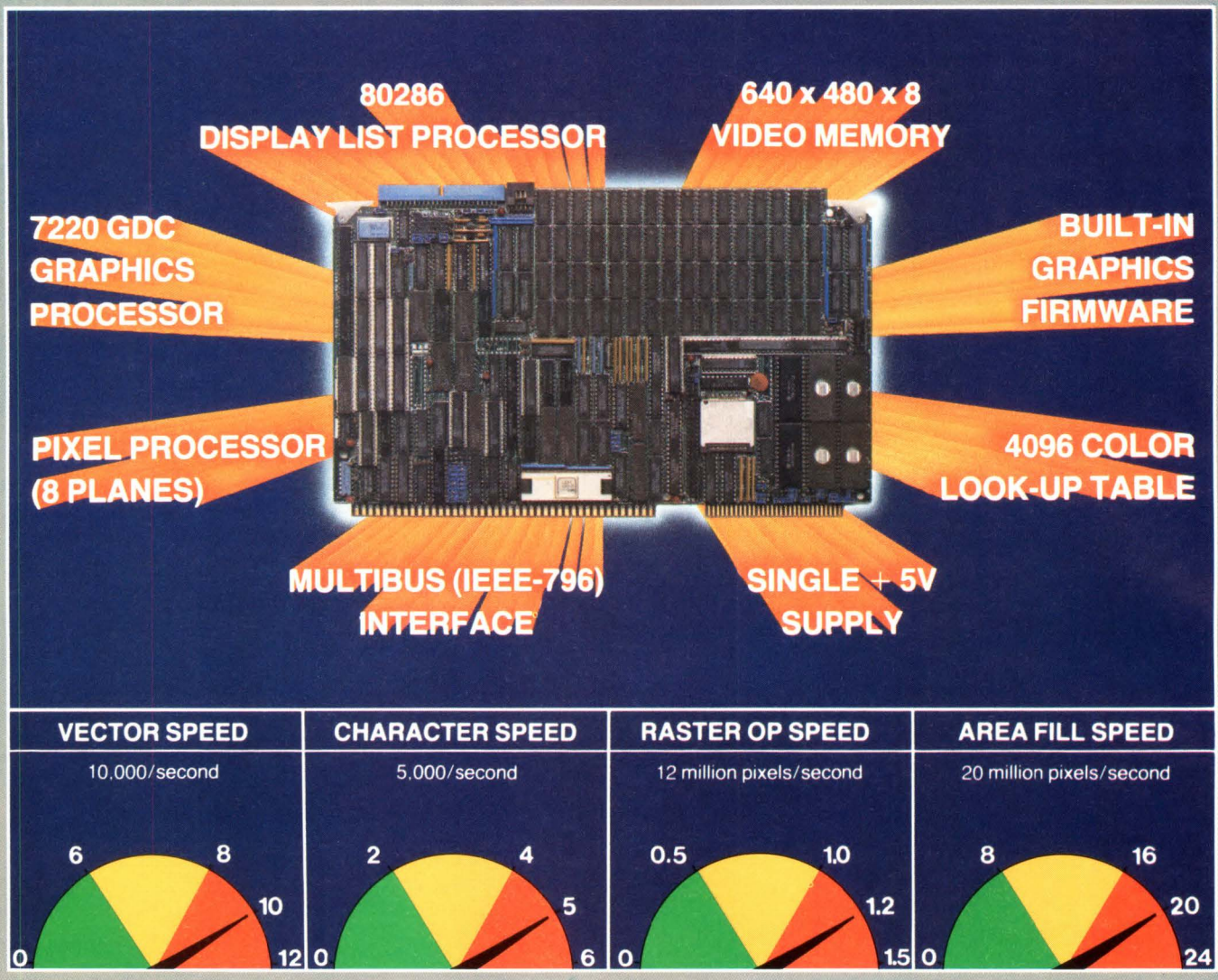
Hybrid Systems CORPORATION

Precision Data Converters, Hybrid Data Acquisition Systems, and Thin-Film Products.

CIRCLE 184

BREAKTHROUGH IN MULTIBUS GRAPHICS!



SX-900 - The New Performance Standard For Color Graphics Boards

- **Powerful on-board graphics firmware**
- **640 x 480 x 8 bits/pixel**
- **50/60Hz non-interlaced refresh**
- **4096 color look-up table**
- **80286 display list processor**
- **7220 GDC graphics primitive processor**
- **8 plane pixel processor**
- **Built-in diagnostics**
- **Complete IEEE-796 (Multibus) interface**
- **+5V only power required**
- **10,000 vectors/second**
- **5,000 characters/second**
- **1,200,000 pixels/second raster ops**
- **20,000,000 pixels/second area fill**

The new Matrox SX-900 is a high performance color graphics display controller. It is the perfect solution for OEM manufacturers of process control and instrumentation equipment. The SX-900 is software compatible with the popular Matrox GXB-1000A high resolution display controllers, but occupies only a single Multibus card slot, and provides high speed drawing capability.

The hardware provides 640 x 480 pixel resolution, 4 or 8 bit planes, a 4096 color look-up table, and a 60Hz flicker free video refresh rate. The fast performance of the SX-900 results from a multi-processor pipelined architecture. A powerful 80286 CPU is used as the front end display list processor and is supported by a 7220 graphics primitive processor and a high speed pixel processor for simultaneous 8 plane drawing.

The SX-900 incorporates the proven on-board graphics firmware used by the GXB-1000. Over 256 high level display list commands are supported including line drawing, character drawing, circle and arc drawing, area fills, cursors and raster ops.

In addition to graphics boards, Matrox can also supply color monitors, cardcages, CPU cards, memory boards, and communications controllers for complete OEM display system requirements.

80286, MULTIBUS - TM INTEL • 7220 - TM NEC

Call now for a complete documentation package.

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CIRCLE 185

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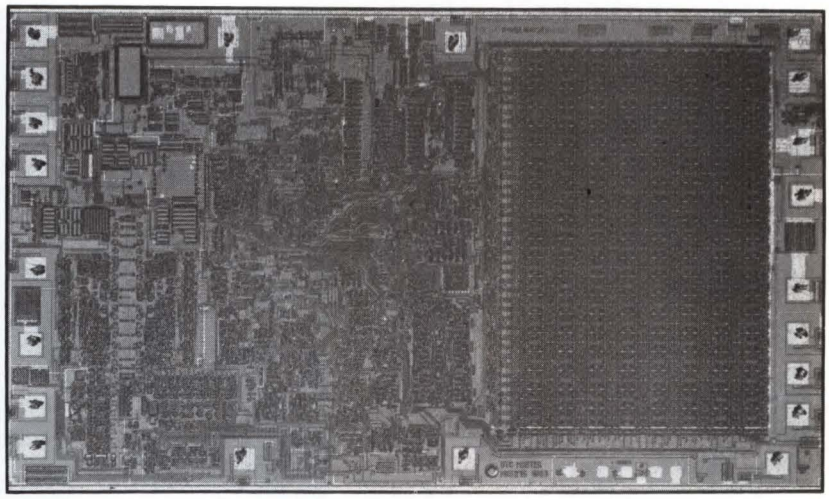
DIGITAL ICs

Repertory dialer chip controls tones and pulses



A CMOS 10-number repertory dialer is the first single chip to handle both tones and pulses, simplifying the design for PBX or long-distance systems that require both dial pulsing and DTMF signals.

The MK5375 tone-pulse dialer from Mostek stores ten 16-digit telephone numbers. An individual may dial any of the numbers with a single keystroke. A memory lock protects these numbers from inadvertently being cleared before desired.

The last number dialed on the system can be redialed with a single keystroke. Alternatively, the buffer that holds that number can be cleared to prevent it from being redialed. Clearing the last number dialed does not affect the other stored numbers.

Rapid keystrokes fill a FIFO register, allowing up to 25 key entries per second, without loss of data. The output signaling rate is determined by external components; the dialer customizes itself to any system.

A keypad interface connects directly to either a calculator-type keypad or the standard telephone keypad. A key entry is considered valid when either a single column or a logic 0 is applied to both a single row and column.

Debouncing circuitry protects against invalid readings. If both row and column information is valid, the information enters the last-number-dialed buffer.

The 18-pin plastic MK5375 costs $6.35 in quantities of 1000 and is available from stock.

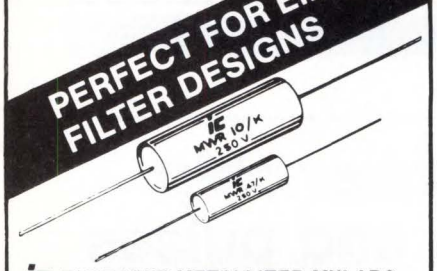
Mostek Corp., 1215 West Crosby Road, Carrollton, Texas 75006; (214) 466-6000.

CIRCLE 306

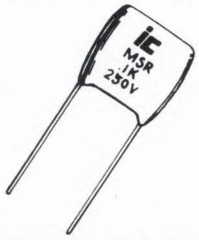
Heather Bryce

"AVAILABILITY" DEPENDABLE

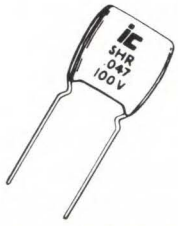
PERFECT FOR EMI-RFI FILTER DESIGNS



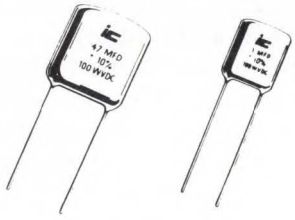
TYPE MWR METALLIZED MYLAR® POLYESTER FILM CAPACITORS
WRAP & FILLED CONSTRUCTION
NON-INDUCTIVE WINDING, +125°C.
SELF HEALING DESIGN
100 WVDC to 1,000 WVDC
0.01 Mfd. to 22 Mfd.
TOLERANCE: ±10% (±5% Opt.)



TYPE MSR METALLIZED MYLAR® POLYESTER FILM CAPACITORS
NON-INDUCTIVE WINDING, +125°C.
SELF HEALING, EPOXY DIP
250 WVDC to 1,000 WVDC
0.01 Mfd. to 10 Mfd.
TOLERANCE: ±10% (±5% Opt.)



TYPE SHR EXTENDED FOIL POLYESTER FILM CAPACITORS
NON-INDUCTIVE WINDING, +125°C.
100 WVDC
0.001 Mfd. to .47 Mfd.
TOLERANCE: ±10% (±5% Opt.)



TYPE UMR POLYESTER FILM CAPACITORS
EPOXY DIP, +85°C
100 WVDC
.001 Mfd. to .47 Mfd.
TOLERANCE: ±10% (±5% Opt.)

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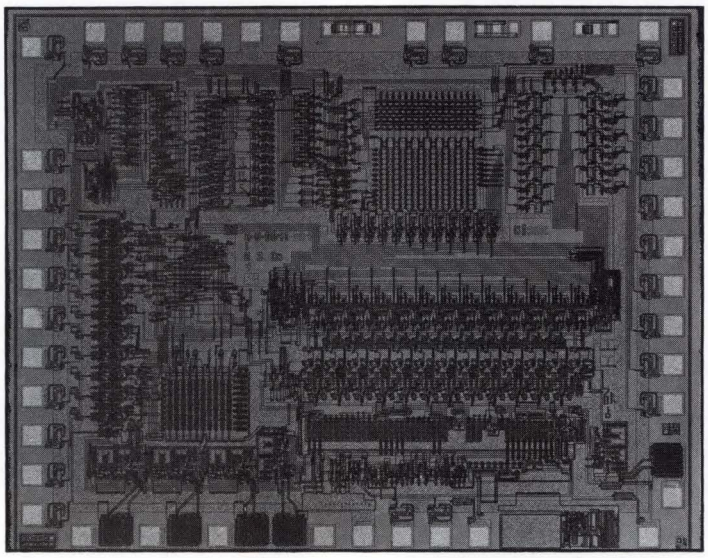
CIRCLE 186

DIGITAL ICs

Video-attributes chip emulates VT220, VT100



For the first time, the attributes of Digital Equipment's VT220 and VT100 terminals can be bestowed on a video control subsystem with the simple addition of one chip, Standard Microsystems' CRT 9041.

An enhanced version of the earlier CRT 9021, the attributes controller can operate at frequencies ranging from 28.5 to 33 MHz, speeds fast enough for displaying 132 characters per row. The chip controls reverse video, two underlines, character blanking and blinking, four intensity levels, and two cursors. When used with the company's CRT 9007 video controller chip, it can produce double-height and double-width characters.

The controller permits the video system to use external character-generation memory. It sits between the memory and the monitor, converting the parallel font data into serial video data and adding the graphics attributes to the serial data stream.

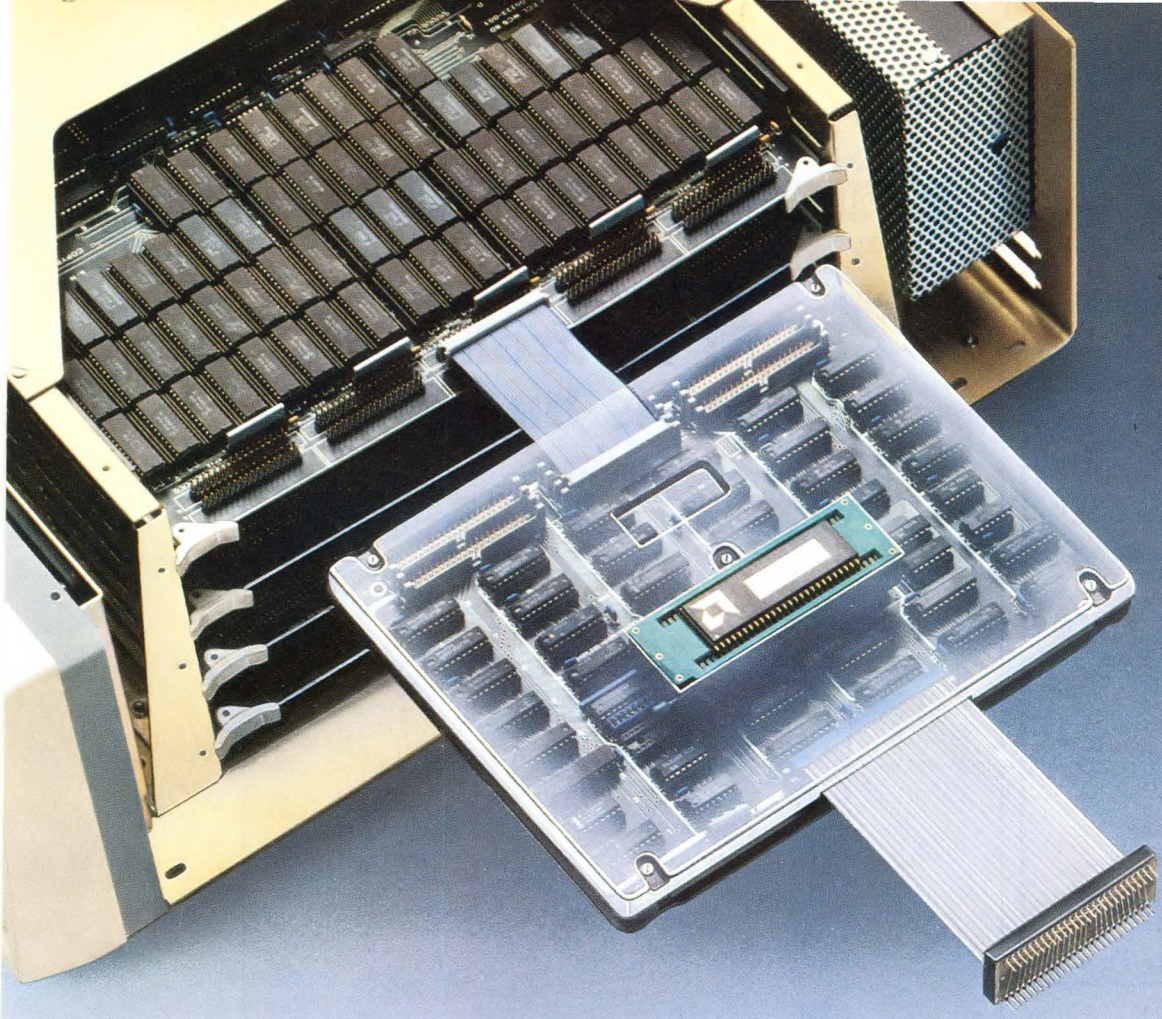
The chip works in two graphics modes. For wide graphics, it displays up to 256 symbols, each the size of a character block. When the chip enters the thin graphics mode, it creates thin-line drawings and forms.

The chip consumes about 500 mW with a 5-V supply and comes in a plastic or ceramic 40-pin DIP. The 28.5-MHz plastic version costs $15.25 in 100-unit quantities.

Standard Microsystems Corp., 35 Marcus Blvd, Hauppauge, N.Y. 11788; (516) 273-3100

Dave Bursky

CIRCLE 301



STEP-27 SERIES

Bit-Slice Microprogramming ROM-Simulation Support

29116 & 2910 Emulation? Only from STEP!

Since STEP Engineering has always been a "Step Ahead" in quality high-speed processor development support, it's only natural to be the first with these emulators. The STEP-27, a complete development station, includes the following:

Disassembler? The First For the Microprogrammer! No need to convert ones and zeros into mnemonics. Poly-Meta-Symbolics (PMS)™ does it for you. It even enters your patches symbolically.

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Software? The Best! In addition to full software support for either a local or a remote host, STEP provides a general-purpose meta-assembler.

Poly-Meta-Symbolics (PMS) is a trademark of STEP Engineering.

CIRCLE 187

Writable Control Store (WCS)? The Fastest! STEP's ten nanosecond WCS provides real-time execution of the most demanding high-speed designs. With any number of arrays (each up to 512-bits wide by 64K deep), the STEP-27 supports the largest micro-program requirements.

Communications? Of course! Using an RS232 linkup, the STEP-27, with a unique, general-purpose, menu-driven communication program, easily interfaces with the IBM® PC, VAX®, PDP-11® or CP/M®-based and other operating systems.

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CIRCLE 240

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CITY_____STATE_____ZIP_____

18-84

3. Mail to:
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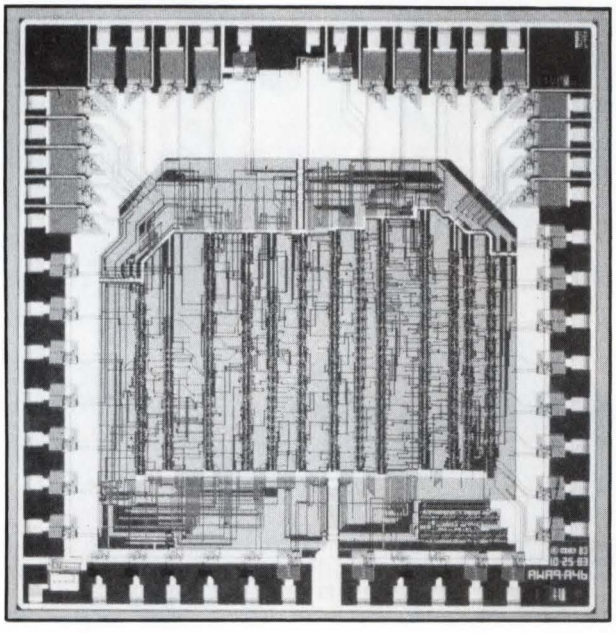
DIGITAL ICs

SCSI controller chip contains bus drivers



A single-chip controller from NCR not only has the intelligence to decode SCSI (Small Computer Systems Interface) commands for peripheral devices, but also comes with high-current bus drivers. Sinking 48 mA at 0.5 V, the drivers simplify the interface for a controller board that is located at a distance from the host, by allowing direct connection to the SCSI bus.

The NCR 5380 fully meets the latest ANSC X3T9.2 draft specifications, yet remains versatile for older SCSI designs. Essentially an enhanced version of the first SCSI controller (the NCR 5385), it is itself one of the first disk controllers dedicated to the SCSI bus.

The 5380 offloads many peripheral control functions from the host computer by disconnecting itself from the host during disk seeks and reconnecting only when ready for DMA transfer—a basic part of the SCSI specification.

DMA transfers can be initiated by writing to one of the chip's three registers (the other two identify senders and receivers); transfers take place at 1.5 Mbytes/s.

In small quantities, the controller is $40 per device. Production quantities will be ready in January.

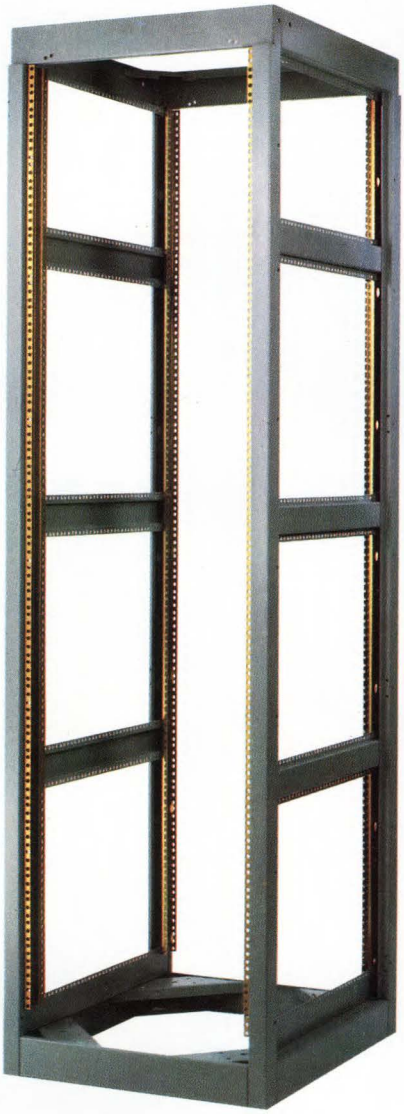
NCR Corp., Microelectronics Division, 1635 Aeroplaza Drive, Colorado Springs, Colo. 80916; Harold Mason, (303) 569-6512.

Stephan Ohr

CIRCLE 302

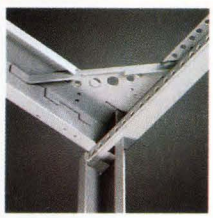
How To Select Enclosures

For Strength and Structural Integrity



AMCO presents a guide for comparing structural features of modular electronic consoles.

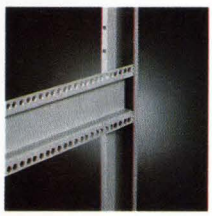
Enclosures are selected for both superior aesthetic quality and structural function. While AMCO offers the most comprehensive styling selection program for enclosures, ***at the heart of the AMCO system is the carefully designed FX Series frame.*** *A closer look at the construction detail reveals AMCO's method of achieving a very high strength-to-weight ratio. Use the following key features as a guide for comparison with any other manufacturer's enclosure. Take the AMCO challenge: can you find an enclosure superior to the AMCO FX Series for structural integrity?*



Cross Sections

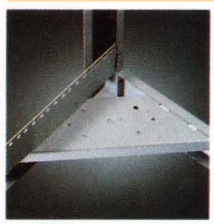
- *Side channel, top of frame*
- *Front channel, top of frame*

Four separate 14 ga. channels, each with three forms (bends), provide a rugged top frame assembly. Seam (heliarc) welded top corners are reinforced by formed 12 ga. gusseting. Gussets also serve as built-in receptacles for lift-eye mounts.



- *Vertical frame channel*
- *Horizontal side strut*

14 ga. vertical and side strut channels, each containing four forms, are interlocked and welded to dual return flanges.



- *Front channel, frame base*
- *Side channel, frame base*

Frame base channels are interlocked and heliarc seam welded to the main vertical channels. Formed 12 ga. gussets reinforce frame base corners and also serve as caster mounts or, after inverting (on request), direct floor mounts.

Extreme Test Demonstrates 10.7:1 strength-to-weight ratio.

AMCO frames have been built to satisfy the most stringent military shock and vibration standards. In Mil Spec testing, AMCO's FX78-19-22 frame (112 lbs. with mtg. channels) passed the following tests while carrying a load of 1200 lbs., demonstrating a strength-to-weight ratio of 10.7:1.

Vibration	*20 minute duration for each cycle.*	
	1-7 cycles—no resonance.	*PASSED*
	7-15 minimal resonance.	*PASSED*
	No cracks or fractures.	*PASSED*
Shock	*Air Force 16G sand drop—3 consecutive drops in all planes except upside down. Distortion allowed, but no breaks, cracks or fractures. Equipment must be functional after test.*	*PASSED*

Details and support documentation available on request for the above, as well as other structural tests.

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AMCO Engineering Co.
3801 N. Rose St.
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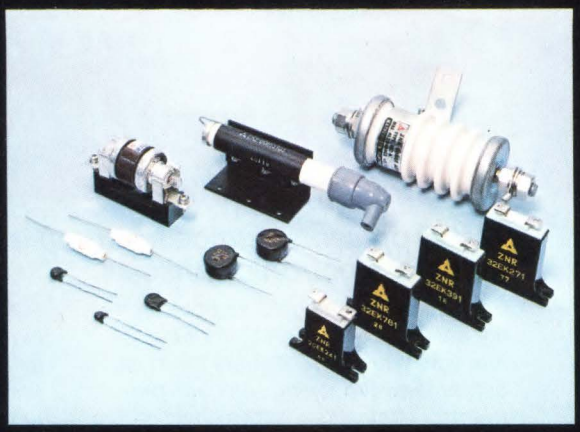
Fight the protection racket.

Why pay for back-to-back zeners to get positive/negative protection, when a single Panasonic ZNR can provide complete, highly reliable circuit protection in either direction... and for less cost.

These zinc oxide nonlinear resistors also provide an excellent alternative to RC circuits and spark gaps. Their ohmic values change in less than 50 nsec when subjected to impulse surges, so their response time is fast...without the discharge lag conventional gap-type arrestors can't avoid.



Result: you can use them for ground fault interrupter circuits or input line transient protection. Use them in applications ranging from low-voltage switchboards and communications equipment to video displays and TVs. Use them anywhere you want an economical, efficient way to protect vulnerable AC and DC circuits against repeated high voltage transients (positive or negative), or such steep-rise surges as those caused by lightning, switching or noise spikes.

Providing excellent temperature and humidity characteristics, ZNR's are available in a wide varistor voltage range—from 22 V to 1800 V in the PC-mountable D Series and the top-connected, flange-mounted E Series, and in stacked types for voltages up to 26 KV. Surge withstand capabilities are from 50 to 2,000 amps in the D Series, or 2,500 to 20,000 in the E. Our D series includes several UL recognized numbers for line voltage applications. For complete details, samples and prices, write or call: Panasonic Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5256.

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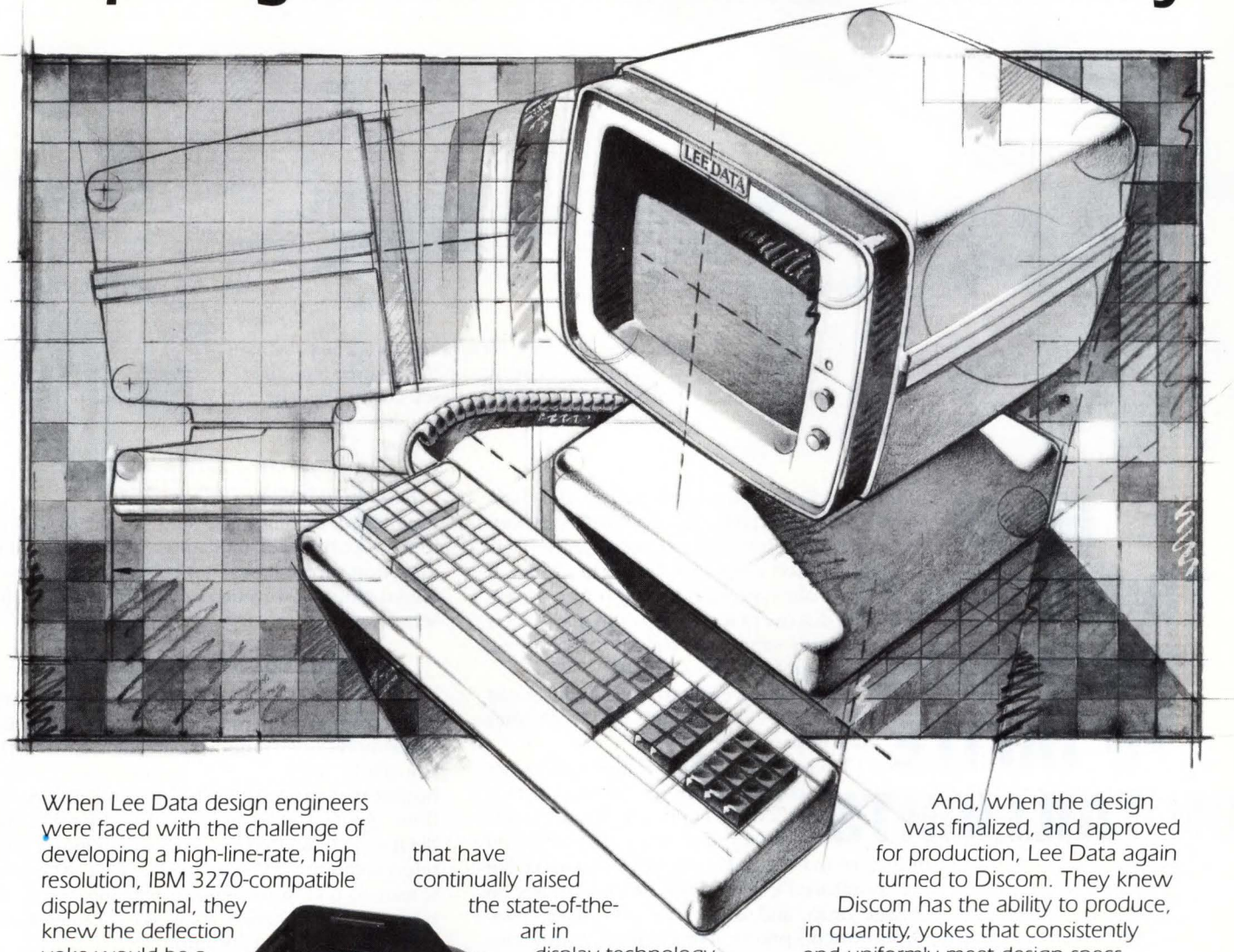
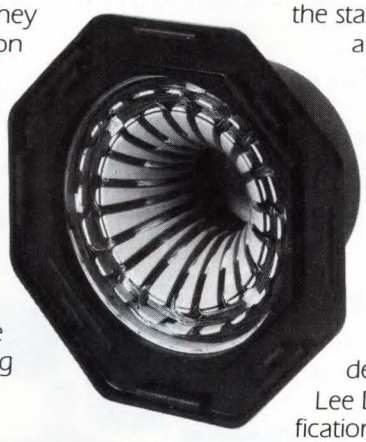
CIRCLE 190

THE CHALLENGE:

Develop a volume production yoke with geometry tolerance of less than 1% requiring no recorrection after assembly.



When Lee Data design engineers were faced with the challenge of developing a high-line-rate, high resolution, IBM 3270-compatible display terminal, they knew the deflection yoke would be a key component. They would require a yoke with geometry tolerance of less than 1% in production quantities. A yoke that would not require recorrection during final assembly in their plant.



So they turned to Discom. Taking advantage of Discom's thirteen-plus years developing components that have continually raised the state-of-the-art in display technology, Lee Data engineers were able to realize their objectives.

Using Discom's patented non-uniform conductor distribution process, Discom engineers developed a specially designed yoke to meet Lee Data's exacting specifications. Then Discom's full-capability prototype lab built prototypes for testing and evaluation.

And, when the design was finalized, and approved for production, Lee Data again turned to Discom. They knew Discom has the ability to produce, in quantity, yokes that consistently and uniformly meet design specs.

In VDT applications, as well as avionics and large-screen graphics, Discom is helping the world's largest electronics manufacturers meet their design challenges. And often saving them time and money in the process. Circle the number below on the reader response card, or call (617) 692-6000 and challenge Discom.

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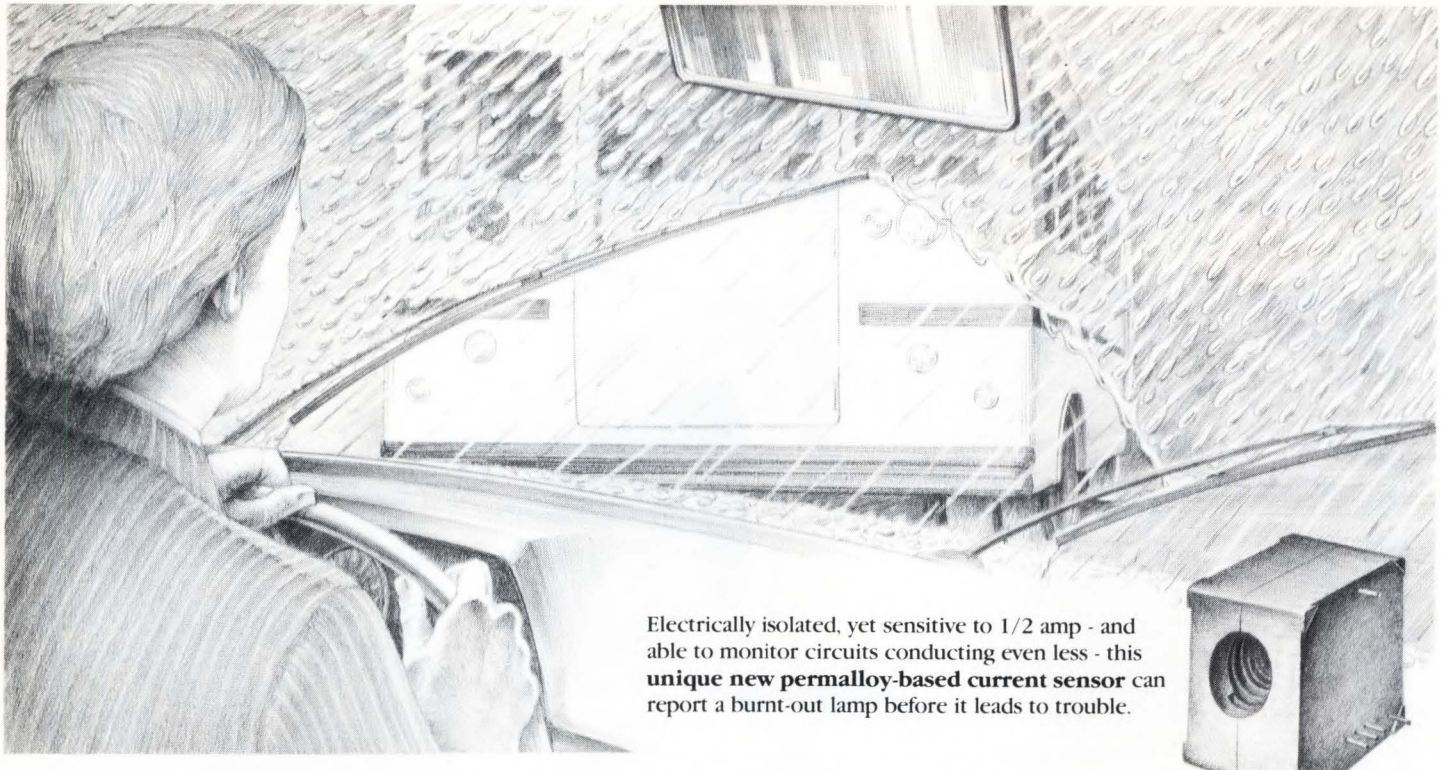
4th in a series from The Sensor Consultants



Electrically isolated, yet sensitive to 1/2 amp - and able to monitor circuits conducting even less - this **unique new permalloy-based current sensor** can report a burnt-out lamp before it leads to trouble.

HOW TO MOTIVATE MILLIAMPS TO TATTLE ON TAILLIGHTS.

Your car's suspension stabilizes, but your heart is still revved into the red. Thanks to poor visibility and a failed taillight, you've nearly backended a slow-moving school bus. It makes you wonder how often drivers discover electrical problems — their own or someone else's — by accident. This time, everyone's lucky.

But discovering that a light is out needn't be left to luck, or to another motorist.

There's a dependable new solid state current monitor that can detect electrical faults and failures in any number of settings. It operates on milliamps in DC or AC circuit(s). Isolated from the monitored circuits, this sensor causes no voltage drop, and is immune to voltage transients. And it's practical in all kinds of situations where you want to know if current is or isn't flowing.

Wired to an indicator, it can signal burnt-out lamps, a discharging battery, or a useless heater coil in a pilot's airspeed indicator system. As a factory outpost sentry, it alerts you to the status of remote motors or relays.

Examine this new sensor closely.

Nothing else lets you detect 1/2 amp so efficiently without invading the conductor. Use of the magnetically super-sensitive nickel-iron alloy, permalloy, boosts sensitivity 10x or more beyond that of other electrically isolated sensors of comparable size. It allows you to tap a lower level signal reliably, and without sacrificing space or convenience.

Thin-film deposit of the permalloy on a bipolar IC silicon chip combines the milliamp sensitivity with voltage regulation and temperature compensation. That makes this sensor unique and complete, ready to use.

Pass the conductor to be monitored through the sensor one or more times. Five hundred milliamps, flowing in either direction through the flux collector, triggers a digital output. Overcurrent will not damage the sensor.

Examine your options fully.

At MICRO SWITCH, the current sensors range from low-current, digital output devices that simply detect whether current is flowing, to adjustable, high-current sensors with linear output that varies with the amount of current flow. Special designs include low-milliamp devices to detect power drain in computer and telecommunication circuits. And we can tailor a sensor to give you a special housing, termination, or signal conditioning. We'd rather have you customize than compromise.

For more information about current sensors, use the reader service card to contact us. If you'd like to discuss your application, or are interested in pressure, position, airflow, or temperature sensors, phone us at 815-235-6600; or write MICRO SWITCH, The Sensor Consultants, Freeport, IL 61032.

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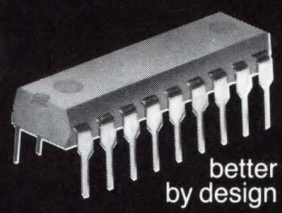
CIRCLE 192

Fast! 9μs μP Compatible 8 Bit A/D Converters



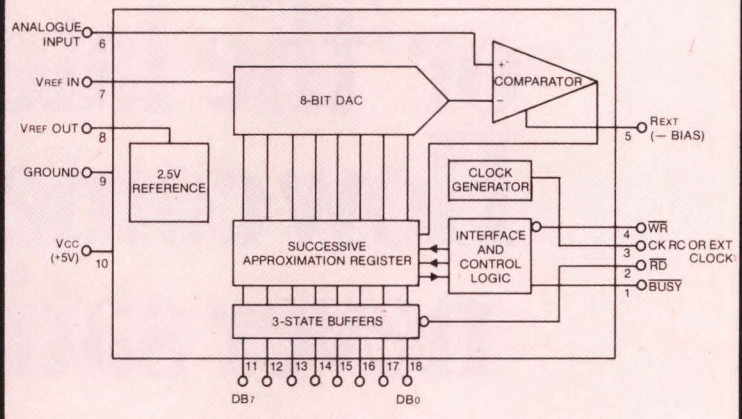
better by design

The Ferranti Models ZN447, ZN448 and ZN449 9μs Monolithic A/D Converters offer 8 bit resolution and microprocessor compatability with a minimum of support components.

Features:

- Tri-state buffers and interface logic for μP compatability.
- Available with ¼, ½ and 1 LSB linearity ratings.
- On-chip clock, comparator and 50PPM reference.
- Bipolar or unipolar operation.
- Continuous conversion mode operation.
- Can be operated from a single +5V source.
- Commercial and military temperature ranges available.

FUNCTION DIAGRAM



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CIRCLE 193

NEW PRODUCTS

DIGITAL ICs

CMOS chip drives dichroic LCDs

The industry's first driver for dichroic liquid-crystal displays is capable of supplying 30 V, as compared with the 3 to 15 V used for conventional twisted-nematic displays. Designated the S4520, the CMOS chip permits users to take advantage of the wider viewing angles (up to 180°) and high color contrast offered by dichroic LCDs.

Operating from a logic supply voltage of 3 to 16 V and a display supply voltage that can be as low as −29 V, the S4520 provides an output swing of up to 32 V. What's more, the chip draws as little as 400 μA.

Gould AMI Semiconductors, 3800 Homestead Road, Santa Clara, Calif. 95051; (408) 246-0330. $12.60 (plastic), $22.85 (ceramic) (1000 units). **CIRCLE 314**

Array densities span 380 to 4205 gates

A family of CMOS gate array devices ranges in density from 380 to 4205 gates and provides up to 77 functional logic blocks for the user to implement his logic. The MSM60000 and MSM70000 series are 3-μm silicon-gate devices with dual-layer metal for interconnection. Both series feature two-input NAND-gate propagation delays of 3 ns and have TTL- and CMOS-compatible inputs and outputs. The gate arrays offer a voltage range of 3 to 6 V, a toggle frequency of 50 MHz, and an operating temperature range of −40° to +85°C.

The devices are available in dual-in-line packages, plastic flat packs, pin-grid arrays, and plastic leaded chip carriers. Oki is manufacturing packages that have as many as 132 pins.

Oki Semiconductor, 650 N. Mary Ave., Sunnyvale, Calif. 94086; (408) 720-1900.

CIRCLE 315

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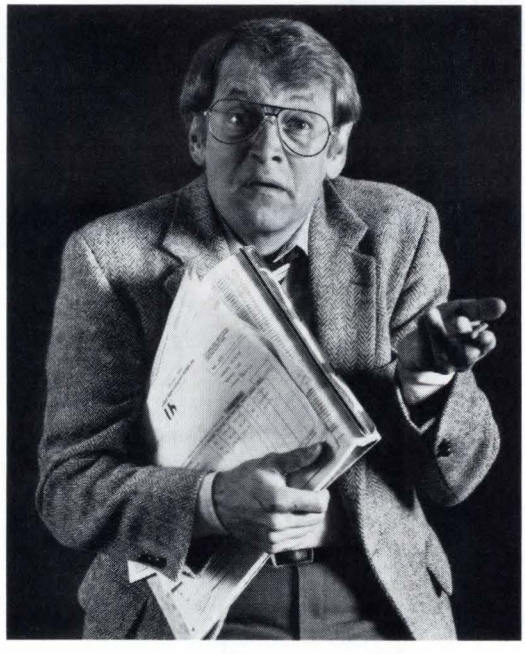

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Sight for Sore Eyes

Hitachi helps you reduce user eye fatigue by producing monochrome and color display tubes that excel in resolution, contrast, brightness and clarity. Tubes that your customers will love at first sight, because they are the result of these human-oriented breakthroughs in CRT technology:

Fine-patterned phosphor screens

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Reduction of glare

Screen glare is a leading cause of user discomfort, so we came up with special treatments that cut glare to a minimum. Available on models of all sizes, one is our "direct-etching antiglare face." Spray coating and multilayer coating can also be applied to reduce reflection.

Less flicker, higher contrast

Hitachi offers long-persistence phosphors for both monochrome and color screens to cut down irritating flicker. Numerous phosphor tones allow users to specify their own monochrome display colors; color tubes can be supplied with the traditional R-G-B combination or a new R-G-Light Blue. And lower-transmission glass, ranging from clear to grey to dark tint, can help improve contrast according to your requirements.

We believe people deserve to be pampered, and we've committed our engineering skills to just that. Manufacturing each and every product with the end-user in mind. Supplying you with components that exceed expectations. So give your own eyes a treat. Look up your nearest Hitachi representative for a personal view of our complete CRT line-up.

HITACHI

CIRCLE 195

For more information:

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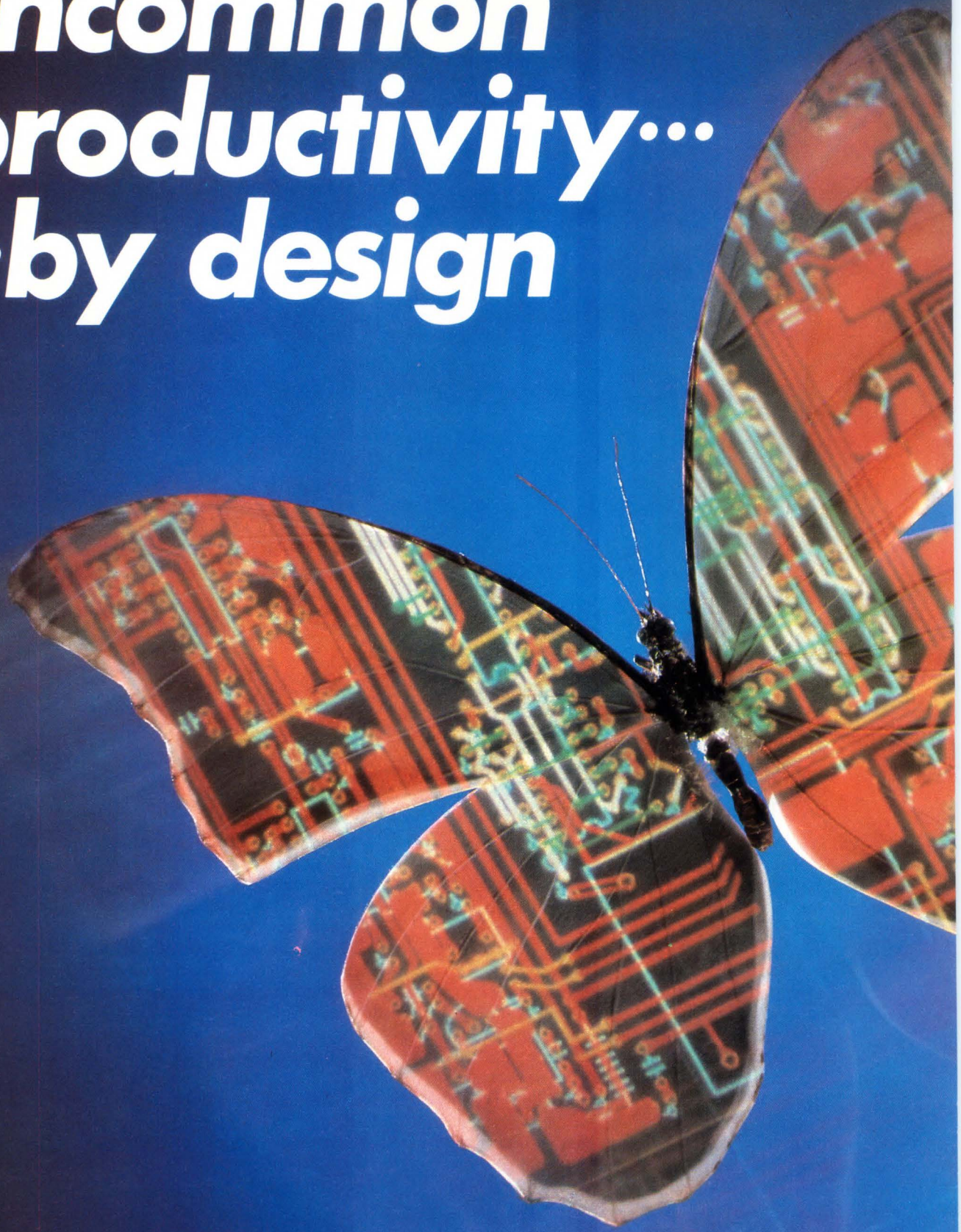

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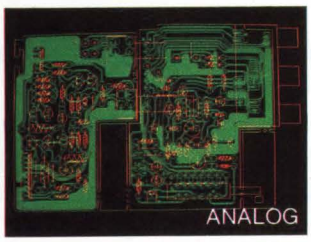

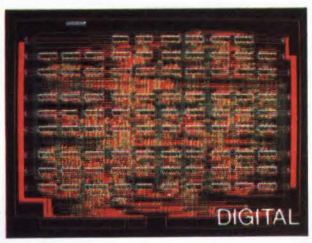

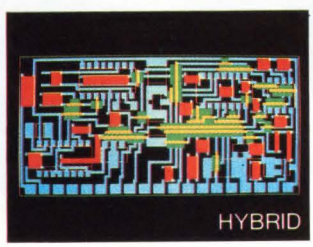

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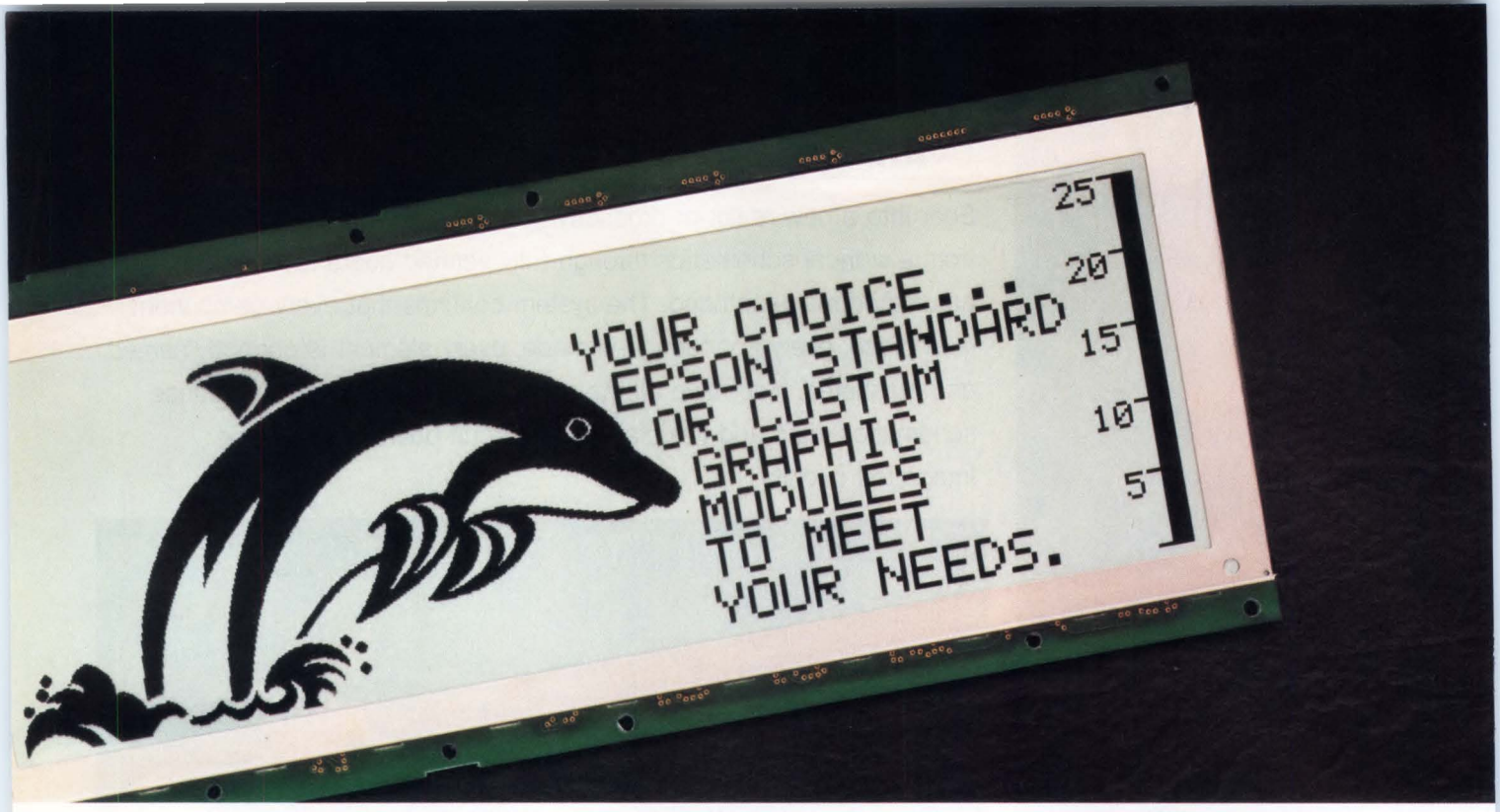

There's an Epsonomic answer to your flat panel display needs.

Our new 25-line LCD modules are part of it.

Epsonomics is made up of many things. State-of-the-art products are part of it. Products like this 640 by 200 dot matrix LCD display module.

Just as important as the products is the marriage of technologies that made them possible and practical. Advanced materials formulation combined with CMOS technology to produce large area, high density displays which combine contrast, viewing angle and operating temperature range with fast response time and low power consumption. That's part of Epsonomics, too.

Another part of Epsonomics is choice. Graphic display modules range from 640 x 200 to 84 x 32 dot formats which display 80 characters by 25 lines to 14 characters by 4 lines. All are available. In volume. Now. And if none of our standard graphic modules satisfy your design criteria, you can take advantage of our custom capability to meet your needs.

But Epsonomics is more than products. It's long life and dependable performance. It's on-time delivery. It's after sale service and support. It's giving that extra effort to help your gross profits grow. Because we want to grow with you.

Epsonomics. It's a way of doing business. In LCDs as in floppy drives, printers and printer mechanisms, it's a dedication to your needs that can help you control costs and increase sales. Let us help you design the Epsonomic answer that works best for you. Call or write today.

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CIRCLE 198

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In-phase Voltage	✓		
Total Harmonic Distortion			✓
Harmonic Phase		✓	
Magnitude	✓	✓	✓
Real Power	✓	✓	✓
VA	✓	✓	
VAR	✓	✓	
Power Factor	✓	✓	
Ratio	✓	✓	✓
Complex Ratio	✓	✓	
Frequency	✓		
Phase	✓	✓	
Group Delay	✓		

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CIRCLE 199

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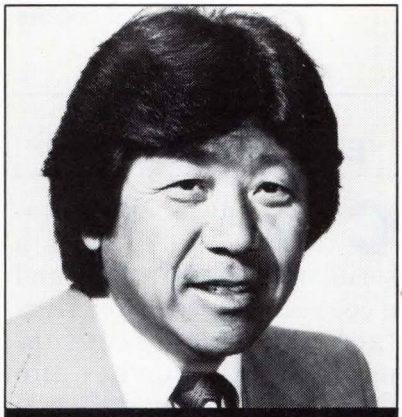

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Jan. 8, '85	Irvine, CA
Jan. 29, '85	Houston, TX
Jan. 31, '85	Dallas, TX
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COMMUNICATIONS

Multiplexer provides greater network access

Improving efficiency by enabling a larger number of terminal users to communicate with the host through fewer ports, the TS-600 switching statistical multiplexer concentrates up to 32 data devices onto a single telephone line. The unit operates at speeds up to 19,200 bits/s and provides switching and port contention capabilities. It allows users to mix and match equipment from a variety of vendors and is compatible with Digital Equipment, Data General, Hewlett-Packard, IBM, and virtually all other host computers. The multiplexer features a touch-key front panel for setting operating parameters, as well as for monitoring and testing the data communications system.

ComDesign Inc., 751 S. Kellogg Ave., Goleta, Calif. 93117; (805) 964-9852. From $3100.

CIRCLE 316

Chip set supports Ethernet, Cheapernet

Comprising a network interface controller, a serial network interface, and a coaxial transceiver interface, a three-chip set supports both Ethernet and Cheapernet systems. Cheapernet, the LAN scheme developed in Europe, soon to be incorporated into the IEEE 802.3 standard, is a protocol-compatible version of Ethernet, offering the same 10-Mbit/s bandwidth but utilizing lower-cost RG58AU coaxial cable. Combined to meet the requirements of the IEEE 802.3 standards, the CSMA/CD chip set performs the same functions as currently available boards requiring dozens of chips.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $125 (100 sets); end of 1984.

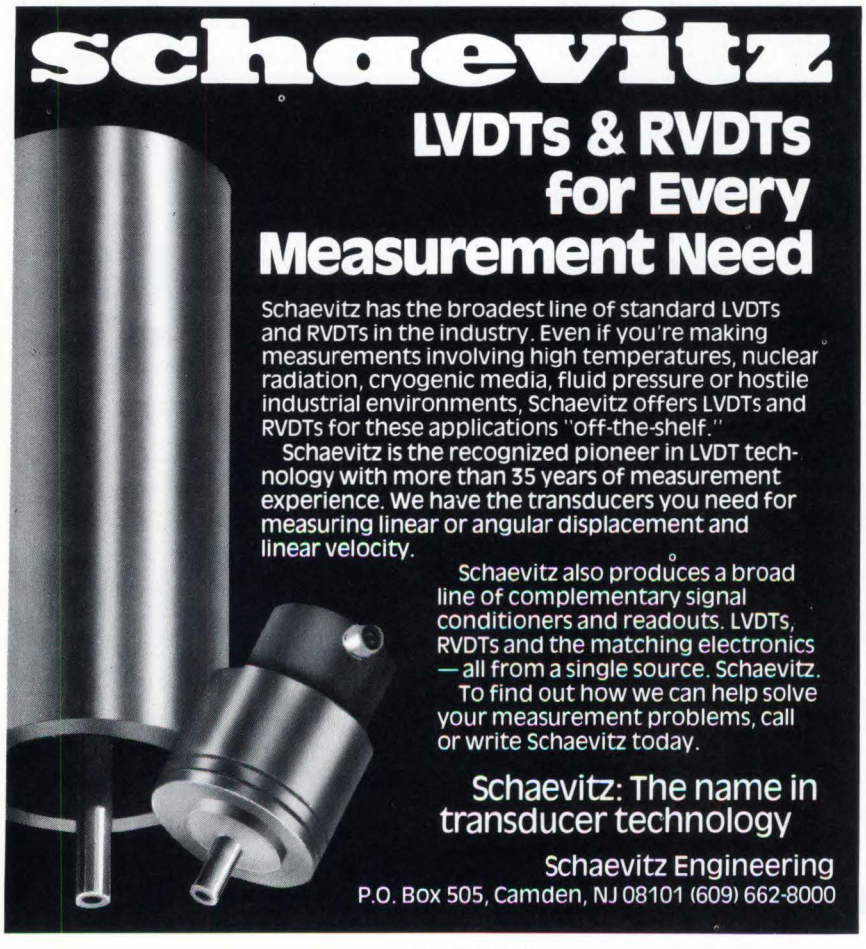
CIRCLE 390

Transfer switch selects printer

For use in minicomputer word-processing applications, a versatile transfer switch permits access to a high-speed printer for generating reports and to a slower letter-quality printer for correspondence printing. In multiple microcomputer environments, the Model 8862-D may be used to switch a single printer between two microcomputers equipped with parallel interfaces. The device is data speed- and code-transparent and requires no power. All connections are made via three 36-pin female connectors on the rear panel. A front-panel selector switch routes the data stream from the common connector to either of the other two ports.

Electro Standards Laboratory Inc., PO Box 9144, Providence, R.I. 02940; (401) 943-1164. $175; stock.

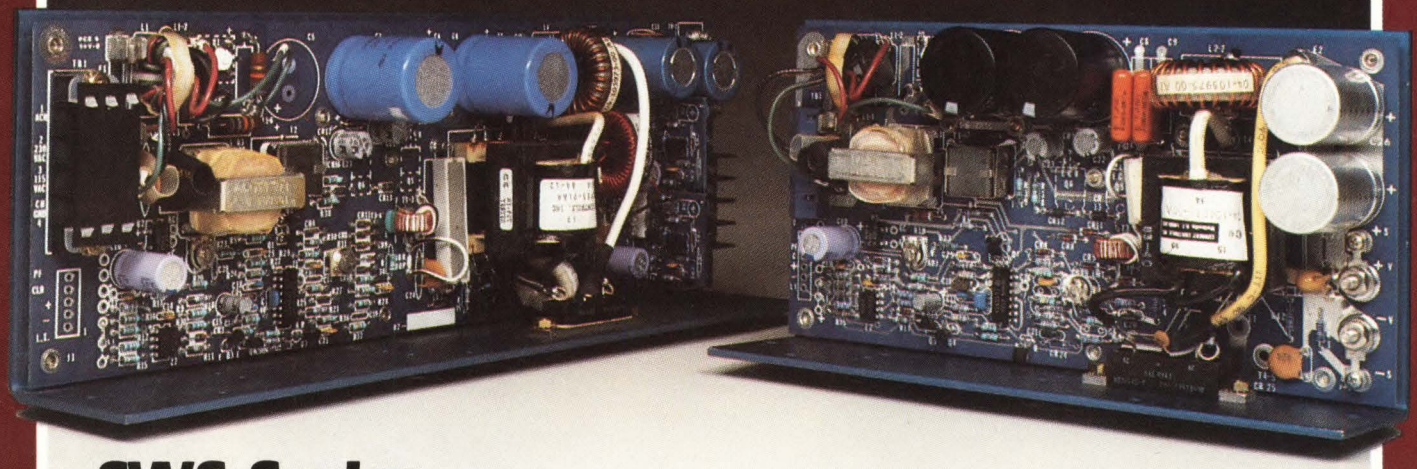
CIRCLE 317



CIRCLE 201

Computers, Peripherals, Instrumentation, Communications, Medical Electronics . . .

Our switchers are as good as gold in all these applications and markets.



SWS Series

But it doesn't end there. For many years, Standard Power has designed and manufactured switching power supplies. In fact, our SWS Series of regulated switchers represents a third-generation power system—a design using a minimum number of components, with 100 percent burn-in, which means reliability. And that's critical to your system's reliability.

That's why Standard Power switchers keep showing up in applications like process controllers, test equipment, telephone switching systems, such computer peripherals as drives, terminals, tapes and printers, document sorting equipment and machine tools.

The SWS Series includes 25 models—single, triple and quadruple outputs—in a power range from 150 to 250 watts. Each unit features line and load regulation at .2 percent each, built-in overvoltage protection and remote voltage sense on the main output, 20 millisecond holdup time and UL recognition.

In addition, we were the first manufacturer to sell power supplies through electronic distribution. Today, more than 120 distributor locations stock our power supplies for off-the-shelf delivery. So go ahead and specify Standard Power . . . the quality switcher that's available.

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CIRCLE 202

At Nichicon, an innovative design means a capacitor you can use today and tomorrow.

Building a better capacitor. That's what we've been doing since we delivered our first capacitor back in 1918.

And that's what we're still doing for you today, by improving capacitor designs to help save you *time* and *money*. By packing in greater CV in *smaller case sizes*. With *anti-solvent designs* that allow Nichicon capacitors to withstand harmful cleaning agents like Freon and Daiflon for up to five minutes—without bulky and expensive epoxy end-seals. And by exploring the realities of leadless chip capacitors of the future.

Today our SA, SL, SP, ST, MA and VX aluminum electrolytic series' are being used to replace tantalum capacitors for reasons ranging from operating reliability to size and price.

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But we're not stopping there. Call us today to find out how our 65 year investment in capacitors of the future can help meet your design needs today.

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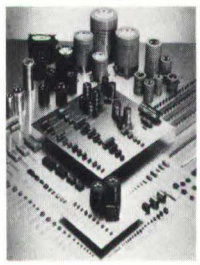

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CIRCLE 203

"SEE US AT MIDCON BOOTHS Nos. 1330-1332"

COMMUNICATIONS

Ethernet transceiver complies with 802.3

The newest member of the Net/Plus product line, the NT100 Ethernet transceiver is fully compliant with the IEEE 802.3 local area network standard. It features a nonintrusive cable tap, which permits nodes to be attached or removed from an active network without disturbing network communications. An alternative tap with an N-type connector is available for those portions of a network that can be installed with preassembled coaxial cable. The transceiver contains the necessary electronics to send and receive 10-Mbit/s bit streams, detect the occurrence of collisions, provide electrical isolation between the coaxial cable and the stations, and protect the network from transceiver and station malfunctions. The device is only 10.12 by 3.75 by 1.7 in. and installs easily in ceilings, wiring troughs, and other areas where space is limited.

Interlan Inc., 3 Lyberty Way, Westford, Mass. 01886; (617) 692-3900. $250 (100 units).

CIRCLE 318

Ethernet kit implements fiber-optic LAN

Fully compatible with Ethernet hardware and software, the Codenet starter kit implements a three-node fiber-optic local area network in the amount of time it takes to unpack the devices, connect the 12 screw-on optical connectors, and attach the transceivers to the Ethernet controllers via the user-supplied transceiver cables. Typically, this is accomplished in less than 30 minutes. The starter kit consists of three Codenet-3020/3030 fiber-optic Ethernet transceivers, one Codestar 2004 four-by-four optical star coupler, and three 100-μm fiber-optic cables, 10 meters long and factory-terminated with SMA connectors.

Codenoll Technology Corp., 1086 N. Broadway, Yonkers, N.Y. 10701; (914) 965-6300. $2995.

CIRCLE 319

1200-bit/s modem features secure access

A Bell 212A-compatible modem, designated the Auto Data 300/1200S, offers computer systems protection against unauthorized access. Access is controlled via a central modem at the host computer. It answers the incoming call, verifies the caller's code number with previously stored information, and disconnects. The modem automatically dials back the caller's telephone number, which is stored in memory. If an illegal access has been attempted, the unit resets to standby mode, thereby preventing access to the host computer. In addition to the security functions, the modem operates at dual data rates of 300 or 1200 bits/s.

Penril DataComm, 207 Perry Pkwy., Gaithersburg, Md. 20877; (301) 921-8600.

CIRCLE 320

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AND
CONTROL

MODEL DASH-8 $375
- 4,000 Samples/Sec (30,000 in Assembly Language)
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- Event, Period, Pulse Width, Frequency Measurement
- 7 Bits of Digital I/O
- Programmable Scan Rate
- Interrupt Handling
- Foreground/Background Operation

MODEL DASH-16 $895
- 40,000 Samples/Sec
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- 2 Multiplying Analog Output Channels
- 8 Bit Digital I/O
- Interrupt Handling
- Foreground/Background Operation

MODEL DASCON-1 $485
- 30 Samples/Sec, 4 D.I. Channel 12 Bit Analog Inputs
- On-Board Signal Conditioning
- Direct Temperature Measurement (−200 to +650 C.)
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- Interrupt Handling
- 2 Optional 12 Bit Analog Output Channels
- 2 Optional Instrumentation Amplifiers (0.5 MicroVolt/Bit)
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MODEL PIO-12 $ 97
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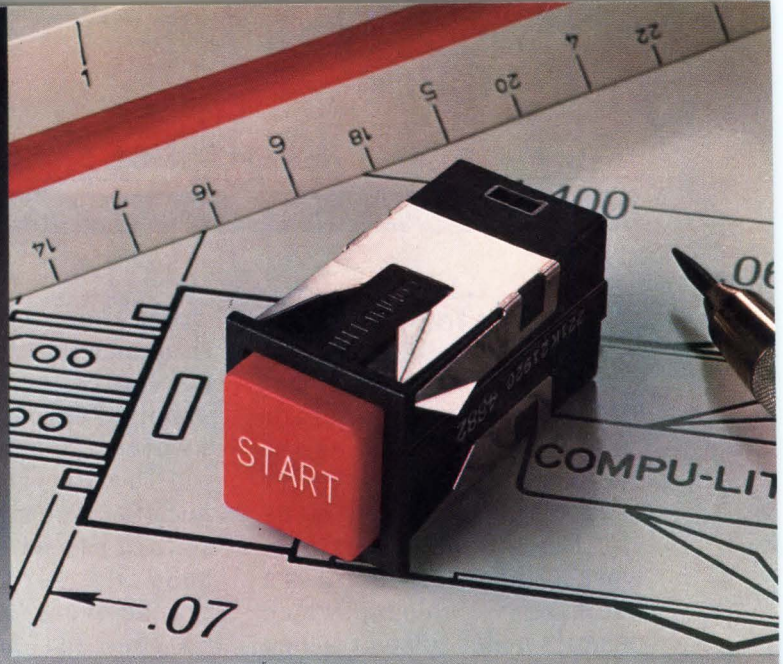
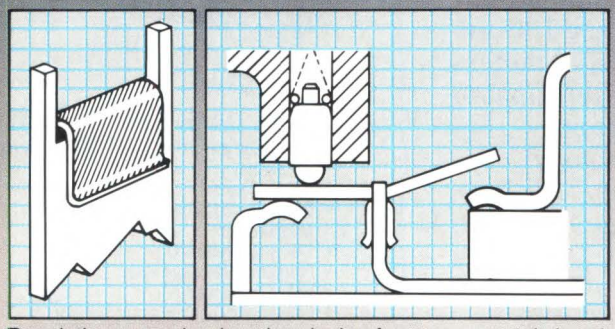
CIRCLE 204

Make the Switch





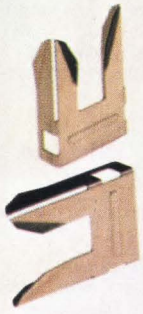
Revolutionary rocker bearing design features a metal sheath covering the pivot point. This lessens friction, resulting in reduced heat build-up, higher current ratings, and extended switch life. (patent pending)

Our new **Compu-Lite pushbutton line** is designed years ahead of the competition.

You'll stay out in front of the future with our new advance-design illuminated pushbuttons. They're the brightest idea to light up a panelboard in decades.

Get 5 amp performance at a 3 amp price. Don't let the price fool you. Our new Compu-Lite pushbuttons are conservatively rated at 5 amps. So with a 2 or 3 amp load, they'll keep working years longer. Naturally they're UL and CSA approved. Also, they're the *only* switches of this type designed to meet VDE requirements.

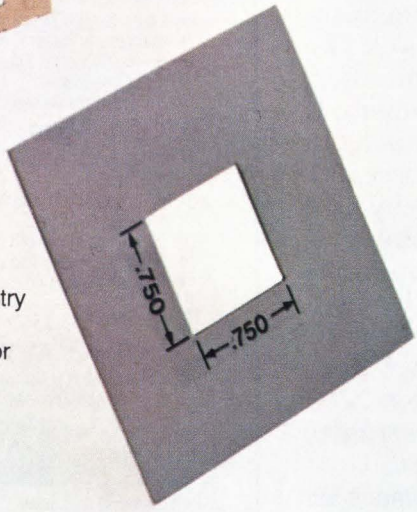
Unique contact assembly. An innovative new rocker bearing design virtually eliminates friction at the contact assembly pivot point. This distributes contact pressure more evenly, reducing resistance, arcing and bounce, thus minimizing heat build-up during operation.



Improved mounting clips let you snap Compu-Lite pushbuttons into panels ranging in thickness from .040″ to .188″

Directly interchangeable. These switches fit standard industry mounting holes and conform to behind-panel depth requirements. They are provided with solder lug or PC terminations.

The clip with true grip. Our refined clip design lets you snap our Compu-Lite pushbuttons into a wider range of panel thicknesses—and get a snug fit that holds tight. So you enjoy greater design flexibility.



Designed to fit standard industry panel cutouts (.750″ x .750″ or .750″ x 1.140″)

Get our new switch free. Write us for a free sample. We'll make sure you get one, along with our complete catalog. Eaton Corporation, Aerospace/Commercial Controls Division, 4201 N. 27th Street, Milwaukee, WI 53216.

CIRCLE 205

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EATON Electrical/Electronic Control

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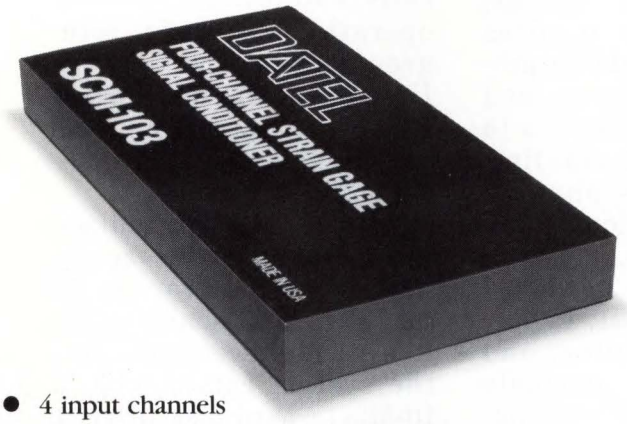
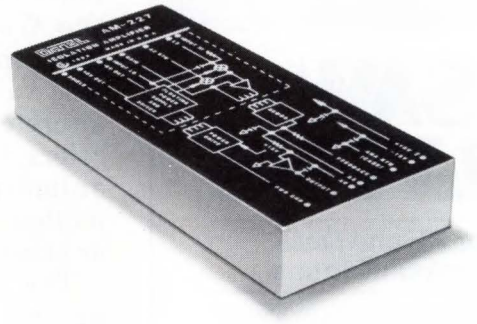
SCM-100 SERIES RTD, THERMOCOUPLE, HIGH LEVEL, STRAIN GAGE,



- 4 input channels
- 3000 channel/s scan (SCM-102, 103)
- 1000V isolation (SCM-100, 101)
- 156 db CMRR min.
- Replaces AD2B series

DATEL's SCM-100 series is composed of four 4-channel signal conditioning modules designed for industrial and process control applications. The SCM-100 and SCM-101 provide 1000 Vpk isolation and are designed for thermocouple and high level transducer signal conditioning and isolation. The SCM-102 and SCM-103 are designed for RTD and strain gage amplification and signal conditioning. For complete engineering data sheets, call the literature hot line number listed below today.

AM-227 PRECISION ISOLATION AMPLIFIER



- 1000 VDC isolation
- 0.005% nonlinearity
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- 176 dB CMRR
- Multi-sourced

DATEL's AM-227 offers excellent DC input characteristics, low cost and small size. It is an excellent choice for plant floor applications requiring isolation and precision amplification of thermocouples, RTDs, strain gages and other low level transducers. For complete engineering data sheets, call the literature hot line number listed below today.

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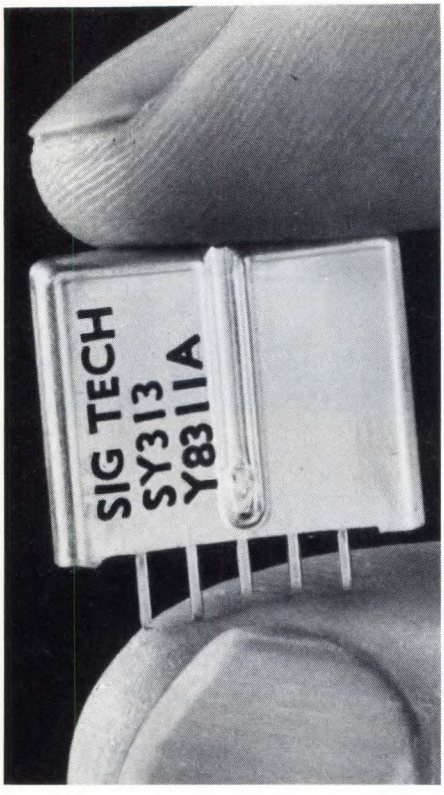
CIRCLE 206



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CIRCLE 207

FACTORY AUTOMATION

Terminal programs process controllers

Designed to work on the factory floor, a suitcase-sized terminal is used for programming and documenting programs for the Series Six, Series Three, and Series One programmable controllers. The Workmaster programmer, which is compatible with IBM PC hardware and software, also performs data acquisition and analysis functions to access critical information.

By adding a high-resolution color graphics package, the Workmaster acquires and displays in real time process variables, alarms, and discrete device states—in 16 colors. In addition, real-time animation shows physical motion, position, liquid level, or other variables.

The system is hardened against heat, dust, grime, vibration, humidity, and electrical noise commonly found in industrial environments. It operates in temperatures ranging from 0° to +50°C (+32° to +122°F). Each of Workmaster's 368-kbyte 3½-in. diskettes are plastic-enclosed for added protection and feature a spring-loaded metal shutter to protect the recording surface when not in use.

General Electric Co., Programmable Control Department, PO Box 8106, Charlottesville, Va. 22906; (800) 626-2001. From $8200 to $10,500; late third and fourth quarters.

CIRCLE 331

Computer supervises automated processes

For complete distributed control of automated factories—a multitasking master controller—the S256 Supervisor—monitors the real-time operations of vision systems, inspection stations, robotic work cells, and other products required to automate industrial and production processes. The MC68000-based computer system, which is capable of overseeing the operation of multiple sets of robotic work cells, employs a real-time operating system for foreground operations and the Unix operating system for background processing and program-development applications.

Housed in a ruggedized cabinet for use on the factory floor, the S256 provides 12 card slots (expandable to 32). In a standard configuration, the system comes with a 10-Mbyte hard-disk drive, 1 Mbyte of RAM, several specialized PROMs, and a memory-management unit, which can access up to 16 Mbytes of memory. In addition to serving as a master controller for all automated devices, it serves as its own vision/image analysis processing system when coupled with the appropriate sensing cameras.

International Robomation/Intelligence, 2281 Las Palmas Drive, Carlsbad, Calif. 92008; (619) 438-4424. From $30,000 to $50,000.

CIRCLE 332

good partners—aerosols and electronics

For years, Miller-Stephenson has specialized in aerosols designed exclusively for the electronics industry. Our high-purity spray containers suit the electronics style. Safe. Pure. Compact. Portable. Convenient. Easy to apply. Sealed containers provide uncontaminated solvent, spray after spray. Here are some of our star performers. Wouldn't one meet your specific need?

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Freon® TMC Flux Remover and Heavy Duty Flux Remover flush all types of organic flux off PCBs and other electronic assemblies without recontamination. With the Cobra Spray Brush attached, the flux remover becomes an efficient system combining chemical and scrubbing actions.

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The active ingredient for our release agents is a Teflon-like material which is dispersed in various solvents.

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To meet RFI/EMI regulations, we also offer new conductive coating sprays, which provide low cost protection and are compatible with many substrates.

and more in our catalog

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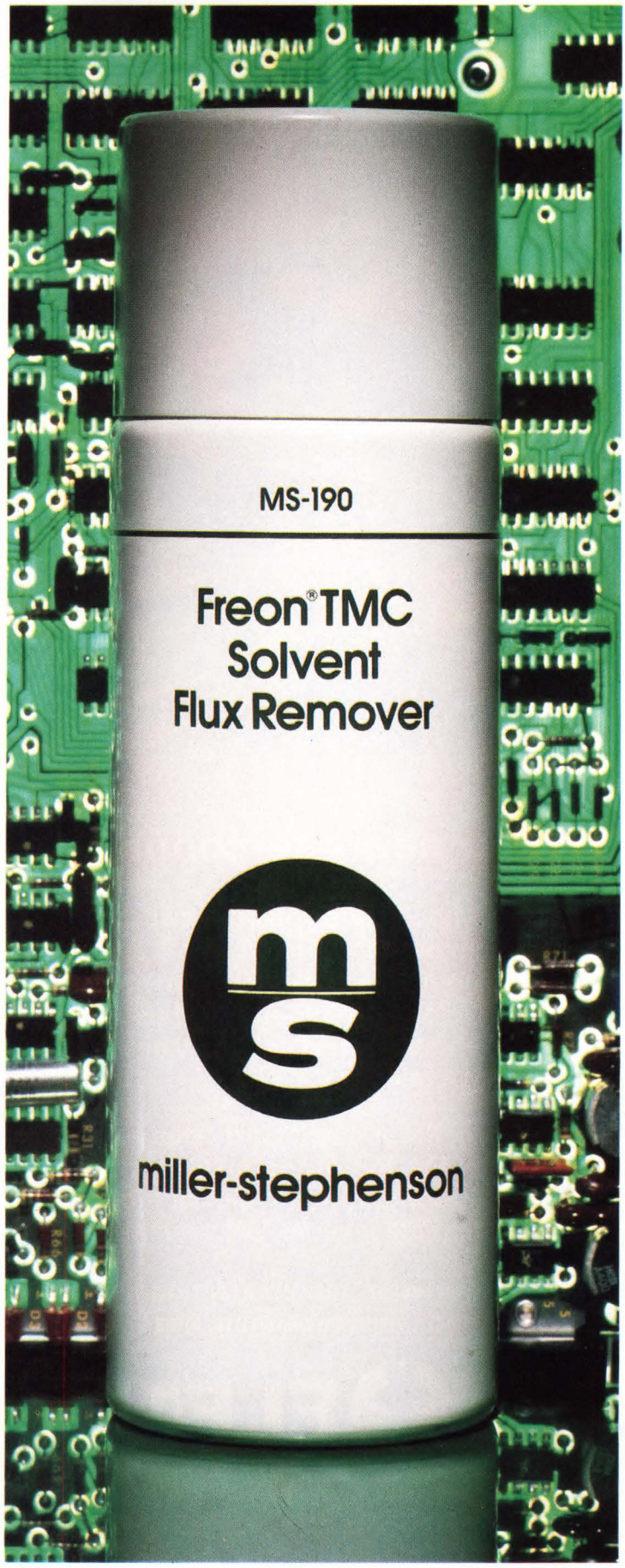
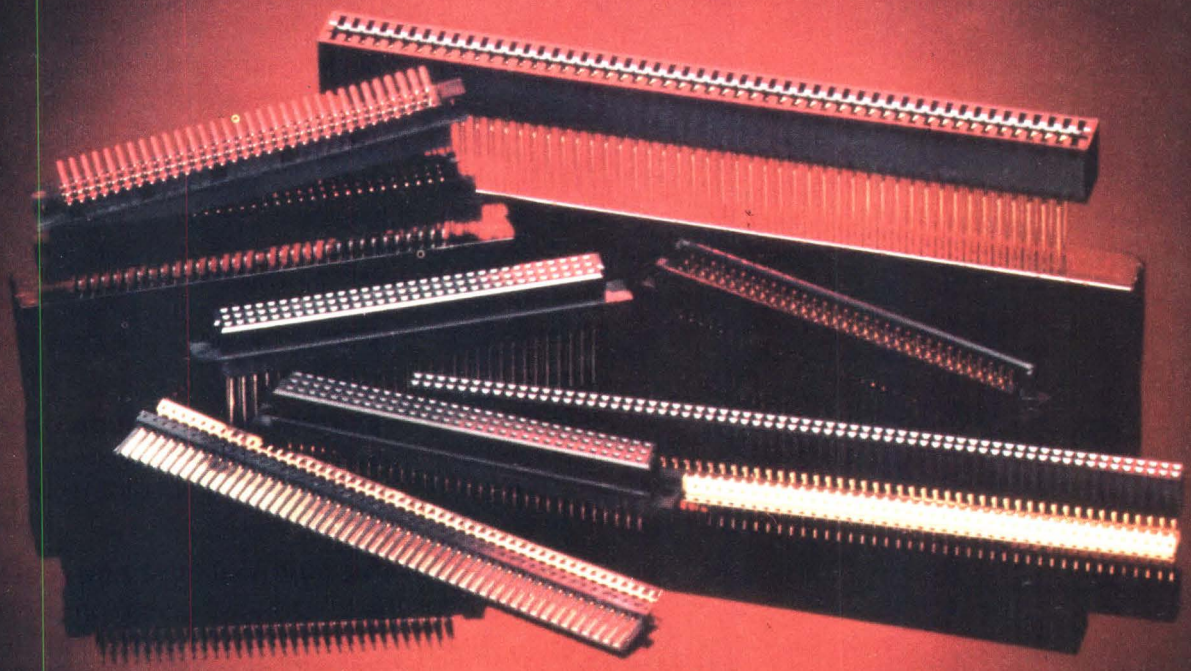


CIRCLE 208



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ELFAB now offers you our newest line of interconnect products. Our surface-mounted Finger-Pac™ and new two-row or four-row Box-Pac™ connectors simply reflow solder onto your daughter boards. Box-Pac offers high-current bussing capabilities, and occupies the least amount of real estate, of any high-density two-piece connector system available today.

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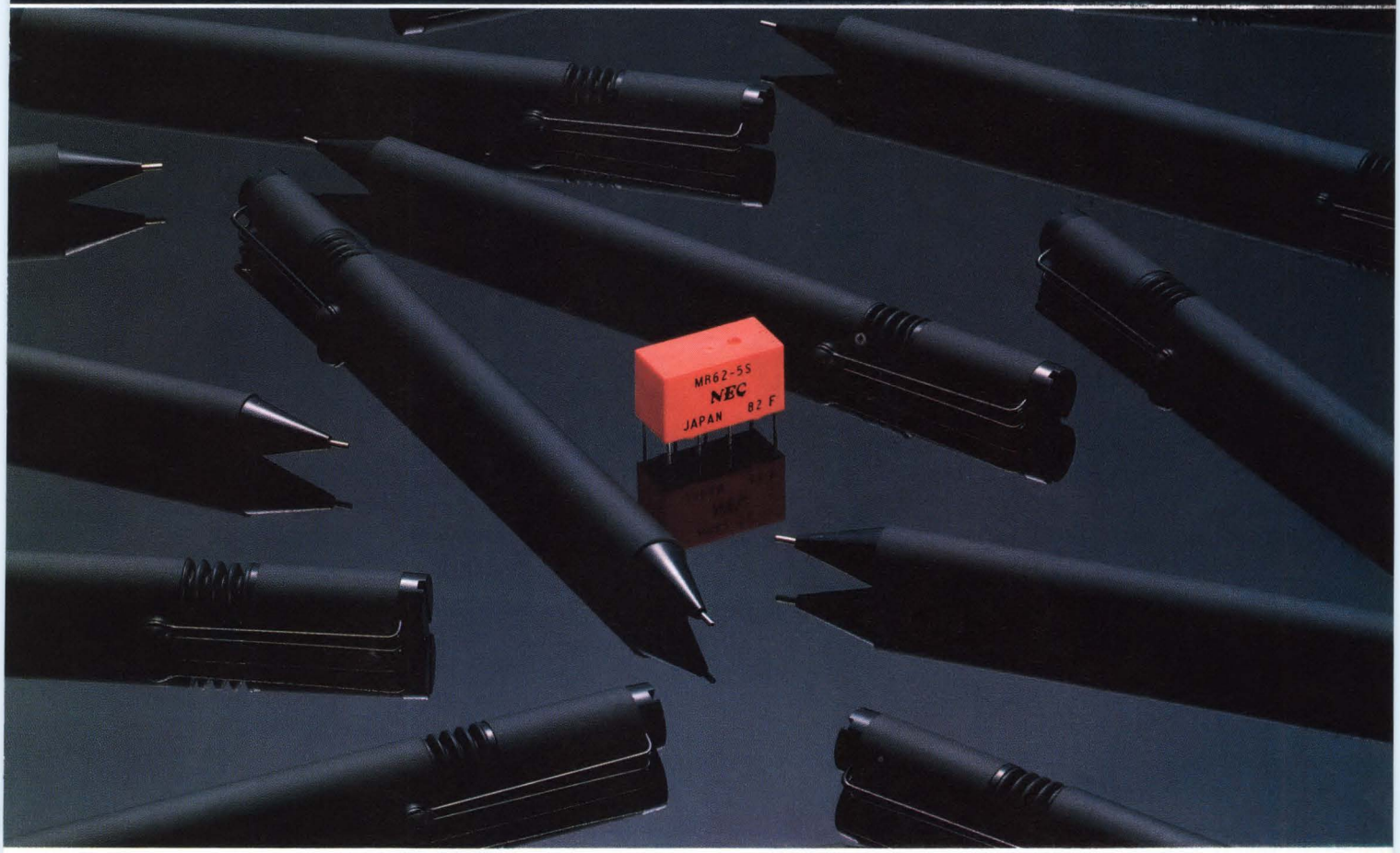
CIRCLE 80

MR62 Subminiature Relays



Leading reliability from a world leader in computers and communications.

When space is tight and conditions tough, specify MR62. It's the reliable DIP DPDT relay that really thrives on challenge. And delivers flawless performance in far-ranging applications.

MR62 relays—with nitrogen-gas-filled, twin crossbar contacts—come encased in impermeable armor. Their PBT shield scorns almost any attack—auto soldering, immersion cleaning, even chlorinated solvents.

Yet all this reliability stands only 0.45-inch high. And occupies a mere 0.31 square-inch of precious PC board real estate.

MR62 relays come in two series: standard and extra-high reliability.

We use our own relays in a full range of NEC computers and communications equipment. So we totally understand your need for reliability. Because our reputation, like yours, can rest on a single relay.

Contact form: 2C (DPDT).
Contact rating: 30W, 150VDC, 1.25A; 50VA, 125VAC, 1.25A.
Dimensions: H0.45" (+pins 0.13") ×W0.795"×D0.386".
Availabilities: Single Coil Latching Type; High Breakdown Voltage Version (Meets FCC Part 68).

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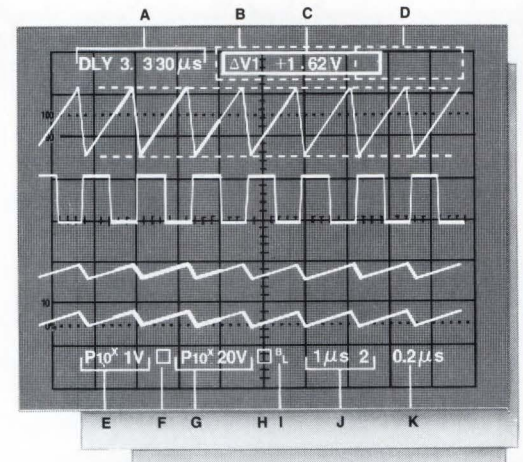
NEC America, Inc.

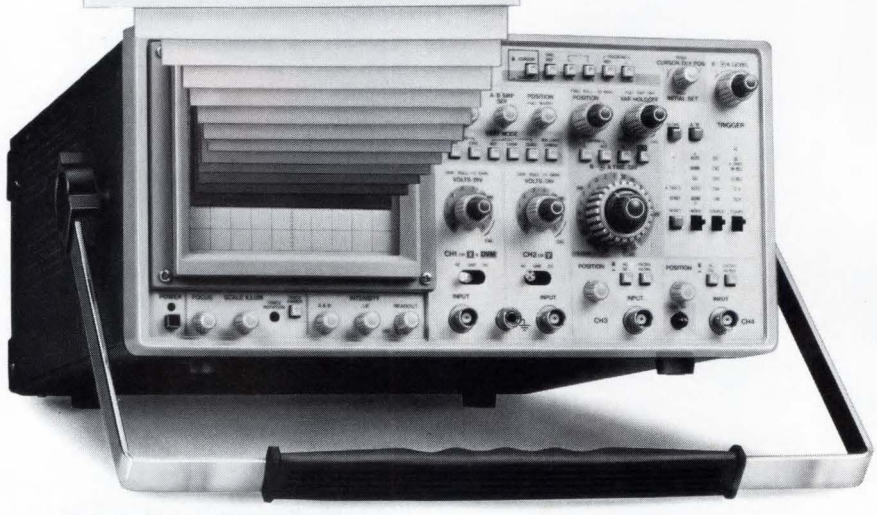
CIRCLE 209

THE INTELLIGENT SCOPE!

HITACHI V-1100



A. Delay Time
B. DVM Measured Values
C. Cursor Measured Values
D. DVM Relative Values And Frequency Measured Values
E. Scaling Factor (CH1)
F. Add Indicator
G. Scaling Factor (CH2)
H. Invert Indicator
I. BWL Indicator
J. Scaling Factor (Sweep A)
K. Scaling Factor (Sweep B)



The only Portable 100 MHz Oscilloscope with CRT readout and built-in micro-computer to make measurements faster, easier and more accurately.

Research, electronics, medical equipment development, military applications, or just general trouble-shooting...the Hitachi V-1100 Oscilloscope offers the ultimate in high-tech, high-versatility and high-value.

The Intelligent Scope is the smartest choice you can make.

This innovative state-of-the-art system is ruggedly engineered for enhanced reliability in the lab or out in the field.

Compare and you'll see why the Hitachi V-1100 is an incomparable value.

The exclusive Hitachi V-1100 features:

Readout functions	Digital Measurement functions	DVM	DC voltage: Corresponds to screen AC voltage: 50Hz to 10MHz	CH1 only	Display: 3 digits + units
		Frequency counter	Frequency: 120Hz to 99.9MHz		
	Cursor Readout function	REF, Δ cursors	Voltage Vabs: REF to GND Voltage V: Δ to REF Amplitude ratio: % (5 div = 100%) Time T: Δ to REF Time duty ratio: % (5 div = 100%) Phase: Deg (5 div = 360°) Frequency: 1/T = Δ to REF		
	Panel setting Value displays		Vertical axis: V/div, INVERT, ADD, BWL, UNCAL, MAG Sweep speed: s/div, UNCAL, MAG Other: delay time and A trigger source		
GND Reference function	Ground line display (GND LINE)		CH1 and CH2 displays are available.		

Additional features include quad channel (CH. 1, 2, 3, 4) with independent position controls, 8 trace with alternate sweep, 18kV-6" rectangular CRT, minimum deflection factor 1mv/div, maximum sweep time 2ns/div, TV-sync, X-Y operation up to 1 MHz (3° or less), variable hold-off, gate output for A and B sweep, CH 1 signal output to 100 MHz (-3dB)...plus much more.

HITACHI®

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CIRCLE 210

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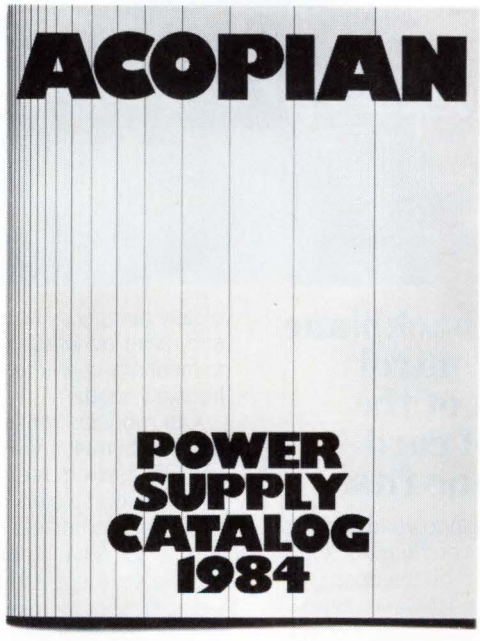
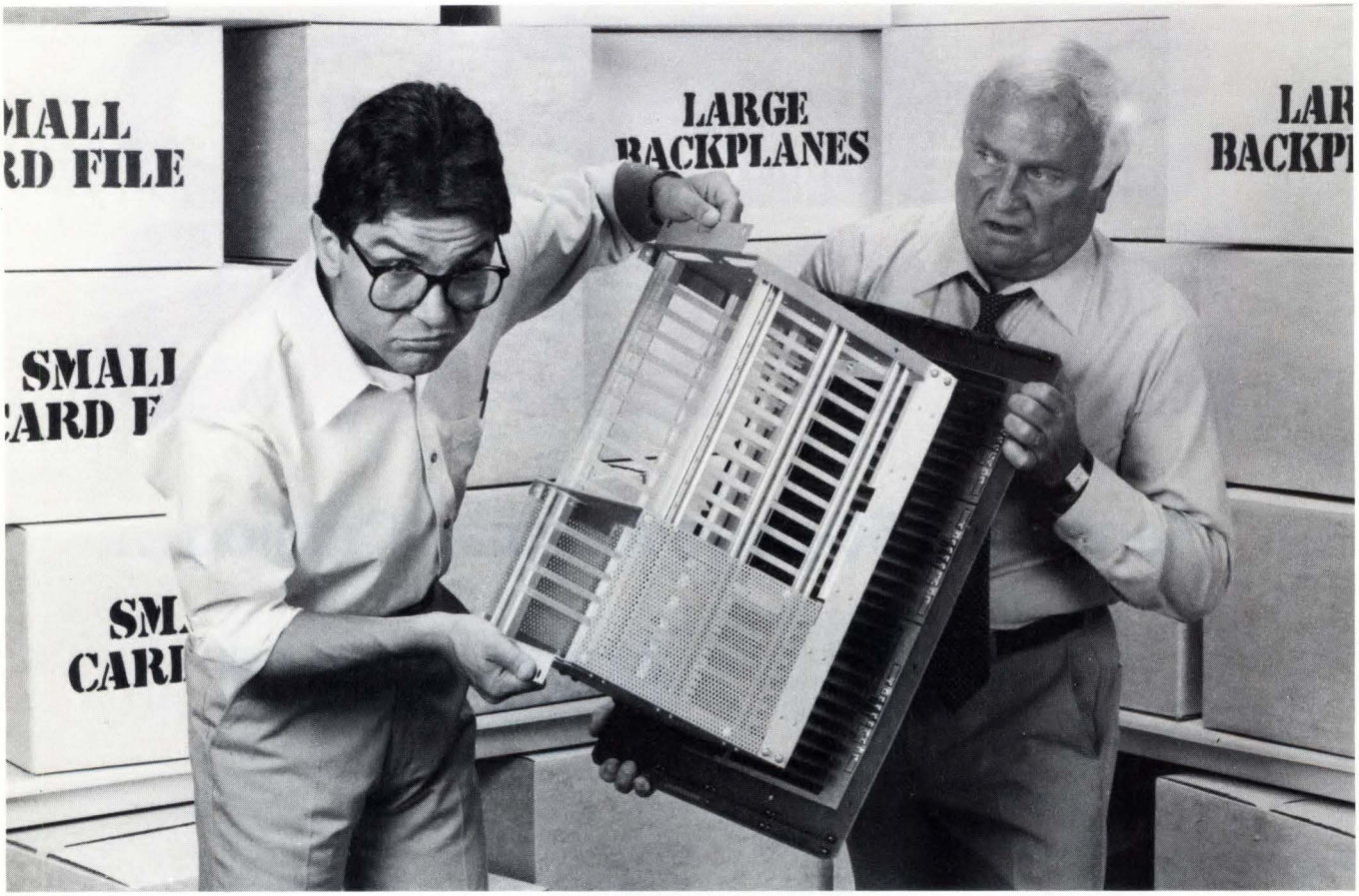


Acopian Corp., P.O. Box 638, Easton, PA 18042 • Toll free number: (800) 523-9478

CIRCLE 211

When it comes to card file integration, is this the kind of fit your backplane vendor gives you?



SAE's total backplane packaging control assures you of the right kind of card file-backplane fits.

Too bad your backplane vendor didn't tell your card file supplier the mounting holes had been moved on the board. SAE offers integrated backplane manufacturing and card file construction operations to eliminate problems like this one. We're the only backplane vendor who can take single-source responsibility for *every* backplane system building, testing, and servicing step—including backplane-card file alignment. Our in-house, completely numerically controlled machine and metal fabrication shop delivers cages to meet any card size, air flow, or external housing needs.

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Besides our complete card file and backplane-chassis integration capabilities, SAE also offers PC board and metal backplane construction • logic panel manufacturing • complete backplane testing • wire-wrapping • plastics molding • contact plating and stamping. In short, everything you need to maintain total control over system quality and reliability.

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(408) 988-0700 **CIRCLE 212**

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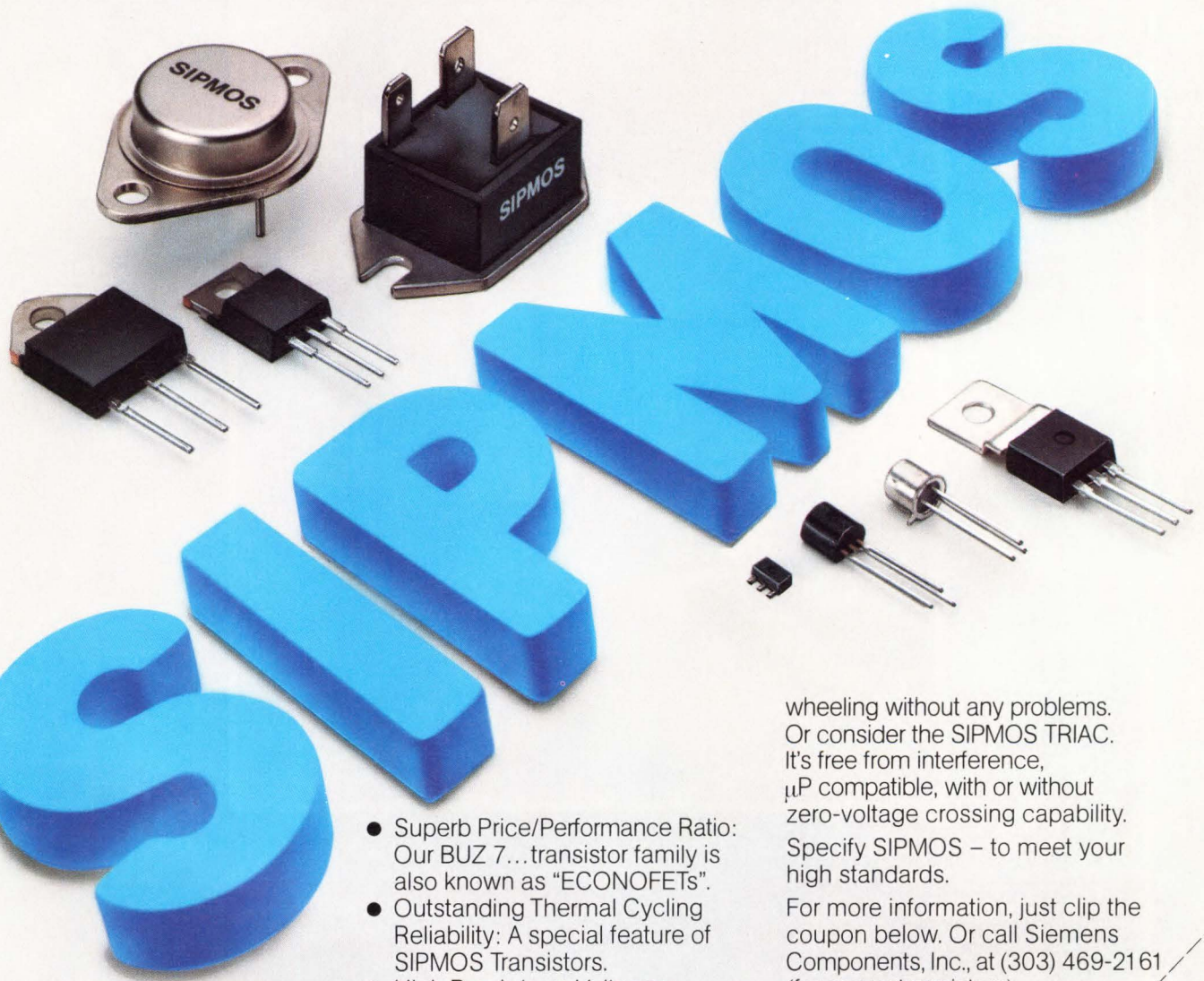

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Whether your design requires SIPMOS power or SIPMOS small signal transistors, you get the benefit of state-of-the art components. Just look at these outstanding examples.

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Specify SIPMOS – to meet your high standards.

For more information, just clip the coupon below. Or call Siemens Components, Inc., at (303) 469-2161 (for power transistors), (800) 222-2203 (for small signal transistors), or (408) 257-7910 (for SIPMOS TRIACs).

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CIRCLE 339

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Please send me information on ☐ SIPMOS power transistors; ☐ SIPMOS small signal transistors; ☐ SIPMOS TRIACs.

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ED 9/6/84

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CIRCLE 214

When it comes to enclosures, we've got you covered.

ANALOG

Voltage-output version of DAC80 settles to 0.012% within 1 μs

The latest voltage-output renditions of the DAC80 digital-to-analog converter include one with the fastest settling time yet of any such chip. The Harris HI-5690 guarantees an output swing of 20 V (from +10 to −10 V or vice versa) in under 1 μs to within 0.012% of its final value. That guarantee holds for the full operating temperature range of 0° to +75°C.

Two other chips in the family, the HI-5695 and the HI-5697, have a guaranteed settling time of 1.2 μs over −25° to +85°C and −55° to +125°C, respectively. They typically settle in 750 ns.

The chips' output op amp slews at 50 V/μs yet overshoots less than 1 V. That high speed is attributed largely to a dielectric isolation process that decreases parasitic capacitances, minimizes glitches, and permits the construction of fast vertical pnp transistors.

Like their settling time, the converters' accuracy is guaranteed over temperature. A segmented circuit architecture produces the 3 MSBs by adding equal current sources and consequently ensures monotonicity over temperature. These equal current sources are connected to a laser-trimmed R-2R ladder for the 9 LSBs. The results are terminal, or integral, nonlinearity specifications of ±¾ LSB over temperature for all three family members. (In an all-codes, 4096 test, a typical unit remains accurate to within +0.12 and −0.18 LSB, far better than the mandatory ±0.5 LSB.)

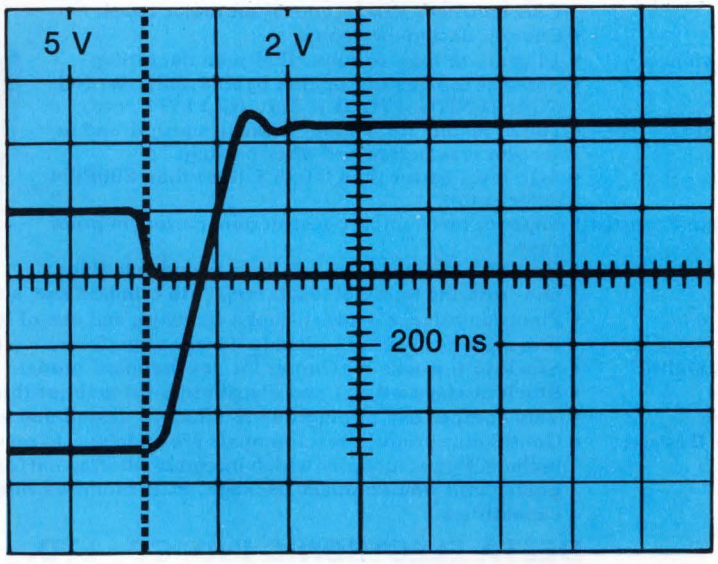
The converters operate from power supplies of ±11.4 to ±16.5 V and do not need +5 V power.

The devices, which come in a 24-pin side-brazed DIP, can be connected to provide full-scale output voltage swings of ±10, +10, ±5, and +5 V. They are available screened to MIL-STD-883C.

Housed in a ceramic DIP, the chips sell for $25 to $130 apiece. Sample quantities are available from stock.

Harris Corp., Analog Products Division, PO Box 883, Melbourne, Fla. 32901; Mary Lozito, (305) 729-5627.

CIRCLE 305



With an output swing of −10 to +10 V, the HI-5690 d-a converter settles to within 0.012% of its final value in less than 1 μs.

Heather Bryce

ANALOG

S-h amplifier offers tight specs

By using a combination of bipolar and junction FET transistors and optimizing the key parameters of design, fabrication, and testing, the LF198A sample-and-hold amplifier is able to meet the tight electrical specifications of the industry standard. A maximum offset voltage of 1 mV and a guaranteed 0.005% maximum gain error enable the LF198A to be used in 12-bit data acquisition systems. Dynamic performance can be optimized through the selection of the external hold capacitor. Acquisition times can be as low as 4 μs for small capacitors, while hold step and droop errors can be held below 0.1 mV and 30 μV/s, respectively, when using larger capacitors. The sample-and-hold amplifier is available in a TO-5 metal can or an 8-pin plastic DIP.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, Calif. 95035; (408) 942-0810. From $2.85 (100 units). **CIRCLE 323**

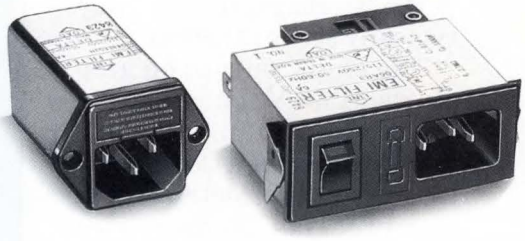
16-bit DAC has ±0.0008% nonlinearity

The DAC-02900, a 16-bit hybrid d-a converter, settles within 15 μs and is offered in linearity-error grades of 0.0008%, 0.0015%, and 0.003%. Gain and offset errors are both specified at 0.1% FSR. The device has a 10-V full-scale output range and operates over the entire military temperature range of −55° to +125°C. It also contains a 6.4-V precision internal reference and an output op amp. Housed in a 24-pin double-wide DIP, the converter has dimensions of 1.3 by 0.8 by 0.2 in. and weighs only 0.4 oz. The DAC-02900 is a pin-for-pin replacement for DAC-HP16 and DAC-72 types. Screening to MIL-STD-883B is available.

ILC Data Device Corp., 105 Wilbur Place, Bohemia, N.Y. 11716; (516) 567-5600. $239 (±0.0008 nonlinearity); stock to eight weeks.

CIRCLE 324

DELTA EMI FILTERS
THE RIGHT CHOICE FOR DESIGN-IN



1. Selection	• Over 200 standard part numbers UL recognized and CSA certified. VDE approval on major types. • Custom designs welcome.
2. Experience	• 14 years in high volume OEM manufacturing. • Rated as top quality supplier by IBM, DEC, WANG, RCA, ZENITH, PHILIPS, ITT, TELETYPE, etc.
3. Quality	• 100% tested for hi-pot, leakage current and insertion loss before and after potting. • AQL level better than 0.025% (less than 200PPM defect rate).
4. Design Features	• Superior mechanical construction, corrosion-proof case. • Molded core cover to separate toroid windings, non- rotating terminal insulators, both crimped and soldered connections. • Precision balance between choke windings, and use of low leakage current, high voltage and temperature stable capacitors provide excellent performance under actual operating conditions.
5. Availability	• Stock to 6 weeks maximum for any standard model. • Stock at Hayward, CA and distributors throughout the U.S.
6. Price	• Very competitive pricing due to efficient design and automated mass production.
7. New Designs	• Continuous product developments are underway to meet changing market requirements. New products include: Power modules which integrate filtering, on/off power switch, voltage selector switch and fuse holder into one compact package, PCB mounted line filters, and AC line cords incorporating filter capabilities.

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ANALOG

12-bit TTL DAC settles in 65 ns

One of the highest speed TTL-compatible d-a converters available, the DAC812 has a current-output settling time of less than 65 ns to within ±0.012% of full scale. The 12-bit converter's fast settling time and excellent stability over time and temperature are the result of a proprietary high-speed bipolar process.

An internal applications resistor, for use with an external op amp, is included to convert the output current into a voltage for ranges of 0 to +10 V or −5 to +5 V. An output compliance voltage range of ±4 V allows the generation of an output voltage without using an external op amp. The DAC812 is specified over the temperature range of −25° to +85°C.

Burr-Brown Corp., Data Products Division, PO Box 11400, Tucson, Ariz. 85734; (602) 746-1111. From $86 to $115 (100 units). **CIRCLE 325**

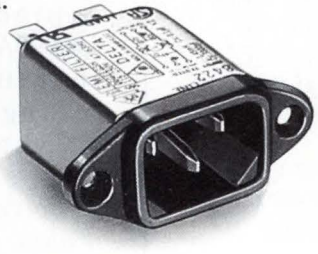
Synchro-to-dc units do 400 conversions/s

Miniature 1.5³-in. synchro-to-dc converters, which convert three-phase synchro or two-phase resolver inputs into dc sine and cosine outputs, perform 400 conversions/s. In addition, the units offer a peak angular error of ±3 minutes. Designated the Series SD109, the converters accept the output of a standard 11.8- or 90-V three-wire synchro or four-wire resolver. Input frequency is 400-Hz, ±10%, with a nominal impedance of 10 kΩ. The input is transformer-isolated and balanced line to line. The output voltage range is 0 to ±5 V dc. Specified for operation in the temperature range of −55° to +85°C, the 1.75-by-1.75-in. device stands 0.5 in. high. and is designed for pc board-mounting.

Computer Conversions Corp., 6 Dunton Court, East Northport, N.Y. 11731; (516) 261-3300. From $350 (unit quantities); stock to three weeks. **CIRCLE 326**

DELTA EMI FILTER
THE COST-EFFECTIVE SOLUTION FOR NOISE SUPPRESSION

Customers tell us that the high costs of filters on the market today force them to use discrete component on-board filtering, even though this may allow input AC wiring to pickup undesirable internally radiated noise. We feel these high costs are due to excessive profit margins and/or inefficient manufacturing methods. Delta's goal is to drive down the cost of filters through the use of modern manufacturing methods, automated production techniques, high quality raw components and strict attention to quality control.



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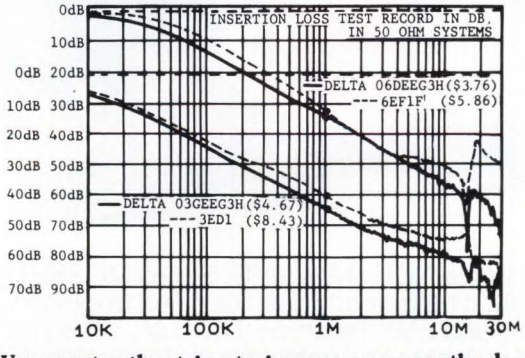
CSA 48852
VDE 32526



We constantly strive to improve our methods; shown above are comparative test results on insertion loss versus frequency for Delta's and a competitor's filters. Measurements were made on an HP 3577A network analyzer. Figures shown in brackets are the 500-999 unit prices for comparison purposes.

SEE US AT MIDCON BOOTH NO. 1517

FOR MORE INFORMATION, PLEASE CONTACT:
DELTA ELECTRONIC IND. CO., LTD.
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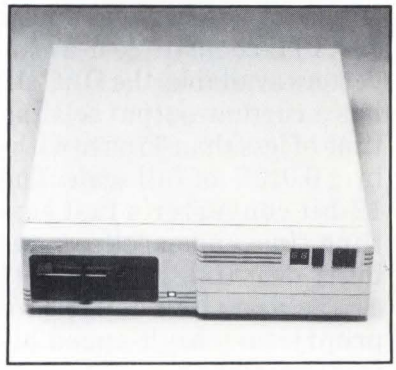
TELEX: "26524 DELTATRO" TEL: (02) 511-3621, 521-3328—9

CIRCLE 215

COMPUTER PERIPHERALS

Tape backup unit works on its own

A 1/4-in. tape cartridge unit, designed for Hewlett-Packard's desktop computers, offloads backup functions from the host computer, stores 20 Mbytes, and in emergencies can stand in for a 5 1/4-in. Winchester disk drive. Bering Industries' Model T100, also called the Sponge, backs up an HP913x-type hard disk by taking command of the Hewlett-Packard Interface Bus (HP-IB) and isolating the disk from the CPU.



The user simply pushes a button to activate the tape unit, which, in its interaction with the host, resembles an intelligent Winchester disk drive. A built-in 64-kbyte cache memory improves the unit's data access, making its performance comparable to that of a disk drive. Consequently, the unit can be used as a disk drive if necessary.

The drive's full streaming data transfer rate is 25 seconds per megabyte. Thus a 15-Mbyte hard disk can be copied onto a standard DC600A tape cartridge in less than 8 minutes.

Single-piece pricing is $2380, and delivery is within 30 days.

Bering Industries Inc., 1400 Fulton Place, Fremont, Calif. 94539; Chin Choy, (415) 651-3300. **CIRCLE 303**

When we offer international safety/EMI compliance, we make it stick!

Every time NCR ships an "S" Series MOSFET switching power supply, it has already been certified to exacting international safety and EMI standards. UL, CSA, VDE(TUV), FCC and IEC set the design and performance requirements our products routinely meet. NCR also certifies custom designed and modified standard power supplies prior to shipment.

We offer a wide choice of MOSFET switchers — single or multiple output, 100 watts and up, open frame or enclosed.

If your application demands the latest in power supply technology, with safety and EMI standards already met, contact NCR for detailed specifications and price quotation. NCR Power Systems, 584 S. Lake Emma Road, Lake Mary, FL 32746. Phone 800/327-7612.

NCR Power Systems

CIRCLE 216

COMPUTER PERIPHERALS

Graphics display suits military applications

The Miligraphic display, a rugged system that combines high-resolution raster-scan graphics with the processing power of multiple MC68000 microprocessors, is designed for severe airborne, shipboard, and ground mobile environments. The display features a VMEbus architecture and is compatible with the MIL-STD-1553B high-speed graphics network, Naval Tactical Data Systems (NTDS) interfaces, and RS-232-C communication links. The 19-in. display has a resolution of 1280 by 1024 pixels and is capable of displaying up to 256 colors or shades of gray from a palette of 16 million.

Sanders Associates Inc., Miligraphic Display Products, Defense and Information Systems Division, C.S. 2035, Nashua, N.H. 03061; (603) 885-3522.

CIRCLE 327

Rasterizer optimizes color graphics copiers

Designed for use with the 4691 and 4692 color graphics copiers, the 4510 color graphics rasterizer accepts images as high-level graphics commands across an RS-232-C interface and converts them into 4691- and 4692-compatible raster data. The image is rasterized at the full resolution of the copier—2460 by 1560 dots for the 4691 and 1536 by 1152 dots for the 4692. In contrast, a 4690 series copier connected directly to a display terminal is limited to the terminal's resolution.

The rasterizer also expands the color range for both copiers by supporting up to 256 colors from a palette of more than 1300. It is available in three memory configurations: 128 kbytes, 512 kbytes, and 2 Mbytes, which are priced at $4495, $5995, and $9995, respectively.

Tektronix Inc., MS 63-635, PO Box 500, Beaverton, Ore. 97077; (503) 644-0161.

CIRCLE 328

Adapter links GPIB with parallel printers

A parallel printer adapter, designated the GPAD-C, allows any printer that has a Centronics parallel interface to be connected with any computer or controller that has a GPIB (IEEE-488) interface. The GPIB address is selected by a five-position DIP switch. The 3½-by-5¾-in. device includes a power supply and two cables, which allow six feet between the printer and the GPIB connection. Compatible computers and controllers include those from Hewlett-Packard, Tektronix, and Osborne, to name a few. Compatible printers range from low-cost dot-matrix types to high-speed, letter-quality daisy-wheel printers.

Connecticut microComputer Inc., 150 Pocono Road, Brookfield, Conn. 06804; (203) 354-9395. $179; stock.

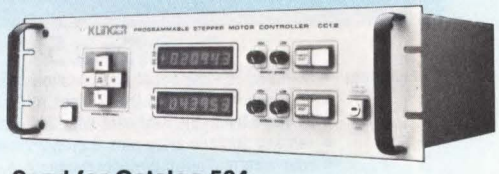
CIRCLE 329

MICRO POSITIONERS FOR MICRO ELECTRONICS

Programmable, Repeatable, Ultra-High Precision.

- Full range of computer compatible linear, vertical and rotational positioners.
- X, X-Y, X-Y-Z modes with rotation.
- 0.1μ linear accuracy; 0.001° angular resolution.
- Ideal for wafer probing, dicing, scribing, resistor trimming, mask alignment and thick or thin film measurement.
- Computer controlled indexer provides full logic and drive input for unerring repeatable accuracy.
- Versatile design permits use for electronic and electro-optical applications.

Model CC1 Programmable Controller.



Send for Catalog 584.

KLINGER SCIENTIFIC

110-20 Jamaica Avenue
Richmond Hill, NY 11418
(212) 846-3700

CIRCLE 217

COMPUTER PERIPHERALS

RS-232-C adapters ease interconnection

Simplifying the interconnection of personal computers and peripherals is the EZ-232 system—a series of adapters that permanently attaches to the computer's RS-232-C serial port and to its peripherals. The adapters terminate in standard six-wire RJ-12 jacks and are connected by ordinary telephone-type cable, which is supplied in various lengths. Adapters are available for all popular types of connectors, including those used on IBM PC and Apple computers. The adapters provide full handshaking and perform all the proper signal matching. A push-button unit is also available that permits routing data between up to four peripherals or computers that have been outfitted with the EZ-232 adapters.

Micro-Module Systems Inc., PO Box 2198, La Jolla, Calif. 92038; (619) 268-8028. $12.95; stock. **CIRCLE 330**

RGB color monitor plugs into Apples

The AppleColor Monitor 100, a 12-in. RGB monitor, works with Apple IIe, III, and III Plus personal computers to produce a high-quality color display of both text and graphics. The monitor features a screen tilting mechanism for adjusting the viewing angle and an antireflective screen surface that reduces glare. The extended 80-column text/AppleColor card is required to connect the monitor to the Apple IIe computer. In addition to providing RGB color output capability and 80-column text-display support, the plug-in card adds 64 kbytes of internal memory. When being used with the Apple III and III Plus computers, the monitor plugs directly into their built-in video ports.

Apple Computer Inc., 20525 Mariani Ave., Cupertino, Calif. 95014; (408) 996-1010. $599 (monitor), $299 (RGB interface card).

CIRCLE 331

$249. TERMINAL

TRANSTERM 5

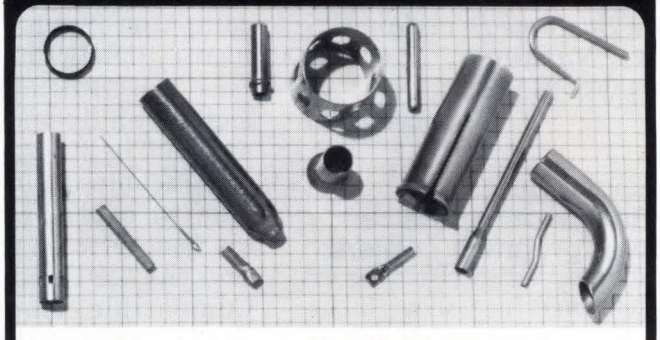
Featuring
- Standard RS-232 Serial Asynchronous ASCII Communications
- 48 Character LCD Display (2 Lines of 24 each)
- 24 Key Membrane Keyboard with embossed graphics.
- Ten key numeric array plus 8 programmable function keys.
- Four-wire multidrop protocol mode.
- Keyboard selectable SET-UP features—baud rates, parity, etc.
- Size (5.625" W × 6.9" D × 1.75" H), Weight 1.25 lbs.
- 5 × 7 Dot Matrix font with underline cursor
- Displays 96 Character ASCII Set (upper and lower case)

Options—backlighting for display, RS-422 I/O, 20 Ma current loop I/O, integral bar code wand support (Code 39).

COMPUTERWISE, INC.
4006 E. 137th Terrace • Grandview, MO 64030 • (816) 765-3330 • TELEX 705337

CIRCLE 218

What Design Engineers Should Know About Miniature Metal Tubing



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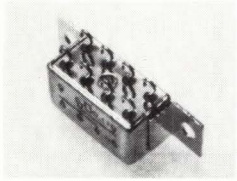
CIRCLE 219

Genicom Relay Technology Helps Make The Space Shuttle Fly.



The Space Shuttle is an outstanding example of some of the most advanced technology on Earth, and in space. And inside this marvel of science, Genicom relays play their vital role in making shuttle missions successful.

Genicom, formerly part of GE, is now an independently owned corporation. So the reliability of Genicom relays is insured, because Genicom combines decades of experience with the most advanced manufacturing techniques to create state of the art, precision relays.

We're experts in the specialized processing technologies that help make Genicom relays the first choice for operations in hostile environments or anywhere consistent reliability is vital.

Precision laser beam sealing, specially selected contact materials, super clean room environments and rigorous high tech cleaning processes all help insure the Genicom standard of quality and performance upon which our customers depend.

Of course, our final step is testing. The latest automated equipment submits each relay to rigid and exacting operational standards. So if your application has a special need, Genicom stands ready to respond with proven, quality relays.

Today, Genicom offers a wide range of crystal can relays, including the new DeciGrid Relay, which is less than 3/16 of an inch high...the smallest profile available today. The new DeciGrid, like all Genicom relays, is designed for a broad range of commercial and military aircraft, missile systems, test equipment, process control systems and satellites.

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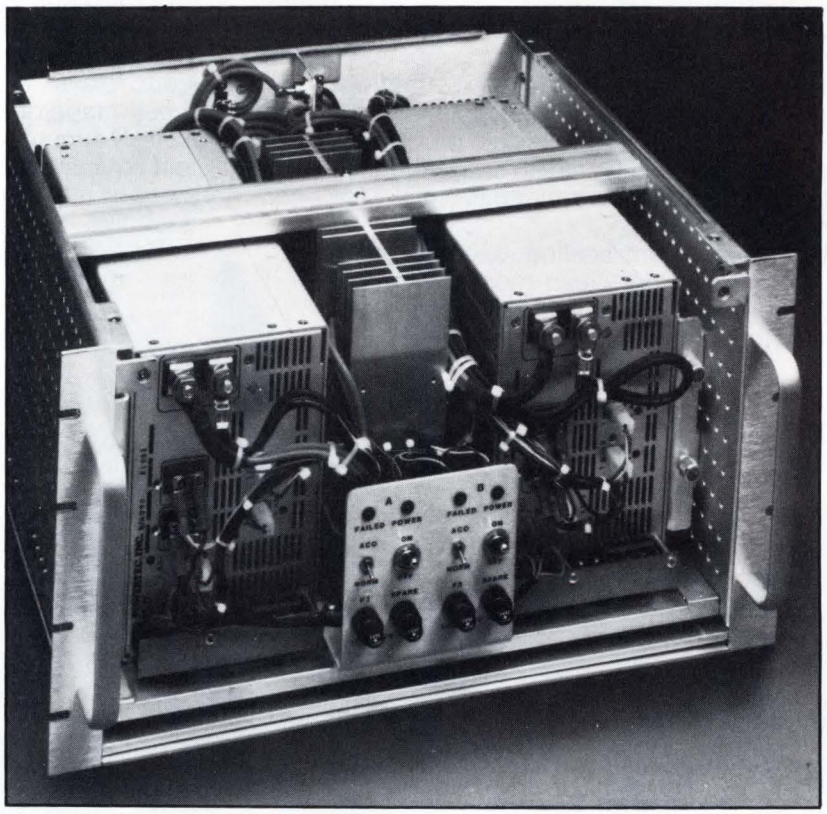
POWER

Mirrored, parallel supplies hike reliability by sharing the load



Two power supplies in parallel ordinarily cannot ensure power delivery for systems demanding high reliability; if one fails, it may bring the system down. The Powertec PowerSystem solves this problem by paralleling two power supplies in a load-sharing configuration, combining their regulated outputs using isolation diodes. Each supply drives 50% of the load in normal operation and 100% if a failure occurs.

Reduced loading has the added benefit of dropping the supply's operating temperature, resulting in a longer life for each supply.

Also, typically in OEM systems, the supplies are loaded to 75% to 80% of their power ratings. The PowerSystem can be loaded closer to its rating, because a single supply will operate at that load only for the short time that the other is down. However, the power dissipation in the isolation diodes (12%) must be taken into account when loading is considered.

The PowerSystem's front panel includes lights to indicate failures. A failed supply can be quickly replaced while its partner carries the load; the front panel drops down and the user simply slides supply out.

The unit is designed for a standard 19-in. rack and meets UL, CSA, and BT (British Telecom) standards. It uses standard Powertec power supplies from the MultiMod, ValuSwitcher, and SuperSwitcher lines. Outputs of 50 to 1700 W are available with a wide range of output configurations. Pricing and delivery depend on the supplies chosen.

Powertec Inc., 20550 Nordhoff St., Chatsworth, Calif. 91311; Barry Chenes, (818) 882-0004.

CIRCLE 308

Ray Weiss

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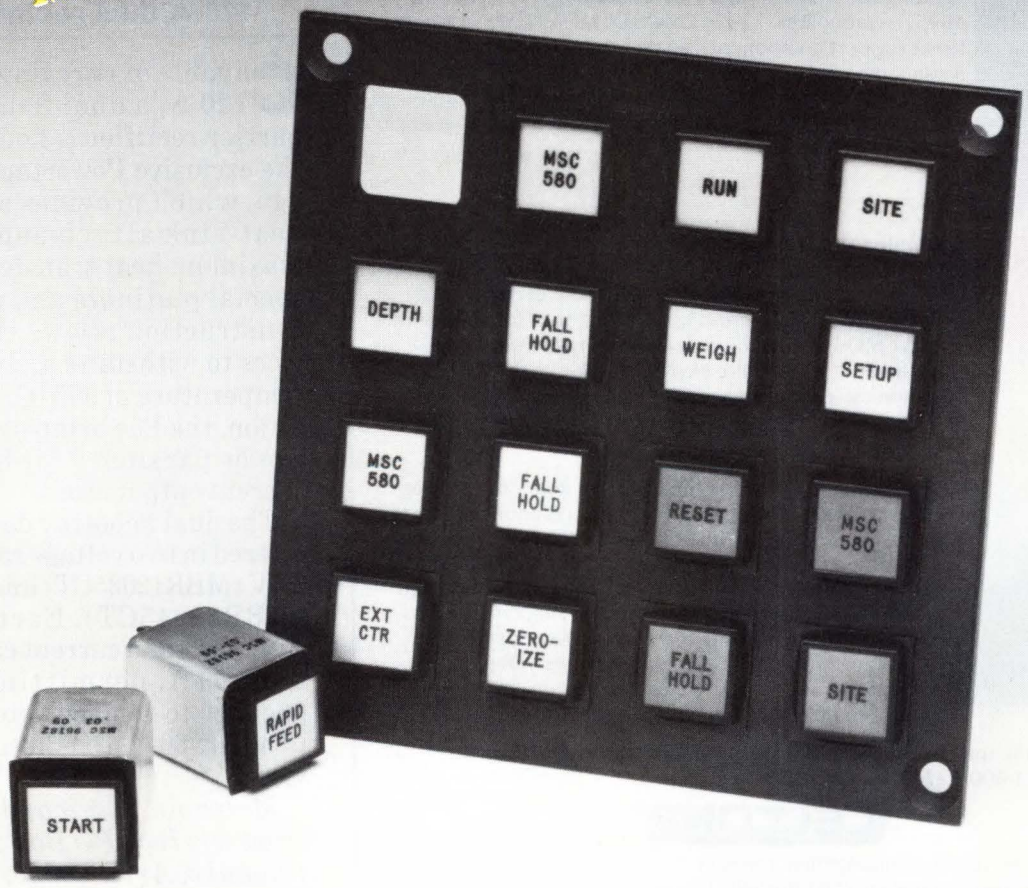


EATON

Eaton Corporation, Aerospace & Commercial Controls Division, MSC Products, 1640 Monrovia, Costa Mesa, CA 92627, Phone (714) 642-2427, Telex 678-433. Europe: Produktieweg 123, P.O. Box 304, 1520 AH Wormerveer, The Netherlands, Phone 075 28 06 01

CIRCLE 221

POWER

UPS is ⅓ the size of standard UPS units

The compact, bipolar-transistorized UPSjr., a down-sized uninterruptible power supply, packs 750 VA, 1.25 kVA, or 2.5 kVA of power into one-third the volume of standard UPS models and is 20% to 30% lower in cost. The on-line reverse transfer system provides complete power protection to sensitive electronic equipment with zero-delay transfer times. Transients are suppressed, voltage is regulated during brownouts, and continuous power is supplied to the load during power outages. Moreover, the desk-high UPSjr. is whisper quiet—producing less than 55 dBa. Though compact in size, it includes the features and performance of a full-sized UPS.

Clary Corp., 320 W. Clary Ave., San Gabriel, Calif. 91776; (818) 287-6111.

CIRCLE 332

'Powertap' case enhances 120-A dual rectifiers

Capable of carrying up to 120 A, a dual Schottky barrier rectifier is housed in the exclusive Powertap package, which provides secure heat-sink attachment and maximum heat transfer. The special platinum and nickel construction allows the devices to withstand a junction temperature of 175°C. In addition, the Powertap package can be paralleled for higher current output uses.

The dual Schottky device is offered in two voltage ratings: 35 V (MBR12035CT) and 45 V (MBR12045CT). Each rectifier leg has a current capacity of 60 A, permitting the package to replace two independent 60-A DO-5 stud devices.

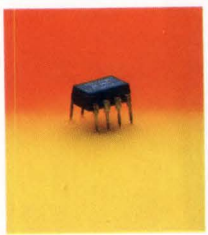
Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 244-4284. $16.15 (35 V) and $18.95 (45 V) (100 units); stock to four weeks. **CIRCLE 333**

Teltone IC's

Covering the full spectrum of your telecommunications needs.

Solve your telecommunications design problems with Teltone's complete family of telecom IC's. You'll find innovative, up-to-the-moment single-chip and hybrid generators, detectors, receivers and relays — all backed by Teltone's commitment to performance, reliability and quality.

Leading the industry in DTMF technology. Consider the M-957, a monolithic 22-pin CMOS DTMF receiver. It needs fewer support components, so designs can be simple and use a minimum of space. The new M-958 is a hybrid PCM-compatible DTMF receiver that is dial tone immune and packs μ-Law or A-Law PCM input at up to 3 MHz into a single 22-pin package.



Designing the *first* call progress IC's. Need to monitor for or generate dial tone, circuit or station busy, audible ringing and other call routing tones? Take a look at our exciting 8-pin CMOS M-980 Call Progress Tone Detector or our unique new 14-pin CMOS M-991, the only Call Progress Tone *Generator* on the market. If you require *precise* detection of the four common call progress tones (350, 440,480 and 620 Hz), Teltone has a 22-pin CMOS solution for you called the M-982.

A reputation for telecom innovations. Rounding out our complete family of telecommunications components are the M-949 Line Sense Relay and the M-959 Dial Pulse Counter and Hook Status Monitor. The M-949 is a small PWB-mount loop current detector that, when connected to the tip and ring voice pair of an ordinary telephone line, responds to currents of 18-125 mA with a 1 form A relay closure. The low-cost, low-power CMOS M-959 features independent hook status monitoring and includes time-guarded dial pulse counting and pin-selectable dialing speeds of 10 or 20 PPS.

For more information on components from the leader in telecom technology, call Teltone today: **1-800-227-3800, ext. 1130.**

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Teltone Corporation, the telecommunications company. P.O. Box 657, Kirkland, WA 98033. In the east call: Teltone Corporation, (904) 262-6910. In Canada, contact: Teltone Ltd., 183 Amber Street, Markham, Ontario L3R 3B4, (416) 475-0837.

CIRCLE 222

POWER

Servo amp offers two current/voltage ratings

Providing greater flexibility in selecting a servomotor, the Series 1000 pulse-width modulated amplifier offers two current and two voltage ratings. These include 15 to 25 A dc, with continuous current of 10 to 20 A dc, and maximum bus voltage of 200 to 350 V dc. Horsepower ratings are from 2 to 8 hp. The servo amplifier is supplied as a system, with plug-in circuit boards that can be easily interchanged. Up to eight individual axis drives can be operated from the integrated dc power supply. A group of modules may be connected in parallel to obtain higher current ratings and different power combinations. Protection features include LED fault indicators and an adjustable current limit, as well as overvoltage and -temperature sensing.

Unico Inc., 3725 Nicholson Road, Franksville, Wis. 53126; (414) 886-5678.

CIRCLE 334

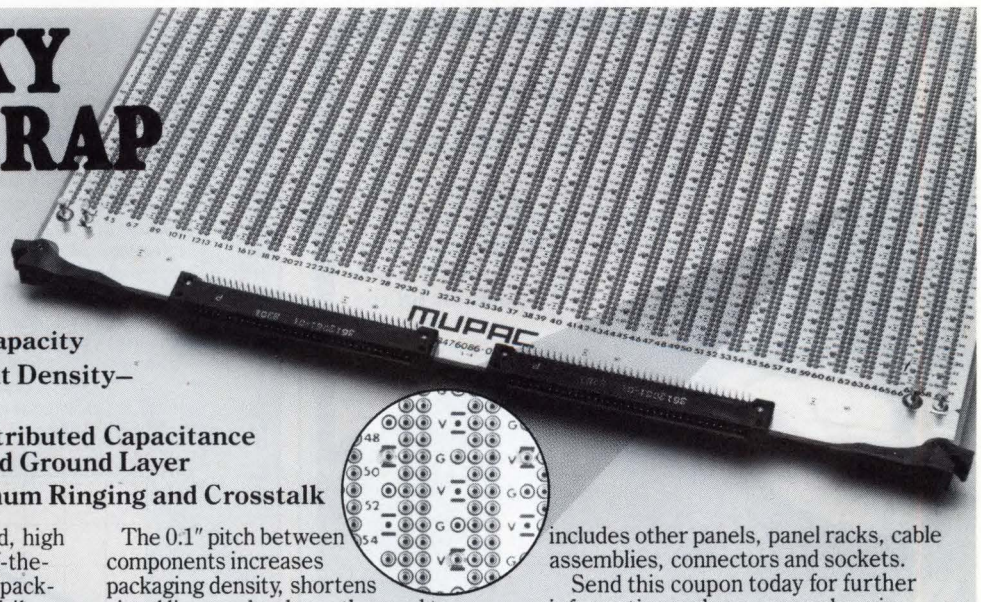
Power supply fits add-on disk drives

Designed for use in add-on disk drive systems, the Model LR1029 dual-output power supply delivers 5 V at 3 A for controller logic circuits and 12 V at 1.5/2.5 A for spindle-drive and head motors. The total variation on both outputs is ±5%, including load and line regulation, as well as centering and cross regulation. The input voltage range, which is jumper-selectable, is 90 to 132 or 180 to 264 V. The card's small size of 3.5 by 5.5 in. makes it suitable for a wide variety of mass-storage packages, including full- and half-height floppy- and hard-disk drives, streaming tape units, and removable media systems.

California DC, 2150 Anchor Court, Newbury Park, Calif. 91320; (805) 499-3621. $33 (1000 units); two to four weeks.

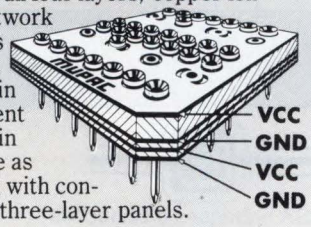
CIRCLE 335

SCHOTTKY WIRE WRAP PANELS



- Four-Layer Multilayer Construction
- 60% Higher Current Capacity
- 30% Higher Component Density– Up to 480, 16 Pin Dips
- Ten Times Greater Distributed Capacitance Between VCC Layer and Ground Layer
- High Shielding–Minimum Ringing and Crosstalk

These patent pending, high speed, high current panels are a true state-of-the-art advance in wire wrap system packaging. On all four layers, copper foil lattice network surrounds every pin, resulting in a 60 percent decrease in resistance as compared with conventional three-layer panels.



The 0.1" pitch between components increases packaging density, shortens signal lines and reduces the need to interconnect through the backplane, thereby minimizing crosstalk, ringing and propagation delays.

The four-layer construction has a component side VCC layer plus a second VCC layer sandwiched between two closely spaced ground layers. Available in five sizes, Schottky panels are part of the total Mupac IC packaging family which also includes other panels, panel racks, cable assemblies, connectors and sockets.

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CIRCLE 223

COMPUTER BOARDS

Multibus board mixes features

A Multibus-compatible single-board computer gives users a high degree of flexibility. It affords designers, for the first time on one board, a choice of an 8-MHz 68000 or a 10-MHz 68010 CPU, memory management, and iSBX connectors.

For the memory management, the MultiSBC 68K, from Ackerman Digital Systems, accepts Motorola's MC68451 MMU chip, enabling it to translate addresses for the 68000's full 16-Mbyte address space.

The board's two iSBX connectors permit direct memory access, using either two or four channels. They handle both 8- and 16-bit data paths, accommodating a variety of devices with either serial or parallel I/O.

The card has room for up to 16 dynamic RAMs, a total of 512 kbytes if 256-kbit RAMs are used. When memory demands are not critical, 64-kbit RAMs will suffice at lower cost.

Optional piggyback daughter boards let users add battery backup or quadruple RAM. Dual ports make the memory accessible to either the CPU or off-card processors.

Six ROM slots hold up to 192 kbytes of program storage, enough for C programs. The minimum ROM configuration is 48 kbytes.

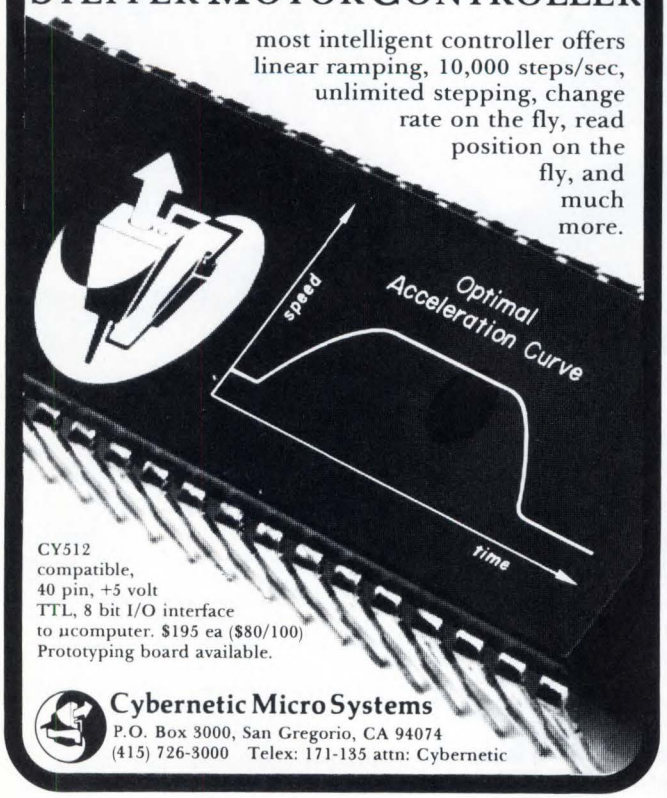
Standard features include a real-time clock-calendar with 50 bytes of battery-backed RAM, a programmable LED indicator, 27 vectored interrupts, and automatic external and built-in collision detection.

In the minimum setup, the MultiSBC 68K lists for $995. Prototypes will be available in October.

Ackerman Digital Systems Inc., 216 West Stone Court, Villa Park, Ill. 60181; (312) 530-8992. **CIRCLE 307**

NEW CY525 3rd generation
STEPPER MOTOR CONTROLLER

most intelligent controller offers linear ramping, 10,000 steps/sec, unlimited stepping, change rate on the fly, read position on the fly, and much more.



CY512 compatible, 40 pin, +5 volt TTL, 8 bit I/O interface to µcomputer. $195 ea ($80/100) Prototyping board available.

Cybernetic Micro Systems
P.O. Box 3000, San Gregorio, CA 94074
(415) 726-3000 Telex: 171-135 attn: Cybernetic

CIRCLE 224

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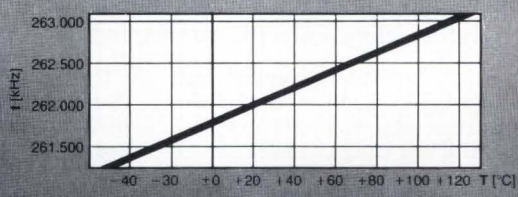
- *Operating temperature range −55°C to +125°C*
- *Simple circuit design*



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Th-2/84ETA

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Quartz Division
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ETA Industries Inc.
608 Fifth Avenue, New York, N.Y.10020, Tel. 212-307-5276, Telex 239865

CIRCLE 225

RF switches

10 to 2500 MHz from $19.95 PSW 1211 (500 qty.)

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No waiting, immediate delivery . . . with one year guarantee. Call or write for 64-page, catalog or see our catalog in the Gold Book, EBG, EEM or Microwaves Product Data Directory.

SPECIFICATIONS for PSW 1111 (SPST) **and PSW 1211** (SPDT)

FREQUENCY RANGE	10-2500 MHz
INSERTION LOSS	
10-2000 MHz	1.7 dB max.
2000-2500 MHz	2.7 dB max.
ISOLATION	
10-500 MHz	40 dB min.
500-1000 MHz	30 dB min.
1000-2000 MHz	25 dB min.
2000-2500 MHz	20 dB min.
SWR	1.5 max. ("on" state)
SWITCHING SPEED	1 μsec. (max.)
MAXIMUM RF INPUT	+20 dBm
CONTROL	+5 V (5 mA max.)
OPERATING TEMPERATURE	−54°C to +100°C
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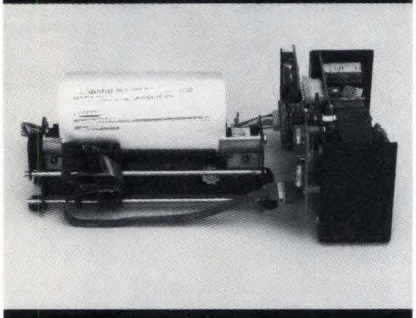

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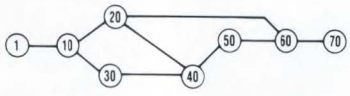
At 3 lps and 48 characters/line nominal, the DC-4004A throughout is 144 cps. Or use the other versions doing 80 columns per line (compact font) or 120 dot/in. graphics on the 4¾" paper. The DC-4004A is available alone at $120 ea. (500's); or with a parallel or serial (110-9600 bps) ram buffered interface at $205 (500's)*. This archival electrosensitive, dot matrix printer is only 2⅝" tall (paper mounted).

Call or write NOW: HYCOM, 16841 Armstrong Ave., Irvine, CA 92714 — (714) 557-5252

*Power supply available extra.

HYCOM

CIRCLE 227



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CIRCLE 228

COMPUTER BOARDS

Q-bus board offers 128 kbytes of RAM

Compatible with DEC LSI-11 microprocessors, the LM1164 memory board provides up to 128 kbytes of CMOS static RAM with a minimum data-retention time of two months. An optional lithium battery extends retention time to a minimum of two years, while automatic memory-protection logic completes the self-contained nonvolatile memory system. The Q-bus board uses 8k-by-8 memory chips and has a typical access time of 247 ns. It also features a jumper-selectable starting address on 4-kword boundaries and memory write protection on 8-kword boundaries.

Diversified Technology Inc., PO Box 748, Ridgeland, Miss. 39157; (601) 856-4121.

CIRCLE 336

Graphics card offers programmed I/O, DMA

Compatible with Multibus standards, the VM-8851 color graphics processor combines DMA and programmed I/O functions for optimized communications. It also utilizes an 8088 CPU to rasterize display list commands, which results in an intelligent graphics engine with drawing speeds of up to 25 million pixels/s. Using 256k RAM devices, the 512-kbyte display RAM expands to 2 Mbytes. Multiple virtual-image size options include up to eight buffers and a 1k-by-1k image space. The processor simultaneously displays 256 colors—chosen from one of four 4096-color palettes—on a 512-by-512- or 640-by-480-pixel programmable screen format. The VM-8851 is equipped with an iSBX connector and the Interact graphics command interpreter.

Vermont Microsystems Inc., 1 Main St., PO Box 236, Winooski, Vt. 05404; (802) 655-2860. $3500 (OEM discounts available). **CIRCLE 337**

STD bus RAM board stores 128 kbytes

The 6210 dynamic RAM board is an STD bus-compatible memory board with 128 kbytes of parity-checked storage. The memory board contains interrupt control logic that is compatible with a variety of processors, including the 8085, Z80, 6809, and 6502. Multiple boards can be used in one system to increase the storage capacity to a maximum of 16 Mbytes.

The 6210 has on-board bank-select logic for mapping the processor's memory space into eight 16-kbyte segments. It also features a dynamic RAM controller that refreshes the 64k chips independently of the CPU. The board can be configured to generate "hidden" refresh cycles that occur between memory cycles to avoid degrading the throughput of the processor.

Systek, 1023 N. Kellogg St., Kennewick, Wash. 99336; (509) 735-1200. $465.

CIRCLE 338

COMPUTER BOARDS

Fast analog I/O board suits DSP applications

With 12-bit resolution and a total throughput time of 3 μs/channel, the MPV950 analog input board is suitable as a front end for digital signal processing systems. The VMEbus-compatible board offers 16 single-ended inputs or 8 single-ended inputs and eight user-configurable channels. The latter can be used for current input, single-ended input, or differential input with resistor-programmable gains of 1 to 10. The MPV950 uses the high-speed ADC803 12-bit a-d converter (1.5-μs conversion time) and the high-speed SHC803 sample-and-hold amplifier (250-ns acquisition time). A front-panel LED indicates if sampling speed has exceeded the capabilities of the converter. High- and low-level input signals range from ±5 V to ±500 mV, 0 to +10 V, or 0 to +1 V.

Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; (602) 746-1111. **CIRCLE 339**

Cache memory optimizes hard-disk controller

Capable of supporting two ST-506 5¼-in. Winchester disk drives, the Model STDC controller enhances system performance through the use of five 10-kbyte tracks of cache memory. One of these tracks is a dedicated verification buffer, which is used to verify data after it is written to the disk. The remaining four tracks allow the STDC to reserve separate caches for several users or processes, or for source and destination data in transfer operations. System performance is improved by reducing the number of disk accesses that the system has to make. Disk transfers are handled by the S-100 bus-compatible, Z80A-based controller at 5 Mbits/s.

Cromemco Inc., 280 Bernardo Ave., PO Box 7400, Mountain View, Calif. 94039; (415) 964-7400. $795; stock.

CIRCLE 340

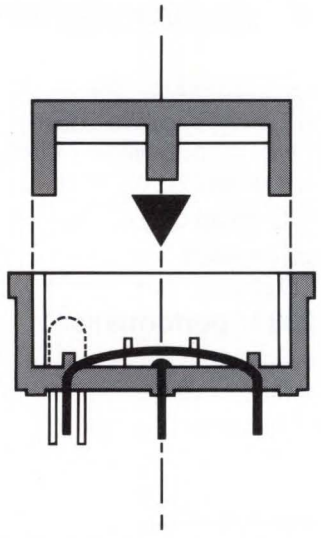
Graphics controller displays 16 colors

Compatible with the STD bus, a high-resolution color graphics controller is capable of displaying up to 576 by 432 pixels in 16 colors on a standard RGB monitor. The two-card module, designated the GRX-8401/2, appears to the bus as one command/data port and one status port. A Z80A processor handles bus interfacing and the processing of graphics parameters, while an NEC 7220 graphics display controller generates vectors and arcs and performs video-memory management. Resident firmware interprets English language commands for drawing lines and arcs, performing polygon fill, and creating text. The controller also features an on-board compiler.

Bytewyse Technology, 4710 University Way NE, Seattle, Wash. 98105; (206) 547-2920. $895 (first unit only).

CIRCLE 341

Feel and hear switch click millions of times



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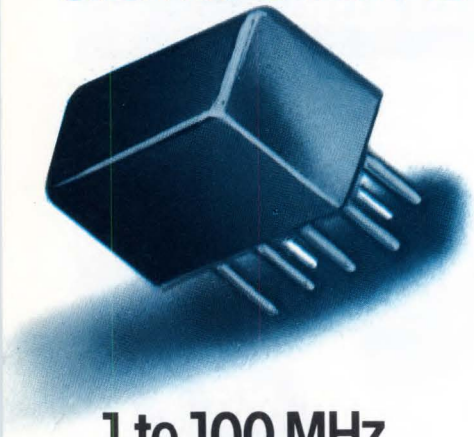

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FREQUENCY RANGE	
L and R ports	1-100 MHz
Output ports	DC-60 MHz
SCALE FACTOR	8 mV/Degree
IMPEDANCE	
L and R ports	50 ohms
I port	500 ohms
L AND R SIGNAL LEVELS	+7 dBm
ISOLATION, L-R	40 dB min.
MAXIMUM DC OUTPUT, mV	1000 mV typ.
DC OUTPUT POLARITY	Negative
DC OUTPUT OFFSET	0.2 mV typ.

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C101-3 REV. ORIG.

CIRCLE 230

COMPONENTS

Thin-film RTD responds quickly

Mounted in a TO-220 package for ease of operation, the TD3A resistance temperature detector (RTD) has a typical response time of two seconds in liquid. The sensing element is a 40-by-50-mil silicon chip, onto which has been patterned a thin-film resistive network. Chips are trimmed to provide 2000 Ω of nominal resistance at room temperature. Requiring no calibration, the TD3A is accurate to within ±0.7°C at 20°C. It also has a sensitivity of 8 mV/°C with 1 mA excitation and an inherently near-linear output. The maximum error over the full operating temperature range of −40° to +150°C is within ±2.5°C.

Micro Switch, 11 West Spring St., Freeport, Ill. 61032; (815) 235-5731. $1.09 (quantity orders).

CIRCLE 342

Surface inductors suit pick-and-place robots

Priced at less than $1 in quantities of 25,000, a line of surface-mounted inductors is suitable for vacuum pick-up and handling by robotic pick-and-place systems. The SMI-200 series is offered in two package sizes —0.215 by 0.215 in. and 0.400 by 0.400 in., with a maximum height of 0.250 in.—and with inductance values ranging from a few microhenries to several hundred microhenries. The device, which has an operating temperature range of −40° to +70°C, is capable of enduring a humidity level of 80% RH at 85°C for 250 hours and thermal shocks between −40° and +70°C for up to 20 cycles. Furthermore, the SMI-200 withstands solder reflow and detergent washing processes.

West-Cap Arizona, SFE Technologies, 2201 E. Elvira Road, Tucson, Ariz. 85706; (602) 294-2646. CIRCLE 343

Surface-mount diodes are hermetically sealed

A variety of hermetically sealed diodes are suitable for surface mounting and immersion soldering. The BAS32, BAV100-103, and BZV55 devices are leadless diodes encapsulated in a cylindrical glass package that is 1.6 mm in diameter and 3.5 mm in length.

The BAS32 is a high-speed switching diode for use in fast logic circuits. The BAV100, 101, 102, and 103 are general-purpose diodes intended for switching applications in industrial equipment, such as oscilloscopes and DVMs. Finally, the BZV55 series of voltage-regulating diodes covers the range of 2.4 to 75 V.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.

Amperex Sales Corp., Providence Pike, Slatersville, R.I. 02876; (401) 762-9000.

CIRCLE 344

COMPONENTS

Thin EL display suits portable applications

Designated the MDM 512.256-11, an electroluminescent display module is intended for electronic systems where portability is required and space is at a premium. The solid-state display panel and an electronic board with the required high-voltage drivers are housed in a 5.67-by-10.2-in. package that is only 0.37 in. thick. With a resolution of 512 by 256 pixels, the module is capable of displaying a full 25 lines of 80 characters each or high-resolution graphics. Crisp and stable images are produced in a pleasant yellow color.

Finlux Inc., 20395 Pacifica Drive, Suite 109, Cupertino, Calif. 95014; (408) 725-1972. $700 (1000 units); samples are available now, with volume production to begin in the fall.

CIRCLE 345

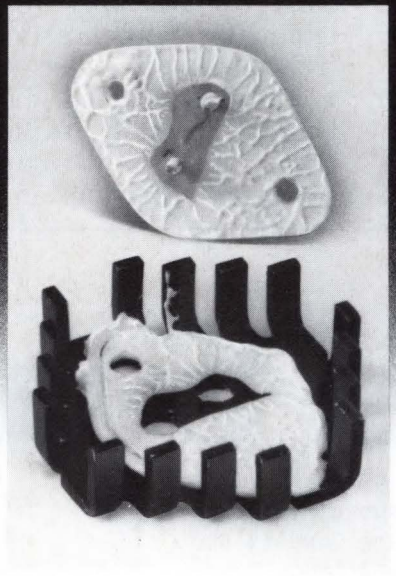
Rotary-lever switch is only 1½ by 3 in.

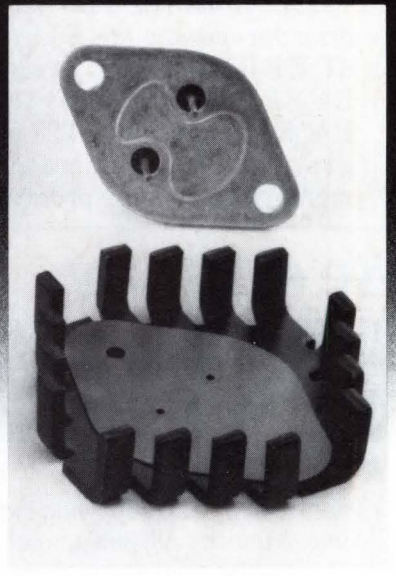
The compact size of a rotary-lever limit switch—which is only 1½ in. wide and 3 in. high—makes it particularly adaptable for downsized machinery and equipment. The miniature switch, designated the MS04S01-00, has a unique head-mounting design, with holes near the lever shaft that virtually eliminate the effects of torque and vibration. An epoxy compound is used to encapsulate both the electrical connections and the zinc die-cast housing, and gold or silver contacts can be provided. Gold cross-point contacts, suitable for low-level logic switching, offer longer life, obtain positive contact with a force of 5000 psi, and have an initial resistance below 50 mΩ.

Gould Inc., Industrial Controls Division, 100 Relay Road, Plantsville, Conn. 06479; (203) 621-6771.

CIRCLE 346

Greasework Guesswork SIL-PAD®





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CIRCLE 231

PACKAGING & PRODUCTION

Robot automates simple, mundane tasks

Small and low-cost, the Alpha II production robot system performs simple assembly tasks, particularly those that are repetitive or dangerous. The five-axis articulated robot arm, which has an 18-in. reach, moves at selectable speeds up to 51 in./s and carries a maximum payload of 3 lb. Repeatability is within ±0.015 in. for payloads up to 1½ lb.

The Alpha II's 8-bit 6502A microprocessor has 8 kbytes of EPROM, 4 kbytes of EEPROM, and 1 kbyte of RAM. It stores up to 227 program steps in permanent memory and can be programmed through a hand-held teaching pendant or an external computer via an RS-232-C asynchronous serial interface.

Microbot Inc., 453-H Ravendale Drive, Mountain View, Calif. 94043; (415) 968-8911. $13,425. **CIRCLE 347**

Robot randomly places nonstandard components

Featuring a Seiko RT-3000 dc servo-driven robot, the ECA 101 assembly system eliminates hand insertion of irregularly shaped components into printed circuit boards. The end effector of the robot system compensates for variations in the body-to-lead orientation of irregularly shaped components, enabling it to handle standard and nonstandard parts ranging from 0 to 1½ in. in size. Components may be randomly placed with spacings as little as 0.05 in. The standard work cell measures 46 by 53 in. and is also available in an 84-by-84-in. configuration. The ECA 101 includes the end-effector system, the robot, software, and a base. Parts feeding stations may be provided, depending upon the application and the user's requirements.

Chad Industries, 1060-K N. Batavia St., Orange, Calif. 92667; (714) 997-4350. Between $45,000 and $55,000.

CIRCLE 348

We sell Hybrid Solutions.

For years we've been supplying industry with hybrid solutions to their circuit design problems. Our thick-film hybrids are used in Oil Logging Instrumentation, Telecommunications, Computers, Medical Electronics, and by the Military in airborne, satellite, missile, and fuze applications to MIL-STD-883.

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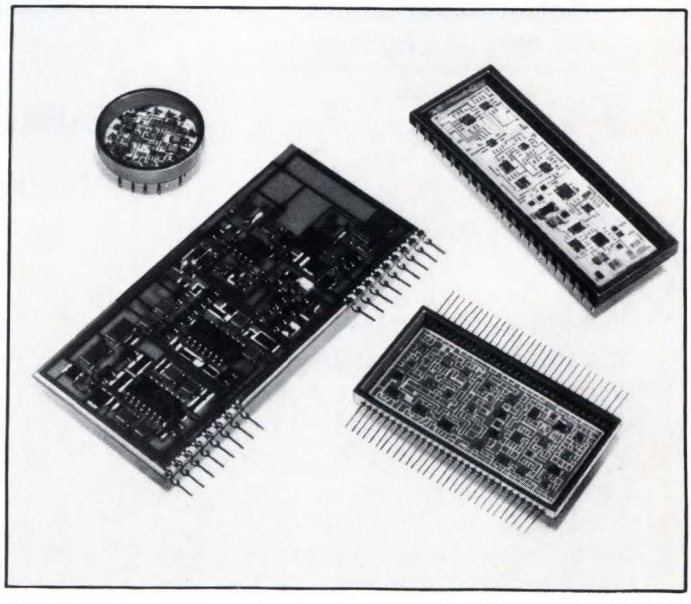

White Technology, Inc.

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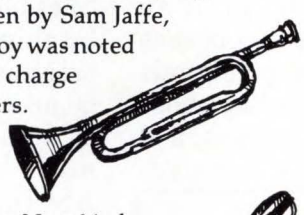
CIRCLE 232

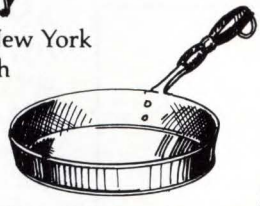
TAKE THE DIN QUIZ!

How Much Do You Really Know About DIN?

1 Immortalized in poetry by Rudyard Kipling, and portrayed on the screen by Sam Jaffe, this famous Indian water boy was noted for his courage during the charge of the British Sepoy Lancers.

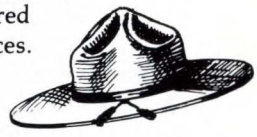


2 Name the famous district in New York City commonly associated with musicians and composers.



3 Name the powerful, 1958 Tennessee Williams drama in which Elizabeth Taylor wore fetching slips, Paul Newman's pajamas matched his eyes, and Big Daddy Burl Ives looked sweaty in a rumpled white suit.

4 During the 50s and 60s, a warmhearted tale of a boy and his dog captured the hearts of television audiences. Name the dog who assisted in maintaining law and order in the early west.



5 Name the popular Dashiell Hammett novel which was made into a movie starring William Powell, as the ultimate nonchalant criminologist and Myrna Loy, as his trouble-prone wife.

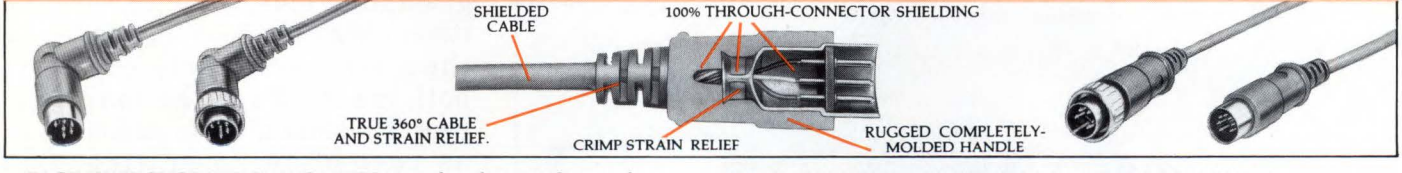
6 In this famous 1967 movie, two diverse families sit down face to face to consider a rather unsettling situation. Starring Sidney Poitier, this urbane and stylish comedy was Spencer Tracey's last movie.

If you answered any or all of the above questions, you definitely qualify for Switchcraft DIN Connector and Cable literature and samples. Fill in the coupon below, or if you can't wait a moment longer, call Mr. Dean Arvantis at (312) 792-2700, our DIN expert.

Answers to Quiz:

1) Gunga DIN, 2) DIN Pan Alley, 3) Cat on a Hot DIN Roof, 4) Rin DIN DIN, 5) The DIN Man, 6) Guess Who's Coming to DIN-DIN.

Some famous facts about Switchcraft DIN connectors and cables



FACT: SWITCHCRAFT CUSTOMIZES. Switchcraft can make exactly what you need when you need it. Whether it's color, wire size, type of shielding, or molding in your company logo—Switchcraft has complete custom design capabilities to match your equipment or define your corporate identity.

FACT: SWITCHCRAFT CONNECTORS—QUALITY TESTED. Switchcraft's shielded connectors are effective ways to make your computers comply with the FCC's Electro-Magnetic Interference (EMI) regulations. Fully address FCC 29780 Docket.

FACT: SWITCHCRAFT SHIELDED CONNECTORS ARE DESIGNED TO CONTROL INTERFERENCE. Switchcraft shielded connectors will "bleed off" EMI/FRI—virtually eliminating annoying glitches, memory loss or possible damage to CPU components.

FACT: SWITCHCRAFT OFFERS A LARGE SELECTION OF CONNECTORS AND CABLES. Switchcraft offers a broad line of DIN Connectors/Receptacles/Cables; male-female, straight or right angle, push-on or locking, 8 different pin/contact configurations. Plus, an exclusive one piece shield design reduces costly assembly.

FACT: SWITCHCRAFT DESIGNS REDUCE CABLE FATIGUE AND WIRE FRACTURING. Four-way flex relief relieves strain in up/down or side to side motion.

FACT: SWITCHCRAFT PROVIDES THE OPTIMUM SOLUTION TO YOUR SPECIFIC DIN CONNECTOR AND CABLE DESIGN REQUIREMENTS.

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CIRCLE 233

INSTRUMENTS

GPIB interface unit has 80 TTL I/O lines

The System 488 digital I/O interface unit for the GPIB (IEEE-488 bus) enables up to 80 bits of TTL-level data to be read or output by a bus controller. The 6809-based unit interfaces most types of digital signals with the bus, including those for relays, indicators, a-d converters, and BCD instruments. Additional signal lines for service request, data latching, handshaking, and triggers are also included. Operating parameters, such as data format (binary, decimal, hexadecimal, and ASCII), port selection, polarity, and bus terminators, are software-programmable by the controller. The System 488 offers three expansion ports.

IOtech Inc., PO Box 21204, Cleveland, Ohio 44121; (216) 321-0609. $895; eight weeks. **CIRCLE 349**

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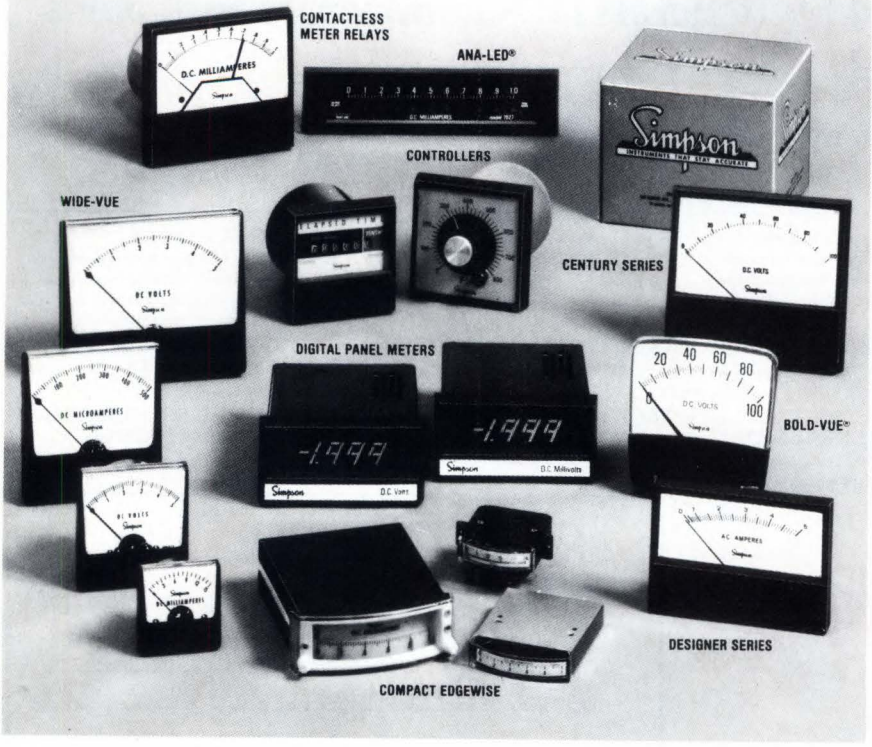


CIRCLE 234

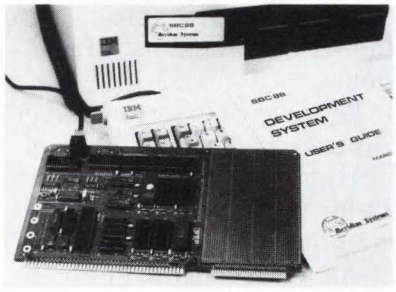
Card links IBM PCjr with IEEE-488 bus

Transforming the IBM PCjr into an IEEE-488 instrument controller is an interface card that includes software designed for optimum performance and ease of use. Since the user can program functions using primitive or high-level commands, the system is attractive to both the OEM and the end-user. The software is installed as part of the operating system—PC-DOS 2.0 or later—so that the operating system can manage the interface bus. Application software can be written in Interpretive Basic, Compiled Basic, Fortran, SuperSoft Fortran, Pascal, Lattice C, or Assembly languages.

National Instruments, 12109 Technology Blvd., Austin, Texas 78727; (800) 531-5066 or (512) 250-9119. $385 (interface card), $75 (software), and $50 (language options). **CIRCLE 350**

INSTRUMENTS

Board turns IBM PC into development system



The SBC88 is a Multibus-compatible single-board computer that enables the IBM PC to function as an 8088 development system. Since most projects require specialized interface circuitry, a 4-by-6-in. wire-wrap area is included on-board. The SBC88 development system includes an 8088 central processing unit with pseudo-static RAM, latched and buffered interface signals, a monitor PROM, an RS-232-C port, and a parallel interface adapter that provides 24 general-purpose I/O lines. It also includes three counter/timer channels and eight interrupt lines.

The PROM-based monitor software performs hardware initialization, handles the communications interface with the IBM PC, provides utility routines, and supervises debugging. The diskette-based monitor allows communications with the target hardware for downloading and uploading files, and it performs full-function debugging and user-transparent communications with the IBM PC-DOS.

Assembly language programs can be written on the PC using any editor and assembled directly into downloadable files with the supplied assembler. Programs can also be written using commercially available compilers, like Pascal or C, compiled, linked, and converted into absolute files for downloading.

Meridian Systems, 321 Aviador St., Suite 111, PO Box 3034, Camarillo, Calif. 93011; (805) 484-8696. $500; stock to 45 days.

CIRCLE 351

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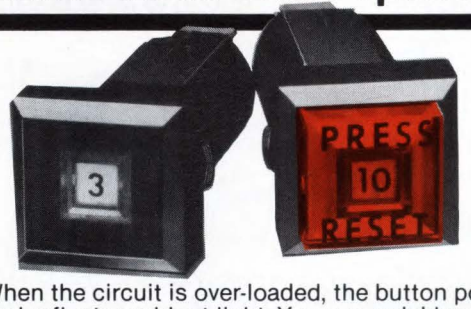
CIRCLE 235

The technology behind this circuit protector came from outer space.



When the circuit is over-loaded, the button pops out and reflects ambient light. You can quickly see that a failure has occured.

Fuse holder size Amlit™ circuit protector snaps into both round and square mounting holes. It is UL and CSA recognized. Standard button colors are red and Dayglo orange.

Forty years of innovation like this have earned us a place in outer space, on the Columbia. And we put the same kind of effort into your economical, down-to-earth applications.

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CIRCLE 236

COMPUTER SYSTEMS

IBM 3270 look-alike runs PC software

An intelligent workstation for IBM 3270 users, the Model 1186 is designed to run most IBM PC software. The 80186-based system operates as either a stand-alone local processor, under the MS-DOS operating system, or as an on-line 3270 display station for host interaction. In addition to supporting a monochrome display, the 1186 has built-in support for a color monitor as well.

The 1186 is offered with either two double-sided, double-density floppy-disk drives, each with a capacity of 360 kbytes, or with a 10-Mbyte hard-disk and a single floppy-disk drive. Main memory ranges from 128 kbytes of RAM and 32 kbytes of ROM to 512 kbytes of RAM.

Telex Computer Products Inc., 6422 E. 41st St., Tulsa, Okla. 74135; (918) 627-1111. From $3025. **CIRCLE 352**

32-bit mini boasts price/performance

A line of 32-bit minicomputers uses custom chips to deliver twice the performance and four times the storage of present machines at two-thirds the price. The Astra 300 series, which starts at less than $15,000, supports as many as 32 workstations. Since it is software-compatible with the Astra 200 series, existing applications run faster and without alteration.

The price/performance advantage is attained by combining a custom-designed 32-bit VLSI CPU with virtual memory segmentation, creating an execution environment without memory constraints. The top-of-the-line Astra 370 VS system has 1024 kbytes of main memory, expandable to 4096 kbytes, and a maximum fixed-disk storage capacity of 1 Gbyte.

NEC Information Systems Inc., 1414 Massachusetts Ave., Boxborough, Mass. 01719; (617) 264-8000.

CIRCLE 353

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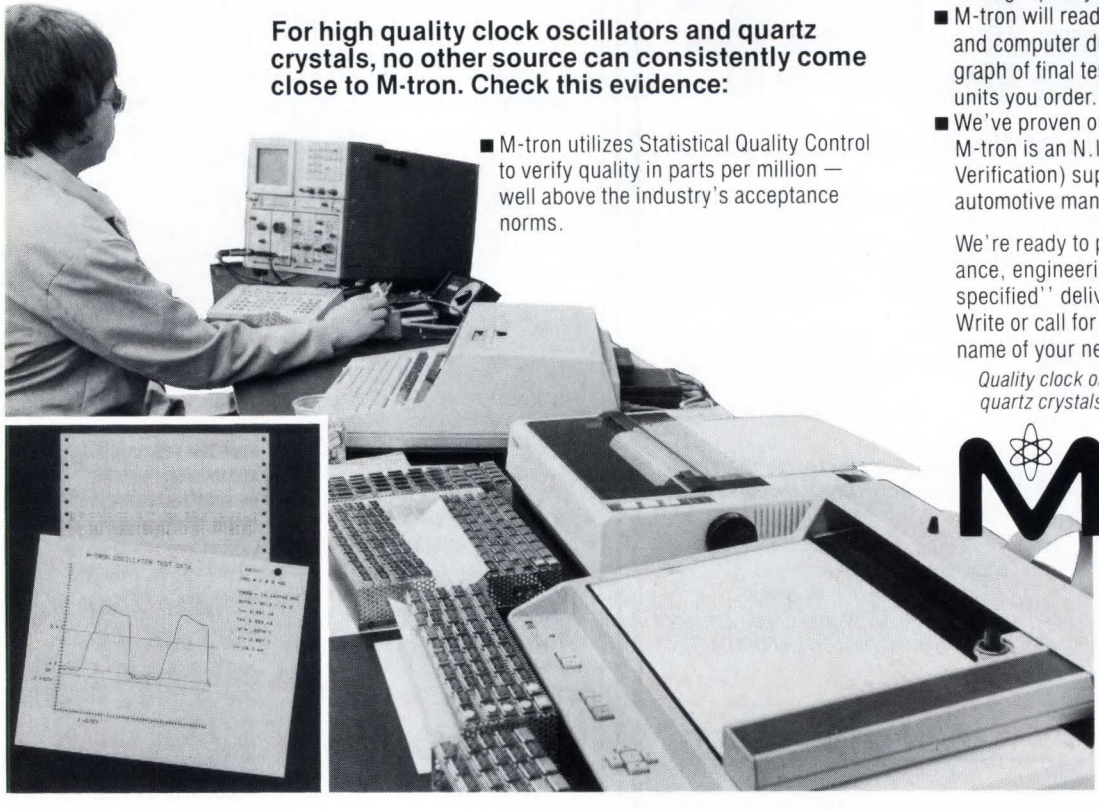

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MI-45

CIRCLE 237

COMPUTER SYSTEMS

Unix-based mini sits on desktop

Berkeley's 4.2 version of Unix is at the heart of the U! technical workstation, a personal minicomputer in a compact desktop design. The system offers more than 250 utilities including line and screen editors, stream editing, document preparation tools, data manipulation, and a variety of office automation aids. The workstation is based on an 8-MHz 68010 microprocessor and features demand-paged virtual memory.

Programming languages available for the U! computer include C, Fortran-77, Pascal, Lisp, and Assembly. Standard features include 1 Mbyte of memory, a 640-kbyte diskette drive, a 22-Mbyte hard-disk drive, two RS-232-C interfaces, and one parallel interface.

NBI Inc., PO Box 9001, Boulder, Colo. 80301; (303) 938-2795. $15,495. **CIRCLE 354**

Industrial computer is PC XT-compatible

Compatible with the IBM PC XT, the ISI 6160 is packaged specifically for industrial environments. The system comprises an 8088 CPU, 128 kbytes of RAM, a a floppy-disk controller, a 125-W power supply, and a cooling fan. Disk storage consists of one or two double-sided, double-density 5¼-in. drives and optional 10-, 20-, or 30-Mbyte Winchester drives. Two RS-232-C serial ports and one parallel printer port are available on the rear panel. The computer may be custom-configured for analog or digial industrial I/O via its five expansion slots.

The ISI 6160 is housed in a standard 19-in. rack-mounted enclosure and is delivered with MS-DOS and GW Basic. It is also compatible with Concurrent CP/M.

ISI International Corp., 1275 Hammerwood Ave., Sunnyvale, Calif. 94089; (408) 743-4300. **CIRCLE 355**

Workstations boast supermini performance

Based on the Eclipse MV/4000 computer, two engineering workstations offer high-resolution graphics, built-in Ethernet IEEE-802.3 support, and integrated peripherals. The DS/4000 and DS/4200 systems both run under the Advanced Operating System/Virtual Storage (AOS/VS) and a native Berkeley Unix operating system.

The DS/4000 comes with an integrated 1024-by-1024-pixel monochrome graphics system, while the DS/4200 is offered with a similar high-resolution color graphics system. Both are available in main memory configurations of 1, 2, or 4 Mbytes and support local mass storage capacities of 77.2 Mbytes.

Data General Corp., 4400 Computer Drive, Westboro, Mass. 01580; (617) 366-8911. From $35,500 (DS/4000) and from $44,500 (DS/4200).

CIRCLE 356

GP-IB
programmable simulation of transducers
± 4 to 20mA, 10 to 50mAdc
thermocouples
± 0.1μV to 10.0Vdc
and calibration to
± 1000V & ± 100mA

Stability and accuracy are guaranteed with EDC's new Programmable DC Voltage and Current Calibration Standard

Model 520A is:
- Accurate (±0.002%) — guaranteed for one year.
- Highly stable (±20 ppm for 12 months)
- Extremely versatile in voltage and current modes

Voltage range: ± 100mVdc resolved to 0.1μV; ± 10Vdc resolved to 10μV; ± 100Vdc resolved to 100μV

Current range: ± 10mAdc resolved to 0.01μA; ± 100mAdc resolved to 0.1μA (± 100V compliance with variable limit)

- Programmable with zero "crowbar" reference
- GP-IB IEEE-488 (1978) programmable
- Priced at $2450 (1000Vdc range optional $525)

The 520A is ideally suited for the following applications:
- Calibration of DVMs, DMM, meters, chart recorders, A/D converters, ATE, monitors, controllers, logging systems, etc.
- Simulation of thermocouples and strain gages. (4 to 20 mA and 10 to 50 mA) + other transducers. Note: compliance voltage up to 100Vdc.
- Linearity check of amplifiers and function modules.

For more information call Bob Ross
Engineering representatives throughout the U.S.A., Canada and Mexico. Distributors in Europe and selected countries throughout the world.

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CIRCLE 238

MATERIALS

Adhesive bonds hybrid circuits

A silk-screenable adhesive, called Eccobond 282, provides secure, thermally conductive bonds between components and ceramic substrates. The one-part adhesive material also provides thermally conductive bonds between ceramic substrates and aluminum headers or heat sinks. Eccobond 282 offers a thermal conductivity of 0.003 W/cm °C and a coefficient of thermal expansion of 31×10^{-6}/°C. The product exhibits a tensile lap shear strength of 2300 psi (aluminum to aluminum) and has a dielectric strength or volume resistivity of 500 V/m. Eccobond 282 cures in 30 minutes and withstands continuous service at 175°C.

Emerson & Cuming, 869 Washington St., Canton, Mass. 02021; (617) 828-3300.

CIRCLE 357

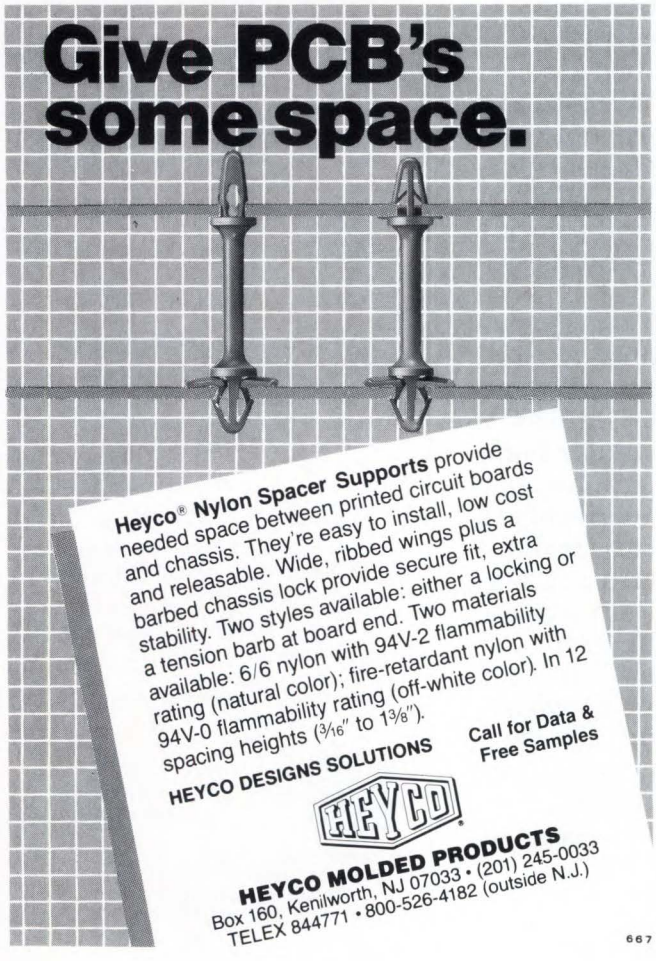
Die-attach adhesive increases yields

Du Pont 4621 is a conductive adhesive that exhibits exceptionally high shear strength to increase yields in automated die-attach applications. It exhibits a hot-die shear strength of 4 kg at 300°C (using a 180-by-180-mil die)—significantly higher than other commercially available adhesives. Room-temperature shear strength is greater than 2800 psi (more than 12 kg) and lap shear is greater than 1500 psi.

For optimum thermal stability, the recommended cure cycle is 60 minutes at 175°C. After aging a cured sample for 100 hours at 105°C, the volume resistivity was 1.3×10^{-4} Ω-cm. The silver-filled epoxy adhesive also has a low ionic content, substantially eliminating corrosion problems that could decrease device reliability.

Du Pont Co., Electronic Materials Division N-2526, Marketing Communications Department, Wilmington, Del. 19898; (302) 773-3218.

CIRCLE 358



CIRCLE 239

PRODUCT NEWS

Op amp joins CMOS standard-cell library

A high-gain (90-dB) op amp, the first in a line of standard-cell op amps from **NCR Corp.'s Microelectronics Division (Fort Collins, Colo.)**, has been added to the company's semicustom design system—a library of more than 50 CMOS analog and digital standard cells. The device can be placed in various locations on a digital chip, permitting maximum use of the real estate. The input reference noise is typically 80 nV rms/$\sqrt{\text{Hz}}$ at 100 Hz or 40 nV rms/$\sqrt{\text{Hz}}$ at 1 kHz. CMOS input transistors lower the op amp's bias currents to less than 100 pA when it is not linked to a bonding pad.

CIRCLE 359

FAST logic IC family grows by 13

Offering design engineers many of the key building blocks needed in digital systems applications, **Signetics Corp. (Sunnyvale, Calif.)** has added 13 devices to its line of proprietary FAST logic ICs. The FAST devices are designed to replace Schottky TTL in systems where higher speed and lower power consumption are required. The parts are 30% faster and consume 75% less power than earlier Schottky TTLs. Devices include inverting and noninverting octal buffers, 8- and dual 4-bit addressable latches, an inverting quad bus transceiver, a comparator, two transmission line drivers, three Schmitt trigger circuits, and a quad two-input multiplexer that has a maximum propagation delay of 9 ns (three times faster than the closest equivalent part).

CIRCLE 360

Enhancements sweep Kaypro line

With only minimal price increases, **Kaypro Corp. (Solana Beach, Calif.)** has upgraded each of its personal computers with more storage capability. The Kaypro 2, now designated the 2X, has doubled its storage space with the addition of 400-kbyte double-sided, double-density disk drives. It sells for $1595, which represents a $300 increase. Priced at $2495, the new Kaypro 4X boasts a total storage capacity of 5 Mbytes using high-density floppy-disk drives, each capable of holding 2.6 Mbytes. At the high end of the line, the 12X complements the Kaypro 10's 10-Mbyte hard disk with a 2.6-Mbyte floppy-disk drive that is capable of backing up the entire hard disk on only a few floppies. At $3295, the company expects the 12X to give IBM's PC XT a run for its money.

CIRCLE 361

4IA DIGITAL DELAY LINE
MACHINE INSERTABLE
Delay Lines Available From ESAN USA, INC.
• 41A-5 tap, Digital Delay Line, DIP, Automatic Insertion
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• 10A, 11A, 12A - Passive Delay Line, DIP, Automatic Insertion
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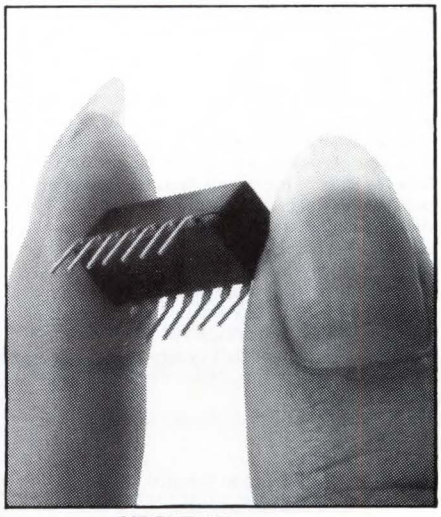
CIRCLE 188

ElectronicDesign

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- To provide a central source of timely electronics information.
- To promote communication among members of the electronics community.

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PRODUCT NEWS

SNA gateway software lets PC emulate 3274

The latest addition to the PLAN series of personal computer networking systems, from **Nestar Systems Inc. (Palo Alto, Calif.),** release 1.0 of the IBM SNA Gateway allows a dedicated IBM PC on the network to emulate a remote IBM 3274 supporting up to 16 user-stations per gateway. User-stations are PCs running DOS 2.0 or 2.1 and emulating 3278s and 3279s. The gateway station interfaces with IBM mainframes that support the 3270 SNA protocols and, at the same time, allows other IBM PCs to function as interactive workstations. Features emulated by the gateway software include upper- and lowercase display, 24-row-by-80-column screen format with 25th status line, protected and unprotected fields, program function and access keys, audible alarm, host-initiated printing, and color display. **CIRCLE 362**

Modem links micros with mainframe

Gamma Technology Inc. (Palo Alto, Calif.) has announced two enhancements to its FAXT-96 line of 9600-bit/s integral modems for the IBM PC XT: automatic speed selection and operation in a stand-alone chassis at the mainframe. The latter allows remote PC XT users with FAXT-96 modems to communicate with the mainframe over ordinary dial-up lines. A stand-alone enclosure, which holds up to three modem boards, is available for $1500. The former enhancement, a proprietary feature that is unavailable on other modems, automatically tests the circuit and selects the best transmission speed for optimum throughput. By using two FAXT-96 modems in an end-to-end link, users need not attempt transmission speeds that result in lower overall throughput. **CIRCLE 363**

Oasis operating system is improved

Oasis Technologies Inc. (Lafayette, Calif.) has released Version VI of the Oasis operating system for 8-bit microcomputers. Version VI offers additional tools for applications development, as well as increased speed and overall system performance. Enhancements include a command-level, full-function algebraic calculator, new extensions to the EXEC job control language, optimized Oasis Basic for applications development, and disk I/O and overlay management, which are controlled by FIFO queues to improve and balance multi-user performance. In addition, overlays can now be stored—at the user's option—in banked memory to improve performance. True record locking, rather than sector locking, ensures maximum data integrity. **CIRCLE 364**

PRODUCT NEWS

HP cuts cost of floppy, Winchester drives

For the second time in one year, **Hewlett-Packard Co. (Palo Alto, Calif.)** has reduced the price of its 270-kbyte 3½-in. flexible-disk drive. The HP 9121S single drive now sells for $710, formerly $900. The HP 9121D dual drive can be had for $965, dropped from $1270. Also reduced are the HP 9133XV 5-Mbyte Winchester drive and the HP 9134XV stand-alone 15-Mbyte Winchester. Respectively, the drives sell for $3345 and $3040, reduced from $3650 and $3345. **CIRCLE 365**

Module analyzes waveforms to 100 kHz

Capable of analyzing waveforms up to 100 kHz in either storage or real-time modes, a waveform storage module offers users a sample rate that is 10 times faster, and an internal memory that is twice as long, than previous modules. The Model 13-4616-20, from **Gould Inc.'s Recording Systems Division (Cleveland, Ohio),** operates at a fixed data output rate of 200 samples/s and captures transients as fast as 3 μs. The unit, which sells for $2190, has a full-scale sensitivity range of 50 mV to 500 V throughout its dc to 100-kHz frequency response range. **CIRCLE 366**

TI Professional gets upgraded Winchester

For applications that require a large data base, **Texas Instruments Inc. (Dallas, Texas)** is offering an 18.2-Mbyte Winchester disk option for its Professional computer. The disk option, which is especially useful in resource-sharing environments such as local area networks, has nearly twice the data and program storage of the Professional's current 10-Mbyte Winchester. In addition, the drive's average access time of 40 ms makes it twice as fast. Compatible with MS-DOS 1.25 and 2.1, the $2295 disk option includes diagnostic software, a controller board, and cables. **CIRCLE 367**

Tiny chip capacitors span 0.5 pF to 0.015 μF

One of the smallest multilayer ceramic chip capacitors is being produced by **Johanson Dielectrics Inc. (Burbank, Calif.).** Standing 0.030 in. high, the space-saving chip has dimensions of 0.040 in. long and 0.030 in. wide. Designated the R09 size, it is available in three families covering the capacitance ranges of 0.5 to 100 pF (NPO/COG), 100 to 2200 pF (BX/X7R), and 1000 pF to 0.015 μF (Z5U/Y5V). Prices range from $0.773 to $2.40 in 1000-unit orders, with delivery from stock to 10 weeks. **CIRCLE 368**

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APPLICATION NOTES

Controlling solenoid motion

A two-page data sheet, entitled *Taming the Solenoid,* discusses the control of solenoid motion using air dashpots. It presents a brief but informative overview of solenoid problems and explains how dashpots are an effective method for damping shock and vibration, for controlling velocity, and for providing adjustable mechanical time delays. The bulletin includes characteristic peformance curves, illustrations, and applications information. It also lists available dashpot types and sizes.

Airpot Corp., 29 Lois St., Norwalk, Conn. 06851.

CIRCLE 369

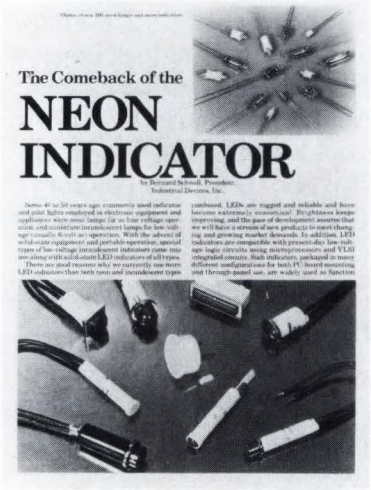
Personal computers for data acquisition

The *Data Acquisition Handbook* describes the use of personal computers for data acquisition and control applications. The 58-page reference guide introduces pc users to the basics of signal interfacing with computers and illustrates the simple techniques for setting up a computer-based data acquisition and control system in virtually any setting. It also includes a chapter on the software considerations of interfacing.

Taurus Computer Products Inc., 1755 Woodward Drive, Ottawa, Ont. K2C 0P9, Canada.

CIRCLE 370

The advantages of neon indicators


The Comeback of the
NEON
INDICATOR

The Comeback of the Neon Indicator is an illustrated technical article that describes the operation of neon indicators. It covers light output and color, as well as factors that determine lamp life. Two graphs are included that enable designers to determine the optimum values of series resistors to be used with standard and high-brightness lamps. In addition, a chart presents the specifications and operating characteristics of a full line of neon indicators.

Industrial Devices Inc., 7 Hudson Ave., Edgewater, N.J. 07020.

CIRCLE 371

Surface mounting chip capacitors

Chip Capacitors Relating to Surface Mounting Technology discusses the latest research in processing techniques for mounting leadless chip capacitors directly to integrated circuit boards. Detailing the technology and methodologies for applying surface-mounted devices, the brochure also covers methods for avoiding such problems as thermo shock and leaching of the capacitor terminations. In addition, chip standardization, packaging, and automated assembly are reviewed. Five figures and four tables accompany the text.

AVX Corp., PO Box 867, Myrtle Beach, S.C. 29577.

CIRCLE 372

How HP 3065 speeds board repair time

Cluster-based Paperless Repair/Reporting explains how this feature builds on the architecture of the HP 3065 in-circuit board test system. The data sheet shows how paperless repair/reporting (PRR) can speed the repair process and provide insight into problem causes. It also explains how test data is collected and electronically transferred to repair stations within the test cluster.

A second data sheet, *Cluster-based Q-STATS,* explains how data from the test and repair loops is integrated to provide a high-level user interface and automatic report generation. Like PRR, Q-STATS is a standard feature of the HP 3065 test system.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303.

CIRCLE 373

NEW LITERATURE

Dc-dc converter handbook

Containing comprehensive data on a line of dc-dc converters, this 32-page handbook covers more than 35 new products. Power supply characteristics are presented in selection tables, followed by complete engineering data on all models. Also included is a glossary of dc-dc converter terminology and tutorial information on converter operation.

Power General, 152 Will Drive, PO Box 189, Canton, Mass. 02021. **CIRCLE 374**

Logic analyzer selection and use

Illustrated with line drawings and photographs, a 40-page guide for the selection and use of logic analyzers helps designers evaluate their equipment needs in terms of state analysis, timing measurements, and software debugging and performance analysis. A flow diagram further aids in the selection process. The guide also gives summaries of a line of instruments, ranging from the 32-channel LAM-3250 to the Colt and Atlas digital workstations. Descriptions of plug-ins and accessories for the logic analyzers complete the booklet.

Dolch Logic Instruments Inc., 3052 Orchard Drive, San Jose, Calif. 95134.

CIRCLE 375

Semiconductor selection guide

Completely updated, expanded, and indexed, a 13-page selection guide provides key specifications for memories, microcontrollers, microprocessors and peripheral devices, linear ICs, and power products.

Mitsubishi Electronics America Inc., 777 N. Pastoria Ave., Sunnyvale, Calif. 94086.

CIRCLE 376

VMEbus and Eurobus products

Modular boards for the VMEbus and the Eurobus are presented in a 48-page catalog, which includes color photographs and specifications for CPU and microcomputer boards, memory modules, a-d and d-a converter boards, and I/O and control modules. Additional products include universal development systems, peripherals, racks and power supplies. An informative section describes and illustrates CP/M, VERSAdos, Unix, and other operating systems.

PEP Elektronik Systeme GmbH, Am Klosterwald 4, D-8950 Kaufbeuren, Germany. **CIRCLE 377**

Micropositioning, measurement, and control

Micropositioning Systems describes programmable microscope systems—as well as individual motors, controllers, and encoders—for applications requiring micron and submicron positioning, measurement, and control. The brochure includes systems for optical fiber alignment and disk head and media inspection.

Burleigh Instruments Inc., Burleigh Park, Fishers, N.Y. 14453. **CIRCLE 378**

Intelligent 'hand' for industrial robots

Foreman, an intelligent robot hand for industrial robots, is the focus of a six-page data sheet. The document describes Foreman's sensors, quick connect/disconnect fingertip tooling, and intelligent controller properties. Interface details and photos of various assembly operations are included.

Monforte Robotics Inc., 2333 Whitehorse-Mercerville Road, Trenton, N.J. 08619.

CIRCLE 379

NEW LITERATURE

Servo accelerometers and inclinometers

An 11-page bulletin serves as a valuable aid in the selection of force-balance servo accelerometers and inclinometers. The guide depicts both stock units and special units, along with their respective specifications and applications. Tutorial information defines scale factor, bias, input axis, cross axis sensitivity, composite error, repeatability, nonlinearity, hysteresis error, resolution, threshold, and rectification error.

Columbia Research Laboratories Inc., MacDade Blvd. and Bullens Lane, Woodlyn, Pa. 19094.

CIRCLE 380

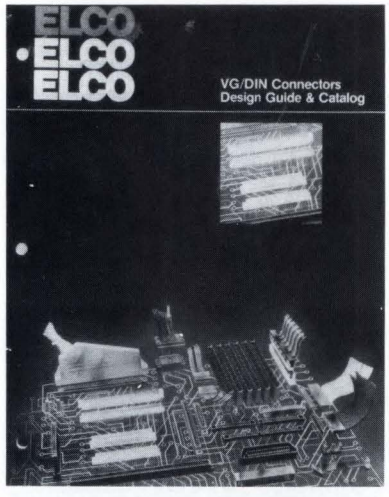
Scotchflex brand interconnection products

Containing how-to-use drawings and photos of Scotchflex brand interconnection products, an updated source book specifies items such as cable connector systems; a backplane socket/header system; socket, plug, pc board, DIP, and card-edge connectors; the Delta connector and Delta ribbon connector systems; breadboards; and cables. A toll-free phone line is given for ordering the latest spec sheets on Scotchflex products—delivered to the caller within 48 hours.

3M, Electronic Products Division, EP84-13, PO Box 33600, St. Paul, Minn. 55133.

CIRCLE 381

VG/DIN high-density connectors



A 32-page design guide and catalog describes a broad line of two-, three-, and four-row VG/DIN connectors for single, double, and multilayer boards. The low-insertion/withdrawal force connectors have up to 201 contact positions in both standard and inverted styles. The design guide section details connectors in a variety of I/O and board-to-board applications.

Elco Corp., 74 Brookhollow Drive, Santa Ana, Calif. 92705.

CIRCLE 382

Solid-state relay backgrounder

Illustrated with circuit drawings, a pocket-sized booklet discusses the differences in construction, operation, and performance of reed- and optically-coupled solid-state relays. It provides insight into random and zero-voltage switching and points out the important specifications concerning both the power and control aspects of SSRs. Applications information is also supplied.

Sigma Instruments Inc., Switching Division, 170 Pearl St., Braintree, Mass. 02184.

CIRCLE 383

Data communications equipment and cable

The Codex 1984 spring/summer direct-order catalog enables data communications users to order products without going through their Codex sales representatives. The catalog covers network processors; statistical multiplexers; limited-distance, high-speed, and Bell-compatible modems; and cable. All stocked products are shipped within 72 hours following receipt of order.

Codex Corp., 20 Cabot Blvd., Mansfield, Mass. 02048.

CIRCLE 384

CMOS product directory

Covering a full line of advanced CMOS integrated circuits, a 24-page directory provides descriptions and technical data for microprocessors, single-chip microcomputers, supporting development systems, peripheral control circuits, memory products, communications ICs, gate arrays, standard cells, and logic.

GTE Microcircuits, Marketing Services, 2000 W. 14th St., Tempe, Ariz. 85281.

CIRCLE 385

NEW LITERATURE

Commercializing artificial intelligence

The commercialization of artificial intelligence technology is the subject of a 16-page pamphlet, which documents the nature of artificial intelligence and the developing applications for AI technology. The brochure emphasizes what is needed for AI to succeed in the commercial world—applying it not to narrow specialties, but to situations and problems encountered in a wide range of industries.

Lisp Machines Inc., 6033 W. Century Blvd., Suite 900, Los Angeles, Calif. 90045.

CIRCLE 386

Powdered-iron toroidal cores

High-permeability powdered-iron toroidal cores, with permeability ratings of 60, 67, and 75, are presented in an eight-page brochure that provides performance curves, outline drawings, inductance values, and other related technical data.

Pyroferric International Inc., 200 Madison St., Toledo, Ill. 62468. **CIRCLE 387**

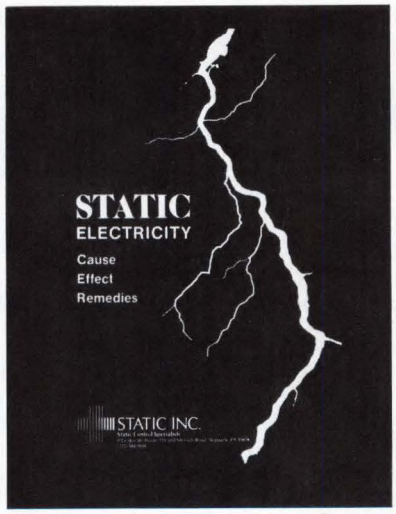
Industrial robots

Robots that can be applied to a wide variety of industrial applications are the subject of this brochure, which includes technical specifications for 20 robot models. The literature describes each robot, outlining applications, work-envelope definition, axis-drive method, position repeatability, and payload. Drawings illustrate configuration and axis travel for each model. Applications include material handling, assembly, machine loading, arc and spot welding, sealing, spray painting, and more.

GMF Robotics Corp., 5600 New King St., Troy, Mich. 48098.

CIRCLE 388

Solutions for static electricity



An eight-page brochure discusses the causes and effects of static electricity, along with remedies for the problems it creates. The bulletin covers such topics as conductivity, induction, grounding, and ionization. It also discusses the selection of equipment to diffuse static electricity and presents a number of static-neutralizing products.

Static Inc., PO Box 80, Skippack, Pa. 19474.

CIRCLE 389

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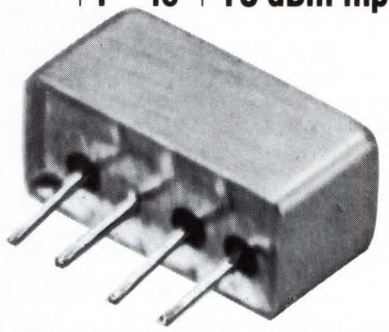

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- low conversion loss, 13 dB
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*Units are not QPL listed

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OUTPUT	2-1000	
CONVERSION LOSS, dB	TYP.	MAX.
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100-300 MHz	13.5	15.5
300-500 MHz	14.0	16.5
Spurious Harmonic Output, dB	TYP.	MIN.
2-200 MHz F1	−40	−30
F3	−50	−40
200-600 MHz F1	−25	−20
F3	−40	−30
600-1000 MHz F1	−20	−15
F3	−30	−25

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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CIRCLE 242

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Nicolet Biomedical Instruments, leader in the manufacture and sale of clinical electrophysiological instrumentation, has an immediate opportunity for an experienced Analog Design Engineer.

The candidate selected for this position will design analog circuits for sophisticated medical instruments as part of the team dedicated to excellence. The experience necessary for this position should include noise interaction, stability analysis, design of high gain physiological amplifiers, filtering circuits, patient isolation systems, and A/D and D/A converters. A strong background in interfacing analog and digital circuitry and the design of hybrid circuits is strongly preferred. A BS or MS in electrical engineering is required with additional training in physiology helpful.

Nicolet is a rapidly growing, high technology company in the rolling woodlands of Madison, Wisconsin. With a metropolitan population of 335,000, the Madison community places a high priority on education, quality of life and is recognized as one of the top three metropolitan areas of its size in which to live.

We offer a complete benefit package and a progressive relocation program. If you are interested in pursuing this opportunity send your credentials to : Robert W. Lovely, Nicolet Biomedical Instruments, 5225-4 Verona Road, Madison, WI 53711-0287, 608/273-5036. Nicolet is an equal opportunity employer m/f/h.

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CALIFORNIA INSTRUMENTS is the leader in IEEE programmable AC power conversion equipment and our expanding business has created a few key positions within our Engineering Department.

If your analog design background includes some exposure to linear and switching power conversion and digital design, have we got a challenge for you! The successful candidate will be asked to assume project responsibility from design inception through production. You will be expected to push the state-of-the-art in AC power conversion in both commercial and military environments.

In addition to a professional working environment, CALIFORNIA INSTRUMENTS offers a very competitive salary and fringe benefit package. We are an equal opportunity/affirmative action employer. **Please send your resume with salary history in confidence to: L. LOONEY: or call Toll-Free 1-800-356-2244 or inside Calif. 1-800-821-1634.**

California INSTRUMENTS

5150 Convoy Street
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At our high technology facility in Rolling Meadows, Illinois, just northwest of Chicago, Northrop Engineers collaborate on special projects involving the design and development of sophisticated ECM systems. Experienced professionals can become a vital part of an outstanding team of R&D engineers working in a technologically progressive advanced systems environment. Our suburban location offers the advantage of a lifestyle rich in educational, cultural and recreational values.

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Positions require BSEE or equivalent, and DESIGN/DEVELOPMENT experience in one of the following:
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BSEE, BSCS or equivalent and related ATE or MTE software/hardware experience involving design of automated/semi-automated test equipment systems.
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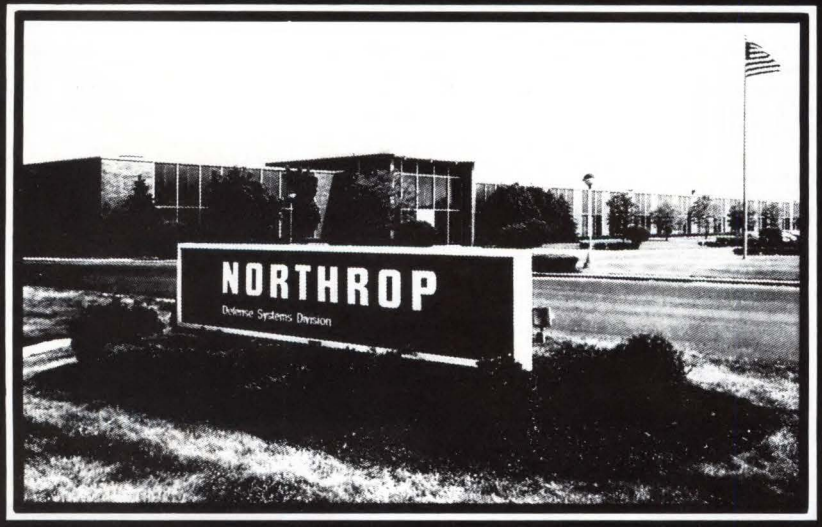

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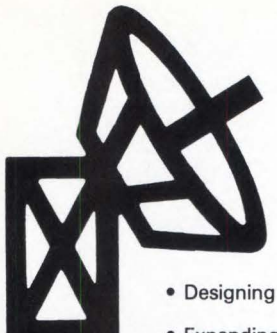

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Responsible for the design, development and systems integration of major portions of digital signal processing systems. Experience and interest in high-speed digital logic, signal processing, microprocessor based systems and high-speed parallel pipeline processors would be desirable for this challenging position. BSEE/MSEE with 5 or more years of relevant experience.

DEVELOPMENT ENGINEERS
Responsible for the design, development and test of general and special purpose digital signal processing equipment. Both hardware and microprocesor based software design tasks are anticipated. Familiarity with microprocessor applications and digital signal processing techniques preferred. BSEE plus 3 years of applicable experience required.

ELECTRONIC DESIGN ENGINEERS
Requires experience in advanced digital hardware design, microprocessor applications, firmware design and microprogrammable systems. BSEE plus 3-5 years experience in design and implementation of digital hardware. MSEE desirable.

DESIGN SPECIALISTS
Design major subsystems of digital signal processing systems as applied to acoustic signal analysis, including design, development, test and integration of subsystem. Experience in signal processing, bit slice processors, 6800 microprocessors and sonar signal processing desirable. BSEE or MSEE plus 5 years experience in CPU based digital systems design required.

SENIOR SYSTEMS ENGINEER
Systems engineering of major digital signal processing systems as applied to acoustic signal analysis and communication. Includes proposals, system requirements specifications, system designs and hardware/software performance verification. BSEE or equivalent plus 5-7 years experience in digital sonar or undersea communications. MSEE desirable.

SOFTWARE

SOFTWARE PROJECT ENGINEERS
Responsible for the overall technical direction of software projects to include computer systems, software design for microprocessed based systems, development of software specifications, detailed software design and integration of software with hardware systems. Will also be involved with customer interface, proposal writing and supervision of technical personnel. Should be proficient in systems level programming and real-time control of hardware. Familiarity with "C", PASCAL, UNIX and DEC operating systems and 68000 microprocessor desirable. BSCS/MSCS with 5 or more years of revelant experience.

SENIOR SOFTWARE DESIGN ENGINEERS
Assist in design of software modules involving generation of software documentation, software code and debug. Must be familiar with "C", Pascal, Unix operating Systems, DEC operating systems or 68000 microprocessor. BSEE/CS plus 3-5 years design experience required. Experience with microprocessors and hardware drives preferred.

DESIGN SPECIALISTS
Design and documentation of significant software tasks associated with ASW and signal processing systems. Experience in real-time software development and systems software design utilizing 68000 and 280 microprocessors required. Experience with "C", Pascal, UNIX and DEC Operating Systems desirable. BSEE/CS plus 5 or more years experience in software design.

An additional opportunity exists for a:

SR. RELIABILITY ENGINEER
Responsible for the preparation and implementation of reliability/maintainability program plans, procedures and demonstration testing. Will analyze part failures and recommend corrective action to improve product reliability, maintainability or safety. Familiarity with microprocessor based digital signal processing circuts preferred. Ability to use and program IBM PC for computer aided circuit analysis desired. BSEE or the equivalent and recent reliability/maintainability experience in a military environment required. 5 or more years experience required.

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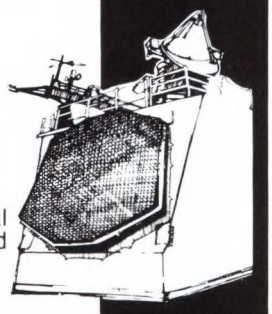

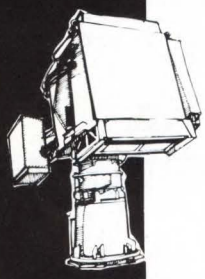

CHALLENGING OPPORTUNITIES ALSO EXIST FOR:

Analog Design Engineers

Experienced engineers needed to design linear and non-linear circuits for analog Signal Processing applications. Should be familiar with circuit modeling and computer aided analysis techniques.

Analog Engineers

BS Degree in computer science or electrical engineering with experience in programming automatic test equipment using HP-1000 and HP-9836 computers. Responsible for the planning and implementation of the Automatic Testing of a series of RF and microwave chassis including reviewing and supporting the work of individual test engineers in the detailed generation of Test Programs.

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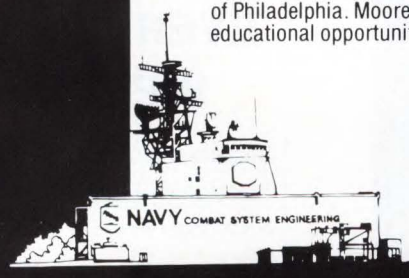

CONTACT RCA MSR TODAY!

Forward your resume to:

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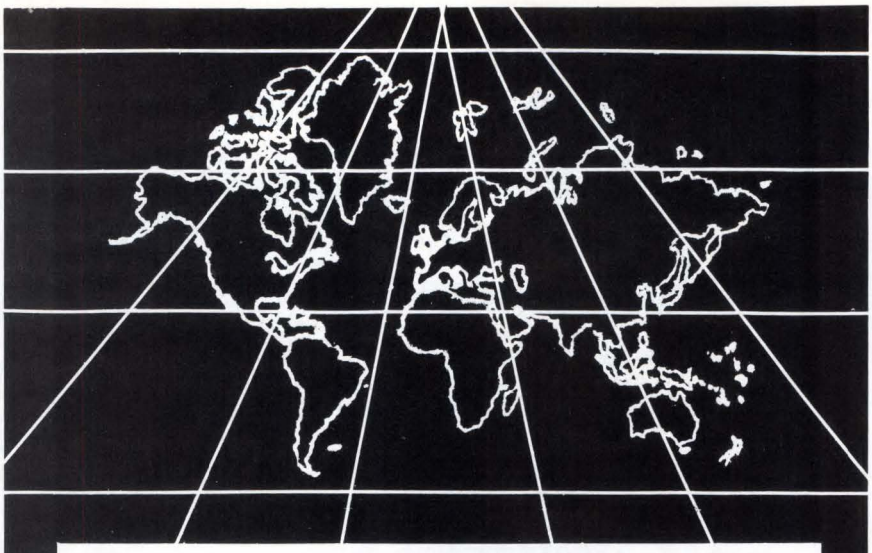

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Use your semiconductor packaging or fiber optic expertise to design and develop high volume optoelectronic packaging for fiber optic applications, and demonstrate a leadership role in project planning and management. Your background includes 3-5 years' experience in the design of semiconductor packaging and assembly or related areas, solid communication and organizational skills and a BSME. MS in ME, EE, physics or optics is highly desirable. Respond to Dept. DT.

Analog Design Project Manager

Use your fiber optic design and managerial skills to develop transmitters and receivers for high speed data communications, and lead a team of engineers from development concept to product. Your background includes 5 years of design or related experience to include analog circuits, demonstrated project leadership skills and a BSEE. MSEE is highly desirable. Respond to Dept. IO.

Analog Development Engineer

Use your design knowledge to develop high speed fiber optic data links and discrete analog circuits (LED drivers, low noise amplifiers, etc.), and to assist in defining new products. Your background includes 3-5 years' experience in analog design including discrete circuit design and a BSEE. MSEE is highly desirable. Respond to Dept. IO.

Optical Measurement Engineer

Use your high frequency and optics experience to develop and augment computer controlled, high frequency characterization systems for fiber optic components. Requires an MS in EE/applied physics with training/experience with high frequency analog electrical or optical measurements. Optics experience, especially fiber optics, is desired. Respond to Dept. JT.

Project Leader/Analog Circuit Designer

You will be responsible for the development of new high performance optocoupler products. Primary activities include analog circuit design, device modelling, circuit simulations, product and device characterization. You will participate in the development of new packages and optical components and work with other engineers doing market investigations, reliability evaluations and process evaluations. Requirements include a BSEE (MSEE preferred) with a minimum of two years' experience in analog circuit, interface circuit or switching power supply design and a good understanding of solid state devices. Experience with high voltage or high power semiconductors is valuable. Leadership and supervisory responsibility will be commensurate with experience. Respond to Dept. JP.

Optocoupler Development Engineer

You will utilize your linear circuit design or semiconductor device physics background to design and/or improve current optocouplers. Initial activities will include evaluation and characterization of prototype products and participation in the development of new assembly/packaging line. Requires a BSEE or equivalent, 2 years' experience in the development, manufacturing or testing of semiconductor components. Respond to Dept. JP.

Optocoupler Development Engineer

You will be the primary electrical contributor on package development projects for new and current optocouplers. Responsibilities include development and evaluation of prototype products, product characterization, test equipment specification and acquisition, and evaluation of optical and semiconductor components. Requires a BSEE, BSME or equivalent with a minimum of 2 years' experience in semiconductor or hybrid packaging design and development. Respond to Dept. JP.

Analog IC Design Engineer

Use your IC design knowledge to develop state-of-the-art analog ICs for fiber optic transmitters and receivers. Activities include design, modelling, simulation, and characterization of ICs, as well as participating on the product development team from product definition to manufacturing release. Your background includes a BSEE (MSEE preferred), at least 2 years' experience in analog IC design, and good communication skills. Respond to Dept. KS.

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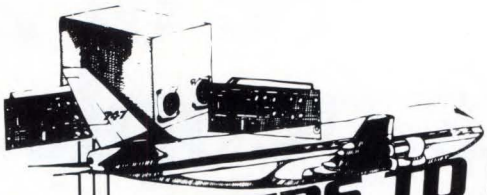

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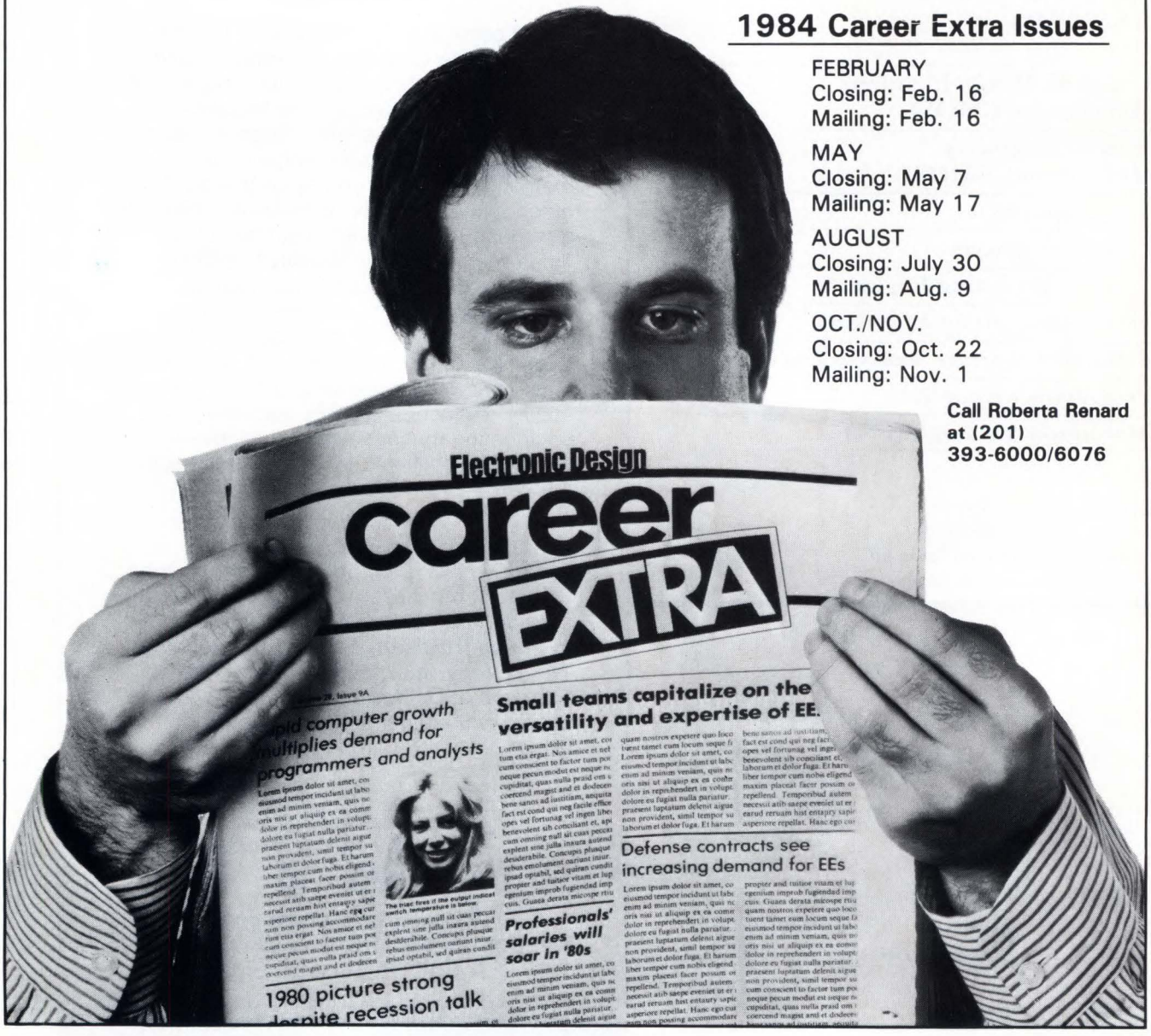

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Chicago, IL 60611
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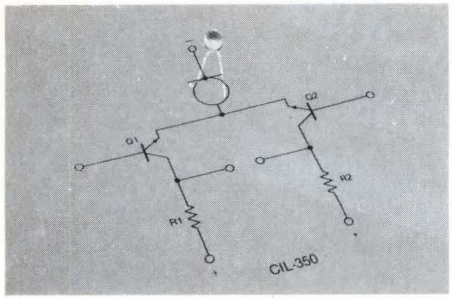


New 50mA CURRENT REGULATING DIODE Crystalonics offers new line of very high current regulating diodes, including a 50 mA device. CIL350 Series ranges from 11mA to 50mA, has high source impedance and peak operating voltages of 45V Max with selections available to 65V Max. Ideal stable reference currents for TC zeners, high stability biasing for oscillators, & protection for IC's. Free short form catalog & data sheet. TELEDYNE CRYSTALONICS, 147 Sherman ST., Cambridge, MA 02140 (617) 491-1670 TWX: 710-320-1196

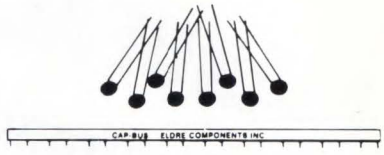
CURRENT REGULATING DIODE **261**

Alphacom/Olivetti 20, 40, 80 Column Printers, Mechanisms Controllers, Thermal Paper

A complete line of cost effective Printers Mechanisms, Controllers. The PU1100 impact print mechanism includes a snap in ribbon. The PU1800 and PU1840 series are 20 and 40 column thermal print mechanisms. The EM1100 EM1800, EM1840 series are controller boards with mechanism mounted on them. Serial and Parallel interfaces are standard. The Alphacom 20, 40, 42, 80 are a series of low cost stand alone printers. Available from Micro Electronic Business Inc. 312-539-2994 3748 W Montrose Ave., Chicago, IL 60618

PRINTERS, MECHANISMS, ETC. **262**

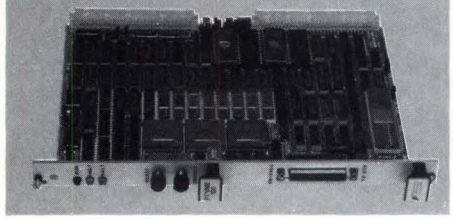
ELIMINATE DECOUPLING CAPACITORS



CAP-BUS® CAPACITOR/BUS BAR Eliminate the decoupling capacitors and the power and ground traces from your PCB for more reliability. CAP-BUS® has distributed capacitance of .05 micro-farads per lin. in., at 50 VDC with low inductance and low impedance. The capacitor and the bus bar have been joined together for CAP-BUS®; a more efficient capacitive decoupled power distribution system, increasing IC density on a two sided board. **ELDRE COMPONENTS, INC.**, 1500 Jefferson Rd., Rochester, NY 14623 (716) 244-2570

BUS BAR CAPACITOR **263**

MAIN FRAME PERFORMANCE NOW AVAILABLE ON VMEbus

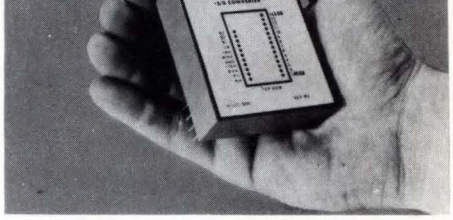


A general purpose VMEbus processing element yielding high-end processing power in compact cost-effective package. Combines 68010 microprocessor, high-speed memory management facility, fast access cache memory and full 32-bit data interface for high-end processor performance. Executes memory resident programs with 75% zero wait state hit rate. Performance Technologies, Inc., 300 Main Street, East Rochester, New York 14445. (716) 586-6727.

PROCESSOR MODULE **264**

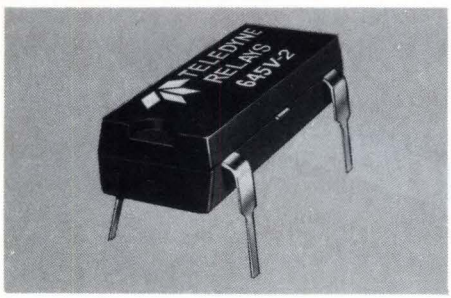
Immediate Delivery - Low Profile Keyboard Housings. Only $18.25 for one. Quantity discounts. 18" wide pictured. Other models. Molded of UL vo 94-95 materials; includes metal base plate, inserts, screws, bumpons. Fabrication, EMI shielding and painting to your specifications. Hettinga, Inc., 2123 N.W. 111th. St., Des Moines, Iowa 50322 USA. (515) 270-6900. Telex 478315.

KEYBOARD HOUSINGS **265**



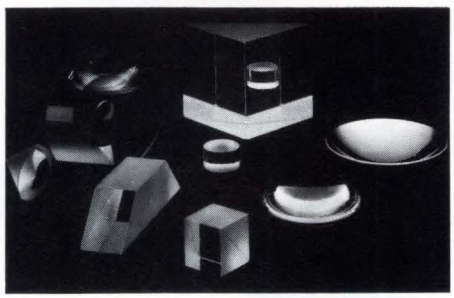
SYNCHRO TO DIGITAL CONVERTER—.42" HIGH —50 to 400 Hz operation—tracks input rates up to 36000°/sec—low power consumption—Cmos or TTL or LP Shottky Logic—Velocity output available-0° C to 70° C or -55° C to +105° C operation—10, 12 or 14 Bit resolution—2.6" × 3.1" × .42" High-units from $199.00 each (PT No. SDC610 or 410). For other CCC products send for free catalog and Application Notes. COMPUTER CONVERSIONS CORPORATION. 6 Dunton Court, East Northport, New York 11731 (516) 261-3300.

S/D CONVERTER **266**



LOW EMI AC DIP SOLID STATE RELAY Teledyne's 645V meets FCC and VDE stds. Features 3.8 to 32V input and TTL logic compatibility, up to 1 amp switching at 250VRMS, back to back SCR output, low leakage current of 1mA RMS, 3750VRMS VDE level optical isolation, low insertion factor of + 1.5V, high noise immunity, and virtually no switching transients. $4.90 ea for 5000 pcs. Teledyne Solid State Products, 12525 Daphne Ave., Hawthorne, Ca. 90250 (213) 777-0077.

RELAYS **267**



ROLYN OPTICS CO. supplies all types of "Off the Shelf" optical components. Lenses, prisms, mirrors, irises, microscope objectives and eyepieces and many others. All from stock. We also supply custom products and coatings in prototype or production quantities. 75 page catalog describes products and prices. ROLYN OPTICS CO., 738 Arrowgrand Circle, Covina, CA 91725 (818) 915-5707 & (818) 915-5717. TELEX: 67 0380.

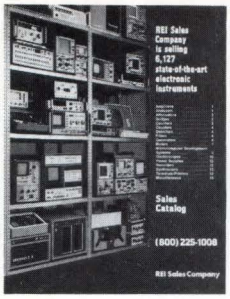
OPTICS **268**

FEDERAL COMMUNICATIONS COMMISSION

FCC PART 15, VDE 0871, UL COMPLIANCE WORK FOR CUSTOMERS USA, EUROPE AND FAR EAST

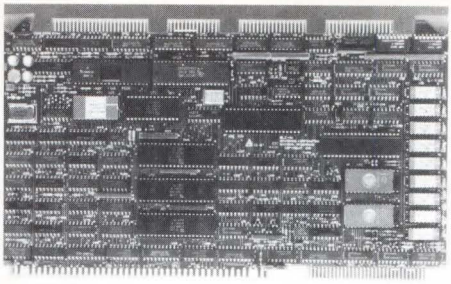
Radiation Technology is an EMI/RFI test laboratory. Our test site, equipment and procedures are a very close copy of the F.C.C. in Maryland. We will test/verify your product for F.C.C. compliance and/or do the complete F.C.C. submission. If your product does not comply with Federal Law, we can **very** cost effectively bring it into compliance in a short time. RADIATION TECHNOLOGY 18675 ADAMS CT. UNIT G. MORGAN HILL, CA 95037 (408) 778-0577.

COMPLIANCE WORK **269**



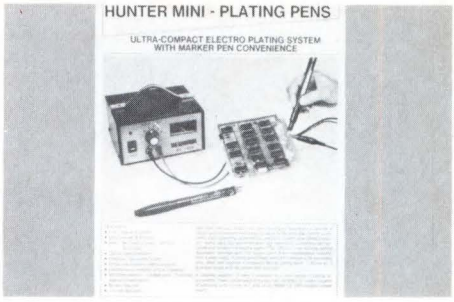
LIKE NEW PRODUCTS FOR SALE NOW. Free new catalog describes over 6,000 state-of-the-art electronic instruments for sale. It all comes with Money Back Guarantee. Before you buy new equipment, check these items! Phone toll-free (800) 225-1008. . .in Massachusetts (617) 938-0900. Or write today to Genstar REI Sales Company, 6307 DeSota Ave., Suite J, Woodland Hills, CA 91367.

FREE SALES CATALOG **270**



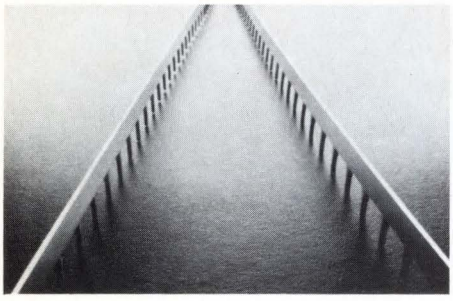
A MULTI-USER SBC the MLZ-92A has Z-80A CPU, floppy controller. Winchester and streamer I/F, DMA, AM 9511 math chip, up to 64K RAM with parity, 2 ROM sockets, 4 serial ports (2 RS 232 ports plus 2 RS 232/422), 4 counter/timers, 20 bit Intel Multibus, Bi-directional I/F, memory mapping RAM, I/O map, user defined LEDS and dip switch positions, and CP/M and MP/M. Heurikon Corporation, 3201 Latham Drive, Madison, Wisconsin 53713. (800) 356-9602. In Wisconsin (608) 271-8700.

MULTI-USER SBC **271**



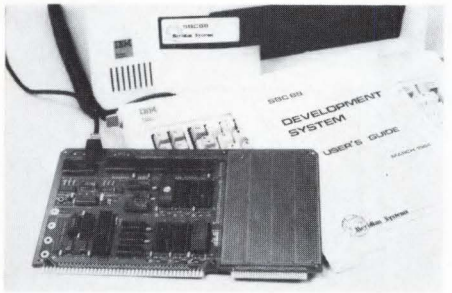
Mini-Plating Pens 4-page brochure describes the Hunter ultra compact electro-plating system, which was developed specifically to provide a simple convenient & safe electro-plating capability for electronic repair & touch-up work. Utilizing special, disposable marker-type pens, this system permits an instantaneous selection from a wide variety of plating possibilities without the bother & trouble of handling plating solutions. HUNTER PRODUCTS, INC., Hunter Associates Div., 792 Partridge Dr., Bridgewater, N.J. 08807. (201) 526-8440

MINI-PLATING PENS **272**



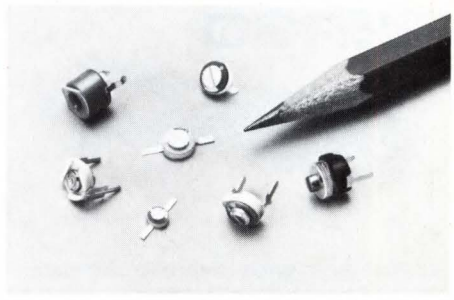
PLANE FACT. Nothing prevents warpage of printed wiring boards during soldering more simply and effectively than Rogers' board stiffeners. Contact Rogers for a free board stiffener sample. You'll see how they can also serve as ground or voltage suppliers of up to 25 amps. Call today for the full story. And get it straight. Rogers Corporation, Bus Products Division, 5750 E. McKellips Rd., Mesa, AZ 85205, telephone 602 830-3370.

BOARD STIFFENERS **273**



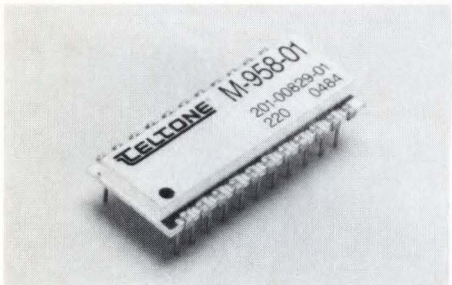
IS the IBM PC a DEVELOPMENT SYSTEM? YES!!! For only $600 you get: 8088 Single Board Computer (SBC88) + Development Software + Cable (SBC88 to PC) + Documentation. Applications include: Robortic Design, Process Control and Automation, Education, Dedicated Testers, Lab Application, Prototype Designs, etc. Also available: PROM PROGRAMER, PAL PROGRAMER. PC Software included. **MERIDIAN SYSTEMS** 321 Aviador St., #111, P.O. Box 3034, Camarillo, CA 93011; (805)-484-8696.

SBC88 DEVELOPMENT SYSTEM **274**



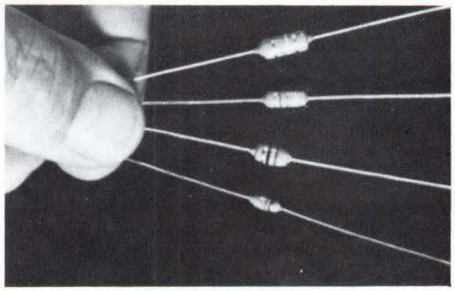
WORLD'S LARGEST SELECTION OF 5MM (OR SMALLER) TRIMMER CAPACITORS. The most wanted features found in various models include high stability, low cost, very small size, and very high Q at high frequency. SPRAGUE-GOODMAN ELECTRONICS, INC. (An affiliate of the Sprague Electric Company) 134 Fulton Ave., Garden City Park, N.Y. 11040. 516-746-1385 • TLX 14-4533.

CAPACITORS **275**



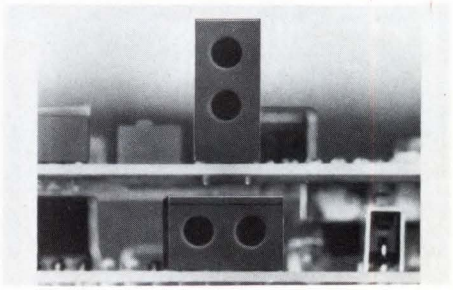
HYBRID DTMF RECEIVER SAVES SPACE. Replace separate CODEC components and tone-receiver chips with Teltone's M-958-01 CMOS circuit. Our dial-tone-immune receiver utilizes 1.544 MHz μ-Law PCM input (CCITT standards are also available). The M-958-01 offers high noise immunity and features wide dynamic range. The M-958-01 joins Teltone's complete family of DTMF generators, detectors, receivers and relays. 1-800-227-3800, ext. 1130. TELTONE CORPORATION, P.O. Box 657, Kirkland, WA 98033.

HYBRID DTMF RECEIVER **276**



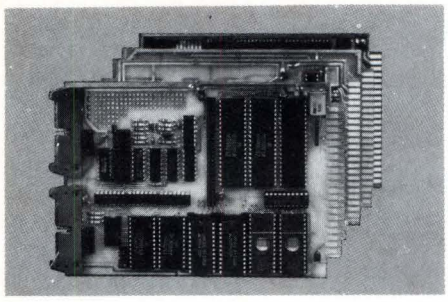
CONFORMAL COATED INDUCTORS ... Manufactured to the same high quality standards as MIL-SPEC molded chokes ... **at considerable savings** ... epoxy resin coated inductors withstand severe environmental conditions ... standard values from .1 uH to 1,000 uH ... custom winding on special order ... 40-page industrial inductors catalog on request. J. W. MILLER DIVISION of Bell Industries, 19070 Reyes Ave., P.O. Box 5825, Rancho Dominguez, CA 90224. (213) 537-5200.

INDUCTORS **277**



PCB JACKS FOR DIRECT ACCESS AND TESTING. Choose ADC's new vertically-designed, double-density PCB jack and **save space on the board.** Or use our low profile horizontal dual jack and **save space between boards.** Both also save on separate jack mounting hardware, front plates, connecting wires, mother boards and several soldering or wire-wrap steps. **FREE SAMPLE** and details on full line of jacks and accessories are available. ADC/Magnetic Controls Company, 4900 West 78th Street, Minneapolis, MN 55435; (612) 893-3010.

PCB JACKS **278**



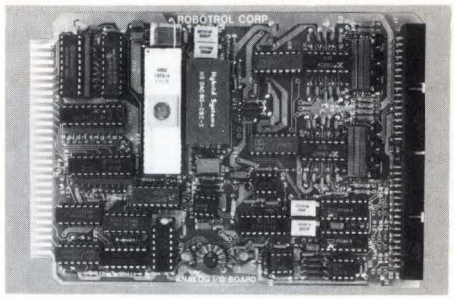
6809 Single Board Computer. 6809 MPU, 2 serial ports, 4 parallel ports, RAM, EPROM, real-time clock, watchdog timer, 44-pin 4.5" x 6.5" PCB. EXPANSION MODULES: RAM, EPROM, CMOS RAM/battery, analog I/O, serial I/O, parallel I/O, counter/timer, IEEE-488, EPROM programmer, floppy disks, cassette, breadboard, keyboard/display. Wintek Corporation, 1801 South Street, Lafayette, IN 47904-2993. (317) 742-8428.

SINGLE BOARD COMPUTER **279**

Logic Simulation System

Interactive Logic Simulation System. A four state unit delay simulator. (1, 0, unknown, hi-z.) Standard ASCII files or keyboard entry. User defined macros, signal sources, patterns. Output is timing diagram (screen or printer) loading report (fanout). Circuit, macros and externals. Signal sources are periodic and aperiodic, user defined. It is easy to use and handles errors gracefully. Full documentation is provided. For microcomputers running CP/M or MS-DOS. Price: $175.00. Tatum Labs, P.O. Box 698, Sandy Hook CT 06482, 203-426-2184.

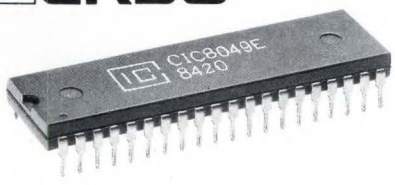
SIMULATION SYSTEM **280**



INTELLIGENT ANALOG I/O. The RSD-7728 is STD bus compatible w. 16 S.E. or 8 diff. inputs and 8 outputs, all with 12 bit resolution. Onboard microprocessor has 13 programmable modes, 6 for outputs, 7 for the inputs. Add'l self-test mode. Inputs have software programmable gain. I/O may be either voltage or current loop. Several jumper connected voltage ranges. Memory or I/O mappable. Vectored interrupt. Dealer inquiries welcome. ROBOTROL CORP., 1250 Oakmead Parkway, Suite 210, Sunnyvale, CA 94086. 408-778-0400.

INTELLIGENT STD ANALOG I/O **281**

ERSO



CIC8049 8-bit single chip microcomputer

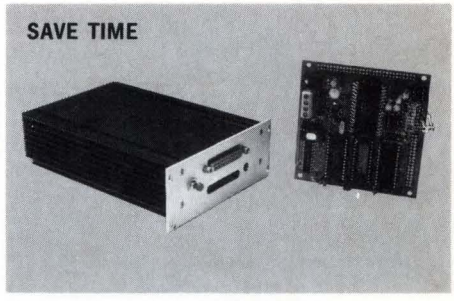
FIRST IN SOUTHEAST ASIA. FEATURES NMOS Technology • Internal Memory-2K × 8 ROM • 128 × 8 RAM • Internal Timer/Event Counter • Single level interrupt • Single 5-volt supply • Over 90 instructions. 70% Single Byte • Timer/counter interrupt available • Reduced Power Consumption • Compatible with Intel's MCS-80/85 peripherals • Easily Expandable Memory and I/O • Up to 1.36 μsec instruction cycle (11 MHz operation), all instructions 1 or 2 cycles. ERSO/ITRI 8th Fl. No. 315, Sung Chiang Rd., Taipei, Taiwan, ROC Telex 12974 ERSO ITRI Tel (02) 542-8212.

SINGLE CHIP MICROCOMPUTER **282**

PORTABLE INDUSTRIAL TERMINAL, for use in the rugged industrial environment, is versatile and easy to use as an operator workstation or programming device. User selects RS232 or RS422 to interface to any ASCII computer. Features include: cast aluminum housing, 110-19.2K software selectable baud rates; 2×40 LCD; 65-key QWERTY style membrane keyboard; 1280 character memory buffer; conversation or edit mode; input power range AC/DC, 8-30V; customizing options. **MAPLE SYSTEMS, INC.**, 2615 W. CASINO RD., EVERETT, WA 98204 (206) 347-1292.

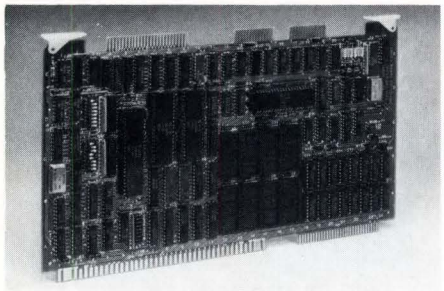
PORTABLE INDUSTRIAL TERMINAL **283**

SAVE TIME



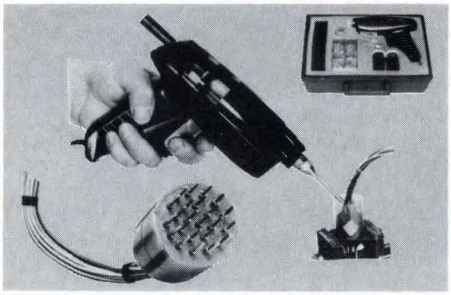
SINGLE BOARD COMPUTER/CONTROLLER/DEVELOPMENT SYSTEM. FEATURES; 40 TTL/CMOS Compatible I/O lines, RS-232 Serial Channel, 2 counter timers, Multifunction lines, 3 RAM/ROM/PROM sockets, In circuit EPROM/EEPROM programming, OPERATING SYSTEM, and Advanced feature, high level language FORTH. Complete w/case and power supply. $290/unit As low as $120 in OEM config. and quantity. New Micros Inc. 808 Dalworth, Grand Prairie, TX. 75050. (AC) 214-642-5494.

SINGLE BOARD COMPUTER **284**



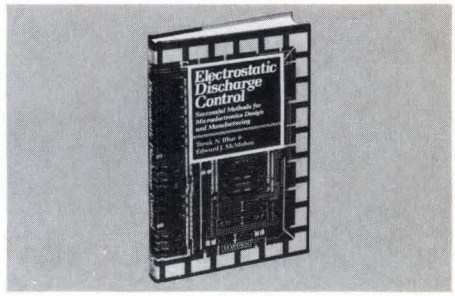
Z8000™ MULTIBUS™ SBC. Z8001 or Z8002 16-bit CPU (6 MHz); 32K or 128K DRAM (upgradable to 512K); up to 48K static RAM or EEPROM; up to 128K EPROM; 2 RS-232 ports (Z8030 SCC); 40 parallel I/O lines, six 16-bit counter-timers (Z8036 CIOs); vectored interrupts. EPROM Debug Monitor, MICRO CONCURRENT PASCAL, C, FORTH, VRTX. Dev. Z8000 software on IBM PC, PDP-11, Intel MDS, Olivetti M20 or 8080/Z80 CP/M system. Z8000™ Zilog, Multibus™ Intel Corp. SINGLE BOARD SOLUTIONS, 7669 Rainbow Dr., Cupertino, CA 95014. 408-253-0181.

SINGLE BOARD SOLUTIONS **285**



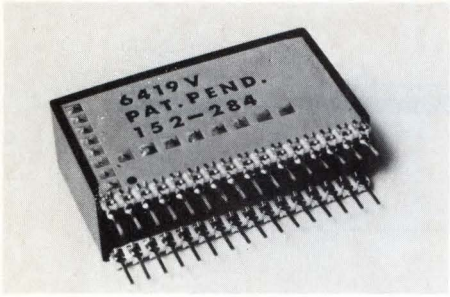
INSTANT CONNECTOR/POTTING KIT. Using polyethylene cartridges, connector contacts & heat gun, all in kit, inexpensive mating connectors can be made on the spot for countless connector configurations. Indispensable in test, maintenance, mfg., R&D and more. The polyethylene, an excellent insulator, is also a superior encapsulation/potting compound for backshells, circuit boards etc. Wiring Analyzers Inc., PO Box 4535, Chatsworth, CA 91311; 818/709-4500.

WIRING ANALYZERS **286**



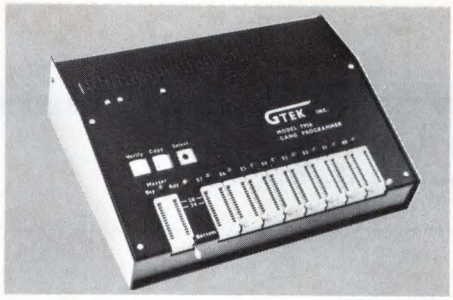
ELECTROSTATIC DISCHARGE CONTROL: Tarak N. Bhar & Edward J. McMahon, A complete guide to establishing, implementing, and monitoring an ESD control program. Static control materials, manufacturing processes, and special precautions are emphasized. Send $21.95 plus $2.00 to cover postage & handling to Hayden Book Company, 10 Mulholland Dr., Hasbrouck Hts., NJ 07604. Reference number 5689 must be included on your check or money order. If not satisfied, return the book undamaged, within 10 days for refund.

HAYDEN BOOK **287**



HPI-6418V/25618V 64kb/256 kilobyte dynamic RAM module reduces required PC board space by 70% compared to conventional memory modules. This memory module offers lower distributed capacitance, higher speeds & fewer support components. The module operates at a lower temp. & has higher speeds & reliability factor. The HPI-6418V operates on +5 volts & is ideal for computer/telecommunication applications. Units 100% tested. Pricing starts at $125.00 in 100 piece lots. Hy-Pac Inc., 760 San Aleso, Sunnyvale, CA 94086. (408) 745-0950.

DYNAMIC RAM MODULE **288**

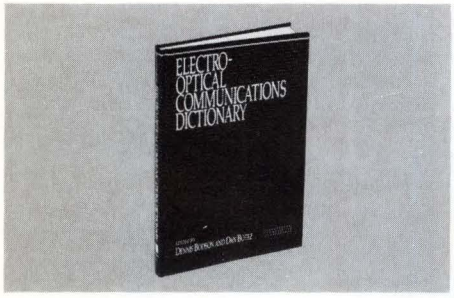


Need to Program Chips? GTEK's outstanding Model 7956 Gang Programmer with intelligent algorithms can copy 8 EPROMS at a time! The 7956 will program all popular chips on the market through the 27512 EPROMS. It also supports the Intel 2764A and 27128A chips. The 7956 also programs single chip processors. $879 stand alone; $1099 with RS232 option. GTEK, Inc., P.O. Box 289, Waveland, MS 39576; 601-467-8048.

GANG PROGRAMMER **289**

The NEW OMEGA SLC-II is a "stand-alone" computer voice simulator. The SLC-II will monitor any RS232C data stream, analyze the information and route it through any of 16 possible outputs to a data bank, computer terminal, or even call & brief you directly via the phone. Eighty-five actions can be stimulated over the phone. Programming is done in BASIC. For information in a RUSH, call (203) 359-7874. OMEGA ENGINEERING, INC., P.O. Box 4047, Stamford, CT. 06907.

SLC-II TALKING MONITOR **290**



ELECTRO—OPTICAL COMMUNICATIONS DICTIONARY: Dennis Bodson & Dan Botez, Eds., Never be at a loss for words with this complete reference to the most commonly used terms in electro-optical communications. Send $22.95 plus $2.00 to cover postage & handling to Hayden Book Company, 10 Mulholland Dr., Hasbrouck Hts., NJ 07604. Reference number 0961 must be included on your check or money order. If not satisfied, return the book undamaged, within 10 days for refund.

COMMUNICATIONS DICTIONARY **291**

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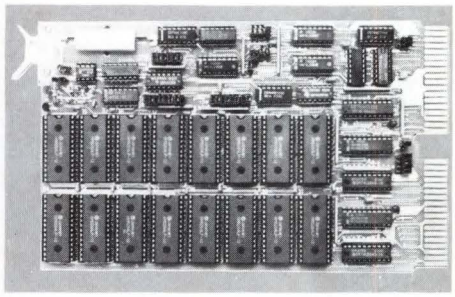
MODEL 106 LINK SIMULATOR **292**



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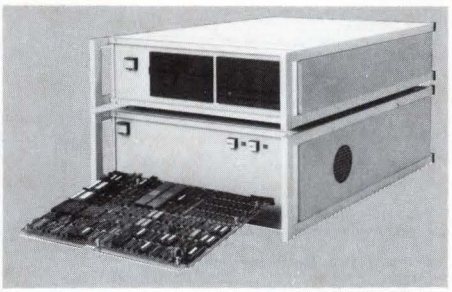

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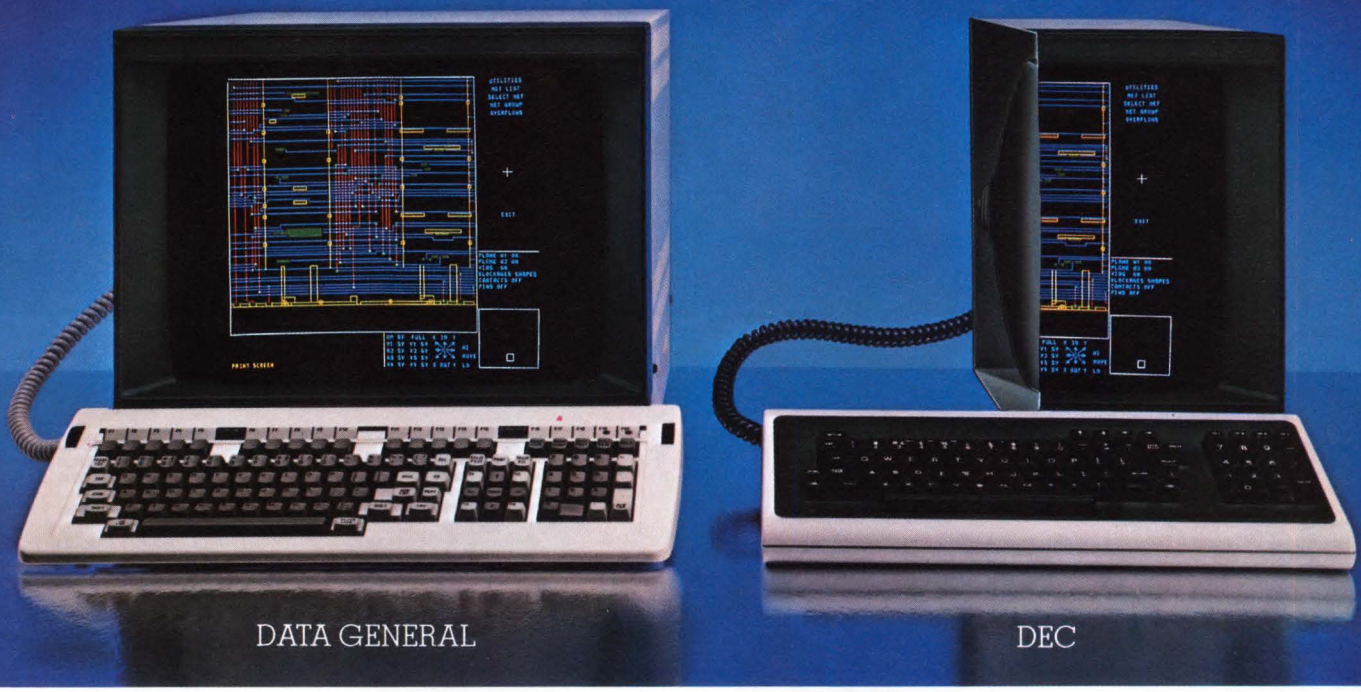

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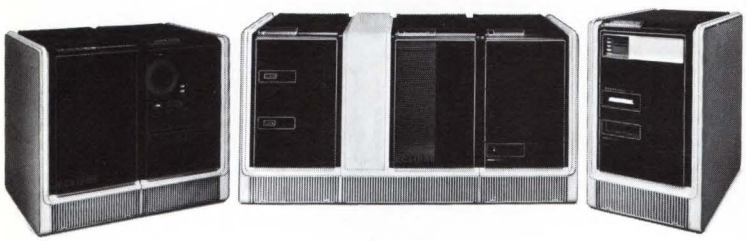

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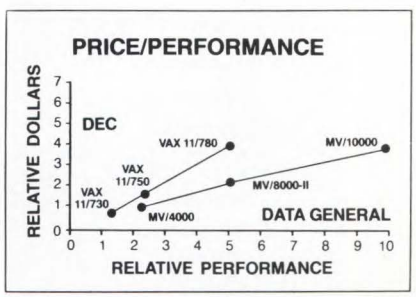

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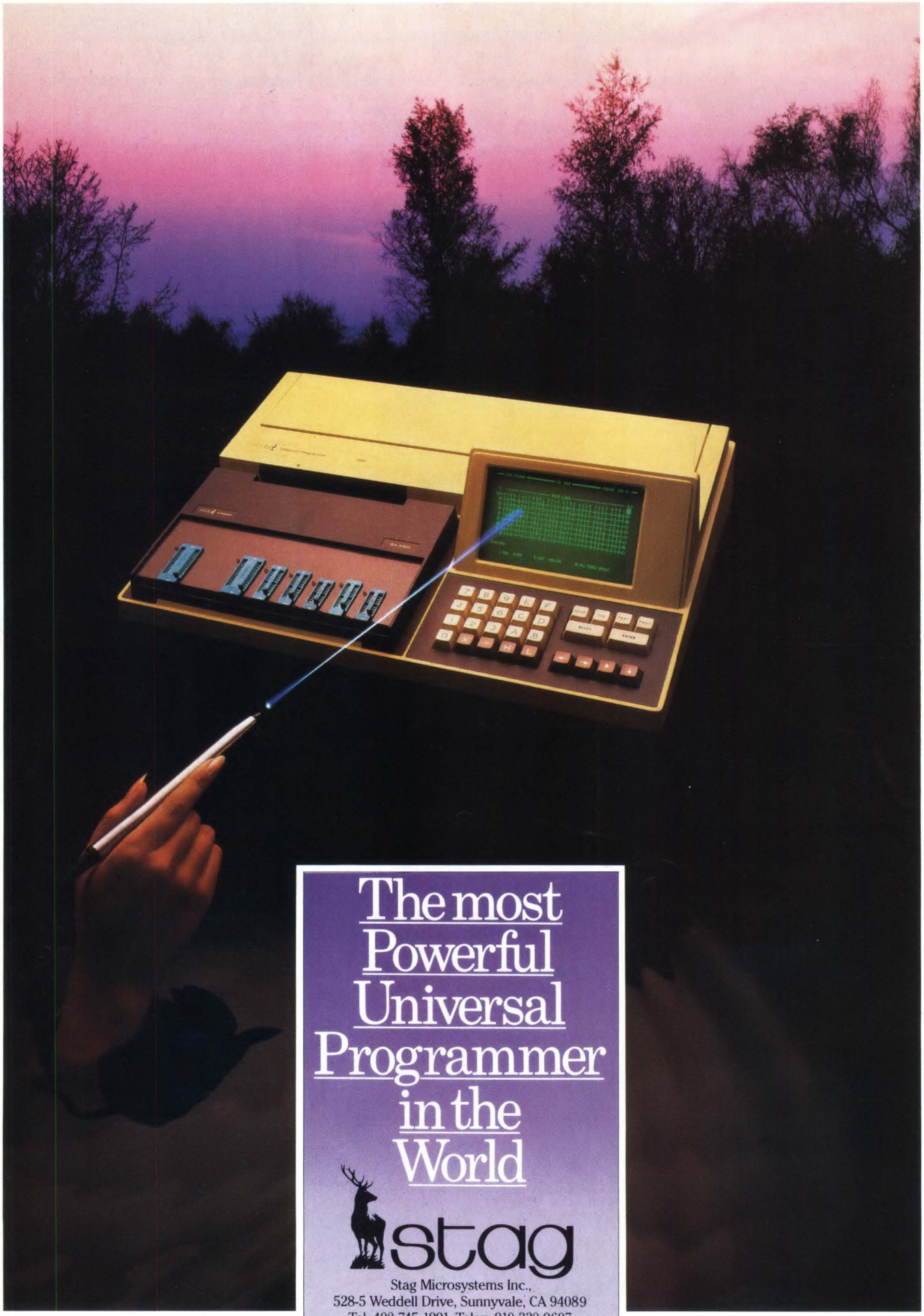

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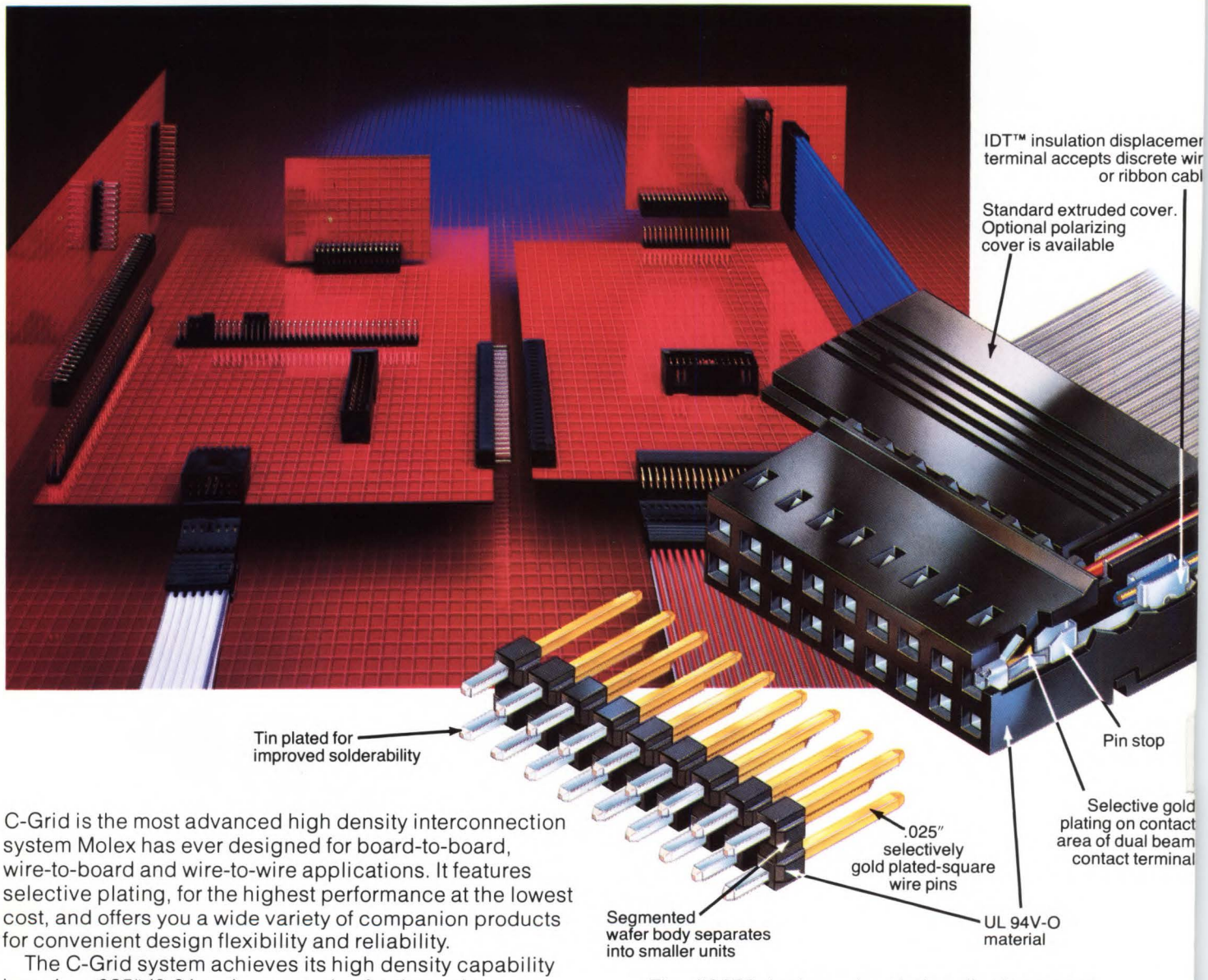

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