SYSTEMS LOGIC/PERIPHERAL

WD6030

Cache/DRAM and

Channel Control Device

15

WESTERN DIGITAL

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ADDITIONAL REFERENCES

IBM PS/2 Model 70 Technical Reference Manual
IBM PS/2 Model 80 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD6030 integrated circuit forms part of Western Digital's innovative WD6500 chip set. It facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture, decreases design complexity, saves space by combining the functions of many discrete arrays and components, and reduces system cost and increases system reliability.

The Extended Setup Facility, or ESF, is a Western Digital enhancement designed to allow more functionality such as a Winchester Controller, LAN Adapter, or additional Serial Port to be added onto the system board. It provides product differentiation at the system level and helps reduce costs. The block diagram in Figure 1 illustrates a typical system utilizing the WD6500 chip set. Devices with bold outlines are available from Western Digital Corporation.

1.2 FEATURES

- Hardware (register level) and software compatible to the IBM Personal System/2 Micro Channel implementations
- Direct-Mapped Cache Controller
  - Direct-mapped, write-through implementation
  - Line size equals four bytes
  - Page mode hits on cache misses
- DRAM Controller
  - Memory Configuration Registers
  - Complete 256 KB, 1 MB, and 4 MB DRAM support
  - Ability to mix DRAM sizes in different banks
  - Support for up to four banks (up to 64 M-Bytes) of memory
- Channel Controller
- Channel Buffer Controls
- Programmable Wait States
- Shadow RAM for fast BIOS execution
- Extended Setup Facility (ESF)
- Low Power 0.9 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

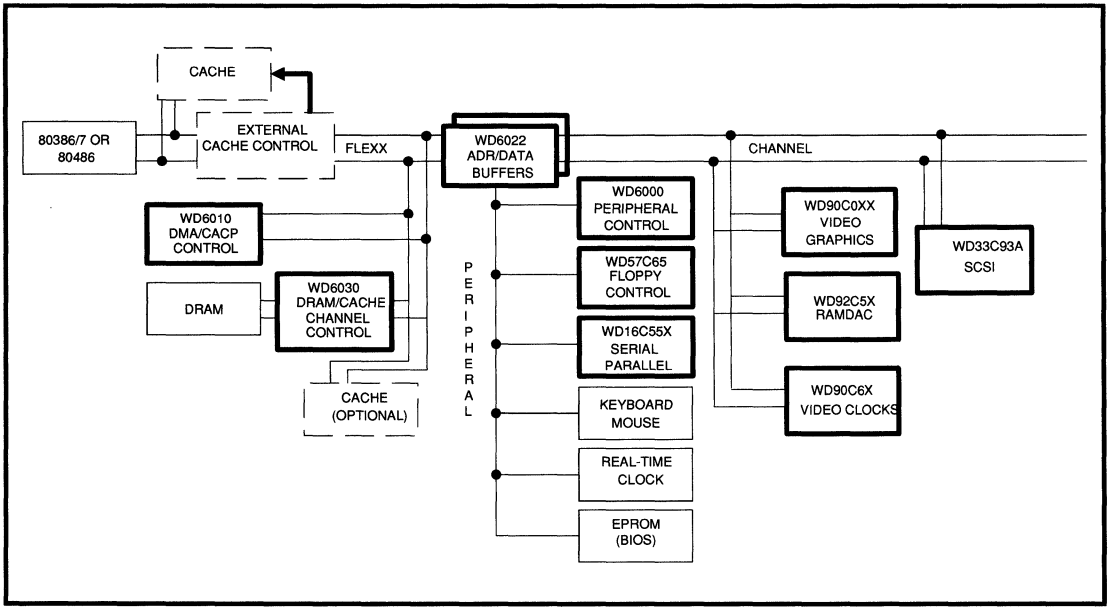

Figure 1. System Block Diagram

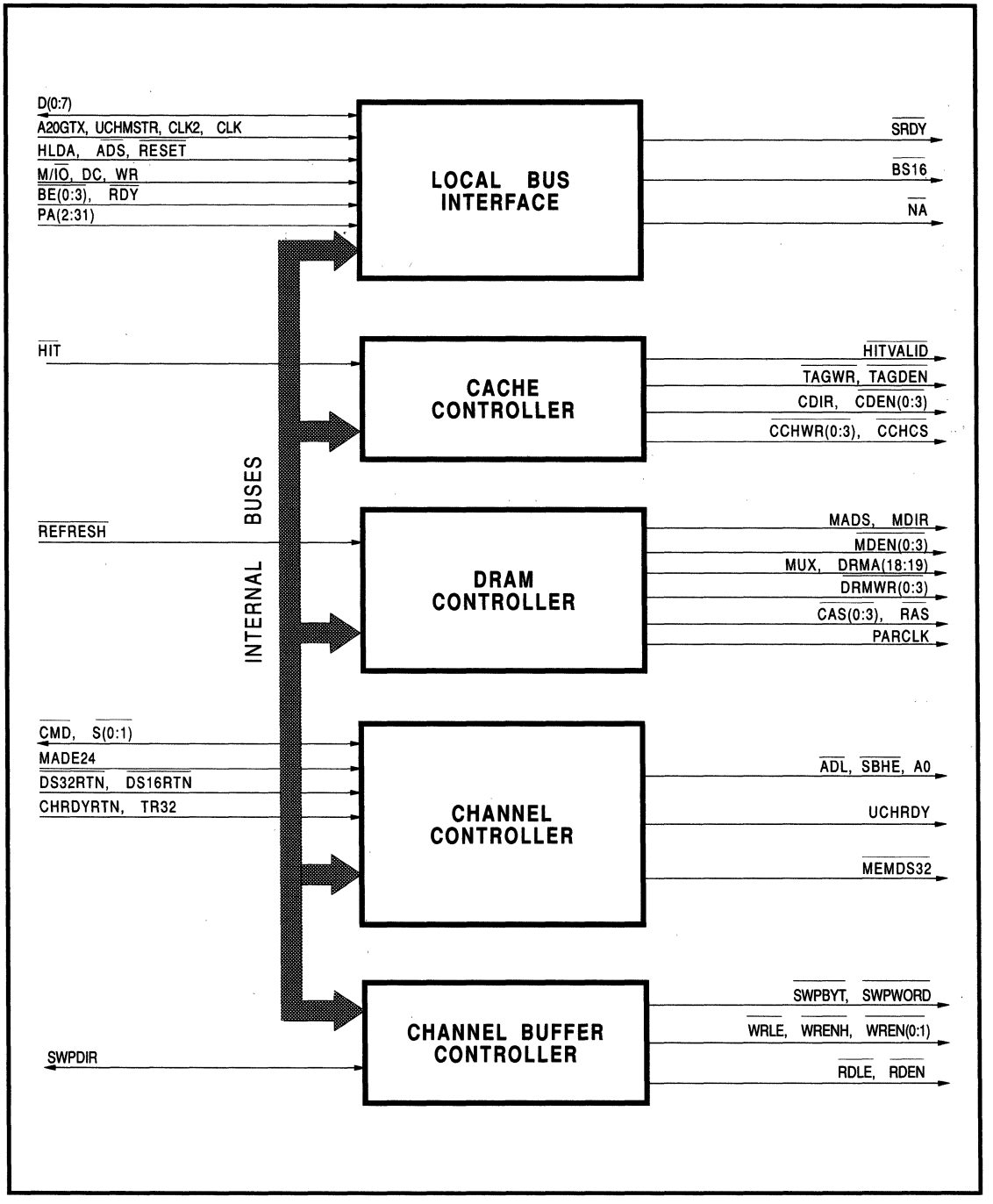

Figure 2. WD6030 Block Diagram

2.0 PIN DESCRIPTION

The signals assigned to different pins are grouped according to their function and discussed individually in Table 1.

2.1 LOCAL BUS INTERFACE

The WD6030 sits directly on the CPU bus, controlling the CPU/DMA accesses to local memory, I/O, and the Channel. The WD6030 also controls Micro Channel master accesses to the local memory.

2.2 CACHE CONTROLLER

The Cache Controller in the WD6030 implements a direct-mapped cache for the 80386, which improves performance significantly by allowing the majority of memory cycles to be run at zero wait states. These signals form part of the interface between the cache controller and the external cache and TagRAMs. See Section 3.0 for a detailed description of the cache controller.

2.3 DRAM CONTROLLER

The DRAM Controller supports Page Mode and allows DRAMs of different sizes to be used together. Pipelined operation, which allows fast accesses to the DRAMs, is also supported.

2.4 CHANNEL CONTROLLER

The Channel controller implements the interface to the system board. The WD6030 generates the Channel interface signals whenever the CPU or the DMA controller accesses any resource on the Channel.

2.5 CHANNEL BUFFER CONTROLLER

The Channel Buffer signals control the data buffers between the local processor data bus and the Channel data bus. The data buffers are integrated in the WD6022 device providing the interface to that device. Note that the WD6022 must be strapped in the Data Buffer Mode.

2.6 MISCELLANEOUS

This set of signals includes the V_{SS} and V_{DD} signal pins, as well as the reserved pins, which should not be connected but left open in the system.

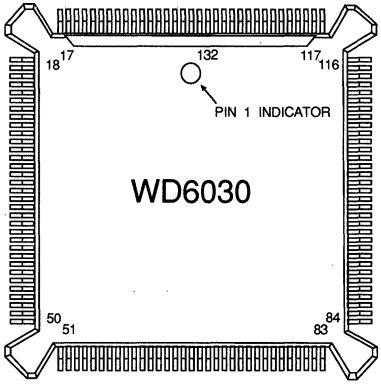

Figure 3. 132-PIN PLASTIC QUAD FLAT PACK

PIN	–	NAME	PIN	–	NAME	PIN	–	NAME	PIN	–	NAME
1	–	PA2	34	–	N.C.	67	–	WREN1	100	–	CDEN2
2	–	PA3	35	–	TR32	68	–	WRENH	101	–	CDEN1
3	–	PA4	36	–	CHRDYRTN	69	–	WRLE	102	–	CDEN0
4	–	PA5	37	–	DS16RTN	70	–	SWPWORD	103	–	CDIR
5	–	PA6	38	–	DS32RTN	71	–	V_{SS}	104	–	TAGWR
6	–	PA7	39	–	V_{DD}	72	–	SWPBYT	105	–	TAGDEN
7	–	PA8	40	–	MEMDS32	73	–	SWPDIR	106	–	V_{SS}
8	–	PA9	41	–	UCHRDY	74	–	RAS	107	–	HITVALID
9	–	PA10	42	–	S0	75	–	CAS0	108	–	SRDY
10	–	PA11	43	–	S1	76	–	CAS1	109	–	MADS
11	–	PA12	44	–	V_{SS}	77	–	CAS2	110	–	RDY
12	–	PA13	45	–	CMD	78	–	CAS3	111	–	HIT
13	–	PA14	46	–	A0	79	–	DRMWR0	112	–	MADE24
14	–	PA15	47	–	SBHE	80	–	DRMWR1	113	–	BE0
15	–	PA16	48	–	ADL	81	–	DRMWR2	114	–	BE1
16	–	PA17	49	–	N.C.	82	–	DRMWR3	115	–	BE2
17	–	V_{SS}	50	–	V_{SS}	83	–	V_{SS}	116	–	V_{SS}
18	–	PA18	51	–	PARCLK	84	–	DRMA19	117	–	BE3
19	–	PA19	52	–	NA	85	–	DRMA18	118	–	W/R
20	–	PA20	53	–	BS16	86	–	MUX	119	–	D/C
21	–	PA21	54	–	D0	87	–	MDEN3	120	–	M/IO
22	–	PA22	55	–	D1	88	–	MDEN2	121	–	ADS
23	–	PA23	56	–	D2	89	–	MDEN1	122	–	V_{DD}
24	–	V_{DD}	57	–	D3	90	–	MDEN0	123	–	REFRESH
25	–	PA24	58	–	V_{SS}	91	–	MDIR	124	–	RESET
26	–	PA25	59	–	D4	92	–	V_{DD}	125	–	HLDA
27	–	PA26	60	–	D5	93	–	CCHCS	126	–	UCHMSTR
28	–	V_{SS}	61	–	D6	94	–	CCHWR3	127	–	A20GTX
29	–	PA27	62	–	D7	95	–	V_{SS}	128	–	N.C.
30	–	PA28	63	–	RDEN	96	–	CCHWR2	129	–	TEST
31	–	PA29	64	–	RDLE	97	–	CCHWR1	130	–	CLK
32	–	PA30	65	–	WREN0	98	–	CCHWR0	131	–	CLK2
33	–	PA31	66	–	VDD	99	–	CDEN3	132	–	V_{SS}

PIN NO.	NAME	TYPE	FUNCTION
			LOCAL BUS INTERFACE
127	A20GTX	I	GATE At power-up, the state of A20GTX is latched at the trailing edge of $\overline{\text{RESET}}$ and, in conjunction with UCHMSTR, determines the frequency at which the WD6030 operates. The following table lists the clock frequencies available. **FREQUENCY / UCHMSTR / A20GTX** 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1 33 MHz / 1 / 0 After power-up, A20GTX is used to wrap around addresses in the Real and Virtual 8086 modes of the processor. The signal is generated by the WD6010 and is a combination of the A20GATE generated by the 8742 and the Alternate Gate A20 signal from Port 0092H, bit 1. The WD6030 uses this signal internally to generate the address for memory accesses. Depending on the frequency configuration required, this signal should be pulled up/down with a 470K resistor.
126	UCHMSTR	I	CHANNEL MASTER At power-up, the state of UCHMSTR is latched at the trailing edge of $\overline{\text{RESET}}$, and in conjunction with A20GTX, determines the frequency at which the WD6030 operates. After power-up, UCHMSTR functions as a signal from the Central Arbitration Control Point (CACP) in the WD6010. When active, it indicates that a Channel master has the bus. A 2.7K resistor is used to pull up/down this signal.
54 - 57 59 - 62	D0 - D7	I/O	CHANNEL DATA BUS The WD6030 internal registers are programmed via the Channel Data Bus. These registers can only be accessed by 8-bit operations. When the registers are accessed, a Channel cycle ($\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{CMD}}$, etc.) is initiated, and the controls for the Channel buffers are activated to complete the cycle.
131 130	CLK2 CLK	I I	CLOCKS Both CLK and CLK2 are CMOS level signals. CLK is of the same frequency as the processor clock, while CLK2 is twice the frequency of the processor clock. The WD6030 shares CLK2 with the CPU.
125	HLDA	I	HOLD ACKNOWLEDGE HLDA indicates that the CPU has given control of the system local bus to a different master (Channel Bus Master or DMA Controller). HLDA prevents non-system CPU accesses to locations 0000-00FFH in the WD6000 during master cycles.

Table 1. Pin Description

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PIN NO.	NAME	TYPE	FUNCTION
124	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ $\overline{\text{RESET}}$ is driven by the WD6010 and is asserted at power-on. It initializes all internal state machines and registers to the power-up default values.
121	$\overline{\text{ADS}}$	I	$\overline{\text{ADDRESS STROBE}}$ The WD6030 uses $\overline{\text{ADS}}$ to keep track of bus cycles on the CPU address, data, and status busses.
120 119 118	M/$\overline{\text{IO}}$ D/$\overline{\text{C}}$ W/$\overline{\text{R}}$	I	MEMORY $\overline{\text{I/O}}$, DATA/$\overline{\text{CONTROL}}$, WRITE/$\overline{\text{READ}}$ The M/IO, D/C, and W/R signals define the type of bus cycle being executed on the CPU local bus. When the CPU is in control of the CPU local bus, M/IO, D/C, and W/R are input from the CPU. When the WD6010 DMA Controller is in control of the CPU local bus, M/IO, D/C, and W/R are input from the WD6010.
117 115 114 113	$\overline{\text{BE3}}$ $\overline{\text{BE2}}$ $\overline{\text{BE1}}$ $\overline{\text{BE0}}$	I	$\overline{\text{BYTE ENABLES}}$ These Byte-Enable signals are driven by the CPU, the WD6010 DMA controller, or the Channel master.
110	$\overline{\text{RDY}}$	I	$\overline{\text{READY}}$ The Ready signal is used to track bus cycles on the CPU local bus. The $\overline{\text{READY}}$ signals from the chip set are combined externally to generate one $\overline{\text{RDY}}$ signal to the CPU.
1 - 16 18 - 23 25 - 27 29 - 33	PA2 - PA17 PA18 - PA23 PA24 - PA26 PA27 - PA31	I	PROCESSOR ADDRESS BUS PA2 through PA31 is the local processor address bus on the motherboard and interfaces directly with the 80386/80486 address bus. This address bus is driven by the CPU, DMA Controller, or a Channel Master.
108	SRDY	O	SYSTEM READY The WD6030 generates a READY signal for system resources not on the local bus, including the local DRAM. The SRDY signal is generated whenever the 80386, 80486, or DMA Controller performs a bus cycle that is neither an access to the numeric coprocessor (80387 or Weitek 3167) nor a memory access resulting in a cache hit. This signal is logically ORed on the system board with the other sources of READY to generate READY to the CPU. Note that the default for the READY signal to the 80386, 80486, or DMA Controller is a "not ready" interface.

M/$\overline{\text{IO}}$	D/$\overline{\text{C}}$	W/$\overline{\text{R}}$	WD6030 OPERATION
0	0	0	Reserved
0	0	1	Reserved
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Memory Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

Table 1. Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
53	BS16	O	BUS SIZE 16 BS16 is used to indicate whether the CPU or WD6030 is accessing a 32-bit, 16-bit, or 8-bit port. When a 32-bit port is accessed, BS16 is de-asserted and all byte enables should be active. When a 16-bit or 8-bit port is accessed, BS16 is asserted and the byte enables are sampled to determine whether the access is to a 16-bit or 8-bit port.
52	NA	O	NEXT ADDRESS The Next Address signal is asserted when a pipelined cycle can be supported by the system. The WD6030 requests a pipeline cycle whenever a cycle other than a Cache-Read-Hit occurs.
			CACHE CONTROLLER
111	HIT	I	CACHE HIT The external tag subsystem sends this signal to the WD6030 to indicate that the current cycle resulted in a match of the Tag. Depending on whether or not the DRAM cycle can be cached, this signal is internally qualified to generate a cache hit indication. If a cache hit occurs on a memory read cycle, a zero wait state operation is accomplished.
107	HITVALID	O	CACHE HIT QUALIFIER The WD6030 asserts the HITVALID signal to indicate that the HIT signal from the tag subsystem is valid and can be sampled by the external logic. HIT and HITVALID are logically ANDed externally to assert the READY signal to the 80386, 80486, or DMA Controller, resulting in a zero wait state cycle on a Cache-Read-Hit. For a cycle requiring a cache update, HIT may be inactive in the early part of the cycle and active in the latter part when the Tag is updated. HITVALID is de-asserted in the latter part of the cycle to prevent generating a spurious READY signal to the CPU.
105	TAGDEN	O	TAG DATA ENABLE TAGDEN opens a "Tag Buffer", such as a 74F244, during a Tag update cycle. Tag updates occur on a Cache-Miss cycle on cachable memory areas.
104	TAGWR	O	TAG WRITE TAGWR updates the Tag in the TagRAM for a Cache-Update cycle. A pipelined cycle is requested and TAGWR updates the Tag value when a Cache-Miss occurs.
103	CDIR	O	CACHE BUFFER DIRECTION CDIR determines the direction of the data flow between the Processor Data Bus (PD) and Cache Data Bus (CD) for the 74F245 buffers. The 74F245 buffers minimize the loading on the CPU local bus and permit more relaxed timings on the Cache Data SRAMs. The 74F245 buffers also permit the use of SRAMs which do not require the Output Enable function. **CDIR** **Direction** 0 CD(0:31) to PD(0:31) 1 PD(0:31) to CD(0:31)

Table 1 Pin Description (Continued)

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PIN NO.	NAME	TYPE	FUNCTION
102 101 100 99	CDEN0 CDEN1 CDEN2 CDEN3	O	CACHE BUFFER ENABLES CDEN(0:3) provides the enable signals for the 74F245 buffers between the Processor Data Bus (PD) and the Cache Data Bus (CD). Each data byte has a separate enable which is qualified internally by the byte enable from the 80386, 80486, or DMA Controller. Figure 4 illustrates a typical cache cycle with page hits.
98 97 96 94	CCHWR0 CCHWR1 CCHWR2 CCHWR3	O	DATA CACHE WRITE CCHWR(0:3) individually enables each of the four bytes of the cache data. The WD6030 asserts the write signal corresponding to the byte enable asserted during the cycle.
93	CCHCS	O	DATA CACHE CHIP SELECT CCHCS is the Chip Select signal to the Cache Data SRAMs. CCHCS is always asserted at the beginning of a cycle, permitting the slowest possible SRAMs to be used. CCHCS is only de-asserted for a cache update operation.
			DRAM CONTROLLER
123	REFRESH	I	REFRESH REFRESH from the WD6010 indicates that a Refresh cycle is in progress and a Memory Read cycle is taking place run on the local bus. When REFRESH is asserted, the DRAM controller initiates a RAS-only cycle, with the address supplied by the WD6010. Simultaneously, a Memory Read cycle is initiated on the Channel. A READY signal is generated when both cycles have been completed.
109	MADS	O	MEMORY ADDRESS STROBE The MADS signal from the WD6030 latches all addresses for the external cache data and DRAM to the external address latches 74AS373. Figures 5 through 8 illustrate a typical cycle to the DRAM.
91	MDIR	O	DRAM BUFFER DIRECTION MDIR determines the direction of the data flow for the 74F657 bidirectional transceivers between the Processor Data Bus (PD), and the DRAM Data Bus (MD). **MDIR** **Direction** 0 MD(0:31) to PD(0:31) 1 PD(0:31) to MD(0:31)
90 89 88 87	$\overline{\text{MDEN0}}$ $\overline{\text{MDEN1}}$ $\overline{\text{MDEN2}}$ $\overline{\text{MDEN3}}$	O	$\overline{\text{DRAM BUFFER ENABLES}}$ $\overline{\text{MDEN}}$(0:3) are the enable signals for the 74F657 transceivers between the Processor Data Bus (PD) and DRAM Data Bus (MD). Each data byte has its own enable which is qualified internally by the byte enables from the 80386, 80486, or DMA Controller.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
86	MUX	O	ADDRESS MULTIPLEXER MUX interfaces with the external address multiplexers and controls the generation of the row and column addresses to the DRAM. **MUX** **Function** 0 Row Address 1 Column Address
85 84	DRMA18 DRMA19	O	DRAM SPLIT MEMORY ADDRESS DRMA(18:19) provide Address Bits 18 and 19 for DRAM accesses, which are sent to the external DRAM address multiplexers. These signals implement the split addressing memory feature.
82 81 80 79	DRMWR3 DRMWR2 DRMWR1 DRMWR0	O	DRAM WRITE DRMWR(3:0) are the enable signals to the system DRAM. Each data byte has a separate enable which is internally qualified by the byte enables from the 80386, 80486, or DMA Controller. The four write enable signals to the DRAM should be buffered by a 74AS1832.
78 77 76 75	CAS3 CAS2 CAS1 CAS0	O	DRAM CAS Each of the four banks has its own CAS signal. The bank being accessed has its CAS signal asserted during a cycle. At the end of the cycle, all CAS signals are de-asserted. These signals should be buffered by a 74AS1832. Page Mode DRAMs can be employed because the WD6030 de-asserts this signal at the end of each cycle. Static Column DRAMs may also be used, however, they will operate in Page Mode.
74	RAS	O	DRAM RAS RAS connects to the RAS inputs of all the DRAMs and should be buffered by a 74AS1832. This signal is active in Page Mode as long as the accesses remain within the same row. RAS remains active even if the accesses are made to addresses in different memory banks which share the same row address, because the row addresses are shared by the different memory banks. In normal RAS/CAS Mode, a RAS precharge takes place for every DRAM access.
51	PARCLK	O	PARITY ERROR CLOCK PARCLK is used as a clock to latch in parity error information during DRAM read cycles. At the rising edge of this signal, the parity error information is latched in. The Parity Error Latch function is implemented on the system board.
			CHANNEL CONTROLLER
45	CMD	I/O	COMMAND CMD defines when data to or from the Channel is valid. CMD is an input during Channel Master Cycles and an output during all other cycles.
43 42	S1 S0	I/O	CHANNEL STATUS S1 and S0, along with M/IO, identify the type of cycle taking place on the channel. S1 and S0 are input signals during a Channel Master Cycle and an output during all other cycles.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
112	MADE24	I	MEMORY ADDRESS ENABLE 24 MADE24 is asserted by the channel when an address greater than 16 Mbytes is placed on the Processor Address Bus (PA). The WD6022 Address Buffer Device de-asserts MADE24 whenever the CPU or DMA Controller performs a Channel Memory access above the 16 Mbyte boundary.
38	DS32RTN	I	DATA SIZE 32 RETURN DS32RTN corresponds to, and directly interfaces with, the DS32RTN signal on the Channel and is generated by ORing all the CDDS32N signals on the Channel. Asserting DS32RTN during a Channel cycle indicates that the slave being addressed is capable of transferring 32 bits of data.
37	DS16RTN	I	DATA SIZE 16 RETURN DS16RTN corresponds to, and directly interfaces with, the DS16RTN signal on the Channel and is generated by ORing all the CDDS16N signals on the Channel. Asserting DS16RTN during a Channel cycle indicates that the slave being addressed is capable of transferring 16 bits of data.
36	CHRDYRTN	I	CHANNEL READY RETURN CHRDYRTN is an AND of all CDCHRDY signals present on the Channel, i.e., the individual Channel slots, video subsystem, WD6000 (IORDY) and the system board DRAM (UCHRDY). A Channel slave uses CHRDYRTN to extend the Channel cycle.
35	TR32	I	TRANSLATE 32 TR32 facilitates communication between a 16-bit master and a 32-bit slave. TR32 generates the necessary control signals used in data swapping. When asserted, it indicates that a 16-bit master has the Channel and that the Central Translator function should be turned on. The CPU and DMA Controller are 32-bit masters, therefore, the WD6022 de-assertes TR32 when the Channel is accessed by the CPU or DMA Controller.
48	ADL	O	ADDRESS DECODE LATCH ADL provides the slave with an appropriate method to latch valid addresses and status signals.
47 46	SBHE A0	O	SYSTEM BYTE HIGH ENABLE ADDRESS BIT 0 SBHE and A0 are used by 16-bit slaves to determine the byte that contains data during the current transfer of data. **A0 SBHE DATA AVAILABLE** 0 0 D(0:15) 0 1 D(0:7) 1 0 D(8:15) 1 1 Reserved Note that this signal is not used by 8-bit or 32-bit slaves. The latter uses BE(0:3) signals to perform the same function.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
41	UCHRDY	O	LOCAL DRAM CHANNEL READY UCHRDY is used to extend cycles when a Channel Master accesses the system board DRAM. UCHRDY is also used in the external logic to generate CHRDYRTN. Figures 9 through 12 indicate typical Channel Master cycles to the system board DRAM.
40	$\overline{\text{MEMDS32}}$	O	LOCAL DRAM MEMORY SIZE 32 $\overline{\text{MEMDS32}}$ is used in external logic on the system board to generate the $\overline{\text{DS16RTN}}$ and $\overline{\text{DS32RTN}}$ signals. $\overline{\text{MEMDS32}}$ is driven by the WD6030 when a Channel Master accesses the system board DRAM and indicates that the memory accessed is 32 bits wide.
			CHANNEL BUFFER CONTROLLER
73	SWPDIR	I/O	SWAP DIRECTION At power-up, the state of SWPDIR is latched by the trailing edge of RESET to determine the presence or absence of the numeric processor. **SWPDIR** **RESET STATE FUNCTION** 0 Numeric coprocessor present 1 Numeric coprocessor absent After power-up, SWPDIR indicates the direction of the byte and word swap buffers. SWPDIR de-asseted indicates a read operation, byte swap D(0:7) to D(8:15) or a Channel Master write operation, word swap D(0:15) to D(16:31). SWPDIR asserted indicates a write operation, byte swap D(8:15) to D(0:7) or a Channel Master read operation, word swap D(16:31) to D(0:15).
72	SWPBYT	O	BYTE SWAP When the CPU or DMA accesses an 8-bit port, the cycle is split into two. This signal is used to swap data to the correct bytes. D(0:7) is swapped to D(8:15) for a read and normal operation D(8:15) is swapped to D(0:7) for a write operation
70	SWPWORD	O	WORD SWAP SWPWORD swaps words when a 16-bit Channel Master communicates with a 32-bit slave. The cycle is split into two and SWPWORD is used to swap data to the correct word. D(16:31) is swapped to D(0:15) for a Channel Master read operation, D(0:15) is swapped to D(16:31) for a Channel Master write operation. This function is known as steering.
69	WRLE	O	WRITE LATCH ENABLE WRLE latches the write data during a CPU or DMA write operation to the Channel. It provides the write-data-hold time required by the Channel during these operations. WRLE also latches data when the CPU or DMA writes to an 8-bit port and the cycle must be split in two.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
68 67 65	WRENH WREN1 WREN0	O	WRITE ENABLE (HIGH, 0:1) These signals enable the buffer during data flow from the Processor Data Bus (PD) to the Channel Data Bus (D). These signals control byte 0 (0:7) (WREN0), byte 1 (8:15) (WREN1), and the upper word (16:31) (WRENH). These signals are valid when the CPU or DMA controller performs a write operation to the Channel or when a Channel Master performs a read operation from the system board DRAM.
64	$\overline{\text{RDLE}}$	O	$\overline{\text{READ LATCH ENABLE}}$ $\overline{\text{RDLE}}$ is the latch enable signal for byte 0 (0:7). When the CPU or DMA controller performs a cycle to an 8-bit device on the Channel, the cycle is split in two. This signal latches the first 8 bits (0:7) during the first cycle, reads the next 8 bits (8:15) during the second cycle, and then presents the 16 bits to the CPU.
63	$\overline{\text{RDEN}}$	O	$\overline{\text{READ ENABLE}}$ $\overline{\text{RDEN}}$ enables the buffer for the Processor Data Bus (PD) when the data flows from the Channel Data Bus (D) to the Processor Data Bus (PD). $\overline{\text{RDEN}}$ is asserted when the CPU or DMA controller performs a read from the Channel or when a Channel Master writes to the system board DRAM.
			MISCELLANEOUS
24, 39, 66, 92, 122	V_{DD}	I	+5 V Power Supply
17, 28, 44, 50, 58, 71, 83, 95, 106, 116, 132	V_{SS}	I	0 V Ground
34, 49, 128	N.C.		Not connected
129	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low signal that facilitates board-level testing. When low, this signal tri-states all outputs and bidirectional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bidirectional lines are enabled by the WD6030.

Table 1 Pin Description (Continued)

Table 2 details the state of the pins on the WD6030 after a reset.

SIGNAL	BUS STATE AFTER RESET
D (0:7)	Z*
NA, BS16	High
S (0:1), ADL, CMD	High
SBHE, A0	High
MEMDS32	High
UCHRDY, SRDY	High
MADS	High
HITVALID	High
CCHCS	High
CDIR, MDIR	Low
CCHWR (0:3), CDEN (0:3)	High
TAGWR, TAGDEN	High
RAS, CAS (0:3)	High
MUX, PARCLK	Low
DRMWR (0:3)	High
DRMA (18:19)	High
MDEN (0:3)	High
RDEN	High
RDLE	Low
WREN (0:1), WRENH	High
WRLE	Low
SWPBYT, SWPWORD	High
SWPDIR	High
* Z = High Impedance	

Table 2. Pin State After Reset

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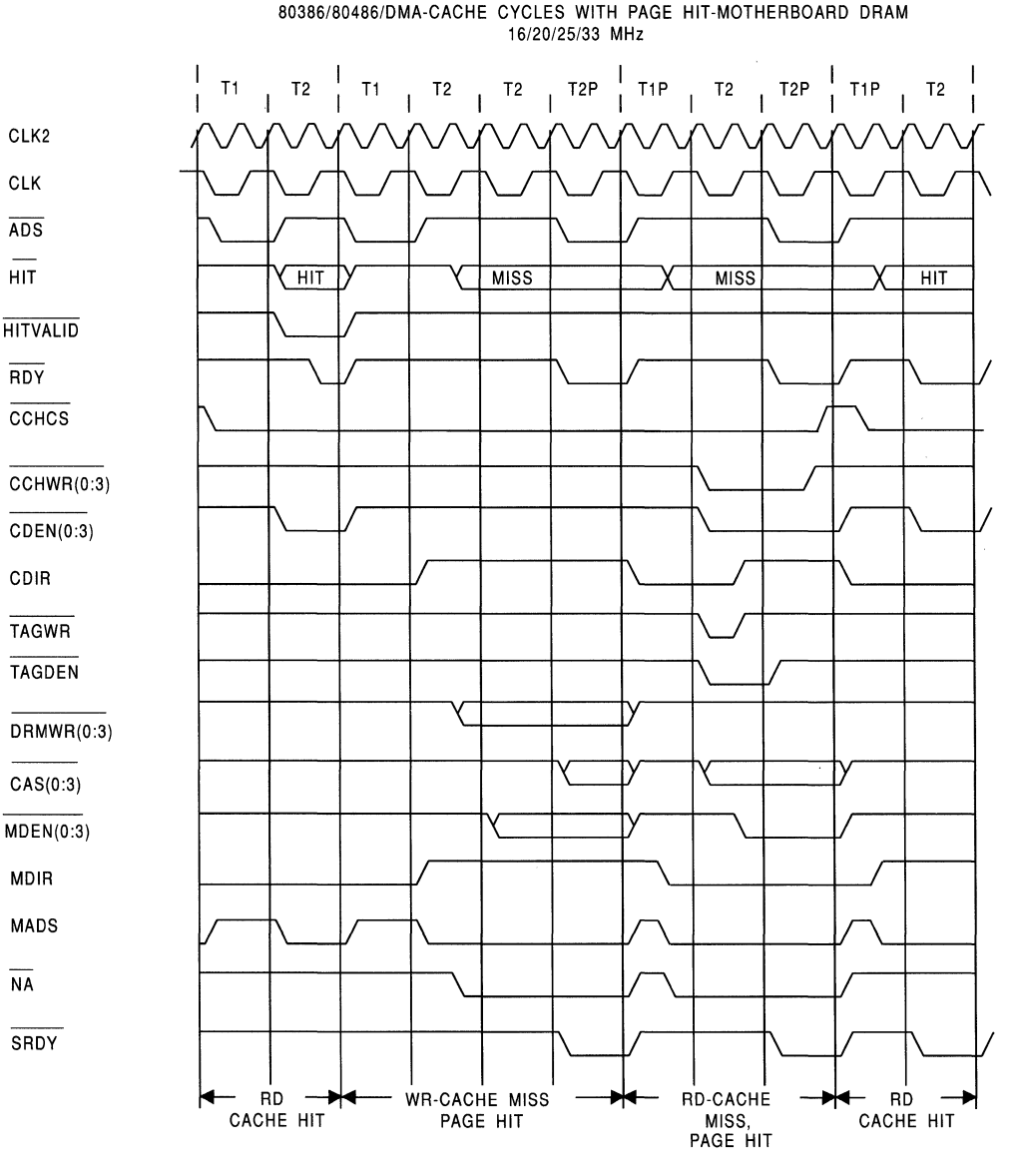

Figure 4. Cache Cycle with Page Hits

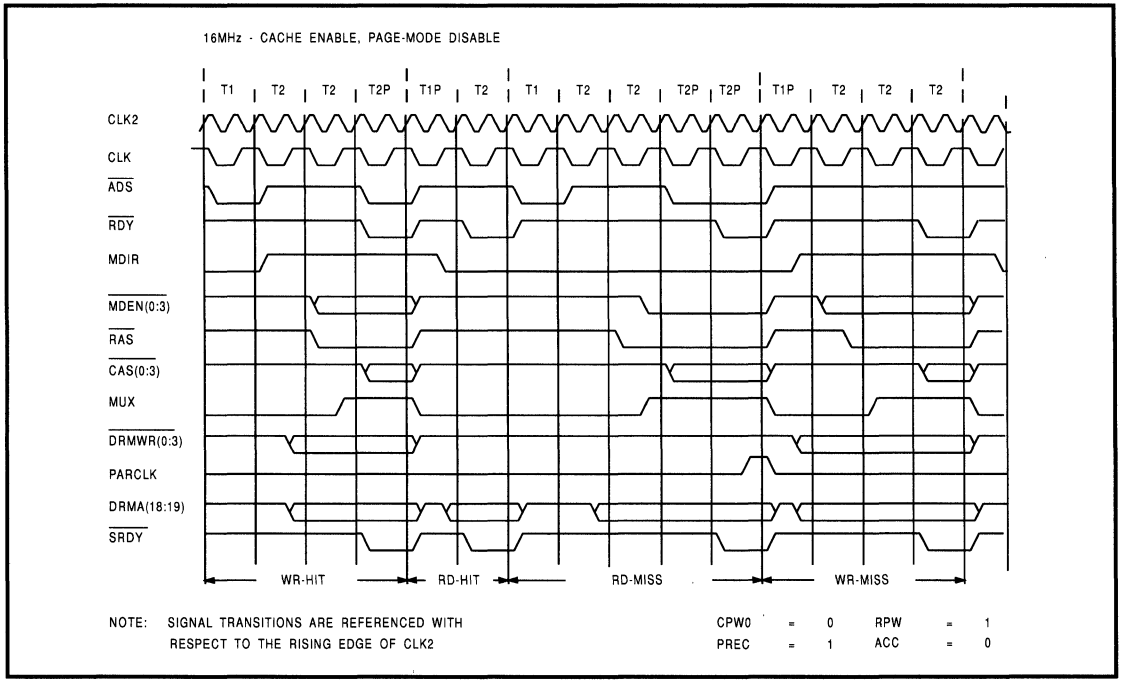

Figure 5. 80386/80486/DMA 16 MHz DRAM Access

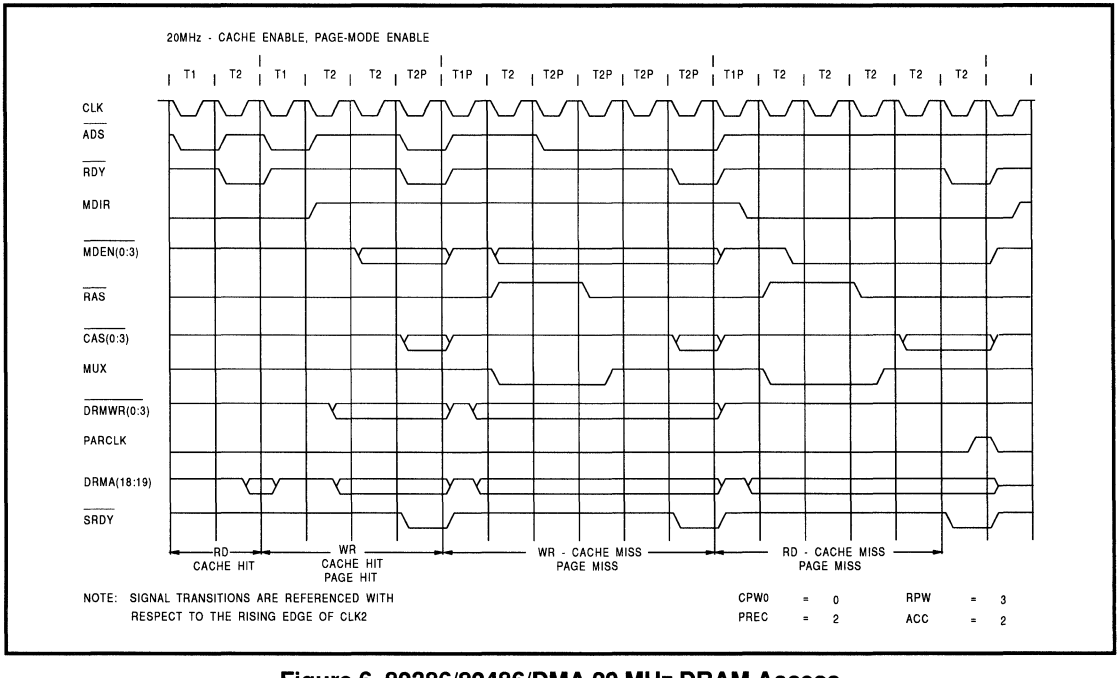

Figure 6. 80386/80486/DMA 20 MHz DRAM Access

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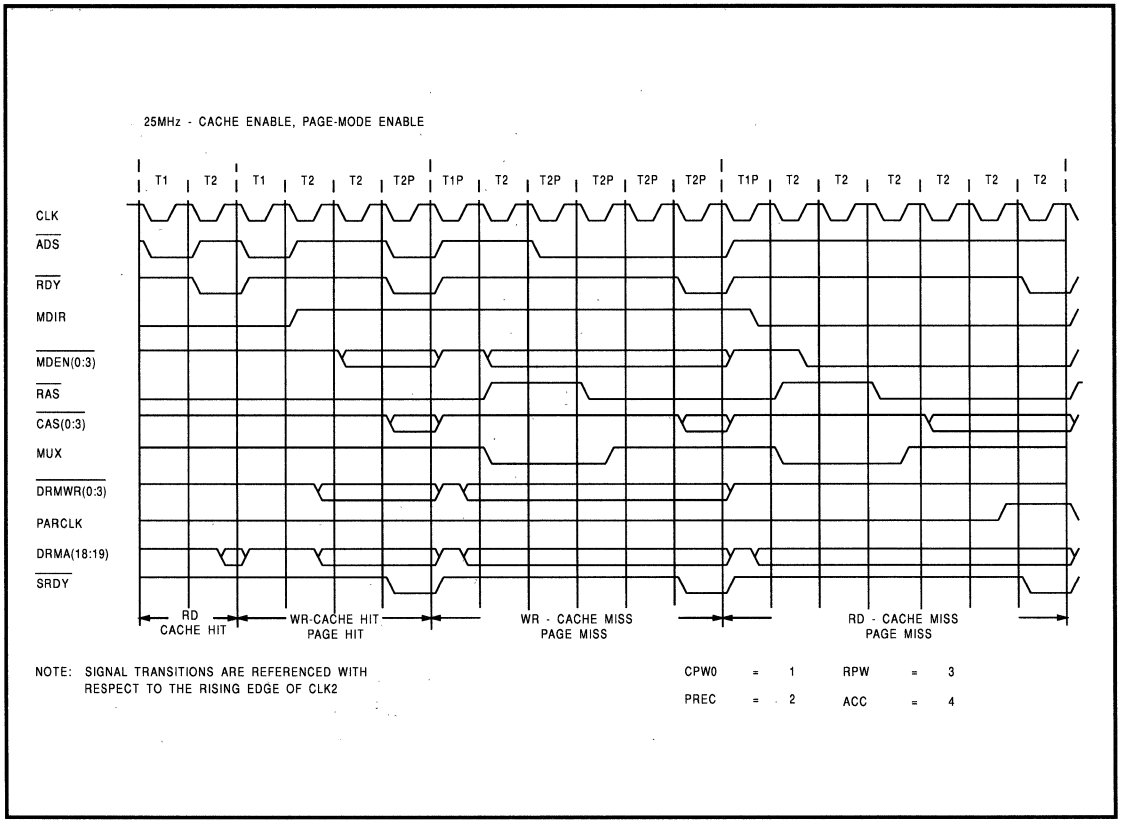

Figure 7. 80386/80486/DMA 25 MHz DRAM Access

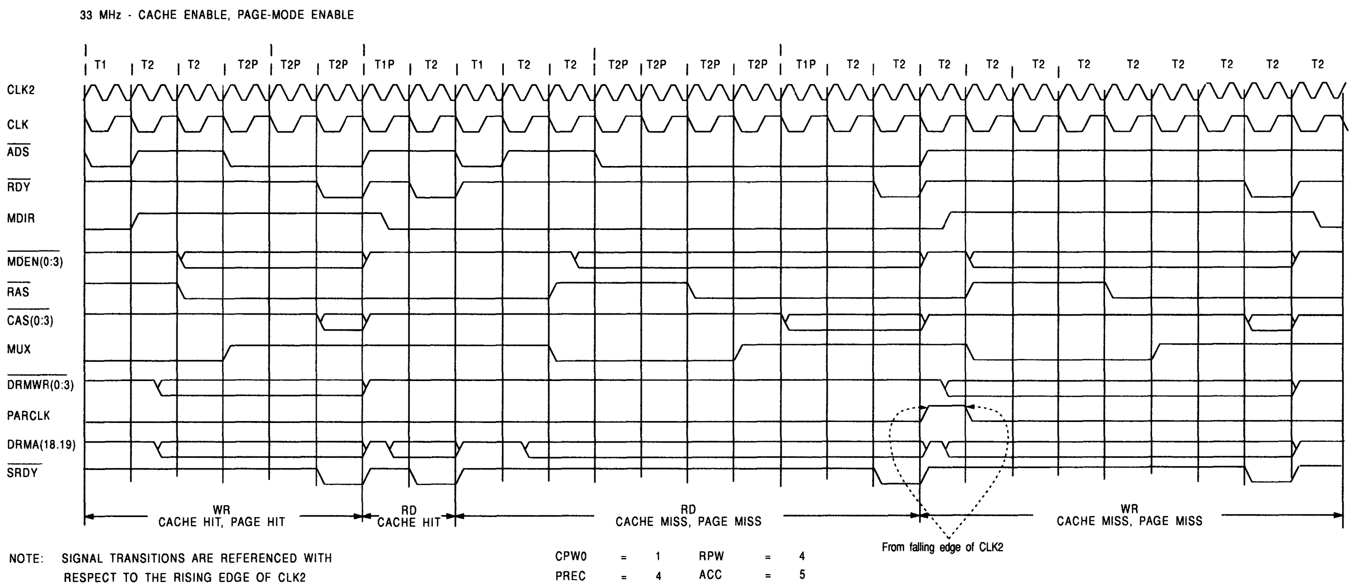

Figure 8. 80386/80486/DMA 33 MHz DRAM Access

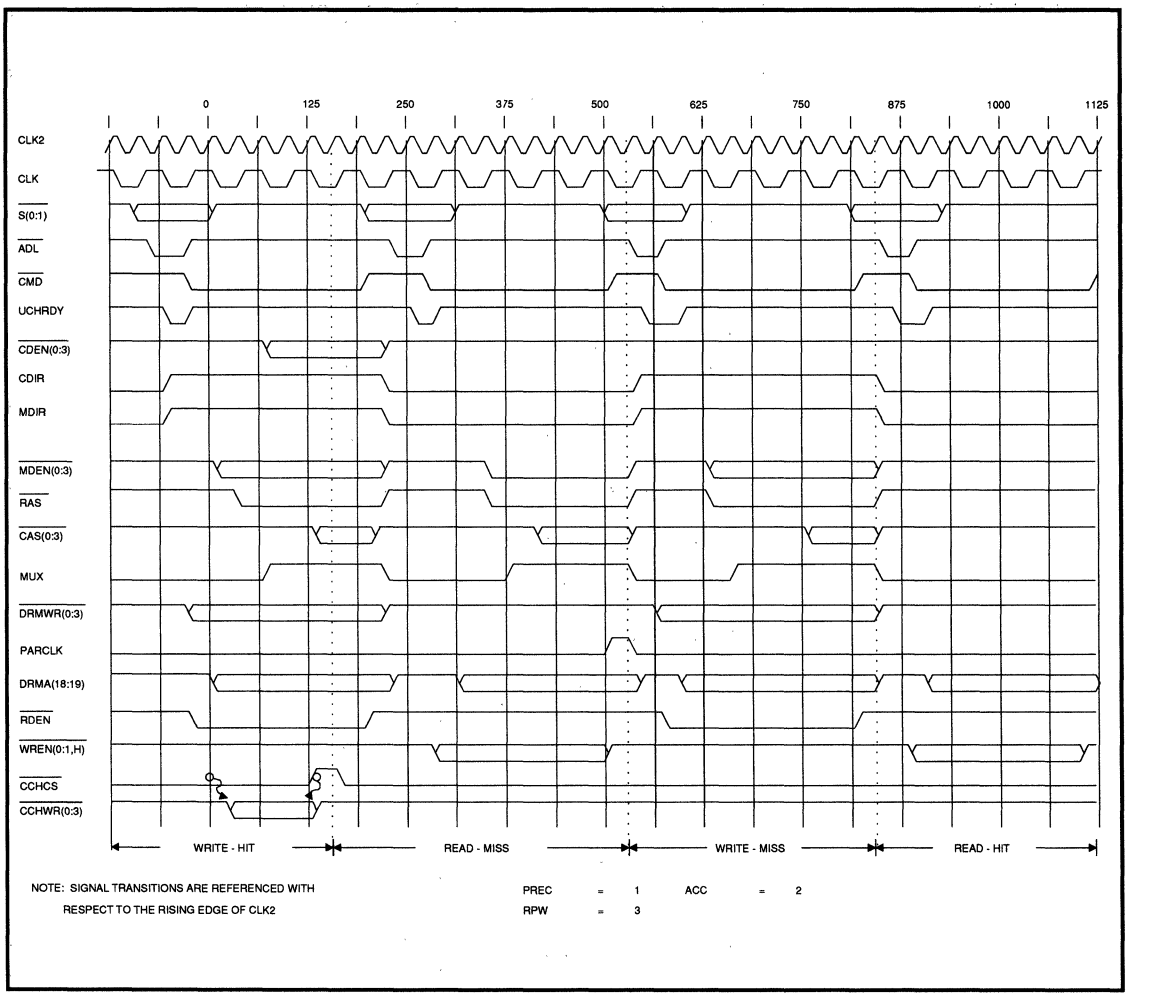

Figure 9. 16 MHz Synchronous Extended Master Cycle

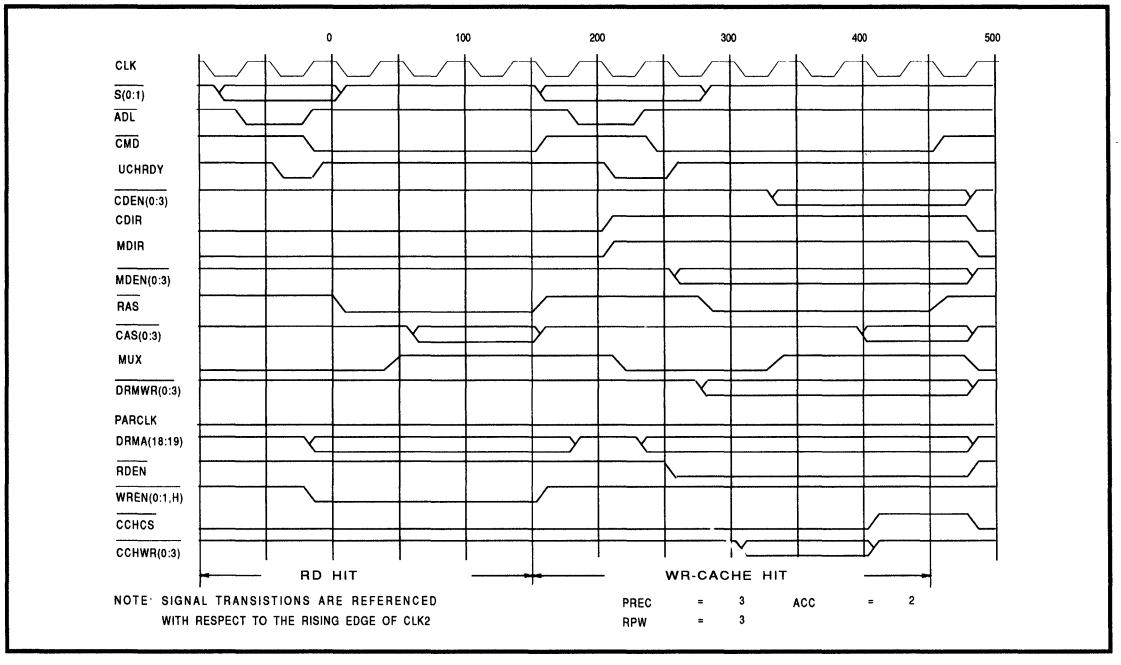

Figure 10. 20 MHz Sysnchronous Extended Master Cycle

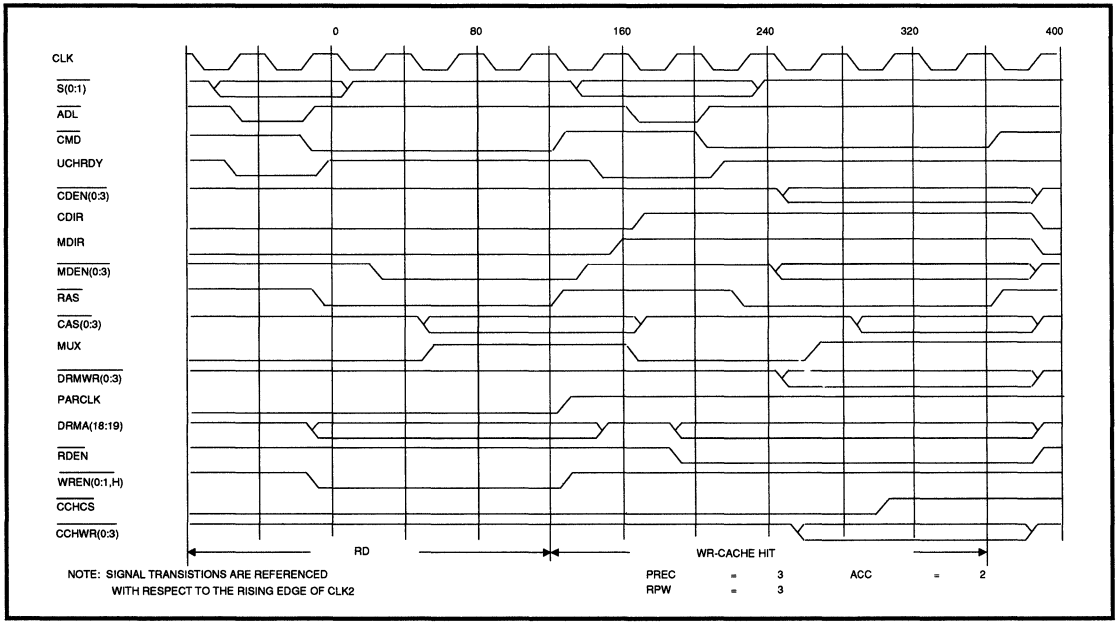

Figure 11. 25 MHz Synchronous Extended Master Cycle

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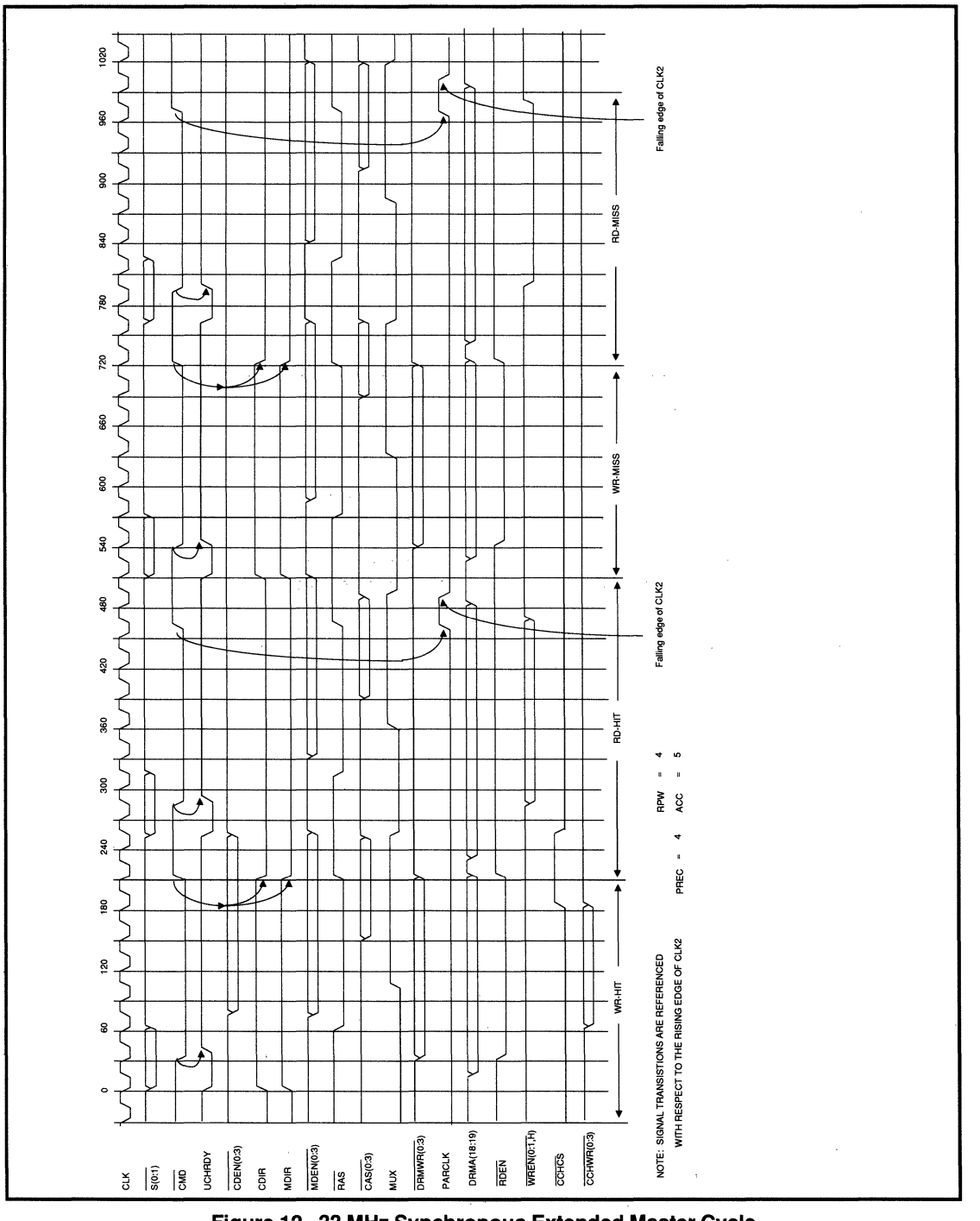

Figure 12. 33 MHz Synchronous Extended Master Cycle

3.0 DRAM CONTROLLER

3.1 MEMORY ORGANIZATION

The WD6030 supports up to four banks of DRAMs, each consisting of 36 bits, with each byte having an associated parity bit. The total memory capacity on the system board is dependent on the type of memory used and the number of banks populated, and could range from 1 MB to 64 MB. Table 3 lists the memory size options that are available.

DRAM TYPE	MEMORY CAPACITY
256K x 1	1 MB x (Number of Banks)
1M x 1	4 MB x (Number of Banks)
4M x 1	16 MB x (Number of Banks)

Table 3. Memory Size Options

The Model 80-071 provides two banks, each with 1 MB of memory. The Model 80-111 has two banks of 2 MB each. The WD6030 default setting at power-up is compatible with the Model 80-071 and Model 80-111: two 1 MB memory banks. The Extended Setup Facility feature can be used to enable more memory on the board.
Each of the banks can be enabled or disabled by programming the Memory Configuration Register. In addition, banks can be swapped, in order to map around defective memory banks.

The WD6030 permits DRAMs of different sizes to be used in the four banks. However, all the DRAMs within a bank should be of the same size. For example, if Bank 0 were composed of 1M x 1 DRAMs, Bank 1 of 256K x 1 DRAMs, and Banks 2 and 3 were unpopulated, this would be a valid use of different-sized DRAMs. Certain restrictions that apply to mixing DRAM sizes should be noted carefully:

- The WD6030 does not support Page Mode operation when DRAMs of different sizes are used in different banks; therefore, in such cases, the DRAMs must be set in Forced Row Misses Mode through the Memory Configuration register. This will result in degraded performance when compared to Page Mode operation for the DRAMs.
- When using a mixture of DRAM sizes, always place the larger-sized DRAMs in the lower banks, or the system will not function. A system populating three banks with 4M x 1, 1M x 1, and 256K x 1 DRAMs should organize them such that Bank 0 consists of 4M x 1, Bank 1 of 1M x 1, and Bank 2 of 256K x 1 DRAMs, with Bank 3 unpopulated.
- When DRAMs of different sizes are used together and the Split RAM is placed in the memory map, the BIOS must ensure that the split RAM starting address is located at an address that is a multiple of the largest DRAMs. Thus, for 4M x 1 DRAMs, it should be located at a 16 Mbyte boundary, for 1M x 1 DRAMs at a 4 Mbyte boundary, for 256K x 1 DRAMs on a 1 Mbyte boundary. See Section 2.1.2.4 for further information.

When the DRAMs are used in Page Mode, the following address assignments should be used for the external multiplexers. REF refers to the addresses for Refresh Cycles. The DA bus is the address bus for the physical DRAM. RAS, CAS, and REF are from the MA or Latched Memory Addresses Bus.

When DRAMs of different sizes are used in the banks, the following address assignments are recommended for use with the external multiplexers. Other address assignments may be used; however, care should be taken to ensure that the addressing for the smaller DRAMs is a subset of the addressing for the larger DRAMs, so that the DRAMs are addressed correctly even though different sizes are used in different banks.

The DA bus is the address bus for the physical DRAMs. The address bits for RAS, CAS, and REF are from the MA bus. REF refers to the addresses for Refresh cycles.

256K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	8	10	11	9	
RAS	20	21	13	14	15	16	17	18	19	12	
REF	2	3	4	5	6	7	8	0	1	X	
4M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	8	9	10	11	12
RAS	20	21	13	14	15	16	17	18	19	22	23
REF	2	3	4	5	6	7	8	9	0	1	X

Table 4. Page Mode DRAM Address Assignments

256 K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	9	10	8	20	
RAS	11	12	13	14	15	16	17	18	19	21	
REF	2	3	4	5	6	7	0	1	8	X	
4 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	9	10	8	20	22
RAS	11	12	13	14	15	16	17	18	19	21	23
REF	2	3	4	5	6	7	0	1	8	9	X

Table 5. Addresses For Different Sized DRAMs

3.1.1 Memory Maps

The first 640K of memory is used for system RAM. Additional banks of RAM are mapped in contiguous blocks, starting at 1 MB. The 256/384K of extra RAM from the first 1 MB is the Split RAM, and is remapped to the top of the last block of memory on the system after the BIOS has determined the total memory size.

Tables 6 through 13 provide memory maps for a typical system. In these tables, 'A' represents the amount, in Mbytes, of system board memory installed and enabled, starting at 00000000H; 'B' represents the amount, in Mbytes, of memory available on the Channel, starting at or above 000100000H.

ENSPLIT = 1 **SIX40 = 1** **ROMEN = 1** **Split Address = Disabled**	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 6. Memory Map 1

ENSPLIT = 1 **SIX40 = 0** **ROMEN = 1** **Split Address = Disabled**	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 7. Memory Map 2

ENSPLIT = 0 SIX40 = 1 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 8. Memory Map 3

ENSPLIT = 0 SIX40 = 0 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 9. Memory Map 4

ENSPLIT = 1 SIX40 = 1 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 10. Memory Map 5

ENSPLIT = 1 SIX40 = 0 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 11. Memory Map 6

ENSPLIT = 0 SIX40 = 1 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 12. Memory Map 7

ENSPLIT = 0 SIX40 = 0 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 13. Memory Map 8

3.1.2 MEMORY CONFIGURATION

The tables in this section describe the format of the ESF and I/O registers that are used to configure memory on the system board. Note that the registers on the WD6030 can only be accessed by the CPU. In this description of the registers that can be written to, bits marked RESERVED should always be written with zeros; this will ensure compatibility with future Western Digital products.

3.1.2.1 Memory Control Register 0103H (W)

The Memory Control Register is implemented in the WD6000. At power-on, a refresh rate compatible with that of the Model 80, 0.8 µs refreshes, is selected, but the BIOS later changes this to 15.1 µs.

Bit 0	Reserved
Bit 1	$\overline{\text{FREF}}$ Fast Refresh 0 = Refresh of 0.8 µs 1 = Refresh of 15.1 µs
Bits 2-7	Reserved
(Power-on Default = 00000000)	

Table 14. Memory Control Register

3.1.2.2 Memory Card Definition Register 0103H (R)

In the Western Digital chip set, this register is implemented in the WD6000. The power-on default, 256K x 1 DRAMs, is compatible with both the 80-071 and the 80-111.

The IBM Memory Card Definition register is implemented on the Model 80 to detect the presence of two memory modules on the system board.

This register treats memory on the system board as being installed in two connectors. The Model 80-071 has connectors with 1 MB each; the Model 80-111 connectors can have up to 2 MB. Bits T1 and R1 are the encodings for Connector 1, and Bits T2 and R2 are the encodings for Connector 2. Some bits that were reserved on the 80-071 have been coded on the 80-111, but are compatible with the 80-071.

There are certain differences between the Western Digital and IBM implementations of this register. The Western Digital Memory Card Definition register does not support the detection of memory connectors, so it always indicates 11110000. Further, it views the system board memory sequentially in four banks of 1 MB, 4 MB, or 16 MB each. However, to maintain compatibility with the Model 80, at power-up the 256K x 1 DRAMs are mapped to correspond to the IBM connector mappings. Table 16 shows the mapping used in the Model 80 Compatibility Mode (256K x 1 DRAMs).

Bits 1, 0	R1, T1 00 - 1 MB RAM in Connector 1 10 - 2 MB RAM in Connector 1 X1 - No RAM (Should be at least 1 MB)
Bits 3, 2	R2, T2 00 - 1 MB RAM in Connector 2 10 - 2 MB RAM in Connector 2 X1 - No RAM
Bits 4-7	1 = Reserved
(Power-on Default = 11110000)	

Table 15. Memory Card Definition Register

W D-Implementation	IBM Model 80 Implementation
Bank 0	Lower 1 MB of Connector 1
Bank 2	Upper 1 MB of Connector 1
Bank 1	Lower 1 MB of Connector 2

Table 16. Model 80 Compatibility Mode

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3.1.2.3 Memory Encoding Register 1 00E1H And Shadow RAM (R/W)

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this register on the WD6030 with all the bits being read/write. The register is compatible with the 80-111. Bit 0, ENPLRPCH, is duplicated in the WD6010, where it is a write-only bit used to control the ENPCHK signal. Table 17 shows the bit assignment for this register.

This register implements the Shadow RAM function and controls the copying of ROM to RAM, and the subsequent execution out of RAM.

When ROMEN is one, all read accesses are directed to the ROM, and all write accesses are directed towards the RAM. When it is zero, all read accesses are directed to the RAM, and write accesses are directed to the Channel, where they are ignored. Physical RAM locations E0000H-FFFFFH are always reserved for this purpose.

To use the Shadow RAM, execute the following steps:

1. Set ROMEN to one.
2. Read Locations E0000 - FFFFFH, and write to the same locations. This copies the ROM code to the RAM.
3. Set ROMEN to zero. The code will now execute out of RAM.

Bit 0	ENPLRPCH 0 - Enable Parity Checking of DRAM 1 - DisableParityCheckingof DRAM
Bit 1	ROMEN 0 - ROM Address Space (E0000-FFFFFH) in DRAM 1 - ROM Address Space in ROM
Bit 2	SIX40 0 - First Meg Split at 640K 1 - First Meg Split at 512K
Bit 3	ENSPLIT 0 -Split Memory Mapped by Split Address Register 1 - Split Memory Disabled
Bits 4-5	EN01, EN02 00 - 2 MB Enabled in Connector 1 10 - First 1 MB Disabled in Connector 1 01 - 1 MB Enabled in Connector 1 11 - Invalid (Memory Disabled in Connector 1)
Bits 6-7	Reserved
(Power-on Default = 11101011)	

Table 17. Memory Encoding Register 1

NOTE
Do not perform any ESF operations while these three steps are being executed, as the ESF register may be corrupted.

Table 18 details different memory configurations generated under the combinations of ENSPLIT, SIX40 and ROMEN.

ENSPLIT	SIX40	ROMEN	CONFIGURATION
0	0	0	ROM Disabled. 256 KB at Split Address
0	0	1	ROM Enabled. 256 KB at Split Address
0	1	0	ROM Disabled. 384 KB at Split Address
0	1	1	ROM Enabled. 384 KB at Split Address

Table 18. ENSPLIT, SIX40, and ROMEN Memory Configurations

3.1.2.4Memory Encoding Register 2 00E0H (R/W)

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this 80-111 compatible register on the WD6030. Bits 0 - 3 of this register define the starting address for the Split Memory and should not be set to zero unless ENSPLIT is one. The Split Address can be used in conjunction with the Split Address Extension Register to map the Split Memory anywhere in the 4 Gigabyte memory space. The only restriction being that the split memory should always be remapped at an address that is a multiple of the largest bank size, for example, with 1M x 1 DRAMs, it should be remapped at a 4 MByte boundary. Table 19 contains the bit assignments for this register.

Bit 0	SPA20 Split Address 20
Bit 1	SPA21 Split Address 21
Bit 2	SPA22 Split Address 22
Bit 3	SPA23 Split Address 23
Bits 4-5	$\overline{EN11}$, $\overline{EN12}$ 00 - 2 MB Enabled in Connector 2 10 - First 1 MB Disabled in Connector 2 01 - 1 MB Enabled in Connector 2 11 - Invalid (Memory Disabled in Connector 2)
Bits 6-7	1 - Reserved
(Power-on Default = 11100010)	

Table 19. Memory Encoding Register 2

The Western Digital implementation of the memory encoding registers differs from the IBM implementation. Bits 4 and 5 of these registers ($\overline{EN12}$, $\overline{EN11}$, $\overline{EN01}$, $\overline{EN02}$) are only applicable when all the banks are populated with 256K x 1 DRAMs, the IBM-compatible power-on default. When other DRAMs are used, the encodings in Table 20 are used. In this table, the "x" in $\overline{ENx2}$ and $\overline{ENx1}$ indicates either a zero or a one.

REGISTER	$\overline{ENx2}$	$\overline{ENx1}$	FUNCTION
00E1	0	0	Bank 0 Enabled
	1	1	Bank 0 Disabled
	0	1	Reserved
	1	0	Reserved
00E0	0	0	Bank 1 Enabled
	1	1	Bank 1 Disabled
	0	1	Reserved
	1	0	Reserved

Table 20. DRAM Encodings

3.1.2.5 Split Address Extension Register ESF:0183H (R/W)

This read/write register is a Western Digital enhancements and is accessed through the Extended Setup Facility. It is used in combination with the Split Address Register to relocate the Split Address at any 1 MByte boundary in the 4 Gigabyte memory address space of the 80386/80486. Most systems will place the split address above the Channel adapter memory in the memory map. Table 21 contains the bit assignment for this register.

Bit 0	- Split Address Bit 24
Bit 1	- Split Address Bit 25
Bit 2	- Split Address Bit 26
Bit 3	- Split Address Bit 27
Bit 4	- Split Address Bit 28
Bit 5	- Split Address Bit 29
Bit 6	- Split Address Bit 30
Bit 7	- Split Address Bit 31
(Power-on Default = 00000000)	

Table 21. Split Address Extension Register

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3.1.2.6 Bank Enable And Version Number Register ESF:0182H (R/W)

This read/write register is a Western Digital enhancement, and does not exist on the Model 80. It disables or enables Memory Banks 2 and 3 and provides the version number of the WD6030 device. Table 22 provides the bit assignment for this register.

Bits 0, 1	$\overline{EN22}$, $\overline{EN21}$ 00 - Enables Bank 2 11 - Disables Bank 2 10 - Reserved 01 - Reserved
Bits 2, 3	$\overline{EN32}$, $\overline{EN31}$ 00 - Enables Bank 3 11 - Disables Bank 3 01 - Reserved 10 - Reserved
Bits 4-7	WD6030 Version Number
(Power-on Default = xxxx1111) The value of 'x' is dependent upon the version number of the WD6030.	

Table 22. Bank Enable And Version Number Register

3.1.2.7 Memory Size Register ESF:0181H (R/W)

This read/write register is a Western Digital enhancement that does not exist on the Model 80. It indicates the type of DRAM chips being used in the memory banks, information that is used internally to implement the memory maps. The software must initialize these bits appropriately, as outlined in Section 3.1.3. Table 23 shows the bit assignment. All the bits are read/write.

Certain points must be kept in mind when using this register.

- When the system integrator uses different-sized DRAMs in the memory banks, the software programming and the hardware must ensure that the larger DRAMs are always placed in the lower banks and the smaller DRAMs placed in the higher banks.
- To get the best performance from the system, Page Mode DRAMs should be used in Page Mode. This mode requires the system to have DRAMs of the same size in all the banks.

Bits 0, 1	- MSIZ00, MSIZ01 Memory Size in Bank 0 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 2, 3	- MSIZ10, MSIZ11 Memory Size in Bank 1 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 4, 5	- MSIZ20, MSIZ21 Memory Size in Bank 2 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 6, 7	- MSIZ30, MSIZ31 Memory Size in Bank 3 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
(Power-on Default = 00000000)	

Table 23. Memory Size Register

3.1.2.8 Memory Window Bank 0 Register ESF:0184H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 0 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 0 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space.

To program any of the Memory Window registers correctly, the software must make sure that the address re-mapping does not cause any address conflicts. This means that it has to account for the size of the DRAMs installed in the banks and must program the register so that Bank 0 has unique addresses.

Table 24 details the bit assignment for this register. Note that only the combination of bits indicated by the + in the table needs to be programmed for the different DRAM sizes. This applies to the other memory window registers as well, described in Sections 3.1.2.9 - 3.1.2.11.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000000 (256K x 1 DRAMs)				

Table 24. Memory Window Bank 0 Register

3.1.2.9 Memory Window Bank 1 Register ESF:0185H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 1 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 1 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space. Table 25 details the bit assignment for this register.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000001 (256K x 1 DRAMs)				

Table 25. Memory Window Bank 1 Register

2.1.2.10 Memory Window Bank 2 Register ESF:0186H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 2 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 2 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space.

Table 26 details the bit assignment for this register.

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		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000010 (256K x 1 DRAMs)				

Table 26. Memory Window Bank 2 Register

3.1.2.11 Memory Window Bank 3 Register ESF:0187H (R/W)

This read/write register is a Western Digital enhancement, accessed through the ESF. It relocates Memory Bank 3 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 3 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space.

While re-mapping banks, the software should ensure that no holes are created in memory and that the system board memory always starts at Address 00000000H. Further, all system board memory should be placed contiguously in the memory map. The only exception is the split addresses, which are placed contiguously above the Channel RAM. Table 27 details the bit assignment for this register.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	Reserved			
Power-on Default = 00000011 (256K x 1 DRAMs)				

Table 27. Memory Window Bank 3 Register

3.1.2.12 Memory Configuration Register ESF:0180H (R/W)

This read/write register is a Western Digital ESF enhancement. It controls the enabling and disabling of the cache and Page Mode for the DRAMs. Table 28 details the bit assignment for this register.

At power-on, the software must read the Memory Size Register and ensure that all the banks have DRAMs of the same size before setting Bit 4, FRMISS, to zero. When the cache is set for Forced Misses at power-up to ensure proper cache initialization, read data for the Memory Read cycle comes from the DRAM and writes go to the DRAM. The TagRAM and cache are updated on each Read Miss. When the DRAMs are set in Forced Row Misses, the DRAMs are not operated in Page Mode, and a RAS/CAS precharge is performed for every DRAM cycle. This mode should be used if there are no Static Column or Page Mode DRAMs being used in the system.

Bit 0	FMISS Cache Forced Miss 0 - Cache Operating in Normal Mode 1 - Cache Operating in Forced Misses Mode
Bits 1-3	Reserved
Bit 4	FRMISS Forced Row Miss 0 - DRAMs Operating in Page Mode 1 - DRAMs Operating in Normal RAS/CAS Mode
Bits 5-6	Reserved
Bit 7	RASTMOUT RAS Time-out 0 - 10 microseconds RAS Time-out Disabled 1 - 10 microseconds RAS Time-out Enabled
Power-on Default = 00010001	

Table 28. Memory Configuration Register

When Bit 7, RASTMOUT, is set, it enables an internal timer which monitors the length of the NRAS pulse and precharges it every 10 ms. The bit must be set for DRAMs requiring the maximum pulse width on NRAS to be less than or equal to 10 ms. Do not, however, enable Bit 7 for DRAMs that do not require it, as this will degrade memory performance.

The approximate RAS time-out periods at different operating frequencies is tabulated below.

FREQ.	APPROXIMATE RAS TIME-OUT PERIOD
16 MHz	9 µs
20 MHz	9.6 µs
25 MHz	8.96 µs
33 MHz	8.64 µs

Western Digital allows memory performance to be fine-tuned to the CPU frequency through a series of Memory Timing Registers which allow the critical DRAM parameters in the memory cycle to be directly programmed. This enables DRAMs with different parameters, including different access times, to be used. The memory wait states obtained are a result of this programming and can not be explicitly programmed. The system's primary (CLK2) and phase clock (CLK) signals provide the time granularity for programming. Refer to Section 3.3, Timing Configuration, for further details on programming.

3.1.2.13CAS Pulse Width Register ESF:0188H (R/W)

This read/write register is a Western Digital ESF enhancement; Table 29 describes its format.

Bit 0 programs the CAS pulse width for DRAM read cycles when the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles cannot be programmed. The programming of this bit determines the number of wait states to be provided by the WD6030 wait state generator.

When a Channel master performs a read to system board memory, Bit 1 extends the cycle if the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles can not be programmed. Bit 1 (CPW1) also controls the reassertion of CHRDY, as shown in Table 29. Note that CLK2 in this table denotes a frequency twice that of the processor. Bit 2 allows timing between RAS to MUX and MUX to CAS to be controlled by sofware. For 33 MHz systems this bit can be programmed to one, and the DRAM controller in the WD6030 will change MUX after two CLK2s and CAS will drop two CLK2s after MUX. Bit 3 CPW allows programming of UCHRDY signal. For asynchronous extended cycles during Master accesses, the UCHRDY is removed as CMD falling edge. This feature improves system performance for Master accesses for 25 and 33 MHz systems.

Bit 0	CPW0 CAS Pulse Width from 386/486/DMA cycles 0 - CAS Pulse Width = 2CLK (1 WS with Page Hit) 1 - CAS Pulse Width = 3CLK (2 WS with Page Hit)
Bit 1	CPW1 CHRDY Re-assertion for Channel Master cycle 0 - UCHRDY released after leading edge of CAS 1 - UCHRDY released after leading edge of CLK2
Bit 2	RAS to MUX to CAS 0 - 1 CLK2 (default) 1 - 2 CLK2
Bit 3	0 - Sync extended Master cycle 1 - Async Master cycle
Bits 4-7	Reserved
(Power-on Default = 00000111)	

Table 29. CAS Pulse Width Register

3.1.2.14 RAS Precharge Delay Register ESF:0189H (R/W)

This read/write register is a Western Digital ESF enhancement, which permits the RAS precharge time to be programmed in CLK2 (twice the processor frequency) increments to suit the type of DRAM being used. The range extends from a minimum delay of 2 CLK2s (62.5 ns at 16 MHz) up to a maximum of 6 CLK2s (90 ns at 33 MHz).

Bits 2-0	PREC (2:0) RAS Precharge 000 - 2 CLK2s 001 - 3 CLK2s 010 - 4 CLK2s 011 - 5 CLK2s 100 - 6 CLK2s 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000100)	

Table 30. RAS Precharge Delay Register

3.1.2.15 RAS Pulse Width Register ESF:018AH (R/W)

This read/write register is a Western Digital ESF enhancement, which permits the RAS pulse width to be programmed and tailored to the DRAM. The pulse width obtained in actual operation is equal to or greater than the programmed value. It can range from 3 CLK2s (93.75 ns at 16 MHz) to 7 CLK2s (105 ns at 33 MHz).

Bits 2:0	RPW (2:0) RAS Pulse Width 000 - 3CLK2 001 - 4CLK2 010 - 5CLK2 011 - 6CLK2 100 - 7CLK2 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000100)	

Table 31. RAS Pulse Width Register

3.1.2.16 RAS Access Time Register ESF:018BH (R/W)

This read/write register is a Western Digital ESF enhancement; it programs the RAS pulse width to meet the DRAM RAS access times. The pulse widths can range from 4 CLK2s (125 ns at 16 MHz) up to a maximum of 9 CLK2s or (135 ns at 33 MHz). Actual pulse widths will be equal to or greater than the value programmed.

For Memory Configuration Registers ESF:188, ESF:189, ESF:18A, and ESF 18B (Sections 3.1.2.13 - 3.1.2.16), the software must program these registers appropriately before accessing them if the DRAMs being used have parameters that differ from the default values.

Bits 2:0	ACC (2:0) RAS Pulse Width due to access time 000 - 4 CLK2s 001 - 5 CLK2s 010 - 6 CLK2s 011 - 7 CLK2s 100 - 8 CLK2s 101 - 9 CLK2s 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000101)	

Table 32. RAS Access Time Register

3.1.2.17 System Configuration Register ESF:018FH (R/W)

This read/write register is a Western Digital ESF enhancement that provides configuration data for the system. Bit 0 is used to detect the presence/absence of an optional numeric coprocessor device, Intel's 80387. If it is present, the I/O bus cycles with Address Bit 31 (PA31) set are directed towards the 80387, and the 80387 generates a Ready signal. If the coprocessor is absent, the Ready signal for those bus cycles is generated by the WD6030.

Bit 1 enables/disables the optional Weitek 3167 or compatible coprocessor. When Bit 1 is enabled, memory accesses in the range C0000000 - C000FFFFH are directed to the Weitek coprocessor and the coprocessor generates the Ready signal. When it is disabled, the WD6030 generates the Ready signal for those addresses.

Bits 7 and 6 latch the state of the frequency configuration bits. The software uses this information to determine the speed at which the system is operating.

When the system is powered on, the state of the UCHMSTR, A20GTX and SWPDIR signals are latched into WD6030 internal signals F1, F0 and COPRES, respectively.

Bit 0	80387 Present/Absent (R/O) 0 - 80387 Present 1 - 80387 Absent
Bit 1	WTKEN Weitek 1167 Enable/Disable (R/W) 0 - Module Disabled 1 - Module Enabled
Bits 2-5	Reserved
Bits 6-7	UCHMSTR, A20GTX (R/O) 00 - 16 MHz 01 - 20 MHz 11 - 25 MHz 10 - 33 MHz
(Power-on Default = xx00000x)	

Table 33. System Configuration Register

The value of "x" in the power-on default above depends on the configuration of the system, and may vary.

3.1.3 Operating Modes

The DRAM controller is optimized for Page Mode DRAMs. They allow one wait state operation on a cache miss if the access was to the same DRAM row, thus keeping the cache miss overhead low.

The first cache miss takes two wait states, but subsequent misses only take one wait state, because of the operation of the CPU and the WD6010 in Pipelined Mode.

Page Mode and ordinary RAS/CAS DRAMs are also supported. Note that the Static Column Mode should be turned off in the DRAM controller when using RAS/CAS DRAMs, or degraded performance could result.

The system requires 100 ns DRAMs. Faster DRAMs can be used, but all accesses to the DRAMs will still take at least one wait state because of the use of the cache.

3.2 MEMORY INITIALIZATION

The system power-on default configuration follows:

- 1 MByte per bank
- Banks 0 and 1 enabled; all other banks disabled
- Split Address at 000100000H
- ROM enabled through Memory Encoding Register 1
- Split Memory enabled through Memory Encoding Register 1
- 640 enabled through Memory Encoding Register 1
- Page Mode disabled
- Cache disabled
- 80386 in Protected Mode at power-on

The following steps describe one possible way to initialize the system board DRAM in a system using a mixture of DRAM sizes.

1. Determine the first bank in the system, which contains Addresses 00000000 - 0007FFFFH.

   To determine the bank, enable Bank n (0, 1, 2 or 3) and disable the others. Execute a RAM test on the first 512K. If the test passes, Bank n is the first bank. If it fails, disable that bank, and identify it as a failed bank. Repeat the test with the next bank, until you find a bank that passes the test. If all the banks fail the test, the system is non-functional.

2. Determine the size of the DRAMs in the first bank that passes the RAM test.

> **NOTE**
> If any portion of a bank is found to be bad, that bank can still be used by setting the memory size bits to the next lower value. For example, if MBytes 8-16 are found to be bad with 4M x 1 DRAMs, set the memory size to 1M x 1, and use that bank as a 1M x 1 bank.

Enable Bank n (0, 1, 2, or 3), and disable the others. Set the Memory Window Bank n register to 0000H, and set the memory size bits for the bank to 256K x 1.

Do a RAM test on the first MByte.
FAIL - Bank is bad; disable it
PASS ↓
Set the memory size bits to 1M x 1
FAIL - Bank is bad; disable it
PASS ↓
Do a RAM test on Mbytes 0-4
FAIL - DRAMs in this bank are 4M x 1
PASS ↓
Set the memory size bits to 4M x 1
Do a RAM test on Mbytes 0 - 16
FAIL - DRAMs are 1M x 1
PASS - Leave the memory size bits at 4M x 1

By the end of Step 2, the Memory Size register and the Bank Enable bits should have been correctly programmed.

3. Set ROMEN = 1, read Locations 000E0000-000FFFFFH and write to the same addresses. This copies the ROM to the physical DRAM. Then set ROMEN = 0. This directs all read accesses to the RAM, which now holds the contents of the ROM, and also write-protects these RAM locations. The shadow RAM is now in operation.

4. Perform the RAM tests described in Step 2 on each of the remaining untested banks to determine their availability and memory size. If any bank is bad or is unpopulated, re-assign the addresses through the Memory Window registers.

At the end of this step, the memory size bits for all the populated banks should be known. The software should now re-assign the addresses for the banks using the Memory Window registers, and avoiding address conflicts. All the addresses should be contiguous, starting at 00000000H.

5. If the banks are found to contain DRAMs of different sizes, during address assignment the software must ensure that the larger DRAMs are always mapped to the lower banks. If the DRAMs are of the same size, Page Mode can be turned ON through the Memory Configuration register after initializing the cache as described in Section 4.3. The cache may also be turned ON at this point, using the same register.

3.3 TIMING CONFIGURATION

The WD6030 supports DRAMs with different timing parameters by reprogramming the Memory Timing Registers. To facilitate programming, the critical RAM parameters in the memory cycle can be directly programmed. These parameters include RAS access time (ESF:018B), RAS pulse width (ESF:018A), RAS precharge (ESF:0189) and CAS pulse width (ESF:0188). Thus, the system can be programmed for the best memory performance at different CPU and memory speeds.

At power-up, the WD6030 defaults to the largest value of each parameter so as to accomodate the slowest RAMs. The Memory Timing Registers must then be re-programmed by the BIOS to extract the best possible performance from the system.

The WD6030 automatically inserts the wait states to satisfy all the programmed parameters. The wait states in the system can not be explicitly programmed.

The minimum time granularity for programming is the primary clock, CLK2: 15 ns with a 66 MHz CLK2 for a system operating at 33 MHz. Note that the system always operates at half the clock speed. The RAS CAS time is always guaranteed to be 2*CLK2.

Table 34 shows the programming for a typical DRAM.

NOTE
This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the DRAMs used in their particular systems.

System Operation 25 MHz CLK2: Frequency= 50 MHz CLK2: Period= 20 ns DRAM: 1M x 1 Fast Page Mode DRAM	
TIMING	DESCRIPTION
tRAC	RAS Access Time = 100 ns RAS Access Time Register 01H. (Programmed for 5 CLK2s)
tRAS	RAS Pulse Width = 100 ns (min) 100,000 ns (max) RAS Pulse Width Register 02H. (Programmed for 5 CLK2s)
tRP	RAS Precharge = 80 ns RAS Precharge Delay Register 02H. (Programmed for 4 CLK2s)
tCAC	Access Time from CAS = 25 ns CAS Pulse Width Register, Bit 0 = 0. Programmed for CAS pulse width of 4 CLK2s = 80 ns, which ensures that a pipelined one-wait state operation to the DRAM can complete. CAS Pulse Width Register, Bit 0 = 1. CHRDY re-asserted from the leading edge of CAS for Master cycles.
tRCD	RAS to CAS Delay Time = 25 ns (min), 75 ns (max) RAS to CAS Delay = 2 CLK2s = 40 ns

Table 34. Typical DRAM Program Parameters

4.0 CACHE CONTROLLER

The cache is organized in sets. Each set contains one or more lines, a line being the basic unit of data transfer between the cache and the DRAM. The cache controller in the WD6030 implements a direct-mapped, write-through cache for the 80386/80486 with a line-size of four bytes, that executes 80386 bus cycles, DMA, and Channel master bus cycles. Each set in an WD6030-based system contains one line.

The cache subsystem delivers high performance by ensuring zero wait state cache read-hits, and a low, one wait state miss overhead. Zero wait state access is achieved on a cache read-hit, and cache misses are supported by the page mode DRAMs which provide fast, one wait state access for a page hit.

4.1 CACHE ORGANIZATION

The WD6030 implements the cache controller on the chip, but the Tag subsystem is implemented externally to ensure more flexibility in design. The cache controller allows the system designer to determine the amount of DRAM to be cached and the size of the cache according to the cost and performance requirements. A typical cache system uses 64 KBytes of cache, caching 16 MB of DRAM.

To build a direct-mapped cache, the processor addresses are organized in the following manner:

$\overline{\text{BE}}$ (0:3)

They select the bytes in the line for transfer. A write-hit causes only the selected bytes to be replaced, but a cache update operation executed after a cache miss will replace the entire line.

PA (2:N)

They form the index for the cache and determine which line is to be transferred to the device requesting the transfer. "N" depends on the size of the implemented cache.

PA (N+1:M)

They form the tag for the cache. These bits are compared to the ones stored in the TagRAM for that particular index. If they match bit-for-bit, the requested data lies in the cache. "M" depends on the size of the DRAM being cached. The table below shows the values when 16 Mbytes of DRAM are cached.

CACHE SIZE	TAG	INDEX
32 Kbytes	PA(15:23)	PA(2:14)
64 Kbytes	PA(16:23)	PA(2:15)
128 Kbytes	PA(17:23)	PA(2:16)
256 Kbytes	PA(18:23)	PA(2:17)

Table 35. Typical Cache Values

4.2 CACHE POLICY

The cache policy used in an WD6030-based system is described in Table 36. Only the local DRAM, that is, the DRAM set by the Memory Window registers, is cached. All other bus cycles, such as I/O cycles or accesses to the Channel, are treated as non-cachable areas and are not cached.

80386/80486 BUS CYCLES		
TYPE	**CACHE HIT**	**OPERATION**
Read	Yes No	Read from cache Read from DRAM, Update cache
Write	Yes No	Write to the cache and DRAM Write to the DRAM only
DMA (WD6010) CYCLE		
TYPE	**CACHE HIT**	**OPERATION**
Read	Yes No	Read from cache Read from DRAM
Write	Yes No	Write to the cache and DRAM Write to the DRAM only
CHANNEL MASTER BUS CYCLES		
TYPE	**CACHE HIT**	**OPERATION**
Read	X	Read from DRAM
Write	Yes No	Write to Cache and DRAM Write to DRAM

Table 36. Cache Operation in Different Bus Cycles

4.3 CACHE INITIALIZATION AND DIAGNOSTICS

At power-up, invalid tags are stored in the TagRAMs. These tags in the tag directory must be correctly initialized before the cache can be used. To initialize the tags, the power-up default for the cache controller is Forced Misses Mode. The software reads the cache size data (e.g. 64 Kbytes for a 64K cache) from the DRAM, and this action updates the cache and tags to their correct values. The cache can then be programmed in Normal Mode and is ready for use.

There are several ways to conduct system-level diagnostics and verify the correct operation of the cache and DRAM in a cache-based system. Examples of software DRAM testing and cache testing follow.

To test the DRAMs, a typical write-read-compare operation can be performed on the data. Before doing this, ensure that the data always comes from the DRAMs, by using the Memory Configuration Register to program the cache to Forced Misses Mode; this directs all read and write accesses to the DRAM. The cache is updated on a read operation, but a write operation does not affect the cache. To prevent the code executing this diagnostic routine from being overwritten in the cache, either make the code ROM-based, or ensure that the area being tested does not overlap the area where the code resides. Then execute the write-read-compare operation:

1. Write a pattern of data.

2. Read it back and compare it.

To test the cache, perform another write-read-compare operation, using the following sequence:

1. Disable the cache by setting it in Forced Misses Mode.

   Write Pattern 1:
   DRAM = Pattern 1, Cache = unknown
   Read Pattern 1:
   DRAM = Pattern 1, Cache = Pattern 1
   Write Pattern 2:
   DRAM = Pattern 2, Cache = Pattern 1

2. Enable the cache by setting it to Normal Mode. Read and compare the results. If it is Pattern 1, the cache is functioning properly. If it shows Pattern 2, it indicates that the Hit/Miss circuitry has failed. Any other pattern indicates that the cache is bad.

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4.4 CACHE TIMING

Table 37 shows the typical speeds for the SRAMs required to build the data cache and the TagRAMs required for zero wait state operation.

NOTE
This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the SRAMs used in their particular systems.

TIMING/FREQUENCY	16 MHz	20 MHz	25 MHz	33 MHz
Processor Address to HIT generation*	57 ns	47 ns	38 ns	20 ns
Data Cache SRAM Access Time (Address to data)	64 ns	45 ns	35 ns	21 ns

*The parameters take into account a 6 ns delay to generate A20 externally.

Table 37. Cache Timing

5.0 CHANNEL CONTROLLER

The Channel Controller in the WD6030 controls the CPU and the DMA accesses to the Micro Channel. Accesses by a Channel master to the system board DRAM are controlled by the DRAM controller in the WD6030. The timing generated by the WD6030 are compatible with the IBM Micro Channel specifications. Figures 24 through 27 illustrates typical accesses to the Channel.

Control is provided for default and extended memory or I/O Channel cycles. 8-bit, 16-bit and 32-bit data can be transferred to the Channel. The CPU always treats a port as being at least sixteen bits wide. Therefore, on an access to an 8-bit port, the WD6030 splits a 16-bit cycle into two cycles and performs any necessary byte swaps. Though the byte-swap is implemented by the WD6022 in Data Buffer Mode, the Channel controller provides the controls for it. It also controls the word swaps, which are necessary when a 16-bit master talks to a 32-bit slave. Figures 26 through 29 illustrates typical byte-swap cycles.

The special timings required by the Channel setup cycles are also implemented by the Channel controller. The Channel Controller also functions as a buffer controller, controlling all data transfers to or from the Channel.

Since the Channel timing remain constant in a system, the WD6030 determines the speed of the processor and optimizes its Channel bus cycles to match Channel specifications. This allows the controller to support the 80386 and 80486 processors at different frequencies: 16, 20, 25, and 33 MHz. The speed of the processor is determined by the state of signals UCHMSTR and A20GTX at power-up. Table 38 supplies a frequency table.

FREQUENCY	UCHMSTR	A20GTX
16 MHz	0	0
20 MHz	0	1
25 MHz	1	1
33 MHz	1	0

Table 38. Frequency Table

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6.0 EXTENDED SETUP FACILITY (ESF)

The Extended Setup Facility (ESF) is a Western Digital enhancement that permits additional functionality to be configured on the board. Based on the concept of "alternate I/O space", it uses memory space that is currently unused on the Model 80 to add more features, or to tailor the board to meet specific needs. The ESF is flexible and can be reprogrammed to other locations if a conflict should arise with future IBM enhancements to the Model 80 design.

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the WD6010 to the WD6000. The ESF is designed to extend the configuration architecture established with POS features. Refer to Figures 13 and 14 for an overview of the ESF function. ESF supports:

- System Configuration Registers
- Memory Map Control Registers
- Additional Physical Serial Port
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include:
  System Identification
  System Version

6.1 ESF ADDRESS MAP

The lower sixty-four bytes (EAR0 = 00H - 3FH) of the ESF are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. Refer to Table 39 for details. All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be zero when addressing only 128 ESF registers. To expand the ESF to Location 32,768, set EAR0 Bit 7 to one and write the second ESF address byte to EAR1.

FUNCTION	ESF ADDRESS	R/W	WD6500 DEVICE
Reserved	0 - 001FH	-	-
Peripheral Configuration	20H	R/W	WD6000
Port A, B Control	21, 24H	R/W	WD6000
Port A, B Address (LSB)	22, 25H	R/W	WD6000
Port A, B Address (MSB)	23, 26H	R/W	WD6000
Reserved	30 - 3FH	-	-
Customer-specified	40 - 7FH	-	-
Memory Configuration	0180H	R/W	WD6030
Memory Size Register	0181H	R/W	WD6030
Bank Enable Register	0182H	R/W	WD6030
Split Address Extension	0183H	R/W	WD6030
Memory Window Bank 0	0184H	R/W	WD6030
Memory Window Bank 1	0185H	R/W	WD6030
Memory Window Bank 2	0186H	R/W	WD6030
Memory Window Bank 3	0187H	R/W	WD6030
CAS Pulse Width	0188H	R/W	WD6030
RAS PreCharge Delay	0189H	R/W	WD6030
RAS Pulse Width	018AH	R/W	WD6030
RAS Access Time	018BH	R/W	WD6030
Enhanced Addressing	018CH	R/W	WD6010
Reserved	018DH	-	-
Reserved	018EH	-	-
System Control Register	018FH	R/W	WD6030

Table 39. ESF Address Map In A WD6500 System Environment

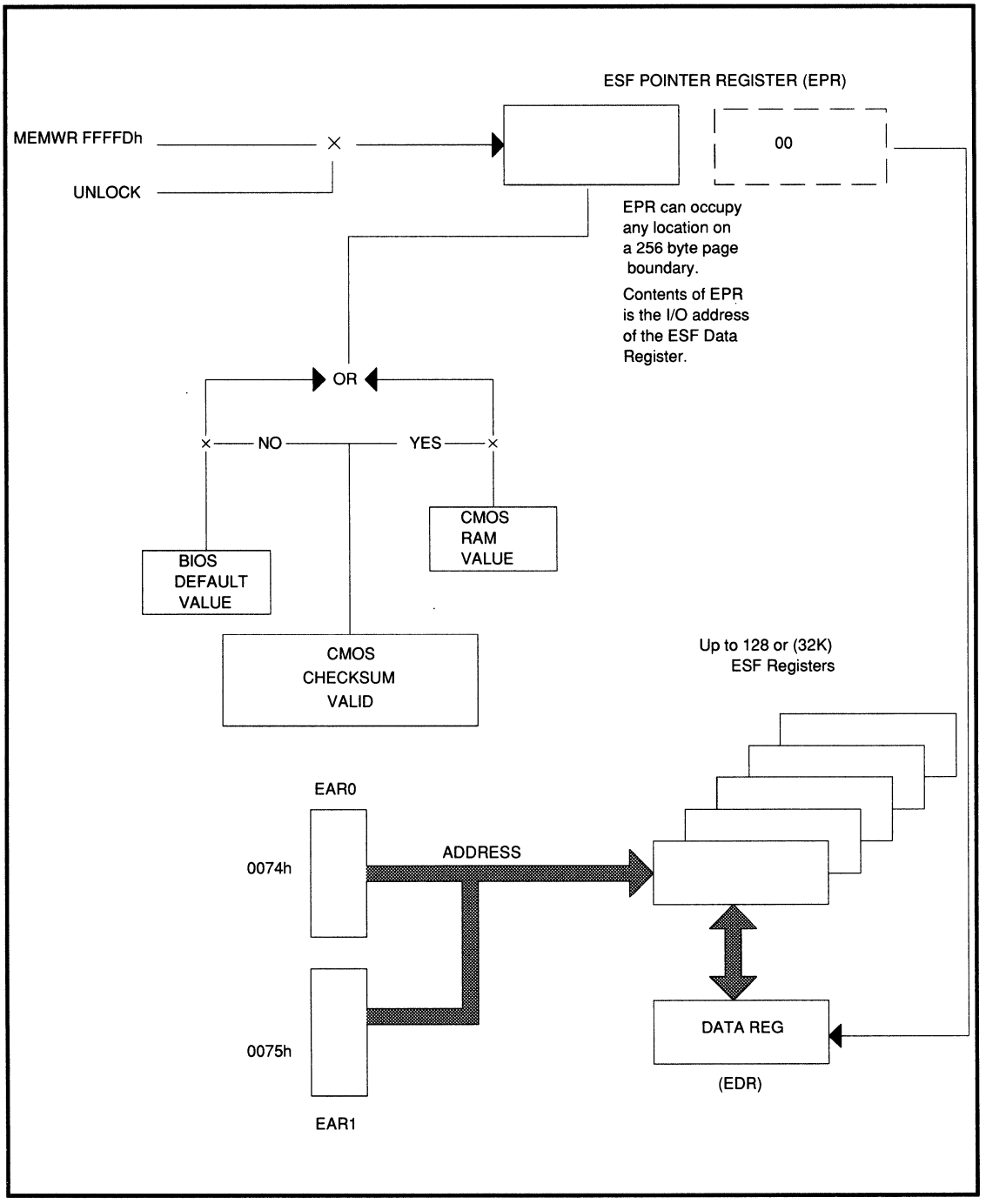

Figure 13. ECR And ESF Block Diagram

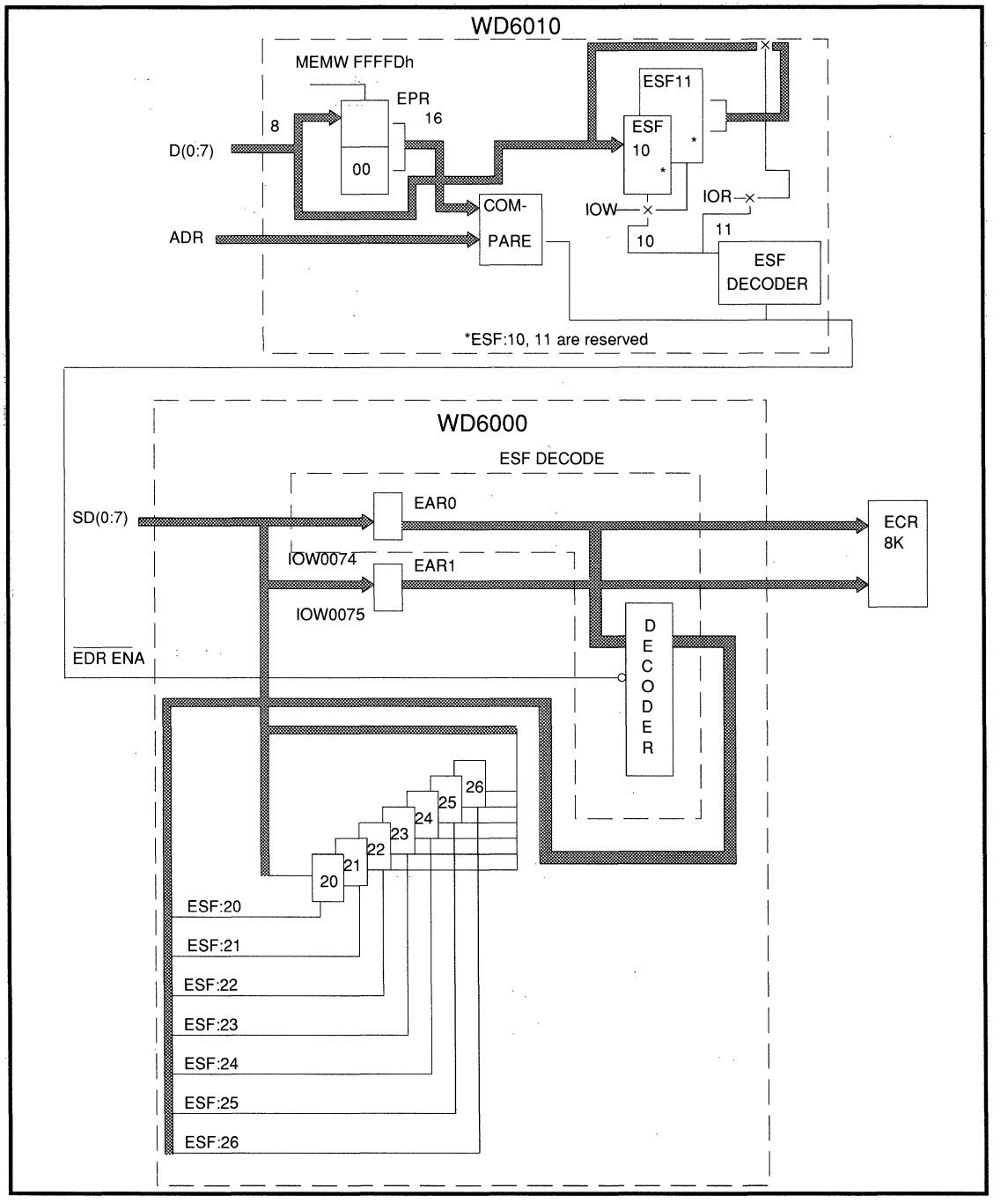

Figure 14. Extended Set-UP Facility Overview

6.2 ESF ACCESS

ESF space consists of 128 locations expandable to 32K, and may be implemented as word-wide or byte-wide, at the discretion of the designer. Table 39 provides an address map of the ESF registers, access to which is accomplished through the Extended Data registers EAR0 and EAR1, and a "real I/O space" window, the Extended Data register (EDR). Registers that are not documented in this table are reserved and should not be used. For a discussion of some ESF registers, see Section 3.1.2.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFDH or FFFF, FFFDH, a PROM. The power-on default location for the EDR is at I/O Address 0700H.

The following procedure is recommended to modify the EPR:

1. Set Port 0700H to 8DH to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4, Refresh Toggle, to synchronize it with the refresh circuitry.

3. To unlock the EPR, read EAR0 at 0074H, normally a write-only address.

4. Write the new value into the EPR at FFFFDH. This locks the EPR once again.

5. Enable NMI if required. Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first. The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space, follow these steps:

1. Write 8DH to Port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H. If Expanded ESF is being used, also write the value to EAR1.

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

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7.0 PERFORMANCE

7.1 MEMORY PERFORMANCE

The performance of a system using a cache depends on several factors, such as the hit rate, the miss overhead, etc. A 64K direct-mapped cache typically produces an 85 - 90% hit rate, with a 30% improvement in performance over a 2 wait state memory design for memory-intensive applications. In DOS environments, the hit rates can exceed 99%. Table 40 shows the performance that can be obtained from the memory subsystem.

NOTE

The performance figures noted above could vary with the software being run.

7.2 TYPICAL CHANNEL ACCESS PERFORMANCE

Table 41 shows typical performance obtained on 80386/80486 or DMA accesses to the Channel. The numbers refer to the cycle times.

Notes

1. For DRAM accesses, the Page Miss performance may vary, depending on the timing parameters of the DRAMs used and the programming in the registers for the CAS pulse width, RAS precharge delay, RAS pulse width and RAS access time.

2. The CAS access time in Page Mode must be equal to or better than 35 ns to achieve the performance shown in Table 41.

3. The numbers in parentheses denote the wait states.

As described above, when operating in Pipelined Mode, the default Page Mode results in one wait state on a cache miss.

CACHE/PAGE MODE ENABLE	16 MHz	20 MHz	25 MHz	33MHz
CACHE HIT	125 ns (0)	100 ns (0)	80 ns (0)	62.5 ns (0)
CACHE MISS AND PAGE HIT, PIPELINED	187.5 (1)	150 ns (1)	120 ns (1)	93.75 ns (1)

Table 40. Typical Performance Of A Memory Subsystem

CHANNEL BUS CYCLE	16 MHz	20 MHz	25 MHz	33 MHz
I/O or Memory without wait*	321.5 ns	300 ns	280 ns	281.25 ns
I/O or Memory with wait*	375+ ns	350+ ns	360+ ns	375 + ns
*The timings shown are for Pipelined Mode. For Non-Pipelined Mode, add an extra wait state.				

Table 41. Channel Bus Cycle

7.3 PERFORMANCE FOR OTHER BUS CYCLES

The wait state controller within the WD6030 generates the required number of wait states on an 80386/80486 or DMA bus cycle, by delaying the SRDY signal until the cycle is completed. It does not, however, respond to accesses to the 80387, as the 80387 generates its own signal RDY0 (READY0), nor to memory accesses that result in a cache hit.

The wait states generated by the controller obey the following rules:

- Local memory accesses that do not generate cache hits result in wait states as shown in Table 42.
- Accesses to the local I/O, including the registers on the WD6010 and the WD6030, and the ESF registers, but excluding Port 00F1H, require an access time of 100 ns, which results in the wait states shown in Table 42.
- Channel cycles, including Interrupt Acknowledge cycles, are determined by the assertion of CHRDYRTN.
- With Halt or Shutdown cycles, a zero wait state operation is completed.
- When a write operation is carried out to Port 00F1H to reset the 80387, 130 wait states are inserted.

I/O CYCLE	16 MHz	20 MHz	25 MHz	33 MHz
Cycle following pipelined cycle	3 WS	3 WS	5 WS	7 WS
Cycle following non-pipelined cycle	4 WS	4 WS	6 WS	8 WS

Table 42. Typical Performance for Accesses to Local I/O

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8.0 TECHNICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for this device are listed below. Note that permanent device damage could result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}-V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}-0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	V_{SS}-0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	125	°C

8.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the recommended normal operating conditions for extended periods of time could affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	-	850	mW
Supply Current	I_{DD}	-	165	mA

8.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	±10	µA
Tristate Output Leakage	I_{OL}	-	±30	µA
I/O Pin Leakage	I_{IOL}	-	±40	µA
OUTPUT $\overline{CCHCS}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	6	mA
OUTPUTS D(0:7), $\overline{S(0:1)}$, $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	24	mA
ALL OTHER OUTPUTS				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	4	mA

Note:
When $\overline{TEST}$ = 0, all outputs and bidirectional lines are tri-stated.

8.4 AC LOAD SPECIFICATIONS

OUTPUTS	SYMBOL	MIN	MAX	UNITS
$\overline{CCHCS}$	C_L	-	75	pF
D(0:7), $\overline{S(0:1)}$, $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$	C_L	-	240	pF
All other outputs	C_L	-	50	pF

9.0 TIMING

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CLOCKS					
Operating Frequency	4/16	4/20	4/25	8/33	MHz
T1C/CLK2 Period	31.25/125	25/125	20/125	15/62.5	=CLK2
T2AC/CLK2 High Time	9/-	8/-	7/-	6.25/-	@ 2 V
T2BC/CLK2 High Time	5/-	5/-	4/-	4.5/-	@ V_{CC}
T3AC/CLK2 Low Time	9/-	8/-	7/-	6.25/-	@ 2 V
T3BC/CLK2 Low Time	7/-	6/-	4/-	4.5/-	@ 0.8 V
T4C/CLK Period	62.5/250	50/250	40/250	30/125	=CLK
T5C/CLK High Time	20/-	14/-	10/-	8/-	
T6C/CLK Low Time	15/-	12/-	10/-	8/-	
80386/80486 BUS INTERFACE					
$\overline{RDY}$					
T1B/Setup Time	20/-	12.5/-	10.5/-	7.5/	
T2B/Hold Time	3/-	3/-	3/-	4	
HLDA					
T3B/Setup Time	20/-	20/-	18/-	10	
T4B/Hold Time	3/-	3/-	3/-	4	
PA(2:31), $\overline{BE(0:3)}$					
T5B/Setup Time	22/-	18/-	19 (PA2:31) 16 (BE0:3)	15	
T6B/Hold Time	2/-	2/-	4	4	
M/$\overline{IO}$, $\overline{DC}$, $\overline{WR}$, $\overline{ADS}$					
T7B/Setup Time	22/-	20/-	19	15	
T8B/Hold Time	2/-	2/-	4	4	
$\overline{NA}$, $\overline{BS16}$, $\overline{SRDY}$					
T9B/Valid	2/15	2/20 ($\overline{SRDY}$) 2.25 (NA, BS16)	2/18 ($\overline{SRDY}$) 2/20 (NA, BS16)	2/12 ($\overline{SRDY}$) 2/15 (NA, BS16)	
WD6030 Register Read					
T10B/D (0:31) Valid	2/50	2/40	2/31	2/31	
T11B/D (0:31) Disable	2/50	2/40	2/22	2/22	
WD6030 Register Write					
T12B/D (0:31) Setup	30/-	30/-	30/-	301	
T13B/D (0:31) Hold	30/-	30/-	30/-	19	

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PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CACHE INTERFACE					
HIT					
T1I/Setup Time	25/-	20/-	15/-	11	
T2I/Hold Time	5/-	5/-	5/-	5	
MADS, HITVALID, CDIR, CDEN(0:3), TAGWR, TAGDEN, CCHCS T3I/Valid	2/20	2/24 (MADS, CDIR, CCHCS) 2/20 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	2/20 (MADS, CDIR, CCHCS) 2/17 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	2/15 (MADS, CDIR, CCHCS) 2/12 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	4
CCHWR(0:3)					
T4I/Assertion	2/20	2/25	2/20	2/15	
T5I/De-assertion	-/20	-/25	/20	/15	
T6I/Pulse Width	1.5CLK/-	1.5CLK/-	1.5CLK/-		
DATA CACHE TIMINGS REQUIRED (EXTERNAL SRAMS) **					
ADDRESS					
T1S/Access Time	-/64	-/45	-/30	-/20	
OUTPUT HOLD					
T2S/From Address Change	2/-	2/-	2/-	2/	
CHIP SELECT					
T3S/Access Time	-/64	-/45	-/35	-/20	
WRITE					
T4S/Pusle Width	-/1.5CLK	-/1.5CLK	-/1.5CLK	-/1.5CLK	
ADDRESS					
T5S/Hold from WRITE	-/2	-/2	-/2	-/2	
CACHE-WRITE					
T6S/Data Setup	-/CLK-7	-/CLK-7	-/CLK-7	-/CLK-7	
T7S/Data Hold	-/0	-/0	-/0	-/0	
TAGRAM TIMINGS REQUIRED (EXTERNAL TAGRAM) ***					
HIT					
T1T/From Address	-/57	-/47	-/38	-/23	
WRITE					
T2T/Pulse Width	-/CLK2	-/CLK2	-/CLK2	-/CLK2	
DRAM INTERFACE					
RAS, MUX, CAS(0:3), DRMWR(0:3), MDEN(0:3), MDIR, PARCLK, DRMA(18:19) T1D/Valid	2/20	2/25 [MDEN(0:3), DRMWR(0:3), PARCLK MDIR] 2/20 [RAS, MUX, CAS(0:3), DRMA(18:19)]	2/20 [MDEN(0:3), DRMWR(0:3), PARCLK] 2/25 (MDIR) 2/17 [RAS, MUX, CAS(0:3), DRMA(18:19)]	2/15 [MDEN(0:3), DRMWR(0:3), PARCLK MDIR] 2/12 [RAS, MUX, CAS(0:3), DRMA(18:19)]	1
DRMWR(0:3)					
T2D/Hold from CAS	0/-	0/-	0/-	0/-	

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CHANNEL CONTROLLER					
CHRDYRTN*					
DS16RTN, DS32RTN					
T1E/Setup	25	25	20	20/-	2
T2E/Hold	5/-	5/-	5/-	5/-	2
A0					
T3E/Valid from BE(0:3)	-/25	-/35	-/35	-/30	
T4E/Hold from S(0:1)	0/-	0/-	0/-	0	
ADL, S(0:1), CMD, RDEN, RDLE, WREN(0:1, H), WRLE, SWPBYT, SWPWORD, SWPDIR			2/25 [ADL, CMD, S(0:1)]	2/20 (ADL,CMD)	
T5E/Valid	2/20	2/25	2/20 (Rest)	2/15 (Rest)	
CHANNEL MASTER ACCESSING SYSTEM BOARD DRAM					
PA (2:31), BE(0:3), M/IO, SBHE, MADE24, S(0:1), ADL, CMD, TR32					
T1M/Setup to CLK2	15/-	15/-	15/-	15/-	2
T2M/Hold from CLK2	2/-	2/-	2/-	2/	2
UCHRDY					
T3M/De-assert from address	-/35	-/35	-/35	/35	
T4M/De-assert from S(0:1)	0/30	-/30	-/30	-/30	
T5M/Valid from CLK2	-/15	-/20	-/20	-/20	
MEMDS32					
T6M/Assert from Addr, M/IO	-/25	-/25	-/25	-/25	
RDEN, WREN(0:1, H)					
T7M/Valid from CMD	-/20	-/20	-/20	-/20	
READ DATA					
T8M/From UCHRDY	-/60	-/60	-/60	-/60	3
CENTRAL TRANSLATOR					
SWPWORD from S(0:1), CMD, TR32, DS32RTN, BE(0:3) T1X/Valid	-/25	-/25	-/25	-/25	

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NOTES

1. These outputs should track each other and the cache control outputs.
2. These inputs can be asynchronous to CLK2.
3. This is a system level specification.
4. These outputs should track each other and the DRAM controller outputs.

* CHRDYRTN can tolerate a 20 ns setup.

** The SRAMs used should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

*** The TagRAMs used, whether built out of discrete components or not, should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

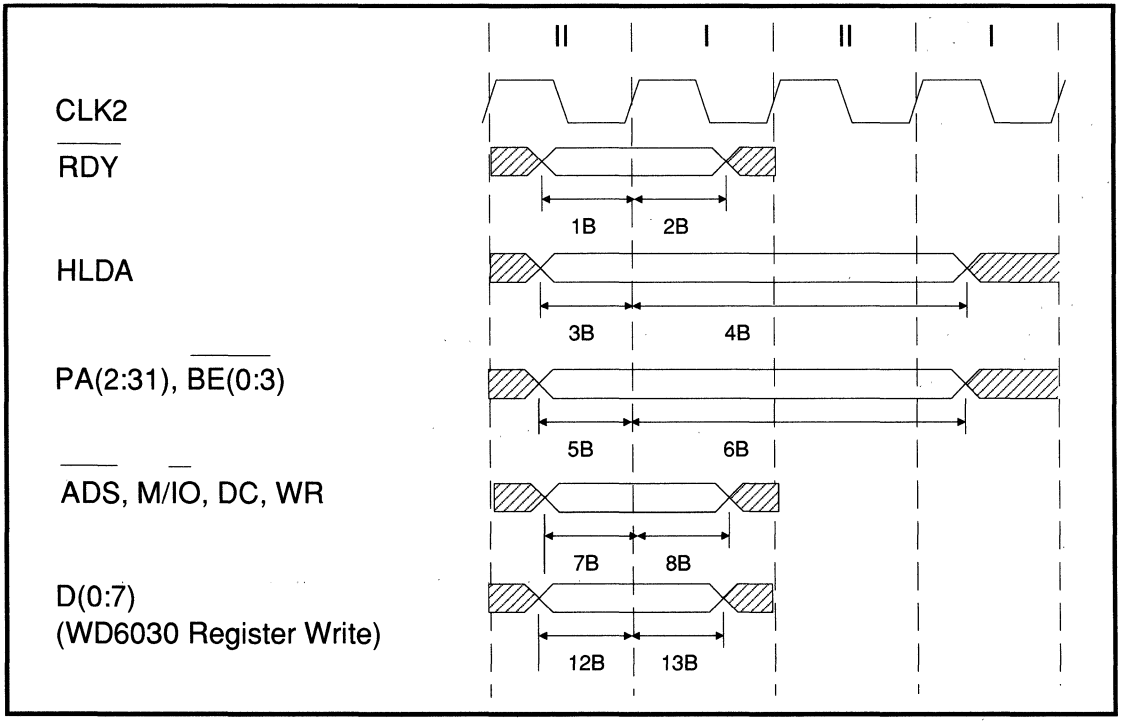

Figure 15. 80386/80486 Bus Interface Input Setup And Hold

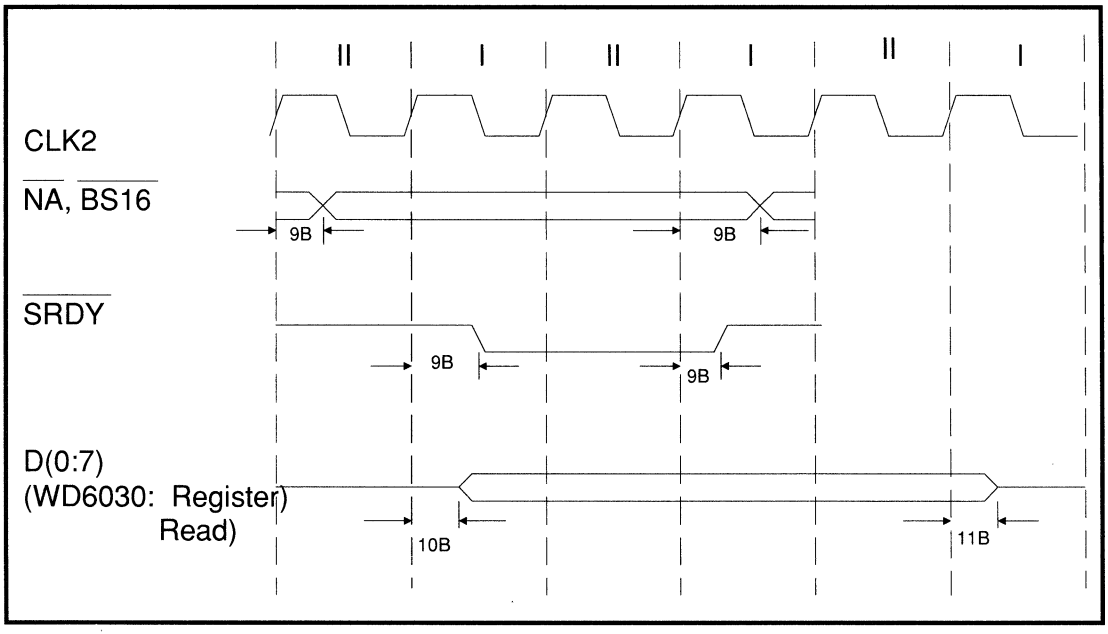

Figure 16. 80386/80486 Bus Interface Output Valid Delay

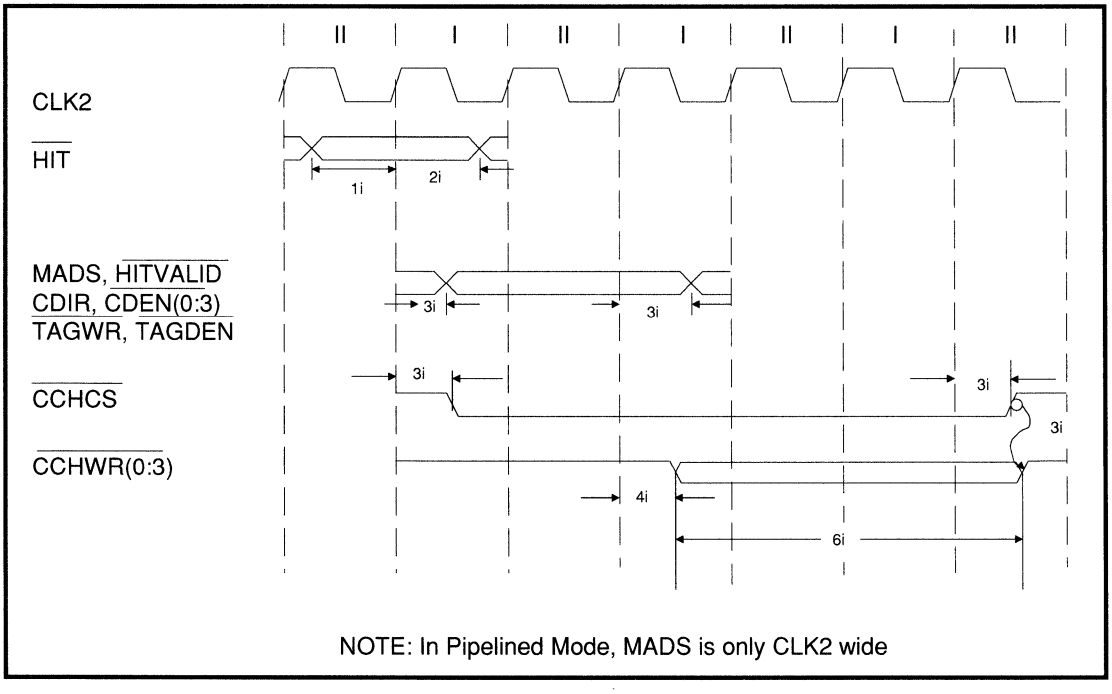

Figure 17. WD6030 Cache Interface Timing

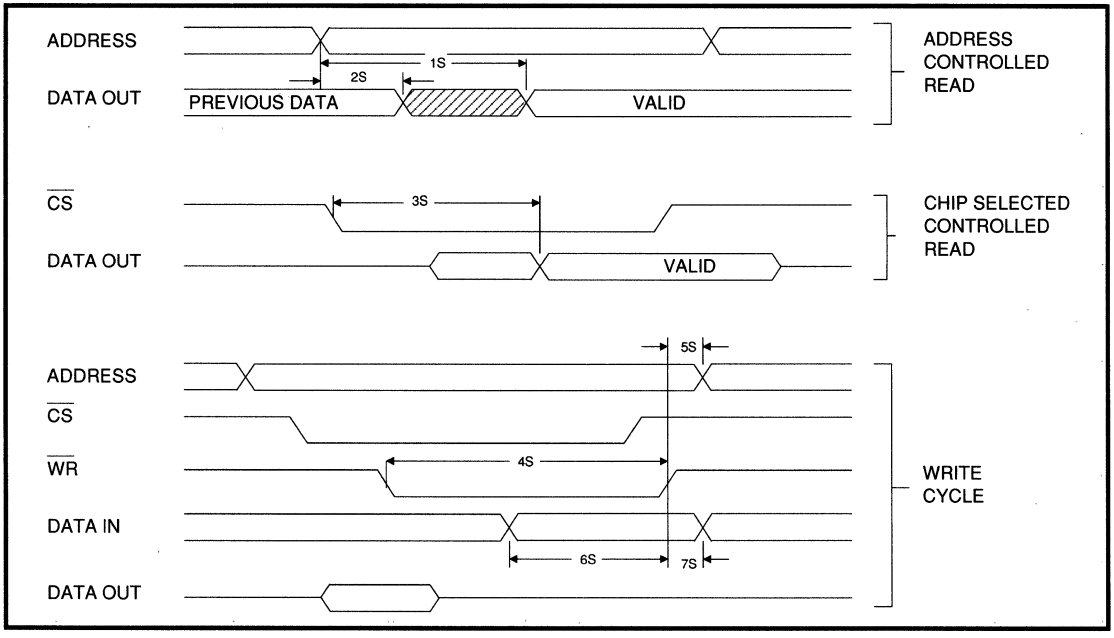

Figure 18. Data Cache SRAM Timing

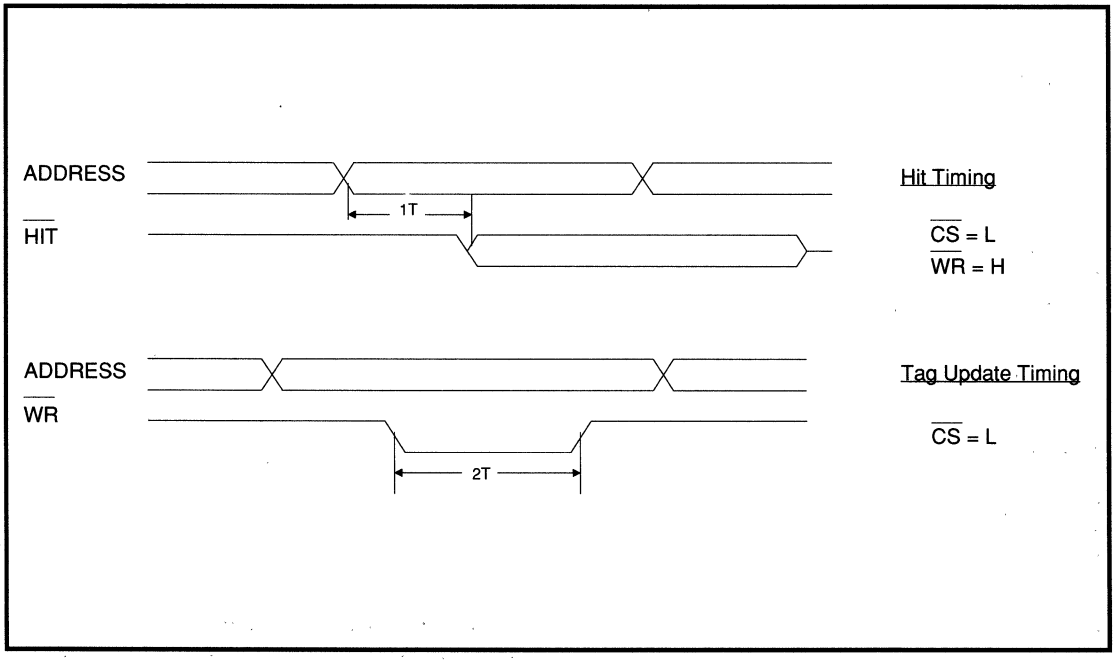

Figure 19. WD6030 TagRAM Timing

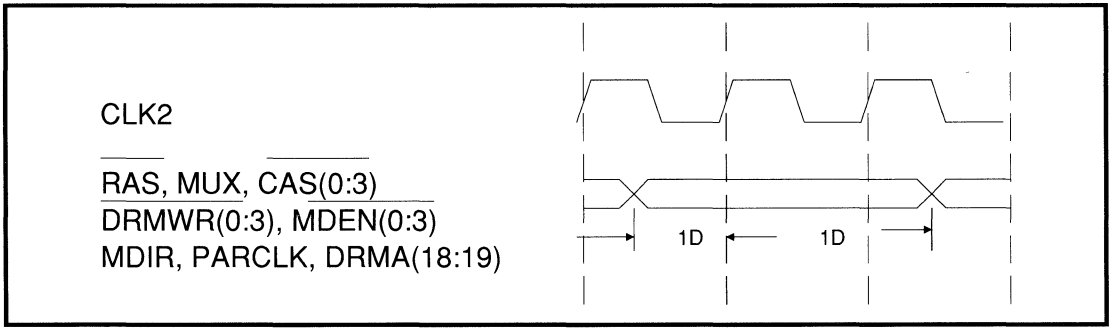

Figure 20. DRAM Interface Output Valid Delay Timing

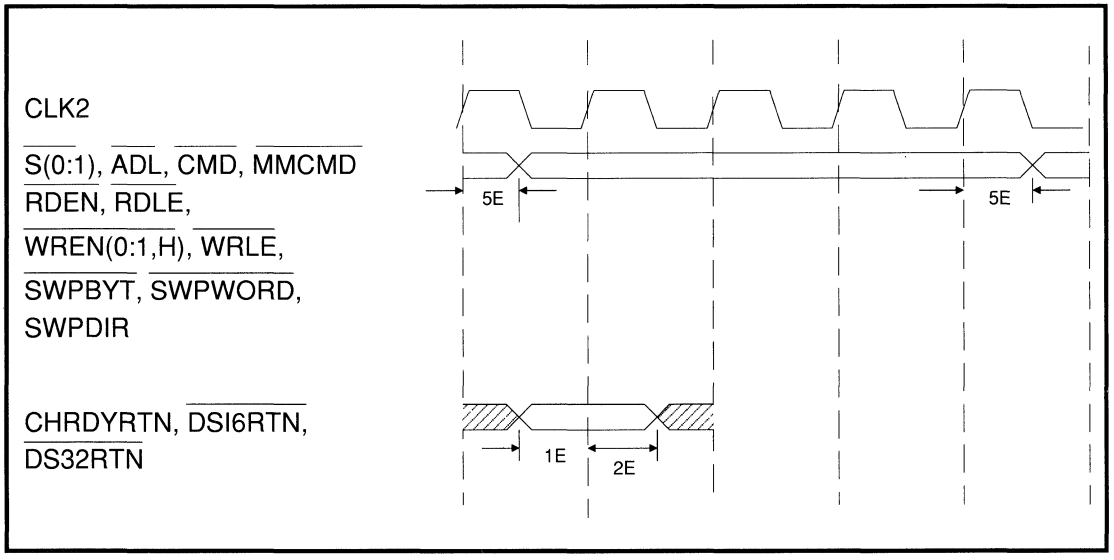

Figure 21. Channel Controller Timing

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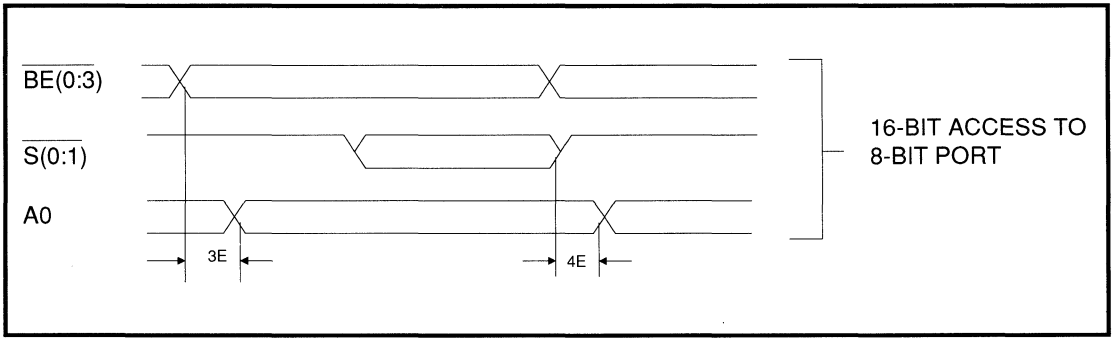

Figure 22. Channel Controller: 16-Bit Access to 8-Bit Port

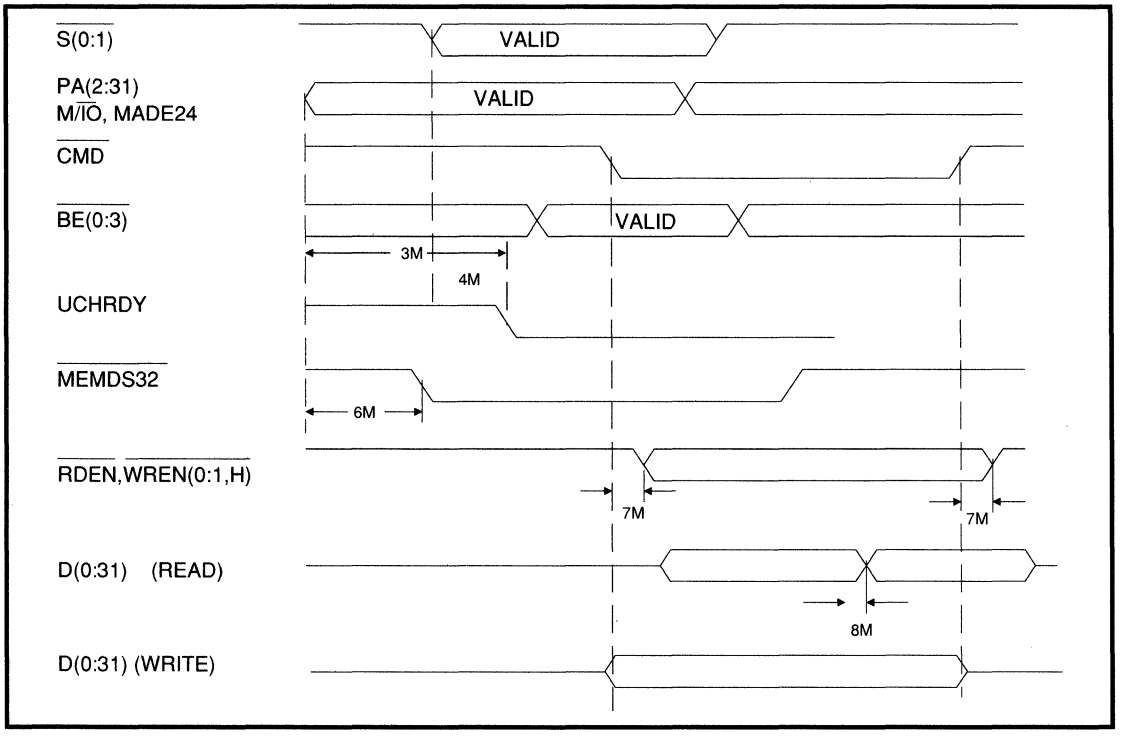

Figure 23. Channel Master Accesses to System Board DRAM

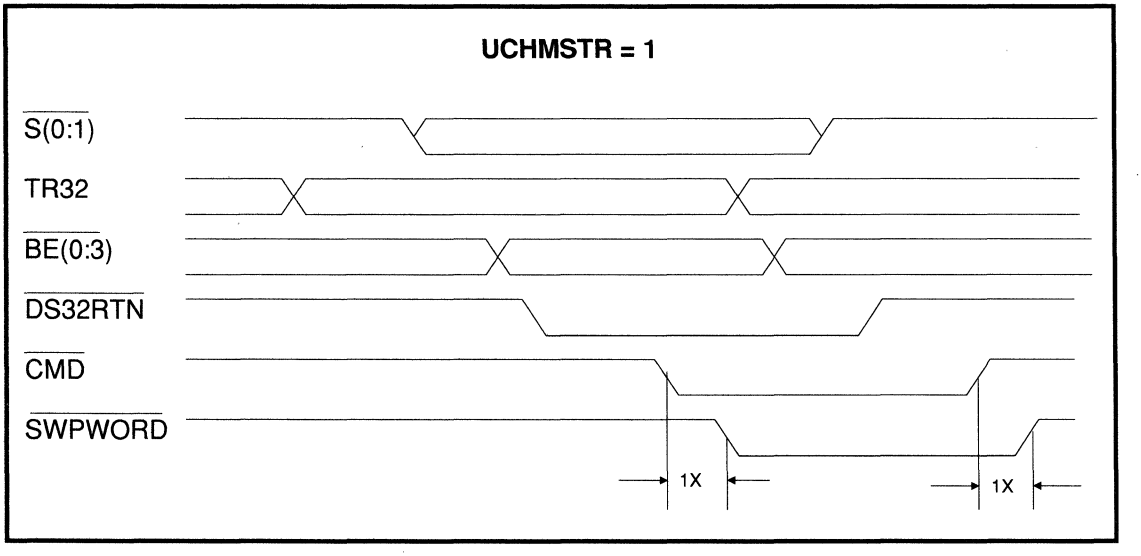

Figure 24. Central Translator Function

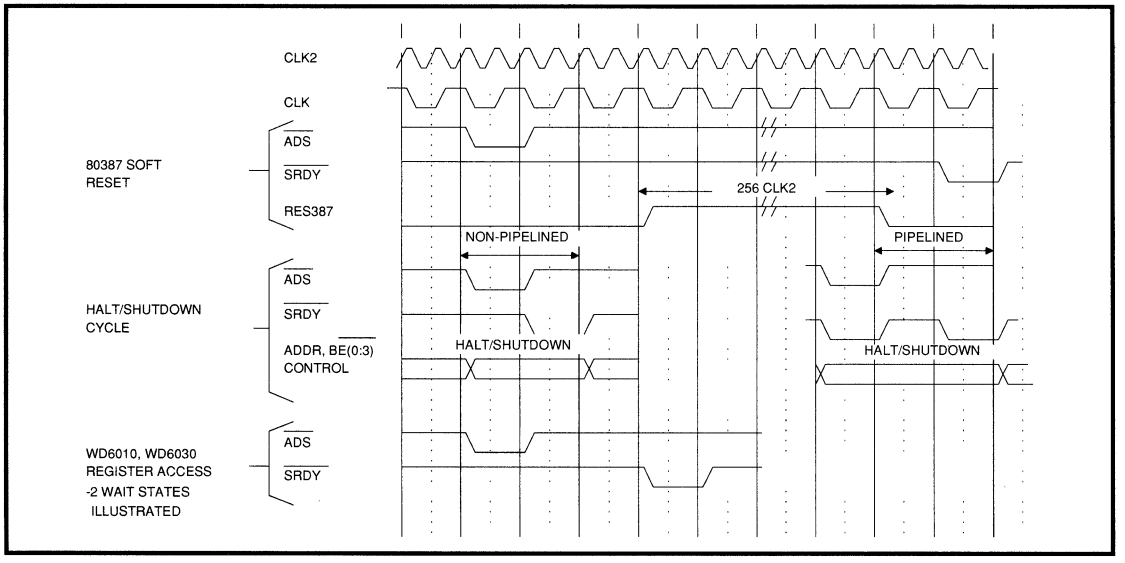

Figure 25. Miscellaneous Cycles

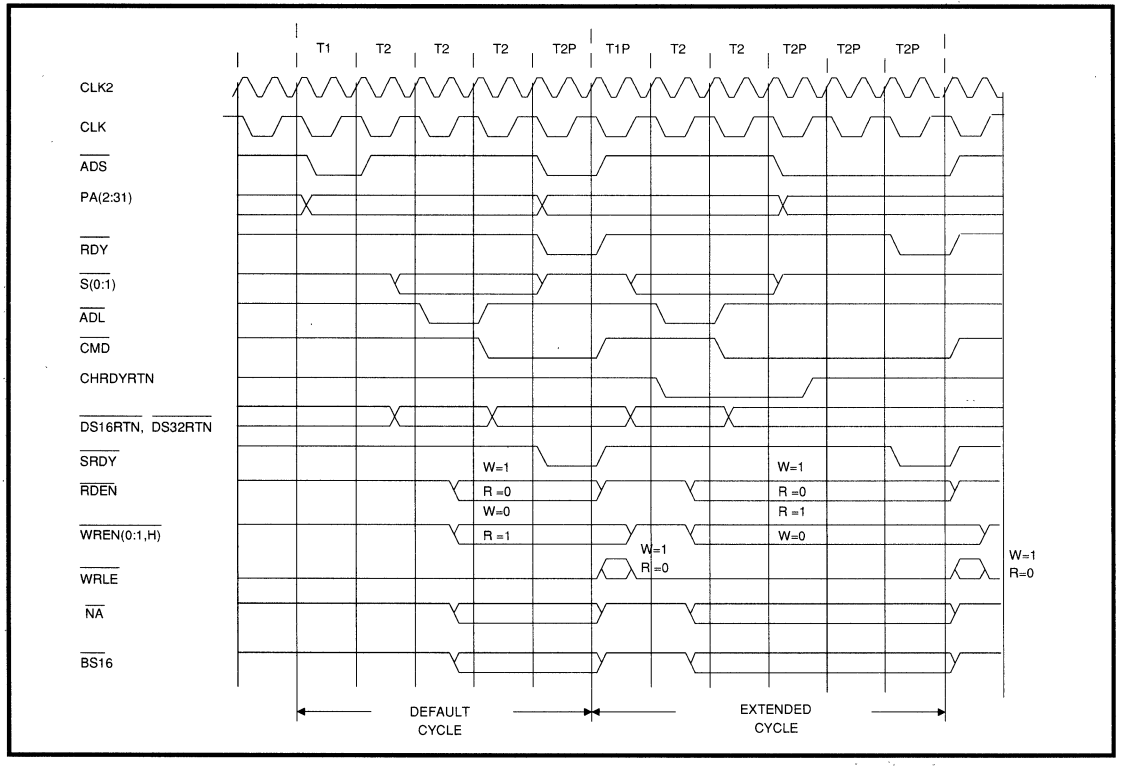

Figure 26. Channel Accesses 16 MHz Back-to-Back Cycles

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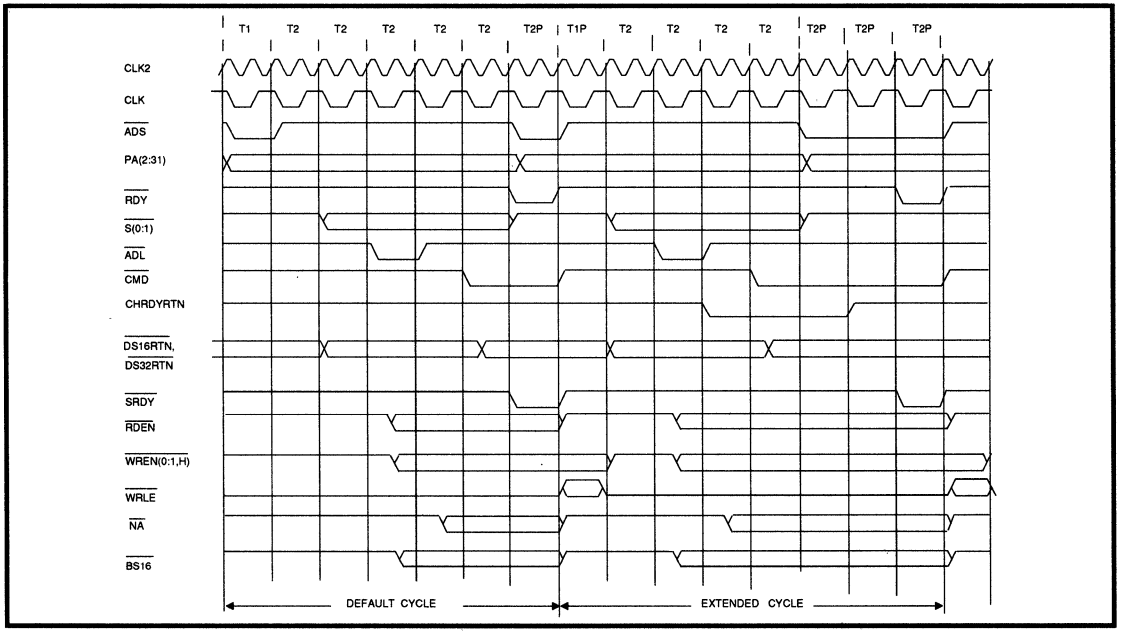

Figure 27. Channel Accesses 20 MHz Back-to-Back Cycles

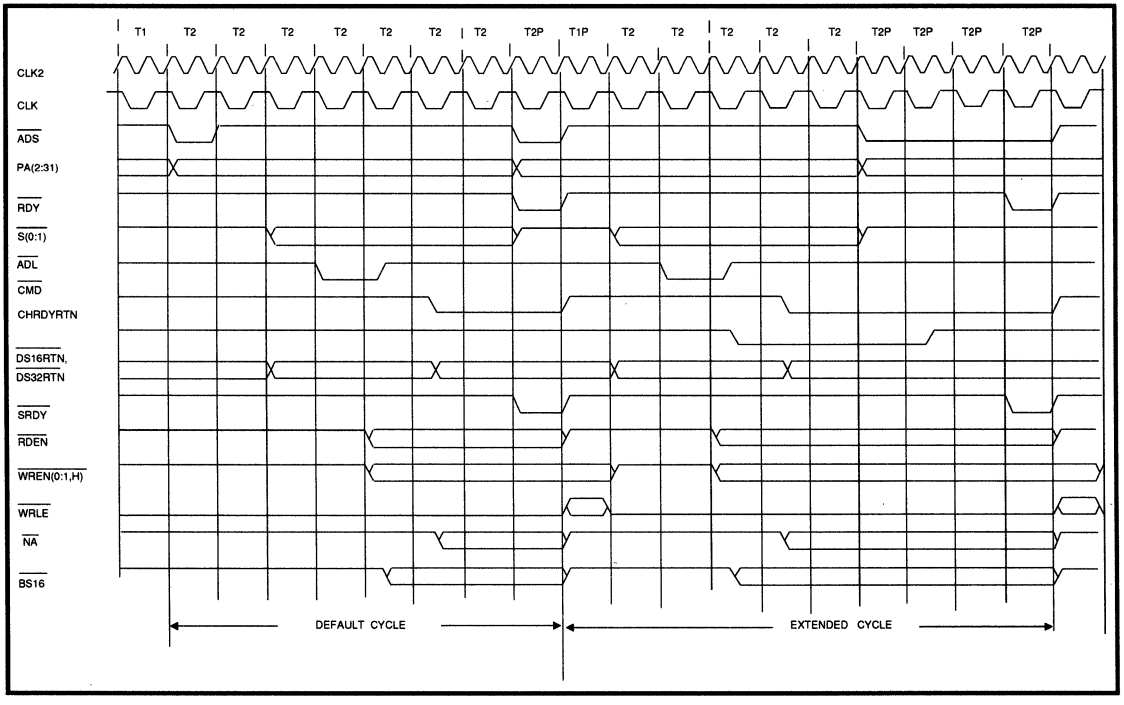

Figure 28. Channel Access 25 MHz Back-to-Back Cycles

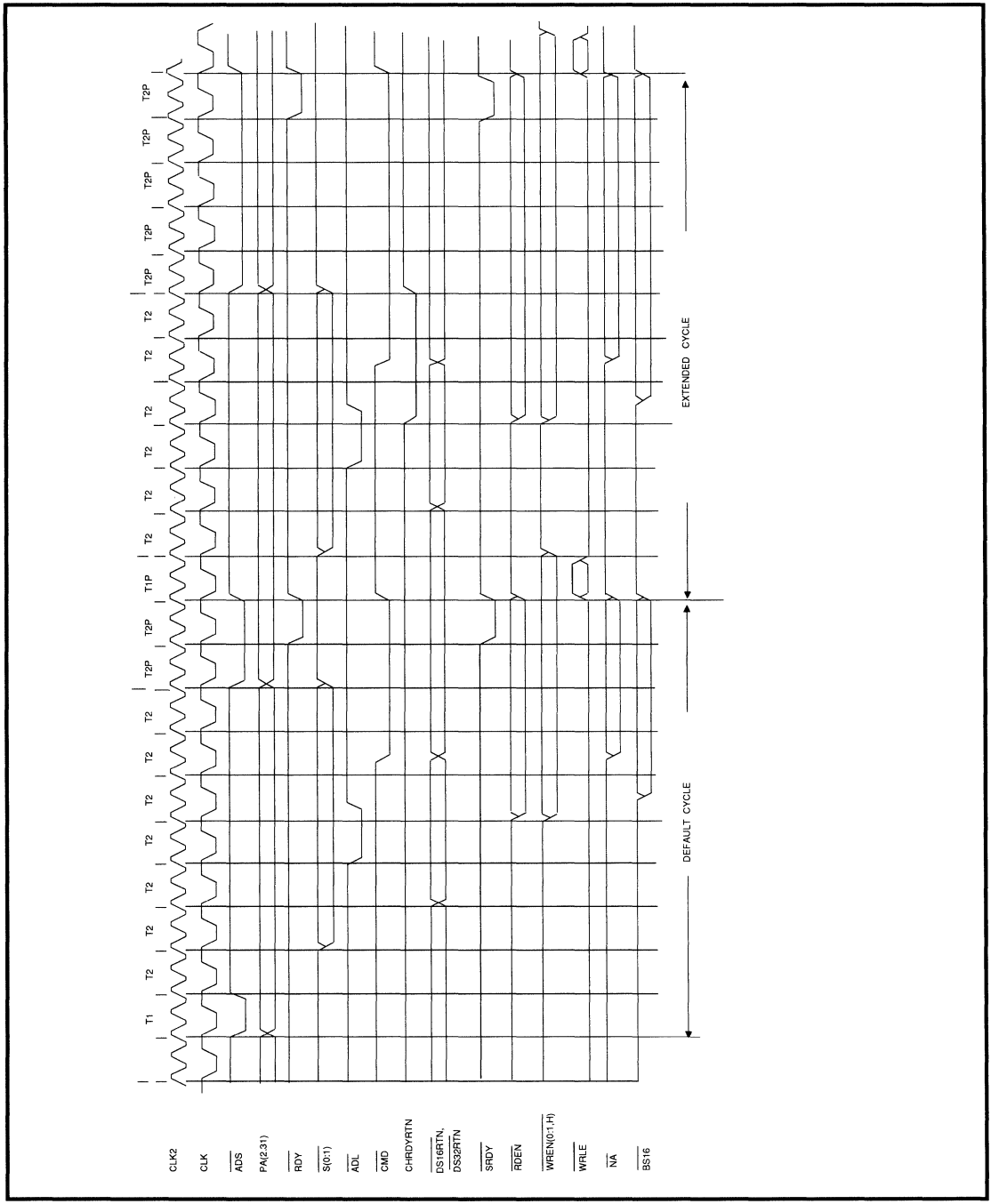

Figure 29. Channel Acess 33 MHz Back-to-Back Cycles

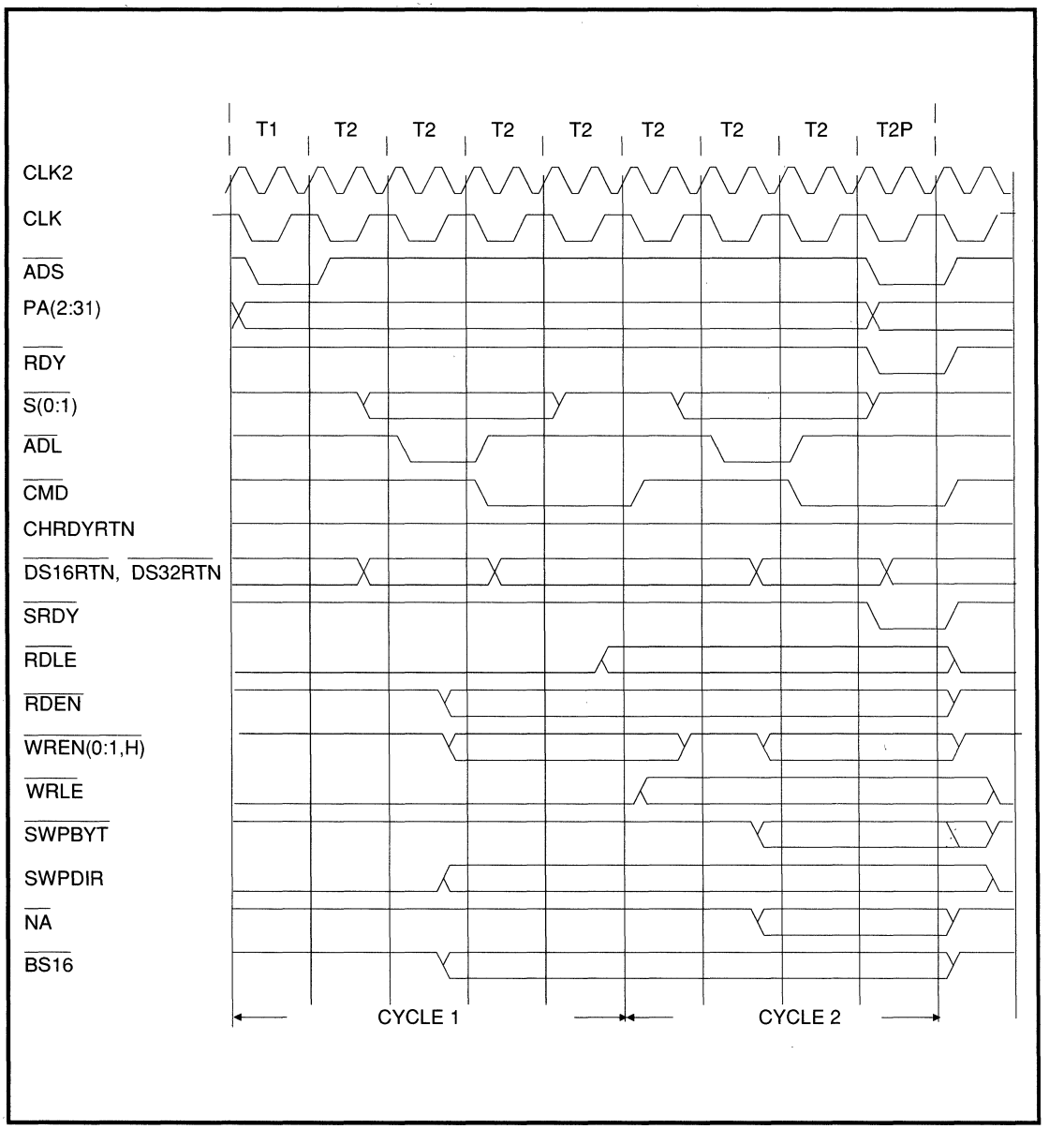

Figure 30. 16 MHz 16-Bit Access To 8-Bit Channel Port

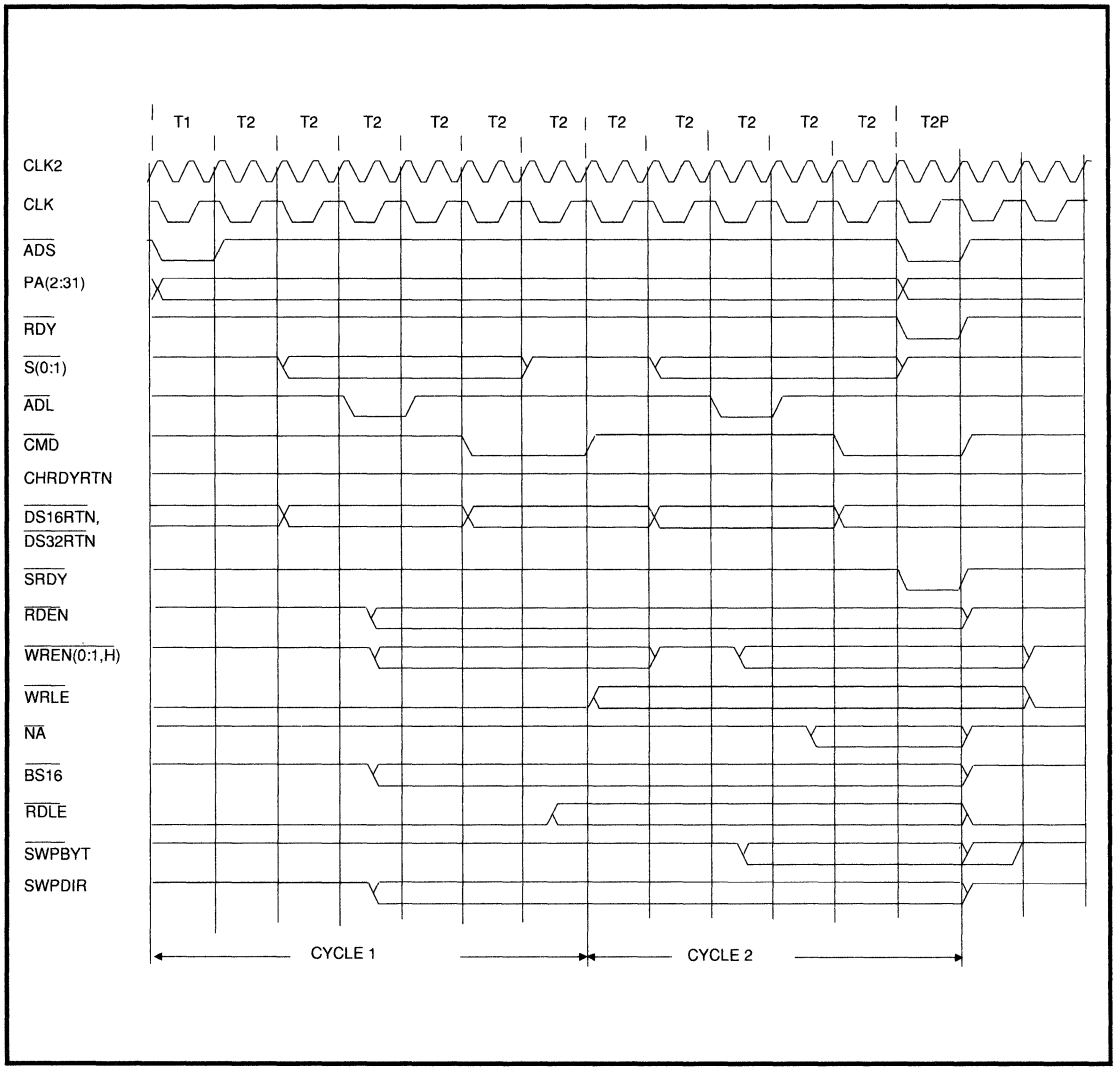

Figure 31. 20 MHz 16-Bit Access To 8-Bit Channel Port

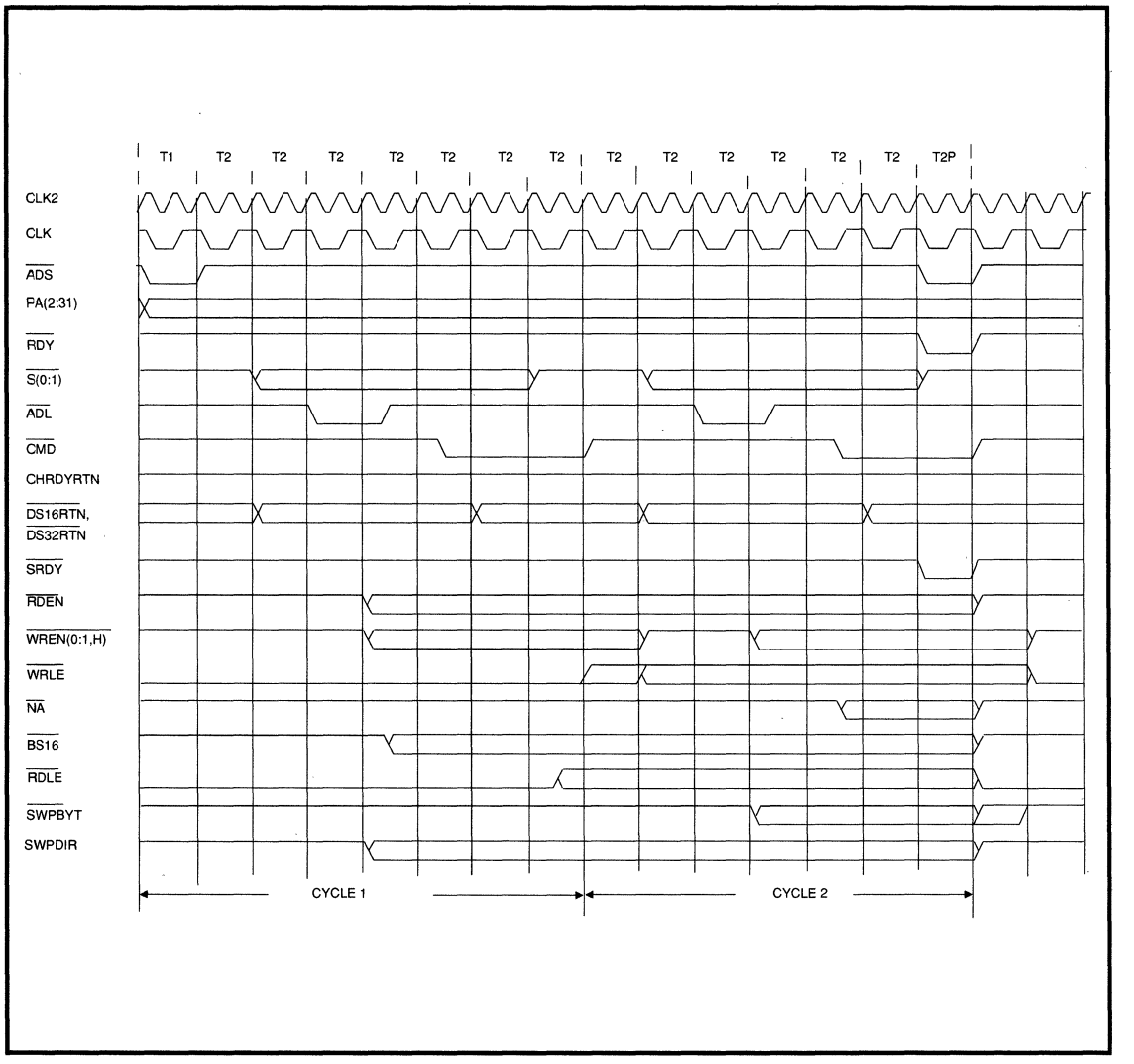

Figure 32. 25 MHz 16-Bit Access To 8-Bit Channel Port

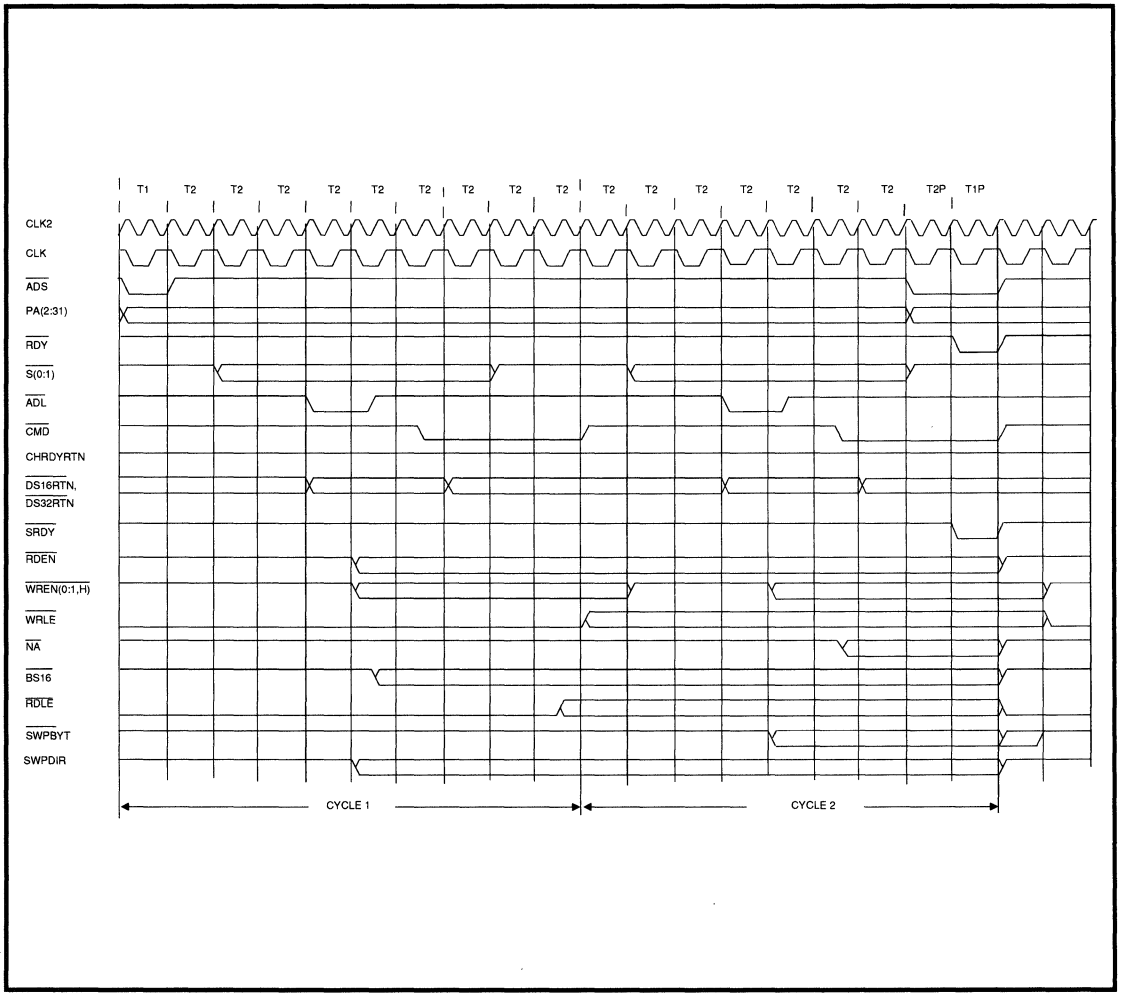

Figure 33. 33 MHz 16-Bit Access To 8-Bit Channel Port

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10.0 PACKAGE DIMENSIONS

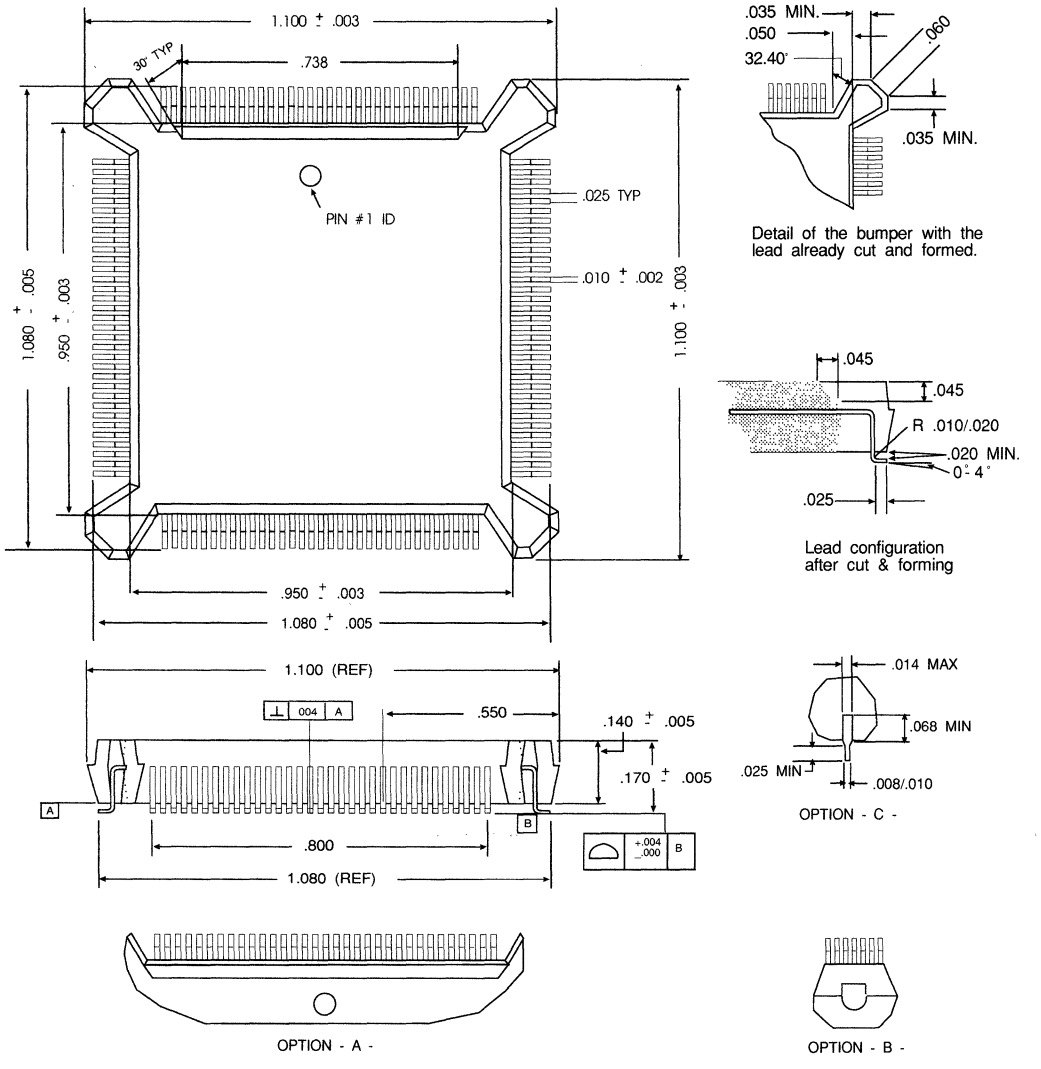

Figure 34. 132-Pin JEDEC Flat Pack Packaging Diagram