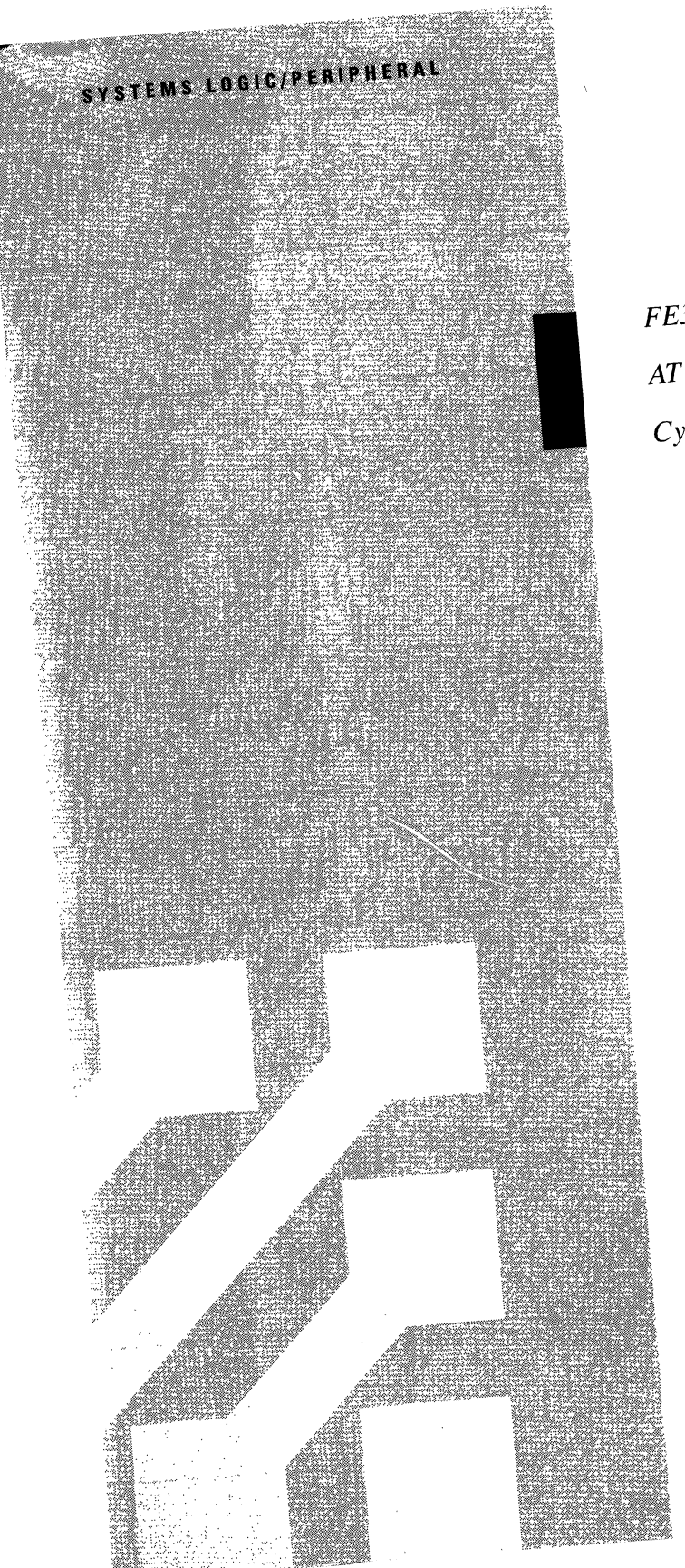
SYSTEMS LOGIC/PERIPHERAL

# *FE3001*

# *AT Clock Generation and Cycle Control Device*



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# 1.0 INTRODUCTION

## 1.1 DESCRIPTION

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an IBM AT compatible computer. It is part of the FE3600 chip set intended to simplify the design of 80286 based AT computers.

Its features include programmable CPU and DMA clock generation, system clock generation, programmable bus timing, programmable wait state generator, refresh and DMA controls, bus arbitration logic, NMI generator and parity error logic, reset/shutdown control, sleep mode, and 80286 interface logic and packaged in an 84-pin PLCC.

## 1.2 FEATURES

- Programmable CPU and DMA clock generator
- System clock generator
- Programmable bus timing
- Programmable wait state generator
- Refresh and DMA controls
- Bus arbitration logic
- NMI generator and Parity error logic
- Reset/shutdown control
- Sleep mode
- 80286 interface logic
- 1.25 micron HCMOS technology
- 84-Pin PLCC

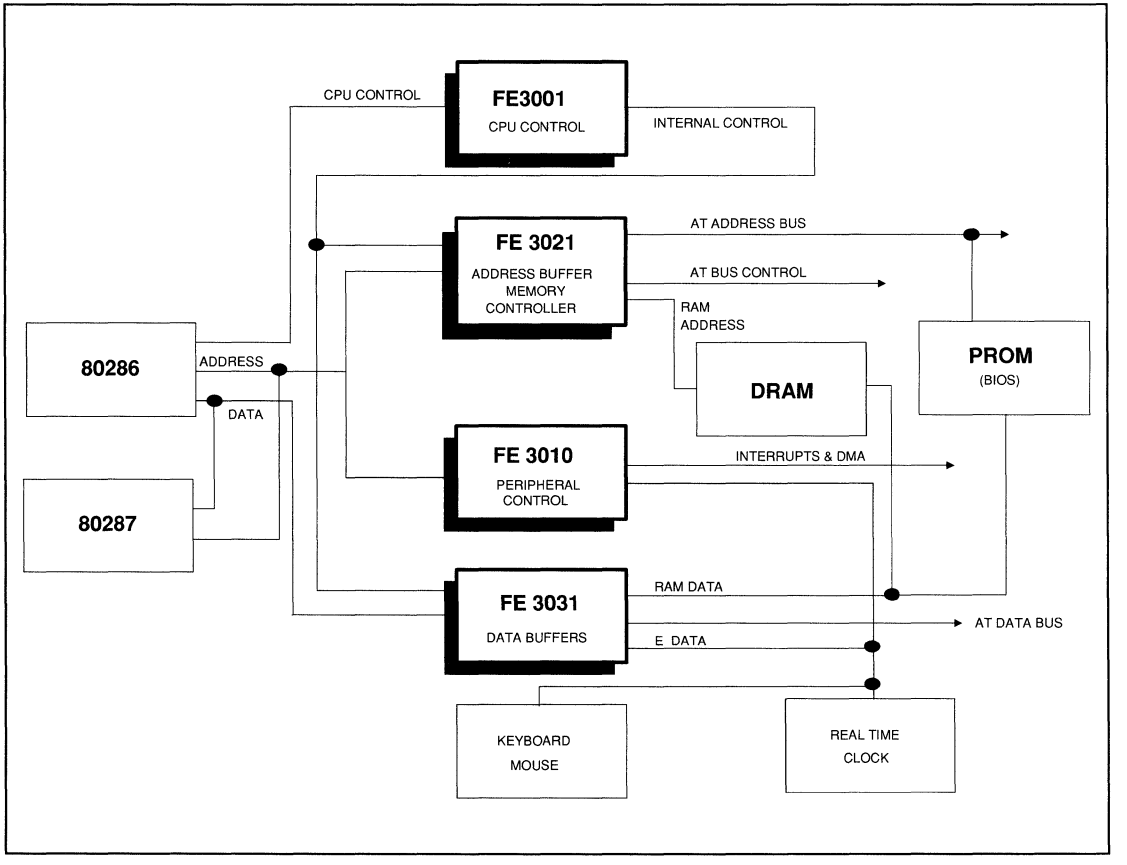



**FIGURE 1-1. FE3600 CHIP SET FUNCTIONAL BLOCK DIAGRAM**

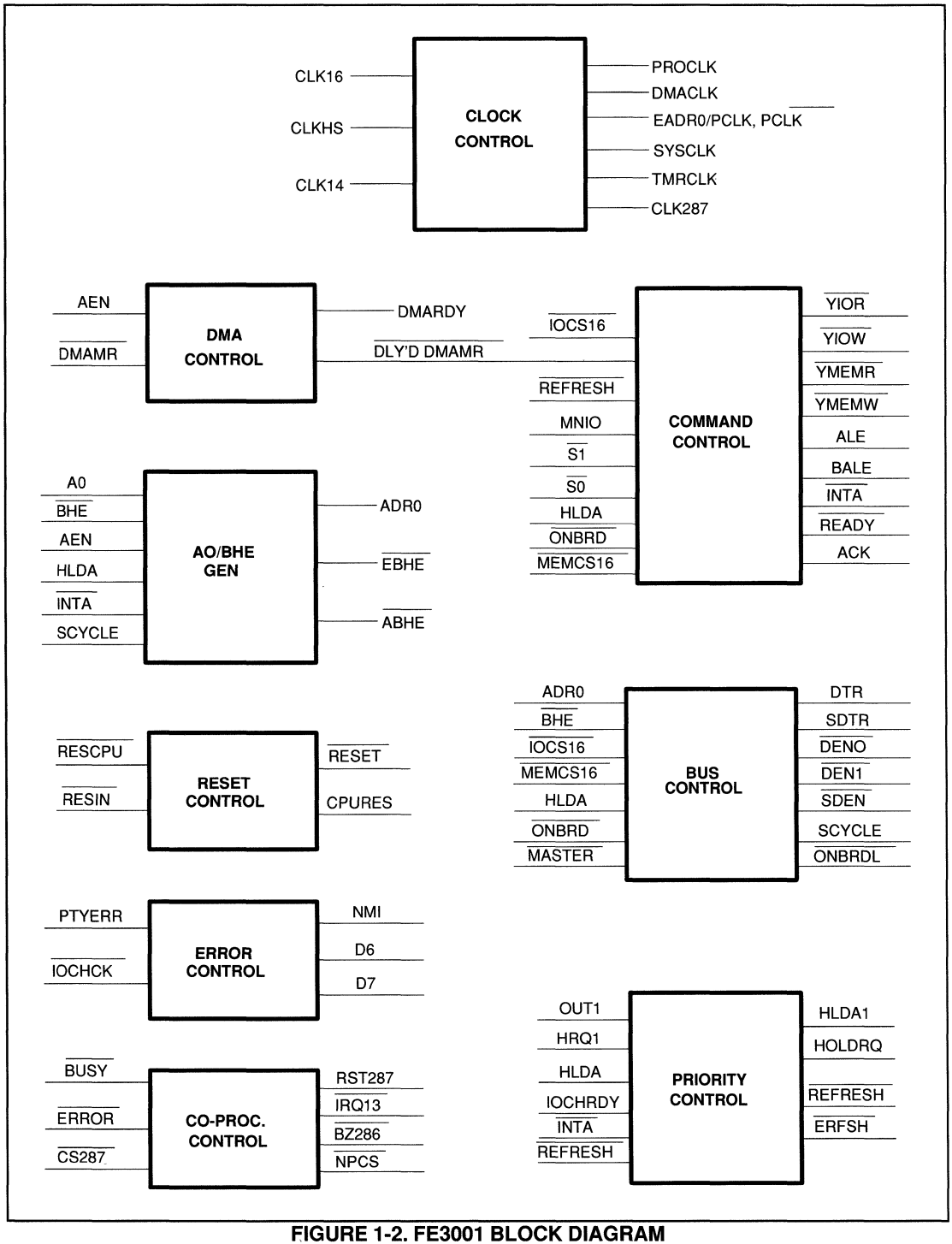



**FIGURE 1-2. FE3001 BLOCK DIAGRAM**

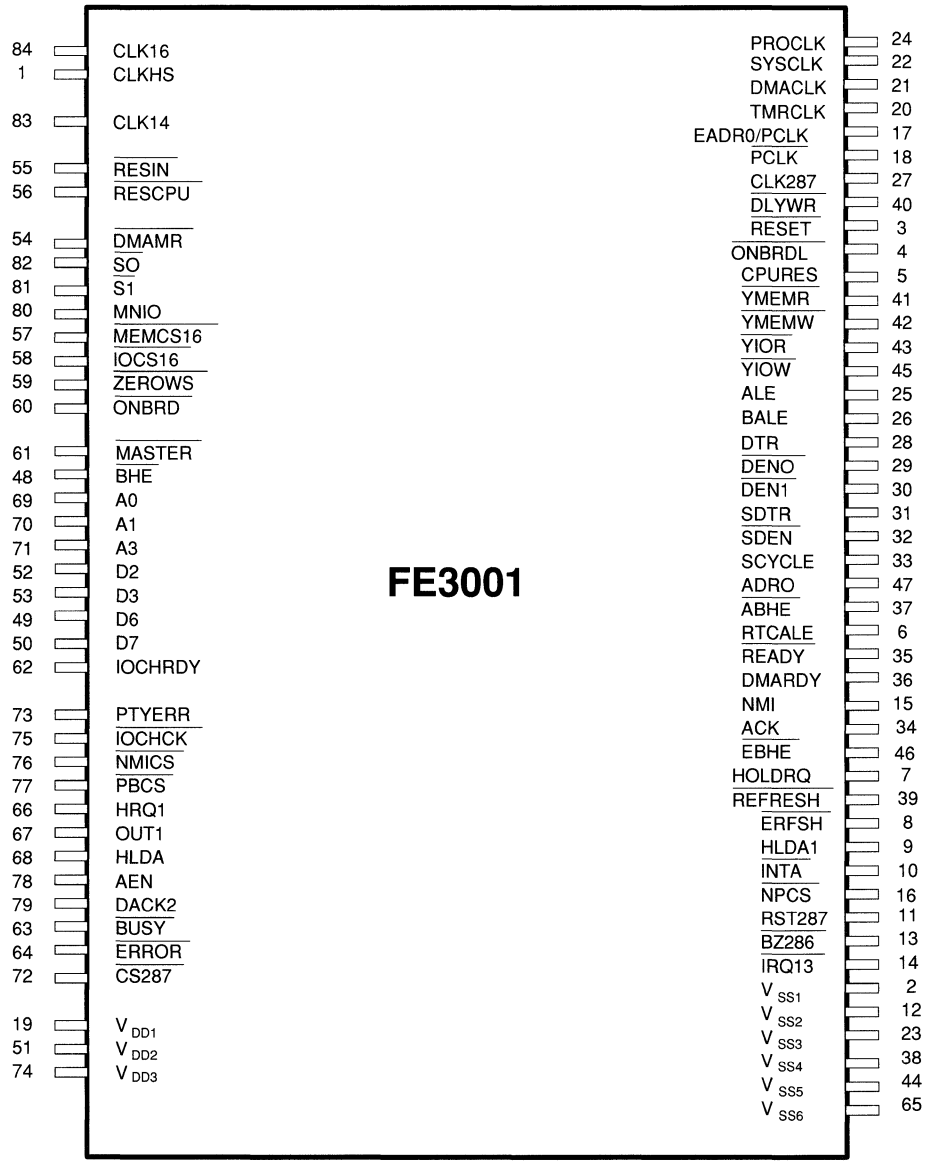



**FIGURE 1-3. FE3001 PIN ASSIGNMENTS**

| PIN# | SIGNAL | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | CLKHS | I | High speed clock input. This provides the high speed clock when selected. When CLK16 (pin 84) is pulled high, this input (divided by two) is used as the low speed clock. |
| 2 | $V_{SS1}$ | | Ground. |
| 3 | $\overline{\text{RESET}}$ | O | Reset to the system. |
| 4 | ONBRDL | O | ONBRD input latched by ALE internally.Follows $\overline{\text{ONBRD}}$ when HLDA high. |
| 5 | CPURES | O | Reset to 80286. |
| 6 | RTCALE | O | Real Time Clock Address Latch Enable (I/O address 70H). |
| 7 | HOLDRQ | O | Hold request to 80286 for DMA or Refresh. |
| 8 | $\overline{\text{ERFSH}}$ | O | Enable refresh address signal to FE3010. Puts refresh address on address bus. |
| 9 | HLDA1 | O | DMA hold acknowledge signal to FE3010. Not active during refresh. |
| 10 | $\overline{\text{INTA}}$ | O | Interrupt acknowledge to FE3010. |
| 11 | RST287 | O | Reset to 80287 (Write to I/O address F1H or system reset). |
| 12 | $V_{SS2}$ | | Ground. |
| 13 | $\overline{\text{BZ286}}$ | O | 80287 busy signal to 80286. Latched low by 80287 ERROR signal. |
| 14 | $\overline{\text{IRQ13}}$ | O | Interrupt request 13 for 80287 error to FE3010. |
| 15 | NMI | O | Non-Maskable Interrupt to 80286.<br>Generated in response to a parity error or bus IOCHCK. |
| 16 | $\overline{\text{NPCS}}$ | O | 80287 Co-processor chip select. (I/O Addresses F8H, FAH and FCH). |
| 17 | EADR0/PCLK | O | Tristate output to AT bus SA0 & 7.16 MHz clock for keyboard controller. |
| 18 | $\overline{\text{PCLK}}$ | O | Inverted PCLK. |
| 19 | $V_{DD1}$ | | +5 V $V_{DD}$. |
| 20 | TMRCLK | O | 1.19 MHz timer clock to FE3010. |
| 21 | DMACLK | O | Software selectable clock for DMA to FE3010. |
| 22 | SYSCLK | O | System clock needed for bus timing.<br>See description in synchronization section. |
| 23 | $V_{SS3}$ | | Ground. |
| 24 | PROCLK | O | Software selectable 80286 clock. |
| 25 | ALE | O | Local Address Latch Enable. |
| 26 | BALE | O | Bus Address Latch Enable. (Programmable) |
| 27 | CLK287 | O | Clock for 80287. See clock section for details. |
| 28 | DTR | O | Data direction to FE3031 data buffer. |
| 29 | $\overline{\text{DEN0}}$ | O | Low byte PC/AT Bus data enable to FE3031 data buffer. |
| 30 | $\overline{\text{DEN1}}$ | O | High byte PC/AT Bus data enable to FE3031 data buffer. |
| 31 | SDTR | O | PC/AT Bus byte swap direction to FE3031 data buffer. |
| 32 | $\overline{\text{SDEN}}$ | O | PC/AT Bus byte swap enable to FE3031 data buffer. |
| 33 | SCYCLE | O | Latch low byte during byte swap read. |

**TABLE 1-1. SIGNAL DESCRIPTIONS**

| PIN | SIGNAL | TYPE | DESCRIPTION |
|---|---|---|---|
| 33 | SCYCLE | O | Latch low byte during byte swap read. |
| 34 | ACK | O | DMA or Refresh Acknowledge signal to the PC/AT bus. |
| 35 | READY | O | Ready to 80286. |
| 36 | DMARDY | O | When high allows FE3010 to complete a DMA cycle. |
| 37 | ABHE | O | High byte enable for devices on local bus. |
| 38 | $V_{SS4}$ | | Ground. |
| 39 | REFRESH | I/O | Refresh cycle. Generated from FE3010 timer signal OUT1 or externally from the bus. |
| 40 | DLYWR | I/O | YIOW delayed to the FE3010, active edge delayed one PROCLK. Input from FE3010 during DMA to generate YIOW. |
| 41 | YMEMR | I/O | Memory read. Input during Master cycle. |
| 42 | YMEMW | I/O | Memory write. Input during HLDA cycle. |
| 43 | YIOR | I/O | I/O read. Input during HLDA cycle. |
| 44 | $V_{SS5}$ | | Ground. |
| 45 | YIOW | I/O | I/O write. Input during Master cycle. |
| 46 | EBHE | I/O | High byte enable to expansion bus. Input during Master cycle. |
| 47 | ADR0 | I/O | Low byte enable. Latched with ALE during a CPU cycle, driven low during 16-Bit DMA cycles. |
| 48 | BHE | I/O | High byte enable from the 80286. Output during MASTER and DMA cycles for use by the FE3021. |
| 49 | D6 | I/O | Peripheral data bus bit 6. |
| 50 | D7 | I/O | Peripheral data bus bit 7. |
| 51 | $V_{DD2}$ | | +5 V $V_{DD}$. |
| 52 | D2 | I | Peripheral data bus bit 2. |
| 53 | D3 | I | Peripheral data bus bit 3. |
| 54 | DMAMR | I | DMA memory read from DMA controller. |
| 55 | RESIN | I | System reset input. |
| 56 | RESCPU | I | CPU reset input from keyboard controller. |
| 57 | MEMCS16 | I | Signals 16 bit memory transfer capability on the PC/AT bus. |
| 58 | IOCS16 | I | Signals 16 bit I/O transfer capability on the PC/AT bus. |
| 59 | ZEROWS | I | Zero wait state bus cycle request. See description for more details. |
| 60 | ONBRD | I | 16 bit on-board DRAM memory, BIOS, or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles. |
| 61 | MASTER | I | Master on PC/AT bus has control of the bus when asserted. |
| 62 | IOCHRDY | I | Current bus cycle may complete when high. May be used to extend CPU, DMA, or refresh cycles. |
| 63 | BUSY | I | 80287 co-processor busy. |
| 64 | ERROR | I | Error from 80287. |
| 65 | $V_{SS6}$ | | Ground. |
| 66 | HRQ1 | I | Hold request from DMA controller in FE3010. |

**TABLE 1-1. SIGNAL DESCRIPTIONS, Continued**

| PIN | SIGNAL | TYPE | DESCRIPTION |
|---|---|---|---|
| 67 | OUT1 | I | Refresh timer input from FE3010. |
| 68 | HLDA | I | Hold acknowledge from 80286. |
| 69 | A0 | I | Local 80286 address bus 0. |
| 70 | A1 | I | Local 80286 address bus 1. |
| 71 | A3 | I | Local 80286 address bus 3. |
| 72 | CS287 | I | 80287 select decode from FE3021 (0E0H - 0FFH). |
| 73 | PTYERR | I | On-board RAM parity error. Sampled on the first falling edge of PROCLK after YMEMR goes high. |
| 74 | $V_{DD3}$ | | +5 V $V_{DD}$. |
| 75 | IOCHCK | I | Error from PC/AT bus. |
| 76 | NMICS | I | NMI port enable decode (07XH). Also used for programming bus control registers. |
| 77 | PBCS | I | Port B chip select decode (061H - 06FH, 0DD). See register description for decode definitions. |
| 78 | AEN | I | DMA cycle enable from FE3010. |
| 79 | DACK2 | I | 16 bit DMA acknowledge from FE3010. |
| 80 | M/IO | I | 80286 memory/IO select. High indicates memory halt, or shut-down cycles. Low indicates I/O or interrupt acknowledge cycles. |
| 81 | S1 | I | 80286 Status 1. |
| 82 | S0 | I | 80286 Status 0. |
| 83 | CLK14 | I | 14.318 MHz clock input used to derive TMRCLK, EADR0/PCLK, and PCLK. |
| 84 | CLK16 | I | 16 MHz clock input. This provides the low speed CPU clock for 8 MHz operation. When this pin is pulled high, CLKHS ÷ 2 is used as the low speed clock. |

**TABLE 1-1. SIGNAL DESCRIPTIONS, Continued**

# 2.0 FUNCTIONAL DESCRIPTION

## 2.1 OVERVIEW

The FE3001 is designed to run with the FE3010 peripheral controller, and the FE3021 and FE3031 buffers/memory controls to create a 16 MHz or 20 MHz PC/AT compatible system. The basic architecture of an AT compatible system using the FE3600B chip set involves putting the system DRAM on the local data and command bus, allowing high speed access. The BIOS ROM can be put on the local bus or expansion bus; the FE3021 has provisions especially to use the ROM on the higher speed bus. During accesses to local memory, the data buffer controls in the FE3001A prevent data collisions between the local and expansion buses. The FE3021 and FE3031 also inhibit memory read and write signals to the expansion bus for local memory accesses.

The FE3001 generates all of the clocks needed in the system. The CPU clock to the 80286 processor (PROCLK) is programmable, as is the DMA clock for the DMA controller in the FE3010 (DMACLK). The expansion bus clock (SYSCLK) and coprocessor clock for the 80287 (CLK287) automatically adjust to the current operating configuration. The clock for the timers in the FE3010 (TMRCLK) is fixed at 1.19 MHz, and the clocks for the keyboard controller (PCLK and $\overline{\text{PCLK}}$) are fixed at 7.16 MHz.

The FE3001 has registers to delay the five commands (memory read and write, I/O read and write, interrupt acknowledge) during a CPU cycle and control the length of the commands based on various input signals (16-bit memory, 16-bit I/O, on-board memory, fast 16-bit I/O device, and zero wait state device). On power-up, these registers are loaded with values to run the system with a 16 MHz PROCLK (8 MHz system) with full AT compatibility and no register programming necessary. Before switching to high speed operation, it is necessary to program the registers for proper bus emulation. These registers eliminate the need to either slow down the processor for expansion bus operations or run the bus asynchronously. Note that a 16 MHz system can be made to exactly match the bus timing of an 8 MHz system.

## 2.2 CLOCK GENERATOR

This module generates clocks for the CPU, DMA, 8042 keyboard controller, timer and 80287 Numeric Processor. The CPU clock is software selectable for low speed or high speed CPU operation. The DMA clock is also software selectable between standard and high speed. The 80287 clock is fixed at the low speed CPU clock.

### 2.2.1 PROCLK

The CLK16 and CLKHS input clocks to the FE3001 are used to create the low speed and high speed clocks to the CPU. The CLKHS input is used when the high speed CPU clock is selected. If the CLK16 input is connected to an oscillator, it will be used when the low speed CPU clock is selected (typically from 6 to 8 MHz CPU speed). Alternatively, if CLK16 is tied high through a pullup resistor, then CLKHS ÷ 2 will be used as the low speed clock, saving an oscillator.

The CPU clock circuitry ensures a glitchless speed switch. PROCLK will be held high at most 1 1/2 clock periods of the clock being selected in order to achieve synchronization. Since SYSCLK and DMACLK are based on PROCLK, they will also switch speeds without glitches.

### 2.2.2 DMACLK

DMACLK can be software selected between standard speed and a special high speed mode. Standard speed provides a 4 MHz DMA clock to the DMA controller on a 16 MHz system, the same as an 8 MHz IBM PC/AT. This will be the most common selection of DMA speed. Selecting high speed DMA runs the DMA controller at twice standard speed. This would likely be confined to special dedicated systems where only well defined DMA peripherals that can run that fast are used.

DMACLK is PROCLK ÷ 4 when the low speed CPU clock is selected. DMACLK is PROCLK ÷ 8 when the high speed CPU clock is selected. DMACLK will always change on CPU "t" state boundaries, but no other synchronization is attempted. The previous discussion applies to standard speed DMA. If high speed DMA is selected, it runs twice as fast in all cases.

### 2.2.3 CLK287

CLK287 is always the same as the low speed CPU clock. It is not affected by speed switching. It follows CLK16 if that input is toggling or is CLKHS ÷ 2 if CLK16 is pulled high.

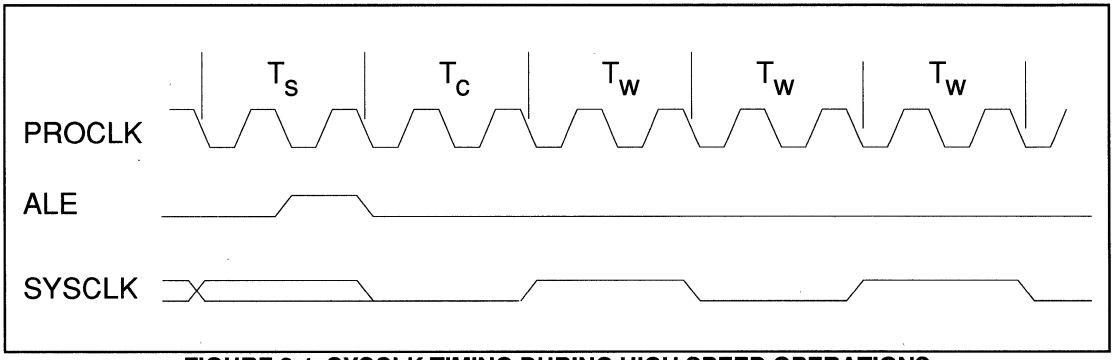



**FIGURE 2-1. SYSCLK TIMING DURING HIGH SPEED OPERATIONS**

### 2.2.4 SYSCLK

When the low speed clock is selected, SYSCLK is PROCLK ÷ 2. During high speed operation, SYSCLK is PROCLK ÷ 4. In the high speed case, SYSCLK is brought into sync with the PC/AT bus at the end of ALE. See Figure 2-1 for SYSCLK functional timing.

### 2.2.5 EADR0/PCLK, $\overline{\text{PCLK}}$, and TMRCLK

The CLK14 input is used to generate EADR0/PCLK, $\overline{\text{PCLK}}$, and TMRCLK. It must be 14.31818 MHz in order for TMRCLK to be 1.1932 MHz, as required for the timers in the FE3010 to be AT compatible. TMRCLK is CLK14 ÷ 12. EADR0/PCLK is CLK14 ÷ 2 (7.16 MHz). $\overline{\text{PCLK}}$ is the complement of EADR0/PCLK. EADR0/PCLK and $\overline{\text{PCLK}}$ can be used to drive the 8042 keyboard controller.

### 2.2.6 STOPPING THE CLOCKS (SLEEP MODE)

Software may put the FE3001 in sleep mode by setting port 063H bit 6. In sleep mode, PROCLK and DMACLK will be stopped at a high level. SYSCLK will also be stopped, but at an indeterminate logic level. DMACLK and PROCLK will each stop on their first rising edge after HLDA is seen active by the FE3001. Typically, this would be the first refresh cycle after the sleep bit is written. SYSCLK will stop with PROCLK.

By stopping these clocks, power can be conserved in battery operated systems. Note that a static CMOS 80286 must be used in order to stop the CPU clock. EADR0/PCLK, $\overline{\text{PCLK}}$, TMRCLK, and CLK287 will continue to run in sleep mode, allowing the keyboard controller, timers, and coprocessor to operate. Either a keyboard interrupt or a system clock interrupt is a likely choice to wake the CPU up.

To restart the clocks (wake up the CPU), the $\overline{\text{RESCPU}}$ input must be pulsed low. The rising edge of $\overline{\text{RESCPU}}$ will kick off internal synchronization that will restart the clocks roughly 2 EADR0/PCLK periods later. No glitches will occur on the clocks as a result of a restart. Also note that the pulse on $\overline{\text{RESCPU}}$ will not reset the CPU if the FE3001 is in sleep mode. Refer to Application Notes for information on external logic needed to implement sleep mode.

## 2.3 COMMAND CONTROL

This module generates the I/O read and write commands, memory read and write commands, interrupt acknowledge, ALE and BALE from $\overline{\text{S1}}$, $\overline{\text{S0}}$, and MNIO. It also controls the number of wait states used during each CPU cycle. See the register descriptions for programming information. For recommended program values, refer to Appendix A.

### 2.3.1 ON-BOARD CYCLES

When the $\overline{\text{ONBRD}}$ signal is active, then this cycle is directed toward 16-bit, high speed local DRAM, BIOS, or I/O. The timing for these cycles is defined by registers R9, R10, and R12. The AT bus timing signals $\overline{\text{MEMCS16}}$ and $\overline{\text{IOCS16}}$ have no effect. IOCHRDY can be used to lengthen the cycle, and indeed is used by the FE3021 to add wait states for a DRAM page miss or EMS cycles.

The wait states for on-board reads and writes are individually programmable by registers R9 and R10 in order to optimize DRAM access speed. Both memory and I/O cycles use these values.

The command delay for on-board I/O cycles is set by register R12. The command delay for on-board memory cycles is always zero.

### 2.3.2 AT BUS CYCLES

All I/O and memory cycles where ONBRD is inactive will be directed to the AT bus. The command delay and wait states are programmable for each type of AT bus cycle. Refer to section 3 for more details.

Memory cycles use 16-bit timing when MEMCS16 is driven low before either the memory command (YMEMR or YMEMW) is programmed to go active or BALE falls, whichever is earlier. I/O cycles use 16-bit timing when IOCS16 is driven low before the I/O command (YIOR or YIOW) is programmed to go active. Otherwise, all cycles use 8-bit timing.

ZEROWS can be driven low for either 8-bit or 16-bit cycles to terminate the cycle early. As on the AT, it should not be driven until a command is active. It will cause the cycle to end after the prescribed minimum number of wait states in register R8 is met. Note that the FE3001 contains circuitry to ensure that an AT bus cycle will end (command goes high) on a rising edge of SYSCLK and will add a wait state if needed to enforce this. This synchronization circuitry will override register programming and the IOCHRDY and ZEROWS inputs.

### 2.3.3 OTHER CYCLES

Interrupt acknowledge cycles follow the same command timing as an 8-bit AT bus cycle. HALT cycles do not generate ALE, BALE or cause the READY output to go high. Effectively, the FE3001A does not respond to a HALT cycle. A SHUTDOWN cycle is handled like a HALT, except that it causes the CPURES line to be pulsed, resetting the CPU only.

## 2.4 BUS CONTROL

This module generates the data buffer controls for CPU, DMA, and refresh cycles. DEN0 and DEN1 are used to enable the lower and upper bytes of the FE3031 AT Bus data buffers, respectively. DTR sets the direction of these buffers. SDEN and SDTR control the enable and direction of a buffer which transfers data between the upper and lower bytes of the AT data bus. The rising edge of SCYCLE latches data on the lower byte of the AT bus into the FE3031, needed for 16-bit to 8-bit bus conversion cycles. ONBRDL is ONBRD latched by ALE to keep it valid throughout the cycle.

The ONBRD signal is used to indicate on-board DRAM and I/O operations. On-board memory and fast on-board I/O devices are assumed to be 16 bit devices. During CPU cycles which access on-board memory, the AT data buffers will be disabled. For Bus Master and DMA cycles, ONBRD must be decoded only for on-board memory.

## 2.5 A0/BHE GENERATOR

This module generates the system ADR0, ABHE, and EBHE using A0 and BHE from the 80286 CPU and AEN and DACK2 from the DMA controller in the FE3010.

### 2.5.1 ADR0

During CPU cycles, A0 from the 80286 is latched with ALE to produce ADR0. For 16 bit DMA transfers and interrupt acknowledge cycles, ADR0 is forced low so that the low byte of the data bus is activated. For all other CPU hold conditions ADR0 is tri-stated. The FE3001 performs two cycles when the CPU attempts a 16 bit operation to an 8-bit device on an even address boundary. ADR0 is automatically forced to one at the start of the second cycle to select the second byte.

### 2.5.2 ABHE

ABHE is the local upper byte select used by the FE3031. During CPU cycles, ABHE is BHE latched with ALE. It is forced low during 16-bit DMA (DACK2 and AEN inputs high) so that the upper byte is always selected. For 8-bit DMA, it is the inversion of ADR0 so that only one byte is selected at a time. During master mode, ABHE follows the EBHE input.

### 2.5.3 EBHE

EBHE is the upper byte select to the AT bus. During CPU cycles, EBHE is ABHE latched with BALE to provide proper AT bus timing. During DMA, EBHE follows ABHE. During refresh the EBHE output is disabled. It is an input during Master Mode transfers.

## 2.6 PRIORITY CONTROL

The Priority Control module generates the hold request signal to the CPU in response to a request from the DMA controller or refresh timer.

### 2.6.1 REFRESH CYCLES

The FE3001 generates a hold request in response to a rising edge on the OUT1 input, sig-

nalling that a refresh cycle is needed. A refresh cycle is initiated when HLDA comes back from the CPU. The FE3001 refresh state machine drives REFRESH low to signal a refresh cycle to the AT bus, and sets ERFSH low to the FE3010 to enable the refresh address onto the CPU address bus. YMEMR will also be strobed low during a refresh cycle. Refer to the timing diagrams for more detail. Note that REFRESH is a bidirectional open-collector signal, and a refresh cycle can be started by an expansion card.

### 2.6.2 DMA CYCLES AND REQUEST ARBITRATION

Requests for control by the DMA controller are made by taking the HRQ1 input high. The FE3001 grants control to the DMA controller by setting HLDA1 high.

When the FE3001 receives a HLDA, it grants control either to the refresh state machine (REFRESH goes low) or to the DMA controller (HLDA1 goes high). Priority is given to the refresh state machine in the event of simultaneous requests. Note that if simultaneous requests do exist, then HOLDRQ will not be dropped after the first request is satisfied. Instead, the FE3001 will grant control sequentially to both requestors with the same HLDA.

## 2.7 DMA CONTROL

This module generates the DMARDY signal for the FE3010 peripheral controller. This signal indicates that the DMA may complete its cycle. The module also generates YMEMR during DMA by delaying the leading (falling) edge of the FE3010 DMAMR signal by one DMA clock.

## 2.8 ERROR CONTROL

This module generates a non-maskable interrupt (NMI) to the 80286 when a parity error or system bus error is encountered. Parity error, system bus error or NMI can be enabled or disabled from software. They are all disabled on system reset.

The PTYERR input is examined each time YMEMR goes high and it is an on-board cycle (ONBRDL low). The state of the PTYERR input is actually latched on the first falling edge of PROCLK after YMEMR goes high. This applies to all on-board reads including CPU, DMA, and Bus Master cycles. If PTYERR was high, it signals a parity failure and will generate an NMI to the CPU if enabled. The parity error latch can be cleared by disabling and then enabling parity errors.

The IOCHCK input is driven low by a device on the AT bus to signal a catastrophic error, such as a parity error on a plug-in RAM card. A low on the IOCHCK input will generate an NMI to the CPU if enabled. The error condition can be cleared by disabling and then enabling IOCHCK. However, the IOCHCK input must also be reset high or it will generate another NMI.

When the CPU receives an NMI, it can interrogate I/O register 061H (PORT B) to determine whether a parity error or an IOCHCK is the source of the interrupt. Note that this is the only time the FE3001 will drive the data bus. All other I/O locations are write only. Also, only bits 6 and 7 will be driven during the read. The FE3010 will supply the 6 lower order bits.

## 2.9 COPROCESSOR INTERFACE

The Coprocessor Interface module provides the system interface to the 80287 Numeric Processor Extension. The reset and chip select to the 80287 are generated in this module in addition to the busy signal to the CPU and interrupt request 13 to the interrupt controller.

In a FE3600 system, as in any PC/AT compatible system, ERROR from the 80287 coprocessor is not connected to the ERROR input on the 80286. Instead, the ERROR input on the 80286 is tied high, while BUSY and interrupt request 13 are used to flag errors. The FE3001 has a BZ286 output which connects to the BUSY input of the 80286. It also has ERROR and BUSY inputs which hook to those outputs from the 80287.

Normally, BZ286 just follows the BUSY input. However, when ERROR goes low while BUSY is low, IRQ13 will go active to signal the CPU that a coprocessor error has occurred. IRQ13 will stay active until ERROR goes back high. Also, BZ286 will be latched low to prevent another coprocessor instruction from being loaded. BZ286 will stay low until either the 80287 is reset or there is a write to I/O address 0F0H. When either of these occurs, then BZ286 will return to following the BUSY input.

The FE3001 RST287 output connects to the 80287 RESET input. This allows the coprocessor to be reset through software by an I/O write to address 0F1H. It will also be reset when the sys-

| M/$\overline{IO}$ | $\overline{S1}$ | $\overline{S0}$ | TYPE OF BUS CYCLE |
|---|---|---|---|
| 0 | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | I/O Read |
| 0 | 1 | 0 | I/O Write |
| 0 | 1 | 1 | None, not a status cycle |
| 1 | 0 | 0 | Halt (if A1 =1) or Shutdown (if A1 = 0) |
| 1 | 0 | 1 | Memory Read |
| 1 | 1 | 0 | Memory Write |
| 1 | 1 | 1 | None, not a status cycle |

**TABLE 2-1. BUS CYCLES**

tem $\overline{RESET}$ output is active.

The FE3001 expects the $\overline{CS287}$ input to be active for addresses 0E0H-0FFH. This is used to provide the $\overline{NPCS}$ chip select decode output for the 80287. It will be active for addresses 0E8H-0EFH and 0F8H-0FFH when $\overline{INTA}$ is high and M/$\overline{IO}$ from the CPU was low for this cycle.

## 2.10 RESET CONTROL

This module generates the CPURES signal which is used to reset only the 80286 and the $\overline{RESET}$ signal which resets the rest of the system (including the FE3001). The $\overline{RESIN}$ input causes a full system reset when driven low. Both CPURES and $\overline{RESET}$ will go active for as long as $\overline{RESIN}$ is low and for at least 30 PROCLK cycles after $\overline{RESIN}$ goes high.

The $\overline{RESCPU}$ input, when driven low, causes only the CPURES output to go high. $\overline{RESCPU}$ would normally be connected to both the 8042 keyboard controller and the FE3021 (to provide "hot" reset). The CPURES output will stay high for at least 4 DMACLK periods, longer if $\overline{RESCPU}$ remains low. CPURES will also go high for 4 DMACLK periods if the 80286 executes a Shutdown cycle.

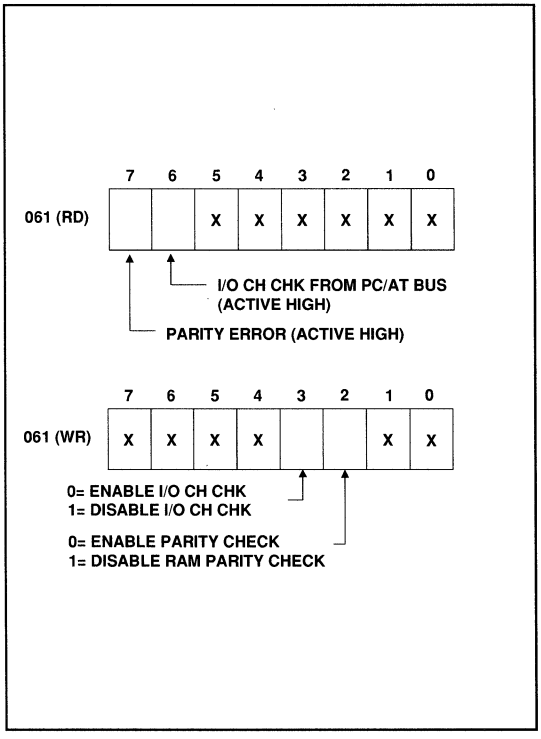
## 2.11 GENERAL NOTES

- *$\overline{ONBRD}$ must not be active during interrupt acknowledge cycles.*
- *For memory cycles with $\overline{ONBRD}$ asserted, the system will use the MDATA bus of the FE3031 for data transfers. For I/O cycles with $\overline{ONBRD}$ asserted, the system will use the expansion bus (DATA) of the FE3031 for data transfers.*
- *On-board I/O devices must drive $\overline{IOCS16}$ in order for a Bus Master to access them as 16-bit devices. Otherwise, $\overline{SDEN}$ will go low for Bus Master I/O cycles where ADR0 is high.*
- *Inputs CLK16, $\overline{BUSY}$, $\overline{ERROR}$, and $\overline{CS287}$ have internal 100k Ω (approx.) pull-up resistors.*

# 3.0 REGISTERS

## 3.1 ERROR CONTROL REGISTER (061H), READ/WRITE

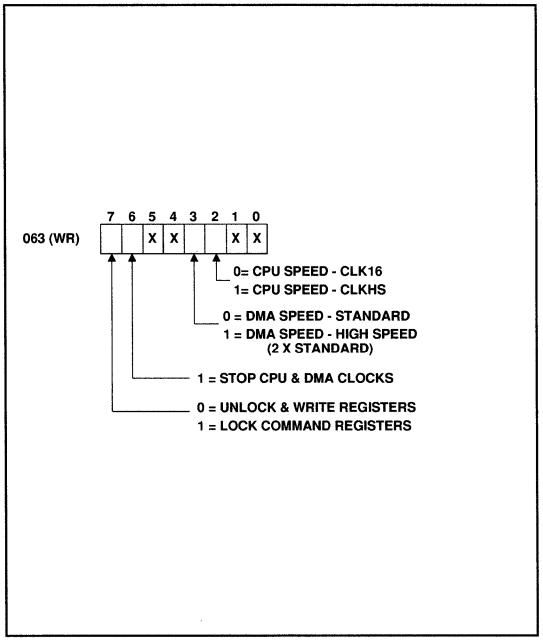
The error control register contains masks for the on-board RAM parity check and I/O channel check signals. It also provides a read port to check the status of these signals.




## 3.2 SPEED SELECT (063H), WRITE

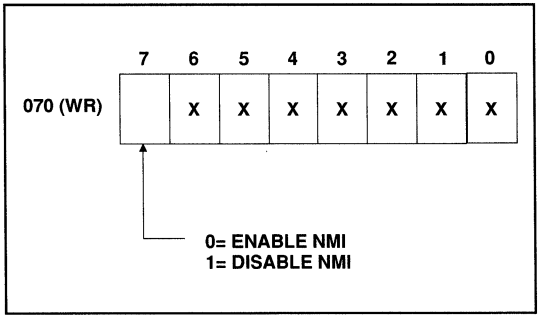
The speed select register controls the speed of the CPU and DMA clocks. This register is also used to stop the CPU (sleep mode) and unlock the command control and speed select registers for access. The lock bit must be reset and D7 must be low to change speed or stop clocks.

The Stop Clock bit stops all the clocks except for the timer clock, coprocessor clock, and keyboard controller clocks. This allows refresh to continue. Bits 2,3, and 6 in the register are cleared and bit 7 is set by system reset.




## 3.3 NMI ENABLE (070H), WRITE

The NMI enable register contains the mask for NMI to the 80286. Bit 7 is set on power-up.



## 3.4 COMMAND CONTROL REGISTERS (072H,073H), WRITE

The timing of the command controls on the expansion bus is programmable via the Command Control Registers. These registers control the timing of BALE, YMEMR, YMEMW, YIOR, YIOW, INTA and the number of wait states in a CPU cycle. This section describes the programming of these registers. Recommended program values for CPU clock speeds of 16, 25, and 32 MHz are provided in Appendix A.

The programmable bus signals are shown in Figure 3-1. A summary of the timing registers is shown in Table 3-1.

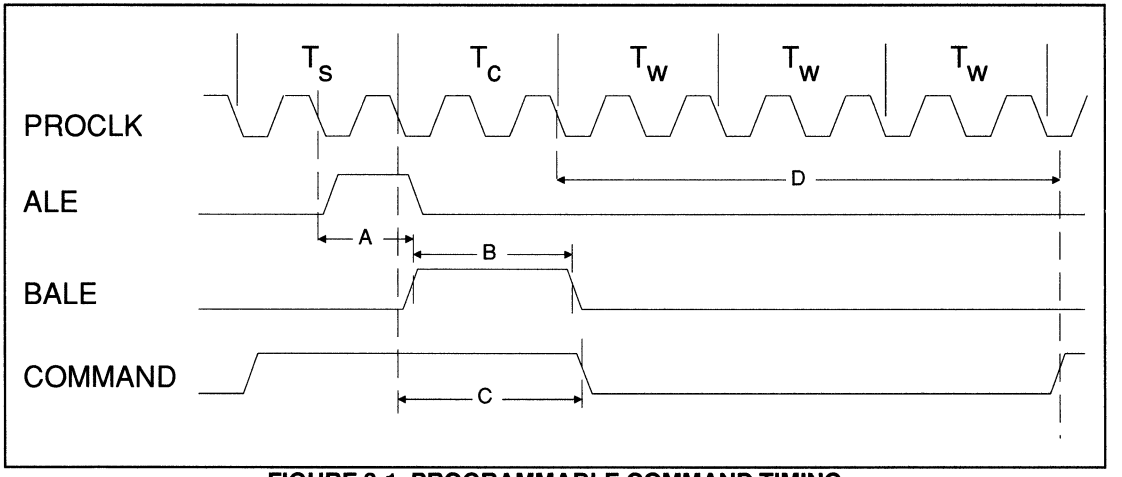



**FIGURE 3-1. PROGRAMMABLE COMMAND TIMING**

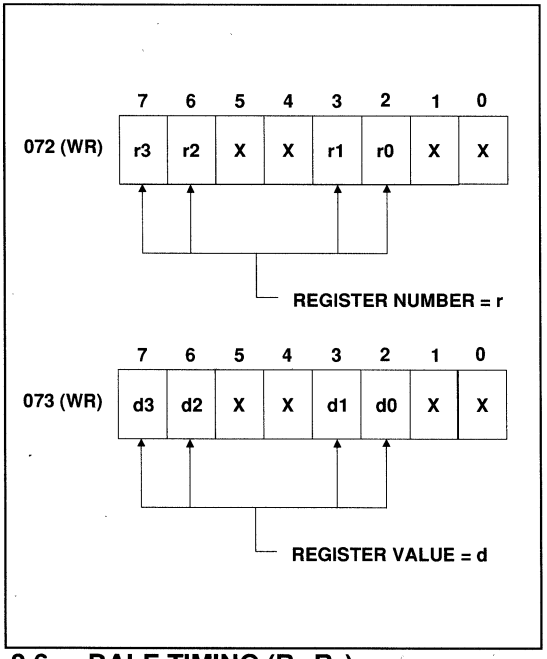
| REG | BITS | FUNCTION | WAVEFORM | DEFAULT | RANGE |
|---|---|---|---|---|---|
| $R_0$ | 2 | BALE delay from ALE leading edge | A | 0 | 0 - 3 |
| $R_1$ | 2 | BALE width | B | 1 | 1 - 3 |
| $R_2$ | | Not used | | | |
| $R_3$ | 4 | 8-bit memory, 8/16-bit I/O - command delay | C | 1 | 0 - 15 |
| $R_4$ | 4 | 8-bit operation - wait states | D | 4 | 0 - 15 |
| $R_5$ | 4 | 16-bit I/O operation - wait states | D | 1 | 0 - 15 |
| $R_6$ | 4 | 16-bit memory operation - command delay | C | 0 | 0 - 15 |
| $R_7$ | 4 | 16-bit memory operation - wait states | D | 1 | 0 - 15 |
| $R_8$ | 4 | Minimum number of wait states when ZEROWS is asserted - wait states | D | 0 | 0 - 15 |
| $R_9$ | 4 | On-board 16-bit read cycle - wait states | D | 1 | 0 - 15 |
| $R_{10}$ | 4 | On-board 16-bit write cycle - wait states | D | 1 | 0 - 15 |
| $R_{11}$ | | Not used | | | |
| $R_{12}$ | 4 | On-Board I/O operation - command delay | C | 1 | 0 - 15 |

**TABLE 3-1. SUMMARY OF COMMAND TIMING REGISTERS**

- *Command delay is number of PROCLKs from end of $T_S$*
- *Each wait state is two PROCLKs.*
- *One wait state may be added in high speed mode for synchronization.*

## 3.5 COMMAND REGISTER POINTER (072H)

The Command Register Pointer points to one of 11 registers at location 073H. Each register contains a command timing parameter based on the selected CPU clock. Whichever register number is loaded in bits 7,6,3, and 2 in location 072H is the register which is loaded with the next write to address 073H. Refer to Table 3 -1 for details.




## 3.6 BALE TIMING ($R_0$,$R_1$)

The leading edge and width of BALE are controlled by these two registers. BALE delay is defined as the number of PROCLK cycles from the leading edge of ALE. BALE width is the width in PROCLK cycles.

Default values: Delay ($R_0$) - 0
Width ($R_1$) - 1

## 3.7 8-BIT MEMORY AND 8/16-BIT I/O COMMAND DELAY ($R_3$)

This register controls the command delay for 8-bit memory and 8/16-bit I/O operations. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE to the start of the command.

Default value: Command Delay ($R_3$) - 1

## 3.8 8-BIT MEMORY AND I/O WAIT STATES ($R_4$)

This register controls the number of wait states for 8-bit operations. The number of wait states is the number of CPU wait states required for these operations.

Default value: Wait States ($R_4$) - 4

## 3.9 16-BIT I/O WAIT STATES ($R_5$)

This register controls the number of wait states for 16-bit I/O cycles. These cycles are indicated by the assertion of $\overline{IOCS16}$. The number of wait states is the number of CPU wait states required for this operation.

Default values: Wait States ($R_5$) - 1

## 3.10 16-BIT AT BUS MEMORY TIMING ($R_6$,$R_7$)

These registers control the command delay and number of wait states for 16-bit memory operations. These cycles are indicated by the assertion of $\overline{MEMCS16}$. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states is the number of CPU wait states required for this operation.

Default values: Command Delay ($R_6$) - 0
Wait States ($R_7$) - 1

## 3.11 $\overline{ZER0WS}$ BUS CYCLE WAIT STATES

This register sets the minimum number of wait states which must occur before the assertion of the $\overline{ZER0WS}$ signal can terminate a cycle.

Default values: Wait States, $\overline{ZWS}$ ($R_8$) - 0

## 3.12 ON-BOARD MEMORY TIMING ($R_9$,$R_{10}$)

These two registers control the number of wait states for on-board operations. These cycles are indicated by the assertion of $\overline{ONBRD}$ during CPU cycles. Command delay is zero for all on board memory operations. The number of wait states is the number of CPU wait states required for this operation. There are separate registers to program the number of wait states for read and write operations to give the system designer added flexibility and potential for greater speed.

Default values: Wait States,Read ($R_9$) - 1
Wait States,Write ($R_{10}$) - 1

### 3.13 ON-BOARD I/O TIMING ($R_{12}$)

This register controls the command delay for 16-bit on-board I/O operations. These cycles are indicated by the assertion of $\overline{ONBRD}$ during CPU I/O cycles. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states for on-board I/O is defined by the on-board memory registers described above. Additional wait states can be added by using the IOCHRDY signal.

Default values: Command Delay ($R_{12}$) - 1

### 3.14 CLEAR 80287 BUSY (0F0H), WRITE

When an error signal is received from the 80287, the $\overline{BZ286}$ signal is latched low. The latch is cleared by an OUT instruction to this port. The output data is don't care.

### 3.15 RESET 80287 (0F1H), WRITE

An OUT instruction to this port generates a reset to the 80287.

## 4.0 PACKAGE

The FE3001 is packaged in a 84-pin PLCC.

## 5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (operating): 0° to + 70° C
Storage Temperature: -40° to +125° C
Voltage on any pin to ground: - .5 V to +7 V
Power Dissipation: 400 mW

## 6.0 DC CHARACTERISTICS

Refer to Table 6-1 below.

| SYMBOL | PARAMETER | MIN | MAX | UNIT | TEST CONDITION |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | 0.8 | V | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | V | |
| $I_{OL}$ | LOW V Output Current[1,4] | 4 | | mA | $V_{OL}$= 0.4 V |
| $I_{OH}$ | HIGH V Output Current[1] | -4 | | mA | $V_{OH}$= 2.4 V |
| $I_{OL}$ | LOW V Output Current[2] | 8,20[3] | | mA | $V_{OL}$= 0.4 V |
| $I_{OH}$ | HIGH V Output Current[2] | -8 | | mA | $V_{OH}$= 2.4 V |
| $V_{OHC}$ | PROCLK Out HIGH Volt | 3.8 | | V | $I_{OH}$= -2 mA |
| $V_{DD}$ | Supply Voltage (Any $V_{DD}$) | 4.5 | 5.5 | V | |
| $I_{DD}$ | Supply Current (Total) | | | mA | |

**TABLE 6-1. DC CHARACTERISTICS**

- *1. Output currents are for DMACLK, TMRCLK, PCLK, $\overline{PCLK}$, CLK287, CPURES, ALE, RTCALE, DTR, SDTR, $\overline{DEN0}$, $\overline{DEN1}$, $\overline{SDEN}$, SCYCLE, $\overline{READY}$, DMARDY, $\overline{NPCS}$, RST287, $\overline{BZ286}$, IRQ13, NMI, HOLDRQ, $\overline{ERFSH}$, HLDA1, $\overline{INTA}$, $\overline{DLYWR}$, $\overline{ABHE}$, $\overline{BHE}$, $\overline{ONBRDL}$.*
- *2. Output currents are for $\overline{RESET}$, $\overline{YMEMR}$, $\overline{YMEMW}$, $\overline{YIOR}$, $\overline{YIOW}$, D6, D7, ADR0, SYSCLK, BALE, $\overline{EBHE}$, ACK.*
- *3. Output current for $\overline{REFRESH}$ should be 20 mA at 0.4V. This is an I/O pin which is only driven low in output mode. It is in a tri-state condition otherwise. A 300 ohm pull-up resistor is needed to bring the output high.*
- *4. Output low current for PROCLK.*

## 7.0 TIMING PARAMETERS

($T_a$=0° to 70°C, $V_{DD}$=4.5 to 5.5V,$C_L$=50pf)

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T1 | ALE rising edge delay from PROCLK | | 12 |
| T2 | ALE falling edge delay from PROCLK | | 15 |
| T3 | BALE rising edge delay from PROCLK | | 21 |
| T4 | BALE falling edge delay from PROCLK | | 20 |
| T5 | $\overline{YMEMR}$, $\overline{YMEMW}$ fall delay from PROCLK | | 16 |
| T6 | $\overline{YMEMR}$, $\overline{YMEMW}$ rise delay from PROCLK | | 19 |
| T7 | $\overline{YIOR}$, $\overline{YIOW}$ falling delay from PROCLK | | 20 |
| T8 | $\overline{YIOR}$, $\overline{YIOW}$ rising delay from PROCLK | | 20 |
| T11 | $\overline{READY}$ falling edge delay from PROCLK | | 12 |
| T12 | $\overline{READY}$ rising edge delay from PROCLK | | 16 |
| T13 | DTR fall delay from PROCLK; read cycle | | 20 |
| T16 | $\overline{DEN0}$, $\overline{DEN1}$ rise delay from PROCLK; read cycle | | 18 |
| T17 | $\overline{DEN0}$, $\overline{DEN1}$ low delay from PROCLK; write cycle | | 28 |
| T18 | $\overline{DEN0}$, $\overline{DEN1}$ rise delay from PROCLK; write cycle | | 24 |
| T21 | $\overline{S1}$, $\overline{S0}$ setup time to PROCLK | 13 | |
| T23 | $\overline{ONBRD}$ setup time to PROCLK; memory cycle | 22 | |
| T24 | $\overline{ONBRD}$ setup time to PROCLK; I/O cycle | 32 | |
| T25 | $\overline{MEMCS16}$ setup time to PROCLK | 32 | |
| T26 | $\overline{IOCS16}$ setup time to PROCLK | 35 | |
| T27 | IOCHRDY setup time to PROCLK | 12 | |
| T28 | IOCHRDY hold time from PROCLK | 0 | |
| T30 | $\overline{S1}$, $\overline{S0}$ hold time from PROCLK | 1 | |
| T31 | A0 setup time to PROCLK | 10 | |
| T32 | $\overline{BHE}$ setup time to PROCLK | 2 | |
| T33 | $\overline{BHE}$ hold time from PROCLK | 15 | |
| T34 | A0 hold time from PROCLK | 15 | |
| T35 | $\overline{ABHE}$ delay from PROCLK | | 21 |
| T36 | ADR0 delay from PROCLK | | 20 |
| T37 | $\overline{EBHE}$ delay from PROCLK | | 28 |
| T38 | $\overline{ONBRD}$ hold time from PROCLK | 10 | |

**TABLE 7-1. TIMING PARAMETERS**

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T39 | $\overline{\text{ONBRDL}}$ delay from $\overline{\text{ONBRD}}$ | | 19 |
| T40 | $\overline{\text{ONBRDL}}$ delay from PROCLK | | 24 |
| T41 | CLK14 period | 69 | |
| T42 | CLK14 low time | 27 | |
| T43 | CLK14 high time | 27 | |
| T44 | EADR0 /PCLK rise/fall delay from CLK14 falling | | 29 |
| T45 | $\overline{\text{PCLK}}$ rise/fall delay from CLK14 falling | | 24 |
| T46 | TMRCLK rise/fall delay from CLK14 falling | | 27 |
| T47 | CLKHS period | 31 | |
| T48 | CLKHS high time | 14 | |
| T49 | CLKHS low time | 14 | |
| T50 | PROCLK falling edge delay from CLKHS fall; High speed PROCLK selected | | 20 |
| T51 | PROCLK rising edge delay from CLKHS rising; High speed PROCLK selected | | 16 |
| T52 | PROCLK duty cycle skew (T50 - T51); High speed PROCLK selected. PROCLK low time = T49 - T52 PROCLK high time = T48 + T52 | - 2 | 4 |
| T53 | PROCLK rise/fall delay from CLKHS falling; Low speed PROCLK, CLK16 tied to +5V | | 26 |
| T54 | CLK287 rise/fall delay from CLKHS falling; CLK16 input tied to +5V | | 18 |
| T55 | CLK16 period | 62 | |
| T56 | CLK16 high time | 28 | |
| T57 | CLK16 low time | 28 | |
| T58 | PROCLK rise/fall delay from CLK16 ; low speed PROCLK, CLK16 toggling | | 22 |
| T59 | CLK287 rise/fall delay from CLK16 ; CLK16 toggling | | 18 |
| T60 | SYSCLK rise/fall delay from PROCLK; Low speed PROCLK selected | | 17 |
| T61 | SYSCLK rise/fall delay from PROCLK; High speed PROCLK selected | | 17 |
| T62 | DMACLK rise/fall delay from PROCLK; Divide by 2 | | 30 |
| T63 | DMACLK rise/fall delay from PROCLK; Divide by 4 | | 37 |

**TABLE 7-1. TIMING PARAMETERS, Continued**

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T64 | DMACLK rise/fall delay from PROCLK; Divide by 8 | | 37 |
| T65 | M/$\overline{IO}$ setup time to $\overline{S0}$, $\overline{S1}$ falling edge | 4 | |
| T66 | M/$\overline{IO}$ hold time from PROCLK (end of Ts) | 15 | |
| T67 | DTR rise delay from PROCLK; read cycle | | 24 |
| T68 | SDTR rise delay from PROCLK | | 24 |
| T69 | SDTR fall delay from PROCLK | | 30 |
| T70 | PTYERR setup time to PROCLK | 11 | |
| T71 | PTYERR hold time from PROCLK | 4 | |
| T72 | $\overline{MEMCS16}$ hold time from PROCLK | 17 | |
| T73 | $\overline{DEN0}$ low delay from PROCLK; read cycle | | 27 |
| T74 | $\overline{DEN1}$ low delay from PROCLK; read cycle | | 25 |
| T75 | $\overline{ZER0WS}$ setup time to PROCLK | 24 | |
| T76 | $\overline{ZER0WS}$ hold time from PROCLK | 0 | |
| T77 | $\overline{DEN0}$, $\overline{DEN1}$ low delay from $\overline{ONBRD}$ high; write cycle | | 28 |
| T78 | $\overline{IOCS16}$ hold time from PROCLK | 5 | |
| T79 | $\overline{DLYWR}$ falling edge delay from PROCLK | | 13 |
| T80 | $\overline{DLYWR}$ rising edge delay from PROCLK | | 23 |
| T81 | $\overline{SDEN}$ falling edge delay from PROCLK | | 30 |
| T82 | $\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YMEMR}$, $\overline{YMEMW}$, or $\overline{YIOR}$ active | | 32 |
| T83 | $\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YIOW}$ active | | 16 |
| T84 | SCYCLE rising edge delay from PROCLK | | 17 |
| T85 | SCYCLE falling edge delay from PROCLK | | 22 |
| T86 | $\overline{INTA}$ falling edge delay from PROCLK | | 18 |
| T87 | $\overline{INTA}$ rising edge delay from PROCLK | | 17 |
| T88 | ADR0 low delay from PROCLK; interrupt acknowledge cycle | | 21 |
| T89 | $\overline{DEN0}$ low delay from PROCLK; interrupt acknowledge cycle | | 26 |
| T90 | $\overline{DEN0}$ rise delay from PROCLK; interrupt acknowledge cycle | | 19 |
| T91 | CPURES rising edge delay from PROCLK; shutdown cycle | | 18 |

**TABLE 7-1. TIMING PARAMETERS, Continued**

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T92 | CPURES falling edge delay from PROCLK; shutdown cycle | | 17 |
| T93 | OUT1 setup time to EADR0/PCLK; asynchronous input | 15 | |
| T94 | HOLDRQ rising edge delay from EADR0/PCLK | | 12 |
| T95 | HOLDRQ falling edge delay from EADR0/PCLK | | 14 |
| T96 | HLDA setup time to EADR0/PCLK; asynchronous input | 26 | |
| T97 | $\overline{\text{REFRESH}}$ low delay from HLDA high | | 29 |
| T98 | $\overline{\text{REFRESH}}$ output tristate delay from EADR0/PCLK | | 9 |
| T99 | $\overline{\text{ERFSH}}$ falling edge delay from EADR0/PCLK | | 10 |
| T100 | $\overline{\text{ERFSH}}$ rising edge delay from EADR0/PCLK | | 10 |
| T101 | $\overline{\text{YMEMR}}$ falling edge delay from EADR0/PCLK; refresh cycle | | 10 |
| T102 | $\overline{\text{YMEMR}}$ rising edge delay from EADR0/PCLK; refresh cycle | | 10 |
| T103 | IOCHRDY setup time to EADR0/PCLK | 19 | |
| T104 | HRQ1 setup to EADR0/PCLK; asynchronous input | 18 | |
| T105 | HLDA1 rising edge delay from EADR0/PCLK | | 10 |
| T106 | HLDA1 high delay from HLDA high | | 20 |
| T107 | HLDA1 falling edge delay from EADR0/PCLK | | 11 |
| T108 | BALE high delay from HLDA high | | 18 |
| T109 | BALE low delay from HLDA low | | 19 |
| T110 | ACK high delay from HLDA high | | 16 |
| T111 | ACK high delay from $\overline{\text{MASTER}}$ high | | 16 |
| T112 | ACK low delay from HLDA low | | 16 |
| T113 | ACK low delay from $\overline{\text{MASTER}}$ low | | 16 |
| T114 | $\overline{\text{ONBRD}}$ setup before $\overline{\text{YIOR}}$ falls | 9 | |
| T115 | $\overline{\text{ONBRD}}$ to $\overline{\text{ONBRDL}}$ delay; HLDA high | | 19 |
| T116 | HLDA high to ADR0 float delay | | 20 |
| T117 | HLDA low to ADR0 enable delay | | 20 |
| T118 | ADR0 input to $\overline{\text{ABHE}}$ output delay | | 19 |
| T119 | HLDA high to $\overline{\text{EBHE}}$ float delay | | 23 |
| T120 | HLDA low to $\overline{\text{EBHE}}$ enable delay | | 23 |
| T121 | AEN high to $\overline{\text{EBHE}}$ enable delay | | 23 |
| T122 | AEN low to $\overline{\text{EBHE}}$ float delay | | 22 |
| T123 | ADR0 input to $\overline{\text{EBHE}}$ output delay | | 28 |
| T124 | HLDA1 high to $\overline{\text{BHE}}$ enable delay | | 10 |
| T125 | HLDA1 low to $\overline{\text{BHE}}$ float delay | | 11 |

**TABLE 7-1. TIMING PARAMETERS, Continued**

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T126 | $\overline{EBHE}$ to $\overline{BHE}$ delay | | 11 |
| T127 | HLDA high to $\overline{YIOR}$ float delay | | 21 |
| T128 | HLDA low to $\overline{YIOR}$ enable delay | | 23 |
| T129 | HLDA high to $\overline{YMEMW}$ float delay | | 21 |
| T130 | HLDA low to $\overline{YMEMW}$ enable delay | | 23 |
| T131 | $\overline{YIOR}$ low to $\overline{DEN0}$ low delay | | 20 |
| T132 | $\overline{YIOR}$ high to $\overline{DEN0}$ high delay | | 19 |
| T 133 | $\overline{YIOR}$ low to DTR low delay | | 18 |
| T134 | $\overline{YIOR}$ high to DTR high delay | | 18 |
| T135 | $\overline{YIOR}$ low to SDTR high delay | | 26 |
| T136 | $\overline{YIOR}$ high to SDTR low delay | | 23 |
| T137 | $\overline{ONBRD}$ setup before DMACLK which causes $\overline{YMEMR}$ to go low | 22 | |
| T138 | $\overline{DMAMR}$ setup time to DMACLK | 16 | |
| T139 | $\overline{YMEMR}$ falling edge delay from DMACLK | | 10 |
| T140 | $\overline{DMAMR}$ high to $\overline{YMEMR}$ high delay | | 19 |
| T141 | $\overline{DLYWR}$ input low to $\overline{YIOW}$ output low | | 16 |
| T142 | $\overline{DLYWR}$ input high to $\overline{YIOW}$ output high | | 16 |
| T143 | $\overline{YMEMR}$ low to $\overline{DEN1}$ low delay | | 18 |
| T144 | $\overline{YMEMR}$ high to $\overline{DEN1}$ high delay | | 17 |
| T145 | $\overline{YMEMR}$ low to $\overline{SDEN}$ low delay | | 21 |
| T146 | $\overline{YMEMR}$ high to $\overline{SDEN}$ high delay | | 19 |
| T147 | AEN high to ADR0 enable delay; DACK2 high | | 25 |
| T148 | DACK2 low to ADR0 float delay | | 20 |
| T149 | AEN high to $\overline{ABHE}$ low delay; DACK2 high | | 27 |
| T150 | IOCHRDY setup time before DMACLK | 14 | |
| T151 | $\overline{YIOR}$ low to DMARDY low delay | | 17 |
| T152 | $\overline{DMAMR}$ low to DMARDY low delay | | 18 |
| T153 | DMARDY rising edge delay from DMACLK | | 11 |
| T154 | $\overline{YMEMR}$ setup time before PROCLK | 11 | |
| T155 | $\overline{ONBRDL}$ hold time from PROCLK | 2 | |
| T156 | $\overline{EBHE}$ to $\overline{ABHE}$ delay; master mode | | 22 |
| T157 | AEN low to ADR0 float delay; master mode | | 23 |
| T158 | AEN high to $\overline{DLYWR}$ float delay | | 20 |
| T159 | AEN low to $\overline{DLYWR}$ enable delay | | 21 |

**TABLE 7-1. TIMING PARAMETERS, Continued**

| SYMBOL | PARAMETER | 16 MHz MIN | 16 MHz MAX (NS) |
|---|---|---|---|
| T160 | $\overline{\text{ONBRD}}$ setup time before memory command falls; master mode | 18 | |
| T161 | ADR0 setup time before memory command falls; master mode | 6 | |
| T162 | $\overline{\text{EBHE}}$ setup time before memory command falls; master mode | 6 | |
| T163 | DTR low delay from memory command low; master mode | | 17 |
| T164 | DTR high delay from memory command high; master mode | | 17 |
| T165 | $\overline{\text{DEN0}}$ low delay from memory command low; master mode | | 20 |
| T166 | $\overline{\text{DEN0}}$ high delay from memory command high; master mode | | 19 |
| T167 | $\overline{\text{DEN1}}$ low delay from memory command low; master mode | | 19 |
| T168 | $\overline{\text{DEN1}}$ high delay from memory command high; master mode | | 18 |
| T169 | $\overline{\text{MEMCS16}}$ setup time before memory command falls; master mode, ADR0 high | 9 | |
| T170 | SDTR low delay from memory command low; master mode, ADR0 high | | 21 |
| T171 | SDTR high delay from memory command high; master mode, ADR0 high | | 20 |
| T172 | $\overline{\text{SDEN}}$ low delay from memory command low; master mode, ADR0 high | | 21 |
| T173 | $\overline{\text{SDEN}}$ high delay from memory command high; master mode, ADR0 high | | 20 |
| T174 | ADR0 setup time before I/O command falls; master mode | 5 | |
| T175 | SDTR low delay from I/O command low; master mode, ADR0 high | | 19 |
| T176 | SDTR high delay from I/O command high; master mode, ADR0 high | | 19 |
| T177 | $\overline{\text{SDEN}}$ low delay from I/O command low; master mode, ADR0 high | | 23 |
| T178 | $\overline{\text{SDEN}}$ high delay from I/O command high; master mode, ADR0 high | | 23 |
| T179 | $\overline{\text{IOCS16}}$ setup time before I/O command falls; master mode, ADR0 high | 14 | |

**TABLE 7-1. TIMING PARAMETERS, Continued**

NOTES:

All delays with respect to PROCLK are with respect to the falling edge of PROCLK.

T22:$\overline{\text{ZEROWS}}$ SETUP TIME NOTES

The $\overline{\text{ZEROWS}}$ signal is sampled by the FE3001 in the middle of every CPU wait state during AT bus cycles. $\overline{\text{ZEROWS}}$ will terminate an AT bus cycle early when it is sampled after the minimum number of wait states programmed into R8 have occurred.

T25: $\overline{\text{MEMCS16}}$ SETUP TIME NOTES

$\overline{\text{MEMCS16}}$ is only examined during AT bus memory cycles. It must be valid before the earlier of either (1) the memory command strobe falls as programmed by R6, or (2) BALE falls as programmed by R0 and R1.

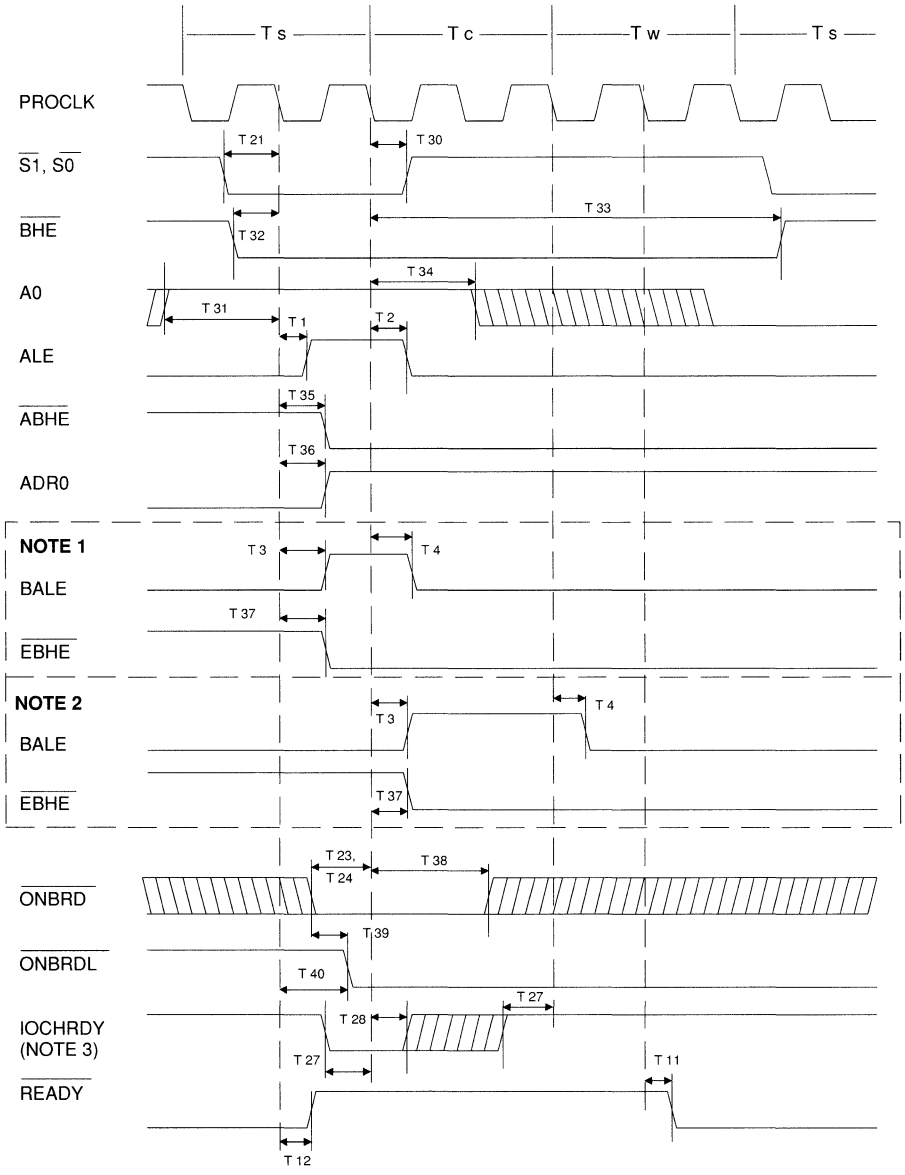
T26: $\overline{\text{IOCS16}}$ SETUP TIME NOTES

$\overline{\text{IOCS16}}$ is only examined during AT bus I/O cycles. It must be valid before the I/O command falls as programmed by R3.

T27: IOCHRDY SETUP TIME NOTES

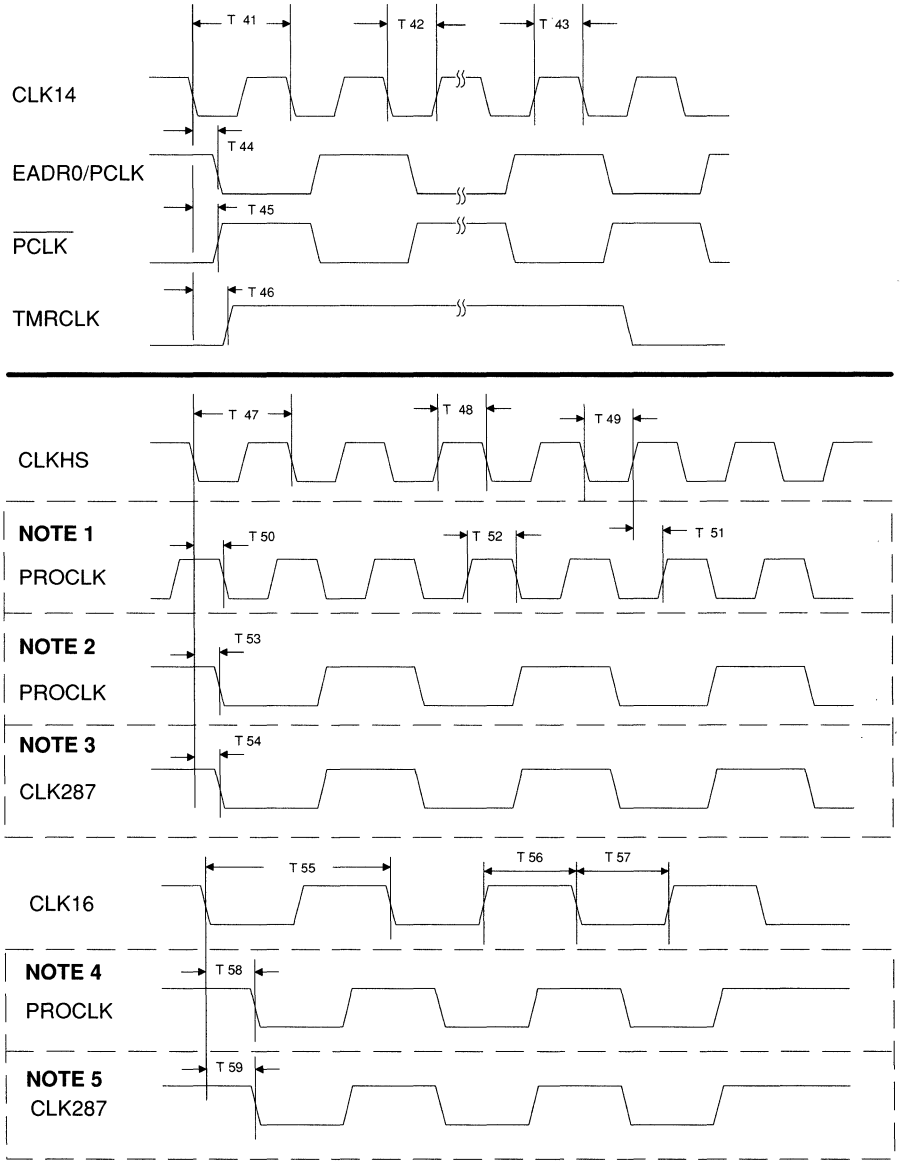
IOCHRDY is sampled with the falling edge of PROCLK at the end of each CPU "t" state. It must be sampled low one full "t" state before a cycle would normally end in order to extend it.





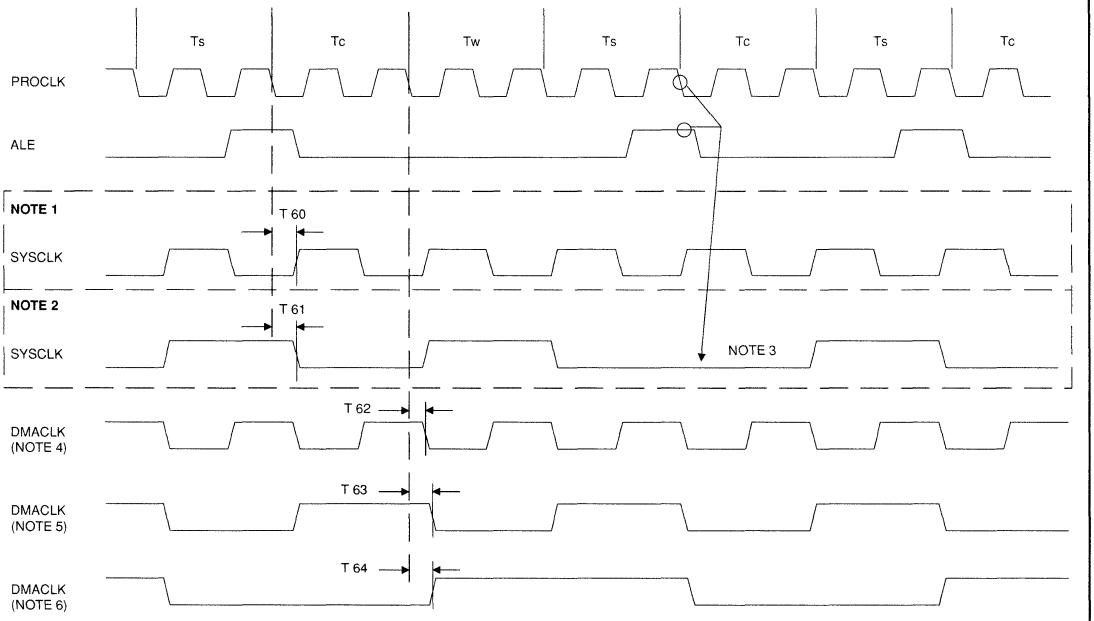

NOTES:
(1) R0 = 0; R1 = 1 (low speed BALE timing)
(2) R0 = 1; R1 = 2 (16MHz BALE timing)
(3) IOCHRDY is being used to add one wait state to this on-board cycle, which is otherwise programmed by R9 or R10 to be 0 wait states

**FIGURE 7-1. CPU CYCLE TIMING FOR ALE, BYTE SELECT, ONBRD and READY**




NOTES:
(1) Bit 2 of I/O Addr 63 set to 1 (High speed CPU clock)
(2) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and CLK16 input connected to +5V
(3) CLK16 input connected to +5V
(4) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and CLK16 input driven by an oscillator
(5) CLK16 input driven by an oscillator

**FIGURE 7-2. CLOCK TIMING (1 of 2)**




NOTES:

(1) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock)

(2) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock)

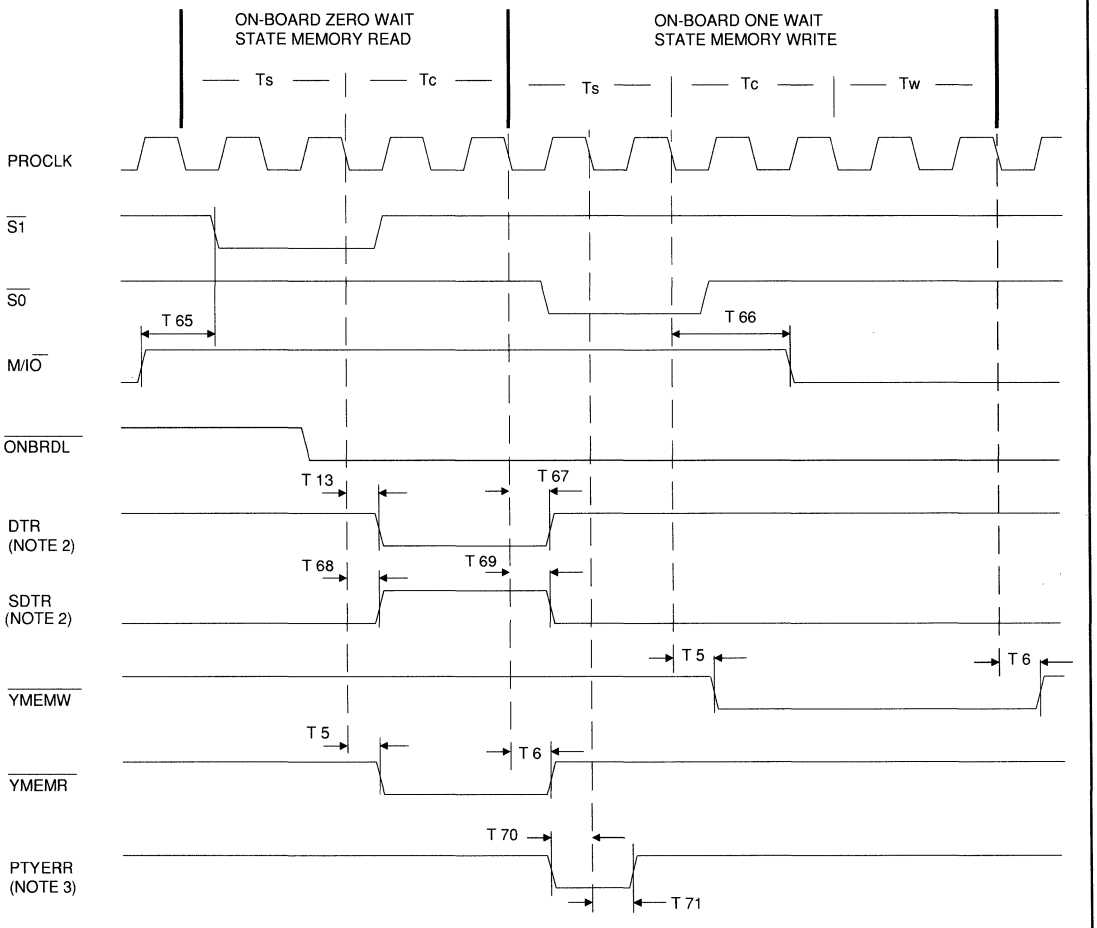
(3) SYSCLK low time extended when SYSCLK is low while ALE is high and the high speed CPU clock has been selected

(4) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and Bit 3 set to 1 (high speed DMA)

(5) I/O Addr 63 Bits 2 and 3 set to the same value; low speed CPU clock and low speed DMA, or high speed CPU clock and high speed DMA

(6) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock) and Bit 3 set to 0 (low speed DMA)

**FIGURE 7-3. CLOCK TIMING (2 of 2)**



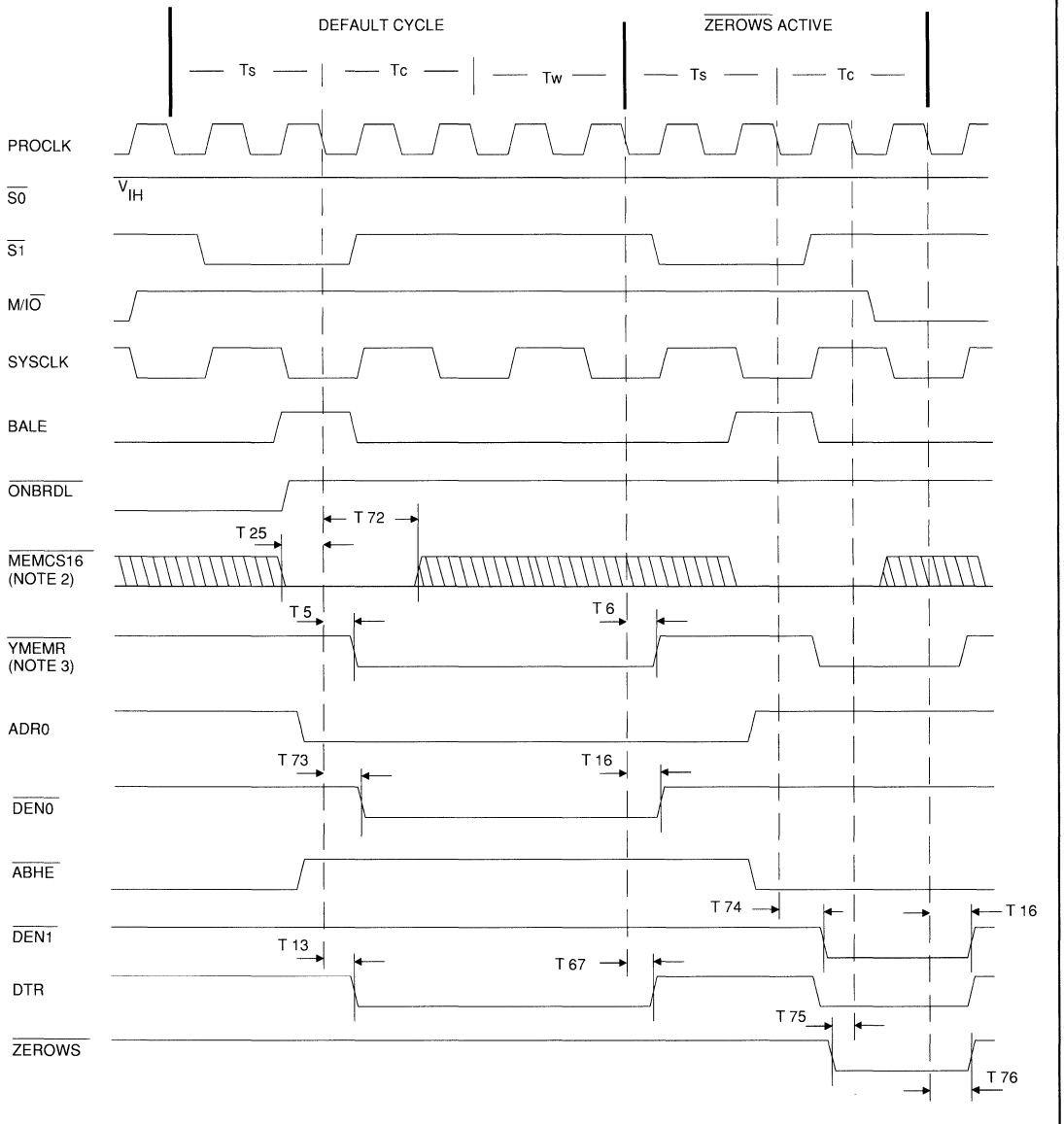

NOTES:

(1) $\overline{DEN0}$, $\overline{DEN1}$, and $\overline{SDEN}$ will remain high and SYSCLE will remain low during on-board memory cycles

(2) NOT USED by the FE3031 during on-board memory cycles; shown for reference only

(3) PTYERR must be low when shown to prevent a parity NMI from being generated (if enabled). PTYERR is sampled one PROCLK ***after*** the end of an on-board memory read

**FIGURE 7-4. ON-BOARD MEMORY CYCLE TIMING**



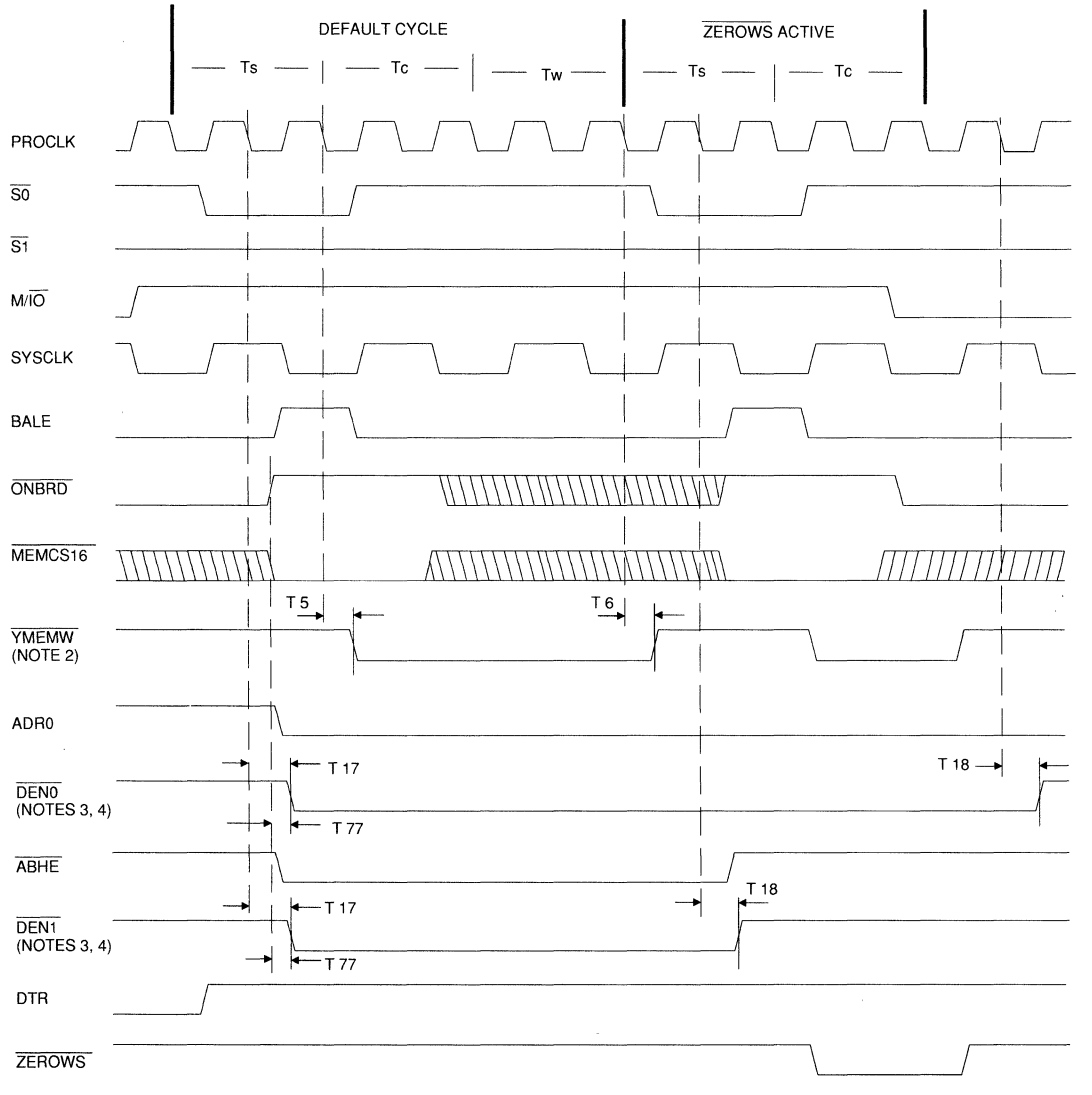

NOTES:

(1) NPCS is high during these cycles

(2) Setup/Hold times referenced to PROCLK edge which is programmed by R6 to cause YMEMR or YMEMW to go low

(3) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

**FIGURE 7-5. 16-BIT MEMORY READ TIMING FOR LOW SPEED CPU CLOCK**




NOTES:

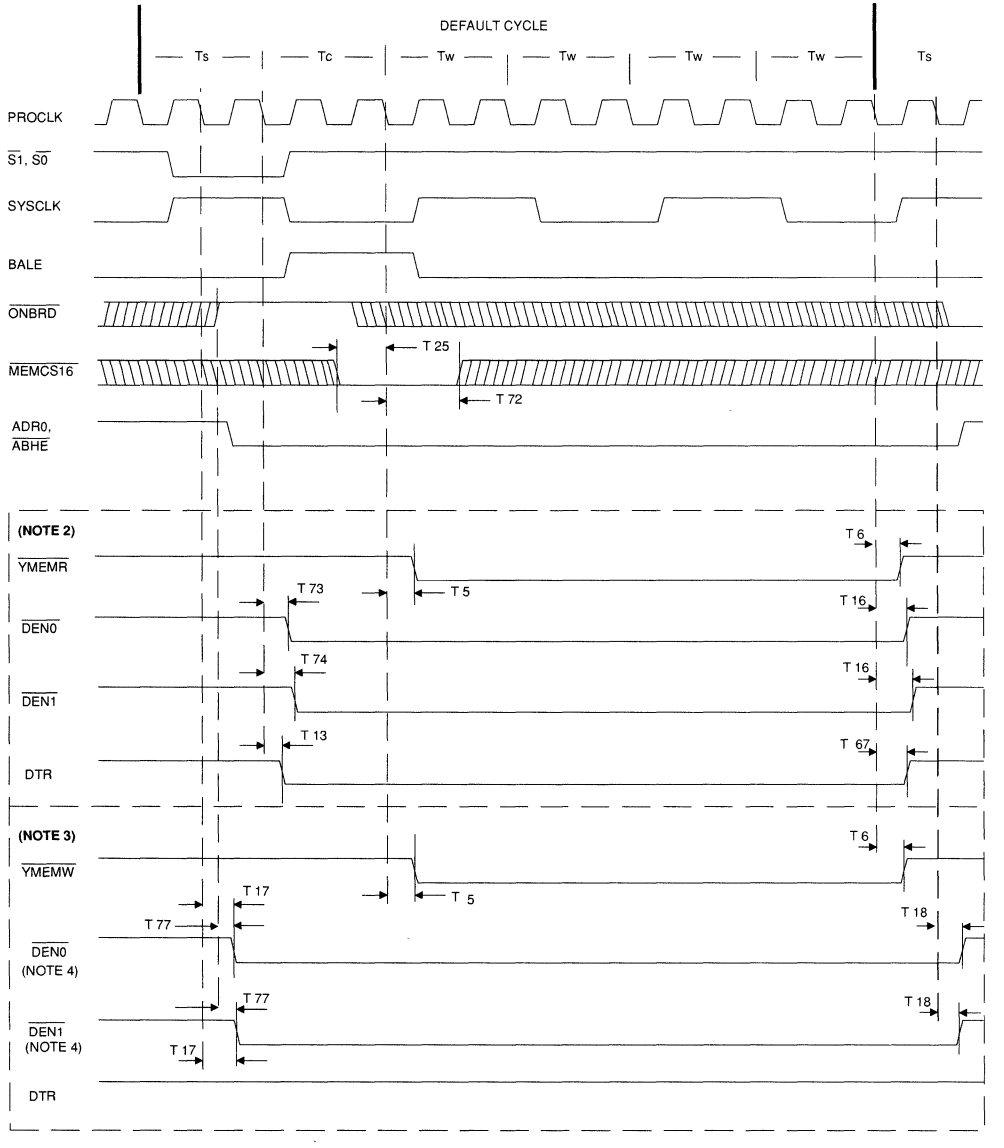
(1) NPCS is high during these cycles

(2) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

(3) DEN0 and DEN1 go high one PROCLK cycle after the write command goes high. However, each will remain low for back to back write cycles when it is active in both cycles.

(4) The falling edge of DEN0 or DEN1 in a write cycle will be controlled by ONBRD if it goes high in the last half of the processor Ts state, or by PROCLK if ONBRD is high earlier.

**FIGURE 7-6. 16-BIT MEMORY WRITE TIMING FOR LOW SPEED CPU CLOCK**




NOTES:

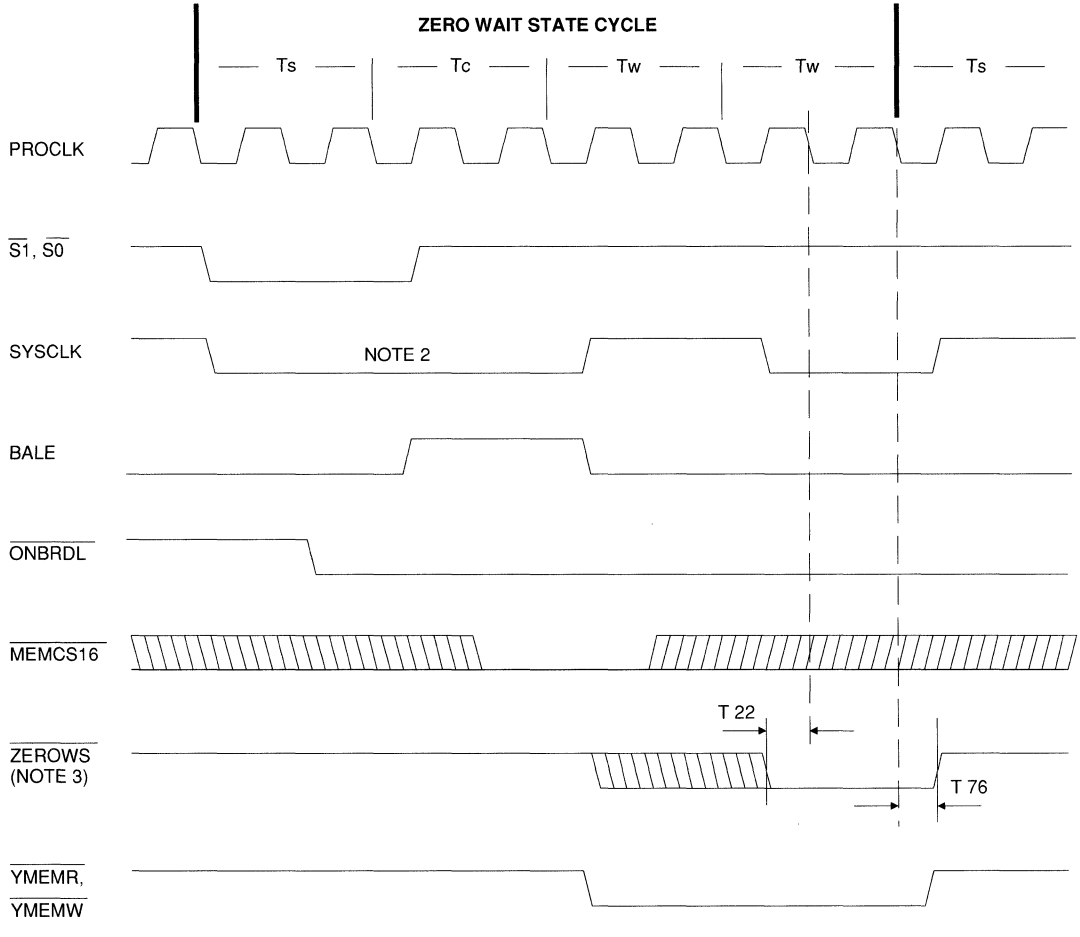
(1) R0 = 1; R1 = 2; R6 = 2; R7 = 4; $\overline{\text{NPCS}}$ is high during these cycles

(2) Memory read cycle timing

(3) Memory write cycle timing

(4) The falling edge of $\overline{\text{DEN0}}$ or $\overline{\text{DEN1}}$ in a write cycle will be controlled by $\overline{\text{ONBRD}}$ if it goes high in the last half of the processor Ts state, or by PROCLK if $\overline{\text{ONBRD}}$ goes high earlier

**FIGURE 7-7. 16-BIT MEMORY TIMING FOR HIGH SPEED (16 MHZ) CPU**



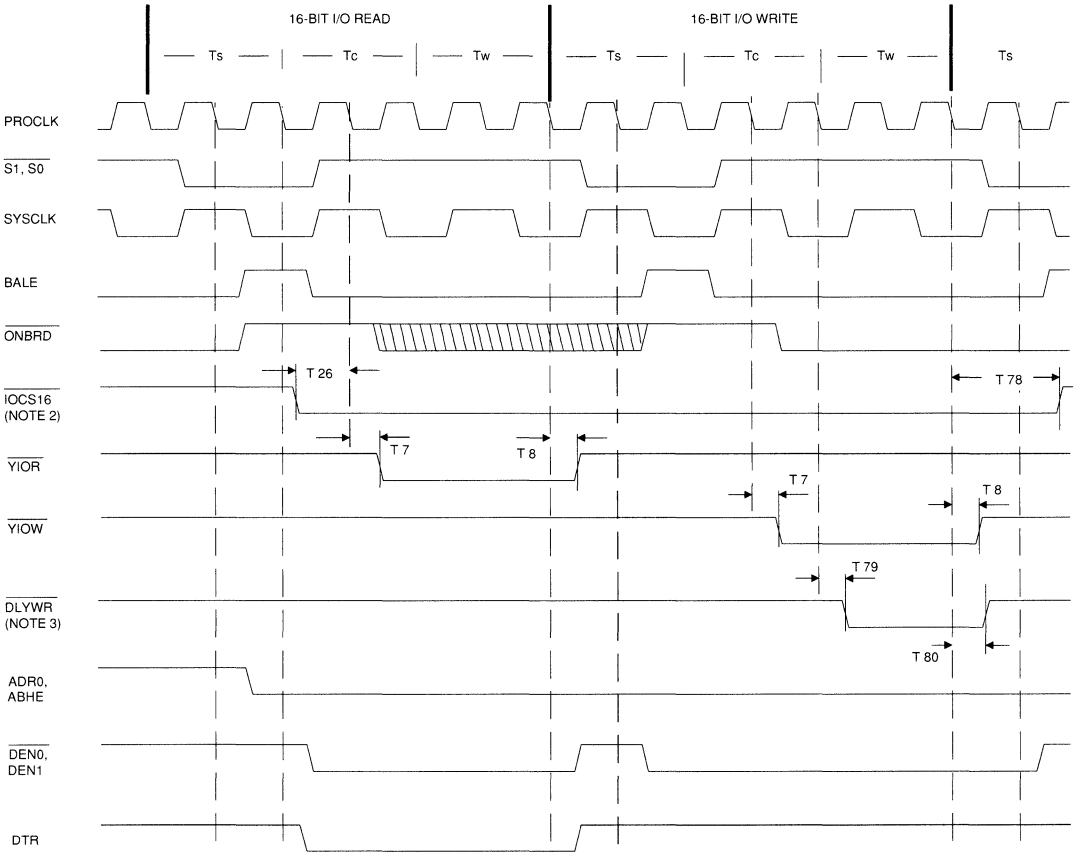

NOTES:

(1) R0 = 1; R1 = 2; R6 = 2; NPCS is high during these cycles

(2) SYSCLK is extended low one extra half period when it is low during the processor's Ts state and the high speed CPU clock is selected

(3) Register R8 = 2. When the high speed CPU clock is selected, no AT bus cycle can terminate until the cycle when SYSCLK goes high. This ensures proper synchronization of the rising edge of the command strobes with SYSCLK

**FIGURE 7-8. 16-BIT MEMORY TIMING WITH ZEROWS ASSERTED AND HIGH SPEED (16 MHz) CPU**



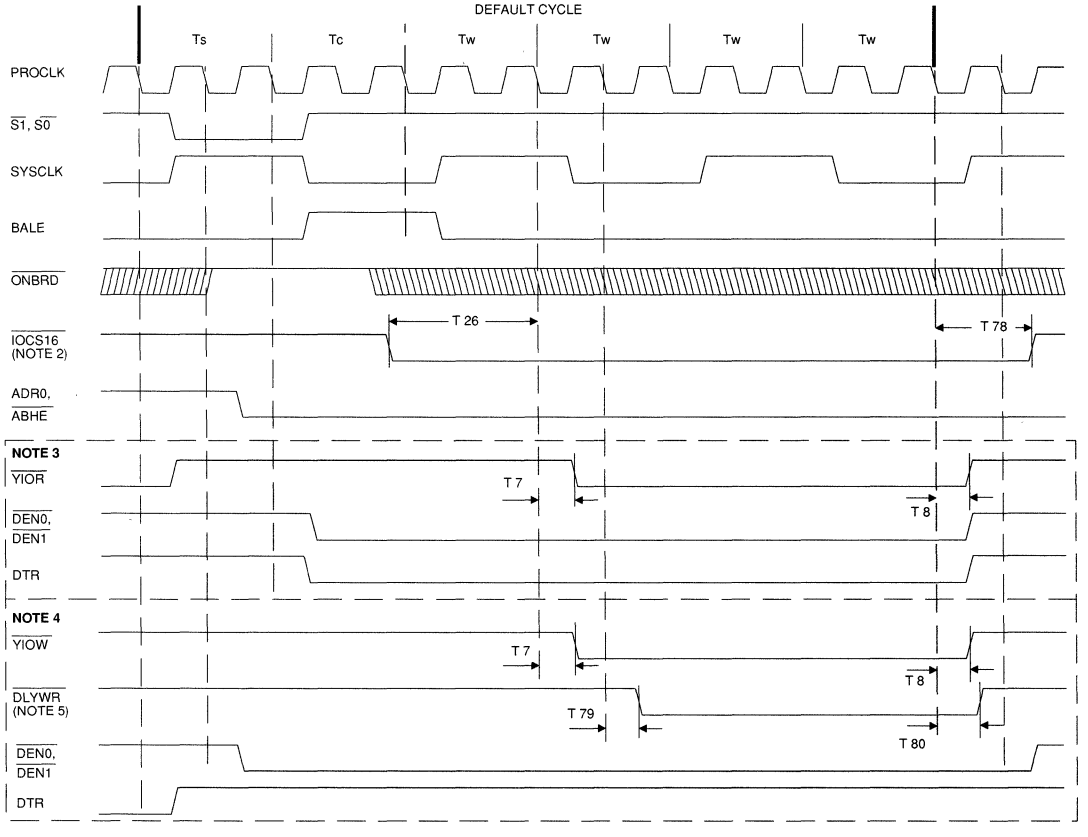

NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R5 = 1

(2) $\overline{\text{IOCS16}}$ setup time is to the PROCLK which causes $\overline{\text{YIOR}}$ or $\overline{\text{YIOW}}$ to go low as pro-. grammed by R3. Hold time is from the end of the cycle

(3) $\overline{\text{DLYWR}}$ falling edge is one PROCLK later than $\overline{\text{YIOW}}$. $\overline{\text{DLYWR}}$ rising edge is coincident with $\overline{\text{YIOW}}$ rising edge

**FIGURE 7-9. 16-BIT I/O TIMING WITH LOW SPEED CPU CLOCK**




NOTES:

(1) R0 = 1; R1 = 2; R3 = 4; R5 = 4. NPCS is high during these cycles

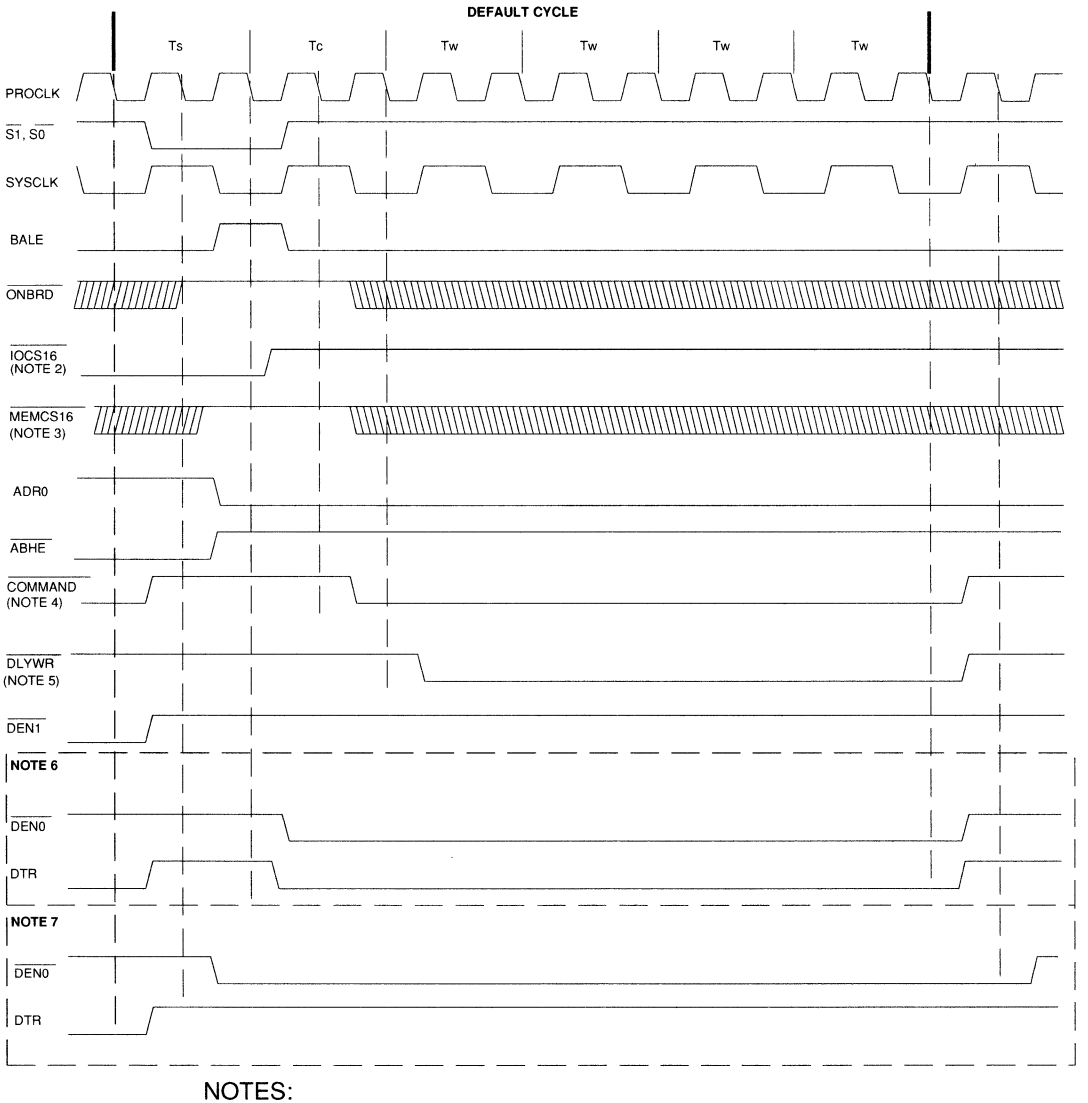
(2) IOCS16 setup time is referenced to the PROCLK which causes IOR or IOW to go low as programmed by R3. Hold time is from the cycle end

(3) I/O read cycle timing

(4) I/O write cycle timing

(5) DLYWR falling edge is one PROCLK later than IOW. DLYWR rising edge is coincident with IOW rising edge

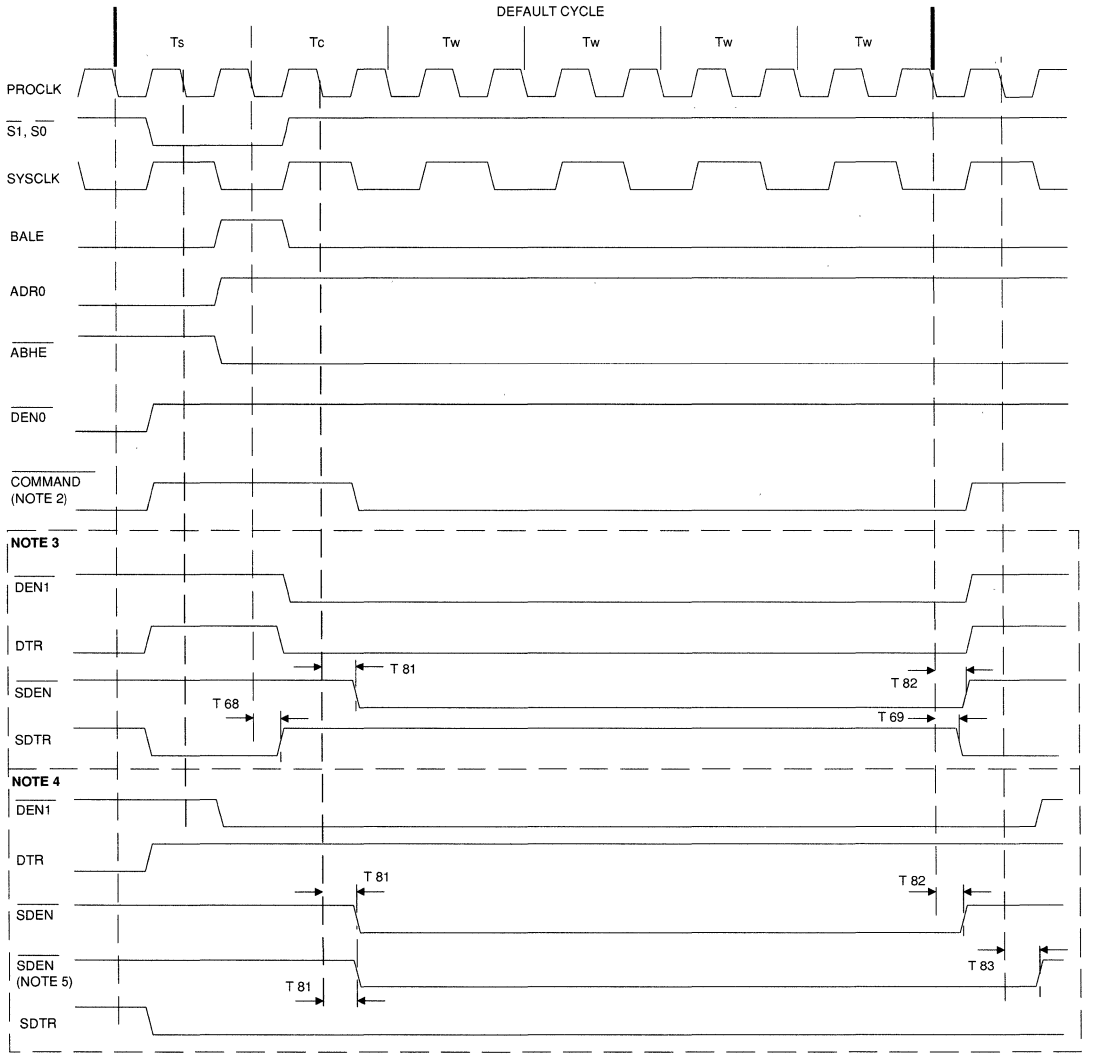
**FIGURE 7-10. 16-BIT I/O TIMING WITH HIGH SPEED (16 MHZ) CPU CLOCK**




NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS is high during this cycle
(2) IOCS16 affects only I/O cycles
(3) MEMCS16 affects only memory cycles
(4) COMMAND means either YIOR, YIOW, YMEMR, or YMEMW
(5) DLYWR is active only in cycles where YIOW is active
(6) Read cycle timing
(7) Write cycle timing

**FIGURE 7-11. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- EVEN BYTE ACCESS**




NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. $\overline{\text{NPCS}}$ and $\overline{\text{ONBRD}}$ are inactive. $\overline{\text{IOCS16}}$ is inactive during I/O cycles. $\overline{\text{MEMCS16}}$ is inactive during memory cycles

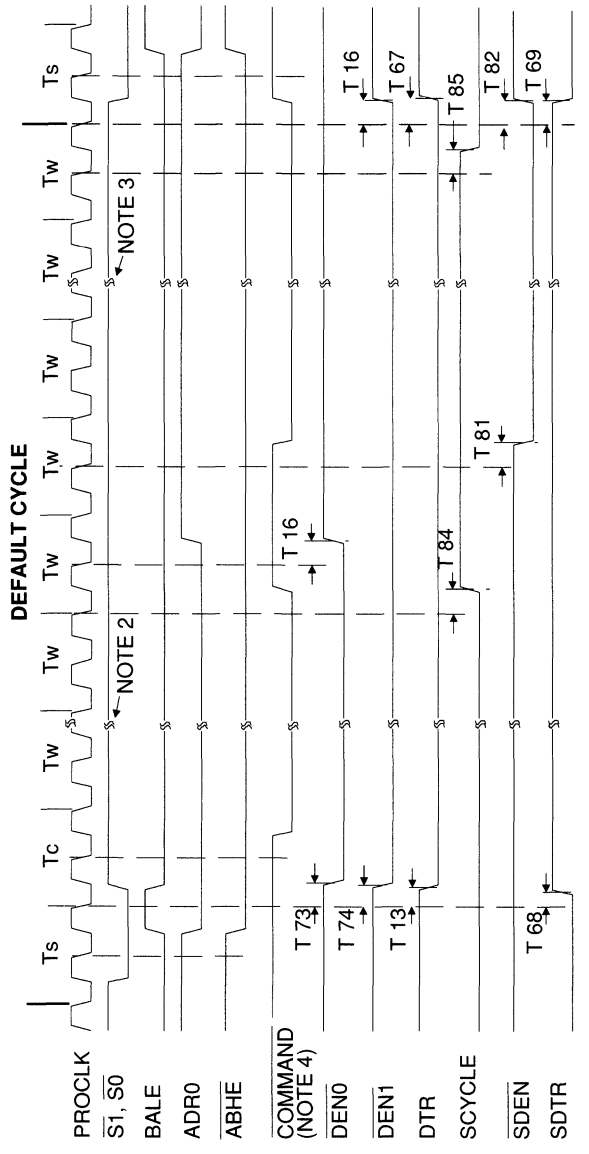
(2) $\overline{\text{COMMAND}}$ means either $\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$, $\overline{\text{YMEMR}}$, or $\overline{\text{YMEMW}}$

(3) Read cycle timing

(4) Write cycle timing

(5) $\overline{\text{SDEN}}$ stays low one additional PROCLK during cycles when $\overline{\text{YIOW}}$ is active

**FIGURE 7-12. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- ODD BYTE ACCESS**




NOTES:

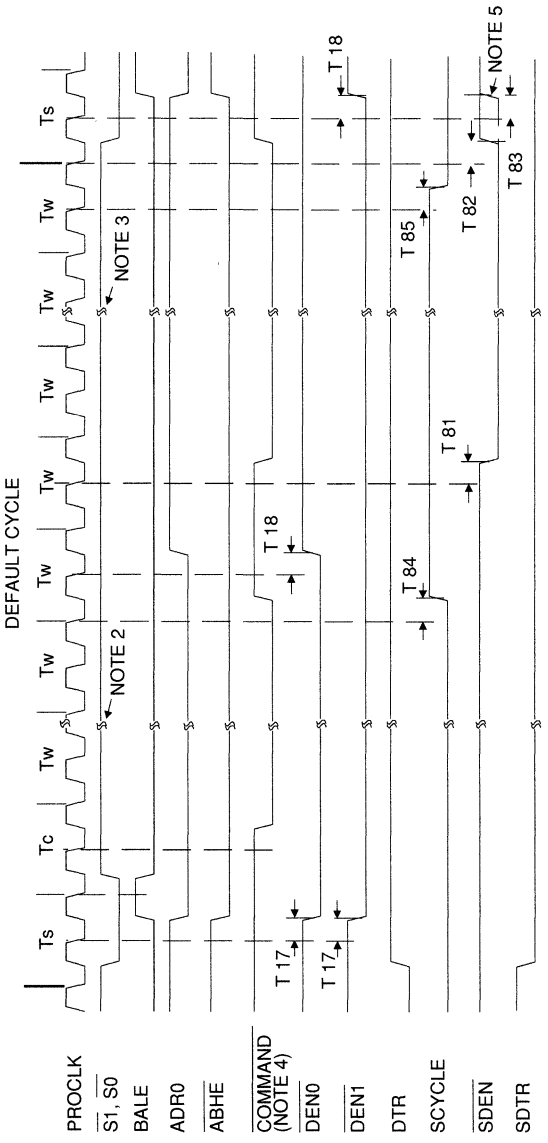
(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) COMMAND means either YIOR or YMEMR

**FIGURE 7-13. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- WORD READ FROM EVEN ADDESS**




NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

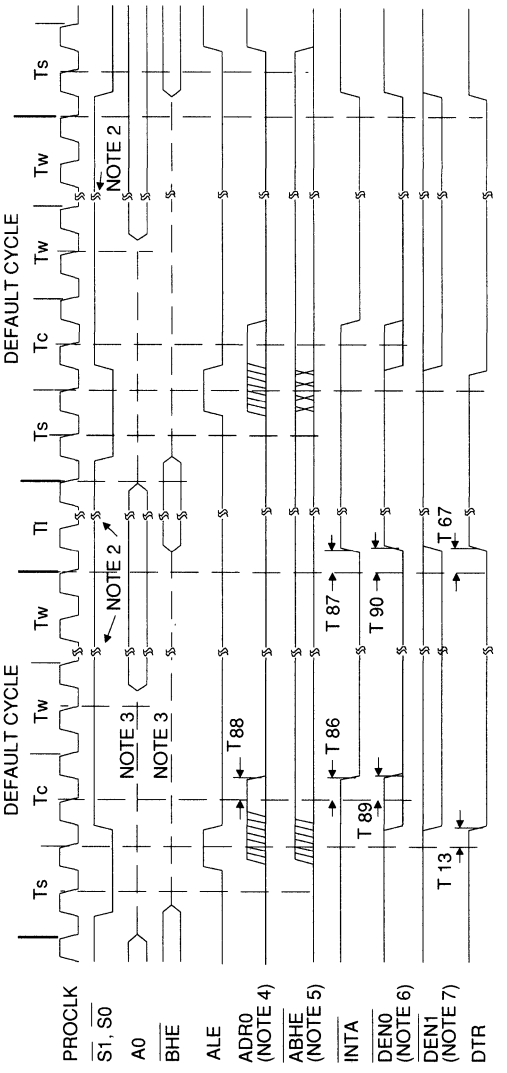
(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) COMMAND means either YIOW or YMEMW

(5) SDEN low time extended one PROCLK for I/O write cycles

**FIGURE 7-14. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- WORD WRITE TO EVEN ACCESS**




NOTES:

(1) R3 = 1; R4 = 4

(2) Two additional processor T states not shown

(3) 80286 floats these lines during interrupt acknowledge cycles

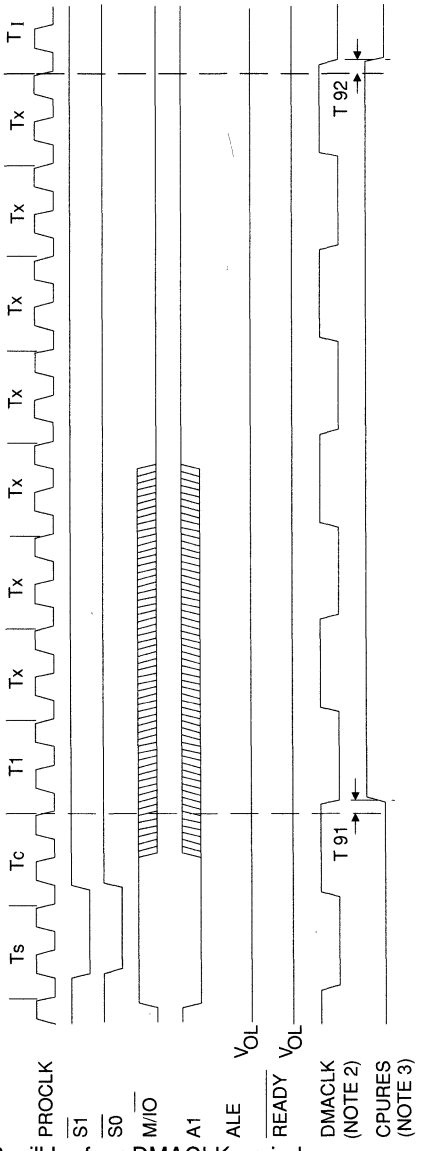
(4) Because A0 is floating, the state of ADR0 is unknown from the rising edge of ALE until INTA falls, when ADR0 is forced low

(5) Because BHE is floating, the state of ABHE (and EBHE ) is unknown

(6) DEN0 is forced low when INTA falls. It could have gone low at the end of Ts depending on the state of ADR0

(7) The state of DEN1 follows ABHE and therefore cannot be determined

**FIGURE 7-15. INTERRUPT ACKNOWLEDGE CYCLE FOR LOW SPEED CPU CLOCK**



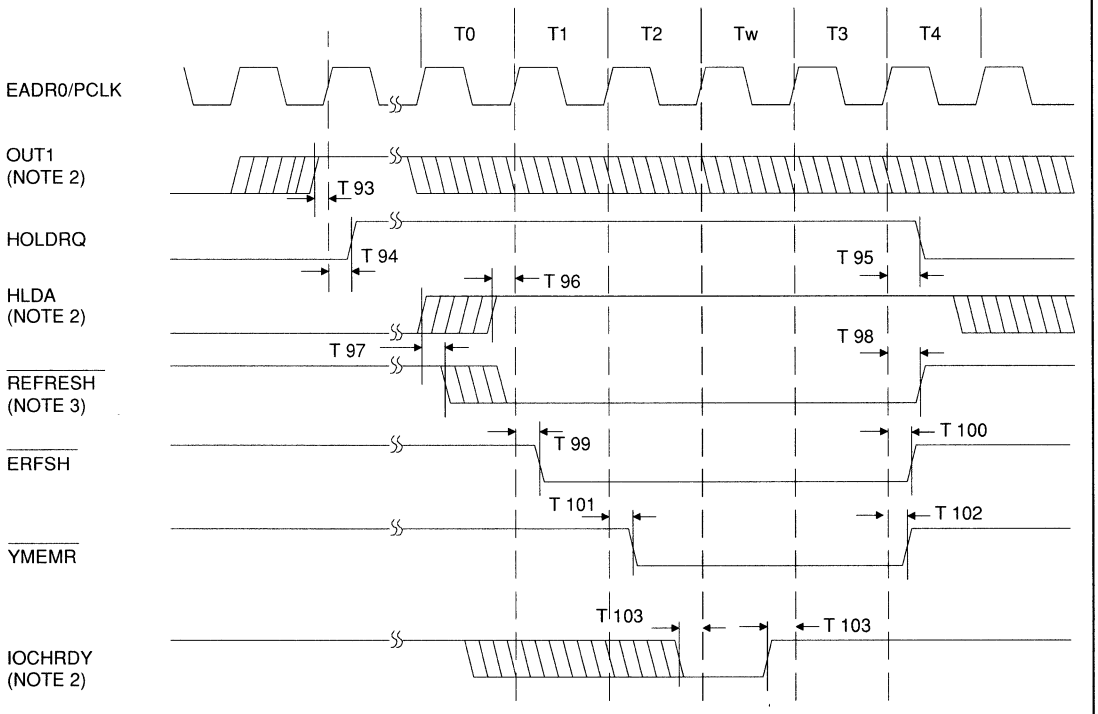

NOTES:

(1) The width of CPURES will be four DMACLK periods

(2) DMACLK is shown as it would be for high speed DMA and a high speed CPU clock or for low speed DMA and a low speed CPU clock. Refer to Figure 8. Note that the phase of DMACLK with respect to Ts is uncertain.

(3) CPURES will be asserted on the first PROCLK edge which begins a T state, after an internal divide by 4 of DMACLK makes a low to high transition. The phase of this internal signal is impossible to determine, although it changes on the rising edge of DMACLK. CPURES is shown going active here as early as possible. It could be delayed up to three more DMACLK periods

**FIGURE 7-16. SHUTDOWN CYCLE TIMING**




NOTES:

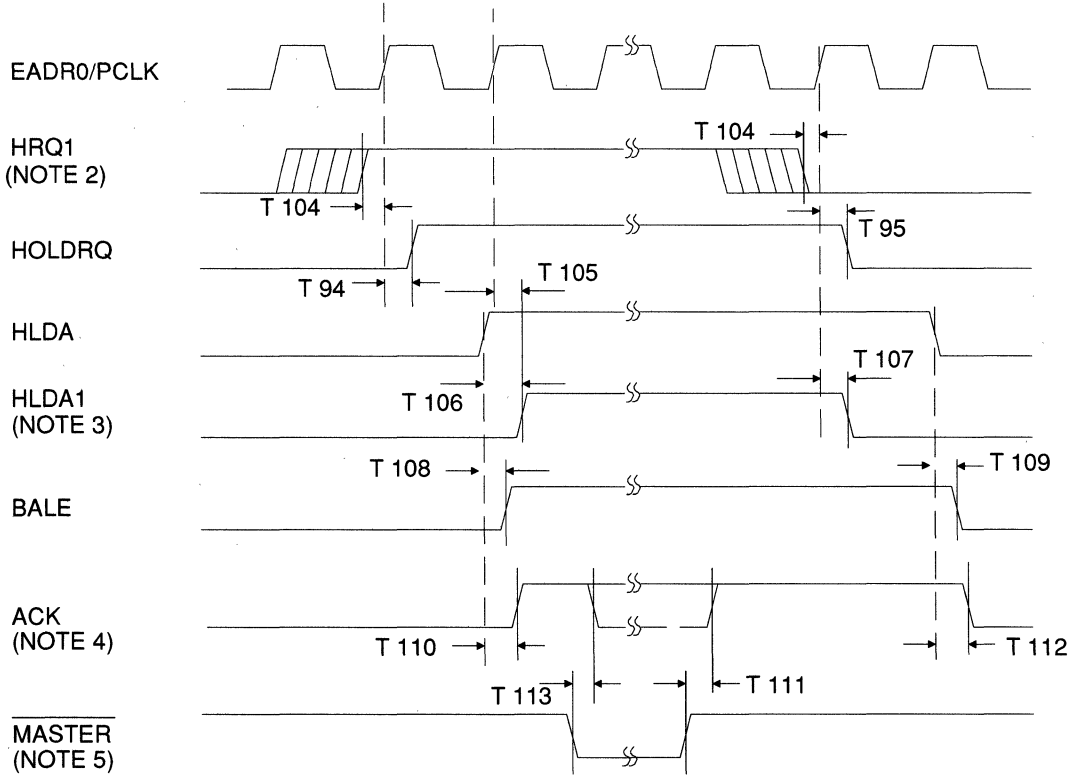
(1) Cycle shown with one wait state (one EADR0/PCLK period) inserted

(2) OUT1, HLDA , and IOCHRDY are asynchronous inputs. Setup times are shown only to guarantee recognition at a particular edge of EADR0/PCLK

(3) The falling edge of REFRESH is combinatorially generated from HLDA. The rising edge is controlled by the FE3001

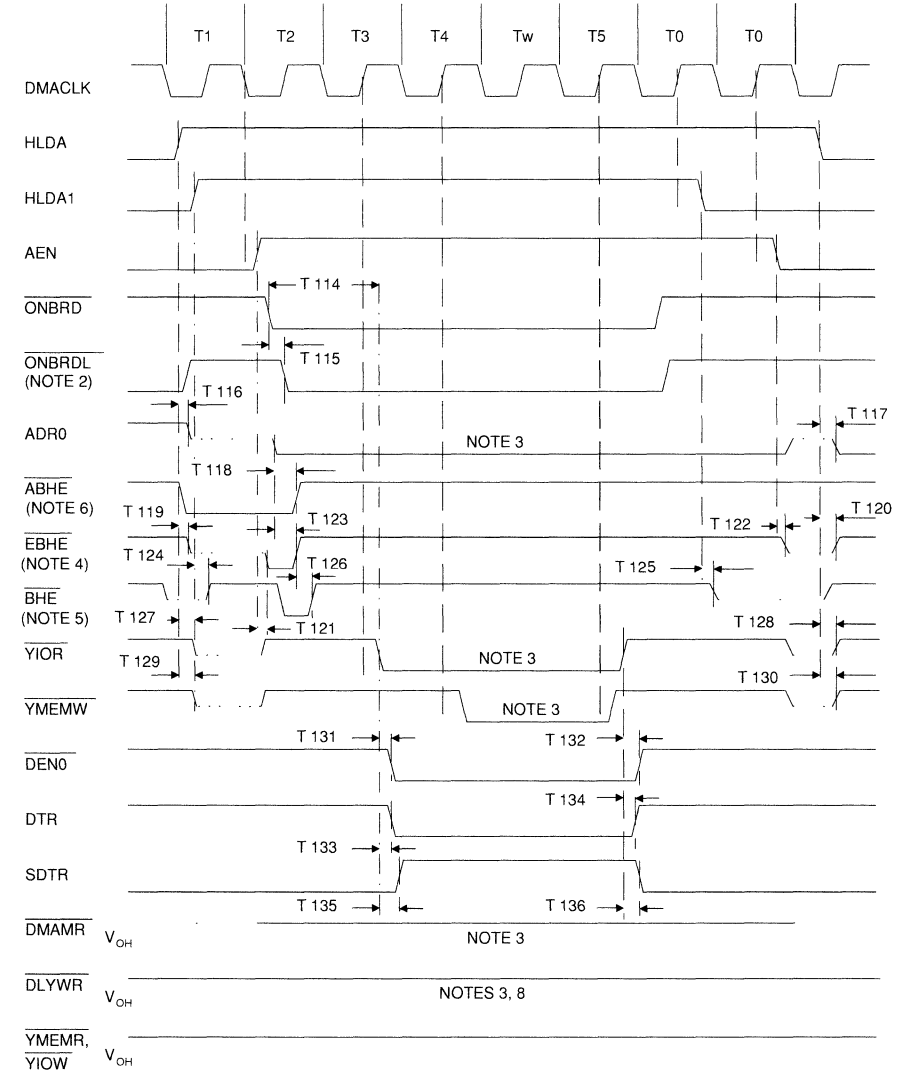
(4) HRQ1 and HLDA1 are not active

**FIGURE 7-17. REFRESH CYCLE TIMING**




NOTES:
(1) No refresh cycle is pending
(2) HRQ1 is an asynchronous input. Setup time is shown only to guarantee recognition at a particular EADR0/PCLK edge
(3) HLDA1 rising edge will be controlled by the later of the EADR0/PCLK edge shown or HLDA
(4) ACK will follow the dashed lines shown only when $\overline{\text{MASTER}}$ is asserted
(5) Applicable for Bus Master cycles only

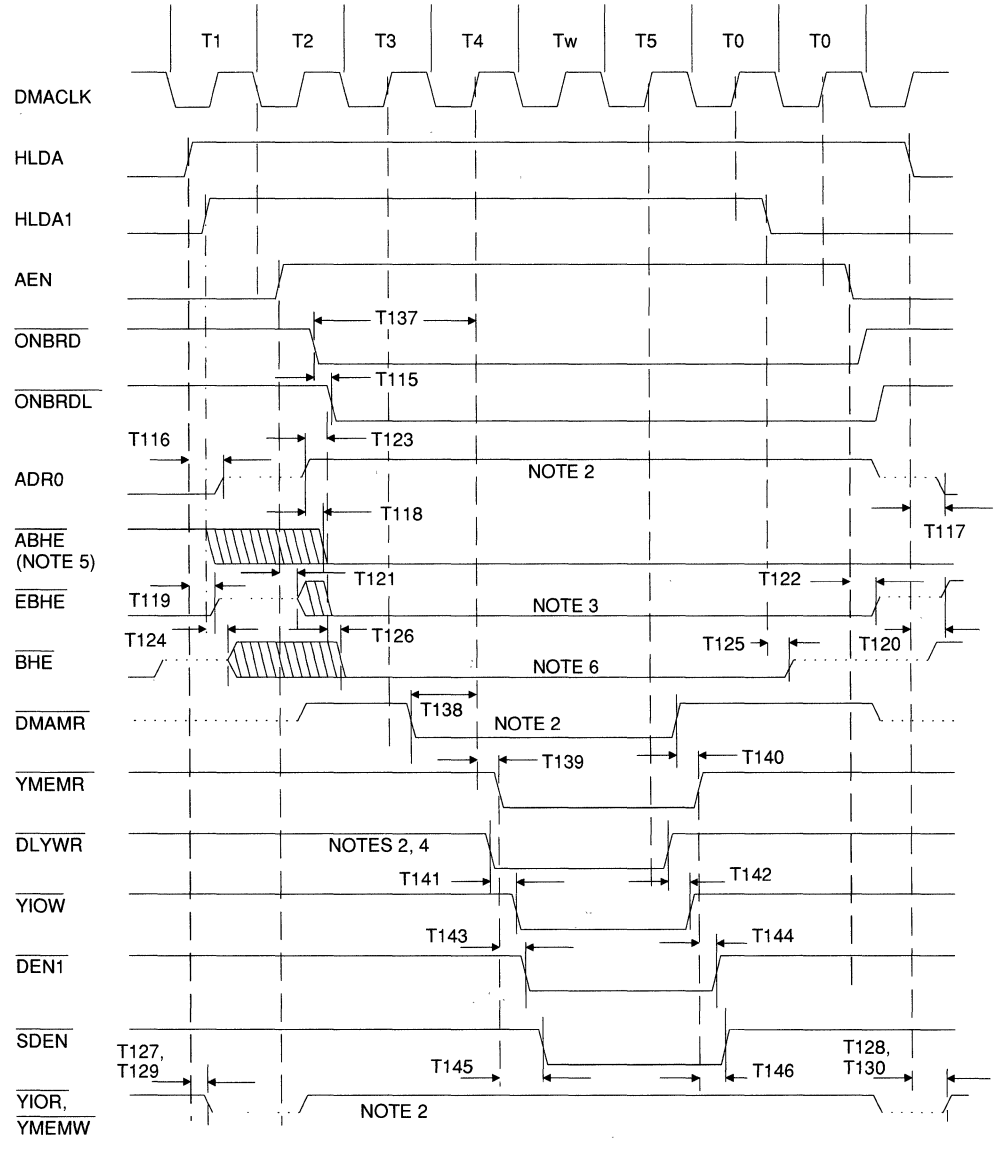
**FIGURE 7-18. BASIC HOLD/HDLA TIMING FOR DMA AND MASTER MODE TRANSFERS**




NOTES:

(1) No refresh cycles are pending
(2) ONBRDL follow ONBRD when HLDA is high
(3) The FE3010 drives these signals when AEN is high
(4) The FE3001 tri-states EBHE when HLDA goes high, but drives it again when AEN is high. It is the inversion of ADR0
(5) BHE is driven by the FE3001 when HLDA1 is high. It follows EBHE
(6) ABHE is the inversion of ADR0 while HLDA is high (8-Bit DMA)
(7) DEN1 and SDEN remain high during 8-Bit, even byte transfers
(8) The FE3001 tri-states DLYWR when AEN is high

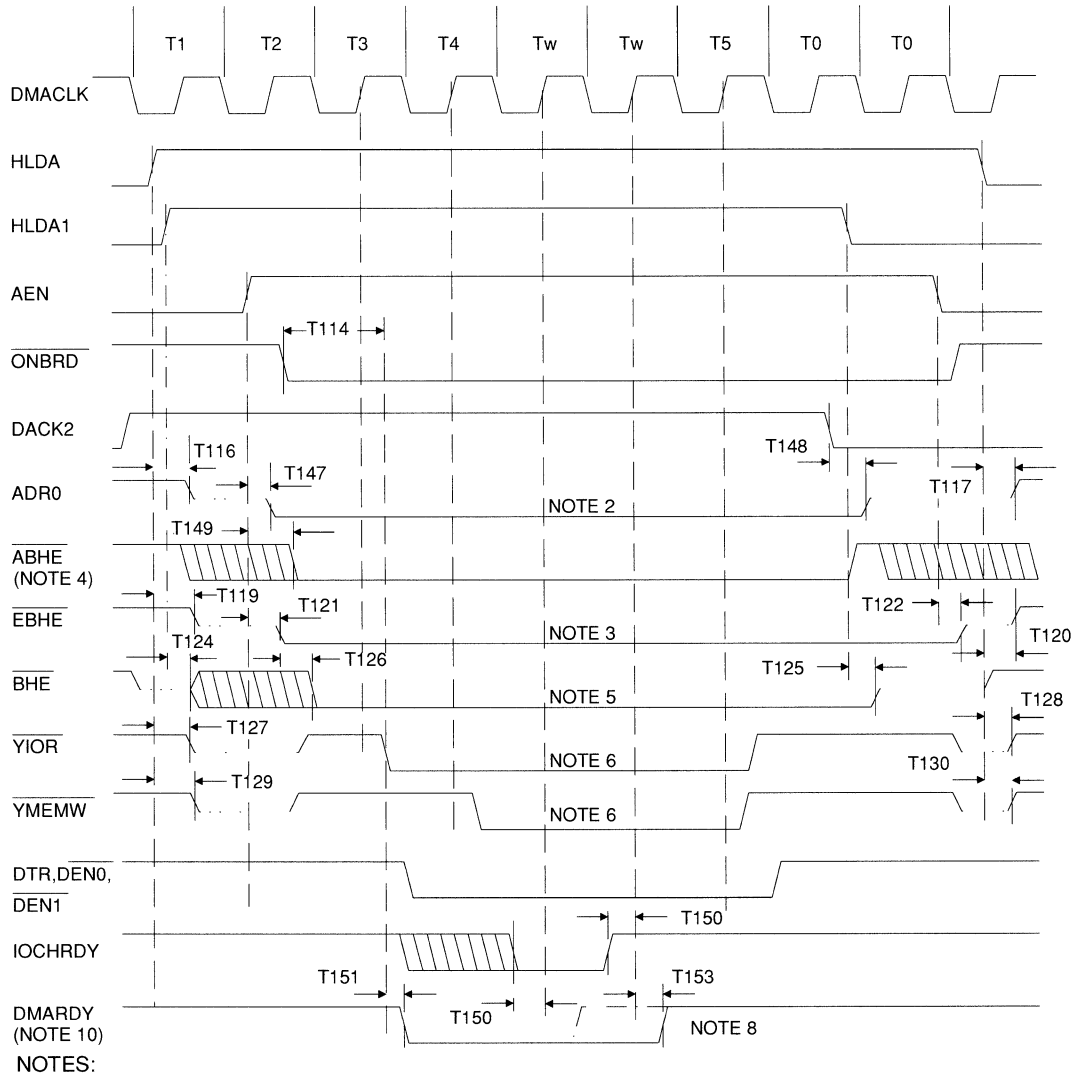
**FIGURE 7-19. DMA TRANSFER TIMING: 8-BIT, I/O TO ON-BOARD MEMORY, EVEN BYTE, WITH NO ADDED WAIT STATES**




NOTES:

(1) No refresh cycles are pending
(2) The FE3010 drives these signals when AEN is high
(3) The FE3001 tri-states $\overline{EBHE}$ when HLDA goes high, but drives it again when AEN is high
(4) The FE3001 tri-states $\overline{DLYWR}$ when AEN is high
(5) $\overline{ABHE}$ is the inversion of ADR0 when HLDA is high
(6) $\overline{BHE}$ is driven by the FE3001 when HLDA1 is high. It follows $\overline{EBHE}$
(7) $\overline{DEN0}$ and DTR remain high and SDTR remains low during this cycle

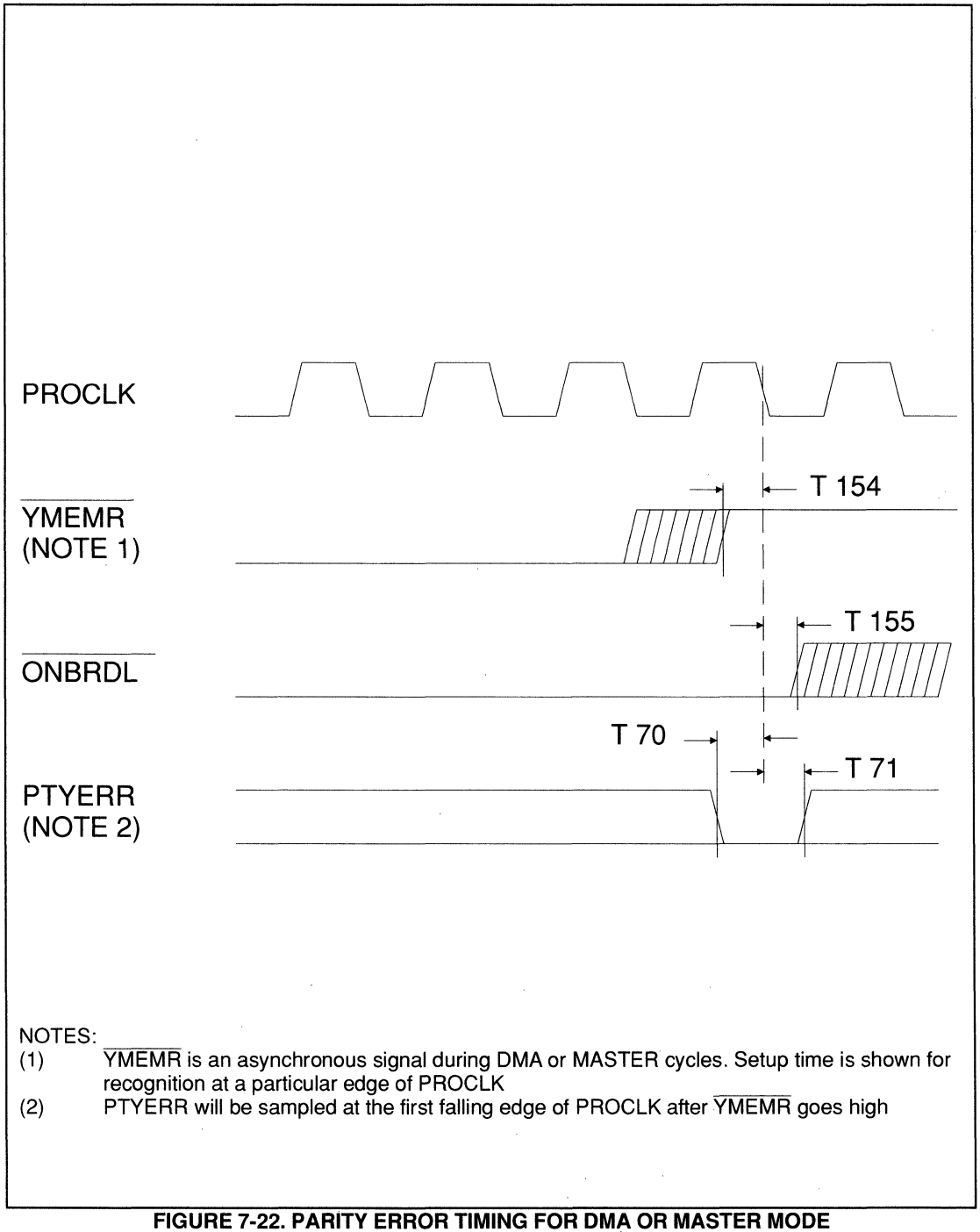
**FIGURE 7-20. DMA TRANSFER TIMING: 8-BIT, ON-BOARD MEMORY TO I/O, ODD BYTE, WITH NO ADDED WAIT STATES**




NOTES:

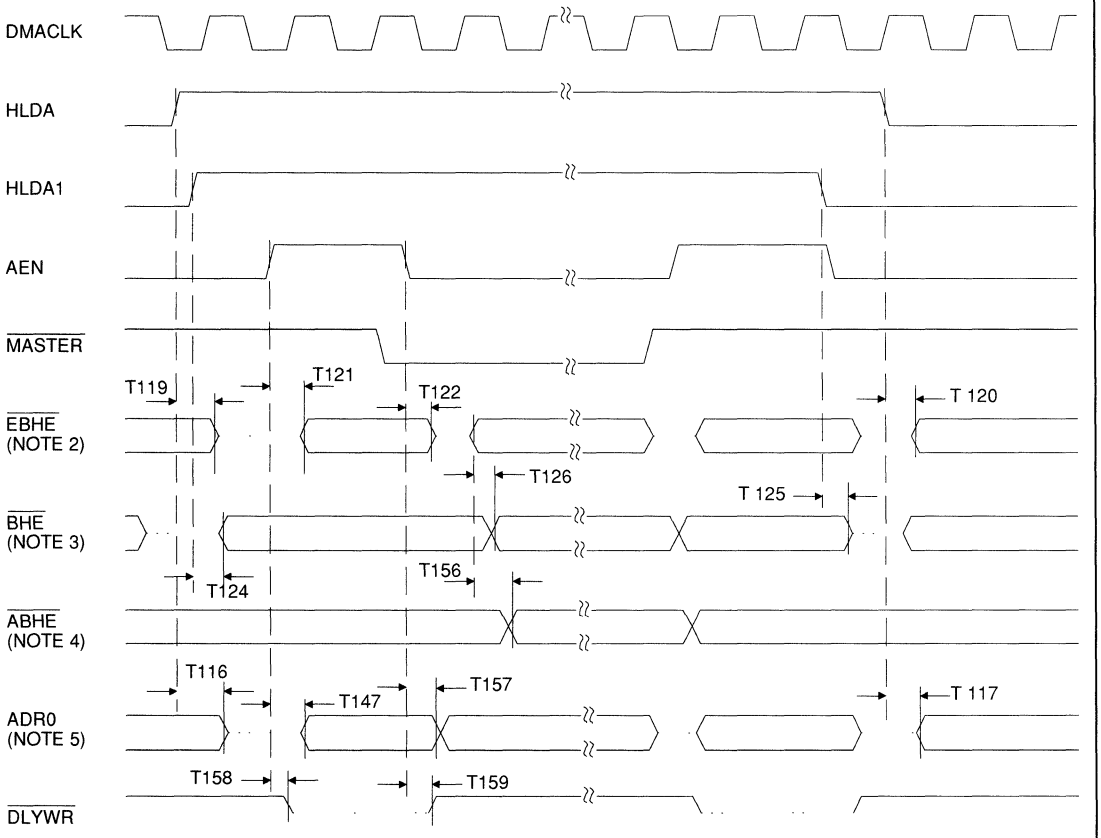
(1) No refresh cycles are pending
(2) ADR0 is tri-stated when HLDA goes high, then driven again when both DACK2 and AEN are high(16-Bit DMA)
(3) EBHE is tri-stated when HLDA goes high, then driven again when AEN is high
(4) ABHE is set low when HLDA, DACK2, and AEN are high
(5) BHE is driven by the FE3001 when HLDA1 is high. It follows EBHE
(6) The FE3010 drives these signals when AEN is high
(7) SDEN is high and SDTR is the inversion of DTR for this cycle
(8) DMARDY would follow the dashed line shown for any DMA cycle where IOCHRDY is not driven low (default timing)
(9) DMAMR, DLYWR, YMEMR, and YIOW timing is the same as for an 8-Bit I/O to memory cycle
(10) DMARDY is driven low by DMAMR in a Memory to I/O DMA cycle

**FIGURE 7-21. DMA TRANSFER TIMING: 16-BIT, I/O TO ON-BOARD MEMORY, WAIT STATE ADDED**




NOTES:
(1) YMEMR is an asynchronous signal during DMA or MASTER cycles. Setup time is shown for recognition at a particular edge of PROCLK
(2) PTYERR will be sampled at the first falling edge of PROCLK after YMEMR goes high

**FIGURE 7-22. PARITY ERROR TIMING FOR DMA OR MASTER MODE TRANSFERS**




NOTES:

(1) No refresh cycles are pending

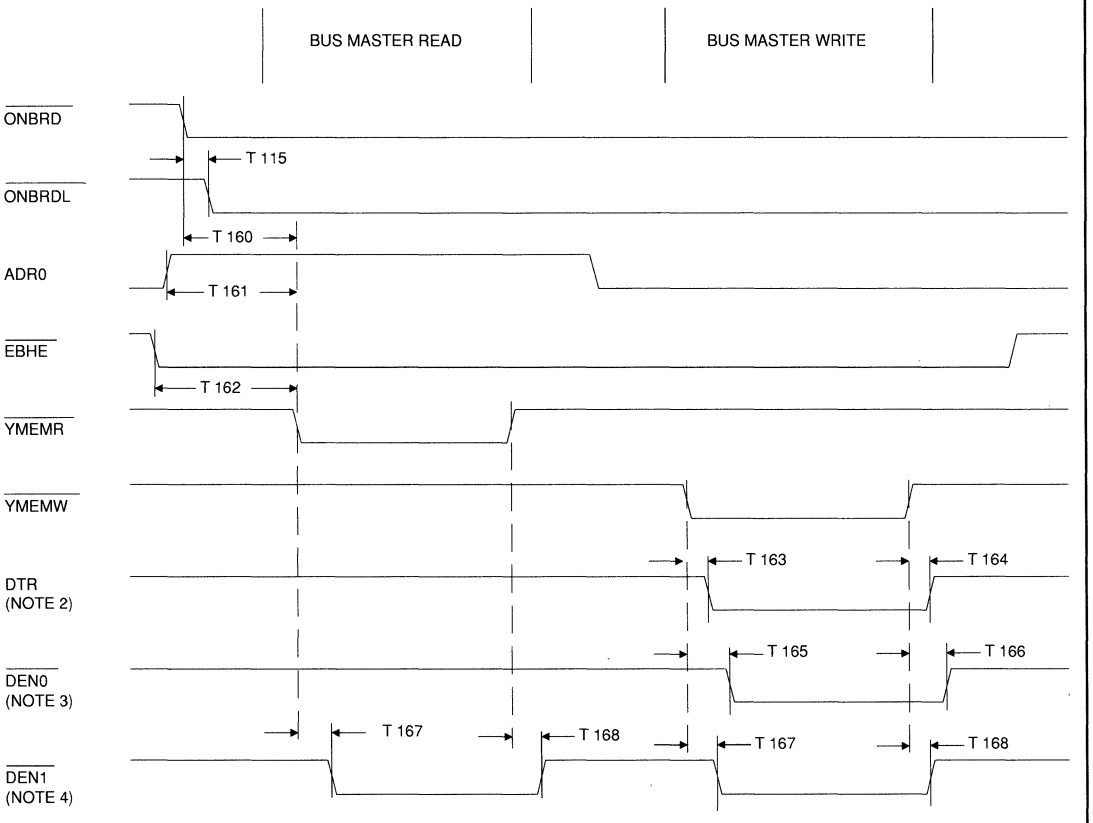
(2) EBHE is driven by the FE3001 when HLDA is low or AEN is high. It is driven by a Bus Master when MASTER is low

(3) BHE is driven by the FE3001 when HLDA1 is high. BHE will follow EBHE during Master mode

(4) ABHE follows EBHE during Master mode

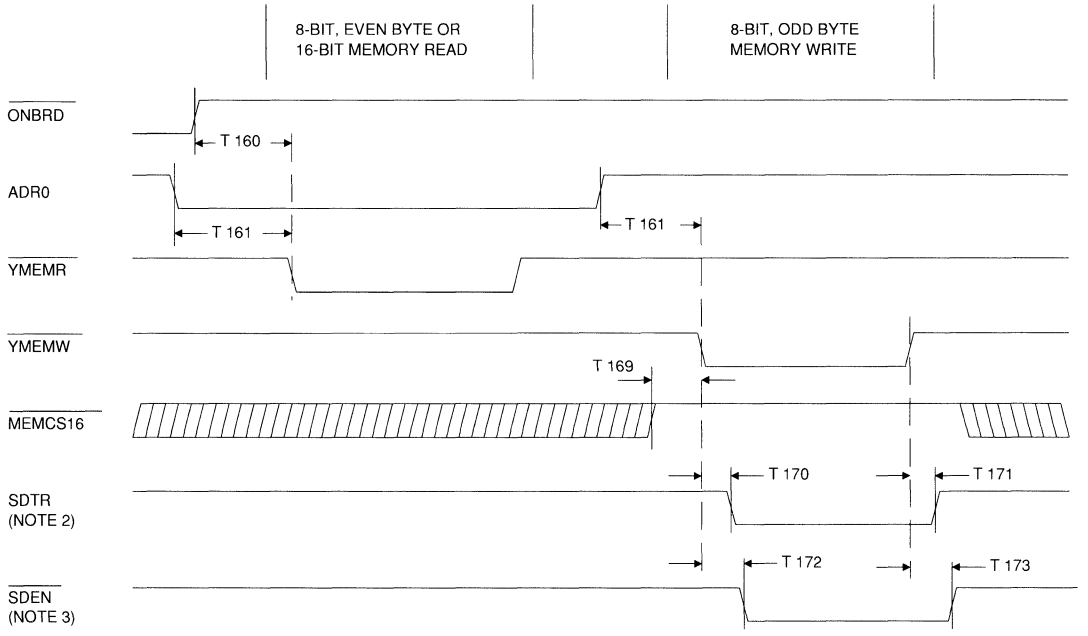
(5) ADR0 is driven by the FE3001 when HLDA is low. It will also be driven by the FE3001 when AEN is high if DACK2 is high (Bus Master uses DMA channel 5 - 7). ADR0 will be driven by the FE3021 when MASTER is low

**FIGURE 7-23. BASIC MASTER MODE TRANSFER TIMING**



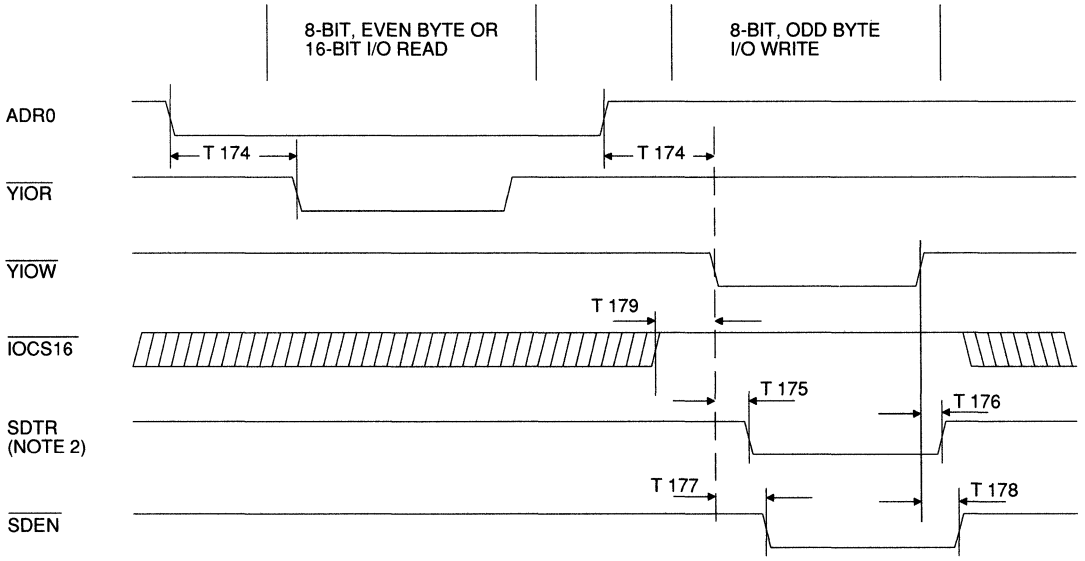

NOTES:
(1) MASTER is low during these cycles
(2) DTR follows YMEMW during Master Mode
(3) DEN0 follows YMEMR or YMEMW if both ONBRD and ADR0 are low
(4) DEN1 follows YMEMR or YMEMW if both ONBRD and EBHE are low
(5) SDEN is high during these cycles

**FIGURE 7-24. MASTER MODE TRANSFER TIMING: ON-BOARD MEMORY READ/WRITE**




NOTES:
(1) MASTER is low during these cycles
(2) SDTR follows YMEMW when MASTER is low
(3) SDEN follows YMEMR or YMEMW when ADR0, MEMCS16, and ONBRD are high
(4) DEN0 and DEN1 will stay high during these cycles because ONBRD is high

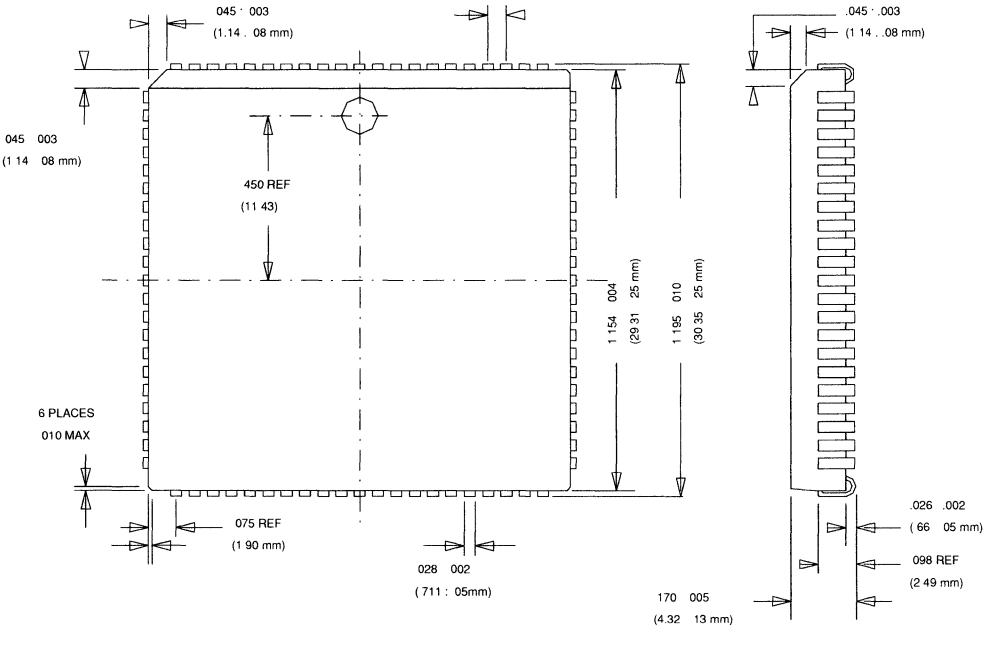
**FIGURE 7-25. MASTER MODE TIMING: OFF-BOARD MEMORY READ/WRITE**




NOTES:
(1) MASTER is low during these cycles
(2) SDTR follows YIOW
(3) SDEN follows YIOR or YIOW when ADR0 and IOCS16 are high. ONBRD does not affect SDEN for I/O cycles
(4) DEN0 and DEN1 will stay high during I/O cycles

**FIGURE 7-26. MASTER MODE TIMING: OFF-BOARD I/O READ/WRITE**

84-Pin Plastic Chip Carrier (J-bend Leads)




1 Mating Socket: Burndy part number Q1LE84P10

3010JLED RVA 12 13 86

**FIGURE 7-27. 84-PIN PLCC PACKAGING DIAGRAM**

# APPENDIX A
# RECOMMENDED BUS CYCLE PROGRAMMING

The following tables give recommended values for programming bus timing registers R0-R8 (see Figure 5 and Table 3). These tables address only AT bus timing parameters, as on-board timing is very application specific. Values are provided for 6.25, 8, 12.5 and 16 MHz system clock speeds. The recommended values in these tables are based on emulating an 8 MHz IBM PC/AT Expansion Bus. Two issues that may affect these recommended values are listed below. Consult application notes for additional details.

**(1)** If the sum of R0 and R1 is 3 or greater, then an internal BALE logic error in first production FE3001 parts may cause BALE to remain high from a previous on-board cycle and fall one PROCLK cycle too early. Widening BALE by one clock accounts for this.

**(2)** Some adapter boards decode the SA0-SA19 address lines to generate $\overline{\text{MEMCS16}}$, a dangerous practice. However, widening BALE and delaying the commands relative to an 8 MHz AT provides relaxed $\overline{\text{MEMCS16}}$ setup time, which is needed for some of these boards to function reliably.

When preparing to select a new CPU clock speed, it is important to setup the FE3001 registers in a particular order so that BALE and commands do not become too short during the programming process. The recommended programming order for selecting high speed or low speed CPU clocks are given below:

**Selecting High Speed CPU Clock:**

R5, R6, R7, R8, R9, R10, R12, R4, R3, R1, R0

**Selecting Low Speed CPU Clock:**

R5, R6, R7, R8, R9, R10, R12, R0, R1, R3, R4

## A.1 6.25 MHz SYSTEM CLOCK SPEED

| REGISTER | FUNCTION | VALUE |
|---|---|---|
| R0 | BALE delay from ALE leading edge | 0 |
| R1 | BALE width | 1 |
| R3 | 8-bit memory, 8/16-bit I/O - command delay | 1 |
| R4 | 8-bit memory or I/O cycle - wait states | 4 |
| R5 | 16-bit I/O cycle - wait states | 1 |
| R6 | 16-bit memory cycle - command delay | 0 |
| R7 | 16-bit memory cycle - wait states | 1 |
| R8 | Minimum number of wait states when ZEROWS is asserted | 0 |

## A.2 8 MHz SYSTEM CLOCK SPEED

| REGISTER | FUNCTION | VALUE |
|---|---|---|
| R0 | BALE delay from ALE leading edge | 0 |
| R1 | BALE width | 1 |
| R3 | 8-bit memory, 8/16-bit I/O - command delay | 1 |
| R4 | 8-bit memory or I/O cycle - wait states | 4 |
| R5 | 16-bit I/O cycle - wait states | 1 |
| R6 | 16-bit memory cycle - command delay | 0 |
| R7 | 16-bit memory cycle - wait states | 1 |
| R8 | Minimum number of wait states when ZEROWS is asserted | 0 |

## A.3 12.5 MHz SYSTEM CLOCK SPEED

| REGISTER | FUNCTION | VALUE |
|---|---|---|
| R0 | BALE delay from ALE leading edge | 1 |
| R1 | BALE width | 2 |
| R3 | 8-bit memory, 8/16-bit I/O - command delay | 4 |
| R4 | 8-bit memory or I/O cycle - wait states | 8 |
| R5 | 16-bit I/O cycle - wait states | 4 |
| R6 | 16-bit memory cycle - command delay | 2 |
| R7 | 16-bit memory cycle - wait states | 4 |
| R8 | Minimum number of wait states when ZEROWS is asserted | 2 |

## A.4 16 MHz SYSTEM CLOCK SPEED

| REGISTER | FUNCTION | VALUE |
|---|---|---|
| R0 | BALE delay from ALE leading edge | 1 |
| R1 | BALE width | 2 |
| R3 | 8-bit memory, 8/16-bit I/O - command delay | 4 |
| R4 | 8-bit memory or I/O cycle - wait states | 10 |
| R5 | 16-bit I/O cycle - wait states | 4 |
| R6 | 16-bit memory cycle - command delay | 2 |
| R7 | 16-bit memory cycle - wait states | 4 |
| R8 | Minimum number of wait states when ZEROWS is asserted | 2 |