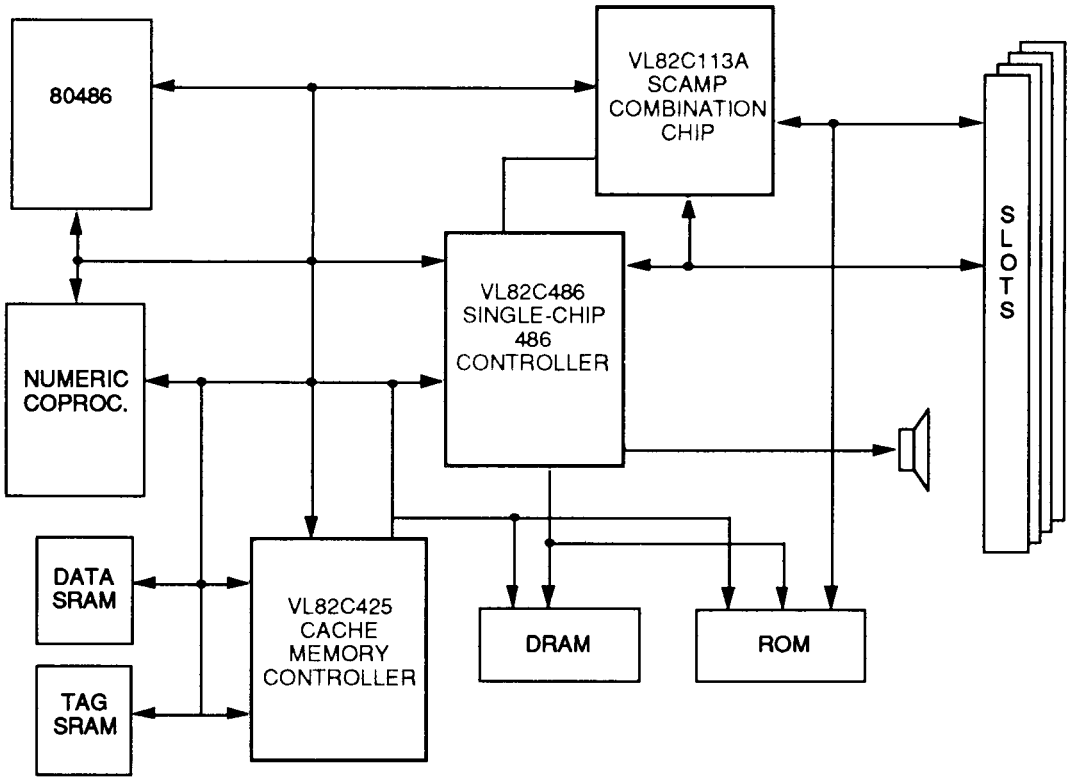
VL82C425 CACHE MEMORY CONTROLLER



OVERVIEW

VLSI Technology, Inc.'s VL82C425 is a high-performance, high-integration, single-chip second-level cache memory controller for use in the design of 486-based PC/AT-compatible systems. When used with the VLSI SC486™ Controller, VL82C486, the VL82C425 provides system designers with an optional 'look-aside' cache to support single motherboard designs for 8 MB to 256 MB memories.

The VL82C425 incorporates comparator, line buffer, and write back control logic on a single chip, providing system designers with many advantages including low total cache system costs, high performance, flexibility, upgradeability, and low product cost.

The device lowers total cache system costs by allowing designers to use standard commodity SRAMs for cache tag and cache data. Zero wait state cache hit burst reads and minimum cache miss penalty for higher performance and flexibility are gained through the VL82C425's support of one or two banks of cache data SRAM operating with bus rates up to 33 MHz. On a read hit, the VL82C425 performs a 2-1-1-1 burst read if two banks of SRAM are used. It performs a 2-2-2-2 burst read if one bank of SRAM is used.

The VL82C425 is housed in a cost-effective 128-lead package and developed with VLSI's 1-micron CMOS process technology.

VL82C425 CACHE MEMORY CONTROLLER

CACHE ORGANIZATION

The VL82C425 Cache Controller provides a low-cost direct map, look-aside write-back cache option for use with the VL82C486 system controller. It supports cache sizes from 64 KB to 1 MB. It can cache from the first 8 MB to the first 256 MB of on-board DRAM, depending on the cache size and tag option selected.

One or two 32-bit wide banks of SRAM may be used to hold the cache data. Standard commodity SRAMs can be used. Increased read performance is obtained by using two banks which allow interleaved accesses during burst read cycles.

A single 8- or 9-bit SRAM is required to hold the tag (upper memory address bits) and the optional dirty bit. The number of tag SRAM locations required is equal to the size of the data cache (in bytes) divided by 16.

On a read hit, the VL82C425 performs a 2-1-1-1 burst read if two banks of SRAM are used. It performs a 2-2-2-2 burst read if one bank of SRAM is used.

On a write hit, the VL82C425 performs a 1 wait state (3 clock cycle) write. A 0 wait state write option is provided for use with data SRAMs which have aggressive set-up and hold times.

For read-misses, the VL82C425 uses an internal line buffer for increased performance. On a read-miss, the data is always read immediately from on-board DRAM and returned to the CPU to allow the 486 CPU to complete its primary cache line-fill without delay. The data is simultaneously loaded into the VL82C425's internal line buffer. The VL82C425 then becomes a LOCAL bus master and writes the contents of the line buffer to the cache SRAMs. If the location in cache to which the data is to be written is dirty, then the old data is first written back to DRAM.

Cacheability of data returned from DRAM memory read is determined from the state of the –KEN input.

On write misses, the VL82C425 is bypassed and the data is written directly to DRAM (no cache line is allocated).

LOCAL bus mastership for performing cache line fills and write-backs is obtained by asserting CHOLD and waiting for CHLDA back from the CPU before taking ownership of the bus. Bus arbitration for other LOCAL bus requesters (such as the VL82C486 during DMA/Master Mode cycles) is provided through means of the SHOLD and SHLDA signals.

During DMA and Master Mode cycles, the VL82C425 checks to see if the contents of a requested memory location are valid in cache. If a cache hit is obtained on a DMA or Master Mode read, then –MISS is made inactive to inhibit the system DRAM controller, and the contents of the selected cache location are enabled onto the bus. If a cache hit is obtained on a DMA or Master Mode write, then the selected cache location is updated with the new data. DMA and Master Mode cycles are ignored by the VL82C425 on a cache miss.

The VL82C425 will detect and respond as above to both synchronous LOCAL bus DMA and Master Mode cycles as well as asynchronous ISA-bus type DMA and Master Mode cycles.

The VL82C425 contains a set of write-protection registers which may be used to protect cached memory in the range from 640 KB to 1 MB from being written. This is to ensure that cached ROM locations cannot become corrupted.

A "Direct Access" mode of operation is provided which allows the cache to appear as ordinary memory on the CPU LOCAL bus. This allows BIOS to easily size the cache memory at power-on reset.

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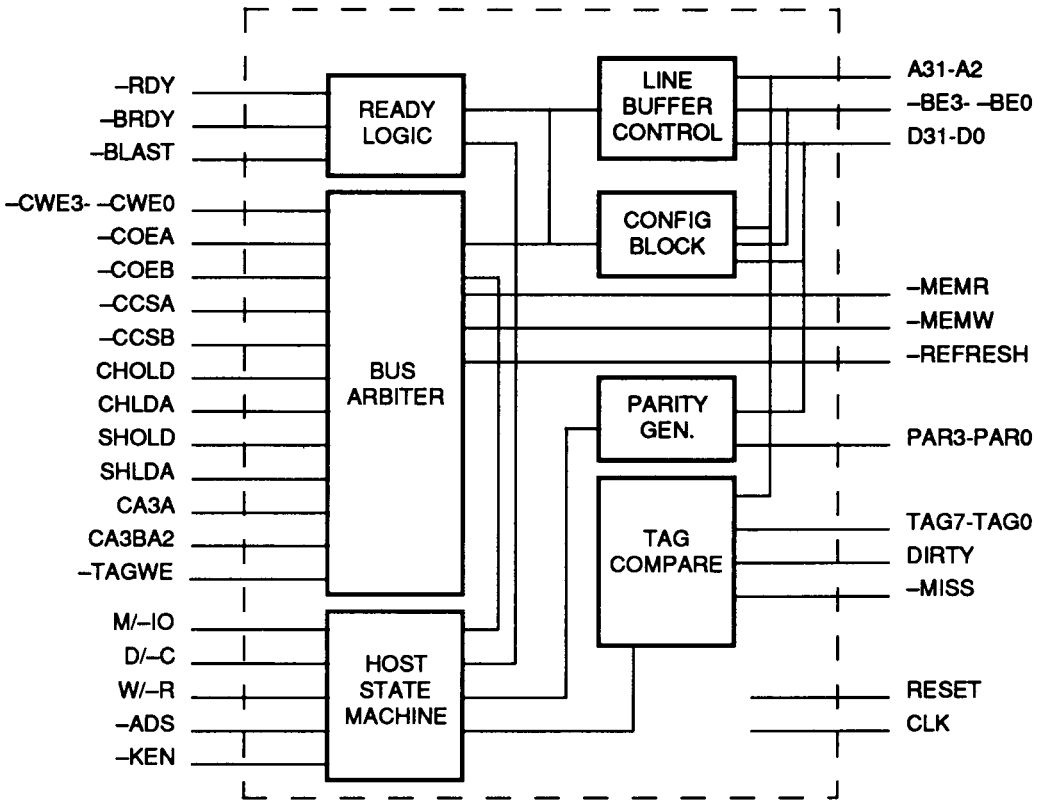

PACKAGING

PART NUMBER	DESCRIPTION	PACKAGE
VL82C425-FC	Cache Memory Controller	128-lead Metric Quad Flat Pack
NOTE: Operating temperature range is 0°C to +70°C		

VL82C425 CACHE MEMORY CONTROLLER

SYSTEM SUPPORT

VLSI Technology offers extensive support for system designers to assist them in their design applications.

- Samples of the VL82C425 Cache Memory Controller
- Evaluation boards available
- Documentation
  - Data sheet
  - Sample schematics
- Software
  - Provided by VLSI Technology and approved BIOS vendors
- Support
  - Support provided by VLSI Technology's Applications Group

RELATED PRODUCTS LISTING

VL82C486 - Single-chip high-performance 486 PC/AT-compatible controller for use in 486SX- and 486DX-based personal computer systems running up to 33 MHz.

VL82C113A - The SCAMP™ Combination I/O chip is an integrated peripheral controller that has been optimized for use with VLSI's VL82C486, VL82C310, VL82C311, and VL82C311L single-chip controllers in PC/AT-compatible computer systems. This chip combines a keyboard controller and a real-time clock with the slot address latches/buffers which are normally required in PC/AT-compatible systems. The VL82C113A was developed with VLSI's 1.0 micron CMOS technology and is available in a 100-lead MQFP. When used with VLSI's single-chip controllers, this chip allows designers to implement a very cost-effective minimum chip count motherboard.

VL82C425 CACHE MEMORY CONTROLLER

FEATURES	BENEFITS
• Single-chip second-level cache controller for 486-based PC/AT-compatible systems	• Optimized for use with the VL82C486 chip set
• "Look-aside" architecture allows cache to be board-level option	• Single-board design for cached/non-cached systems (wide range of performance options)
• Optional 0 or 1 wait state writes on cache hits	• Increased write performance and design flexibility
• Write-back architecture	• Increased write performance
• Direct Map with External Tag SRAM	• Cost control and flexibility in cache size
• Up to 33 MHz operation	• Supports all popular 486 CPUs
• Support single motherboard designs for the following cache sizes: – 64 KB (caches 8 or 16 MB DRAM) – 128 KB (caches 16 or 32 MB DRAM) – 256 KB (caches 32 or 64 MB DRAM) – 512 KB (caches 64 or 128 MB DRAM) – 1 MB (caches 128 or 256 MB DRAM)	• Single design for a wide range of performance options and system configurations
• Uses commodity SRAMs for Cache Tag and Cache Data	• Low-cost cache system
• Burst read cycles: – 2-1-1-1 burst cycles with 2 banks of data SRAM – 2-2-2-2 burst cycles with 1 bank of data SRAM – Minimum cache miss penalty	• High-performance operation
• Maintains full coherency during DMA/Master Mode Cycles	• Required for proper cache operation
• Supports 8- or 9-bit TAG RAM (inclusive of DIRTY bit)	• Flexible system design
• Supports 1 or 2 banks of SRAM	• Flexible system design, increased performance
• 1-micron CMOS technology	• Proven, reliable, high-performance technology
• 128-lead metric quad flat pack	• Cost-effective, industry-standard package

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VLSI CORPORATE OFFICES

CORPORATE HEADQUARTERS • COMMUNICATIONS PRODUCTS DIVISION AND SPECIAL PRODUCTS DIVISION
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FAX 408-922-5252
Mail:
1109 McKay Drive
San Jose, CA 95131

6345 Balboa Blvd.,
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Encino, CA 91316
818-609-9981
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France
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Germany
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