STANDARD
MICROSYSTEMS
CORPORATION

SLC90E46
ADVANCE INFORMATION

SLC90E46 SouthBridge
(Member of High Performance TeXas Chipset)

FEATURES

- 324 Pin BGA South Bridge Chip
- Supports Pentium Compatible Processor With SLC90E42 North Bridge Chip
- 3V Operation with 5V Tolerant Buffers
- PCI 2.1 Compliant
- Integrated PCI To ISA Bridge
  - Supports PCI Bus up to 33 MHz
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA/EIO At 1/4 of PCI Frequency
- Integrated IDE Controller
  - Independent Timing Options for up to Four Drives
  - Supports PIO Mode 0 to 4, DMA Mode 1 and 2
  - Supports "Ultra DMA/33" Synchronous DMA Mode with Transfer Rate up to 33Mbytes/Second
  - Integrated 16 DW Buffer For Each IDE Channel
  - Supports Glue-Less "Swap-Bay" Option with Full Electrical Isolation
  - Supports Both Legacy and PCI-Native Modes
- Integrated USB Host Controller
  - Supports OHCI Host Interface
  - Supports Two USB 1.0 Ports for Serial Transfers at 12 or 1.5Mbit/Sec
  - Supports Legacy Keyboard and Mouse Software with USB-Based Keyboard and Mouse
- Comprehensive Power Management Capability
  - Supports Power-On Suspend and Soft-Off for Desktop Applications
  - All Registers Readable/Restorable For Proper Resume From 0V Suspend
  - Global and Local Device Management
  - Comprehensive Suspend/Resume Logic for Notebook Applications
  - Supports Thermal Alarm
  - Support For External Microprocessor
  - Full Support of ACPI Specification and OS Directed Power Management
  - Supports PCI nCLKRUN Protocol
- Integrated SMBus Host Controller
  - Host Interface Logic Allows CPU to Communicate Via SMBus
  - Slave Interface Logic Allows External SMBus Master to Control Resume Events

- Enhanced DMA Controller
  - Two 8237 DMA Controllers
  - Supports PCI DMA with 3 PC/PCI Channels and Distributed DMA Protocols
  - Supports Type-F DMA with a Deep 4-DW Buffer
- Interrupt Controller
  - Two 8259 Interrupt Controllers
  - Independently Programmable Edge/Level Sensitivity
  - Supports Serial Interrupt
  - Supports Optional External I/O APIC
- Integrated 8254 Timer
- Real Time Clock
  - 56-Byte Battery Backup CMOS SRAM
  - Date Alarm
  - Two 8-Byte Lockout Ranges

The SLC90E46 is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. As a PCI-to-ISA bridge, the SLC90E46 integrates most I/O functions found in a common ISA bridge chip, that include two DMA controllers, two interrupt controllers, an 8254 timer, and a Real Time Clock. The DMA controllers support Type-F data transfers on each of the eight channels. The SLC90E46 also supports PC/PCI and Distributed DMA protocols for PCI based DMA applications. The Interrupt Controllers support Edge or Level sensitive programmable inputs and the use of an external I/O APIC and serial interrupts. The SLC90E46 can be configured to provide chip select decoding for BIOS, RTC, keyboard controller, external microcontroller, and two programmable chip selects. The SLC90E46 can be configured as a subtractive decode bridge or as an positive decode bridge. This allows the use of a subtractive decode PCI-to-PCI bridge.

The SLC90E46 supports two IDE channels for up to four IDE devices in either PIO or Bus Master mode. The SLC90E46 also supports “Ultra DMA/33” synchronous DMA compatible devices for up to 33Mbytes per second data transfer rate. The embedded 16DW deep buffers allow zero wait state PCI burst transfer in either direction.

The SLC90E46 integrates a USB host controller that is Open Host Controller Interface (OHCI) compatible. Two USB ports are implemented in the root hub.

The SLC90E46 supports comprehensive power management, including full clock control, device power management for up to 14 devices, global power management and suspend and resume logic with Power On Suspend, Suspend to RAM or Suspend to Disk. It fully supports operating system directed power management via the ACPI specification. A System Management Bus (SMBus) host and slave interface logic is integrated for communication with other on-board devices.

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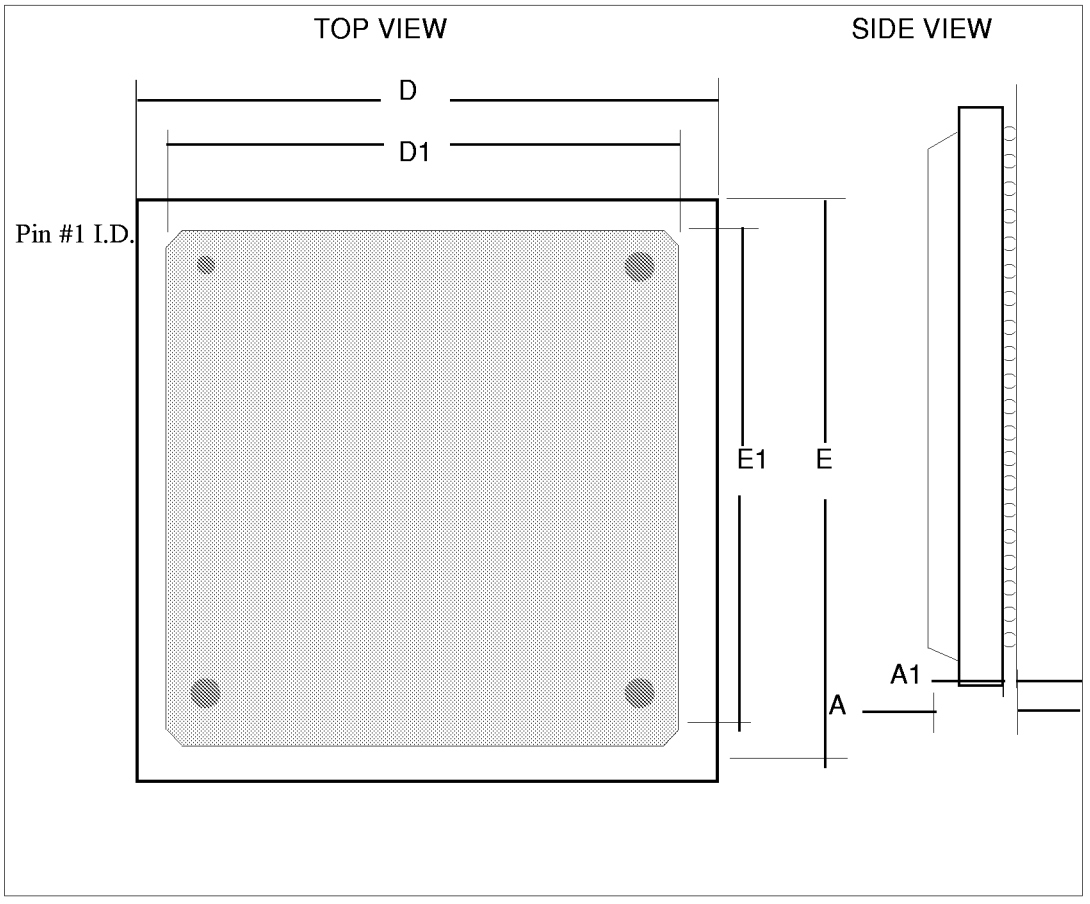
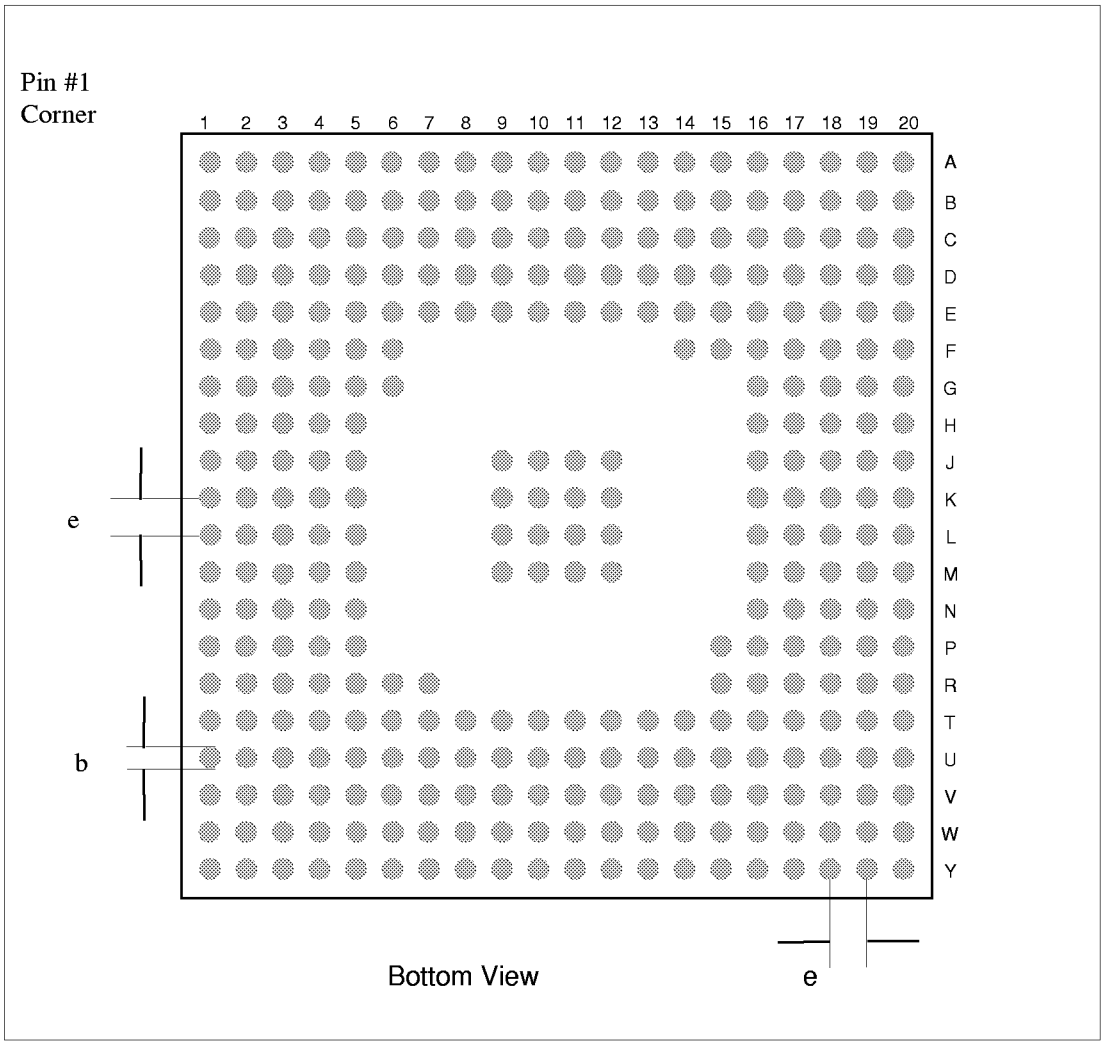
1. SLC90E46 Pinout And Package Specification

The SLC90E46 uses a 324-ball Plastic Ball Grid Array (PBGA) package. These mechanical dimensions and the pinout of the chip are outlined as follows.

1.1. SLC90E46 BGA Package Information





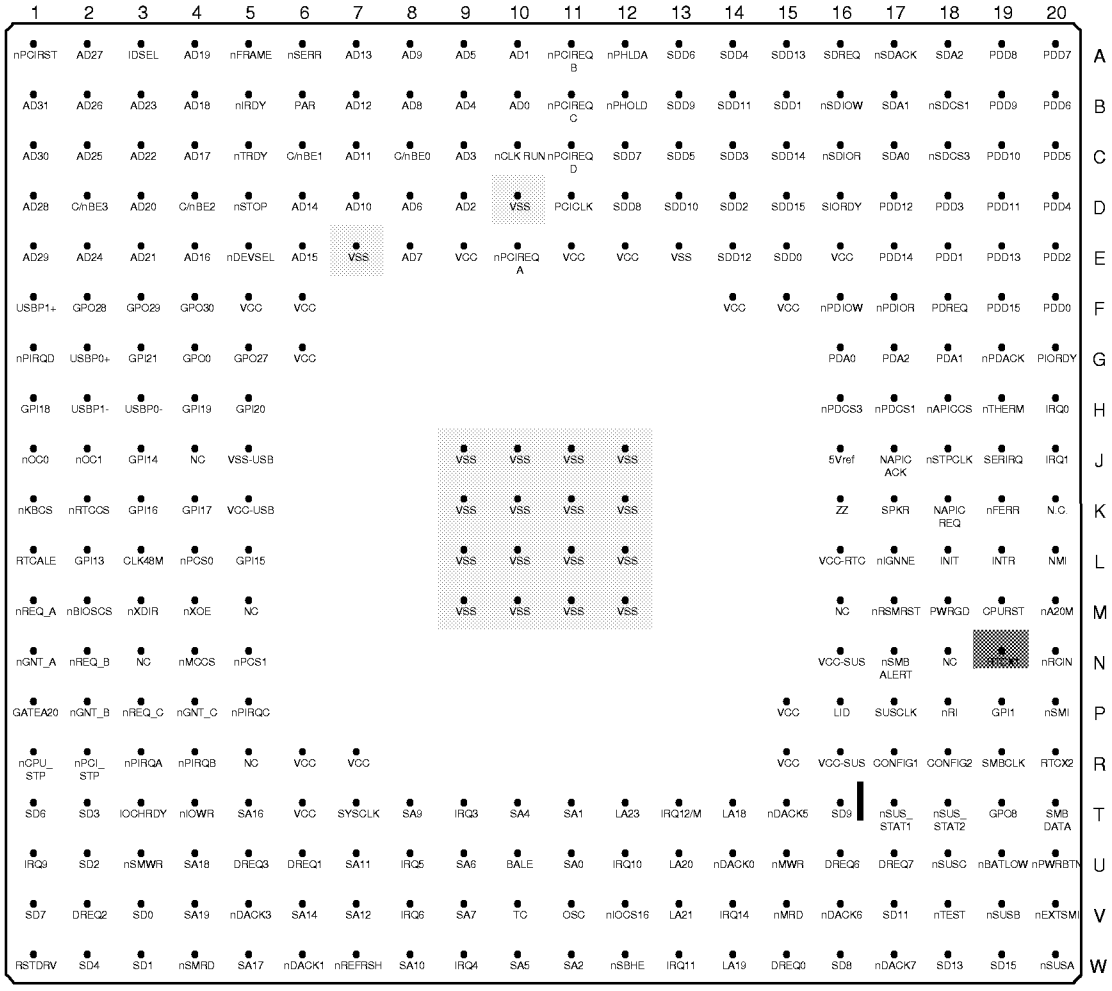
SLC90E46 324-Ball BGA Ball Pattern

SLC90E46 324-pin Ball Grid Array Package

SYMBOL	MIN (mm)	NOMINAL (mm)	MAX (mm)
A	2.16	2.36	2.56
A1	0.50	0.60	0.70
D	26.80	27.00	27.20
D1	23.90	24.00	24.10
E	26.80	27.00	27.20
E1	23.90	24.00	24.10
b	0.60	0.75	0.90
e	1.07	1.27	1.47

1.2. SLC90E46 Pin Assignments

The following diagram shows the pin assignment for the SLC90E46.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	nPCIRST	AD27	IDSEL	AD19	nFRAME	nSERR	AD13	AD9	AD5	AD1	nPCIREQB	nPHLDA	SDD6	SDD4	SDD13	SDREQ	nSDACK	SDA2	PDD8	PDD7	A
B	AD31	AD26	AD23	AD18	nIRDY	PAR	AD12	AD8	AD4	AD0	nPCIREQC	nPHOLD	SDD9	SDD11	SDD1	nSDIOW	SDA1	nSDCS1	PDD9	PDD6	B
C	AD30	AD25	AD22	AD17	nTRDY	C/nBE1	AD11	C/nBE0	AD3	nCLK RUN	nPCIREQD	SDD7	SDD5	SDD3	SDD14	nSDIOR	SDA0	nSDCS3	PDD10	PDD5	C
D	AD28	C/nBE3	AD20	C/nBE2	nSTOP	AD14	AD10	AD6	AD2	VSS	PCICLK	SDD8	SDD10	SDD2	SDD15	SIORDY	PDD12	PDD3	PDD11	PDD4	D
E	AD29	AD24	AD21	AD16	nDEVSEL	AD15	VSS	AD7	VCC	nPCIREQA	VCC	VCC	VSS	SDD12	SDD0	VCC	PDD14	PDD1	PDD13	PDD2	E
F	USBP1+	GPO28	GPO29	GPO30	VCC	VCC								VCC	VCC	nPDIOW	nPDIOR	PDREQ	PDD15	PDD0	F
G	nPIRQD	USBP0+	GPI21	GPO0	GPO27	VCC										PDA0	PDA2	PDA1	nPDACK	PIORDY	G
H	GPI18	USBP1-	USBP0-	GPI19	GPI20											nPDCS3	nPDCS1	nAPICCS	nTHERM	IRQ0	H
J	nOC0	nOC1	GPI14	NC	VSS-USB				VSS	VSS	VSS	VSS				5Vref	NAPICACK	nSTPCLK	SERIRQ	IRQ1	J
K	nKBCS	nRTCCS	GPI16	GPI17	VCC-USB				VSS	VSS	VSS	VSS				ZZ	SPKR	NAPICREQ	nFERR	N.C.	K
L	RTCALE	GPI13	CLK48M	nPCS0	GPI15				VSS	VSS	VSS	VSS				VCC-RTC	nIGNNE	INIT	INTR	NMI	L
M	nREQ_A	nBIOSCS	nXDIR	nXOE	NC				VSS	VSS	VSS	VSS				NC	nRSMRST	PWRGD	CPURST	nA20M	M
N	nGNT_A	nREQ_B	NC	nMCCS	nPCS1											VCC-SUS	nSMBALERT	NC	VSS	nRCIN	N
P	GATEA20	nGNT_B	nREQ_C	nGNT_C	nPIRQC										VCC	LID	SUSCLK	nRI	GPI1	nSMI	P
R	nCPU_STP	nPCI_STP	nPIRQA	nPIRQB	NC	VCC	VCC								VCC	VCC-SUS	CONFIG1	CONFIG2	SMBCLK	RTCX2	R
T	SD6	SD3	IOCHRDY	nIOWR	SA16	VCC	SYSCLK	SA9	IRQ3	SA4	SA1	LA23	IRQ12/M	LA18	nDACK5	SD9	nSUS_STAT1	nSUS_STAT2	GPO8	SMBDATA	T
U	IRQ9	SD2	nSMWR	SA18	DREQ3	DREQ1	SA11	IRQ5	SA6	BALE	SA0	IRQ10	LA20	nDACK0	nMWR	DREQ6	DREQ7	nSUSC	nBATLOW	nPWRBTN	U
V	SD7	DREQ2	SD0	SA19	nDACK3	SA14	SA12	IRQ6	SA7	TC	OSC	nIOCS16	LA21	IRQ14	nMRD	nDACK6	SD11	nTEST	nSUSB	nEXTSMI	V
W	RSTDRV	SD4	SD1	nSMRD	SA17	nDACK1	nREFRSH	SA10	IRQ4	SA5	SA2	nSBHE	IRQ11	LA19	DREQ0	SD8	nDACK7	SD13	SD15	nSUSA	W

1.3. SLC90E46 Pin Assignment Tables in Alphabetical Order

SIGNAL	BALL NO.	SIGNAL	BALL NO.	SIGNAL	BALL NO.
AD0	B10	nDEVSEL	E5	LA20	U13
AD1	A10	DREQ0	W15	LA21	V13
AD10	D7	DREQ1	U6	LA22	Y13
AD11	C7	DREQ2	V2	LA23	T12
AD12	B7	DREQ3	U5	LID	P16
AD13	A7	DREQ5	Y16	nMCCS	N4
AD14	D6	DREQ6	U16	nMEMCS16	Y12
AD15	E6	DREQ7	U17	nMEMR	V15
AD16	E4	nEXTSMI	V20	nMEMW	U15
AD17	C4	nFERR	K19	NMI	L20
AD18	B4	nFRAME	A5	nOC0	J1
AD19	A4	nGNTA	N1	nOC1	J2
AD2	D9	nGNTB	P2	OSC	V11
AD20	D3	nGNTC	P4	PAR	B6
AD21	E3	nGPI1	P19	PCICLK	D11
AD22	C3	GPI13	L2	nPCIREQA	E10
AD23	B3	GPI14	J3	nPCIREQB	A11
AD24	E2	GPI15	L5	nPCIREQC	B11
AD25	C2	GPI16	K3	nPCIREQD	C11
AD26	B2	GPI17	K4	nPCIRST	A1
AD27	A2	GPI18	H1	nPCI_STP	R2
AD28	D1	GPI19	H4	nPCS0	L4
AD29	E1	GPI20	H5	nPCS1	N5
AD3	C9	GPI21	G3	PDA0	G16
AD30	C1	GPO0	G4	PDA1	G18
AD31	B1	GPO8	T19	PDA2	G17
AD4	B9	GPO27	G5	nPDCS1	H17
AD5	A9	GPO28	F2	nPDCS3	H16
AD6	D8	GPO29	F3	PDD0	F20
AD7	E8	GPO30	F4	PDD1	E18
AD8	B8	IDSEL	A3	PDD10	C19
AD9	A8	nIGNNE	L17	PDD11	D19
nAPICACK	J17	INIT	L18	PDD12	D17
nAPICCS	H18	INTR	L19	PDD13	E19
nAPICREQ	K18	nIOCHK	Y1	PDD14	E17
AEN	Y4	IOCHRDY	T3	PDD15	F19
A20GATE	P1	nIOCS16	V12	PDD2	E20
nA20M	M20	nIOR	Y5	PDD3	D18
BALE	U10	nIOW	T4	PDD4	D20
nBATLOW	U19	nIRDY	B5	PDD5	C20
nBIOSCS	M2	IRQ0	H20	PDD6	B20
nC/BE0	C8	IRQ1	J20	PDD7	A20
nC/BE1	C6	IRQ3	T9	PDD8	A19

SIGNAL	BALL NO.	SIGNAL	BALL NO.	SIGNAL	BALL NO.
nC/BE2	D4	IRQ4	W9	PDD9	B19
nC/BE3	D2	IRQ5	U8	nPDDACK	G19
CLK48	L3	IRQ6	V8	PDDREQ	F18
nCLKRUN	C10	IRQ7	Y8	nPDIOR	F17
CONFIG1	R17	nIRQ8	Y20	nPDIOW	F16
CONFIG2	R18	IRQ9	U1	nPHOLD	B12
CPURST	M19	IRQ10	U12	nPHLDA	A12
nCPU_STP	R1	IRQ11	W13	PIORDY	G20
nDACK0	U14	IRQ12/M	T13	nPIRQA	R3
nDACK1	W6	IRQ14	V14	nPIRQB	R4
nDACK2	Y10	IRQ15	Y14	nPIRQC	P5
nDACK3	V5	nKBCCS	K1	nPIRQD	G1
nDACK5	T15	LA17	Y15	POWEROK	M18
nDACK6	V16	LA18	T14	nPWRBTN	U20
nDACK7	W17	LA19	W14	nRCIN	N20
nRI	P18	SDD1	B15	VCC	F15 G6 P15 R6 R7 R15 T6
nRSMRST	M17	SDD10	D13		
RTCALE	L1	SDD11	B14		
nRTCCS	K2	SDD12	E14		
RTCX1	N19	SDD13	A15		
RTCX2	R20	SDD14	C15		
nREFRESH	W7	SDD15	D15		
nREQA	M1	SDD2	D14	VCC-RTC	L16
nREQB	N2	SDD3	C14	VCC-SUS	N16 R16
nREQC	P3	SDD4	A14		
RSTDRV	W1	SDD5	C13	VCC-USB	K5
SA0	U11	SDD6	A13	VREF	J16
SA1	T11	SDD7	C12	VSS	D10 E7
SA10	Q8	SDD8	D12		

SIGNAL	BALL NO.	SIGNAL	BALL NO.	SIGNAL	BALL NO.
SA11	U7	SDD9	B13	VSS	E13 J9 J10 J11 J12 K9 K10 K11 K12 L9 L10 L11 M9 M10
SA12	V7	nSDDACK	A17		
SA13	Y7	SDDREQ	A16		
SA14	V6	nSDIOR	C16		
SA15	Y6	nSDIOW	B16		
SA16	T5	nSERR	A6		
SA17	W5	SIORDY	D16		
SA18	U4	SERIRQ	J19		
SA19	V4	nSLP	K20		
SA2	W11	nSMBALERT	N17		
SA3	Y11	SMBCLK	R19		
SA4	T10	SMBDATA	T20		
SA5	W10	nSMEMR	W4		
SA6	U9	nSMEMW	U3		
SA7	V9	nSMI	P20	VSS	M11 M12
SA8	Y9	SPKR	K17		
SA9	T8	nSTOP	D5	VSS-USB	J5
nSBHE	W12	nSTPCLK	J18	nXDIR	M3
SD0	V3	nSUSA	W20	nXOE	M4
SD1	W3	nSUSB	V19	nZEROWS	Y3
SD10	Y17	nSUSC	U18	ZZ	K16
SD11	V17	SUSCLK	P17	N.C.	J4 M5 M16 N3 N18 R5
SD12	Y18	nSUS_STAT1	T17		
SD13	W18	nSUS_STAT2	T18		
SD14	Y19	SYSCLK	T7		
SD15	W19	TC	V10		
SD2	U2	nTEST	V18		

SIGNAL	BALL NO.	SIGNAL	BALL NO.	SIGNAL	BALL NO.
SD3	T2	nTHRM	H19		
SD4	W2	nTRDY	C5		
SD5	Y2	USBP0+	G2		
SD6	T1	USBP0-	H3		
SD7	V1	USBP1+	F1		
SD8	W16	USBP1-	H2		
SD9	T16	VCC	E9 E11 E12 E16 F5 F6 F14		
SDA0	C17				
SDA1	B17				
SDA2	A18				
nSDCS1	B18				
nSDCS3	C18				
SDD0	E15				

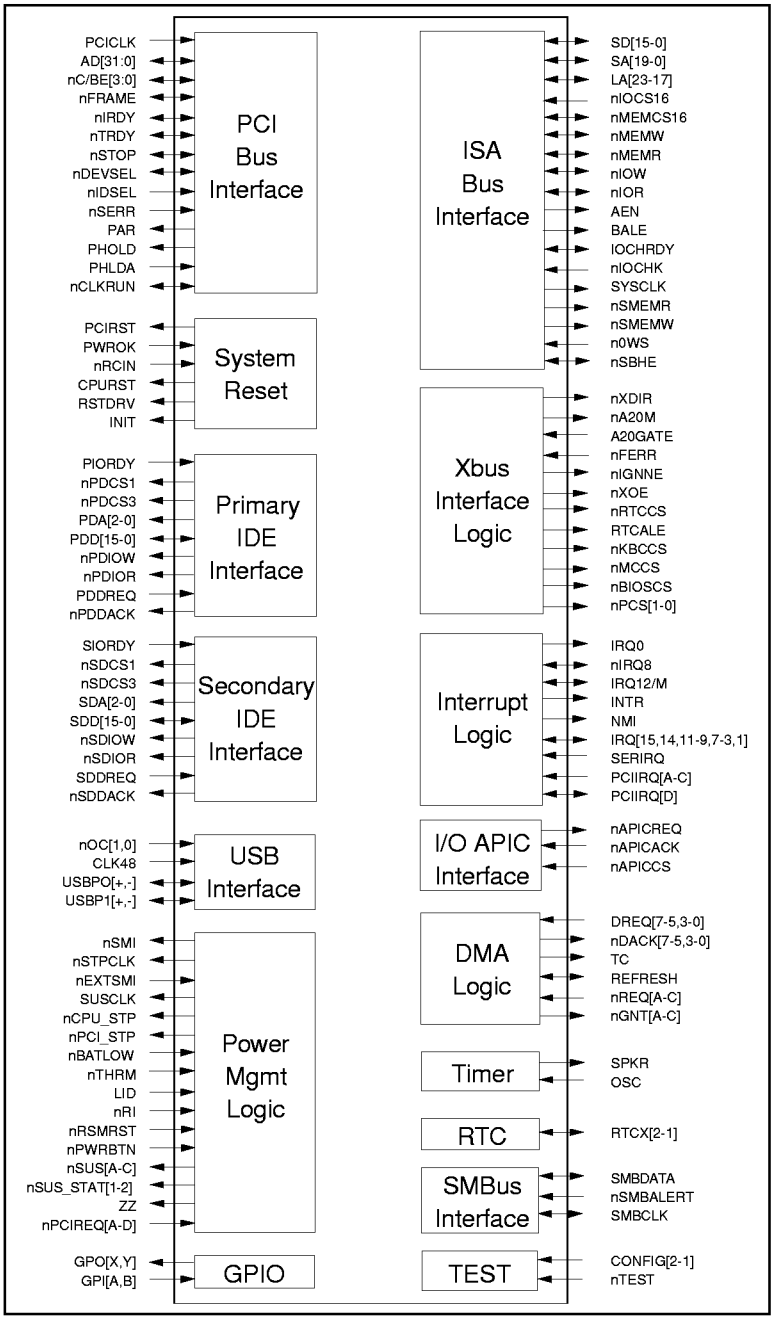


FIGURE 1 - SLC90E46 BLOCK DIAGRAM

2. SLC90E46 Functional Block Overview

The SLC90E46 is a high integration, multiple functions chip. Below is a brief overview of the major functional blocks in the SLC90E46.

2.1. PCI-to-ISA/EIO Bridge

The SLC90E46 is compatible with the PCI 2.1 specification, as well as the ISA bus specification. The SLC90E46 operates as a PCI master for internal modules, such as the IDE controller, USB controller, DMA controller, distributed DMA masters, and ISA masters. The SLC90E46 operates as a slave for its internal registers and for cycles that are passed to the ISA or EIO buses. The SLC90E46 positively decodes all internal registers.

The SLC90E46 can be configured for a full ISA bus or a subset of the ISA bus called the Extended IO (EIO) bus. When EIO bus is configured, unused signals can be configured for General Purpose Inputs and Outputs. Like standard ISA bridge chips, the SLC90E46 also provides byte-swap logic, I/O recovery support, wait-state generation, and SYSCLK generation. Chip select signals are also generated for keyboard controller, BIOS, external RTC, external microcontroller, and two programmable chip selects. The SLC90E46 is designed to directly drive up to 5 ISA slots without external data or address buffering.

The SLC90E46 can be configured as either a subtractive decode PCI to ISA bridge or as positive decode bridge. This allows a system designer to place another subtractive decode bridge in the system, such as a PCI docking chip.

2.1.1. DMA CONTROLLERS, TIMER/COUNTERS, AND INTERRUPT CONTROLLERS

The DMA controllers contain seven independently programmable channels. Channels [0-3] are hardwired to 8-bit, count-by-byte transfers, and channels [5-7] are hardwired to 16-bit, count-by-word transfers. Each of the seven DMA channels can be programmed to support fast Type-F transfers.

The DMA controller supports two different methods for handling legacy DMA via the PCI bus. The Distributed DMA method allows reads and writes to 8237 registers to be distributed to other PCI slave devices. The PC/PCI protocol allows PCI-based peripherals to initiate DMA cycle by encoding requests and grants through three PC/PCI nREQ/nGNT pairs. The two methods can be used concurrently.

The integrated 82C54 controller provides three counters that are used to provide the system timer function, refresh request, and speaker tone. A 14.31818 MHz oscillator input provides the clock source for these three counters.

The SLC90E46 integrates two 8259 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. The SLC90E46 also supports a serial interrupt scheme.

2.1.2. RTC

The SLC90E46 contains a Motorola MC146818A-compatible real-time clock with 256 bytes of battery backed RAM. The RTC operates on a 32.768 Khz crystal. The RTC is integrated to keep track of the time of day and storing system data.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses, that prevents unauthorized reading of passwords or other system security information..

2.1.3. GPIO and Chip Selects

The SLC90E46 provides various general purpose inputs and outputs for custom system design. The number of inputs and outputs varies depending on the configuration. The SLC90E46 also provides two programmable chip selects which allow designer to place devices on the X-Bus without the needs for external decoding logic.

2.2. PCI IDE Controller

The SLC90E46 IDE controller supports two IDE channels, up to four IDE devices such as IDE hard disks and CD-ROM drives. Each IDE device can have independent timings. The IDE transfer rate can be up to 14 Mbytes/second in PIO mode, or 33 Mbytes/second in bus master mode. A 16-by- 32-bit buffer is implemented for each channel so that both channels can operate concurrently and achieve optimal transfers.

The two IDE signal channels are electrically isolated. They can be configured to the standard primary and secondary channel (4 devices) or primary drive 0 and primary drive 1 (2 devices). It allows flexibility in system design and device power management.

2.3. Enhanced Universal Serial Bus (USB) Controller

The SLC90E46 provides Open Host Controller Interface (OHCI) USB support. This includes support that allow legacy software to use a USB-based keyboard and mouse.

2.4. Power Management

The SLC90E46 power management functions include enhanced clock control, local and global device monitoring, and various low-power (suspend) states, such as Power-On Suspend, Suspend-to-RAM, and Suspend-to-Disk. A hardware-based thermal management circuit allows software-transparent entrance to low-power states. Various external events, such as notebook lid open/close, modem/phone ring, suspend/resume button, battery low warning signals can be connected to the dedicated pins of the SLC90E46. It also contains full support for the ACPI specification.

The SLC90E46 also integrates a SMBus Host controller, which includes a Host interface for the CPU to communicate with SMBus slaves and a Slave interface that allows external masters to activate power management events.

3. The SLC90E46 Signal Description

This section provides a detailed description of each SLC90E46 signal. The signals are arranged in functional groups according to their associated function.

The 'n' symbol at the beginning of a signal name indicates that it is an active low signal. When 'n' is not present before the signal name, it indicates an active high signal.

The term **assert** or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate** or **negation** indicates that a signal is inactive.

Certain signals have different functions, depending on the configuration programmed in the PCI configuration space. This signal whose function is being described is in bold font.

The term **High-Z** means tri-stated.
The term **Undefined** means the signal could be high, low, tri-stated, or in some in-between level.

The following notations are used to describe the signal type.

I Input is an input-only signal.
O Totem pole output is a standard active driver.
I/O Input/Output is a bi-directional, tri-state input/output pin.
OD Open drain.
I/OD Input/Open Drain Output is a standard input buffer with an Open Drain Output.
s/t/s Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives a s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it. An external pull-up resistor is required to sustain the inactive state until another agent drives it and must be provided by the central resource.
V This is a power supply pin.

All 3V output signals can drive 5V TTL inputs. Most of the 3V input signals are 5V tolerant. The 3V input signals which are powered via the RTC or Suspend power planes should not exceed their power supply voltage. The open drain (OD) CPU interface signals should be pulled up to the CPU interface signal voltages.

3.1. PCI Interface

NAME	TYPE	DESCRIPTION
AD[31-0]	I/O	**Address/Data.** PCI address and data lines. Address is driven with nFRAME asserted, data is driven or received in following clocks. During Reset: High-Z After Reset: High-Z During POS: High-Z
C/nBE[3-0]	I/O	**Command/Byte Enable.** The command is driven with nFRAME asserted, byte enables corresponding to supplied or requested data is driven in following clocks. C/nBE0 applies to byte 0, C/nBE1 applies to byte 1, etc. During Reset: High-Z After Reset: High-Z During POS: High-Z
nFRAME	I/O	**FRAME.** Its assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer will be followed. nFRAME remains tri-stated until driven by the SLC90E46 as an initiator. During Reset: High-Z After Reset: High-Z During POS: High-Z
nDEVSEL	I/O	**Device Select.** The SLC90E46 asserts nDEVSEL to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, the SLC90E46 asserts nDEVSEL when it samples IDSEL active in configuration cycles to SLC90E46 configuration registers. The SLC90E46 also asserts nDEVSEL when an internal SLC90E46 register is accessed or when the SLC90E46 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, nDEVSEL indicates the response to a SLC90E46 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. nDEVSEL is asserted or sampled at medium decode time. It remains tri-stated until driven by the SLC90E46 as a target. During Reset: High-Z After Reset: High-Z During POS: High-Z
nIRDY	I/O	**Initiator Ready.** The signal is asserted when the SLC90E46 is ready for a data transfer. A data phase is completed on any clock both nIRDY and nTRDY are sampled asserted. nIRDY is an input to the SLC90E46 when the SLC90E46 is the target and an output when the SLC90E46 is an initiator. It remains tri-stated until driven by the SLC90E46 as a master. During Reset: High-Z After Reset: High-Z During POS: High-Z

NAME	TYPE	DESCRIPTION
nTRDY	I/O	**Target Ready.** The signal is asserted when the SLC90E46 is ready for a data transfer. A data phase is completed on any clock both nIRDY and nTRDY are sampled asserted. nTRDY is an input to the SLC90E46 when the SLC90E46 is the initiator and an output when the SLC90E46 is a target. It remains tri-stated until driven by the SLC90E46 as a target. During Reset: High-Z After Reset: High-Z During POS: High-Z
nSTOP	I/O	**Stop.** nSTOP indicates that the SLC90E46, as a Target, is requesting the initiator to stop the current transaction. As an initiator, nSTOP causes the SLC90E46 to stop the current transaction. nSTOP is an output when the SLC90E46 is a Target and an input when the SLC90E46 is an initiator. nSTOP is tri-stated from the leading edge of nPCIRST., and it remains tri-stated until driven by the SLC90E46 as a slave. During Reset: High-Z After Reset: High-Z During POS: High-Z
IDSEL	I	**Initialization Device Select.** IDSEL is used as a chip select during PCI configuration read and write cycles. The SLC90E46 samples IDSEL during the address phase of a transaction. The SLC90E46 responds by asserting nDEVSEL if nIDSEL is sampled active during configuration cycle.
nPHLD	O	**PCI Hold.** The SLC90E46 asserts nPHLD to indicate its desire to use the PCI bus. nPHLD has the highest priority among the five bus request signals. Once the request is granted, nPHLDA will remain asserted until the nPHLD is de-asserted. During Reset: High-Z After Reset: High During POS: High
nPHLDA	I	**PCI Hold Acknowledge.** When it is asserted, it indicates that the SLC90E46 has been granted use of the PCI bus. Once it is asserted, nPHLDA cannot be de-asserted until nPHLD is de-asserted first.
nSERR	I/O	**System Error.** nSERR can be driven active by any PCI device that detects a system error condition. Upon sampling nSERR active, the SLC90E46 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. During Reset: High-Z After Reset: High-Z During POS: High-Z

NAME	TYPE	DESCRIPTION
PAR	O	**Parity.** PAR is "even" parity and is calculated on 36 bits (AD[31-0] and C/BE[3-0]#). PAR is calculated on 36 bits regardless of the valid byte enables. PAR is driven and tri-stated identically to the AD[31-0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase for all SLC90E46 initiated transactions. It is also an output during the data phase when the SLC90E46 is the initiator of a PCI write transaction, and when it is the target of a read transaction. During Reset: High-Z After Reset: High-Z During POS: High-Z
nCLKRUN	I/O 3.3V/5 V	**Clock Run Enable.** SLC90E46 uses this signal to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert nCLKRUN to request that the PCI clock be restarted or to keep it from stopping. The nCLKRUN protocol is specified in the PCI Mobile Design Guide Revision 1.0. During Reset: Low After Reset: Low During POS: High
nPCIRST	O	**Reset.** SLC90E46 asserts nPCIRST to reset devices that resides on the PCI bus. The SLC90E46 asserts nPCIRST during power-up and when a hard reset sequences is initiated through the RC register. nPCIRST is asserted for a minimum of 1 ms after PWROK is driven active. It is driven for a minimum of 1ms when initiated through the RC register. The signal is driven asynchronously relative to PCICLK. During Reset: Low. After Reset: High. During POS: High.

3.2. ISA/EIO Interface Signals

NAME	TYPE	DESCRIPTION
SA[19-0]	I/O	**System Address.** The address lines SA[19-17] that are coincident with LA[19-17] are defined to have the same values as LA[19-17] for all memory cycles. For I/O accesses, only SA[15-0] are used, and SA[19-16] are undefined. SA[19-0] are outputs when the SLC90E46 owns the ISA bus. They are inputs when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: Undefined During POS: Last SA
LA[23-17] / GPO[7-1]	I/O	**ISA LA[23-17].** LA[23-17] address lines allow accesses to physical memory on the ISA bus up to 16 Mbytes. They are outputs when the SLC90E46 owns the ISA bus. They become inputs whenever an ISA master owns the ISA bus. These signals are at an undefined state upon nPCIRST. **GPO.** If EIO configuration is selected, these signals become general purpose outputs. During Reset: High-Z After Reset: Undefined. During POS: Last LA/GPO
SD[15-0]	I/O	**System Data.** 16-bit data path for devices residing on the ISA bus. They are undefined during refresh. During Reset: High-Z After Reset: Undefined. During POS: High-Z.
nSMEMR	O	**Standard Memory Read.** The SLC90E46 asserts nSMEMR to request an ISA memory slave to drive data onto the data lines. If the memory access is below the 1Mbyte range during DMA, SLC90E46 master, or ISA master cycles, the SLC90E46 asserts nSMEMR. nSMEMR is a delayed version of nMEMR. During Reset: High-Z After Reset: High During POS: High
nSMEMW	O	**Standard Memory Write.** The SLC90E46 asserts nSMEMR to request an ISA memory slave to receive data from the data lines. If the memory access is below the 1Mbyte range during DMA, SLC90E46 master, or ISA master cycles, the SLC90E46 asserts nSMEMW. nSMEMW is a delayed version of nMEMW. During Reset: High-Z After Reset: High During POS: High
nMEMR	I/O	**Memory Read.** nMEMR is the command to a memory slave that it may drive data onto the ISA data bus. nMEMR is an output when the SLC90E46 owns the ISA bus or during refresh cycles. nMEMR is an input when an ISA master owns the ISA bus. For DMA cycles, the SLC90E46, as a master, asserts nMEMR. During Reset: High-Z After Reset: High During POS: High.

NAME	TYPE	DESCRIPTION
nMEMW	I/O	**Memory Write.** nMEMW is the command to a memory slave that it may latch data from the ISA data bus. nMEMW is an output when the SLC90E46 owns the ISA bus. nMEMW is an input when an ISA master owns the ISA bus. For DMA cycles, the SLC90E46, as a master, asserts nMEMW. During Reset: High-Z After Reset: High During POS: High.
nREFRESH	I/O	**Refresh Request.** As an output, nREFRESH is used to indicate when a refresh is in progress. The SA[7-0] should be applied to all banks of DRAM on the ISA bus so that when nMEMR is asserted, the entire expansion bus DRAM is refreshed. This signal is an output only when the SLC90E46 DMA controller is a master on the bus responding to the internally generated request for refresh. It is an input signal during ISA master cycles. During Reset: High-Z After Reset: High During POS: High
AEN	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from claiming DMA cycles as valid I/O cycles. When de-asserted, it indicates that an I/O slave may respond to the bus command. When asserted, it informs I/O slave that a DMA transfer is occurring on the ISA bus. The signal is driven high during SLC90E46 initiated refresh cycles, it is driven low upon nPCIRST. During Reset: High-Z After Reset: Low During POS: Low
BALE	O	**Address Latch Enable.** BALE is asserted by the SLC90E46 to indicate that the address and nSBHE signal lines are valid. The LA[23-17] are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. During Reset: High-Z After Reset: Low During POS: Low
nSBHE	I/O	**System Byte High Enable.** When asserted indicates that a byte is being transferred on the SD[15-8] of the data bus. It is negated during refresh cycle. nSBHE is an output when the SLC90E46 owns the ISA bus. It becomes an input when an external ISA master owns the ISA bus. During Reset: High-Z After Rest: Undefined During POS: High
nIOCHK / GPI0	I	**IO Channel Check.** When asserted, the signal indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI feature is enabled. **GPI[0].** If the EIO bus is selected, it becomes a general purpose input.

NAME	TYPE	DESCRIPTION
IOCHRDY	I/O	**IO Channel Ready.** When asserted, the signal indicates that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when the SLC90E46 owns the ISA bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. It becomes an output when an external ISA master owns the ISA bus and is accessing DRAM or a SLC90E46 register. As an output, the signal is driven low from the falling edge of the ISA commands by the SLC90E46. After data is available for the ISA master to read or the SLC90E46 latches the data for a write cycle, IOCHRDY is asserted for 70ns. After that, the IOCHRDY is floated. The SLC90E46 does not drive the signal when it is not the target of a bus master cycle. During Reset: High-Z After Reset: High-Z During POS: High-Z
nIOCS16	I	**16-Bit IO Chip Select.** When asserted, it indicates that the ISA IO device supports 16-bit I/O bus cycles.
nIOR	I/O	**IO Read.** ISA I/O Read command to an ISA I/O device. The I/O device must hold the data valid until after nIOR is negated. nIOR is an input when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: High During POS: High
nIOW	I/O	**IO Write.** ISA I/O Write command to an ISA I/O device. The I/O device may latch data from the ISA data bus. nIOW is an input when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: High During POS: High
nMEMCS16	I/O	**Memory Chip Select 16.** nMEMCS16 is a decode of LA[23-17] without any qualification of the command signals. ISA devices that are 16-bit memory devices drive this signal low. The SLC90E46 ignores nMEMCS16 during I/O and refresh cycles. It is used by byte-swap logic during DMA cycles. This signal is an output when an ISA master owns the ISA bus. The SLC90E46 drives this signal low during ISA master to DRAM cycles. During Reset: High-Z After Reset: High-Z During POS: High-Z
nMEMR	I/O	**Memory Read.** ISA Memory Read command to an ISA Memory device. nMEMR is an input when an external ISA master owns the ISA bus. It is an output when the SLC90E46 is a master on the ISA bus. This signal is also an output during refresh and DMA cycles. During Reset: High-Z After Reset: High During POS: High
nMEMW	I/O	**Memory Write.** ISA Memory Write command to an ISA Memory device. nMEMW is an input when an external ISA master owns the ISA bus. It is an output when the SLC90E46 is a master on the ISA bus. This signal is also an output during DMA cycles. During Reset: High-Z After Reset: High During POS: High

NAME	TYPE	DESCRIPTION
n0WS	I	**Zero Wait States.** The signal is asserted by an ISA slave to indicate that the current cycle can be shortened after the address and command signals are decoded. 16-Bit ISA memory cycle can be reduced to 2 SYSCLKs. 8-Bit memory or I/O cycle can be reduced to 3 SYSCLKs. 16-Bit IO cycle is not affected. If IOCHRDY is de-asserterd and n0WS is asserted during the same clock, then n0WS is ignored and wait states are added whil IOCHRDY is de-asserted.
RSTDRV	O	**Reset Drive.** The SLC90E46 asserts RSTDRV to reset devices that reside on the ISA/EIO bus. The SLC90E46 asserts the signal during hard reset and power-up. It is also driven active for a minimum of 1ms if a hard reset has been programmed in the RC register. During Reset: High After Reset: Low During POS: Low

3.3. Xbus Interface Signals

NAME	TYPE	DESCRIPTION
A20GATE	I	**Address 20 Gate.** This input from the keyboard controller is internally "ORed" with bit 1 (FAST_A20) of the Port 92 register, which is then output via the nA20M signal.
nBIOSCS	O	**BIOS Chip Select.** This signal is driven active during read or write accesses to the enabled BIOS memory range by decoding the SA[19-0] and LA[23-17] address signals. During DMA cycles, nBIOSCS is not generated. During Reset: High After Reset: High During POS: High
nKBCCS / GPO26	O	**Keyboard Controller Chip Select.** This signal is asserted during I/O Read or Write accesses to I/O ports 60h and 64h by decoding the ISA addresses SA[19-0] and LA[23-17]. **GPO26.** If the keyboard controller does not require a fully decoded chip select signal, this pin can be used as a general purpose output. During Reset: High After Reset: High During POS: High.
nMCCS	O	**Microcontroller Chip Select.** nMCCS is asserted during I/O read or write accesses to IO locations 62h and 66h by decoding the ISA addresses SA[19-0] and LA[23-17]. During Reset: High After Reset: High During POS: High

NAME	TYPE	DESCRIPTION
RTCALE / GPO25	O	**Real Time Clock Address Latch Enable.** RTCALE is used to latch memory address into the RTC. A write to port 70h with the appropriate RTC memory address causes RTCALE to be asserted. RTCALE is asserted on the falling edge of nIOW and remains asserted for 2 SYSCLKs. **GPO25.** This pin can be used as GPO25 when the internal RTC is enabled. During Reset: Low After Reset: Low During POS: Low / GPO
nRTCCS / GPO24	O	**RTC Chip Select.** nRTCCS is asserted during Read or Write I/O accesses to I/O location 71h. **GPO24.** This pin can be used as GPO24 when the internal RTC is enabled. During Reset: High After Reset: High During POS: High / GPO
nPCS[1-0]	O	**Programmable Chip Selects.** These active low chip select signals are asserted for ISA I/O cycles (generated by PCI masters) which hit the programmable I/O ranges. The X-Bus buffer signals (nXOE and nXDIR) are enabled while the chip select is active. During Reset: High After Reset: High During POS: High
nRCIN	I	**Reset CPU.** This signal is coming from keyboard controller to generate INIT signal to the CPU.
nXOE / GPO23	I/O	**XBus Transceiver Output Enable.** nXDIR is tied to the output enable of a 245 transceiver that buffers the XD[7-0] from SD[7-0]. nXOE is asserted anytime a Xbus device is decoded, and the devices decode is enabled in the Xbus Chip Select Enable Register (nBIOSCS, nKBCCS, nRTCCS, and nMCCS) or the Device Resource B and C (nPCS0 and nPCS1). nXOE is asserted from the falling edge of the ISA commands for PCI/ISA master initiated cycles. It is negated from the rising edge of the ISA command signals. nXOE is not generated during any access to an Xbus peripheral in which its decode space has been disabled. **GPO23.** If Xbus is not used, then this signal can be used as a general purpose output. During Reset: High After Reset: High During POS: High / GPO

3.4. DMA Signals

NAME	TYPE	DESCRIPTION
DREQ[0-3] DREQ[5-7]	I	**DMA Request.** These DREQ lines are used to request DMA services from the DMA controller or for a 16-bit ISA master to gain control of the ISA bus. The active level (high or low) can be programmed via the DMA command register. The request must remain active until the corresponding nDACK is asserted.
nDACK[0-3] nDACK[5-7]	O	**DMA Acknowledge.** DMA acknowledge signals for the corresponding requests. If the DREQ goes inactive before nDACK being asserted, the nDACK signal will not be asserted. During Reset: High After Reset: High During POS: High
nREQ[A-C]/ GPI[2-4]	I	**PC/PCI DMA Request.** These are DMA requests for PC/PCI protocol. **GPI[2-4].** If PC/PCI protocol is not used, these can be used as general purpose inputs.
nGNT[A-C]/ GPO[9-11]	O	**PC/PCI DMA Grant.** There are DMA grant for PC/PCI protocol. **GPO[9-11].** If PC/PCI protocol is not used, these can be used as general purpose outputs.. During Reset: High After Reset: High During POS: High / GPO
TC	O	**Terminal Count.** Terminal count indicator. The SLC90E46 asserts TC after a new address has been output and the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization.

3.5. Interrupt and APIC Signals

NAME	TYPE	DESCRIPTION
IRQ0 / GPO14	O	**Interrupt Request 0.** If the external APIC is used, this is an output reflecting the state of the internal IRQ0 signal from the system timer. **GPO[14]:** General purpose output if there is no external APIC. During Reset: Low After Reset: Low During POS: IRQ0/GPO
IRQ1	I	**Interrupt Request 1.** A low to high edge transition on IRQ1 is latched by SLC90E46. IRQ1 must remain asserted until after the interrupt is acknowledged. If IRQ1 goes inactive before it is acknowledged, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ[3-7, 10-11, 14-15]	I	**Interrupt Requests.** These interrupts may be programmed for either an edge sensitive or a high level sensitive mode. Default is edge sensitive mode. If the request goes inactive before it is acknowledged, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
nIRQ8/ GPI6	I	**nIRQ8.** An edge trigger interrupt input from external RTC. **GPI6.** If used the internal RTC, this pin can be used a general purpose input. If APIC is enabled, this pin becomes an output.
IRQ12/M	I	**Interrupt Request 12.** This is an interrupt request channel 12. In addition, this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt is selected, the SLC90E46 latches a low to high transition on this signal and generates an INTR to the CPU as IRQ12. An internal IRQ12 interrupt will continue to be generated until a Reset or an I/O read access to address 60h is detected.
nPIRQ[A-D]	I/OD PCI	**PCI Programmable Interrupt Requests.** The nPIRQx signals are active low, level sensitive interrupt inputs. They can be individually steered to ISA interrupts IRQ[3-7,9-12,14-15]. The USB controller uses nPIRQD as its interrupt output signal. The Power Management controller uses nPIRQA as its interrupt output.
SERIRQ / GPI7	I/O	**Serial Interrupt Request.** Serial interrupt input decoder, typically used with the Distributed DMA protocol. **GPI7.** If not using DDMA, this pin can be used as a general-purpose input.

NAME	TYPE	DESCRIPTION
nIRQ9OUT/ GPO29	O	**nIRQ9OUT.** nIRQ9OUT is used to route the internally generated SCI and SMBus interrupts out of the SLC90E46 for connection to an external IO-APIC. **GPO29.** If APIC is disabled, this signal pin is a General Purpose Output. During Reset: High After Reset: High During POS: IRQ9OUT/GPO
nAPICCS/ GPO13	O	**APIC Chip Select.** This signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmable I/O APIC address space. **GPO13.** When the external APIC is not used, then this pin can be used as general purpose output. During Reset: High After Reset: High During POS: High/GPO
nAPICREQ/ GPI5	I	**APIC Request.** The external APIC device asserts the signal prior to sending an interrupt over the APIC serial bus. When the SLC90E46 samples the active signal, it will assert the nAPICACK after the internal buffers (Type-F DMA buffer) are flushed. The nAPICREQ input must be synchronous to PCICLK. **GPI5.** If no external APIC is used, then this pin can be used as general purpose input.
nAPICACK/ GPO12	O	**APIC Acknowledge.** The SLC90E46 asserts this signal after its internal buffers are flushed in response to the nAPICREQ signal. The asserted nAPICACK signal indicates that the APIC can proceed to send the APIC interrupt. This signal is synchronous to PCICLK. **GPO12.** If no external APIC is used, then this pin can be used as general purpose output.

3.6. CPU Interface Signals

NAME	TYPE	DESCRIPTION
nA20M	OD	**A20 Mask.** The SLC90E46 asserts this signal to the CPU based on an internal OR of bit 1 (FAST_A20), port 92 and A20GATE input. During Reset: High-Z After Reset: High-Z During POS: High-Z
nFERR	I	**Numerical Processor Error.** When it is asserted by the CPU, the SLC90E46 activates IRQ13 to the internal interrupt controller. An IO write to port F0h will cause the SLC90E46 to assert nIGNNE to the CPU while nFERR is active. nFERR is used to gate the nIGNNE signal to ensure that nIGNNE is not asserted to the CPU unless nFERR is active.
nIGNNE	OD	**Ignore Numeric Exception**. An output signal to the CPU. While FERR_ is low, an IO write to port F0h will cause this signal to go low. It is inactivated by the SLC90E46 when FERR_ goes high. If nFERR is not asserted when the port F0h is written, the nIGNNE signal is not asserted. During Reset: High-Z After Reset: High-Z During POS: High-Z
INTR	OD	**CPU Interrupt.** Interrupt request signal to the CPU. This is an open-drain output signal, it requires a pull-up resistor to the CPU voltage. During Reset: Low After Reset: Low During POS: Low
NMI	OD	**Non-Maskable Interrupt.** NMI is used to cause a non-maskable interrupt to the CPU. The SLC90E46 asserts NMI signal when either nSERR or nIOCHK is asserted. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bit in the NMI Status and Control Register are cleared by software. To determine the source of the interrupt, the handler must read this register. The NMI is reset by setting the corresponding NMI source enable/disable bit in the register. To enable NMI, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and RTC Address Register must be set to 0. During Reset: Low After Reset: Low During POS: Low
nSMI	OD	**System Management Interrupt.** nSMI is a synchronous output in response to enabled hardware and software events. During Reset: High-Z After Reset: High-Z During POS: High-Z
nSTPCLK	OD	**Stop Clock**. nSMI is a synchronous output in response to enabled hardware and software events. During Reset: High-Z After Reset: High-Z During POS: High-Z

NAME	TYPE	DESCRIPTION
CPURST	OD	**CPU Reset.** The SLC90E46 asserts CPURST during power up and when a hard reset sequence is initiated through the RC register. CPURST is driven active a minimum of 2 ms after PWROK is driven active or when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, the SLC90E46 resets its internal register (in both core and suspend wells) to their default states. During Reset: High-Z After Reset: Low During POS: Low
INIT	OD	**CPU Initialization.** The INIT signal is asserted when: (1) PCI Shut Down special cycle is decoded. (2) If nRCIN is asserted. (3) A write occurs to port 92h, bit0. (4) The System Reset bit in the Reset Control register is set to 0, and the Reset CPU bit toggles from 0 to 1 to trigger a soft reset. When asserted, INIT remains asserted for approximately 64 PCI clocks before being de-asserted. During Reset: Low After Reset: Low

3.7. Clocks

NAME	TYPE	DESCRIPTION
PCICLK	I	**PCI Clock.** This is a clock signal provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK , and all timing parameters are defined with respect to the edge. The signal has to keep active, even if the PCI bus clock is not active.
OSC	I	**14.31818 MHz Clock.** Clock signals used by the internal 8254 timer. This clock signal may be stopped during suspend mode.
RTCX1, RTCX2	IO	**RTC Crystal Inputs.** These pins are connected directly to a 32.768KHz crystal. External capacitors are required. These crystal signals are required at all time.
CLK48	I	**48 MHz Clock.** Clock signal for the internal USB host controller. This clock signal may be stopped during suspend modes.
SUSCLK	O	**Suspend Clock.** This is a 32.768KHz clock outputted to the North Bridge for maintenance of DRAM refresh during suspend modes. This signal is stopped during Suspend-to-Disk mode. During Reset: Running After Reset: Running During POS: Running
SYSCLK	O	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is derived by dividing PCICLK by 4. During Reset: Running After Reset: Running During POS: Low

3.8. IDE Signals - Function 1

NAME	TYPE	DESCRIPTION
PDD[15-0]	I/O	**Primary Disk Data.** These are data bus for transferring data to or from the IDE device. When the IDE controller is configured to support both primary and secondary channels, these signals are connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, these signals are connected to the primary 0 connector. During Reset: High-Z After Reset: Undefined During POS: PDD

NAME	TYPE	DESCRIPTION
PDA[2-0]	O	**Primary Disk Address.** These signals select which byte, either ATA block or control block, is being accessed. When the IDE controller is configured to support both primary and secondary channels, these signals are connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, these signals are connected to the primary 0 connector. During Reset: High-Z After Reset: Undefined During POS: PDA
nPDCS1	O	**Primary Disk Chip Select for 100 Address Range.** Chip select signal for ATA command register block. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector. During Reset: High After Reset: High During POS: High
nPDCS3	O	**Primary Disk Chip Select for 300 Address Range.** Chip select signal for control register block. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector. During Reset: High After Reset: High During POS: High
nPDIOR	O	**Primary Disk IO Read.** Disk read command to the IDE device indicating that it may drive data onto the PDD[15-0] lines. Data is latched on the rising edge of nPDIOR. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector. During Reset: High After Reset: High During POS: High

NAME	TYPE	DESCRIPTION
nPDIOW	O	**Primary Disk IO Write.** Disk Write command to the IDE device indicating that it may latch data from the PD.[15-0] lines. Data is latched by the IDE device on the rising edge of nPDIOW. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector. During Reset: High After Reset: High During POS: High
PDDREQ	I	**Primary Disk DMA Request.** This signal is driven by the IDE device to request for a data transfer to or from the IDE device during PCI bus master IDE operating mode. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector.
nPDDACK	O	**Primary Disk DMA Acknowledge.** This signal is connected to the nDMACK signal of the IDE device. It is asserted by the SLC90E46 to indicate that a given data transfer cycle, assertion of nPDIOR or nPDIOW, is a DMA data transfer cycle. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector. During Reset: High After Reset: High During POS: High
PIORDY	I	**Primary IO Channel Ready.** This signal is driven by the IDE device IORDY signal. This is a schmitt triggered input. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the primary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 0 connector.

NAME	TYPE	DESCRIPTION
SDD[15-0]	I/O	**Secondary Disk Data.** These are data bus for transferring data to or from the IDE device. When the IDE controller is configured to support both primary and secondary channels, these signals are connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, these signals are connected to the primary 1 connector. During Reset: High-Z After Reset: Undefined During POS: SDD
SDA[2-0]	O	**Secondary Disk Address.** These signals select which byte, either ATA block or control block, is being accessed. When the IDE controller is configured to support both primary and secondary channels, these signals are connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, these signals are connected to the primary 1 connector. During Reset: High-Z After Reset: Undefined During POS: SDA
nSDCS1	O	**Secondary Disk Chip Select for 100 Address Range.** Chip select signal for ATA command register block. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector. During Reset: High After Reset: High During POS: High
nSDCS3	O	**Primary Disk Chip Select for 300 Address Range.** Chip select signal for control register block. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector. During Reset: High After Reset: High During POS: High

NAME	TYPE	DESCRIPTION
nSDIOR	O	**Secondary Disk IO Read.** Disk read command to the IDE device indicating that it may drive data onto the SDD[15-0] lines. Data is latched on the rising edge of nSDIOR. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector. During Reset: High After Reset: High During POS: High
nSDIOW	O	**Secondary Disk IO Write.** Disk Write command to the IDE device indicating that it may latch data from the SDD[15-0] lines. Data is latched by the IDE device on the rising edge of nSDIOW. When the IDE controller is configured to support both primary and secondary, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector. During Reset: High After Reset: High During POS: High
SDDREQ	I	**Secondary Disk DMA Request.** This signal is driven by the IDE device to request for a data transfer to or from the IDE device during PCI bus master IDE operating mode. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector.
nSDDACK	O	**Secondary Disk DMA Acknowledge.** This signal is connected to the nDMACK signal of the IDE device. It is asserted by the SLC90E46 to indicate that a given data transfer cycle, assertion of nSDIOR or nSDIOW, is a DMA data transfer cycle. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector. During Reset: High After Reset: High During POS: High

NAME	TYPE	DESCRIPTION
SIORDY	I	**Secondary IO Channel Ready.** This signal is driven by the IDE device IORDY signal. This is a schmitt triggered input. When the IDE controller is configured to support both primary and secondary channels, this signal is connected to the secondary IDE connector. When the IDE controller is configured to support primary 0 and primary 1 devices, this signal is connected to the primary 1 connector.

3.9. USB Signals - Function 2

NAME	TYPE	DESCRIPTION
nOC[1-0]	I	**Over-Current Detect.** These signals are used to monitor the status of the USB power supply lines. Once an over-current signal is asserted, the corresponding USB port is disabled.
USBP0+, USBP0-	I/O	**Serial Bus Port 0.** This signal pair is the differential data signal for USB port 0. During Reset: High-Z After Reset: High-Z During POS: High-Z
USBP1+, USBP1-	I/O	**Serial Bus Port 1.** This signal pair is the differential data signal for USB port 1. During Reset: High-Z After Reset: High-Z During POS: High-Z

3.10. Power Management Signals - Function 3

NAME	TYPE	DESCRIPTION
LID / GPI10	I	**LID Input.** This signal is used to monitor the display lid opening and closing of a notebook computer. The SLC90E46 can detect either high to low transition or low to high transition, and generates an nSMI if enabled. **GPI10.** This pin can be used as a general purpose input if the LID function is not used.
nSMBALER T/GPI11	I	**SMBus Alert.** This signal is used by the SMBus logic to generate an interrupt (SMI or IRQ) or power management resume event if enabled. **GPI11.** This pin can be used as an general purpose input if it is not used as nSMBALERT.
nRI/ GPI12	I	**Ring Indicate.** This is an input signal monitored by the power management logic, most typically used as wake up signal from a modem. **GPI12.** This pin can be used as an general purpose input if Ring detection is not needed.

NAME	TYPE	DESCRIPTION
nPWRBTN	I	**Power Button.** This is an external system event monitored by the power management logic. It is most typically used as a system on/off button or switch..
nBATLOW/ GPI9	I	**Battery Low Indicate.** Indicates that battery power is low. The SLC90E46 can be programmed to prevent from resume when nBATLOW is active. **GPI9.** This pin can be used as an general purpose input if nBATLOW detection is not needed.
nTHRM/ GPI8	I	**Thermal Detect.** External hardware logic can assert this signal to force the system to enter hardware clock throttling mode, if enabled. **GPI8.** This pin can be used as an general purpose input if this function is not needed.
nEXTSMI	I/OD	**External SMI.** This is a falling edge triggered input to the SLC90E46 requesting the system to enter SMM mode. nEXTSMI is an asynchronous input to the SLC90E46. When the setup and hold time are met the nEXTSMI is only required to be asserted for one PCICLK. Once de-asserted, it must remain de-asserted for at least 4 PCICLKs in order to allow the edge detection logic to reset. The SLC90E46 may assert the nEXTSMI signal in response to nSMI activation detected from the Serial IRQ function. A pull-up resistor is required.
NPCIREQ [A-D]	I/O	**PCI Request.** PCI Master request signals monitored by the power management logic.
nCPU_STP/ GPO14	O	**CPU Clock Stop Command.** This signal is connected to the clock generator to disable the host clock outputs. **GPO14.** This pin can be used as a general purpose output if host clock control is not needed. During Reset: High After Reset: High During POST: Low
nPCI_STP/ GPO18	O	**CPU Clock Stop Command.** This signal is connected to the clock generator to disable the host clock outputs. **GPO18.** This pin can be used as a general purpose output if host clock control is not needed. During Reset: High After Reset: High During POST: Low
nRSMRST	I	**Resume Reset.** It is used to reset the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBCLK	I/O	**SMBus Clock.** SMBus clock to synchronize data transfer on SMBus. During Reset: High-Z After Reset: High-Z During POS: High-Z
SMBDATA	I/O	**SMBus Data.** Serial data line to transfer data on SMBus. During Reset: High-Z After Reset: High-Z During POS: High-Z

NAME	TYPE	DESCRIPTION
nSUSA	O	**Suspend Plane A Control.** Suspend state power plane control signal, primarily used to control the primary power plane. This signal is asserted in all supported Suspend states, including POS, STR and STD states. During Reset: Low After Reset: High During POS: Low
nSUSB/ GPO15	O	**Suspend Plane B Control.** Suspend state power plane control signal, primarily used to control the secondary power plane. This signal is asserted during STR and STD states. **GPO15.** This pin can be used as a general purpose output if the power plane control is not needed. During Reset: Low After Reset: High During POS: High /GPO
nSUSC/ GPO16	O	**Suspend Plane C Control.** Suspend state power plane control signal, primarily used to control the tertiary power plane. This signal is asserted during STD state. **GPO16.** This pin can be used as a general purpose output if the power plane control is not needed. During Reset: Low After Reset: High During POS: High / GPO
nSUS_STAT 1/GPO20	O	**Suspend Status 1.** This signal typically connects to the North Bridge to indicate, when active, that the system may stop the host clock. This signal is asserted during StopClock mode, and all suspend states. **GPO20.** If the function is not used, this pin can be used as a general purpose output. During Reset: Low After Reset: High During POS: Low / GPO
nSUS_STAT 2/GPO21	O	**Suspend Status 2.** This signal typically connects to the other system peripherals and is used to provide status on system suspend state. This signal is asserted during POS, STR, and STD suspend states. **GPO21.** If the function is not used, this pin can be used as a general purpose output. During Reset: Low After Reset: High During POS: Low / GPO
ZZ/ GPO19	O	**L2 PBSRAM Low-Power Mode Command.** This signal is connected to the L2 PBSRAM to enable low-power mode when the SLC90E46 places the CPU into StopClock state. **GPO19.** This pin can be used as a general purpose output if this function is not required. During Reset: Low After Reset: Low During POST: High-Z

3.11. Other System and Test Signals

NAME	TYPE	DESCRIPTION
CONFIG1	I	**Configure 1.** Currently, this is a N.C. pin. The SLC90E46 supports Pentium and compatible processors at this time.
CONFIG2	I	**Configure 2.** When CONFIG2=1, the SLC90E46 will decode FFFF0000h-FFFFFFFFh with subtractive decode timings only. When CONFIG2=0, the SLC90E46 will positively decode FFFF0000h-FFFFFFFFh range. This input value must remain static and may not dynamically change during system operations.
PWROK	I	**Power OK.** When asserted, this signal indicates that power and PCICLK has been stable for at least 1ms. When negated, the SLC90E46 asserts CPURST, nPCIRST and RSTDRV. When asserted, the SLC90E46 de-asserts asserts CPURST, nPCIRST and RSTDRV.
SPKR	O	**Speaker Out.** This is the output of timer 2 and is internally "ANDed" with port 61h bit 1 to provide the speaker data out. During Reset: Low After Reset: Low During POS: Last state.
nTEST	I	**Test Mode Select. Test In.** This pin should be pulled up to VCC-SUS with an external pull-up during normal operation

3.12. General Purpose Input and Output Signals

NAME	TYPE	DESCRIPTION
GPI[x]	I	**General Purpose Inputs.** These input signals can be monitored through Function 3 IO registers.
GPO[x]	O	**General Purpose Outputs.** These signals can be controlled by Function 3 IO registers. If a GPO pin is not multiplexed with another signal or default to GPO, then its state after reset is low. If the GPO defaults to another signal, then it defaults to that signal's state after reset. The GPO pins which default to GPO will remain stable after reset. The others may toggle due to system boot or power control sequencing after reset before they are programmed as GPOs. The GPO[8] signal will be driven low upon removal of power from the SLC90E46 core power plane. All other GPO signals will be invalid. During Reset: Undefined. After Reset: Undefined During POS: GPO

Dedicated & Multiplexed GPI Signals

Signal	Multiplexed With	Default Function	Configuration Register	NOTES
GPI0	nIOCHK	*GPI*	Bit 0 of GENCFG	Functions as GPI when EIO bus mode is selected
nGPI1		*GPI*		Dedicated GPI signal pin. Active low as power management signal pin.
GPI[2-4]	nREG[A-C]	*GPI*	Bits [8-10] of GENCFG	Muxed with PC/PCI request signals. Can be individually enabled when the pin is not served as PC/PCI request input.
GPI5	nAPICREQ	*GPI*	Bit 8 of XBCS	Functions as GPI when external APIC is not used.
GPI6	nIRQ8	*GPI*	Bit 14 of GENCFG	Functions as GPI when not using external RTC or APIC.
GPI7	SERIRQ	*GPI*	Bit 16 of GENCFG	Functions as GPI when not using SERIRQ protocol.
GPI8	nTHRM	nTHRM	Bit 23 of GENCFG	Functions as GPI when disable the nTHRM function.
GPI9	nBATLOW	nBATLOW	Bit 24 of GENCFG	Functions as GPI when disable the battery low function.
GPI10	nLID	nLID	Bit 25 of GENCFG	Functions as GPI when disable the LID feature.
GPI11	nSMBALERT	nSMBALERT	Bit 15 of GENCFG	Functions as GPI when not using the SMBALERT feature.
GPI12	nRI	nRI	Bit 27 of GENCFG	Functions as GPI when the ring indicator feature is not used.
GPI [13-21]		*GPI*		Dedicated GPI signal pins.

Dedicated & Multiplexed GPO Signals

Signal	Multiplexed With	Default Function	Configuration Register	NOTES
GPO0		*GPO*		Dedicated GPO signal pin.
GPO[1-7]	LA[17-23]	*GPO*	Bit 0 of GENCFG	Functions as GPO when EIO bus mode is selected.
GPO8		*GPO*		Dedicated GPO signal pin. GPO8 will be driven low upon power removal from core power plane.
GPO[9-11]	nGNT[A-C]	*GPO*	Bits[8-10] of GENCFG	Muxed with PC/PCI grant signals. Can be individually enabled when the pin is not served as PC/PCI grant output.
GPO12	nAPICACK	*GPO*	Bit 8 of XBCS	Functions as GPO when not using external APIC.
GPO13	nAPICCS	*GPO*	Bit 8 of XBCS	Functions as GPO when not using external APIC.

Signal	Multiplexed With	Default Function	Configuration Register	NOTES
GPO14	IRQ0	*GPO*	Bit 8 of XBCS	Functions as GPO when not using external APIC.
GPO15	nSUSB	nSUSB	Bit 17 of GENCFG	Functions as GPO when disable the nSUSB function.
GPO16	nSUSC	nSUSC	Bit 17 of GENCFG	Functions as GPO when disable the nSUSC function.
GPO17	nCPU_STP	nCPU_STP	Bit 18 of GENCFG	Functions as GPO when disable the CPU clock control.
GPO18	nPCI_STP	nPCI_STP	Bit 19 of GENCFG	Functions as GPO when disable the PCI clock control.
GPO19	ZZ	ZZ	Bit 20 of GENCFG	Functions as GPO when disable the SRAM power control
GPO20	nSUS_STAT1	nSUS_STAT1	Bit 21 of GENCFG	Functions as GPO when disable the nSUS_STAT1 func.
GPO21	nSUS_STAT2	nSUS_STAT2	Bit 22 of GENCFG	Functions as GPO when disable the nSUS_STAT2 func.
GPO22	nXDIR	nXDIR	Bit 28 of GENCFG	Functions as GPO when not using Xbus transceiver.
GPO23	nXOE	nXOE	Bit 28 of GENCFG	Functions as GPO when not using Xbus transceiver.
GPO24	nRTCCS	nRTCCS	Bit 29 of GENCFG	Functions as GPO when not using external RTC, or the external RTC can self decode.
GPO25	RTCALE	RTCALE	Bit 30 of GENCFG	Functions as GPO when not using external RTC, or the external RTC can self decode.
GPO26	nKBCCS	nKBCCS	Bit 31 of GENCFG	Functions as GPO when the external KBC can self decode.
GPO[27-28]		*GPO*		Dedicated GPO signal pins.
GPO29	IRQ9	*GPO*	Bit 8 of XBCS	Functions as GPO when not using external APIC.
GPO30		*GPO*		Dedicated GPO signal pins.

3.13. Power and Ground Signals

NAME	TYPE	DESCRIPTION
VCC	V	**Main Voltage Supply.** These pins are the primary voltage supply for the SLC90E46 core and IO periphery and must be tied to 3.3V.
VCC-RTC	V	**RTC Well Voltage Supply.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC-SUS	V	**Suspend Well Voltage Supply.** These pins are the primary voltage supply for the suspend logic and IO signals and must be tied to 3.3V.
VCC-USB	V	**USB Voltage Supply.** This pin is the supply voltage for the USB I/O buffers and must be tied to 3.3V.
VSS	V	**Main Ground.** These pins are the primary ground for the SLC90E46.
VSS-USB	V	**USB Ground.** This pin is the ground for the USB I/O buffers.

4. SLC90E46 - PCI/ISA Bridge Register Description

The SLC90E46 internal registers are organized into four functions - ISA bridge with other AT compatibility logic, IDE Controller, USB Host Controller, and Power Management Controller. Each function has its registers divided into a set of PCI configuration registers and one or more register sets located in the system I/O space.

Some of the SLC90E46 registers contain reserved bits. Software must ensure that the value of reserved bit positions are preserved. That is, Software must first read the value of the reserved bits, merge the value with the new values for the other bits and then write back to the register.

Upon reset, the SLC90E46 sets its internal registers to predetermined default states, which represents the minimum functionality feature set required for the BIOS to bring up the system. It is the responsibility of the BIOS to properly program the configuration registers to achieve optimal system performance.

The following notation is used to describe register access attributes:

RO Read Only. Writes have no effect.
WO Write Only. Reads have no effect.
R/W Read/Write. The register can be read or written.
R/WC Read/Write Clear. A register bit with this attribute can be read and written. However, a write of a 1 clears the corresponding bit (sets to 0) and a write of a 0 has no effect.

4.1. PCI/ISA Bridge Register Mapping

4.1.1. PCI Configuration Register Mapping Table (Function 0)

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
00-01h	VID	Vendor Identification	RO
02-03	DID	Device Identification	RO
04-05	PCICMD	PCI Command Register	R/W
06-07	PCISTS	PCI Status Register	R/W
08	RID	Revision ID	RO
09-0B	CLASSCODE	Class Code	RO
0C-0D		Reserved	
0E	HEDT	Header Type	RO
0F-4B		Reserved	
4C	IORT	ISA I/O Recovery Timer	R/W
4D		Reserved	
4E-4F	XBCS	X-Bus Chip Select	R/W
50-5F		Reserved	
60-63	PIRQRC[A:D]	PIRQx Route Control	R/W
64	SERIRQC	Serial IRQ Control	R/W
65	FDMA	Type-F DMA Control	R/W
65-68		Reserved	
69	TOM	Top of Memory	R/W

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
6A-75		Reserved	
76-77	MBDMA[1:0]	Motherboard Device DMA Control	R/W
78-7F		Reserved	
80	APICBASE	APIC Base Address Relocation	R/W
81		Reserved	
82	DLC	Deterministic Latency Control	R/W
83-8F		Reserved	
90-91	PDMACFG	PCI DMA Configuration	R/W
92-95	DDMABASE	Distributed DMA Slave Base Pointer	R/W
96-AF		Reserved	
B0-B3	GENCFG	General Configuration	R/W
B4-CA		Reserved	
CB	RTCCFG	Real Time Clock Configuration	R/W
CC-FF		Reserved	

4.1.2. IO Space Register Mapping Table (Function 0)

ADDRESS	ALLIASED ADDRESSES	ACCESS TYPE	ACCESSES	REGISTER NAME
0000h	0010h	R/W	PCI	DMA1 CH0 Base and Current Address
0001h	0011h	R/W	PCI	DMA1 CH0 Base and Current Count
0002h	0012h	R/W	PCI	DMA1 CH1 Base and Current Address
0003h	0013h	R/W	PCI	DMA1 CH1 Base and Current Count
0004h	0014h	R/W	PCI	DMA1 CH2 Base and Current Address
0005h	0015h	R/W	PCI	DMA1 CH2 Base and Current Count
0006h	0016h	R/W	PCI	DMA1 CH3 Base and Current Address
0007h	0017h	R/W	PCI	DMA1 CH3 Base and Current Count
0008h	0018h	R/W	PCI	DMA1 status (Read) and command (Write) register.
0009h	0019h	WO	PCI	DMA1 Request
000Ah	001Ah	WO	PCI	DMA1 Write Single Mask Bit
000Bh	001Bh	WO	PCI	DMA1 Channel Mode
000Ch	001Ch	WO	PCI	DMA1 Clear Byte Pointer
000Dh	001Dh	WO	PCI	DMA1 Master Clear
000Eh	001Eh	WO	PCI	DMA1 Clear Mask
000Fh	001Fh	R/W	PCI	DMA1 Read/Write All Mask Bits
0020h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	R/W	PCI/ISA	Interrupt Controller I: Initialization Command Word 1, Operational Command Word 2, Operational Command Word 3
0021h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	R/W	PCI/ISA	Interrupt Controller I: Initialization Command Word 2, Initialization Command Word 3, Initialization Command Word 4, Operational Command Word 1

ADDRESS	ALLIASED ADDRESSES	ACCESS TYPE	ACCESSES	REGISTER NAME
0040h	0050h	R/W	PCI/ISA	Timer Count - Counter 0 Timer Status - Counter 0 (Read Only)
0041h	0051h	R/W	PCI/ISA	Timer Count - Counter 1 Timer Status - Counter 1 (Read Only)
0042h	0052h	R/W	PCI/ISA	Timer Count - Counter 2 Timer Status - Counter 2 (Read Only)
0043h	0053h	R/W	PCI/ISA	Timer Control Word
0060h		RO	PCI/ISA	Reset Xbus IRQ12/M and IRQ1
0061h	63h, 65h, 67h	R/W	PCI/ISA	NMI Status and Control. Read/Write accesses are always broadcast to ISA bus.
0070h	72h[1], 74h, 76h	WO	PCI/ISA	NMI Enable. Read/Write accesses are always broadcast to ISA bus.
0070h	72h[1], 74h, 76h	WO	PCI/ISA	RTC Index. Read/Write accesses are always broadcast to ISA bus.
0071h	73h[2], 75h, 77h	R/W	PCI/ISA	RTC Data. Read/Write accesses are always broadcast to ISA bus.
0072h		R/W	PCI/ISA	RTC Extended Index.
0073h		R/W	PCI/ISA	RTC Extended Data.
0080h[3,4]	0090h	R/W	PCI/ISA	DMA1 Page (Reserved)
0081h[4]	0091h	R/W	PCI/ISA	DMA1 CH2 Low Page.
0082h[4]		R/W	PCI/ISA	DMA1 CH3 Low Page.
0083h[4]	0093h	R/W	PCI/ISA	DMA1 CH1 Low Page.
0084h[3,4]	0094h	R/W	PCI/ISA	DMA1 Page (Reserved).
0085h[3,4]	0095h	R/W	PCI/ISA	DMA1 Page (Reserved).
0086h[3,4]	0096h	R/W	PCI/ISA	DMA1 Page (Reserved).
0087h[4]	0097h	R/W	PCI/ISA	DMA1 CH0 Low Page.
0088h[3,4]	0098h	R/W	PCI/ISA	DMA Page (Reserved).
0089h[4]	0099h	R/W	PCI/ISA	DMA2 CH2 Low Page (CH6).
008Ah[4]	009Ah	R/W	PCI/ISA	DMA2 CH3 Low Page (CH7).
008Bh[4]	009Bh	R/W	PCI/ISA	DMA2 CH1 Low Page (CH5).
008Ch[3,4]	009Ch	R/W	PCI/ISA	DMA2 Page (Reserved).
008Dh[3,4]	009Dh	R/W	PCI/ISA	DMA2 Page (Reserved).
008Eh[3,4]	009Eh	R/W	PCI/ISA	DMA2 Page (Reserved).
008Fh[4]	009Fh	R/W	PCI/ISA	DMA2 Low Page Refresh.
0092h		R/W	PCI/ISA	Port 92
00A0h	A4h, A8h, Ach, B0h, B4h, B8h, BCh	R/W		Interrupt Controller II: Initialization Command Word 1, Operational Command Word 2, Operational Command Word 3
00A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	R/W	PCI/ISA	Interrupt Controller II: Initialization Command Word 2, Initialization Command Word 3, Initialization Command Word 4, Operational Command Word 1

ADDRESS	ALLIASED ADDRESSES	ACCESS TYPE	ACCESSES	REGISTER NAME
00B2h		R/W	PCI	Advanced Power Management Control
00B3h		R/W	PCI	Advanced Power Management Control
00C0h	00C1h	R/W	PCI	DMA2 CH0 Base and Current Address
00C2h	00C3h	R/W	PCI	DMA2 CH0 Base and Current Count
00C4h	00C5h	R/W	PCI	DMA2 CH1 Base and Current Address
00C6h	00C7h	R/W	PCI	DMA2 CH1 Base and Current Count
00C8h	00C9h	R/W	PCI	DMA2 CH2 Base and Current Address
00CAh	00CBh	R/W	PCI	DMA2 CH2 Base and Current Count
00CCh	00CDh	R/W	PCI	DMA2 CH3 Base and Current Address
00CEh	00CFh	R/W	PCI	DMA2 CH3 Base and Current Count
00D0h	00D1h	R/W	PCI	DMA2 status (Read) and command (Write) register.
00D2h	00D3h	WO	PCI	DMA2 Request
00D4h	00D5h	WO	PCI	DMA2 Write Single Mask Bit
00D6h	00D7h	WO	PCI	DMA2 Channel Mode
00D8h	00D9h	WO	PCI	DMA2 Clear Byte Pointer
00DAh	00DBh	WO	PCI	DMA2 Master Clear
00DCh	00DDh	WO	PCI	DMA2 Clear Mask
00DEh	00DFh	R/W	PCI	DMA2 Read/Write All Mask Bits
00F0h		WO	PCI/ISA	Coprocessor Error. Read/Write accesses are always broadcast to ISA bus.
04D0h		R/W	PCI/ISA	Interrupt Controller I - Edge / Level Control
04D1h		R/W	PCI/ISA	Interrupt Controller II - Edge / Level Control
0CF9h		R/W	PCI	Reset Control.

Notes:

1. Not aliased to 0072h or 0076h if extended RAM (RTC) enabled.
2. Not aliased to 0073h or 0077h if extended RAM (RTC) enabled.
3. Write accesses to these locations are broadcast to the ISA bus. Read accesses are not. If programmed in the ISA I/O Recovery Timer Register, the SLC90E46 does not alias the entire 90h-9Fh address range. These locations are considered ISA Bus register locations and not SLC90E46 registers.
4. The SLC90E46 does not support Distributed DMA for the 90h range, even if aliasing is enabled.

4.2. PCI/ISA Bridge PCI Register Description (Function 0)

This section describes in detail the registers associated with the SLC90E46 PCI-to-ISA bridge function.

4.2.1. VID Vendor Identification Register

Offset Address: 00 - 01h
Default Value: 10B8h
Access: Read Only

This is a 16 bit PCI Vendor ID assigned to SMSC.

4.2.2. DID Device Identification Register

Offset Address: 02 - 03h
Default Value: 9460h
Access: Read Only

This is the PCI device ID of the SLC90E46.

4.2.3. PCICMD PCI Command Register

Offset Address: 04 - 05h
Default Value: 07h
Access: Read/Write

This register provides basic control over the SLC90E46's ability to respond to PCI cycles.

BIT	FUNCTION
15-10	Reserved.
9	Fast Back-to-Back: not implemented, hardwired to 0..
8	**nSERR Enable**: **When enabled (and DLC register, bit 3 =1),** a delayed transaction time-out causes the SLC90E46 to assert nSERR.
7-5	Reserved. Read as 0
4	Postable Memory Write Enable. This bit is hardwired to 0.
3	**Special Cycle Enable**: When enabled (set to 1), the SLC90E46 recognizes all PCI special cycles. 0: the SLC90E46 ignores all PCI Special Cycles.
2	Bus Master Enable: This bit is hardwired to a 1 (always enabled).
1	Memory Access Enable: The SLC90E46 does not support disabling function 0 response to PCI memory cycles. Always 1.
0	IO Access Enable: The SLC90E46 does not support disabling its function 0 response to PCI I/O cycles. This bit is hardwired to a 1.

4.2.4. PCISTS PCI Status Register

Offset Address: 06 - 07h
Default Value: 0280h
Access: Read/Write

BIT	FUNCTION
15	Detected Parity Error. Not implemented, hardwired to a 0.
14	**Signaled nSERR Status: When the SLC90E46 asserts** the nSERR signal (delay transaction time out), this bit is set to 1. Software can set this bit to a 0 by writing a 1 to it.
13	**Master Abort Status:** When the SLC90E46, as a master (for function 0), generates a master abort, this bit is set to 1. To reset this bit, write a 1 to it.
12	**Received Target Abort Status**: When the SLC90E46 is a master on the PCI bus (for function 0) and receives a target abort, this bit is set to 1. To reset the bit, write a 1 to it.
11	**Signaled Target Abort:** This bit is set when the SLC90E46 ISA bridge function is targeted with a transaction that the SLC90E46 terminates with a target abort. To reset this bit, write a 1 to the bit.
10-9	nDEVSEL timing: Always 01 to select "medium" timing, which is two PCI clocks after the assertion of nFRAME, when the SLC90E46 asserts nDEVSEL as a PCI target.
8	Parity Detected: Always 0, not implemented.
7	Fast Back-to-Back: RO. This bit indicates to the PCI master that the SLC90E46 as a target is capable of accepting fast back-to-back transaction.
6-0	Reserved.

4.2.5. RID Revision Identification Register

Offset Address: 08h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
7-0	Hardwired to the revision number, which is set to 00 as the initial number.

4.2.6. CLASSC Class Code Register

Offset Address: 09 - 0Bh
Default Value: 060100h
Access: Read Only

BIT	FUNCTION
23-16	Base Class Code: always 06 indicating that the SLC90E46 is a bridge device.
15-8	Sub-Class Code: PCI-to-ISA bridge = 01h Other bridge device (Positive Decode Bridge) = 80h. This value depends on the programming of bit 1 of the General Configuration Register. If programmed as a subtractive decode bridge (default), this field will read 01h. If programmed as an positive decode bridge, this will read 80h.
7-0	Programming Interface: 00, no interface is defined.

4.2.7. HEDT Header Type Register

Offset Address: 0Eh
Default Value: 80h
Access: Read

BIT	FUNCTION
7-0	(Device Type) 80h= multi-function device.

4.2.8. IORT ISA I/O Recovery Timer Register

Offset Address: 4Ch
Default Value: 4Dh
Access: Read/Write

This register is used to define the actual recovery delay between CPU or PCI master originated 8 bit or 16 bit IO cycles to the ISA bus. The default delay is 3.5 SYSCLKs between back-to-back 8 and 16 bit IO cycles on the ISA Bus. The delay is measured from the rising edge of the IO command to the falling edge to the next IO command.

BIT	FUNCTION
7	**DMA Reserved Page Register Aliasing Control (DMAAC):** When set to a 0, the SLC90E46 aliases IO accesses in the 90-9Fh range to the 80-8Fh range. In this case, the SLC90E46 only forwards (*broadcasts*) write accesses to the 90-9Fh to the ISA bus. ISA master accesses to the 90-9Fh range are forwarded to the PCI bus. When this bit is a 1, aliasing is disabled for the address range 90-9Fh. The SLC90E46 forwards read and write accesses to the ISA bus. ISA master accesses to the 90-9Fh range are ignored by the SLC90E46. The port 92h is always a distinct register in the 90-9Fh range and is never forwarded from the PCI bus to the ISA bus. It is also never forwarded from ISA to PCI or to the internal Port 92h register. The SLC90E46 does not support aliasing of the 90h range for the Distributing DMA function, even if aliasing is enabled.
6	**8 bit IO recovery enable.** When set to a 1, enables the recovery time programmed in bits[5-3]. When set to a 0, disables programmed recovery times and uses the default timing of 3.5 SYSCLKs.
5-3	**8 bit IO recovery times (actual recovery clock counts) when bit 6 is set to 1.** 000: 11.5 001: 4.5 010: 5.5 011: 6.5 100: 7.5 101: 8.5 110: 9.5 111: 10.5
2	**16 bit IO recovery enable.** When set to a 1, enables the recovery time programmed in bits[1-0]. When set to a 0, disables programmed recovery times and uses the default timing of 3.5 SYSCLKs.
1-0	**16 bit IO recovery times (actual recovery clock counts) when bit 2 is set to 1.** 01: 4.5 10: 5.5 11: 6.5 00: 7.5.

4.2.9. XBCS X-Bus Chip Select Register

Offset Address: 4E-4Fh
Default Value: 03h
Access: Read/Write.

This register enables or disables accesses to the RTC, keyboard controller, I/O APIC, a secondary controller, and BIOS. Disabling any of these accesses prevents the assertion of the chip select and X-Bus output enable control signals for that device.

BIT	FUNCTION
15-11	Reserved.
10	**Embeded Microcontroller Address Decode Enable**. 1=Enable nMCCS and positive PCI decode for address locations 62h and 66h. 0=Disable nMCCS and positive PCI decode for these two locations.
9	**1Meg Extended BIOS enable.** When this bit is a 1, PCI master accesses to locations FFF00000h-FFF7FFFFh are forwarded to ISA and result in generation of nBIOSCS and nXOE. When forwarding the additional 512KB region, the PCI address A[23:20] are propagated to the ISA LA[23:20] lines as all 1's. ISA memory should not present in this region (0F00000 -0F7FFFFh) to avoid contention. When bit 9 is a 0, the SLC90E46 does not generate nBIOSCS or nXOE for accesses to this memory region.
8	**APIC Chip Select**. When set to a 1, nAPICCS is asserted for PCI memory accesses to the programmable IO APIC region. The cycle is forwarded to the ISA bus. The default IO APIC addresses are memory FEC0_0000h and FEC0_0010h, which can be relocated via the APIC Base Address Relocation Register. When set to a 0, the PCI memory cycle which accesses to the programmable IO APIC region is ignored and nAPICCS and nXOE are not generated. In either case, the SLC90E46 does not assert nAPICCS for ISA-originated cycles. This bit is also used to select the actual function on the following multiplexed pins: nAPICREQ, nAPICACK, nAPICCS, and IRQ0 signals. When bit 8 is 0, these signals become GPIO pins.
7	**Extended BIOS Enable.** When set to a 1, PCI master accesses to locations FFF80000h-FFFDFFFFh are forwarded to ISA and result in generation of nBIOSCS and nXOE. When forwarding this 384KB region at the top of 4GBytes, the PCI address A[23:20] are propagated to the ISA LA[23:20] lines as all 1's. ISA memory should not present in this region (0F80000 -0FDFFFFh) to avoid contention. When set to a 0, the SLC90E46 does not generate nBIOSCS and nXOE for accesses to this memory range.

BIT	FUNCTION
6	**Lower BIOS Enable.** When set to a 1, PCI master or ISA master accesses to the 0E0000-0EFFFFh range or FFFE0000-FFFEFFFFh result in the generation of nBIOSCS and nXOE. The PCI cycle's A[23:20] are propagated to the ISA LA[23:20] lines. ISA memory should not present in this region (0FE0000 -0FDEFFFh) to avoid contention. When this bit is set to 0, SLC90E46 does not generate nBIOSCS and nXOE when accesses to these ranges and does not forward the accesses to ISA bus.
5	**Coprocessor Error Function Enable.** When enabled, the nFERR input triggers the assertion of an internal IRQ13. nFERR is also used to gate the nIGNNE output.
4	**IRQ12/M Mouse Function Enable.** 1: Select Mouse Function. 0: Standard IRQ12 interrupt function.
3	**Port 61h Alias Enable.** When set to a 1, 63h, 65h and 67h are treated as alias addresses of 61h.
2	**nBIOSCS Write Protect Enable.** When set to a 1, the nBIOSCS is asserted for both BIOS memory read and write cycles in the decoded BIOS region. When set to a 0, nBIOSCS is asserted only in BIOS read cycle.
1	**nKBCCS Enable.** When set to a 1, nKBCCS and nXOE are asserted when IO ports 60h and 64h are accessed.
0	**nRTCCS/RTCALE Enable.** When set to a 1, enable nRTCCS/RTCALE and nXOE for accesses to address locations 70-77h. Set to a 0 disables nRTCCS/RTCALE and nXOE for these accesses.

BIOS Memory Spaces and The Control Bits

OPTIONAL BIOS MEMORY RANGE	DESCRIPTION	CONTROL BIT
000E0000 - 000EFFFFh FFFE0000 - FFFEFFFFh	Low BIOS Range	Bit 6 of XBCS
FFF00000 - FFF7FFFFh	1 Meg Extended BIOS Range (512K bytes)	Bit 9 of XBCS
FFF80000 - FFFDFFFFh	Extended BIOS Range (384K bytes)	Bit 7 of XBCS

4.2.10. PIRQRC[A:D] PIRQx Route Control Registers

Offset Address: 60h (nPIRQRCA) - 63h (nPIRQRCD)
Default Value: 80h
Access: Read/Write

These registers define the routing of the nPIRQ[A:D] signals to the IRQ inputs of the interrupt controller. Each nPIRQx can be independently routed to any one of the 11 interrupts. All four nPIRQx lines can be routed to the same IRQx input. The IRQ that is selected through bits [3:0] must be set to level sensitive mode in the corresponding ELCR register. The SLC90E46 always masks the corresponding IRQ signal to which a PIRQ signal is routed to avoid possible sharing problem between PCI and ISA interrupt signals.

BIT	FUNCTION
7	Interrupt Routing Enable. 0:Enable; 1:Disable.
6-4	Reserved. Read as 0s.
3-0	**Interrupt Routing**. When bit 7 is a 0, this field selects the routing of the PIRQx to one of the interrupt inputs of the interrupt controllers. 0000: Reserved 0001: Reserved 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Reserved 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Reserved 1110: IRQ14 1111: IRQ15

4.2.11. SERIRQC Serial IRQ Control Register

Offset Address: 64h
Default Value: 10h
Access: Read/Write

BIT	FUNCTION
7	Serial IRQ Enable. 1: Enable the Serial Interrupt function. Bit 16 in register offset B0h-B3h must also be set to a 1. 0: Disable the function.
6	Serial IRQ Mode Select. 1: The Serial Interrupt operates in Continuous mode. 0: The Serial Interrupt operates in Quiet mode.
5-2	Serial IRQ Frame Size. These bits select the frame size used by the Serial IRQ logic. The default is 0100b indicating a frame size of 21 (17+4). These bits are readable and writeable, however the only programmable value supported by the SLC90E46 is 0100b. All other frame sizes are not supported.
1-0	Start Frame Pulse width. These bits define the Start Frame pulse width generated by the Serial Interrupt control logic. 00: 4 clocks. 01: 6 clocks. 10: 8 clocks 11: Reserved.

4.2.12. FDMA Type-F DMA Control Register

Offset Address: 65h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7	Type-F DMA Buffer Enable. 1: Enable the 16-byte collection buffer for ISA master/DMA device' data transfer. 0: Disable the data collection feature.
6	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 7. 1: Enable. 0: Disable.
5	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 6. 1: Enable. 0: Disable.
4	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 5. 1: Enable. 0: Disable.
3	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 3. 1: Enable. 0: Disable.
2	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 2. 1: Enable. 0: Disable.
1	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 1. 1: Enable. 0: Disable.
0	Enable type-F timing, 3 SYSCLKs cycle, for DMA channel 0. 1: Enable. 0: Disable.

4.2.13. TOM Top of Memory Register

Offset Address: 69h
Default Value: 02h
Access: Read/Write

This register controls the forwarding of DMA or ISA master memory cycles to the PCI bus and sets the top of main memory accessible by ISA or DMA devices. In addition, this register controls the forwarding of ISA or DMA accesses to the lower BIOS range (E0000h-EFFFFh) and the 512-640Kbyte main memory region.

BIT	FUNCTION
7-4	**Top of Memory Accessible by the ISA Master/DMA devices.** The top of memory can be assigned in 1Mbyte increments from 1-16 Mbytes. ISA or DMA accesses within this range, and not in the memory hole region, are forwarded to PCI. 0000: 1 Mbytes 0001: 2 Mbytes 0010: 3 Mbytes 0011: 4 Mbytes 0100: 5 Mbytes 0101: 6 Mbytes 0110: 7 Mbytes 0111: 8 Mbytes 1000: 9 Mbytes 1001: 10 Mbytes 1010: 11 Mbytes 1011: 12 Mbytes 1100: 13 Mbyes 1101: 14 Mbytes 1110: 15 Mbytes 1111: 16 Mbytes Note if a 1Mbyte memory hole is created for the Host-to-PCI bridge chip between 15 and 16 Mbytes, this register should be set to 15 Mbytes.
3	**ISA/DMA Lower BIOS Region (E0000-EFFFFh) Forwarding (to PCI) Enable.** If this bit is a 1 and bit 6 of the XBCS register is a 0, ISA/DMA cycles which access lower BIOS region are forwarded to PCI. If this bit is a 0 and bit 6 of the XBCS register is a 0, no forwarded (always contained to ISA). Note that if the XBCS register bit 6 is a 1 (which enables the lower BIOS region), ISA/DMA accesses in this range are always contained to ISA.
2	**ISA/DMA 640-768K Memory Region (A0000-BFFFFh) Forwarding Enable.** 1: Enable, ISA/DMA cycles which access 640-768K memory region are forwarded to PCI. 0: Disable (contained to ISA).
1	**ISA/DMA 512K-640K Memory Region Forwarding Enable.** 1: Enable, ISA/DMA cycles which access 512-640K memory region are forwarded to PCI. 0: Disable (contained to ISA).
0	**Reserved**

4.2.14. MBDMA Motherboard device DMA Control Registers

Offset Address: 76h-77h
Default Value: 04h
Access: Read/Write

These registers are not defined.

4.2.15. APICBASE APIC Base Address Relocation Register

Offset Address: 80h
Default Value: 00h
Access: Read/Write

This register is used to modify the APIC base address. APIC is mapped in the memory space at the locations FEC0_xy00h and FEC0_xy10h (x=0-Fh, y=0, 4, 8, Ch). The value of y is defined by bits 1 and 0, and the value of x is defined by bits 5 to 2. Thus, the relocation register provides 1K byte address granularity (i.e. potentially up to 64 I/O APICs can be uniformly addresses in the memory space). The default base addresses of the I/O APIC unit are FEC0_0000h and FEC0_0010h.

BIT	FUNCTION
7	Reserved.
6	**A12Mask.** When set to a 1, address bit A12 is ignored allowing the nAPICCS signal to be generated for two consecutive I/O APIC address ranges. External logic is required to select individual I/O APICs by combining SA12 and nAPICCS. For example, if x y are 0 and A12Mask is a 1, nAPICCS is generated for addresses FEC0_0000h, FEC0_0010, as well as FEC0_1000h, FEC0_1010h. When this bit is a 0, nAPICCS is generated for one I/O APIC address range.
5-2	**X-Base Address.** Define the base address bits of A[15:12].
1-0	**Y-Base Address.** Define the base address bits of A[11:10].

4.2.16. DLC Deterministic Latency Control Register

Offset Address: 82h
Default Value: 00h
Access: Read/Write

This register enables and disables the Delayed Transaction function.

BIT	FUNCTION
7-4	**Reserved.**
3	**nSERR Generation Due To Delayed Transaction Time-out Enable.** 1: Enable. 0: Disable.
2	**USB Passive Release Enable.** No effect, dummy R/W register bit.
1	**Passive Release Enable.** Not effect. Passive Release is enabled through bit 7 of FDMA (function 0, offset 65h).
0	**Delayed Transaction Enable.** 1: Enable the Delayed Transaction mechanism as a PCI transaction target. 0: Disable.

4.2.17. PDMACFG PCI DMA Configuration Register

Offset Address: 90-91h
Default Value: 00h
Access: Read/Write

This register defines the type of DMA performed by a particular DMA channel. If a channel is programmed for Distributed DMA mode, the SLC90E46 does not respond to either the ISA DREQ signal or to the PC/PCI encoding for that channel.

BIT	FUNCTION
15-14	**DMA CH 7 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.
13-12	**DMA CH 6 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.
11-10	**DMA CH 5 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.
9-8	**Reserved**
7-6	**DMA CH 3 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.
5-4	**DMA CH 2 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.
3-2	**DMA CH 1 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.

BIT	FUNCTION
1-0	**DMA CH 0 Select.** Select the type of DMA performed on this channel. 00: Normal ISA DMA (default) 01: PC/PCI DMA 10: Distributed DMA 11: Reserved.

4.2.18. DDMABP Distributed DMA Slave Base Pointer Registers

Offset Address: 92-93h (CH0-3) 94-95h (CH5-7)
Default Value: 0000h
Access: Read/Write

These register pairs provide the base addresses for distributed DMA slave channel registers, one for each DMA controller. Bits 5 to 0 are reserved to provide access to a 64 byte IO space (16 bytes per channel). The channels are accessed using offset from base address as follows (Note that channel 4 is reserved and is not accessible).

BASE OFFSET	CHANNEL
00-0Fh	0,4
10-1Fh	1,5
20-2Fh	2,6
30-3Fh	3,7

BIT	FUNCTION
15-6	**Base Pointer**: IO address pointer to DMA Slave Channel registers, corresponds to PCI address AD[15:6].
5-0	**Reserved.** Read as 0.

4.2.19. GENCFG General Configuration Register

Offset Address: B0-B3h
Default Value: 0000h
Access: Read/Write

This register provides general system configuration for SLC90E46, including signal and GPIO selects, ISA / EIO select , IDE signal configuration and IDE signal enables.

BIT	FUNCTION
31	**nKBCCS / GPO26 Signal Pin Select:** 0: Select nKBCCS (default) 1: The pin is used as GPO26.
30	**RTCALE / GPO25 Signal Pin Select:** 0: Select nKBCCS (default) 1: The pin is used as GPO25.
29	**nRTCCS / GPO24 Signal Pin Select:** 0: Select nRTCCS (default) 1: The pin is used as GPO24.

BIT	FUNCTION
28	**nXOE and nXDIR / GPO[22-23] Signal Pin Select:** 0: Select nXOE and nXDIR (default). 1: The pins are used as GPO23 and GPO22.
27	**nRI / GPI12 Signal Pin Select:** 0: Select nRI function (default) 1: The pin is used as GPI12.
26	**Reserved**
25	**LID / GPI10 Signal Pin Select:** 0: Select LID (default) 1: The pin is used as GPI10.
24	**nBATLOW / GPI9 Signal Pin Select:** 0: Select nBATLOW (default) 1: The pin is used as GPI9.
23	**nTHRM / GPI8 Signal Pin Select:** 0: Select nTHRM (default) 1: The pin is used as GPI8.
22	**nSUS_STAT2 / GPO21 Signal Pin Select:** 0: Select nSUS_STAT2 (default) 1: The pin is used as GPO21.
21	**nSUS_STAT1 / GPO20 Signal Pin Select:** 0: Select nSUS_STAT1 (default) 1: The pin is used as GPO20.
20	**ZZ / GPO19 Signal Pin Select:** 0: Select ZZ (default) 1: The pin is used as GPO19.
19	**nPCI_STP / GPO18 Signal Pin Select:** 0: Select nPCI_STP (default) 1: The pin is used as GPO18.
18	**nCPU_STP / GPO17 Signal Pin Select:** 0: Select nCPU_STP (default) 1: The pin is used as GPO17.
17	**nSUSB and nSUSC / GPO[15-16] Pin Select:** 0: Select nSUSB and nSUSC (default) 1: The pins are used as GPO15 and GPO16.
16	**SERIRQ / GPI7 Signal Pin Select:** 0: Select GPI7 (default) 1: The pin is used as SERIRQ.
15	**nSMBALERT / GPI11 Signal Pin Select:** 0: Select nSMBALERT (default) 1: The pin is used as GPI11.
14	**nIRQ8 / GPI6 Signal Pin Select:** 0: Select GPI6(default) 1: The pin is used as nIRQ8.
13	**Reserved.**

BIT	FUNCTION
12	**Secondary IDE Signal Interface Tri-State:** 0: Enable Secondary IDE signal pin interface (default). 1: Tri-state (disable) Secondary IDE signal pin interface. This bit functions independently of bit 4.
11	**Primary IDE Signal Interface Tri-State:** 0: Enable Primary IDE signal pin interface (default). 1: Tri-state (disable) Primary IDE signal pin interface. This bit functions independently of bit 4.
10	**PC/PCI REQC and GNTC / GPI4 and GPO11 Signal Pin Select:** 0: Select GPI4 and GPO11 (default). 1: The pins are used for PC/PCI REQC and GNTC.
9	**PC/PCI REQB and GNTB / GPI3 and GPO10 Signal Pin Select:** 0: Select GPI3 and GPO10 (default). 1: The pins are used for PC/PCI REQB and GNTB.
8	**PC/PCI REQA and GNTA / GPI2 and GPO9 Signal Pin Select:** 0: Select GPI2 and GPO9 (default). 1: The pins are used for PC/PCI REQA and GNTA.
7	**Reserved.**
6	**Plug and Play (PnP) Address Decode Enable.** 0: Disable PnP address positive decode (default). 1: Enable PnP address positive decode and forwarding to the ISA bus. The PnP addresses which are decoded are 279h and A79h. If positive decode is selected through bit 1, this bin must be set for these address to be forwarded to ISA.
5	**Alternate Access Mode Enable** 0: Disable Alternate Access Mode (default). 1: Enable Alternate Access Mode to allow access to shadow registers. Enabling this function allows special access to various internal registers.
4	**IDE Signal Configuration.** 0: Primary and Secondary interface enable (default). 1: Primary 0 and Primary 1 interface enable. This bit selects whether the IDE interface are split for Primary and Secondary channels allowing access to 4 IDE devices or are split into Primary Drive 0 and Primary Drive 1 channels allowing access to only the 2 primary IDE devices.
3	**CONFIG 2 Status (RO).** This bit provides indication of signal present on CONFIG2 pin. Its meaning is currently undefined. The use of this pin is RESERVED and should be tied low through a pull down resistor.

BIT	FUNCTION
2	**CONFIG1 Status (RO).** 0: Pentium processor. 1: Pentium Pro Processor. This bit provides indication of signal present on CONFIG1 pin. It is used to change the polarity of the INIT and CPURST signals to match the requirements of microprocessors.
1	**Positive or Subtractive Decode Configuration.** 0: Subtractive Decode (default). 1: Positive Decode. This bit determines how the SLC90E46 decodes accesses on the PCI bus for forwarding to ISA. If set for positive decode, the SLC90E46 will positively decode, with medium decode timing, and forward PCI access to ISA only for address ranges which are enabled within the SLC90E46. If set for subtractive decode, the SLC90E46 still positively decodes and forwards those cycles whose addresses are enabled within the SLC90E46. It will subtractively decode and forward all other cycles not positively decoded by other devices on the PCI bus. The functionality and setting of this bit is independent of bit 0.
0	**ISA or EIO Select:** 0: EIO (default). 1: ISA. This bit determines whether the expansion bus on the SLC90E46 supports the full ISA bus or whether it supports the EIO bus. This bit also selects the functionality multiplexed onto the nIOCHK and LA[17-23] pins: 0: GPI0 and GPO[1-7], 1: nIOCHK and LA[17-23] respectively.

4.2.20. RTCCFG Real Time Clock Configuration Register

Offset Address: CBh
Default Value: 21h
Access: Read/Write

This register is used to configure the internal Real Time Clock.

BIT	FUNCTION
7-6	**Reserved**.
5	**RTC Positive Decode Enable.** 0: SLC90E46 subtractively decodes for RTC I/O registers. 1: SLC90E46 positively decodes for RTC I/O registers (default). The PCI cycles with addresses 70-73h are either positively or subtractively decoded based on this bit. The cycles are then routed to the internal RTC controller or forwarded to ISA bus based on bits 2 and bit 0 below. This bit should be set to a 0 if the SLC90E46's internal RTC is not used and the external RTC is on the PCI bus, or if subtractive decode is desired for an external RTC on the ISA or XBus.
4	**Lock Upper RAM Bytes.** 0: Upper RAM data bytes 38-3Fh in the extended bank are read/writeable (default). 1: Upper RAM data bytes 38-3Fh in the extended bank are neither readable nor writeable This is used to lock bytes 38h-3Fh in the upper 128-byte bank of RAM. Write cycles will have no effect and read cycle will not return a guaranteed value. WARNING: This is a write once register that can only be reset by a hardware reset.
3	**Lock Lower RAM Bytes.** 0: Upper RAM data bytes 38-3Fh in the standard bank are read/writeable (default). 1: Upper RAM data bytes 38-3Fh in the standard bank are neither readable nor writeable This is used to lock bytes 38h-3Fh in the lower 128-byte bank of RAM. Write cycles will have no effect and read cycle will not return a guaranteed value. WARNING: This is a write once register that can only be reset by a hardware reset.
2	**Upper RAM Enable.** 0: Accesses to RTC Upper 128 byte extended bank at I/O address 72-73h is disabled. Accesses will be forwarded to ISA bus as determined by bit 5 of this register (default). 1: Accesses to 72-73h are forwarded to RTC Upper 128 byte extended bank.
1	Reserved.
0	**RTC Enable.** 0: Accesses to RTC lower 128 byte standard bank at I/O address 70-71h is disabled. Accesses will be forwarded to ISA bus as determined by bit 5 of this register. 1: Accesses to 70-71h are forwarded to RTC lower 128 byte standard bank. When this bit is reset, the upper bank of RAM may still be accessed by enabling bit 2 of this register.

4.2.21. SBMISCL South Bridge Miscellaneous Low Register

Offset Address: 0E0h
Default Value: 40h
Access: Read/Write

BIT	FUNCTION
7-6	AT bus clock. 00: PCICLK/4. 10: PCICLK/3. x1: PCICLK/2
5	AT cycle one extra wait state option. 0: Disable. 1: Enable.
4-3	Reserved
2	AT hidden refresh option. 0: Enable hidden refresh. 1: Disable AT hidden refresh. When this bit is set to 1, the CPU will be held while the AT bus is doing refresh.
1	AT refresh option. 0: Enable. 1: Disable (no refresh signal will be asserted).
0	AT DRAM slow refresh. 0: Disable. 1: Enable. Refresh interval is extended to 60 us.

4.2.22. SBMISCH South Bridge Miscellaneous High Register

Offset Address: 0E1h
Default Value: 40h
Access: Read/Write

BIT	FUNCTION
7	Delay nFRAME Assertion (one PCI clock) Enable. 0: Disable. 1: Enable.
6	Port 92 Enable Control. 0: Disable 1: Enable.
5	Special patch for cards which do not assert nIO16 for 16-bit cycles. 0: Disable. 1: Enable.
4	PCI System Parity Errors (nSERR) qualifer. 0: Always disqualify the nSERR signal. 1: Allows the nSERR signal to pass through the qualify circuit and generate NMI if bit 2 of IO register 61h is a '0'.
3-1	PCI IDE IRQ routing. 000: IRQ3. 001: IRQ5. 010: IRQ7. 011: IRQ8. 100: IRQ11. 101: IRQ12. 110: IRQ14. 111: IRQ15.
0	PCI IDE controller interrupt routing option. 0: route to the PCI INTA signal. 1: Decided by bits [3-1] of this register.

4.3. PCI to ISA/EIO Bridge IO Space Registers

The SLC90E46 contains compatible IO configuration registers of the two DMA controllers, two Interrupt controllers, and the timer. This section gives brief descriptions of these IO registers.

4.3.1. DMA Registers

The DMA registers control the operation of the DMA controllers and are all accessible from the host CPU via the PCI bus interface. In addition, some of the registers are accessible from the ISA bus via ISA I/O space. Unless otherwise stated, a CPURST sets each register to its default states.

4.3.1.1. DMA Command Register

I/O Address: Channels 0-3: 08h; Channels 4-7: 0D0h
Default Value: 00h (CPURST or Master Clear)
Access: Write Only

This register controls the configuration of the DMA controllers. Note that disabling channels 4-7 also disables channels 0-3, since channels 0-3 are cascaded onto channel 4.

BIT	FUNCTION
7	**nDACK Active Level.** 1: Active high; 0: Active low.
6	**DREQ Sense Assert Level.** 1: Active low; 0: Active high.
5	**Reserved.** Must be 0.
4	**DMA Group Arbitration Priority.** 1: Rotating priority; 0: Fixed Priority.
3	**Reserved.** Must be 0.
2	**DMA Channel Group Enable.** 1: Disable; 0: Enable.
1-0	**Reserved.** Must be 0.

4.3.1.2. DMA Channel Mode Register

I/O Address: Channels 0-3: 0Bh; Channels 4-7: 0D6h
Default Value: Bits[7-2]=0; Bits[1-0]=undefined (CPURST or Master Clear)
Access: Write Only

BIT	FUNCTION
7-6	**DMA Transfer Mode.** Each DMA channel can be programmed in one of four modes: 00: Demand mode; 01: Single mode; 10: Block mode; 11: Cascade mode.
5	**Address Increment/Decrement Select.** 1: Decrement; 0: Increment.
4	**Autoinitialize Enable** 1: Enable; 0: Disable.
3-2	**DMA Transfer Type.** When DMA transfer mode is Cascade mode, this field is irrelevant. 00: Verify transfer 01: Write transfer 10: Read transfer 11: Illegal

BIT	FUNCTION
1-0	**DMA Channel Select.** Selects the DMA Channel Mode Register written to by bits [7-2]. 00: Channel 0 (4) . 01: Channel 1 (5) 10: Channel 2 (6) 11: Channel 3 (7)

4.3.1.3. DMA Request Register

I/O Address: Channels 0-3: 09h; Channels 4-7: 0D2h
Default Value: Bits[7-2]=0; Bits[1-0]=undefined (CPURST or Master Clear)
Access: Write Only

This register is used by software to initiate a DMA request. The DMA responds to the software request as though DREQx is asserted. These request are non-maskable. For a software request, the channel must be in Block mode. The Request register status for DMA1 and DMA2 is shown on bits[7-4] of a Status Register read.

BIT	FUNCTION
7-3	**Reserved.** Must be 0.
2	**DMA Channel Service Request.** 1: Sets the request bit; 0: Resets the software DMA channel request bit. Generation of a TC also sets this bit to 0.
1-0	**DMA Channel Select.** Selects the DMA Channel. 00: Channel 0 (4) . 01: Channel 1 (5) 10: Channel 2 (6) 11: Channel 3 (7)

4.3.1.4. Write Single Mask Bit Register

I/O Address: Channels 0-3: 0Ah; Channels 4-7: 0D4h
Default Value: Bits[7-3]=0; Bit 2=1; Bits[1-0]=undefined (CPURST or Master Clear)
Access: Write Only

A channel's mask bit is automatically set when the Current Byte/Word count register reaches terminal count (unless the channel is programmed for autoinitialization). When a channel is masked, all DMA requests are disabled until a clear mask register instruction occurs. Masking channel 4 also masks channels 0 to 3.

BIT	FUNCTION
7-3	**Reserved.** Must be 0.
2	**DMA Channel Mask Select.** 1: Disable DREQ for the selected channel (bits [1-0]); 0: Enable DREQ for the channel.
1-0	**DMA Channel Select.** Selects the DMA Channel. 00: Channel 0 (4) . 01: Channel 1 (5) 10: Channel 2 (6) 11: Channel 3 (7)

4.3.1.5. Read/Write All Mask Bits Register

I/O Address: Channels 0-3: 0Fh; Channels 4-7: 0DEh
Default Value: Bits[7-4]=0; Bits[3-0]=1 (CPURST or Master Clear)
Access: Write Only

A channel's mask bit is automatically set when the Current Byte/Word count register reaches terminal count (unless the channel is programmed for autoinitialization). Setting bits [3-0] to 1 disables the corresponding DMA channel until a clear mask register instruction enables the channel.

BIT	FUNCTION
7-4	**Reserved.** Must be 0.
3	**DMA Channel 3 (7) Mask Bit.** 1: Disable the corresponding DREQ; 0: Enable the corresponding DREQ.
2	**DMA Channel 2 (6) Mask Bit.** 1: Disable the corresponding DREQ; 0: Enable the corresponding DREQ.
1	**DMA Channel 1 (5) Mask Bit.** 1: Disable the corresponding DREQ; 0: Enable the corresponding DREQ.
0	**DMA Channel 0 (4) Mask Bit.** 1: Disable the corresponding DREQ; 0: Enable the corresponding DREQ.

4.3.1.6. DMA Status Register

I/O Address: Channels 0-3: 08h; Channels 4-7: 0D0h
Default Value: 00h
Access: Read Only

Each DMA controller has a read-only DMA status register that indicates which channels have reached terminal count and which channels have a pending DMA request.

BIT	FUNCTION
7-4	**Channel Request Status.** When a valid DMA request is pending for a channel, the corresponding bit is set to 1. The source of the DREQ may be hardware or a software request. Since the channel 4 does not have DREQ or DACK lines, so the response for a read of DMA2 status for channel 4 is irrelevant. Bit7: Channel 3 (7). Bit 6: Channel 2 (6). Bit5: Channel 1 (5). Bit 4: Channel 0.
3-0	**DMA Terminal Count Status.** 1: TC is reached. 0: TC is not reached. Bit7: Channel 3 (7). Bit 6: Channel 2 (6). Bit5: Channel 1 (5). Bit 4: Channel 0.

4.3.1.7. DMA Base and Current Address Registers

I/O Address: DMA Channel 0: 00h; DMA Channel 1: 02h
DMA Channel 2: 04h; DMA Channel 3: 06h
DMA Channel 4: C0h; DMA Channel 5: C4h
DMA Channel 6: C8h; DMA Channel 7: CCh
Default Value: Undefined (CPURST or Master Clear)
Access: Read/Write

This register works in conjunction with the Low Page Register. After autoinitialization, this register retains the original programmed value. The address register is automatically incremented or decremented after each transfer. Software must issue the "Clear Byte Pointer Flip-Flop" command to reset the internal byte pointer and correctly align the write prior to programming the current address register. Autoinitialization occurs only after a TC. This register is read/written in successive 8 bit bytes.

BIT	FUNCTION
15-0	**Base and Current Address.** These bits represent address bits[15-0] used when forming the 24 bit addresses for DMA transfers.

4.3.1.8. DMA Base and Current Count Registers

I/O Address: DMA Channel 0: 01h; DMA Channel 1: 03h
DMA Channel 2: 05h; DMA Channel 3: 07h
DMA Channel 4: C2h; DMA Channel 5: C6h
DMA Channel 6: CAh; DMA Channel 7: CEh
Default Value: Undefined (CPURST or Master Clear)
Access: Read / Write

This register determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in this register. When the value is decremented from 0 to 0ffffh, a TC is generated. Autoinitialization can only occur when a TC occurs. If it is not autoinitialized, this register has a count of FFFFh after TC.

BIT	FUNCTION
15-0	**Base and Current Byte/Word Count.**

4.3.1.9. DMA Low Page Registers

I/O Address: DMA Channel 0: 87h; DMA Channel 1: 83h
DMA Channel 2: 81h; DMA Channel 3: 82h
DMA Channel 5: 8Bh
DMA Channel 6: 89h; DMA Channel 7: 8Ah
Default Value: Undefined (CPURST or Master Clear)
Access: Read/Write

This register works in conjunction with the Current Address Register to form a 24 bit address. After autoinitialization, this register retains the original programmed value. Autoinitialization occurs after a TC.

BIT	FUNCTION
7-0	**DMA Low Page [23-16].** These bits represent address bits [23-16] of the 24 bit DMA address.

4.3.1.10. DMA Clear Byte Pointer Register

I/O Address: DMA Channels 0-3: 0Ch; DMA Channels 4-7: D8h
Default Value: Undefined
Access: Write Only

Writing to this register executes the Clear Byte Pointer Command. The command initializes the byte-pointer to a known state so that subsequent accesses to register contents address upper and lower bytes in the correct sequence. The Clear Byte Command (or CPURST or the Master Clear Command) clears the internal latch used to address the upper or lower byte of the 16 bit Address and Word Count Registers.

BIT	FUNCTION
7-0	**Clear Byte Pointer.** No specific pattern is required.

4.3.1.11. DMA Master Clear Register

I/O Address: DMA Channels 0-3: 0Dh; DMA Channels 4-7: DAh
Default Value: Undefined
Access: Write Only

This command has the same effect as the hardware reset.

BIT	FUNCTION
7-0	**Master Clear.** No specific pattern is required.

4.3.1.12. DMA Clear Mask Register

I/O Address: DMA Channels 0-3: 0Eh; DMA Channels 4-7: DCh
Default Value: Undefined
Access: Write Only

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

BIT	FUNCTION
7-0	**Clear Mask Register.** No specific pattern is required.

4.3.2. Interrupt Controller Registers

4.3.2.1. ICW1 - Initialization Command Word 1 Register

I/O Address: Controller I: 020h; Controller II: 0A0h
Default Value: Undefined
Access: Write Only

A write to the register starts the interrupt controller initialization sequence. Addresses 020h and 0A0h are referred to as the base addresses of interrupt controller I and interrupt controller II, respectively. An I/O write to the controller I and controller II base address with bit 4 equal to 1 is interpreted as ICW1. For SLC90E46-based systems, three I/O writes to "base address +1" must follow the ICW1. The first write to "base address +1" performs ICW2, the second write performs ICW3, and the third one performs ICW4.

The ICW1 command starts the following initialization sequence:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
5. The SLC90E46 requires the ICW4 to be programmed.

BIT	FUNCTION
7-5	**ICW/OCW select.** These bits should be 000 when programming the SLC90E46.
4	**ICW/OCW Select.** This bit must be 1 to select ICW1. After the fixed initialization sequence to ICW1, ICW2, ICW3 and ICW4, the controller base address is used to write to OCW2 and OCW3. Bit 4 should be a 0 on writes to these registers.
3	**Edge/Level Bank Select.** This bit is disabled.
2	**ADI.** Ignored.
1	**Single or Cascade.** Must be a 0.
0	**ICW4 Write Required.** This bit must be set to a 1.

4.3.2.2. ICW2 - Initialization Command Word 2 Register

I/O Address: Controller I: 021h; Controller II: 0A1h
Default Value: Undefined
Access: Write Only

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address.

BIT	FUNCTION
7-3	**Interrupt Vector Base Address.** Bits[7-3] define the base address in the interrupt vector table for the interrupt routines.
2-0	**Interrupt Request Level.** Must be programmed to all 0's.

4.3.2.3. ICW3 - Initialization Command Word 3 Register (Controller I)

I/O Address: 021h
Default Value: Undefined
Access: Write Only

On Interrupt Controller I, the master controller, ICW3 indicates which IRQ line physically connects the INTR output of Controller II to Controller I.

BIT	FUNCTION
7-3	**Reserved.** Must be programmed to all 0's.
2	**Cascaded Mode Enable.** This bit must be programmed to 1 selecting cascade mode.
1-0	**Reserved.** Must be programmed to all 0's.

4.3.2.4. ICW3 - Initialization Command Word 3 Register (Controller II)

I/O Address: 0A1h
Default Value: Undefined
Access: Write Only

On Interrupt Controller II, the slave controller, ICW3 is the slave identification code broadcast by Controller I.

BIT	FUNCTION
7-3	**Reserved.** Must be programmed to all 0's.
2-0	**Slave Identification Code.** Must be programmed to 010b.

4.3.2.5. ICW4 - Initialization Command Word 4 Register

I/O Address: Controller I: 021h; Controller II: 0A1h
Default Value: 01h
Access: Write Only

Both controllers must have ICW4 programmed as part of the initialization sequence.

BIT	FUNCTION
7-5	**Reserved.** Must be programmed to all 0's.
4	**Special Fully Nested Mode.** This bit should normally set to 0. When it is a 1, the special fully nested mode is programmed.
3	**Buffered Mode.** Must be programmed to 0 selecting non-buffered mode.
2	**Master/Slave in Buffered Mode.** This bit is not used. Should always be programmed to 0.
1	**AEOI (Automatic End of Interrupt).** This bit should normally set to 0 for normal end of interrupt mode. If this bit is 1, the AEOI mode is programmed.
0	**Microprocessor Mode.** Must be programmed to 1 indicating an 808x-based system.

4.3.2.6. OCW1 - Operation Control Word 1 Register

I/O Address: Controller I: 021h; Controller II: 0A1h
Default Value: 00h
Access: Read/Write

OCW1 sets and clears the mask bits in the Mask Register. Each request line can be selectively masked or unmasked any time after initialization. The Interrupt Mask Register ("IMR") stores the interrupt line mask bits. Masking of a higher priority input does not affect the interrupt request lines of lower priority. Unlike status reads of the ISR and IRR, for reading the IMR, no OCW3 is needed. The IMR can be accessed when an I/O read is active and the I/O address is 021h or 0A1h. All writes to OCW1 must occur following the ICW1 to ICW4 initialization sequence, since they all share the same I/O port.

BIT	FUNCTION
7-0	**Interrupt Request Mask.** Writing a 1 to any bit of the register causes the corresponding IRQx line to be masked (no interrupt will be generated). Once a request line is masked, the corresponding bit of the Interrupt Request Register ("IRR") will not be set by asserted interrupt requests. Writing a 0 to any bit of the register causes the corresponding IRQx line to be unmasked. Masking IRQ2 also masks the interrupt requests from Controller II.

4.3.2.7. OCW2 - Operation Control Word 2 Register

I/O Address: Controller I: 020h; Controller II: 0A0h
Default Value: Bits[7-5]: 001b; Bits[4-0]: Undefined
Access: Write Only

OCW2 controls both the Rotate mode and the End of Interrupt mode. After a CPURST or ICW initialization, the controller enters the fully nested mode of operation. Both rotation mode and specific EOI mode are disabled.

BIT	FUNCTION
7-5	**Rotate and EOI Codes**. (Bit 7 - R, Bit 6 - SL, Bit 5- EOI) 000: Rotate in Auto EOI mode (Clear) 001: Non-Specific EOI command 010: No Operation 011: Specific EOI command 100: Rotate in Auto EOI mode (Set). 101: Rotate in Non-Specific EOI Command 110: *Set priority command 111: *Rotate on Specific EOI command. *Bits [2-0] are used.
4-3	**OCW2 Select.** Must be programmed to 00 selecting OCW2.
2-0	**Interrupt Level Select.** Determines the interrupt level acted upon when the bit 6 (SL) is active. When the bit 6 is inactive, this field have no defined function. In this case, this field can be programmed to 0. 000: IRQ0 (8) 001: IRQ1 (9) 010: IRQ2 (10) 011: IRQ3 (11) 100: IRQ4 (12) 101: IRQ5 (13) 110: IRQ6 (14) 111: IRQ7 (15)

4.3.2.8. OCW3 - Operation Control Word 3 Register

I/O Address: Controller I: 020h; Controller II: 0A0h
Default Value: Bits[6,0]: 0b; Bits[7, 4-2]: Undefined; Bits[5,1]: 1b
Access: Read/Write

BIT	FUNCTION
7	**Reserved.** Must be 0.
6	**Special Mask Mode (SMM).** If both SMM and ESMM are set to 1, the interrupt controller enters Special Mask Mode. If ESMM is 1 and SMM is 0, the interrupt controller is in normal mask mode. When ESMM is 0, then SMM has no effect.
5	**Enabled Special Mask Mode (ESMM).** Set this bit to 1 to enable the SMM bit.
4-3	**OCW3 Select.** Must be programmed to 01 to select OCW3
2	**Poll Mode Command.** When this bit is a 1, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle indicating highest priority request. To disable the Poll Mode Command, set the bit to a 0.
1-0	**Register Read Command.** Bits[1-0] provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1 equals to 1, bit 0 selects the register status returned following an OCW3 read. Following ICW initialization, the default OCW3 port address read will be read "IRR". To retain the current selection, always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. 00: No Action. 01: No Action. 10: Read Interrupt Request Register (IRR) 11: Read In-Service Register (ISR)

4.3.2.9. ELCR1 - Edge/Level Control Register

I/O Address: 4D0h
Default Value: 00h
Access: Read/Write

This register selects the interrupt triggering mode for interrupt channel 7 to 3.

BIT	FUNCTION
7	**IRQ7 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
6	**IRQ6 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
5	**IRQ5 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
4	**IRQ4 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
3	**IRQ3 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
2-0	**Reserved.** Must be 0 to select Edge mode for IRQ 2, IRQ1, and IRQ0.

4.3.2.10. ELCR2 - Edge/Level Control Register

I/O Address: 4D1h
Default Value: 00h
Access: Read/Write

This register selects the interrupt triggering mode for interrupt channel [15, 14, 12-9].

BIT	FUNCTION
7	**IRQ15 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
6	**IRQ14 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
5	**Reserved.** Must be 0. IRQ13 is always in Edge trigger mode.
4	**IRQ12 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
3	**IRQ11 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
2	**IRQ10 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
1	**IRQ9 Trigger Mode.** 0: Edge triggered mode. 1: Level (High) trigger mode.
0	**Reserved.** Must be 0. IRQ8 is always in Edge trigger mode.

4.3.3. Counter/Timer Registers

4.3.3.1. Timer Control Word Register

I/O Address: 043h
Default Value: Undefined
Access: Write Only

BIT	FUNCTION
7-6	**Counter Select.** 00: Counter 0 select 01: Counter 1 select 10: Counter 2 select 11: Read Back Command
5-4	**Read/Write Select.** 00: Counter Latch Command 01: R/W Least Significant Byte (LSB) 10: R/W Most Significant Byte (MSB) 11: R/W LSB then MSB
3-1	**Counter Mode Selection.** 000: Mode 0 - Out signal on end of count (=0) 001: Mode 1 - Hardware retriggerable one-shot x10: Mode 2 - Rate generator (divide by n counter) x11: Mode 3 - Square wave output 100: Mode 4 - Software triggered strobe 101: Mode 5 - Hardware triggered strobe
0	**Binary/BCD Countdown Select.** 0: Binary countdown. The largest possible binary count is 2^{16}. 1: Binary Coded Decimal (BCD) count is used. The largest BCD count allowed is 10^4.

Read Back Command

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter(s). The Read Back Command is first written to the Timer Control Word register which latches the current states of the above mentioned variables. The value of the Counter and its status may then be read by accessing to the counter address. Following is the bit definitions for the Timer Control Word Register during the Read Back Command.

BIT	FUNCTION
7-6	**Read Back Command.** =11. Following the Read Back Command, I/O reads from the selected counter's I/O addresses produce the current latch status, the latched count, or both if bits 4 and 5 are both 0.
5	**Latch Count of Selected Counters.** 0: Latches the current count value of the selected counters. 1: No counter latch on the selected counters.
4	**Latch Status of Selected Counters.** 0: Latches the status of the selected counters. 1: No status latch on the selected counters.
3	**Counter 2 Select.** 0: This command will not apply to counter 2. 1: Counter 2 status /counter value will be latched.
2	**Counter 1 Select.** 0: This command will not apply to counter 1. 1: Counter 1 status /counter value will be latched.
1	**Counter 0 Select.** 0: This command will not apply to counter 0. 1: Counter 0 status /counter value will be latched.
0	**Reserved.** Must be 0.

Counter Latch Command

The Counter Latch Command latches the current count value at the time the command is received. If a Counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Latch Command was issued. IF the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read successively. Read, write, or programming operations for other counters may be inserted between the reads. Following is the bit definitions for the Timer Control Word Register during the Counter Latch Command.

BIT	FUNCTION
7-6	**Counter Select.** 00: Counter 0 select 01: Counter 1 select 10: Counter 2 select 11: Reserved.
5-4	**Counter Latch Command.** When this field is 00, the Counter Latch Command is selected during a write to the Timer Control Word Register. Following I/O reads from the selected counter's I/O addresses return the current latched count.
3-0	**Reserved.** Must be 0.

4.3.3.2. Timer Status Register

I/O Address: Counter 0: 040h, Counter 1: 041h, Counter 2: 042h
Default Value: Bit[7]=0, Bits[6-0]=Undefined.
Access: Read Only

Each Counter's status byte can be read following a Read Back Command. If latch status is chosen as a read back option, the next read from the counter's Timer Status Register returns the status byte.

BIT	FUNCTION
7	**Counter OUT pin state.** 1: Pin is 1. 0: Pin is 0.
6	**Count Register Status.** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). 0: Count has been transferred from CR to CE, and is available for reading. 1: Count has not been transferred from CR to CE, and is not yet available for reading.
5-4	**Read/Write Selection Status.** This field reflects the read/write selection made through bits[5-4] of the Control Register. 00: Counter Latch Command 01: R/W Least Significant Byte (LSB) 10: R/W Most Significant Byte (MSB) 11: R/W LSB then MSB
3-1	**Mode Selection Status.** This field returns the counter mode programming. 000: Mode 0 001: Mode 1 x10: Mode 2 x11: Mode 100: Mode 4 101: Mode 5
0	**Countdown Type Status.** 0: Binary countdown. 1: Binary Coded Decimal (BCD) countdown.

4.3.3.3. Timer Count Register

I/O Address: Counter 0: 040h, Counter 1: 041h, Counter 2: 042h
Default Value: All bits undefined.
Access: Read/Write

Each of these I/O ports can be used for writing count values to the Count Registers. Reading the current count value from the counter by either an I/O read, after a counter-latch command, or after a Read Back Command.

BIT	FUNCTION
7-0	**Counter Port Bit[7-0] or [15-8].** Each counter I/O port can be used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined by the Timer Control Word Register. The counter I/O port is also used to read the current count from the Count Register and return counter programming status following a Read Back Command.

4.3.4. NMI Register

The NMI logic has two 8 bit registers. The CPU reads the NMISC Register to determine the NMI source (with bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable/disable bit to a 1. The NMI Enable and Real-Time Clock Register can mask the NMI signal and disable/enable all NMI sources.

To ensure that all NMI requests are serviced, the following software flow should be followed:

1. NMI is detected by the processor on the rising edge of the NMI input.
2. The processor will read the status stored in ports 061h to determine what sources caused the NMI. The processor may then set to 0 the register bits controlling the sources that it has determined to be active. Between the time the processor reads the NMI sources and sets them to a 0, an NMI may have been generated by another source. The level of NMI will then remain active. This new NMI source will not be recognized by the processor because there was no edge on NMI.
3. The processor must then disable all NMIs by setting bit 7 of port 070h to a 1 and then enable all NMIs by setting bit 7 of port 070h to a 0. This will causes the NMI output to transition low then high if there are any pending NMI sources. The CPU's NMI input logic will then recognize a new NMI.

4.3.4.1. NMISC NMI Status and Control Register

Address: 061h
Default Value: 00h
Access: Read/Write

This register reports the status of different system components, controls the output of the speaker counter (Counter 2), and gates the counter output that drives the SPKR signal.

BIT	FUNCTION
7	**nSERR NMI Source Status - Read Only.** 1: A system board agent (PCI devices or main memory) detects a system board error and pulses the PCI nSERR line. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 0 and then set it to 1. When writing to port 61h, bit 7 must be 0.
6	**nIOCHK NMI Source Status - Read Only.** 1: An expansion board asserts nIOCHK on the ISA bus. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 0 and then set it to 1. When writing to port 061h, bit 6 must be 0.
5	**Timer Counter 2 OUT Status - Read Only.** The Counter 2 OUT signal state is reflected in bit 5. The value on this bit following a read is the current state of the Counter 2 OUT signal. Counter 2 must be programmed following a CPURST for this bit to have a determinate value. When writing to port 061h, bit 5 must be a 0.
4	**Refresh Cycle Toggle - Read Only.** The Refresh Cycle Toggle signal toggles from either 0 to 1 or 1 to 0 following every refresh cycle. When writing to port 061h, bit 4 must be a 0.
3	**nIOCHK NMI Enable.** 1: Clear and disable. 0: Enable nIOCHK NMIs.
2	**PCI nSERR Enable.** 1: Clear and disable. 0: Enable. In addition, bit 7 of SBMISCH must be set to a '1' to enable the nSERR feature.
1	**Speaker Data Enable.** 1: The SPKR output is the Counter 2 OUT signal value. 0: SPKR output is 0.
0	**Timer Counter 2 Enable.** 1: Enable. 0: Disable.

4.3.4.2. NMIEN NMI Enable Register

Address: 070h
Default Value: Bit[6:0]-undefined; Bit7=1
Access: Write Only

This port is shared with the real-time clock. The contents of this register should not be modified without considering the effects on the state of the other bits. Reads and writes to this register address flow through to the ISA bus. Reads to register 70h will cause X-bus reads, but no nRTCCS or RTCALE will be generated.

BIT	FUNCTION
7	**NMI Enable.** 1: Disable generation of NMI. 0: Enable generation of NMI.
6-0	**Real Time Clock Address.** Used by the Real Time Clock to address memory locations. Not used for NMI enabling/disabling.

4.3.5. Real Time Clock Register

4.3.5.1. RTCI Real-Time Clock Index Register

Address: 070h
Default Value: Bit[6:0]-undefined; Bit 7=1
Access: Write Only

This register is shared with the NMI enable register. Reads and writes to this register address flow through to the ISA bus. Reads to register 70h will cause X-bus reads, but no nRTCCS or RTCALE will be generated.

BIT	FUNCTION
7	**NMI Enable.**
6-0	**Real Time Clock Address.** Latched by the Real Time Clock to address memory locations within the standard RAM bank accessed via the Real Time Clock Data Register (071h).

4.3.5.2. RTCD Real-Time Clock Data Register

Address: 071h
Default Value: Undefined
Access: Read/Write

The data port for accesses to the RTC standard RAM bank.

BIT	FUNCTION
7-0	**Standard RAM Data Port.** Data written to standard RAM bank address selected via RTC Index Register (070h).

4.3.5.3. RTCEI Real-Time Clock Extended Index Register

Address: 072h
Default Value: Unknown
Access: Write Only

The index port for accesses to the RTC extended RAM bank.

BIT	FUNCTION
7	**Reserved.**
6-0	**Real Time Clock Extended Address.** Latched by the Real Time Clock to address memory locations within the extended RAM bank accessed via the Real Time Clock Data Register (073h).

4.3.5.4. RTCED Real-Time Clock Extended Data Register

Address: 073h
Default Value: Unknown
Access: Read/Write

The data port for accesses to the RTC extended RAM bank.

BIT	FUNCTION
7-0	**Extended RAM Data Port.** Data written to extended RAM bank address selected via RTC Extended Index Register (072h).

4.3.6. Advanced Power Management (APM) Registers

4.3.6.1. APMC Advanced Power Management Control Port

Address: 0B2h
Default Value: 00h
Access: Read/Write

This register passes data (APM Commands) between the OS and the SMI handler. In addition, writes can generate an SMI. The SLC90E46 operation is not effected by the data in this register.

BIT	FUNCTION
7-0	**APM Control Port (APMC).** Writes to this register store data in the APMC Register and reads return the last data written. In addition, writes generate an SMI, if the APMC_EN bit (PCI function 3, offset 58h, bit 25) is set to 1. Reads do not generate an SMI.

4.3.6.2. APMS Advanced Power Management Status Port

Address: 0B3h
Default Value: 00h
Access: Read/Write

This register passes status information between the OS and the SMI handler. The SLC90E46 operation is not effected by the data in this register.

BIT	FUNCTION
7-0	**APM Status Port (APMS).** Writes to this register store data in the APMS Register and reads return the last data written.

4.3.7. X-Bus, Coprocessor, and Reset Registers

4.3.7.1. RIRQ Reset X-Bus IRQ12/M and IRQ1 Register

Address: 060h
Default Value: N/A
Access: Read Only

This register clears the mouse interrupt function (IRQ12/M) and the keyboard interrupt (IRQ1). Reads and writes to this address are accepted by the SLC90E46 and sent to ISA (Keyboard access must be enabled if in Positive decode). The SLC90E46 latches low to high transitions on IRQ1 and IRQ12/M (when enabled as mouse interrupt). A read of 60h clears the internally latched signal of IRQ1 and IRQ12/M.

BIT	FUNCTION
7-0	**Reset IRQ12 and IRQ1.** No specific pattern. A read of address 060h clears the internally latched IRQ1 and IRQ12/M signals.

4.3.7.2. P92 Port 92 Register

Address: 92h
Default Value: 00h
Access: Read/Write.

BIT	FUNCTION
7:2	**Reserved.** Returns 0 when read.
1	**FAST_A20.** 1: Causes nA20M signal to be asserted. 0: nA20M signal determined by A20GATE signal. This signal is internally combined (Ored) with the A20GATE input signal. The result is then output via the nA20M signal to the processor for support of real mode compatible software.
0	**FAST_INIT.** This read/write bit provides a fast software executed processor reset function. This function provides an alternate means to reset the system processor to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to this bit will cause the INIT signal to pulse active (high) for approximately 16 PCI clocks. Before another INIT pulse can be generated via this register, this bit must be written back to a 0.

4.3.7.3. CERR Coprocessor Error Register

Address: F0h
Default Value: N/A
Access: Write only.

Write to this register causes the SLC90E46 to assert nIGNNE. The SLC90E46 also negates IRQ13 (internal to the SLC90E46). Note that nIGNNE is not asserted unless nFERR is active. Read/Write flow through to the ISA bus.

BIT	FUNCTION
7:0	**Assert nIGNNE.** No special pattern required. A write to address F0h causes assertion of nIGNNE if nFERR is asserted.

4.3.7.4. RC Reset Control Register

Address: 0CF9h
Default Value: N/A
Access: Read/Write.

Bits 1 and 2 are used by the SLC90E46 to generate a hard reset or a soft reset. During a hard reset, the SLC90E46 asserts CPURST, nPCIRST, and RSTDRV, as well as reset its core and suspend well logic. During a soft reset, the SLC90E46 asserts INIT.

BIT	FUNCTION
7-3	**Reserved.**
2	**Reset CPU (RCPU).** This bit is used to initiate (transitions from 0 to 1) a hard reset (bit 1 in this register is set to 1) or a soft reset (bit 1 in this register is set to 0) to the CPU. The SLC90E46 also initiate a hard reset when PWROK is asserted. This bit cannot be read as a 1.
1	**System Reset (SRST).** This bit is used to select the type of reset generated when bit 2 is set to 1. 1: The SLC90E46 will generate a hard reset to the CPU when bit 2 transitions from 0 to 1. 0: The SLC90E46 will generate a soft reset when bit 2 transitions from 0 to 1.
0	**Reserved.**

5. SLC90E46 - IDE CONTROLLER REGISTER DESCRIPTION

Upon reset, the SLC90E46 sets its internal registers to predetermined default states, which represents the minimum functionality feature set required to bring up the system. It is the responsibility of the BIOS to properly program the configuration registers to achieve optimal system performance.

5.1. IDE Controller Register Mapping Table (Function 1)

5.1.1. PCI Configuration Registers (Function 1)

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
00-01h	VID	Vendor Identification	RO
02-03	DID	Device Identification	RO
04-05	PCICMD	PCI Command Register	R/W
06-07	PCISTS	PCI Status Register	R/W
08	RID	Revision ID	RO
09-0B	CLASSCODE	Class Code	RO
0D	MLT	Master Latency Timer	R/W
0E	HEDT	Header Type	RO
0F		Reserved	
10-13	IDEBASE1	PCI Base Address Register I	R/W
14-17	IDEBASE2	PCI Base Address Register II	R/W
18-1B	IDEBASE3	PCI Base Address Register III	R/W
1C-1F	IDEBASEIV	PCI Base Address Register IV	R/W
20-23	BMIBA	Bus Master Interface Base Address Register	R/W
24-3B		Reserved	
3C	INTLINE	PCI IDE Interrupt Line	R/W
3D	INTPIN	PCI IDE Interrupt Pin	R/W
3E-3F		Reserved	
40-41	IDETIM	Primary IDE Channel Timing Register	R/W
42-43	IDETIM	Secondary IDE Channel Timing Register	R/W
44	SIDETIM	Slave IDE Timing Register	R/W
45-47		Reserved	
48	SDMACTL	Ultra DMA/33 Control Register	R/W
4A-4B	SDMATIM	Ultra DMA/33 Timing Register	R/W
4C-FF		Reserved	

5.1.2. IO Space Registers (Function 1)

ADDRESS	ACCESS TYPE	ACCESSES	REGISTER NAME
Base +0000h	R/W	PCI	Primary Channel IDE Command Register
Base +0002h	R/WC	PCI	Primary channel IDE Status Register
Base +0004h	R/W	PCI	Primary Channel IDE Descriptor Pointer Table.
Base +0008h	R/W	PCI	Secondary Channel IDE Command Register
Base +000Ah	R/WC	PCI	Secondary Channel IDE Status Register.
Base +000Ch	R/W	PCI	Secondary Channel IDE Descriptor Pointer Table

5.2. IDE Controller PCI Register Description (Function 1)

This section describes in detail the registers associated with the SLC90E46 IDE Controller function.

5.2.1. VID Vendor Identification Register

Offset Address: 00 - 01h
Default Value: 10B8h
Access: Read

5.2.2. DID Device Identification Register

Offset Address: 02 - 03h
Default Value: 9461h
Access: Read

5.2.3. PCICMD PCI Command Register

Offset Address: 04 - 05h
Default Value: 00h
Access: Read

BIT	FUNCTION
1510	Reserved.
9	Fast Back-to-Back: not implemented, hardwired to 0..
8-5	Reserved. Read as 0
4	**Memory Write and Invalidate Enable**. This bit is hardwires to 0.
3	**Special Cycle Enable:** This bit is hardwired to 0.
2	**Bus Master Enable:** 1=Enable. 0=Disable.
1	**Memory Access Enable**: This bit is hardwired to 0.
0	**IO Access Enable**: This bit controls access to the I/O space registers. When it is 1, access to legacy IDE ports (both primary and secondary) and the PCI Bus Master IDE I/O registers is enable. The Base Address Register for the PCI Bus Master IDE I/O registers should be programmed before this bit is set to 1.

5.2.4. PCISTS PCI Device Status Register

Offset Address: 06 - 07h
Default Value: 0280h
Access: Read/Write

BIT	FUNCTION
15	**Detected Parity Error**. Not implemented, hardwired to 0.
14	**Signaled nSERR Status.** Read as 0.
13	**Master Abort Status.** When the Bus Master IDE interface function, as a master, generates a master abort, this bit is set to 1. **To reset this bit, write a 1 to it.**
12	**Received Target Abort Status**. When the Bus Master IDE interface function is a master on the PCI bus and receives a target abort, this bit is set to 1. **To reset the bit, write a 1 to it.**
11	**Signaled Target Abort.** This bit is set when the SLC90E46 IDE controller function is targeted with a transaction that the SLC90E46 terminates with a target abort. To reset this bit, write a 1 to the bit.
10-9	**nDEVSEL Timing**. Always 01 to select "medium" timing for nDEVSEL assertion, which is two PCI clocks after the assertion of nFRAME, when performing a positive decode. nDEVSEL timing does not include configuration cycles.
8	**Data Parity Detected.** Always 0, not implemented.
7	**Fast Back-to-Back Capable**: **RO**. Hardwired to 1. This bit indicates to the PCI master that the SLC90E46 as a target is capable of accepting fast back-to-back transaction.
6-0	Reserved.

5.2.5. RID Revision Identification Register

Offset Address: 08h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
7-0	Hardwired to the revision number, which is set to 00 as the initial number.

5.2.6. CLASSC Class Code Register

Offset Address: 09 - 0Bh
Default Value: 01018Ah
Access: Read

BIT	FUNCTION
23-16	**Base Class Code**. 01h: Mass storage device.
15-8	**Sub-Class Code**. 01h: IDE controller.
7	1: Master mode IDE controller.
6-4	Reserved (always 0).
3	1: Secondary IDE channel can be either native or legacy more.
2	Secondary IDE channel operating mode. 1: native PCI mode. 0: legacy mode.
1	1: Primary IDE channel can be either native or legacy more.
0	Primary IDE channel operating mode. 1: native PCI mode. 0: legacy mode.

5.2.7. MLT Master Latency Timer Register

Offset Address: 0Dh
Default Value: 00h
Access: Read / Write

MLT controls the amount of time SLC90E46, as a bus master, can burst data on the PCI bus. The count value is an 8 bit quantity. However, MLT[3:0] are reserved and 0 when determining the count value. The Master Latency Timer is cleared and suspended when the SLC90E46 is not asserting nFRAME. When SLC90E46 asserts nFRAME, the counter begins counting, If the SLC90E46 finishes its transaction before the count expires, the MLT count is ignored. If the count expires before the transaction completes (Count equals number of clocks programmed in MLT), SLC90E46 initiates a transaction termination as soon as the its nPHLDA is removed. The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allocated to SLC90E46. The default value of MLT is 0 PCI clocks.

BIT	FUNCTION
7-4	**Master Latency Timer Count Value.** SLC90E46-initiated PCI burst cycles can last indefinitely, as long as nPHLDA remains active. However, if nPHLDA is negated after the burst cycle is initiated, SLC90E46 limits the burst cycle to the number of PCI Bus clocks specified by this field.
3-0	Reserved.

5.2.8. HEDT Header Type Register

Offset Address: 0Eh
Default Value: 00h
Access: Read

BIT	FUNCTION
7-0	(Device Type) 00h: The IDE Controller is a single function device.

5.2.9. IDEBASE1 PCI Base Address Register I

Address offset: 10-13h
Value: **01F1h**
Attribute: Read/Write.

5.2.10. IDEBASE2 PCI Base Address Register II

Address offset: 14-17h
Value: **03F5h**
Attribute: Read/Write.

5.2.11. IDEBASE3 PCI Base Address Register III

Address offset: 18-1Bh
Value: **0171h**
Attribute: Read/Write.

5.2.12. IDEBASE4 PCI Base Address Register IV

Address offset: 1C-1Fh
Value: **0375h**
Attribute: Read/Write

5.2.13. BMIBA Bus Master Interface Base Address Register

Offset Address: 20-23h
Default Value: 00000001h
Access: Read/Write

This register selects the base address of a 16 byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary and 6 bytes for secondary).

BIT	FUNCTION
31-16	**Reserved.** Hardwired to 0.
15-4	**Bus Master Interface Base Address.** These bits provide the base address for the Bus Master interface registers and correspond to AD[15:4].
3-2	**Reserved.** Hardwired to 0.
1	**Reserved.**
0	**Resource Type Indicator - Read Only.** This bit is hardwired to 1 indicating that the base address field in this register maps to I/O space.

5.2.14. INTLINE PCI IDE Interrupt Line

Address offset: 3Ch
Value: 0Eh
Attribute: Read/Write

5.2.15. INTPIN PCI IDE Interrupt Pin

Address offset: 3Dh
Value: 01h
Attribute: Read/Write

5.2.16. IDETIM IDE Timing Register

Offset Address: 40-41h: Primary Channel. 42-43h: Secondary Channel.
Default Value: 0000h
Access: Read/Write

This register controls the SLC90E46's IDE interface and selects the timing characteristics of the PCI IDE cycle for PIO and standard Bus Master transfers. Note that primary and secondary denotations distinguish between the cables and the 0/1 denotations between master (0) and slave (1).

BIT	FUNCTION
15	**IDE Decode Enable**. 1: Enable. 0: Disable. When enabled, I/O transactions on PCI targeting the IDE ATA register blocks (command and control blocks) are positively decoded on PCI and drive on the IDE interface. When disabled, these accesses are subtractively decoded to ISA.
14	**Slave IDE Timing Register Enable**. 1:Enable SIDETIM register. 0: Disable (default). When enabled, this register defines the timing for the drive 0 device, and the SIDETIM registers can be programmed for the drive 1 devices. When disabled, this register defines the timing for both drive 0 and drive 1 devices on each channel.
13-12	**IORDY Sample Point.** This field selects the number of PCI clocks between nDIOx assertion and the first IORDY sample point. 00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks.
11-10	**Reserved**.
9-8	**Recovery Time.** This field selects the minimum number of PCI clocks between the last nIORDY sample point and the next nDIOx strobe. 00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1 clock.
7	**DMA Timing Enable Only for Drive 1.** When this bit is a 1, fast timing mode is enabled for DMA data transfers for Drive 1. PIO transfer to the IDE data port will run in compatible timing. When this bit is a 0, both DMA and PIO data transfers to drive 1 will use the fast timing mode.
6	**Prefetch and Posting Enable for Drive 1.** When this bit is a 1, prefetch and posting to the IDE data port is enabled for drive 1. When this bit is a 0, prefetch and posting is disabled for drive 1.
5	**IORDY Sample Point Enable for Drive 1.** When this bit is a 1 and the currently selected drive (via a copy of bit 4 of 1x6h) is drive 1, all accesses to the enabled IO address range sample IORDY. The IORDY sample point is specified by the "IORDY Sample Point" field of this register. When this bit is a 0, IORDY sampling is disabled for drive 1. The internal IORDY signal is forced asserted guaranteeing that IORDY is sampled asserted at the first sample point as specified by the "IORDY Sample Point" field in this register.
4	**Fast Timing Bank for Drive 1.** When this bit is a 1 and the currently selected drive is drive 1, accesses to the data port of the enabled IO address range uses fast timings. PIO accesses to the data port use fast timing only if bit 7 of this register is zero. Accesses to all non-data ports of the enabled I/O address range always use the 8 bit compatible timings. When this bit is a 0, accesses to the data port of the enabled I/O address range uses the 16-bit compatible timing.

BIT	FUNCTION
3	**DMA Timing Enable Only for Drive 0.** When this bit is a 1, fast timing mode is enabled for DMA data transfers for Drive 0. PIO transfer to the IDE data port will run in compatible timing. When this bit is a 0, both DMA and PIO data transfers to drive 0 will use the fast timing mode.
2	**Prefetch and Posting Enable for Drive 0.** When this bit is a 1, prefetch and posting to the IDE data port is enabled for drive 0. When this bit is a 0, prefetch and posting is disabled for drive 0.
1	**IORDY Sample Point Enable for Drive 0.** When this bit is a 1 and the currently selected drive (via a copy of bit 4 of 1x6h) is drive 0, all accesses to the enabled IO address range sample IORDY. The IORDY sample point is specified by the "IORDY Sample Point" field of this register. When this bit is a 0, IORDY sampling is disabled for drive 0. The internal IORDY signal is forced asserted guaranteeing that IORDY is sampled asserted at the first sample point as specified by the "IORDY Sample Point" field in this register.
0	**Fast Timing Bank for Drive 0.** When this bit is a 1 and the currently selected drive is drive 0, accesses to the data port of the enabled IO address range uses fast timings. PIO accesses to the data port use fast timing only if bit 3 of this register is zero. Accesses to all non-data ports of the enabled I/O address range always use the 8 bit compatible timings. When this bit is a 0, accesses to the data port of the enabled I/O address range uses the 16 bit compatible timing.

5.2.17. SIDETIM Slave IDE Timing Register

Offset Address: 44h
Default Value: 00h
Access: Read/Write

This register controls the SLC90E46's IDE interface and selects the timing characteristics for the slave drive on each IDE channel. This allows for programming of independent operating modes for each IDE agent. This register has no effect unless the bit 14 of the register IDETIM is enabled.

BIT	FUNCTION
7-6	**Secondary Drive 1 IORDY Sample Point**. This field selects the number of PCI clocks between nSDIOx assertion and the first nSIORDY sample point for the slave drive on the secondary channel. 00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks.
5-4	**Secondary Drive 1 Recovery Time.** This field selects the minimum number of PCI clocks between the last nSIORDY sample point and the next nSDIOx strobe for the slave drive on the secondary channel. 00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1clock
3-2	**Primary Drive 1 IORDY Sample Point**. This field selects the number of PCI clocks between nPDIOx assertion and the first nPIORDY sample point for the slave drive on the primary channel. 00: 5 clocks 01: 4 clocks 10: 3 clocks 11: 2 clocks.

BIT	FUNCTION
1-0	**Primary Drive 1 Recovery Time.** This field selects the minimum number of PCI clocks between the last nPIORDY sample point and the next nPDIOx strobe for the slave drive on the primary channel. 00: 4 clocks 01: 3 clocks 10: 2 clocks 11: 1clock

5.2.18. UDMACTL Ultra DMA/33 Control Register

Offset Address: 48h
Default Value: 00h
Access: Read/Write

This register enables each individual channel and drive for Ultra DMA/33 transfers. For non-Ultra DMA/33 operation, this registers should be left programmed to its default value.

BIT	FUNCTION
7-4	Reserved.
3	Secondary Drive 1 UDMA Enable.. 1: Enable UDMA mode for secondary channel drive 1. 0: Disable (default).
2	Secondary Drive 0 UDMA Enable.. 1: Enable UDMA mode for secondary channel drive 0. 0: Disable (default).
1	Primary Drive 1 UDMA Enable. 1: Enable UDMA mode for primary channel drive 1. 0: Disable (default).
0	Primary Drive 0 UDMA Enable. 1: Enable UDMA mode for primary channel drive 0. 0: Disable (default)..

5.2.19. UDMATIM Ultra DMA/33 Timing Register

Offset Address: 4A-4Bh
Default Value: 00h
Access: Read/Write

This register controls the timing used by each Ultra DMA/33 enabled device. For non-Ultra DMA/33 operation, this register should be left programmed to its default value. The table below shows bit setting requirements for Ultra DMA/33 Timing Modes.

BIT	FUNCTION
15-14	**Reserved.**
13-12	**Secondary Drive 1 Cycle Time.** These bit settings determine the minimum data write strobe Cycle Time (CT) and minimum Ready to Pause time (RP), measured in PCI clock. 00: CT=4 clocks, RP=6 clocks 01: CT=3 clocks, RP=5 clocks 10: CT=2 clocks, RP=4 clocks. 11: Reserved.
11-10	**Reserved.**
9-8	**Secondary Drive 0 Cycle Time.** These bit settings determine the minimum data write strobe Cycle Time (CT) and minimum Ready to Pause time (RP), measured in PCI clock. 00: CT=4 clocks, RP=6 clocks 01: CT=3 clocks, RP=5 clocks 10: CT=2 clocks, RP=4 clocks. 11: Reserved.
7-6	**Reserved.**
5-4	**Primary Drive 1 Cycle Time.** These bit settings determine the minimum data write strobe Cycle Time (CT) and minimum Ready to Pause time (RP), measured in PCI clock. 00: CT=4 clocks, RP=6 clocks 01: CT=3 clocks, RP=5 clocks 10: CT=2 clocks, RP=4 clocks. 11: Reserved.
3-2	**Reserved.**
1-0	**Primary Drive 0 Cycle Time.** These bit settings determine the minimum data write strobe Cycle Time (CT) and minimum Ready to Pause time (RP), measured in PCI clock. 00: CT=4 clocks, RP=6 clocks 01: CT=3 clocks, RP=5 clocks 10: CT=2 clocks, RP=4 clocks. 11: Reserved.

	ULTRA DMA/33 TIMING MODES		
Cycle Time Bit Settings	Mode 0 (120ns)	Mode 1 (90ns)	Mode 2 (60ns)
	00	01	10

5.3. IDE Controller IO Space Registers

The PCI IDE function uses 16 bytes of I/O space, allocated by the BMIBA register. All bus master IDE I/O space registers can be accessed as byte, word, or double-word quantities.

5.3.1. BMICx Bus Master IDE Command Register (IO)

Offset Address: Primary channel - Base +00h; Secondary channel - Base + 08h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-4	Reserved.
3	Bus Master Read/Write Control. Set the direction of the bus master data transfer. 0: PCI bus master reads are performed. 1: PCI bus master writes are performed. This bit must not be changed when the bus master function is active.
2:1	Reserved.
0	Start/Stop Bus Master. 1: Start. 0: Stop. Writing a '1' to this bit enable bus master operation of the controller. Bus master operation begins when this bit is detected changing from a zero to a one. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. Master mode operation cannot be stopped and then resumed. If this bit is set to 0 while bus master operation is still active (i.e., Bit 0 of the Bus Master IDE Status Register for that IDE channel is 1) and the drive has not yet finished its data transfer (bit 2 of the Bus Master IDE Status Register for that IDE channel is 0), the bus master command is aborted and data transferred from the drive may be discarded by the SLC90E46 rather than being written to system memory. This bit is intended to be set to a 0 after the data transfer is completed, as indicated by either bit 0 or bit 2 being set in the IDE Channel's Bus Master IDE Status Register.

5.3.2. BMISx Bus Master IDE Status Register

Address offset: Primary: Base address + 02h
Secondary: Base address + 0Ah
Value: 00h
Attribute: Read/Write Clear

BIT	FUNCTION
7	Simplex only indication bit. 0: Both primary and secondary channels can be used at the same time. 1: One channel may be used at a time.
6	Drive 1 DMA capable. 1: Drive 1 for this channel is capable of DMA transfers. This bit is a software controlled status bit that indicates IDE DMA device capability and does not affect hardware operation.
5	Drive 0 DMA capable. 1: Drive 0 for this channel is capable of DMA transfers.
4-3	Reserved
2	Interrupt: This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is read as a one, all data transferred from the drive is visible in the system memory and all write data has been transferred to the IDE device.
1	IDE DMA Error: This bit is set when the controller encounters an error in transferring data to/from memory. This bit is cleared when a '1' is written to it by software.
0	Bus Master IDE active-Read Only. This bit is set when the Start/Stop bit is written to the Command register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start/Stop bit is cleared in the command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in the system memory, unless the bus master command was aborted.

The Following Table Lists the Four Possible Interrupt/Activity Status Combinations

BIT 2	BIT 0	DESCRIPTION
0	1	**DMA transfer is in progress**. No interrupt has been generated by the IDE device.
1	0	**The IDE device generated an interrupt and the Physical Region Descriptors exhausted.** This is normal completion where the size of the physical memory regions is equal to the IDE device transfer size.
1	1	**The IDE device generated an interrupt.** The controller has not reached the end of the physical memory regions. This is a valid completion case when the size of the physical memory regions is larger than the IDE device transfer size.
0	0	**Error Condition.** If the IDE DMA Error bit is a 1, there is a problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the Error bit is a 0, the PRD specified a smaller buffer size than the programmed IDE transfer size.

5.3.3. BMIDTPx Bus Master IDE Descriptor Table Pointer Register

Address offset: Primary: Base address + 04h
Secondary: Base address + 0Ch
Value: 00h
Attribute: Read/Write

BIT	FUNCTION	DEFAULT
31-2	Base address of Descriptor table. Corresponds to A[31:2]	0
1-0	Reserved.	0

6. SLC90E46 USB REGISTER DESCRIPTION (Function 2)

6.1. PCI Configuration Registers

Table 1 - PCI Configuration Register Summary

PCI CONF. REG.	R/W	REGISTER NAME
00-01	R	Vendor ID
02-03	R	Device ID
04-05	R/W	Command
06-07	R/W	Status
08	R	Revision ID
09-0B	R	Class Code
0C-0D	--	Reserved
0E	R	Header Type
0F	--	Reserved
10-13	R/W	Base Address Register 0
14-3B	--	Reserved
3C	R/W	Interrupt Line
3D	R/W	Interrupt Pin
3E	R/W	Min. Grant
3F	R/W	Max. Latency
40-43	R/W	Test Mode Enable Register
44	R/W	Operational Mode Enable Register
45-FF	--	Reserved

The PCI Configuration Registers are 32 bit registers decoded from the PCI address bits 7 through 2 and C/nBE[3:0], when IDSEL is high, AD[10:8] select the appropriate function, and AD[1:0] are '00'. Bytes within a 32 bit address are selected with the valid byte enables. All registers can be accessed via 8, 16, or 32 bit cycles (i.e. each byte is individually selected by the byte enables.) Registers marked as reserved, and reserved bits within a register are not implemented and should return 0s when read. Writes have no effect for reserved registers. The following paragraphs describe the USB PCI configuration registers implemented in the SLC90E46.

6.1.1. Vendor ID Register

PCI Address: 01-00h
Default Value: 10B8h.
Access: Read
This is a 16 bit Vendor ID assigned to SMSC.

6.1.2. Device ID Register

PCI Address: 03-02h
Default Value: A0F8h.
Access: Read

This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID it identifies any PCI device.

6.1.3. Command Register

PCI Address: 05-04h
Default Value: 0000h.
Access: Read/Write

Table 2 - PCI Command Register

BIT	FUNCTION
15-10	Reserved Bits - These bits are always 0.
9	Back to Back enable. USB Host Controller only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8	nSERR (Response) Detection Enable bit - If set to 1, USB Host Controller asserts nSERR when it detects an address parity error. nSERR is not asserted if this bit is 0.
7	Wait Cycle Control - USB Host Controller does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6	nPERR (Response) Detection Enable bit - If set to 1, USB Host Controller asserts nPERR when it is the agent receiving data AND it detects a data parity error. nPERR is not asserted if this bit is 0.
5	VGA Palette Snooping bit - This bit is always 0.
4	Memory Write and Invalidate Command - If set to 1, USB Host Controller is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cacheline size is set to 32 bytes and the memory write is exactly one cacheline.
3	Special Cycle Enable - USB Host Controller does not run special cycles on PCI. This bit is always 0.
2	PCI Master Enable - If set to 1, USB Host Controller is enabled to run PCI Master cycles.
1	Memory Enable - If set to 1, USB Host Controller is enabled to respond as a target to memory cycles.
0	I/O Enable - If set to 1, USB Host Controller is enabled to respond as a target to I/O cycles.

6.1.4. Status Register

PCI Address: 07-06h
Default Value: 0280h.
Access: Read/Write

The PCI Specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

Table 3 - PCI Status Register

BIT	FUNCTION
15	Detected Parity Error. This bit is set to 1 whenever USB Host Controller detects a parity error, even if the Parity Error (Response) Detection Enable bit (command register, bit 6) is disabled. Cleared (reset to 0) by writing a 1 to it.
14	nSERR Status. This bit is set to 1 whenever the USB Host Controller detects a PCI address parity error. Cleared (reset to 0) by writing a 1 to it.
13	Received Master Abort Status. Set to 1 when USB Host Controller, acting as a PCI master, aborts a PCI bus memory cycle. Cleared (reset to 0) by writing a 1 to it.
12	Received Target Abort Status. This bit is set to 1 when a USB Host Controller generated PCI cycle (USB Host Controller is the PCI master) is aborted by a PCI target. Cleared (reset to 0) by writing a 1 to it.
11	Signaled Target Abort Status. This bit is set to 1 when USB Host Controller signals target abort. Cleared (reset to 0) by writing a 1 to it.
10-9	nDEVSEL timing - Read only bits indicating nDEVSEL timing when performing a positive decode. Since nDEVSEL is asserted to meet the medium timing, these bits are encoded as 01b.
8	Data Parity Reported. Set to 1 if the Parity Error Response bit (Command Register bit 6) is set, and USB Host Controller detects nPERR asserted while acting as PCI master (whether nPERR was driven by USB Host Controller or not).
7	Fast Back-to-Back Capable. USB Host Controller does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-0	Reserved Bits - These bits are always 0.

6.1.5. Revision ID Register

PCI Address: 08h
Default Value: 00h.
Access: Read

This register contains the device's revision information. This is a read only register.

Table 4 – Revision Register

BIT	FUNCTION	
7-6	ASIC Vendor:	00 - 01 - Reserved 10 - Reserved 11 - Reserved
5-0	Functional Revision Level	000000

6.1.6. Class Code Register

PCI Address: 0B-09h
Default Value: 0C0310h
Access: Read

This register identifies the generic function of USB Host Controller the specific register level programming interface. The Base Class is 0Ch (Serial Bus Controller). The Sub Class is 03h (Universal Serial Bus). The Programming Interface is 10h (OpenHCI).

6.1.7. Cache Line Size

PCI Address: 0Ch
Default Value: 00h
Access: Read/Write

This register identifies the system cacheline size in units of 32-bit words. USB Host Controller will only store the value of bit 3 in this register since the cacheline size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

6.1.8. Latency Timer

PCI Address: 0Dh
Default Value: 00h
Access: Read/Write

This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.

6.1.9. Header Type Register

PCI Address: 0Eh
Default Value: 00h
Access: Read

This register identifies the type of the pre-defined header in the configuration space. Since USB Host Controller is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

6.1.10. BIST

PCI Address: 0Fh
Default Value: 00h
Access: Read

This register identifies the control and status of Built In Self Test. USB Host Controller does not implement BIST, so this register is read only.

6.1.11. Base Address Register

PCI Address: 13h-10h
Default Value: 00h
Access: Read/Write

This register identifies the base address of a contiguous memory space in main memory. POST will write all 1's to this register, then read back the value to determine how big of a memory space is requested. After allocating the requested memory, POST will write the upper bytes with the base address.

BIT	FUNCTION
31-12	Base Address. POST writes the value of the memory base address to this register.
11-4	Always 0. Indicates a 4K byte address range is requested
3	Always 0. Indicates there is no support for pre-fetchable memory.
2-1	Always 0. Indicates that the base register is 32-bits wide and can be placed anywhere in 32-bit memory space.
0	Always 0. Indicates that the operational registers are mapped into memory space.

6.1.12. Interrupt Line Register

PCI Address: 3Ch
Default Value: 00h
Access: Read/Write

This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to USB Host Controller.

6.1.13. Interrupt Pin Register

PCI Address: 3Dh
Default Value: 01h
Access: Read

This register identifies which interrupt pin a device uses. Since USB Host Controller uses nINTA, this value is set to 01h.

6.1.14. Min_Gnt Register

PCI Address: 3Eh
Default Value: 00h
Access: Read

This register specifies the desired settings for how long of a burst USB Host Controller needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

6.1.15. Max_Lat Register

PCI Address: 3Fh
Default Value: 00h
Access: Read

This register specifies the desired settings for how often USB Host Controller needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

6.1.16. Test Mode Enable Register

PCI Address: 43-40h
Default Value: 0XXXXXXXh
Access: Read / Write

This register selects which test mode is enabled. Bits defined as write-only are read as 0's.

Table 5 - USB Controller Test Mode Enable Register

BIT	FUNCTION
31	**SieTest** When set the SIE test mode interface is enabled. **SieTest** and **LpTest** enabled simultaneously results in undefined behavior.
30	**DbTest** When set the Data Buffer test mode is enabled.
29	**CntrTest** When set the Counter test mode is enabled.
28	**Clock12Overdrive** When set the CLK48 input clock bypasses the divide by 4 circuit and directly sources the USB 12 MHz clocks (both the static and data rate). When enabled the phase lock, LS mode, and clock suspension functions are disabled. The purpose of the this mode is to remove the divide by four logic for trace vector reduction when not testing the SIE.
27	**SpeedTest** When set the Technology Speed test mode is enabled.
26	**TestIOEnable** When set the device's Test I/O outputs are enabled. The pins are normally tri-stated unless enabled for visibility of internal nodes.
25	**DataBufferNoWrite** When set writes into the data buffer from the SIE will be disabled.
24	**DataBufferCount** When set the counter test modes are enabled in the data buffer.

BIT	FUNCTION
23	**ListProcessorTest** When set the List Processor observability outputs are enabled.
22	**FrameManagementTest1** When set the Frame Management Flags are visible
21	**FrameManagementTest2** When set the Frame Management Flags are visible.
22-20	Reserved. read/write 0
19-16	**TransactionStatus[3:0]: Read Only Bits** SIE completion code status.
15	**TdDataToggle: Write Only Bit** SIE test mode transaction Data Toggle control field
14	**EdSpeed: Write Only Bit** SIE test mode endpoint Speed control field
13	**EdFormat: Write Only Bit** SIE test mode endpoint Format control field
12-11	**TdDirection[1:0]: Write Only Bits** SIE test mode transaction Direction control field.
10-0	**EpAddr[10:0]: Write Only Bits** SIE test mode transaction Endpoint Address control field.

6.1.17. ASIC Operational Mode Enable Register

PCI Address: 44h
Default Value: 00h
Access: Read/Write

This register selects which operational mode is enabled. Bits defined as write-only are read as 0's.

BIT	FUNCTION
0	**DataBuffer Region 16** When set the size of the region for the data buffer is 16 bytes. Otherwise, the size is 32 bytes.

6.2. SB OpenHCI Memory Mapped Registers

Table 6 - HC Operational Register Summary

OFFSET	REGISTER
00-03	*HCREVISION*
04-07	*HCCONTROL*
08-0B	*HCCOMMANDSTATUS*
0C-0F	*HCINTERRUPTSTATUS*
10-13	*HCINTERRUPTENABLE*
14-17	*HCINTERRUPTDISABLE*
18-1B	*HCHCCA*
1C-1F	*HCPERIODCURRENTED*
20-23	*HCCONTROLHEADED*
24-27	*HCCONTROLCURRENTED*
28-2B	*HCBULKHEADED*
2C-2F	*HCBULKCURRENTED*
30-33	*HCDONEHEAD*
34-37	*HCFMINTERVAL*
38-3B	*HCFRAMEREMAINING*
3C-3F	*HCFMNUMBER*
40-43	*HCPERIODICSTART*
44-47	*HCLSTHRESHOLD*
48-4B	*HCRHDESCRIPTORA*
4C-4F	*HCRHDESCRIPTORB*
50-53	*HCRHSTATUS*
54-57	*HcRhPortStatus[1]*
58-5C	*HcRhPortStatus[2]*
100	*HceControl*
104	*HceInput*
108	*HceOutput*
10C	*HceStatus*

6.2.1. HCREVISIONfc

Table 7 - HCREVISION Register

REGISTER: *HCREVISION*			ADDRESS OFFSET: 00-03
Bits	**Reset**	**R/W**	**Description**
7-0	10h	R	**Revision** Indicates the OpenHCI Specification revision number implemented by the Hardware. (X.Y = XYh) supports the 1.0 specification.
31-8	0h	-	Rsvd. Read/Write 0's

6.2.2. HCCONTROL

Table 8 - HCCONTROL Register

REGISTER: *HCCONTROL*			ADDRESS OFFSET: 04-07
BITS	**RESET**	**R/W**	**DESCRIPTION**
1-0	00b	R/W	**ControlBulkServiceRatio** Specifies the number of Control Endpoints serviced for every Bulk Endpoint. Encoding is N-1 where N is the number of Control Endpoints (i.e. '00' = 1 Control Endpoint; '11' = 3 Control Endpoints)
2	0b	R/W	**PeriodicListEnable** When set, this bit enables processing of the Periodic (interrupt and isochronous) list. The Host Controller checks this bit prior to attempting any periodic transfers in a frame.
3	0b	R/W	**IsochronousEnable** When clear, this bit disables the Isochronous List when the Periodic List is enabled (so Interrupt EDs may be serviced). While processing the Periodic List, the Host Controller will check this bit when it finds an isochronous ED.
4	0b	R/W	**ControlListEnable** When set this bit enables processing of the Control list.
5	0b	R/W	**BulkListEnable** When set this bit enables processing of the Bulk list.
7-6	00b	R/W	**HostControllerFunctionalState** This field is used to set the Host Controller state. The state encodings are: 00: USBRESET 01: USBRESUME 10: USBOPERATIONAL 11: USBSUSPEND The Host Controller may force a state change from USBSUSPEND to USBRESUME after detecting resume signaling from a downstream port.
8	0b	R/W	**InterruptRouting** This bit is used for interrupt routing: 0: Interrupts routed to normal interrupt mechanism (INT). 1: Interrupts routed to SMI.
9	0b	R	**RemoteWakeupConnected** This bit indicated whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hard-coded to '0.'
10	0b	R/W	**RemoteWakeupConnectedEnable** If a remote wakeup signal is supported, this bit is used to enable that operation. Since there is no remote wakeup signal supported, this bit is ignored.
31-11	0h	-	Rsvd. Read/Write 0's

6.2.3. HCCOMMANDSTATUS

Table 9 - HCCOMMANDSTATUS Register

REGISTER: *HCCOMMANDSTATUS*			ADDRESS OFFSET: 08-0B
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**HostControllerReset** This bit is set to initiate a software reset. This bit is cleared by the Host Controller upon completion of the reset operation.
1	0b	R/W	**ControlListFilled** When set, this bit indicates there is an active ED on the Control List. The bit may be set by either software or the Host Controller. The bit is cleared by the Host Controller each time it begins processing the head of the Control List.
2	0b	R/W	**BulkListFilled** When set, this bit indicates there is an active ED on the Bulk List. The bit may be set by either software or the Host Controller. The bit is cleared by the Host Controller each time it begins processing the head of the Bulk List.
3	0b	R/W	**OwnershipChangeRequest** When set by software, this bit sets the **OwnershipChange** field in *HcInterruptStatus*. The bit is cleared by software.
15-4	0h	-	Rsvd. Read/Write 0's
17-16	00b		**ScheduleOverrunCount** This field increments every time the **SchedulingOverrun** bit in *HcInterruptStatus* is set. The count wraps from '11' to '00.'
31-18	0h	-	Reserved. Read/Write 0's

6.2.4. HCINTERRUPTSTATUS

All bits are set by hardware and cleared by software.

Table 10 - HCINTERRUPTSTATUS Register

REGISTER: *HCINTERRUPTSTATUS*			ADDRESS OFFSET: 0C-0F
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrun** This bit is set when the List Processor determines a Schedule Overrun has occurred.
1	0b	R/W	**WritebackDoneHead** This bit is set after the Host Controller has written *HcDoneHead* to *HccaDoneHead*.
2	0b	R/W	**StartOfFrame** This bit is set when the Frame Management block signals a 'Start of Frame' event.
3	0b	R/W	**ResumeDetected** This bit is set when the Host Controller detects resume signaling on a downstream port.
4	0b	R	**UnrecoverableError** This event is not implemented and is hard-coded to '0.' All writes are ignored.
5	0b	R/W	**FrameNumberOverflow** This bit is set when bit 15 of **FrameNumber** changes value from '0' to '1' or from '1' to '0.'
6	0b	R/W	**RootHubStatusChange** This bit is set when the content of *HcRhStatus* or the content of any *HcRhPortStatus* register has changed.
29-7	0h	-	Rsvd. Read/Write 0's
30	0b	R/W	**OwnershipChange** This bit is set when the **OwnershipChangeRequest** bit of *HcCommandStatus* is set.
31	0h	-	Reserved. Read/Write 0's

6.2.5. HCINTERRUPTENABLE

Writing a '1' to a bit in this register sets the corresponding bit, while writing a '0' to a bit leaves the bit unchanged.

Table 12 - HCINTERRUPTENABLE Register

REGISTER: *HCINTERRUPTENABLE*			ADDRESS OFFSET: 10-13
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrunEnable** 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun.
1	0b	R/W	**WritebackDoneHeadEnable** 0: Ignore 1: Enable interrupt generation due to Writeback Done Head.
2	0b	R/W	**StartOfFrameEnable** 0: Ignore 1: Enable interrupt generation due to Start of Frame.
3	0b	R/W	**ResumeDetectedEnable** 0: Ignore 1: Enable interrupt generation due to Resume Detected.
4	0b	R/W	**UnrecoverableErrorEnable** This event is not implemented. All writes to this bit will be ignored.
5	0b	R/W	**FrameNumberOverflowEnable** 0: Ignore 1: Enable interrupt generation due to Frame Number Overflow.
6	0b	R/W	**RootHubStatusChangeEnable** 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change.
29-7	0h	-	Rsvd. Read/Write 0's
30	0b	R/W	**OwnershipChangeEnable** 0: Ignore 1: Enable interrupt generation due to Ownership Change.
31	0b	R/W	**MasterInterruptEnable** This bit is a global interrupt enable. A write of '1' allows interrupts to be enabled via the specific enable bits listed above.

6.2.6. HCINTERRUPTDISABLE

Writing a '1' to a bit in this register clears the corresponding bit, while writing a '0' to a bit leaves the bit unchanged.

Table 13 - HCINTERRUPTDISABLE Register

REGISTER: *HCINTERRUPTDISABLE*			ADDRESS OFFSET: 14-17
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrunEnable** 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun.
1	0b	R/W	**WritebackDoneHeadEnable** 0: Ignore 1: Disable interrupt generation due to Writeback Done Head.
2	0b	R/W	**StartOfFrameEnable** 0: Ignore 1: Disable interrupt generation due to Start of Frame.
3	0b	R/W	**ResumeDetectedEnable** 0: Ignore 1: Disable interrupt generation due to Resume Detected.
4	0b	R/W	**UnrecoverableErrorEnable** This event is not implemented. All writes to this bit will be ignored.
5	0b	R/W	**FrameNumberOverflowEnable** 0: Ignore 1: Disable interrupt generation due to Frame Number Overflow.
6	0b	R/W	**RootHubStatusChangeEnable** 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change.
29-7	0h	-	Rsvd. Read/Write 0's
30	0b	R/W	**OwnershipChangeEnable** 0: Ignore 1: Disable interrupt generation due to Ownership Change.
31	0b	R/W	**MasterInterruptEnable** This bit is a global interrupt disable. A write of '1' disables all interrupts.

6.2.7. HCHCCA

Table 14 - HCHCCA Register

REGISTER: *HCHCCA*			ADDRESS OFFSET: 18-1B
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	0h	-	Rsvd. Read/Write 0's
31-8	0h	R/W	**HCCA** Pointer to HCCA base address.

6.2.8. HCPERIODCURRENTED

Table 15 - HCPERIODCURRENTED Register

REGISTER: *HCPERIODCURRENTED*			ADDRESS OFFSET: 1C-1F
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**PeriodCurrentED** Pointer to the current Periodic List ED.

6.2.9. HCCONTROLHEADED

Table 16 - HCCONTROLHEADED Register

REGISTER: *HCCONTROLHEADED*			ADDRESS OFFSET: 20-23
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**ControlHeadED** Pointer to the Control List Head ED.

6.2.10. *HCCONTROLCURRENTED*

Table 17 - HCCONTROLCURRENTED Register

REGISTER: *HCCONTROLCURRENTED*			ADDRESS OFFSET: 24-27
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**ControlCurrentED** Pointer to the current Control List ED.

6.2.11. HCBULKHEADED

Table 18 - HCBULKHEADED Register

REGISTER: *HCBULKHEADED*			ADDRESS OFFSET: 28-2B
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**BulkHeadED** Pointer to the Bulk List Head ED.

6.2.12. HCBULKCURRENTED

Table 19 - HCBULKCURRENTED Register

REGISTER: *HCBULKCURRENTED*			ADDRESS OFFSET: 2C-2F
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**BulkCurrentED** Pointer to the current Bulk List ED.

6.2.13. HCDONEHEAD

Table 20 - HCDONEHEAD Register

REGISTER: *HCDONEHEAD*			ADDRESS OFFSET: 30-33
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Rsvd. Read/Write 0's
31-4	0h	R/W	**DoneHead** Pointer to the current Done List Head ED.

6.2.14. HCFMINTERVAL

Table 21 - *HCFMINTERVAL* Register

REGISTER: *HCFMINTERVAL*			ADDRESS OFFSET: 34-37
BITS	**RESET**	**R/W**	**DESCRIPTION**
13-0	2EDFh	R/W	**FrameInterval** This field specifies the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.
15-14	0h	-	Rsvd. Read/Write 0's
30-16			**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame.
31			**FrameIntervalToggle** This bit is toggled by HCD whenever it loads a new value into **FrameInterval**.

6.2.15. HCFRAMEREMAINING

Table 22 - HCFRAMEREMAINING Register

REGISTER: *HCFRAMEREMAINING*			ADDRESS OFFSET: 38-3B
BITS	**RESET**	**R/W**	**DESCRIPTION**
13-0	0b	R	**FrameRemaining** This field is a 14 bit decrementing counter used to time a frame. When the Host Controller is in the USBOPERATIONAL state the counter decrements each 12 MHz clock period. When the count reaches 0, the end of a frame has been reached. The counter reloads with **FrameInterval** at that time. In addition, the counter loads when the Host Controller transitions into USBOPERATIONAL.
30-14	0h	-	Rsvd. Read/Write 0's
31	0b	R	**FrameRemainingToggle** This bit is loaded with **FrameIntervalToggle** when **FrameRemaining** is loaded.

6.2.16. HCFMNUMBER

Table 23 - HCFMNUMBER Register

REGISTER: *HCFMNUMBER*			ADDRESS OFFSET: 3C-3F
BITS	**RESET**	**R/W**	**DESCRIPTION**
15-0	0b	R	**FrameNumber** This field is a 16 bit incrementing counter. The count is incremented coincident with the loading of **FrameRemaining**. The count will roll over from 'FFFFh' to '0h.'
31-16	0h	-	Rsvd. Read/Write 0's

6.2.17. HCPERIODICSTART

Table 24 - HCPERIODICSTART Register

REGISTER: *HCPERIODICSTART*			ADDRESS OFFSET: 40-43
BITS	**RESET**	**R/W**	**DESCRIPTION**
13-0	0b	R/W	**PeriodicStart** This field contains a value used by the List Processor to determine where in a frame the Periodic List processing must begin.
31-14	0h	-	Rsvd. Read/Write 0's

6.2.18. HCLSTHRESHOLD

Table 25 - HCLSTHRESHOLD Register

REGISTER: *HCLSTHRESHOLD*			ADDRESS OFFSET: 44-47
BITS	**RESET**	**R/W**	**DESCRIPTION**
11-0	0b	R/W	**LSThreshold** This field contains a value used by the Frame Management block to determine whether or not a low speed transaction can be started in the current frame.
31-12	0h	-	Rsvd. Read/Write 0's

6.2.19. HCRHDESCRIPTORA

This register is only reset by a power-on reset (nPCIRST). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.

Table 26 - HCRHDESCRIPTORA Register

REGISTER: *HCRHDESCRIPTORA*			ADDRESS OFFSET: 48-4B
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	02h	R	**NumberDownstreamPorts** supports two downstream ports.
8	0	R/W	**PowerSwitchingMode** implements a global power switching mode. 0 = Global Switching 1 = Individual Switching This bit is only valid when **NoPowerSwitching** is cleared. This bit should be written '0'.
9	0	R/W	**NoPowerSwitching** implements global power switching. 0 = Ports are power switched. 1 = Ports are always powered on. This bit should be written to support the external system port power switching implementation.
10	0	R	**DeviceType** is not a compound device.
11	0	R/W	**OverCurrentProtectionMode** implements global over-current reporting 0 = Global Over-Current 1 = Individual Over-Current This bit is only valid when **NoOverCurrentProtection** is cleared. This bit should be written '0'.
12	0	R/W	**NoOverCurrentProtection** implements global over-current reporting 0 = Over-current status is reported 1 = Over-current status is not reported This bit should be written to support the external system port over-current implementation.

REGISTER: *HCRHDESCRIPTORA*			ADDRESS OFFSET: 48-4B
BITS	**RESET**	**R/W**	**DESCRIPTION**
23-13	0h	-	Rsvd. Read/Write 0's
31-24	01h	R/W	**PowerOnToPowerGoodTime** power switching is effective within 2 ms. The field value is represented as the number of 2 ms intervals. Only bits [25:24] are implemented as R/W. The remaining bits are read only as '0'. It is not expected that these bits be written to anything other than 1h, but limited adjustment is provided. This field should be written to support the system implementation. This field should always be written to a non-zero value.

6.2.20. HCRHDESCRIPTORB

This register is only reset by a power-on reset (nPCIRST). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.

Table 27 - HCRHDESCRIPTORB Register

REGISTER: *HCRHDESCRIPTORB*			ADDRESS OFFSET: 4C-4F
BITS	**RESET**	**R/W**	**DESCRIPTION**
15-0	0000h	R/W	**DeviceRemoveable** ports default to removable devices. 0 = Device not removable 1 = Device removable Port Bit relationship 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15 Unimplemented ports are reserved, read/write '0'.

REGISTER: *HCRHDESCRIPTORB*			ADDRESS OFFSET: 4C-4F
BITS	**RESET**	**R/W**	**DESCRIPTION**
31-16	0000h	R/W	**PortPowerControlMask** implements global-power switching. This field is only valid if **NoPowerSwitching** is cleared and **PowerSwitchingMode** is set (individual port switching). When set, the port only responds to individual port power switching commands (**Set/ClearPortPower**). When cleared, the port only responds to global power switching commands (**Set/ClearGlobalPower**). 0 = Device not removable 1 = Global-power mask Port Bit relationship 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15 Unimplemented ports are reserved, read/write '0'.

6.2.21. HCRHSTATUS

This register is reset by the USBRESET state.

Table 28 - HCRHSTATUS Register

REGISTER: *HCRHSTATUS*			ADDRESS OFFSET: 50-53
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0	R/W	(read) **LocalPowerStatus** Not Supported. Always read '0'. (write) **ClearGlobalPower** Writing a '1' issues a **ClearGlobalPower** command to the ports. Writing a '0' has no effect.
1	-	R	**OverCurrentIndicator** This bit reflects the state of the OVRCUR pin. This field is only valid if **NoOverCurrentProtection** and **OverCurrentProtectionMode** are cleared. 0 = No over-current condition 1 = Over-current condition
14-2	0h	-	Rsvd. Read/Write 0's
15	0	R/W	(read) **DeviceRemoteWakeupEnable** This bit enables ports' **ConnectStatusChange** as a remote wakeup event. 0 = disabled 1 = enabled (write) **SetRemoteWakeupEnable** Writing a '1' sets **DeviceRemoteWakeupEnable**. Writing a '0' has no effect.

REGISTER: *HCRHSTATUS*			ADDRESS OFFSET: 50-53
BITS	**RESET**	**R/W**	**DESCRIPTION**
16	0	R/W	(read) **LocalPowerStatusChange** Not supported. Always read '0'. (write) **SetGlobalPower** Write a '1' issues a **SetGlobalPower** command to the ports. Writing a '0' has no effect.
17	0	R/W	**OverCurrentIndicatorChange** This bit is set when **OverCurrentIndicator** changes. Writing a '1' clears this bit. Writing a '0' has no effect.
30-18	0h	-	Rsvd. Read/Write 0's
31	0	W	(write) **ClearRemoteWakeupEnable** Writing a '1' to this bit clears **DeviceRemoteWakeupEnable**. Writing a '1' has no effect.

6.2.22. HcRhPortStatus[1:2]

This register is reset by the USBRESET state.

Table 29 - HcRhPortStatus Register

REGISTER: *HCRHPORTSTATUS[1:2]*			ADDRESS OFFSET: 54-57,58-5B
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0	R/W	(read) **CurrentConnectStatus** 0 = No device connected. 1 = Device connected. Note: If **DeviceRemoveable** is set (not removable) this bit is always '1'. (write) **ClearPortEnable** Writing a '1' clears **PortEnableStatus**. Writing a '0' has no effect.
1	0	R/W	(read) **PortEnableStatus** 0 = Port disabled. 1 = Port enabled. (write) **SetPortEnable** Writing a '1' sets **PortEnableStatus**. Writing a '0' has no effect.
2	0	R/W	(read) **PortSuspendStatus** 0 = Port is not suspended 1 = Port is selectively suspended (write) **SetPortSuspend** Writing a '1' sets **PortSuspendStatus**. Writing a '0' has no effect.

REGISTER: *HCRHPORTSTATUS[1:2]*			ADDRESS OFFSET: 54-57,58-5B
BITS	**RESET**	**R/W**	**DESCRIPTION**
3	0	R/W	(read) **PortOverCurrentIndicator** supports global over-current reporting. This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if **NoOverCurrentProtection** is cleared and **OverCurrentProtectionMode** is set. 0 = No over-current condition 1 = Over-current condition (write) **ClearPortSuspend** Writing a '1' initiates the selective resume sequence for the port. Writing a '0' has no effect.
4	0	R/W	(read) **PortResetStatus** 0 = Port reset signal is not active. 1 = Port reset signal is active. (write) **SetPortReset** Writing a '1' sets **PortResetStatus**. Writing a '0' has no effect.
7-5	0h	-	Rsvd. Read/Write 0's
8	0	R/W	(read) **PortPowerStatus** This bit reflects the power state of the port regardless of the power switching mode. 0 = Port power is off. 1 = Port power is on. Note: If **NoPowerSwitching** is set, this bit is always read as '1'. (write) **SetPortPower** Writing a '1' sets **PortPowerStatus**. Writing a '0' has no effect.
9	0	R/W	(read) **LowSpeedDeviceAttached** This bit defines the speed (and bud idle) of the attached device. It is only valid when **CurrentConnectStatus** is set. 0 = Full Speed device 1 = Low Speed device (write) **ClearPortPower** Writing a '1' clears **PortPowerStatus**. Writing a '0' has no effect
15-10	0h	-	Rsvd. Read/Write 0's
16	0	R/W	**ConnectStatusChange** This bit indicates a connect or disconnect event has been detected. Writing a '1' clears this bit. Writing a '0' has no effect. 0 = No connect/disconnect event. 1 = Hardware detection of connect/disconnect event. Note: If DeviceRemoveable is set, this bit resets to '1'.

REGISTER: *HCRHPORTSTATUS[1:2]*			ADDRESS OFFSET: 54-57,58-5B
BITS	**RESET**	**R/W**	**DESCRIPTION**
17	0	R/W	**PortEnableStatusChange** This bit indicates that the port has been disabled due to a hardware event (cleared **PortEnableStatus**). 0 = Port has not been disabled. 1 = PortEnableStatus has been cleared.
18	0	R/W	**PortSuspendStatusChange** This bit indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed. 1 = Port resume is complete.
19	0	R/W	**PortOverCurrentIndicatorChange** This bit is set when **OverCurrentIndicator** changes. Writing a '1' clears this bit. Writing a '0' has no effect.
20	0	R/W	**PortResetStatusChange** This bit indicates that the port reset signal has completed. 0 = Port reset is not complete. 1 = Port reset is complete.
31-21	0h	-	Rsvd. Read/Write 0's

6.2.23. HceInput

Table 30 - *HceInput Register*

HCEINPUT REGISTER: *HCEINPUT*			ADDRESS OFFSET: 100
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0			**InputData** This register holds data that is written to I/O ports 60h and 64h.
31-0	0	-	Reserved

6.2.24. HCECONTROL

This register is used to enable and control the emulation hardware and report various status information.

Table 31 - HCECONTROL

REGISTER: *HCECONTROL*			ADDRESS OFFSET: 100
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**EmulationEnable** When set to 1 the Host Controller will be enabled for legacy emulation. The Host Controller will decode accesses to I/O registers 60H and 64H and generate IRQ1 and/or IRQ12 when appropriate. Additionally, the host controller will generate an emulation interrupt at appropriate times to invoke the emulation software.
1	0b	R	**EmulationInterrupt** This bit is a static decode of the emulation interrupt condition.
2	0b	R/W	**CharacterPending** When set, an emulation interrupt will be generated when the **OutputFull** bit of the *HceStatus* register is set to 0.
3	0b	R/W	**IRQEn** When set the Host Controller will generate IRQ1 or IRQ12 as long as the **OutputFull** bit in *HceStatus* is set to 1. If the **AuxOutputFull** bit of *HceStatus* is 0 then IRQ1 is generated and if it is 1, then an IRQ12 is generated.
4	0b	R/W	**ExternalIRQEn** When set to 1, IRQ1 and IRQ12 from the keyboard controller will cause an emulation interrupt. The function controlled by this bit is independent of the setting of the **EmulationEnable** bit in this register.
5	0b	R/W	**GateA20Sequence** Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
6	0b	R/W	**IRQ1Active** Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0).. SW write of a 0 to this bit has no effect.
7	0b	R/W	**IRQ12Active** Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0).. SW write of a 0 to this bit has no effect.
8	0b	R/W	**A20State** Indicates current state of Gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
9-31	-	-	Reserved- read 0

6.2.25. HCEINPUT

This register is the emulation side of the legacy Input Buffer register.

Table 32 - HCEINPUT Register

REGISTER: *HCEINPUT*			ADDRESS OFFSET: 104
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	X		**InputData** This register holds data that is written to I/O ports 60h and 64h.
31-0	-	-	Reserved- read 0

6.2.26. HCEOUTPUT

This register is the emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.

Table 33 - HCEOUTPUT Register

REGISTER: *HCEOUTPUT*			ADDRESS OFFSET: 108
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	X		**OutputData** This register hosts data that is returned when an I/O read of port 60h is performed by application software.
31-0	-	-	Reserved - read 0

6.2.27. HCESTATUS

This register is the emulation side of the legacy Status register.

Table 34 - HCESTATUS Register

REGISTER: *HCESTATUS*			ADDRESS OFFSET: 10C
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**OutputFull** The HC will set this bit to 0 on a read of I/O port 60h. If **IRQEn** is set and **AuxOutputFull** is set to 0 then an IRQ1 is generated as long as this bit is set to 1. If **IRQEn** is set and **AuxOutputFull** is set to 1 then and IRQ12 will be generated a long as this bit is set to 1. While this bit is 0 and **CharacterPending** in *HceControl* is set to 1, an emulation interrupt condition exists.
1	0b	R/W	**InputFull** Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
2	0b	R/W	**Flag** Nominally used as a system flag by software to indicate a warm or cold boot.

REGISTER: *HCESTATUS*			ADDRESS OFFSET: 10C
BITS	**RESET**	**R/W**	**DESCRIPTION**
3	0b	R/W	**CmdData** The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h the HC will set this bit to 1.
4	0b	R/W	**Inhibit Switch** This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
5	0b	R/W	**AuxOutputFull** IRQ12 is asserted whenever this bit is set to 1 and **OutputFull** is set to 1 and the **IRQEn** bit is set.
6	0b	R/W	**Timeout** Used to indicate a time-out
7	0b	R/W	**Parity** Indicates parity error on keyboard/mouse data.
8-31	-	-	Reserved - read 0

7. POWER MANAGEMENT REGISTER DESCRIPTION (Function 3)

Upon reset, the SLC90E46 sets its internal registers to predetermined default states, which represents the minimum functionality feature set required to bring up the system. It is the responsibility of the BIOS to properly program the configuration registers to achieve optimal system performance.

7.1. Power Management Register Summary (Function 3)

7.1.1. PCI Configuration Registers (Function 3)

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS TYPE
00-01h	VID	Vendor Identification	RO
02-03	DID	Device Identification	RO
04-05	PCICMD	PCI Command Register	R/W
06-07	PCISTS	PCI Status Register	R/W
08	RID	Revision ID	RO
09-0B	CLASSCODE	Class Code	RO
0D		Reserved	R/W
0E	HEDT	Header Type	RO
0F-1F		Reserved	
20-3B		Reserved	
3C	INTLINE	Power Management Interrupt Line	R/W
3D	INTPIN	Power Management Interrupt Pin	R/W
3E-3F		Reserved	
40-43	PMBA	Power Management Base Address Register	R/W
44-47	CNTA	Count A Register for IDLE Timers	R/W
48-4B	CNTB	Count B Register for Burst & IDLE Timers	R/W
4C-4F	GPICTL	General Purpose Input Control	R/W
50-52	DEVRESD	Device Resource D Register	R/W
53		Reserved	
54-57	DEVACTA	Device Activity A	R/W
58-5B	DEVACTB	Device Activity B	R/W
5C-5F	DEVRESA	Device Resource A	R/W
60-63	DEVRESB	Device Resource B	R/W
64-67	DEVRESC	Device Resource C	R/W
68-6A	DEVRESE	Device Resource E	R/W
6C-6F	DEVRESF	Device Resource F	R/W
70-72	DEVRESG	Device Resource G	R/W
73		Reserved	
74-77	DEVRESH	Device Resource H	R/W
78-7B	DEVRESI	Device Resource I	R/W
7C-7F	DEVRESJ	Device Resource J	R/W
80	PMREGMISC	Miscellaneous Power Management	R/W
81-89		Reserved	
90-93	SMBBA	SMBus Base Address	R/W
94-D1		Reserved	

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS TYPE
D2	SMBHSTCFG	SMBus Host Configuration	R/W
D3	SMBREV	SMBus Revision ID	RO
D4	SMBSLVC	SMBus Slave Command	R/W
D5	SMBSHDW1	SMBus Slave Shadow Port 1	R/W
D6	SMBSHDW2	SMBus Slave Shadow Port 2	R/W
D7-FF		Reserved	

7.1.2. Power Management IO Space Registers (Function 3)

ADDRESS Offset from Base	ACCESS TYPE	MNEMONIC	REGISTER NAME
00h	R/W	PMSTS	Power Management Status Register
02h	R/W	PMEN	Power Management Resume Enable Register
04h	R/W	PMCNTRL	Power Management Control Register
06h			Reserved
08h	RO	PMTMR	Power Management Timer
09 - 0Bh			Reserved
0Ch	R/W	GPSTS	General Purpose Status Register
0Eh	R/W	GPEN	General Purpose Enable Register
10h	R/W	PCNTRL	Processor Control Register
14h	RO	PLVL2	Processor Level 2 Register
15h	RO	PLVL3	Processor Level 3 Register
16 -17h			Reserved
18h	R/W	GLBSTS	Global Status Register
1A - 1Bh			Reserved
1Ch	R/W	DEVSTS	Device Status Register
20h	R/W	GLBEN	Global Enable Register
22 - 27h			Reserved
28h	R/W	GLBCTL	Global Control Register
2Ch	R/W	DEVCTL	Device Control Register
30h	RO	GPIREG	General Purpose Input Register
34h	R/W	GPOREG	General Purpose Output Register

7.1.3. SMBus Controller IO Space Registers (Function 3)

ADDRESS Offset from Base	ACCESS TYPE	MNEMONIC	REGISTER NAME
00h	R/W	SMBHSTSTS	SMBus Host Status Register
01h	R/W	SMBSLVSTS	SMBus Slave Status Register
02h	R/W	SMBHSTCNT	SMBus Host Count Register
03h	R/W	SMBHSTCMD	SMBus Host Command Register
04h	R/W	SMBHSTADD	SMBus Host Address Register
05h	R/W	SMBHSTDAT0	SMBus Host Data 0
06h	R/W	SMBHSTDAT1	SMBus Host Data 1
07h	R/W	SMBBLKDAT	SMBus Block Data
08h	R/W	SMBSLVCNT	SMBus Slave Count

ADDRESS Offset from Base	ACCESS TYPE	MNEMONIC	REGISTER NAME
09h	R/W	SMBSHDWCMD	SMBus Shadow Command Register
0Ah	R/W	SMBSLVEVT	SMBus Slave Event Register
0Ch	R/W	SMBSLVDAT	SMBus Slave Data Register

7.2. PCI Configuration Registers (Function 3)

7.2.1. VID Vendor Identification Register

Offset Address: 00 - 01h
Default Value: 10B8h
Access: Read

7.2.2. DID Device Identification Register

Offset Address: 02 - 03h
Default Value: 9463h
Access: Read

7.2.3. PCICMD PCI Command Register

Offset Address: 04 - 05h
Default Value: 00h
Access: Read

BIT	FUNCTION
15-10	Reserved.
9	Fast Back-to-Back: not implemented, hardwired to 0.
8-5	Reserved. Read as 0
4	**Memory Write and Invalidate Enable**. This bit is hardwires to 0.
3	**Special Cycle Enable (SCE):** 1=Enable, the SLC90E46 recognizes the x86 Stop Grant special cycle. 0=Disable. The SCE bit in function 0 PCI Command Register controls SLC90E46 response to the Shutdown special cycle.
2	**Bus Master Enable:** not implemented, hardwired to 0.
1	**Memory Access Enable**: (Not Implemented). 1=Enable. 0=Disable. This bit controls the access to the memory space. If this bit is set, access to the memory space by power management logic is enabled.
0	**IO Space Enable (IOSE) - R/W** 1=Enable, 0=Disable. This bit controls the access to the SMBus I/O space registers whose base address is described in the SMBus Base Address register. When it is a 1, access to the SMBus IO registers are enabled. The base register for the I/O registers must be programmed before this bit is set. **When disabled, all IO accesses associated with SMBus Base Address are disabled.** This bit functions independent of the state of Function 3 Power Management IO Space Enable (PMIOSE) bit (PMREGMISC, bit 0).

7.2.4. PCISTS PCI Device Status Register

Offset Address: 06 - 07h
Default Value: 0280h
Access: Read/Write

BIT	FUNCTION
15	**Detected Parity Error**. Not implemented, hardwired to 0.
14	**Signaled nSERR Status.** Not implemented, hardwired to 0.
13	**Master Abort Status.** Not implemented, hardwired to 0.
12	**Received Target Abort Status**. When the Bus Master IDE interface function is a master on the PCI bus and receives a target abort, this bit is set to 1. **To reset the bit, write a 1 to it.**
11	**Signaled Target Abort.** This bit is set when the SLC90E46 power management function is targeted with a transaction that the SLC90E46 terminates with a target abort. To reset this bit, write a 1 to this bit.
10-9	**nDEVSEL Timing**. Always 01 to select "medium" timing for nDEVSEL assertion, which is two PCI clocks after the assertion of nFRAME, when performing a positive decode. nDEVSEL timing does not include configuration cycles.
8	**Data Parity Detected.** Always 0, not implemented.
7	**Fast Back-to-Back Capable**: **RO**. Hardwired to 1. This bit indicates to the PCI master that the power management function as a target is capable of accepting fast back-to-back transaction.
6-0	Reserved.

7.2.5. RID Revision Identification Register

Offset Address: 08h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
7-0	Hardwired to the revision number, which is set to 00 as the initial number.

7.2.6. CLASSC Class Code Register

Offset Address: 09 - 0Bh
Default Value: 068000h
Access: Read

BIT	FUNCTION
23-16	**Base Class Code**. 06h: Bridge Device.
15-8	**Sub-Class Code**. 80h: Other Bridge Device.
7-0	Programming Interface (PI). 00h: No specific register level programming defined.

7.2.7. HEDT Header Type Register

Offset Address: 0Eh
Default Value: 00h
Access: Read

BIT	FUNCTION
7-0	(Device Type) 00h: The power management module is a single function device.

7.2.8. INTLINE Power Management Interrupt Line

Address offset: 3Ch
Value: 00h
Attribute: Read/Write

The value in this register has no effect on SLC90E46 hardware operations.

7.2.9. INTPIN Power Management Interrupt Pin

Address offset: 3Dh
Value: 01h
Attribute: Read/Write

BIT	FUNCTION
7-3	**Reserved.**
2-0	**Serial Bus Module Interrupt Routing.** This field is hardwired to 01h to indicate that PCI interrupt pin nPIRQA is used.

7.2.10. PMBA Power Management Base Address

Address offset: 40-43h
Value: 00000001h
Attribute: Read/Write

BIT	FUNCTION
31-16	**Reserved.** Hardwired to 0. Must be written as 0s.
15-6	**Index Register Base Address.** Bits [15-6] correspond to I/O address signals AD[15-6], respectively.
5-1	**Reserved.** Read as 0.
0	**Resource Type Indicator - Read Only.** This bit is hardwired to 1 indicating that the base address field in this register maps to I/O space.

7.2.11. CNTA Count A Register for Idle Timers (Function 3)

Address Offset: 44-47h
Default Value: 00h
Access: Read/Write

This register contains the initial counts of the idle timers for device 0-11, the selection bits for the timer granularity of the timers for devices 0, 1, 2 and 3. In addition, it contains the count for the slow burst timer.

BIT	FUNCTION
31-28	**Slow Burst Timer Count (SB_CNT) - R/W.** Specifies the initial and reload value of the slow burst timer.
27-23	**Idle Timer Count D (IDL_CNTD) - R/W.** Specifies the initial and reload count of the device 11 (user interface) idle timer.
22	**Device 11 Idle Timer Resolution Selection (IDL_SEL_DEV11)-R/W.** Selects the clock resolution of the device 11 (user interface) idle timer. 0: 1 second granular. 1: 1 minute granular.
21-17	**Idle Timer Count C (IDL_CNTC) - R/W.** Specifies the initial and reload count of the device 9-10 (generic range) idle timers.
16-12	**Idle Timer Count B (IDL_CNTB) - R/W.** Specifies the initial and reload count of the device 4-7 (audio, floppy, serial ports, parallel port) idle timers.
11-8	**SW Idle Timer Count (SW_CNT) - R/W.** Specifies the initial and reload count of the device 3 (secondary IDE drive 1, software SMI) idle timer.
7	**Device 3 Idle Timer Resolution (IDL_SEL_DEV3) - R/W.** Selects the clock source for the device 3 (secondary IDE drive 1, software SMI) idle timer. 0: 8 second granular. 1: 1ms granular.
6	**Device 2 Idle Timer Resolution (IDL_SEL_DEV2) - R/W.** Selects the clock source for the device 2 (secondary IDE 0) idle timer. 0: 8 second granular. 1: 1 second granular.
5	**Device 1 Idle Timer Resolution (IDL_SEL_DEV1) - R/W.** Selects the clock source for the device 1 (primary IDE 1) idle timer. 0: 8 second granular. 1: 1 second granular.
4	**Device 0 Idle Timer Resolution (IDL_SEL_DEV0) - R/W.** Selects the clock source for the device 0 (primary IDE 0) idle timer. 0: 8 second granular. 1: 1 second granular.
3-0	**Idle Timer Count A (IDL_CNTA) - R/W.** Specifies the initial and reload count of the device 2-0 (primary IDE drives 0 and 1, secondary IDE drive 0) idle timers.

7.2.12. CNTB Count B Register for Burst & Idle Timers (Function 3)

Address Offset: 48-4Bh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-25	**Reserved.** Read as 0.
24	**Video Status (VID_STS) - R/W Clear.** 1: The PCI bus utilization monitor has detected PCI activity which exceeds its defined threshold (see Device Monitor 11's description). This bit is set by hardware and reset by writing a 1 to this bit position.
23	**Reserved.** Read as 0.
22-18	**Bus Master Timer Count C (BM_CNT) - R/W.** Specifies the initial and reload count of the device 8 (parallel port and PCI bus master) idle timer.
17-16	**Reserved.** Read as 0.
15	**Device 8 Idle Timer Resolution (IDL_SEL_DEV8) - R/W.** Selects the clock source for the device 8 (parallel port) idle timer. 0: 1 second granular. 1: 1ms granular.
14	**ZZ Enable (ZZ_EN) - R/W.** 1: Enable SLC90E46 assertion of the ZZ signal. 0: Disable. When enabled, the SLC90E46 will assert ZZ signal under certain conditions when entering clock control mode. Whether or not ZZ is asserted depends on: 1. Time from nSTPCLK assertion to Stop Grant Cycle. 2. Frequency of any enabled Stop Break or Burst Events. 3. Programmed throttles duty cycle if throttling enabled.
13-11	**Thermal Duty Cycle (THRM_DTY) - R/W.** This 3-bit field determines the duty cycle for the clock control thermal throttling mode (nTHRM is asserted). The duty cycle indicates the percentage of time the nSTPCLK signal is asserted while in the thermal throttle mode. The field is decoded as follows: 000: Reserved. 001: 12.5%. 010: 25%. 011: 37.5% 100: 50% 101: 62.5% 110: 75% 111: 87.5% The thermal clock throttling is not controlled by THRM_EN.
10-6	**Processor PLL Lock Count (CPU_LCK) - R/W.** Specifies the initial count of fast burst timer when used to measure the processor PLL lock time. The fast burst timer is loaded with the CPU_LCK value and the appropriate clock source selected when the processor transitions from the stop clock or deep sleep state.
5	**Processor PLL Lock Resolution (CPU_SEL) - R/W.** Selects the clock resolution used for the fast burst timer when it is used to count the processor's PLL lock time. 0: 1ms granular. 1: 1us granular.
4-0	**Fast Burst Timer Count (FB_CNT) - R/W.** Specifies the initial and reload count of the fast burst timer.

7.2.13. GPICTL General Purpose Input Control

Address Offset: 4C-4Fh
Default Value: 00h
Access: Read/Write

This register contains the enable bits, the polarity bits and edge selection bits for the General Purpose IO in device monitors 1-13.

BIT	FUNCTION
31-28	**Reserved.**
27	**GPI Edge Select (GPI_EDG_DEV13) - R/W.** Selects edge or level sensitivity of device monitor 13 GPI signal. 0: level, 1: edge.
26	**GPI Edge Select (GPI_EDG_DEV12) - R/W.** Selects edge or level sensitivity of device monitor 12 GPI signal. 0: level, 1: edge.
25-13	**GPI Polarity Select (GPI_POL_DEV[13-1]) - R/W.** Selects the assertion polarity for an enabled GPI signal for device monitors 1-13. Bit 25 corresponds to device monitor 13 and bit 13 corresponds to device monitor 1. 0: asserted HIGH. 1: asserted LOW.
12-0	**GPI Enable (GPI_EN_DEV[13-1]) - R/W.** Bit 12 corresponds to device monitor 13 and bit 0 corresponds to device monitor 0. 1: Enable the device monitor's GPI signal into the trap and idle decode logic for devices [13:1]. 0: Disable.

The following table illustrates which GPI signals associated with which devices.

DEVICE MONITORING	OPTIONAL GPI SIGNAL
DEV0	None
DEV1	GPI5
DEV2	GPI6
DEV3	GPI0
DEV4	GPI13
DEV5	GPI14
DEV6	GPI15
DEV7	GPI16
DEV8	GPI17
DEV9	GPI4
DEV10	GPI18
DEV11	GPI19
DEV12	GPI20
DEV13	GPI21

7.2.14. DEVRESD Device Resource D Register

Address Offset: 50h-52h
Default Value: 00h
Access: Read/Write

This register contains the event enable bits for DMA channels 0, 1, 3, 5, 6, 7. It also contains the floppy disk controller monitor enable bit, serial port monitor enable bits. Device 11 IRQ1 monitor enable bit, Device 11 IRQ12 monitor enable bit and LPT DMA select bits.

BIT	FUNCTION
23	**Reserved.**
22-21	**LPT DMA Select (LPT_DMA_SEL) - R/W.** Selects the active DACK signal used to reload the idle timer for device 8 (parallel port). Enabled by RES_EN_DEV8 bit (bit 17 of the register). 00:DACK0 01: DACK1 10:DACK3 11:Reserved.
20	**Device 11 IRQ12 Enable (IRQ12_EN_DEV11) - R/W.** 1: Enable an asserted IRQ12/M signal (mouse activity) to generate a device 11 (user interface) decode event. 0: Disable.
19	**Device 11 IRQ1 Enable (IRQ1_EN_DEV11) - R/W.** 1: Enable an asserted IRQ1 signal (keyboard activity) to generate a device 11 (user interface) decode event. 0:Disable.
18	**LPT Port Enable (LPT_MON_EN) - R/W.** 1: Enable access to parallel port address range, LPT_DEC_SEL (bits[26-25] of DEVRESB register), to generate a device 8 (parallel port) decode event. 0: Disable.
17	**LPT DMA Monitor Enable (RES_EN_DEV8) - R/W.** 1: Enable the selected DACKs , which is controlled by LPT_DMA_SEL (bits[22-21] of the register), to generate a device 8 (parallel port) decode event. 0: Disable.
16	**Serial Port B Monitor Enable (SB_MON_EN) - R/W.** 1: Enable accesses to serial port address range (COMB_DEC_SEL, bits[30-28] of DEVRESC) to generate a device 7 (serial port B) decode event. 0: Disable.
15	**Reserved.**
14	**Serial Port A Monitor Enable (SA_MON_EN) - R/W.** 1: Enable accesses to serial port address range (COMA_DEC_SEL, bits[26-24] of DEVRESC) to generate a device 6 (serial port A) decode event. 0: Disable.
13	**Reserved**
12	**Floppy Disk Controller Monitor Enable (FDC_MON_EN) - R/W.** 1: Enable accesses to floppy disk controller address range (FDC_DEC_SEL, bit 28 of DEVRESB) to generate a device 5 (floppy controller) decode event. 0: Disable.
11	**FDC DMA Monitor Enable (RES_EN_DEV5) - R/W.** 1: Enable nDACK2 to generate a device 5 reload event. 0: Disable

BIT	FUNCTION
10-6	**Reserved.**
5	**DACK7 Enable (DACK7_EN_DEV4) - R/W** 1: Enable nDACK7 to generate a device 4 (audio controller) reload event. 0: Disable.
4	**DACK6 Enable (DACK6_EN_DEV4) - R/W** 1: Enable nDACK6 to generate a device 4 (audio controller) reload event. 0: Disable.
3	**DACK5 Enable (DACK5_EN_DEV4) - R/W** 1: Enable nDACK5 to generate a device 4 (audio controller) reload event. 0: Disable.
2	**DACK3 Enable (DACK3_EN_DEV4) - R/W** 1: Enable nDACK3 to generate a device 4 (audio controller) reload event. 0: Disable.
1	**DACK1 Enable (DACK1_EN_DEV4) - R/W** 1: Enable nDACK1 to generate a device 4 (audio controller) reload event. 0: Disable.
0	**DACK0 Enable (DACK0_EN_DEV4) - R/W** 1: Enable nDACK0 to generate a device 4 (audio controller) reload event. 0: Disable.

7.2.15. DEVACTA Device Activity A

Address Offset: 54-57h
Default Value: 00h
Access: Read/Write

This register contains bits that enable Device Activity as Global Standby Timer Reload events or Clock Events (Burst or Break).

BIT	FUNCTION
31	**Device 5 Reload Select (BRLD_SEL_DEV5) - R/W.** Select which burst timer is reloaded upon an enabled device 5 monitor idle event. 1: Reload the fast burst timer. 0: Reload the slow burst timer.
30	**Device 3 Reload Select (BRLD_SEL_DEV3) - R/W.** Select which burst timer is reloaded upon an enabled device 3 monitor idle event. 1: Reload the fast burst timer. 0: Reload the slow burst timer.
29	**Device 2 Reload Select (BRLD_SEL_DEV2) - R/W.** Select which burst timer is reloaded upon an enabled device 2 monitor idle event. 1: Reload the fast burst timer. 0: Reload the slow burst timer.
28	**Device 1 Reload Select (BRLD_SEL_DEV1) - R/W.** Select which burst timer is reloaded upon an enabled device 1 monitor idle event. 1: Reload the fast burst timer. 0: Reload the slow burst timer.

27-14	**Burst Timer Reload Enable (BRLD_EN_DEV[13-0]) - R/W.** Bit 27 corresponds to device monitor 13 and bit 14 corresponds to device monitor 0. 1: Enable reload events from the respective device monitor to reload the enabled burst timer or generate a Stop Break Event. 0: Disable.
13-0	**Global Standby Timer Reload Enable (GRLD_EN_DEV[13-0]) - R/W.** Bit 13 corresponds to device monitor 13 and bit 0 corresponds to device monitor 0. 1: Enable reload events from the respective device monitor to reload the Global Standby Timer. 0: Disable.

7.2.16. DEVACTB Device Activity B

Address Offset: 58-5Bh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-26	**Reserved.**
25	**APMC Enable (APMC_EN) - R/W.** 1: Enable generation of nSMI when APMC register is read and nSMI is enabled. 0: Disable.
24	**Video Enable (VIDEO_EN) - R/W.** This logic detects PCI bus utilization as set by two fields: BUS_UTIL an %BUS_UTIL. 1: Enable the video detect (PCI Bus Utilization) logic to generate a timer reload event for device monitor 11.. 0: Disable.
23-16	**Percentage Bus Utilization Threshold (%BUS_UTIL) - R/W.** This field controls the percentage of time that the minimum bus utilization threshold (represented by the BUS_UTIL field) must be maintained in order to generate a video event. The actual count is measured by the number of time slices that exceeds the BUS_UTIL within a 256 time slice window.
15-8	**Bus Utilization Threshold (BUS_UTIL) - R/W.** This field controls the threshold for bus utilization detection. If the video detect logic finds more PCI data phases than specified by BUS_UTIL within a 256 clock period (time slice), then that time slice is counted.
7	**Reserved.**
6	**IRQ Global Reload Enable (GRLD_EN_IRQ) - R/W.** 1: Enable an unmasked IRQ[1,3-7,9-15], NMI, INIT to, when asserted, reload the Global Standby Timer. 0: Disable.
5	**IRQ8 Burst Timer Reload Enable (BRLD_EN_IRQ8) - R/W** 1: Enable an unmasked nIRQ8 to, when asserted, generate a Fast Burst Timer reload or Stop Break event. 0: Disable.
4	**PME Burst Timer Reload Enable (BRLD_EN_PME) - R/W** 1: Enable an asserted nSMI, nGPI1, nPWRBTN, or LID signal to generate a Fast Burst Timer reload or Stop Break event. 0: Disable.

BIT	FUNCTION
3	**Undefined.** Must be written as a 0.
2	**Keyboard/Mouse Global Reload Enable (GRLD_EN_KBC_MS) - R/W** 1: Enable an assertion of IRQ1 or IRQ12/M to reload the Global Standby Timer. 0: Disable.
1	**IRQ Burst Timer Reload Enable (BRLD_EN_IRQ) - R/W** 1: Enable an unmasked IRQ[1,3-7,9-15], NMI or INIT to generate a Burst event or Stop Break event. 0: Disable.
0	**IRQ0 Burst Timer Reload Enable (BRLD_EN_IRQ0) - R/W.** 1: Enable an unmasked IRQ0 to generate a Burst event or Stop Break event. 0: Disable.

7.2.17. DEVRESA Device Resource A

Address Offset: 5C-5Fh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31	**Device 8 EIO Enable (EIO_EN_DEV8) - R/W.** 1: Enable PCI access to the device 8 enabled I/O range to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The LPT_MON_EN must be set to enable the decode. 0: Disable.
30	**Device 13 EIO Enable (EIO_EN_DEV13) - R/W.** 1: Enable PCI access to the device 13 enabled **memory and I/O** range to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The MEM_EN_DEV13 or IO_EN_DEV13 must be set to enable the memory or IO decodes respectively. 0: Disable.
29	**Device 12 EIO Enable (EIO_EN_DEV12) - R/W.** 1: Enable PCI access to the device 12 enabled **memory and I/O** range to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The MEM_EN_DEV12 or IO_EN_DEV12 must be set to enable the memory or IO decodes respectively. 0: Disable.
28	**Device 11 Keyboard Enable (KBC_EN_DEV11) - R/W.** 1: Enable PCI bus decode for accesses to keyboard controller I/O ports (60h and 64h). 0: Disable. The EIO enable bit, idle enable bit, or trap enable bit for this device must also be set in order to enable these respective functions.
27	**Graphics A/B Segment Memory Enable (GRAPH_AB_EN) - R/W.** 1: Enable PCI bus decode for accesses to the PC compatible frame buffer ranges (A and B segments). 0: Disable. The idle enable bit or trap enable bit for this device (DEV11) must also be set in order to enable these respective functions. SLC90E46 does not positive decode these accesses for forwarding to the ISA bus.

BIT	FUNCTION
26	**Graphics I/O Enable (GRAPH_IO_EN) - R/W.** 1: Enable PCI bus decode for accesses to the VGA I/O address (3B0h-3DFh). 0: Disable. The idle enable bit or trap enable bit for this device (DEV11) must also be set in order to enable these respective functions. SLC90E46 does not positive decode these accesses for forwarding to the ISA bus.
25	**Sound Blaster EIO Enable(SB_EIO_EN) - R/W.** 1: Enable PCI bus decode for accesses to the SoundBlaster device enabled decode ranges (bits[3, 5:6] of the register) to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. 0: Disable. The SB_EN bit (bit 3 of the register) must be set to enable their respective ranges.
24	**Linear Frame Buffer Decode Enable (LFB_DEC_EN) - R/W.** 1: Enable PCI bus decode for accesses to the generic memory range for linear frame buffer. 0: Disable. The linear frame buffer address range is defined by the linear frame buffer base address and mask bits (bits [23:10] of the register). The idle enable bit or trap enable bit for the device (DEV11) must also be set in order to enable
23-22	**Linear Frame Buffer Address Mask (LFB_MASK_DEV11) - R/W.** This field defines a 2-bit mask for the linear frame buffer address, corresponding to AD[21-20]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. This field defines the size of the linear frame buffer window. Note that programming these bits to '10' results in a split address range.
21-10	**Linear Frame Buffer Base Address (LFB_BASE_DEV11) - R/W** This field defines the 12-bit memory base address range, corresponding to AD[31-20] for the linear frame buffer address. This field in conjunction with the LFB_MASK_DEV11 field defines a 1Mbyte to 8 Mbyte linear frame buffer that can be enabled for monitoring through device 11.
9-8	**Microsoft Sound System Decode Select (MSS_SEL) - R/W** This field is used to select the Microsoft Sound System decode range enabled with bit 7. This field is decoded as follows: 00: 530h-537h 01: 604h-60Bh 10: E80h-E87h 11: F40h-F47h
7	**Microsoft Sound System Decode Enable (MSS_EN) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the MSS_SEL field. 0: Disable. The EIO enable bit, idle enable bit, or trap enable bit for device 4 must also be set in order to enable those respective functions.

BIT	FUNCTION
6-5	**Sound Blaster Decode Select (SB_SEL) -R/W.** Selects the Sound Blaster decode range which can be enabled through bit 3. This field is decoded as follows: 00: 220-22Fh, 230-233h 01: 240-24Fh, 250-253h 10: 260-26Fh, 270-273h 11: 280-28Fh, 290-293h
4	**Game Port Enable (GAME_EN) - R/W.** 1: Enable PCI bus decode for accesses to the Game port I/O address range (200-207h). 0: Disable. The Game Port EIO enable bit, or Device 4 idle enable bit or trap enable must also be set in order to enable the respective functions.
3	**Sound Blaster 8/16 bit Decode Enable (SB_EN) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the SB_SEL field and to game port (200-207h) and ADLIB (388-38Bh) address range. 0: Disable. The SoundBlaster EIO enable bit, idle enable bit or trap enable bit of device 4 must also be set in order to enable those respective functions.
2-1	**MIDI Decode Select (MIDI_SEL) - R/W** This field is used to select the MIDI decode range enabled with bit 1. This field is decoded as follows: 00: 300-303h 01: 310-313h 10: 320-323h 11: 330-333h
0	**MIDI Enable (MIDI_EN) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the MIDI_SEL field. 0: Disable. The EIO enable bit, idle enable bit, or trap enable bit for device 4 must also be set in order to enable those respective functions.

7.2.18. DEVRESB Device Resource B

Address Offset: 60-63h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31	**Game Port EIO Enable (GAME_EIO_EN) - R/W** 1: Enable PCI bus decode for accesses to the Game Port enabled decode ranges to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. 0: Disable. The GAME_EN bit, bit 4 of DEVRESA, must be set to enable this range.
30	**Keyboard EIO Enable (KBC_EIO_EN) - R/W.** 1: Enable PCI access to the keyboard controller enabled IO ranges (60h and 64h) to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The KBC_EN_DEV11 of DEVRESA must be set to enable the decode. 0: Disable.
29	**Device 5 EIO Enable (EIO_EN_DEV5) - R/W.** 1: Enable PCI access to the floppy disk controller enabled I/O ranges selected by FDC_DEC_SEL field of the register to be claimed by SLC90E46 and forwarded to the ISA/EIO bus. The FDC_MON_EN, bit 5 of DEVRESD, must be set to enable the decode. 0: Disable.
28	**Floppy Disk Controller Decode Select (FDC_DEC_SEL) - R/W.** Selects the FDC I/O range enabled with bit 29. This field is decoded as follows: 1: Primary FDC address (3F0h-3F5h, 3F7h) 0: Secondary FDC address (370h-375h, 377h)
27	**Reserved.**
26-25	**LPT Controller Decode Select (LPT_DEC_SEL) - R/W.** Selects the parallel port (device 8) I/O range enabled with the LPT_MON_EN bit of DEVRESD. This field is decoded as follows: 00: 3BCh-3BFh, 7BCh-7BEh 01: 378h-37Fh, 778h-77Ah 10: 278h-27Fh, 678h-67Ah 11: Reserved.
24	**Microsoft Sound System EIO Enable (MSS_EIO_EN) - R/W.** 1: Enable PCI bus decode for accesses to the Microsoft Sound System enabled decode ranges, bits [9-7] of DEVRESA, to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. 0: Disable. The MSS_EN of DEVRESA must be set to enable this range.

BIT	FUNCTION
23	**Device 9 Generic Decode Chip-Select (CS_EN_DEV9) - R/W.** 1: Enable assertion of the chip-select signal nPCS0 for all accesses within the device 9 I/O decode range. The EIO_EN_DEV9 bit of the register must also be set to enable this function. 0: Disable.
22	**Device 9 EIO Enable (EIO_EN_DEV9) - R/W** 1: Enable PCI access to the device 9 enabled I/O range or embedded controller IO range to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The GDEC_MON_DEV9 bit or EC_EN_DEV9 bit must be set to enable the decode. 0: Disable.
21	**Device 9 Generic Decode Monitor Enable (GDEC_MON_DEV9) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the BASE_DEV9 and MASK_DEV9 fields. 0: Disable. The EIO enable bit, idle enable bit, or trap enable bit for device 9 must also be set in order to enable these respective functions.
20	**MIDI EIO Enable (MIDI_EIO_EN) - R/W** 1: Enable PCI bus decode for accesses to the MIDI enabled decode ranges, bits [2-0] of DEVRESA, to be claimed by the SLC90E46 and forwarded to the ISA / EIO bus. 0: Disable. The MIDI_EN of DEVRESA must be set to enable this range.
19-16	**Device 9 Generic Decode Mask (MASK_DEV9) - R/W.** Specifies the 4-bit I/O base address mask used to determine the IO address range size for device 9 accesses. MASK_DEV9 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.
15-0	**Device 9 Generic Decode Base Address (BASE_DEV9) - R/W.** Specifies the 16-bit I/O base address range (AD[15-0]) for the device 9 I/O range. When this field is combined with MASK_DEV9 field, an I/O range is defined starting from the base address register value to the size defined by the mask register.

7.2.19. DEVRESC Device Resource C

Address Offset: 64-67h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31	**Device 7 EIO Enable (EIO_EN_DEV7) - R/W.** 1: Enable PCI access to the device 7 (serial port B) enabled IO ranges selected by COMB_DEC_SEL field to be claimed by SLC90E46 and forwarded to the ISA/EIO bus. The SB_MON_EN bit of DEVRESD must be set to enable the decode. 0: Disable.

BIT	FUNCTION
30-28	**Serial Port B Decode Select (COMB_DEC_SEL) - R/W.** Selects the I/O range that the Serial Port B (Device 7) decode responds to. This field is decoded as follows: 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)
27	**Device 6 EIO Enable (EIO_EN_DEV6) - R/W.** 1: Enable PCI access to the device 6 (serial port A) enabled IO ranges selected by COMA_DEC_SEL field to be claimed by SLC90E46 and forwarded to the ISA/EIO bus. The SA_MON_EN bit of DEVRESD must be set to enable the decode. 0: Disable.
26-24	**Serial Port A Decode Select (COMA_DEC_SEL) - R/W.** Selects the I/O range that the Serial Port A (Device 6) decode responds to. This field is decoded as follows: 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)
23	**Device 10 Generic Decode Chip-Select (CS_EN_DEV10) - R/W.** 1: Enable assertion of the chip-select signal nPCS1 for all accesses within the device 10 I/O decode range. The EIO_EN_DEV10 bit of the register must also be set to enable this function. 0: Disable.
22	**Device 10 EIO Enable (EIO_EN_DEV10) - R/W** 1: Enable PCI access to the device 10 enabled I/O range or embedded controller IO range to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. The GDEC_MON_DEV10 bit must be set to enable the decode. 0: Disable.
21	**Device 10 Generic Decode Monitor Enable (GDEC_MON_DEV10) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the BASE_DEV10 and MASK_DEV10 fields. 0: Disable. The EIO enable bit, idle enable bit, or trap enable bit for device 10 must also be set in order to enable these respective functions.
20	**Reserved.**
19-16	**Device 10 Generic Decode Mask (MASK_DEV10) - R/W.** Specifies the 4 bit I/O base address mask used to determine the IO address range size for device 10 accesses. MASK_DEV10 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.

BIT	FUNCTION
15-0	**Device 10 Generic Decode Base Address (BASE_DEV10) - R/W.** Specifies the 16 bit I/O base address range (AD[15-0]) for the device 10 I/O range. When this field is combined with MASK_DEV10 field, an I/O range is defined starting from the base address register value to the size defined by the mask register.

7.2.20. DEVRESE Device Resource E

Address Offset: 68-6Ah
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
23-21	**Reserved.**
20	**Device 12 I/O Monitor Enable (IO_EN_DEV12) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the IBASE_DEV12 and IMASK_DEV12 fields. 0: Disable. The EIO enable bit or trap enable bit for device 12 must also be set in order to enable these respective functions.
19-16	**Device 12 I/O Decode Mask (IMASK_DEV12) - R/W.** Specifies the 4-bit I/O base address mask used to determine the IO address range size for device 12 accesses. IMASK_DEV12 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.
15-0	**Device 12 I/O Decode Base Address (IBASE_DEV12) - R/W.** Specifies the 16-bit I/O base address range (AD[15-0]) for the device 12 I/O range. When this field is combined with IMASK_DEV12 field, an I/O range is defined starting from the base address register value to the size defined by the mask register.

7.2.21. DEVRESF Device Resource F

Address Offset: 6C-6Fh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-15	**Device 12 Memory Decode Base Address (MBASE_DEV12) - R/W.** Specifies the 17-bit memory base address range (AD[31-15]) for the device 12 memory range. When this field is combined with MMASK_DEV12 field, a memory range is defined starting from the base address register value to the size defined by the mask register.
14-8	**Reserved.**

BIT	FUNCTION
7	**Device 12 Memory Monitor Enable (MEM_EN_DEV12) - R/W** 1: Enable PCI bus decode for accesses to the memory address range selected by the MBASE_DEV12 and MMASK_DEV12 fields. 0: Disable. The EIO enable bit or trap enable bit for device 12 must also be set in order to enable these respective functions.
6-0	**Device 12 Memory Decode Mask (MMASK_DEV12) - R/W.** Specifies the 7-bit memory base address mask used to determine the memory address range size for device 12 accesses. MMASK_DEV12 corresponds to AD[21-15]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1100001') results in a split range.

7.2.22. DEVRESG Device Resource G

Address Offset: 70-72h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
23-21	**Reserved.**
20	**Device 13 I/O Monitor Enable (IO_EN_DEV13) - R/W** 1: Enable PCI bus decode for accesses to the I/O address range selected by the IBASE_DEV13 and IMASK_DEV13 fields. 0: Disable. The EIO enable bit or trap enable bit for device 13 must also be set in order to enable these respective functions.
19-16	**Device 13 I/O Decode Mask (IMASK_DEV13) - R/W.** Specifies the 4-bit I/O base address mask used to determine the IO address range size for device 13 accesses. IMASK_DEV13 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.
15-0	**Device 13 I/O Decode Base Address (IBASE_DEV13) - R/W.** Specifies the 16-bit I/O base address range (AD[15-0]) for the device 13 I/O range. When this field is combined with IMASK_DEV13 field, an I/O range is defined starting from the base address register value to the size defined by the mask register.

7.2.23. DEVRESH Device Resource H

Address Offset: 74-77h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-15	**Device 13 Memory Decode Base Address (MBASE_DEV13) - R/W.** Specifies the 17-bit memory base address range (AD[31-15]) for the device 13 memory range. When this field is combined with MMASK_DEV13 field, a memory range is defined starting from the base address register value to the size defined by the mask register.
14-8	**Reserved.**
7	**Device 13 Memory Monitor Enable (MEM_EN_DEV13) - R/W** 1: Enable PCI bus decode for accesses to the memory address range selected by the MBASE_DEV13 and MMASK_DEV13 fields. 0: Disable. The EIO enable bit or trap enable bit for device 13 must also be set in order to enable these respective functions.
6-0	**Device 13 Memory Decode Mask (MMASK_DEV13) - R/W.** Specifies the 7-bit memory base address mask used to determine the memory address range size for device 13 accesses. MMASK_DEV13 corresponds to AD[21-15]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1100001') results in a split range.

7.2.24. DEVRESI Device Resource I

Address Offset: 78-7Bh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
23-21	**Reserved.**
20	**Generic I/O Decode 0 Enable (IO_EN_GDEC0) - R/W** 1: Enable accesses to the I/O address range selected by the IO_MASK_GDEC0 and IO_BASE_GDEC0 fields to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. 0: Disable.
19-16	**Generic Decode I/O Mask (IO_MASK_GDEC0) - R/W.** Specifies the 4-bit I/O base address mask used to determine the IO address range size. IO_MASK_GDEC0 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.

7.2.25. DEVRESJ Device Resource J

Address Offset: 7C-7Fh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
23-21	**Reserved.**
20	**Generic I/O Decode 1 Enable (IO_EN_GDEC1) - R/W** 1: Enable accesses to the I/O address range selected by the IO_MASK_GDEC1 and IO_BASE_GDEC1 fields to be claimed by the SLC90E46 and forwarded to the ISA/EIO bus. 0: Disable.
19-16	**Generic Decode I/O Mask (IO_MASK_GDEC1) - R/W.** Specifies the 4-bit I/O base address mask used to determine the IO address range size. IO_MASK_GDEC1 corresponds to AD[3-0]. A '1' in a bit position indicates that the corresponding address bit is masked (i.e. ignored) when performing the decode. Note that programming these bits to certain patterns (such as '1001') results in a split range.
15-0	**Generic Decode I/O Base Address (IO_BASE_GDEC1) - R/W.** Specifies the 16-bit I/O base address range (AD[15-0]) for the generic decode range 0. When this field is combined with IO_MASK_GDEC1 field, an I/O range is defined starting from the base address register value to the size defined by the mask register.

7.2.26. PMREGMISC Miscellaneous Power Management

Address Offset: 80h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-1	**Reserved.**
0	**Power Management IO Space Enable (PMIOSE) - R/W** 1: Enable. 0: Disable. This bit controls the access to the Power Management I/O space registers whose base address is described in the Power Management Base Address register. If this bit is set, access to the power management IO registers are enabled. When disabled, all IO accesses associated with Power Management Base Address are disabled. This bit functions independent of the state of Function 3 IO Space Enable (IOSE) bit (PCICMD register, bit 0).

7.3. SMBus Host Controller PCI Configuration Registers

7.3.1. SMBBA SMBus Base Address

Address offset: 90-93h
Value: 00000001h
Attribute: Read/Write

BIT	FUNCTION
31-16	**Reserved.** Hardwired to 0. Must be written as 0s.
15-4	**Index Register Base Address.** Bits [15-4] correspond to I/O address signals AD[15-4], respectively.
3-1	**Reserved.** Read as 0.
0	**Resource Type Indicator - Read Only.** This bit is hardwired to 1 indicating that the base address field in this register maps to I/O space.

7.3.2. SMBHSTCFG SMBus Host Configuration (Function 3)

Address Offset: D2h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-4	**Reserved.**
3-1	**SMBus Interrupt Select (SMB_INTRSEL)** Select the type of interrupt generated by the SMBus controller. 000: nSMI 001: Reserved. 010: Reserved. 011: Reserved 100: IRQ9 101: Reserved 11x: Reserved.
0	**SMBus Controller Host Interface Enable (SMB_HST_EN)** When set to 1, enables the SMBus Controller host interface. 0=Disable

7.3.3. SMBSLVC SMBus Slave Command (Function 3)

Address Offset: D3h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-0	**SMBus Host Slave Command (SMBCMD).** Specifies the command values to be matched for external SMBus master accesses to the SMBus controller host slave interface (SMBus port 10h).

7.3.4. SMBSHDW1 SMBus Slave Shadow Port 1 (Function 3)

Address Offset: D4h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-1	**SMBus Slave Address for shadow port 1 (SLVPORT1).** Specifies the address used to match against incoming SMBus addresses for shadow port 1.
0	**Read/Write for shadow port 1 (SLVPORT1RW).** This bit must be programmed to 0 since the SLC90E46 SMBus slave controller only responds to Word Write transactions.

7.3.5. SMBSHDW2 SMBus Slave Shadow Port 2 (Function 3)

Address Offset: D5h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-1	**SMBus Slave Address for shadow port 2 (SLVPORT2).** Specifies the address used to match against incoming SMBus addresses for shadow port 2.
0	**Read/Write for shadow port 2 (SLVPORT2RW).** This bit must be programmed to 0 since the SLC90E46 SMBus slave controller only responds to Word Write transactions.

7.3.6. SMBREV SMBus Revision Identification (Function 3)

Address Offset: D6h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
7-0	**Revision ID (REVID).** This register contains a hardwired current revision ID for the SMBus Host/Slave controller.

7.4. Power Management I/O Space Registers

The "Base" address is programmed in the SLC90E46 Configuration Space for Function 3, Offset 40h-43h.

7.4.1. PMSTS Power Management Status Register (IO)

I/O Address: Base + 00h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15	**Resume Status (RSM_STS) - R/Write Clear** 1: An enabled resume event has occurred. 0: No enabled resume event has occurred. The SLC90E46 sets this bit to 1 upon detection of the resume event and then transition the system to the ON state. This can only be set by hardware and can only be cleared by writing a one to this bit position.
14-12	**Reserved.**
11	**Power Button Override Status (PWRBTNOR_STS) - R/Write Clear** 1: Power Button Over-ride has been signaled. 0: Power Button Over-ride has not been signaled. This bit is set when Power Button Over-ride has been enabled and the nPWRBTN signal has been continuously asserted for greater than 4 seconds. The SLC90E46 will automatically transition the system into the soft off state and clear the PWRBTN_STS bit. This bit is only set by hardware and can only be reset by writing a '1' to this bit position.
10	**RTC Status (RTC_STS) - R/Write Clear** 1: RTC alarm has been signaled. 0: RTC alarm has not been signaled. This bit is set when the internal RTC asserts its IRQ8 signal. This bit is only set by hardware and can only be cleared by writing a '1' to this bit position.
9	**Reserved.**
8	**Power Button Status (PWRBTN_STS) - R/Write Clear** 1: nPWRBTN signal has been asserted. 0: nPWRBTN signal has not been asserted. There is a 16ms delay from external signal assertion to the setting of this bit due to internal switch debounce circuitry. This bit is only set by hardware and can only be reset by writing a one to this bit position. If the nPWRBTN signal is held LOW for more than 4 seconds, then this bit is cleared and the PWRBTNOR_STS bit is set.
7-6	**Reserved.**

BIT	FUNCTION
5	**Global Status (GBL_STS) - R/Write Clear** 1: SCI has been generated due a write of 1 to the BIOS_RLS bit. The GBL_EN bit of PMEN IO register must be set to enable the SCI generation. 0: No SCI has been generated due to write to BIOS_RLS bit. This bit is set by hardware and can only be reset by writing a one to this bit position.
4	**Bus Master Status (BM_STS) - R/Write Clear** 1: PCIREQ[0-3] or nPHOLD has been asserted (PCI bus master request). 0: No bus master request. This bit is set when PCIREQ[0-3] or nPHOLD is asserted and can only be cleared by writing a one to this bit position.
3-1	**Reserved**
0	**Timer Overflow Status (TMROF_STS) - R/Write Clear** 1: Bit 22 of the 24 bit Power Management timer has toggled. 0: Bit 22 of the Power management timer has not toggled. When the TMROF_EN is set then the setting of the TMROF_STS bit will automatically generate an SCI. This bit is only set by hardware and can only be reset by writing a one to this bit position.

7.4.2. PMEN Power Management Resume Enable Register (IO)

I/O Address: Base + 02h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15-11	**Reserved.**
10	**RTC Enable (RTC_EN) - R/W** 1: Enable the generation of a resume event upon setting of the RTC_STS bit. 0: Disable.
9	**Reserved.**
8	**Power Button Enable (PWRBTN_EN) - R/W** 1: Enable the generation of an nSMI **or SCI** upon setting of the PWRBTN_STS bit. 0: Disable. The nPWRBTN event is always enabled to generate resume event.
7-6	**Reserved.**
5	**Global Enable (GLB_EN) - R/W** 1: Enable the generation of a **SCI** upon setting of the GBL_STS bit. 0: Disable.
4-1	**Reserved.**
0	**Power Management Timer Overflow Enable (TMROF_EN) - R/W** 1: Enable **SCI** generation upon setting of the TMROF_STS bit. 0: Disable.

7.4.3. PMCNTRL Power Management Control Register (IO)

I/O Address: Base + 04h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15-14	**Reserved.**
13	**Suspend Enable (SUS_EN) - Write Only** This is a write only bit and reads to it always return a zero. Writing this bit to a 1 causes the system to automatically sequence into the suspend state defined by the SUS_TYP field.
12-10	**Suspend Type (SUS_TYP) - R/W** Specifies the type of hardware suspend mode the system should enter when the SUS_EN bit is set. This field is decoded as follows: 000: Soft or STD (Soft Off or Suspend to Disk) 001: STR (Suspend to RAM) 010: POSCL (Power On Suspend, Context Lost) 011: POSCCL (Power On Suspend, CPU Context Lost) 100: POS (Power On Suspend, Context Maintained) 101: Working (Clock Control) 110: Reserved 111: Reserved The SUS_TYP field may also be used by the BIOS and OS code to determine the type of suspend state the system is resuming from. Before entering any low power clock control state (LVL2 or LVL3), this field should be programmed to the Working state (101). This does not cause any action by the SLC90E46, but is for information storage only.
9	Reserved. nPWRBTN function is always enabled as required by the ACPI specification.
8-3	**Reserved**
2	**Global Release (GBL_RLS) - R/W** 1: A '1' written to this bit position will cause an nSMI to be generated and BIOS_STS bit set if enabled by the BIOS_EN bit. 0: No nSMI generated. This bit is used by ACPI software to raise an event to the BIOS software.
1	**Burst Timer Bus Master Reload Enable (BRLD_EN_BM) - R/W** 1: Enable the generation of a Burst Reload or Stop Break event upon setting of the BM_STS bit. 0: Disable.
0	**SCI Enable (SCI_EN) - R/W** 1: Enable generation of SCI upon assertion of the following bits: PWRBTN_STS, LID_STS, THRM_STS, GBL_STS, TMROF_STS or GPI_STS bit 0: Disable

7.4.4. PMTMR Power Management Timer Register (IO)

I/O Address: Base + 08h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
23-0	**Timer Value (TMR_VAL) - RO** This field returns the running count of the power management timer. This is a 24-bit counter that runs off a 3.579545MHz clock. The timer **is reset to an initial value of zero during a PCI reset**, and then continues counting unless the 14.31818 MHz OSC input to the chip is stopped. If the clock is restarted without a PCI reset, then the counter will continue counting from where it stopped. Any time bit 22 of the timer transitions from HIGH to LOW or LOW to HIGH, the TMROF_STS bit is set. If the PMTMR_EN (TMROF_EN) is set an SCI interrupt is also generated.

7.4.5. GPSTS General Purpose Status Register (IO)

I/O Address: Base + 0Ch
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15-12	**Reserved.**
11	**LID Status (LID_STS) - R/Write Clear** 1: LID signal has been asserted. 0: LID signal has not been asserted. Assertion level is dependent upon the value of the polarity selection bit LID_POL of GLBCTL IO register. If the LID_EN bit of GPEN IO register is set then the setting of the LID_STS bit will generate an SCI, nSMI or resume event. This bit is set by hardware and can only be reset by writing a '1' to this bit position.
10	**RING Status (RI_STS) - R/Write Clear** 1: Ring indicates nRI signal has been asserted. 0: nRI has not been asserted. If the RI_EN bit is set then the setting of the RI_STS bit will generate a resume event. This bit is only set by hardware and can only be reset by writing a one to this bit position.
9	**GPI Status (GPI_STS) - R/Write Clear** 1: nGPI1 signal has been asserted. 0: nGPI1 has not been asserted. If the GPI_EN bit is set then the setting of the GPI_STS bit will generate an nSMI, SCI or resume event. This bit is set by hardware and can only be reset by writing a one to this bit position.

BIT	FUNCTION
8	**USB Status (USB_STS) - R/Write Clear** 1: USB interface has indicated that a USB resume event has been driven onto one of thw two USB ports while in Power On Suspend. 0: No USB resume has been detected. If the USB_EN bit is set the setting of the USB_STS bit will generate a resume event. This bit is set by hardware and can only be reset by writing a one to this bit position.
7	**Thermal Override Status (THMOR_STS) - R/Write Clear** 1: nTHRM signal has been asserted LOW and thermal clock throttling has been initiated. 0: Thermal clock throttling has not been initiated. This bit is set anytime the thermal state machine generates a thermal over-ride condition and starts throttling the CPU's clock at the THRM_DTY ratio. This bit is set by hardware and can only be cleared by writing a one to this bit position.
6-1	**Reserved.**
0	**Thermal Status (THRM_STS) - R/Write Clear** 1: nTHRM signal has been asserted. 0: nTHRM signal has not been asserted. Assertion level is dependent upon polarity enable bit, THRM_POL of GLBCTL IO register. If the THRM_EN bit is set then the setting of the THRM_STS bit will generate an SCI or SMI. This bit is set by hardware and can only be reset by writing a one to this bit position.

7.4.6. GPEN General Purpose Enable Register (IO)

I/O Address: Base + 0Eh
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15-12	**Reserved.**
11	**LID Enable (LID_EN) - R/W** 1: Enable the generation of an nSMI, SCI or resume event upon the setting of the LID_STS bit. 0: Disable.
10	**RING Enable (RI_EN) - R/W** 1: Enable the generation of a resume event upon the setting of the RI_STS bit. 0: Disable.
9	**GPI Enable (GPI_EN) - R/W** 1: Enable the generation of an nSMI, SCI or resume event upon the setting of the GPI_STS bit. 0: Disable.
8	**USB Enable (USB_EN) - R/W** 1: Enable the generation of a resume event upon the setting of the USB_STS bit. 0: Disable.
7-1	**Reserved**

BIT	FUNCTION
0	**Thermal Enable (THRM_EN) - R/W** 1: Enable the generation of an nSMI or SCI upon the setting of the THRM_STS bit. 0: Disable.

7.4.7. PCNTRL Processor Control Register (IO)

I/O Address: Base + 10h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-18	**Reserved.**
17	**Clock Control Status (CC_STS) - Read Only** 1: SLC90E46 clock control active 0: Clock control inactive.
16-14	**Reserved.**
13	**Clock Run Enable (CLKRUN_EN) - R/W** 1: Enable PCI Clock Run (nCLKRUN) protocol. 0: Disable. When enabled, SLC90E46 will request to stop the PCI clock when the PCI bus has been idle for 26 PCI clocks.
12	**Stop Clock Enable (STPCLK_EN) - R/W** 1: Enable stopping of Host clock when placed into a LVL3 clock control condition. 0: Disable.
11	**Sleep Enable (SLEEP_EN) - R/W** 1: Enable assertion of nSLP signal when placed into a LVL3 clock control condition. 0: Disable. This enables Sleep or Deep Sleep clock control for Pentium Pro processor. This feature is not supported in the current revision of SLC90E46.
10	**Burst Enable (BST_EN) - R/W** 1: Enable clock control bursting which causes enabled system events to become Burst events and reload the burst timers. 0: Disable clock control bursting which causes enable system events to become Stop Break events and restore the system to normal full speed clocked operation.
9	**Clock Control Enable (CC_EN) - R/W** 1: Enable clock control. This enables reads to the LVL2 and LVL3 registers to cause SLC90E46 to enter the enabled clock mode. 0: Disable.
8-5	**Reserved.**
4	**Throttle Enable (THT_EN) - R/W** 1: Enable system throttle clock control. 0: Disable.

BIT	FUNCTION
3-1	**Throttle Duty Programming Bits (THT_DTY) - R/W** Selects the duty cycle of the nSTPCLK signal when the system is in the system throttling mode. The duty cycle indicates the percentage of time the nSTPCLK signal is asserted while in the throttle mode. The field is decoded as follows: 000: Reserved. 001: 12.5% 010: 25% 011: 37.5% 100: 50% 101: 62.5% 110: 75% 111: 87.5%
0	**Reserved.**

7.4.8. PLVL2 Processor Level 2 Register (IO)

I/O Address: Base + 14h
Default Value: 00h
Access: Byte Read Only

Reads to this register cause the SLC90E46 to transition into a Stop Grant or Quick Start power state (LVL2) and return a value of 00h. Writes to this register have no effect.

7.4.9. PLVL3 Processor Level 3 Register (IO)

I/O Address: Base + 15h
Default Value: 00h
Access: Byte Read Only

Reads to this register cause the SLC90E46 to transition into a Stop Clock, Sleep, or Deep Sleep power state (LVL3) and return a value of 00h. Writes to this register have no effect.

7.4.10. GLBSTS Global Status Register (IO)

I/O Address: Base + 18h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15-12	**Reserved.**
11	**IRQ Resume Status (IRQ_RSM_STS) - R/Write Clear** 1: System was resumed from a Powered On Suspend (POS) state due to an interrupt assertion (IRQ[1,3-15]). 0: System was not resumed due to IRQ.
10	**External SMI Status (EXTSMI_STS) - R/Write Clear** 1: nEXTSMI signal was asserted. 0: nEXTSMI was not asserted. 0: Disable. This bit is set by hardware and can only be reset by writing a one to this bit position.
9	**Reserved.**
8	**Global Standby Status (GSTBY_STS) - R/Write Clear** 1: Global Standby Timer expired (counted down to zero). 0: Global Standby Timer did not expire. This bit is set by hardware and can only be reset by writing a one to this bit position.

BIT	FUNCTION
7	**GP Status (GP_STS) - Read Only** 1: Indicates that one of the status bits in the GPSTS register is set. 0: All bits in GPSTS register are reset. This bit can only be reset by resetting all bits in the GPSTS register.
6	**PM1 Status (PM1_STS) - Read Only** 1: Indicates that one of the status bits in the PMSTS register is set. 0: All bits in PMSTS register are reset. This bit can only be reset by resetting all bits in the PMSTS register.
5	**APM Status (APM_STS) - R/Write Clear** 1: A write occurred to the APMC register (function 0) causing generation of an nSMI. 0: No write has occurred to the APMC register causing generation of an nSMI. This bit is cleared by writing a one to this bit position.
4	**All Device Status(DEV_STS) - Read Only** 1: Indicates that one of the status bits in the DEVSTS register is set. 0: All bits in DEVSTS register are reset. This bit can only be reset by resetting all bits in the DEVSTS register.
3	**Reserved**
2	**SLC90E46 Master Abort Status (MA_STS) - Read / Write Clear** 1: An nSMI was generated due to a SLC90E46 PCI cycle being Master Aborted. 0: No nSMI was generated due to SLC90E46 PCI cycle having been Master Aborted. This bit is set by hardware and only be reset by writing a one to this bit position.
1	**Legacy USB Status (LEGACY_USB_STS) - R/Write Clear** 1: USB legacy keyboard logic generated an nSMI. 0: USB legacy keyboard logic did not generate an nSMI. This bit is set by hardware and can only be cleared by writing a one to this bit position.
0	**BIOS Status (BIOS_STS) - R/Write Clear** 1: A write of 1 occurred to the GBL_RLS bit. 0: A write of 1 did not occur to the GBL_RLS bit. This bit is set by hardware and is cleared by writing a 1 to it.

7.4.11. DEVSTS Device Status Register (IO)

I/O Address: Base + 1Ch
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-30	**Reserved.**
29-16	**Device[13-0] Trap Status Bits (TRP_STS_DEV[13-0]) - R/Write Clear** 1: A nSMI was generated by an I/O trap to the associated device monitor's enabled address range. 0: No nSMI was generated due to an I/O trap of the associated device. Bit 29 corresponds to device monitor 13 and bit 16 corresponds to device monitor 0. This bit is cleared by writing a one to its bit position.
15-12	**Reserved.**
11-0	**Device [11-0] Idle Status Bits (IDL_STS_DEV[11-0]) - R/Write Clear** 1: A nSMI was generated by the expiration of the associated device monitor's idle timer. 0: No nSMI was generated. Bit 29 corresponds to device monitor 13 and bit 16 corresponds to device monitor 0. This bit is cleared by writing a one to its bit position.

7.4.12. GLBEN Global Enable Register (IO)

I/O Address: Base + 20h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
15	**Battery Low Enable (BATLOW_EN) - R/W** 1: Enable nBATLOW assertion to prevent a system resume from any suspend state. 0: Disable
14-12	**Reserved**
11	**IRQ Resume Enable (IRQ_RSM_EN) - R/W** 1: Enable an unmasked interrupt (IRQ[1,3-15]) assertion to generate a resume from the Power On Suspend state. 0: Disable
10	**External SMI Enable (EXTSMI_EN) - R/W** 1: Enable the setting of the EXTSMI_STS bit to generate an nSMI or resume event. 0: Disable
9	**Reserved**
8	**Global StandBy Enable (GSTBY_EN) - R/W** 1: Enable the setting of the GSTBY_STS bit to generate an nSMI or resume event. 0: Disable
7-5	**Reserved**
4	**SLC90E46 Master Abort Enable (MA_EN) - R/W** 1: Enable the setting of MA_STS bit to generate an nSMI. 0: Disable.

BIT	FUNCTION
3	**Bus Master Trap Enable (BM_TRP_EN) - R/W** 1: Enable the setting of BM_STS bit to generate an nSMI. 0: Disable
2	**Reserved.**
1	**BIOS Enable (BIOS_EN) - R/W** 1: Enable the generation of an nSMI by writing a 1 to the GBL_RLS bit. 0: Disable.
0	**Legacy USB Enable (LEGACY_USB_EN) - R/W** 1: Enable the USB legacy function to generate an nSMI. 0: Disable.

7.4.13. GLBCTL Global Control Register (IO)

I/O Address: Base + 28h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-27	**Reserved**
26	**Global Standby Timer clocking selection B (GSTBY_SELB) - R/W** This bit in conjunction with bit 8 selects the clock source for the Global Standby Timer.
25	**LID Polarity (LID_POL) - R/W** 1: Active low LID assertion will set the LID_STS bit. 0: Active high LID assertion will set the LID_STS bit.
24	**System Management Freeze (SM_FREEZE) - R/W** 1: Disable all Device Monitor Idle timers and the Global Standby timer from counting. 0: Enable timers to count.
23-17	**Reserved**
16	**End of SMI (EOS) - R/W** 1: Enable SLC90E46 to assert an nSMI. 0: Disable. This bit is cleared by hardware upon generation of an nSMI.
15-9	**Global Standy By Timer Initial Count (GSTBY_CNT) - R/W** Specifies the initial and reload count of the Global Standby Timer.
8	**Global Standby Timer Clocking Select A (GSTBY_SELA) - R/W** This bit in conjunction with bit 26 selects the clock source for the Global Standby Timer. **Bit 26 Bit 8 Clock Rate** 0 0 32 seconds 0 1 4 minutes 1 0 4 milliseconds 1 1 4 seconds
7-3	**Reserved**
2	**Thermal Polarity (THRM_POL) - R/W** 1: Active low nTHRM assertion will set the THRM_STS bit. 0: Active high nTHRM assertion will set the THRM_STS bit.

BIT	FUNCTION
1	**BIOS Release (BIOS_RLS) - R/W** 1: A 1 written to this bit position will cause an SCI to be generated and GBL_STS bit set if enabled by the GBL_EN bit. 0: No SCI generated.. This bit is used by the BIOS software to raise an event to the ACPI software. This bit always reads as a zero.
0	**SMI Enable (SMI_EN) - R/W** 1: Enable the generation of nSMI upon any enabled nSMI event. 0: Disable. This bit is reset by a PCI reset event.

7.4.14. DEVCTL Device Control Register (IO)

I/O Address: Base + 2Ch
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
31-28	**Reserved**
27	**Device 8 Bus Master Reload Enable (BM_RLD_DEV8) - R/W** 1: Enable any PCI Bus Master request (PCIREQ[3-0], nPHOLD) to reload the device monitor 8 idle timer . 0: Disable.
26	**Device 3 Idle Reload Enable (IDL_RLD_EN_DEV3) - R/W** 1: Enable the device monitor 3 idle timer events to reload the device monitor 3 idle timer. 0: Disable. When device 3 is being used as a software SMI timer, this bit should be cleared to prevent any events from reloading the timer.
25	**Device 13 Trap Enable (TRP_EN_DEV13) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 13 enabled trap decode ranges. 0: Disable.
24	**Device 12 Trap Enable (TRP_EN_DEV12)- R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 12 enabled trap decode ranges. 0: Disable.
23	**Device 11 Trap Enable (TRP_EN_DEV11) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 11 enabled trap decode ranges. 0: Disable.
22	**Device 11 Idle Reload Enable (IDL_EN_DEV11) - R/W** 1: Enable the device monitor 11 idle reload events to reload the device monitor 11 idle timer. 0: Disable.

BIT	FUNCTION
21	**Device 10 Trap Enable (TRP_EN_DEV10) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 10 enabled trap decode ranges. 0: Disable.
20	**Device 10 Idle Reload Enable (IDL_EN_DEV10) - R/W** 1: Enable the device monitor 10 idle reload events to reload the device monitor 10 idle timer. 0: Disable.
19	**Device 9 Trap Enable (TRP_EN_DEV9) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 9 enabled trap decode ranges. 0: Disable.
18	**Device 9 Idle Reload Enable (IDL_EN_DEV9) - R/W** 1: Enable the device monitor 9 idle reload events to reload the device monitor 9 idle timer. 0: Disable.
17	**Device 8 Trap Enable (TRP_EN_DEV8) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 8 enabled trap decode ranges. 0: Disable.
16	**Device 9 Idle Reload Enable (IDL_EN_DEV8) - R/W** 1: Enable the device monitor 8 idle reload events to reload the device monitor 8 idle timer. 0: Disable.
15	**Device 7 Trap Enable (TRP_EN_DEV7) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 7 enabled trap decode ranges. 0: Disable.
14	**Device 7 Idle Reload Enable (IDL_EN_DEV7) - R/W** 1: Enable the device monitor 7 idle reload events to reload the device monitor 7 idle timer. 0: Disable.
13	**Device 6 Trap Enable (TRP_EN_DEV6) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 6 enabled trap decode ranges. 0: Disable.
12	**Device 6 Idle Reload Enable (IDL_EN_DEV6) - R/W** 1: Enable the device monitor 6 idle reload events to reload the device monitor 6 idle timer. 0: Disable.
11	**Device 5 Trap Enable (TRP_EN_DEV5) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 5 enabled trap decode ranges. 0: Disable.
10	**Device 5 Idle Reload Enable (IDL_EN_DEV5) - R/W** 1: Enable the device monitor 5 idle reload events to reload the device monitor 5 idle timer. 0: Disable.
9	**Device 4 Trap Enable (TRP_EN_DEV4) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 4 enabled trap decode ranges. 0: Disable.

BIT	FUNCTION
8	**Device 4 Idle Reload Enable (IDL_EN_DEV4) - R/W** 1: Enable the device monitor 4 idle reload events to reload the device monitor 4 idle timer. 0: Disable.
7	**Device 3 Trap Enable (TRP_EN_DEV3) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 3 enabled trap decode ranges. 0: Disable.
6	**Device 3 Idle Reload Enable (IDL_EN_DEV3) - R/W** 1: Enable the device monitor 3 idle reload events to reload the device monitor 3 idle timer. 0: Disable.
5	**Device 2 Trap Enable (TRP_EN_DEV2) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 2 enabled trap decode ranges. 0: Disable.
4	**Device 2 Idle Reload Enable (IDL_EN_DEV2) - R/W** 1: Enable the device monitor 2 idle reload events to reload the device monitor 2 idle timer. 0: Disable.
3	**Device 1 Trap Enable (TRP_EN_DEV1) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 1 enabled trap decode ranges. 0: Disable.
2	**Device 1 Idle Reload Enable (IDL_EN_DEV1) - R/W** 1: Enable the device monitor 1 idle reload events to reload the device monitor 1 idle timer. 0: Disable.
1	**Device 0 Trap Enable (TRP_EN_DEV0) - R/W** 1: Enable generation of an I/O trap SMI for accesses to the device monitor 0 enabled trap decode ranges. 0: Disable.
0	**Device 0 Idle Reload Enable (IDL_EN_DEV0) - R/W** 1: Enable the device monitor 0 idle reload events to reload the device monitor 0 idle timer. 0: Disable.

7.4.15. GPIREG General Purpose Input Register (IO)

I/O Address: Base + 30h
Default Value: 00h
Access: Read Only (Byte Reads Only)

This register is used to store command values of external SMBus master accesses to the host slave and slave shadow ports.

BIT	FUNCTION
31-22	**Reserved**
21- 0	**General Purpose Input (GPI) - Read Only** Each bit directly represents the logical value on the pin. Some of the GPI signals can be configured as another input signal. The value in this register of a bit which is not configured as a GPI is indeterminate and may change randomly.

7.4.16. GPOREG General Purpose Output Register (IO)

I/O Address: Base + 34h
Default Value: 00h
Access: Read/Write (Byte Accesses Only)

BIT	FUNCTION
31	**Reserved**
30-0	**General Purpose Output (GPO) - R/W** Each bit directly represents the logical value output onto the pin. Reads to this register return the last value written. Some GPO signals can be configured as another output signal. In that case, the output pin will not reflect the state of the corresponding GPO bit in this register. Some of the output signals default to another signal.

7.5. SMBus IO Space Registers

The "Base" address is programmed in the SLC90E46 Configuration Space for Function 3, Offset 90h-93h.

7.5.1. SMBHSTSTS SMBus Host Status Register (IO)

I/O Address: Base + 00h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-5	**Reserved.**
4	**Failed (FAILED).** When it is 1 indicates that the source of SMBus interrupt was a failed bus transaction, set when KILL bit is set (SMBHSTCNT register). When it is 0, SMBus interrupt is not caused by KILL bit. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
3	**Bus Collision (BUS_ERR).** When it is 1 indicates that the source of SMBus interrupt was a transaction collision. When it is 0, SMBus interrupt was not caused by transaction collision. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
2	**Device Error (DEV_ERR)** When it is 1 indicates that the source of SMBus interrupt was the generation of an SMBus transaction error . When it is 0, SMBus interrupt was not caused transaction error. Transaction errors are caused by: Illegal Command Field Unclaimed Cycle (host initiated) Host device Time-Out This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
1	**SMBus Interrupt (INTER).** When it is 1 indicates that the source of SMBus interrupt was the completion of the last host command. When it is 0, SMBus interrupt was not caused by host command completion. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
0	**Host Busy (HOST_BUSY) - READ ONLY** When it is 1 indicates that the SMBus controller host interface is in the process of completing a command. When it is 0, SMBus controller host interface is not processing a command. None of the other registers should be accessed if this bit is set.

7.5.2. SMBSLVSTS SMBus Slave Status Register (IO)

I/O Address: Base + 01h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-6	**Reserved.**
5	**Alert Status (ALERT_STS).** When it is 1 indicates that the source of SMBus interrupt or resume event was the assertion of the nSMBALERT signal. When it is 0, SMBus interrupt was not caused by nSMBALERT signal. Setting of this bit requires that the ALERT_EN bit be set. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
4	**Shadow2 Status (SHDW2_STS).** When it is 1 indicates that the source of SMBus interrupt or resume event was a slave cycle address match of the SMBSHDW2 port. When it is 0, SMBus interrupt was not caused by address match to SMBSHDW2 port. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
3	**Shadow1 Status (SHDW1_STS).** When it is 1 indicates that the source of SMBus interrupt or resume event was a slave cycle address match of the SMBSHDW1 port. When it is 0, SMBus interrupt was not caused by address match to SMBSHDW1 port. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
2	**Slave Status (SLV_STS).** When it is 1 indicates that the source of SMBus interrupt or resume event was a slave cycle event match of the SMBSLVC (command match) and SMBSLVEVT (data event match). When it is 0, SMBus interrupt was not caused by slave event match. This bit is only set by hardware and can only be reset by writing a 1 to this bit position.
1	**Reserved.**
0	**Slave Busy (SLV_BSY) - READ ONLY** When it is 1 indicates that the SMBus controller slave interface is in the process of receiving data. When it is 0, SMBus controller slave interface is not processing data. None of the other registers should be accessed if this bit is set.

7.5.3. SMBHSTCNT SMBus Host Control Register (IO)

I/O Address: Base + 02h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7	**Reserved.**
6	**Start (START).** Writing a 1 to this bit initiates the SMBus controller host interface to execute the command programmed in the SMB_CMD _PROT field. All necessary registers should be setup before writing a 1 to this bit. Writing a 0 has no effect. This bit always reads zero. The HOST_BUSY bit can be used to identify when the SMBus host controller has finished executing the command.
5	**Reserved**
4-2	**SMBus Command Protocol (SMB_CMD_PROT)** This field selects the type of command the SMBus controller host interface will execute. Reads or writes are determined by bit 0 of SMBHSTADD register. 000 Quick Read or Write 001 Byte Read or Write 010 Byte Data Read or Write 011 Word Data Read or Write 100 Reserved 101 Block Read or Write 110/111 Reserved
1	**Kill (KILL)** Writing a 1 to this bit stops the current in process SMBus controller host transaction. This sets the FAILED status bit of SMBHSTSTS register and asserts the interrupt selected by the SMB_INTRSEL field. When it is 0 it allows the SMBus controller host interface to function normally.
0	**Interrupt Enable (INTEREN)** When it is 1 it enables the generation of interrupts upon the completion of the current host transaction. Setting to 0 will disable the interrupt generation.

7.5.4. SMBHSTCMD SMBus Host Command Register (IO)

I/O Address: Base + 03h
Default Value: 00h
Access: Read/Write

This register is transmitted by the SMBus controller host interface in the command field of the SMBus protocol.

BIT	FUNCTION
7-0	**SMBus Host Command (HST_CMD)** This field contains the data transmitted in the command field of SMBus host transaction.

7.5.5. SMBHSTADD SMBus Host Address Register (IO)

I/O Address: Base + 04h
Default Value: 00h
Access: Read/Write

This register is transmitted by the SMBus controller host interface in the slave address field of the SMBus protocol.

BIT	FUNCTION
7-1	**SMBus Address (SMB_ADDRESS)** This field contains the 7-bit address of the targeted slave device.
0	**SMBus Read or Write (SMB_RW)** 1=A Read Command. 0=A Write Command.

7.5.6. SMBHSTDAT0 SMBus Host Data 0 Register (IO)

I/O Address: Base + 05h
Default Value: 00h
Access: Read/Write

This register is transmitted by the SMBus controller host interface in the Data0 field of the SMBus protocol.

BIT	FUNCTION
7-0	**SMBus Data 0 (SMBD0)** This register should be programmed with the value to be transmitted in the Data0 field of an SMBus host interface transaction. For a block write command, the count of the memory block should be stored in this field. The value of this register is loaded into the block transfer count field. This register must be programmed to a value between 1 and 32 for block command counts. A count of 0 or a count above 32 will result in unpredictable behavior. For block reads, the count received from the SMBus device is stored here.

7.5.7. SMBHSTDAT1 SMBus Host Data 1 Register (IO)

I/O Address: Base + 06h
Default Value: 00h
Access: Read/Write

This register is transmitted by the SMBus controller host interface in the Data1 field of the SMBus protocol.

BIT	FUNCTION
7-0	**SMBus Data 1 (SMBD1)** This register should be programmed with the value to be transmitted in the Data1 field of an SMBus host interface transaction.

7.5.8. SMBHSTDAT SMBus Block Data Register (IO)

I/O Address: Base + 07h
Default Value: 00h
Access: Read/Write

Reads and writes to this register are used to access the 32-byte block data array. An internal index pointer is used to address the array. It is reset to 0 by reading the SMBHSTCNT register. The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

BIT	FUNCTION
7-0	**SMBus Block Data (BLK_DAT)** This register is used to transfer data into or out of the block data storage array.

7.5.9. SMBSLVCNT SMBus Slave Control Register (IO)

I/O Address: Base + 08h
Default Value: 00h
Access: Read/Write

The control register is used to enable SMBus controller slave interface functions.

BIT	FUNCTION
7:4	**Reserved.**
3	**SMBus Alert Enable (ALERT_EN)** 1: Enable the assertion of nSMBALERT signal to generate an interrupt or resume event. 0: Disable.
2	**SMBus Shadow Port 2 Enable (SHDW2_EN)** 1: Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBSHDW2 register. 0: Disable.
1	**SMBus Shadow Port 1 Enable (SHDW1_EN)** 1: Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBSHDW1 register. 0: Disable.
0	**Slave Enable (SLV_EN)** 1=Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the host controller slave port of 10h, a command field which matches the SMBSLVC register, and a match of one of the corresponding enabled events in the SMBSLVENT register. 0: Disable.

7.5.10. SMBSHDWCMD SMBus Shadow Command Register (IO)

I/O Address: Base + 09h
Default Value: 00h
Access: Read Only

This register is used to store command values of external SMBus master accesses to the host slave and slave shadow ports.

BIT	FUNCTION
7-0	**Shadow Command (SHDW_CMD)** This register contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

7.5.11. SMBSLVEVT SMBus Slave Event Register (IO)

I/O Address: Base + 0Ah
Default Value: 0000h
Access: Read/Write

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

BIT	FUNCTION
15-0	**SM Bus Slave Event (SMB_SLV_EVT)** This field contains data bits used to compare against incoming data to the SMBSLVDAT register. When a bit in this register is a 1 and the corresponding bit in the SMBSLVDAT register is set, then an interrupt or resume event will be generated if the command value matches the value in the SMBSLVC register and the access was to SMBus host address 10h.

7.5.12. SMBSLVEVT SMBus Slave Data Register (IO)

I/O Address: Base + 0Ch
Default Value: 00h
Access: Read Only

This register is used to store data values of external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

BIT	FUNCTION
15-0	**Slave Data (SMB_SLV_DATA)** This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

8. PCI/ISA BRIDGE FUNCTIONAL DESCRIPTION

This section describes the major functions of the SLC90E46 PCI-to-ISA bridge.

8.1. Memory and IO Address Map

The SLC90E46 interfaces to two system buses: PCI and ISA buses. The SLC90E46 normally acts as a subtractive decoding agent, it also provides positive decode for certain I/O and memory space accesses on the PCI bus. ISA masters and DMA devices can access PCI memory and some of the internal SLC90E46 registers. ISA masters and DMA devices, however, do not have accesses to host or PCI I/O space.

8.1.1. I/O Accesses

The SLC90E46 positively decodes accesses to all internal registers, including PCI configuration registers (PCI only), ISA compatible IO registers (PCI and ISA), and all relocatable IO space registers (IDE, USB, Power Management).

Accesses to the ISA/EIO bus can be configured to be either subtractive decode or positive decode. The SLC90E46 provides a wide variety of positive decode ranges for standard devices as well as a number of programmable ranges for additional devices. In addition, the SLC90E46 also provides positive decode for BIOS, X-Bus, and system event decode for power management support.

8.1.2. Memory Access

PCI Memory Access

When subtractive decoding is enabled, PCI accesses to memory below 16Mbyte (including BIOS space) that are not claimed by a PCI device are forwarded to the ISA bus. When subtractive decoding is disabled, the SLC90E46 only forwards cycles for programmable ranges (32K-4M size) associated with power management devices 12 and 13 and for BIOS ranges.

For write accesses that are not claimed by an ISA slave, the cycle completes normally (6 SYSCLKS for 8 bit cycles). For read accesses that are not claimed by the ISA slave, the SLC90E46 returns data corresponding to the state of the ISA bus and completes the cycle normally (6 SYSCLKS for 8 bit cycles).

The SLC90E46 also forwards any accesses to an enabled I/O-APIC address range.

ISA/DMA Memory Access

For ISA or DMA accesses to main memory, all accesses to memory locations 0-512Kbytes, 512-640KB if enabled, above 1M and below the Top of Memory are forwarded to the PCI bus. All remaining ISA originated memory accesses are confined to the ISA bus.

Memory Address Range of A DMA/ISA Master Cycle	Action
(Top of Memory) to 128 Mbyte	Confine to ISA
1Mbyte to (Top of Memory)	Forward to PCI.
(1Mbyte - 128Kbyte) to (1Mbyte -64Kbyte)	Forward to PCI if bit6/XBCS=0 and bit3/TOM=1.
640Kbyte to (1Mbyte - 128Kbyte)	Confine to ISA
512Kbyte to 640Kbyte	Forward to PCI if bit1/TOM=0
0-512Kbyte	Forward to PCI

8.1.3. BIOS Memory Space

The SLC90E46 supports 1 Mbytes of BIOS memory space. That includes the normal 128 Kbytes space, plus an additional 384 Kbytes (extended BIOS space) and 512 Kbytes of BIOS space (1M extended BIOS area). The XBCS register provides the BIOS space access control.

PCI Access to BIOS Memory Space

The normal 128 Kbytes BIOS space is located at 0E0000 - 0FFFFFh and is aliased at FFFE0000h (top of 4 Gbytes). This 128 Kbytes block is split into two 64 Kbytes blocks. PCI Accesses to the top 64 Kbytes (0F0000 - 0FFFFFh) and its aliased region (FFFF0000-FFFFFFFFh) are always forwarded to the ISA Bus and nBIOSCS is always generated. Accesses to the bottom 64 Kbytes (0E0000h - 0EFFFFh) and its aliased region (FFFE0000 - FFFEFFFFh) are forwarded to the ISA bus and nBIOSCS is generated when this BIOS range is enabled (bit 6 of XBCS is set to 1).

The Extended BIOS space is located at FFF80000 - FFFDFFFFh. When this region is enabled (bit 7 of the XBCS register is set to 1), PCI accesses are forwarded to ISA and nBIOSCS is asserted.

The 1M Extended BIOS space is located at FFF00000 - FFF7FFFFh. When this region is enabled (bit 9 of the XBCS register is set to 1), PCI accesses are forwarded to ISA and nBIOSCS is asserted.

Write Protection

The nBIOSCS can be disabled from assertion during BIOS memory write accesses to the decoded BIOS region by setting bit 2 of XBCS to a 0. When the bit is 1, nBIOSCS is asserted for both memory read and memory write accesses to the decoded BIOS region.

Positive Decode

The SLC90E46 always positively decodes PCI accesses to the enabled BIOS memory regardless of the status of the Positive / Subtractive Decode Configuration bit (bit 1 of PCI configuration register at B0h, Function 0).

PCI Accesses to BIOS Memory Spaces

BIOS Memory Space	Aliased Address Space	Configuration Register	Action
000F0000-000FFFFFh	FFFF0000 - FFFFFFFFh	NO	Forward to ISA, nBIOSCS always generated. For FFFF0000 - FFFFFFFFh, it is converted into FF0000 - FFFFFFh in ISA memory space.
000E0000-000EFFFFh	FFFE0000-FFFEFFFFh	Bit 6/XBCS	When set to 1, forwarded to ISA and nBIOSCS generated. When set to 0, not forwarded to ISA. For FFFE0000 - FFFEFFFFh, it is converted into FE0000 - FEFFFFh in ISA memory space.
FFF80000-FFFDFFFFh		Bit 7/XBCS	When set to 1, forwarded to ISA and nBIOSCS generated. When set to 0, not forwarded to ISA. For FFF80000 - FFFDFFFFh, it is converted into F80000 - FDFFFFh in ISA memory space.
FFF00000-FFF7FFFFh		Bit 9/XBCS	When set to 1, forwarded to ISA and nBIOSCS generated. When set to 0, not forwarded to ISA. For FFF00000 - FFF7FFFFh, it is converted into F00000 - F7FFFFh in ISA memory space.

ISA Access to BIOS Memory Space

All ISA-initiated BIOS accesses to the top 64 Kbytes (0F0000 - 0FFFFFh) BIOS region are confined to the ISA bus and nBIOSCS is asserted, even when BIOS is shadowed in main memory. When the bottom 64 Kbytes (0E0000 - 0EFFFFh) BIOS region is enabled, ISA-initiated BIOS accesses are confined to the ISA bus and nBIOSCS asserted. When the BIOS region is disabled, accesses are forwarded to PCI bus and nBIOSCS negated.

BIOS MEMORY SPACE	ALIASED ADDRESS SPACE	CONTROL BIT	ACTION
000F0000-000FFFFFh	FFFF0000-FFFFFFFFh (not applied)	NO	Confined to ISA, even if BIOS is shadowed. nBIOSCS generated.
000E0000-000EFFFFh	FFFE0000-FFFEFFFFh (not applied)	Bit6/XBCS	When set to 1, confined to ISA. nBIOSCS generated. When set to 0, forwarded to PCI bus.
FFF80000-FFFDFFFF			Not Applied.
FFF00000-FFF7FFFF			Not Applied.

8.2. PCI Interface

The SLC90E46 contains a complete PCI Bus Master and Slave interface. As a PCI master, the SLC90E46 runs cycles on behalf of ISA masters, DMA devices, bus master IDE, or USB host controller. When it is a slave, the SLC90E46 accepts cycles initiated by PCI masters targeted for the SLC90E46's internal register set or the ISA bus.

PCI Transaction Termination

As a master, the SLC90E46 supports the following forms of master initiated termination:

- Normal termination of a completed transaction.
- Normal termination of an incomplete transaction due to time out.
- Abnormal termination due to the slave not responding to the transaction (abort).

As a master, the SLC90E46 responds correctly to the following target initiated termination:

- Target-Abort.
- Retry.
- Disconnect.

As a target, the SLC90E46 supports the following types of target initiated termination:

- Target-Abort
- Retry
- Disconnect

PCI Bus Arbitration

The SLC90E46 uses the signal pair: nPHOLD and nPHLDA to request the use of PCI bus on behalf of ISA masters and DMA devices. ISA devices asserts DREQ to gain access to the ISA bus. When type-F DMA is not enabled, the SLC90E46 will assert nPHOLD to the SLC90E42. The nDACK signal will be asserted after nPHLDA is asserted. The ISA devices can then start to transfer data on the ISA bus. When type-F DMA is enabled and a DREQ is asserted, the SLC90E46 will assert DACK signal right after the ISA bridge is idle. The SLC90E46 will assert nPHOLD to the SLC90E42 when the DMA buffer is full (data is transferred to system memory) or when the DMA buffer is empty (data is retrieved from system memory).

PCI Parity

As a master, the SLC90E46 generates address parity for read/write cycles and data parity during write cycle. As a slave, the SLC90E46 generates data parity for read cycles. The SLC90E46 does not check parity and does not generate nSERR due to an address parity error. The SLC90E46 does generate an NMI when another PCI device asserts nSERR (if enabled).

8.3. ISA/EIO Interface

The SLC90E46 supports either full ISA Bus compatible master and slave interface or a subset interface called the Extended IO (EIO) bus. The SLC90E46 can drive five ISA slots without external data buffers. The ISA and EIO interfaces also provide byte swap logic, IO recovery support, wait state generation, and SYSCLK generation.

ISA Interface

The ISA interface, when enabled, supports the following types of cycles:

- PCI master initiated I/O and memory cycles to the ISA bus
- DMA compatible cycles between main memory and ISA I/O and between ISA I/O and ISA memory.
- Type-F DMA cycles between PCI memory and ISA I/O.
- ISA refresh cycles initiated by either the SLC90E46 or an external ISA master.
- ISA master initiated memory cycles to PCI and ISA master-initiated I/O cycles to the internal SLC90E46 registers (DMA, Timer, 60h/61h/70h/72h/B2h/B3h, Interrupt, 4D0h/4D1h, CF9h, 0F0h)

EIO Interface

The EIO Interface Differs from ISA Interface in the following ways:

- ISA Master cycles are not supported.
- Only 20-bit addressing allowed
- ISA refresh is not supported.

8.4. DMA Controller

The SLC90E46 includes two 8237 DMA controllers with seven programmable channels. DMA channels 0-3 are supported by DMA controller 1 (DMA-1). DMA channels 5-7 are supported by DMA controller 2 (DMA-2). DMA channel 4 is used to cascade the two controllers and is put in cascade mode in the DMA Channel Mode Register. The DMA controller can also responds to requests that are initiated by software. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

Channels 0-3 are hardwired to 8-bit, count-by-byte transfers, and channels 5-7 are hardwired to 16 bit, count-by-word transfers. Both ISA compatible and Type-F DMA timing are supported. The SLC90E46 supports 24 bit DMA addressing. Each channel includes a 16 bit Current Address Register and an 8 bit ISA compatible Page register which contains the most significant eight bits of address.

The DMA controller is at any time in either master mode or slave mode. In master mode, the DMA controller is either servicing a DMA slave's request for DMA cycles, or allowing a 16-bit ISA master to use the bus. In slave mode, the SLC90E46 monitors the ISA and PCI bus, and responds to I/O read and write commands that address its registers.

In DMA transfer cycles, the I/O device is always on the ISA bus, the memory device can be located on either ISA bus or on PCI bus. The SLC90E46 will drive the nMEMR or nMEMW signals if the address is less than 16 Mbytes, regardless of whether the cycle is decoded for PCI or ISA memory. The nSMEMR and nSMEMW will be generated if the address is less than 1 Mbytes. The SLC90E46 will not assert nMEMR or nMEMW when address is greater than 16 Mbytes.

During DMA cycles, both AEN and BALE signals are driven high.

8.4.1. DMA Transfer Modes

The DMA controller supports four transfer modes, including single, block, demand, or cascade.

Single Transfer Mode

In single transfer mode, the DMA makes one transfer only. The byte/word count will be decremented and the address decremented/incremented following each transfer. When the count "rolls over" from zero to 0FFFFh, a Terminal Count (TC) will cause an auto-initialize if the channel has been programmed to do so.

DREQ must be held active until nDACK becomes active in order to be recognized. The bus will be released after a single transfer. If DREQ remains high, the DMA I/O device will re-arbitrate for the bus. Another single transfer can be performed once the bus is granted.

Block Transfer Mode

In block transfer mode, the DMA is activated by DREQ, and it continues making transfers until a TC, caused by counter going to FFFFh, is encountered. DREQ only need be held active until nDACK becomes active. Autoinitialization can be programmed to occur at the end of service.

In block transfer mode, it is possible to lock out other service for a period of time if the transfer count is a large number.

Demand Transfer Mode

In demand transfer mode, the DMA continues making transfers until a TC, caused by counter going to FFFFh, is encountered or until the DMA I/O device releases DREQ. Transfers may continue until the I/O device has exhausted its data buffer. The DMA service can be re-established when the DMA I/O device reasserts DREQ. During the time between services the system is allowed to operate. A TC can cause an autoinitialization at the end of the service, if enabled.

Cascade Mode

In cascade mode, the DMA controller will only respond to DREQ with DACK without driving other address and command signals.

ISA bus master devices (16 bit) also use cascade mode to directly access system memory. The ISA master asserts DREQ to request for the bus. If it wins the bus arbitration, the SLC90E46 responds with an ISA master acknowledge nDACK signal asserted. While an ISA master owns the ISA bus, BALE is driven high while AEN is driven low. The ISA master can control the ISA bus until it negates the DREQ line.

8.4.2. DMA Transfer Types

The DMA controller supports three transfer types, including Write, Read and Verify, for each of the three active transfer modes (Single, Block or Demand).

Write Transfers

Write transfers move data from ISA device to memory located on the ISA bus or in system memory. The SLC90E46 activates ISA memory control signals as soon as the DMA memory address is available. In compatible DMA timing mode, the PCI transfer is initiated after the data is valid on the ISA bus. When the DMA buffer mode is enabled, the PCI transfer is initiated when the 16-byte buffer is full or the DMA transfer is completed. When the memory is located on the ISA bus, a PCI cycle is not initiated.

Read Transfers

Read transfers move data from ISA memory or the system memory to ISA I/O. The SLC90E46 activates nIOW command and the appropriate ISA memory and system memory control signals to indicate a memory read. The PCI transfer is initiated as soon as the DMA address is valid when the cycle involves system memory. When the DMA buffer mode is enabled, the PCI transfer is initiated when the DMA transfer first starts or the 16-byte buffer becomes empty. When the memory is located on the ISA bus, a PCI cycle is not initiated.

Verify Transfers

During verify transfers, the DMA controller generates addresses as in normal read/write transfers. However, no ISA memory or I/O control lines will be activated. The SLC90E46 asserts the nDACK signal for nine SYSCLKs. If verify transfer are repeated during Block or Demand mode operation, each additional verify transfer adds 8 SYSCLKs. The nDACK lines will not be toggled for repeated transfers.

8.4.3. DMA Timing

The SLC90E46 supports two types of timing: ISA compatible timing and Type-F timing. The repetition rate for ISA compatible DMA cycles is 8 SYSCLKs. The Type-F cycles can occur back to back at a minimum rate of 3 SYSCLKs. Type-F DMA is supported for each of the seven DMA channels. The Type-F timing can be enabled through register 65h.

Bit 7 of register 65h can be used to turn on a 16-byte post-write/prefetch buffer on the SLC90E46.

8.4.4. DMA Buffer

The SLC90E46 integrates a 16-byte data buffer to improve ISA master or DMA devices data transfer efficiency.

When the buffer is enabled, the SLC90E46 asserts nDACK signal in response to DMA device' or ISA master's request when there is no pending ISA cycle. The PHOLD signal is only asserted when data transfer on the PCI bus is demanded. The PHOLD signal is negated after the 16-byte buffer is filled with prefetched memory data (in Read Transfer mode) or when the post-write data are moved from the buffer to the system memory (in Write Transfer mode). The de-assertion of PHOLD allows the processor or other PCI master devices to use the PCI bus while the DMA device or the ISA master transfers data to/from the buffer. During the DMA or ISA master transaction period, the SLC90E46 will initiate Retry cycle in response to any ISA-bounded PCI cycle until the DMA / ISA master cycle completes.

When the buffer is enabled and a DMA device is requesting for data from the system memory, the SLC90E46 is acting as a PCI bus master to prefetch 16-byte of data from the system memory. PCI bus is then relinquished, data is transferred directly from the buffer to the DMA device until the buffer is empty or the DMA transfer is completed. In a write transfer, data is first collected in the 16-byte buffer. When the buffer is full or when the DMA device drops the DREQ, the SLC90E46 then acts as a PCI bus master to burst transfer the 16-byte data to the system memory.

The 16-byte DMA buffer greatly improves the available PCI bus bandwidth even with the slow DMA or ISA master devices, and makes the Type-F DMA transactions feasible.

8.4.5. DMA Channel Priority

The DMA consists of two channel groups: channels 3-0 and channels 7-4. Each group may be programmed to work in either fixed or rotating mode through the DMA Command Register. Note that a software DMA request is subject to the same prioritization as any hardware request.

For Fixed Priority, the priority ordering is 0, 1, 2, 3, 5, 6 and 7, with channel 0 has the highest priority and channel 7 has the lowest priority.

For Rotating Priority, the priority chain rotates so that the last channel serviced is assigned the lowest priority in each channel group: (0-3, 5-7).

In Rotating Priority, channels 5 - 7 rotate as part of a group of 4. That is, channels 5 -7 form the first three positions in the rotation, while the whole group (0-3) is the forth position in the arbitration. Channels 0-3 rotate as a group of 4. They are always placed between Channel 5 and Channel 7 in the priority list.

8.4.6. DMA Transfer Sizes

The following table lists each of the two DMA transfer sizes.

DMA Data Size and Word Count	Unit of Current Byte/ Word Count Register	Current address Increment/Decrement
8 bit I/O, Count by Bytes	Bytes	1
16 bit I/O, Count by Words (Address Shifted)	Words	1

8.4.7. Address Shifting in 16-Bit DMA I/O Transfer

The following table shows how the address is shifting during 16 bit DMA I/O transfer.

Output Memory Address	8 Bit I/O Mode (CH 0-3)	16 Bit I/O Mode (CH 5-7)
A0	A0	0
A[16-1]	A[16-1]	A[15-0]
A[23-17]	A[23-17]	A[23-17]

Note that the least significant bit of the Low Page Register is dropped in 16-bit mode. When programming the Current Address Register for DMA channels which are in this mode, the Current Address must be programmed to an even address with the address value shifted right by one bit.

8.4.8. Autoinitialization

When a channel is set up as an autoinitialization channel (via Channel Mode Register), the autoinitialization (invoked by a TC) will restore the original values of the Current Address, Current Page, Current Byte/Word Count Registers from the Base Address, Page and Byte/Word Count registers of that channel automatically. Following autoinitialization, the channel is ready to perform another DMA service as soon as a valid DREQ is detected.

8.4.9. Special DMA Commands

Clear Byte Pointer Flip-Flop

This command initializes the flip-flop to a known state so that subsequent accesses to the registers, address or count register, will address upper and lower bytes in a known sequence. The command is normally executed prior to writing or reading new address or word count information to or from the controller. I/O port 0Ch is used for channels 0-3 and 0D8h is for channels 4-7.

DMA Master Clear

This command has the same effect as the hardware reset. The Command, Status, Request and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The DMA controller will enter the idle cycle. I/O port 0Dh is used for channels 0-3 and 0DAh is for channels 4-7.

Clear Mask Register

This command clears the mask bits of a DMA controller (four channels), enabling them to accept DMA requests. I/O port 0Eh is used for channels 0-3 and 0DCh is for channels 4-7.

8.4.10. ISA Refresh

The ISA refresh requests can be generated by two sources: the SLC90E46 or ISA bus master other than the SLC90E46. In both cases, the SLC90E46 will generate the ISA memory refresh. The SLC90E46 will drive the SA[7-0] so that when nMEMR becomes active, the entire ISA memory is refreshed at one time. ISA memory devices should not drive any data onto the data bus during the refresh cycle.

SLC90E46 Initiated ISA Refresh Cycle

Counter 1 is programmed to provide ISA refresh request for every 15us. The SLC90E46 asserts nREFRESH to indicate a refresh cycle. It then drives the SA[7-0] and generates nMEMR and nSMEMR. Both AEN and BALE are driven high for the entire refresh cycle. The memory device may pull the IOCHRDY low to extend the refresh cycle.

System DRAM refreshes are controlled by the north bridge (SLC90E42), and are completely decoupled from ISA memory refresh.

ISA Master Initiated Refresh Cycle

If an ISA master holds the ISA bus longer than 15usec, the ISA master must initiate memory refresh cycles. When an ISA master initiates a refresh cycle, it floats the address and control signals and asserts the nREFRESH signal to the SLC90E46. The SLC90E46 drives the SA[7-0] and generates nMEMR onto the ISA bus. BALE is driven high and AEN is driven low for the entire refresh cycle.

8.5. PCI DMA

The SLC90E46 supports Distributed DMA as the PCI DMA protocol. The Distributed DMA is based on monitoring CPU accesses to the 8237 DMA controller. If the accesses are associated with DMA channels that are “distributed” into some PCI peripherals, then the SLC90E46 collects or distributed the data from or to the PCI peripherals before letting the CPU complete its accesses. The Distributed DMA protocol allows legacy software to function as if it is accessing a standard 8237-based system, even though the registers are not located in the SLC90E46.

A 16-bit configuration register, located at offset 90h of Function 0 configuration space, is used to configure the 7 DMA channels. Each DMA channel can be independently configured to be either a standard DMA channel or a Distributed DMA channel.

8.5.1. Distributed DMA (DDMA)

The Distributed DMA scheme is based on a concept that the registers associated with individual DMA channel can physically reside on other PCI devices, outside of the SLC90E46. The Distributed DMA logic in the SLC90E46 is used only when the CPU accesses to the 8237 registers. It's the responsibility of the PCI peripherals to do the data movement.

The SLC90E46 contains two registers to indicate the I/O locations for the relocated DMA registers. The first register indicates the offset of the register associated with DMA channels 0-3. The second indicates the offset of the register associated with DMA channels 5-7. BIOS or other configuration software has to program the DDMA peripherals to the corresponding locations.

DDMA Read Cycles Protocol

The SLC90E46 responds to PCI read cycles that correspond to distributed DMA channels in the following ways:

- The SLC90E46 will respond with a PCI retry to terminate the PCI cycle.
- Immediately, the SLC90E46 will request the PCI bus. Upon being granted the bus, the SLC90E46 will perform one or more read cycles to the 8237 and/or the PCI peripherals. The I/O location of the read cycle is calculated based on the following parameters: (1) the DDMA Base Pointer registers in the PCI configuration space, (2) the DMA channel number, and (3) the register location (0h-Fh).
- The SLC90E46 will use the data obtained from the read cycles (along with the values from the 8237) to construct the proper data value.
- The SLC90E46 releases the PCI bus.
- When CPU retries the PCI read cycles, the SLC90E46 will respond with the proper data value.

DDMA Write Cycles Protocol

The SLC90E46 responds to PCI read cycles that correspond to distributed DMA channels in the following ways:

- The SLC90E46 will latch the data and respond with a PCI retry to terminate the PCI cycle.
- Immediately, the SLC90E46 will request the PCI bus. Upon being granted the bus, the SLC90E46 will perform one or more write cycles to the 8237 and/or the PCI peripherals. The I/O location of the write cycle is calculated based on the following parameters: (1) the DDMA Base Pointer registers in the PCI configuration space, (2) the DMA channel number, and (3) the register location (0h-Fh).
- The SLC90E46 will use the data obtained from the CPU's original write cycles to determine the proper values to write to the peripherals and to the 8237.
- The SLC90E46 releases the PCI bus.
- When CPU retries the PCI read cycles, the SLC90E46 will terminate the cycle normally.

I/O Address Calculation

When the SLC90E46 attempts to access the PCI peripherals, it has to first get the exact I/O address for performing I/O read or write cycles. This section shows how the I/O address is constructed.

Bits 31-16 0.

Bits 15-6

The Base Pointer in the PCI configuration space for function 0 indicates the value for this field. The Base Pointer at offset 92h is for channels 0-3. The Base Pointer at offset 94h is for DMA channels 5-7.

Bits 5-4

This field is determined by the DMA channel number being accessed.

DMA Channel Number	Bits[5-4]
0	00
1 or 5	01
2 or 6	10
3 or 7	11

Bits 3-0

This field is determined by the register being accessed.

The following table shows the mapping of the 8237 registers to the Distributed DMA peripherals.

I/O ADDRESS	8237 F/F STATUS	R/W	REGISTER NAME	"DISTRIBUTED" CYCLE I/O ADDRESS
0, 2, 4, 6h, C4, C8, CCh	0	W	Base Address Register A0-A7	Base Pointer + Channel # + 0h
0, 2, 4, 6h, C4, C8, CCh	0	R	Current Address Register A0-A7	Base Pointer + Channel # + 0h
0, 2, 4, 6h, C4, C8, CCh	1	W	Base Address Register A8-A15	Base Pointer + Channel # + 1h
0, 2, 4, 6h, C4, C8, CCh	1	R	Current Address Register A8-A15	Base Pointer + Channel # + 1h
87, 83, 81, 82, 8B, 89, 8Ah	x	R/W	Page Register	Base Pointer + Channel # + 2h
1, 3, 5, 7h, C6, CA, CEh	0	W	Base Word Count Register D0-D7	Base Pointer + Channel # + 4h
1, 3, 5, 7h, C6, CA, CEh	0	R	Current Word Count Register D0-D7	Base Pointer + Channel # + 4h
1, 3, 5, 7h, C6, CA, CEh	1	W	Base Word Count Register D8-D15	Base Pointer + Channel # + 5h

I/O ADDRESS	8237 F/F STATUS	R/W	REGISTER NAME	"DISTRIBUTED" CYCLE I/O ADDRESS
1, 3, 5, 7h, C6, CA, CEh	1	R	Current Word Count Register D8-D15	Base Pointer + Channel # + 5h
08h, D0h	X	W	Command Register	Base Pointer + Channel # + 8h
08h, D0h	X	R	Status Register	Base Pointer + Channel # + 8h
09h, D2h	X	W	Request Register	Base Pointer + Channel # + 9h
0Bh, D6h	X	W	Mode Register	Base Pointer + Channel # + Bh
0Dh, DAh	X	W	Master Clear	Base Pointer + Channel # + Dh
0Fh, DEh	X	W	Write All Masks Register	Base Pointer + Channel # + Fh
Ah, D4h	X	W	Single Channel Mask	See Note 1 below
Eh, DCh	X	W	Clear Mask Register	See Note 2 below

Note 1: Single Channel Mask Register

The Distributed DMA specification doesn't have the peripherals implement the Single Channel Mask Registers. Instead, a write to the Single Channel Mask register will cause write the Write All Masks Register. The Distributed DMA peripheral uses bit 0 in the Write All Masks Register for that particular channel.

When a write occurs to the Single Channel Mask registers, the SLC90E46 will examine the low two data bits to determine the DMA channel number. The SLC90E46 will generate a write to the peripheral device at (Base Pointer + Channel # + Fh). The data value of bit 0 for that write cycle will be determined by data bit 2 of the original CPU write.

Note 2: Clear Mask Register

The Distributed DMA specification doesn't have the peripherals implement the Clear Mask Command. Instead, a write to the Clear Mask Command register will cause writes to all the distributed channels associated with that 8237.

When a write occurs to the Clear Mask Command register, the SLC90E46 will perform up to 4 writes to the Write All Masks register (Base Pointer + Channel # + Fh) with a data value of 0h.

8.6. Interrupt Controller

The SLC90E46 integrates an ISA compatible interrupt controller which incorporates the functionality of two 8259 interrupt controllers. The two interrupt controllers are cascaded. The master controller provides IRQ[7-0] and the slave controller provides IRQ[15-8]. There are three interrupts used for internal functions only. IRQ0 is used as a system timer interrupt and is tied to interval Timer 1, Counter 0. IRQ0 is available to the user only if an external IO APIC is enabled. IRQ2 is used to cascade the two controllers together and is not available to the user. IRQ13 is connected internally to nFERR. There are 13 interrupt lines (IRQ1, IRQ3-IRQ12, IRQ14, IRQ15) available for external uses. Edge or level trigger mode can be programmed independently for each channel. Note that when bit 4 of the XBCS register is set to 1, the IRQ12/M is generated internally as part of a the mouse support. When it is set to 0, standard IRQ12 function is provided and IRQ12 appears externally.

The two 8259 cores are initialized separately and can be programmed to operate in different modes. The default settings are 80x86 Mode, Edge Sensitive Detection, Normal EOI, Non-Buffered Mode, Special Fully Nested Mode disabled, and Cascade Mode. Controller 1 is configured as the Master Interrupt Controller and controller 2 is connected as the Slave Interrupt Controller.

8.6.1. Programming the Interrupt Controller

The interrupt controller accepts two types of command words generated by the CPU or bus master.

Initialization Command Words (ICWs)

The interrupt controller must be initialized before normal operation can begin. The SLC90E46 interrupt controllers require four byte sequence to configure the controller correctly. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

An I/O write to the Controller 1 or Controller 2 base address, which is 20h and A0h respectively, with data bit 4 equal to 1 is interpreted as ICW1. To complete the initialization, the SLC90E46 requires three I/O writes to "base address +1", which is 21h for Controller 1 and A1h for Controller 2, to follow the ICW1. The first write performs ICW2, the second one performs ICW3 and the third write performs ICW4.

Following is a brief description about the four commands:

ICW1 starts the initialization sequence for the controller.

ICW2 is to provide bits[7-3] of the interrupt vector that will be released onto the data bus during an interrupt acknowledge cycle. A different base [7-3] is selected for each interrupt controller.

ICW3 has different meaning for two controllers:

1. For Controller 1, the master controller, ICW3 is used to indicate which IRQx input line is used to cascade the slave controller. In the SLC90E46 implementation, IRQ2 of the master controller is used to cascade the INTR output of the slave controller. Therefore, bit 2 of ICW3 on Controller 1 is set to 1, and the other bits are all set to 0's.

2. For Controller 2, ICW3 is the slave identification code used during an interrupt acknowledge cycle. Controller 1 broadcasts a code to Controller 2 over three internal cascade lines if an IRQ[x] line of Controller 2 won the priority arbitration on the master controller and was granted an interrupt acknowledge by the CPU. If this identification code is equal to bits[2-0] of ICW3, Controller 2 will broadcast the interrupt vector during the second interrupt acknowledge cycle.

ICW4 must be programmed on both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an 80x86 based system.

Operation Command Words (OCWs)

These are the command words which dynamically reprogram the interrupt controllers to operate in various interrupt modes. The OCWs can be written into the Interrupt Controller any time after initialization. Following is a brief description of these command words.

OCW1 can be used to mask interrupt lines. By writing a 1 in any bit of this command word will mask incoming interrupt requests on the corresponding IRQx line.

OCW2 is used to control the rotation of interrupt channel priorities when operating in the rotating priority mode. It can also control the End of Interrupt (EOI) function of the controller.

OCW3 is used to set up reads of the ISR and IRR, to enable or disable the Special Mask Mode, and to set up the interrupt controller in Poll Command Mode.

8.6.2. End of Interrupt Operation

The In Service (IS) bit can be set to 0 automatically following the trailing edge of the second nINTA pulse when the Automatic EOI mode is enabled or by a command word that must be issued to the interrupt controller before returning from a service routine (EOI command). An EOI command must be issued twice, once for the master and once for the slave.

There are two forms of EOI commands: Specific and Non-Specific. When the Interrupt Controller is operated in fully nested modes, it can determine which IS bit to set to 0 on EOI. When a Non-Specific EOI command is issued, the interrupt controller will automatically set to 0 the highest IS bit of those that are set to 1, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, and R=0).

When a mode is used which may disturb the fully nested structure, the interrupt controller may no longer be able to determine the last level acknowledged. In this case, a Specific End Of Interrupt must be issued which states the IS level to be reset. A Specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 specifies the IS bit to be reset to 0 in binary format).

An IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the Interrupt Controller is in the Specific Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI is 1 in ICW4, then the interrupt controller will operate in AEOI mode continuously until reprogrammed by ICW4. To reprogram ICW4 requires that ICW1, ICW2 and ICW3 must be reprogrammed first. In AEOI mode, the interrupt controller will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. This mode should be used only when a nested multi-level interrupt structure is not required within a single interrupt controller. Consequently, the AEOI mode can only be used in the master interrupt controller (controller 1) and not a slave controller (controller 2).

8.6.3. Modes of Operation

Fully Nested Mode

This is the default operating mode after initialization unless another mode is programmed. The interrupt request are ordered in priority from 0 through 7, with 0 being the highest priority. Priority can be changed when rotating priority mode is selected.

When an interrupt is acknowledged by the CPU, the highest priority request is determined and its vector is placed on the bus. Additionally, a bit of the Interrupt Service Register (IS[0-7]) is set, and it remains set until the CPU issues an EOI command immediately before returning from the interrupt service routine. Or, if the AEOI bit is set, this IS bit remains set until the trailing edge of the second nINTA pulse. While the IS bit is set, all further interrupts of the same or lower priority are inhibited. Interrupt requests with higher priority level will generate an interrupt, but it will be acknowledged only if the CPU internal interrupt enable control has been re-enabled by the software.

Special Fully Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. The master controller is programmed to be in the Special Fully Nested Mode using ICW4. This mode is similar to the normal nested mode with the following exceptions:

When an interrupt request from a certain slave is in service, this slave is not locked out form the master's priority logic and further interrupt requests from higher priority IRQs within the slave will be recognized by the master and will initiate interrupt to the CPU. While in the normal nested mode, a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.

When exiting the interrupt service routine, the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific EOI command to the slave and then reading its In-Service Register and checking for zero. If no bit is set, a non-specific EOI can be sent to the master too. If it is not zero, no EOI should be sent.

Automatic Rotation Mode (Equal Priority Devices)

Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt will have to wait until each of seven other devices are serviced once.

There are two ways to accomplish automatic rotation using OCW2: the Rotation on Non-Specific EOI command (R=1, SL=0, and EOI=1) and the Rotation in Automatic EOI Mode which is set by (R=1, SL=0, and EOI=0) and cleared by (R=0, SL=0, and EOI=0).

Specific Rotation Mode (Specific Priority Devices)

The programmer can change priorities by selecting the bottom priority and thus fixing all other priorities. For example, if IRQ6 is programmed as the bottom priority device, then IRQ7 will be the highest priority device.

The Set Priority Command is issued in OCW2 with R=1, SL=1 and L0-L2 is the binary code of the bottom priority device.

Note that, in this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 with R=1, SL=1, EOI=1, and L0-L2 is the binary code of the IRQ channel to receive bottom priority.

Polled Mode

In the Polled mode, the INTR output is not used and the CPU internal interrupt Enable control is reset, disabling its interrupt input. Services to devices is achieved by software using a Poll Command.

The Poll Command is issued by setting P=1 in OCW3. The interrupt controller treats the next I/O read pulse to the interrupt controller as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupts are frozen from the I/O write to the I/O read.

The Polled Mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command.

The Polled Mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table.

This mode is useful if there is a routine command common to several levels so that the nINTA sequence is not needed.

8.6.4. Cascade Mode

The SLC90E46's interrupt controllers are interconnected in a cascade mode with one master and one slave. Totally, there are 15 separate priority levels (IRQs). The master controls the slaves through a three line internal cascade bus. When the master drives 010b on the internal cascade bus, this bus acts like a chip select to the slave controller.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and then acknowledged, the master will enable the corresponding slave to release the interrupt vector address during the second nINTA cycle of the interrupt acknowledge sequence.

Each interrupt controller in the cascaded system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice, one for the master and another one for the slave.

8.6.5. Edge and Level Triggered Mode

In ISA compatible systems the triggered mode is selected using bit 3 in ICW1. The SLC90E46 adds two new registers, ELCR1 and ELCR2, for edge and level triggered mode selection for the two controllers. The default programming is equivalent to programming the LTIM bit (bit 3 of ICW1) to a 0 (edge triggered mode for all interrupts). Note that IRQ0, 1, 2, 8 and 13 can not be programmed for level sensitive mode and can not be modified by software.

When an ELCR bit is set to 0, an interrupt request will be recognized by a low to high transition on the corresponding IRQx input. The IRQ input can remain high without generating another interrupt.

When an ELCR bit is set to 1, an interrupt request will be recognized by a low level on the corresponding IRQ input. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In either triggered mode, the IRQ inputs must remain active until after the falling edge of the first nINTA. If the IRQ input goes inactive before this time, a default "IRQ7" will occur when the CPU acknowledges the interrupt. To implement this feature, the IRQ7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IRQ7 is needed for other purposes, a default IRQ7 can still be detected by reading the ISR. A normal IRQ7 interrupt will set the corresponding ISR bit, while a default IRQ7 will not set this bit. If a default IRQ7 routine occurs during a normal IRQ7 routine, the ISR will remain set. In this case, it is necessary to keep track of whether or not the IRQ7 routine was previously entered. If another IRQ7 occurs, it is a default.

8.6.6. Interrupt Masks

Masking on an Individual Interrupt Request Basis

Each interrupt request input can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel, when it is set to 1. Masking an IRQ channel does not affect other channel's operation, with one exception. Masking IRQ2 on Controller 1 will mask off all requests for service from Controller 2 because the Controller 2's INTR output is directly connected to the Controller 1's IRQ2 input.

Special Mask Mode (SMM)

The Special Mask Mode enables all interrupts not masked by a bit set in the Mask Register. Interrupt Service Routines that require dynamic alteration of interrupt priorities can take advantage of the Special Mask Mode. For example, a service routine can inhibit lower priorities request during a part of the interrupt service routine, then enable some of them during another part.

In the Special Mask mode, if a mask bit is set to 1 in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels that are not masked. Therefore, any interrupts may be selectively enabled by loading the Mask Register with an appropriate pattern. Without Special Mask Mode, the interrupt controller inhibits all lower priority requests until an EOI is issuing to clear the IS bit. The SMM provides an easy way for the service routine to selectively enable only the interrupts needed by loading the Mask register.

The SMM is set by OCW3 with SSMM=1, and SMM=1. The SMM can be cleared by OCW3 with SSMM=1, and SMM=0.

8.6.7. Interrupt Controller Status

The Interrupt Request Register (IRR) and In-Service Register (ISR) can be read via OCW3. The Interrupt Mask Register (IMR) is read through a read of OCW1.

IRR

This is an 8-bit register which contains the status of each interrupt request line. Bits that are clear indicate interrupts that have not requested service. The interrupt controller clears the IRR's highest priority bit during an interrupt acknowledge cycle.

Prior to reading IRR, a Read Register Command must be issued with OCW3 (RR=1, RIS=0).

ISR

This is an 8 bit register indicating the priority levels currently receiving service. Bits that are cleared indicate interrupt request lines that have not been asserted, or interrupt requests that have not been acknowledged. Bits that are set indicate interrupts that have been acknowledged and their service routine started. At any time only the highest priority interrupt service routine executes, since the lower priority interrupt services are suspended while higher priority interrupts are serviced. The ISR is updated when an EOI command is issued.

Prior to reading ISR, a Read Register Command must be issued with OCW3 (RR=1, RIS=1)

IMR

An 8 bit register indicating which interrupt request lines are masked. OCW1 is used for reading the IMR.

The interrupt controller retains the ISR/IRR status read selection following each write to OCW3. Therefore, there is no need to write an OCW3 before every status read operation, as long as the current status read corresponds to the previously selected register. After initialization the interrupt controller is set to read the IRR.

8.6.8. Interrupt Steering

The SLC90E46 allows four PCI interrupts (nPIRQA - nPIRQD) to be internally routed to one of 11 interrupts: 3-7, 9-12, 14 or 15. The nPIRQx lines are run through an internal multiplexer that routes an individual nPIRQx line to any one of 11 IRQ inputs. PCLK is used to synchronize the nPIRQx inputs. The assignment is programmable through the nPIRQx Route Control Registers. One or more nPIRQx lines can be routed to the same IRQx input.

The nPIRQx lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line. The software must change an IRQ to level sensitive mode if a nPIRQx is routed to that IRQ line. The selected IRQ can no longer be used by an ISA device, even that ISA device can respond as an active low level sensitive interrupt.

8.7. Serial Interrupts (SIRQ)

The SLC90E46 supports a serial Interrupt scheme, that allows a single signal to be used to report ISA-style interrupt requests. Serial Interrupt scheme is typically used in a mobile system.

Since more than one device may need to share the single IRQ signal, an Open Collector signaling scheme is used. Serial Interrupt scheme is based on the PCI clock. If the PCI clock is inactive when a device needs to signal an interrupt, the nCLKRUN signal must first be asserted by the device to restart the PCI clock.

8.7.1. SIRQ Protocol

Serial interrupt information is transferred using three types of frames: a Start Frame, one or more IRQ data frames, and one Stop frame. There are two modes of operation: Quiet Mode and Continuous Mode.

Quiet (Active) Mode

The peripheral brings the SERIRQ signal active for one clock, and then tri-state it to indicate an interrupt. This brings all the state machines to the active state.

The SLC90E46 will then take control of the SERIRQ signal by driving it low on the next clock, and will continue driving it low for 3-7 more clocks, which makes the total number of clocks low from 4 to 8. After those clocks, the SLC90E46 will drive SERIRQ high for one clock and then tri-state the signal.

Continuous (Idle) Mode

Continuous mode is the default mode after reset, and can be used to enter the Quiet mode. In this mode, the SLC90E46 initiates the START frame, rather than the peripherals. Typically, this will be done to update IRQ status (acknowledges). The SLC90E46 will drive SERIRQ low for 4 to 8 clocks.

Data Frame

Once the Start frame has been initialized, all of the serial interrupt peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each: a Sample phase, a Recovery phase, and a Turn-around phase.

During the Sample phase, the device drives SERIRQ low if the corresponding interrupt signal should be active. If the corresponding interrupt is inactive, then the device should not drive the SERIRQ signal line. The external pull-up resistor will keep the signal high to indicate an inactive IRQ request.

During the other two phases (Turn Around and Recovery), no device should drive the SERIRQ signal line.

The following table shows the supported IRQ signals and the specific ordering of these signals in the SIRQ protocol.

DATA FRAME NUMBER	USAGE	# CLOCKS PAST START
1	UNASSIGNED	2
2	IRQ1	5
3	nSMI	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	UNASSIGNED	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	UNASSIGNED	41
15	IRQ14	44
16	IRQ15	47
17	nIOCHCK	50
18	nPCI INTA	53
19	nPCI INTB	56
20	nPCI INTC	59
21	nPCI INTD	62
32:22	UNASSIGNED	96

If an nSMI is active on frame 3, the SLC90E46 will drive its nEXTSMI signal active, which will then cause an nSMI to the CPU if enabled.

Stop Frame

After all of the data frames, a Stop Frame will be done by the SLC90E46. This is done by pulling SERIRQ low for 2-3 clocks. The number of clocks determines the next working mode:

If Stop Frame is 2 clocks, then the next mode is the Quiet mode. Any device may initiate a Start Frame in the second clock (or more) after the rising edge of the Stop Frame.

If the Stop Frame is 3 clocks, then the next mode is the Continuous mode. Only the SLC90E46 may initiate a Start Frame in the second clock (or more) after the rising edge of the Stop Frame.

8.8. Timer / Counters

The SLC90E46 integrates an 8254 equivalent programmable interval timer, which contains three counters. Each counter output provides a key system function. Counter 0 is internally connected to IRQ0 and provides a system timer interrupt event for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal to refresh ISA memory device. Counter 2 generates the tone for the speaker. The counters normally use the 14.31818 MHz OSC as a clock source.

8.8.1. Counter 0

This counter functions as the system timer by generating IRQ0 periodically and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period, which is 838ns, and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

8.8.2. Counter 1

This counter provides the refresh request signal and is typically programmed for Mode 2 operation. The counter negates refresh request for one counter period, which is 838ns, during each count cycle. The initial count value is loaded one counter period after software writes the count value to the counter I/O address. The counter initially asserts refresh request and negates it for 1 counter period when the count value reaches 1. The counter then asserts refresh request, reload the initial count value and continue counting down the initial count value.

8.8.3. Counter 2

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a frequency equal to the counter clock frequency, which is 1.193MHz, divided by the initial count value. The speaker output must be enabled by a write to port 061h.

8.8.4. The Interval Timer Programming Interface

The timer uses a single Control Word Register to control the operation of all three counters. The Control Word Register is write-only. The Control Word Command specifies:

- Which counter to read or write
- The operating mode
- The count format: binary or BCD

The Read/Write logic selects the Control Word Register during an I/O write when address lines A[1-0]=11b. This condition occurs during an I/O Write to address 043h. When the CPU writes to port 43h, the data is stored in the Control Word Register and is interpreted as the Control Word used to define the operation of the Counters.

The interval timer is an I/O mapped device. Several commands are available:

The Counter Latch Command latches the current count so that it can be read by the system. The countdown process is not affected by the latch command.

The ReadBack Command reads the count value, programming mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

After power up, the timer counters stay in an unknown state. It is recommended to program the timer counter immediately after power up.

Write Operations

To write (program) the interval timer is very straight forward: First write a control word, then write an initial count for each counter by loading the least and/or most significant bytes (as required by Control Word bits 5, 4) of the 16-bit counter.

The control word must be written before the initial count is written. And the initial count must follow the count format specified in the control word: least significant byte only, most significant byte only, or least significant byte first and then most significant byte.

Since the Control Word Register and the three counters have separate addresses (selected by the A1 and A0 address lines) and each control word specifies the counter it applies to (SC0 and SC1 bits), no special instruction sequence is required. A new initial count may be written to a counter at any time without affecting the counter's operating mode. The new count must follow the programmed count format.

When a counter is programmed to read or write two-byte counts, the program must not transfer the control between accessing the first and second byte to another routine which may also access that same counter.

Control Word Format

The control word specifies the counter, the operating mode, the order and size of the count value, and whether it counts down in a 16-bit or BCD format. After the control word is programmed, a new count can be written at any time. The new value will take effect according to the programming mode.

Read Operations

There are three possible ways for reading the counters: a simple read operation, the Counter Latch Command and the ReadBack Command.

1. Counter I/O Port Read (Simple Read)

To read the counter, the CLK input of the selected counter must be inhibited by using either GATE input or external logic. Otherwise, the count may be in the process of changing while it is read, giving an undefined result. Within the timer unit, the GATE inputs of Counter 0 and Counter 1 are tied high. Therefore, Simple Read should not be used on these two counters. The GATE input of Counter 2 is controlled by I/O port 061h. When Counter 2 GATE input is disabled through this register, I/O reads of port 042h will return correct count value.

2. Counter Latch Command

This command latches the count at the time the command is received. It ensures that the count read from the counter is accurate. The count value can be read from each counter's Count Register as was programmed by the Control Register.

When the Counter Latch Command is received, the selected counter's output latch (OL) latches the count. This count is held in the latch until it is read by the CPU or till the counter is reprogrammed. The count is then unlatched automatically and the output latch returns to follow the counting element (CE). This mode allows reading the contents of the counters "on the fly" without affecting counting in progress.

The Counter Latch Command does not affect the programmed mode of the counter, and it can be used for each of the three counters.

A Counter Latch Command is only honored by the Counter if the output latch contents of the previous latch command is read. For example, if a Counter is latched and then, some time later, latched again before the count in the output latch is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Latch Command was issued.

The SLC90E46 timer allows reads and writes of the same counter may be interleaved. For example, if the Counter is programmed for two byte counts, the following programming sequence is still valid:

(1) Read least significant byte
(2) Write new least significant byte
(3) Read most significant byte
(4) Write new most significant byte

Read Back Command

The Read Back command is used to determine the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. When the Read Back command is written to the Control Word Register, the current states of the above mentioned variables are latched. They can be read by I/O access to the counter address.

The Read Back Command allows to latch multiple counters at one time. When bit 5 of the Command word is a 0 and multiple counters are selected through bit 1 to bit 3 of the Command word, the single Read Back Command is functionally equivalent to several Counter Latch Commands, one for each counter latched. Like the Counter Latch Command, each counter's latched count is held until it is read or until the counter is reprogrammed. Once read, the counter is unlatched. The other counters remain latched until they are read. If multiple Read Back Commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back Command can also be used to latch status information of selected counters by setting bit 4 of the Command word to a 0. Status has to latch to be read. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored. The status returned from the read is the counter status at the time the first status Read Back Command was issued.

It is also possible to latch both count and status of the selected counters simultaneously by setting both bit 5 and bit 4 of the Command word to 0 (bits[5-4]=00b). It is functionally the same as issuing two consecutive, separate Read Back Commands.

If both count and status of a counter are latched, the first read operation from that counter will return the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, return the latched count. Subsequent reads return unlatched count.

8.9. Real Time Clock Module

The SLC90E46 contains a Motorola MC146818A-compatible real-time clock module with 256 bytes static RAM as a date-and-time keeping device with alarm features and battery backed-up operation. The RTC counts seconds, minutes, hours, days, day of the week, date, month, and year. Leap year compensation is provided.

Three interrupt features are provided by the RTC module: time of day alarm with once a second to once of a month range, periodic rates of 122μs to 500ms, and end of update cycle notification.

The RTC module contains 256 bytes of battery backed RAM. The memory is divided into two banks, namely, the standard bank and the extended bank, each with 128 bytes. The standard bank contains 10 bytes indicating time and date information, 4 bytes used as Control Registers (A, B, C, D), and 114 bytes used as general purpose RAM. The extended bank has the whole 128 bytes as general purpose RAM.

The RTC also supports two lockable memory ranges. By turning on bits in the configuration register, two 8-byte space can be locked to read and write accesses, which prevents unauthorized reading of passwords or other security information.

Time, calendar, and alarm can be represented in either binary or BCD format, determined by bit 2 of Control Register B. The hour is represented either in 12 or 24 hour format, selected by bit 1 of Control Register B. When changing the format, the programmer has to reinitialize the time registers to the new data format.

The RTC module is operated on a 32.768Khz crystal and a separate 3V lithium battery that provides up to 7 years of protection. The clock signal is internally divided down to 1 Hz signal, one of the 15 taps from the divider chain can be selected as a periodic interrupt.

8.9.1. RTC Registers and RAM

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A-D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and is accessible even when the RTC module is disabled (through the RTC configuration register).

All data movement between the CPU and the RTC is done through registers mapped to the ISA IO space at locations 70-73h:

IO locations 70h and 71h are the standard ISA locations for the RTC. The following table shows the address map for this bank. IO locations 72h and 73h are for accessing the extended RAM, and may be disabled.

INDEX ADDRESS	NAME
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Date of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh-7Fh	114 bytes of user RAM

Note: Both banks are accessed through an indexed scheme: ISA IO addresses 70h/72h are the address pointers for the standard bank/extended bank respectively. ISA IO addresses 71h/73h are the data registers for the standard bank/extended bank respectively.

The programmer has to make sure that data stored in these locations is within the reasonable values and represents a possible date and time. The only exception is to store a value of C0h - FFh in the alarm bytes to indicate a “don’t care” situation. The software has to make sure that bit 7 of Control Register A must be read as 0 to avoid the RTC update process before access to these locations, bit 7 of Control Register B has to set to a 1 before program these locations to avoid clashes with the RTC update cycle.

The internal RTC registers can only be accessed by PCI masters. ISA master access is not supported.

8.9.2. Register A

Address Offset: 0Ah
Default Value: NA, this register is not affected by any system reset signal.
Access: Read/Write

This is a general configuration register.

BIT	FUNCTION
7	**Update In Progress (UIP):** When set to 1, the update is soon to occur or is in progress. If 0, the update cycle will not start for at least 244us. The time, calendar, and alarm information in RAM is always available when the bit is 0. This bit may be monitored as a status flag.
6-4	**Division Chain Select (DVx):** There three bits control the divider chain for the oscillator. 000: Osc disabled. 001: Osc disabled. 010: Normal function. 011: Test mode. 10x: Test mode. 11x: Divider reset
3-0	**Rate Select Bits (RSx):** Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in register B. Otherwise, this tap will set the PF flag of register C. If the periodic interrupt is not to be used, these bits should all be set to zero.

RS3	RS2	RS1	RS0	FREQUENCY OF INTERRUPT	PERIODIC RATE
0	0	0	0	0.0	none
0	0	0	1	256 Hz	3.90625 ms
0	0	1	0	128 Hz	7.8125 ms
0	0	1	1	8.192 kHz	122.070 us
0	1	0	0	4.096 kHz	244.141 us
0	1	0	1	2.048 kHz	488.281 us
0	1	1	0	1.024 kHz	976.5625 us
0	1	1	1	512 Hz	1.953125 ms
1	0	0	0	256 Hz	3.90625 ms
1	0	0	1	128 Hz	7.8125 ms
1	0	1	0	64 Hz	15.625 ms
1	0	1	1	32 Hz	31.25 ms
1	1	0	0	16 Hz	62.5 ms
1	1	0	1	8 Hz	125 ms
1	1	1	0	4 Hz	250 ms
1	1	1	1	2 Hz	500 ms

8.9.3. Register B

Address Offset: 0Bh
Default Value: X0000XXXb.
Access: Read/Write

This is a general configuration register.

BIT	FUNCTION
7	**SET: Enable the update cycles.** When it is zero, update cycle occurs normally once a second. If set to 1, a current update cycle will abort and subsequent update cycles will not occur until SET is reset to zero. When set to 1, the BIOS can initialize time and calendar bytes safely. This bit is not affected by the nRSMRST (Reset signal asserted during resume from suspension).
6	**Periodic Interrupt Enable (PIE).** When set to 1, the Periodic Interrupt Enable allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared (set to zero) on active nRSMRST.
5	**Alarm Interrupt Enable (AIE).** If set to one, the Alarm Interrupt Enable (AIE) bit allows an interrupt to occur when the AF is one as set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared on active nRSMRST.
4	**Update-ended Interrupt Enable (UIE).** If set to one, this bit allows an interrupt to occur when the update cycle ends. This bit is cleared on active nRSMRST.
3	**Square Wave Enable (SQWE).** The bit serves no function in this device, yet is left in the register to provide compatibility with the Motorola 146818B. There is no SQW output pin assigned on the SLC90E46. This bit is cleared on active nRSMRST.
2	**Data Mode (DM).** When set to 1 selects binary as data representation format. When set to 0 selects BCD as data representation format. This bit is not affected by nRSMRST.
1	**Hour Mode (HF).** When set to 1, 24 hour mode is used. If it is 0, 12 hour mode is selected. In 12 hour mode, bit 7 of the hour register represents AM as zero and PM as one. This bit is not affected by nRSMRST.
0	**Daylight Savings Enable (DSE).** The daylight savings enable bit is read only and is always set to a 0 to indicate that the daylight savings time option is not available.

8.9.4. Register C

Address Offset: 0Ch
Default Value: 00h
Access: Read/Write

This register is used for various flags. All bits are cleared upon active nRSMRST or a read of register C.

BIT	FUNCTION
7	**Interrupt Request Flag (IRQF).** IRQF = PF*PIE + AF*AIE + UF*UFE. This also causes the CH_IRQ_8 signal to be asserted..
6	**Periodic Interrupt Flag (PIF).** This flag is one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero.
5	**Alarm Flag (AF).** This bit is high after all Alarm Values match the current time.
4	**Update-ended Flag (UF).** This bit is high immediately following an update cycle for each second.
3-0	Reserved.

8.9.5. Register D

Address Offset: 0Dh
Default Value: NA - this register is not affected by any system reset signal.
Access: Read/Write

This register is used for various flags

BIT	FUNCTION
7	**Valid RAM and Time Bit (VRT).** This bit is set to 1 when the PWRGD (power good) signal is high. This bit is not typically used. This bit should always set to 0 for write to this register.
6	**Reserved.**
5-0	**Date Alarm (DA).** These bits store the date of month alarm value. If set to 00000b, it is assumed to be "don't care". The host must configure the date alarm field to do anything, yet it can be written at any time. If the date alarm is not enabled, this field will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by nRSMRST.

8.9.6. RTC Update Cycle

An update cycle occurs once a second, if the SET bit of register B is not asserted and the device chain is properly configured. During this procedure, the stored time and date will be incremented, overflow will be checked, a matching alarm condition will be checked, and the time and date will be rewritten to the RAM locations. The update cycle will start at least 244 μs after the UIP bit of register A is asserted, and the entire cycle will not take more than 1984 μs to complete. The time and date RAM will be disconnected from the external bus during this time. To avoid update and data contention, external RAM access to these locations should occur at two times. When a updated-ended interrupt is detected, almost 999 ms is available to read and write valid time and date data. If the UIP bit of register A is detected to be 0, there is at least 244 μs before the update cycle begins.

Because the overflow conditions for leap years and daylight savings adjustments are based on more than one date or time item, when adjusting time, it should be set to at least 2 seconds before one of the special adjustment events occur to ensure proper operation.

8.9.7. RTC Interrupt

The interrupt output of the RTC module is connected to the ISA nIRQ8 internally. If the internal RTC is disabled, the GPI6 signal line will be used as the IRQ8 input.

8.9.8. Lockable RAM Ranges

The SLC90E46 RTC supports two 8-byte ranges that can be enabled via the configuration space. If the configuration bits are set, the corresponding range in the RAM will not be readable or writeable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the actual value.
Once enabled (locked), this function can only be disabled by a hard (cold) reset.

8.9.9. RTC External Connections

RTC Crystal

The RTC module requires an externally connected crystal on the RTCX1 and RTCX2 pins.

RTC Battery

The RTC modules requires an external battery connection to maintain the RTC block while the SLC90E46 is not powered. The battery minimum voltage is 2.0V. The recommended batteries are Duracell 2032, 2025 or 2016.

The battery must be connected to the SLC90E46 via isolation diodes. The diode circuit allows the RTC-well to be powered by the battery when system power is not available, but by the system when it is available.

8.10. XBus Support

The SLC90E46 provides positive decode (chip selects) and X-Bus buffer control (nXDIR and nXOE) for an external RTC, keyboard controller, BIOS ROM, and 2 programmable IO ranges for PCI and ISA initiated cycles. The chip selects are generated by decoding ISA SA[16-0] and LA[23-17] address lines. It is assumed that ISA masters drive address lines SA[19-16] and LA[23-17] low when accessing I/O devices.

The SLC90E46 also provides coprocessor error support and is enabled via the XBCS register. The CPU coprocessor error signal is tied directly to the nFERR pin. When the signal goes low, an internal IRQ13 is generated, which causes the INTR output of the SLC90E46 go active. When the CPU writes to the I/O port 0F0h, the SLC90E46 negates IRQ13 and drives nIGNNE active. nIGNNE will remain active until nFERR is negated by the CPU.

The SLC90E46 also provides support for the mouse interrupt function. When it is enabled, a mouse interrupt generates an interrupt through IRQ12 to the CPU. A read of 60h causes the SLC90E46 to release IRQ12. When the function is disabled, reads and writes to the I/O port 60h will flow through to the ISA bus and have no effect on IRQ12/M.

8.11. Stand Alone I/O APIC Support

The SLC90E46 supports a stand-alone I/O APIC device on the ISA Xbus. It provides handshake signals to maintain buffer coherency in the I/O APIC environment. nAPICCS is generated when the PCI memory cycle address matches the APIC's programmed address and the nAPICCS function is enabled (via XBCS). The APIC address can be relocated by programming the APIC base address register (APICBASE).

nAPICCS is only generated for PCI Master originated memory cycles. The PCI cycle is forwarded to the ISA bus. To avoid address aliasing conflicts with other ISA devices, SA[19:16] and LA[23:17] are driven to 0 and SA[15:0] are correponded to PCI AD[15:2] and C/nBE[3:0].

When nAPICCS function is enabled, the nXOE/nXDIR signals controlling the X-bus transceiver are also enabled during accesses to the I/O APIC.

8.12. System Reset Logic

The SLC90E46 generates system reset signals, such as CPURST, nPCIRST and RSTDRV, during power up (PWROK) and when a hard reset is initiated through hardware Reset Switch or the RC register. During certain power management resume operations, these signals are also asserted to bring the system to a known state.

8.13. Host Interface Logic

The SLC90E46 has many signals that are interfaced to the host processor, namely: CPURST, nSTPCLK, nSLP, nSMI, nIGNNE, NMI, and INTR. These are open drain signals, thus external logic is not required even when interfacing with 2.5V processor which do not support 3.3V tolerant input buffers.

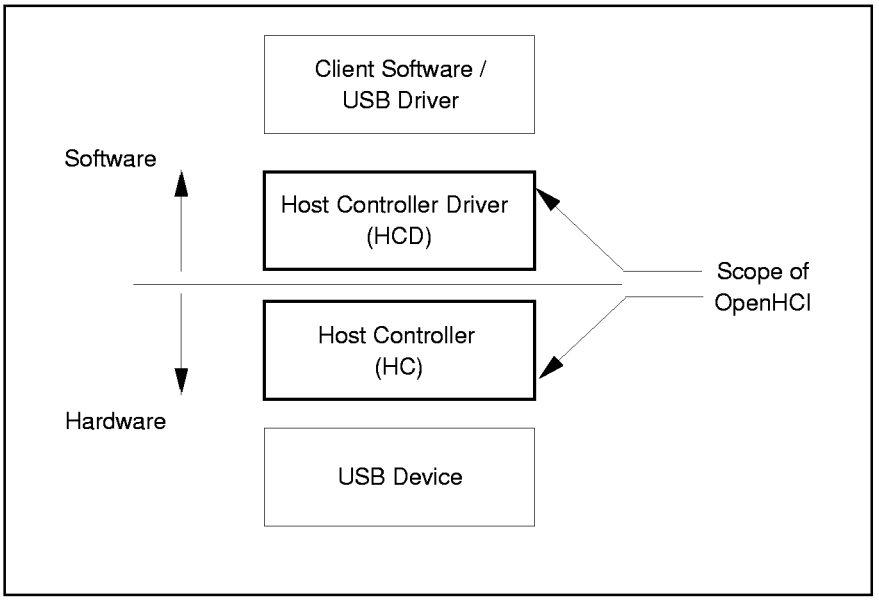
9. USB Host Controller

The SLC90E46 contains a USB Host Controller. The Host Controller includes the root hub with two USB ports, that allows direct connection of two USB peripheral devices to the SLC90E46. To support more than two USB devices in a system, an external hub can be connected to either of the two built-in ports. The USB Host Controller is implemented as function 2 of the SLC90E46 PCI configuration space.

The USB Host Controller fully implements the standard Open Host Controller Interface (OpenHCI) specification and, therefore, is compatible with the standard software drivers written to be compatible with OpenHCI. The following figure shows a conceptual view of a USB system. A USB system has four main focus areas. These areas are the Client Software/USB Driver (USBD), Host Controller Driver (HCD), Host Controller (HC), and USB Devices. The Host Controller and USB Devices are implemented in hardware. The Client Software/USB Driver and Host Controller Driver are implemented in software. OpenHCI specifies the interface between the Host Controller Driver and the Host Controller and the fundamental operation of each.

In addition, the USB Host Controller includes a mechanism to emulate legacy keyboard and mouse operation to support software which directly access to the legacy keyboard/mouse IO ports 60h and 64h. The emulation mechanism is achieved through a combination of SMI interrupt (handler) and emulation IO ports which can be accessed at addresses: 60h and 64h.

This chapter provides a brief introduction of the SLC90E46 OpenHCI-compliant USB Host Controller. For a complete description of the USB Host Controller, please refer to the USB 1.0 Specification and the OpenHCI 1.0 Specification.



9.1. Host Controller Driver

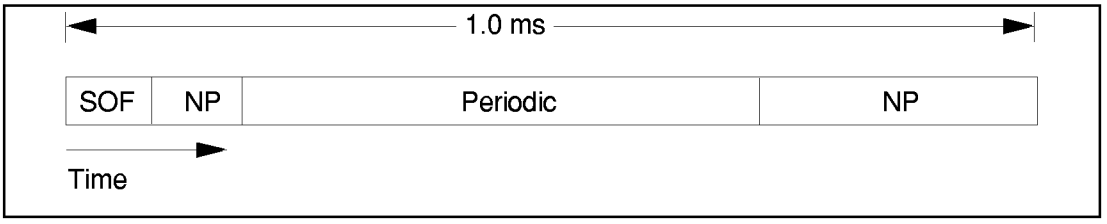
The Host Controller Driver and the Host Controller work in tandem to transfer data between client software and a USB device. Data is transferred from share-memory data structures at the client software end to USB signal protocols at the USB device end, and vice-versa. The Host Controller Driver manages the operation of the Host Controller. It does so by communicating directly to the operational registers in the Host Controller and establishing the interrupt Endpoint Descriptor list head pointers in the share-memory data structure (HCCA). The Host Controller Driver maintains the state of the HC, list processing pointers, list processing enables, and interrupt enables.

9.1.1. Bandwidth Allocation

All accesses to the USB is also scheduled by the HCD. The HCD allocates a portion of the available bandwidth to each periodic endpoint. If bandwidth is not sufficient, a newly-connected periodic endpoint will be denied access to the bus.

A portion of the bandwidth is reserved for non-periodic transfers. This ensures that some amount of bulk and control transfers will occur in each frame period. The frame period is defined for USB to be 1.0 ms.

The bandwidth allocation policy for OpenHCI is shown below. Each frame begins with the Host Controller sending the Start of Frame (SOF) synchronization packet to the USB bus. This is followed by the Host Controller servicing non-periodic transfers until the frame interval counter reaches the value set by the Host Controller Driver, indicating that the Host Controller should begin servicing periodic transfers. After the periodic transfers complete, any remaining time in the frame is consumed by servicing non-periodic transfers once more.



OpenHCI Frame Bandwidth Allocation

9.1.2. List Management

The transport mechanism for USB data packets is via Transfer Descriptor queues linked to Endpoint Descriptor lists. The Host Controller Driver creates these data structures then passes control to the Host Controller for processing.

The HCD is responsible for creating, enqueuing and dequeuing Endpoint Descriptors. Enqueuing is done by adding the Endpoint Descriptor to the tail of the appropriate list. This may occur simultaneously with the Host Controller processing the list without requiring any lock mechanism. Before dequeuing an Endpoint Descriptor, the HCD may disable the Host Controller from processing the entire Endpoint Descriptor list of the data type being removed to ensure that the Host Controller is not accessing the Endpoint Descriptor.

The HCD is also responsible for enqueuing Transfer Descriptors to the appropriate Endpoint Descriptor. Under normal operation, the Host Controller dequeues the Transfer Descriptor. However, when the Transfer Descriptor is being canceled due to a request from the client software or certain error conditions, the HCD dequeues the Transfer Descriptor. In this instance, the Endpoint Descriptor is disabled prior to the Transfer Descriptor being dequeued.

9.2. Host Controller

This section briefly describes the responsibility of the Host Controller.

9.2.1. USB States

There are four USB states defined in OpenHCI: UsbOperational, UsbReset, UsbSuspend, and UsbResume. The Host Controller puts the USB bus in the proper operating mode for each state.

9.2.2. Frame Management

The Host Controller keeps track of the current frame counter and the frame period. At the beginning of each frame, the Host Controller generates the Start of Frame (SOF) packet on the USB bus and updates the frame count value in system memory. The Host Controller also determines if enough time remains in the frame to send the next data packet.

9.2.3. List Processing

The USB Host Controller moves data between system memory and devices on the USB by processing the Endpoint Descriptors and Transfer Descriptors enqueued by the Host Controller Driver.

For periodic transfers, the Host Controller begins at the Interrupt Endpoint Descriptor head pointer for the current frame. The list is traversed sequentially until one packet transfer from the first Transfer Descriptor of all interrupt and isochronous Endpoint Descriptors scheduled in the current frame is attempted.

For non-periodic transfers, such as bulk and control transfers, the Host Controller begins in the respective list where it last left off. When the Host Controller reaches the end of a list, it loads the value from the head pointer and continues processing. The Host Controller processes *n* control transfers to 1 bulk transfer where the value of *n* is set by the Host Controller Driver.

When a Transfer Descriptor completes, either successfully or due to error condition, the Host Controller moves it to the Done Queue. Enqueuing on the Done Queue occurs by placing the most recently completed Transfer Descriptor at the head of the queue. The Done Queue is transferred periodically from the Host Controller to the Host Controller Driver via the HCCA.

10. IDE Controller Functional Overview

The SLC90E46 integrates a high performance PCI Bus Master IDE Controller. This controller is capable of accelerating PIO data transfers, it can also acts as a PCI Bus Master to transfer IDE data without the host involvement. The SLC90E46 supports interface to two IDE connectors, primary and secondary, and each connector can support two IDE devices, master and slave. A 2-Device configuration option allows a system designer to modify the interface so that it supports primary IDE drive 0 (master) on the primary IDE connector and primary IDE drive 1 (slave) on the secondary IDE connector.

Two full sets of signals are provided to enhance electrical characteristics, and provide full concurrent capability to simultaneously work with more than one IDE devices on the two IDE connectors. All IDE command strobes, DMA request and grant signals, IORDY signal, address and data lines directly interface to the SLC90E46.

The SLC90E46 only allows PCI masters to access to the IDE port. ISA masters cannot access the IDE I/O port addresses.

10.1. IDE Configurations

The SLC90E46 supports two completely independent IDE channels. This not only improves the signal timings but also allows separate power management monitoring of the two channels. The SLC90E46 has options to tri-state or isolate each channel's signals, which makes power down individual IDE devices on separate channels possible. This feature can also apply to Swap-Bay implementation where a system may have different types of devices inserted into the bay. (That requires more than one set of devices signals being connected to one Bay connector).

The IDE connectors can be configured to support 4 devices, 2 devices on each of the two channels. Or it can be configured to support two devices on the two channels so that the primary channel drive 0 is connected to the primary IDE connector, and the primary channel drive 1 is connected to the secondary IDE connector. This configuration is very useful for mobile environment since it allows for power management on individual devices.

10.2. IDE Register Blocks

The SLC90E46 IDE controller supports both legacy and PCI native modes. In PCI native mode, the register block addresses as well as the interrupt channel of the IDE controller can be relocated as a normal PCI device. In legacy mode, addresses and interrupt channels are fixed as specified by the ATA specification.

10.2.1. Legacy Mode

The ATA I/O registers are implemented in the IDE drive itself. When the IDE I/O port decoding is enabled, the SLC90E46 asserts appropriate chip select signals and the IDE command strobes, nDIOR and nDIOW, when the IDE registers are accessed.

For each cable (primary or secondary), there are two I/O ranges:

- Command block that corresponds to the nCS1x:

Primary channel: 01F0h
Secondary channel: 0170h.
This is an 8 byte range.

- Control block that corresponds to the nCS3x:

Primary Channel: 03F4h
Secondary Channel: 0374h
This is a 4 byte range

The following tables show the definitions of the Command and Control Blocks.

IDE Legacy I/O Port Definition: COMMAND BLOCK (nCS1x chip select)

IO OFFSET (BASE: 1F0/170h)	REGISTER FUNCTION (R/W)	ACCESS
00	Data	R/W
01	Error/Feature	R/W
02	Sector Count	R/W
03	Sector Number	R/W
04	Cylinder Low	R/W
05	Cylinder High	R/W
06	Drive/Head	R/W
07	Status/Command	R/W

The Data Register is accessed as a 16-bit register for PIO transfer (except for ECC bytes). All other registers are accessed as 8-bit quantities.

To determine the targeted drive, the SLC90E46 shadows the value of bit 4 (drive bit) of byte 6 (Drive/Head Register: 01F6h/0176h) of the ATA Command Block (nCS1x) for each of the two IDE connectors.

IDE Legacy I/O Port Definition: CONTROL BLOCK (nCS3x chip select)

IO OFFSET (BASE:3F4/374h)	REGISTER FUNCTION (R/W)	ACCESS
00	Reserved	Reserved
01	Reserved	Reserved
02	Alt Status/Device Control	R/W
03	Forward to ISA (floppy)	R/W

10.2.2. PCI Native Mode

In PCI native mode, the registers of the IDE channels are completely relocatable in I/O space. Base address registers at offset l0h, 14h, 18h and 1Ch in the IDE Controller configuration space are used to relocate the IDE registers into different I/O locations. Specific base address registers are used to map the different register blocks as defined in the following table:

CHANNEL	COMMAND BLOCK REGISTERS	CONTROL BLOCK REGISTERS
Primary	Base address at offset 10h	Base address at offset 14h
Secondary	Base address at offset 18h	Base address at offset 1Ch

10.3. PIO IDE Operations

The IDE controller includes both compatible and fast timing modes. The fast timing mode can only apply to the IDE data ports. All other transactions to the IDE registers are run in single transaction mode with compatible timings. The IDETIM and SIDETIM registers permit different timing modes, from ATA Mode 0 to ATA Mode 4, to be programmed for drive 0 and drive 1 on the same connector, which translates into 3MB/sec to 16MB/sec data transfer rate. The Ultra DMA/33 synchronous DMA timing modes can also be applied to each drive by programming the UDMACTL and UDMATIM registers. When a drive is enabled in Ultra DMA mode operation, the DMA transfers are executed with the Ultra DMA timings. The PIO data transfers are still executed using compatible timings or fast timings when enabled.

10.3.1. PIO IDE Data Transfer Cycle

IDE data transfer cycle can be decomposed into three portions: startup latency, cycle latency, and shutdown latency.

- **Startup Latency:** If the DA[2:0] and nCSxx lines are not set up, startup latency is incurred when a PCI cycle that accesses the IDE data port is decoded. Startup latency provides the setup time for assertion of the DA[2:0] and nCSxx lines prior to assertion of the read and write strobes (nDIOR and nDIOW).

- **Cycle Latency:** Cycle latency consists of the I/O command strobe assertion length and recovery time. Recovery time is needed so that back-to-back transactions, which does not incur startup and shutdown latency, may occur on the IDE interface without violating minimum cycle periods for the IDE interface. The command strobe assertion width (IORDY Sample Point: ISP) for the fast timing mode is selected by the IDETIM Register and it can be set to 2, 3, 4, or 5 PCI clocks. The recovery time (RCT) is also decided by the IDETIM Register and it can be set to 1,2,3 or 4 PCI clocks.

If the IORDY is asserted when the IORDY sample point is reached, no wait states are added to the command strobe assertion length. If IORDY is negated when the sample point is reached, additional wait states are added. Since the rising edge of IORDY is synchronized by PCI clock, at least two additional PCI clocks will be added to the Cycle latency.

IORDY Masking: The IORDY signal can be ignored and assumed asserted at the first ISP on a drive by drive basis through the IDETIM register.

- **Shutdown Latency:** Shutdown latency is incurred after the IDE data transactions (either a non-empty write post buffer to the IDE drive or an outstanding read prefetch cycles from the IDE drive) have completed and before other IDE transactions can proceed. The latency provides hold time on the DA[2:0] and nCSxx lines with respect to the read and write strobes (nDIOR and nDIOW). Shutdown latency is set to 2 PCI clocks in duration.

The following table shows the IDE cycle timings for various IDE transaction types.

IDE TRANSACTION TYPE	STARUP LATENCY (PCI Clocks)	ISP (PCI Clocks)	RCT (PCI Clocks)	SHUTDOWN LATENCY (PCI Clocks)
Non-Data Port Compatible	4	11	22	2
Data Port Compatible	3	6	14	2
Fast Timing Mode (for Data Port Accessing)	2	2-5	1-4	2

Note: When any of the fast timing modes are used, the IDE data access cycles are not affected by the selection of the ISA IO Recovery time.

10.3.2. 32-Bit PIO IDE Data Transfer Cycle

A 32-bit PCI transaction to the IDE data ports results in two back to back 16-bit IDE accesses to the data ports. The 32-bit data transfer feature is enabled for all timings, including Compatible timing modes. In Compatible timing modes, the SLC90E46 adds a shutdown and startup latency between the two 16-bit halves of the IDE transaction. This will cause IDE chip selects be deasserted for at least 2 PCI clocks between the two 16-bit cycles.

10.3.3. PIO IDE Data Prefetching and Posting

The IDE controller starts data prefetching when a data port read cycle is decoded by the SLC90E46. The prefetched IDE data is stored in the 64-byte data buffer (one for each IDE channel) for the host processor to retrieve. The read prefetch eliminates read latency to the IDE data ports and allows IDE data reads to be performed in a back-to-back way for highest possible PIO data transfer rates.

The IDE controller performs data posting for writes to the IDE data ports through the 64-byte buffer. The SLC90E46 completes the PCI transaction after data is received and stored into the buffer. The IDE controller then runs IDE cycles to transfer data to the drive. If the data buffer is not empty and a unrelated (non-data or same channel but different device) IDE transaction occurs, that transaction will be pending until all current data in the write buffer is transferred to the drive.

10.4. Bus Master Operations

The SLC90E46 IDE controller supports two bus master channels for the two IDE connectors. Both devices attached to a connector can be programmed for bus master transfers. The Bus Master IDE data transfer can off-load the processor and improve system performance in a multitasking environment.

10.4.1. Physical Region Descriptor (PRD)

The Physical Region Descriptors provide the necessary information of IDE data transfer requests for the Bus Master controller. The PRDs are stored sequentially in a Descriptor Table in memory. The data transfer proceeds until all regions described by the PRDs in the table have been transferred. Descriptor tables must be aligned on 64 Kbyte boundaries.

Each PRD entry in the table is 8 bytes in length. The first four bytes specify the address of a physical memory region. The memory region has to be DWORD aligned, and should not cross a 64KB boundary. The next 2 bytes specify the size of the region in bytes (up to 64kbyte per region). 64kbyte is represented by a value of 0. When bit 7 of the last byte (EOT) is a 1, it indicates that this is the last PRD in the Descriptor table.

Byte 3	Byte 2	Byte 1	Byte 0	
Memory Region Physical Base Address [31:1]				0
EOT	Reserved	Byte Count [15:1]		0

When reading data from the memory region, bit 1 of the Base Address is masked and byte enables are asserted for all read transfers. When writing data to the memory region, bit 1 of the Base Address is not masked and if it is set, will cause the lower WORD "byte enable" to be deasserted for the first DWORD transfer.

The total sum of the byte counts in every PRD of the descriptor table must be equal to or greater than the size of the disk transfer request. If greater than the disk transfer request, the driver must terminate the bus master transaction (by setting bit 0 in the Bus Master IDE Command Register to 0) when the drive issues an interrupt to signal transfer completion.

10.4.2. Bus Master Transfer Operation

Bus Master IDE Timings

The IDE controller supports the IDE cycle timing specifications defined for Multiword DMA Mode 0, and Multiword DMA MODES 1 and 2. The same set of IDE Timing Registers is used to select the IDE data transfer cycle timing for both Master transfers mode and PIO transfer mode.

The Initialization Phase

- The driver has to prepare a PRD table in main memory. In the table, two consecutive PRDs are offset by 8-byte and are aligned on a 4-byte boundary.
- The driver then writes the address of the PRD Table into the PRD Table Pointer Register of the IDE controller. Then it sets the transfer direction, clear the interrupt bit and error bit.
- The driver then writes the appropriate DMA commands to the disk drive, including the data transfer count.
- Finally, the driver can start the bus master function by writing a 1 to the Start bit of the Bus Master IDE Command Register.

The Data Transfer Phase

- The IDE controller starts the data transfer phase by fetching the first PRD from the PRD Table. From the PRD, the controller gets the address of the physical memory block and the memory block size.

  When enabled and supported by the device, DMA transfers are executed on the IDE interface, the selected ports' chip selects (nPDCS1 and nPDCS3 for primary or nSDCS1 and nSDCS3 for secondary) will be negated (high). When the IDE device asserts P(S)DDREQ, the SLC90E46 will return nP(S)DDACK to the IDE device when it is ready for the DMA data transfer. For multiword DMA transfers, the nP(S)DIOR or nP(S)DIOW signal will free run at the programmed rate as long as P(S)DDREQ remains asserted and the SLC90E46 is prepared to complete a data transfer. If P(S)DDREQ has not de-asserted by the rising edge of the nP(S)DIOW or nP(S)DIOR signal multiword DMA is assumed and at least one more cycle will be executed. If P(S)DDREQ de-asserts before nP(S)DIOW or nP(S)DIOR is de-asserted while nP(S)DDACK is asserted, it indicates that one last data transfer remains for the current session. In this case, nP(S)DDACK will be de-asserted one clock after the nP(S)DIOW or nP(S)DIOR signal de-asserts. This allows the IDE controller to support both single and multiword DMA cycles automatically.

  The IDE device DMA request signal is sampled on the same PCI clock that the IO strobe is deasserted. If inactive, the DMA Acknowledge signal is deasserted on the next PCI clock and no more transfers take place until DMA request is again asserted.

- The controller transfers data to or from memory region responding to the DMA requests from the IDE device. The controller will fetch the next PRD from the table once the last data transfer for a memory region has been completed.

The Completion of DMA Data Transfers

The IDE device signals an interrupt once its programmed data count has been transferred. The IDE device will also deassert its DMA request signal, causing the SLC90E46 to stop transferring data. If the SLC90E46 has also transferred the final data from the last PRD memory region, it will reset the BMIDEA bit in the status register and mask the DMA request signal from the drive.

The BMIDEA bit in the BMIDE Status register is reset automatically when the controller has transferred all data associated with a Descriptor Table. The IDE Interrupt Status bit is set when the IDE device generates an interrupt. These events may occur prior to buffer emptying for memory writes. The SLC90E46 will buffer the IDE interrupt until the buffer is cleared. All PCI Master non-memory read accesses to SLC90E46 are retried until all data in the buffer has been transferred to memory.

10.5. Ultra DMA/33 Synchronous DMA Operation

Ultra DMA/33 is a new IDE transfer protocol used to transfer data between a Ultra DMA/33 capable IDE controller and Ultra DMA/33 capable IDE devices. Ultra DMA/33 utilizes a "source synchronous" signaling protocol to transfer data at rates up to 33 Mbytes/sec.

10.5.1. Ultra DMA/33 Signals

The Ultra DMA/33 protocol defines three hand-shaking signals: STOP, STROBE and DMARDY.

STOP: STOP is always driven by the IDE controller, such as the SLC90E46, and is used to request that a transfer be stopped or as an acknowledgment to stop a request from IDE device.

STROBE: This is a data strobe signal driven by the TRANSMITTER of a data transfer, which is either the IDE device of a DMA Read transfer or the SLC90E46 of a DMA Write transfer, on which data is transferred during each rising and falling edge transition of the signal.

nDMARDY: This is a target ready signal driven by the RECEIVER of a data transfer, which is either the SLC90E46 of a DMA Read transfer or the IDE device of a DMA Read transfer, to signal when the RECEIVER is ready to transfer data or to add wait states to the current transaction.

The Ultra DMA/33 protocol uses the existing signal pins on the IDE connector. It redefines a number of the standard IDE control signals when the controller is put in the Ultra DMA/33 mode. The following table shows the signal redefinition.

STANDARD IDE SIGNAL NAME	SLC90E46 PRIMARY CHANNEL SIGNAL NAME	SLC90E46 SECONDARY CHANNEL SIGNAL NAME	SIGNAL NAME DURING ULTRA DMA/33 READ CYCLE	SIGNAL NAME DURING ULTRA DMA/33 WRITE CYCLE
nDIOW	nPDIOW	nSDIOW	STOP	STOP
nDIOR	nPDIOR	nSDIOR	nDMARDY	STROBE
IORDY	PIORDY	SIORDY	STROBE	nDMARDY

Note: **"Ultra DMA/33 Read Cycle":** Transferring data from the IDE device to the SLC90E46.
"Ultra DMA/33 Write Cycle": Transferring data from the SLC90E46 to the IDE device.

The nDIOW signal is redefined as STOP for both read and write transfers.

The nDIOR signal is redefined as nDMARDY when transferring data from the IDE device to the SLC90E46. It is used by the SLC90E46 to signal when it is ready to transfer data or to add wait states to the current transaction. The nDIOR signal is redefined as STROBE for transferring data from the SLC90E46 to the IDE device. It is the data strobe signal driven by the SLC90E46 to transfer data on each rising and falling edge transition.

The IORDY signal is redefined as STROBE when transferring data from the IDE device to the SLC90E46. It is the data strobe signal driven by the IDE device to transfer data on each rising and falling edge transition. The IORDY signal is redefined as nDMARDY for transferring data from the SLC90E46 to the IDE device. It is used by the IDE device to signal when it is ready to transfer data or to add wait states to the current transaction.

10.5.2. Ultra DMA/33 Operation

Initialization

Initialization includes enabling and performing proper set up on the SLC90E46 and the IDE device. For SLC90E46, it is necessary to enable Ultra DMA/33 mode for the targeting IDE device and setting up the Ultra DMA/33 cycle timings through the register SDMATIM. The SLC90E46 supports three timing modes: Mode 0 (120ns cycle time), Mode 1 (80 ns cycle time) and Mode 2 (60ns cycle time).

Data Transfer Operation

The actual data transfer consists of three phases, a start-up phase, a data transfer phase, and a burst termination phase.

- **Start-Up Phase**: The IDE device begins the start-up phase by asserting DMARQ signal. When ready to begin the transfer, the SLC90E46 will assert nDMACK. When nDMACK is asserted, the SLC90E46 will drive nCS0/1 inactive, DA0-DA2 low and the IDE device will drive nIOCS16 inactive.
    - **For Write cycles,** the SLC90E46 will deassert STOP, wait for the IDE device to assert nDMARDY and then drive the first data word and the STROBE signal.
    - **For Read cycles,** the SLC90E46 will tristate the data lines, deassert STOP, and assert nDMARDY. The IDE device will then drive the first data word and the STROBE signal.
- **Data-Transfer Phase:** The burst data transfer continues with the data source (Writes: SLC90E46, Reads: IDE devices) providing data and toggling STROBE. Data is transferred (latched by receiver) on each rising and falling edge of STROBE.
    - The source can pause the burst stream by holding STROBE high or low, resuming the burst stream by again toggling STROBE.
    - The receiver can pause the burst stream by negating the nDMARDY and resumes the transfers by asserting nDMARDY.

The SLC90E46 may pause a burst transaction in order to prevent an internal data buffer (64 bytes in size per channel) over or under flow condition, resuming once the condition has cleared. It may also pause a transaction if the current PRD byte count has expired, resuming once it has fetched the next PRD.

- **Termination Phase:** Either the source or the receiver can terminate a burst transfer. A burst termination consists of a Stop Request, Stop Acknowledge and transfer of CRC data.
    - The SLC90E46 can stop a burst by asserting STOP, with the IDE device acknowledged by deasserting DMARQ.
    - The IDE device stops a burst by deasserting DMARQ and the SLC90E46 acknowledges by asserting STOP.
    - The source then drives the STROBE signal to a high level. The SLC90E46 then drive the CRC value onto the data lines and deassert nDMACK. The IDE devices will latch the CRC value on the rising edge of nDMACK.

The SLC90E46 will terminate a burst transfer if a Programmed I/O (PIO) cycle is executed to the IDE channel currently running the burst, or upon transferring the last data from the final PRD.

Cyclic Redundancy Checking (CRC) Calculation

Cyclic Redundancy Checking (CRC-16) is used for error checking on Ultra DMA/33 transfers. The CRC value is calculated for all data by both the SLC90E46 and the IDE device over the duration of the DMA burst transfer segment. This segment is defined as all data transferred with a valid STROBE edge from nDDACK assertion to nDDACK deassertion. At the end of the transfer burst segment, the SLC90E46 will drive the CRC value onto the DD[15:0] signals. The value is then latched by the IDE device on deassertion of nDDACK. The IDE device compares the SLC90E46 CRC value to its own and reports an error if there is a mismatch.

10.6. IDE Data Buffer

The SLC90E46 IDE controller integrates a 64-byte data buffer for each of the two IDE channels. The buffer is used in both PIO mode and Bus Master mode (including Ultra DMA/33 mode). While in the PIO mode the deep buffer is used only partially because of the slow nature of the IDE interface, in Bus Master mode, it greatly enhances PCI bus efficiency as well as CPU's availability since long burst stream (to or from the deep 64-byte data buffer) can be sustained on the PCI bus without CPU's intervention.

The 16-level Dword buffer (per channel) is organized into two 8-level Dword buffers (per channel). In Read IDE operation, the IDE controller starts a PCI master transaction to transfer data to the system memory when one of the two 8-level Dword buffers is full. While data is being moved to the system memory on the PCI bus, the IDE controller continues to fill the other 8-level Dword buffer with the incoming IDE data. It takes 8 PCICLKs (plus a bus arbitration latency) to transfer data from a full buffer to the system memory.

In Write IDE operation, the IDE controller starts a PCI master transaction to fetch data from the system memory when an 8-level Dword buffer is empty. While the controller is fetching data from system memory through the PCI bus, it continues to move data from the other buffer to the IDE device. It takes 8 PCICLKs (plus a bus arbitration latency) to fill up a 32-byte buffer with system data.

11. Power Management Overview

The SLC90E46 Power Management covers the following four main areas:

- Processor Complex Management
- Peripheral Device Management
- System Management (SMI Generation, System Management Bus)
- System Suspend and Resume

The SLC90E46 helps the power management software initiate and manage the transitions between different power states. It provides system-wide Peripheral Event Monitors to identify idle and wake-up conditions, System Management Interrupt (nSMI) support, Advanced Power Management (APM) 1.2 interface, Pentium nSTPCLK Clock Control, Suspend/Resume Hardware, and System Management Bus.

System power management operates through a combination of hardware and software control. The software consists of System Management Mode (SMM) BIOS for legacy mode and Operating System (OS) for ACPI mode. The basic power management operation can be depicted as follow:

- The software sets up the desired configuration and the power savings level.
- The hardware then performs actions to maintain the power state. It also monitors the system for events which may require changing the system power state.
- Upon detection of one of these events, the hardware informs the BIOS or OS, which make the decision to switch power states. This is done by a System Management Interrupt (nSMI) in legacy mode or a System Control Interrupt (SCI) for ACPI OS.

Following is a brief description of the SLC90E46 Power Management function.

Processor Complex

The Processor Complex includes Processor, L2 Cache, DRAM, and Host Bridge, which are applied with the same clock source (but could be driven by different clock buffers).

Clock Control

When the operating system (or application program, or system software) is not doing useful work (but stays in an idle loop), the processor complex can be placed in a power saving state. The SLC90E46 manages the host and peripheral bus clocks to achieve low power consumption in various power saving states:

- Various nSTPCLK schemes for processor clock control.
  - **Throttling:** nSTPCLK duty cycle control for low frequency emulation.
  - **Stop Grant State:** Processor clock RUNNING but nSTPCLK asserted.
  - **Stop Clock State:** Processor clock STOPPED and nSTPCLK asserted.
- Clock resume (break) from interrupts, device monitors, bus activity, and external inputs.
- Automatic burst Mechanism
  - Hardware processor clock control scheme.
- Automatic processor clock throttling during critical thermal conditions.
- Low power mode for L2 cache memory during standby state

- ZZ Mode
- nCLKRUN protocol for PCI clock control
  - Independent from processor clock control.

Peripheral Device Power Management

The SLC90E46 monitors peripheral device resources to detect when a specific device is idle. It will then inform power management software to put that individual device into a power saving state (such as Standby or Powered Off).

The SLC90E46 also monitors accesses targeting low-power-state devices. When detected, an nSMI is generated to inform the software to restore the device to its operating state.

The SLC90E46 implements the following logic to support Device Power Management:

- 14 distinct device monitors and idle timers
- 4 generic device monitors
- Monitor devices on PCI or ISA bus
- Monitor general purpose inputs
- I/O traps with nSMI assertion and I/O cycle restart

System Management

The SLC90E46 also monitors many other system events, including an external power button, notebook lid and other type of switches, modem ring signal, global system activity, thermal alarm input, countdown timers, and SMBus message generation and receipt. These events can trigger the SLC90E46 to generate an SMI to the processor for system power management.

System Suspend

Once an idle system is detected or a critical system event has occurred, the software can place the system into a suspend state for further power savings. The software configures the SLC90E46 for the type of suspend, types of resume or wake-up events, and then triggers the SLC90E46 to switch the system into the selected suspend state. Upon detection of any enabled resume events, the SLC90E46 will automatically restore the system to its normal operating state.

Following is a summary of Suspend and Resume features:

- Supports Three Suspend States
  - Power-On-Suspend (POS) with 3 system reset options
  - Suspend-to-RAM (STR)
  - Suspend-to-Disk (STD) or Soft Off (Soff)
- Supports Resume Power and Reset Sequencing
- Integrate a Global Standby Timer to monitor overall system idleness and as a resume timer.
- Power Button Input (nPWRBTN)
  - Supports ACPI over-ride feature forcing immediate transition to Soft Off
- Battery Low Indication Input (nBATLOW)
- Shadow Standard AT Write-Only Registers to save and restore system state information.

11.1. System Clock Control

In a PCI-Bus based system, there are two clock sources, system host clocks and PCI clocks, to be managed for lower system power consumption. The SLC90E46 allows separately control the system host clocks and PCI clocks. The Host Clock Control primarily uses the processor clock control features, but also adds some capabilities to allow for more flexible and robust power management. It supports the Pentium Processor Stop Grant and Stop Clock states. The PCI Clock Control uses the Clock Run mechanism as described in the PCI Mobile Design Guide. This figure shows an example of system configuration.

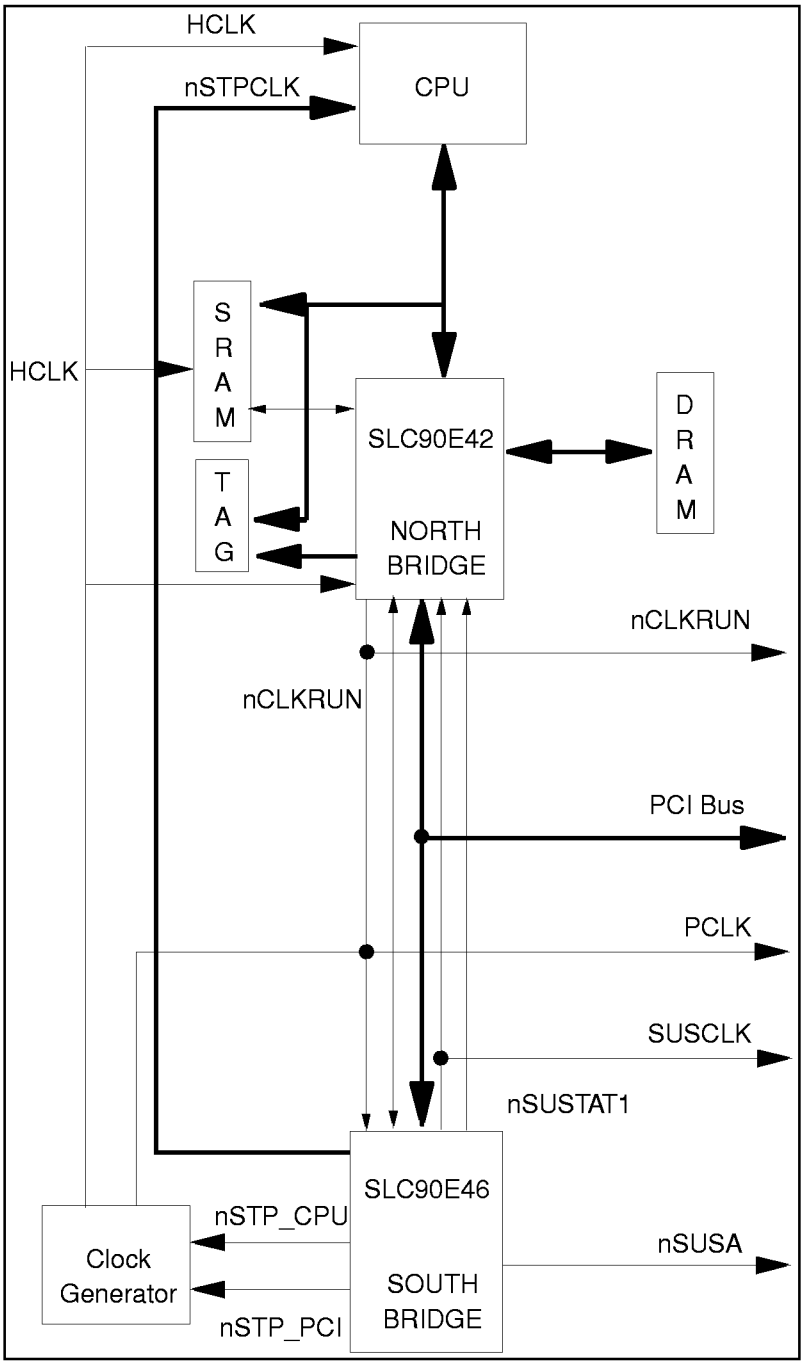


FIGURE 2 - SLC90E46 SYSTEM CONFIGURATION

11.1.1. Host Clock Control

The SLC90E46 supports two primary Host Clock Control Mechanisms with three types of variations. The SLC90E46 monitors system events to break out of clock control modes or to generate burst execution. Software can enable clock control by setting [CC_EN] bit with other optional control bits.

Primary Host Clock Control Mechanisms

- For Pentium Processor
  - Stop Grant
  - Stop Clock

Clock Control Variations

- Manual Throttle
- Thermal Throttle
- Stop Break and Burst Execution

Table 35 - Clock Control Mechanisms Programming

CLOCK CONTROL MECHANISM	INVOKING MECHANISM	CONTROL BIT CC_EN	CONTROL BIT STP_CLK_EN	CONTROL BIT SLEEP_EN	CONTROL BIT THT_EN
Thermal Throttle	External thermal input: nTHRM	x	x	x	x
Disable Clock Control		0	x	x	x
Stop Grant w/o Throttle	Read LVL2 Register	1	x	x	x
Stop Grant w. Throttle	Read LVL2 Register	1	x	x	1
Reserved	Read LVL3	1	0	0	x
Sleep	Read LVL3	1	0	1	x
Stop Clock	Read LVL3	1	1	0	x
Deep Sleep	Read LVL3	1	1	1	x
Enable Burst Execution **	Read LVL3	1	x	x	x

Note: ** **Burst Execution** is always enabled for any of the above modes (except disabled and thermal throttle) if **BRST_EN bit is set.**

Stop Grant State

The Stop Grant state can be initiated by a read to the LVL2 register, the nSTPCLK signal is asserted and the SLC90E46 waits for the processor to issue a Stop Grant bus cycle. Upon termination of the Stop Grant cycle**,** the SLC90E46 will assert the ZZ pin to the L2 SRAM if the [ZZ_EN] bit is set. The SLC90E46 does not assert the nCPU_STP signal and the Host Clocks remain running in this state. In this state, the processor disables clocks to portion of its internal logic, but is able to snoop host bus cycles in order to maintain cache coherency. To exit this state, the SLC90E46 will first deassert the ZZ signal (if applicable) and then deassert nSTPCLK.

To initiate Stop Grant state:
Read LVL2 with CC_EN bit set.

In Stop Grant state, the SLC90E46 will

1. Assert nSTPCLK.
2. Upon termination of STOP GRANT cycle, assert the ZZ signal.

To exit from Stop Grant state (when a wakeup event is detected), the SLC90E46 will

1. Deassert ZZ signal, and then nSTPCLK.

Stop Clock State

Stop Clock State is initiated by a read to the LVL3 register, the nSTPCLK signal is asserted by the SLC90E46 and the processor issues a Stop Grant Bus Cycle. Upon termination of the Stop Grant cycle, the SLC90E46 asserts the ZZ pin to L2 SRAM (if [ZZ_EN] is set), asserts the nSUS_STAT1 signal to Host Bridge to enable Suspend Refresh for the DRAM, and then assert nCPU_STP signal to the clock synthesizer.

The Host clocks stop running in this state. The processor does not snoop host bus cycles and no other master devices should access main memory during this state. To exit this state, the SLC90E46 will deassert the nCPU_STP signal. At this time the SLC90E46 will first load the FAST BURST TIMER with [CPU_LCK] value and count down allowing time for the processor PLL to lock. After the timer expires, the SLC90E46 will then deassert nSUS_STAT1 signal, the ZZ signal (if applicable), and finally nSTPCLK.

To initiate Stop CLOCK state:
Read LVL3 with CC_EN and STP_CLK_EN bits set.

In Stop CLOCK state, the SLC90E46 will

1. Assert nSTPCLK.
2. Upon termination of STOP GRANT cycle, assert the ZZ signal.
3. Assert nSUS_STAT1 to the host bridge chip to start suspend refresh.
4. Assert the nCPU_STP signal to the clock synthesizer. At this time, all components of the Processor Complex receive no clock.

To exit from Stop CLOCK state (when a Resume Event is detected), the SLC90E46 will

1. Deassert nCPU_STP signal, and load the FAST BURST TIMER with [CPU_LCK] value and starts to count down (that allows the CPU PLL to lock).
2. After the fast burst timer expires, deassert the nSUS_STAT1, then ZZ signal, and finally nSTPCLK.

Thermal Throttle Control Mechanism

When the nTHRM signal is asserted for greater than 2 seconds, it indicates a Thermal Alert condition. When it occurs and the system is not in the Stop Clock state, the SLC90E46 will automatically start toggling the nSTPCLK signal and ZZ signal (if [ZZ_EN] set) with a period of 244μs and a programmable duty cycle to reduce thermal dissipation. This system will toggle between full-speed operation and the Stop Grant state. The duty cycle can be set in 12.5% increments by programming the [THRM_DTY] bits in the Count B (CNTB) register.

The functionality of thermal throttling is independent of the [THRM_EN] bit, which is used to enable events, via generation of nSMI/SCI signal, for other power management functions. The [THRM_DTY] field must be programmed by the BIOS. This emulates a reduced frequency host clock, resulting in reduced power and thermal generation. When the nTHRM signal is deasserted, the system will return to clock control previously in use.

The thermal throttle state is not affected by [CC_EN] setting.

To Enter Thermal Throttle Mode
The nTHRM is asserted for greater than 2 seconds, and system is not in Stop Clock.

Thermal Throttle Mode Behavior
nSTPCLK and ZZ signal are toggled.

To Exit From Thermal Throttle Mode
Deasserts the nTHRM, and it will be back to the clock control mode previously in use.

Clock Throttle Control Mechanism

If the system has been placed into the Stop Grant state and [THT_EN] bit is set, the SLC90E46 will toggle both nSTPCLK and ZZ (if [ZZ_EN] set) with a period of 244μs (approximately eight 32Khz clock periods) and a programmable duty cycle. This system will toggle between full-speed operation and the Stop Grant state. The duty cycle can be set in 12.5% increments by programming the [THTL_DTY] bits in the Processor Control [P_CNTRL] register.

Burst Execution and Stop Break Control Mechanism

Once the hardware has been placed into a clock control state, it can be restored to full operation through hardware event or software. Software can restore the system to full speed operation by cleaning the [CC_EN] bit, but this is only possible after the system is waken up by a resume event or if the system is in Stop Grant Throttle mode. Hardware events can be enabled to return the system to a non-clock controlled condition. If the [BRST_EN] bit is reset, these events are called Stop Break Events. If the [BRST_EN] bit is set, these events are called Burst Event.

Stop Break events return the system to non-clock controlled state. In order to restore clock control, software must set up the desired clock control configuration and again perform a read from LVL2 or LVL3 register to initiate the control.

Burst Events cause the reload of a Burst Timer, which begins to count down from its loaded initial value. While the timer is counting, the system return to full clock operation. Once the burst timer expires, the system automatically returns to the clock controlled state. The SLC90E46 provides 2 different burst timers, a fast burst timer (which generates a short burst period) and a slow burst timer (which generates a longer burst period).

Stop Break events are superset of fast burst and slow burst Events. If the [BRST_EN] bit is set, the burst events will reload their associated burst timer. When the [BRST_EN] bit is cleared, these events will generate a Stop Break event. The Fast Burst and Slow Burst timers and the burst event programming information are summarized as follows.

Fast Burst Timer

Resolution: 1msecond
Count: [FB_CNT] / 5 bit

Slow Burst Timer
Resolution: 1 second
Count: [SB_CNT] / 4 bit

Fast Burst Timer for CPU PLL Lock
Resolution: [CPU_SEL]: 1 usec or 1 msec
Count: [CPU_LCK] / 5 bit

Fast Burst Events

EVENT NAME	CONTROL BIT
IRQ0	[BRLD_EN_IRQ0]
IRQ8	[BRLD_EN_IRQ8]
NMI, INIT, IRQ[1, 3-7, 9-15]	[BRLD_EN_IRQ]
PCI Bus Master Activity	[BRLD_EN_BM]
Device 0-13 Monitors:	[BRLD_EN_DEVx] x=1 - 13
Slow/Fast Burst Select	[BRLD_SEL_DEVx] x=1 - 3, 5
Power Management Events:	[BRLD_EN_PME] - GPI1] Asserted - LID Asserted - Polarity Select [LID_POL] - PWRBTN Asserted - nSMI Event

Slow Burst Events

Device 0 - 13 Monitors:	[BRLD_EN_DEVx] x=1 - 3, 5
Slow/Fast Burst Select	[BRLD_SEL_DEVx] x=1 - 3, 5

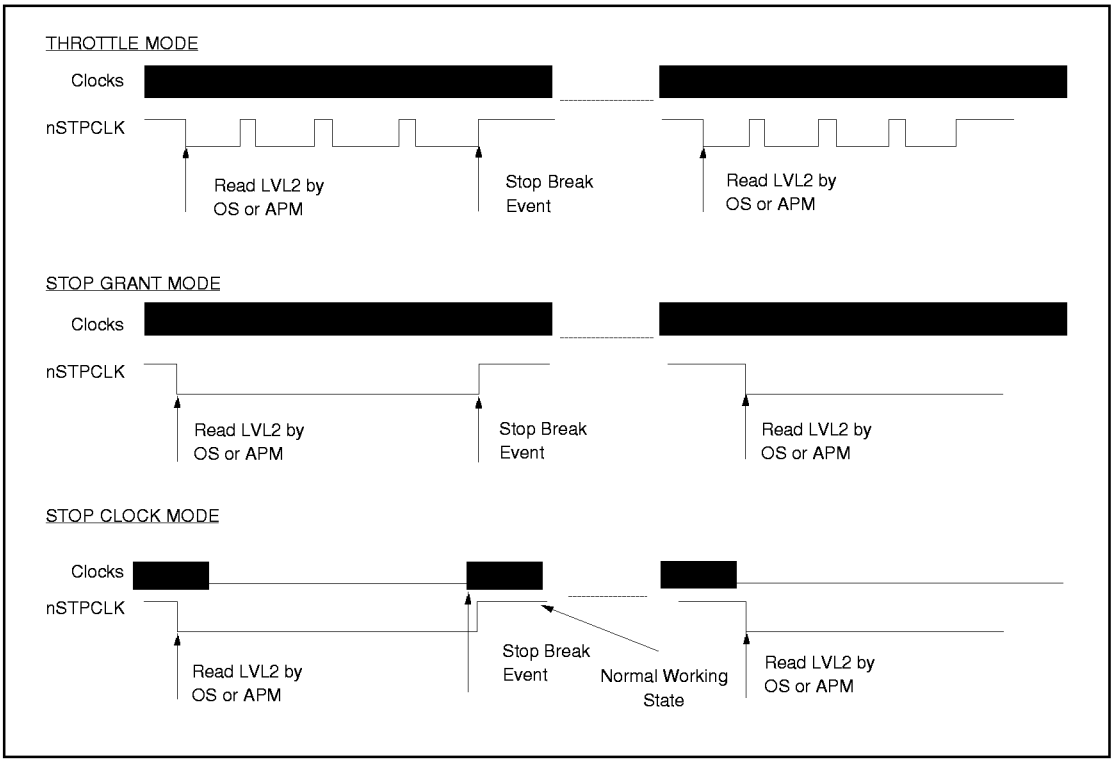


FIGURE 3 - CLOCK CONTROL MECHANISM (NON-BURST)

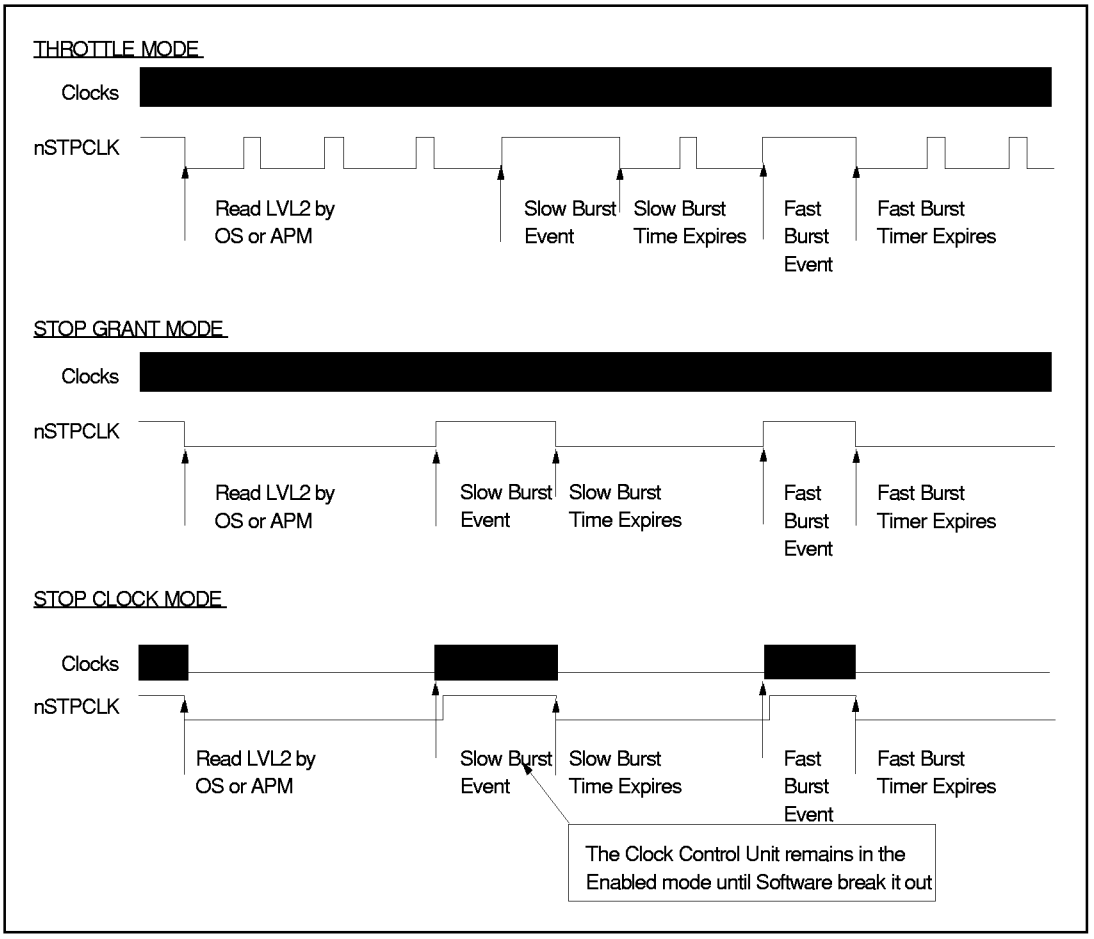


FIGURE 4 - CLOCK CONTROL MECHANISMS (WITH BURST ENABLED)

11.1.2. Stop Clock State Example Sequence

The Stop Clock Mode requires special consideration to allow the processor PLL to stabilize before starting any activity that would involve the processor. The following is an example of system transition into and out of Stop Clock. The following figure shows an example timing diagram. The numbers shown in braces {} below correspond to the number shown in the diagram.

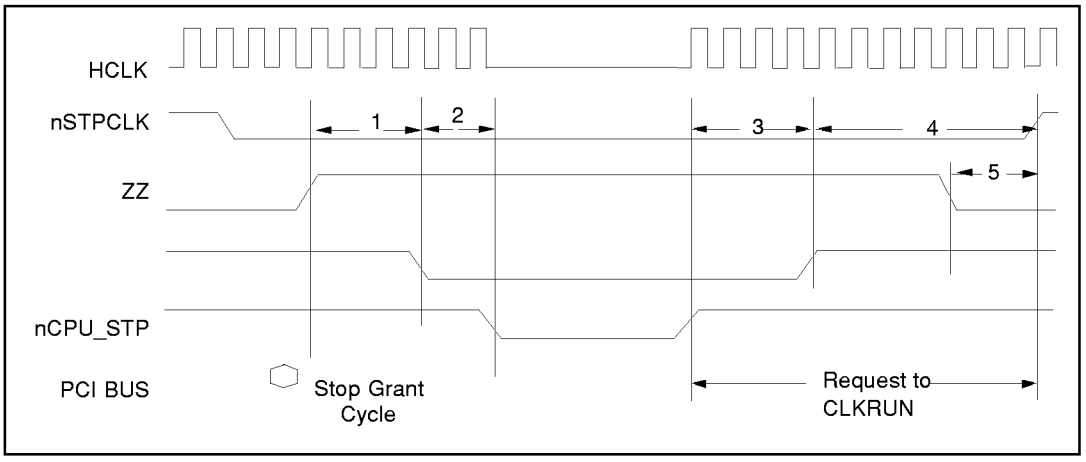


FIGURE 5 - STOP CLOCK EXAMPLE

Notes:

1) SLC90E46 waits 2 32kHz clock periods to assert nSUS_STAT1 to the Host Bridge to allow the Host Bridge to complete pending cycles to DRAM.
2) SLC90E46 waits one 32 kHz clock period to assert nCPU_STP to the Clock Synthesizer to allow the Host Bridge to switches from Normal Refresh to Suspend Refresh. The assertion of nCPU_STP will stop the Host Clocks to the processor, host bridge, L2 Cache, and SDRAM.
3) SLC90E46 waits around 1ms + 1 32 kHz, timed by Burst Timer, to deassert nSUS_STAT1 after the deassertion of nCPU_STP, which allows the processor PLL to start and lock.
4) SLC90E46 waits up to 2 32kHz to deassert nSTPCLK after the deassertion of nSUS_STAT1.
5) SLC90E46 deasserts ZZ at least 2 PCI clocks before the deassertion of nSTPCLK.

To Enter Stop Clock State

Initialization

Software sets up the SLC90E46 for the appropriate Clock Control Mechanism. Software disables the PCI arbiter in the Host Bridge.

Invoke State Transition

Software reads register LVL3.

SLC90E46 Actions (In Sequence)

- SLC90E46 asserts nSTPCLK.
  1. Processors accepts nSTPCLK, flushes buffers, issues STOP GRANT cycles.

2. SLC90E42 Host Bridge forwards Stop Grant bus cycle to the PCI bus then does a PCI Master Abort cycle. The CPU cycle is completed by returning a nBRDY to the processor.
3. Processor gates the internal clocks to the processor core and enters the Stop Grant state.

- SLC90E46 asserts ZZ pin to L2 SRAM if [ZZ_EN] is set after the PCI Stop Grant cycle.
- SLC90E46 waits 2 32Khz clock periods after receiving the Stop Grant Bus Cycle to assert nSUS_STAT1 to the SLC90E42.
  - SLC90E42 has to complete pending DRAM cycle before the nSUS_STAT1 is asserted.
  - SLC90E42 switches from Normal Refresh to Suspend Refresh with the assertion of nSUS_STAT1.

- SLC90E46 waits an additional 32Khz clock period after the assertion of nSUS_STAT1 to assert nCPU_STP to the Clock Synthesizer.
  - Clock Synthesizer stops the host clocks to the Processor Complex, including L2 cache, SLC90E42 and SDRAM. Processor now is in Stop Clock state.

- SLC90E46 waits for Stop Break or Burst Event to occur.

To Leave Stop Clock State

Invoke State Transition

- A Stop Break or Burst Event occurs.

SLC90E46 Actions (In Sequence)

- SLC90E46 deasserts nCPU_STP to the Clock Synthesizer to start the host clocks.
- SLC90E46 loads the Fast Burst Timer with the [CPU_LCK] value and then count downs to wait for the processor PLL to start and lock.
- SLC90E46 deasserts nSUS_STAT1 after the Fast Burst Timer expires.
  - SLC90E42 switches from Suspend Refresh to Normal Refresh after the de-assertion of nSUS_STAT1.
- SLC90E46 deasserts ZZ at least 2 PCI clocks before the deassertion of nSTPCLK.
- SLC90E46 waits 2 - 32Khz clock periods after the deassertion of nSUS_STAT1 to deassert nSTPCLK.

Result of the SLC90E46 Operation

- Processor returns to the On state and resume normal operation.
  - SLC90E42 PCI Arbiter still remains in disabled state. Bus Master request must be trapped to generate nSMI, which will invoke power management software to enable PCI Arbiter. Device 8 Peripheral Device Monitor can be used for that purpose.

11.1.3. PCI Clock Control

The SLC90E46 follows the nCLKRUN protocol as specified by the PCI Mobile Design Guide to manage the PCI Clock. The SLC90E46 is the Central Resources of the nCLKRUN protocol.

If the [CLKRUN_EN] bit is set in the Processor Control Register, the SLC90E46 will request to stop the PCI clock if the bus has been idle for 26 PCI clocks. The SLC90E46 will drive the PCI nCLKRUN signal HIGH for four clocks. If no other device in the system against the request to stop before the 5th PCI clocks, then SLC90E46 will assert nPCI_STP signal to the Clock Synthesizer to gate the PCI clocks to the system. The SLC90E46 should always receive a PCI clock even after the clocks has been stopped to the rest of the system. The clock synthesizer must have one non-gated PCI clock signal routed to the SLC90E46. The clock synthesizer must follow the following timing diagrams for stopping and starting the PCI clocks.

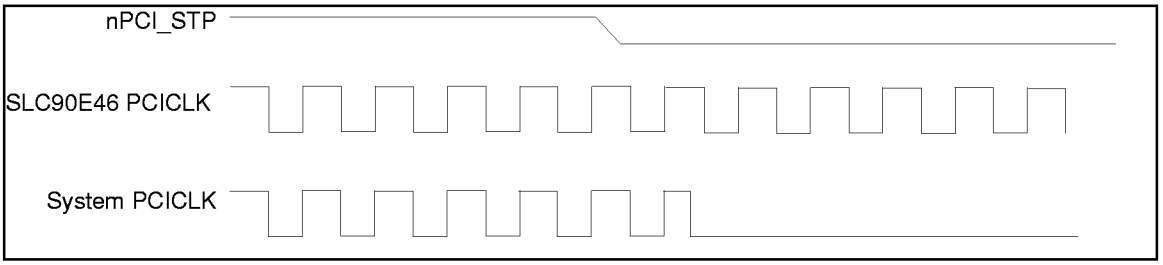


FIGURE 6 - PCI CLOCK STOP TIMING

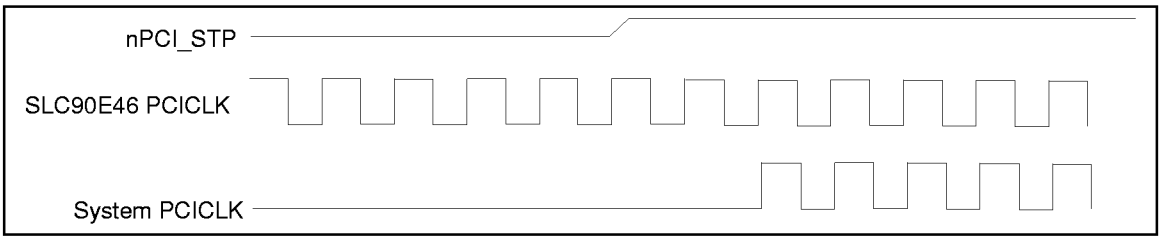


FIGURE 7 - PCI CLOCK START TIMING

11.2. Peripheral Device Management

The Peripheral Device Management mechanisms provide means to detect idle peripheral devices and to trap accesses to peripheral devices that have been powered-down. Enabled device activities can also reload the Global Standby Timer or can generate a Burst or Stop Break event. Device accesses, either I/O or Memory, are monitored from the PCI bus. There are 14 independent device monitors, each capable of detecting activity for a different type of device.

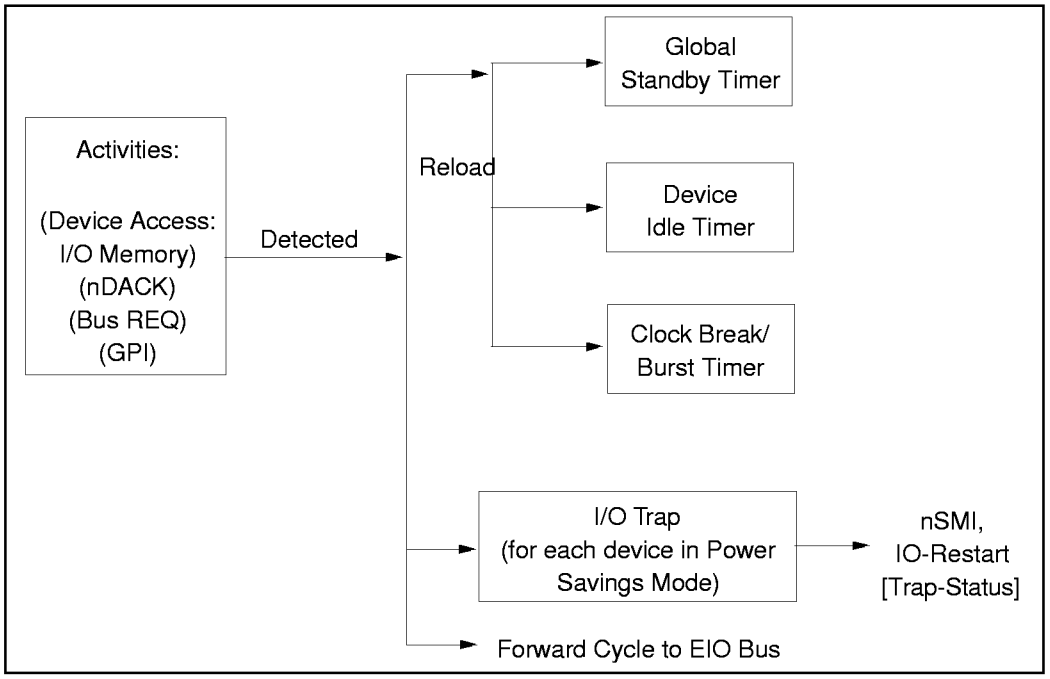


FIGURE 8 - PERIPHERAL DEVICE MANAGEMENT

11.2.1. Device Monitor and Idle Timer

Each device has an Idle Timer that can be reloaded by activity on that device. Activity monitoring is specific to each device and can include the following:

- **Device Access**. Specific I/O or memory ranges associated with that device are monitored on the PCI bus. Many devices have multiple options to set up a wide range of system configurations.
- **DMA Acknowledge.** nDACK used for DMA transfers by the device, such as Audio, Floppy, and LPT.
- **General Purpose Input.** Most device monitor can watch for assertion of a specific General Purpose Input (GPI) pin. Each GPI signal can have its assertion polarity modified to be high or low. Two GPI signals (device 12 and 13) can also be enabled for edge transition detection.
- **System Activity.** Miscellaneous activity, such as Keyboard or Mouse interrupt, PCI bus Master activity, or PCI bus utilization (such as nFRAME assertion) may be monitored for specific device.

A device event can be enabled to reload the device's Idle Timer as well as to reload the Global Standby Timer or the Fast or Slow Burst Timers.

Some of the monitors can serve multiple functions. For example, the Device 3 IDE secondary IDE Drive 1 monitor can also be enabled as a programmable Software Timer. The Device 8 LPT monitor can be enabled to monitor parallel port activity or PCI Bus Master activity.

When the Idle Timer expires due to no detected activity, an Idle Status bit is set and an nSMI is generated if enabled. The power management software can then put the device into a power managed state. The idle timers stop counting when the [SM_FREEZE] bit is set. This can be used to keep the idle timers from counting down when the system is executing an SMI routine.

11.2.2. Device Trap

Each device monitor can enable an IO Trap so that when software makes an access to the enabled I/O or memory range a trap status bit is set and an nSMI is generated if enabled. The device trap feature normally is enabled for devices which have been switched to power down state so that when the power-down device's address ranges are decoded software can be invoked (via nSMI) to restore the device to normal working state.

The I/O Trap nSMI is synchronous to the completion of the I/O instruction. The I/O instruction is completed when nBRDY is returned to the processor. SLC90E46 will coordinate the assertion of nSMI to the processor with the generation of nBRDY to the processor form the Host Bridge chip such that nSMI is asserted at least 3 HCLKs before nBRDY is asserted. This will allow the processor to perform an IO restart cycle.

If the device to be trapped is a PCI device, the SLC90E46 must be enabled to claim the cycle so that nSMI can be generated synchronously. The SLC90E46 should be programmed to send the I/O access cycle to the ISA bus where it will be terminated normally (but the read cycle will return unknown data).

11.2.3. Peripheral Device Management

Following is a brief description of the power management process for peripheral devices:

Initialization

The software initializes the device's I/O address range and the Idle Timer counter for each peripheral device.

Normal to Low Power State Transition

When power management software enables the Idle Timer for a device, the Idle Timer starts to count down. Any detected activity of the enabled device will reload its Idle Timer. When the Idle Timer expires, the associated idle status bit is set, and an nSMI is generated. The SMI handler can identify the device from the idle status bit, then put the peripheral device into a low power state, disable the Idle Timer and enable the I/O Trap mechanism for the device.

Low Power to Normal State Transition

When the system performs an access to an I/O Trap enabled device range, the access is trapped, an nSMI is generated, and the corresponding I/O Trap SMI status bit is set. The SMI handler can identify the device by examining the I/O Trap SMI status bits, restore the peripheral device to "on" state, clear the Trap SMI status bits, and enable the Idle Timer hardware. The processor will then issue an I/O restart to access the device again.

11.2.4. PCI/ISA Peripheral Devices

The Device Activity Monitor is watching cycles on the PCI bus to generate activity events. The device monitors also can be enabled to forward cycles which address the device's enabled address ranges to the ISA bus. Devices which reside on the ISA bus must have both address ranges selected and enabled and the ISA/EIO forwarding enabled.

The following table summarizes peripheral devices which are monitored by the SLC90E46 Power Management function.

	MONITORED DEVICE ACTIVITIES			TIMER AFFECTED			
PERIPHERAL DEVICE	ADDRESS RANGES	nDACK	GPI	IDLE TIMER	GLOBAL STANDBY	FAST BURST	SLOW BURST
0. Primary IDE Drive 0	1F0h - 1F7h 3F6h	IDE nPDDACK		CNT-A	x		x
1. Primary IDE Drive 1	1F0h-1F7h 3F6h	IDE nPDDACK	GPI5	CNT-A	x	x	x
2. Secondary IDE Drive 0	170h - 177h 376h	IDE nSDDACK	GPI6	CNT-A	x	x	x
3. Secondary IDE Drive 1 / Software SMI Timer	170h - 177h 376h	IDE nSDDACK	GPI0	SWCNT	x	x	x
4. Audio	300h-303h MIDI 310h-313h MIDI 320h-323h MIDI 330h-333h MIDI 200h-207h GAME 388h-38Bh ADLIB 220h-233h SB8/16 240h-253h SB8/16 260h-273h SB8/16 280h-293h SB8/16 530h-537h MSS 604h-60Bh MSS E80h-E87h MSS F40h-F47h MSS	any or all: nDACK[x], x=0,1,3,5,6,7	GPI13	CNT-B	x	x	
5. FDD	3F0h-3F5h, 3F7h 370h-375h, 3F7h	nDACK2	GPI14	CNT-B	x	x	x
6. Serial Port A (Modem)	3F8h-3FFh COM1 2F8h-2FFh COM2 3E8h-3EFh COM3 2E8h-2EFh COM4 220h-227h 228h-22Fh 238h-23Fh 338h-33Fh		GPI15	CNT-B	x	x	
7. Serial Port B (IR)	3F8h-3FFh COM1 2F8h-2FFh COM2 3E8h-3EFh COM3 2E8h-2EFh COM4 220h-227h 228h-22Fh 238h-23Fh 338h-33Fh		GPI16	CNT-B	x	x	

	MONITORED DEVICE ACTIVITIES			TIMER AFFECTED			
PERIPHERAL DEVICE	ADDRESS RANGES	nDACK	GPI	IDLE TIMER	GLOBAL STANDBY	FAST BURST	SLOW BURST
8A. LPT	LPT_DEC_SEL: 0,0=3BCh-3BFh, 7BCh-7BEh 0,1=378h-37Fh, 778h-77Ah 1,0=278h-27Fh, 678h-67Ah	one of: nDACK[x] x=0,1,3	GPI17	BM_CNT	x	x	
8B. Bus Master Activity		nPCIREQ [A-D], nPHOLD		Dev8 Timer	x	x	
9. Generic IO Range 0	16-byte IO range		GPI4	CNT-C	x	x	
10. Generic IO Range 1	16-byte IO range		GPI18	CNT-C	x	x	
11. User Interface: Graphics, Keyboard, Mouse, PCI Utilization	1M to 8M Mem range. A0000h-BFFFFh, 3B0h-3DFh VGA, 60h, 64h, IRQ0, IRQ12/M		GPI19	CNT-D	x	x	
12. Cardbus 0	16-byte I/O range, 32K-4M Mem range		GPI20		x	x	
13. Cardbus 1	16-byte I/O range, 32K-4M Mem range		GPI21		x	x	

11.2.5. Device Specific Details

This section gives detailed descriptions for the 14 device monitors. For each device monitor, the system events which can cause actions such as timer reloads or IO traps are listed. The names of register bits which are programmed to enable power management resources or status bits set when events occur are shown in brackets for each device.

11.2.5.1. Device 0: IDE Primary Drive 0

Device 0 monitors the primary IDE device, drive 0. The IDE device DRV bit (bit 4 of port 1F6h) is shadowed to determine if drive 0 is active on the primary connector.

Device 0 System Events

- PCI accesses to IO address 1F0h-1F7h, 3F6h, independent of whether IDE is enabled in PCI function 1, if IDE drive 0 is active. This allows monitoring of devices on PCI or ISA bus.
  Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion
- nPDDACK assertion if primary IDE drive 0 is active and BMIDE is active for primary connector.
  Effect: Reload idle, burst, or global standby timer.
- No GPI events associated with device 0.

Device 0 Idle Timer

• Resolution: 1 or 8 second	Control Bit: [IDL_SEL_DEV0]
• Timer count: 4 bit	Register Bit: [IDL_CNTA]
• Enable:	Control Bit: [IDL_EN_DEV0]
• Expiration nSMI Assertion	Control Bit: [IDL_EN_DEV0]
	Status Bit: [IDL_STS_DEV0]

Global Standby Timer Reload:

• Enable:	Control Bit: [GRLD_EN_DEV0]

Burst Timer Reload (only Slow burst)

• Enable:	Control Bit: [BRLD_EN_DEV0]

IO Trap nSMI:

• Enable:	Control Bit: [TRP_EN_DEV0]
	Status Bit: [TRP_STS_DEV0]

11.2.5.2. Device 1: IDE Primary Drive 1

Device 1 monitors the primary IDE device, drive 1 and GPI5. The IDE device DRV bit (bit 4 of port 1F6h) is shadowed to determine if drive 1 is active on the primary connector.

Device 1 System Events

- PCI accesses to IO address 1F0h-1F7h, 3F6h, independent of whether IDE is enabled in PCI function 1, if IDE drive 1 is active. This allows monitoring of devices on PCI or ISA bus.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion

- nPDDACK assertion if primary IDE drive 1 is active, the IDE interface is configured as primary and secondary and BMIDE is active for primary connector.

Effect: Reload idle, burst, or global standby timer.

- Assertion of GPI5. The polarity of active signal (high or low) is selectable.
  Effect: Reload idle, burst, or global standby timer, or IO Trap nSMI assertion.

Device 1 GPI5 Enable:

• Enable	Control Bit: [GPI_EN_DEV1]
• Polarity Selection	Control Bit: [GPI_POL_DEV1]

Device 1 Idle Timer:

• Resolution: 1 or 8 second	Control Bit: [IDL_SEL_DEV1]
• Timer count: 4 bit	Register Bit: [IDL_CNTA]
• Enable/Reload:	Control Bit: [IDL_EN_DEV1]

- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV1]; Status Bit: [IDL_STS_DEV1]

Global Standby Timer Reload:
- Enable — Control Bit: [GRLD_EN_DEV1]

Burst Timer Reload:
- Enable — Control Bit: [BRLD_EN_DEV1]
- Fast or Slow Burst Select — Control Bit: [BRLD_SEL_DEV1]

IO Trap nSMI:
- Enable — Control Bit: [TRP_EN_DEV1]; Status Bit: [TRP_STS_DEV1]

11.2.5.3. Device 2: IDE Secondary Drive 0

Device 2 monitors the Secondary IDE device, drive 0 and GPI6. The IDE device DRV bit (bit 4 of port 176h) is shadowed to determine if drive 0 is active on the secondary connector.

Device 2 System Events
- PCI accesses to IO address 170h-177h, 376h, independent of whether IDE is enabled in PCI function 1, if secondary IDE drive 0 is active. This allows monitoring of devices on PCI or ISA bus.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion
- nSDDACK assertion if secondary IDE drive 0 is active, the IDE interface is configured as primary and secondary and BMIDE is active for secondary connector.

Effect: Reload idle, burst, or global standby timer.
- Assertion of GPI6. The polarity of active signal (high or low) is selectable.
  Effect: Reload idle, burst, or global standby timer, or IO Trap nSMI assertion.

DEVICE 2 GPI6 Enable:
- Enable — Control Bit: [GPI_EN_DEV2]
- Polarity Selection — Control Bit: [GPI_POL_DEV2]

DEVICE 2 Idle Timer:
- Resolution: 1 or 8 second — Control Bit: [IDL_SEL_DEV2]
- Timer count: 4 bit — Register Bit: [IDL_CNTA]
- Enable/Reload: — Control Bit: [IDL_EN_DEV2]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV2]; Status Bit: [IDL_STS_DEV2]

Global Standby Timer Reload:
- Enable — Control Bit: [GRLD_EN_DEV2]

Burst Timer Reload:
- Enable — Control Bit: [BRLD_EN_DEV2]
- Fast or Slow Burst Select — Control Bit: [BRLD_SEL_DEV2]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV2]; Status Bit: [TRP_STS_DEV2]

11.2.5.4. DEVICE 3: IDE Secondary Drive 1

DEVICE 3 monitors the Secondary IDE device, drive 1 and GPI0. The IDE device DRV bit (bit 4 of port 176h) is shadowed to determine if drive 1 is active on the secondary connector. Device 3 can also be used as a Software nSMI Timer. It has a configuration bit to disable the Idle Timer Reload so that the timer can be allowed to expire based only on the timer count.

DEVICE 3 System Events

- PCI accesses to IO address 170h-177h, 376h, independent of whether IDE is enabled in PCI function 1, if secondary IDE drive 1 is active. This allows monitoring of devices on PCI or ISA bus.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion

- nSDDACK assertion if secondary IDE drive 1 is active, the IDE interface is configured as primary and secondary and BMIDE is active for secondary connector.

Effect: Reload idle, burst, or global standby timer.

- Assertion of GPI0. The polarity of active signal (high or low) is selectable.
  Effect: Reload idle, burst, or global standby timer, or IO Trap nSMI assertion.

DEVICE 3 GPI0 Enable:

- Enable — Control Bit: [GPI_EN_DEV3]
- Polarity Selection — Control Bit: [GPI_POL_DEV3]

DEVICE 3 Idle Timer:

- Resolution: 1 ms or 8 second — Control Bit: [IDL_SEL_DEV3]
- Timer count: 4 bit — Register Bit: [SW_CNT]
- Enable/Reload: — Control Bit: [IDL_EN_DEV3]
- Reload Disable (to select SW func.): — Control Bit: [IDL_RLD_EN_DEV3]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV3]; Status Bit: [IDL_STS_DEV3]

Global Standby Timer Reload:

- Enable — Control Bit: [GRLD_EN_DEV3]

Burst Timer Reload:

- Enable — Control Bit: [BRLD_EN_DEV3]
- Fast or Slow Burst Select — Control Bit: [BRLD_SEL_DEV3]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV3]; Status Bit: [TRP_STS_DEV3]

11.2.5.5. DEVICE 4: Audio

Device 4 monitors an audio subsystem and GPI13. The available address ranges cover the following type of audio devices: 8/16 bit Sound Blaster, standard Game Port, ADLIB music synthesizer, Microsoft Sound System, and MIDI. The actual address ranges selectable for each type is shown below.

DEVICE 4 System Events

- PCI accesses to any of the enabled IO addresses.

Effect: Reload idle, burst, or global standby timer, IO trap nSMI assertion, or forward the cycle from PCI to ISA.

- nDACKx assertion (x=0,1,3,5,6,7) if enabled.

Effect: Reload idle, burst, or global standby timer.

- Assertion of GPI13. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer.

DEVICE 4 GPI13 Enable:

- Enable — Control Bit: [GPI_EN_DEV4]
- Polarity Selection — Control Bit: [GPI_POL_DEV4]

DEVICE 4 Address Ranges:

- Sound Blaster — Control Bit: [SB_EN]; Selection Bits: [SB_SEL]; 220h-22Fh, 230h-233h, OR 240h-24Fh, 250h-253h, OR 260h-26Fh, 270h-273h, OR 280h-28Fh, 290h-293h
- Game Port — Control Bit: [SB_EN]; 200h-207h
- ADLIB Synthesizer — Control Bit: [SB_EN]; 388h-38Bh
- Microsoft Sound System: Control Bit: [MSS_EN]; Selection Bits: [MSS_SEL]; 530h-537h OR 604h-60Bh OR E80h-E87h OR F40h-F47h
- MIDI — Control Bit: [MIDI_EN]; Selection Bits: [MIDI_SEL]; 300h-303h OR 310h-313h OR 320h-323h OR 330h-333h

DEVICE 4 ISA Forwarding Enable:

- MIDI — Control Bit: [MIDI_EIO_EN]
- MSS — Control Bit: [MSS_EIO_EN]
- Game — Control Bit: [GAME_EIO_EN]
- Sound Blaster — Control Bit: [SB_EIO_EN]

DEVICE 4 nDACKx (x=0,1,3,5,6,7)

- Enable: Control Bit: [DACKx_EN_DEV4]

DEVICE 4 Idle Timer:

- Resolution: 1 second
- Timer count: 5 bit Register Bit: [IDL_CNTB]
- Enable/Reload: Control Bit: [IDL_EN_DEV4]
- Expiration nSMI Assertion Control Bit: [IDL_EN_DEV4]
  Status Bit: [IDL_STS_DEV4]

Global Standby Timer Reload:

- Enable Control Bit: [GRLD_EN_DEV4]

Burst Timer Reload (Fast Bursts Only):

- Enable Control Bit: [BRLD_EN_DEV4]

IO Trap nSMI:

- Enable Control Bit: [TRP_EN_DEV4]
  Status Bit: [TRP_STS_DEV4]

11.2.5.6. DEVICE 5: Floppy Disk Drive

Device 5 monitors accesses to Floppy Drive Controller or GPI14.

DEVICE 5 System Events

- PCI accesses to IO addresses for the floppy drive, selectable below.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion, or forwarding of the cycle from PCI to ISA.

- nDACK2 assertion if enabled.

Effect: Reload idle, burst, or global standby timer.

- Assertion of GPI14. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer.

DEVICE 5 GPI14 Enable:

- Enable Control Bit: [GPI_EN_DEV5]
- Polarity Selection Control Bit: [GPI_POL_DEV5]

DEVICE 5 Address Ranges:

- Floppy Drive: Control Bit: [FDC_MON_EN]
  Selection Bits: [FDC_DEC_SEL]
  3F0h-3F5h, 3F7h OR 370h-375h, 377h

DEVICE 5 ISA Forwarding Enable: Control Bit: [EIO_EN_DEV5]

DEVICE 5 nDACK2 Enable: Control Bit: [RES_EN_DEV5]

DEVICE 5 Idle Timer:

- Resolution: 1 second
- Timer count: 5 bit Register Bit: [IDL_CNTB]

- Enable/Reload: Control Bit: [IDL_EN_DEV5]
- Expiration nSMI Assertion Control Bit: [IDL_EN_DEV5]
  Status Bit: [IDL_STS_DEV5]

Global Standby Timer Reload:
- Enable Control Bit: [GRLD_EN_DEV5]

Burst Timer Reload:
- Enable Control Bit: [BRLD_EN_DEV5]
- Fast or Slow Burst Select Selection Bit: [BRLD_SEL_DEV5]

IO Trap nSMI:
- Enable Control Bit: [TRP_EN_DEV5]
  Status Bit: [TRP_STS_DEV5]

11.2.5.7. DEVICE 6: Serial Port A

Device 6 monitors accesses to Serial Port A or GPI15. Device 7 also monitors serial port resources. This gives the capability to monitor 2 separate serial ports in a system.

DEVICE 6 System Events
- PCI accesses to IO addresses for a serial port, selectable below.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion, or forwarding of the cycle from PCI to ISA.
- Assertion of GPI15. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer.

DEVICE 6 GPI15 Enable:
- Enable Control Bit: [GPI_EN_DEV6]
- Polarity Selection Control Bit: [GPI_POL_DEV6]

DEVICE 6 Address Ranges:
- Serial Port A: Control Bit: [SA_MON_EN]
  Selection Bit: [COMA_DEC_SEL]
  3F8h-3FFh, or
  2F8h-2FFh, or
  220h-227h, or
  228h-22Fh, or
  238h-23Fh, or
  2E8h-2EFh, or
  338h-33Fh, or
  3E8h-3EFh

DEVICE 6 ISA Forwarding Enable: Control Bit: [EIO_EN_DEV6]

DEVICE 6 Idle Timer:

- Resolution: 1 second
- Timer count: 5 bit — Register Bit: [IDL_CNTB]
- Enable/Reload: — Control Bit: [IDL_EN_DEV6]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV6]; Status Bit: [IDL_STS_DEV6]

Global Standby Timer Reload:

- Enable — Control Bit: [GRLD_EN_DEV6]

Burst Timer Reload (Fast Burst Only):

- Enable — Control Bit: [BRLD_EN_DEV6]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV6]; Status Bit: [TRP_STS_DEV6]

11.2.5.8. DEVICE 7: Serial Port B

DEVICE 7 monitors accesses Serial Port B or GPI16. Device 7 also monitors serial port resources. This gives the capability to monitor 2 separate serial ports in a system.

DEVICE 7 System Events

- PCI accesses to IO addresses for a serial port, selectable below.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion, or forwarding of the cycle from PCI to ISA.

- Assertion of GPI16. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer.

DEVICE 7 GPI16 Enable:

- Enable — Control Bit: [GPI_EN_DEV7]
- Polarity Selection — Control Bit: [GPI_POL_DEV7]

DEVICE 7 Address Ranges:

- Serial Port B: — Control Bit: [SA_MON_EN]; Selection Bits: [COMB_DEC_SEL]
  3F8h-3FFh, or
  2F8h-2FFh, or
  220h-227h, or
  228h-22Fh, or
  238h-23Fh, or
  2E8h-2EFh, or
  338h-33Fh, or
  3E8h-3EFh

DEVICE 7 ISA Forwarding Enable: — Control Bit: [EIO_EN_DEV7]

DEVICE 7 Idle Timer:

- Resolution: 1 second

- Timer count: 5 bit — Register Bit: [IDL_CNTB]
- Enable/Reload: — Control Bit: [IDL_EN_DEV7]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV7]; Status Bit: [IDL_STS_DEV7]

Global Standby Timer Reload:
- Enable — Control Bit: [GRLD_EN_DEV7]

Burst Timer Reload (Fast Burst Only):
- Enable — Control Bit: [BRLD_EN_DEV7]

IO Trap nSMI:
- Enable — Control Bit: [TRP_EN_DEV7]; Status Bit: [TRP_STS_DEV7]

11.2.5.9. DEVICE 8: LPT (Parallel Port)

Device 8 monitors accesses to Parallel Port or GPI17. It can also be used to monitor PCI Bus Master activity.

DEVICE 8 System Events
- PCI accesses to IO addresses for a parallel port, selectable below.

Effect: Reload idle, burst, or global standby timer or IO trap nSMI assertion, or forwarding of the cycle from PCI to ISA.
- Assertion of GPI17. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer.
- Assertion of PCIREQ[0-3] or nPHOLD, signifying PCI Master activity.
  Effect: Reload idle, burst, or global standby timer, or IO Trap nSMI. The Bus Master activity can be programmed to cause a IO Trap nSMI independent of IO address accesses.

DEVICE 8 GPI17 Enable:
- Enable — Control Bit: [GPI_EN_DEV8]
- Polarity Selection — Control Bit: [GPI_POL_DEV8]

DEVICE 8 Address Ranges:
- LPT (Parallel Port): — Control Bit: [LPT_MON_EN]; Selection Bits: [LPT_DEC_SEL]; 378-37Fh, 778-77Ah OR 278-27Fh, 678-67Ah OR 3BC-3BFh, 7BC-7BEh

DEVICE 8 nDACKx Enable: — Control Bit: [RES_EN_DEV8]
- nDACKx Select (x=0, 1, or 3) — Selection Bits: [LPT_DMA_SEL]

DEVICE 8 ISA Forwarding Enable: — Control Bit: [EIO_EN_DEV8]

DEVICE 8 Idle Timer:
- Resolution: 1msec or 1 second — Selection Bits: [IDL_SEL_DEV8]
- Timer count: 5 bit — Register Bits: [BM_CNT]

- Enable/Reload: Control Bit: [IDL_EN_DEV8]
- Expiration nSMI Assertion Control Bit: [IDL_EN_DEV8]
  Status Bit: [IDL_STS_DEV8]

Global Standby Timer Reload:
- Enable Control Bit: [GRLD_EN_DEV8]

Burst Timer Reload (Fast Burst Only):
- Addr. Decode, DACK, and GPI Control Bit: [BRLD_EN_DEV8]
- Above and Bus Master Events Control Bit: [BM_RLD_DEV8]
- Bus Master Events Only Control Bit: [BRLD_EN_BM]

IO Trap nSMI:
- LPT or GPI Only Control Bit: [TRP_EN_DEV8]
  Status Bit: [TRP_STS_DEV8]
- Bus Master (PCIRQ) Only Control Bit: [BM_TRP_EN]
  Status Bit: [BM_STS]

11.2.5.10. DEVICE 9: Generic I/O Device 0

Device 9 monitors a device on the PCI bus with a programmable IO address or GPI4.

DEVICE 9 System Events
- PCI accesses to programmable IO addresses, selectable below.

Effect: Reload idle, burst, or global standby timer**;** IO trap nSMI assertion; Forwarding of the cycle from PCI to ISA; Optionally generate a Chip Select signal: nPCS0.
- Assertion of GPI4. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer, NO IO Trap nSMI assertion.

DEVICE 9 GPI4 Enable:
- Enable Control Bit: [GPI_EN_DEV9]
- Polarity Selection Control Bit: [GPI_POL_DEV9]

DEVICE 9 Address Ranges:
- Enable: Control Bit: [GDEC_MON_DEV9]
- Programmable Base Address (16 bit) Register Bits: [BASE_DEV9]
- Programmable Mask (4 bit) Register Bits: [MASK_DEV9]
  - allows 1 to 16 bytes range

DEVICE 9 ISA Forwarding Enable: Control Bit: [EIO_EN_DEV9]

DEVICE 9 Chip Select (nPCS0) Enable: Control Bit: [CS_EN_DEV9]

DEVICE 9 Idle Timer:
- Resolution: 1 second
- Timer count: 5 bit Register Bit: [IDL_CNTC]
- Enable/Reload: Control Bit: [IDL_EN_DEV9]
- Expiration nSMI Assertion Control Bit: [IDL_EN_DEV9]
  Status Bit: [IDL_STS_DEV9]

Global Standby Timer Reload:
- Enable Control Bit: [GRLD_EN_DEV9]

Burst Timer Reload (Fast Burst Only):

- Enable — Control Bit: [BRLD_EN_DEV9]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV9]; Status Bit: [TRP_STS_DEV9]

11.2.5.11. DEVICE 10: Generic I/O Device 1

Device 10 monitors a device on the PCI bus with a programmable IO address or GPI18.

DEVICE 10 System Events

- PCI accesses to programmable IO addresses, selectable below.

Effect: Reload idle, burst, or global standby timer**;** IO trap nSMI assertion; Forwarding of the cycle from PCI to ISA.; Optionally generate a Chip Select signal: nPCS1.

- Assertion of GPI18. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer, NO IO Trap nSMI assertion.

DEVICE 10 GPI18 Enable:

- Enable — Control Bit: [GPI_EN_DEV10]
- Polarity Selection — Control Bit: [GPI_POL_DEV10]

DEVICE 10 Address Ranges:

- Enable: — Control Bit: [GDEC_MON_DEV10]
- Programmable Base Address (16 bit) — Register Bits: [BASE_DEV10]
- Programmable Mask (4 bit) — Register Bits: [MASK_DEV10] - allows 1 to 16 bytes range

DEVICE 10 ISA Forwarding Enable: Control Bit: [EIO_EN_DEV10]

DEVICE 10 Chip Select (nPCS1) Enable: Control Bit: [CS_EN_DEV10]

DEVICE 10 Idle Timer:

- Resolution: 1 second
- Timer count: 5 bit — Register Bit: [IDL_CNTC]
- Enable/Reload: — Control Bit: [IDL_EN_DEV10]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV10]; Status Bit: [IDL_STS_DEV10]

Global Standby Timer Reload:

- Enable — Control Bit: [GRLD_EN_DEV10]

Burst Timer Reload (Fast Burst Only):

- Enable — Control Bit: [BRLD_EN_DEV10]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV10]; Status Bit: [TRP_STS_DEV10]

11.2.5.12. DEVICE 11: User Interface (Keyboard, Mouse, Video)

Device 11 monitors the system's primary user interfaces, including the keyboard, PS/2 mouse, or the video subsystem. It contains a special logic to monitor the PCI bus utilization in order to detect video activity. This will allow a system to playback video without power managing the video subsystem due to user inactivity (no keyboard or mouse movement).

DEVICE 11 System Events

- PCI accesses to programmable linear frame buffer addresses, selectable below.

Effect: Reload burst timer.

- PCI accesses to VGA I/O addresses (3B0h-3DFh) or the A and B segment video memory ranges (A0000-BFFFFh).

Effect: Reload burst timer.

- PCI accesses to keyboard controller I/O addresses (60h-64h).

Effect: Reload idle, burst or global standby timer; IO Trap nSMI; Forwarding KBC cycles to ISA.

- PCI bus utilization: number of PCI data phases (as measured by nFRAME assertion) exceeds a set limit.

Effect: Reload idle or global standby timer.

- Assertion of IRQ1 or IRQ12/M.

Effect: Reload idle, burst, or global standby timer; IO Trap nSMI.

- Assertion of GPI19. The polarity of active signal (high or low) is selectable.

Effect: Reload idle, burst, or global standby timer; IO Trap nSMI assertion.

DEVICE 11 GPI19 Enable:

- Enable — Control Bit: [GPI_EN_DEV11]
- Polarity Selection — Control Bit: [GPI_POL_DEV11]

DEVICE 11 Linear Frame Buffer Ranges:

- Decode Enable: — Control Bit: [LFB_DEC_EN]
- Programmable Base Address (12 bit) — Register Bits: [LFBASE_DEV11]
- Programmable Mask (2 bit) — Register Bits: [LFMASK_DEV11]
  - allows 1Mbyte to 4Mbytes range.

DEVICE 11 PCI Bus Utilization:

- Enable: — Control Bit: [VIDEO_EN]; Status Bit: [VIDEO_STS]
- Threshold — Register Bits: [BUS_UTIL]
- Percent Active — Register Bits: [%BUS_UTIL]

DEVICE 11 VGA Decode Enable: — Control Bit: [GRAPH_IO_EN]
DEVICE 11 A,B Segment Decode Enable: — Control Bit: [GRAPH_AB_EN]
DEVICE 11 KBC Decode Enable: — Control Bit: [KBC_EN_DEV11]
DEVICE 11 IRQ1 Enable: — Control Bit: [IRQ1_EN_DEV11]
DEVICE 11 IRQ12/M Enable: — Control Bit: [IRQ12_EN_DEV11]
DEVICE 11 ISA Forwarding Enable: — Control Bit: [KBD_EIO_EN]

DEVICE 11 Idle Timer:

- Resolution: 1 second or 1 min — Selection Bit: [IDL_SEL_DEV11]

- Timer count: 5 bits — Register Bit: [IDL_CNTD]
- Enable/Reload: — Control Bit: [IDL_EN_DEV11]
- Expiration nSMI Assertion — Control Bit: [IDL_EN_DEV11]; Status Bit: [IDL_STS_DEV11]

Global Standby Timer Reload:
- Enable — Control Bit: [GRLD_EN_DEV11]

Burst Timer Reload (Fast Burst Only):
- Enable — Control Bit: [BRLD_EN_DEV11]

IO Trap nSMI:
- Enable — Control Bit: [TRP_EN_DEV11]; Status Bit: [TRP_STS_DEV11]

11.2.5.13. DEVICE 12: Cardbus Slot (or Generic I/O and MEM Device)

Device 12 monitors a generic I/O device or Memory device with a programmable IO or memory address or GPI20.

DEVICE 12 System Events:
- PCI accesses to programmable IO addresses and memory addresses, selectable below.

Effect: Reload burst, or global standby timer**.** NO IDLE TIMER ASSOCIATED with DEVICE 12; IO trap nSMI assertion; Forwarding of the cycle from PCI to ISA.
- Assertion of GPI20. The polarity of active signal (high or low) is selectable, or edge-triggered.

Effect: Reload burst or global standby timer, or IO Trap nSMI assertion.

DEVICE 12 GPI20 Enable:
- Enable — Control Bit: [GPI_EN_DEV12]
- Polarity Selection — Control Bit: [GPI_POL_DEV12]
- GPI Edge Select. 0=level, 1=edge — Selection Bit: [GPI_EDG_DEV12]

DEVICE 12 IO Address Ranges:
- Enable: — Control Bit: [IO_EN_DEV12]
- Programmable IO Base Address (16 bit) — Register Bits: [IBASE_DEV12]
- Programmable Mask (4 bit) — Register Bits: [IMASK_DEV12] - allows 1 to 16 bytes range.

DEVICE 12 Memory Address Ranges:
- Enable: — Control Bit: [MEM_EN_DEV12]
- Programmable Base Address (17 bit: AD15-AD31) — Register Bits: [MBASE_DEV12]
- Programmable Mask (7 bit: AD15-AD21) — Register Bits: [MMASK_DEV12] - allows 32KB to 4MB in size.

DEVICE 12 ISA Forwarding Enable: — Control Bit: [EIO_EN_DEV12]

DEVICE 12 Idle Timer: NONE

Global Standby Timer Reload:

- Enable — Control Bit: [GRLD_EN_DEV12]

Burst Timer Reload (Fast Burst Only):

- Enable — Control Bit: [BRLD_EN_DEV12]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV12]
  Status Bit: [TRP_STS_DEV12]

11.2.5.14. DEVICE 13: Cardbus Slot (or Generic I/O and MEM Device)

Device 13 monitors a generic I/O device or Memory device with a programmable IO or memory address or GPI21.

DEVICE 13 System Events

- PCI accesses to programmable IO addresses and memory addresses, selectable below.

Effect: Reload burst, or global standby timer**.** NO IDLE TIMER ASSOCIATED with DEVICE 13; IO trap nSMI assertion; Forwarding of the cycle from PCI to ISA.

- Assertion of GPI21. The polarity of active signal (high or low) is selectable. Or edge-triggered.

Effect: Reload burst or global standby timer, IO Trap nSMI assertion.

DEVICE 13 GPI21 Enable:

- Enable — Control Bit: [GPI_EN_DEV13]
- Polarity Selection — Control Bit: [GPI_POL_DEV13]
- GPI Edge Select. 0=level, 1=edge — Selection Bit: [GPI_EDG_DEV13]

DEVICE 13 IO Address Ranges:

- Enable: — Control Bit: [IO_EN_DEV13]
- Programmable IO Base Address (16 bit) — Register Bits: [IBASE_DEV13]
- Programmable Mask (4 bit) — Register Bits: [IMASK_DEV13]
  - allows 1 to 16 bytes range

DEVICE 13 Memory Address Ranges:

- Enable: — Control Bit: [MEM_EN_DEV13]
- Programmable Base Address (17 bit: AD15-AD31) — Register Bits: [MBASE_DEV13]
- Programmable Mask (7 bit: AD15-AD21) — Register Bits: [MMASK_DEV13]
  - allows 32KB to 4MB in size.

DEVICE 13 ISA Forwarding Enable: — Control Bit: [EIO_EN_DEV13]

DEVICE 13 Idle Timer: NONE

Global Standby Timer Reload:

- Enable — Control Bit: [GRLD_EN_DEV13]

Burst Timer Reload (Fast Burst Only):

- Enable — Control Bit: [BRLD_EN_DEV13]

IO Trap nSMI:

- Enable — Control Bit: [TRP_EN_DEV13]
  Status Bit: [TRP_STS_DEV13]

11.3. Suspend / Resume Control Mechanism

11.3.1. Suspend Modes

The SLC90E46 supports three types of Suspend modes. The SLC90E46 power management function is designed to allow a single system to support multiple suspend modes and to switch between those modes as needed. A suspended system can be resumed by a number of events. It will then return to full operation where it can continue processing or be placed into another suspend mode.

POWER STATE	nRSMRST	nSUS_STAT1	nSUS_STAT2	nSUSA	nSUSB	nSUSC
ON	1	x[1]	1	1	1	1
POS	1	0	0	0	1	1
STR	1	0	0	0	0	1
STD/SOFF	1	0	0	0	0	0
MOFF	0	0	0	0	0	0

Note: nSUS_STAT1 is also used when the system is running. It signals to the North Bridge when to switch between the normal and suspend refresh mode for DRAMs during Stop Clock state. In the Stop Clock state, HCLK is stopped and the North Bridge must run DRAM refresh off the SUSCLK input.

The SLC90E46 controls the system entering the various suspend states through the suspend control signals listed in the above Table. Upon initialization of Suspend, the SLC90E46 will assert nSUS_STAT[1-2], nSUSA, nSUSB and nSUSC signals in a well defined sequence to switch the system into the desired power state. The nSUSA, nSUSB and nSUSC signals can be used to control various power planes in the system. nSUS_STAT1 is a status signal that signals to the North Bridge when to enter or exit a suspend state, or when to enter or exit a stop clock state (when the system is still running). It is normally used to place the DRAM controller into a Suspend Refresh mode of operation. The nSUS_STAT2 signal is a status signal that can be used to indicate to other system devices when to enter or exit a suspend state.

The system is placed into a suspend mode by programming the Power Management Control register. The Suspend Type is first programmed and then the Suspend Enable bit is set. This causes the SLC90E46 to automatically sequences into the programmed suspend mode.

The basic system usage models for the suspend modes are described here, including Power On Suspend (POS), Suspend to RAM (STR), and Suspend to Disk (STD).

11.3.1.1. Power On Suspend (POS) Mode

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive and the SLC90E46 provides control signals and 32Khz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system is due to DRAM Refresh and leakage current of the powered devices.

When the system resumes from POS, SLC90E46 can optionally:

- Resume without resetting the system
- Reset the processor only
- Reset the entire system

When no reset is performed, the SLC90E46 only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. It takes typically 20ms.

11.3.1.2. Suspend to RAM (STR) Mode

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to the Suspend Refresh logic in SLC90E42 as well as RTC and Suspend Well logic in SLC90E46. SLC90E46 provides control signals and 32Khz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes. SLC90E46 will reset the system on resume from STR.

11.3.1.3. Suspend to Disk (STD) Mode

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the SLC90E46.

This state is also called the Soft Off (Soff) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or if the system is rebooted. The SLC90E46 will reset the system on resume from STD.

11.3.1.4. Mechanical Off (Moff) Mode

This is not a suspend state. This is a condition where all power except the RTC battery has been removed from the system. It is typically controlled by a mechanical switch turning off AC power to a power supply. It could be used as a condition in which a mobile system's battery has been removed.

The following table summarizes these models along with their target system power consumption and resume latency.

POWER SAVINGS MODE	POWER MANAGEMENT STRATEGY	SYSTEM TARGET POWER	SYSTEM TARGET RESUME LATENCY
Global Standby	All monitored peripheral devices are powered off, and the processor's clock is stopped.	Variable	Variable
Powered-On-Suspend (POS)	Same as Global Standby, but Power is removed from clock generator.	<250mW	~20ms
Suspend-to-RAM (STR)	Power is removed everywhere in the system, except: Power management section of the SLC90E46, slow refresh logic in the memory controller, graphics chip, and the graphics and DRAM memory.	<20mW	~1 sec.
Suspend-to-Disk/ Soft Off (STD)	Power is removed everywhere except the power management sections of the SLC90E46.	<300 uW	~30 sec.

11.3.2. System Resume Mechanism

The SLC90E46 can resume the system from either a Suspend or Soft Off state. Depending on the suspend state the system is in, different events can be enabled to resume the system. The SLC90E46 suspend resume logic is contained in two power wells: main power well and Suspend well. Those events whose logic in the Suspend well can resume the system from any Suspend or Soft Off state. Those events whose logic in the main power well can only resume the system from the Powered On Suspend state. The following table lists the supported resume events in the four SLC90E46 suspend states.

Upon detection of an enabled resume event, the SLC90E46 will set appropriate status signals and automatically transition its suspend control signals bringing the system into a "full-on" condition. The sequencing is shown in the following System Suspend And Resume Control Signaling section.

Global Standby Timer Resume

During normal operation, the Global Standby Timer is used to monitor for global system activity and is reloaded by system activity events. Upon expiration, it generates an nSMI. When the system is placed in a Suspend Mode, the Global Standby Timer can be used to generate a resume event. The Global Standby Timer supports two different timer resolutions for wake-up times from approximately 30 seconds to 8.5 hours. This can be used to transition the system into a lower power suspend state.

Table 36 - Resume Events Supported in Different Power States

RESUME EVENT (SIGNAL)	CONTOL REGISTER BIT	SUSPEND STATES			
		POS	STR	STD	MOFF
RTC Alarm (IRQ8)*	[RTC_EN]: Bit10 of IO Reg. 02	x	x	x	
SMBus Resume Event (Slave Port Match)	[ALERT_EN]: Bit3 of SM IO Reg. 08 [SLV_EN]: Bit 0 of SM IO Reg. 08 [SHDW1_EN]: Bit 1 of SM IO Reg. 08 [SHDW2_EN]: Bit 2 of SM IO Reg. 08	x	x	x	
Serial A Ring (RI)	[RI_EN]: Bit10 of IO Reg. 0Eh	x	x	x	
Power Button (nPWRBTN)		x	x	x	
External SMI (nEXTSMI)	[EXTSMI_EN]: Bit10 of IO Reg. 20h	x	x	x	
LID (LID) - LID Polarity Selection [LID_POL]: Bit25/IO Reg.28h	[LID_EN]: Bit11 of IO Reg. 0Eh	x	x	x	
GPI1	[GPI_EN]: Bit9 of IO Reg. 0Eh	x	x	x	
GSTBY Timer Expiration	[GSTBY_EN]: Bit8 of IO Reg. 20h	x	x	x	
Interrupt (IRQ 1, 3-15) - Only applied in POS mode	[IRQ_RSM_EN]: Bit11 of IO Reg. 20h	x			
USB	[USB_EN]: Bit 8 of IO Reg. 0Eh	x			

*Note: RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI1, LID, nEXTSMI, or nRI) for the resume functionality.

11.3.3. Suspend and Resume Control Signaling

The SLC90E46 provides various control signals to manage Host and PCI clocks, main memory and video memory refresh, system power plane control, and system reset. It automatically controls the signals required to transition the system between the various power states.

The following figures show the system timings for changing the power states of a system using the standard POS/STR/STD models.

11.3.3.1. Power Well Timing

This timing figure describes the relative transitions for SLC90E46 power supplies.

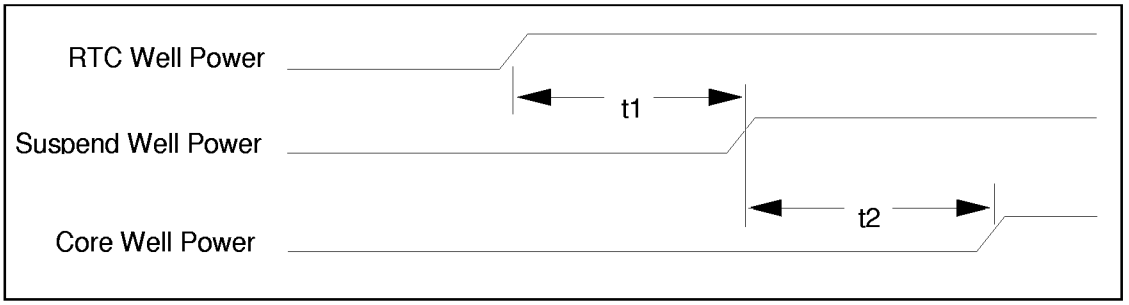


FIGURE 9 - SLC90E46 POWER WELL TIMINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t1	RTC Well Power to Suspend Well Power	0		ns	
t2	Suspend Well Power to Core Well Power	0		ns	

11.3.3.2. nRSMRST and PWROK Timing

This timing figure describes the required timings for SLC90E46 power active status signals.

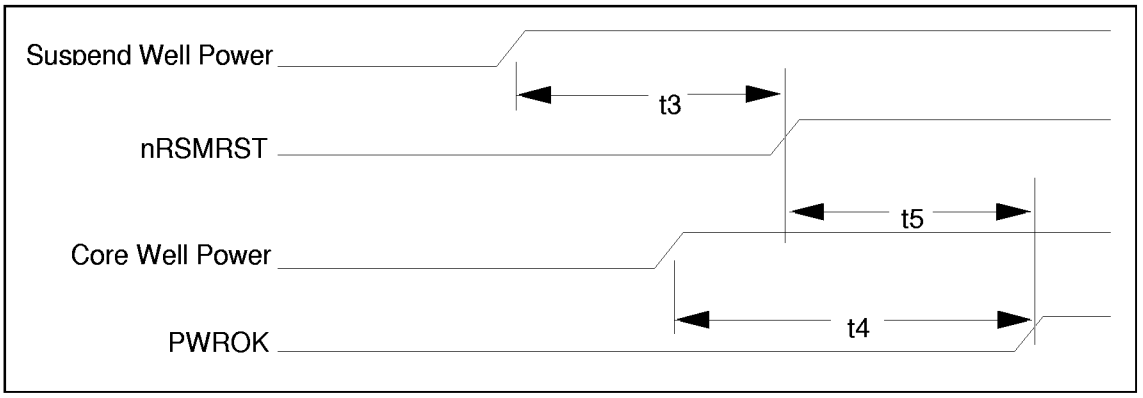


FIGURE 10 - nRSMRST AND PWROK TIMINGS

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t3	Suspend Well Power to nRSMRST Inactive	1		ms	
t4	Core Well Power to PWROK	1		ms	
t5	nRSMRST Inactive to PWROK Active	0		ns	

11.3.3.3. Suspend Well Power and nRSMRST Activated Signals

This timing figure describes the timing relationships for the SLC90E46 power management signals which are powered from the Suspend Power Well. These timings hold independent of the condition of Core Well power or the PWROK signal.

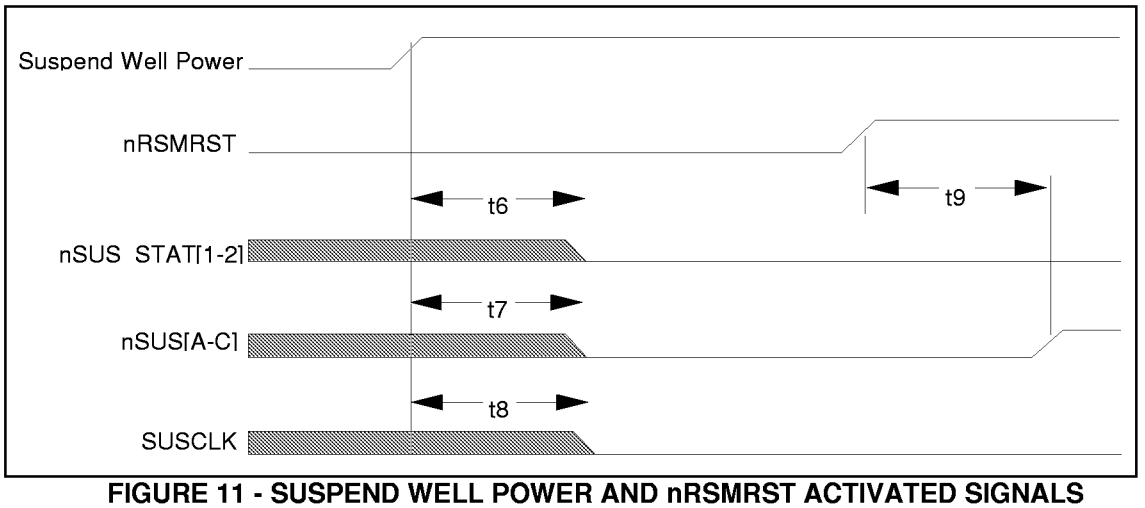


FIGURE 11 - SUSPEND WELL POWER AND nRSMRST ACTIVATED SIGNALS

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t6	Suspend Well Power and nRSMRST Active to nSUS_STAT[1-2] Active		1	RTC	1
t7	Suspend Well Power and nRSMRST Active to nSUS[A-C] Active		1	RTC	1
t8	Suspend Well Power and nRSMRST Active to SUSCLK low		1	RTC	1
t9	nRSMRST inactive to nSUS[A-C] Inactive	1	2	RTC	

Note: These signals are controlled off an internal RTC clock. 1 RTC unit is approximately 32 μs.

11.3.3.4. Core Well Power and PWROK Activated Signals (I)

Core Well Power Applied before nRSMRST Inactive

This timing figure shows the timing relations for Power Management signals powered from the SLC90E46 Main Core well. Here the power active status signals (nRMSRST and PWROK) transition after the application of all power to the SLC90E46. It can be applied to situations where 2 or more of the SLC90E46 power planes are connected together. It also shows timings when nRSMRST and PWROK are connected together.

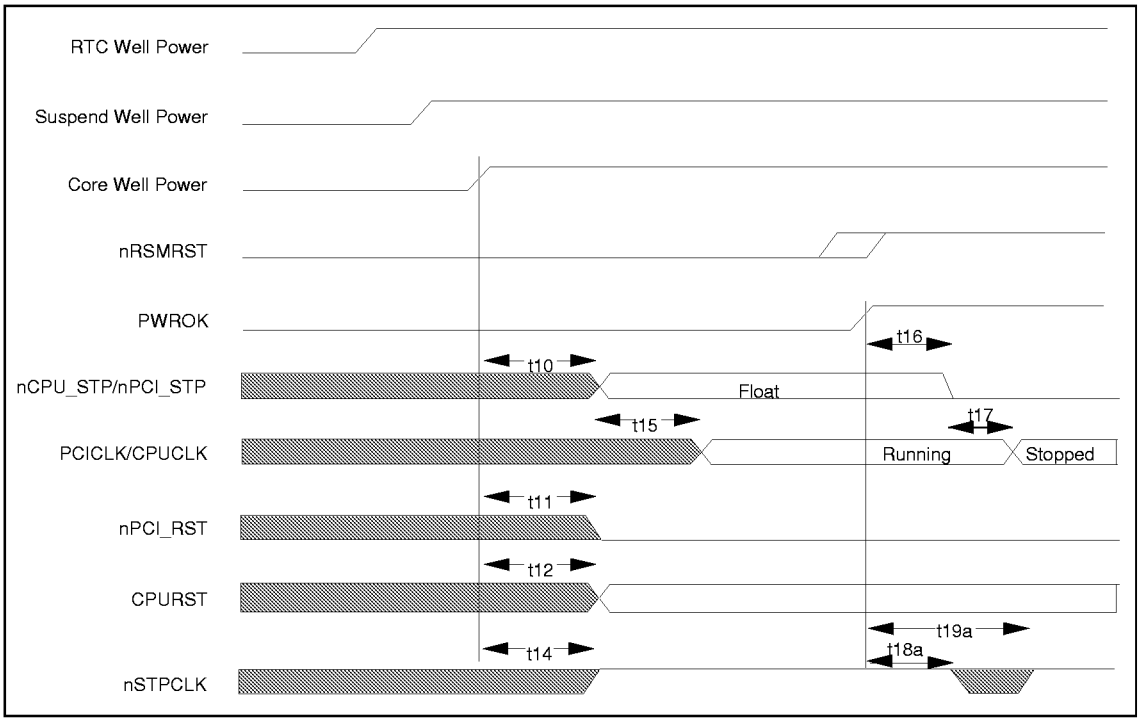


FIGURE 12 - CORE WELL POWER AND PWROK ACTIVATED SIGNALS (CORE WELL POWER APPLIED BEFORE nRSMRST INACTIVE)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t10	Core Well Power Active and PWROK Inactive to nCPU_STP and nPCI_STP Float		1	RTC	1
t11	Core Well Power Active and PWROK Inactive to nPCIRST Active		1	RTC	1
t12	Core Well Power Active and PWROK Inactive to CPURST Active		1	RTC	1
t13	Core Well Power Active and PWROK Inactive to nSLP Inactive		1	RTC	1
t14	Core Well Power Active and PWROK Inactive to nSTPCLK Inactive		1	RTC	1
t15	nCPU_STP and nPCI_STP float to Clocks Running				2
t16	PWROK Active to nCPU_STP and nPCI_STP Active		1	RTC	1
t17	nCPU_STP and nPCI_STP Active to Clocks Stopped				2
t18a	PWROK Active to nSTPCLK Active	0		ns	3
t19a	PWROK Active to nSTPCLK Inactive	1	2	RTC	1, 3

Note 1: These signals are controlled off an internal RTC clock. 1 RTC unit is approximately 32 μs.

Note 2: There are no specific requirements for these timings related to the SLC90E46. As a minimum, the clocks must be available and stable after time t30.

Note 3: These timings depend on the relative timings between nRSMRST and PWROK. If nRSMRST goes inActive 2 RTC periods before PWROK Active, then nSTPCLK will remain inActive. If nRSMRST goes inActive less than 2 RTC periods before PWROK Active, then a Active pulse will be seen on nSTPCLK.

11.3.3.5. Core Well Power and PWROK Activated Signals (II)

nRSMRST Inactive Before Core Well Power Applied

This timing figure shows the timing relations for Power Management signals powered from the SLC90E46 Main Core well. Here the suspend well power Active status signals (nRMSRST) transition before the application of core well power to the SLC90E46.

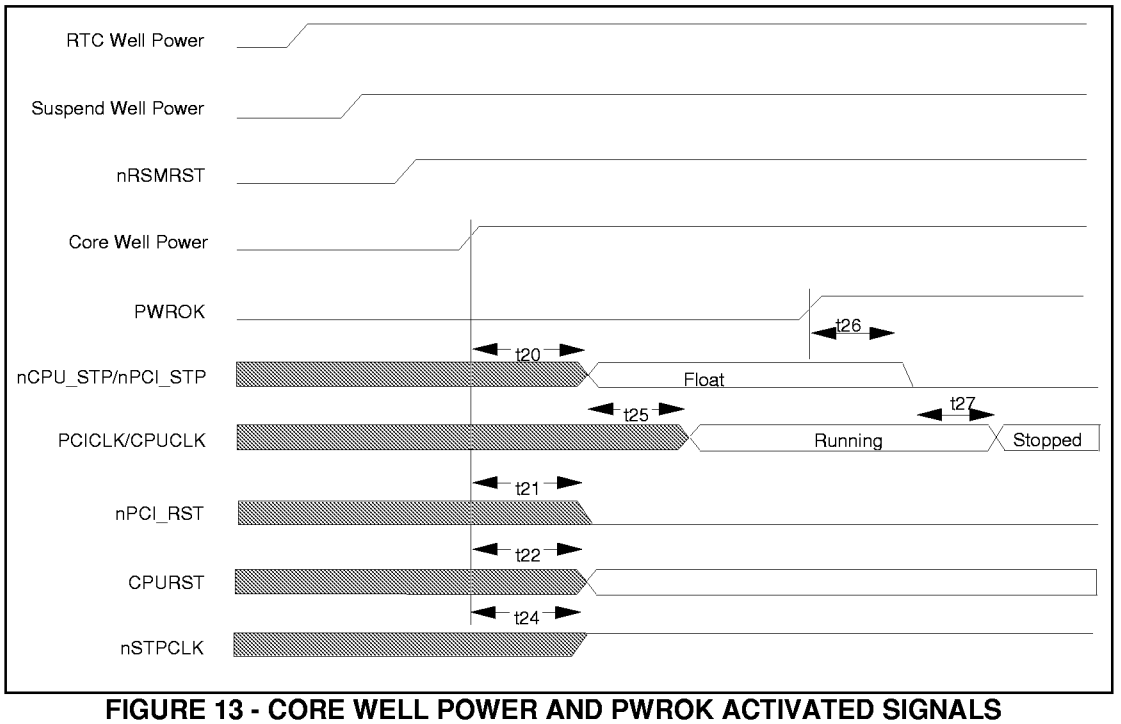


FIGURE 13 - CORE WELL POWER AND PWROK ACTIVATED SIGNALS (nRSMRST INACTIVE BEFORE CORE WELL POWER APPLIED)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t20	Core Well Power Active and PWROK Inactive to nCPU_STP and nPCI_STP Float		1	RTC	1
t21	Core Well Power Active and PWROK Inactive to nPCIRST Active		1	RTC	1
t22	Core Well Power Active and PWROK Inactive to CPURST Active		1	RTC	1
t24	Core Well Power Active and PWROK Inactive to nSTPCLK Inactive		1	RTC	1
t25	nCPU_STP and nPCI_STP Float to Clocks Running				2
t26	PWROK Active to nCPU_STP and nPCI_STP Active		1	RTC	1
t27	nCPU_STP and nPCI_STP Active to Clocks Stopped				2

Note 1: These signals are controlled off an internal RTC clock. 1 RTC unit is approximately 32 µs.
Note 2: There are no specific requirements for these timings related to the SLC90E46. As a minimum, the clocks must be available and stable after time t30.

11.3.3.6. Mechanical Off to On Signal Timing

The timing figure shows the transition from a Mechanical Off condition to the On condition.

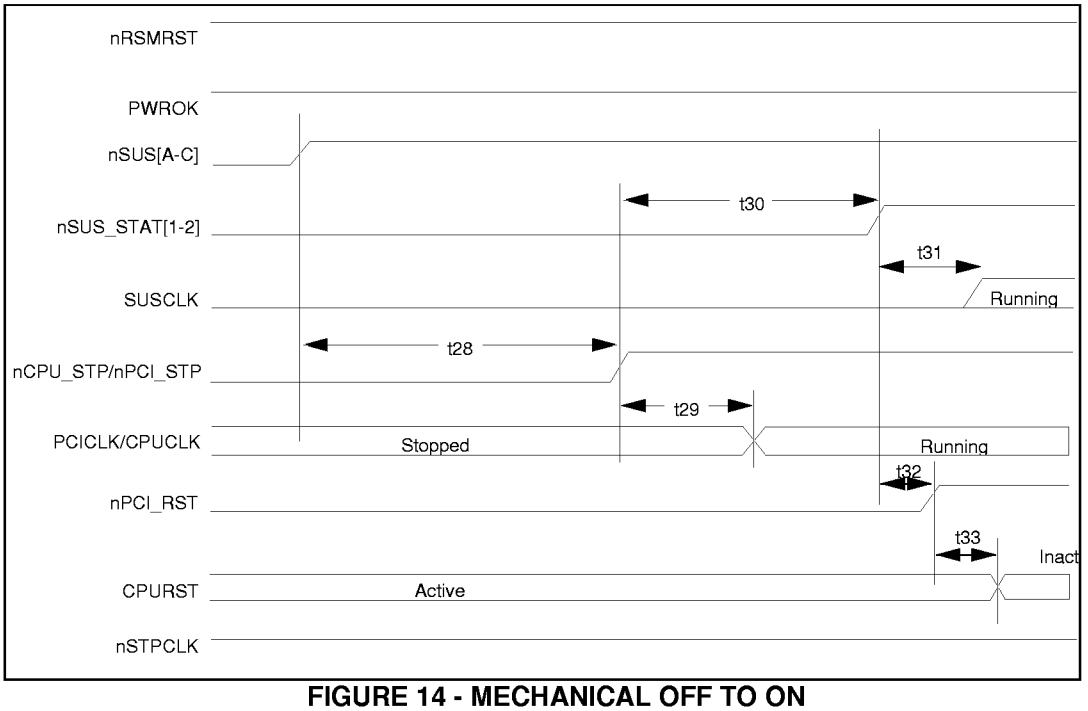


FIGURE 14 - MECHANICAL OFF TO ON

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t28	nSUS[A-C] Inactive to nCPU_STP and nPCI_STP Inactive	16		ms	1
t29	nCPU_STP and nPCI_STP Inactive to Clock Running		2	RTC	2
t30	nCPU_STP and nPCI_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t31	nSUS_STAT[1-2] Inactive to SUSCLK Running		1	RTC	3
t32	nSUS_STAT[1-2] Inactive to nPCI_RST Inactive		1	RTC	3
t33	nPCI_RST Inactive to CPURST Inactive		1	RTC	3

Note 1: This transition requires both a minimum of 16 ms wait for clock synthesizer PLL lock and PWROK to be Active. If PWROK goes Active after 16 ms from nSUS[A-C] inactive, the transition will occur a minimum of 1 RTC period from PWROK Active.

Note 2: This is the PCICLK requirements for use with PC/PCI DMA and serial IRQs.

Note 3: These signals are controlled off an internal RTC clock. 1 RTC unit is approximately 32 μs.

11.3.3.7. On State to Power on Suspend State Timing

The timing figure shows the signal transitions from On state to Power On Suspend state.

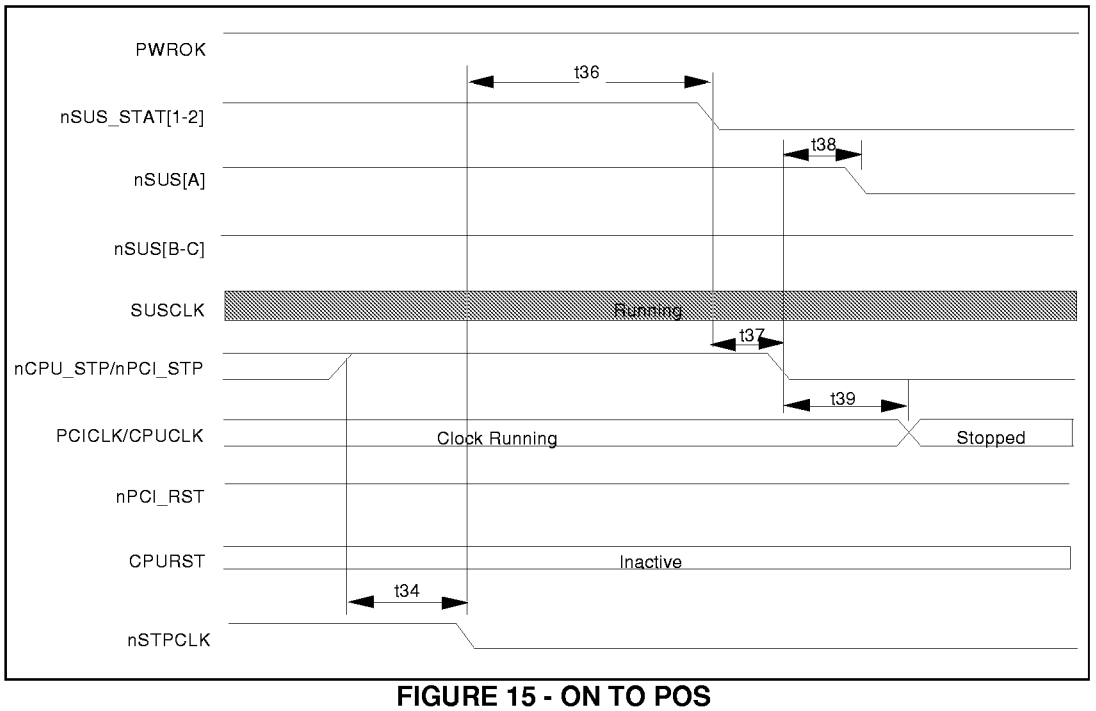


FIGURE 15 - ON TO POS

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t34	nCPU_STP and nPCI_STP Inactive to nSTPCLK Active	1		RTC	1,2
t36	nSTPCLK Active to nSUS_STAT[1-2] Active	1	2	RTC	1,3
t37	nSUS_STAT[1-2] Active to nCPU_STP and nPCI_STP Active		1	RTC	1
t38	nCPU_STP and nPCI_STP Active to nSUS[A] Active		1	RTC	1
t39	nCPU_STP and nPCI_STP Active to Clocks Stopped (if applicable)		2	PCICLK	4,5

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.
Note 2: nCPU_STP and nPCI_STP will only be active if system is under clock control.
Note 3: This transition will also wait for the Stop Grant cycle to execute.
Note 4: It is up to the system vendor to determine if nCPU_STP and nPCI_STP signals are used to control system clocks.
Note 5: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.3.8. POS to On Signal Timing (I) (with Processor and PCI Reset)

The timing figure shows the signal transitions from Power On Suspend to On with a full system reset.

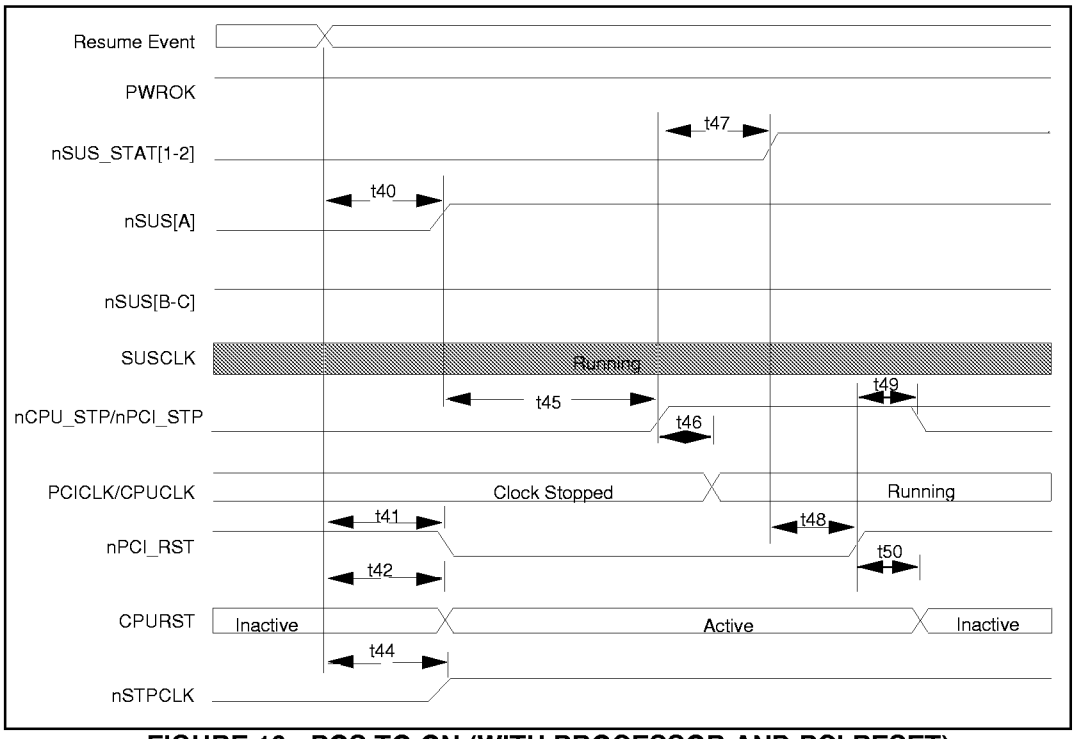


FIGURE 16 - POS TO ON (WITH PROCESSOR AND PCI RESET)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t40	Resume Event to nSUS[A] Inactive	1		RTC	1
t41	Resume Event to nPCI_RST Active	1		RTC	1
t42	Resume Event to CPURST Active	1		RTC	1
t44	Resume Event to nSTPCLK Inactive	1		RTC	1
t45	nSUS[A] Inactive to nPCI_STP and nCPU_STP Inactive	16		ms	2
t46	nPCI_STP and nCPU_STP Inactive to Clocks Running		2	PCICLK	3
t47	nPCI_STP and nCPU_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t48	nSUS_STAT[1-2] Inactive to nPCI_RST Inactive		1	RTC	1
t49	nPCI_RST Inactive to nPCI_STP and nCPU_STP allowed to change		1	RTC	1
t50	nPCI_RST Inactive to CPURST Inactive		1	RTC	1

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.

Note 2: This transition requires both a minimum of 16 ms wait for clock synthesizer PLL lock and PWROK to be active. If PWROK goes Active after 16 ms from nSUS[A-C] inactive, the transition will occur a minimum of 1 RTC period from PWROK active. PWROK remains active throughout standard POS system usage.

Note 3: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.3.9. POS to On Signal Timing (II) (with Processor Reset)

The timing figure shows the signal transitions from Power On Suspend to On with only a processor reset.

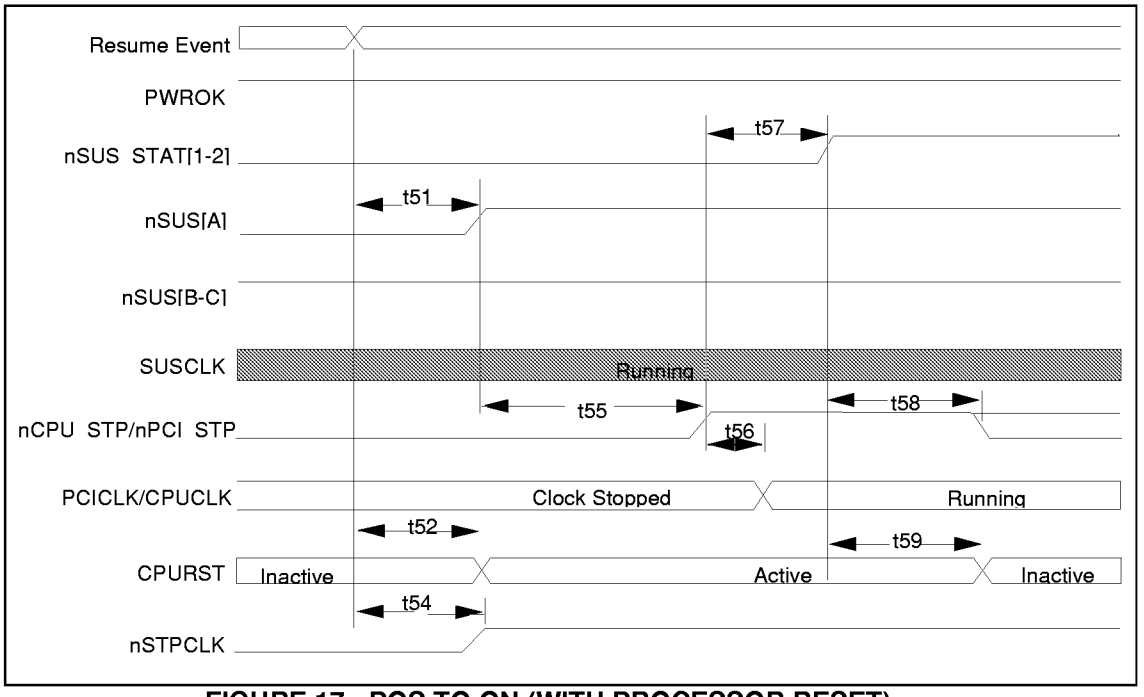


FIGURE 17 - POS TO ON (WITH PROCESSOR RESET)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t51	Resume Event to nSUS[A] Inactive	1		RTC	1
t52	Resume Event to CPURST Active	1		RTC	1
t54	Resume Event to nSTPCLK Inactive	1		RTC	1
t55	nSUS[A] Inactive to nPCI_STP and nCPU_STP Inactive	16		ms	2
t56	nPCI_STP and nCPU_STP Inactive to Clocks Running		2	PCICLK	3
t57	nPCI_STP and nCPU_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t58	nSUS_STAT[1-2] Inactive to nPCI_STP and nCPU_STP allowed to change		2	RTC	1
t59	nSUS_STAT[1-2] Inactive to CPURST Inactive		2	RTC	1

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.

Note 2: This transition requires both a minimum of 16 ms wait for clock synthesizer PLL lock and PWROK to be Active. If PWROK goes active after 16 ms from nSUS[A-C] inActive, the transition will occur a minimum of 1 RTC period from PWROK Active. PWROK remains active throughout standard POS system usage.

Note 3: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.3.10. POS to On Signal Timing (III) (No Reset)

The timing figure shows the signal transitions from Power On Suspend to On with no reset performed.

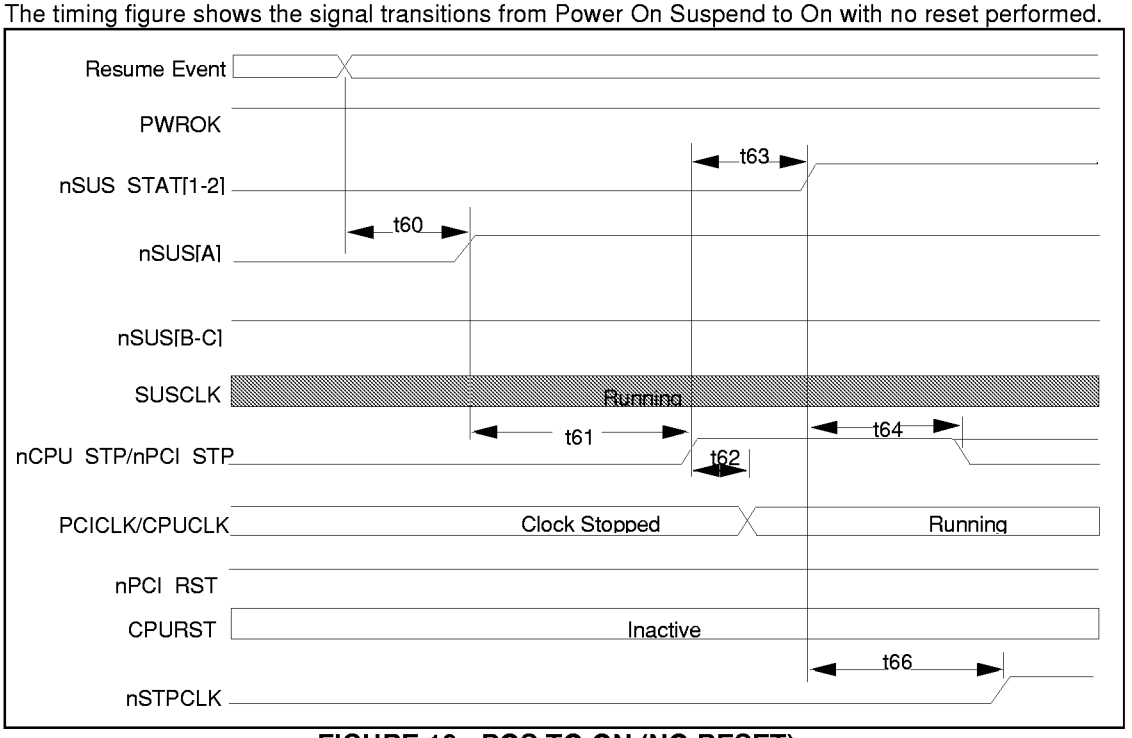


FIGURE 18 - POS TO ON (NO RESET)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t60	Resume Event to nSUS[A] Inactive	1		RTC	1
t61	nSUS[A] Inactive to nPCI_STP and nCPU_STP Inactive	16		ms	2
t62	nPCI_STP and nCPU_STP Inactive to Clocks Running		2	PCICLK	3
t63	nPCI_STP and nCPU_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t64	nSUS_STAT[1-2] Inactive to nPCI_STP and nCPU_STP allowed to change		2	RTC	1
t66	nSUS_STAT[1-2] Inactive to nSTPCLK Inactive		2	RTC	1

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32 µs.

Note 2: This transition requires both a minimum of 16 ms wait for clock synthesizer PLL lock and PWROK to be Active. If PWROK goes active after 16 ms from nSUS[A-C] inActive, the transition will occur a minimum of 1 RTC period from PWROK Active. PWROK remains active throughout standard POS system usage.

Note 3: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.3.11. On to STR Signal Timing

The timing figure shows the signal transitions from On state to Suspend to RAM state.

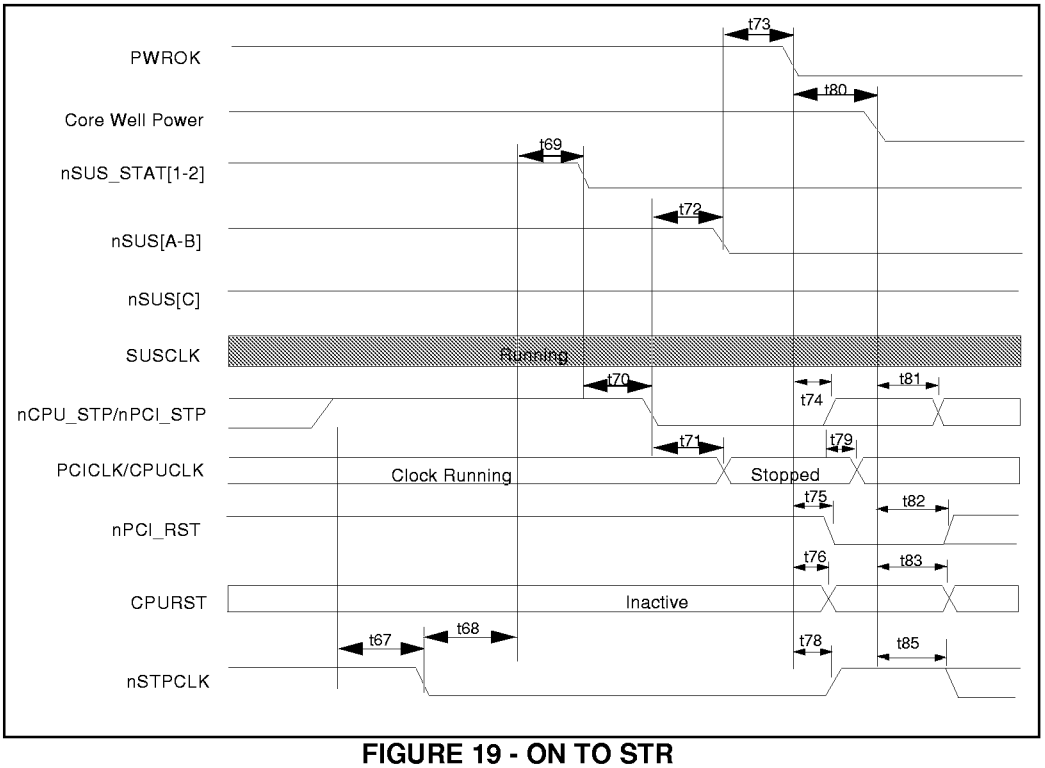


FIGURE 19 - ON TO STR

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t67	nCPU_STP and nPCI_STP Inactive to nSTPCLK Active	1		RTC	1,2
t68	nSTPCLK Active to nSLP Active	1		RTC	1,3
t69	nSLP Active to nSUS_STAT[1,2] Active		1	RTC	1
t70	nSUS_STAT[1-2] Active to nCPU_STP and nPCI_STP Active		1	RTC	1
t71	nCPU_STP and nPCI_STP Active to Clocks Stopped		2	PCICLK	4,5
t72	nCPU_STP and nPCI_STP Active to nSUS[A-B] Active		1	RTC	1
t73	nSUS[A-B] Active to PWROK Inactive	0		ns	6
t74	PWROK Inactive to nCPU_STP and nPCI_STP Float		1	RTC	1
t75	PWROK Inactive to nPCI_RST Active		1	RTC	1
t76	PWROK Inactive to CPURST Active		1	RTC	1
t78	PWROK Inactive to nSTPCLK Inactive		1	RTC	1
t79	nCPU_STP and nPCI_STP Float to Clocks Inavalid	0		ns	7
t80	PWROK Inactive to Core Well Power Removed	0		ns	
t81	Core Well Power Removed to nPCI_STP and nCPU_STP Invalid	0		ns	
t82	Core Well Power Removed to nPCIRST Invalid	0		ns	
t83	Core Well Power Removed to CPURST Invalid	0		ns	
t85	Core Well Power Removed to nSTPCLK Invalid	0		ns	

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.
Note 2: nCPU_STP and nPCI_STP will only be active if system is under clock control.
Note 3: This transition will also wait for the Stop Grant cycle to execute.
Note 4: It is up to the system vendor to determine if nCPU_STP and nPCI_STP signals are used to control system clocks.
Note 5: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.
Note 6: It is up to the system vendor to determine if nSUS[A-B] signals are used to control system power planes. If power remains applied to system board and PWROK stays alive during STR, the SLC90E46 signals will remain in the states shown after t73.
Note 7: Clocks may or may not be running depending on condition of Power Supply Voltages.

11.3.3.12. STR to On Signal Timing

The timing figure shows the system transition from Suspend To RAM to On with a full system reset.

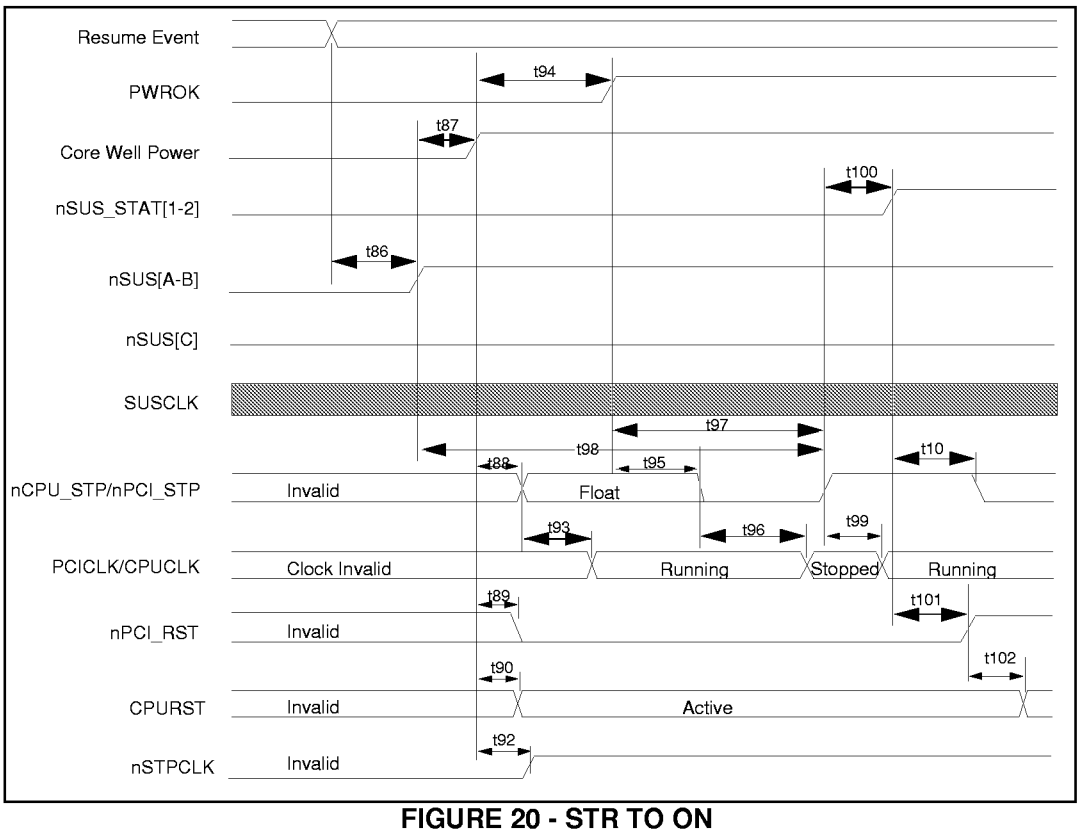


FIGURE 20 - STR TO ON

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t86	Resume Event to nSUS[A-B] Inactive	1		RTC	1
t87	nSUS[A-B] Inactive to Core Well Power Applied	0		ns	
t88	Core Well Power Applied to nPCI_STP and nCPU_STP Float	0		ns	
t89	Core Well Power Applied to nPCI_RST Active	0		ns	
t90	Core Well Power Applied to CPURST Active	0		ns	
t92	Core Well Power Applied to nSTPCLK Inactive	0		ns	
t93	nPCI_STP and nCPU_STP Float to Clocks Running				2
t94	Core Well Power Applied to PWROK Active	1		ms	
t95	PWROK Active to nCPU_STP and nPCI_STP Active	0		ns	
t96	nPCI_STP and nCPU_STP Active to Clocks Stopped		2	PCICLK	3
t97	PWROK Active to nCPU_STP and nPCI_STP Inactive	1		RTC	1
t98	nSUS[A-B] Inactive to nCPU_STP and nPCI_STP Inactive	16		ms	
t99	nCPU_STP and nPCI_STP Inactive to Clocks Running		2	PCICLK	3
t100	nCPU_STP and nPCI_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t101	nSUS_STAT[1-2] Inactive to nCPU_STP and nPCI_STP allowed to change	2		RTC	1
t101a	nSUS_STAT[1-2] Inactive to nPCI_RST Inactive	1		RTC	1
t102	nPCI_RST Inactive to CPURST Inactive	1		RTC	1

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32μs.

Note 2: There are no specific requirements for these timings related to the SLC90E46. The system manufacturer should make sure that the clocks on power up meet any other system specification. As a minimum, the clocks must be available and stable after time t99.

Note 3: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.3.13. On to STD / SOFF Signal Timing

The timing figure shows the signal transitions from On state to Suspend to Disk or Soft Off state.

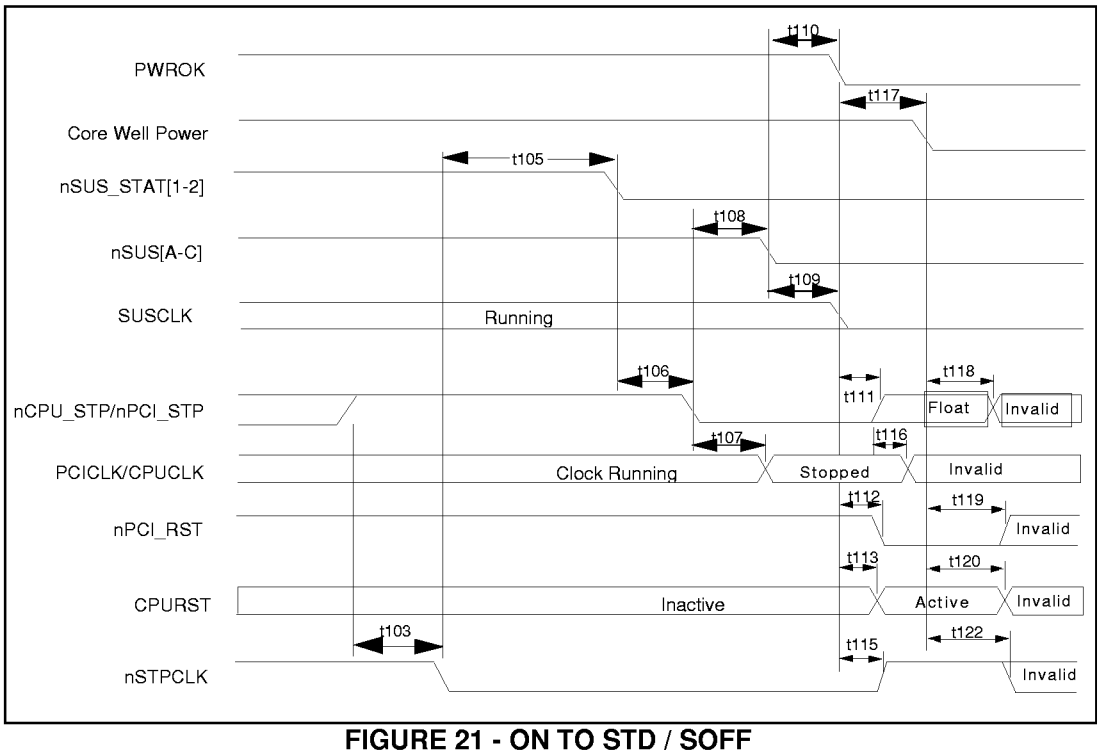


FIGURE 21 - ON TO STD / SOFF

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t103	nCPU_STP and nPCI_STP Inactive to nSTPCLK Active	1		RTC	1,2
t105	nSTPCLK Active to nSUS_STAT[1,2] Active	1	2	RTC	1
t106	nSUS_STAT[1-2] Active to nCPU_STP and nPCI_STP Active		1	RTC	1
t107	nCPU_STP and nPCI_STP Active to Clocks Stopped		2	PCICLK	1,4,5
t108	nCPU_STP and nPCI_STP Active to nSUS[A-C] Active		1	RTC	1
t109	nSUS[A-C] Active to SUSCLK Low		1	RTC	1
t110	nSUS[A-C] Active to PWROK Inactive	0		ns	6
t111	PWROK Inactive to nCPU_STP and nPCI_STP Float		1	RTC	1
t112	PWROK Inactive to nPCI_RST Active		1	RTC	1
t113	PWROK Inactive to CPURST Active		1	RTC	1
t114	PWROK Inactive to nSLP Inactive		1	RTC	1
t115	PWROK Inactive to nSTPCLK Inactive		1	RTC	1
t116	nCPU_STP and nPCI_STP Float to Clocks Inavalid	0		ns	
t117	PWROK Inactive to Core Well Power Removed	0		ns	
t118	Core Well Power Removed to nPCI_STP and nCPU_STP Invalid	0		ns	
t119	Core Well Power Removed to nPCIRST Invalid	0		ns	
t120	Core Well Power Removed to CPURST Invalid	0		ns	
t121	Core Well Power Removed to nSLP Invalid	0		ns	
t122	Core Well Power Removed to nSTPCLK Invalid	0		ns	

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.
Note 2: nCPU_STP and nPCI_STP will only be Active if system is under clock control.
Note 3: This transition will also wait for the Stop Grant cycle to execute.
Note 4: It is up to the system vendor to determine if nCPU_STP and nPCI_STP signals are used to control system clocks.
Note 5: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.
Note 6: It is up to the system vendor to determine if nSUS[A-C] signals are used to control system power planes. If power remains applied to system board and PWROK stays alive during STR, the SLC90E46 signals will remain in the states shown after t110.

11.3.3.14. STD / SOFF to On Signal Timing

The timing figure shows the system transition from Suspend To Disk to On with a full system reset.

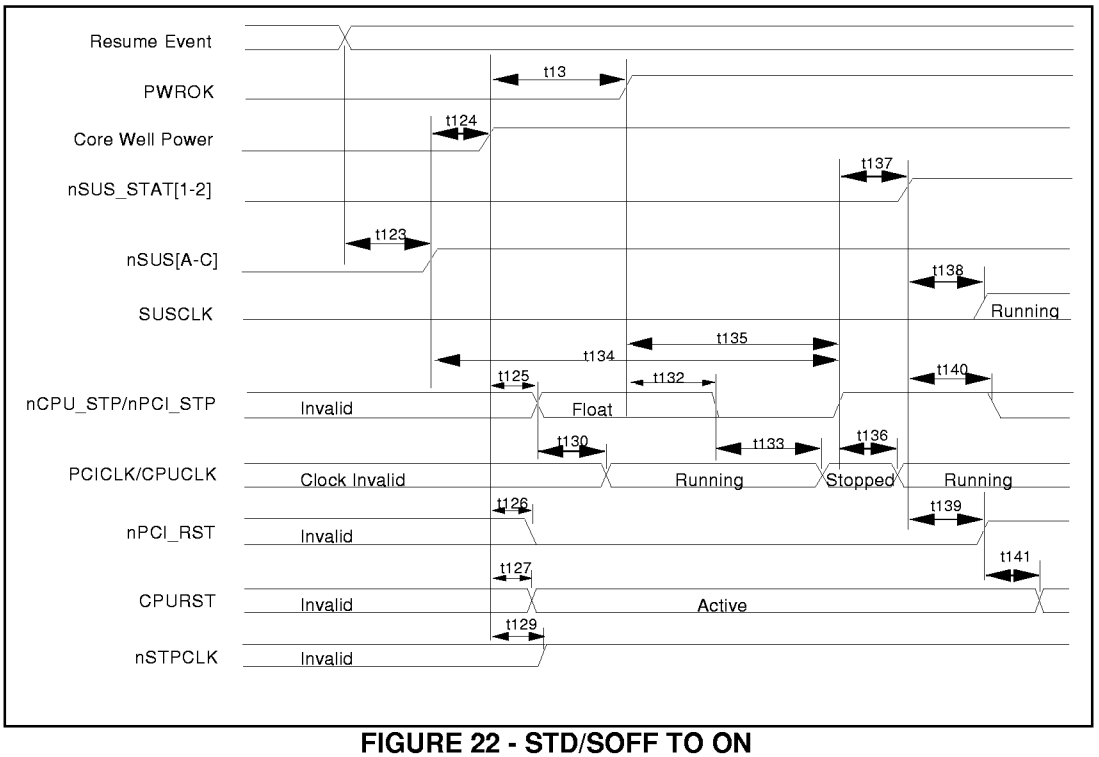


FIGURE 22 - STD/SOFF TO ON

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
t123	Resume Event to nSUS[A-C] Inactive	1		RTC	1
t124	nSUS[A-C] Inactive to Core Well Power Applied	0		ns	
t125	Core Well Power Applied to nPCI_STP and nCPU_STP Float	0		ns	
t126	Core Well Power Applied to nPCI_RST Active	0		ns	
t127	Core Well Power Applied to CPURST Active	0		ns	
t129	Core Well Power Applied to nSTPCLK Inactive	0		ns	
t130	nPCI_STP and nCPU_STP Float to Clocks Running				2
t131	Core Well Power Applied to PWROK Active	1		ms	
t132	PWROK Active to nCPU_STP and nPCI_STP Active	0		ns	
t133	nPCI_STP and nCPU_STP Active to Clocks Stopped		2	PCICLK	3
t134	nSUS[A-C] Inactive to nCPU_STP and nPCI_STP Inactive	16		ms	
t135	PWROK Active to nCPU_STP and nPCI_STP Inactive	1		RTC	1
t136	nCPU_STP and nPCI_STP Inactive to Clocks Running	1	2	PCICLK	3
t137	nCPU_STP and nPCI_STP Inactive to nSUS_STAT[1-2] Inactive	1		ms	
t138	nSUS_STAT[1-2] Inactive to SUSCLK Running	1		RTC	1
t139	nSUS_STAT[1-2] Inactive to nPCI_RST Inactive	1		RTC	1
t140	nSUS_STAT[1-2] Inactive to nCPU_STP and nPCI_STP allowed to change	2		RTC	1
t141	nPCI_RST Inactive to CPURST Inactive	1		RTC	1

Note 1: These signals are controlled off an internal RTC clock. 1RTC unit is approximately 32µs.

Note 2: There are no specific requirements for these timings related to the SLC90E46. The system manufacturer should make sure that the clocks on power up meet any other system specification. As a minimum, the clocks must be available and stable after time t136.

Note 3: See PCICLK requirements for use with PC/PCI DMA and serial IRQs.

11.3.4. Alternate AT Register Access Mode

The SLC90E46 implements a shadow mechanism for storing the data written to the AT write-only registers. An "Alternate AT Register Access Mode" is also implemented so that, in the transition to Suspend mode, the contents of these registers can be read and saved to non-volatile memory so the system state can be restored when resumed.

Once placed in the "Alternate Access" mode, the SLC90E46 allows various registers that would otherwise be inaccessible be read and written. To enable the Alternate Access mode, set Bit 5, Register 0B0h of the SLC90E46 PCI Function 0 to a 1.

Since there are no provisions are made for stopping events from occurring while the BIOS is reading or restoring register values, the BIOS should exercise with great care while using this feature. For example, when reading the status of the DMA controller, all the DMA channel should be temporarily masked.

It is assumed that no other accesses to the module will be permitted once in ALT Access mode.

Table 37 - DMA Controller Registers In Alternate Access Mode

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
0000h	W	Base Address for Channel 0	Current Address for Channel 0
0000h	R	Current Address for Channel 0	Base Address for Channel 0
0001h	W	Base Byte Count for Channel 0	Current Byte Count for Channel 0
0001h	R	Current Byte Count for Channel 0	Base Byte Count for Channel 0
0002h	W	Base Address for Channel 1	Current Address for Channel 1
0002h	R	Current Address for Channel 1	Base Address for Channel 1
0003h	W	Base Byte Count for Channel 1	Current Byte Count for Channel 1
0003h	R	Current Byte Count for Channel 1	Base Byte Count for Channel 1
0004h	W	Base Address for Channel 2	Current Address for Channel 2
0004h	R	Current Address for Channel 2	Base Address for Channel 2
0005h	W	Base Byte Count for Channel 2	Current Byte Count for Channel 2
0005h	R	Current Byte Count for Channel 2	Base Byte Count for Channel 2
0006h	W	Base Address for Channel 3	Current Address for Channel 3
0006h	R	Current Address for Channel 3	Base Address for Channel 3
0007h	W	Base Byte Count for Channel 3	Current Byte Count for Channel 3
0007h	R	Current Byte Count for Channel 3	Base Byte Count for Channel 3
0008h	W	Command Register (Ch. 0-3)	Status Register (Ch. 0-3)
0008h	R	Status Register (Ch. 0-3)	1st Read: Command Register (Ch. 0-3) 2nd Read: Request Register (Ch. 0-3) 3rd Read: Mode Register (Ch 0) 4th Read: Mode Register (Ch 1) 5th Read: Mode Register (Ch 2) 6th Read: Mode Register (Ch 3)
0009h	W	Request Register (Ch 0-3)	Reserved
0009h	R	Reserved	Reserved
000Ah	W	Write Single Mask (Ch 0-3)	Reserved

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
000Ah	R	Reserved	Reserved
000Bh	W	Mode Register (Ch 0-3)	Reserved
000Bh	R	Reserved	Reserved
000Ch	W	Clear Byte Pointer	Clear Byte Pointer
000Ch	R	Reserved	Reserved
000Dh	W	Master Clear	Master Clear
000Dh	R	Reserved	Reserved
000Eh	W	Clear Masks	Clear Masks
000Eh	R	Reserved	Reserved
000Fh	W	Write All Masks (0-3)	Write All Masks (0-3)
000Fh	R	Reserved	Read All Masks (0-3)
DMA CONTROLLER II (16 BIT)			
00C0h	W	Base Address for Channel 4	Current Address for Channel 4
00C0h	R	Current Address for Channel 4	Base Address for Channel 4
00C2h	W	Base Word Count for Channel 4	Current Word Count for Channel 4
00C2h	R	Current Word Count for Channel 4	Base Word Count for Channel 4
00C4h	W	Base Address for Channel 5	Current Address for Channel 5
00C4h	R	Current Address for Channel 5	Base Address for Channel 5
00C6h	W	Base Word Count for Channel 5	Current Word Count for Channel 5
00C6h	R	Current Word Count for Channel 5	Base Word Count for Channel 5
00C8h	W	Base Address for Channel 6	Current Address for Channel 6
00C8h	R	Current Address for Channel 6	Base Address for Channel 6
00CAh	W	Base Word Count for Channel 6	Current Word Count for Channel 6
00CAh	R	Current Word Count for Channel 6	Base Word Count for Channel 6
00CCh	W	Base Address for Channel 7	Current Address for Channel 7
00CCh	R	Current Address for Channel 7	Base Address for Channel 7
00CEh	W	Base Word Count for Channel 7	Current Word Count for Channel 7
00CEh	R	Current Word Count for Channel 7	Base Word Count for Channel 7
00D0h	W	Command Register (Ch. 4-7)	Status Register (Ch. 4-7)
00D0h	R	Status Register (Ch. 4-7)	1st Read: Command Register (Ch. 4-7) 2nd Read: Request Register (Ch. 4-7) 3rd Read: Mode Register (Ch 4) 4th Read: Mode Register (Ch 5) 5th Read: Mode Register (Ch 6) 6th Read: Mode Register (Ch 7)
00D2h	W	Request Register (Ch 4-7)	Reserved
00D2h	R	Reserved	Reserved
00D4h	W	Write Single Mask (Ch 4-7)	Reserved
00D4h	R	Reserved	Reserved
00D6h	W	Mode Register (Ch 4-7)	Reserved
00D6h	R	Reserved	Reserved
00D8h	W	Clear Byte Pointer	Clear Byte Pointer
00D8h	R	Reserved	Reserved

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
00DAh	W	Master Clear	Master Clear
00DAh	R	Reserved	Reserved
00DCh	W	Clear Masks	Clear Masks
00DCh	R	Reserved	Reserved
00DEh	W	Write All Masks (4-7)	Write All Masks (4-7)
00DEh	R	Reserved	Read All Masks (4-7)

Note: The Alternate Access Mode allows reading and restoring all of the initial base address and byte/word counts. Also makes it possible to read command, mode, and mask registers, as well as restore status, mode and mask registers.

Table 38 - NMI Enable Bit Changes in Alternate Access Mode

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
0070h (bit7 only)	R	Invalid	Bit 7 (NMI Enable Bit) value is returned.

Table 39 - Programmable Interval Timer Changes In Alternate Access Mode

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
0040h	R	Status Byte Counter 0.	1st Read: Status Byte Counter 0. 2nd Read: CR_L for Counter 0. 3rd Read: CR_M for Counter 0. 4th Read: CR_L for Counter 1. 5th Read: CR_M for Counter 1. 6th Read: CR_L for Counter 2. 7th Read: CR_M for Counter 2.
0041h	R	Status Byte Counter 1.	Status Byte Counter 1.
0042h	R	Status Byte Counter 2.	Status Byte Counter 2.

The BIOS must perform 7 consecutive reads from port 40h in alternate access mode. If BIOS deviates from this, it may get inaccurate data. It also allows BIOS to set the Alt Access Mode and still read the status of all the counters. Setting the Alt Access Mode automatically clears the high/low flip flop. When the Alt Access mode is entered the timers do not stop counting, hence the current values will change from the time the initial value is read.

Table 40 - Programmable Interrupt Controller

I/O ADDRESS	R/W MODE	STANDARD MODE USAGE	ALT ACCESS MODE
0020h	R	Interrupt Request Register for Controller 1.	1st Read: ICW1 for Controller 1 2nd Read: ICW2 for Controller 1 3rd Read: ICW3 for Controller 1 4th Read: ICW4 for Controller 1 5th Read: OCW1 for Controller 1 6th Read: OCW2 for Controller 1 7th Read: OCW3 for Controller 1 8th Read: ICW1 for Controller 2 9th Read: ICW2 for Controller 2 10th Read: ICW3 for Controller 2 11th Read: ICW4 for Controller 2 12th Read: OCW1 for Controller 2 13th Read: OCW2 for Controller 2 14th Read: OCW3 for Controller 2
0021h	R	In-Service Register for Controller 1.	In-Service Register for Controller 1.
00A0h	R	Interrupt Request Register for Controller 2.	Interrupt Request Register for Controller 2.
00A1h	R	In-Service Register for Controller 2.	In-Service Register for Controller 2.

11.4. System Management

The SLC90E46 system management function provides mechanisms to communicate detected system activities to system management software and to communicate with other devices on the system board. Communication with system software is through the System Management Interrupt (SMI) mechanism, and an integrated System Management Bus host and slave controller can be used to communicate with on-board devices.

11.4.1. SMI Assertion Mechanism

The following figure shows operation of SMI generation logic. SMI generation is enabled by setting the [SMI_EN] bit, bit 0 of GLBCTL IO Register, and controlled by the End of SMI [EOS] bit, bit 16 of GLBCTL IO Register. The EOS bit is first set to enable the generation of the first SMI. When an enabled nSMI generation event occurs, the EOS bit is reset to 0. When this bit is cleared the nSMI signal is asserted. The processor will then enter System Management Mode and the SMI handler will service all requesting SMIs. If an SMI event occurs while the SLC90E46 has this bit, EOS, cleared, then no additional SMIs to the processor are generated, however the appropriate status bits will be set. At the end of the SMI handler, the software will set this bit. When the bit is set, the SLC90E46 will drive the nSMI signal inactive for a minimum of 1 PCI clock. The combination of this bit being set, and another SMI request being active (one of the SMI status bits is set) will cause the SLC90E46 to reset [EOS] bit again and re-assert the SMI signal to the processor.

It is important to know that EOS bit will not get set until all SMI status bits are cleared. Therefore, before exiting, the SMI handler has to verify that the bit is successfully set. Otherwise, there could be other pending SMI that will prevent the EOS bit from being set. In this case, the SMI handler should clear that SMI status bit and set the EOS bit again.

11.4.2. nSMI Generation Events

Some of the nSMI generation events may also generate the ACPI compatible System Control Interrupt (SCI) or suspend state resume events. The nSMI or SCI is selectable through the [SCI_EN] bit, which is bit 0 of the PMCNTRL IO Register. When the bit is set to 1, these events will generate an SCI if enabled. When the bit is reset, these events will generate an nSMI if enabled.

When an nSMI event occurs, a status bit is set. The status bits from various sources are combined together to create hierarchical status bits. The hierarchical status bits cannot be reset through software. Their respective “children” status bits must all be cleared in order for them to clear.

The nSMI generation events include:

- nPWRBTN Assertion
- LID Assertion
- nGPI1 Assertion
- EXTnSMI Asssertion.
- SMBus Events
- Global Standby Timer Expiration.
- PCI Bus Master Requests.
- APMC Control Register Writes
- USB Legacy Keyboard/Mouse Event.

- Software Timer SMI.
- Device Monitor Trap.
- Device Monitor Idle Timer Expiration.
- SLC90E46 Master Abort on PCI
- Global Release.
- Thermal Alarm (nTHRM Assertion).

nPWRBTN Assertion Event

The nPWRBTN input signal can be used to generate an nSMI upon its assertion. It contains a 16ms debounce circuit to filter out mechanical switch bounce. When asserted, it will set the [PWRBTN_STS] bit after the 16ms debounce. This will cause generation of an nSMI if enabled. If the nPWRBTN signal is held active for greater than 4 seconds and Power Button Override feature is enabled, the [PWRBTN_STS] bit is cleared, the [PWRBTNOR_STS] bit is set, and the SLC90E46 will automatically transition the system into the Soft Off Suspend state. This signal can also be used to generate an SCI or a suspend state resume event.

In a suspend state, the assertion of nPWRBTN signal will always set the PWRBTN_STS bit and generate a resume event causing the SLC90E46 to initiate a resume sequence.

Enable Bits:	[PWRBTN_EN]	Bit 8 of PMEN IO Register (Base + 02h)
	[PWRBTNOR_EN]	Bit 9 of PMCNTRL IO Register (Base + 04h)
Status Bits:	[PWRBTN_STS]	Bit 8 of PMSTS IO Register (Base + 00h)
	[PWRBTNOR_STS]	Bit 11 of PMSTS IO Register (Base + 00h)

LID Assertion Event

The LID signal, when asserted, will set the [LID_STS] bit after a 16ms debounce, and when enabled will generate an nSMI. The assertion polarity can be controlled to allow system code to detect when LID signal transistions from low to high or high to low. This signal can also be used to generate an SCI or a suspend state resume event.

Enable Bit:	[LID_EN]	Bit 11 of GPEN IO Register (Base + 0Eh)
Polarity Select:	[LID_POL]	Bit 25 of GLBCTL IO Register (Base + 28h)
Status Bits:	[LID_STS]	Bit 11 of GPSTS IO Register (Base + 0Ch)

nGPI1 Assertion Event

The nGPI1 signal, when asserted LOW, will set the [GPI_STS] bit, and when enabled will generate an nSMI. This signal can also be used to generate an SCI or a suspend state resume event.

Enable Bit:	[GPI_EN]	Bit 9 of GPEN IO Register (Base + 0Eh)
Status Bit:	[GPI_STS]	Bit 9 of GPSTS IO Register (Base + 0Ch)

nEXTSMI Assertion Event

The nEXTSMI signal, when asserted LOW, will set the [EXTSMI_STS] bit, and when enabled will generate an nSMI. This signal can also be used to generate an SCI or a suspend state resume event.

Enable Bit:	[EXTSMI_EN]	Bit 10 of GLBEN IO Register (Base + 20h)
Status Bit:	[EXTSMI_STS]	Bit 10 of GLBSTS IO Register (Base + 18h)

SMBus Events

The SMBus Controller has several ways to generate an nSMI. They can also be used to generate a suspend state resume event. See SMBus Functional Description for additional information.

Enable Bits:	[ALERT_EN]	Bit 3 of SMBSLVCNT SMBus IO Register (Base + 08h)
	[SLV_EN]	Bit 0 of SMBSLVCNT SMBus IO Register (Base + 08h)
	[SHDW1_EN]	Bit 1 of SMBSLVCNT SMBus IO Register (Base + 08h)
	[SHDW2_EN]	Bit 2 of SMBSLVCNT SMBus IO Register (Base + 08h)
Status Bits:	[ALERT_STS]	Bit 5 of SMBSLVSTS SMBus IO Register (Base + 01h)
	[SLV_STS]	Bit 2 of SMBSLVSTS SMBus IO Register (Base + 01h)
	[SHDW1_STS]	Bit 3 of SMBSLVSTS SMBus IO Register (Base + 01h)
	[SHDW2_STS]	Bit 4 of SMBSLVSTS SMBus IO Register (Base + 01h)

Global Standby Timer Expiration Event

The Global Standby Timer will set the [GSTBY_STS] bit upon expiration, and if enabled will generate an nSMI. It can also be used to generate a suspend state resume event.

Enable Bits:	[GSTBY_EN]	Bit 8 of GLBEN IO Register (Base + 20h)
Status Bits:	[GSTBY_STS]	Bit 8 of GLBSTS IO Register (Base + 18h)

PCI Bus Master Requests Event

Assertion of nPCIREQ[0-3] or nPHOLD will generate an nSMI if enabled. This can also cause idle, burst, or global standby timer reloads as part of Device 8 Monitor logic.

Enable Bits:	[BM_TRP_EN]	Bit 3 of GLBEN IO Register (Base + 20h)
	[BM_RLD_DEV8]	Bit 27 of DEVCTL IO Register (Base + 2Ch)
Status Bit:	[BM_STS]	Bit 4 of PMSTS IO Register (Base + 00h)

APMC Control Register Writes

Writes to the APM Control Register (APMC, IO port B2h) will generate an nSMI if enabled.

Enable Bit:	[APMC_EN]	Bit 25 of DEVACTB PCI Configuration Register (58-5Bh)
Status Bit:	[APM_STS]	Bit 5 of GLBSTS IO Register (Base + 18h)

USB Legacy Keyboard/Mouse Event (Not Implemented Yet)

The USB Legacy Keyboard logic uses nSMI generation as part of its operation. The [LEGACY_USB_EN] bit must be set active in order for USB Legacy Keyboard to function.

Enable Bit:	[LEGACY_USB_EN]	Bit 0 of GLBEN IO Register (Base + 20h)
Status Bit:	[LEGACY_USB_STS]	Bit 1 of GLBSTS IO Register (Base + 18h)

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Software Timer SMI Event

The Idle Timer for Device 3 Monitor can be used as a Software SMI Timer. If the Idle Timer reload events are disabled (via [IDL_RLD_EN_DEV3] bit), the timer will count down without reload and its expiration will generate an nSMI.

Enable Bit:	[IDL_EN_DEV3]	Bit 6 of DEVCTL IO Register (Base + 2Ch)
	[IDL_RLD_EN_DEV3]	Bit 26 of DEVCTL IO Register (Base + 2Ch)
Status Bit:	[IDL_STS_DEV3]	Bit 3 of DEVSTS IO Register (Base + 1Ch)

Device Trap Event

The IO Trap for Device Monitoring subsystem will generate an nSMI when the programmed trap event occurs. The [DEV_STS] bit is a logical OR of [TRAP_STS_DEVx] and [IDL_STS_DEVx] bits.

Enable Bit:	[TRAP_EN_DEVx]	See DEVCTL IO Register (Base + 2Ch)
Status Bits:	[TRAP_STS_DEVx]	See DEVSTS IO Register (Base + 1Ch)
	[DEV_STS]	Bit 4 of GLBSTS IO Register (Base + 18h) where x = 0-13

Device Idle Timer Expiration Event

The Idle Timers for Device Monitoring subsystem will count down and generate an nSMI upon expiration if enabled. The [DEV_STS] bit is logical "OR" of [TRP_STS_DEVx] and [IDL_STS_DEVx] bits.

Enable Bits:	[IDL_EN_DEVx]	See DEVCTL IO Register (Base + 2Ch)
Status Bits:	[IDL_STS_DEVx]	Bits[11-0] of DEVSTS IO Register (Base + 1Ch)
	[DEV_STS]	Bit 4 of GLBSTS IO Register (Base +18h) where x = 0-11.

SLC90E46 Master Abort on PCI

A Master Abort to the SLC90E46 initiated PCI cycle will generate an nSMI if enabled.

Enable Bits:	[SBMA_EN]	Bit 4 of GLBEN IO Register (Base + 20h)
Status Bits:	[SBMA_STS]	Bit 2 of GLBSTS IO Register (Base + 18h)

Global Release Event

Writes to the Power Management I Control Register (PM1_CNTRL) with bit 2 set will generate an nSMI if enabled. See ACPI Support section for more information.

Enable Bits:	[BIOS_EN]	Bit 1 of GLBEN IO Register (Base + 20h)
Status Bits:	[BIOS_STS]	Bit 0 of GLBSTS IO Register (Base + 18h)

Thermal Alarm Event (nTHRM Assertion)

The nTHRM signal will set the [THRM_STS] bit when asserted and if enabled will generate an nSMI. The assertion polarity can be programmed to allow system code to detect when nTHRM signal transitions from low to high or high to low. This signal can also be used to generate an SCI. When asserted, the nTHRM will also cause automatic clock throttling, which is independent of the [THEM_EN] control bit.

Enable Bit:	[THEM_EN]	Bit 0 of GPEN IO Register (Base + 0Eh)
Polarity Select:	[THRM_POL]	Bit 2 of GLBCTL IO Register (Base + 28h)
Status Bit:	[THEM_STS]	Bit 0 of GPSTS IO Register (Base + 0Ch)

11.4.3. Global Standby Timer

The Global Standby Timer is used to monitor global system activity during normal operation and can be reloaded by system activity events. When enabled, the timer will load and start counting down. Enabled system events will cause the timer to reload its initial value and begin counting down again. If no system events reload the timer, it will eventually count to zero. Upon this expiration, it generates an nSMI. When the system is placed in a Suspend Mode, the Global Standby Timer can also be used to generate a resume event.

The Global Standby Timer stops counting when the SM_FREEZE bit is set. This can be used to keep it from counting down when the system is executing an SM routine. The SM_FREEZE bit is disregarded while in a Suspend state, so that the Global Standby Timer will count down independent of the SM_FREEZE value.

Resolution: 4 milliseconds, 4 seconds, 32 seconds or 4 minutes

	[GSTBY_SELA]	Bit 8 of GLBCTL IO Register (Base+28h)
	[GSTBY_SELB]	Bit 26 of GLBCTL IO Register
Count (7-bit):	[GSTBY_CNT]	Bit[15-9] of GLBCTL IO Register
Counter and nSMI Enable:	[GSTBY_EN]	Bit 8 of GLBEN IO Register (Base+20h)
Expiration Status:	[GSTBY_STS]	Bit 8 of GLBSTS IO Register (Base+18h)

Global Standby Timer Reload Events and The Control Register Bits:

IRQ1, IRQ12/M	[GRLD_EN_KBC_MS]	Bit 2 of DEVACTB PCI Register (58h-5Bh)
NMI, INIT, IRQ[1,3-7,9-15]:	[GRLD_EN_IRQ]	Bit 6 of DEVACTB PCI Register (58h-5Bh)
Device 0-13 Monitors:	[GRLD_EN_DEVx]	Bit[13-0] of DEVACTA PCI Reg.(54h-57h)
Video Monitor (PCI Bus Utilization):		
	[VIDEO_EN]	Bit 24 of DEVACTB PCI Reg. (58h-5Bh)
PCI Bus Master Activity:	[BM_RLD_DEV8]-	Bit 27 of DEVCTL IO Register (Base+2Ch)
	[GRLD_EN_DEV8]	Bit 8 of DEVACTA PCI Reg. (54h-57h)

11.5. ACPI Support

The SLC90E46 fully supports the new ACPI specification, including the ACPI I/O register mapping, the SCI interrupt and a Power Management Timer. A semaphore mechanism is also implemented to coordinate access to the power management resources by either ACPI or the BIOS.

11.5.1. SCI Generation

The nPWRBTN, nGPI1, nTHRM, and LID events can be enabled to generate the ACPI interrupt, SCI (IRQ9) or an nSMI. The nSMI or SCI is selectable with the [SCI_EN] bit. When set to 1, an enabled event will generate an SCI.

SCI Generation Events Control Bits

nPWRBTN Asserted	[PWRBTN_EN]
GPI1 Asserted	[GPI_EN]
Thermal Alarm (nTHRM Assertion)	[THRM_EN]
-Polarity Select	[THRM_POL]
LID Asserted	[LID_EN]
-Polarity Select	[LID_POL]
Power Management Timer Overflow	[TMROF_EN]
BIOS Release	[GLB_EN]

11.5.2. Power Management Timer

The SLC90E46 integrates an ACPI compatible power management timer. The timer consists of a free running counter (with a 14.31818 / 4, or 3.579545MHz clock source), a timer register, and a single interrupt source. This circuit is illustrated below. The interrupt source is used to indicate that the counter has changed bit 22 high to low or low to high, this condition generates a System Control Interrupt (SCI). The overflow interrupt is used by ACPI software to understand when the timer is about to overflow, and allows software to emulate a larger timer.

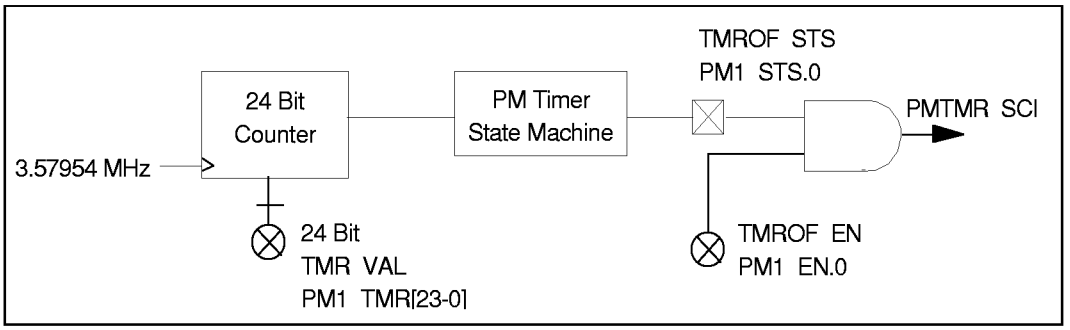

FIGURE 24 - POWER MANAGEMENT TIMER

Power Management Timer Programming:

Clock Frequency: 3.579545 MHz (14.31818/4)
Timer Value: [TMR_VAL]
Timer Overflow Status: [TMROF_STS]
SCI Generation Control: [TMROF_EN]

11.5.3. Global Lock Mechanism

If the BIOS and ACPI software will share resources through a common I/O port, a Global Lock mechanism must be applied as a semaphore to arbitrate to these shared resources. For example, if both the BIOS and the ACPI driver shares the same system management microcontroller I/O ports to manage the system, the access must be controlled through the Global Lock mechanism.

If the BIOS attempts to use the shared resources and there is a conflict, the Global Lock logic is used by the ACPI driver to inform the BIOS when it is finished using a shared resource. To do so, the BIOS first accesses the GBL_RLS bit to attempt to gain ownership of the lock. This access will set the BIOS_STS bit. ACPI software will release the lock by setting the BIOS_EN bit. SLC90E46 then generates an SMI which informs BIOS software that the shared resource is now available.

Likewise if the ACPI attempts to use the shared resources and there is a conflict, the Global Lock logic is used by the BIOS to inform the ACPI driver when it is finished using the shared resources. The ACPI software first accesses the BIOS_RLS bit to attempt to gain ownership of the lock. This access will set the GBL_STS bit. BIOS will release the lock by setting the GBL_EN bit. SLC90E46 then generates an SCI which informs ACPI software that the shared resource is now available.

11.6. System Management Bus Controller

The System Management Bus (SMBus) is a two-wire interface for the system to communicate with on-board devices. With SMBus, a device can provide information about its model/part number/manufacture, accept control parameters, report its status, and save its states for a suspend event.

The SLC90E46 SMBus controller includes a host controller, host controller slave port, and two SMBus slave shadow ports. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals. The SMBus slave interface provides a mechanisum for other SMBus masters to communicate with the SLC90E46 and can be used to generate interrupts or resume events for a suspended system. The SMBus nALERT protocol is also supported. The SLC90E46 SMBus controller has 3.3V input buffers, which requires the system's SMBus to be designed with a 3.3V termination voltage. The programming model is split between function 3 (power management module) PCI configuration registers and SMBus I/O space registers. The SLC90E46 SM Bus is a subset of the Philips I^2C protocol.

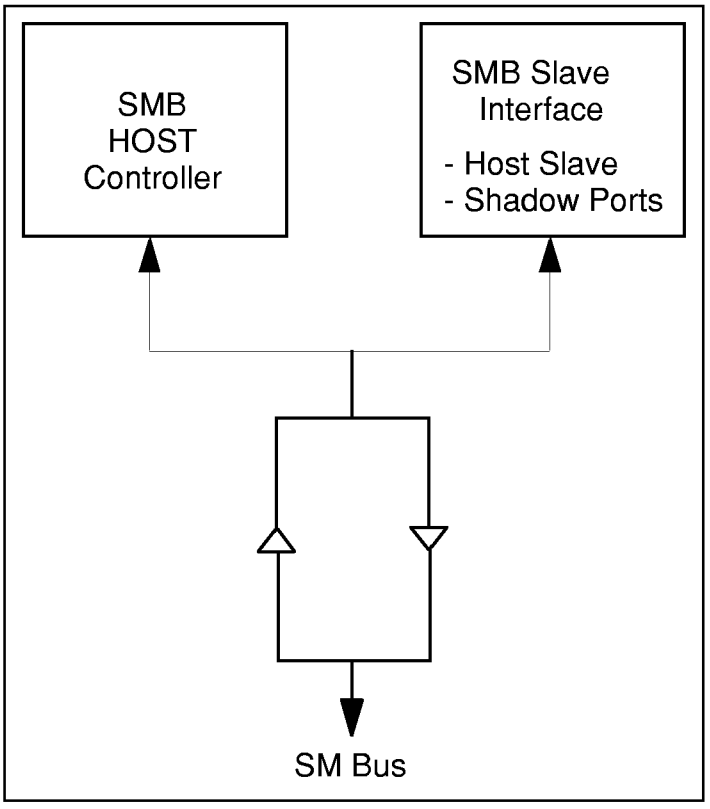

FIGURE 25 - SYSTEM MANAGEMENT BUS CONTROLLER

The SMBus Host Controller is used to send host commands to various SMBus devices. The SLC90E46 contains a full host controller implemenatation. The SLC90E46 SMBus controller supports seven command protocols of the SMBus interface (See System Management Bus Specification, Rev. 1.0):

- Quick Command
- Send Byte
- Receive Byte
- Write Byte/Word
- Read Byte/Word
- Block Read
- Block Write

To initiate a SMBus host transfer, the type of transfer protocol, the address of the SMBus device, the device specific command, the data, and any control bits are first setup. Then the START bit is set, which triggers the host controller to execute the transaction. Upon completion of the transaction, the SLC90E46 will generate an interrupt if enabled. The interrupt can be selected either IRQ9 or nSMI. The system software can wait for interrupt to signal completion or it can monitor the HOST_BUSY status bit. An interrupt will also be signaled if an error occurred during the transaction or if the transaction was terminated by software setting the KILL bit. After setting the START bit while the HOST_BUSY bit is Active, all the host controller registers, whose names have a prefix SMBHST---, should not be accessed.

The SMBus controller will not respond to the START bit being set unless all interrupt status bits in the SMBHSTSTS register have been cleared.

11.6.1.1. Block Read/Write

For Block Read or Block Write protocols, the data is stored in a 32-byte block data storage array. This array is addressed via an internal index pointer. The index pointer is initialized to zero on each read of the SMBHSTCNT register, and it is incremented by one after each access to the SMBBLKDAT register.

For Block Write transactions, the data to be transferred is stored in this array and the byte count is stored in SMBHSTDAT0 register before initiating the transaction.

For Block Read transactions, the SMBus peripheral decides the amount of data to be transferred. After the transactions is completed, the byte count transferred is stored in the SMBHSTDAT0 register and data is stored in the block data array.

Accesses to the data array during execution of the SMBus transaction always starts at address 0.

Any register values needed for later reference purpose should be saved before the starting of a new transaction, as the SMBus host controller will update the registers while executing the new transaction.

11.6.2. SMBus Slave Interface

There are three mechanisms for SMBus peripherals to communicate to the SLC90E46. In addition to transferring data, these mechanisms can generate an interrupt or resume the system from a suspend state. Once the slave interface has received a transaction and generated an interrupt, it will stop responding to new requests until all the interrupt status bits in the SMBSLVSTS register are cleared.

Mechanism 1: Access to Host Slave Port 10h

The first mechanism consists of accesses to the SMBus controller host slave port at address 10h. (Note this address is actually 0001 000x as this is a 7 bit address with bit 0 being R/W bit.) The host slave port only responds to Word Write transactions with the incoming data being stored in the SMBSLVDAT register and incoming command in the SMBSHDWCMD register. An interrupt or resume event will be generated (if enabled) if the incoming command matches the command stored in SMBSLVC register and at least one bit read into the register matches with the corresponding bit in the SMBSLVEVT register.

Mechanism 2: Access to Slave Shadow Ports

The second mechanism monitors for accesses to the SMBus controller slave shadow ports at address stored in SMBSHDW1 and SMBSHDW2 registers. The shadow slave ports also only responds to Word Write transactions with the incoming data being stored in SMBSLVDAT register and incoming command being stored in the SMBSHDWCMD register. An interrupt or resume event will be generated (if enabled) upon accesses to the slave shadow ports.

The SLV_BSY bit indicates that the SLC90E46 slave interface is receiving an incoming message. The SMBSLVCNT, SMBSHDWCMD, SMBSLVENT, SMBSLVDAT and SMBSLVC registers should not be accessed while the SLV_BSY bit is active (until completion of transaction).

Mechanism 3: nSMBALERT Assertion

The third method for SMBus devices to communicate with the SLC90E46 is through the nSMBALERT signal. When enabled and the nSMBALERT signal is asserted, the SLC90E46 will generate an interrupt or resume the system from a suspend state. This mechanism allows a device without SMBus master capabilities to request service from the SMBus host. To determine which device asserted the nSMBALERT signal, the SLC90E46 host controller should be programmed to execute a read command using the Alert Response Address.

Circuit diagrams utilizing SMSC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any licenses under the patent rights of SMSC or others. SMSC reserves the right to make changes at any time in order to improve design and supply the best product possible. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer.

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