SMC®
STANDARD
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CORPORATION

FDC37C667
ADVANCE INFORMATION

Plug and Play Compatible Advanced High-Performance Multi-Mode™ Parallel Port Super I/O Floppy Disk Controller

FEATURES

- Plug and Play Compatible, Version 1.0a
  - Serial EEPROM Interface
  - Eight Logic Devices, 10 Bit Addressing with 16 Bit Address Decoding
  - 15 Selectable IRQs
  - Three Selectable 8-Bit DMA Channels
  - Three Selectable 16-Bit DMA Channels
  - Supports ISA Card or Motherboard Designs
- Floppy Disk Available on Parallel Port Pins
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible to the 82077AA Using SMC's Proprietary Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - 48 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers Now in Core (Three Mode Drive Support)
  - Swap Drives A & B
  - Non-Burst Mode DMA Option
  - 16 Byte Data FIFO
  - Low Power CMOS 0.8μ Design
- Enhanced Digital Data Separator
  - Low Cost Implementation - 24 MHz Crystal
  - No Filter Components Required
  - Ease of Test and Use, Lower System Cost, and Reduced Board Area
  - 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Supports Floppy Disk Drives and Tape Drives
  - Programmable Precompensation Modes
- Multi-Mode Parallel Port
  - Standard Mode:
    - IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Mode
    - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - High Speed Mode
    - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
  - Incorporates ChiProtect™ Circuitry for Protection Against Damage Due to Printer Power-On
  - Provides Backdrive Current Protection
  - 24 mA Output Drivers
- Serial Ports
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - MIDI Compatible
  - Programmable Baud Rate Generator

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SMC®

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- Modem Control Circuitry
- Infrared - IrDA (HPSIR) and Amplitude Shift Keyed IR (ASKIR)
- Alternate IRRX2 and IRTX2 Pins Optional

Two IDE Interfaces (Four Drive Support)

- On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
- IDE Plug and Play Address Selection

- Supports Four Floppy Drives Directly (Standard and Enhanced Modes)
- General Purpose 10 Bit Plug and Play Selectable Address Decoder with 16 Bit Address Qualification
- Game Port Select Logic, Plug and Play Selectable Base Address
- Serial EEPROM (Optional) Interface
- 160 Pin QFP Package

GENERAL DESCRIPTION

The SMC FDC37C667 Plug and Play Compatible Advanced High Performance Multi-Mode Parallel Port Super I/O Floppy Disk Controller IC utilizes SMC's proven SuperCell™ technology for increased product reliability and functionality. The FDC37C667 is jumper selectable for motherboard applications or for ISA Plug and Play card applications.

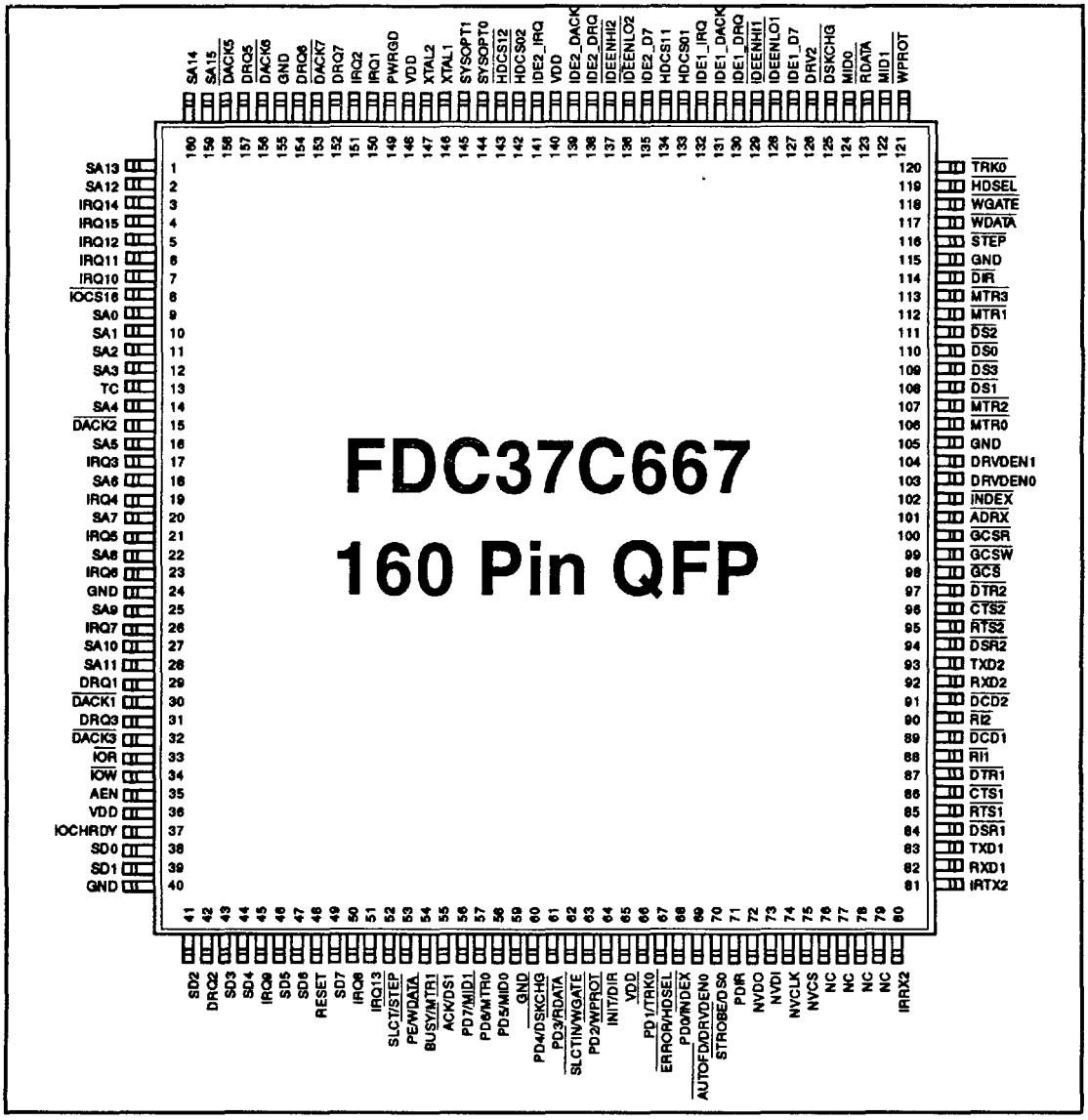
The FDC37C667 consists of eight logical devices: SMC's true CMOS 765B floppy disk controller, two IDE interfaces, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP support, game port chip select, and a general purpose address decoder. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. The parallel port, the IDE interfaces and the game port select logic are compatible with IBM PC/XT and PC/AT architectures, as well as EPP and ECP. The FDC37C667 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C667 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. The FDC37C667 supports 1 Mb/s data rates for vertical recording operation. Use of the SCL feature allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs. The parallel port ChiProtect prevents damage caused by the printer being powered when the FDC37C667 is not powered.

The FDC37C667 does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The FDC37C667 is software and register compatible with SMC's proprietary 82077AA core.

Through internal configuration registers, each of the FDC37C667's logical device's resource requirements may be programmed. The FDC37C667 allows I/O address, DMA channel, and IRQ level and type resources to be programmed, where applicable, for each logical device.

PIN CONFIGURATION



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
		HOST PROCESSOR INTERFACE		
38, 39, 41, 43, 44, 46, 47,49	System Data Bus 0-7	SD[0:7]	I/O24	The data bus connection used by the host microprocessor to transmit data to and from the FDC37C667. These pins are in a high-impedance state when not in the output mode.
9-12, 14, 16, 18, 20, 22, 25, 27, 28, 2, 1, 160, 159	System Address Bus 0-15	SA[0:15]	I	These host address bits determine the I/O address to be accessed during $\overline{IOR}$ and $\overline{IOW}$ cycles. These bits are latched internally by the leading edge of $\overline{IOR}$ and $\overline{IOW}$.
33	$\overline{I/O\ Read}$	$\overline{IOR}$	I	This active low signal is issued by the host microprocessor to indicate a read operation.
34	$\overline{I/O\ Write}$	$\overline{IOW}$	I	This active low signal is issued by the host microprocessor to indicate a write operation.
35	Address Enable	AEN	I	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
29, 42, 31, 157, 154, 152	DMA Request 1-3, 5-7	DRΩ[1:3] DRΩ[5:7]	O24	These active high outputs are the DMA requests for byte transfers of data to the host. These signals are cleared on the last byte of the data transfer by the $\overline{DACK}$ signal going low (or by $\overline{IOR}$ going low if $\overline{DACK}$ was already low as in demand mode).
30, 15, 32, 158, 156, 153	$\overline{DMA\ Acknowledge\ 1\text{-}3, 5\text{-}7}$	$\overline{DACK[1:3]}$ $\overline{DACK[5:7]}$	I	Active low inputs acknowledging the request for a DMA transfer of data. These inputs enable the DMA read or write internally.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
13	Terminal Count	TC	I	This signal indicates to the FDC37C667 that data transfer is complete. TC is only accepted when $\overline{\text{DACK}}$ is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.
150, 151, 17, 19, 21, 23, 26, 50, 45, 7-5, 51, 3, 4	Interrupt Request	IRQ[1:15]	O24	This programmable output indicates that the interrupting device requires servicing. The logical devices can be mapped to the individual IRQx by configuration register 70 and 71.
37	I/O Channel Ready	IOCHRDY	OD24P	In EPP mode, this pin is pulled low to extend the read/write command. This pin has an internal pull-up.
8	$\overline{\text{I/O 16 Bit}}$ $\overline{\text{Indicator}}$	$\overline{\text{IOCS16}}$	I	This input indicates, in AT mode only, when 16 bit transfers are to take place. This signal is generated by the hard disk interface. Logic "0" = 16 bit mode; logic "1" = 8 bit mode.
48	Reset	RESET	IS	This active high signal resets the FDC37C667 and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
		FLOPPY DISK INTERFACE		
123	$\overline{\text{Read Disk Data}}$	$\overline{\text{RDATA}}$	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
118	$\overline{\text{Write}}$ $\overline{\text{Gate}}$	$\overline{\text{WGATE}}$	OD48	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
117	$\overline{\text{Write}}$ $\overline{\text{Data}}$	$\overline{\text{WDATA}}$	OD48	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
119	Head Select	HDSEL	OD48	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
114	Direction Control	DIR	OD48	This high current active low output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
116	Step Pulse	STEP	OD48	This active low high current driver issues a low pulse for each track-to-track movement of the head.
125	Disk Change	DSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
110, 108, 111, 109	Drive Select 0-3	DS[0:3]	OD48	Active low open drain outputs select drives 0-3.
106, 112, 107, 113	Motor On 0-3	MTR[0:3]	OD48	These active low open drain outputs select motor drives 0-3.
103, 104	Drive Density Select 0, 1	DRVDEN0, DRVDEN1	OD48	These outputs are used to control the floppy disk drive. Refer to Table 12 and Table 13.
121	Write Protected	WPROT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
120	Track 0	TRK0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
102	$\overline{\text{Index}}$	$\overline{\text{INDEX}}$	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
124, 122	Media ID0, Media ID1	MID0 MID1	I	In Floppy Enhanced Mode 2, these bits are the Media ID 0,1 inputs. The value of these bits can be read as bits 6 and 7 of the Floppy Tape register.
126	Drive 2	DRV2	I	In PS/2 mode, this input indicates whether a second drive is connected; DRV2 should be low if a second drive is connected. This status is reflected in a read of Status Register A.
		SERIAL PORT INTERFACE		
82, 92	Receive Data	RXD1, RXD2	I	Receiver serial data input.
83, 93	Transmit Data	TXD1 TXD2	O4	Transmitter serial data output
80	IRRX2	IRRX2	1	Alternate IR Receiver for Serial Port 2 data input
81	IRTX2	IRTX2	O4	Alternate IR transmitter for transmit of Serial Port 2 data output
85, 95	$\overline{\text{Request to Send}}$	$\overline{\text{RTS1}}$ $\overline{\text{RTS2}}$	O4	Active low Request to Send output for Primary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{RTS}}$ signal to inactive mode (high). Forced inactive during loop mode operation.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
87, 97	Data Terminal Ready	DTR1 DRT2	O4	Active low Data Terminal Ready output for primary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the DTR signal to inactive mode (high). Forced inactive during loop mode operation.
86, 96	Clear to Send	CTS1, CTS2	I	Active low Clear to Send inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTS signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of CTS.
84, 94	Data Set Ready	DSR1, DSR2	I	Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSR signal by reading bit 5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
89, 91	$\overline{\text{Data Carrier Detect}}$	$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$	I	Active low Data Carrier Detect inputs for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of $\overline{\text{DCD}}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{\text{DCD}}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DCD}}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{\text{DCD}}$.
88, 90	$\overline{\text{Ring Indicator}}$	$\overline{\text{RI1}}$, $\overline{\text{RI2}}$	I	Active low Ring Indicator input for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of $\overline{\text{RI}}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{\text{RI}}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{RI}}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{\text{RI}}$.
PARALLEL PORT INTERFACE				
62	$\overline{\text{Printer Select Input}}$ $\overline{\text{Write Gate}}$	$\overline{\text{SLCTIN}}$ $\overline{\text{WGATE}}$	OD24 OD24P	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register.
64	$\overline{\text{Initiate Output}}$ $\overline{\text{Step Direction}}$	$\overline{\text{INIT}}$ $\overline{\text{DIR}}$	OD24 OD24P	This output is bit 2 of the printer control register. This is used to initiate the printer when low.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
69	$\overline{\text{Autofeed}}$ $\overline{\text{Output}}$	$\overline{\text{AUTOFD}}$	OD24	This output goes low to cause the printer to automatically feed one line after each line is printed. The $\overline{\text{AUTOFD}}$ output is the complement of bit 1 of the Printer Control Register.
	Density Select 0	DRVDEN0	OD24P	
70	$\overline{\text{Strobe Output}}$	$\overline{\text{STROBE}}$	OD24	An active low pulse on this output is used to strobe the printer data into the printer. The $\overline{\text{STROBE}}$ output is the complement of bit 0 of the Printer Control Register.
	$\overline{\text{Drive Select 0}}$	$\overline{\text{DS0}}$	OD24P	
54	Busy	BUSY	I	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
	$\overline{\text{Motor Select 1}}$	$\overline{\text{MTR1}}$	OD24	
55	$\overline{\text{Acknowledge}}$	$\overline{\text{ACK}}$	I	An active low output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the $\overline{\text{ACK}}$ input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
	$\overline{\text{Drive Select 1}}$	$\overline{\text{DS1}}$	OD24	
53	Paper End	PE	I	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
	$\overline{\text{Write Data}}$	$\overline{\text{WDATA}}$	OD24	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
52	Printer Selected Status $\overline{\text{Step}}$	SLCT $\overline{\text{STEP}}$	I OD24	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
67	$\overline{\text{Error}}$ $\overline{\text{Head Select}}$	$\overline{\text{ERROR}}$ $\overline{\text{HDSEL}}$	I OD24	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the $\overline{\text{ERR}}$ input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
68, 66, 63, 61, 60, 58, 57, 56	Port Data	PD[0:7]	I/OP24	The bi-directional parallel data bus is used to transfer information between CPU and peripherals. Refer to Parallel Port Floppy Disk Controller section for floppy disk pin assignments.
71	Port Direction	PDIR	O4	
		IDE1 INTERFACE		
128	$\overline{\text{IDE1 Low Byte Enable}}$	$\overline{\text{IDEENLO1}}$	O4	This active low signal is used in both the XT and AT modes. In the XT and AT modes, this pin is active when the IDE is enabled and the I/O address is accessing a location programmed in IDE1's logical device configuration registers (0x60, 0x63). This signal is active for IDE1 DMA transfers.
129	$\overline{\text{IDE1 High Byte Enable}}$	$\overline{\text{IDEENHI1}}$	O4	This signal is active low only in the AT mode, and when $\overline{\text{IO16CS}}$ is also active. The I/O addresses for which this pin reacts are set according to the Base I/O Address programmed in IDE1's configuration register (0x60, 0x61). In AT mode, this pin is active for IDE1 DMA transfers. This pin is not used in XT mode.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
133	IDE1 Disk Chip Select 0	HDCS01	O24	This is the hard disk chip select corresponding to addresses set according to the Base I/O Address programmed in IDE1's configuration register (0x60, 0x61).
134	IDE1 Disk Chip Select 1	HDCS11	O24	This is the hard disk chip select corresponding to Base Addresses in the IDE1 Logical Device configuration regiser (0x62, 0x63).
132	IDE1 Interrupt Request	IDE1_IRQ	I	This active high input is the interrupt request from IDE1 and is mapped to IRQx as selected by IDE1 configuration registers 70 and 71.
130	IDE1 DMA Request	IDE1_DRQ	I	This active high input is the DMA request from IDe1 and is mapped to DMAx as selected by IDE1 configuration register 74.
131	IDE1 DMA Acknowledge	IDE1_DACK	04	This active low output is the DMA acknowledge to IDE1 and is mapped from DMAx as selected by IDE1 configuration register 74.
127	IDE1 Data Bit 7	IDE[1:7]	I/O24	IDE data bit 7. IDED7 transfers data at I/O addresses selected by the IDE1 Base I/O Address registers (0x60, 0x61) and/or (0x62, 0x63) (read/write). IDED7 should be connected to IDE data bit 7. The FDC37C667 functions as a buffer transferring data bit 7 between the IDE device and the host. During I/O read of the FDC base address +0x07, IDED7 is the FDC disk change bit.
		IDE2 INTERFACE		
136	IDE2 Low Byte Enable	IDEENLO2	O4	This active low signal is used in both the XT and AT modes. In the AT mode, this pin is active when the IDE is enabled and the I/O address is accessing a location programmed in IDE2's Logical Device configuration registers (0x60, 0x61; 0x62, 0x63). This signal is active for IDE2 DMA transfers.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
137	IDE2 High Byte Enable	IDEENHI2	O4	This signal is active low only in the AT mode, and when IO16CS is also active. The I/O addresses for which this pin reacts are IDE2 Logical Device configuration registers (0x60, 0x61). This pin is not used in XT mode.
142	IDE2 Disk Chip Select 0	HDCS02	O24	This is the hard disk chip select corresponding to addresses IDE2 Logical Device configuration registers (0x60, 0x61).
143	IDE2 Disk Chip Select 1	HDCS12	O24	This is the hard disk chip select corresponding to IDE2 Logical Device configuration registers (0x62, 0x63).
141	IDE2 Interrupt Request	IDE2_IRQ	I	This active high input is the interrupt request from IDE2 and is mapped to IRQx as selected by IDE2 configuration registers 70 and 71.
138	IDE2 DMA Request	IDE2_DRQ	I	This active high input is the DMA request from IDE2 and is mapped to DMAx as selected by IDE2 configuration register 74.
139	IDE2 DMA Acknowledge	IDE2_DACK	04	This active low output is the DMA acknowledge to IDE2 and is mapped from DMAx as selected by IDE2 configuration register 74.
135	IDE2 Data Bit 7	IDE[2:7]	I/O24	IDE data bit 7. IDED7 transfers data at I/O addresses selected by the IDE2 Base I/O Address registers (0x60, 0x61) and/or (0x62, 0x63) (R/W). IDED7 should be connected to IDE data bit 7. The FDC37C667 functions as a buffer transferring data bit 7 between the IDE device and the host. During I/O read of the FDC base address +0x07, IDED7 is the FDC disk change bit.
		EEPROM INTERFACE		
74	EEPROM Clock	NV_CLK	04	This output is the clock for the serial EEPROM.
73	EEPROM Data In	NV_DI	I	This input is the Read Data from the serial EEPROM.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
72	EEPROM Data Out	NV_DO	04	This output is the Write Data for the serial EEPROM.
75	EEPROM Chip Select	NV_CS	04	This output is the Chip Select for the serial EEPROM.
MISCELLANEOUS				
149	Power Good	PWRGD	I	This input indicates that the power (V_{DD}) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to the FDC37C667 are disconnected and put in a low power mode, all outputs are put into high impedance. The contents of all registers are preserved as long as V_{DD} has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has a weak pullup resistor to V_{DD}.
98	$\overline{\text{Game Port Chip Select}}$	$\overline{\text{GCS}}$	O4	This is the Game Port Chip Select output - active low. It will assert when the I/O address is 201H.
99	$\overline{\text{Game Port Chip Select Write}}$	$\overline{\text{GCSW}}$	04	This active low output is the Game Port Write. It asserts when the I/O address is 201H and $\overline{\text{IOW}}$ is active.
100	$\overline{\text{Game Port Chip Select Read}}$	$\overline{\text{GCSR}}$	04	This active low output is the Game Port Read. It asserts when the I/O address is 201H and $\overline{\text{IOR}}$ is active.
144	System Option Configuration Input 0	SYSOPT0	I	These jumper inputs are used to configure the FDC37C667 as follows: 1 = PNP-MODE (ISA card for PNP aware system) 0 = STD-MODE (ISA card for non-PNP aware system)

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
145	System Option Configuration Input 1	SYSOPT1	I	These jumper inputs are used to configure the FDC37C667 as follows: If SYSOPT0 = 1: 1 = EEPROM Size = 2K/4Kbit 0 = EEPROM Size = 256 bit/1Kbit If SYSOPT0 = 0: 1 = CONFIG Port Base I/O Address = 0x370 0 = CONFIG Port Base I/O Address = 0x3F0
101	$\overline{\text{Optional I/O Port Address Decode Output}}$	$\overline{\text{ADRx}}$	04	This active low output is the I/O port address decode output. It can be programmed to be active for any single byte or 8 byte block of addresses. This must be externally qualified with a memory or I/O strobe. Refer to Logical Device #7 configuration registers.
146	Clock 1	XTAL1	ICLK	The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
147	Clock 2	XTAL2	OCLK	24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
36, 65, 140, 148	Power	VDD		+5V supply pin.
24, 40, 59, 105, 115, 155	Ground	GND		Ground pin.

BUFFER TYPE DESCRIPTIONS

BUFFER TYPE	DESCRIPTION
I/O24	Input/output. 24 mA sink; 12 mA source.
O24	Output. 24 mA sink; 12 mA source.
OD24	Output. 24 mA sink.
OD24P	Open drain. 24 mA sink; 30 μA source.
OD48	Open drain. 48 mA sink.
O4	Output. 4 mA sink; 2.0 mA source.
OCLK	Output to external crystal
ICLK	Input to Crystal Oscillator Circuit (CMOS levels)
I	Input TTL compatible.
IS	Input with Schmitt Trigger.

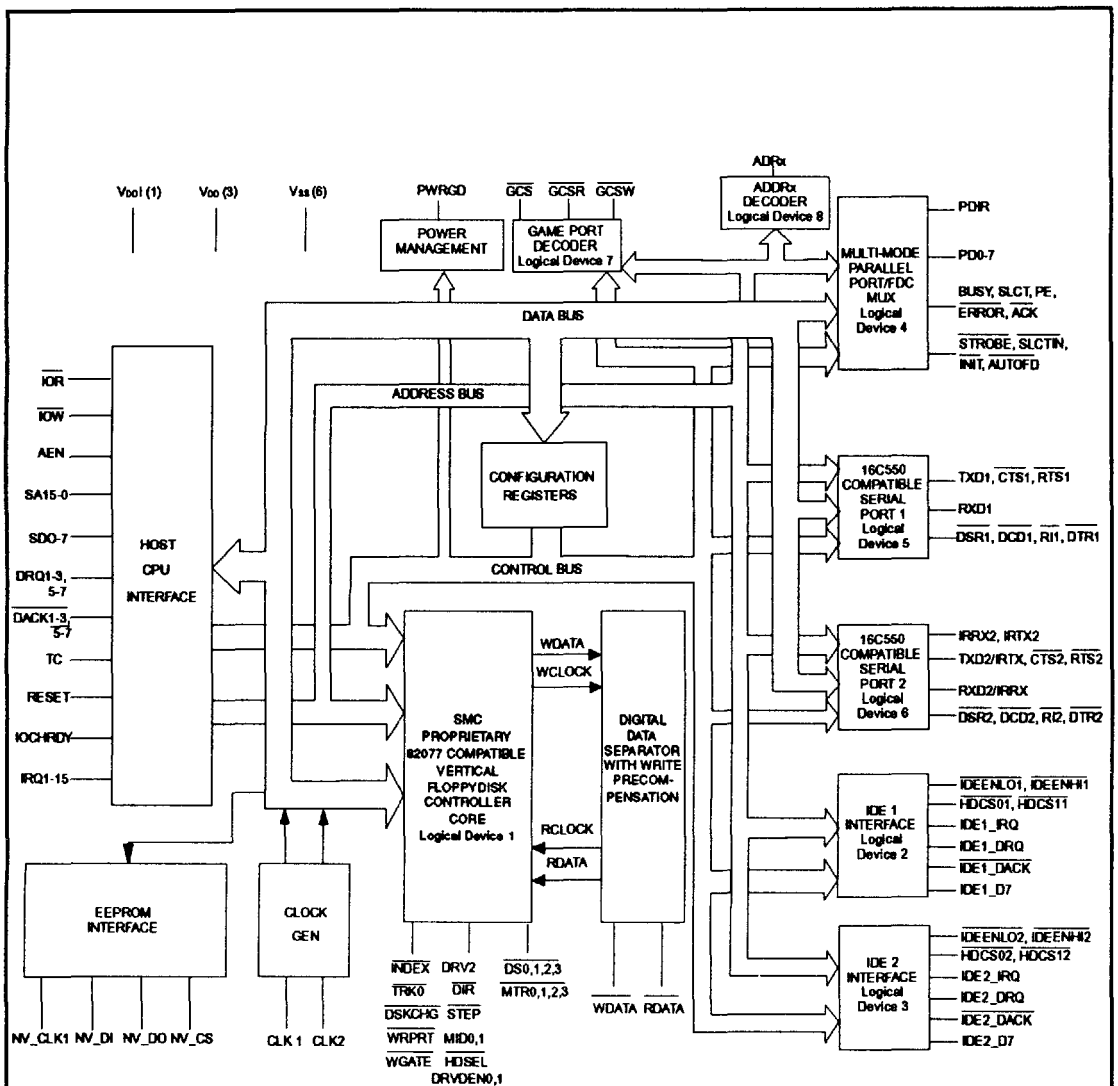


FIGURE 1 - FDC37C667 BLOCK DIAGRAM

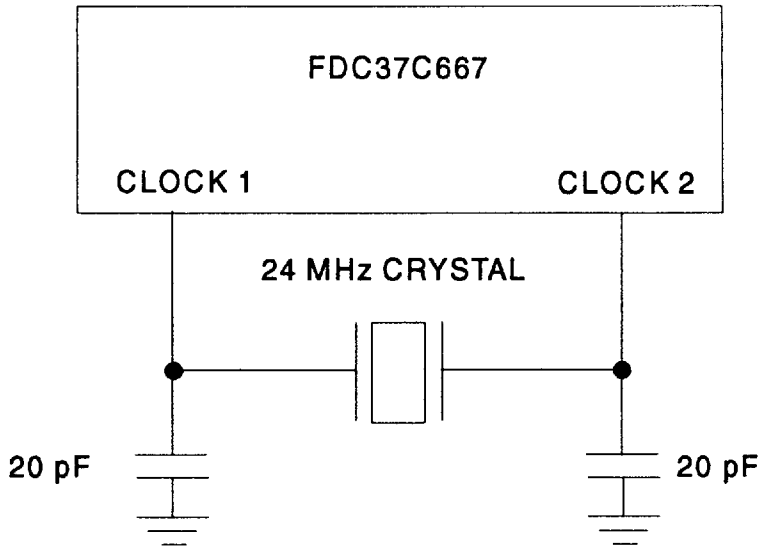


FIGURE 2 - SUGGESTED 24 MHz OSCILLATOR CIRCUIT

PLUG AND PLAY GENERAL DESCRIPTION

PNP-MODE VS. STD-MODE

The FDC37C667 has two modes of operation: PNP-MODE and STD-MODE. SYSOPT0 (pin 144) is strapped "high" to power the FDC37C667 into PNP-MODE and is strapped "low" to power the FDC37C667 into STD-MODE. The PNP-MODE is used for add-in cards and allows a full implementation of Plug and Play protocols. The STD-MODE is used for motherboard designs or to initialize the serial EEPROM. Refer to the Serial EEPROM Interface and Configuration descriptions for more information.

PNP-MODE SEQUENCE OF OPERATION

Refer to Figure 3 for Plug and Play ISA Card State Transitions. The following is an example of the procedure that may be followed to set up the FDC37C667. This is not the only sequence of events that can occur. For any state, any valid command can be received at any time and must have the proper response.

1. At power up or when the RESET_DRV signal is active:
   a. The Card Select Number (CSN) is set to 0x00.
   b. All logical device configuration registers are set to their internal power-on default values and SMC-unique registers are overridden using data read from the Boot Configuration Word.

2. The Linear Feedback Shift Register (LFSR) is reset to its initial state (0x6A).]

3. Enter the Wait for Key state. The FDC37C667 enters this state within 1.5ms from the RESET_DRV or reset command. The initiation key is sent to the FDC37C667. Each value of the initiation key is calculated by shifting the LFSR by one clock for each write and the written data is compared with the calculated (expected) data. In this state the chip will reset the LFSR to 0x6A any time it receives a write to the Address Port that does not match the current value in the LFSR.

4. Once the initiation key is received correctly, the chip enters the Sleep state (the auto configuration ports are enabled).

5. The system sends a WAKE[CSN=0] command to place the chip into the Isolation state.

6. The system sets the RD_DATA port to an address (arbitrary).

7. The system preforms the isolation protocol by performing a sequence of 72 pairs of I/O reads. Refer to 3.3.1 Hardware Protocol in The Proposal for Plug and Play ISA Specification, Version 1.0a, March 24, 1994, by Intel and Microsoft.

8. Assuming that the FDC37C667 wins the isolation protocol, the system sets the CSN to a non-zero value (assigns OUR_CSN) and FDC37C667 enters the Configuration state.

9. System reads the resource data from the FDC37C667.

10. The system places the FDC37C667 into sleep mode by sending a Wake comand with a CSN that does not equal OUR_CSN. While the FDC37C667 is in sleep mode, the system can perform operations on other Plug and Play chips.

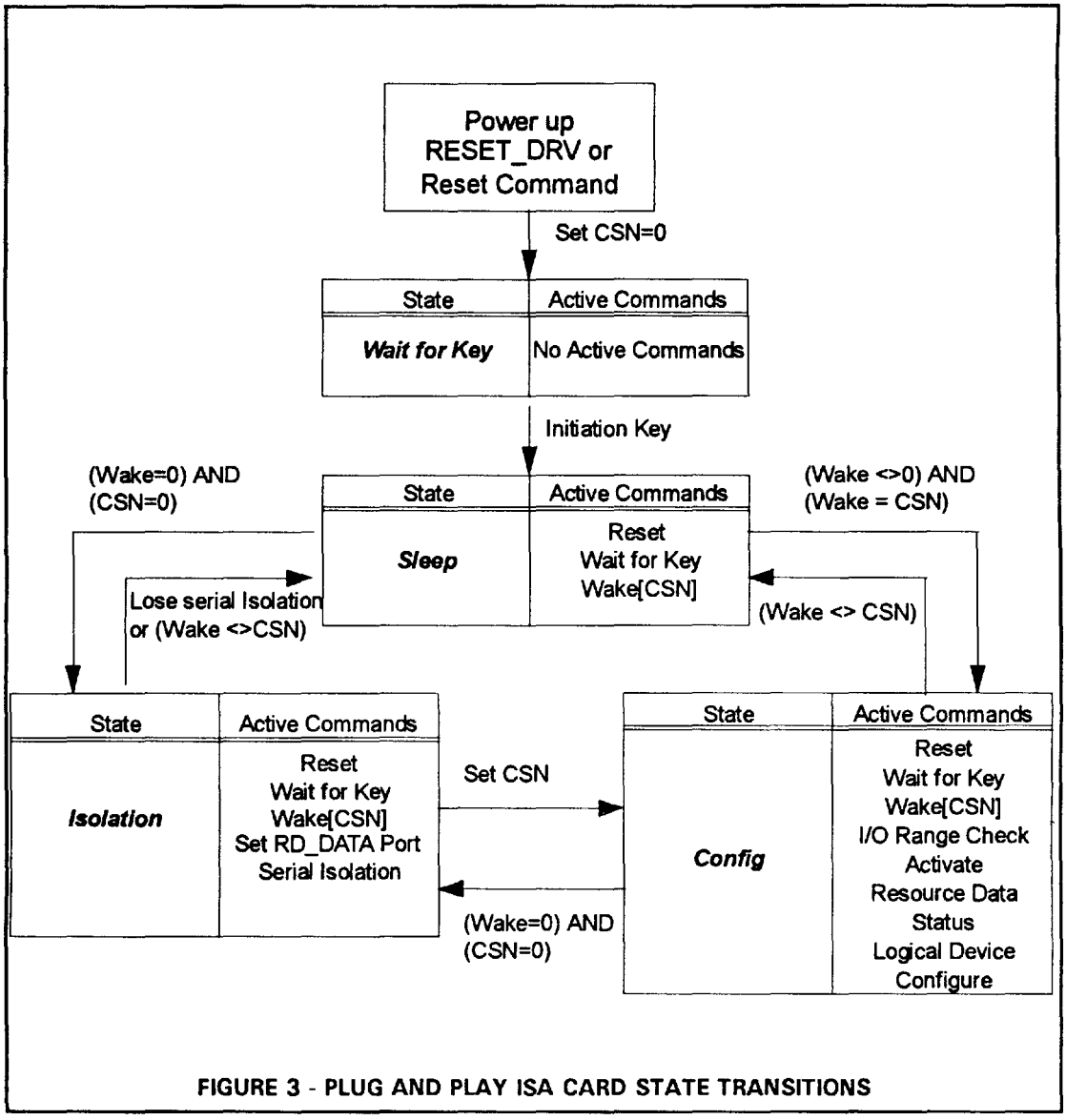


FIGURE 3 - PLUG AND PLAY ISA CARD STATE TRANSITIONS

11. System sends a WAKE[OUR_CSN] command and the FDC37C667 goes back to Configuration state.

12. The system sets the logical device information and activates each of the logical devices.

13. The system sends other commands.

14. The system sends the Wait for Key command and the FDC37C667 returns to the Wait for Key state (the auto configuration ports are disabled).

Notes:

1. On power-up or when the RESET_DRV signal is active, go to step 1.

2. When the Wait for Key command is received, go to step 2.

STD-MODE SEQUENCE OF OPERATION

1. At power-up or when the RESET_DRV signal is active, all logical device configuration registers are set to their internal default state. The Boot Configuration Word is not read from the serial EEPROM as the EEPROM interface powers up disabled.

2. The LFSR is reset to its initial state (0x6A).

3. The FDC37C667 enters the Run state and is ready to be placed into Configuration state. In this state, the LFSR may be reset to 0x6A by writing two consecutive bytes of 0x00 to the configuration port. To place the FDC37C667 into the Configuration State, the Configuration Key is sent to the FDC37C667's configuration port. Each value of the Initiation Key is calculated by shifting the LFSR by one clock for each write and the written data is compared with the calculated (expected) data. In this state, the FDC37C667 will reset the LFSR to 0x6A any time it receives a write to the configuration port that does not match the current value in the LFSR.

4. Once the Initiation Key is received correctly, the next two bytes written to the configuration port define the address location of the index port and place the FDC37C667 into the Configuration state (the auto configuration ports are enabled).

5. The system sets the logical device information and activates desired logical devices through the FDC37C667's index and data ports.

6. The system sends other commands.

7. The system writes 0x02 to the Configuration Control Register and the FDC37C667 returns to the Run state (the auto configuration ports are disabled).

Note: Only two states are defined in the STD-MODE (Run and Configuration). In the Run state, the FDC37C667 will always accept the Configuration Key to its configuration port to enter the Configuration state.

FUNCTIONAL DESCRIPTION

SUPER I/O REGISTERS

The address map, shown below in Table 1, shows the address range and registers for each block (logical devices) of the FDC37C667. A Boot Configuration Word, stored in the external serial EEPROM, is read in Plug and Play Mode to preset the FDC, Serial, Parallel and IDE port resources upon Power on Reset or Reset_Drive. The system resources of the FDC, IDE, serial and parallel ports as well as the decoder base address of the Game and ADRx chip selects can be set via the configuration registers.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C667 through a series of read/write registers. The port address ranges for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register which is 16 bits wide (AT mode). All host interface output buffers are capable of sinking a minimum of 24 mA.

Table 1 - FDC37C667 Logical Device I/O Map

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	BASE I/O RANGE[1]	FIXED BASE OFFSETS
0x00	FDC	[0x100:0x3F8] ON 8 BYTE BOUNDARIES	+0: SRA +1: SRB +2: DOR +3: TSR +4: MSR/DSR +5: FIFO +7: DIR/CCR[2]
0x01	IDE1	[0x100:0x3F8] ON 8 BYTE BOUNDARIES	IDE TASK +0: Data Register (16 Bit) +1: ERRF/WPRE +2: Sector Count +3: Sector Number +4: Cylinder Low +5: Cylinder High +6: Head, Drive +7: Status/Command
		[0x100:0x3FF] ON 1 BYTE BOUNDARIES	IDE MISC AT +0: Status/Fixed Disk

Table 1 - FDC37C667 Logical Device I/O Map

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	BASE I/O RANGE[1]	FIXED BASE OFFSETS
0x02	IDE2	[0x100:0x3F8] ON 8 BYTE BOUNDARIES	IDE TASK +0: Data Register (16 Bit) +1: ERRF/WPRE +2: Sector Count +3: Sector Number +4: Cylinder Low +5: Cylinder High +6: Head, Drive +7: Status/Command
		[0x100:0x3FF] ON 1 BYTE BOUNDARIES	IDE MISC AT +0: Status/Fixed Disk
0x03	PP	[0x100:0x3FC] ON 4 BYTE BOUNDARIES (EPP not supported) or [0x100:0x3F8] ON 8 BYTE BOUNDARIES (all modes supported; EPP is only available when the base address is on an 8-byte boundary)	+0: Data|ecpAfifo +1: Status +2: Control +3: EPP Address +4: EPP Data 0 +5: EPP Data 1 +6: EPP Data 2 +7: EPP Data 3 +400h: cfifo|ecpDfifo|tfifo|cnfgA +401h: cnfgB +402h: ecr
0x04	SP1	[0x100:0x3F8] ON 8 BYTE BOUNDARIES	+0: RB/TB|LSB div +1: IER|MSB div +2: IIR/FCR +3: LCR +4: MCR +5: LSR +6: MSR +7: SCR

Table 1 - FDC37C667 Logical Device I/O Map

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	BASE I/O RANGE[1]	FIXED BASE OFFSETS
0x05	SP2	[0x100:0x3F8] ON 8 BYTE BOUNDARIES	+0: RB/TB|LSB div +1: IER|MSB div +2: IIR/FCR +3: LCR +4: MCR +5: LSR +6: MSR +7: SCR
0x06	Game Port	[0x100:0x3FF] ON 1 BYTE BOUNDARIES	+0: Read/Write Game Port
0x07	ADDRx	[0x100:0x3F8] ON 8 BYTE BOUNDARIES or [0x100:0x3FF] ON 1 BYTE BOUNDARIES	+0 to 7: Read/Write ADDRx or +0: Read/WRite ADDRx

Note 1: The FDC37C667 performs a full 16-bit address decode to access each of its logical devices. In ECP mode, A10 is decoded during ECP operations, but is not needed to set the base address of the parallel port.

Note 2: The FDC, when configured for the AT mode, drives bit D7 only. When configured for PS/2 or Model 30 mode, the FDC will drive the entire byte.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37C667 is compatible to the 82077AA using SMC's proprietary floppy disk controller core.

FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. **The rest of the FDC description assumes that the FDC base I/O address has been programmed to 3F0h.**

Table 2 - Status, Data and Control Registers

FDC BASE ADDRESS		REGISTER	
+0	R	Status Register A	SRA
+1	R	Status Register B	SRB
+2	R/W	Digital Output Register	DOR
+3	R/W	Tape Drive Register	TSR
+4	R	Main Status Register	MSR
+4	W	Data Rate Select Register	DSR
+5	R/W	Data (FIFO)	FIFO
+6		Reserved	
+7	R	Digital Input Register	DIR
+7	W	Configuration Control Register	CCR

For information regarding the floppy disk on parallel port pins, refer to the NVS/OSC/PPFDC Configuration Register (0x23) and the Parallel Port Floppy Disk Controller description.

STATUS REGISTER A (SRA)

Address 3F0 READ ONLY
This register is read-only and monitors the state of the selected FDC IRQ pin and several disk interface pins in PS/2 and Model 30 modes.

The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	$\overline{DRV2}$	STEP	$\overline{TRK0}$	HDSEL	$\overline{INDX}$	$\overline{WP}$	DIR
RESET COND.	0	N/A	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicating inward direction a logic "0" outward.

BIT 1 $\overline{\text{WRITE PROTECT}}$
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicating that the disk is write protected.

BIT 2 $\overline{\text{INDEX}}$
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 $\overline{\text{TRACK 0}}$
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 $\overline{\text{DRV2}}$
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	$\overline{\text{HDSEL}}$	INDX	WP	$\overline{\text{DIR}}$
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 $\overline{\text{DIRECTION}}$
Active low status indicating the direction of head movement. A logic "0" indicating inward direction a logic "1" outward.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicating that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 $\overline{\text{HEAD SELECT}}$
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DRQ output pin.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

STATUS REGISTER B (SRB)

Address 3F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins, in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE
Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	$\overline{DRV2}$	$\overline{DS1}$	$\overline{DS0}$	WDATA F/F	RDATA F/F	WGATE F/F	$\overline{DS3}$	$\overline{DS2}$
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 $\overline{\text{DRIVE SELECT 2}}$
Active low status of the DS2 disk interface output.

BIT 1 $\overline{\text{DRIVE SELECT 3}}$
Active low status of the DS3 disk interface output.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 $\overline{\text{DRIVE SELECT 0}}$
Active low status of the DS0 disk interface output.

BIT 6 $\overline{\text{DRIVE SELECT 1}}$
Active low status of the DS1 disk interface output.

BIT 7 $\overline{\text{DRV2}}$
Active low status of the DRV2 disk interface input.

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	$\overline{\text{RESET}}$	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the four drive selects DS0-DS3, thereby allowing only one drive to be selected at a time.

BIT 2 $\overline{\text{RESET}}$
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode:
Writing this bit to logic "1" will enable the selected DMA channel pins (DRQ, $\overline{\text{DACK}}$, TC), as well as the selected IRQ level pin. The DMA channel and IRQ level are selected in the FDC's logical device IRQ and DMA configuration registers. This bit being a logic "0" will disable the $\overline{\text{DACK}}$ and TC inputs, and hold the DRQ and IRQ outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the selected DMA channel (DRQ, $\overline{\text{DACK}}$, TC) levels are always enabled. During a reset, the DRQ, $\overline{\text{DACK}}$, TC, and FINTR pins will remain enabled, but this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to assert.

BIT 5 MOTOR ENABLE 1
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to assert.

BIT 6 MOTOR ENABLE 2
This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to assert.

BIT 7 MOTOR ENABLE 3
This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output pin to assert.

Table 3 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

This register is included for 82077 software compatability. The robust digital data separator used in the FDC37C667 does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Table 4- Tape Select Bits

TAPE SEL1	TAPE SEL2	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	$\overline{DS3}$	$\overline{DS2}$	$\overline{DS1}$	$\overline{DS0}$	$\overline{MTR3}$	$\overline{MTR2}$	$\overline{MTR1}$	$\overline{MTR0}$
X	X	X	1	0	0	1	1	1	0	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 5}$	$\overline{BIT\ 4}$
X	X	1	X	0	1	1	1	0	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 5}$	$\overline{BIT\ 4}$
X	1	X	X	1	0	1	0	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 5}$	$\overline{BIT\ 4}$
1	X	X	X	1	1	0	1	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 5}$	$\overline{BIT\ 4}$
0	0	0	0	X	X	1	1	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 5}$	$\overline{BIT\ 4}$

Table 6 - Internal 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	$\overline{DS3}$	$\overline{DS2}$	$\overline{DS1}$	$\overline{DS0}$	$\overline{MTR3}$	$\overline{MTR2}$	$\overline{MTR1}$	$\overline{MTR0}$
X	X	X	1	0	0	1	1	0	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 4}$	$\overline{BIT\ 5}$
X	X	1	X	0	1	1	1	1	0	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 4}$	$\overline{BIT\ 5}$
X	1	X	X	1	0	1	0	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 4}$	$\overline{BIT\ 5}$
1	X	X	X	1	1	0	1	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 4}$	$\overline{BIT\ 5}$
0	0	0	0	X	X	1	1	1	1	$\overline{BIT\ 7}$	$\overline{BIT\ 6}$	$\overline{BIT\ 4}$	$\overline{BIT\ 5}$

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are a high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

For this mode, the MID0 and MID1 pins are gated into bits 6 and 7 of the 3F3 register. These two bits are not affected by a hard or soft reset.

BIT 7 MEDIA ID 1 READ ONLY (Pin 122) (See Table 7)

BIT 6 MEDIA ID 0 READ ONLY (Pin 124) (See Table 8)

BITS 5 and 4 DRIVE TYPE ID - These bits reflect two of the bits of the FDC type configuration register (0xF2). Which two bits these are depends on the last drive selected in the Digital Output Register (3F2). (See Table 9)

BITS 3 and 2 FLOPPY BOOT DRIVE - Bits DB3 and DB2 reflect the value of the FDD option configuration register (0xF1) bits 7 and 6 respectively.

Bits 1 and 0 - TAPE DRIVE SELECT (READ/WRITE). Same as in Normal and Enhanced Floppy Mode. 1.

Table 7 - Media ID1

MID1 INPUT	MEDIA ID1 BIT 7	
Pin 122	FDD Option Reg (0xF1) Bit 5 = 0	FDD Option Reg (0xF1) Bit 5 = 1
0	0	1
1	1	0

Table 8 - Media ID0

MID0 INPUT	MEDIA ID0 BIT 6	
Pin 124	FDD Option Reg (0xF1) Bit 4 = 0	FDD Option Reg (0xF1) Bit 4 = 1
0	0	1
1	1	0

Table 9 - Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	FDD Type Reg (0xF2) - Bit 1	FDD Type Reg. (0xF2) - Bit 0
0	1	FDD Type Reg. (0xF2) - Bit 3	FDD Type Reg. (0xF2) - Bit 2
1	0	FDD Type Reg. (0xF2) - Bit 5	FDD Type Reg. (0xF2) - Bit 4
1	1	FDD Type Reg. (0xF2) - Bit 7	FDD Type Reg. (0xF2) - Bit 6

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250kb/s.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 12 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250kb/s after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 10 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

BIT 5 UNDEFINED

Should be written as a logic "0".

BIT 6 LOW POWER

A logic 1 written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Table 10 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY	
	< = 1Mbps	@2Mbps
111	0.00 ns-DISABLED	0.00 ns
001	41.67 ns	20.8 ns
010	83.34 ns	41.7 ns
011	125.00 ns	62.5 ns
100	166.67 ns	83.3 ns
101	208.33 ns	104.2 ns
110	250.00 ns	125 ns
000	Default (See Table 11)	

Table 11 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Table 12 - Data Rates

DRIVE RATE TABLE		DATA RATE		DATA RATE		DENSEL	DRATE	
DRT1	DRT0	Sel 1	Sel 0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended)
00 = Regular drives and 2.88 vertical format
01 = 3-mode drive
10 = 2 meg tape

DENSEL, DRATE1 and DRATE0 map onto output pins DRVDEN0 and DRVDEN1 as shown in Table 13.

Table 13 - DRVDEN Mapping

DT0	DT1	DRVDEN0	DRVDEN1	DRIVE TYPE
0	0	DENSEL	DRATE0	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-Mode)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{DENSEL}}$	DRATE0	
1	1	DRATE0	DRATE1	

MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

BIT 0 - 3 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the result phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 14 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold } \# \times \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\,\mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 14 - FIFO Service Delay

FIFO THRESHOLD	DELAY AT 500	1Mbps	2Mbps
1	14.5ns	6.5ns	2.5ns
2	30.5ns	14.5ns	6.5ns
8	126.5ns	62.5ns	30.5ns
15	238.5ns	118.5ns	58.5ns

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC/AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	$\overline{\text{HIGH}}$ $\overline{\text{DENS}}$
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 $\overline{\text{HIGH DENS}}$
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 12 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 12 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC
This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the pin.

CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY
PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 12 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0"

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
						NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 12 for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0"

The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 15 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 16 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 17 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. Read Data command - the FDC encountered a deleted data address mark. 2. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 18 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are four sources of system reset on the FDC: the RESET pin of the FDC37C667, a reset generated via a bit in the DOR, a reset generated via a bit in the DSR, and a reset generated via a bit in the Configuration Control Register (0x02). At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

RESET Pin (Hardware Reset)

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset, DSR Reset, and Configuration Control Reset (Software Reset)

These three resets are functionally the same. All will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR and Configuration Control resets clear themselves automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence and is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the IDENT and MFM bits 3 and respectively of the FDD Mode configuration register (0xF0).

PC/AT mode - (IDENT high, MFM a "don't care")
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid, the FDC's IRQ and DMA, selected through the logical device configuration registers, can be hi Z, and TC and DENSEL become active high signals.

PS/2 mode - (IDENT low, MFM high)
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care", FINTR and DRQ are always valid if selected through the logical device's configuration register, TC and DENSEL become active low.

Model 30 mode - (IDENT low, MFM low)
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid, FINTR and DRQ can be hi Z, IRQ and DMA channels are selected through the device's configuration register, TC is active high and DENSEL is active low.

DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating the selected FDC DRQ pin during a data transfer command. The FIFO is enabled directly by asserting the FDC's selected $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read With the FIFO enabled, the FDC can perform the above operation by using the new Verify command; no DMA operation is needed.

CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 19 for the command set descriptions.) These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an FDC IRQ or an FDC DRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The FDC's IRQ pin and RQM bit in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The FDC's IRQ pin can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate its IRQ pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The FDC's IRQ pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The FDC's IRQ pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FDC's IRQ pin will also be deactivated if TC and the selected $\overline{\text{DACK}}$ both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC activates the selected DRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate its DRQ pin when the FIFO becomes empty. The DRQ pin goes inactive after $\overline{\text{DACK}}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{\text{IOR}}$, on the last byte, if no edge is present on $\overline{\text{DACK}}$). A data underrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

DMA Mode - Transfers from the Host to the FIFO

The FDC activates its selected DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the $\overline{\text{DACK}}$ and $\overline{\text{IOW}}$ pins and placing data in the FIFO. The DRQ pin remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate its DRQ pin when TC becomes true (qualified by $\overline{\text{DACK}}$), indicating that no more data is required. The DRQ goes inactive after $\overline{\text{DACK}}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{\text{IOW}}$ of the last byte, if no edge is present on $\overline{\text{DACK}}$). A data overrun may occur if the DRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of FDC's IRQ determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CMD BUSY bit is cleared, indicating that the FDC is ready to accept the next command.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 19 for explanations of the various symbols used. Table 20 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 19 - Description of Command Symbols

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>C</td><td>Cylinder Address</td><td>The currently selected address; 0 to 255.</td></tr>
<tr><td>D</td><td>Data Pattern</td><td>The pattern to be written in each sector data field during formatting.</td></tr>
<tr><td>D0, D1,
D2, D3</td><td>Drive Select 0-3</td><td>Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.</td></tr>
<tr><td>DIR</td><td>Direction Control</td><td>If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.</td></tr>
<tr><td>DS0, DS1</td><td>Disk Drive Select</td><td><table><tr><th>DS1</th><th>DS0</th><th>DRIVE</th></tr><tr><td>0</td><td>0</td><td>drive 0</td></tr><tr><td>0</td><td>1</td><td>drive 1</td></tr><tr><td>1</td><td>0</td><td>drive 2</td></tr><tr><td>1</td><td>1</td><td>drive 3</td></tr></table></td></tr>
<tr><td>DTL</td><td>Special Sector Size</td><td>By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.</td></tr>
<tr><td>EC</td><td>Enable Count</td><td>When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).</td></tr>
<tr><td>EFIFO</td><td>Enable FIFO</td><td>This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).</td></tr>
</table>

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The (ap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either tha DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive.
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and $\overline{\text{DACK}}$ signals.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

INSTRUCTION SET

Table 20 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERIFY									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution for Each Sector Repeat:	W	C								Input Sector Parameters
	W	H								
	W	R								
	W	N								
										FDC formats an entire cylinder
Result	R	ST0								Status information after Command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	——— ST0 ———								Status information at the end of each seek operation.
	R	——— PCN ———								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	——— SRT ———				——— HUT ———				
	W	——— HLT ———							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

SEEK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	FIFOTHR				
Execution	W	PRETRK								

RELATIVE SEEK									
PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG									
PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	FIFOTHR				
	R	PRETRK								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								
	R	——— H ———								
	R	——— R ———								Disk status after the Command has completed
	R	——— N ———								

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC37C667 goes into Standby State)
Result	R	——— ST0 ———								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

NOTE: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 21 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 21 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 22.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the $\overline{\text{INDEX}}$ pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 23 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 23, the C or R value of the sector address is automatically incremented (see Table 25).

Table 22 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 23 - Skip Bit vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 24 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 24, the C or R value of the sector address is automatically incremented (see Table 25).

Table 24 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the $\overline{\text{INDEX}}$ pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 25 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

Write Data

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address

Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 13) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 25 and Table 26 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 26 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command.

Table 27 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	22x 4E	12x 00	3x A1	FB F8		R C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA AM	DATA	C	GAP3	GAP 4b
40x FF	6x 00	FC	26x FF	6x 00	FE	Y L	D	E C	O	R C	11x FF	6x 00	FB or F8		R C		

PERPENDICULAR FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	41x 4E	12x 00	3x A1	FB F8		R C		

Table 27 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the $\overline{\text{INDEX}}$ pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the $\overline{\text{TR0}}$ pin from the FDD. As long as the $\overline{\text{TR0}}$ pin is low, the DIR pin remains 0 and step pulses are issued. When the $\overline{\text{TR0}}$ pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the $\overline{\text{TR0}}$ pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN:	Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN:	Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status

An interrupt signal on FDC's selected DRQ pin is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command

2. End of Seek, Relative Seek, or Recalibrate command

3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 28 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status

Sense Drive Status obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining

step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 29. The values are the same for MFM and FM.

Table 29 - Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
..	..	..	.	..	..	..	..	..
E	112	224	373	448	1.0	2	3.33	4
F	120	240	400	480	0.5	1	1.67	2

	HLT			
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
..	..	..	..	.
7F	126	252	420	504
7F	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the selected FDC DRQ pin. Non-DMA mode uses the RQM bit and the selected FDC IRQ pin to signal data transfers.

Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to

one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

DIR	ACTION
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to

calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 30 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes.

The format field shown on page 71 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, an approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown on page 71. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This

enhancement allows data transfers between a Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, and D3 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1". If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 30 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to

their default values. A status byte is returned immediately after issuing a a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

COMPATIBILITY

The FDC37C667 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

PARALLEL PORT FLOPPY DISK CONTROLLER

In this mode, the Floppy Disk Control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in the NVS/OSC/PPFDC Configuration Register (0x23). PPFD1 has only drive 1 on the parallel port pins; PPFD2 has drive 0 and 1 on the parallel port pins.

PPFD1: Drive 0 is on the FDC pins
Drive 1 is on the Parallel port pins
Drive 2 is on the FDC pins
Drive 3 is on the FDC pins

PPFD2: Drive 0 is on the Parallel port pins
Drive 1 is on the Parallel port pins
Drive 2 is on the FDC pins
Drive 3 is on the FDC pins

The following parallel port pins are read as follows by a read of the parallel port register:

1. Data Register (read) = last Data Register (write)
2. Control Register are read as "cable not connected" STROBE, AUTOFD and SLC = 0 and $\overline{INIT}$ = 1;
3. Status Register reads: $\overline{BUSY}$ = 0, PE = 0, SLCT = 0, $\overline{ACK}$ = 1, $\overline{ERR}$ = 1.

The following FDC pins are all in the high impedence state when the PPFDC is actually selected by the drive select register:

1. $\overline{WDATA}$, DENSEL, $\overline{HDSEL}$, $\overline{WGATE}$, $\overline{DIR}$, $\overline{STEP}$, $\overline{DS1}$, $\overline{DS0}$, $\overline{MTR0}$, $\overline{MTR1}$.

2. If PPFDx is selected, then the parallel port cannot be used as a parallel port until "Normal" mode is selected.

The FDC signals are muxed onto the Parallel Port pins as shown in Table 31:

Table 31 - FDC Parallel Port Pins

CONNECTOR PIN #	CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
1	67	$\overline{STB}$	I/O	($\overline{DS0}$)	(0)*
2	65	PD0	I/O	$\overline{INDEX}$	I
3	63	PD1	I/O	$\overline{TRK0}$	I
4	59	PD2	I/O	$\overline{WP}$	I
5	57	PD3	I/O	$\overline{RDATA}$	I
6	56	PD4	I/O	$\overline{DSKCHG}$	I
7	55	PD5	I/O	MID0	I
8	54	PD6	I/O	($\overline{MTR0}$)	(0)*
9	53	PD7	I/O	MID1	I
10	52	$\overline{ACK}$	I	$\overline{DS1}$	0
11	51	BUSY	I	$\overline{MTR1}$	0
12	50	PE	I	$\overline{WDATA}$	0
13	49	SLCT	I	$\overline{WGATE}$	0
14	66	$\overline{ALF}$	I/O	DRVDEN0	0
15	64	$\overline{ERR}$	I	$\overline{HDSEL}$	0
16	62	$\overline{INIT}$	I/O	$\overline{DIR}$	0
17	58	$\overline{SLCTIN}$	I/O	$\overline{STEP}$	0

*These pins are outputs in mode PPFD2; NC in mode PPFD1.

SERIAL PORT (UART)

The FDC37C667 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16550A. The UARTs perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART are also capable of supporting the MIDI data rate. Refer to the FDC37C667 Configuration Registers for information on disabling, power down, changing the base address of the UARTs, and selecting the IRQ channel and type for each UART. The selected interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt.

REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37C667 contains two serial ports, each of which contains a register set as described below.

Table 32 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*NOTE: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)
Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, by setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37C667. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs and to set the RCVR FIFO trigger level. Note: DMA is not supported.

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFO's. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFO's and clears all bytes from both FIFO's. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFO's. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3
Writting to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5
Reserved

Bit 6,7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

INTERRUPT IDENTIFICATION REGISTER (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3
In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5
These bits of the IIR are always logic "0".

Bits 6 and 7
These two bits are set when the FIFO Control Register bit 0 equals 1.

Table 33 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
Bit 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

LINE CONTROL REGISTER (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0
This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic "1", the $\overline{DTR}$ output is forced to a logic "0". When bit 0 is a logic "0", the $\overline{DTR}$ output is forced to a logic "1".

Bit 1
This bit controls the Request To Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that of bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected.
5. The four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, OUT1 and OUT2) are internally connected to the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, RI and DCD) respectively.
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register

is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When a break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the XMIT FIFO and TSR are both empty.

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a

control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the $\overline{DSR}$ input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the $\overline{RI}$ input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to $\overline{RTS}$ in the MCR.

Bit 5
This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)
Address Offset = 7H, DLAB = X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

Table 34 shows the baud rates possible with a 1.8462 MHz crystal.

Effect Of The Reset on Register File

The Reset Function Table (Table 35) details the effect of the Reset input on each of the registers of the Serial Port.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.

D. The data ready bit (LSR bit 0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
   - at least one character is in the FIFO
   - The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
   - The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

   This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and

XMITTER are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

- Bit 0 = 1 as long as there is one byte in the RCVR FIFO.
- Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2 = 0.
- Bit 5 indicates when the XMIT FIFO is empty.
- Bit 6 indicates that both the XMIT FIFO and shift register are empty.
- Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 34 - Baud Rates Using 1.8462 MHz Clock (24 MHz/13)

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2307	0.03
75	1538	0.03
110	1049	0.005
134.5	858	0.01
150	769	0.03
300	384	0.16
600	192	0.16
1200	96	0.16
1800	64	0.16
2000	58	0.5
2400	48	0.16
3600	32	0.16
4800	24	0.16
7200	16	0.16
9600	12	0.16
19200	6	0.16
38400	3	0.16
57800	2	1.6
115200	1	0.16

Table 35 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1-7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4-7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/FCR1*FCR0/ΔFCR0	All Bits Low
XMIT FIFO	RESET/FCR1*FCR0/ΔFCR0	All Bits Low

Table 36 - Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 36 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

NOTES ON SERIAL PORT OPERATION
FIFO MODE OPERATION:

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt.**

This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (115 kbaud).

PARALLEL PORT

The FDC37C667 incorporates an IBM XT/AT compatible parallel port. The FDC37C667 supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the FDC37C667 Configuration Registers for information on disabling, power down, changing the base address of the parallel port, selecting the mode of operation, configuring IRQs, and selecting the DMA channel.

The FDC37C667 also incorporates SMC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

DATA PORTBASE ADDRESS + 00H
STATUS PORTBASE ADDRESS + 01H
CONTROL PORTBASE ADDRESS + 02H
EPP ADDR PORTBASE ADDRESS + 03H

EPP DATA PORT 0BASE ADDRESS + 04H
EPP DATA PORT 1BASE ADDRESS + 05H
EPP DATA PORT 2BASE ADDRESS + 06H
EPP DATA PORT 3BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	Note
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	$\overline{ERR}$	SLCTIN	PE	$\overline{ACK}$	$\overline{BUSY}$	1
CONTROL PORT	STROBE	AUTOFD	$\overline{INIT}$	SLCTIN	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	AD7	2,3
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.
Note 3 : For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 37 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	70	$\overline{\text{Strobe}}$	$\overline{\text{Write}}$	$\overline{\text{Strobe}}$
2-9	68, 66, 63, 61, 60, 58, 57, 56	PData<0:7>	PData<0:7>	PData<0:7>
10	55	$\overline{\text{Ack}}$	Intr	$\overline{\text{Ack}}$
11	54	Busy	$\overline{\text{Wait}}$	Busy, PeriphAck(3)
12	53	PE	(NU)	PError, $\overline{\text{AckReverse}}$(3)
13	52	Select	(NU)	Select
14	69	$\overline{\text{Autofd}}$	$\overline{\text{Datastb}}$	$\overline{\text{AutoFd}}$, HostAck(3)
15	67	$\overline{\text{Error}}$	(NU)	$\overline{\text{Fault}}$(1) $\overline{\text{PeriphRequest}}$(3)
16	64	$\overline{\text{Init}}$	(NU)	$\overline{\text{Init}}$(1) $\overline{\text{ReverseRqst}}$(3)
17	62	$\overline{\text{Selectin}}$	$\overline{\text{Addrstrb}}$	$\overline{\text{SelectIn}}$(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

IBM XT/AT COMPATIBLE, BI-DIRECTIONAL AND EPP MODES

DATA PORT
ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the $\overline{IOW}$ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an $\overline{IOR}$ read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 usec time out has occured on the EPP bus. A logic 0 means that no time out error has occured; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2
Not implemented as register bits. During a read of the Printer Status Register these bits are a low level.

BIT 3 $\overline{ERR}$ - $\overline{ERROR}$
The level on the $\overline{ERROR}$ input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 $\overline{ACK}$ - $\overline{ACKNOWLEDGE}$
The level on the $\overline{ACK}$ input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 $\overline{BUSY}$ - $\overline{BUSY}$
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT
ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the $\overline{\text{STROBE}}$ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the $\overline{\text{AUTOFD}}$ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 $\overline{\text{INIT}}$ - $\overline{\text{INITIATE OUTPUT}}$
This bit is output onto the $\overline{\text{INIT}}$ output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the $\overline{\text{SLCTIN}}$ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit, when set to a high level, may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going $\overline{\text{ACK}}$ input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is valid in extended mode only (PP Mode Register bits [2:0] ≠ 100b). In printer mode, the direction is always out regardless of the state of this bit. In bi-directional mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 AND 7
During a read are a low level and cannot be written.

EPP ADDRESS PORT
ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of $\overline{\text{IOW}}$ causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of $\overline{\text{IOW}}$ latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of $\overline{\text{IOR}}$ causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of $\overline{\text{ADDRSTRB}}$ latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0
ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of $\overline{\text{IOW}}$ causes an EPP DATA WRITE cycle to be performed, the trailing edge of $\overline{\text{IOW}}$ latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of $\overline{\text{IOR}}$ causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the $\overline{\text{IOR}}$ cycle. This register is only available in EPP mode.

EPP DATA PORT 1
ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2
ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP

DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3
ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 OPERATION

When the EPP mode is selected in the PP Mode configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle ($\overline{IOR}$ or $\overline{IOW}$ asserted) to $\overline{WAIT}$ being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the $\overline{WRITE}$ signal to always be asserted.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (ie a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 Write

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. IOCHRDY is driven active low at the start of each EPP write and is released when it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready ($\overline{WAIT}$ is active low) when $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ goes active then the write can complete when $\overline{WAIT}$ goes inactive high.

2. If the EPP bus is ready ($\overline{WAIT}$ is inactive high) then the chip must wait for it to go active low before changing the state of $\overline{DATASTB}$, $\overline{WRITE}$ or $\overline{ADDRSTRB}$. The write can complete once $\overline{WAIT}$ is determined inactive.

Write Sequence of operation

1. The host selects an EPP register, places data on the SData bus and drives $\overline{IOW}$ active.
2. The chip drives IOCHRDY inactive (low).
3. If $\overline{WAIT}$ is not asserted, the chip must wait until $\overline{WAIT}$ is asserted.
4. The chip places address or data on PData bus, clears PDIR, and asserts $\overline{WRITE}$.
5. Chip asserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ indicating that PData bus contains valid information, and the WRITE signal is valid.
6. Peripheral deasserts $\overline{WAIT}$, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
7. a) The chip deasserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.

b) The chip latches the data from the SData bus for the PData bus and asserts (releases) IOCHRDY allowing the host to complete the write cycle.

8. Peripheral asserts $\overline{WAIT}$, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
9. Chip may modify $\overline{WRITE}$ and $\overline{PDATA}$ in preparation for the next cycle.

EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. IOCHRDY is driven active low at the start of each EPP read and is released when it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1. If the EPP bus is not ready ($\overline{WAIT}$ is active low) when $\overline{DATASTB}$ goes active then the read can complete when $\overline{WAIT}$ goes inactive high.

2. If the EPP bus is ready ($\overline{WAIT}$ is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before $\overline{DATASTB}$ goes active. The read can complete once $\overline{WAIT}$ is determined inactive.

Read Sequence of Operation

1. The host selects an EPP register and drives $\overline{IOR}$ active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip tri-states the PData bus and deasserts $\overline{WRITE}$.
5. Chip asserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ indicating that PData bus is tri-stated, PDIR is set and the $\overline{WRITE}$ signal is valid.
6. Peripheral drives PData bus valid.
7. Peripheral deasserts $\overline{WAIT}$, indicating that PData is valid and the chip may begin the termination phase of the cycle.
8. a) The chip latches the data from the PData bus for the SData bus and deasserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$. This marks the beginning of the termination phase.
   b) The chip drives the valid data onto the SData bus and asserts (releases) IOCHRDY allowing the host to complete the read cycle.
9. Peripheral tri-states the PData bus and asserts $\overline{WAIT}$, indicating to the host that the PData bus is tri-stated.
10. Chip may modify $\overline{WRITE}$, PDIR and $\overline{PDATA}$ in preparation for the next cycle.

EPP 1.7 OPERATION

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle ($\overline{IOR}$ or $\overline{IOW}$ asserted) to the end of the cycle $\overline{IOR}$ or $\overline{IOW}$ deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. IOCHRDY is driven active low when $\overline{WAIT}$ is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when $\overline{WAIT}$ is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "0". This asserts $\overline{WRITE}$.
2. The host selects an EPP register, places data on the SData bus and drives $\overline{IOW}$ active.
3. The chip places address or data on PData bus.
4. Chip asserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If $\overline{WAIT}$ is asserted, IOCHRDY is deasserted until the peripheral deasserts $\overline{WAIT}$ or a time-out occurs.
6. When the host deasserts $\overline{IOW}$ the chip deasserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ and latches the data from the SData bus for the PData bus.
7. Chip may modify $\overline{WRITE}$, PDIR and $\overline{PDATA}$ in preparation of the next cycle.

EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. IOCHRDY is driven active low when $\overline{WAIT}$ is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when $\overline{WAIT}$ is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts $\overline{WRITE}$ and tri-states the PData bus.
2. The host selects an EPP register and drives $\overline{IOR}$ active.
3. Chip asserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$ indicating that PData bus is tri-stated, PDIR is set and the $\overline{WRITE}$ signal is valid.
4. If $\overline{WAIT}$ is asserted, IOCHRDY is deasserted until the peripheral deasserts $\overline{WAIT}$ or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts $\overline{WAIT}$, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. When the host deasserts $\overline{IOR}$ the chip deasserts $\overline{DATASTB}$ or $\overline{ADDRSTRB}$.
8. Peripheral tri-states the PData bus.
9. Chip may modify $\overline{WRITE}$, PDIR and $\overline{PDATA}$ in preparation of the next cycle.

Table 38 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
$\overline{\text{WRITE}}$	$\overline{\text{Write}}$	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP.)
WAIT	$\overline{\text{Wait}}$	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	$\overline{\text{Data Strobe}}$	O	This signal is active low. It is used to denote data read or write operation.
RESET	$\overline{\text{Reset}}$	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	$\overline{\text{Address Strobe}}$	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
$\overline{\text{ERR}}$	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output/write condition and a high means an input/read condition. This signal is normally a low (output/write) unless PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.
Note 2: $\overline{\text{Write}}$ is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

EXTENDED CAPABILITIES PARALLEL PORT

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

Vocabulary

The following terms are used in this document:

assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward Host to Peripheral communication.
reverse Peripheral to Host communication.

PWord A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

- PeriphClk, $\overline{\text{Ack}}$
- HostAck, $\overline{\text{AutoFd}}$
- PeriphAck, Busy
- $\overline{\text{PeriphRequest}}$, $\overline{\text{Fault}}$
- $\overline{\text{ReverseRequest}}$, $\overline{\text{Init}}$
- $\overline{\text{AckReverse}}$, PError
- Xflag, Select
- ECPMode, $\overline{\text{SelectIn}}$
- HostClk, $\overline{\text{Strobe}}$

Reference Document

The IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	Note
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	$\overline{\text{Busy}}$	$\overline{\text{Ack}}$	PError	Select	$\overline{\text{Fault}}$	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	$\overline{\text{Init}}$	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	0	0	0	0	0	0	
ecr	MODE			$\overline{\text{ErrIntrEn}}$	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 39 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
$\overline{\text{Strobe}}$	O	During write operations $\overline{\text{Strobe}}$ registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
$\overline{\text{Ack}}$	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with $\overline{\text{AutoFd}}$ in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with $\overline{\text{Strobe}}$ in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with $\overline{\text{Strobe}}$. PeriphAck also provides command information in the reverse direction.
PError ($\overline{\text{AckReverse}}$)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge $\overline{\text{ReverseRequest}}$. It is an "interlocked" handshake with $\overline{\text{ReverseRequest}}$. The host relies upon $\overline{\text{AckReverse}}$ to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
$\overline{\text{AutoFd}}$ (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with $\overline{\text{Ack}}$ in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with $\overline{\text{Ack}}$. HostAck also provides command information in the forward phase.
$\overline{\text{Fault}}$ ($\overline{\text{PeriphRequest}}$)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
$\overline{\text{Init}}$	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and $\overline{\text{SelectIn}}$ is high.
$\overline{\text{SelectIn}}$	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other than those specified is undefined.

Table 40 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.

Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 41 - Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

DATA and ecpAFifo PORT
ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the $\overline{IOW}$ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

DEVICE STATUS REGISTER (dsr)
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 $\overline{Fault}$
The level on the $\overline{Fault}$ input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 $\overline{Ack}$
The level on the $\overline{Ack}$ input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 $\overline{Busy}$
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

DEVICE CONTROL REGISTER (dcr)
ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the $\overline{STROBE}$ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the $\overline{AUTOFD}$ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 $\overline{INIT}$ - $\overline{INITIATE\ OUTPUT}$
This bit is output onto the $\overline{INIT}$ output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the $\overline{SLCTIN}$ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt

requests from the Parallel Port to the CPU due to a low to high transition on the $\overline{ACK}$ input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)
ADDRESS OFFSET = 400h
Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)
ADDRESS OFFSET = 400H
Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)
ADDRESS OFFSET = 400H
Mode = 110
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction

bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)
ADDRESS OFFSET = 400H
Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)
ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrValue
Returns the value on the ISA iRq line to determine possible conflicts.

BITS 5:0 Reserved
These bits reflect the IRQ and DMA selected in the configuration registers and they cannot be written.

IRQ SELECTED	CONFIG REG B BITS 5:3
14	110
13	101
11	100
10	011
9	010
7	001
5	111
All Others	000

DMA SELECTED	CONFIG REG B BITS 2:0
3	011
2	010
1	001
All Others	000

ecr (Extended Control Register)
ADDRESS OFFSET = 402H
Mode = all

This register controls the extended ECP parallel port functions.

BITS 7,6,5
These bits are Read/Write and select the Mode.

BIT 4 $\overline{\text{ErrIntrEn}}$
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of $\overline{\text{Fault}}$.
0: Enables an interrupt pulse on the high to low edge of $\overline{\text{Fault}}$. Note that an interrupt will be generated if $\overline{\text{Fault}}$ is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware, it must be reset

to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

case dmaEn = 1:

During DMA (this bit is set to a 1 when terminal count is reached).

case dmaEn = 0 direction = 0:

This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.

case dmaEn = 0 direction = 1:

This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full

Read only

1: The FIFO cannot accept another byte or the FIFO is completely full.

0: The FIFO has at least 1 free byte.

BIT 0 empty

Read only

1: The FIFO is completely empty.

0: The FIFO contains at least 1 byte of data.

Table 42 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode. In this mode the FIFO is reset and common collector drivers are used on the control lines ($\overline{\text{Strobe}}$, $\overline{\text{AutoFd}}$, $\overline{\text{Init}}$ and $\overline{\text{SelectIn}}$). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in the PP Mode configuration register. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert $\overline{\text{AutoFd}}$ independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction = 0, enabling the drivers.
- Set strobe = 0, causing the $\overline{\text{Strobe}}$ signal to default to the deasserted state.
- Set autoFd = 0, causing the $\overline{\text{AutoFd}}$ signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are not supported in hardware.

Table 43
Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression

The FDC37C667 supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers for $\overline{\text{Strobe}}$, $\overline{\text{AutoFd}}$, $\overline{\text{Init}}$ and $\overline{\text{SelectIn}}$ are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the previous section.) Single byte wide

transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is defined by the mode of the Parallel Port and bit 7 of the PP Mode configuration register.

An interrupt is generated when:

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC is received.

2. For Programmed I/O:
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b. (1) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or a DMA request depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA TRANSFERS

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the Parallel Port's selected DRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests DRQ shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting the selected $\overline{DACK}$ and addresses need not be valid. The Parallel Port's IRQ is generated when a TC is received. DRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, DRQ must be kept unasserted until $\overline{DACK}$ is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller, then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the Parallel Port's DRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the DRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by $\overline{DACK}$), indicating that no more data is required. DRQ goes inactive after $\overline{DACK}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{IOR}$, on the last byte, if no edge is present on $\overline{DACK}$). If DRQ goes inactive due to the FIFO going empty, then DRQ is active again as soon as there is one byte in the FIFO. If DRQ goes inactive due to the TC, then DRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.)

Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the Parallel Port's selected IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold = (16-<threshold>) data bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The Parallel Port IRQ pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The Parallel Port IRQ pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

Two IDE interfaces enable up to four hard disks with embedded controllers (AT and XT) to be interfaced to the host processor. The following definitions are for reference only. These registers are not implemented in the FDC37C667. Access to these registers is controlled by the FDC37C667. For more information, refer to the IDE pin descriptions and the ATA specification.

HOST FILE REGISTERS

The Host File Registers are accessed by the AT Host. There are two groups of registers, the AT Task File, and the Miscellaneous AT Registers.

TASK FILE REGISTERS

Task File Registers may be accessed by the host AT when pin $\overline{\text{HDCS01}}$ or $\overline{\text{HDCS02}}$ is asserted. The Data Register (TASK BASE ADDR +0H) is 16 bits wide; the remaining task file registers are 8 bits wide. The task file registers are ATA and EATA compatible. These registers communicate data, command, and status information with the AT host, and are addressed when $\overline{\text{HDCS0}}$ is low.

MISCELLANEOUS AT REGISTERS

These AT registers may be used by the BIOS for drive control. They are accessed by the AT interface when $\overline{\text{HDSC11}}$ or $\overline{\text{HDCS12}}$ is asserted.

Figure 4 shows the AT Host Register Map of the FDC37C667.

Please refer to the ATA and EATA specifications. These are available from:

Global Engineering
2805 McGaw Street
Irvine, CA 92714
(800) 854-7179
(714) 261-1455

FIGURE 4 - HOST PROCESSOR REGISTER ADDRESS MAP (AT MODE)

ADDRESS	
TASK BASE +0H | TASK BASE +07H	TASK FILE REGISTERS
MISC BASE +0H	MISC AT REGISTERS

COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
RESTORE (RECALIBRATE)	0	0	0	1	r	r	r	r
SEEK	0	1	1	1	r	r	r	r
READ SECTOR	0	0	1	0	D	0	L	T
WRITE SECTOR	0	0	1	1	D	0	L	T
FORMAT TRACK	0	1	0	1	D	0	0	0
READ VERIFY	0	1	0	0	D	0	0	T
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAMETERS	1	0	0	1	0	0	0	1

Bit definitions:

r: specifies the step rate to be used for the command.
D: If set, 16 bit DMA is to be used for the data transfer. (Optional for high performance)
L: If set, the ECC will be transferred following the data.
T: if set, retries are inhibited for the command.

XT MODE

Each IDE interface defaults to AT Mode, but may be programmed for XT Mode by clearing bit 0 of its IDE Mode Register (Configuration Register 0xF0). Under XT Mode, DMA transfers are byte-wide. XT-type IDE drives contain only one set of four contiguous registers, therefore, if an IDE interface is programmed for XT mode, only its primary I/O base address configuration registers (0x60, 0x61) should be set to a valid base address. The secondary I/O base address configuration register (0x62, 0x63) should be set to "0x00".

AT HOST ADDRESSABLE REGISTERS
(For Reference Only)

TASK FILE REGISTERS

ADDR	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
000H	R/W	DATA REGISTER (REDIRECTED TO FIFO)																DATA REG

ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NAME
001H	R	BB	CRC	-	ID	-	AC	TK	DM	ERROR FLAGS
001H	W	CYLINDER NUMBER ÷ 4								WRITE PRECOMP CYLINDER
002H	R/W	NUMBER OF SECTORS								SECTOR COUNT
003H	R/W	SECTOR NUMBER								SECTOR NUMBER
004H	R/W	CYLINDER NUMBER (LSB'S)								CYLINDER LOW
005H	R/W	CYLINDER NUMBER (MSB'S)								CYLINDER HIGH
006H	R/W	-	-	DRIVE		HEAD				HEAD, DRIVE
007H	R	BSY	RDY	WF	SC	DRQ	CD	INDEX	ERR	STATUS
007H	W	COMMAND								COMMAND

MISCELLANEOUS AT REGISTERS

ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NAME
3F6H/ 376H	R	BSY	RDY	WF	SC	DRQ	CD	INDEX	ERR	STATUS
3F6H/ 376H	W	RESERVED				HS3EN	ADPTR RESET	DISABLE IRQ	RE-SERVED	FIXED DISK
3F7H/ 377H	R	-	$\overline{WG}$	$\overline{HS3}$	$\overline{HS2}$	$\overline{HST}$	$\overline{HS0}$	$\overline{DST}$	$\overline{DS0}$	DIGITAL INPUT
3F7H/ 377H	W	-	-	-	-	-	-	-	-	RESERVED

SERIAL EEPROM INTERFACE

The serial EEPROM is used to store the boot configuration word, as well as serial identification and resource data information.

The FDC37C667 must interface with x16 serial EEPROMS compatible with the industry-standard 93C06/93C46/93C56/93C66 family of devices. The FDC37C667 does not support these devices if they are configured to operate in x8 mode.

The host must be able to read the serial EEPROM using the resource data and status registers. The host must be able to write the Serial EEPROM using the program resource data and program status registers. Access to the serial EEPROM through these registers is only possible when in the Configuration State.

STD-MODE

The FDC37C667 should be strapped for STD-MODE for motherboard applications. The FDC37C667 powers-up disabled and is configured by the BIOS. The EEPROM interface powers up disabled, but may be enabled and used to store miscellaneous information.

The FDC37C667 may be strapped for STD-MODE on an ISA card to provide a convienient mechanism for programming the card's serial EEPROM. In the STD-MODE the serial EEPROM interface powers-up disabled. The host can access the serial EEPROM by first putting the FDC37C667 into Configuration Mode and then by setting the NVS bits of Configuration Register 0x23.

PNP-MODE

The FDC37C667 should be strapped for PNP-MODE when on an ISA Card and the serial EEPROM contains valid data. The serial EEPROM interface powers up active and may be configured to operate with a 256/1K bit serial EEPROM or a 2K/4K bit serial EEPROM.

Note: The lower byte of word 5 contains the LFSR generated checksum. Since the FDC37C667 does not perform this checksum in hardware it is necessary that the user/customer calculate and program this value into the EEPROM.

The Resource Data may only be accessed in the Configuration State. The FDC37C667 may enter the Configuration State by either winning the Serial Isolation Protocol and having a CSN assigned or in response to receiving a WAKE[CSN] command that matches the FDC37C667's assigned CSN. In the first case, the FDC37C667 finds itself in the Configuration State having already accessed the nine serial ID bytes. Therefore, the first read of the Resource Data Register will return resource data. In the latter case, the FDC37C667 finds itself in the Configuration State with the serial device pointer reset and pointing to word 1. The Serial ID is read byte-wise through the Resource Data Register. The host will read nine bytes for the Serial ID. The checksum is not considered valid when read in this manner. The tenth read of the Resource Data Register will return the first byte of resource data

Note: Resource data should always be returned immediately after the serial ID. Any zeros between the serial ID and the resource data would be interpreted by the system as meaning the card's resource data is invalid.

EEPROM DATA FORMAT

The EEPROM is used to store the boot configuration word, the serial ID, and the resource data as shown in Table 44. The serial identifier and resource data are defined in Section 6 the Proposal for Plug and Play ISA

Specification, Version 1.0a, March 24, 1994, by Intel and Microsoft. The following resource data structure is provided as an example. The FDC37C667 does not need to interpret the serial ID or resource data, but only read it from the EEPROM (in sequential order) and pass it to the system.

Table 44 - EEPROM Data Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDD Control		IDE1 Control		IDE2 Control		PP ADDR		PP MODE		SP1 ADDR		SP2 ADDR		Config Override	
VENDOR ID							BYTE 1	VENDOR ID							BYTE 0
VENDOR ID							BYTE 3	VENDOR ID							BYTE 2
SERIAL NUMBER							BYTE 3	SERIAL NUMBER							BYTE 0
SERIAL NUMBER							BYTE 3	SERIAL NUMBER							BYTE 2
LOGICAL DEVICE 0 ID							0	CHECKSUM							BYTE 0
LOGICAL DEVICE 0 ID							BYTE 2	LOGICAL DEVICE 0 ID							BYTE 1
LOGICAL DEVICE 0 ID							BYTE 4	LOGICAL DEVICE 0 ID							BYTE 3
DEVICE 0 RESOURCE							BYTE 0	LOGICAL DEVICE 0 ID							BYTE 5
DEVICE 0 RESOURCE							BYTE 2	DEVICE 0 RESOURCE							BYTE1
DEVICE 0 RESOURCE							BYTE 4	DEVICE 0 RESOURCE							BYTE 3
							0								
							0								
DEVICE 0 RESOURCE							BYTE m	DEVICE 0 RESOURCE							BYTE m-1
LOGICAL DEVICE 1 ID							BYTE 1	LOGICAL DEVICE 1 ID							BYTE 0
LOGICAL DEVICE 1 ID							BYTE 3	LOGICAL DEVICE 1 ID							BYTE 2
LOGICAL DEVICE 1 ID							BYTE 5	LOGICAL DEVICE 1 ID							BYTE 4
DEVICE 1 RESOURCE							BYTE 1	DEVICE 1 RESOURCE							BYTE 0
							0								
							0								
END TAG							BYTE 0	DEVICE 1 RESOURCE							BYTE n
XXXXX							XXXXX	END CHECK SUM							BYTE 1

NOTE : Resource Data Fields are not required to start on even byte boundaries, rather they are expected to be contiguous.

BOOT CONFIGURATION WORD (BCW - Word 0)

When the FDC37C667 is strapped for PNP-MODE, the FDC37C667 always reads the serial EEPROM's BCW stored at address 0x00 (word 0) regardless of whether the system is PNP-AWARE or not. The format for the Boot Configuration Word is as follows. Note: If a logical device is set disabled in the Boot Configuration Word then no resources are assigned (IRQ, DMA, Base I/O Address) and its activate bit is not set.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDD Control		IDE1 Control		IDE2 Control		PP ADDR		PP MODE		SP1 ADDR		SP2 ADDR		Config Override	

default IRQ type is edge high

BITS[15:14]: FDD CONTROL
[0,0] = Disabled
[0,1] = Disabled
[1,0] = Base I/O at 0x370
[1,1] = Base I/O at 0x3F0

Interrupt Level = IRQ6 --,
DMA Request = DRQ2 |---- if not Disabled
DMA Ack = DACK2 --'

BITS[13:12]: IDE1 CONTROL
[0,0] = Disabled
[0,1] = Disabled
[1,0] = Base I/O Address TASK at 0x170, MISC AT at 0x376, IRQ15
[1,1] = Base I/O Address TASK at 0x1F0, MISC AT at 0x3F6, IRQ14

BITS[11:10]: IDE2 CONTROL
[0,0] = Disabled
[0,1] = Disabled
[1,0] = Base I/O Address TASK at 0x1F0, MISC AT at 0x3F6, IRQ14
[1,1] = Base I/O Address TASK at 0x170, MISC AT at 0x376, IRQ15

BITS[9:8]: Parallel Port Address
[0,0] = Disabled
[0,1] = Base I/O Address at 0x3BC
[1,0] = Base I/O Address at 0x378
[1,1] = Base I/O Address at 0x278

BITS[7:6]: Parallel Port Mode
[0,0] = Printer Mode - IRQ7
[0,1] = Printer Mode - IRQ5
[1,0] = SPP (Bi-Directional) - IRQ 7
[1,1] = SPP (Bi-Directional) - IRQ 5

BITS[5:4]: Serial Port 1 Address
[0,0] = Disabled
[0,1] = Base I/O Address at 0x3E8 (COM3) - IRQ 4
[1,0] = Base I/O Address at 0x2F8 (COM2) - IRQ 3
[1,1] = Base I/O Address at 0x3F8 (COM1) - IRQ 4

BITS[3:2]: Serial Port 2 Address
[0,0] = Disabled
[0,1] = Base I/O Address at 0x2E8 (COM4) - IRQ 3
[1,0] = Base I/O Address at 0x3F8 (COM1) - IRQ 4
[1,1] = Base I/O Address at 0x2F8 (COM2) - IRQ 3

BITS[1:0]: Config Override
This bit field is used to provide the system with an alternate way of accessing the FDC37C667's internal Configuration registers when the FDC37C667 is strapped for PNP-MODE.

[0,0] = PNP Only
[0,1] = PNP Only
[1,0] = PNP or CONFIG PORT at I/O address 0x3F0.
[1,1] = PNP or CONFIG PORT at I/O address 0x370.5.

CONFIGURATION

The Plug-N-Play system for the Super I/O consists of the following:

PRIMARY ADDRESS DECODER

The FDC37C667 will be expected to power up in **PNP-MODE** or **STD-MODE** depending on the configuration of the System Configuration Pin, SYSOPT0. SYSOPT1 is used to select options under each basic mode (see System Configuration Table).

PNP-MODE means that the chip implements the full PNP protocol as outlined in the Proposal for Plug and Play ISA Specification Version 1.0a, March 24, 1994, by Intel and Microsoft and the PNP-MODE Sequence of Operations section in this data sheet.

STD-MODE means that the FDC37C667 implements only a subset of the PNP specification. The device does not need to be isolated and assigned a CSN in order to configure the device. The FDC37C667 does not participate in the Wait-for-Key State, the Isolation protocol, nor does it respond to Wake[CSN] commands. The FDC37C667 runs in only the Run State or in the Configuration State. Under STD-MODE all logical devices on the FDC37C667 power-up disabled (the internal default values).

Table 45 - System Configuration Table

SYSOPT0	SYSOPT1	CHIP IS CONFIGURED FOR	
		ENVIRONMENT	OPTIONS
0	0	1. Motherboard designs. 2. ISA Card with invalid EEPROM. Allows user to program EEPROM using SMC supplied utility program. In this mode the serial EEPROM interface is activated when the NVS bits of Configuration Register 0x23 are properly set. 3. ISA Card with no EEPROM. System equipped with a BIOS extension or device driver.	STD-MODE: CONFIG PORT I/O Address = 0x3F0. On power up, the device is fully disabled and makes no attempt to read the Boot Configuration Word from the Serial EEPROM.
0	1	Same configurations as above.	STD-MODE: Same as above except the CONFIG PORT I/O address = 0x370.
1	0	ISA Card with valid EEPROM.	PNP-MODE: Full PNP, serial ID and Configuration Data stored in 256 or 1K bit serial EEPROM.
1	1	ISA Card with valid EEPROM.	PNP-MODE: Full PNP, serial ID and Configuration Data stored in 2K or 4K bit serial EEPROM.

Note: The SYSOPT pins are latched on the falling edge of the RESET_DRV or on Power On Reset.

Table 46 - PNP-Mode Ports

PORT NAME	LOCATION	TYPE
Address (AP)	0x0279	Write-Only
Write_Data	0x0A79	Write-Only
Read_Data	Relocatable (0x0203 -0x03FF)	Read-Only

PNP-Mode

This mode is recommended for use on an ISA card with valid EEPROM data in either a PNP-aware or a non-PNP-aware system (the SYSOPT1 pin is used to select the serial EEPROM size). In this case the three main PNP interface registers are decoded. This block is used to generate the address decodes for the Address Port, Write_Data Port and Read_Data Strobe. This block may also contain the Read_Data Port register required to generate the Read_Data Strobe. 16 bit accesses (assertion of $\overline{IOCS16}$) to these ports are not supported.

The 8-bit address written to the Address (AP) Port points to the FDC37C667's Control or Configuration register which is then written through the Write_Data Port and read through the Read_Data Port.

Table 47 - STD-Mode Ports

PORT NAME	SYSOPT1 = 0	SYSOPT1 = 1	TYPE
Configuration Port	0x03F0	0x0370	Write
Index Port	Relocatable (0x00 - 0x3FE)		Write
Data Port	Relocatable INDEX PORT + 1		Read/Write

STD-Mode

This mode is recommended for use on a motherboard or for use on an ISA card with either an invalid EEPROM or no EEPROM. In this case the FDC37C667 always powers-up disabled and is configurable through two standard Configuration I/O Ports (Index and Data). The SYSOPT1 pin is now used to select the Configuration Port's power up I/O address.

All I/O addresses are qualified with AEN and 16 bit accesses (assertion of $\overline{IOCS16}$) to these ports are not supported.

The Index and Data Ports are effective only when the FDC37C667 is in the Configuration State (these ports are undefined at power-up). In the Configuration State, the 8-bit address written to the Index Port points to the FDC37C667's Control or Configuration Register which is then written or read through the Data Port.

The FDC37C667 enters the Configuration State and sets the location of the Index Port and Data Port when the following Configuration Key is successfully written to the Configuration Port. Entering the Configuration State will also reset the Serial Device Pointer to zero.

Config Key = < 0x00,0x00,the Initiation Key Sequence,MSB_I,LSB_I>

The Initiation Key Sequence is a 32 byte sequence defined on page 53 of the Proposal for Plug and Play ISA Specification and is shown below :

Initiation Key Sequence = <0x6A, 0xB5, 0xDA, 0xED, 0xF6, 0xFB, 0x7D, 0xBE, 0xDF, 0x6F, 0x37, 0x1B, 0x0D, 0x86, 0xC3, 0x61, 0xB0, 0x58, 0x2C, 0x16, 0x8B, 0x45, 0xA2, 0xD1, 0xE8, 0x74, 0x3A, 0x9D, 0xCE, 0xE7, 0x73, 0x39>

MSB_I: the most significant byte of the Index Port location.

LSB_I: the least significant byte of the Index Port location. This is forced to reside on even boundaries (the least significant bit is truncated and forced to zero).

Configuration Override

The FDC37C667, strapped for PNP-MODE, may be placed directly from the Wait-for-Key State into the Configuration State by writing the Configuration Key to the Configuration Port selected through bits[1:0] of the Boot Configuration Word. This provides an alternate mechanism for accessing the FDC37C667's internal configuration registers.

Once the Init Key sequence has begun to the Address Port or the Configuration Key sequence has begun to the BCW-selected Configuration Port, the sequence must be completed to that port; writes to the alternate port will be ignored.

A new Init Key or Configuration Key sequence may begin:

1) after receiving an incorrect Init Key sequence
2) after receiving an incorrect Configuration Key sequence
3) after a hardware RESET or POR
4) after bit-1 of the Configuration Control Register is set.

When the Configuration State is entered by writing the Configuration Key to the Configuration Port, the FDC37C667 directly enters the Configuration State and follows the STD-MODE defined protocol until the Configuration State is left putting the device back into the Wait-for-Key State.

Table 48 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS				
0x00	W	n/a	n/a	set RD_DATA Port
0x01	R	n/a	n/a	Serial Isolation
0x02	W	0x00	0x00	Config Control
0x03	W	n/a	n/a	Wake[CSN]
0x04	R	n/a	n/a	Resource Data
0x05	R	n/a	n/a	Status
0x06	R/W	0x00	n/a	Card Select Number
0x07	R/W	0x00	0x00	Logical Device Number
0x20	R	0x01	0x01	Device ID - hard wired

Table 48 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
0x21	R	0x01	0x01	Device Rev - hard wired
0x22	R/W	0x00	n/a	Power Control
0x23	R/W	0x08	n/a	NVS/OSC/PPFDC
0x24	R/W	0x00	0x00	Serial EEPROM Pointer
0x25	W	n/a	n/a	Program Resource Data
0x26	bits[6:0] R bit[7] R/W	0x03	0x03	Write EEPROM Status
0x2F	R/W	TBD	n/a	TEST
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDC)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address
0x61	R/W	0x00	0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Level
0x71	R/W	0x02	0x02	Primary Interrupt Type
0x74	R/W	0x04	0x04	DMA channel Select
0xF0	R/W	0x0E	n/a	FDD Mode Register
0xF1	R/W	0x00	n/a	FDD Option Register
0xF2	R/W	0xFF	n/a	FDD Type Register
0xF3	R/W	0x00	0x00	Reserved, read always as 0
0xF4	R/W	0x00	n/a	FDD0
0xF5	R/W	0x00	n/a	FDD1
0xF6	R/W	0x00	n/a	FDD2
0xF7	R/W	0x00	n/a	FDD3
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (IDE1)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0x62, 0x63	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Level

Table 48 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
0x71	R/W	0x02	0x02	Second Interrupt Type
0x74	R/W	0x04	0x04	DMA channel Select
0xF0	R/W	0x01	n/a	IDE1 Mode Register
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (IDE2)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0x62	R/W	0x00	0x00	Second Base I/O Address Addr(9:8)
0x63	R/W	0x00	0x00	Second Base I/O Address Addr(7:0)
0x70	R/W	0x00	0x00	Primary Interrupt Level
0x71	R/W	0x02	0x02	Primary Interrupt Type
0x74	R/W	0x04	0x04	DMA channel Select
0xF0	R/W	0x01	n/a	IDE2 Mode Register
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Parallel Port)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0x70	R/W	0x00	0x00	Primary Interrupt Level
0x71	R/W	0x02	0x02	Primary Interrupt Type
0x74	R/W	0x04	0x04	DMA channel Select
0xF0	R/W	0x3C	n/a	Parallel Port Mode Register
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Serial Port 1)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0x70	R/W	0x00	0x00	Primary Interrupt Level
0x71	R/W	0x02	0x02	Primary Interrupt Type
0xF0	R/W	0x00	n/a	Serial Port 1 Mode Register

Table 48 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Serial Port 2)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0x70	R/W	0x00	0x00	Primary Interrupt Level
0x71	R/W	0x02	0x02	Primary Interrupt Type
0xF0	R/W	0x00	n/a	Serial Port 2 Mode Register
0xF1	R/W	0x00	n/a	SP2IR Register
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (Game Port)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (ADDRx)				
0x30	R/W	0x00	0x00	Activate
0x31	R/W	0x00	0x00	I/O Range Check
0x60	R/W	0x00	0x00	Primary Base I/O Address Addr(9:8)
0x61	R/W	0x00	0x00	Primary Base I/O Address Addr(7:0)
0xF0	R/W	0x00	n/a	ADDRx Mode Register

PRIMARY REGISTER DECODER [0x00-0x2F]

The card-level registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the Address Port for register selection. All un-implemented registers and bits ignore writes and return zero when read.

PNP-Mode

The Address Port (AP) latch is used to select a primary (card-level) register in the FDC37C667. The Write_Data and Read_Data registers are then used to access the selected register. The last column of Table 49 indicates the states in which each register is accessible. (S = Sleep, I = Isolation, C = Configure). When a register is not accessible, then attempts to access it will have no effect on that register.

STD-Mode

The Index Port latch is used to select a primary (card-level) register in the FDC37C667. The Data Port register is then used to access the selected register. These registers are accessable only in the Configuration State.

Table 49 - Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
		CARD/CHIP CONTROL	
PNP-MODE: set Read_ Data Port Default = the Read_ Data Port is considered unimplemented until set through this register	0x00 W	Stores address of the read data register. Bits 7:0 become addresses [9:2] -- addresses [1:0] are "11b" and addresses [11:10] are "00b". This register can only be written to when the FDC37C667 is in the Isolation state.	I
PNP-MODE: Serial Isolation	0x01 R	A read of this register causes a card in the Isolation state to compare one bit of the board's ID. 72 pairs of I/O reads are performed on this register for each pass of the PNP Serial Isolation protocol.	I
PNP-MODE: Configuration Control Refer to Table 48 for full description. Default = 0x00	0x02 W	The hardware automatically clears these bits after the write, there is no need for software to clear the bits. Bit 0 = 1: Reset all logical devices and restores non-vendor unique configuration registers to their power-up default values. The CSN, Read_Data Port and PNP state are preserved. Bit 1 = 1: Return to the Wait for Key state. CSN is preserved and all logical devices are not affected. Bit 2 = 1: Reset CSN to 0 Note: If 0x03 is written to this register, the logical devices are reset, the CSN and Read_Data Port are retained, and the FDC37C667 enters the Wait for Key state. A write of 0x07 is equivalent to a RESET_DRV, however note that SMC (vendor) unique configuration registers are not reset.	S, I, C
STD-MODE: Configuration Control Refer to Table 48 for full description. Default = 0x00	0x02 W	The hardware automatically clears these bits after the write, there is no need for software to clear the bits. Bit 0 = 1: Reset all logical devices and restores non-vendor unique configuration registers to their internal power-up values. Bit 1 = 1: Leave Configuration Mode. Logical devices are not affected. Note: A write of xxxxxx11b is equivalent to a RESET_DRV, however note that SMC (vendor) unique configuration registers are not reset.	C

Table 49 - Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
PNP-MODE: Wake[CSN]	0x03 W	[7:0] are significant. A write to this port causes all cards that have a CSN that matches the write data [7:0] to go from the Sleep state to either the Isolation state if CSN=0 or the Configuration state if CSN>0. Any cards with a CSN that does not match the write data [7:0] will enter the Sleep state. This command also resets the pointer to the start of the serial identifier.	S, I, C
Resource Data	0x04 R	A read from this register reads the next byte of resource information and resets bit 0 of the Status Register. The Status Register, bit-0, must be polled before reading this register. Note: the Serial Device Pointer is auto-incremented following each pair of Resource Data register reads.	C
Status	0x05 R	Bit 0 = 1 indicates that data in the Resource Data Register is valid. This bit is cleared when Resource Data is read until the next byte is valid. Reading the Resource Data Register when bit-0 is clear will have no detremental effects; the data will simply be invalid.	C
PNP-MODE : Card Select # Default = 0x00	0x06 R/W	A write to this register sets the card's CSN. This register may be written to when in the Configuration State or after completing and winning the Isolation protocol. After winning the Isolation protocol, the FDC37C667 will remain in the Isolation state until a CSN is assigned to the FDC37C667. Note: the host CPU should not set the CSN to zero through this register. This register may be read only when the device is in the Configuration Mode.	I, C
Logical Device # Default = 0x00	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: the I/O range check and activate commands operate only on the selected logical device.	C
Card Level Reserved	0x08-0x1F	Reserved for future use (not used).	C
CARD/CHIP LEVEL, SMC DEFINED			
Device ID Hard wired = 0x01	0x20 R	A read only register which provides device identification. Bits[7:0] = 0x01 when read	C

Table 49 - Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Device Rev Hard wired = 0x01	0x21 R	A read only register which provides device revision information. Bits[7:0] = 0x01 when read	C
Power/Control Default = 0x00. on POR or Reset_Drv hardware signal.	0x22 R/W	Bit[0] : FDC Power Bit[1] : IDE1 Enable Bit[2] : IDE2 Enable Bit[3] : Parallel Port Power Bit[4] : UART 1 Power Bit[5] : UART 2 Power Bit[6] : Game Port Enable Bit[7] : Addrx Enable = 0 Power off or disabled = 1 Power on or enabled	C
NVS/OSC/PPFDC Default = 0x08, on POR or Reset_Drv hardware signal. if strapped for the PNP-Mode the NVS [5:4] bits are set to match the SYSOPT [0:1] pins and are read only	0x23 R/W	Bits[1:0] : PPFDC - muxed PP/FDC control = 00 Normal Parallel Port = 01 PPFD1 - Drive 0 is on the FDC pins Drive 1 is on the PP pins Drive 2 is on the FDC pins Drive 3 is on the FDC pins = 10 PPFD1 - Drive 0 is on the PP pins Drive 1 is on the PP pins Drive 2 is on the FDC pins Drive 3 is on the FDC pins Bits[3:2] : OSC = 01: Osc is on, BRG clock is on when PWRGD is active. When PWRGD is inactive, Osc is off and BRG clock is disabled (default). = 10: Same as above (01) case. = 00: Osc is on, BRG Clock enabled. = 11 Osc is off, BRG clock is disabled. Bits[5:4] : NVS These bits may be read in either PNP or STD-MODE, but are writable only when the device is configured for STD-MODE. These bits are set by a utility program to enable access to the serial EEPROM. = 0X No EEPROM present = 10 256/1K bit EEPROM present = 11 2K/4K bit EEPROM present Bit [7:6] : Reserved, set to zero	C

Table 49 - Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Serial Device Pointer Default = 0x00, on POR, Reset_Drv or Software Reset.	0x24 R/W	Use this register to set the Serial EEPROM's pointer. The value in this register always reflects the current EEPROM pointer address. The Serial Device Pointer increments after each pair of reads from the Resource Data Register or after each pair of writes to the Program Resource Data Register. Note: In STD-mode, just after entering Config State or programming the NVS bits, this pointer must be explicitly written in order to cause the serial EEPROM controller to fetch a word of data from the EEPROM.	C
Program Resource Data	0x25 W	This register is used to program the serial device from the host. This device supports serial EEPROMs in x16 configurations. Two bytes must be written to this register in order to generate a EEPROM write cycle. The LSB leads the MSB. The first write to this register resets bit 0 of the Program Status Register. The second write resets bit 1 of the Program Status Register and generates a write cycle to the Serial EEPROM. Next the Serial Device Pointer is auto incremented. The Program Status Register must be polled before performing a pair of writes to this register.	C

Table 49 - Global Configuration Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Program Status Default = 0x03, on POR, Reset_Drv or Software Reset.	0x26 Bit[6:0] Read Only Bit[7] R/W	Bits [1:0]: = 1,1 Indicates that the Program Resource Data register is ready to accept a pair of bytes. = 1,0 Bit 0 is cleared on the first write of Program Resource Data Register. This status indicates that the serial device controller has received one byte (LSB) and is waiting for the second byte (MSB). = 0,0 Bit 1 is cleared on the second write of the Program Resource Data Register indicating that two bytes have been accepted and that the serial device interface is busy writing the word to the EEPROM. Bits [5:2]: Reserved, set to zero Bit [6]: EEPROM Busy = 1 EEPROM interface is active = 0 EEPROM interface is idle Bit [7] : = 0 Enables a prefetch of serial EEPROM when the Serial Device Pointer Register is written or auto-incremented. = 1 Disables a prefetch of serial EEPROM when the Serial Device Pointer Register is written or auto-incremented.	C
Card Level Vendor Defined	0x27-0x2D	Reserved for future use, writes have no effect and reads return zero.	C
TEST 1 Default = 0x00, on POR or Reset_Drv hardware signal.	0x2F R/W	Test Modes: Not for customer use.	C
TEST 2 Default = 0x00, on POR or Reset_Drv hardware signal	0x2E R/W	Test Modes: Not for customer use	C

Table 50 - Configuration Control Register

	PNP-MODE	STD-MODE
	bit0 : Rst cmd bit1 : Wait for Key cmd bit2 : Rst CSN cmd	bit0 : Rst cmd bit1 : Wait for Key cmd bit2 : Rst CSN cmd
RESET_DRV or POR	While RESET_DRV (int-rst-drv) signal is asserted: * Reset all config control bits * Reset CSN to zero * Enter Wait for Key State * Reset all PNP registers to default * Send reset pulse to all logical devices On the falling edge of RESET_DRV (int-rst-drv) signal: * latch sysop pins * download BCW from EEPROM and program appropriate registers	* Latch sysop pins on trailing edge of int-rst-drv signal. * Reset all config control bits * Enter Run State * Reset all PNP registers to default * Send reset pulse to all logical devices On the falling edge of RESET_DRV (int-rst-drv) signal: * latch sysop pins
CONFIG CONTROL BITS	**PNP-MODE ACTION**	**STD_MODE ACTION**
0 0 0	Reset to 000 on RESET_DRV, POR and at end of every Configuration Control Register write. No action if written to 000.	Reset to 000 on RESET_DRV, POR and at end of every Configuration Control Register write. No action if written to 000.
0 0 1	* Send reset pulse to all logical devices * Reset only PNP Config registers that are not vendor specific * Reset Serial Device Pointer to zero * Download BCW from EEPROM and restore configuration registers of boot devices to power up values * Preserve CSN, RD_DATA Port and PNP State	* Send reset pulse to all logical devices. * Reset only PNP Configuration Registers that are not vendor specific. * Preserve State

Table 50 - Configuration Control Register

	PNP-MODE	STD-MODE
0 1 0	* Enter Wait for Key State * Preserve CSN & Read_Data Port * Preserve all register values	* Enter Run State * Preserve all register values
0 1 1	* Enter Wait for Key State plus all actions in 001 except for preservation of PNP State	* Same actions as in 001 except alway return to Run State
1 0 0	* Reset CSN to zero	N/A
1 0 1	* Reset CSN plus everything in 001 except preserve CSN	N/A
1 1 0	* Reset CSN * Enter Wait for Key State * no other action	N/A
1 1 1	* Reset CSN * Enter Wait for Key State * Perform all actions in 001	N/A

LOGICAL REGISTER DECODER [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. The FDC37C667 supports eight logical units through eight sets of Logical Device Registers. The eight logical devices are Floppy, IDE1, IDE2, Parallel, Serial 1 and Serial 2, Game Port, and Addrx (general purpose address decode output). A separate set of control and configuration registers exists for each logical device and is selected through the Logical Device # Register (0x07).

PNP-Mode

The Address Port (AP) Register is used to select a specific Logical Device Register. These registers are all read/write and once selected are written to through the Write_Data and read from through the Read_Data main registers.

STD-Mode

The Index Port is used to select a specific Logical Device Register. These registers are all read/write and once selected are written and read through the Data Port.

The Logical Device Registers are accessible only when the device is in the Configuration Mode.

Table 51 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Activate [1] Default = 0x00	(0x30)	Bits[7:1]: Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # Register. = 0 Logical device currently selected is inactive	C
I/O Range Check Default = 0x00	(0x31)	This register is used to perform an I/O port conflict check for the currently selected logical device. Bit[7:2] Reserved, set to zero. Bit[1] Set to enable I/O Range Check (valid only if logical device is inactive) Bit[0] = 1 Logical device drives 0x55 in response to I/O reads in assigned range. = 0 Logical device drives 0xAA in response to I/O reads in assigned range. Note: AEN must be deasserted (low) during I/O range check operations.	C
Logical Device Control	(0x32-0x37)	Reserved - not used, writes have no effect, reads return zero.	C
Logical Device Control	(0x38-0x3f)	Vendor Defined - not used, writes have no effect, reads return zero.	C
Mem Base Addr	(0x40-0x5F)	Not used, writes have no effect, reads return zero.	C
I/O Base Addr (see Device Base I/O Address Table - Table 1) Default = 0x00 0x60,62 = A[9:8] 0x61,63 = A[7:0]	(0x60-0x6F)	All logical devices contain 0x60, 0x61. IDE1 and IDE2, Logical Devices 0x01 and 0x02 respectively, contain 0x60 - 0x63 since the IDE registers are split and two base addresses are required. In the case of IDE [0x60,0x61] are used to set the I/O base of the TASK FILE registers and [0x62,0x63] are used to set the I/O base of the MISCELLANEOUS AT register[2]. Unused registers will ignore writes and return zero when read.	C

Table 51 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Interrupt Select Defaults : 0x70 = 0x00, 0x71 = 0x02	(0x70-073)	Only 0x70, 0x71 is implemented for each logical device. Refer to Interrupt Configuration Register description. Unused registers (0x72, 0x73) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).	C
DMA Channel Select Default = 0x04	(0x74, 0x75)	Only 0x74 is implemented for FDC, parallel port and IDE. If unimplemented 0x74 and 0x75 ignore writes and return 0x04 when read. Refer to DMA Channel Configuration.	C
32-Bit Memory Space Configuration	(0x76-0xAB)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
Logical device	(0xA9-0xEF)	Reserved - not implemented. These register locations ignore writes and return zero when read.	C
Logical Device Config.	(0xF0-0xFE)	Reserved - Vendor Defined (see SMC defined Logical Device Configuration Registers)	C
Reserved	0xFF	Reserved	C

Note 1: A logical device will be active and powered up according to the following equation:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET)

The Logical Device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other. If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 2: The IDE/FDC split register, normally found at either 0x3F7 or 0x377 is now an FDC support only register. The IDE Logical Device will now support only a status register (typically found at 0x3F6 or 0x376). The IDE Decoder operates as follows:

nHDCS0# = IDE TASK BASE + [7:0]
nHDCS1# = IDE MISC AT BASE + 0 (typically located at 0x3F6 or 0x376)

Table 52 - Interrupt Configuration Register Description

NAME	REG INDEX	DEFINITION	STATE
Interrupt request level select 0	0x70 (R/W)	Bits[3:0] selects which interrupt level is used for Interrupt 0. 0x00 = no interrupt selected. 0x01 = IRQ1 0x02 = IRQ2 o o o 0x0E = IRQ14 0x0F = IRQ15	C
Interrupt request type select 0	0x71 (R/W)	Bit[0]: Interrupt type, 1 = level, 0 = edge Bit[1]: level, 1 = high, 0 = low	C

Notes : An Interrupt is activated by:
Setting the Interrupt Request Level Select 0 register to a non-zero value :

And:

for the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
for the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
for the PP logical device in ECP mode by clearing serviceIntr, bit D2 of the ecr.
for the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.

And:

By activating the particular logical device.

Note: IRQ pins must tri-state if not used/selected by any logical device. Deactivated logical devices will not drive (i.e., will tri-state) the IRQ line allowing a common IRQ to be time-shared by two or more logical devices.

Table 53 - DMA Channel Configuration

NAME	REG INDEX	DEFINITION	STATE
DMA Channel select 0	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00 = DMA0 (not valid, reserved) 0x01 = DMA1 0x02 = DMA2 0x03 = DMA3 0x04 = No DMA active 0x05 = DMA5 0x06 = DMA6 0x07 = DMA7.	C

Note : A DMA channel is activated by:
Setting the DMA Channel Select 0 register to [0x01-0x03, 0x05-0x07] :

And:

for the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
for the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.

And:

by activating the partiular device.

Note: DMAREQ pins must tri-state if not used/selected by any Logical device. Deactivated logical devices will not drive (i.e.,will tri-state) the DRQ line or respond to $\overline{\text{DACK}}$ signals allowing a common DMA channel to be time shared by two or more logical devices.

Table 54 - Parallel Port DMA and IRQ Operation

MODE (FROM ECR REGISTER)		IRQ TRI-STATE CONTROLLED BY	PDREQ CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	Always DRIVEN	dmaEn
011	ECP	Always DRIVEN	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	Always DRIVEN	dmaEn
111	CONFIG	IRQE	dmaEn

IRQE = ackIntEn = bit 4 of the Parallel Port Control Register.
dmaEn = bit 3 of the ecr register.

SMC Specific Logical Device Configuration Registers

The SMC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by POR or the RESET_DRV signal. These registers are not affected by Soft Resets.

Table 55 - Floppy Disk Controller - Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	STATE
FDD Mode Register Default = 0x0E	0xF0 R/W	Bit[0] : Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] : FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-burst Mode (default) Bit[3:2] : Interface Mode (bit[3] = IDENT bit[2] = MFM) = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 Bit[4] : Swap Drives 0,1 Mode = 0 No swap (default) = 1 Drive and Motor sel 0 and 1 are swapped. Bits[7:5] : Reserved, set to zero.	C
FDD Option Register Default = 0x00	0xF1 R/W	Bits[1:0] : Reserved, not implemented Bits[3:2] : Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 = 11 0 Bits[5:4] : Media ID Polarity = 00 (default) = 01 = 10 = 11 Bits[7:6] : Boot Floppy = 00 FDD 0 (default) = 01 FDD 1 = 10 FDD 2 = 11 FDD 3	C

Table 55 - Floppy Disk Controller - Logical Device 0 [Logical Device Number = 0x00]

<table>
<tr><th>NAME</th><th>REG INDEX</th><th>DEFINITION</th><th>STATE</th></tr>
<tr><td>FDD Type Register

Default = 0xFF</td><td>0xF2 R/W</td><td>Byte format for 0xF4-0xF7:

<table>
<tr><td>BIT 7
0</td><td>BIT 6
PTS</td><td>BIT 5
0</td><td>BIT 4
DRT1</td><td>BIT 3
DRT0</td><td>BIT 2
0</td><td>BIT 1
DT1</td><td>BIT 0
DT0</td></tr>
</table>
Bits[1:0] : Floppy Drive A Type
Bits[3:2] : Floppy Drive B Type
Bits[5:4] : Floppy Drive C Type
Bits[7:6] : Floppy Drive D Type
= 11 (default)
= 01
= 10
= 00</td><td>C</td></tr>
<tr><td></td><td>0xF3 R</td><td>Reserved, Read as 0 (read only)</td><td>C</td></tr>
<tr><td>FDD0

Default = 0x00</td><td>0xF4 R/W</td><td>Bits[1:0] : Drive Type select "Table 13"
Bits[2] : Read as 0 (read only)
Bits[3:4] : Data Rate Table Select "Table 12"
Bits[5] : Read as 0 (read only)
Bits[6] : Precomp Disable
Bits[7] : Read as 0 (read only)</td><td>C</td></tr>
<tr><td>FDD1</td><td>0xF5 R/W</td><td>Refer to definition and default for 0xF4</td><td>C</td></tr>
<tr><td>FDD2</td><td>0xF6 R/W</td><td>Refer to definition and default for 0xF4</td><td>C</td></tr>
<tr><td>FDD3</td><td>0xF7 R/W</td><td>Refer to definition and default for 0xF4</td><td>C</td></tr>
</table>

Table 56 - IDE Drive 1 - Logical Device 1 [Logical Device Number = 0x01]

NAME	REG INDEX	DEFINITION	STATE
IDE Mode Register Default = 0x01	0xF0 R/W	Bit[0] : IDE AT/XT = 1 AT Type IDE (default) = 0 XT Type IDE Bits[7:1] : Reserved, set to zero	C

Table 57 - IDE Drive 2 - Logical Device 2 [Logical Device Number = 0x02]

NAME	REG INDEX	DEFINITION	STATE
IDE Mode Register Default = 0x01	0xF0 R/W	Bit[0] : IDE AT/XT = 1 AT Type IDE (default) = 0 XT Type IDE Bits[7:1] : Reserved, set to zero	C

Table 58 - Parallel Port - Logical Device 3 [Logical Device Number = 0x03]

NAME	REG INDEX	DEFINITION	STATE
PP Mode Register Default = 0x3C	0xF0 R/W	Bits[2:0] : Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] : ECP FIFO Threshold 0111b (default) Bit[7] : PP Interupt Type Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000) as shown above in bits [2:0]. = 1 Pulsed Low, released to high-Z = 0 IRQ follows $\overline{ACK}$ when parallel port is in EPP Mode or [Printer,SPP, EPP] under ECP. IRQ is level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode under ECP.	C

Table 59 - Serial Port 1 - Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION	STATE
SP1 Mode Register Default = 0x00	0xF0 R/W	Bit[0] : MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] : UART Speed = 0 Standard Speed UART (default) = 1 High Speed UART enabled Bit[2] : Reserved, set to zero Bit[3] : UART Auto Power = 0 Auto Powerdown disabled (default) = 1 Auto Powerdown enabled Bit[7:4] : Reserved, set to zero	C

Table 60 - Serial Port 2, Logical Device 5 [Logical Device Number = 0x05]

NAME	REG INDEX	DEFINITION	STATE
SP2 Mode Register Default = 0x00	0xF0 R/W	Bit[0] : MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] : UART Speed = 0 Standard Speed UART (default) = 1 High Speed UART enabled Bit[2] : Reserved, set to zero. Bit[3] : UART Auto Power = 0 Auto Powerdown disabled (default) = 1 Auto Powerdown enabled Bit[7:4] : Reserved, set to zero	C
SP2IR Register Default = 0x00 SP2 IR Register Default = 0x00	0xF1 R/W	Bit[0] : Receive Polarity = 0 RCV active High (default) = 1 RCV active Low Bit[1] : Transmit Polarity = 0 XMIT active High (default) = 1 XMIT active Low Bit[2] : Duplex Select = 0 Full Duplex (default) = 1 Half Duplex Note: When Serial Port 2 is placed into loopback mode by setting bit-4 (Loop) of Serial Port 2's Modem Control Register (MCR), Serial Port 2 will operate as a full duplex UART regardless of the value of this Duplex Select bit. When bit-4 of the MCR is cleared, the value of this bit defines the duplexity of Serial Port 2.	

Game Port - Logical Device 6 [Logical Device Number = 0x06]

No SMC defined registers for this device, all accesses to 0xF0 through 0xFF return zero.

Table 61 - ADDRx - Logical Device 7 [Logical Device Number = 0x07]

NAME	REG INDEX	DEFINITION	STATE
ADDRx Mode Register Default = 0x00	0xF0 R/W	Bit[0] : Decode Width = 0 Single byte on 1 byte boundaries (default) = 1 Eight bytes on 8 byte boundaries Bit[7:1] : Reserved, set to zero	C

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . V_{cc} +0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum V_{cc} . . . . . +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +5.0 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}	0.8			V	Schmitt Trigger
High Input Level	V_{IHIS}			2.2	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}	0.4			V	
High Input Level	V_{IHCK}			3.0	V	
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	μA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	μA	V_{IN} = V_{CC}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Current PWRGD	I_{OH}		75	150	μA	V_{IN} = 0
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
O24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
OD24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
OD24P Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -30 μA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
OD48 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 48 mA
Output Leakage	I_{OH}	-10		+10	μA	V_{OH} = 0 to V_{CC} (Note 2)
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
Supply Current Active	I_{CC}		35	50	mA	All outputs open.
Supply Current Standby	I_{CSBY}		300	500	μA	Note 3

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
ChiProtect (SLCT, PE, BUSY, $\overline{ACK}$, $\overline{ERROR}$)	I_{IL}			±10	μA	Chip in circuit: V_{CC} = 0V V_{IN} = 6V Max.
Backdrive ($\overline{STROBE}$, $\overline{AUTOFD}$, $\overline{INIT}$, $\overline{SLCTIN}$)	I_{IL}			±10	μA	V_{CC} = 0V V_{IN} = 6V Max.
Backdrive (PD0-PD7)	I_{IL}			±10	μA	V_{CC} = 0V V_{IN} = 6V Max.

Note 1: All output leakages are measured with the current pins in high impedance as defined by the PWRGD pin .

Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD.

Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

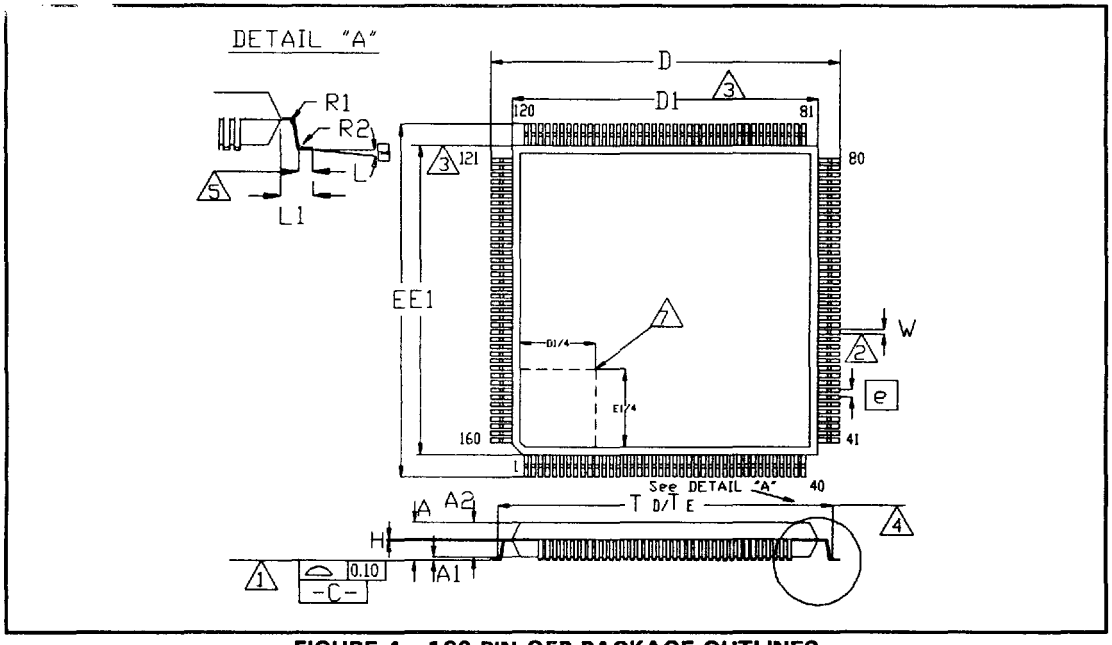


FIGURE 4 - 160 PIN QFP PACKAGE OUTLINES

	MIN	NOM	MAX
A			4.07
A1	0.05		0.5
A2	3.10		3.67
D	30.95	31.20	31.45
D1	27.90	28.00	28.10
E3	30.95	31.20	31.45
E1	27.90	28.00	28.10
H	0.10		0.200
L	0.65	0.80	0.95
L1		1.60	
e		0.65BSC	
O	0°		7°
W	0.20		0.40
R1		0.20	
R2		0.30	
T_D		30.45	
T_E		30.45	

Notes:

1. Coplanarity is 0.100 mm maximum
2. Tolerance on the position of the leads is 0.120 mm maximum
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm
4. Dimensions T_D and T_E are important for testing by robotic handler.
5. Dimensions for foot length L when measured at the centerline of the leads are given at the table. Dimension for foot length L when measured at the gauge plane 0.25 mm above the seating plane, is 0.78-1.03 mm
6. Controlling dimension: millimeter
7. Details of pin 1 identifier are optional but must be located within the zone indicated