

Panasonic
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2004 Ver. 2

Microcomputer
Selection Guide

SELECTION
GUIDE



AM1 Series
AM2 Series
AM3 Series
AM33 Series
ARM7 Series
MN1500 Series

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How to Read This Manual

■ Performing Searches

This manual offers three methods to find the information you need quickly.

- (1) To search for the start of a series, refer to the index at the beginning of the volume.
- (2) To look for a particular listed product, refer to the chart of listed products at the beginning of the volume.
- (3) The names of the listed products are located at the top right corner of every page. This makes it possible to leaf through the pages and stop at the place where the desired product name appears.

■ Format of this Manual

This manual is divided by lists, specifications for the various series, package lists, and the glossary. The page layout for the series specifications is composed of the product name, the specification support tools, and the pin configuration. Shown below is a sample of page layout and the meaning of each section.

Product name

Package

Minimum instruction execution time

Interrupts

I/O pins

Electrical characteristics

Pin assignment

Support tools

MN101C273

Type	MN101C273			
ROM (x8-bit)	4 K			
RAM (x8-bit)	0.5 K			
Package (Conventional Package)	SDIP28-P-0400 TM ***			
Minimum Instruction Execution Time	0.200 μs at 2.7 V to 5.2 V, 0.30 MHz 0.800 μs at 2.7 V to 5.2 V, 2 MHz			
Interrupts	* RSTET • Watchdog • External 0 • External 1 • Timer 2 • Timer 3 • Serial 0 • A/D conversion finish			
Timer Counter	Timer counter 2: 1/8 bit × 1 (square wave for PWM output, timer count, synchronous output event) Clock source: 1/4, 1/8 of system clock frequency; external clock input Interrupt source: coincidence with compare register 2 Timer counter 3: 8-bit × 1 (square wave output, timer count, generation of remote control carrier, serial 0 baud rate timer) Clock source: 1/4, 1/8 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source: coincidence with compare register 3 Timer counter 2, 3 can be cascade-connected. Watchdog timer Interrupt source: 1/328256 of system clock frequency			
Serial Interface	Serial 0: non-retransmission-type UART (full-duplex) × 1 Clock source: 1/2, 1/4, 1/8 of system clock frequency; 1/2 of timer counter 3 frequency			
I/O Pins	I/O 16 Input 8 * Common use • Specified pull-up resistor available • Input/output selectable (bit set)			
A/D Inputs	10-bit × 4-ch. (width 8-bit)			
Special Ports	Remote control carrier signal output, high-current drive port			
Electrical Characteristics	Supply current			
Parameter	Symbol	Condition	Limit	Unit
Operating supply current	ID01	I _{osc} = 0.30 MHz, V _{DD} = 5 V	25	mA
Supply current at HALT	ID02	I _{osc} = 0.30 MHz, V _{DD} = 5 V	3	mA
Supply current at ST	ID01	V _{DD} = 5 V, T _a = 25°C	2	μA
		V _{DD} = 5 V, T _a = -40°C to +85°C	0	μA

MN101C273 □

() Conventional Package

Pin Assignment

SDIP28-P-0400 TM ***
(SDIP28-P-0400)

Support Tool

In-circuit Emulator	FX-ICE100(C)-FX-PEB100(C)-SDIP28-P-0400
EPR0M Built-in Type	Type: MN101C273 ROM (x 8-bit): 4 K RAM (x 8-bit): 0.5 K Minimum instruction execution time: 0.200 μs (at 2.7 V to 5.2 V, 0.30 MHz) Package: SDIP28-P-0400 TM *** (QJ4 Package) (SDIP28-P-0400)

■ Description

● Type

Development status may be either “in production” (no indication), “ES (Engineering Sample) available”, “Under Development”, or “Under Planning”.

Please indicate the values in square brackets (“[]”) when you order ROM.

● Package

The lead-free package is referred to as “*Lead-free.” For details on the conventional package, see the contents enclosed in parentheses ().

For information on the supported packages, be sure to contact our business reception.

● Minimum instruction execution time

If it is possible to select the microcontroller operation clock (OSC or X), execution times are given separately for the main clock and the sub-clock.

When two types of minimum instruction execution time are given with no special description, the values are given as variations in the operating voltage range or oscillation frequency.

● Interrupts

Interrupts are listed by source.

When jointly used, values are separated by a slash (“/”).

The number of sources indicated in the list is the total number except RESET.

● I/O pins

The number stated is the number of ports available for general use.

The detailed description provides an explanation of each pin. “P” is an abbreviation for “port”.

● Electrical characteristics

The values listed under electrical characteristics are all reference values.

● Piggyback

Development status is either “available” (no indication) or “Under Development”.

● EPROM built-in type, Flash memory built-in type

Development status may be either “in production” (no indication), “ES (Engineering Sample) available”, “Under Development”, or “Under Planning”.

Specifications may vary slightly from the chip described. Please consult our sales staffs.

■ Note!

For information regarding chip development status, package, piggyback an EPROM built-in type, and availability of flash memory built-in type, please consult our sales staffs (contact points are listed at the end of this manual).

■ Note on Naming

If the additional digits for customer ROM version, etc. should produce a device name exceeding 12 characters, we reduce it to 12 characters with the following schema.

The final device name appears, however, on delivery specifications and similar documents.

Description	Full device name (13 or more characters)	Abbreviated name (12 characters)
4-bit microcomputer	MN <u>15</u> - - - - - →	MN <u>Y</u> - - - - -
8-bit microcomputer	MN <u>101</u> - - - - - →	MN <u>B</u> - - - - -
16-bit microcomputer	MN <u>102</u> - - - - - →	MN <u>P</u> - - - - -
32-bit microcomputer	MN <u>103</u> - - - - - →	MN <u>Z</u> - - - - -

If a device name still exceeds 12 digits regardless of the use of the abbreviated name, the name shall be determined according to a separate standard.

PRODUCTS

Products

■ 8-bit Single-chip Microcomputer AM1 (MN101) Series

Category	Type	ROM (× 8-bit)	RAM (× 8-bit)	Package	Built-in EPROM	Built-in Flash	I/O (Pins)	Speed (μs)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D (Pins)	D/A (Pins)	FL	LCD	Page									
ADC Built-in Type	MN101C273	4 K	0.5 K	SDIP028-P-0400D	○	-	22	0.238	2.7 to 5.5	7	8-bit × 2	Synchronous Type /Half-Duplex UART × 1	4	-	-	-	12									
	MN101C425	8 K	0.25 K	SDIP042-P-0600C QFP044-P-1010F TQFP048-P-0707B			39 ^{*5}	0.1 125 ^{*6}	4.5 to 5.5 2.0 to 5.5	12 ^{*4}	8-bit × 3 16-bit × 1		14													
	MN101C427	16 K	0.5 K	QFP044-P-1010F			37	0.1	4.5 to 5.5	11		14					Synchronous Type /UART × 1	18	Synchronous Type × 1 Synchronous Type /Half-Duplex UART × 1 Synchronous Type /Single-Master I ² C × 1	8	-	-	-	16		
	MN101C457						40	0.1 62.5	4.5 to 5.5	17	17		20													
	MN101C539	24 K	1 K	LQFP048-P-0707B			70	0.1 125	4.5 to 5.5 2.0 to 5.5	18	8-bit × 5 16-bit × 1	25	8-bit × 7 16-bit × 1				Synchronous Type × 1, Synchron- ous Type/UART × 2 Synchronous Type /Single-Master I ² C × 1	6	4	-	-	-	18			
	MN101C309																						54	17	20	
	MN101C30A	32 K	1.5 K	LQFP064-P-1414			68	0.1 0.25 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	25	8-bit × 6 16-bit × 2	26	8-bit × 6 16-bit × 1				Synchronous Type × 1, Synchron- ous Type/UART × 2 Synchronous Type /Single-Master I ² C × 1 Synchronous Type /UART × 2	8	-	-	-	24				
	MN101C28A																					69	17	20		
	MN101C28C	48 K	2 K	LQFP080-P-1414A TQFP080-P-1212D QFP084-P-1818E			-	0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	26	8-bit × 6 16-bit × 1	23	8-bit × 6 16-bit × 1				Sync. Type × 1, Sync. Type/ UART × 2, Sync. Type /Single-Master I ² C × 1, I ² C slave × 1	7	-	-	-	28				
	MN101C28D	64 K																				68	25	32		
	MN101C28F	96 K	4 K	LQFP080-P-1414A			-	0.1 0.25 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	23	8-bit × 6 16-bit × 1	29	8-bit × 6 16-bit × 1				Synchronous Types/UART × 2 Single-Master I ² C × 1	6	-	-	-	32				
	MN101C28L																					10 K	36			
	MN101C51F	6 K	3 K	TQFP080-P-1212D			-	0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	23	8-bit × 6 16-bit × 1	29	8-bit × 6 16-bit × 1				Synchronous Types/UART × 3, Synchronous Type/Single- Master I ² C × 1, Synchronous Type/I ² C × 1	8	-	-	-	36				
	MN101C61D	64 K																				36				
	MN101C61G	128 K	12 K	LQFP080-P-1414A			-	0.1 0.25 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	23	8-bit × 6 16-bit × 1	29	8-bit × 6 16-bit × 1				Synchronous Types/UART × 3, Synchronous Type/Single- Master I ² C × 1, Synchronous Type/I ² C × 1	8	-	-	-	40				
	MN101C62D	64 K	2 K																			44				
	MN101C62F	96 K	4 K	TQFP080-P-1212D			-	0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	23	8-bit × 6 16-bit × 1	29	8-bit × 6 16-bit × 1				Synchronous Types/UART × 3, Synchronous Type/Single- Master I ² C × 1, Synchronous Type/I ² C × 1	8	-	-	-	44				
	MN101C67D	64 K	6 K																			44				
	MN101C67G	128 K	10 K	QFP048-P-0707B			-	0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	23	8-bit × 6 16-bit × 1	29	8-bit × 6 16-bit × 1				Synchronous Types/UART × 3, Synchronous Type/Single- Master I ² C × 1, Synchronous Type/I ² C × 1	8	-	-	-	44				
	MN101CF91D ^{*3}	64 K	2 K																			44				
MN101E16K ^{*3}	256 K	12 K	QFP100-P-1818B ^{*1} LQFP100-P-1414 ^{*3}	-	0.0588 30.6	2.7 to 3.6 2.7 to 3.6	29	8-bit × 9 16-bit × 1	29	8-bit × 9 16-bit × 1	Synchronous Types/UART × 3, Synchronous Type/Single- Master I ² C × 1, Synchronous Type/I ² C × 1	8	-	-	-	44										
MN101E16L ^{*3}	320 K	14 K														44										
MN101E16M ^{*1}	384 K	20 K	QFP084-P-1818E	-	0.1 125	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	22	8-bit × 5 16-bit × 1	22	8-bit × 5 16-bit × 1	Synchronous Type/ UART × 2 Single-Master I ² C × 1/ Synchronous × 1 I ² C slave × 1	7	2 ^{*7}	-	-	56										
MN101C08C	48 K	1.5 K														56										
DAC Built-in Type	MN101C49G	128 K	4 K	QFP100-P-1818B LQFP100-P-1414	-	-	88	0.1 62.5	4.5 to 5.5 2.0 to 5.5	23	8-bit × 6 16-bit × 1	Synchronous Type × 1 Synchronous Type /UART × 2 Synchronous Type /Single-Master I ² C × 1	8	4	-	-	-	52								
	MN101C49H	160 K	6 K				88	0.1 62.5	4.5 to 5.5 2.0 to 5.5	23	8-bit × 6 16-bit × 1	56														
	MN101C49K	224 K	10 K	88			0.1 62.5	4.5 to 5.5 2.0 to 5.5	23	8-bit × 6 16-bit × 1	56															
	MN101C77A ^{*1}	32 K	1.5 K	LQFP064-P-1414 TQFP064-P-1010C ^{*1}			53	0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	22	8-bit × 5 16-bit × 1	56														
	MN101C77C	48 K	3 K	53			0.1 0.2 62.5	2.5 to 3.6 2.1 to 3.6 1.8 to 3.6	22	8-bit × 5 16-bit × 1	56															
	MN101E01J	192 K	10 K	QFP100-P-1818B LQFP100-P-1414			-	-	84	0.0625 62.5	3.0 to 3.6	26	8-bit × 7 16-bit × 1	Synchronous Type/UART × 3 Synchronous Type /Single-Master I ² C × 2				8	1	-	-	-	60			
	MN101E01K	256 K	10 K						84	0.0625 62.5	3.0 to 3.6	26	8-bit × 7 16-bit × 1	60												
	MN101E01L	320 K	14 K						84	0.0625 62.5	3.0 to 3.6	26	8-bit × 7 16-bit × 1	60												
MN101E01M	384 K	20 K	84	0.0625 62.5	3.0 to 3.6	26			8-bit × 7 16-bit × 1	60																
LCD Built-in Type	MN101C78A ^{*1}	32 K	1.5 K	QFP044-P-1010F ^{*3}	-	-			35	0.1 0.5 62.5	2.7 to 3.6 1.8 to 3.6 1.8 to 3.6	21	8-bit × 5 16-bit × 2	Synchronous Type/UART × 2 Synchronous Type/ Single-Master I ² C × 1 I ² C slave × 1	4	-	-	-	SEG12 COM4				64			
				TQFP048-P-0707B					40	0.1 0.5 62.5	2.7 to 3.6 1.8 to 3.6 1.8 to 3.6												7	64		
	MN101C485	8 K	0.5 K	LQFP064-P-1414 TQFP064-P-1010B					-	-	47	0.1 125	4.5 to 5.5 2.0 to 5.5	12	8-bit × 3 16-bit × 1	Synchronous Type /Half-Duplex UART × 1	8	-	-				-	-	SEG25 COM4	68
	MN101C487	16 K									LQFP064-P-1414 TQFP064-P-1010B	47	0.1 125													4.5 to 5.5 2.0 to 5.5
	MN101C527		24 K	1.5 K			LQFP064-P-1414	-				-	49	0.1 0.25 62.5	4.5 to 5.5 2.7 to 5.5 2.0 to 5.5	17	8-bit × 5 16-bit × 2	Synchronous Type /UART × 1	4	-	-	-	SEG24 COM4	70		
	MN101C589	49									0.1 0.25 62.5		4.5 to 5.5 2.7 to 5.5 2.0 to 5.5	17	8-bit × 5 16-bit × 2									70		
	MN101C58A	32 K	2 K	TQFP080-P-1212D			-				-		61	0.1 125	4.5 to 5.5 2.0 to 5.5	14	8-bit × 3 16-bit × 1	Synchronous Type × 1 Synchronous Type /Half-Duplex UART × 1	8	-	-	-	SEG28 COM4	74		
	MN101C39C	48 K											2 K	TQFP080-P-1212D	61									0.1 125	4.5 to 5.5 2.0 to 5.5	14

*1 under development *2 ES (Engineering Sample) available *3 under planning *4 11 for other than TQFP048
*5 x37 for QFP044, x36 for SDIP042 *6 No low-speed mode for types other than TQFP048 *7 Serves as AD pin, as well
I/O: at single chip mode
Page: Please ask our sales offices about the product of '-'.
-

8-bit Single-chip Microcomputer AM1 (MN101) Series (Continue)

Category	Type	ROM (× 8-bit)	RAM (× 8-bit)	Package	Built-in EPROM	Built-in Flash	I/O (Pins)	Speed (μs)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D (Pins)	D/A (Pins)	FL	LCD	Page			
LCD Driver Built-in Type (Continue)	MN101C54A	32 K	2 K	QFP084-P-1818E LQFP080-P-1414A	○	○	65	0.1 0.25 62.5	4.5 to 5.5 2.7 to 5.5 2.0 to 5.5	19	8-bit × 5 16-bit × 2	Synchronous Type × 1 Synchronous Type /UART × 1	8				80			
	MN101C54C	48 K															84			
	MN101C66D	64 K																		
	MN101C66G	128 K	4 K	LQFP080-P-1414A TQFP080-P-1212D *3	-	○*1	66	0.1 0.235 62.5	3.0 to 3.6 1.8 to 3.6 1.8 to 3.6	20	8-bit × 6 16-bit × 2	Synchronous Type /Single-Master I ² C × 1 Synchronous Type /UART × 1	16			88				
	MN101C70C	48 K	2 K																	
	MN101C70G*3	128 K	10 K	QFP100-P-1818B LQFP100-P-1414	○	-	57	0.1 0.25 125	4.5 to 5.5 2.7 to 5.5 2.0 to 5.5	14	8-bit × 3 16-bit × 1	Synchronous Type × 1 Synchronous Type /Half-Duplex UART × 1	8	-	-		92			
	MN101C38A	32 K	1.5 K																	
	MN101C38C	48 K	2 K	QFP100-P-1818B LQFP100-P-1414 *3	○	-	83	0.1 62.5	4.5 to 5.5 2.0 to 5.5	24		Synchronous Type × 1 Synchronous Type /UART × 1	16				94			
	MN101C57C																64 K			
	MN101C73A *1	32 K	1.5 K	LQFP064-P-1414	-	○	55	0.1 0.235 62.5	3.0 to 3.6 1.8 to 3.6 1.8 to 3.6	24	8-bit × 5 16-bit × 2	Synchronous Type/ UART × 2 Synchronous Type /Single-Master I ² C × 1	12				98			
	MN101C73D *3	64 K	2 K																	
	MN101C74D *1	64 K	2 K	LQFP100-P-1414 *3 QFP100-P-1818B	-	○*1	86	0.1 62.5	3.0 to 3.6 1.8 to 3.6 1.8 to 3.6	26		Synchronous Type/ UART × 2 Synchronous Type /Single-Master I ² C × 1 /I ² C slave × 1	16				102			
	MN101C74F *3	96 K	4 K																	
	MN101C74G *1	128 K	6 K	LQFP064-P-1414	-	○	52	0.1 0.25 62.5	4.5 to 5.5 2.7 to 5.5 2.0 to 5.5	18		Synchronous/UART × 1	8				106			
MN101C84A *1	32 K	1 K																		
MN101C84D *3	64 K	2 K																		
FL Driver Built-in Type	MN101C07A	32 K	1 K	LQFP064-P-1414	○	-	53	0.25 125	2.7 to 5.5	16	8-bit × 3 16-bit × 1	Synchronous Type × 1 Synchronous Type /Half-Duplex UART × 1	5			SEG16 DGT10	110			
	MN101C35D	64 K	2 K	QFP100-P-1818B			89		2.7 to 5.5 2.2 to 5.5	19	8-bit × 5 16-bit × 1	Synchronous Type × 1, Synchron- ous Type/ Simple I ² C × 1, Synchron- ous Type/ Half-Duplex UART × 1	8			SEG43 DGT10	112			
	MN101C87A *1	32 K	1.25 K	LQFP064-P-1414	-	○*1	52	0.25 62.5 0.1	2.7 to 5.5 2.0 to 5.5 4.5 to 5.5	20	8-bit × 5 16-bit × 1	Synchronous/UART × 1 Synchronous/ Single-Master I ² C × 1	8				116			
	MN101C87D *3	64 K	2 K																	
	MN101C88D *3	64 K	2 K	QFP100-P-1818B	-	○*1	88	0.1	4.5 to 5.5	22	Synchronous/UART × 2 Synchronous/ Single-Master I ² C × 1	8					120			
	MN101C88F *3	96 K	4 K																	
MN101C88G *1	128 K	4 K																		
USB Built-in Type	MN101C75D *3	64 K	2 K	LQFP080-P-1414A	-	○*3	62	0.125 62.5	3.0 to 3.6 3.0 to 3.6	21	8-bit × 6 16-bit × 2	Synchronous Type/ UART × 1	12	-	-		124			
	MN101C93D *3			LQFP100-P-1414			82		8-bit × 5 16-bit × 2	Synchronous Type /Single-Master I ² C × 1	8		SEG32 COM4 SEG47 COM4				-			
Multiplication/ Division functions improved	MN101C29D	64 K	1.5 K	LQFP080-P-1414A	-	○	55	0.1	4.5 to 5.5	14	8-bit × 2 16-bit × 1	Synchronous Type × 1	-	-	-	-	128			
TV Channel Selector	MN101C46F	96 K	3 K	SDIP042-P-0600C	-	○*2	35	0.279	3.0 to 3.6	18	8-bit × 3	I ² C Multimaster × 2	8	-	-	-	130			
	MN101C47C	48 K	1.5 K	SDIP042-P-0600C						14							132			
	MN101C47D	64 K	2 K	LQFP064-P-1414																
3-line comb filter for TV selector Built-in VCJ	MN101E02H	160 K	16 K	QFP084-P-1818E	-	○*2	30	0.1	3.135 to 3.465	22	8-bit × 4	Synchronous Type/ UART × 1 I ² C Multimaster × 2	8	-	-	-	134			
	MN101E11G	128 K	4 K				35										136			
	MN101E13G						30										138			
	MN101E04G						30										140			
VTR Servo	MN101D06F	96 K	3 K	QFP100-P-1818B	-	○	77	0.14 61	4.0 to 5.5 2.2 to 5.5	31	8-bit × 1 16-bit × 6 19-bit × 1	8-bit × 3 One I ² C dedicated One UART Selectable	13	-	1	-	142			
	MN101D06G	128 K	4 K				LQFP112-P-2020										87	146		
	MN101D06H	160 K	5 K														57	150		
	MN101D07G	128 K	4 K	LQFP080-P-1414A			-		-	-	-	-	-	-	-	-	-	-	154	
	MN101D07H	160 K	5 K																77	158
	MN101D08E	80 K	2 K	QFP100-P-1818B			-		-	-	-	-	-	-	-	-	-	-	-	154
	MN101D09E																			57
	MN101D10F	96 K	2.5 K	QFP100-P-1818B			-		-	-	-	-	-	-	-	-	-	-	-	158
MN101D10G	128 K	3.5 K	77		158															
Hardware task Multiplication/ Division functions improved	MN101D03D	64 K	2 K	LQFP080-P-1414A	○	○	68	0.1 122	4.0 to 5.5 2.0 to 5.5	26	8-bit × 6 16-bit × 2	8-bit × 3 One I ² C dedicated One UART Selectable	8	-	-	-	162			

*1 under development *2 ES (Engineering Sample) available *3 under planning I/O: at single chip mode
Page: Please ask our sales offices about the product of '-'.
Products

■ 16-bit Single-chip Microcomputer AM2 (MN102) Series

Category	Type	ROM (× 8-bit)	RAM (× 8-bit)	Package	Built-in EPROM	Built-in Flash	I/O (Pins)	Speed (μs)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D (Pins)	D/A (Pins)	FL	LCD	Page
ADC Built-in Type	MN102L59D	64 K	2 K	LQFP064-P-1414	—	○ ^{*2}	52	0.1	4.5 to 5.5	24	8-bit × 9 16-bit × 3	1 to 8-bit × 2 Simple UART Selectable	12				168
	MN102L62G	128 K	5 K	LQFP100-P-1414	○	○	80	0.1 62.5		26	8-bit × 6 16-bit × 2	7, 8-bit × 2 UART Selectable	8	—	—	—	170
	MN102L490A	External	3 K		LQFP100-P-1414	—	—	48	0.0885 62.5								50
	MN102L610B		4 K	LQFP100-P-1414 MLGA100-L-1010						—	○	82	0.058 62.5	3.0 to 3.6	54	8-bit × 16 16-bit × 5 24-bit × 1	
	MN102H60G	128 K	4 K		LQFP128-P-1818C FLGA165-C-1111	—	○	108	0.05 0.1								3.0 to 3.6 2.0 to 3.6
	MN102H60K	256 K		10 K						LQFP100-P-1414	—	○	108	0.05 0.1	3.0 to 3.6 2.0 to 3.6	54	
	MN1021617	128 K	4 K	LQFP128-P-1818C FLGA165-C-1111	—	○	108	0.05 0.1	3.0 to 3.6 2.0 to 3.6	54							8-bit × 16 16-bit × 5 24-bit × 1
	MN102H460B	External									LQFP128-P-1818C TQFP128-P-1414B	—	—	63	0.05 0.1	3.0 to 3.6 2.0 to 3.6	
ADC·DAC Built-in Type	MN102L360C	External	5 K	LQFP128-P-1818C	○	—	83	0.1 62.5	4.5 to 5.5	30	8-bit × 6 16-bit × 2						7, 8-bit × 2 UART Selectable 8-bit × 2
	MN102H55G	128 K	4 K	LQFP100-P-1414	—	○	82	0.058 62.5	3.0 to 3.6	50	8-bit × 10 16-bit × 6	7, 8-bit × 2 UART Selectable 7, 8-bit × 3	12	4	—	—	194
	MN102H730F	External	10 K	TQFP128-P-1414B													—
	MN102H73G	128 K		TQFP128-P-1414A	—	○	104	0.058 62.5	3.0 to 3.6	47	7-, 8-bit × 5	12	4	—	—	202	
	MN102H73K	256 K	12 K	LQFP100-P-1414A MLGA100-L-1010A ^{*1}	—	—	63									0.058 62.5	3.0 to 3.6
	MN102H930F	external	10 K					LQFP100-P-1414A MLGA100-L-1010A ^{*1}	—	—	63	0.058 62.5	3.0 to 3.6	47	7-, 8-bit × 5		
	MN102H950F			LQFP100-P-1414	—	—	63	0.058 62.5								3.0 to 3.6	47
USB	MN102H74D	64 K	4 K	LQFP100-P-1414					—	○	77	0.0833 62.5	3.0 to 3.6	54	8-bit × 10 16-bit × 4		
	MN102H74F	96 K			210												
	MN102H74G	128 K			210												
TV Channel Selector	MN102L35G	144 K	5 K	SDIP064-P-0750C	○	—	50	0.167	4.75 to 5.25	27	8-bit × 2 16-bit × 2	I ² C, UART	8				214
	MN102H75K	256 K	8 K	QFP084-P-1818E	—	○	66	0.083	3.0 to 3.6	36	8-bit × 4 16-bit × 2	7, 8-bit × 2 UART Selectable I ² C Multimaster × 2	12	4	—	—	216
	MN102H85K			SDIP064-P-0750C			50										218
	MN102H90M	384 K or external	20 K	QFP160-P-2828F	—	—	111	0.083	3.135 to 3.465	35	8-bit × 10	7-, 8-bit × 3 UART Selectable I ² C Multimaster × 3	8	—	—	—	220
3-line comb filter for TV selection Built-in VCJ	MN102H76G	128 K	4 K	QFP084-P-1818E	—	—	35										3.135 to 3.465
	MN102H81G						30	33	224								

^{*1} under development
^{*2} ES (Engineering Sample) available
^{*3} under planning

■ 32-bit Single-chip Microcomputer AM3 (MN103/MN103S) Series

Type	CPU Performance ^{*2}	On-Chip Memory	Package	Built-in Flash	Expanded Calculation Functions	I/O (Pins)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D Converter	DMA Controller	Bus Interface	Page
MN103000	60 MIPS (60 MHz)	Instruction RAM : 16 KB Data RAM : 16 KB	QFP160-P-2828F	—	Multiply Saturation	89	3.3 (Tolerance = ±5%)	48	32-bit × 2 16-bit × 5 WDT × 1	UART/CSI /I ² C × 2	10-bit × 8-ch	4-ch	Data : 8-/16-/32-bit Selectable DRAM Interface	228
MN103001G		Instruction ROM : 128 KB Data RAM : 8 KB	LQFP100-P-1414	○		72	3.0 to 3.6	38	32-bit × 3 16-bit × 4 WDT × 1	UART/CSI/I ² C × 1 UART × 1 CSI × 2	10-bit × 4-ch	—	—	Data : 8-/16-bit Selectable DRAM Interface
MN103002A	66 MIPS (66 MHz)	Instruction Cache : 4 KB Data Cache : 4 KB	QFP160-P-2828F	—	Multiply-and-Accumulate Multiply Saturation	26	3.3 (Tolerance = ±5%)	30	32-bit × 1 16-bit × 3 WDT × 1	UART/CSI/I ² C × 2 UART × 1	—	4-ch	Data : 16-/32-bit Selectable DRAM Interface	236
MN103004K	40 MIPS (40 MHz)	Instruction ROM : 256 KB Data RAM : 10 KB	FLGA239-C-1313 QFP208-P-2828F	○		171	2.7 to 3.6	72	32-bit × 3 16-bit × 6 WDT × 1	UART/CSI/I ² C × 2 UART × 1 CSI × 5	10-bit × 16-ch	2-ch	Data : 8-/16-bit Selectable DRAM Interface	240
MN103016K		FLGA239-C-1313	—		—	—	—	—	—	—	—	—	—	—
MN103S33N	41 MIPS (41 MHz)	Instruction ROM : 512 KB Data RAM : 24 KB	MBGA360-C-1313A	○ ^{*1}	Multiply-and-Accumulate Multiply Saturation	194	2.3 to 2.7	125	16-bit × 12 8-bit × 20 WDT × 1	UART/CSI/I ² C × 10 UART × 2	10-bit × 25-ch	4-ch	Data : 8-/16-/32-bit Selectable SDRAM Interface	244
MN103S57G	40 MIPS (40 MHz)	Instruction ROM : 128 KB Data RAM : 16 KB	LQFP100-P-1414A	○		73	3.0 to 3.6	55	16-bit × 6 8-bit × 10 WDT × 1	UART/CSI/I ² C × 2 CSI × 3	10-bit × 12-ch	4-ch	Data : 8-/16-bit Selectable	248
MN103S52G		Instruction ROM : 128 KB Data RAM : 4 KB	QFP100-P-1818		○	72	4.3 to 5.5	42	16-bit 3-phase PWM × 1 16-bit × 4 8-bit × 8 WDT × 1	UART/CSI × 3	10-bit × 2-ch × 2 10-bit × 12-ch × 1	—	—	—
MN103S65G	LQFP080-P-1414	—	60	10-bit × 2-ch × 2 10-bit × 6-ch × 1		252								
MN103S83D	Instruction ROM : 64 KB Data RAM : 2 KB	QFP084-P-1818E LQFP080-P-1414 ^{*1}	—	—	40	—	—	—	—	—	—	—	—	254
MN103S77N ^{*1}	48 MIPS (60 MHz)	Instruction ROM : 512 KB Data RAM : 32 KB	LQFP128-P-1818	○ ^{*1}	Multiply-and-Accumulate Multiply Saturation	104	3.0 to 3.6	65	16-bit × 6 8-bit × 10 WDT × 1	I ² C × 1, UART/CSI × 3, UART/CSI/Multi-Master I ² C × 2	10-bit × 12-ch	4-ch	8-, and 16-bit Access SDRAM Interface Supporting	256
MN103S927 ^{*1}	40 MIPS (40 MHz)	Instruction ROM : 16 KB Data RAM : 2 KB	LQFP064-P-1414			49		25	16-bit 3-phase PWM × 1 16-bit × 2 8-bit × 4 WDT × 1	UART/CSI × 1	10-bit × 2-ch × 1, 10-bit × 6-ch × 1	—	—	—
MN103S92A ^{*1}		Instruction ROM : 32 KB Data RAM : 2 KB		—	—	—	—	—	—	—	—	—	—	—
MN103S97N ^{*1}	41 MIPS (41 MHz)	Instruction ROM : 512 KB Data RAM : 24 KB	MBGA255-C-1111A	—	—	195	2.7 to 3.6	106	16-bit × 12 8-bit × 16 WDT × 1	UART/CSI × 7 I ² C × 2	10-bit × 25-ch	4-ch	8-, 16-, and 32-bit Access	260

^{*1} under development
^{*2} Dhrystone 2.1

■ 32-bit Microprocessor AM33 (MN103E) Series

Type	CPU Performance ^{*2}	On-Chip Memory	Package	Built-in Flash	Expanded Calculation Functions	I/O (Pins)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D Converter	DMA Controller	Bus Interface	Page
MN103E010HRA	133 MIPS (133 MHz)	Instruction cache : 16 KB Data cache : 16 KB	BGA292-P-2727	—	Multiply-and-Accumulate Multiply Saturation Floating Point (Single Precision)	34	1.8 (Tolerance = ±5%)	41	16-bit × 8 8-bit × 4 WDT × 1	UART/CSI × 2 UART × 1 AFE × 1 I ² C × 2 IrDA × 1	10-bit × 8-ch	4-ch	Memory Interface Supporting 16-, and 32-bit Access SDRAM Interface Supporting 16-bit	266
MN103E040HYB			FLGA424-C-1717											270
MN103E0600YD ^{*1}			MLGA239-C-1111											—

^{*2} Dhrystone 2.1

■ 32-bit Single-chip Microcomputer ARM7 (MN1A7) Series

Type	ROM	RAM	Package	I/O (Pins)	Speed (μs)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D	D/A	Bus Interface	Page
MN1A7T0200	External	External	FLGA152-C-1111	40	0.1 62.5	2.3 to 2.7	43	16-bit × 10	UART × 3 SSI × 2	10-bit × 8-ch	—	Data: 8-/16-/32-bit Selectable	276

■ 4-bit Single-chip Microcomputer MN1500 Series

Type	ROM (× 8-bit)	RAM (× 4-bit)	Package	Built-in EPROM	Built-in Flash	I/O (Pins)	Speed (μs)	Operating Voltage (V)	Interrupt Sources	Timer Counter	Serial Interfaces	A/D (Pins)	FL	LCD	Page				
MN15G1601	16 K	512	LQFP064-P-1414	○	—	35	0.5 1.0 2.0	3.0 to 5.5 2.4 to 5.5 2.0 to 5.5	3	8-bit × 4	Synchronous Type × 1-ch	8	—	—	280				
MN15G0202	2 K	128	SOP020-P-0300D	○ ^{*2}		15									8-bit × 2	4	—	—	282
MN15G0402	4 K			—		—									—	—	—	—	—
MN15G0804	8 K	512	QFP044-P-1010E	○		34									0.96 1.91	2.4 to 5.5 2.0 to 5.5	—	8-bit × 3	—

^{*2} ES (Engineering Sample) available

AM1 8-bit ASERIES

AM1 (MN101) Series

The AM1 Series of 8-bit microcomputers is the realization of developments in C programming.

Because of the 8-bit architecture, which allows half-byte instruction sets and offers other advantages, assembler ROM code size can be reduced.

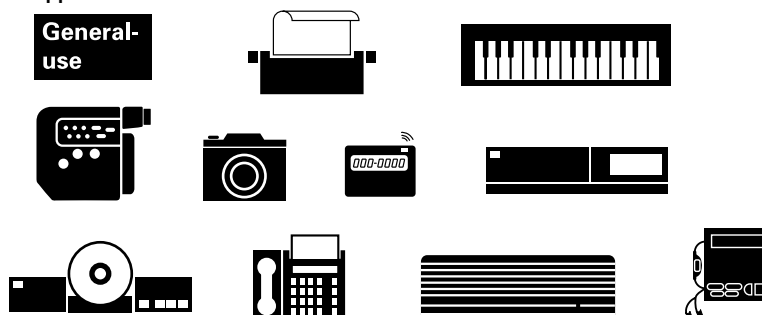
They are compact and consume little power, but feature a shortest instruction processing time of 63 ns (5 V).

They can be used in a wide variety of applications where cost performance is a demand.

Features

- **Efficiency of C-based ROM code:** Assembler rate 1 or less
- **High-speed instruction processing:** 63 ns (32 MHz)
- **Linear address space:** 1 MB
- **Identical architecture for 32- and 16-bit microcomputers**
- **Option functions**
 - Hardware task switching (Max. 4 task)
 - 16-bit multiplication
 - ROM collection

Application



□ MN101C273

Type	MN101C273
ROM (x8-bit)	4 K
RAM (x8-bit)	0.5 K
Package (Conventional Package)	SDIP028-P-0400D *Lead-free (SDIP028-P-0400)
Minimum Instruction Execution Time	0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 1.00 μs (at 2.0 V to 5.5 V, 2 MHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.

Interrupts • RESET • Watchdog • External 0 • External 1 • Timer 2 • Timer 3 • Serial 0 • A/D conversion finish

Timer Counter

Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event)
 Clock source 1/1, 1/4 of system clock frequency; external clock input
 Interrupt source coincidence with compare register 2

Timer counter 3 : 8-bit × 1
 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer)
 Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency;
 external clock input
 Interrupt source coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.

Watchdog timer
 Interrupt source 1/1048576 of system clock frequency

Serial Interface Serial 0 : synchronous type/simple UART (half-duplex) × 1
 Clock source 1/2, 1/4, 1/16 of system clock frequency; output of timer counter 3

I/O Pins	I/O	16	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	6	• Common use • Specified pull-up resistor available

A/D Inputs 10-bit × 4-ch. (with S/H)

Special Ports Remote control carrier signal output, high-current drive port

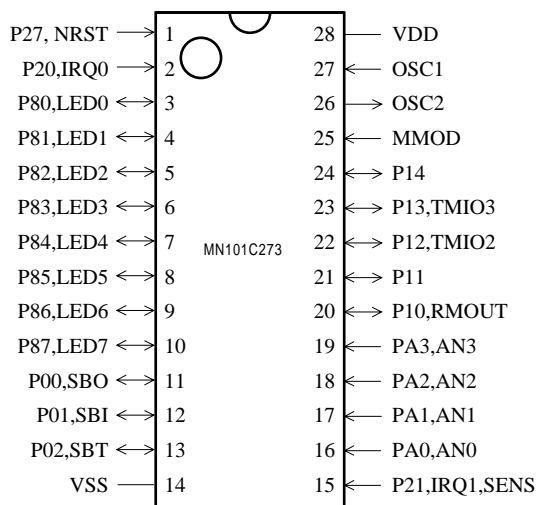
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8.39 MHz, VDD = 5 V		10	25	mA
Supply current at HALT	IDD2	fosc = 8.39 MHz, VDD = 5 V		1.2	3	mA
Supply current at STOP	IDD3	VDD = 5 V, Ta = 25°C			2	μA
		VDD = 5 V, Ta = -40°C to +85°C			20	μA

Pin Assignment

() : Conventional Package



SDIP028-P-0400D *Lead-free
(SDIP028-P-0400)

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C27-SDIP028-P-0400	
EPROM Built-in Type	Type	MN101CP273
	ROM (× 8-bit)	4 K
	RAM (× 8-bit)	0.5 K
	Minimum instruction execution time	0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)
	Package	SDIP028-P-0400D *Lead-free
	(Conventional Package)	(SDIP028-P-0400)

□ MN101C425 , MN101C427

Type	MN101C425		MN101C427	
ROM (×8-bit)	8 K		16 K	
RAM (×8-bit)	0.25 K		0.5 K	
Package (Conventional Package)	SDIP042-P-0600C *Lead-free, TQFP048-P-0707B *Lead-free, QFP044-P-1010F *Lead-free (SDIP042-P-0600)			
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 0.477 μs (at 2.0 V to 5.5 V, 4.19 MHz)* 125 μs (at 2.0 V to 5.5 V, 32.768 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.			
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 (only 48-pin package) • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • A/D conversion finish			
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency (only 48-pin package); external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency (only 48-pin package) Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>			
Serial Interface	Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; output of timer counter 3			
I/O Pins	I/O	27	• Common use: 16 • Specified pull-up resistor available • Input/output selectable (bit unit): 26 (for 44-pin), 25 (for 42-pin)	
	Input	12	• Common use • Specified pull-up resistor available	
A/D Inputs	10-bit × 8-ch. (with S/H)			
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port			

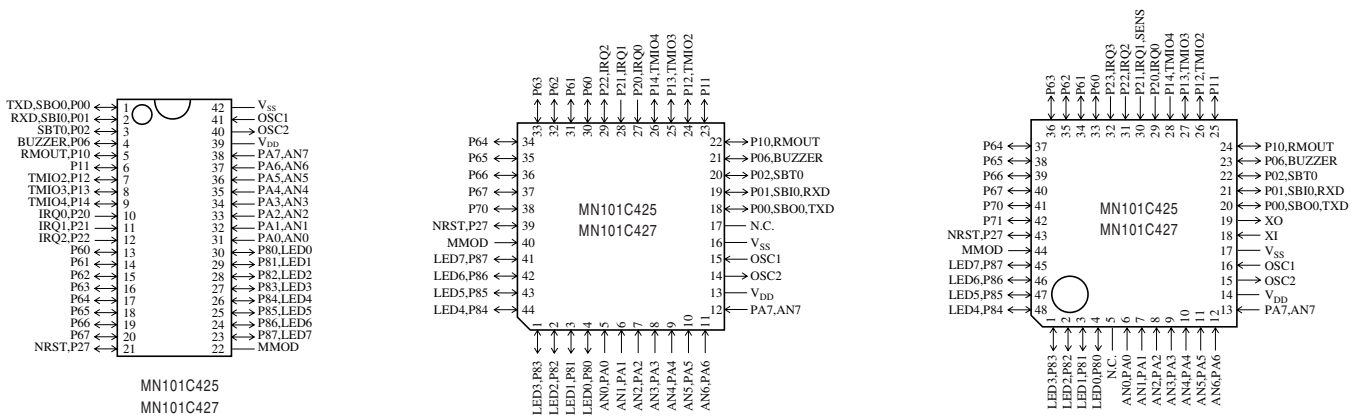
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		15	40	mA
	IDD2	fosc = 8.39 MHz, VDD = 5 V		6	18	mA
	IDD3	fx = 32.768 kHz, VDD = 3 V			100	μA
Supply current at HALT	IDD4	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C			8	μA
	IDD5	fx = 32.768 kHz, VDD = 3 V, Ta = -40°C to +85°C			18	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
		VDD = 5 V, Ta = -40°C to +85°C			20	μA

Pin Assignment

() : Conventional Package



SDIP042-P-0600C *Lead-free
(SDIP042-P-0600)

QFP044-P-1010F *Lead-free

TQFP048-P-0707B *Lead-free

Support Tool

In-circuit Emulator

PX-ICE101C/D+PX-PRB101C42-QFP044-P-1010
 PX-ICE101C/D+PX-PRB101C42-TQFP048-P-0707B
 PX-ICE101C/D+PX-PRB101C42-SDIP042-P-0600

EPROM Built-in Type

Type	MN101CP427DP, MN101CP427BF, MN101CP427HT
ROM (× 8-bit)	16 K
RAM (× 8-bit)	0.5 K
Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
	0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)
Package	[All lead-free] SDIP042-P-0600C, TQFP048-P-0707B, QFP044-P-1010F (Conventional Package) (SDIP042-P-0600)

□ MN101C457

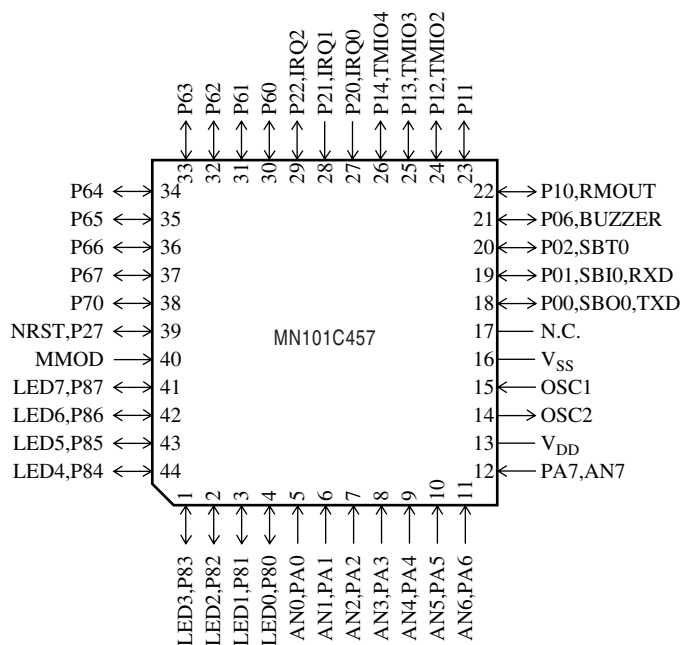
Type	MN101C457		
ROM (×8-bit)	16 K		
RAM (×8-bit)	0.5 K		
Package	QFP044-P-1010F *Lead-free		
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 0.477 μs (at 2.0 V to 5.5 V, 4.19 MHz)*		
* The lower limit for operation guarantee for EPROM built-in type is 2.7 V.			
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • A/D conversion finish		
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>		
Serial Interface	Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; pulse output of timer counter 3		
I/O Pins	I/O	26	• Common use: 16 • Specified pull-up resistor available • Input/output selectable (bit unit): 26
	Input	11	• Common use • Specified pull-up resistor available
A/D Inputs	10-bit × 8-ch. (with S/H)		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		15	40	mA
	IDD2	fosc = 8.39 MHz, VDD = 5 V		6	18	mA
Supply current at STOP	IDD3	VDD = 5 V, Ta = 25°C			2	μA
	IDD4	VDD = 5 V, Ta = -40°C to +85°C			20	μA

Pin Assignment



QFP044-P-1010F *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C42-QFP044-P-1010		
EPROM Built-in Type	Type	MN101CP457BF	
	ROM (× 8-bit)	16 K	
	RAM (× 8-bit)	0.5 K	
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)	
		0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)	
Package	QFP044-P-1010F *Lead-free		

□ MN101C539

Type	MN101C539		
ROM (x8-bit)	24 K (External memory can not be expanded)		
RAM (x8-bit)	0.5 K (External memory can not be expanded)		
Package	TQFP048-P-0707B *Lead-free		
Minimum Instruction Execution Time	High speed mode: 0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 1.00 μs (at 2.0 V to 5.5 V, 4 MHz)* Low speed mode: 61.04 μs (at 2.0 V to 5.5 V, 32.768 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.		
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • Timer 2 • Timer 3 • Timer 6 • Time Base • Serial 0 (2 systems) • A/D conversion finish • Timer 7 (2 systems)		
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p> <p>Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p>		
Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency		
I/O Pins	I/O	36	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	4	• Common use • Specified pull-up resistor available

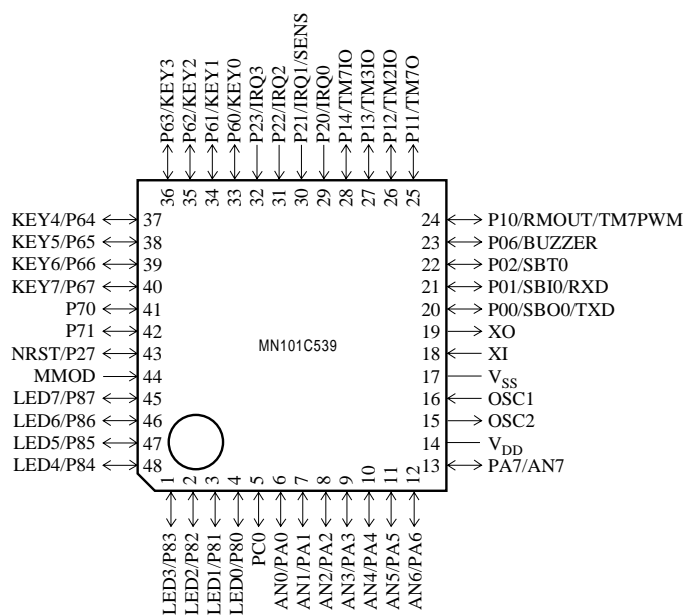
A/D Inputs 10-bit × 8-ch. (with S/H)

Special Ports Buzzer output, remote control carrier signal output, high-current drive port

Electrical Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	$f_{osc} = 20 \text{ MHz}, V_{DD} = 5 \text{ V}$		20	50	mA
	IDD2	$f_{osc} = 8.39 \text{ MHz}, V_{DD} = 5 \text{ V}$		10	20	mA
	IDD3	$f_x = 32.768 \text{ kHz}, V_{DD} = 3 \text{ V}$		20	70	μA
Supply current at HALT	IDD4	$f_x = 32.768 \text{ kHz}, V_{DD} = 3 \text{ V}, T_a = 25^\circ\text{C}$		2	6	μA
	IDD5	$f_x = 32.768 \text{ kHz}, V_{DD} = 3 \text{ V}, T_a = -40^\circ\text{C to } +85^\circ\text{C}$			15	μA
Supply current at STOP	IDD6	$V_{DD} = 5 \text{ V}, T_a = 25^\circ\text{C}$			2	μA
		$V_{DD} = 5 \text{ V}, T_a = -40^\circ\text{C to } +85^\circ\text{C}$			20	μA

Pin Assignment



TQFP048-P-0707B *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C53-TQFP048-P-0707B-M	
EPROM Built-in Type	Type	MN101CP539HT
	ROM (× 8-bit)	24 K
	RAM (× 8-bit)	0.5 K
	Minimum instruction execution time	High speed mode: 0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 1.00 μs (at 2.7 V to 5.5 V, 4 MHz) Low speed mode: 61.04 μs (at 2.7 V to 5.5 V, 32.768 kHz)
	Package	TQFP048-P-0707B *Lead-free

□ MN101C309 , MN101C30A

Type	MN101C309	MN101C30A
ROM (×8-bit) External memory can be expanded	24 K	32 K
RAM (×8-bit) External memory can be expanded	1 K	1.5 K
Package	LQFP064-P-1414 *Lead-free	
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 1.00 μs (at 2.0 V to 5.5 V, 2 MHz)* 125 μs (at 2.0 V to 5.5 V, 32.768 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.	
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time Base • Serial 0 • Serial 1 • Automatic transfer finish • A/D conversion finish	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier) Clock source 1/1, 1/4 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/16, 1/64 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>	

Serial Interface		Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency	
		Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; output of timer counter 3	

I/O Pins	I/O	41	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	13	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 8-ch. (with S/H)
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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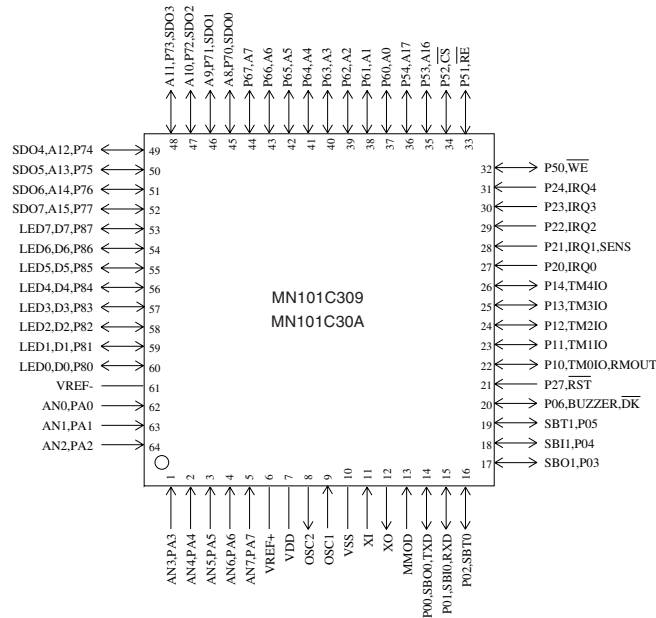
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fx = 32.768 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD3	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
		fx = 32.768 kHz, VDD = 3 V, Ta = 85°C			18	μA
Supply current at STOP	IDD4	VDD = 5 V, Ta = 25°C			2	μA
		VDD = 5 V, Ta = -40°C to +85°C			20	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C30-LQFP064-P-1414	
EPROM Built-in Type	Type	MN101CP30ABL
	ROM (× 8-bit)	32 K
	RAM (× 8-bit)	1.5 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.238μs (at 2.7 V to 5.5 V, 8 MHz)
	Package	LQFP064-P-1414 *Lead-free

MN101C309 , MN101C30A □

□ MN101C28A , MN101C28C , MN101C28D , MN101C28F , MN101C28L

Type	MN101C28A	MN101C28C	MN101C28D	MN101C28F	MN101C28L
ROM (x8-bit) External memory can be expanded	32 K	48 K	64 K	96 K	96 K
RAM (x8-bit) External memory can be expanded	1.5 K	2 K	2 K	4 K	10 K
Package (Conventional Package)	[All lead-free] LQFP080-P-1414A, TQFP080-P-1212D, QFP084-P-1818E (TQFP080-P-1212C)			LQFP080-P-1414A *Lead-free	
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.6 V to 5.5 V, 8.39 MHz) 0.333 μs (at 2.3 V to 5.5 V, 6 MHz) 1.00 μs (at 2.0 V to 5.5 V, 2 MHz)* 125 μs (at 2.0 V to 5.5 V, 32.768 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V.				
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • Serial 2 • Automatic transfer finish • A/D conversion finish 				
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier) Clock source 1/1, 1/4 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/16, 1/64 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>				

MN101C28A , MN101C28C , MN101C28D □
MN101C28F , MN101C28L

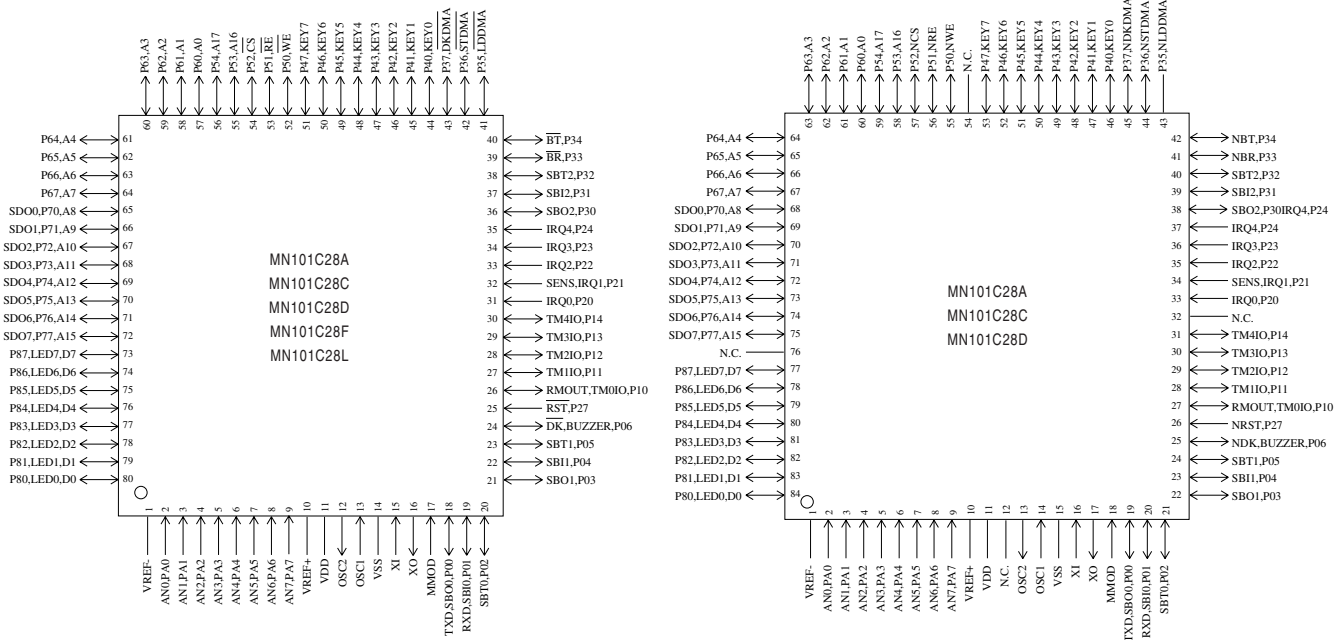
Serial Interface	Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; output of timer counter 3		
	Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; output of timer counter 3		
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/4, 1/8, 1/16, 1/32 of system clock frequency; 1/4 of timer counter 0 frequency		
I/O Pins	I/O	57	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	13	• Common use • Specified pull-up resistor available
A/D Inputs	10-Bit × 8-ch. (with S/H)		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port		

Electrical Characteristics						
Supply current						
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	50	mA
	IDD2	fx = 32.768 kHz, VDD = 3 V		40	120	μA
Supply current at HALT	IDD3	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
		fx = 32.768 kHz, VDD = 3 V, Ta = 85°C			20	μA
Supply current at STOP	IDD4	VDD = 5 V, Ta = 25°C			1	μA
		VDD = 5 V, Ta = -40°C to +85°C			30	μA

See the next page for pin assignment and support tool.

Pin Assignment

() : Conventional Package



LQFP080-P-1414A *Lead-free

QFP084-P-1818E *Lead-free

TQFP080-P-1212D *Lead-free [MN101C28A/28C/28D]

(TQFP080-P-1212C)

Support Tool

In-circuit Emulator

PX-ICE101C/D+PX-PRB101C28-TQFP080-P-1212
 PX-ICE101C/D+PX-PRB101C28-QFP084-P-1818E
 PX-ICE101C/D+PX-PRB101C28-LQFP080-P-1414A

EPROM Built-in Type

Type MN101CP28DBF, MN101CP28DAL, MN101CP28DHT,
 MN101CP28LAL

ROM (× 8-bit) 64 K / 64 K / 64 K / 96 K

RAM (× 8-bit) 2 K / 2 K / 2 K / 10 K

Minimum instruction execution time 0.10 μs (at 4.5 V to 5.5 V, 20 MHz)

0.238 μs (at 2.6 V to 5.5 V, 8.39 MHz)

0.333 μs (at 2.3 V to 5.5 V, 6 MHz)

Package [All lead-free] LQFP080-P-1414A, TQFP080-P-1212D, QFP084-P-1818E

(Conventional Package) (TQFP080-P-1212C)

**MN101C28A , MN101C28C , MN101C28D □
MN101C28F , MN101C28L**

□ MN101C51F

Type	MN101C51F
ROM (×8-bit)	96 K (External memory can be expanded)
RAM (×8-bit)	6 K (External memory can be expanded)
Package	LQFP080-P-1414A *Lead-free
Minimum Instruction Execution Time	0.10 μs (4.5 V to 5.5 V, 20 MHz) 0.238 μs (2.6 V to 5.5 V, 8.39 MHz) 0.333 μs (2.3 V to 5.5 V, 6 MHz) 1.00 μs (2.0 V to 5.5 V, 2 MHz) 125 μs (2.0 V to 5.5 V, 32.768 kHz)
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time Base • Serial 0 • Serial 1 • Serial 2 • Automatic transfer finish • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier) Clock source 1/1, 1/4 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/16, 1/64 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/1048576 of system clock frequency</p>

Serial Interface	Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency
	Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; 1/2 of timer counter 3 frequency
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/4, 1/8, 1/16, 1/32 of system clock frequency; 1/4 of timer counter 0 frequency

I/O Pins	I/O	57	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	13	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 8-ch. (with S/H)
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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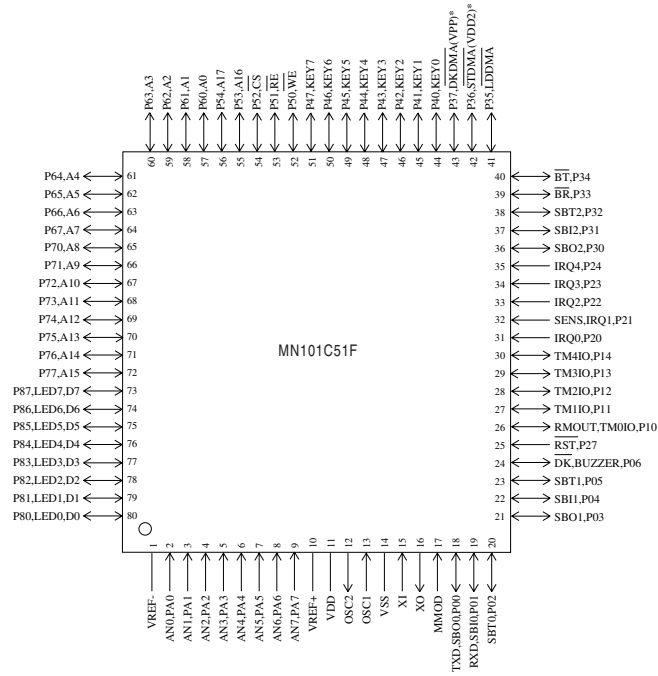
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V			50	mA
	IDD2	fx = 32.768 kHz, VDD = 3 V			120	μA
Supply current at HALT	IDD3	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C			8	μA
		fx = 32.768 kHz, VDD = 3 V, Ta = 85°C			20	μA
Supply current at STOP	IDD4	VDD = 5 V, Ta = 25°C			1	μA
		VDD = 5 V, Ta = 85°C			30	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP080-P-1414A *Lead-free

Support Tool

In-circuit Emulator

PX-ICE101C/D+PX-PRB101C51-LQFP080-P-1414A

□ MN101C61D, MN101C61G

Type	MN101C61D (under development)	MN101C61G
ROM (x8-bit)	64 K	128 K
RAM (x8-bit)	3 K	12 K

Package TQFP080-P-1212D *Lead-free

Minimum Instruction Execution Time	Standard:	0.1 μs (at 2.5 V to 3.6 V, 20 MHz) 0.2 μs (at 2.1 V to 3.6 V, 10 MHz) 0.5 μs (at 1.8 V to 3.6 V, 4 MHz)* 125 μs (at 1.8 V to 3.6 V, 32 kHz)*
	Double speed:	0.1 μs (at 2.5 V to 3.6 V, 10 MHz) 0.2 μs (at 2.1 V to 3.6 V, 5 MHz) 0.5 μs (at 1.8 V to 3.6 V, 2 MHz)* 62.5 μs (at 1.8 V to 3.6 V, 32 kHz)*

* The operation guarantee range for flash memory built-in type is 2.2V to 3.0 V or 2.7V to 3.6 V.

Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Timer 6 • Time base • Serial 0 reception • Serial 0 transmission • Serial 1 reception • Serial 1 transmission • Serial 2 • Serial 3 • Automatic transfer finish • A/D conversion finish • Timer 7 (2 systems) • Key interrupts (8 lines)
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Timer Counter	Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0
	Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1
	Timer counter 0, 1 can be cascade-connected.
	Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2
	Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3
	Timer counter 2, 3 can be cascade-connected.
	Timer counter 4 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 1 baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; 1/1 of external clock input frequency Interrupt source coincidence with compare register 4
	Timer counter 5 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 0 baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; 1/1 of external clock input frequency Interrupt source coincidence with compare register 5

Timer Counter (Continue)	<p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture)</p> <p>Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency</p> <p>Interrupt source coincidence with compare register 7 (2 lines)</p> <p>Time base timer (one-minute count setting)</p> <p>Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency</p> <p>Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency</p> <p>Watchdog timer</p> <p>Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p> <p>DMA controller (automatic data transfer)</p> <p>Max. Transfer cycles 255</p> <p>Starting factor external request, various types of interrupt, software</p> <p>Transfer mode 1-byte transfer, word transfer, burst transfer</p>
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Serial Interface	<p>Serial 0 : synchronous type / UART (full-duplex) × 1</p> <p>Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 5; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p> <p>Serial 1 : synchronous type / UART (full-duplex) × 1</p> <p>Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p> <p>Serial 2 : synchronous type × 1</p> <p>Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency</p> <p>Serial 3 : synchronous type/single-master I²C × 1</p> <p>Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency</p>
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I/O Pins	I/O	62	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	6	• Common use • Specified pull-up resistor available

A/D Inputs	10-Bit × 6-ch. (with S/H)
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

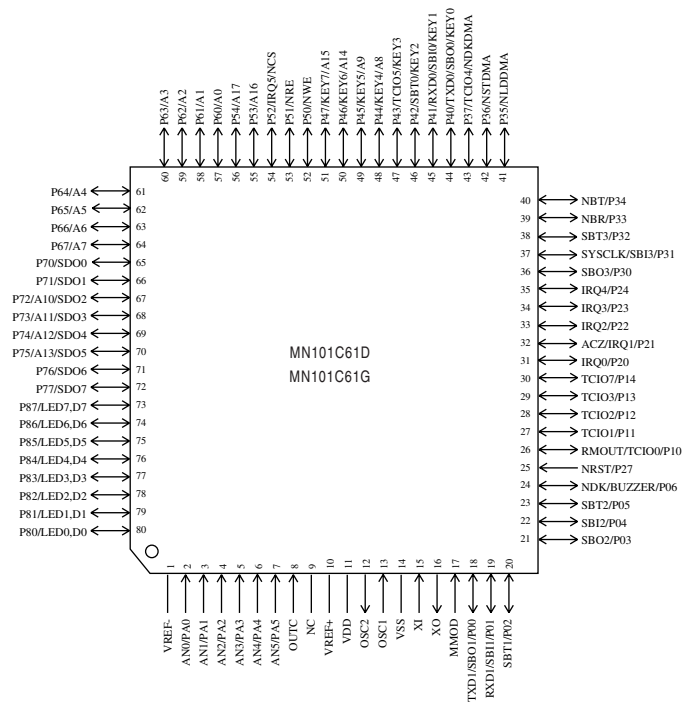
Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 3 V, (fs = fosc/2)		5	12	mA
	IDD2	fosc = 8.39 MHz, VDD = 3 V, (fs = fosc/2)		2	5	mA
	IDD3	fx = 32.768 kHz, VDD = 3 V, (fs = fx/2)			40	μA
Supply current at HALT	IDD4	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32.768 kHz, VDD = 3 V			30	μA
Supply current at STOP	IDD6	VDD = 3 V, Ta = 25°C			2	μA
	IDD7	VDD = 3 V			20	μA

Ta = -40°C to +85°C, VDD = 1.8 V to 3.6 V, VSS = 0 V

Note) Ta = -20°C to +70°C for a flash memory built-in version. Supply voltage range and supply current ratings are also different from the values mentioned above. Refer to Chapter 18 “Flash EEPROM” for details

Pin Assignment



TQFP080-P-1212D *Lead-free

NC serves as the VPP pin in the MN101CF61G, and cannot be used as a user pin.

Support Tool

■ In-circuit Emulator	PX-ICE101C / D + PX-PRB101C61-TQFP080-P-1212-M	
■ Flash Memory Built-in Type	Type	MN101CF61G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	12 K
	Minimum instruction execution time	0.1 μs (at 2.7 V to 3.6 V, 20 MHz)
		0.2 μs (at 2.7 V to 3.6 V, 10 MHz)
		0.5 μs (at 2.7 V to 3.6 V, 4 MHz)
		125 μs (at 2.7 V to 3.6 V, 32 kHz)
	Package	TQFP080-P-1212D *Lead-free
	Type	MN101CF60G
	ROM (× 8-bit)	128 K
RAM (× 8-bit)	12 K	
Minimum instruction execution time	0.1 μs (at 2.5 V to 3.0 V, 20 MHz)	
	0.2 μs (at 2.2 V to 3.0 V, 10 MHz)	
	0.5 μs (at 2.2 V to 3.0 V, 4 MHz)	
	125 μs (at 2.2 V to 3.0 V, 32 kHz)	
Package	TQFP080-P-1212D *Lead-free	

□ MN101C62D, MN101C62F

Type	MN101C62D	MN101C62F
ROM (×8-bit)	64 K	96 K
RAM (×8-bit)	2 K	4 K
Package	LQFP080-P-1414A *Lead-free	
Minimum Instruction Execution Time	Standard: 0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 1.00 μs (at 2.0 V to 5.5 V, 2 MHz)* 125 μs (at 2.0 V to 5.5 V, 32 kHz)*	Double speed: 0.125 μs (at 4.5 V to 5.5 V, 8 MHz) 0.25 μs (at 3.0 V to 5.5 V, 4 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)*
Interrupts	<ul style="list-style-type: none"> • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Automatic transfer completion • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 2 • A/D conversion finish • Key interrupt 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event, serial baud rate timer)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, event count, synchronous output event, simple pulse width measurement, generation of real time, serial baud rate timer)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial baud rate timer)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p> <p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p>	

Timer Counter (Continue)	Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, generation of real time) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency
	Timer counter 8 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, generation of real time) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/8 of timer counter 2 output; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type / single-master I ² C Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/8, 1/32 of OSC oscillation clock frequency

I/O Pins	I/O	68	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
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A/D Inputs	10-bit × 8-ch. (with S/H)
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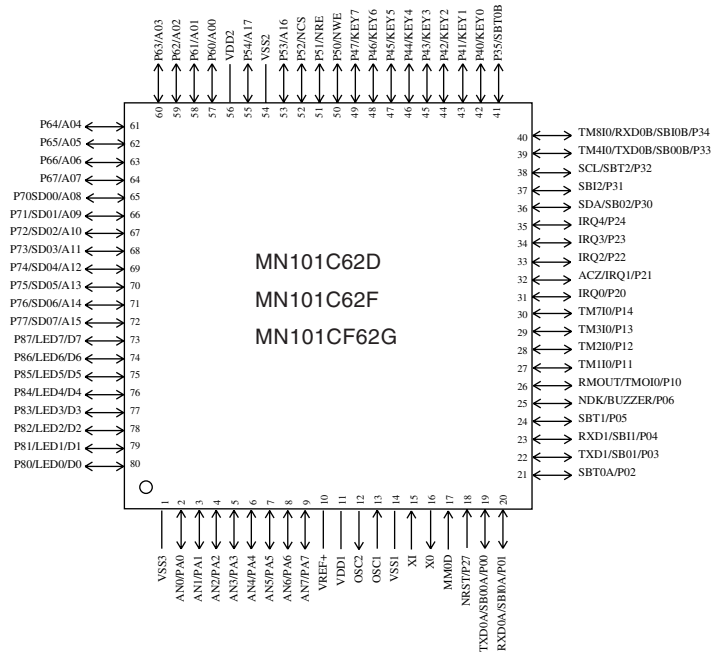
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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Electrical Characteristics						
Supply current						
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	$f_{osc} = 20 \text{ MHz}, V_{DD} = 5 \text{ V}$		15(20)	30(40)	mA
	IDD2	$f_x = 32 \text{ kHz}, V_{DD} = 3 \text{ V}$		30(50)	60(120)	μA
Supply current at HALT	IDD3	$f_x = 32 \text{ kHz}, V_{DD} = 3 \text{ V}, T_a = 25^\circ\text{C}$		6	8	μA
	IDD4	$f_x = 32 \text{ kHz}, V_{DD} = 3 \text{ V}, T_a = 85^\circ\text{C}$			30	μA
Supply current at STOP	IDD5	$V_{DD} = 5 \text{ V}, T_a = 25^\circ\text{C}$			2	μA
	IDD6	$V_{DD} = 5 \text{ V}, T_a = 85^\circ\text{C}$			50	μA

() : Flash memory built-in type

See the next page for pin assignment and support tool.

Pin Assignment



LQFP080-P-1414A *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C62-LQFP080-P-1414A-M	
Flash Memory Built-in Type	Type	MN101CF62G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	10 K
	Minimum instruction execution time	Standard: 0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 1.0 μs (at 2.5 V to 5.5 V, 2 MHz) 125 μs (at 2.5 V to 5.5 V, 32 kHz) Double speed: 0.125 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 3.0 V to 5.5 V, 8 MHz) 62.5 μs (at 2.7 V to 5.5 V, 32 kHz)
	Package	LQFP080-P-1414A *Lead-free

MN101C62D , MN101C62F □

□ MN101C67D, MN101C67G

Type	MN101C67D	MN101C67G
ROM (×8-bit)	64 K	128 K
RAM (×8-bit)	6 K	10 K
Package	TQFP080-P-1212D *Lead-free	
Minimum Instruction Execution Time	Standard: 0.1 μs (at 2.5 V to 3.6 V, 20 MHz)* 0.2 μs (at 2.1 V to 3.6 V, 10 MHz)* 0.5 μs (at 1.8 V to 3.6 V, 4 MHz)* 62.5 μs (at 1.8 V to 3.6 V, 32 kHz)* Double speed: 0.119 μs (at 2.5 V to 3.6 V, 8.39 MHz)* * The operation guarantee range for flash memory built-in type is 2.7 V to 3.6 V.	
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Timer 6 • Time base • Serial 0 reception • Serial 0 transmission • Serial 1 reception • Serial 1 transmission • Serial 2 • Serial 3 • Serial 4 • Automatic transfer finish • A/D conversion finish • Timer 7 (2 systems) • Key interrupts (8 lines) 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 1 baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; 1/1 of external clock input frequency Interrupt source coincidence with compare register 4</p> <p>Timer counter 5 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 0 baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; 1/1 of external clock input frequency Interrupt source coincidence with compare register 5</p>	

Timer Counter (Continue)	<p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p> <p>Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p> <p>DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer</p>
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Serial Interface	<p>Serial 0 : synchronous type / UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 5; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p> <p>Serial 1 : synchronous type / UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p> <p>Serial 2 : synchronous type × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency</p> <p>Serial 3 : synchronous type/single-master I²C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency</p> <p>Serial 4 : I²C slave × 1 Applicable for I²C high-speed transfer mode, 7 bit/10bit address setting, general call</p>
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I/O Pins	I/O	62	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	7	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 7-ch. (with S/H)
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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See the next page for electrical characteristics, pin assignment and support tool.

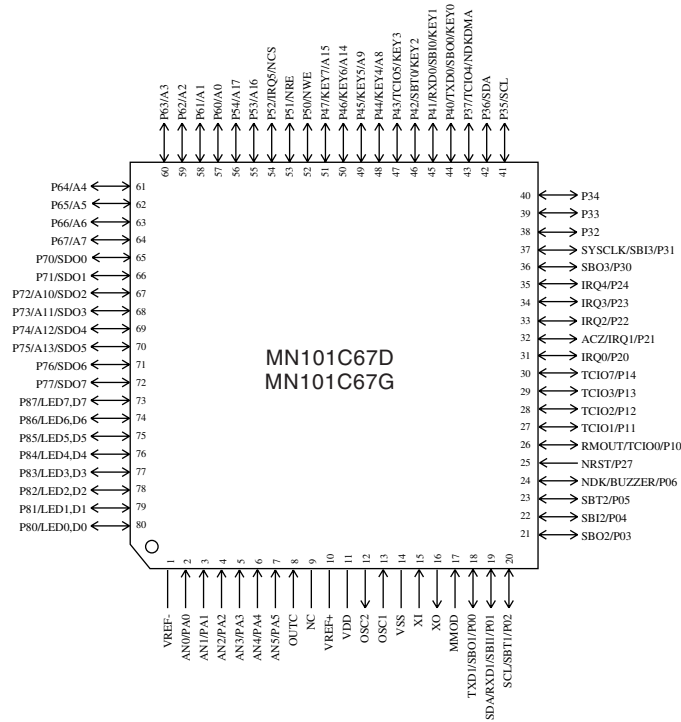
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 3 V, (fs = fosc/2)		5	12	mA
	IDD2	fosc = 8.39 MHz, VDD = 3 V, (fs = fosc/2)		2	5	mA
	IDD3	fx = 32.768 kHz, VDD = 3 V, (fs = fx/2)			40	μA
Supply current at HALT	IDD4	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32.768 kHz, VDD = 3 V			30	μA
Supply current at STOP	IDD6	VDD = 3 V, Ta = 25°C			2	μA
	IDD7	VDD = 3 V, Ta = 85°C			20	μA

Ta = -40°C to +85°C, VDD = 1.8 V to 3.6 V, VSS = 0 V

Pin Assignment



TQFP080-P-1212D *Lead-free

NC serves as the VPP pin in the MN101CF67G, and cannot be used as a user pin.

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C67-TQFP080-P-1212-M	
Flash Memory Built-in Type	Type	MN101CF67G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	10 K
	Minimum instruction execution time	Standard: 0.1 μs (at 2.7 V to 3.6 V, 20 MHz)
	Package	TQFP080-P-1212D *Lead-free

□ MN101E16K, MN101E16L, MN101E16M

Type	MN101E16K	MN101E16L (under planning)	MN101E16M (under development)
ROM (×8-bit) External memory can be expanded	256 K	320 K	384 K
RAM (×8-bit) External memory can be expanded	12 K	14 K	20 K
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under development)		
Minimum Instruction Execution Time	0.0588 μs (at 2.7 V to 3.6 V, 17 MHz at internal 2,4,8 times oscillation used) 0.1 μs (at 2.7 V to 3.6 V, 20 MHz) 30.6 μs (at 2.7 V to 3.6 V, 32.768 kHz)		
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Timer 6 • Timer 7 (2 systems) • Timer A, B, C, D, E • Time base • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 2 • Serial 3 (3 systems) • Serial 4 (2 systems) • Automatic transfer finish (2 systems) • A/D conversion finish • Key interrupts 		
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, simple pulse width measurement, real time output control)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event, 16-bit timer with cascade connection (Timer 0 and connection), serial clock output)</p> <p>Clock source 1/2, 1/8 of system clock frequency 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement, real time output control, serial baud rate timer)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 2</p> <p>Timer counter 0, 1, 2 can be cascade-connected.</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, serial baud rate timer)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 0, 1, 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer, time base timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt generating cycle ... 1/128, 1/256, 1/512, 1/1024, 1/8192 1/32768 of OSC oscillation clock frequency 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p>		

Timer Counter (Continue)	Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)
	Timer counter A, B, C, D, E : 8-bit × 5 Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of OSC oscillation clock frequency Interrupt source coincidence with compare register A, B, C, D, E
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576, 1/4194304 of system clock frequency
	DMA controller (automatic data transfer) × 2-ch. Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, A; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3, B; 1/2, 1/4, 1/8, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3, C; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency
	Serial 3 : synchronous type/I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, D; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency
	Serial 4 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, E; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency

I/O Pins	I/O	22	• (5 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
		63	• (3 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit)

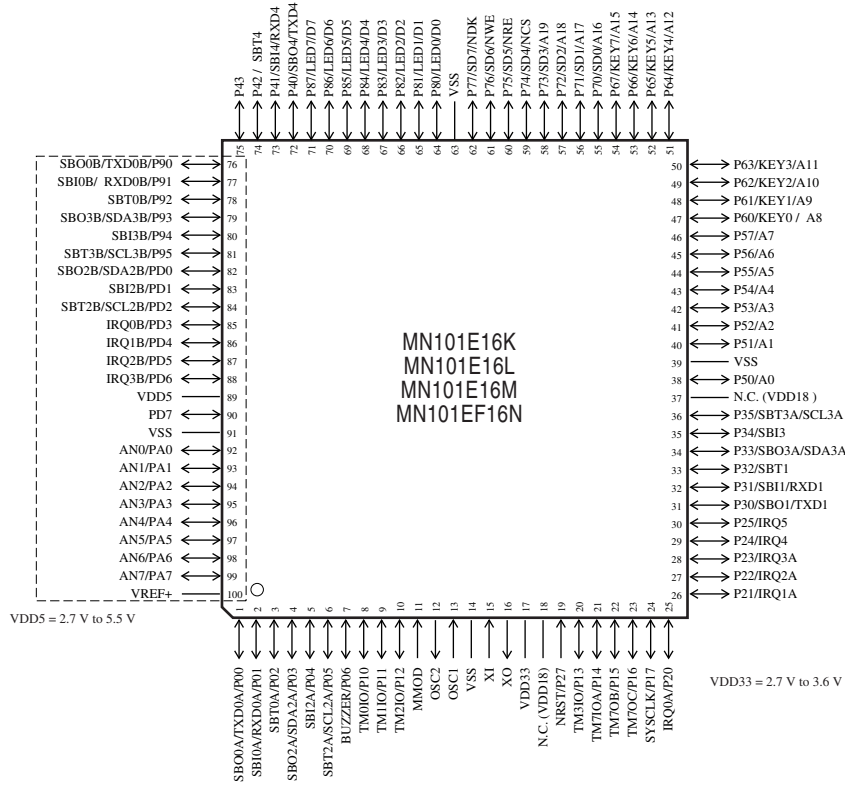
A/D Inputs	10-bit × 8-ch. (with S/H)
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Special Ports	Buzzer output, high-current drive port
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Electrical Characteristics	T.B.D
Supply current	

See the next page for electrical characteristics, pin assignment and support tool.

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free (under planning)

(): Flash memory built-in type

Support Tool

In-circuit Emulator	Under development	
Flash Memory Built-in Type	Type	MN101EF16N (under development)
	ROM (× 8-bit)	512 K
	RAM (× 8-bit)	30 K
	Minimum instruction execution time	0.0588 μs (at 2.7 V to 3.6 V, 17 MHz)
	Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under planning)

MN101E16K, MN101E16L, MN101E16M □

□ MN101C08C

Type	MN101C08C
ROM (x8-bit)	48 K (External memory can be expanded)
RAM (x8-bit)	1.5 K (External memory can be expanded)
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 1.00 μs (at 2.0 V to 5.5 V, 2 MHz)* 125 μs (at 2.0 V to 5.5 V, 32.768 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • Automatic transfer finish • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier) Clock source 1/1, 1/4 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/16, 1/64 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>
Serial Interface	<p>Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; output of timer counter 3</p> <p>Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; output of timer counter 3</p>

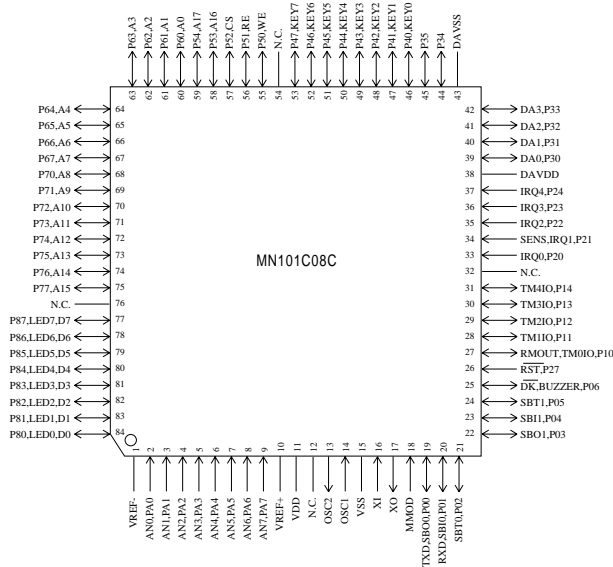
I/O Pins	I/O	55	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	13	• Common use • Specified pull-up resistor available
A/D Inputs	10-bit × 8-ch. (with S/H)		
D/A Outputs	8-bit × 4-ch.		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fx = 32.768 kHz, VDD = 3 V		30	100	µA
Supply current at HALT	IDD3	fx = 32.768 kHz, VDD = 3 V, Ta = 25°C		4	8	µA
		fx = 32.768 kHz, VDD = 3 V, Ta = 85°C			20	µA
Supply current at STOP	IDD4	VDD = 5 V, Ta = 25°C			1	µA
		VDD = 5 V, Ta = -40°C to +85°C			30	µA

Pin Assignment



QFP084-P-1818E *Lead-free

See the next page for support tool.

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C08-QFP084-P-1818E	
EPROM Built-in Type	Type	MN101CP08CBF
	ROM (× 8-bit)	48 K
	RAM (× 8-bit)	1.5 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)
Package	QFP084-P-1818E *Lead-free	

□ MN101C49G , MN101C49H , MN101C49K

Type	MN101C49G	MN101C49H	MN101C49K
ROM (×8-bit) External memory can be expanded	128 K	160 K	224 K
RAM (×8-bit) External memory can be expanded	4 K	6 K	10 K
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free		
Minimum Instruction Execution Time	Standard:	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz) 125 μs (at 2.0 V to 5.5 V, 32 kHz)*	
	Double speed:	0.12 μs (at 4.5 V to 5.5 V, 8.39 MHz) 0.25 μs (at 3.0 V to 5.5 V, 4 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)*	
		* The lower limit for operation guarantee for EPROM built-in type is 2.7 V. * The lower limit for operation guarantee for flash memory built-in type is 4.5 V.	
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Timer 7 (2 systems) • Time base • Serial 0 • Serial 1 • Serial 2 • Serial 3 • Automatic transfer finish • A/D conversion finish • Key interrupts (8 lines)		
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 1 baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; 1/1 of external clock input frequency Interrupt source coincidence with compare register 4</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p>		

Timer Counter (Continue)	Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency
	DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 1 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency
	Serial 3 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency

I/O Pins	I/O	73 (72)	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) () : Flash memory built-in type.
	Input	15 (14)	• Common use • Specified pull-up resistor available () : Flash memory built-in type.

A/D Inputs	10-bit × 8-ch. (with S/H)
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D/A Outputs	8-bit × 4-ch.
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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See the next page for electrical characteristics, pin assignment and support tool.

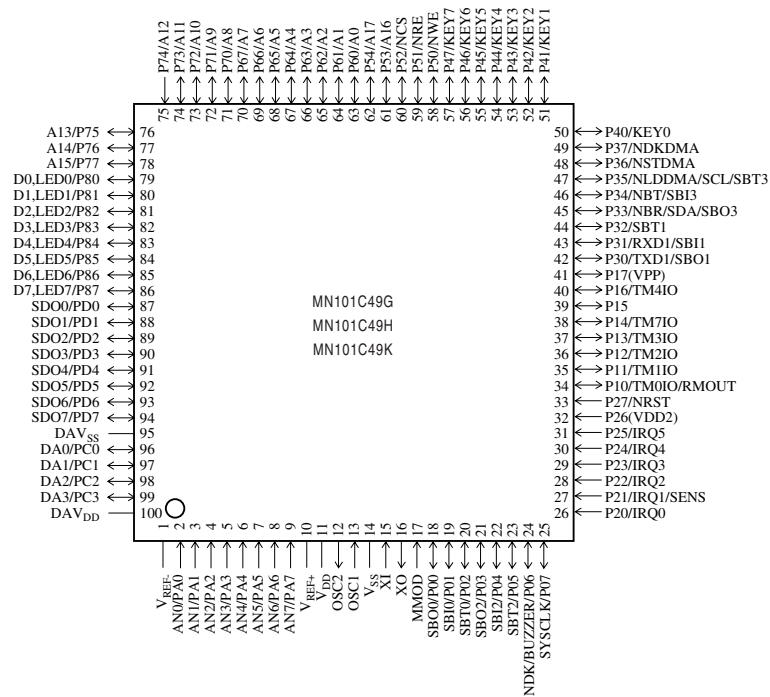
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		30	70	mA
	IDD2	fosc = 8.39 MHz, VDD = 5 V		15	30	mA
	IDD3	fx = 32.768 kHz, VDD = 3 V		40	120	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V (5 V), Ta = 25°C		5 (13)	11 (30)	μA
	IDD5	fx = 32.768 kHz, VDD = 3 V (5 V), Ta = 85°C			30 (90)	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			3	μA
	IDD7	VDD = 5 V, Ta = 85°C			60	μA

() : Flash memory built-in type.

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free

() : Flash memory built-in type.

Support Tool

■ In-circuit Emulator	PX-ICE101C / D + PX-PRB101C49-QFP100-P-1818B		
	PX-ICE101C / D + PX-PRB101C49-LQFP100-P-1414		
■ EPROM Built-in Type	Type	MN101CP49K	
	ROM (× 8-bit)	224 K	
	RAM (× 8-bit)	10 K	
	Minimum instruction execution time	Standard:	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
			0.25 μs (at 2.7 V to 5.5 V, 8.39 MHz)
		Double speed:	0.12 μs (at 4.5 V to 5.5 V, 8.39 MHz)
0.25 μs (at 3.0 V to 5.5 V, 4 MHz)			
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free		
■ Flash Memory Built-in Type	Type	MN101CF49K	
	ROM (× 8-bit)	224 K	
	RAM (× 8-bit)	10 K	
	Minimum instruction execution time	Standard:	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		Double speed:	0.12 μs (at 4.5 V to 5.5 V, 8.39 MHz)
	Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free	

□ MN101C77A, MN101C77C

Type	MN101C77A (under development)	MN101C77C
ROM (×8-bit)	32 K	48 K
RAM (×8-bit)	1.5 K	3 K

Package LQFP064-P-1414 *Lead-free, TQFP064-P-1010C *Lead-free

Minimum Instruction Execution Time	Standard:	0.1 μs (at 2.5 V to 3.6 V, 20 MHz)*
		0.2 μs (at 2.1 V to 3.6 V, 10 MHz)*
		0.5 μs (at 1.8 V to 3.6 V, 4 MHz)*
		62.5 μs (at 1.8 V to 3.6 V, 32 kHz)*
		Double speed: 0.119 μs (at 2.5 V to 3.6 V, 8.39 MHz)*

* The operation guarantee range for flash memory built-in type is 2.7 V to 3.6 V.

Interrupts

- RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4
- Timer 0 • Timer 1 • Timer 4 • Timer 5 • Timer 6 • Time base
- Serial 0 reception • Serial 0 transmission • Serial 1 reception • Serial 1 transmission • Serial 3
- Serial 4 • Automatic transfer finish • A/D conversion finish • Timer 7 (2 systems) • Key interrupts (8 lines)

Timer Counter

Timer counter 0 : 8-bit × 1
 (square-wave/8-bit PWM output, event count, generation of remote control carrier, pulse width measurement)
 Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
 Interrupt source coincidence with compare register 0

Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event)
 Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input
 Interrupt source coincidence with compare register 1

Timer counter 0, 1 can be cascade-connected.

Timer counter 4 : 8-bit × 1
 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 1 baud rate timer)
 Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency;
 1/1 of external clock input frequency
 Interrupt source coincidence with compare register 4

Timer counter 5 : 8-bit × 1
 (square-wave/8-bit PWM output, event count, pulse width measurement, serial 0 baud rate timer)
 Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency;
 1/1 of external clock input frequency
 Interrupt source coincidence with compare register 5

Timer Counter (Continue)	Timer counter 6 : 8-bit freerun timer
	Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency
	Interrupt source coincidence with compare register 6
	Timer counter 7 : 16-bit × 1
	(square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture)
	Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency
	Interrupt source coincidence with compare register 7 (2 lines)
	Time base timer (one-minute count setting)
	Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency
	Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency
Watchdog timer	
Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency	
DMA controller (automatic data transfer)	
Max. Transfer cycles 255	
Starting factor external request, various types of interrupt, software	
Transfer mode 1-byte transfer, word transfer, burst transfer	

Serial Interface	Serial 0 : synchronous type / UART (full-duplex) × 1
	Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 5; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 1 : synchronous type / UART (full-duplex) × 1
	Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 3 : synchronous type/single-master I ² C × 1
Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency	
Serial 4 : I ² C slave × 1	
Applicable for I ² C high-speed transfer mode, 7 bit/10bit address setting, general call	

I/O Pins	I/O	53	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
A/D Inputs		10-bit × 7-ch. (with S/H)	
D/A Outputs		8-bit × 2-ch. (Serves as AD pin, as well)	
Special Ports		Buzzer output, remote control carrier signal output, high-current drive port	

See the next page for electrical characteristics, pin assignment and support tool.

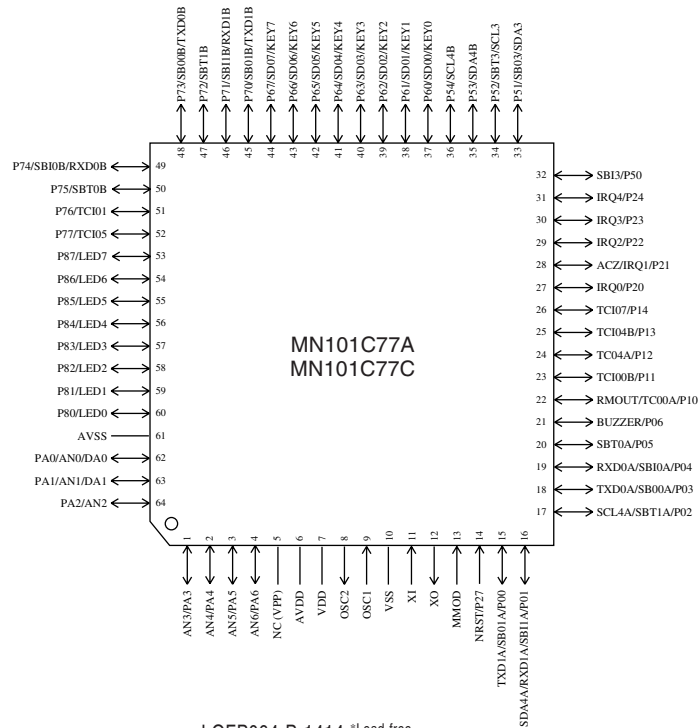
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 3.3 V, (fs = fosc/2)		6	12	mA
	IDD2	fosc = 8.39 MHz, VDD = 3.3 V, (fs = fosc/2)		3	6	mA
	IDD3	fx = 32.768 kHz, VDD = 3.3 V, (fs = fx/2)			40	μA
Supply current at HALT	IDD4	fx = 32.768 kHz, VDD = 3.3 V, Ta = 25°C		5	10	μA
	IDD5	fx = 32.768 kHz, VDD = 3.3 V			40	μA
Supply current at STOP	IDD6	VDD = 3.3 V, Ta = 25°C		0	2	μA
	IDD7	VDD = 3.3 V, Ta = 85°C			30	μA

Ta = -40°C to +85°C, VDD = 1.8 V to 3.6 V, VSS = 0 V

Pin Assignment



LQFP064-P-1414 *Lead-free

TQFP064-P-1010C *Lead-free (under development)

NC serves as the VPP pin in the MN101CF77G, and cannot be used as a user pin.

Support Tool

■ In-circuit Emulator	PX-ICE101C/D;PX-PRB101C77-TQFP064-P1010C		
	PX-ICE101C/D;PX-PRB101C77-LQFP064-P1414		
■ Flash Memory Built-in Type	Type	MN101CF77G	
	ROM (× 8-bit)	128 K	
	RAM (× 8-bit)	6 K	
	Minimum instruction execution time	Standard: 0.1 μs (at 2.7 V to 3.6 V, 20 MHz)	
	Package	LQFP064-P-1414 *Lead-free	
		TQFP064-P-1010C *Lead-free (under development)	

Support Tool

■ In-circuit Emulator	PX-ICE101C/D;PX-PRB101C77-TQFP064-P1010C		
	PX-ICE101C/D;PX-PRB101C77-LQFP064-P1414		
■ Flash Memory Built-in Type	Type	MN101CF77G	
	ROM (× 8-bit)	128 K	
	RAM (× 8-bit)	6 K	
	Minimum instruction execution time	Standard: 0.1 μs (at 2.7 V to 3.6 V, 20 MHz)	
	Package	LQFP064-P-1414 *Lead-free	
		TQFP064-P-1010C *Lead-free (under development)	

□ MN101E01J, MN101E01K, MN101E01L, MN101E01M

Type	MN101E01J	MN101E01K	MN101E01L	MN101E01M
ROM (×8-bit) External memory can be expanded	192 K	256 K	320 K	384 K
RAM (×8-bit) External memory can be expanded	10 K	10 K	14 K	20 K
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free			
Minimum Instruction Execution Time	Standard: 0.0625 μs (at 3.0 V to 3.6 V, 32 MHz) 0.1 μs (at 3.0 V to 3.6 V, 20 MHz) 62.5 μs (at 3.0 V to 3.6 V, 32 kHz) Double speed: 0.10 μs (at 3.0 V to 3.6 V, 10 MHz)			
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Timer 6 • Timer 7 (2 systems) • Time base • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 2 • Serial 3 • Serial 4 (2 systems) • Automatic transfer finish • A/D conversion finish • Key interrupts (8 lines)			
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, pulse width measurement, generation of real time) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement generation of real time, serial baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 8-bit × 1 (square-wave/8-bit PWM output, event count, pulse width measurement, serial baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input frequency Interrupt source coincidence with compare register 4</p> <p>Timer counter 5 : 8-bit × 1 (square-wave output, event count, serial baud rate timer) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 5</p>			

Timer Counter (Continue)	Timer counter 4, 5 can be cascade-connected.
	Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6
	Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output event, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576, 1/4194304 of system clock frequency
	DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, 4; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 4, 5; 1/2, 1/4, 1/8, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, 3; 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 of OSC oscillation clock frequency
	Serial 3 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3, 5; 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 of OSC oscillation clock frequency
	Serial 4 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2, 5; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency

I/O Pins	I/O	34	• (5 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
		50	• (3 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
A/D Inputs	10-bit × 8-ch. (with S/H)		
D/A Outputs	8-bit × 1-ch.		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port		

See the next page for electrical characteristics, pin assignment and support tool.

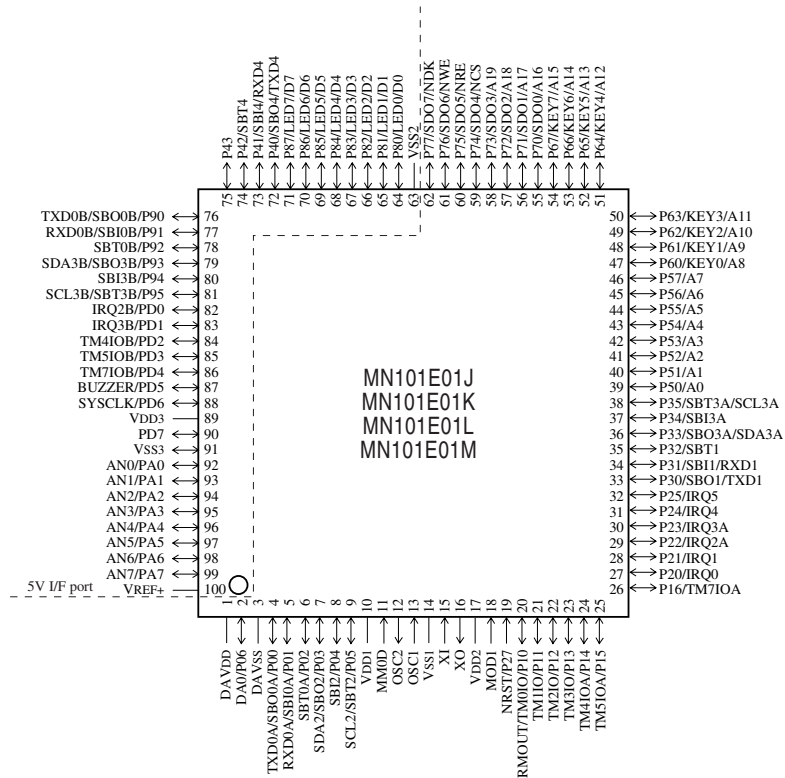
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		11(48)	30(80)	mA
	IDD2	fx = 32 kHz, VDD = 3 V		8(43)	22(75)	mA
	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		30(60)	120(180)	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C		12	30	μA
Supply current at STOP	IDD5	VDD = 3 V, Ta = 25°C		0.3	3.0	μA
	IDD6	VDD = 3 V, Ta = -40°C to +85°C			80	μA

() : Flash memory built-in type.

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free

MN101E01J, MN101E01K, MN101E01L, MN101E01M □

Support Tool

■ In-circuit Emulator	PX-ICE101E9+PX-PRB101E01-QFP100-P-1818B		
	PX-ICE101E9+PX-PRB101E01-QFP100-P-1414		
■ Flash Memory Built-in Type	Type	MN101EF01M	
	ROM (× 8-bit)	384 K	
	RAM (× 8-bit)	24 K	
	Minimum instruction execution time	Standard:	0.0625 μs (at 3.0 V to 3.6 V, 32 MHz)
		Double speed:	0.10 μs (at 3.0 V to 3.6 V, 10 MHz)
	Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free	

□ MN101C78A

Type	MN101C78A (under development)
ROM (×8-bit)	32 K
RAM (×8-bit)	1.5 K
Package	TQFP048-P-0707B ^{*Lead-free} (under development), QFP044-P-1010F ^{*Lead-free} (under planning)
Minimum Instruction Execution Time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz) 0.235 μs (at 1.8 V to 3.6 V, 4.25 MHz) 62.5 μs (at 1.8 V to 3.6 V, 32 kHz) <small>* The lower limit for operation guarantee for flash memory built-in type is 2.7 V.</small>
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 3, Serial 4 • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse (2-bit) system PWM output, real time output control) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, real time output control, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines), input capture register</p>

Timer Counter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines), input capture register
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM input capture, pluse width measurement is possible as a 32-bit timer.)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock
	Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock
	Serial 3 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock
	Serial 4 : I ² C slave × 1 Applicable for I ² C high-speed transfer mode, 7bit/10bit address setting, general call

I/O Pins	I/O	39 (35)	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) (): QFP044-P-1010F
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A/D Inputs	10-bit × 7-ch. (with S/H)
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LCD	12 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) (usable if VLCD ≤ VDD)
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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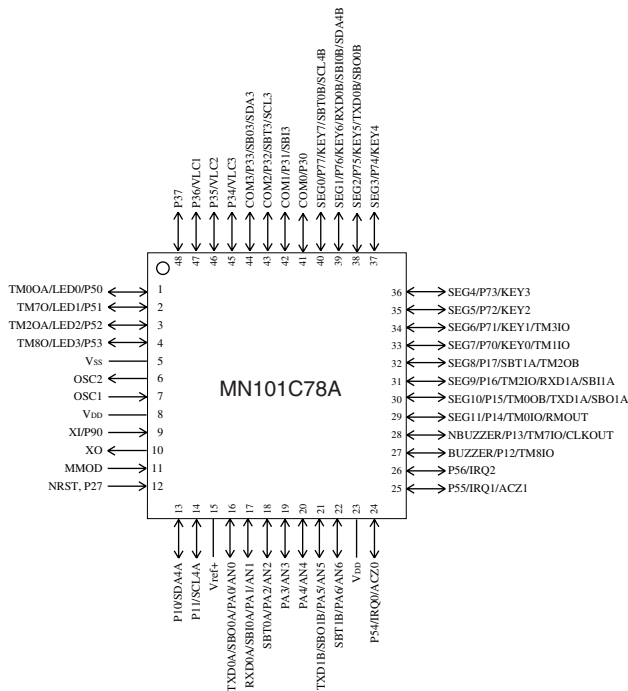
Electrical Characteristics

Supply current

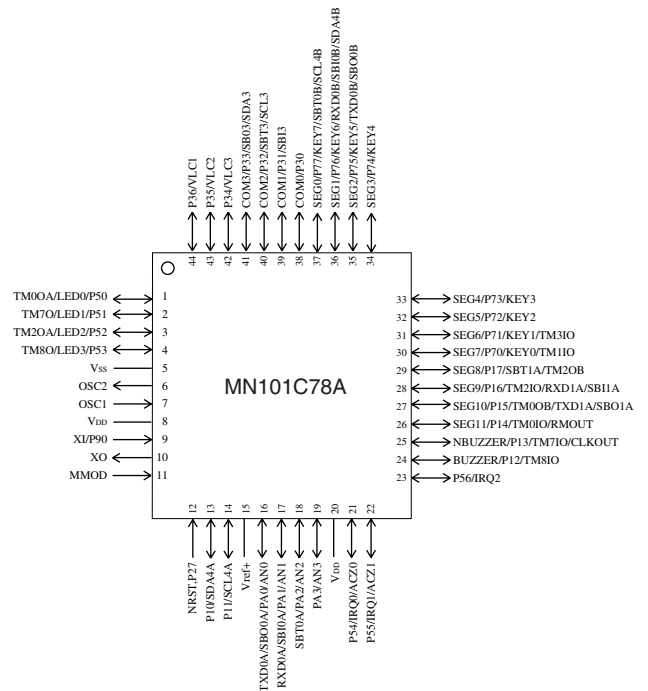
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, VDD = 3 V		4	15	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		2	5	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			10	μA
Supply current at STOP	IDD5	VDD = 3 V, Ta = 25°C			2	μA
	IDD6	VDD = 3 V, Ta = -40°C to +85°C			8	μA

See the next page for pin assignment and support tool.

Pin Assignment



TQFP048-P-0707B *Lead-free (under development)



QFP044-P-1010F *Lead-free (under planning)

Support Tool

In-circuit Emulator

PX-ICE101C / D + PX-PRB101C78-TQFP048-P-0707B-M (under development)
 PX-ICE101C / D + PX-PRB101C78-QFP044-P-1010F-M (under planning)

Flash Memory Built-in Type

Type	MN101CF78A (under development)
ROM (× 8-bit)	32 K
RAM (× 8-bit)	1.5 K
Minimum instruction execution time	0.2 μs (at 3.0 V to 3.6 V, 10 MHz) 0.235 μs (at 2.7 V to 3.6 V, 4 MHz) 62.5 μs (at 2.7 V to 3.6 V, 32 kHz)
Package	TQFP048-P-0707B *Lead-free (under development)

MN101C78A □

□ MN101C485 , MN101C487

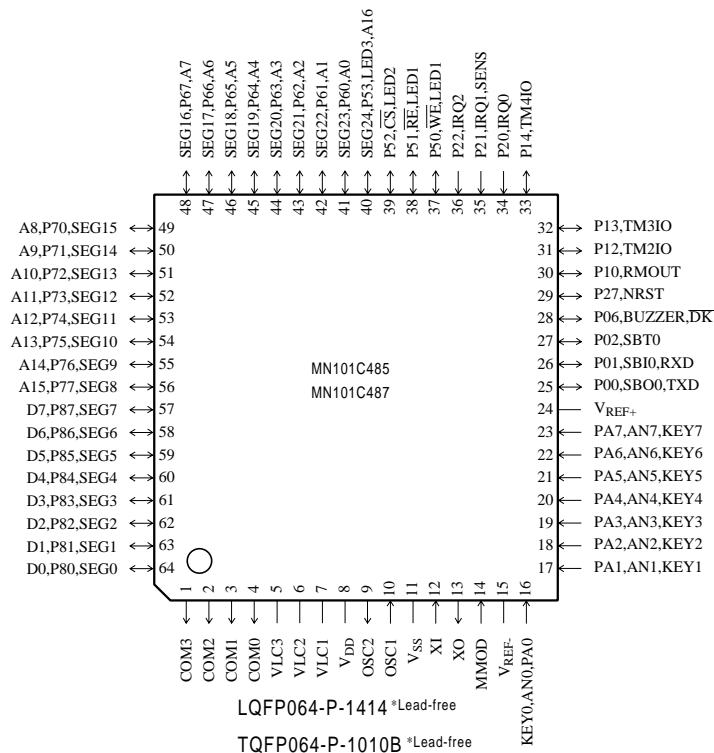
Type		MN101C485	MN101C487
ROM (x8-bit) External memory can be expanded		8 K	16 K
RAM (x8-bit) External memory can be expanded		0.5 K	0.5 K
Package LQFP064-P-1414 *Lead-free, TQFP064-P-1010B *Lead-free			
Minimum Instruction Execution Time		0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.0 V to 5.5 V, 32 kHz)*	
* The lower limit for operation guarantee for EPROM built-in type is 2.3 V.			
Interrupts		• RESET • Watchdog • External 0 • External 1 • External 2 • External 4 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • A/D conversion finish	
Timer Counter		<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>	
Serial Interface		Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency	
I/O Pins	I/O	36	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) • Specified pull-down resistor partially selectable
	Input	11	• Common use • Specified pull-up resistor available • Specified pull-down resistor partially selectable
A/D Inputs		10-bit × 8-ch. (with S/H)	
LCD		25 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty)	
Special Ports		Buzzer output, remote control carrier signal output, high-current drive port	

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD2	fx = 32 kHz, VDD = 3 V		15	100	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD5	VDD = 5 V, Ta = 25°C			1	μA
		VDD = 5 V, Ta = -40°C to +85°C			25	μA

Pin Assignment



Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C48-TQFP064-P-1010B	
	PX-ICE101C / D + PX-PRB101C48-LQFP064-P-1414	
EPROM Built-in Type	Type	MN101CP487
	ROM (× 8-bit)	16 K
	RAM (× 8-bit)	0.5 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.25 μs (at 2.7 V to 5.5 V, 8 MHz)
		125 μs (at 2.3 V to 5.5 V, 32 KHz)
Package	LQFP064-P-1414 *Lead-free, TQFP064-P-1010B *Lead-free	

□ MN101C527

Type	MN101C527
ROM (x8-bit)	16 K
RAM (x8-bit)	1.5 K
Package	LQFP064-P-1414 *Lead-free
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)*
* The lower limit for operation guarantee for EPROM built-in type is 2.3 V.	
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Timer 7 (2 systems) • Timer 8 • Time base • Serial 0 (2 systems) • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave/16-bit PWM output [cycle / duty continuous variable], event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>

Timer Counter (Continue)	<p>Timer counter 8: 16-bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source agreement with compare register 8</p> <p>Timer counters 7, 8 can be cascade-connected. (square-wave output, input capture, pulse width measurement is possible as a 32-bit timer.)</p> <p>Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p>
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Serial Interface	<p>Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; 1/2 pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p>
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I/O Pins	I/O		
	Input	42	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) • Specified pull-down resistor partially selectable
	Input	7	• Common use • Specified pull-up resistor available • Specified pull-down resistor partially selectable

A/D Inputs	10-bit × 4-ch. (with S/H)
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LCD	<p>24 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 5.5 V) LCD power step-up circuit contained (3/2, 2 and 3 times) LCD shunt resistance contained</p>
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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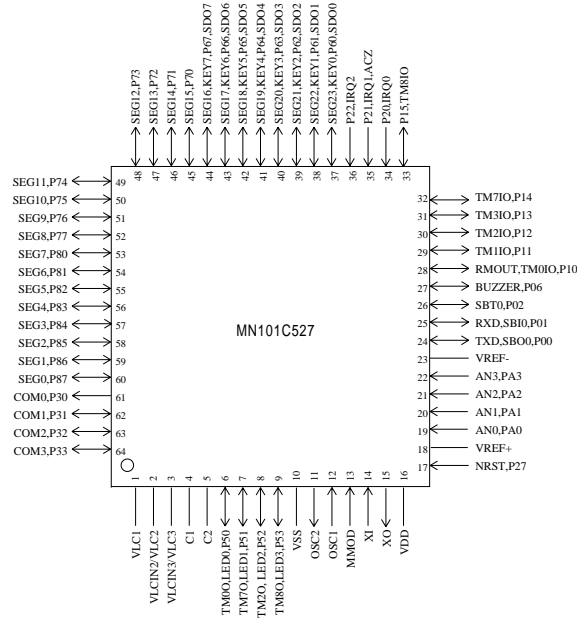
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C			8	μA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
		VDD = 5 V, Ta = -40°C to +85°C			35	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C52-LQFP064-P-1414-M	
EPROM Built-in Type	Type	MN101CP52A
	ROM (× 8-bit)	32 K
	RAM (× 8-bit)	1.5 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.3 V to 5.5 V, 32 KHz)
	Package	LQFP064-P-1414 *Lead-free

□ MN101C589 , MN101C58A

Type	MN101C589	MN101C58A
ROM (x8-bit)	24 K	32 K
RAM (x8-bit)	1.5 K	1.5 K
Package	LQFP064-P-1414 *Lead-free	

Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz)
	0.25 μs (at 2.7 V to 5.5 V, 8 MHz)* ¹
	62.5 μs (at 2.0 V to 5.5 V, 32 kHz)* ^{1,2}

*¹ The lower limit for operation guarantee for flash memory built-in type is 4.5 V.

*² The lower limit for operation guarantee for EPROM built-in type is 2.3 V.

Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • A/D conversion finish
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Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p>
	<p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p>
	<p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 2</p>
	<p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p>
	<p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p>
	<p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible)</p> <p>Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency</p> <p>Interrupt source coincidence with compare register 7 (2 lines)</p>
	<p>Timer counter 8 : 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible)</p>

Timer Counter (Continue)	Clock source	1/1, 1/2, 1/4, 1/16, 1/128 of system clock frequency; 1/1, 1/2, 1/4, 1/16, 1/128 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency
	Interrupt source	coincidence with compare register 8 (2 lines)
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.)	
	Time base timer (one-minute count setting) Clock source	
	Interrupt source	1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer Interrupt source	
		1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1
	Clock source
	1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency

I/O Pins	I/O	46	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	3	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 8-ch. (with S/H)
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LCD	24 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty)
	LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 5.5 V)
	LCD power step-up circuit contained (3/2, 2 and 3 times)
	LCD power shunt resistance contained

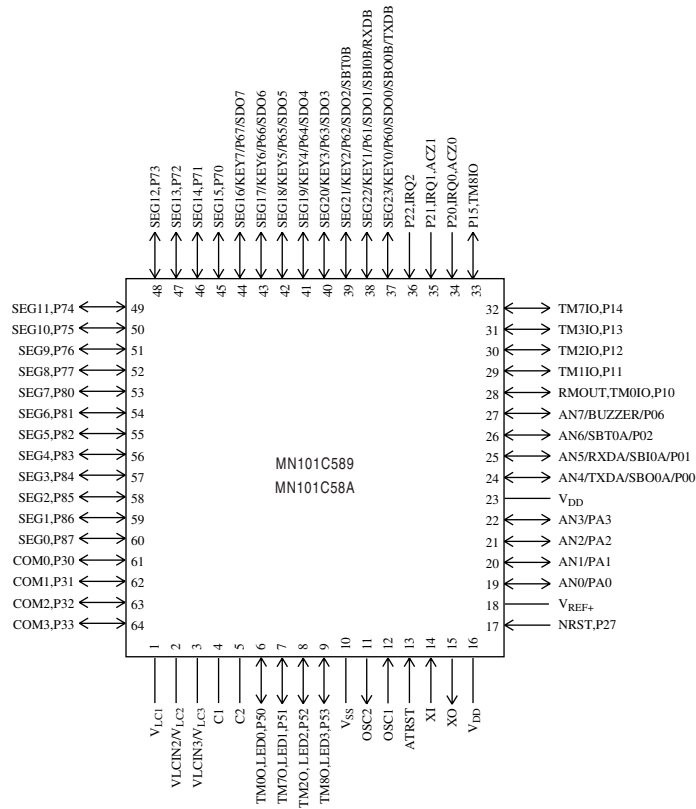
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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Electrical Characteristics

Supply current						
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
	IDD7	VDD = 5 V, Ta = -40°C to +85°C			50	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C58-LQFP064-P-1414-M	
EPROM Built-in Type	Type	MN101CP58A
	ROM (× 8-bit)	32 K
	RAM (× 8-bit)	1.5 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.3 V to 5.5 V, 32 kHz)
	Package	LQFP064-P-1414 *Lead-free
Flash Memory Built-in Type	Type	MN101CF58D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 4.5 V to 5.5 V, 8 MHz) 62.5 μs (at 4.5 V to 5.5 V, 32 kHz)
	Package	LQFP064-P-1414 *Lead-free

MN101C589 , MN101C58A □

□ MN101C39C

Type	MN101C39C		
ROM (×8-bit) External memory can be expanded	48 K		
RAM (×8-bit) External memory can be expanded	2 K		
Package (Conventional Package)	TQFP080-P-1212D *Lead-free (TQFP080-P-1212C)		
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.0 V to 5.5 V, 32 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V.		
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • A/D conversion finish		
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (ROM option)</p>		
Serial Interface	<p>Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency</p> <p>Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; 1/2 of timer counter 3 frequency</p>		
I/O Pins	I/O	49	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) • Specified pull-down resistor partially selectable
	Input	12	• Common use • Specified pull-up resistor available • Specified pull-down resistor partially selectable
A/D Inputs	10-bit × 8-ch. (with S/H)		
LCD	28 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty)		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port		

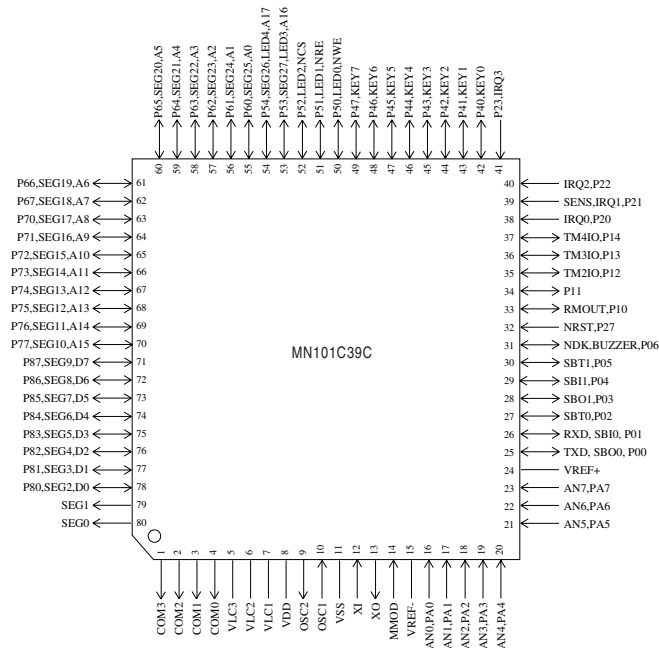
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 5 V		8	25	mA
	IDD2	fx = 32 kHz, VDD = 3 V		18	100	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		3	8	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			25	μA
Supply current at STOP	IDD5	VDD = 5 V, Ta = 25°C			1	μA
		VDD = 5 V, Ta = -40°C to +85°C			20	μA

Pin Assignment

() : Conventional Package



TQFP080-P-1212D *Lead-free
(TQFP080-P-1212C)

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C39-TQFP080-P-1212	
EPROM Built-in Type	Type	MN101CP39C
	ROM (× 8-bit)	48 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.3 V to 5.5 V, 32 kHz)*
	Package	TQFP080-P-1212D *Lead-free
	(Conventional Package)	(TQFP080-P-1212C)

□ MN101C54A, MN101C54C

Type	MN101C54A	MN101C54C
ROM (×8-bit)	32 K	48 K
RAM (×8-bit)	2 K	2 K
Package	QFP084-P-1818E *Lead-free, LQFP080-P-1414A *Lead-free	
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz)* ¹ 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)* ^{1,2}	
	* ¹ The lower limit for operation guarantee for flash memory built-in type is 4.5 V. * ² The lower limit for operation guarantee for EPROM built-in type is 2.3 V.	
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3*¹ • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish * ¹ LQFP080-P-1414A: Not mounted	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>	

Timer Counter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16, 1/128 of system clock frequency; 1/1, 1/2, 1/4, 1/16, 1/128 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines)
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency

I/O Pins	I/O	61 (60)	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) (): LQFP080-P-1414A
	Input	4 (3)	• Common use • Specified pull-up resistor available (): LQFP080-P-1414A

A/D Inputs	10-bit × 8-ch. (with S/H)
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LCD	32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 5.5 V) LCD power step-up circuit contained (3/2, 2 and 3 times) LCD power shunt resistance contained
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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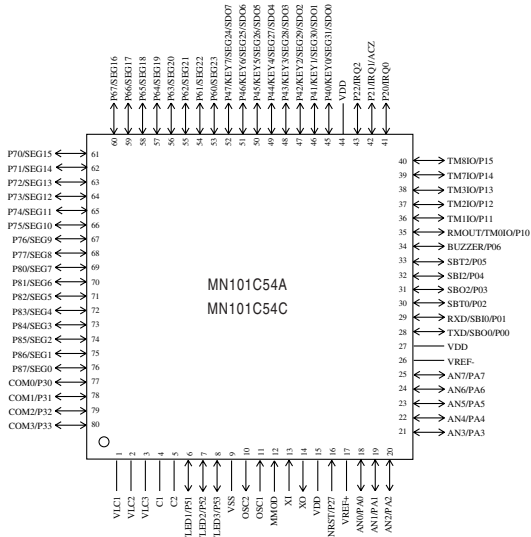
Electrical Characteristics

Supply current

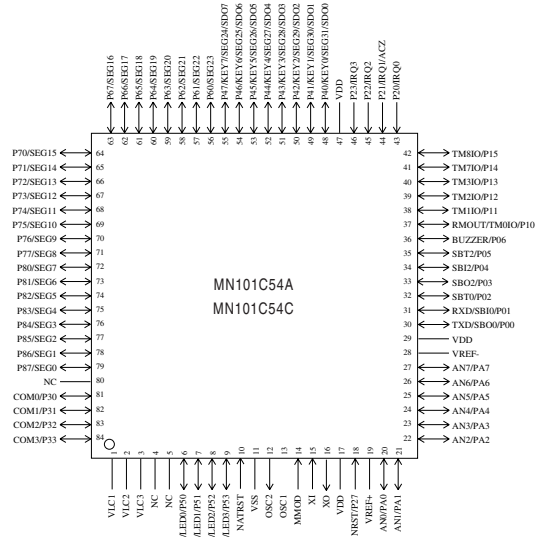
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	µA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	µA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	µA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	µA
	IDD7	VDD = 5 V, Ta = -40°C to +85°C			50	µA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP080-P-1414A *Lead-free



QFP084-P-1818E *Lead-free

Support Tool

In-circuit Emulator

PX-ICE101C / D + PX-PRB101C54-QFP084-P-1818E-M
 PX-ICE101C / D + PX-PRB101C54-LQFP080-P-1414A-M

EPROM Built-in Type

Type MN101CP54C

ROM (× 8-bit) 48 K

RAM (× 8-bit) 2 K

Minimum instruction execution time 0.1 μs (at 4.5 V to 5.5 V, 20 MHz)

0.25 μs (at 2.7 V to 5.5 V, 8 MHz)

62.5 μs (at 2.3 V to 5.5 V, 32 kHz)

Package LQFP080-P-1414A *Lead-free, QFP084-P-1818E *Lead-free

Flash Memory Built-in Type

Type MN101CF54D [ES (Engineering Sample) available]

ROM (× 8-bit) 64 K

RAM (× 8-bit) 2 K

Minimum instruction execution time 0.1 μs (at 4.5 V to 5.5 V, 20 MHz)

0.25 μs (at 4.5 V to 5.5 V, 8 MHz)

62.5 μs (at 4.5 V to 5.5 V, 32 kHz)

Package LQFP080-P-1414A *Lead-free, QFP084-P-1818E *Lead-free

MN101C54A, MN101C54C □

□ MN101C66D, MN101C66G

Type	MN101C66D	MN101C66G (under development)
ROM (×8-bit)	64 K	128 K
RAM (×8-bit)	2 K	4 K
Package	QFP084-P-1818E *Lead-free, LQFP080-P-1414A *Lead-free	
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)* ¹ * ¹ The lower limit for operation guarantee for flash memory built-in type is 2.5 V. The lower limit for operation guarantee for EPROM built-in type is 2.3 V.	
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3*¹ • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish * ¹ LQFP080-P-1414A: Not mounted	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>	

Timer Counter (Continue)	<p>Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, inputcapture) (square-wave/PWM output to large current terminal P53 possible)</p> <p>Clock source 1/1, 1/2, 1/4, 1/16, 1/128 of system clock frequency; 1/1, 1/2, 1/4, 1/16, 1/128 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency</p> <p>Interrupt source coincidence with compare register 8 (2 lines)</p> <p>Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.)</p> <p>Time base timer (one-minute count setting)</p> <p>Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency</p> <p>Watchdog timer</p> <p>Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p>
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Serial Interface	<p>Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency</p> <p>Serial 2 : synchronous type × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency</p>
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I/O Pins	I/O	61 (60)	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) () : LQFP080-P-1414A
	Input	4 (3)	• Common use • Specified pull-up resistor available () : LQFP080-P-1414A

A/D Inputs	10-bit × 8-ch. (with S/H)
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LCD	<p>32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VLCD ≤ VDD) LCD power shunt resistance contained</p>
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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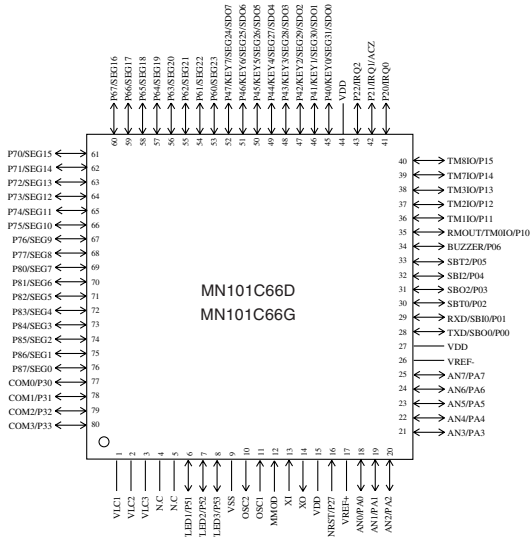
Electrical Characteristics

Supply current

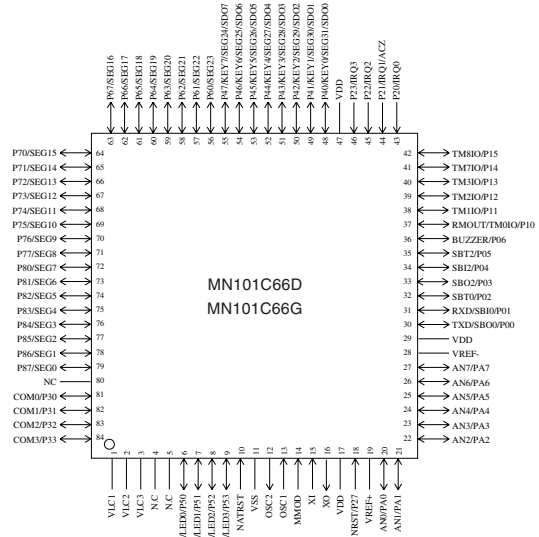
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
	IDD7	VDD = 5 V, Ta = -40°C to +85°C			50	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP080-P-1414A *Lead-free



QFP084-P-1818E *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C66-QFP084-P-1818E-M	
	PX-ICE101C / D + PX-PRB101C66-LQFP080-P-1414A-M	
EPROM Built-in Type	Type	MN101CP66D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.3 V to 5.5 V, 32 kHz)
	Package	LQFP080-P-1414A *Lead-free, QFP084-P-1818E *Lead-free
Flash Memory Built-in Type	Type	MN101CF66G [ES (Engineering Sample) available]
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.5 V to 5.5 V, 32 kHz)
	Package	LQFP080-P-1414A *Lead-free, QFP084-P-1818E *Lead-free

MN101C66D, MN101C66G □

□ MN101C70C , MN101C70G

Type	MN101C70C	MN101C70G (under planning)
ROM (x8-bit)	48 K	128 K
RAM (x8-bit)	2 K	10 K
Package	LQFP080-P-1414A *Lead-free, TQFP080-P-1212D *Lead-free (under planning)	

Minimum Instruction Execution Time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz)
	0.235 μs (at 1.8 V to 3.6 V, 4.25 MHz)
	62.5 μs (at 1.8 V to 3.6 V, 32 kHz)

* The lower limit for operation guarantee for flash memory built-in type is 2.2 V.

Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish • Automatic transfer finish
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Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse (2-bit) system PWM output, real time output control) (square-wave/PWM output to large current terminal P50 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p>
	<p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 1</p>
	<p>Timer counter 0, 1 can be cascade-connected.</p>
	<p>Timer counter 2 : 8-bit × 1 (square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, real time output control, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 2</p>
	<p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 3</p>
	<p>Timer counter 2, 3 can be cascade-connected.</p>
	<p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p>
	<p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output (Cycle/Duty can be changed constantly)) (square-wave/PWM output to large current terminal P51 possible)</p> <p>Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency</p> <p>Interrupt source coincidence with compare register 7 (2 lines), input capture register</p>

Timer Counter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines), input capture register
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency
	DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock

I/O Pins	I/O	66	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
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A/D Inputs	10-bit × 16-ch. (with S/H)
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LCD	32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty)
	LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 3.6 V)
	LCD power step-up circuit contained (3/2, 2 and 3 times)
	LCD power shunt resistance contained LCD reference voltage is contained.

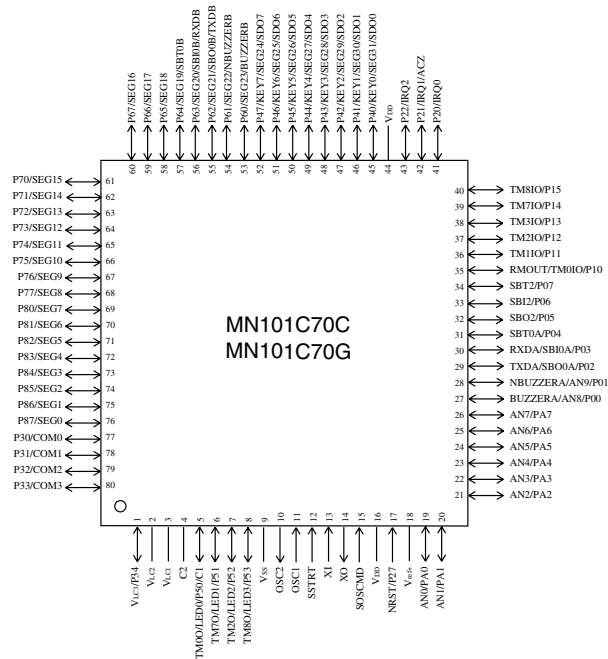
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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Electrical Characteristics

Supply current						
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, VDD = 3 V		4	15	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		2	5	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			10	μA
Supply current at STOP	IDD5	VDD = 3 V, Ta = 25°C			2	μA
	IDD6	VDD = 3 V, Ta = -40°C to +85°C			8	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP080-P-1414A *Lead-free

TQFP080-P-1212D *Lead-free

Support Tool

In-circuit Emulator

PX-ICE101C / D + PX-PRB101C70-LQFP080-P-1414A-M

PX-ICE101C / D + PX-PRB101C70-TQFP080-P-1212-M (under planning)

Flash Memory Built-in Type

Type	MN101CF70G (under development)
ROM (× 8-bit)	128 K
RAM (× 8-bit)	10 K
Minimum instruction execution time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz)
	0.235 μs (at 2.2 V to 3.6 V, 4.25 MHz)
	62.5 μs (at 2.2 V to 3.6 V, 32 kHz)
Package	LQFP080-P-1414A *Lead-free, TQFP080-P-1212D *Lead-free (under planning)

MN101C70C , MN101C70G □

□ MN101C38A , MN101C38C

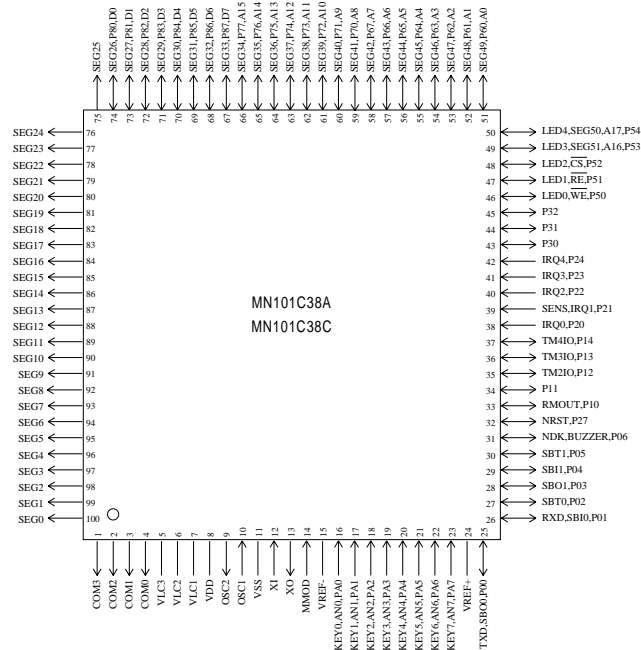
Type	MN101C38A		MN101C38C	
ROM (x8-bit) External memory can be expanded	32 K		48 K	
RAM (x8-bit) External memory can be expanded	1.5 K		2 K	
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free			
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.0 V to 5.5 V, 32 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V.			
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • A/D conversion finish			
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency (mask option)</p>			
Serial Interface	<p>Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency</p> <p>Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; 1/2 of timer counter 3 frequency</p>			
I/O Pins	I/O	44	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit) • Specified pull-down resistor partially selectable	
	Input	13	• Common use • Specified pull-up resistor available • Specified pull-down resistor partially selectable	
A/D Inputs	10-bit × 8-ch. (with S/H)			
LCD	52 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty)			
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port			

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD2	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C			8	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			24	μA
Supply current at STOP	IDD5	VDD = 5 V, Ta = 25°C			1	μA
		VDD = 5 V, Ta = -40°C to +85°C			20	μA

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free

Support Tool

In-circuit Emulator	Type	PX-ICE101C / D + PX-PRB101C38-QFP100-P-1818B
		PX-ICE101C / D + PX-PRB101C38-LQFP100-P-1414
EPROM Built-in Type	Type	MN101CP38C
	ROM (× 8-bit)	48 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.3 V to 5.5 V, 32 kHz)
	Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free

□ MN101C57C , MN101C57D

Type	MN101C57C	MN101C57D
ROM (x8-bit)	48 K	64 K
RAM (x8-bit)	2 K	2 K
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under planning)	

Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)*
* The lower limit for operation guarantee for flash memory built-in type is 2.5 V.	

Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 (key interrupt selectable) • External 5 (key interrupt dedicated) • External 6 • External 7 • Remote control • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish
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Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>
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Timer Counter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16, 1/128 of system clock frequency; 1/1, 1/2, 1/4, 1/16, 1/128 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines)
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.)
	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768 of clock source frequency
	Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; 1/2 of pulse output of timer counter 3 frequency ; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type × 1 Clock source 1/2, 1/4 of system clock frequency; 1/2 of pulse output of timer counter 3 frequency; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency

Remote Control Interface	Remote control output: timer 0 and 3 output: the remote control carrier output of 1/2 and 1/3 duty. Remote control reception: correspondence with low speed clock waiting Correspondence with AEHA (Association for Electric Home Appliances) format (selection of a format is available by the set-up)
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I/O Pins	I/O	77	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	6	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 16-ch. (with S/H)
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LCD	47 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VLCD ≤ VDD) LCD power shunt resistance contained
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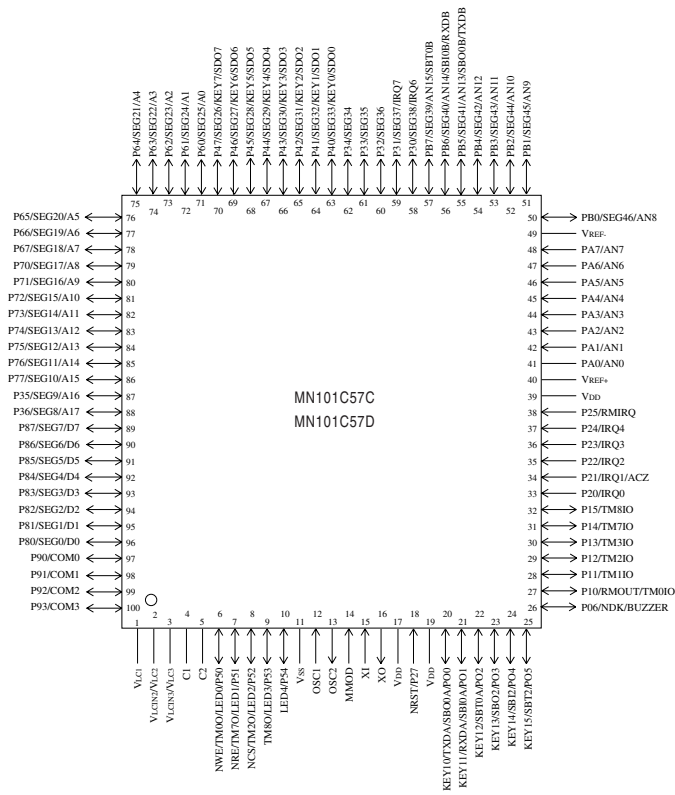
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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Electrical Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
	IDD7	VDD = 5 V, Ta = -40°C to +85°C			50	μA

See the next page for pin assignment and support tool.

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free (under planning)

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C57-QFP100-P-1818B-M	
Flash Memory Built-in Type	Type	MN101CF57D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.5 V to 5.5 V, 32 kHz)
	Package	QFP100-P-1818B *Lead-free LQFP100-P-1414 *Lead-free (under planning)

MN101C57C , MN101C57D □

□ MN101C73A , MN101C73D

Type	MN101C73A (under development)	MN101C73D (under planning)
ROM (×8-bit)	32 K	64 K
RAM (×8-bit)	1.5 K	2 K
Package	TQFP064-P-1010C *Lead-free, LQFP064-P-1414 *Lead-free (under planning)	
Minimum Instruction Execution Time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz) 0.235 μs (at 1.8 V to 3.6 V, 4.25 MHz) 62.5 μs (at 1.8 V to 3.6 V, 32 kHz)	
	* The lower limit for operation guarantee for flash memory built-in type is 2.2 V.	
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • External 6 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 3 • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse (2-bit) system PWM output) (square-wave/PWM output to large current terminal P50 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input; timer counter 8 output</p> <p>Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P51 possible)</p> <p>Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, serial transfer clock)</p> <p>Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer</p> <p>Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency</p> <p>Interrupt source coincidence with compare register 6</p>	

<p>Timer Counter (Continue)</p>	<p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output (Cycle/Duty can be changed constantly)) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines), input capture register</p> <p>Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines), input capture register</p> <p>Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.)</p> <p>Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/4096, 1/8192, 1/16384, 1/32768, of clock source frequency</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p>			
<p>Serial Interface</p>	<p>Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock</p> <p>Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock</p> <p>Serial 3 : synchronous type/single-master I²C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock</p>			
<p>I/O Pins</p>	<table border="1"> <tr> <td data-bbox="306 1400 491 1451">I/O</td> <td data-bbox="491 1400 545 1451">55</td> <td data-bbox="545 1400 1479 1451">• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)</td> </tr> </table>	I/O	55	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
I/O	55	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)		
<p>A/D Inputs</p>	<p>10-bit × 12-ch. (with S/H)</p>			
<p>LCD</p>	<p>32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) Usable if VLCD ≤ VDD LCD power shunt resistance contained</p>			
<p>Special Ports</p>	<p>Buzzer output, remote control carrier signal output, high-current drive port</p>			

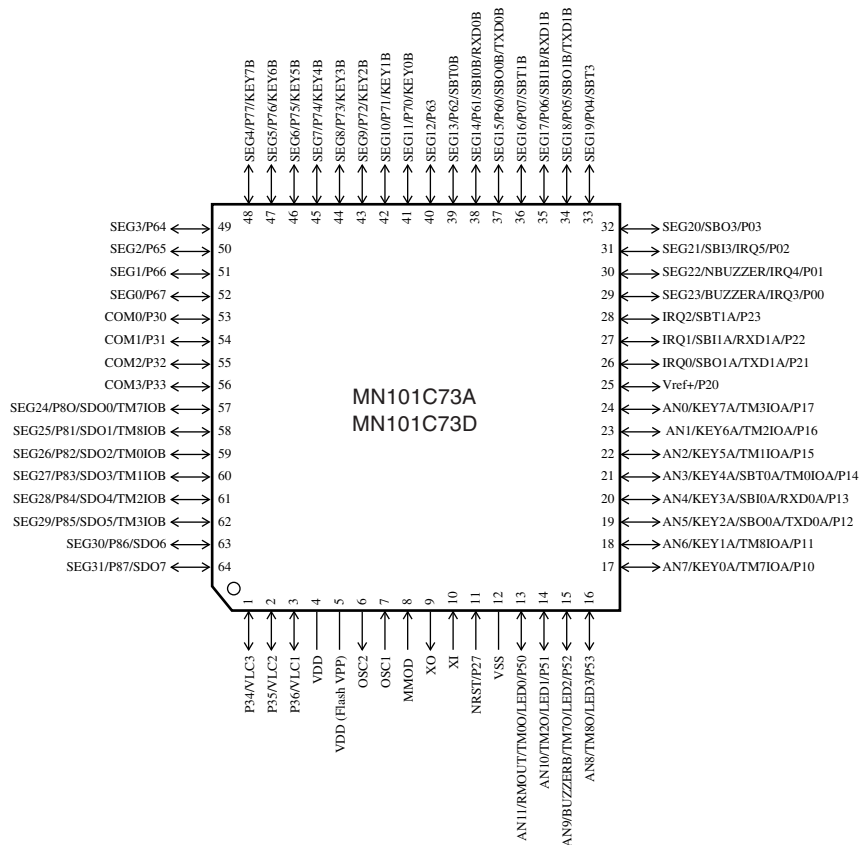
See the next page for pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, VDD = 3 V		4	15	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		2	5	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			10	μA
Supply current at STOP	IDD5	VDD = 3 V, Ta = 25°C			2	μA
	IDD6	VDD = 3 V, Ta = -40°C to +85°C			8	μA

Pin Assignment



TQFP064-P-1010C *Lead-free

LQFP064-P-1414 *Lead-free (under planning)

Support Tool

■ In-circuit Emulator	PX-ICE101C / D + PX-PRB101C73-TQFP064-P-1010C-M (under development)	
	PX-ICE101C / D + PX-PRB101C73-LQFP064-P-1414-M (under development)	
■ Flash Memory Built-in Type	Type	MN101CF73A (under development), MN101CF73D (under planning)
	ROM (× 8-bit)	32 K, 64K
	RAM (× 8-bit)	2.0 K
	Minimum instruction execution time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz)
		0.235 μs (at 2.2 V to 3.6 V, 4.25 MHz)
		62.5 μs (at 2.2 V to 3.6 V, 32 kHz)
Package	TQFP064-P-1010C *Lead-free, LQFP064-P-1414 *Lead-free (under planning)	

□ MN101C74D , MN101C74F, MN101C74G

Type	MN101C74D (under planning)	MN101C74F (under planning)	MN101C74G (under development)
ROM (×8-bit)	64 K	96 K	128 K
RAM (×8-bit)	1.5 K	6 K	6 K
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under planning), MLGA100-L-1010 *Lead-free (under planning)		
Minimum Instruction Execution Time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz) 0.235 μs (at 1.8 V to 3.6 V, 4.25 MHz) 62.5 μs (at 1.8 V to 3.6 V, 32 kHz) * The lower limit for operation guarantee for flash memory built-in type is 2.2 V.		
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • External 6 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 3 • A/D conversion finish • Automatic transfer finish 		
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse (2-bit) system PWM output) (square-wave/PWM output to large current terminal PC3 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input; timer counter 8 output Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal PC5 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output (Cycle/Duty can be changed constantly)) (square-wave/PWM output to large current terminal PC4 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines), input capture register</p>		

Timer Counter (Continue)	<p>Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal PC6 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines), input capture register</p> <p>Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.)</p> <p>Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/4096, 1/8192, 1/16384, 1/32768, of clock source frequency</p> <p>Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency</p> <p>Max. Transfer cycles 255</p> <p>Starting factor external request, various types of interrupt, software</p> <p>Transfer mode 1-byte transfer, word transfer, burst transfer</p> <p>DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer</p>			
Serial Interface	<p>Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock</p> <p>Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock</p> <p>Serial 3 : synchronous type/single-master I²C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock</p> <p>Serial 4 : I²C slave × 1 Applicable for I²C high-speed transfer mode, 7-bit/10-bit address setting, general call</p>			
I/O Pins	<table border="1"> <tr> <td data-bbox="308 1529 491 1574">I/O</td> <td data-bbox="491 1529 547 1574">87</td> <td data-bbox="547 1529 1481 1574"> <ul style="list-style-type: none"> • Common use • Specified pull-up resistor available • Input/output selectable (bit unit) </td> </tr> </table>	I/O	87	<ul style="list-style-type: none"> • Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
I/O	87	<ul style="list-style-type: none"> • Common use • Specified pull-up resistor available • Input/output selectable (bit unit) 		
A/D Inputs	10-bit × 16-ch. (with S/H)			
LCD	<p>47 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 3.6 V) LCD power step-up circuit contained (3/2, 2 and 3 times) LCD power shunt resistance contained LCD reference voltage is contained.</p>			
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port			

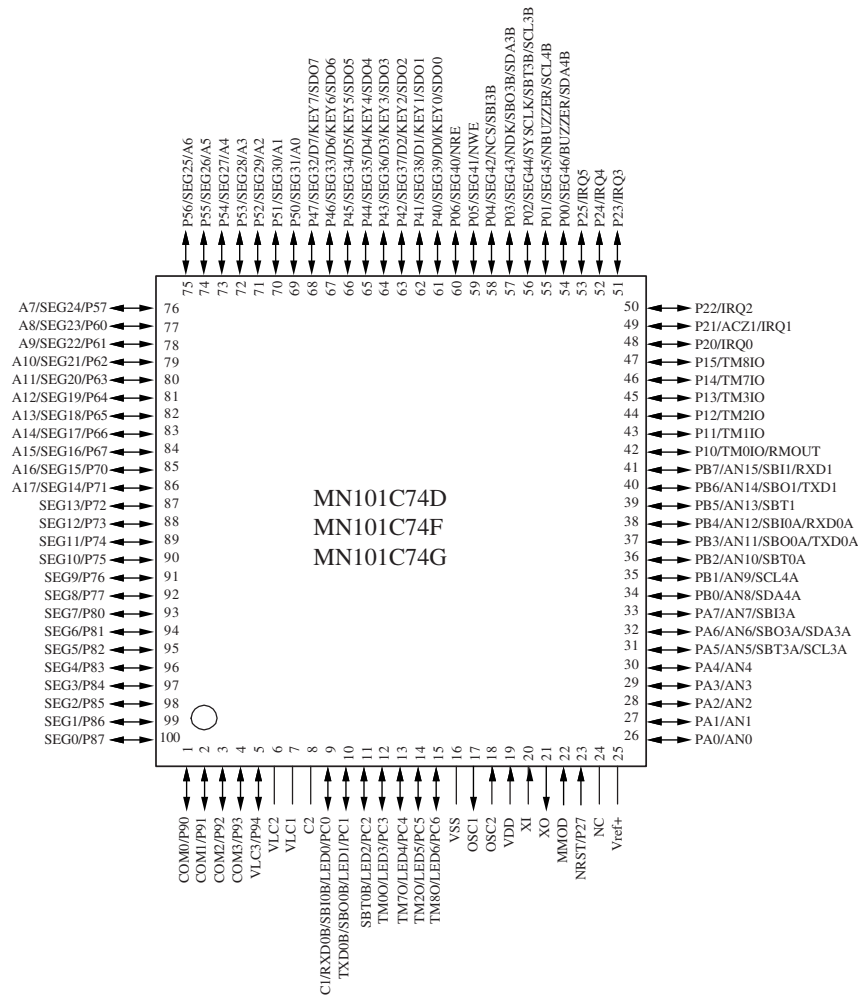
See the next page for pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, VDD = 3 V		4	15	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		2	5	μA
	IDD4	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			10	μA
Supply current at STOP	IDD5	VDD = 3 V, Ta = 25°C			2	μA
	IDD6	VDD = 3 V, Ta = -40°C to +85°C			8	μA

Pin Assignment



QFP100-P-1818B *Lead-free

LQFP100-P-1414 *Lead-free

MLGA100-L-1010 *Lead-free

Support Tool

■ In-circuit Emulator	PX-ICE101C / D + PX-PRB101C74-QFP100-P-1818B-M (under development)	
	PX-ICE101C / D + PX-PRB101C74-LQFP100-P-1414-M (under planning)	
■ Flash Memory Built-in Type	Type	MN101CF74G (under development)
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	6 K
	Minimum instruction execution time	0.1 μs (at 3.0 V to 3.6 V, 10 MHz)
		0.235 μs (at 2.2 V to 3.6 V, 4.25 MHz)
		62.5 μs (at 2.2 V to 3.6 V, 32 kHz)
	Package	QFP100-P-1818B ^{*Lead-free} , LQFP100-P-1414 ^{*Lead-free} (under planning)
MLGA100-L-1010 ^{*Lead-free} (under planning)		

□ MN101C84A , MN101C84D

Type	MN101C84A (under development)	MN101C84D (under planning)
ROM (×8-bit)	32 K	64 K
RAM (×8-bit)	1K	2 K
Package	LQFP064-P-1414 *Lead-free	
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz)	
	0.25 μs (at 2.7 V to 5.5 V, 8 MHz)	
	62.5 μs (at 2.0 V to 5.5 V, 32 kHz) *	
* The lower limit for operation guarantee for flash memory built-in type is 2.5 V.		
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/8192, 1/32768 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/4096, 1/8192 of OSC oscillation clock frequency; 1/1, 1/4096, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, IGBT/16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p> <p>Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible)</p>	

Timer Counter (Continue)	Clock source	1/1, 1/2, 1/4, 1/16, 1/128 of system clock frequency; 1/1, 1/2, 1/4, 1/16, 1/128 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency
	Interrupt source	coincidence with compare register 8 (2 lines)
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.)	
	Time base timer (one-minute count setting) Clock source	
	Interrupt source	1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer Interrupt source	
		1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1
	Clock source
	1/2, 1/4 of system clock frequency; pulse output of timer counter 3; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency

I/O Pins	I/O	49	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	3	• Common use • Specified pull-up resistor available

A/D Inputs	10-bit × 8-ch. (with S/H)
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LCD	32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VLCD ≤ VDD ≤ 5.5 V) LCD power shunt resistance contained
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Special Ports	Buzzer output, remote control carrier signal output, high-current drive port
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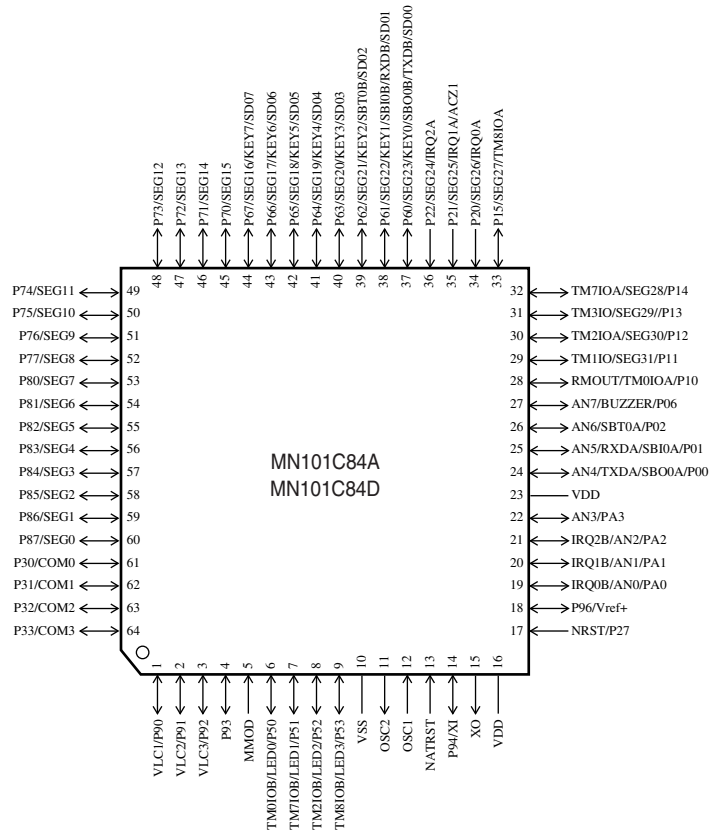
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V		25	60	mA
	IDD2	fosc = 8 MHz, VDD = 5 V		10	25	mA
	IDD3	fx = 32 kHz, VDD = 3 V		30	100	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3 V, Ta = 25°C		4	8	μA
	IDD5	fx = 32 kHz, VDD = 3 V, Ta = -40°C to +85°C			30	μA
Supply current at STOP	IDD6	VDD = 5 V, Ta = 25°C			2	μA
	IDD7	VDD = 5 V, Ta = -40°C to +85°C			50	μA

See the next page for pin assignment and support tool.

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C84-LQFP064-P-1414-M	
Flash Memory Built-in Type	Type	MN101CF84D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 62.5 μs (at 2.5 V to 5.5 V, 32 kHz)
	Package	LQFP064-P-1414 *Lead-free

MN101C84A, MN101C84D □

□ MN101C07A

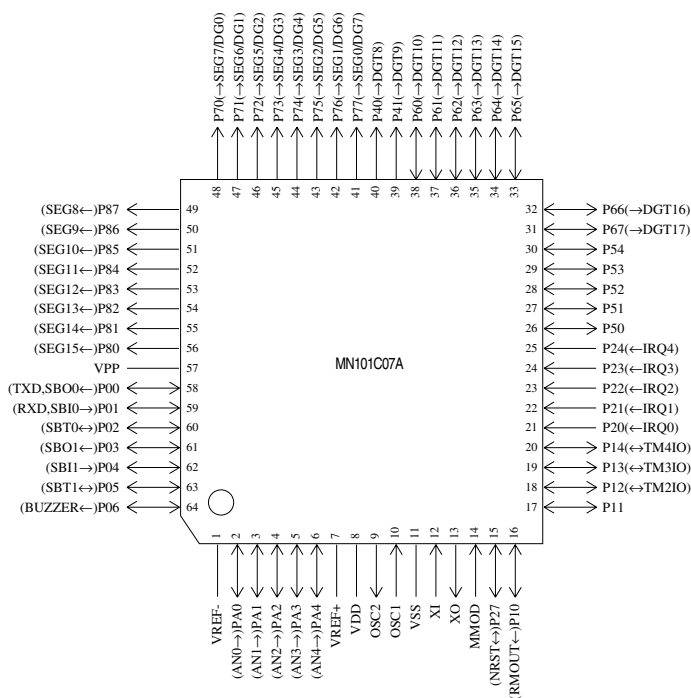
Type	MN101C07A		
ROM (x8-bit)	32 K		
RAM (x8-bit)	1 K		
Package	LQFP064-P-1414 *Lead-free		
Minimum Instruction Execution Time	0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.7 V to 5.5 V, 32 kHz)		
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • Automatic transfer finish • A/D conversion finish • Key scan 		
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/2097152 of system clock frequency</p>		
Serial Interface	<p>Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency</p> <p>Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; 1/2 of timer counter 3 frequency</p>		
I/O Pins	I/O	27	• Common use : 21 • Specified pull-up resistor available • Input/output selectable (bit unit)
	High Voltage	26	• Output: 18 • I/O: 8 • P-ch open drain (breakdown voltage -30 V): FL drive: 26 • Specified pull-down resistor mask option: 8
A/D Inputs	8-bit × 5-ch. (with S/H)		
FL	(8 to 16) segments × (18 to 10) digits		
Special Ports	Buzzer output, remote control carrier signal output		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 5 V			25	mA
	IDD2	fx = 32 kHz, VDD = 3 V			120	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V			10	μA
Supply current at STOP	IDD4	VDD = 3 V			10	μA

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C07-LQFP064-P-1414	
EPROM Built-in Type	Type	MN101CP07D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.7 V to 5.5 V, 32 kHz)
	Package	LQFP064-P-1414 *Lead-free

□ MN101C35D

Type	MN101C35D
ROM (x8-bit)	64 K
RAM (x8-bit)	2 K
Package	QFP100-P-1818B *Lead-free
Minimum Instruction Execution Time	0.25 μs (at 2.7 V to 5.5 V, 8 MHz) 125 μs (at 2.2 V to 5.5 V, 32 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.7 V.
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Time base • Serial 0 • Serial 1 • Serial 2 • Automatic transfer finish • A/D conversion finish • Key scan
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier) Clock source 1/1, 1/4 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/16, 1/64 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave/8-bit PWM output, event count, synchronous output event) Clock source 1/1, 1/4 of system clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 16-bit × 1 (square-wave/16-bit PWM output, event count, synchronous output event, input capture) Clock source 1/4, 1/16 of system clock frequency; 1/1 of OSC oscillation clock frequency; external clock input Interrupt source coincidence with compare register 4</p> <p>Time base timer (one-minute count setting, independently operable 8-bit timer counter 5) Clock source 1/4 of system clock frequency; 1/1, 1/8192 of OSC oscillation clock frequency; 1/1, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 5; 1/8192 prescaler overflow</p> <p>Watchdog timer Interrupt source 1/2097152 of system clock frequency</p>
Serial Interface	<p>Serial 0 : synchronous type/simple UART (half-duplex) × 1 Clock source 1/2, 1/4, 1/16 of system clock frequency; 1/2 of timer counter 3 frequency</p> <p>Serial 1 : synchronous type × 1 Clock source 1/2, 1/8, 1/64 of system clock frequency; 1/2 of timer counter 3 frequency</p> <p>Serial 2 : synchronous type/simple I²C × 1 Clock source 1/1, 1/2, 1/4 of system clock frequency; 1/2 of timer counter 0 frequency</p>

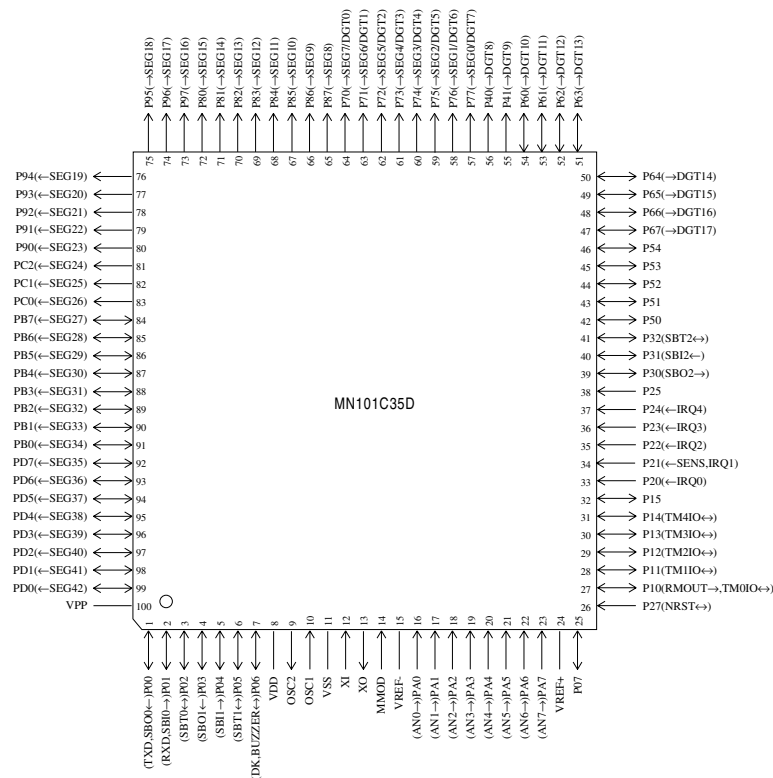
I/O Pins	I/O	36	• Common use : 28 • Specified pull-up resistor available • Input/output selectable (bit unit)
	High Voltage	53	• Output: 29 • I/O: 24 • P-ch open drain (breakdown voltage –30V): FL drive: 53 • Specified pull-down resistor mask option: 35
A/D Inputs	8-bit × 8-ch. (with S/H)		
FL	(35 to 43) segments × (18 to 10) digits		
Special Ports	Buzzer output, remote control carrier signal output		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 5 V			25	mA
	IDD2	fx = 32 kHz, VDD = 3 V			120	μA
Supply current at HALT	IDD3	fx = 32 kHz, VDD = 3 V			10	μA
Supply current at STOP	IDD4	VDD = 3 V			10	μA

Pin Assignment



QFP100-P-1818B *Lead-free

See the next page for support tool.

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C35-QFP100-P-1818B	
EPROM Built-in Type	Type	MN101CP35D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.25 μs (at 2.7 V to 5.5 V, 8 MHz)
		125 μs (at 2.7 V to 5.5 V, 32 kHz)
	Package	QFP100-P-1818B *Lead-free

MN101C35D □

□ MN101C87A , MN101C87D

Type	MN101C87A (under development)	MN101C87D (under planning)
ROM (×8-bit)	32 K	64 K
RAM (×8-bit)	1.25 K	2 K
Package	LQFP064-P-1414 *Lead-free	
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.24 μs (at 2.7 V to 5.5 V, 8.4 MHz) 0.48 μs (at 2.3 V to 5.5 V, 4.19 MHz) * 0.24 μs (at 2.0 V to 5.5 V, 2.0 MHz)* 62.5 μs (at 2.0 V to 5.5 V, 32 kHz) * * The lower limit for operation guarantee for EPROM built-in type is 2.5 V	
Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish • Automatic transfer finish • Key scan	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, PWM output, serial transfer clock, event count, simple pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>	

Timer Counter (Continue)	Time base timer (one-minute count setting)
	Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency
	Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency
	Watchdog timer
	Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency
	DMA controller (automatic data transfer)
	Max. Transfer cycles 255
	Starting factor external request, various types of interrupt, software
	Transfer mode 1-byte transfer, word transfer, burst transfer

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1
	Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock
	Serial 2 : synchronous type/single-master I ² C × 1
	Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock

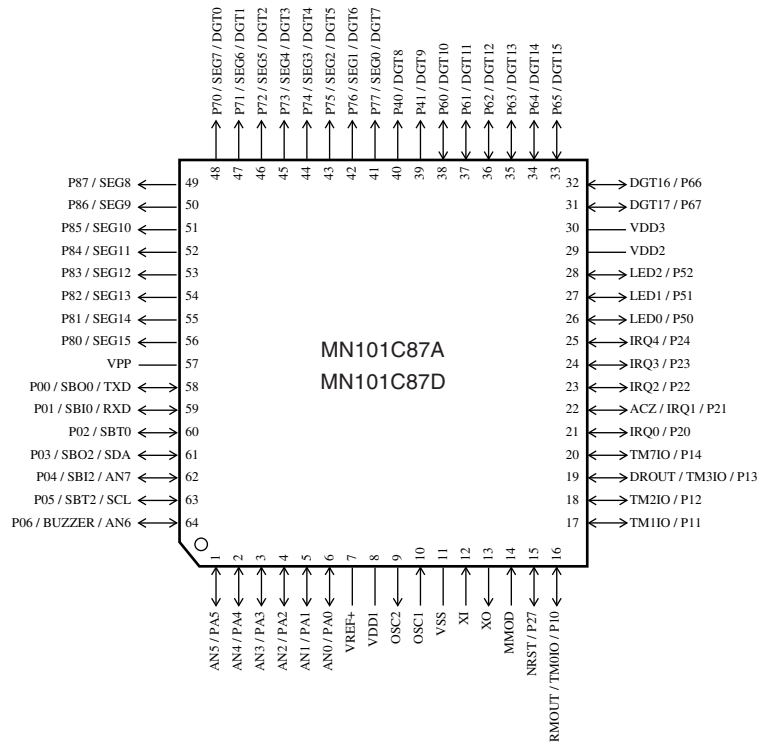
I/O Pins	I/O	26	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	High voltage	7	• Output: 18 • I/O: 8 • P-ch. open drain (breakdown voltage –30 V) : FL drive: 26 • Specified pull-down resistor mask option: 16

A/D Inputs	10-bit × 8-ch. (with S/H)
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FL	(8 to 16) segments × (18 to 10) digits
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Special Ports	Buzzer output, high-current drive port
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Pin Assignment



LQFP064-P-1414 *Lead-free

See the next page for pin assignment and support tool.

Support Tool

■ In-circuit Emulator	PX-ICE101C / D + PX-PRB101C87-LQFP064-P-1414-M (under development)	
■ Flash Memory Built-in Type	Type	MN101CF87G (under development)
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.24 μs (at 2.7 V to 5.5 V, 8.4 MHz)
		0.48 μs (at 2.5 V to 5.5 V, 4.19 MHz)
62.5 μs (at 2.5 V to 5.5 V, 32 kHz)		
Package	LQFP064-P-1414 *Lead-free	

MN101C87A , MN101C87D □

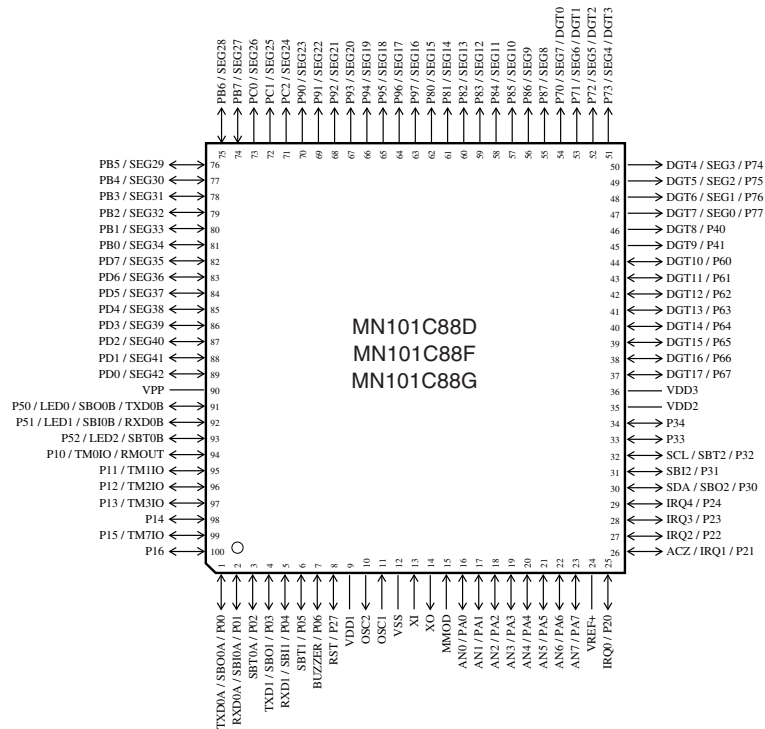
□ MN101C88D , MN101C88F , MN101C88G

■ Type	MN101C88D (under planning)	MN101C88F (under planning)	MN101C88G (under development)
■ ROM (×8-bit)	64 K	96 K	128 K
■ RAM (×8-bit)	2 K	4 K	4 K
■ Package	QFP100-P-1818B *Lead-free		
■ Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.24 μs (at 2.7 V to 5.5 V, 8.4 MHz) 0.48 μs (at 2.3 V to 5.5 V, 4.19 MHz) * 0.24 μs (at 2.0 V to 5.5 V, 2.0 MHz)* 62.5 μs (at 2.0 V to 5.5 V, 32 kHz) *		
* The lower limit for operation guarantee for EPROM built-in type is 2.5 V			
■ Interrupts	• RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 2 • A/D conversion finish • Automatic transfer finish • Key scan		
■ Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, PWM output, serial transfer clock, event count, simple pulse width measurement) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output, event count, generation of remote control carrier, serial transfer clock) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 3</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency Interrupt source coincidence with compare register 6</p> <p>Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, pulse width measurement, input capture) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 7 (2 lines)</p>		

Timer Counter (Continue)	Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency DMA controller (automatic data transfer) Max. Transfer cycles 255 Starting factor external request, various types of interrupt, software Transfer mode 1-byte transfer, word transfer, burst transfer	
Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock Serial 1 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency, external clock Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency, external clock	
I/O Pins	I/O	35 • Common use • Specified pull-up resistor available • Input/output selectable (bit unit) <hr/> High voltage 53 • Output: 29 • I/O: 24 • P-ch. open drain (breakdown voltage –30 V) : FL drive: 53 • Specified pull-down resistor mask option: 35
A/D Inputs	10-bit × 8-ch. (with S/H)	
FL	(8 to 16) segments × (18 to 10) digits	
Special Ports	Buzzer output, high-current drive port	

See the next page for pin assignment and support tool.

Pin Assignment



QFP100-P-1818B *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C88-LQFP100-P-1818B-M (under development)	
Flash Memory Built-in Type	Type	MN101CF88G (under development)
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.24 μs (at 2.7 V to 5.5 V, 8.4 MHz) 0.48 μs (at 2.5 V to 5.5 V, 4.19 MHz) 62.5 μs (at 2.5 V to 5.5 V, 32 kHz)
	Package	QFP100-P-1818B *Lead-free

MN101C88D, MN101C88F, MN101C88G □

□ MN101C75D

Type	MN101C75D(under development)
ROM (x8-bit)	64 K
RAM (x8-bit)	2 K
Package	LQFP080-P-1414A *Lead-free
Minimum Instruction Execution Time	0.125 μs (at 3.0 V to 3.6 V, 8 MHz, non-use of USB) 0.167 μs (at 3.0 V to 3.6 V, 6 MHz, use of USB) 62.5 μs (at 3.0 V to 3.6 V, 32 kHz, non-use of USB)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 4 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 2 • A/D conversion finish • Automatic transfer finish • USB interrupts
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement) (square-wave/PWM output to large current terminal P50 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 0</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 1</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output, additional pulse type 10-bit PWM output, event count, synchronous output event, simple pulse width measurement) (square-wave/PWM output to large current terminal P52 possible) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input Interrupt source coincidence with compare register 2</p> <p>Timer counter 3 : 8-bit × 1</p>

Timer Counter (Continue)

(square-wave output, event count, generation of remote control carrier, serial 0 baud rate timer)

Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input

Interrupt source coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.

Timer counter 6 : 8-bit freerun timer

Clock source 1/1 of system clock frequency; 1/1, 1/128, 1/8192 of OSC oscillation clock frequency; 1/1, 1/128, 1/8192 of XI oscillation clock frequency

Interrupt source coincidence with compare register 6

Timer counter 7 : 16-bit × 1

(square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P51 possible)

Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency

Interrupt source coincidence with compare register 7 (2 lines)

USB Functions

Conforms to USB1.1.

USB transceiver built-in

Full-speed (12 Mbps) supported.

5 end points (FIFO built-in independently)

FIFO size

(EP0, 1, 2, 3, 4): 16, 128, 128, 128, 128 bytes

- EP0

Control transfer

IN/OUT (two ways)

- EP1 to EP4

Interrupt/Bulk/Isochronous transfer supported.

Settable to IN or OUT.

Double Buffering function supported.

When the MAXP size is set to a half or less of the MAXFIFO size for each EP, the Double Buffering function is made valid automatically.

Timer Counter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal P53 possible) Clock source 1/1, 1/2, 1/4, 1/16 of system clock frequency; 1/1, 1/2, 1/4, 1/16 of OSC oscillation clock frequency; 1/1, 1/2, 1/4, 1/16 of external clock input frequency Interrupt source coincidence with compare register 8 (2 lines)
	Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM, input capture, pulse width measurement is possible as a 32-bit timer.) Time base timer (one-minute count setting) Clock source 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency Interrupt source 1/128, 1/256, 1/512, 1/1024, 1/8192, 1/32768, of clock source frequency Watchdog timer Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

Serial Interface	Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 1 or 2; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency
	Serial 2 : synchronous type/single-master I ² C × 1 Clock source 1/2, 1/4 of system clock frequency; pulse output of timer counter 2 or 3; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency

I/O Pins	I/O	62	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
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A/D Inputs	10-bit × 12-ch. (with S/H)
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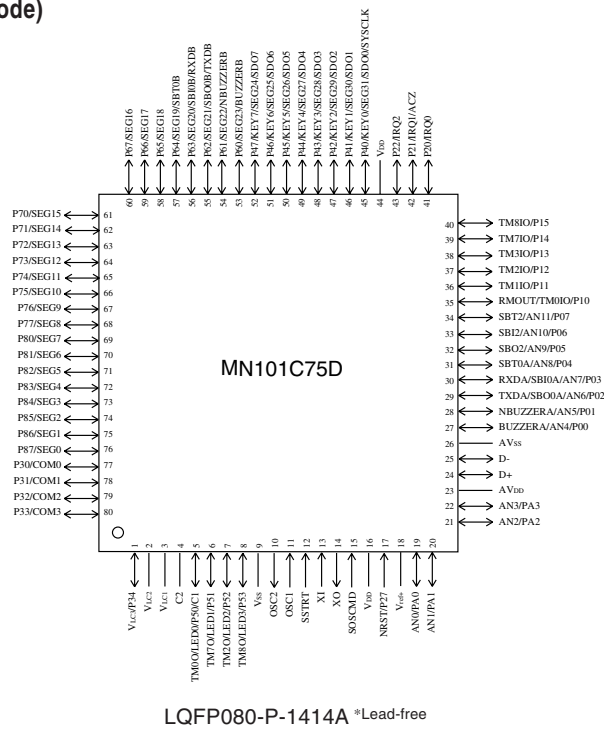
LCD	32 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 3.6 V) LCD power step-up circuit contained (3/2, 2 and 3 times) LCD power shunt resistance contained
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Special Ports	USB ports (D+, D-), buzzer output, remote control carrier signal output, high-current drive port
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Electrical Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz, VDD = 3.3 V (non-use of USB)			T.B.D.	mA
	IDD2	fosc = 6 MHz, VDD = 3.3 V (use of USB)			T.B.D.	mA
	IDD3	fx = 32 kHz, VDD = 3.3 V			T.B.D.	μA
Supply current at HALT	IDD4	fx = 32 kHz, VDD = 3.3 V, Ta = 25°C			T.B.D.	μA
	IDD5	fx = 32 kHz, VDD = 3.3 V, Ta = -40°C to +85°C			T.B.D.	μA
Supply current at STOP	IDD6	VDD = 3.3 V, Ta = 25°C			T.B.D.	μA
	IDD7	VDD = 3.3 V, Ta = -40°C to +85°C			T.B.D.	mA

Pin Assignment (at single chip mode)



LQFP080-P-1414A *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101C75-LQFP080-P-1414A-M (under planning)	
Flash Memory Built-in Type	Type	MN101CF75D (under planning)
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.125 μs (at 3.0 V to 3.6 V, 8 MHz) 0.167 μs (at 3.0 V to 3.6 V, 6 MHz) 62.5 μs (at 3.0 V to 3.6 V, 32 kHz)
	Package	LQFP080-P-1414A *Lead-free

□ MN101C29D

Type	MN101C29D
ROM (x8-bit)	64 K
RAM (x8-bit)	1.5 K
Package	LQFP080-P-1414A *Lead-free
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 8 (2 systems) • Serial 2 • Key interrupts (8 lines)
Timer Counter	<p>Timer counter 2 : 8-bit × 1 (square-wave output[timer pulse output], PWM output, event count, timer synchronous output, simple pulse width measurement function) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output[timer pulse output], event count, remote control carrier output) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Time base timer Clock source 1/1, 1/2⁷, 1/2⁸, 1/2⁹, 1/2¹⁰, 1/2¹³, 1/2¹⁵ of OSC oscillation clock frequency; 1/1, 1/2⁷, 1/2⁸, 1/2⁹, 1/2¹⁰, 1/2¹³, 1/2¹⁵ of XI oscillation clock frequency</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/2⁷, 1/2¹³ of OSC oscillation clock frequency; 1/1, 1/2⁷, 1/2¹³ of XI oscillation clock frequency</p> <p>Timer counter 8 : 16-bit × 1 Clock source either of system clock, OSC oscillation clock, external clock 1 or external clock 2 divided into 1/1, 1/2, 1/4 and 1/16 (hardware configuration) double buffer type compare register × 2 input capture register × 1 (timer functions) square-wave output (timer pulse output), PWM output (duty continuously variable), event count, simple pulse width measurement function and input capture function</p> <p>Watchdog timer Interrupt source runaway detection frequency selection from 1/2¹⁶, 1/2¹⁸ and 1/2²⁰ of system clock</p>
Serial Interface	<p>Serial 2 : synchronous type × 1 Synchronous type (MSB or LSB first selectable, 1 to 8 bits arbitrary transmission) Transfer clock source 1/2, 1/4 of system clock frequency; 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency; timer counter 2, 3 output; 1/3 of frequency of the above clocks</p>
Multiplication / Division functions	<p>Signed/unsigned: 16-bit × 16-bit arithmetic operation (execution in 15 cycles) Unsigned: 32-bit ÷ 16-bit arithmetic operation (execution in 17 cycles)</p>

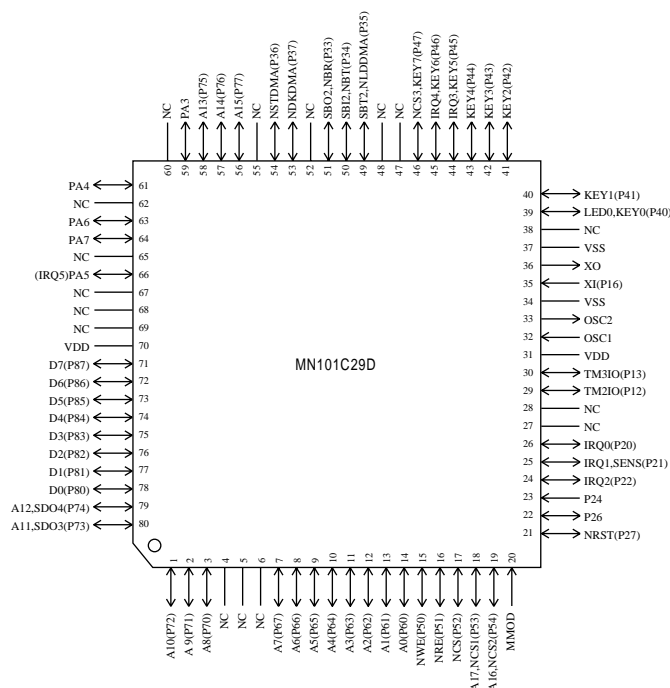
I/O Pins	I/O	53	• Common use: 48 • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	2	• Common use: 1

Special Ports	High-current drive port × 1
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Electrical Characteristics
Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz, VDD = 5 V			60	mA
Supply current at STOP	IDD2	VDD = 5 V			10	µA

Pin Assignment



LQFP080-P-1414A *Lead-free

Support Tool

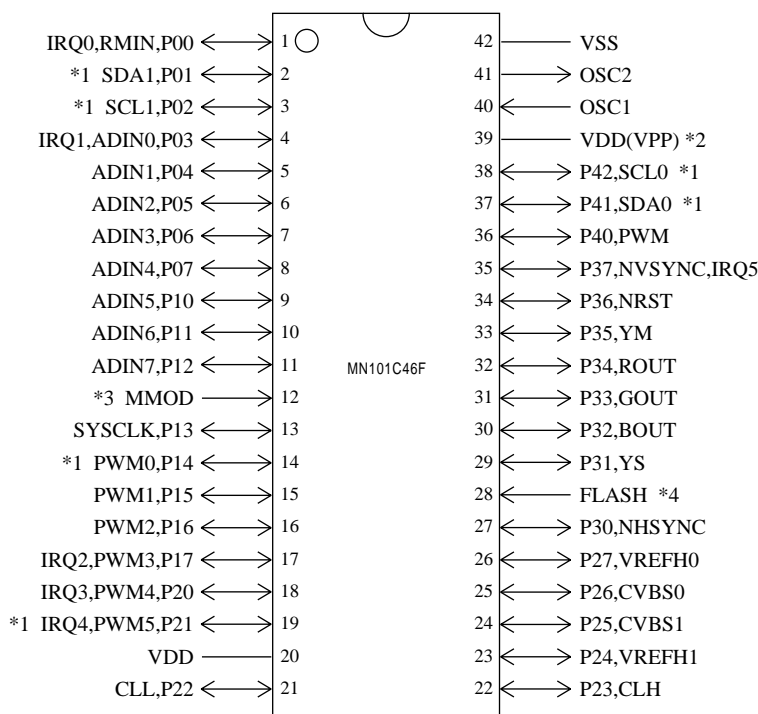
In-circuit Emulator	PX-ICE101C / D + PX-PRB101C29-LQFP080-P-1414A (under planning)	
Flash Memory Built-in Type	Type	MN101CF29D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	1.5 K
	Minimum instruction execution time	0.10 µs (at 4.5 V to 5.5 V, 20 MHz)
	Package	LQFP080-P-1414A *Lead-free

□ MN101C46F

Type	MN101C46F
ROM (x8-bit)	96 K
RAM (x8-bit)	3 K
Package (Conventional Package)	SDIP042-P-0600C *Lead-free (SDIP042-P-0600)
Minimum Instruction Execution Time	279 ns (at 3.0 V to 3.6 V, 14.32 MHz)
Interrupts	External (6 lines) Internal (12 lines) : Timer × 3, A/D, OSD, I ² C, Caption × 4, Remote control, Watchdog
Timer Counter	8-bit timer × 3 Watchdog timer: system clock fs 1/2 ¹⁶ , 1/2 ¹⁸ , 1/2 ²⁰ triple selection
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems
Caption	• Built-in sync separator × 2
I/O Pins	I/O 35 • Common use
A/D Inputs	5-bit × 8-ch. (with S/H)
PWM	8-bit × 6-ch. , 14-bit × 1-ch.
Special Ports	Remote control reception
CRTC	1-layer display (graphics, characters)
Notes	Remote control input discriminant circuit built-in

Pin Assignment

() : Conventional Package



SDIP042-P-0600C *Lead-free

(SDIP042-P-0600)

*1: 5 V dielectric Nch open drain output pin

*2: MN101C46F (VDD), MN101CF46F (VPP)

*3: MMOD = H (fixed) (Set the test mode pin to the normal mode.)

*4: FLASH = L (fixed) (Set the flash mode pin to the normal mode.)

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C46-SDIP042-P-0600-M	
EPROM Built-in Type	Type	MN101CF46F [ES (Engineering Sample) available]
	ROM (× 8-bit)	96 K
	RAM (× 8-bit)	3 K
	Minimum instruction execution time	279 ns (at 3.0 V to 3.6 V, 14.32 MHz)
	Package	SDIP042-P-0600C *Lead-free
	(Conventional Package)	(SDIP042-P-0600)

□ MN101C47C, MN101C47D

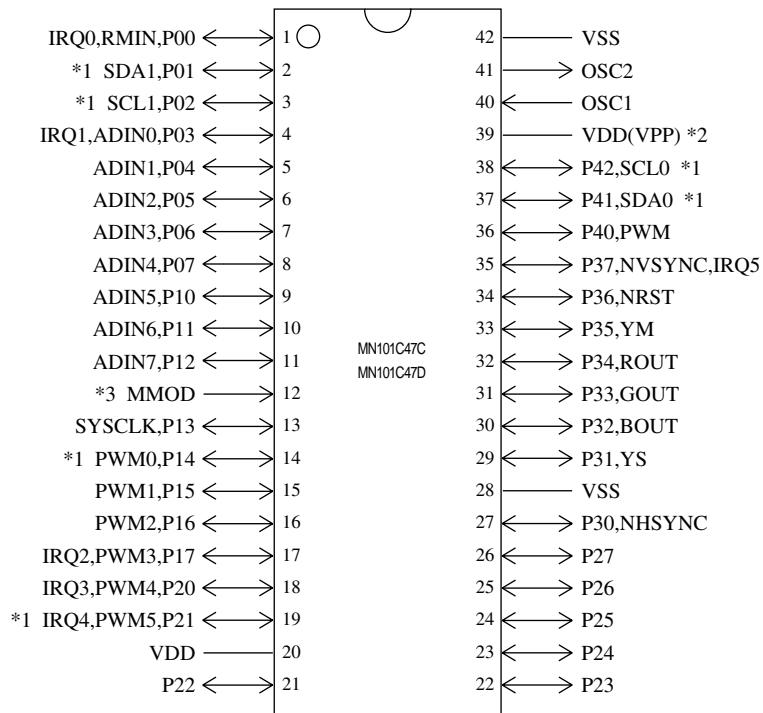
Type	MN101C47C	MN101C47D
ROM (x8-bit)	48 K	64 K
RAM (x8-bit)	1.5 K	2 K
Package (Conventional Package)	SDIP042-P-0600C *Lead-free, LQFP064-P-1414 *Lead-free (SDIP042-P-0600)	
Minimum Instruction Execution Time	279 ns (at 3.0 V to 3.6 V, 14.32 MHz)	
Interrupts	External (6 lines) Internal (8 lines) : Timer × 3, A/D, OSD, I ² C, Remote control, Watchdog	
Timer Counter	8-bit timer × 3 Watchdog timer: system clock fs 1/2 ¹⁶ , 1/2 ¹⁸ , 1/2 ²⁰ triple selection	
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems	
Caption	• Built-in sync separator × 2	
I/O Pins	I/O	35 • Common use: 29
A/D Inputs	5-bit × 8-ch. (with S/H)	
PWM	8-bit × 6-ch. , 14-bit × 1-ch.	
Special Ports	Remote control reception	
CRTC	1-layer display (graphics, characters)	
Notes	Remote control input discriminant circuit built-in	

Support Tool

In-circuit Emulator	PX-ICE101C/D+PX-PRB101C47-SDIP046-P-0600-M (under development)		
EPROM Built-in Type	Type	MN101CF46F (under development)	
	ROM (× 8-bit)	96 K	
	RAM (× 8-bit)	3 K	
	Minimum instruction execution time	279 ns (at 3.0 V to 3.6 V, 14.32 MHz)	
	Package (Conventional Package)	SDIP042-P-0600C *Lead-free, LQFP064-P-1414 *Lead-free (SDIP042-P-0600)	

Pin Assignment

() : Conventional Package



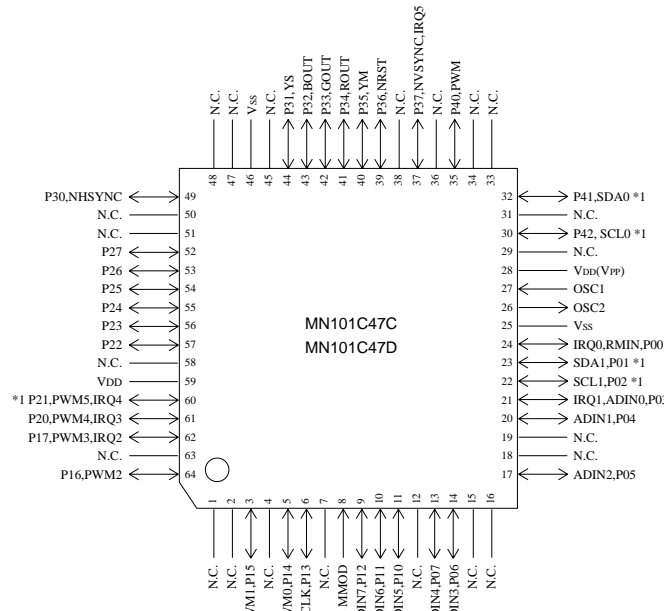
SDIP042-P-0600C *Lead-free

(SDIP042-P-0600)

*1: 5 V dielectric Nch open drain output pin

*2: Mask ROM = VDD, Flash memory built-in type = VPP

*3: MMOD = H (fixed) (Set the test mode pin to the normal mode.)



LQFP064-P-1414 *Lead-free

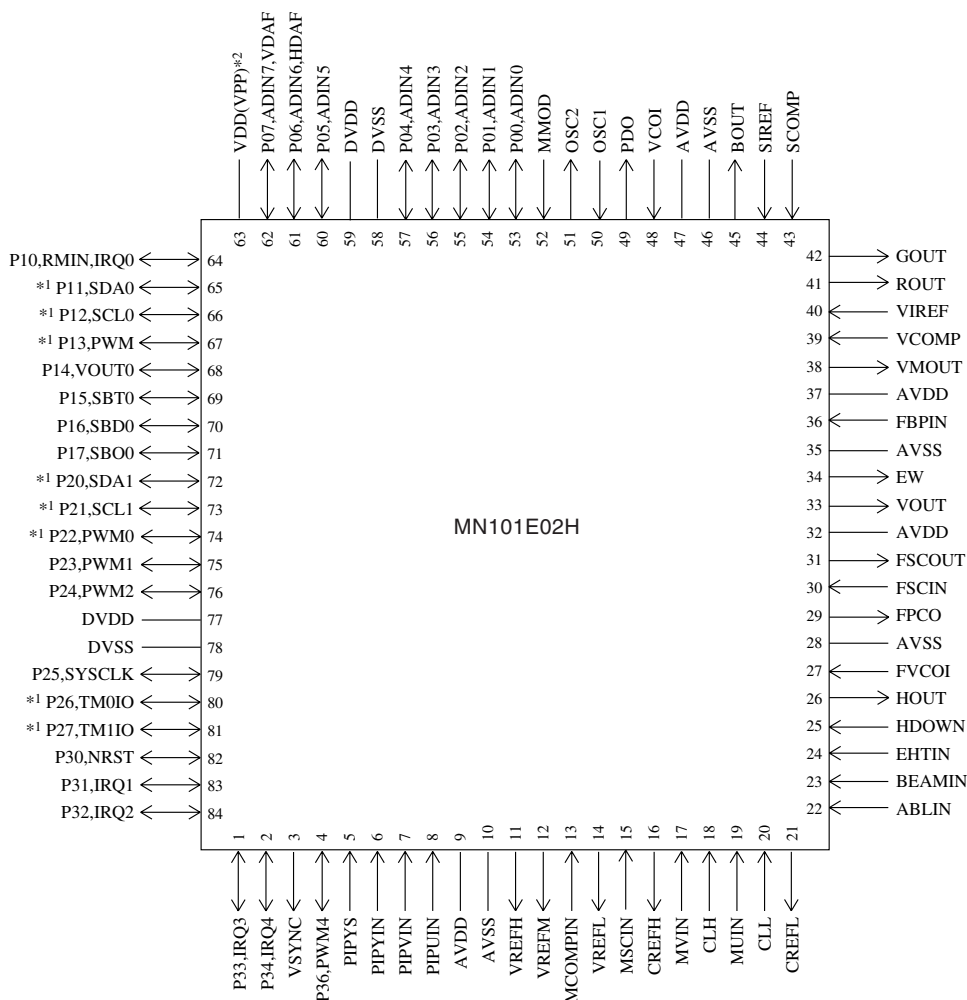
*1: 5 V dielectric Nch open drain output pin

*2: MMOD = H (fixed)

□ MN101E02H

Type	MN101E02H
ROM (×16-bit)	160 K
RAM (×16-bit)	16 K
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	100 ns (at 3.135 V to 3.465 V, normal-mode)
Interrupts	External (5 lines) Internal (15 lines) : Timer × 4, A/D × 1, RESET × 1, OSD × 1, Serial × 2, Teletext decoder × 2, I ² C × 1, Caption × 1, Remote control × 1, HSYNC × 1, VSYNC × 1
Timer Counter	8-bit timer × 4 Watchdog timer: Time-out period is selectable.
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1
Caption/Teletext Decoder	• Built-in sync separator × 1
I/O Pins	I/O 35 • Common use
A/D Inputs	10-bit × 8-ch. (with S/H)
PWM	8-bit × 4-ch. , 14-bit × 1-ch.
Special Ports	Remote control reception
CRTC	1-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in, built-in NTSC/PAL (BGHIDK, M, N)/SECAM/NTSC443 video signal processing circuit, built-in 3-line comb filter (NTSC) built-in adaptive 2-line comb filter (PAL), built-in teletext decoder

Pin Assignment



QFP084-P-1818E *Lead-free

*1: 5V dielectric Nch open drain output pin

*2: Mask ROM=VDD, Flash Memory built-in type=VPP

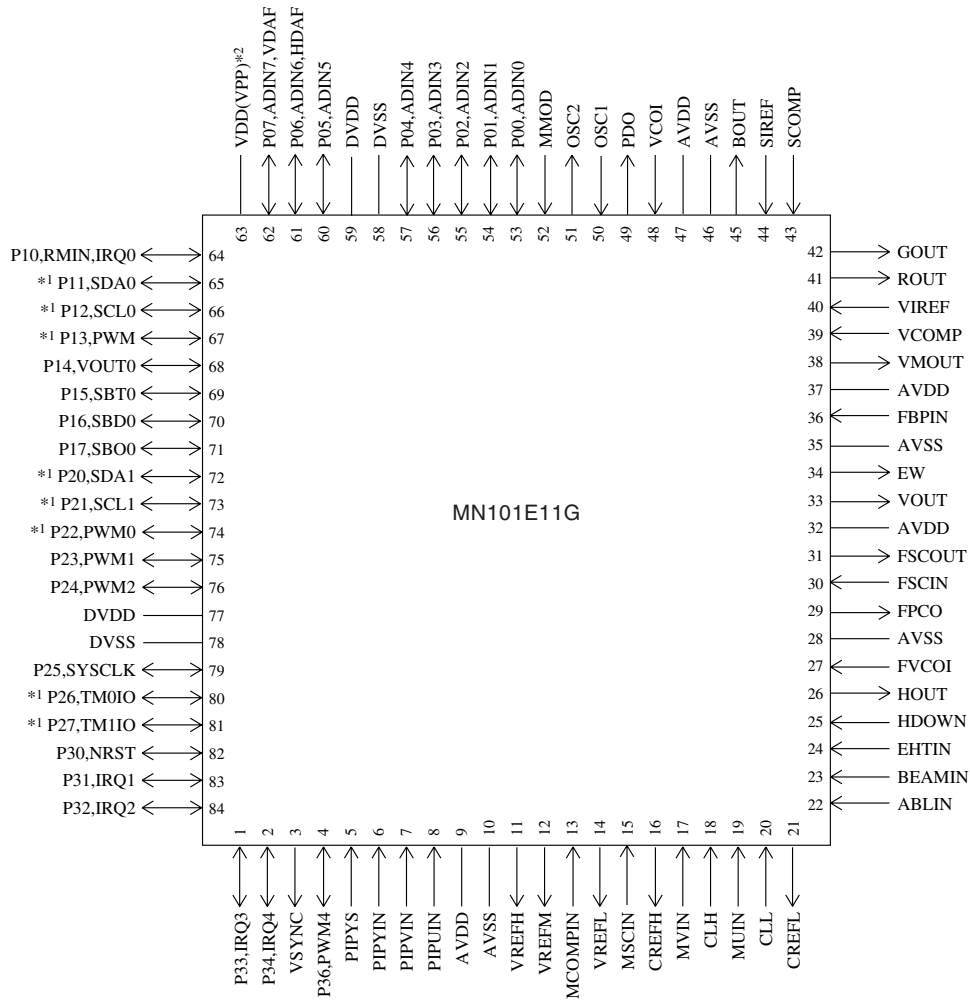
Support Tool

In-circuit Emulator	PX-PAC101E02-4W9J	
Flash Memory Built-in Type	Type	MN101EF02K [ES (Engineering Sample) available]
	ROM (× 8-bit)	160 K
	RAM (× 8-bit)	16 K
	Minimum instruction execution time	100 ns
	Package	QFP084-P-1818E *Lead-free

□ MN101E11G

Type	MN101E11G
ROM (×16-bit)	128 K
RAM (×16-bit)	4 K
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	100 ns (at 3.135 V to 3.465 V, normal-mode)
Interrupts	External (5 lines) Internal (13 lines) : Timer × 4, A/D × 1, RESET × 1, OSD × 1, Serial × 2, I ² C × 1, Caption × 1, Remote control × 1, HSYNC × 1, VSYNC × 1
Timer Counter	8-bit timer × 4 Watchdog timer: Time-out period is selectable.
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1
Caption/Teletext Decoder	• Built-in sync separator × 1
I/O Pins	I/O 30 • Common use
A/D Inputs	10-bit × 8-ch. (with S/H)
PWM	8-bit × 4-ch. , 14-bit × 1-ch.
Special Ports	Remote control reception
CRTC	1-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in, build-in NTSC video signal processing circuit, built-in 3-line comb filter PinP available

Pin Assignment



QFP084-P-1818E *Lead-free

*1: 5V dielectric Nch open drain output pin

*2: Mask ROM=VDD, Flash Memory built-in type=VPP

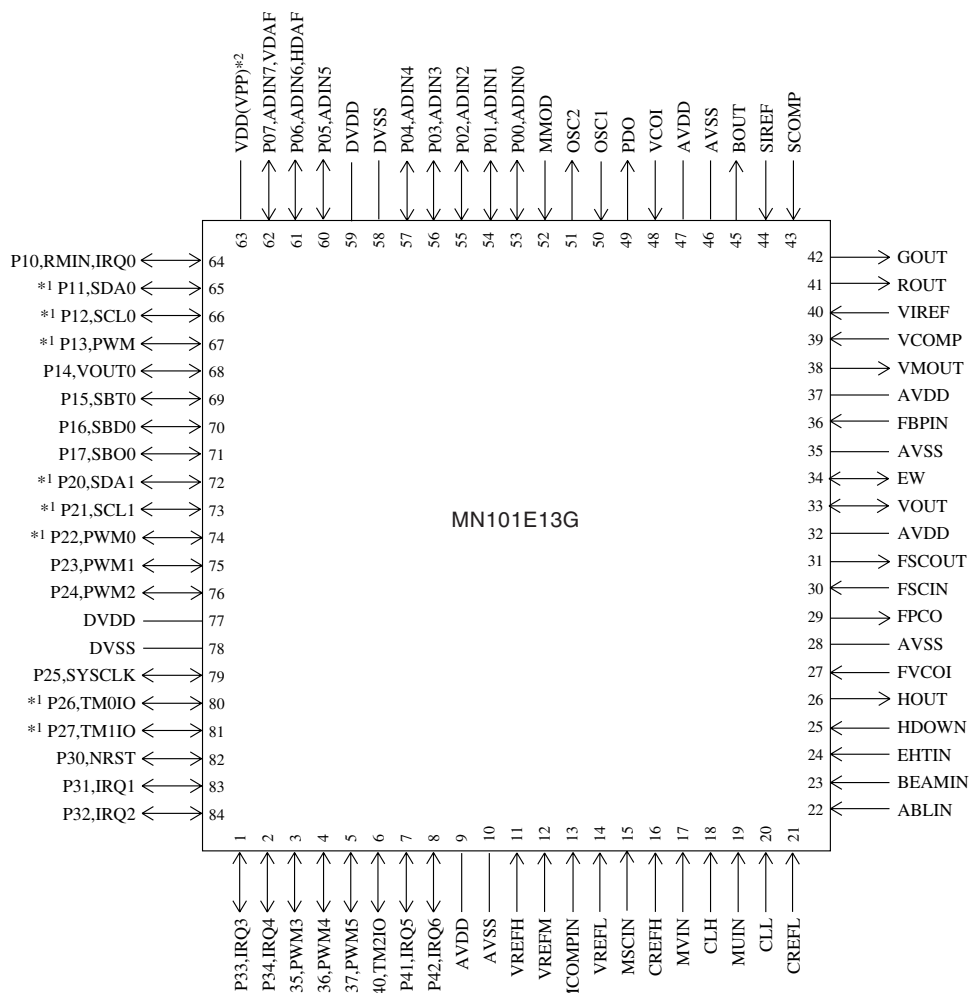
Support Tool

In-circuit Emulator	PX-PAC101E02-4W9J	
Flash Memory Built-in Type	Type	MN101EF03G [ES (Engineering Sample) available]
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	100 ns
	Package	QFP084-P-1818E *Lead-free

□ MN101E13G

Type	MN101E13G
ROM (×16-bit)	128 K
RAM (×16-bit)	4 K
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	100 ns (at 3.135 V to 3.465 V, normal-mode)
Interrupts	External (7 lines) Internal (13 lines) : Timer × 4, A/D × 1, RESET × 1, OSD × 1, Serial × 2, I ² C × 1, Caption × 1, Remote control × 1, HSYNC × 1, VSYNC × 1
Timer Counter	8-bit timer × 4 Watchdog timer: Time-out period is selectable.
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1
Caption/Teletext Decoder	• Built-in sync separator × 1
I/O Pins	I/O 35 • Common use
A/D Inputs	10-bit × 8-ch. (with S/H)
PWM	8-bit × 6-ch. , 14-bit × 1-ch.
Special Ports	Remote control reception
CRTC	1-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in, built-in NTSC video signal processing circuit, built-in 3-line comb filter

Pin Assignment



QFP084-P-1818E *Lead-free

*1: 5V dielectric Nch open drain output pin

*2: Mask ROM=VDD, Flash Memory built-in type=VPP

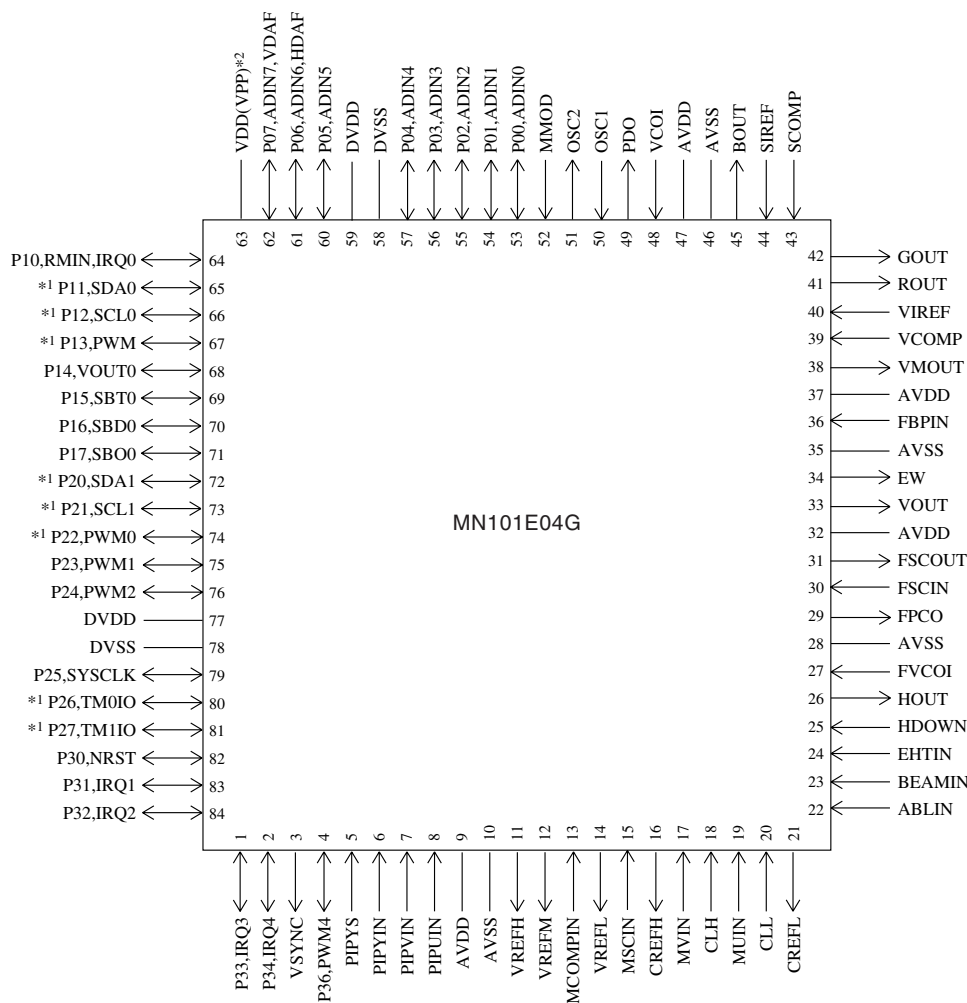
Support Tool

In-circuit Emulator	PX-PAC101E02-4W9J	
Flash Memory Built-in Type	Type	MN101EF13G [ES (Engineering Sample) available]
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	100 ns
	Package	QFP084-P-1818E *Lead-free

□ MN101E04G

Type	MN101E04G
ROM (×16-bit)	128 K
RAM (×16-bit)	4 K
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	100 ns (at 3.135 V to 3.465 V, normal-mode)
Interrupts	External (5 lines) Internal (13 lines) : Timer × 4, A/D × 1, RESET × 1, OSD × 1, Serial × 2, I ² C × 1, Caption × 1, Remote control × 1, HSYNC × 1, VSYNC × 1
Timer Counter	8-bit timer × 4 Watchdog timer: Time-out period is selectable.
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1
Caption/Teletext Decoder	• Built-in sync separator × 1
I/O Pins	I/O 30 • Common use
A/D Inputs	10-bit × 8-ch. (with S/H)
PWM	8-bit × 4-ch. , 14-bit × 1-ch.
Special Ports	Remote control reception
CRTC	1-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in, built-in NTSC/PAL/SECAM video signal processing circuit, built-in 3-line comb filter (NTSC) built-in adaptive 2-line comb filter (PAL)

Pin Assignment



QFP084-P-1818E *Lead-free

*1: 5V dielectric Nch open drain output pin

*2: Mask ROM=VDD, Flash Memory built-in type=VPP

Support Tool

In-circuit Emulator	PX-PAC101E02-4W9J	
Flash Memory Built-in Type	Type	MN101EF04G [ES (Engineering Sample) available]
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	100 ns
	Package	QFP084-P-1818E *Lead-free

□ MN101D06F , MN101D06G , MN101D06H

Type	MN101D06F	MN101D06G	MN101D06H
ROM (x8-bit)	96 K	128 K	160 K
RAM (x8-bit)	3 K	4 K	5 K
Package	QFP100-P-1818B *Lead-free		
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)	
		71.5 μs (at 3.0 V to 5.5 V fixed to 14.32 MHz internal frequency division)	
	When sub-clock operated	61 μs (at 2.2 V to 5.5 V, 32.768 kHz)	
Interrupts	<ul style="list-style-type: none"> • RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4 • key input (P50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW • Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 4 reference frequency) • OSD V-sync 		
Timer Counter	Timer counter 0: 16-bit × 1		
	(timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6])		
	Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6; 1/512 of XI oscillation clock or OSC oscillation clock frequency		
	Interrupt source overflow of timer counter 0		
	Timer counter 1: 16-bit × 1 (timer function, linear timer counter function)		
	Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; CTL signal		
	Interrupt source overflow of timer counter 1		
	Timer counter 2: 16-bit × 1 (timer function, input capture, duty judgment of CTL signal(VISS/VASS detection function))		
	Clock source 1/2, (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency		
	Interrupt source overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register		
Timer counter 3: 16-bit × 1			
(timer function, detection of serial indexing, generation of remote control output carrier frequency)			
Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock			
Interrupt source overflow of timer counter 3			
Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)			
Clock source 1/8, (1/16) of system clock frequency; external clock input			
Interrupt source overflow of timer counter 4; coincidence of timer counter 4 with OCR4			
Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)			
Clock source system clock			
Watchdog interrupt source .. 1/2 ¹⁶ , 1/2 ¹⁹ of timer counter 5 frequency			
Clear by stable oscillation .. after 256 counts by timer counter 5 (2 ¹⁸ counts of OSC oscillation clock)			
Timer counter 6: 16-bit × 1 (clock function [max. 2 s])			
Clock source 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, (1/8,) 1/64, (1/128) of system clock frequency			
Interrupt source 1/2 ¹³ , 1/2 ¹⁴ , 1/2 ¹⁵ overflow of timer counter 6			
Timer counter 7: 8-bit × 1 or 4-bit × 2 (timer function, event count)			
Clock source 1/4, (1/8,) 1/16, (1/32) of system clock frequency; external clock input			
Interrupt source overflow of timer counter 7 (although when 4-bit × 2, there is one interrupt vector.)			
Serial Interface	Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable)		
	Synchronous type clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT0 pin input		
	Clock for UART 8-division of above clock; 2-division timer 4 output; NSBT0 pin input		

Serial Interface (Continue)	Serial 1: 8-bit × 1 (synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function) Clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT1 pin input Remote control clock 2-division timer 4 output
	Serial 2: 8-bit × 1 (I ² C) (master transmission/reception, slave transmission/reception) Clock source 1/144 to 1/252 of system clock; SCK pin input

OSD	OSD mode: Accommodation with menu(internal synchronous) or super impose(external synchronous) display Applicable broadcasting system:NTSC, PAL, PAL-M, PAL-N Screen configuration : 24 characters × 2n rows (n = 1 to 6) Character type : max. 512 character types (variable, include special characters) Character size : 12 × 18 dots (Vertical direction: 1 dot for 2H at not enlargement) Enlarged characters : each × 2, × 3 or × 4 settings in horizontal and vertical Character interpolation : none Line background color : 8-hue settable (settable in the row unit at menu display) Line background intensity : 8 gradations settable in the row unit (at output of composite video signal) Screen background color : 8-hue settable (at output of composite video signal) Character color : white (at output of composite video signal) Character intensity : 8 gradations settable in the row unit (at output of composite video signal) Frame function : 1-dot frame in 4 or 8 directions Frame intensity : 4 gradations settable in the row unit (at output of composite video signal) Box shade function : settable in the character unit (at output of composite video signal with 129 or more characters (character types)) Blinking : none (covered by software) Inverted character : settable in the character unit Halftone : settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)
	CCD mode: Supports Closed Caption in the U.S.A. Screen configuration : 32 characters × 16 rows Character type : max. 128 character types (variable) Character size : 12 × 26 dots (Vertical direction: 1 dot for 1H, including 8 dots in the underlined area) Enlarged characters : none Character interpolation : none Line background color : 8-hue settable Line background intensity : 8 gradations settable in the screen unit (at output of composite video signal) Screen background color : 8-hue settable (at output of composite video signal) Character color : 8 colors (at RGB output) : White (at output of composite video signal) Character intensity : 8 gradations settable in the screen unit (at output of composite video signal) Frame function : none Box shade function : none Inverted character : none Halftone : settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal) Others : Underline, italic, blinking function and scroll Input : composite video signal input (output level: 1 V[p-p] / 2 V[p-p]) Clamp method : sync tip clamp, clamp level in 4 levels Output : composite video output : digital output (6 pins) Measure against image fluctuation : built-in AFC circuit Dot clock : 1/2 of OSC oscillation clock (automatic phase adjustment)

See the next page for electrical characteristics, pin assignment and support tool.

XDS	Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)		
ROM Correction	Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
I/O Pins	I/O	75	• Common use: 66
	Input	2	• Common use: 2
A/D Inputs	8-bit × 13-ch. (without S/H)		
PWM	13-bit × 2-ch. (at repetition cycle 572 μs at 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 μs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 71.5 μs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
ICR	18-bit × 6-ch.		
OCR	16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchronous output), 16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec CTL)		
Special Ports	Buzzer output; 3-state output VLP pin; remote control receive; CTL signal input terminal; Capstan FG input terminal; Sylinder(Durm) PG/FG input terminals; HSW output terminal; Head Amp/Rortary control output terminals; output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p])		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 3.0 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55 °C			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

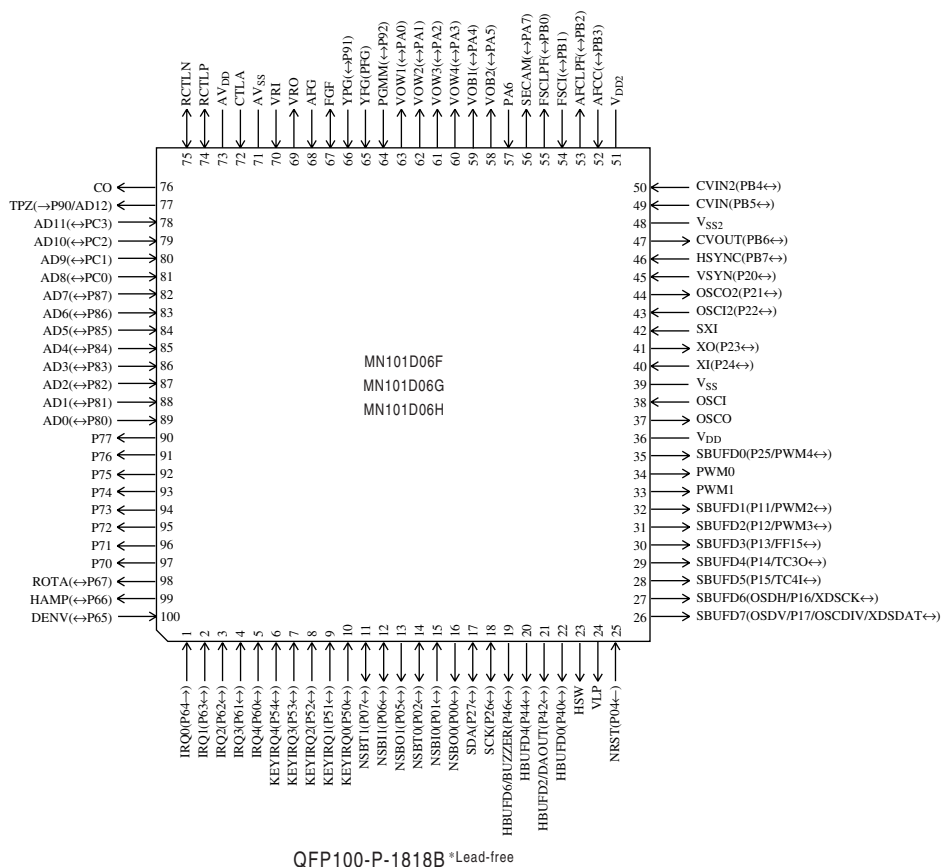
(Ta = 25 °C ± 2 °C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25 °C ± 2 °C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D06-QFP100-P-1818B-M	
Flash Memory Built-in Type	Type	MN101DF06ZAF
	ROM (× 8-bit)	224 K
	RAM (× 8-bit)	6 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

□ MN101D07G, MN101D07H

Type	MN101D07G	MN101D07H
ROM (×8-bit)	128 K	160 K
RAM (×8-bit)	4 K	5 K
Package	LQFP112-P-2020 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 3.0 V to 5.5 V fixed to 14.32 MHz internal frequency division)
	When sub-clock operated	61 μs (at 2.2 V to 5.5 V, 32.768 kHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4 • key input (P50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Timer 7 • Capstan FG • Control • HSW • Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 4 reference frequency) • OSD V-sync 	
Timer Counter	<p>Timer counter 0: 16-bit × 1 (timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6]) Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6; 1/512 of XI oscillation clock or OSC oscillation clock frequency Interrupt source overflow of timer counter 0</p> <p>Timer counter 1: 16-bit × 1 (timer function, linear timer counter function) Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; CTL signal Interrupt source overflow of timer counter 1</p> <p>Timer counter 2: 16-bit × 1 (timer function, input capture (DCTL specified edge), duty judgment of DCTL signal) Clock source 1/2, (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency Interrupt source overflow of timer counter 2; input of DCTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register</p> <p>Timer counter 3: 16-bit × 1 (timer function, detection of serial indexing, generation of remote control output carrier frequency) Clock source 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock Interrupt source overflow of timer counter 3</p> <p>Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock) Clock source 1/8, (1/16) of system clock frequency; external clock input Interrupt source overflow of timer counter 4; coincidence of timer counter 4 with OCR4</p> <p>Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function) Clock source system clock Watchdog interrupt source ... 1/2¹⁶, 1/2¹⁹ of timer counter 5 frequency Clear by stable oscillation ... after 256 counts by timer counter 5 (2¹⁸ counts of OSC oscillation clock)</p> <p>Timer counter 6: 16-bit × 1 (clock function [max. 2 s]) Clock source 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, (1/8,) 1/64, (1/128) of system clock frequency Interrupt source 1/2¹³, 1/2¹⁴, 1/2¹⁵ overflow of timer counter 6</p> <p>Timer counter 7: 8-bit × 1 or 4-bit × 2 (timer function, event count) Clock source 1/4, (1/8,) 1/16, (1/32) of system clock frequency; external clock input Interrupt source overflow of timer counter 7 (although when 4-bit × 2, there is one interrupt vector.)</p>	
Serial Interface	<p>Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable) Synchronous type clock source ... 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT0 pin input Clock for UART 8-division of above clock; 2-division timer 4 output; NSBT0 pin input</p>	

Serial Interface (Continue)	Serial 1: 8-bit × 1 (synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function)
	Clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT1 pin input
	Remote control clock 2-division timer 4 output
	Serial 2: 8-bit × 1 (I ² C) (master transmission/reception, slave transmission/reception)
	Clock source 1/144 to 1/252 of system clock, SCK pin input

OSD	OSD mode: Accommodation with menu(internal synchronous) or super impose(external synchronous) display																																												
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See the next page for electrical characteristics, pin assignment and support tool.

XDS	Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)		
ROM Correction	Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
I/O Pins	I/O	85	• Common use: 71
	Input	2	• Common use: 2
A/D Inputs	8-bit × 13-ch. (without S/H)		
PWM	13-bit × 2-ch. (at repetition cycle 572 μs at 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 μs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 71.5 μs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
ICR	18-bit × 6-ch.		
OCR	16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchronous output), 16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec CTL)		
Special Ports	Buzzer output; 3-state output VLP pin; remote control receive; CTL signal input terminal; Capstan FG input terminal; Sylinder(Durm) PG/FG input terminals; HSW output terminal; Head Amp/Rortary control output terminals; output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p])		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 3.0 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55 °C			20	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

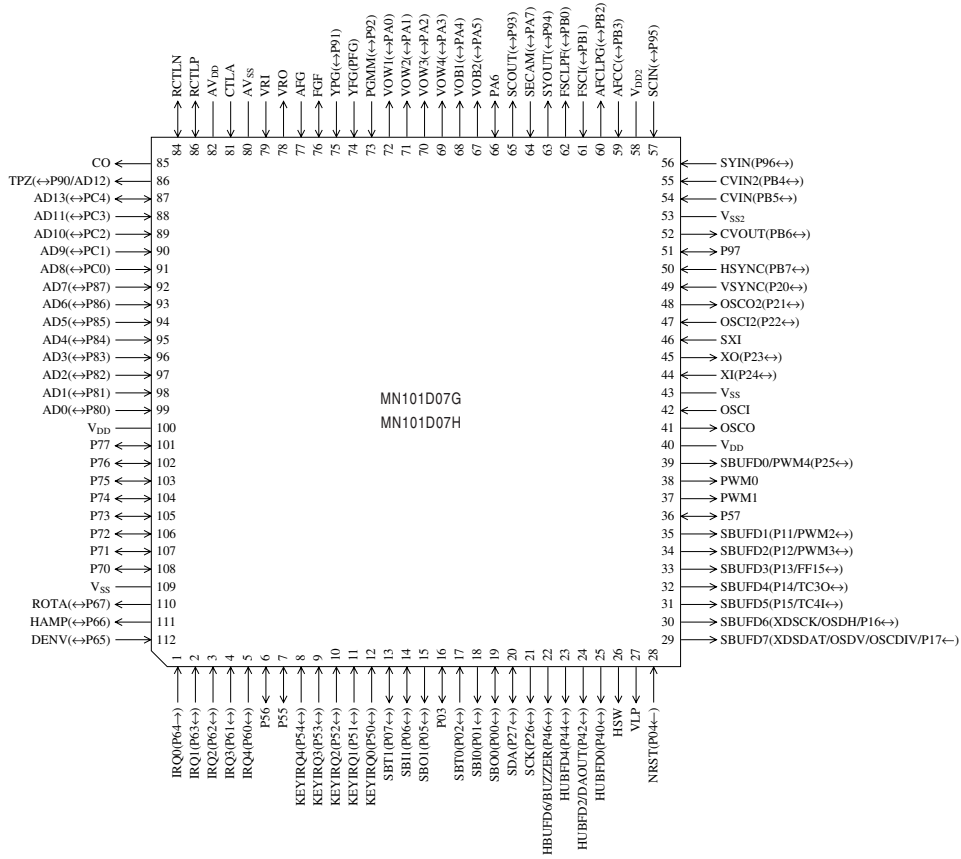
(Ta = 25 °C ± 2 °C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25 °C ± 2 °C, VSS = 0 V)

Pin Assignment



LQFP112-P-2020 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D07-LQFP112-P-2020-M	
Flash Memory Built-in Type	Type	MN101DF07ZAL
	ROM (× 8-bit)	224 K
	RAM (× 8-bit)	6 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	LQFP112-P-2020 *Lead-free

OSD		Display mode	:	Menu(Internal synchronized) display, super impose(external synchronized) display
		Applicable broadcasting system	:	NTSC, PAL, PAL-M, PAL-N
		Screen configuration	:	24 characters ´ 2n rows (n = 1 to 6)
		Character type	:	max. 128 character types (variable, include special characters)
		Character size	:	12 ´ 18 dots (Vertical direction: 1 dot for 2H at not enlargement.)
		Enlarged characters	:	each ´ 2 settings in horizontal and vertical
		Character interpolation	:	none
		Line background color	:	8-hue settable (settable in the row unit at menu display)
		Line background intensity	:	8 gradations settable in the row unit
		Screen background color	:	8-hue settable at menu display
		Character color	:	white
		Character intensity	:	8 gradations settable in the row unit
		Frame function	:	1-dot frame in 4 directions
		Frame intensity	:	4 gradations settable in the row unit
		Blinking	:	none (covered by software)
		Inverted character	:	settable in the character unit
		Halftone	:	none
		Input	:	composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
		Clamp method	:	sync tip clamp, clamp level in 4 levels
		Output	:	composite video output
		Measure against image fluctuation:	:	built-in AFC circuit
		Dot clock	:	1/2 of OSC oscillation clock (automatic phase adjustment)
XDS		Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.)		
ROM Correction		Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
I/O Pins	I/O	56	• Common use: 45	
	Input	1	• Common use: 1	
A/D Inputs		8-bit ´ 11-ch. (without S/H)		
PWM		13-bit ´ 2-ch. (at repetition cycle 572 µs at 14.32 MHz), 8-bit ´ 1-ch. (at repetition cycle 71.5 µs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
ICR		16-bit ´ 2-ch.(Speed system), 18-bit ´ 4-ch.(Phase system)		
OCR		16-bit ´ 3 (Synchronous output ´ 2, Rec CTL ´ 1)		
Special Ports		3-state output (PTO) VLP pin; CTL input; Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output; Head amp/ Rotary control outputs; output of 1/4 OSC oscillation clock (1 V[p-p])		
Notes				

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

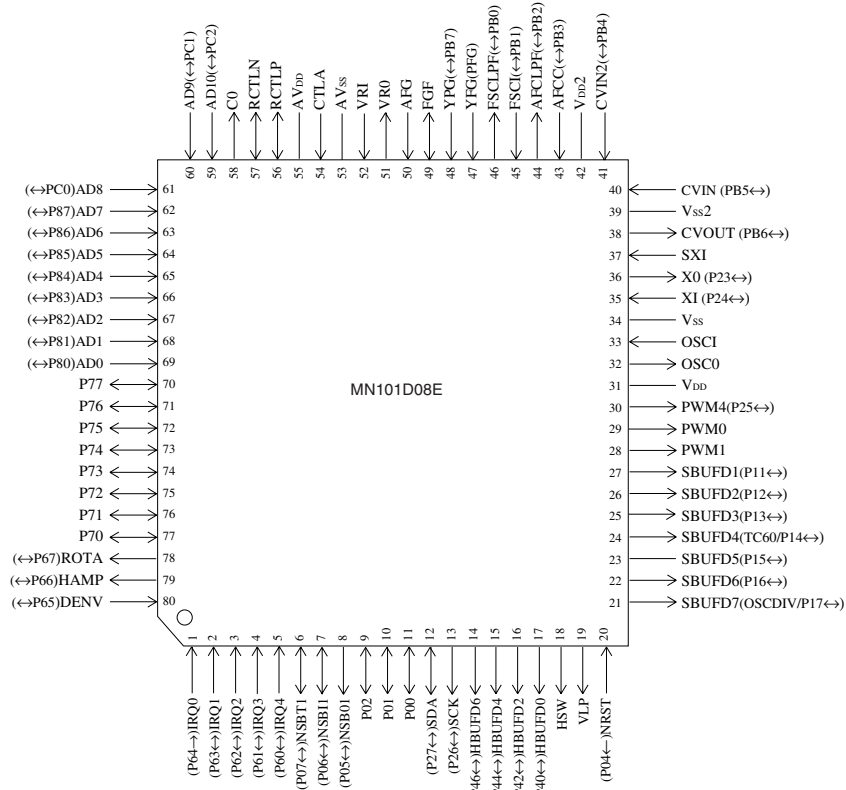
(Ta = 25°C ± 2°C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25°C ± 2°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



LQFP080-P-1414A *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D08-LQFP080-P-1414A	
Flash Memory Built-in Type	Type	MN101DF08G AL
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	LQFP080-P-1414A *Lead-free

□ MN101D09E

Type	MN101D09E	
ROM (x8-bit)	80 K	
RAM (x8-bit)	2 K	
Package	QFP100-P-1818B *Lead-free	
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)
		71.5 μs (at 2.7 V to 5.5 V fixed to 14.32 MHz internal frequency division)
	When sub-clock operated	61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Runaway • External 0, 1, 2, 3, 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Capstan FG • Control • HSW • Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 1 • Serial 2 • PWM 4 • OSD V-sync 	
Timer Counter	Timer counter 0: 8-bit × 1 (timer function)	
	Clock source	1/4, 1/16 of system clock frequency
	Interrupt source	overflow of timer counter 0
	Timer counter 1: 8-bit × 1 (timer function, linear timer counter function)	
	Clock source	1/4 of system clock frequency; CTL signal
	Interrupt source	overflow of timer counter 1
	Timer counter 2: 16-bit × 1 (timer function, input capture (CTL specified edge), duty judgment of CTL signal)	
	Clock source	1/4, 1/16, 1/24 of system clock frequency
	Interrupt source	overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register
	Timer counter 3: 16-bit × 1 (timer function)	
	Clock source	1/4, 1/16 of system clock frequency
	Interrupt source	overflow of timer counter 3
Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)		
Clock source	system clock	
Watchdog interrupt source	1/2 ¹⁶ , 1/2 ¹⁹ of timer counter 5 frequency	
Clear by stable oscillation	after 256 counts by timer counter 5 (2 ¹⁸ counts of OSC oscillation clock)	
Timer counter 6: 16-bit × 1 (clock function [max. 2 s])		
Clock source	1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency	
Interrupt source	1/2 ¹³ , 1/2 ¹⁴ , 1/2 ¹⁵ overflow of timer counter 6	
Serial Interface	Serial 1: 8-bit × 1 (synchronous type)	
	(transfer direction of MSB/LSB selectable, start condition function)	
	Clock source	1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; NSBT1 pin input
Serial 2: 8-bit × 1 (I ² C) (master transmission/reception, slave transmission/reception)		
Clock source	1/144 to 1/252 of system clock; SCK pin input	

OSD		Display mode	:	Menu(Internal synchronized) display, super impose(external synchronized) display
		Applicable broadcasting system	:	NTSC, PAL, PAL-M, PAL-N
		Screen configuration	:	24 characters × 2n rows (n = 1 to 6)
		Character type	:	max. 128 character types (variable, include special characters)
		Character size	:	12 × 18 dots (Vertical direction: 1 dot for 2H at not enlargement)
		Enlarged characters	:	each × 2 settings in horizontal and vertical
		Character interpolation	:	none
		Line background color	:	8-hue settable in the row unit at menu display
		Line background intensity	:	8 gradations settable in the row unit
		Screen background color	:	8-hue settable at menu display
		Character color	:	white
		Character intensity	:	8 gradations settable in the row unit
		Frame function	:	1-dot frame in 4 directions
		Frame intensity	:	4 gradations settable in the row unit
		Blinking	:	none (covered by software)
		Inverted character	:	settable in the character unit
		Halftone	:	none
		Input	:	composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
		Clamp method	:	sync tip clamp, clamp level in 4 levels
		Output	:	composite video output
		Measure against image fluctuation:	:	built-in AFC circuit
		Dot clock	:	1/2 of OSC oscillation clock (automatic phase adjustment)
XDS		Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.)		
ROM Correction		Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
I/O Pins	I/O	56	• Common use: 45	
	Input	1	• Common use: 1	
A/D Inputs		8-bit × 11-ch. (without S/H)		
PWM		13-bit × 2-ch. (at repetition cycle 572 μs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 71.5 μs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
ICR		16-bit × 2-ch.(Speed system), 18-bit × 4-ch.(Phase system)		
OCR		16-bit × 3 (Synchronous output × 2, Rec CTL × 1)		
Special Ports		3-state output (PTO) VLP pin; CTL input; Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output; Head amp/ Rotary control outputs; output of 1/4 OSC oscillation clock (1 V[p-p])		
Notes				

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

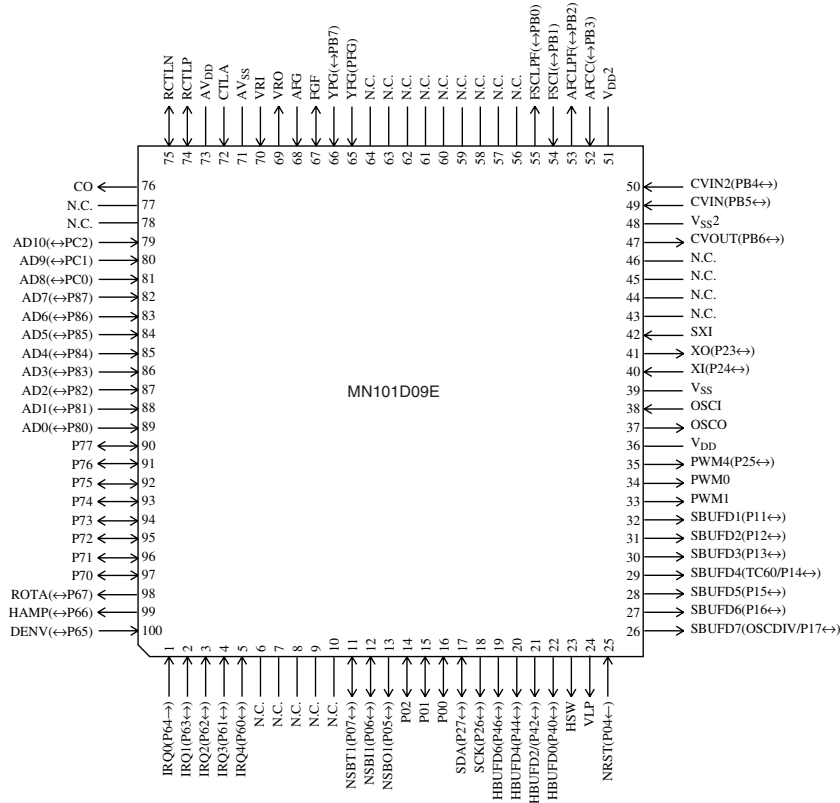
(Ta = 25°C ± 2°C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25°C ± 2°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



QFP100-P-1818B *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D08-QFP100-P-1818B-M	
Flash Memory Built-in Type	Type	MN101DF09GAF
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

□ MN101D10F , MN101D10G

Type	MN101D10F	MN101D10G
ROM (x8-bit)	96 K	128 K
RAM (x8-bit)	2.5 K	3.5 K
Package	QFP100-P-1818B *Lead-free	
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V fixed to 14.32 MHz internal frequency division)
	When sub-clock operated	61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Capstan FG • Control • HSW • Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • PWM 4 • OSDV-sync 	
Timer Counter	Timer counter 0: 8-bit × 1 (timer function)	
	Clock source	1/4, 1/16 of system clock frequency
	Interrupt source	overflow of timer counter 0
	Timer counter 1: 8-bit × 1 (timer function, linear timer counter function)	
	Clock source	1/4 of system clock frequency; CTL signal
	Interrupt source	overflow of timer counter 1
Timer counter 2: 16-bit × 1 (timer function, input capture, duty judgment of CTL signal(VISS/VASS detection function), generation of remote control output carrier frequency)		
Clock source	1/4, 1/16, 1/24 of system clock frequency	
Interrupt source	overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register	
Timer counter 3: 16-bit × 1 (timer function, generation of serial transmission clock)		
Clock source	1/4, 1/16 of system clock frequency	
Interrupt source	overflow of timer counter 3	
Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)		
Clock source	system clock	
Watchdog interrupt source	1/2 ¹⁶ , 1/2 ¹⁹ of timer counter 5 frequency	
Clear by stable oscillation	after 256 counts by timer counter 5 (2 ¹⁸ counts of OSC oscillation clock)	
Timer counter 6: 16-bit × 1 (clock function [max. 2 s])		
Clock source	1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency	
Interrupt source	1/2 ¹³ , 1/2 ¹⁴ , 1/2 ¹⁵ overflow of timer counter 6	
Serial Interface	Serial 0: 8-bit × 1 (synchronous type)	
	(transfer direction of MSB/LSB selectable, start condition function)	
	Clock source	1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; NSBT0 pin input
	Serial 1: 8-bit × 1 (synchronous type/remote control transmission)	
(transfer direction of MSB/LSB selectable, start condition function)		
Clock source	1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 3 output; NSBT1 pin input	
Remote control clock	2-division timer 3 output	
Serial 2: 8-bit × 1 (I ² C) (master transmission/reception, slave transmission/reception)		
Clock source	1/144 to 1/252 of system clock; SCK pin input	

OSD		Display mode	:	menu(internal synchronized) display, superimpose(externally synchronized) display
		Applicable broadcasting system	:	NTSC, PAL, PAL-M, PAL-N
		Screen configuration	:	24 characters × 2n rows (n = 1 to 6)
		Character type	:	max. 256 character types (variable, include special characters)
		Character size	:	12 × 18 dots (vertical direction: 1 dot for 2H at not enlargement)
		Enlarged characters	:	each × 2 settings in horizontal and vertical
		Character interpolation	:	none
		Line background color	:	8-hue settable in the row unit at menu display
		Line background intensity	:	8 gradations settable in the row unit
		Screen background color :	:	8-huesettable at menu display
		Character color	:	white
		Character intensity	:	8 gradations settable in the row unit
		Border function	:	1-dot border in 8 directions
		Border brightness	:	4 gradations settable in the row unit
		Blinking	:	none (covered by software)
		Inverted character	:	settable in the character unit
		Halftone	:	none
		Input	:	composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
		Clamp method	:	sync tip clamp, clamp level in 4 levels
		Output	:	composite video output
		Measure against image fluctuation	:	built-in AFC circuit
		Dot clock	:	1/2 of OSC oscillation clock (automatic phase adjustment)
		MESECAM compatibility	:	Subcarrier leak function for superimpose display
XDS		Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.)		
ROM Correction		Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
I/O Pins	I/O	76	• Common use: 56	
	Input	1	• Common use: 1	
A/D Inputs		8-bit × 12-ch. (without S/H)		
PWM		13-bit × 2-ch. (at repetition cycle 572 μs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 35.7 μs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
ICR		16-bit × 2-ch.(Speed system), 18-bit × 4-ch.(Phase system)		
OCR		16-bit × 3 (Synchronous output × 2, Rec CTL × 1)		
Special Ports		3-state output (PTO) VLP pin; CTL input;Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output; Head amp/ Rotary outputs; built-in FG amp; output of 1/4 OSC oscillation clock (1 V[p-p])		
Notes				

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55 °C			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

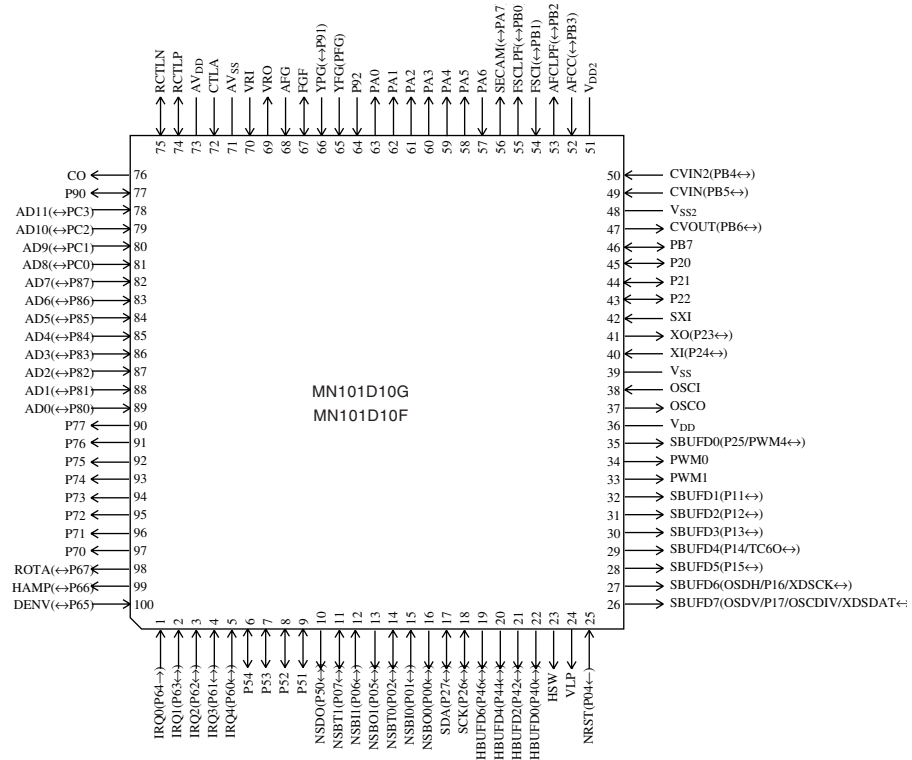
(Ta = 25 °C ± 2 °C, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25 °C ± 2 °C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



QFP100-P-1818B *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D10-QFP100-P-1818B-CN-M	
Flash Memory Built-in Type	Type	MN101DF10GAF
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

□ MN101D03D

Type	MN101D03D
ROM (x8-bit)	64 K
RAM (x8-bit)	2 K
Package	LQFP080-P-1414A *Lead-free
Minimum Instruction Execution Time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz) 0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)*1 125 μs (at 2.0 V to 5.5 V, 32 kHz)*2

*1 The lower limit for operation guarantee for flash memory built-in type is 4.5 V.

*2 The lower limit for operation guarantee for EPROM built-in type is 2.3 V.

Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • External 0 • External 1 • External 2 • External 3 • External 4 • External 5 • External 6 • External 7 • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 5 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 reception • Serial 0 transmission • Serial 1 • Serial 2 • Automatic transfer finish • A/D conversion finish • Key interrupts (8 lines)
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Timer Counter	<p>Timer counter 0 : 8-bit × 1 (square-wave output [timer pulse output], PWM output, event count, remote control carrier output, simple pulse width measurement function) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 1 : 8-bit × 1 (square-wave output [timer pulse output], event count, timer synchronous output) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 0, 1 can be cascade-connected.</p> <p>Timer counter 2 : 8-bit × 1 (square-wave output [timer pulse output], PWM output, event count, timer synchronous output, simple pulse width measurement function) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 3 : 8-bit × 1 (square-wave output [timer pulse output], event count, remote control carrier output) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 2, 3 can be cascade-connected.</p> <p>Timer counter 4 : 8-bit × 1 (square-wave output [timer pulse output], PWM output, event count, simple pulse width measurement function) Clock source 1/2, 1/4 of system clock frequency; 1/1, 1/4, 1/16, 1/32, 1/64 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 5 : 8-bit × 1 (square-wave output [timer pulse output], event count) Clock source 1/2, 1/8 of system clock frequency; 1/1, 1/4, 1/16, 1/64, 1/128 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; external clock input</p> <p>Timer counter 4, 5 can be cascade-connected.</p> <p>Time base timer Clock source 1/2⁷, 1/2⁸, 1/2⁹, 1/2¹⁰, 1/2¹³, 1/2¹⁵ of OSC oscillation clock frequency; 1/2⁷, 1/2⁸, 1/2⁹, 1/2¹⁰, 1/2¹³, 1/2¹⁵ of XI oscillation clock frequency</p> <p>Timer counter 6 : 8-bit freerun timer Clock source 1/1 of system clock frequency; 1/1, 1/2⁷, 1/2¹³ of OSC oscillation clock frequency; 1/1, 1/2⁷, 1/2¹³ of XI oscillation clock frequency</p>
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Timer Counter (Continue)

Timer counter 7 : 16-bit × 1

Clock source either of system clock, OSC oscillation clock, external clock 1 or external clock 2 frequency-divided into 1/1, 1/2, 1/4 or 1/16)
 (hardware configuration)
 double buffer type compare register × 2
 input capture register × 1
 (timer functions)
 square-wave output (timer pulse output), high-precision PWM output (cycle/duty continuously variable), event count, simple pulse width measurement function and input capture function

Timer counter 8 : 16-bit × 1

Clock source either of system clock, OSC oscillation clock, external clock 1 or external clock 2 frequency-divided into 1/1, 1/2, 1/4 or 1/16)
 (hardware configuration)
 double buffer type compare register × 2
 input capture register × 1
 (timer functions)
 square-wave output (timer pulse output), PWM output (duty continuously variable), event count, simple pulse width measurement function and input capture function

Watchdog timer

Interrupt source runaway detection frequency selection from $1/2^{16}$, $1/2^{18}$ and $1/2^{20}$ of system clock frequency

Serial Interface

Serial 0 : 8-bit × 1 (full-duplex UART/ synchronous type)

Synchronous type (MSB or LSB first selectable; 1 to 8 bits arbitrary transmission; continuous transmission, continuous reception and continuous transmission-reception possible by combination with ATC function)

Transfer clock source 1/2, 1/4 of system clock frequency;
 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency;
 timer counter 2 to 5 output;
 1/3 of frequency of the above clocks

Full-duplex UART (built-in baud rate timer, parity check, overrun error/framing error detection, transfer bit selectable from 7 and 8 bits)

Serial 1 : 8-bit × 1 (simple I²C/ synchronous type)

Synchronous type (MSB or LSB first selectable; 1 to 8 bits arbitrary transmission; continuous transmission, continuous reception and continuous transmission-reception possible by combination with ATC function)

Transfer clock source: 1/2, 1/4 of system clock frequency;
 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency;
 timer counter 2 to 5 output;
 1/3 of frequency of the above clocks

Simple I²C (I²C transmission function with single master [9-bit transmission])

Serial 2 : 8-bit × 1 (3-wire synchronous type)

Synchronous type (MSB or LSB first selectable; 1 to 8 bits arbitrary transmission; continuous transmission, continuous reception and continuous transmission-reception possible by combination with ATC function)

Transfer clock source 1/2, 1/4 of system clock frequency;
 1/2, 1/4, 1/16, 1/32 of OSC oscillation clock frequency;
 timer counter 2 to 5 output;
 1/3 of frequency of the above clocks

See the next page for electrical characteristics, pin assignment and support tool.

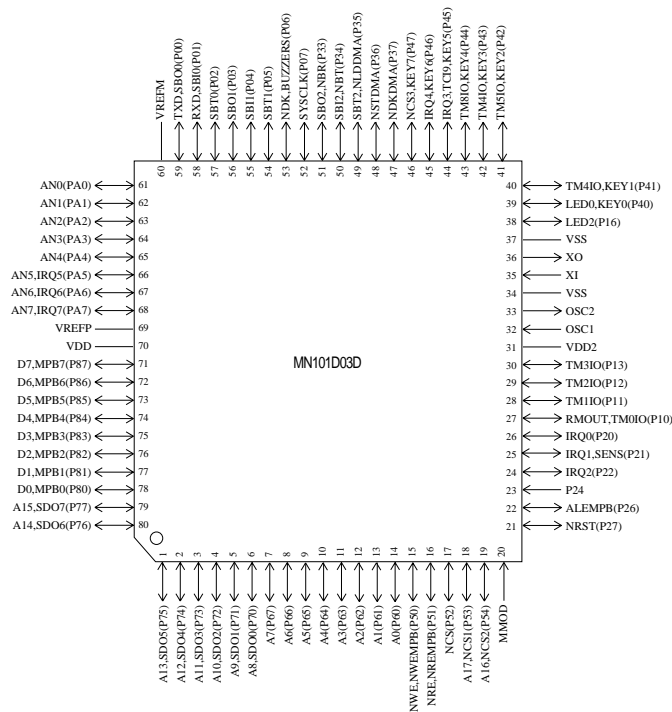
I/O Pins	I/O	67	• Common use • Specified pull-up resistor available • Input/output selectable (bit unit)
	Input	1	• Common use
A/D Inputs	10-bit × 8-ch. (with S/H) Conversion Cause 7 A/D control register setting; timer 4, 6 or 8 interrupt; external interrupt 3 or 7; serial 1 interrupt		
Special Ports	Buzzer output, remote control carrier signal output, high-current drive port × 1		

Electrical Characteristics
Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz , VDD = 5 V			60	mA
	IDD2	fosc = 8.39 MHz , VDD = 5 V			25	mA
	IDD3	*fx = 32 kHz , VDD = 3 V			120	μA
Supply current at HALT	IDD4	fx = 32 kHz , VDD = 3 V , Ta = 25°C			8	μA
		fx = 32 kHz , VDD = 3 V , Ta = 85°C			20	μA
Supply current at STOP	IDD5	VDD = 5 V			10	μA

* Flash memory built-in type : 300 μA max. at VDD = 5 V

Pin Assignment



LQFP080-P-1414A *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D03-LQFP080-P-1414A	
EPROM Built-in Type	Type	MN101DP03FAL
	ROM (× 8-bit)	96 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.238 μs (at 2.7 V to 5.5 V, 8.39 MHz)
		125 μs (at 2.3 V to 5.5 V, 32 kHz)
Package	LQFP080-P-1414A *Lead-free	
Flash Memory Built-in Type	Type	MN101DF03D
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	0.10 μs (at 4.5 V to 5.5 V, 20 MHz)
		0.238 μs (at 4.5 V to 5.5 V, 8.39 MHz)
	Package	LQFP080-P-1414A *Lead-free

AM2^{16-bit} SERIES

AM2 (MN102) Series

The AM2 series uses a simple and elegant architecture that executes basic instructions at a rate of 1 byte per cycle to achieve high-speed operation with a minimum instruction execution time of 100 ns at 20 MHz. These are 16-bit microcontrollers with an ASIC expansion bus to allow the customers to incorporate peripheral circuitry of their original design in them with ease.

These equipment-oriented microcontrollers demonstrate high realtime performance.

Features

- **16-bit architecture**

1-bit minimum instruction code -- 50 ns minimum instruction execution time (at 40 MHz)

- **Elegant architecture**

High-Efficiency 1 byte per cycle instructions

Achievement of higher speeds for load/store transfer and branch instructions, etc.

- **Flexible expansion of functions**

Achievement of a microcontroller that supports customization through an ASIC expansion bus

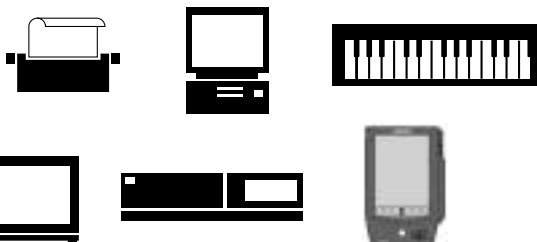
- **Software support**

ANSI C language -- μ ITRON*-specification realtime OS

* ITRON is an abbreviation of "Industrial TRON."

■ Application

General-use



□ MN102L59D

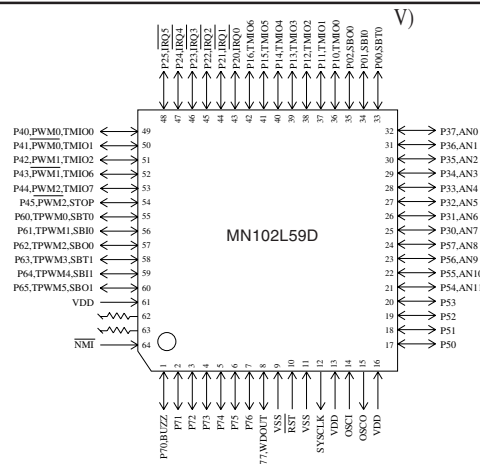
Type	MN102L59D
ROM (×8-bit)	64 K
RAM (×8-bit)	2 K
Package	LQFP064-P-1414 *Lead-free
Minimum Instruction Execution Time	With main clock operated: 100 ns (at 4.5 V to 5.5 V, 5 MHz externally, multiplied by 4 internally)
Interrupts	• RESET • Watchdog • Timer counter 0 to 11 • External 0 to 5 • Serial ch.0, 1 transfer finish • NMI pin • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (timer output, event count) Clock source 1/1, 1/64, 1/128 of system clock frequency; external clock Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (timer output, event count, A/D conversion start up) Clock source 1/1, 1/64 of system clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1 (timer output, event count) Clock source system clock; external clock; timer counter 0, 1 output Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1 (interval timer, UART baud rate generator) Clock source 1/1, 1/2, 1/64 of system clock frequency; timer counter 0 output Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1 (interval timer) Clock source 1/1, 1/64, 1/128 of system clock frequency; timer counter 0 output Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1 (interval timer) Clock source 1/1, 1/64 of system clock frequency; timer counter 0, 4 output Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 16-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 16-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1 (timer output, event count, simple PWM output) Clock source 1/2, 1/8 of system clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 8</p> <p>Timer counter 9 : 8-bit × 1 (timer output, event count, simple PWM output) Clock source 1/2, 1/8 of system clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 9</p> <p>Timer counter 10 : 8-bit × 1 (timer output, simple inverter control [simple 6-phase PWM output]) Clock source high-speed clock (after multiplication); 1/1, 1/2, 1/8 of system clock frequency Interrupt source overflow of timer counter 10</p> <p>Timer counter 11 : 16-bit updown counter × 1 (highly functional inverter control [simple 6-phase PWM output], A/D conversion start) Clock source high-speed clock (after multiplication); 1/1 of system clock frequency Interrupt source overflow of timer counter 11; underflow of timer counter 11</p>
	<div style="border: 1px solid black; border-radius: 10px; padding: 2px; display: inline-block;">Connectable</div> timer counter 0, 1, 2 timer counter 0, 4, 5

Serial Interface	Serial 0, 1 : 1 to 8-bit × 1 (common use with half-duplex UART, transfer direction of MSB/LSB selectable) Clock source 1/2, 1/4, 1/16 of system clock, 1/2 of timer counter 3, external clock Half-duplex UART × 2 (common use with serial 0, 1)
I/O Pins	I/O 52 • Common use : 52 (by bit)
A/D Inputs	10-bit × 12-ch. (with S/H) : 4 channels for common use
PWM	16-bit × 2-ch. (common use with timer counter 6,7) simple 6-phase PWM output 8-bit × 1-ch.(common use with timer counter 10) 6-phase PWM output 16-bit × 1ch. (timer counter 11)
Notes	6-phase PWM output support

Electric Characteristics						
Supply current						
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 5 MHz, VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT0	IDDH	pins are simultaneously applied VDD or VSS level f = 5 MHz, VDD = 5.0 V, output open			30	mA

(Ta = -20°C to +85°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



LQFP064-P-1414 *Lead-free

* The MN102LF59D is manufactured and sold under license agreement with BULL CP8 Inc.

Support Tool

Note that MN102LF59D cannot be used as the IC card.

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L59-LQFP064-P-1414	
Flash Memory Built-in Type	Type	MN102LF59D [ES (Engineering Sample) available]
	ROM (× 8-bit)	64 K
	RAM (× 8-bit)	2 K
	Minimum instruction execution time	100 ns (at 4.5 V to 5.5 V, 5 MHz externally, multiplied by 4 internally)
	Package	LQFP064-P-1414 *Lead-free

□ MN102L62G

Type	MN102L62G
ROM (×8-bit)	128 K
RAM (×8-bit)	5 K
Package	LQFP100-P-1414 *Lead-free
Minimum Instruction Execution Time	100 ns (at 4.5 V to 5.5 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer counter 0 to 5 • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 4 • Serial ch.0, 1 transmission • Serial ch.0, 1 reception • NMI pin • A/D conversion finish
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (timer output, event count, A/D conversion start up) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 to 3 : 8-bit × 1 (timer output, event count, UART baud rate generator) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source underflow of timer counter 2, 3</p> <p>Timer counter 4, 5 : 8-bit × 1 (timer output, event count) Clock source 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source underflow of timer counter 4, 5</p> <p>Timer counter 6, 7 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7</p> <p style="text-align: center;">(Connectable) timer counter 0 to 5</p>
Serial Interface	<p>Serial 0 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency</p> <p>Serial 1 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency</p> <p>UART × 2 (common use with serial 0, 1)</p> <p>I²C × 2 (single master)</p>
I/O Pins	I/O 80 • Common use : 16 (by 8 bits), 8 (by 4 bits), 56 (by bit)
A/D Inputs	8-bit × 8-ch. (with S/H)
PWM	16-bit × 2-ch.
Notes	Burst ROM interface support, ATC (between serial 0ch and internal RAM) support

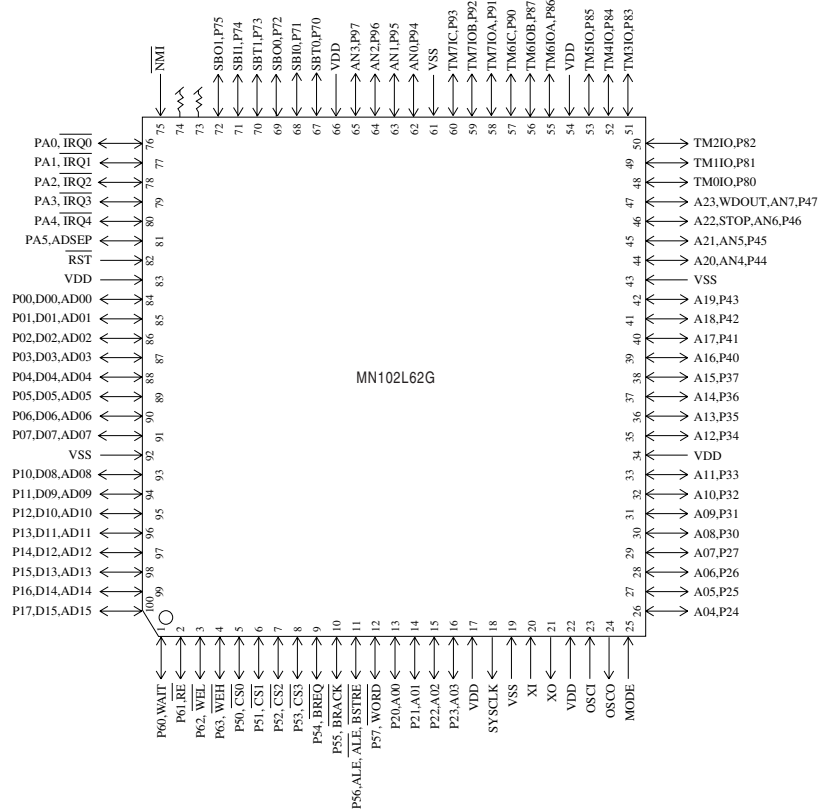
Electric Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 20 MHz, VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 20 MHz, VDD = 5.0 V, output open			30	mA

(Ta = -40°C to +85°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

See the next page for support tool.

Support Tool

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L25-LQFP100-P-1414	
EPROM Built-in Type	Type	MN102LP25G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	5 K
	Minimum instruction execution time	100 ns (4.5 V to 5.5 V , 20 MHz)
	Package	LQFP100-P-1414 *Lead-free
Flash Memory Built-in Type	Type	MN102LF25Z
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	3 K
	Minimum instruction execution time	100 ns (4.5 V to 5.5 V , 20 MHz)
	Package	LQFP100-P-1414 *Lead-free

□ MN102L490A

Type	MN102L490A	
ROM (×8-bit)	External	
RAM (×8-bit)	3 K	
Package	LQFP100-P-1414 *Lead-free	
Minimum Instruction Execution Time	With Main Clock operated	100 ns (at 4.5 V to 5.5 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer counter 0 to 5 • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 4 • Serial ch.0, 1 transmission • Serial ch.0, 1 reception • NMI pin • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (timer output, event count, A/D conversion start up) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 to 3 : 8-bit × 1 (timer output, event count, UART baud rate generator) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source underflow of timer counter 2, 3</p> <p>Timer counter 4, 5 : 8-bit × 1 (timer output, event count) Clock source 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source underflow of timer counter 4, 5</p> <p>Timer counter 6, 7 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7</p> <p style="text-align: center;">(Connectable) timer counter 0 to 5</p>	
Serial Interface	<p>Serial 0 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency</p> <p>Serial 1 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency</p> <p>UART × 2 (common use with serial 0, 1)</p> <p>I²C × 2 (single master)</p>	
I/O Pins	I/O	48 • Common use : 8 (by 4 bits), 40 (by bit)
A/D Inputs	8-bit × 8-ch. (with S/H)	
PWM	16-bit × 2-ch.	
Notes	Burst ROM interface support; ATC (between serial 0ch and internal RAM) support; Main pin inputs : TTL level	

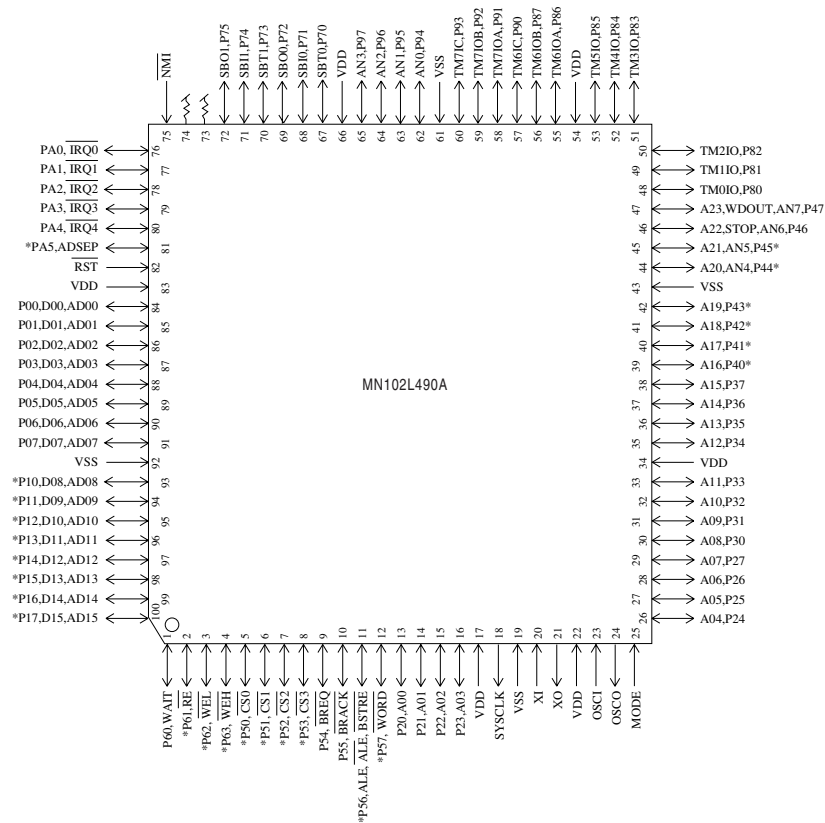
Electric Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 20 MHz, VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	µA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 20 MHz, VDD = 5.0 V, output open			30	mA

(Ta = -40°C to +85°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use of these ports are disabled

Support Tool

In-circuit Emulator

PX-ICE102L00 + PX-PRB102L49-LQFP100-P-1414

MN102L610B

Type	MN102L610B						
ROM (×8-bit)	External						
RAM (×8-bit)	4 K						
Package	LQFP100-P-1414 *Lead-free						
Minimum Instruction Execution Time	88.5 ns (at 4.5 V to 5.5 V, 22.6 MHz)						
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer counter 0 to 5 • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 4 • Serial ch.0, 1 transmission • Serial ch.0, 1 reception • NMI pin • A/D conversion finish 						
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (timer output, event count, A/D conversion start up) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 to 3 : 8-bit × 1 (timer output, event count, UART baud rate generator) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source underflow of timer counter 2, 3</p> <p>Timer counter 4, 5 : 8-bit × 1 (timer output, event count) Clock source 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source underflow of timer counter 4, 5</p> <p>Timer counter 6, 7 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7</p> <p>Connectable timer counter 0 to 5</p>						
Serial Interface	<p>Serial 0 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency</p> <p>Serial 1 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency</p> <p>UART × 2 (common use with serial 0, 1)</p> <p>I²C × 2 (single master)</p>						
I/O Pins	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">I/O</th> <th style="width: 85%;">I/O</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">80</td> <td>• Common use : 16 (by 8 bits), 8 (by 4 bits), 56 (by bit)(MN102LF61G)</td> </tr> <tr> <td style="text-align: center;">48</td> <td>• Common use : 8 (by 4 bits), 40 (by bit)(MN102L610B)</td> </tr> </tbody> </table>	I/O	I/O	80	• Common use : 16 (by 8 bits), 8 (by 4 bits), 56 (by bit)(MN102LF61G)	48	• Common use : 8 (by 4 bits), 40 (by bit)(MN102L610B)
I/O	I/O						
80	• Common use : 16 (by 8 bits), 8 (by 4 bits), 56 (by bit)(MN102LF61G)						
48	• Common use : 8 (by 4 bits), 40 (by bit)(MN102L610B)						
A/D Inputs	8-bit × 8-ch. (with S/H)						
PWM	16-bit × 2-ch.						
Special Ports	LED drive port × 2						
Notes	Burst ROM interface support, ATC (between serial 0ch and internal RAM) support						

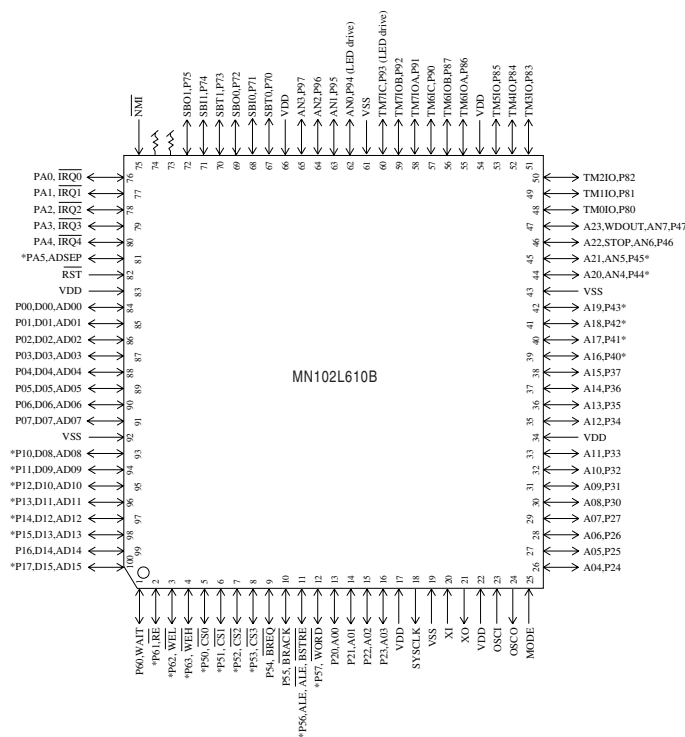
Electrical Characteristics

A/D characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D conversion relative error		VDD = 5 V , VSS = 0 V	ch.0 to 3		±3	LSB
			ch.4 to 7		±4	
A/D conversion time			4.248			μs
Analog input voltage	VIA		VSS		VDD	V

(Ta = 25°C , VDD = 5.0 V , VSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Port unusable in MN102L610B

* The MN102LF61G is manufactured and sold under license agreement with BULL CP8 Inc. Note that MN102LF61G cannot be used as the IC card.

Support Tool

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L53-LQFP100-P-1414	
Flash Memory Built-in Type	Type	MN102LF61G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	88.5 ns (at 4.5 V to 5.5 V, 22.6 MHz)
	Package	LQFP100-P-1414 *Lead-free

□ MN102H60G, MN102H60K

Type	MN102H60G	MN102H60K
ROM (x8-bit)	128 K	256 K
RAM (x8-bit)	4 K	10 K
Package	LQFP100-P-1414 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)
Interrupts	<ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin • Watchdog • $\overline{\text{NMI}}$ pin • Timer counter 0 to 7 underflow • Timer counter 8 to 12 underflow • Timer counter 8 to 12 compare capture A • Timer counter 8 to 12 compare capture B • ATC ch.0 to 3 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 4 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (prescaler, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; 1/4 of system clock (XI) frequency; system clock (BOSC); TM0IO pin Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1 (A/D conversion start up, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1 (prescaler, serial clock generator, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM4IO pin Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; system clock (BOSC) Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 8-bit × 1 (timer interrupts) Clock source 1/4 of system clock (XI) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 8-bit × 1 (timer output, event count, timer interrupts) Clock source 1/4 of system clock (XI) frequency; underflow of timer counter 0; TM7IO pin Interrupt source underflow of timer counter 7</p> <p>Connectable timer counter 0 to 7</p> <p>Timer counter 8 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM8IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM8IOA pin/TM8IOB pin (1 ×, 4 ×); TM8IC pin Interrupt source underflow of timer counter 8; timer counter 8 compare capture A; timer counter 8 compare capture B</p>	

Timer Counter (Continue)	Timer counter 9 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 0, 4; TM9IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM9IOA pin/TM9IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 9; timer counter 9 compare capture A; timer counter 9 compare capture B
	Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 0, 4; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B
	Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 0, 4; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B
	Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 0, 4; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×), TM12IOB pin
	Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B
	Timer counter 13, 14 : 8-bit × 1 (simple PWM output)
	Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0
	Timer counter 15 : 16-bit × 1 (pulse width measurement)
Clock source system clock (BOSC); 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM15IB pin	
Connectable timer counter 13, 14	

Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 1 underflow frequency; 1/8, 1/2 of timer counter 2 underflow frequency; external pin
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 4 underflow frequency; 1/8, 1/2 of timer counter 5 underflow frequency; external pin
	Serial 4 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 1 underflow frequency; 1/8, 1/2 of timer counter 5 underflow frequency; external pin
	UART × 2 (common use with serial 3, 4)
I ² C × 2 (common use with serial 3,4; single master)	

I/O Pins	I/O	82	• Common use : 46 (address data separate 8-bit mode) • Common use : 53 (address data multiplex 8-bit mode)
A/D Inputs		10-bit × 8-ch. (with S/H)	
PWM		16-bit × 5-ch. (timer counter 8 to 12)	
ICR		16-bit × 5-ch. (timer counter 8 to 12)	
OCR		16-bit × 5-ch. (timer counter 8 to 12)	
Notes		Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable	

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz, VDD = 3.3 V			60+10 α *	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open All other input pins and Hi-Z state input/output			70	μ A
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 34 MHz, VDD = 3.3 V, output open			30+10 α *	mA

(Ta = -40°C to +85°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

* "α" depends on products.

MN102H60G, MN102H60K : α = 0

MN102HF60G : α = 1

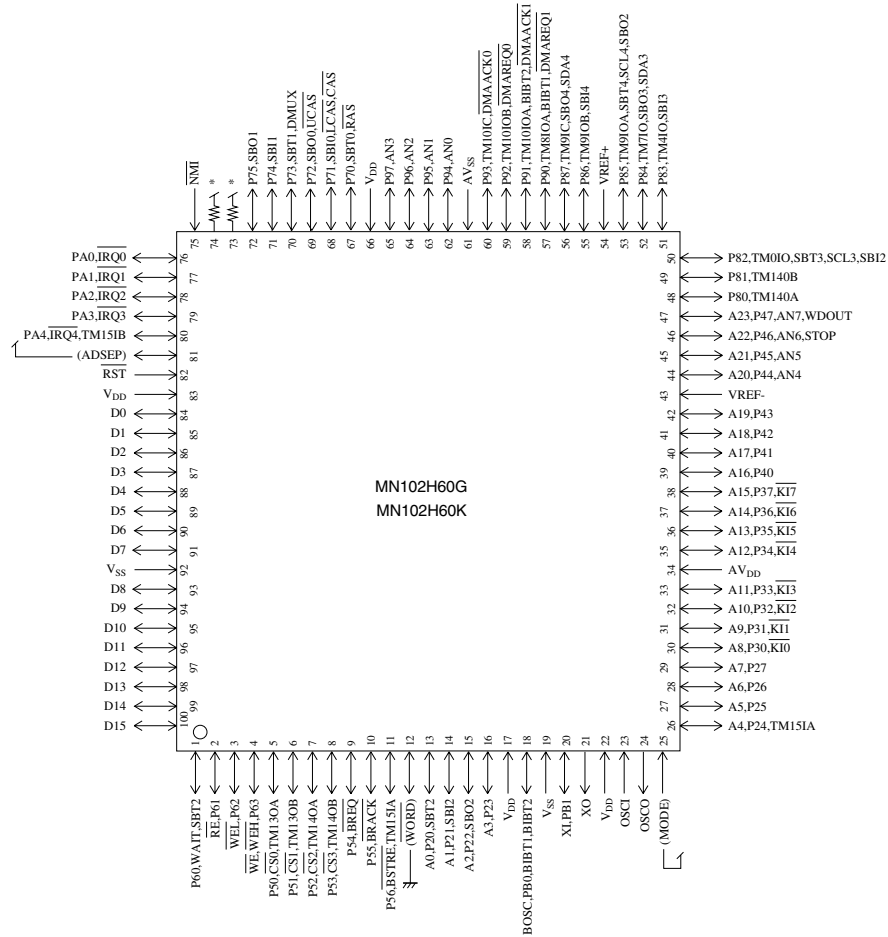
MN102HF60K : α = 2

A/D characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Non-linear error		10-bit			\pm 4	LSB
A/D conversion time		at 34 MHz	3.29			μ s
Analog input voltage	VIA		VSS		VDD	V

(Ta = 25°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use 33 kΩ to 50 kΩ.

* Pin position in 16-bit bus width address data split memory extension mode.

Support Tool

In-circuit Emulator	PX-ICE102H60-LQFP100-P-1414	
Flash Memory Built-in Type	Type	MN102HF60G, MN102HF60K
	ROM (× 8-bit)	128 K / 256 K
	RAM (× 8-bit)	4 K / 10 K
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)
	Package	LQFP100-P-1414 *Lead-free

□ MN1021617

Type	MN1021617	
ROM (x8-bit)	128 K	
RAM (x8-bit)	4 K	
Package	LQFP128-P-1818C *Lead-free, FLGA165-C-1111 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	50 ns (at 3.0 V to 3.6 V, 40 MHz) 100 ns (at 2.0 V to 3.6 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin • Watchdog • NMI pin • Timer counter 4 to 15 • Timer counter 16, 17, 21 • Timer counter 16 to 20 compare capture A • Timer counter 16 to 20 compare capture B • Timer counter 21 capture A • Timer counter 21 capture B • Timer counter 21 capture D • Timer counter 21 compare E • Timer counter 21 compare F • ATC ch.0 to 3 transfer finish • External 0 to 7 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (prescalers) Clock source 1/2 of system clock frequency; timer counter 1 output</p> <p>Timer counter 1 : 8-bit × 1 (prescalers) Clock source 1/2 of system clock frequency; timer counter 0 output</p> <p>Timer counter 2 : 8-bit × 1 (UART baud rate generator) Clock source 1/2 of system clock frequency; timer counter 0 output</p> <p>Timer counter 3 : 8-bit × 1 (UART baud rate generator) Clock source 1/2 of system clock frequency; timer counter 0 output; external clock input</p> <p>Timer counter 4 : 8-bit × 1 (timer output, A/D conversion start up) Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output Interrupt source underflow of timer counter 4</p> <p>Timer counter 5, 9 : 8-bit × 1 (UART baud rate generator) Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output Interrupt source underflow of timer counter 5, 9</p> <p>Timer counter 6, 10, 11 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output Interrupt source underflow of timer counter 6, 10, 11</p> <p>Timer counter 7 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output Interrupt source underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source underflow of timer counter 8</p> <p>Timer counter 12 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0 output; timer counter 1 output Interrupt source underflow of timer counter 12</p> <p>Timer counter 13 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output Interrupt source underflow of timer counter 13</p> <p>Timer counter 14 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0 output Interrupt source underflow of timer counter 14</p>	

Timer Counter (Continue)	<p>Timer counter 15 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0 output Interrupt source underflow of timer counter 15</p> <p>Connectable timer counter 0 to 3, 4 to 7, 8 to 11, 12 to 15</p> <p>Timer counter 16, 17 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input (with edge, timer counter 17 only); timer counter 0 output; timer counter 1 output (timer counter 16 only) Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 16, 17</p> <p>Timer counter 18 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 18, 19, 20</p> <p>Timer counter 19, 20 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock; timer counter 0 output; timer counter 1 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 18, 19, 20</p> <p>Timer counter 21 : 24-bit × 1 (servo control) Clock source 1/2 of system clock frequency; timer counter 1 output Interrupt source when capturing to capture A; when capturing to capture B; when capturing to capture D; when coinciding to compare E; when coinciding to compare F</p>
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Serial Interface	<p>Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 2 frequency; 1/8, 1/2 of timer counter 5 frequency; external clock</p> <p>Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 3 frequency; 1/8, 1/2 of timer counter 9 frequency; external clock</p> <p>UART × 4 (common use with serial 0 to 3)</p> <p>I²C × 2 (common use with serial 1, 3; single master)</p>
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I/O Pins	I/O	100	• Common use : 56 (address data separate 8-bit mode) • Common use : 73 (address data multiplex 8-bit Mode)
	Input	8	• Common use : 8

A/D Inputs	10-bit × 12-ch. (maximum input is 16) (with S/H)
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PWM	16-bit × 5-ch. (timer counter 16 to 20)
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ICR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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OCR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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Notes	Address / data multiplex bus Interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable
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See the next page for electrical characteristics, pin assignment and support tool.

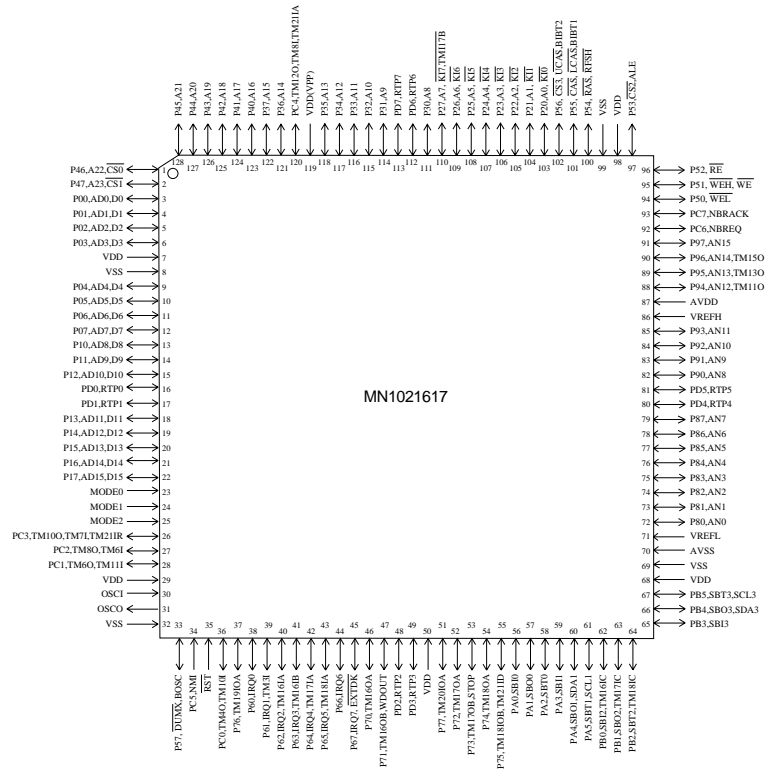
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 40 MHz, VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 40 MHz, VDD = 3.3 V, output open			25	mA

(Ta = -20°C to +70°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP128-P-1818C *Lead-free

Pin Assignment (Continue)

Perspective



N.D.	N.D.	PB5,SBT3, SCL3	AVDD	P81,AN1	P83,AN3	P87,AN7	AVDD	P94,AN12, TM110	AVDD	P50,WEL	N.D.	N.D.	N
N.D.	N.D.	PB3,SB13	VSS	VREFL	P85,AN5	PD5, RTP5	P93,AN11	P96,AN14, TM150	PC6,NBREQ	P52,/RE	N.D.	N.D.	M
VSS	PB2,SBT2, TM181C	PB1,SBO2, TM171C	PB4,SBO3, SDA3	P80,AN0	P84,AN4	AVSS	P91,AN9	P95,AN13, TM130	PC7, NBRACK	P51,/WEH, /WE	VDD	P54,/RAS, /RFSH	L
PB0,SB12, TM161C	PA4,SBO1, SDA1	PA5,SBT1, SCL1	VDD	AVSS	P86,AN6	P90,AN8	P92,AN10	P97,AN15	VSS	P53,/CS2, ALE	P56,/CS3, /UCAS, BIBT2	VDD	K
PA1,SBO0	PA3,SB11	PA0,SB10	PA2,SBT0	AVSS	P82,AN2	PD4, RTP4	VREFH	P55,/CAS, /LCAS, BIBT1	VPP	P20,A0,/K10	P21,A1,/K11	P23,A3,/K13	J
P75, TM181OB, TM211D	P73, TM170B, STOP	P77, TM201OA	P72, TM170A	P74, TM180A	N.D.	N.D.	N.D.	P22,A2,/K12	P26,A6,/K16	P24,A4,/K14	P27,A7,/K17, TM117B	P25,A5,/K15	H
P71, TM160B, WDOUT	PD3, RTP3	VDD	VDD	PD2, RTP2	N.D.	N.D.	N.D.	P30,A8	PD7, RTP7	VPP	P31,A9	PD6, RTP6	G
P65,IRQ5, TM 181A	P67,IRQ7,/EX TDK	P66,IRQ6	P70, TM160A	P64,IRQ4, TM171A	N.D.	N.D.	N.D.	P34,A12	P32,A10	P33,A11	P35,A13	PC4, TM120, TM81, TM211A	F
P63,IRQ3, TM161B	P61,IRQ1, TM31	P62,IRQ2, TM161A	VDD	P60,IRQ0	MODE0	PD0, RTP0	P05,AD5,D5	P03,AD3,D3	P36,A14	VPP	P41,A17	P37,A15	E
VSS	P76, TM191OA	PC0, TM40, TM101	VDD	PC2, TM80, TM61	P15,AD13, D13	P13,AD11, D11	P11,AD9,D9	VSS	P01,AD1,D1	P42,A18	P40,A16	VDD	D
/RST	P57,/DUMX, BOSC	PC5,NMI	OSCO	MODE2	P14,AD12, D12	VSS	P07,AD7,D7	VSS	P47,A23, /CS1	P44,A20	P45,A21	P43,A19	C
N.D.	N.D.	VSS	PC1, TM60, TM111	PC3, TM100, TM71, TM211R	P16,AD14, D14	PD1, RTP1	P10,AD8,D8	VDD	P02,AD2,D2	P46,A22, /CS0	N.D.	N.D.	B
N.D.	N.D.	OSCI	VSS	MODE1	P17,AD15,D1 5	P12,AD10, D10	P06,AD6,D6	P04,AD4,D4	VDD	P00,AD0,D0	N.D.	N.D.	A

FLGA165-C-1111 *Lead-free

The MN102F1617 is manufactured and sold under license agreement with BULL CP8 Inc. Note that MN102F1617 cannot be used as the IC card.

* A1 has no electrode (pin).

* N.D. (not defined) has an electrode (pin) but not guaranteed for N.C. (not connected). Pay sufficient attention so as not to cause shorting with any other wiring on the user board.

* VPP, VDD, VSS, AVDD and AVSS has multiple electrodes (pins). Electrodes having the same name are shorted internally.

Support Tool

In-circuit Emulator	PX-ICE102H1617-LQFP128-P-1818C	Not applicable to FLGA165-C-1111.	
	Minimum instruction execution time	57.1 ns (at 35 MHz)	
Flash Memory Built-in Type	Type	MN102F1617	
	ROM (× 8-bit)	128 K	
	RAM (× 8-bit)	4 K	
	Minimum instruction execution time		62.5 ns (at 3.0 V to 3.6 V, 32 MHz)
			83.3 ns (at 2.7 V to 3.6 V, 24 MHz)
Package	LQFP128-P-1818C *Lead-free, FLGA165-C-1111 *Lead-free		

□ MN102H460B

Type	MN102H460B	
ROM (x8-bit)	External	
RAM (x8-bit)	4 K	
Package	LQFP128-P-1818C *Lead-free, TQFP128-P-1414B *Lead-free	
Minimum Instruction Execution Time	With main clock operated	50 ns (at 3.0 V to 3.6 V, 40 MHz)
		100 ns (at 2.0 V to 3.6 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin • Watchdog • NMI pin • Timer counter 4 to 15 • Timer counter 16, 17, 21 • Timer counter 16 to 20 compare capture A • Timer counter 16 to 20 compare capture B • Timer counter 21 capture A • Timer counter 21 capture B • Timer counter 21 capture D • Timer counter 21 compare E • Timer counter 21 compare F • ATC ch.0 to 3 transfer finish • External 0 to 7 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish 	
Timer Counter	Timer counter 0 : 8-bit × 1 (prescalers)	
	Clock source	1/2 of system clock frequency; timer counter 1 output
	Timer counter 1 : 8-bit × 1 (prescalers)	
	Clock source	1/2 of system clock frequency; timer counter 0 output
	Timer counter 2, 3 : 8-bit × 1 (UART baud rate generator)	
	Clock source	1/2 of system clock frequency; external clock input; timer counter 0 output
	Timer counter 4 : 8-bit × 1 (timer output, A/D conversion start up)	
	Clock source	1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output
	Interrupt source	underflow of timer counter 4
	Timer counter 5, 9 : 8-bit × 1 (UART baud rate generator)	
	Clock source	1/2 of system clock frequency; timer counter 0 output; timer counter 1 output
	Interrupt source	underflow of timer counter 5, 9
	Timer counter 6, 10, 11 : 8-bit × 1 (timer output)	
	Clock source	1/2 of system clock frequency; external clock input; timer counter 0 output
Interrupt source	underflow of timer counter 6, 10, 11	
Timer counter 7 : 8-bit × 1 (timer output)		
Clock source	1/2 of system clock frequency; external clock input; timer counter 0 output	
Interrupt source	underflow of timer counter 7	
Timer counter 8 : 8-bit × 1 (timer output)		
Clock source	1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output	
Interrupt source	underflow of timer counter 8	
Timer counter 12 : 8-bit × 1 (timer output)		
Clock source	1/2 of system clock frequency; external clock input with edge; timer counter 0 output; timer counter 1 output	
Interrupt source	underflow of timer counter 12	
Timer counter 13 : 8-bit × 1 (timer output)		
Clock source	1/2 of system clock frequency; timer counter 0 output; timer counter 1 output	
Interrupt source	underflow of timer counter 13	
Timer counter 14 : 8-bit × 1 (timer output)		
Clock source	1/2 of system clock; external clock input with edge; timer counter 0 output	
Interrupt source	underflow of timer counter 14	

Timer Counter (Continue)	Timer counter 15 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0 output Interrupt source underflow of timer counter 15
	Connectable timer counter 0 to 3, 4 to 7, 8 to 11, 12 to 15
	Timer counter 16, 17 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input (with edge, timer counter 17 only); timer counter 0 output; timer counter 1 output (timer counter 16 only) Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 16, 17
	Timer counter 18, 19, 20: 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 18, 19, 20
	Timer counter 21 : 24-bit × 1 (servo control) Clock source 1/2 of system clock frequency; timer counter 1 output Interrupt source when capturing to capture A; when capturing to capture B; when capturing to capture D; when coinciding to compare E; when coinciding to compare F

Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 2; 1/8, 1/2 of timer counter 5; external clock
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 3; 1/8, 1/2 of timer counter 9; external clock
	UART × 4 (common use with serial 0 to 3) I ² C × 2 (common use with serial 1, 3; single master)

I/O Pins	I/O	55	<ul style="list-style-type: none"> • Common use : 55 (use of full address, address data separate 16-bit mode) • Common use : 72 (use of address 16-bit, address data multiplex 16-bit mode)
	Input	8	<ul style="list-style-type: none"> • Common use : 8

A/D Inputs	10-bit × 12-ch. (maximum input is 16) (with S/H)
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PWM	16-bit × 5-ch. (timer counter 16 to 20)
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ICR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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OCR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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Notes	Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable
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See the next page for electrical characteristics, pin assignment and support tool.

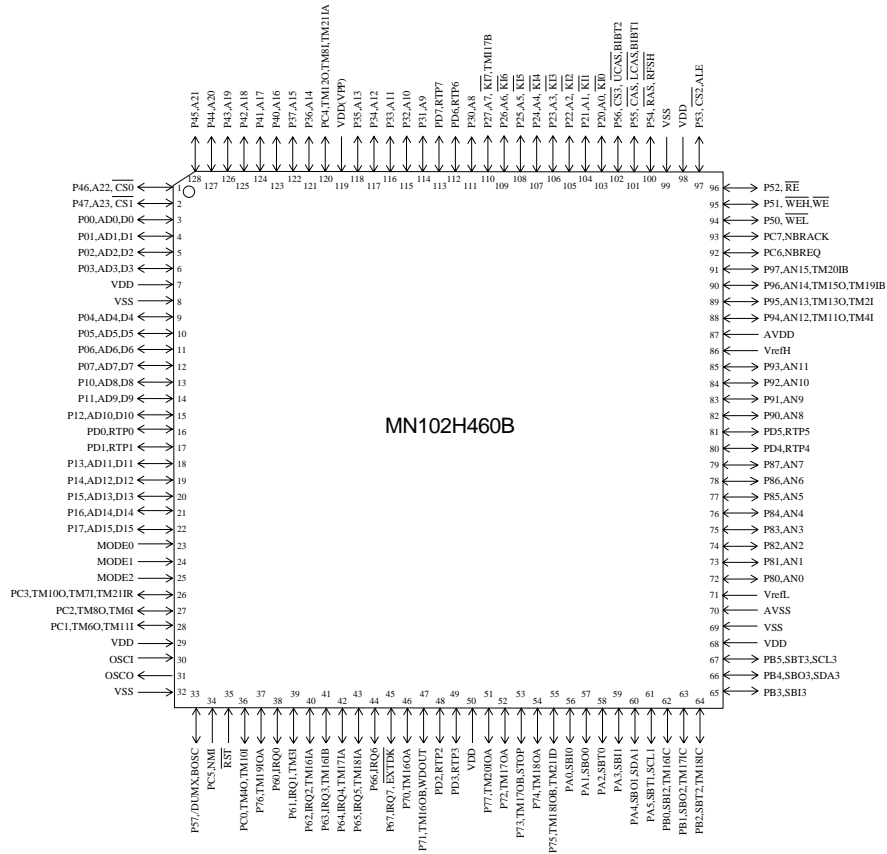
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 40 MHz , VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 40 MHz , VDD = 3.3 V, output open			25	mA

(Ta = -20°C to +70°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

Pin Assignment



LQFP128-P-1818C *Lead-free

TQFP128-P-1414B *Lead-free

Support Tool■ **In-circuit Emulator**

PX-ICE102H46-LQFP128-P-1818C
PX-ICE102H46-TQFP128-P-1414B

Minimum instruction execution time 57.1 ns (at 30 MHz)

□ MN102L360C

Type	MN102L360C	
ROM (×8-bit)	External	
RAM (×8-bit)	5 K	
Package	LQFP128-P-1818C *Lead-free	
Minimum Instruction Execution Time	100 ns (at 4.5 V to 5.5 V, 20 MHz)	
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer counter 0 to 5 • Fixed-length serial ch.0,1 transmission • Fixed-length serial ch.0,1 reception • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 7 • Serial ch.0,1 transmission • Serial ch.0,1 reception • NMI pin • A/D conversion finish 	
Timer Counter	<p>Timer counter 0: 8-bit × 1 (timer output, event count) Clock source 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source timer counter 0 underflow</p> <p>Timer counter 1: 8-bit × 1 (timer output, even count, A/D conversion start) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source timer counter 1 underflow</p> <p>Timer counter 2 to 3: 8-bit × 1 (timer output, event count, UART baud rate generation) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source timer counter 2, 3 underflow</p> <p>Timer counter 4,5: 8-bit × 1 (timer output, event count) Clock source 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source timer counter 4, 5 underflow</p> <p>Timer counter 6, 7: 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7</p> <p style="text-align: center;">(Connectable) timer counter 0 to 5</p>	
Serial Interface	<p>Serial 0: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency I²C mode (master transmission/reception is possible in the master system.)</p> <p>Serial 1: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency I²C mode (master transmission/reception is possible in the single master system.)</p> <p>Fixed-length serial 0: 8-bit × 1 Clock source external clock Sending direction LSB</p> <p>Fixed-length serial 1: 8-bit × 1 Clock source external clock Sending direction LSB</p>	
I/O Pins	I/O	83 • Common use: 8 (by 4 bits), 75 (by bit)
A/D Inputs	8-bit × 8-ch. (with S/H)	

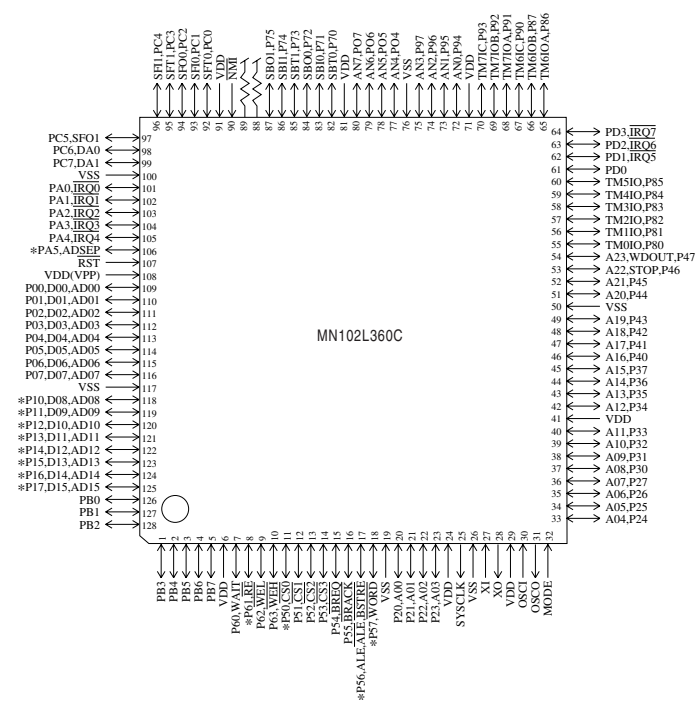
D/A Outputs	8-bit × 2-ch.
PWM	16-bit × 2-ch.
Notes	Burst ROM interface support, ATC (between serial 0 ch and built-in RAM) support

Electric Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 20 MHz , VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 20 MHz , VDD = 5.0 V, output open			30	mA

(Ta = -40°C to +85°C , VDD = 5.0 V , VSS = 0 V)

Pin Assignment



LQFP128-P-1818C *Lead-free
* Port unusable

See the next page for support tool.

Support Tool

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L36-LQFP128-P-1818C	
EPROM Built-in Type	Type	MN102LP36Z
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	10 K
	Minimum instruction execution time	100 ns (at 4.5 V to 5.5 V, 20 MHz)
	Package	LQFP128-P-1818C *Lead-free

MN102L360C □

□ MN102H55G

Type	MN102H55G	
ROM (x8-bit)	128 K	
RAM (x8-bit)	4 K	
Package	LQFP100-P-1414 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)
Interrupts	<ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin • Watchdog • NMI pin • Timer counter 0 to 7 underflow • Timer counter 8 to 12 underflow • Timer counter 8 to 12 compare capture A • Timer counter 8 to 12 compare capture B • ATC ch.0 to 3 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 4 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (prescaler, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; 1/4 of system clock (XI) frequency; system clock (BOSC); TM0IO pin Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1 (A/D conversion start, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1 (serial clock generator, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM4IO pin Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; system clock (BOSC) Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 8-bit × 1 (timer interrupts) Clock source 1/4 of system clock (XI) frequency; underflow of timer counter 0, 4 Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 8-bit × 1 (timer output, event count, timer interrupts) Clock source 1/4 of system clock (XI) frequency; underflow of timer counter 0; TM7IO pin Interrupt source underflow of timer counter 7</p> <p>Connectable timer counter 0 to 7</p> <p>Timer counter 8 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM8IB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM8IA pin/TM8IB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 8; timer counter 8 compare capture A; timer counter 8 compare capture B</p>	

Timer Counter (Continue)	<p>Timer counter 9 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM9IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM9IA pin/TM9IB pin (1 ×, 4 ×); TM9IC pin Interrupt source underflow of timer counter 9; timer counter 9 compare capture A; timer counter 9 compare capture B</p> <p>Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM10IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM10IA pin/TM10IB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B</p> <p>Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM11IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM11IA pin/TM11IB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B</p> <p>Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 0, 4; TM12IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM12IA pin/TM12IB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B</p> <p>Timer counter 13, 14 : 8-bit × 2 (simple PWM output) Clock source 1/2 of system clock (BOSC); underflow of timer counter 0</p> <p>Timer counter 15 : 16-bit × 1 (pulse width measurement) Clock source system clock (BOSC); 1/2 of system clock (BOSC); underflow of timer counter 0; TM15IB pin</p>
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Serial Interface	<p>Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 1 underflow; 1/8, 1/2 of timer counter 2 underflow; external pin</p> <p>Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 4 underflow; 1/8, 1/2 of timer counter 5 underflow; external pin</p> <p>Serial 4 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 1 underflow; 1/8, 1/2 of timer counter 5 underflow; external pin</p> <p>UART × 2 (common use with serial 3, 4)</p> <p>I²C × 2 (common use with serial 3,4; single master)</p>
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I/O Pins	I/O	82 • Common use : 46 (address data separate 8-bit mode) • Common use : 53 (address data multiplex 8-bit mode)
A/D Inputs		10-bit × 8-ch. (with S/H)
D/A Outputs		8-bit × 2-ch.
PWM		16-bit × 5-ch. (timer counter 8 to 12)
ICR		16-bit × 5-ch. (timer counter 8 to 12)
OCR		16-bit × 5-ch. (timer counter 8 to 12)
Notes		Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable

See the next page for electrical characteristics, pin assignment and support tool.

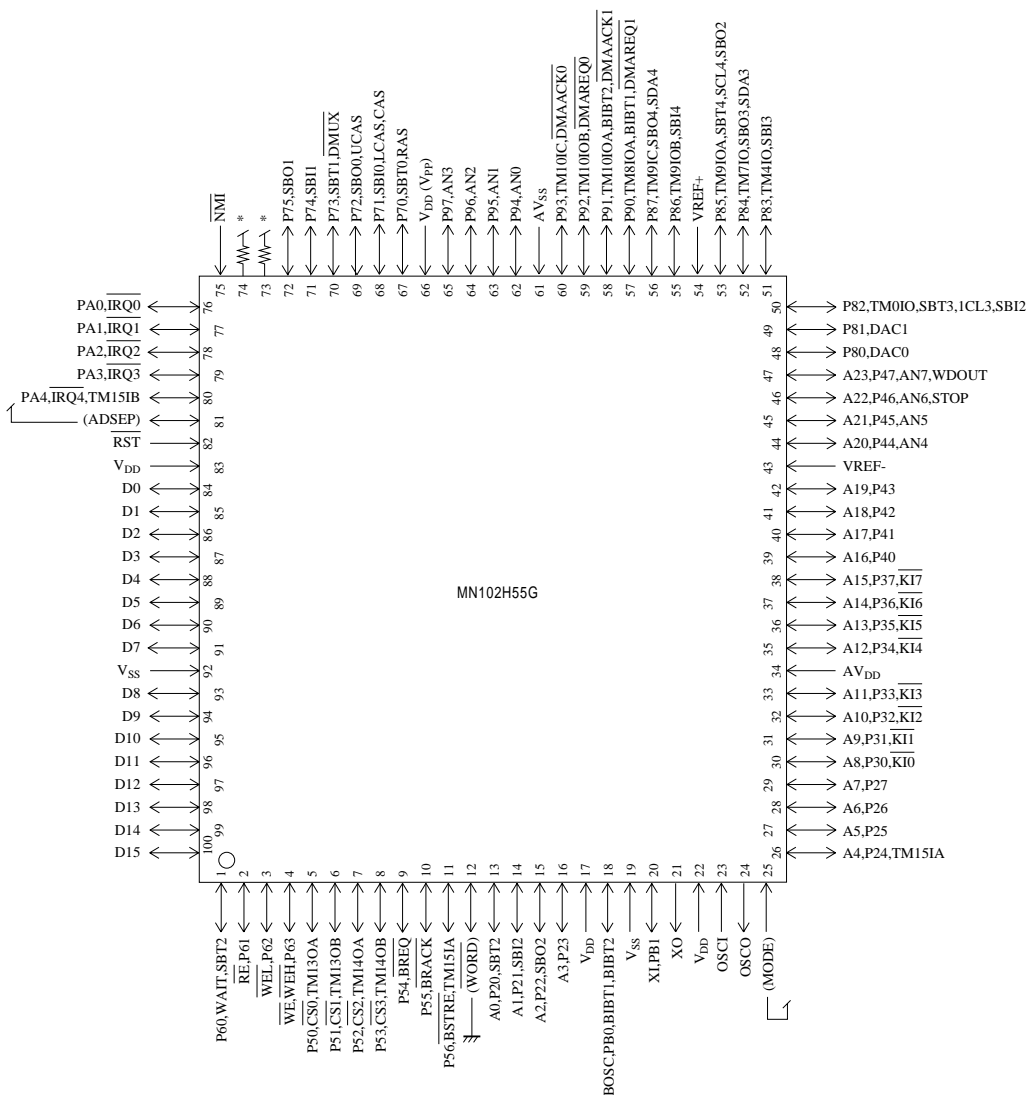
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz, VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level			70	μA
Supply current at HALT	IDDH	f = 34 MHz, VDD = 3.3 V, output open			23	mA

(Ta = -40°C to +85°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use 33 kΩ to 50 kΩ

* Pin position in 16-bit bus width address data split memory extension mode.

Support Tool

In-circuit Emulator	PX-ICE102H55-LQFP100-P-1414	
Flash Memory Built-in Type	Type	MN102HF55G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	66.6 ns (at 3.0 V to 3.6 V, 30 MHz)
	Package	LQFP100-P-1414 *Lead-free

□ MN102H730F , MN102H73G , MN102H73K

Type	MN102H730F	MN102H73G	MN102H73K
ROM (x8-bit)	External	128 K	256 K
RAM (x8-bit)	10 K	10 K	12 K
Package	TQFP128-P-1414B *Lead-free	TQFP128-P-1414A *Lead-free	
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)	
Interrupts	<ul style="list-style-type: none"> • RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B • ATC ch.0 to 1 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 7 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • A/D conversion finish 		
Timer Counter	<p>Timer counter 0 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM0IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM1IO pin; timer counter 0 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM2IO pin; timer counter 1 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM3IO pin; timer counter 2 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM4IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM5IO pin; timer counter 4 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM6IO pin; timer counter 5 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM7IO pin; timer counter 6 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; system clock (BOSC); 1/4 of system clock (XI) frequency; TM8IO pin</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 8</p>		

Timer Counter (Continue)	Timer counter 9 : 8-bit × 1
	Clock source 1/2 of system clock (BOSC) frequency; 1/64 of system clock (BOSC) frequency; TM9IO pin; timer counter 8 output
	Interrupt source underflow of timer counter 9
	Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B
Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)	
Clock source underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×)	
Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B	
Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)	
Clock source underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×)	
Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B	
Timer counter 13 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)	
Clock source underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin (1 ×, 4 ×)	
Interrupt source underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B	
Timer counter 14 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)	
Clock source underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin (1 ×, 4 ×)	
Interrupt source underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture B	

Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 6 underflow frequency; 1/8, 1/2 of timer counter 0 underflow frequency; external pin
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
Clock source 1/8 of timer counter 2 underflow frequency; 1/8, 1/2 of timer counter 4 underflow frequency; external pin	
UART × 4 (common use with serial 0 to 3)	
I ² C × 2 (common use with serial 1,3; single master)	

Multiply-and-Accumulate	16-bit sign × 16-bit sign + 40-bit sign	
I/O Pins	I/O	104 <ul style="list-style-type: none"> • Common use : 59 (use of full address, address data separate 16-bit mode) • Common use : 76 (use of address 16-bit, address data separate 8-bit mode)
A/D Inputs	10-bit × 12-ch. (with S/H)	
D/A Outputs	8-bit × 4-ch.	
PWM	16-bit × 5-ch. (timer counter 10 to 14)	
ICR	16-bit × 5-ch. (timer counter 10 to 14)	
OCR	16-bit × 5-ch. (timer counter 10 to 14)	
Notes	Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface	

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz , VDD = 3.3 V			60+10 α *	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			70	μ A
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open			30+10 α *	mA

(Ta = -40°C to +85°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

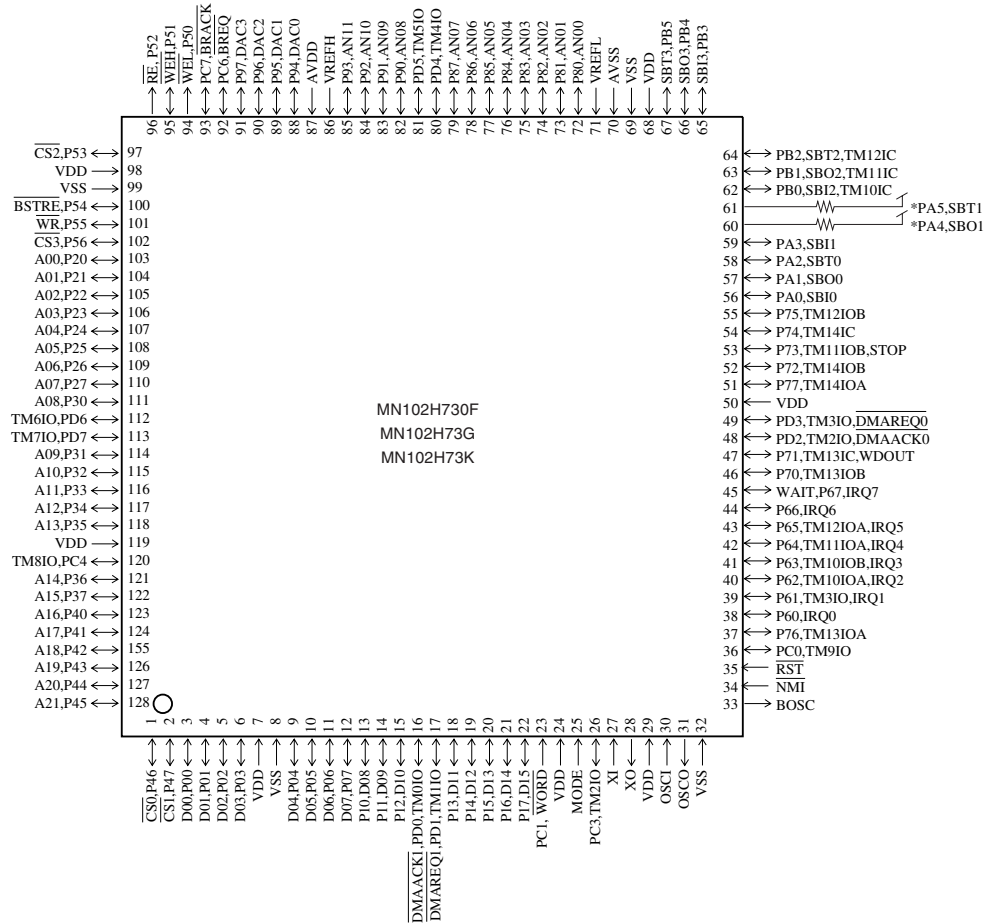
* "α" depends on products .

MN102H73G/73K/730F $\alpha = 0$

MN102HF73G $\alpha = 1$

MN102HF73K $\alpha = 2$

Pin Assignment



TQFP128-P-1414A *Lead-free
 TQFP128-P-1414B *Lead-free
 * Use 4.7 kΩ to 10 kΩ.

Support Tool

In-circuit Emulator	PX-ICE102H73-128P1414	
Flash Memory Built-in Type	Type	MN102HF73G, MN102HF73K
	ROM (× 8-bit)	128 K / 256 K
	RAM (× 8-bit)	10 K / 12 K
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)
	Package	TQFP128-P-1414B *Lead-free

□ MN102H930F

Type	MN102H930F	
ROM (×8-bit)	External	
RAM (×8-bit)	10 K	
Package	LQFP100-P-1414 *Lead-free	MLGA100-L-1010 *Lead-free
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)
Interrupts	<ul style="list-style-type: none"> • RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B • ATC ch.0 to 3 transfer finish • External 0 to 4 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM0IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8, 9; timer counter 0 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM2IO pin; timer counter 1 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM3IO pin; timer counter 2 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM4IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8, 9; timer counter 4 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM6IO pin; timer counter 5 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM7IO pin; timer counter 6 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; system clock (BOSC); 1/4 of system clock (XI) frequency; TM8IO pin</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 8</p>	

Timer Counter (Continue)	<p>Timer counter 9 : 8-bit × 1 Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM9IO pin; timer counter 8 output Interrupt source underflow of timer counter 9</p> <p>Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B</p> <p>Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B</p> <p>Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B</p> <p>Timer counter 13 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B</p> <p>Timer counter 14 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture B</p>
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Serial Interface	<p>Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 6 underflow frequency; 1/8, 1/2 of timer counter 0 underflow frequency; external pin</p> <p>Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 2 underflow frequency; 1/8, 1/2 of timer counter 4 underflow frequency; external pin</p> <p>UART × 4 (common use with serial 0 to 3)</p> <p>I²C × 2 (common use with serial 1,3; single master)</p>
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I/O Pins	I/O	63	<ul style="list-style-type: none"> • Common use : 43 (use of full address, address data separate 16-bit mode) • Common use : 57 (use of address 16-bit, address data separate 8-bit mode)
A/D Inputs		10-bit × 12-ch. (with S/H)	
D/A Outputs		8-bit × 4-ch.	
PWM		16-bit × 5-ch. (timer counter 10 to 14)	
ICR		16-bit × 5-ch. (timer counter 10 to 14)	
OCR		16-bit × 5-ch. (timer counter 10 to 14)	
Notes		Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface	

See the next page for electrical characteristics, pin assignment and support tool.

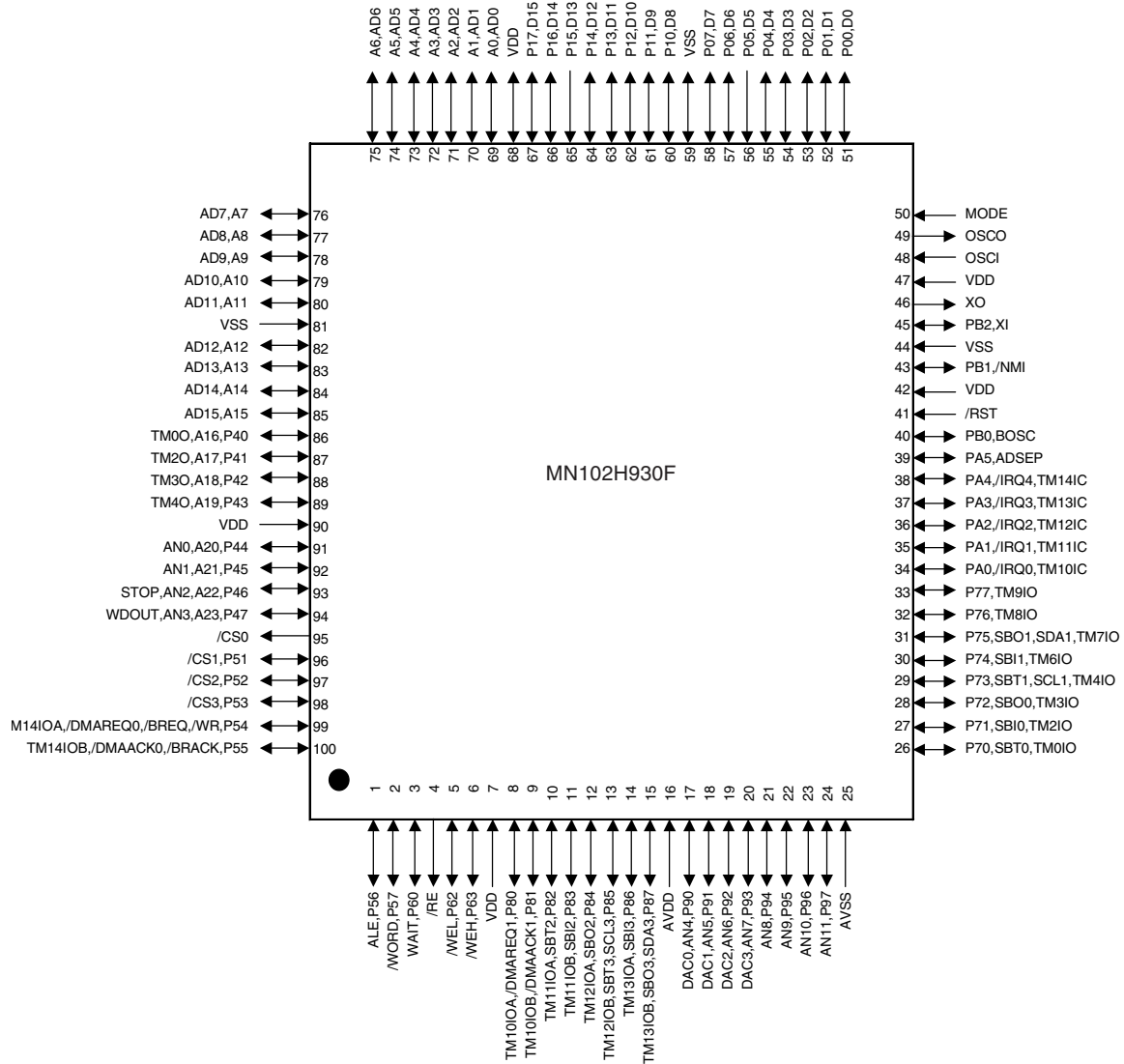
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz, VDD = 3.3 V			60	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			70	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 34 MHz, VDD = 3.3 V, output open			30	mA

(Ta = -40°C to +85°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

MLGA100-P-1010 *Lead-free

Support Tool

In-circuit Emulator

PX-ICE102H930F-LQFP100-P-1414

□ MN102H950F

Type	MN102H950F	
ROM (x8-bit)	External	
RAM (x8-bit)	10 K	
Package	LQFP100-P-1414 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)
Interrupts	<ul style="list-style-type: none"> • RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B • ATC ch.0 to 3 transfer finish • External 0 to 4 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • A/D conversion finish 	
Timer Counter	<p>Timer counter 0 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM0IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 0</p> <p>Timer counter 1 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8, 9; timer counter 0 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 1</p> <p>Timer counter 2 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM2IO pin; timer counter 1 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 2</p> <p>Timer counter 3 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM3IO pin; timer counter 2 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 3</p> <p>Timer counter 4 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM4IO pin; system clock (BOSC)</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 4</p> <p>Timer counter 5 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8, 9; timer counter 4 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 5</p> <p>Timer counter 6 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM6IO pin; timer counter 5 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 6</p> <p>Timer counter 7 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM7IO pin; timer counter 6 output</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1</p> <p style="padding-left: 20px;">Clock source 1/2 of system clock (BOSC) frequency; system clock (BOSC); 1/4 of system clock (XI) frequency; TM8IO pin</p> <p style="padding-left: 20px;">Interrupt source underflow of timer counter 8</p>	

Timer Counter (Continue)	Timer counter 9 : 8-bit × 1
	Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM9IO pin; timer counter 8 output
	Interrupt source underflow of timer counter 9
	Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B
	Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B
	Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×)
	Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B
	Timer counter 13 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
	Clock source underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin (1 ×, 4 ×)
Interrupt source underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B	
Timer counter 14 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)	
Clock source underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin (1 ×, 4 ×)	
Interrupt source underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture B	

Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 6 underflow frequency; 1/8, 1/2 of timer counter 0 underflow frequency; external pin
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)
	Clock source 1/8 of timer counter 2 underflow frequency; 1/8, 1/2 of timer counter 4 underflow frequency; external pin
	UART × 4 (common use with serial 0 to 3)
	I ² C × 2 (common use with serial 1,3; single master)

I/O Pins	I/O	63	<ul style="list-style-type: none"> • Common use : 43 (use of full address, address data separate 16-bit mode) • Common use : 57 (use of address 16-bit, address data separate 8-bit mode) • Common use : 56 (use of full address, address data separate 16-bit mode) • Common use : 63 (use of address 16-bit, address data separate 8-bit mode)

A/D Inputs	10-bit × 12-ch. (with S/H)
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D/A Outputs	8-bit × 4-ch.
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PWM	16-bit × 5-ch. (timer counter 10 to 14)
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ICR	16-bit × 5-ch. (timer counter 10 to 14)
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OCR	16-bit × 5-ch. (timer counter 10 to 14)
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Notes	Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface
	Address / data multiplex bus interface support

See the next page for electrical characteristics, pin assignment and support tool.

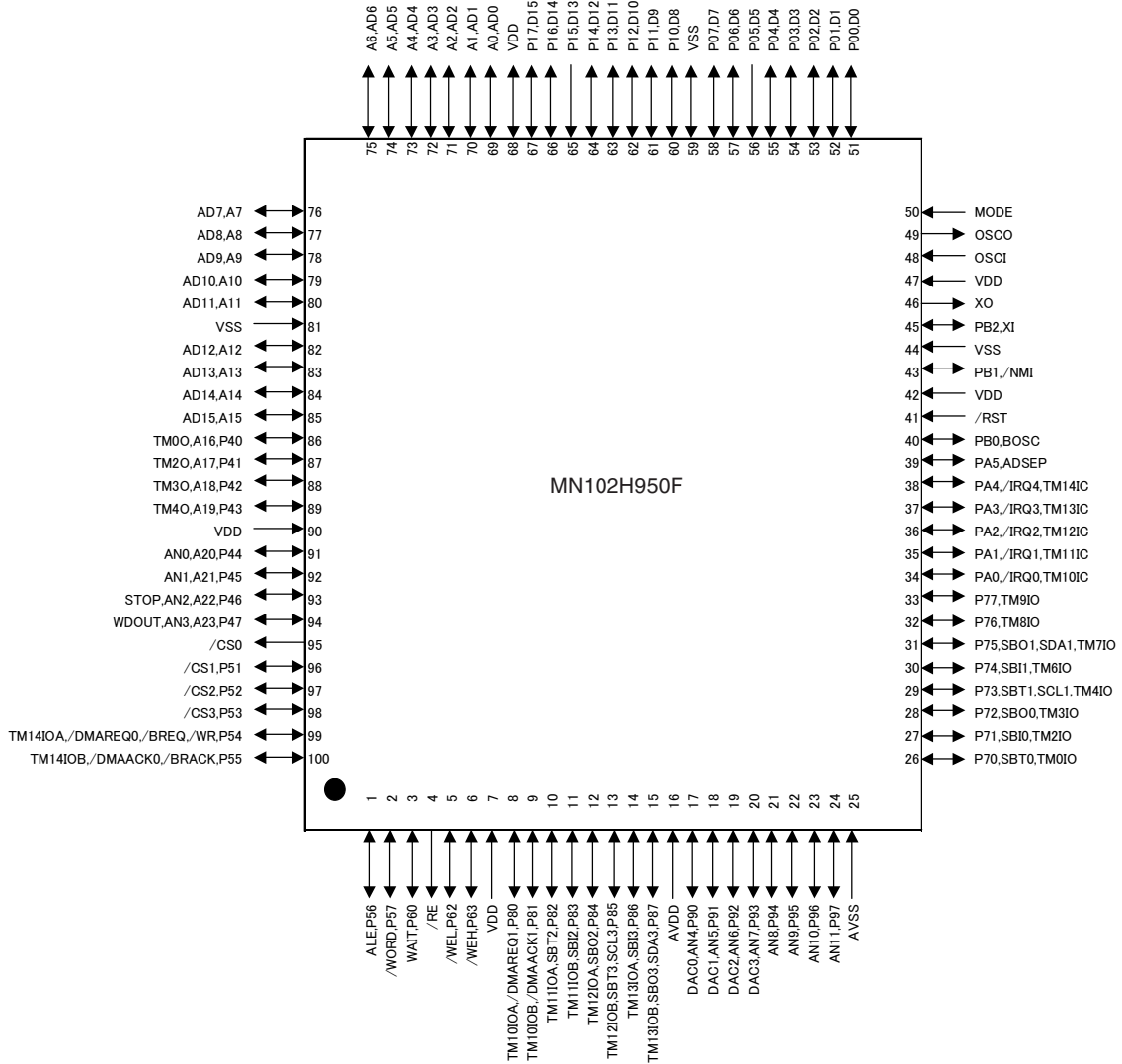
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz, VDD = 3.3 V			60	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			70	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 34 MHz, VDD = 3.3 V, output open			30	mA

(Ta = -40°C to +85°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

Support Tool

In-circuit Emulator

PX-ICE102H930F-LQFP100-P-1414

□ MN102H74D, MN102H74F, MN102H74G

Type	MN102H74D	MN102H74F	MN102H74G
ROM (x8-bit)	64 K	96 K	128 K
RAM (x8-bit)	4 K	4 K	4 K
Package	LQFP100-P-1414 *Lead-free		
Minimum Instruction Execution Time	With main clock operated	83.3 ns (at 3.0 V to 3.6 V, 12 MHz)	
Interrupts	<ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin • Watchdog • $\overline{\text{NMI}}$ pin • Timer counter 0 to 9 underflow • Timer counter 10 to 13 under/overflow • Timer counter 10 to 13 compare capture A • Timer counter 10 to 13 compare capture B • ATC ch.0 to 3 transfer finish • External 0 to 5 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • A/D conversion finish • USB general-purpose • USB SOF • USB end points 1 to 8 		
USB Functions	<p>Conforms to USB1.1. USB transceiver built-in Full-speed (12 Mbps) supported. 9 end points (FIFO built-in independently) FIFO size (EP0, 1, 2, 3, 4, 5, 6, 7, 8): 64, 128, 128, 128, 128, 128, 128, 128 bytes</p> <ul style="list-style-type: none"> • EP0 Control transfer IN/OUT (two ways) • EP1 to EP8 Interrupt/Bulk/Isochronous transfer supported. Settable to IN or OUT. Double Buffering function supported. When the MAXP size is set to a half or less of the MAXFIFO size for each EP, the Double Buffering function is made valid automatically. 		
Timer Counter	<p>Timer counter 0: 8-bit × 1 (timer output, event count, timer interrupt) Clock source SYSCLK; XI; prescaler 0; TM0IO pin Interrupt source Timer counter 0 underflow</p> <p>Timer counter 1: 8-bit × 1 (timer output, event count, timer interrupt) Clock source SYSCLK; prescaler 0; TM1IO pin Interrupt source Timer counter 1 underflow</p> <p>Connectable Timer counters 0 to 1</p> <p>Timer counter 2: 8-bit × 1 (timer output, event count, timer interrupt, A/D conversion start) Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 3 underflow; timer counter 4 underflow; TM2IO pin Interrupt source Timer counter 2 underflow</p> <p>Timer counter 3: 8-bit × 1 (timer output, event count, timer interrupt) Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow; timer counter 4 underflow; TM3IO pin Interrupt source Timer counter 3 underflow</p> <p>Timer counter 4: 8-bit × 1 (timer output, event count, timer interrupt) Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow; timer counter 3 underflow; TM4IO pin Interrupt source Timer counter 4 underflow</p>		

Timer Counter (Continue)

Timer counter 5: 8-bit × 1 (timer output, event count, timer interrupt)
 Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 2 underflow;
 timer counter 3 underflow; timer counter 4 underflow; TM5IO pin
 Interrupt source Timer counter 5 underflow

Connectable Timer counters 2 to 5

Timer counter 6: 8-bit × 1 (timer output, event count, timer interrupt, serial clock generation)
 Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 7 underflow;
 timer counter 8 underflow; TM6IO pin
 Interrupt source Timer counter 6 underflow

Timer counter 7: 8-bit × 1 (timer output, event count, timer interrupt, serial clock generation)
 Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow;
 timer counter 8 underflow; TM7IO pin
 Interrupt source Timer counter 7 underflow

Timer counter 8: 8-bit × 1 (timer output, event count, timer interrupt, serial clock generation)
 Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow;
 timer counter 7 underflow; TM8IO pin
 Interrupt source Timer counter 8 underflow

Timer counter 9: 8-bit × 1 (timer output, event count, timer interrupt)
 Clock source SYSCLK; 1/8 of SYSCLK; 1/32 of SYSCLK; timer counter 6 underflow;
 timer counter 7 underflow; timer counter 8 underflow; TM9IO pin
 Interrupt source Timer counter 9 underflow

Connectable Timer counters 6 to 9

Timer counter 10: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
 Clock source SYSCLK; 1/8 of SYSCLK; timer counter 2 or 3 underflow; 2-phase encoding of
 TM10IOA/TM10IOB pin (1×, 4×); TM10IOB pin
 Interrupt source Timer counter 10 under/overflow; timer counter 10 compare capture A;
 timer counter 10 compare capture B

Timer counter 11: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
 Clock source SYSCLK; 1/8 of SYSCLK; timer counter 8 or 9 underflow; 2-phase encoding of
 TM11IOA/TM11IOB pin (1×, 4×); TM11IOB pin
 Interrupt source Timer counter 11 under/overflow; timer counter 11 compare capture A;
 timer counter 11 compare capture B

Timer counter 12: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
 Clock source SYSCLK; 1/8 of SYSCLK; timer counter 4 or 5 underflow; 2-phase encoding of
 TM12IOA/TM12IOB pin (1×, 4×); TM12IOB pin
 Interrupt source Timer counter 12 under/overflow; timer counter 12 compare capture A;
 timer counter 12 compare capture B

Timer counter 13: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)
 Clock source SYSCLK; 1/8 of SYSCLK; timer counter 6 or 7 underflow; 2-phase encoding of
 TM13IOA/TM13IOB pin (1×, 4×); TM13IOB pin
 Interrupt source Timer counter 13 under/overflow; timer counter 13 compare capture A;
 timer counter 13 compare capture B

See the next page for electric characteristics, pin assignment, and support tool.

Serial Interface	Serial 0: 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length) Clock source 1/2 or 1/16 of timer counter 6 underflow; external pin
	Serial 1: 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length) Clock source 1/2 or 1/16 of timer counter 7 underflow; external pin
	Serial 2: 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length) Clock source 1/2 or 1/16 of timer counter 8 underflow; external pin
	Serial 3: 8-bit × 1 (transfer direction of MSB/LSB selectable; transmission / reception of 7, 8-bit length) Clock source 1/2 or 1/16 of timer counter 9 underflow; external pin
	UART × 2 (common use with serial 0 to 3) I ² C × 2 (common use with serial 0, 1; single master)

ATC	4-ch DMA transfer enabled between memory and memory or memory and peripheral register by set interrupt factor and software activation setting Transfer unit: bytes/word Transfer mode: 1 word/burst (max. 128 K bytes) Transfer addressing: source/destination pointer fix/increment High-speed transfer enabled between USB-FIFO and internal RAM in single address mode
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I/O Pins	I/O	77 • Common use : 77 (pull-up resistance specifiable)
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A/D Inputs	10-bit × 8-ch. (with S/H)
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Special Ports	USB ports (D+, D-)
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Notes	4 multiply PLL built-in, generation of internal 48 MHz at external oscillation 12 MHz
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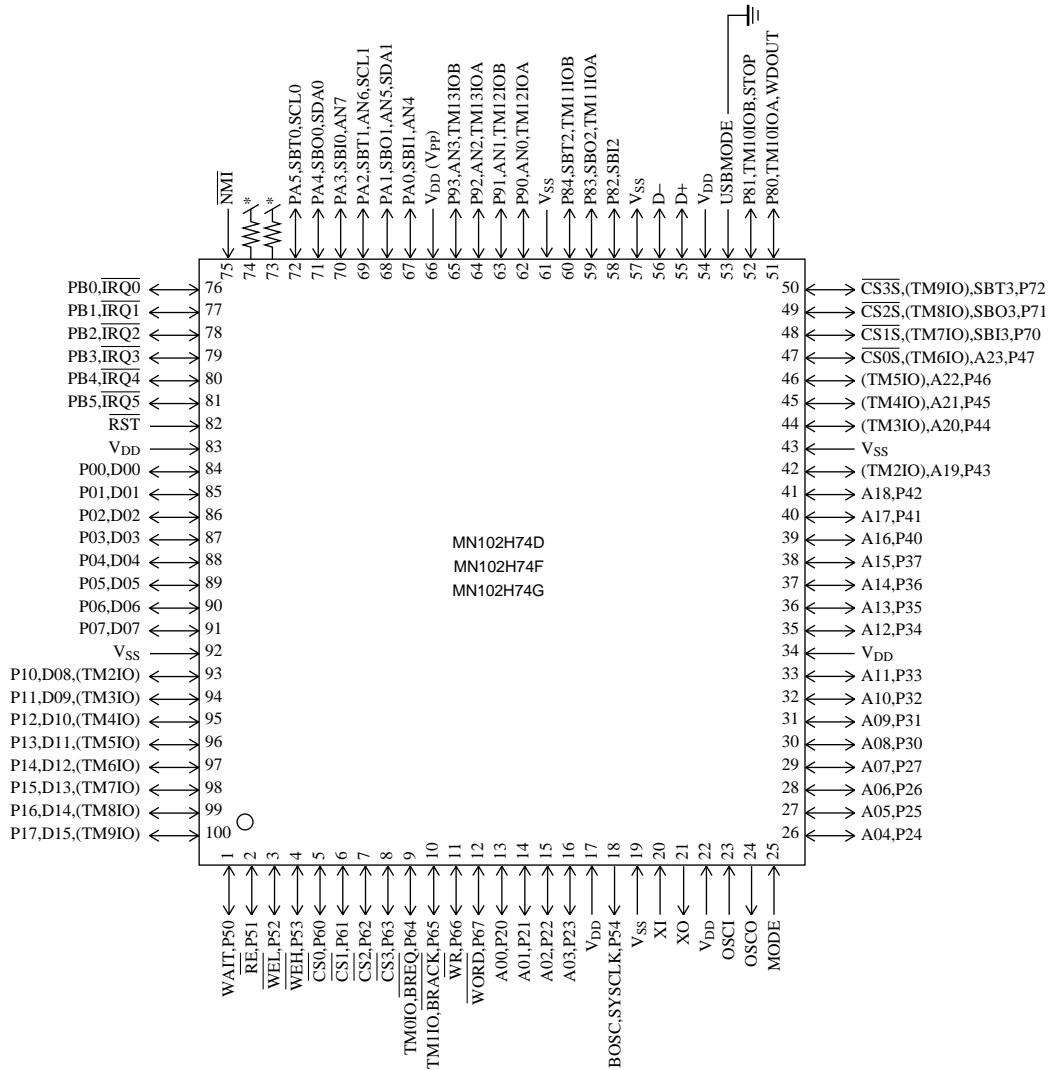
Electrical Characteristics
Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 12 MHz, VDD = 3.3 V			65+10α*	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			70	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 12 MHz, VDD = 3.3 V, output open			30+10α*	mA

(Ta = -20°C to +70°C, VDD = 3.3 V, VSS = 0 V)

* "α" depends on products. MN102H74D, MN102H74F, MN102H74G: α = 0
MN102HF74G: α = 1

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use 4.7 kΩ to 10 kΩ.

Support Tool

In-circuit Emulator	PX-ICE102H74-LQFP100-P-1414	
Flash Memory Built-in Type	Type	MN102HF74G [ES (Engineering Sample) available]
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	83.3 ns (at 3.0 V to 3.6 V, 12 MHz)
	Package	LQFP100-P-1414 *Lead-free

□ MN102L35G

Type	MN102L35G						
ROM (×8-bit)	144 K						
RAM (×8-bit)	5 K						
Package (Conventional Package)	SDIP064-P-0750C *Lead-free (SDIP064-P-0750)						
Minimum Instruction Execution Time	167 ns (at 4.75 V to 5.25 V, 12 MHz)						
Interrupts	External (4 lines) Internal (23 lines): Timer × 8, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 2, I ² C × 1, Caption × 2, Remote control × 1, Address coincidence × 4						
Timer Counter	8-bit timer × 2 16-bit timer × 2 Watchdog timer: 17-bit × 1						
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / I ² C (master) / UART × 1						
Caption	• Built-in sync separator × 2						
I/O Pins	<table border="1"> <tr> <td>I/O</td> <td>49</td> <td>• Common use</td> </tr> <tr> <td>Input</td> <td>1</td> <td>• Common use</td> </tr> </table>	I/O	49	• Common use	Input	1	• Common use
I/O	49	• Common use					
Input	1	• Common use					
A/D Inputs	8-bit × 8-ch. (with S/H)						
D/A Outputs	4-bit × 4-ch. (analog R, G, B, YM output)						
PWM	8-bit × 6-ch.						
Special Ports	Remote control reception						
CRTC	3-layer display (graphics, characters, splits)						
Notes	Remote control input discriminant circuit built-in						

Electrical Characteristics

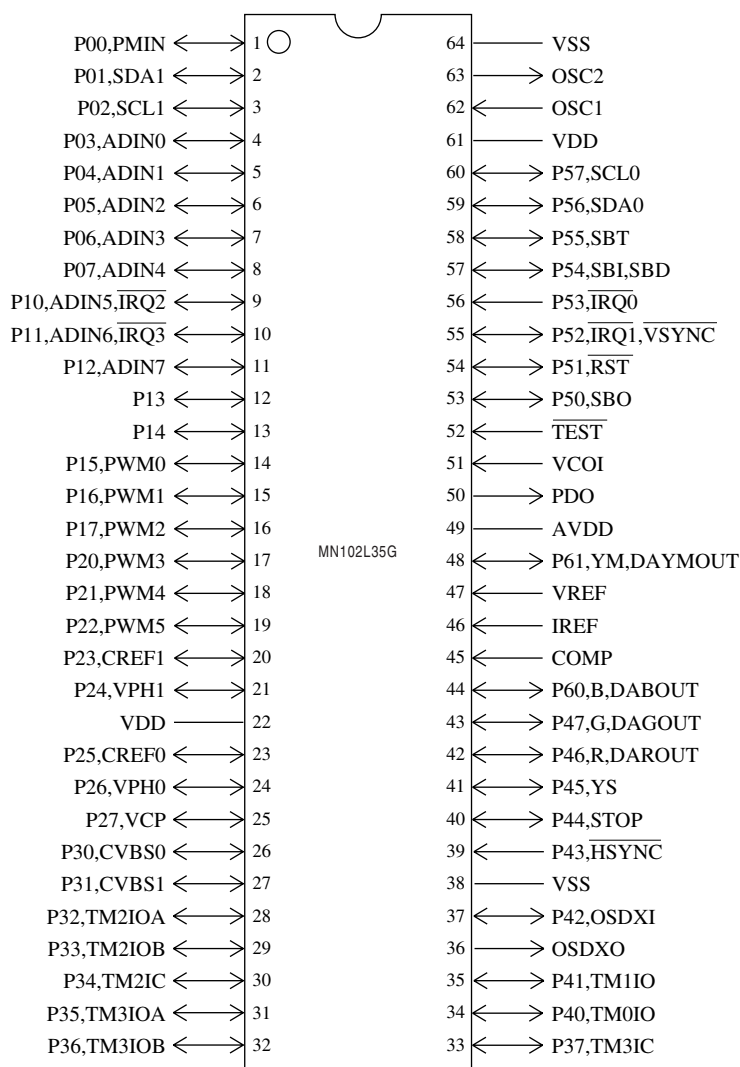
D/A characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
D/A full-scale output current	IFS	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	4.5	5.0	5.5	mA
D/A output voltage setting range	VO	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			1.1	V
D/A non-linear error	NLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A differential non-linear error	DNLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A channel interval error	IFS	VREF = 1.2 V, RIREF = 1.2 kΩ, Error from 4-channel average IFS			± 5	%

(Ta = 25°C, VDD = AVDD = 5.0 V, VSS = 0 V, fosc = 4 MHz)

Pin Assignment

() : Conventional Package



SDIP064-P-0750C *Lead-free
(SDIP064-P-0750)

Support Tool

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L35-SDIP064-P-0750	
EPROM Built-in Type	Type	MN102LP35Z
	ROM (× 16-bit)	144 K
	RAM (× 16-bit)	5 K
	Minimum instruction execution time	167 ns (at 4.75 V to 5.25 V, 12 MHz)
	Package	SDIP064-P-0750C *Lead-free
	(Conventional Package)	(SDIP064-P-0750)

□ MN102H75K

Type	MN102H75K
ROM (×8-bit)	256 K
RAM (×8-bit)	8 K
Package	QFP084-P-1818E *Lead-free
Minimum Instruction Execution Time	83 ns (at 3.0 V to 3.6 V, 12 MHz)
Interrupts	External (6 lines) Internal (30 lines) : Timer × 11, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 4, I ² C × 1, Caption × 4, Remote control × 1, Address coincidence × 4
Timer Counter	8-bit timer × 4 16-bit timer × 2 Watchdog timer: 17-bit × 1
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / I ² C (master) / UART × 2
Caption	• Built-in sync separator × 2
I/O Pins	I/O 66 • Common use
A/D Inputs	8-bit × 12-ch. (with S/H)
D/A Outputs	4-bit × 4-ch. (analog R, G, B, YM output)
PWM	8-bit × 7-ch.
Special Ports	Remote control reception
CRTC	3-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in

Electrical Characteristics

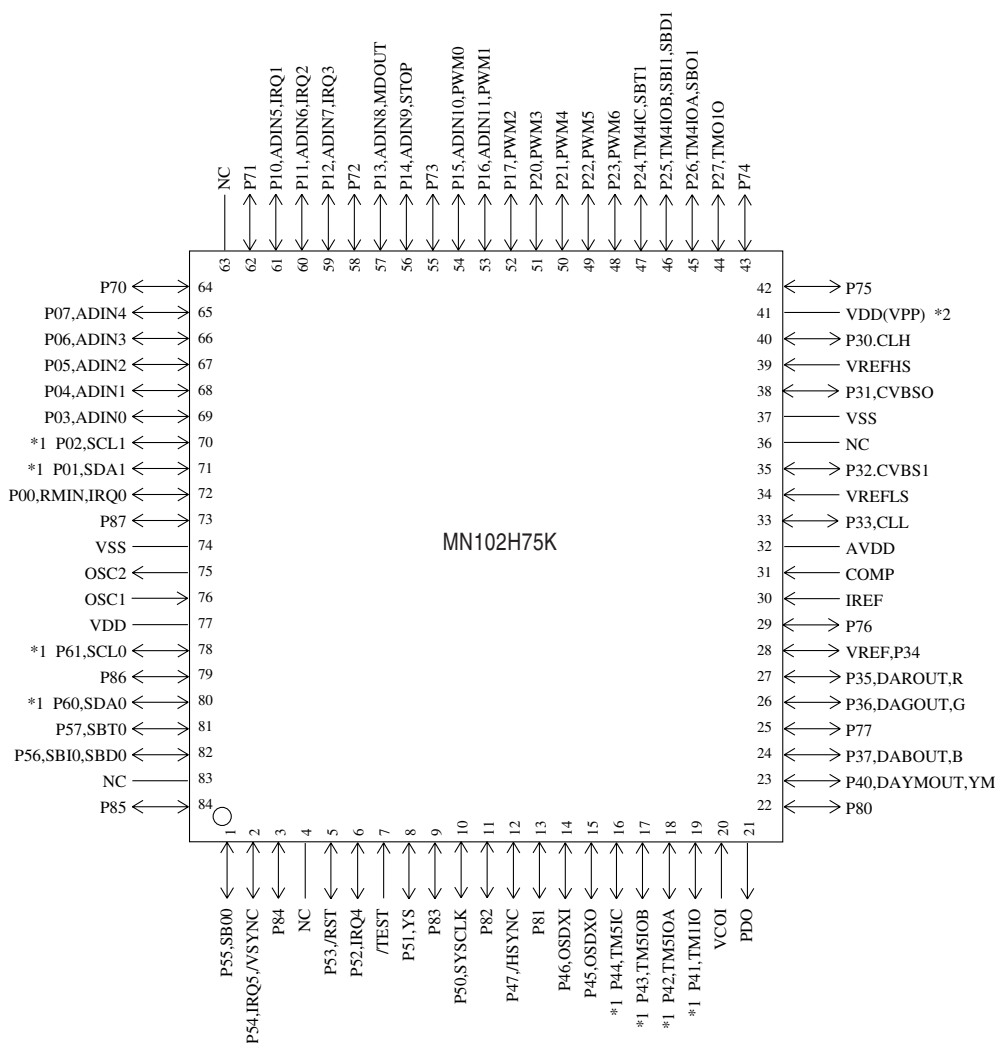
D/A characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
D/A full-scale output current	IFS	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	4.5	5.0	5.5	mA
D/A output voltage setting range	VO	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	0.9		1.1	V
D/A non-linear error	NLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A differential non-linear error	DNLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A differential non-linear error	IFS	VREF = 1.2 V, RIREF = 1.2 kΩ, Error from 4-channel average IFS			± 5	%

D/A channel interval error

(Ta = 25°C, VDD = AVDD = 3.3 V, VSS = 0 V, fosc = 4 MHz)

Pin Assignment



QFP084-P-1818E *Lead-free

*1: 5 V dielectric Nch open drain output pin

*2 : MN102H75K (VDD), MN102HF75K (VPP)

Support Tool

In-circuit Emulator	PX-ICE102H75-QFP084-P-1818E	
Flash Memory Built-in Type	Type	MN102HF75K
	ROM (× 16-bit)	256 K
	RAM (× 16-bit)	8 K
	Minimum instruction execution time	83 ns (at 3.0 V to 3.6 V, 12 MHz)
	Package	QFP084-P-1818E *Lead-free

□ MN102H85K

Type	MN102H85K
ROM (×8-bit)	256 K
RAM (×8-bit)	8 K
Package (Conventional Package)	SDIP064-P-0750C *Lead-free (SDIP064-P-0750)
Minimum Instruction Execution Time	83 ns (at 3.0 V to 3.6 V, 12 MHz)
Interrupts	External (6 lines) Internal (30 lines): Timer × 11, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 4, I ² C × 1, Caption × 4, Remote control × 1, Address coincidence × 4
Timer Counter	8-bit timer × 4 16-bit timer × 2 Watchdog timer: 17-bit × 1
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / I ² C (master) / UART × 2
Caption	• Built-in sync separator × 2
I/O Pins	I/O 50 • Common use
A/D Inputs	8-bit × 12-ch. (with S/H)
D/A Outputs	4-bit × 4-ch. (analog R, G, B, YM output)
PWM	8-bit × 7-ch.
Special Ports	Remote control reception
CRTC	3-layer display (graphics, characters, splits)
Notes	Remote control input discriminant circuit built-in

Electrical Characteristics

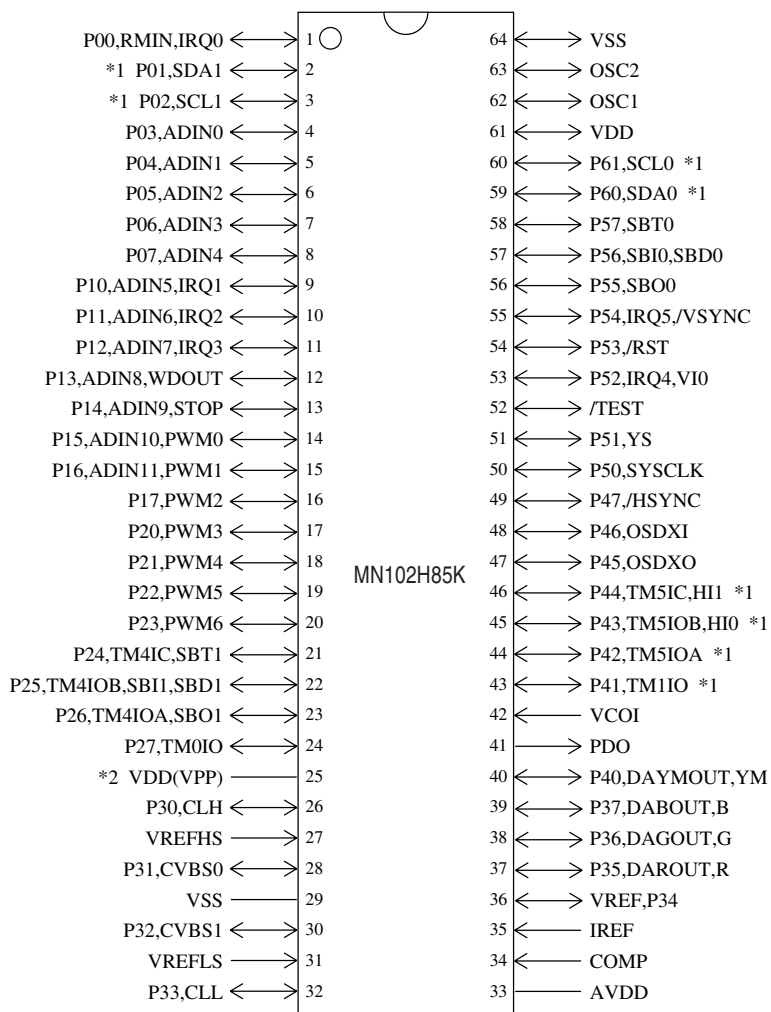
D/A characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
D/A full-scale output current	IFS	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	4.5	5.0	5.5	mA
D/A output voltage setting range	VO	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	0.9		1.1	V
D/A non-linear error	NLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A differential non-linear error	DNLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			± 0.5	LSB
D/A channel interval error	IFS	VREF = 1.2 V, RIREF = 1.2 kΩ, Error from 4-channel average IFS			± 5	%

(Ta = 25°C, VDD = AVDD = 3.3 V, VSS = 0 V, fosc = 4 MHz)

Pin Assignment

() : Conventional Package



SDIP064-P-0750C *Lead-free
(SDIP064-P-0750)

*1: 5 V dielectric Nch open drain output pin

*2 : MN102H85K (VDD), MN102HF85K (VPP)

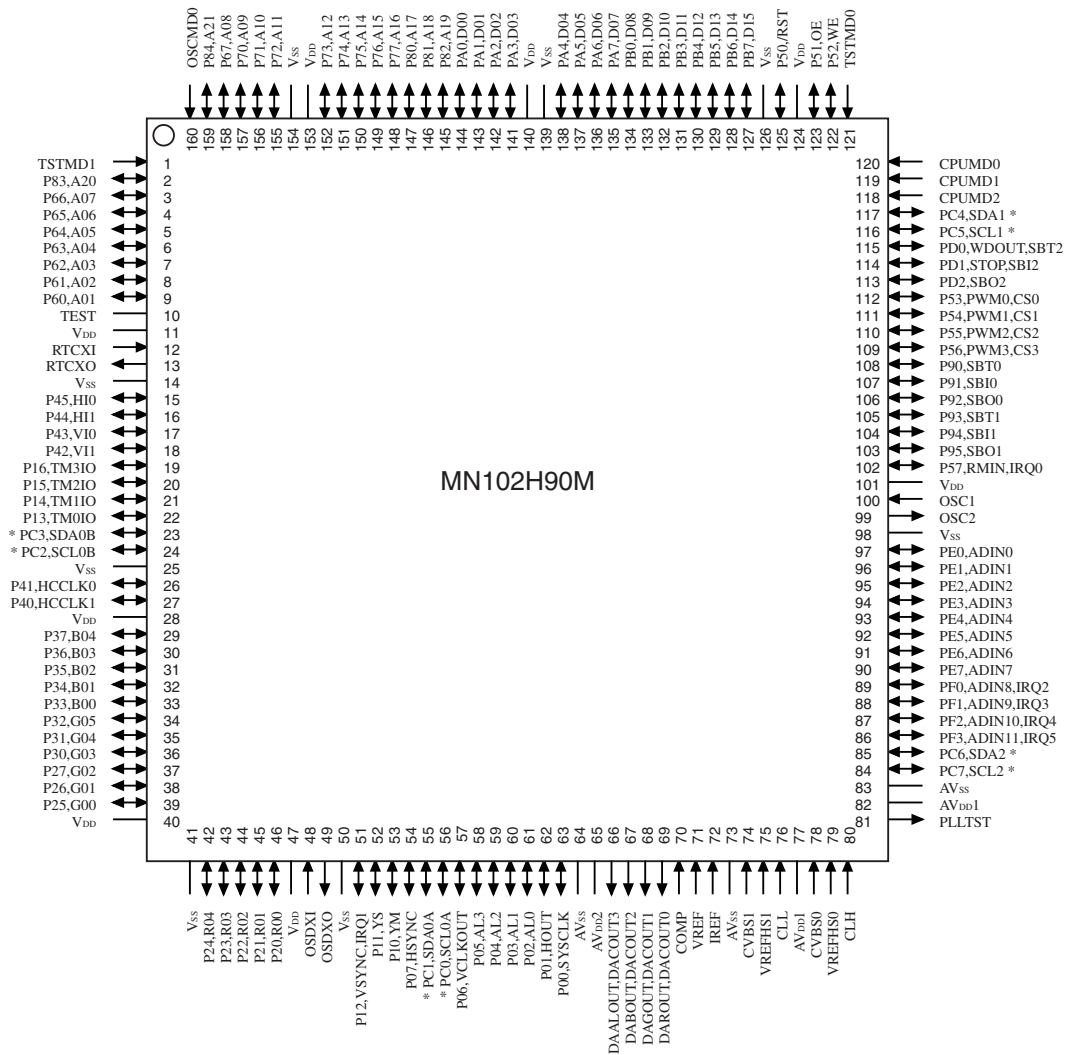
Support Tool

In-circuit Emulator	PX-ICE102H85-SDIP064-P-0750	
Flash Memory Built-in Type	Type	MN102HF85K
	ROM (× 16-bit)	256 K
	RAM (× 16-bit)	8 K
	Minimum instruction execution time	83 ns (at 3.0 V to 3.6 V, 12 MHz)
	Package	SDIP064-P-0750C *Lead-free
	(Conventional Package)	(SDIP064-P-0750)

□ MN102H90M

Type	MN102H90M
ROM	384 Kbyte or external ROM
RAM	20 K
Package	*QFP160-P-2828F *Lead-free
Minimum Instruction Execution Time	83 ns (at 3.0 V to 3.6 V, 12 MHz)
Interrupts	External (6 lines) Internal (35 lines) : Timer × 10, A/D × 1, OSD × 3, Serial × 6, I ² C × 3, Caption × 4, Remote control × 1, Address coincidence × 4, RTC × 3
Timer Counter	8-bit timer × 10 Watchdog timer: 16-bit × 1
Serial Interface	I ² C × 3: for multimaster mode, bus line (output) has 4 systems Sync serial / I ² C (master) / UART × 3
Caption	• Built-in sync separator × 2
I/O Pins	I/O 111 • Common use
A/D Inputs	8-bit × 12-ch. (with S/H)
D/A Outputs	8-bit × 4-ch. (general use or analog R, G, B, α output)
PWM	8-bit × 4-ch.
Special Ports	Remote control reception, digital OSD output
CRTC	3-layer display (graphics, characters, sprites)
Notes	Remote control input discriminant circuit, real time clock, hcounter built-in

Pin Assignment



*QFP160-P-2828F *Lead-free

*: 5 V tolerant Nch open drain output pin

Support Tool

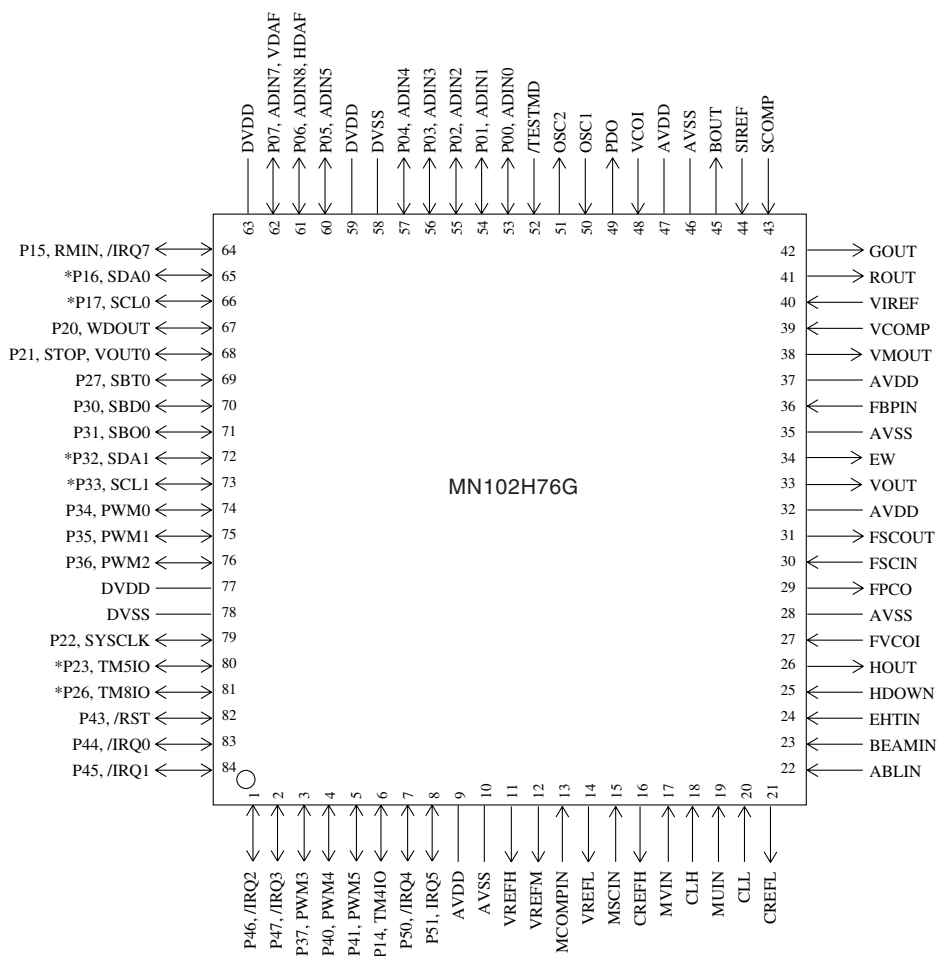
In-circuit Emulator

PX-ICE102H90-QFP160-P-2828F

□ MN102H76G

Type	MN102H76G		
ROM (×8-bit)	128 K		
RAM (×8-bit)	4 K		
Package	QFP084-P-1818E *Lead-free		
Minimum Instruction Execution Time	83 ns (at 3.135 V to 3.465 V, 12 MHz)		
Interrupts	External (7 lines) Internal (28 lines) : Timer × 11, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 2, I ² C × 1, Caption × 2, Remote control × 1, Address coincidence × 4, HSYNC × 1, VSYNC × 1		
Timer Counter	8-bit timer × 10 Watchdog timer: 17-bit × 1		
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1		
Caption	• Built-in sync separator × 1		
I/O Pins	I/O	35	• Common use
A/D Inputs	10-bit × 8-ch. (with S/H)		
PWM	8-bit × 6-ch.		
Special Ports	Remote control reception		
CRTC	3-layer display (graphics, characters, splits)		
Notes	Remote control input discriminant circuit built-in, built-in NTSC video signal processing circuit, built-in 3-line comb filter		

Pin Assignment



QFP084-P-1818E *Lead-free

*5 V dielectric Nch open drain output pin

Support Tool

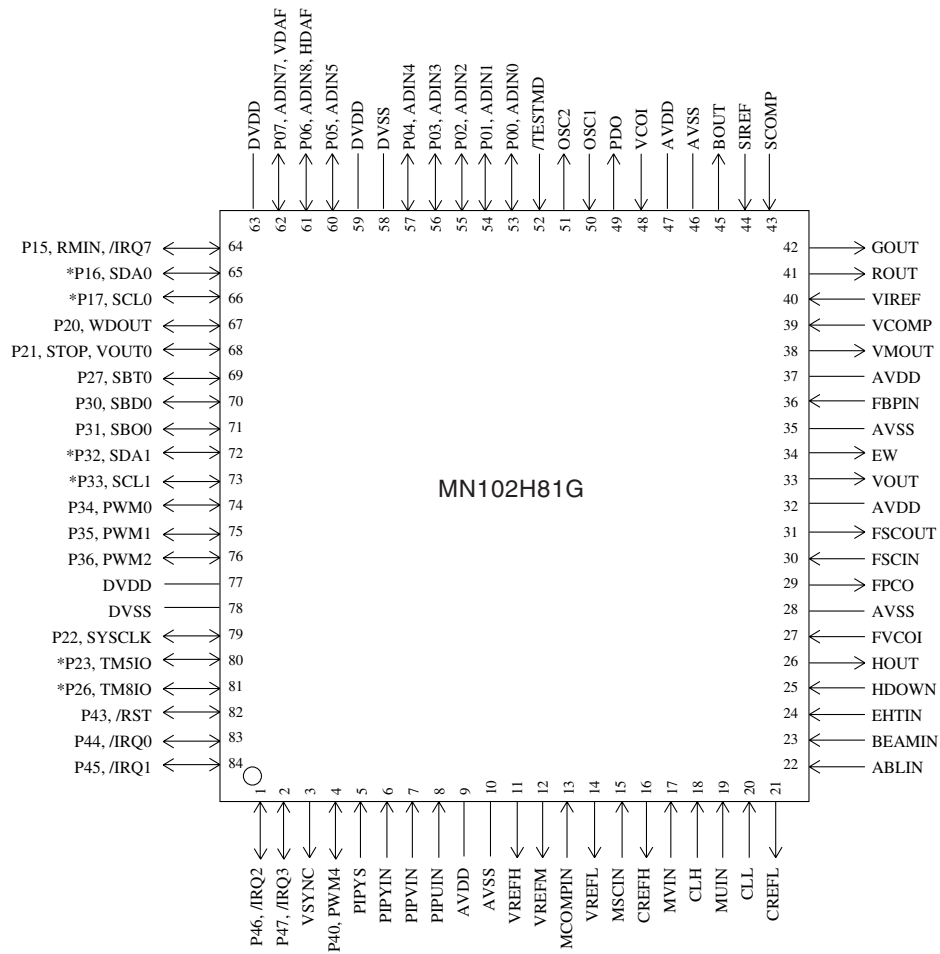
In-circuit Emulator

PX-ICE102H76-QFP084-P-1818E

□ MN102H81G

Type	MN102H81G		
ROM (×8-bit)	128 K		
RAM (×8-bit)	4 K		
Package	QFP084-P-1818E *Lead-free		
Minimum Instruction Execution Time	83 ns (at 3.135 V to 3.465 V, 12 MHz)		
Interrupts	External (5 lines) Internal (28 lines) : Timer × 11, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 1, I ² C × 1, Caption × 2, Remote control × 1, Address coincidence × 4, HSYNC × 1, VSYNC × 1		
Timer Counter	8-bit timer × 10 Watchdog timer: 17-bit × 1		
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / UART × 1		
Caption	• Built-in sync separator × 1		
I/O Pins	I/O	30	• Common use
A/D Inputs	10-bit × 8-ch. (with S/H)		
PWM	8-bit × 6-ch.		
Special Ports	Remote control reception		
CRTC	3-layer display (graphics, characters, splits)		
Notes	Remote control input discriminant circuit built-in, built-in NTSC video signal processing circuit, built-in 3-line comb filter		

Pin Assignment



QFP084-P-1818E *Lead-free

*5 V dielectric Nch open drain output pin

Support Tool

In-circuit Emulator

PX-ICE102H81-QFP084-P-1818E

AM3^{32-bit} SERIES

AM3 (MN103/MN103S) Series

The AM3 series are the 32-bit microcomputer suitable for multimedia applications such as movie, digital audio, graphic and communications.

Both high quality and low power consumption have been achieved through use of the C language architecture and optimized C compiler. Combined use of the extension calculation command features which can be applied flexibly to various multimedia applications permits efficient system development.

Features

- **32-bit C language architecture**

- Simple and highly efficient command sets

- High code generation efficiency of commands by 1 byte basic word length

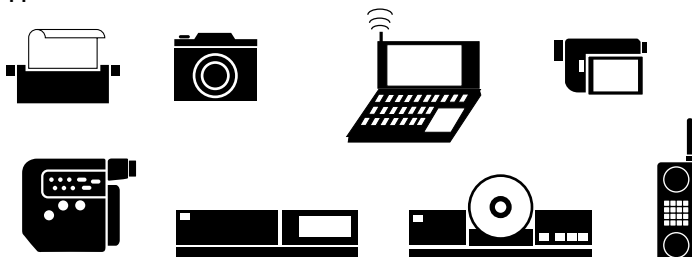
- High speed command execution by 5-step pipeline configured load/store architecture

- High speed execution of branch commands

- **Extension calculation function meeting multimedia requirements**

- **Optimized C language compiler that generates high-speed command codes**

■ Application



□ MN103000

Type	MN103000
Command RAM (x64-bit)	16 K-byte
Data RAM (x32-bit)	16 K-byte
Package (Conventional Package)	QFP160-P-2828F *Lead-free (QFP160-P-2828B)
Minimum Instruction Execution Time	17 ns (at 3.3 V to lerrance = ± 5%, 60 MHz)
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 28 • SIF × 4 • DMAC × 4 • WDT • A/D • System error
Timer Counter	<p>Timer counter 0 to 3: 32-bit × 1 (interval timer, event count, timer output, interrupt, clock source for serial I/F, A/D conversion trigger) Clock Source IOCLK; external clock input; underflow of timer counter Interrupt Source underflow of timer counter 0, 1, 2, 3</p> <p>Timer counter 4 to 7: 32-bit × 1 (interval timer, event count, timer output, interrupt, clock source for serial I/F) Clock source IOCLK; external clock input; underflow of timer counter Interrupt source underflow of timer counter 4, 5, 6, 7</p> <p>*: Configuration of each of timer counters 0 to 3 and timer counters 4 to 7 can be changed to 8-, 16- and 24-bit timer counters.</p> <p>Timer counter 8: 16-bit × 1 (interval timer, event count, toggle output (2 lines), PWM output, one-shot output, input capture (2 lines), interrupt, DMA start, generation of timer synchronous output timing) Clock source IOCLK; external clock input; underflow of timer counter Interrupt source overflow of timer counter 8; coincidence with compare capture (2 lines) or at capture</p> <p>Timer counter 9: 16-bit × 1 (interval timer, event count, toggle output (2 lines), PWM output, high-speed PWM output, one-shot output, input capture (2 lines), interrupt, DMA start, generation of timer synchronous output timing) Clock source IOCLK; external clock input; underflow of timer counter Interrupt source overflow of timer counter 9; coincidence with compare capture (2 lines) or at capture</p> <p>Timer counter 10: 16-bit × 1 (interval timer, event count, toggle output (3 lines), PWM output (2 lines), one-shot output, input capture (3 lines), interrupt, DMA start, 2-phase encode) Clock source IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source overflow of timer counter 10; underflow of timer counter 10; coincidence with compare capture (3 lines) or at capture</p> <p>Timer counter 11: 16-bit × 1 (interval timer, event count, toggle output (4 lines), PWM output, inter-offset 3-phase PWM output, one-shot output, input capture (4 lines), interrupt, DMA start, 2-phase encode) Clock source IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source overflow of timer counter 11; underflow of timer counter 11; coincidence with compare capture (4 lines) or at capture</p> <p>Timer counter 12: 16-bit × 1 (interval timer, event count, toggle output (4 lines), PWM output (3 lines), one-shot output, input capture (4 lines), interrupt, 2-phase encode) Clock source IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source overflow of timer counter 12; underflow of timer counter 12; coincidence with compare capture (4 lines) or at capture</p>

Timer Counter (continue)	Watchdog timer: 16-bit to 25-bit × 1		
Serial Interface	Serial 0, 1: 7-bit, 8-bit × 2 (clock synchronous mode, start-stop synchronous mode, I ² C mode) Clock source: (clock synchronous mode, start-stop synchronous mode) IOCLK; underflow of timer counter; external clock (I ² C mode) IOCLK; underflow of timer counter		
I/O Pins	I/O	51	• Common use
	Output	25	• Common use
	Input	13	• Common use
A/D Inputs	10-bit × 8-ch.		
PWM	16-bit × 5-ch.		
ICR	16-bit × 15-ch. (common with OCR)		
OCR	16-bit × 15-ch. (common with ICR)		
Timer Synchronous Output	4-bit (synchronous output) × 2-ch.		
DMAC	4-ch.		

Electrical Characteristics**Supply current**

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	VDD , PVDD , AVDD = 3.3 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			250	mA
Supply current at SLEEP	IDD2	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			50	mA
Supply current at HALT	IDD3	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			5	mA
Supply current at stopping	IDD4	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , Fosc = Oscillation stopped Output open			300	μA

(Ta = -20°C to +70°C)

See the next page for electrical characteristics (continue), pin assignment and support tool.

Electrical Characteristics (Continue)

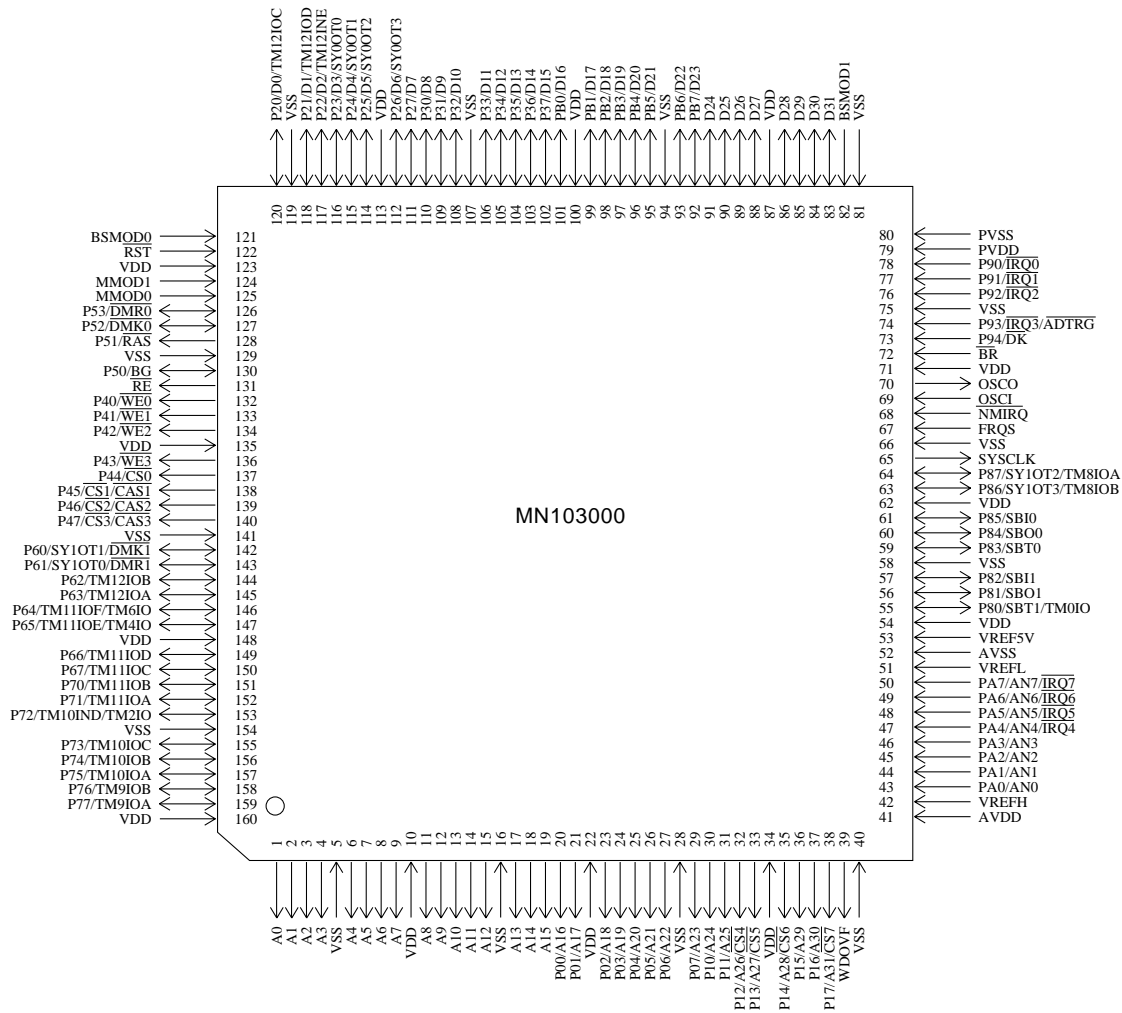
A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.3 V, VREF- = 0.0 V			± 7	LSB
A/D conversion relative error		A/D conversion clock = 5 MHz			± 5	LSB
A/D conversion time			2.8			μs

(Ta = -20°C to +70°C, AVDD = 3.3 V, AVSS = 0.0 V)

Pin Assignment

() : Conventional Package



QFP160-P-2828F *Lead-free

(QFP160-P-2828B)

Support Tool

In-circuit Emulator

PX-ICE103000-QFP160-P-2828B

On-board Development Tools

CSIDE-MN10300 (Computex Co., Ltd, product)

MN103000

□ MN103001G

Type	MN103001G		
Command ROM (x64-bit)	128 K-byte		
Data RAM (x32-bit)	8 K-byte		
Package	LQFP100-P-1414 *Lead-free		
Minimum Instruction Execution Time	17 ns (at 3.0 V to 3.6 V, 60 MHz)		
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 18 • SIF × 8 • WDT • A/D • System error		
Timer Counter	<p>Timer counter 0 to 3: 32-bit × 1 (interval timer, event count, timer output, interrupt, clock source for serial I/F, A/D conversion trigger) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 0, 1, 2, 3</p> <p>Timer counter 4 to 7: 32-bit × 1 (interval timer, event count, timer output, PWM output, interrupt) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 4, 5, 6, 7</p> <p>Timer counter 8 to B: 32-bit × 1 (interval timer, event count, timer output, PWM output, interrupt, clock source for serial I/F) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 8, 9, A, B</p> <p>*: each of timer counters 0 to 3, 4 to 7, and 8 to B can be changed to an 8-, 16-, or 24-bit timer counter.</p> <p>Timer counter 10: 16-bit × 1 (interval timer, event count, PWM output, toggle output (2 lines), interrupt, input capture (2 lines), one-shot output) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source overflow of timer counter 10; coincidence with compare capture (2 lines) or at capture</p> <p>Timer counter 11: 16-bit × 1 (interval timer, event count, toggle output, interrupt) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter</p> <p>Timer counter 12: 16-bit × 1 (same functions as those of timer counter 11)</p> <p>Timer counter 13: 16-bit × 1 (same functions as those of timer counter 11)</p> <p>Watchdog timer: 16- to 25-bit × 1-ch.</p>		
Serial Interface	<p>Serial 0: 7-, 8-bit × 1 (clock synchronous, start-stop synchronous, I²C mode)</p> <p>Serial 1, 2: 7-, 8-bit × 2 (clock synchronous mode)</p> <p>Serial 3: 7-, 8-bit × 1 (start-stop synchronous mode) Clock source (clock synchronous mode, start-stop synchronous mode) IOCLK; underflow of timer counter; external clock (I²C mode) IOCLK; underflow of timer counter</p>		
I/O Pins	I/O	53	• Common use
	Output	15	• Common use
	Input	4	• Common use

A/D Inputs	10-bit × 4-ch.
PWM	16-bit × 1-ch., 8-bit × 8-ch. (common with timer)
ICR	16-bit × 2-ch. (common with OCR)
OCR	16-bit × 2-ch., 8-bit × 8-ch. (common partially with ICR)

Electrical Characteristics**Supply current**

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	VDD , PVDD , AVDD = 3.3 V VI = VDD or VSS fosc = 15.0 MHz CKSEL pin = Hi level At internal = 60 MHz Output open			180	mA
Supply current at stopping	IDD4	VDD , PVDD , AVDD = 3.6 V VI = VDD or VSS fosc = Oscillation stopped Output open			100	μA

(Ta = -20°C to +70°C)

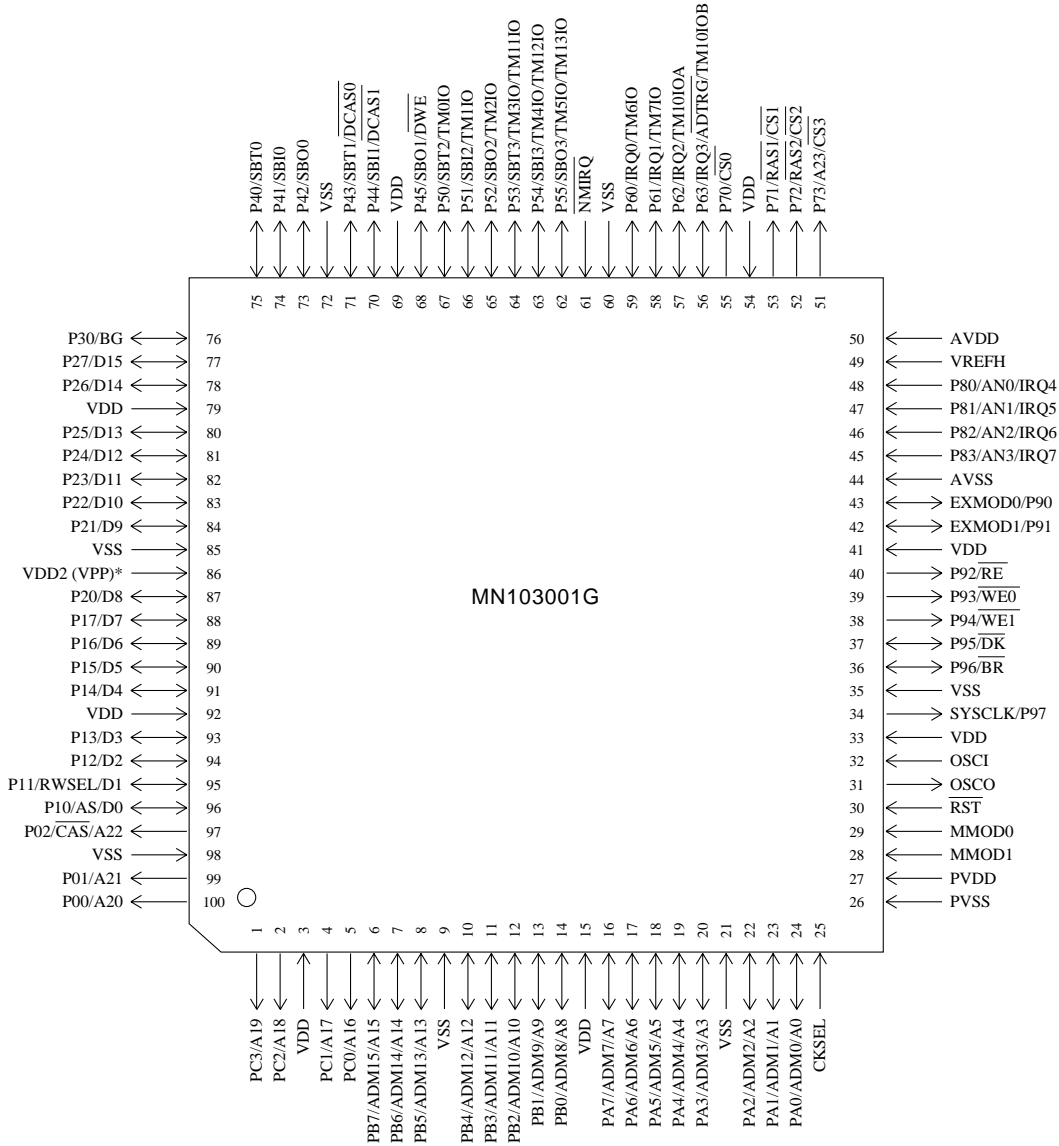
A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.3 V A/D conversion clock = 5 MHz			± 7	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.8			μs

(Ta = -20°C to +70°C, AVDD = 3.3 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

Pin Assignment



LQFP100-P-1414 *Lead-free

* VDD2 for MN103001G and VPP for MN1030F01K

Support Tool

In-circuit Emulator	PX-ICE103001-LQFP100-P-1414
On-board Development Tools	PX-ODB103S-O CSIDE-MN10300 (Computex Co., Ltd, product)
Flash Memory Built-in Type	Type MN1030F01K
	Command ROM (× 64-bit) 256 K-byte
	Data RAM (× 32-bit) 8 K-byte
	Minimum instruction execution time 25 ns (at 3.0 V to 3.6 V, 40 MHz)
	Package LQFP100-P-1414 *Lead-free

□ MN103002A

Type	MN103002A
Command Cache	4 K-byte (2-Way)
Data Cache	4 K-byte (2-Way)
Package (Conventional Package)	QFP160-P-2828F *Lead-free (QFP160-P-2828B)
Minimum Instruction Execution Time	15 ns (at 3.3 V to lerrance = ± 5%, 66 MHz)
Interrupts	• RESET • IRQ0 to 7 • NMI • Timer 0 to 8 • SIO0 to 5 • DMAC0 to 3 • WDT • System error
Timer Counter	<p>Timer counter 0: 8-bit × 1 (timer output, 16-bit timer clock source, interval timer, event count, clock source for serial I/F0) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; underflow of timer 1, 2 Interrupt source underflow of timer counter</p> <p>Timer counter 1: 8-bit × 1 (timer output, 16-bit timer clock source, interval timer, event count, clock source for serial I/F1) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; output of timer counter 0; underflow of timer 0, 2 Interrupt source underflow of timer counter</p> <p>Timer counter 2: 8-bit × 1 (timer output; interval timer; event count; clock source for serial I/F 0, 2; DMA start) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; output of timer counter 1; underflow of timer 0, 1 Interrupt source underflow of timer counter</p> <p>Timer counter 3: 8-bit × 1 (timer output; interval timer; event count; clock source for serial I/F 1, 2; DMA start) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; output of timer counter 2; underflow of timer 0, 1, 2 Interrupt source underflow of timer counter</p> <p>Timer counter 4: 16-bit × 1 (timer output, down count, interval timer, event count) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; underflow of timer 0, 1, 2 Interrupt source underflow of timer counter</p> <p>Timer counter 5: 16-bit × 1 (timer output, down count, interval timer, event count) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; output of timer counter 4; underflow of timer 0, 1, 2 Interrupt source underflow of timer counter</p> <p>Timer counter 6: 16-bit × 1 (event count, input capture, toggle output, PWM output, high-speed PWM output, up count, interval timer, one-shot output) Clock source 1/(1, 8, 32) of I/O clock frequency; external clock input; underflow of timer 0, 1, 2 Interrupt source overflow of timer counter; compare capture A, B</p> <p>Watchdog timer × 1 (watchdog overflow output) Clock source system clock Interrupt source overflow of watchdog timer</p>
DMA Controller	<p>Number of channels: 4 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65536 Starting factor: external request, various types of interrupt, software Transfer method: 2-bus cycle transfer, 1-bus cycle transfer Transfer modes: word transfer, burst transfer, intermittent transfer</p>

Serial Interface	Serial 0: 8-bit × 1 (start-stop synchronous mode, clock synchronous mode, I ² C mode) Clock source I/O clock; timer counter 0, 2; external clock
	Serial 1: 8-bit × 1 (start-stop synchronous mode, clock synchronous mode, I ² C mode) Clock source I/O clock; timer counter 1, 3; external clock
	Serial 2: 8-bit × 1 (start-stop synchronous mode with CTS control) Clock source I/O clock; timer counter 2, 3; external clock

I/O Pins	I/O	26	• Common use
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Electrical Characteristics

Supply current

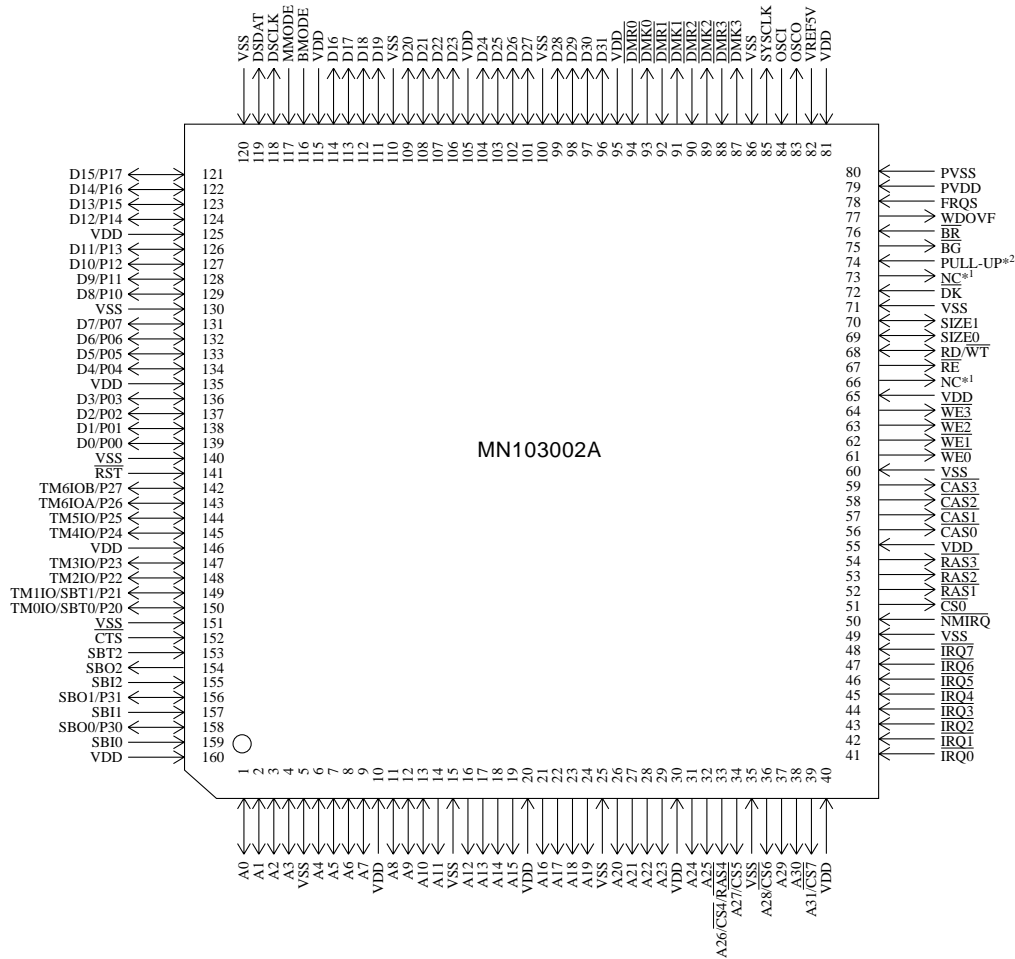
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 16.6 MHz FRQS pin = Hi level Output open			250	mA
Supply current at SLEEP	IDD2	fosc = 16.6 MHz FRQS pin = Hi level Output open			50	mA
Supply current at HALT	IDD3	fosc = 16.6 MHz FRQS pin = Hi level Output open			6	mA
Supply current at stopping	IDD4	fosc = oscillation stopped Output open			1.25	mA

(Ta = -20°C to +70°C, VDD = 3.3 V, VSS = 0 V)

See the next page for pin assignment and support tool.

Pin Assignment

() : Conventional Package



QFP160-P-2828F *Lead-free
(QFP160-P-2828B)

*1: Set to open.

*2: Pull up via the resistor.

Support Tool

In-circuit Emulator	PX-ICE103002-QFP160-P-2828B
ROM Emulator	Partner ET-II (KMC product), ROMICE64 (Computex Co., Ltd, product)
On-board Development Tools	PX-ODB103S-O CSIDE-MN10300 (Computex Co., Ltd, product)

□ MN103004K, MN103016K

Type	MN103004K	MN103016K
Command ROM (x64-bit)	256 K-byte	256 K-byte
Data RAM (x32-bit)	10 K-byte	10 K-byte
Package (Conventional Package)	QFP208-P-2828F *Lead-free, FLGA239-C-1313 *Lead-free (QFP208-P-2828A)	FLGA239-C-1313 *Lead-free
Minimum Instruction Execution Time	25 ns (at 2.7 V to 3.6 V, 40 MHz)	
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 22 • Input capture × 14 • PWM × 4 • SIF × 16 • DMAC × 4 • WDT • A/D • System error	
Timer Counter	<p>Timer counter 0 to 3: 32-bit × 1 (interval timer, event count, toggle output, interrupt, A/D conversion trigger) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 0, 1, 2, 3</p> <p>Timer counter 4 to 7: 32-bit × 1 (interval timer, event count, toggle output, interrupt, clock source for serial I/F, generation of timer synchronous output timing) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 4, 5, 6, 7</p> <p>Timer counter 8 to B: 32-bit × 1 (interval timer, event count, toggle output, interrupt, clock source for serial I/F, generation of timer synchronous output timing) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter Interrupt source underflow of timer counter 8, 9, A, B</p> <p>*: each of timer counters 0 to 3, 4 to 7, and 8 to B can be changed to an 8-, 16-, or 24-bit timer counter.</p> <p>Timer counter 10 to 13: 16-bit × 4 (interval timer, event count, toggle output, interrupt, DMA start) Clock source IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter 0, 1, 2 Interrupt source underflow of timer counter 10, 11, 12, 13</p> <p>Timer counter 14, 15: 16-bit × 2 (interval timer, event count, toggle output, PMW output, interrupt, input capture (2 lines), one-shot output, external trigger start, generation of timer synchronous output timing, DMA start) Clock source IOCLK; IOCLK/8; external clock input (2 lines); underflow of timer counter 0, 1; 2-phase encode Interrupt source overflow of timer 14, 15; underflow of timer 14, 15; coincidence of compare register with binary counter or at capture</p> <p>Watchdog timer: 16- to 25-bit × 1</p>	
DMA Controller	Number of channels: 2 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65535 Starting factor: external interrupt, timer factor, PNM factor, serial transmission/reception factor, A/D conversion finish, software factor Transfer method: 2-bus cycle transfer Addressing modes: fixed, increment, decrement Transfer modes: word transfer, burst transfer, intermittent transfer	

Serial Interface	Serial 0, 1: 7-, 8-bit × 2 (clock synchronous mode, start-stop synchronous mode, I ² C mode)
	Serial 2: 7-, 8-bit × 1 (start-stop synchronous mode)
	Serial 3 to 7: 7-, 8-bit × 5 (clock synchronous mode)
	Clock source (clock synchronous mode, start-stop synchronous mode) IOCLK; underflow of timer counter; external clock (I ² C mode) IOCLK; underflow of timer counter

I/O Pins	I/O	155	• Common use : 137
	Input	16	• Common use : 16

A/D Inputs	10-bit × 16-ch.
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PWM	12-, 14-bit resolution × 4-ch. (dedicated), 16-bit resolution × 2-ch. (common with timer)
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ICR	28-bit × 13-ch. + 16-bit × 4-ch. (common with timer)
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OCR	16-bit × 4-ch. (common with timer)
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Timer Synchronous Output	4-bit (synchronous output) × 2-ch.
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Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	VDDH, VDDB, VDD, PVDD, AVDD = 3.0 V VI = VDDH (VDDB) or VSS At internal = 40 MHz Output open			150	mA
Supply current at stopping	IDD4	VDDH, VDDB, VDD, PVDD, AVDD = 3.6 V VI = VDDH (VDDB) or VSS fosc = oscillation stopped Output open			150*	μA

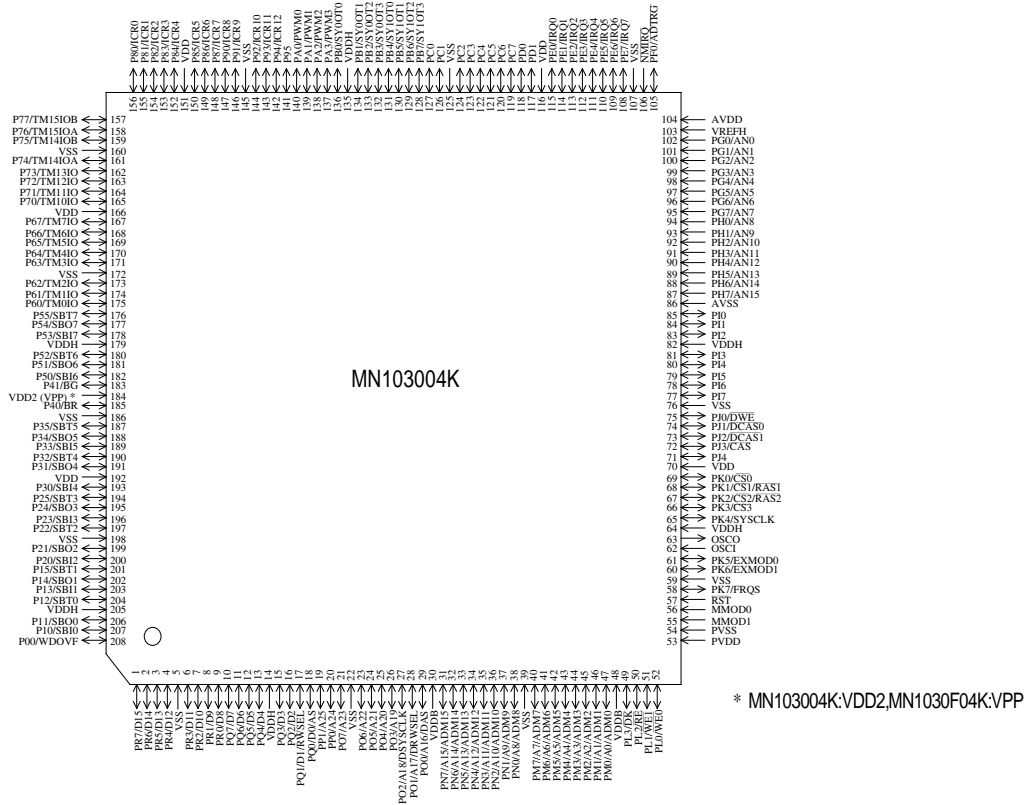
(Ta = -20°C to +85°C)
*FLGA239-C-1313

A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.0 V A/D conversion clock = 5 MHz			± 7	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.8			μs

(Ta = -20°C to +85°C, AVDD = 3.0 V, AVSS = 0 V)

See the next page for pin assignment and support tool.



QFP208-P-2828F *Lead-free
(QFP208-P-2828A)

Pin Assignment (Continue)

Perspective
↓

N.D.	N.D.	PE7, IRQ7	NMIRQ	PE1, IRQ1	PD0	PC4	PC1	PB1, SYOOT1	PA2, PWM2	P94, ICR12	P91, ICR9	P84, ICR4	P80, ICR0	N.D.	N.D.	T	
N.D.	N.D.	N.D.	PE5, IRQ5	PE3, IRQ3	VDD	PC2	PB7, SY1OT3	PB3, SYOOT3	PA0, PWM0	P92, ICR10	P85, ICR5	P82, ICR2	N.D.	N.D.	N.D.	R	
AVDD	N.D.	PF0, ADTRG	VSS	PE4, IRQ4	PC6	PC5	VSS	PB5, SY1OT1	PB0, SYOOT0	VSS	VDD	P87, ICR7	P77, TM15IOB	N.D.	P76, TM15IOA	P	
PG2, AN2	PG0, AN0	VREFH	PE6, IRQ6	PE2, IRQ2	PD1	PC3	PB6, SY1OT2	VDDH	PA1, PWM1	P90, ICR8	P83, ICR3	P74, TM14IOA	P75, TM14IOB	P73, TM13IO	VSS	N	
PG3, AN3	PG5, AN5	PG1, AN1	PG4, AN4	PE0, IRQ0	PC7	PC0	PB2, SYOOT2	PA3, PWM3	P95	P86, ICR6	P81, ICR1	P70, TM10IO	P72, TM12IO	VDD	P71, TM11IO	M	
PG7, AN7	PH1, AN9	PH2, AN10	PG6, AN6	PH3, AN11	PH0, AN8	PB4, SY1OT0	N.D.	N.D.	P93, ICR11	P67, TM7IO	P63, TM3IO	P65, TM5IO	VSS	P66, TM6IO	P64, TM4IO	L	
PH7, AN15	PH5, AN13	PH6, AN14	AVSS	PI0	PH4, AN12	N.D.	N.D.	N.D.	N.D.	P60, TM0IO	P54, SBO7	P62, TM2IO	P55, SBT7	P61, TM1IO	P53, SBT7	K	
PI2	PI3	PI4	VDDH	PI1	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P41, BG	VDDH	P51, SBO6	P52, SBT6	P50, SBT6	J	
PI0, DWĒ	PI7	VSS	PI5	PI6	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P35, SBT5	P34, SBO5	P40, BR	VDD2 (VPP)	VSS	H	
PK2, CS2, RAS2	PK0, CS0	PK1, CS1, RAS1	VDD	PI4	PI2, DCAS1	N.D.	N.D.	N.D.	N.D.	P31, SBO4	P33, SBT5	P30, SBT4	P32, SBT4	VDD	P25, SBT3	G	
OSCO	PK4, SYSCLK	VDDH	PK3, CS3	PI3, CAS	PI1, DCAS0	PN5, A13, ADM13	N.D.	N.D.	N.D.	PO5, A21	P24, SBO3	P21, SBO2	P22, SBT2	P15, SBT1	P23, SBT3	VSS	F
OSCI	VSS	PK7, FRQS	PK6, EXMOD1	PK5, EXMOD0	PN1, A9, ADM9	PN3, A11, ADM11	PO0, A16, DAS	PO2, A18, DSYSCLR	PP0, A24	PQ2, D2	PR1, D9	P13, SBT1	P20, SBT2	P14, SBO1	P12, SBT0	E	
MMOD1	RST	MMOD0	PVSS	PM4, A4, ADM4	PN0, A8, ADM8	PN4, A12, ADM12	PO7, A23	PO3, A19	PQ0, D0, AS	PQ5, D5	PQ7, D7	P10, SBO0	VDDH	P11, SBO0	P00, WDOVF	D	
PVDD	N.D.	PL1, WE1	PL3, TK	PM2, A2, ADM2	PM6, A6, ADM6	VSS	PN7, A15, ADM15	VSS	PQ3, D3	VDDH	PR3, D11	PR4, D12	PR6, D14	N.D.	N.D.	C	
N.D.	N.D.	PL2, RE	PM0, A0, ADM0	PM1, A1, ADM1	PM5, A5, ADM5	PN6, A14, ADM14	VDDH	PO6, A22	PP1, A25	PQ6, D6	PR0, D8	PR5, D13	N.D.	N.D.	N.D.	B	
N.D.	N.D.	PL0, WE0	VDDH	PM3, A3, ADM3	PM7, A7, ADM7	PN2, A10, ADM10	PO1, A17, DRWSEL	PO4, A20	PQ1, D1, RWSEL	PQ4, D4	PR2, D10	VSS	PR7, D15	N.D.	N.D.	A	

* C1 has no electrode (pin).
 * N.D. has an electrode (pin) but N.C. is not guaranteed.
 Please design so as not to cause short circuit with other wiring on the user board.
 * Each of VDD, VDDH, VDDH and VSS has multiple electrodes (pins).
 Pins having the same name are internally shorted.
 *H2: MN103004K(VDD2), MN103016K(VDD2), MN1030F04K(VPP)

FLGA239-C-1313 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE103004-QFP208-P-2828A	Not applicable to FLGA239-C-1313.
On-board Development Tools	PX-ODB103S-0 CSIDE-MN10300 (Computex Co., Ltd, product)	
Flash Memory Built-in Type	Type	MN1030F04K
	Command ROM (× 64-bit)	256 K-byte
	Data RAM (× 32-bit)	12 K-byte
	Minimum instruction execution time	25 ns (at 3.0 V to 3.6 V, 40 MHz)
	Package	QFP208-P-2828F *Lead-free, FLGA239-C-1313 *Lead-free
	(Conventional Package)	(QFP208-P-2828A)

□ MN103S33N

Type	MN103S33N		
Command ROM (×64-bit)	512 K-byte		
Data RAM (×32-bit)	24 K-byte		
Package	MBGA360-C-1313A *Lead-free		
Minimum Instruction Execution Time	24.3 ns (at 2.3 V to 2.7 V, 41 MHz)		
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ × 15 • NMI • Key input • Timer × 44 • Input capture × 16 • PWM × 8 • SIF × 25 • DMA × 12 • WDT • A/D • System error 		
Timer Counter	<p>8-bit timer × 12</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) <p>8-bit timer with PWM × 8</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) PWM generating function <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Up-down count Input capture function PWM generating function Compare/capture register 2-ch. <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Reload-down count <p>Watchdog timer × 1</p>		
DMA Controller	<p>Number of channels: 4</p> <p>Unit of transfer: 8/16/32 bits</p> <p>Max. Transfer cycles: 65535</p> <p>Starting factor: external interrupt, timer factor, PWM factor, serial transmission/reception factor, A/D conversion finish, software factor</p> <p>Transfer method: 2-bus cycle transfer</p> <p>Addressing modes: fixed, increment, decrement</p> <p>Transfer modes: word transfer, burst transfer, intermittent transfer</p>		
Serial Interface	<p>Serial 0, 1, 3 to 8, A, B: start-stop synchronization/synchronization/I²C commonly used, 10 lines</p> <p>Serial 2, 9: 2 lines for start-stop synchronization only, serial 2: 10 bytes containing receive FIFO</p>		
I/O Pins	I/O	169	• Common use
	Input	25	• Common use
A/D Inputs	10-bit × 25-ch.		
PWM	<p>12-, 14-bit resolution × 5-ch.</p> <p>output waveform value load control function provided 16-bit resolution × 2-ch.</p>		
ICR	28-bit × 13-ch. + 16-bit × 6-ch. (common with timer)		
OCR	16-bit × 12-ch. (common with timer)		
Timer Synchronous Output	4-bit (synchronous output) × 2-ch.		

Pin Assignment

Perspective

N.D.	N.D.	TDI	PF3, TM25IOB	PF1, TM24IOB	VDD2	PD5, TM15IO	PD2, TM12IO	PC6, SY1OT2, SBT8	PC4, SY1OT0, SB18	VSS	PB2, IRQ14	PA2, SBT6	P91, ICR9	P87, ICR7	P83, ICR3	P81, ICR1	N.D.	N.D.	W
N.D.	N.D.	TCK	PF2, TM25IOA	PE0, TM20IOA	PE5, TM22IOB	PE3, TM21IOB	PD3, TM13IO	VDD2	PC2, SY0OT2	PB4, BR	PA4, SBO7	PA0, SB16	VSS	P85, ICR5	P60, IRQ8	P80, ICR0	N.D.	N.D.	V
TDO	PV2, SBTA	PV1, SBOA	PE6, TM23IOA	PE2, TM21IOA	PD4, TM14IO	PD1, TM11IO	PC7, SY1OT3	PC1, SY0OT1	PB5, BG	PB1, IRQ13	PA5, SBT7	PA3, SB17	P92, ICR10	P86, ICR6	VSS	P62, IRQ10	P63, IRQ11	P61, IRQ9	U
PV0, SB1A	PG6, AN6	VREFL	TMS	PF0, TM24IOA	PE4, TM22IOA	PE7, TM23IOB	PE1, TM20IOB	PD0, TM10IO	PC0, SY0OT0	PB0, IRQ12	P93, ICR11	P94, ICR12	VDD2	P82, ICR2	P84, ICR4	P54, IRQ4	P33, D27, SBT2	N.C.*2 (VDDF)	T
PV3, ADTRG	VSS	PG2, AN2	VDD	TRST	N.D.	VDD	N.C.*1 (VSS)	VSS	PC5, SY1OT1, SBO8	PC3, SY0OT3	PB3, WDOVF	PA1, SBO6	N.C.*1 (VSS)	P90, ICR8	P56, IRQ6	P34, D28, SB13	P25, D21, SBT0	P57, IRQ7	R
PG3, AN3	AVDD	PG4, AN4	VREFH	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P52, IRQ2	P43, PWM4	P53, IRQ3	P51, IRQ1	P	
PG7, AN7	PG5, AN5	PH2, AN10	PG1, AN1	PG0, AN0	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P50, IRQ0	P55, IRQ5	P41, PWM2, TM11O	VSS	P40, PWM1, TM10O	N
PH5, AN13	PH3, AN11	PH4, AN12	PH1, AN9	PH0, AN8	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P36, D30, SBT3	P42, PWM3, TM2IO	P37, D31, PWM0	VDDH	P35, D29, SBO3	M
PI5, AN21	PI3, AN19	PH7, AN15	PI1, AN17	PI0, AN16	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P27, D23, SBO1	VSS	P31, D25, SB12	P32, D26, SBO2	P30, D24, SBT1	L
AVSS	PI7, AN23	PH6, AN14	PI4, AN20	PI6, AN22	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P21, D17, SBOB	P24, D20, SBO0	P23, D19, SB10	P22, D18, SBTB	P26, D22, SB11	K
VSS	PM1, CS1	PI2, AN18	VDD	P70, AN24	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P12, D10	P16, D14	N.C.*1 (VSS)	P20, D16, SB1B	VSS	J
PM3, ADM3, CS3	PNO, WEO, SDQM0	PM0, CS0	PM4, CS4	VSS	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P10, D8	VDDH	P17, D15	P13, D11	N.C.*2 (VDDF)	H
PN2, SYSCLK	VSS	PM5, RWSEL	PN4, DK	VDD	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P02, D2	VSS	P15, D13	P07, D7	P11, D9	G
PO0, ADM0, A0	VDD	PM2, CS2	PN5, AS	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	VSS	P00, D0	P06, D6	P03, D3	P05, D5	F
VDD	POS, ADM5, A5	PN1, WET, SDQM1	PO1, ADM1, A1	VSS	N.D.	PVSS	MMOD1	VSS	PK3, TM33IO	PL2, TM5IO	PR1, A20, KI1	PR7, KI7, PWM5	N.D.	PT1, SBO9	VOUT	P04, D4	P14, D12	P01, D1	E
PO3, ADM3, A3	PO2, ADM2, A2	PN3, RE	PO7, ADM7, A7	VSS	RST	VDDH	CKSEL	VDD	PK4, TM34IO	PL3, TM6IO	PR2, A21, KI2, SWE	PS0, SB14	VSS	PS5, SBT5	PS3, SB15	VDDH	VOUT	electrode (pin none)	D
PO6, ADM6, A6	VDD	PP2, ADM10, A10	PO4, ADM4, A4	PP4, ADM12, A12	PK1, TM31IO	PK5, TM35IO	PK7, TM37IO	PK0, TM30IO	PL1, TM4IO	PL4, TM7IO	PQ0, A16	PQ2, A18	VDDH	PR4, A23, KI4, SDCLKO	PU0, WE2, SCAS	NMIRQ	VDDH	VSS	C
N.D.	N.D.	PP6, ADM14, A14	P0, EXMOD0	PP3, ADM11, A11	PP7, ADM15, A15	P11, EXMOD1	FRQS	PK2, TM32IO	PK6, TM36IO	PL5, PWM6	PR0, A19, KI0	PR5, A24, KI5, SDCLKI	PS2, SBT4	PT0, SB19	PS1, SB04	LON	N.D.	N.D.	B
N.D.	N.D.	PP0, ADM8, A8	PP1, ADM9, A9	PP5, ADM13, A13	PVDD	MMOD0	OSCO	OSCI	PL0, TM3IO	VSS	PQ1, A17	PR3, A22, KI3, SCKE	PR6, A25, KI6	PS4, SBO5	PT2, SBT9	PU1, WE3, SRA5	N.D.	N.D.	A
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

MBGA360-C-1313A *Lead-free

* N.D. has an electrode (pin) but N.C. is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* Each of VDDH, VDD, VDDB, VDDF, VDD2, and VSS has multiple electrodes (pins). Connect the same electrode names to the same power supply.

*1: Connect the J3, R6, and R12 pins to the VSS for the MN103SF33N.

*2: Connect the H1 and T1 pins to the VDDF power for the MN103SF33N.

Support Tool

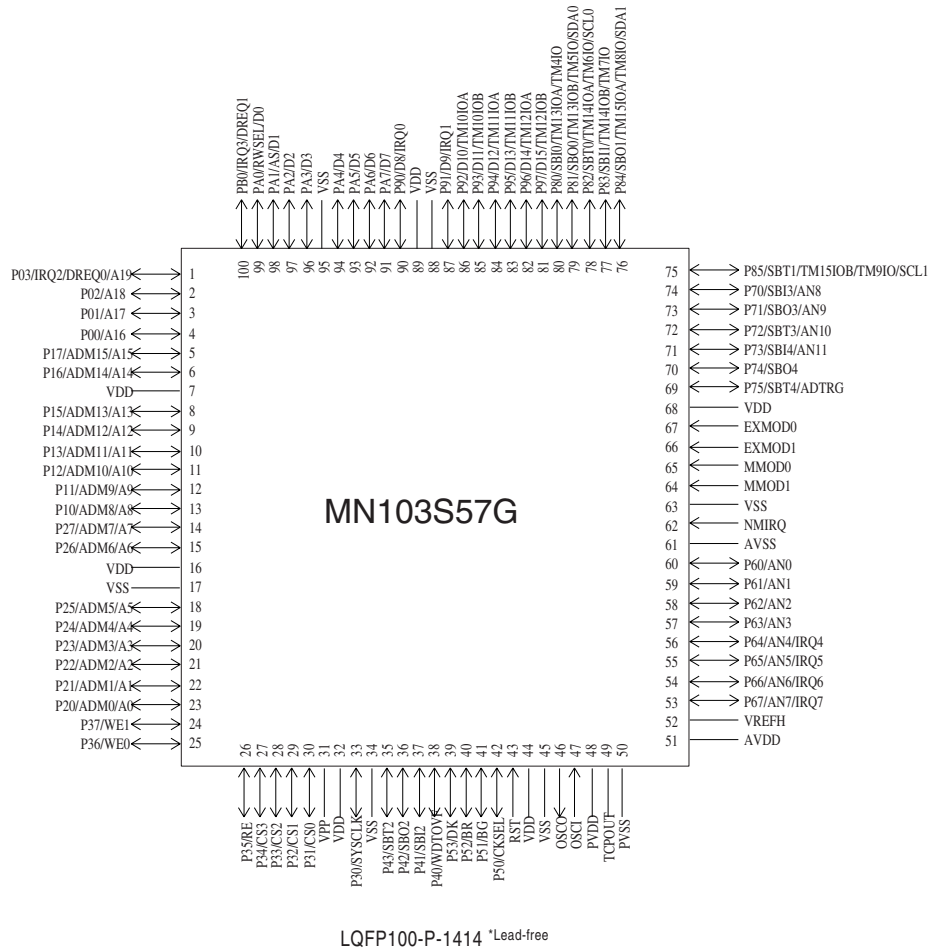
■ In-circuit Emulator	PX-ICE103S33	Not applicable to MBGA360-C-1313A
■ On-board Development Tools	PX-ODB103S-O	
■ Flash Memory Built-in Type	Type	MN103SF33N
	Command ROM (× 64-bit)	512 K-byte
	Data RAM (× 32-bit)	24 K-byte
	Minimum instruction execution time	24.3 ns (at 2.3 V to 2.7 V, 41 MHz)
	Package	MBGA360-C-1313A ^{*Lead-free}

MN103S33N □

□ MN103S57G

Type	MN103S57G	
Command ROM (×64-bit)	128 K-byte	
Data RAM (×32-bit)	16 K-byte	
Package	LQFP100-P-1414 *Lead-free	
Minimum Instruction Execution Time	25.0 ns (at 3.0 V to 3.6 V, 40 MHz)	
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ × 8 • NMI • Timer × 28 • SIF × 10 • I²C × 2 • DMA × 12 • WDT • A/D • System error 	
Timer Counter	<p>8-bit timer × 10</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Up-down count Input capture function PWM generating function Compare/capture register 2-ch. <p>Watchdog timer × 1</p>	
DMA Controller	<p>Number of channels: 4</p> <p>Unit of transfer: 8/16/32 bits</p> <p>Max. Transfer cycles: 65535</p> <p>Starting factor: external interrupt, timer factor, serial transmission/reception factor, I²C transmission/reception factor, external transmission request factor, A/D conversion finish, software factor</p> <p>Transfer method: 2-bus cycle transfer</p> <p>Addressing modes: fixed, increment, decrement</p> <p>Transfer modes: word transfer, burst transfer, intermittent transfer</p>	
Serial Interface	<p>UART/synchronous/multi-master I²C interface selective: 2</p> <p>UART/synchronous interface selective: 3</p>	
I/O Pins	I/O	73 • Common use
A/D Inputs	10-bit × 12-ch.	
Electrical Characteristics	T.B.D.	

Pin Assignment



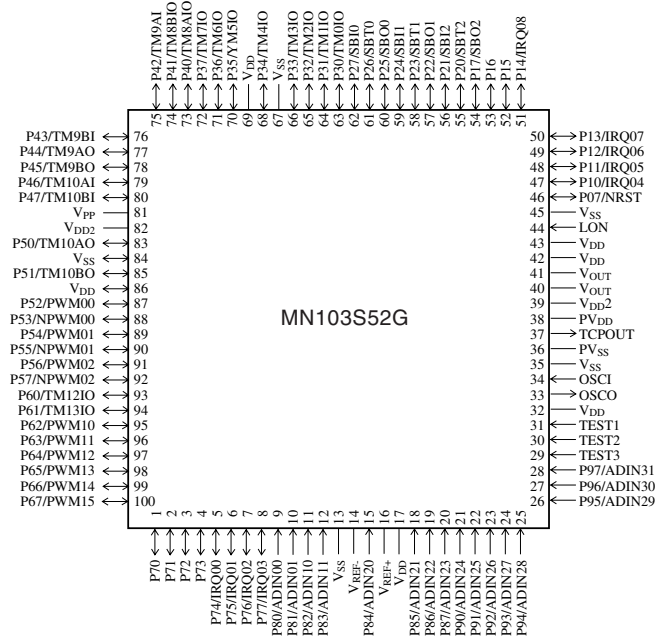
Support Tool

In-circuit Emulator	PX-ICE103S57	
On-board Development Tools	PX-ODB103-O	
Flash Memory Built-in Type	Type	MN103SF57G
	Command ROM (× 64-bit)	128 K-byte
	Data RAM (× 32-bit)	16 K-byte
	Minimum instruction execution time	25.0 ns (at 3.0 V to 3.6 V, 40 MHz)
	Package	LQFP100-P-1414A *Lead-free

□ MN103S52G

Type	MN103S52G		
Internal ROM	128 K-byte		
Internal RAM	4 K-byte SRAM		
Package	QFP100-P-1818B *Lead-free		
Minimum Instruction Execution Time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz) *at internal 4 times oscillation used)		
Interrupts	<ul style="list-style-type: none"> • 9 external interrupts • 42 internal interrupts (watch dog timer, timer, serial I/F, PWM, A/D, system error) 		
Timer Counter	<p>Ten 8-bit timers Interval timer, Event counter, Cascading</p> <p>Four 16-bit timers Interval timer, Event counter, PWM output, Double buffer Watch dog timer</p>		
Serial Interface	UART (full duplex) / synchronous interfaces selective: 3		
I/O Pins	I/O	56	exclusive: 8, selective: 48
	Input	16	selective: 16
A/D Inputs	10-bit, 2 inputs: 2, 12 inputs: 1 Minimum conversion time 1.5us		
PWM	3-phase PWM output 16-bit counter, triangular waveform or jigsaw waveform dead time setup, Double buffer		
Electrical Characteristics	T.B.D.		

Pin Assignment



QFP100-P-1818B *Lead-free

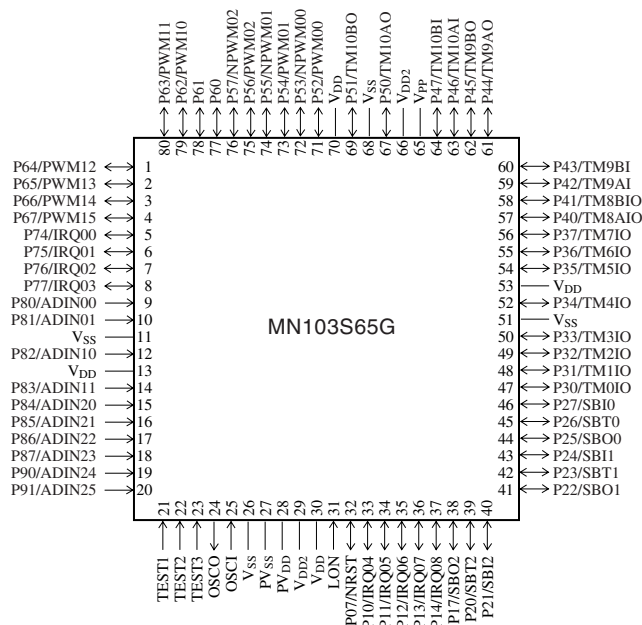
Support Tool

In-circuit Emulator	PX-ICE-103S52	
On board Debugger	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF52G
	ROM	128 K-byte
	RAM	4 K-byte SRAM
	Minimum instruction execution time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz)
	Package	QFP100-P-1818B *Lead-free

□ MN103S65G

Type	MN103S65G		
Internal ROM	128 K-byte		
Internal RAM	4 K-byte SRAM		
Package	LQFP080-P-1414A *Lead-free		
Minimum Instruction Execution Time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz) *at internal 4 times oscillation used)		
Interrupts	<ul style="list-style-type: none"> • 9 external interrupts • 42 internal interrupts (watch dog timer, timer, serial I/F, PWM, A/D, system error) 		
Timer Counter	<p>Eight 8-bit timers Interval timer, Event counter, Cascading</p> <p>Four 16-bit timers Interval timer, Event counter, PWM output, Double buffer</p> <p>Watch dog timer</p>		
Serial Interface	UART (full duplex) / synchronous interfaces selective: 3		
I/O Pins	I/O	50	exclusive: 2, selective: 48
	Input	10	selective: 10
A/D Inputs	10-bits, 2 inputs: 2, 6 inputs: 1 Minimum conversion time 1.5 μ s		
PWM	3-phase PWM output 16-bit counter, triangular waveform or jigsaw waveform dead time setup, Double buffer		
Electrical Characteristics	T.B.D.		

Pin Assignment



LQFP080-P-1414A *Lead-free

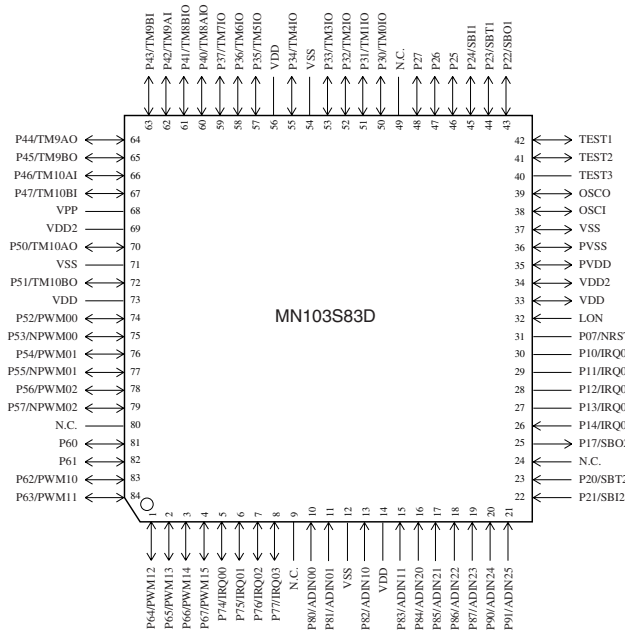
Support Tool

In-circuit Emulator	PX-ICE-103S52	
On board Debugger	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF65GAL
	ROM	128 K-byte
	RAM	4 K-byte SRAM
	Minimum instruction execution time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz)
	Package	LQFP080-P-1414A *Lead-free

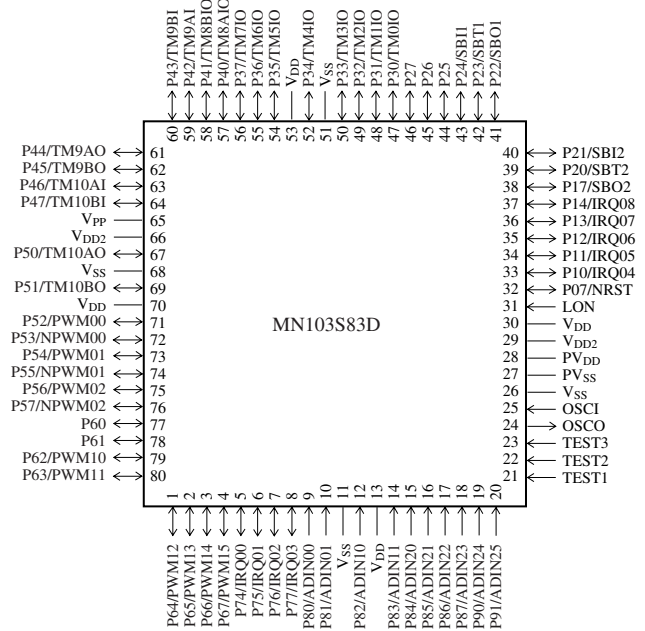
□ MN103S83D

Type	MN103S83D		
Internal ROM	64 K-byte		
Internal RAM	2 K-byte SRAM		
Package	QFP084-P-1818E ^{*Lead-free} , LQFP080-P-1414A ^{*Lead-free} (under development)		
Minimum Instruction Execution Time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz) *at internal 4 times oscillation used)		
Interrupts	<ul style="list-style-type: none"> • 9 external interrupts • 40 internal interrupts (watch dog timer, timer, serial I/F, PWM, A/D, system error) 		
Timer Counter	<p>Eight 8-bit timers Interval timer, Event counter, Cascading</p> <p>Four 16-bit timers Interval timer, Event counter, PWM output, Double buffer</p> <p>Watch dog timer</p>		
Serial Interface	Two UART (full duplex) / synchronous interfaces selective		
I/O Pins	I/O	50	exclusive: 5, selective: 45
	Input	10	selective: 10
A/D Inputs	10-bits, 2 inputs: 2, 6 inputs: 1 Minimum conversion time 1.5 μ s		
PWM	3-phase PWM output 16-bit counter, triangular waveform or jigsaw waveform dead time setup, Double buffer		

Pin Assignment



QFP084-P-1818E *Lead-free
QFP084-P-1818I *Lead-free



LQFP080-P-1414A *Lead-free (under development)

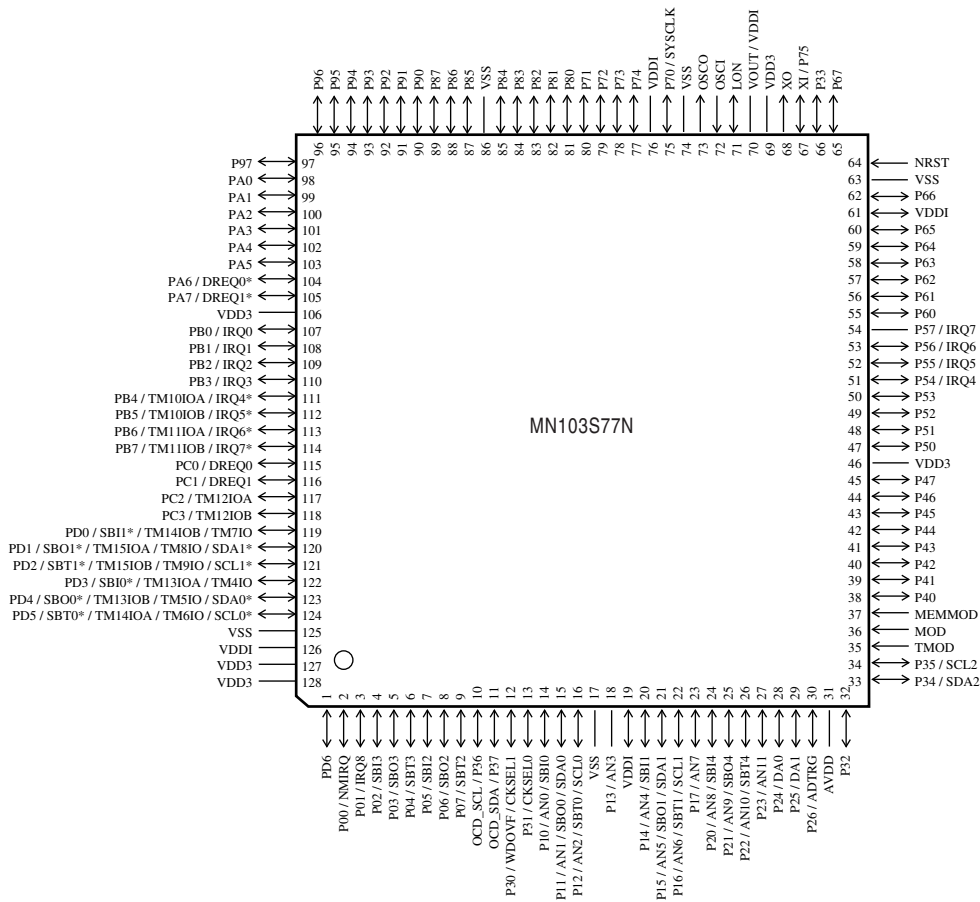
Support Tool

In-circuit Emulator	PX-ICE-103S52	
On board Debugger	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF65GBF, MN103SF65GAL
	ROM	128 K-byte
	RAM	4 K-byte SRAM
	Minimum instruction execution time	25 ns (at 4.3 V to 5.5 V, 10 MHz internal regulator used) 25 ns (at 3.0 V to 3.6 V, 10 MHz)
	Package	QFP084-P-1818I *Lead-free, LQFP080-P-1414A *Lead-free

□ MN103S77N

Type	MN103S77N (under development)		
Command ROM (×64-bit)	512 K-byte		
Data RAM (×32-bit)	32 K-byte		
Package	LQFP128-P-1818C *Lead-free		
Minimum Instruction Execution Time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)		
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ × 9 • NMI • Timer × 28 • SIF × 10 • I²C × 3 • Time base timer × 1 • DMA × 12 • WDT • A/D • System error 		
Timer Counter	<p>8-bit timer × 10</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Up-down count Input capture function PWM generating function Compare/capture register 2-ch. <p>Time base timer × 1</p> <p>Watchdog timer × 1</p>		
DMA Controller	<p>Number of channels: 4</p> <p>Unit of transfer: 8/16/32 bits</p> <p>Max. Transfer cycles: 65535</p> <p>Starting factor: external interrupt, timer factor, serial transmission/reception factor, I²C transmission/reception factor, external transmission request factor, A/D conversion finish, software factor</p> <p>Transfer method: 2-bus cycle transfer</p> <p>Addressing modes: fixed, increment, decrement</p> <p>Transfer modes: word transfer, burst transfer, intermittent transfer</p>		
Serial Interface	<p>UART/synchronous/multi-master I²C interface selective: 2</p> <p>UART/synchronous interface selective: 3</p> <p>Multi master I²C: 1</p>		
I/O Pins	I/O	104	• Common use
A/D Inputs	10-bit × 12-ch.		
D/A Outputs	8-bit × 4-ch.		
ROM Collection	8-ch.		
Electrical Characteristics	T.B.D.		

Pin Assignment



LQFP128-P-1818C *Lead-free

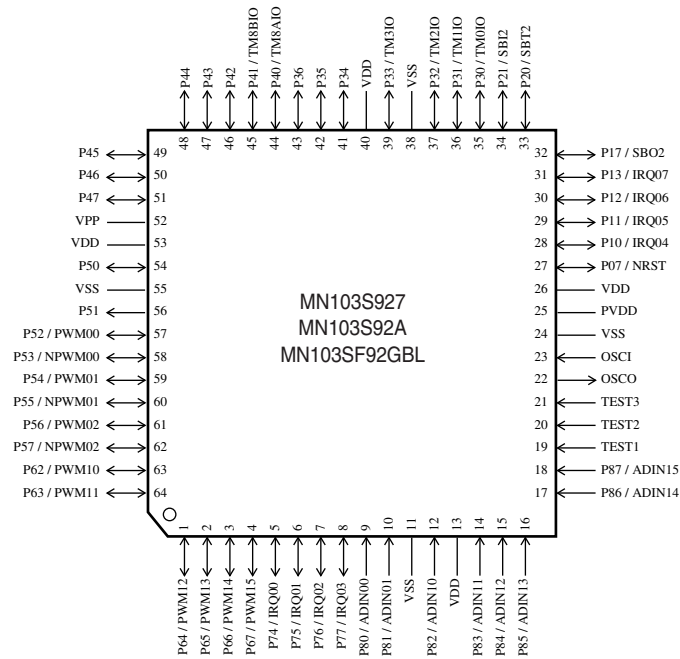
Support Tool

In-circuit Emulator	PX-ICE103S77	
On-board Development Tools	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF77R (under development)
	Command ROM (× 64-bit)	1024 K-byte
	Data RAM (× 32-bit)	32 K-byte
	Minimum instruction execution time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)
	Package	LQFP128-P-1818C *Lead-free

□ MN103S927, MN103S92A

Type	MN103S927 (under development)		MN103S92A (under development)
Internal ROM	16 K-byte		32 K-byte
Internal RAM	2 K-byte SRAM		
Package	LQFP064-P-1414 *Lead-free		
Minimum Instruction Execution Time	25 ns (at 3.0 V to 3.6 V, 10 MHz) *at internal 4 times oscillation used)		
Interrupts	<ul style="list-style-type: none"> • 8 external interrupts • 18 internal interrupts (watch dog timer, timer, serial I/F, PWM, A/D, system error) 		
Timer Counter	8-bit timer × 4 Interval timer, Event counter, Cascading 16-bit timer × 2 Interval timer, Event counter, PWM output, Double buffer Watch dog timer		
Serial Interface	Two UART (full duplex) / synchronous interfaces selective		
I/O Pins	I/O	41	exclusive: 11, selective: 30
	Input	8	selective: 8
A/D Inputs	10-bits, 2 inputs: 1, 6 inputs: 1 Minimum conversion time 1.5 us		
PWM	3-phase PWM output 16-bit counter, triangular waveform or jigsaw waveform dead time setup, Double buffer		

Pin Assignment



LQFP064-P-1414 *Lead-free

Support Tool

In-circuit Emulator	PX-ICE-103S92	
On board Debugger	PX-ODB103-DO	
Flash Memory Built-in Type	Type	MN103SF92G (under development)
	ROM	128 K-byte
	RAM	4 K-byte SRAM
	Minimum instruction execution time	25 ns (at 3.0 V to 3.6 V, 10 MHz)
	Package	LQFP064-P-1414 *Lead-free

□ MN103S97N

Type	MN103S97N (under development)		
Command ROM (×64-bit)	512 K-byte		
Data RAM (×32-bit)	24 K-byte		
Package	MBGA255-C-1111A *Lead-free		
Minimum Instruction Execution Time	16 ns (at 1.65 V to 1.95 V, 60 MHz)		
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ × 11 • NMI • Key input • Timer × 40 • Input capture × 16 • PWM × 5 • SIF × 17 • DMA × 12 • WDT • A/D • System error 		
Timer Counter	<p>8-bit timer × 8</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) <p>8-bit timer with PWM × 8</p> <ul style="list-style-type: none"> Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) PWM generating function <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Up-down count Input capture function PWM generating function Compare/capture register 2-ch. <p>16-bit timer × 6</p> <ul style="list-style-type: none"> Reload-down count <p>Watchdog timer × 1</p>		
DMA Controller	<p>Number of channels: 4</p> <p>Unit of transfer: 8/16/32 bits</p> <p>Max. Transfer cycles: 65535</p> <p>Starting factor: external interrupt, timer factor, PWM factor, serial transmission / reception factor, A/D conversion finish, software factor</p> <p>Transfer method: 2-bus cycle transfer</p> <p>Addressing modes: fixed, increment, decrement</p> <p>Transfer modes: word transfer, burst transfer, intermittent transfer</p>		
Serial Interface	<p>Serial 0, 1, 3 to 6: start-stop synchronization / synchronization commonly used, 6 lines</p> <p>Serial 2: start-stop synchronization / synchronization commonly used: 16 bytes containing transmission/reception FIFO</p> <p>I2CO: I²C serial interface, multi master transmission/reception function</p>		
I/O Pins	I/O	170	• Common use
	Input	25	• Common use
A/D Inputs	10-bit × 25-ch.		
PWM	12-, 14-bit resolution × 5-ch.		
ICR	28-bit × 13-ch. + 16-bit × 6-ch. (common with timer)		
OCR	16-bit × 12-ch. (common with timer)		
Timer Synchronous Output	4-bit (synchronous output) × 2-ch.		

Electrical Characteristics

Parameter	Symbol	Condition	Limit		Unit
			typ	max	
Operating Supply current	IDD1	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = 15 MHz, PLL = ON	55(TBD)	85(TBD)	mA
	IDDH1	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = 15 MHz, PLL = ON	10(TBD)	20(TBD)	mA
Supply current at STOP	IDD4	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = oscillation stopped Tj = 85°C		150(TBD)	μA
	IDDH4	VDD = 1.95 V VDDDB, VDDH, AVDD = 3.6 V fosc = oscillation stopped Tj = 85°C		5(TBD)	μA

(Ta = -20°C to +85°C, VSS = AVSS = 0.0 V)

A/D Converter Performance

Parameter	Condition	Limit			Unit
		min	typ	max	
Resolution				10	Bits
A/D conversion absolute error	A/D Conversion clock = 5 MHz			±7(TBD)	LSB
A/D conversion relative error				±4(TBD)	LSB
A/D conversion time		2.4			μs

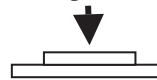
(Ta = -20°C to +85°C, AVDD = 3.0 V, AVSS = 0.0 V)

Pin Assignment

N.D	PL4 / A12 / ADM12	PM1 / ICR1	PM0 / ICR0	PN0 / ICR8	PO1	PP4 / D4	PP7 / D7	PQ5 / D13	PQ7 / D15	PP5 / D5	PR5 / TM22IOB	PR7 / TM23IOB	PSS / BG	PT0 / A16	N.D	T
PL3 / A11 / ADM11	PL6 / A14 / ADM14	PM3 / ICR3	PM4 / ICR4	PM2 / ICR2	PN2 / ICR10	PP1 / D1	PQ1 / D9	PQ6 / D14	PR4 / TM22IOA	PR3 / TM21IOB	PS3 / WE2	PS2 / WDOVF	PT2 / A18	PU5 / A24 / K15	PU7 / K17	R
PK7 / A7 / ADM7	PL7 / A15 / ADM15	PM7 / ICR7	PM6 / ICR6	PM5 / ICR5	PN4 / ICR12	PP3 / D3	PQ3 / D11	PR1 / TM20IOB	PS1	PU1 / A20 / K11	PU3 / A22 / K13	PT1 / A17	PU2 / A21 / K12	P03 / D19 / SB11	PU0 / A19 / K10	P
PK5 / A5 / ADM5	PK4 / A4 / ADM4	PO0	PN1 / ICR9	PL5 / A13 / ADM13	PL1 / A9 / ADM9	PP0 / D0	PP6 / D6	PQ0 / D8	PQ4 / D12	PS4 / WE3	PR0 / TM20IOA	P01 / D17 / SB07	P05 / D21 / SBT1	P04 / D20 / SB01	P13 / D27 / SB03	N
PI5 / AS	PL0 / A8 / ADM8	PI3 / RE	PL2 / A10 / ADM10	PK6 / A6 / ADM6	PN3 / ICR11	PP2 / D2	PQ2 / D10	PR6 / TM23IOA	PR2 / TM21IOA	PS0 / PWM4	PU4 / A23 / K14	P07 / D23 / SB12	P12 / D26 / SB13	PU6 / A25 / K16	P00 / D16 / SB10	M
PI1 / CS1	P4 / DK	PK3 / A3 / ADM3	PK1 / A1 / ADM1	PK2 / A2 / ADM2	PK0 / A0 / ADM0	VDDDB	VDDDB	VDDDB	VSS	PS6 / BR	P10 / D24 / SBO2	P11 / D25 / SBT2	P14 / D28 / SBT3	P06 / D22	P02 / D18 / SBT0	L
*2 N.C [VREFH]	PI5 / RWSEL	PI1 / WE1	PI2 / SYSCLK	PI2 / CS2	PI0 / WE0	VSS	VDDH	VDD	VDD	P20 / SBI4	P21 / SBO4	*1 N.C (VDDH)	P16 / D30	VDDDB	P15 / D29	K
AVDD	PG5 / AN21	PI0 / CS0	PI3 / CS3	PH0 / AN24	PI4 / CS4	VSS	VDDH	VDD	VSS	P31 / IRQ1	P36 / IRQ6	P24 / SBO5	P23 / SBI5	P22 / SBT4	P17 / D31	J
PG2 / AN18	PG4 / AN20	PG1 / AN17	PG6 / AN22	PG0 / AN16	PG3 / AN19	VSS	VDDH	VDD	VSS	P33 / IRQ3	P25 / SBT5	P34 / IRQ4	VSS	VDDH	OSCI	H
PF4 / AN12	PF0 / AN8	PG7 / AN23	PF6 / AN14	PF1 / AN9	PF5 / AN13	VSS	VDDH	VOUT	VSS	N.C ^{*3}	P35 / IRQ5	N.C ^{*3}	N.C ^{*3}	P32 / IRQ2	OSCO	G
PF2 / AN10	PE4 / AN4	PE7 / AN7	PE6 / AN6	PE3 / AN11	PE3 / AN3	P82 / SYOOT2	VSS	VSS	VSS	P41 / IRQ9	P37 / IRQ7	P50 / NMIRQ	MMOD1	P30 / IRQ0	N.C ^{*4}	F
PE2 / AN2	PE0 / AN0	PE1 / AN1	PF7 / AN15	PE5 / AN5	PB1 / TM110 / PWM2	P90 / SB16	P80 / SYOOT0	P66 / TM36IO	P72 / TM12IO	N.C ^{*6} [TRCD1]	P70 / TM10IO	MMOD0	P53 / FRQS0	P42 / IRQ10	N.C ^{*5}	E
PD3 / TM25IOB	PD1 / TM24IOB	PCS / SCL0	PA0 / ADTRG	P94	P92 / SBT6	P84 / SY1OT0	P74 / TM14IO	P73 / TM13IO	P64 / TM34IO	P62 / TM32IO	N.C ^{*6} [EXTRG1]	N.C ^{*3}	P52 / EXMOD	P51 / EXMOD0	P40 / IRQ8	D
PC1	AVSS	PD0 / TM24IOA	PB5 / TM5IO	PB7 / TM7IO	PB4 / TM4IO	P93	P85 / SY1OT1	P63 / TM33IO	N.C ^{*6} [EXTRG0]	N.C ^{*6} [TRCLK]	TDO	N.C ^{*6} [TRCST]	NRST	FRQS1	N.D	C
PC3 / PWM0	PD2 / TM25IOA	PC4 / SDA0	PB3 / TM3IO	PB6 / TM6IO	P95	P87 / SY1OT3	P86 / SY1OT2	P75 / TM15IO	P65 / TM35IO	N.C ^{*6} [TRCD0]	P60 / TM30IO	N.C ^{*6} [TRCD3]	TMS	TRST	CKSEL / P55	B
N.D	PC2	PC0	PB2 / TM2IO / PWM3	PB0 / TM0IO / PWM1	P91 / SBO6	P83 / SYOOT3	P81 / SYOOT1	P71 / TM11IO	P67 / TM37IO	P61 / TM31IO	N.C ^{*6} [TRCD2]	TCK	TDI	LON	N.D	A

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Perspective



MBGA255-C-1111A *Lead-free

* ND has an electrode (pin) but NC is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

Each of VDD, VDDDB, VDDH, and VSS has multiple electrodes (pins). Connect the same electrode names to the same power supply.

[]: Not available with MN103S97N.

*1 Connect the K4 pin to the VDDH power for the MN103SF66R.

*2 Connect the K16 pins to the AVDD power for the MN103SF66R.

*3 D4, G3, G4 and G6 pins have signal electrodes for the MN103SF66R. Perform the necessary pin processing.

*4 F1 pin should be pull-down, or pull-up to the VDDH power for the MN103SF66R.

*5 E1 pin should be open for the MN103SF66R.

*6 A5, B4, B6, C4, C6, C7, D5 and E6 pins are debugging pins. Perform the necessary pin processing.

Support Tool

On-board Development Tools	PX-ODBAMD (on-board debug unit)	
Flash Memory Built-in Type	Type	MN103SF66R (under development)
	Command ROM (× 64-bit)	1024 K-byte
	Data RAM (× 32-bit)	40 K-byte
	Minimum instruction execution time	16 ns (at 1.65 V to 1.95 V, 60 MHz)
	Package	MBGA255-C-1111A *Lead-free

AM33^{32-bit} SERIES

AM33 (MN103E) Series

The AM33 (MN103E) series is a group of 32-bit microprocessors suitable for multimedia uses such as movie, voice, graphics and communication. Its C-language-oriented architecture and C compiler which optimizes and outputs instruction code realize high performance with minimum power consumption. High system performance is attained by enhanced data processing capability by DSP commands and high data transmission capacity by adoption of a crossbar switch.

Features

- **32-bit RISC architecture**
 - Upward compatible AM3 (MN103) microprocessor
 - Enhanced OS support function by MMU
 - Built-in DSP commands
- **Elimination of bus bottleneck by the crossbar switch**
 - 2-bus configuration consisting of highly expansible general-purpose bus and high-speed bus

□ MN103E010HRA, MN103E040HYB

Type	MN103E010HRA	MN103E040HYB
Instruction Cache	16 K-byte (4-way, set-associative)	
Data Cashe	16 K-byte (4-way, set-associative)	
SRAM Used by Both Instructions and Data	16 K-byte	
Package	BGA292-P-2727 *Lead-free	FLGA424-C-1717 *Lead-free
Minimum Instruction Execution Time	7.5 ns (at 1.8 V tolerance = ± 5%, 133 MHz)	
Interrupts	<ul style="list-style-type: none"> • XIRQ × 8 • NMI • Timer × 14 • DMAC × 4 • WDT • A/D • SIO × 6 • I²C × 2 • IrDA • Softmodem • Realtime clock • Asynchronous bus error 	
Timer Counter	<p>8-bit timer × 4 (all down counters)</p> <p style="padding-left: 20px;">Cascade connection possible (usable as a 16/24/32-bit timer)</p> <p style="padding-left: 20px;">Timer output possible (Duty = 1:1)</p> <p style="padding-left: 20px;">Internal clock source or external clock source selectable</p> <p style="padding-left: 20px;">Selectable as a serial interface clock</p> <p>16-bit timer × 7 (down counters)</p> <p style="padding-left: 20px;">Cascade connection possible (usable as a 32-bit timer)</p> <p style="padding-left: 20px;">Timer output possible (Duty = 1:1)</p> <p style="padding-left: 20px;">Internal clock source or external clock source selectable</p> <p style="padding-left: 20px;">Partially selectable as a serial interface clock</p> <p>16-bit timer × 1 (up counter)</p> <p style="padding-left: 20px;">Internal clock source or external clock source selectable</p> <p style="padding-left: 20px;">Input capture function (rising edge, falling edges, or both selectable)</p> <p style="padding-left: 20px;">PWM generating function (compare/capture register × 2 contained)</p> <p>Watchdog timer × 1</p>	
DMA Contoroller	<p>Number of channels: 4</p> <p>Transfer unit: 1/2/4/16 byte</p> <p>Maximum number of bytes transferred: 1Mbyte</p> <p>Start factor: External request, interrupt, software</p> <p>Transfer mode: 2-bus cycle transfer</p> <p>Transfer mode: Batch transfer, intermittent transfer</p> <p>Addressing mode:</p> <p style="padding-left: 20px;">Source/destination each fixed, increment/decrement specification possible</p> <p style="padding-left: 20px;">Increment/decrement automatically executed according to the transfer unit</p>	
Serial Interface	<p>UART/synchronous (co-used) × 2-ch.</p> <p>UART (with CTS control) × 1-ch.</p>	
I/O Pins	I/O	34 • Common use : 33
FPU (floating point unit)	<ul style="list-style-type: none"> • Data types complying with the IEEE754 standard supported • Round to the nearest mode complying with the IEEE754 standard supported • 32 single-precision floating point operation registers (FS0-FS31) <li style="padding-left: 20px;">These can also be referenced as 16 double-precision floating point operation registers (FD0-FD30) • Floating point operation exceptions (5 types) and floating point unload instruction exceptions complying with the IEEE754 standard supported 	
Memory Management Function	<p>32-entry full-associative TLB loaded (instructions/data separated from each other)</p> <p>Address conversion by paging (page size: 1 K-byte, 4 K-byte, 128 K-byte, 4 M-byte variable)</p>	
On-chip Bus Controller	Concurrent access from three types of master devices to four types of slave devices possible	

System Bus Interface	External memory space allocation to 8 banks possible The external interface can use the built-in memory, RAM, ROM, SDRAM interfaces
Memory Bus Interface	SDRAM directly connected interface contained
Soft Modem Interface	<ul style="list-style-type: none"> • Interface with an external AFE (analog front end) • Output data parallel-serial conversion, input data serial-parallel conversion • Send/receive FIFO contained (16-bit width, 16 steps) • NCU control via the parallel IO port
Real-time Clock	<ul style="list-style-type: none"> • Clock/calendar function • Interrupt: periodic, alarm, update ended • BCD/binary accommodated • Leap year automatic correcting function • 24-hour/12-hour selectable • Daylight saving time mode accommodated
A/D Converter	<ul style="list-style-type: none"> • 10-bit charge re-distribution mode (error: $\pm 4\text{LSB}$) • Number of channels: 8-channel
IrDA Interface	<ul style="list-style-type: none"> • IrDA 1.0 SIR (-115.2 Kb/s, half-duplex) • IrDA 1.1 MIR ($0.576, 1.152\text{ Mb/s}$, half-duplex) • IrDA 1.1 FIR (4.0 Mbp/s, half-duplex) • UART (-1.5 Mbp/s, full-duplex) • 48 MHz clock input (baud rate generating function contained)
I²C Interface	2 ports Master-slave interface (multi-master supported) 3.3 V interface (open drain output)

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	I_{DD18A}	VDD18 = 1.8 V ; VDD33, PVDD, AVDD, RVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1:0] = 0.0 ; Output open	-	-	460	mA
Supply current at stopping	I_{DD18D}	VDD18 = 1.89 V ; VDD33, PVDD, AVDD, RVDD = 3.465 V fOSC = Stop ; FRQS[1:0] = 0.0 ; Output open ; Tj = 70°C	-	-	50	mA

(Ta = -20°C to +70°C)

A/D conversion performance

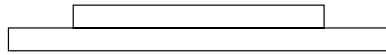
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution			-	-	10	Bit
A/D conversion relative error		VREFH = 3.3 V	-	-	± 4	LSB
A/D conversion differential non-linear error		Conversion reference clock = 4.166 MHz	-	-	± 4	LSB
A/D conversion time			2.6	-	-	μs

(Ta = -20°C to +70°C, AVDD = 3.3 V \pm 0.165 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

Pin Assignment

Perspective



ND	XSWE1	XSCS6	XSCS2	XSCS1	SD29	SD27	VDD18	SD21	SD19	SD14	VDD18	SD6	SD1	CLK48	PIO1[3]	PIO1[1]	PIO1[0]	ND		21		
	XSWE3	SD31	XSCS7	SD30	XSAS	SD23	SD22	SD17	SD16	SD9	SD8	SD3	SD4	PIO5[1]	PIO5[2]	PIO1[4]	PIO1[2]	ND			20	
RCLKI	XSCS3	XSWE0	XSWE2	XSCS0	XSCS4	SD28	SD25	SD24	SD18	VDD33	SD15	SD11	SD10	VDD33	PIO0[7]	PIO5[0]	AN1	AN3	AN7	VREFH	19	
RCLKO	PIO2[0]	PWROK	ND	ND	ND	SD26	SD20	SD13	SD12	SD7	SD2	SD0	SD5	PIO0[1]	ND	ND	ND	AN5	PIO0[5]	AVSS	18	
RVDD	PIO2[4]	PIO2[2]	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	AN6	AN0	AN2	17	
TCPOUT	PIO2[3]	XSDK	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO0[3]	XIRQ7	AN4	16	
PVDD	SSZ0	XSBG	VDD33	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	XIRQ4	SBT2	PIO0[4]	AVDD	15
PVSS	SA4	SA2	XSCS5	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	SBO0	XIRQ5	XNMI	XIRQ2	14
OSCI	SA10	SA5	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	ND	SBO1	XIRQ0	PIO0[6]	PIO0[2]	13
OSCO	SA17	SA11	SA0	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	VDD33	XRESET	PIO0[0]	XIRQ6	12	
SYSCLK	SA18	SA12	XSRE	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	TRCST	VDD33	XIRQ3	VDD18	11	
PIO2[1]	SRXW	SSZ1	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	SB11	SB12	SBO2	XIRQ1	10	
XSBR	SA1	SA3	SA14	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	PIO3[2]	PIO3[3]	XRSTOUT	VDD18	09	
VDD18	SA6	SA7	SA8	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO3[0]	PIO3[1]	SBT0	SBT1	08	
SA9	SA13	SA15	SA22	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	TRST MOD	PIO4[0]	PIO4[2]	SB10	07	
SA16	SA19	SA21	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO4[1]	PIO3[4]	TCK	06	
VDD18	SA23	VDD33	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	TRCD1	PIO4[3]	TDI	05	
SA27	SA26	SA24	ND	ND	ND	VDD33	VDD18	VDD33	VDD33	VDD33	VDD33	VDD18	TRCD2	TRCD7	ND	ND	ND	TRCD5	TMS	TDO	04	
SA29	SA31	SA25	SA20	SA28	MA4	MA1	MA7	MA13	MA11	MA12	XMBE0	MD9	MD4	MD12	MD1	MD15	TRCD4	TRCD0	EXTRG	TRCLK	03	
ND	SA30	MA3	MA5	MA0	MA8	MA14	XMCS1	SDCKE	XMWE	XMCA5	MD6	MD10	MD11	MD2	MD14	TRCD3	TRCD6	ND			02	
	NP	MA2	MA6	MA10	MA9	XMCS0	XMRAS	SDCLK	XMBE1	MDK	MD7	MD8	MD5	SDCKI	MD3	MD13	MD0	ND				01
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA		

FLGA424-C-1717 *Lead-free

* ND has an electrode (pin) but N.C. is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* The NDs on the four corners are the lands intended for reinforcement. You are required to connect them to the PCB.

* NP (No pin.) has no electrode.

Pin Assignment(Continue)

Perspective

TRCD6	TRCD1	TDO	TRST MOD	PIO4[2]	PIO3[2]	SBI0	SBO1	SBT1	SBT2	XRST OUT	XIRQ1	XIRQ4	XIRQ5	PIO0[0]	PIO0[4]	AVDD	AN4	AVSS	VREFH	20
TRCD3	EXTRG	TCK	PIO4[0]	PIO3[0]	PIO3[3]	SBO0	SBI1	SBI2	XIRQ0	XIRQ2	XNMI	XIRQ7	PIO0[2]	PIO0[6]	AN6	AN2	AN1	PIO1[2]	PIO5[0]	19
TRCD7	TRCD4	TRCD0	TDI	TMS	PIO4[1]	PIO3[1]	PIO3[4]	SBT0	SBO2	XRESET	XIRQ3	XIRQ6	PIO0[1]	PIO0[5]	AN7	AN3	AN0	PIO1[1]	PIO5[2]	18
MD0	TRCD2	TRCD5	VSS	VSS	PIO4[3]	VDD18	VDD33	VSS	VDD18	VDD33	VSS	PIO0[3]	VSS	PIO0[7]	AN5	PIO1[0]	PIO1[3]	PIO5[1]	CLK48	17
MD13	TRC CLK	TRCST	VSS													VSS	PIO1[4]	SD3	SD0	16
MD3	MD14	MD15	VSS													SD2	SD1	SD6	SD4	15
sdcki	MD2	MD1	VDD33													VDD33	SD5	SD9	SD7	14
MD5	MD11	MD12	VD18	VSS						VSS						VSS	SD8	SD12	SD10	13
MD8	MD10	MD4	VDD33	VSS						VSS						VDD18	SD11	SD15	SD13	12
MD7	MD6	MD9	VSS	VSS						VSS						VDD33	SD14	SD17	SD16	11
MDK	XMCA5	XMBE0	VDD33	VSS						VSS						VSS	SD23	SD18	SD19	10
XMBE1	XMWE	MA12	VSS	VSS						VSS						VDD18	SD21	SD20	SD22	09
SDCLK	SDCKE	MA11	VDD18	VSS						VSS						VSS	SD25	SD24	SD26	08
XMRAS	XMCE1	MA13	VDD33	VSS						VSS						VDD33	SD29	SD27	SD28	07
XMCS0	MA14	MA7	VDD33	VSS						VSS						XSCS2	XSAS	SD30	SD31	06
MA9	MA8	MA1	VSS	VSS						VSS						VSS	XSCS3	XSCS0	XSCS1	05
MA10	MA0	MA4	VSS	VSS	SA22	VDD18	VDD33	VSS	VDD33	SA0	XSBR	XSRE	VDD18	VDD33	VSS	VSS	XSCS6	XSCS4	XSCS5	04
MA6	MA5	SA31	SA26	SA23	SA19	SA16	SA13	SA9	SA10	SA1	XSBG	PIO2[4]	PIO2[3]	PIO2[0]	VSS	XSWE3	XSWE0	XSCS7	RCLKI	03
MA2	MA3	SA28	SA25	SA21	SA18	SA15	SA12	SA8	SA6	SA2	SSZ0	SRXW	PIO2[2]	PIO2[1]	TCP OUT	PWROK	XSWE2	XSWE1	RCLKO	02
SA30	SA29	SA27	SA24	SA20	SA17	SA14	SA11	SA7	SA5	SA4	SA3	SSZ1	XSDK	SYS CLK	OSCO	OSCI	PVSS	PVDD	RVDD	01
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

BGA292-P-2727 *Lead-free

Support Tool

ROM Emulator PARTNER-ETII (KMC product)

On-board Development Tools
 PX-ODB103E-J (On-board debug unit)
 PX-ODB-AMT-20 (Trace unit)
 PARTNER-J (KMC product)

□ MN103E0600YD

Type	MN103E0600YD (under development)
Instruction Cache	16 K-byte (4-way, set-associative)
Data Cashe	16 K-byte (4-way, set-associative)
Package	MLGA239-C-1111
Minimum Instruction Execution Time	7.5 ns (at 1.8 V tolerance = ±5% , 133 MHz)
Interrupts	• XIRQ × 8 • NMI • Timer × 14 • DMAC × 4 • WDT • SIO × 6 • I ² C × 2 • Asynchronous bus error
Timer Counter	<p>8-bit timer × 4 (all down counters)</p> <p>Cascade connection possible (usable as a 16/24/32-bit timer)</p> <p>Timer output possible (Duty = 1:1)</p> <p>Internal clock source or external clock source selectable</p> <p>Selectable as a serial interface clock</p> <p>16-bit timer × 7 (down counters)</p> <p>Cascade connection possible (usable as a 32-bit timer)</p> <p>Timer output possible (Duty = 1:1)</p> <p>Internal clock source or external clock source selectable</p> <p>Partially selectable as a serial interface clock</p> <p>16-bit timer × 1 (up counter)</p> <p>Internal clock source or external clock source selectable</p> <p>Input capture function (rising edge, falling edges, or both selectable)</p> <p>PWM generating function (compare/capture register × 2 contained)</p> <p>Watchdog timer × 1</p>
DMA Contoroller	<p>Number of channels: 4</p> <p>Transfer unit: 1/2/4/16 byte</p> <p>Maximum number of bytes transferred: 1Mbyte</p> <p>Start factor: External request, interrupt, software</p> <p>Transfer mode: 2-bus cycle transfer</p> <p>Transfer mode: Batch transfer, intermittent transfer</p> <p>Addressing mode:</p> <p>Source/destination each fixed, increment/decrement specification possible</p> <p>Increment/decrement automatically executed according to the transfer unit</p>
Serial Interface	<p>UART/synchronous (co-used) × 2-ch.</p> <p>UART (with CTS control) × 1-ch.</p>
I/O Pins	I/O
	19 • Common use : 19
On-chip Bus Controller	Concurrent access from three types of master devices to four types of slave devices possible

System Bus Interface	External memory space allocation to 8 banks possible
Memory Bus Interface	SDRAM directly connected interface contained
I²C Interface	2 ports Master-slave interface (multi-master supported) 3.3 V interface (open drain output)

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	I _{DD18A}	VDD18 = 1.8 V ; VDD33, PVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1:0] = 0.0 ; Output open	–	–	460	mA
Supply current at stopping	I _{DD18D}	VDD18 = 1.89 V ; VDD33, PVDD = 3.465 V fOSC = Stop ; FRQS[1:0] = 0.0 ; Output open ; T _j = 70°C	–	–	70	mA

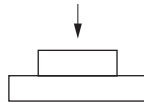
(T_a = –20°C to +70°C)

See the next page for pin assignment and support tool.

Pin Assignment

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
16	ND		XSCS5	XSCS2	SD31	SD27	SD21	SD17	SD12	SD8	SD6	SD1	XIRQ7	SD2		ND
15			XSCS0	XSCS7	SD28	SD29	SD25	SD19	SD13	SD11	SD4	SD3	SD7	XIRQ6		
14	TCP OUT	PIO0[0]	XSCS6	XSCS3	XSDK	SD26	SD24	SD23	SD15	SD18	SD14	SD9	SD0	PIO1[1]	PIO1[3]	PIO1[0]
13	PVDD	XSWE2	PIO0[1]	XSCS4	XSCS1	VDD33	SD22	SD20	SD16	VDD18	SD10	SD5	XIRQ5	PIO1[2]	XIRQ4	XRST OUT
12	PVSS	XSAS	XSWE0	PIO0[2]	VSS	VSS	SD30	VSS	VSS	VDD33	VSS	XNMI	XIRQ1	XIRQ0	XIRQ2	XRE SET
11	OSCI	SRXW	XSWE3	XSWE1	VDD33	VDD18	VSS	VDD33	ND	ND	VSS	XIRQ3	SBT2	SBO2	PIO1[4]	SBI2
10	OSCO	SA1	XSRE	VDD18	VSS	ND	ND	ND	ND	ND	VDD18	PIO1[5]	PIO2[7]	PIO2[5]	PIO2[1]	SBI1
09	SYS CLK	SA3	SA0	VSS	VDD33	ND	ND	ND	ND	ND	VDD33	VSS	PIO2[3]	PIO1[7]	PIO1[6]	SBI0
08	SA2	SA5	SA7	SA8	VSS	ND	ND	ND	ND	ND	ND	VSS	TMS	PIO2[6]	PIO2[4]	PIO2[2]
07	SA9	SA11	SA14	SA4	VDD18	VDD33	ND	ND	ND	ND	ND	VDD33	EXTRG	TRST MOD	TCK	PIO2[0]
06	SA12	SA16	SA6	SA10	SA15	VSS	VSS	VSS	VDD33	VSS	VDD18	VDD18	TRCD6	TRCD7	TDI	TDO
05	SA17	SA20	SA13	SA18	SA21	VSS	VDD33	XMRAS	XMBE1	MD9	VSS	VSS	VSS	TRCD4	TRCD3	TRCD5
04	SA19	SA22	SA24	SA26	VDD33	MA8	MA14	MA12	XMWE	MD6	VDD33	MD12	VDD33	TRCD2	TRCD1	TRC CLK
03	SA23	SA25	SA27	VSS	MA6	MA10	MA9	XMCS1	XMCAS	MD8	MD10	MD3	MD1	MD15	TRCST	TRCD0
02	ND		MA3	MA2	MA1	MA7	VDD18	XMCS0	SDCKE	MD7	MD5	MD11	MD13	MD0		ND
01			NP	MA4	MA5	MA0	MA13	MA11	SDCLK	XMBE0	SDCKI	MD4	MD2	MD14		

Perspective



* ND has an electrode (pin) but NC is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* The NDs on the four corners are the lands intended for reinforcement. You are required to connect them to the PCB.

* NP (No pin.) has no electrode.

Support Tool

■ ROM Emulator	PARTNER-ETII (KMC product)
■ On-board Development Tools	PX-ODB103E-J (On-board debug unit) PX-ODB-AMT-20 (Trace unit) PARTNER-J (KMC product)

ARM7^{32-bit} SERIES

The ARM7 (MN1A7) are 32-bit microcomputers with the ARM7TDMI as the core in the ARM RISC processor family being accepted as the de facto standard in the mobile communication field centering around the portable telephones.

The series features excellent balance between high performance and low cost and power consumption, realizes high code density (also supporting 16-bit instruction set) while providing a variety of peripheral functions to cope with a wide range of applications including multimedia equipment.

Features

● 32-bit ARM7TDMI architecture

Simple, high-efficiency instruction set

High code generation efficiency using ARM 32-bit and thumb 16-bit instructions

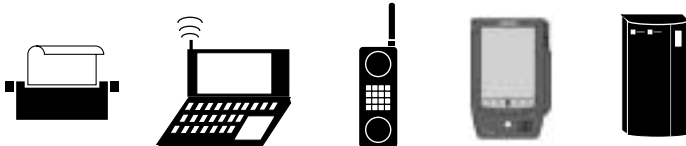
High-speed instruction execution by ARM7TDMI architecture in 3-stage pipeline configuration

High-speed execution of branch instruction

● Rich development environment thanks to abundant middleware, OS and design support tools

ARM7 (MN1A7) Series

■ Application



□ MN1A7T0200

Type	MN1A7T0200
ROM (x8-bit / x16-bit / x32-bit)	Max. 16 M in total
RAM (x8-bit / x16-bit / x32-bit)	External ROM and RAM
Package	FLGA152-C-1111 *Lead-free
Minimum Instruction Execution Time	100 ns (at 2.3 V to 2.7 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ0 to 5 • NMI • Timer 0 to 9 underflow • Timer 8 to 9 compare capture A • Timer 8 to 9 compare capture B • Serial ch.0 to 2 transmission • Serial ch.0 to 2 reception • Serial ch.0 to 2 in communication state • Serial ch.0 to 2 modem status • Serial ch.0 to 2 character • Serial ch.3 to 4 transmission • Serial ch.3 to 4 reception • WDT • A/D conversion finish
Timer Counter	<p>Timer counter 0: 16-bit × 1 (interval timer, event count, interrupt, A/D conversion trigger) Clock source PS0 underflow; PS1 underflow; external clock Interrupt source timer counter 0 underflow</p> <p>Timer counter 1 to 6: 16-bit × 1 (interval timer, event count, timer output, interrupt) Clock source PS0 underflow; PS1 underflow; external clock Interrupt source timer counter 1, 2, 3, 4, 5 or 6 underflow</p> <p>Timer counter 7: 16-bit × 1 (interval timer, event count, timer output, interrupt) Clock source PS0 underflow; PS1 underflow; external clock input; timer 6 cascade input Interrupt source timer counter 7 underflow</p> <p>*: timer counter 6 or 7 can be changed in configuration into a 32-bit timer counter.</p> <p>Timer counter 8: 16-bit × 1 (interval timer, event count, output compare, PWM output, one-shot output, input capture, interrupt) Clock source PS0 underflow; PS1 underflow; external clock input Interrupt source timer counter 8 underflow; coincidence with compare capture A or at capture; coincidence with compare capture B or at capture</p> <p>Timer counter 9: 16-bit × 1 (interval timer, event count, output compare, PWM output, one-shot output) Clock source PS0 underflow; PS1 underflow; external clock input Interrupt source timer counter 9 underflow; coincidence with compare capture A or at capture; coincidence with compare capture B or at capture</p> <p>Pre-scaler counters: 2 lines</p>
Serial Interface	<p>Serial 0, 1, 2 (UART): 5-, 6-, 7-, 8-bit × 3 Clock source baud rate generator; IOCLKH; external clock</p> <p>Serial 3, 4 (SSD): 4- to 16-bit × 2 Clock source IOCLKH; external clock</p>
I/O Pins	40 • Common use
A/D Inputs	10-bit × 8-ch.
PWM	16-bit × 2-ch.
ICR	16-bit × 2-ch.
OCR	16-bit × 2-ch.

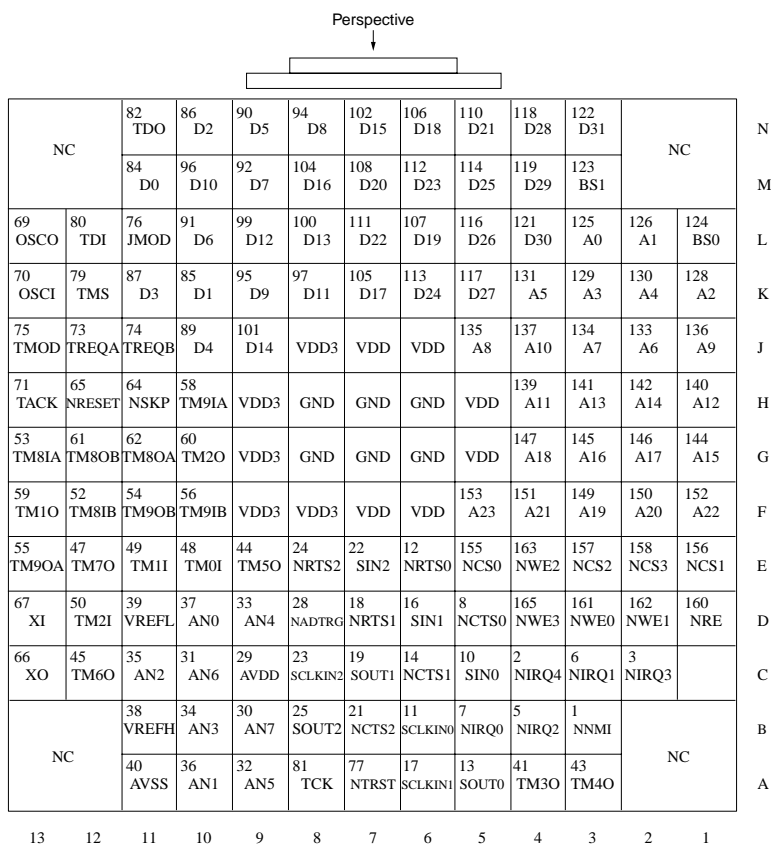
Electrical Characteristics

A/D Characteristic

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREFH = 3.0 V VREFL = 0.0 V A/D conversion clock = 6 MHz			± 5	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.0		24	μs

(Ta = 25°C, AVDD = 3.0 V, AVSS = 0 V)

Pin Assignment



FLGA152-C-1111 *Lead-free

Support Tool

- In-circuit Emulator** Advice (YDC product) (applicable to 16- or 8-bit bus mode), UniSTAC (Sophia Systems Co.,Ltd. product)
- On-board Development Tools** Multi-ICE (ARM product), JEENI (Embedded Performance Inc. product, TOYO Corporation dealings), Logic Analyzer (Agilent Technologies product) NEXTiCE for ARM7(Computex Co., Ltd. product)
- ROM Emulator** PARTNER-ETII (KMC product) NEXTiCE for ARM7(Computex Co., Ltd. product)

1500 4-bit SERIES

The MN1500 Series could be called the standard for 4-bit microcomputers. In addition to the general purpose I/O ports, this series also provides numerous peripheral functions for analog interface such as LCD drive, fluorescent display, telephone, etc., and meets to wider range of applications.

Features

● 4-bit Standard Microcomputer

Execution speed: 1 μ s to 2 μ s (4 MHz)

Maximum ROM capacity: 16 K-byte

RAM: 64 to 512 nibbles

Package: 20 pins to 100 pins

● Large Family Line-Up

With analog interface for household apparatus, remote control, telephone, TV channel selection, FLP display and LCD drive.

● Application in ASICs

The standard CMOS core is now being applied in ASICs.

MN1500 Series

■ Application



□ MN15G1601

Type	MN15G1601		
ROM (x8-bit)	16 K		
RAM (x4-bit)	512		
Package	LQFP064-P-1414 *Lead-free		
Number of Instructions	103		
Minimum Instruction Execution Time	0.5 μs at 1/4 frequency dividing (at 3.0 V to 5.5 V, 8 MHz) 1.0 μs at 1/4 frequency dividing (at 2.4 V to 5.5 V, 4 MHz) 2.0 μs at 1/8 frequency dividing (at 2.0 V to 5.5 V, 4 MHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V.		
Interrupts	• RESET • IRQ1 • IRQ2 • IRQ3		
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (event count, pulse output, simple pulse width measurement, PWM output, remote control carrier output) Clock source 1/2, 1/8, 1/32, 1/128 of system clock frequency; 1/1, 1/4, 1/16, 1/64 of XI(OSC) oscillation clock frequency</p> <p>Timer counter 1 : 8-bit × 1 (event count, pulse output, remote control carrier output) Clock source 1/2 of system clock frequency; 1/1, 1/2¹⁴ of OSC oscillation clock frequency; 1/1, 1/2⁶ of XI oscillation clock frequency Possible 16-bit cascade connection with timer counter 0</p> <p>Timer counter 2 : 8-bit × 1 (event count, pulse output, simple pulse width measurement, PWM output, remote control carrier output, one-shot timer output, trigger start PWM output, trigger start timer output) Clock source 1/2 of system clock frequency; 1/1, 1/2 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; TCI input</p> <p>Timer counter 3 : 8-bit × 1 (event count, pulse output, remote control carrier output, high-functional PWM output) Clock source 1/2 of system clock frequency; 1/1, 1/2 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency; TCI input Possible 16-bit cascade connection with timer counter 2</p> <p>Watchdog timer</p>		
Serial Interface	Serial : 8-bit × 1 (synchronous type) Clock source 1/1, 1/2 of system clock frequency; SBT pin input		
I/O Pins	I/O	35	• Common use : 31 • Specified pull-up resistor available : 27 (software programmable) • Specified output architecture available : Nch open drain / push-pull : 31 (software programmable)
A/D Inputs	10-bit × 8-ch. (with S/H)		
LCD	30 segments × 4 commons (1/2, 1/3, 1/4 duty)		
Zero-Cross Inputs	1		
Special Ports	Buzzer output (1 kHz, 2 kHz, 4 kHz : fosc = at 4 MHz)		

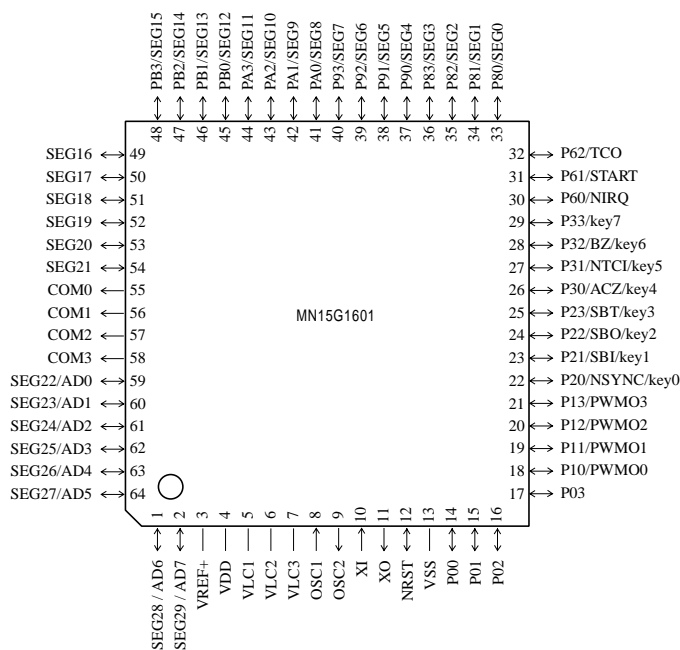
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz (1/8 dividing)		1.8	3.5	mA
	IDD2	fosc = 4 MHz (1/8 dividing)		1.2	2.5	mA
	IDD3	fosc = 32.768 kHz (1/8 dividing)		9.0	20	μA
Supply current at HALT	IDD4	fosc = 4 MHz (1/8 dividing)		0.3	0.6	mA
	IDD5	fosc = 32.768 kHz (1/8 dividing)		1.5	8.0	μA
Supply current at STOP	IDD6	ACZ = 1/2 VDD, Ta = 25°C		4.0	10	μA
	IDD7	ACZ = 1/2 VDD, Ta = -40°C to +85°C			30	μA
	IDD8	Ta = 25°C			1.0	μA
	IDD9	Ta = -40°C to +85°C			5.0	μA

(Ta = -40°C to +85°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment



LQFP064-P-1414 *Lead-free

SupportTool

In-circuit Emulator	PX-ICE1500 + PX-PRB15G1601-LQFP064-P-1414	
EPROM Built-in Type	Type	MN15GP1601
	ROM (× 8-bit)	16 K
	RAM (× 4-bit)	512
	Minimum instruction execution time	0.5 μs at 1/4 frequency dividing (at 3.0 V to 5.5 V, 8 MHz) 1.0 μs at 1/4 frequency dividing (at 2.4 V to 5.5 V, 4 MHz) 2.0 μs at 1/8 frequency dividing (at 2.3 V to 5.5 V, 4 MHz)
	Package	LQFP064-P-1414 *Lead-free

□ MN15G0202 , MN15G0402

Type	MN15G0202	MN15G0402
ROM (x8-bit)	2 K	4 K
RAM (x4-bit)	128	128
Package (Conventional Package)	SOP020-P-0300D *Lead-free (SOP020-P-0300)	
Number of Instructions	103	
Minimum Instruction Execution Time	0.5 μs at 1/4 frequency dividing (at 3.0 V to 5.5 V, 8 MHz) 1.0 μs at 1/4 frequency dividing (at 2.4 V to 5.5 V, 4 MHz) 2.0 μs at 1/8 frequency dividing (at 2.0 V to 5.5 V, 4 MHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V.	
Interrupts	• RESET • IRQ1 • IRQ2 • IRQ3	
Timer Counter	Timer counter 2 : 8-bit × 1 (pulse output, PWM output) Clock source 1/2, 1/8, 1/32, 1/128 of system clock; 1/1, 1/4, 1/16, 1/64 of OSC oscillation clock Timer counter 3 : 8-bit × 1 (pulse output, high-functional PWM output) Clock source 1/2 of system clock; 1/1, 1/2 ⁶ , 1/2 ¹⁴ of OSC oscillation clock Timer counter 2 can be cascade-connected. Watchdog timer	
I/O Pins	I/O	15 • Common use : 11 • Specified pull-up resistor available : 7 (software programmable) • Specified output architecture available : Nch open drain / push-pull : 11 (software programmable) • 4-ch. LED direct drive available (15 mA / 1.0 V)
A/D Inputs	10-bit × 4-ch. (with S/H)	
Zero-Cross Input	1	
Special Ports	Buzzer output (1 kHz, 2 kHz, 4 kHz : fosc = at 4 MHz)	
Notes	Auto-Reset circuit selectable (none, circuit 1, circuit 2) (mask option)	

Electrical Characteristics

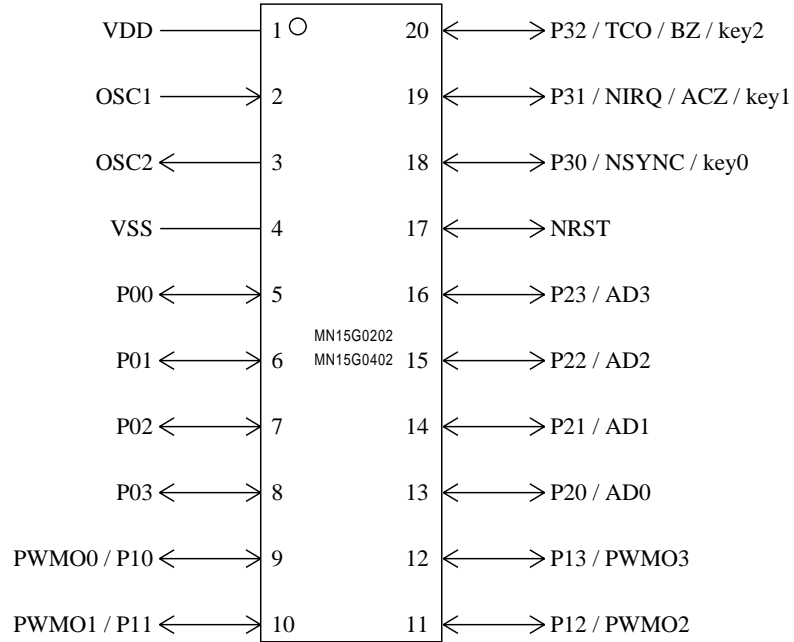
Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 8 MHz (1/8 dividing)		1.5	3.0	mA
	IDD2	fosc = 4 MHz (1/8 dividing)		1.2	2.5	mA
Supply current at HALT	IDD3	fosc = 4 MHz (1/8 dividing)		0.3	0.6	mA
Supply current at SOTP	IDD4	ACZ = 1/2 VDD, Ta = 25°C		3.0	10.0	μA
	IDD5	ACZ = 1/2 VDD, Ta = -40°C to +85°C			20.0	μA
	IDD6	Ta = 25°C			1.0	μA
	IDD7	Ta = -40°C to +85°C			5.0	μA
Auto reset current consumption	IDD8			4.0	8.0	μA

(Ta = -40°C to +85°C, VDD = 5.0 V, VSS = 0 V)

Pin Assignment

() : Conventional Package



SOP020-P-0300D *Lead-free
(SOP020-P-0300)

Support Tool

In-circuit Emulator	PX-ICE1500 + PX-PRB15G0202 / 0402-SOP020-P-0300	
EPROM Built-in Type	Type	MN15GP0402 [ES (Engineering Sample) available]
Note) • Because of a special writing system, only a particular writer model manufactured by Data I/O is applicable. • The mask option applies only to no auto reset circuit. (No other options are set.)	ROM (× 8-bit)	4 K
	RAM (× 4-bit)	128
	Minimum instruction execution time	0.5 μs at 1/4 frequency dividing (at 3.0 V to 5.5 V, 8 MHz)
		1.0 μs at 1/4 frequency dividing (at 2.4 V to 5.5 V, 4 MHz)
2.0 μs at 1/8 frequency dividing (at 2.3 V to 5.5 V, 4 MHz)		
Package	SOP020-P-0300D *Lead-free	
(Conventional Package)	(SOP020-P-0300)	

□ MN15G0804

Type	MN15G0804		
ROM (x8-bit)	8 K		
RAM (x4-bit)	512		
Package	QFP044-P-1010E *Lead-free		
Number of Instructions	103		
Minimum Instruction Execution Time	0.96 ms at 1/4 frequency dividing (at 2.4 V to 5.5 V, 32 kHz) 1.91 ms at 1/8 frequency dividing (at 2.0 V to 5.5 V, 32 kHz)* * The lower limit for operation guarantee for EPROM built-in type is 2.3 V. V _{RST} when using auto reset.		
Interrupts	• RESET • IRQ1 • IRQ2 • IRQ3		
Timer Counter	<p>Timer counter 0 : 8-bit × 1 (event count, pulse output) Clock source 1/2 of system clock frequency; RMO; TCO2; TCI input</p> <p>Timer counter 1 : 8-bit × 1 (event count, pulse output) Clock source 1/2 of system clock frequency; fout1; TCO0; fx1 Possible 16-bit cascade connection with timer counter 0</p> <p>Timer counter 2 : 8-bit × 1 (event count, pulse output) Clock source 1/2 of system clock frequency; RMO; fx1; TCI input</p> <p>Time base timer</p> <p>Watchdog timer</p>		
I/O Pins	I/O	34	<ul style="list-style-type: none"> • Common use : 34 • Specified pull-up resistor available : 34 (software programmable) • Specified output architecture available : Nch open drain / push-pull : 34 (software programmable)
LCD	30 segments × 4 commons (1/2, 1/3, 1/4 duty)		
Remote Control Output	Duty and period are variable.		
Notes	Auto reset circuit selectable (mask option)		

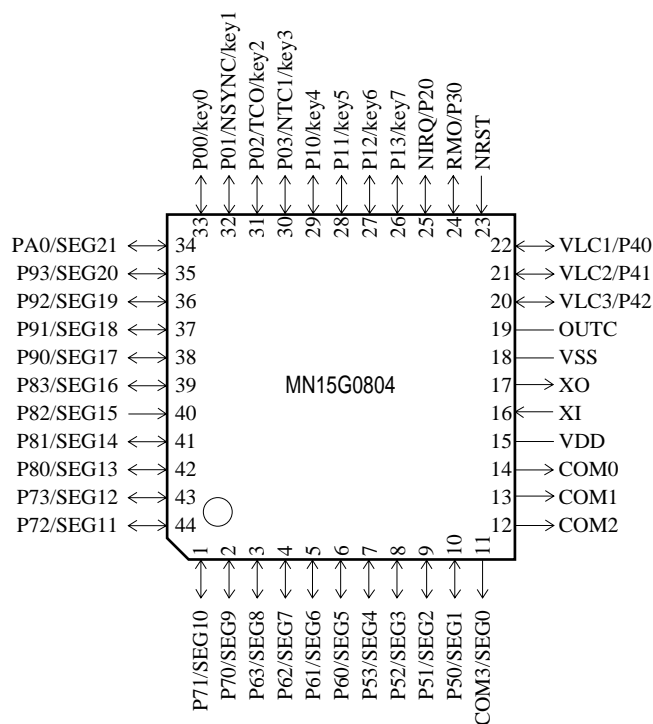
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	$f_{x1} = 32.768 \text{ kHz}$ (1/8 dividing) when using multiply circuit		3.0	5.0	mA
	IDD2	$f_{x1} = 32.768 \text{ kHz}$ (1/8 dividing)		10	40	μA
Supply current at HALT	IDD3	$f_{x1} = 32.768 \text{ kHz}$ (1/8 dividing)		3	15	mA
Supply current at STOP	IDD6	$f_{x1} = 32.768 \text{ kHz}$		2.0	5.0	μA
	IDD7	$f_{x1} = \text{Stop}$		1.0	3.5	μA
Auto reset power consumption	IDD9			3.0	6.0	μA

($T_a = -10^\circ\text{C}$ to $+60^\circ\text{C}$, $V_{DD} = 3.0 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Pin Assignment



QFP044-P-1010E *Lead-free

Support Tool

In-circuit Emulator	PX-ICE1500 + PX-PRB15G1604-QFP044-P-1010E	
EPROM Built-in Type	Type	MN15GP1604
	ROM (× 8-bit)	16 K
	RAM (× 4-bit)	512
	Minimum instruction execution time	0.96 μs at 1/4 frequency dividing (at 2.4 V to 5.5 V, 32 kHz) 1.91 μs at 1/8 frequency dividing (at 2.3 V to 5.5 V, 32 kHz)
	Package	QFP044-P-1010E *Lead-free

Development Support Tools

Development Support Tools

Development Support Tools

● AM1 (MN101) Series of 8-bit Microcomputers

	AM1 (MN101C) Series	AM14 (MN101D) Series	AM13E (MN101E) Series
C Compiler and Assembler	ANSI C compiler with extensions for 8-bit microcomputers (8-bit internal computation and bit fields within chars)		
Debuggers	C source code debuggers for Windows®		
Emulator	In-circuit emulator supporting real-time debugging with 224 KB (944 KB) of ROM and 16 KB (64 KB) of RAM, trace function, break functions, etc. ():MN101E Series		
Middleware	ADPCM codec	—	—
Software Simulator	Tool for debugging without the actual machine (DebugFactory)	—	—

● AM2 (MN102) Series of 16-bit Microcomputers

	AM22 (MN102H) Series
C Compiler and Assembler	ANSI C compiler with linear address space
Debuggers	C source code debuggers for Windows®
Emulator	In-circuit emulator supporting real-time debugging with emulation function for up to 1.8 megabytes extended RAM.

● AM3 (MN103) Series of 32-bit Microcomputers

	AM30 (MN1030), AM32 (MN103S) Series	AM33 (MN103E) Series
Compiler and Assembler	Conforms to ANSI C compiler Conforms to EC++ compiler	
Debuggers	C source code debuggers for Windows®	
Emulator	In-circuit emulator supporting real-time debugging with 1 megabyte (256 kilobytes) of ROM and up to 4 megabytes (1 megabyte) of RAM, trace function, break functions, etc. [():MN1030 Series]	—
Onboard Debugger	Onboard debugging environment providing real-time debugging of target device: This product is effective for field debugging and final evaluation including analog characteristics.	Onboard debugging environment providing real-time debugging of target device: memory display/modification functions, break functions, trace functions, etc.
Middleware	JPEG decoder / encoder, ADPCM codec	JPEG decoder / encoder, ADPCM codec, MP3 decoder, AAC decoder, MPEG4 decoder, USB host stack, G.726 codec

*1:This set includes a Computex debugger.

● Operating Environment

	SUN/SPARC	Windows	
		98 / Me	2000 / XP
Compiler and Assembler	○ *1	○	○ *2
Debuggers and Emulator	—	○	○

★ The middleware is independent of operating environment.

*1:Solaris 2.6 or later.
*2:In a DOS box.

Business Partner for Development Support Tools

● AM1 (MN101) Series of 8-bit Microcomputers

Tool Name	Model Number	Description	Developer
In-circuit Emulators	Uni STAC MN101C Series	Set consisting of in-circuit emulator for MN101C series plus Watchpoint debugger for Windows® 95 / 98 / NT. Target probe selections for emulation is option.	Sophia Systems and Technology
	PJ110	Recommended POD Body : AD250 Requires PU952 POD common unit.	Yokogawa Digital Computer Corporation Advice division
Parallel flash memory gang programmer	Y1000-8T	Gang programmer that supports parallel write operations.	Weve Technology Co., Ltd. Sales Department
Onboard flash memory gang programmer	ITF2000	Gang programmer that supports onboard serial write operations.	Interface Co., Ltd. System Instruments Division
Flash on-board serial programmer	NET IMPRESS AF220/AF210	General-purpose in-circuit programmer for flash microcomputer.	Yokogawa Digital Computer Corporation Instruments Business Div.
Flash parallel /on-board serial programmer	AF9708/9709 AF9723(Gang)	Parallel (independent write, gang)/Programmer that supports onboard serial write operations.	ANDO Corporation (Flash Support Group, Inc.)
CPU Evaluation Board	AM1 STARTER KIT	This CPU evaluation board supports evaluation of AM1 (MN101C/E) applications over a USB connection and includes both a compiler and a debugger.	OBJECT Co., Ltd.
Onboard Debugging Environment	AM1 debug Probe	Onboard debugging environment that supports debugging when connected to the AM1 (MN101C/E) microcontroller in a target system Includes a device that already has debugger and monitor routines downloaded and can be connected over a USB connection that does not require a separate power supply.	

● AM22 (MN102H) Series of 16-bit Microcomputers

Tool Name	Model Number	Description	Developer
In-circuit Emulators	MN102H-G	Set consisting of in-circuit emulator for MN102H series plus Watchpoint debugger for Windows® 95 / 98 / NT.	Sophia Systems and Technology
Parallel flash memory gang programmer	Y1000-8T	Gang programmer that supports parallel write operations.	Weve Technology Co., Ltd. Sales Department
Onboard flash memory gang programmer	ITF2000	Gang programmer that supports onboard serial write operations.	Interface Co., Ltd. System Instruments Division
Flash on-board serial programmer	NET IMPRESS AF220/AF210	General-purpose in-circuit programmer for flash microcomputer.	Yokogawa Digital Computer Corporation Instruments Business Div.
Flash parallel /on-board serial programmer	AF9708/9709 AF9723(Gang)	Parallel (independent write, gang)/Programmer that supports onboard serial write operations.	ANDO Corporation (Flash Support Group, Inc.)

● AM30 (MN1030), AM32 (MN103S) Series of 32-bit Microcomputers

Tool Name	Model Number	Description	Developer
C Compilers	GNU Pro	C/C++ compiler based on GNU gcc plus simulator/debugger.	Red Hat, Inc.
	exeGCC	GNU C/C++ compiler for developing high-speed, compact embedded systems.	Kyoto Micro Computer Co., Ltd.
In-circuit Emulators	UniSTAC MN103 series	Set consisting of in-circuit emulator for MN103 series plus Watchpoint debugger for Windows® 95 / 98 / 2000 / NT. MN103 series support available as option.	Sophia Systems and Technology
Parallel flash memory gang programmer	Y1000-8T	Gang programmer that supports parallel write operations.	Weve Technology Co., Ltd. Sales Department
Onboard flash memory gang programmer	ITF2000	Gang programmer that supports onboard serial write operations.	Interface Co., Ltd. System Instruments Division
Flash on-board serial programmer	NET IMPRESS AF220/AF210	General-purpose in-circuit programmer for flash microcomputer.	Yokogawa Digital Computer Corporation Instruments Business Div.
Flash parallel /on-board serial programmer	AF9708/9709 AF9723(Gang)	Parallel (independent write, gang)/Programmer that supports onboard serial write operations.	ANDO Corporation (Flash Support Group, Inc.)
ROM Emulators	PARTNER-ET II	High-speed download at 4 MB/s. Including hardware break functions matching for in-circuit emulators, real-time trace functions, etc. PC card, PCI and LAN interfaces are standard equipment. Includes industry standard source level debugger, PARTNER-ETII / Win.	Kyoto Micro Computer Co., Ltd.
Programmer Adapter	FLS344CSP-103F33	Conversion adapter for connecting a MN103SF33N flash microcomputer to a Flash programmer.	Sunhayato Corporation

※ Business Partner addresses appear the following page.

● AM3 (MN103) Series of 32-bit Microcomputers

Tool Name	Model Number	Description	Developer
C Compilers	GNU Pro	C/C++ compiler based on GNU gcc plus simulator/debugger.	Red Hat, Inc.
	exeGCC	GNU C/C++ compiler for developing high-speed, compact embedded systems.	
ROM Emulators	PARTNER-ET II	High-speed download at 4 MB/s. Including hardware break functions matching for in-circuit emulators, real-time trace functions, etc. PC card, PCI and LAN interfaces are standard equipment. Includes industry standard source level debugger, PARTNER-ETII/Win. JTAG support available with special-purpose option kit.	Kyoto Micro Computer Co., Ltd.
Onboard Debugger	PARTNER-J	USB 2.0 support is standard and models that support LAN connection are also available. Ultrahigh-speed JTAG ICE supports 3 MB/s high-speed downloading. High-capacity trace memory (up to 18 Mbits)	

※ Business Partner addresses appear the following page.

● Common Components

Tool Name	Model Number	Description	Distributor
Surface Mount Sockets	PRB-TETxxxLFxx: Sockets manufactured by Tokyo Eletech Corporation	Sockets that can be mounted directly above a flat foot pattern.	Daimaru Kogyo, Ltd. Technical inquiries: panax@mecse.mec.mei.co.jp
	PRB-SKTxxxQFxx: Sockets manufactured by Yamaichi Electronics Co., Ltd.		

● Package - Surface Mount Socket

Manufacturer	Package	Catalog Number	Socket Manufacturer Catalog Number
Yamaichi Electronics Co., Ltd.	QFP044-P-1010	PRB-SKT44QF10	IC149-044-*24-*5
	QFP064-P-1414	PRB-SKT64QF14	IC149-064-*27-*5
	QFP064-P-1818	PRB-SKT64QF18	IC149-064-1KS-10883
	QFH080-P-1212	PRB-SKT80QF12	IC149-080-*30-*5*
	QFH080-P-1414	PRB-SKT80QF14	IC149-080-*16-*5
	QFP084-P-1818	PRB-SKT84QF18	IC149-084-1KS-10884-*
	QFH100-P-1414	PRB-SKT100QF14	IC149-100-*25-*5
	QFP100-P-1818	PRB-SKT100QF18	IC149-100-1KS-10804B
	QFP128-P-1818	PRB-SKT128QF18	IC149-128-*33-*5*
Tokyo Eletech Corporation	QFH048-P-0707	PRB-TET48TH07	HQPACK048SD, NQPACK048SD
		PRB-TET48TH07-SL	HQPACK048SD, NQPACK048SD-SL
	QFH064-P-1010	PRB-TET64TH10	HQPACK064SD, NQPACK064SD
		PRB-TET64TH10-SL	HQPACK064SD, NQPACK064SD-SL
	LQFP064-P-1414	PRB-TET64LF14	HQPACK064SA160, NQPACK064SA160
		PRB-TET64LF14-SL	HQPACK064SA160, NQPACK064SA160-SL
	QFH080-P-1212	PRB-TET80TH12	HQPACK080SD, NQPACK080SD
	TQFP080-P-1212	PRB-TET80TH12-SL	HQPACK080SD, NQPACK080SD-SL
	LQFP080-P-1414	PRB-TET80LF14	HQPACK080SB160, NQPACK080SB
		PRB-TET80LF14-SL	HQPACK080SB160, NQPACK080SB-SL
	LQFP100-P-1414	PRB-TET100LF14	HQPACK100SD, NQPACK100SD
		PRB-TET100LF14-SL	HQPACK100SD, NQPACK100SD-SL
	QFP100-P-1818	PRB-TET100QF18	HQPACK100SB, NQPACK100SB
		PRB-TET100QF18-SL	HQPACK100SB, NQPACK100SB-SL
	LQFP112-P-2020	PRB-TET112LF20	HQPACK112SB, NQPACK112SB
		PRB-TET112LF20-SL	HQPACK112SB, NQPACK112SB-SL
	TQFP128-P-1414	PRB-TET128LF14	HQPACK128SE, NQPACK128SE
		PRB-TET128LF14-SL	HQPACK128SE, NQPACK128SE-SL
	LQFP128-P-1818	PRB-TET128LF18	HQPACK128SD, NQPACK128SD
		PRB-TET128LF18-SL	HQPACK128SD, NQPACK128SD-SL
QFP160-P-2828	PRB-TET160QF28	HQPACK160SB, NQPACK160SB	
	PRB-TET160QF28-SL	HQPACK160SB, NQPACK160SB-SL	
QFP208-P-2828	PRB-TET208QF28H	HQPACK208SD306H, NQPACK208SD	

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