

# **NS486™SXF Evaluation Board**

## *Theory of Operation*

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## Release Notes

### **27-NOV-95, Initial Release**

### **26-FEB-96, Revised per Rev. C release of board**

1. Added U\_OUT1/ and U\_OUT2/ signals to feature connector.
2. Described PC/104 vs. FLASH boot options, W7.

### **12-DEC-96, Revised per Rev. D release of board**

1. Added OUT1 and OUT2 LEDs.
2. Major revision of PLD to support various DMA possibilities.
3. Changed PLD design entry from schematic entry to Altera HDL.
4. Added isolation jumper for battery and added battery socket option.
5. Added jumper to set CPU frequency.

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# NS486™SXF Evaluation Board

## *Theory of Operation*

## 1. Introduction

### 1.1 Purpose of Document

This document provides a theory of operation for the NS486SXF Evaluation Board. This documents the details of the design of the Evaluation board for use by hardware engineers, software engineers and technical documentation personnel.

### 1.2 References

The following documents are required references for understanding this document (items marked with \* are supplied with this document):

1. NS486SXF Evaluation Board, Functional Specification, for National Semiconductor, BCT Systems.\*
2. NS486™SXF Optimized 32-bit 486-class Controller With On-Chip Peripherals for Embedded Systems, ADVANCED INFORMATION November 1996, National Semiconductor.
3. NS486SXF Evaluation Board Schematic, Rev. D.\*
4. NS486SXF Evaluation Board Bill of Materials, Rev. D.\*
5. NS486SXF Evaluation Board Cross Reference, Rev. D.\*
6. EVB Altera design files, Rev. D.\*
7. NS486SXF Evaluation Board, Boot Code Source Listing.\*

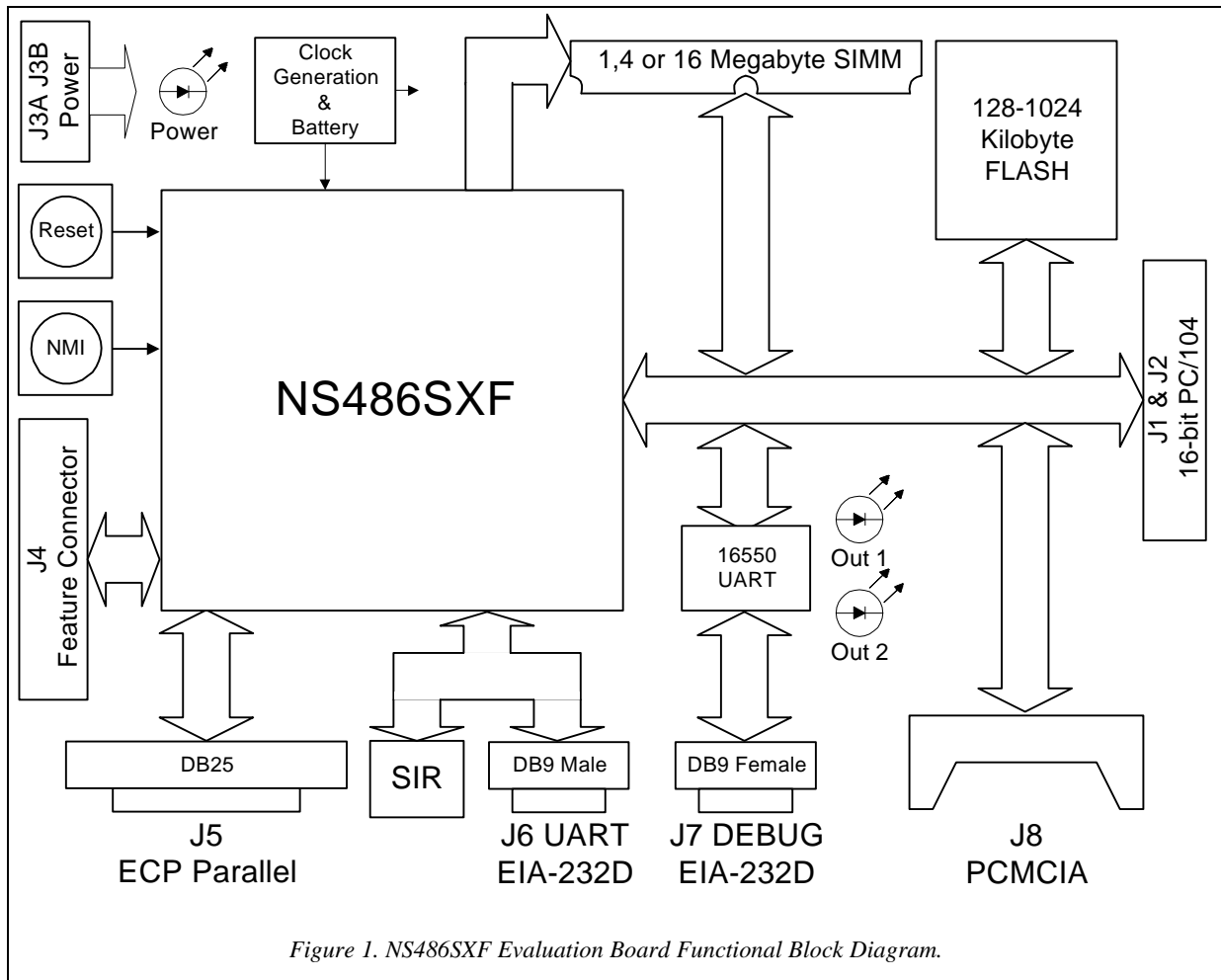
## 2. Block Diagram

The NS486SXF Evaluation Board is a complete, functioning controller board for development and evaluation purposes. A single FLASH EPROM device provides a convenient place for non-volatile data, including, for example, boot, monitor, kernel and application code. The FLASH can be from 128 kilobytes to 1 megabyte, though the standard configuration contains 256 kilobytes. Volatile data storage is provided in the no-wait state, fast-page mode DRAM contained in a 72-pin DRAM SIMM. The socket will accommodate 1, 4 or 16 megabytes of DRAM. Interface to external computers and peripherals is supported by the two serial ports, ECP parallel port and PC-Card (PCMCIA) socket. Additionally, a PC/104 expansion connector is provided for expansion of the boards capabilities through addition of PC/104 modules. PC/104<sup>1</sup> is a bus that is electrically similar to Industry Standard Architecture (ISA) but is a smaller form factor with pin and socket connectors for interconnection. The evaluation board includes battery and crystal to enable the NS486SXF real-time clock. Reset and

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<sup>1</sup> PC/104 boards are manufactured by numerous companies. For a complete specification and list of PC/104 vendors, contact: PC/104 Consortium, P.O. Box 4303, Mountain View, CA 94040-4303, (415) 903-8304

Non-Maskable Interrupt (NMI) push buttons are included on the board. Figure 1 is a functional block diagram of the NS486SXF Evaluation Board.



### 3. Bus Structure and Buffering

Figure 2 shows the major address and data bus buffering for the board. The unbuffered address (A25..0) directly drives only the DRAM and a set of address buffers. This address buffer configuration is a requirement for high speed operation of the NS486SXF with DRAM. The NS486SXF data bus (D15..0) connects to all on board resources plus the buffers for PCMCIA and the buffers for the PC/104 data bus. An individual set of buffers is provided for the PCMCIA socket so that

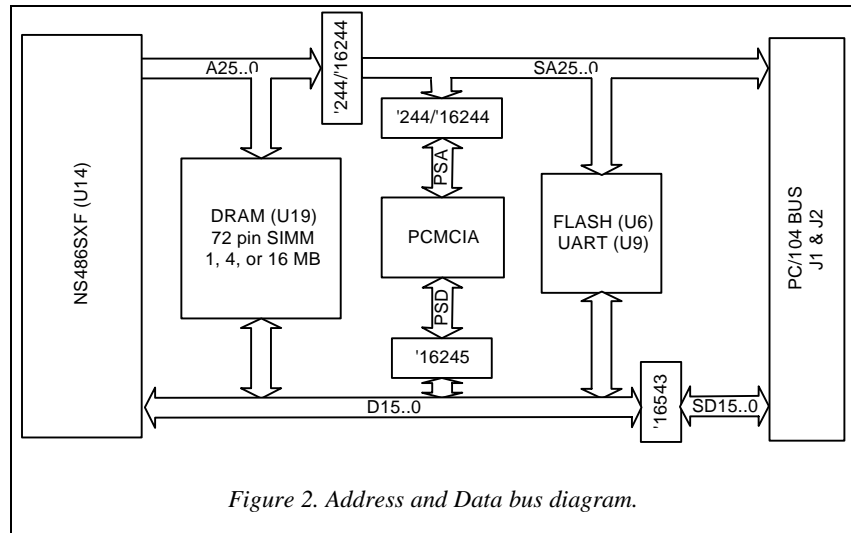


Figure 2. Address and Data bus diagram.

PCMCIA can be powered up and down independent of the board. The PCMCIA busses are the PSA and PSD busses. The data bus buffers for the SD bus include latches to improve the hold data on data write to PC/104 bus peripherals.

## 4. Functional Blocks

### 4.1 NS486SXF Embedded System Controller

The NS486SXF is U14 and is on sheet 1 of the schematic. All signal lines on the NS486SXF are also connected to the emulator header pins, J9, on the right of sheet 1. J9 is used to connect to an in-circuit emulator without requiring an expensive emulator connector for the 160 pin PQFP package. When the board is being used without an emulator, J9 is useful for connecting to NS486SXF signals for logic analyzers or oscilloscopes.

Most of the NS486SXF signals are identified in the schematic by a C\_prefix. With the exception of the address bus, data bus and DRAM control signals, all NS486SXF signals have the C\_ prepended so that it is easy to identify NS486SXF controller signals throughout the schematic.

The schematic shows two 32.768 KHz. crystals. Y1A is surface mount and Y1B is through hole, so only one of these two crystals is populated on a given board. This crystal provides the time base for the real-time clock contained in the NS486SXF. Power for the real-time clock when system power is removed is obtained from the Lithium battery, BT1.

The "RESET" pushbutton, S1 in the lower left corner of sheet 1 is the reset button for the board. The pushbutton is debounced by the cross-coupled gates, U7A and U7B to provide the power good signal to the NS486SXF. Additionally, an RC time constant on the C\_PWRGD signal holds this signal unasserted for a short time after power is applied.

## 4.2 Timebase Generation

With the exception of the real-time clock oscillator in the NS486SXF controller, all timing is generated by the timing synthesis chip, U20 on the lower right of schematic sheet 3. Although two crystals are shown, only one is installed on a board. Y2A is a surface mount crystal while Y2B is thru-hole. The crystal provides the primary 14.31818 MHz. Time base from which all other frequencies required on the board are generated.

U20 outputs a buffered 14.31818 Mhz. that is used for the OSC signal on the PC/104 bus. It also supplies a 1.84 Mhz output time base for the UART BAUD generation.

A programmable output from U20, CLK\_2X, drives the NS486SXF controller. Jumper W9 selects the programmable frequency output to one of the two frequencies of most interest for the Evaluation board, 40 and 50 Mhz. (for 20 and 25 Mhz. controller operation, respectively). Table 1 shows the W9 settings for the 40, 50 or 52 MHz operation. Although not supported or recommended, it is possible to obtain other frequencies beyond those shown in Table 1. This is accomplished by removing some combination of R30, R31 and R32 and grounding pins 1 and 2 of W9. The frequencies available in this manner are shown in Table 2. The CLK\_FS2 signal that reflects the state of the R32 programming resistor is used by the FPGA, U18, to adjust PC/104 timing based on 40 or 50 Mhz. operation. **Therefore, if any frequency other than 40 or 50 Mhz. is used, the FPGA, U18 must be redesigned to provide proper timing to the PC/104 bus.**

Table 1. W9 Frequency Selection.

W9	CLK_2X MHz.
<u>1-2</u>	<u>40</u>
<u>2-3</u>	<u>50</u>
<u>Open</u>	<u>52</u>

Table 2. Resistor frequency programming with W9-1 and W9-3 grounded.

R32	R31	R30	CLK_2X MHz.
YES	YES	YES	75
YES	YES	NO	32
YES	NO	YES	60
YES	NO	NO	40
NO	YES	YES	50
NO	YES	NO	66.66
NO	NO	YES	80
NO	NO	NO	52

## 4.3 Feature Connector (J4)

The feature connector, J4, is provided to give access to NS486SXF peripherals not used on the Evaluation Board. These peripherals include the LCD display, counter / timer, MICROWIRE / three-wire interface and UART Outputs. Additionally, the clocks, power good and high order addresses not available on the PC/104 bus are on J4. Power is also supplied to permit J4 to be used alone. J4 can also be used in conjunction with the PC/104 bus connectors J1 and J2 to provide access to the features plus the full address, data, and control busses. Table 3 shows the pin-out and signals on J4.



Table 3. J4 Feature Connector Pin Assignments

Pin	I/O	Signal	Description
1	-	GND	Ground
2	-	GND	Ground
3	O	C_CS0/	Chip Select 0 (Flash)
4	O	C_CS3/	Chip Select 3 (UART)
5	O	C_CS4/	Chip Select 4 (PC/104)
6	O	C_CS5/	Chip Select 5
7	O	C_LCD0	LCD Data Output, bit 0
8	O	C_LCD1	LCD Data Output, bit 1
9	O	C_LCD2	LCD Data Output, bit 2
10	O	C_LCD3	LCD Data Output, bit 3
11	O	C_CL2	LCD Word Clock
12	O	C_CL1	LCD Row Clock
13	O	C_CLF	LCD Frame Clock
14	-	GND	Ground
15	O	C_SYSCLK	NS486SXF System Clock
16	O	CLK_2X	NS486SXF Clock Input
17	I/O	C_TEST/	NS486SXF Test/ Signal
18	I/O	C_PWRGD	Power good input
19	I	FVPP	Flash boot block programming supply
20	O	C_UCLK	NS486SXF UART Clock
21	I/O	C_T0	NS486SXF Timer T0 signal
22	I/O	C_T1	NS486SXF Timer T1 signal
23	O	A24	NS486SXF Address 24
24	O	A25	NS486SXF Address 25
25	O	C_SO	NS486SXF MICROWIRE Serial Data Output
26	I	C_SI	NS486SXF MICROWIRE Serial Data Input
27	O	C_SCLK	NS486SXF MICROWIRE Serial Clock
28	O	U_OUT1/	UART Output 1
29	O	U_OUT2/	UART Output 2
30	-	<u>C_RESET/</u>	<u>Low asserted reset</u>
31	O	+12	+12 Volt Supply
32	-	RFU	Reserved for future use
33	O	-12	-12 Volt Supply
34	-	RFU	Reserved for future use
35	O	GND	Ground
36	O	GND	Ground
37	O	+5	+5 Volt Supply
38	O	+5	+5 Volt Supply
39	O	GND	Ground
40	O	GND	Ground

## 4.4 System ROM (FLASH)

Table 4. FLASH access times, ns.

### 4.4.1 Boot Block FLASH

The FLASH device, U6, is the processor boot device and is on sheet 3 of the schematic. The FLASH device used is a top-boot, boot block device. The device is a sixteen-bit wide device directly connected to the unbuffered data bus. The device is enabled via FLASH/, the boot device chip select from the NS486SXF controller when FLASH booting is enabled. The design will accommodate FLASH devices from AMD, Intel, or Micron.

Number of wait states	20 MHz. access time, ns.	25 MHz. access time, ns.
1	122	82
2	172	122
3	222	162
4	272	202
5	322	242
6	372	282
7	422	322

### 4.4.2 FLASH Timing Requirements

Timing requirements for the FLASH is determined by the NS486SXF timing with the addition of the delays due to address buffering on the board. The address buffering adds a delay of 8 ns. worst case to the access time. Access time requirements for the FLASH depends on the frequency of the NS486SXF and the chip select wait programming. The formula for access time (in nanoseconds) is therefore:

$$t_{access} = (WAIT + 3)T - 78, \text{ with command delay}$$

Where *WAIT* is the number of programmed wait states and *T* is the period of the clock.

The FLASH must have the command delay of 1 state to function properly due to the requirement for valid address before the leading edge of the write strobe. Table 4 shows the FLASH speeds supported for various numbers of wait states at both 20 and 25 MHz. operation.

### 4.4.3 FLASH Programming Considerations

Although FLASH can be programmed prior to board assembly, the FLASH devices used on the board can be programmed in place via appropriate software. Jumper W7 was added to the C revision of the board to accommodate board operation with no data programmed in the FLASH. When W7-1 is shorted to W7-2, the board will boot from the FLASH device as it always did in previous revisions of the board. When W7-2 is shorted to W7-3, the board will instead boot from the PC/104 bus. In the later case, an 8 or 16-bit memory board must be installed in the PC/104 sockets and must have valid boot code for the NS486SXF. The board logic enables the PC/104 bus whenever CS0/ is asserted and does not enable the FLASH when CS0/ is asserted. The FLASH must be enabled by programming CS5/ to enable the FLASH device to an unoccupied area of system memory for programming.

**Note: FLASH programming via W7-2 to W7-3 is intended for manufacturing use. When this condition is set up, the PC/104 bus may not properly support the simultaneous operation of 8-bit and 16-bit PC/104 boards.** This is because the normal use of CS5/, i.e. the lower meg enables for the SMEMR/ and SMEMW/ is not available when booting from PC/104.

## 4.5 DRAM

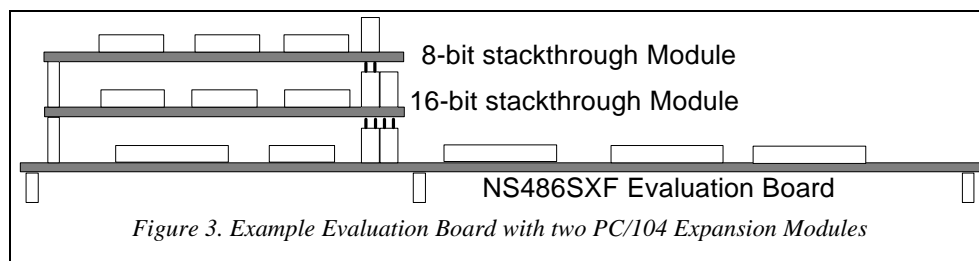
The Evaluation Board has a single 72-pin socket for a DRAM SIMM. This DRAM is controlled by the NS486SXF built-in DRAM controller. The controller is designed to accommodate up to two banks of 16-bit wide DRAM. The DRAM design for the evaluation board, shown in the upper left of sheet one of the schematic, organizes the SIMM as two 16-bit banks. Because double sided SIMMs require four banks for 16-bit wide usage, the evaluation board can only be used with single sided SIMMs. The standard sizes single-sided DRAM SIMMs that can be used with the Evaluation Board are 1, 4, or 16 Megabyte. **Double sided SIMMs, e.g. 2, 8 or 32 Megabytes can not be used with the evaluation board.**

The speed requirements of the DRAM are determined by the NS486SXF controller as the Evaluation Board meets the loading requirements specified for the NS486SXF DRAM controller. For operation at 20 Mhz., most any 70 ns. or faster SIMMs can be used.

For operation at 25 Mhz., the SIMM must be 60 ns. Additionally, the SIMM must have a column address access time,  $t_{CAC}$  maximum of 15 ns. Since a number of DRAM devices have  $t_{CAC}$  a of 20 ns., some 60 ns. devices will not be fast enough for 25 Mhz. operation with the NS486SXF. This is particularly true for parity memory on SIMMs.

## 4.6 PC/104

PC/104 is a bus designed for embedded systems that uses compact, stackable modules to construct a PC compatible computer. PC/104 offers full architecture, hardware and software compatibility with the PC bus, but in ultra-compact (3.6" x 3.8") stackable modules. The Evaluation Board includes PC/104 bus compatible expansion connectors. Figure 3 shows an example system based on an Evaluation Board with two PC/104 modules stacked on top.



The PC/104 connectors and support circuitry are shown on sheet 5 of the schematic. Although only four DMA channels are available, the bus supports most standard 8-bit and 16-bit memory and I/O modules. All six external NS486SXF interrupt request lines are available to support PC/104 interrupts.

The PC/104 bus, which has timing specifications based on the I.E.E.E. P996 draft standard, has various strobe timing requirements for 8-bit, 16-bit, memory and I/O operations. Since the NS486SXF can generate only one strobe timing for 8 or 16 bit operations, plus it does not support the ENDXFR/ signal on the bus, additional circuitry on the Evaluation Board controls the NS486SXF RDY signal to better support the various PC/104 bus cycles. This circuitry is described in Section 4.6.2.

The Evaluation Board PC/104 interface does not support the following standard PC/104 capabilities:

1. MEMORY/ signal is not supported. The signal is driven unasserted (high).
2. Temporary masters are not supported. The MASTER/ signal is ignored.

3. The BALE (address latch enabled) is not supported. The signal is always asserted.

#### 4.6.1 PC/104 Control Signals

The PC/104 interface is on sheet 5 of the schematic. The control circuitry is generated in the PC/104 control FPGA, U18 on this sheet. The schematic for this FPGA is shown in the *EVb Altera Design Files*. The NS486SXF C\_RDY and C\_CS16 signals are generated in the *rdy* block and described below in section 4.6.2.

The PC/104 memory strobes, SMEMR/, SMEMW/, MEMR/ and MEMW/ are simply qualified versions of the NS486SXF C\_MEMR/ and C\_MEMW/ signals. The MEMR/ and MEMW/ signals must only be enabled during PC/104 bus accesses and not during on board accesses to other memory, in this case the FLASH. This is accomplished with the PC104SEL/ signal, which is CS4/ from the NS486SXF. SMEMR/ and SMEMW/ are similar, but must only be active during accesses to the first one megabyte of PC/104 memory. This address decoding is provided by MEG1EN/, which is CS5/ from the NS486SXF. (Note that MEG1EN/ is used differently than normal whenever PC/104 booting is enabled by W7, see section 4.4.3)

The FLASH booting vs. the PC/104 booting is determined by the state of the SBHE/ signal whenever a reset occurs. Due to the relative timing of the trailing edge of RESET and SBHE/, the delayed state of SBHE/ is sampled at the end of reset.

SYSCLK for the PC/104 bus is generated from the master CLK\_2X. This master clock is divided by six to obtain an acceptable PC/104 SYSCLK. Under normal operation, CLK\_2X is 40 or 50 Mhz., thus yielding a SYSCLK frequency of 6.67 or 8.33 Mhz. respectively.

The DB\_RDEN/, DB\_WREN/ and DB\_LEN/ control the data buffer for the PC/104 bus, U17 on sheet five. The data buffer is enabled for read only when a valid PC/104 cycle occurs or during DMA cycles to the PC/104 bus. PC104SEL/ (C\_CS4/) indicates that an address range that falls in PC/104 address space is present. Since the UART (see section 4.10) is in the I/O space also used by PC/104, the buffer is disabled whenever UART accesses occur. PCMCIA I/O also overlaps the PC/104 I/O space, so the buffer must not be enabled for PCMCIA cycles. The PLD signal PC104EN combines the PC104SEL/ signal with the flash boot signal and is disabled for PCMCIA access (P\_ENA1 or P\_ENA2) or UART accesses (UARTEN/). In order to support DMA to or from the PC/104 bus, the buffer must be enabled during DMA cycles, but only DMA cycles to the PC/104 bus. Therefore, the DB\_RDEN/ is asserted during DMA cycles that are not to the local flash device or to PCMCIA. This situation is covered by the ENB\_DMAREADBUF signal in the PLD. The DB\_RDEN/ equation thus includes both the PC104EN and the ENB\_DMAREADBUF terms

Because PC/104 has data hold time requirements that exceed the NS486SXF specifications, U17 latches write data and holds the data beyond the valid time out of the NS486SXF. An additional timing constraint for the data buffer is the disable time for the buffer during reads. The '08 gate, U21D, provides fast disable of read data, to meet NS486SXF requirements for  $t_{\text{DOFF}}$ .

The AEN signal for the PC/104 bus is set low to enable programmed I/O to PC/104 modules when CS4/ is asserted and there is no DMA cycle in progress.

### 4.6.2 PC/104 Wait State Control

The PC/104 bus, which has timing specifications based on the I.E.E.E. P996 draft standard, has various strobe timing requirements for 8-bit, 16-bit, memory and I/O operations. Since the NS486SXF can generate only one strobe timing for 8 or 16 bit operations, plus it does not support the ENDXFR/ signal on the bus, additional circuitry on the Evaluation Board controls the NS486SXF RDY signal to better support the various PC/104 bus cycles. Although it would have been possible to have a common cycle timing defined for all transfers, this would have to be at the slowest cycle required for any expansion module. Because the 8-bit timing was defined by the original IBM-PC that used a slow, 8-bit microprocessor, to have a single slow cycle would make the system terribly inefficient for 16-bit operations.

The wait state generation logic is in the PC/104 control FPGA on sheet 5 of the schematic. The logic is contained in the RDY.TDF design file for this FPGA. The WAIT flip-flop is set whenever a command (IOR/, IOW/, MEMR/ or MEMW/) is asserted and the access is to PC/104 (CS4/ asserted). The WAIT signal is synchronized to the clock and the WAITS signal enables the counter (ctr[4..0]) to begin counting up. The ENDWAIT/ signal will be asserted whenever a terminating condition occurs. This will clear the counter and clear the WAIT flip-flop allowing RDY to be asserted to the NS486SXF. The two signals BYTECYC and WORDCYC are for Byte access and Word access on the bus, respectively. They are generated from the IOCS16/ and MEMCS16/ signals from the bus with the appropriate type cycle in progress. The CLKIS50 signal is from the time base generation circuitry (section 4.2) and is asserted when RDY\_CLK is 50 Mhz., and unasserted when it is 40 Mhz. The BYTECYC or WORDCYC signal is combined with count values to generate most of the terminating conditions. The terminating conditions are:

- **ENDXFR/.** This is an end of transfer initiated by a 16-bit ISA memory card that can handle 0 wait states (and is asserted in response to 0WS/ ). There is no need to qualify this value by the counter, since the NS486SXF CS4/ must have a logical chip select bus cycle that meets the minimum PC/104, zero wait state cycle. Note the ENDXFR/ is synchronized to the RDYCLK clock.
- **WORDIO.** A minimum of 165 ns. for 16-bit I/O cycles.
- **WORDMEM.** A minimum of 240 ns. for 16-bit memory cycles.
- **BYTEMEMIO.** A minimum of 530 ns. for 8-bit memory or I/O cycles.

The RDY signal can also be driven by IOCRDY and PCMRDY signals. RDY will be asserted only when all conditions have been met, so the slower of the WAIT signal and the IOCRDY will determine the bus cycle time for PC/104 accesses. The RDY signal is delayed into the RDY.TDF circuitry to increase the command hold from IOCRDY. The P996 specification requires 120 ns. The NS486SXF can only be programmed to two cycles, or 80 ns. at 25 MHz. By adding the delay, a total command hold of 120 ns. can be achieved. Note that the command hold delay must be considered in calculating total bus cycle time.

The C\_CS16/ signal is routed out of the device to drive the NS486SXF C\_CS16/ signal. This is because PC/104 requires the bus master to properly qualify the IOCS16/ and MEMCS16/ signals with the appropriate strobes. (I.e., MEMCS16/ can, and usually will be, asserted by 16-bit PC/104 memory cards when an I/O access occurs. IOCS16/ will be asserted by 16-bit I/O cards when the low order address bits of a memory address match the I/O address).

### 4.6.3 PC/104 Interrupt Capability

An PC/104 bus supports thirteen interrupts. The NS486SXF only supports 6 external interrupts. Table 5 shows the interrupt mapping from the PC/104 bus to the NS486SXF interrupt inputs and the W1 pins associated with each interrupt request signal.

C\_IRQ2 can also be used as the interrupt request for the debug serial port. This interrupt is enabled via W2. If W2 is installed, then no jumper should be installed for W1, 7-8.

Table 5. PC/104 to NS486SXF Interrupt Mappings.

PC/104 bus		NS486SXF	
Interrupt	W1 Pin	Interrupt	W1 Pin
IRQ5	12	C_IRQ0	11
IRQ6	10	C_IRQ1	9
IRQ7	8	C_IRQ2	7
IRQ9	6	C_IRQ3	5
IRQ14	4	C_IRQ4	3
IRQ15	2	C_IRQ5	1

The PC/104 specification defines a method of interrupt sharing, which is incompatible with the P996 draft specification. To properly support non-shared interrupts, the bus master must pull-up each interrupt request line with a 2.2K resistor. In order to operate with PC/104 shared interrupts, a minimum pull-up value of 15K is required. The evaluation board supports either option by providing a socket for RP3 to allow user selection of the appropriate pull-up value for the user's application.

### 4.6.4 PC/104 DMA Capability

The PC/104 bus supports a total of 8 DMA channels. The NS486SXF has four external DMA channels. Table 6 shows the support of PC/104 DMA channels by the NS486SXF external DMA channels.

Table 6. DMA Channel Assignments.

PC/104 DMA Channel	NS486SXF DMA channel
1	0
2	2
5	4
6	6

### 4.6.5 PC/104 IOCHK/

The PC/104 signal IOCHK/ is asserted for board error conditions, typically conditions such as parity error on a memory board. The IOCHK/ signal from PC/104 is combined with a de-bounced NMI pushbutton through the cross-coupled gates, U7C and U7D to create the C\_NMI signal for the NS486SXF.

### 4.6.6 PC/104 timing requirements.

The PC/104 access must have the following characteristics programmed:

1. Two CPUCLK periods of ready extension (Bits 5 and 6 of *Boot ROM Access Time Register*).
2. One CPUCLK period of command delay (CSCD bit set for appropriate *Chip Select Access Time Register*).
3. Three CPUCLK periods of strobe width (value of 2 programmed into appropriate *Chip Select Access Time Register*).

## 4.7 PCMCIA

The PCMCIA interface circuitry is on sheet 4 of the schematic. The PCMCIA host interface requires minimal logic on the board as the NS486SXF contains the host adapter circuitry. The board circuitry consists of buffering and power control. By buffering all address, data and control signals to the PCMCIA socket, it is possible to turn power off to a device in the socket while the Evaluation Board is powered and fully operational.

## 4.8 ECP Interface

The Extended Capabilities Port (ECP) is implemented entirely within the NS486SXF. Signal filtering and connector are provided on the Evaluation Board as shown in the lower left part of sheet 3 of the schematic. J5 is the ECP interface connector.

## 4.9 NS486SXF Serial Port

Table 7. NS486SXF Serial Port Jumpers

The NS486SXF on-chip NS16550 UART supports either EIA-232 interface levels or Serial Infrared (SIR) mode. The Evaluation Board has both types of interface circuitry. Configuration jumpers W3 and W5 select which interface is used. Table 7 shows the jumper settings for the NS486SXF Serial Port.

W3	W5	Port Enabled
1-2	None	EIA-232
2-3	1-2	Serial Infrared Interface

### 4.9.1 Serial Infrared (SIR) Interface

An infrared LED and receiver are included on the board for infrared remote control application. The circuitry is shown at the bottom of sheet 2 on the schematic.

The transmitter uses a TSIP5201 Infrared emitting diode (IED) driven by the NS486SXF serial port. The receiver uses a BPV22F sensor.

### 4.9.2 EIA-232 Interface

Because the NS486SXF MICROWIRE™ has been kept available for use through the feature connector, the CTS/, DCD/ and RI signals are not available for the EIA-232 interface. Only the RTS/, DTR/ and DSR/ control signals plus the data are available for the interface. The interface is a data terminal equipment (DTE) interface using a 9 pin, male, D type connector. This is J6 on sheet 2 of the schematic. Level translation from the NS486SXF CMOS levels to EIA-232D levels is accomplished through U2 and U3.

## 4.10 Debug Serial Port

An additional serial port is provided on the Evaluation Board, primarily as a debug port for Evaluation Board monitor to host computer communication (though the port could be used for other purposes, if desired). The debug serial port is implemented using a National Semiconductor PC16550 UART. The UART is U9, in the upper left corner of sheet 2 of the schematic. Address decoding to select the UART is accomplished in the NS486SXF via CS3/ (signal C\_CS3/). The master Time base for BAUD clock generation is the 1.84MHZ signal. This signal is derived from the master time base generator (see section 0).

The PC16550 is designed to be used as a Data Terminal Equipment (DTE) but is being used in as a Data Communications Equipment port (DCE). This is why the signal names on the chip are not consistent with the signals going to the EIA-232 drivers and receivers.

Jumper W2 connects or isolates the interrupt request from the UART to C\_IRQ2.

The general purpose outputs from the UART, OUT1 and OUT2 are routed to the feature connector as U\_OUT1/ and U\_OUT2/. These two outputs are buffered to drive LED indicators on the board. When the OUT1 or OUT2 bits in the UART modem control register are cleared, the respective LEDs will be on. When they are set, the respective LEDs will off.

## 5. NS486SXF Chip Select Usage

Five of the six external, physical chip select signals generated by the NS486SXF are utilized by the Evaluation Board. The following sections describe the usage of these signals on the board.

### 5.1 CS0/ - Flash Select

CS0/ is used to select the Flash on the Evaluation Board. The boot code must program a logical chip to include the entire Flash address range for CS0/ prior to jumping outside the upper 64 Kilobytes of memory. To include all Flash, the chip select should be programmed to respond to access from 0xFFF00000 to 0xFFFFFFFF.

### 5.2 CS1/ & CS2/ - PCMCIA Selects

The CS1/ and CS2/ are used for the PCMCIA interface.

### 5.3 CS3/ - UART Select

The CS3/ signal from the NS486SXF is programmed to select the UART used for the debug serial port.

### 5.4 CS4/ - PC/104 Select

The PC/104 select is programmed to be active for either memory or I/O. PC/104 is designed to match the speeds of a standard 8 MHz. AT and adhere to the IEEE P996 draft standard specification. Normally, this means access to PC/104 memory in the NS486SXF range of 0x03000000 to 0x3FFFFFFF and I/O addresses in the range of 0x0000 to 0xFFFF.

### 5.5 CS5/ - PC/104 First Meg

CS5/ is used to enable the SMEMR/ and SMEMW/ strobes on the PC/104 bus. These strobes must be active only in the first megabyte of the PC/104 address space. This requires the NS486SXF program this chip select to be active in the range of 0x3000000 to 0x30FFFFF.

When PC/104 booting is enabled (see section 4.4.3), CS5/ must be programmed to an unused memory space to enable the FLASH device for FLASH programming.



## 6. Programmer's Interface

### 6.1 Memory Map

The allocation of the external system memory space is shown in the address map in Table 8.

Table 8. Evaluation Board System Memory Map.

Starting Address (hex)	Ending Address (hex)	Size	Description
00000000	00FFFFFF	16M	System DRAM
01000000	02FFFFFF	<u>16</u> M	<i>Unused</i>
02000000	02FFFFFF	16M	PCMCIA Interface
03000000	030FFFFF	1M	First Meg of PC/104
03100000	03FFFFFF	15M	PC/104
04000000	FFFFFFFF		<i>Unused</i>
FFF00000	FFFFFFFF	1M	System boot FLASH

### 6.2 I/O Map

The allocation of the Evaluation Board I/O space, excluding internal NS486SXF ports, is shown in the I/O address map in Table 9.

Table 9. Evaluation Board I/O Address and Port Map.

Starting Address (hex)	Ending Address (hex)	Read - Write	Description
0x0000	0xFFFF	-	PC/104 I/O
0x02F8	0x02FF	-	UART

## 7. Configuration Jumper Summary

### 7.1 W1 - PC/104 Interrupt Request Jumpers

W1 allows isolation, connection and redirection of PC/104 interrupts. The interrupt signals on W1 are summarized in Table 10.

Table 10. PC/104 to NS486SXF Interrupt Mappings.

PC/104 bus		NS486SXF	
Interrupt	W1 Pin	Interrupt	W1 Pin
IRQ5	12	C_IRQ0	11
IRQ6	10	C_IRQ1	9
IRQ7	8	C_IRQ2	7
IRQ9	6	C_IRQ3	5
IRQ14	4	C_IRQ4	3
IRQ15	2	C_IRQ5	1

### 7.2 W2 - Debug Serial Port Interrupt Request Isolation

W2 is installed to connect the debug serial port interrupt request to the NS486SXF External interrupt request 2 (C\_IRQ2) and removed to isolate the interrupt.

### 7.3 W3, W5 - Serial Port Type Selection

W3 and W5 select the NS486SXF serial port interface to be EIA-232D or HP Serial Infrared. Table 11 summarizes the jumper settings for serial port interface selection.

Table 11. NS486SXF Serial Port Jumpers

W3	W5	Port Enabled
1-2	None	EIA-232
2-3	1-2	Serial Infrared Interface

### 7.4 W4 - FLASH $V_{pp}$ Jumper

W4 is must have a jumper installed between pins 1 and 2 for normal operation. For AMD flash devices only, sector protection can only be done by applying  $V_{pp}$  to address 9 of the device. By moving this jumper to short pins 2 and 3, the flash address 9 is available at the feature connector. This is meant to be used only by manufacturing programming equipment.

### 7.5 W6 - Monitor / User Boot Jumper

A single, general purpose, jumper is provided for indicating to the boot code whether boot should complete by jumping to a monitor or to user code. This is jumper W6. It is connected to the RI input on the debug serial port, U9.

### 7.6 W7 - FLASH / PC/104 Boot Jumper

W7 controls the 10K resistor tied to the C\_SBHE/ signal to determine if booting is to be from PC/104 or FLASH. W7-1 to W7-2 enables FLASH booting while W7-2 to W7-3 enables PC/104 booting.

### 7.7 W8 - Battery Isolation Jumper

The battery, BT1, connects to the  $V_{BAT}$  signal on the NS486SXF through jumper W8. The battery can be isolated from the processor by removing W8.

### **7.8 W9 - Frequency Selection**

W9 selects the frequency of operation for the NS486SXF. The frequency is selected according to Table 1 on page 4.