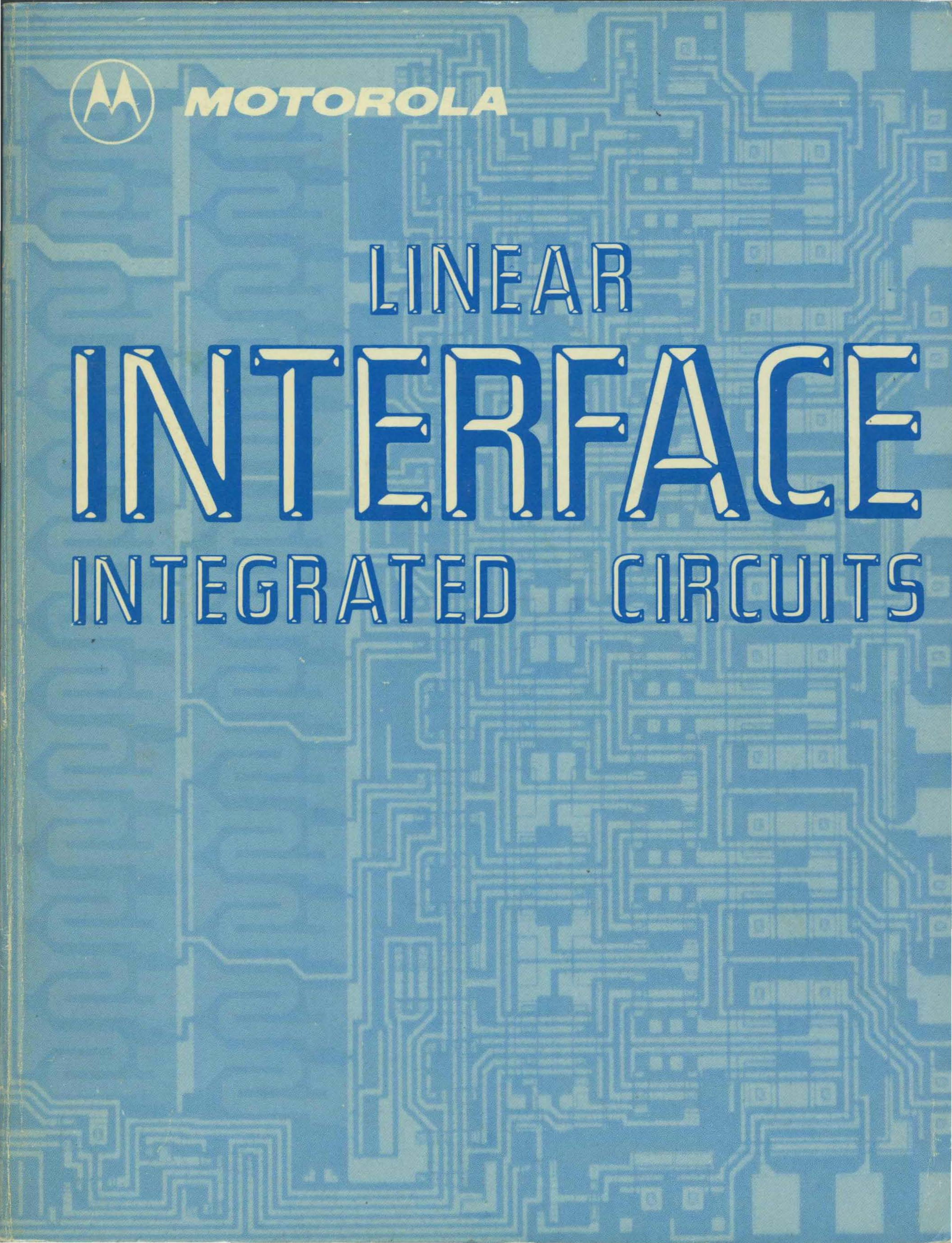

MOTOROLA

LINEAR
INTERFACE
INTEGRATED CIRCUITS

MOTOROLA

LINEAR INTERFACE INTEGRATED CIRCUITS

Prepared by
Technical Information Center

This Linear Interface Data Book contains technical information on a portion of Motorola Linear's product offering. Detailed information on other Linear products is contained in a separate Linear Data Book. For your convenience, this book contains the following:

- Cross-Reference
- Selector Guides (by Product Category)
- Data Sheets
- Package Information
- Abstracts Covering Application Notes and Engineering Bulletins

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Series C
Second Printing

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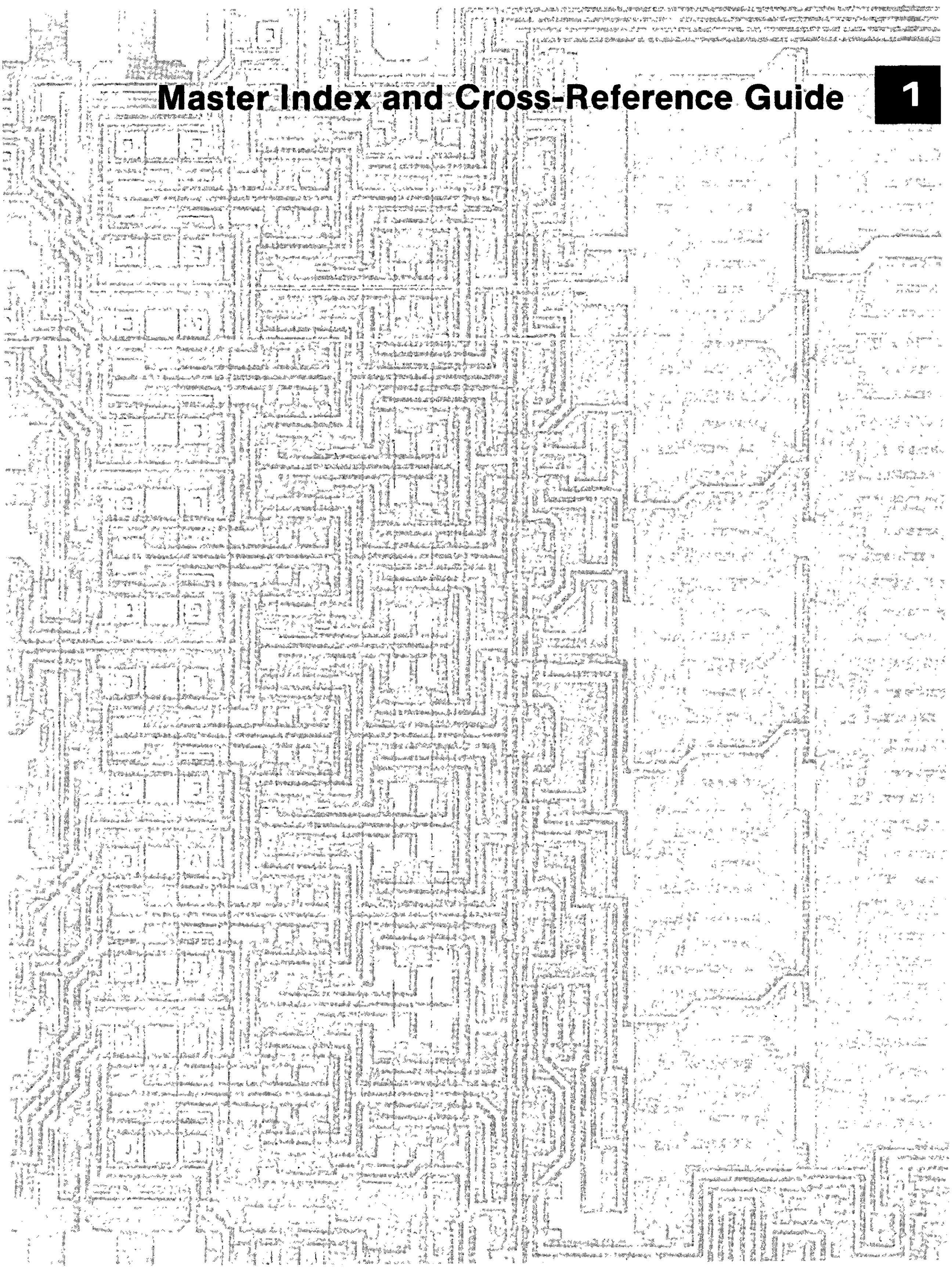

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This index includes *all* devices in Motorola Linear's product line. Devices with *Linear* in the page number column are fully characterized in the separate **Linear Data Book**; however, selection characteristics are given in Chapter 10 of this volume for your convenience.

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LF157	Monolithic JFET Operational Amplifier	Linear
LF157A	Monolithic JFET Operational Amplifier	Linear
LF255	Monolithic JFET Operational Amplifier	Linear
LF256	Monolithic JFET Operational Amplifier	Linear
LF257	Monolithic JFET Operational Amplifier	Linear
LF355	Monolithic JFET Operational Amplifier	Linear
LF355A	Monolithic JFET Operational Amplifier	Linear
LF355B	Monolithic JFET Operational Amplifier	Linear
LF356	Monolithic JFET Operational Amplifier	Linear
LF356A	Monolithic JFET Operational Amplifier	Linear
LF356B	Monolithic JFET Operational Amplifier	Linear
LF357	Monolithic JFET Operational Amplifier	Linear
LF357A	Monolithic JFET Operational Amplifier	Linear
LF357B	Monolithic JFET Operational Amplifier	Linear
LM101A	General Purpose Adjustable Operational Amplifier	Linear
LM104	Adjustable Negative Voltage Regulator	Linear
LM105	Adjustable Positive Voltage Regulator	Linear
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MC1536	High-Voltage Operational Amplifier	Linear
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MOTOROLA

LINEAR
INTEGRATED CIRCUITS

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. . . provides a complete interchangeability list linking over 3000 devices offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Functional Equivalent" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
709BE	MC1709G	
709BH	MC1709F	
709CE	MC1709CG	
709CH	MC1709CF	
709CJ	MC1709CP2	
710BE	MC1710G	
710CE	MC1710CG	
711BE	MC1711G	
711BN	MC1711L	
711CE	MC1711CG	
711CJ	MC1711CP	
723BE	MC1723G	
723CE	MC1723CG	
723CJ	MC1723CL	
741BE	MC1741G	
741BH	MC1741F	
741BN	MC1741L	
741CE	MC1741CG	
747BE		MC1747G
747BN		MC1747L
747CE		MC1747CG
748BE		MC1748G
748CE		MC1748CG
809BE		MC1776G
809CE		MC1776CG
823AE		MC1723G
1458CE	MC1458CG	
3232		MC3232AL
3245	MC3245L	
6605J		MC3443P
6605L		MC3443P
8216		MC8T26AL
8226		MC8T28L
9614DC		MC75S110L
9614DM		MC75S110L
9615DC		MC75108L
9615DM		MC55108L
9615FM		MC55108L
9616CDC		MC1488L
9616EDC		MC1488L
9616DM		MC1488L
9617DC		MC1489AL
9620DC		MC75S110L
9620DM		MC75S110L
9621DC		MC75108L
9621DM		MC55108L
9622DC		MC75140P1
9622DM		MC75140P1
9624DC		MMH0026CL
9624DM		MMH0026CL
9625DC		MMH0026CL
9625DM		MMH0026CL
9627CDC		MC1489AL
9627DM		MC1489AL
9636AT	MC3488AP	
9637T		MC3486P
9638T		MC3487P
9640J	MC3443P	
9640D		MC3443P
9640DC		MC3440AP
9640NC	MC3440AP	
9665DC	MC1411L	
9665PC	MC1411P	
9666DC	MC1412L	
9666PC	MC1412P	
9667DC	MC1413L	
9667PC	MC1413P	
9668DC	MC1416L	
9668PC	MC1416P	
55107ADM	MC55107L	
55107BDM		MC55107L
55108ADM	MC55108L	
55108BDM		MC55108L
55110DM		MC75S110L
55121DM		MC8T13L
55122DM		MC8T14L
55207DM		MC55107L
55208DM		MC55108L
55325DM	MC55325L	
55325FM	MC55325L	
75107ADC	MC75107L	
75107APC	MC75107P	
75107BDC		MC75107L
75107BPC		MC75107P
75108ADC	MC75108L	
75108APC	MC75108P	
75108BDC		MC75108L
75108BPC		MC75108P
75110DC	MC75S110L	
75110PC	MC75S110P	
75121DC	MC8T13L	
75121PC	MC8T13P	
75122DC	MC8T14L	
75122PC	MC8T14P	
75123DC	MC8T23L	
75123PC	MC8T23P	
75124DC	MC8T24L	
75124PC	MC8T24P	
75207DC		MC75107L
75207PC		MC75107P
75208DC		MC75108L
75208PC		MC75108P
75325DC	MC75325L	
75325PC	MC75325P	
75450ADC	MC75450L	
75450APC	MC75450P	
75450BDC		MC75450L
75450BPC		MC75450P
75451APC	MC75451U	
75451ATC	MC75451P	
75451BRC		MC75451U
75451BTC	SN75451BP	
75452ARC	MC75452U	
75452ATC	MC75452P	
75452BRC		MC75452U
75452BTC	SN75452BP	
75453ARC	MC75453U	
75453ATC	MC75453P	
75453BRC		MC75453U
75453BTC	SN75453BP	
75454ARC	MC75454U	
75454ATC	MC75454P	
75454BRC		MC75454U
75454BTC	SN75454BP	
75460DC		MC75450L
75460PC		MC75450P
75461RC	MC75461U	
75461TC	MC75461P	
75462RC	MC75462U	
75462TC	MC75462P	
75463RC	MC75463U	
75463TC	MC75463P	
75464RC	MC75464U	
75464TC	MC75464P	
75491DC		MC75491P
75491PC	MC75491P	
75491ADC		MC75491P
75491APC		MC75491P
75492DC		MC75492P
75492PC	MC75492P	
75492ADC		MC75492P
75492APC		MC75492P
AD301AL		LM301AH
AD505J		MC1776CG
AD505K		MC1776CG
AD505S		MC1776G
AD509J		LM301AH
AD509K		LM301AH
AD509S		LM101AH
AD518J		LM301AH
AD518K		LM301AH
AD518S		LM101AH
AD530		MC1595L
AD531		MC1595L
AD532J		MC1595G
AD559JD	MC1408L8	
AD559K	MC1408L8	
AD559KD	MC1408L8	
AD559S	MC1508L8	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
AD559SD	MC1508L8	
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD741CJ		MC1741CG
AD741J		MC1741G
AD741K		MC1741G
AD741L		MC1741G
AD741S		MC1741SG
AD7520D		MC3410L
AD7520F		MC3410L
AD7520N		MC3410L
AM26S10DC	MC26S10L	
AM26S10PC	MC26S10P	
AM26S11DC	MC26S11L	
AM26S11PC	MC26S11P	
AM725A31T		MC1556G
AM166039F		LM301AH
AM166039T		LM301AH
AMLM101	LM101AH	
AMLM101A	LM101AH	
AMLM101AD		LM101AH
AMLM101AF		LM101AH
AMLM101D		LM101AH
AMLM101F		LM101AH
AMLM105	LM105H	
AMLM105F		LM105H
AMLM105H	LM105H	
AMLM107	LM107H	
AMLM107D		LM107H
AMLM107F		LM107H
AMLM111D	LM111J	
AMLM111H	LM111H	
AMLM201	LM201AH	
AMLM201A	LM201AH	
AMLM201AD		LM201AN
AMLM201AF		LM201AH
AMLM201D		LM201AN
AMLM201F		LM201AH
AMLM205	LM205H	
AMLM205F		LM205H
AMLM205H	LM205H	
AMLM207	LM207H	
AMLM207D		LM207H
AMLM207F		LM207H
AMLM211D	LM211J	
AMLM211H	LM211H	
AMLM301	LM301AH	
AMLM301A	LM301AH	
AMLM301AD		LM301AJ
AMLM301D		LM301AJ
AMLM305	LM305H	
AMLM305A		LM305H
AMLM305F		LM305H
AMLM305H	LM305H	
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AMLM311H	LM311H	
AMU3F7733312		MC1733L
AMU3F7733393		MC1733CL
AMU3F7748312		MC1748G
AMU3I7741312	MC1741F	
AMU3I7741393	MC1741CL	
AMU5B7733312	MC1733G	
AMU5B7733393	MC1733CG	
AMU5B7741312	MC1741G	
AMU5B7741393	MC1741CG	
AMU5B7747312	MC1747G	
AMU5B7747393	MC1747CG	
AMU5B7748312	MC1748G	
AMU5B7748393	MC1748CG	
AMU5R7723312	MC1723G	
AMU5R7723393	MC1723CG	
AMU6A7723312	MC1723L	
AMU6A7723393	MC1723CL	
AMU6A7733312	MC1733L	
AMU6A7733393	MC1733CL	
AMU6A7741312	MC1741L	
AMU6A7741393	MC1741CL	
AMU6A7748312		MC1748G
AMU6A7748393		MC1748CP1
AMU6W7747312	MC1747L	
AMU6W7747393	MC1747CL	
CA101AT	LM101AH	
CA101T	LM101AH	
CA107T	LM107H	
CA108AS	LM108AJ-8	
CA108AT	LM108AH	
CA108S	LM108J-8	
CA108T	LM108H	
CA139AG	LM139AJ	
CA139G	LM139J	
CA201AT	LM201AH	
CA201T		LM201AH
CA207T	LM207H	
CA208AT	LM208AH	
CA208S	LM208J-8	
CA208T	LM208H	
CA239AE	LM239AN	
CA239AG	LM239AJ	
CA239E	LM239N	
CA239G	LM239J	
CA301AT	LM301AH	
CA307T	LM307H	
CA308AS	LM308N	
CA308AT	LM308AH	
CA308S	LM308H	
CA339AE	LM339AN	
CA339AG	LM339AJ	
CA339E	LM339N	
CA339G	LM339J	
CA723CE	MC1723CP	
CA741CS	MC1741CP1	
CA741CT	MC1741CG	
CA741S	MC1741U	
CA741T	MC1741G	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747CT	MC1747CG	
CA747E	MC1747L	
CA747F	MC1747L	
CA747T	MC1747G	
CA748CS	MC1748CP1	
CA748CT	MC1748CG	
CA748S	MC1748U	
CA748T	MC1748G	
CA758E		MC1310P
CA1310E	MC1310P	
CA1352E	MC1352P	
CA1391E	MC1391P	
CA1394E	MC1394P	
CA1398E	MC1398P	
CA1458S	MC1458CP1	
CA1458T	MC1458G	
CA1558S		MC1558U
CA1558T	MC1558G	
CA2111AE	MC1357P	
CA2111AQ	MC1357PQ	
CA3000		MC1550G
CA3001		MC1550G
CA3002		MC1550G
CA3004		MC1550G
CA3005		MC1550G
CA3006		MC1550G
CA3007		MC1550G
CA3008		MC1709F
CA3008A		MC1709F
CA3010		MC1709G
CA3010A		MC1709G
CA3011		MC1590G
CA3012		MC1590G
CA3013		MC1357P
CA3014		MC1357P
CA3015		MC1709G
CA3015A		MC1709G
CA3016		MC1709F
CA3016A		MC1709F
CA3020		MC1554G
CA3020A		MC1454G
CA3021		MC1590G
CA3022		MC1590G
CA3023		MC1590G
CA3026		CA3054
CA3028A		MC1550G
CA3028AF		MC1550G
CA3028AS		MC1550G
CA3028B		MC1550G
CA3028BF		MC1550G
CA3028BS		MC1550G
CA3029		MC1709P2
CA3029A		MC1709P2
CA3030		MC1709P2
CA3030A		MC1709P2
CA3031		MC1712G
CA3032		MC1712CG
CA3033		MC1533L
CA3033A		MC1533L
CA3035		MC1352P
CA3035V1		MC1352P
CA3037		MC1709L
CA3037A		MC1709L
CA3038		MC1709L
CA3038A		MC1709L
CA3040		MC1510G
CA3041		MC1351P
CA3042		MC1357P
CA3043		MC1357P
CA3044		MC1364P
CA3044V1		MC1364P
CA3045		MC3346P
CA3045F		MC3346P
CA3046	MC3346P	
CA3047		MC1433L
CA3047A		MC1433L
CA3048		MC3301P
CA3052		MC3301P
CA3053		MC1550G
CA3053F		MC1550G
CA3053S		MC1550G
CA3054	CA3054	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
CA3056	MC1741CG	
CA3056A	MC1741G	
CA3058		CA3059
CA3059	CA3059	
CA3064		MC1364P
CA3064E	MC1364P	
CA3065	MC1358P	
CA3066		MC1399P
CA3067		MC1323P
CA3068		MC1352P
CA3070		MC1399P
CA3071		MC1399P
CA3072		MC1323P
CA3076		MC1590G
CA3078AS		MC1776G
CA3078AT		MC1776G
CA3078S		MC1776CG
CA3078T		MC1776CG
CA3079		CA3059
CA3085		MC1723G
CA3085A		MC1723G
CA3085AF		MC1723L
CA3085AS		MC1723G
CA3085B		MC1723G
CA3085BF		MC1723L
CA3085BS		MC1723G
CA3085F		MC1723L
CA3085S		MC1723G
CA3086	MC3386P	
CA3086F		MC3346P
CA3090AQ		MC1310P
CA3091D		MC1594L
CA3120E		MC1344P
CA3125E		MC1323P
CA3134E		TDA1190Z
CA3134EM		TDA1190Z
CA3134QM		TDA1190Z
CA3136A		MC3346P
CA3137E		MC1323P
CA3139	CA3139	
CA3146		MC3346P
CA3401E	MC3401P	
CA6078AS		MC1776G
CA6078AT		MC1776G
CA6741S		MC1776G
CA6741T		MC1776G
CA3302E	MC3302P	
CMP-01CJ		MC1556G
CMP-01CP		MC1556P
D555CJ		MC1555G
D3232	MC3232AP	
D3242	MC3242AP	
D3245	MC3245P	
D8216		MC8T26AL
D8226		MC8T28L
DAC-01		MC1506L
DAC-08		MC1408L8
DAC-IC10BC	MC3410L	
DM7820AD		MC75140P1
DM7820J		MC75140P1
DM7822J		MC1489AL
DM7837J		MC3437L
DM7838J		MC3438L
DM7887J		MC3490P
DM7887N		MC3490P
DM7889J		MC3491P
DM7889N		MC3491P
DM7897J		MC3494P
DM7897N		MC3494P
DM8820AN		MC75140P1
DM8820J		MC75140P1
DM8820N		MC75140P1
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DM8838N	MC3438P	
DM8861N		MC75491P
DM8863N		MC75492P
DM8887J		MC3490P
DM8889J		MC3491P
DM8897J		MC3494P
DM75491N	MC75491P	
DM75492N	MC75492P	
DS0026CG		MMH0026CG
DS0026CH	MMH0026CG	
DS0026CJ	MMH0026CL	
DS0026CN	DS0026CP1	
DS0026G		MMH0026G
DS0026H	DS0026G	
DS0026J	DS0026L	
DS0056CG		MMH0026CG
DS0056CH		MMH0026CG
DS0056CJ		MMH0026CL
DS0056CN		MMH0026CP1
DS0056G		MMH0026G
DS0056H		MMH0026G
DS0056J		MMH0026L
DS1488J	MC1488L	
DS1488N	MC1488P	
DS1489AJ	MC1489AL	
DS1489AN	MC1489AP	
DS1489J	MC1489L	
DS1489N	MC1489P	
DS3486J	MC3486L	
DS3486N	MC3486P	
DS3487J	MC3487L	
DS3487N	MC3487P	
DS3612H		MC1472U
DS3612N		MC1472P1
DS3632H		MC1472U
DS3632J		MC1472U
DS3632N		MC1472P1
DS3644J		MC3245L
DS3644N		MC3245P
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS3674J	MC3460L	
DS3674N	MC3460P	
DS55107J	MC55107L	
DS55107W		MC75107L
DS55108J	MC55108L	
DS55108W		MC55108L
DS55110J		MC75S110L
DS55121J		MC8T13L
DS55121W		MC8T13L
DS55122J		MC8T14L
DS55122W		MC8T14L
DS55325J	MC55325L	
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75110J	MC75S110L	
DS75110N	MC75S110P	
DS75121J	MC8T13L	
DS75121N	MC8T13P	
DS75122J	MC8T14L	
DS75122N	MC8T14P	
DS75123J	MC8T23L	
DS75123N	MC8T23P	
DS75124J	MC8T24L	
DS75124N	MC8T24P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC75108P
DS75325J	MC75325L	
DS75325N	MC75325P	
DS75450J	MC75450L	
DS75450N	MC75450P	
DS75451H		MC75451U
DS75451N	SN75451BP	
DS75452H		MC75452U
DS75452N	SN75452BP	
DS75453H		MC75453U
DS75453N	SN75453BP	
DS75454H		MC75454U
DS75454N	SN75454BP	
DS75461H		MC75461U
DS75461N	MC75461P	
DS75462H		MC75462U
DS75462N	MC75462P	
DS75463H		MC75463U
DS75463N	MC75463P	
DS75464H		MC75464U
DS75464N	MC75464P	
DS75491J		MC75491P
DS75491N	MC75491P	
DS75492J		MC75492P
DS75492N	MC75492P	
DS7837J		MC3437L
DS7837W		MC3437L
DS7838J		MC3438L
DS7838W		MC3438L
DS7887J		MC3490P
DS7889J		MC3491P
DS7897J		MC3494P
DS8833J		MC8T28L
DS8833N		MC8T28P
DS8834J		MC8T26AL
DS8834N		MC8T26AP
DS8835J		MC8T26AL
DS8835N		MC8T26AP
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8838J	MC3438L	
DS8838N	MC3438P	
DS8839J		MC8T28L
DS8839N		MC8T28P
DS8887J		MC3490P
DS8887N		MC3490P
DS8889J		MC3491P
DS8889N		MC3491P
DS8897J		MC3494P
DS8897N		MC3494P

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
HA1199	HA1199	
ICB8000C		LM111J
ICB8001C		LM111J
ICB8741C		MC1741CG
ICH8500ATV		MC1776CG
ICH8500TV		MC1776CG
ICL101ALNDP		LM101AH
ICL101ALNFB		LM101AH
ICL101ALNTY		LM101AH
ICL301ALNPA		LM301AH
ICL301ALNTY		LM301AH
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL741LNDP		MC1741L
ICL741LNFB		MC1741L
ICL741LNTY		MC1741L
ICL8001CTZ		LM111J
ICL8001MTZ		LM111J
ICL8007CTA		MC1709CG
ICL8007MTA		MC1709CG
ICL8008CPA		LM301AN
ICL8008CTY		LM301AN
ICL8013A		MC1594G
ICL8013B		MC1594G
ICL8013C		MC1594G
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8021C		MC1776G
ICL8021M		MC1776G
ICL8022C		MC1776G
ICL8022M		MC1776G
ICL8043CDE		MC1776G
ICL8043CPE		MC1776G
ICL8043MDE		MC1776G
ICL8048CDE		MC1776G
ICL8048DPE		MC1776G
IH5101IIE		MC1545G
IH5101MIE		MC1545G
ITT641		MC1385P
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
ITT1330	MC1330P	
ITT1352	MC1352P	
ITT3064	MC1364P	
ITT3065	MC1358P	
ITT3066		MC1399P
ITT3701		TDA1190Z
ITT3707		MC1399P
ITT3710		MC1391P
ITT3714		MC1394P
L144AP		LM324N
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
LD111CJ	MC1405L	
LF152D		LF155J
LF155AH	LF155AH	
LF155AJG	LF155AJ	
LF155AL	LF155AH	
LF155H	LF155H	
LF155JG	LF155J	
LF155L	LF155H	
LF156AH	LF156AH	
LF156AJG	LF156AJ	
LF156AL	LF156AH	
LF156H	LF156H	
LF156JG	LF156J	
LF156L	LF156H	
LF157AH	LF157AH	
LF157AJG	LF157AJ	
LF157AL	LF157AH	
LF157H	LF157H	
LF157JG	LF157J	
LF157L	LF157H	
LF252D		LF255J
LF255H	LF255H	
LF255JG	LF255J	
LF255L	LF255H	
LF255P	LF255J	
LF256H	LF256H	
LF256JG	LF256J	
LF256L	LF256H	
LF256P	LF256J	
LF257H	LF257H	
LF257JG	LF257J	
LF257L	LF257H	
LF257P	LF257J	
LF347N	MC34004P	
LF347AN	MC34004AP	
LF347BN	MC34004BP	
LF351H	MC34001G	
LF351AH	MC34001AG	
LF351BH	MC34001BG	
LF351N	MC34001P	
LF351AN	MC34001AP	
LF351BN	MC34001BP	
LF352D		LF355J
LF353H	MC34002G	
LF353AH	MC34002AG	
LF353BH	MC34002BG	
LF353N	MC34002P	
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF355AH	LF355AH	
LF355AJG	LF355AJ	
LF355AL	LF355AH	
LF355AP	LF355AN	
LF355BH	LF355BH	
LF355BJ	LF355BJ	
LF355BN	LF355BN	
LF355H	LF355H	
LF355JG	LF355J	
LF355L	LF355H	
LF355N	LF355N	
LF355P	LF355N	
LF356AH	LF356AH	
LF356AL	LF356AH	
LF356AJG	LF356AJ	
LF356AP	LF356AN	
LF356BH	LF356BH	
LF356BJ	LF356BJ	
LF356BN	LF356BN	
LF356H	LF356H	
LF356JG	LF356J	
LF356L	LF356H	
LF356N	LF356N	
LF356P	LF356N	
LF357AH	LF357AH	
LF357BH	LF357BH	
LF357BJ	LF357BJ	
LF357BN	LF357BN	
LF357H	LF357H	
LF357JG	LF357J	
LF357L	LF357H	
LF357N	LF357N	
LF357P	LF357N	
LH0001ACH		MC1776CG
LH0001AH		MC1776G
LH0001ACD		MC1776CG
LH0001AD		MC1776G
LH0001ACF		MC1776CG
LH0001AF		MC1776G
LH0002CH		MC1538R
LH0002H		MC1538R
LH0004CH		MC1436G
LH0004H		MC1536G
LH0042CH		MC1776G
LH101F		MC1741F
LH101H		MC1741G
LH201F		MC1741F
LH201H		MC1741G
LH740ACH		LF355H
LH740AH		LF155H
LH2101AD		MC1537L
LH2101AF		MC1537L
LH2201AD		MC1537L
LH2201AF		MC1537L
LH2301AD		MC1437L
LH2301AF		MC1437L
LM100F		LM105H
LM100H		LM105H
LM101AD		LM101AH
LM101AF		LM101AH
LM101AH	LM101AH	
LM101AJ		LM101AJ
LM101AJ-14		LM101AJ
LM101AJG	LM101AJ	
LM101AL	LM101AH	
LM101D		LM101AJ
LM101F		LM101AH
LM101H	LM101AH	
LM101J-14		LM101AJ
LM104F		LM104H
LM104H	LM104H	
LM104J		LM104H
LM104L	LM104H	
LM105F		LM105H
LM105H	LM105H	
LM105JG		LM105H
LM105L	LM105H	
LM106H		MC1710G
LM107F		LM107H
LM107H	LM107H	
LM107L	LM107H	
LM108AD	LM108AJ	
LM108AF	LM108AF	
LM108AH	LM108AH	
LM108AJ	LM108J-8	
LM108D	LM108J	
LM108F	LM108F	
LM108H	LM108H	
LM109H	LM109H	
LM109K	LM109K	
LM109LA	LM109K	
LM111D	LM111J	
LM111H	LM111H	
LM112D		MC1556L
LM112F		MC1556L
LM112H		MC1556G
LM117H	LM117H	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM117K	LM117K	
LM118D		MC1741SL
LM118F		MC1741SL
LM118H		MC1741SG
LM120H-5 0	LM120H-5 0	
LM120H-5.2		MC7905 2CK
LM120H-6 0	LM120H-6 0	
LM120H-8 0	LM120H-8 0	
LM120H-12	LM120H-12	
LM120H-15	LM120H-15	
LM120H-18	LM120H-18	
LM120H-24	LM120H-24	
LM120K-5 0	LM120K-5 0	
LM120K-5 2		MC7905 2CK
LM120K-6 0	LM120K-6 0	
LM120K-8 0	LM120K-8.0	
LM120K-12	LM120K-12	
LM120K-15	LM120K-15	
LM120K-18	LM120K-18	
LM120K-24	LM120K-24	
LM122F		MC1555G
LM122H		MC1555G
LM124AD		LM124J
LM124AF		LM124J
LM124AJ		LM124J
LM124D	LM124J	
LM124F		LM124J
LM124J	LM124J	
LM125H		MC1568G
LM126H		MC1568G
LM128H		MC1568G
LM139AD	LM139AJ	
LM139AJ	LM139AJ	
LM139D	LM139J	
LM139J	LM139J	
LM140K-5 0	LM140K-5 0	
LM140K-6 0	LM140K-6 0	
LM140K-8.0	LM140K-8 0	
LM140K-12	LM140K-12	
LM140K-15	LM140K-15	
LM140K-18	LM140K-18	
LM140K-24	LM140K-24	
LM140LAH-5 0		MC78L05ACG
LM140LAH-6 0		MC78L06ACG
LM140LAH-8 0		MC78L08ACG
LM140LAH-12		MC78L12ACG
LM140LAH-15		MC78L15ACG
LM140LAH-18		MC78L18ACG
LM140LAH-24		MC78L24ACG
LM143D		MC1536G
LM143F		MC1536G
LM143H		MC1536G
LM145K		MC7905CK
LM148D	LM148J	
LM148J	LM148J	
LM148F		MC4741L
LM149D		MC4741L
LM149F		MC4741L
LM158AH		LM158H
LM158H	LM158H	
LM158JG	LM158J	
LM158L	LM158H	
LM163J		MC3450L
LM171H		MC1590G
LM200F		LM205H
LM200H		LM205H
LM201AD		LM201AJ
LM201AF		LM201AH
LM201AH	LM201AH	
LM201AJ		LM201AJ
LM201AJG	LM201AJ	
LM201AL	LM201AH	
LM201AN		LM201AN
LM201AP	LM201AN	
LM201AJ-14		LM201AJ
LM201D		LM201AJ
LM201F		LM201AH
LM201H	LM201AH	
LM201J	LM201AJ	
LM201J-14		LM201AJ
LM204H	LM204H	
LM204F		LM204H
LM205F		LM205H
LM205H	LM205H	
LM206H		MC1710CG
LM207F		LM207H
LM207H	LM207H	
LM208AD	LM208AJ	
LM208AF	LM208AF	
LM208AH	LM208AH	
LM208AJ	LM208AJ-8	
LM208D		LM208J-8
LM208F	LM208F	
LM208H	LM208H	
LM209K	LM209K	
LM209H	LM209H	
LM211D	LM211J	
LM211H	LM211H	
LM212D		MC1556L
LM212F		MC1556L
LM212H		MC1456G
LM217H	LM217H	
LM217K	LM217K	
LM218D		MC1741SL
LM218F		MC1741SL
LM218H		MC1741SG
LM220H-5 0		MC7905CK
LM220H-5 2		MC7905 2CK
LM220H-6 0		MC7906CK
LM220H-8 0		MC7908CK
LM220H-12		MC7912CK
LM220H-15		MC7915CK
LM220H-18		MC7918CK
LM220H-24		MC7924CK
LM220K-5 0		MC7905CK
LM220K-5 2		MC7905.2CK
LM220K-6 0		MC7906CK
LM220K-8 0		MC7908CK
LM220K-12		MC7912CK
LM220K-15		MC7915CK
LM220K-18		MC7918CK
LM220K-24		MC7924CK
LM222H		MC1555G
LM224AD		LM224J
LM224AF		LM224J
LM224AJ		LM224J
LM224D	LM224J	
LM224F		LM224L
LM224J	LM224J	
LM225H		MC1568G
LM226H		MC1568G
LM228H		MC1568G
LM239AD	LM239AJ	
LM239AJ	LM239AJ	
LM239D	LM239J	
LM239J	LM239J	
LM240LAH-5.0		MC78L05ACG
LM240LAH-6 0		MC78L06CG
LM240LAH-8 0		MC78L08ACG
LM240LAH-12		MC78L12ACG
LM240LAH-15		MC78L15ACG
LM240LAH-18		MC78L18ACG
LM240LAH-24		MC78L24ACG
LM240LAZ-5 0		MC78L05ACP
LM240LAZ-6 0		MC78L06ACP
LM240LAZ-8 0		MC78L08ACP
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM243H		MC1536G
LM245K		MC7905CK
LM248D	LM248J	
LM248J	LM248J	
LM249D		MC4741L
LM249J		MC4741L
LM258AH		LM258H
LM258H	LM258H	
LM2901N	LM2901N	
LM300F		LM305H
LM271H		MC1590G
LM300H		LM305H
LM301AD		LM301AJ
LM301AF		LM301AH
LM301AH	LM301AH	
LM301AJ	LM301AJ	
LM301AJG	LM301AJ	
LM301AL	LM301AH	
LM301AN	LM301AN	
LM301AP	LM301AN	
LM302H	LM310H	
LM304F		LM304H
LM304H	LM304H	
LM304J		LM304H
LM304L	LM304H	
LM304N		LM304H
LM305AH		LM305H
LM305AJG		LM305H
LM305AL		LM305H
LM305AP		LM305H
LM305F		LM305H
LM305H	LM305H	
LM305JG		LM305H
LM305L	LM305H	
LM305P		LM305H
LM306H		MC1710CG
LM307F		LM307H
LM307H	LM307H	
LM307L	LM307H	
LM307N	LM307N	
LM307P	LM307N	
LM308AD	LM308AJ	
LM308AF		LM308AJ
LM308AH	LM308AH	
LM308AH-1		LM308AH
LM308AH-2		LM308AH
LM308AJ	LM308AJ-8	
LM308D	LM308J	
LM308H	LM308H	
LM308N	LM308N	
LM309H	LM309H	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM309K	LM309K	
LM309KC	LM309K	
LM309LA	LM309K	
LM311D	LM311J	
LM311H	LM311H	
LM311N	LM311N	
LM311N-14	LM311J	
LM312D		MC1456L
LM312F		MC1456L
LM312H		MC1456G
LM317H	LM317H	
LM317K	LM317K	
LM317P	LM317T	
LM317T	LM317T	
LM318D		MC1741SCL
LM318F		MC1741SCL
LM318H		MC1741SCG
LM318N		MC1741SCP1
LM320H-5 0	LM320H-5 0	
LM320H-5 2		MC7905 2CK
LM320H-6 0	LM320H-6 0	
LM320H-8 0	LM520H-8 0	
LM320H-12	LM320H-12	
LM320H-15	LM320H-15	
LM320H-18	LM320H-18	
LM320H-24	LM320H-24	
LM320K-5 0	LM320K-5 0	
LM320K-6 0	LM320K-6 0	
LM320K-8 0	LM320K-8 0	
LM320K-12	LM320K-12	
LM320K-15	LM320K-15	
LM320K-18	LM320K-18	
LM320K-24	LM320K-24	
LM320MP-5 0		MC7905CT
LM320MP-5 2		MC7905 2CT
LM320MP-6 0		MC7906CT
LM320MP-8 0		MC7908CT
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320T-5 0	LM320T-5 0	
LM320T-5.2		MC7905 2CT
LM320T-6.0	LM320T-6 0	
LM320T-8 0	LM320T-8 0	
LM320T-12	LM320T-12	
LM320T-15	LM320T-15	
LM320T-18	LM320T-18	
LM320T-24	LM320T-24	
LM322H		MC1455G
LM322N		MC1455P1
LM324AJ		LM324J
LM324AN		LM324N
LM324J	LM324J	
LM324N	LM324N	MC3403P
LM325AN		MC1468L
LM325H		MC1468G
LM325N		MC1468L
LM326H		MC1468G
LM326N		MC1468L
LM328AN		MC1468L
LM328H		MC1468G
LM328N		MC1468L
LM339AD	LM339AJ	
LM339AN	LM339AN	
LM339N	LM339N	
LM340K-5 0	LM340K-5.0	
LM340K-6 0	LM340K-6 0	
LM340K-8 0	LM340K-8.0	
LM340K-12	LM340K-12	
LM340K-15	LM340K-15	
LM340K-18	LM340K-18	
LM340K-24	LM340K-24	
LM340KC-5 0	MC7805CK	
LM340KC-6.0	MC7806CK	
LM340KC-8 0	MC7808CK	
LM340KC-12	MC7812CK	
LM340KC-15	MC7815CK	
LM340KC-18	MC7818CK	
LM340KC-24	MC7824CK	
LM340LAH-5 0		MC78L05ACG
LM340LAH-6 0		MC78L06ACG
LM340LAH-8 0		MC78L08ACG
LM340LAH-12		MC78L12ACG
LM340LAH-15		MC78L15ACG
LM340LAH-18		MC78L18ACG
LM340LAH-24		MC78L24ACG
LM340LAZ-5 0		MC78L05ACP
LM340LAZ-6 0		MC78L06ACP
LM340LAZ-8 0		MC78L08ACP
LM340LAZ-12		MC78L12ACP
LM340LAZ-15		MC78L15ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340T-5 0	MC7805CT	
LM340T-6 0	MC7806CT	
LM340T-8 0	MC7808CT	
LM340T-12	MC7812CT	
LM340T-15	MC7815CT	
LM340T-18	MC7818CT	
LM340T-24	MC7824CT	
LM341P-5 0	MC78M05CT	
LM341P-6 0	MC78M06CT	
LM341P-8 0	MC78M08CT	
LM341P-12	MC78M12CT	
LM341P-15	MC78M15CT	
LM341P-18	MC78M18CT	
LM341P-24	MC78M24CT	
LM342P-5 0	MC78M05CT	
LM342P-6 0	MC78M06CT	
LM342P-8 0	MC78M08CT	
LM342P-12	MC78M12CT	
LM342P-15	MC78M15CT	
LM342P-18	MC78M18CT	
LM342P-24	MC78M24CT	
LM343D		MC1436G
LM343H		MC1436G
LM345K		MC7905CK
LM348D	LM348J	
LM348J	LM348J	
LM348N	LM348N	
LM349D		MC4741CL
LM349J		MC4741CL
LM349N		MC4741CL
LM358AH		LM358H
LM358AN		LM358N
LM358H	LM358H	
LM358JG	LM358J	
LM358L	LM358H	
LM358N	LM358N	
LM358P	LM358N	
LM363AJ		MC3450L
LM363AN		MC3450P
LM363J		MC3450L
LM363N		MC3450P
LM371H		MC1590G
LM376JG		LM305H
LM376L	LM305H	
LM376N		LM305H
LM376P		LM305H
LM386N		MC1306P
LM555CH	MC1455G	
LM555CN	MC1455P1	
LM555H	MC1555G	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556D	MC3556L	
LM556J	MC3556L	
LM565CH		NE565N
LM565CN	NE565N	
LM565H		NE565N
LM703LN		MC1350P
LM709AH	MC1709AG	
LM709AJ	MC1709AL	
LM709CH	MC1709CG	
LM709CJ	MC1709CL	
LM709CN	MC1709CP2	
LM709CN-8	MC1709CP1	
LM709H	MC1709G	
LM709J	MC1709L	
LM710CH	MC1710CG	
LM710CN	MC1710CP	
LM710H	MC1710G	
LM711CH	MC1711CG	
LM711CN	MC1711CP	
LM711H	MC1711G	
LM723CD	LM723CJ	
LM723CH	LM723CH	
LM723CJ	LM723CJ	
LM723CN	LM723CN	
LM723D	LM723J	
LM723H	LM723H	
LM723J	LM723J	
LM733CD	MC1733CL	
LM733CH	MC1733CG	
LM733CJ	MC1733CL	
LM733CN	MC1733CP	
LM733D	MC1733L	
LM733H	MC1733G	
LM733J	MC1733L	
LM741AD		MC1741L
LM741AF		MC1741F
LM741AH		MC1741G
LM741AJ-14		MC1741L
LM741CD	LM1741CJ	
LM741CF	LM741CF	
LM741CH	LM741CH	
LM741CJ	LM741CJ	
LM741CJ-14	LM741CJ-14	
LM741CN	LM741CN	
LM741CN-14	LM741CN-14	
LM741D	LM741J-14	
LM741ED		MC1741CL
LM741EH		MC1741CG
LM741EJ		MC1741CU
LM741EJ-14		MC1741CL
LM741EN		MC1741CP1
LM741F	LM741F	
LM741H	LM741H	
LM741J-14	LM741J-14	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM746N		MC1323P
LM747CD	LM747CJ	
LM747CF	LM747CF	
LM747CH	LM747CH	
LM747CJ	LM747CJ	
LM747CN	LM747CN	
LM747D	LM747J	
LM747F	LM747F	
LM747H	LM747H	
LM747J	LM747J	
LM748CH	MC1748CG	
LM748CJ	MC1748CU	
LM748CN	MC1748CP1	
LM748H	MC1748G	
LM748J	MC1748U	
LM1310N	MC1310P	
LM1351N	MC1351P	
LM1391N	MC1391P	
LM1394N	MC1394P	
LM1414J	MC1414L	
LM1414N	MC1414P	
LM1458H	MC1458G	
LM1458J	MC1458U	
LM1458N	MC1458P1	
LM1458N-14	MC1458P2	
LM1488J	MC1488L	
LM1488N	MC1488P	
LM1489AJ	MC1489AL	
LM1489AN	MC1489AP	
LM1489J	MC1489L	
LM1489N	MC1489P	
LM1496H	MC1496G	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM1514J	MC1514L	
LM1558H	MC1558G	
LM1558J	MC1558U	
LM1596H	MC1596G	
LM1596J	MC1596L	
LM1800AN		MC1310P
LM1800N		MC1310P
LM1805		MC1385P
LM1808N		TDA1190Z
LM1828N		MC1323P
LM1841N	MC1356P	
LM1845N		MC1344P
LM1848N		MC1323P
LM1850N		MC3426L
LM1900D		MC3301L
LM2111N	MC1357P	
LM2113N		MC1357P
LM2900J		MC3301L
LM2900N		MC3301P
LM2902J	LM2902J	
LM2902N	LM2902N	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM3011H		MC1550G
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM3064N	MC1364P	
LM3065N	MC1358P	
LM3066N		MC1399P
LM3067N		MC1323P
LM3070N		MC1399P
LM3071N		MC1399P
LM3075N	MC1375P	
LM3086N	MC3386P	
LM3126		MC1399P
LM3146		MC3346P
LM3146A		MC3346P
LM3301N	MC3301P	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM3401N	MC3401P	
LM3900N		MC3401P
LM3905N		MC1455P1
LM4250CH		MC1776CG
LM4250CN		MC1776CP1
LM4250H		MC1776G
LM5525J	MC5525L	
LM5528J	MC5528L	
LM5529J	MC5529L	
LM5534J	MC5534L	
LM5535J	MC5535L	
LM5538J	MC5538L	
LM5529J	MC5539L	
LM7524J	MC7524L	
LM7524N	MC7524P	
LM7525J	MC7525L	
LM7805KC	MC7805CK	
LM7806KC	MC7806CK	
LM7808KC	MC7808CK	
LM7812KC	MC7812CK	
LM7815KC	MC7815CK	
LM7818KC	MC7818CK	
LM7824KC	MC7824CK	
LM78L05ACH	MC78L05ACG	
LM78L05ACZ	MC78L05ACP	
LM78L05CH	MC78L05CG	
LM78L05CZ	MC78L05CP	
LM78L08ACH	MC78L08ACG	
LM78L08ACZ	MC78L08ACP	
LM78L08CH	MC78L08CG	
LM78L08CZ	MC78L08CP	
LM78L12ACH	MC78L12ACG	
LM78L12ACZ	MC78L12ACP	
LM78L12CH	MC78L12CG	
LM78L12CZ	MC78L12CP	
LM78L15ACH	MC78L15ACG	
LM78L15ACZ	MC78L15ACP	
LM78L15CH	MC78L15CG	
LM78L15CZ	MC78L15CP	
LM78L18ACH	MC78L18ACG	
LM78L18ACZ	MC78L18ACP	
LM78L18CH	MC78L18CG	
LM78L18CZ	MC78L18CP	
LM78L24ACH	MC78L24ACG	
LM78L24ACZ	MC78L24ACP	
LM78L24CH	MC78L24CG	
LM78L24CZ	MC78L24CP	
LM55107AJ	MC55107L	
LM55108AJ	MC55108L	
LM55109J		MC75S110L
LM55110J		MC75S110L
LM55121J		MC8T13L
LM55122J		MC8T14L
LM55123J		MC8T23L
LM55124J		MC8T24L
LM55325N	MC55325L	
LM75107AJ	MC75107L	
LM75107AN	MC75107P	
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75S110L	
LM75110N	MC75S110P	
LM75121J	MC8T13L	
LM75121N	MC8T13P	
LM75122J	MC8T14L	
LM75122N	MC8T14P	
LM75123J	MC8T23L	
LM75123N	MC8T23P	
LM75124J	MC8T24L	
LM75124N	MC8T24P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
LM75324J		MC75325L
LM75324N		MC75325P
LM75325J	MC75325P	
LM75325N	MC75325L	
LM75450N	MC75450P	
LM75451N	MC75451P	
LM75452N	MC75452P	
LM75453N	MC75453P	
LM75454N	MC75454P	
MC1310A	MC1310P	
MC1408B	MC1408P8	
MC1408F	MC1408L8	
MC1458JG	MC1458U	
MC1458L	MC1458G	
MC1458P	MC1458P1	
MC1558JG	MC1558U	
MC1558L	MC1558G	
MH0026H		MMH0026CG
MH0026CH	MMH0026CG	
MH0026CN	MMH0026CP1	
MH0026G		MMH0026CG
MH0026CG		MMH0026CG
MH0026F		MMH0026CL
MH0026CF		MMH0026C1
MIC709-1	MC1709G	
MIC709-5	MC1709CG	
MIC710-1C	MC1710G	
MIC710-5C	MC1710CG	
MIC711-1C	MC1711G	
MIC711-5C	MC1711CG	
MIC712-1B	MC1712F	
MIC712-1C	MC1712G	
MIC712-1D	MC1712L	
MIC712-5B	MC1712CF	
MIC712-5C	MC1712CG	
MIC712-5D	MC1712CL	
MIC723-1	MC1723G	
MIC723-5	MC1723CG	
MIC741-1C	MC1741G	
MIC741-1D	MC1741L	
MIC741-5C	MC1741CG	
MIC741-5D	MC1741CL	
ML101AF		LM101AH
ML101AM		LM101AH
ML101AT	LM101AH	
ML101F		LM101AH
ML101M		LM101AH
ML101T	LM101AH	
ML107F		LM107H
ML107M		LM107H
ML107T	LM107H	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

ML108AF —OP-08B

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ML108AF		MC1556G
ML108AM	LM108AJ	
ML108AT	LM108AH	
ML108M	LM108J	
ML108T	LM108H	
ML111M	LM111J	
ML111S		LM111J
ML111T	LM111H	
ML118F		MC1741SG
ML118M		MC1741SG
ML118T		MC1741SG
ML201AF		LM201AH
ML201AM		LM201AH
ML201AT	LM201AH	
ML201F		LM201AH
ML201M		LM201AH
ML201T	LM201AH	
ML207F		LM207H
ML207M		LM207H
ML207T	LM207H	
ML208AF		MC1556G
ML208AM	LM208AJ	
ML208AT	LM208AH	
ML208M	LM208J	
ML208T	LM208H	
ML211M	LM211J	
ML211S	LM211N	
ML211T	LM211H	
ML218F		MC1741SG
ML218M		MC1741SG
ML218T		MC1741SG
ML301AP		LM301AN
ML301AS	LM301AN	
ML301AT	LM301AH	
ML301P		LM301AN
ML301S	LM301AN	
ML301T	LM301AN	
ML307P		LM307H
ML307S	LM307N	
ML307T	LM307H	
ML308AM	LM308AJ	
ML308AT	LM308AH	
ML308M	LM308J	
ML308T	LM308H	
ML311M	LM311J	
ML311P	LM311J	
ML311S	LM311N	
ML311T	LM311H	
ML318M		MC1741SCP1
ML318T		MC1741SCG
ML709AF	MC1709AF	
ML709AM	MC1709AL	
ML709AT	MC1709AG	
ML709CP	MC1709CP2	
ML709CT	MC1709CG	
ML709F	MC1709F	
ML709M	MC1709L	
ML709T	MC1709G	
ML723CF		MC1723CL
ML723CM	MC1723CL	
ML723CP	MC1723CL	
ML723CT	MC1723CG	
ML723F		MC1723L
ML723M	MC1723L	
ML723T	MC1723G	
ML741AF		MC1556G
ML741AM		MC1556G
ML741AT		MC1556G
ML741CP	MC1741CP2	
ML741CS	MC1741CP1	
ML741CT	MC1741CG	
ML741F	MC1741F	
ML741M	MC1741L	
ML741T	MC1741G	
ML747CP	MC1747CL	
ML747CT	MC1747CG	
ML747F	MC1747F	
ML747M	MC1747L	
ML747T	MC1747G	
ML748CP		LM301AN
ML748CS	LM301AN	
ML748CT	MC1748CG	
ML748F		MC1748G
ML748M		MC1748G
ML748T	MC1748G	
ML1436T	MC1436G	
ML1437P	MC1437P	
ML1458P	MC1458P2	
ML1458S	MC1458P1	
ML1458T	MC1458G	
ML1488M	MC1488L	
ML1489AM	MC1489AL	
ML1489M	MC1489L	
ML1536T	MC1536G	
ML1537M	MC1537L	
ML1558M	MC1558L	
ML1558T	MC1558G	
ML3046P	MC3346P	
ML4250T		MC1776G
ML4250CS		MC1776CG
ML4250CT		MC1776CG
ML4251T		MC1776G
ML4251CS		MC1776CG
ML4251CT		MC1776CG
ML6503M		MC1537L
ML7503M		MC1437L
N5065A	MC1358P	
N5070B		MC1399P
N5071A		MC1399P
N5072A		MC1323P
N5556T	MC1456G	
N5556V	MC1456P1	
N5558F	MC1458L	
N5558T	MC1458G	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5596K	MC1496G	
N5709A	MC1709CP2	
N5709G	MC1709CF	
N5709T	MC1709CG	
N5709V	MC1709CP1	
N5710A	MC1710CP	
N5710T	MC1710CG	
N5711A	MC1711CP	
N5711K	MC1711CG	
N5723A		MC1723CP
N5723T	MC1723CG	
N5733K	MC1733CG	
N5741A	MC1741CP2	
N5741T	MC1741CG	
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N5748A		MC1747CG
N5748T	MC1748CG	
N8T13B	MC8T13P	
N8T13P	MC8T13L	
N8T14B	MC8T14P	
N8T14E	MC8T14L	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T23B	MC8T23P	
N8T23E	MC8T23L	
N8T24B	MC8T24P	
N8T24E	MC8T24L	
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26B	MC8T26AP	
N8T28B	MC8T28P	
N8T37A	MC3437P	
N8T38A	MC3438P	
N8T95B	MC8T95P	
N8T95F	MC8T95L	
N8T96B	MC8T96P	
N8T96F	MC8T96L	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
NE501A		MC1733CL
NE501K		MC1733CG
NE515A		MC1420G
NE515G		MC1520F
NE515K		MC1420G
NE516A		MC1420G
NE516G		MC1520F
NE516K		MC1420G
NE531G		MC1439G
NE531T		MC1439G
NE531V		MC1439P
NE533G		MC1776CG
NE533T		MC1776CG
NE533V		MC1776CG
NE537G		MC1456G
NE537T		MC1456G
NE540L		MC1554G
NE550A		MC1723CP
NE550L		MC1723CG
NE555JG	MC1455U	
NE555L	MC1455G	
NE555P	MC1455P1	
NE555T	MC1455G	
NE555V	MC1455P1	
NE556A	MC3456P	
NE556I	MC3456L	
NE565A	NE565N	
NE565K		NE565N
NE592A	NE592A	
NE592K	NE592K	
OP-01C		MC1536
OP-01G		MC1536
OP-01H		MC1536
OP-01J		MC1536G
OP-01L		MC1536G
OP-01P		MC1536P
OP-08		MC1776
OP-08A		MC1776
OP-08B		MC1776

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
OP-08C		MC1776
OP-08E		MC1776
PA239A		MC1303P
RC702T	MC1712CG	
RC709D	MC1709CL	
RC709DN	MC1709CP1	
RC709DP	MC1709CP2	
RC709T	MC1709CG	
RC710DC	MC1710CL	
RC710DP	MC1710CP	
RC710T	MC1710CG	
RC711DC	MC1711CL	
RC711DP	MC1711CP	
RC711T	MC1711CG	
RC723D	MC1723CL	
RC723T	MC1723CG	
RC733D	MC1733CL	
RC733T	MC1733CG	
RC741D	MC1741CL	
RC741DN	MC1741CP1	
RC741DP	MC1741CP2	
RC741Q	MC1741CF	
RC741T	MC1741CG	
RC747D	MC1747CL	
RC747T	MC1747CG	
RC748T	MC1748CG	
RC1414DC	MC1414L	
RC1414DP	MC1414P	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC8T13DD	MC8T13L	
RC1437D	MC1437L	
RC1437DP	MC1437P	
RC1458DN	MC1458P1	
RC1458T	MC1458G	
RC1556T	MC1456CG	
RC1558T	MC1558G	
RC3302DB	MC3302P	
RC4131DP		MC1471SCP1
RC4131T		MC1741SG
RC4136D		MC3403L
RC4136DP		MC3403P
RC4136J		MC3403L
RC4136N		MC3403P
RC4195T		MC1468G
RC4195TK		MC1468R
RC4444R	MC3416L	
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4558L	MC4558CG	
RC4558P	MC4558CP1	
RC4558T	MC4558CG	
RC8T13MP	MC8T13P	
RC8T14DD	MC8T14L	
RC8T14MP	MC8T14P	
RC8T23DD	MC8T23L	
RC8T23MP	MC8T23P	
RC8T24DD	MC8T24L	
RC8T24MP	MC8T24P	
RC75107AD	MC75107L	
RC75107ADP	MC75107P	
RC75108AD	MC75108L	
RC75108ADP	MC75108P	
RC75109D		MC75S110L
RC75109DP		MC75S110P
RC75110D	MC75S110L	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
RC75110DP	MC75S110P	
RC75325DD	MC75325L	
REF-01CJ		C1404U10
REF-01DJ		C1404U10
REF-01J		C1504AU10
REF-01HJ		C1404AU10
REF-02CJ		C1404U5
REF-02DJ		C1404U5
REF-02HJ		C1404AU5
REF-02J		C1504AU5
RM702Q	MC1712F	
RM702T	MC1721G	
RM709D	MC1709L	
RM709Q	MC1709F	
RM709T	MC1709G	
RM710D	MC1710L	
RM710T	MC1710G	
RM711DC	MC1711L	
RM711T	MC1711G	
RM723D	MC1723L	
RM723T	MC1723G	
RM733D	MC1733L	
RM733T	MC1733G	
RM741D	MC1741L	
RM741DP	MC1741P	
RM741Q	MC1741F	
RM741T	MC1741G	
RM747D	MC1747L	
RM747T	MC1747G	
RM748T	MC1748G	
RM1514DC	MC1514L	
RM1537D	MC1537L	
RM4136D		MC3503L
RM4136J		MC3503L
RM4195T		MC1568G
RM4195TK		MC1568R
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM4558L	MC4558G	
RM4558T	MC4558G	
RM55107AD	MC55107L	
RM55325DD	MC55325L	
RV3301DB	MC3301P	
S8T13E		MC8T13L
S8T14E		MC8T14L
S5556T	MC1556G	
S5558E	MC1558L	
S5558T	MC1558G	
S5596F	MC1596L	
S5596K	MC1596G	
S5709G	MC1709F	
S5709T	MC1709G	
S5710T	MC1710G	
S5711K	MC1711G	
S5723T	MC1723G	
S5733K	MC1733G	
S5741T	MC1741G	
SE501K		MC1733G
SE515G		MC1520F
SE515K		MC1520G
SE516A		MC1520G
SE516G		MC1520F
SE516K		MC1520G
SE528E		MC1544L
SE528R		MC1544L
SE531G		MC1539G
SE531T		MC1539G

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SE533G		MC1776G
SE533T		MC1776G
SE537G		MC1556G
SE537T		MC1556G
SE550L		MC1723G
SE555JG	MC1555U	
SE555L	MC1555G	
SE555T	MC1555G	
SE556A	MC3556L	
SE565A		MLM565CP
SE565K		MLM565CP
SE592A	SE592L	
SE592K	SE592G	
SG100T		MC1723G
SG101AD		LM101AH
SG101AT	LM101AH	
SG101J		LM101AH
SG101T	LM101AH	
SG104T	LM104H	
SG105N		LM105H
SG105T	LM105H	
SG107J		LM107H
SG107T	LM107H	
SG108AJ	LM108AJ	
SG108AT	LM108AH	
SG108J	LM108J	
SG108T	LM108H	
SG109K	LM109K	
SG109T	LM109H	
SG111D	LM111J	
SG111T	LM111H	
SG118J		MC1741SL
SG118T		MC1741SG
SG120K-05	LM120K-05	
SG120K-5 2		MC7905.2CK
SG120K-12	LM120K-12	
SG120K-15	LM120K-15	
SG120T-05	LM120T-05	
SG120T-5 2		MC7905 2CK
SG120T-12	LM120T-12	
SG120T-15	LM120T-15	
SG124J	LM124J	
SG140K-05	LM140K-5 0	
SG140K-06	LM140K-6 0	
SG140K-08	LM140K-8 0	
SG140K-12	LM140K-12	
SG140K-15	LM140K-15	
SG140K-18	LM140K-18	
SG140K-24	LM140K-24	
SG200T		MC1723G
SG201AD		LM201AH
SG201AM	LM201AN	
SG201AN		LM201AN
SG201AT	LM201AH	
SG201J		LM201AH
SG201M	LM201AN	
SG201N		LM201AN
SG201T	LM201AH	
SG204T	LM204H	
SG205N		LM205H
SG205T	LM205H	
SG207J		LM207H
SG207M		LM207H
SG207N		LM207H
SG207T	LM207H	
SG208AJ	LM208AJ	
SG208AM	LM208AJ-8	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG208AT	LM208AH	
SG208J	LM208J	
SG208M	LM208J-8	
SG208T	LM208H	
SG209K	LM209K	
SG209T	LM209H	
SG211D	LM211J	
SG211M	LM211N	
SG211T	LM211H	
SG218J		MC1741SL
SG218M		MC1741SL
SG218T		MC1741SG
SG224J	LM224J	
SG224N	LM224N	
SG300N		MC1723CP
SG300T		MC1723CG
SG301AD		LM301AH
SG301AM	LM301AN	
SG301AN		LM301AN
SG301AT	LM301AH	
SG304T	LM304H	
SG305AT		LM305H
SG305N		LM305H
SG305T	LM305H	
SG307J		LM307N
SG307M	LM307N	
SG307N		LM307N
SG307T	LM307H	
SG308AJ	LM308AJ	
SG308AM	LM308AN	
SG308AT	LM308AH	
SG308J	LM308J	
SG308M	LM308N	
SG308T	LM308H	
SG309K	LM309K	
SG309T	LM309H	
SG311D	LM311J	
SG311M	LM311N	
SG311T	LM311H	
SG318J		MC1741SCL
SG318M		MC1741CP1
SG318T		MC1741CG
SG320K-05	LM320K-5.0	
SG320K-5 2		MC7905 2CK
SG320K-12	LM320K-12	
SG320K-15	LM320K-15	
SG320T-05	LM320T-5 0	
SG320T-5 2		MC7905.2CT
SG320T-12	LM320T-12	
SG320T-15	LM320T-15	
SG324J	LM324J	
SG324N	LM324N	
SG340K-05	MC7805CK	
SG340K-06	MC7806CK	
SG340K-08	MC7808CK	
SG340K-12	MC7812CK	
SG340K-15	MC7815CK	
SG340K-18	MC7818CK	
SG340K-24	MC7824CK	
SG555CM	MC1455P1	
SG555CT	MC1455G	
SG555T	MC1555G	
SG556CJ	MC3456L	
SG556CN	MC3456P	
SG556J	MC3556L	
SG556N	MC3556L	
SG710CD	MC1710CL	
SG710CN	MC1710CP	
SG710CT	MC1710CG	
SG710D	MC1710L	
SG710N	MC1710CP	
SG710T	MC1710G	
SG711CD	MC1711CL	
SG711CN	MC1711CP	
SG711CT	MC1711CG	
SG711D	MC1711L	
SG711N	MC1711CP	
SG711T	MC1711G	
SG723CD	MC1723CL	
SG723CN	MC1723CP	
SG723CT	MC1723CG	
SG723D	MC1723L	
SG723T	MC1723G	
SG733CD	MC1733CL	
SG733CN		MC1733CP
SG733CT	MC1733CG	
SG733D	MC1733L	
SG733N		MC1733L
SG733T	MC1733G	
SG741CD	MC1741CL	
SG741CF	MC1741CF	
SG741CM	MC1741CP1	
SG741CN	MC1741CP2	
SG741CT	MC1741CG	
SG741D	MC1741L	
SG741F	MC1741F	
SG741T	MC1741G	
SG741SCM	MC1741SCP1	
SG741SCT	MC1741SCG	
SG741ST	MC1741SG	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747CT	MC1747CG	
SG747J	MC1747L	
SG747T	MC1747G	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG748CT	MC1748CG	
SG748D		MC1748G
SG748T	MC1748G	
SG777CJ		LM308AJ
SG777CM		LM308AN
SG777CN		LM308AN
SG777CT		LM308AH
SG777J		LM108AJ
SG777T		LM108AH
SG1118AJ		LM108AJ
SG1118AT		LM108AH
SG1118J		LM108J
SG1118T		LM108H
SG1217		MC1741G
SG1217J		MC1741SL
SG1217T		MC1741SG
SG1250T		MC1776G
SG1401N		MC1533G
SG1401T		MC1533G
SG1402N		MC1594L
SG1402T		MC1594L
SG1436CT	MC1436CG	
SG1436M	MC1436U	
SG1436T	MC1436G	
SG1456CT	MC1456CG	
SG1456T	MC1456G	
SG1458M	MC1458P1	
SG1458T	MC1458G	
SG1468J	MC1468L	
SG1468N	MC1468L	
SG1468T	MC1468G	
SG1495D	MC1495L	
SG1495N	MC1495L	
SG1496D	MC1496L	
SG1496N		MC1496L
SG1496T	MC1496G	
SG1501AD		MC1568L
SG1501AT		MC1568G
SG1501D	MC1568L	
SG1501T	MC1568G	
SG1502D		MC1568L
SG1502N		MC1568L
SG1503	MC1503U	
SG1524J		MC3520L
SG1536T	MC1536G	
SG1556T	MC1556G	
SG1558T	MC1558G	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG1596T	MC1596G	
SG1660D		LM301AH
SG1660J		LM308J
SG1660M		LM308N
SG1660T		LM308H
SG1760D		LM307H
SG1760F		LM307H
SG1760J		LM308J
SG1760M		LM&08N
SG1760T		LM308H
SG2118AJ		LM208AJ
SG2118AM		LM208AJ-8
SG2118AT		LM208AH
SG2118J		LM208J
SG2118M		LM208J-8
SG2118T		LM208H
SG2250T		MC1776G
SG2401N		MC1433G
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501AT		MC1468G
SG2501D	MC1468L	
SG2501N	MC1468L	
SG2501T	MC1468G	
SG2502D		MC1468L
SG2502N		MC1468L
SG2502T		MC1468G
SG2503	MC1403AU	
SG2524J		MC3520L
SG3118AJ		MLM308AL
SG3118AM		MLM308AP1
SG3118AT		MLM308AG
SG3118J		MLM308L
SG3118M		MLM308P1
SG3118T		MLM308G
SG3250T		MC1776G
SG3401N		MC1433G
SG3401T		MC1433G
SG3402N		MC1494L
SG3402T		MC1494L
SG3501AD	MC1468L	
SG3501AT	MC1468G	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG3501D	MC1468L	
SG3501N	MC1468L	
SG3501T	MC1468G	
SG3502D		MC1468L
SG3502G		MC1468G
SG3502N		MC1468L
SG3503	MC1403U	
SG3524J		MC3420L
SG4250CM		MC1776CP1
SG4250CT		MC1776CG
SG4250T		MC1776G
SG4501D	MC1468L	
SG4501N	MC1468L	
SG4501T	MC1468G	
SG7805CK	MC7805CK	
SG7805K		MC7805CK
SG7806CK	MC7806CK	
SG7806K		MC7806CK
SG7808CK	MC7808CK	
SG7808K		MC7808CK
SG7812CK	MC7812CK	
SG7812K		MC7812CK
SG7815CK	MC7815CK	
SG7815K		MC7815CK
SG7818CK	MC7818CK	
SG7818K		MC7818CK
SG7824CK	MC7824CK	
SG7824K		MC7824CK
SH0013HC		MMH0026CG
SH0013HM		MMH0026G
SH2001FC		MC75462P
SH2001FM		MC75462P
SH2001HC		MC75462P
SH2001HM		MC75462P
SH2002FC		MC75462P
SH2002FM		MC75462P
SH2002HC		MC75462P
SH2002HM		MC75462P
SH2002HC		MC75462P
SH2200FC		MC75462P
SH2200FM		MC75462P
SH2200HC		MC75462P
SH2200HM		MC75462P
SH2200PC		MC75462P
SH8090FM		MC1508L8
SN5510FA	MC1510F	
SN5510L	MC1510G	
SN52101AL	LM101AH	
SN52104L	LM101H	
SN52105L	LM105H	
SN52106J		MC1710L
SN52106L		MC1710G
SN52107L	LM107H	
SN52108AL	LM108AH	
SN52108L	LM108H	
SN52109L	LM109H	
SN52510J		MC1710L
SN52510L		MC1710G
SN52514J	MC1514L	
SN52555L	MC1555G	
SN52558L	MC1558G	
SN52702AFA		MC1712F
SN52702AJ		MC1712L
SN52702AL		MC1712G
SN52702FA	MC1712F	
SN52702J	MC1712L	
SN52702L	MC1712G	
SN52709AFA	MC1709AF	
SN52709AJ	MC1709AL	
SN52709AL	MC1709AG	
SN52709FA	MC1709F	
SN52709J	MC1709L	
SN52709L	MC1709G	
SN52710FA	MC1710F	
SN52710J	MC1710L	
SN52710L	MC1710G	
SN52711FA	MC1711F	
SN52711J	MC1711L	
SN52711L	MC1711G	
SN52723FA	MC1723F	
SN52723J	MC1723L	
SN52723L	MC1723G	
SN52733J	MC1733L	
SN52733L	MC1733G	
SN52741FA	MC1741F	
SN52741J	MC1741L	
SN52741L	MC1741G	
SN52747FA	MC1747F	
SN52747J	MC1747L	
SN52747L	MC1747G	
SN52748L	MC1748G	
SN52770L		MC1556G
SN52771L		MC1556G
SN52810FA		MC1710F
SN52810J		MC1710L
SN52810L		MC1710G
SN52811FA		MC1711F
SN52811J		MC1711L
SN52811L		MC1711G
SN55107AJ	MC55107L	
SN55107BJ		MC55107L
SN55108AJ	MC55108L	
SN55108BJ		MC75108L
SN55109J		MC75S110L
SN55110J		MC75S110L
SN55244J	MC1544L	
SN55325J	MC55325L	
SN72301AL	LM301AH	
SN72301AP	LM301AN	
SN72304L	LM304H	
SN72305AL		LM305H
SN72305L	LM305H	
SN72306J		MC1710CL
SN72306L		MC1710CG
SN72306N		MC1710CP
SN72307L	LM307H	
SN72308AL	LM308AH	
SN72308L	LM308H	
SN72309L	LM309H	
SN72311L	LM311H	
SN72311P	LM311N	
SN72376L		LM305H
SN72440J		MC3370P
SN72440N		MC3370P
SN72510J		MC1710CL
SN72510L		MC1710CG
SN72510N		MC1710CP
SN72514J		MC1414L
SN72514N		MC1414P
SN72555L	MC1455G	
SN72555P	MC1455P1	
SN72558L	MC1458G	
SN72558P	MC1458P1	
SN72702J	MC1712CL	
SN72702L	MC1712CG	
SN72709J	MC1709CL	
SN72709L	MC1709CG	
SN72709N	MC1709CP2	
SN72709P	MC1709CP1	
SN72710J	MC1710CL	
SN72710L	MC1710CG	
SN72710N	MC1710CP	
SN72711J	MC1711CL	
SN72711L	MC1711CG	
SN72711N	MC1711CP	
SN72720J		MC1710CL
SN72720L		MC1710CG
SN72720N		MC1710CP
SN72723J	MC1723CL	
SN72723L	MC1723CG	
SN72733J	MC1733CL	
SN72733L	MC1733CG	
SN72741FA	MC1741CF	
SN72741J	MC1741CL	
SN74741L	MC1741CG	
SN72741N	MC1741CP2	
SN72741P	MC1741CP1	
SN72747FA	MC1747CF	
SN72747J	MC1747CL	
SN72747L	MC1747CG	
SN72747N	MC1747CP2	
SN72748L	MC1748CG	
SN72748P	MC1748CP1	
SN72770L		MC1456G
SN72771L		MC1456G
SN72810J		MC1710CL
SN72810L		MC1710CG
SN72810N		MC1710CP
SN72811J		MC1711CL
SN72811L		MC1711CG
SN72811N		MC1711CP
SN72905	MC7905CT	
SN72906	MC7906CT	
SN72908	MC7908CT	
SN72912	MC7912CT	
SN72915	MC7915CT	
SN72L022P		LM358N
SN72L044JA		LM324N
SN72L044N		LM324N
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75121J	MC8T13L	
SN75121N	MC8T13P	
SN75122J	MC8T14L	
SN75122N	MC8T14P	
SN75123J	MC8T23L	
SN75123N	MC8T23P	
SN75124J	MC8T24L	
SN75124N	MC8T24P	
SN75125J	MC75125L	
SN75125N	MC75125P	
SN75126J		MC3481/5L
SN75126N		MC3481/5P
SN75127J	MC75127L	
SN75127N	MC75127P	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

SN75128J -- TL494CN

PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN75128J	MC75128L	
SN75128N	MC75128P	
SN75129J	MC75129L	
SN75129N	MC75129P	
SN75138N		MC3443P
SN75138J		MC3443P
SN75140P	MC75140P1	
SN75150J		MC1488L
SN75150N		MC1488P
SN75154J		MC1489L
SN75154N		MC1489P
SN75188J	MC1488L	
SN75188N	MC1488P	
SN75189AJ	MC1489AL	
SN75189J	MC1489L	
SN75189AN	MC1489AP	
SN75189N	MC1489P	
SN75207J		MC75107L
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75261N		MC3245L
SN75322N		MC3245P
SN75362P		MMH0026CP
SN75365J	MC75365L	
SN75365N	MC75365P	
SN75368J	MC75368L	
SN75368N	MC75368P	
SN75369P	MMH0026CP1	
SN75450AJ	MC75450L	
SN75450AN	MC75450P	
SN75450BN		MC75450P
SN75450N	MC75450P	
SN75451AP	MC75451P	
SN75451P	MC75451P	
SN75452P	MC75452P	
SN75453P	MC75453P	
SN75454P	MC75454P	
SN75460AJ	MC75460L	
SN75460AN	MC75460P	
SN75461	MC75461	
SN75461AP	MC75461P	
SN75462	MC75462	
SN75462AP	MC75462P	
SN75463	MC75463	
SN75463AP	MC75463P	
SN75464	MC75464	
SN75464AP	MC75464P	
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475P	MC1472P1	
SN75475JG	MC1472U	
SN75491N	MC75491P	
SN75492N	MC75492P	
SN76000P		MC1306P
SN76104N		MC1310P
SN76105N		MC1310P
SN76111N		MC1310P
SN76113N		MC1310P
SN76115N	MC1310P	
SN76116N		MC1310P
SN76117N		MC1310P
SN76130N		MC1303P
SN76131N		MC1303P
SN76149N		MC1303P
SN76242N		MC1399P
SN76243N		MC1399P
SN76246N		MC1323P
SN76298N	MC1398P	
SN76514L		MC1496G
SN76514N	MC1496P	
SN76564N	MC1364P	
SN76565N	MC1364P	
SN76591P	MC1391P	
SN76594P	MC1394P	
SN76600P	MC1350P	
SN76642N	MC1357P	
SN76644N		MC1352P
SN76650N	MC1352P	
SN76651N	MC1351P	
SN76653N		MC1352P
SN76660N		MC1357P
SN76665N	MC1364P	
SN76666N	MC1358P	
SN76669N	MC1356P	
SN76675N	MC1375P	
SN76678P		MC1355P
SSS101AL		LM101AH
SSS101AJ	LM101AH	
SSS107J	LM107H	
SSS107P		LM107H
SSS201AJ	LM201AH	
SSS201AL		LM201AH
SSS201AP		LM201AN
SSS207J	LM207H	
SSS207P		LM207H
SSS301AJ	LM301AH	
SSS301AL		LM301AH
SSS301AP	LM301AN	
SSS741BJ		MC1741G
SSS741BL		MC1741F
SSS741BP	MC1741P2	
SSS741CJ		MC1741CG
SSS741CL		MC1741CF
SSS741CP	MC1741CP2	
SSS741GJ	MC1741SG	
SSS741GP		MC1741SG
SSS741J		MC1741G
SSS741L		MC1741F
SSS741P		MC1741P2
SSS747B2	MC1747F	
SSS747BP		MC1747L
SSS747CK		MC1747CG
SSS747CM		MC1747CF
SSS747CP		MC1747CL
SSS747GK		MC1747G
SSS747GM	MC1747F	
SSS747GP		MC1747L
SSS747L		MC1747F
SSS747P		MC1747L
SSS1408A-6Z	MC1408L6	
SSS1408A-7Z	MC1408L7	
SSS1408A-8Z	MC1408L8	
SSS1458J	MC1458G	
SSS1508A-8Z	MC1508L8	
SSS1558J	MC1558G	
TAA630		MC1327P
TBA120S		MC1358P
TBA440		MC1352P
TBA520		MC1327P
TBA920		MC1391P
TBA920S		MC1391P
TBA940		MC1344P
TBA950		MC1344P
TBA990		MC1327P
TBA1190Z	TBA1190Z	
TDA1190Z	TDA1190Z	
TDA2002	TDA2002	
TL022CJG		LM358J
TL022CL		LM358H
TL022CP		LM358N
TL022MJG		LM158J
TL022ML		LM158H
TL044CJ		LM324J
TL044CN		LM324N
TL044MJ		LM124J
TL071ACJG		MC34001BU
TL071ACL		MC34001BG
TL071ACP		MC34001BP
TL071BCJG		MC34001AU
TL071BCL		MC34001AG
TL071BCP		MC34001AP
TL071CJG		MC34001U
TL071CL		MC34001G
TL071CP		MC34001P
TL072ACJG		MC34002BU
TL072ACL		MC34002BG
TL072ACP		MC34002BP
TL072BCJG		MC34002AU
TL072BCL		MC34002AG
TL072BCP		MC34002AP
TL072CJG		MC34002U
TL072CL		MC34002G
TL072CP		MC34002P
TL074ACJ		MC34004BL
TL074ACN		MC34004BP
TL074BCJ		MC34004A
TL074BCN		MC34004AP
TL074CJ		MC34004L
TL074CN		MC34004P
TL081ACJG		MC34001BU
TL081ACL		MC34001BG
TL081ACP		MC34001BP
TL081BCJG		MC34001AU
TL081BCL		MC34001AG
TL081BCP		MC34001AP
TL081CJG		MC34001U
TL081CL		MC34001G
TL081CP		MC34001P
TL082ACJG		MC34002BU
TL082ACL		MC34002BG
TL082ACP		MC34002BP
TL082BCJG		MC34002AU
TL082BCL		MC34002AG
TL082BCP		MC34002AP
TL082CJG		MC34002U
TL082CL		MC34002G
TL082CP		MC34002P
TL084ACJ		MC34004BL
TL084ACN		MC34004BP
TL084BCJ		MC34004AL
TL084BCN		MC34004AP
TL084CJ		MC34004L
TL084CN		MC34004P
TL494CJ	TL494CJ	
TL494CN	TL494CN	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

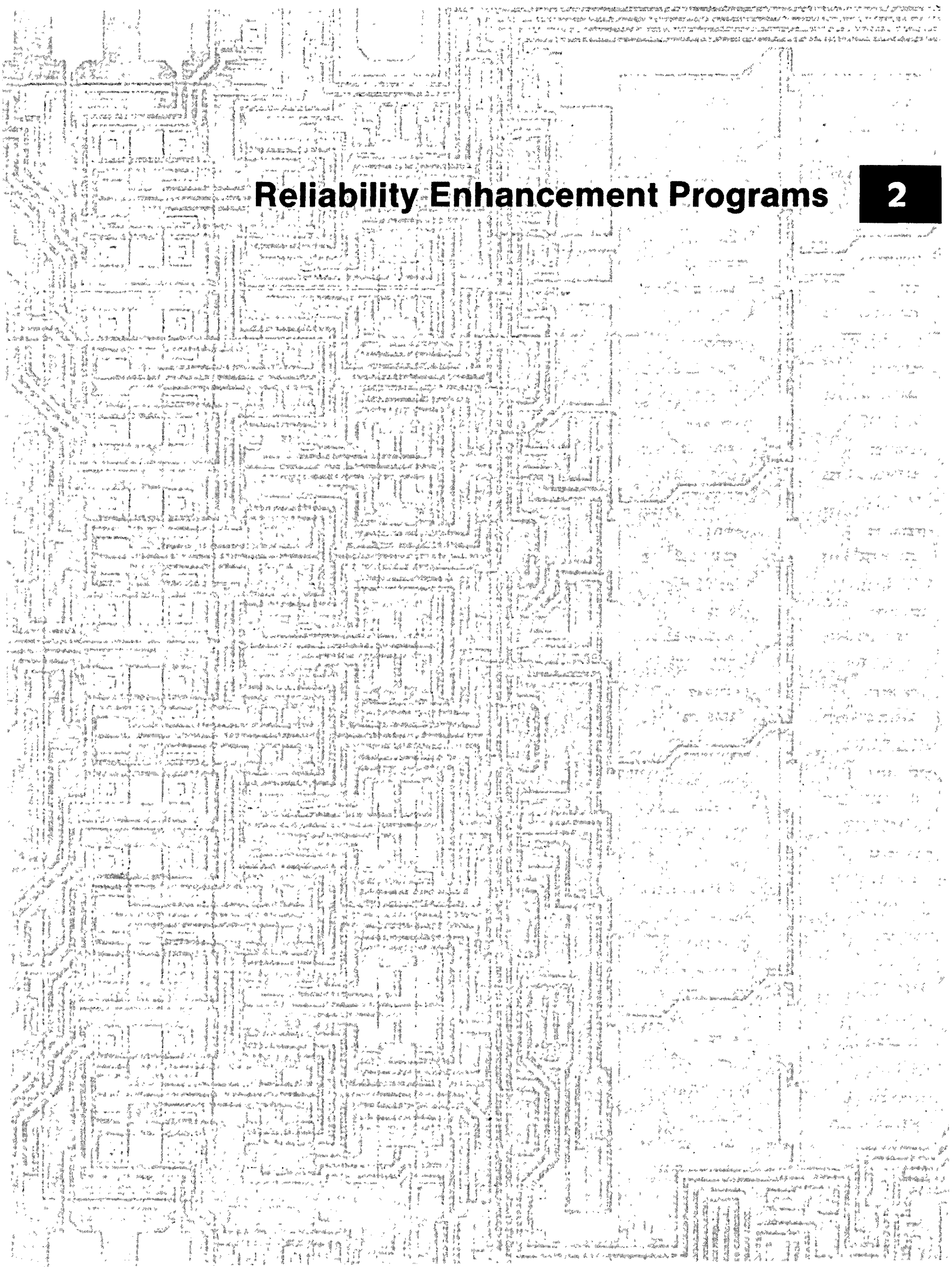
PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
TL495CJ	TL495CJ	
TL495CN	TL495CN	
TL497CJ		MC3420L
TL497CN		MC3420P
TL497MJ		MC3520L
UDN5711M	MC1471P1	
UDN5712M	MC1472P1	
UDN5713M	MC1473P1	
UDN5714M	MC1474P1	
UDN-6144A		MC3490P
UDN-6164A		MC3490P
UDN-6184A		MC3490P
UDN-7183A		MC3491P
UDN-7184A		MC3491P
UDN-7186A		MC3491P
UHD-490		MC3494P
UHD-491		MC3494P
UHP-490		MC3494P
UHP-491		MC3494P
UHP-495		MC3490P
ULN2001A	ULN2001A	
ULN2002A	ULN2002A	
ULN2003A	ULN2003A	
ULN2004A	ULN2004A	
ULN2111A	MC1357P	
ULN2111N	MC1357PQ	
ULN2113A		MC1357P
ULN2113N		MC1357P
ULN2114A		MC1323P
ULN2114K		MC1323P
ULN2114N		MC1323P
ULN2120A		MC1310P
ULN2121A		MC1310P
ULN2122A		MC1310P
ULN2124A		MC1399P
ULN2125A		MC1344P
ULN2127A		MC1399P
ULN2128A		MC1310P
ULN2136A	MC1356P	
ULN2139D		MC1439G
ULN2139G		MC1439G
ULN2139H		MC1439P2
ULN2139M		MC1439P1
ULN2151D		MC1741CG
ULN2151G		MC1741CF
ULN2151H		MC1741CP2
ULN2151M		MC1741CP1
ULN2156D		MC1456G
ULN2156G		MC1456G
ULN2156H		MC1456G
ULN2156M		MC1456G
ULN2157A		MC1458P2
ULN2157H		MC1458P2
ULN2157K		MC1458G
ULN2165A	MC1358P	
ULN2165N	MC1358PQ	
ULN2209A		MC1356P
ULN2210A	MC1310P	
ULN2224A	MC1324P	
ULN2228A		MC1323P
ULN2244A		MC1310P
ULN2262A		MC1399P
ULN2264A	MC1364P	
ULN2267A		MC1323P
ULN2298A	MC1398P	
ULN2741D		MC1741CG
ULN2747A		MC1747CL
ULS2139D		MC1539G
ULS2139G		MC1539G
ULS2139H		MC1539L
ULS2139M		MC1439P1
ULS2151D		MC1741G
ULS2151G		MC1741F
ULS2151H		MC1741L
ULS2151M		MC1741CP1
ULS2156D		MC1556G
ULS2156G		MC1556G
ULS2156H		MC1556G
ULS2156M		MC1556G
ULS2157A		MC1558L
ULS2157H		MC1558L
ULS2157K		MC1558G
μA0802DC-1	MC1408L8	
μA0802DC-2	MC1408L7	
μA0802DC-3	MC1408L6	
μA0802DM-1	MC1508L8	
μA0802PC-1	MC1408P8	
μA0802PC-2	MC1408P7	
μA0802PC-3	MC1408P6	
μA101AD		LM101AJ
μA101AF		LM101AJ
μA101AH	LM101AH	
μA101D		LM101AJ
μA101F		LM101AJ
μA101H	LM101AH	
μA104HM	LM104H	
μA105HM	LM105H	
μA107H	LM107H	
μA108AD	LM108AJ	
μA108AF	LM108AF	
μA108AH	LM108AH	
μA108D	LM108J	
μA108F	LM108F	
μA108H	LM108H	
μA109KM	LM109K	
μA201AD		LM201AJ
μA201AF		LM201AJ
μA201AH	LM201AH	
μA201D		LM201AJ
μA201F		LM201AJ
μA201H	LM201AH	
μA207H	LM207H	
μA208AD	LM208AJ	
μA208AF	LM208AF	
μA208AH	LM208AH	
μA208D	LM208J	
μA208F	LM208F	
μA208H	LM208H	
μA209KM	LM209K	
μA301AD		LM301AJ
μA301AH	LM301AH	
μA301AT	LM301AN	
μA304HC	LM304H	
μA305HC		LM305H
μA305HC	LM305H	
μA307H	LM307H	
μA307T	LM307N	
μA308AD	LM308AJ	
μA308AH	LM308AH	
μA308D	LM308J	
μA308H	LM308H	
μA309KC	LM309K	
μA311T	LM311N	
μA376TC		LM305H
μA555HC	MC1455G	
μA555HM	MC1555G	
μA555TC	MC1455P1	
μA556DC	MC3456L	
μA556DM	MC3556L	
μA556PC	MC3456P	
μA702DC	MC1712CL	
μA702DM	MC1712L	
μA702FM	MC1712F	
μA702HC	MC1712CG	
μA702HM	MC1712G	
μA702MJ	MC1712L	
μA702ML	MC1712G	
μA709ADM	MC1709AL	
μA709AFM	MC1709AF	
μA709AHM	MC1709AG	
μA709AMJ	MC1709AL	
μA709AMJG	MC1709AU	
μA709AML	MC1709AG	
μA709CJ	MC1709CL	
μA709CJG	MC1709CU	
μA709CL	MC1709CG	
μA709CN	MC1709CP2	
μA709CP	MC1709CP1	
μA709DC	MC1709CL	
μA709DM	MC1709L	
μA709FM	MC1709F	
μA709HC	MC1709CG	
μA709HM	MC1709G	
μA709MJ	MC1709L	
μA709MJG	MC1709U	
μA709ML	MC1709G	
μA709TC	MC1709CP1	
μA709PC	MC1709CP2	
μA710DC	MC1710CL	
μA710DM	MC1710L	
μA710HC	MC1710CG	
μA710HM	MC1710G	
μA710PC	MC1710CP	
μA711DC	MC1711CL	
μA711DM	MC1711L	
μA711HC	MC1711CG	
μA711HM	MC1711G	
μA711PC	MC1711CP	
μA715DC		MC1741SCL
μA715DM		MC1741SL
μA715HC		MC1741SCG
μA715HM		MC1741SG
μA723CJ	MC1723CL	
μA723CL	MC1723CG	
μA723CN	MC1723CP	
μA723DC	μA723DC	
μA723DM	MC1723L	
μA723HC	μA723HC	
μA723HM	MC1723G	
μA723MJ	MC1723L	
μA723ML	MC1723G	
μA723PC	μA723PC	
μA725AHM		LM108AH
μA725EHC		LM308AH
μA725HC		LM308AH
μA725HM		LM108AH
μA727HC		MC1420G
μA727HM		MC1520G
μA730HC		MC1420G
μA730HM		MC1520G
μA732DC		MC1310P

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA732PC		MC1310P
μA733CJ	MC1733CL	
μA733CL	MC1733CG	
μA733CN	MC1733CP	
μA733DC	MC1733CL	
μA733DM	MC1733L	
μA733FM	MC1733F	
μA733HC	MC1733CG	
μA733HM	MC1733G	
μA733MJ	MC1733L	
μA733ML	MC1733G	
μA734DC		LM311J
μA734DM		LM311J
μA734HC		LM311H
μA734HM		LM311H
μA740HC		LF355H
μA740HM		LF155H
μA741ADM		MC1741L
μA741AFM		MC1741F
μA741AHM		MC1741G
μA741CJ	MC1741CL	
μA741CJG	MC1741CU	
μA741CL	MC1741CG	
μA741CN	MC1741CP2	
μA741CP	MC1741CP1	
μA741DC	μA741DC	
μA741DM	MC1741L	
μA741EDC		MC1741L
μA741EHC		MC1741G
μA741FC	MC1741CF	
μA741FM	MC1741F	
μA741HC	μA741HC	
μA741HM	MC1741G	
μA741MJ	MC1741L	
μA741MJG	MC1741U	
μA741ML	MC1741G	
μA741RC	MC1741CU	
μA741RM	MC1741U	
μA741PC	MC1741CP2	
μA741TC	μA741TC	
μA742DC		CA3059
μA746DC		MC1323P
μA746HC		MC1323P
μA747ADM		MC1747L
μA747AHM		MC1747G
μA747CJ	MC1741CL	
μA747CL	MC1747CG	
μA747CN	MC1747CP2	
μA747DC	MC1747CL	
μA747DM	MC1747L	
μA747EDC	MC1747CCBM	
μA747EHC	MC1747CICM	
μA747HC	MC1747CG	
μA747HM	MC1747G	
μA747MJ	MC1747L	
μA747ML	MC1747G	
μA747PC	MC1747CP2	
μA748AFM		MC1748F
μA748AHM		MC1748G
μA748CJ	MC1748CL	
μA748CJG	MC1748CU	
μA748CL	MC1748CG	
μA748CN	MC1748CP2	
μA748CP	MC1748CP1	
μA748DC	MC1748CL	
μA748DM	MC1748L	
μA748FM	MC1748F	
μA748HC	MC1748CG	
μA748HM	MC1748G	
μA748MJ	MC1748L	
μA748MJG	MC1748U	
μA748ML	MC1748G	
μA748TC	MC1748CP1	
μA749DC		MC1435L
μA749DHC		MC1435G
μA749DM		MC1535L
μA749HC		MC1435G
μA753TC		MC1356P
μA754HC		MC1355P
μA754TC		MC1355P
μA757DC		MC1350P
μA757DM		MC1350P
μA758DC		MC1310P
μA758PC		MC1310P
μA767DC		MC1310P
μA767PC		MC1310P
μA772		MC1741S
μA775DC	LM339J	
μA775DM	LM339J	
μA775PC	LM339N	
μA776DC		MC1776CG
μA776DM		MC1776G
μA776HC	MC1776CG	
μA776HM	MC1776G	
μA776TC	MC1776CP1	
μA777CJ		LM308AJ-8
μA777CJG		LM308AJ-8
μA777CL		LM308AH
μA777CN		LM308AN
μA777CP		LM308AN
μA777DC		LM308AJ-8
μA777HC		LM308AH
μA777MJ		LM108AJ-8
μA777MJG		LM108AJ-8
μA777ML		LM108AH
μA777TC		LM308AN
μA780DC		MC1399P
μA780PC		MC1399P
μA781DC		MC1399P
μA781PC		MC1399P
μA786DC		MC1327P
μA787PC		MC1399P
μA791KC		MC1438R
μA791KM		MC1538R
μA791P5		MC1438R
μA796HC	MC1496G	
μA796HM	MC1596G	
μA796DC	MC1496L	
μA796DM	MC1596L	
μA798HC	MC3458G	
μA798HM	MC3558G	
μA798RC	MC3458U	
μA798RM	MC3558U	
μA798TC	MC3458P1	
μA799HC		MC1741G
μA799HM		MC1741G
μA1312PC	MC1312P	
μA1314PC	MC1314P	
μA1315PC	MC1315P	
μA1391PC	MC1391P	
μA1394PC	MC1394P	
μA1458CHC	MC1458CG	
μA1458CP	MC1458CP1	
μA1458CRC	MC1458CU	
μA1458CTC	MC1458CP1	
μA1458E	MC1458G	
μA1458HC	MC1558G	
μA1458P	MC1458P1	
μA1458RC	MC1458U	
μA1458TC	MC1458P1	
μA1558E	MC1558G	
μA1558HM	MC1558G	
μA2136PC	MC1356P	
μA2240DC		MC1455U
μA2240DM		MC1555G
μA2240PC		MC1455P1
μA3026HM		CA3054
μA3045		MC3346P
μA3046DC	MC3346P	
μA3054DC	CA3054P	
μA3064PC	MC1364P	
μA3065PC	MC1358P	
μA3086DM	MC3386P	
μA3301P	MC3301P	
μA3302P	MC3302P	
μA3303P	MC3303P	
μA3401P	MC3401P	
μA3403D	MC3403L	
μA3403P	MC3403P	
μA4136DC		MC4741CL
μA4136DM		MC4741L
μA4136PC		MC4741CP
μA4558HC	MC4558CG	
μA4558HM	MC4558G	
μA4558TC	MC4558CP1	
μA7805CKC	MC7805CT	
μA7805KC	MC7805CK	
μA7805KM	MC7805K	
μA7805UC	MC7805CT	
μA7806CKC	MC7806CT	
μA7806KC	MC7806CK	
μA7806KM	MC7806K	
μA7806UC	MC7806CT	
μA7808CKC	MC7808CT	
μA7808KC	MC7808CK	
μA7808KM	MC7808K	
μA7808UC	MC7808CT	
μA7812CKC	MC7812CT	
μA7812KC	MC7812CK	
μA7812KM	MC7812K	
μA7812UC	MC7812CT	
μA7815CKC	MC7815CT	
μA7815KC	MC7815CK	
μA7815KM	MC7815K	
μA7815UC	MC7815CT	
μA7818CKC	MC7818CT	
μA7818KC	MC7818CK	
μA7818KM	MC7818K	
μA7818UC	MC7815CT	
μA7824CKC	MC7824CT	
μA7824KC	MC7824CK	
μA7824KM	MC7824K	
μA7824UC	MC7824CT	
μA78GHM		LM117K
μA78GKC		LM117K
μA78GKM		LM117K
μA78GU1C		LM317T
μA78H05KC		MC7805CK
μA78L02ACJG		MC78L02ACG
μA78L05ACJG		MC78L05ACG
μA78L05ACLP	MC78L05ACP	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA78L05AHC	MC78L05ACG	
μA78L05AWC	MC78L05ACP	
μA78L05CJG		MC78L05CG
μA78L05CLP	MC78L05CP	
μA78L05HC	MC78L05CG	
μA78L05WC	MC78L05CP	
μA78L06ACJG		MC78L06ACG
μA78L06ACLP	MC78L06ACP	
μA78L06CJG		MC78L06CG
μA78L06CLP	MC78L06CP	
μA78L08ACJG		MC78L08ACG
μA78L08ACLP	MC78L08ACP	
μA78L08CJG		MC78L08CG
μA78L08CLP	MC78L08CP	
μA78L12ACJG		MC78L12ACG
μA78L12ACLP	MC78L12ACP	
μA78L12AHC	MC78L12ACG	
μA78L12AWC	MC78L12ACP	
μA78L12CJG		MC78L12CG
μA78L12CLP	MC78L12CP	
μA78L12HC	MC78L12CG	
μA78L12WC	MC78L12CP	
μA78L15ACJG		MC78L15ACG
μA78L15ACLP	MC78L15ACP	
μA78L15AHC	MC78L15ACG	
μA78L15AWC	MC78L15ACP	
μA78L15CJG		MC78L15CG
μA78L15CLP	MC78L15CP	
μA78L15HC	MC78L15CG	
μA78L15WC	MC78L15CP	
μA78L26AWC	MC7802ACP	
μA78MGHC		LM317H
μA78MGT2C		LM317T
μA78MGU1C		LM317T
μA78M05CKC	MC78M05CT	
μA78M05HC	MC78M05CG	
μA78M05HM		MC78M05CG
μA78M05UC	MC78M05CT	
μA78M06CKC	MC78M06CT	
μA78M06HC	MC78M06CG	
μA78M06HM		MC78M06CG
μA78M06UC	MC78M06CT	
μA78M08CKC	MC78M08CT	
μA78M08HC	MC78M08CG	
μA78M08HM		MC78M08CG
μA78M08UC	MC78M08CT	
μA78M12CKC	MC78M12CT	
μA78M12HC	MC78M12CG	
μA78M12HM		MC78M12CG
μA78M12UC	MC78M12CT	
μA78M15CKC	MC78M15CT	
μA78M15HC	MC78M15CG	
μA78M15HM		MC78M15CG
μA78M15UG	MC78M15CT	
μA78M18HC	MC78M18CG	
μA78M18HM		MC78M18CG
μA78M18UG	MC78M18CT	
μA78M20CKC	MC78M20CT	
μA78M20HC	MC78M20CG	
μA78M20HM		MC78M20CG
μA78M20UG	MC78M20CT	
μA78M24CKC	MC78M24CT	
μA78M24HC	MC78M24CG	
μA78M24HM		MC78M24CG
μA78M24UC	MC78M24CT	
μA7902KC	MC7902K	
μA7902KM		MC7902K
μA7902UC	MC7902CT	
μA7905KC	MC7905CK	
μA7905KM		MC7905CK
μA7905UC	MC7905CT	
μA7906KC	MC7906CK	
μA7906KM		MC7906CK
μA7906UC	MC7906CT	
μA7908KC	MC7908CK	
μA7908KM		MC7908CK
μA7908UC	MC7908CT	
μA7912KC	MC7912CK	
μA7912KM		MC7912CK
μA7912UC	MC7912CT	
μA7915KC	MC7915CK	
μA7915KM		MC7915CK
μA7915UC	MC7915CT	
μA7918CKC	MC7918CT	
μA7918KC	MC7918CK	
μA7918KM		MC7918CK
μA7918UC	MC7918CT	
μA7924CKC	MC7924CT	
μA7924KC	MC7924CK	
μA7924KM		MC7924CK
μA7924UC	MC7924CT	
μA79L05AHC	MC79L05ACG	
μA79L05AWC	MC79L05ACP	
μA79L05HC	MC79L05CG	
μA79L05WC	MC79L05CP	
μA79L12AHC	MC79L12ACG	
μA79L12AWC	MC79L12ACP	
μA79L12HC	MC79L12CG	
μA79L12WC	MC79L12CP	
μA79L15AHC	MC79L15ACG	
μA79L15AWC	MC79L15ACP	
μA79L15HC	MC79L15CG	
μA79L15WC	MC79L15CP	
μA79M05AHM		MC7905CK
μA79M05AUC		MC7905CT
μA79M05CKC	MC7905CT	
μA79M05HM		MC7905CK
μA79M05UC		MC7905CT
μA79M06AHM		MC7906CK
μA79M06AUC		MC7906CT
μA79M06CKC	MC7906CT	
μA79M06HM		MC7906CK
μA79M06UC		MC7906CT
μA79M08AHM		MC7908CK
μA79M08AUC		MC7908CT
μA79M08CKC	MC7908CT	
μA79M08HM		MC7908CK
μA79M08UC		MC7908CT
μA79M12AHM		MC7912CK
μA79M12AUC		MC7912CT
μA79M12CKC	MC7912CT	
μA79M12HM		MC7912CK
μA79M12UC		MC7912CT
μA79M15AHM		MC7915CK
μA79M15AUC		MC7915CT
μA79M15CKC	MC7915CT	
μA79M15HM		MC7915CK
μA79M15UC		MC7915CT
μA79M18AHM		MC7918CK
μA79M18AUC		MC7918CT
μA79M18HM		MC7918CK
μA79M18UC		MC7918CT
μA79M24AHM		MC7924CK
μA79M24AUC		MC7924CT
μA79M24HM		MC7924CK
μA79M24UC		MC7924CT
μA8T13DC	MC8T13L	
μA8T13PC		



Reliability Enhancement Programs

2

The "Better" Program

Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.

THE "BETTER" program is offered on CMOS, Linear, TTL, TTL/LS, DTL, HTL, and NMOS in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate incoming electrical inspection
- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING – STANDARD PRODUCT PLUS:

100% SCREEN	LEVEL I "S"	LEVEL II "D"	LEVEL III "DS"
TEMP CYCLE, 10 CYCLES -25°C to +150°C	X		X
BURN-IN — MIL-STD-883		X	X
POST BURN-IN ELECTRICAL		X	X
100°C FUNCTIONAL	X		X
DC PARAMETRIC AT 25°C*	X	X	X
TIGHTENED QA SAMPLE	X	X	X

*NMOS does Functional and dc 100% at 100°C

"BETTER" AQL GUARANTEES

TEST	CONDITION	AQL		
		LEVEL I	LEVEL II	LEVEL III
HIGH TEMPERATURE FUNCTIONAL	T_A = 100°C	0.15		0.15
DC PARAMETRIC	T_A = 25°C	0.28	0.28	0.28
DC PARAMETRIC	T_A MIN, TA MAX	0.40	0.40	0.40
DC PARAMETRIC (LINEAR AND NMOS)	T_A MIN, TA MAX	0.65	0.65	0.65
AC PARAMETRIC	T_A = 25°C	0.65	0.65	0.65
DYNAMIC TEST (LINEAR AND NMOS)	T_A = 25°C	0.65	0.65	0.65
EXTERNAL VISUAL AND MECHANICAL	MAJOR	0.11	0.11	0.11
	MINOR	2.50	2.50	2.50
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS	0.40	0.40	0.40
	FINE	1.00	1.00	1.00

HOW TO ORDER

MC14001B — **Part Identification**

CP — **Standard Package Suffix**

S — **BETTER PROCESSING**
LEVEL I = SUFFIX S
LEVEL II = SUFFIX D
LEVEL III = SUFFIX DS

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

The Motorola Standard HIGH REL Programs

Motorola, a pioneer in the manufacture of *high-reliability* integrated circuits*, now offers you a two-way program for Hi Rel products.

1. A growing line of JAN-QUALIFIED integrated circuits.
2. An extensive program to supply JEDEC PROCESSED devices that approaches the Qualified Reliability goals without the delay and high cost of the actual qualification program.

Motorola stocks many circuits which meet JAN-QUALIFIED specifications, and is actively pursuing an expansion of this qualification listing with product in all IC categories — encompassing Bipolar Digital, Linear and MOS technologies.

Motorola JEDEC PROCESSED products complement JAN-QUALIFIED products by making available hi-rel versions of nearly all Motorola full-temperature range circuits, while adding the advantage of hi-rel standardization.

The Motorola JEDEC Program offers you these benefits:

1. Standardization of environmental and electrical test procedures.
2. Less specification writing required.
3. Less time required in negotiating specifications.
4. Fast delivery.
5. Lower costs.

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*Motorola, in early 1971, was the first company to be qualified as a MIL-M-38510 approved facility by the Defense Electronics Supply Center of DOD

MIL-M-38510 JAN-Qualified Product

Screening Levels Available:
Class B & Class C

How to order
MIL-M-38510
JAN-Qualified Product

J	M38510	/XXX	XX	Y	Y	Y
INDICATES A QUALIFIED DEVICE	MILITARY DESIGNATOR	DETAIL SPECIFICATION NUMBER	DEVICE TYPE WITHIN DETAIL SPECIFICATION	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1-1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2-1/16")
R	D-8	20-lead DIP (1/4" x 1-1/16")
S	NONE	NONE
T	NONE	NONE
U	NONE	NONE
V	D-6	18-lead DIP (.300" x 1")
W	D-7	22-lead DIP (.400" x 1.1")
X Y Z	Reserved for use with "special" non-standard case outlines which are specified in the individual detail specifications.	

Features:

1. Manufactured in a government-approved facility.
2. G.S.I. (Government Source Inspection)

Example of MIL-M-38510 JAN-Qualified markings

ORDER: JM38510/00104BCB
MARKING: JM38510/00104BCB

Lead Finish Table

A—Type A or B Per MIL-M-38510 with hot solder dip
B—Type A or B Per MIL-M-38510 with acid tin plate
C—Type A or B Per MIL-M-38510 with gold plate
X—Any of the above, for ordering purposes only.

JEDEC Processed Product

Screening Levels Available:
Class B & Class C

How to order JEDEC Processed Product

XXXX/	Y	Y	Y	JC
MOTOROLA DEVICE TYPE (WITHOUT LETTER PREFIX)	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)	JEDEC DESIGNATOR PER JEDEC PUBLICATION NO 101

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1-1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2-1/16")
R	D-8	20-lead DIP (1/4" x 1-1/16")
S	NONE	NONE
T	NONE	NONE
U	NONE	NONE
V	D-6	18-lead DIP (.300" x 1")
W	D-7	22-lead DIP (400" x 1 1")
X	Dual-in-line packages not listed above	
Y	Flat packages not listed above	
Z	All other configurations not listed above.	

Features:

1. Lower cost than JAN-Qualified.
2. Devices manufactured using design and processing guidelines contained in MIL-M-38510 and MIL-STD-883
3. Product supplied with Motorola standard data sheet electricals

Example of JEDEC Processed Markings

DEVICE: 5400/BCBJC
ORDER: 5400/BCBJC
MARKING: 5400/BCBJC

Lead Finish Table

A—Type A or B Per MIL-M-38510 with hot solder dip
B—Type A or B Per MIL-M-38510 with acid tin plate
C—Type A or B Per MIL-M-38510 with gold plate
X—Any of the above, for ordering purposes only.

Screening Procedures

For MIL-M-38510 Jan-Qualified and JEDEC Processed Product (To MIL-STD-883 Requirements)

In recognition of the fact that the level of screening has a direct impact on the cost of the product, as well as its quality and reliability, two standard levels of screening are provided to coincide with two device classes, or levels of quality assurance.

Flexibility is provided in the choice of test conditions and stress levels to provide screens tailored to a particular product or application. Selection of a level better than that required for the specific product and application will result in unnecessary expense. A level less than that required may result in a risk that reliability requirements will not be met. For general hi-rel applications, the Class B screening levels should be considered.

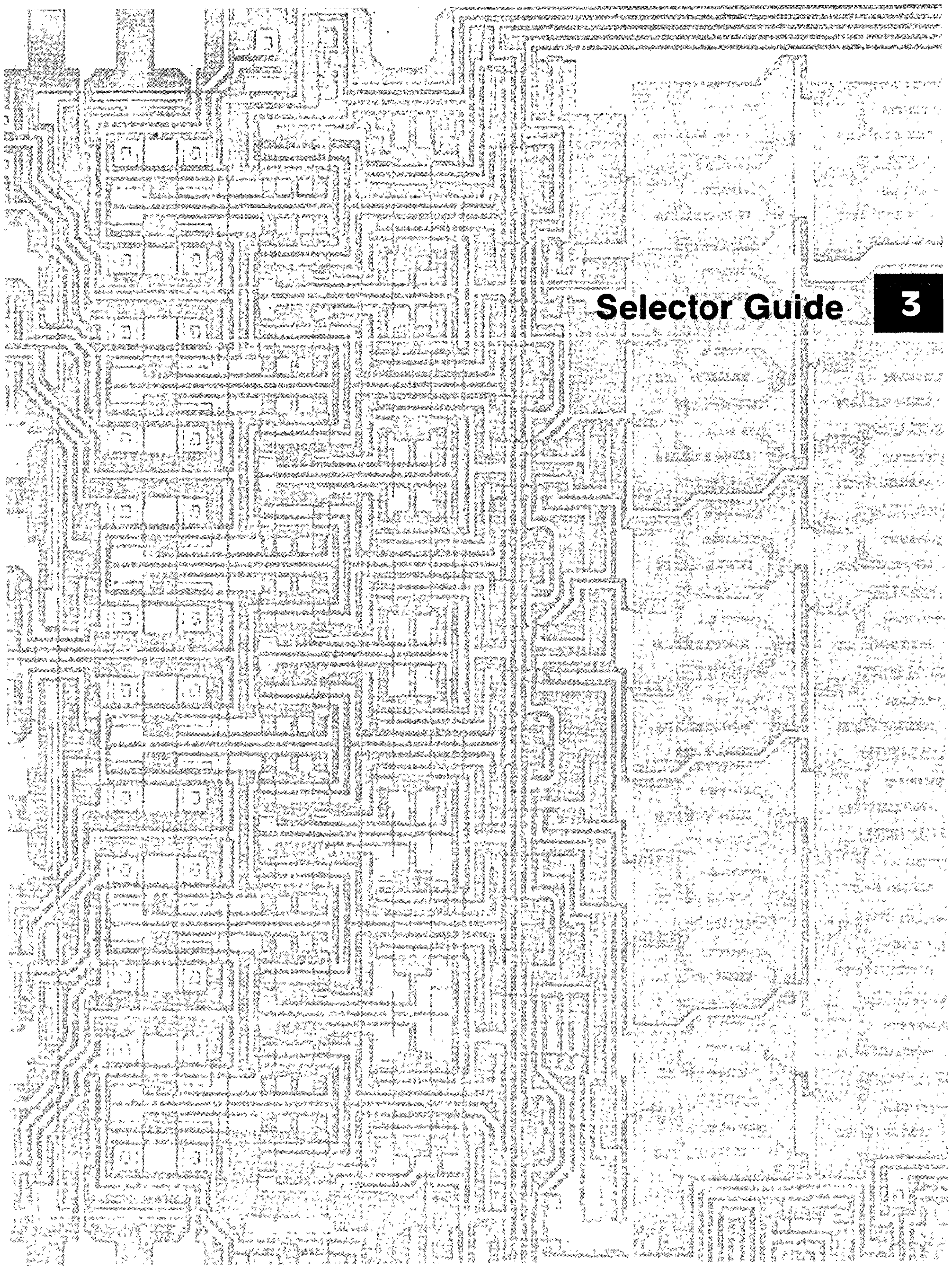
Device Class Table

	CLASS B		CLASS C	
SCREEN	METHOD	RQMT	METHOD	RQMT
Internal Visual (Precap)	2010 Condition B and 38510	100%	2010 Condition B and 38510	100%
Stabilization Bake	1008, 24 hrs test Condition C or Equivalent	100 %	1008, 24 hrs test Condition C or Equivalent	100%
Temperature Cycling	1010 Condition C	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E Y_1 plane	100%	2001 Condition E Y_1 plane	100%
Seal (a) Fine (b) Gross	1014	100%	1014	100%
Interim Electrical Parameters	Per applicable device specification 1			—
Burn-In Test	1015 160 hrs @ 125° C or Equivalent	100%		—
Interim Electrical Parameters	Per applicable device specification 1	100%		—
Final Electrical Tests (a) Static tests	Per applicable device specification 2		Per applicable device specification 2	
(1) 25° C (subgroup 1, table 1, 5005)		100%		100%
(2) Max. & min rated operating temp (subgroups 2 & 3, table 1, 5005)		100%		Sample at Group A
(b) Dynamic tests &/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005)		100%		Sample at Group A
(c) Functional test @ 25°C (subgroup 7, table 1 5005)		100%		100%
Qualification or Quality Conformance Inspection	5005 Class B 3	Sample per 38510	5005 Class C 3	Sample per 38510
External Visual	2009	100%	2009	100%

1 When specified in the applicable device specification 100% of the devices shall be tested

2 MIL-M-38510 QUALIFIED product is tested per applicable 38510 detail specification JEDEC PROCESSED product is tested per the Motorola standard data sheet electrical specification

3 For JEDEC PROCESSED product, Groups A and B per 5005 and JEDEC Publication No 101. Groups C and D are available upon request



Selector Guide

Microprocessor Bus

This family of devices is designed to extend the limited drive capabilities of today's standard 6800 and 8080 type NMOS microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

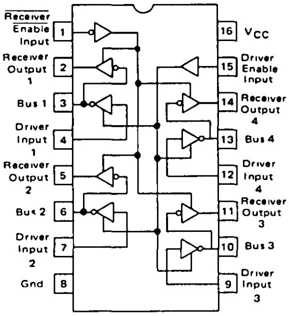
General features include:

- Single +5.0 V Power Supply Requirement
- Three-State Logic Output
- Low Input Loading – 200 μA Max.

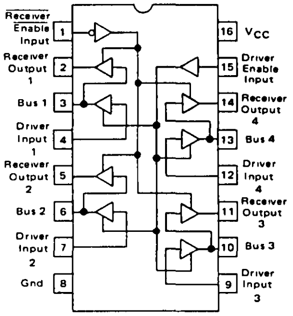
DATA BUS EXTENDERS

Quad, Bidirectional, with 3-State Outputs

MC6880A/MC8T26A# – Inverting



MC6889/MC8T28# – Non-inverting



#These devices may be ordered by either of the paired numbers

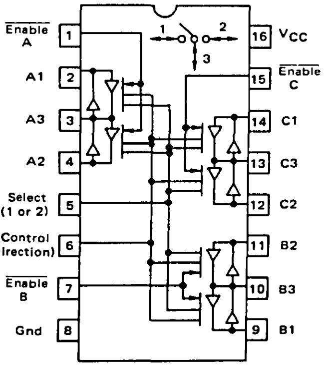
Both types
T_A = 0 to 75°C

Packages
L Suffix – Case 620
P Suffix – Case 648

Device Number	Input Current		I_{OHL} Output Disabled Leakage Current – High Logic State μA Max	t_{PLH}, t_{PHL} Propagation Delay Time – High to Low or Low to High ns Max
	I_{IH} μA Max	I_{IL} μA Max		
MC6880A/MC8T26A	25	-200	100	14
MC6889/MC8T28	25	-200	100	17

BIDIRECTIONAL BUS SWITCH

MC6881/MC3449# – For exchanging TTL level digital information between selected pairs of ports in a 3-port network.



#This device may be ordered by either of the numbers.

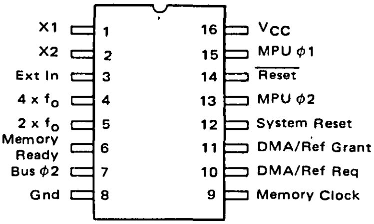
Both types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OL} @ I_{OL} = 8.0 mA Volts Max	I_{OD} @ V_O = 2.7 V μA Max	I_{IL} @ V_{IL} = 0.4 V μA Max	I_{IH} @ V_{IH} = 2.7 V μA Max
0.5	25	-200	40

M6800 CLOCK GENERATOR

MC6875 – Provides the non-overlapping two-phase clock signals for M6800 MPU systems.



V_{OLC} = 0.3 V Max

V_{OHC} = V_{CC} – 0.3 V Min

f_{op} = 2.0 MHz Typ

MC6881/MC3449 TRUTH TABLE

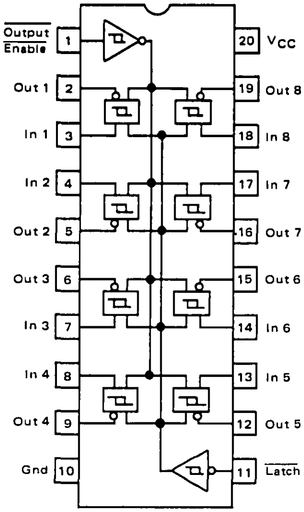
Enable	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

ADDRESS AND CONTROL BUS EXTENDERS

Octal, Buffer/Latch Unidirectional with 3-State Outputs

MC6882A/MC3482A# – Inverting



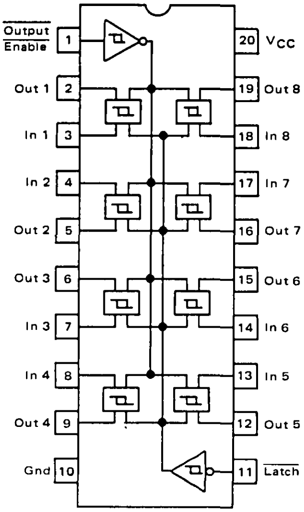
Output Enable	Latch	Input	Output
0	1	0	1
0	1	1	0
0	0	X	Q_0
1	X	X	Z

#These devices may be ordered by either of the paired numbers.

All types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 732
P Suffix – Case 738

MC6882B/MC3482B# – Non-inverting



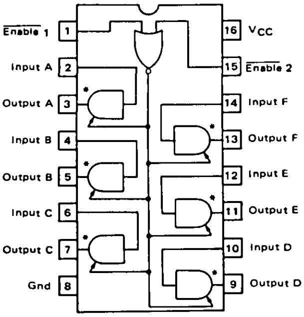
Output Enable	Latch	Input	Output
0	1	0	0
0	1	1	1
0	0	X	Q_0
1	X	X	Z

Device Number	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = −5.2 mA Volts Min	I_{OS} mA Typ	t_{PHL} ns Typ
MC6882A/MC3482A	0.5	2.4	−80	8.0
MC6882B/MC3482B	0.5	2.4	−80	10

Hex, Unidirectional, with 3-State Outputs

MC6885/MC8T95# – Non-inverting
MC6886/MC8T96# – Inverting

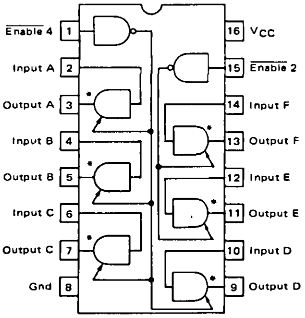
Two-input Enable controls all six buffers.



•Add inverter for MC6886/MC8T96.

MC6887/MC8T97# – Non-inverting
MC6888/MC8T98# – Inverting

Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



•Add inverter for MC6888/MC8T98.

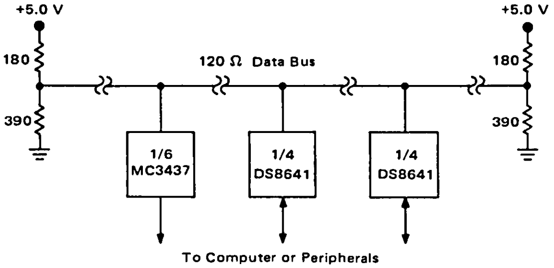
All four types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = −5.2 mA Volts Min	I_{OS} mA Typ	t_{PLH} ns Typ	$t_{P(Enable)}$ ns Typ
0.5	2.4	−80	6.0	11

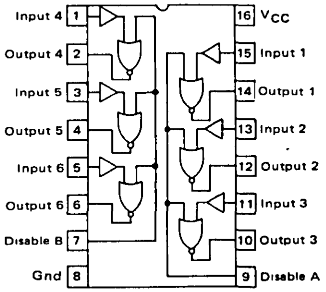
Minicomputer Bus

Transceivers and receivers for bus organized minicomputers employing 120-ohm terminated lines.



HEX RECEIVERS

MC3437 — Hysteresis-equipped for improved noise immunity. DS8837 equivalent.



$I_{I(R)}$ @ $V_{I(R)} = 4.0$ V μA Max	Hysteresis Volts Min	$t_{PLH(R)}$ @ $C_L = 15$ pF ns Max
50	0.5	30

All three devices:
$T_A = 0$ to 70^oC

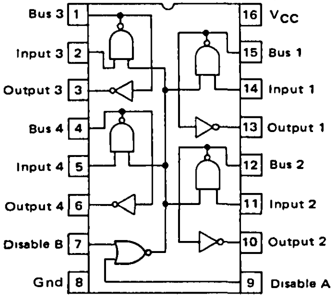
Packages:

MC3437
MC3438 DS8641
L Suffix — Case 620 — J Suffix
P Suffix — Case 648 — N Suffix

QUAD TRANSCEIVERS

DS8641-MC3438

Open collector driver outputs allow wire-OR connection. MC3438 has hysteresis-equipped receiver for improved noise immunity (not available with DS8641). MC3438 is equivalent to the DS8838.



Receiver Hysteresis Volts Min	$V_{L(BUS)}$ @ $I_{BUS} =$ 50 mA Volts Max	I_{BUS} @ $V_{IH(BUS)} =$ 4.0 V μA Max	$t_{PLH(D)}$ @ $C_L =$ 15 pF ns Max	$t_{PLH(R)}$ @ $C_L =$ 15 pF ns Max
0.25*	0.7	100	25	30

*MC3438 only.

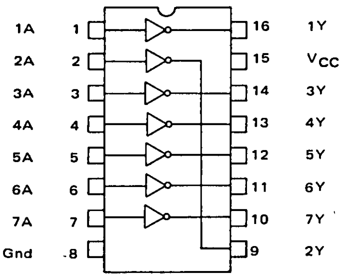
Computer Bus

NEW IBM 360/370 I/O INTERFACE

Line Receivers and Drivers designed to operate compatibly. The MC75125/MC75127 Seven-Channel Receivers, MC75128/MC75129 Eight-Channel Receivers, and the MC3481/MC3485 Drivers meet the new IBM System 360/370 I/O standard requirements.

SEVEN-CHANNEL LINE RECEIVERS

MC75125

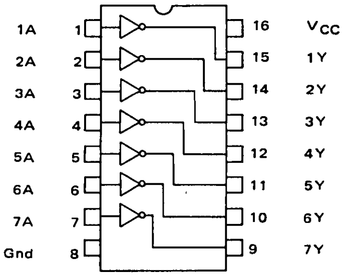


Logic: $Y = \overline{A}$

All types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

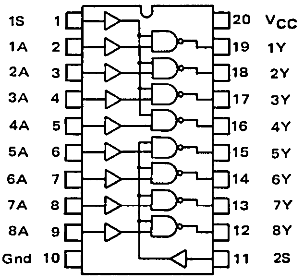
MC75127 – Standard V_{CC} and Ground Pinouts.



Logic. $Y = \overline{A}$

EIGHT-CHANNEL LINE RECEIVERS

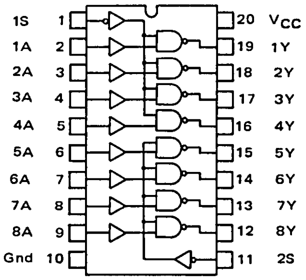
MC75128 – Active-High Strobe



Packages:
L Suffix – Case 732
P Suffix – Case 738

positive logic: Y = AS

MC75129 – Active-Low Strobe



Device Number	Input Resistance kΩ Min/Max	$I_{IH(R)}$ @ V_{IH} = 3.11 V mA Max	t_{PLH} @ C_L = 50 pF ns Max
MC75125/75127	7.4/20	0.42	25
MC75128/75129	7.4/20	0.42	25

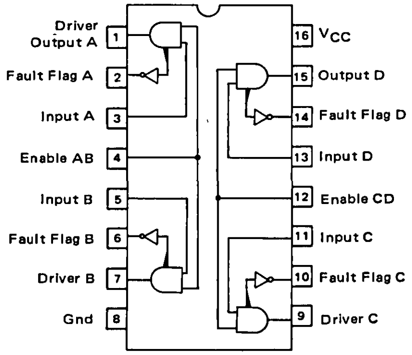
New IBM 360/370 I/O Interface (continued)

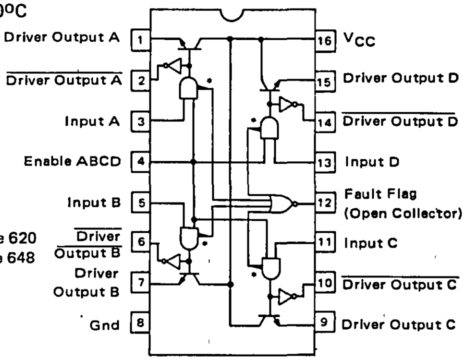
QUAD LINE DRIVERS
(To be introduced)

MC3481 – Open emitter driver with individual fault flags.

MC3485 – Open emitter driver with combined open collector fault flag and inverted outputs.

Both types:
$T_A = 0$ to 70°C





Packages:
L Suffix – Case 620
P Suffix – Case 648

Device Number	V_{OH} @ $I_{OH} = -59.3$ mA Volts Max	I_{OS}* @ $V_O = 0$ mA Max	t_{PLH} @ $C_L = 100$ pF ns Typ
MC3481/3485	3.11	0.0	25

*Fault Protection

GENERAL-PURPOSE I/O INTERFACE

Line drivers and receivers designed to operate compatibly. The MC8T13/MC8T14 combination is specified for general TTL system applications. The MC8T23/MC8T24 combination is oriented toward older IBM 360/370 system requirements.

DUAL LINE DRIVERS

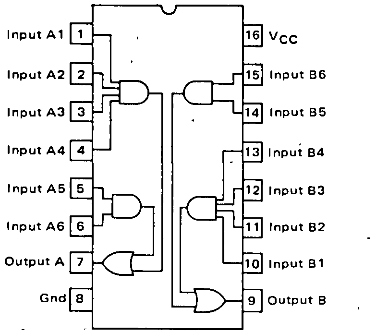
MC8T13 – Open emitter driver; specified for general TTL systems.

MC8T23 – Open emitter driver; specified to meet older IBM system requirements.

TRIPLE LINE RECEIVERS

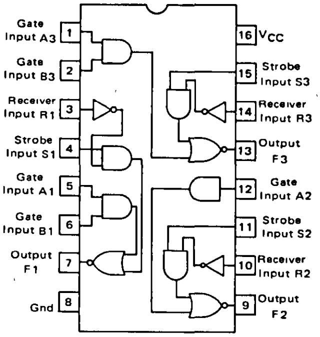
MC8T14 – Hysteresis-equipped receiver; specified for general TTL systems.

MC8T24 – Hysteresis-equipped receiver; specified to meet older IBM system requirements.



All four devices:
$T_A = 0$ to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648



Device Number	V_{OH} @ $I_{OH} = -75$ mA @ $I_{OH} = -59.3$ mA* Volts Max	I_{OS} @ $V_O = 0$ mA Max	t_{PLH} @ $C_L = 15$ pF ns Max
MC8T13	2 4	-30	20
MC8T23	3.11*	-30	20

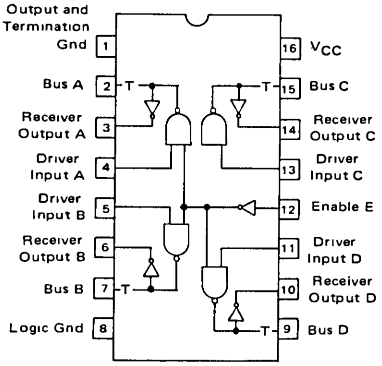
Device Number	$V_{H(R)}$ Volts Min	$I_{IH(R)}$ @ $V_{IH(R)} = 3.8$ V @ $V_{IH(R)} = 3.11$ V* mA Max	$t_{PLH(R)}$ @ $C_L = 15$ pF ns Max
MC8T14	0.3	0.17	30
MC8T24	0.2	0 17*	30

Instrumentation Bus

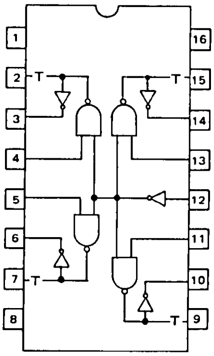
QUAD INTERFACE TRANSCEIVERS

These devices are designed to meet the GPIB bus specification of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

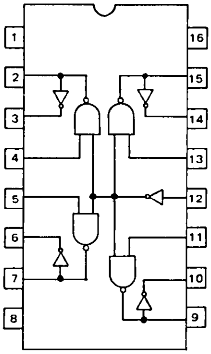
MC3440AP — Three drivers with common Enable input; one driver without Enable.



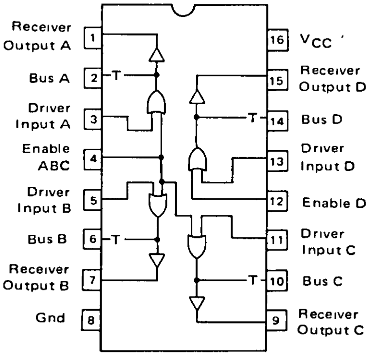
MC3441AP — Four drivers with common Enable input.



MC3443P — Four drivers with common Enable input; no termination resistors.



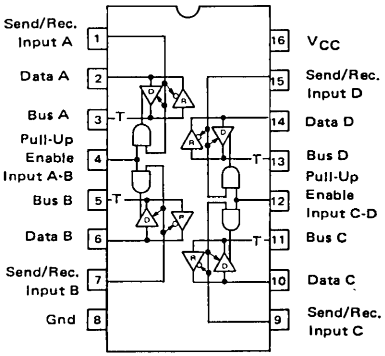
MC3446AP — For low-power instruments, including MOS.

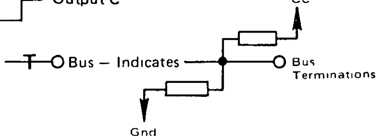


Packages.
L Suffix — Case 620
P Suffix — Case 648

All types:
$T_A = 0$ to 70°C

MC3448A — For common Send-Receive bus; bidirectional.





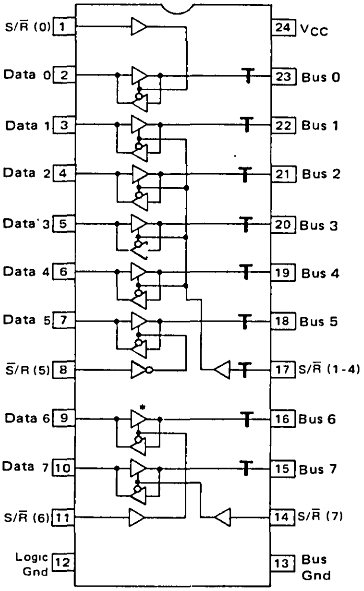
Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3440AP	400	0.5	30
MC3441AP	400	0 5	30
MC3443P	400	0.4	25(D) 22 (R)
MC3446AP	400	0.5	50 (D) 40 (R)
MC3448A	400	0.5	17 (D) 23 (R)

Instrumentation Bus (continued)

OCTAL LOW-POWER INTERFACE TRANSCEIVER

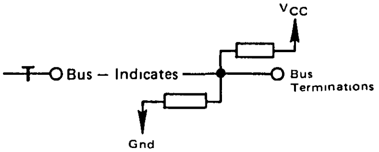
These devices are designed to meet the GPIB bus specifications of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

MC3447 – Open collector, 3-State outputs with terminations.



All types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 623
P3 Suffix – Case 724
(Narrow)



Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3447	400	0.5	30 (D) 22 (R)*

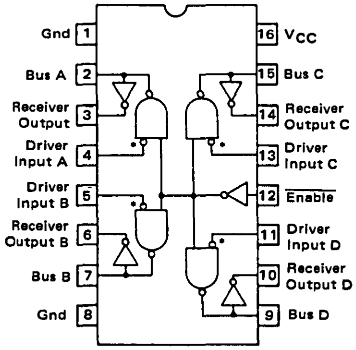
*Fast Channel.

HIGH-CURRENT PARTY-LINE BUS TRANSCEIVERS

Devices for industrial control and data communication.

MC26S10 – Inverting
MC26S11 – Non-inverting

Quad transceivers with open-collector drivers and PNP-buffered inputs for MOS compatibility.



*Inverter on MC26S11 only.

Packages:
L Suffix – Case 620
P Suffix – Case 648

Test	Condition	Limits
V_{OL} (D)	I_{OL} = 100 mA	0.8 Volts Max
I_O (D)	V_{OH} = 4.5 V	100 µA Max
I_{O1}(D)	V_{CC} = 0 V, V_{OH} = 4.5 V	100 µA Max
I_{IH} (D)	V_{IH} = 2.7 V	30 µA Max
I_{IL} (D)	V_{IL} = 0.4 V	-0.54 mA Max
t_P (D)	MC26S10 MC26S11	15 ns Max 19 ns Max
t_P (R)	Both Types	15 ns Max

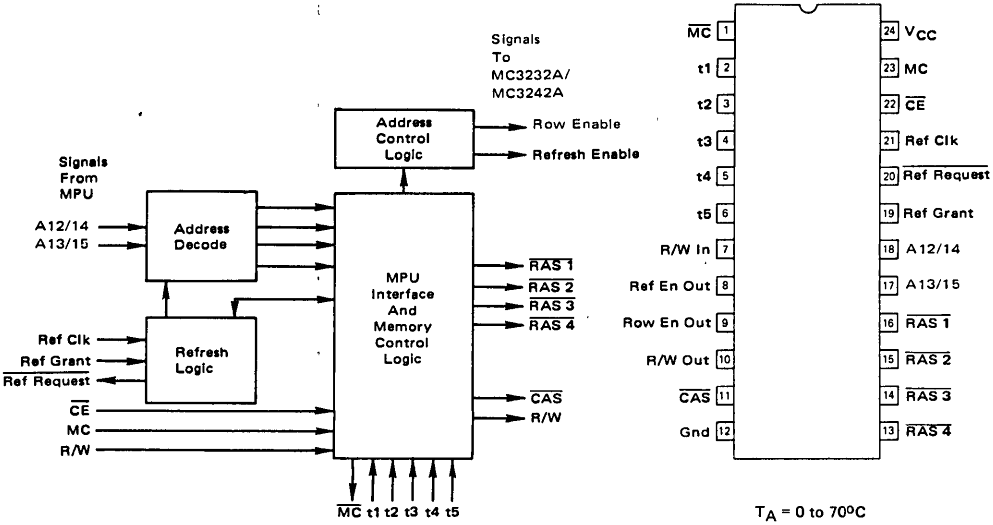
NMOS Memories to TTL Systems

MULTIPLEXED 16-PIN RAM CONTROL
(For 4K, 16K, and 64K Dynamic Memories)

MC3480 – Memory Controller. Used with all three levels of RAM.

The memory controller chip is designed to greatly simplify the interface logic required to control popular 16-pin 4K, 16K, or 64K dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper $\overline{RAS}$ and timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

With Schottky TTL technology for high performance, and high input impedance for minimum loading of the MPU bus, the MC3480 reduces package count, and reduces system access/cycle times by 30%. The chip enable allows expansion to larger-word capacity.



$T_A = 0$ to $70^{\circ}C$

Packages:
L Suffix – Case 623
P Suffix – Case 649

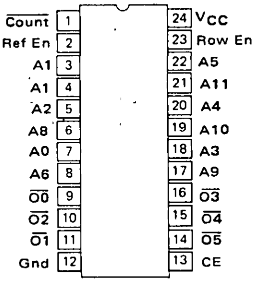
Designed to interface directly with MC3232A or MC3242A address/multiplexers/refresh counters.

NMOS Memories to TTL Systems (continued)
Multiplexed 16-Pin RAM Control (continued)
(For 4K, 16K, and 64K Dynamic Memories)

MC3232A – 6-Bit (4K RAM) Address Multiplexer/Refresh Counter
MC3242A – 7-Bit (16K RAM) Address Multiplexer/Refresh Counter
MC3482A/B – 8-Bit Address Multiplexer (See Microprocessor Bus Section)

MC3232A – Designed for multiplexing 12 address lines into 6 for the 16-pin multiplexed 4K RAMs, while also containing a 6-bit refresh counter.

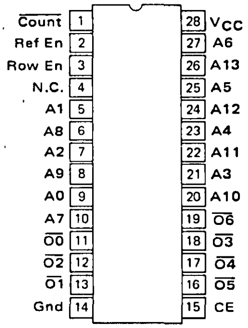
MC3242A – Designed for multiplexing 14 address lines into 7 for the 16-pin multiplexed 16K RAMs, while also containing a 7-bit refresh counter.

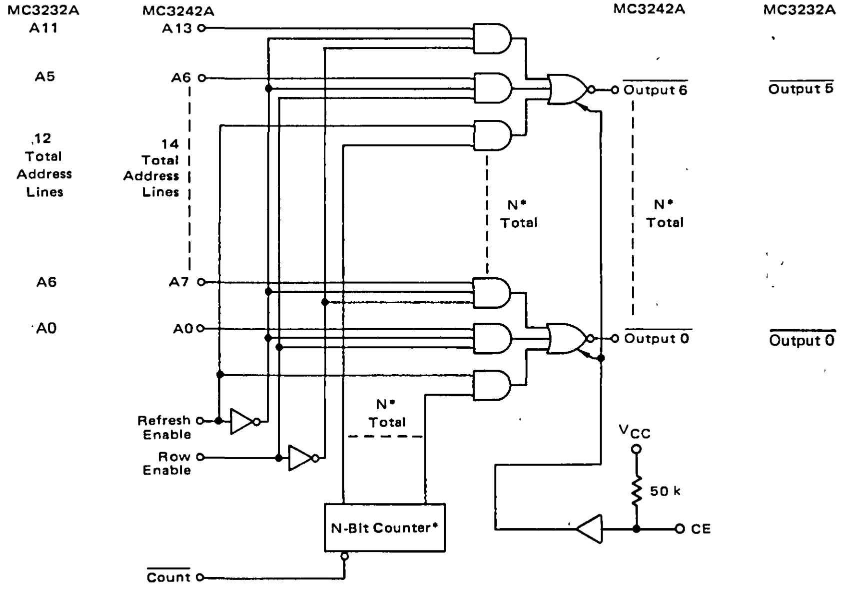


Both types:
T_A = 0 to 75°C

Packages:
MC3232A – L Suffix – Case 623
P Suffix – Case 649

MC3242A – L Suffix – Case 733
P Suffix – Case 710





*N = 6-Bit for MC3232A
= 7-Bit for MC3242A

NMOS Memories to TTL Systems (continued)

BUS EXTENSION
(See Microprocessor Bus)

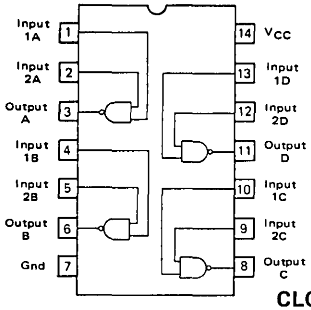
Data Bus (Bidirectional) Extenders
- MC6880A/MC8T26A – Inverting
- MC6889/MC8T28A – Non-inverting

Address Bus (Unidirectional) Extenders
- MC6885/MC8T95 – Hex Non-inverting
- MC6886/MC8T96 – Hex Inverting
- MC6887/MC8T97 – Hex Non-inverting
- MC6888/MC8T98 – Hex Inverting
- MC6882A/MC3482A – Octal Inverting
- MC6882B/MC3482B – Octal Non-inverting

Bus Switches
- MC3449 – Triple Bidirectional

DATA AND ADDRESS LINE DRIVERS
(Low Level)

MC3459 – Quad Address Line Driver



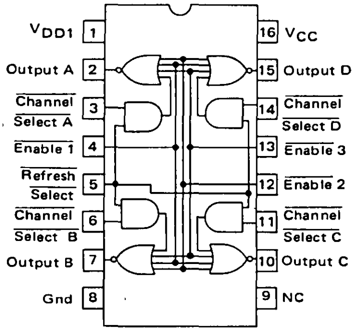
T_A = 0 to 70°C

Packages:
- L Suffix – Case 632
- P Suffix – Case 646

Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	Propagation Delay ns Max	@ C_L pF	Features
MC3459	2.4	–2.0	0.7	80	26	360	High fan-out capability

CLOCK AND CHIP ENABLE LINE DRIVERS
(High Level)

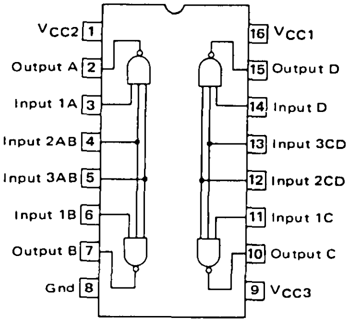
MC3245 – Quad Clock Drivers with Refresh Select Logic



T_A = 0 to 70°C

Packages:
- L Suffix – Case 620
- P Suffix – Case 648

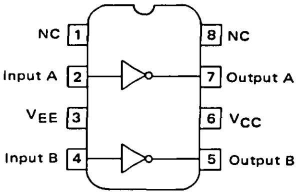
MC75365 – Quad Clock Driver or High-Current NAND Gate



T_A = 0 to 70°C

Packages:
- L Suffix – Case 620
- P Suffix – Case 648

MMH0026
MMH0026C – Dual Clock Driver



(Pin Connections for U or P1 Package)

T_A:
- MMH0026 – -55 to 125°C
- MMH0026C – 0 to 70°C

Packages
- G Suffix – Case 601
- L Suffix – Case 632
- U Suffix – Case 693
- P1 Suffix – Case 626 (For MMH0026C only)

Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	t_{DHL} ns Max	@ C_L pF	Feature
MC3245	V_{DD} - 0.5	-1.0	0.45	5.0	32	250	Does not require second high voltage supply. Low input loading.
MC75365	V_{CC2} - 0.3	-0.1	0 3	10	18	200	Derives V_{CC1} power from TTL 5-V supply, and V_{CC2} and V_{CC3} from V_{SS} and V_{BB} supplies from NMOS memories.
MMH0026 MMH0026C	V_C - 1.0	0.4 V*	V_{EE} + 1.0	2.4 V*	12	1000	For very high capacitance loads.

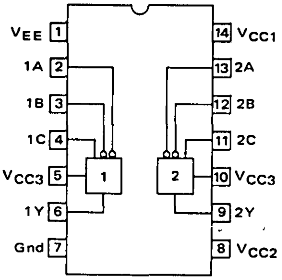
*@ $V_I - V_{EE}$

NMOS Memories to MECL Systems

DRIVER/TRANSLATORS

MECL-to-MOS driver/translators convert standard MECL 10,000 input signals to suitable levels for NMOS memory systems. The MC75368 may also be used as positive logic NOR or non-inverting gates.

MC75368 – Dual Clock Line Drivers suitable for driving address, control, and timing inputs.



Maximum Supply Voltage:
MC75368 = 18 V

T_A = 0 to 70°C

Packages:
L Suffix – Case 632
P Suffix – Case 646

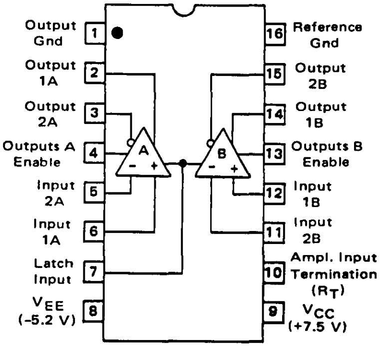
Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	t_{DHL} ns Max	@ C_L pF
MC75368	V_{CC2} - 0.3	0.1	0.3	10	26	300

SENSE AMPLIFIER

MC3461L – Dual Sense Amplifier with MECL 10,000-compatible control inputs and complementary, open-emitter outputs. Designed for 7001 and 2105 type NMOS 1K RAMs.

I_{TH} µA Max	t_{PD} (Amplifier) ns Max	t_{PD} (Enable) ns Max
±200	10	6.0

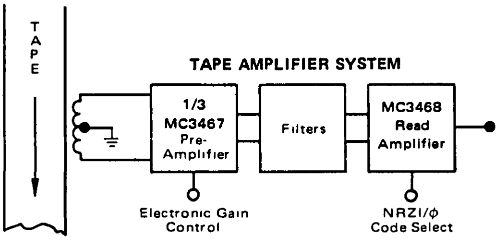
T_A = 0 to 75°C
Package:
Case 620



Magnetic Memories to TTL Systems

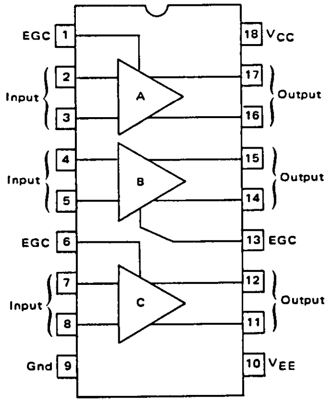
SENSE AMPLIFIERS

. . . for Magnetic Tape Memories



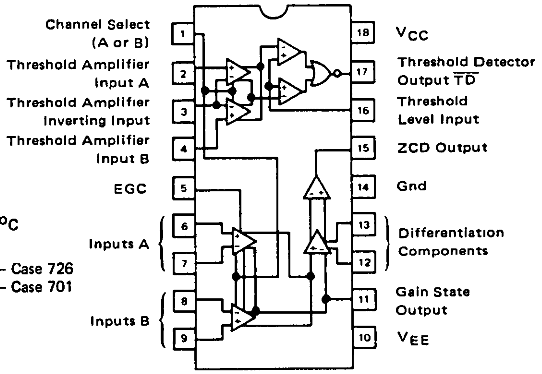
A two-component preamplifier/amplifier combination that provides the interface between magnetic tape heads and digital logic. Suitable for both open reel and cartridge tape systems. Triple preamp has individually adjustable gain controls. LSI Read Amplifier performs peak detection and threshold detection functions, as required for NRZI/phase encoded recording formats.

MC3467 – Triple Preamplifier



Both types:
T_A = 0 to 70°C
Packages:
L Suffix – Case 726
P Suffix – Case 701

MC3468 – Read Amplifier



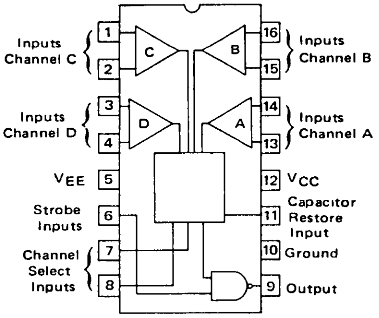
. . . for Plated Wire and Thin-Film Memories

and other low-level sensing applications.

MC1544 – T_A = -55 to 125°C
MC1444 – T_A = 0 to 70°C

Features 4-channel input with decoded channel selection and strobed output capability.

Packages:
MC1544/MC1444
L Suffix – Case 620

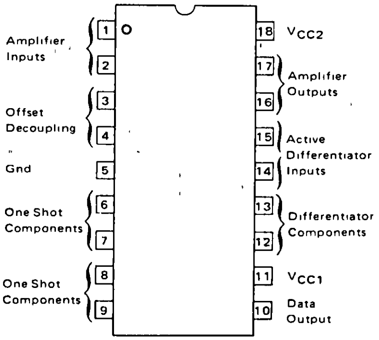


Device Number	V_{TH} mV	V_{OH} @ I_{OH} = -400 μA Volts Min	V_{OL} @ I_{OL} = 10 mA Volts Max	t_{PD} ns Max
MC1544	0.5 to 1.5	2.4	0.5	25
MC1444	0.3 to 2.3	2.4	0.5	25

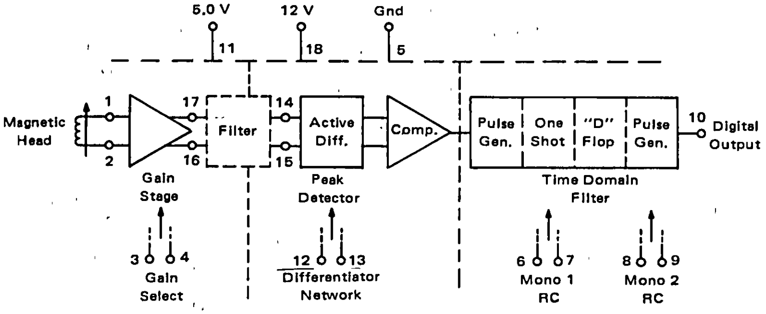
Magnetic Memories to TTL Systems (continued)

FLOPPY DISK READ AMPLIFIER SYSTEM

MC3470 — Designed as a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. It combines all the active circuitry to perform the floppy disk READ amplifier function in one circuit, and is guaranteed to have a maximum peak shift of 5.0%, adjustable to zero.



T_A = 0 to 70°C
Package:
P Suffix — Case 701

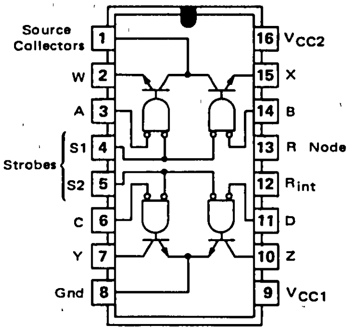


CORE DRIVER

MC55325 – T_A = -55 to 125°C
MC75325 – T_A = 0 to 70°C

Contains two source switches and two sink switches. Source and sink selection is determined by one of two logic inputs, and turn-on is determined by the appropriate strobe.

Packages:
L Suffix — Case 620
P Suffix — Case 648 (MC75325 only)



Device Number	V_{sat} @ I_{sink} or I_{source} = 600 mA Volts Max	I_{off} @ V_{CC2} = 24 V µA Max	t_{PLH} (Source) ns Max	t_{PLH} (Sink) ns Max
MC55325	0.70	150	50	45
MC75325	0.75	200	50	45

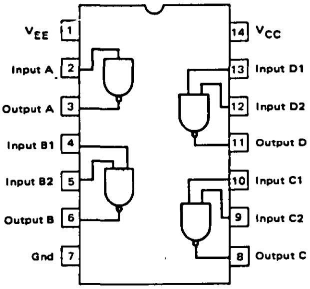
LINE DRIVERS AND RECEIVERS
for Modem/Terminal Applications

Voltage Mode

RS-232C SPECIFICATION

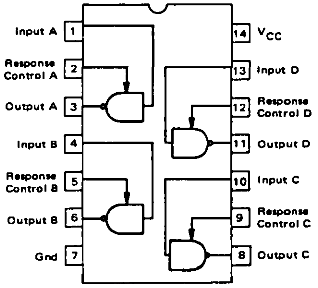
DRIVER

MC1488 – Quad; output current limiting.



RECEIVERS

MC1489 – Quad; 0.25 V input hysteresis.
MC1489A – Quad; 1.1 V input hysteresis.



All devices:
T_A = 0 to 70°C
Package:
L Suffix – Case 632

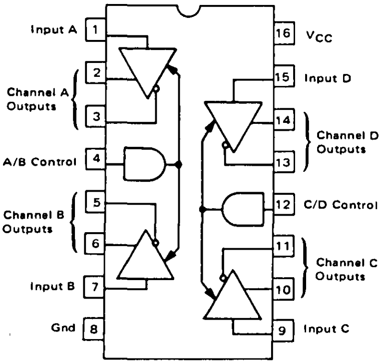
V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	-6.0	±6.0 to 12	175

Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

RS-422/423 SPECIFICATION

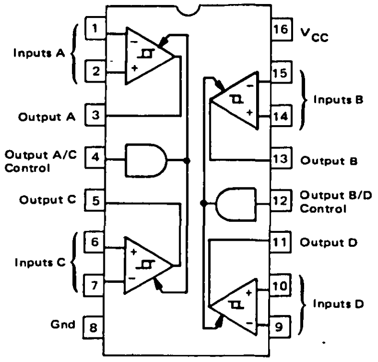
DRIVER

MC3487 – Quad; three-state outputs.



RECEIVER

MC3486 – Quad; three-state outputs and input hysteresis.



Both devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OH} @ I_{OH} = 50 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OD}(Differential) @ R_L = 100 Ω Volts Min	t_{PLH}/t_{PHL} ns Typ
2.0	0.5	2.0	15

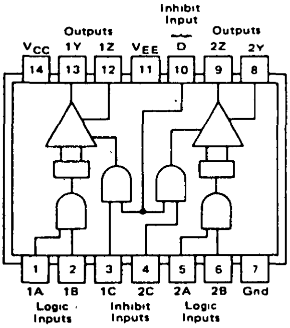
$V_{TH(D)}$ @ V_{ICM} = ±7.0 V Volts Max	I_{ID} @ V_{ID} = ±10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
±0.2	±3.25	20/25	25

Line Drivers and Receivers for Modem/Terminal Applications (continued)

Differential Current Mode

DRIVERS

MC75S110 – Dual; industry standard.

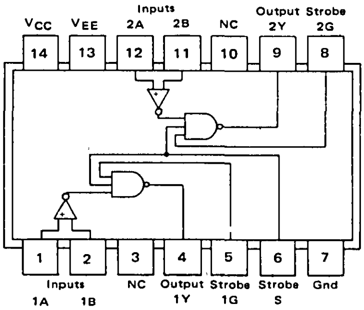


T_A = 0 to 70°C
(MC75xxx)
-55 to 125°C
(MC55xxx)

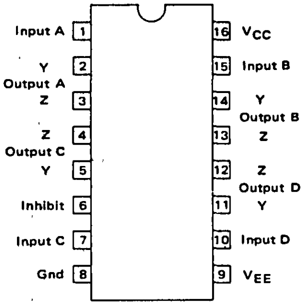
Packages:
L Suffix – Case 632
P Suffix – Case 646
(MC75xxx only)

RECEIVERS

MC75107/MC55107 – Dual; active pullup output.
MC75108/MC55108 – Dual; open collector output.



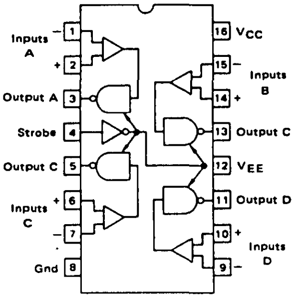
MC3453 – Quad; common inhibit input; current sink approximately 12 mA.



All three devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

MC3450 – Quad; active pullup outputs; common three-state enable.

MC3452 – Quad; open collector outputs.



BOTH DRIVERS

I_O (on) mA Min	I_O (off) μA Max	t_{PHL} ns Max
6.5	100	15

ALL RECEIVERS

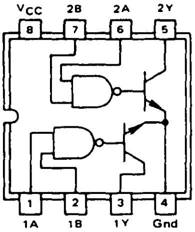
Input V_{TH} mV Max	I_{IH} @ V_{ID} = 0.5 V μA Max	I_{IL} @ V_{ID} = -2.0 V μA Max	t_{PLH} ns Max
±25	75	-10	25

Dual Drivers

. . . for relays, lamps, and other peripherals requiring more power than generally available from logic gates.

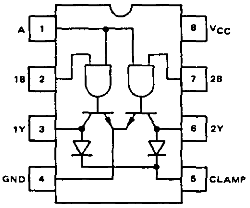
Representative Diagrams

MC754xx Series



(MC75451/MC75461)

MC147x Series



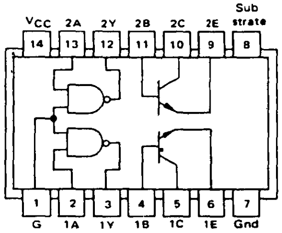
(MC1472)

Logic gates vary to provide output shown

Logic Output (Including Transistor Inversion)	BV_{CER}			
	30 V	30 V	35 V	70 V Hi-Z Input
AND NAND OR NOR	MC75451 MC75452 MC75453 MC75454	SN75451B* SN75452B* SN75453B* SN75454B*	MC75461 MC75462 MC75463 MC75464	MC1472

*Same as equivalent MC types, but with guaranteed switching limits.

MC75450 – Similar to MC75451, but with uncommitted output transistors.



All Devices
$T_A = 0$ to 70°C

Packaging:
MC75450
L Suffix – Case 632
P Suffix – Case 646
MC75451–54/MC75461–64
P Suffix – Case 626
U Suffix – Case 693
MC1472
P1 Suffix – Case 626
U Suffix – Case 693

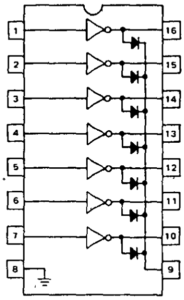
Driver Arrays

. . . Seven Darlington transistors with output clamp diodes.

Device Number	Application	Input Element
MC1411	General Purpose	Basic
MC1412	14–25 V PMOS	Zener and Series 10 5 kΩ resistor
MC1413	5 V CMOS or TTL	Series 2 7 kΩ resistor
MC1416	8–18 V MOS	Series 10.5 kΩ resistor

All Types:
$V_{Max} = 50$ V
$I_{Max} = 500$ mA
$T_A = 0$ to 85°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

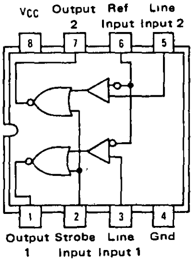


Dual Receiver

MC75140P1 – Dual single-ended receiver with common strobe and reference inputs for maximizing noise immunity. Useful for bus-organized (party line) TTL systems.

V_{TH}	V_{Ref}	$t_{PLH(L)}$
±100 V	1.5 to 3.5 V	35 ns

$T_A = 0$ to 70°C
Package – Case 626

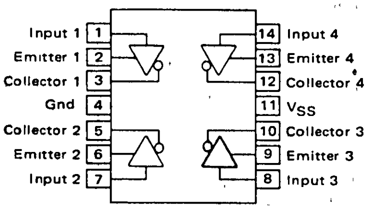


NUMERIC DISPLAY INTERFACE

. . . for mating multiplexed LED or gas discharge numeric displays to MOS or TTL logic systems.

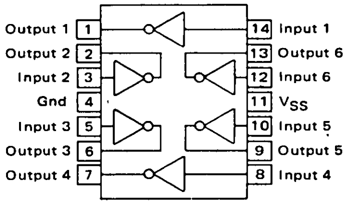
LED Drivers for Common-Cathode Displays

MC75491 – Quad segment driver



Both Devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 632
P Suffix – Case 646

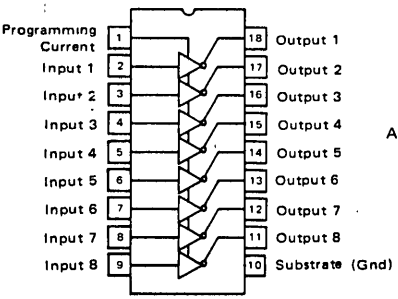
MC75492 – Hex digit driver



Device Number	I_I @ V_I = 10 V mA Max	V_{OL} Volts Max	@ I_{OL} mA	V_{SS} Volts Max
MC75491	3.3	1.2	250	10
MC75492	3.3	1.2	50	10

Gas Discharge Drivers

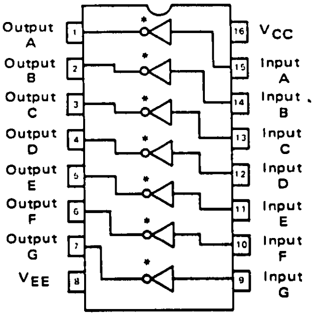
MC3491
MC3492 – Eight segment cathode drivers with programmable current.



All Devices:
T_A = 0 to 70°C

Package: P Suffix – Case 701

MC3490 – High Level
MC3494 – Low Level
Seven digit anode drivers



*Inverter on MC3494 only.
Package: P Suffix – Case 648

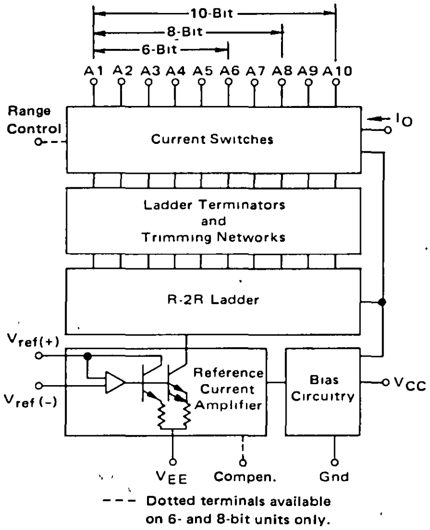
Device Number	Output ON Current mA Max	Breakdown Voltage Volts Min	Current Deviation (All 8 Outputs) % Max	Output Voltage Compliance Range Volts
MC3491	1.85	80	10	5.0 to 50
MC3492	5.25	80	10	5.0 to 50

Device Number	Breakdown Voltage Volts Min	Input Voltage (OFF-State) Volts	Input Voltage (ON-State) Volts	Input Current µA Max
MC3490	48	-5.0 Min	-2.0 Max	450
MC3494	48	-2.0 Max	-5.0 Min	-350

PRECISION CIRCUITS — DATA CONVERSION

Low-cost building blocks for construction of D-A/A-D systems. Involves use of advanced technologies such as ion implantation, laser trimming and CMOS processing where necessary to achieve the required functional capability, operating accuracy and production repeatability.

D-A Converters — General Purpose



Multiplying D-A converters designed to supply an output current that is a linear product of an analog input reference voltage and a digital input word. Devices for 6-, 8- and 10-bit digital word inputs are available.

Device Number	Error % Max	P_D @ V_{EE} = -5 V mW Max	$t_{Settling}$ ns Typ	I_O @ V_{Ref} = 2 V mA	Suffix	Case
6-Bit						
MC1506*	±0.78	120	150	1.9 to 2.1	L	632
MC1406						
8 Bit						
MC1508L8*	±0.19	170	300	1.9 to 2.1	L	620
MC1408L8					L, P	620, 648
MC1408L7	±0.39					
MC1408L6	±0.78					
MC3408	±0.5				L	620
10-Bit						
MC3510*	±0.05	220	250	3.8 to 4.2	L	690
MC3410					L, P	690, 648
MC3410C	±0.1					

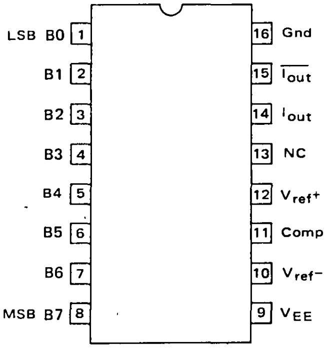
*T_A = -55 to 125°C,
Devices without asterisk. T_A = 0 to 70°C.

D-A Converters — High Speed

MC10318 – A high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, display processing, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability. 8-bit accurate (± 1/2 LSB) and monotonic over the full temperature range, the outputs typically settle in less than 15 ns.

T_A = 0 to 70°C

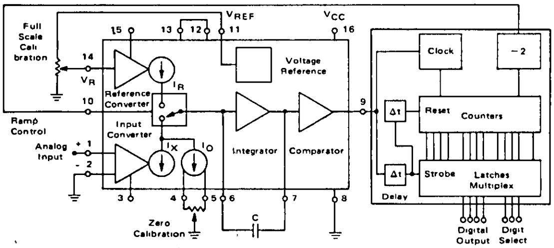
Packages:
L Suffix – Case 620/690



Device Number	Error % Max	P_D @ V_{EE} = -5.2 V mW Max	$t_{Settling}$ ns Typ	I_O & $\overline{I_O}$ @ V_{Ref} = 10.56 V mA Typ
MC10318L	±0.19	675	15	51
MC10318L9	±0.10	675	15	51

A-D Subsystems

2-Chip A-D Converter System Functional Diagram



MC1505/1405 — A-D Converter

MC14435 — Digital Logic
(See CMOS Data Book for data.)

These devices are relatively complex subsystems. The bipolar, dual-ramp A-D converter has up to 4-1/2-digit conversion capability. The CMOS logic subsystem specifically adapts the A-D converter to a 3-1/2-digit DVM function.

MC1505L — T_A = -55 to 125°C — Case 620
MC1405L — T_A = 0 to 70°C — Case 620

Linearity Error % Max	Voltage Reference Volts	Temperature Coefficient of Reference %/°C	I_{CC} @ V_{CC} = 5.0 V mA Max
±0.05	1.15 to 1.35	0.005	12

MC14435EFL/EVL* — T_A = -55 to 125°C — Case 620
MC14435FL/VL* — T_A = -40 to 85°C — Case 620
MC14435FP/VP* — T_A = -40 to 85°C — Case 648

$P_{C(quiescent)}$ @ V_{DD} = 5.0 V mW Max	I_{OL} @ V_{DD} = 5.0 V (Digit Selects) mA Min	I_{OL} @ V_{DD} = 5.0 V (BCD Outputs) mA Min	I_{OL} @ V_{DD} = 5.0 V (All Outputs) mA Min
1.75	1.6	1.6	-0.2

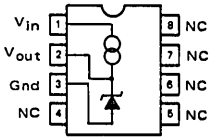
*MC14435EFL/FL/FP: V_{DD} = 3.0 to 18 Vdc
MC14435EVL/VL/VP: V_{DD} = 3.0 to 6.0 Vdc

VOLTAGE REFERENCES

Precision Low-Voltage References

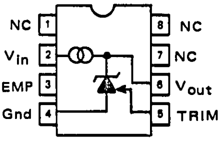
A family of precision low-voltage bandgap voltage reference, these devices are designed for applications requiring low temperature drift.

MC1403/MC1503



Packages:
U Suffix — Case 693

MC1404/MC1504



Low Temperature Drift, Low Voltage Reference

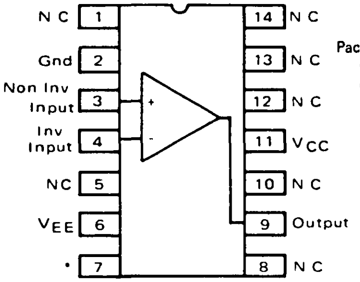
V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device Number	Reg_{line} 4.5< V_I ≤15 V/ 15 V≤V_I≤40 V mV Max	Reg_{line} V_{in} = V_{out}+ 2.5 V to 40 V mV Max	Reg_{load} 0.0 mA I_O<10 mA mV Max	T_A °C
2.5 ± 25 mv	10	40	MC1403	3.0/4.5	N/A	10	0 to +70
		25	MC1403A				
		55	MC1503				−55 to +125
		25	MC1503A				
5.0 ± 50 mV	10	40	MC1404U5	N/A	6.0	10	0 to +70
		25	MC1404AU5				
		55	MC1504U5				−55 to +125
		25	MC1504AU5				
6.25 ± 60 mV	10	40	MC1404U6	N/A	6.0	10	0 to +70
		25	MC1404AU6				
		55	MC1504U6				−55 to +125
		25	MC1504AU6				
10 ± 100 mV	10	40	MC1404U10	N/A	6.0	10	0 to +70
		25	MC1404AU10				
		55	MC1504U10				−55 to +125
		25	MC1504AU10				

General Purpose Comparators

. . . for detecting the polarity relationship between two analog levels and giving a corresponding TTL output.

MC1710 – T_A = -55 to 125°C
MC1710C – T_A = 0 to 70°C
Single comparators

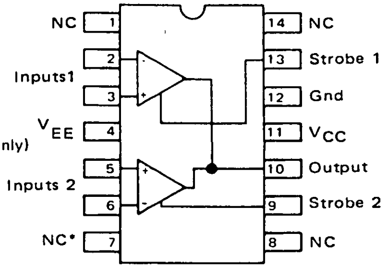
MC1711 – T_A = -55 to 125°C
MC1711C – T_A = 0 to 70°C
Dual comparators with strobes and wire-ORed outputs



•Connected to pin 6 via the substrate on some plastic units.

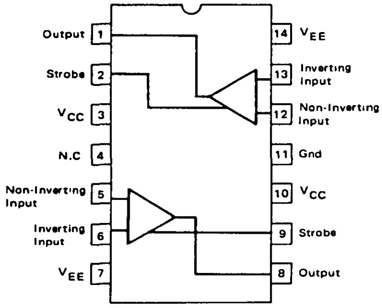
Packages:
G Suffix – Case 601 (MC1710)
G Suffix – Case 603 (MC1711)
L Suffix – Case 632
P Suffix – Case 646 (for MC1710C, MC1711C only)

(Pin Connections for L or P Package)



•Connected to pin 4 via the substrate on some plastic units.

MC1514 – T_A = -55 to 125°C
MC1414 – T_A = 0 to 70°C
Dual comparators with strobes.

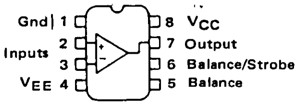


Packages:
L Suffix – Case 632
P Suffix – Case 646 (MC1414 only)

Device Number	V_{IO} mV Max	I_{IB} µA Max	A_{VOL} V/V Min
MC1710C	5.0	25	1000
MC1710	2.0	20	1250
MC1711C	5.0	100	700
MC1711	3.5	75	700
MC1514	2.0	20	1250
MC1414	5.0	25	1000

Precision Comparators

. . . featuring low input loading, high voltage gain, and a choice of either dual or single positive power supply operation.



(Pin Connections for J-8 or N Package)
Packages:
H Suffix – Case 601
J-8 Suffix – Case 693
J Suffix – Case 632
N Suffix – Case 626 (LM311 only)

LM111 – T_A = -55 to 125°C
LM211 – T_A = -25 to 85°C
LM311 – T_A = 0 to 70°C
Single comparators; high gain, high input impedance; strobe and balance inputs provided.

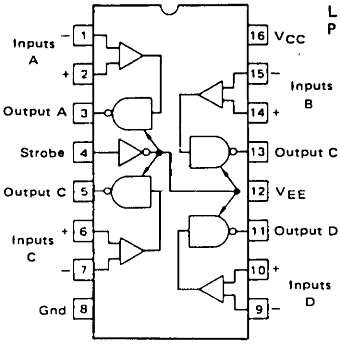
Device Number	V_{IO} mV Max	I_{IB} nA Max	V_{OL} @ I_{OL} = 50 mA Volts Max
LM111	3.0	100	1.5
LM211	3.0	100	1.5
LM311	7.5	250	1.5

Quad Comparators . . . for applications requiring multiple comparators.

MC3430
MC3431 } – High-speed quad comparators with three-state Enable common to all four devices; ±5 volt supply; T_A = 0 to 70°C.

MC3432
MC3433 } – Quad comparators with open collector outputs, common strobe input; ±5 volt supply; T_A = 0 to 70°C.

Packages:
L Suffix – Case 620
P Suffix – Case 648



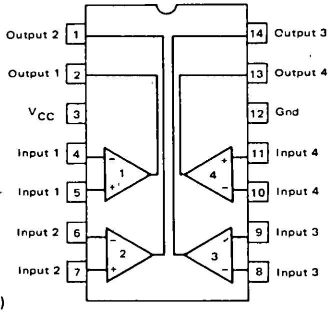
Device Number	V_{IS} mV Max	I_{IB} µA Max	t_{PHL} ns Max
MC3430	±6.0	20	45
MC3431	± 10	20	45
MC3432	±6.0	20	50
MC3433	± 10	20	50

LM139
LM139A } – T_A = -55 to 125°C

MC3302
LM2901
LM239
LM239A } – T_A = -40 to 85°C

LM339
LM339A } – T_A = 0 to 70°C

Single supply voltage comparators.



Packages:
J Suffix – Case 632
N Suffix – Case 646 (For all devices *except* LM139, LM139A)

Device Number	V_{IO} @ 25°C mV Max	I_{IB} @ 25°C nA Max	I_{sink} @ V_{OL} = 500 mV mA Min	V_{OL} @ I_{OL} = 2.0 mA* @ I_{OL} = 3.0 mA** @ I_{OL} = 4.0 mA mV Max
MC3302	20	1000	–	400*
LM2901	7.0	250	6.0	400**
LM139	5.0	100	6.0	500
LM139A	2.0	100	6.0	500
LM239	5.0	250	6.0	500
LM239A	2.0	250	6.0	500
LM339	5.0	250	6.0	500
LM339A	2.0	250	6.0	500

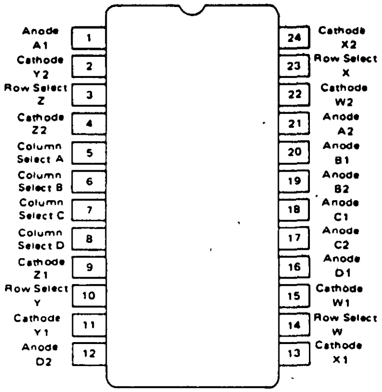
Crosspoint Switch

MC3416 – Low-cost solid-state crosspoint switch offers important advantages in modern telephone exchanges employing space-division switching. Features 4 x 4 two-wire monolithic structure for PABX applications. Select inputs are both CMOS and TTL compatible.

T_A = 0 to 70°C

Packages:
P Suffix – Case 649
L Suffix – Case 623

r_{off} @ V_{AK} = 10 V MΩ Min	r_{on} @ I_{AK} = 20 mA Ohms Max	BV_{AK} BV_{KA} Volts Min	V_{AK} @ I_{AK} = 20 mA Volts Max
100	10	25	1.1



Voice Encoding/ Decoding

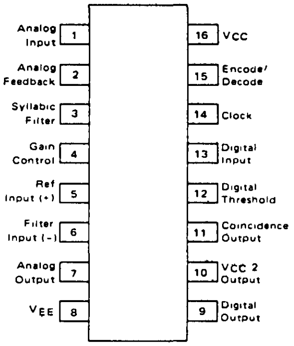
Simplified voice encoding/decoding using continuous Variable Slope Delta Modulator (CVSD) technique.

MC3417/MC3517 – 3-bit algorithm; for military secure communication and general-purpose low-sampling rate applications.

MC3418/MC3518 – 4-bit algorithm; telephone quality.

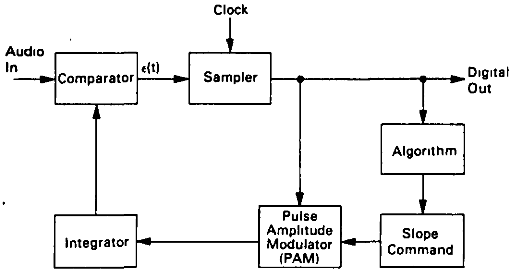
T_A = 0 to 70°C – MC3417/MC3418
= –55 to +125°C – MC3517/MC3518

Packages:
L Suffix – Case 620
P Suffix – Case 648

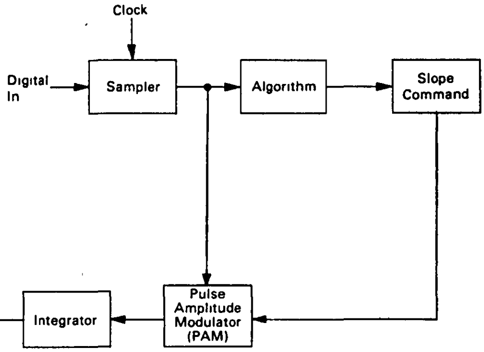


Device Number	Sample Rate Samples/s Typ	Total Loop Offset Voltage mV Max	t_{PD}, Clock Trigger to Output µs Max
MC3417/MC3517	16 k	±5.0	2.5
MC3418/MC3518	38 k	±2.0	2.5

CVSD Encoder



CVSD Decoder



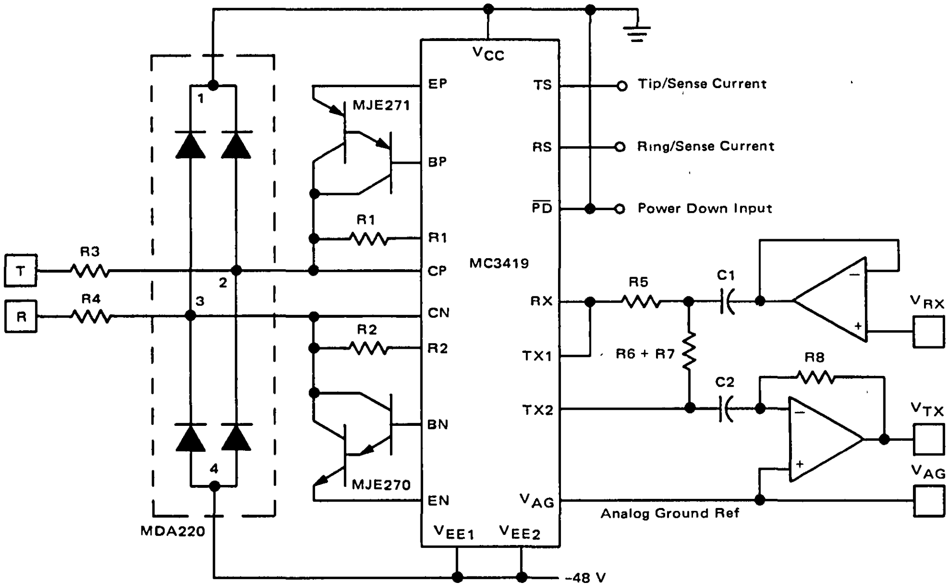
Digital Voice Channel

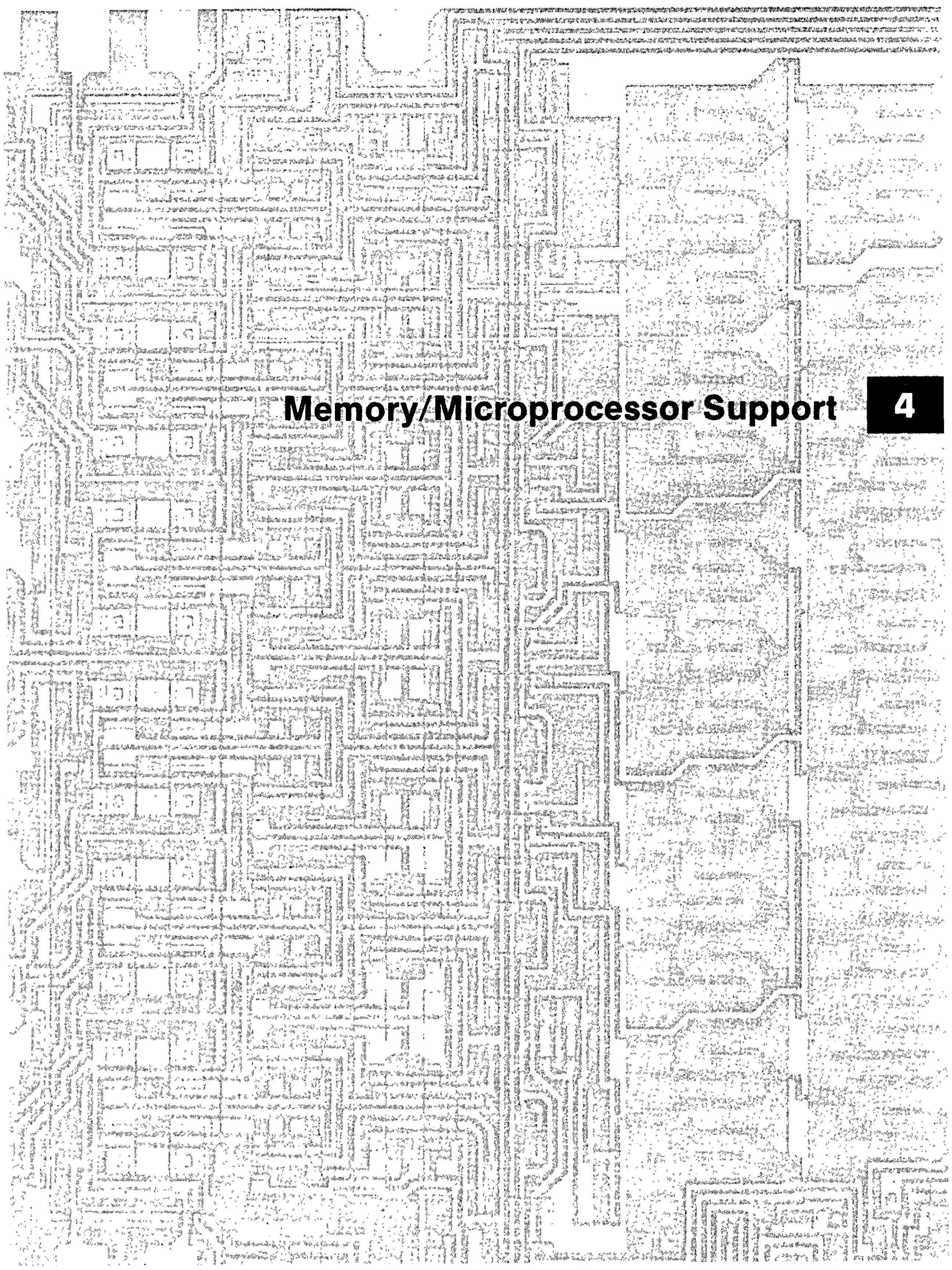
SUBSCRIBER LOOP INTERFACE CIRCUIT

MC3419/MC3519 — Designed to replace the hybrid transformer in Class 5, PBAX and Subscriber Carrier Equipment, this circuit provides signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. The transhybrid gain is externally selected and provides dc line current for powering the telset. It operates from up to a 60 V supply. On-hook power is below 5 mW and current sensing outputs are provided for off-hook status from both tip and ring leads. It offers size and weight reduction over present approaches and is compatible with IEEE and REA specifications.

T_A = 0 to 70°C — MC3419
= −40 to +85°C — MC3519

Packages:
L Suffix — Case 726
P Suffix — Case 701





Memory/Microprocessor Support

4

MEMORY/MICROPROCESSOR SUPPORT

MOTOROLA

MC1444
MC1544

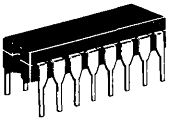
HIGH-SPEED, LOW THRESHOLD SENSE AMPLIFIERS

The MC1444 and MC1544 are high-speed quad sense amplifiers for use with plated wire, thin film or other memory systems requiring very low threshold sensitivity and narrow pulse widths. Both devices feature internal capacitive coupling to reduce the effects of voltage offsets.

- Threshold Level – 1.5 mV (Typ), 100 ns Rectangular Pulse
- Decoded Input Channel Selection
- Output Strobe Capability
- DC Level Restore Gate on Internal Capacitors Eliminates Repetition Rate Limitations

AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CASE 620

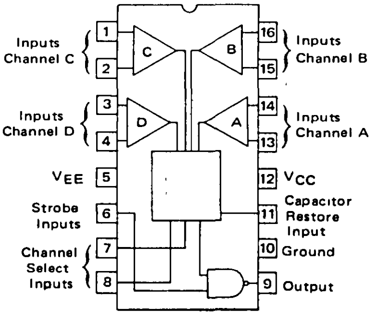
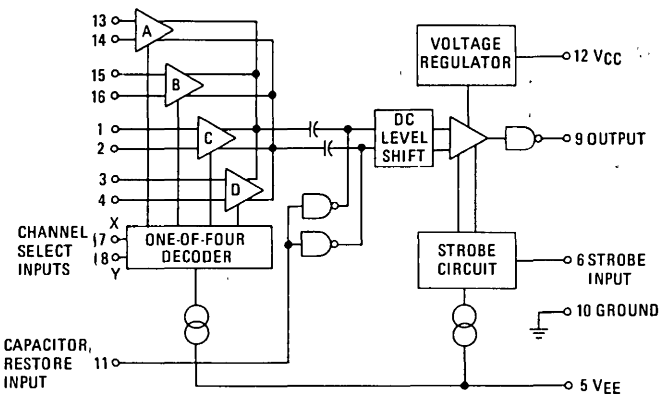


FIGURE 1 – BLOCK DIAGRAM



TRUTH TABLES

Channel Select		
Pin 7(X)	Pin 8(Y)	Channel Selected
H	H	A
L	H	B
H	L	C
L	L	D

H = high level (steady state, $V_I \geqslant V_{IH(min)}$ or $V_{ID} > V_{th}$

L = low level (steady state), $V_I \leqslant V_{IL(max)}$ or $V_{ID} < V_{th}$

X = irrelevant (any input, including transitions)

↑ = transition from low level to high level

⊔ = low-level output pulse

Inputs					Output
Strobe	Capacitor Restore	Differential Input *Channel A	Channel Selects		
L	X	X	X	X	H
X	H	X	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	L	H	H	↑	⊔
H	L	H	↑	H	⊔
↑	L	H	H	H	⊔

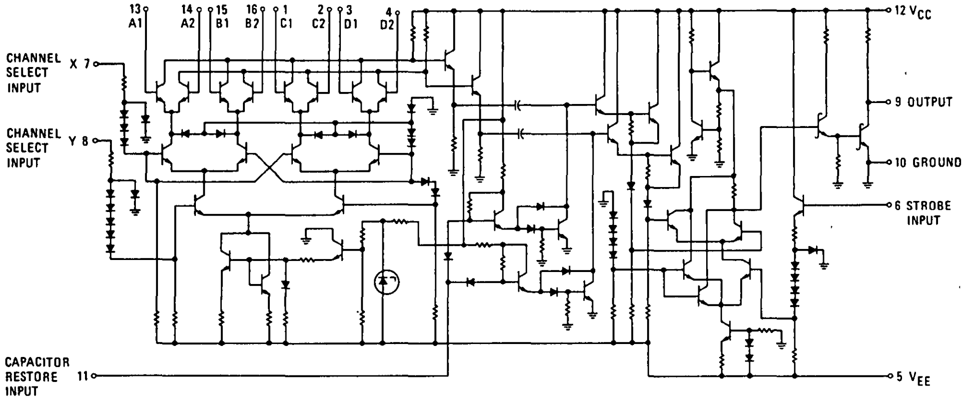
*Channel A used as an example, other channels function similarly. See channel select table.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating		Symbol	Value	Unit
Power Supply Voltages(1)		V_{CC} V_{EE}	+7.0 -8 0	Vdc
Input Common-Mode Voltage Range		V_{ICR}	+5 0, -6.0	Vdc
Input Differential-Mode Voltage Range(2)		V_{IDR}	+5.0, -6 0	Vdc
Input Capacitor Restore, Channel Select, and Strobe Voltage		$V_{I(CR)}$ $V_{I(CS)}$ $V_{I(S)}$	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = 25°C		P_D	1.0 6.7	Watt mW/°C
Operating Ambient Temperature Range	MC1444 MC1544	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Operating Junction Temperature		T_J	+175	°C

(1) All voltage values, except differential voltages, are with respect to the network ground terminal.
(2) Differential input voltages are at A1 with respect to A2, and similarly B1 to B2, C1 to C2, and D1 to D2

FIGURE 2 — EQUIVALENT CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	4.75 -5.7	5.0 -6.0	5.25 -6.30	V

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 V $\leq V_{CC} \leq$ 5.25 V, -5.7 V $\geq V_{EE} \geq$ -6.3 V, T_A = 25°C.)

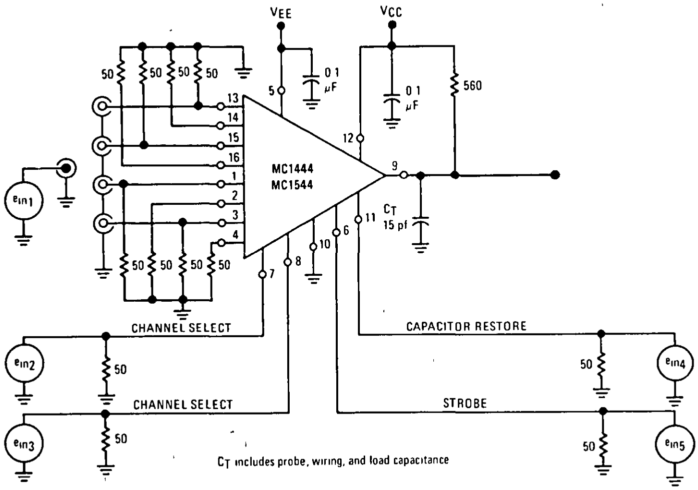
Characteristic	Symbol	MC1444			MC1544			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Threshold Voltage (Figure 4) (V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = T_{high} to T_{low}) (1)	V_{th}	0.3	1.0	2.3	0.5	1.0	1.5	mV
Input Bias Current (Selected Channel)	I_{IB}	–	20	50	–	20	50	µA
Input Offset Current (Selected Channel)	I_{IO}	–	1.0	10	–	1.0	10	µA
Channel Select Input Current-High Logic State, ($V_{IH(CS)}$ = 3 5 V)	$I_{IH(CS)}$	–	–	2.6	–	–	2.6	mA
Channel Select Input Current - Low Logic State, ($V_{IL(CS)}$ = 0 V)	$I_{IL(CS)}$	–	–	1.0	–	–	1 0	mA
Capacitor Restore Input Current - High Logic State, ($V_{IH(CR)}$ = 3 5 V)	$I_{IH(CR)}$	–	–	10	–	–	10	µA
Capacitor Restore Input Current-Low Logic State, ($V_{IL(CR)}$ = 0 V)	$I_{IL(CR)}$	–	–	-3 5	–	–	-3 5	mA
Strobe Input Current-High Logic State, ($V_{IH(S)}$ = 3.5 V)	$I_{IH(S)}$	–	–	200	–	–	200	µA
Strobe Input Current-Low Logic State ($V_{IL(S)}$ = 0 V)	$I_{IL(S)}$	–	–	200	–	–	200	µA
Channel Select Input Voltage-Low Logic State	$V_{IL(CS)}$	–	–	0.7	–	–	0 7	V
Channel Select Input Voltage-High Logic State	$V_{IH(CS)}$	2.1	–	–	2.1	–	–	V
Capacitor Restore Input Voltage-Low Logic State	$V_{IL(CR)}$	–	–	0 8	–	–	0 8	V
Capacitor Restore Input Voltage-High Logic State	$V_{IH(CR)}$	2 0	–	–	2.0	–	–	V
Strobe Input Voltage-Low Logic State	$V_{IL(S)}$	–	–	0 8	–	–	0 8	V
Strobe Input Voltage-High Logic State	$V_{IH(S)}$	2 0	–	–	2.0	–	–	V
Input Common-Mode Voltage Range	V_{ICR+} V_{ICR-}	– –	4.7 -6.0	– –	– –	4 7 -6 0	– –	V
Input Differential Voltage Range	V_{IDR}	–	±3.7	–	–	±3 7	–	V
Output Voltage-Low Logic State (I_{OL} = 10 mA)	V_{OL}	–	0.4	0 5	–	0.4	0.5	V
Output Voltage-High Logic State (I_{OH} = -400 µA)	V_{OH}	2.4	–	–	2.4	–	–	V
Positive Power Supply Current	I_{CC}	–	–	30	–	–	30	mA
Negative Power Supply Current	I_{EE}	–	–	30	–	–	30	mA

SWITCHING CHARACTERISTICS (unless otherwise noted, T_A = 25°C, V_{CC} = 5 0 V, V_{EE} = -6.0 V)

Characteristic	Symbol	MC1444			MC1544			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time Differential Inputs to High Logic State Output	$t_{PLH(D)}$	–	40	–	–	40	–	ns
Propagation Delay Time Differential Input to Low Logic State Output	$t_{PHL(D)}$	–	18	25	–	18	25	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	30	–	–	30	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	18	25	–	18	25	ns
Lead Time from Channel Select Input to Application of Differential Input Voltage	$t_{L(CS)}$	–	45	–	–	45	–	ns
Lead Time from Application of a 50 mV Offset Signal to Application of the Capacitor Restore Signal	$t_{L(CRO)}$	–	15	–	–	15	–	ns
Lead Time from Application of Strobe Input to Application of Differential Input Signal	$t_{L(S)}$	–	10	–	–	10	–	ns
Lead Time from Application of Capacitor Restore Signal to Application of Differential Input Signal	$t_{L(CR)}$	–	10	–	–	10	–	ns
Common-Mode Recovery Time (e_{in1} = +2 0 V) (e_{in1} = -2.0 V)	 t_{CMR+} t_{CMR-}	 – –	 50 50	 – –	 – –	 50 50	 – –	ns
Differential-Mode Recovery Time (e_{in1} = +1 0 V) (e_{in1} = -1.0 V)	 t_{DMR+} t_{DMR-}	 – –	 65 65	 – –	 – –	 65 65	 – –	ns

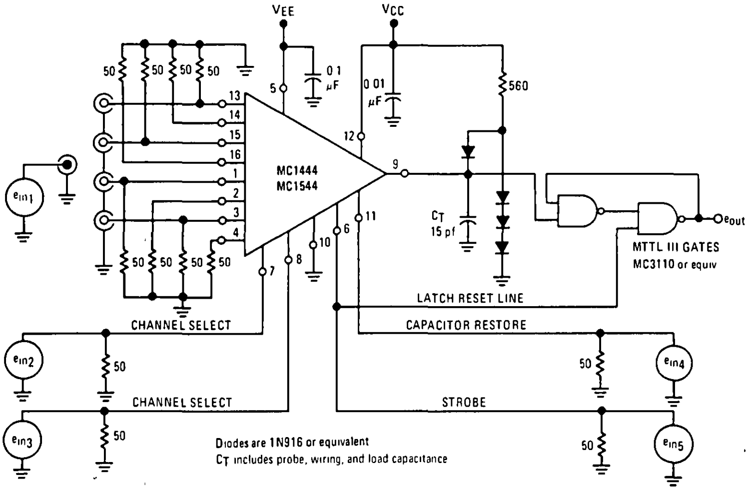
(1) T_{high} = 75°C for MC1444, 125°C for MC1544.
T_{low} = 0°C for MC1444, -55°C for MC1544.

FIGURE 3 – THRESHOLD VOLTAGE TEST CIRCUIT



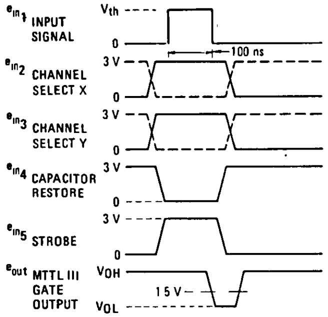
C_T includes probe, wiring, and load capacitance

FIGURE 4 – SWITCHING CHARACTERISTICS TEST CIRCUIT



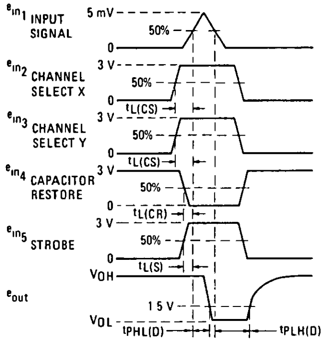
Diodes are 1N916 or equivalent
C_T includes probe, wiring, and load capacitance

FIGURE 5 – THRESHOLD VOLTAGE TEST



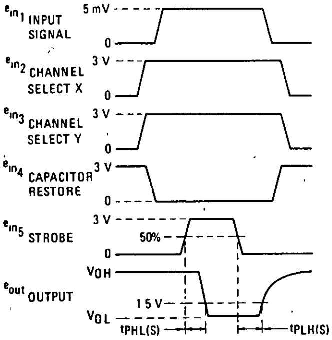
NOTE e_{in_2} and e_{in_3} to be normal or inverted (dotted line) as necessary to select desired channel For e_{in_1} - e_{in_5} $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} < 10$ ns

FIGURE 6 – $t_{L(CS)}$, $t_{L(CR)}$, $t_{L(S)}$, $t_{PLH(D)}$



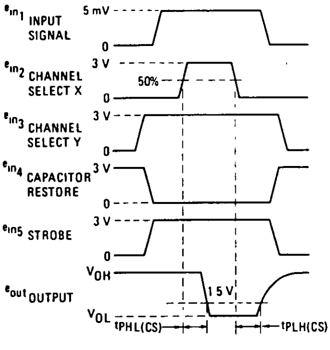
NOTE e_{in_2} - e_{in_5} $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} < 10$ ns

FIGURE 7 – $t_{PLH(S)}$, $t_{PHL(S)}$



NOTE e_{in_1} - e_{in_2} $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} < 10$ ns

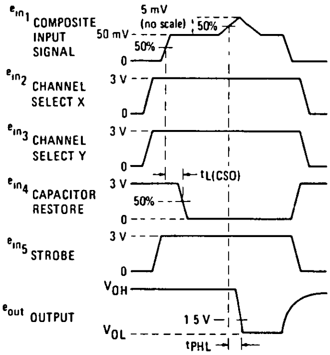
FIGURE 8 – $t_{PLH(CS)}$, $t_{PHL(CS)}$



NOTE To test other channel select input, reverse e_{in_2} and e_{in_3}

$e_{in1} - e_{in5}\begin{cases} t_{TLH} < 10\text{ ns} \\ t_{THL} \end{cases}$

FIGURE 9 – $t_{L(CRO)}$



NOTE $e_{in1} - e_{in2}\begin{cases} t_{TLH} < 10\text{ ns} \\ t_{THL} \end{cases}$

DEFINITIONS

V_{OH}	Output Voltage – High Logic State
V_{OL}	Output Voltage – Low Logic State
$V_{IH(S)}$	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
$V_{IL(S)}$	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal (e_{in_1}) required to drive the MTTL III gates to obtain the e_0 waveform shown in Figure 5
V_{ICM+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{ICM-}	The minimum common-mode input voltage that will not break down the amplifier
$V_{IH(CR)}$	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
$V_{IL(CR)}$	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
$V_{IH(CS)}$	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
$V_{IL(CS)}$	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{ID}	The maximum differential-mode input voltage that will not saturate the amplifier
I_{OH}	Output Source Current – High Logic State
I_{OL}	Output Sink Current - Low Logic State
$I_{IH(S)}$	The current into the strobe input when the input is at a high-level of 3 5 volts
$I_{IL(S)}$	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 2 volt common-mode signal (t_{TLH}, t_{THL} $\leqslant$ 15 ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
$t_{L(CRO)}$	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 9
$t_{L(CR)}$	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{L(CS)}$	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{PLH(CS)}$	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{PHL(CS)}$	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 1 volt differential-mode signal (t_{TLH}, t_{THL} $\leqslant$ 15 ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 23
$t_{PLH(D)}$	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 6
$t_{PHL(D)}$	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 6
$t_{L(S)}$	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 6
$t_{PLH(S)}$	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the High Logic Level as shown in Figure 7
$t_{PHL(S)}$	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the High Logic Level as shown in Figure 7
$I_{IH(CS)}$	The current into the channel select input when the input is at a high-level of 3.5 volts
$I_{IH(CR)}$	The current out of the capacitor restore input when the input is at a low-level of 0 volts
$I_{IL(CS)}$	The input current to a channel select input when that input is at a high-level of 3.5 volts
$I_{IL(CR)}$	The current into a channel select input when the input is at a low-level of 0 volts

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 10 – THRESHOLD VOLTAGE versus TEMPERATURE

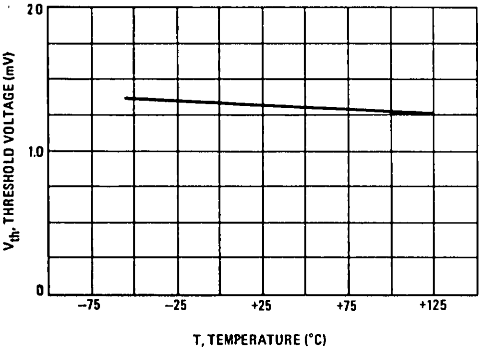


FIGURE 11 – THRESHOLD VOLTAGE versus POWER SUPPLIES

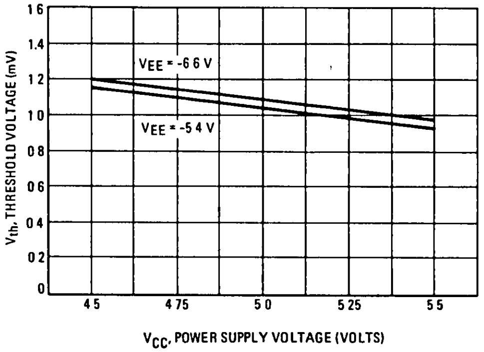


FIGURE 12 – THRESHOLD versus INPUT OFFSET VOLTAGE

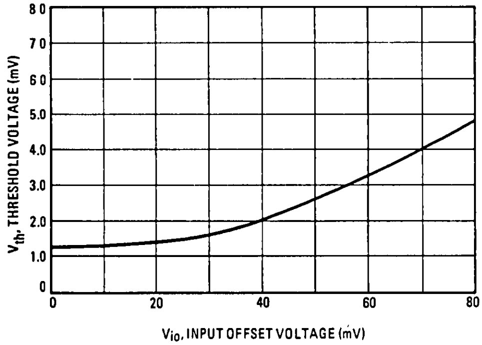


FIGURE 13 – THRESHOLD VOLTAGE versus PULSE WIDTH

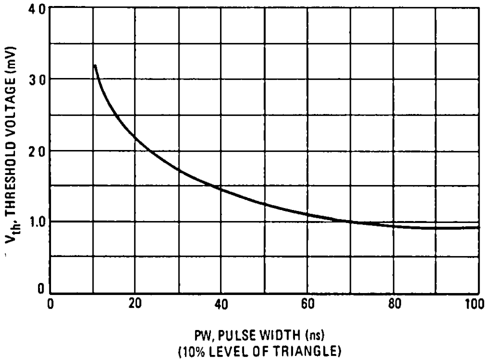


FIGURE 14 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

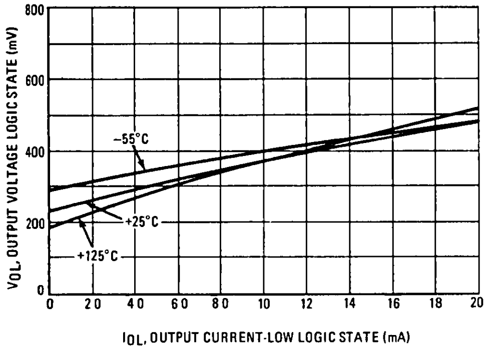
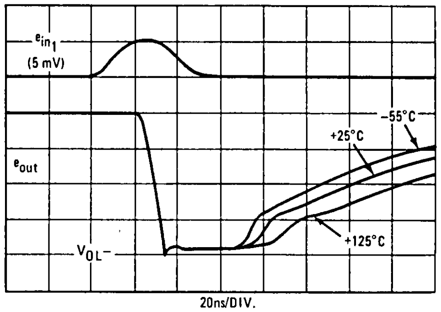


FIGURE 15 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figure 3 and 6)



TYPICAL CHARACTERISTICS (continued)

FIGURE 16 – INPUT IMPEDANCE versus FREQUENCY

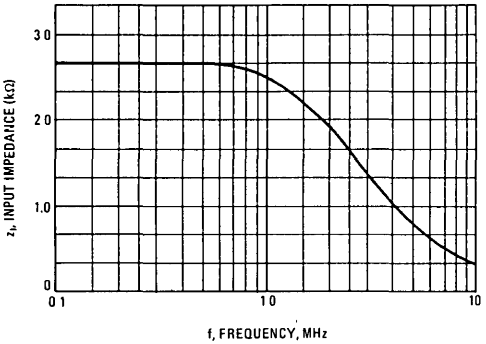


FIGURE 17 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

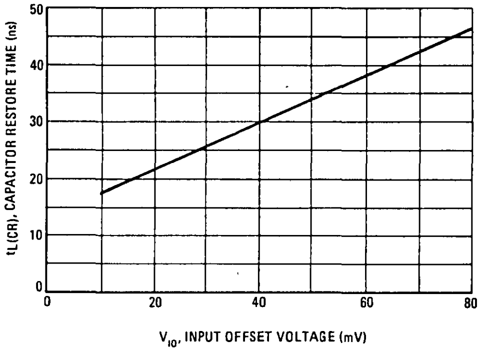


FIGURE 18 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

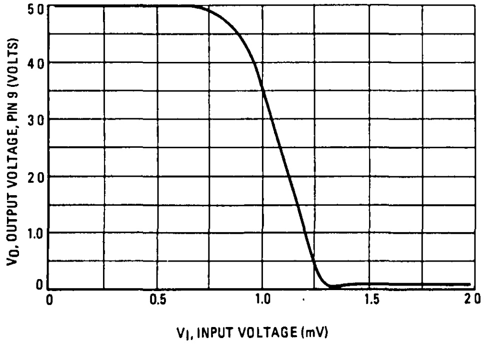


FIGURE 19 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

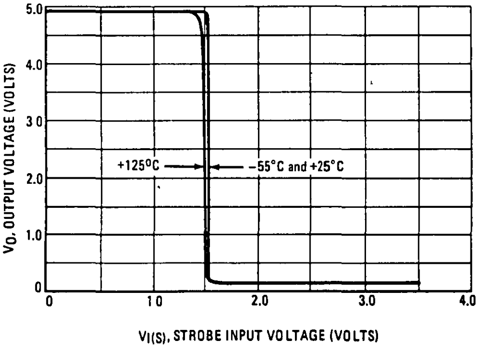


FIGURE 20 – CHANNEL SELECT X to OUTPUT TRANSFER CHARACTERISTICS

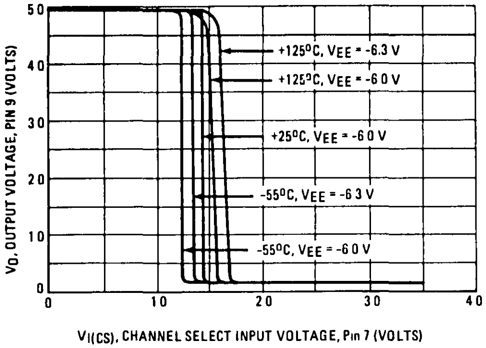


FIGURE 21 – CHANNEL SELECT Y to OUTPUT TRANSFER CHARACTERISTICS

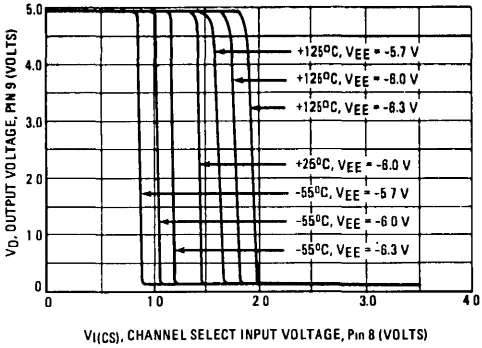


FIGURE 22 – COMMON-MODE CHARACTERISTICS

Note The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only

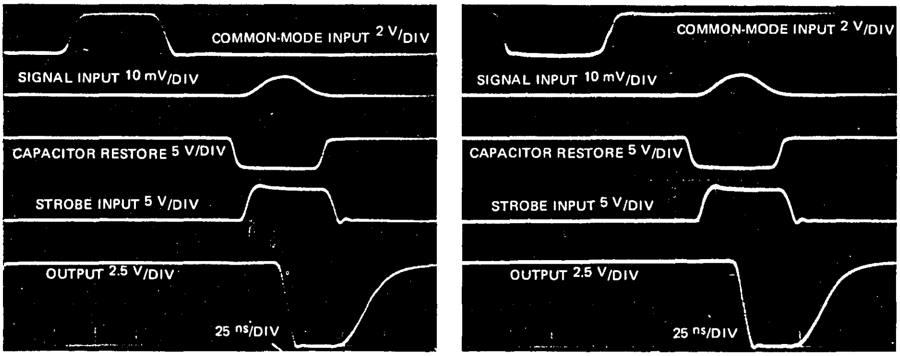
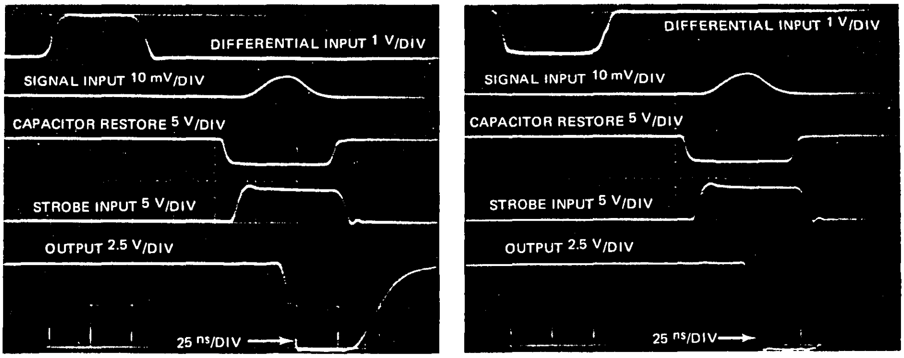


FIGURE 23 – DIFFERENTIAL-MODE CHARACTERISTICS

Note The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only



MOTOROLA

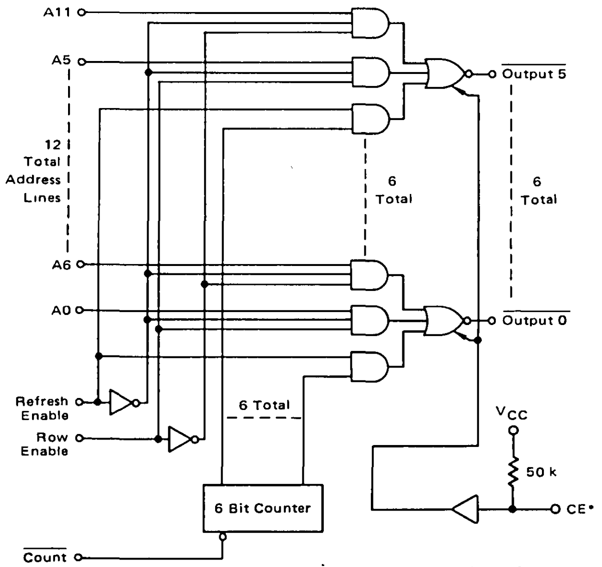
MC3232A

MEMORY ADDRESS MULTIPLEXER

The Motorola MC3232A is an address multiplexer and refresh counter for 16-pin 4K dynamic RAMs that require a 64-cycle refresh. It multiplexes twelve system address bits to the six input address pins of the memory device. The MC3232A also contains a 6-bit refresh counter that is clocked externally to generate the 64 sequential addresses required for refresh. The high performance of the MC3232A will enhance the high speed of the fast N-channel RAMs such as the MCM4027.

- Simplifies 16-Pin 4K Dynamic Memory Design
- Reduces Package Count
- 6-Bit Binary Counter for 64 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address
  Input to Output Delay
  t_{AO} = 25 ns @ C_L = 250 pF, 9.0 ns Max @ C_L = 15 pF
- Second Source to Intel 3232
  (Detect Zero Function Not Included and Additional
  Power Fail Feature Added at Pin 13)

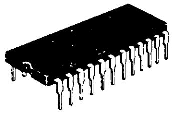
LOGIC DIAGRAM



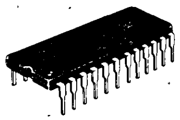
*See Pin Definitions

MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

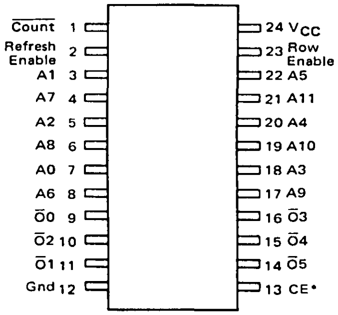
SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649



Note: A0 Through A5 Are Row Addresses
A6 Through A11 Are Column Addresses
*See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A5)
L	L	Column Address (A6 through A11)

$\overline{\text{Count}}$ – Advances Internal Refresh Counter

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V $\leq V_{CC} \leq$ 5.5 V, 0°C $\leq T_A \leq$ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	–	-0.04	-0.25	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	–	10	µA
Input Voltage, Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	–	–	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	–	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = -1.0 mA)	V_{OH}	2.8	4.0	–	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	-0.8	-1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	75	125	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V $\leq V_{CC} \leq$ 5.5 V, 0°C $\leq T_A \leq$ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output	t_{AO}				ns
(Load = 1 TTL, C_L = 250 pF)		–	12	25	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		–	6.0	9.0	
Row Enable to Output	t_{OO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	27	41	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	12	27	
Refresh Enable to Output	t_{EO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	30	45	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	14	27	
$\overline{\text{Count}}$ Pulse Width	$t_{W\overline{C}}$	30	–	–	ns
Counting Frequency	$f_{\overline{C}}$	5.0	10	–	MHz

FIGURE 1 – AC WAVEFORMS with MCM6604 NORMAL CYCLE

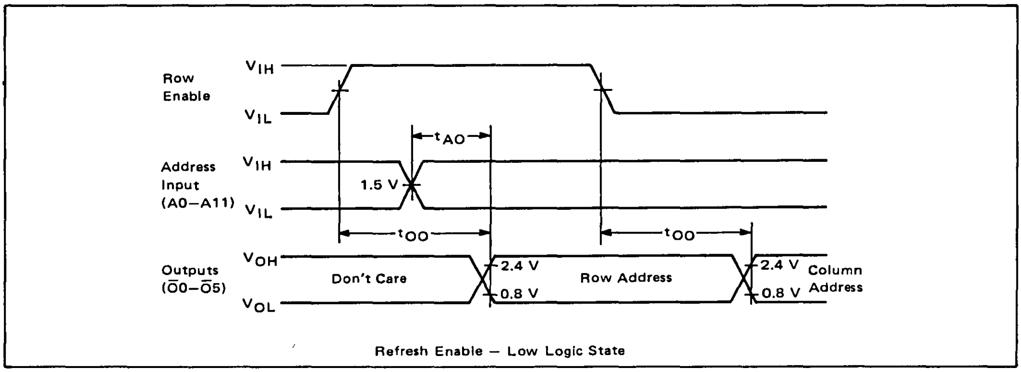
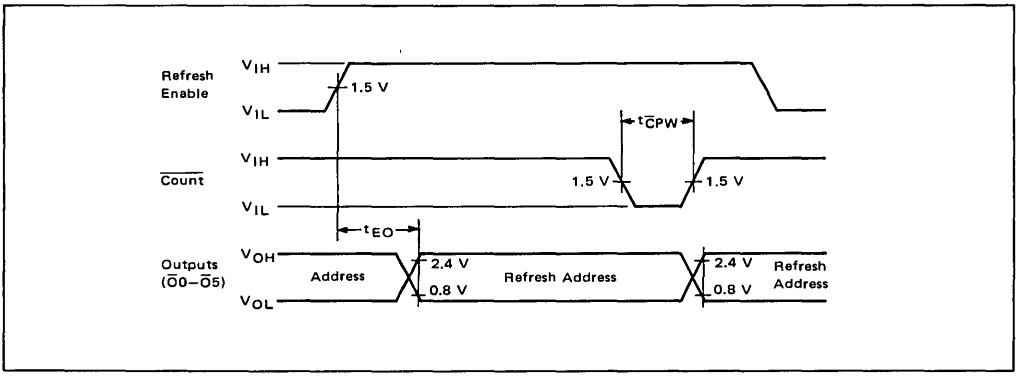


FIGURE 2 – REFRESH CYCLE



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

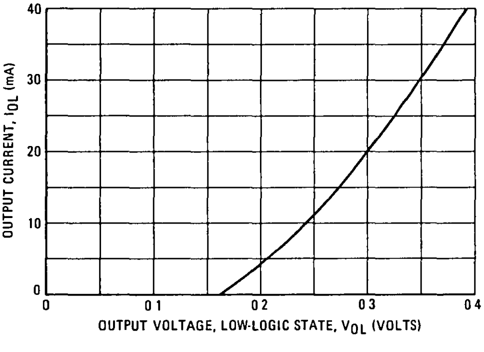
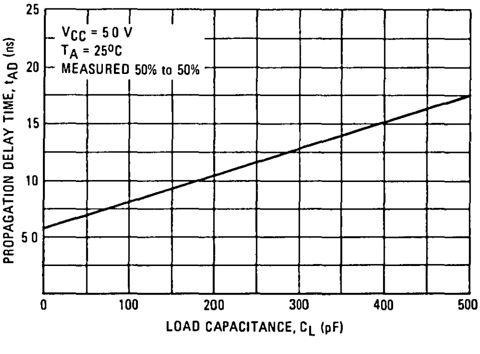


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



PIN DEFINITIONS

$\overline{\text{Count}}$ Input – Pin 1
Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2
Active high input which determines whether the MC3232A is in refresh mode (H) or address enable (L).

A0–A5 Inputs – Pins 7, 3, 5, 18, 20, 22
Row address inputs.

A6–A11 Inputs – Pins 8, 4, 6, 17, 19, 21
Column address inputs.

$\overline{\text{O}}$0–$\overline{\text{O}}$5 Outputs – Pins 9, 11, 10, 16, 15, 14
Address outputs to memories. Inverted with respect to address inputs.

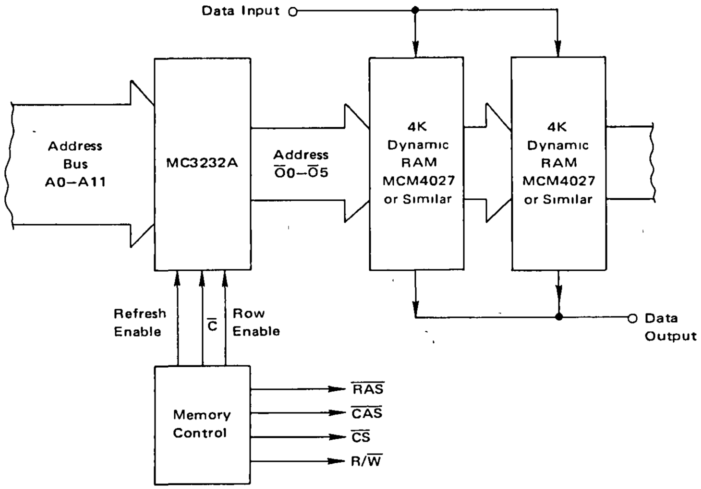
Gnd – Pin 12
Power supply ground.

CE Input – Pin 13
Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3232A is a functional replacement for the Intel 3232 (without detect zero function). As an active input, when pulled low, all 3232A outputs go three-state. Regardless of Pin 13 (CE) condition, when power (V_{CC}) is removed, all 3232A outputs go three-state. In addition, the refresh address counter is reset to all 1s so that upon return of supply power, control of refresh addressing can be returned to the MC3232A (by pulling Pin 13 high) at a known address (i.e., all 1s). This option is available tested by consulting factory.

Row Enable Input – Pin 23
High input selects row, low input selects column addresses of the driven memories.

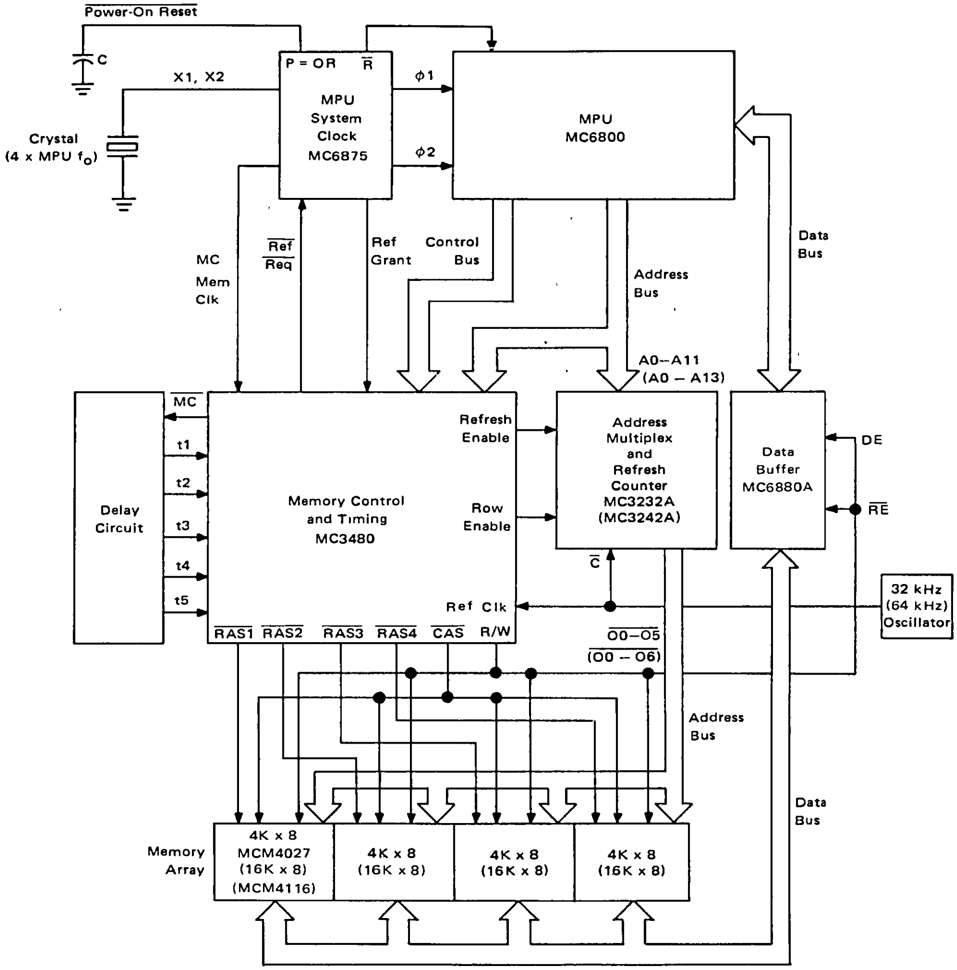
V_{CC} – Pin 24
+5 V power supply input. Due to high capacitance drive capability, a 0.1 µF capacitor should be used to ground along with careful V_{CC} and Gnd Bus layout.

GENERAL 4K DYNAMIC RAM
SIMPLIFIED BLOCK DIAGRAM



TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note. Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



MOTOROLA

MC3242A

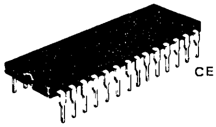
MEMORY ADDRESS MULTIPLEXER FOR 16K RAMS

The Motorola MC3242A is an address multiplexer and refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh. It multiplexes fourteen system address bits to the seven address pins of the memory device. The MC3242A also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

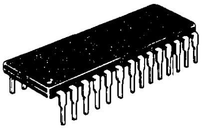
- Simplifies 16-Pin 16K Dynamic Memory Design
- Reduces Package Count
- 7-Bit Binary Counter for 128 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address Input
  to Output Delay —
  t_{AO} = 25 ns @ C_L = 250 pF
- Second Source to Intel 3242
  (Detect Zero Function Not Included and Additional
  Chip Enable Feature Added at Pin 15)

MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

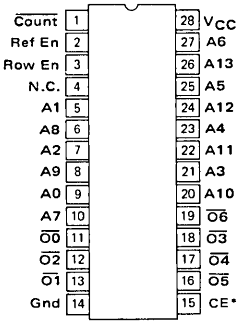
SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 733



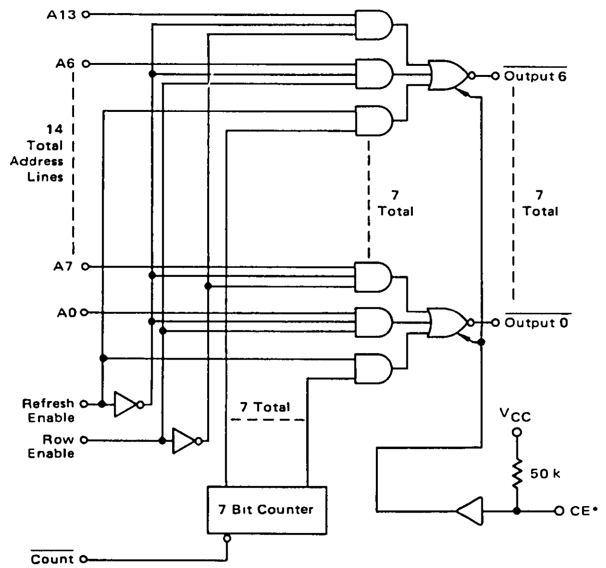
P SUFFIX
PLASTIC PACKAGE
CASE 710



Note: A0 Through A6 Are Row Addresses
A7 Through A13 Are Column Addresses

*See Pin Definitions

LOGIC DIAGRAM



*See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A6)
L	L	Column Address (A7 through A13)

$\overline{\text{Count}}$ — Advances Internal Refresh Counter

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	–	-0.04	-0.25	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	–	10	µA
Input Voltage, Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	–	–	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	–	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = -1.0 mA)	V_{OH}	3.0	4.0	–	V
Input Clamp Voltage (I_{IK} = -12 mA)	V_{IK}	–	-0.8	-1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	95	125	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C, typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output	t_{AO}				ns
(Load = 1 TTL, C_L = 250 pF)		–	12	25	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		–	6.0	9.0	
Row Enable to Output	t_{OO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	27	41	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	12	27	
Refresh Enable to Output	t_{EO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	30	45	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	14	27	
$\overline{\text{Count}}$ Pulse Width	$t_{W\overline{C}}$	30	–	–	ns
Counting Frequency	$f_{\overline{C}}$	5.0	10	–	MHz

FIGURE 1 – AC WAVEFORMS WITH MCM4116 NORMAL CYCLE

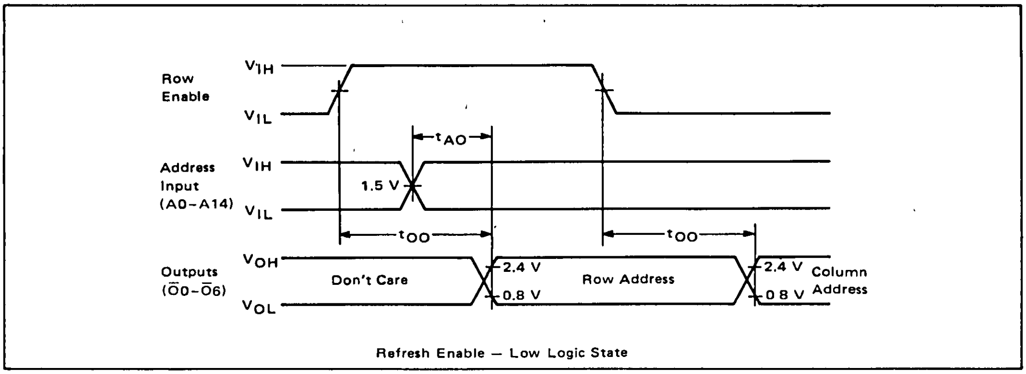
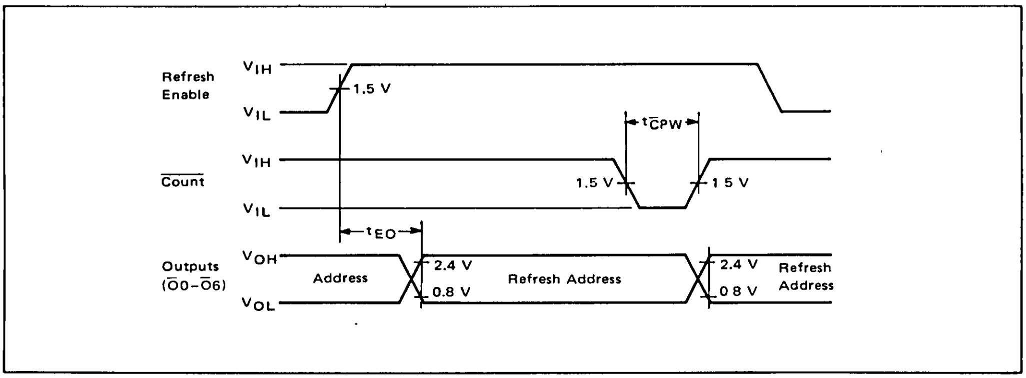


FIGURE 2 – REFRESH CYCLE



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

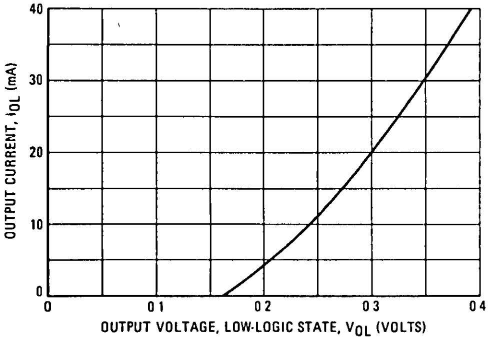
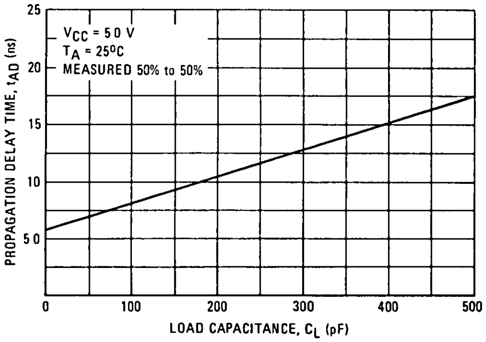


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



PIN DEFINITIONS

$\overline{\text{Count}}$ Input – Pin 1

Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2

Active high input which determines whether the MC3242A is in refresh mode (H) or address enable (L).

A0–A6 Inputs – Pins 9, 5, 7, 21, 23, 27

Row address inputs.

A7–A13 Inputs – Pins 10, 6, 8, 20, 22, 24, 26

Column address inputs.

$\overline{O0}$–$\overline{O6}$ Outputs – Pins 11, 12, 13, 18, 17, 16, 19

Address outputs to memories. Inverted with respect to address inputs.

Gnd – Pin 14

Power supply ground.

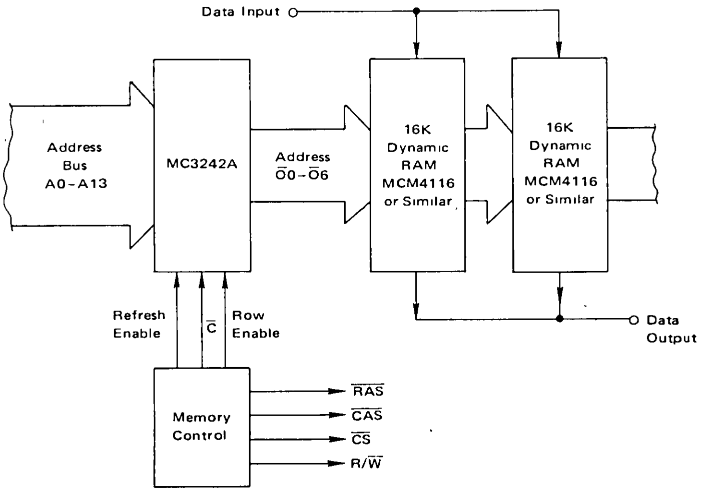
CE Input – Pin 15

Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state. Regardless of Pin 15 (CE) condition, when power (V_{CC}) is removed, all 3242A outputs go three-state. In addition, the refresh address counter is reset to all 1s so that upon return of supply power, control of refresh addressing can be returned to the MC3242A (by pulling Pin 15 high) at a known address (i.e., all 1s). This option is available tested by consulting factory.

V_{CC} – Pin 28

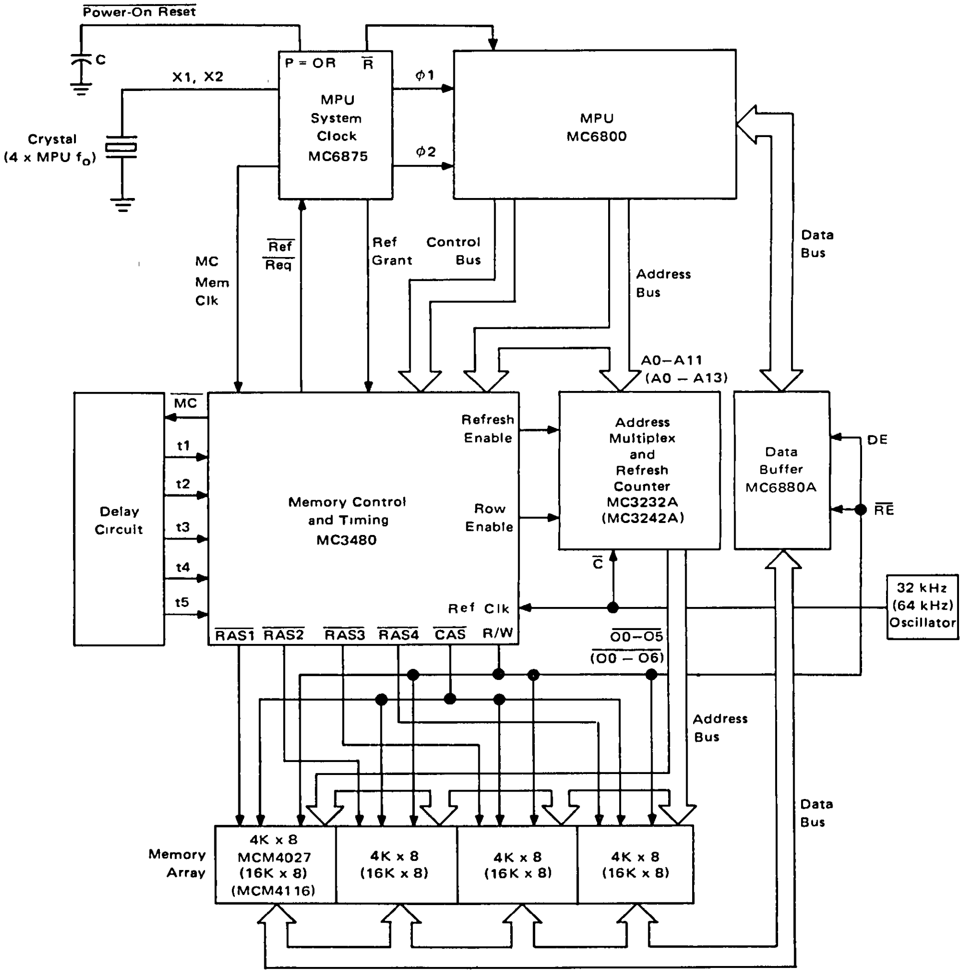
+5 V power supply input. Due to high capacitance drive capability, a 0.1 μF capacitor should be used to ground along with careful V_{CC} and Gnd Bus layout.

GENERAL 16K DYNAMIC RAM
SIMPLIFIED BLOCK DIAGRAM



TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



MOTOROLA

MC3245

QUAD TTL TO MOS DRIVER

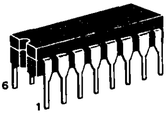
This high-speed driver is intended as a clock (high-level) driver for 22-pin and 18-pin dynamic NMOS RAMs and CCD memories. It is designed to operate on nominal +5 V and +12 V power supplies.

The channel control logic is organized so that all four drivers may be deactivated for STANDBY operation, or single driver may be activated for READ/WRITE operation or all four drivers may be activated for REFRESH operation.

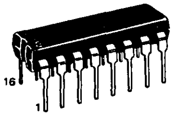
- Control Logic Optimized for Use in MOS RAM Systems
- Output Voltages Compatible with Many Popular MOS RAMs
- TTL and DTL Compatible Inputs — High-Speed Switching
- Interchangeable with Intel 3245

GATE-CONTROLLED FOUR-CHANNEL MOS CLOCK DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

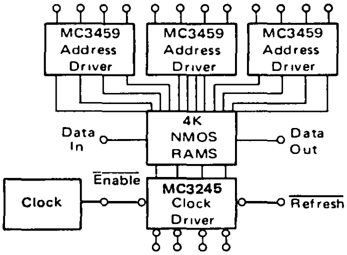


L SUFFIX
CERAMIC PACKAGE
CASE 620

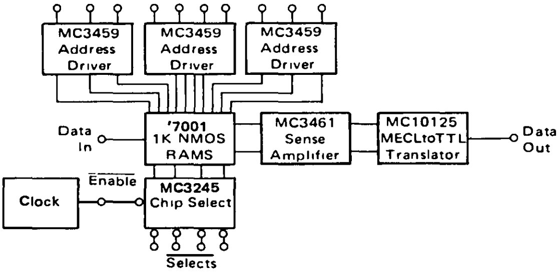


P SUFFIX
PLASTIC PACKAGE
CASE 648

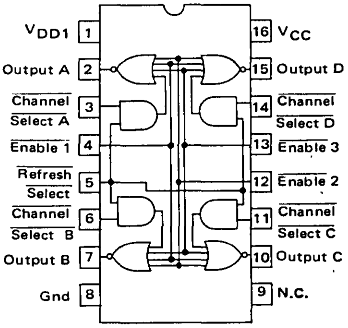
TYPICAL APPLICATION WITH 4K NMOS RAM IN TTL SYSTEM



TYPICAL APPLICATION WITH '7001 RAM AND TTL SYSTEMS



PIN CONNECTIONS



TRUTH TABLE

Inputs					Output
Control			Address		
$\overline{\text{Enable 1}}$	$\overline{\text{Enable 2}}$	$\overline{\text{Enable 3}}$	$\overline{\text{Channel}}$ $\overline{\text{Select}}$	$\overline{\text{Refresh}}$ $\overline{\text{Select}}$	
H	I	I	I	I	L
I	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	H	L
L	L	L	L	I	H
L	L	L	I	L	H

H = High Logic State
L = Low Logic State
I = Irrelevant

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{DD}	-0.5 to +7.0 -0.5 to +14	Vdc Vdc
Output Voltage	V_O	-1.0 to V_{DD} +1.0	Vdc
Input Voltage	V_I	-1.0 to V_{DD}	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{DD}	4.75 11.4	5.0 12	5.25 12.6	Vdc Vdc
Operating Ambient Temperature Range	T_A	0	–	75	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage – High Logic State (V_{IL} = 0.8 V, I_{OH} = -1.0 mA)	V_{OH}	V_{DD} - 0.5	–	–	Vdc
Output Clamp Voltage – High Logic State (I_{OH} = 5.0 mA, V_{IL} = 0 V)	V_{OHC}	–	–	V_{DD} + 1.0	Vdc
Output Voltage – Low Logic State (V_{IH} = 2.0 V, I_{OL} = 5.0 mA)	V_{OL}	–	–	0.45	Vdc
Output Clamp Voltage – Low Logic State (V_{IH} = 5.0 V, I_{OL} -5.0 mA)	V_{OLC}	-1.0	–	–	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (I_{IK} = -5.0 mA)	V_{IK}	–	–	-1.0	Vdc
Input Current – High Logic State (V_I = 5.0 V) Channel Select Inputs Refresh Select and Enable Inputs	I_{IH}	 – –	 – –	 10 40	µA
Input Current – Low Logic State (V_{IL} = 0.45 V) Channel Select Inputs Refresh Select and Enable Inputs	I_{IL}	 – –	 – –	 -0.25 -1.0	mA
Power Supply Current – Output High Logic State (V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OH} = 0 mA, V_{DD} = 12.6 V)	I_{CCH} I_{DDH}	– –	23 19	30 26	mA
Power Supply Current – Output Low Logic State (V_{CC} = 5.25, V_{IH} = 5.0 V, I_{OL} = 0 mA, V_{DD} = 12.6 V)	I_{CCL} I_{DDL}	– –	29 12	39 15	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at +25°C.)

Characteristic	Symbol	Min (1)	Typ (2)	Max (3)	Unit
Delay Time					ns
Output High to Low Level (R_S = 0 Ω)	t_{DHL}	3.0	7.0	–	
Output Low to High Level (R_S = 0 Ω)	t_{DLH}	5.0	11	–	
Transition Time					ns
Output High to Low Level (R_S = 20 Ω)	t_{THL}	5 0	17	25	
Output Low to High Level (R_S = 20 Ω)	t_{TLH}	10	17	25	
Propagation Delay Time					ns
Output High to Low Level (R_S = 0 Ω)	t_{PHL}	–	18	32	
Output Low to High Level (R_S = 0 Ω)	t_{PLH1}	–	20	32	
(R_S = 20 Ω)	t_{PLH2}	–	27	38	

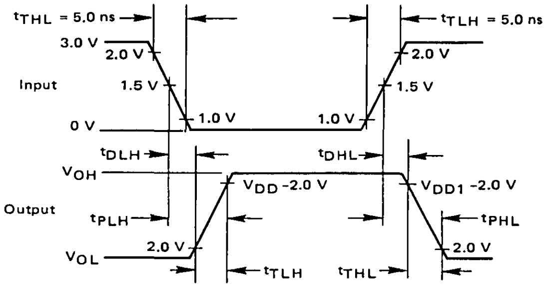
(1) C_L = 150 pF
(2) C_L = 200 pF
(3) C_L = 250 pF

CAPACITANCE* (Unless otherwise specified, T_A = +25°C, f = 1.0 MHz, V_I = 2.0 V, and V_{CC} = 0 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance Channel Select Inputs	$C_{in}(\overline{CS})$	–	5.0	8.0	pF
Input Capacitance Refresh or Enable Inputs	$C_{in}(\overline{E})$	–	8.0	12	pF

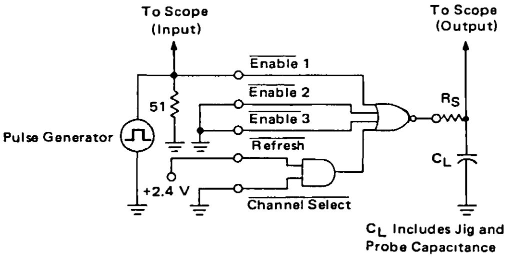
*Periodically sampled, but not 100% tested.

FIGURE 1 – SWITCHING TEST WAVEFORMS



Input Pulse Characteristics
PRR = 1 MHz
PW = 500 ns

FIGURE 2 – SWITCHING TEST CIRCUIT



C_L Includes Jig and Probe Capacitance

MOTOROLA

MC3459

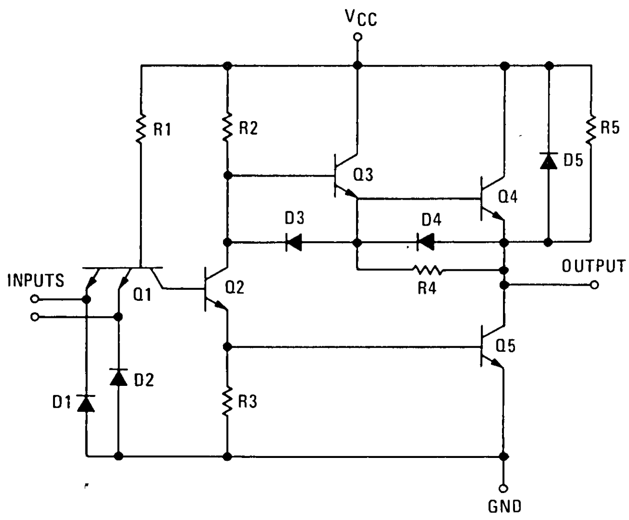
Specifications and Applications Information

QUAD NMOS MEMORY ADDRESS DRIVER

The MC3459 is designed for high-speed driving of the highly capacitive Address select inputs for NMOS Memories. It is also useful in numerous applications requiring a high-current MTTL NAND gate. It is pin-compatible with the popular MC7400 Quad NAND gate.

- Fast Propagation Delay Time – 20 ns Typical with 360 pF Load
- Output Voltages Compatible with NMOS Memories
- Inputs Compatible in MTTL and MDTL Logic Families
- Output Loading Factor – 50

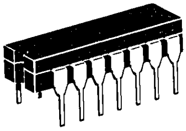
REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)

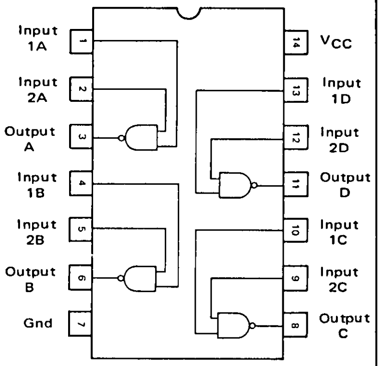


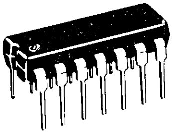
QUAD NMOS ADDRESS LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

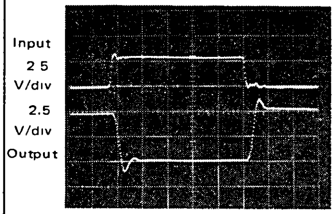






P SUFFIX
PLASTIC PACKAGE
CASE 646

TYPICAL OPERATION



V_{CC} = 5.0 V T_A = 25°C 50 ns/div C_L = 360 pF R_S = 0 Ω

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.5	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C)

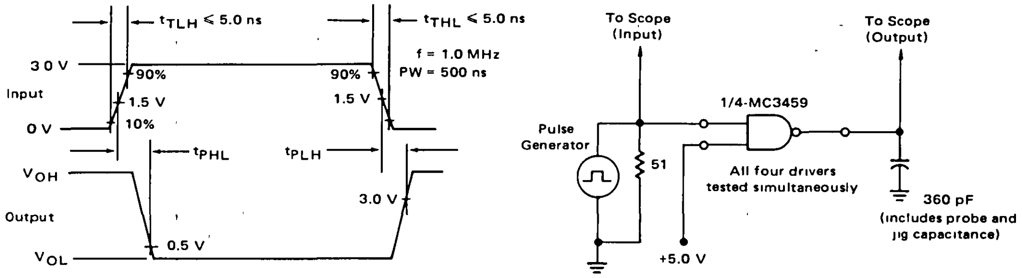
Characteristic	Symbol	Min	Typ(1)	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Current — High Logic State					
(V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH1}	–	–	80	µA
(V_{CC} = 5.25 V, V_{IH} = 5.5 V)	I_{IH2}	–	–	2.0	mA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.4 V)	I_{IL}	–	–	-3.6	mA
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output Voltage — High Logic State					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -640 µA)	V_{OH1}	3.2	–	–	
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -2.0 mA)	V_{OH2}	2.4	–	–	
Output Clamp Voltage (V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OC} = 5.0 mA)	V_{OC}	–	5.8	6.75	V
Output Voltage — Low Logic State					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 640 µA)	V_{OL1}	–	–	0.3	
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 80 mA)	V_{OL2}	–	–	0.7	
Power Supply Current — Outputs High Logic State (V_{CC} = 5.25 V, V_{IL} = 0 V)	I_{CCH}	–	12	18	mA
Power Supply Current — Outputs Low Logic State (V_{CC} = 5.25 V, V_{IH} = 5.0 V)	I_{CCL}	–	85	122	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C, C_L = 360 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — High to Low Logic State	t_{PHL}	–	21	32	ns
Propagation Delay Time — Low to High Logic State	t_{PLH}	–	16	26	ns

(1) Typical values measured at T_A = 25°C, V_{CC} = 5.0 V.

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES



TYPICAL PREFORMANCE CURVES

FIGURE 2 — POWER CONSUMPTION versus OPERATING FREQUENCY

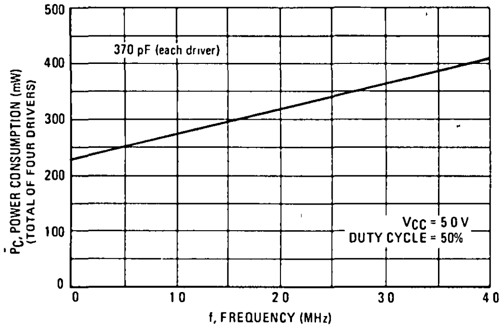


FIGURE 3 — OUTPUT VOLTAGE — HIGH LOGIC STATE versus OUTPUT CURRENT

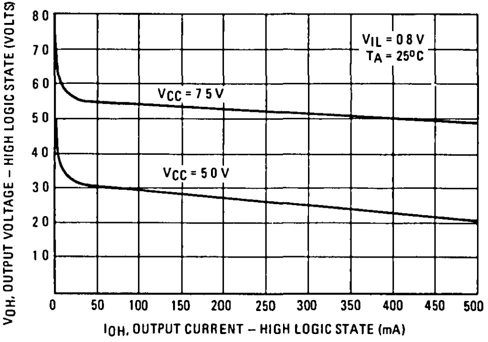


FIGURE 4 — OUTPUT VOLTAGE — HIGH LOGIC STATE versus OUTPUT CURRENT (Expanded Scale)

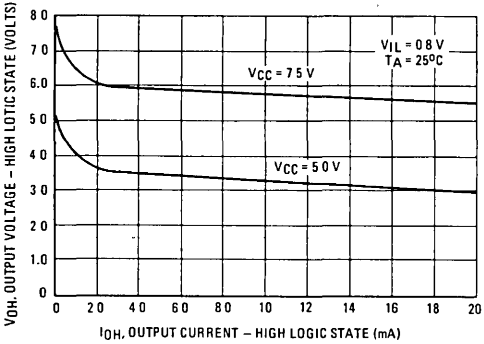
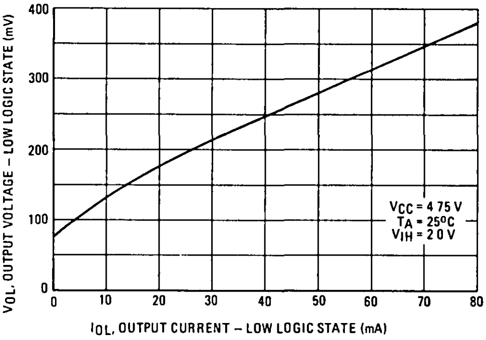


FIGURE 5 — OUTPUT VOLTAGE — LOW LOGIC STATE versus OUTPUT CURRENT



APPLICATIONS SUGGESTIONS

A majority of the new N-Channel MOS memories have TTL logic compatible inputs that exhibit extremely low input current and capacitance (typically 5 pF to 10 pF). However, in a typical memory system (Figure 6) where some of the inputs such as Address lines have to be common, the total parallel input capacitance can be over 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load; a high speed buffer, such as the MC3459, is required.

A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of the MC3459. The high capacitive discharge current during the high to low transition, plus current spikes can result in a considerable amount of noise being generated on the ground lead. Current spikes are due to both the upper and lower output drive transistors being on for a short period of time during switching. This causes a very low impedance path between V_{CC} and ground.

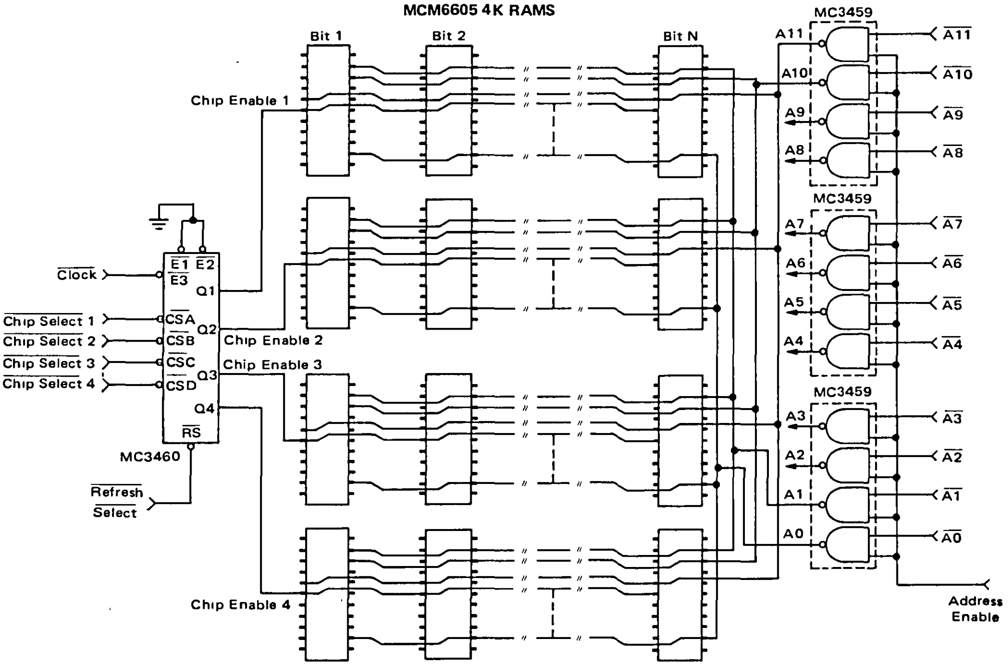
In order to minimize the effects of these currents, the following layout rules should be followed:

1. The V_{CC} supply pin of each package should be bypassed with a low inductance 0.01 μF capacitor. The 0.01 μF capacitor will sustain the high surge currents required during switching.
2. There is a large amount of current out of the ground node during switching — the noise seen at this node will be proportional to the ground impedance. The impedance of the ground bus can be reduced by increasing its width. At least a 50 mil ground width is recommended.

Some of the NMOS memories with TTL logic compatible inputs do not actually meet the TTL logic level requirements in the input high state voltage (V_{IH}). There are N-Channel MOS memories with a V_{IH} minimum ranging from 2.4 V to 4.0 V. The MC3459 can directly interface with those N-Channel memories having a V_{IH} minimum of 3.0 V. The higher driver output levels can be accomplished by adding a pull-up resistor to V_{CC} or by increasing the V_{CC} voltage.' There are some N-Channel MOS memories, such as the MCM7001, that have a supply requirement of 7.5 V. The high maximum supply voltage rating of the MC3459 can accommodate a 7.5 V V_{CC} supply without affecting its input TTL logic compatibility. Figure 4 gives the typical V_{OH} versus I_{OH} characteristics for both V_{CC} = 5.0 V and V_{CC} = 7.5 V. An expanded output characteristic curve of Figure 4 is illustrated in Figure 5.

The MC3459 can be used in a variety of applications including, high fan-out buffer (drives 50 standard TTL loads) and low impedance transmission line driver.

FIGURE 6 — TYPICAL APPLICATION
16 K X N Memory System Employing
MCM6605 4K RAMS



4N MCM6605 RAMS

MOTOROLA

MC3461

HIGH-SPEED NMOS/MECL SENSE AMPLIFIER

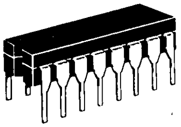
The MC3461 is a dual current sense amplifier with MECL 10,000 compatible control inputs and open emitter complementary outputs. The device is designed for use with Motorola MCM7001 or Intel 2105 NMOS 1K RAMs. A common latch input retains information in the amplifier at the time of latch closure. Separate channel output enables are provided to force the outputs to predetermined states until amplifier information exchange is desired.

When the latch input goes to a logic "0" the outputs are locked in their present state unless the output enable is at, goes to, logic "1". In this event, the Output 1 and Output 2 remain at, or go to, logic "0" and logic "1" respectively.

- Complete NMOS Sense Amplifier — No External Components Required
- Minimum Propagation Delay —
  - Amplifier Response - 5.0 ns Typ
  - Enable Response - 2.5 ns Typ
  - Latch Response - 1.0 ns Typ
- Power Supplies Compatible With MCM7001/MECL10,000 Systems
- Amplifier Input Termination Voltage Range from Gnd to V_{REF} Supply on MCM7001

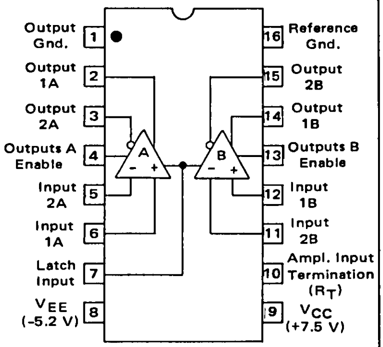
DUAL NMOS MEMORY SENSE AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

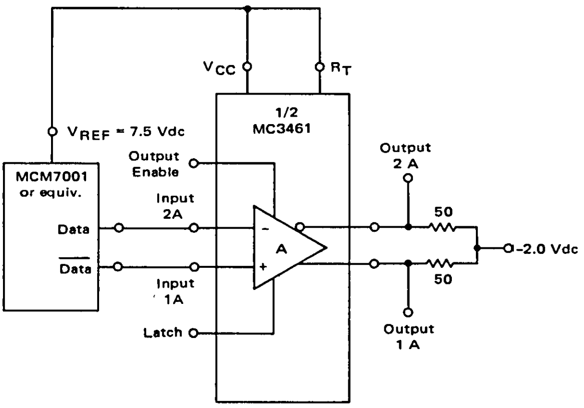


L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



APPLICATION WITH MCM7001 MEMORY



TRUTH TABLE
for latch input at logic 1

Input	Output Enable	Output 1	Output 2
I(1) ≥ -200 µA I(2) = 0 µA	0 1	0 0	1 1
I(1) = 0 µA I(2) ≥ 200 µA	0 1	1 0	0 1

Negative Currents Defined as Flowing into Device Pin.

MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^oC$)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}	8.5	V
	V_{EE}	-6.0	V
Termination Voltage	V_T	0 to V_{CC}	–
Operating Ambient Temperature Range	T_A	0 to 75	°C
Package Power Dissipation			
Still Air	P_D	1000	mW
Derate above 25°C		6.7	mW/°C
Transverse Air flow ⩾ 500 linear fpm		2000	mW
Derate above 25°C		13.3	mW/°C

ELECTRICAL CHARACTERISTICS

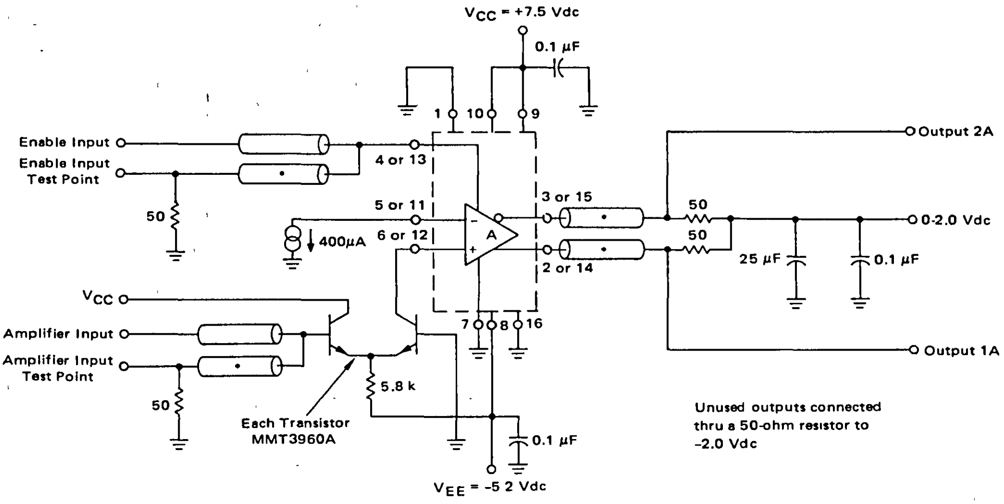
This device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one sense amplifier. The other half is tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts)						
	I_{sense}	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CC}	V_{EE}
0°C	⩾200µA	-0 850	-1 870	-1 155	-1 485	+7 5	-5 2
25°C	⩾200µA	-0 810	-1 850	-1 105	-1 475	+7 5	-5.2
75°C	⩾200µA	-0 720	-1 830	-1 045	-1 445	+7 5	-5 2

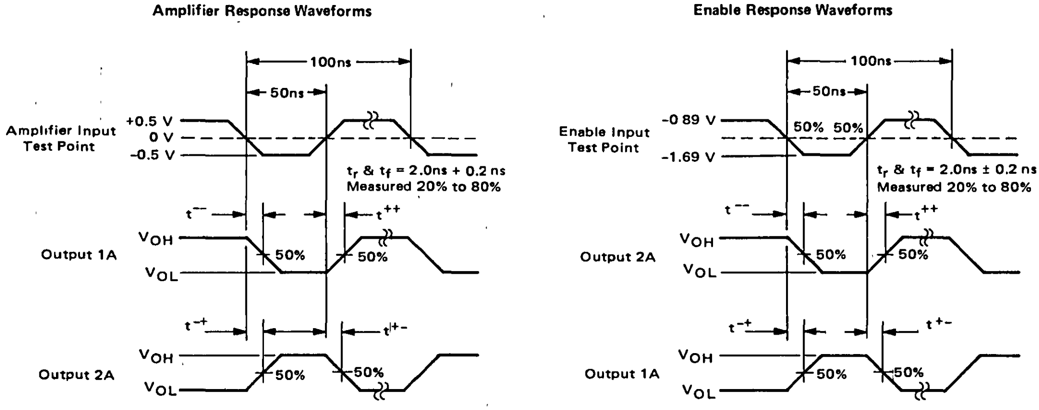
			MC3461 Test Limits								TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:							
			0°C		+25°C			75°C										
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Typ	Max	Min	Max	Unit	I_{sense}	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CC}	V_{EE}	Gnd
Power Supply Drain Current	I_{CC}	9	–	–	–	40	59	–	–	mAdc	6 12	–	–	–	–	9, 10	8	1, 16
	I_{EE}	8	–	–	–	-50	-73	–	–	mAdc	6,12	–	–	–	–	9, 10	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	500	–	–	µAdc	5, 11	4	–	–	–	9, 10	8	1, 16
		7	–	–	–	–	500	–	–	µAdc	5, 11	7	–	–	–	9, 10	8	1, 16
	I_{inL}	4	–	–	0 5	–	–	–	–	µAdc	5, 11	–	4	–	–	9, 10	8	1, 16
		7	–	–	0 5	–	–	–	–	µAdc	5, 11	–	7	–	–	9, 10	8	1, 16
Logic "1" Output Voltage	V_{OH}	3	-1 010	-0 850	-0 960	–	-0 810	-0 900	-0 720	Vdc	6	7	–	–	–	9, 10	8	1, 16
		2	↓	↓	↓	–	↓	↓	↓	↓	5	7	–	–	–	↓	↓	↓
		3	↓	↓	↓	–	↓	↓	↓	↓	5	7, 4	–	–	–	↓	↓	↓
Logic "0" Output Voltage	V_{OL}	3	-1 870	-1 660	-1 850	–	-1 650	-1 830	-1 620	Vdc	5	7	–	–	–	9, 10	8	1, 16
		2	↓	↓	↓	–	↓	↓	↓	↓	6	7	–	–	–	↓	↓	↓
		2	↓	↓	↓	–	↓	↓	↓	↓	5	7, 4	–	–	–	↓	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	3	-1 030	–	-0 980	–	–	-0 920	–	Vdc	6	–	–	7	4	9, 10	8	1, 16
		2	↓	–	↓	–	–	↓	–	↓	5	–	–	7	4	↓	↓	↓
		3	↓	–	↓	–	–	↓	–	↓	5	–	–	4,7	–	↓	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1 640	–	–	-1 630	–	-1 600	Vdc	5	–	–	7	4	9, 10	8	1, 16
		2	–	↓	–	–	↓	–	↓	↓	6	–	–	7	4	↓	↓	↓
		2	–	↓	–	–	↓	–	↓	↓	5	–	–	4,7	–	↓	↓	↓
Switching Times (50-ohm load)														Pulse In	Pulse Out			
Propagation Delay Amplifier	t--	2	–	–	–	5 0	10 0	–	–	ns	–	–	–	6	2	9, 10	8	1, 16
	t++	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓
	t-+	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
	t+-	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
Enable	t--	3	–	–	–	2 5	5 0	–	–	ns	–	–	–	4	3	9, 10	8	1, 16
	t++	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
	t-+	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓
	t+-	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓

*Negative currents are defined as currents leaving the device

FIGURE 1 – SWITCHING RESPONSE TEST CIRCUIT AND WAVEFORMS @ 25°C
(Other Section Tested Similarly)



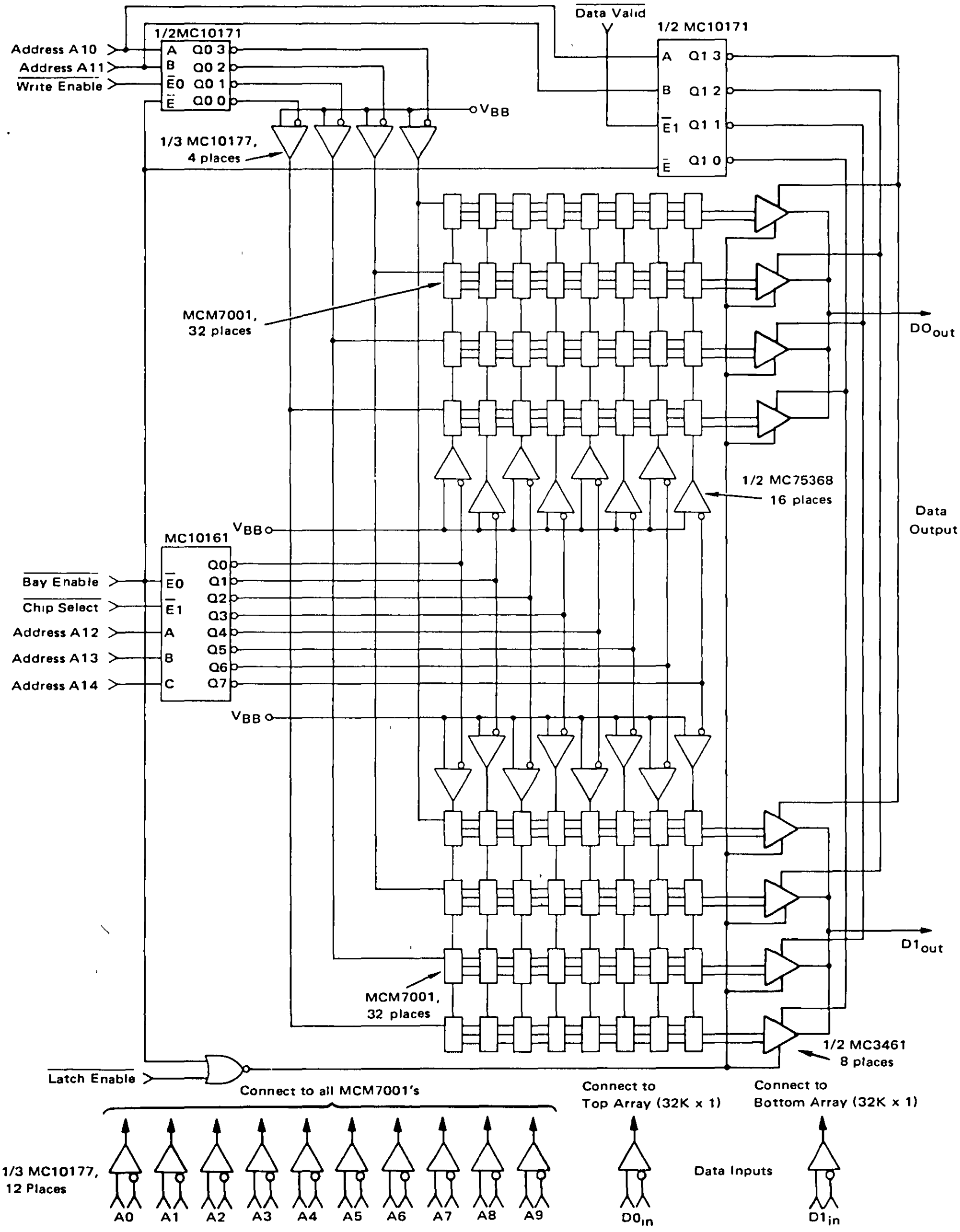
*Denotes equal lengths of 50-ohm coaxial cable. Wire length should be ⩽ 1/4" from test point to pin or BNC connector.



Enable input held at -1.69 Vdc for Amplifier Response Tests.

Amplifier input held at +0.5 Vdc for Enable Response Tests.

FIGURE 2 — 32K x 2 MEMORY BOARD (MECL SYSTEM)



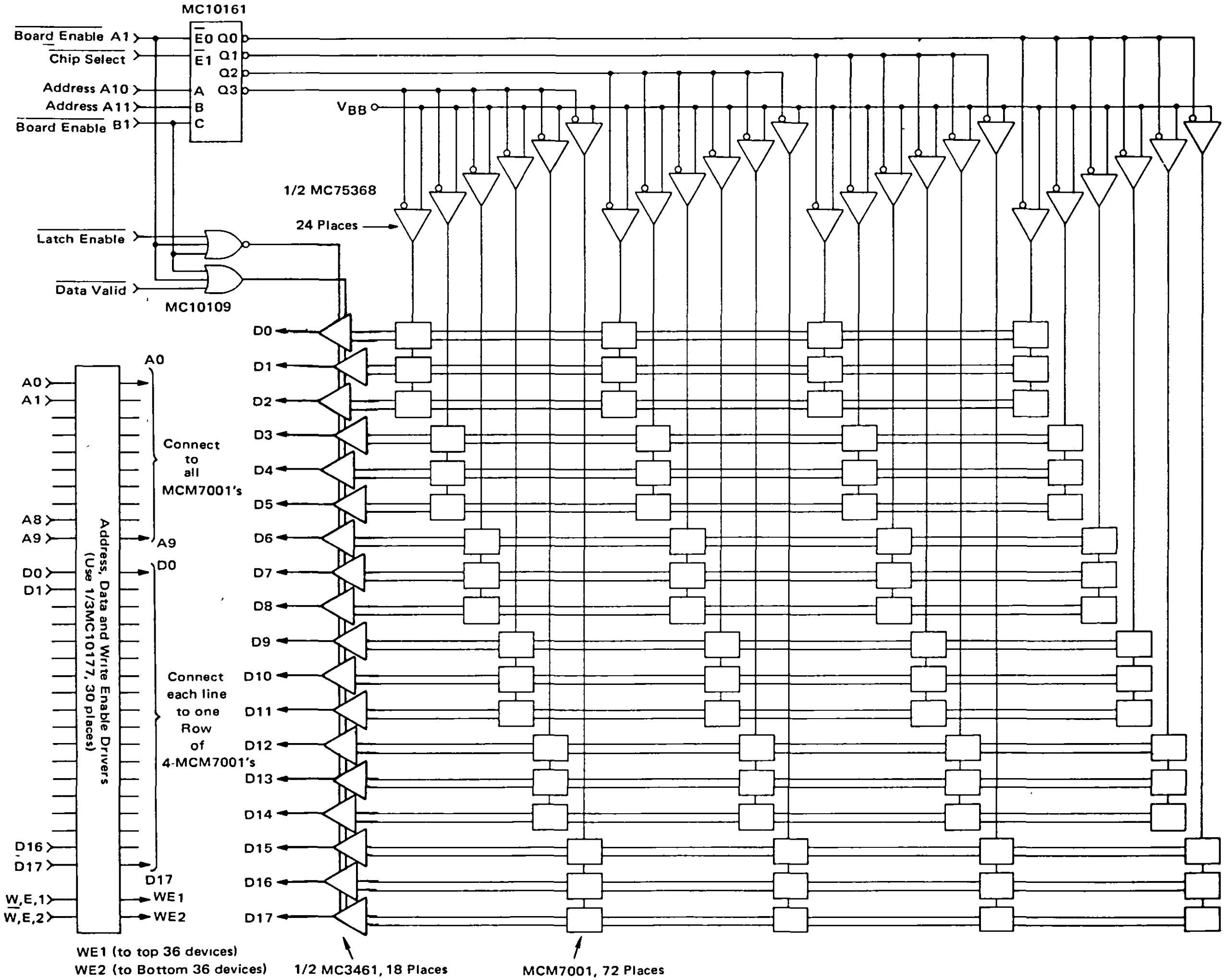
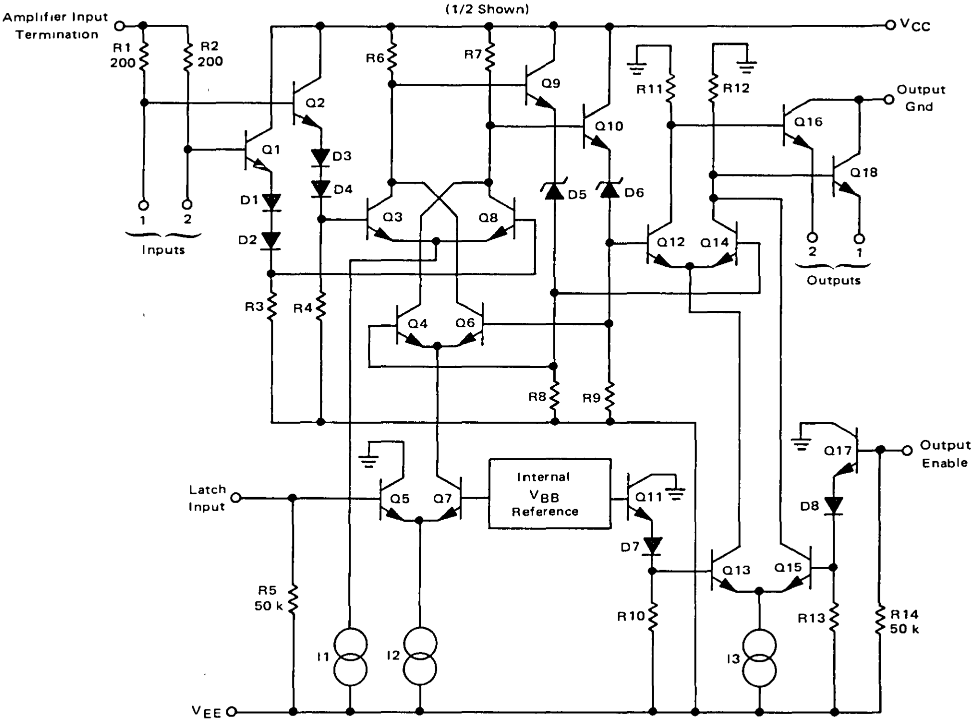


FIGURE 3 — 4K x 18 MEMORY BOARD (MECL SYSTEM)

REPRESENTATIVE CIRCUIT SCHEMATIC

Simplified MC3461
(1/2 Shown)



MOTOROLA

MC3467

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

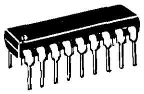
The MC3467 is intended to mate with the MC3468 read amplifier to provide the entire magnetic tape read function.

- Wide Bandwidth — 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

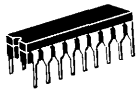
TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

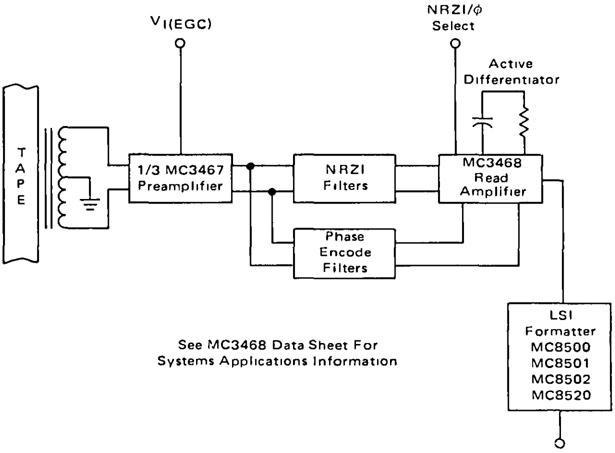
P SUFFIX
PLASTIC PACKAGE
CASE 701



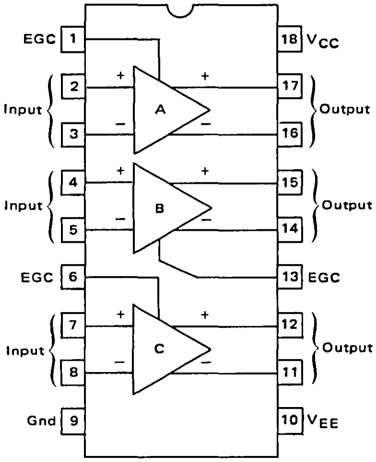
L SUFFIX
CERAMIC PACKAGE
CASE 726



TYPICAL APPLICATION HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM



See MC3468 Data Sheet For Systems Applications Information



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages			V
Positive Supply Voltage	V_{CC}	6.0	
Negative Supply Voltage	V_{EE}	−9.0	
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	−5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	±5.0	V
Input Common-Mode Voltage	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_s	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, f = 100 kHz, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range					
Positive Supply Voltage	V_{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EER}	−5.5	−6.0	−7.0	V
Operating EGC Voltage	$V_{I(EGC)}$	0	–	V_{CC}	V
Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, e_i = 25 mVp-p) (See Figure 1)	A_{VD}	85	100	120	V/V
Differential Voltage Gain ($V_{I(EGC)}$ = V_{CC})	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVp-p)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common-Mode Range	V_{ICR}	±1.5	±2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common-Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common Mode Rejection Ratio (Figure 2) $V_{I(EGC)}$ = 0, V_{CM} = 1.0 V_{pp}	CMRR				dB
(f = 100 kHz)		60	100	–	
(f = 1.0 MHz)		40	100	–	
Small-Signal Bandwidth (Figure 1) (−3.0 dB, e_i = 1.0 mVp-p, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	µA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	−30	−40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT
(Channel A under test, other channels tested similarly)

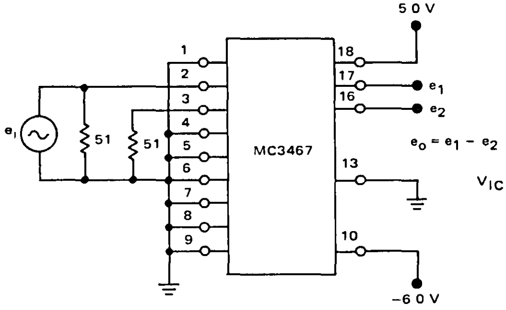
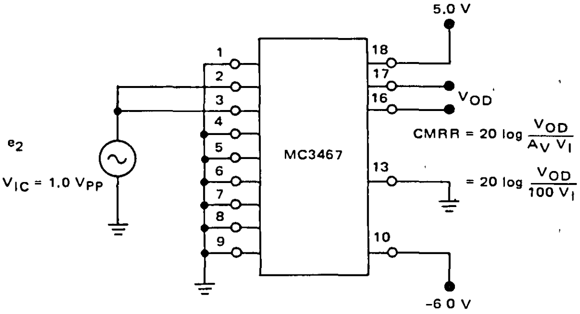
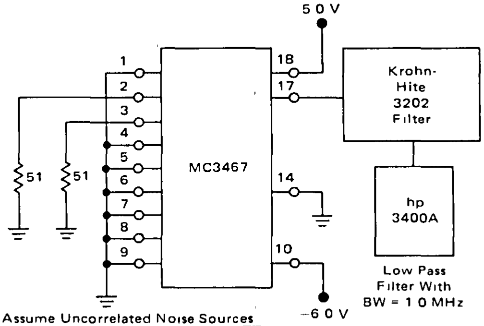


FIGURE 2 – COMMON-MODE REJECTION RATIO
(Channel A under test, other amplifiers tested similarly)



$$\mathrm{CMRR} = 20 \log \frac{V_{OD}}{A_V\, V_I} = 20 \log \frac{V_{OD}}{100\, V_I}$$

FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT



Assume Uncorrelated Noise Sources
e_n (Differential Noise at Input) = $e_o \sqrt{2}/100$

FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

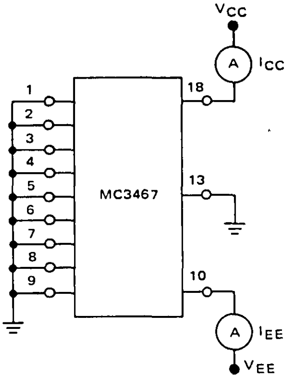


FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT
(Channel A under test, other channels tested similarly)

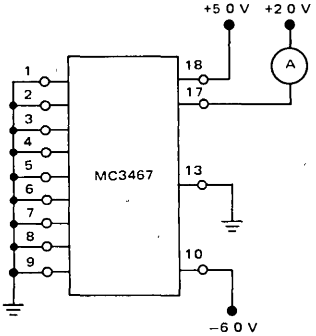
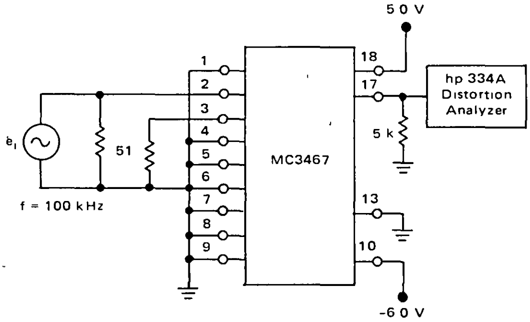


FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT
(Channel A under test, other channels tested similarly)



TYPICAL CHARACTERISTICS
$(V_{CC} = 5.0\ V,\ V_{EE} = -6.0\ V,\ T_A = 25^{\circ}$ **unless otherwise noted)**

FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE

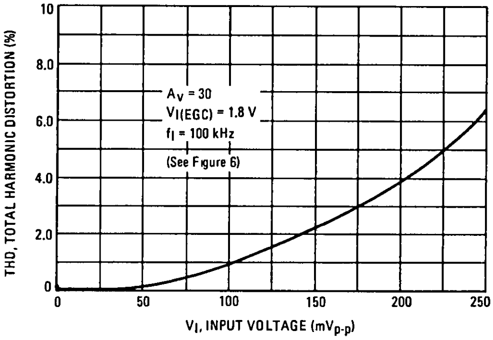


FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY

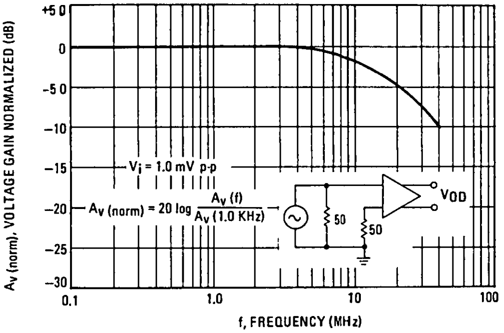


FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE

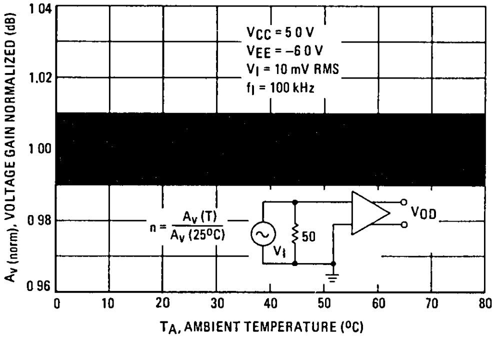


FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE

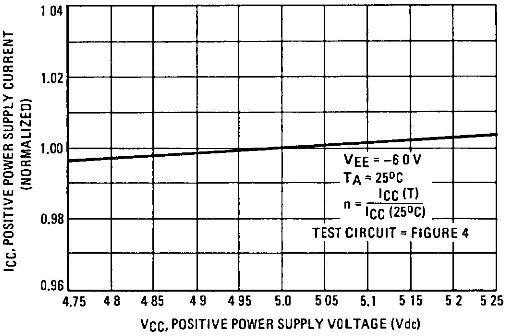


FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

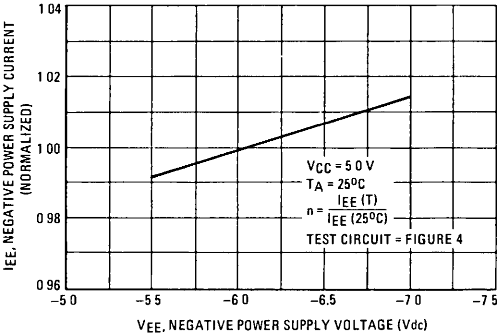


FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE

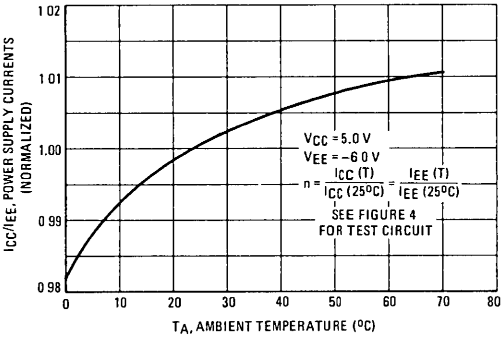


FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

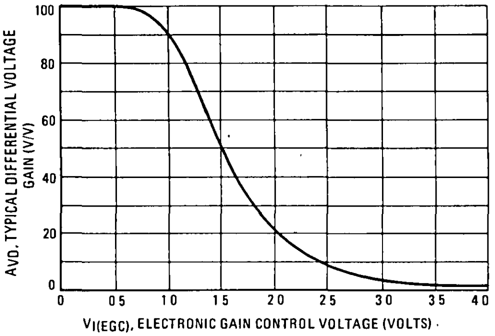


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

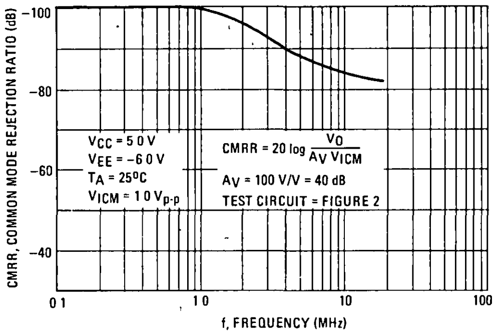


FIGURE 15 – PHASE SHIFT versus FREQUENCY

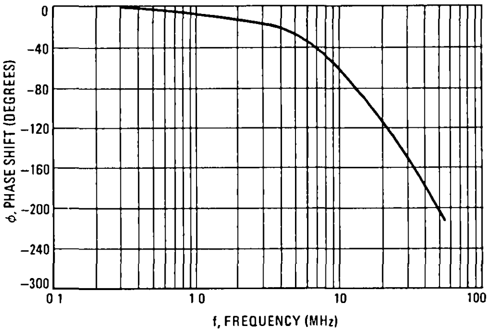
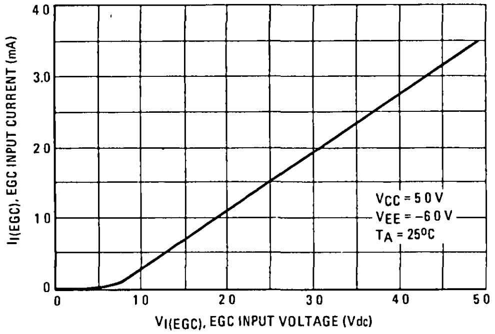
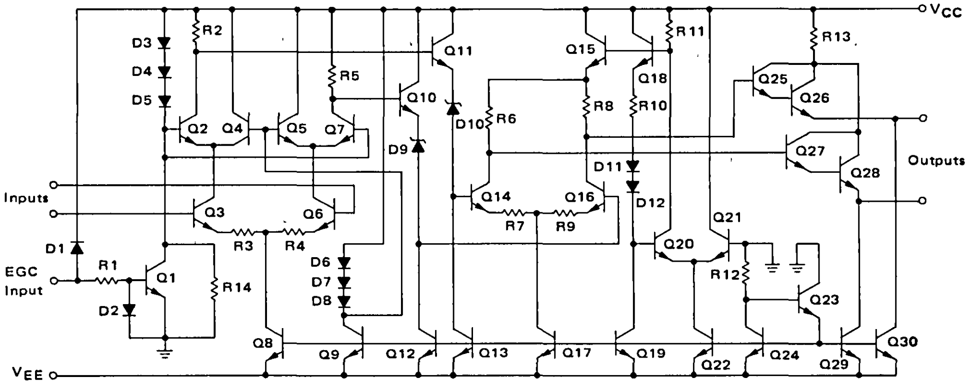


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467



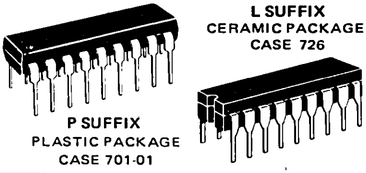
MOTOROLA

MC3468

Specifications and Applications Information

MAGNETIC TAPE MEMORY READ AMPLIFIER

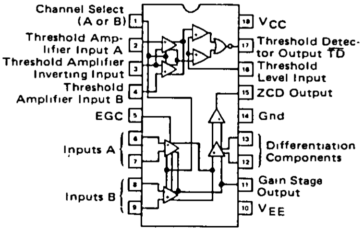
SILICON MONOLITHIC INTEGRATED CIRCUIT



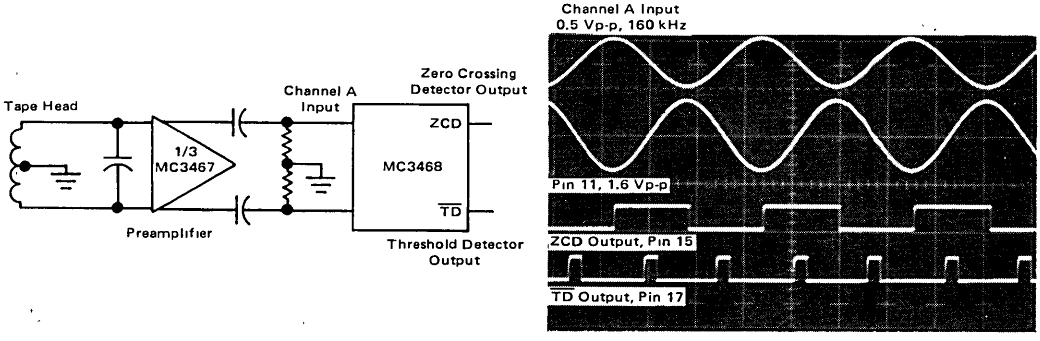
LSI MAGNETIC MEMORY READ SUBSYSTEM

The MC3468 READ Subsystem when used with the MC3467 triple preamplifier provides the interface between magnetic tape heads and digital logic. This system is well suited for open-reel and cartridge magnetic tape systems. The MC3468 performs peak detection, and threshold detection functions as required for NRZI, Phase-Encoded or Group-Encoded recording formats. The device consists of: 1) Input Multiplex function, 2) Gain Stage with Electronic Gain Control (EGC), 3) Active Differentiation Amplifier, 4) Zero Crossing Detector (ZCD), 5) Threshold Detector Amplifier with Multiplexed Inputs and 6) Threshold Detector.

- Complete READ Function in One LSI Device
- Two Pair of Differential Inputs Allow Logically Controlled Selection of Input Filter or Tape Head Configuration
- Low Recovered Error Rate
- Input/Outputs are Low Power Schottky TTL Compatible



MC3468 TYPICAL APPLICATION AND WAVEFORMS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages			
Positive Supply Voltage	V_{CC}	+7.0	V
Negative Supply Voltage	V_{EE}	−8.0	V
Pin Voltages			
EGC Voltage (Pin 5)	$V_{I(EGC)}$	−5.0 to +7.0	V
Threshold Voltage (Pin 16)	$V_{I(T)}$	+1.0 to −3.5	V
ZCD Output (Pin 15)	$V_{O(ZCD)}$	+7.0	V
Channel Select A/B Input (Pin 1)	$V_{I(CS)}$	+7.0 to −2.0	V
Threshold Output $\overline{TD}$ (Pin 17)	$V_{O(\overline{TD})}$	+7.0	V
Differential Input Voltage			
Threshold Amplifier	$V_{ID(T)}$	±5.0	V
Gain Amplifier	V_{ID}	±5.0	V

MAXIMUM RATINGS (continued)

Rating	Symbol	Value	Unit
Common Mode Input Voltage			
Threshold Amplifier	$V_{IC(T)}$	±5.0	V
Gain Amplifier	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (Ground Pin 11)	t_S	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE						
Power Supply Voltage Range @ T_A = 25°C						
Positive Supply Voltage		V_{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage		V_{EER}	−5.5	−6.0	−7.0	V
Positive Supply Current (V_{CC} = +5.25 V)	7-13	I_{CC}	–	35	45	mA
Negative Supply Current (V_{EE} = −7.0 V)	7-13	I_{EE}	–	30	45	mA
Channel Select Input Voltage — Low Logic State		$V_{IL(CS)}$	–	–	0.8	V
Channel Select Input Voltage — High Logic State		$V_{IH(CS)}$	2.0	–	–	V
Channel Select Input Current — Low Logic State ($V_{IL(CS)}$ = 0, V_{CC} = 5.25 V)	6	$I_{IL(CS)}$	–	–	−100	µA
Channel Select Input Current — High Logic State ($V_{IH(CS)}$ = V_{CC} = 5.25 V)	6	$I_{IH(CS)}$	–	–	10	µA
GAIN AMPLIFIER SECTION						
Voltage Gain (Unbalanced @ Max Gain) (e_i = 100 mV_{p-p}, f = 1.0 kHz	1, 14	A_V	6.5	7.5	8.5	V/V
Voltage Gain (Unbalanced @ Min Gain) ($V_{I(EGC)}$ = V_{CC}, e_i = 800 mV_{p-p})	1, 14	A_{VS}	–	0.05	0.1	V/V
Operating EGC Current (V_{EGC} = 0 to +5.25 V)	1, 15	$I_I(EGC)$	–	–	6.0	mA
Maximum Differential Input Voltage (T_A = 25°C)		V_{IDR}	0.8	–	–	Vpp
Common Mode Rejection Ratio ($V_{I(EGC)}$ = 0, V_{CM} = 1.0 Vpp, f = 100 kHz, T_A = 25°C)	3	CMRR	40	80	–	dB
Bandwidth (−3.0 dB, T_A = 25°C)	1	BW	–	15	–	MHz
Input Resistance		r_i	30	60	–	kΩ
Channel Isolation (f = 100 kHz, e_i = 800 mV_{p-p})	2, 16		40	60	–	dB
Input Bias Current	4	I_{IB}	–	5.0	15	µA
Input Common Mode Voltage Range		V_{ICR}	±1.0	±1.5	–	V
Output Resistance (Pin 11) (T_A = 25°C)		r_o	–	15	30	Ohms
Output Sink Current (Pin 11)	5	I_{OS-}	1.2	2.1	–	mA
Output Voltage Swing (Pin 11) (f = 1.0 kHz, e_i = 800 mV_{p-p})	1	V_{OR}	2.25	3.0	–	Vpp
Output Offset Voltage (T_A = 25°C)		V_{OO}	–	±400	–	mV

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted) (Continued)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Timing Distortion (I = 1.0 mA, A = 1.5 Vpp, f = 100 kHz, T_A = 25°C)	12		–	1.0	3.0	%
Zero Cross Detector – High Level Output Current (V_{OH} = 5.5 V)	8	$I_{OH(ZCD)}$	–	–	150	µA
Zero Cross Detector – Low Level Output (I_{OL} = 8.0 mA)	9	$V_{OL(ZCD)}$	–	–	0.50	V
Differentiator Output Sink Current (Pins 12 and 13)	5	$I_{O(D)-}$	1.0	1.4	–	mA
Differentiator Output Resistance (Unbalanced) (T_A = 25°C)		$r_{o(D)}$	–	20	–	Ohms
THRESHOLD AMPLIFIER SECTION						
Differential Voltage Gain (e_i = 200 mV)		A_{VD}	4.25	5.0	5.75	V/V
Maximum Differential Input Voltage Without Distortion (T_A = 25°C)		$V_{IDR(T)}$	–	–	400	mVpp
Maximum Differential Input Voltage Before Timing Shift (T_A = 25°C)		$V_{IDR(T)}$	–	–	1.4	Vpp
Maximum Threshold Voltage (Linear Operation)		$V_{IR(T)}$	–	–	−1.0	V
Threshold Voltage Required to Disable Threshold Comparators ($V_{\overline{TD}}$ > 2.7 V, T_A = 25°C)		$V_{I(T)}$	–	−2.0	−2.5	V
Bandwidth (−3.0 dB, T_A = 25°C)		BW	–	15	–	MHz
Input Resistance		$r_{i(INT)}$	25	50	–	kΩ
Threshold Amplifier Bias Current	4	$I_{IB(T)}$	–	5.0	15	µA
Channel Isolation Ratio (f = 100 kHz)	2		40	60	–	dB
Threshold Detector Output Voltage – Low Logic State (I_{OL} = 8.0 mA, Pin 17)	10	$V_{OL(T)}$	–	–	0.50	V
Threshold Detector Output Current – High Logic State (V_{OH} = 5.5 V, Pin 17)	11	$I_{OL(T)}$	–	–	150	µA
Threshold Voltage Input Current (Pin 16)		I_{THC}	–	25	50	µA

DESCRIPTION OF FUNCTION

Input Multiplex – Input multiplexing allows logic-controlled (TTL compatible) selection of either of a pair of differential gain stages. Two separate tracks or one track processed through different filter networks for different recording formats can be selected (e.g., Phase Encoded/NRZI, Group-Coded/PE).

Gain Stage – The gain stage is controlled by Electronic Gain Control (EGC) and differential outputs are provided for the active differentiator and a single output is available for the threshold function. The EGC range is from essentially zero to 7.5 (unbalanced).

Active Differentiation – Active differentiation requires minimum external passive component count. The procedure for selecting component values insures linear operation and optimum zero-crossing detector performance for excellent noise rejection.

Zero Crossing Detector (ZCD) – The zero-crossing detector generates an output transition corresponding to the peak of the incoming signal to the MC3468. Careful attention has been paid to avoid timing distortion between the outputs of the active differentiator and the inputs of the zero crossing comparator.The output is open collector Schottky TTL.

Threshold Amplifier and Detector – The gain stage output is ac coupled or differentiated into the Threshold Amplifier multiplexer. This allows logic-controlled (TTL compatible) selection of either of a pair of single-ended to differential gain stages. Thus, the possibility of selecting between a differentiated or straight capacitive coupled signal for thresholding. The select line is the same as for the Gain Stage multiplexing. The unbalanced gain of the threshold amplifier is 5. An inverting input is available for balancing the input signal to minimize the effects of offset current. The differential outputs of the threshold amplifier are compared to an external threshold in the threshold comparators. An output signal is provided whenever the signal exceeds the threshold setting in the positive or negative direction. The output is open collector Schottky TTL.

The versatility of the MC3468 facilitates the design of dual mode (NRZI/PE, Group/PE) tape drives with the ability of dynamically switch gain, active differentiator components, and thresholds for different recording speeds or interchanged tapes.

Note: For proper operation a dc path must be provided for all inputs of all amplifiers.

MC3468 BLOCK SCHEMATIC

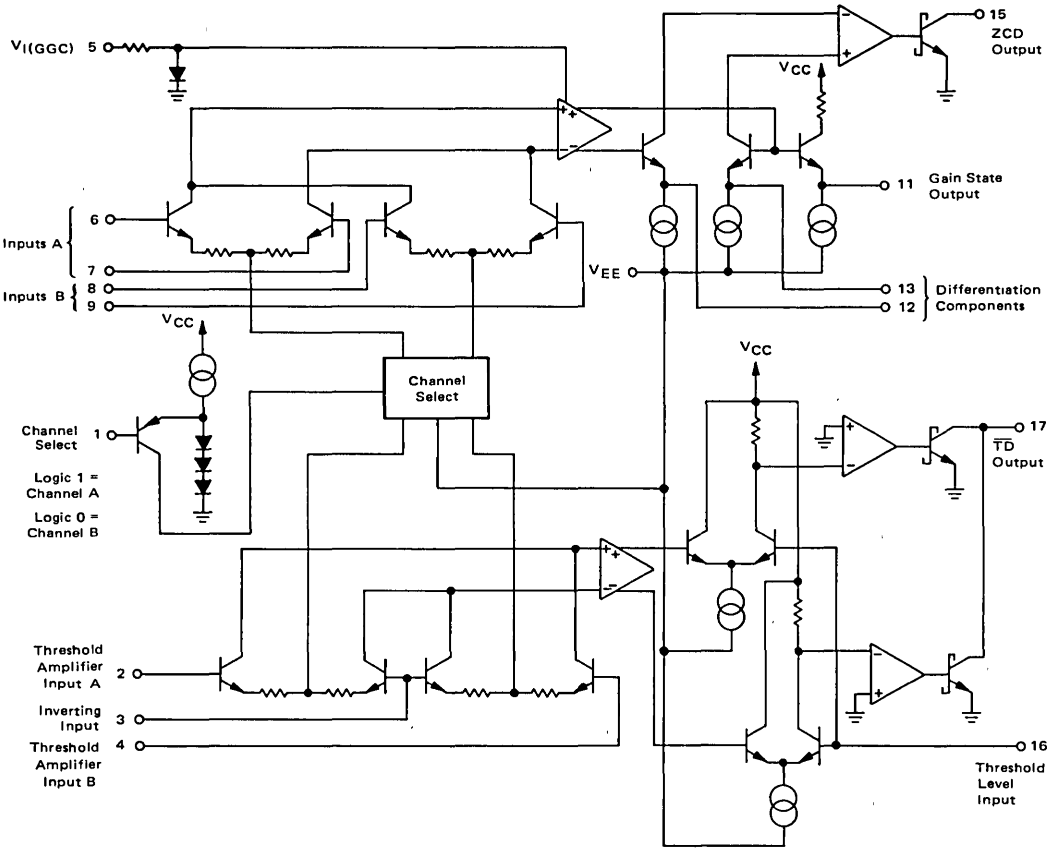


FIGURE 1 – VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING
(A Input Shown)

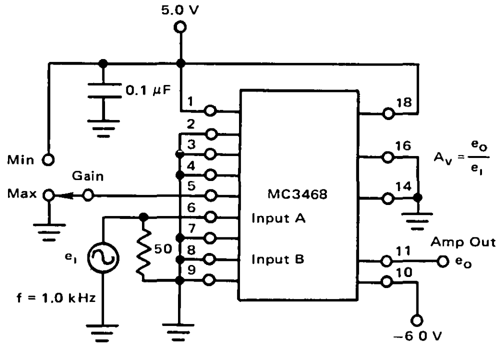
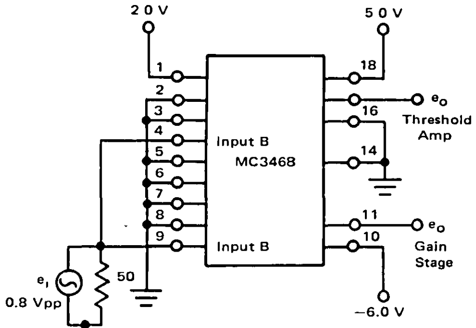
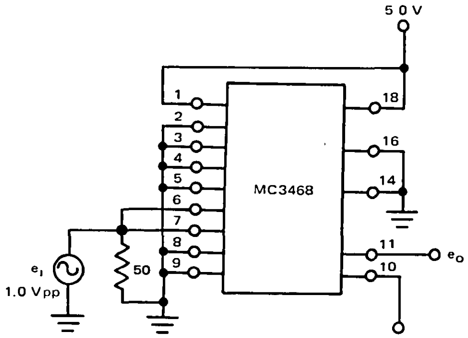


FIGURE 2 – CHANNEL ISOLATION RATIO
(B Inputs Shown)



$$\mathrm{CIR} = 20\log\frac{e_O}{A_V\,e_I} = 20\log\frac{e_O}{7\,5\,e_I}$$

FIGURE 3 – COMMON MODE REJECTION RATIO (CMRR)



$$\mathrm{CMRR} = 20\log\frac{e_O}{A_V\,e_I} = 20\log\frac{e_O}{7\,5\,e_I}$$

FIGURE 4 – INPUT BIAS CURRENT TEST CIRCUIT

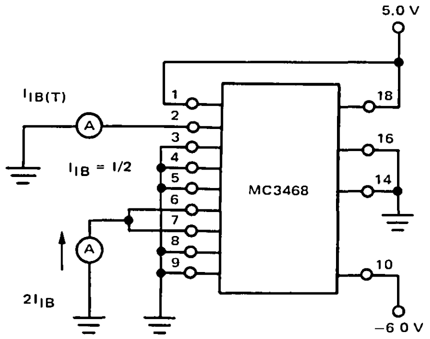


FIGURE 5 – AMPLIFIER OUTPUT AND DIFFERENTIATOR OUTPUT SINK CURRENT TEST CIRCUIT

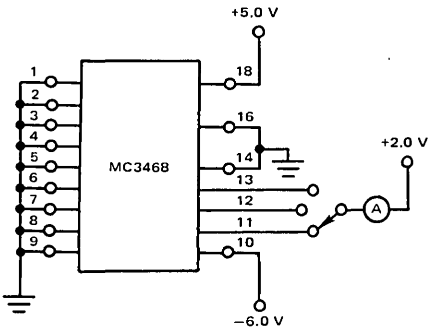


FIGURE 6 – CHANNEL SELECT INPUT CURRENT TEST CIRCUIT

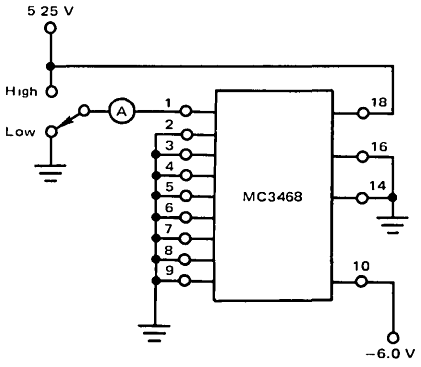


FIGURE 7 – POSITIVE AND NEGATIVE SUPPLY CURRENT TEST CIRCUIT

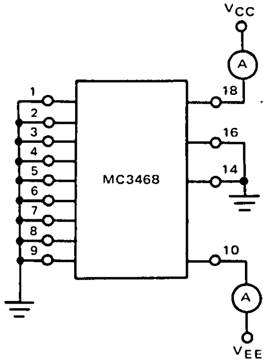


FIGURE 8 – ZERO CROSS DETECTOR OUTPUT CURRENT HIGH LOGIC STATE TEST CIRCUIT

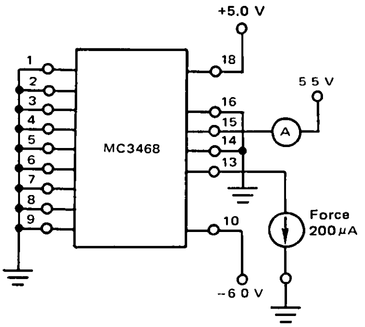


FIGURE 9 – ZERO CROSSING DETECTOR OUTPUT VOLTAGE LOW LOGIC STATE TEST CIRCUIT

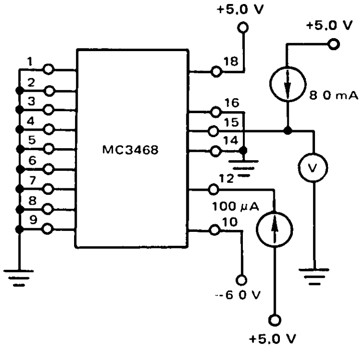


FIGURE 10 – THRESHOLD DETECTOR OUTPUT VOLTAGE – LOW LOGIC STATE TEST CIRCUIT

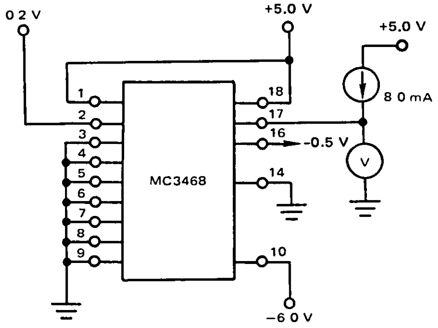


FIGURE 11 – THRESHOLD DETECTOR OUTPUT CURRENT – HIGH LOGIC STATE TEST CIRCUIT

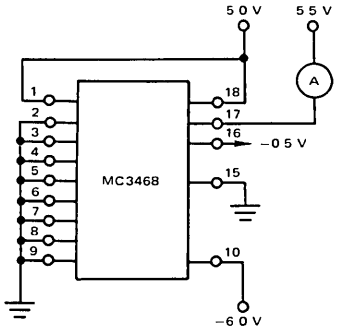
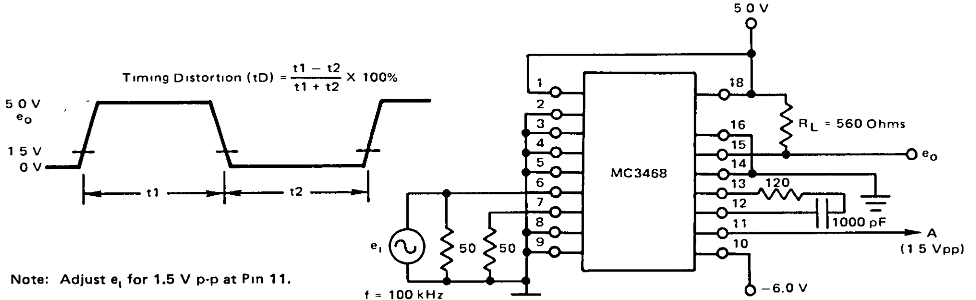


FIGURE 12 – TIMING DISTORTION $T_A = 25^oC$



$$\text{Timing Distortion (tD)} = \frac{t1 - t2}{t1 + t2} \times 100\%$$

Note: Adjust e_i for 1.5 V p-p at Pin 11.

$$C = \frac{1\ 0\ \text{mA}}{(1\ 5\ \text{Vpp})\ 2\pi\ 100\ \text{kHz}} - 1000\ \text{pF}$$

$$R = \frac{1}{2\pi\ (1\ \text{MHz})\ 1000\ \text{pF}} - 40\ \Omega \simeq 120\ \text{Ohms}$$

TYPICAL PERFORMANCE CURVES

FIGURE 13 – NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

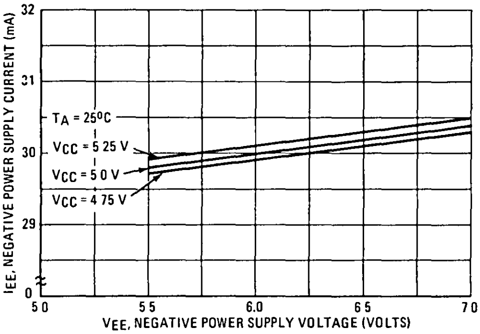


FIGURE 14 – NORMALIZED VOLTAGE GAIN versus EGC INPUT VOLTAGE

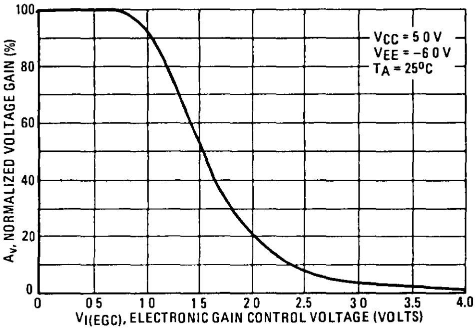


FIGURE 15 – ELECTRONIC GAIN CONTROL INPUT CURRENT versus VOLTAGE

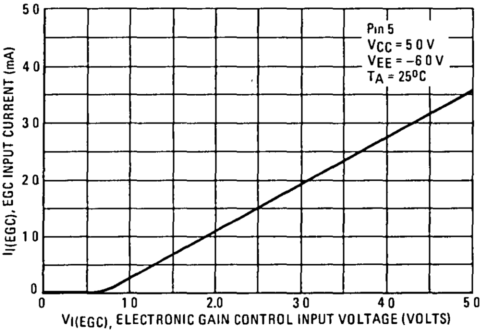


FIGURE 16 – CHANNEL ISOLATION RATIO versus FREQUENCY

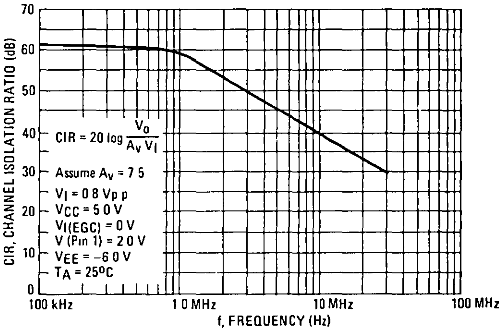
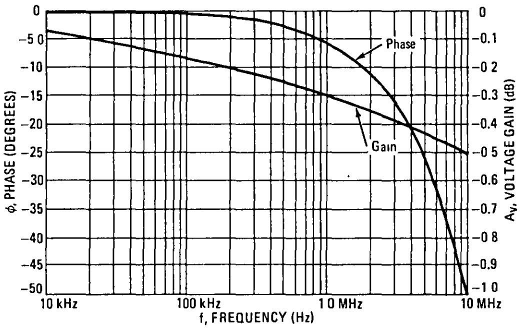


FIGURE 17 – GAIN AND PHASE versus FREQUENCY FROM Pins 6, 7 to Pins 12, 13



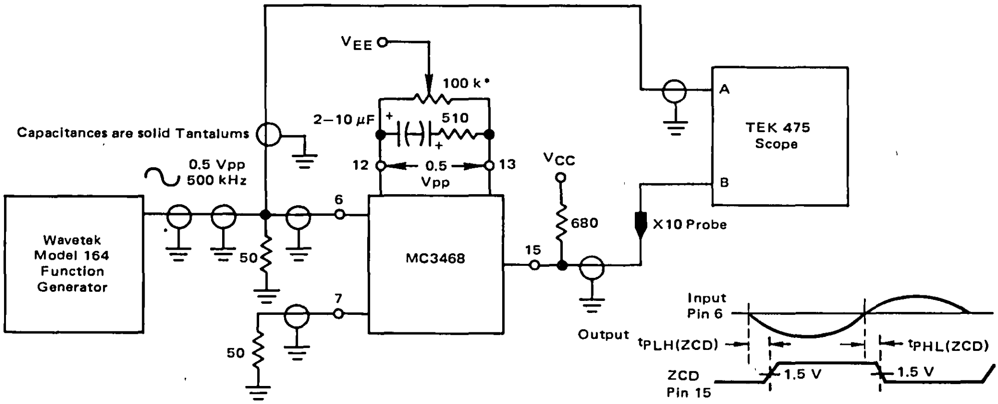
SYSTEM PARAMETERS

The following system parameters are characteristic of not only the device but external component values and circuit layout. Detailed test circuits and measured parameters are provided only as a guide to expected system performance. These parameters are not readily measureable on a production volume basis.

FIGURE 18 – TEST CIRCUIT FOR MEASURING PROPAGATION DELAYS

From Gain Stage Input to Zero Crossing Detector Output

(Pin 6 to Pin 15) (Subtract 8 ns from measurement for probe and cable delays)



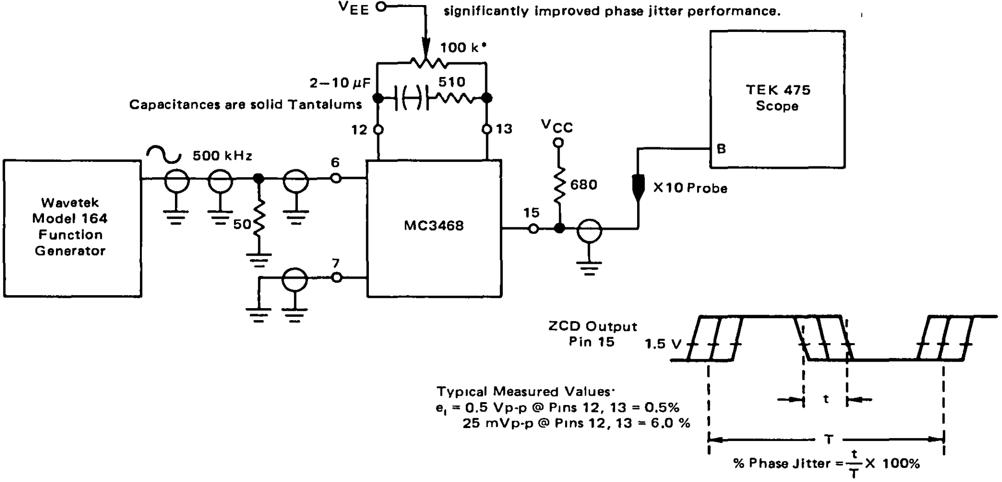
Note: Symmetry is adjusted @ 50 kHz and 50 mVpp

*Adjust 100 k per Figure 21, Part II

Typical Measured Values $t_{PLH(ZCD)} = 40$ ns

$t_{PHL(ZCD)} = 50$ ns

FIGURE 19 – TEST SETUP FOR MEASURING PHASE JITTER



Note: Use of a series inductor in the differentiator network significantly improved phase jitter performance.

Typical Measured Values·

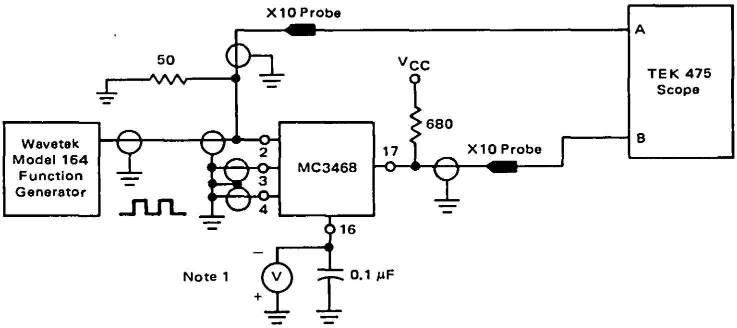
e_i = 0.5 Vp-p @ Pins 12, 13 = 0.5%

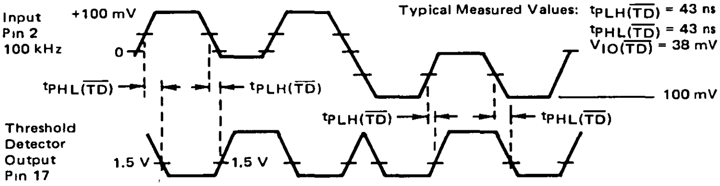
25 mVp-p @ Pins 12, 13 = 6.0 %

$$\% \text{ Phase Jitter} = \frac{t}{T} \times 100\%$$

Note: The jitter window, t, is defined as the 3 σ points on a Gussion curve.

FIGURE 20 – TEST SETUP FOR THRESHOLD AMPLIFIER DELAY AND THRESHOLD COMPARATOR EQUIVALENT OFFSET MEASUREMENTS

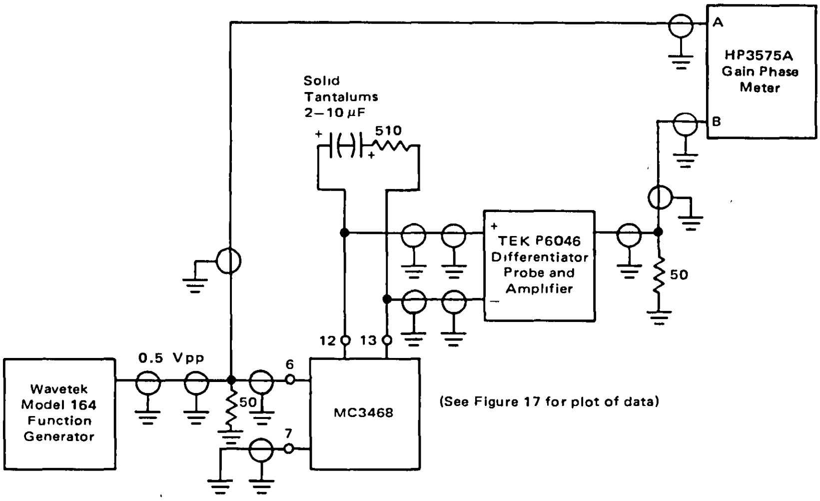




Notes:
1. For Delay measurements, V is fixed at −250 mV; for equivalent comparator offset voltage measurements, V is adjusted until Pin 17 goes low. The voltage, V, is the equivalent offset, $V_{IO(\overline{TD})}$.
2. Some compensation is possible using a resistor from Pin 3 to ground.

FIGURE 21 – TEST SETUP FOR GAIN AND PHASE versus FREQUENCY (5 kHz to 1 MHz) FROM INPUT TO DIFFERENTIATOR (Pin 6, 7 to Pin 12, 13)

Actual Test Measurements (Calibrate Instrumentation for Phase Compensation)



(See Figure 17 for plot of data)

DESIGN SUGGESTIONS

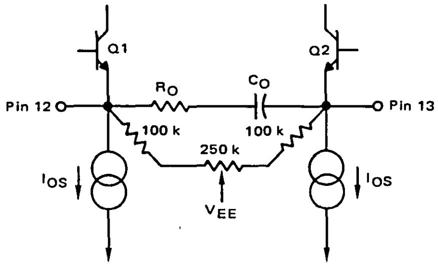
Gain Stage Bias Current

One must consider supplying 15 μA of bias current to the Gain Stage when designing a filter network. A good design value for the equivalent resistance from each input leg to ground is 5 kΩ.

Adjusting Peak Shift to Zero (See Figure 22)

The worst peak shift observed on the ZCD output occurs for the smallest slew rate provided by the Active Differentiator at the ZCD inputs. In Turn, the Active Differentiator produces the smallest slew rate when the gain-bandwidth product applied at its inputs is the smallest. Current source, resistors, and diode imbalances will exhibit the maximum peak shift under this condition. Using the resistor network shown, these imbalances are adjusted out for the worst case condition.

FIGURE 22 – PEAK SHIFT NETWORK



Note: The 100 kΩ resistors should be close to the IC to suppress noise.

MC3468 APPLICATIONS INFORMATION

MC3468 For NRZI Encoded Magnetic Tape

NRZI Encoding was one of the first popular recording formats and is formalized as an American National Standard for the purpose of facilitating the interchange of magnetic tapes. Although the Phase-Encoded format is now more widely accepted than NRZI, vast libraries of NRZI tapes still exist. Computers will be reading these tapes for years to come, and in some cases, re-writing them in phase-encoded format. Thus, the ability of the tape drive electronics to read both NRZI and PE tapes is a feature often sought in new designs.

For NRZI recording, the magnetic surface of the tape is magnetized to saturation in one direction or the other each time a logical "1" is to be recorded. The magnetization remains unchanged for a logical "0". The resulting signal from the read head for a typical NRZI data stream is shown in Figure 23. The NRZI data stream consists of a continuum of Fourier components up to a maximum frequency of $5f_H$, where f_H is numerically equal to one-half the maximum flux changes per second (FCPS). For long strings of zeroes, the lowest Fourier component could theoretically be near dc, but on a typical tape a long interval with no "1's" is not allowed. Consequently, most of the energy in the pulse train is around f_H and its harmonics (up to the fifth). A suitable corner frequency for ac coupling from the preamplifier is 60 Hz, although for high speed systems it could be considerably higher (1/10 fH). The -3 dB frequency of a low pass filter is usually placed at a frequency greater than f_H. In most systems, this low pass filter must do more than provide a roll-off for high-frequency transients. It also equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated either as part of the ac coupling between the preamplifier and amplifier or as part of the differentiation network.

The American National Standard specifies that NRZI be recorded at 800 BPI (Bits Per Inch) on open reel magnetic tape. Typical read/write tape speeds range from 12.5 to 300 IPS (Inches Per Second). Examples 1 and 4 show MC3468 NRZI designs.

MC3468 For Phase-Encoded (PE) Magnetic Tape

Of the numerous methods for encoding digital data on magnetic tape, phase encoding is currently most popular. As shown in Figure 23, data is represented by transitions occurring in the middle of a "data cell". A low-to-high flux transition (toward the magnetization level representing erased tape) is defined as a logical "one" and a high-to-low transition is defined as a logical "zero". For consecutive "one's" or "zero's" phase transitions are introduced as needed at the "data cell" borders. Phase transitions are not required when the encoded data consists of "one-zero" patterns.

The read head signal resulting from mixed data streams consists of two fundamental frequencies, f_H and f_L which represent most of the harmonic content (with some energy at harmonics up to the fifth). These are numerically equal to $\frac{\text{FCPI}}{2} \times \text{IPS}$ and $\frac{\text{FCPI} \times \text{IPS}}{4}$ (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). In high-speed, low-level systems, the amplitude of these read head signals is only a few millivolts and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. In most systems, the bandpass filter must do more than filter out noise. The low-pass portion also equalizes the read amplifier chain and differentiation network for a linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

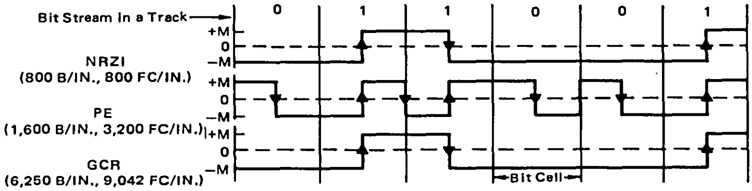
The American National Standard specifies that PE data be recorded at 1600 BPI (Bits Per Inch) on open-reel magnetic tape. Typical read/write tape speeds range from 6.25 to 200 IPS (Inches Per Second). Cartridges use 1600 BPI and have tape speeds of 30 IPS for read/write. Examples 2, 3, and 4 show MC3468 designs for PE systems.

MC3468 For Group Code Recorded (GCR) Magnetic Tape

Basically, Group-Coded Recording (GCR) is a high density recording scheme which uses the NRZI convention for "1's" and "0's", but adds the restriction that flux changes occur at least once in every three bit cells (Figure 23). The read head signal resulting from mixed data streams consists primarily of Fourier components from f_L to $3f_L = f_H$ and their harmonics up to the fifth. The frequencies f_L and f_H are numerically equal to $\frac{\text{FCPI} \times \text{IPS}}{2}$ and $\frac{\text{FCPI} \times \text{IPS}}{6}$, respectively (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). The amplitude of the read head signals is only a few millivolts or less and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. The bandpass filter must do more than filter out noise. The low pass portion equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

The proposed American National Standard specifies that GCR data be recorded at 9042 FCPI (Flux Changes Per Inch). Because of the data format, the usable data density is 6250 BPI rather than 9042 BPI. The "6250 BPI" is a throughput specification and should not be used in read amplifier calculations. The original GCR concept was intended for high speed drives (200 IPS). However, it is also being applied to lower speed (125 IPS) systems. Examples 5 and 6 illustrate the use of the MC3468 in GCR systems.

FIGURE 23 – MOST POPULAR MAGNETIC TAPE RECORDING FORMATS



CIRCUIT OPERATION

(See Figure 24 for component wiring and Figures 25 and 26 for Timing Diagrams)

The operation of the MC3468 is similar for NRZI, PE, and GCR data formats. The preamplifier and filtered signal is applied differentially to either Channel A or B Gain Stages. The Gain Stage output differentially feeds an Active Differentiator and a single-ended output is available for straight capacitive or differentiated (active or passive) coupling into either Channel A or B inputs to the Threshold Amplifier.

For the circuit configuration shown, the Active Differentiator output leads the input by almost 90°. The Active Differentiator output is applied to a Zero-Crossing Detector, which goes low for positive levels and high for negative levels, changing state at the zero crossings. The Threshold Circuit amplifies the Gain Stage output and compares positive and negative signals to a threshold level. When the level is exceeded, the $\overline{TD}$ output is low. From the waveforms, it is seen that the ZCD output makes a transition approximately in the middle of the period when $\overline{TD}$ is low. Wiring ZCD "anded" with TD to the set input and $\overline{ZCD}$ "anded" with TD to the "reset" input of the R-S type flip-flop reconstructs the data stream encoded on the tape. This circuit works for zero clip (zero threshold) operation, but has the disadvantage that timing distortion results from capacitive loading. Digital circuits for reconstructing the data stream which utilize pipe-line delays to overcome capacitive loading timing distortion are shown in Figure 27.

FIGURE 24 – TYPICAL MC3468 COMPONENT HOOKUP

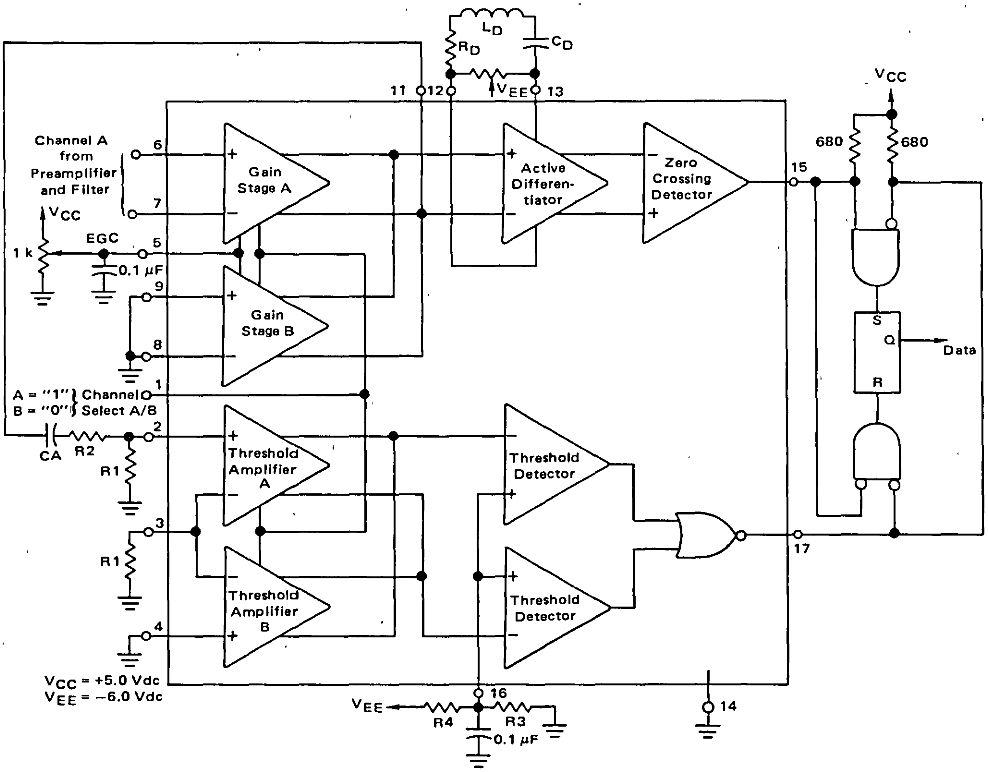


FIGURE 25 – WAVEFORMS SHOWING MC3468 OPERATION FOR NRZI DATA

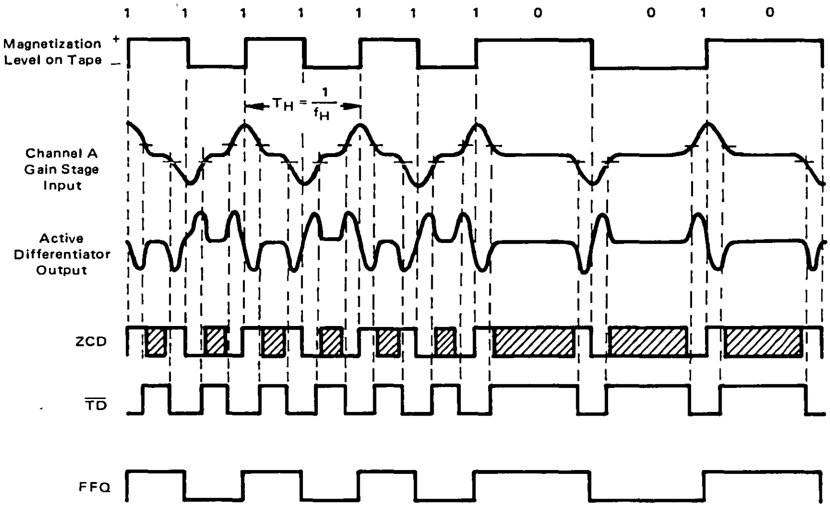


FIGURE 26 – TIMING DIAGRAM WAVEFORMS SHOWING MC3468 OPERATION FOR PHASE-ENCODED DATA

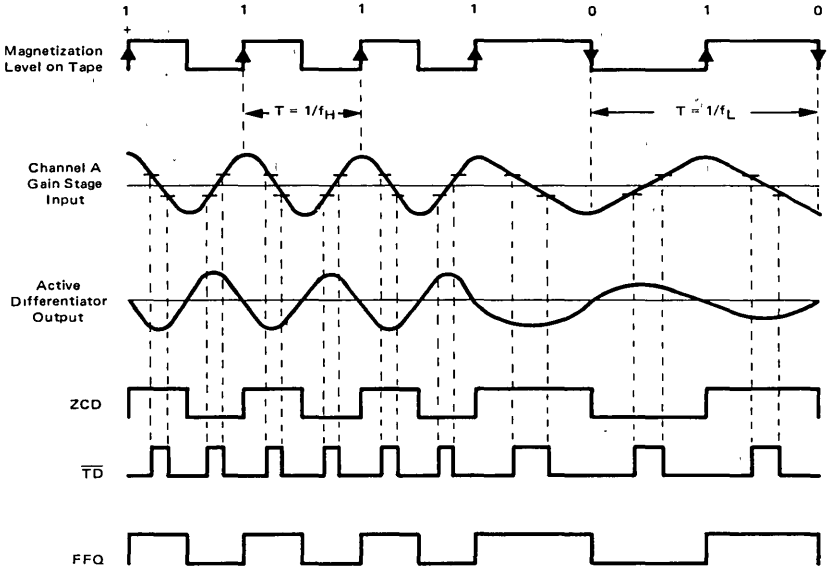
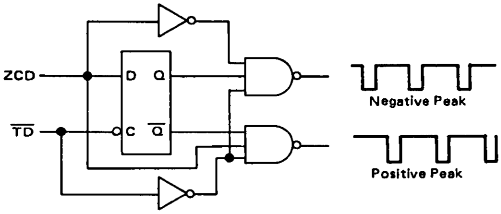
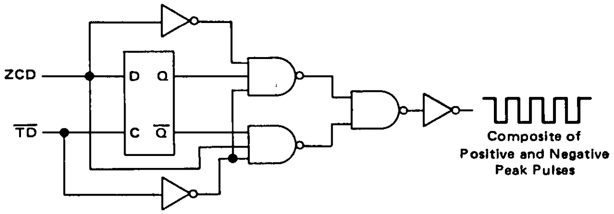


FIGURE 27 — OTHER DIGITAL CIRCUITS FOR RECONSTRUCTING DATA STREAMS FROM THE MC3468

1) Dual Output Circuit (Pipeline Delay for Negative Edge Must Be the Same for Both Outputs)



2). Single Output Circuit (Operation Independent of Capacitive Loading Effects on Delays)



Group Delay Distortion

The ultimate purpose of the magnetic read amplifier chain in Figure 28 is to produce a digital signal with transitions corresponding to the peaks of a read head signal. Because the active and passive elements in the chain exhibit phase characteristics, there will be a "pipe-line" delay between peaks at the read head and the digital output from the zero-crossing detector. Variations in this delay with frequency or amplitudes cause timing distortion which translates directly into increasing error rates. The primary consideration in the read chain implementation is to equalize the read chain for almost flat delay over the frequencies and amplitudes of required operation. Figure 28 depicts one of several possible read chain configurations which can be equalized for best-flat time delay performance.

The determination of the component values is relatively straight forward provided the active elements have negligible phase characteristics in the frequency range of operation. Below 1 MHz, the MC3467/MC3468 read chain active elements have negligible phase characteristics. Although phase effects start showing above 1 MHz, phase versus frequency is linear (constant time delay).

Other read chain configurations have a band-pass filter between the preamplifier and Gain Stage. It is possible to move some of the poles of the filter into the active differentiator. The technique suggested in Figure 28 transfers poles into the active differentiator to minimize component count. The insertion loss of the technique is also less than an equalization filter ahead of the READ amplifier.

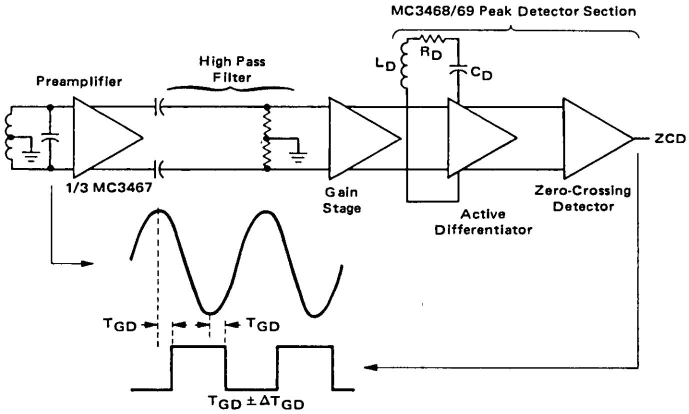


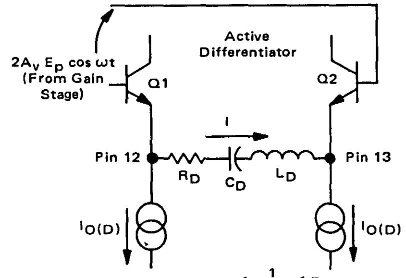
FIGURE 28 — GROUP DELAY DISTORTION THROUGH READ CHAIN

Determining R_D, C_D, and L_D For the Active Differentiator

For the equalized read chain shown in Figure 28, C_D, R_D and L_D are determined respectively in that order. The phase characteristics of the active elements are assumed to be negligible.

An active differentiator is formed by R_D, C_D and L_D coupling the emitters of a differential amplifier having current sources I_{OD} in each leg. If a differential voltage A_VE_p cos ωt is applied to the Active Differentiator, the resulting current through R_D and C_D is:

$$I = \frac{2A_VE_p}{\sqrt{R_T{}^2 + \left(\frac{1}{\omega C_D} + \omega L_D\right)^2}} \cos\left\{\omega t - \arctan\left(\frac{-1/\omega C_D}{R_T}\right)\right\}$$



when $\omega L_D < \frac{1}{\omega C_D} < R_T$

$I \cong 2A_V\ E_p\ C_D\ \omega \sin \omega t$

where $2A_VE_p$ is the product of the differential input to the Gain Stage E_p and its unbalanced gain, A_V.
where R_T is the total of R_D and the output impedances of Q1 and Q2. The combined output impedances of Q1 and Q2 is 40 Ohms.

This condition is approximated for $\frac{1}{R_TC_D} = \omega_C = 3\omega_H$ (where ω_H is the maximum applied frequency of appreciable Fourier content).

The peak value of I (i.e., $2A_V\ E_p\ C_D\ \omega$) is important. As I approaches $I_{O(D)}$, the transistor Q2 turns off and the waveform at Pin 12 distorts. The circuit no longer behaves as a differentiator and peak distortion results.

For best zero crossing detector performance, it is essential that I be maximized. A design value of I which results in good noise performance and minimum peak shift is 900 microamperes.[1]

$$I = 2A_V\ E_p\ C_D\ \omega = 900 \times 10^{-6}$$

Rearranging the equation for I,

$$\boxed{C_D = \frac{900 \times 10^{-6}}{2A_V\ E_p\ \omega}}$$

Also, solving $\omega_C = \frac{1}{R_TC_D}$ for R_T,

$$R_T = \frac{1}{\omega_C C_D}$$

Assuming the output impedance of Q1 and Q2 combined is 40 Ohms,

$$\boxed{R_D = \frac{1}{\omega_C C_D} - 40}$$

where $\omega_C = 3\ \omega_H$.

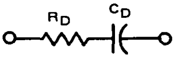
As shown in Table 1, the addition of an inductor, L_D, significantly improves phase linearity versus frequency as well as providing a roll off for high frequency noise. This optimum solution requires the following relationships:

$$\frac{2}{R_TC_D} = \frac{R_T}{L_D}$$

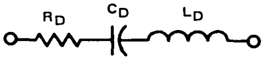
rearranging,

$$\boxed{L_D = \frac{R_T{}^2\ C_D}{2}}$$

TABLE 1 – PHASE LINEARITY (CONSTANT TIME DELAY) PERFORMANCE FOR RC versus RLC ACTIVE DIFFERENTIATOR NETWORK



$\omega_C = \frac{1}{R_D\ C_D} = 3\omega_H$



$\omega_n = \frac{\sqrt{2}}{R_D\ C_D} = \frac{1}{\sqrt{LC}}$

$\frac{\omega}{\omega_C}$	θ	$\Delta\theta$	$\frac{\omega}{\omega_n}$	θ	$\Delta\theta$
1.0	+45.00		1.0	0	
0.9	+48.01	+3.01	0.9	+8.49	+8.49
0.8	+51.34	+3.33	0.8	+17.65	+9.16
0.7	+55.01	+3.67	0.7	+27.26	+9.61
0.6	+59.04	+4.03	0.6	+37.03	+9.77
0.5	+63.43	+4.39	0.5	+46.69	+9.66
0.4	+68.20	+4.77	0.4	+56.04	+9.35
0.3	+73.30	+5.10	0.3	+65.00	+8.96
0.2	+78.69	+5.39	0.2	+73.58	+8.58
0.1	+84.29	+5.60	0.1	+81.87	+8.29

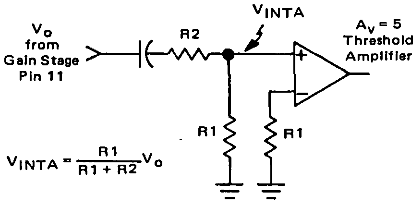
[1] For optimum zero-crossing detector performance, dI/dt should be as large as possible at zero-crossing.

Motorola guarantees a minimum $I_{O(D)}$ of 1.0 mA.

Threshold Considerations

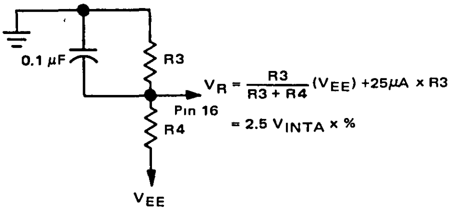
The threshold circuitry is used in read after write systems to insure that good data was written, to set up gain during an ID burst, and sometimes to indicate a minimum signal voltage for invalid data. Optimum thresholding requires a large swing at the threshold amplifier inputs. A good design value for V_{INTA} is 1.0 Vp-p, and should not exceed 1.4 Vp-p. If it does, a timing shift results. Internal clipping is provided for all signals greater than 400 mVp-p. The distortion resulting from clipping has no effect on thresholding because only peaks are clipped.

As shown in Figure 24, the Gain Stage output at Pin 11 is ac coupled to the threshold amplifier so that voltage offsets do not influence thresholding. An attenuator, R1/R2, is often required in the ac coupling networks because the gain stage output is between 1.6 Vp-p and 2.4 Vp-p for optimum zero-crossing-detector performance.



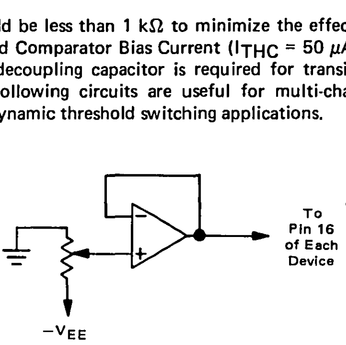
The magnitude of R1 should be less than 5 kΩ to minimize the effects of Threshold Amplifier Bias current (I_{THA} = 15 μA). Also, R1 + R2 must be greater than 3 kΩ because the minimum output sink current (I_{OS}) of the Gain Stage is 1.5 mA. A resistance equal to R1 should be wired to ground from the − leg of the Threshold Amplifier (minimize offset bias current effects).

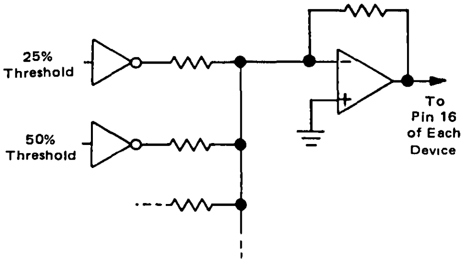
Note that only the selected amplifier input contributes to bias current. Each output of the Threshold Amplifier is 5 V_{INTA}, and is applied to its resepctive Threshold comparator. Each comparator sees 2.5 V_{INTA}. Thresholding is based on a percentage of the nominal voltage applied to the comparators, 2.5 V_{INTA}. Both positive and negative references are derived from V_{EE} as follows:



R3 should be less than 1 kΩ to minimize the effects of Threshold Comparator Bias Current (I_{THC} = 50 μA). A 0.1 μF decoupling capacitor is required for transients.

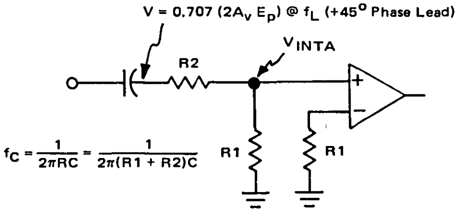
The following circuits are useful for multi-channel and/or dynamic threshold switching applications.





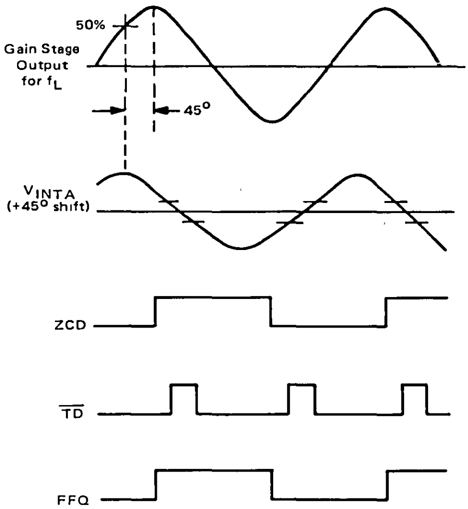
Base Line Shift in PE Systems

In phase-encoded recording, the read signal may not make symmetrical transitions about the zero bias level. A lower amplitude signal with a low frequency component is often superimposed. Although a highpass filter attenuates some of this component, its frequency is often close to the −3 dB frequency of the filter and may be only −6 dB down from signal amplitudes. This baseline shift has no adverse effects on the performance of the Active Differentiator. However, the Threshold Detector is sensitive to the unequal signal peaks. Signal-to-noise ratio can be improved by performing a passive differentiation into the Threshold Amplifier. With the corner frequency, f_C, placed at f_L, the f_L signal is attenuated −3 dB; the $f_H = 2f_L$ signal is for all practical purposes unattenuated. Figure 29 shows the 45° phase lead introduced by passive differentiation. Note that this technique is not directly applicable to high thresholds because the ZCD transitions fall outside the thresholding window. However, the threshold window can be delayed to overcome this drawback.



The design of the attenuator, R1/R2, follows as described previously. Example 3 shows a typical application of passive differentiation to overcome base-line shift.

FIGURE 29 – RESULTING OPERATION FOR PASSIVE DIFFERENTIATION INTO THRESHOLD AMPLIFIER



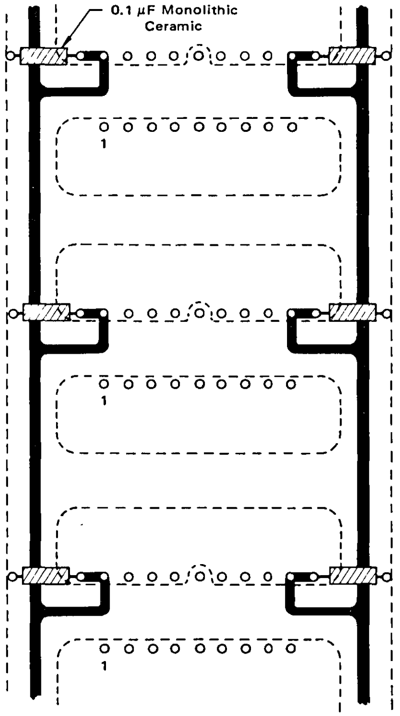
Board Layout and Testing Considerations

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 30.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in 3-dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC, also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 µF capacitors for decoupling power supply transients. One from V_{CC} to ground and one from V_{EE} to ground for each IC package. Keep lead lengths to ¼ inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible. The lead on Pin 15 will radiate and can couple back into the active differentiator. This will result in excessive phase jitter. The tell-tale behavior is a ringing at Pin 11 corresponding to the transitions at Pin 15. To overcome this coupling problem, keep the lead on Pin 15 short and isolated from the other Input/Output lines to the MC3468. Preferably, put it over or next to a ground plane. For long distance runs, use a twisted pair or coaxial cable.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test set-ups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 30 – POWER AND GROUND DISTRIBUTION FOR MC3468 PRINTED CIRCUIT BOARD LAYOUT



Note: Dotted Lines Outline Ground Plane on Back Side of Printed Circuit Board

EXAMPLES

Example #1 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: NRZI
Recording Density: 800 BPI (800 FCPI)
Tape Speed: 200 IPS
Signal into Gain Stage

$$E_{pp} = 0.3 \text{ to } 0.6 \text{ Vp-p @ 80 kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.6} = A_V = 2.7$$

Set the EGC for a gain of 2.7, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$$R1 + R2 \geqslant 3\ k\Omega \text{ and } R1 \leqslant 5\ k\Omega \text{ (See text)}$$

These constraints are satisfied when R1 = 4.7 kΩ and R2 = 3 kΩ. This is an optimum solution for a minimum coupling capacitor value.

Now consider the minimum voltage applied to the Threshold Amplifier

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 2.7 \times 0.3 = 0.5 \text{ Vp-p,}$$

The threshold comparator reference voltage, V_R, is set at 25% of $2.5V_{INTA(MIN)}$

$$V_R = 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$$R3 \leqslant 1\ k\Omega \text{ (See text)}$$

Let R3 = 470 Ω; then R4 ≅ 10 kΩ

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_V\, E_p\, \omega} = \frac{900 \times 10^{-6}}{A_V\, E_{pp}\, \omega}$$

$$= \frac{900 \times 10^{-6}}{2.7 \times 0\ 6 \times 2\pi \times 80 \times 10^3}$$

$$C_D \cong 1000 \text{ pF}$$

Assume $f_c = 3f$

$$R_D = \frac{1}{\omega_C C_D} - 40 = \frac{1}{2\pi \times 3 \times 80 \times 10^3 \times 10^{-9}} - 40$$

$$R_D = 670 - 40 \cong 600\ \Omega$$

$$L_D = \frac{R_T{}^2\, C_D}{2} = \frac{(670)^2 \times 10^{-9}}{2} = 224\ \mu H$$

Example #2 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Phase-Encoded
Recording Density: 1600 BPI (3200 FCPI)
Tape Speed: 200 IPS
Signal Into Gain Stage

$$E_{pp} = 0.2 \text{ Vp-p @ 320 kHz}$$
$$0.4 \text{ Vp-p @ 160 kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.4} = A_V = 4$$

Set the EGC for a gain of 4, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$$R1 + R2 \geqslant 3\ k\Omega \text{ and } R1 \leqslant 5\ k\Omega \text{ (See text)}$$

These constraints are satisfied when R1 ≅ 4.7 kΩ and R2 ≅ 3 kΩ. This is an optimum solution for a minimum coupling capacitor value. Now consider the minimum voltage applied to the Threshold Amplifier.

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 4 \times 0.2 = 0.5 \text{ Vp-p}$$

The threshold comparator reference voltage, V_R, is set at 25% of 2.5 $V_{INTA(MIN)}$

$$V_R = 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$$R3 \leqslant 1\ k\Omega \text{ (See text)}$$

Let R3 = 470 Ω; then R4 ≅ 10 kΩ

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_V\, E_{pp}} = \frac{900 \times 10^{-6}}{A_V\, E_p} = \frac{900 \times 10^{-6}}{4 \times 0.4 \times 2\pi \times 160 \times 10^3}$$

$$C_D \cong 560 \text{ pF}$$

Assume $f_C = 3f_H$

$$R_D = \frac{1}{W_C C_D} - 40$$

$$= \frac{1}{2\pi \times 3 \times 320 \times 10^3 \times 5.6 \times 10^{-10}} - 40$$

$$R_D = 295 \text{ ohms} - 40 \cong 250\ \Omega$$

$$L_D = \frac{R_T{}^2\, C_D}{2} = \frac{(295)^2 \times 560 \times 10^{-12}}{2} = 24\ \mu H$$

Example #3 (See Figure 24 for Component Hookup)

Same as Example #2, but consider base-line shift.

In addition to ac coupling between the Gain Stage and Threshold, a passive differentiation is performed to attenuate the lower frequencies producing base-line shift. This improves signal-to-noise ratio. The corner frequency is chosen at f_L = 160 kHz where the attenuation is 0.707 (−3 dB) and the phase angle is +45°.

$$f_L = \frac{1}{2\pi C\,(R1 + R2)} = 160 \times 10^3$$

For C = 200 pF

$$R1 + R2 \cong 5\ k\Omega$$

$$\text{Now } \frac{R1}{R1 + R2} = \frac{1}{1.6 \times 0.707} = 0.9$$

Let R1 = 4.7 kΩ, then R2 = 470 Ω

Example #4 (See Figure 31 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Dual Mode (Phase-Encoded/NRZI)
Recording Density: 1600 BPI (3200 FCPI) for PE mode and 800 BPI (800 FCPI) for NRZI mode
Tape Speed: 200 IPS
Signal Into Gain Stage

Same as Examples 1 and 2

Threshold: 25% of minimum voltage peaks

NOTE: Consider base-line shift for PE mode.

This tape drive performs either the NRZI or the PE functions of Examples #1 and #3, under control of the SEL A/B line. Using the Gain Stage and Threshold Amplifier Channel A, Channel B inputs, the hook-up for a single track is implemented as shown in Figure 31. Note that an electronic switch is required for Gain switching when the mode is changed. This particular design did not require the threshold voltage to be switched, although in a typical system it probably would be.

It is necessary to electronically switch differentiator components. A low impedance MOSFET switch is shown.

Example #5 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Group Code
Recording Density: 6250 BPI, 9042 FCPI
Tape Speed: 200 IPS
Signal Into Gain Stage

$$E_{pp} = 0.1 \text{ Vp-p @ } 900 \text{ kHz} = f_H$$

$$E_{pp} = 0.3 \text{ Vp-p @ } 300 \text{ kHz} = f_L$$

Considerations for setting Gain Stage EGC, coupling (passive differentiation for base-line shift or straight ac) into the Threshold Amplifier, and Threshold setting are similar to the previous examples. For Group-coded data the EGC setting can be electronically locked during the ID burst in conjunction with Threshold setting. (See Figure 32.)

Values for C_D and R_D

$$C_D = \frac{900 \times 10^{-6}}{2A_V\, E_p\, \omega}$$

$$= \frac{900 \times 10^{-6}}{A_V\, E_{pp}\, \omega} = \frac{900 \times 10^{-6}}{5.3 \times 0.3 \times 2\pi \times 300 \times 10^3}$$

$$C_D \cong 300 \text{ pF}$$

Assume $f_C = 3f_H$

$$R_D = \frac{1}{\omega_C C_D} - 40 = \frac{1}{2\pi \times 3 \times 900 \times 10^3 \times 300 \times 10^{-12}} - 40$$

$$R_D = 200 - 40 = 160 \text{ Ohms}$$

$$L_D = \frac{R_T{}^2\, C_D}{2} = \frac{(200)^2 \times 300 \times 10^{-12}}{2} = 6\ \mu\text{H}$$

Example #6 (See Figure 24 for Component Hookup)

Same as Example #5 except 125 IPS tape speed.

Signal Into Gain Stage

$$E_{pp} = 0.3 \text{ Vp-p @ } 565 \text{ kHz}$$

$$E_{pp} = 0.6 \text{ Vp-p @ } 188 \text{ kHz}$$

$$C_D = 300 \text{ pF},\ R_D = 250\ \Omega$$

$$L_D = 12.6\ \mu\text{H}$$

FIGURE 31 — MC3468 COMPONENT HOOKUP FOR DUAL MODE PE/NRZI EXAMPLE #4

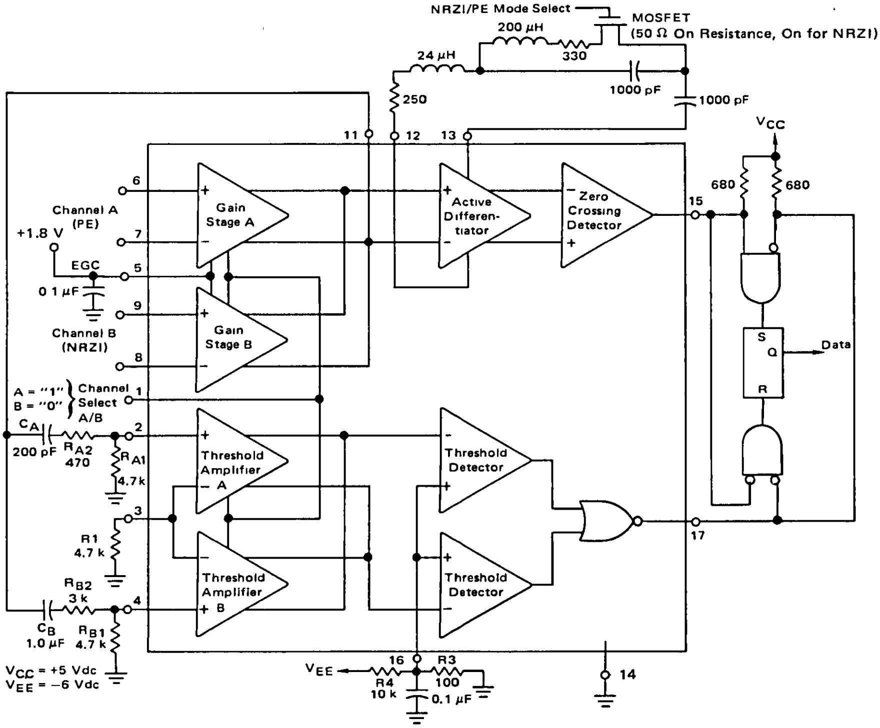
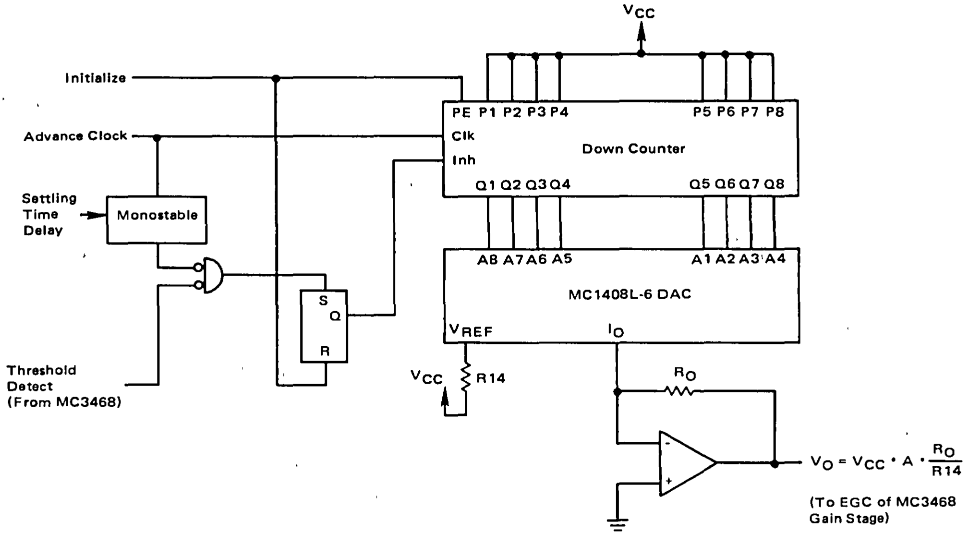


FIGURE 32 — APPLICATIONS CIRCUITS

Digital Attenuator for Setting MC3468 Gain Stage Automatically During ID Burst



MOTOROLA

MC3470

Advance Specifications and Applications Information

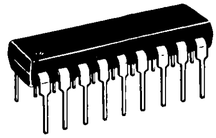
FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 5.0%

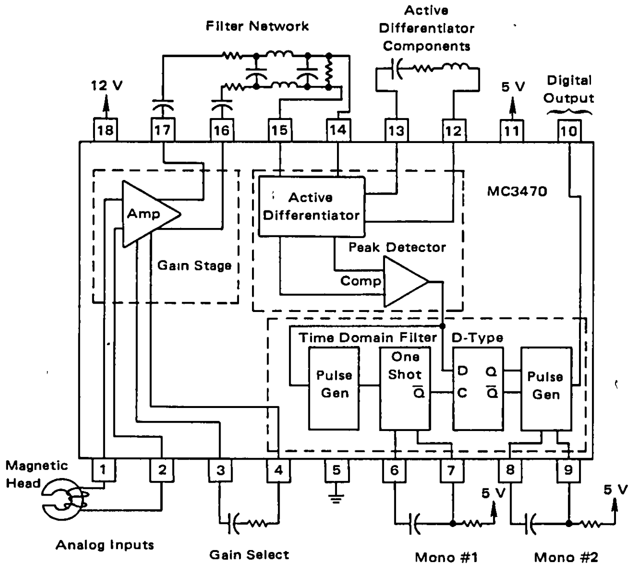
FLOPPY DISK READ AMPLIFIER SYSTEM

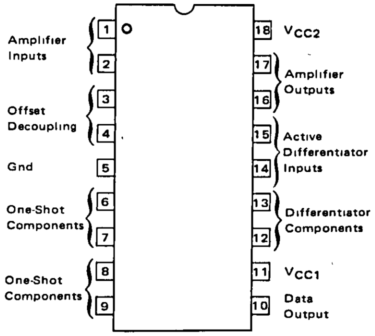
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701-01

TYPICAL APPLICATION





This is advance information and specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Note 1)(T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V_{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V_I	-0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V_O	-0.2 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package	T_J	150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provices conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
GAIN AMPLIFIER SECTION						
Differential Voltage Gain (f = 200 kHz, V_{ID} = 5.0 mV(RMS))	2	A_{VD}	80	100	120	V/V
Input Bias Current	3	I_{IB}	–	-10	-25	µA
Input Common Mode Range Linear Operation (5% max THD)		v_{ICM}	-0.1	–	1.0	V
Differential Input Voltage Linear Operation (5% max THD)		v_{ID}	–	–	25	mVp-p
Output Voltage Swing Differential	2	v_{OD}	3.0	4.0	–	Vp-p
Output Source Current, Toggled		I_O	–	8.0	–	mA
Output Sink Current, Pins 16 and 17	4	I_{OS}	2.8	4.0	–	mA
Small Signal Input Resistance (T_A = 25°C)		r_I	100	250	–	kΩ
Small Signal Output Resistance, Single-Ended (T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V		r_O	–	15	–	Ω
Bandwidth, -3.0 dB (v_{ID} = 2.0 mV(RMS), T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	2	BW	5.0	–	–	MHz
Common Mode Rejection Ratio (T_A = 25°C, f = 100 kHz, A_{VD} = 40 dB, v_{in} = 200 mVp-p, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	5	CMRR	50	–	–	dB
V_{CC1} Supply Rejection Ratio (T_A = 25°C, V_{CC2} = 12 V, $4.75 \leq V_{CC1} \leq 5.25$ V, A_{VD} = 40 dB)		–	50	–	–	dB
V_{CC2} Supply Rejection Ratio (T_A = 25°C, V_{CC1} = 5.0 V, 10 V $\leq V_{CC2} \leq$ 14 V, A_{VD} = 40 dB)		–	60	–	–	dB
Differential Output Offset (T_A = 25°C, $v_{iD} = v_{in}$ = 0 V)		V_{DO}	–	–	0.4	V
Common Mode Output Offset ($v_{iD} = V_{in}$=0 V, Differential and Common Mode)		V_{CO}	–	3.0	–	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T_A = 25°C)	22	e_n	–	15	–	µV(RMS)

ELECTRICAL CHARACTERISTICS (continued)(T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 (V_{OD} = V_{CC1})	6	I_{OD}	1.0	1.4	–	mA
Peak Shift (f = 250 kHz, v_{iD} = 1.0 Vp-p, i_{cap} = 500 μA, where PS = 1/2 $\frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}}$ X 100%, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	7, 8	PS	–	–	5.0	%
Differentiator Input Resistance, Differential		r_{iD}	–	30	–	kΩ
Differentiator Output Resistance, Differential (T_A = 25°C)		r_{oD}	–	40	–	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = –0.4 mA)	9	V_{OH}	2.7	–	–	V
Output Voltage Low Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8.0 mA)	10	V_{OL}	–	–	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	–	–	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	–	–	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A,B}$	500	–	4000	ns
Timing Accuracy Mono #1 (t1 = 1.0 μs = 0.625 R1C1 + 200 ns) (R1 = 6.4 kΩ, C1 = 200 pF) Accurancy guaranteed for R1 in the range 1.5 kΩ ⩽ R1 ⩽ 10 kΩ and C1 in the range 150 pF ⩽ C1 ⩽ 680 pF. Note: To minimize current transients, C1 should be kept as small as is convenient.	12,13	E_{t1}	85	–	115	%
Timing Range Mono #2	11, 12	t2	150	–	1000	ns
Timing Accuracy Mono #2 (t2 = 200 ns = 0.625 R2C2) (R2 = 1 6 kΩ, C2 = 200 pF) Accuracy guaranteed for 1.5 kΩ ⩽ R2 ⩽ 10 kΩ, 100 pF ⩽ C2 ⩽ 800 pF	12, 13	E_{t2}	85	–	115	%

MC3470 CIRCUIT SCHEMATIC

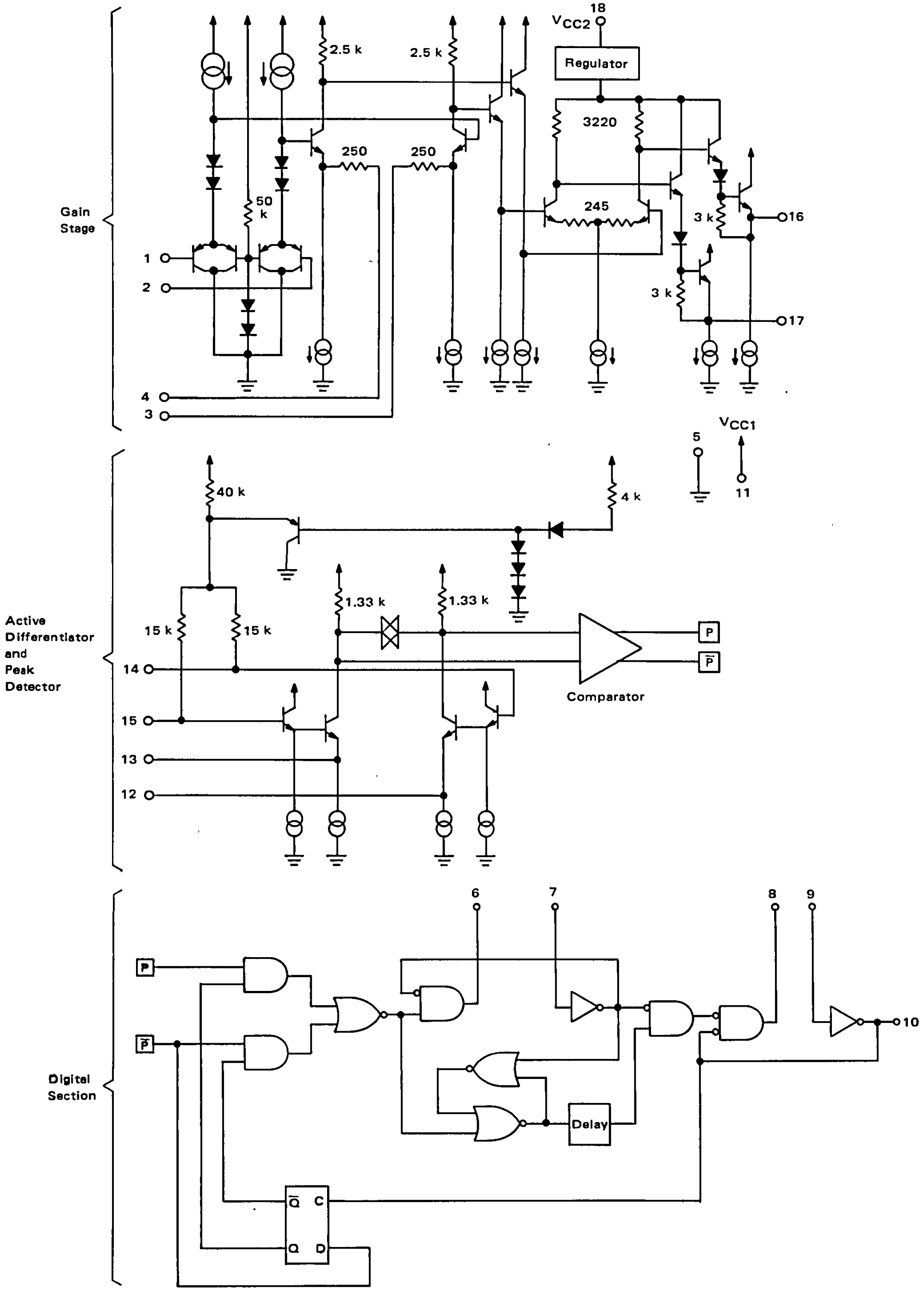


FIGURE 1 – POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

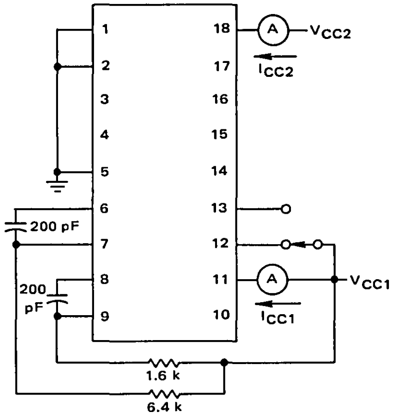


FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

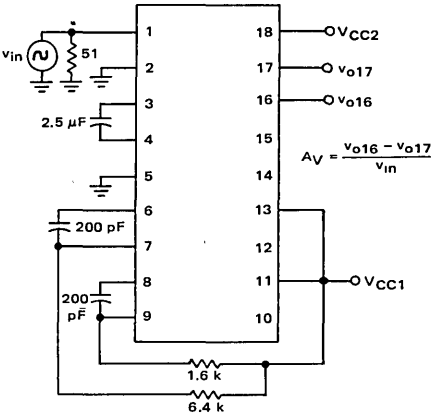


FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, I_{IB}

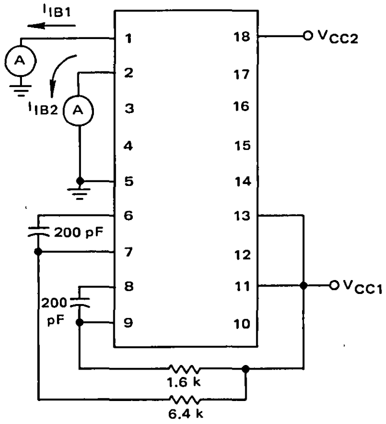


FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17

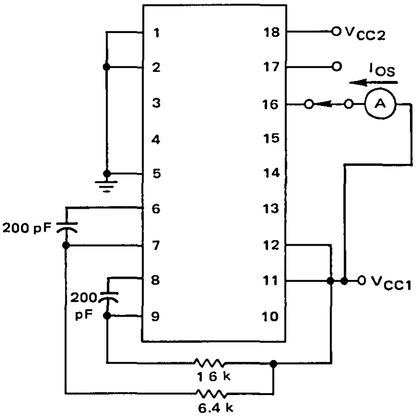
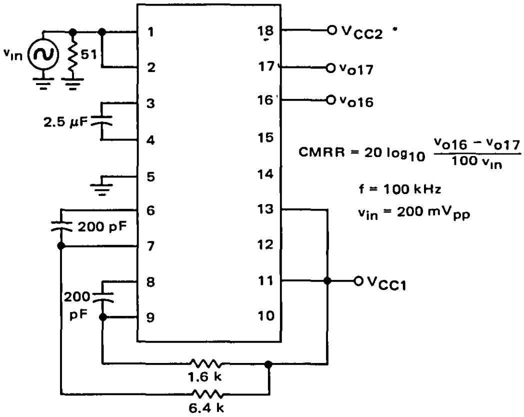


FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR



$$\text{CMRR} = 20 \log_{10} \frac{v_{o16} - v_{o17}}{100\, v_{in}}$$

f = 100 kHz

v_{in} = 200 mVpp

NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

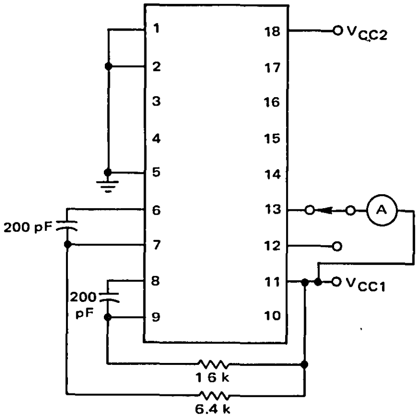


FIGURE 7 – PEAK SHIFT, PS

See Figure 8 for Output Waveform

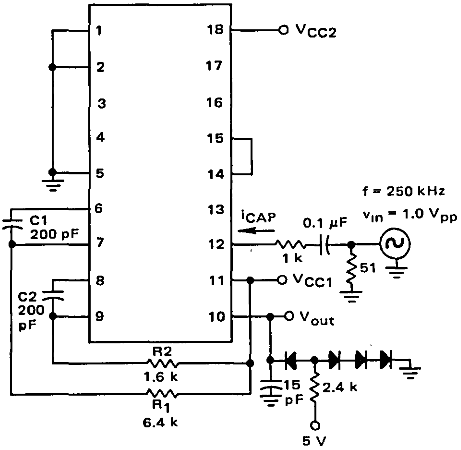
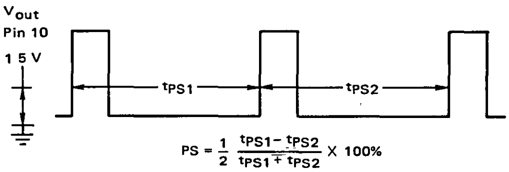


FIGURE 8 – PEAK SHIFT, PS

V_{in} = 1.0 V_{pp} f = 250 kHz

Test schematic on Figure 7



$$PS = \frac{1}{2} \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$$

FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

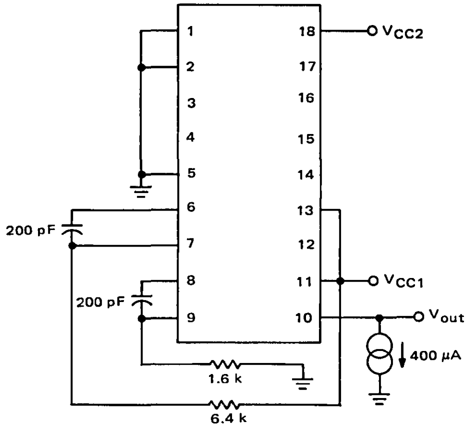


FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

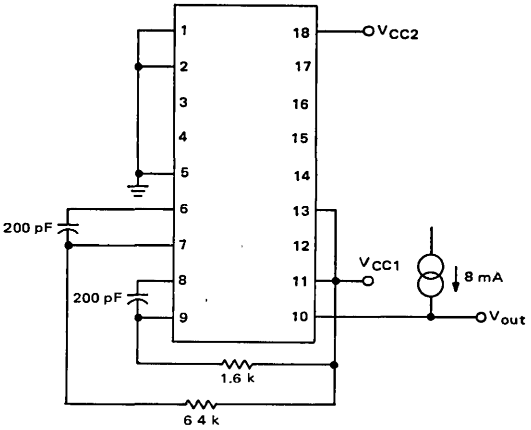
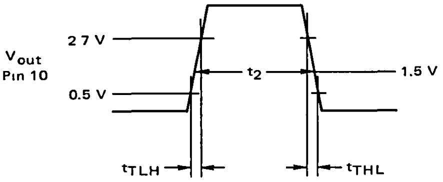


FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{T2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12



$$E_{T2} = \frac{t_2}{200\ \text{ns}} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

V_{in} shown on Figure 13

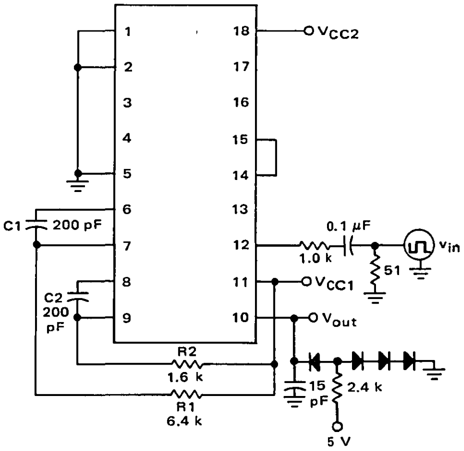
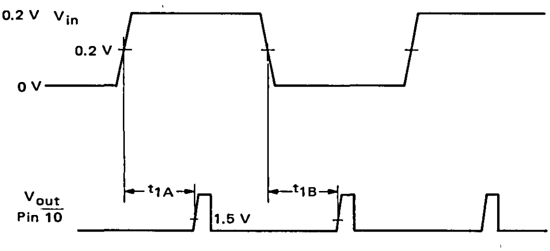


FIGURE 13 — TIMING ACCURACY MONO #1, E_{t1}

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

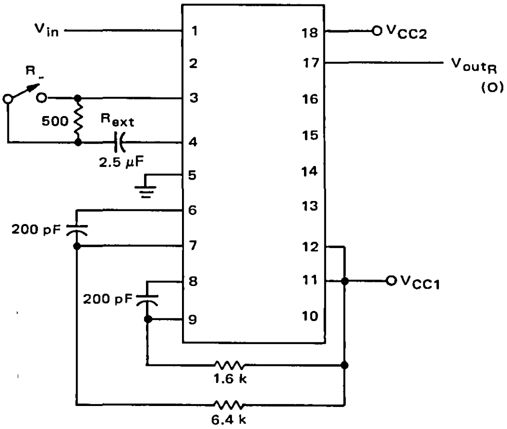


$$E_{t1A} = \frac{t_{1A}}{1000\text{ ns}} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\text{ ns}} \times 100\%$$

FIGURE 14 — AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500\ \Omega$



f = 250 kHz

V_{in} = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{V_O}}{A_{V_R}} - 1\right)} = \frac{500\ \Omega}{2\left(\frac{V_{out_O}}{V_{out_R}} - 1\right)}$$

FIGURE 15 — NORMALIZED POWER SUPPLY CURRENT (I_{CC}/I_{CC} 25°C) versus TEMPERATURE

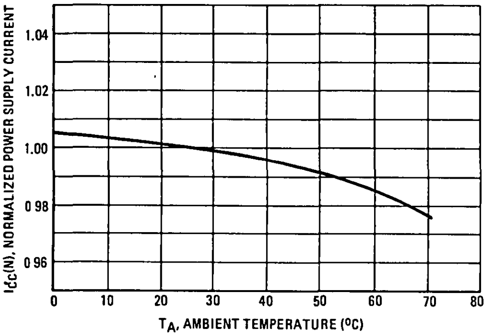


FIGURE 16 — NORMALIZED VOLTAGE GAIN (A_V/A_V 25°C) versus TEMPERATURE

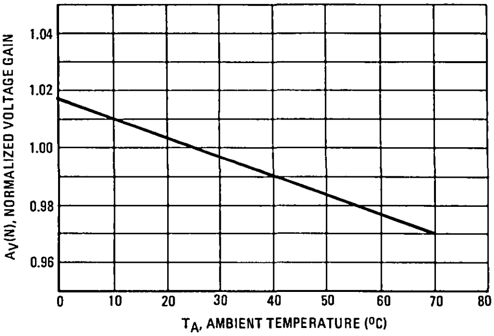


FIGURE 17 — PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

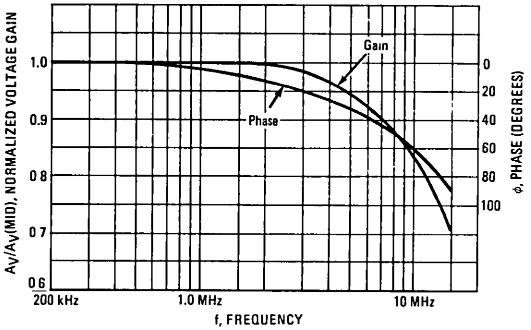


FIGURE 18 — NORMALIZED TIME DELAY t_1 versus TEMPERATURE

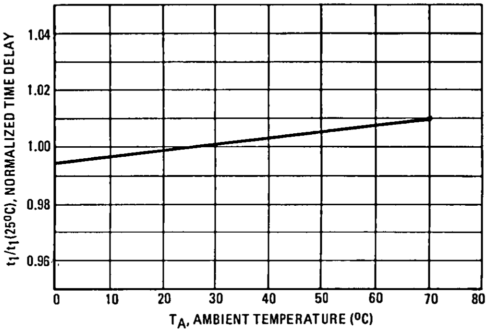


FIGURE 19 — NORMALIZED OUTPUT PULSE WIDTH, t_2/t_2 25°C

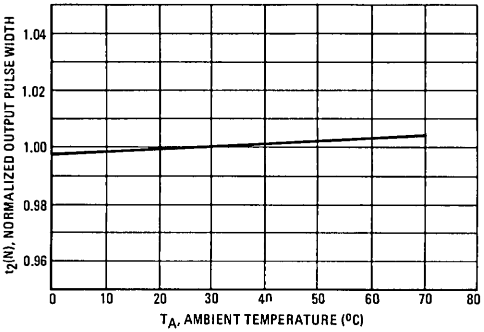


FIGURE 20 — NORMALIZED VOLTAGE GAIN, A_{VR}/A_{VR} 25°C

See Figure 14, Switch Position R

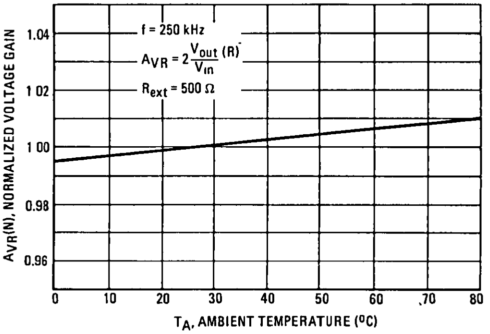


FIGURE 21 — EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

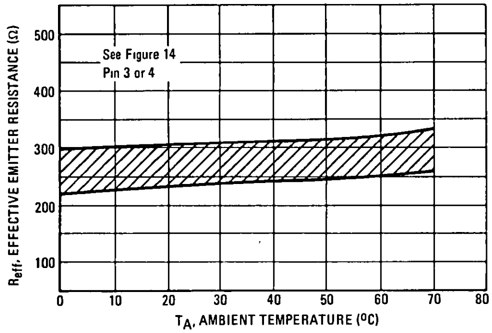
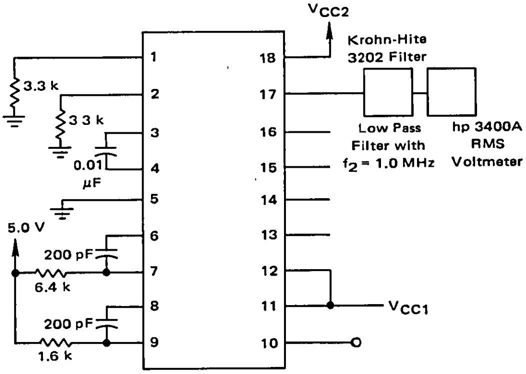


FIGURE 22 — DIFFERENTIAL NOISE VOLTAGE



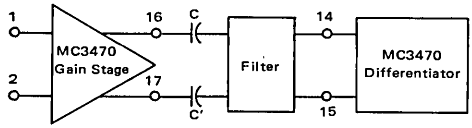
NOTE: Assume uncorrelated noise sources

e_n (differential noise at input) = $e_o\sqrt{2}/100$

APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a), enabling the active differentiator and time domain filter to produce the desired output.

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C′ are placed before the filter as shown in Figure 23a. The charging and discharging of C and C′ is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic — pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_pA_{VD})_{max}}{2.8\ mA}$$

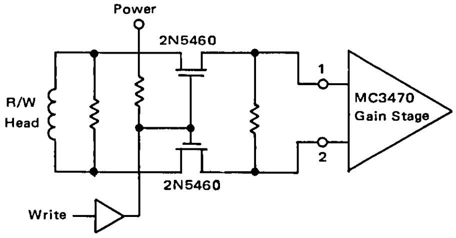
where E_p is the peak differential input voltage to the MC3470.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$\frac{A_{VO}}{A_{VR}} = \frac{R_{ext}}{2(r_e + R_e)} + 1$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,
$A_{VR} \triangleq$ voltage gain with the external resistor in,
$R_{ext} \triangleq$ the external resistor, and
$r_e + R_e \triangleq$ the resistance looking into pin 3 or pin 4.

Thus,

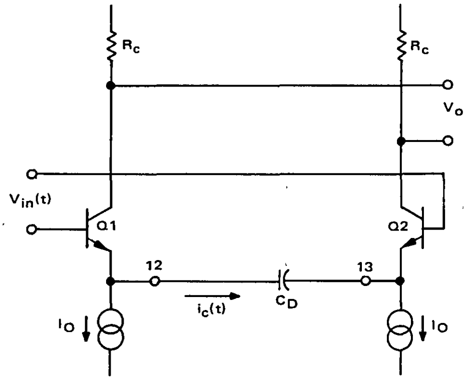
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

FIGURE 24 — ACTIVE DIFFERENTIATOR NETWORK



$$I = Cdv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

V_o is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_p \triangleq$ peak differential voltage applied to MC3470 amplifier input.

$E_p \sin \omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

$A_{VD} \triangleq$ differential voltage gain of input amplifier.

$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.

$= E_pA_{VD}\sin \omega t$ (Note: The filter is assumed to be lossless.)

$i_c(t) \triangleq$ current through capacitor C_D.

$R_O \triangleq$ output resistance of Q1 (Q2) at pin 12 (13).

If $v_{in}(t) = E_pA_{VD}\sin \omega t$, then the current through the capacitor C_D is given by

$$i_c(t) = C_DA_{VD}E_p\omega\cos\omega t$$

$$\text{and } V_O(t) = 2R_CC_DA_{VD}E_p\omega\cos\omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω, the maximum slew rate occurs for the maximum value of i_c or $\cos\omega t = 1$. Therefore,

$$i_c = C_DA_{VD}E_p\omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_c; therefore, C_D must be chosen such that the maximum i_c occurs at the maximum $A_{VD}E_p\omega$ product.

$$C_D = -\frac{i_{c}max}{(A_{VD}E_p\omega)_{max}} = \frac{1 \text{ mA}}{(120)(E_p\omega)_{max}}.$$

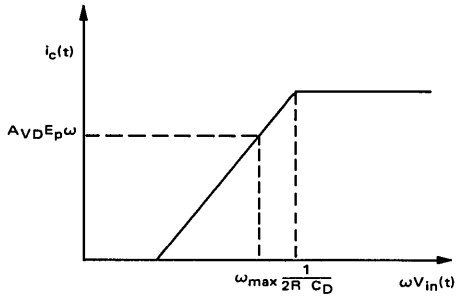
If the peak value specified for i_c is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2R_OC_D$. If this pole is ten times greater than the maximum operating frequency (ω_{max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 ω_{max} needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\,10\,\omega_{max}}.$$

If R_O is not large enough to satisfy this condition, a series

FIGURE 25 — RESPONSE OF DIFFERENTIATOR USING ONLY C_D

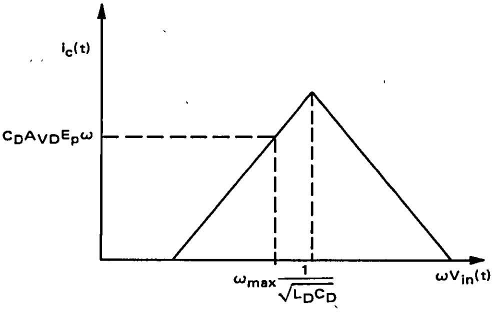


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\,10\,\omega_{max}}.$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_o) and the damping ratio (δ) to meet the systems requirements where

FIGURE 26 — COMPLETE RESPONSE OF DIFFERENTIATOR



$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\,\omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100\,C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

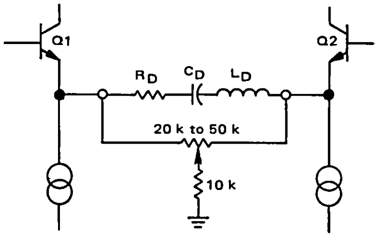
$$R = \frac{\delta}{5\,C_D\omega_{max}}$$

The total resistance (R) is the effective output resistance (R_O) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 — PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

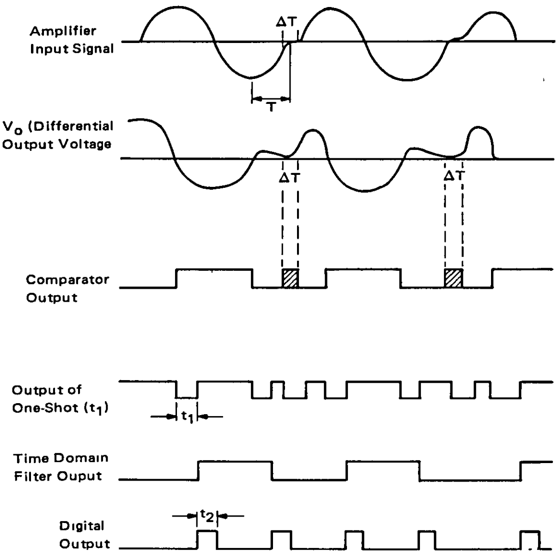
$$t_1 = R_1C_1K_1 + T_o$$

where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 > T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse t_2 (pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1, R_2, C_1, and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For $t_1 = 1\ \mu s$ and $t_2 = 200$ ns, suggested good values for the capacitors are

$$C_1 = 250\text{ pF}$$

$$C_2 = 160\text{ pF}$$

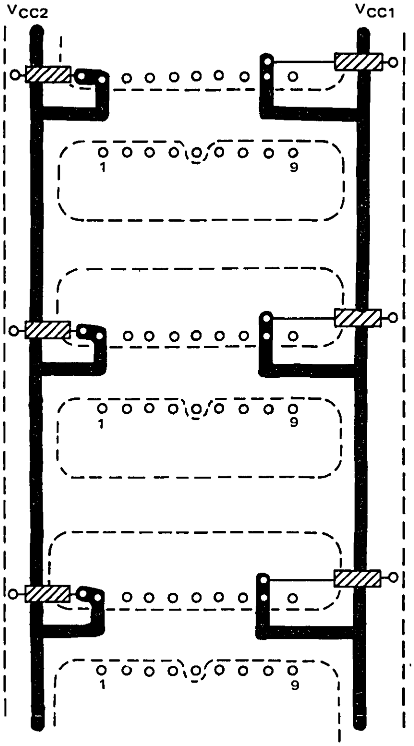
BOARD LAYOUT AND TESTING CONSIDERATIONS

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.

MC3480

Specifications and Applications Information

DYNAMIC MEMORY CONTROLLER

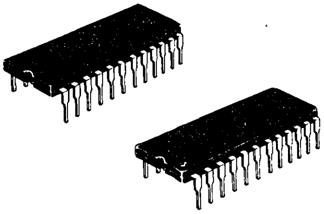
SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

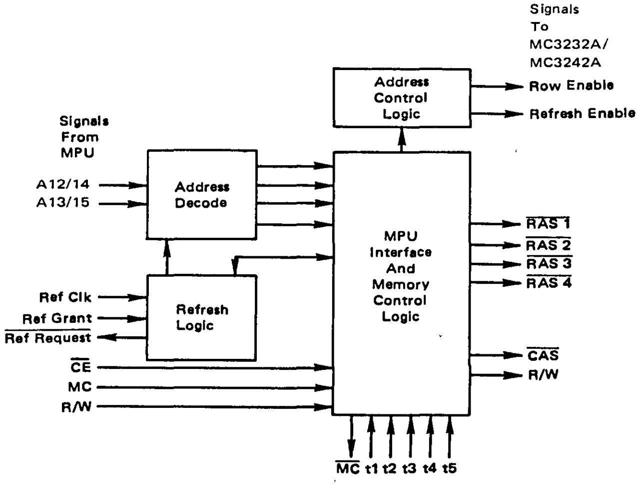
- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 $\overline{\text{RAS}}$ Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

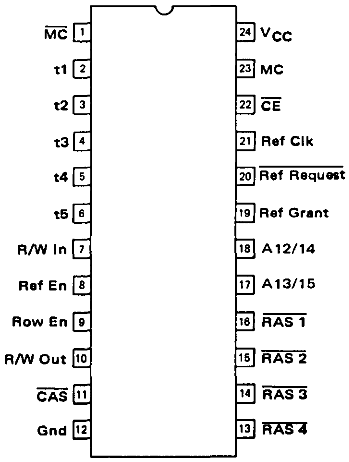
BLOCK DIAGRAM



Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

PIN CONNECTIONS



See Pin Descriptions

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	−0.5 to +7.0	Vdc
Output Voltage	V_O	−0.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

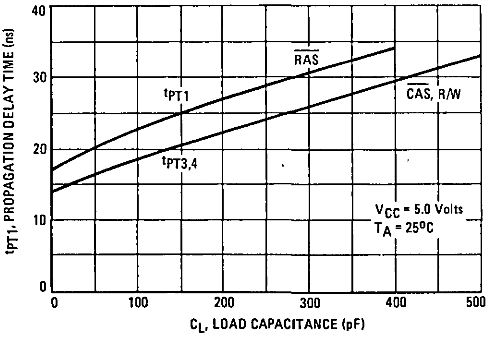
RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.50 to +5.50	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Current — Low Logic State (V_{IL} = 0.5 V)	I_{IL}	—	—	-250	µA
Input Current — High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	—	—	40 100	µA
Input Clamp Voltages (I_{IK} = 18 mA)	V_{IK}	—	—	-1.5	V
Output Voltage — Low Logic State (I_{OL} = 24 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OL} = 8.0 mA for Row En, Ref En, $\overline{MC}$, $\overline{Ref\ Req}$)	V_{OL}	 — —	 — —	 0.5 0.5	V
Output Voltage — High Logic State (I_{OH} = -1.0 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OH} = -0.4 mA for Row En, Ref En, and $\overline{MC}$) I_{OH} = -0.2 mA for $\overline{Ref\ Req}$ (Note: $\overline{Ref\ Req}$ output has internal 5.0 k resistive pullup to V_{CC}.)	V_{OH}	 3.0 2.4 2.4	 — — —	 — — —	V
Power Supply Current — During R/W or Refresh — During Idle	I_{CC}	—	—	65 40	mA
Output Short-Circuit Current (V_{OL} = 0 V for Row En, Ref En, and $\overline{MC}$)	I_{OS}	 -10	 —	 -55	mA

FIGURE 1 — TYPICAL $t_{PT1,3,and4}$ (HIGH TO LOW) versus LOAD CAPACITANCE — $\overline{RAS}$, $\overline{CAS}$ and R/W



SWITCHING CHARACTERISTICS (Unless otherwise noted, $4.5 < V_{CC} < 5.5$ V, and $0 < T_A < 70^{\circ}C$

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times (Full AC Load – All Outputs)					ns
MC to $\overline{\text{MC}}$ – Low to High	$t_{PLH(\overline{MC})}$	–	–	14	
MC to $\overline{\text{MC}}$ – High to Low	$t_{PHL(\overline{MC})}$	–	–	17	
t1 to $\overline{\text{RAS}}$	t_{PT1}	18	–	40	
t2 to Row En	t_{PT2}	16	–	35	
t3 to $\overline{\text{CAS}}$	t_{PT3}	17	–	45	
t4 to R/W	t_{PT4}	16	–	45	
t5 to $\overline{\text{CAS}}$	t_{PT5C}	22	–	42	
to $\overline{\text{RAS}}$	t_{PT5R}	19	–	40	
to R/W	t_{PT5W}	30	–	58	
to Row En (Refresh)	t_{PT5ER}	30	–	65	
to Row En (R/W)	t_{PT5E}	25	–	48	
to Refresh En	t_{PT5F}	22	–	46	
Ref Clk to $\overline{\text{Ref Req}}$	t_{PCQ}	10	–	27	
Ref Grant to Row En }	t_{PGS}	20	–	43	
to Ref En }					
t1 to $\overline{\text{Ref Req}}$ (Ref only)	t_{PTQ}	22	–	60	
Propagation Delay Times (AC Load, 15 pF – All Outputs)					ns
t1 to $\overline{\text{RAS}}$	t_{PT1}	10	–	30	
t2 to Row En	t_{PT2}	16	–	35	
t3 to $\overline{\text{CAS}}$	t_{PT3}	8.0	–	25	
t4 to R/W	t_{PT4}	8.0	–	25	
t5 to $\overline{\text{CAS}}$	t_{PT5C}	14	–	35	
to $\overline{\text{RAS}}$	t_{PT5R}	14	–	35	
to R/W	t_{PT5W}	22	–	45	
to Row En (Refresh)	t_{PT5ER}	30	–	65	
to Row En (R/W)	t_{PT5E}	25	–	48	
to Refresh En	t_{PT5F}	22	–	46	
Setup Times (Full AC Load – All Pins)					ns
Ref Clk before Ref Grant	$t_{su(RC)}$	35	–	–	
A12, A13 before t1	$t_{su(A)}$	10	–	–	
R/W Input before t4	$t_{su(R/W)}$	33	–	–	
$\overline{\text{CE}}$ before t1	$t_{su(\overline{CE})}$	30	–	–	
Ref Grant before t1	$t_{su(RG)}$	25	–	–	
Hold Times (Full AC Load – All Pins)					ns
A12, A13 after t5	$t_{h(A)}$	15	–	–	
$\overline{\text{CE}}$ after t1	$t_{h(\overline{CE})}$	0	–	–	
R/W after t4	$t_{h(R/W)}$	0	–	–	
MC Rising after t1 Rising	$t_{h(MC)}$	30	–	–	
Minimum Delay Times (Note 2 – Full AC Load – All Pins)					ns
t1 Low to High to t2 Low to High	$t_{d(1-2)}$	30	–	–	
t1 Low to High to t4 Low to High	$t_{d(1-4)}$	33	–	–	
t2 Low to High to t3 Low to High	$t_{d(2-3)}$	30	–	–	
t3 Low to High to t5 Low to High	$t_{d(3-5)}$	30	–	–	
Minimum Pulse Widths					ns
t1 through t5 Low	$t_{WL(t)}$	30	–	–	
High	$t_{WH(t)}$	30	–	–	
MC	$t_{W(MC)}$	30	–	–	
Ref Grant	$t_{W(RG)}$	25	–	–	

Note 2: If delays between t1–t5 are less than the minimum specified, the succeeding outputs may not switch.

AC LOADS (Note 3)

R/W and $\overline{\text{CAS}}$ Outputs	450 pF to Gnd*
$\overline{\text{RAS}}$ Outputs	150 pF to Gnd*
$\overline{\text{MC}}$, Row En, Ref En, and $\overline{\text{Ref Req}}$ Outputs	15 pF to Gnd*

*Includes probe and jig capacitance.

NOTE 3: All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.

PIN DESCRIPTION TABLE

Name	No.	Function
$\overline{RAS1}$ • $\overline{RAS2}$ $\overline{RAS3}$ $\overline{RAS4}$	16 15 14 13	Row Address Strobe pins which connect to each of the dynamic RAMs to latch in row address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle.
$\overline{CAS}$ •	11	Column Address Strobe pin which connects to each dynamic RAM to latch in column address.
R/W Out •	10	This pin signals the dynamic RAM whether the RAM is to be read from or written into.
Row En	9	Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses.
Ref En	8	Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done.
$\overline{CE}$	22	Chip Enable Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the $\overline{MC}$ output. $\overline{CE}$ must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of $\overline{CE}$.
R/W In	7	The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle.
A13 (A15) A12 (A14)	17 18	Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four $\overline{RAS}$ outputs. A14 and A15 apply to 16K RAMs.
MC	23	Memory Clock input from MC6875 clock or other signal source. The rising edge of MC must occur after the rising edge of t1 to avoid aborting the refresh cycle. When MC rises, it resets an internal flag that will terminate refresh at the end of the current cycle. Failure to reset the flag forces the 3480 to refresh every cycle thereafter. MC can be connected to t2 or t3 in noncritical applications.
$\overline{MC}$	1	The buffered complement output of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t1 through t5.
t1 RAS t2 Row EN t3 CAS t4 WRITE t5 END	2 3 4 5 6	These pins use external timing inputs to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four $\overline{RAS}$ outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the $\overline{CAS}$ output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of $\overline{MC}$, Ref En, and $\overline{Ref\ Req}$). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1.
Ref Clk	21	The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the $\overline{Ref\ Req}$ pin goes to a Logic 0.
$\overline{Ref\ Req}$	20	The Refresh Request output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 kΩ pullup resistor to the V_{CC} supply to allow wire-ORing if desired.
Ref Grant	19	Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the $\overline{Ref\ Req}$ pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes $\overline{Ref\ Req}$ to go high and all the $\overline{RAS}$ outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t3 and t4 go high because no $\overline{CAS}$ or R/W signal is needed during refresh. A positive edge on t5 resets the $\overline{RAS}$ and Row En to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle.
V_{CC}	24	+5.0 V supply. A 0.1 µF capacitor is recommended to bypass pin 24 to ground.
Gnd	12	System Ground.

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMs/(150 pF for $\overline{RAS}$ outputs, and 450 pF for $\overline{CAS}$ and R/W outputs). Consequently, these outputs have no short-circuit limit and must be handled accordingly. Good high capacitance load driving techniques usually include a 10 Ω or greater series damping resistor. It is highly recommended that this be done on $\overline{RAS}$, $\overline{CAS}$ and R/W outputs of the MC3480. The effect of these series damping resistors on rise and fall times must be included in timing considerations.

NOTE: All other outputs are LS/TTL totem-pole configuration unless otherwise noted.

TIME DELAY INFORMATION

TIMING REQUIREMENT CONSTRAINTS

$\Delta t1$	Minimum is determined by MPU Address Delay (t_{AD}), plus RAM Row Address Set-Up Time (t_{ASR}), minus MC3480 Propagation Delay (t_{PT1}).
$\Delta t2 - \Delta t1$	Minimum is determined by RAM Row Address Hold Time (t_{RAH}) minus the minimum MC3232A/3242A Row Enable to Output Delay (t_{00MIN}).
$\Delta t3 - \Delta t2$	Minimum is determined by RAM Column Address Set-Up Time ($t_{ASC\ minimum}$) plus maximum MC3232A/3242A Row Enable to Output Delay (t_{001MAX}).
$\Delta t4 - \Delta t3$	No Minimum
$\Delta t5 - \Delta t3$	Minimum is determined by RAM minimum $\overline{CAS}$ Pulse Width (t_{CAS}) or Access Time from $\overline{CAS}$ (t_{CAC}) plus Data Set-Up Time of MPU (t_{DSR}).
$\Delta t5 - \Delta t4$	Minimum is determined by the RAM minimum Write Pulse Width (t_{WP}).

Note: Also required in computing time delays are the various delays incurred by the particular delay scheme used; i.e., delays between 4 x f_o, 2 x f_o, and f_o from the MC6875 which are used as inputs or the gate delays of the gates used in Figures 5A through 5C.

TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs

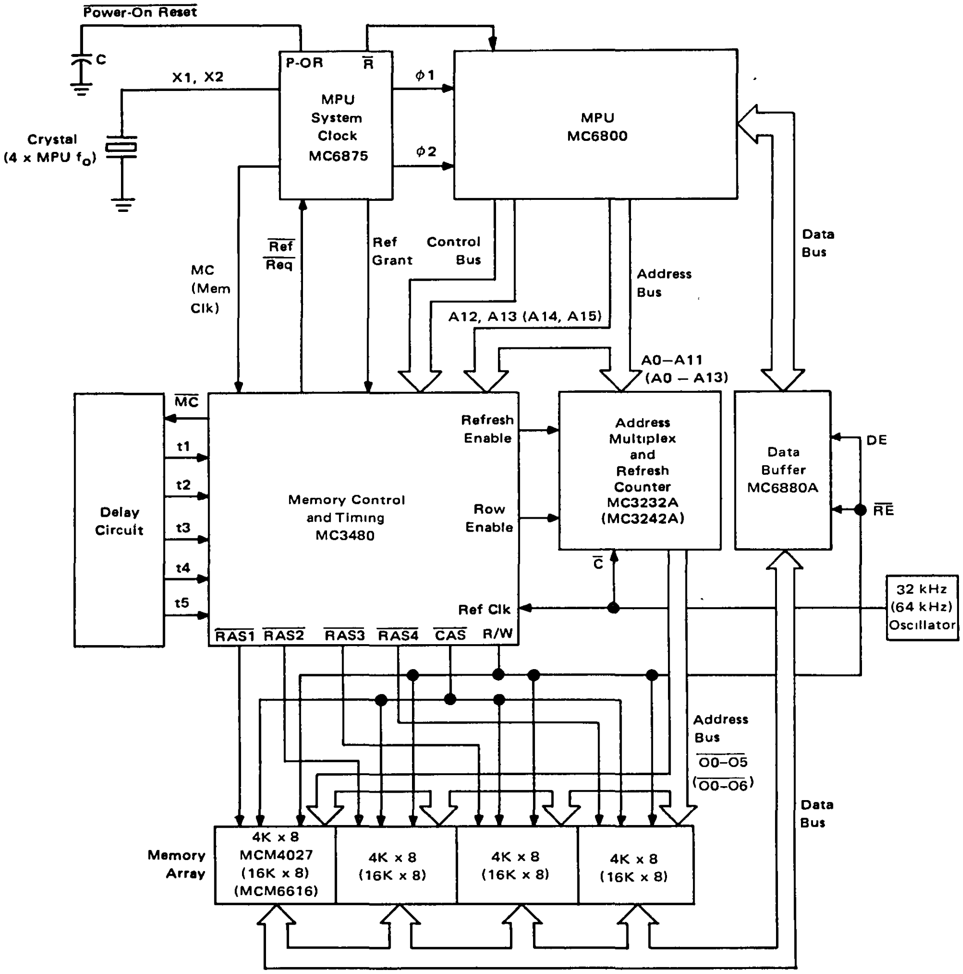
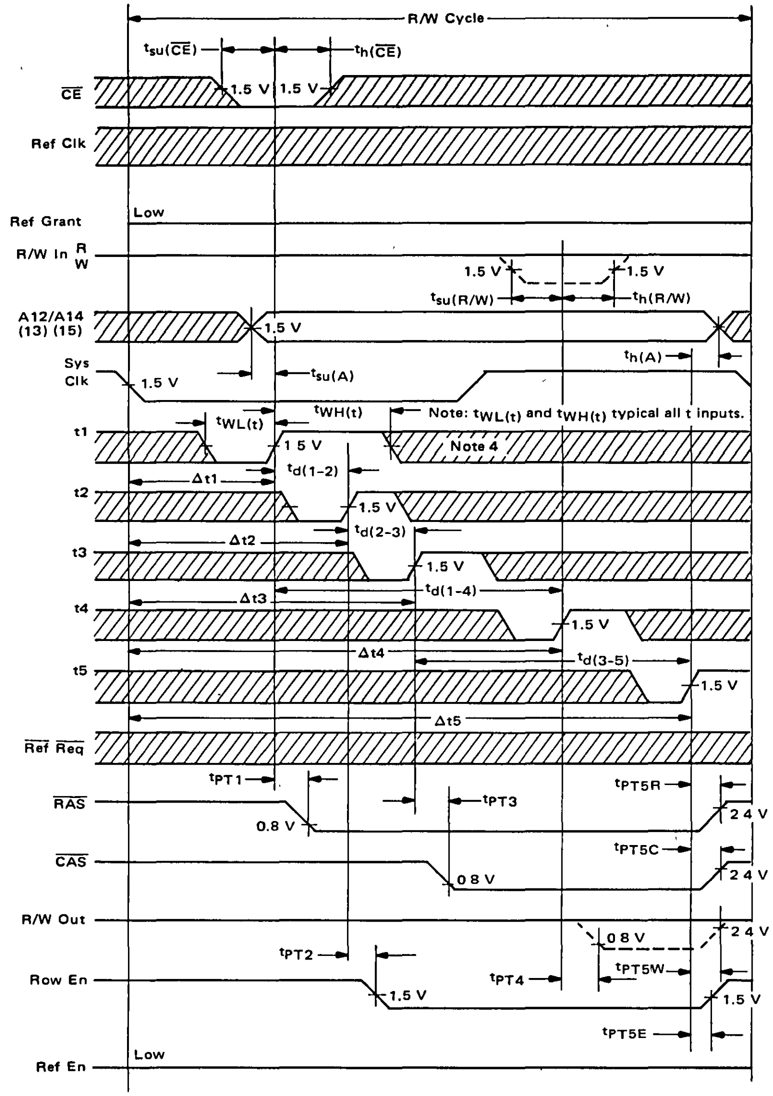


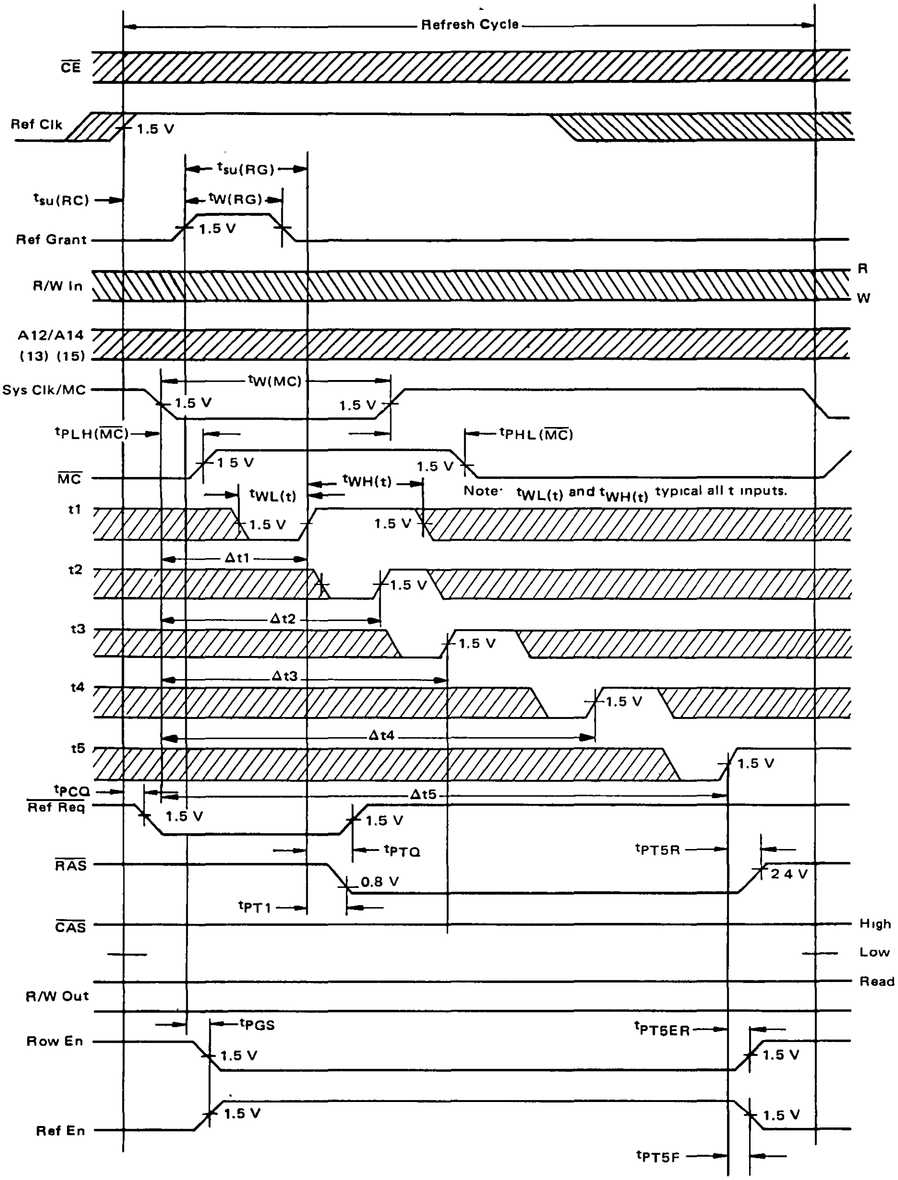
FIGURE 2 – READ/WRITE TIMING CYCLE



▨ = Don't care.

NOTE 4: Although t1 and $\overline{CE}$ are shown as don't care after their respective minimum hold times, t1 may rise again after the initial rising edge in a R/W cycle only if $\overline{CE}$ is low. Bringing t1 high a second time during a cycle when $\overline{CE}$ is high will improperly terminate the cycle.

FIGURE 3 — REFRESH TIMING CYCLE

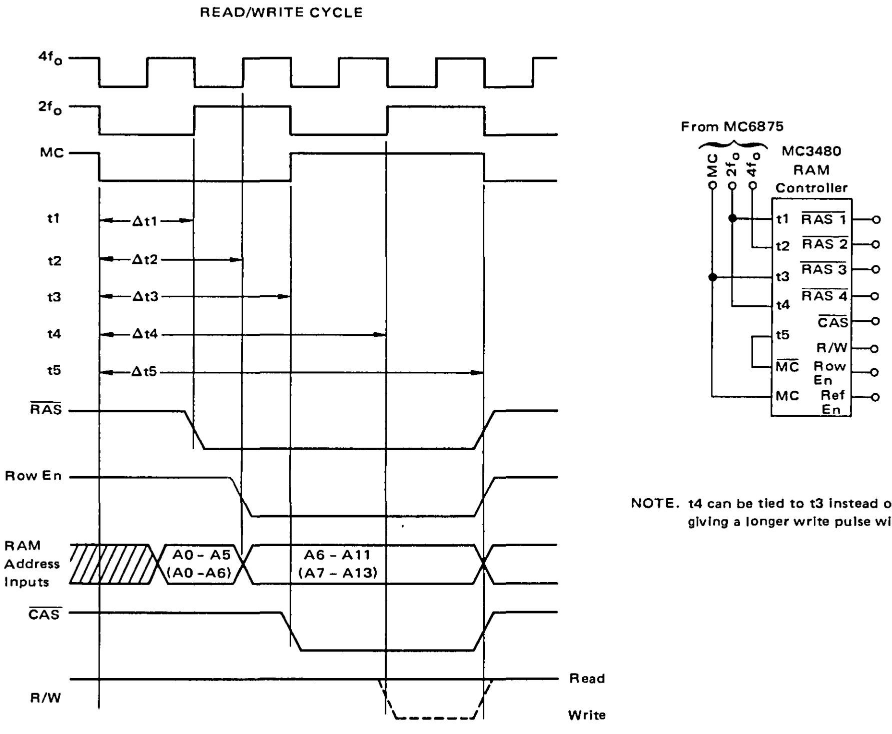


APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The MC3480 uses five general timing inputs in place of a master clock with on-chip timing generation. This gives the system designer optimum flexibility in interfacing with the various microprocessor families and dynamic memories that are available. In simpler slow speed systems, the timing signals required can be directly obtained from those available from the microprocessor. In systems requiring high speed memory/microprocessor cycle times, timing input t1-t5 can be obtained using delay lines or a range of techniques as shown in Figures 4 thru 8. It is only necessary to maintain the time delay relationships shown under time delay information.

FIGURE 4 – UNIVERSAL TIME DELAY USING MC6875



NOTE. t4 can be tied to t3 instead of $2f_o$, giving a longer write pulse width

FIGURE 5 — ALTERNATE TIME DELAYS USING MC6875
(Read/Write Cycle Shown)

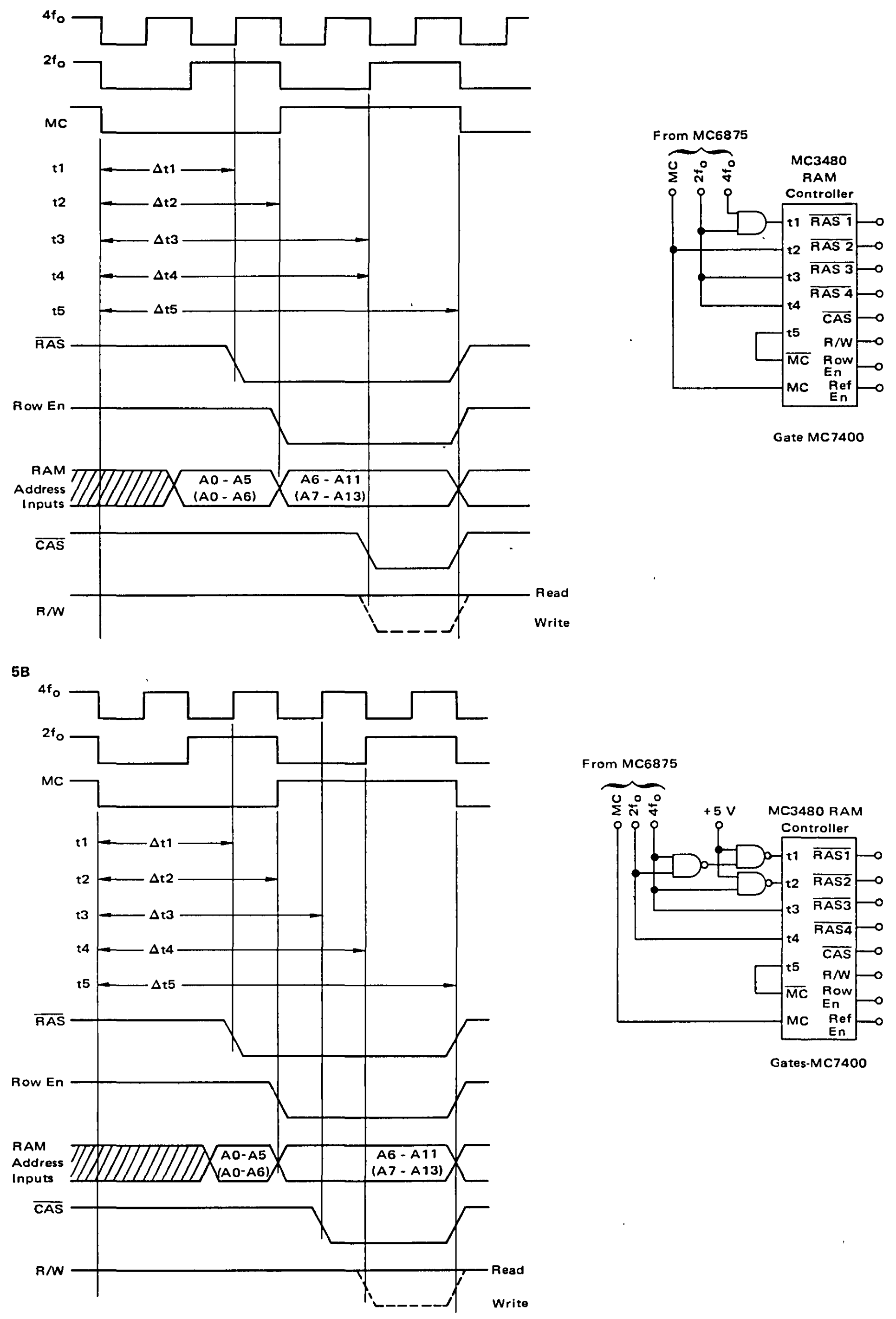
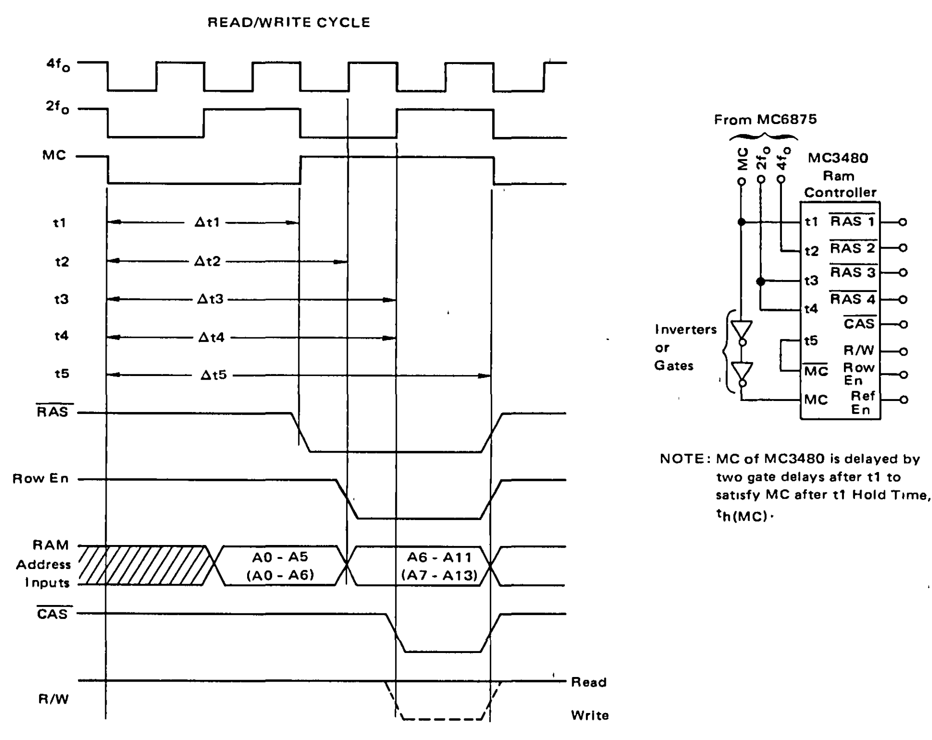
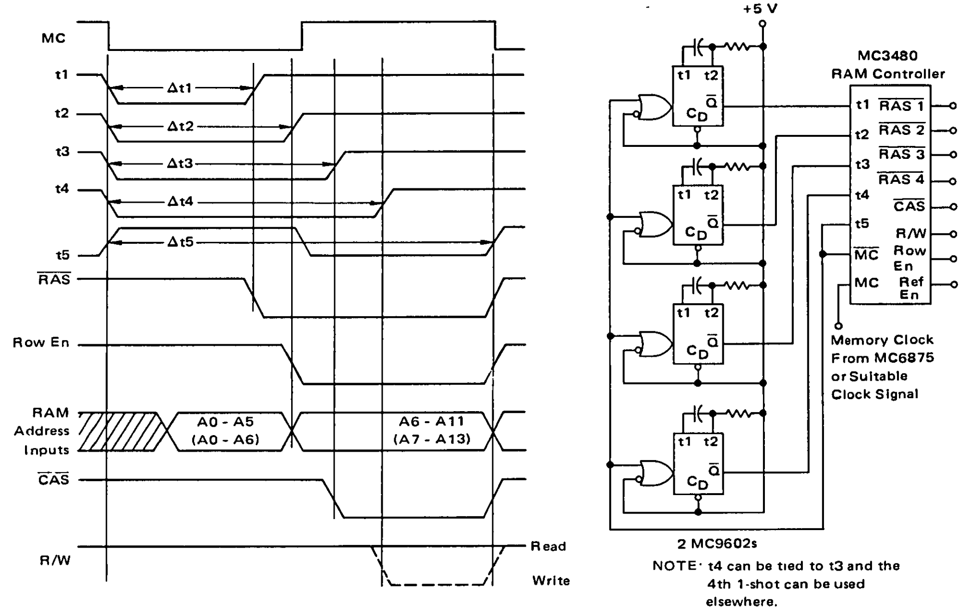


FIGURE 5C – ALTERNATE TIME DELAYS USING MC6875



NOTE: MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

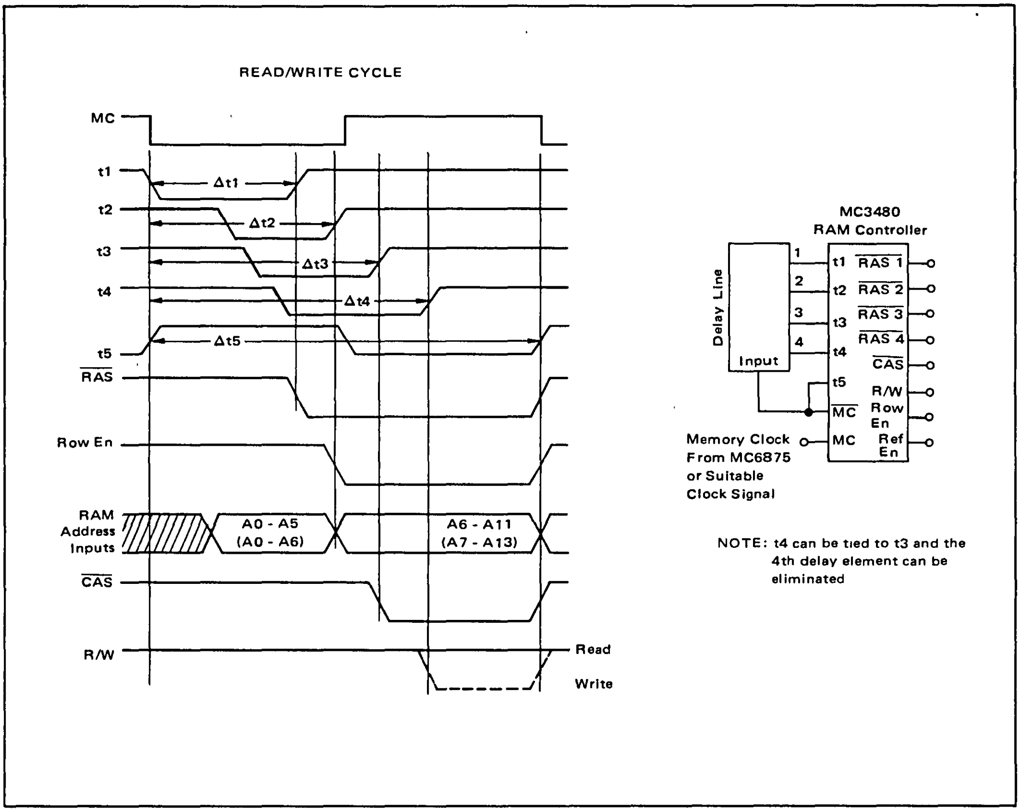
FIGURE 6 – ONE SHOT TIME DELAY METHOD



2 MC9602s

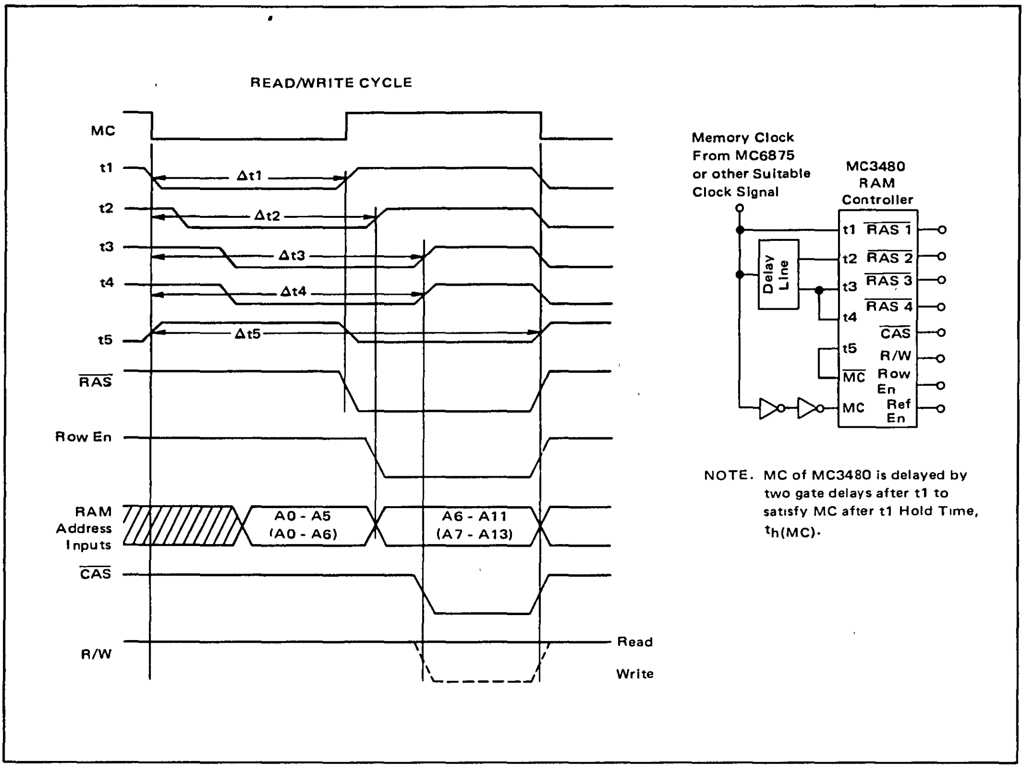
NOTE: t4 can be tied to t3 and the 4th 1-shot can be used elsewhere.

FIGURE 7 — DELAY LINE TIME DELAY METHOD



NOTE: t4 can be tied to t3 and the 4th delay element can be eliminated

FIGURE 8 – DELAY LINE TIME DELAY (ALTERNATE METHOD)



NOTE. MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

REFRESH CONSIDERATIONS

The MC3480/MC3232A (MC3242A) memory control system can be used with either cycle steal or transparent refresh methods. Figure 9 shows one transparent technique employing refresh during $\phi2$ low in an M6800 microprocessor-based system. Using this technique requires that the memory be capable of completing a Read/Write Cycle and a Refresh Cycle sequentially during the M6800 cycle. The minimum cycle time at the time of printing for dynamic multiplexed RAMs is 320 ns, therefore limiting the microprocessor to 1.56 MHz operation. The D flip-flops of Figure 9 produce a trigger at the beginning of both $\phi1$ and $\phi2$. For a 1.0 MHz system, the t1–t5 inputs should be adjusted for the following delays:

RAS falls at 150 ns (triggered by t1)
Row En falls at 250 ns (triggered by t2)
CAS, R/W falls at 300 ns (triggered by t3)
t5 rises at 500 ns.

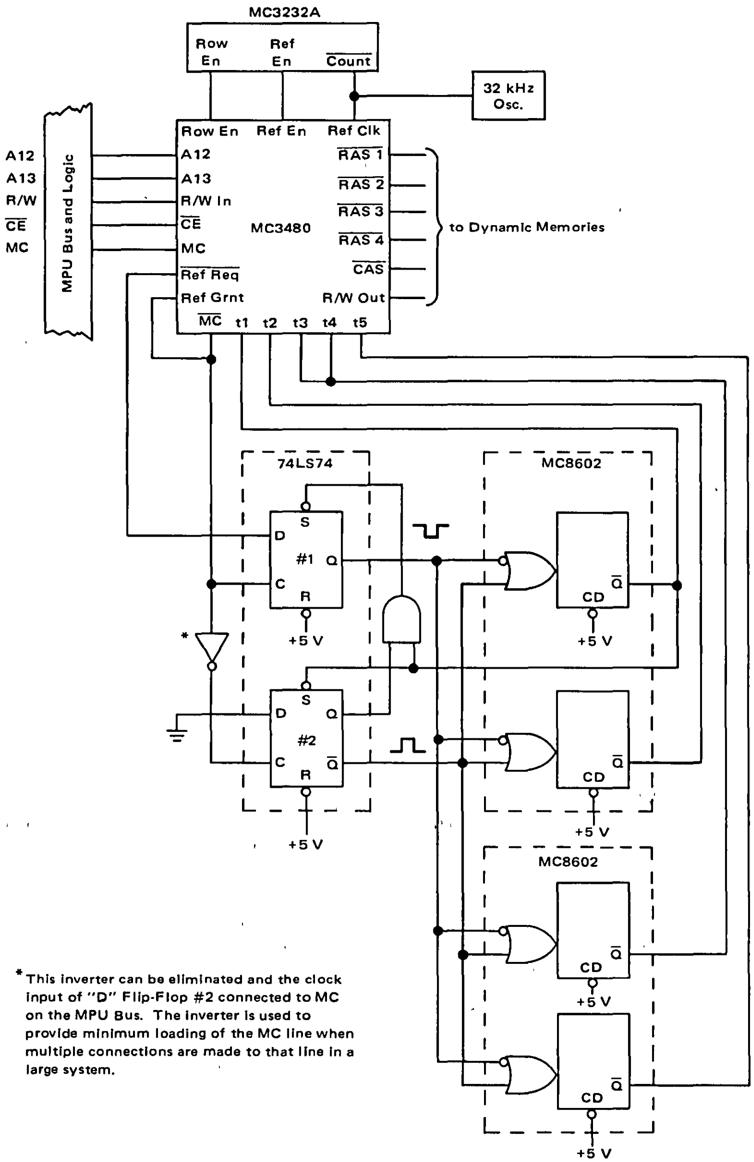
A delay line could be used to generate t1-t5 in place of the four monostables. For the 1.0 MHz system, it would require either two 5 tap delay lines with 50 ns per tap or a 10 tap line with 50 ns/tap. For use with a 600 kHz system, a delay line with 5 taps of 150 ns each could be used. For this case:

RAS falls at 150 ns
Row En falls at 300 ns
CAS, R/W falls at 450 ns
t5 rises at 750 ns .

Figure 10 shows typical refresh oscillator configurations for both 32 kHz (f_{REF}min for 4K) and 64 kHz (f_{REF}min for 16K). In the case of transparent refresh, if the designer is not concerned with power consumption, the refresh oscillator may be eliminated and the Ref Clk input connected to the MC input yielding a refresh every $\phi1$.

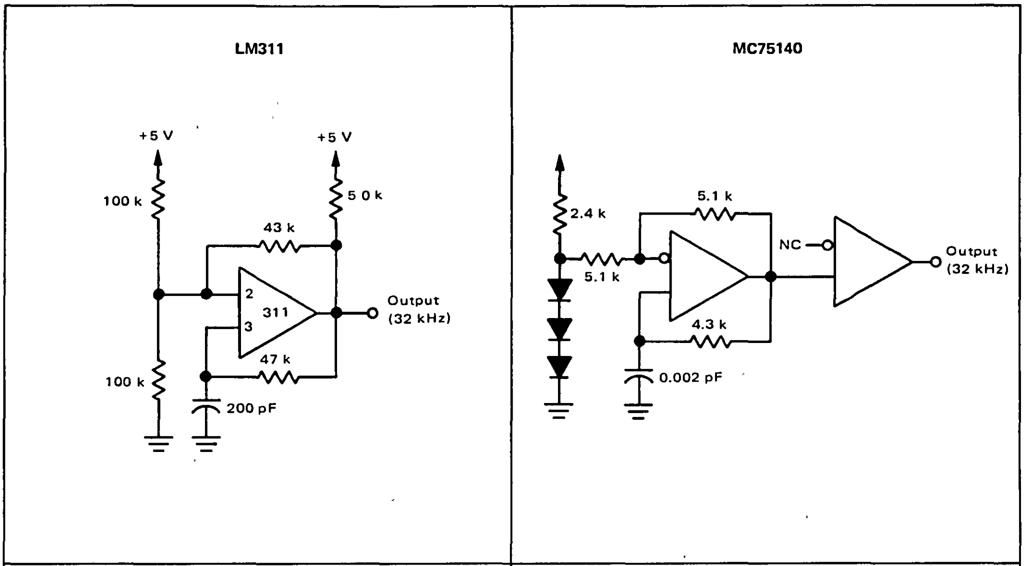
For DMA operation combined with cycle stealing refresh, care must be taken not to allow a DMA request during a Refresh Request/Grant period and to hold off a refresh during a DMA operation. See comments under pin descriptions, Pin 19.

FIGURE 9 — EXAMPLE OF $\phi 2$ LOW METHOD OF HIDDEN REFRESH USING MC3480 AND 4K RAMS



*This inverter can be eliminated and the clock input of "D" Flip-Flop #2 connected to MC on the MPU Bus. The inverter is used to provide minimum loading of the MC line when multiple connections are made to that line in a large system.

FIGURE 10 — SUGGESTED 32 kHz OSCILLATORS

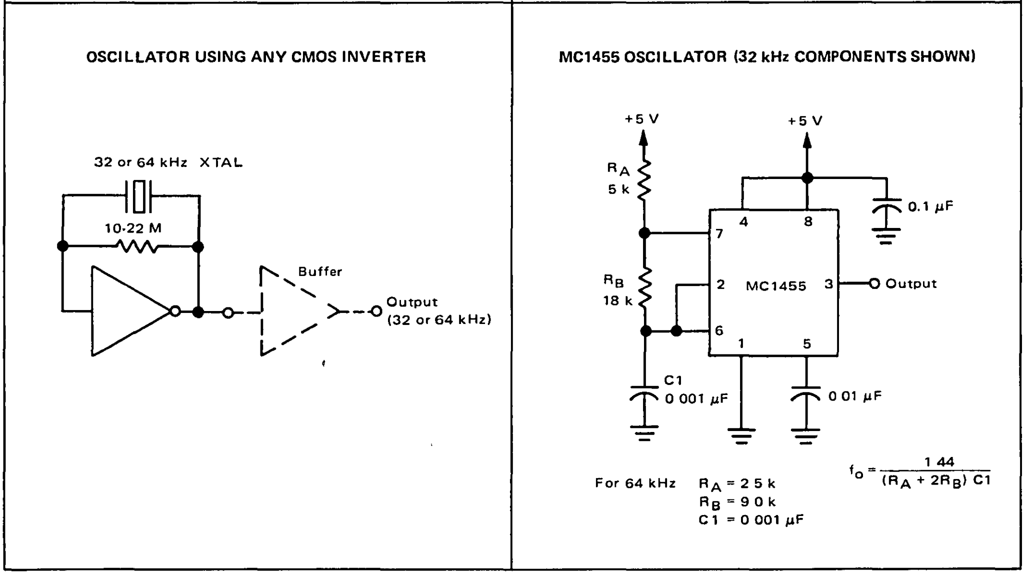


LM311

MC75140

OSCILLATOR USING ANY CMOS INVERTER

MC1455 OSCILLATOR (32 kHz COMPONENTS SHOWN)



MOTOROLA

MC6875
MC6875A

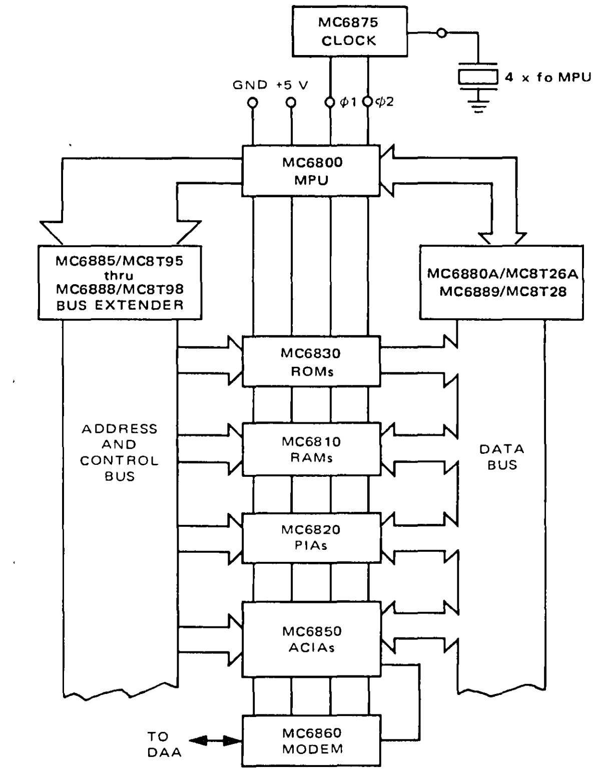
Specifications and Applications Information

M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi1$ and $\phi2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

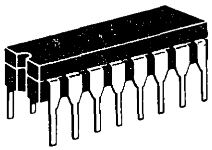
Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

Typical MPU System with Bus Extenders



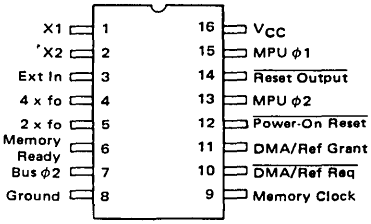
M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted T_A = 25°C.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_I	+5.5	Vdc
Operating Ambient Temperature Range MC6875L MC6875AL	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State MPU φ1 and φ2 Outputs (V_{CC} = 4.75 V, I_{OHM} = -200 μA) (V_{CC} = 5.25 V, I_{OHMK} = +5.0 mA)	 V_{OHM} V_{OHMK}	 V_{CC} - 0.6 –	 – –	 – V_{CC} + 1.0	V
Bus φ2 Output (V_{CC} = 4.75 V, I_{OHB} = -10 mA) (V_{CC} = 5.25 V, I_{OHBK} = +5.0 mA)	 V_{OHB} V_{OHBK}	 2.4 –	 – –	 – V_{CC} + 1.0	V
4 x fo Output (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OH4X} = -500 μA)	V_{OH4X}	2.4	–	–	V
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OH} = -500 μA)	V_{OH}	2.4	–	–	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IH} = 3.3 V, $I_{OH\overline{R}}$ = -100 μA)	$V_{OH\overline{R}}$	2.4	–	–	V
Output Voltage — Low Logic State MPU φ1 and φ2 Outputs (V_{CC} = 4.75 V, I_{OLM} = +200 μA) (V_{CC} = 4.75 V, I_{OLMK} = -5.0 mA)	 V_{OLM} V_{OLMK}	 – –	 – –	 0.4 -1 0	V
Bus φ2 Output (V_{CC} = 4.75 V, I_{OLB} = +48 mA) (V_{CC} = 4.75 V, I_{OLBK} = -5.0 mA)	 V_{OLB} V_{OLBK}	 – –	 – –	 0.5 -1.0	V
4 x fo Output (V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL4X} = 16 mA)	V_{OL4X}	–	–	0.5	V
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OL} = 16 mA)	V_{OL}	–	–	0.5	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IL} = 0.8 V, $I_{OL\overline{R}}$ = 3.2 mA)	$V_{OL\overline{R}}$	–	–	0.5	V
Input Voltage — High Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IL}	–	–	0 8	V
Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2) Output Low to High Output High to Low	 V_{ILH} V_{IHL}	 – 0.8	 2 8 1.4	 3.6 –	V
Input Clamp Voltage MC6875L (V_{CC} = 4.75 V, I_{IC} = -5.0 mA) MC6875AL	V_{IC}	– –	– –	-1 0 -1 5	V
Input Current — High Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 4.75 V, V_{IH} = 5.0 V)	I_{IH}	–	–	25	μA
$\overline{\text{Power-On Reset}}$ (V_{CC} = 5.0 V, $V_{IH\overline{R}}$ = 5.0 V)	$I_{IH\overline{R}}$	–	–	50	μA
Input Current — Low Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	I_{IL}	–	–	-250	μA
$\overline{\text{Power-On Reset}}$ Input (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	$I_{IL\overline{R}}$	–	–	-250	μA

OPERATING DYNAMIC POWER SUPPLY CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Currents (V_{CC} = 5.25 V, f_{osc} = 8.0 MHz, V_{IL} = 0 V, V_{IH} = 3.0 V) Normal Operation (Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs at High Logic State)	I_{CCN}	–	–	150	mA
Memory Ready Stretch Operation ($\overline{\text{Memory Ready Input}}$ at Low Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at High Logic State)	I_{CCMR}	–	–	135	mA
DMA/Refresh Request Stretch Operation ($\overline{\text{Memory Ready Input}}$ at High Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at Low Logic State)	I_{CCDR}	–	–	135	mA

SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10).
Typical values measured at V_{CC} = 5.0 V, T_A = 25°C, fo = 1.0 MHz (see Figure 8).

Characteristic	Symbol	Min	Typ	Max	Unit
MPU φ1 AND φ2 CHARACTERISTICS					
Output Period (Figure 3)	t_o	500	–	–	ns
Pulse Width (Figure 3)	t_{PWM}				ns
(fo = 1.0 MHz)		400	–	–	
(fo = 1.5 MHz)		230	–	–	
(fo = 2.0 MHz)		180	–	–	
Total Up Time (Figure 3)	t_{UPM}				ns
(fo = 1.0 MHz)		900	–	–	
(fo = 1.5 MHz)		600	–	–	
(fo = 2.0 MHz)		440	–	–	
Delay Time Referenced to Output Complement (Figure 3) Output High to Low State (Clock Overlap at 1.0 V)	t_{PLHM}	0	–	–	ns
Delay Times Referenced to 2 x fo (Figure 4 MPU φ2 only)					
Output Low to High Logic State	t_{PLHM2X}	–	–	85	ns
Output High to Low Logic State	t_{PHLM2X}	–	–	70	ns
Transition Times (Figure 3)					
Output Low to High Logic State	t_{TLHM}	–	–	25	ns
Output High to Low Logic State	t_{THLM}	–	–	25	ns
BUS φ2 CHARACTERISTICS					
Pulse Width – Low Logic State (Figure 4)	t_{PWLB}				ns
(fo = 1.0 MHz)		430	–	–	
(fo = 1.5 MHz)		280	–	–	
(fo = 2.0 MHz)		210	–	–	
Pulse Width – High Logic State	t_{PWHB}				ns
(fo = 1.0 MHz)		450	–	–	
(fo = 1.5 MHz)		295	–	–	
(fo = 2.0 MHz)		235	–	–	
Delay Times – (Referenced to MPU φ1) (Figure 4)					
Output Low to High Logic State	t_{PLHBM1}				ns
(fo = 1.0 MHz)		480	–	–	
(fo = 1.5 MHz)		320	–	–	
(fo = 2.0 MHz)		240	–	–	
Output High to Low Logic State	t_{PHLBM1}				
(C_L = 300 pF)		–	–	25	
(C_L = 100 pF)		–	–	20	
Delay Times (Referenced to MPU φ2) (Figure 4)					
Output Low to High Logic State	t_{PLHBM2}	-30	–	+25	ns
Output High to Low Logic State	t_{PHLBM2}	0	–	+40	ns
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLHB}	–	–	20	ns
Output High to Low Logic State	t_{THLB}	–	–	20	ns

SWITCHING CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
MEMORY CLOCK CHARACTERISTICS					
Delay Times (Referenced to MPU ϕ2) (Figure 4)					
Output Low to High Logic State	t_{PLHCM}	-50	–	+25	ns
Output High to Low Logic State	t_{PHLCM}	0	–	+40	ns
Delay Times (Referenced to 2 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLHC2X}	–	–	65	ns
Output High to Low Logic State	t_{PHLC2X}	–	–	85	ns
Transition Times (Figure 4)					
Output Low to High State	t_{TLHC}	–	–	25	ns
Output High to Low State	t_{THLC}	–	–	25	ns
2 x fo CHARACTERISTICS					
Delay Times (Referenced to 4 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLH2X}	–	–	50	ns
Output High to Low Logic State	t_{PHL2X}	–	–	65	ns
Delay Time (Referenced to MPU ϕ1) (Figure 4)					
Output High to Low Logic State	$t_{PHL2XM1}$				ns
(fo = 1.0 MHz)		365	–	–	
(fo = 1.5 MHz)		220	–	–	
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLH2X}	–	–	25	ns
Output High to Low Logic State	t_{THL2X}	–	–	25	ns
4 x fo CHARACTERISTICS					
Delay Times (Referenced to Ext. In) (Figure 4)					
Output Low to High Logic State	t_{PLH4X}	–	–	50	ns
Output High to Low Logic State	t_{PHL4X}	–	–	30	ns
Transition Time (Figure 4)					
Output Low to High Logic State	t_{TLH4X}	–	–	25	ns
Output High to Low Logic State	t_{THL4X}	–	–	25	ns
MEMORY READY CHARACTERISTICS					
Set-Up Times (Figure 5)					
Low Input Logic State	t_{SMRL}	55	–	–	ns
High Input Logic State	t_{SMRH}	75	–	–	ns
Hold Time (Figure 5)					
Low Input Logic State	t_{HMRL}	10	–	–	ns
$\overline{\text{DMA/REFRESH REQUEST}}$ CHARACTERISTICS					
Set-Up Times (Figure 6)					
Low Input Logic State	t_{SDRL}	65	–	–	ns
High Input Logic State	t_{SDRH}	75	–	–	ns
Hold Time (Figure 6)					
Low Input Logic State	t_{HDRL}	10	–	–	ns
DMA/REFRESH GRANT CHARACTERISTICS					
Delay Time Referenced to Memory Clock (Figure 6)					
Output Low to High Logic State	t_{PLHG}	-15	–	+25	ns
Output High to Low Logic State	t_{PHLG}	-25	–	+15	ns
Transition Times (Figure 6)					
Output Low to High Logic State	t_{TLHG}	–	–	25	ns
Output High to Low Logic State	t_{THLG}	–	–	25	ns
$\overline{\text{RESET}}$ CHARACTERISTICS					
Delay Time Referenced to $\overline{\text{Power-On Reset}}$ (Figure 7)					
Output Low to High Logic State	$t_{PLH\overline{R}}$	–	–	1000	ns
Output High to Low Logic State	$t_{PHL\overline{R}}$	–	–	250	ns
Transition Times (Figure 7)					
Output Low to High Logic State	$t_{TLH\overline{R}}$	–	–	100	ns
Output High to Low Logic State	$t_{THL\overline{R}}$	–	–	50	ns

DESCRIPTION OF PIN FUNCTIONS

- 4 x fo – A free running oscillator at four times the MPU clock rate useful for a system sync signal
- 2 x fo – A free running oscillator at two times the MPU clock rate
- $\overline{\text{DMA/REF REQ}}$ – An asynchronous input used to freeze the MPU clocks in the ϕ1 high, ϕ2 low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access)
- REF GRANT – A synchronous output used to synchronize the refresh or DMA operation to the MPU
- MEMORY READY – An asynchronous input used to freeze the MPU clocks in the ϕ1 low, ϕ2 high state for slow memory interface
- MPU ϕ1
MPU ϕ2 – Capable of driving the ϕ1 and ϕ2 inputs on two MC6800s
- BUS ϕ2 – An output nominally in phase with MPU ϕ2 having MC8T26A type drive capability
- MEMORY CLOCK – An output nominally in phase with MPU ϕ2 which free runs during a refresh request cycle
- $\overline{\text{POWER-ON RESET}}$ – A Schmitt trigger input which controls $\overline{\text{Reset}}$ A capacitor to ground is required to set the desired time constant Internal 50 k resistor to V_{CC} See General Design Suggestions for Manual Reset Operation
- $\overline{\text{RESET}}$ – An output to the MPU and I/O devices
- X1, X2 – Provision to attach a series resonant crystal or RC network
- EXT IN – Allows driving by an external TTL signal to synchronize the MPU to an external system

FIGURE 1 – BLOCK DIAGRAM

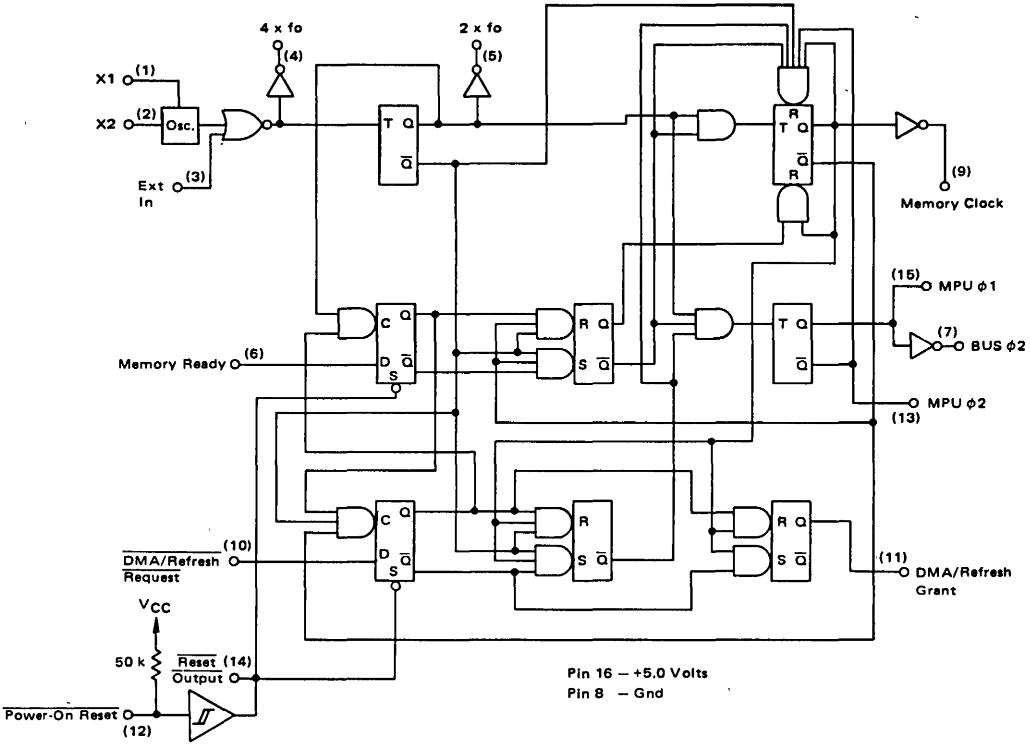


FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF $\overline{\text{RESET}}$ FUNCTION

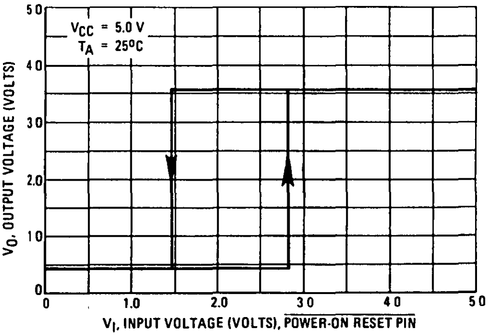
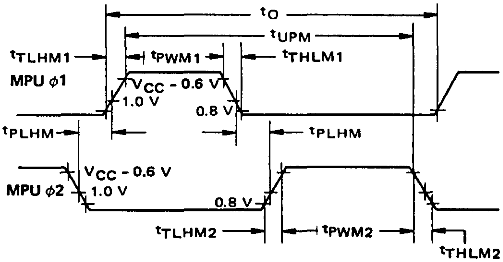


FIGURE 3 – TIMING DIAGRAM FOR MPU ϕ1 AND ϕ2



V_{OV} = 1.0 V = Clock Overlap measurement point

FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION
(Memory Ready and $\overline{\text{DMA/Refresh Request}}$ held high continuously)
Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns

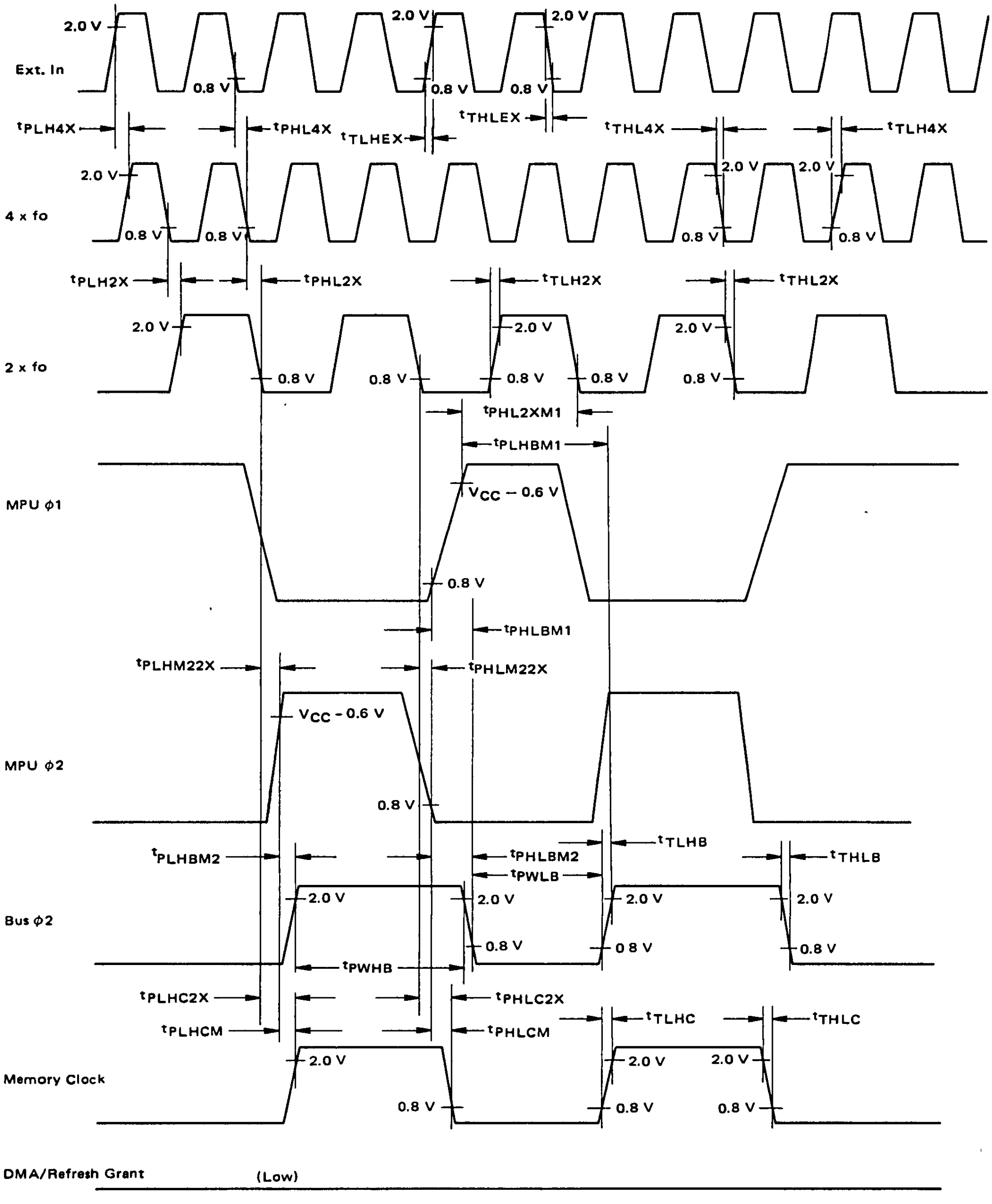


FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns

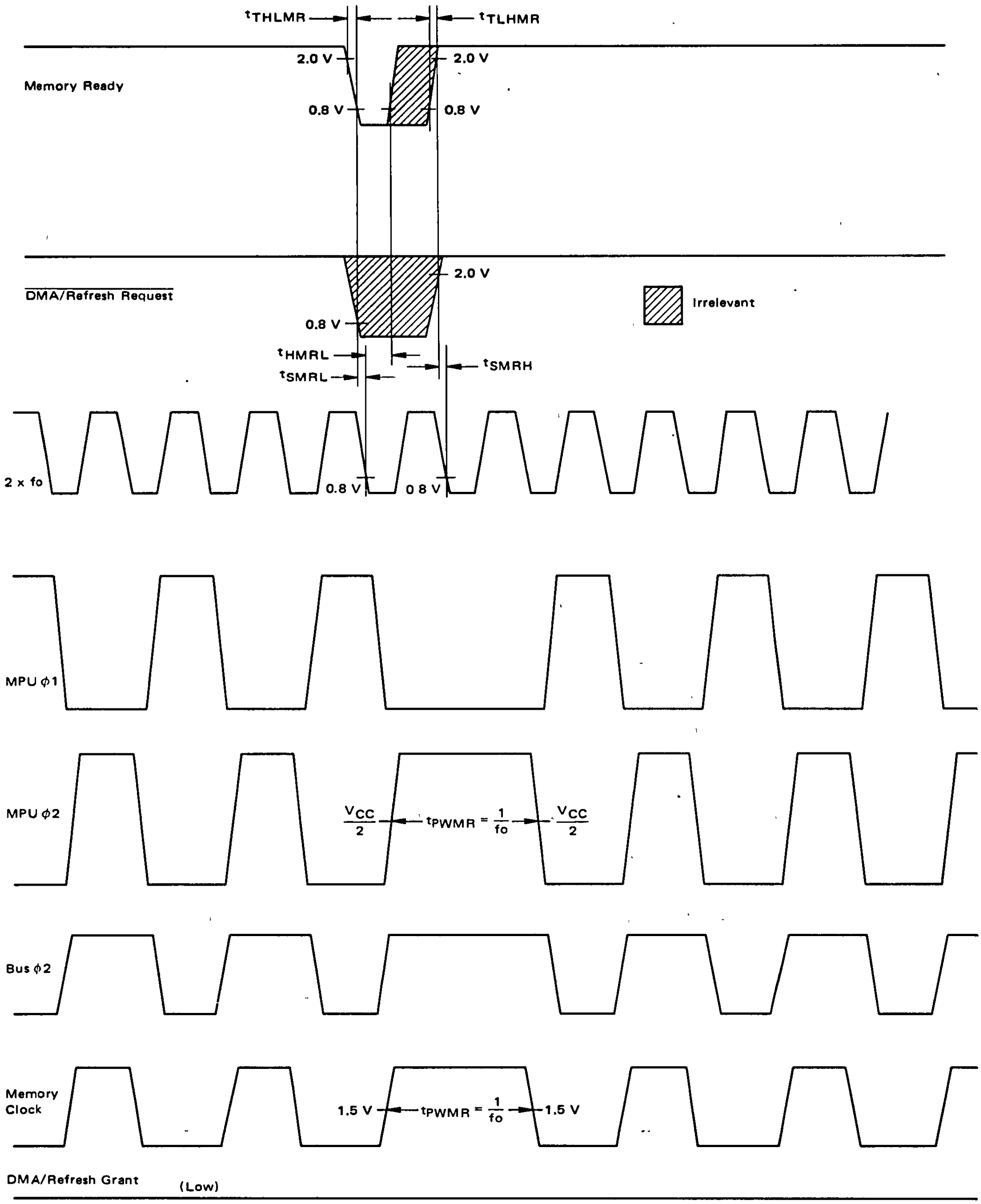


FIGURE 6 – TIMING DIAGRAM FOR $\overline{\text{DMA/REFRESH REQUEST}}$ STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns

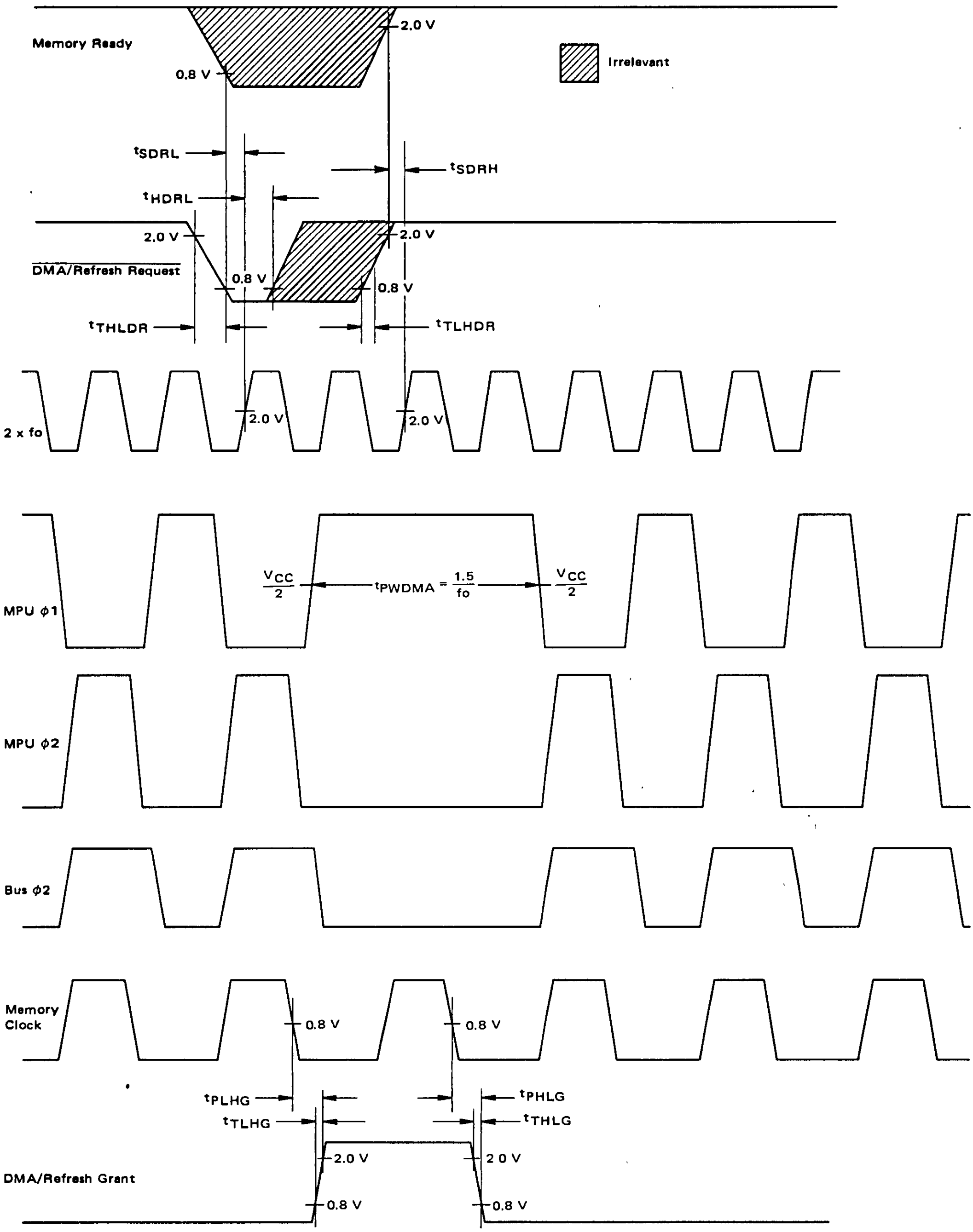


FIGURE 7 — $\overline{\text{POWER ON RESET}}$

Input Voltage: 0 to 5.0 V, f = 100 kHz — Pulse Width = 1.0 μs, $t_{TLH} = t_{THL} = 25$ ns

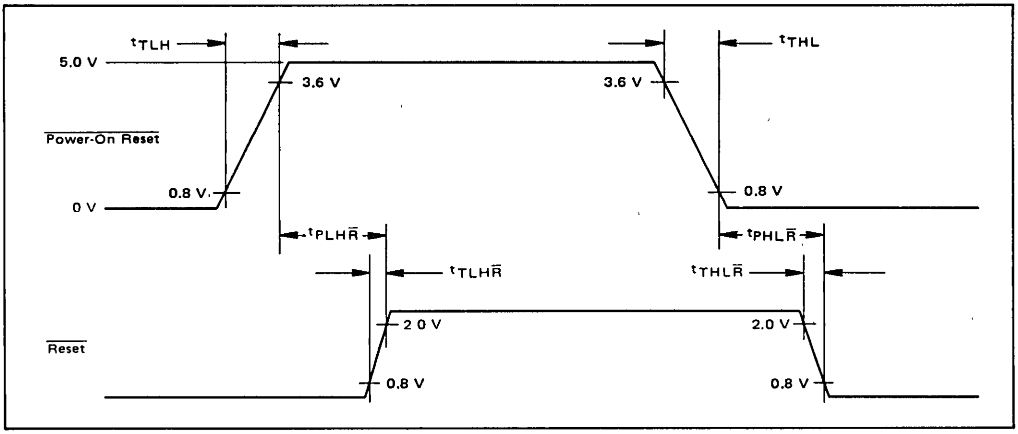
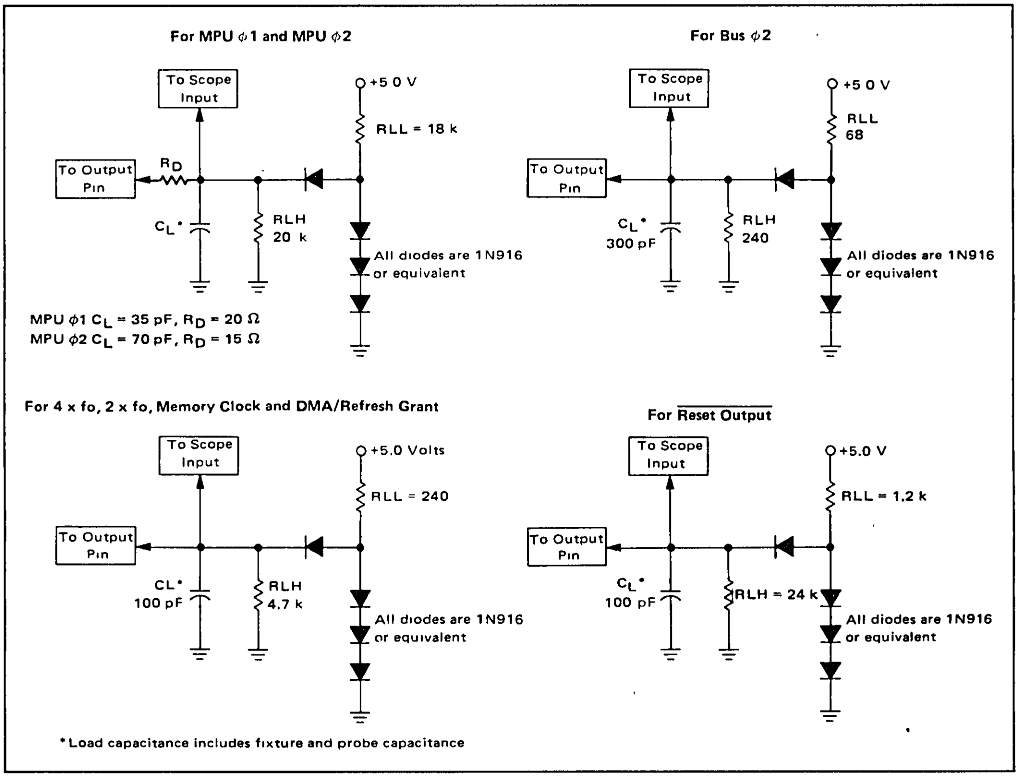


FIGURE 8 — LOAD CIRCUITS



*Load capacitance includes fixture and probe capacitance

APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

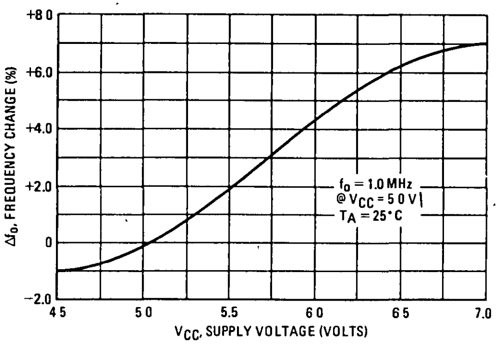


FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

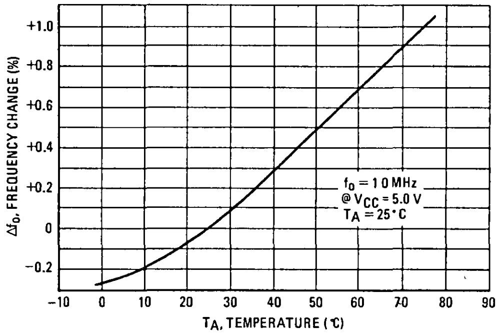
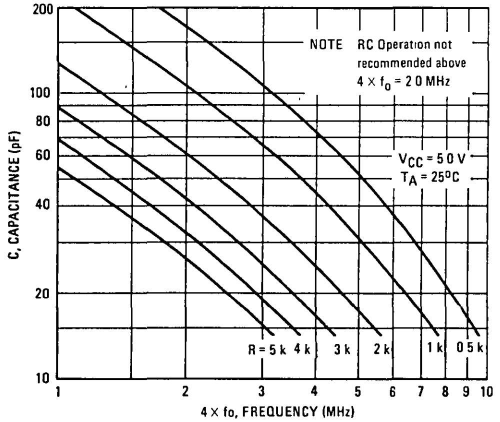


FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The V_{CC} pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 μF capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

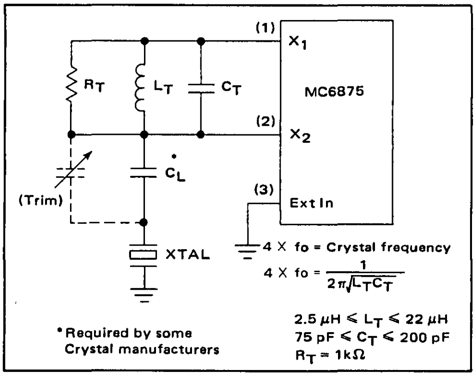
Unused inputs should be connected to V_{CC} or ground. $\overline{\text{Memory Ready}}$, $\overline{\text{DMA/Refresh Request}}$ and $\overline{\text{Power-On Reset}}$ should be connected to V_{CC} when not used. The External Input should be connected to ground when not used.

OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals X_1 and X_2 as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1kΩ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance (C_L) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and V_{CC} supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION



4 X fo = Crystal frequency

$$4 \times f_o = \frac{1}{2\pi\sqrt{L_T C_T}}$$

*Required by some Crystal manufacturers

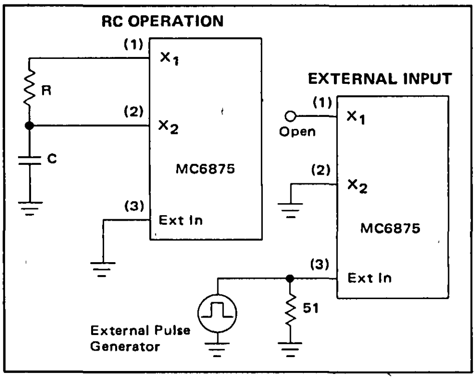
2.5 μH ≤ L_T ≤ 22 μH
75 pF ≤ C_T ≤ 200 pF
R_T = 1kΩ

TABLE 1 – OSCILLATOR COMPONENTS

TANK CIRCUIT PARAMETERS		APPROXIMATE CRYSTAL PARAMETERS				CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411	McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411	TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945
L_T µH	C_T pF	R_S Ohms	Co pF	C_1 mpF	fo MHz			
10	150	15-75	3-6	12	4.0	MP-04A * 390 pF	113-31	150-3260
4.7	82	8-45	4-7	23	8.0	MP-080 * 47 pF	113-32	150-3270

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for C_T and L_T, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (Mϕ1) is approximately:

Formula

$$4 \times \text{fo} \approx \frac{320}{C\,(R+.27)+23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at X_1 which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between X_1 and X_2.

POWER-ON RESET

As the power to the MC6875 comes up, the Reset Output will be in a high impedance state and will not give a solid V_{OL} output level until V_{CC} has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately V_{CC} = 3 V. At some V_{CC} level above that, where Reset Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the Reset Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the Power-On Reset input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the DMA/Ref Req or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the DMA/Ref Req or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the DMA/Ref Req or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING DMA/REFRESH REQUEST OR MEMORY READY INPUTS

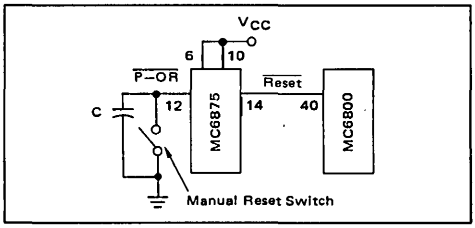
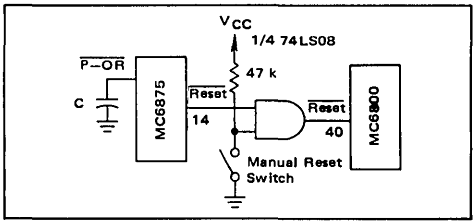


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR DMA/REFRESH REQUEST INPUTS



MOTOROLA

MC6880A
MC8T26A

This device may be ordered under either of the above type numbers.

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

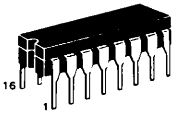
QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

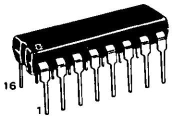
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

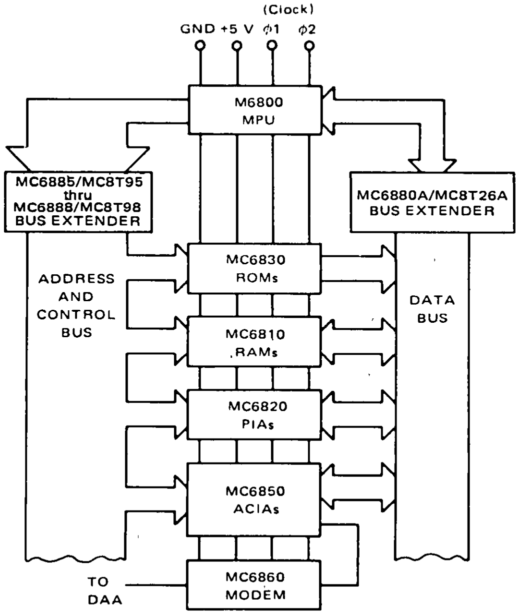


L SUFFIX
CERAMIC PACKAGE
CASE 620

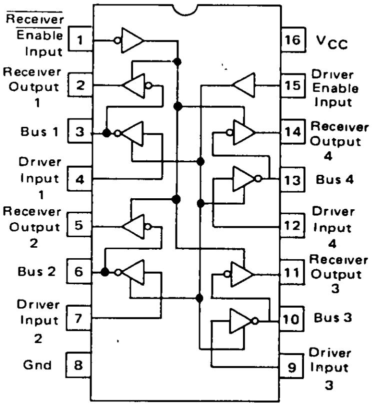


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS – MC6880A MC8T26A



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V < V_{CC} < 5.25 V and 0°C < T_A < 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (Receiver Enable Input, $V_{IL(\overline{RE})}$ = 0.4 V) (Driver Enable Input, $V_{IL(DE)}$ = 0.4 V) (Driver Input, $V_{IL(D)}$ = 0.4 V) (Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	 $I_{IL(\overline{RE})}$ $I_{IL(DE)}$ $I_{IL(D)}$ $I_{IL(B)}$	 – – – –	 – – – –	 -200 -200 -200 -200	 µA
Input Disabled Current — Low Logic State (Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	 –	 –	 -25	 µA
Input Current-High Logic State (Receiver Enable Input, $V_{IH(\overline{RE})}$ = 5.25 V) (Driver Enable Input, $V_{IH(DE)}$ = 5.25 V) (Driver Input, $V_{IH(D)}$ = 5.25 V) (Receiver Input, $V_{IH(B)}$ = 5.25 V)	 $I_{IH(\overline{RE})}$ $I_{IH(DE)}$ $I_{IH(D)}$ $I_{IH(B)}$	 – – – –	 – – – –	 25 25 25 100	 µA
Input Voltage — Low Logic State (Receiver Enable Input) (Driver Enable Input (Driver Input) (Receiver Input)	 $V_{IL(\overline{RE})}$ $V_{IL(DE)}$ $V_{IL(D)}$ $V_{IL(B)}$	 – – – –	 – – – –	 0.85 0.85 0.85 0.85	 V
Input Voltage — High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	 $V_{IH(\overline{RE})}$ $V_{IH(DE)}$ $V_{IH(D)}$ $V_{IH(B)}$	 2.0 2.0 2.0 2.0	 – – – –	 – – – –	 V
Output Voltage — Low Logic State (Bus Driver) Output, $I_{OL(B)}$ = 48 mA) (Receiver Output, $I_{OL(R)}$ = 20 mA)	 $V_{OL(B)}$ $V_{OL(R)}$	 – –	 – –	 0.5 0.5	 V
Output Voltage — High Logic State (Bus (Driver) Output, $I_{OH(B)}$ = −10 mA) (Receiver Output, $I_{OH(R)}$ = −2.0 mA) (Receiver Output, $I_{OH(R)}$ = −100 µA, V_{CC} = 5.0 V)	 $V_{OH(B)}$ $V_{OH(R)}$ 	 2.4 2.4 3.5	 3.1 3.1 –	 – – –	 V
Output Disabled Leakage Current — High Logic State (Bus Driver) Output, $V_{OH(B)}$ = 2.4 V) (Receiver Output, $V_{OH(R)}$ = 2.4 V)	 $I_{OHL(B)}$ $I_{OHL(R)}$	 – –	 – –	 100 100	 µA
Output Disabled Leakage Current — Low Logic State (Bus Output, $V_{OL(B)}$ = 0.5 V) (Receiver Output, $V_{OL(R)}$ = 0.5 V)	 $I_{OLL(B)}$ $I_{OLL(R)}$	 – –	 – –	 −100 −100	 µA
Input Clamp Voltage (Driver Enable Input $I_{ID(DE)}$ = −12 mA) (Receiver Enable Input $I_{IC(RE)}$ = +12 mA) (Driver Input $I_{IC(D)}$ = −12 mA)	 $V_{IC(DE)}$ $V_{IC(RE)}$ $V_{IC(D)}$	 – – –	 – – –	 -1.0 -1.0 -1.0	 V
Output Short-Circuit Current, V_{CC} = 5.25 V (1) (Bus (Driver) Output) (Receiver Output)	 $I_{OS(B)}$ $I_{OS(R)}$	 -50 -30	 – –	 -150 -75	 mA
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at T_A = 25°C and V_{CC} = 5.0 V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

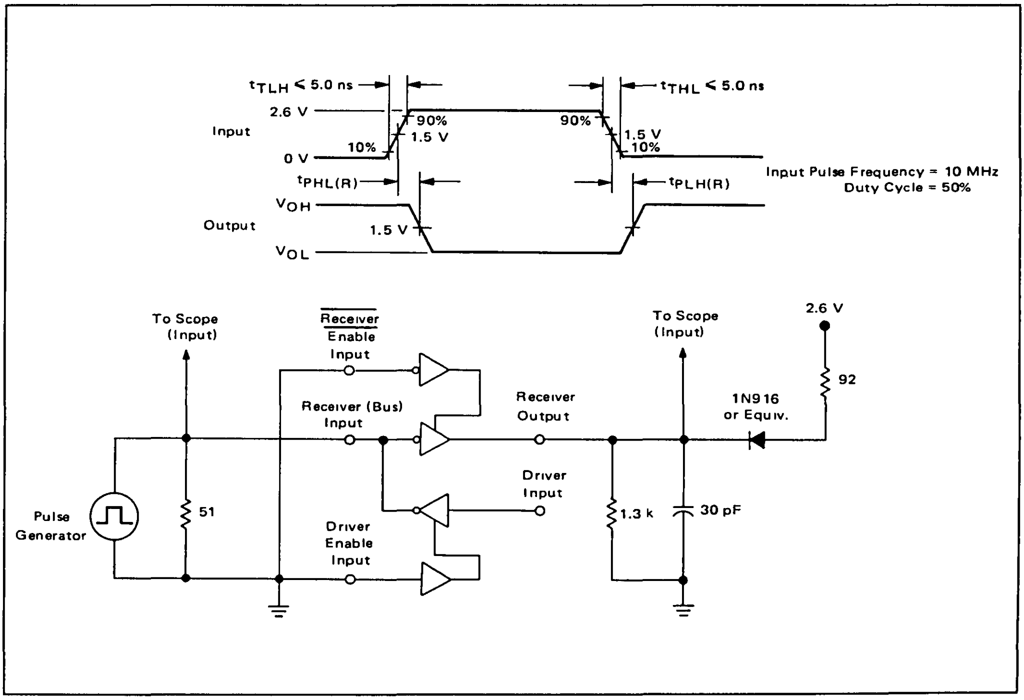


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

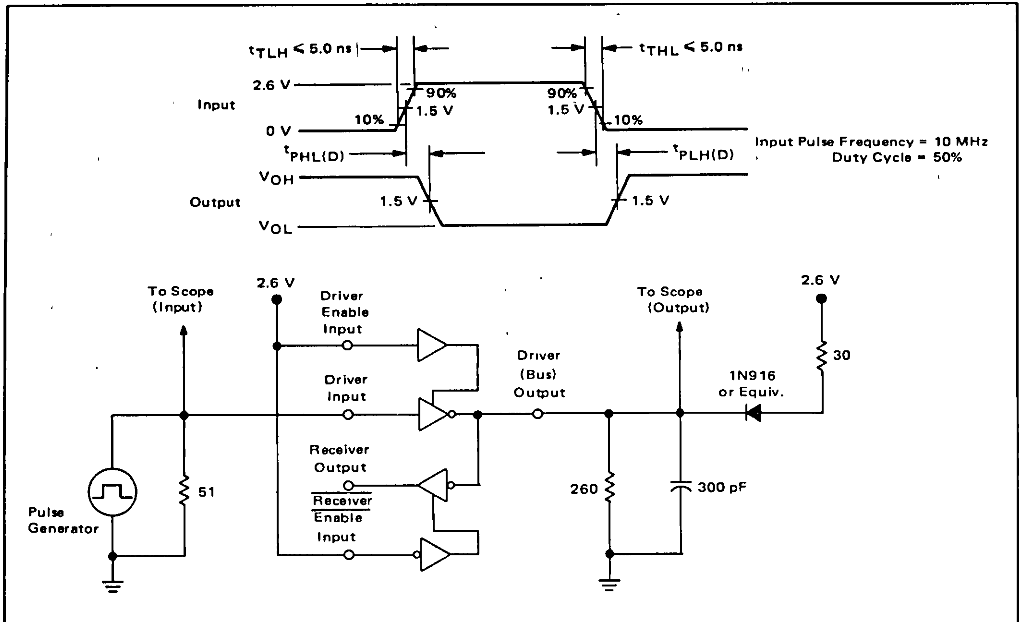


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

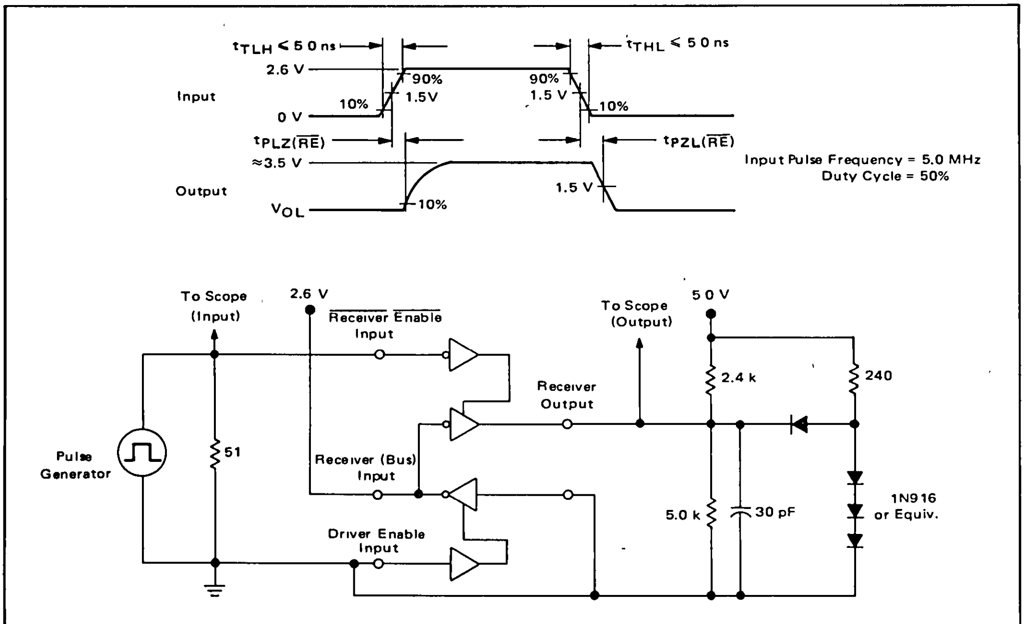


FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

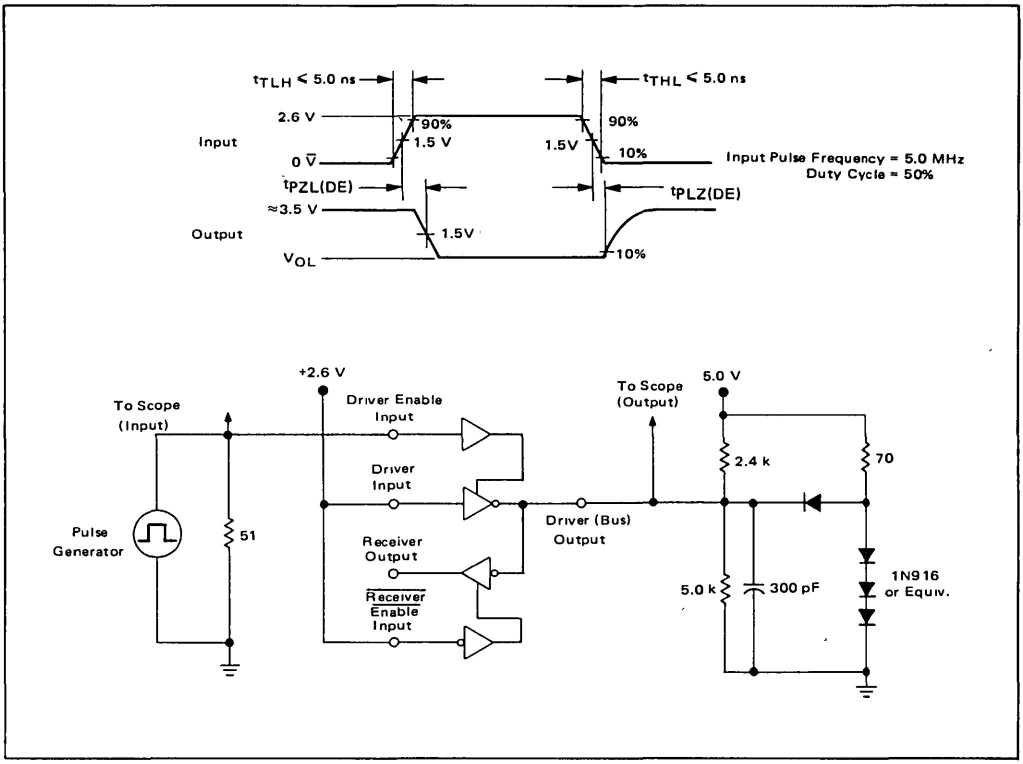
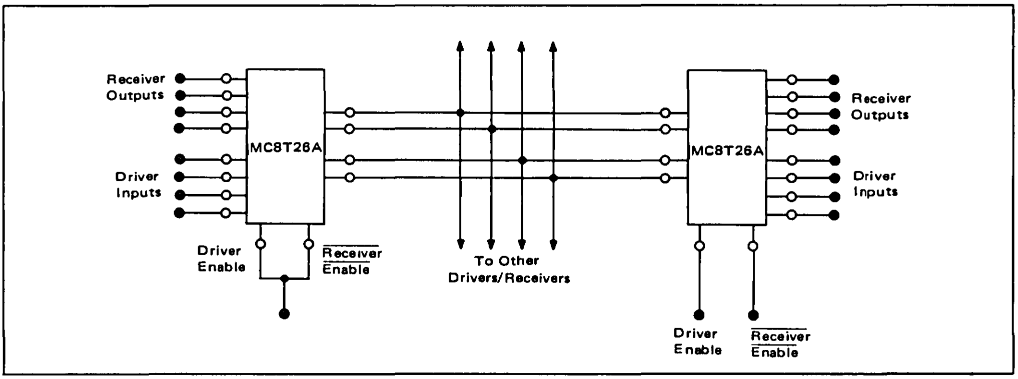


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



MOTOROLA

MC6881
MC3449

This device may be ordered under either of the above type numbers.

TRIPLE BI-DIRECTIONAL BUS SWITCH

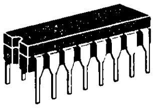
The MC6881/3449 is a three channel, non-inverting, bi-directional Bus Extender. It is designed to allow the bi-directional exchange of TTL level digital information between a selected pair of ports in a three port network. All three ports of each channel may be forced to a high impedance condition through that channel's $\overline{\text{Enable}}$ input.

Port pair selection and listener/talker status for the three channels is determined through the Control and Select inputs. All inputs are PNP buffered, M6800 Family compatible, and protected with Schottky-Barrier diode clamps to suppress undershoot voltages.

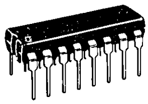
A summary of MC6881/3449 features include:

- Three Channels
- Non-Inverting Data Exchange
- Bi-Directional Operation
- Active Pull-Up with Three-State Capability
- High Impedance Inputs
- TTL Compatible
- High Speed Schottky Technology
- Single Power Supply

BI-DIRECTIONAL BUS EXTENDER/SWITCH



L SUFFIX
CERAMIC PACKAGE
CASE 620



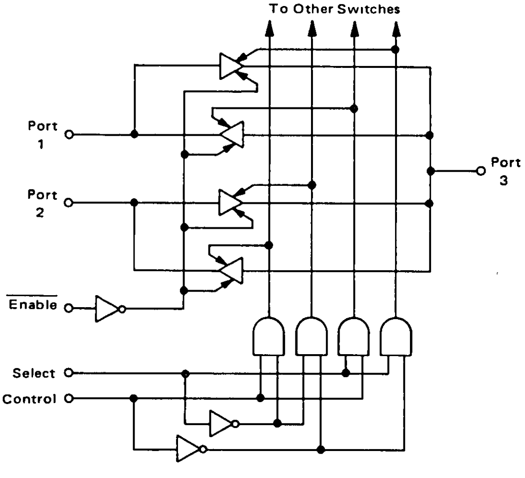
P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

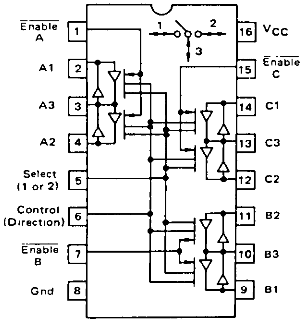
$\overline{\text{Enable}}$	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS (Unless otherwise noted T_A = 25°C.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25 Volts and T_A = 0 to +70°C unless otherwise noted.)

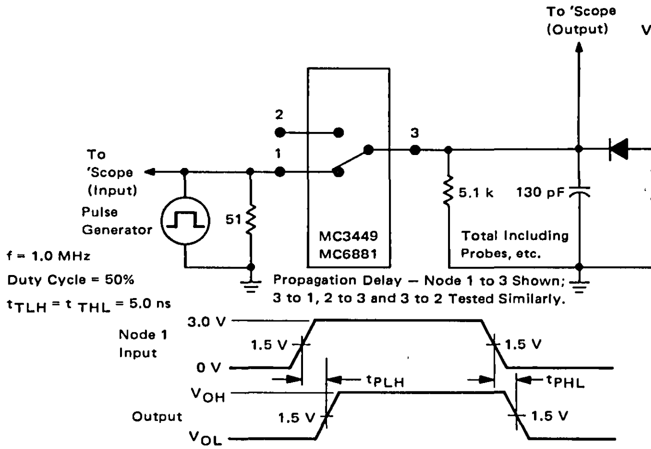
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–	-100	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.25 V)	I_{IH}	 – –	 – –	 40 100	µA
Input Clamp Voltage (I_{IC} = -18 mA)	V_{IC}	–	–	-1.5	Vdc
Output Voltage – Low Logic State (I_{OL} = 8.0 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = -400 µA)	V_{OH}	2.7	–	–	V
Output Disabled Leakage Current (V_{OZ} = 0.4 V) (V_{OZ} = 2.7 V) (V_{OZ} = 5.25 V)	I_{OZ}	 – – –	 – – –	 -40 40 100	µA
Output Short Circuit Current	I_{OS}	-20	–	-55	mA
Crosstalk Current – Low Logic State (V_{IH} = 2.4 V on Node 3, opposite node selected V_{IL} = 0.4 V on node tested)	I_{XL}	–	–	-40	µA
Crosstalk Current – High Logic State (V_{IL} = 0.8 V on Node 3, opposite node selected V_{IH} = 2.4 V on node tested).	I_{XH}	–	–	40	µA
Power Supply Current (V_{IH} = 2.4 V, V_{CC} = 5.25 V)	I_{CC}	–	–	70	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V and T_A = 25°C unless otherwise noted.)

Propagation Delay Times – Nodes 1, 2, 3 Low-to-High Output High-to-Low Output	 t_{PLH} t_{PHL}	 – –	 30 24	 – –	ns
Enable Delay Times Disabled to High or Low-Logic State High or Low-Logic State to Disabled	 t_{EN} t_{DIS}	 – –	 18 10	 – –	ns
Select Delay Times Third-State to High or Low-Logic State High or Low-Logic State to Third-State	 t_{ON} t_{OFF}	 – –	 25 25	 – –	ns
Control Delay Times Third-State to High or Low-Logic State High or Low-Logic State to Third-State	 t_{ON} t_{OFF}	 – –	 25 25	 – –	ns

PROPAGATION DELAY TIME TEST CIRCUITS AND WAVEFORMS

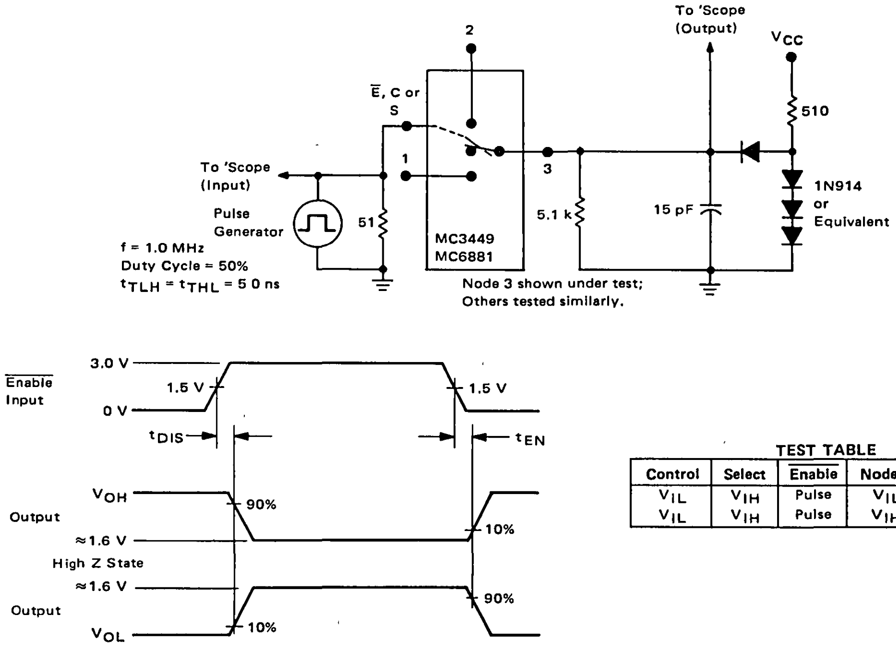
FIGURE 1 – NODE TO OUTPUT



$\overline{\text{Enable}}$ = Gnd
Select = V_{IH}
Control = Gnd
Node 2 = Open

Input Pulse Characteristics
f = 1.0 MHz, 50% Duty Cycle
$t_{TLH} = t_{THL} = 5.0$ ns
All voltages referenced to Gnd.

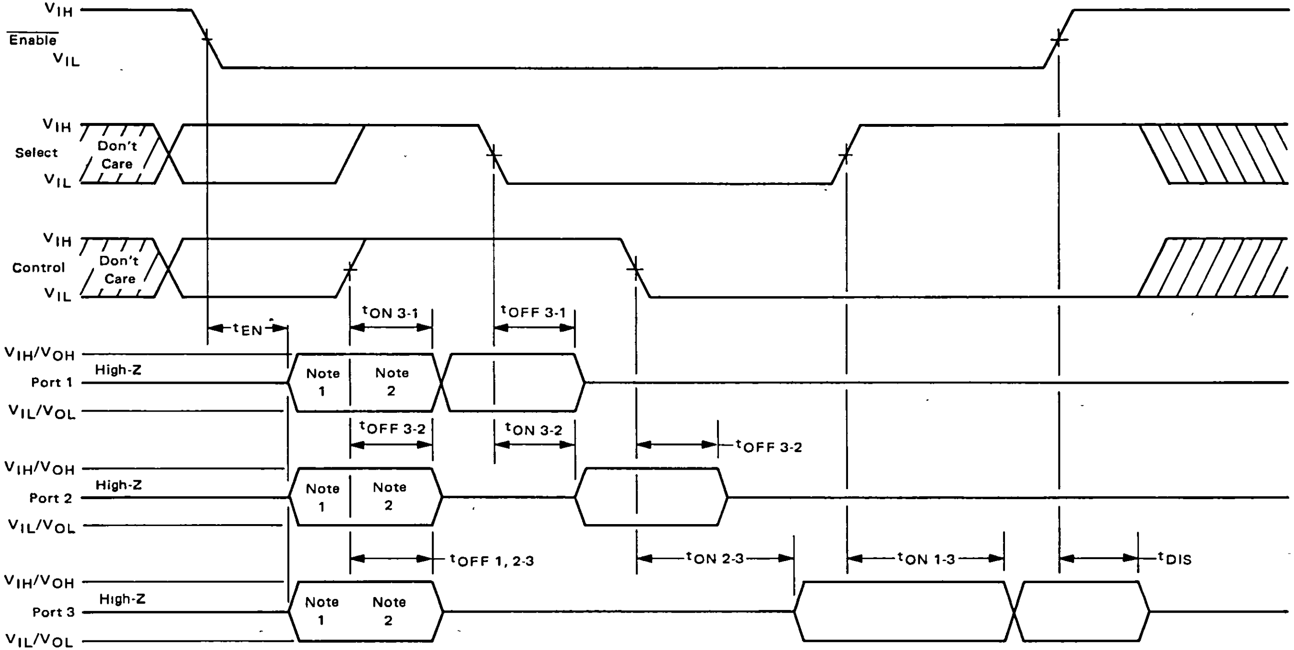
FIGURE 2 – THIRD-STATE



TEST TABLE

Control	Select	$\overline{\text{Enable}}$	Node 1	Test
V_{IL}	V_{IH}	Pulse	V_{IL}	t_{EN}/t_{DIS}
V_{IL}	V_{IH}	Pulse	V_{IH}	t_{EN}/t_{DIS}

FIGURE 3 – TIMING DIAGRAM



Note 1: Data is transmitted to only 1 of the 3 ports. Which port acts as an output depends on logic state of the select and control pins when the channel is enabled.

Note 2: A port chosen to act as the output is either high or low, depending on the logic state of the port chosen to be the input.

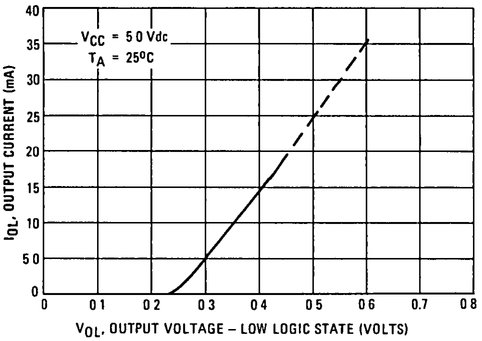
Note 3. The arrow indicates the direction of data flow. Each buffer is non-inverting, so data maintains the same logic state through the buffer.

Note 4: t_{ON} is the time from third state to active (high or low) state, t_{OFF} is time from active to third state.

TRUTH TABLE

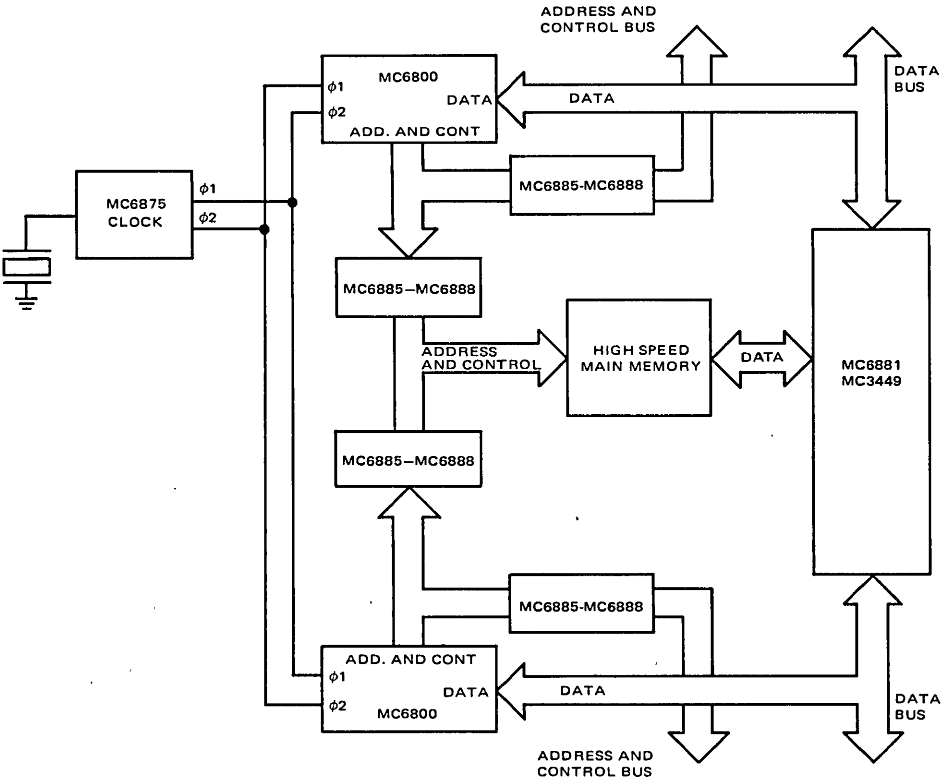
$\overline{\text{Enable}}$	Select	Control	Data Direction (Note 3)
1	X	X	All Ports are High-Z
0	0	0	Port 2 → Port 3
0	0	1	Port 3 → Port 2
0	1	0	Port 1 → Port 3
0	1	1	Port 3 → Port 1

FIGURE 4 – TYPICAL I_{OL} versus V_{OL}



TYPICAL APPLICATION

FIGURE 5 – TWO MPUs SHARING A COMMON MAIN-MEMORY

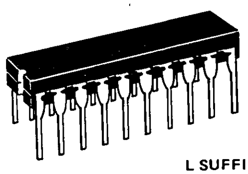


MOTOROLA

MC6882A/MC3482A
MC6882B/MC3482B

This device may be ordered under
either of the above type numbers.

OCTAL THREE-STATE BUFFER/LATCH



L SUFFIX
CASE 732

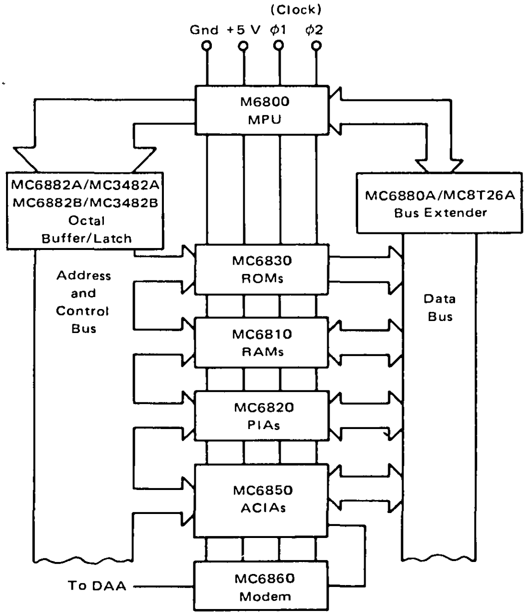
Advance Information

OCTAL THREE-STATE BUFFER/LATCH

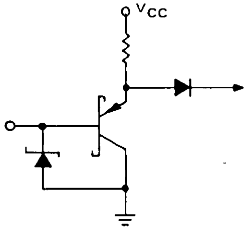
This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

- Inverting and Non-Inverting Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All Inputs Have Hysteresis to Improve Noise Rejection
- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

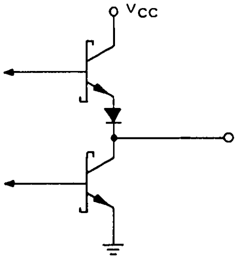
MICROPROCESSOR BUS EXTENDER APPLICATION



INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J		°C
Plastic Package		150	
Ceramic Package		175	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^\circ C \leqslant T_A \leqslant 75^\circ C$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current — High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	µA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{OE})}$ = 0.5 V)	I_{IL}	–	–	−250	µA
Output Voltage — High Logic State (V_{CC} = 4.75 V, I_{OH} = −20 mA)	V_{OH}	2.4	–	–	V
Output Voltage — Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current — High Impedance State	I_{OZ}				µA
(V_{CC} = 5.25 V, V_{OH} = 2.4 V)		–	–	100	
(V_{CC} = 5.25 V, V_{OL} = 0.5 V)		–	–	−100	
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	−30	−80	−130	mA
Power Supply Current (V_{CC} = 5 25 V) MC6882A/MC3482A	I_{CC}	–		130	mA
MC6882B/MC3482B				150	
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IK} = −12 mA)	V_{IK}	–	–	−1.2	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

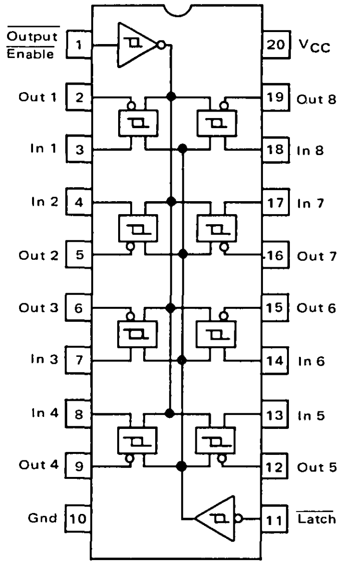
Characteristics	Symbol	MC6882A/ MC3482A			MC6882B/ MC3482B			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Times								ns
Data to Output								
Low to High	$t_{PLH(D)}$							
C_L = 50 pF		–	10	–	–	12	–	
C_L = 250 pF		–	–	–	–	–	–	
C_L = 375 pF		–	–	–	–	–	–	
C_L = 500 pF		–	21	–	–	20	–	
High to Low	$t_{PHL(D)}$							
C_L = 50 pF		–	8.0	–	–	10	–	
C_L = 250 pF		–	–	–	–	–	–	
C_L = 375 pF		–	–	–	–	–	–	
C_L = 500 pF		–	17	–	–	18	–	
Propagation Delay Times								ns
Latch Disable (Low to High) to Output								
Low to High	$t_{PLH(L)}$							
C_L = 50 pF		–	17	–	–	22	–	
High to Low	$t_{PHL(L)}$							
C_L = 50 pF		–	19	–	–	17	–	
Propagation Delay Times								ns
(C_L = 20 pF)								
High Output Level to High Impedance	$t_{PHZ(\overline{OE})}$	–	7.0	–	–	7.0	–	
Low Output to High Impedance	$t_{PLZ(\overline{OE})}$	–	18	–	–	18	–	
High Impedance to High Output	$t_{PZH(\overline{OE})}$	–	8.0	–	–	15	–	
High Impedance to Low Output	$t_{PZL(\overline{OE})}$	–	12	–	–	9.0	–	

AC SETUP CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC6882A/ MC3482A			MC6882B/ MC3482B			Unit
		Min	Typ	Max	Min	Typ	Max	
Setup Time (Data to Negative Going Latch Enable)	$t_{su(D)}$	–	0	–	–	0	–	ns
Hold Time (Data to Negative Going Latch Enable)	$t_{h(D)}$	–	11	–	–	11	–	ns
Minimum Latch Enable Pulse Width (High or Low)	$t_{W(L)}$	–	15	–	–	15	–	ns

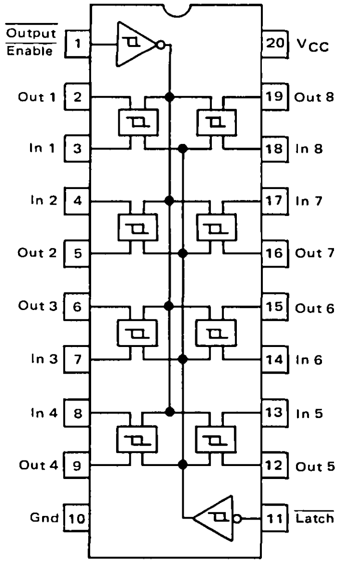
PIN CONNECTIONS AND TRUTH TABLES

MC6882A/MC3482A



$\overline{\text{Output Enable}}$	$\overline{\text{Latch}}$	Input	Output
0	1	0	1
0	1	1	0
0	0	X	Q_o
1	X	X	Z

MC6882B/MC3482B



$\overline{\text{Output Enable}}$	$\overline{\text{Latch}}$	Input	Output
0	1	0	0
0	1	1	1
0	0	X	Q_o
1	X	X	Z

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

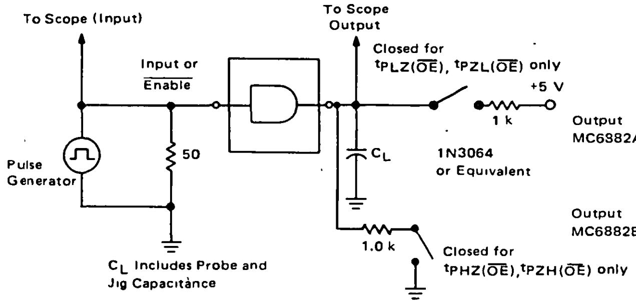
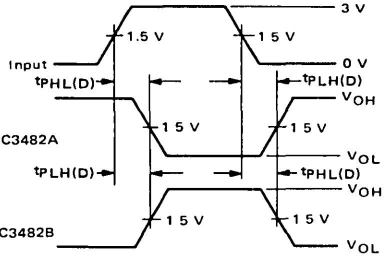


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES DATA TO OUTPUT



Input Pulse Conditions
$t_{THL} = t_{TLH} \leq 5$ ns
f - 1.0 MHz

FIGURE 3 – WAVE FORMS FOR AC SETUP AND LATCH DISABLE TO OUTPUT DELAY

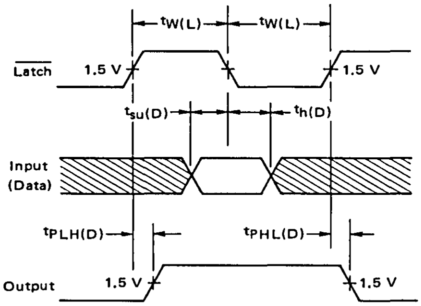
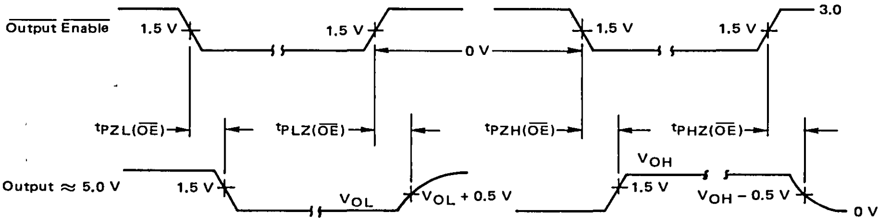


FIGURE 4 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{OUTPUT ENABLE}}$ TO OUTPUT



MOTOROLA

MC6885/MC8T95
MC6886/MC8T96
MC6887/MC8T97
MC6888/MC8T98

This device may be ordered under either of the above type numbers.

HEX THREE-STATE BUFFER INVERTERS

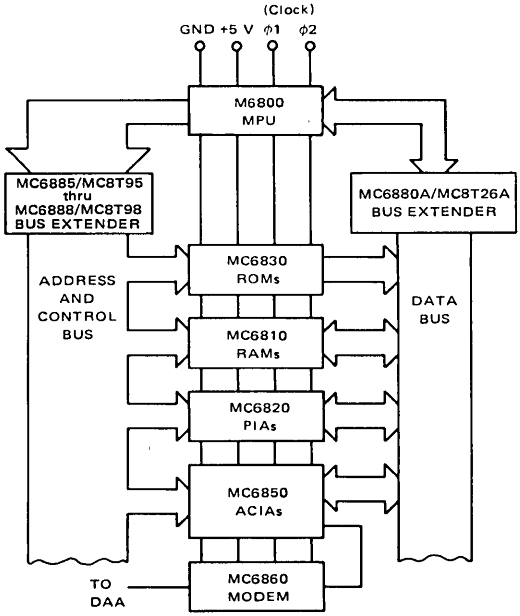
This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

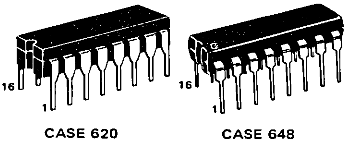
The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

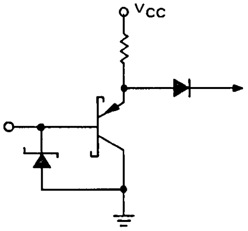
MICROPROCESSOR BUS EXTENDER APPLICATION



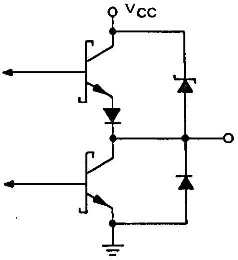
HEX THREE-STATE BUFFER/INVERTERS



INPUT EQUIVALENT CIRCUIT

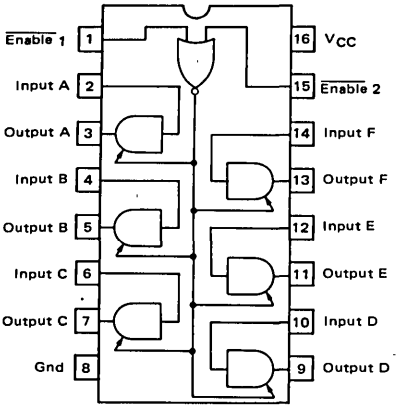


OUTPUT EQUIVALENT CIRCUIT



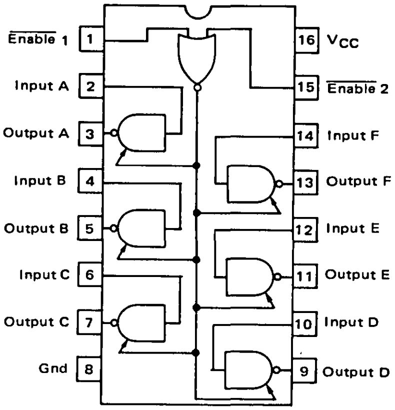
PIN CONNECTIONS AND TRUTH TABLES

MC6885/MC8T95



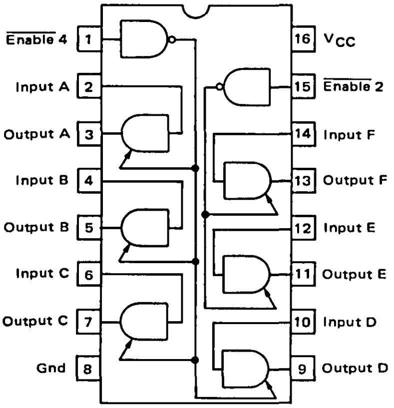
$\overline{\text{Enable}}$ 2	$\overline{\text{Enable}}$ 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

MC6886/MC8T96



$\overline{\text{Enable}}$ 2	$\overline{\text{Enable}}$ 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

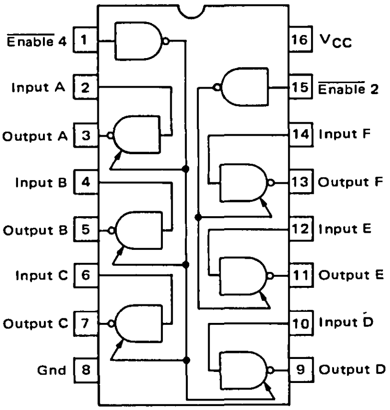
MC6887/MC8T97



$\overline{\text{Enable}}$	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC6888/MC8T98



$\overline{\text{Enable}}$	Input	Output
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 150 175	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^{\circ}C \leqslant T_A \leqslant 75^{\circ}C$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current – High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	µA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V)	I_{IL}	–	–	-400	µA
Input Current – High Impedance State (V_{CC} = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$= 2.0 V)	$I_{IH(\overline{E})}$	–	–	-40	µA
Output Voltage – High Logic State (V_{CC} = 4.75 V, I_{OH} = -5.2 mA)	V_{OH}	2.4	–	–	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current – High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	I_{OZ}	 – –	 – –	 40 -40	µA
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current (V_{CC} = 5.25 V) MC8T95, MC8T97, MC6885, MC6887 MC8T96, MC8T98, MC6886, MC6888	I_{CC}	 – –	 65 59	 98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	–	–	1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = -12 mA)	V_{OC}	–	–	-1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	5.5	–	–	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87			MC8T96/98 MC6886/88			Unit
		Min	Typ	Max	Min	Typ	Min	
Propagation Delay Time – High to Low State (C_L = 50 pF) (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{PHL}	 3.0 – – –	 – 16 20 23	 12 – – –	 4.0 – – –	 – 15 18 22	 11 – – –	ns
Propagation Delay Time – Low to High State (C_L = 50 pF) (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{PLH}	 3.0 – – –	 – 25 33 42	 13 – – –	 3.0 – – –	 – 22 28 35	 10 – – –	ns
Transition Time – High to Low State (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{THL}	 – – –	 10 11 14	 – – –	 – – –	 10 13 15	 – – –	ns
Transition Time – Low to High State (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{TLH}	 – – –	 32 42 60	 – – –	 – – –	 28 38 53	 – – –	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87			MC8T96/98 MC6886/88			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time – High State to Third State (C_L = 5.0 pF)	$t_{PHZ(\overline{E})}$	3.0	–	10	3.0	–	10	ns
Propagation Delay Time – Low State to Third State (C_L = 5.0 pF)	$t_{PLZ(\overline{E})}$	3.0	–	12	5.0	–	16	ns
Propagation Delay Time – Third State to High State (C_L = 50 pF)	$t_{PZH(\overline{E})}$	8.0	–	25	7.0	–	22	ns
Propagation Delay Time – Third State to Low State (C_L = 50 pF)	$t_{PZL(\overline{E})}$	12	–	25	11	–	24	ns

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

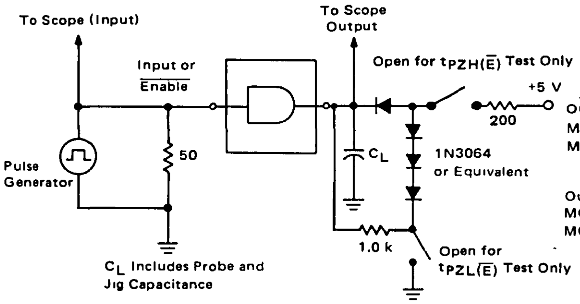


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

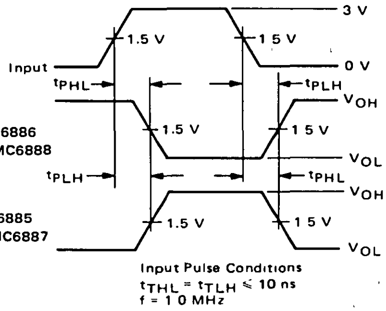
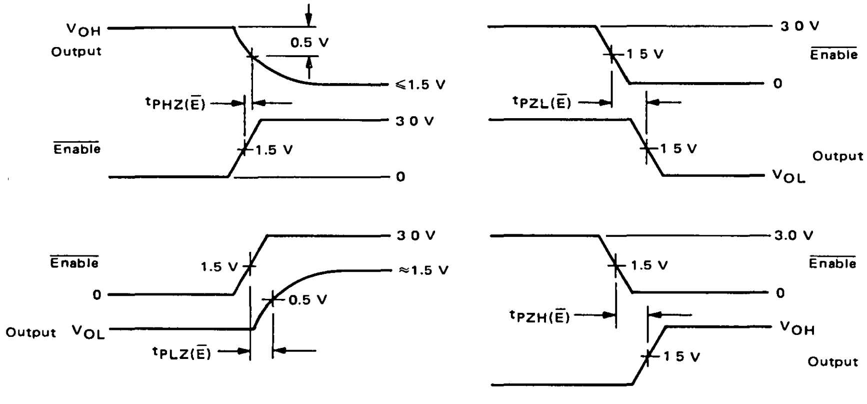
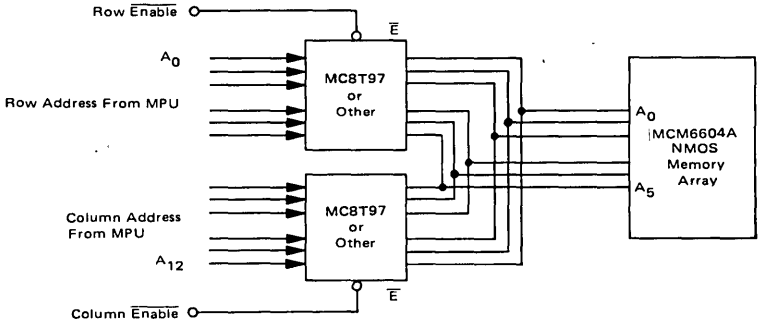


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT



H = High-Logic State, L = Low-Logic State, Z = High Impedance State

FIGURE 4 – ADDRESS MULTIPLEXER FOR 16-PIN 4K NMOS MEMORY



MOTOROLA

MC6889
MC8T28

This device may be ordered under either of the above type numbers.

NON-INVERTING QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

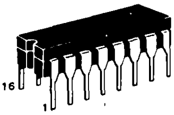
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

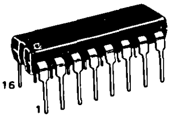
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

NON-INVERTING BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

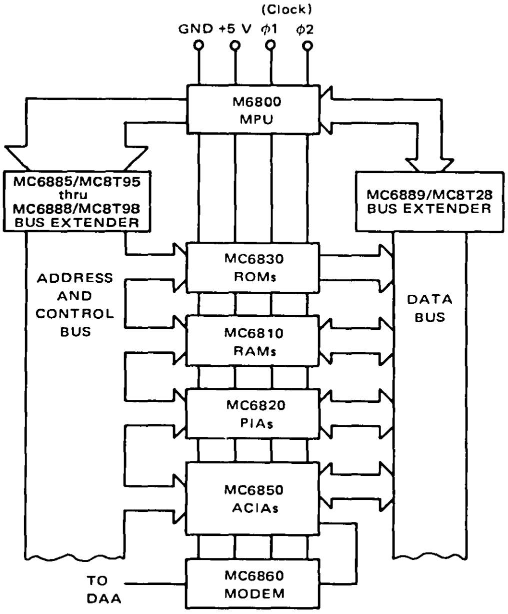


L SUFFIX
CERAMIC PACKAGE
CASE 620

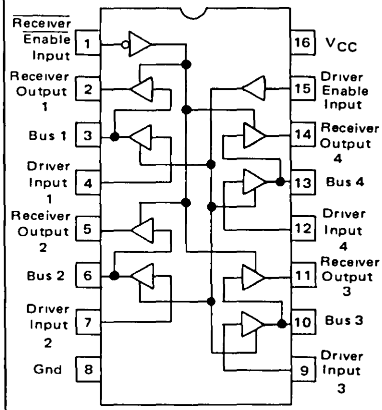


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS – MC6889 MC8T28



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V < V_{CC} < 5.25 V and 0°C < T_A < 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State					
(Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current — Low Logic State (Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
Input Voltage — Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage — High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage — Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage — High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = −10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = −2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = −100 μA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current — High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current — Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	-100	μA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	-100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = −12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = −12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	110	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver (C_L = 30 pF)	$t_{PLH(R)}$ $t_{PHL(R)}$	–	17 17	ns
Propagation Delay Time—Driver (C_L = 300 pF)	$t_{PLH(D)}$ $t_{PHL(D)}$	–	17 17	ns
Propagation Delay Time—Enable (C_L = 30 pF) – Receiver	$t_{PZL(R)}$ $t_{PLZ(R)}$	– –	23 18	ns
– Driver Enable (C_L 300 pF)	$t_{PZL(D)}$ $t_{PLZ(D)}$	– –	28 23	

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

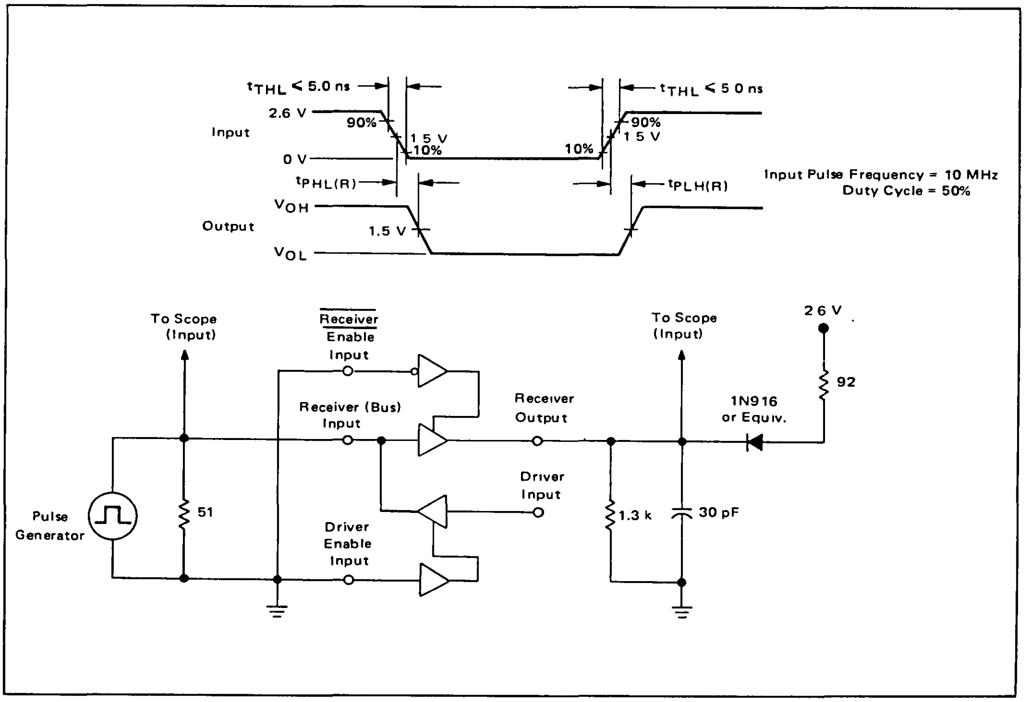
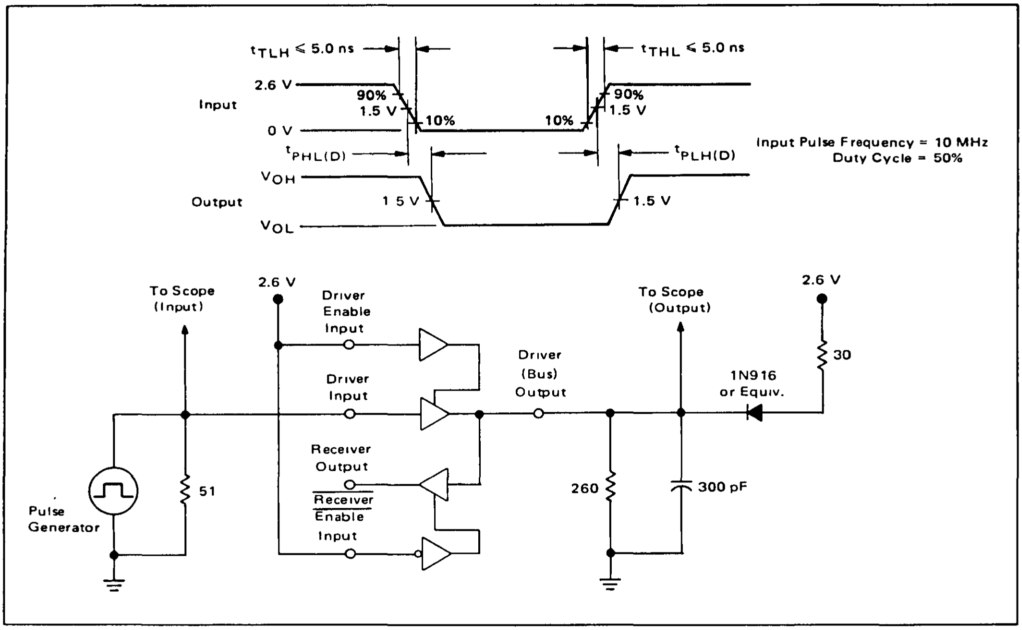
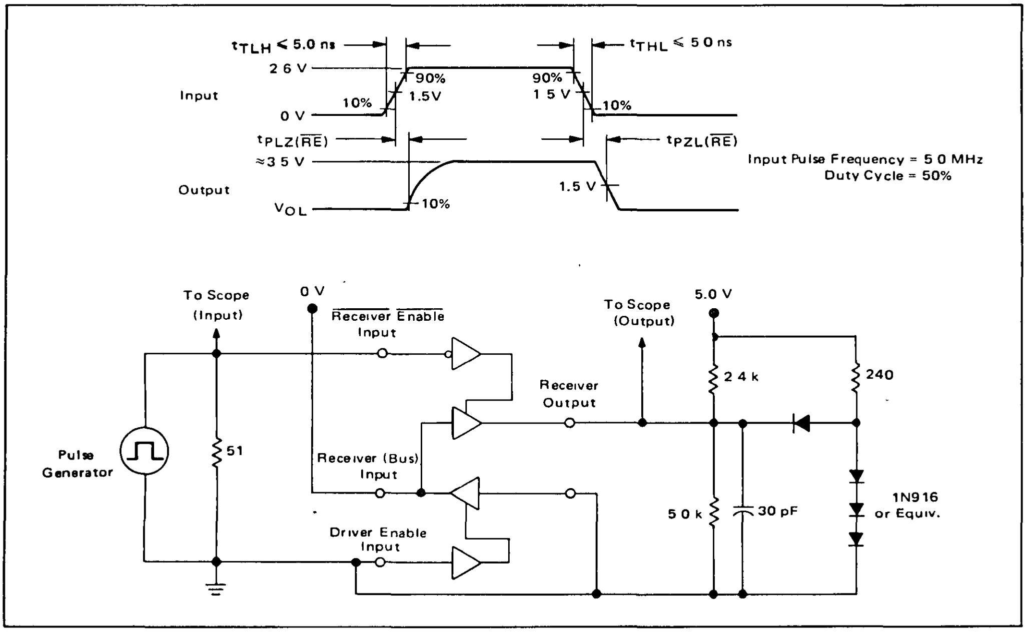


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$



Input Pulse Frequency = 10 MHz
Duty Cycle = 50%

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



Input Pulse Frequency = 5 0 MHz
Duty Cycle = 50%

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

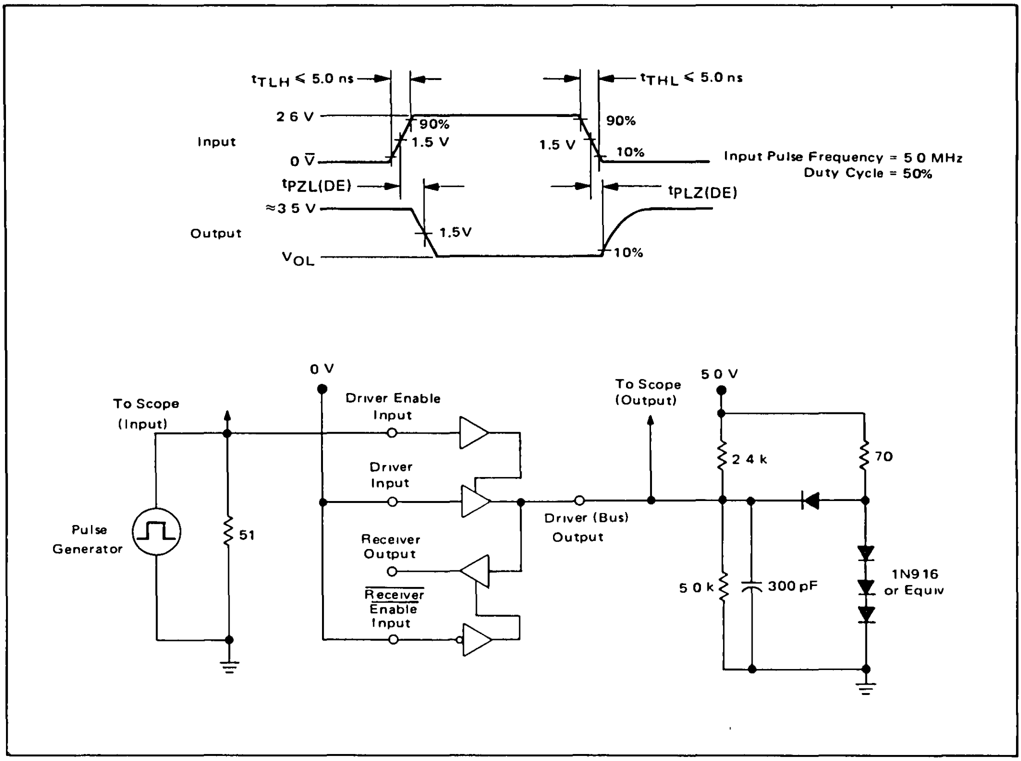
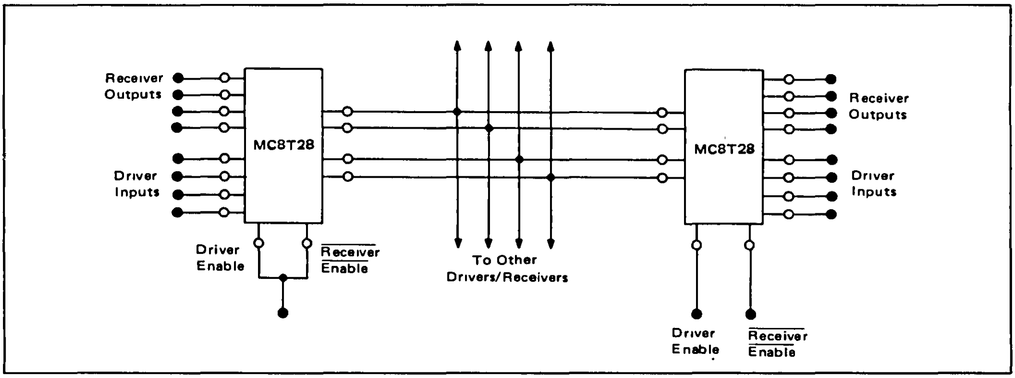


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



MOTOROLA

MC6890

FOR COMPLETE DATA
SEE PAGE 8-61

Product Preview

BUS-COMPATIBLE 8-BIT MPU D-TO-A CONVERTER

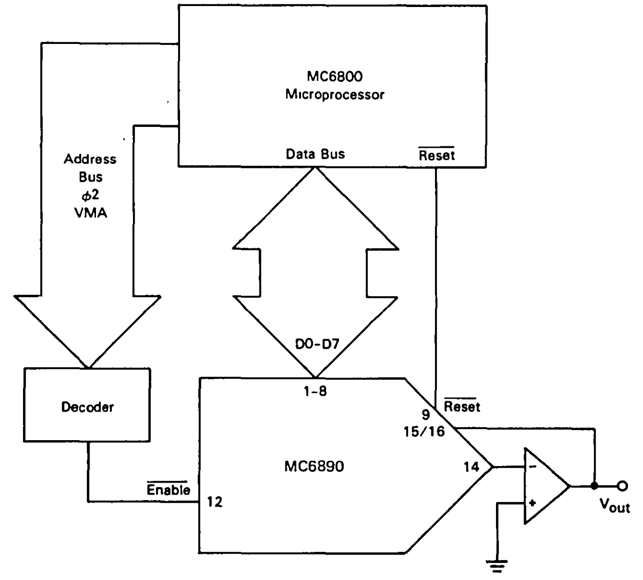
The MC6890 is a self-contained, bus-compatible, 8-bit (± 0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high-stability, laser-trimmed, thin-film resistors for both reference input and output span and offset control.

A reset pin provides for overriding stored data and forcing I_{out} to zero.

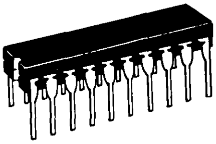
- ±1/2 LSB Nonlinearity
- Available in Military Temperature Range
- Direct Data Bus Link
- Low Power: 130 mW Typ
- Fast Settling Time. 140 ns Typ
- Single Enable: 10 ns Max Data Hold Time
- Self-Contained 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Reset Pin to Override Data
- Output Voltage Ranges: +5 0, +10, +20, or ±2.5, ±5.0, ±10 Volts

OPERATION WITH MC6800



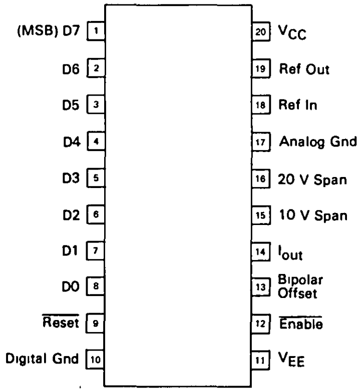
This is advance information and specifications are subject to change without notice.

8-BIT BUS-COMPATIBLE MPU DAC



L SUFFIX
CASE 732

PIN CONNECTIONS



MOTOROLA

MC75365

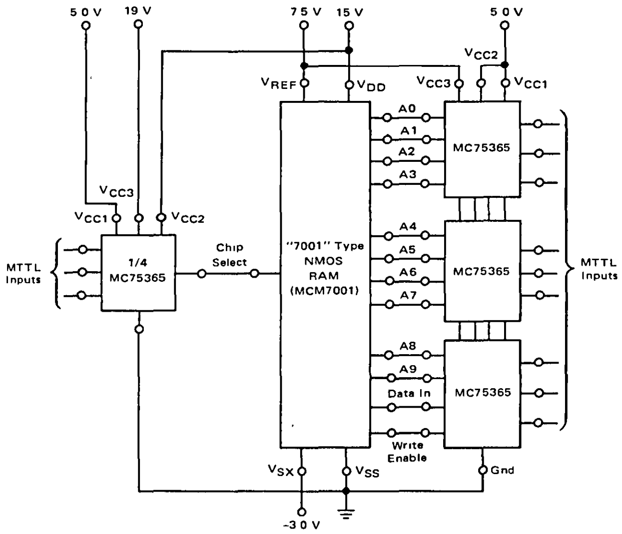
Specifications and Applications Information

QUAD MOS CLOCK DRIVER OR HIGH-VOLTAGE, HIGH-CURRENT NAND DRIVER

The MC75365 is intended for driving the highly capacitive Address, Control and Timing inputs on a variety of MOS RAMs such as the "1103" and "7001" types. It is designed to operate from the MTTL 5.0 V power supply and the V_{SS} and V_{BB} power supplies used with the memories in most applications. Operation is recommended at $V_{CC3} \simeq V_{CC2} + 3$ V, but the part is useable over a wide latitude of supply voltages. V_{CC2} may be tied directly to V_{CC3} in many conditions.

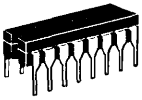
- Pin Compatible with Intel 3207 and Interchangeable with T. I. SN75365
- MTTL and MDTL Compatible, Diode-Clamped Inputs
- Two Common Enable Inputs per Gate Pair
- Low Standby Power Consumption Transient
- Capable of Driving High Capacitive Loads
- Fast Switching Operation

TYPICAL APPLICATION
with "7001" Type 1 K RAM

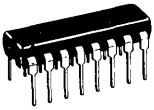


QUAD MOS CLOCK DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUITS

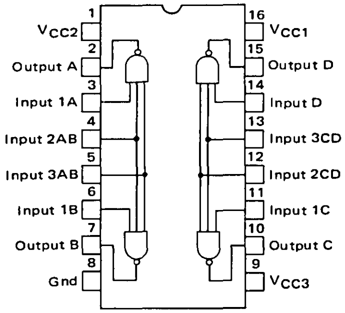


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

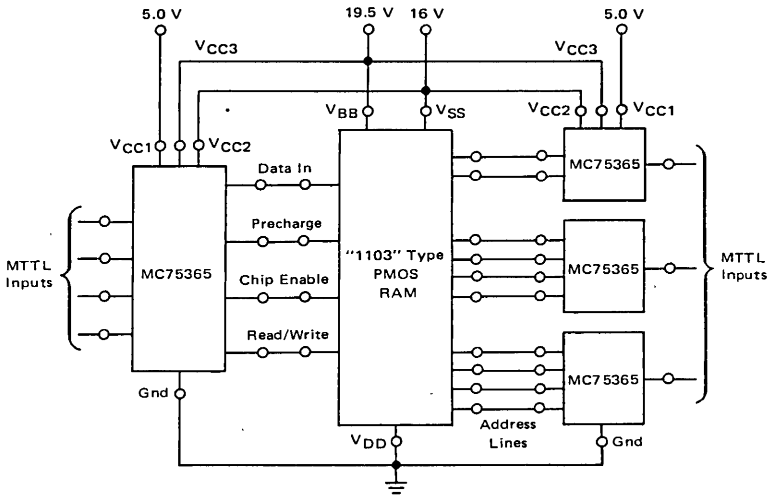


TRUTH TABLE

INPUT			OUTPUT
1	2	3	
H	H	H	L
L	I	I	H
I	L	I	H
I	I	L	H

Where:
H = High Logic State
L = Low Logic State
I = I = Irrelevant

TYPICAL APPLICATION
with "1103" Type 1 K RAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	-0.5 to 7.0 -0.5 to 25 -0.5 to 30	V
Input Voltage	V_I	5.5	V
Input Differential Voltage (see Note 1)	V_{ID}	5.5	V
Power Dissipation (Package Limitation) Ceramic Package @ T_A = 25°C Derate above T_A = 25°C Plastic Package @ T_A = 25°C Derate above T_A = 25°C Ceramic Package @ T_C = 25°C Derate above T_C = 25°C Plastic Package @ T_C = 25°C Derate above T_C = 25°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JC}$	 1000 6 6 830 6 6 3.0 20 1.8 14	 mW mW/°C mW mW/°C Watts mW/°C Watts mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. This is the differential voltage between any two inputs to any single gate.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	4.75 4.75 V_{CC2}	5 0 20 24	5.25 24 28	V
Difference between V_{CC3} and V_{CC2}	V_{CC3}-V_{CC2}	0	4.0	10	V
Operating Temperature Range	T_A	0	–	70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V, V_{CC3} = 24 V, C_L = 200 pF, R_D = 24Ω, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	1.5	V
Input Current — Maximum Input Voltage (V_{IH} = 5.5 V)	I_{IH1}	–	–	1.0	mA
Input Current — High Logic State (V_{IH} (1) = 2.4 V) (V_{IH} (2) or V_{IH} (3) = 2.4 V)	I_{IH2}	 – –	 – –	 40 80	µA
Input Current — Low Logic State (V_{IL} (1) = 0.4 V) (V_{IL} (2) or V_{IL} (3) = 0.4 V)	I_{IL}	 – –	 -1.0 -2.0	 -1.6 -3.2	mA
Output Voltage — High Logic State ($V_{CC3} = V_{CC2} + 3.0$ V, V_{IL} = 0.8 V, I_{OH} = -100 µA) ($V_{CC3} = V_{CC2} + 3.0$ V, V_{IL} = 0.8 V, I_{OH} = -10 mA) ($V_{CC3} = V_{CC2}$, V_{IL} = 0.8 V, I_{OH} = -50 µA) ($V_{CC3} = V_{CC2}$, V_{IL} = 0.8 V, I_{OH} = -10 mA)	 V_{OH1} V_{OH2} V_{OH3} V_{OH4}	 V_{CC2} -0.3 V_{CC2} -1.2 V_{CC2} -1.0 V_{CC2} -2.3	 V_{CC2} -0.1 V_{CC2} -0.9 V_{CC2} -0.7 V_{CC2} -1.8	 – – – –	V
Output Clamp Voltage (V_{IL} = 0 V, I_{OC} = 20 mA)	V_{OC}	–	–	V_{CC2} +1.5	V
Output Voltage — Low Logic State (V_{IH} = 2.0 V, I_{OL} = 10 mA) (15 V ≤ V_{CC3} ≤ 28 V, V_{IH} = 2.0 V, I_{OL} = 40 mA)	 V_{OL1} V_{OL2}	 – –	 0.15 0.25	 0.3 0.5	V
Power Supply Currents — Outputs High Logic State (V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, V_{IL} = 0 V, I_{OH} = 0 mA) (V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 24 V V_{IL} = 0 V, I_{OH} = 0 mA)	 $I_{CC1(H)}$ $I_{CC2(H)}$ $I_{CC3(H)}$ $I_{CC2(H)}$ $I_{CC3(H)}$	 – – – – –	 4.0 -2.2 2.2 – –	 8.0 -3.2/+0.25 3.5 0.25 0.5	mA
Power Supply Currents — Output Low Logic State (V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V V_{IH} = 5.0 V, I_{OL} = 0 mA)	 $I_{CC1(L)}$ $I_{CC2(L)}$ $I_{CC3(L)}$	 – – –	 31 – 16	 47 2.5 25	mA
Power Supply Currents — Standby Condition (V_{CC1} = 0 V, V_{CC2} = 24 V, V_{CC3} = 24 V V_{IH} = 5.0 V, I_{OL} = 0 mA)	 $I_{CC2(S)}$ $I_{CC3(S)}$	 – –	 – –	 0.25 0.5	mA

*Typical Values at 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V and V_{CC3} = 24 V

SWITCHING CHARACTERISTICS (Unless otherwise noted T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V, V_{CC3} = 24 V, C_L = 200 pF, R_D = 24Ω, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time, Low to High State Output Propagation Delay Time, High to Low State Output	t_{PLH} t_{PHL}	10 10	31 30	48 46	ns
Delay Time, Low to High State Output Delay Time, High to Low State Output	t_{DLH} t_{DHL}	– –	11 10	20 18	ns
Transition Time, Low to High State Output Transition Time, High to Low State Output	t_{TLH} t_{THL}	– –	20 20	33 33	ns

FIGURE 1 – SWITCHING CHARACTERISTIC TEST CIRCUIT

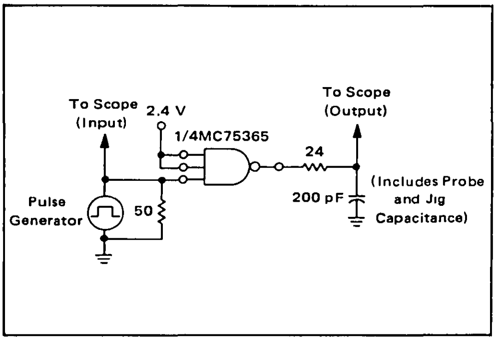
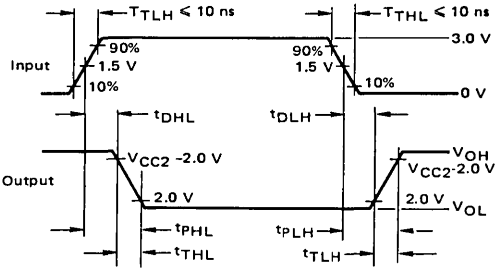


FIGURE 2 – SWITCHING CHARACTERISTICS WAVEFORMS



Input Pulse Characteristics:
PRR = 1.0 MHz, PW = 500 ns, $t_{TLH} = t_{THL} \leq 10$ ns

TYPICAL PERFORMANCE CURVES

FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

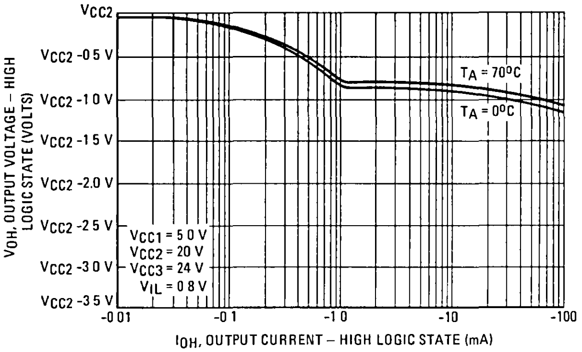


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

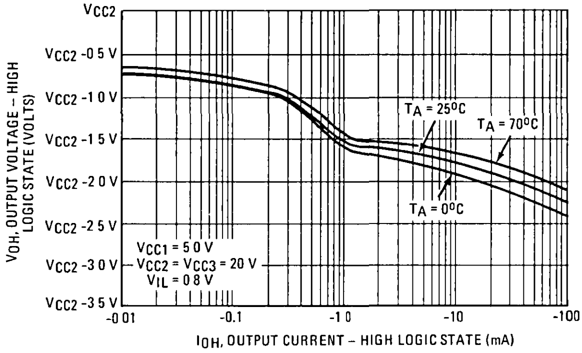


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT

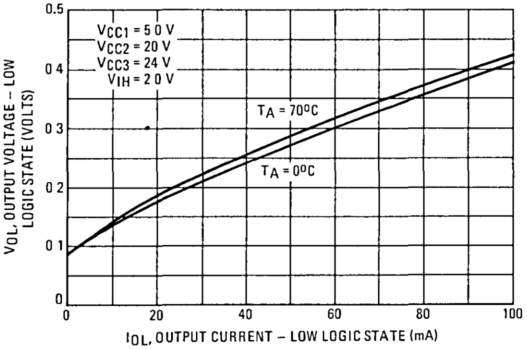
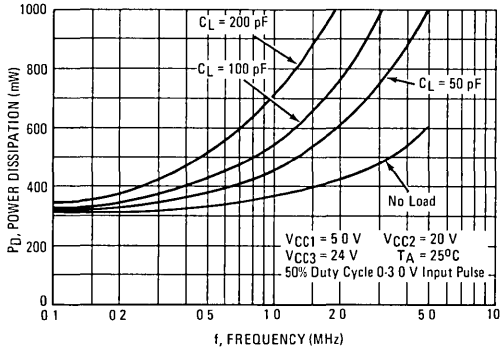


FIGURE 6 – TOTAL POWER DISSIPATION versus FREQUENCY (All Four Drivers)



TYPICAL PERFORMANCE CURVES

FIGURE 7 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus AMBIENT TEMPERATURE

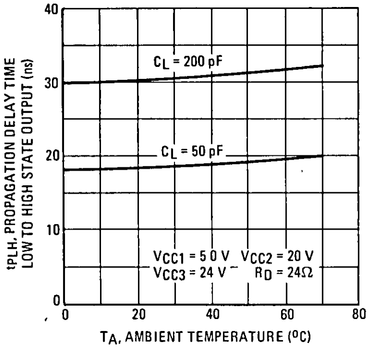


FIGURE 8 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus AMBIENT TEMPERATURE

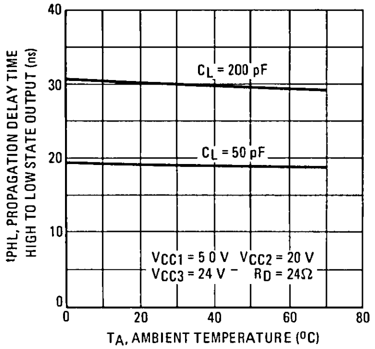


FIGURE 9 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

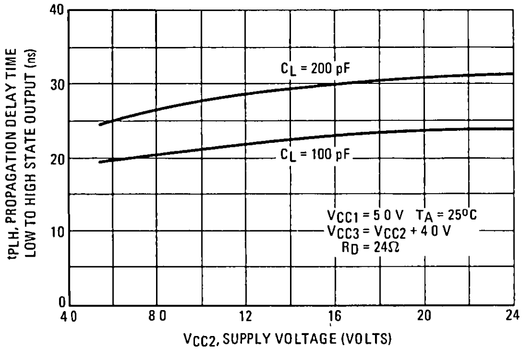


FIGURE 10 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

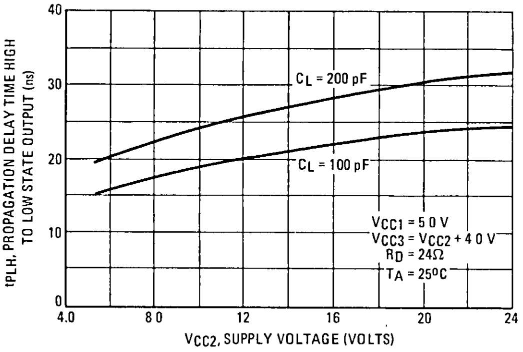


FIGURE 11 – PROPAGATION DELAY TIME – LOW TO HIGH LOGIC STATE versus LOAD CAPACITANCE

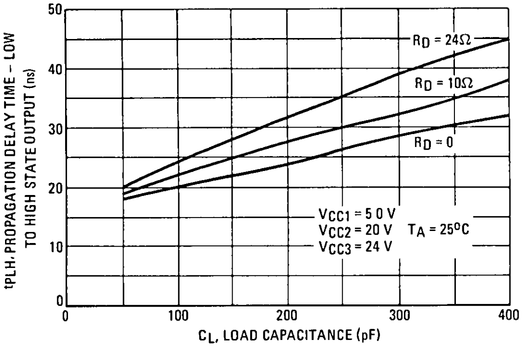
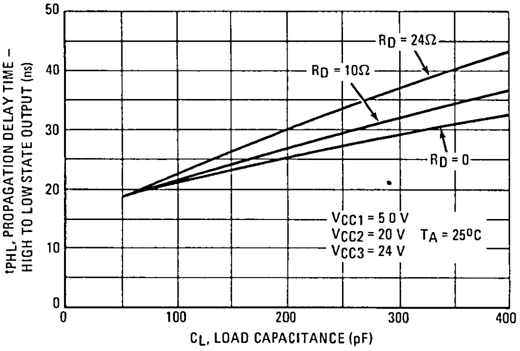


FIGURE 12 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus LOAD CAPACITANCE



APPLICATIONS SUGGESTIONS

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \qquad (1)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \qquad (2)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

Power Dissipation for the MC75365 MOS Clock Driver: The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The variation of power dissipation with frequency and load capacitance for the MC75365 is illustrated in Figure 6. The power dissipation, when substituted into equation (2), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for two integrated circuit packages in the maximum ratings section of this data sheet.

With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (1) and (2) and the maximum thermal resistance values given in Table 1 shown on the following page.

TABLE 1 – THERMAL CHARACTERISTICS OF "L" AND "P" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"L" (Ceramic Package)	150	100	50	27
"P" (Plastic Package)	150	100	70	40

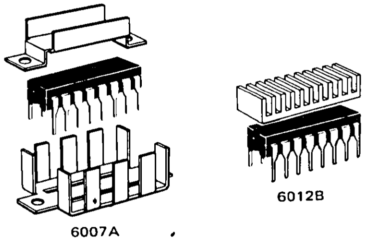
If the power dissipation determined by a given system produces a junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing tne surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 13.

FIGURE 13 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co of Texas

From Table 1, $R_{\theta JA}$(max) for the ceramic package with no heat sink and in a still air environment is 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 14 is 44°C/W. From Table 1 $R_{\theta JC}$(max) = 50°C/W for the ceramic package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

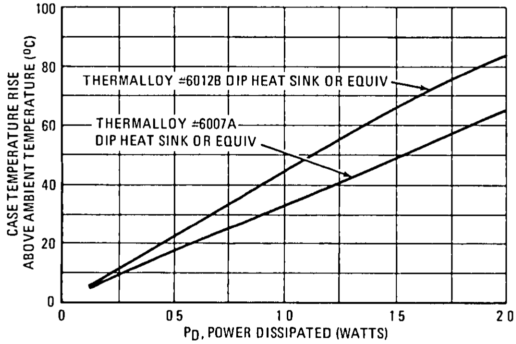
$R_{\theta JA}(max) = 50°C/W + 44°C/W = 94°C/W.$

Thus the addition of the heat sink has reduced $R_{\theta JA}$ (max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (2) at T_A = +70°C is:

$$P_D = \frac{175°C - 70°C}{+94°C/W} = 1.11 \text{ watts.}$$

This gives approximately a 60% increase in maximum power dissipation over the power dissipation which is allowable with no heat sink.

FIGURE 14 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 15, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA}(typ) = 100°C/W$

(b) $R_{\theta JC}(typ) = 27°C/W$

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (4)$$

Therefore, in still air

$R_{\theta CA}(typ) = 100°C/W - 27°C/W = 73°C/W$

From Curve 1 of Figure 14 at 500 LFPM and equation (4),

$R_{\theta CA}(typ) = 53°C/W - 27°C/W = 26°C/W.$

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

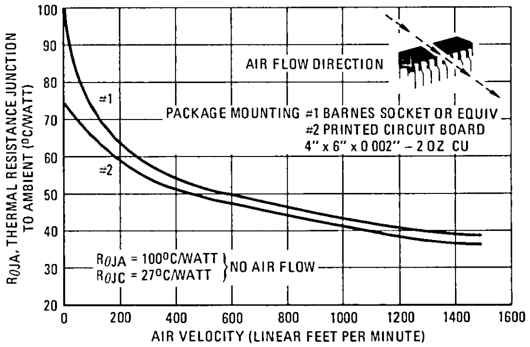
This yields an $R_{\theta CA}$(max) at 500 LFPM of 36°C/W. Therefore, from equation (3):

$R_{\theta JA}(max) = 50°C/W + 36°C/W = 86°C/W.$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (2):

$$P_D = \frac{175°C - 70°C}{86°C/W} = 1.2 \text{ watts.}$$

FIGURE 15 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



Heat Sink and Forced Air Combined:

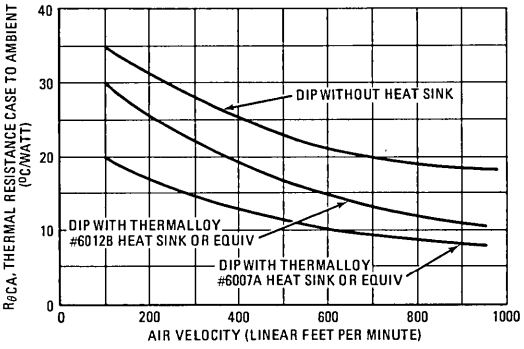
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 16. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 15. From equation (3):

Max $R_{\theta JA} = 50^{\circ}C/W + 17^{\circ}C/W = 67^{\circ}C/W$

From equation (2) at $T_A = +70^{\circ}C$

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W}\ 1.57 \text{ watts.}$$

FIGURE 16 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



Note from Table 1 and Figure 15 that if the 16-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine the maximum power dissipation for this condition.

Given data from Table 1:

typical $R_{\theta JA} = 100^{\circ}C/W$

typical $R_{\theta JC} = 27^{\circ}C/W$

From Curve 2 of Figure 15, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (3).

$R_{\theta JA} = 50^{\circ}C/W + 66^{\circ}C/W = 116^{\circ}C/W.$

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found. If $T_A = 70^{\circ}C$ then from equation (2) the maximum power dissipation may be found to be 905 mW.

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although data for PC mounting is generally not available, this should present no problem. Note in Figure 15 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ of the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

MOTOROLA

MC75368

DUAL MECL-to-MOS DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

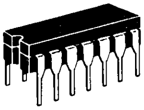
DUAL MECL-to-MOS DRIVER

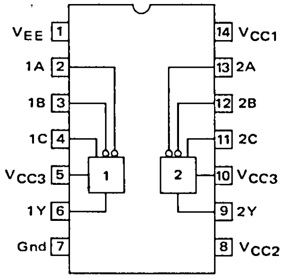
The MC75368 is a dual MECL-to-MOS driver and interface circuit. The device accepts standard MECL 10,000 and IBM grounded-reference ECL input signals and creates high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs. The device may also be used as a MECL-to-MTTL translator.

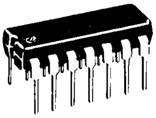
The MC75368 is optimized for higher voltage capability.

- Dual MECL-to-MOS Driver
- Dual MECL-to-MTTL Driver
- Versatile Interface Circuit for Use Between MECL and High-Current, High-Voltage Systems

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

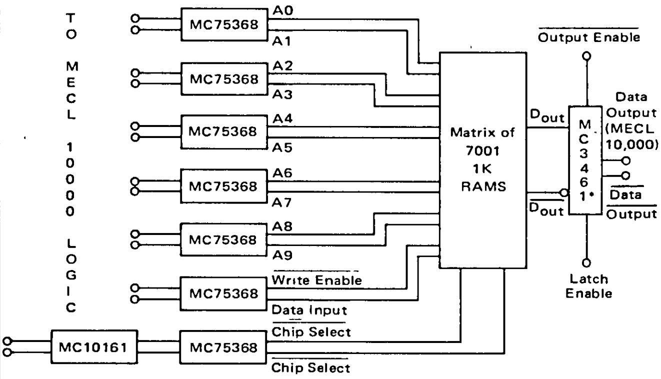






P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL APPLICATION WITH 7001 1K NMOS RAM



*MC3461 Dual Sense Amplifier

FUNCTION TABLE

Input Voltage Conditions		Output
Differential	Logic Level	Output
(More positive of A or B) -C	A B C	Y
($V_{ID} \geq$ 150 mV)	L H L H L H H H L	L
(-150 mV $\leq V_{ID} \leq$ 150 mV)	X X X	Indeterminate
($V_{ID} \leq$ -150 mV)	L L H	H

H = high logic level, L = low logic level,
X = irrelevant

MAXIMUM RATINGS (Unless otherwise noted, voltages measured with respect to GND terminals, $T_A = 25^oC$.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}	-0 5 to 7.0	Vdc
	V_{CC2}	-0.5 to 22	Vdc
	V_{CC3}	-0.5 to 30	Vdc
	V_{EE}	-8.0 to 0.5	Vdc
Most Negative of V_{CC1}, V_{CC2}, or V_{CC3} with respect to V_{EE}	–	-0.5	Vdc
Input Voltage	V_I	-8 0 to 0.5	Vdc
Inter-Input Voltage(1)	–	5 5	Vdc
Most negative Input Voltage with respect to V_{EE}	$V_I - V_{EE}$	-5.0	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ $T_A = 25^oC$	P_D	1000	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6 6	mW/°C
Plastic Package @ $T_A = 25^oC$	P_D	830	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ $T_C = 25^oC$	P_D	3 0	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ $T_C = 25^oC$	P_D	1 8	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

(1) With respect to any pair of inputs to either of the input gates.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1}	4.75	5.0	5 25	V
	V_{CC2}	4 75	20	22	V
	V_{CC3}	V_{CC2}	24	28	V
	$V_{CC3} - V_{CC2}$	0	4.0	10	V
	V_{EE}	-4.68	-5.2	-5.72	V
Operating Ambient Temperature Range	T_A	0	–	70	°C

DEFINITION OF INPUT LOGIC LEVELS

Input Voltage – High Logic State (Any Input) (1)	V_{IH}	-1.5	–	-0.7	V
Input Voltage – Low Logic State (Any Input) (1)	V_{IL}	V_{EE}	–	V_{IH}-150	mV
Input Differential Voltage – High Logic State (2)	V_{IDH}	150	–	–	mV
Input Differential Voltage – Low Logic State (2)	V_{IDL}	-150	–	–	mV

(1) The definition of these Logic Levels use Algebraic System of notation

(2) The input differential voltage is measured from the more positive inverting input (A or B) with respect to the non-inverting input (C) of the same gate.

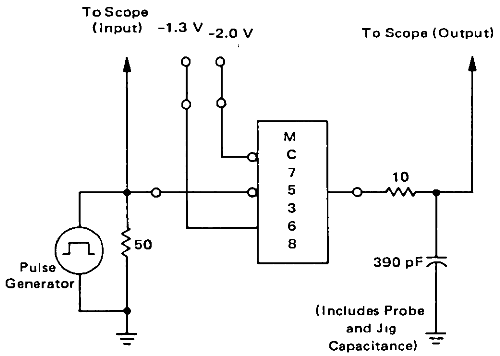
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20, V_{CC3} = 24 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State					V
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -100 µA)	V_{OH1}	V_{CC2} - 0.3	V_{CC2} - 0.1	–	
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH2}	V_{CC2} - 1.2	V_{CC2} - 0.9	–	V
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -50 µA)	V_{OH3}	V_{CC2} - 1.0	V_{CC2} - 0.7	–	V
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH4}	V_{CC2} - 2 3	V_{CC2} - 1.8	–	V
Output Voltage — Low Logic State					V
(V_{IDH} = 150 mV, I_{OL} = 10 mA)	V_{OL1}	–	0.15	0.3	
(V_{IDH} = 150 mV, I_{OL} = 30 mA)	V_{OL2}				V
10 V ≤ V_{CC3} ≤ 22 V		–	–	–	
10 V ≤ V_{CC2} ≤ 28 V		–	0 2	0.4	
Output Clamp Voltage (V_{IDH} = 500 mV, I_{OC} = 20 mA)	V_{OC}	–	–	V_{CC2}+1.5 V	V
Input Current — High Logic State (V_{EE} = -5.72 V, V_{IL} = -5.72 V, V_{IH} = -0.7 V)	I_{IH}	–	300	800	µA
Input Current — Low Logic State					µA
(V_{IH} = -0.7 V, V_{IL} = -2.0 V)	I_{IL1}	–	–	-10	
(V_{EE} = -5 72 V, V_{IH} = -0.7 V, V_{IL} = -5.72 V)	I_{IL2}	–	–	-100	
Power Supply Current — Both Outputs High Logic State					
(V_{CC} = 5.25 V, V_{CC2} = 22 V,	$I_{CC1(H)}$	–	21	38	mA
V_{CC3} = 26 V, V_{EE} = -5.72 V,	$I_{CC2(H)}$	–	-1.1	+0 25	mA
V_{IL} (A) and (B) = -2 0 V, $V_{IH(C)}$ = -0.7 V, I_{OH} = 0)	$I_{CC3(H)}$	–	0.6	1 0	mA
	$I_{EE(H)}$	–	-21	-38	mA
Power Supply Current — Both Outputs Low Logic State					
(V_{CC1} = 5 25 V, V_{CC2} = 22 V, V_{CC3} = 28 V, V_{EE} = -5.72 V,	$I_{CC1(L)}$	–	13	24	mA
$V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2 0 V, I_{OL} = 0)	$I_{CC2(L)}$	–	0.5	1.0	mA
	$I_{CC3(L)}$	–	4.0	7.0	mA
	$I_{EE(L)}$	–	-21	-38	mA
Power Supply Current — Both Outputs High Logic State (V_{CC1} = 5.25 V, V_{CC2} = 22.V,	$I_{CC2(H)}$	–	–	0.25	mA
V_{CC3} = 22 V, V_{EE} = -5.72 V, $V_{IL(A)}$ and (B) = -2.0 V, $V_{IH(C)}$ = -0.7 V, I_{OL} = 0)	$I_{CC3(H)}$	–	–	0.25	mA
Power Supply Current — Stand By Condition (V_{CC1} = 0 V, V_{CC2} = 22 V, V_{CC3} = 22 V, V_{EE} = 0 V,	$I_{CC2(S)}$	–	–	0.25	mA
$V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2.0 V, I_{OL} = 0)	$I_{CC3(S)}$	–	–	0 25	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20 V.)

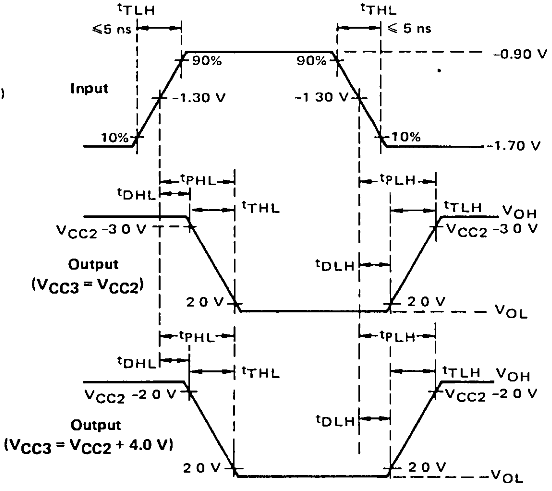
Characteristic	Symbol	Min	Typ	Max	Unit
Delay Time — Low to High Output Logic Level	t_{DLH}				ns
(V_{CC3} = 24 V)		–	12	24	
(V_{CC3} = 20 V)		–	13	25	
Delay Time — High to Low Output Logic Level	t_{DHL}				ns
(V_{CC3} = 24 V)		–	13	24	
(V_{CC3} = 20 V)		–	15	26	
Transition Time, Low-to-High Output Logic Level	t_{TLH}				ns
(V_{CC3} = 24 V)		–	19	30	
(V_{CC3} = 20 V)		–	20	30	
Transition Time, High-to-Low Output Logic Level	t_{THL}				ns
(V_{CC3} = 24 V)		–	20	33	
(V_{CC3} = 20 V)		–	18	30	
Propagation Delay Time, Low-to-High Logic Level	t_{PLH}				ns
(V_{CC3} = 24 V)		–	31	54	
(V_{CC3} = 20 V)		–	33	55	
Propagation Delay Time, High-to-Low Logic Level	t_{PHL}				ns
(V_{CC3} = 24 V)		–	33	57	
(V_{CC3} = 20 V)		–	33	56	

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



The pulse generator has the following characteristics.
PRR = 1 MHz. $z_o \approx 50\ \Omega$.
Duty Cycle = 50%

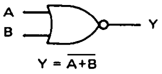
FIGURE 3 — SWITCHING TIMES WAVEFORM



APPLICATIONS INFORMATION

MODES OF OPERATION

FIGURE 4 – POSITIVE-NOR GATE

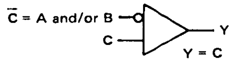


FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

H – High Level, L – Low Level, X – Irrelevant
V_{BB} – Reference Supply voltage for MECL 10,000

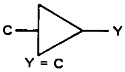
FIGURE 5 – DIFFERENTIAL MECL LINE RECEIVER



FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

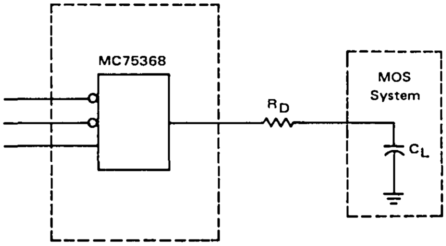
FIGURE 6 – NON-INVERTING GATE



FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

FIGURE 7 – USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN MC75368 APPLICATIONS



Note $R_D \approx 10\Omega$ to 30Ω (optional)

The need for four separate power supplies V_{CC1}, V_{CC2}, V_{CC3} and V_{EE} can be avoided in many cases by tying V_{CC2} to V_{CC3}. However, performance advantages can be obtained by connecting either one or both V_{CC3} pins to an additional power supply of higher voltage than V_{CC2}. Both V_{CC3} pins do not have to be held at the same voltage. For MECL-to-TTL level converter applications both V_{CC2} and V_{CC3} are generally connected to a +5.0 V power source.

By providing two out-of-phase (A and B) inputs and one in-phase (C) input, each gate can be used as positive NOR, or as a inverting or non-inverting gate. This flexibility is achieved by connecting an externally supplied MECL 10,000 Series reference supply voltage (V_{BB}) to the appropriate input as shown in Figures 4 thru 6. An unused out-of-phase input should be tied low or connected to the other out-of-phase input of the same gate. The required V_{BB} voltage source may be obtained from MECL 10,000 Series devices such as the MC10115 line receiver, or by connecting the output of a MECL 10,000 gate, like the MC10102, to the respective out-of-phase inputs (as an example connect pins 4 and 5 to 2 of the MC10102 to obtain a V_{BB} reference voltage).

When driven differentially, the MC75368 may be used as a differential MECL line receiver, without the need for the V_{BB} reference voltage.

Undesirable output transient overshoot due to load or wiring inductance and the fast switching speeds of the MC75368 can be eliminated or reduced by adding a small amount of series resistance. The value of this damping resistance is dependent on specific load characteristics and switching speed but typical values lie in the range of 10 to 30 ohms. This is illustrated in Figure 7.

MOTOROLA

MMH0026
MMH0026C

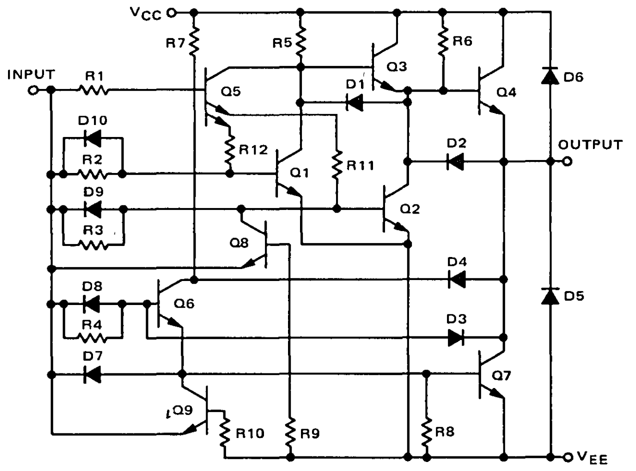
Specifications and Applications Information

DUAL MOS CLOCK DRIVER

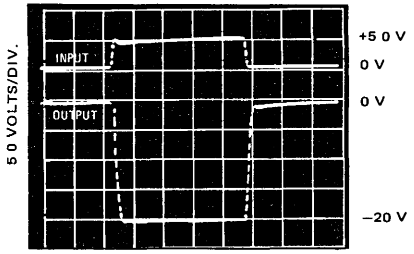
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

- Fast Transition Times – 20 ns with 1000 pF Load
- High Output Swing – 20 Volts
- High Output Current Drive – ±1.5 Amperes
- High Repetition Rate – 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State – 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

FIGURE 1 – CIRCUIT SCHEMATIC
(1/2 CIRCUIT SHOWN)



TYPICAL OPERATION
(R_S = 10 Ω, C_L = C_{in} = 1000 pF, f = 1.0 MHz,
PW = 500 ns, V_{CC} = 0 V, V_{EE} = -20 V)

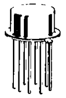


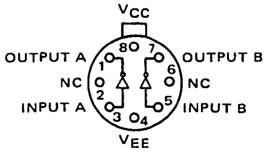
100 ns/DIV.

DUAL MOS
CLOCK DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

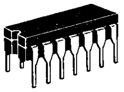
G SUFFIX
METAL PACKAGE
CASE 601
TO-99

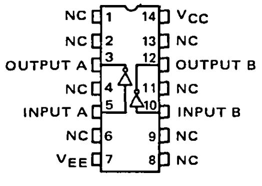




(Top View)

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

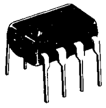


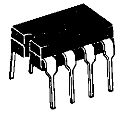


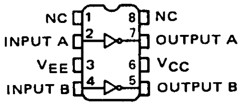
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693







(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Differential Supply Voltage	V_{CC}-V_{EE}	+22			Vdc
Input Current	I_I	+100			mA
Input Voltage	V_I	V_{EE} + 5.5			Vdc
Peak Output Current	I_{Opk}	±1.5			A
Junction Temperature	T_J	+175	+175	+150	°C
Operating Ambient Temperature Range	T_A	G	U,L	P1	°C
MMH0026		-55 to +125	-55 to +125	–	
MMH0026C		0 to +70	0 to +70	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +70°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage V_O = V_{EE} + 1.0 Vdc	V_{IH}	V_{EE} + 2.0	V_{EE} + 1.5	–	Vdc
Logic "1" Level Input Current V_I –V_{EE} = 2.4 Vdc, V_O = V_{EE} + 1.0 Vdc	I_{IH}	–	10	15	mA
Logic "0" Level Input Voltage V_O = V_{CC} -1.0 Vdc	V_{IL}	–	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current V_I –V_{EE} = 0 Vdc, V_O = V_{CC} -1.0 Vdc	I_{IL}	–	-0.005	-10	µA
Logic "0" Level Output Voltage	V_{OH}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -11.6 Vdc		4.0	4.3	–	
V_I –V_{EE} = 0.4 Vdc		V_{CC} -1.0	V_{CC} -0.7	–	
Logic "1" Level Output Voltage	V_{OL}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -9.6 Vdc		–	-11.5	-11	
V_I –V_{EE} = 2.4 Vdc		–	V_{EE} + 0.5	V_{EE} + 1.0	
"On" Supply Current (Note 1) V_{CC}–V_{EE} = 20 Vdc, V_I –V_{EE} = 2.4 Vdc	I_{CCL}	–	30	40	mA
"Off" Supply Current MMH0026C V_{CC}–V_{EE} = 20 Vdc, V_I –V_{EE} = 0 V MMH0026	I_{CCH}	– –	10 –	100 500	µA

SWITCHING CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = 25°C)

Propagation Time						
High to Low	(Figure 2)	t_{PHL}	5.0	7.5	12	ns
	(Figure 3)		–	11	–	
Low to High	(Figure 2)	t_{PLH}	5.0	12	15	
	(Figure 3)		–	13	–	
Transition Time (High to Low)		t_{THL}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	12	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	15	18	
	(Figure 3)		–	30	40	
V_{CC}-V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	20	35	
	(Figure 3)		–	36	50	
Transition Time (Low to High)		t_{TLH}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	10	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	12	16	
	(Figure 3)		–	28	35	
V_{CC} -V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	17	25	
	(Figure 3)		–	31	40	

Note 1: Tested with one output on at a time.

TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

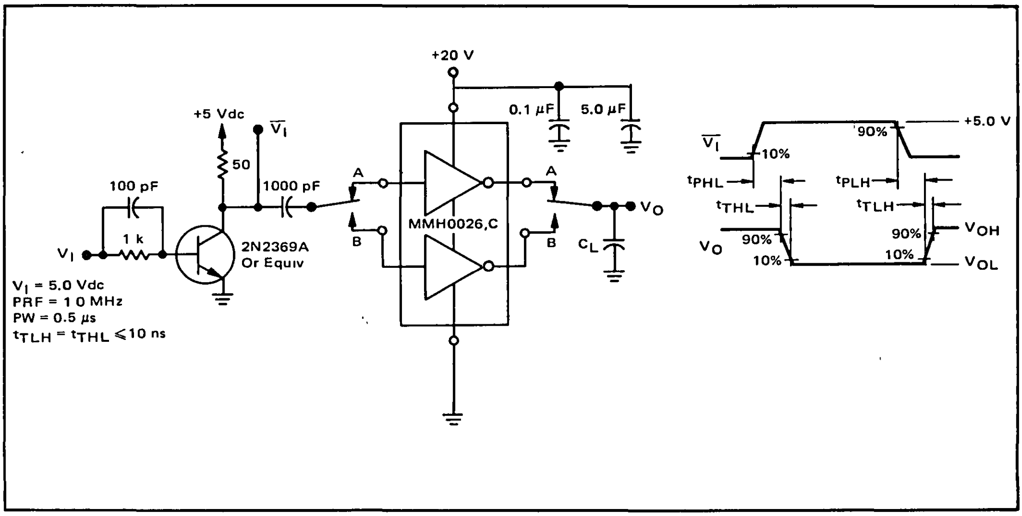
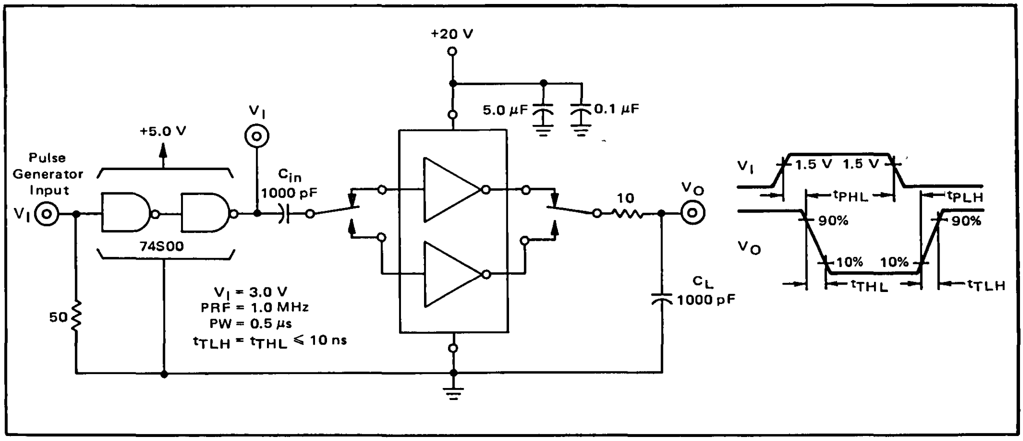


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 – INPUT CURRENT versus INPUT VOLTAGE

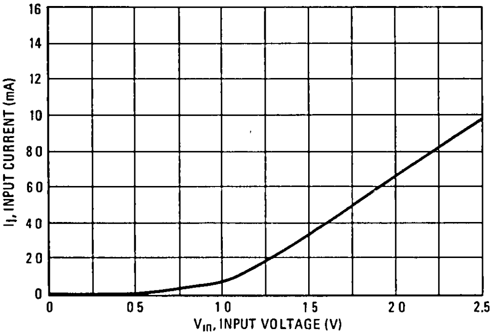


FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

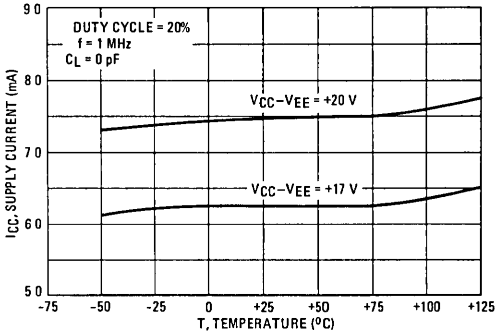


FIGURE 6 – OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

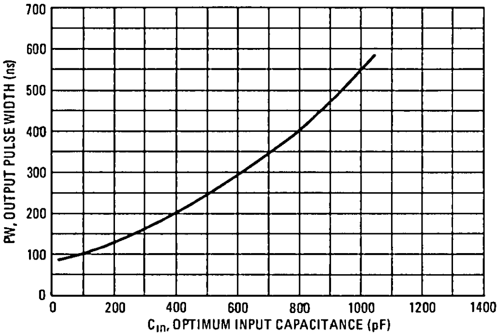


FIGURE 7 – TRANSITION TIMES versus LOAD CAPACITANCE

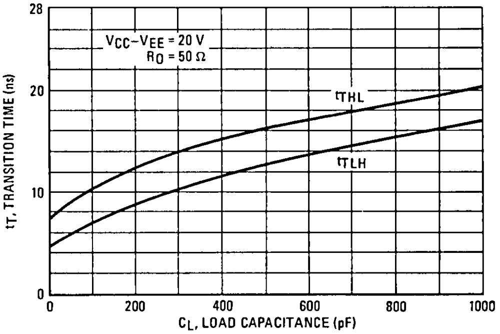


FIGURE 8 – PROPAGATION DELAY TIMES versus TEMPERATURE

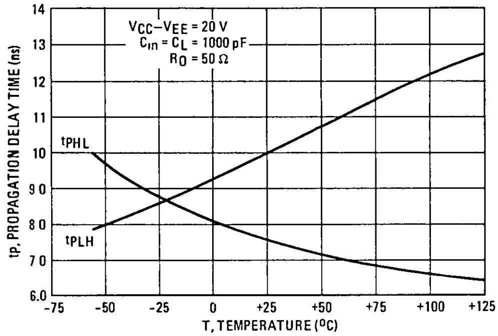
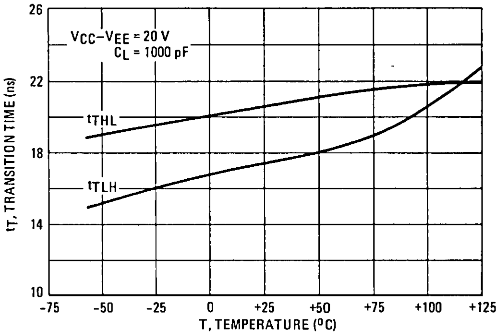


FIGURE 9 – TRANSITION TIMES versus TEMPERATURE



TYPICAL CHARACTISTICS (continued)

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

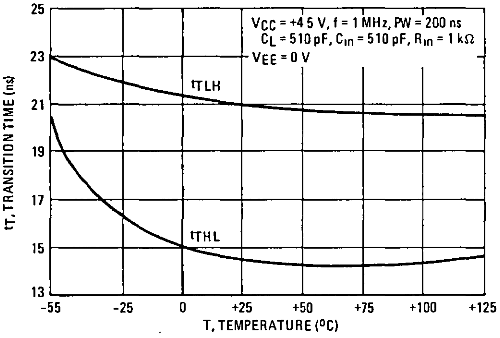


FIGURE 11 – PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

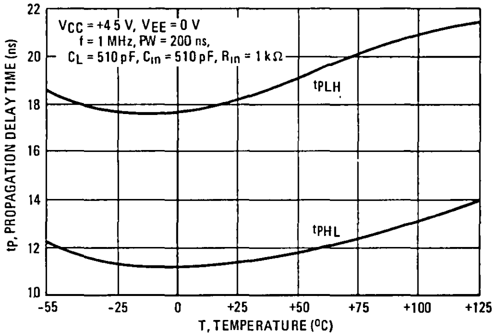


FIGURE 12 – DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

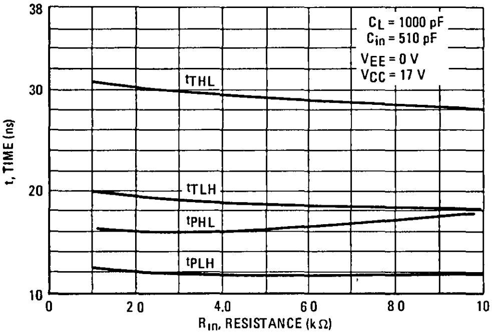


FIGURE 13 – DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

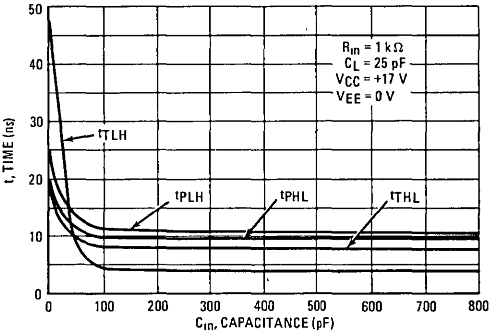


FIGURE 14 – MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

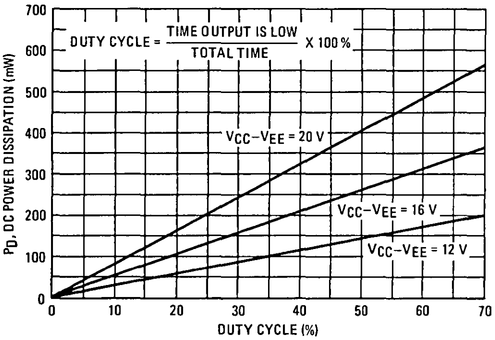
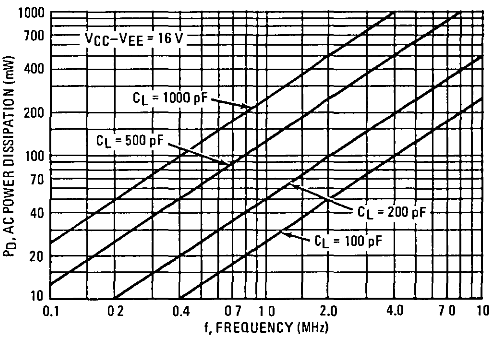


FIGURE 15 – AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



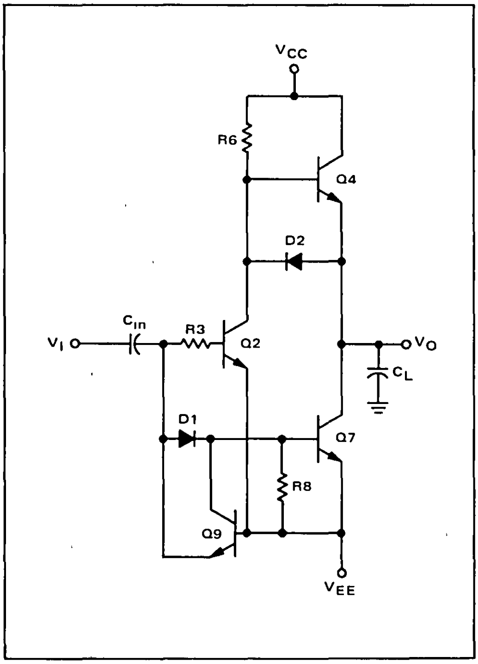
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 16, is useful in explaining the operation of the device. Figure 16 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 16 – SIMPLIFIED SCHEMATIC DIAGRAM
(Ref.: Figure 1)



The complete circuit, Figure 1, basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 16. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies ($V_{EE} <$ GND), ac coupling, as illustrated in Figure23, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

APPLICATIONS INFORMATION (continued)

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 6 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3})\ (PW_O). \qquad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

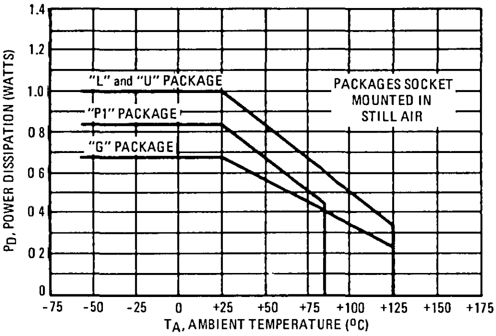
$$C_{in} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\ \text{pF}.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure24can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 12 and 13 show typical switching characteristics for various values of input resistance and capacitance.

TABLE 1 – THERMAL CHARACTERISTICS OF "G", "L", "P1", AND "U" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40
"U" (Ceramic Package)	150	100	50	27

FIGURE 17 – MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \qquad (2)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \qquad (3)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

Power Dissipation for the MMH0026 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 17. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: $R_{\theta JA(max)}$ = 150°C/watt, and from the maximum rating section of the data sheet: $T_J(max)$ = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 17. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \quad (4)$$

$$\text{where } I_{CCL} = 40\text{ mA } \left(\frac{V_{CC} - V_{EE}}{20\text{ V}}\right).$$

Note that Figure 14 is a plot of equation (4) for three values of (V_{CC}–V_{EE}). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 14, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\text{ mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \quad (5)$$

where f = frequency of operation

C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 15, the safe operating area beneath Curve A of Figure 18 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 15 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

Note from Figure 18, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A

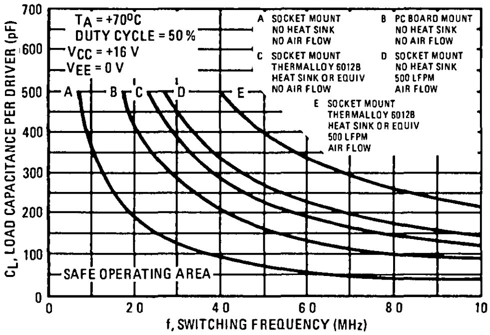
(b) decrease the duty cycle

(c) lower package thermal resistance ($R_{\theta JA}$)

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance $R_{\theta JA}$ that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance ($R_{\theta JC}$) and the other is the case-to-ambient thermal resistance ($R_{\theta CA}$). Since the factor $R_{\theta JC}$ is a function of the die size and type of bonding employed, it cannot be varied. However, the $R_{\theta CA}$ term can be changed as previously discussed, see Page 7.

FIGURE 18 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



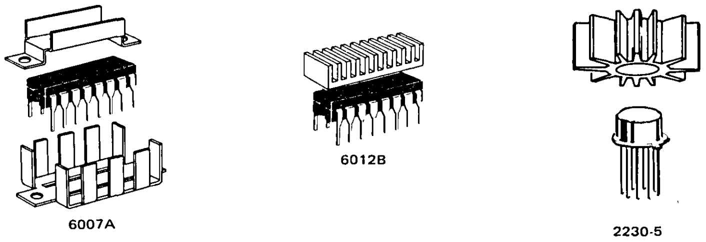
Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 19. In the previous example, with the ceramic package, no heat sink and in a still air environment, $R_{\theta JA(max)}$ was 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 20 is 44°C/W. From Table 1 $R_{\theta JC}(max)$ = 50°C/W for the ceramic

APPLICATIONS INFORMATION (continued)

FIGURE 19 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas

package. Therefore, the new $R_{\theta JA}(max)$ with the 6012B heat sink added becomes:

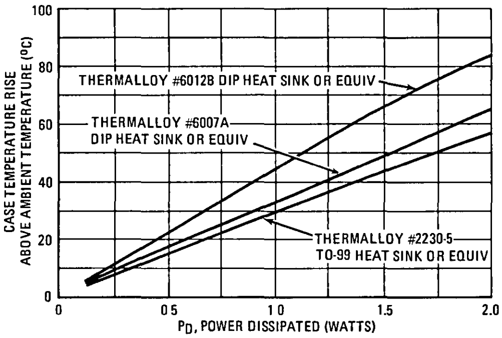
$$R_{\theta JA}(max) = 50^{\circ}C/W + 44^{\circ}C/W = 94^{\circ}C/W.$$

Thus the addition of the heat sink has reduced $R_{\theta JA}(max)$ from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{94^{\circ}C/W} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 18 can now be generated as before with the aid of Figure 15 and equation (5).

FIGURE 20 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 21, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA}(typ) = 100^{\circ}$ C/W
(b) $R_{\theta JC}(typ) = 27^{\circ}$ C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (6)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (7)$$

Therefore, in still air

$$R_{\theta CA}(typ) = 100^{\circ}C/W - 27^{\circ}C/W = 73^{\circ}C/W$$

From Curve 1 of Figure 21 at 500 LFPM and equation (7),

$$R_{\theta CA}(typ) = 53^{\circ}C/W - 27^{\circ}C/W = 26^{\circ}C/W.$$

Thus $R_{\theta CA}(typ)$ has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}(max)$ of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA}(max)$ at 500 LFPM of 36°C/W.

Therefore, from equation (6):

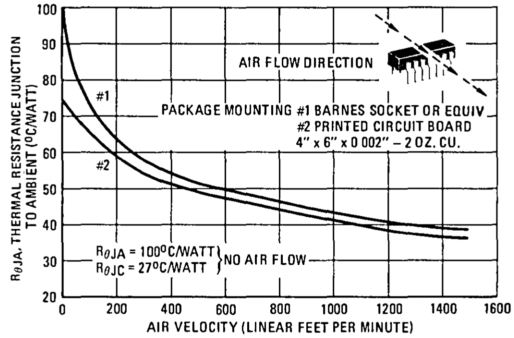
$$R_{\theta JA}(max) = 50^{\circ}C/W + 36^{\circ}C/W = 86^{\circ}C/W.$$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{+86^{\circ}C/W} = 1.2 \text{ watts.}$$

APPLICATIONS INFORMATION (continued)

FIGURE 21 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 18 can now be generated from Figure 15 and equation (5).

Heat Sink and Forced Air Combined:

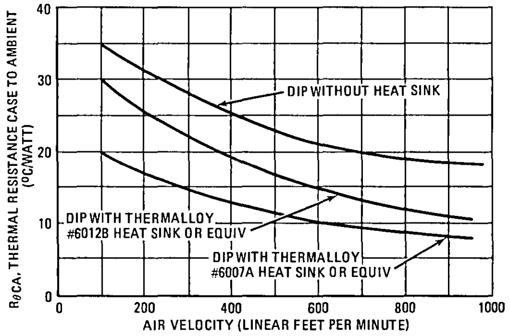
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 22. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 22. From equation (6):

$$\text{Max } R_{\theta JA} = 50^\circ C/W + 17^\circ C/W = 67^\circ C/W$$

From equation (3) at $T_A = +70^\circ C$

$$P_D = \frac{175^\circ C - 70^\circ C}{67^\circ C/W} \; 1.57 \text{ watts.}$$

FIGURE 22 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 18.

Note from Table 1 and Figure 21 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } R_{\theta JA} = 100^\circ C/W$$
$$\text{typical } R_{\theta JC} = 27^\circ C/W$$

From Curve 2 of Figure 21, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^\circ C/W}{1.5} = 66^\circ C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (6).

$$R_{\theta JA} = 50^\circ C/W + 66^\circ C/W = 116^\circ C/W.$$

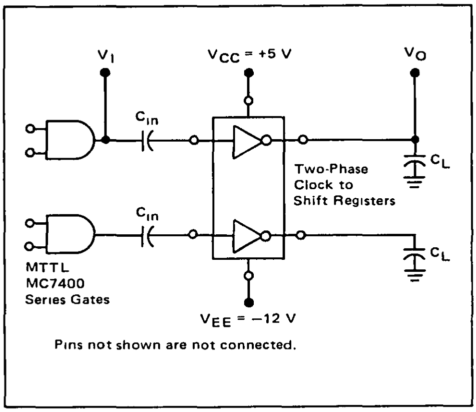
With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 18.

CONCLUSION

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although $R_{\theta CA}$ data for PC mounting is generally not available, this should present no problem. Note in Figure 21 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ on the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

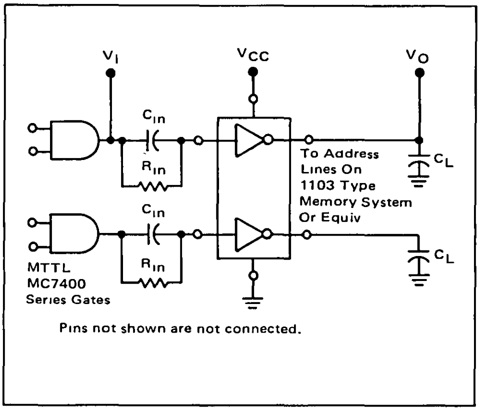
TYPICAL APPLICATIONS

FIGURE 23 – AC-COUPLED MOS CLOCK DRIVER

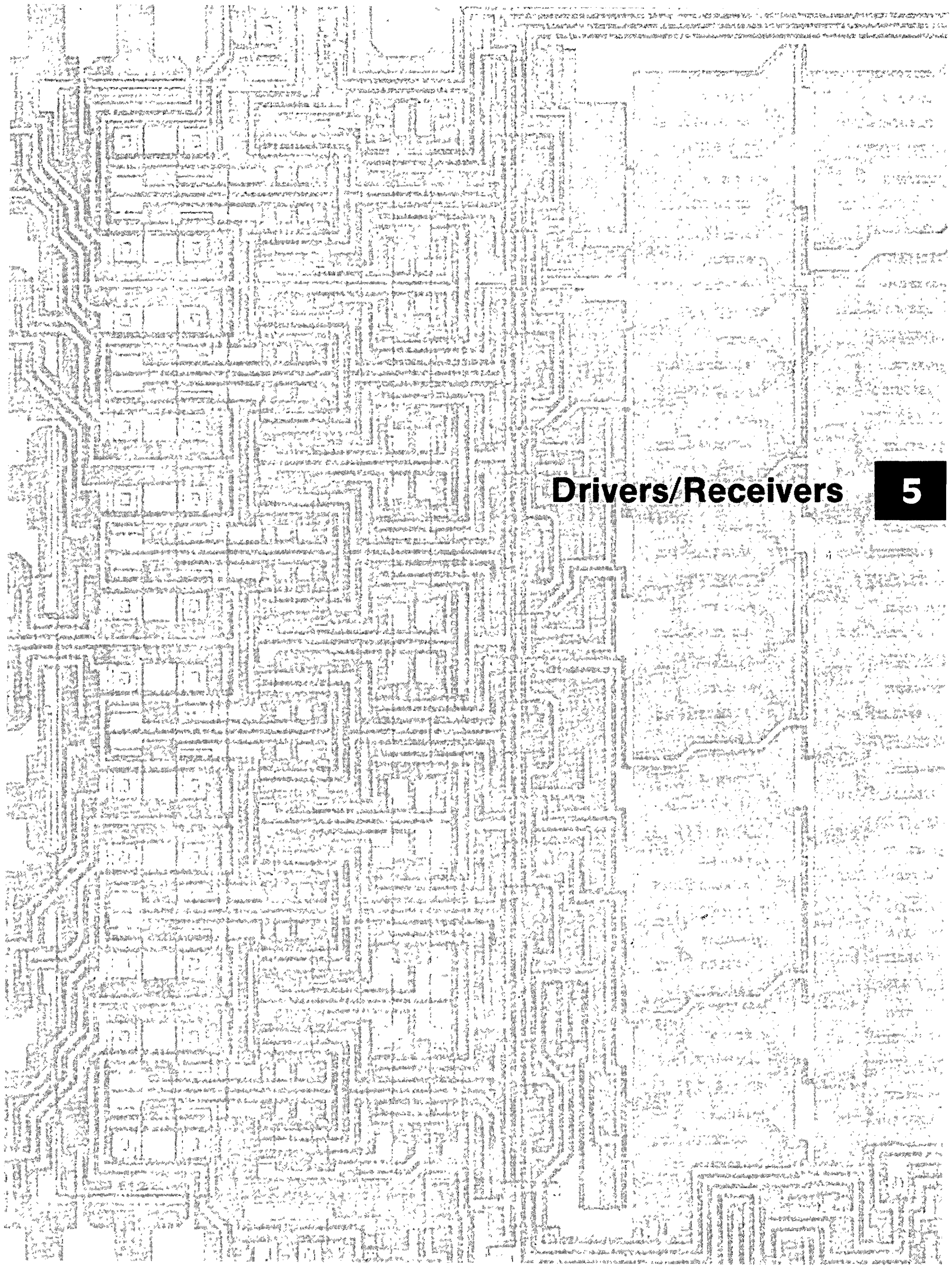


Pins not shown are not connected.

FIGURE 24 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)



Pins not shown are not connected.



Drivers/Receivers

5

DRIVERS/RECEIVERS

*Industrial

MOTOROLA

AM26LS31

QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

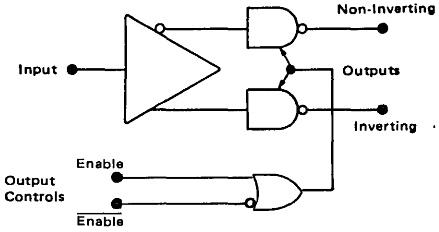
The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA Standard RS-422 and Federal Standard 1020.

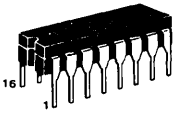
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 RS-422 driver.

The high impedance output state is assured during power down.

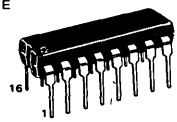
- Full RS-422 Standard Compliance
- Single +5 V Supply
- Meets Full $V_O = 6.0$ V, $V_{CC} = 0$ V, $I_O < 100\ \mu A$ Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

DRIVER BLOCK DIAGRAM



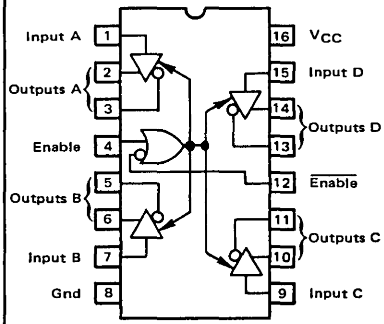


D SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Input	Control Inputs (E/$\overline{E}$)	Non-Inverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*ABSOLUTE MAXIMUM RATINGS			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits The "Table of Electrical Characteristics" provides conditions for actual device operation

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V $\leqslant V_{CC} \leqslant$ 5 25 V and 0°C $\leqslant T_A \leqslant$ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0 8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0 4 V)	I_{IL}	–	–	-360	μA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 7 0 V)	I_{IH}	 – –	 – –	 +20 +100	μA
Input Clamp Voltage (I_{IK} = -18 mA)	V_{IK}	–	–	-1 5	V
Output Voltage – Low Logic State (I_{OL} = 20 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = -20 mA)	V_{OH}	2 5		–	V
Output Short-Circuit Current (V_{IH} = 2.0 V) 2	I_{OS}	-30	–	-150	mA
Output Leakage Current – Hi-Z State (V_{OL} = 0.5 V, $V_{IL(E)}$ = 0 8 V, $V_{IH(\overline{E})}$ = 2 0 V) (V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{O(Z)}$	 – –	 – –	 -20 +20	μA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = -0.25 V, V_{CC} = 0 V)	$I_{O(off)}$	 – –	 – –	 +100 -100	μA
Output Offset Voltage Difference[1]	$V_{OS} - \overline{V}_{OS}$	–	–	±0.4	V
Output Differential Voltage 1	V_T	2.0	–	–	V
Output Differential Voltage Difference 1	$V_T - \overline{V}_T$	–	–	±0.4	V
Power Supply Current (Output Disabled)[3]	I_{CCX}	–	60	80	mA

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Skew		–	–	6 0	ns
Propagation Delay – Control to Output (C_L = 10 pF, R_L = 75 Ω to Gnd) (C_L = 10 pF, R_L = 180 Ω to V_{CC}) (C_L = 30 pF, R_L = 75 Ω to Gnd) (C_L = 30 pF, R_L = 180 Ω to V_{CC})	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 30 35 40 45	ns

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

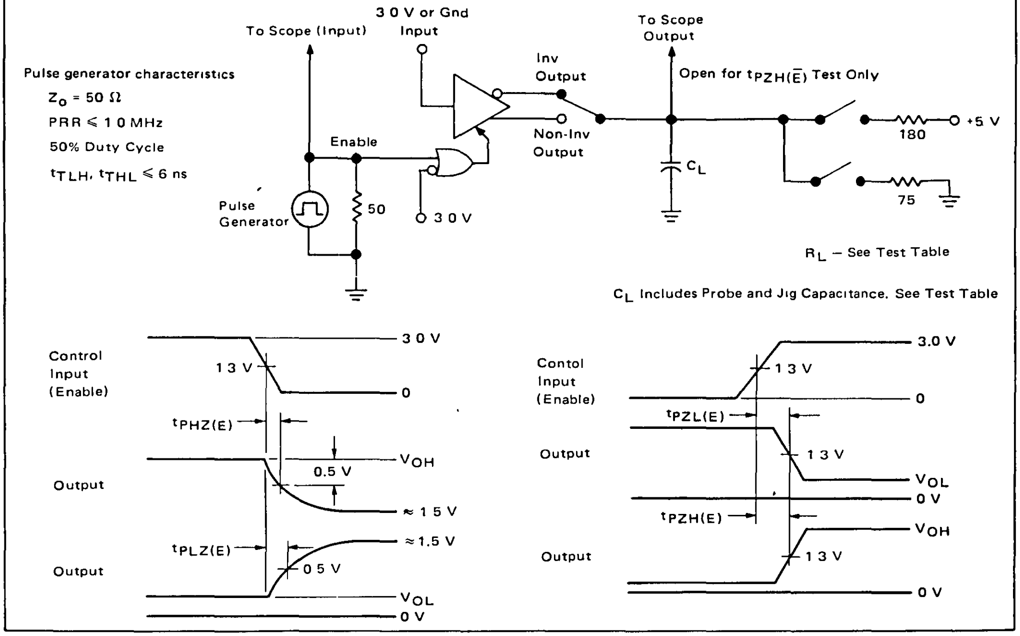
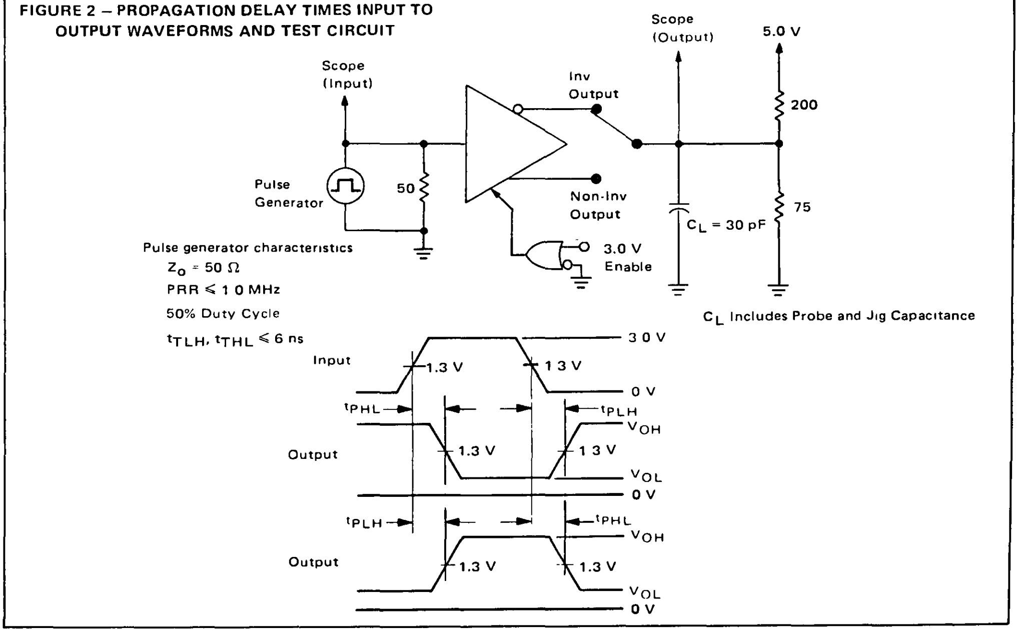


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



MOTOROLA

DS8641

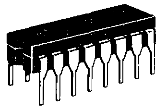
QUAD UNIFIED BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

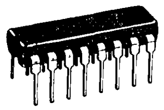
QUAD UNIFIED TRANSCEIVER

Consists of four pair of drivers and receivers with the output of each driver connected to the input of its mating receiver. These devices are intended for use in bus organized data transmission system employing terminated 120 Ω lines. A disable function consisting of a two-input NOR gate is provided to control all four drivers. Up to 27 driver/receiver pairs can share a common line.

- Receiver Input Threshold Is Not Affected by Temperature
- Open Collector Driver Outputs Allow Wire-OR
- TTL Compatible Receiver Outputs and Disable and Driver Inputs
- Driver Propagation Delay = 15 ns
- Receiver Propagation Delay = 20 ns
- Guaranteed Minimum Bus Noise Immunity = 0.6 V
- Low Bus Terminal Current (Supply On or Off) = 30 μA typ

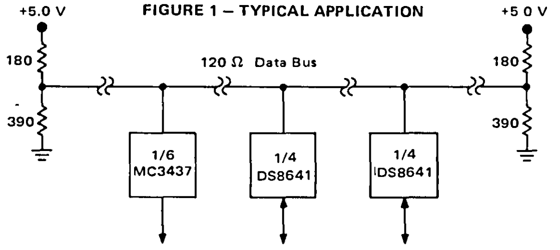


J SUFFIX
CERAMIC PACKAGE
CASE 620

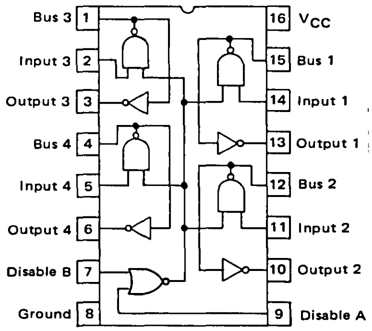


N SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION



PIN CONNECTIONS



TRUTH TABLES

RECEIVER SECTION

Bus	Output
$V_{IH(R)} > 1.7$ V	L
$V_{IL(R)} < 1.3$ V	H

Where L = Low Logic State
H = High Logic State

DRIVER SECTION

Disable 1	Disable 2	Input	Bus
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	7.0	Vdc
Input and Output Voltage		V_O, V_I	5.5	Vdc
Junction Temperature	Plastic Ceramic	T_J	150 175	°C
Operating Ambient Temperature Range		T_A	0 to +70	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leqslant T_A \leqslant 70^oC$ and $4.75 \leqslant V_{CC} \leqslant 5.25$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Disable Input Voltage – High Logic State	$V_{IH(DA)}$	2 0	–	–	V
Disable Input Voltage – Low Logic State	$V_{IL(DA)}$	–	–	0.8	V
Driver Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Receiver Input Threshold Voltage – High Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{OL(R)} \leqslant$ 0 4 V)	$V_{ILH(R)}$	1.70	1 50	–	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OH(R)}$ = -400 μA, $V_{OH(R)} \geqslant$ 2.4 V)	$V_{IHL(R)}$	–	1.50	1.30	V
Disable Input Current – High Logic State ($V_{IH(D)}$ = 2.4 V, $V_{IH(DA)}$ = 2.4 V) ($V_{IH(D)}$ = 5.5 V, $V_{IH(DA)}$ = 5.5 V)	$I_{IH(DA)}$	 – –	 – –	 40 1 0	 μA mA
Driver Input Current – High Logic State ($V_{IH(DA)}$ = 2.4 V, $V_{IH(D)}$ = 2.4 V) ($V_{IH(DA)}$ = 5.5 V, $V_{IH(D)}$ = 5.5 V)	$I_{IH(D)}$	 – –	 – –	 40 1.0	 μA mA
Disable Input Current – Low Logic State ($V_{IL(DA)}$ = 0.4 V, $V_{IL(D)}$ = 0.4 V)	$I_{IL(DA)}$	–	–	-1.6	mA
Driver Input Current – Low Logic State ($V_{IL(D)}$ = 0.4 V, $V_{IL(DA)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-1.6	mA
Bus Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0 8, $V_{IH(BUS)}$ = 4.0 V) (V_{CC} = 5.25 V) (V_{CC} = 0 V)	I_{BUS}	 – –	 30 2.0	 100 100	μA
Bus Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(D)}$ = 2.0 V, I_{BUS} = 50 mA)	$V_{L(BUS)}$	–	0.4	0 7	V
Receiver Output Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0 5 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage – Low Logic State ($V_{IL(DA)}$ = 0 8 V, $V_{IL(D)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	0.25	0.4	V
Receiver Output Short Circuit Current (Note 1) ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, V_{CC} = 5.25 V)	$I_{OS(R)}$	-18	–	-55	mA
Power Supply Current ($V_{IL(DA)}$ = 0 V, $V_{IH(D)}$ = 2.0 V)	I_{CC}	–	50	70	mA
Input Clamp Diode Voltage – (T_A = 25°C) ($I_{I(DA)}$ = $I_{I(D)}$ = I_{BUS} = -12 mA)	V_I	–	-1.0	-1.5	V

NOTE 1: Only one output at a time

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Disable Input to High Logic Level Output	$t_{PLH(DA)}$	–	19	30	ns
Propagation Delay Time from Disable Input to Low Logic Level Output	$t_{PHL(DA)}$	–	15	23	ns
Propagation Delay Time from Driver Input to High Logic Level Output	$t_{PLH(D)}$	–	17	25	ns
Progpgation Delay Time from Drive Input to Low Logic Level Output	$t_{PHL(D)}$	–	9.0	15	ns
Propagation Delay Time from Bus Input to High Logic Level Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Bus Input to Low Logic Level Output	$t_{PHL(R)}$	–	18	30	ns

FIGURE 2 – DRIVER AND DISABLE TEST CIRCUIT AND WAVEFORMS

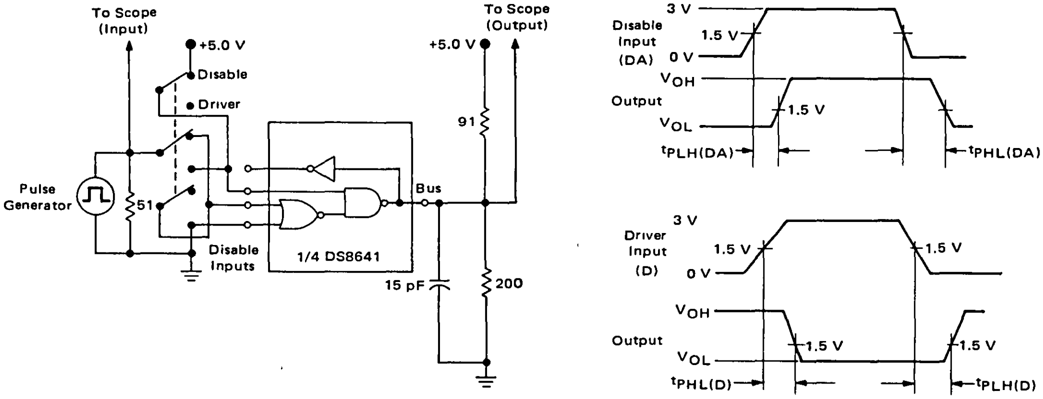
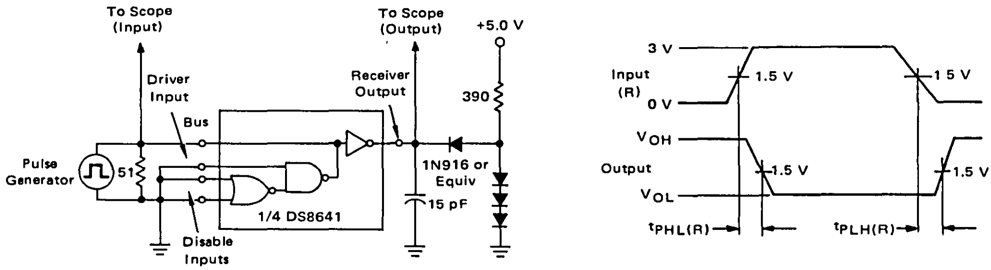
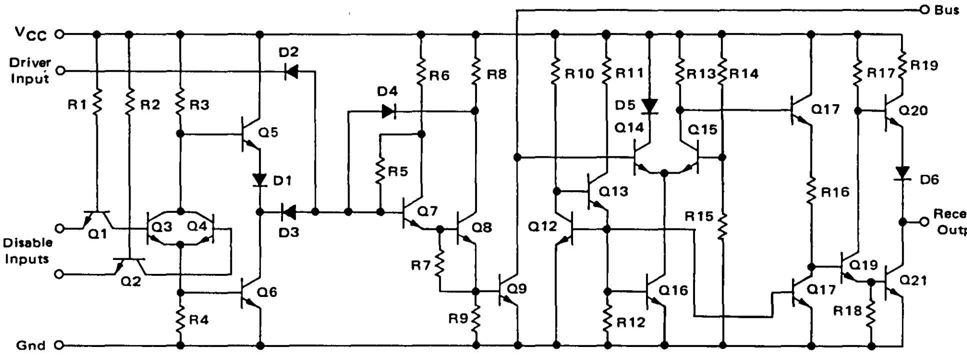


FIGURE 3 – RECEIVER TEST CIRCUIT AND WAVEFORM



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 Shown)



MC8T13
MC8T23

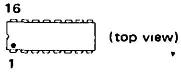
DUAL LINE DRIVERS

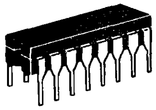
SILICON MONOLITHIC INTEGRATED CIRCUIT

DUAL LINE DRIVERS

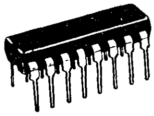
The MC8T13 and MC8T23 are designed to drive transmission lines with impedances of 50 Ω to 500 Ω. The MC8T23 specifically meets all of the input/output requirements of the IBM System 360/System 370 specifications (IBM Specification GA 22-6974-0).

- High Output Drive Capability –
  I_O = -75 mA (Min) @ V_O = 2.4 V – MC8T13
  I_O = -59.3 mA (Min) @ V_O = 3.11 V – MC8T23
- High Speed Operation –
  $t_{PLH} = t_{PHL}$ = 20 ns (Max) with 50 Ω Load
- MTTL and MDTL Compatible Inputs
- Uncommitted Emitter Output Structures Permit Party-Line Operation
- Designed to Operate with MC8T14 or MC8T24 Line Receivers
- Outputs are Short-Circuit Protected
- Equivalent to SN75121 and SN75123 Respectively.



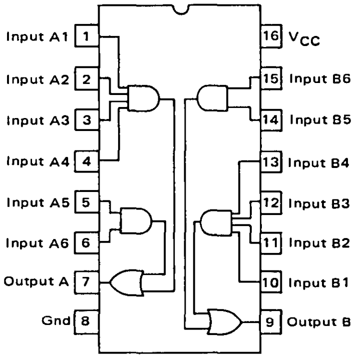


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

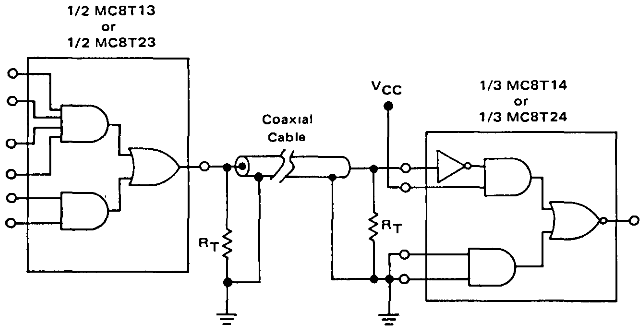


TRUTH TABLE

Inputs						Output
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Combinations						L

H = High Logic State
L = Low Logic State
X = Irrelevant

TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Output Voltage	V_O	7.0	Vdc
Power Dissipation @ T_A = +25°C Derate above 25°C	P_D	1000 6.7	mW. mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

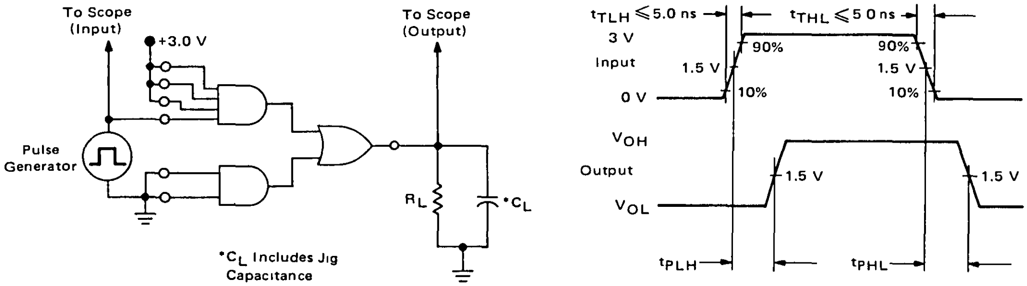
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V and 0°C $\leqslant T_A \leqslant$ 75°C)

Characteristics	Symbol	MC8T13			MC8T23			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	–	–	2.0	–	–	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	-0.1	–	-1.6	-0.1	–	-1.6	mA
Input Current — High Logic State (V_{IH} = 4.5 V)	I_{IH1}	–	–	40	–	–	40	µA
(V_{IH} = 5.5 V, V_{CC} = 5.0 V)	I_{IH2}	–	–	10	–	–	10	mA
Input Clamp Voltage (I_I = -12 mA, V_{CC} = 5.0 V)	$V_{I(clamp)}$	–	–	-1.5	–	–	-1.5	V
Output Voltage — High Logic State (V_{IH} = 2.0 V, I_{OH} = -75 mA)	V_{OH1}	2.4	–	–	–	–	–	V
(V_{CC} = 5.0 V, V_{IH} = 2.0 V, I_{OH} = -59.3 mA)	V_{OH2}	–	–	–	2.9	–	–	V
(T_A = 25°C)		–	–	–	3.11	–	–	
Output Current — High Logic State (V_{IH} = 4.5 V, V_{CC} = 5.0 V, V_O = 2.0 V, T_A = 25°C)	I_{OH}	-100	–	-250	-100	–	-250	mA
Output Current — Low Logic State (V_{IL} = 0.8 V, V_O = 0.4 V)	I_{OL1}	–	–	-800	–	–	–	µA
(V_{IL} = 0.8 V, V_O = 0.15 V)	I_{OL2}	–	–	–	–	–	-240	µA
Output Reverse Leakage Current — Low Logic State (V_{IL} = 0 V, V_O = 3.0 V)	I_{OR1}	–	–	80	–	–	–	µA
(V_{IL} = 0 V, V_O = 3.0 V, V_{CC} = 0 V)	I_{OR2}	–	–	500	–	–	40	µA
Output Short-Circuit Current (V_{IH} = 4.5 V, V_{CC} = 5.0 V, V_O = 0 V, T_A = 25°C)	I_{OS}	–	–	-30	–	–	-30	mA
Power Supply Currents (I_O = 0 mA) Outputs — Low Logic State, V_{IL} = 0.8 V	I_{CCL}	–	–	60	–	–	60	mA
Outputs — High Logic State, V_{IH} = 2.0 V	I_{CCH}	–	–	28	–	–	28	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.) Figure 1

Characteristic	Symbol	MC8T13			MC8T23			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — Low to High Level Output	t_{PLH}							ns
(R_L = 37 Ω, C_L = 15 pF)		–	11	20	–	–	–	
(R_L = 37 Ω, C_L = 1000 pF)		–	22	50	–	–	–	
(R_L = 50 Ω, C_L = 15 pF)		–	–	–	–	12	20	
(R_L = 50 Ω, C_L = 100 pF)		–	–	–	–	20	35	
Propagation Delay Time — High to Low Level Output	t_{PHL}							ns
(R_L = 37 Ω, C_L = 15 pF)		–	8.0	20	–	–	–	
(R_L = 37 Ω, C_L = 1000 pF)		–	20	50	–	–	–	
(R_L = 50 Ω, C_L = 15 pF)		–	–	–	–	12	20	
(R_L = 50 Ω, C_L = 100 pF)		–	–	–	–	15	25	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



Input Pulse Width 200 ns, 50% Duty Cycle

FIGURE 2 – REPRESENTATIVE SCHEMATIC DIAGRAM
(1/2 Shown)

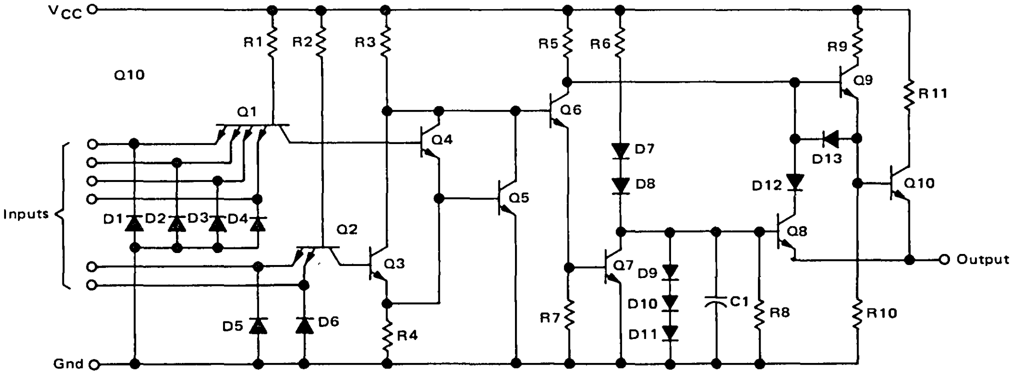
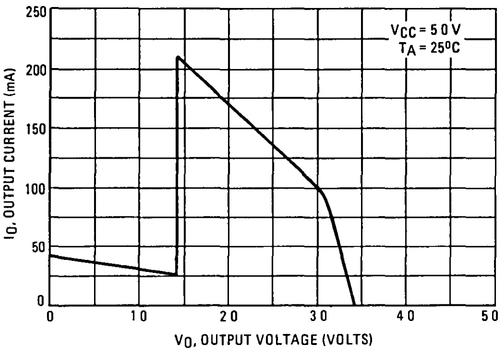


FIGURE 3 – TYPICAL OUTPUT CURRENT
versus OUTPUT VOLTAGE

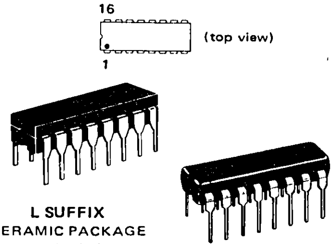


MOTOROLA

MC8T14
MC8T24

TRIPLE LINE RECEIVERS WITH HYSTERESIS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

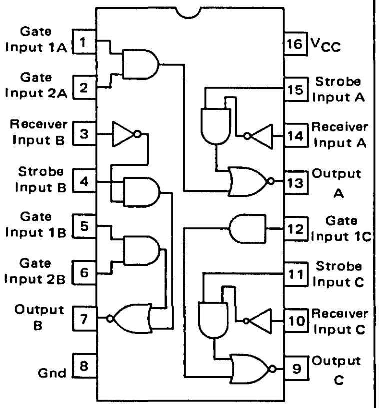
P SUFFIX
PLASTIC PACKAGE
CASE 648

TRIPLE LINE RECEIVERS WITH HYSTERESIS

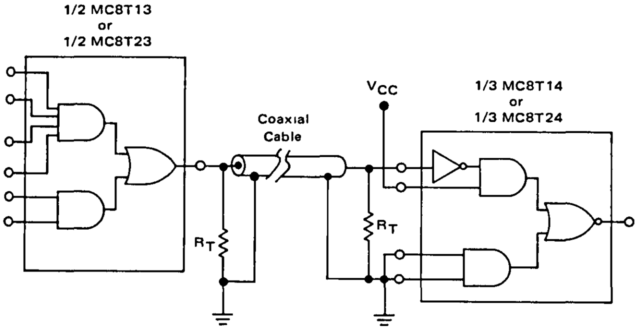
. . . specifically designed to meet the input/output specifications for IBM 360/370 Systems (IBM specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and also high input impedance to minimize loading on the related driver.

- Each Channel Can Be Independently Strobed
- High Speed — $t_{PLH} = t_{PHL} = 20$ ns
- Input Gating Provided on Each Line
- Operates on a Single +5.0 V Power Supply
- Fully Compatible with MTTL or MDTL Logic Systems
- Input Hysteresis Results in High Noise Immunity

PIN CONNECTIONS



TYPICAL APPLICATION



TRUTH TABLE

Inputs				Output
Receiver	Strobe	Gate 1	Gate 2	
X	X	H	H	L
L	H	X	X	L
H	X	L	X	H
X	L	L	X	H
H	X	X	L	H
X	L	X	L	H

Where:
L = Low Logic State
H = High Logic State
X = Don't Care

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Receiver Input Voltage (V_{CC} = 0)	$V_{I(R)}$	7.0 6.0	Vdc
Strobe or Gate Input Voltage	$V_{I(S) \text{ or } (G)}$	5.5	Vdc
Output Voltage	V_O	7.0	Vdc
Output Current	I_O	±100	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above 25°C	P_D	 1000 6.7	 mW mW/°C
Plastic Package Derate above 25°C		830 6.7	mW mW/°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	MC8T14			MC8T24			Unit
		Min	Typ	Max	Min	Typ	Max	
Gate or Strobe Input Voltage — High Logic State	$V_{IH(G) \text{ or } (S)}$	2.0	–	–	2.0	–	–	V
Gate or Strobe Input Voltage — Low Logic State	$V_{IL(G) \text{ or } (S)}$	–	–	0 8	–	–	0.8	V
Receiver Input Voltage — High Logic State	$V_{IH(R)}$	2.0	–	–	1.7	–	–	Vdc
Receiver Input Voltage — Low Logic State	$V_{IL(R)}$	–	–	0.8	–	–	0.7	Vdc
Receiver Input Hysteresis (1) (V_{CC} = 5.0 V, T_A = 25°C, $V_{IL(G)}$ = 0, $V_{IH(S)}$ = 4.5 V)	$V_{H(R)}$	0.3	0.5	–	0.2	0.4	–	V
Input Clamp Voltage (V_{CC} = 5 0 V, T_A = 25°C, I_I = -12 mA) (Strobe or Gate Inputs)	$V_{IC(G) \text{ or } (S)}$	–	–	1.5	–	–	1.5	V
Input Breakdown Voltage (V_{CC} = 5.0 V, I_I = 10 mA) (Strobe or Gate Inputs)	$V_{I(G) \text{ or } (S)}$	5.5	–	–	5.5	–	–	V
Receiver Input Current — High Logic State ($V_{IH(R)}$ = 3 8 V) ($V_{IH(R)}$ = 3.11 V) ($V_{IH(R)}$ = 7 0 V) ($V_{IH(R)}$ = 6.0 V, V_{CC} = 0 V)	$I_{IH(R)}$	 – – – –	 – – – –	 0.17 – – –	 – – – –	 – – – –	 – 0.17 5.0 5.0	mA
Gate or Strobe Input Current — High Logic State ($V_{IH(S)}$ = 4.5 V, $V_{IH(R)}$ = 3.11 V) ($V_{IH(G)}$ = 4.5 V)	$I_{IH(G) \text{ or } (S)}$	 – –	 – –	 40 40	 – –	 – –	 40 40	µA
Gate or Strobe Input Current — Low Logic State ($V_{IL(G) \text{ or } (S)}$ = 0.4 V, $V_{IL(R)}$ = 0 V)	$I_{IL(G) \text{ or } (S)}$	-0.1	–	-1.6	-0.1	–	-1.6	mA
Output Voltage — High Logic State ($V_{IH(R)}$ = 2 0 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 µA) ($V_{IH(R)}$ = 0 8 V, $V_{IL(S)}$ = 0 8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 µA) ($V_{IH(R)}$ = 1.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 µA) ($V_{IH(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 µA)	V_{OH}	 2.6 2.6 – –	 3.5 3.5 – –	 – – – –	 – – 2.6 2.6	 – – 3.4 3.4	 – – – –	V
Output Voltage — Low Logic State ($V_{IL(R)}$ = 0.8 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0 8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.8 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2.0 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2 0 V, I_{OL} = 16 mA)	V_{OL}	 – – – –	 – – – –	 0.4 0 4 – –	 – – – –	 – – – –	 – – 0.4 0.4	V
Output Short-Circuit Current (2) ($V_{IH(R)}$ = 3.8 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0, V_{CC} = 5.0 V, T_A = 25°C) ($V_{IH(R)}$ = 3.11 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0 V, V_{CC} = 5.0 V, T_A = 25°C)	I_{OS}	 -50 –	 – –	 -100 –	 – -50	 – –	 – -100	mA
Power Supply Current (V_{CC} = 5.25 V, T_A = 25°C)	I_{CC}	–	60	72	–	60	72	mA

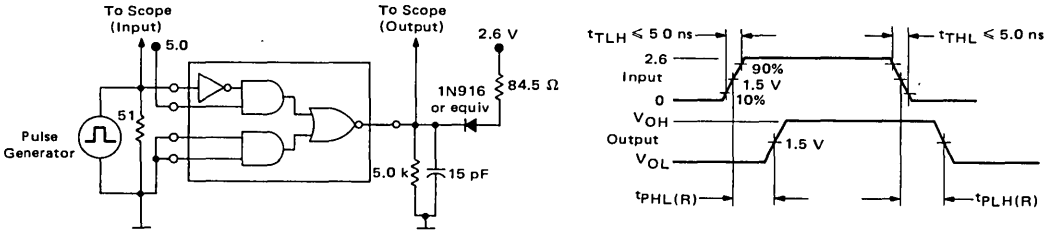
(1) The Input Hysteresis is defined as the difference the input voltage at which the output begins to go from the high logic state to the low logic state and the input voltage which causes the output to begin to go from the low logic state to the high logic state.

(2) Only one output may be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

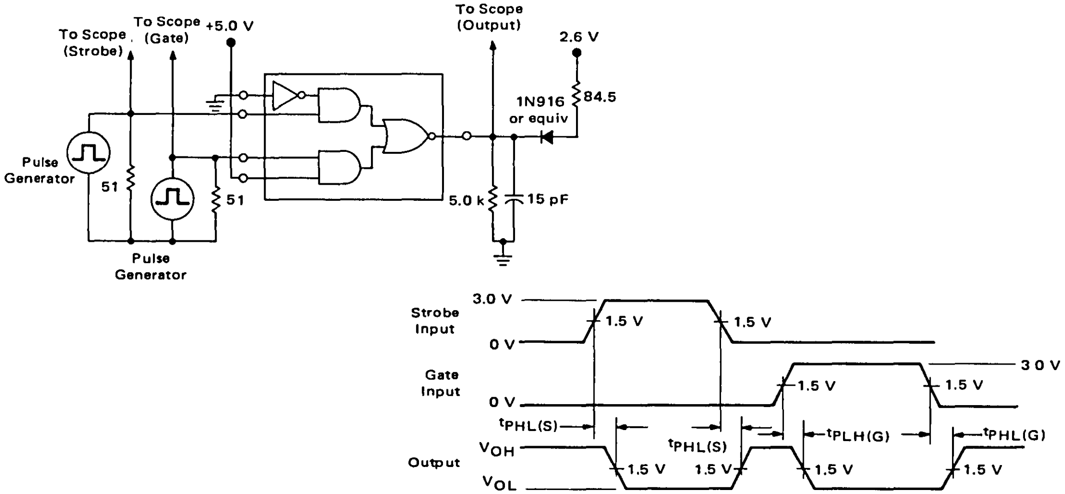
Parameter	Symbol	MC8T14, MC8T24			Unit
		Min	Typ	Max	
Propagation Delay Time – Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	20	30	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	–	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	–	–	ns
Propagation Delay Time Gate Input to High Logic State Output	$t_{PLH(G)}$	–	–	–	ns
Propagation Delay Time Gate Input to Low Logic State Output	$t_{PHL(G)}$	–	–	–	ns

FIGURE 1 – RECEIVER PROPAGATION DELAY TIMES $t_{PLH(R)}$ and $t_{PHL(R)}$ TEST CIRCUIT AND WAVEFORMS



Input Pulse Width = 200 ns
Duty Cycle = 50%

FIGURE 2 – GATE AND STROBE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



Input Pulse Width = 200 ns
Duty Cycle = 50 ns
$t_{TLH} = t_{THL} \leq 5.0$ ns

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTIC

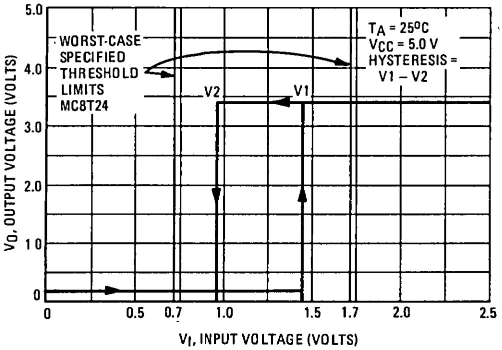
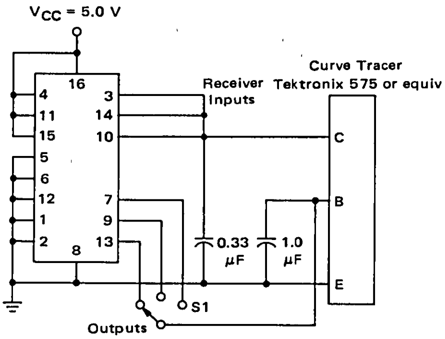
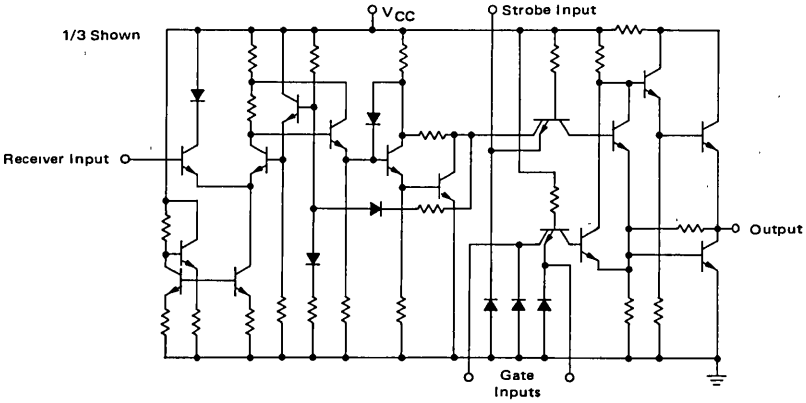


FIGURE 4 – HYSTERESIS TEST CIRCUIT



REPRESENTATIVE CIRCUIT SCHEMATIC



MC26S10
MC26S11

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

These quad transceivers are designed to mate Schottky TTL or NMOS logic to a low impedance bus. The $\overline{\text{Enable}}$ and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

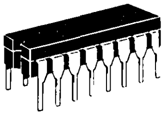
An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

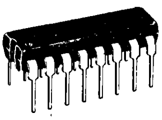
- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver — MC26S10
  Non-Inverting — MC26S11

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUIT

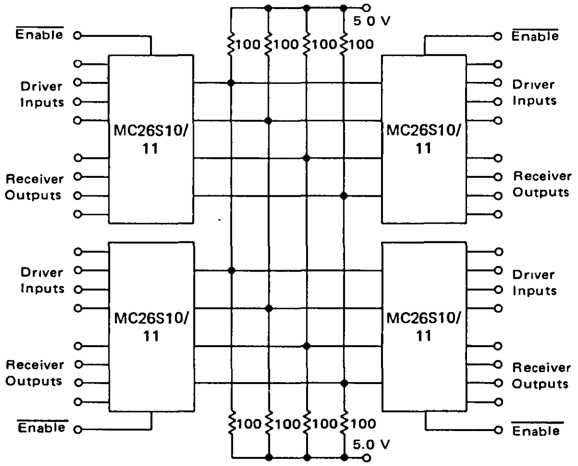


L SUFFIX
CERAMIC PACKAGE
CASE 620

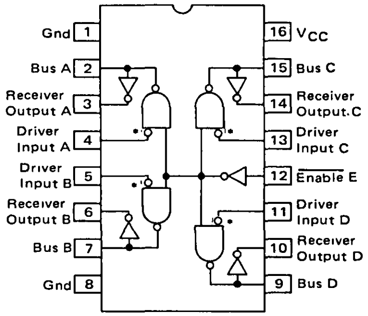


P SUFFIX
PLASTIC PACKAGE
CASE 648

TYPICAL APPLICATION



PIN CONNECTIONS



•Inverter on MC26S11 only

TRUTH TABLE

Enable	Driver Input	Bus 26S10	Bus 26S11	Receiver Output
L	L	H	L	L
L	H	L	H	H
H	X	Y	Y	Y

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_I	-0.5 to +5.5	Vdc
Input Current	I_I	-3.0 to +5.0	mA
Output Voltage – High Impedance State	$V_{O\ (Hi\text{-}z)}$	-0.5 to V_{CC}	V
Output Current–Bus	$I_{o(B)}$	200	mA
Output Current–Receiver	$I_{o(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	–	–	0.8	V
Input Voltage – High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	–	–	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = -18 mA)	V_{IK}	–	–	-1.2	V
Input Current – Low Logic State (V_{IL} = 0.4 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IL}	 – –	 – –	 -0.36 -0.54	mA
Input Current – High Logic State (V_{IH} = 2.7 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IH}	 – –	 – –	 20 30	µA
Input Current – Maximum Voltage (V_{IH1} = 5.5 V) ($\overline{\text{Enable}}$ or Driver Inputs)	I_{IH1}	–	–	100	µA
Driver Output Voltage – Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 – – –	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 – –	 – –	 100 -50	µA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	–	–	100	µA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	–	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	–	2.0	1.75	V
Receiver Output Voltage – Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Voltage – High Logic State (I_{OH} = -1.0 mA)	$V_{OH(R)}$	2.7	3.4	–	V
Receiver Output Short-Circuit Current (Note 1)	$I_{OS(R)}$	-18	–	-60	mA
Power Supply Current – Output Low State ($V_{IL(\overline{E})}$ = 0 V) MC26S10 MC26S11	I_{CC}	 – –	 45 –	 70 80	mA

NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC26S10			MC26S11			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$ $t_{PHL(D)}$	– –	10 10	15 15	– –	12 12	19 19	ns
Propagation Delay Time Enable Input to Output	$t_{PLH(\overline{E})}$ $t_{PHL(\overline{E})}$	– –	14 13	18 18	– –	15 14	20 20	ns
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$ $t_{PHL(R)}$	– –	10 10	15 15	– –	10 10	15 15	ns
Rise and Fall Time of Driver Output	$t_{TLH(D)}$ $t_{THL(D)}$	4.0 2.0	10 4.0	– –	4.0 2.0	10 4.0	– –	ns

SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 – DATA INPUT TO BUS OUTPUT (DRIVER)

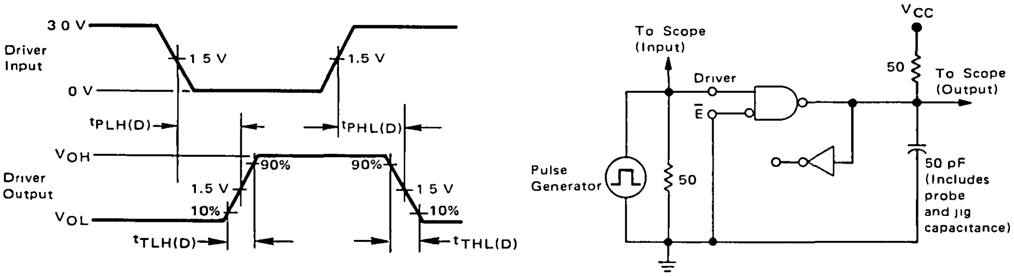


FIGURE 2 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

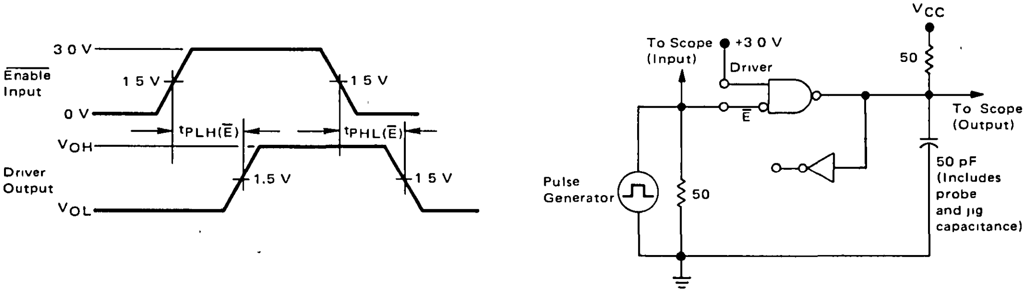
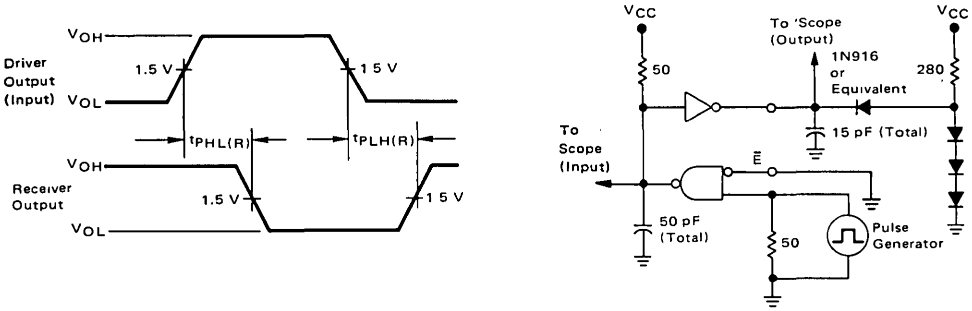


FIGURE 3 – BUS INPUT TO RECEIVER OUTPUT



MOTOROLA

MC75S110

MONOLITHIC DUAL LINE DRIVERS

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes for the MC75S110.

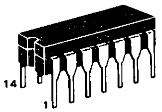
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of -3.0 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

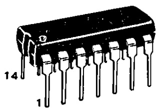
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- High Common-Mode Output Voltage Range (-3.0 V to +10 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS

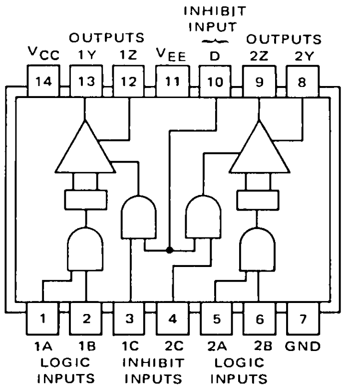
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state
High output represents the "off" state

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual In-Line Packages		1000	mW
Derate above T_A = +25°C		3.85	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}		°C
Ceramic Dual In-Line Package		-65 to +150	
Plastic Dual In-Line Package		-65 to +150	

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5 0 -5.0	+5.25 -5 25	Volts
Common-Mode Output Voltage Range	V_{OCR}				Volts
Positive		0	–	+10	
Negative		0	–	-3.0	

Note 1. These voltage values are in respect to the ground terminal

Note 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	1,2	2 0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	1,2	0	0 8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic # #	Symbol	Test Fig.	MC75S110			Unit
			Min	Typ #	Max	
High-Level Input Current to 1A, 1B, 2A or 2B	I_{IH_L}	1				
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)#			–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)			–	–	1 0	mA
Low-Level Input Current to 1A, 1B, 2A or 2B	I_{IL_L}	1				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)			–	–	-3 0	
High-Level Input Current into 1C or 2C	I_{IH_I}	2				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)			–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)			–	–	1.0	mA
Low-Level Input Current into 1C or 2C	I_{IL_I}	2				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0 4 V)			–	–	-3 0	
High-Level Input Current into D	I_{IH_I}	2				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)			–	–	80	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)			–	–	2 0	mA
Low-Level Input Current into D	I_{IL_I}	2				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)			–	–	-6 0	
Output Current ("on" state)	$I_{O(on)}$	3				mA
(V_{CC} = Max, V_{EE} = Max)			–	12	15	
(V_{CC} = Min, V_{EE} = Min)			6 5	–	–	
Output Current ("off" state)	$I_{O(off)}$	3				µA
(V_{CC} = Min, V_{EE} = Min)			–		100	
Supply Current from V_{CC} (with driver enabled)	$I_{CC(on)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)			–	28	35	
Supply Current from V_{EE} (with driver enabled)	$I_{EE(on)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)			–	-41	-50	
Supply Current from V_{CC} (with driver inhibited)	$I_{CC(off)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)			–	21	–	
Supply Current from V_{EE} (with driver inhibited)	$I_{EE(off)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)			–	-41	-50	

#All typical values are at V_{CC} = +5 0 V, V_{EE} = -5 0 V

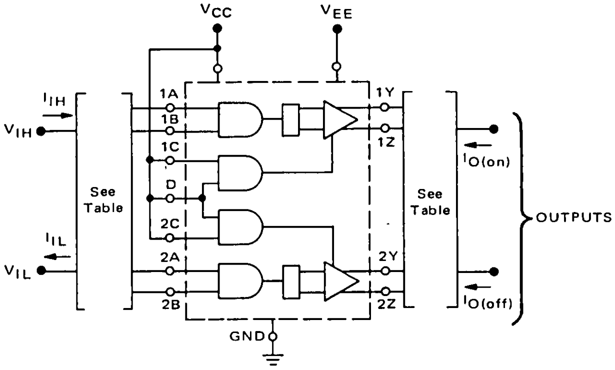
#For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

SWITCHING CHARACTERISTICS (V_{CC} = +5 0 V, V_{EE} = -5 0 V, T_A = +25°C.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)		5				ns
	t_{PLH_L}		–	9.0	15	
	t_{PHL_L}		–	9.0	15	
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)		5				ns
	t_{PLH_I}		–	16	25	
	t_{PHL_I}		–	13	25	

TEST CIRCUITS

FIGURE 1 – V_{IH}, V_{IL}, I_{IH}, and I_{IL}

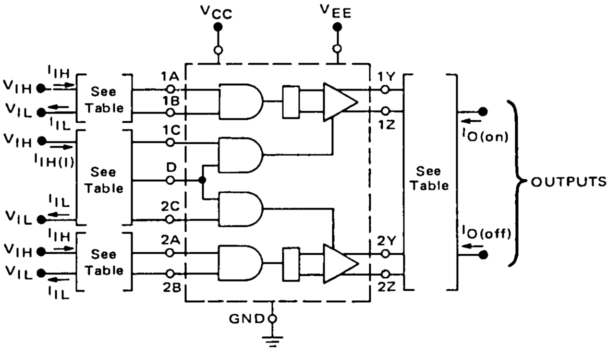


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_L}	Open	V_{IH_I}	H (See Note 1)	L (See Note 1)
V_{IL_L}	V_{CC}	V_{IH_I}	L (See Note 1)	H (See Note 1)
I_{IH_L}	4.5 V	V_{IH_I}	Gnd	Gnd
I_{IL_L}	Gnd	V_{IH_I}	Gnd	Gnd

NOTES. 1. Low output represents the "on" state, high output represents the "off" state.
2. Each input is tested separately.
3 Arrows indicate actual direction of current flow.

FIGURE 2 – V_{IH}, V_{IL}, I_{IH}, I_{IL}

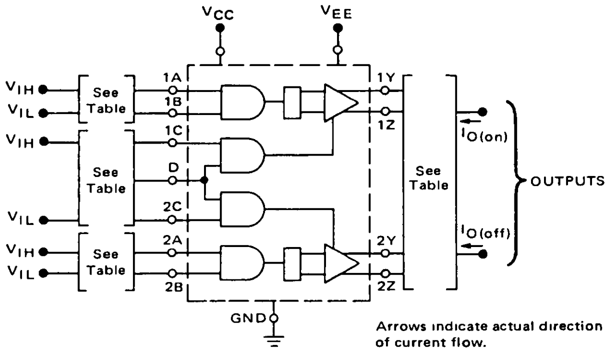


TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_I}	V_{IH_L}	Open	H(See Note 1)	L(See Note 1)
	V_{IL_L}	Open	L(See Note 1)	H(See Note 1)
V_{IL_I}	V_{IH_L}	V_{CC}	H(See Note 1)	H(See Note 1)
	V_{IL_L}	V_{CC}	H(See Note 1)	H(See Note 1)
I_{IH_I}	Gnd	4 5 V	Gnd	Gnd
I_{IL_I}	Gnd	Gnd	Gnd	Gnd

TEST CIRCUITS (continued)

FIGURE 3 – $I_{O(on)}$ and $I_{O(off)}$

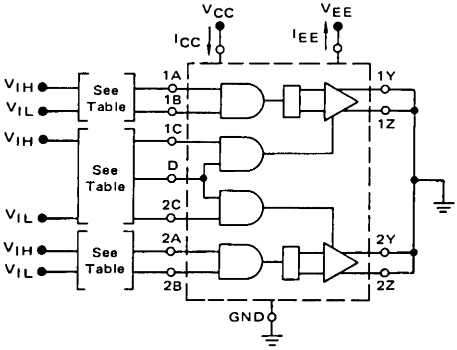


Arrows indicate actual direction of current flow.

TEST TABLE

TEST Ground all output pins not under test.		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

FIGURE 4 – I_{CC} and I_{EE}

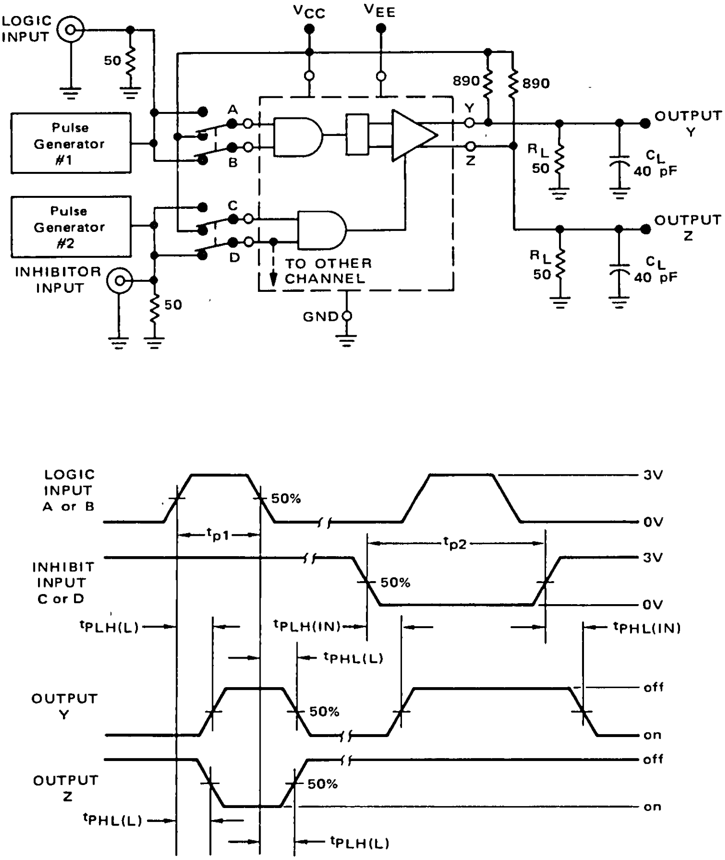


TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{EE(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{CC(off)}$	Driver inhibited	V_{IL}	V_{IL}
$I_{EE(off)}$	Driver inhibited	V_{IL}	V_{IL}

TEST CIRCUITS (continued)

FIGURE 5 – PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



NOTES:
1. The pulse generators have the following characteristics: $z_O = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

MOTOROLA

MC1411 (ULN2001A)
MC1412 (ULN2002A)
MC1413 (ULN2003A)
MC1416 (ULN2004A)

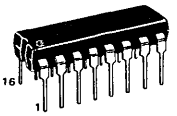
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington-connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412 contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 kΩ series input resistor is well suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 kΩ resistor and is useful in 8-18 Volt MOS systems.

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



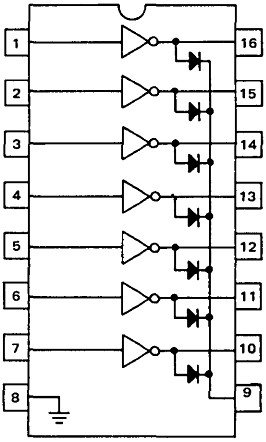
P SUFFIX
PLASTIC PACKAGE.
CASE 648

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Maximum Package Power Dissipation (See Thermal Information Section)
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



DEVICE CROSS-REFERENCE LISTING

9665 – SN75476 – ULN2001A – order MC1411P
9666 – SN75477 – ULN2002A – order MC1412P
9667 – SN75478 – ULN2003A – order MC1413P
9668 – – ULN2004A – order MC1416P

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				µA
*(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
*(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
*(V_O = 50 V, T_A = +70°C, V_I = 6 0 V)	MC1412		–	–	500	
*(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	MC1416		–	–	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)			–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)			–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)			–	0.85	1.1	
Input Current – On Condition		$I_{I(on)}$				mA
(V_I = 17 V)	MC1412		–	0.85	1.3	
(V_I = 3.85 V)	MC1413		–	0.93	1.35	
(V_I = 5.0 V)	MC1416		–	0.35	0.5	
(V_I = 12 V)	MC1416		–	1.0	1.45	
Input Voltage – On Condition		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1412		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1413		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	MC1413		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1413		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	MC1416		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1416		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	MC1416		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	MC1416		–	–	8.0	
Input Current – Off Condition (I_C = 500 µA, T_A = +70°C)		$I_{I(off)}$	50	100	–	µA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	MC1411	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +70°C	I_R	–	–	50 100	µA
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	–	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES – T_A = 25°C

FIGURE 1 – OUTPUT CURRENT versus INPUT VOLTAGE

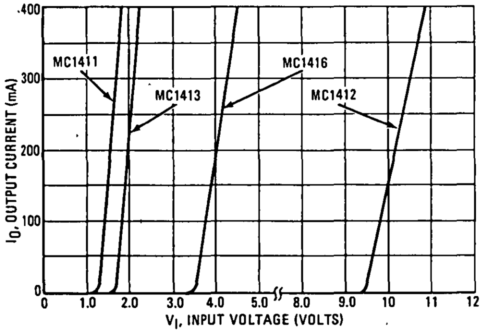
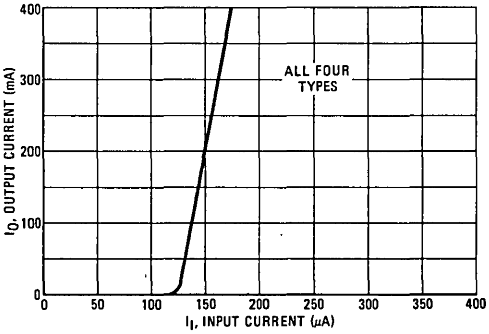


FIGURE 2 – OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES — T_A = 25°C (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

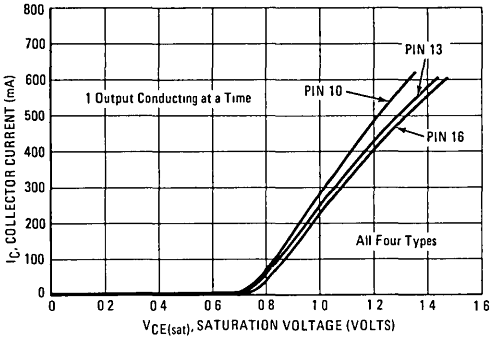


FIGURE 4 — INPUT CHARACTERISTICS — MC1412

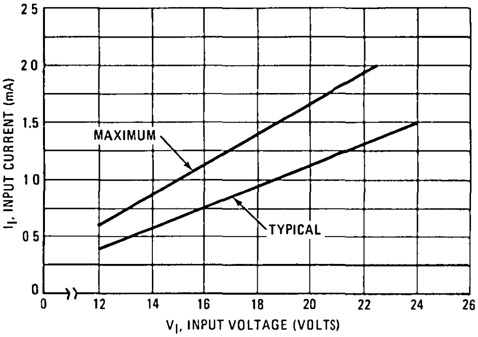


FIGURE 5 — INPUT CHARACTERISTICS — MC1413

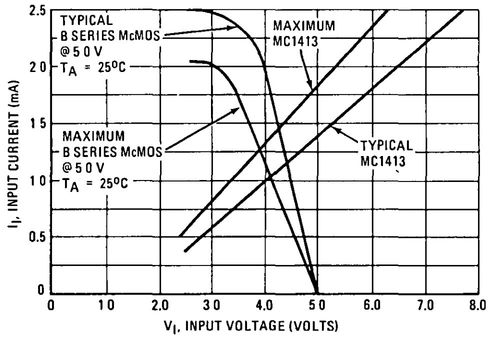


FIGURE 6 — INPUT CHARACTERISTICS — MC1416

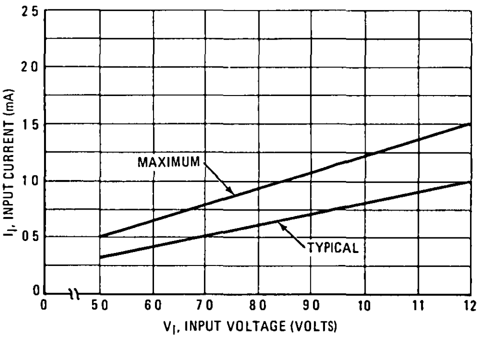
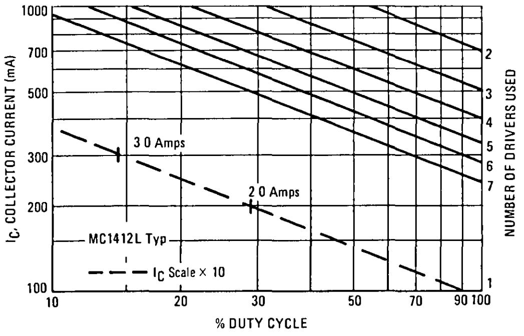
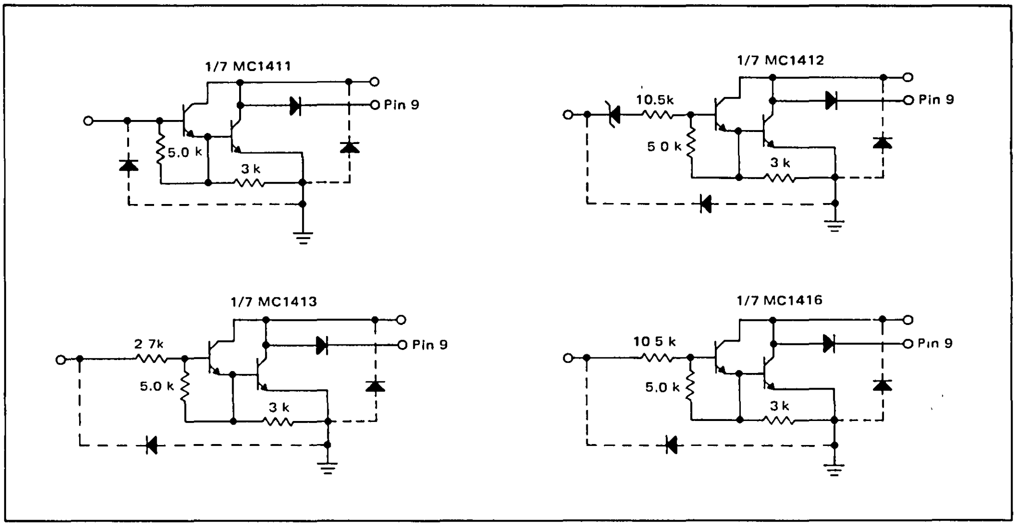


FIGURE 7 — MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE)



REPRESENTATIVE CIRCUIT SCHEMATICS



MOTOROLA

MC1472

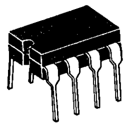
DUAL PERIPHERAL POSITIVE "NAND" DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUITS

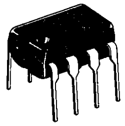
DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER

The dual driver consists of a pair of PNP-buffered AND gates connected to the bases of a pair of high-voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)



U SUFFIX
CERAMIC PACKAGE
CASE 693



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

CROSS REFERENCE
UDN-5712 – SN75475 – MC1472

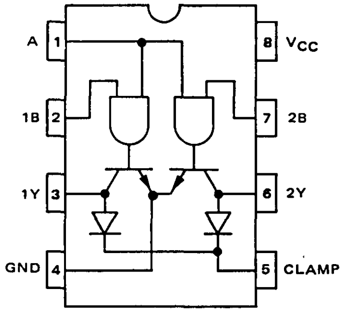
MAXIMUM RATINGS ($T_A = 25^\circ C$, Note 1).

Rating	Value	Unit
Supply Voltage	7.0	Volts
Input Voltage	5.5	Volts
Output Voltage	80	Volts
Clamp Voltage	80	Volts
Output Current (Continuous)	300	mA
Operating Junction Temperature		°C
Ceramic Package	+175	
Plastic Package	+150	
Storage Temperature Range	-65 to +150	°C

Note 1: "Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	°C
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts



Positive Logic: Y=AB•

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	H ("OFF" STATE)
H	L	H ("OFF" STATE)
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

ELECTRICAL CHARACTERISTICS Unless otherwise noted min/max limits apply accross the 0°C to 70°C temperature range with 4.5 V ± V_{CC} ± 5.5 V. All typical values are for T_A = 25°C, V_{CC} = 5 Volts.

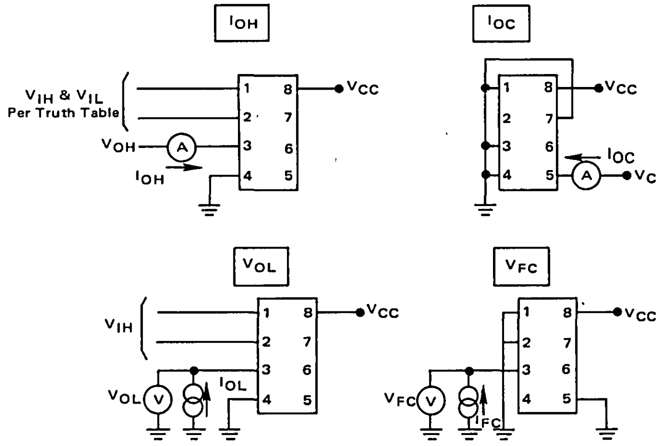
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	5.5	Vdc
Input Voltage – Low Logic State	V_{IL}	0	–	0.8	Vdc
Input Current – Low Logic State (V_{IL} = 0.4V) A Input B Input	I_{IL}	–	–	-0.3 -0.15	mA
Input Current – High Logic State (V_{IH} = 2.4V) A input B Input (V_{IH} = 5.5V) A Input B Input	I_{IH}	– – – –	– – – –	40 20 200 100	µA
Input Clamp Voltage (I_{IC} = -12mA)	V_{IC}	–	–	-1.5	V
Output Leakage Current – High Logic State (V_O = 70V, See test Figure)	I_{OH}	–	–	100	µA
Output Voltage – Low Logic State (I_{OL} = 100 mA) (I_{OL} = 300 mA)	V_{OL}	– –	– –	0.4 0.7	V
Output Clamp Diode Leakage Current (V_C = 70V, See test Figure)	I_{OC}	–	–	100	µA
Output Clamp Forward Voltage (I_{FC} = 300 mA See test Figure)	V_{FC}	–	–	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	– –	– –	15 70	mA

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

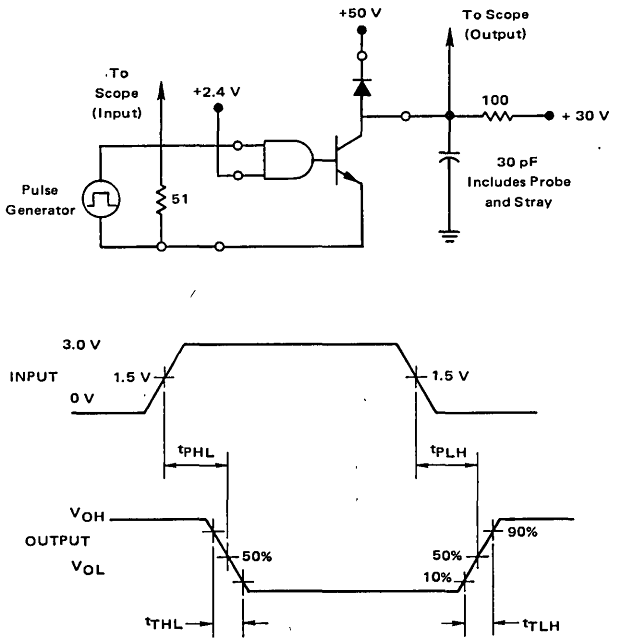
SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	t_{PHL} t_{PLH}	– –	– –	1.0 0.75	µs
Output Transition Time Output High to Low Output Low to High	t_{THL} t_{TLH}	– –	– –	0.1 0.1	µs

TEST CIRCUITS



SWITCHING TEST CIRCUIT AND WAVEFORM



MOTOROLA

MC1488

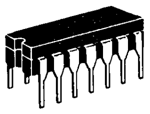
QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

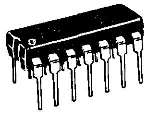
Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

QUAD MDTL LINE DRIVER
RS-232C
SILICON MONOLITHIC
INTEGRATED CIRCUIT

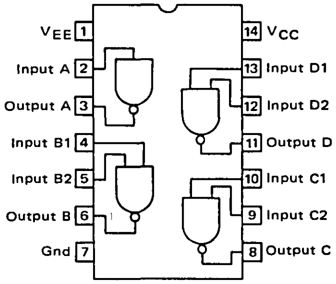


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

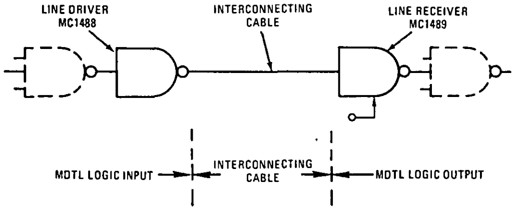


P SUFFIX
PLASTIC PACKAGE
CASE 646

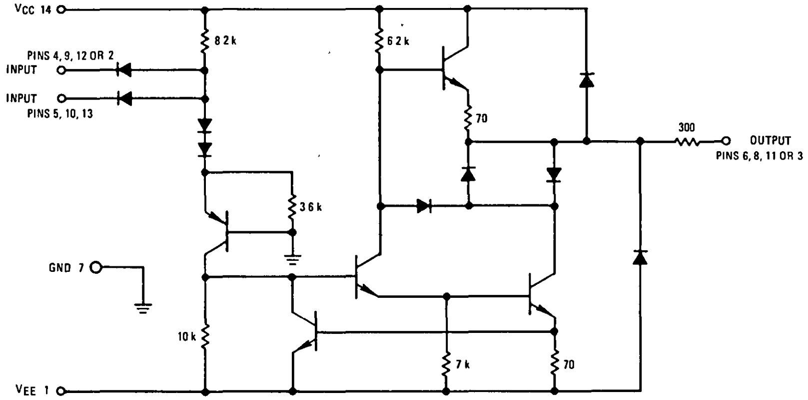
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = 0 to +75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (V_{IL} = 0)	1	I_{IL}	–	1.0	1.6	mA
Input Current – High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	–	–	10	µA
Output Voltage – High Logic State	2	V_{OH}				Vdc
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			+6.0	+7.0	–	
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			+9.0	+10.5	–	
Output Voltage – Low Logic State	2	V_{OL}				Vdc
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			-6.0	-7.0	–	
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			-9.0	-10.5	–	
Positive Output Short-Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current (1)	3	I_{OS-}	-6.0	-10	-12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ±2.0 V)	4	r_o	300	–	–	Ohms
Positive Supply Current (R_l = ∞)	5	I_{CC}				mA
(V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc)			–	+15	+20	
(V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc)			–	+4.5	+6.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc)			–	+19	+25	
(V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc)			–	+5.5	+7.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc)			–	–	+34	
(V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)			–	–	+12	
Negative Supply Current (R_L = ∞)	5	I_{EE}				
(V_{IH} = 1.9 Vdc, V_{EE} = -9.0 Vdc)			–	-13	-17	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -9.0 Vdc)			–	–	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -12 Vdc)			–	-18	-23	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -12 Vdc)			–	–	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -15 Vdc)			–	–	-34	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -15 Vdc)			–	–	-2.5	mA
Power Consumption		P_C				mW
(V_{CC} = 9.0 Vdc, V_{EE} = -9.0 Vdc)			–	–	333	
(V_{CC} = 12 Vdc, V_{EE} = -12 Vdc)			–	–	576	

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PLH}	–	275	350	ns
Fall Time (z_l = 3.0 k and 15 pF)	6	t_{THL}	–	45	75	ns
Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PHL}	–	110	175	ns
Rise Time (z_l = 3.0 k and 15 pF)	6	t_{TLH}	–	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

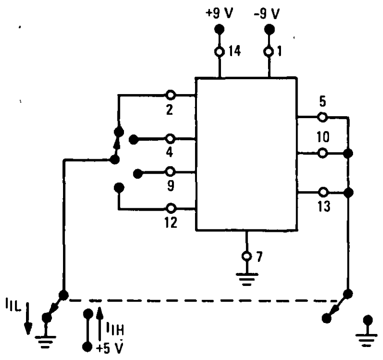


FIGURE 2 – OUTPUT VOLTAGE

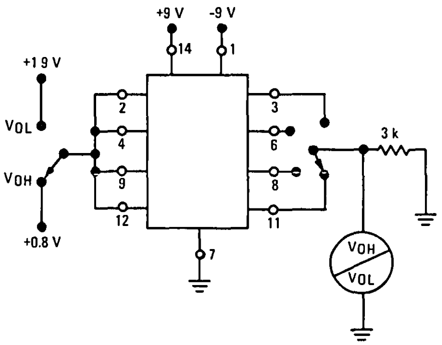


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

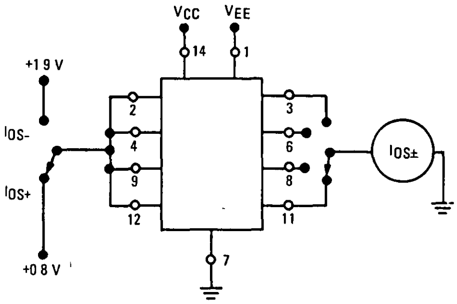


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

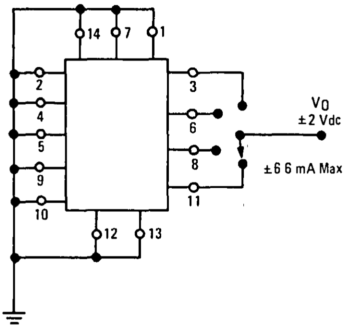


FIGURE 5 – POWER-SUPPLY CURRENTS

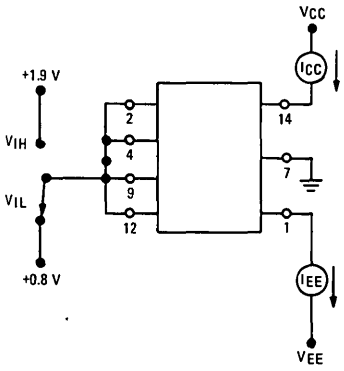
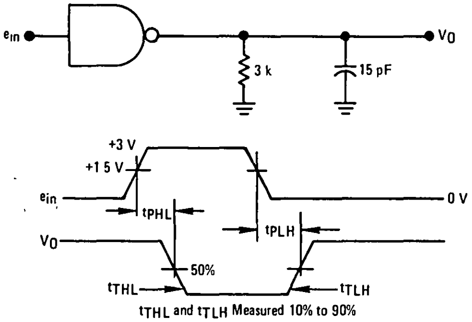


FIGURE 6 – SWITCHING RESPONSE



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

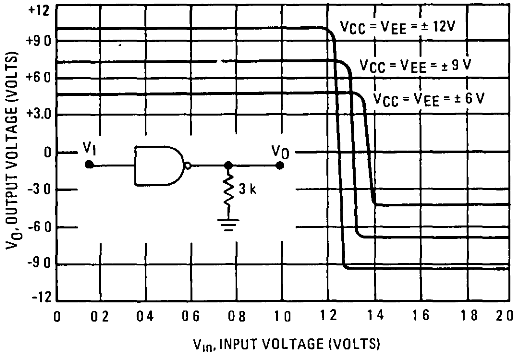


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

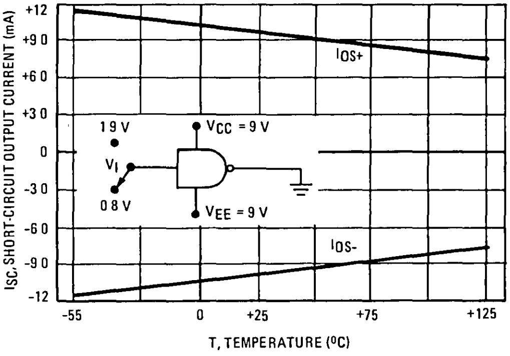


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

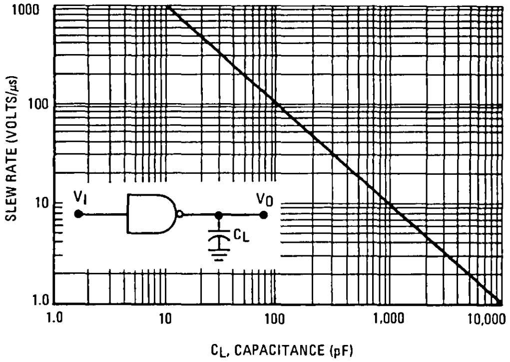


FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

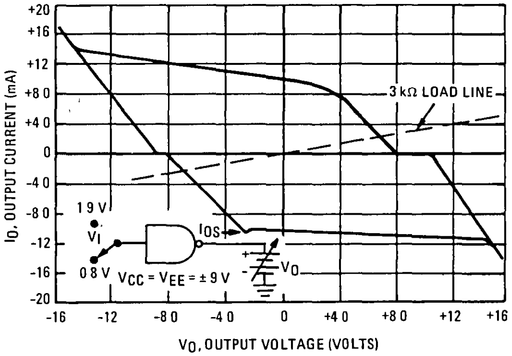
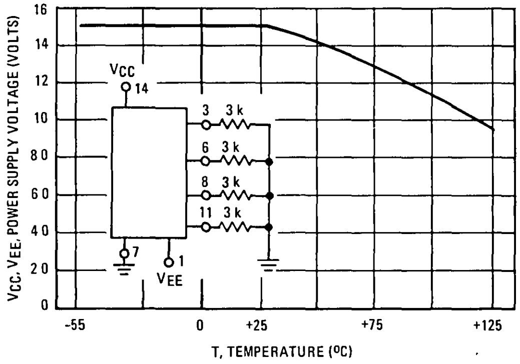


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



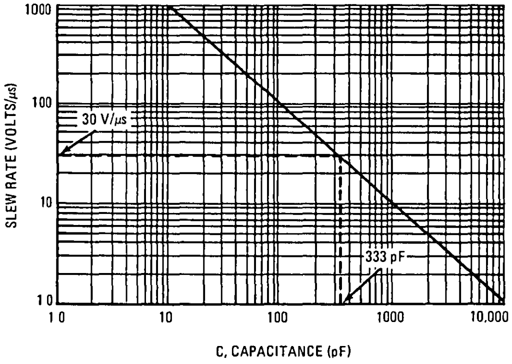
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

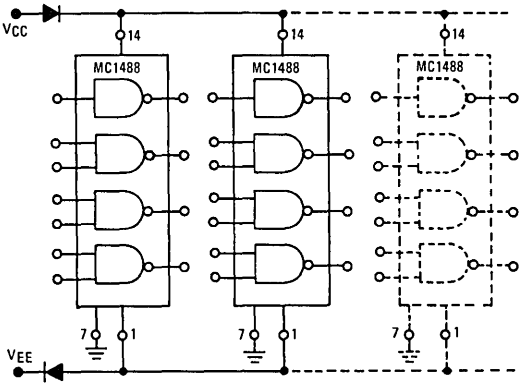
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

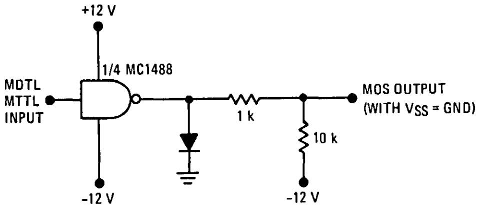
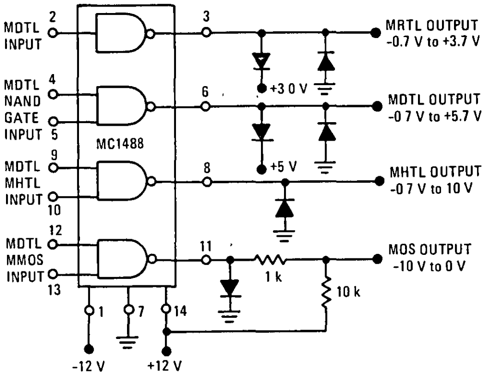


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



MOTOROLA

MC1489L
MC1489AL

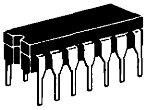
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

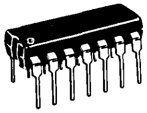
- Input Resistance — 3.0 k to 7.0 kilohms
- Input Signal Range — ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS RS-232C

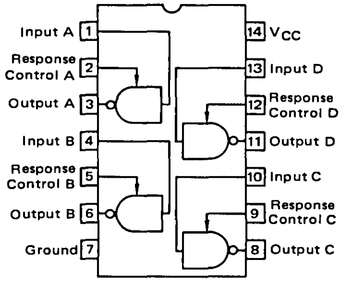
SILICON MONOLITHIC INTEGRATED CIRCUIT



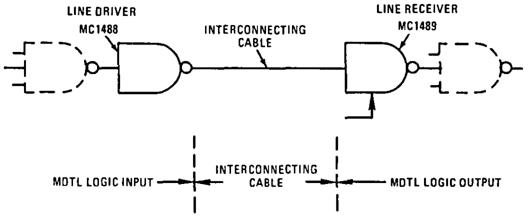
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



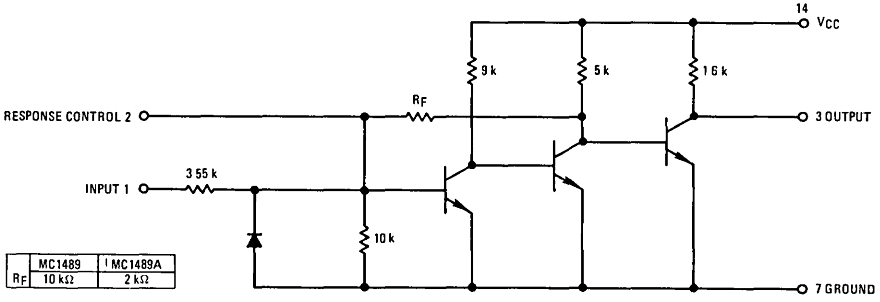
P SUFFIX
PLASTIC PACKAGE
CASE 646



TYPICAL APPLICATION



CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	10 kΩ	2 kΩ

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package)	P_D	1000	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	6.7	mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted)

Characteristics		Figure	Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc)	1	I_{IH}	3.6	–	8 3	mA
	(V_{IH} = +3.0 Vdc)			0.43	–	–	
Negative Input Current	(V_{IL} = -25 Vdc)	1	I_{IL}	-3 6	–	-8 3	mA
	(V_{IL} = -3.0 Vdc)			-0.43	-	–	
Input Turn-On Threshold Voltage		2	V_{IHL}				Vdc
(T_A = +25°C, V_{OL} ≤ 0 45 V)	MC1489			1.0	–	1.5	
	MC1489A			1 75	1.95	2.25	
Input Turn-Off Threshold Voltage		2	V_{ILH}				Vdc
(T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = -0 5 mA)	MC1489			0.75	–	1.25	
	MC1489A			0.75	0 8	1.25	
Output Voltage High	(V_{IH} = 0.75 V, I_L = -0.5 mA)	2	V_{OH}	2.6	4 0	5 0	Vdc
	(Input Open Circuit, I_L = -0.5 mA)			2.6	4 0	5 0	
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	2	V_{OL}	–	0 2	0.45	Vdc
Output Short-Circuit Current		3	I_{OS}	–	3.0	–	mA
Power Supply Current	(V_{IH} = +5 0 Vdc)	4	I_{CC}	–	20	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	4	P_C	–	100	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = +25°C)

Propagation Delay Time	(R_L = 3.9 kΩ)	5	t_{PLH}	–	25	85	ns
Rise Time	(R_L = 3 9 kΩ)	5	t_{TLH}	–	120	175	ns
Propagation Delay Time	(R_L = 390 Ω)	5	t_{PHL}	–	25	50	ns
Fall Time	(R_L = 390 Ω)	5	t_{THL}	–	10	20	ns

TEST CIRCUITS

FIGURE 1 – INPUT CURRENT

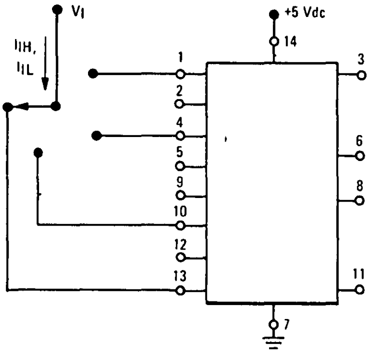


FIGURE 2 – OUTPUT VOLTAGE and INPUT THRESHOLD VOLTAGE

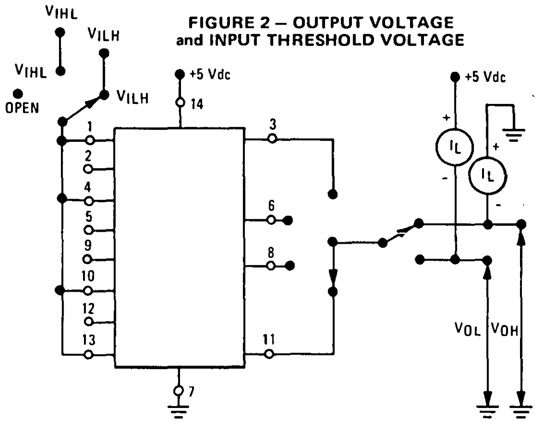


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

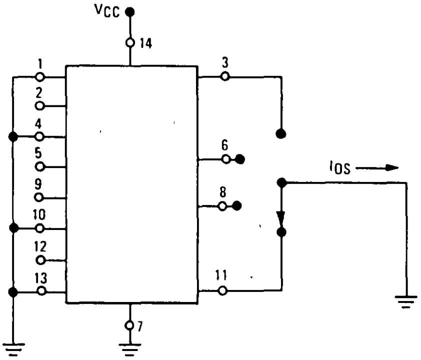


FIGURE 4 – POWER-SUPPLY CURRENT

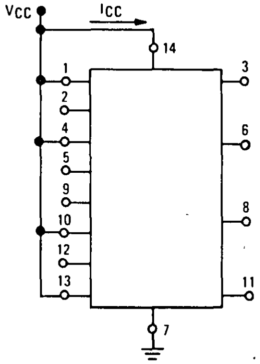
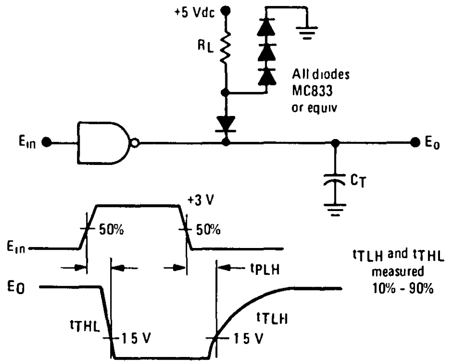
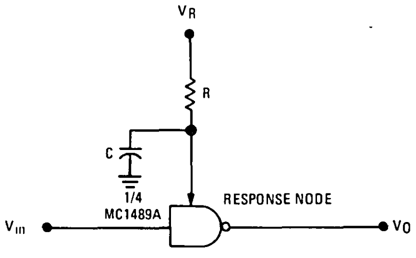


FIGURE 5 – SWITCHING RESPONSE



C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 6 – RESPONSE CONTROL NODE



C, capacitor is for noise filtering
R, resistor is for threshold shifting

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 7 – INPUT CURRENT

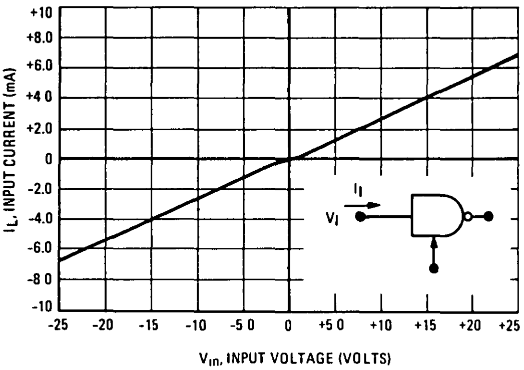


FIGURE 8 – MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

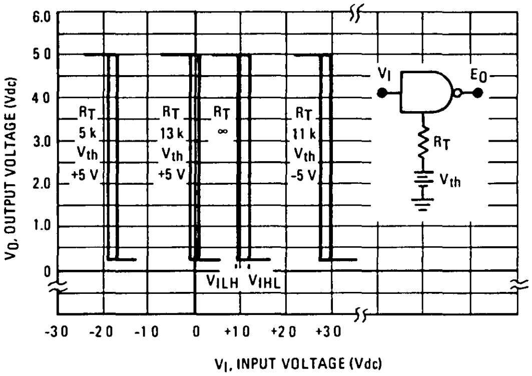


FIGURE 9 – MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

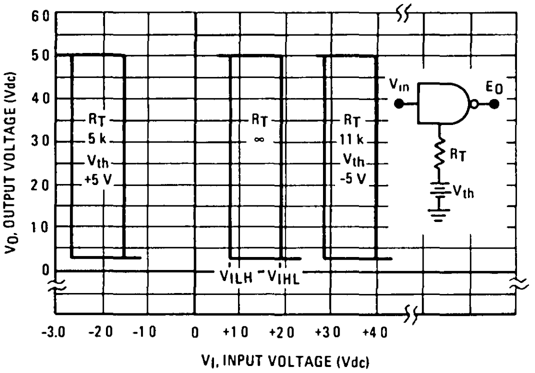


FIGURE 10 – INPUT THRESHOLD VOLTAGE versus TEMPERATURE

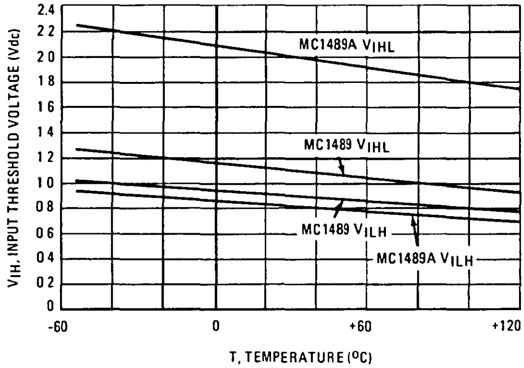
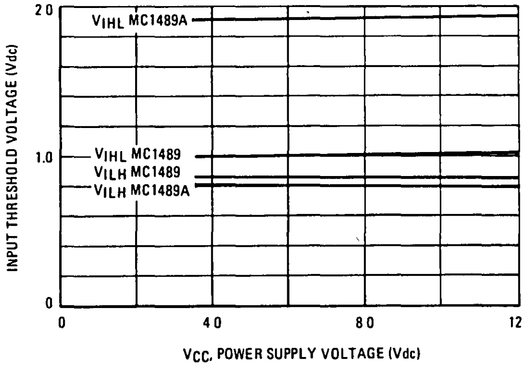


FIGURE 11 – INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels The RS-232C requirements as applied to receivers are discussed herein

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3 0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5) For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0 8 volt for typically 1 15 volts of hysteresis

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 12 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

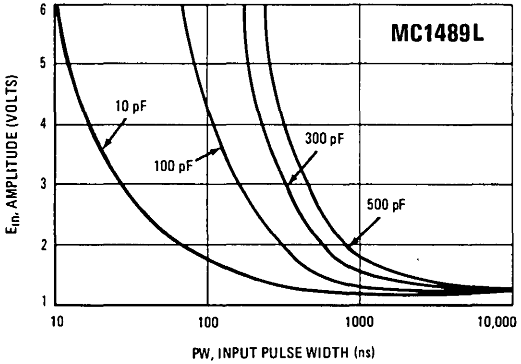
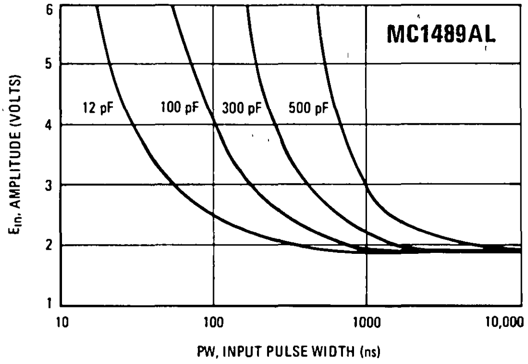


FIGURE 13 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 14 – TYPICAL TRANSLATOR APPLICATION – MOS TO DTL OR TTL

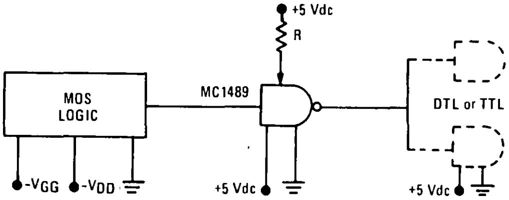
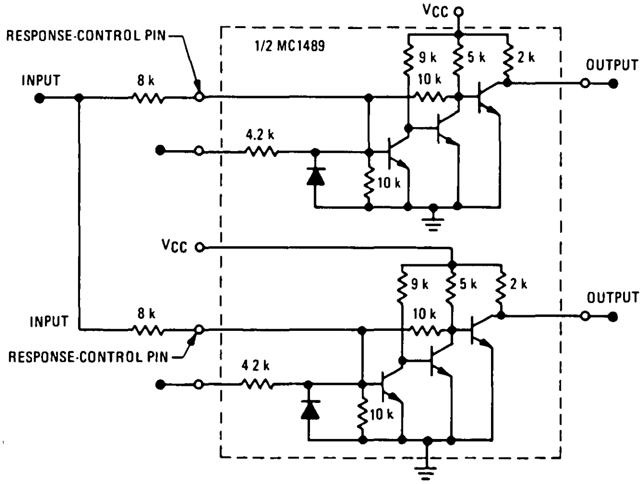


FIGURE 15 – TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



MOTOROLA

MC3437

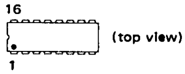
HEX BUS RECEIVER WITH INPUT HYSTERESIS

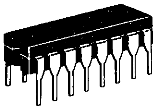
These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time – 20 ns (Typ)
- Direct Replacement for DS8837

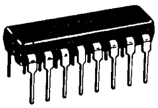
HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



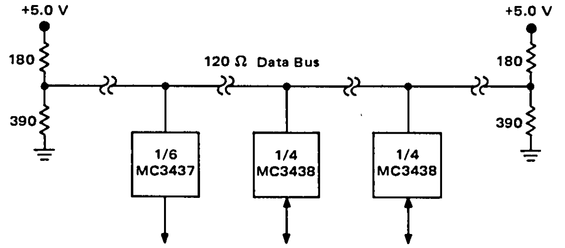


L SUFFIX
CERAMIC PACKAGE
CASE 620



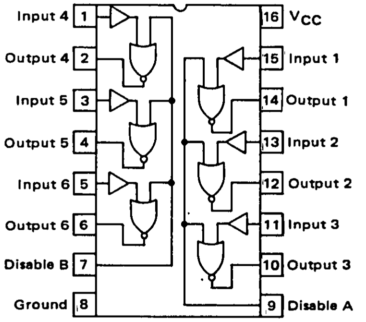
P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION



To Computer or Peripherals

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^{\circ}C$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage — High Logic State ($V_{IL(DA)} = 0.8$ V, $I_{OL} = 16$ mA, $V_{OL} \leq 0.4$ V)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage — Low Logic State ($V_{IL(DA)} = 0.8$ V, $I_{OH} = -400\ \mu A$, $V_{OH} \geq 2.4$ V)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(R)} = 4.0$ V, $V_{CC} = 5.25$ V) ($V_{I(R)} = 4.0$ V, $V_{CC} = 0$ V)	$I_{I(R)}$	 — —	 15 1.0	 50 50	μA
Disable Input Voltage — High Logic State ($V_{I(R)} = 0.5$ V, $V_{OL} \leq 0.4$ V, $I_{OL} = 16$ mA)	$V_{IH(DA)}$	2.0	—	—	V
Disable Input Voltage — Low Logic State ($V_{I(R)} = 0.5$ V, $V_{OH} \geq 2.4$ V, $I_{OH} = -400\ \mu A$)	$V_{IL(DA)}$	—	—	0.8	V
Output Voltage — High Logic State ($V_{I(R)} = 0.5$ V, $V_{IL(DA)} = 0.8$ V, $I_{OH} = -400\ \mu A$)	V_{OH}	2.4	—	—	V
Output Voltage — Low Logic State ($V_{I(R)} = 4.0$ V, $V_{IL(DA)} = 0.8$ V, $I_{OL} = 16$ mA)	V_{OL}	—	0.25	0.4	V
Disable Input Current — High Logic State ($V_{IH(DA)} = 2.4$ V) ($V_{IH(DA)} = 5.5$ V)	$I_{IH(DA)}$	 — —	 — —	 80 2.0	 μA mA
Disable Input Current — Low Logic State ($V_{I(R)} = 4.0$ V, $V_{IL(DA)} = 0.4$ V)	$I_{IL(DA)}$	—	—	-3.2	mA
Output Short Circuit Current ($V_{I(R)} = 0.5$ V, $V_{IL(DA)} = 0$ V, $V_{CC} = 5.25$ V)	I_{OS}	-18	—	-55	mA
Power Supply Current ($V_{I(R)} = 0.5$ V, $V_{IL(DA)} = 0$ V)	I_{CC}	—	45	70	mA
Input Clamp Diode Voltage ($I_{I(R)} = -12$ mA, $I_{I(DA)} = -12$ mA,	V_I	—	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0$ V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH(R)}$	—	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL(R)}$	—	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH(DA)}$	—	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL(DA)}$	—	4.0	15	ns

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

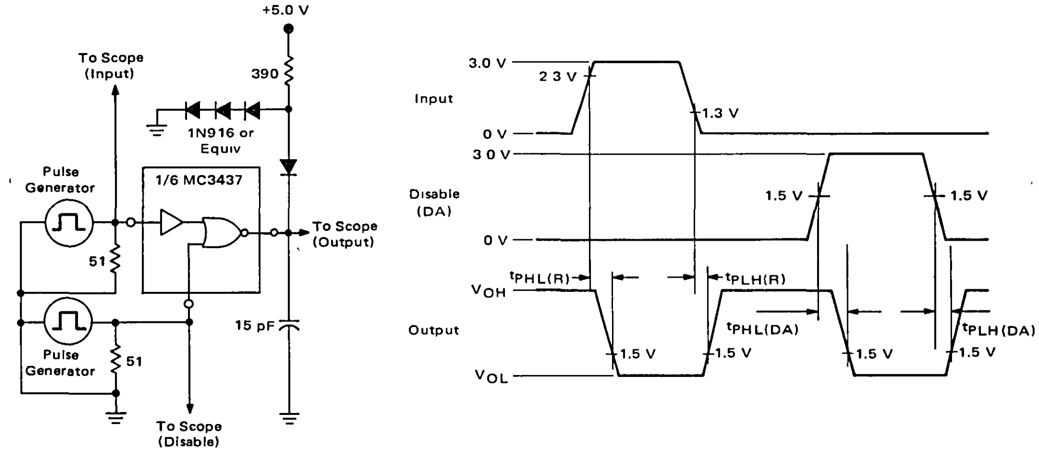
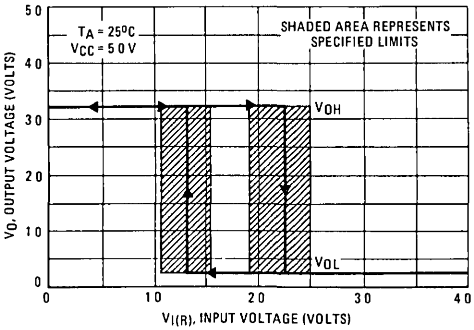
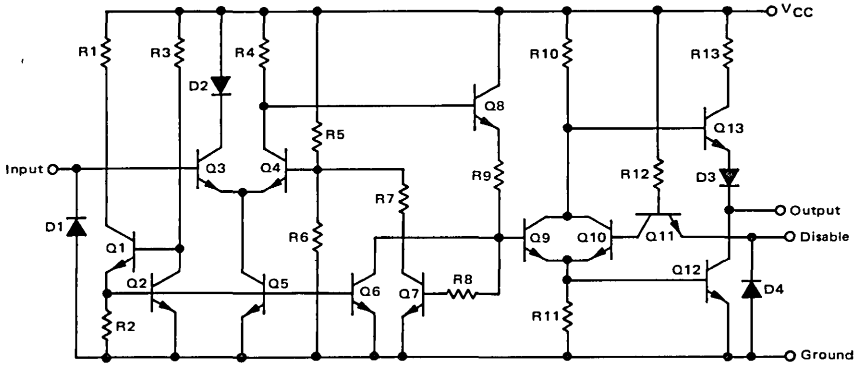


FIGURE 3 – TYPICAL HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)



MOTOROLA

MC3438

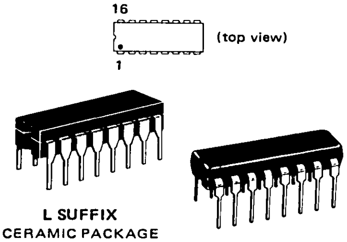
QUAD BUS TRANSCEIVER

Consists of four pair of drivers and receivers with the output of each driver connected to the input of its mating receiver. These devices are intended for use in bus organized data transmission system employing terminated 120 Ω lines. The receivers feature hysteresis to improve noise immunity. A disable function consisting of a two-input NOR gate is provided to control all four drivers.

- Receiver input threshold is not affected by temperature
- Receiver input hysteresis – 1.0 V (Typ)
- Open collector driver outputs allow wire-OR
- MTTL compatible receiver outputs and disable and driver inputs
- Driver propagation delay – 20 ns
- Receiver propagation delay – 20 ns
- Direct replacement for DS8838

QUAD BUS TRANSCEIVER

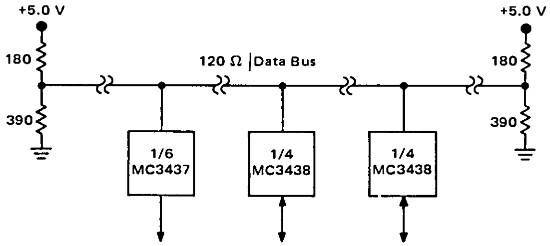
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION

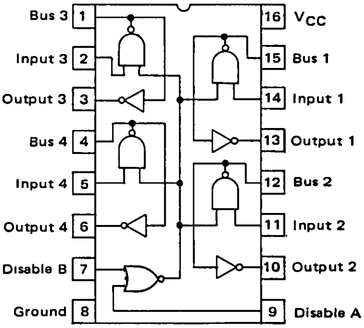


To Computer or Peripherals

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input and Output Voltage	V_O, V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS



TRUTH TABLES

DRIVER SECTION

Disable 1	Disable 2	Input	Bus
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

RECEIVER SECTION

Bus	Output
$V_{IH(R)} > 2.5$ V	L
$V_{IL(R)} < 1.05$ V	H

Where:
L = Low Logic State
H = High Logic State

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leqslant T_A \leqslant 70^{\circ}C$ and $4.75 \leqslant V_{CC} \leqslant 5.25$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Disable Input Voltage – High Logic State ($V_{IH(D)}$ = 2.0 V, $V_{IH(BUS)}$ = 4.0 V, $I_{BUS} < 100\ \mu A$)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage – Low Logic State ($V_{IH(D)}$ = 2.0 V, $V_{IL(BUS)} \leqslant 0.7$ V, I_{BUS} = 50 mA)	$V_{IL(DA)}$	–	–	0.8	V
Driver Input Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, I_{BUS} = 50 mA, $V_{IL(BUS)} \leqslant 0.7$ V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{BUS} < 100\ \mu A$)	$V_{IL(D)}$	–	–	0.8	V
Receiver Input Threshold Voltage – High Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{OL(R)} \leqslant 0.4$ V)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OH(R)}$ = -400 μA, $V_{OH(R)} \geqslant 2.4$ V)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Disable Input Current – High Logic State ($V_{IH(D)}$ = 2.4 V, $V_{IH(DA)}$ = 2.4 V) ($V_{IH(D)}$ = 5.5 V, $V_{IH(DA)}$ = 5.5 V)	$I_{IH(DA)}$	 – –	 – –	 40 1.0	 μA mA
Driver Input Current – High Logic State ($V_{IH(DA)}$ = 2.4 V, $V_{IH(D)}$ = 2.4 V) ($V_{IH(DA)}$ = 5.5 V, $V_{IH(D)}$ = 5.5 V)	$I_{IH(D)}$	 – –	 – –	 40 1.0	 μA mA
Disable Input Current – Low Logic State ($V_{IL(DA)}$ = 0.4 V, $V_{IL(D)}$ = 0.4 V)	$I_{IL(DA)}$	–	–	-1.6	mA
Driver Input Current – Low Logic State ($V_{IL(D)}$ = 0.4 V, $V_{IL(DA)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-1.6	mA
Bus Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8, $V_{IH(BUS)}$ = 4.0 V) (V_{CC} = 5.25 V) (V_{CC} = 0 V)	I_{BUS}	 – –	 20 2.0	 100 100	μA
Bus Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(D)}$ = 2.0 V, I_{BUS} = 50 mA)	$V_{L(BUS)}$	–	0.4	0.7	V
Receiver Output Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	0.25	0.4	V
Receiver Output Short Circuit Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, V_{CC} = 5.25 V)	$I_{OS(R)}$	-18	–	-55	mA
Power Supply Current ($V_{IL(DA)}$ = 0 V, $V_{IH(D)}$ = 2.0 V)	I_{CC}	–	50	70	mA
Input Clamp Diode Voltage ($I_{I(DA)} = I_{I(D)} = I_{BUS}$ = -12 mA)	V_I	–	-1.0	-1.5	V

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Disable Input to High Logic Level Output	$t_{PLH(DA)}$	–	19	27	ns
Propagation Delay Time from Disable Input to Low Logic Level Output	$t_{PHL(DA)}$	–	15	27	ns
Propagation Delay Time from Driver Input to High Logic Level Output	$t_{PLH(D)}$	–	17	25	ns
Propagation Delay Time from Driver Input to Low Logic Level Output	$t_{PHL(D)}$	–	9.0	20	ns
Propagation Delay Time from Bus Input to High Logic Level Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Bus Input to Low Logic Level Output	$t_{PHL(R)}$	–	18	30	ns

FIGURE 2 – DRIVER AND DISABLE TEST CIRCUIT AND WAVEFORMS

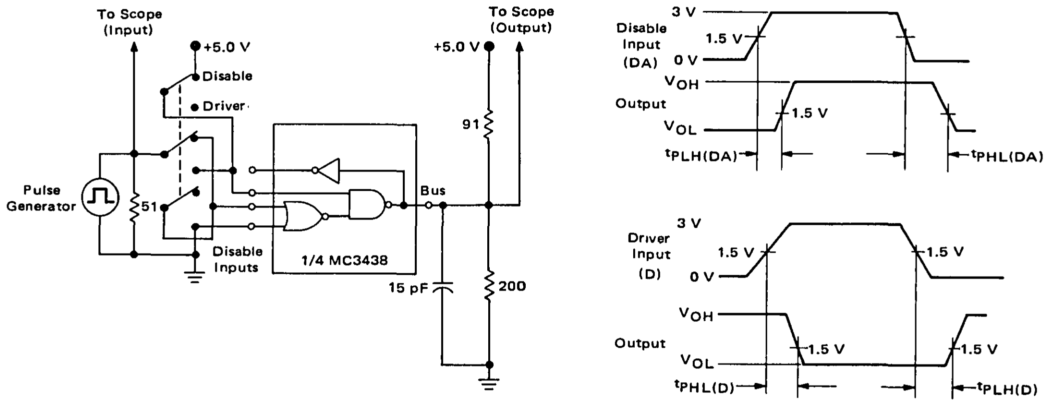


FIGURE 3 – RECEIVER TEST CIRCUIT AND WAVEFORM

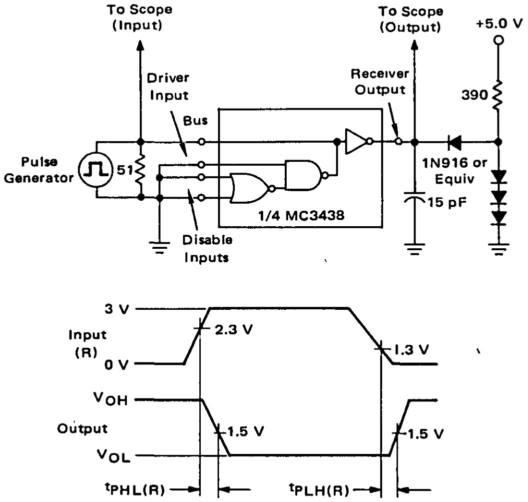
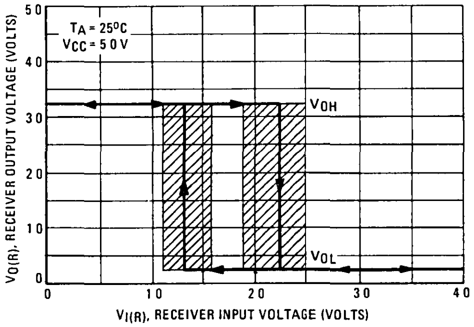
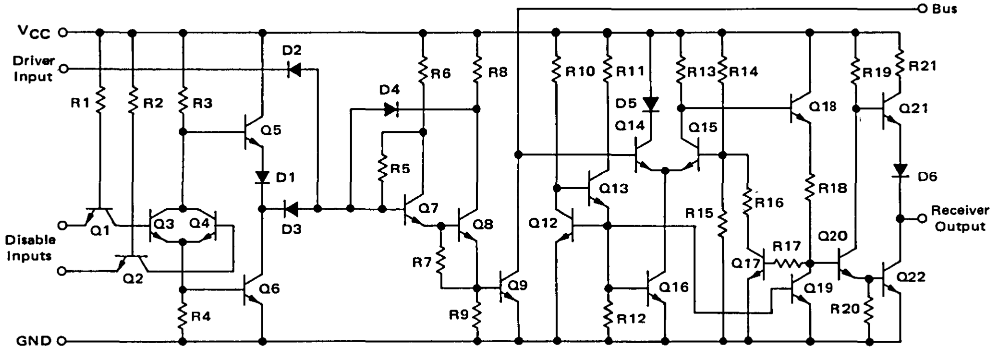


FIGURE 4 – TYPICAL RECEIVER HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 Shown)

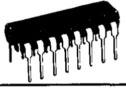


MOTOROLA

MC3440A
MC3441A
MC3443

QUAD INTERFACE BUS TRANSCEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 648

5

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A, MC3443 are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

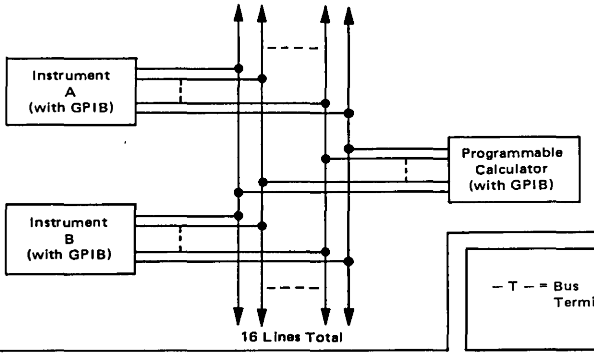
The MC3443 is identical to the MC3441A except that the terminations have been omitted. As such it is pin compatible, and functionally equivalent to the SN75138. It does offer the advantage of receiver input hysteresis.

- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Proposed Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations Provided (except MC3443 version)
- Provides Electrical Compatibility with General-Purpose Interface Bus

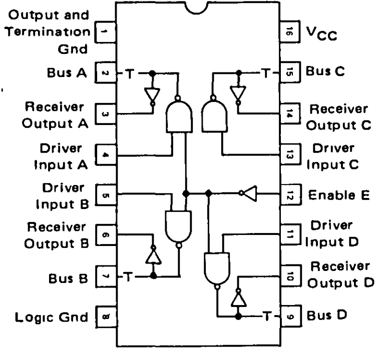
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

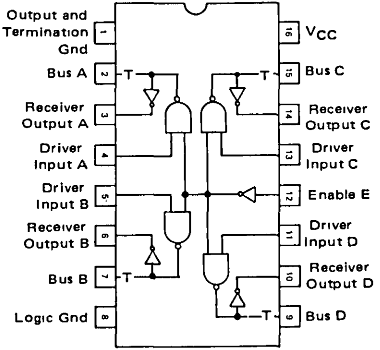
TYPICAL APPLICATION — GPIB MEASUREMENT SYSTEM



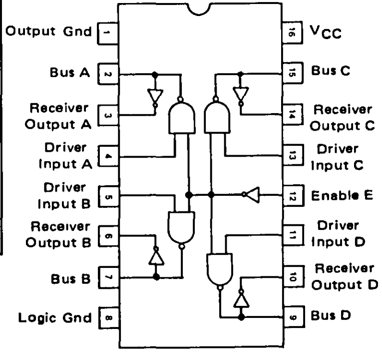
MC3440A



MC3441A



MC3443



— T — = Bus Termination

ELECTRICAL CHARACTERISTICS
(Unless otherwise noted, $4.5\ V \leq V_{CC} \leq 5.5\ V$ and $0 \leq T_A \leq 70^{o}C$, typical values are at $T_A = 25^{o}C$, $V_{CC} = 5\ 0\ V$)

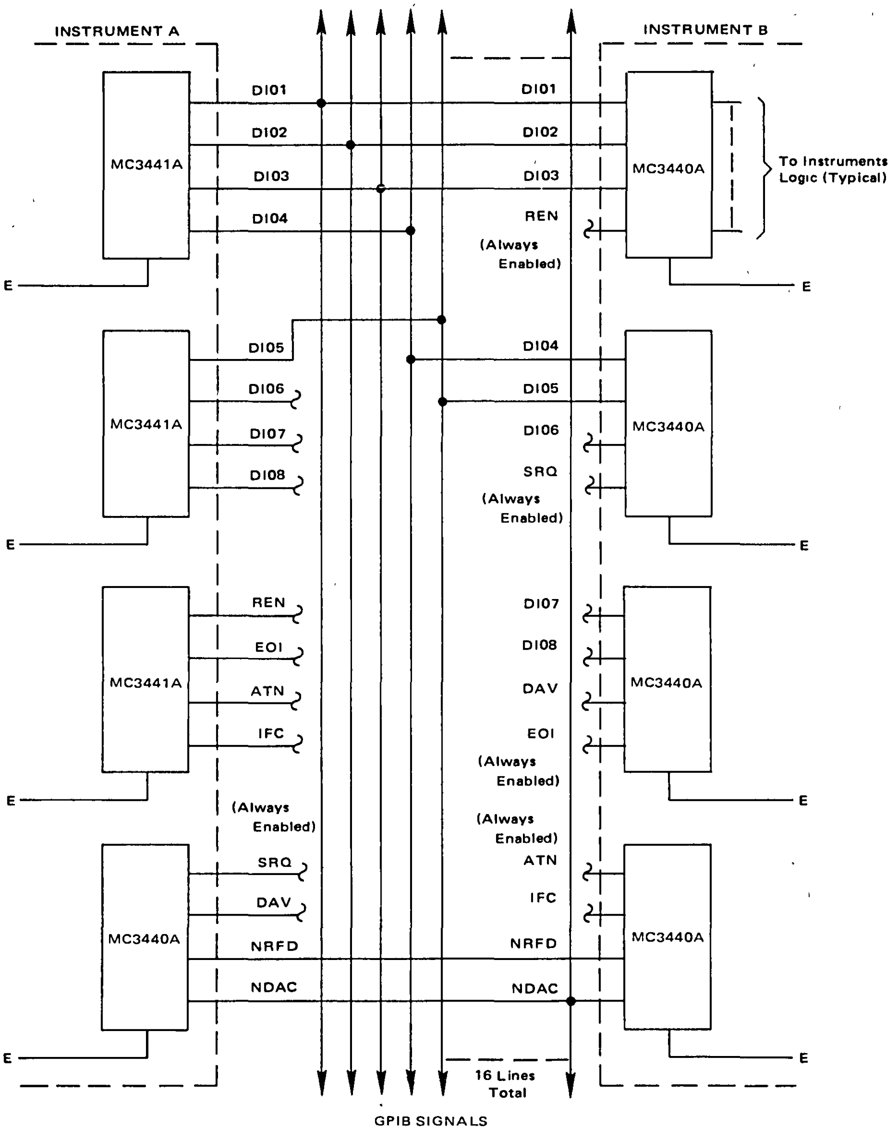
Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2 0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0 8	V
Input Current – High Logic State ($V_{IH} = 2\ 4\ V$)	$I_{IH(D)}$	–	–	40	µA
Input Current – Low Logic State MC3443 ($V_{IL} = 0\ 4\ V$, $V_{CC} = 5\ 0\ V$, $T_A = 25^{o}C$) MC3440A, 3441A	$I_{IL(D)}$	–	–	–1 6 –0.25	mA
Input Clamp Voltage ($I_{IK} = -12\ mA$)	$V_{IK(D)}$	–	–	–1 5	V
Output Voltage – High Logic State (1) (MC3440A, 3441A only) ($V_{IH(S)} = 2\ 4\ V$ or $V_{IL(D)} = 0\ 8\ V$)	$V_{OH(D)}$	2.5	–	–	V
Output Voltage – Low Logic State ($V_{IH(S)} = 2\ 0\ V$, $V_{IL(E)} = 0\ 8\ V$, $I_{OL(D)} = 48\ mA$) MC3443 MC3440A, 3441A ($V_{IH(D)} = 2\ 0\ V$, $V_{IL(E)} = 0\ 8\ V$, $I_{OL(D)} = 100\ mA$)	$V_{OL(D)}$	– – –	– – –	0.4 0.5 0 80	V
Output Leakage Current – MC3443 Only ($V_{IH(E)} = 2\ 0\ V$ or $V_{IL(D)} = 0\ 8\ V$)	$I_{OH(D)}$	–	–	250	µA
RECEIVER PORTION					
Input Hysteresis	–	400	580	–	mV
Input Threshold Voltage – Low to High Output Logic State ($V_{CC} = 5.0\ V$, $T_A = 25^{o}C$)	$V_{ILH(R)}$	0 8	0.98	–	V
Input Threshold Voltage – High to Low Output Logic State ($V_{CC} = 5.0\ V$, $T_A = 25^{o}C$)	$V_{IHL(R)}$	–	1.56	2.0	V
Output Voltage – High Logic State ($V_{IL(R)} = 0\ 8\ V$, $I_{OH(R)} = -400\ \mu A$)	$V_{OH(R)}$	2 4	–	–	V
Output Voltage – Low Logic State MC3440A, 3441A ($V_{IH(R)} = 2\ 0\ V$, $I_{OL(R)} = 16\ mA$) MC3443	$V_{OL(R)}$	– –	– –	0.5 0.4	V
Output Short-Circuit Current ($V_{IL(R)} = 0\ 8\ V$) (Only one output may be shorted at a time)	$I_{OS(R)}$	-20	–	-55	mA
BUS TERMINATION PORTION (Does not apply to MC3443)					
Bus Voltage ($V_{IL(D)} = 0\ 8\ V$) ($I_{BUS} = -12\ mA$) (No Load)	V_{BUS}	 – 2.50	 – –	 –1.5 3.70	V
Bus Current ($V_{IL(D)} = 0\ 8\ V$, $V_{BUS} \geq 5\ 0\ V$) ($V_{IL(D)} = 0.8\ V$, $V_{BUS} \leq 5.5\ V$) ($V_{IL(D)} = 0.8\ V$, $V_{BUS} = 0\ 5\ V$) ($V_{CC} = 0, 0 \leq V_{BUS} \leq 2.75\ V$) (MC3440A, 3441A only)	I_{BUS}	 0 7 – –1.3 –	 – – – –	 – 2.5 –3 2 +0.04	mA
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current ($V_{IH(D)} = 2\ 4\ V$, $V_{IL(E)} = 0\ V$)	I_{CC}	30	56	75	mA

SWITCHING CHARACTERISTICS
($V_{CC} = 5\ 0\ V$, $T_A = 25^{o}C$)

Characteristic	Symbol	MC3441A,3441A			MC3443			Unit
		Min	Typ	Max	Min	Typ	Max	
DRIVER PORTION								
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	13	30	–	13	25	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	17	30	–	17	25	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	25	40	–	25	32	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	25	40	–	25	32	ns
RECEIVER PORTION								
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	15	30	–	15	22	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	15	30	–	15	22	ns

(1) 12 k resistor from the bus terminal to V_{CC} required on the MC3443 version.

GENERAL PURPOSE INTERFACE BUS APPLICATION



8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:
- REN – Remote Enable
- SRQ – Service Request
- EOI – End or Identify
- ATN – Attention
- IFC – Interface Clear

3 Data Byte Transfer Control Bus
- DAV – Data Valid
- NRFD – Not Ready for Data
- NDAC – Not Data Accepted

16 Total Signal Lines

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

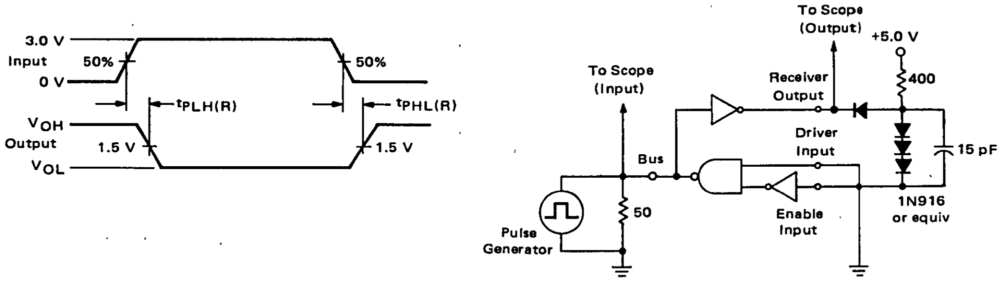
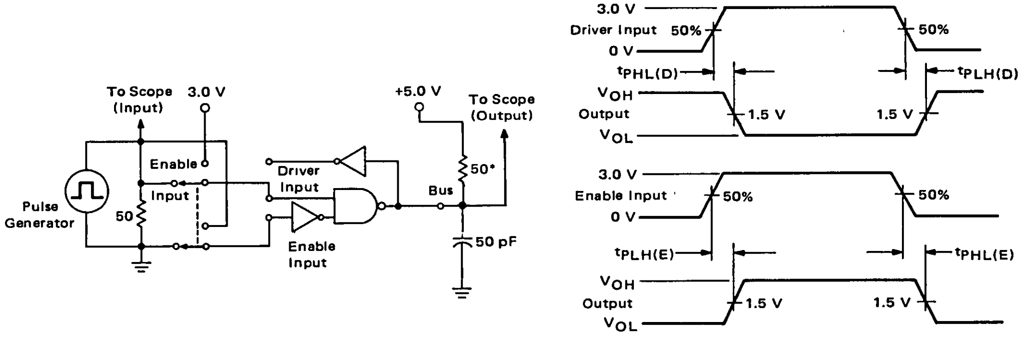
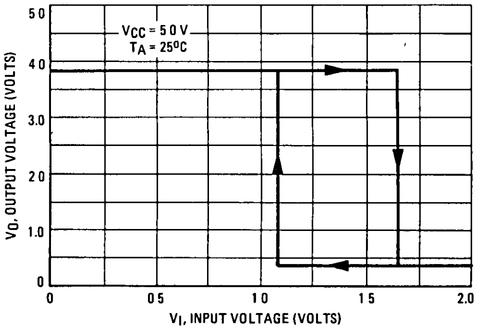


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)



*MC3443 only.
MC3440A/3441A uses 100 Ω

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



MOTOROLA

MC3446A

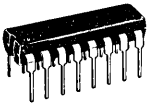
QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVER

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided

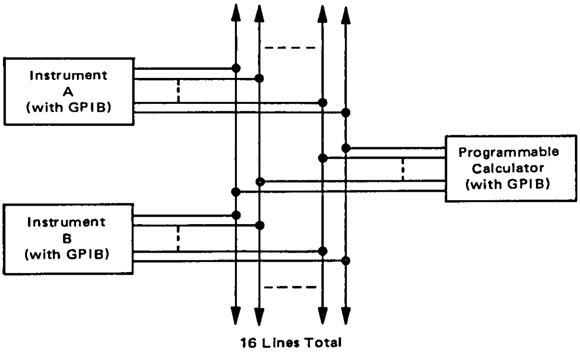
QUAD INTERFACE BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

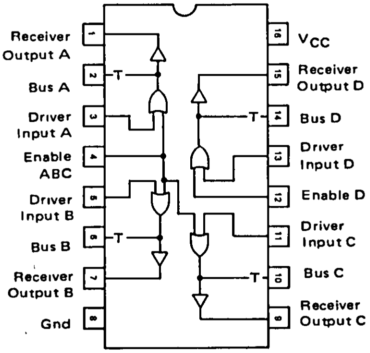


P SUFFIX
PLASTIC PACKAGE
CASE 648

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



— T — = Bus Termination

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, 4.5 V $\leq V_{CC} \leq$ 5.5 V and 0 $\leq T_A \leq$ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	–	5.0	40	µA
Input Current – Low Logic State (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C)	$I_{IL(D)}$	–	-0.2	-0.25	mA
Input Clamp Voltage (I_{IK} = -12 mA)	$V_{IK(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	3.3	3.7	V
Output Voltage – Low Logic State ($V_{IL(S)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	
Input Breakdown Current ($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	1.0	mA
RECEIVER PORTION					
Input Hysteresis	–	400	625	–	mV
Input Threshold Voltage – Low to High Output Logic State	$V_{ILH(R)}$	–	1.66	2.0	V
Input Threshold Voltage – High to Low Output Logic State	$V_{IHL(R)}$	0.8	1.03	–	V
Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OH(R)}$ = -400 µA)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OL(R)}$ = 8.0 mA)	$V_{OL(R)}$	–	–	0.5	V
Output Short-Circuit Current ($V_{IH(R)}$ = 2.0 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	4.0	–	14	mA
BUS LOAD CHARACTERISTICS					
Bus Voltage ($V_{IH(E)}$ = 2.4 V) (I_{BUS} = -12 mA)	$V_{(BUS)}$	2.5 –	3.3 –	3.7 -1.5	V
Bus Current ($V_{IH(D)}$= 2.4 V, $V_{BUS} \geq$ 5.0 V) ($V_{IH(D)}$ = 2.4 V, V_{BUS} = 0.5 V) ($V_{BUS} \leq$ 5.5 V) (V_{CC} = 0, 0 V $\leq V_{BUS} \leq$ 2.75 V)	$I_{(BUS)}$	0.7 -1.3 – –	– – – –	– -3.2 2.5 0.04	mA
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current (All Drivers OFF) (All Drivers ON)	I_{CC}	 – –	 12 32	 19 40	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	–	50	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	–	40	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	–	50	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	–	50	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	–	50	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	–	40	ns

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

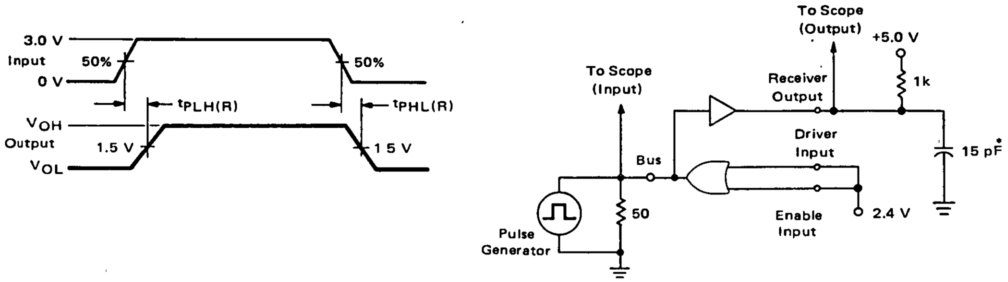
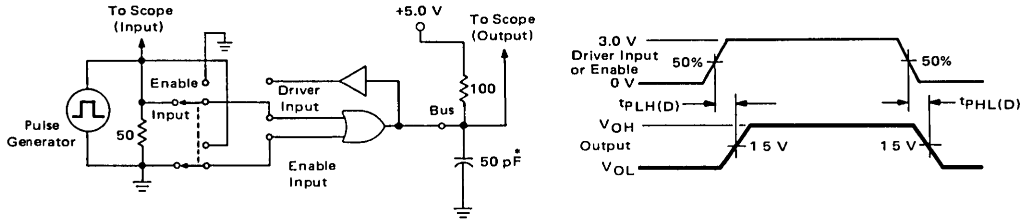


FIGURE 2 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)



* Includes Probe and Jig Capacitance

FIGURE 3 — TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

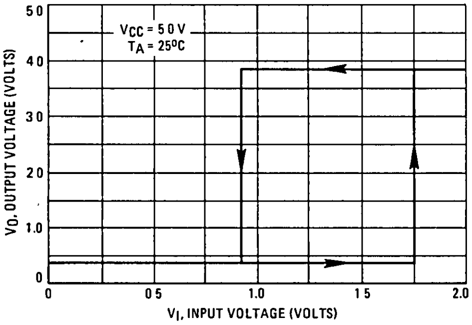
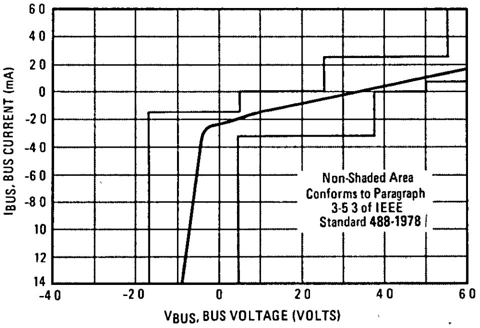


FIGURE 4 — TYPICAL BUS LOAD LINE



MOTOROLA

MC3447

OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

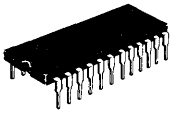
BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

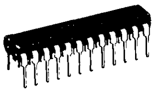
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power — Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided



L SUFFIX
CERAMIC PACKAGE
CASE 623

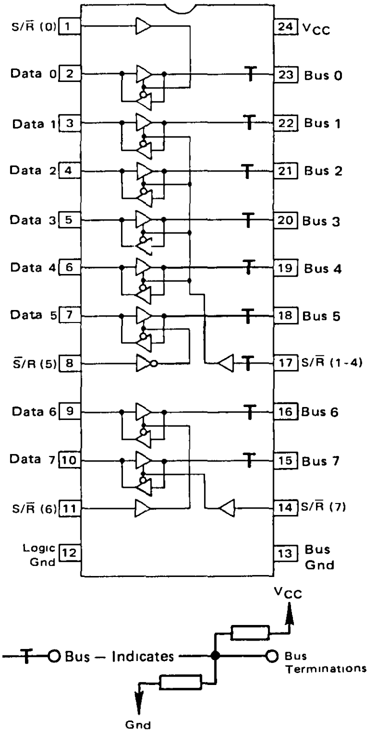


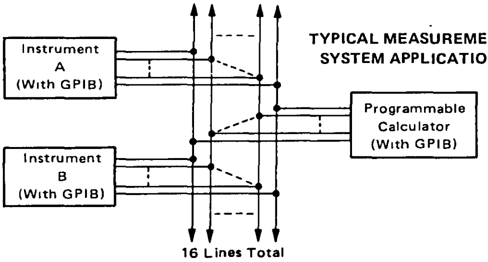
P 3 SUFFIX
PLASTIC PACKAGE
CASE 724

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENTS





TYPICAL MEASUREMENT SYSTEM APPLICATION

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V $\leq V_{CC} \leq$ 5.50 V and 0 $\leq T_A \leq$ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic – Note 2	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/\overline{R})}$ = 0.8 V)	$V_{(Bus)}$	2.5	–	3.7	
($I_{(Bus)}$ = −12 mA)	$V_{IC(Bus)}$	–	–	−1.5	
Bus Current	$I_{(Bus)}$				mA
(5.0 V $\leq V_{(Bus)} \leq$ 5.5 V)		0.7	–	2.5	
($V_{(Bus)}$ = 0.5 V)		−1.3	–	−3.2	
(V_{CC} = 0 V, 0 V $\leq V_{(Bus)} \leq$ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/\overline{R})}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold					V
($V_{I(S/\overline{R})}$ = 0.8 V) Low to High	$V_{ILH(R)}$	–	1.6	2.0	
High to Low	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage – High Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = −200 µA, $V_{(Bus)}$ = 2.0 V)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, ($V_{(Bus)}$ = 0.8 V	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)	$I_{OS(R)}$	−4.0	–	−20	mA
Driver Input Voltage – High Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current – Data Pins ($V_{I(S/\overline{R})}$ = 2.0 V)					µA
(0.5 $\leq V_{I(D)} \leq$ 2.7 V)	$I_{I(D)}$	−100	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current – Send/Receive					µA
(0.5 $\leq V_{I(S/R)} \leq$ 2.7 V)	$I_{I(S/\overline{R})}$	−250	–	20	
($V_{I(S/\overline{R})}$ = 5.5 V)	$I_{IB(S/\overline{R})}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)	$V_{IC(D)}$	–	–	−1.5	V
Driver Output Voltage – High Logic State ($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage – Low Logic State (Note 1) ($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Power Supply Current					mA
(Listening Mode – All Receivers On)	I_{CCL}	–	30	45	
(Talking Mode – All Drivers On)	I_{CCH}	–	75	95	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	7.0	15	
(Output High to Low)	$t_{PHL(D)}$	–	16	30	
Propagation Delay of Receiver (Channels 0 to 5, 7)					ns
(Output Low to High)	$t_{PLH(R)}$	–	28	50	
(Output High to Low)	$t_{PHL(R)}$	–	15	30	
Propagation Delay of Receiver (Channel 6, Note 3)					ns
(Output Low to High)	$t_{PLH(R)}$	–	17	30	
(Output High to Low)	$t_{PHL(R)}$	–	12	22	

NOTES

1. The IEEE 488-1978 Bus Standard Changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
2. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(\overline{S}/R)}$ uses the opposite logic levels.
3. In order to meet the IEEE 488-1978 standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (pins 9 and 16).

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5 0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	15	30	
Third State to Logic High	$t_{PZH(R)}$	–	15	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	15	25	
Third State to Logic Low	$t_{PZL(R)}$	–	10	25	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ(D)}$	–	13	25	
Third State to Logic Low	$t_{PZL(D)}$	–	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

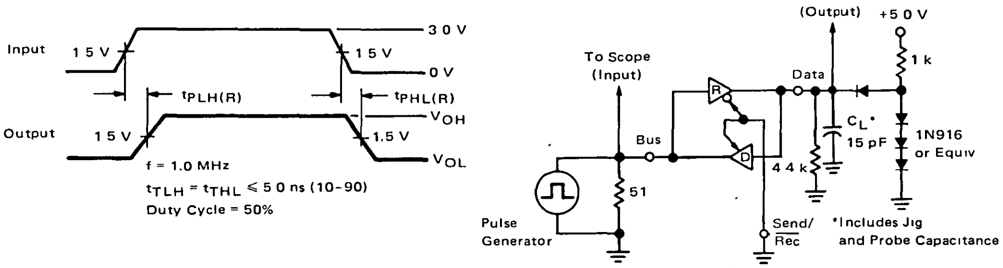


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

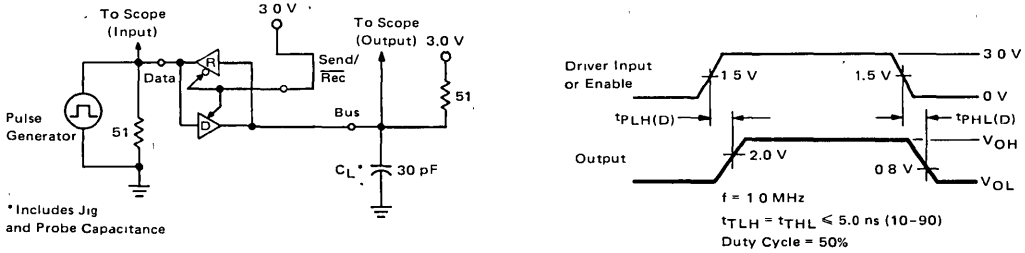


FIGURE 3 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO BUS OUTPUT (DRIVER)

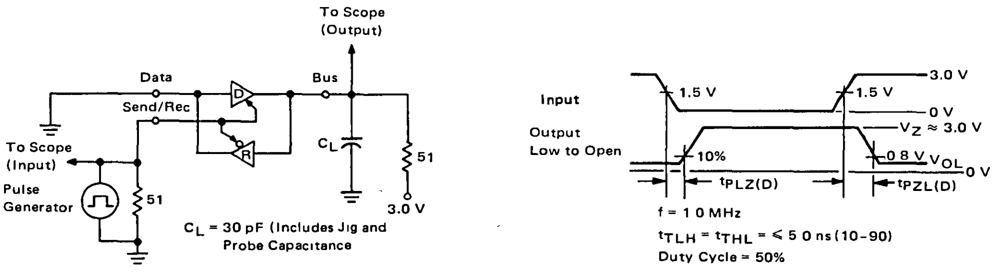


FIGURE 4 — SEND/$\overline{\text{RECEIVE}}$ INPUT TO DATA OUTPUT (RECEIVER)

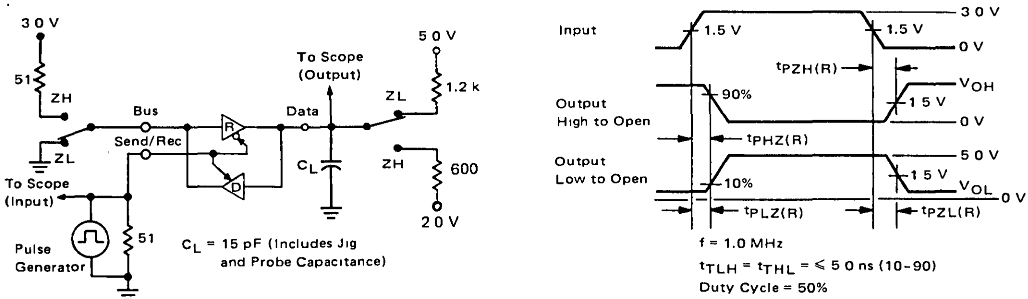


FIGURE 5 — TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

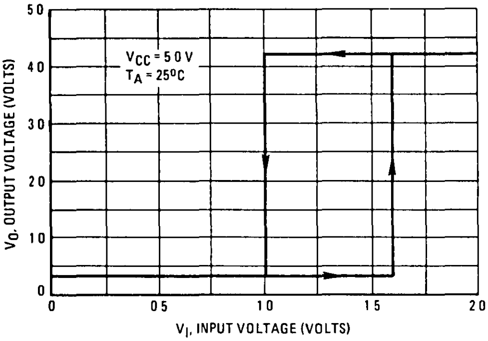


FIGURE 6 — TYPICAL BUS LOAD LINE

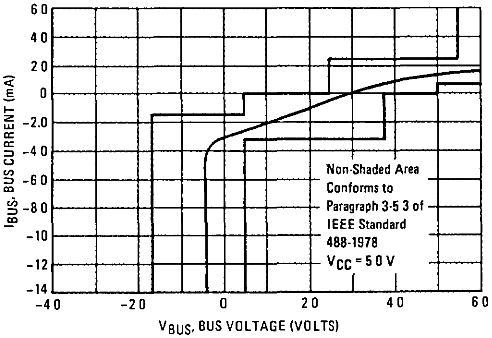


FIGURE 7 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

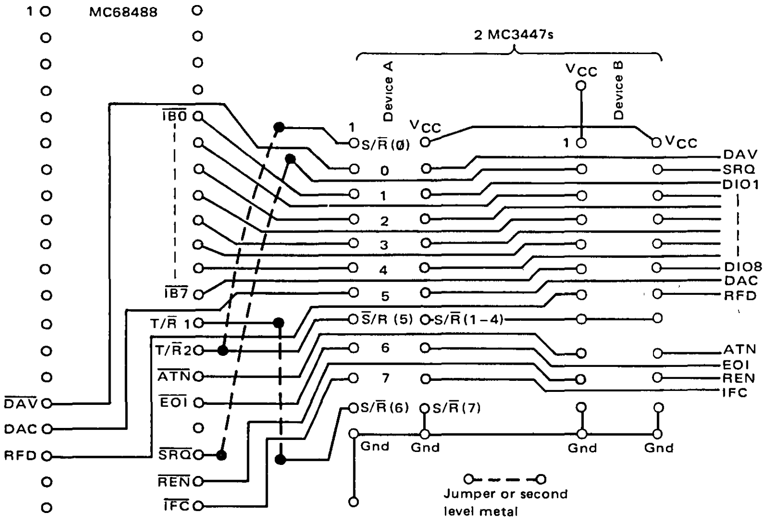
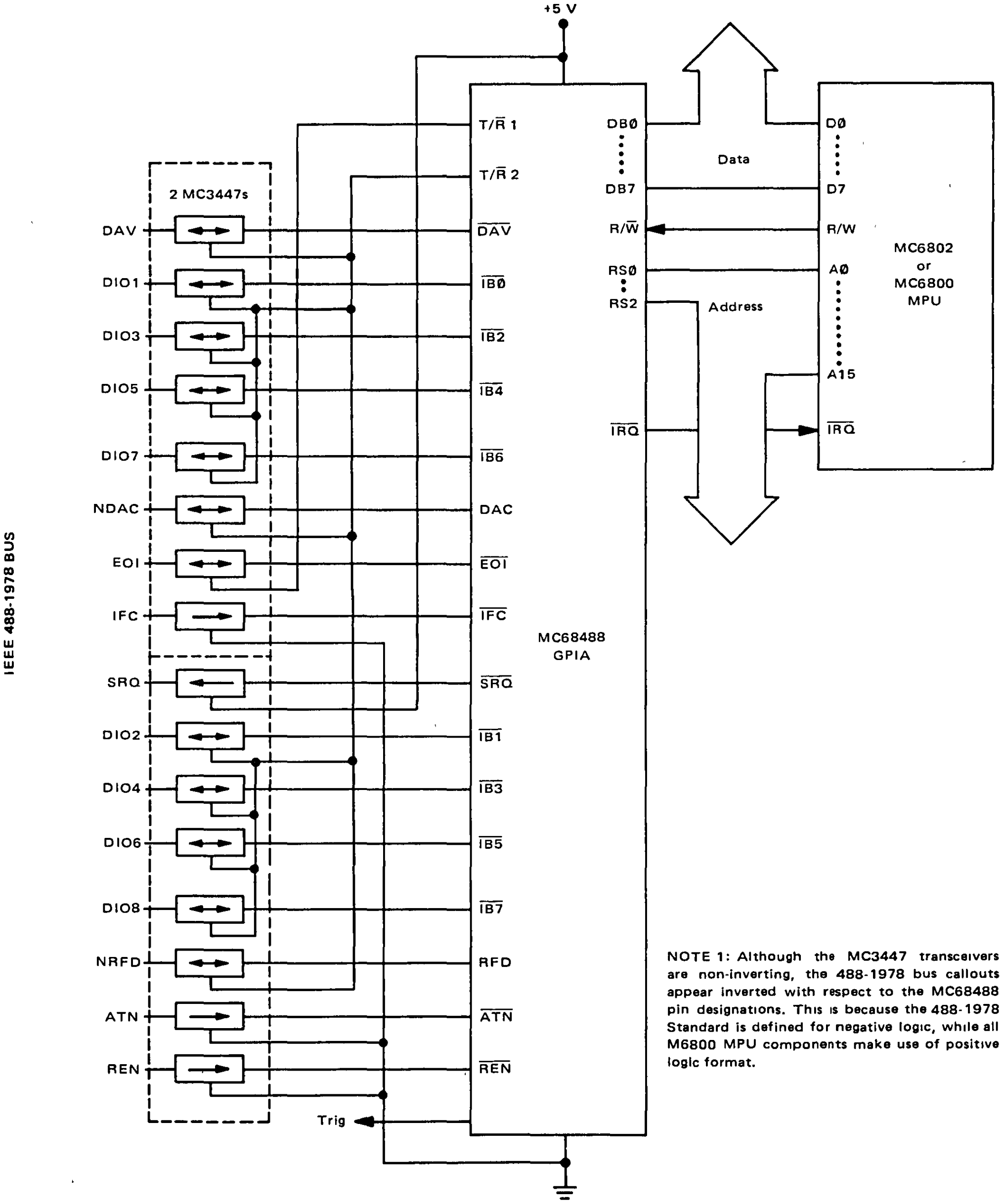


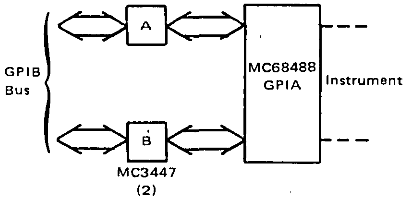
FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3447 transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations					MC68488 Connections	
A	B						A	B
T/$\overline{R}$ 2	V_{CC}	S/$\overline{R}$ (0)	1		24	V_{CC}	V_{CC}	V_{CC}
$\overline{DAV}$	$\overline{SRQ}$	Data 0 0	2		23	Bus 0	DAV	SRQ
$\overline{IB0}$	$\overline{IB1}$	Data 1	3		22	Bus 1	DIO 1	DIO 2
$\overline{IB2}$	$\overline{IB3}$	Data 2	4		21	Bus 2	DIO 3	DIO 4
$\overline{IB4}$	$\overline{IB5}$	Data 3	5		20	Bus 3	DIO 5	DIO 6
$\overline{IB6}$	$\overline{IB7}$	Data 4	6	Octal GPIB Transceiver	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7		18	Bus 5	NDAC	NRFD
T/$\overline{R}$ 2	T/$\overline{R}$ 2	$\overline{S}$/R (5)	8		17	S/$\overline{R}$ (1–4)	T/$\overline{R}$ 2	T/$\overline{R}$ 2
$\overline{EOI}$	$\overline{ATN}$	Data 6	9		16	Bus 6	EOI	ATN
$\overline{IFC}$	$\overline{REN}$	Data 7	10		15	Bus 7	IFC	REN
T/$\overline{R}$ 1	Gnd	S/$\overline{R}$ (6)	11		14	S/$\overline{R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12		13	Bus Gnd	Gnd	Gnd



MOTOROLA

MC3448A

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

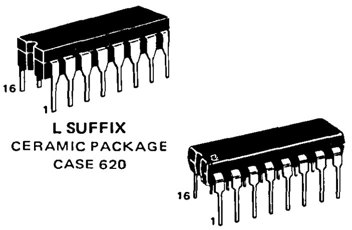
Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector(1) or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option(1)
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

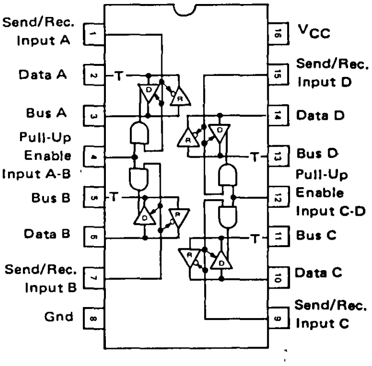
QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT



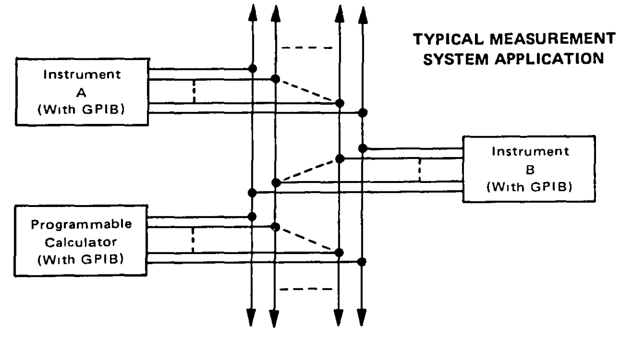
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



TYPICAL MEASUREMENT SYSTEM APPLICATION

TRUTH TABLE

Send/Rec	Enable	Info Flow	Comments
0	X	Bus → Data	–
1	1	Data → Bus	Active Pull Up
1	0	Data → Bus	Open Col

X = Don't Care

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V < V_{CC} < 5.25 V and 0 < T_A < 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open)($V_{I(S/R)}$ = 0.8 V) ($I_{(BUS)}$ = -12 mA)	 $V_{(BUS)}$ $V_{IC(BUS)}$	 2.75 –	 – –	 3.7 -1.5	V
Bus Current (5.0 V < $V_{(BUS)}$ ≤ 5.5 V) ($V_{(BUS)}$ = 0.5 V) (V_{CC} = 0 V, 0 V < $V_{(BUS)}$ ≤ 2.75 V)	$I_{(BUS)}$	 0.7 -1.3 –	 – – –	 2.5 -3.2 +0.04	mA
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold ($V_{I(S/R)}$ = 0.8 V, Low to High) ($V_{I(S/R)}$ = 0.8 V, High to Low)	 $V_{ILH(R)}$ $V_{IHL(R)}$	 – 0.8	 1.6 1.0	 1.8 –	V
Receiver Output Voltage – High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = -800 µA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	-15	–	-75	mA
Driver Input Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current – Data Pins ($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V) (0.5 ≤ $V_{I(D)}$ ≤ 2.7 V) ($V_{I(D)}$ = 5.5 V)	 $I_{I(D)}$ $I_{IB(D)}$	 -200 –	 – –	 40 200	µA
Input Current – Send/Receive (0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V) ($V_{I(S/R)}$ = 5.5 V)	 $I_{I(S/R)}$ $I_{IB(S/R)}$	 -100 –	 – –	 20 100	µA
Input Current – Enable (0.5 ≤ $V_{I(E)}$ ≤ 2.7 V) ($V_{I(E)}$ = 5.5 V)	 $I_{I(E)}$ $I_{IB(E)}$	 -200 –	 – –	 20 100	µA
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = -18 mA)	$V_{IC(D)}$	–	–	-1.5	V
Driver Output Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = -5.2 mA)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage – Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	-30	–	-120	mA
Power Supply Current (Listening Mode – All Receivers On) (Talking Mode – All Drivers On)	 I_{CCL} I_{CCH}	 – –	 63 106	 85 125	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	 $t_{PLH(D)}$ $t_{PHL(D)}$	 – –	 – –	 15 17	ns
Propagation Delay of Receiver (Output Low to High) (Output High to Low)	 $t_{PLH(R)}$ $t_{PHL(R)}$	 – –	 – –	 25 23	ns

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	–	30	
Third State to Logic High	$t_{PZH(R)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	–	30	
Third State to Logic Low	$t_{PZL(R)}$	–	–	30	
Propagation Delay Time — Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	–	30	
Third State to Logic High	$t_{PZH(D)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(D)}$	–	–	30	
Third State to Logic Low	$t_{PZL(D)}$	–	–	30	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	–	–	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	–	–	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

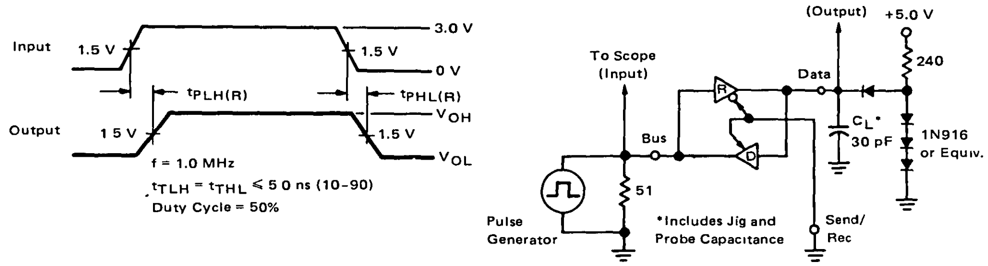


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

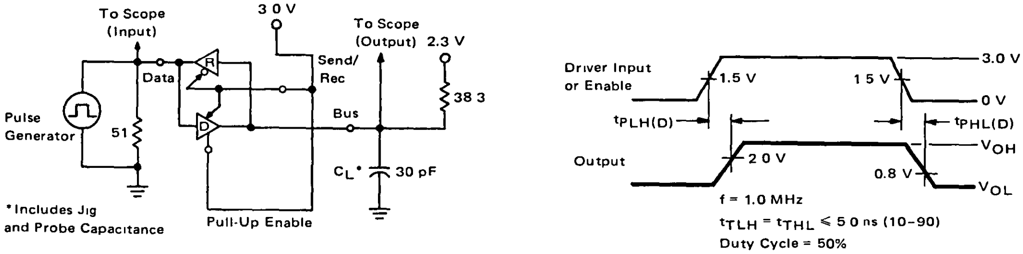


FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

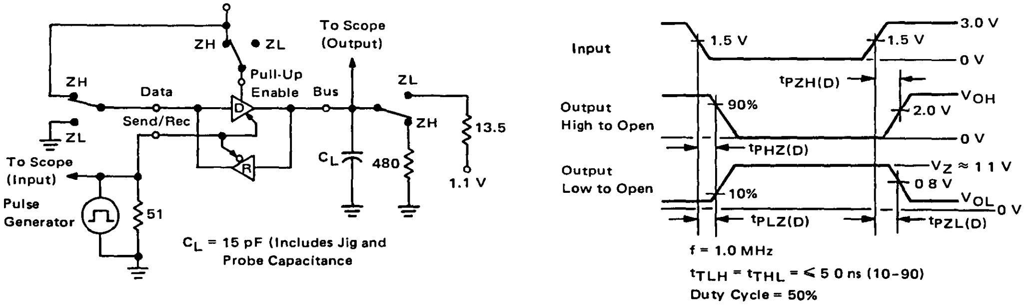
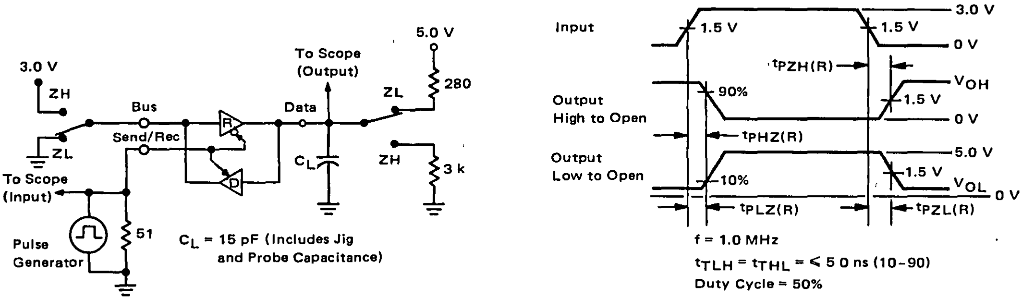


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

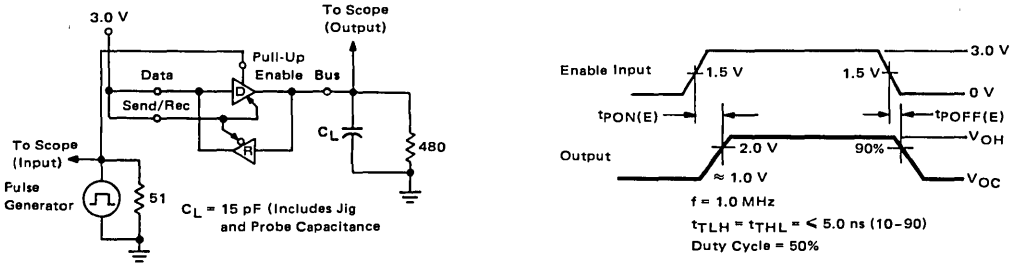


f = 1.0 MHz

$t_{TLH} = t_{THL} = \leq 5\ 0$ ns (10–90)

Duty Cycle = 50%

FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)



f = 1.0 MHz

$t_{TLH} = t_{THL} = \leq 5.0$ ns (10–90)

Duty Cycle = 50%

FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

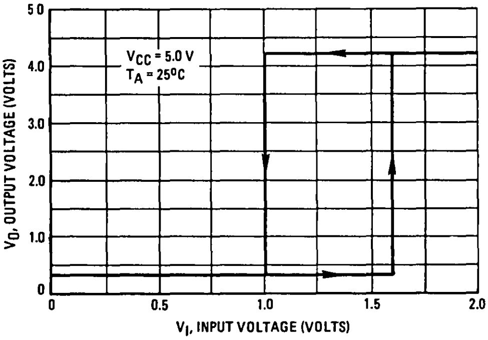


FIGURE 7 – TYPICAL BUS LOAD LINE

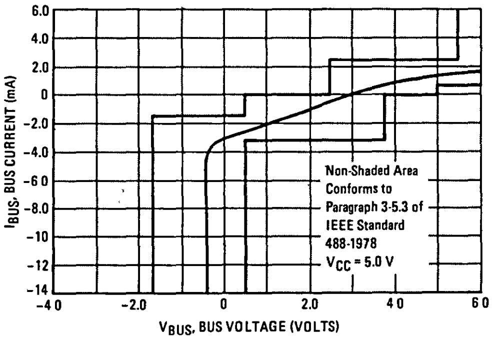
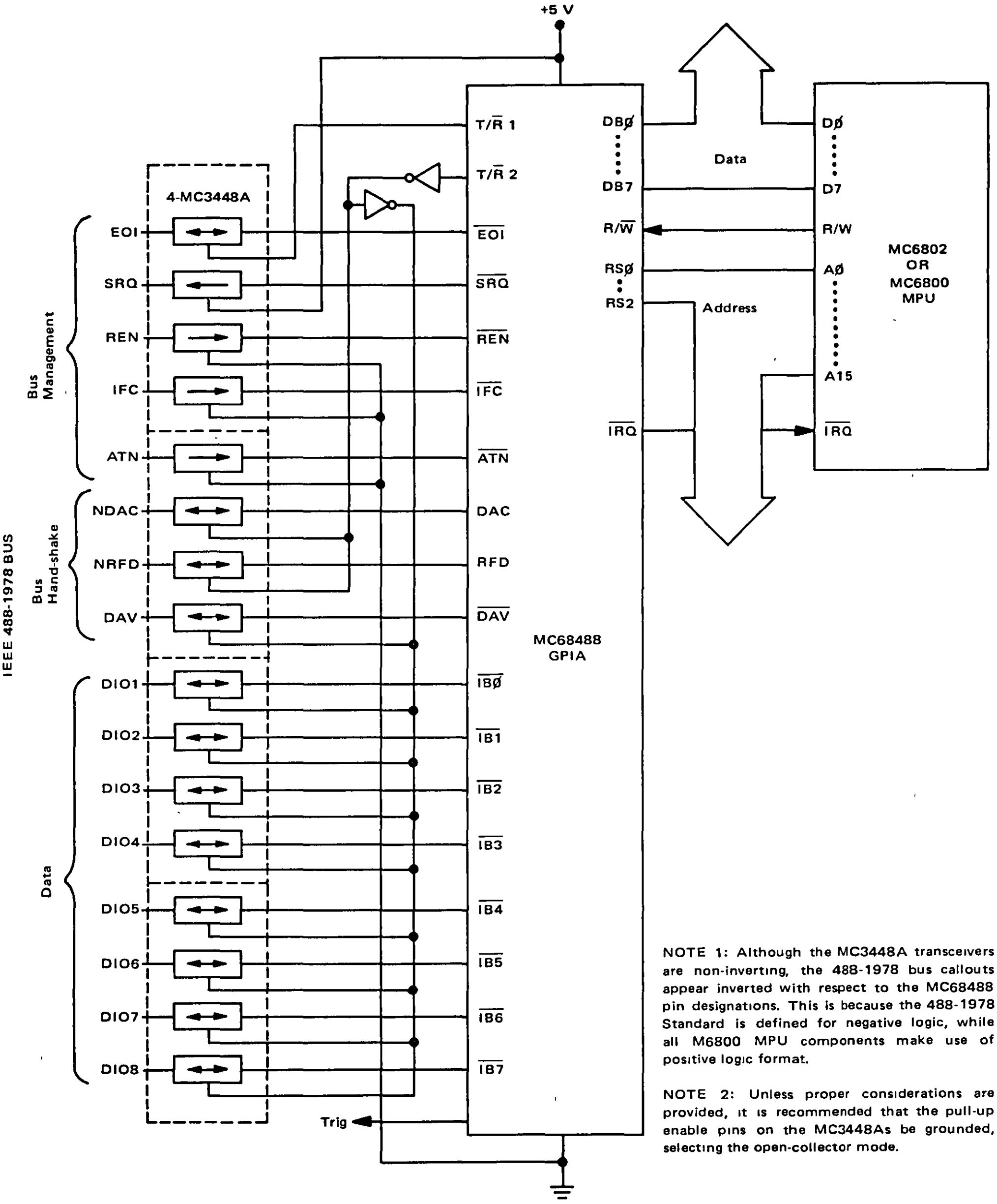


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

MOTOROLA

MC3450
MC3452

Specifications and Applications Information

QUAD MTTL COMPATIBLE LINE RECEIVERS

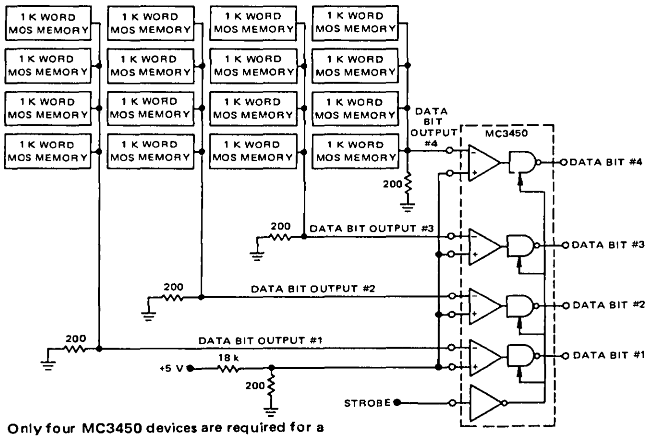
The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

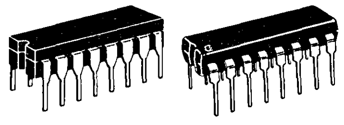
FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

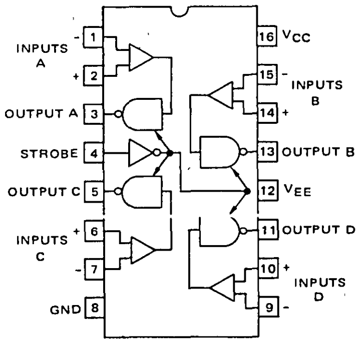
SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM



TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geqslant$ +25 mV	L	H	Off
	H	Z	Off
-25 mV $\leqslant$ $V_{ID} \leqslant$ +25 mV	L	I	I
	H	Z	Off
$V_{ID} \leqslant$ -25 mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5 0 -5.0	+5.25 -5 25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5 0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3 0	Vdc

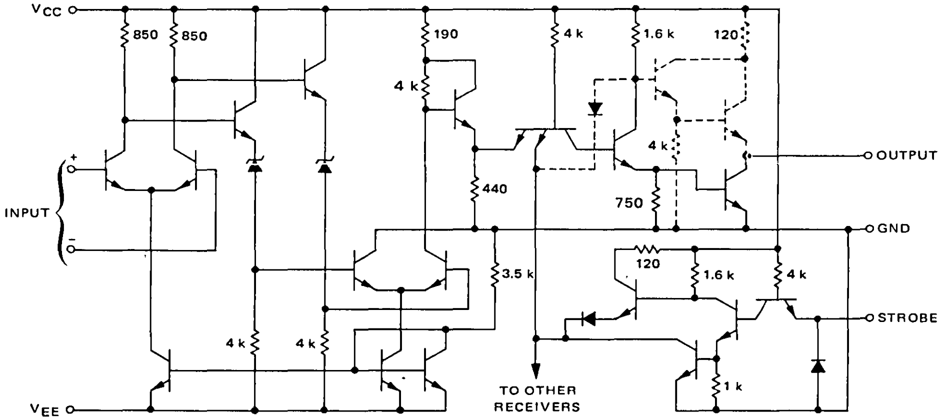
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	µA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	µA
High Level Input Current to Strobe Input	$I_{IH(S)}$	5							
$V_{IH(S)}$ = +2.4 V			–	–	40	–	–	40	µA
$V_{IH(S)}$ = +5.25 V			–	–	1.0	–	–	1.0	mA
Low Level Input Current to Strobe Input $V_{IH(S)}$ = +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	µA
Low Level Output Voltage	V_{OL}	3	–	–	0.4	–	–	0.4	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	µA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

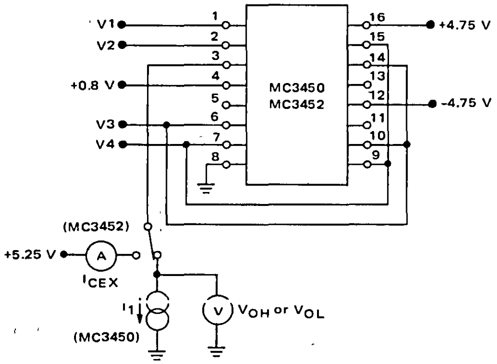
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2 975 V	–	+3 0 V	–	+3 0 V	–	GND	–	+0 4 mA
	-3 0 V	–	-2 975 V	–	GND	–	-3 0 V	–	
I_{CEX}	–	+2 975 V	–	+3 0 V	–	+3 0 V	–	GND	–
	–	-3 0 V	–	-2 975 V	–	GND	–	-3 0 V	–
V_{OL}	+3 0 V	+3 0 V	+2 975 V	+2 975 V	GND	GND	+3 0 V	+3 0 V	-16 mA
	-2 975 V	-2 975 V	-3 0 V	-3 0 V	-3 0 V	-3 0 V	GND	GND	

Channel A shown under test Other channels are tested similarly

FIGURE 4 – I_{CCH} AND I_{EEH}

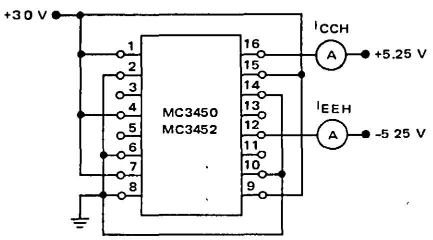
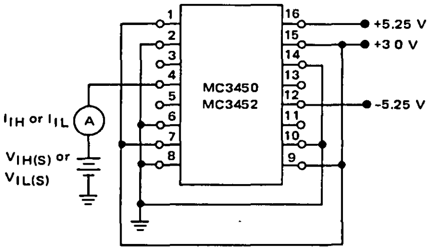
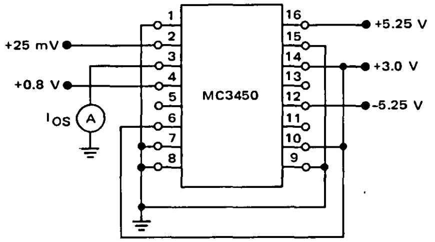


FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$



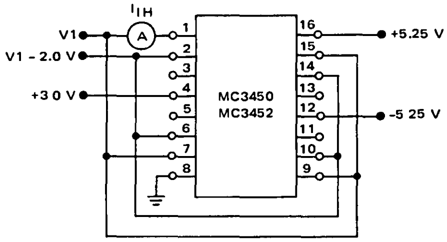
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



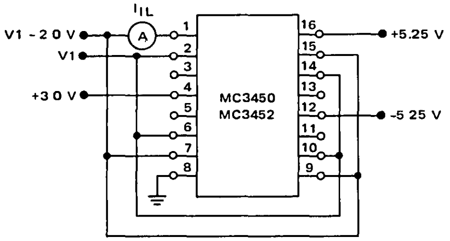
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time

FIGURE 7 – I_{IH}



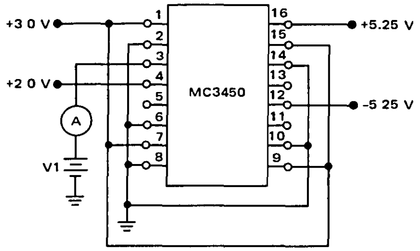
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

FIGURE 8 – I_{IL}



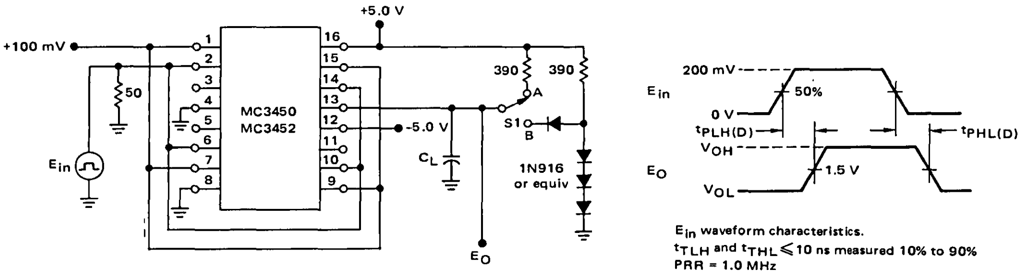
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3 0 V to -3 0 V.

FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0 4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



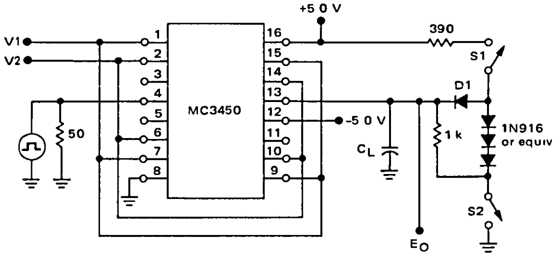
E_{in} waveform characteristics.
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$ $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance
E_{in} waveform characteristics
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 50%

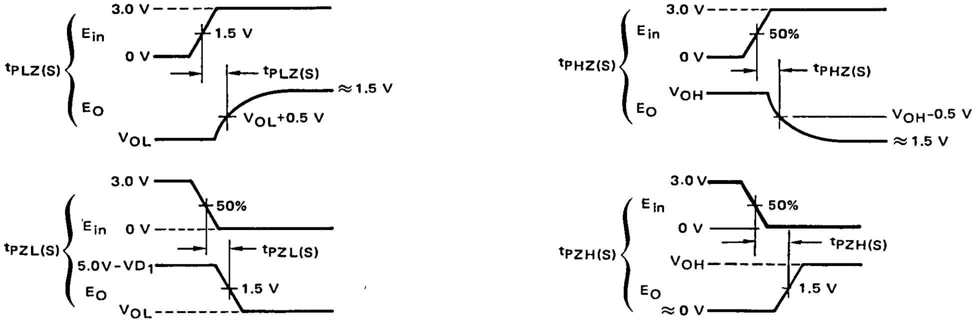
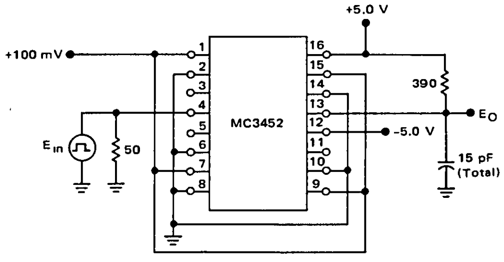
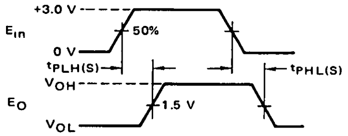


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



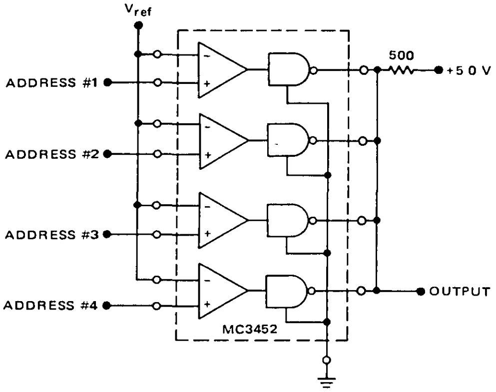


E_{in} waveform characteristics
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

Output of Channel B shown under test, other channels are tested similarly.

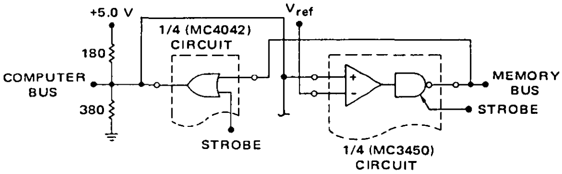
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



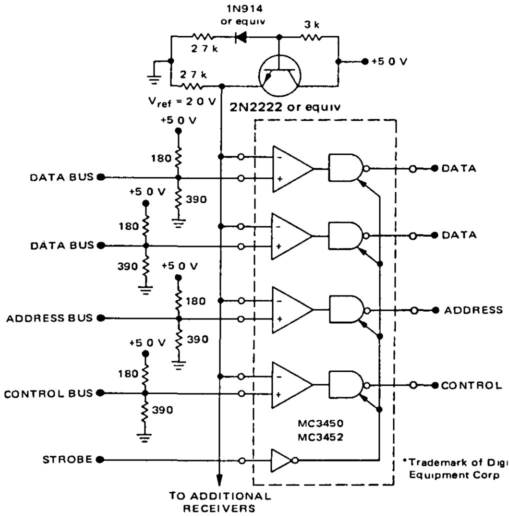
The MC3452 can be used for address decoding as illustrated above All outputs of the MC3452 are tied together through a common resistor to +5 0 volts In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

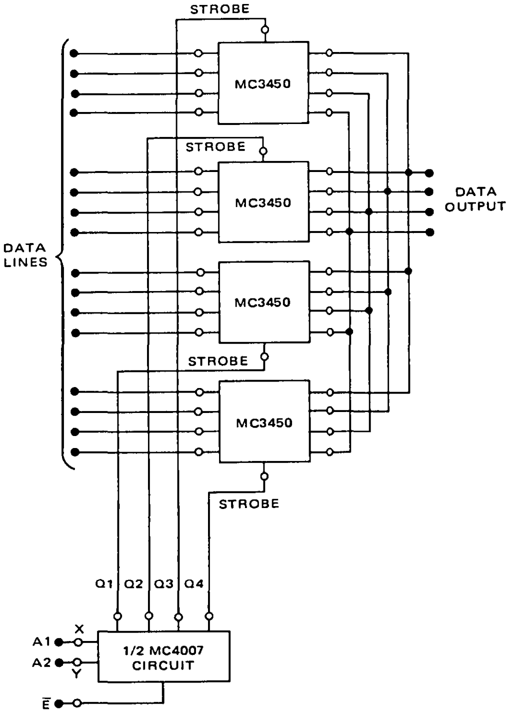
FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



*Trademark of Digital Equipment Corp

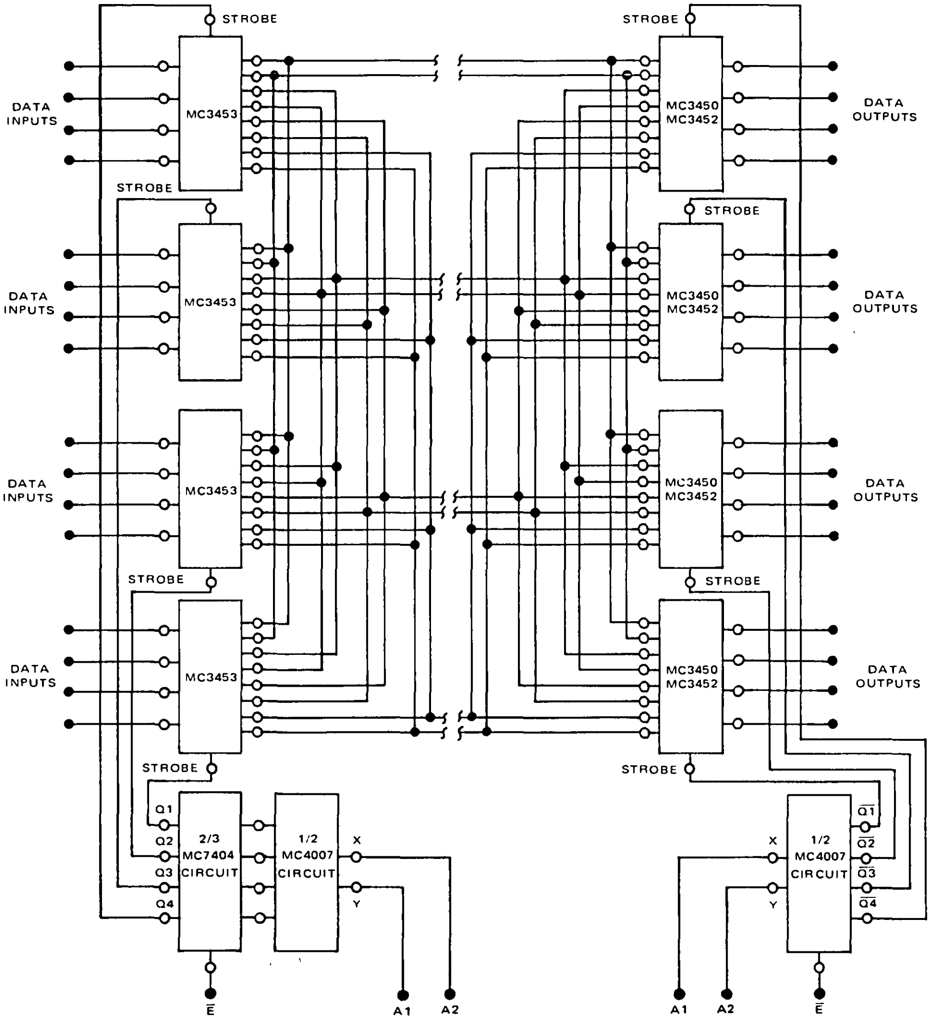
The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum This low-input overdrive enhances differential noise immunity Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects

FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



MOTOROLA

MC3453

QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

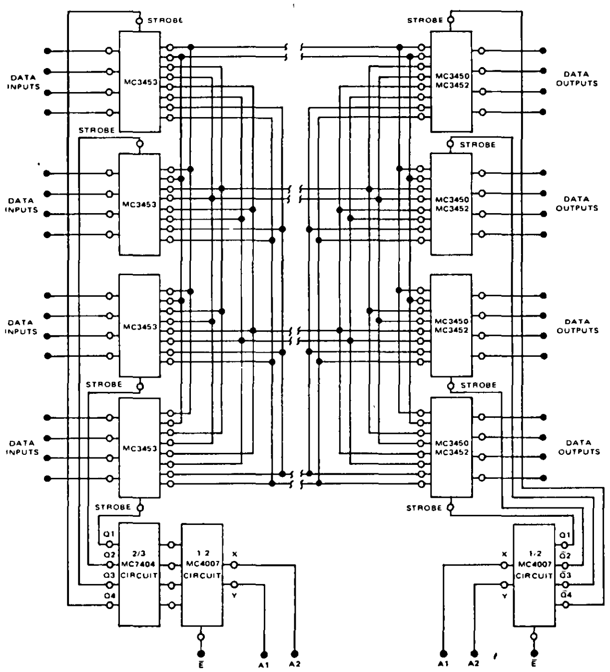
SILICON MONOLITHIC INTEGRATED CIRCUIT

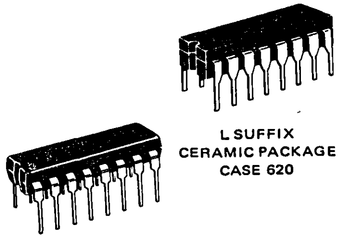
MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four MC75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- -3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular MC75110

FIGURE 1 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING

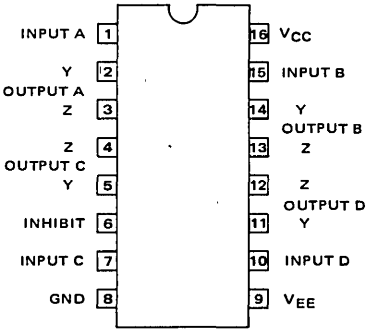




L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM



TRUTH TABLE
(positive logic)

LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT	
		Z	Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual In-Line Packages		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range	V_{OCR}				Volts
Positive		0	–	+10	
Negative		0	–	-3.0	

Note 1. These voltage values are in respect to the ground terminal.

Note 2. When not using all four channels, unused outputs must be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs)	I_{IH_L}				
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)		–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)		–	–	1.0	mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input)	I_{IH_I}				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)		–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)		–	–	1.0	mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state)	$I_{O(on)}$				mA
(V_{CC} = Max, V_{EE} = Max)		–	11	15	
(V_{CC} = Min, V_{EE} = Min)		6.5	11	–	
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.

##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	– –	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	– –	16 20	25 25	ns

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

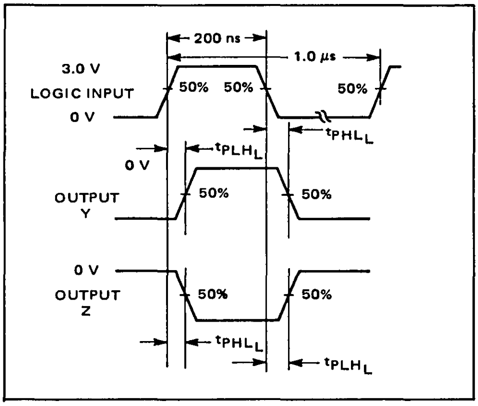
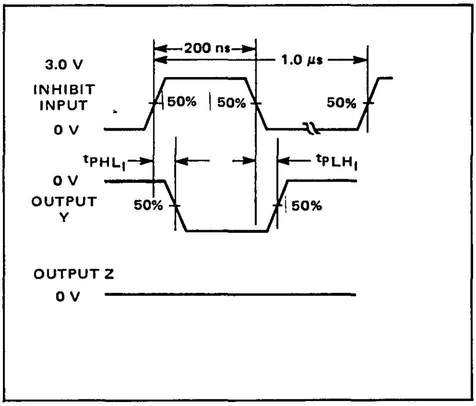
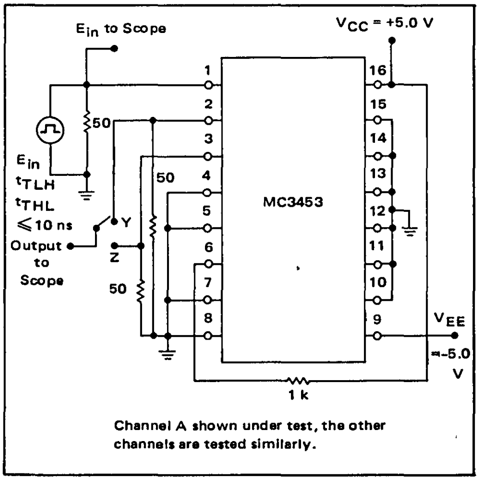


FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



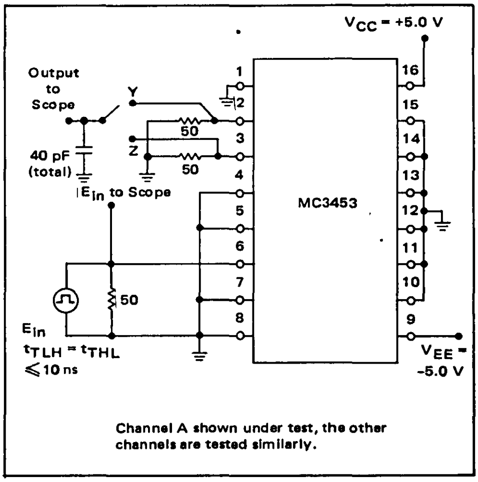
TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



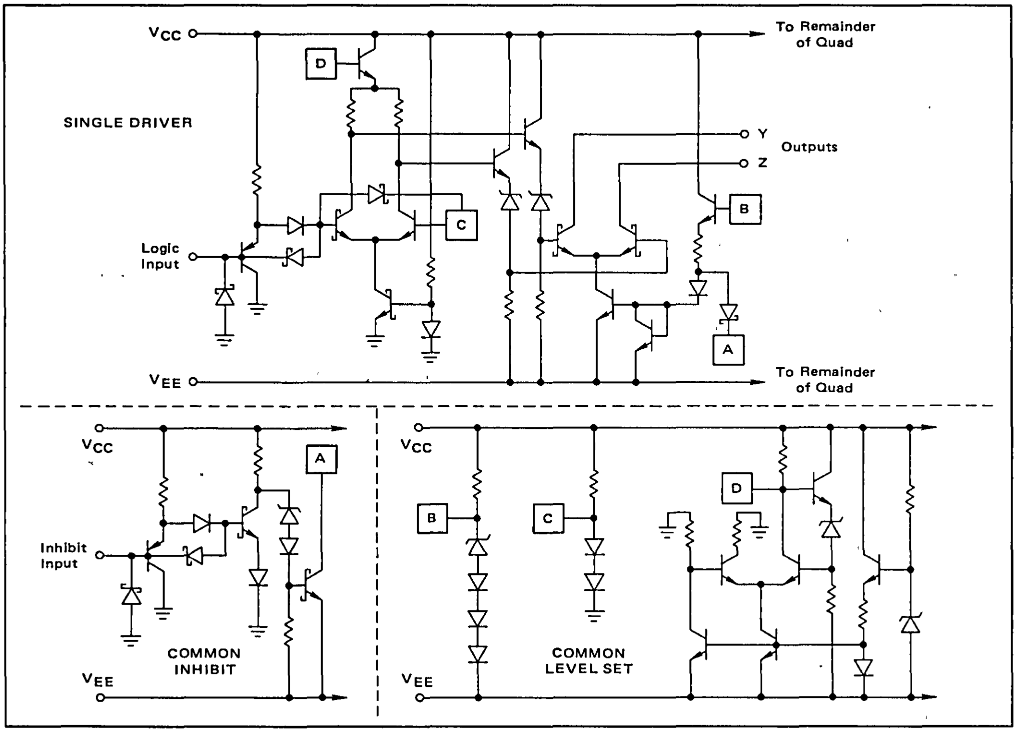
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



Channel A shown under test, the other channels are tested similarly.

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



MOTOROLA

MC3481
MC3485

Product Preview

QUAD SINGLE-ENDED LINE DRIVER

The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification. The two options of enable, fault flag and output configuration provide the designer flexibility in system configuration and simplifies fault flagging.

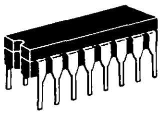
Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operation.

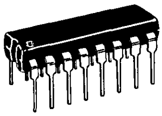
- Separate Enable and Fault Flags – MC3481
- Common Enable and Fault Flag – MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed
- Internal Bootstraps for Faster Rise Times
- 10% Supply Tolerance
- MC3485 has LS Totem Pole $\overline{\text{Driver}}$ Output

IBM 360/370
QUAD
LINE DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 620

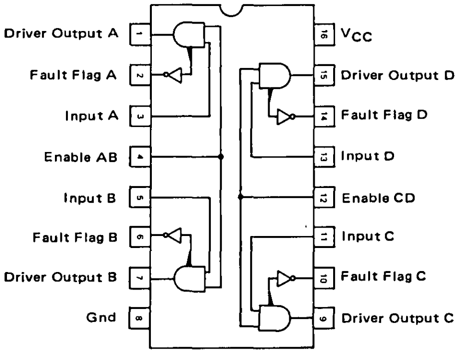




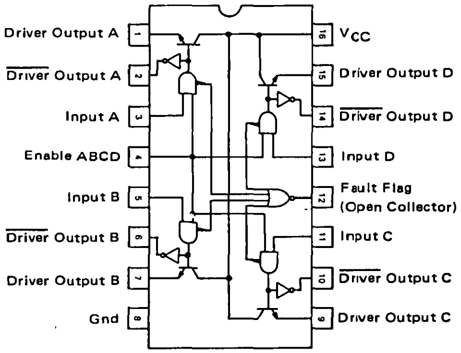
P SUFFIX
PLASTIC PACKAGE
CASE 648

SPECIFICATION GUARANTEE COMPLIANCE WITH
IBM 360/370 INPUT/OUTPUT PERIPHERAL SPECIFICATION GA22-6974-3

MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



See MC75125/7 and MC75128/9 Line Receivers.

This is advance information and specifications are subject to change without notice.

MOTOROLA

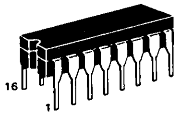
MC3486

QUAD RS-422/423 LINE RECEIVER

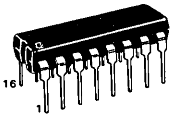
Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- TTL Compatible
- Single 5 V Supply Voltage
- DS 3486 Second Source

QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

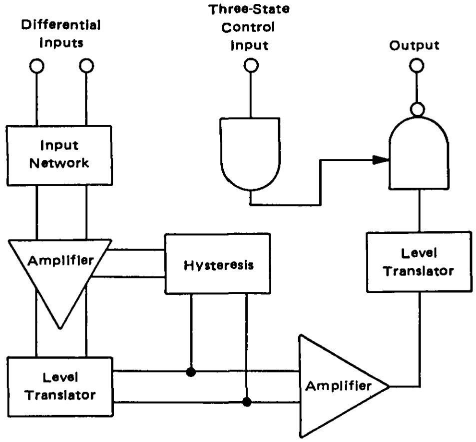


L SUFFIX
CERAMIC PACKAGE
CASE 620

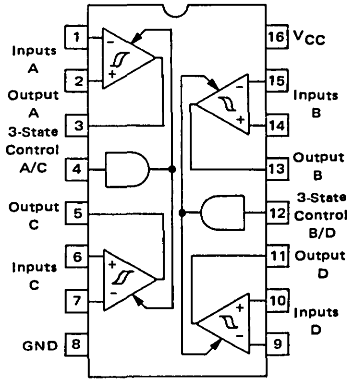


P SUFFIX
PLASTIC PACKAGE
CASE 648

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	±15	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^\circ C$, $V_{CC} = 5.0$ V and $V_{IK} = 0$ V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage (Note 4) (-7.0 V $\leqslant V_{IC} \leqslant 7.0$ V, $V_{IH} = 2.0$ V)	$V_{TH(D)}$				V
($I_O = -0.4$ mA, $V_{OH} \geqslant 2.7$ V)		—	—	0.2	
($I_O = 8.0$ mA, $V_{OL} \geqslant 0.5$ V)		—	—	-0.2	
Input Bias Current ($V_{CC} = 0$ V or 5.25) (Other Inputs at 0 V)	$I_{IB(D)}$				mA
($V_I = -10$ V)		—	—	-3.25	
($V_I = -3.0$ V)		—	—	-1 50	
($V_I = +3.0$ V)		—	—	+1.50	
($V_I = +10$ V)		—	—	+3.25	
Input Balance and Output Level (-7.0 V $\leqslant V_{IC} \leqslant 7.0$ V, $V_{IH} = 2.0$ V, See Note 3)					V
($I_O = -0.4$ mA, $V_{ID} = 0.4$ V)	V_{OH}	2.7	—	—	
($I_O = 8$ 0 mA, $V_{ID} = -0.4$ V)	V_{OL}	—	—	0.5	
Output Third State Leakage Current	I_{OZ}				µA
($V_{I(D)} = +3.0$ V, $V_{IL} = 0.8$ V, $V_{OL} = 0.5$ V)		—	—	-40	
($V_{I(D)} = -3.0$ V, $V_{IL} = 0.8$ V, $V_{OH} = 2.7$ V)		—	—	40	
Output Short-Circuit Current ($V_{I(D)} = 3.0$ V, $V_{IH} = 2.0$ V, $V_O = 0$ V) See Note 2)	I_{OS}	-15	—	-100	mA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.5$ V)	I_{IL}	—	—	-100	µA
Input Current — High Logic State (Three-State Control)	I_{IH}				µA
($V_{IH} = 2.7$ V)		—	—	20	
($V_{IH} = 5.25$ V)		—	—	100	
Input Clamp Diode Voltage (Three-State Control) ($I_{IK} = -10$ mA)	V_{IK}	—	—	-1.5	V
Power Supply Current ($V_{IL} = 0$ V)	I_{CC}	—	—	85	mA

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	35	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted
2. Only one output at a time should be shorted
3. Refer to EIA RS422/3 for exact conditions Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS

Propagation Delay Differential Input to Output

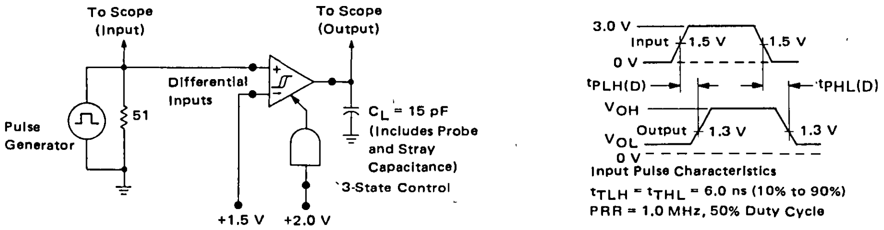
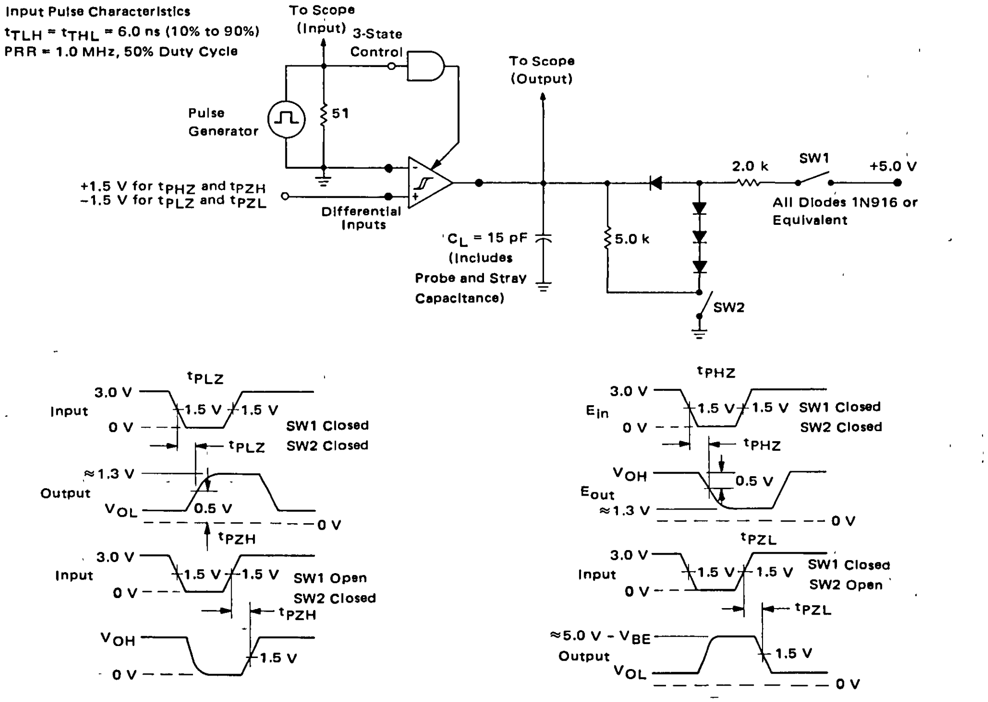


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



MOTOROLA

MC3487

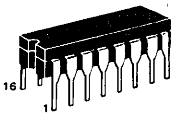
QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad RS-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

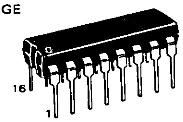
- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Second Source

QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

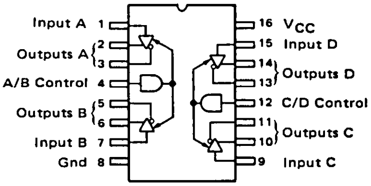


L SUFFIX
CERAMIC PACKAGE
CASE 620

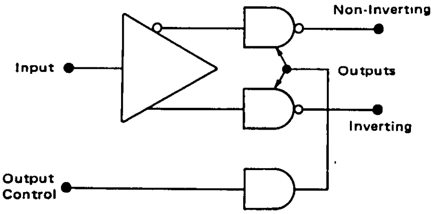


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



DRIVER BLOCK DIAGRAM



TRUTH TABLE			
Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*ABSOLUTE MAXIMUM RATINGS			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V $\leq V_{CC} \leq$ 5.25 V and 0°C $\leq T_A \leq$ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-400	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	 – –	 – –	 +50 +100	µA
Input Clamp Voltage (I_{IK}= -18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = −20 mA)	V_{OH}	2.5	–	–	V
Output Short-Circuit Current (V_{IH} = 2.0 V) 2	I_{OS}	-40	–	-140	mA
Output Leakage Current – Hi-Z State (V_{IL} = 0.5 V, $V_{IL(Z)}$ = 0.8 V) (V_{IH} = 2.7 V, $V_{IL(Z)}$ = 0.8 V)	$I_{OL(Z)}$	 – –	 – –	 ±100 ±100	µA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = -0.25 V, V_{CC} = 0 V)	$I_{OL(off)}$	 – –	 – –	 +100 -100	µA
Output Offset Voltage Difference1	$V_{OS}-\overline{V}_{OS}$	–	–	±0.4	V
Output Differential Voltage 1	V_T	2.0	–	–	V
Output Differential Voltage Difference 1	$V_T - \overline{V}_T$	–	–	±0.4	V
Power Supply Current (Control Pins = Gnd)3 (Control Pins = 2.0 V)	 I_{CCX} I_{CC}	 – –	 – –	 105 85	mA

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Transition Times – Differential High to Low Output Low to High Output	 t_{THL} t_{TLH}	 – –	 – –	 20 20	ns
Propagation Delay – Control to Output (R_L = 200 Ω, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF) (R_L = ∞, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF)	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 25 25 30 30	ns

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

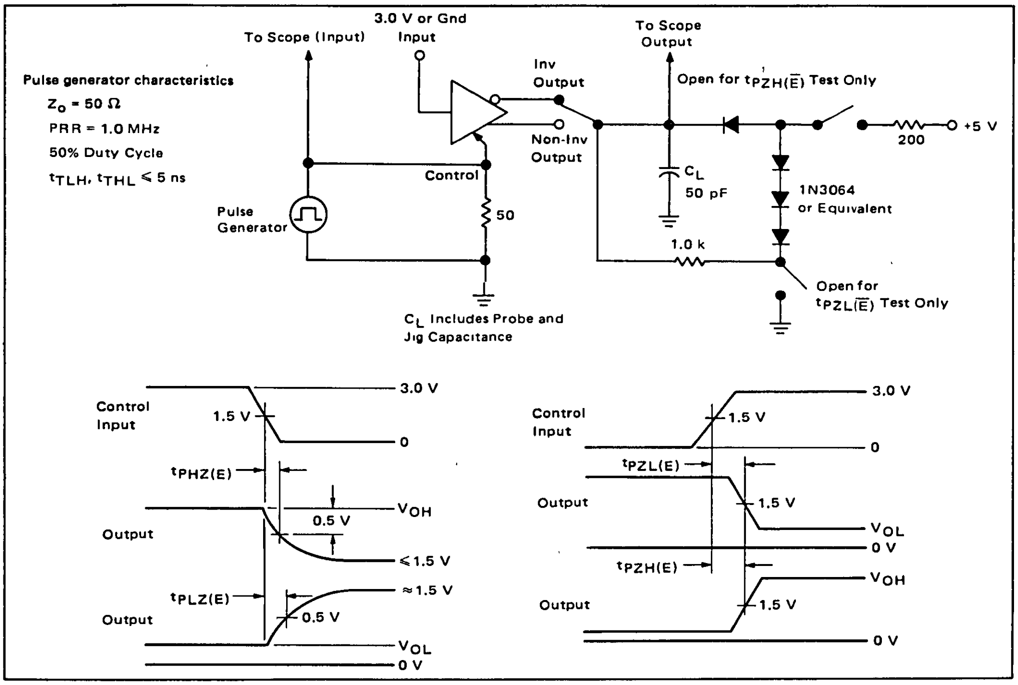


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT

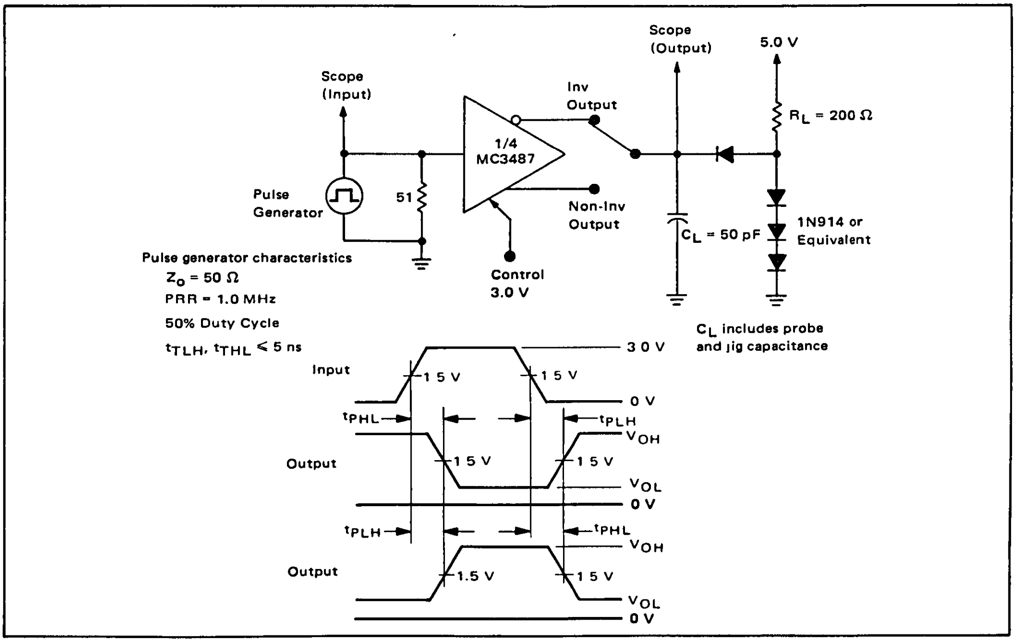


FIGURE 3 — OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

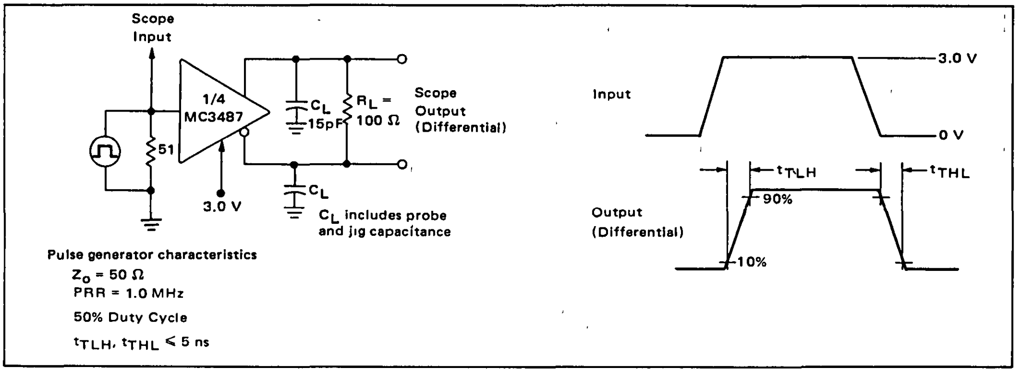


FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE

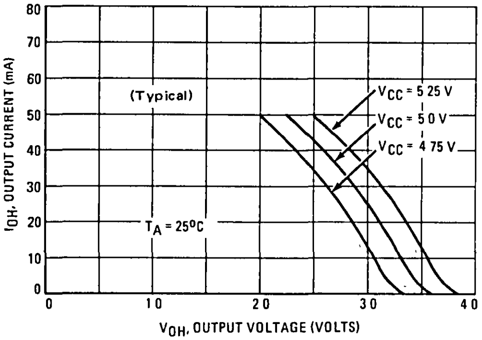
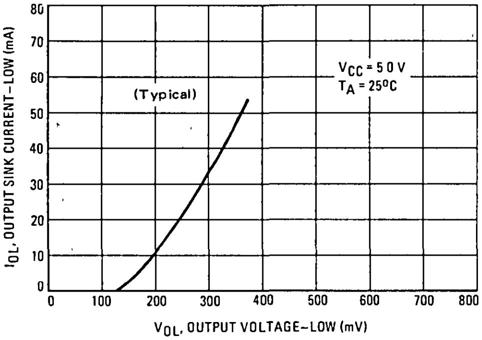


FIGURE 5 — OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



MOTOROLA

MC3488A
MC3488B

Product Preview

DUAL RS-423/RS-232C DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

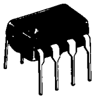
DUAL RS-423/RS-232C LINE DRIVERS

The MC3488A and MC3488B dual single-ended line drivers have been designed to satisfy the requirements of EIA standards RS-423 and RS-232C, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. They are suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μs to 100 μs by a single external resistor. Output level and slew rate are independent of power supply variations or matching. Input undershoot diodes limit transients below ground; output current limiting is provided in both output states. They can be operated with supply voltages from ±9.0 to ±15 V.

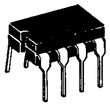
The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility. The MC3488B input logic threshold is set at $V_{CC}/2$ for use with CMOS logic systems.

- PNP Buffered Inputs to Minimize Input Loading
- Wide Power Supply Operating Range
- Adjustable Slew Rate Limiting
- Option of Either 1.5 V or $V_{CC}/2$ Input Threshold
- MC3488A Equivalent to 9636A
- Logic Levels and Slew Rate Independent of Power Supply Voltages or Matching

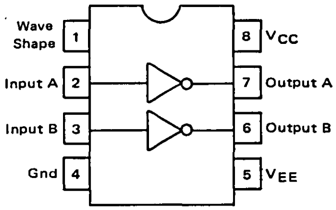
P1 SUFFIX
PLASTIC PACKAGE
CASE626



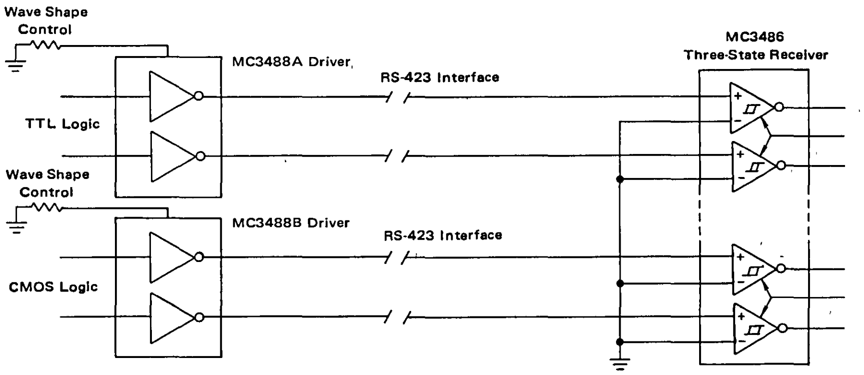
U SUFFIX
CERAMIC PACKAGE
CASE 693



PIN CONNECTIONS



TYPICAL APPLICATION



This is advance information and specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+15 -15	V
Output Current Source Sink	 I_{O+} I_{O-}	 +150 -150	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITION

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	10.8 10.8	12 -12	13.2 -13.2	V
Operating Temperature Range	T_A	0	25	70	°C
Wave Shaping Resistor	R_W	10	–	500	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over $0^{\circ}C < T_A < 70^{\circ}C$, $9.0\ V < |V_{CC}, V_{EE}| < 15\ V$ and $2.0\ k < R_W < 400\ k$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State MC3488A MC3488B	V_{IL}	 – –	 – –	 0.8 $V_{CC}/2$ -2.0	V
Input Voltage — High Logic State MC3488A MC3488B	V_{IH}	 2.0 $V_{CC}/2 + 2.0$	 – –	 – –	V
Input Current — Low Logic State ($V_{IL} = 0.4$ V)	I_{IL}	 –	 –	 -80	µA
Input Current — High Logic State ($V_{IH} = 2.4$ V) MC3488A ($V_{IH} = 5.5$ V) MC3488A ($V_{IH} = V_{CC}$) MC3488B	I_{IH}	 – – –	 – – –	 10 100 100	µA
Input Clamp Diode Voltage ($I_{IK} = -15$ mA)	V_{IK}	 –	 –	 -1.5	V
Output Voltage — Low Logic State ($R_L = \infty$) RS-423 ($R_L = 3.0$ kΩ) RS-232C ($R_L = 450$ Ω) RS-423	V_{OL}	 -5.0 -5.0 -4.0	 – – –	 -6.0 -6.0 -6.0	V
Output Voltage — High Logic State ($R_L = \infty$) RS-423 ($R_L = 3.0$ kΩ) RS-232C ($R_L = 450$ Ω) RS-423	V_{OH}	 5.0 5.0 4.0	 – – –	 6.0 6.0 6.0	V
Output Short-Circuit Current	I_{SC+} I_{SC-}	+15 -15	– –	150 -150	mA
Output Leakage Current ($V_{CC} = V_{EE} = 0$ V, $-6.0\ V < V_o < 6.0$ V)	I_{ox}	-100	–	100	µA
Power Supply Current ($R_W = 2.0$ kΩ) ($R_W = 2.0$ kΩ)	 I_{CC} I_{EE}	 – –	 – –	 +18 -18	mA
Output Resistance ($R_L \geqslant 450$ Ω)	R_O	 –	 25	 50	Ω

Note: A diode is connected in series with V_{EE} for all test conditions.

TRANSITION TIMES (Unless otherwise noted, C_L = 30 pF, f = 1.0 kHz, V_{CC} = 12 V, V_{EE} = -12 V, T_A = 25°C, R_L = 450 Ω. Transition times measure 10% to 90% and 90% to 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low to High State Output	t_{TLH}				µs
(R_W = 10 kΩ)		0.8	–	1.4	
(R_W = 100 kΩ)		8.0	–	14	
(R_W = 500 kΩ)		40	–	70	
(R_W = 1000 kΩ)		80	–	140	
Transition Time, High to Low State Output	t_{THL}				µs
(R_W = 10 kΩ)		0.8	–	1.4	
(R_W = 100 kΩ)		8.0	–	14	
(R_W = 500 kΩ)		40	–	70	
(R_W = 1000 kΩ)		80	–	140	

FIGURE 1 – TEST CIRCUIT & WAVEFORMS FOR TRANSITION TIMES

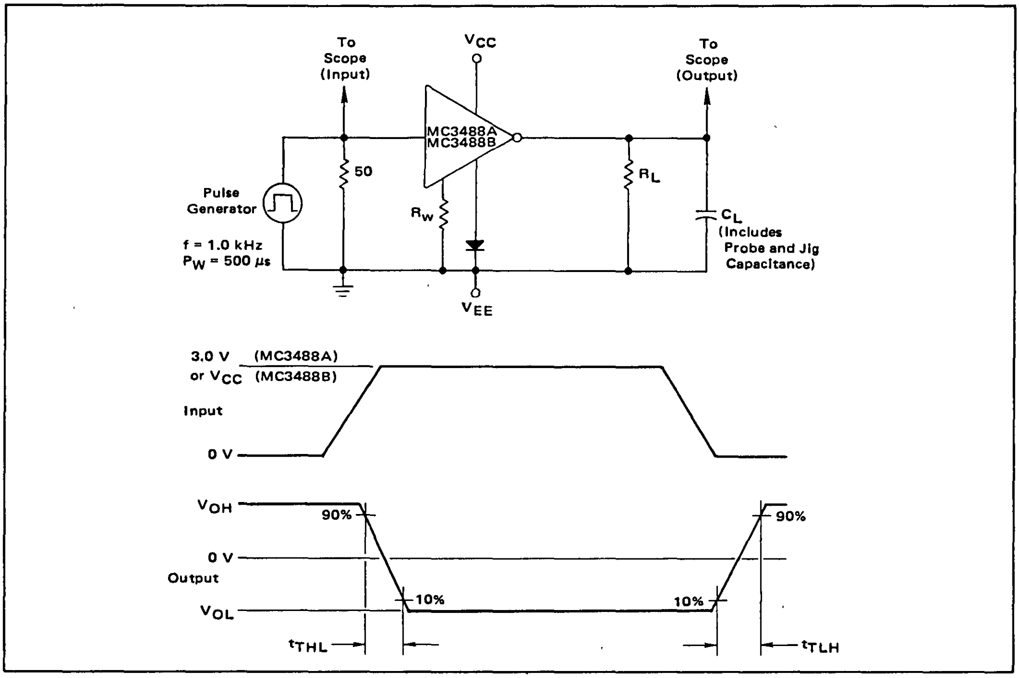
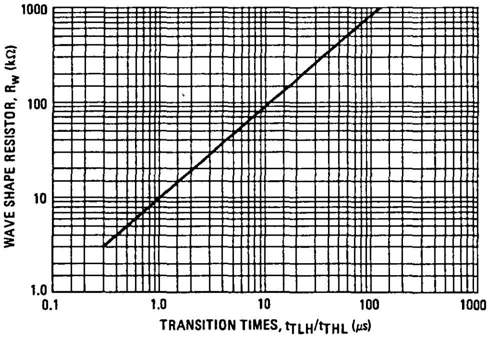


FIGURE 2 – OUTPUT TRANSISTION TIMES versus WAVE SHAPE RESISTOR VALUE



MOTOROLA

MC3490 MC3494

ANODE (DIGIT) DRIVERS FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC INTEGRATED CIRCUIT

SEVEN-DIGIT GAS-DISCHARGE DISPLAY DRIVERS

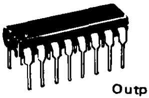
Seven channel digit (anode) drivers, the MC3490 and MC3494 are specifically conceived to be used with high-voltage, gas-discharge numeric displays such as the Burroughs' Panaplex®, Beckman (Sperry) Cherry, or Diacon displays.

The MC3490 version is configured such that a high logic level input causes the driver to turn on while the MC3494 requires a low logic level to turn the drivers on. Both devices are designed to mate with the MC3491 cathode (segment) driver.

With a low input current requirement of only 300 µA typically, these devices are compatible with popular MOS chips.

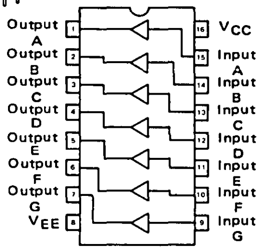
Minimum breakdown voltage is specified at 48 V and output drive current capability is typically 30 mA per channel.

- High Breakdown Voltage – 55 V Typical
- Low Input Current for MOS Compatibility
- Available with Either Active High or Active Low Inputs
- Operable from Either Positive or Negative Supply Voltages
- Input Clamp Diodes on MC3494 Version for DC Restoration
- Internal Pull-down Resistors

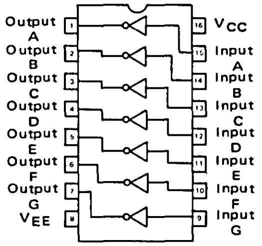


P SUFFIX
PLASTIC
PACKAGE
CASE 648

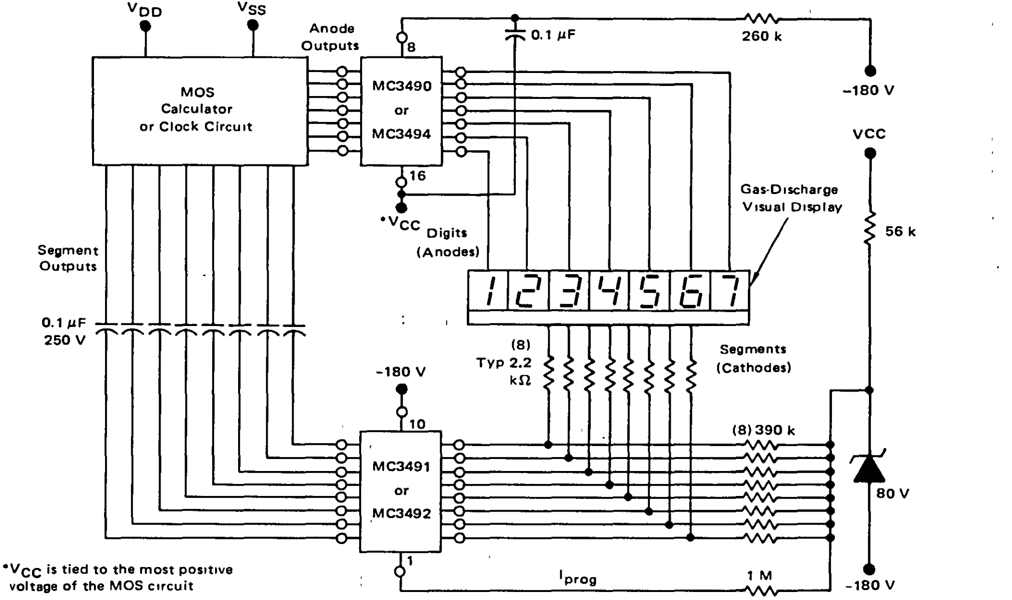
PIN CONNECTIONS
MC3490



MC3494



TYPICAL APPLICATION
WITH CAPACITIVE LEVEL SHIFT TO CATHODE DRIVER



*VCC is tied to the most positive voltage of the MOS circuit

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Negative Supply Voltage (Current Limited to -5 mA)	V_{EE}	-60	Vdc
Negative Supply Current	I_{EE}	-5.0	mAdc
Input Voltage	V_I	V_{CC}-20, V_{CC}	Vdc
Output Current (V_O = -5 V)	I_O	-50	mAdc
Package Power Dissipation Derate above 25°C	P_D	830 6.7	mW mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = Gnd V_{EE} = -60 V thru 5.0 kΩ, unless otherwise noted.)

Characteristic	Symbol	MC3490			MC3494			Unit
		Min	Typ	Max	Min	Typ	Max	
Substrate Breakdown Voltage	$V_{S(BR)}$	-48	-55	–	-48	-55	–	Vdc
Input Current – On State	$I_{I(on)}$							µA
V_I = 0.0 V (See Figure 4)		–	250	700	–	–	–	
V_I = -7.0 V (See Figure 3)		–	–	–	–	-200	-350	
Input Current – Off State	$I_{I(off)}$							µA
V_I = -15 V		–	<-1.0	-45	–	–	–	
V_I = 0.0 V		–	–	–	–	<1.0	50	
Input Voltage – Off State $V_O \approx V_{EE}$ (See Figures 3 and 4)	$V_{I(off)}$	–	–	-5.0	-2.0	–	–	Vdc
Input Voltage – On State V_O = V_{CC}-5.0 V (See Figures 3 and 4)	$V_{I(on)}$	-2.0	–	–	–	–	-5.0	Vdc
Output Voltage – Off State	$V_{O(off)}$							Vdc
V_I = 0.0 V		–	–	–	-48	–	–	
V_I = -7.0 V		-48	–	–	–	–	–	
Output Voltage – On State	$V_{O(on)}$							Vdc
I_O = -20 mA, V_I = 0.0 V		–	–	-3.5	–	–	–	
I_O = -20 mA, V_I = -7.0 V		–	–	–	–	–	-5.0	

NOTE: Minimums and maximums are relative to absolute values.

SYSTEM DISCUSSION

The MC3491 and MC3490/MC3494 high voltage driver system is designed such that it can be floated and any point in the system may be tied to circuit ground. In a MOS system, normally either the ground pin on the MC3491 is tied to the most negative MOS voltage; or the V_{CC} pin on the MC3490/MC3494 is connected to the most positive MOS voltage. In the electrical characteristics table, this V_{CC} voltage is assumed to be 0.0 volts.

The MC3490/MC3494 provides its own internal voltage reference when a current (-100 µA to -5 mA) is drawn at the V_{EE} pin (Pin 8). This can be provided by connecting a resistor from Pin 8 to the high voltage reference on the cathode driver or any other voltage more negative than V_{CC} -60 V. This voltage (Pin 8) is approximately -55 V and provides a reference for the pull-down function for each channel.

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1 – SUBSTRATE CURRENT versus SUBSTRATE VOLTAGE

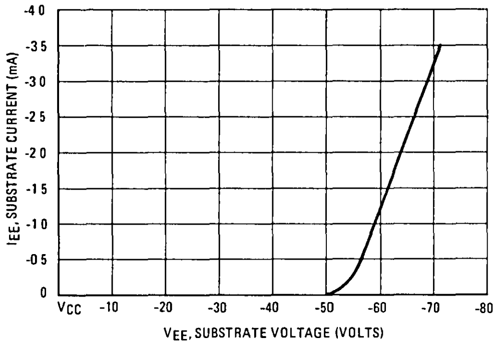


FIGURE 2 – PERMISSIBLE OPERATING RANGE

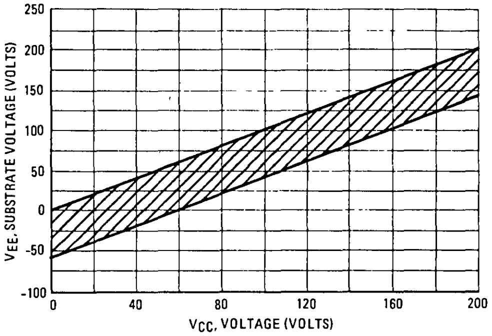


FIGURE 3 – OUTPUT VOLTAGE and INPUT CURRENT versus INPUT VOLTAGE

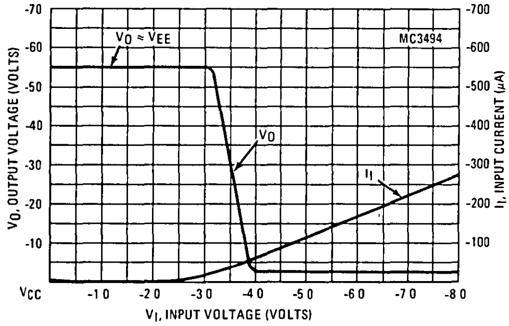
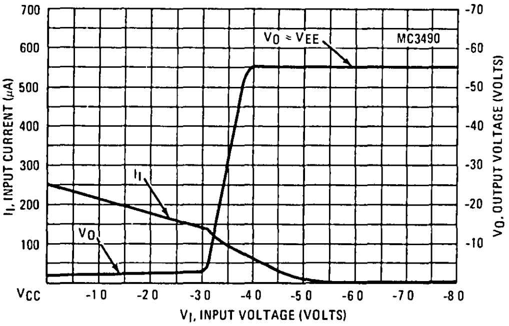
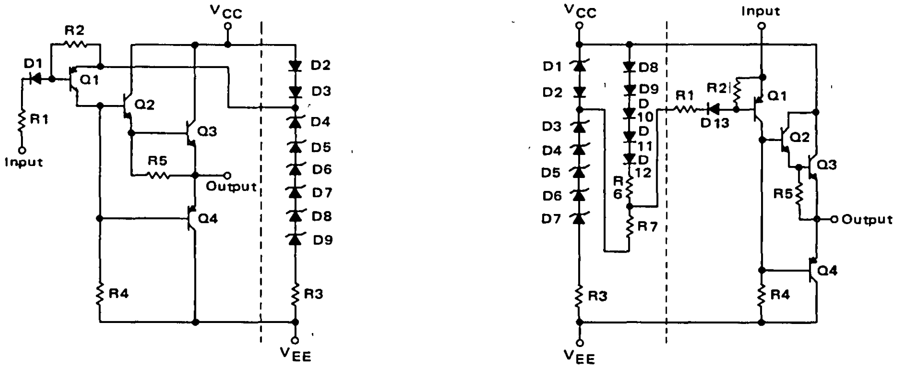


FIGURE 4 – INPUT CURRENT and OUTPUT VOLTAGE versus INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/7 Shown)


MC3494

MC3490

12-DIGIT CMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, it is generally more economical to level translate down to the cathode segments than to translate up to the digit anodes. An example of this technique is shown in the 12 digit display system where the display anodes and cathodes are referenced to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V (V_{DD} = 0, V_{SS} = -10 V) with the MC14558 decoder outputs capacitor-coupled to the MC3491 Segment Drivers and the scan circuit directly-coupled to the MC3490 Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required as compared to 12 capacitors, if the strobed digit drivers were ac coupled.

The MC3491 has input clamp diodes allowing for dc restoration of the segment address pulse. This high voltage driver (80 V) also features programmable segment current by the selection of a single external resistor.

The MC3490 Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494 Anode Driver should be used.) The internal zener diode string of the MC3490 references the off drivers (and display anodes) to -50 V without the need of pull-down resistors.

Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Drivers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490s, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

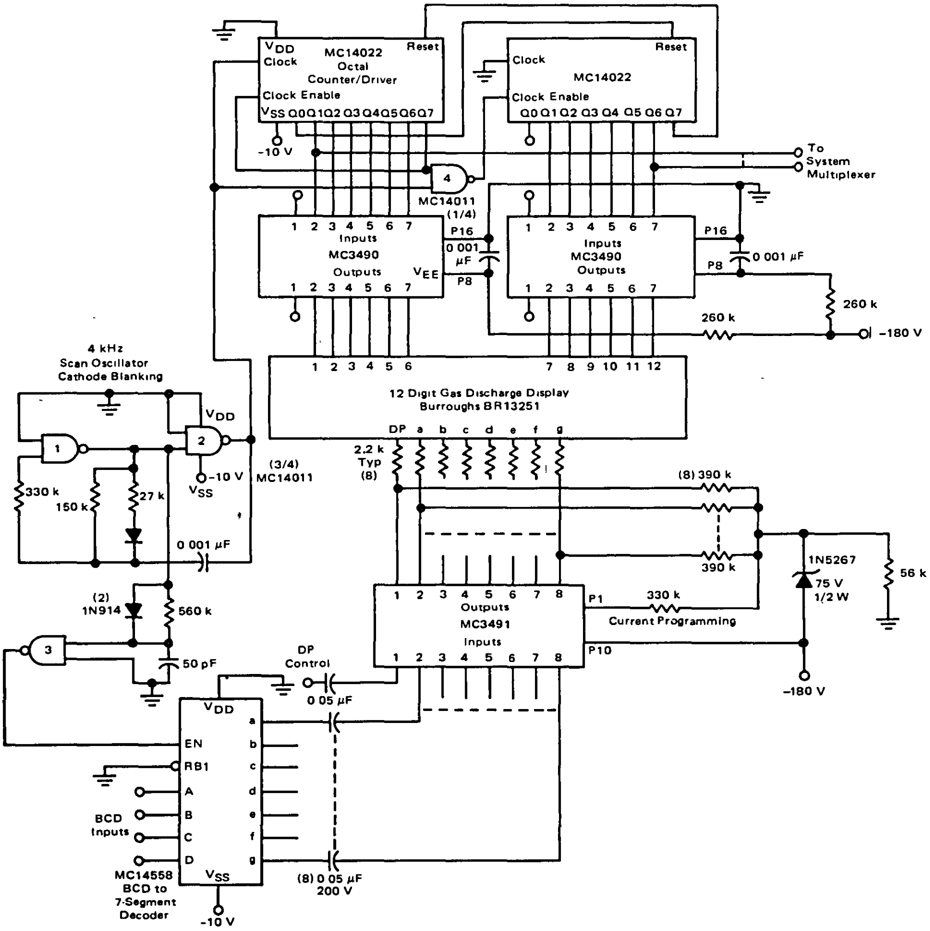
The MC14558 BCD-to-Seven Segment Decoder has an Enable input which readily provides for display cathode blanking For the illustrated display, the cathode drivers should be turned off prior to anode switching and maintained off for some period after the next anode is strobed.

This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrated network and inverter Gate 3.

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 5 – 12-DIGIT CMOS GAS DISCHARGE DISPLAY SYSTEM



3-1/2 DIGIT VOLTMETER

This specific application provides a 3-1/2 digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2 Digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the MC3494 **Anode Drivers.** Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors, connected in a common-base, constant-current configuration, are turned on by the negative going digit select output pulses of the MC14435 The current of approximately 330 µA is compatible with 200 µA typical input current of the MC3494 and the sink current capability of the MC14435

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 Segment Driver. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment current is increased accordingly to 1.1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

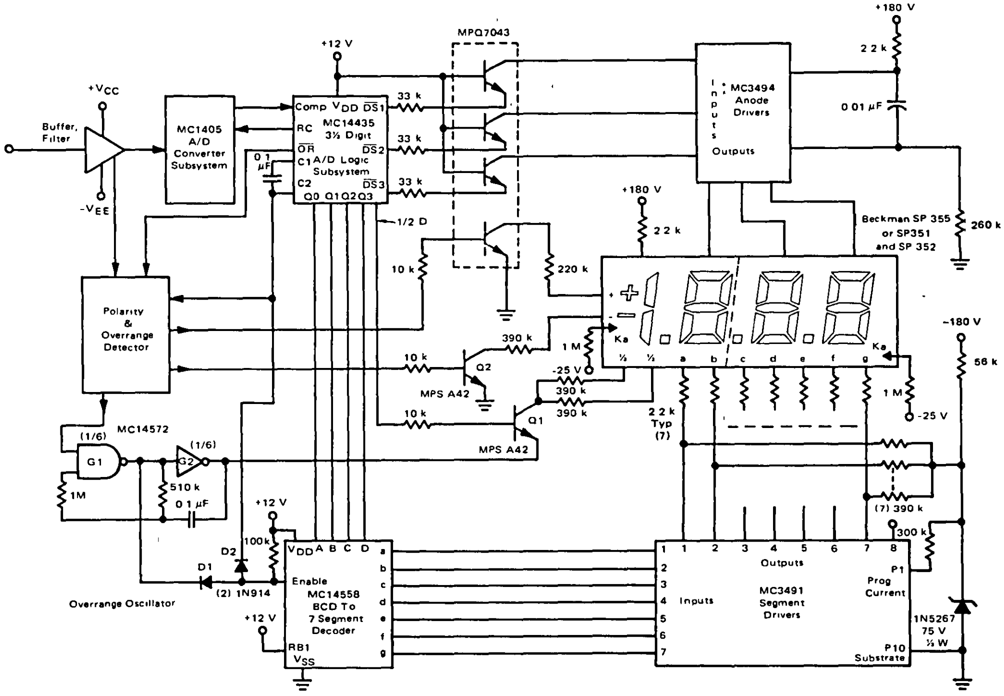
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits

The 1/2 digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 — 3-½ DIGIT DIGITAL VOLTMETER



12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 cathode driver and MC3494 anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6 digit clock display with multiplexed 7 segment outputs. The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the MC3491. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494 anode driver.

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 kΩ resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

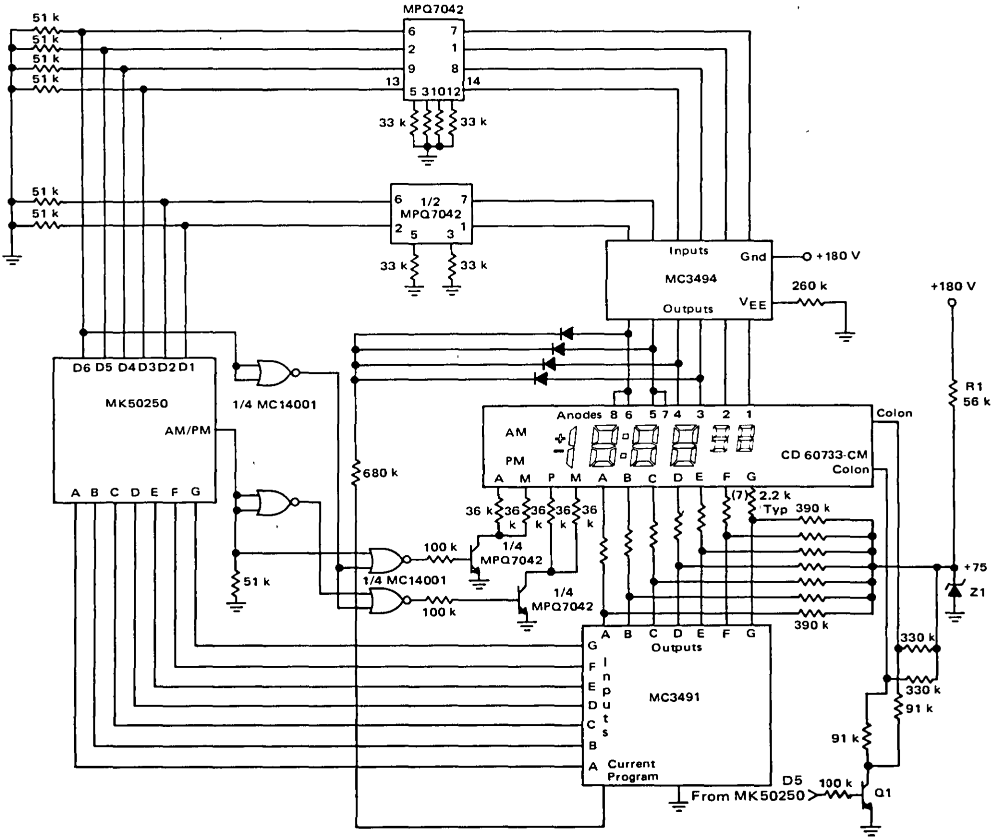
The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494 anode drivers. Inter-digit blanking is provided in the anode circuits. Level translation from the clock chip output to the input to the MC3494 uses two MPQ7042 quad high voltage transistor packages operating in an emitter follower current source mode. Each current source turns on one of the MC3494 drivers by sinking 300 μA to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has a 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 7 — 12 HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



MOTOROLA

MC3491
MC3492

EIGHT-SEGMENT VISUAL DISPLAY DRIVERS

The MC3491 and MC3492 are eight-segment cathode drivers for use with gas-discharge displays, such as the Burroughs' Panaplex®, Beckman, Cherry or Diacon types. Both devices are directly compatible with MOS logic outputs due to their low 300 µA input current requirement.

All eight driver output currents are simultaneously programmable by selection of a single external resistor. As programmed, all eight currents match to within typically 1% of each other.

Both devices provide dc restoration. The units are specified for a minimum breakdown voltage of 80 V.

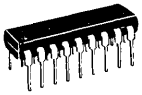
The MC3492 device is made for larger and higher intensity displays requiring higher segment current.

- High Breakdown Voltage – 80 V Min*
- Drives Seven Cathode Segments plus Decimal Point
- All Currents Simultaneously Programmable with One Resistor
- MC3491 is Pin-for-Pin and Functionally Equivalent to DM8889
- Output Current/Programming Current Ratio –
  Typically 4.5:1 for MC3491
  9:1 for MC3492
- Companion with MC3490 and MC3494 Anode Drivers
- MC3492 Provides Increased Output Current for High Intensity Displays

*Higher Voltage Selection Available

SEGMENT DRIVERS FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

PIN CONNECTIONS

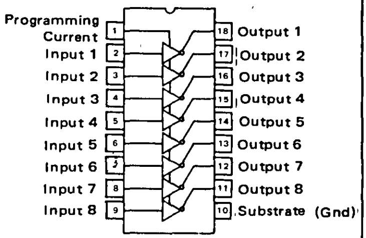
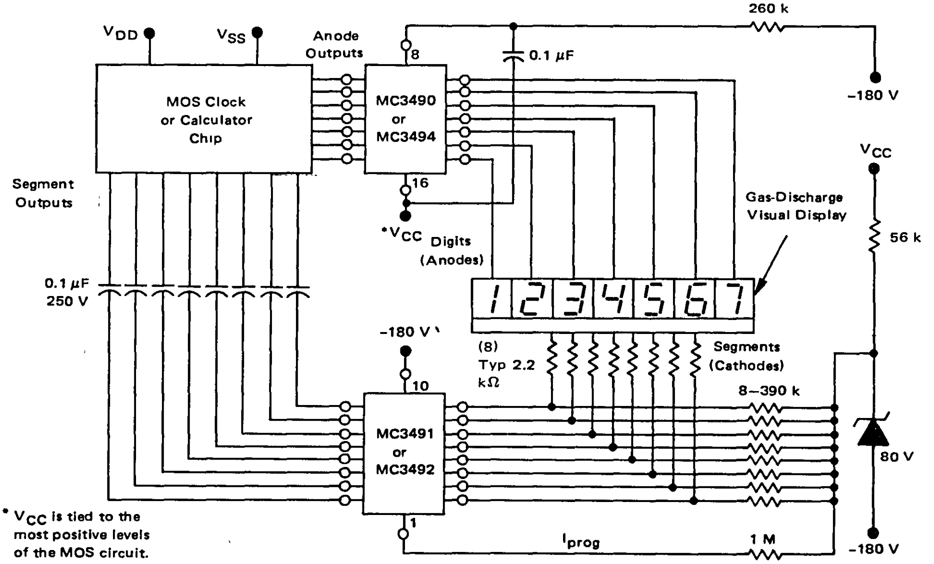


FIGURE 1 – TYPICAL CALCULATOR APPLICATION WITH CAPACITIVE LEVEL SHIFT AND ANODE DRIVER



* V_CC is tied to the most positive levels of the MOS circuit.

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MAXIMUM RATINGS (Unless otherwise noted, T_A = 25°C)

Rating	Symbol	Value	Unit
Output OFF Voltage (Current Limited to 0 5 mA)	$V_{O(off)}$	95	V
Output ON Voltage (Current Limtied to 2 0 mA)	$V_{O(on)}$	50	V
Input Voltage	V_I	20	V
Programming Current	I_{prog}		µA
MC3491		400	
MC3492		2500	
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V_{CC} \leq 80$ V, T_A = 25°C, Pin 10 = Gnd. All voltages with respect to Gnd.)

Characteristic	Symbol	MC3491			MC3492			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Current (V_{IH} = 7.0 V)	I_{IH}	200	300	400	200	300	400	µA
Input Clamp Voltage (I_{IK} = -1.0 mA)	V_{IK}	–	–	-1.0	–	–	-1.0	V
Input OFF Voltage	V_{IL}	1.0	1.5	–	1.0	1.5	–	V
Input ON Voltage	V_{IH}	–	2.4	3.5	–	2.4	3.5	V
Output OFF Current (V_{IL} = 0 V, V_O = V_{CC})	$I_{O(off)}$	–	–	5.0	–	–	5.0	µA
Output ON Current (at V_{IH} = 7.0 V)*	$I_{O(on)}$							µA
(I_{prog} = 100 µA)		400	450	500	–	–	–	
(I_{prog} = 350 µA)		1450	1650	1850	–	–	–	
(I_{prog} = 200 µA)		–	–	–	1.3	1.6	1 9	mA
(I_{prog} = 500 µA)		–	–	–	3.75	4.5	5.25	
Output Current Matching (All eight outputs)	ΔI_O	–	≤ 1	≤ 10	–	≤ 1	≤ 10	%
Output OFF Voltage	$V_{O(off)}$							V
(I_{prog} = 100 µA, R_L = 1.0 MΩ, V_{IL} = 0 V)		V_{CC}-5.0	V_{CC}	–	–	–	–	
(I_{prog} = 200 µA, R_L = 1.0 MΩ, V_{IL} = 0 V)		–	–	–	V_{CC}-5 0	V_{CC}	–	
Output Saturation Voltage	$V_{O(sat)}$							V
(I_{prog} = 100 µA, R_L = 1.0 MΩ, V_{IH} = 7.0 V)		–	3.0	5 0	–	–	–	
(I_{prog} = 200 µA, R_L = 1 0 MΩ, V_{IH} = 7.0 V)		–	–	–	–	3.0	5.0	
Output Voltage Compliance Range	$V_{OR(on)}$							V
(I_{prog} = 100 µA, $I_{O(on)}$ = 450 µA, V_{IH} = 7.0 V) (See Figure 3)		5.0	–	50	–	–	–	
(I_{prog} = 200 µA, $I_{O(on)}$ = 1.6 mA, V_{IH} = 7.0 V) (See Figure 3)		–	–	–	5.0	–	50	

*Measured one channel at a time

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 – OUTPUT CURRENT versus PROGRAMMING CURRENT ($T_A = 25^oC$)

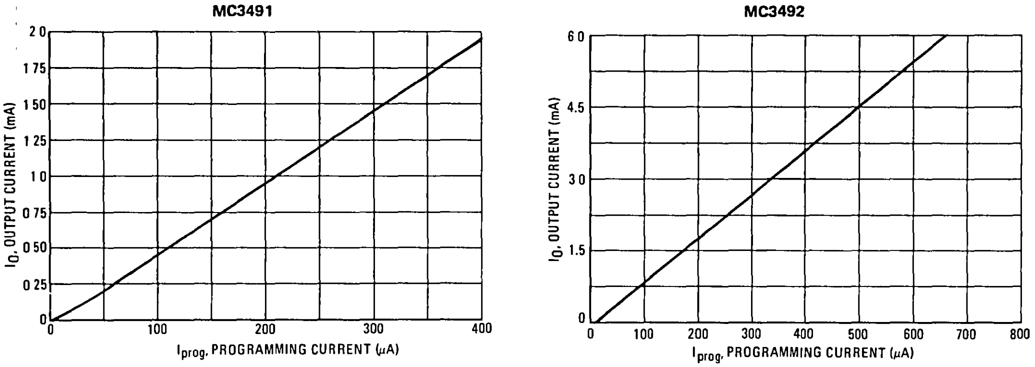


FIGURE 3 – OUTPUT CURRENT versus OUTPUT VOLTAGE ($V_{IH} = 7.0\ V$, $T_A = 25^oC$)

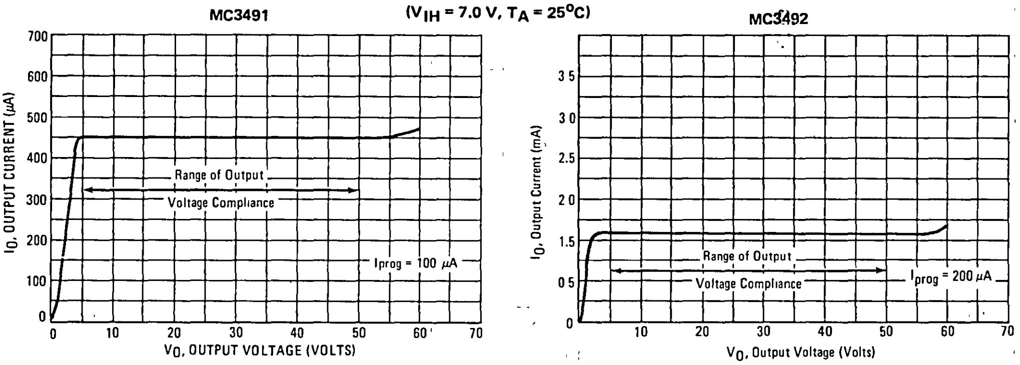
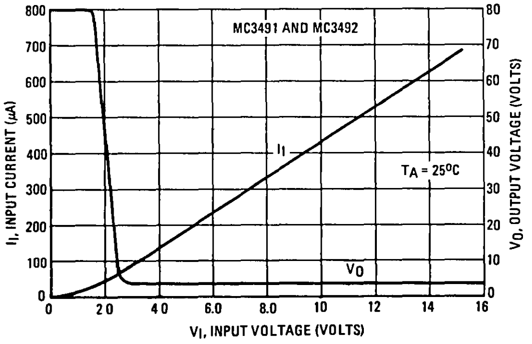
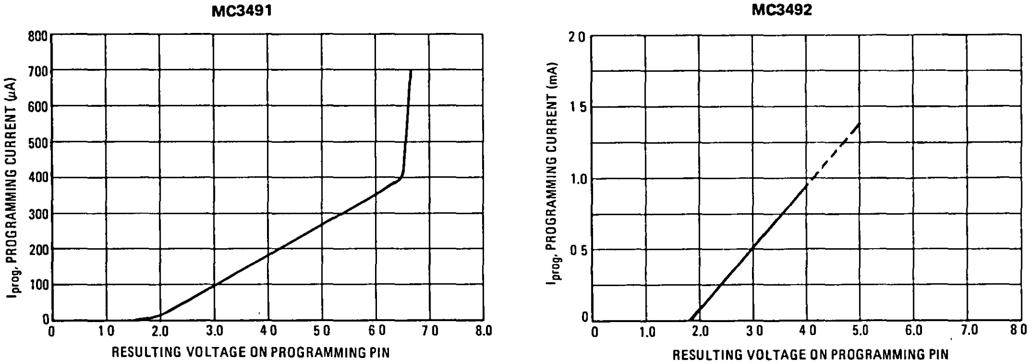


FIGURE 4 – TYPICAL INPUT CURRENT AND OUTPUT VOLTAGE versus INPUT VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS

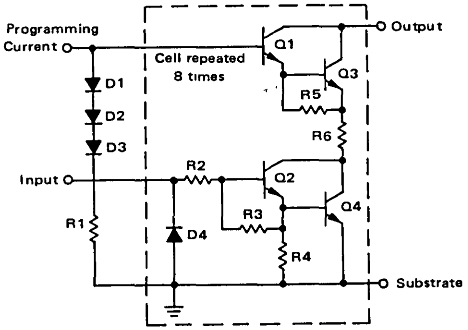
FIGURE 5 — TYPICAL PROGRAMMING CURRENT versus VOLTAGE ON PROGRAMMING PIN (T_A = 25°C)



MC3491

MC3492

REPRESENTATIVE CIRCUIT SCHEMATIC



3-1/2-DIGIT VOLTMETER

This specific application provides a 3-1/2-digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2-digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the MC3494 Anode Drivers. Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors connected in a common-base, constant-current configuration are turned on by the negative-going digit select output pulses of the MC14435. The current of approximately 330 μA is compatible with 200 μA typical input current of the MC3494 and the sink current capability of the MC14435

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 or MC3492 Segment Drivers. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment current is increased accordingly to 1 1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

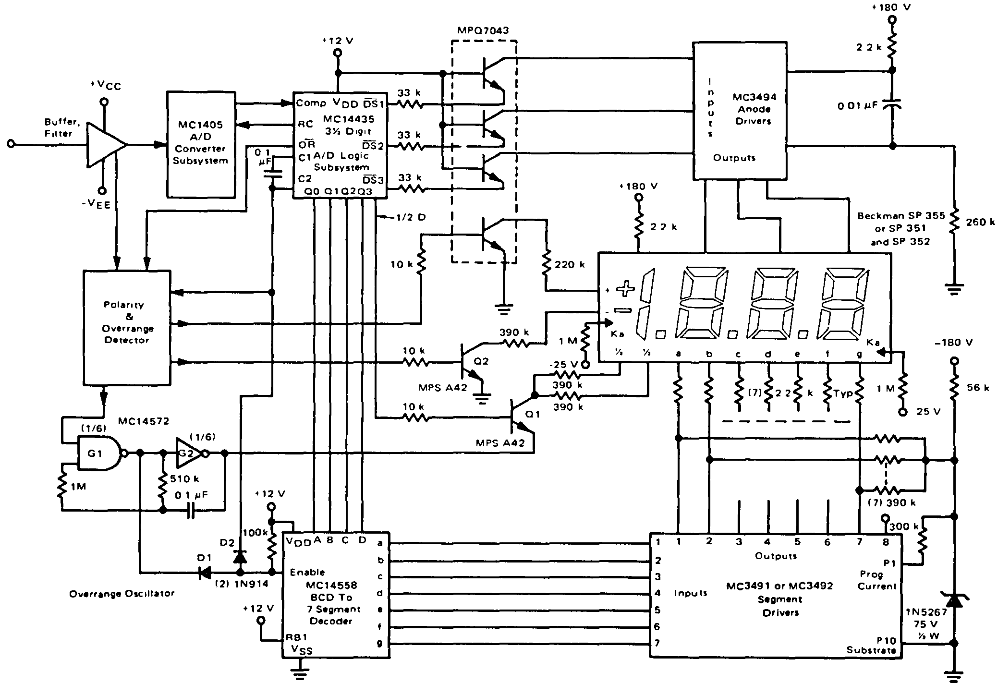
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The 1/2-digit segments are driven by transistor Q1 Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 — 3-½ DIGIT DIGITAL VOLTMETER



12-DIGIT CMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, it is generally more economical to level translate down to the cathode segments than to translate up to the digit anodes. An example of this technique is shown in the 12 digit display system where the display anodes and cathodes are referenced to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V (V_{DD} = 0, V_{SS} = -10 V) with the MC14558 decoder outputs capacitor-coupled to the MC3491 Segment Drivers and the scan circuit directly-coupled to the MC3490 Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required as compared to 12 capacitors, if the strobed digit drivers were ac coupled.

The MC3491 and MC3492 have input clamp diodes allowing for dc restoration of the segment address pulse. These high voltage drivers (80 V) also feature programmable segment current by the selection of a single external resistor.

The MC3490 Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494 Anode Driver should be used.) The internal zener diode string of the MC3490 references the off drivers (and display anodes) to -50 V without the need of pull-down resistors.

Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Drivers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490's, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

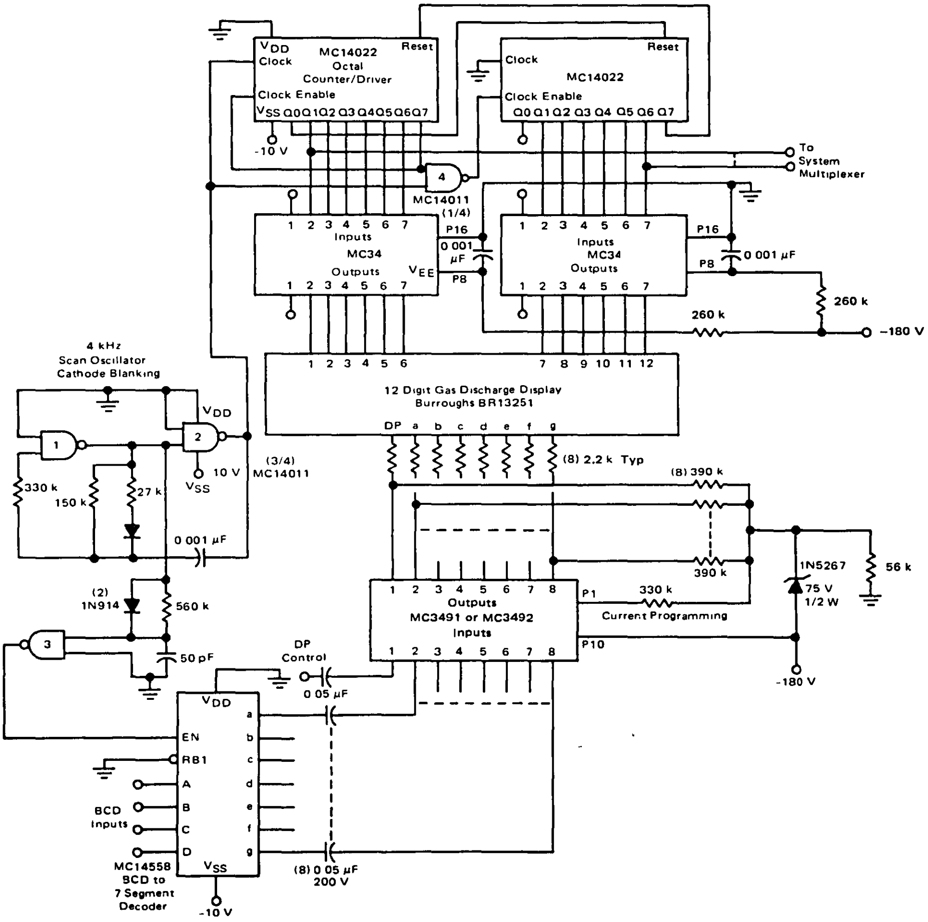
The MC14558 BCD-to-Seven Segment Decoder has an Enable input which readily provides for display cathode blanking. For the illustrated display, the cathode drivers should be turned off prior to anode switching and maintained off for some period after the next anode is strobed.

This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrated network and inverter Gate 3.

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 7 – 12-DIGIT CMOS GAS DISCHARGE DISPLAY SYSTEM



12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 or MC3492 cathode drivers and MC3494 anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6-digit clock display with multiplexed 7-segment outputs The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the MC3491 or MC3492. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494 anode driver.

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 kΩ resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

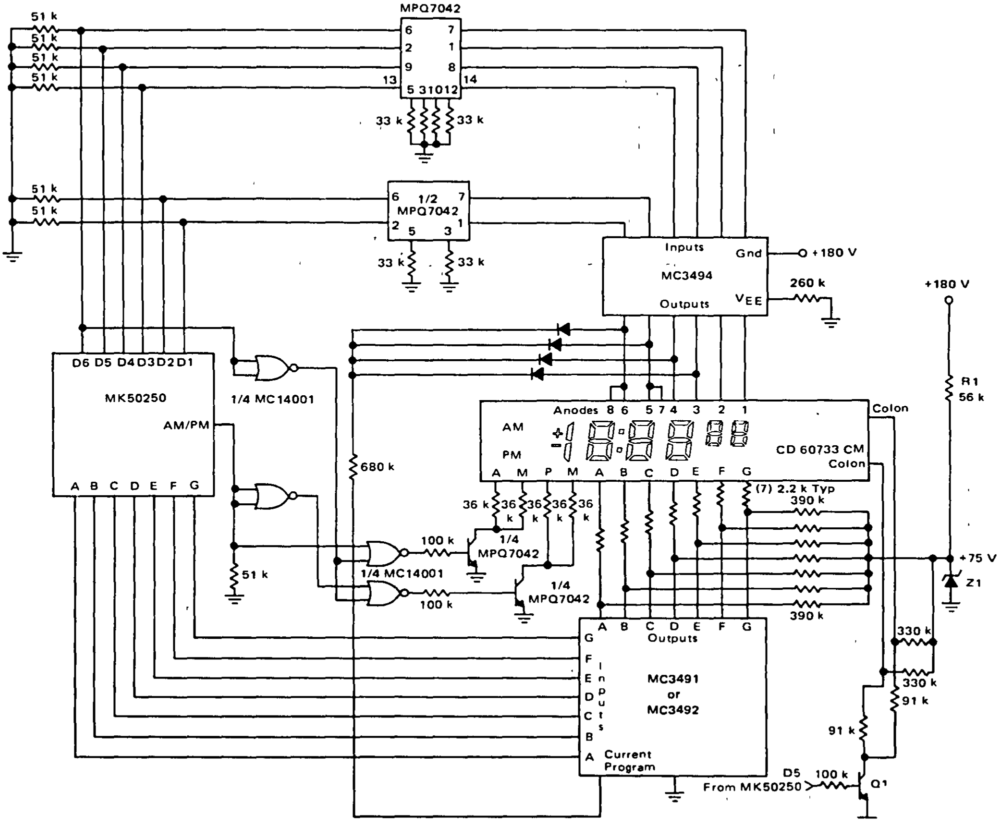
The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494 anode drivers. Inter-digit blanking is provided in the anode circuits Level translation from the clock chip output to the input to the MC3494 uses two MPQ7042 quad high voltage transistor packages operating in an emitter-follower current source mode. Each current source turns on one of the MC3494 drivers by sinking 300 μA to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has an 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection.

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 8 — 12-HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



MOTOROLA

MC75107
MC75108

DUAL LINE RECEIVERS

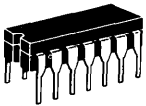
The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

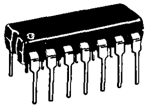
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

DUAL LINE RECEIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

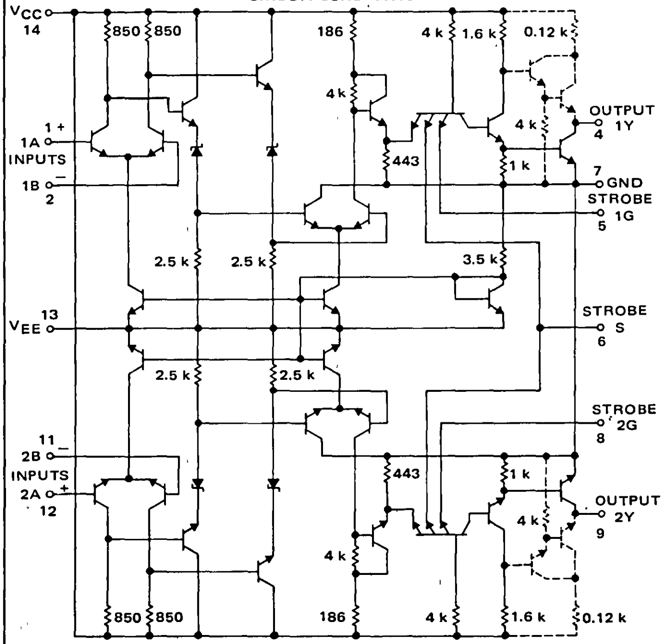


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

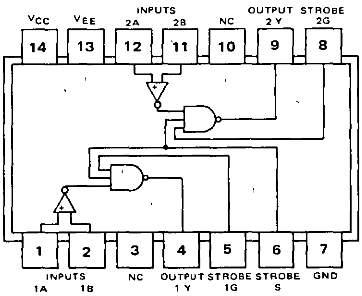


P SUFFIX
PLASTIC PACKAGE
CASE 646

CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC75107 only.



TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geqslant 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leqslant -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

MAXIMUM RATINGS (T_A = 0°C to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6 0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5 0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual-In-Line Packages Derate above T_A = +25°C		625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4 75 -4 75	+5 0 -5 0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}	–	–	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5 0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3 0	–	+3 0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5 0	–	+3 0	Vdc
Operating Temperature Range	T_A	0	–	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0 025	5 0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5 0†	-0 025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2 0	5 5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0 5 V, V_{IC} = -3 0 V to +3.0 V) ‡	I_{IH}	2	–	30	75	µA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = -2.0 V, V_{IC} = -3 0 V to +3 0 V) ‡	I_{IL}	2	–	–	-10	µA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0 4 V)‡	I_{IL}	4	–	–	-1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2 4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 80 2.0	 µA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-3 2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = -400 µA, V_{IC} = -3 0 V to +3 0 V)‡	V_{OH}	3	–	–	–	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = -3.0 V to +3.0 V)‡	V_{OL}	3	–	–	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max)‡	I_{CEX}	3	–	–	250	µA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max)‡	I_{OSC}	5	–	–	–	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) ‡	I_{CCH+}	6	–	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C)‡	I_{CCH-}	6	0	8.4	-15	mA

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5 0 V, T_A = +25°C.

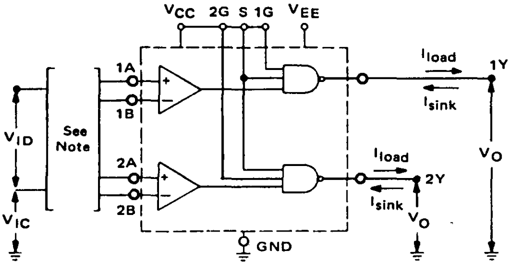
#Not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output	$t_{PLH(D)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	19	25	
Propagation Delay Time, high-to-low level from differential inputs A and B to output	$t_{PHL(D)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	19	25	
Propagation Delay Time, low-to-high level, from strobe input G or S to output	$t_{PLH(S)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	13	20	
Propagation Delay Time, high-to-low level, from strobe input G or S to output	$t_{PHL(S)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	13	20	

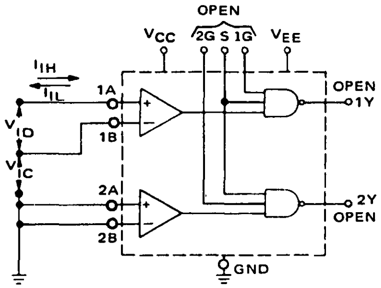
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



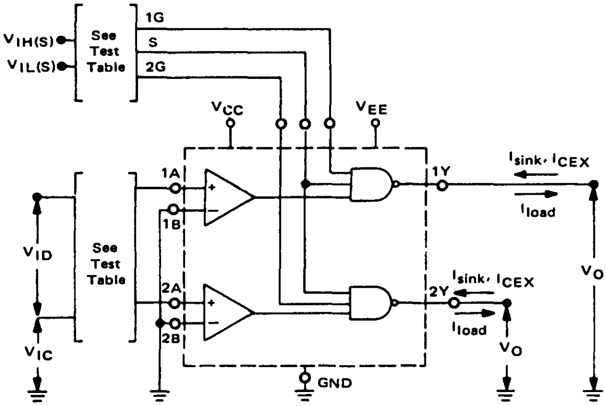
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}



TEST TABLE

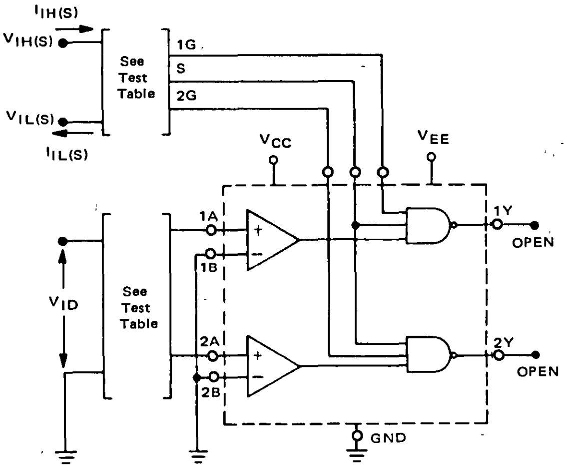
MC75107	MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES 1. V_{IC} = -3 0 V to +3 0 V.

2. When testing one channel, the inputs of the other channel should be grounded.

TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}

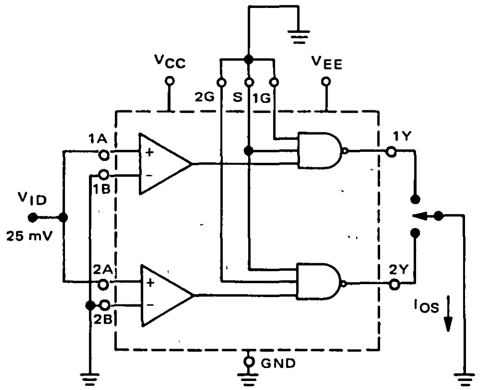
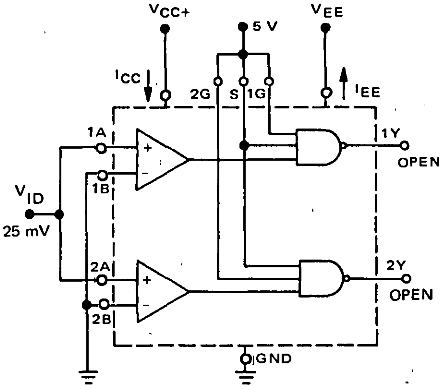


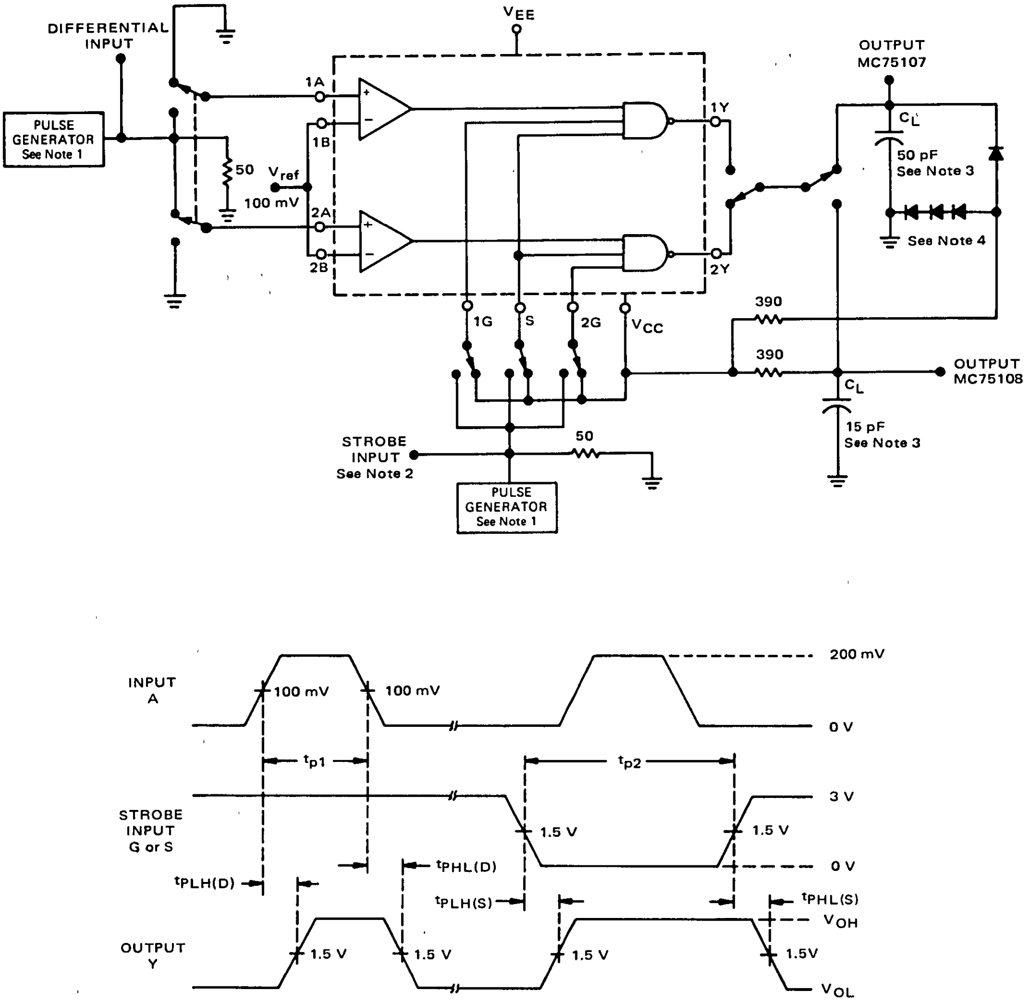
FIGURE 6 – I_{CC} and I_{EE}



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

TEST CIRCUITS (continued)

FIGURE 7 — PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1\ \mu s$, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

3. C_L includes probe and jig capacitance.

4. All diodes are 1N916 or equivalent.

MOTOROLA

MC75125
MC75127

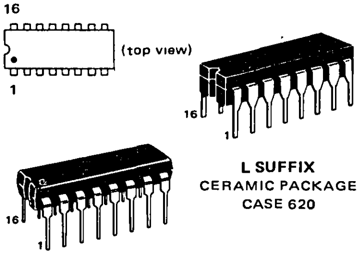
SEVEN CHANNEL LINE RECEIVERS

The MC75125 and MC75127 are seven-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The MC75125 and MC75127 are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance — 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on MC75127

SEVEN CHANNEL LINE RECEIVERS

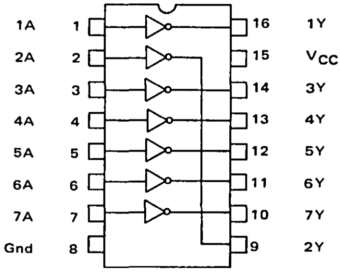


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

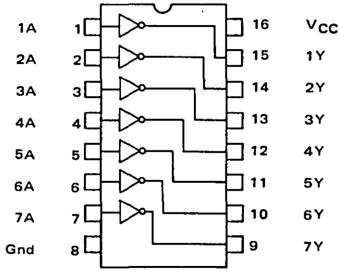
PIN CONNECTIONS

MC75125



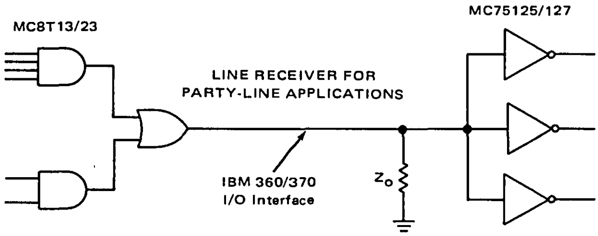
Logic: $Y = \overline{A}$

MC75127



Logic: $Y = \overline{A}$

TYPICAL APPLICATIONS
IBM 360/370 INTERFACE



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	-2.0 to +7.0	V
Power Dissipation (Package Limitation) Ceramic Package Plastic Package Derate Above T_A = 25°C	P_D $1/R_{\theta JA}$	1150 960 7.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	-0.4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	1.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.7	V
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = –0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0 5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V)	I_{IH}	0.2	0.3	0.42	mA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V)	I_{IL}	–	–	–0.24	mA
Short Circuit Output Current* (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	–18	–	–60	mA
Input Resistance (V_{CC} = 4 5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_I	7.4	–	20	kΩ
Power Supply Current Outputs High-Logic State (V_{CC} = 5.5 V, I_{OH} = –0.4 mA, all inputs at 0.7 V)	I_{CCH}	–	15	25	mA
Power Supply Current Outputs Low-Logic State (V_{CC} = 5.5 V, I_{OL} = 16 mA, all inputs at 4.0 V)	I_{CCL}	–	28	47	mA

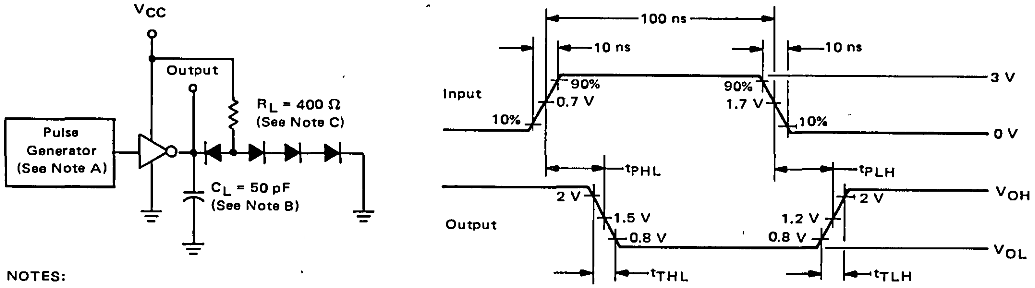
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted. See Figure 1)

		MC75125			MC75127			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Propagation Delay Time Low-to-High-Level Output High-to-Low-Level Output	 t_{PLH} t_{PHL}	 7.0 10	 14 18	 25 30	 7.0 10	 14 18	 25 30	ns
Ratio of Propagation Delay Times	t_{PLH}/t_{PHL}	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

*No more than one output should be shorted at a time.

FIGURE 1 — PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS

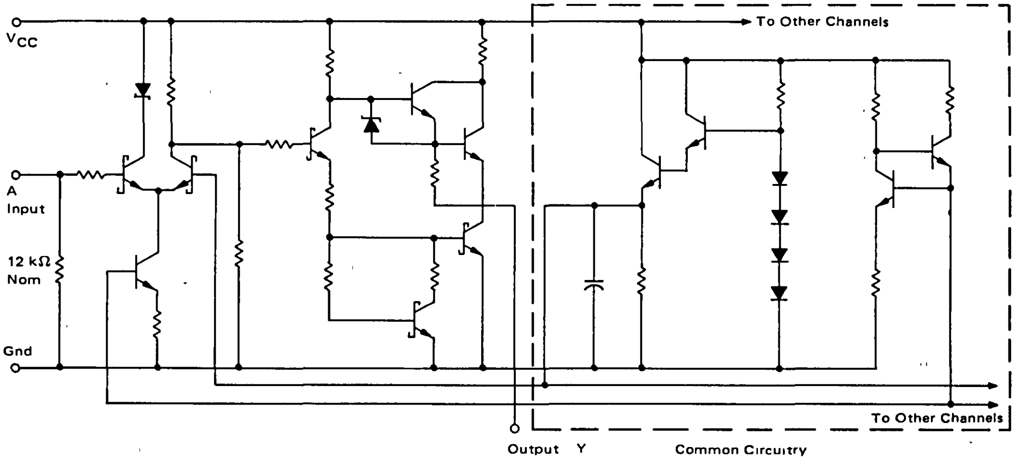
NOTES:

A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.

B. C_L includes probe and jig capacitance.

C. All diodes are MMD7000 or equivalent.

FIGURE 2 — SCHEMATIC (EACH RECEIVER)



TYPICAL CHARACTERISTICS

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

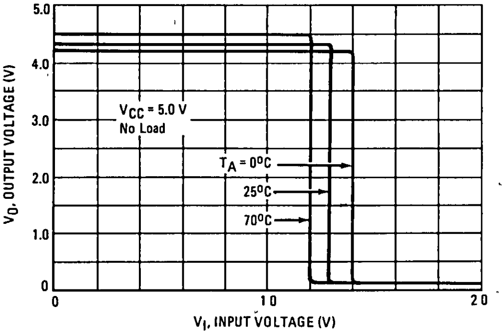


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

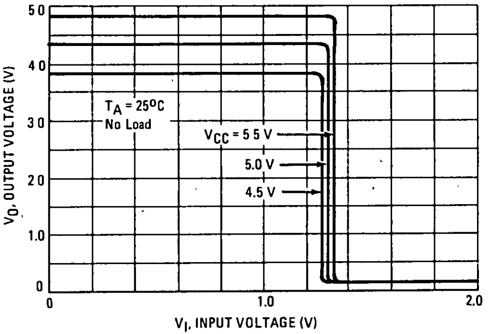


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

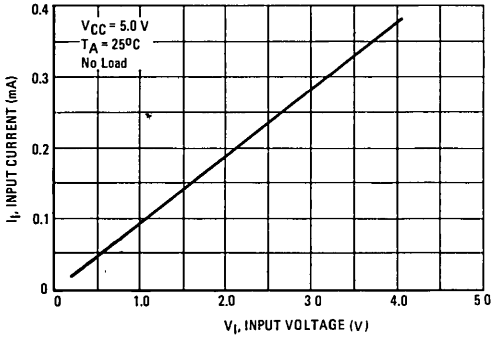


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

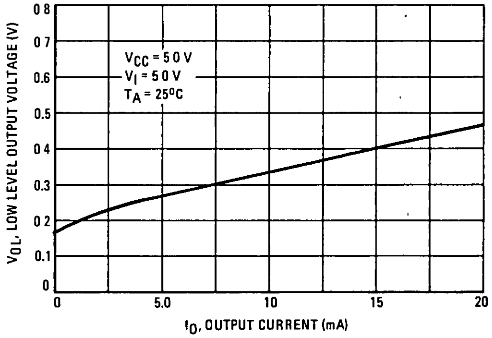
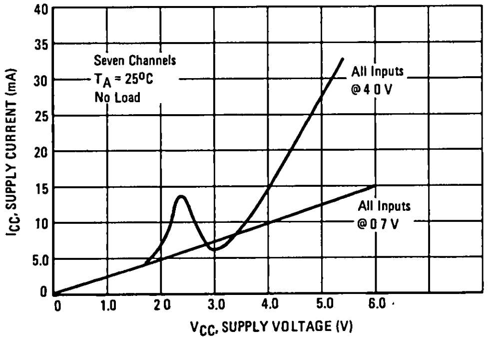


FIGURE 7 — SUPPLY CURRENT versus SUPPLY VOLTAGE



MC75128
MC75129

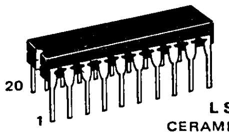
EIGHT-CHANNEL LINE RECEIVERS

EIGHT-CHANNEL LINE RECEIVERS

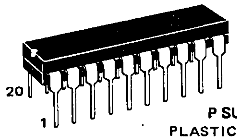
The MC75128 and MC75129 are eight-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The MC75128 has an active-high strobe; the MC75129 has an active-low strobe.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. Both devices are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance — 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- MC75128 Strobe — Active-High
  MC75129 Strobe — Active-Low



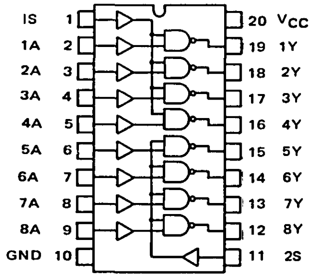
L SUFFIX
CERAMIC PACKAGE
CASE 732



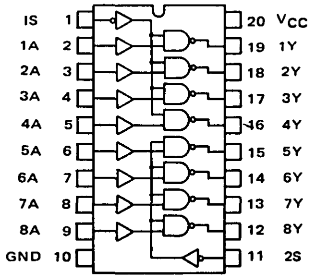
P SUFFIX
PLASTIC PACKAGE
CASE 738

PIN CONNECTIONS

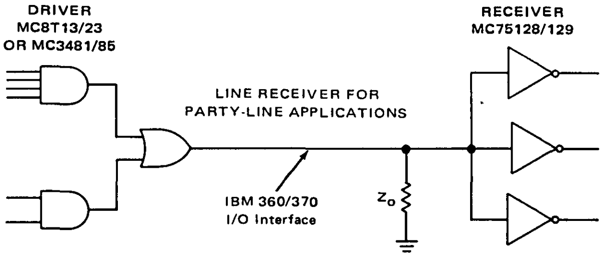
MC75128



MC75129



TYPICAL APPLICATIONS
IBM 360/370 INTERFACE



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
A Input Voltage	V_{IA}	−0.15 to +7.0	V
Strobe Input Voltage	V_{IS}	+7.0	V
Power Dissipation (Package Limitation) Ceramic Package Plastic Package Derate Above T_A = 25°C	P_D $1/R_{\theta JA}$	 1150 960 −7.7	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5 0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	−0 4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage A Inputs S Inputs	V_{IH}	 1.7 2.0	 – –	 – –	V
Low-Level Input Voltage A Inputs S Inputs	V_{IL}	 – –	 – –	 0.7 0.7	V
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0.5	V
Input Clamp Voltage (V_{CC} = 4.5 V, I_I = −18 mA, S Inputs)	V_{IK}	–	–	−1.5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V, A Inputs) (V_{CC} = 5.5 V, V_I = 2.7 V, S Inputs)	I_{IH}	– –	0.3 –	0.42 20	mA µA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V, A Inputs) (V_{CC} = 5.5 V, V_I = 0.4 V, S Inputs)	I_{IL}	– –	– –	−0.24 −0.4	mA
Short Circuit Output Current * (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	−18	–	−60	mA
Input Resistance (V_{CC} = 4.5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_I	7.0	–	20	kΩ
Power Supply Current — Outputs High-Logic State, all inputs at 0.7 V (V_{CC} = 5.5 V, Strobe at 2.4 V — MC75128) (V_{CC} = 5.5 V, Strobe at 0.4 V — MC75129)	I_{CCH}	 – –	 19 19	 31 31	mA
Power Supply Current — Outputs Low-Logic State, all inputs at 4.0 V (V_{CC} = 5.5 V, Strobe at 2.4 V — MC75128) (V_{CC} = 5.5 V, Strobe at 0.4 V — MC75129)	I_{CCL}	 – –	 32 32	 53 53	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted, See Figures 1 and 2)

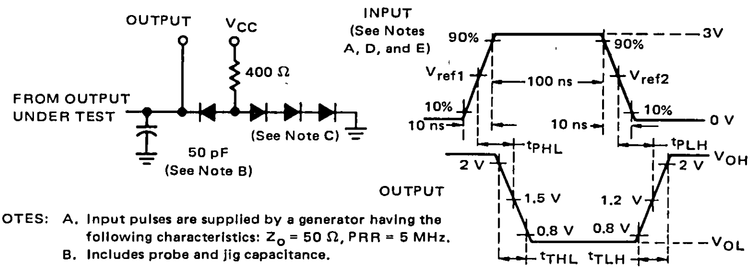
Characteristic	Symbol	MC75128			MC75129			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — From A Inputs Low-to-High-Level Output High-to-Low-Level Output	 $t_{PLH}(A)$ $t_{PHL}(A)$	 7.0 10	 14 18	 25 30	 7.0 10	 14 18	 25 30	ns
Propagation Delay Time — From S Inputs Low-to-High-Level Output High-to-Low-Level Output	 $t_{PLH}(S)$ $t_{PHL}(S)$	 – –	 26 22	 40 35	 – –	 20 16	 35 30	ns
Ratio of Propagation Delay Times — A Inputs	$t_{PLH}(A)/t_{PHL}(A)$	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low-Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

*No more than one output should be shorted at a time.

FIGURE 1 — PARAMETER MEASUREMENT INFORMATION

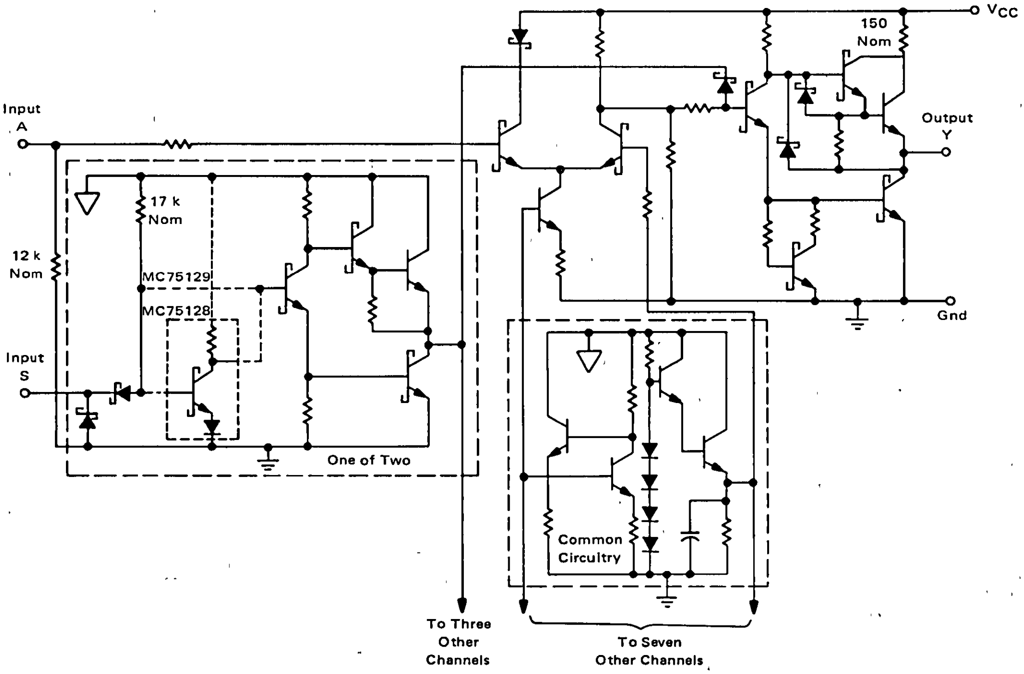
LOAD CIRCUIT

VOLTAGE WAVEFORMS



NOTES:
- A. Input pulses are supplied by a generator having the following characteristics: $Z_o = 50\ \Omega$, PRR = 5 MHz.
- B. Includes probe and jig capacitance.
- C. All diodes are MMD7000 or equivalent.
- D. The strobe inputs of MC75129 are in-phase with the output.
- E. $V_{ref1} = 0.7$ V and $V_{ref2} = 1.7$ V for testing data (A) inputs, $V_{ref1} = V_{ref2} = 1.3$ V for strobe inputs.

FIGURE 2 — SCHEMATIC (EACH RECEIVER)



TYPICAL CHARACTERISTICS

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

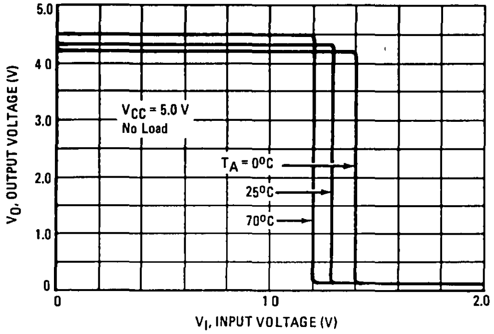


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

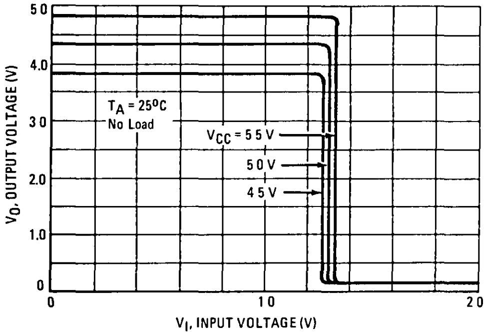


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

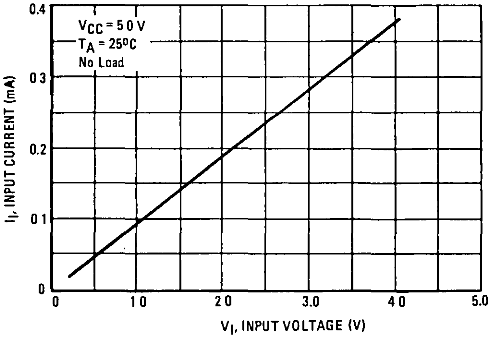
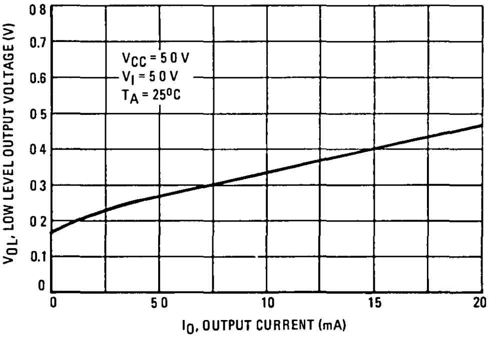


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT



MOTOROLA

MC75140P1

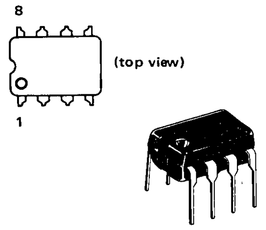
DUAL LINE RECEIVER

The MC75140P1 is a dual line receiver with common Strobe and Reference inputs. The Reference voltage is externally applied. This voltage may range from 1.5 to 3.5 volts, thus allowing for adjustment of maximum noise immunity in a given system design. The MC75140P1 is intended for use as a single-ended receiver in MTTL systems. Use in a party-line (bus-organized) system is aided by the low input current of the receiver.

- Single +5.0-Volts Power Supply
- ±100-mV Sensitivity
- Low Input Current
- MTTL Compatible Outputs
- Adjustable Reference Voltage
- Common Output Strobe

DUAL LINE RECEIVER

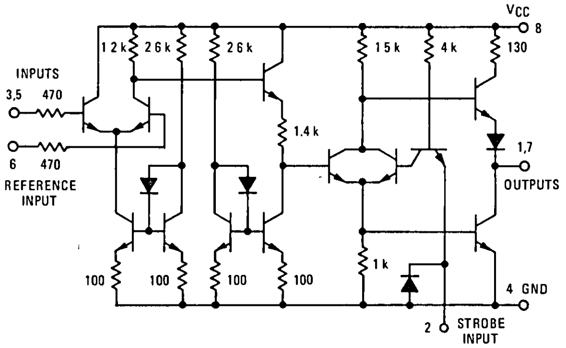
SILICON MONOLITHIC INTEGRATED CIRCUIT



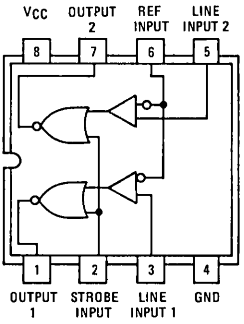
PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC

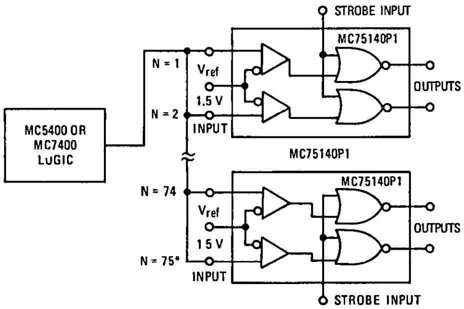
(1/2 Circuit Shown)



PIN CONNECTIONS



TYPICAL APPLICATION
HIGH FAN-OUT FROM A STANDARD MTTL GATE



*Most MC5400/MC7400 devices are capable of maintaining a 2.4-volt level under loads up to 7.5 mA

FUNCTION TABLE

LINE INPUT	STROBE	OUTPUT
V_{ref} − 100 mV	L	H
V_{ref} + 100 mV	X	L
X	H	L

Positive Logic
H = High Level, L = Low Level,
X = Nonsignificant

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7 0	Volts
Reference Voltage	V_{ref}	5.5	Volts
Line Input Voltage (with respect to Ground)	$V_{I(L)}$	-2.0 to +5.5	Volts
Line Input Voltage (with respect to V_{ref})	$V_{I(L)}-V_{ref}$	±5.0	Volts
Strobe Input Voltage	$V_{I(S)}$	5 5	Volts
Power Dissipation (Package Limitation)	P_D		
Plastic Dual In-Line Package		830	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Nom	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts
Reference Voltage Range	$V_{ref\ R}$	1.5	–	3.5	Volts
Input Voltage Range (Line or Strobe)	V_{IR}	0	–	5.5	Volts
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 0 V ±10%, V_{ref} = 1.5 to 3.5 V, T_A = 0 to +70°C unless otherwise noted.)

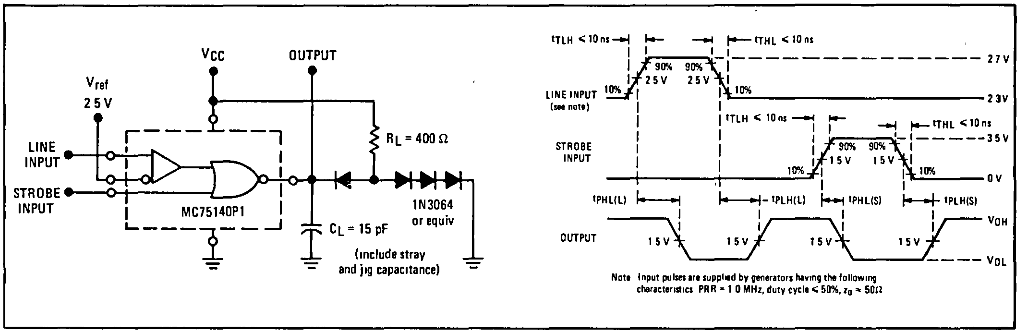
Characteristic	Symbol	Min	Typ*	Max	Unit
High-Level Line Input Voltage	$V_{IH(L)}$	V_{ref} + 100	–	–	mV
Low-Level Line Input Voltage	$V_{IL(L)}$	–	–	V_{ref} - 100	mV
High-Level Strobe Input Voltage	$V_{IH(S)}$	2 0	–	–	Volts
Low-Level Strobe Input Voltage	$V_{IL(S)}$	–	–	0 8	Volt
High-Level Output Voltage	V_{OH}				Volts
$V_{IL(L)} = V_{ref}$ - 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = -400 µA		2.4	–	–	
Low-Level Output Voltage	V_{OL}				Volt
$V_{IH(L)} = V_{ref}$ + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA		–	–	0.4	
$V_{IL(L)} = V_{ref}$ - 100 mV, $V_{IH(S)}$ = 2 0 V, I_{OL} = 16 mA		–	–	0 4	
Strobe Input Clamp Voltage	$V_{I(S)}$				Volts
$I_{I(S)}$ = -12 mA		–	–	-1.5	
Strobe Input Current (at max Input Voltage)	$I_{I(S)}$				mA
$V_{I(S)}$ = 5.5 V		–	–	2 0	
High-Level Input Currents					µA
Strobe ($V_{I(S)}$ = 2.4 V)	$I_{IH(S)}$	–	–	80	
Line ($V_{I(L)} = V_{CC}$, V_{ref} = 1.5 V)	$I_{IH(L)}$	–	35	100	
Reference (V_{ref} = 3.5 V, $V_{I(L)}$ = 1.5 V)	$I_{IH(ref)}$	–	70	200	
Low-Level Input Currents					
Strobe ($V_{I(S)}$ = 0.4 V)	$I_{IL(S)}$	–	–	-3.2	mA
Line ($V_{I(L)}$ = 0 V, V_{ref} = 1.5 V)	$I_{IL(L)}$	–	–	-10	µA
Reference (V_{ref} = 0 V, $V_{I(L)}$ = 1.5 V)	$I_{IL(ref)}$	–	–	-20	µA
Short-Circuit Output Current**	I_{OS}				mA
V_{CC} = 5.5 V		-18	–	-55	
Supply Current (output high)	I_{CCH}				mA
$V_{I(S)}$ = 0 V, $V_{I(L)} = V_{ref}$ - 100 mV		–	18	30	
Supply Current (output low)	I_{CCL}				mA
$V_{I(S)}$ = 0 V, $V_{I(L)} = V_{ref}$ + 100 mV		–	20	35	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, V_{ref} = 2.5 V, C_L = 15 pF, R_L = 400 Ω, T_A = +25°C unless otherwise noted.)
See Figure 1.

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (low-to-high level output from Line input)	$t_{PLH(L)}$	–	22	35	ns
Propagation Delay Time (high-to-low level output from Line input)	$t_{PHL(L)}$	–	22	30	ns
Propagation Delay Time (low-to-high level output from Strobe input)	$t_{PLH(S)}$	–	12	22	ns
Propagation Delay Time (high-to-low level output from Strobe input)	$t_{PHL(S)}$	–	8.0	15	ns

*All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
**Only one output should be shorted at a time.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Note Input pulses are supplied by generators having the following characteristics PRR = 1 0 MHz, duty cycle ≤ 50%, $z_0 \approx 50\Omega$

FIGURE 2 – OUTPUT VOLTAGE versus LINE INPUT VOLTAGE

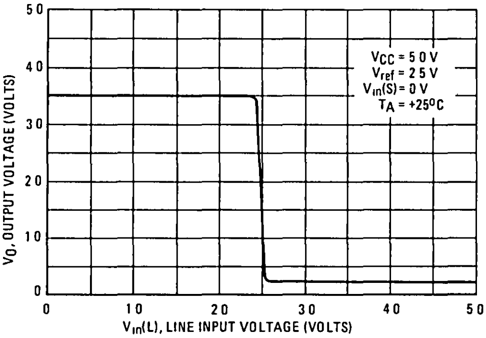


FIGURE 3 – SCHMITT TRIGGER

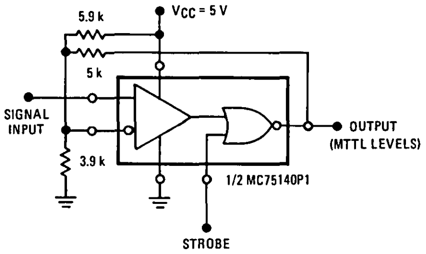


FIGURE 4 – TRANSFER CHARACTERISTICS FOR SCHMITT TRIGGER

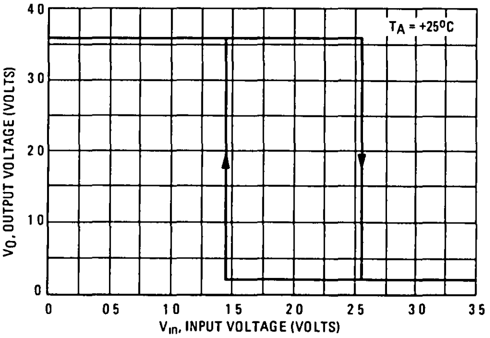


FIGURE 5 – GATED OSCILLATOR

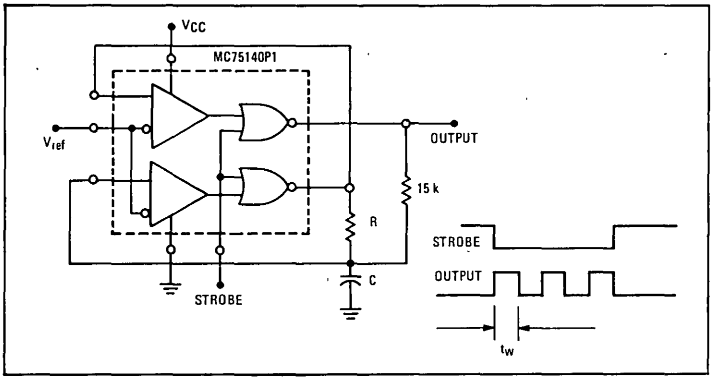


FIGURE 6 – GATE OSCILLATOR FREQUENCY versus RC TIME CONSTANT

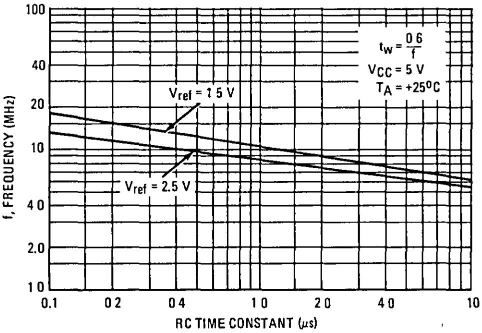
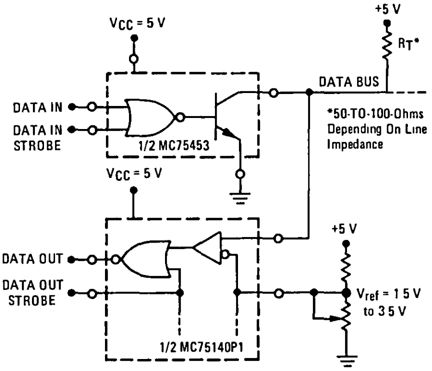


FIGURE 7 – DUAL BUS TRANSCEIVER



MOTOROLA

MC55325
MC75325

Specifications and Applications Information

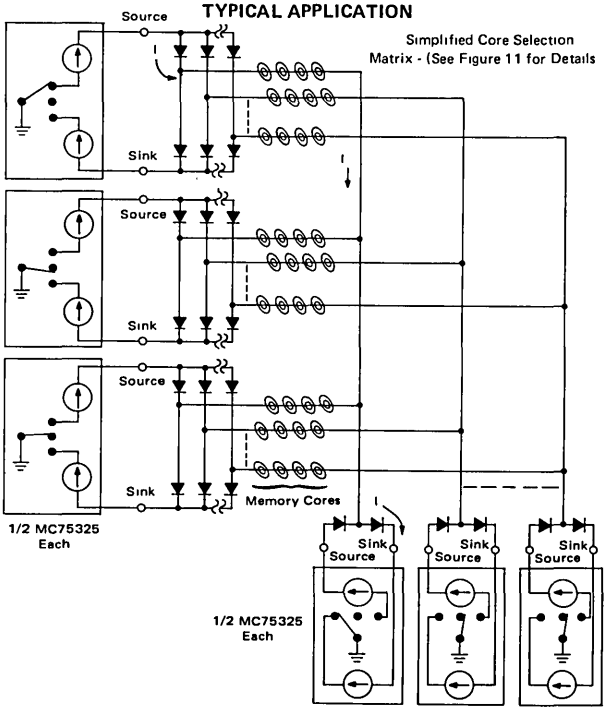
DUAL MEMORY DRIVER

The MC55325/75325 is a monolithic integrated circuit memory driver with logic inputs, and is designed for use with magnetic memories.

The device contains two 600-mA source-switch pairs and two 600-mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. With this arrangement selection of one of the four switches provides turn-on with minimum time skew of the output current rise.

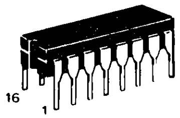
- 600-mA Output Capability
- Fast Switching Times
- Input Clamp Diodes
- Dual Sink and Dual Source Outputs
- MDTL and MTTL Compatibility
- 24-Volt Output Capability

TYPICAL APPLICATION

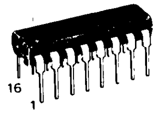


DUAL MEMORY DRIVER

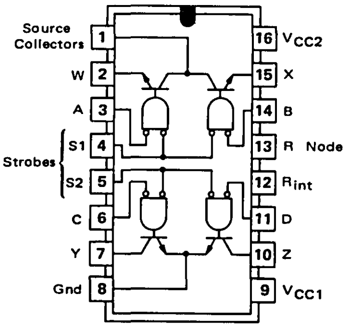
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC75325 only)



MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_{CC1} V_{CC2}	7.0 25	Vdc Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic and Plastic Packages		1.0	W
Derate above T_A = +25°C		6.6	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC55325		-55 to +125	
MC75325		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Voltage values are with respect to the network ground terminal.

TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	On	Off	Off	Off
H	L	X	X	L	H	Off	On	Off	Off
X	X	L	H	H	L	Off	Off	On	Off
X	X	H	L	H	L	Off	Off	Off	On
X	X	X	X	H	H	Off	Off	Off	Off
H	H	H	H	X	X	Off	Off	Off	Off

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

ELECTRICAL CHARACTERISTICS (T_A = T_{low} to T_{high} unless otherwise noted[1])

		MC55325			MC75325			
Characteristic	Symbol	Min	Typ[2]	Max	Min	Typ[2]	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	–	–	2.0	–	–	V
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	V
Input Clamp Voltage (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_I = -10 mA, T_A = 25°C)	V_I	–	-1.3	-1.7	–	-1.3	-1.7	V
Output Current — Off State (V_{CC1} = 4.5 V, V_{CC2} = 24 V)	I_{off}							µA
T_A = T_{low} to T_{high}		–	–	500	–	–	200	
T_A = 25°C		–	3.0	150	–	3.0	200	
Output Voltage — High Logic State (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_O = 0)	V_{OH}	19	23	–	19	23	–	V
Saturation Voltage[3]	V_{sat}							V
Source Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{source} ≈ -600 mA, R_L = 24 ohms, Note 4)								
T_A = T_{low} to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Sink Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{sink} ≈ 600 mA, R_L = 24 ohms, Note 4)								
T_A = T_{low} to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Input Current at Maximum Input Voltage (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 5.5 V)	I_I							mA
Address Inputs		–	–	1.0	–	–	1.0	
Strobe Inputs		–	–	2.0	–	–	2.0	
Input Current — High Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 2.4 V)	I_{IH}							µA
Address Inputs		–	3.0	40	–	3.0	40	
Strobe Inputs		–	6.0	80	–	6.0	80	
Input Current — Low Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 0.4 V)	I_{IL}							mA
Address Inputs		–	-1.0	-1.6	–	-1.0	-1.6	
Strobe Inputs		–	-2.0	-3.2	–	-2.0	-3.2	
Supply Current — Output Condition Off (V_{CC1} = 5.5 V, V_{CC2} = 24 V, T_A = 25°C)	$I_{CC(off)}$							mA
From V_{CC1}		–	14	22	–	14	22	
From V_{CC2}		–	7.5	20	–	7.5	20	
Supply Current from V_{CC1}, Either Sink "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{sink} = 50 mA, T_A = 25°C)	I_{CC1}	–	55	70	–	55	70	mA
Supply Current from V_{CC2}, Either Source "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{source} = -50 mA, T_A = 25°C)	I_{CC2}	–	32	50	–	32	50	mA

(1) T_{low} = -55°C for MC55325, 0°C for MC75325
T_{high} = +125°C for MC55325, +70°C for MC75325

(2) All typical values are at T_A = 25°C

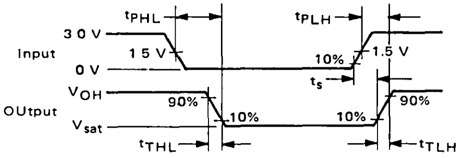
(3) Not more than one output is to be "on" at any one time.

(4) Saturation voltage must be measured using pulse techniques: Pulse Width = 200 µs, Duty Cycle ≤ 2%

SWITCHING CHARACTERISTICS (V_{CC1} = 5.0 V, C_L = 25 pF, T_A = 25°C)

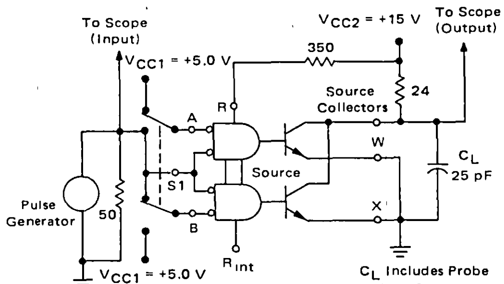
Characteristics	Symbol	MC55325/MC75325			Unit
		Min	Typ	Max	
Propagation Delay Time to Source Collectors					
(V_{CC2} = 15 V, R_L = 24 ohms) Low-to-High Level	t_{PLH}	–	25	50	ns
High-to-Low Level	t_{PHL}	–	25	50	ns
Transition Time					
(V_{CC2} = 20 V, R_L = 1 k ohms) Low-to-High Level	t_{TLH}	–	55	–	ns
High-to-Low Level	t_{THL}	–	70	–	ns
Propagation Delay Time to Sink Outputs					
(V_{CC2} = 15 V, R_L = 24 ohms) Low-to-High Level	t_{PLH}	–	20	45	ns
High-to-Low Level	t_{PHL}	–	20	45	ns
Transition Time					
(V_{CC2} = 15 V, R_L = 24 ohms) Low-to-High Level Output	t_{TLH}	–	7.0	15	ns
High-to-Low Level Output	t_{THL}	–	9.0	20	ns
Storage Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)	t_s	–	15	30	ns

FIGURE 1 – SWITCHING TIMES TO SOURCE COLLECTORS AND SINK OUTPUTS



Input Pulse Characteristics
z_o = 50Ω, Pulse Width = 200 ns,
t_{TLH} = t_{THL} ≤ 10 ns, Duty Cycle ≤ 1%

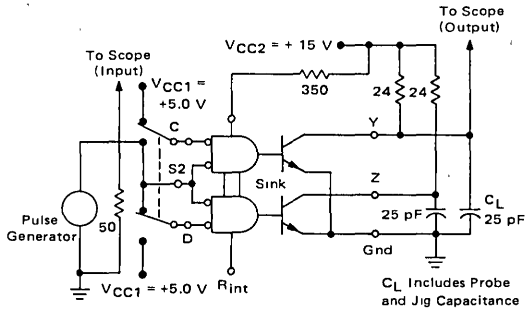
FIGURE 2 – PROPAGATION TIME TO SOURCE COLLECTORS



CL Includes Probe and Jig Capacitance

Source X Shown Under Test

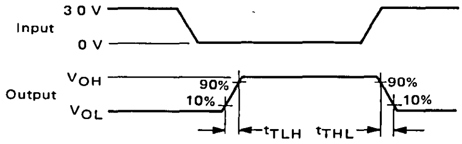
FIGURE 3 – PROPAGATION TIME, TRANSITION TIME AND STORAGE TIME TO SINK OUTPUTS



CL Includes Probe and Jig Capacitance

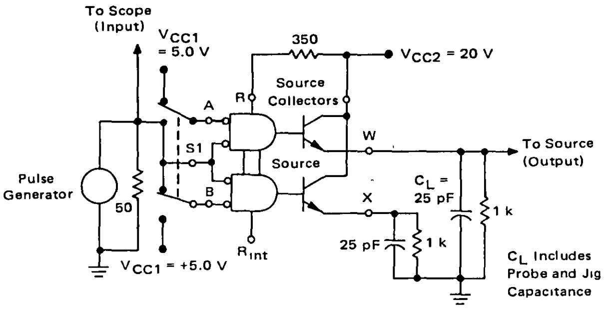
Sink Z Shown Under Test

FIGURE 4 – SWITCHING TIMES ON SOURCE OUTPUTS (See Figure 5)



Input Pulse Characteristics·
t_{THL} = t_{TLH} ≤ 10 ns, Duty Cycle ≤ 1%
Pulse Width = 200 ns

FIGURE 5 – TRANSITION TIME ON SOURCE OUTPUTS



Source X Shown Under Test

TYPICAL PERFORMANCE CURVES

FIGURE 6 – SOURCE COLLECTOR CURRENT (Off-State) versus AMBIENT TEMPERATURE

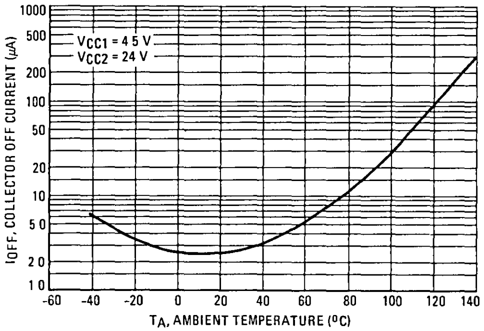


FIGURE 7 – SINK OUTPUT VOLTAGE-HIGH STATE V_{OH} versus AMBIENT TEMPERATURE

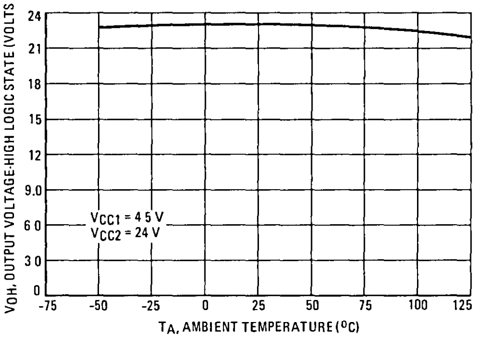


FIGURE 8 – SOURCE OR SINK SATURATION VOLTAGE versus AMBIENT TEMPERATURE

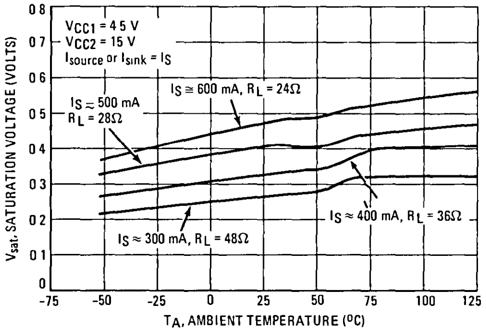
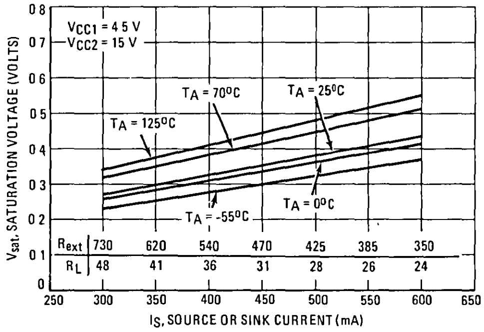


FIGURE 9 – SOURCE OR SINK SATURATION VOLTAGE versus SOURCE OR SINK CURRENT



APPLICATIONS INFORMATION

BASE DRIVE RESISTOR

An internal 575 Ω resistor connected between the V_{CC2} and the R_{int} terminals is provided in the MC55325/75325 to supply sufficient base drive for source currents to 375 mA at V_{CC2} of 15 Volts or 600 mA at V_{CC2} of 24 Volts. Connecting the R node to the R_{int} node selects this internal resistor. If source currents greater than 375 mA are required, the R_{int} node should be left open and an appropriate resistor connected between V_{CC2} and the R node. This method allows source base drive currents regulated to typically within ± 5%. This has an added advantage of removing the power dissipated in the resistor from the IC package, allowing the device to source greater currents at a given junction temperature.

The value of the required external resistor in a particular memory application may be computed using the following equation:

$$R_{ext} = \frac{16\,(V_{CC2\,min} - V_S - 2.2)}{I_L - 1.6\,(V_{CC2\,min} - V_S - 2.9)} \qquad (1)$$

Where: R_{ext} = kΩ.
V_S = the source output voltage referred to ground.
I_L = mA.

During the load current pulse the power dissipated in the resistor, R_{ext} is

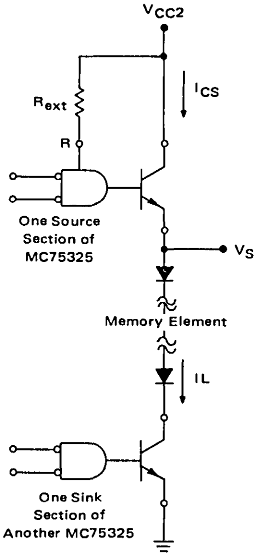
$$P_{R_{ext}} \approx \frac{I_L\,(V_{CC2\,min} - V_S - 2)}{16} \qquad (2)$$

Where: $P_{R_{ext}}$ = mW.

The source collector current I_{CS} is approximately 94% of total load current, I_L. The remaining current flows in the base of the source transistor through the external resistor R_{ext} or the source gate. See Figure 10 for added details.

An internal pull-up resistor in parallel with a clamping diode to V_{CC2} is provided at each sind-output collector to protect against voltage surges generated by switching reduction loads.

FIGURE 10 – TYPICAL CIRCUIT USED FOR R_{ext} CALCULATION



SELECTION MATRIX

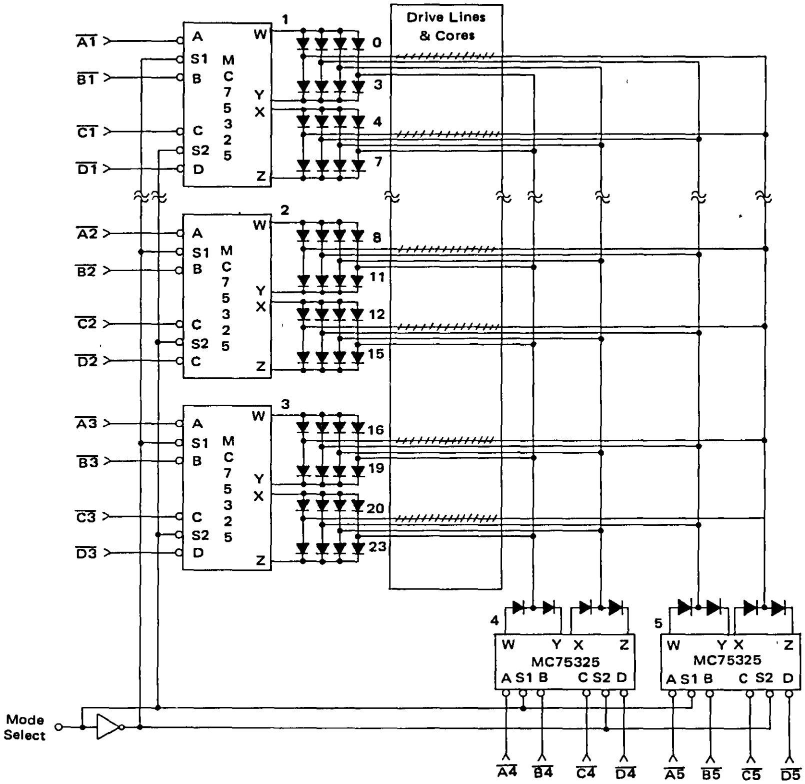
The combination of current source and sink pairs within the MC75325 is often utilized to implement a selection matrix for core memory systems. A typical, simplified system is shown in Figure 11.

The selection of any particular line (line 7, for example) is made by activating a particular, unique combination of two source/sink pairs. For an example, with the Mode Select input high and $\overline{B1}$ low, current source X of #1 MC75325 will be activated. This selects lines 4-7. When input C4 goes low, on #4 MC75325, current will flow through line 7 from source X (of device #1) to sink Y of device #4.

Changing the logic state of device #1 to input $\overline{D1}$ low, device #4 to input $\overline{A4}$ low, and applying a low to the Mode Select input, reverses the direction of the current in line 7 with the #1 MC75325 sinking the current and the #4 device sourcing it.

Drive line inductance and capacitance only limits the number of drive lines a source/sink pair can drive and thus the size of a matrix possible.

FIGURE 11 – TYPICAL APPLICATION - CORE MEMORY SELECTION MATRIX

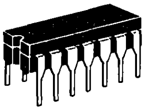


MOTOROLA

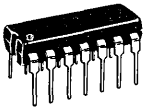
MC75450

DUAL PERIPHERAL POSITIVE "AND" DRIVER

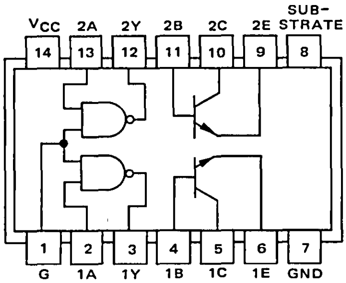
SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646



Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

DUAL PERIPHERAL POSITIVE "AND" DRIVER

The MC75450 is a versatile device designed for use as a general-purpose dual interface circuit in MDTL and MTTL type systems. This device features two standard MTTL gates and two noncommitted, high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

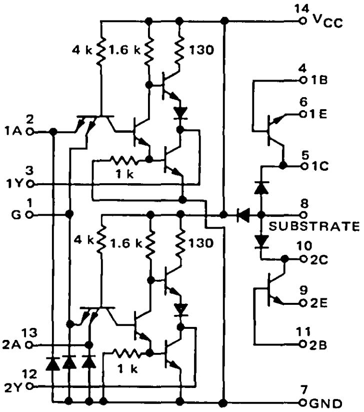
- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- Separate Gate and Output Transistor for Maximum Design Flexibility
- High Output Breakdown Voltage: V_{CER} = 30 Volts minimum

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Note 1)	V_{in}	5.5	Vdc
V_{CC}-to-Substrate Voltage		35	Vdc
Collector-to-Substrate Voltage		35	Vdc
Collector-Base Voltage	V_{CB}	35	Vdc
Collector-Emitter Voltage (See Note 2)	V_{CE}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current (continuous) (See Note 3)		300	mA
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 ohms.
3. Both halves of these dual circuits may conduct the rated current simultaneously.

CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS (See Note 4)

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

Note 4. The substrate, pin 8, must always be at the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic		Symbol	Test Fig.	Min	Typ*	Max	Unit
MTTL GATES							
High-Level Input Voltage		V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage		V_{IL}	2	–	–	0.8	Vdc
High-Level Output Voltage		V_{OH}	2				Vdc
(V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = -400 μA)				2.4	3.3	–	
Low-Level Output Voltage		V_{OL}	1				Vdc
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 16 mA)				–	0.22	0.4	
High-Level Input Current		I_{IH}	3				
(V_{CC} = 5.25 V, V_{in} = 2.4 V)	Input A			–	–	40	μA
	Input G			–	–	80	
(V_{CC} = 5.25 V, V_{in} = 5.5 V)	Input A			–	–	1.0	mA
	Input G			–	–	2.0	
Low-Level Input Current		I_{IL}	4				mA
(V_{CC} = 5.25 V, V_{in} = 0.4 V)	Input A			–	–	-1.6	
	Input G			–	–	-3.2	
Short-Circuit Output Current**		I_{OS}	5				mA
(V_{CC} = 5.25 V)				-18	–	-55	
Supply Current			6				mA
High-Level Output (V_{CC} = 5.25 V, V_{in} = 0)		I_{CCH}		–	2.0	4.0	
Low-Level Output (V_{CC} = 5.25 V, V_{in} = 5.0 V)		I_{CCL}		–	6.0	11	
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)		V_{in}	4	–	–	-1.5	V

OUTPUT TRANSISTORS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	V_{CBO}				Vdc
(I_C = 100 μA, I_E = 0)		35	–	–	
Collector-Emitter Breakdown Voltage	V_{CER}				Vdc
(I_C = 100 μA, R_{BE} = 500 ohms)		30	–	–	
Emitter-Base Breakdown Voltage	V_{EBO}				Vdc
(I_E = 100 μA, I_C = 0)		5.0	–	–	
Static Forward Transfer Ratio (See Note 5)	h_{FE}				
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = +25°C)		25	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = +25°C)		30	–	–	
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = 0°C)		20	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = 0°C)		25	–	–	
Base-Emitter Voltage (See Note 5)	V_{BE}				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.85	1.0	
(I_B = 30 mA, I_C = 300 mA)		–	1.05	1.2	
Collector-Emitter Saturation Voltage (See Note 5)	$V_{CE(sat)}$				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.25	0.4	
(I_B = 30 mA, I_C = 300 mA)		–	0.5	0.7	

Note 5. These parameters must be measured using pulse techniques; t_w = 300 μs, duty cycle ≤ 2%.

*All typical values at V_{CC} = 5.0 V, T_A = +25°C.

**Not more than one output should be shorted at a time.

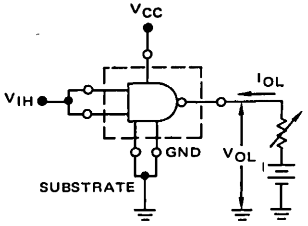
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
MTTL GATES						
Propagation Delay Time (C_L = 15 pF, R_L = 400 ohms)		7				ns
Low-to-High-Level Output	t_{PLH}		–	14	–	
High-to-Low-Level Output	t_{PHL}		–	6.0	–	
OUTPUT TRANSISTORS #						
Switching Times (I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1.0 V, C_L = 15 pF, R_L = 50 ohms)		8				ns
Delay Time	t_d		–	9.0	–	
Rise Time	t_r		–	11	–	
Storage Time	t_s		–	14	–	
Fall Time	t_f		–	8.0	–	
GATES AND TRANSISTORS COMBINED #						
Propagation Delay Time (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{PLH}		–	21	–	
High-to-Low Level Output	t_{PHL}		–	16	–	
Transition Time# (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{TLH}		–	7.0	–	
High-to-Low-Level Output	t_{THL}		–	8.0	–	

=Voltage and current values are nominal, exact values vary slightly with transistors parameters

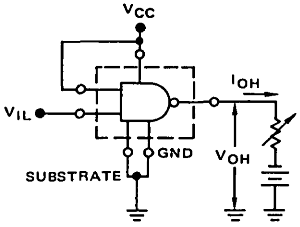
DC TEST CIRCUITS FOR MTTL GATES

FIGURE 1 – V_{IH}, V_{OL}



Both inputs are tested simultaneously.

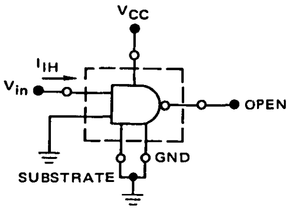
FIGURE 2 – V_{IL}, V_{OH}



Each input is tested separately.

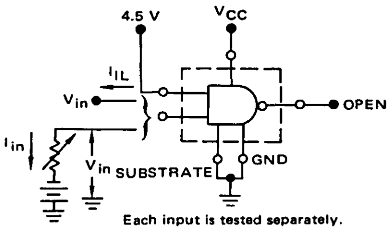
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 3 – I_{IH}



Each input is tested separately.

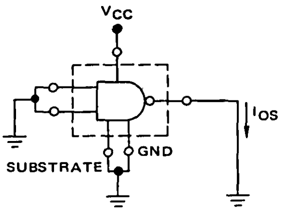
FIGURE 4 – I_{IL}, V_{in}



Each input is tested separately.

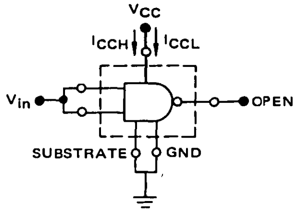
DC TEST CIRCUITS FOR MTTL GATES (continued)

FIGURE 5 – I_{OS}



Each gate is tested separately

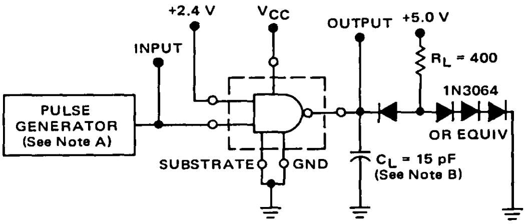
FIGURE 6 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

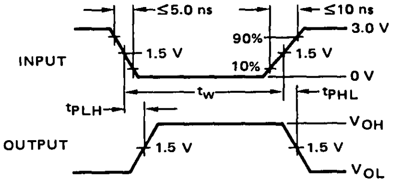
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 7 – PROPAGATION DELAY TIMES, EACH GATE



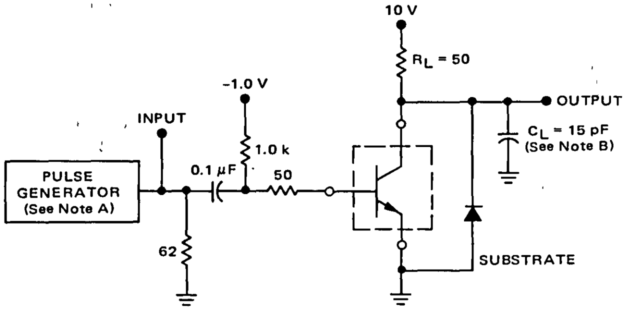
NOTES. A. The pulse generator has the following characteristics. t_W = 0 5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



TEST CIRCUITS (continued)

FIGURE 8 – SWITCHING TIMES, EACH TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.3 µs, duty cycle ≤ 1%, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

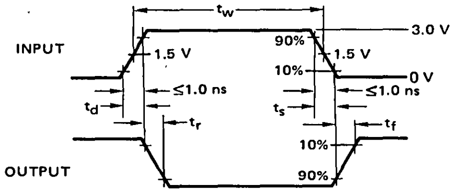
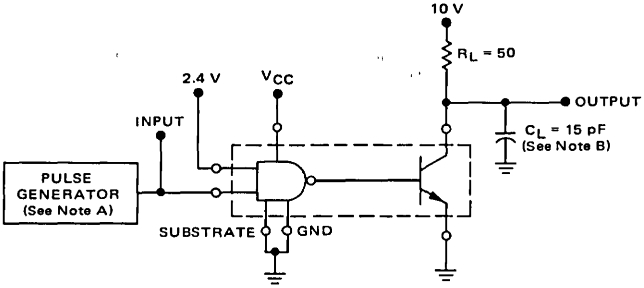
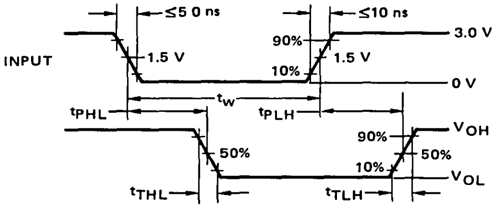


FIGURE 9 – SWITCHING TIMES, GATE AND TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 µs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



MOTOROLA

MC75451
MC75452
MC75453
MC75454

DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

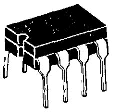
Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

MC75451 provides the AND function
MC75452 provides the NAND function
MC75453 provides the OR function
MC75454 provides the NOR function

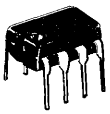
- 300 mA Output Current Capability
- Output Breakdown Voltage – 30 V Min
- MTTL compatible Inputs

DUAL PERIPHERAL DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

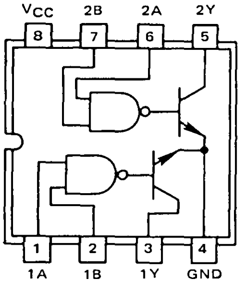


U SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

MC75451 – Positive AND



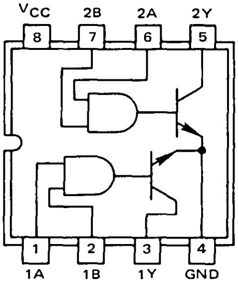
Positive Logic Y = AB

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level

MC75452 – Positive NAND



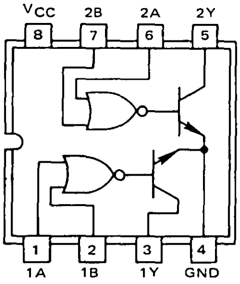
Positive Logic· Y = $\overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

MC75453 – Positive OR



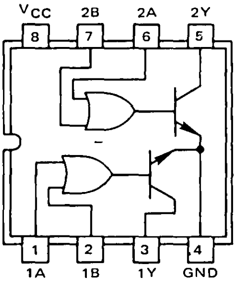
Positive Logic· Y = A + B

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level

MC75454 – Positive NOR



Positive Logic Y = $\overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7.0	Vdc
Input Voltage	V_I	5 5	Vdc
Interemitter Voltage(2)	–	5.5	Vdc
Output Voltage(3)	V_O	30	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ T_A = 25°C Derate above T_A = +25°C	P_D	830 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Voltage values are with respect to network ground terminal.

(2) This is the voltage between two emitters of a multiple-emitter transistor.

(3) This is the maximum voltage which should be applied to any output when it is in the "off" state.

(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

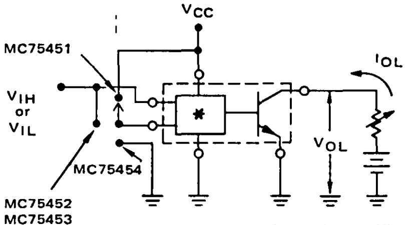
Characteristic	Figure	Symbol	Min	Typ (1)	Max	Unit
Input Voltage — High Logic State	1,2	V_{IH}	2.0	–	–	Vdc
Input Voltage — Low Logic State	1,2	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_I = -12 mA)	4	V_I	–	-1.2	-1.5	Vdc
Output Current — High Logic State (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IH} = 2 0 V) MC75451, MC75453 (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IL} = 0.8 V) MC75452, MC75454	2	I_{OH}	–	–	100	µA
Output Voltage — Low Logic State (V_{CC} = 4.75 V, V_{IL} = 0.8 V) MC75451, MC75453 (V_{CC} = 4.75 V, V_{IH} = 2.0 V) MC75452, MC75454 (I_{OL} = 100 mA) (I_{OL} = 300 mA)	1	V_{OL}	 – –	 0.25 0.5	 0.4 0.7	Vdc
Input Current — High Logic State (V_{CC} = 5 25 V, V_I = 2.4 V) (V_{CC} = 5.25 V, V_I = 5.5 V)	3	I_{IH}	 – –	 – –	 40 1.0	 µA mA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_I = 0.4 V)	4	I_{IL}	–	-1.0	-1.6	mA
Power Supply Current — Output High Logic State (V_{CC} = 5.25 V, V_I = 5 0 V) MC75451 (V_{CC} = 5.25 V, V_I = 0) MC75452 (V_{CC} = 5.25 V, V_I = 5.0 V) MC75453 (V_{CC} = 5.25 V, V_I = 0) MC75454	5	I_{CCH}	 – – – –	 7.0 11 8 0 13	 11 14 11 17	mA
Power Supply Current — Output Low Logic State (V_{CC} = 5 25 V, V_I = 0) MC75451 (V_{CC} = 5 25 V, V_I = 5 0 V) MC75452 (V_{CC} = 5.25 V, V_I = 0) MC75453 (V_{CC} = 5.25 V, V_I = 5 0 V) MC75454	5	I_{CCL}	 – – – –	 52 56 54 61	 65 71 68 79	mA

(1) Typical Values Measured with V_{CC} = 5.0 V, T_A = 25°C.

TEST CIRCUITS

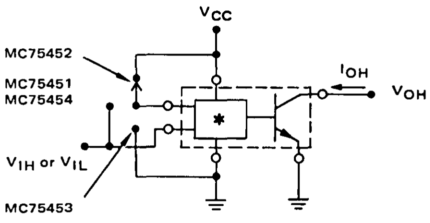
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL}, V_{IH} – MC75452 and MC75454 V_{IL} – MC75451 and MC75453



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH}, V_{IH} – MC75451 and MC75453 V_{IL} – MC75452 and MC75454



Each input is tested separately.

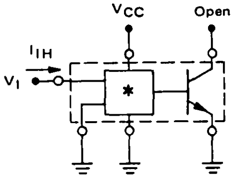
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
MC75451						
Low-to-High-Level Output	t_{PLH}	6	–	17	–	ns
High-to-Low-Level Output	t_{PHL}		–	18	–	
MC75452						
Low-to-High-Level Output	t_{PLH}	6	–	18	–	ns
High-to-Low-Level Output	t_{PHL}		–	16	–	
MC75453						
Low-to-High-Level Output	t_{PLH}	6	–	15	–	ns
High-to-Low-Level Output	t_{PHL}		–	17	–	
MC75454						
Low-to-High-Level Output	t_{PLH}	6	–	25	–	ns
High-to-Low-Level Output	t_{PHL}		–	19	–	
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
MC75451						
Low-to-High-Level Output	t_{TLH}	6	–	6.0	–	ns
High-to-Low-Level Output	t_{THL}		–	11	–	
MC75452						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	–	ns
High-to-Low-Level Output	t_{THL}		–	9.0	–	
MC75453						
Low-to-High-Level Output	t_{TLH}	6	–	5.0	–	ns
High-to-Low-Level Output	t_{THL}		–	8.0	–	
MC75454						
Low-to-High-Level Output	t_{TLH}	6	–	50	–	ns
High-to-Low-Level Output	t_{THL}		–	8.0	–	

TEST CIRCUITS (Continued)

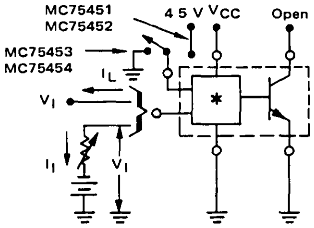
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 – I_{IH}
(ALL DEVICE TYPES)



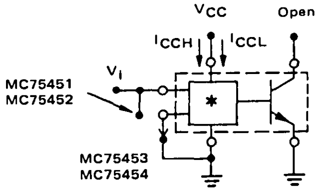
Each input is tested separately.

FIGURE 4 – I_{IL}, V_I
(ALL DEVICE TYPES)



Each input is tested separately.

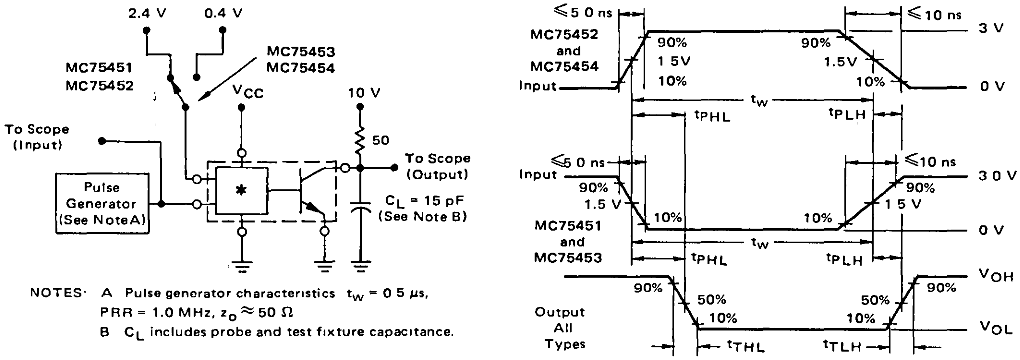
FIGURE 5 – I_{CCH}, I_{CCL}
(ALL DEVICE TYPES)



*See page 1 for specific gate type.

Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

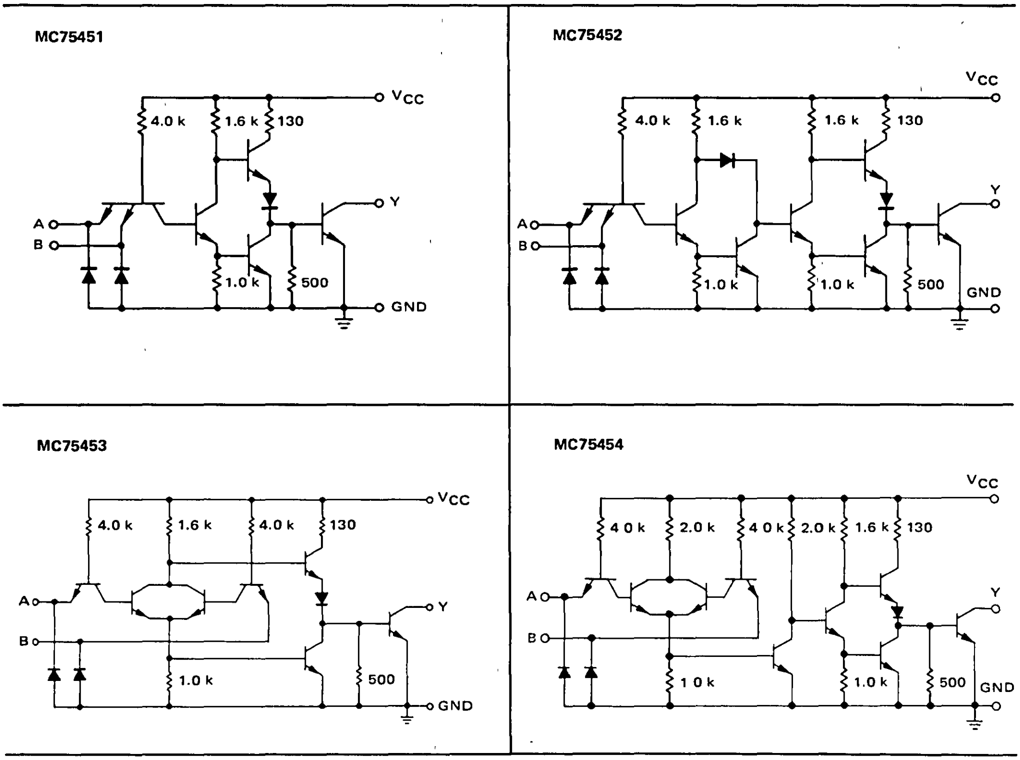


NOTES: A Pulse generator characteristics t_W = 0 5 μs, PRR = 1.0 MHz, $z_0 \approx 50\ \Omega$

B C_L includes probe and test fixture capacitance.

REPRESENTATIVE SCHEMATIC DIAGRAMS

(1/2 Circuits Shown)



MOTOROLA

MC75461
MC75462
MC75463
MC75464

DUAL HIGH-VOLTAGE PERIPHERAL DRIVERS

The MC75461 thru MC75464 series is similar to the MC75451 thru MC75454 series peripheral drivers; however, the MC75461 series features greater voltage capability allowing operation with higher output voltages or with inductive loads. These devices are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

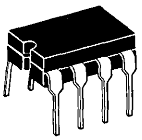
Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

MC75461 provides the AND function
MC75462 provides the NAND function
MC75463 provides the OR function
MC75464 provides the NOR function

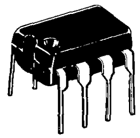
- 300 mA Output Current Capability
- No Output Latch-up at 30 V
- MTTL compatible Inputs

DUAL HIGH-VOLTAGE PERIPHERAL DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

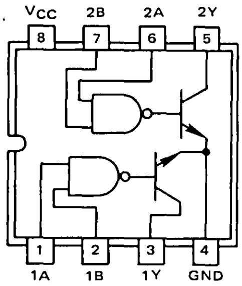


U SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

MC75461 – Positive AND



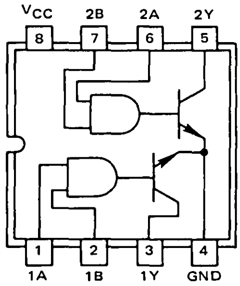
Positive Logic. Y = AB

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level

MC75462 – Positive NAND



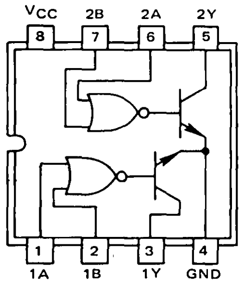
Positive Logic: Y = $\overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

MC75463 – Positive OR



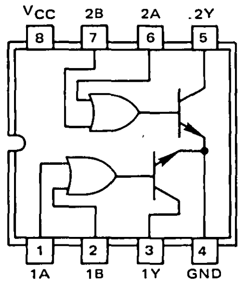
Positive Logic. Y = A + B

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level

MC75464 – Positive NOR



Positive Logic: Y = $\overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Interemitter Voltage(2)	–	5.5	Vdc
Output Voltage(3)	V_O	35	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ T_A = 25°C Derate above T_A = +25°C	P_D	830 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Voltage values are with respect to network ground terminal.
(2) This is the voltage between two emitters of a multiple-emitter transistor.
(3) This is the maximum voltage which should be applied to any output when it is in the "off" state.
(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

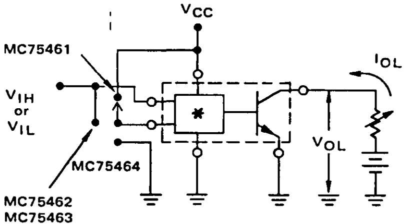
Characteristic		Figure	Symbol	Min	Typ(1)	Max	Unit
Input Voltage — High Logic State		1,2	V_{IH}	2.0	–	–	Vdc
Input Voltage — Low Logic State		1,2	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_I = -12 mA)		4	V_I	–	-1.2	-1.5	Vdc
Output Current — High Logic State		2	I_{OH}	–	–	100	µA
(V_{CC} = 4.75 V, V_{OH} = 35 V, V_{IH} = 2.0 V)	MC75461, MC75463						
(V_{CC} = 4.75 V, V_{OH} = 35 V, V_{IL} = 0.8 V)	MC75462, MC75464						
Output Voltage — Low Logic State		1	V_{OL}				Vdc
(V_{CC} = 4.75 V, V_{IL} = 0.8 V)	MC75461, MC75463						
(V_{CC} = 4.75 V, V_{IH} = 2.0 V)	MC75462, MC75464						
I_{OL} = 100 mA				–	0.15	0.4	
I_{OL} = 300 mA				–	0.35	0.7	
Input Current — High Logic State		3	I_{IH}				
(V_{CC} = 5.25 V, V_I = 2.4 V)				–	–	40	µA
(V_{CC} = 5.25 V, V_I = 5.5 V)				–	–	1.0	mA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_I = 0.4 V)		4	I_{IL}	–	-1.0	-1.6	mA
Power Supply Current — Output High Logic State		5	I_{CCH}				mA
(V_{CC} = 5.25 V, V_{IH} = 5.0 V)	MC75461			–	8.0	11	
(V_{CC} = 5.25 V, V_{IL} = 0)	MC75462			–	13	17	
(V_{CC} = 5.25 V, V_{IH} = 5.0 V)	MC75463			–	8.0	11	
(V_{CC} = 5.25 V, V_{IL} = 0)	MC75464			–	14	19	
Power Supply Current — Output Low Logic State		5	I_{CCL}				mA
(V_{CC} = 5.25 V, V_{IL} = 0)	MC75461			–	61	76	
(V_{CC} = 5.25 V, V_{IH} = 5.0 V)	MC75462			–	65	76	
(V_{CC} = 5.25 V, V_{IL} = 0)	MC75463			–	63	76	
(V_{CC} = 5.25 V, V_{IH} = 5.0 V)	MC75464			–	72	85	

(1) Typical Values Measured with V_{CC} = 5.0 V, T_A = 25°C

TEST CIRCUITS

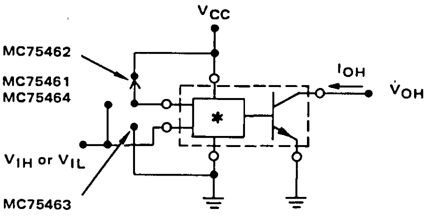
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL}
V_{IH} – MC75462 and MC75464
V_{IL} – MC75461 and MC75463



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH},
V_{IH} – MC75461 and MC75463
V_{IL} – MC75462 and MC75464



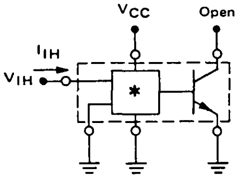
Each input is tested separately.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx 200$ mA, C_L = 15 pF, R_L = 50 ohms) MC75461						
Low-to-High-Level Output	t_{PLH}	6	–	45	55	ns
High-to-Low-Level Output	t_{PHL}		–	30	40	
MC75462						
Low-to-High-Level Output	t_{PLH}	6	–	50	65	ns
High-to-Low-Level Output	t_{PHL}		–	40	50	
MC75463						
Low-to-High-Level Output	t_{PLH}	6	–	45	55	ns
High-to-Low-Level Output	t_{PHL}		–	30	40	
MC75464						
Low-to-High-Level Output	t_{PLH}	6	–	50	65	ns
High-to-Low-Level Output	t_{PHL}		–	40	50	
Transition Time ($I_O \approx 200$ mA, C_L = 15 pF, R_L = 50 ohms) MC75461						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	20	ns
High-to-Low-Level Output	t_{THL}		–	10	20	
MC75462						
Low-to-High-Level Output	t_{TLH}	6	–	12	25	ns
High-to-Low-Level Output	t_{THL}		–	15	20	
MC75463						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	25	ns
High-to-Low-Level Output	t_{THL}		–	10	25	
MC75464						
Low-to-High-Level Output	t_{TLH}	6	–	12	20	ns
High-to-Low-Level Output	t_{THL}		–	15	20	
Output Voltage – High Logic Level after Switching (Latch-up Test) (V_S = 30 V $I_O \approx 300$ mA)	V_{OH}	7	V_S-10	–	–	mV

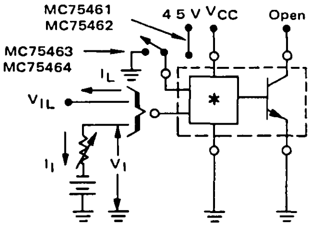
TEST CIRCUITS (Continued)
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 – I_{IH}
(ALL DEVICE TYPES)



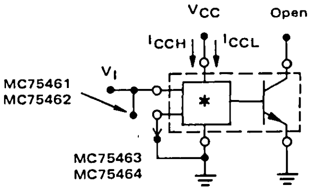
Each input is tested separately.

FIGURE 4 – I_{IL},V_I
(ALL DEVICE TYPES)



Each input is tested separately.

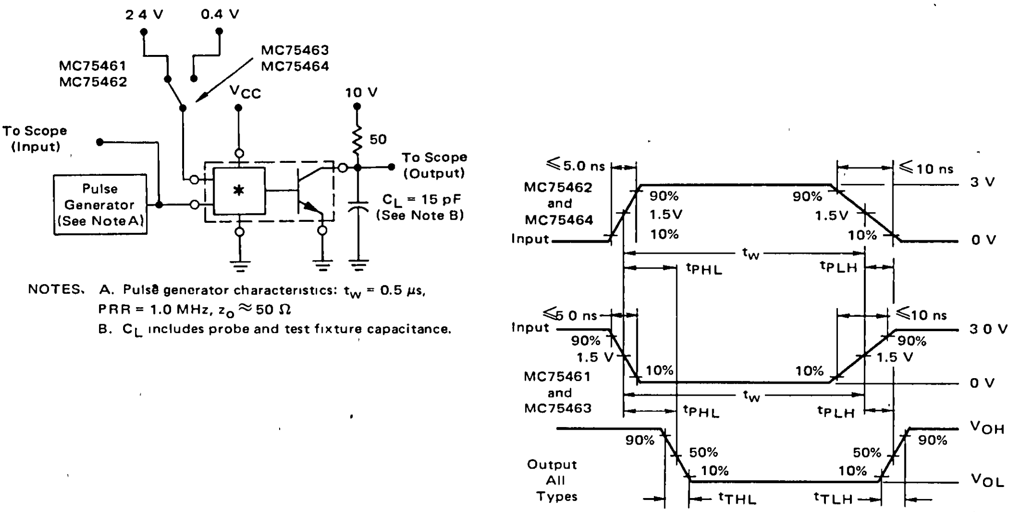
FIGURE 5 – I_{CCH}, I_{CCL}
(ALL DEVICE TYPES)



*See page 1 for specific gate type.

Both gates are tested simultaneously.

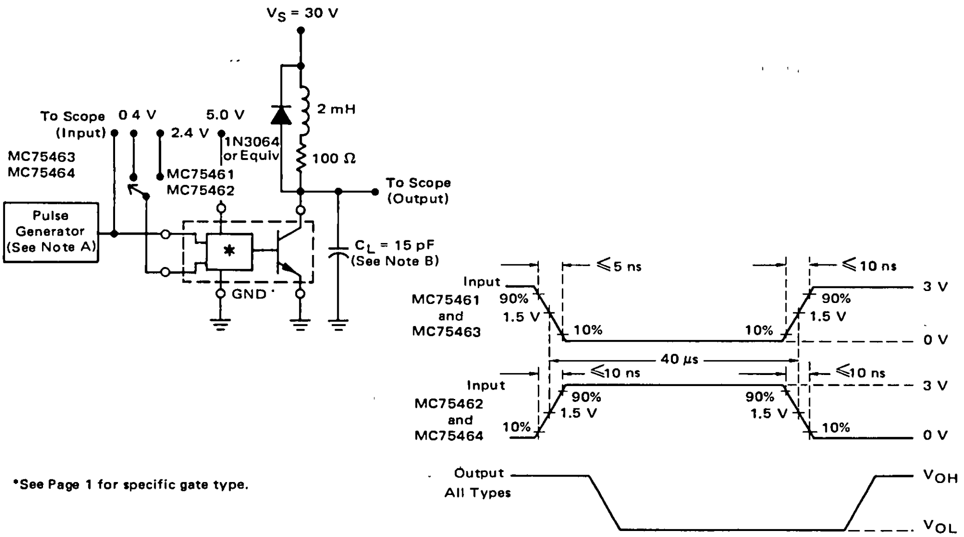
FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



NOTES. A. Pulse generator characteristics: t_w = 0.5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$

B. C_L includes probe and test fixture capacitance.

FIGURE 7 – OUTPUT VOLTAGE AFTER SWITCHING TEST CIRCUIT AND WAVEFORMS (LATCH-UP TEST)



*See Page 1 for specific gate type.

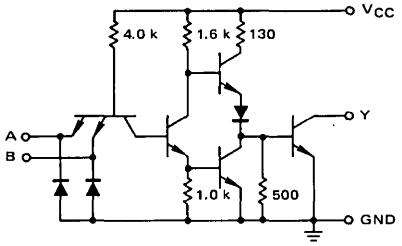
NOTES: A. The pulse generator has the following characteristics PRR = 12 5 kHz, Z_{out} = 50 Ω

B. C_L includes probe and jig capacitance.

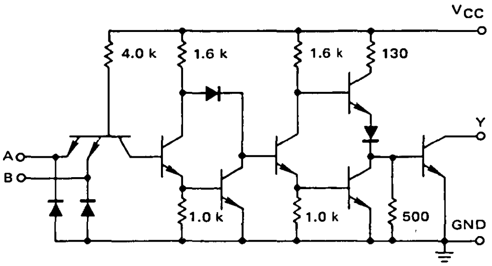
REPRESENTATIVE SCHEMATIC DIAGRAMS

(1/2 Circuits Shown)

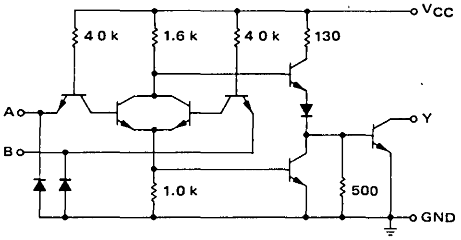
MC75461



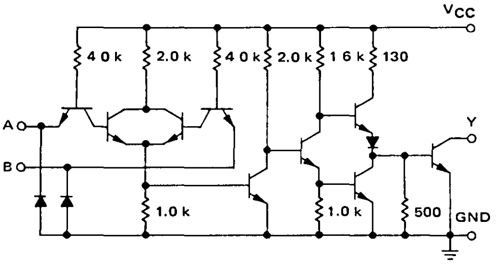
MC75462



MC75463



MC75464



MOTOROLA

MC75491
MC75492

Specifications and Applications Information

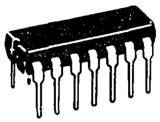
MULTIPLE LIGHT-EMITTING DIODE (LED) DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

QUAD LED SEGMENT DRIVER – MC75491
HEX LED DIGIT DRIVER – MC75492

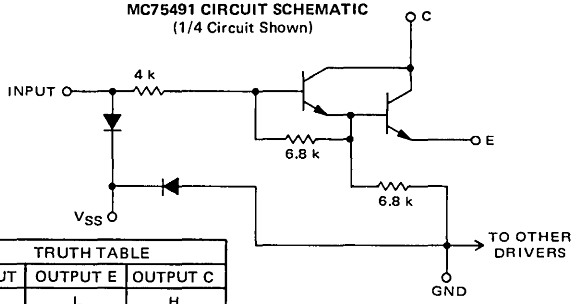
The MC75491 and MC75492 are designed to interface MOS logic to common cathode light-emitting diode readouts in serially addressed multi-digit displays. Using a segment address and digit scan LED drive method in a time multiplexing system results in a minimizing of the number of required drivers.

- Low Input Current Requirement for MOS Compatibility
- Low Standby Power Drain
- Source or Sink Current Capability of 50 mA for MC75491
- Sink Current Capability of 250 mA for MC75492
- Four High-Gain Darlington Drivers in a Single Package – MC75491
- Six High-Gain Darlington Drivers in a Single Package – MC75492



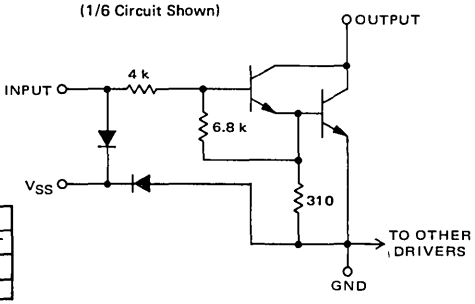
P SUFFIX
PLASTIC PACKAGE
CASE 646

MC75491 CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



TRUTH TABLE		
INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

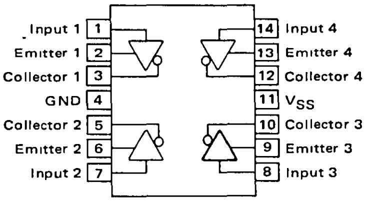
MC75492 CIRCUIT SCHEMATIC
(1/6 Circuit Shown)



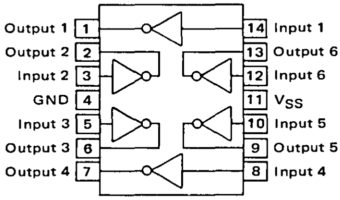
TRUTH TABLE	
INPUT	OUTPUT
L	H
H	L

CONNECTION DIAGRAMS

MC75491



MC75492



MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC75491	MC75492	
Bias Supply Voltage (See Note 1)	V_{SS}	10	10	Vdc
Input Voltage (See Note 2)	V_{in}	-5.0 to V_{SS}	-5.0 to V_{SS}	Vdc
Collector Voltage (See Note 3)	V_C	10	10	Vdc
Collector-to-Emitter Voltage	V_{CE}	10	–	Vdc
Collector-to-Input Voltage	V_{CI}	10	10	Vdc
Emitter Voltage ($V_{in} \geqslant 5.0$ Vdc)	V_E	10	–	Vdc
Emitter-to-Input Voltage	V_{EI}	5.0	–	Vdc
Continuous Collector Current (Each Collector) (All Collectors)	I_C	50 200	250 600	mA mA
Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6		 mW mW/°C
Operating Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150		°C

Note 1. V_{SS} terminal voltage is with respect to any other device terminal.

Note 2. With the exception of the inputs, the GND terminal must always be the most negative device voltage for proper operation.

Note 3. Voltage values are with respect to GND terminal unless otherwise noted.

ELECTRICAL CHARACTERISTICS (V_{SS} = 10 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	MC75491			MC75492			Unit
		Min	Typ	Max	Min	Typ	Max	
Low-Level Collector-to-Emitter Voltage (V_{in} = 8.5 V thru 1.0 kΩ, I_{OL} = 50 mA, V_E = 5.0 V)	V_{CEL}							Vdc
T_A = +25°C		–	0.9	1.2	–	–	–	
T_A = 0 to +70°C		–	–	1.5	–	–	–	
High-Level Collector Current	I_{CH}							µA
V_{CH} = 10 V, V_E = 0, I_{in} = 40 µA		–	–	100	–	–	–	
V_{CH} = 10 V, V_E = 0, V_{in} = 0.7 V		–	–	100	–	–	–	
Low-Level Output Voltage (V_{in} = 6.5 V thru 1.0 kΩ, I_{OL} = 250 mA)	V_{OL}							Vdc
T_A = +25°C		–	–	–	–	0.9	1.2	
T_A = 0 to +70°C		–	–	–	–	–	1.5	
High-Level Output Current	I_{OH}							µA
V_{OH} = 10 V, I_{in} = 40 µA		–	–	–	–	–	200	
V_{OH} = 10 V, V_{in} = 0.5 V		–	–	–	–	–	200	
Input Current at Maximum Input Voltage V_{in} = 10 V, I_{OL} = 20 mA	I_{in}	–	2.2	3.3	–	2.2	3.3	mA
Emitter Current – Reverse Bias I_C = 0, V_{in} = 0, V_E = 5.0 V	I_{ER}	–	–	100	–	–	–	µA
Bias Supply Current (V_{SS} = 10 V)	I_{SS}	–	–	1.0	–	–	1.0	mA

SWITCHING CHARACTERISTICS (V_{SS} = 7.5 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC75491			MC75492			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time, High-to-Low Level	t_{PHL}							ns
R_L = 200 Ω, V_{IH} = 4.5 V, C_L = 15 pF, V_E = 0		–	20*	–	–	–	–	
R_L = 39 Ω, V_{IH} = 7.5 V, C_L = 15 pF		–	–	–	–	40	–	
Propagation Delay Time, Low-to-High Level	t_{PLH}							ns
C_L = 15 pF, V_E = 0, R_L = 200 Ω, V_{IH} = 4.5 Vdc		–	40*	–	–	–	–	
C_L = 15 pF, R_L = 39 Ω, V_{IH} = 7.5 Vdc		–	–	–	–	80	–	

*To collector output.

TYPICAL CHARACTERISTICS

(V_{SS} = +10 Vdc, T_A = +25°C unless otherwise noted.)

MC75491

FIGURE 1 – COLLECTOR CURRENT versus INPUT VOLTAGE

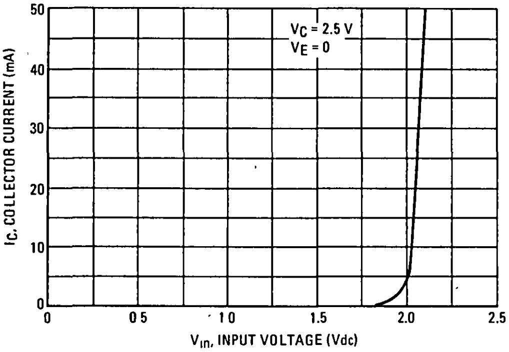


FIGURE 3 – COLLECTOR CURRENT versus INPUT CURRENT

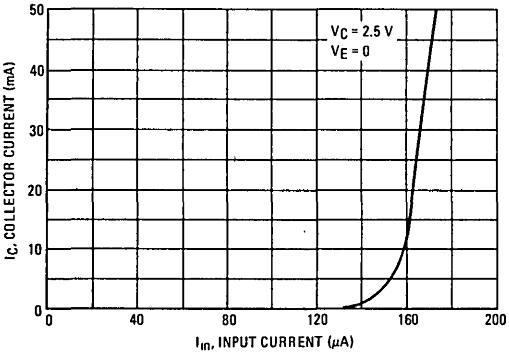
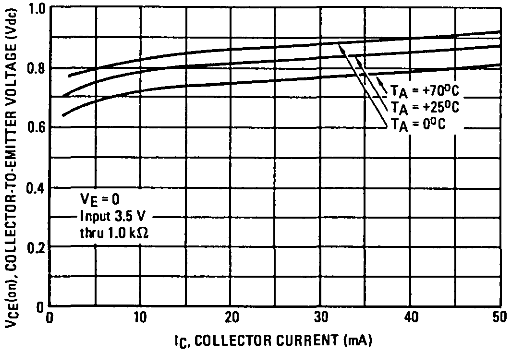


FIGURE 5 – COLLECTOR-TO-EMITTER VOLTAGE (ON) versus COLLECTOR CURRENT



MC75492

FIGURE 2 – OUTPUT CURRENT versus INPUT VOLTAGE

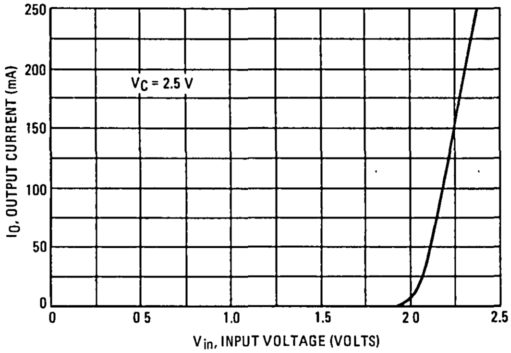


FIGURE 4 – OUTPUT CURRENT versus INPUT CURRENT

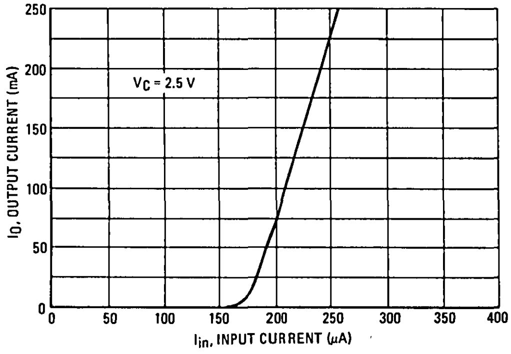
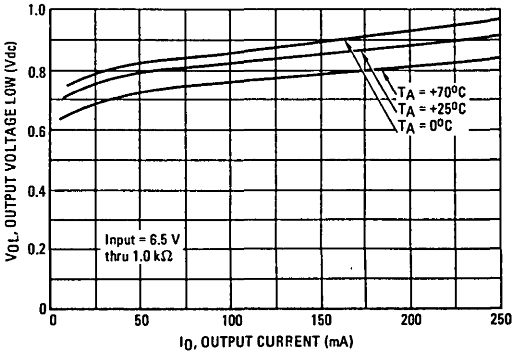


FIGURE 6 – OUTPUT VOLTAGE LOW versus OUTPUT CURRENT



TYPICAL CHARACTERISTICS and SWITCHING TIME CIRCUITS

FIGURE 7 – MC75491/MC75492 INPUT CURRENT versus INPUT VOLTAGE

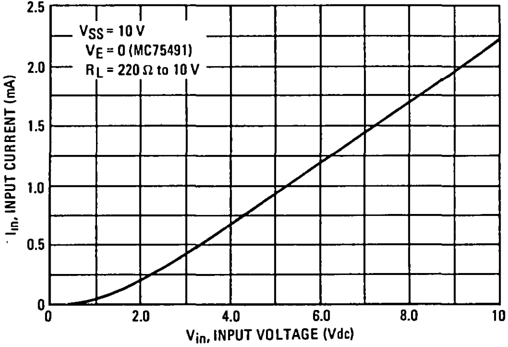


FIGURE 8 – MC75491 SWITCHING CIRCUIT

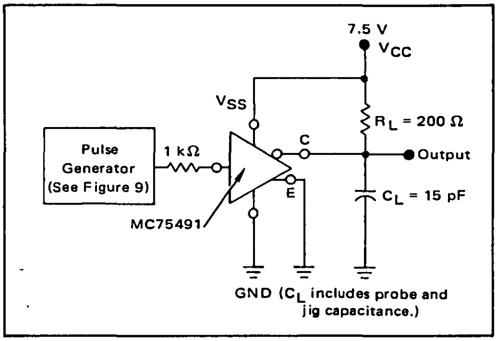
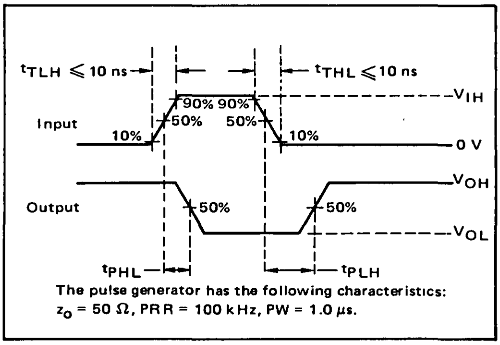
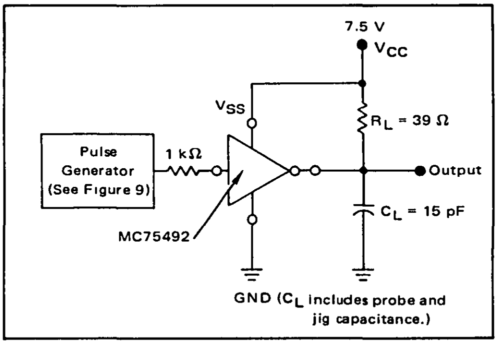


FIGURE 9 – SWITCHING WAVEFORM DEFINITIONS



The pulse generator has the following characteristics: z_o = 50 Ω, PRR = 100 kHz, PW = 1.0 μs.

FIGURE 10 – MC75492 SWITCHING CIRCUIT



TYPICAL APPLICATIONS

FIGURE 11 – QUAD-OR-HEX RELAY DRIVER

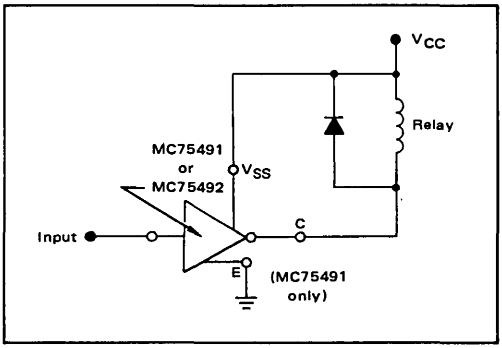
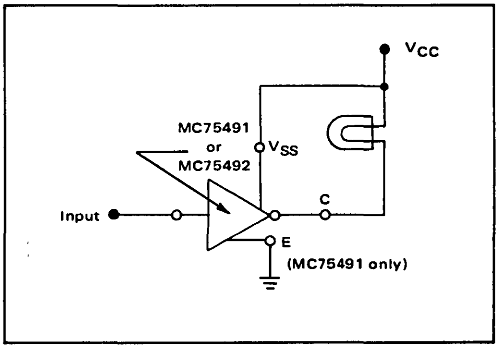


FIGURE 12 – QUAD-OR-HEX LAMP DRIVER



TYPICAL APPLICATIONS (continued)

FIGURE 13 – MOS-TO-MTTL LEVEL TRANSLATOR

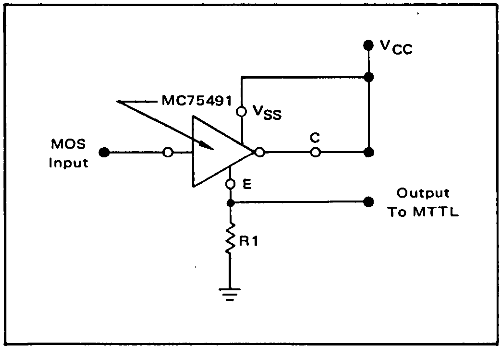


FIGURE 14 – QUAD HIGH-CURRENT NPN TRANSISTOR DRIVER

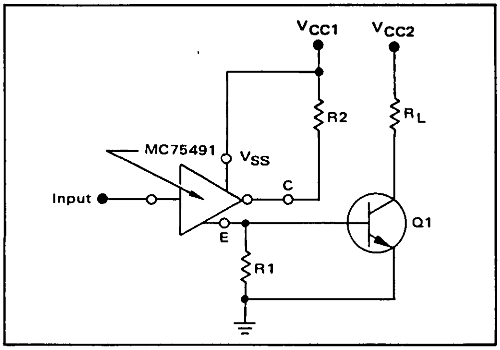
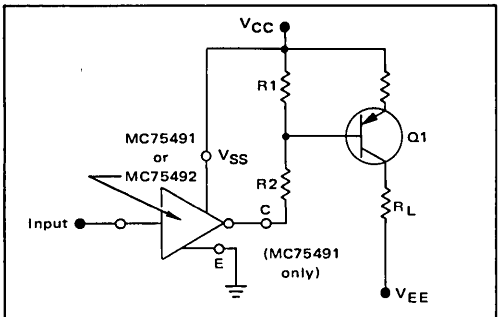


FIGURE 15 – QUAD-OR-HEX HIGH-CURRENT PNP TRANSISTOR DRIVER



(Suitable for use with common-anode VLED displays)

FIGURE 16 – BASE-EMITTER SELECT TRANSISTOR DRIVER

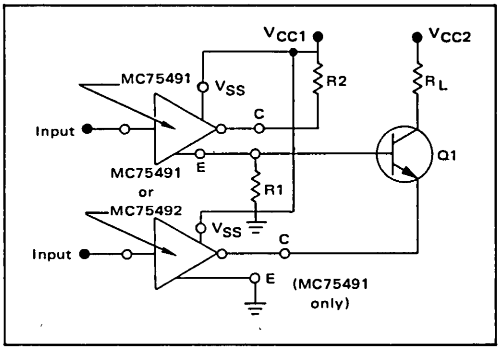
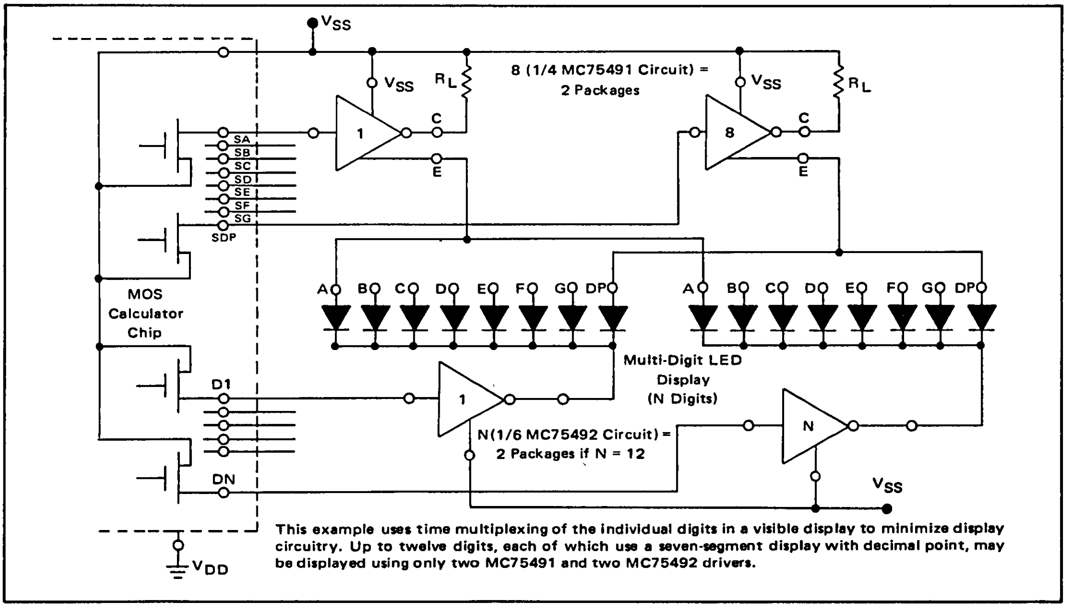


FIGURE 17 – MOS CALCULATOR CHIP-TO-LED INTERFACE CIRCUIT



This example uses time multiplexing of the individual digits in a visible display to minimize display circuitry. Up to twelve digits, each of which use a seven-segment display with decimal point, may be displayed using only two MC75491 and two MC75492 drivers.

TYPICAL APPLICATIONS (continued)

FIGURE 18 – STROBED "NOR" DRIVER

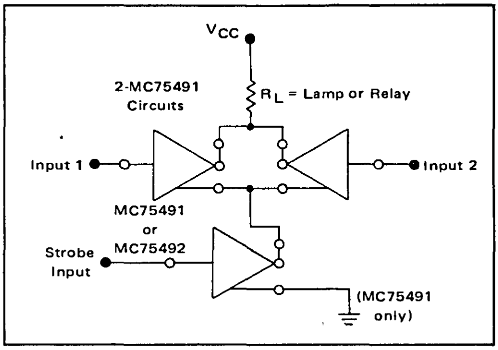
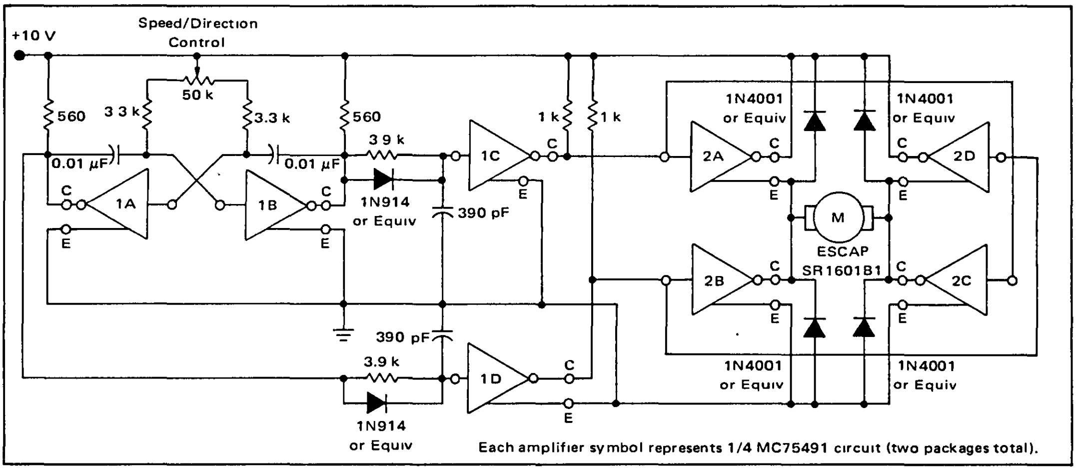


FIGURE 19 – DC MOTOR SPEED/DIRECTION CONTROL CIRCUIT



Each amplifier symbol represents 1/4 MC75491 circuit (two packages total).

MOTOROLA

SN75431
SN75432

Product Preview

DUAL POSITIVE AND/NAND PERIPHERAL DRIVERS

The SN75431 and SN75432 are dual peripheral drivers designed for systems employing either TTL or DTL logic. The SN75431 provides a positive AND function and the SN75432 provides the positive NAND.

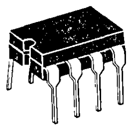
These devices provide a high-speed interface to medium-voltage peripherals requiring drive currents up to 300 mA. Applications include high-speed buffers, line drivers, MOS drivers, memory drivers, and power drivers.

Both parts are mechanically and functionally the same as the 75450B, 460 and 470 equivilents.

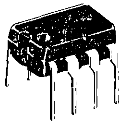
- Characterized for Currents Up to 300 mA
- Very Fast Switching Speed
- TTL or DTL Compatible
- Standard 5.0 V Supply
- Available in Both Plastic and Ceramic Package

DUAL PERIPHERAL DRIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

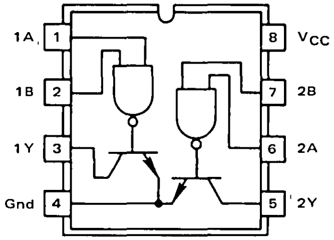


JG SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

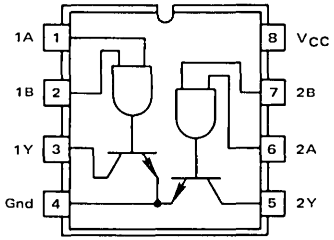
SN75431
Positive AND



Positive Logic Y = AB
Function Table (Each Driver)

A	B	Y
L	L	L(on)
L	H	L
H	L	L
H	H	H

SN75432
Positive NAND



Positive Logic Y = $\overline{AB}$
Function Table (Each Driver)

A	B	Y
L	L	H(off)
L	H	H
H	L	H
H	H	L

H = High Level L = Low Level

This is advance information and specifications are subject to change without notice.

MOTOROLA

SN75451BP
SN75452BP
SN75453BP
SN75454BP

DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

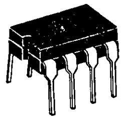
Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

SN75451BP provides the AND function
SN75452BP provides the NAND function
SN75453BP provides the OR function
SN75454BP provides the NOR function

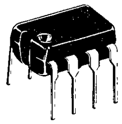
- 300 mA Output Current Capability
- Output Breakdown Voltage — 30 V Min
- MTTL compatible Inputs
- Guaranteed AC Limits

DUAL PERIPHERAL DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

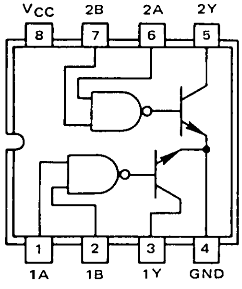


U SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

SN75451BP — Positive AND



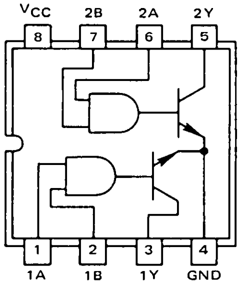
Positive Logic Y = AB

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level

SN75452BP — Positive NAND



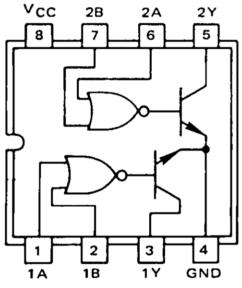
Positive Logic Y = $\overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

SN75453BP — Positive OR



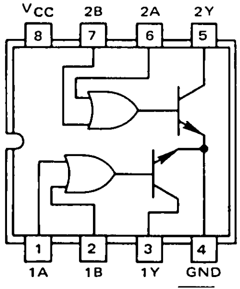
Positive Logic Y = A + B

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H high level, L - low level

SN75454BP — Positive NOR



Positive Logic Y = $\overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7 0	Vdc
Input Voltage	V_I	5 5	Vdc
Interemitter Voltage(2)	–	5 5	Vdc
Output Voltage(3)	V_O	30	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ T_A = 25°C Derate above T_A = +25°C	P_D	830 6 6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Voltage values are with respect to network ground terminal.

(2) This is the voltage between two emitters of a multiple-emitter transistor.

(3) This is the maximum voltage which should be applied to any output when it is in the "off" state

(4) Both halves of these dual circuits may conduct rated current simultaneously, however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

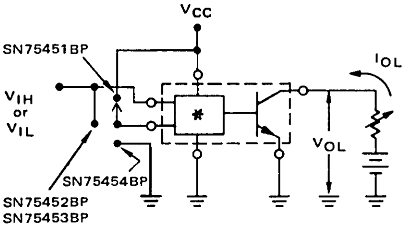
Characteristic		Figure	Symbol	Min	Typ (1)	Max	Unit
Input Voltage — High Logic State		1,2	V_{IH}	2.0	–	–	Vdc
Input Voltage — Low Logic State		1,2	V_{IL}	–	–	0 8	Vdc
Input Clamp Voltage (V_{CC} = 4 75 V, I_I = -12 mA)		4	V_I	–	-1.2	-1.5	Vdc
Output Current — High Logic State (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IH} = 2.0 V) (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IL} = 0.8 V)	 SN75451BP, SN75453BP SN75452BP, SN75454BP	2	I_{OH}	–	–	100	µA
Output Voltage — Low Logic State (V_{CC} = 4.75 V, V_{IL} = 0 8 V) (V_{CC} = 4.75 V, V_{IH} = 2.0 V) (I_{OL} = 100 mA) (I_{OL} = 300 mA)	 SN75451BP, SN75453BP SN75452BP, SN75454BP	1	V_{OL}	 – –	 0.25 0 5	 0 4 0.7	Vdc
Input Current — High Logic State (V_{CC} = 5.25 V, V_I = 2.4 V) (V_{CC} = 5.25 V, V_I = 5 5 V)		3	I_{IH}	 – –	 – –	 40 1.0	 µA mA
Input Current — Low Logic State (V_{CC} = 5 25 V, V_I = 0 4 V)		4	I_{IL}	–	-1.0	-1.6	mA
Power Supply Current — Output High Logic State (V_{CC} = 5.25 V, V_I = 5 0 V) (V_{CC} = 5.25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5.0 V) (V_{CC} = 5.25 V, V_I = 0)	 SN75451BP SN75452BP SN75453BP SN75454BP	5	I_{CCH}	 – – – –	 7 0 11 8 0 13	 11 14 11 17	mA
Power Supply Current — Output Low Logic State (V_{CC} = 5 25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5 0 V) (V_{CC} = 5 25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5 0 V)	 SN75451BP SN75452BP SN75453BP SN75454BP	5	I_{CCL}	 – – – –	 52 56 54 61	 65 71 68 79	mA

(1) Typical Values Measured with V_{CC} = 5 0 V, T_A = 25°C.

TEST CIRCUITS

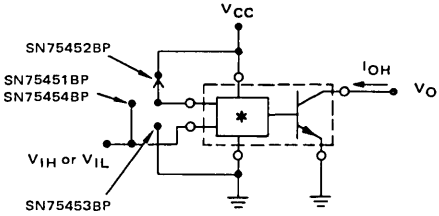
(Current into terminal is shown as a positive value. Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL},
V_{IH} – SN75452BP and SN75454BP
V_{IL} – SN75451BP and SN75453BP



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH},
V_{IH} – SN75451BP and SN75453BP
V_{IL} – SN75452BP and SN75454BP



Each input is tested separately.

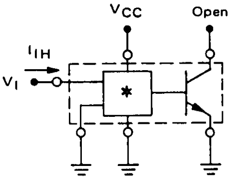
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
SN75451BP						
Low-to-High-Level Output	t_{PLH}	6	–	17	25	ns
High-to-Low-Level Output	t_{PHL}		–	18	25	
SN75452BP						
Low-to-High-Level Output	t_{PLH}	6	–	18	35	ns
High-to-Low-Level Output	t_{PHL}		–	16	35	
SN75453BP						
Low-to-High-Level Output	t_{PLH}	6	–	15	25	ns
High-to-Low-Level Output	t_{PHL}		–	17	25	
SN75454BP						
Low-to-High-Level Output	t_{PLH}	6	–	25	35	ns
High-to-Low-Level Output	t_{PHL}		–	19	35	
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
SN75451BP						
Low-to-High-Level Output	t_{TLH}	6	–	6.0	8.0	ns
High-to-Low-Level Output	t_{THL}		–	8.0	12	
SN75452BP						
Low-to-High-Level Output	t_{TLH}	6	–	6.0	8.0	ns
High-to-Low-Level Output	t_{THL}		–	9.0	12	
SN75453BP						
Low-to-High-Level Output	t_{TLH}	6	–	5 0	8 0	ns
High-to-Low-Level Output	t_{THL}		–	8.0	12	
SN75454BP						
Low-to-High-Level Output	t_{TLH}	6	–	5 0	8.0	ns
High-to-Low-Level Output	t_{THL}		–	8.0	12	

TEST CIRCUITS (Continued)

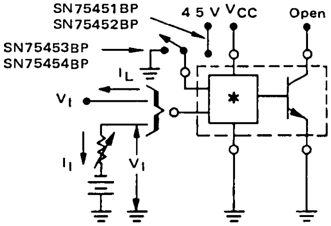
(Current into terminal is shown as a positive value
Arrows indicate actual direction of current flow.)

FIGURE 3 – I_{IH}
(ALL DEVICE TYPES)



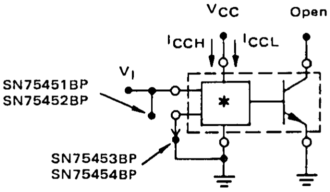
Each input is tested separately

FIGURE 4 – I_{IL},V_I
(ALL DEVICE TYPES)



Each input is tested separately.

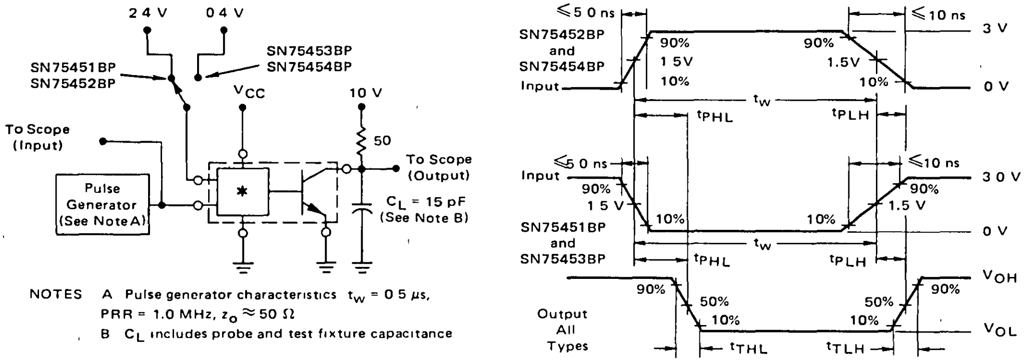
FIGURE 5 – I_{CCH}, I_{CCL}
(ALL DEVICE TYPES)



*See page 1 for specific gate type.

Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

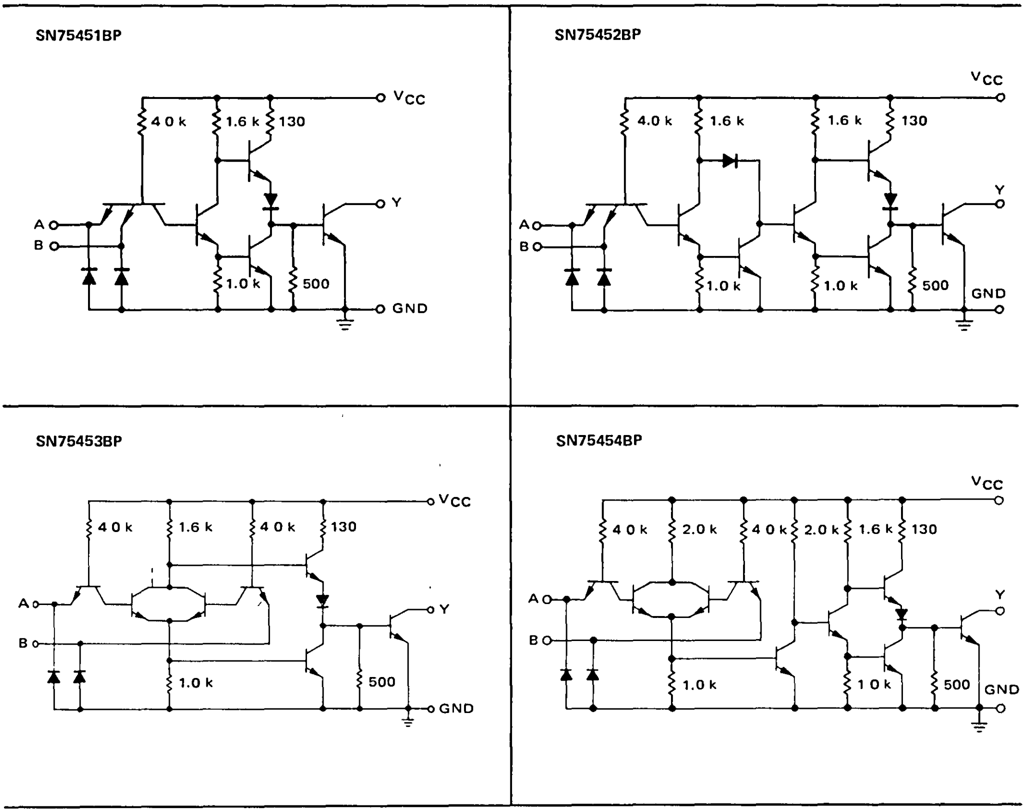


NOTES A Pulse generator characteristics t_w = 0 5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$

B C_L includes probe and test fixture capacitance

REPRESENTATIVE SCHEMATIC DIAGRAMS

(1/2 Circuits Shown)


SN75451BP

SN75452BP

SN75453BP

SN75454BP

Communication Interface (Telephony)

6

COMMUNICATION INTERFACE (Telephony)

*Industrial

MOTOROLA

MC3416

Specifications and Applications Information

4 x 4 x 2 CROSSPOINT SWITCH

The MC3416 consists of a pair of 4 x 4 matrices of dielectrically isolated SCR's, triggered by a common selection matrix. The device is intended for switching analog signals in communication systems. The use of dielectric isolation processing provides excellent crosstalk isolation while maintaining minimal insertion loss.

The selection array consists of PNP transistors with the input thresholds compatible with either CMOS or TTL logic families.

The MC3416 is a monolithic pin-for-pin replacement for the discontinued MCBH7601 hybrid device.

- Low Series Resistance – r_{on} = 6.0 Ohms (Typ) @ I_{AK} = 20 mA
- High Series Resistance – r_{off} = 100 MΩ (Min)
- Pin Compatible with MCBH7601 or RC4444
- High Breakdown Voltage – 30 V (Typ)
- Selection Matrix Compatible with TTL or CMOS Logic Levels
- Dielectric Isolation Insures Low Crosstalk and Low Insertion Loss

4 x 4 x 2 CROSSPOINT SWITCH

DIELECTRICALLY ISOLATED MONOLITHIC INTEGRATED CIRCUIT

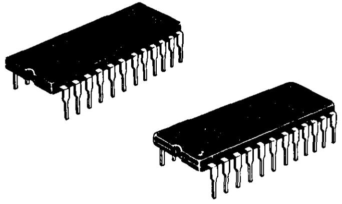


FIGURE 1 – REPRESENTATIVE CELL SCHEMATIC
(Repeated 16 Times)

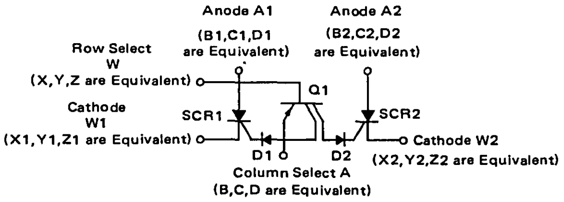
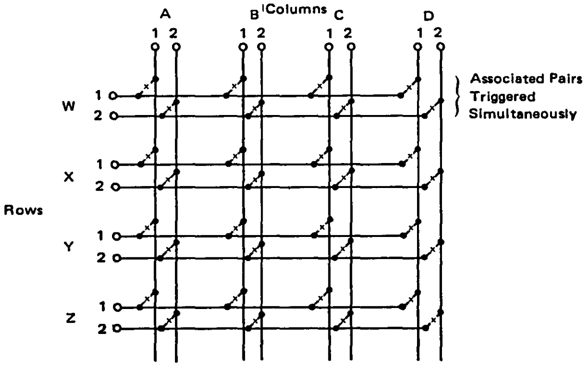
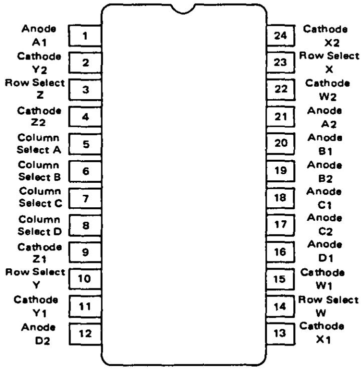


FIGURE 2 – MATRIX CONFIGURATION AND NOMENCLATURE
(X Indicates a Possible Connection)



PIN CONNECTIONS



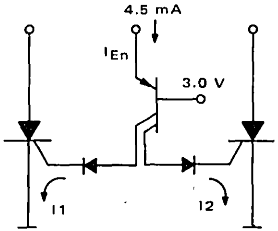
MAXIMUM RATINGS (Unless otherwise noted, T_A = 25°C)

Rating	Symbol	Value	Unit
Anode-Cathode Current — Continuous (only one SCR at a time)	I_{AK}	150	mA
Enable Current	I_{En}	10	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	150°C	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Unit
Anode Cathode Breakdown Voltage (I_{AK} = 25µA)	BV_{AK}	25	—	Vdc
Cathode-Anode Breakdown Voltage (I_{KA} = 25µA)	BV_{KA}	25	—	Vdc
Base-Cathode Breakdown Voltage (I_{BK} = 25µA)	BV_{BK}	25	—	Vdc
Cathode-Base Breakdown Voltage (I_{KB} = 25µA)	BV_{KB}	25	—	Vdc
Base-Emitter Breakdown Voltage (I_{BE} = 25µA)	BV_{BE}	25	—	Vdc
Emitter-Cathode Breakdown Voltage (I_{EK} = 25µA)	BV_{EK}	25	—	Vdc
OFF State Resistance (V_{AK} = 10 V)	r_{off}	100	—	MΩ
Dynamic ON Resistance	r_{on}			Ω
(Center Current = 10 mA) (See Figure 8)		4.0	12	
(Center Current = 20 mA)		2.0	10	
Holding Current (See Figure 10)	I_H	0.7	3.0	mA
Enable Current (V_B = 1.5 V) (See Figure 7)	I_{En}	4.0	—	mA
Anode-Cathode ON Voltage	V_{AK}			V
(I_{AK} = 10 mA)		—	1.0	
(I_{AK} = 20 mA)		—	1.1	
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open) (See Figure 3)	G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage (V_B = 3.0 V) (See Figure 9)	V_{inh}	—	0.3	V
Inhibit Current (V_B = 3.0 V) (See Figure 9)	I_{inh}	—	0.1	mA
OFF State Capacitance (V_{AK} = 0 V) (See Figure 6)	C_{off}	—	2.0	pF
Turn-ON Time (See Figure 4)	t_{on}	—	1.0	µs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)	dv/dt	800	—	V/µs

FIGURE 3 — TEST CIRCUIT



$$G_{Sh} = \frac{I1}{I2}$$

FIGURE 4 – TEST CIRCUIT FOR dv/dt AND t_{on}

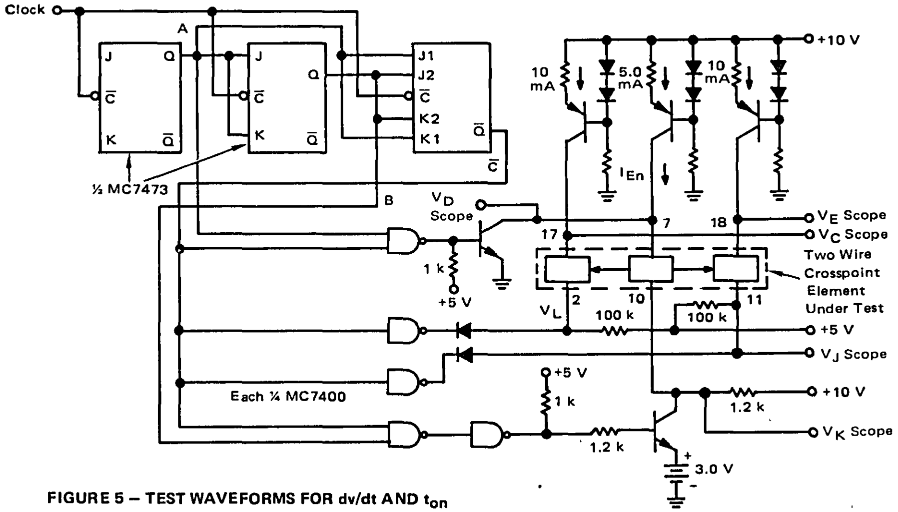


FIGURE 5 – TEST WAVEFORMS FOR dv/dt AND t_{on}

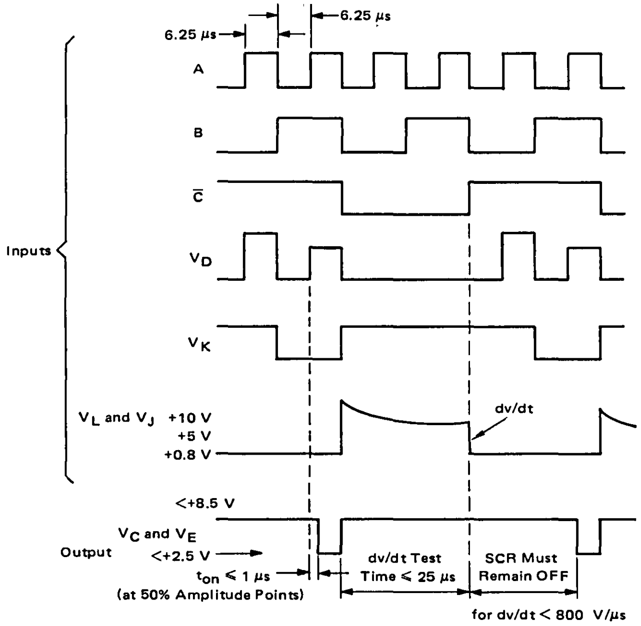
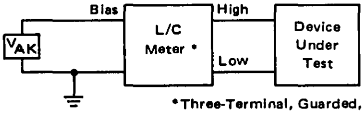


FIGURE 6 – TEST CIRCUIT FOR OFF-STATE CAPACITANCE



All Device Pins Other Than Pins Under Test Are Connected to Test Equipment Ground Terminal

*Three-Terminal, Guarded, Differential Capacitance Meter

FIGURE 7 – ENABLE CURRENT (Both SCR's Must Turn On)

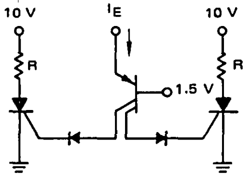


FIGURE 8 – THE CROSSPOINT SCR I-V CHARACTERISTIC (I_G = 0)

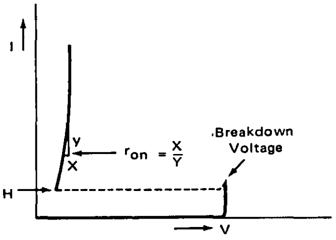
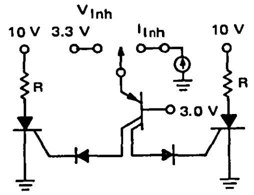


FIGURE 9 – INHIBIT VOLTAGE AND INHIBIT CURRENT (Both SCR's Must Remain OFF)



TYPICAL CHARACTERISTICS

FIGURE 10 – HOLDING CURRENT versus AMBIENT TEMPERATURE

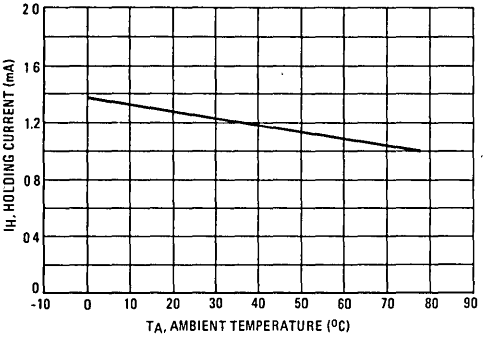


FIGURE 11 – ANODE-CATHODE ON VOLTAGE versus CURRENT AND TEMPERATURE

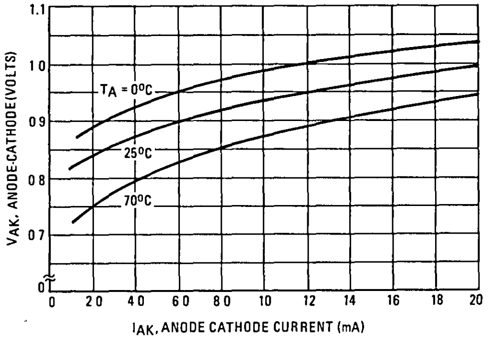


FIGURE 12 – DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) versus ANODE-CATHODE CURRENT

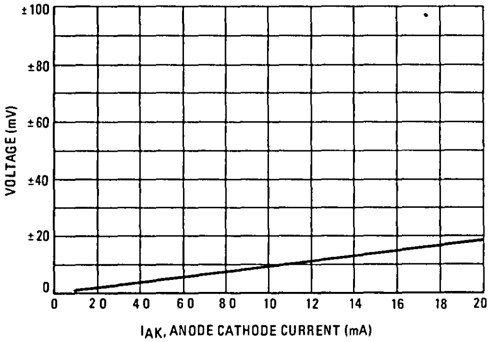


FIGURE 13 – OFF-STATE CAPACITANCE versus ANODE-CATHODE VOLTAGE

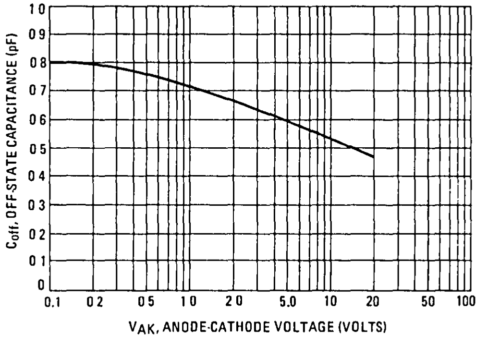


FIGURE 14 – DYNAMIC ON RESISTANCE versus ANODE-CATHODE CURRENT

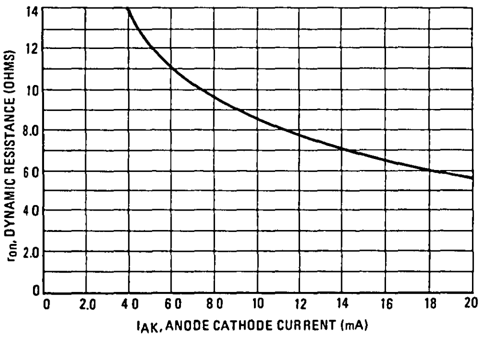


FIGURE 15 – DYNAMIC ON RESISTANCE versus AMBIENT TEMPERATURE

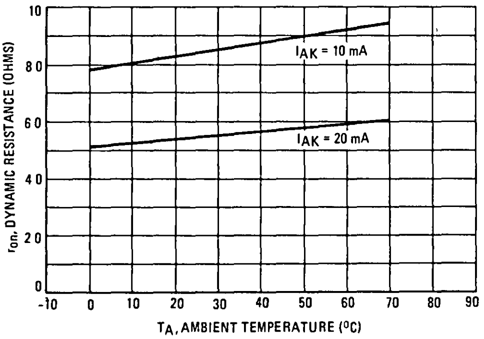


FIGURE 16 – FEEDTHROUGH versus SIGNAL FREQUENCY

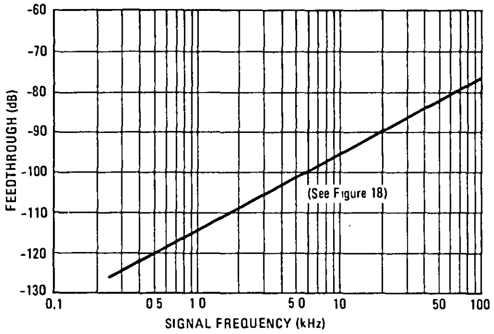


FIGURE 17 – CROSSTALK versus SIGNAL FREQUENCY

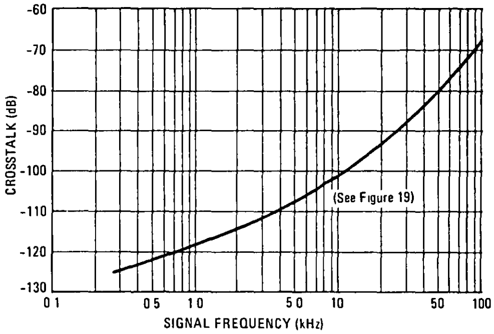
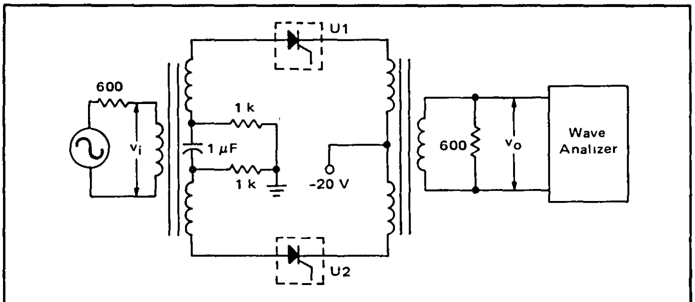
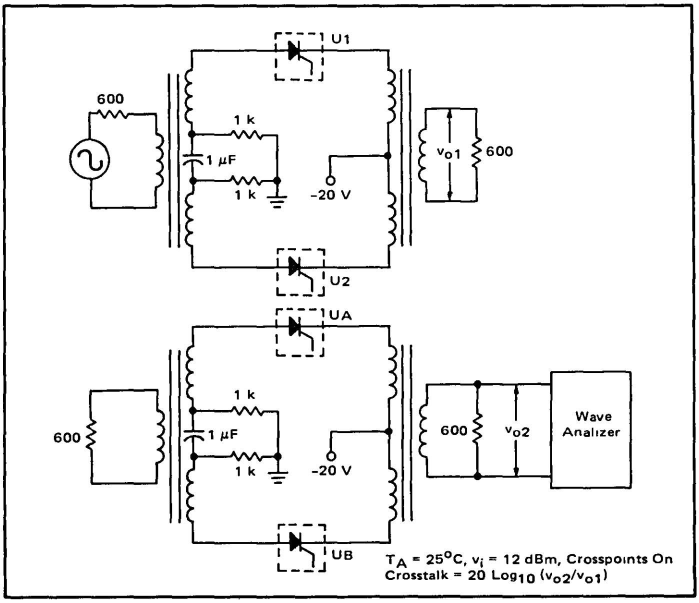


FIGURE 18 – TEST CIRCUIT FOR FEEDTHROUGH versus FREQUENCY



T_A = 25°C, v_i = 12 dBm, Crosspoints Off
Feedthrough = 20 Log_{10} (v_o/v_i)

FIGURE 19 – TEST CIRCUIT FOR CROSSTALK versus FREQUENCY



T_A = 25°C, v_i = 12 dBm, Crosspoints On
Crosstalk = 20 Log_{10} (v_{o2}/v_{o1})

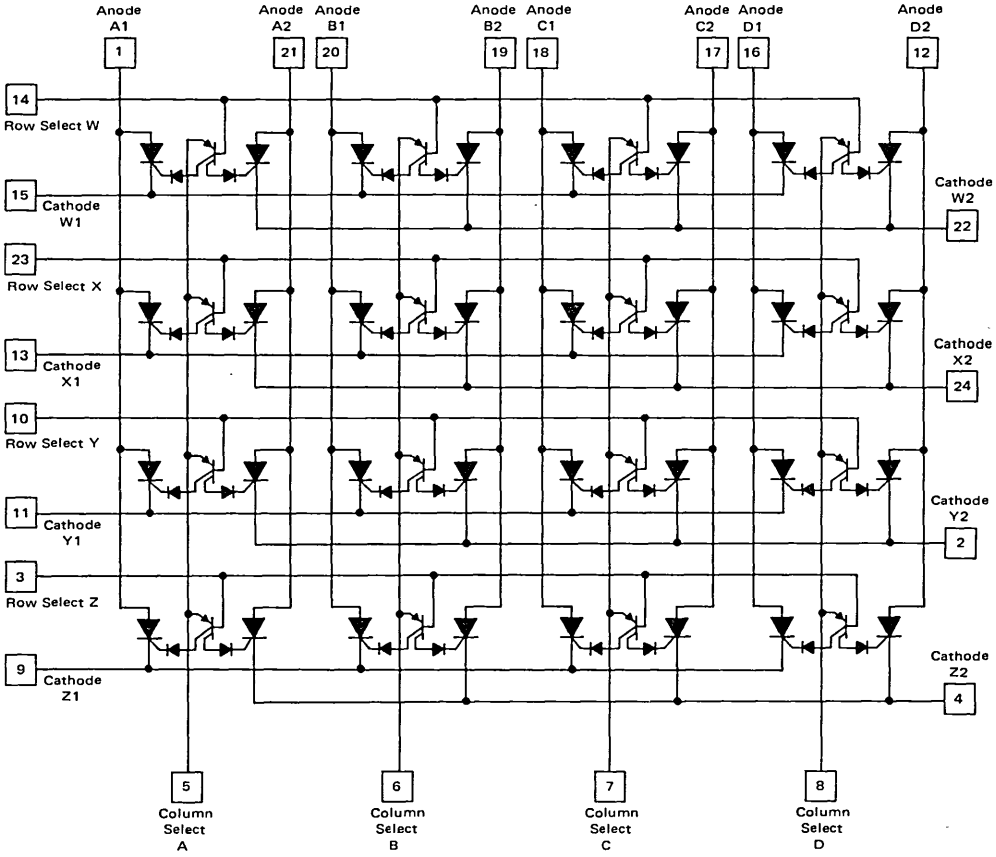


FIGURE 20 — REPRESENTATIVE SCHEMATIC DIAGRAM

TELEPHONE APPLICATION OF THE CROSSPOINT SWITCH

The MC3416 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the MC3416 can significantly reduce the size and cost of existing crosspoint matrices.

SIGNAL PATH CONSIDERATIONS

The MC3416 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward dc current must be maintained through the SCR to retain an ac signal path. This requires that each subscriber-input to the array be capable of sourcing dc current as well as its ac signal. With each subscriber acting as a dc source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 21 shows this configuration. However, with each subscriber acting as a dc source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 22. Here both subscribers source dc current and exchange ac signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The dc

FIGURE 21 – INSTRUMENT-TO-TRUNK CONNECTION

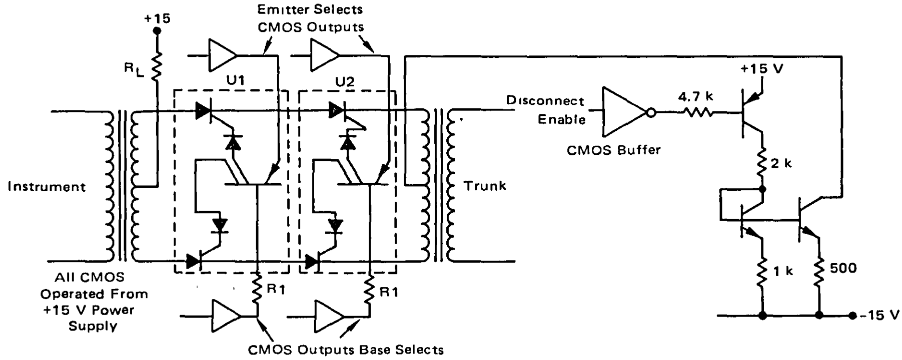
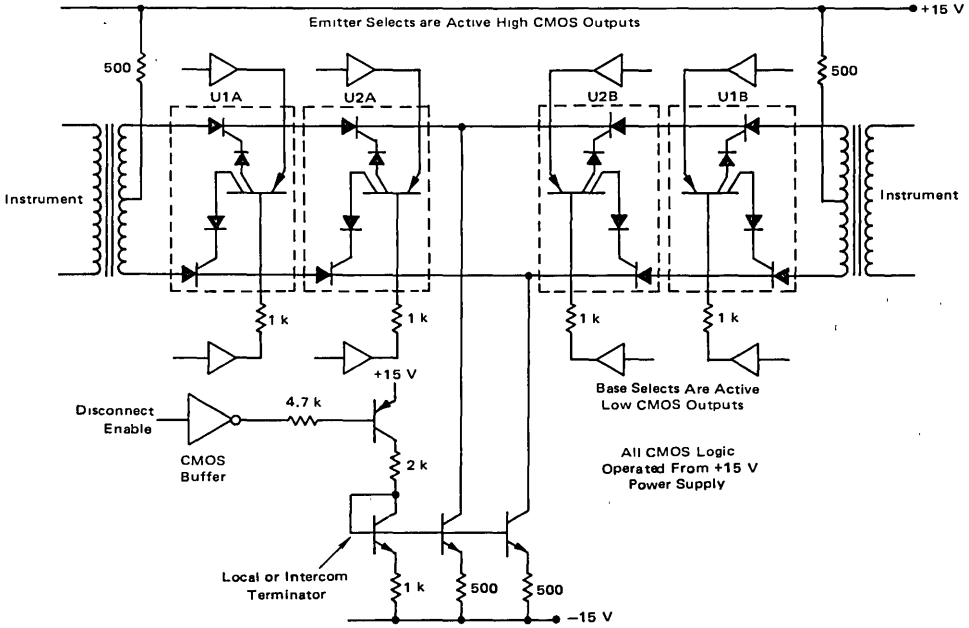


FIGURE 22 – TYPICAL INSTRUMENT TO INSTRUMENT CONNECTION

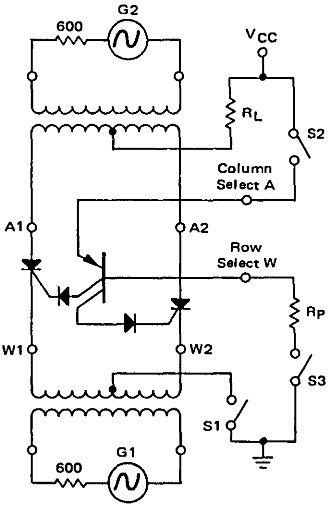


current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 23 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCR's are off as they have no gate drive or dc current path through S1. By closing S2 and S3, gate drive is provided, but the SCR's still remain off as there is no dc current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed — current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an ac signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCR's. To disconnect the ac signal path the SCR's must be commutated off. By opening S1 the dc current path is interrupted and the SCR's switch off. The ac signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCR's simulate a relay contact in that the ac signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired dc current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(V_{CC} - V_{AK})/R_L = 20$ mA. The selection of R_P is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and R_P should drop at least 1.5 Volts. The PNP transistor has a typical gain of one. Thus, R_P should pass at least 2 mA to provide 4 mA column select current.

FIGURE 23— CROSSPOINT OPERATION DEMONSTRATION CIRCUIT



S1	S2	S3	LINE CONDITION
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected.

X = irrelevant

ADDRESSING CONSIDERATIONS

The MC3416 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the MC3416 can be met with standard CMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5 Volts to assure forward bias of the two diodes in the collector circuits. The gate current required for SCR turn on is 1 mA typically. The CMOS one-of-n decoders listed in Table I provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a dc path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the dc path

APPLICATIONS INFORMATION (continued)

requirement, crosspoint arrays should be designed in blocks such that any given dc path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two dc paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 22 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

TABLE I

	Active High Outputs	Active Low Outputs
Dual Binary to 1 of 4	MC14555	MC14556
4-bit latch/4 to 16	MC14514	MC14515
BCD to Decimal Decode	MC14028	

DISCONNECT TECHNIQUES

Since the crosspoint switch maintains signal paths by keeping dc currents through active SCR's, disconnects are easily accomplished by interrupting the dc current path. This can be done anywhere in the circuit, but if the disconnect is done at the terminator then all signal paths established to that terminator are broken simultaneously. In both Figures 21 and 22 this is done by turning off the current sink circuit with a CMOS buffer gate. MC14049 or MC14050 buffers will drive the transistor switch. Once a disconnect is completed, the terminator may be re-enabled and used for another call. Usage of the terminators may be easily monitored with optoelectronic couplers in the collectors of the current sinks without disturbing transmission characteristics.

See Application Note AN-760 for additional applications suggestions.

MOTOROLA

MC3417, MC3517
MC3418, MC3518

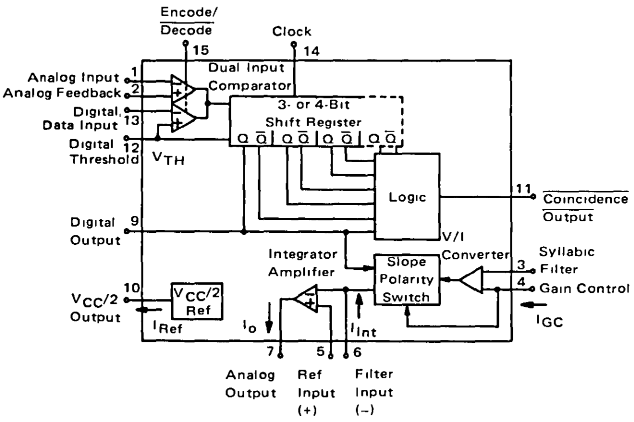
Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

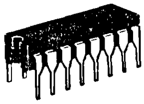
- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

CVSD BLOCK DIAGRAM



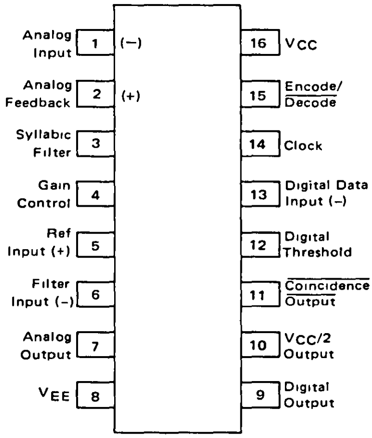
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



MAXIMUM RATINGS

(All voltages referenced to V_{EE}, $T_A = 25^oC$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2 - 1.0$ to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, $T_A = 0^oC$ to $+70^oC$ for MC3417/18, $T_A = -55^oC$ to $+125^oC$ for MC3517/18 unless otherwise noted.)

		MC3417/MC3517			MC3418/MC3518			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16 5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3 7	5 0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16 5 V)	V_I	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16 5 V, I_O = ± 5.0 mA)	V_O	1 3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							µA
Analog Input (I1)		–	0.5	1 5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							µA
Analog Input/Analog Feedback |I1 − I2| – Figure 3		–	0.15	0.6	–	0.05	0.4	
Integrator Amplifier |I5 − I6| – Figure 4		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) – Figure 5	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								µs
Clock Trigger to Digital Output	t_{PLH}	–	1 0	2.5	–	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage – Low Logic State ($I_{OL(Con)}$ = 3 0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current – High Logic State (V_{OH} = 15.0 V, $0^oC \leq T_A \leq 70^oC$)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	µA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	–	V_{CC} – 2.0	+1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current ($1.2\ V \leqslant V_{th} \leqslant V_{CC} - 2.0\ V$)	$I_{I(th)}$							µA
(V_{IL} applied to Pins 13, 14 and 15)		–	–	5.0	–	–	5 0	
(V_{IH} applied to Pins 13, 14 and 15)		–	–10	–50	–	–10	–50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	±5.0	–	–	mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10	–	–	+10	–	–	mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	–	3.0	6.0	–	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \leqslant V_{CC} \leqslant 16.5\ V$)	ϵr	–	–	±3.5	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	–	V_{th} – 0.4	Gnd	–	V_{th} – 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	18.0	V_{th} + 0.4	–	18.0	
Dynamic Total Loop Offset Voltage (Note 2) — Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12 0 µA, V_{CC} = 12 V								
$T_A = 25^{\circ}C$		–	–	–	–	± 0.5	± 1.5	
$0^{\circ}C \leqslant T_A \leqslant +70^{\circ}C$ MC3417/18		–	–	–	–	± 0.75	± 2.3	
$-55^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$ MC3517/18		–	–	–	–	± 1.5	± 4.0	
I_{GC} = 33.0 µA, V_{CC} = 12 V								
$T_A = 25^{\circ}C$		–	± 2.5	± 5 0	–	–	–	
$0^{\circ}C \leqslant T_A \leqslant +70^{\circ}C$ MC3417/18		–	± 3.0	± 7.5	–	–	–	
$-55^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$ MC3517/18		–	±4.5	± 10	–	–	–	
I_{GC} = 12.0 µA, V_{CC} = 5.0 V								
$T_A = 25^{\circ}C$		–	–	–	–	± 1 0	± 2.0	
$0^{\circ}C \leqslant T_A \leqslant +70^{\circ}C$ MC3417/18		–	–	–	–	± 1.3	± 2 8	
$-55^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$ MC3517/18		–	–	–	–	± 2.5	± 5.0	
I_{GC} = 33 0 µA, V_{CC} = 5.0 V								
$T_A = 25^{\circ}C$		–	± 4.0	± 6.0	–	–	–	
$0^{\circ}C \leqslant T_A \leqslant +70^{\circ}C$ MC3417/18		–	± 4.5	± 8.0	–	–	–	
$-55^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$ MC3517/18		–	± 5.5	± 10	–	–	–	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{OH} = –0.35 mA)	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	–	V_{CC}	+3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2)	I_{Int}							
(I_{GC} = 12.0 µA)		8.0	10	12	8.0	10	12	µA
(I_{GC} = 1.5 mA)		1.45	1.50	1.55	1.45	1.50	1.55	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$	–	± 100	± 250	–	± 100	± 250	mV
Input Current — High Logic State (V_{IH} = 18 V)	I_{IH}							µA
Digital Data Input		–	–	+5.0	–	–	+5.0	
Clock Input		–	–	+5.0	–	–	+5.0	
Encode/$\overline{\text{Decode}}$ Input		–	–	+5.0	–	–	+5.0	
Input Current — Low Logic State (V_{IL} = 0 V)	I_{IL}							µA
Digital Data Input		–	–	–10	–	–	–10	
Clock Input		–	–	–360	–	–	–360	
Encode/$\overline{\text{Decode}}$ Input		–	–	–36	–	–	–36	
Clock Input, V_{IL} = 0.4 V		–	–	–72	–	–	–72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and pin 3. The active voltage to current (V-I) converter drives pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_x resistance. Figure 6 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_x resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is tied to pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into pin 6 when the analog input (pin 1) is high with respect to the analog feedback (pin 2) in the encode mode or when the digital data input (pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between pins 6 and 7. Multipole configurations will have different circuitry. The resistance between pins 6 and 7 should always be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long

DEFINITIONS AND FUNCTIONS OF PINS (continued)

while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 – Digital Threshold

This input sets the switching threshold for pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is applied to pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 µs before and after the clock trigger for proper clocking.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 – Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 – POWER SUPPLY CURRENT

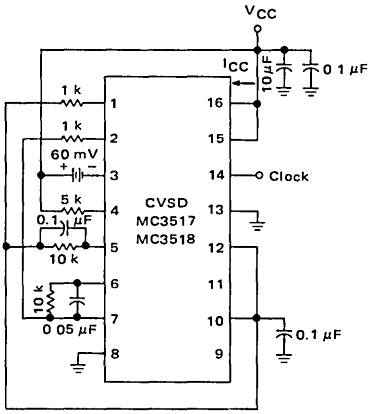
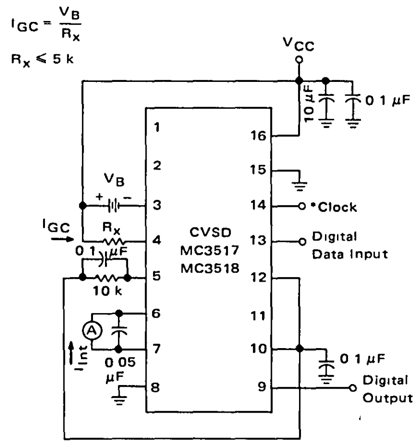


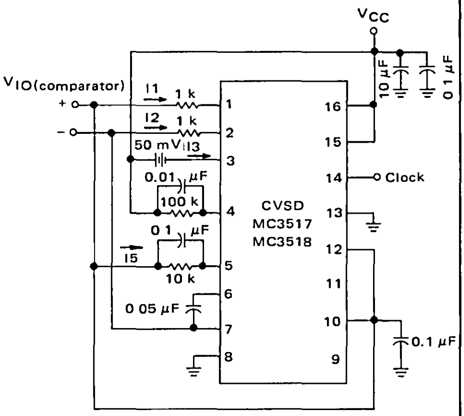
FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{int} – INTEGRATING CURRENT



Note. Digital Output = $\overline{\text{Digital Data Input}}$

•For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

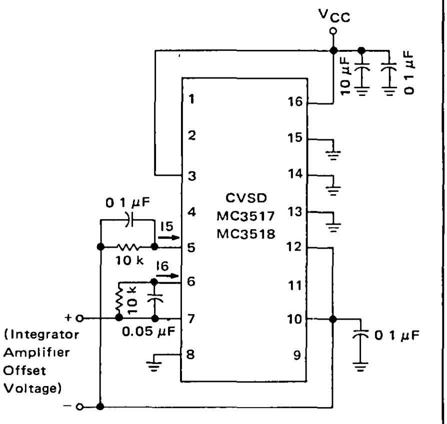
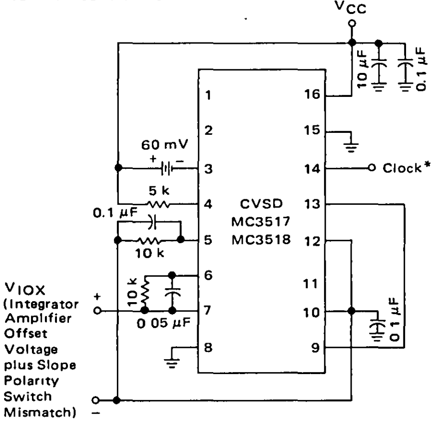


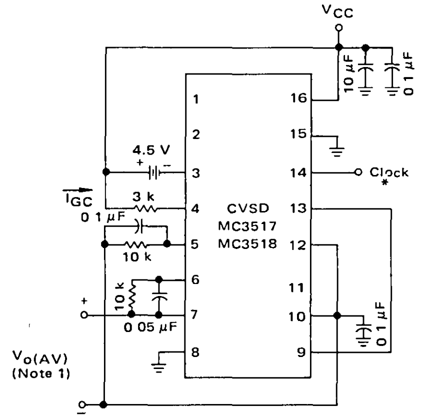
FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}

*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes. 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, page 3

TYPICAL PERFORMANCE CURVES

FIGURE 7 — TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

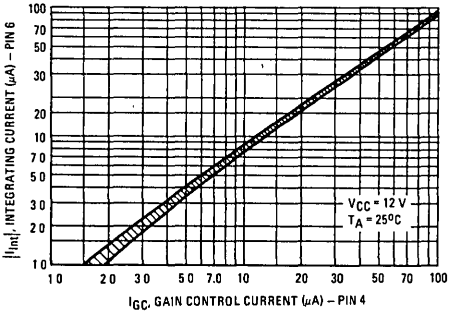


FIGURE 8 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

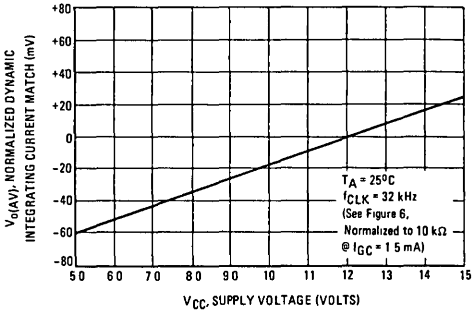


FIGURE 9 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

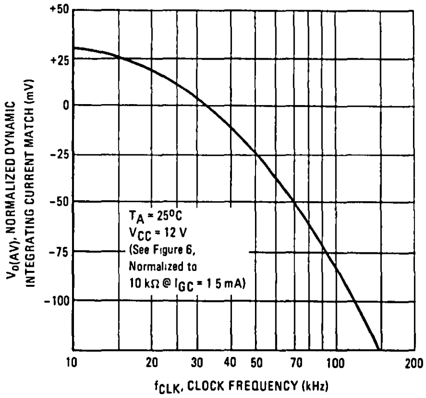


FIGURE 10 — DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

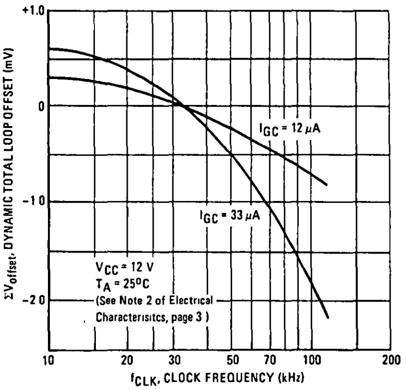


FIGURE 11 — BLOCK DIAGRAM OF THE CVSD ENCODER

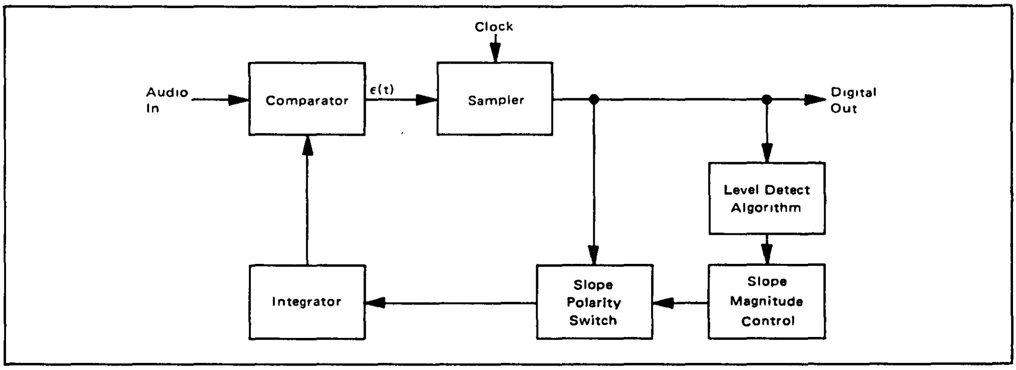


FIGURE 12 – CVSD WAVEFORMS

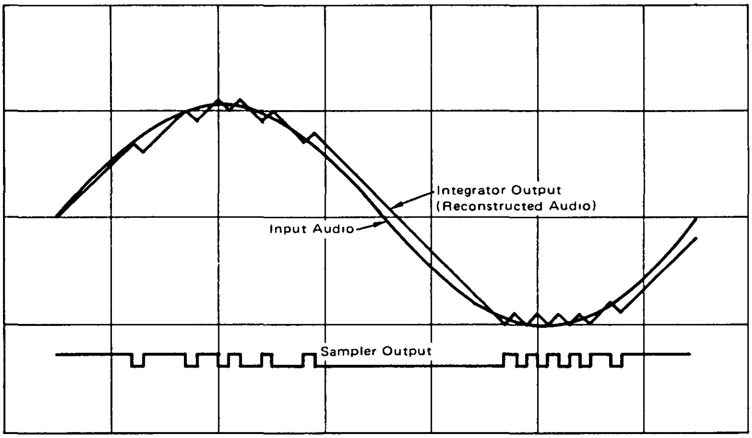


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

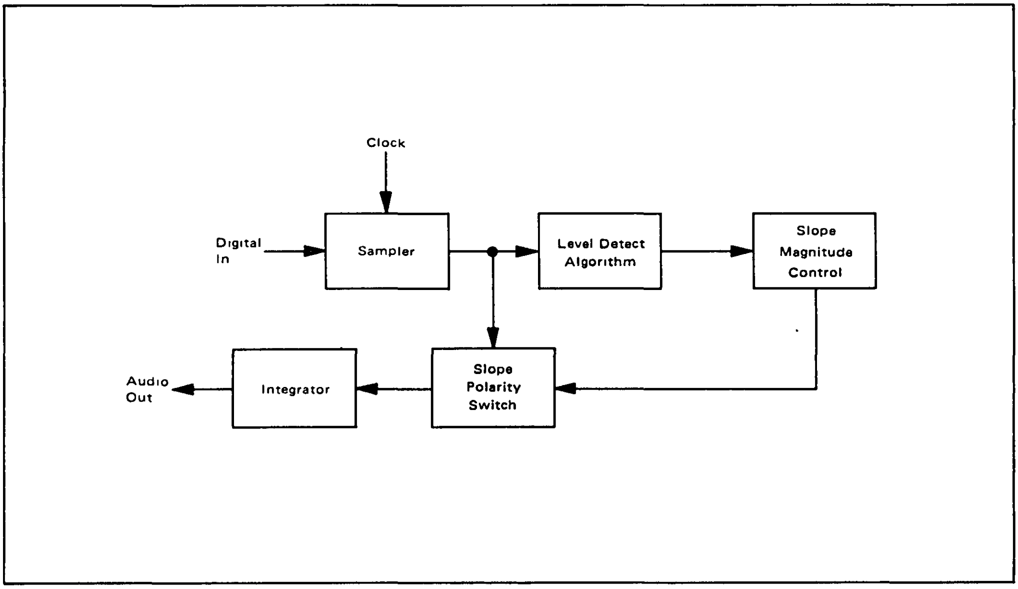
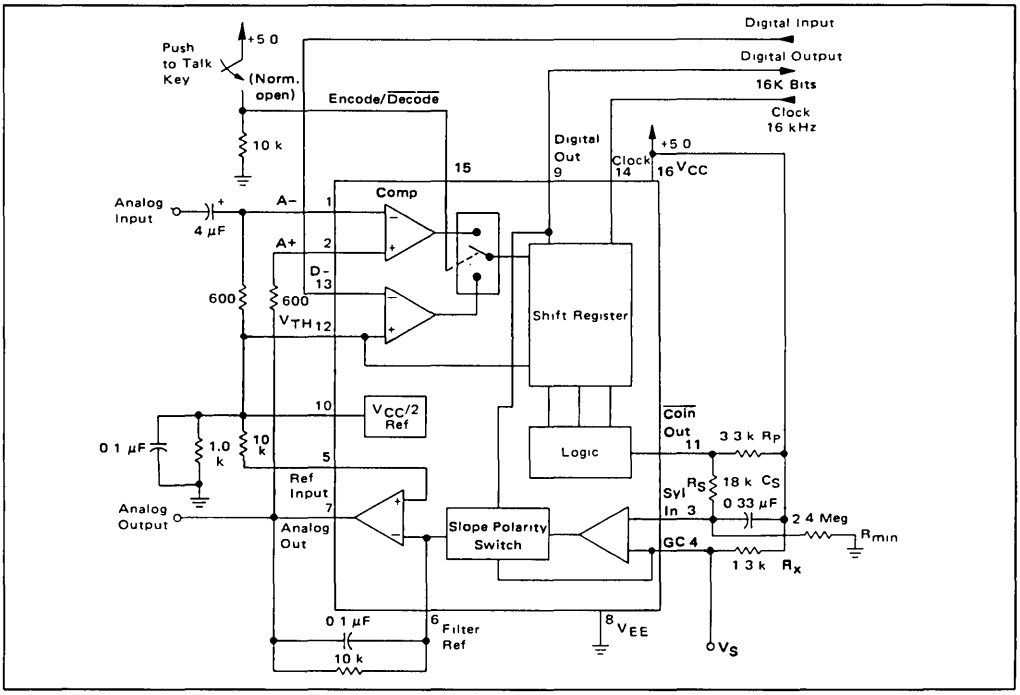


FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

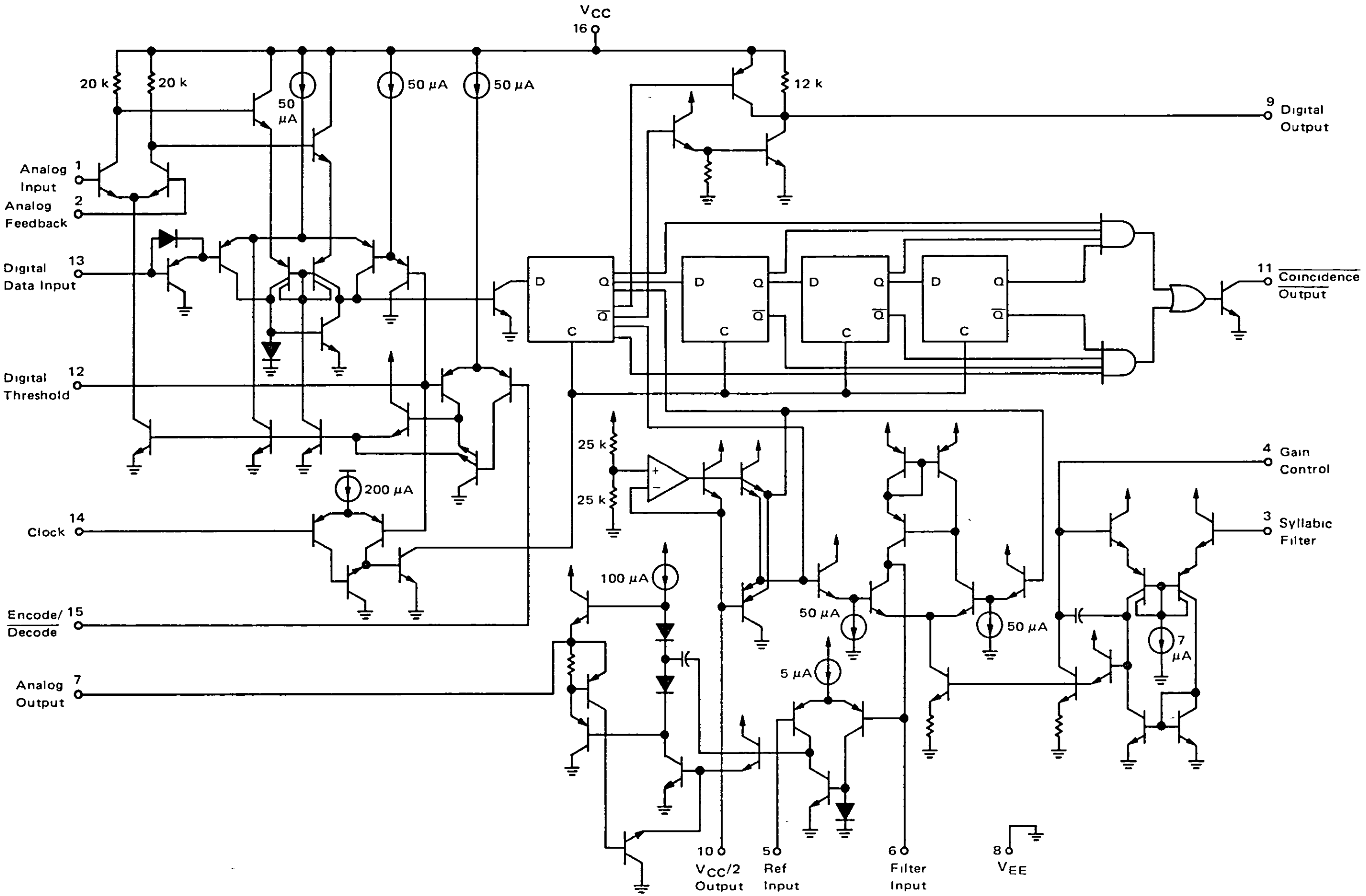
A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

CVSD CIRCUIT SCHEMATIC



CVSD DESIGN CONSIDERATIONS (continued)

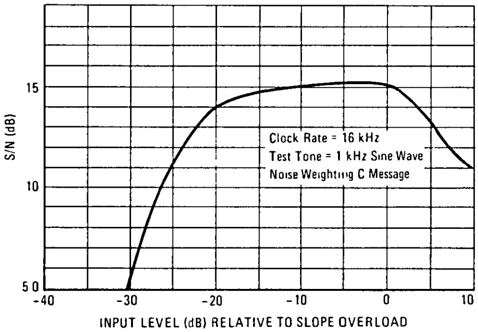
Layout Considerations

Care should be exercised to isolate all digital signal paths (pins 9, 11, 13, and 14) from analog signal paths (pins 1-7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ \text{k}\Omega,\ C = 0.1\ \mu\text{F}$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ \text{Hz}$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R} + \frac{C dV_o}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ \text{V}}{{}^*2(10\ \text{k}\Omega)} + \frac{0.1\ \mu\text{F}(1.1)}{0.125\ \text{ms}} = 0.935\ \text{mA}$$

*The maximum voltage across RI when maximum slew is required is:

$$\frac{1.1\ \text{V}}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ \text{mA}}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

CVSD DESIGN CONSIDERATIONS (continued)

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F\ 20\,mV}{62.5\,\mu s} = 33\,\mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_x.

$$I_i R_x = V_S min;\ for\ 33\,\mu A,\ V_S min = 41.6\,mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \qquad R_{min} \simeq 2.4\,M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

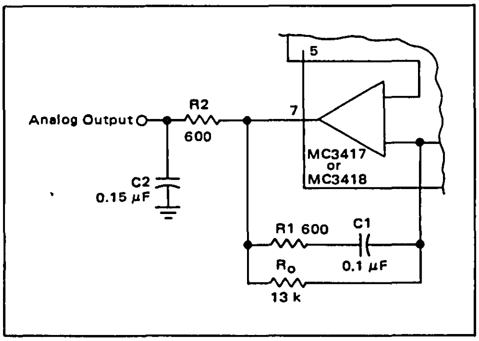
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on pin 1

INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_0}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

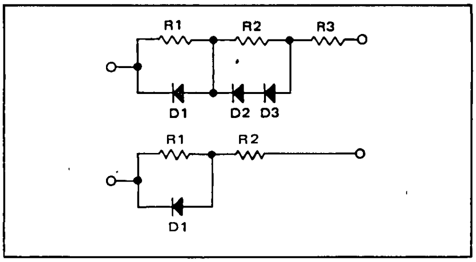
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

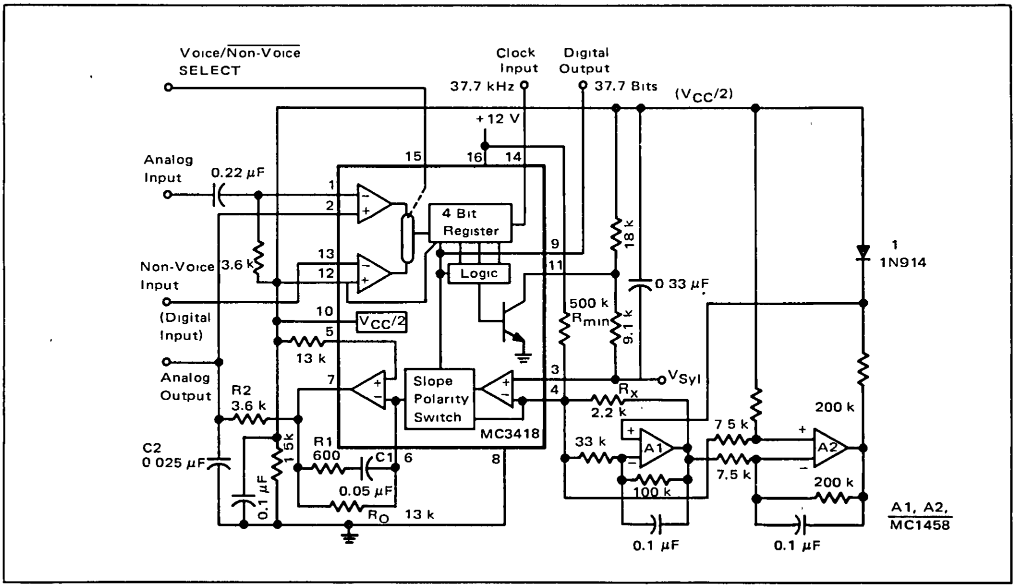
The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% comppanding ratio and the instantaneous companding ratio at pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2

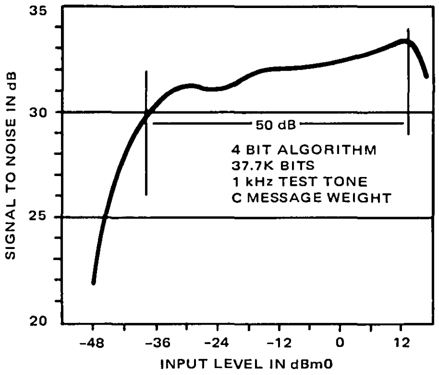
FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER
(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)



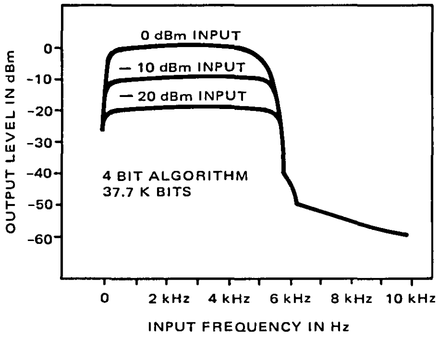
TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

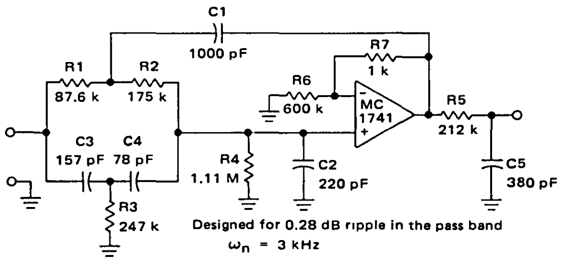
The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

---

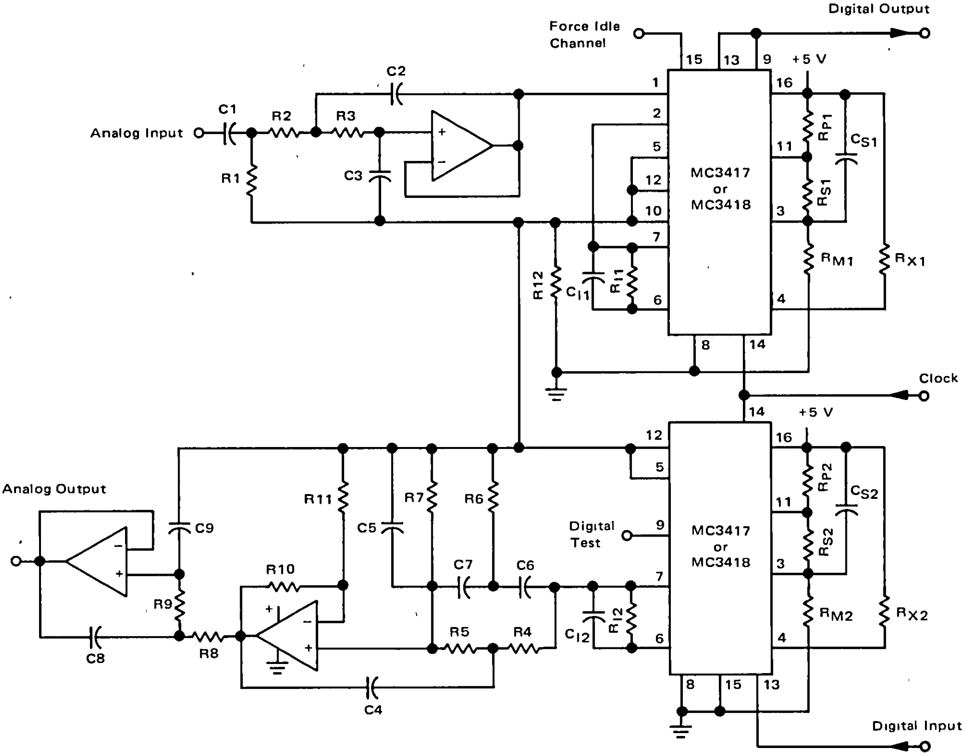
*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 µF would work well.

FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
ω_n = 3 kHz
ω_s = ≅ 6 kHz
AdB at ω_s and above 29.5 dB

FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} – 3 3 kΩ
R_{P1}, R_{P2} – 3 3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} –5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0 05 μF
C_{I1}, C_{I2} – 0 05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res 5%
All Cap 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1 645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29 5 kΩ
R11 – 72 kΩ

C1 – 3 3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note All Res. 0 1% to 1%.
All Cap 1.0%

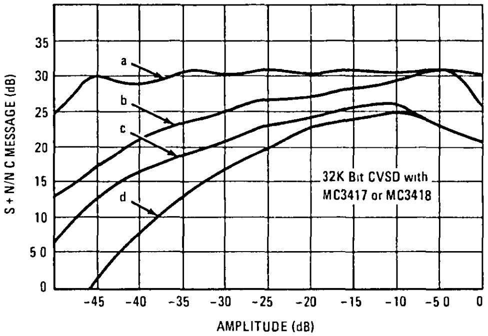
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 — COMPARATIVE CODEC PERFORMANCE — SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18 — MC3418)

Curve b — Double integration (Figure 21 using Figure 6 — MC3418)

Curve c — Single integration (Figure 21 — MC3418) with 6 mV step size

Curve d — Single integration (Figure 21 — MC3417) with 25 mV step size

MOTOROLA

MC3419
MC3519

Product Preview

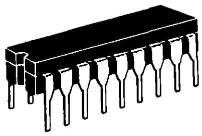
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT

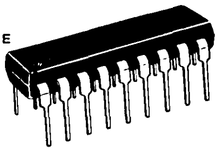
TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Class 5, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 60 V supply.

- Transmit and Receive Gain is Externally Selected
- On-Hook Power Below 5.0 mW
- Current Sensing Outputs Provided for Off-Hook Status from Both Tip and Ring Leads
- Size and Weight Reduction Over Present Approaches
- Compatible with IEEE and REA Specifications
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

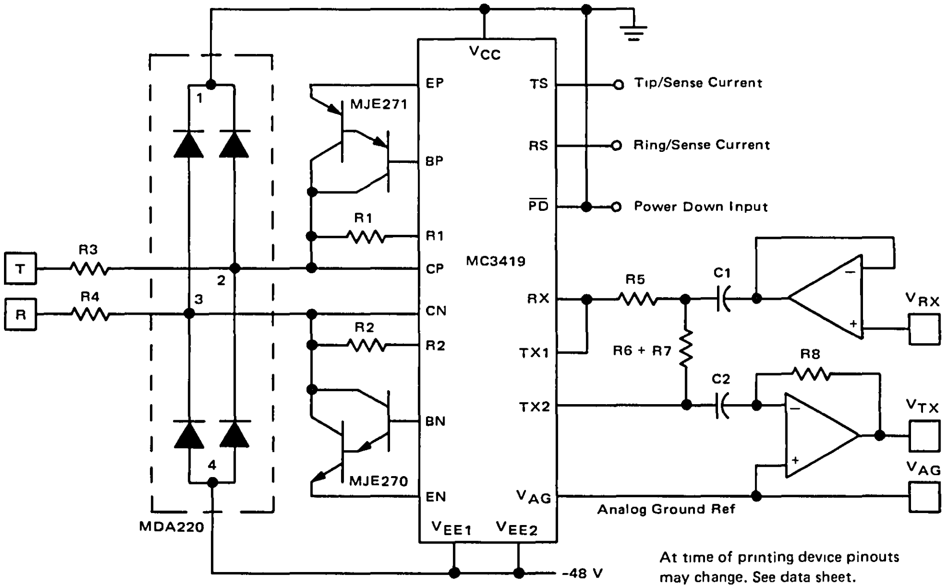


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 701

FIGURE 1 – SUBSCRIBER LOOP INTERFACE CIRCUIT DIAGRAM



At time of printing device pinouts may change. See data sheet.

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Rated Voltage	V_{EE1}, V_{EE2}	60	Vdc
Maximum Power Dissipation $T_A = 25^oC$ Derate above $+25^oC$	P_D	1.5	Watts
Operating Ambient Temperature Range MC3419 MC3519	T_A	0 to +70 -40 to +85	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC
Operating Junction Temperature	T_J	150	^oC

ELECTRICAL CHARACTERISTICS ($V_{EE1} = V_{EE2} = -48$ V, $V_{CC} = 0$, $V_{AG} = -6.0$ V, $T_A = 25^oC$)

Characteristic	Symbol	Min	Typ	Max	Unit
Loop Current Range ($R_{Loop} = 0 - 1900\ \Omega$)	I_{Lp}	20	–	120	mA
Transhybrid Reception Ratio – Figure 2 ($R_L = 900\ \Omega, V_{RX} = 0.775\ V_{RMS}, V_G = 0$)	V_{RL}/V_{RX}	-0.1	0	+0.1	dB
Transhybrid Transmission Ratio – Figure 2 ($R_L = 900\ \Omega, V_{RX} = 0, V_G = 0.775\ V_{RMS}$)	V_{TX}/V_{RL}	-0.1	0	+0.1	dB
Transhybrid Rejection Ratio – Figure 2 ($R_L = 900\ \Omega, V_{RX} = 0.775\ V_{RMS}, V_G = 0$)	V_{TX}/V_{RX}	–	-46	–	dB
Input Resistance (@R and T)–Figure 2	R_{in}		900		Ω
In-Band Longitudinal Suppression Ratio – Figure 3 ($e_{Lon} = 0.775\ V_{RMS}$, f = 1 kHz, $R_L = 900\ \Omega$)	V_{TX}/e_{Lon}	–	-66	–	dB
60 Cycle Longitudinal Suppression Ratio – Figure 3 ($e_{Lon} = 30\ V_{RMS}$, f = 60 Hz, $R_L = 1900\ \Omega$)	V_{TX}/e_{Lon}	–	-66	–	dB
Longitudinal Capacity – Figure 3 (60 Hz)	i_{Lon}	–	35	–	mA_{RMS}
Level Linearity (f = 300 Hz to 3400 Hz, Reception $V_{RX} = 0.775\ V_{RMS}$, Transmission $V_{RL} = 0.775\ V_{RMS}$)	 V_{RX}/V_{RL} V_{RL}/V_{TX}	 -0.1 -0.1	 – –	 +0.1 +0.1	 dB dB
Idle Noise		–	0	–	$dBrnC_o$
Off-Hook Power Dissipation (IC) ($I_{Loop} = 120$ mA)	$P_{D(Off)}$	–	0 6	–	Watts
On-Hook Power Dissipation	$P_{D(On)}$	–	5 0	–	mW
Tip Status Current ($I_{Loop} = 0$ to 120 mA)	I_{TS}/I_T	–	0.0104	–	mA/mA
Ring Status Current ($I_{Loop} = 0$ to 120 mA)	I_{RS}/I_R	–	0.0104	–	mA/mA
Voltage Range of Analog Ground	V_R	0	–	-12	Volts
Analog Ground Input Current	I_{Gnd}	–	1 0	–	μA
Fault Currents (Tip to V_{CC} – Figure 2) (Ring to V_{CC} – Figure 2) (Ring and Tip to V_{CC} – Figure 2) (Tip to Ring Short – Figure 2)	 I_T I_R $\lvert I_T\rvert + \lvert I_R\rvert$ $I_T + I_R$	 – – – –	 0 5.0 5.0 120	 – – – –	 mA mA mA mA
$\overline{\text{Power Down}}$ Input Levels Logic High Logic Low	 V_{IH} V_{IL}	 V_{CC}-1.0 –	 – –	 – V_{CC}-2 0	Vdc

FIGURE 2 — AC TRANSMISSION TESTS OF MC3419 AT BALANCE

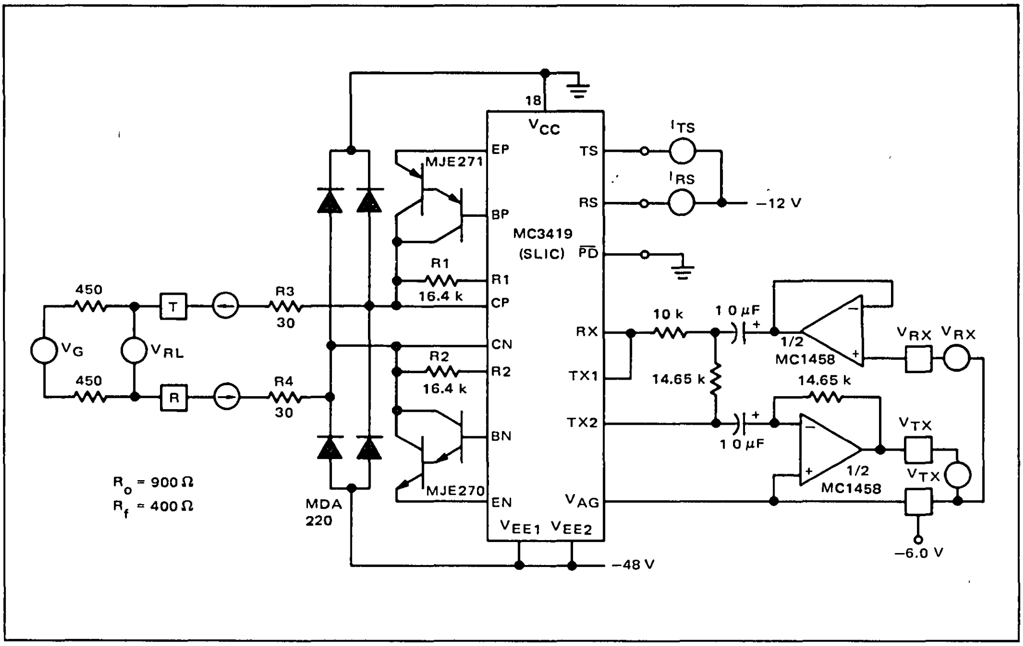


FIGURE 3 — LONGITUDINAL TEST

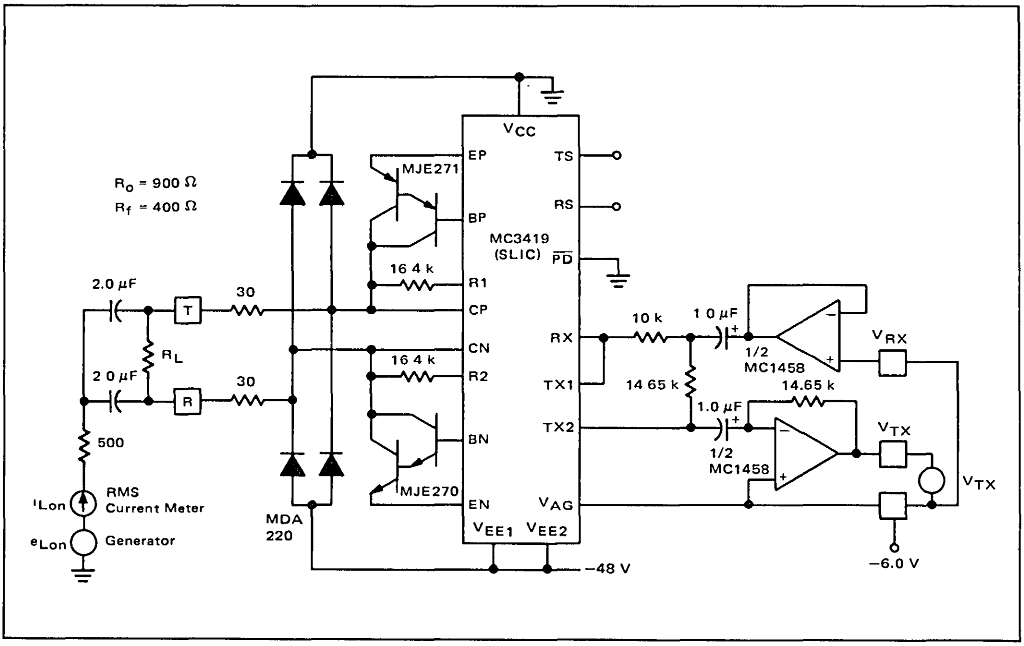
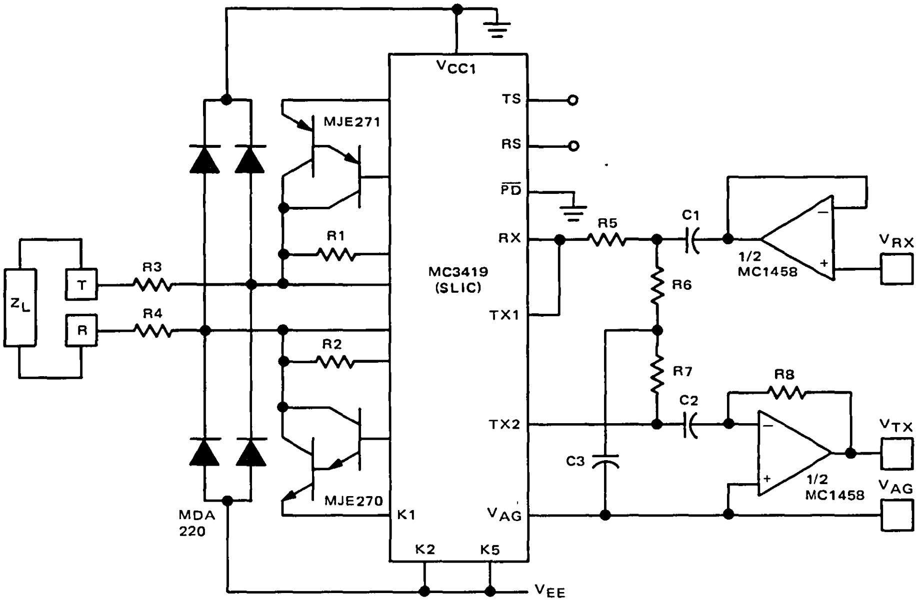


FIGURE 4 – DESIGN EQUATIONS



Internal to the MC3419 are three precise gain constants

K1 = 4   K2 = 23 75   K5 = 0.4   K5' = 0.6

K5 and K5' are selected by connecting TX1 or TX2 to RX respectively. The remaining TX pin is connected to R6 and R7.

1. The dc feed resistance is R_f

$$R_f = \frac{R1 + R2}{1+K1K2} + R3 + R4$$

2 The termination resistance is R_o

$$R_o = \frac{R1 + R2}{1 + K1K2K5} + R3 + R4$$

FIGURE 5 – HYBRID LOOP CURRENT versus LOOP RESISTANCE (FOR 24 AND 48 V SUPPLY)

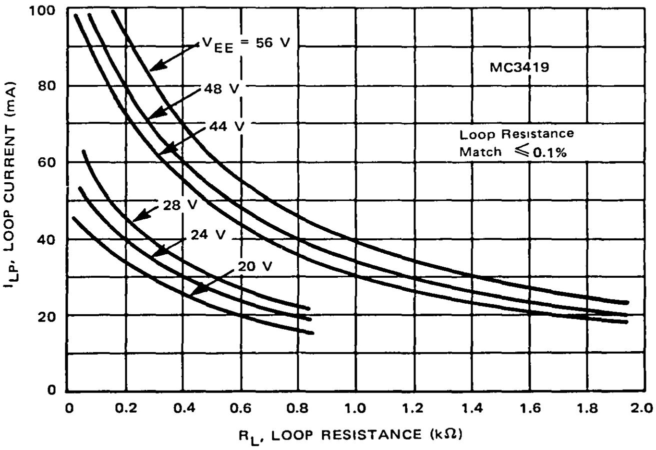


FIGURE 6 – RING TRIP USING MC3419

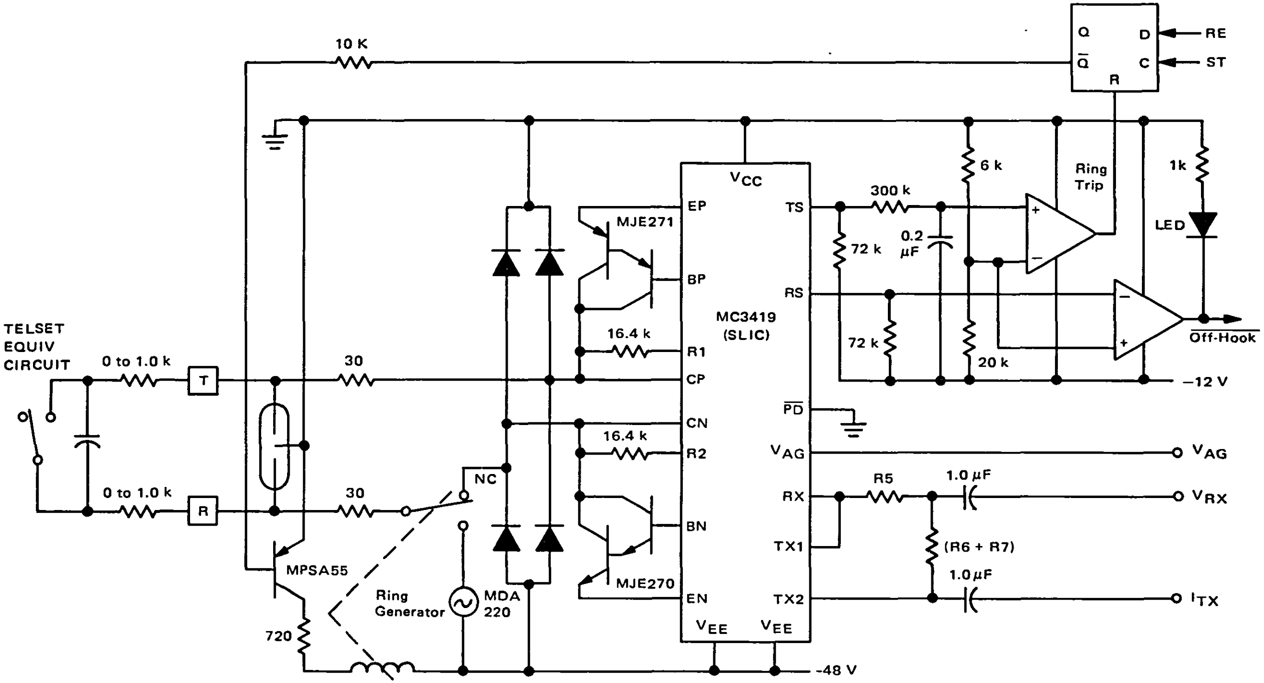


FIGURE 7 — MOTOROLA 3-CHIP SUBSCRIBER CHANNEL UNIT

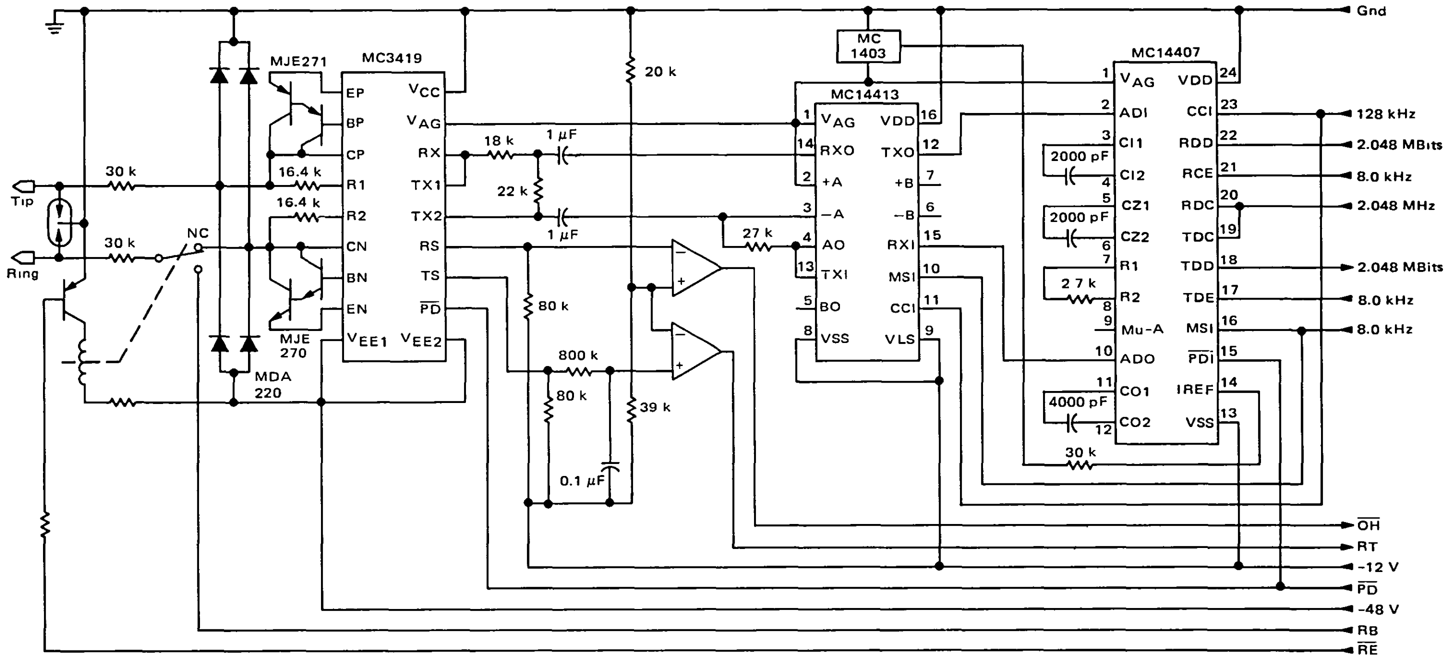
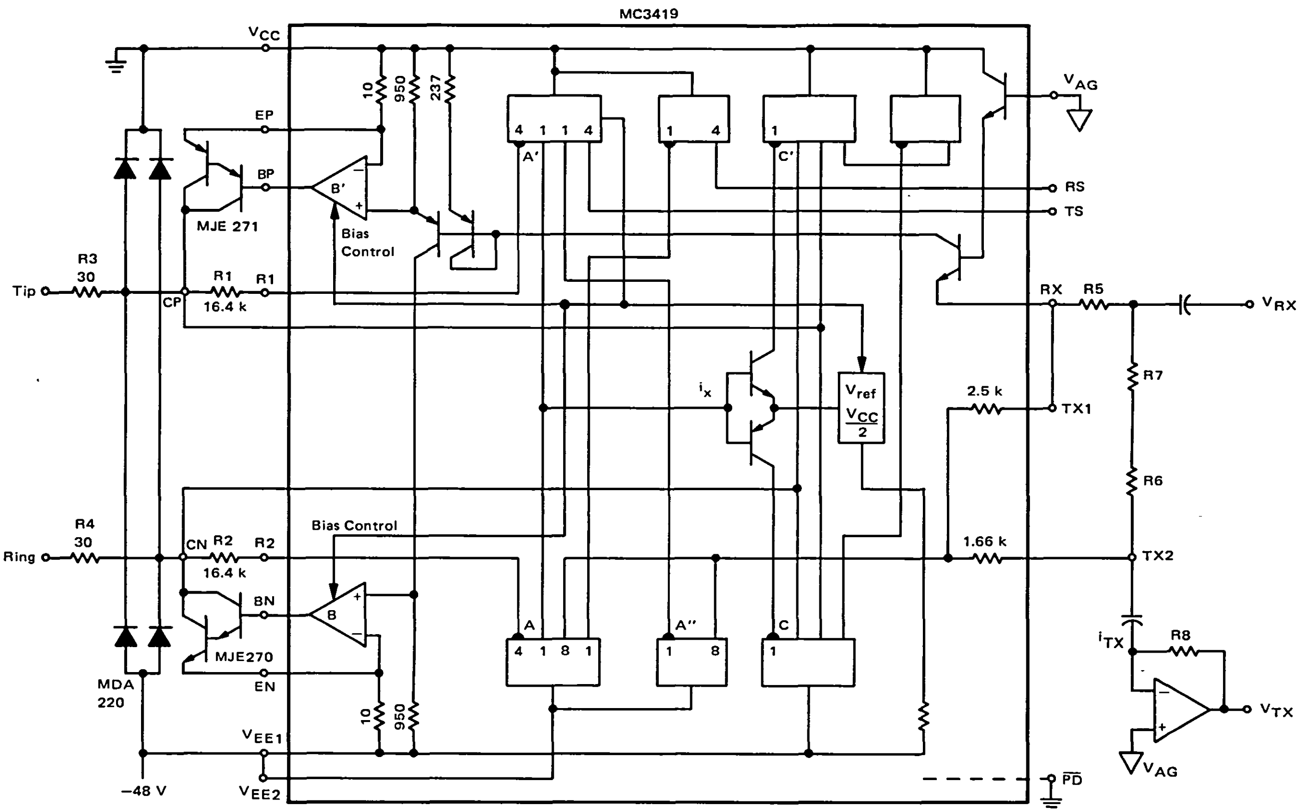


FIGURE 8 – SUBSCRIBER LOOP INTERFACE CIRCUIT, MC3419



NOTE: The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

DESCRIPTION OF MC3419 SUBSCRIBER LOOP INTERFACE CIRCUIT

Figure 8 depicts a complete subscriber loop interface circuit for standard end-office telephone loop connections. The circuit consists of an 18 pin dual in-line MC3419, MJE271 PNP and MJE270 NPN power darlington transistors, an MDA220 bridge rectifier and six resistors. This composite circuit provided the following line interface functions:

1. 2-wire balanced to 4-wire single-ended signal conversion.
2. Independent Receive Gain selection (R5).
3. Independent Transmit Gain selection (R8).
4. Independent Transhybrid null selection (R6 + R7)*
5. 600 to 900 Ω resistance ac loop termination (R1, R2, R3, R4)*.
6. Resistive dc power-feed from 400 to 800 Ω (R1, R2, R3, R4).
7. Ring to ground, Tip to ground, Ring and Tip to ground fault current limiting (10 mA).
8. Rejection of longitudinal or common mode interference from 50 to 3400 Hz (30 mA RMS).
9. 1500 volt secondary lightning protection.
10. Temporary power line fault protection.
11. Proportional ring current sense indication in RS.
12. Proportional tip current sense indication in TS.
13. Suppression of longitudinal component in RS and TS normal connections.
14. Independent 4-wire common input for noise isolation.
15. Independent quiet battery supply input for battery noise rejection.
16. Near zero power dissipation in normal on-hook condition.
17. Level linearity of better than 0.1 dB over the entire level and frequency range.

*Reflected complex impedances may also be provided with an additional capacitor.

DC CHARACTERISTICS

The first function the SLIC must perform is to enable and disable itself on the basis of the switch-hook condition in the attached instrument. With the station on-hook, the Ring and Tip terminals are open. No metallic current can flow in resistors R1 and R2, thus the input and various outputs of circuit A and A' are zero. The control outputs of A and A' are off, causing the op amps B and B' and the voltage reference to have no bias. The reference pull down resistor pulls the reference voltage to V_{EE}. No current flows in any part of the circuit if the Tip and Ring terminals are open. The power dissipation in this state is back bias leakage only.

When a load resistance (R_L) is connected to Tip and Ring, the dc current flows in R1, R2, and circuits A and A', The control outputs, op amps B, B', and the voltage reference are now on. The current gain of circuit A and A' to the TX outputs is K2 = 4. The current gain of circuits B and B' is K1 = 23.75. For a current in R1 and R2 of I_N, the current in the collector of circuits B and B' is $K1K2I_N$. The total current in the load is $(1+K1K2)I_N$. The dc feed resistance at the Tip and Ring terminals is

$$R_f = \frac{(R1 + R2)}{1+K1K2} + R3 + R4$$

The current which flows in the load will be:

$$I_{Loop} = \frac{V_{CC} - V_{EE2}}{R_L + R_f}$$

The dc feed current is thus determined by the loop resistance.

The dc component of i_x is a measure of the mismatch between the source and the sink current of the various differential stages. Circuit C and C' source or sink current through CN and CP until the dc component of $i_x = 0$. C and C' also keep the mid-point voltage of the load at $V_{CC}/2$. Thus, with a metallic current in the load, the SLIC supplies current to the load with impedance R_f.

Various fault dc conditions must be accounted for in practice. The Tip and Ring leads can be shorted to ground in the field in any combination. The SLIC limits these fault currents by the arrangement of the control outputs of circuit A and A'. If the Ring lead is tied to ground, a current through R2 will turn on the control output of circuit A. This enables op amp B' and provides a sinking path for the voltage reference. If the Tip lead is open or connected to ground, the current in R1 is zero. The i_x control lead is sinking current but cannot turn on circuit C' because the voltage reference is V_{EE}. Circuit B is also off since the control output of circuit A' is off. The current in the Ring lead is now $[(V_{CC}\text{-}V_{EE})/(R4 + R2)]$. The Ring fault current in the SLIC is less than 10 mA.

SMALL SIGNAL AC CHARACTERISTICS

With a load R_L applied across Tip and Ring, the flow of metallic current in R_L enables and biases the SLIC circuit. Now consider an ac generator in series with R_L causing differential signal across Ring and Tip at a frequency between 300 and 3400 Hz. The impedance presented to the generator is $R_L + R_o$ where R_o is the ac input impedance of the SLIC at the two-wire part. R_o is derived by a method similar to R_f.

The gain of circuits A, A', B, and B' is K1 = 4 and K2 = 23.75 as before. However, the TX2 path to i_{TX} is an added load for ac signals and the current returned to R_X is divided by the current divider of 2.5 kΩ and 1.66 kΩ. As connected, the ratio of these resistors creates another constant K5 = 0.4. (TX1 and TX2 connection can be reversed to produce K5' = 0.6).

The ac termination is thus:

$$R_f = \frac{R1 + R2}{1+K1K2K5} + R3 + R4$$

The ac current in SLIC is then

$$i_g = \frac{v_g}{R_L + R_o} \quad \text{where } v_g \text{ is the generator voltage.}$$

The current in R1 and R2 is given by $\dfrac{i_g}{1+K1K2K5}$

and the output signal current is

$$i_{TX} = \frac{K1(1\text{-}K5)}{i_g\,(1+K1K2K5)} \quad \text{thus}$$

$$\frac{V_{TX}}{v_g} = \frac{K1(1\text{-}K5)}{1+K1K2K5}\left(\frac{R8}{R_L + R_o}\right)$$

The differential signal in the load is input, as two out of phase signals, into circuits A' and A. The A' signal is inverted and summed in phase with the output of A in A''. The transmit gain voltage of the SLIC can be set at any arbitrary value by selecting R8.

Now assume a two-wire load R_L and a generator v_g at V_{RX}. The generator sees a low impedance at R_X, assuming V_{AG} is connected to a dc potential.The current into R_X is simply $i_{RX} = v_g/R5$.

This current is multiplied by K1 in circuits B and B'. The output transistors drive a load R_L + R3 + R4 in parallel with (R1+R2)/(1+K1K2K5) so that the voltage gain from V_{RX} to Tip and Ring is

$$\frac{V_{RL}}{V_{RX}} = \text{-}K2\,\frac{R_L}{R5} \times C_1 \text{ where}$$

$$C_1 = \left[\frac{R1 + R2}{(R1+R2)+(R_L+R3+R4)(1+K1K2K5)}\right]$$

The signal current across the load is in phase with V_{RX} and out of phase with the termination R_o. The current in R_o causes a signal at i_{TX}.

This current may be cancelled for any load R_L by selecting the sum of (R6 + R7).

Balance is achieved for a load R_L by designing

$$(R6 + R7) = \frac{R5(1+K1K2K5)}{K1K2(1\text{-}K5)} \times C_2 \text{ where}$$

$$C_2 = \left[\frac{(R1+R2) + (R_L+R3+R4)(1+K1K2K5)}{R1 + R2}\right]$$

The current amplifiers within the SLIC are all wide-band amplifiers such that essentially no group delay occurs for 4 kHz band limited signals and resistive loads. Thus, the SLIC functions as a near ideal transimpedance converter for ports V_{RX},V_{RL}, and V_{TX}. Complex loads Z_L may be balanced by replacing (R6 + R7) with a complex balance network z.

LONGITUDINAL SIGNAL SUPPRESSION

Both low frequency and voice-band longitudinal rejection are produced by the same mechanisms within this SLIC.

A longitudinal interference from 0 to 3400 Hz in the loop produces a common mode voltage at Ring and Tip. Circuit A and A' sense these in phase currents in R1 and R2 and cause an ac signal i_x. Circuit C and C' are driven by the Class B transistor pair to produce currents which will reduce the common mode component at nodes CN and CP by the open loop ac gain of the circuit C and C'. The high compliance of the i_x output and a large current gain in circuit C and C' allow the open loop gain to be quite large.

Constants K1, K2 are held in close tolerance within the integrated circuit. If R1 + R3 = R2 + R4, then the longitudinal balance at Tip and Ring will be good. Thus, the remaining component of common mode signal at CP and CN will be equal. The phase inversion in A'' will cause the common mode remainder to sum out of phase at TX2 and thus will contribute little output at V_{TX}. The overall performance of this common mode rejection loop is determined by the matching of R1 + R3 and R4 + R2, as well as the matching of constants within the chip. 60 dB appears readily achievable.

The circuit C and C' outputs are limited to 30 mA to insure longitudinal capacity for both the IEEE and REA standards.

LOOP CONDITION SENSING

Three analog sensing outputs are provided for detecting the condition of the subscriber loop. Each output consists of the open collector of a current sourcing device. The RS and TS outputs are derived from the sense currents in circuits A and A'. Thus, in a normal metallic connection the TS and RS currents are related to Ring and Tip currents by constants.

<u>DC Metallic</u>

$$I_{RS} = \frac{I_R}{1+K1K2} = \frac{V_{CC}\text{-}V_{EE}}{(R_L + R_f)(1+K1K2)}$$

$$I_{TS} = \frac{I_T}{1+K1K2} = \frac{V_{CC} - V_{EE}}{(R_L+R_f)(1+K1K2)}$$

AC Metallic

$$i_{RS} = \frac{V_{RL}}{(R_L+R_o)(1+K1K2K5)}$$

$$i_{TS} = \frac{V_{RL}}{(R_L+R_o)(1+K1K2K5)}$$

Note that if the current has a metallic path from Tip to Ring, but also an unbalanced load to ground in Ring or Tip, that the RS current will be proportional to the Ring current and the TS current will be proportional to the Tip current. Second party detection and ground start detection can be handled using this feature. Providing a metallic path does exist, the longitudinal component in RS and TS will be suppressed in RS and TS by circuit C and C′. With no metallic connection, circuit B and B′ are off such that the longitudinal impedance is R1 + R3 and the induced current from a given source will be decreased by 1 + K1K2. In this case, the longitudinal current will produce peak outputs at RS and TS which are less than the average output of a long-loop metallic current.

The longitudinal sense output provides a full-wave rectified current proportional to the longitudinal loop current once metallic connection has been established. Simple filtering of this lead can produce a dc measure of the longitudinal status of an operating loop. Excessive longitudinal current can produce a fault indication.

NOISE AND POWER SUPPLY REJECTION

The main 48-volt battery in a large office can supply considerable power but is often quite noisy and difficult to filter. Without a means of rejecting supply noise, the channel to channel crosstalk can also become excessive. In this SLIC, two V_{EE} pins are provided to allow for quiet battery and power battery connection. Circuits A and A′ support the sensing resistors and control all other current in the SLIC. If the voltage across V_{CC} and V_{EE2} is filtered, noise at V_{CC} will not effect the performance of the loop. In a short circuit condition, the V_{EE} current will be about 130 mA while the V_{EE2} current is 3 mA. It is, therefore, possible to supply V_{EE2} from a far quieter supply.

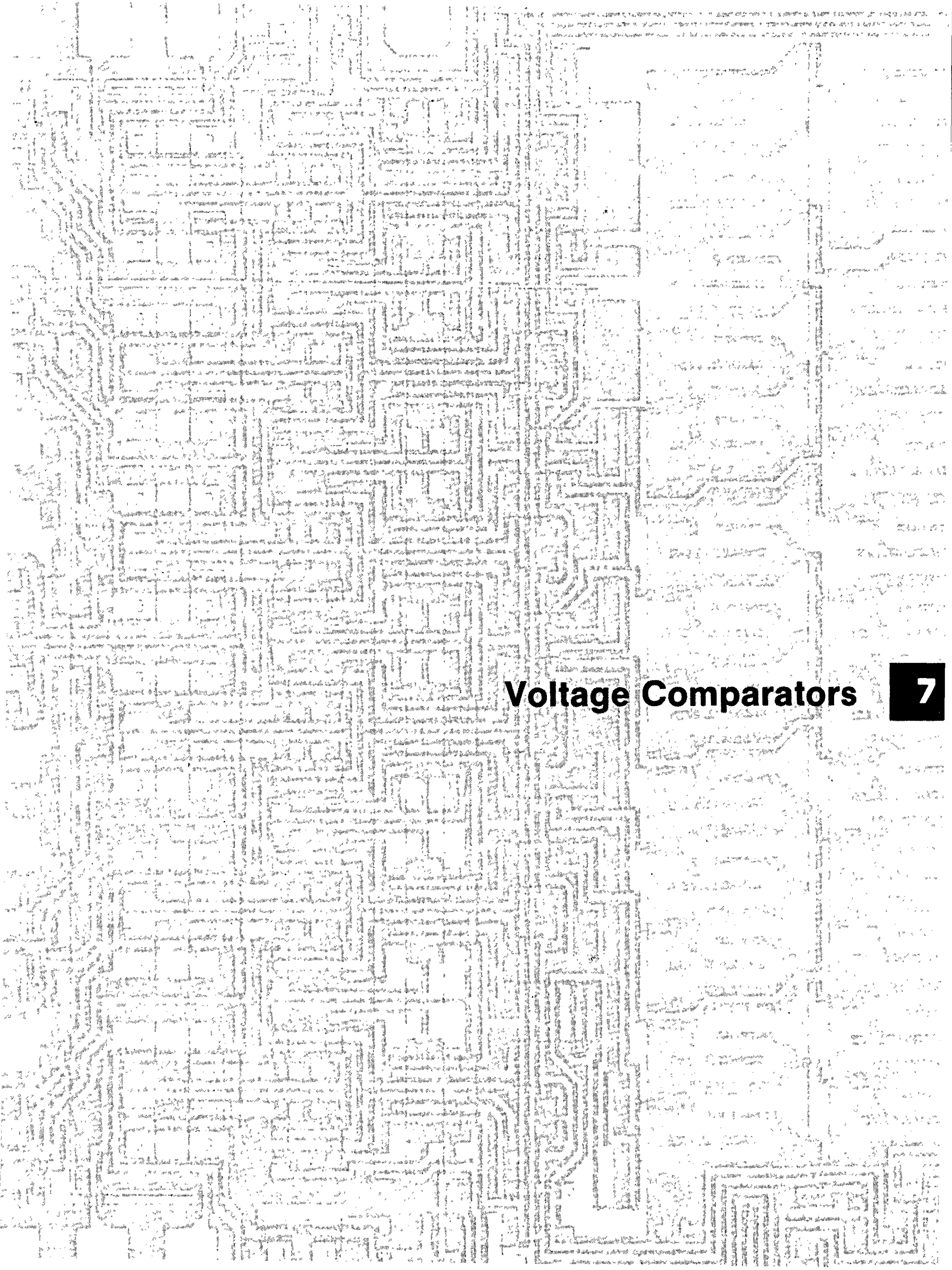
Furthermore, an analog ground input (V_{AG}) is provided to allow for proper noise grounding for the V_{RX} and V_{TX} terminals. The true input signal is the ac voltage between V_{AG} and V_{RX}. The true output voltage should be taken between V_{AG} and V_{TX}.

PROTECTION

Two types of electrical hazards can be expected at the Ring and Tip terminals of the SLIC. Transient currents caused by electrical storms and power line cross connects during installation and maintenance. The diode bridge, coupled with R3 and R4, provide this protection. Ring and Tip are normally protected by a gas tube or carbon blocks against the primary effects of a near lightning strike. The SLIC itself must provide secondary protection for 1500-volt transients. A transient voltage at Ring or Tip will turn on one of the four diodes. The resistors limit the maximum current to 50 amps, which is the rated surge current of the diodes. A typical turn on time of 200 ns is readily achievable with silicon rectifiers.

Power line faults from 120-volt lines will be half-wave rectified by the upper and lower pair resulting in a current of 2 amp RMS in each with 30 ohm source resistors.

Extended short circuit conditions will cause R3 and R4 to burn open, eliminating the fault and causing no further damage. The externalization of the R3 and R4 resistors from the SLIC's feedback loop is a critical step in providing sufficient electrical hazard protection.



Voltage Comparators

7

VOLTAGE COMPARATORS

*Industrial

MOTOROLA

LM111
LM211
LM311

HIGHLY FLEXIBLE VOLTAGE COMPARATORS

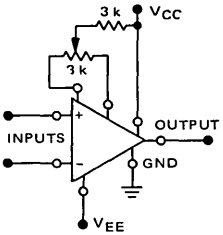
The ability to operate from a single power supply of 5.0 to 30 volts or ±15-volt split supplies, as commonly used with operational amplifiers, makes the LM111 / LM211 / LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive MDTL, MRTL, MTTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the LM111 / LM211 / LM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

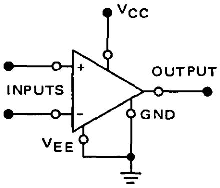
SILICON MONOLITHIC INTEGRATED CIRCUIT

SUGGESTED COMPARATOR DESIGN CONFIGURATIONS

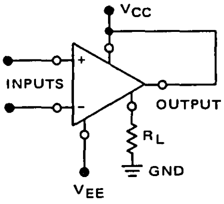
SPLIT POWER-SUPPLY with OFFSET BALANCE



SINGLE SUPPLY

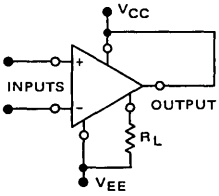


GROUND-REFERRED LOAD



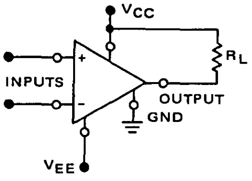
Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to NEGATIVE SUPPLY

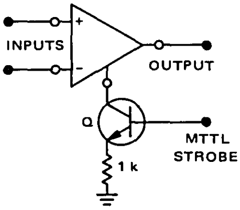


Input polarity is reversed when GND pin is used as an output.

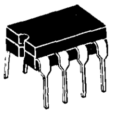
LOAD REFERRED to POSITIVE SUPPLY

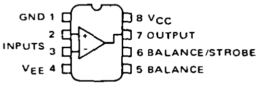


STROBE CAPABILITY



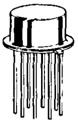
J-8 SUFFIX
CERAMIC PACKAGE
CASE 693

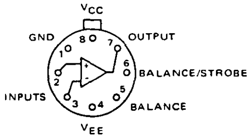




(Top View)

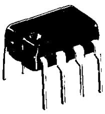
H SUFFIX
METAL PACKAGE
CASE 601

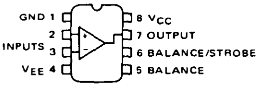




(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM311 Only)





(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value LM111 LM211	Value LM311	Unit
Total Supply Voltage	$V_{CC} + \lvert V_{EE} \rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (See Note 1)	V_{in}	±15	±15	Vdc
Power Dissipation (Pkg Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic* and Ceramic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Ambient Temperatures Range	T_A			°C
LM111		-55 to +125	–	
LM211		-25 to +85	–	
LM311		–	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

*LM311N only is available in the plastic dual in-line package.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	LM111 LM211 Min	Typ	Max	LM311 Min	Typ	Max	Unit
Input Offset Voltage (See Note 2.)	$\lvert V_{IO} \rvert$							mV
$R_S \leqslant 50\ k\Omega$, T_A = +25°C		–	0.7	3.0	–	2.0	7.5	
$R_S \leqslant 50\ k\Omega$, $T_{low}^* \leqslant T_A \leqslant T_{high}^*$		–	–	4.0	–	–	10	
Input Offset Current (See Note 2.)	$\lvert I_{IO} \rvert$							nA
T_A = +25°C		–	4.0	10	–	6.0	50	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	60	100	–	100	250	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	150	–	–	300	
Voltage Gain	A_V	–	200	–	–	200	–	V/mV
Response Time (See Note 3.)	t_{TLH}	–	200	–	–	200	–	ns
Saturation Voltage	V_{OL}							V
T_A = +25°C, $V_{ID} \leqslant -5.0$ mV, I_O = 50 mA		–	0.75	1.5	–	–	–	
$V_{ID} \leqslant -10$ mV, I_O = 50 mA		–	–	–	–	0.75	1.5	
$T_{low} \leqslant T_A \leqslant T_{high}$, $V_{CC} \geqslant 4.5$ V, V_{EE} = 0								
$V_{ID} \leqslant -6.0$ mV, $I_{sink} \leqslant 8.0$ mA		–	0.23	0.4	–	–	–	
$V_{ID} \leqslant -10$ mV, $I_{sink} \leqslant 8.0$ mA		–	–	–	–	0.23	0.4	
Strobe "On" Current	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current	I_{OL}							
T_A = +25°C, $V_{ID} \geqslant 5.0$ mV, V_O = 35 V		–	0.2	10	–	–	–	nA
$V_{ID} \geqslant 10$ mV, V_O = 35 V		–	–	–	–	0.2	50	nA
$T_{low} \leqslant T_A \leqslant T_{high}$, $V_{ID} \geqslant 5.0$ mV, V_O = 35 V		–	0.1	0.5	–	–	–	µA
Input Voltage Range	V_{IR}							V
$T_{low} \leqslant T_A \leqslant T_{high}$		–	±14	–	–	±14	–	
Positive Supply Current	I_{CC}	–	+5.1	+6.0	–	+5.1	+7.5	mA
Negative Supply Current	I_{EE}	–	-4.1	-5.0	–	-4.1	-5.0	mA

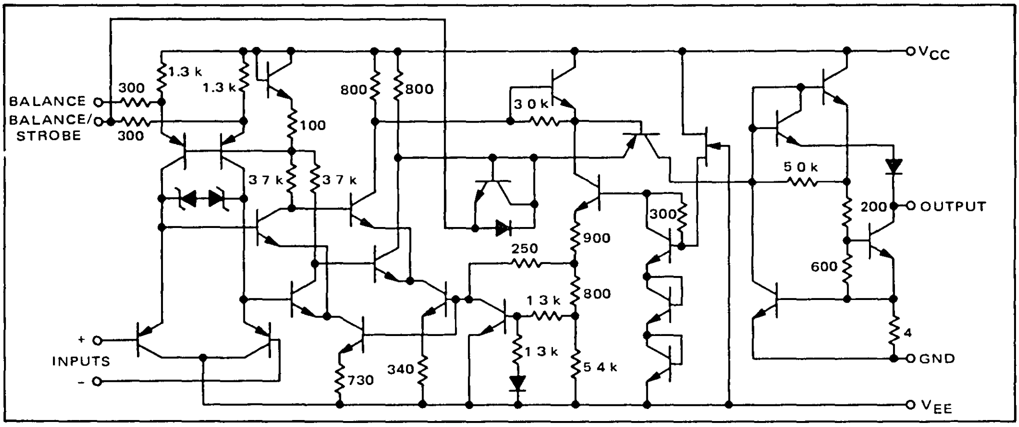
*T_{low} = -55°C for LM111	T_{high} = +125°C for LM111
= -25°C for LM211	= +85°C for LM211
= 0 for LM311	= +70°C for LM311

Note 1. This rating applies for ±15-volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.

Note 2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0-mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.

Note 3. The response time specified is for a 100-mV input step with 5.0-mV overdrive.

FIGURE 1 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 2 – INPUT BIAS CURRENT and INPUT OFFSET CURRENT versus TEMPERATURE

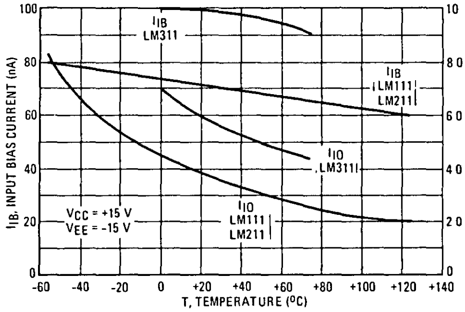


FIGURE 3 – COMMON-MODE LIMITS versus TEMPERATURE

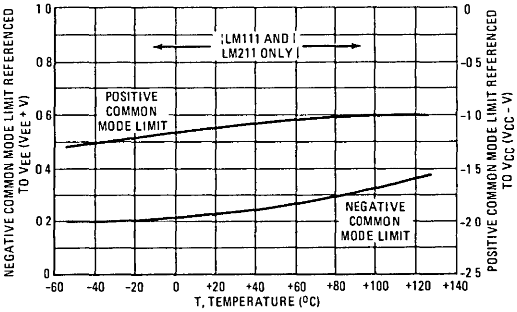


FIGURE 4 – OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT

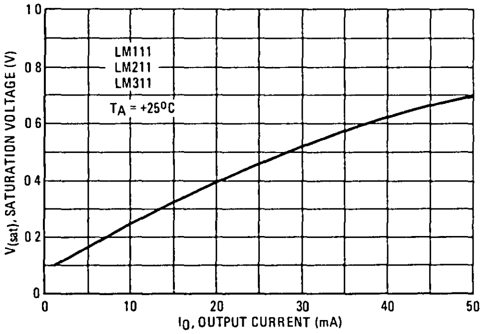
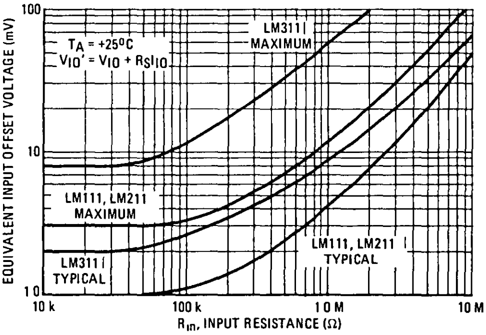


FIGURE 5 – EQUIVALENT OFFSET ERROR versus INPUT RESISTANCE



APPLICATIONS INFORMATION

FIGURE 6 – ZERO-CROSSING DETECTOR DRIVING MOS LOGIC

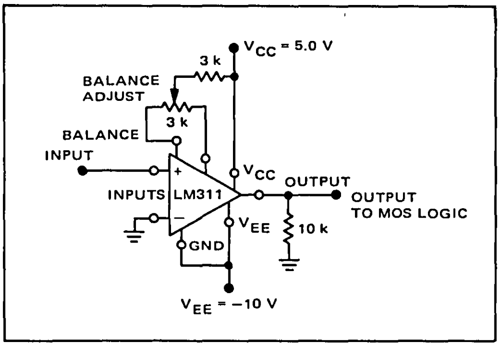
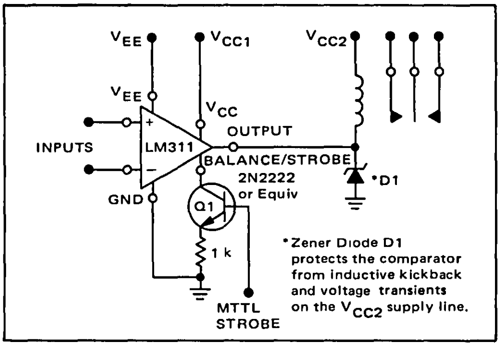


FIGURE 7 – RELAY DRIVER WITH STROBE CAPABILITY



*Zener Diode D1 protects the comparator from inductive kickback and voltage transients on the V_{CC2} supply line.

LM139 LM139A
LM239 LM239A
LM339 LM339A

MOTOROLA

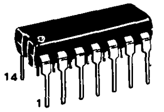
QUAD SINGLE-SUPPLY COMPARATORS

These comparators are designed for use in level detection and low-level sensing applications in Consumer, Automotive and Industrial electronic applications.

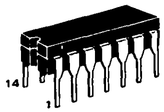
- Power Supply Options –
  Single Supply = 2.0 to 36 Vdc
  Split Supplies = ± 1.0 -±18 Vdc
- Wide Operating Temperature Range – -55 to +125°C
- Low Supply Current Drain – 2.0 mA (Max)
- Low Input Biasing Current – 25 nA (Typ)
- Low Input Offset Voltage – 5.0 mV (Max) LM139, 239, 339
  2.0 mV (Max) LM139A, 239A, 339A
- TTL and CMOS Compatible

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 646
LM239/239A,
LM339/339A only



J SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ T_A = 25°C	P_D		
Ceramic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Plastic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A		°C
LM139, 139A		-55 to +125	
LM239, 239A		-40 to +85	
LM339, 339A		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS

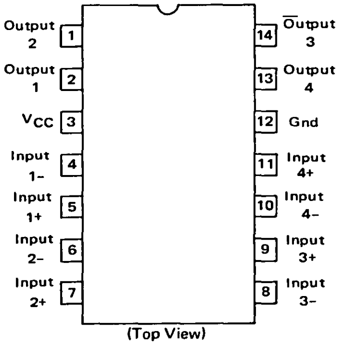
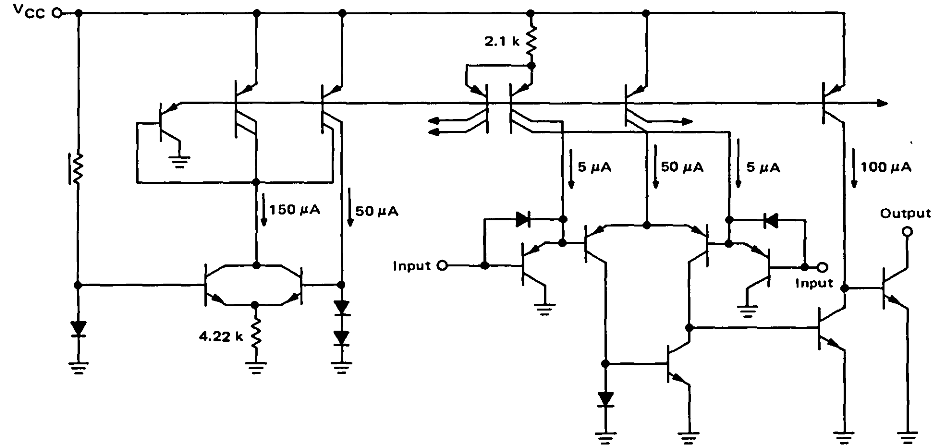


FIGURE 1 – CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



ELECTRICAL CHARACTERISTICS (V_{CC} = +5 0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	LM139, A			LM239, A			LM339, A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = 1.4 Vdc, V_O = 1.4 Vdc, R_S = 0) LM139, 239, 339 LM139A, 239A, 339A	V_{IO}	 – –	 ±2.0 ±1.0	 ±5 0 ±2.0	 – –	 ±2 0 ±1.0	 ±5.0 ±2.0	 – –	 ±2.0 ±1.0	 ±5.0 ±2.0	mVdc
Input Offset Current	I_{IO}	–	±3 0	±25	–	±5.0	±50	–	±5 0	±50	nA
Input Bias Current	I_{IB}	–	25	100	–	25	250	–	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	V
Supply Current (R_L = ∞)	I_{CC} I_{EE}	–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	mA
Response Time (Note 2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1 3	–	–	1 3	–	–	1.3	–	μs
Output Sink Current ($V_{I(-)} \geqslant$ +1.0 Vdc, $V_{I(+)}$ = 0, $V_O \leqslant$ +1.5 Vdc) ($V_{I(-)} \geqslant$ +1 0 Vdc, $V_{I(+)}$ = 0, $V_O \leqslant$ 500 mVdc)	I_{sink}	 6 0 6 0	 16 –	 – –	 6.0 6.0	 16 –	 – –	 6.0 6.0	 16 –	 – –	mA
Saturation Voltage ($V_{I(-)} \geqslant$ +1.0 Vdc, $V_{I(+)}$ = 0, $I_{sink} \leqslant$ 4.0 mAdc) ($V_{I(-)} \geqslant$ +1.0 Vdc, $V_{I(+)}$ = 0, $I_{sink} \leqslant$ 6.0 mAdc)	V_{sat}	 – –	 – –	 400 500	 – –	 – –	 400 500	 – –	 – –	 400 500	mV
Voltage Gain (V_{CC} = 15 V) ($R_L \geqslant$15 kΩ) LM139, 239, 339 LM139A, 239A, 339A	A_V	 – 50	 200 200	 – –	 – 50	 200 200	 – –	 – 50	 200 200	 – –	k
Output Leakage Current ($V_{I(+)} \geqslant$ +1.0 Vdc, $V_{I(-)}$ = 0, V_O = 5.0 Vdc)	I_{OL}	–	0.1	–	–	0.1	–	–	0 1	–	μA

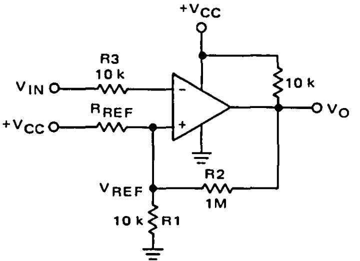
PERFORMANCE CHARACTERISTICS – Guaranteed Over Temperature Range (V_{CC} = +5.0 Vdc)

Characteristic	Symbol	-55 to +125°C			-40°C to +85°C			0° to 70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = +1.4 Vdc, V_O = 1.4 Vdc, R_S = 0) LM139, 239, 339 LM139A, 239A, 339A	V_{IO}	 – –	 – –	 ±9 0 ±4.0	 – –	 – –	 ±9 0 ±4 0	 – –	 – –	 ±9.0 ±4.0	mV
Input Offset Current	I_{IO}	–	–	±100	–	–	±150	–	–	±150	nA
Input Bias Current	I_{IB}	–	–	300	–	–	400	–	–	400	nA
Input Common Mode Voltage Range	V_{ICR}	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	Vdc
Saturation Voltage ($V_{I(-)} \geqslant$ 1.0 Vdc, $V_{I(+)}$ = 0, $I_{sink} \leqslant$ 4.0 mAdc)	V_{sat}	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current ($V_{I(+)} \geqslant$ 1.0 Vdc, $V_{I(-)}$ = 0, V_O = 30 Vdc)	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	μA
Input Differential Voltage (All $V_I \geqslant$ 0 Vdc)	V_{ID}	–	–	36	–	–	36	–	–	36	Vdc

Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is V_{CC} -1.5 V, but either or both inputs can go to +30 Vdc without damage.

2. The response time specified is for a 100 mV input step with 5 mV overdrive For larger signals, 300 ns is typical.

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

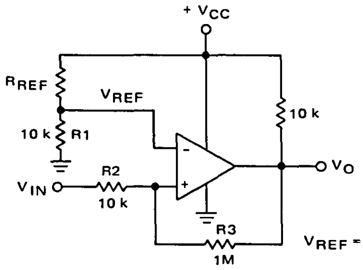


$$V_{REF} \approx \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R3 \simeq R1 \,//\, R_{REF} \,//\, R1$$

$$V_H = \frac{R1//R_{REF}}{R1//R_{REF} + R2}\ (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R2 \approx R1//R_{REF}$$

Amount of Hysteresis V_M

$$V_H = \frac{R2}{R2 + R3}\ (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 4 — NORMALIZED INPUT OFFSET VOLTAGE

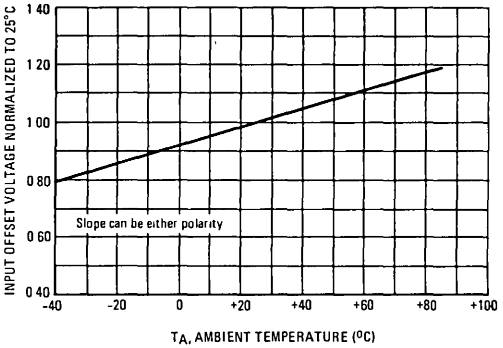


FIGURE 5 — INPUT BIAS CURRENT

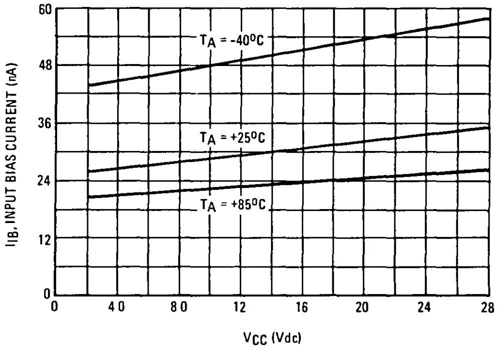


FIGURE 6 — NORMALIZED INPUT OFFSET CURRENT

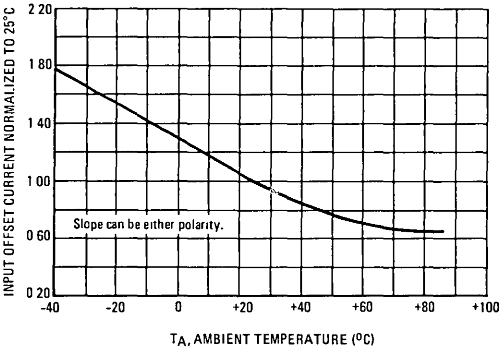


FIGURE 7 — OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

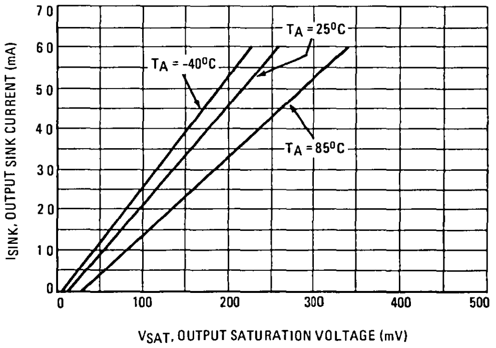
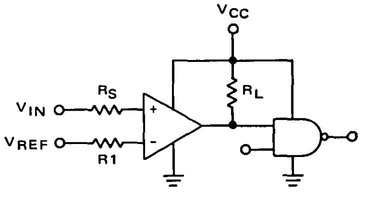


FIGURE 8 — DRIVING LOGIC



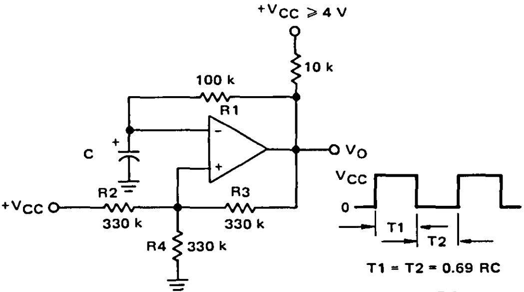
1/4 LM139, 139A

R_S = Source Resistance

R1 ≈ R_S

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 — SQUAREWAVE OSCILLATOR



T1 = T2 = 0.69 RC

$f \approx \frac{7.2}{C(\mu F)}$

R2 = R3 = R4

R1 ≈ R2//R3//R4

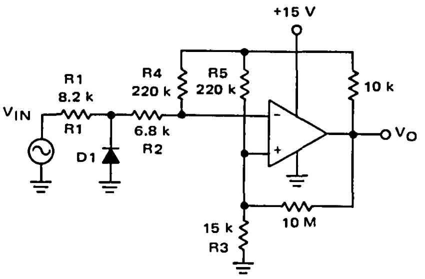
APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practive to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −300 mV should not be used.

FIGURE 10 – ZERO CROSSING DETECTOR
(Single Supply)



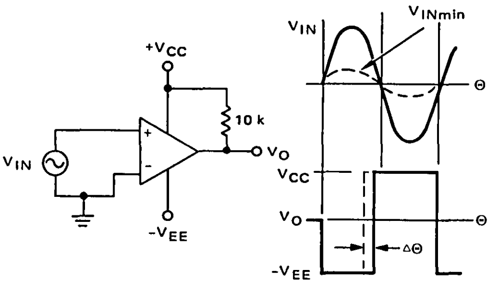
D1 prevents input from going negative by more than 0.6 V.

R1 + R2 = R3

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 11 – ZERO CROSSING DETECTOR
(Split Supplies)

V_{INmin} ≈0.4 V peak for 1% phase distortion (ΔΘ).



MOTOROLA

LM2901N

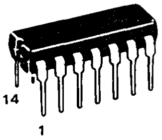
QUAD SINGLE-SUPPLY COMPARATOR

This comparator is designed for use in level detection and low-level sensing applications in Consumer, Automotive and Industrial electronic applications.

- Power Supply Options –
  - Single Supply = 2.0 to 36 Vdc
  - Split Supplies = ±1.0 to ±18 Vdc
- Wide Operating Temperature Range – -40 to +85°C
- Low Supply Current Drain – 2 0 mA (Max)
- Low Input Biasing Current – 25 nA (Typ)
- Low Input Offset Voltage – 2.0 mV (Max)
- TTL and CMOS Compatible

QUAD COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0 3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ T_A = 25°C	P_D		
Plastic Package		1 25	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS

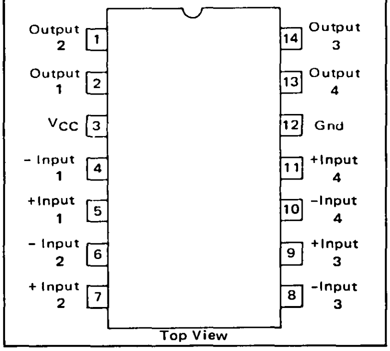
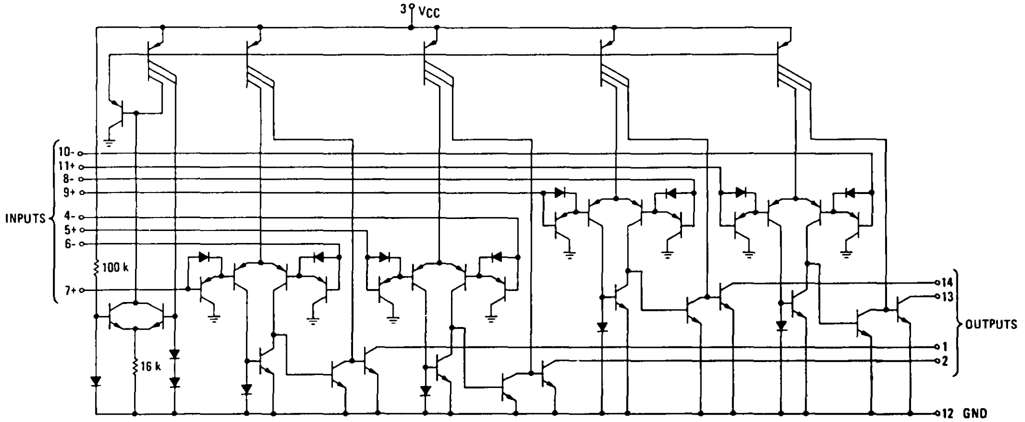


FIGURE 1 – CIRCUIT SCHEMATIC



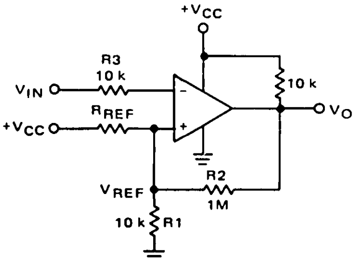
ELECTRICAL CHARACTERISTICS (V_{CC} = +5 0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{ref} = 1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	2.0	7.0	mVdc
Input Offset Current	I_{IO}	–	±5.0	±50	nA
Input Bias Current	I_{IB}	–	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	–	V_{CC} −1.5	V
Supply Current ($R_L = \infty$)	I_{CC} I_{EE}	–	0 8	2.0	mA
Response Time (Note 2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	μs
Output Sink Current ($V_{I(-)} \geqslant$ +1.0 Vdc, $V_{I(+)}$ = 0, $V_O \leqslant$ +1.5 Vdc)	I_{sink}	6.0	16	–	mA
Saturation Voltage ($V_{I(-)} \geqslant$ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} = 4.0 mAdc)	V_{sat}	–	–	400	mV
Output Leakage Current ($V_{I(+)} \geqslant$ +1.0 Vdc, $V_{I(-)}$ = 0, V_O = 5.0 Vdc)	I_{OL}	–	0.1	–	μA

Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is V_{CC} −1.5 V, but either or both inputs can go to +30 Vdc without damage.

2. The response time specified is for a 100 mV input step with 5 mV overdrive. For large signals, 300 ns is typical.

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

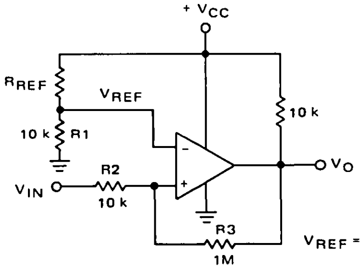


$$V_{REF} \approx \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R3 \simeq R1 \,//\, R_{REF} // \,R1$$

$$V_H = \frac{R1//R_{REF}}{R1//R_{REF} + R2} \quad (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R2 \approx R1//R_{REF}$$

Amount of Hysteresis V_M

$$V_H = \frac{R2}{R2 + R3} \; (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – NORMALIZED INPUT OFFSET VOLTAGE

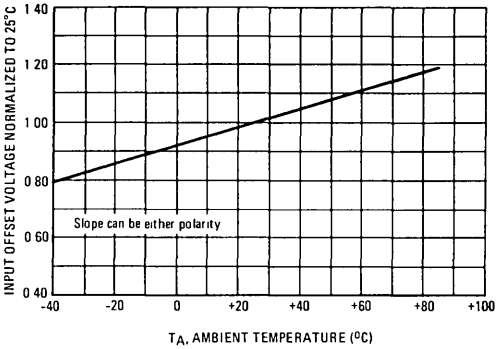


FIGURE 5 – INPUT BIAS CURRENT

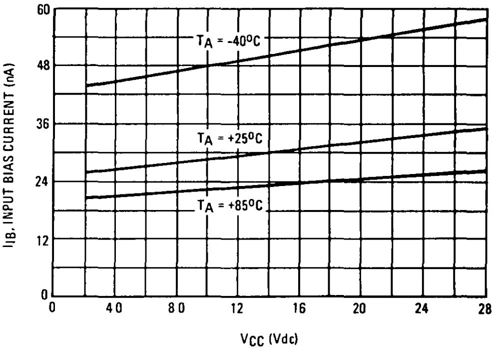


FIGURE 6 – NORMALIZED OFFSET CURRENT

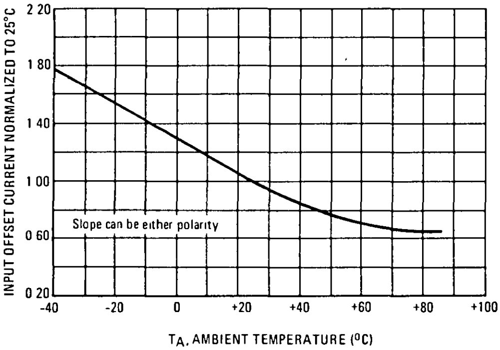


FIGURE 7 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

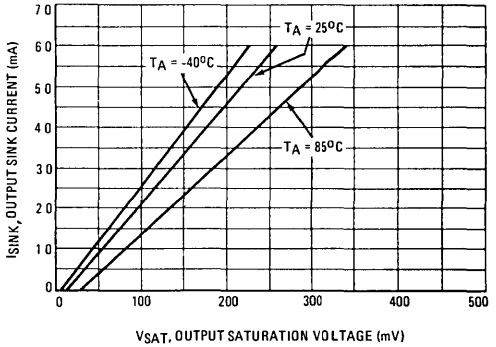
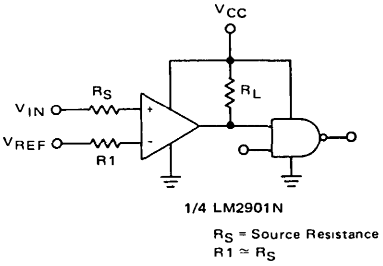
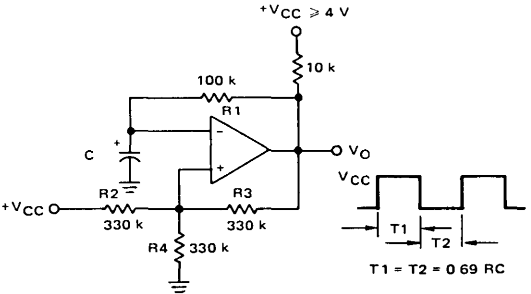


FIGURE 8 – DRIVING LOGIC



LOGIC	DEVICE	VCC Volts	RL kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 – SQUAREWAVE OSCILLATOR



T1 = T2 = 0.69 RC

$$f \approx \frac{7.2}{C(\mu F)}$$

R2 = R3 = R4

R1 ≈ R2//R3//R4

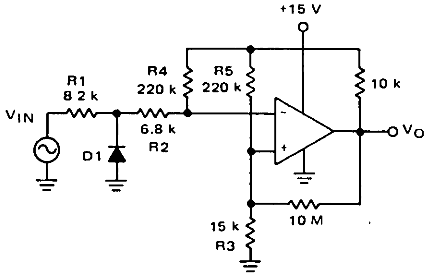
APPLICATIONS INFORMATION

The LM2901N is a quad comparator having high gain, wide bandwidth characteristics. This gives the device oscillator tendencies if the outputs capacitively couple to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should not be used. The addition of positive feedback (<10 mV) is also recommended

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

FIGURE 10 – ZERO CROSSING DETECTOR
(Single Supply)



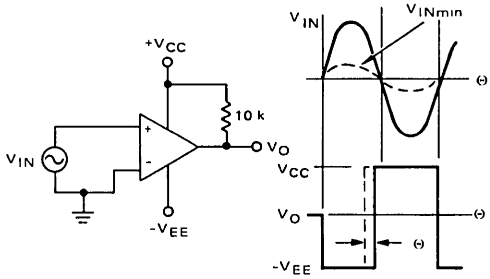
D1 prevents input from going negative by more than 0 6 V

R1 + R2 = R3

$R3 \leqslant \frac{R5}{10}$ for small error in zero crossing

FIGURE 11 – ZERO CROSSING DETECTOR
(Split Supplies)

V_{INmin} ≈0 4 V peak for 1% phase distortion (ΔΘ)



MOTOROLA

MC1414
MC1514

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
  2.8 mA Minimum (Each Comparator) for MC1514
  1.6 mA minimum (Each Comparator) for MC1414
- Differential Input Characteristics
  Input Offset Voltage = 1.0 mV for MC1514
  = 1.5 mV for MC1414
  Offset Voltage Drift = 3.0 μV/°C for MC1514
  = 5.0 μV/°C for MC1414
- Short Propagation Delay Time — 40 ns typical
- Output Compatible with All Saturating Logic Forms
  V_O = +3.2 V to -0.5 V typical

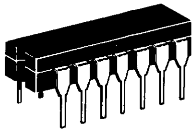
DUAL DIFFERENTIAL COMPARATOR

(DUAL MC1710)

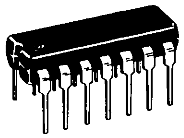
SILICON MONOLITHIC INTEGRATED CIRCUIT

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	±5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = 25°C Plastic Dual In-Line Package Derate above T_A = 25°C	P_D	 1000 6.0 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range MC1514 MC1414	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

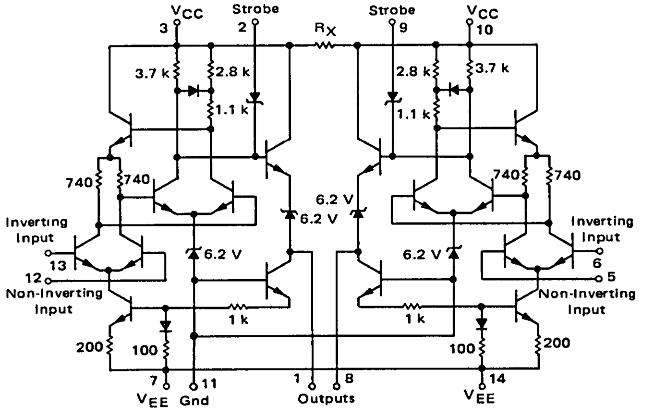


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

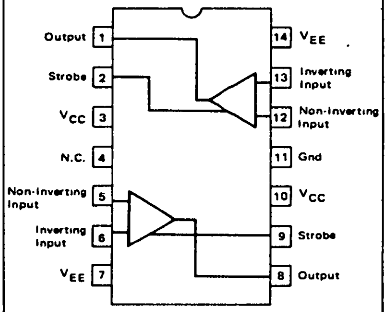


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1414 only)

CIRCUIT SCHEMATIC



R_X = Low Resistance Value, usually $<100\Omega$, not specified.



ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6 Vdc, T_A = 25°C unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514			MC1414			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}							mVdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	2.0	–	1.5	5.0	
(V_O = 1.8 Vdc, T_A = T_{low}*)		–	–	3.0	–	–	6.5	
(V_O = 1.0 Vdc, T_A = T_{high}*)		–	–	3.0	–	–	6.5	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	3.0	–	–	5.0	–	µV/°C
Input Offset Current	I_{IO}							µAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	3.0	–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	7.0	–	–	7.5	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	3.0	–	–	7.5	
Input Bias Current	I_{IB}							µAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	12	20	–	15	25	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	45	–	18	40	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	20	–	–	40	
Open Loop Voltage Gain	A_{vol}							V/V
(T_A = 25°C)		1250	1700	–	1000	1500	–	
(T_A = T_{low} to T_{high})		1000	–	–	800	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geqslant 5.0$ mV, $0 \leqslant I_O \leqslant 5.0$ mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage	V_{OL}							Vdc
($V_{ID} \geqslant -5.0$ mV, I_{OS} = 2.8 mA)		-1.0	-0.5	0	–	–	–	
($V_{ID} \geqslant -5.0$ mV, I_{OS} = 1.6 mA)		–	–	–	-1.0	-0.5	0	
Output Sink Current ($V_{ID} \geqslant -5.0$ mV, $V_{OL} \leqslant 0.4$ V, T_A = T_{low} to T_{high})	I_{OS}	2.8	3.4	–	1.6	2.5	–	mAdc
Input Common Mode Voltage Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Vdc
Common-Mode Rejection Ratio (V_{EE} = -7.0 Vdc, $R_S \leqslant 200\ \Omega$)	CMRR	80	100	–	70	100	–	dB
Strobe Low Level Current (V_{IL} = 0)	I_{IL}	–	–	2.5	–	–	2.5	mA
Strobe High Level Current (V_{IH} = 5.0 Vdc)	I_{IH}	–	–	1.0	–	–	1.0	µA
Strobe Disable Voltage ($V_{OL} \leqslant 0.4$ Vdc)	V_{IL}	–	–	0.4	–	–	0.4	Vdc
Strobe Enable Voltage ($V_{OH} \geqslant 2.4$ Vdc)	V_{IH}	3.5	–	6.0	3.5	–	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH}	–	20	–	–	20	–	ns
	t_{PHL}	–	40	–	–	40	–	
Strobe Response Time (Figure 2)	t_{so}	–	15	–	–	15	–	ns
	t_{sr}	–	6.0	–	–	6.0	–	
Total Power Supply Current, Both Comparators ($V_O \leqslant 0$)	I_{CC}	–	12.8	18	–	12.8	18	mAdc
	I_{EE}	–	11	14	–	11	14	
Total Power Consumption, Both Comparators	P_D	–	230	300	–	230	300	mW

*T_{low} = -55°C for MC1514, 0°C for MC1414
T_{high} = +125°C for MC1514, +75°C for MC1414

FIGURE 1 – PROPAGATION DELAY TIME

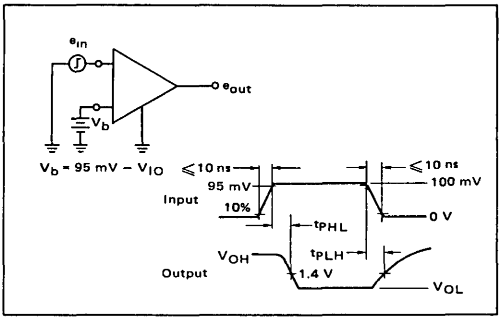
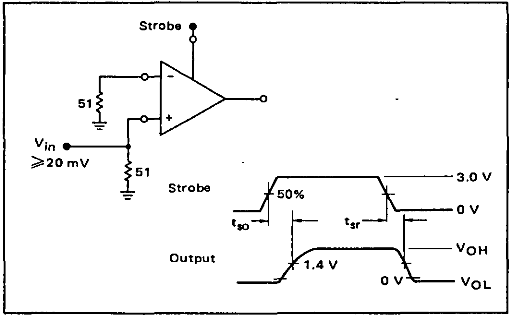


FIGURE 2 – STROBE RESPONSE TIME



TYPICAL CHARACTERISTICS

(Each Comparator)

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS

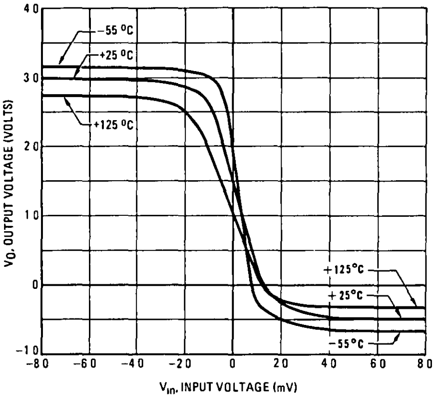


FIGURE 4 – INPUT OFFSET VOLTAGE versus TEMPERATURE

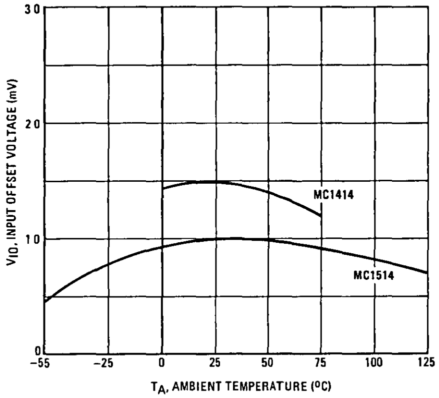


FIGURE 5 – INPUT OFFSET CURRENT versus TEMPERATURE

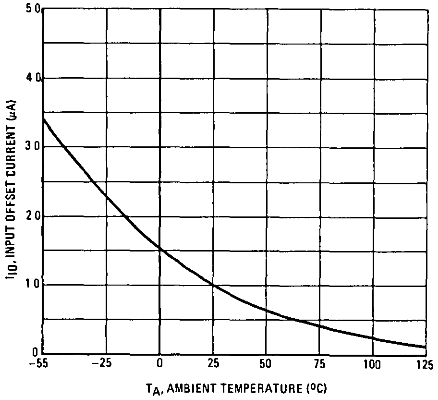


FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

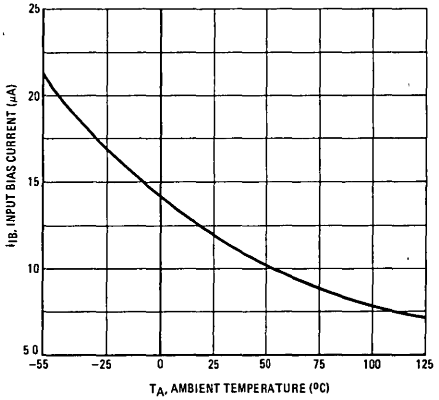


FIGURE 7 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

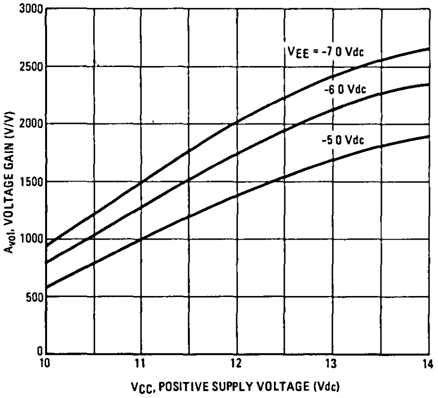


FIGURE 8 – VOLTAGE GAIN versus TEMPERATURE

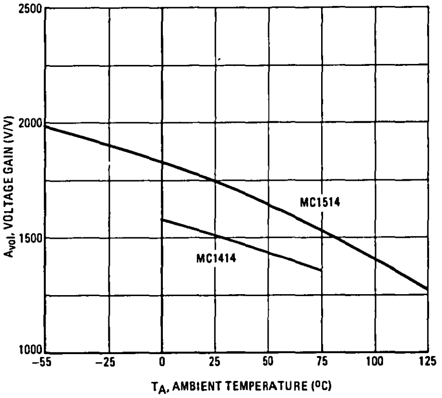


FIGURE 9 – RESPONSE TIME

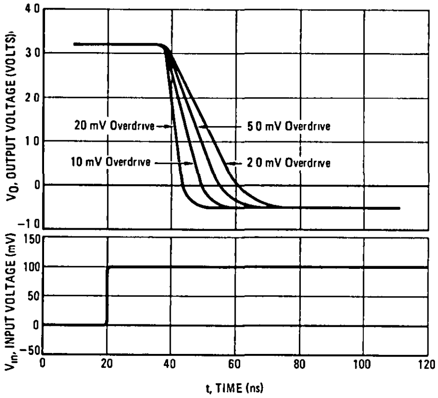


FIGURE 10 – POWER DISSIPATION versus TEMPERATURE

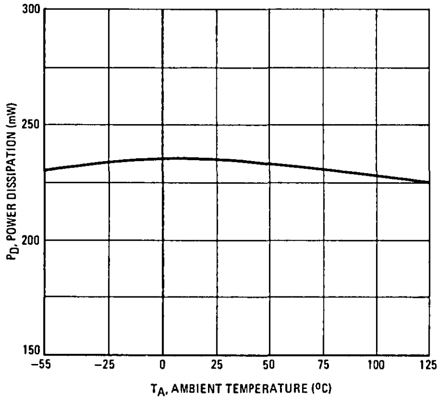


FIGURE 11 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

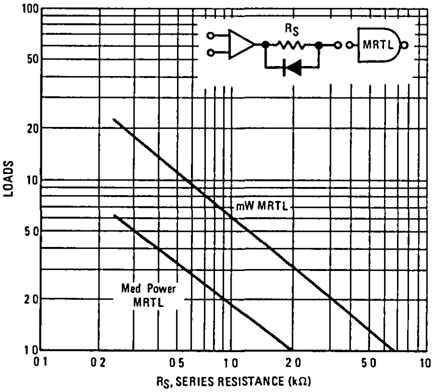


FIGURE 12 – SINK CURRENT versus TEMPERATURE

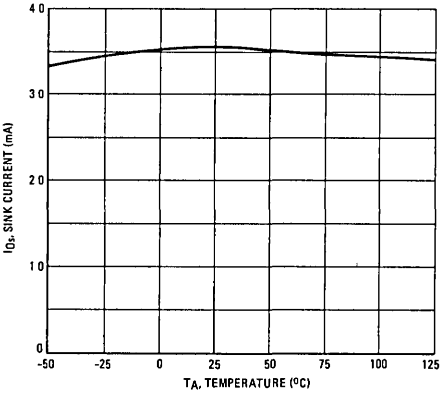
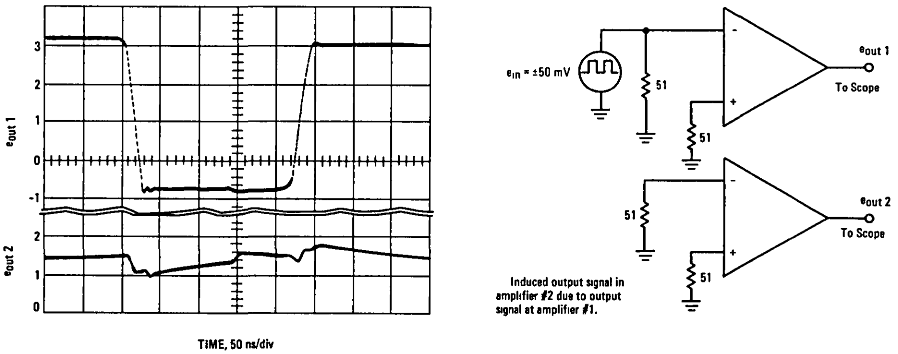


FIGURE 13 – CROSSTALK†



Induced output signal in amplifier #2 due to output signal at amplifier #1.

---

†Worst case condition shown – no load.

MOTOROLA

MC1710
MC1710C

DIFFERENTIAL VOLTAGE COMPARATORS

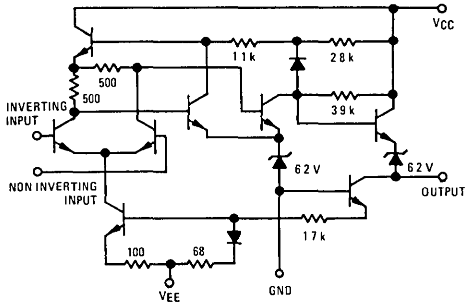
. . . designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV – MC1710
  = 1.5 mV – MC1710C
  Offset Voltage Drift = 3.0 μV/°C – MC1710
  = 5.0 μV/°C – MC1710C
- Fast Response Time – 40 ns
- Output Compatible with all Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V (Typ)
- Low Output Impedance – 200 Ohms

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

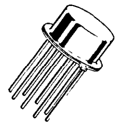
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$ $V_{EE(max)}$	+14 -7.0	Vdc Vdc
Differential Input Signal Voltage	V_{ID}	±5.0	Volts
Common Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitations)	P_D		
Metal Package Derate above T_A = +25°C		680 4.6	mW mW/°C
Ceramic Dual In-Line Package Derate above T_A = +25°C		625 5.0	mW mW/°C
Operating Temperature Range MC1710 MC1710C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

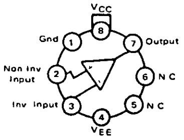
EQUIVALENT CIRCUIT



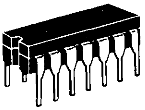
DIFFERENTIAL COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

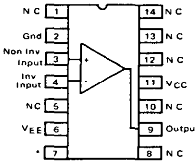




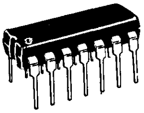
G SUFFIX
METAL PACKAGE
CASE 601



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



*Connected to pin 6 via the substrate on some plastic units



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1710C Only)

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage		V_{IO}				mVdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	2.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	3.0	
(V_O = 1.0 Vdc, T_A = +125°C	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	6.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	6.5	
Temperature Coefficient of Input Offset Voltage		$\Delta V_{IO}/\Delta T$	–	3.0	–	µV/°C
Input Offset Current		I_{IO}				µAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	3.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	7.0	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	7.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	7.5	
Input Bias Current		I_{IB}				µAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	12	20	
	MC1710C		–	12	25	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	45	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	20	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	40	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	40	
Voltage Gain		A_{vol}				V/V
(T_A = +25°C)	MC1710		1250	1700	–	
	MC1710C		1000	1700	–	
(T_A = T_{low} to T_{high}) (1)	MC1710		1000	–	–	
	MC1710C		800	–	–	
Output Resistance		r_o	–	200	–	Ohms
Differential Voltage Range		V_{ID}	±5.0	–	–	Vdc
Positive Output Voltage ($V_{ID} \geqslant 5.0$ mV, $0 \leqslant I_O \leqslant 5.0$ mA)		V_{OH}	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{ID} \geqslant -5.0$ mV)		V_{OL}	-1.0	-0.5	0	Vdc
Output Sink Current		I_{Os}				mAdc
($V_{ID} \geqslant -5.0$ mV, $V_O \leqslant 0$)	MC1710		2.0	2.5	–	
	MC1710C		1.6	2.5	–	
($V_{ID} \geqslant -5.0$ mV, $V_O \geqslant 0$, $T_A = T_{low}$)	MC1710		1.0	2.0	–	
	MC1710C		0.5	–	–	
Input Common-Mode Voltage Range (V_{EE} = -7.0 Vdc)		V_{ICR}	±5.0	–	–	Volts
Common-Mode Rejection Ratio		CMRR				dB
(V_{EE} = -7.0 Vdc, $R_S \leqslant 200$ Ohms)	MC1710		80	100	–	
	MC1710C		70	100	–	
Propagation Delay Time for Positive and Negative Going Input Pulse (V_{ID}= 5.0 mV + V_{IO})		t_{PLH} t_{PHL}	– –	40 35	– –	ns
Power Supply Current ($V_O \leqslant 0$)		I_D+ I_D-	– –	6.4 5.5	9.0 7.0	mAdc
Power Consumption		P_D	–	115	150	mW

(1) T_{low} = -55°C for MC1710, 0°C for MC1710C
T_{high} = +125°C for MC1710, +75°C for MC1710C

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

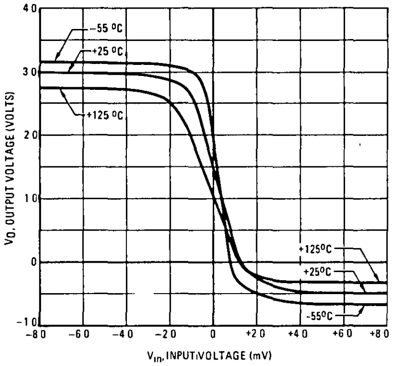


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

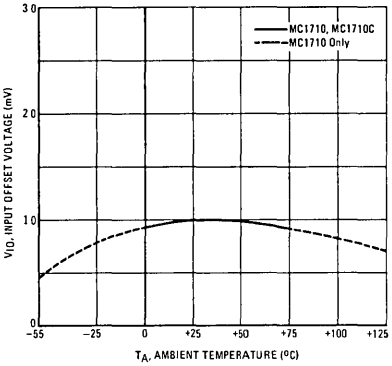


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

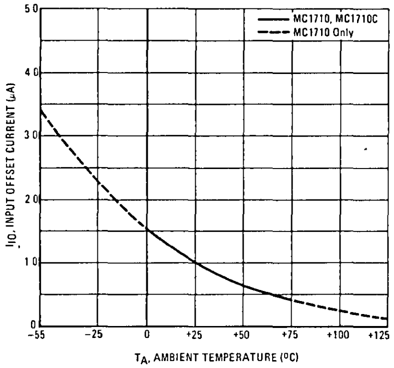


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

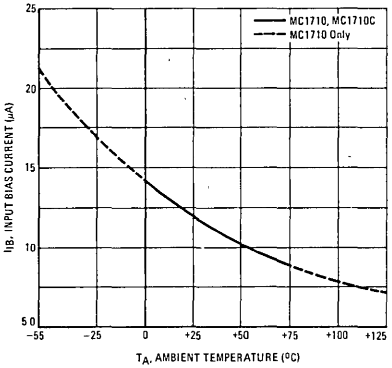


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

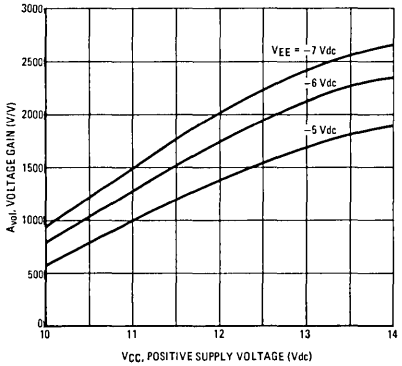
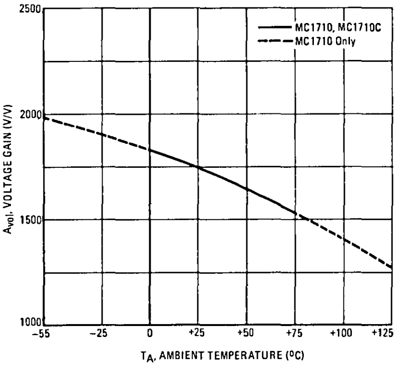


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 7 – RESPONSE TIME

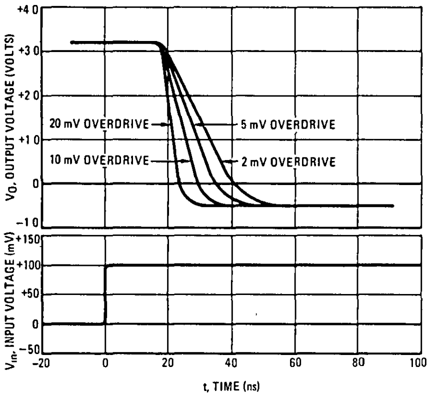


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

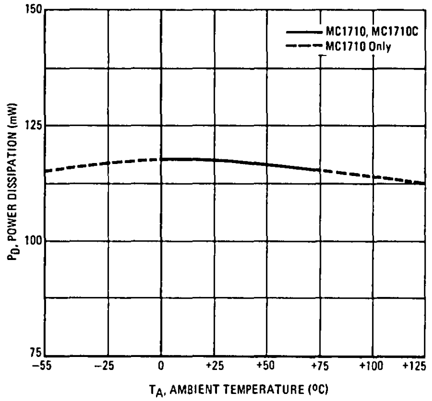


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

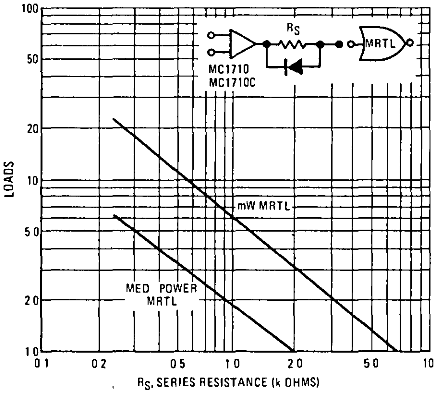
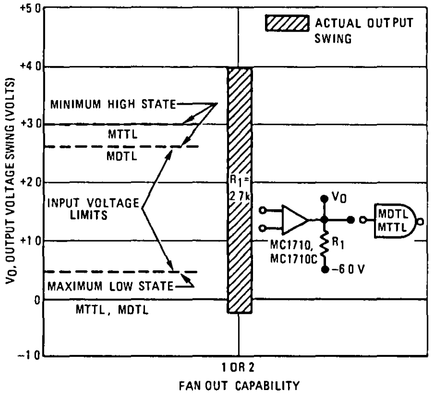


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MOTOROLA

MC1711
MC1711C

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

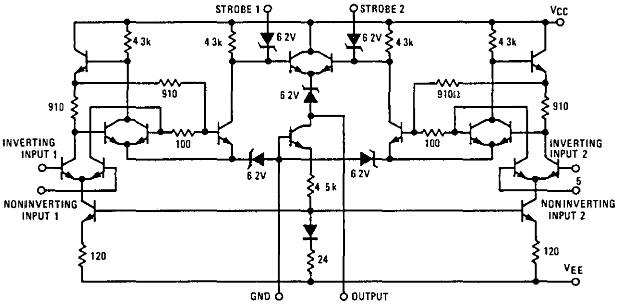
Typical Characteristics:

- Differential Input
  - Input Offset Voltage = 1.0 mV
  - Offset Voltage Drift = 5.0 μV/°C
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms
  - V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance – 200 ohms

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Input Signal Voltage	V_{IDR}	±5.0	Volts
Common-Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Package Derate above T_A = +25°C Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25°C	P_D	 680 4.6 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range MC1711 MC1711C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

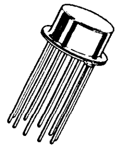
CIRCUIT SCHEMATIC

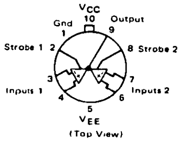


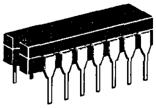
DUAL DIFFERENTIAL COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 603
TO-100

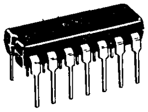


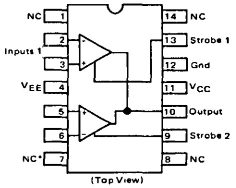




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1711C only)





*Connected to pin 4 via the substrate on some plastic units.

ELECTRICAL CHARACTERISTICS (each comparator) (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1711 Min	MC1711 Typ	MC1711 Max	MC1711C Min	MC1711C Typ	MC1711C Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_{ICR} = 0 Vdc, T_A = +25°C)		–	1.0	3.5	–	1.0	5.0	
($V_{ICR} \neq$ 0 Vdc, T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(V_{ICR} = 0 Vdc, T_A = T_{low} to T_{high}*)		–	–	4.5	–	–	6.0	
($V_{ICR} \neq$ 0 Vdc, T_A = T_{low} to T_{high})		–	–	6.0	–	–	10	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	5.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	0.5	10	–	0.5	15	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	20	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	25	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	20	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	25	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	25	75	–	25	100	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	150	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	150	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	150	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	150	
Voltage Gain	A_{vol}							V/V
(T_A = +25°C)		700	1500	–	700	1500	–	
(T_A = T_{low} to T_{high})		500	–	–	500	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geqslant$ 10 mVdc, $0 \leqslant I_O \leqslant$ 5.0 mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Low Level Output Voltage ($V_{ID} \geqslant$ -10 mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level ($V_{strobe} \leqslant$ 0.3 Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geqslant$ -10 mV, $V_O \geqslant$ 0)	I_{Os}	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Input Common-Mode Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Volts
Response Time (V_b = 5.0 mV + V_{IO})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current ($V_O \leqslant$ 0 Vdc)	I_{CC}	–	8.6	–	–	8.6	–	mAdc
	I_{EE}	–	3.9	–	–	3.9	–	
Power Consumption		–	130	200	–	130	200	mW

*T_{low} = -55°C for MC1711, 0°C for MC1711C
T_{high} = +125°C for MC1711, +75°C for MC1711C

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

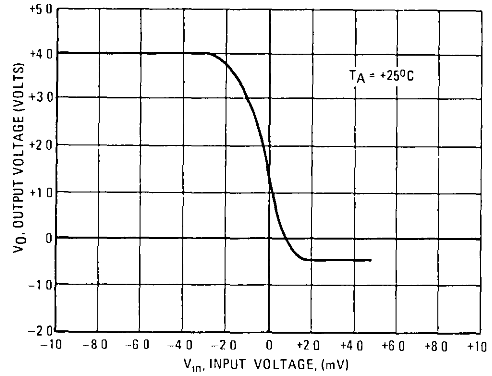


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

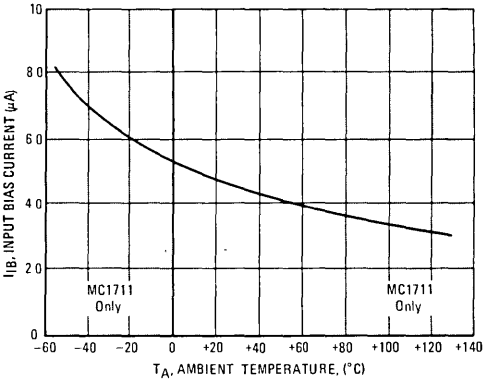


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

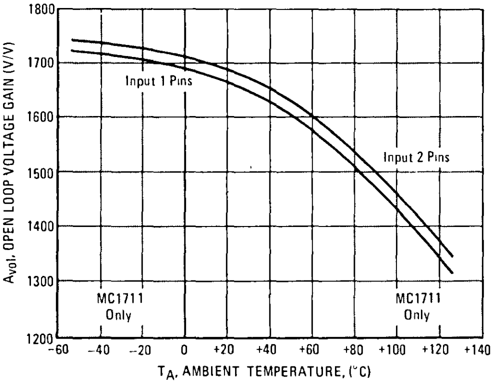


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

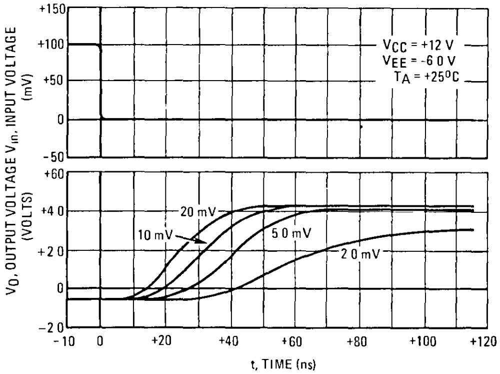


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

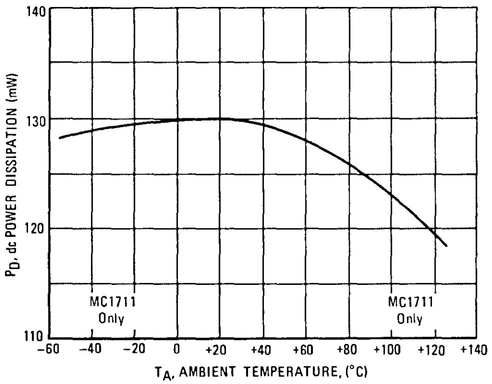


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

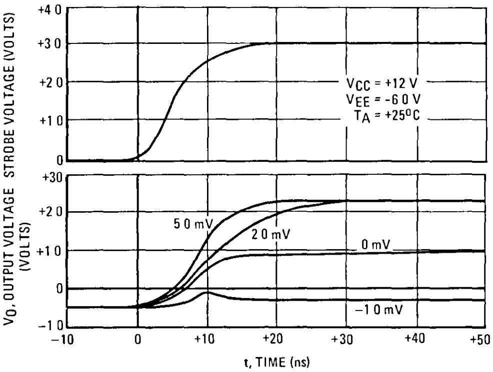


FIGURE 7 – COMMON-MODE PULSE RESPONSE

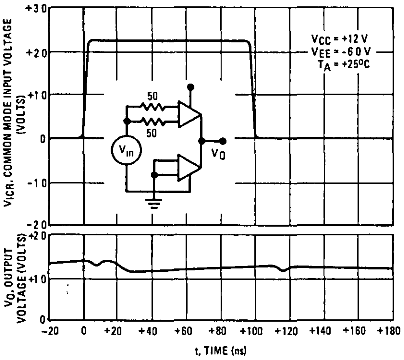


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

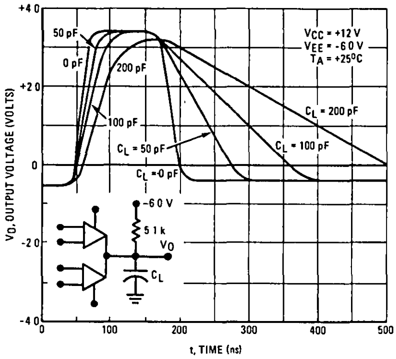


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

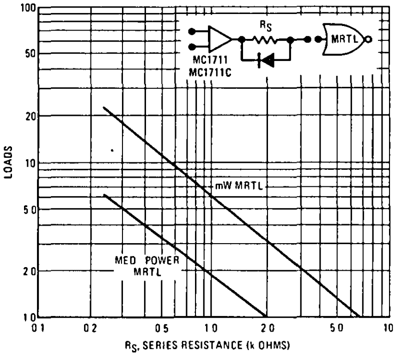
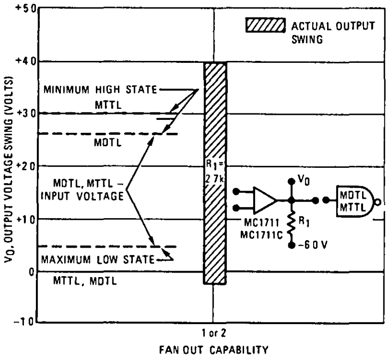


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MOTOROLA

MC3302

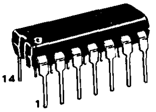
QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302 contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

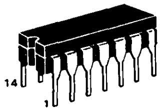
- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = ±V_{CC}
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – 700 μA typical @ V_{CC} +5.0 to +28 Vdc
- Outputs can be Connected to Give the Implied AND Function

QUAD COMPARATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	±V_{CC}	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to +V_{CC}	Vdc
Power Dissipation @ T_A = 25°C	P_D		
Plastic Package – P Suffix		1.2	Watts
Derate above 25°C		10	mW/°C
Ceramic Package – L Suffix		1.2	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A		°C
Plastic Package		-40 to +85	
Ceramic Package		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Requires an external resistor, R_L, to limit current below maximum rating.

Note 2. If either (+) or (-) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

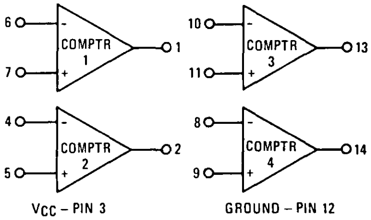
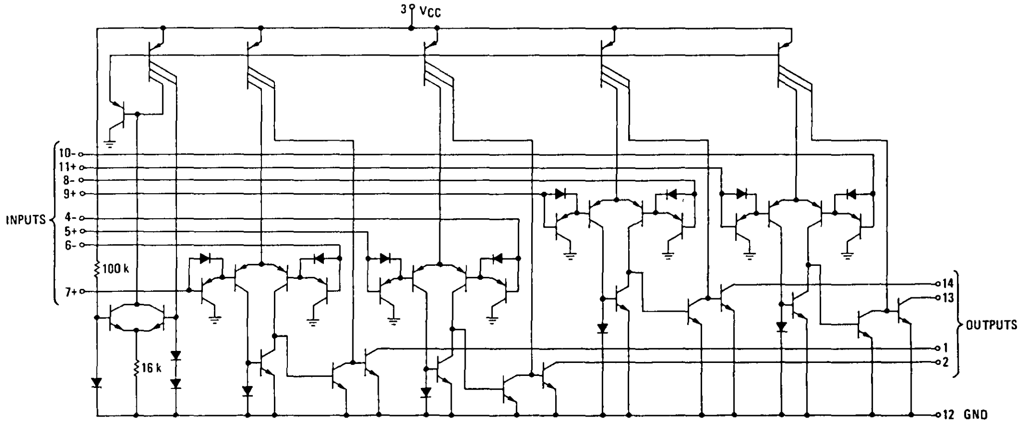
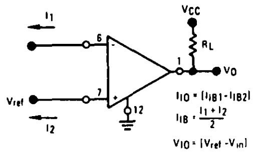
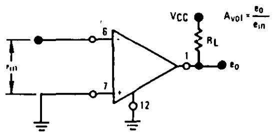
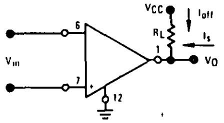
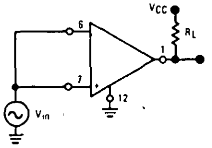
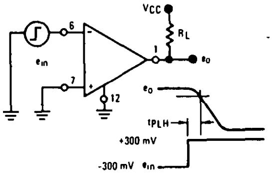
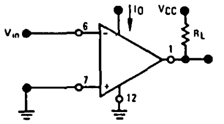


FIGURE 2 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Characteristic Definitions (1/4 Circuit Shown)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage (V_{ref} = 1.2 Vdc) (T_A = +25°C) (T_A = −40 to +85°C)	V_{IO}	– –	3.0 –	20 40	mVdc
	Input Offset Current	I_{IO}	–	3.0	–	nAdc
	Input Bias Current (T_A = +25°C) (T_A = −40 to +85°C)	I_{IB}	– –	30 –	500 1000	nAdc
	Voltage Gain (T_A = +25°C, R_L = 15 kΩ)	A_{vol}	2,000	30,000	–	V/V
	Transconductance	gm	–	2.0	–	mhos
	Input Differential Voltage Range	V_{IDR}	±V_{CC}	–	–	Vdc
	Output Leakage Current (Output Voltage High)	I_{OL}	–	–	1.0	µAdc
	Output Voltage - Low Logic State (I_s = 2.0 mA, V_{CC} = +5.0 to +28 Vdc)	V_{OL}	–	150	400	mVdc
	Output Sink Current (V_{CC} = +5.0 Vdc) (T_A = +25°C, V_{OL} = 400 mV) (T_A = −40 to +85°C, V_{OL} = 800 mV)	I_{sink}	– 2.0	6.0 –	– –	mAdc
	Input Common-Mode Voltage Range (V_{CC} = +28 Vdc)	V_{ICR}	0-26	–	–	Volts
	Common-Mode Rejection Ratio	CMRR	–	60	–	dB
	Propagation Delay Time For Positive and Negative-Going Input Pulse (R_L = 15 kΩ)	$t_{PHL/LH}$	–	2.0	–	µs
	Transition Time (R_L = 15 kΩ)	t_{THL} t_{TLH}	– –	0.15 0.8	– –	µs
	Power Supply Current (Total of four comparators) (R_L = ∞, V_{CC} = +5.0 to +28 Vdc)	I_{CC} I_{EE}	–	0.7	1.8	mAdc

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A +25°C (each comparator) unless otherwise noted.)

FIGURE 3 – NORMALIZED INPUT OFFSET VOLTAGE

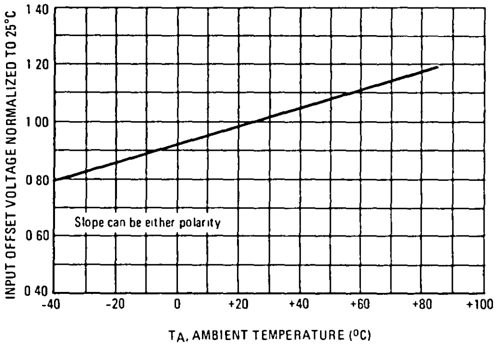


FIGURE 4 – NORMALIZED OFFSET CURRENT

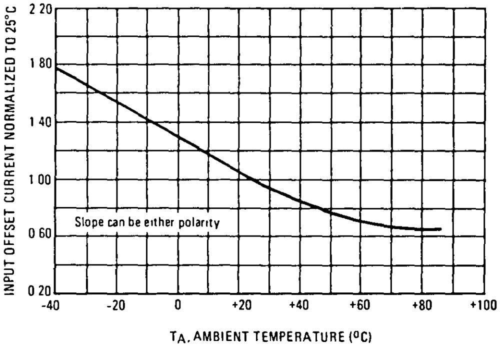
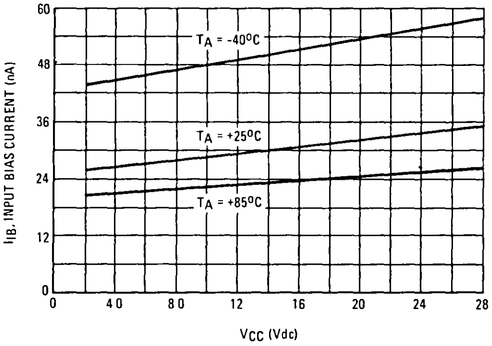


FIGURE 5 – INPUT BIAS CURRENT



TYPICAL APPLICATIONS

The MC3302 is a quad comparator having high gain, wide bandwidth characteristics. This gives the device oscillator tendencies if the outputs capacitively couple to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (1 to 10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −300 mV should not be used.

TYPICAL APPLICATIONS (continued)

FIGURE 6 – FREE-RUNNING SQUARE-WAVE OSCILLATOR

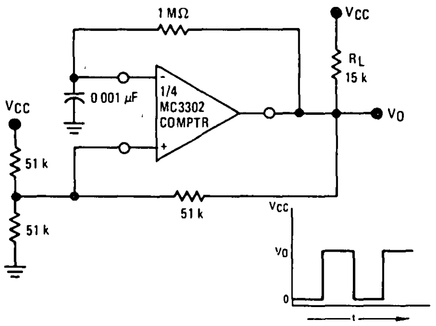


FIGURE 7 – TIME DELAY GENERATOR

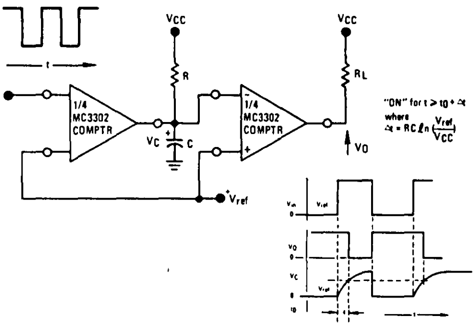
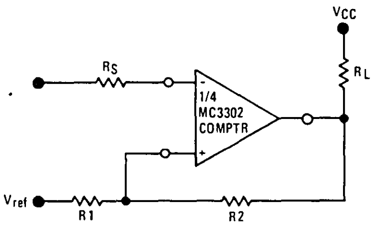


FIGURE 8 – COMPARATOR WITH HYSTERESIS



$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_O\ \mathrm{Low})\,R1}{R1 + R2 + R_L}$$

MOTOROLA

MC3430
thru
MC3433

QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

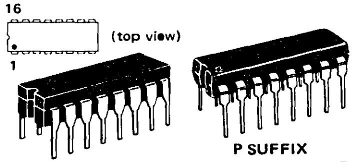
The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versionsare specified for a ±7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leq 200$ ohms.

QUAD HIGH-SPEED VOLTAGE COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM

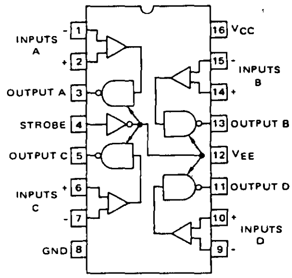
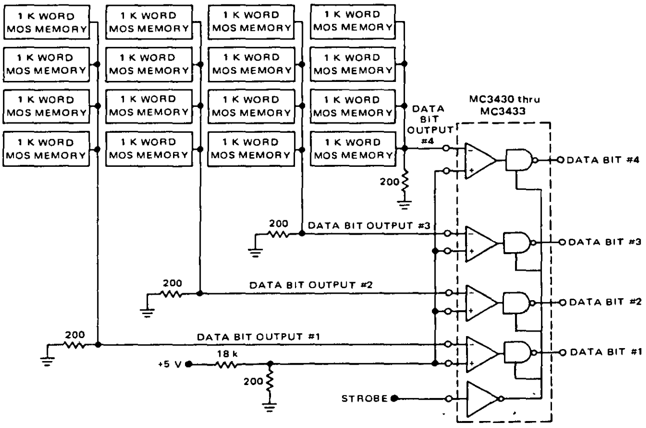


FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE
MC3430 and MC3432

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV T_A = 0 to 70°C	L	H	MC3430
	H	Z	
	L	Off	MC3432
	H	Off	
-7.0 mV $\leq V_{ID}$ $\leq$ 7.0 mV T_A = 0 to 70°C	L	I	MC3430
	H	Z	
	L	I	MC3432
	H	Off	
$V_{ID} \leq$ -7.0 mV T_A = 0 to 70°C	L	L	MC3430
	H	Z	
	L	On	MC3432
	H	Off	

TRUTH TABLE
MC3431 and MC3433

Input	Strobe	Output	Device
$V_{ID} \geq 12$ mV T_A = 0 to 70°C	L	H	MC3431
	H	Z	
	L	Off	MC3433
	H	Off	
-12 mV $\leq V_{ID}$ $\leq$+12 mV T_A = 0 to 70°C	L	I	MC3431
	H	Z	
	L	I	MC3433
	H	Off	
$V_{ID} \leq$ -12 mV T_A = 0 to 70°C	L	L	MC3431
	H	Z	
	L	On	MC3433
	H	Off	

L = Low Logic State   Z = Third (High Impedance)
H = High Logic State   I = Indeterminate State
$R_S \leq 200\ \Omega$

7

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432 — 33 versions)	V_O	+7.0	Vdc
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0°C to +70°C unless otherwise noted.)
Typical Values are Measured at T_A = 25°C

		MC3430, MC3431			MC3432, MC3433			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Sensitivity (See Discussion on Page 3) ($R_S \leqslant 200$ Ohms)	V_{IS}							mV
(Common Mode Voltage Range = -3.0 V $\leqslant V_{in} \leqslant$ 3.0 V)								
4.75 $\leqslant V_{CC} \leqslant$ 5.25 V -4.75 $\geqslant V_{EE} \geqslant$ -5.25 V T_A = 25°C MC3430, MC3432		–	–	±6.0	–	–	±6.0	
MC3431, MC3433		–	–	±10	–	–	±10	
(Common Mode Voltage Range = -3.0 V $\leqslant V_{in} \leqslant$ 3.0 V)								
4.75 $\leqslant V_{CC} \leqslant$ 5.25 V -4.75 $\geqslant V_{EE} \geqslant$ -5.25 V T_A = 0 to 70°C MC3430, MC3432		–	–	±7.0	–	–	±7.0	
MC3431, MC3433		–	–	±12	–	–	±12	
Input Offset Voltage ($R_S \leqslant 200$ Ohms)	V_{IO}	–	2.0	–	–	2.0	–	mV
Input Bias Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V) MC3430, MC3432	I_{IB}	–	20	40	–	20	40	µA
MC3431, MC3433		–	20	40	–	20	40	
Input Offset Current	I_{IO}	–	1.0	–	–	1.0	–	µA
Voltage Gain	A_{vol}	–	1200	–	–	1200	–	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	–	–	-1.6	–	–	-1.6	mA
Strobe Current (High State)	$I_{IH(S)}$							
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 2.4 V)		–	–	40	–	–	40	µA
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 5.25 V)		–	–	1.0	–	–	1.0	mA
Output Voltage (High State) (I_O = -400 µA, V_{CC} = 4.75 V, V_{EE} = -4.75 V)	V_{OH}	2.4	–	–	–	–	–	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = -4.75 V, V_O = 5.25 V)	I_{CEX}	–	–	–	–	–	250	µA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{os}	-18	–	-70	–	–	–	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{off}	–	–	40	–	–	–	µA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{CC} I_{EE}	– –	45 -17	60 -30	– –	45 -17	60 -30	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{vol}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analagous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range – 0 to 70°C
Power Supply Variations – ±5% (all conditions)
Input Source Resistance – ≤200 Ohms
Common-Mode Voltage Range – -3.0 V to +3.0 V

Note Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V (V_{OH}min – V_{OL}max = 2.4 V – 0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

TABLE I – WORST CASE COMPARISONS

	T_A = 25°C						T_A = 0 to 70°C					
Type Number	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV
MC3430, MC3432	–	–	–	–	–	6.0	–	–	–	–	–	7.0
MC3431, MC3433	–	–	–	–	–	10	–	–	–	–	–	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
MLM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

*Typical values given, as minimum gain not always specified
**I_{IO} measured in nA

FIGURE 2 – GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

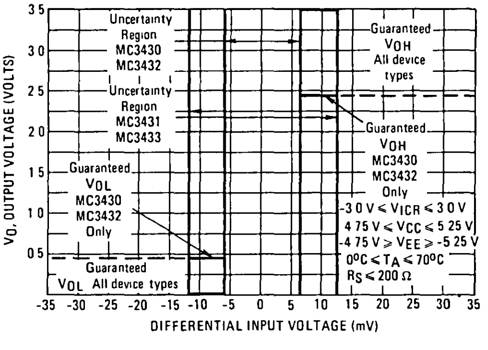
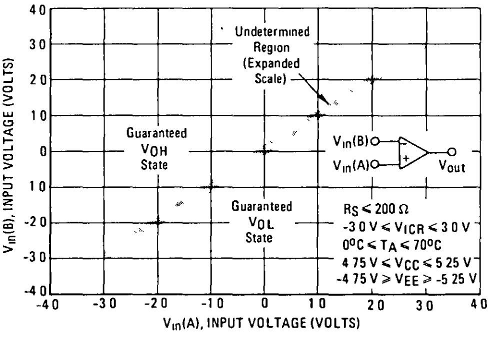


FIGURE 3 – GUARANTEED OUTPUT STATE versus INPUT VOLTAGE

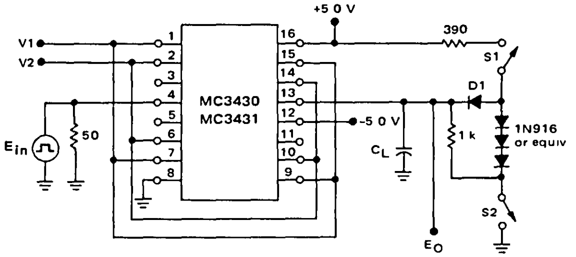


SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431			MC3432, MC3433			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PHL(D)}$	6,8-11	–	20	45	–	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PLH(D)}$	6,8-11	–	33	55	–	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	–	–	35	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	–	–	35	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	–	–	40	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	–	–	35	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	–	–	–	–	–	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	–	–	–	–	–	35	ns

TEST CIRCUITS

FIGURE 4 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{in} waveform characteristics

t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

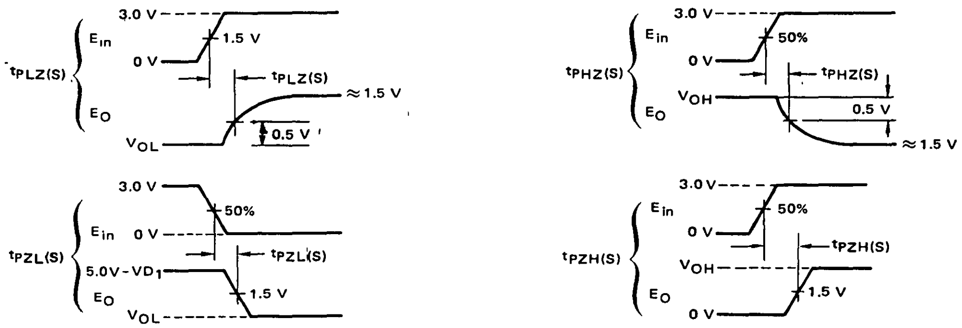
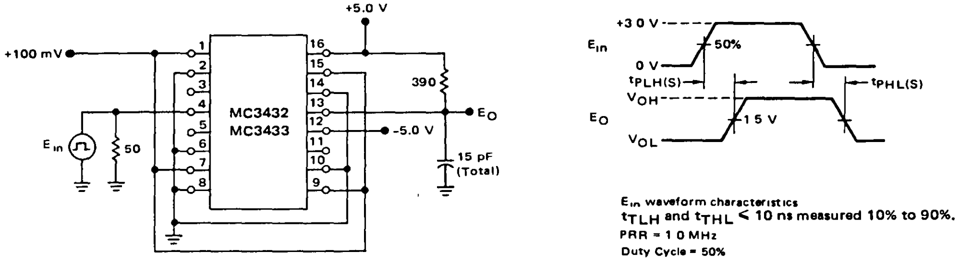


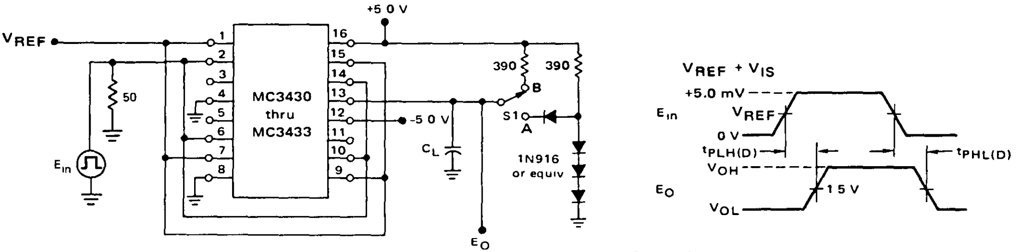
FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



E_{in} waveform characteristics
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1 0 MHz
Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



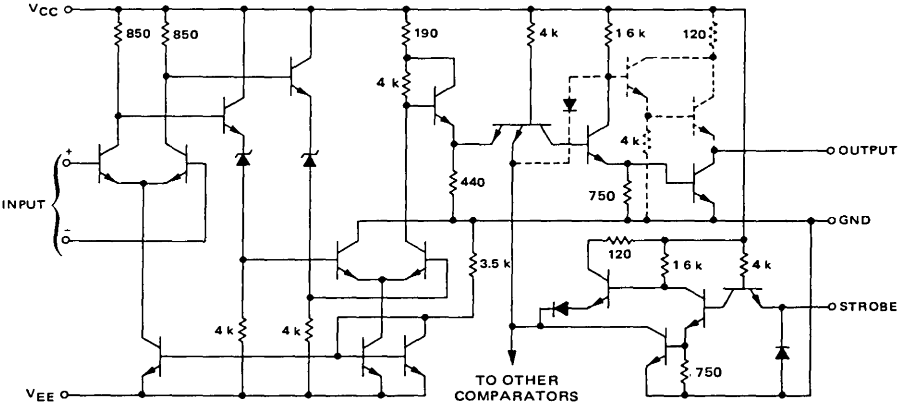
Output of Channel B shown under test, other channels are tested similarly

S1 at "A" for MC3430, MC3431
S1 at "B" for MC3432, MC3433
C_L = 50 pF total for MC3430, MC3431
C_L = 15 pF total for MC3432, MC3433

Device	V_{REF} mV
MC3430	11
MC3431	15
MC3432	11
MC3433	15

E_{in} waveform characteristics
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1 0 MHz
Duty Cycle = 50%

FIGURE 7 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

TYPICAL PERFORMANCE CURVES

RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

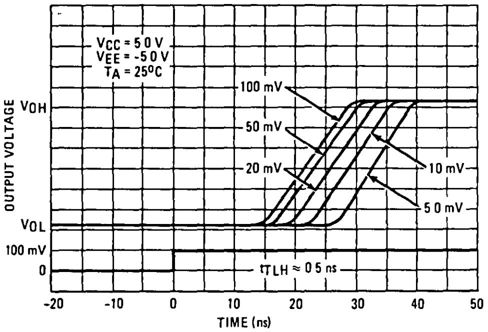
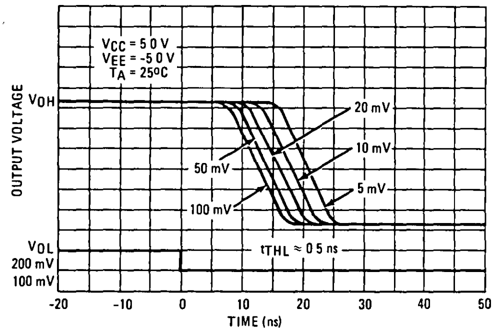


FIGURE 9 – OUTPUT HIGH TO LOW



RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

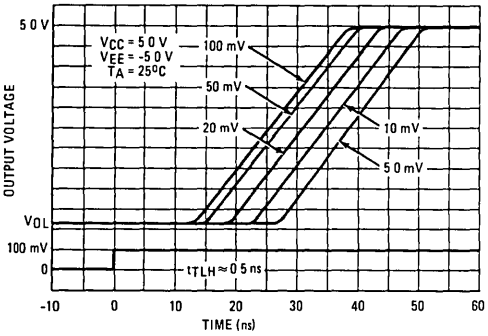


FIGURE 11 – OUTPUT HIGH TO LOW

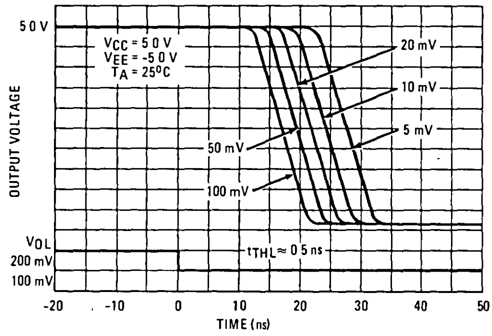


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

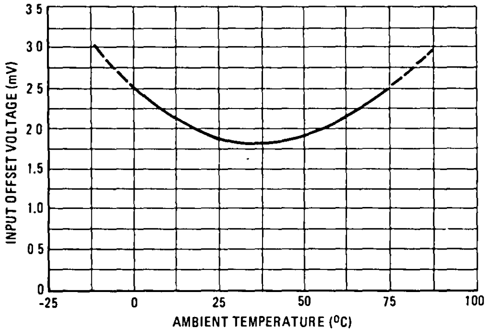
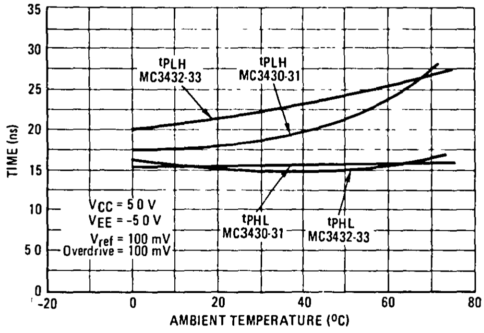
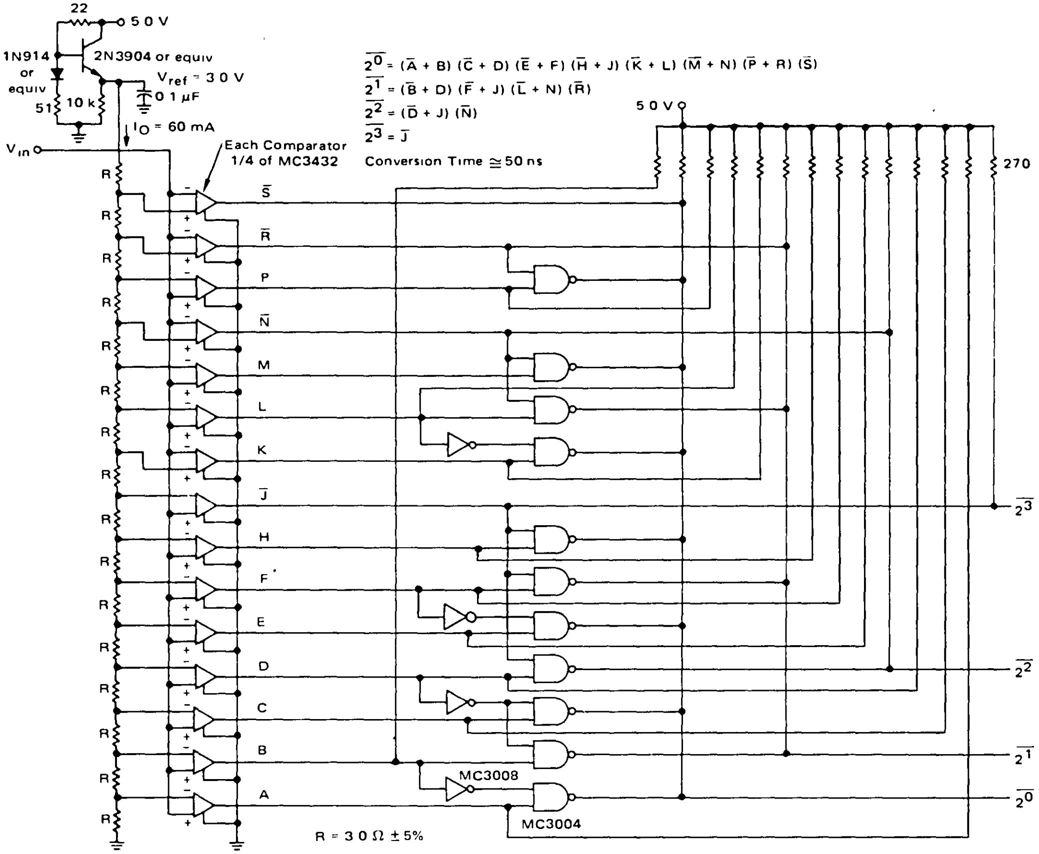


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 14 — 4-BIT PARALLEL A/D CONVERTER



$\overline{2^0} = (\bar{A} + B)\ (\bar{C} + D)\ (\bar{E} + F)\ (\bar{H} + J)\ (\bar{K} + L)\ (\bar{M} + N)\ (\bar{P} + R)\ (\bar{S})$

$\overline{2^1} = (\bar{B} + D)\ (\bar{F} + J)\ (\bar{L} + N)\ (\bar{R})$

$\overline{2^2} = (\bar{D} + J)\ (\bar{N})$

$\overline{2^3} = \bar{J}$

Conversion Time ≅ 50 ns

FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS

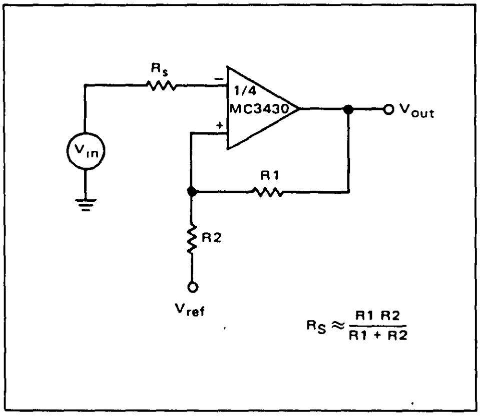
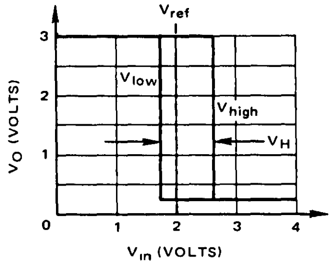


FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15



$$V_{high} = V_{ref} + \frac{R2\,[V_{O(max)} - V_{REF}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\,[V_{O(min)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_h)

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\,[V_{O(max)} - V_{O(min)}]$$

FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

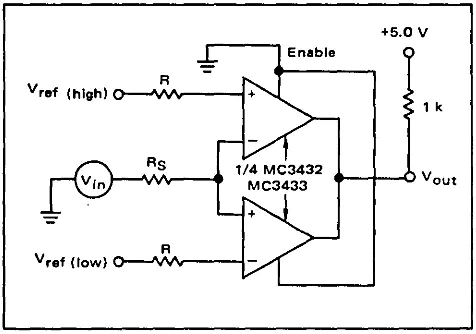
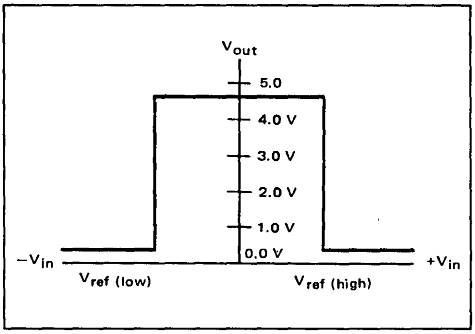
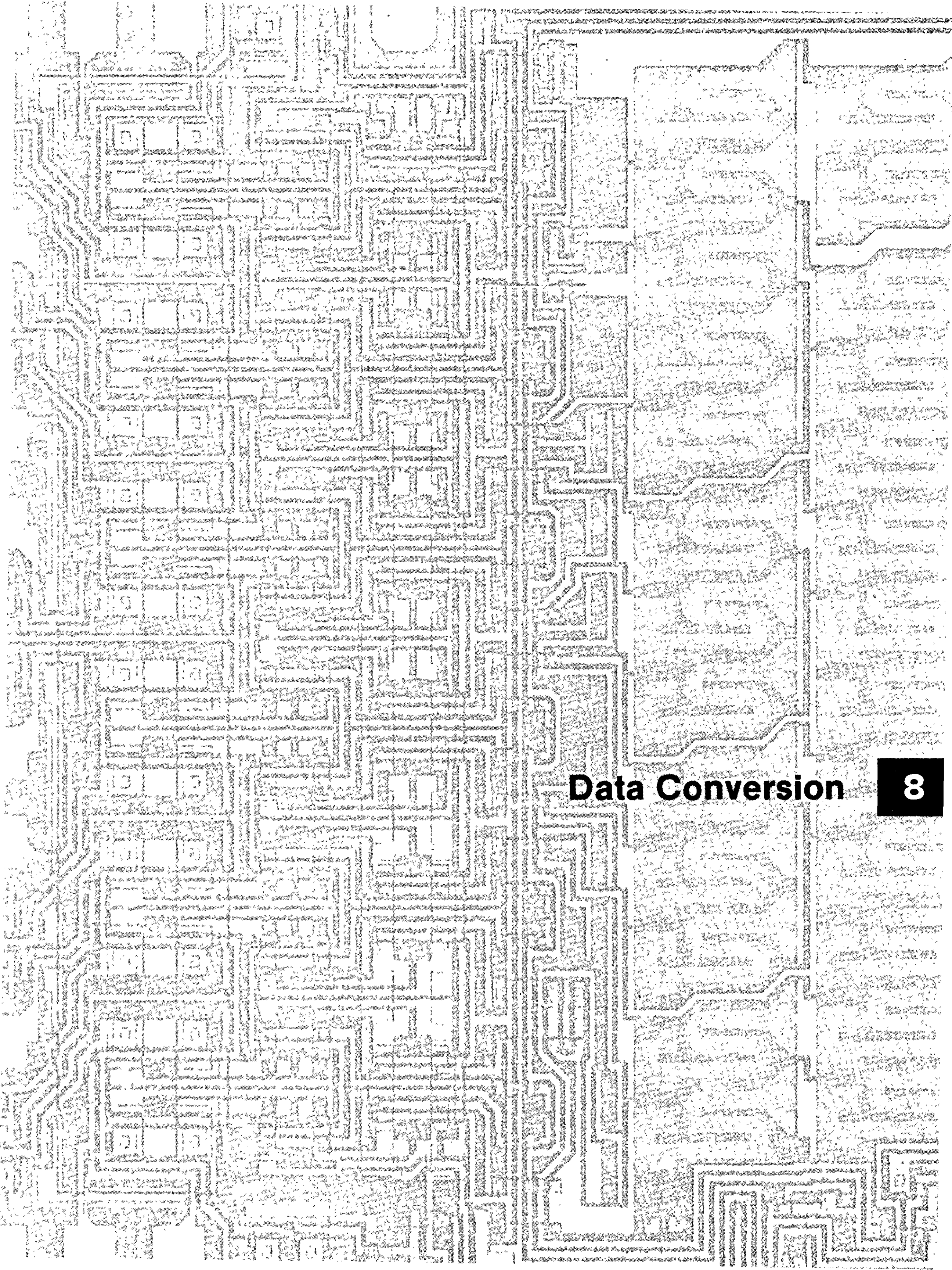


FIGURE 18 – VOLTAGE TRANSFER FUNCTION





Data Conversion

8

DATA CONVERSION

MOTOROLA

MC1405
MC1505

DUAL RAMP A/D CONVERTER SUBSYSTEM

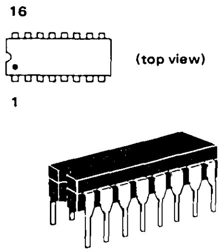
The MC1505/MC1405 is intended to perform the dual ramp function for either a 3-1/2 or 4-1/2 digit DVM or use as a general-purpose analog-to-digital (A/D) converter. It can be combined with the CMOS MC14435 logic system to produce the complete 3-1/2 digit DVM function.

The MC1505 uses the proven dual ramp A/D conversion technique. The subsystem consists of an on-chip voltage reference, a pair of voltage/current converters, an integrator, a comparator, a current switch and associated control and calibration circuitry. Only one capacitor and two calibration potentiometers are required for normal operation.

- Accuracies to 13 Bits
- Low Power Consumption: 42 mW @ +5.0 V
- Single Power Supply Operation – +5.0 V to +15 V
- Low Power Supply and Temperature Sensitivity
- Digital Inputs and Outputs Compatible with Both MTTL and CMOS
- Accepts Either Positive or Negative Input Voltages
- Combines with MC14435 to Produce 3-1/2 Digit A/D Converter

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CASE 620
CERAMIC PACKAGE

FIGURE 1 – COMPLETE A/D CONVERTER SYSTEM

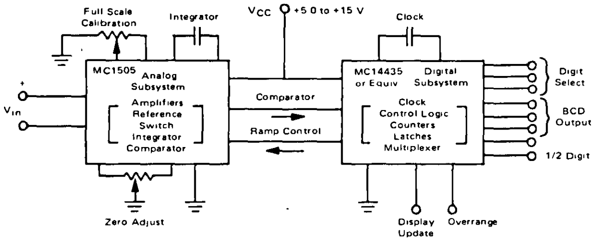
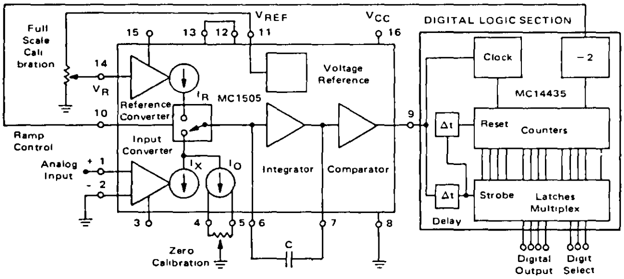


FIGURE 2 – PIN CONNECTIONS AND FUNCTIONAL DIAGRAM (as used in Figure 1)



TYPICAL APPLICATIONS

BCD A/D Converter: 2-1/2 to 4-1/2 Digits (LSI or MSI Logic)
- Panel Meters
- Digital Voltmeters
- Portable Instruments
- Industrial Measurement and Control

Binary A/D Converter: 8-to-13 Bits (LSI or MSI Logic)
- Industrial Measurement and Control
- High Noise Environments (Integrating Converter with MTTL, MHTL, and CMOS Compatibility)

Other Uses:
- Data Acquisition Systems with Remote MC1505
- Voltage to Frequency Conversion
- Delta Modulation and Signal Generation

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16.5	Vdc
Digital Input Voltage	V_{10}	+16.5	Volts
Reference Input Voltage	V_R	2.0	Volts
Unknown Input Voltage Range	V1 V2	±5.0 ±5.0	Volts
Zero Calibration Control Pin Voltage	V4	5.0	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above $T_A = +25^{o}C$	P_D	1000 6.0	mW mW/°C
Operating Ambient Temperature Range MC1505L MC1405L	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ⩾ 2.0 Vdc, $T_A = 25^{o}C$ unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505			MC1405			Unit
			Min	Typ	Max	Min	Typ	Max	
A/D CONVERSION SYSTEM (1)									
Linearity: Deviation from Straight Line through Zero and Full Scale (2)	E_r	9, 11	–	±0 01	±0 05	–	±0.01	±0.05	%F S.
Mid-Scale Power Supply Sensitivity (PSS of $I_R-(I_X+I_O)$, V1 = 1.0 V)	PSSF	3	–	0.002	±0 02	–	0.002	±0.02	%/%
Zero Calibration Power Supply Sensitivity (V1 = V2 = 0 V)	PSSZ	9	–	0 001	–	–	0.001	–	%F.S./%
Input Common Mode Sensitivity (V_X = 2.0 V, V_{CM} = V2 is varied)	$\lvert CMSI_X\rvert$	3	–	0.0006	0.0012	–	0.0006	0.0018	%/mV
Full Scale Temperature Drift (3)	|TCF|	9	–	0.004	–	–	0.004	–	%/°C
Zero Calibration Temperature Drift (3)	|TCZ|	9	–	0.001	–	–	0.001	–	%F.S./°C
VOLTAGE REFERENCE									
Reference Voltage, Pin 11	V_{REF}	3	1.15	1.25	1 35	1.1	1.25	1.4	Vdc
Reference Voltage Power Supply Sensitivity	$PSSV_{REF}$	3	–	0.003	±0 01	–	0.003	±0.02	%/%
Reference Voltage Temperature Drift	$\lvert TCV_{REF}\rvert$	3	–	0.015	–	–	0 015	–	%/°C
REFERENCE CURRENT CONVERTER									
Reference Current	I_R	3	–	250	–	–	250	–	μA
Input Bias Current	I14	3	–	10	40	–	10	40	nA
Input Range of V_R	V14	3	0.8	–	1.2	0.8	–	1 2	Vdc
Input Offset Voltage (V14–V15)	$\lvert V_{RR}\rvert$	3	–	1 0	2.5	–	2.0	5.5	mV
INPUT CURRENT CONVERTER									
Unknown Current	I_X	3	–	500	–	–	500	–	μA
Input Resistance	R_I	3	–	4.0	–	–	4.0	–	kΩ
Input Differential Range	V_X	3,10	0	2 0	–	0	2.0	–	Volts
Input Common Mode Range	CMR	3,10,12	-1.5	–	+1.5	-1.5	–	+1.5	Volts
Input Bias Currents	11 12	3,9	– –	200 -300	– –	– –	200 -300	– –	μA
Input Offset Voltage (V13-V3)	$\lvert V_{XX}\rvert$	3	–	1.0	2.5	–	2.0	5.5	mV
RAMP OFFSET SOURCE									
Ramp Offset Current	I_O	4	–	25	–	–	25	–	μA

(1) System parameters measured using external voltage reference, independent of V11 = V_{REF}.
Integrator Capacitor = 2.0 μF
Clock Frequency = 30 kHz
V_{CC} = 15 V

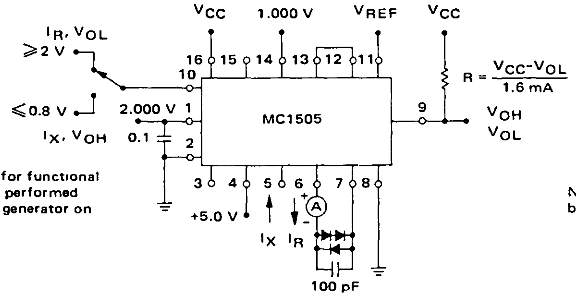
(2) Does not include quanitizing error. See Figure 10 for calibration.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ⩾ 2.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505			MC1405			Unit
			Min	Typ	Max	Min	Typ	Max	
CURRENT SWITCH									
Digital Input Logic Levels, Pin 10									
High Level, Logic "1"	V_{IH}	3,18	2.0	–	–	2.0	–	–	Vdc
Low Level, Logic "0"	V_{IL}	3,18	–	–	0.8	–	–	0.8	Vdc
Digital Input Current									
High Level, Logic "1"	I_{IH}	3	–	0	1.0	–	0	1.0	µA
Low Level, Logic "0"	I_{IL}	3	–	-5.0	-50	–	-5.0	-50	µA
INTEGRATOR									
Input Bias Current	I6	5	–	10	30	–	10	50	nA
Output Voltage Swing	V7	–							Volts
High			12.8	13.0	–	12.8	13.0	–	
Low			–	0.2	0.35	–	0.2	0.35	
COMPARATOR									
Output Logic Levels, Pin 9									Volts
High Level, Logic "1" $T_A = T_{low}$ to T_{high}	V_{OH}	3	13.5	14.0	–	13.5	14.0	–	
Low Leve, Logic "0"	V_{OL}	3	–	0.35	0.5	–	0.35	0.5	
(Sink Current = 1.6 mA)									
Input Threshold	$V_{TH(7)}$	–	0.9	1.0	1.1	0.9	1.0	1.1	Volts
POWER SUPPLY									
Power Supply Current	I_{CC}								mA
(V_{CC} = +5.0 Vdc)		3	–	8.4	12.0	–	8.4	12.0	
(V_{CC} = +15.0 Vdc)		3	–	9 0	13.0	–	9.0	13.0	
Power Supply Voltage Range	V_{CC}	–	4.75	–	16 5	4.75	–	16.5	Vdc
Power Consumption	P_C								mW
(V_{CC} = +5.0 Vdc)		–	–	42	60	–	42	60	
(V_{CC} = +15.0 Vdc)		–	–	135	195	–	135	195	

T_{low} = -55°C for MC1505L, 0°C for MC1405L
T_{high} = +125°C for MC1505L, +70°C for MC1405L

FIGURE 3 – STANDARD TEST CONFIGURATION



Note: A test for functional parts may be performed using a pulse generator on Pin 10.

Note: All dc supplies bypassed with 0.1 µF.

FIGURE 4 – I_O MEASUREMENT

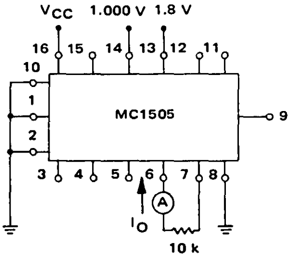
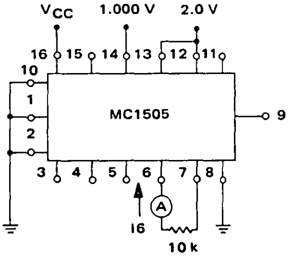


FIGURE 5 – I6 MEASUREMENT



GENERAL INFORMATION

Dual Ramp Analog-to-Digital Conversion

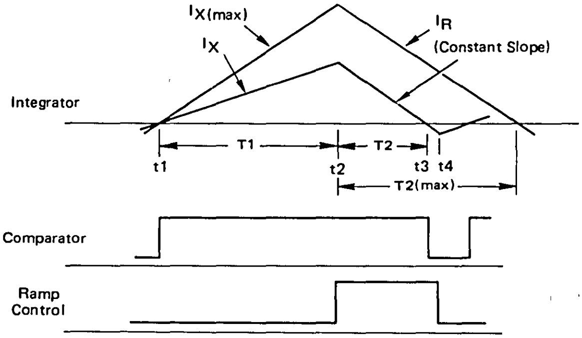
The dual ramp method of A/D conversion is a proven system which is capable of very high accuracy. The conversion is an integrating process which offers high noise rejection and immunity to changes in the clock rate and integrator capacitor value. The particular method used in the MC1505 is a noniterating dual slope technique which produces an accurate result after one conversion period.

Dual ramp conversion is accomplished with the system of Figure 2. The conversion begins at time t1, when current I_X causes the integrator output, or ramp, to cross the comparator threshold, as shown in Figure 6. The clock is activated and the counters begin counting from zero. The system counts for a fixed period T, with a ramp slope which depends on the input voltage, i.e., a steep slope is caused by a high input voltage. When the counters have reached full scale, the overflow count triggers a ÷ 2 flip-flop which changes the ramp control polarity current. I_R now controls the integrator and the down ramp begins at t2. This ramp continues at a fixed slope for a time period which depends on the amplitude achieved by the up ramp. Thus T2 is determined by the input voltage. When the ramp crosses the comparator threshold at t3, the clock stops and the counter holds a digital value which is proportional to the unknown input voltage.

After the down ramp crosses the comparator threshold, a timing sequence in the digital section strobes the latches to store the data, resets the counters, and reverses the ramp at t4 to begin a new conversion.

Since the voltage change across the capacitor is equal on the up and down ramps, an equal amount of charge is exchanged. The equations of Figure 6 show that the system output is the ratio of the unknown and reference currents, and long term changes in the clock rate and integrator capacitor do not effect the reading.

FIGURE 6 – DUAL RAMP A/D CONVERSION WAVEFORMS



ΔV on capacitor is equal in T1 and T2

$$\frac{1}{C}\int_{t1}^{t2} I_X\,dt = \frac{1}{C}\int_{t2}^{t3} I_R\,dt$$

Where I_X is opposite I_R polarity.

$$I_X T1 = I_R T2$$

Since I_X and I_R are proprotional to V_X and V_R,

$$V_X T1 = V_R T2$$

$$\boxed{T2 = T1 \frac{V_X}{V_R}}$$

T2 corresponds to the number of counts in the output digital word.

T1 and T2 are derived from the clock, so their ratio is independent of clock frequency.

A/D Subsystem Circuit Description

The MC1505 incorporates special circuit features which allow all the analog functions of the dual ramp system to be performed on a single monolithic chip using standard bipolar processing.

Voltage-to-current conversion for both the input and reference voltages allows the use of a high-speed current switch and single supply operation. The unbuffered differential inputs have sufficiently high input impedance for power supply monitoring applications, and provide flexibility for other input formats since they will accept either positive or negative voltages.

The voltage reference, shown in Figure 7, is one of the six basic circuits in the subsystem. It provides a low impedance output which has excellent temperature stability, and high power supply rejection. Biasing for the other circuits in the MC1505 is derived from the voltage reference circuitry.

The same basic amplifier circuit is used in both the reference and input voltage-to-current converters. It is an extremely well balanced amplifier with low input offset voltage temperature drift. The reference converter uses a pair of PNP transistors to derive current I_R, in conjunction with a reference resistor which has the same temperature coefficient as those used in the input converter. The value of the reference current is $V_R/R5$. The collectors of transistors Q1, Q2 and Q3 in Figure 7 all track with a two diode temperature coefficient, which assures constant current ratios.

The reference resistor value can vary by 30% of 4.0 kΩ due to process variations. Moreover, these variations will also affect the input bridge resistors. Thus, the ratio of reference to unknown current has a close tolerance for a wide range of resistor values.

The input voltage-to-current converter is a bridge or bilateral current source whose output current is $V_X/R1$. If the bridge is perfectly balanced, its output impedance and common mode rejection are infinite. However, the design has the ability to tolerate bridge mismatches of approximately 0.5%. In order to tolerate this mismatch, the output of the bridge current source is connected to the current switch which is a low temperature coefficient, low impedance source of 1.25 volts. This technique effectively eliminates output current changes due to finite output impedance which is caused by resistor mismatch. This input current converter makes possible the use of a single supply voltage and differential inputs which can be used at or below ground potential.

An important feature of the MC1505 is the ramp offset current source which is added to the unknown current and does not allow the ramp to reach zero slope when the input voltage is zero. The ramp range is shown in Figure 8. The ramp offset current has a value of $I_R/10$, so that the minimum ramp slope is 5% of the full scale slope. This allows reliable conversion at low input voltages by assuring a nearly constant comparator propagation delay and a good ramp signal-to-noise ratio. It also prevents turn-off of the diode in the current switch at low levels, restricting the voltage change at the output of the resistor bridge. Still another feature is that it provides a convenient temperature compensated zero adjust which can correct errors in the resistor bridge and input buffer amplifiers when they are used. The ramp offset current is compensated by 100 extra counts in the digital logic during ramp down, so it does not appear in the digital output (see Figure 8).

The current switch uses current steering for very high speed operation. A smooth transition occurs as one current is turned on while the other is turned off. This minimizes error during the ramp reversal at its peak, especially since the reference current source has a very high output impedance and does not change value when switched. The settling time of the input current converter is not a factor in system accuracy. At the ramp peak, I_X is turned off, so the amplifier settles after the unknown current is decoupled from the integrator. When the ramp is below the comparator threshold, the unknown current is switched on and thus the current can settle before the ramp enters the active conversion range. The switch operates into a voltage of 1.95 volts and is translated by a follower so its input

FIGURE 7 – A/D CONVERTER ANALOG SUBSYSTEM

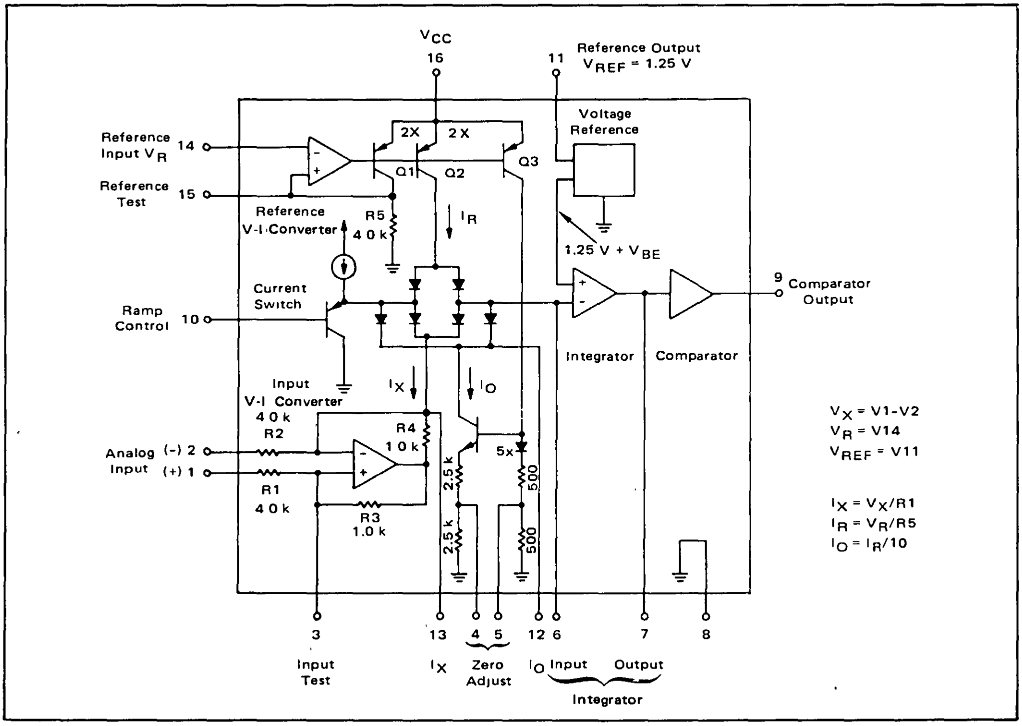
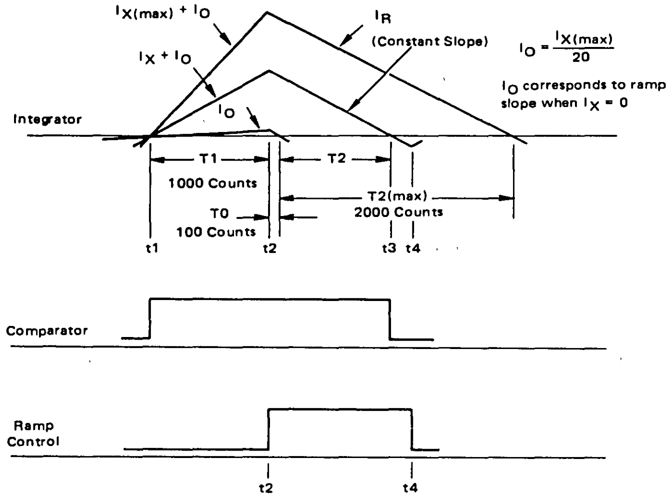


FIGURE 8 – MC1505 SYSTEM TIMING DIAGRAM
(2.0 Volt Full Scale Input)



$$(I_X + I_O)\,T1 = I_R\,(T2 + TO)$$

$$\boxed{T2 = T1\left[\frac{I_X + I_O}{I_R}\right] - TO}$$

threshold is 1.25 volts.

The integrator is a single stage, wide bandwidth amplifier. Its low propagation delay and low output impedance minimize ramp spikes due to output current reversal during ramp turn-around. The input bias current is typically one part in 50,000 of the full scale current, so that its temperature change contributes negligible error. Gain and input offset voltage are not critical since the integrator is driven from current sources.

The comparator is designed for low hysteresis by maintaining a constant power dissipation regardless of output state. This hysteresis is typically 0.1 mV and remains constant with temperature variations, so that no measurable system error is contributed. Temperature variations in the value of the comparator threshold are not an error factor, since the only requirement is that the threshold remain constant during a given conversion cycle. Voltage gain of the comparator is 2,000,000 when driving CMOS, and 40,000 with one TTL load. The comparator output is slew rate controlled to provide output rise and fall times of approximately 80 ns. This minimizes noise generation which could affect system stability.

The system is zeroed and full scale calibrated by potentiometers which provide temperature compensation. All the other resistors are diffused in close proximity, yielding reference and unknown currents which have a closely tracking resistive temperature coefficient.

APPLICATIONS INFORMATION

The input configurations for the MC1505 are shown in Figure 11. Note that the differential input voltage must always remain the same polarity with Pin 1 positive with respect to Pin 2. Figures 11 and 13 will aid in the understanding of the input circuitry.

The input common mode rejection of the MC1505 is high enough to maintain rated accuracy with small changes in common mode voltage, such as would be seen with ground errors and noise. The system must be recalibrated, however, for larger changes in common mode input voltage.

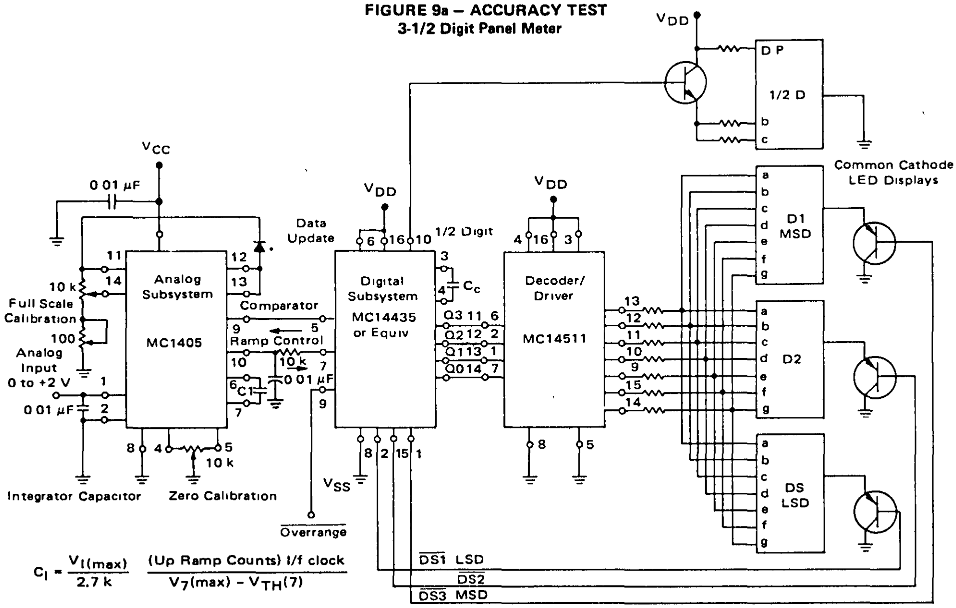
The MC1505 is arranged so that $I_X = I_R$ when $V_X = V_R$, or so that the ramp slopes are equal for input and reference voltages of 1 volt. As shown in Figure 8, a system with a 2 volt full-scale input requires twice as many digital counts during T2 as for T1. A system with a 1 volt full scale would require an equal number of counts in T1 and T2. Figure 9 illustrates a 3-1/2 digit system, but typical accuracies of the MC1505 allow its use in 4 digit applications. It can also be used in systems which require 4-1/2 digit resolution.

The ramp offset current and 100 count delay are shown in Figure 8. In certain applications, a different number of counts may be used. The system will not always operate properly, however, with a 10 count delay since the ramp offset current is used to zero the system and compensate for error in the input resistor bridge. This error, known as I_{XO}, is current which flows to or from the input converter with zero volts applied to the input. It is typically between ±5.0 µA, which is 1% of full scale in a 2 volt system. A 10 count delay would need a 0.5% ramp offset current, which would not always be able to cancel this error. Also, a 10 count delay does not provide enough signal-to-noise margin for consistently accurate low-level conversion.

The integrating capacitor is chosen with the equations shown in Figure 9. The maximum ramp voltage should be used for best signal-to-noise ratio, but temperature changes in I_X, I_R and the capacitor should be anticipated to prevent integrator saturation. Variations in clock frequency should also be considered. A polar capacitor with Pin 7 at the + terminal may be used. However, settling time will be increased when electrolytics are used, Tantalum electrolytics are preferred.

The lower half of the diode current switch is split with separate diodes for I_X and I_O. In most applications Pins 12 and 13 will be connected so that the two device emitters are effectively one, since the main purpose of these pins is for testing. Connecting these pins allows proper system zero adjustment and prevents turn-off of the switch diode with low unknown current levels. This yields better conversion accuracy.

FIGURE 9a – ACCURACY TEST
3-1/2 Digit Panel Meter

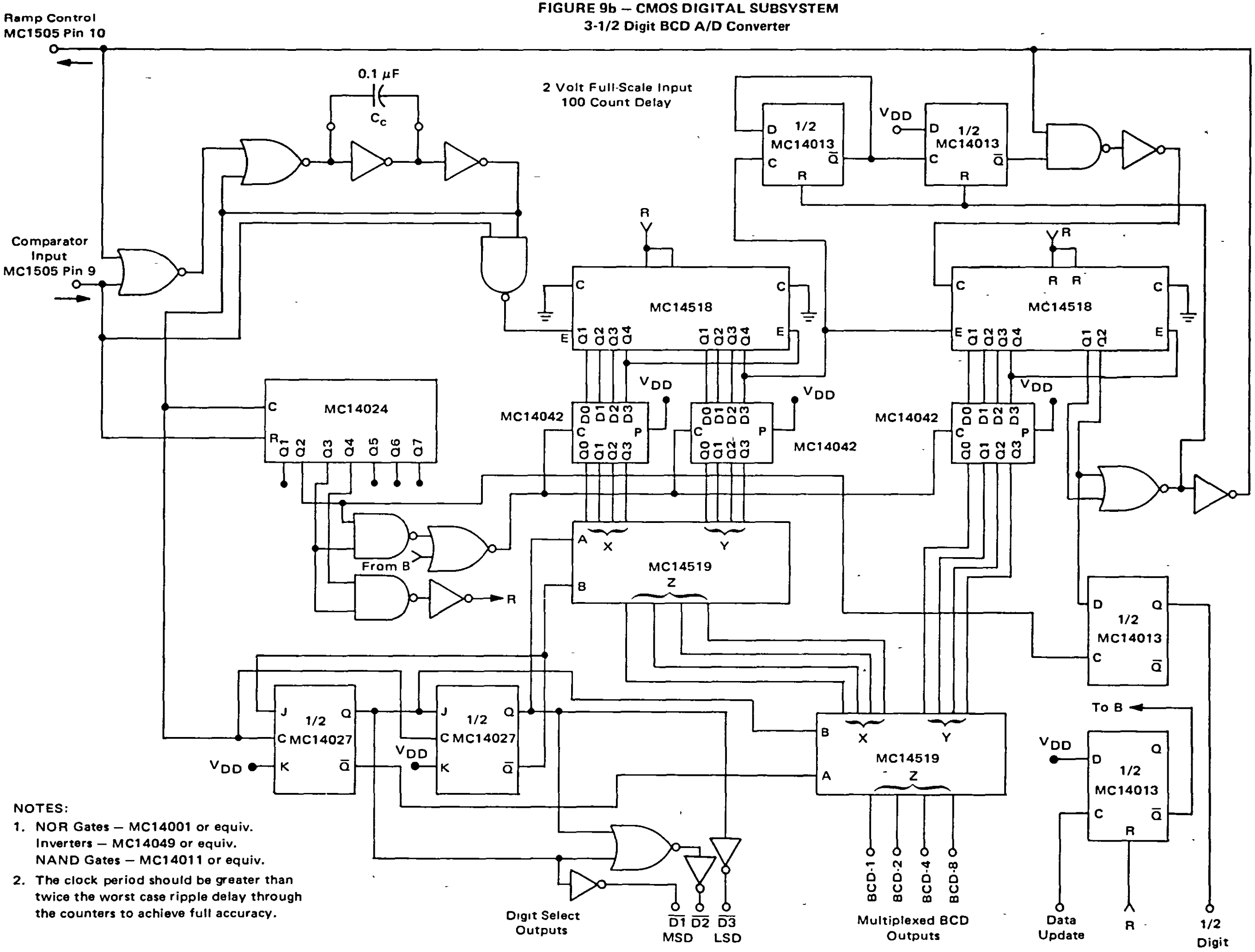


$$C_I = \frac{V_{I(max)}}{2.7\ k} \cdot \frac{(\text{Up Ramp Counts})\ 1/f\ \text{clock}}{V_7(max) - V_{TH}(7)}$$

See Electrical Characteristics Table
V_7 (max) is typically V_{CC} -2.0 V
$V_{TH(7)}$ is typically 1.0 V

*Optional Clamp diode on Pin 13, may be needed for recovery from negative differential inputs.

FIGURE 9b — CMOS DIGITAL SUBSYSTEM
3-1/2 Digit BCD A/D Converter



NOTES:

1. NOR Gates — MC14001 or equiv.
   Inverters — MC14049 or equiv.
   NAND Gates — MC14011 or equiv.
2. The clock period should be greater than twice the worst case ripple delay through the counters to achieve full accuracy.

FIGURE 9c – FUNCTIONAL DIAGRAM OF MC14435 CMOS DIGITAL SUBSYSTEM

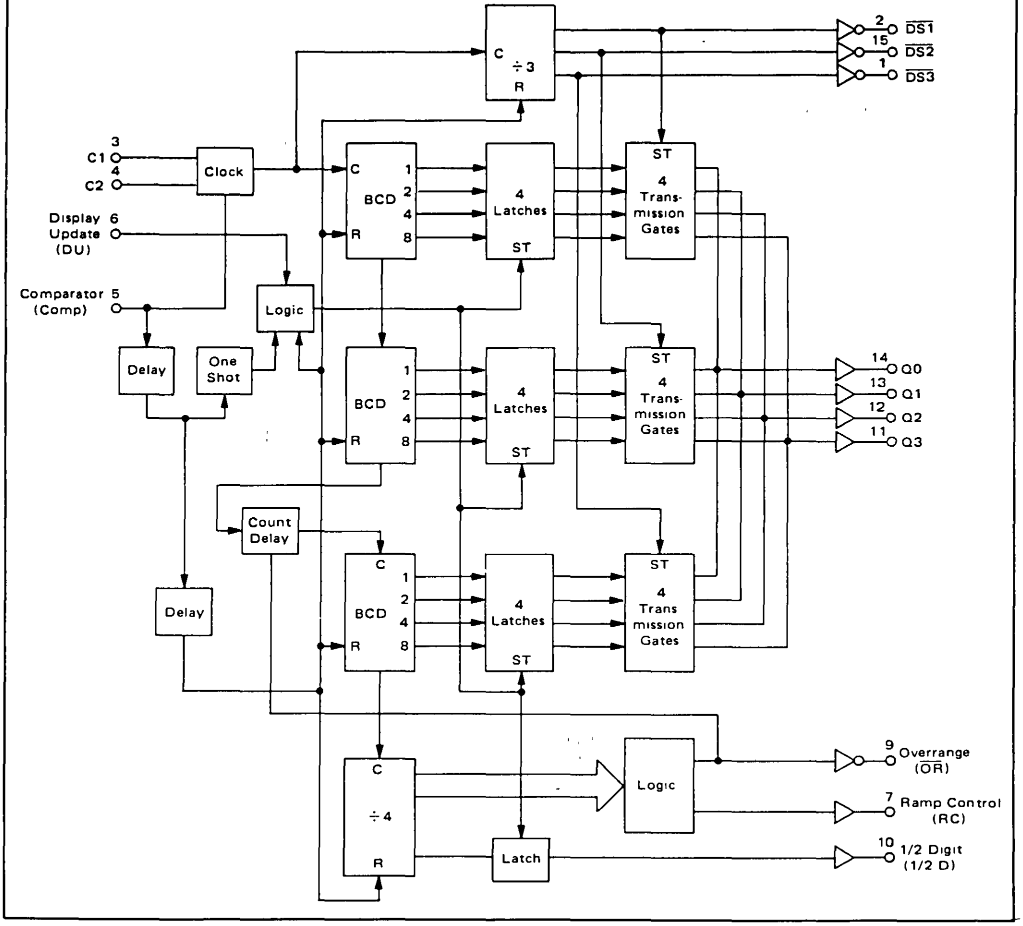
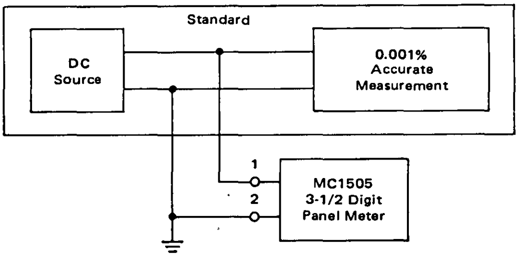


FIGURE 10 – CALIBRATION SET-UP



Zero Calibration.

Set standard at 0.0005 V.

Adjust zero potentiometer for panel meter display transition between 0.000 and 0.001 V. Note: An analog input of –1 mV yields a reading of 0.099.

Repeat zero and full scale calibration until meter is calibrated at both ends of the scale.

Full Scale Calibration:

Set standard at 1.9995 V.

Adjust full scale potentiometer for panel meter display transition between 1.999 and 1.000 V. (overrange)

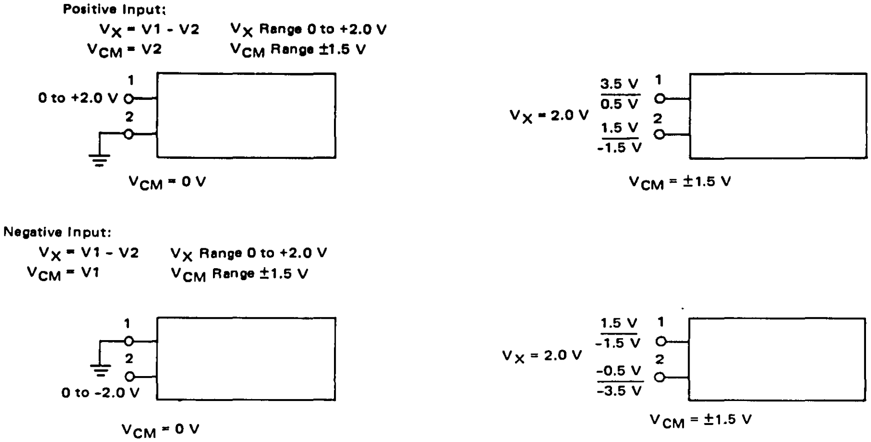
Linearity Test:

Adjust standard for the desired panel meter transition and record the value of the standard.

At initial turn-on, set Pin 14 to ≈1.0 Volt with full scale potentiometer

FIGURE 11 – ANALOG INPUT RANGE

The input circuit for the MC1505 has a unipolar differential input range of +2 volts and a bipolar common mode input range of ±1.5 volts.



Positive Input:

$V_X = V1 - V2$ V_X Range 0 to +2.0 V

$V_{CM} = V2$ V_{CM} Range ±1.5 V

Negative Input:

$V_X = V1 - V2$ V_X Range 0 to +2.0 V

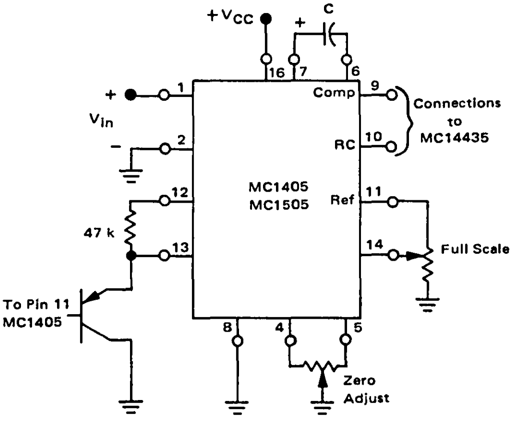
$V_{CM} = V1$ V_{CM} Range ±1.5 V

Allowable Pin Voltages:
Pin 1: -1.5 V to +3.5 V
Pin 2: -3.5 V to +1.5 V

FIGURE 12 – CIRCUIT TO PREVENT POSSIBLE LATCHUP WITH APPLICATION OF NEGATIVE INPUT VOLTAGES

The MC1405/1505 A/D analog subsystem is intended for positive input voltages only (i.e., pin 1 positive with respect to pin 2). However, should pin 2 become more than 100 mV positive with respect to pin 1, the internal input amplifier may go into a latchup mode which will require that the system power be turned off and then reapplied to reset the system. To prevent this problem a PNP transistor can be used as shown in the accompanying figure. The base-emitter junction of the transistor clamps pin 13 at one diode drop above the reference voltage (pin 11) to prevent the latchup. The gain of the transistor insures that the reference need not sink more than 500 μA of current.

The 47 kΩ resistor is required only if the A/D system is to continue to convert under reverse polarity conditions such as for autopolarity schemes.



*47 kΩ resistor required if conversions are to continue during input polarity reversal, otherwise tie pins 12 and 13 together.

TYPICAL PERFORMANCE CURVES

FIGURE 13 – MAXIMUM COMMON-MODE INPUT VOLTAGE versus TEMPERATURE

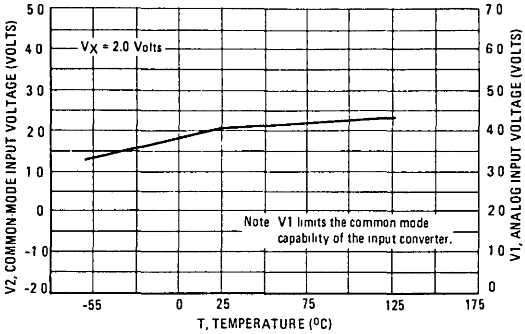


FIGURE 14 – INPUT CURRENT versus INPUT VOLTAGE

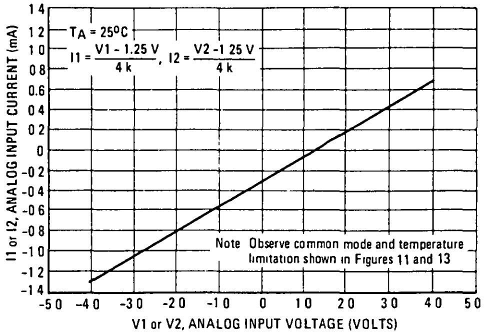


FIGURE 15 – UNKNOWN CURRENT versus ANALOG INPUT VOLTAGE

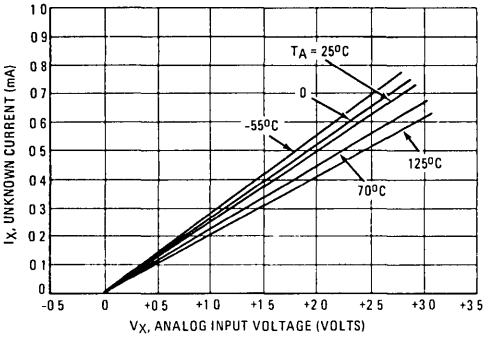


FIGURE 16 – REFERENCE CURRENT versus REFERENCE INPUT VOLTAGE

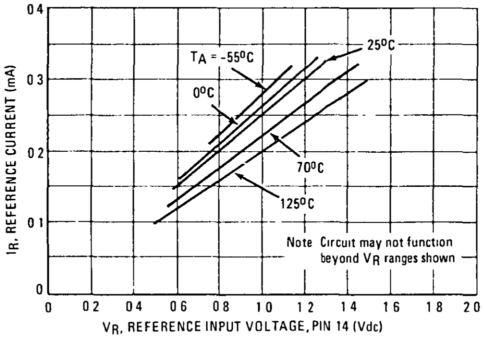


FIGURE 17 – TYPICAL POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

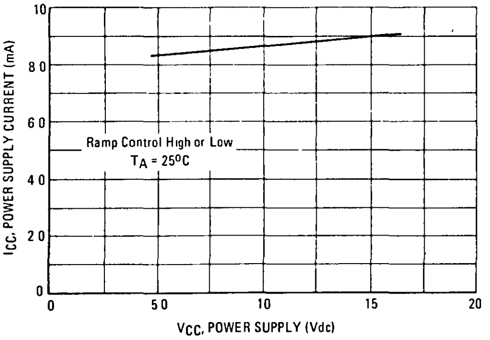


FIGURE 18 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

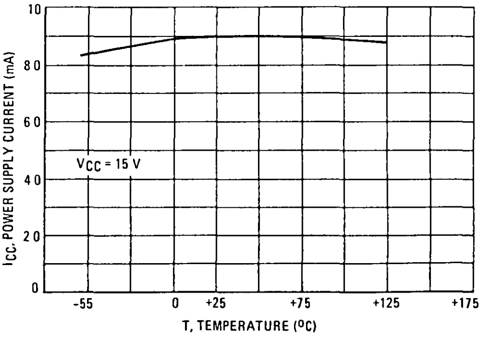


FIGURE 19 – CURRENT SWITCH TRANSFER CHARACTERISTIC

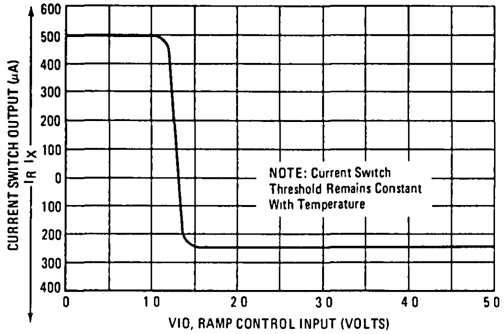


FIGURE 20 – INTEGRATOR OUTPUT SWING versus TEMPERATURE

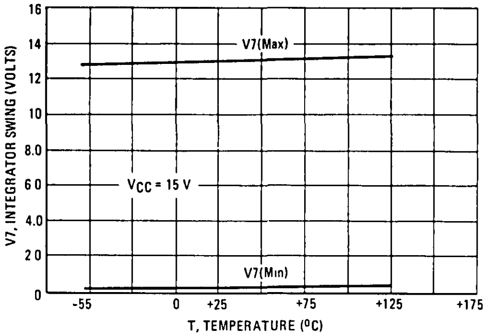


FIGURE 21 – COMPARATOR THRESHOLD versus TEMPERATURE

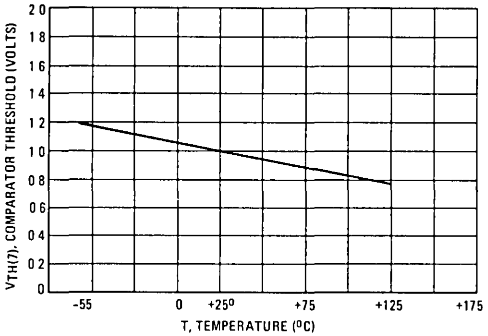


FIGURE 22 – RAMP CURRENT RATIO versus POWER SUPPLY

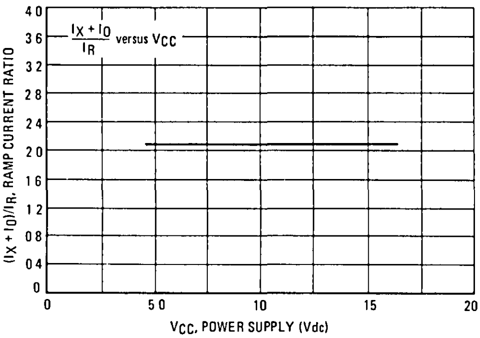
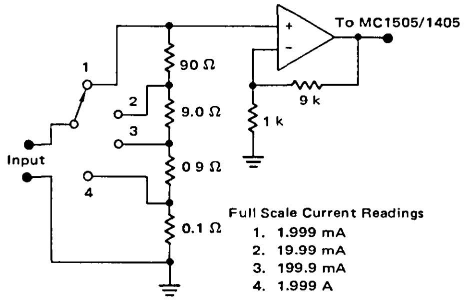


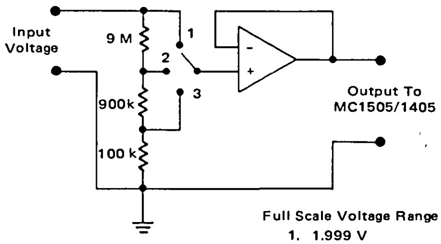
FIGURE 23 – CURRENT MEASUREMENT CIRCUITRY



Full Scale Current Readings
1. 1.999 mA
2. 19.99 mA
3. 199.9 mA
4. 1.999 A

If a voltage drop of 2 0 V full scale can be tolerated the resistors may be increased by a factor of ten and a unity gain buffer may be employed.

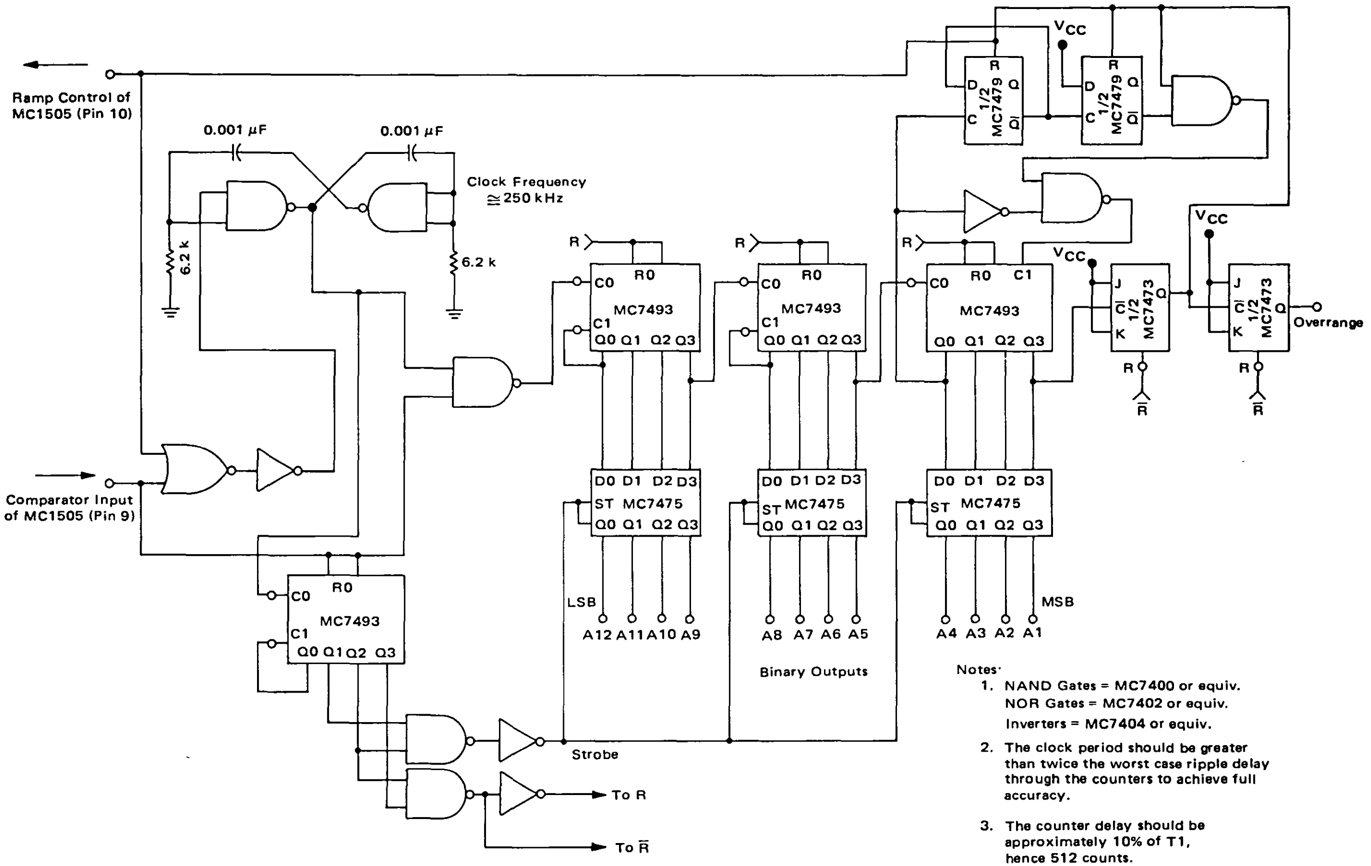
FIGURE 24 – DVM VOLTAGE RANGING



Full Scale Voltage Range
1. 1.999 V
2. 19 99 V
3 199.9 V

FIGURE 25 – MTTL DIGITAL SUBSYSTEM

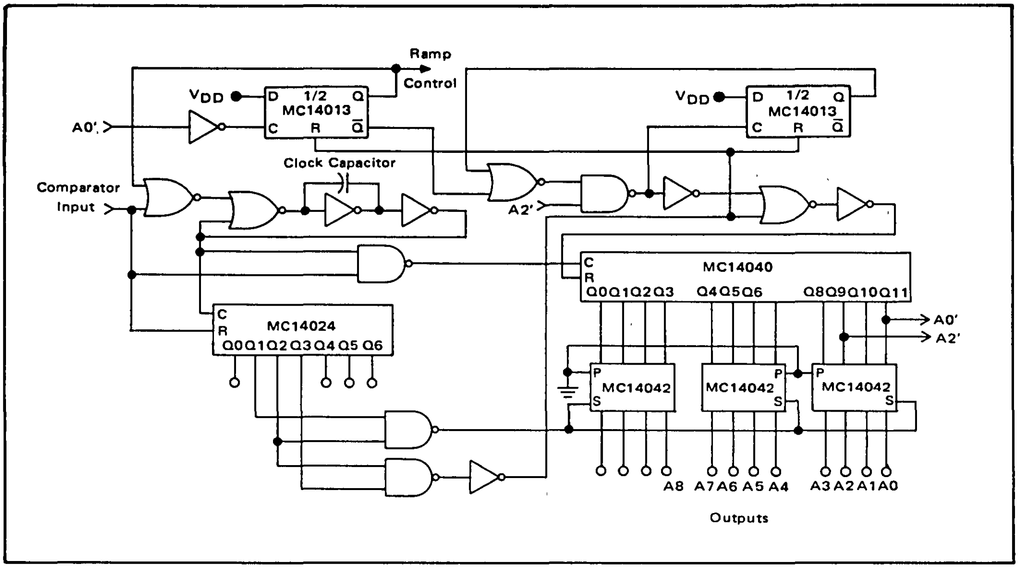
12 Bit Binary A/D Converter
(1.0 Volt Full Scale, 512 Count Delay)



Notes:

1. NAND Gates = MC7400 or equiv.
   NOR Gates = MC7402 or equiv.
   Inverters = MC7404 or equiv.
2. The clock period should be greater than twice the worst case ripple delay through the counters to achieve full accuracy.
3. The counter delay should be approximately 10% of T1, hence 512 counts.

FIGURE 26 – 12-BIT BINARY A/D LOGIC SUBSYSTEM USING CMOS



MOTOROLA

MC1406L
MC1506L

Specifications and Applications Information

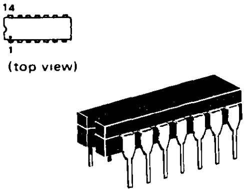
SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy – ±0.78% Error maximum
- Low Power Dissipation – 85 mW typical @ ±5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time -- 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – OUTPUT CURRENT SETTLING TIME
(ALL BITS SWITCHED, R_L = 50 Ω)

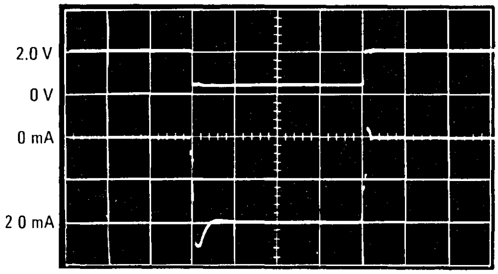
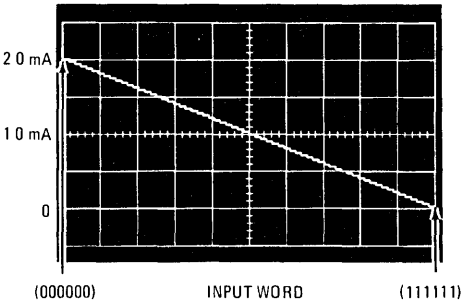


FIGURE 2 – D-to-A TRANSFER CHARACTERISTICS



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Digital-to-Analog Meter Readout
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Digital Varicap Tuning
- Video Systems
- Stepping Motor Drive
- CRT Character Generation
- Digital Addition and Subtraction
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Programmable Power Supplies
- Speech Encoding

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16 5	Vdc
Digital Input Voltage	V_5 thru V_{10}	+8.0, V_{EE}	Vdc
Applied Output Voltage	V_O	±5.0	Vdc
Reference Current	I_{12}	5.0	mA
Reference Amplifier Inputs	V_{12}, V_{13}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1506L MC1406L	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R12}$ = 2.0 mA, all logic inputs in low logic state, T_A = T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	10	E_r	–	–	±0 78	%
Settling Time (within 1/2 LSB [includes t_d] T_A = +25°C)	9	t_S	–	150	300	ns
Propagation Delay Time T_A = +25°C	9	t_{PHL}, t_{PLH}	–	10	50	ns
Output Full Scale Current Drift		$\|TCI_O\|$	–	80	–	PPM/°C
Digital Input Logic Levels High Level, Logic "1" Low Level, Logic "0"	3,14	 V_{IH} V_{IL}	 2.4 –	 – –	 – 0 8	Vdc
Digital Input Current High Level, V_{IH} = 5 0 V Low Level, V_{IL} = 0.8 V	3,13	 I_{IH} I_{IL}	 – –	 0 -0 7	 +0.01 -1 5	mA
Reference Input Bias Current (Pin 13)	3	I_{13}	–	-0.002	-0.01	mA
Output Current Range V_{EE} = -5 0 V V_{EE} = -6 0 to -15 V	3	I_{OR}	 0 0	 2 0 2 0	 2.1 4 2	mA
Output Current V_{ref} = 2.000 V, R_{12} = 1.000 kΩ	3	I_O	 1 9	 1.97	 2.1	mA
Output Current (all bits high)	3	$I_O(min)$	 –	 0	 10	µA
Output Voltage Compliance ($E_r \leqslant$ ±0 78% at T_A = +25°C)	3,4,5	V_{O+} V_{O-}	– –	+0.25 -0 45	+0 1 -0.3	Vdc
Reference Current Slew Rate (T_A = +25°C)	8,15	SR I_{ref}	 –	 2.0	 –	mA/µs
Output Current Power Supply Sensitivity	10	PSRR (–)	–	0 002	0 010	mA/V
Power Supply Current A1 thru A6; V_{IL} = 0 8 V A1 thru A6; V_{IH} = 2.4 V	3,11,12	 I_{CC} I_{EE}	 – –	 +7 2 -9.0	 +11 -11	mA
Power Dissipation (all bits high) V_{EE} = -5 0 Vdc V_{EE} = −15 Vdc		P_D	 – –	 85 175	 120 240	mW

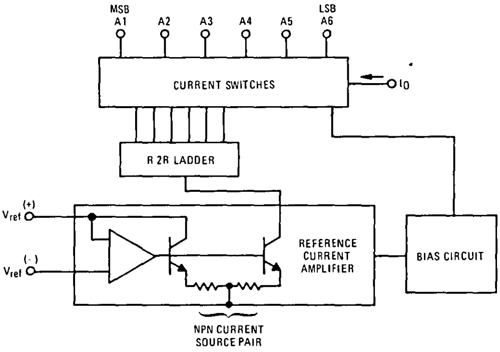
*T_{high} = +70°C for MC1406L T_{low} = 0°C for MC1406L
= +125°C for MC1506L   = -55°C for MC1506L

The MC1506L consists of a reference current amplifier, and R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

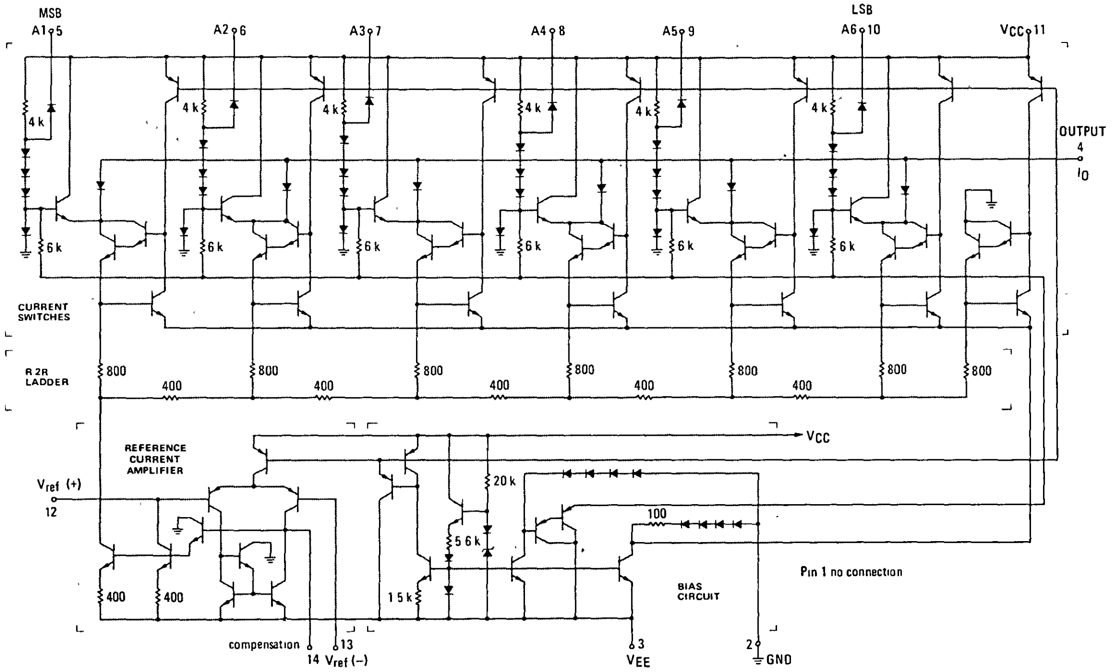
The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

BLOCK DIAGRAM

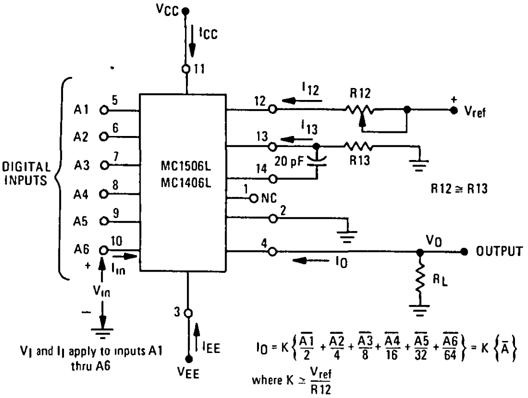


COMPLETE CIRCUIT SCHEMATIC
(Digital Inputs; pins 5,6,7,8,9,10)



TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



$I_O = K\left\{\frac{\overline{A1}}{2}+\frac{\overline{A2}}{4}+\frac{\overline{A3}}{8}+\frac{\overline{A4}}{16}+\frac{\overline{A5}}{32}+\frac{\overline{A6}}{64}\right\} = K\left\{\overline{A}\right\}$

where $K \simeq \frac{V_{ref}}{R12}$

and $\overline{A_N} = 0$ if A_N is at high level

$\overline{A_N} = 1$ if A_N is at low level

FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

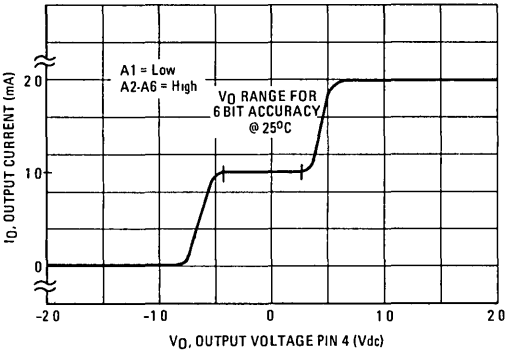


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

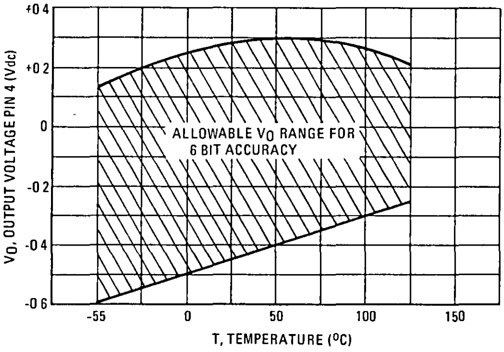


FIGURE 6 – POSITIVE V_{ref}

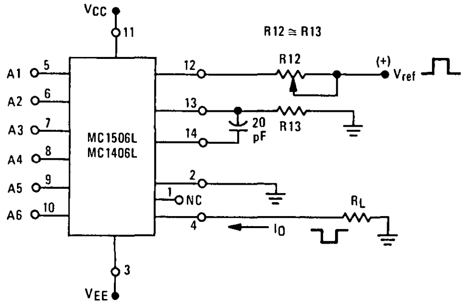


FIGURE 7 – NEGATIVE V_{ref}

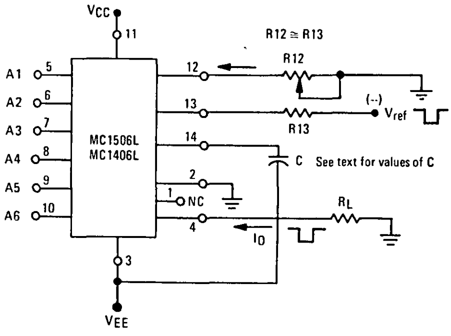
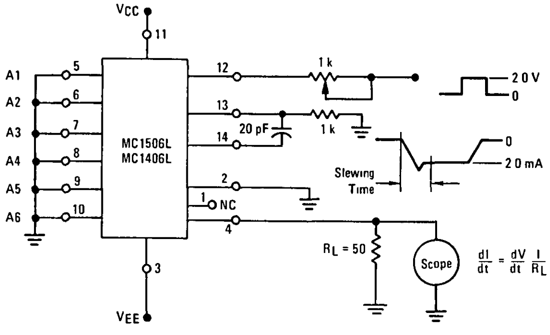


FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT



TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – TRANSIENT RESPONSE

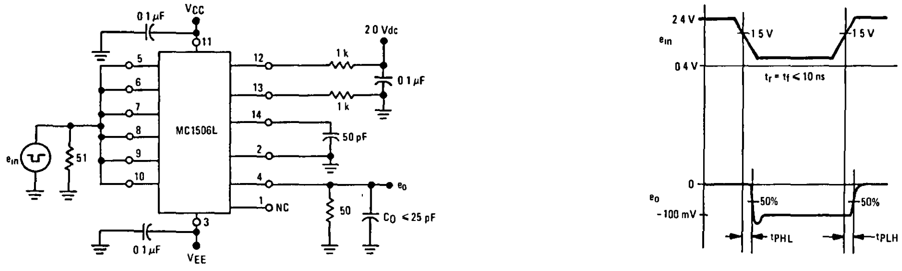
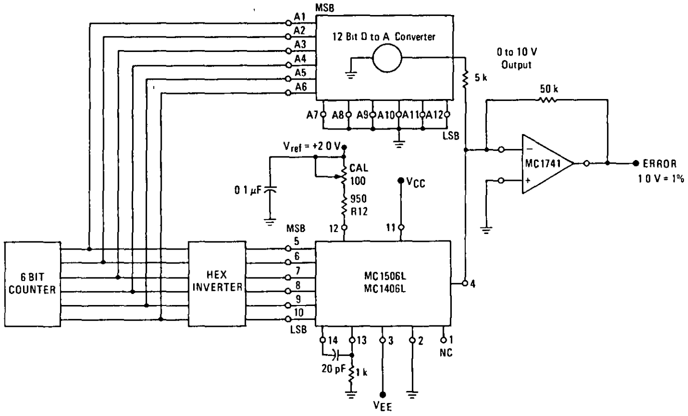


FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT



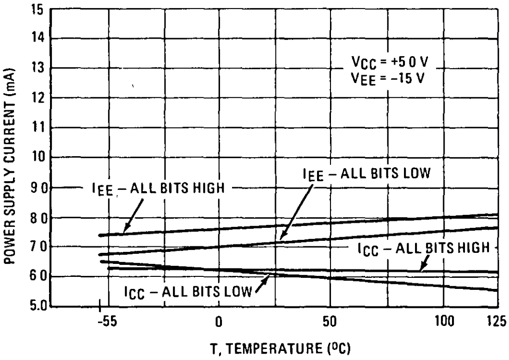


FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

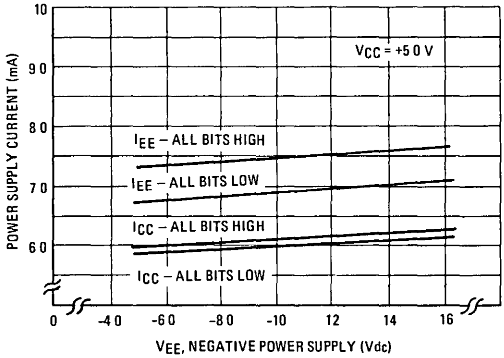


FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus V_{EE}

TYPICAL CHARACTERISTICS (continued)

FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

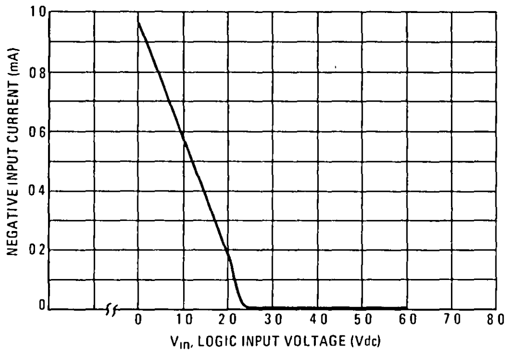


FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")

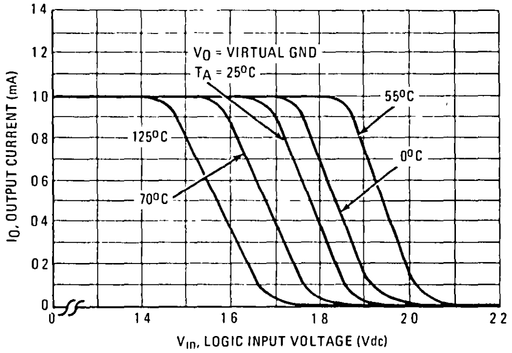
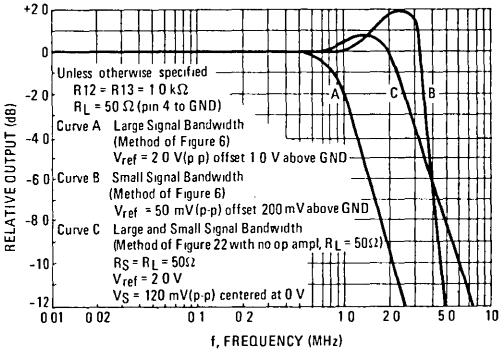


FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE



GENERAL INFORMATION

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

Output Voltage Compliance

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on Pin 4 to maintain six-bit accuracy is +0.1 to -0.3 Volts. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from Pin 4 to ground is 150 ohms.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to Pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

GENERAL INFORMATION (continued)

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of ±1/2 of one part in 4096, or ±0.012%, which is more accurate than the ±0.78% specification provided by the MC1506L.

Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64.1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of 6.0 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 60 μA to 4.0 mA, the 6.0 μA contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within ±1/2 LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at Pin 12 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into Pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from Pin 14 to Pin 13. This compensation method yields the best slew rate, typically better than 2.0 mA/μs, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at Pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to V_{EE}. The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

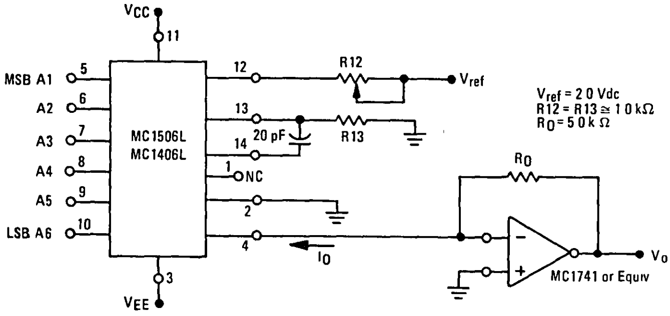
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to V_{EE} on Pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above V_{EE}. Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at Pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 12 and ground.

If Pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) = K\, R_O \left\{ \bar{A} \right\}$$

Adjust R_{ref} so that V_O with all digital inputs at low level is equal to 9 844 volts

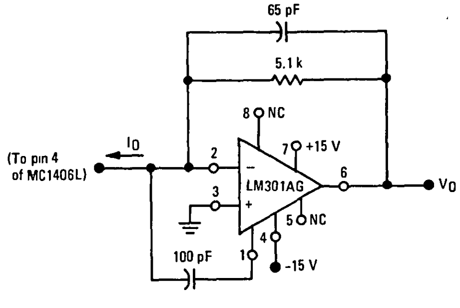
$$V_O = \frac{2\ V}{1\ K}(5\ K)\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}\right) = 10\ V\left(\frac{63}{64}\right) = 9\ 844\ V$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

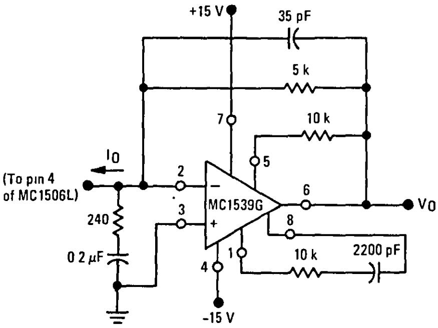
The following circuit shows how the LM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17

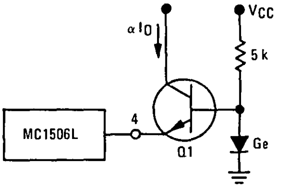


An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs.

FIGURE 18



The positive voltage range may be extended by cascoding the output with a high beta common base transistor, Q1, as shown.



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

APPLICATIONS INFORMATION (continued)

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

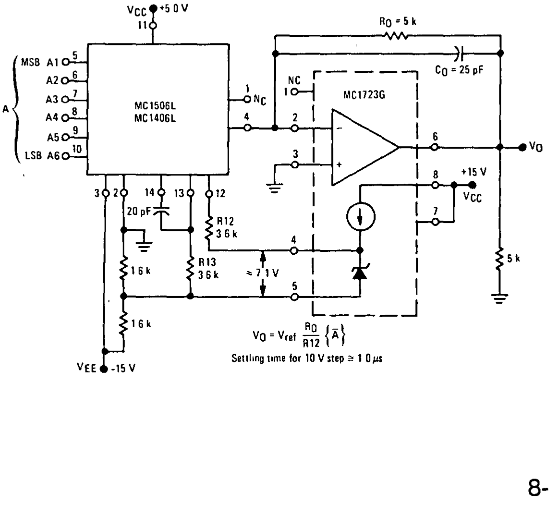
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ±0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ±0.25 volt.

FIGURE 19 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



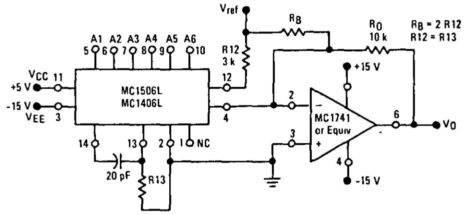
$$V_O = V_{ref}\ \frac{R_O}{R12}\left\{A\right\}$$

Settling time for 10 V step ≅ 1.0 µs

Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

FIGURE 20 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT

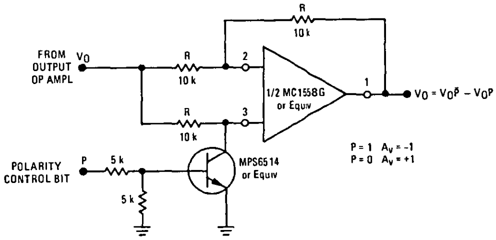


$$V_O = \frac{V_{ref}}{R12}\ (R_O)\ \left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) - \frac{V_{ref}}{R_B}\ (R_O)$$

Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 – POLARITY SWITCHING CIRCUIT (6-Bit Magnitude Plus Sign D-to-A Converter)



$V_O = V_O\bar{P} - V_OP$

P = 1 $A_V = -1$
P = 0 $A_V = +1$

APPLICATIONS INFORMATION (continued)

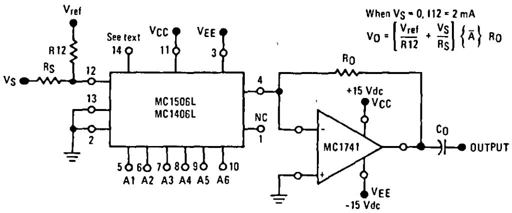
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

The best frequency response is obtained by not allowing I_{12} to reach zero. R_S can be set for a ±1.0 mA variation in relation to I_{12}. I_{12} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



When $V_S = 0$, $I_{12} = 2$ mA

$$V_O = \left[\frac{V_{ref}}{R12} + \frac{V_S}{R_S}\right]\left\{\bar{A}\right\} R_O$$

Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or V_{ref}.

FIGURE 23 – PANEL METER READOUT CIRCUIT

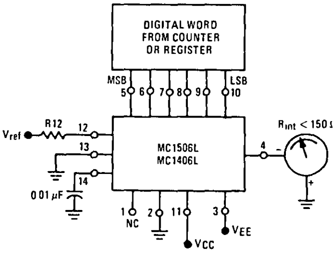
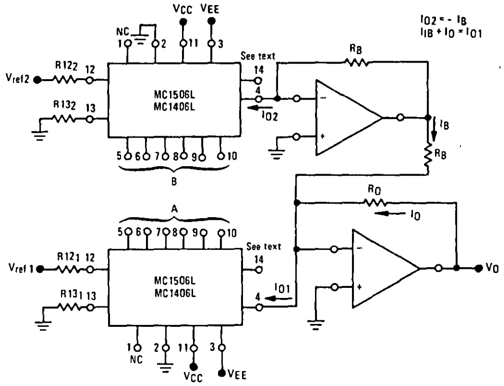


FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$I_{O2} = -I_B$

$I_B + I_O = I_{O1}$

$$I_O = I_{O1} - I_{O2} = \frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\} - \frac{V_{ref2}}{R12_2}\left\{\bar{B}\right\}$$

Digital Subtraction

$$\text{let } \frac{V_{ref1}}{R12_1} = \frac{V_{ref2}}{R12_2}$$

$$V_O = \frac{V_{ref1}}{R12_1} R_O \left|\left\{\bar{A}\right\} - \left\{\bar{B}\right\}\right|$$

Programmable Amplifier

Connect digital inputs so A = B

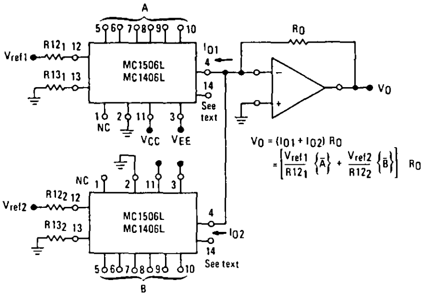
$$V_O = \left\{\bar{A}\right\}\left|\frac{V_{ref1}}{R12_1} - \frac{V_{ref2}}{R12_2}\right|$$

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R12_1$ and $R12_2$ or $R13_1$ and $R13_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R12_1$ and $R12_2$ to a positive reference higher than the most positive input, and drive $R13_1$ and $R13_2$. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

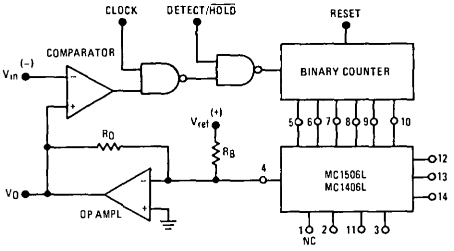
APPLICATIONS INFORMATION (continued)

FIGURE 25 – DIGITAL SUMMING and CHARACTER GENERATION



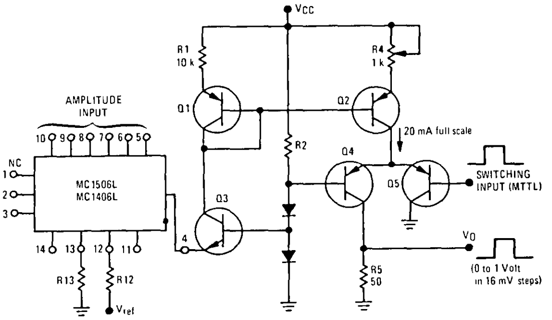
In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

FIGURE 26 – PEAK DETECTING SAMPLE and HOLD
(Features infinite hold time and optional digital output.)



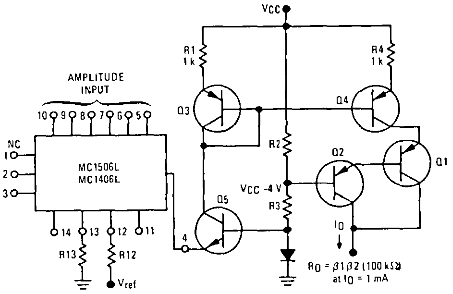
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

FIGURE 27 – PROGRAMMABLE PULSE GENERATOR



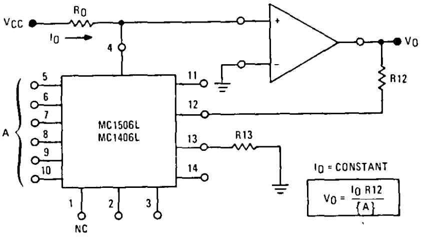
Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input

FIGURE 28 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

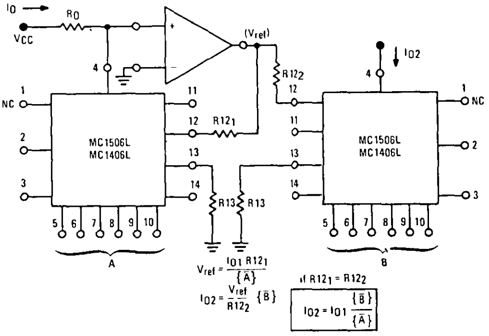
FIGURE 29 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 62 μA so that I_{12} will have a maximum value of 3.938 mA for a digital bit input configuration of 111110.

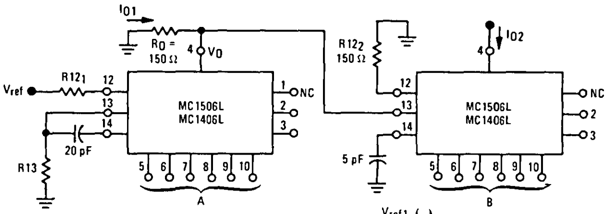
Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 30 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



APPLICATIONS INFORMATION (continued)

FIGURE 31 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = I_{O1}\,R_O = \frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\} R_O$$

$$I_{O2} = -\frac{\left\{\bar{B}\right\}\,|V_O|}{R12_2}$$

$$= \frac{\left\{\bar{B}\right\}}{R12_2}\left[R_O\left(\frac{V_{ref1}}{R12_1}\right)\left\{\bar{A}\right\}\right]$$

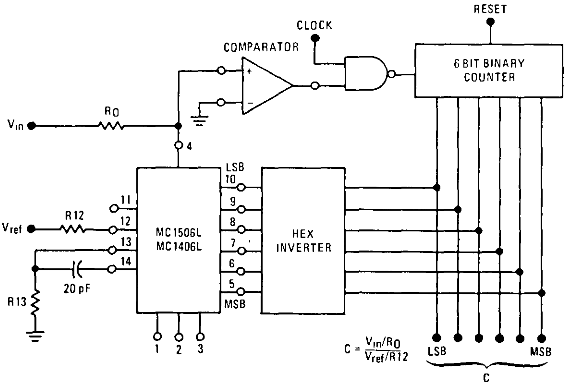
since $R_O = R12_2$ and $K = V_{ref}/R12_1$

$$\boxed{I_{O2} = K\left\{\bar{A}\right\}\left\{\bar{B}\right\}}$$ K can be an analog variable

Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

FIGURE 32 – DIGITAL QUOTIENT of TWO ANALOG VARIABLES
or ANALOG-TO-DIGITAL CONVERSION



The circuit shown is a simple counter-ramp converter An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA

MC1408
MC1508

Specifications and Applications Information

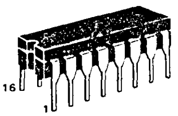
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

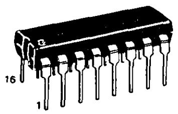
- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0 4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/µs
- Standard Supply Voltages +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

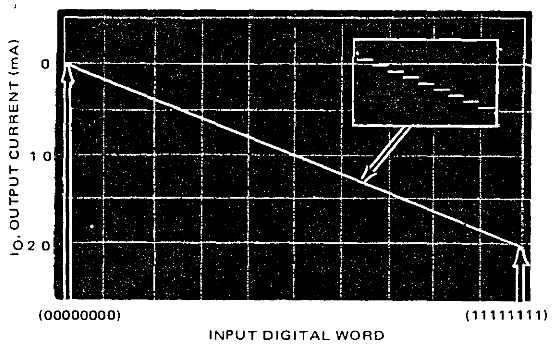
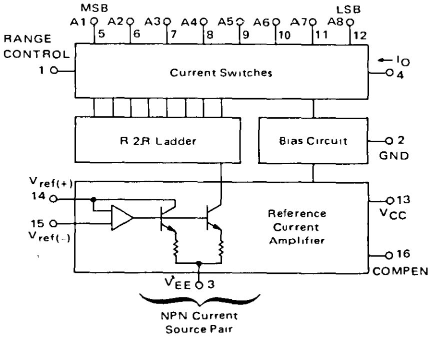


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5 5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5 5	Vdc
Applied Output Voltage	V_O	+0 5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 0 Vdc, V_{EE} = -15 Vdc, $\frac{Vref}{R14}$ = 2 0 mA, MC1508L8 T_A = -55°C to +125°C, MC1408L Series. T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

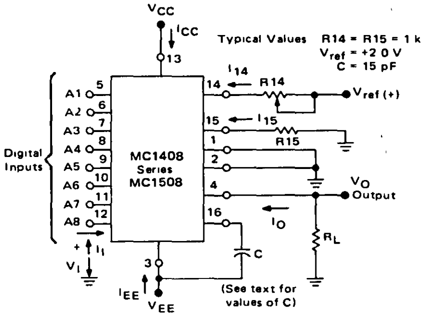
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8 MC1408P7, MC1408L7, See Note 1 MC1408P6, MC1408L6, See Note 1	4	E_r	 – – –	 – – –	 ±0 19 ±0 39 ±0.78	%
Settling Time to within ±1/2 LSB [includes t_{PLH}](T_A=+25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH}, t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	- 20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2 0 –	 – –	 – 0 8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5 0 V Low Level, V_{IL} = 0 8 V	3	 I_{IH} I_{IL}	 – –	 0 -0 4	 0 04 -0 8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5 0	µA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2 0	 2.1 4 2	mA
Output Current V_{ref} = 2 000 V, R14 = 1000 Ω	3	I_O	 1 9	 1 99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4 0	µA
Output Voltage Compliance ($E_r \leq$ 0 19% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0 55, +0 4 -5 0, +0 4	Vdc
Reference Current Slew Rate	6	$SR\ I_{ref}$	–	4 0	–	mA/µs
Output Current Power Supply Sensitivity		PSRR(–)	–	0 5	2 7	µA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13 5 -7 5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4 5 -4 5	+5 0 -15	+5 5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5 0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5 0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current

Note 2. All bits switched

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

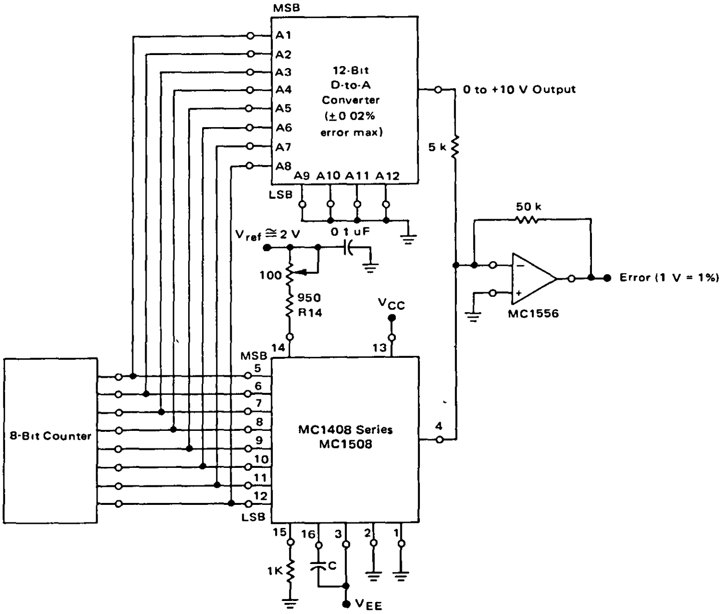
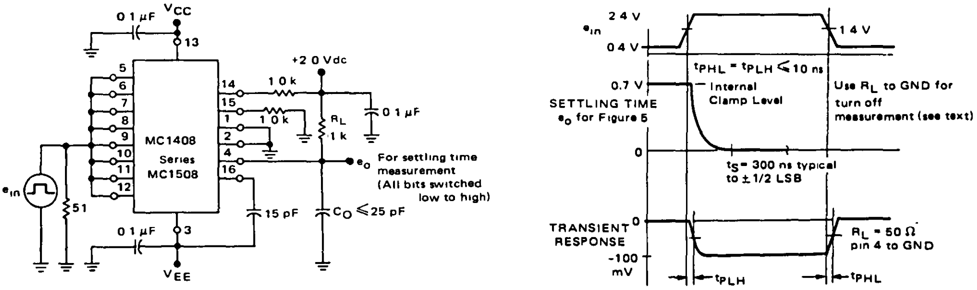


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

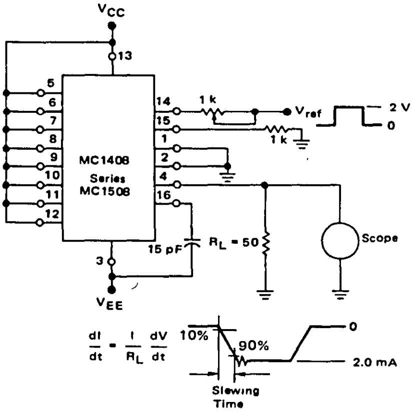


FIGURE 7 – POSITIVE V_{ref}

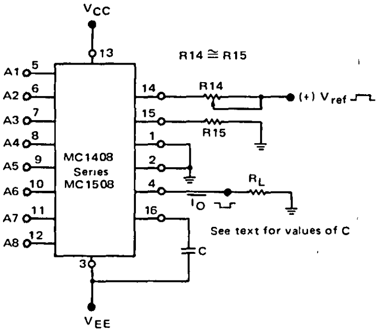


FIGURE 8 – NEGATIVE V_{ref}

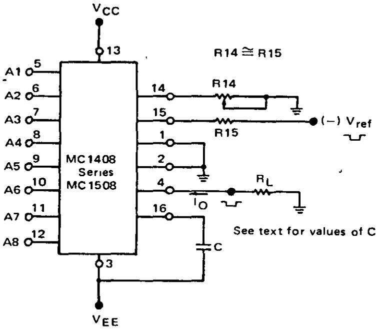
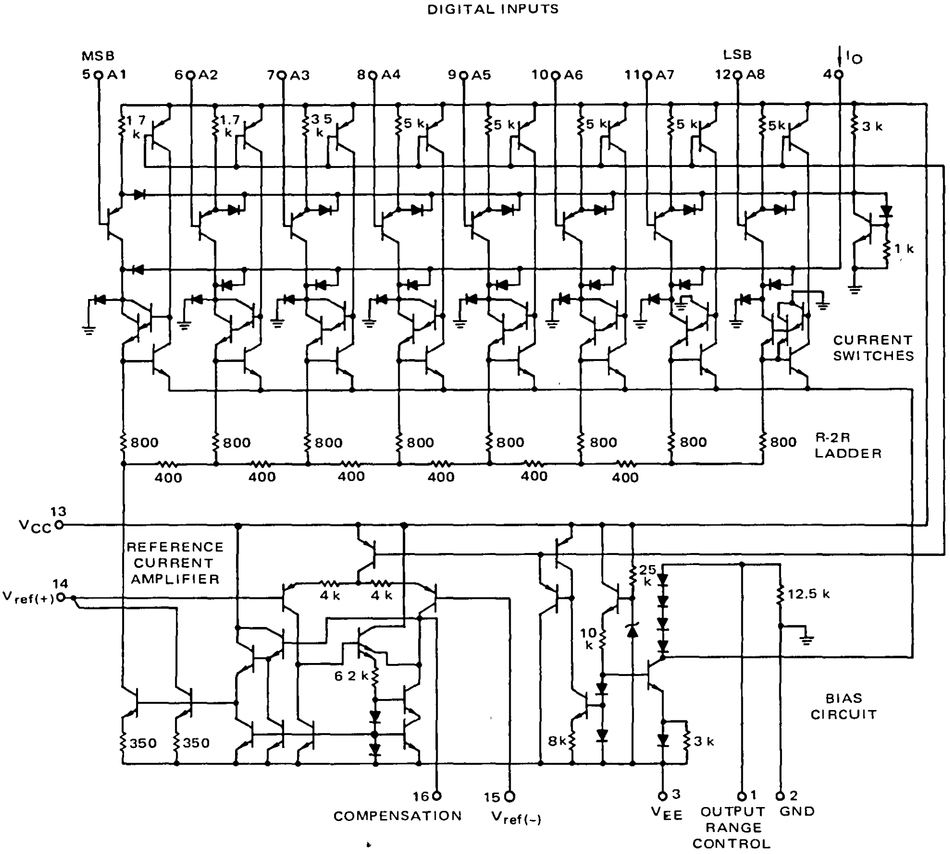


FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches For many applications, only a reference resistor and reference voltage need be added

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1 992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin, for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3 0-volts above the V_{EE} supply Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5 0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5 0 V through another resistor and bypassing the junction of the two resistors with 0 1 µF to ground. For reference voltages greater than 5 0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level When a current switch is turned "on", the negative output voltage range is restricted The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level

The negative output voltage compliance of the MC1408 may be extended to -5 0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1 2 µs (when all bits are switched on) Refer to the subsequent text section on Settling Time for more details on output loading

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing

Output Current Range

The output current maximum rating of 4 2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8 0 µA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2 1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4 The 12-bit converter is calibrated for a full scale output current of 1 992 mA This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0 00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256 1 The major source of error is the bias current of the termination amplifier Under "worst case" conditions, these eight amplifiers can contribute a total of 1 6 µA extra current at the output terminal If the reference current in the multiplying mode ranges from 16 µA to 4.0 mA, the 1 6 µA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word Typically, the MC1408 is monotonic for all values of reference current above 0 5 mA The recommended range for operation with a dc reference current is 0 5 to 4 0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

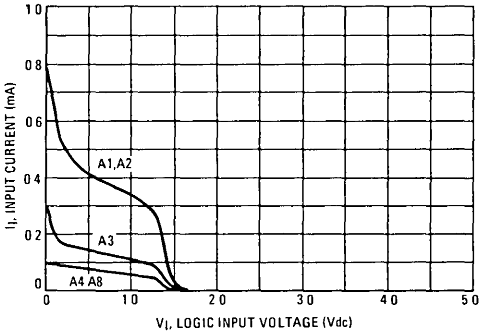


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

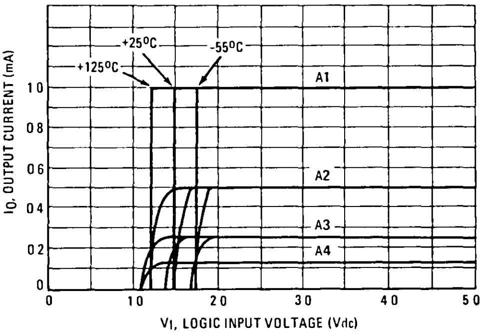


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

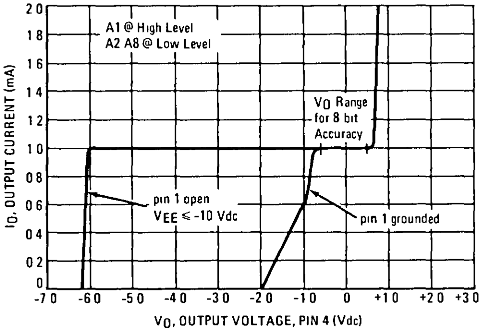
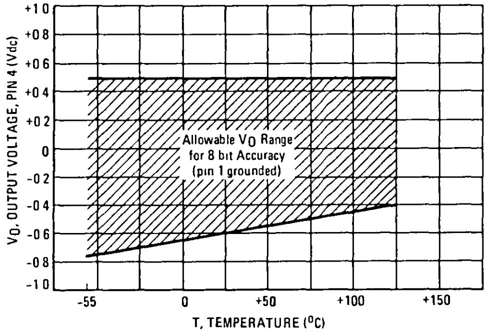


FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE

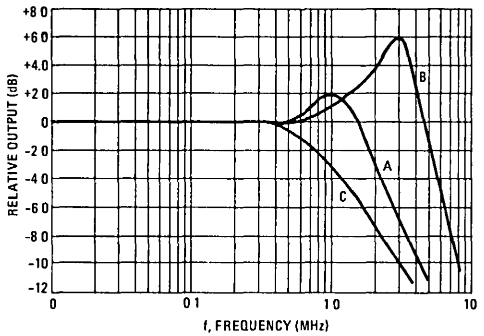
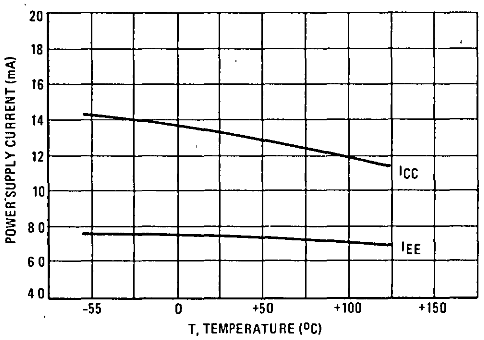


FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

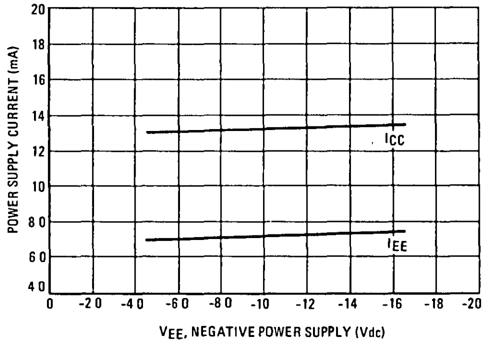


Unless otherwise specified

R14 = R15 = 1 0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

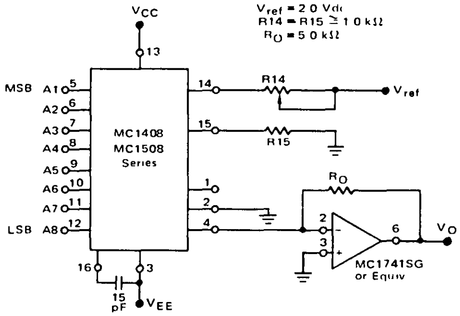
Curve A	Large Signal Bandwidth Method of Figure 7 V_{ref} = 2 0 V(p p) offset 1 0 V above GND
Curve B·	Small Signal Bandwidth Method of Figure 7 R_L = 250 Ω V_{ref} = 50 mV(p p) offset 200 mV above GND
Curve C	Large and Small Signal Bandwidth Method of Figure 25 (no op-ampl, R_L = 50 Ω) R_S = 50 Ω V_{ref} = 2.0 V V_S = 100 mV(p p) centered at 0 V

FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9 961 volts

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9\ 961\ V$$

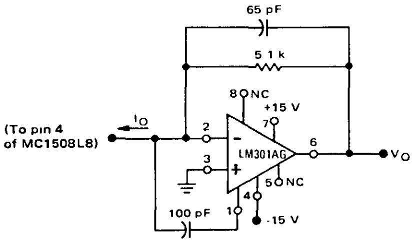
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

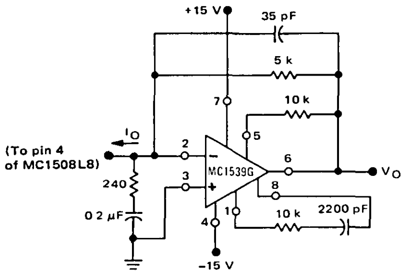
The following circuit shows how the LM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 18



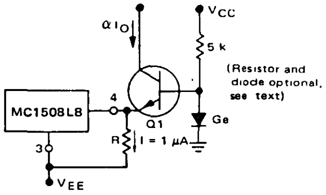
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 µs.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

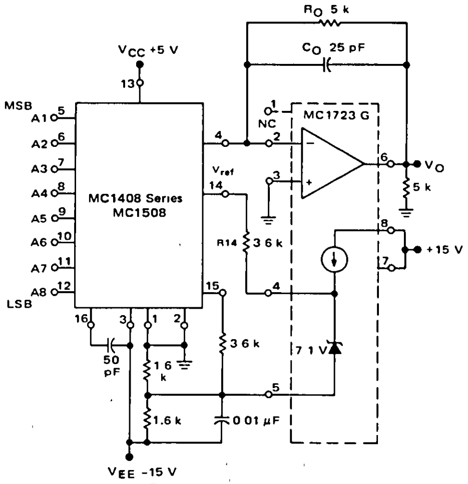
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt, or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



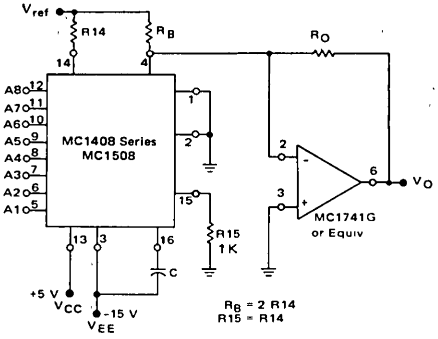
$V_O = V_{ref} = \frac{R_O}{R14}\{A\}$

Settling time for a 10 volt step ≅ 1 0 µs

Bipolar or Negative Output Voltage

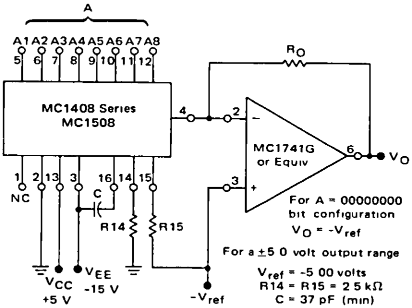
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary V_{ref} may be used as this auxiliary reference Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



For A = 00000000 bit configuration

$V_O = -V_{ref}$

For a ±5 0 volt output range

V_{ref} = -5 00 volts

R14 = R15 = 2 5 kΩ

C = 37 pF (min)

R_O = 5 kΩ

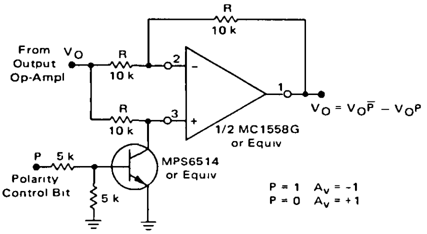
Decrease R_O to 2 5 kΩ for a 0 to -5 0-volt output range This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)



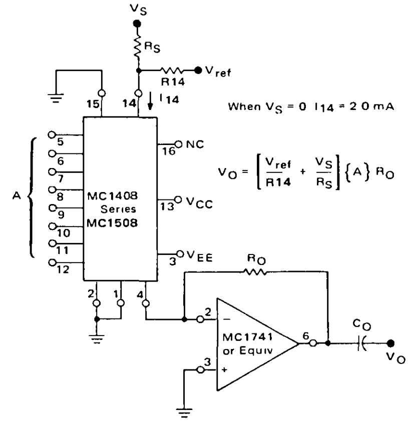
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

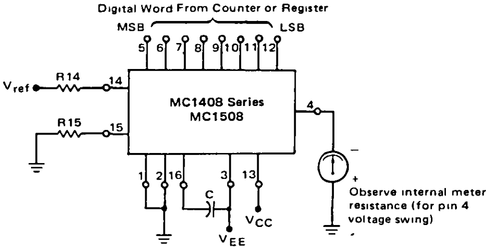
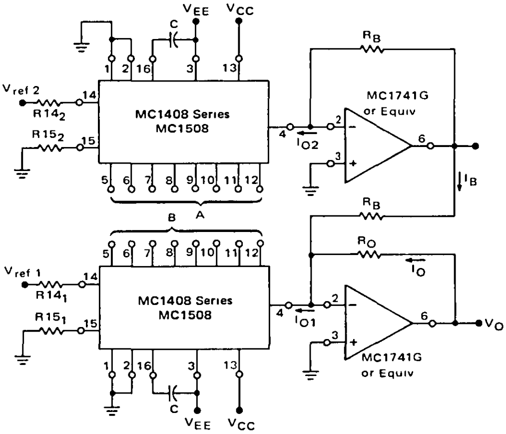


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}\{A\} - \frac{V_{ref\,2}}{R14_2}\{B\}$$

$$I_{O2} = -I_B$$

$$I_B + I_O - I_{O1}$$

Digital Subtraction

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier

Connect Digital Inputs so A = B

$$\boxed{V_O = \frac{V_{ref\,1}}{R14_1} R_O\left[\{A\} - \{B\}\right]}$$

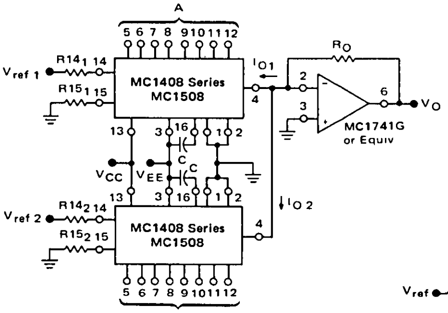
$$\boxed{V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]}$$

APPLICATIONS INFORMATION (continued)

This digital subtraction application is useful for indicating when one digital word is approaching another in value More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$ V_O will be a bipolar signal defined by the above equation Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input, and drive $R15_1$ and $R15_2$ This yields high input impedance, bipolar differential and common-mode range

FIGURE 28 – DIGITAL SUMMING and CHARACTER GENERATION



$V_O = (I_{O1} + I_{O2})\ R_O$

$$\boxed{V_O = \left[\frac{V_{ref\ 1}}{R14_1}\{A\} + \frac{V_{ref\ 2}}{R14_2}\{B\}\right] R_O}$$

In a character generation system one MC1408 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

FIGURE 29,– POSITIVE PEAK DETECTING SAMPLE and HOLD (Features indefinite hold time and optional digital output.)

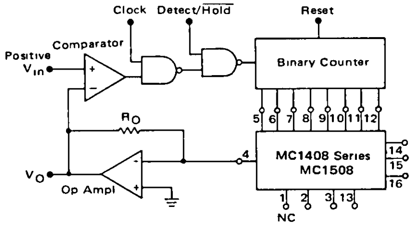
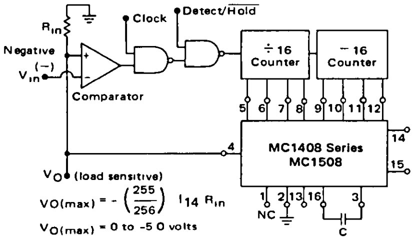


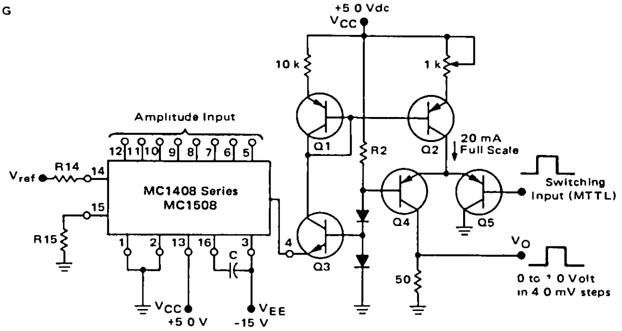
FIGURE 30 – NEGATIVE PEAK DETECTING SAMPLE AND HOLD



$V_{O(max)} = -\left(\frac{255}{256}\right) I_{14}\ R_{in}$

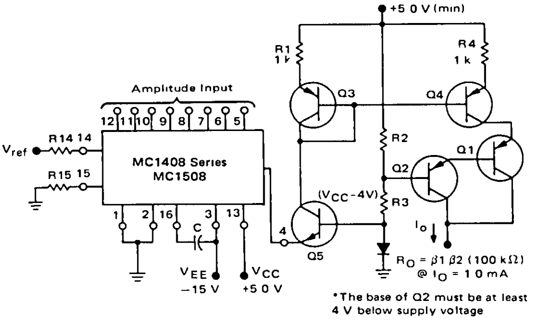
$V_{O(max)} = 0$ to -5.0 volts

FIGURE 31 – PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high-speed switching transistors for the differential pair, Q4 and Q5 Linear ramps and sine waves may be generated by the appropriate reference input

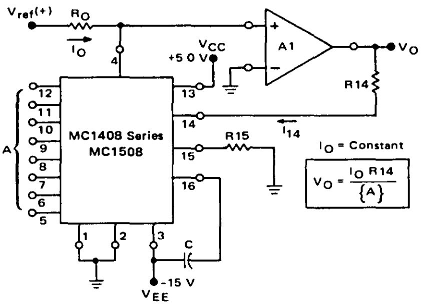
FIGURE 32 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs This circuit is especially useful in curve tracer applications.

APPLICATIONS INFORMATION (continued)

FIGURE 33 – ANALOG DIVISION BY DIGITAL WORD



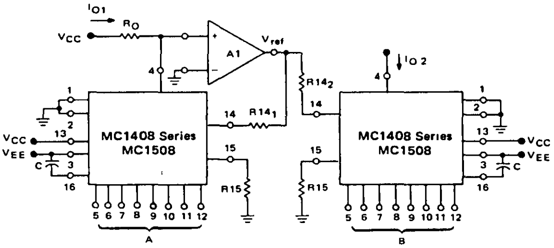
I_O = Constant

$$\boxed{V_O = \frac{I_O\, R14}{\{A\}}}$$

This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1733, MC1520 or any other wideband amplifier are used, the reference amplifier should always be overcompensated.

FIGURE 34 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



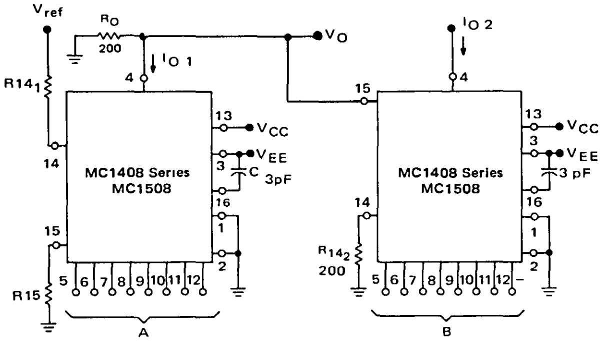
$$V_{ref} = \frac{I_{O1}\, R14_1}{\{A\}}$$

$$I_{O2} = \frac{V_{ref}}{R14_2}\,\{B\}$$

if $R14_1 = R14_2$

$$\boxed{I_{O2} = I_{O1}\,\frac{\{B\}}{\{A\}}}$$

FIGURE 35 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = -I_{O1}\, R_O = \frac{V_{ref}}{R14_1}\, \{A\}\, R_O$$

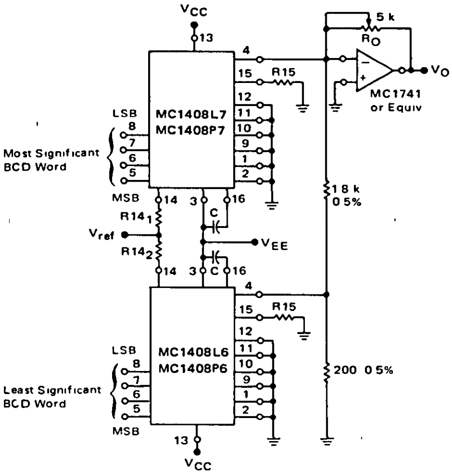
$$I_{O2} = \frac{\{B\}\, |V_O|}{R14_2} = \frac{\{B\}}{R14_2}\left[R_O \left(\frac{V_{ref}}{R14_1}\right) \{A\}\right]$$

Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$\boxed{I_{O2} = K\, \{A\}\, \{B\}}$ K can be an analog variable

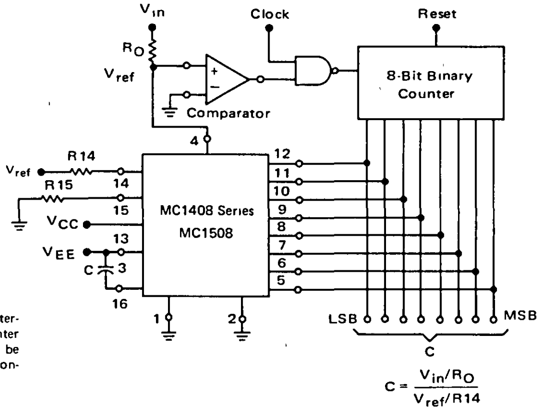
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10 1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0 4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion

MOTOROLA

MC3408

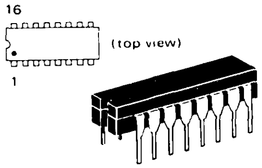
LOW-COST EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Relative Accuracy: ±0.5% Error Maximum
- Low Price Allows Use of a D/A in Many New Applications
- Monotonicity Guaranteed to 8 Bits
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input Slew Rate 4.0 mA/μs
- Standard Supply Voltages +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

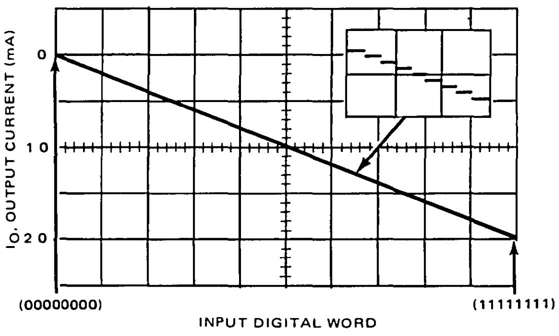
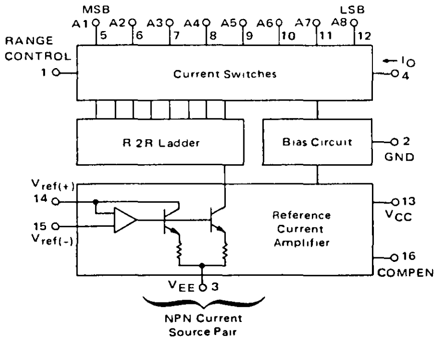


FIGURE 2 — BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7 0 -16 5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +15	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C

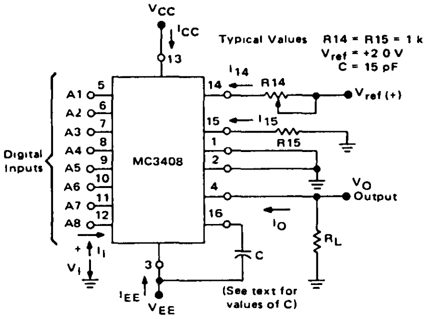
ELECTRICAL CHARACTERISTICS (V_{CC} = +5 0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, T_A = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) Note 1	4	E_r	–	–	±0.5	%
Monotonicity See Multiplying Accuracy on Page 6	–	–	Guaranteed to 8 bits			–
Settling Time to within ±0.5% of Full Scale [includes t_{PLH}] (T_A=+25°C)See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH}, t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	-30	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2 0 –	 – –	 – 0 8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0 8 V	3	 I_{IH} I_{IL}	 – –	 0 -0 4	 0 04 -0 8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	µA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V (T_A = 25°C)	3	I_{OR}	 0 0	 2 0 2.0	 2.1 4 2	mA
Output Current V_{ref} = 2 000 V, R14 = 1000 Ω	3	I_O	 1 9	 1.99	 2 1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4 0	µA
Output Voltage Compliance ($E_r \leq$ 0 5% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0 5, +0 4 -5 0, +0 4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4 0	–	mA/µs
Output Current Power Supply Sensitivity		PSRR(–)	–	0 5	4 0	µA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13 5 -7 5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4 5 -4.5	+5 0 -15	+5 5 -16.5	Vdc
Power Consumption All bits low V_{EE} = -5 0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_C	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. For devices with greater accuracy, see MC1508 Series data sheet.
Note 2. All bits switched

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

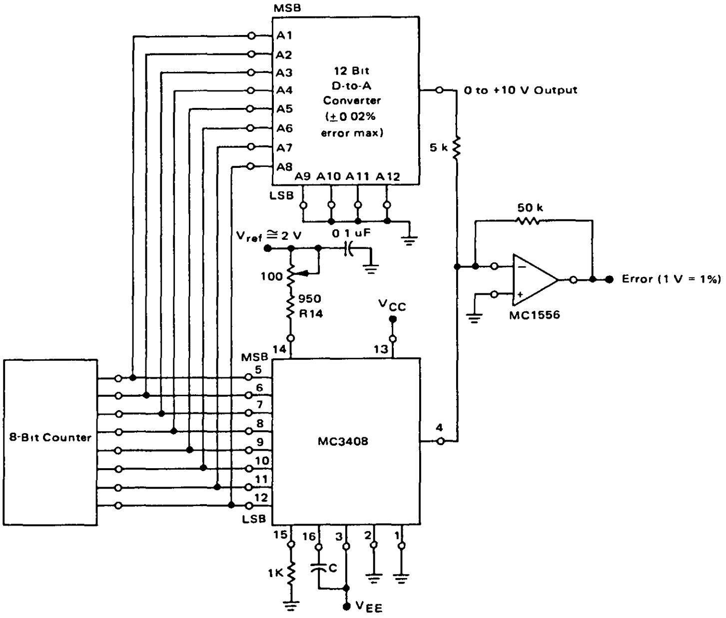
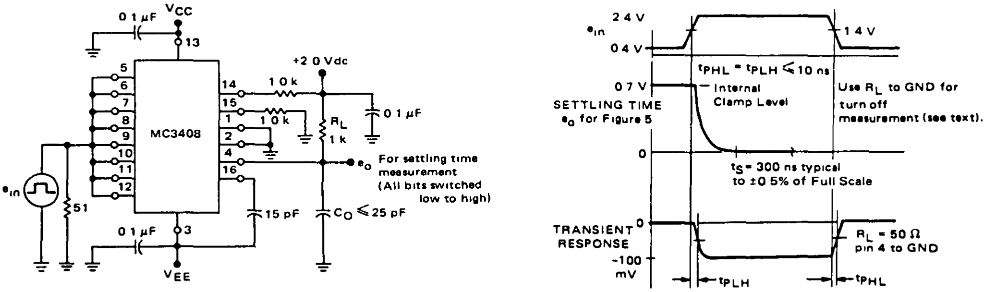


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 — REFERENCE CURRENT SLEW RATE MEASUREMENT

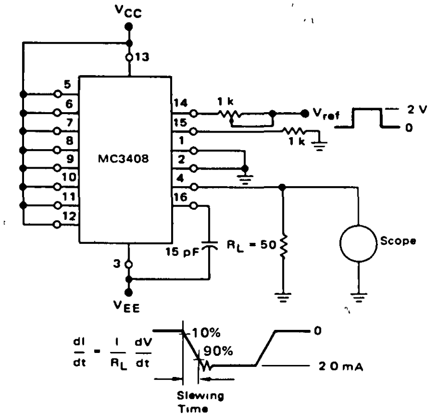


FIGURE 7 — POSITIVE V_{ref}

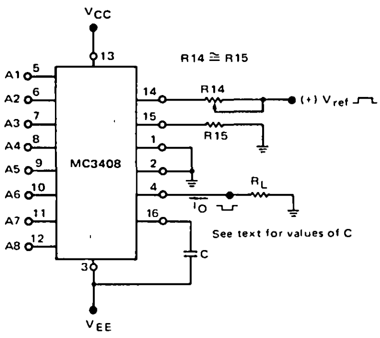


FIGURE 8 — NEGATIVE V_{ref}

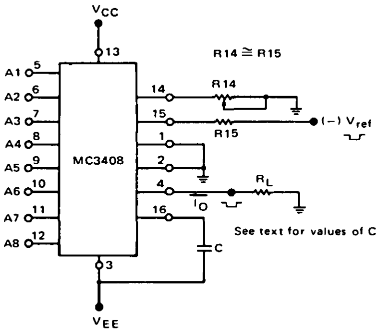
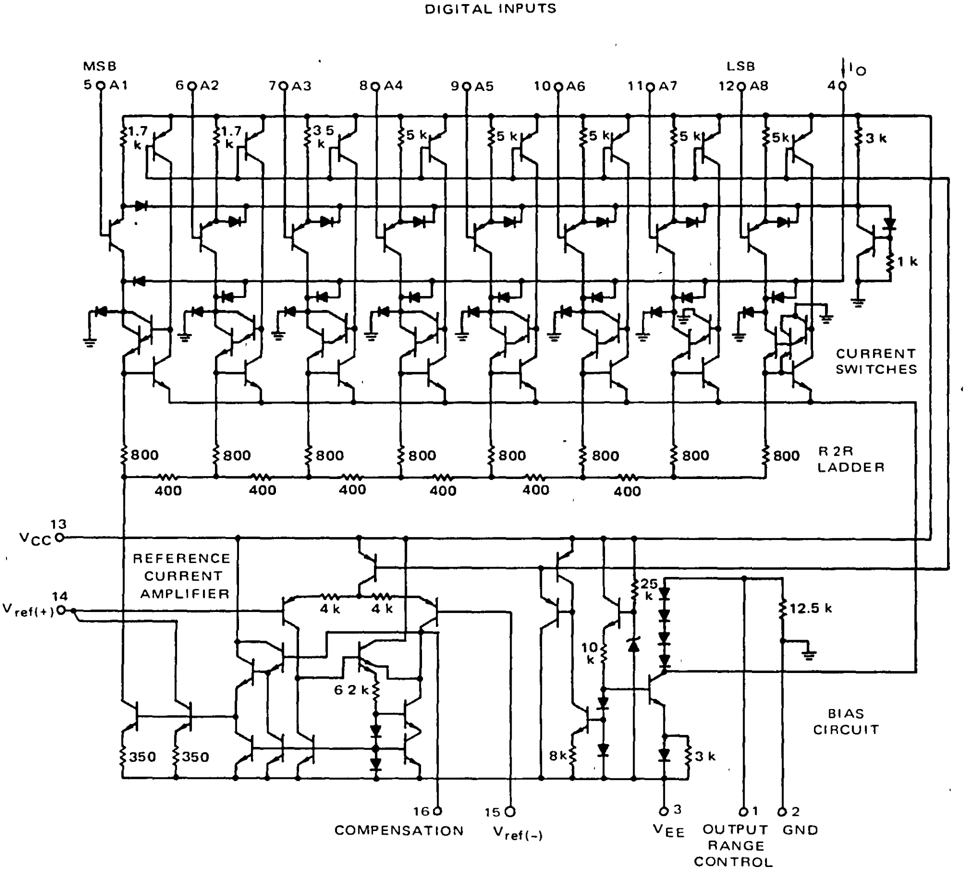


FIGURE 9 – MC3408 EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC3408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches For many applications, only a reference resistor and reference voltage need be added

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches Note that there is always a remainder current which is equal to the least significant bit This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1 992 mA for a 2 0 mA reference amplifier current if the NPN current source pair is perfectly matched

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin, for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 µF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.5 to +0.4 volts at +25°C, due to the current switching methods employed in the MC3408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC3408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 µs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC3408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC3408 has a very low full scale current drift with temperature

The MC3408 is guaranteed accurate to within ±0.5% at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 µA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC3408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC3408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.5% specification provided by the MC3408.

Multiplying Accuracy

The MC3408 may be used in the multiplying mode with good accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 µA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 µA to 2.0 mA, the 1.6 µA contributes an error of 0.2 LSB with respect to the 2.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC3408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 2.0 mA.

MOTOROLA

MC3410
MC3510 MC3410C

LASER TRIMMED

TEN BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

Specifications and Applications Information

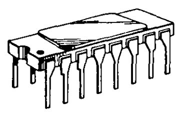
TEN BIT D TO A CONVERTER

The MC3410 series devices are low-cost, high-accuracy monolithic D/A converter subsystems. Like their MC1408 series predecessors, they provide the logic controlled current switches, the R-2R resistor ladder network and output termination networks. The output buffer amplifier and reference voltage have been omitted from the circuit to allow greatest system speed, flexibility and lowest cost. This device is useful in industrial control and microprocessor based systems.

- Relative Accuracy – ±0.05% Error Maximum (MC3510 and MC3410)
- Fast Settling Time – 250 ns Typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible (from 5 to 15 V CMOS)
- Output Voltage Swing – +0.2 V to −2.5 V
- High Speed Multiplying Input Slew Rate – 20 mA/μs
- Standard Supply Voltages – +5 V and – 15 V
- All Categories Guaranteed Monotonic Across Temperature
- Reference Amplifier Internally Compensated

TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 3-Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Speech Compression and Expansion
- Sample Data Systems



L SUFFIX
CASE 690
(CERAMIC PACKAGE)

PIN CONNECTIONS

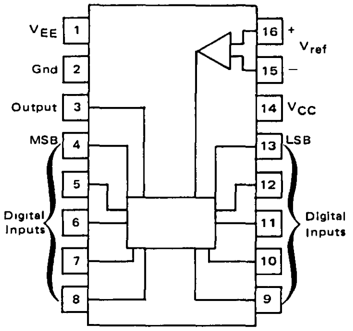


FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

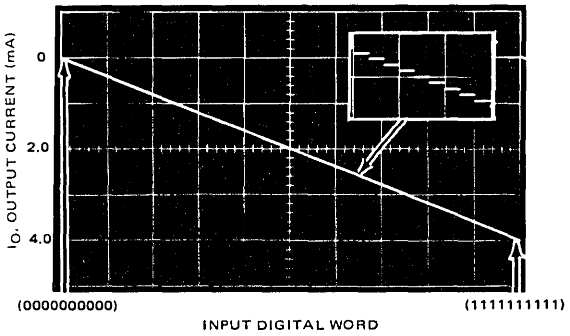
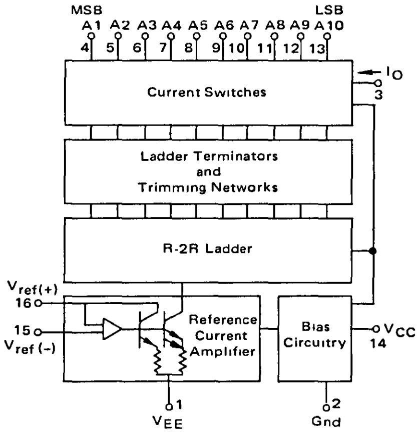


FIGURE 2 – TEN-BIT D/A CONVERTER BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −18	Vdc
Digital Input Voltage	V_I	+15	Vdc
Applied Output Voltage	V_O	+0.5, -5 0	Vdc
Reference Current	$I_{REF(16)}$	2.5	mA
Reference Amplifier Inputs	V_{REF}	V_{CC}, V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{REF(D)}$	0.7	Vdc
Operating Temperature Range	T_A		°C
MC3510		−55 to +125	
MC3410,C		0 to +70	
Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R16}$ = 2.0 mA, MC3510 T_A = −55°C to +125°C. MC3410 Series: T_A = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) T_A = 25°C	E_r				%
MC3510, MC3410		–	–	±0.05	
MC3410C		–	–	±0.1	
Relative Accuracy Temperature Drift (Relative to Full Scale I_O)	TCE_r	–	2.5	–	PPM/°C
Monotonicity (Full Temperature Range)	–	Monotonic to 10 Bits			–
Settling Time to within ±1/2 LSB (T_A = 25°C) (All Bits Low to High)	t_S	–	250	–	ns
Propagation Delay Time	t_{PLH}	–	35	–	ns
T_A = +25°C	t_{PHL}	–	20	–	
Output Full Scale Current Drift MC3410, MC3410C	TCI_O	–	–	60	PPM/°C
MC3510		–	–	70	
Digital Input Logic Levels (All Bits)					Vdc
High Level, Logic "1"	V_{IH}	2.0	–	–	
Low Level, Logic "0"	V_{IL}	–	–	0.8	
Digital Input Current (All Bits)					mA
High Level, V_{IH} = 5.5V	I_{IH}	–	–	0.04	
Low Level, V_{IL} = 0.8V	I_{IL}	–	0.05	0.4	
Reference Input Bias Current (Pin 15)	$I_{REF(15)}$	–	−1.0	−5.0	µA
Output Current Range	I_{OR}	0	4.0	5.0	mA
Output Current	I_O				mA
V_{ref} = 2.000 V, R_{16} = 1000 Ω		3.8	3.996	4.2	
Output Current MC3510, MC3410	$I_{O(min)}$	–	0	2.0	µA
(All bits low) (T_A = 25°C) MC3410C		–	0	4.0	
Output Voltage Compliance (T_A 25°C)	V_O				Vdc
E_r < 0.05% relative to FS – MC3510, MC3410		–	–	-2.5,+0.2	
E_r < 0.10% relative to FS – MC3410C				-2.5,+0.2	
Reference Amplifier Slew Rate	$SR\ I_{ref}$	–	20	–	mA/µs
Reference Amplifier Settling Time (0 to 4.0 mA, ±0.1%)	STI_{REF}	–	2.0	–	µs
Output Current Power Supply Sensitivity MC3510, MC3410	PSRR(–)	–	0.003	0.01	%/%
MC3410C		–	0.003	0.02	
Output Capacitance (V_O = 0)	C_O	–	25	–	pF
Digital Input Capacitance (All Bits, Inputs High)	C_I	–	4.0	–	pF
Power Supply Current	I_{CC}	–	+10	+18	mA
(All Bits low)	I_{EE}	–	−11.4	−20	
Power Supply Voltage Range	V_{CCR}	+4.75	+5.0	+5.25	Vdc
(T_A = +25°C)	V_{EER}	-14.25	−15	−15.75	
Power Consumption	P_C				mW
All Bits low		–	220	380	
All Bits high		–	200	–	

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUITS

V_I and I_I apply to inputs A1 thru A10

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024} \right)$$

where $K \cong \frac{2 V_{ref}}{R16}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Typical Values:
R15 = R16 = 1 k
V_{ref} (+) = +2.0 V
V_{ref} (–) = Gnd
I_O = 4.0 mA

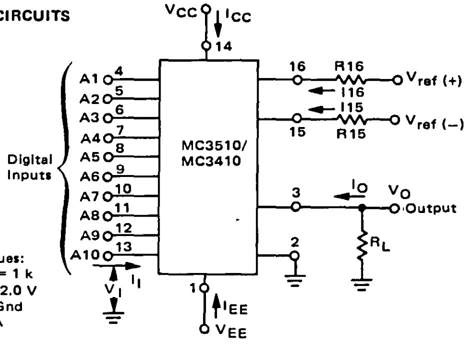


FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

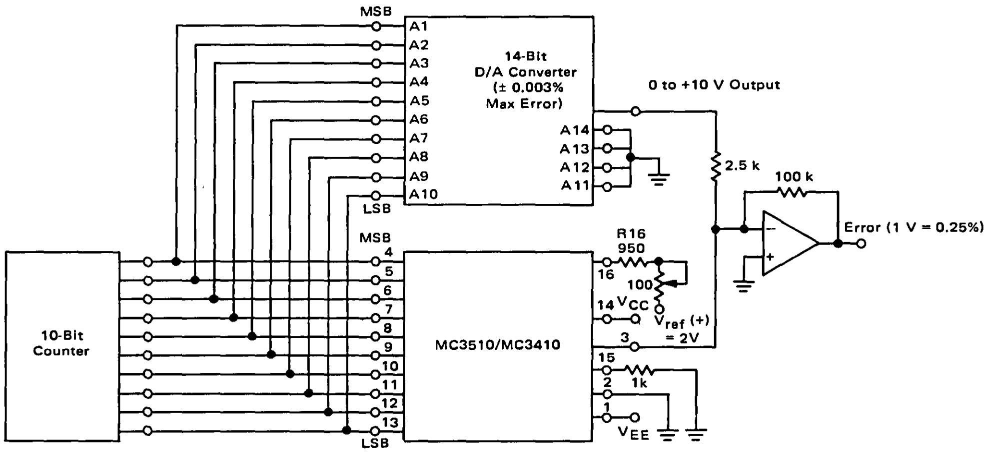
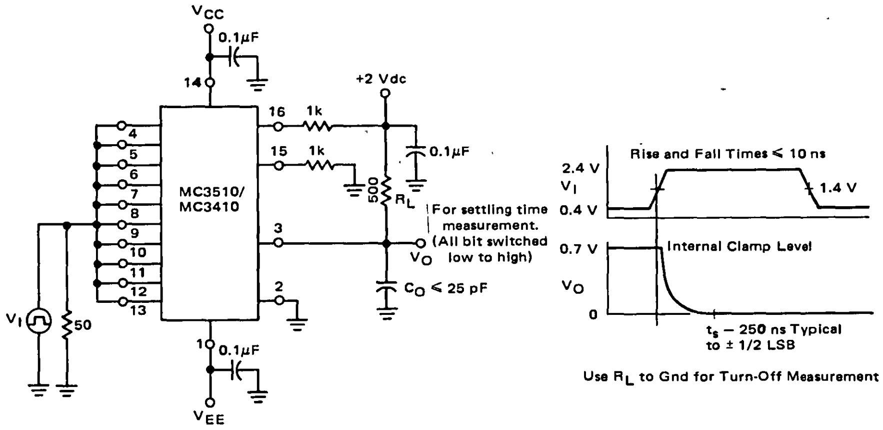


FIGURE 5 – SETTLING TIME



Use R_L to Gnd for Turn-Off Measurement

TEST CIRCUITS (Continued)

FIGURE 6 – PROPAGATION DELAY TIME

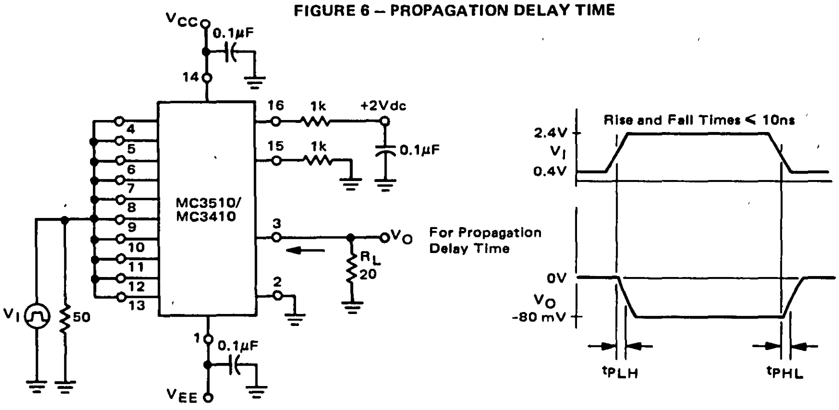
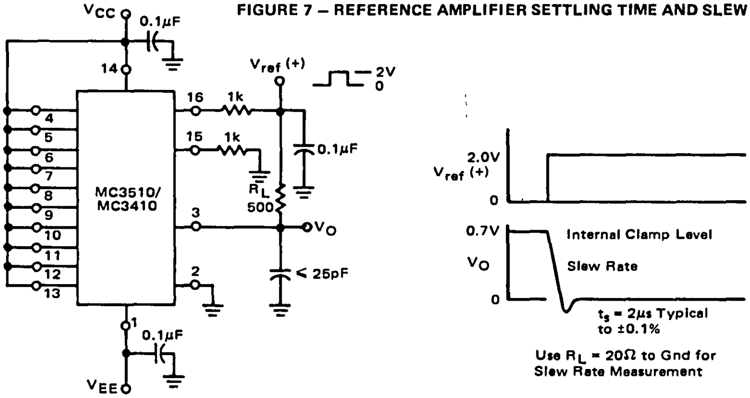
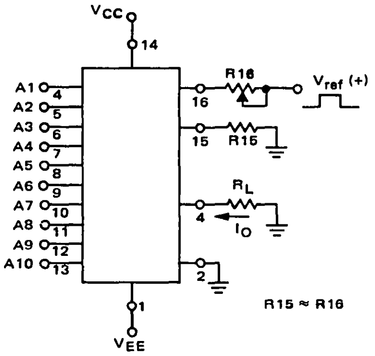


FIGURE 7 – REFERENCE AMPLIFIER SETTLING TIME AND SLEW RATE



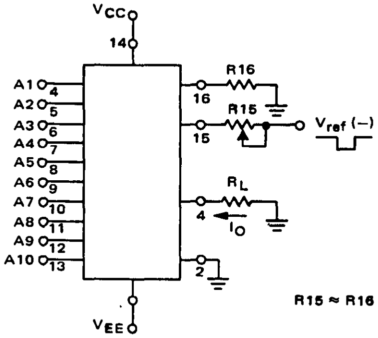
Use RL = 20Ω to Gnd for Slew Rate Measurement

FIGURE 8 – POSITIVE V_{ref}



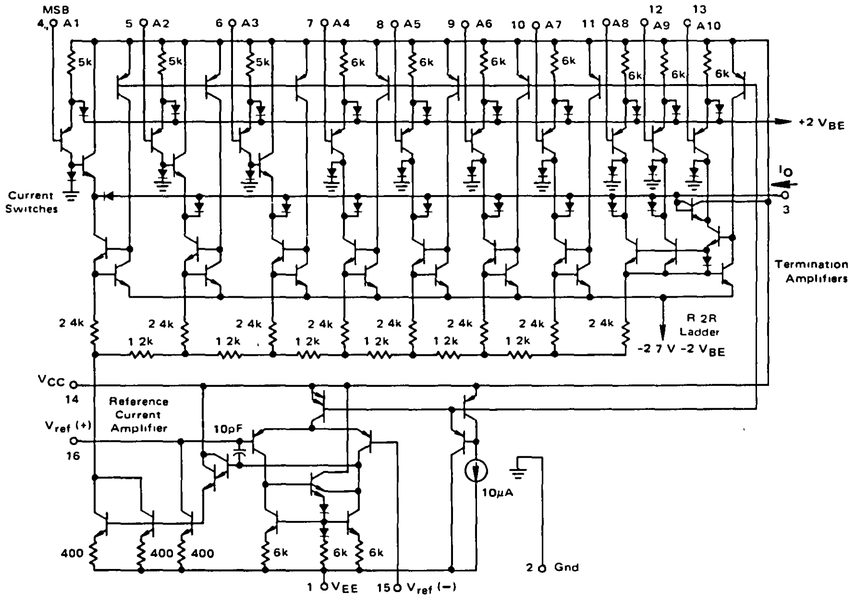
R15 ≈ R16

FIGURE 9 – NEGATIVE V_{ref}



R15 ≈ R16

FIGURE 10 — MC3410 10-BIT D/A CONVERTER EQUIVALENT CIRCUIT



CIRCUIT DESCRIPTION

The MC3410 consists of a reference current amplifier, a diffused R-2R ladder, a laser trimming network, and ten high-speed current switches. The trimming method employed makes it possible to improve the linearity attainable with modern diffusion technology by as much as a factor of ten so that a highly linear part results. The trim is performed by cutting aluminum links arranged to give incremental variations in voltage at the ladder termination amplifiers (See Figure 10). This yields a highly stable trim with no increase in fabrication complexity.

The switches are non-inverting in operation, so that a high state on an input turns on the specific component of output current. The switches use current steering for speed, and interface the R-2R ladder through unity gain feedback termination amplifiers, which provide low impedance terminations of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the current switches. The three least-significant bit switches derive their current through emitter scaling from the last leg of the ladder. The remaining current, equal to one LSB, is shunted to V_{CC} at the LSB switch. Therefore, the maximum output current is 1023/1024 of the reference amplifier current, or nominally 3.996 mA for a 2.000 mA reference input current.

Reference Voltage

To generate the precision voltage reference input for the MC3410, either the MC1403 or the MC1404 may be used. The MC1403 produces a 2.5 V ±1% output voltage while the MC1404 produces a 10 V ±1% output. Both have excellent temperature and long term stability. In order to reduce the effect of reference amplifier offset voltage on overall accuracy, the highest possible stability reference voltage should be used. Therefore, in systems with a +15 V supply, the MC1404 (10 V) is recommended. Where the most positive supply is only +5 V, the MC1403 provides a 2.5 V reference. To set the reference current exactly, a low temperature coefficient potentiometer in series with R1 should be used.

GENERAL INFORMATION

Reference Amplifier

The reference amplifier allows the user to provide a voltage and a resistor to Pin 16 to convert the reference voltage to a current. A current mirror doubles this reference current and feeds it to the R-2R ladder. Thus for a reference voltage of 2.0 Volts and 1 kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0 mA. The reference input current, I16, must flow into Pin 16 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 8. The reference voltage source supplies the full current I16. For bipolar refererence signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level.

The reference amplifier is internally compensated with a 10 pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0 mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0 mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0 MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0 kΩ, and settling time is ≈ 10 μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5 mA for stability.

A negative reference voltage may be used if R16 is grounded and the reference voltage is applied to R15 as shown in Figure 9. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3 Volts above the V_{EE} supply for proper operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0 V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1 μF capacitor to ground.

Output Voltage Range

The voltage on Pin 3 is restricted to a range of −2.5 V to +0.2 V due to the current switching methods employed in the MC3410. When a current switch is turned off, the positive voltage at the output terminal can turn on the output diode and increase the output current. When a current switch is on, the negative output voltage range is restricted to the point at which the low current device of the termination amplifier Darlington begins to saturate, resulting in a decrease in output current.

The output voltage compliance is guaranteed at 25°C. Note from Figure 14 that the output compliance of the MC3410 is nearly constant over temperature.

Accuracy

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the diffused resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full scale current drift with temperature.

The MC3510 and MC3410 are guaranteed accurate to within ±1/2 LSB at 25°C and at a full scale current of 3 996 mA. Input reference current to Pin 16 is guaranteed to be between 1.9 and 2.1 mA to produce a full scale output current of 3.996 mA. The relative accuracy test circuit is shown in Figure 4. The 14 bit D/A converter is calibrated for a full scale output of 3.996 mA. This is an optional step as the relative accuracy of the MC3410 is nearly constant between 3 mA and 5 mA full scale current. The MC3410 is calibrated at full scale with the 14-bit reference D/A by adjusting R16 until the error voltage goes to zero. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored on a peak detector.

Monotonicity

The MC3510, MC3410 and MC3410C are all guaranteed to be monotonic at temperature. This guarantees that for every increase in the input digital word, the output current either remains the same or increases, but never decreases. The MC3510 and MC3410 are monotonic over their respective temperature ranges. In the multiplying mode (when the reference current is varied), monotonicity is typically maintained for all values of input reference current above 0.5 mA.

Settling Time

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200 ns for 8-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (< 0.7 Volt) swing and the external output capacitance is under 25 pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

The slowest switches are bit A10 (LSB) and bit A9, which turn on and settle in typically 200 ns, and turn off in 100 ns.

In the test circuit of Figure 5, the output voltage is internally clamped in the MC3410 at about 0.7 Volts above ground. The output is thus limited to a 0.7 Volt swing. If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5 μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

MC3510 TERMINOLOGY

RELATIVE ACCURACY – Maximum output deviation from the straight line connecting zero and full scale, expressed as a percentage of full scale.

RELATIVE ACCURACY DRIFT – The average change in linearity error that will occur with a change in ambient temperature, expressed in parts per million of full scale per degree C.

MONOTONICITY – For every increase in the input digital word, the output current either remains the same or increases

SETTLING TIME – The elapsed time from the input transition until the output has settled within an error band about its final value.

OUTPUT FULL SCALE CURRENT DRIFT – The average change in full scale current between 25°C and either temperature extreme, expressed in parts per million of full scale per degree C.

REFERENCE AMPLIFIER SLEW RATE – The maximum rate of change of the full scale output current expressed in milliamperes per microsecond.

OUTPUT VOLTAGE COMPLIANCE – The maximum voltage that can be applied to the output pin so that the specified change in output current is not exceeded.

POWER SUPPLY SENSITIVITY – The change in full scale current caused by a change in V_{EE}, expressed as a percent of full scale current per percent change in V_{EE}.

TYPICAL CHARACTERISTICS

FIGURE 11 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

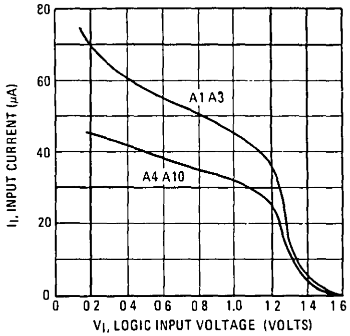


FIGURE 12 – TRANSFER CHARACTERISTIC versus TEMPERATURE

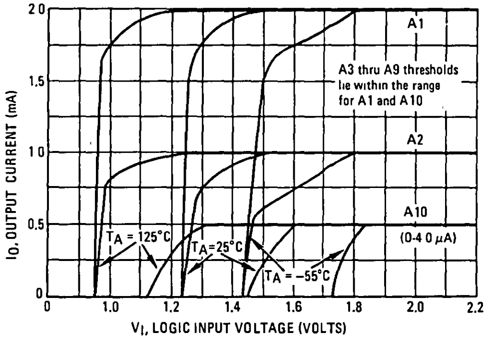


FIGURE 13 – OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Compliance)

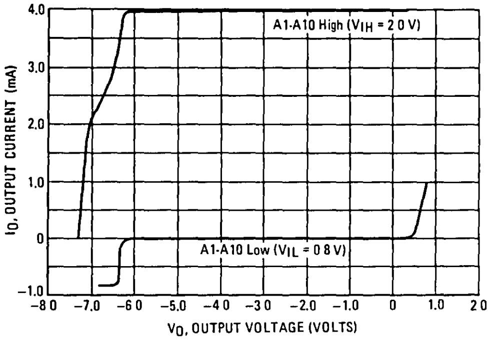


FIGURE 14 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

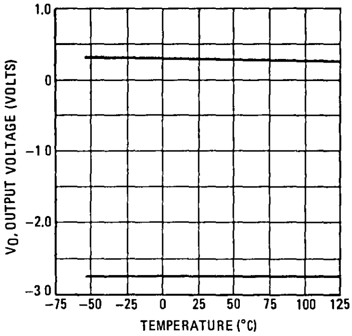


FIGURE 15 – REFERENCE AMPLIFIER FREQUENCY RESPONSE

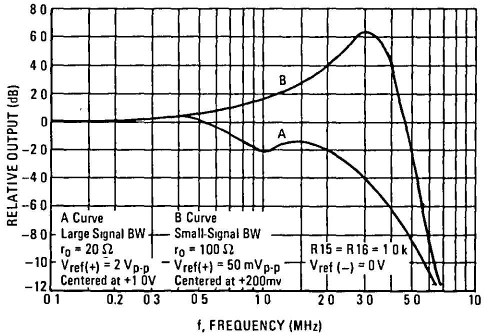
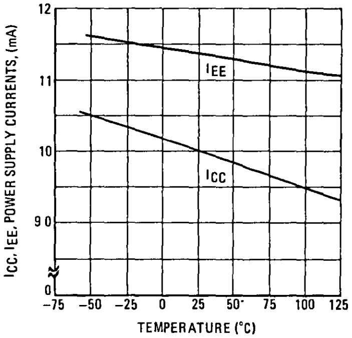


FIGURE 16 – TYPICAL POWER SUPPLY CURRENTS versus TEMPERATURE



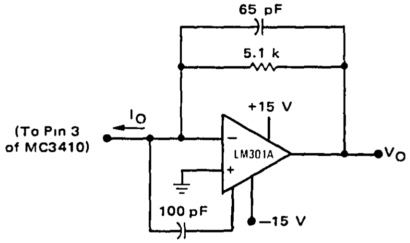
APPLICATIONS INFORMATION

Voltage outputs are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC3410 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

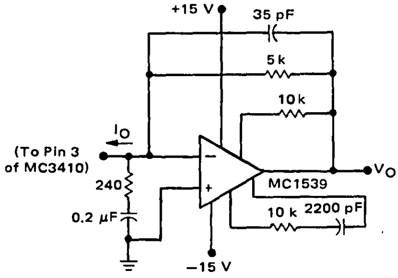
The following circuit shows how the LM301A can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 17



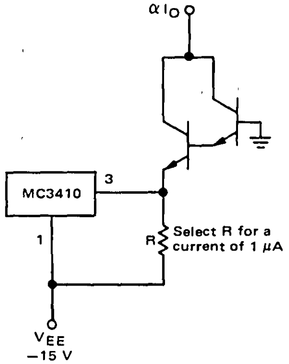
An alternative method is to use the MC1539 and input compensation. Response of this circuit is also on the order of 2.0 µs.

FIGURE 18



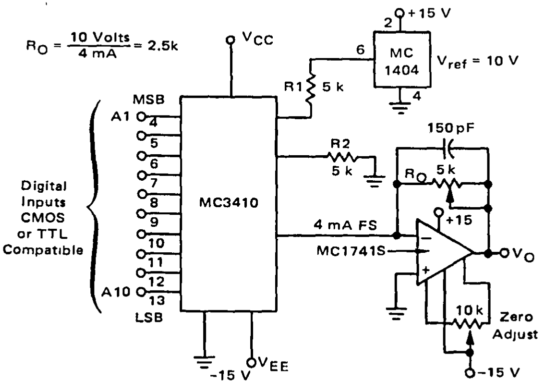
The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 19 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because Pin 3 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

FIGURE 20 – OUTPUT CURRENT TO VOLTAGE CONVERSION



$$R_O = \frac{10\text{ Volts}}{4\text{ mA}} = 2.5k$$

$$V_O = \frac{2R_O}{R_1} V_{ref}\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}+\frac{A9}{512}+\frac{A10}{1024}\right]$$

for 10 volt fullscale calibration

$$V_O = \frac{2(2.5\text{ k})}{5.0\text{ k}} 10\text{ Volts}\left[\frac{1023}{1024}\right] \qquad V_O = 10\text{ Volts }[0.9990]$$

R_O = Full Scale Adjust

APPLICATIONS INFORMATION (Continued)

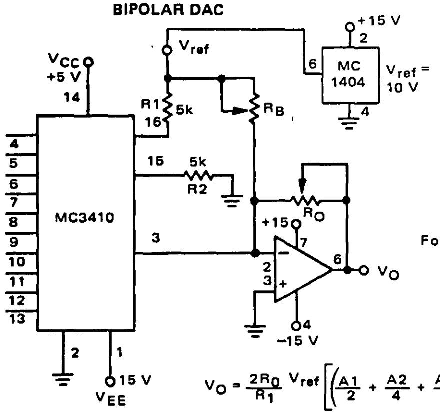
Bipolar or Negative Output Voltage

The circuit in Figure 21 is a variation of the standard output voltage circuit in Figure 20. A negative or offset binary output may be obtained by sourcing current from the reference into the output through R_B. If R_B allows 2 mA (R_B = 5 kΩ from 10 Volts) then 1000000000 input will generate zero output voltage.

Successive Approximation A to D

The fastest and most efficient means of A to D conversion using D to A convertors is successive approximation (SA). Similar in appearance to staircase devices, the SA converter is capable of 100 times faster conversions for a 10-bit result. A complete 10-bit SA coverter using MC3410 and MC14559B/49B successive approximation registers is shown in Figure 22. The complexity which results in higher conversion speeds is contained in the MC14559B/49B registers. Quite simply, the register compares the DAC output resulting from activating each bit with the input voltage. This is done starting with most significant bit and after 10 comparisons generates the 10-bit binary output representing that input. The accuracy of the conversion is fixed by the accuracy of the MC3410 and is not dependent on tolerances of the other components. An EOC outout is available and can be used to latch the parallel output or to synchronize the serial output which is also available. For more details on SA converters, see AN-716.

FIGURE 21 – OFFSET BINARY OR BIPOLAR DAC



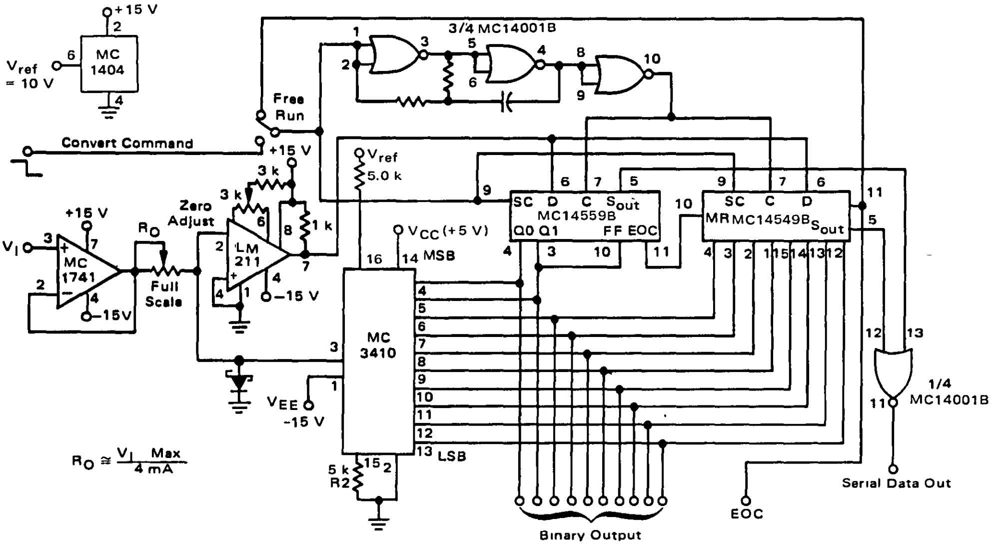
For Offset Binary Output From +5 V to –5 V

$R_O \cong 2.5$ kΩ

$R_B \cong 5$ kΩ

$$V_O = \frac{2R_O}{R_1} V_{ref}\left[\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}\right) - \frac{2R_I}{R_B}\right]$$

FIGURE 22 – SUCCESSIVE APPROXIMATION CONVERTER USING MC3410 AND MC1404



$R_O \cong \frac{V_I \text{ Max}}{4 \text{ mA}}$

APPLICATIONS INFORMATION (Continued)

Staircase A to D

If high conversion speed is not required, a staircase A to D convertor can be built for somewhat lower cost. A complete staircase A/D convertor is shown in Figure 23. Here the complicated SA registers are replaced with simple binary counters. With an input voltage applied, the binary counter is reset by the convert command pulse and the begin accumulating counts. The DAC output steps upward until the comparator detects that the input is equal to the DAC output. The counters are disabled and the conversion result is held at the output until the circuit is reset by the convert command input.

One advantage of staircase convertors is the ease with which BCD outputs may be obtained Figure 24 shows a 3-digit panel meter using the staircase technique and an MC14553B 3-decade counter. The circuit function is similar to Figure 23 but Multiplexed BCD output is available from the MC14553B counters. Parallel BCD may be obtained with equal ease using the MC14518B 2-decade CMOS counters.

In both these staircase designs the system accuracy is determined by the specified accuracy of the MC3410.

FIGURE 23 – 10-BIT STAIRCASE A to D USING MC3410 AND MC1403

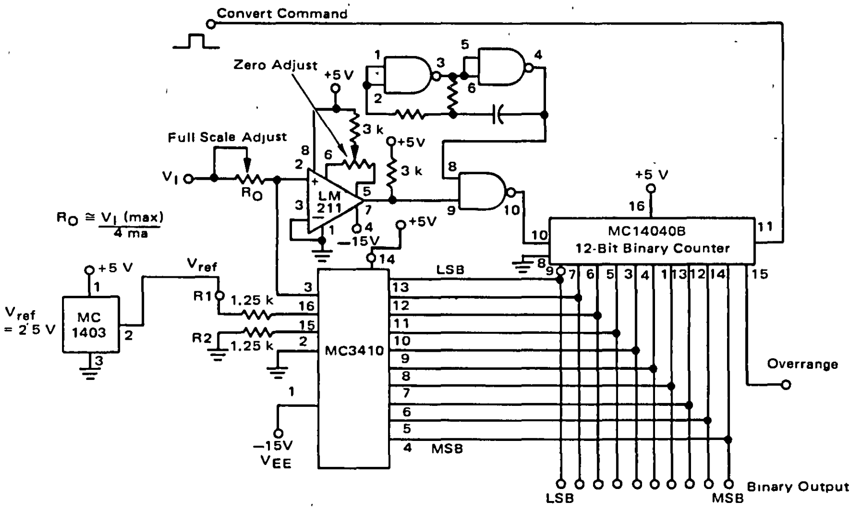
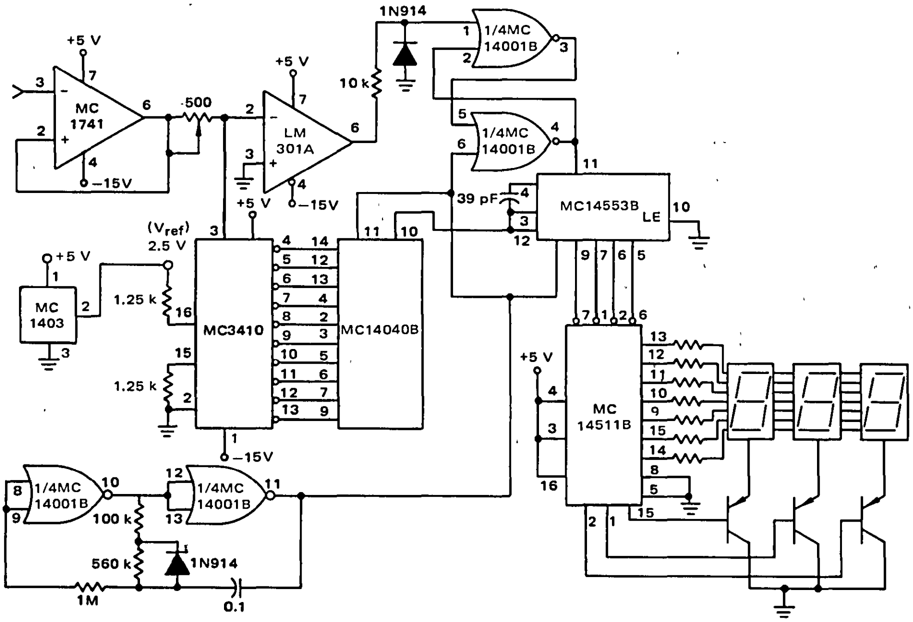
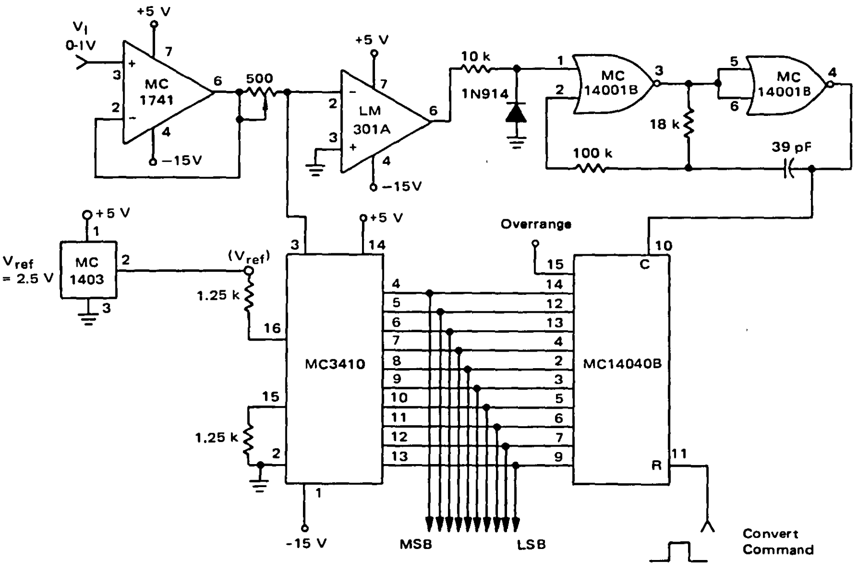


FIGURE 24 – 3-DIGIT DVM USING MC3410 AND MC1403



APPLICATIONS INFORMATION (Continued)

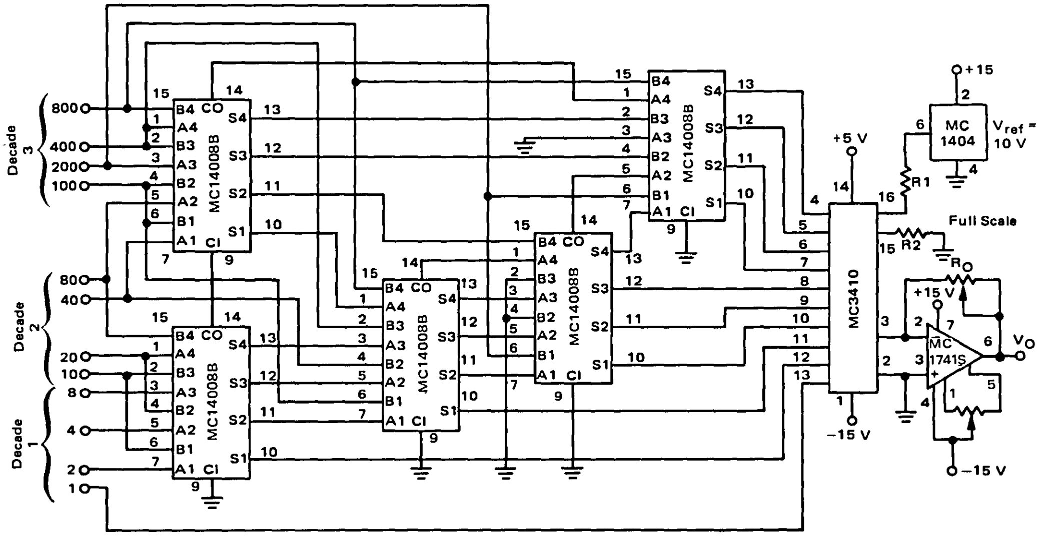
FIGURE 25 – ALTERNATE APPROACH STAIRCASE A TO D



BCD D to A Converter

BCD output A to D conversions are most easily accomplished by accumulating the digital results in two different counters, but that concept does not extend to BCD Dto A techniques. Using the circuit in Figure 26 a three-digit BCD number can be converted to a 10-bit accurate voltage. The MC14008B's perform the combinational BCD-to-Binary conversion. The accuracy of this circuit is also solely dependent on the accuracy of the MC3410.

FIGURE 26 – 3-DECADE BCD DAC



MOTOROLA

MC3412

Product Preview

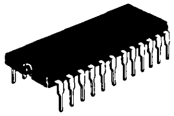
COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

The MC3412 is a monolithic single-chip 12-bit D/A converter. It contains a high-stability voltage reference and both offset and span resistors. Active laser trimming of the thin-film ladder network and voltage reference provide accuracy and linearity of better than ± ½ LSB. 12-bit accuracy and fast settling time (typically better than 200 ns to ± ½ LSB) make this converter an ideal display driver or fast A/D converter building block.

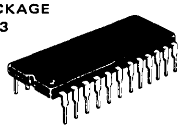
- Fast Settling Time: ± ½ LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- Single-Chip Construction
- High-Stability Voltage Reference on Chip
- Linearity Guaranteed Over Temperature
- Low Power Consumption
- Replaces AD565

HIGH-SPEED 12-BIT D/A CONVERTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

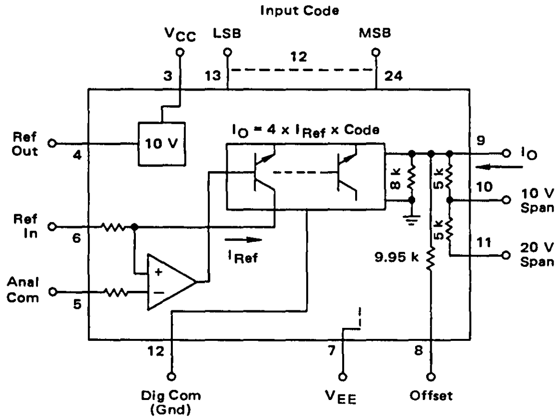


L SUFFIX
CERAMIC PACKAGE
CASE 623

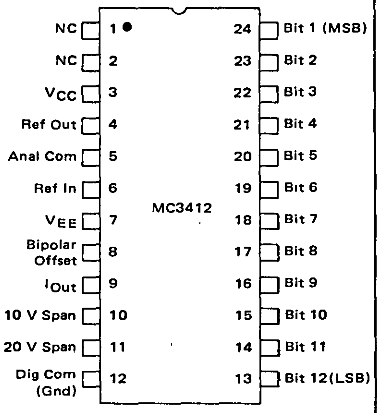


P SUFFIX
PLASTIC PACKAGE
CASE 649

BLOCK DIAGRAM



PIN CONNECTIONS



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MOTOROLA

MC6890

Product Preview

8-BIT BUS-COMPATIBLE MPU DAC

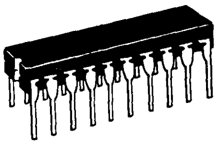
BUS-COMPATIBLE 8-BIT MPU D-TO-A CONVERTER

The MC6890 is a self-contained, bus-compatible, 8-bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high-stability, laser-trimmed, thin-film resistors for both reference input and output span and offset control.

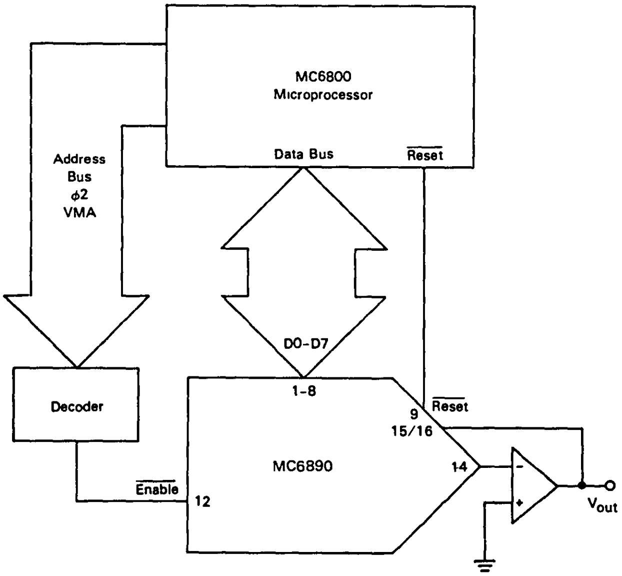
A reset pin provides for overriding stored data and forcing I_{out} to zero.

- ±1/2 LSB Nonlinearity
- Available in Military Temperature Range
- Direct Data Bus Link
- Low Power: 130 mW Typ
- Fast Settling Time: 140 ns Typ
- Single Enable: 10 ns Max Data Hold Time
- Self-Contained 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Reset Pin to Override Data
- Output Voltage Ranges: +5.0, +10, +20, or ±2.5, ±5.0, ±10 Volts

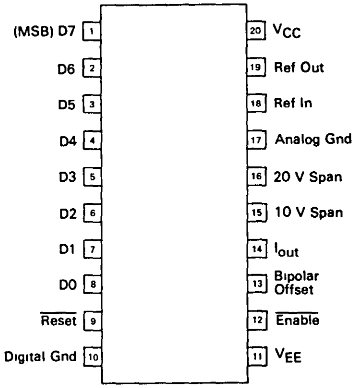


L SUFFIX
CASE 732

OPERATION WITH MC6800



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -18	Vdc
Digital Input Voltage, Pins 1-9, 12	V_{in}	-3.0 to +7.0	Vdc
Applied Output Voltage	V_{out}	V_{EE} to +17	Vdc
Reference Current	I_{ref} (19)	3.5	mA
Reference Amplifier Input	V_{17}	±7.5	Vdc
Operating Temperature Range MC6890 MC6890A	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = − 12 V, V_{ref} = 2.5 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Logic Levels (Each Bit) High Level, Logic 1 Low Level, Logic 0	 V_{IH} V_{IL}	 — 2.0	 — —	 0.8 —	Vdc
Digital Input Current Data (V_{IH} = 3.0 V) (V_{IL} = 0.4 V) $\overline{\text{Enable}}$, $\overline{\text{Reset}}$ (V_{IH} = 3.0 V) (V_{IL} = 0.4 V)	 I_{IH} I_{IL} I_{IH} I_{IL}	 — — — —	 — — — —	 100 -10 100 -50	 nA μA nA μA
Full Scale Output Current — Unipolar	I_O	-1.50	-1.992	-2.50	mA
Output Resistance — Exclusive of Span Resistors	—	7.0	10	—	MΩ
Unipolar Zero Output — All Bits Off	—	—	0.10	1.0	μA
Full Scale Output (Unipolar Zero) Temperature Coefficient (With Internal Reference) Unipolar Zero Bipolar Zero Gain		 — — —	 ± 2.0 ± 35 ± 35	 — — —	ppm/°C
Resolution	—	8 0	8.0	8.0	Bits
Monotonicity (0°C ≤ T_A ≤ +70°C) MC6890 (-55°C ≤ T_A ≤ +125°C) MC6890A		8 Bits Over Temperature			
Relative Accuracy (Error Relative to Full-Scale Output Current)	ϵ_r	—	—	±0.19 (±1/2 LSB)	%
Differential Nonlinearity	—	—	—	± 0.29 (± 3/4 LSB)	%
Output Voltage, Full Scale — Unipolar with Internal Reference (10 V Span) (20 V Span) (5.0 V Span)	V_O	 9.951 19.902 4.976	 9.961 19.922 4 981	 9.971 19.941 4.985	Vdc
Output Voltage, Half Scale — Bipolar Offset Tied to Internal Reference Direct — Input Code = 10000000 (10 V Span) (20 V Span) (5.0 V Span)	V_O	 -9.8 -19.5 4.9	 0 0 0	 9.8 19.5 4.9	mV
Power Supply Range	V_{CC} V_{EE}	4 5 16 5	5.0 -12	5.5 -4 5	Vdc
Power Supply Current (V_{CC} = 5.0 V) (V_{EE} = -5.0 V) (V_{EE} = − 15 V)	 I_{CC} I_{EE} I_{EE}	 — — —	 15 11 12	 — — —	mA
Power Supply Sensitivity To V_{CC} (V_{CC} = 4.5 to 5 5 V, V_{EE} = -5.0 V) To V_{EE} (V_{CC} = 5.0, V_{EE} = -5.0 to -15 V)	PSS	 — —	 ±5.0 ±10	 ±50 ±100	ppm/FS*
Power Dissipation — All Bits Low For V_{CC} = 5.0 V @ V_{EE} = -5.0 V For V_{EE} = − 15 V @ V_{CC} = 5.0 V	P_D	 — —	 130 255	 — —	mW
Reference Input Resistor	R_{ref}	4.0	5.0	6.25	kΩ
Reference Output Voltage I_{Load} = 0 to 3.0 mA	V_{ref}	—	2.500	—	Vdc
Reference Output Current	I_{ref}	—	—	3.0	mA
Reference Output Voltage Temperature Coefficient	TC_{VO}	—	±25	—	ppm/°C

*Full Scale

AC SPECIFICATIONS (V_{CC} = 5.0 V, V_{EE} = −12 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Settling Time ($\overline{\text{Enable}}$ Positive Edge to ±1/2 LSB Output)	t_s	—	140	—	ns
Data Setup Time	$t_{su(D)}$	—	80	—	ns
Data Hold Time	$t_{h(D)}$	-10	—	—	ns
Minimum Pulse Widths $\overline{\text{Enable}}$ $\overline{\text{Reset}}$	 $t_{W(\overline{E})}$ $t_{W(\overline{R})}$	 — —	 50 100	 — —	ns
Propagation Delays $\overline{\text{Enable}}$, Low to High $\overline{\text{Reset}}$, High to Low (I_O < 1.0 μA)	 $t_{PLH(\overline{E})}$ $t_{PHL(\overline{R})}$	 — —	 60 140	 — —	ns

FIGURE 1 — TIMING DIAGRAM

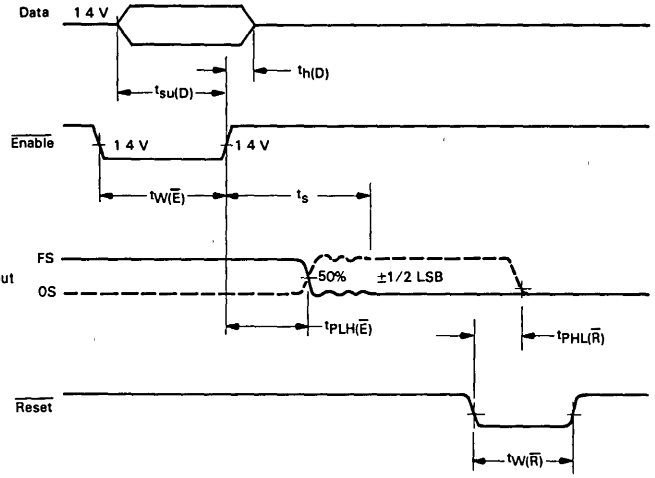


FIGURE 2 — BLOCK DIAGRAM

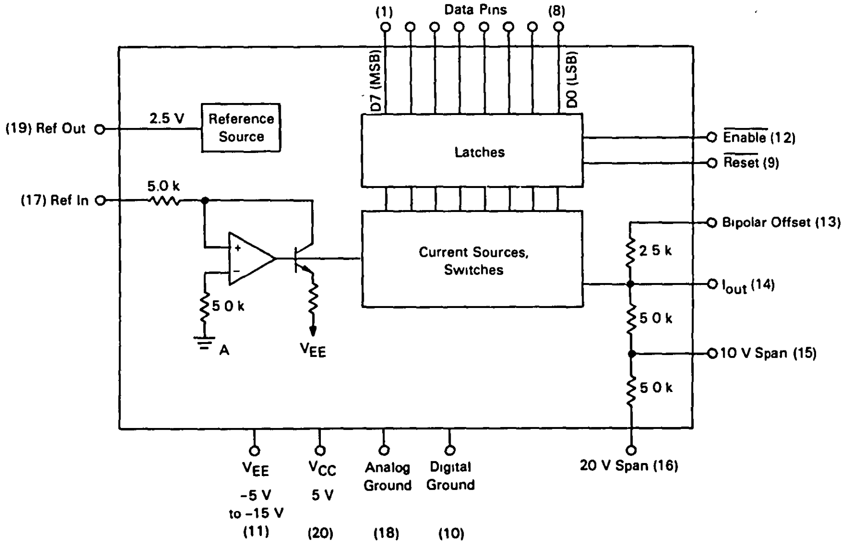
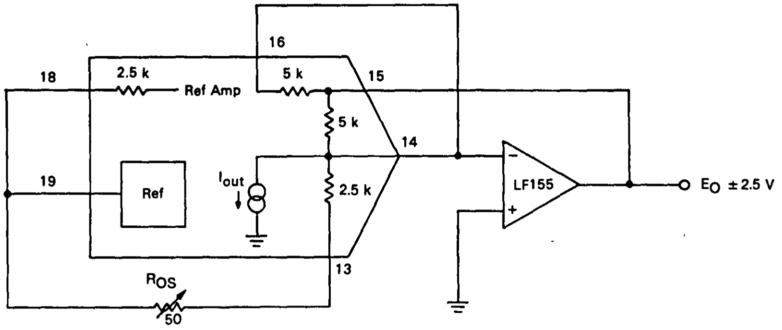
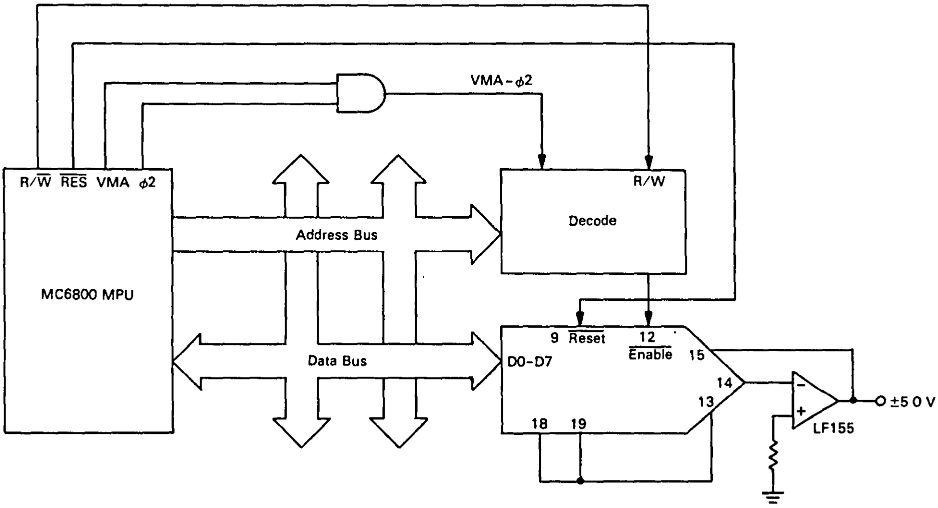


FIGURE 3 — MC6890 IN TYPICAL BIPOLAR ±2.5 V OPERATION



D7	D6	D5	D4	D3	D2	D1	D0	E_O (Volts)	
								$R_{OS} \approx 25\Omega$	$R_{OS} = 0$
1	1	1	1	1	1	1	1	+2.490	+2.480
1	1	1	1	1	1	1	0	+2.470	+2.460
1	0	0	0	0	0	0	0	+0.010	+0.000
0	1	1	1	1	1	1	1	−0.010	−0.020
0	0	0	0	0	0	0	1	−2.470	−2.480
0	0	0	0	0	0	0	0	−2.490	−2.500

FIGURE 4 — TYPICAL APPLICATION FOR OFFSET BINARY ±5.0 V OUTPUT OPERATION



MOTOROLA

MC10317L

Product Preview

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

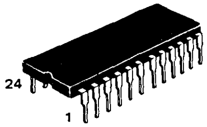
SILICON MONOLITHIC INTEGRATED CIRCUIT

SEVEN BIT PARALLEL HIGH SPEED A/D CONVERTER (WITH OVERRANGE)

The MC10317L is a 7-bit high speed parallel A/D converter which employs ECL processing. The device consists of 128 parallel latched comparators across a high quality input reference network. The 128 comparator outputs are then fed to a 128-to-7 encoder and latched to the outputs which are ECL compatible. An overrange bit is provided to allow overrange sensing, or to facilitate the connection of two 7-bit converters to produce an 8-bit A/D converter.

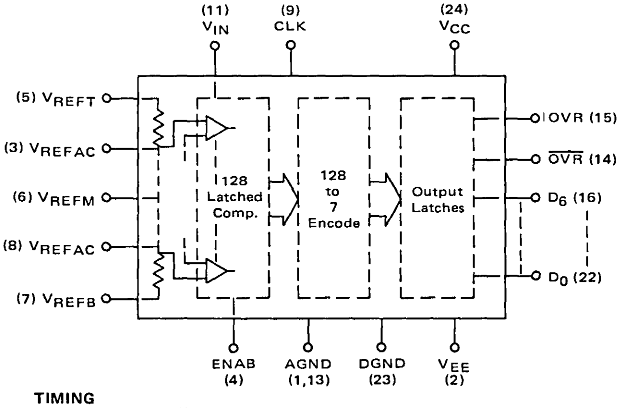
Applications include video display and radar signal processing, high speed instrumentation, and TV broadcast video encoding.

- 7-Bit Resolution/8-Bit Accurate Plus Overrange
- Direct Interconnection for 8-Bit Conversion
- >30 MHz Sampling Rate
- Binary or 2's Compliment Output
- Fully Monolithic - ECL 10K Compatible
- Standard 24-Pin Package
- Wide Range of Input Voltage - ± 2.0 Volts

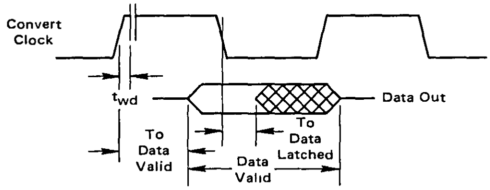


L SUFFIX
CERAMIC PACKAGE
CASE 623

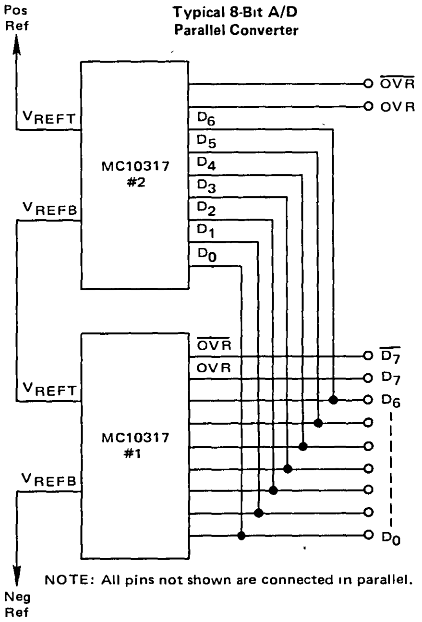
MC10317 DEVICE/APPLICATION CONFIGURATION



TIMING



Typical 8-Bit A/D Parallel Converter



NOTE: All pins not shown are connected in parallel.

This is advance information and specifications are subject to change without notice.

MOTOROLA

MC10318L
MC10318L9

Advance Specifications and Applications Information

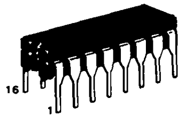
HIGH SPEED
8-BIT DIGITAL-TO-ANALOG CONVERTER

The MC10318 is a high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, display processing, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability 8-bit accurate (±1/2 LSB) and monotonic over the full temperature range, the outputs typically settle in less than 10 ns.

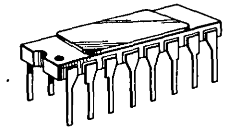
- FAST! Settling Time – 15 ns Typ
- 8-Bit Accuracy (±0.19%) – MC10318L
  9-Bit Accuracy (±0.1%) – MC10318L9
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: –1.3 V to +2.5 V
- Standard: –5.2 V Supply
- Standard 16 Pin Ceramic Package
- Low Dissipation – Typically Less Than 500 mW
- Low Cost

HIGH SPEED
8-BIT DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



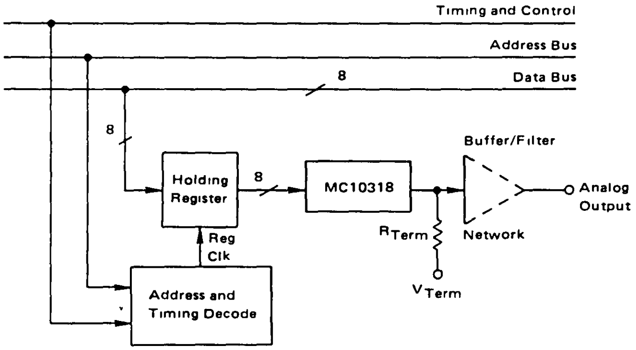
L SUFFIX
CERAMIC PACKAGE
CASE 620



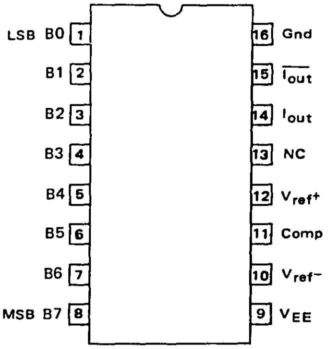
L SUFFIX
CERAMIC PACKAGE
CASE 690

Motorola reserves the right to supply this device in either of the above packages.

TYPICAL MC10318 TO MC10800 PROCESSOR INTERFACE



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	-6.0 to +0.5	Vdc
Digital Input Voltage	V_I	0 to V_{EE}	Vdc
Applied Output Voltage	V_O	+5.0	Vdc
Reference Current	$I_{ref}(12)$	5.0	mA
Output Current	I_{FS}	75	mA
Reference Amplifier Input Range	V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{ref}(D)$	±5.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package	T_J	+175	°C

CHARACTERISTICS

These specifications apply for V_{EE} = -5.2 V, I_{FS} = 51 mA, T_A = 0°C to +70°C after thermal equilibrium is reached.

	TEST VOLTAGE VALUES (Note 1)				
	Volts				
@ Test Temperature	V_{IH}max	V_{IL}min	V_{IHA}min	V_{ILA}max	V_{EE}
0°C	-0.845	-1.868	-1.151	-1.516	-5.2
25°C	-0.810	-1.850	-1.105	-1.505	-5.2
70°C	-0.727	-1.830	-1.052	-1.480	-5.2

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	V_{EE}	-5.46	-5.2	-4.94	V
Power Supply Current (Pins 1 thru 8 Open, I_{FS} = 51 mA)	I_{EE}	–	90	130	mA
Monotonicity	–	8.0	8.0	–	Bits
Nonlinearity MC10318L MC10318L9	– –	– –	– –	±0.19 ±0.10	% FS
Settling Time to 1/2 LSB (All Bits Switched On or Off, T_A = 25°C, Note 3)	t_s	–	15	–	ns
Full Scale Output Temperature Drift	TCI_{FS}	–	±50	±150	ppm/°C
Full Scale Current – Figure 1 (R3, R4 = 3.300 kΩ, V_{ref} = 10.560 V, Note 2)	I_{FS}	46.000	51	56.000	mA
Zero Scale Current (Note 2)	I_{ZS}	–	5.0	50	µA
Full Scale Symmetry (I_{FS15} - I_{FS14}, Note 2)	I_{FSS}	–	15	100	µA
Half Scale Accuracy MC10318L (I_{HS} = 25.5 mA) MC10318L9	HSA	– –	– –	±50 ±25	µA
Output Voltage Compliance (Note 2) Full Scale Current Change ≤ 99 µA MC10318L, 50 µA MC10318L9	V_{OC}	-1.3	–	2.5	V
Power Supply Sensitivity (of Full Scale Current) (V_{EE} = -4.94 V to -5.46 V)	$PSSI_{FS}$	–	±0.002	±0.02	%/%
Reference Bias Current, Pin 10 (I_{ref} = 3.2 mA)	I_{10}	–	6.0	15	µA
Propagation Delay 50% to 50% (All Bits Switched Low to High, High to Low)	tp	–	3.0	–	ns

NOTES. 1. Logic input levels are compatible with MECL 10,000 logic series.

2. Output characteristics apply to both pins 14 and 15, I_{out} and $\overline{I_{out}}$.

3. See comments on construction and evaluation techniques in Figure 2 and text.

FIGURE 1 – FULL SCALE AND HALF SCALE CURRENT TEST CIRCUIT

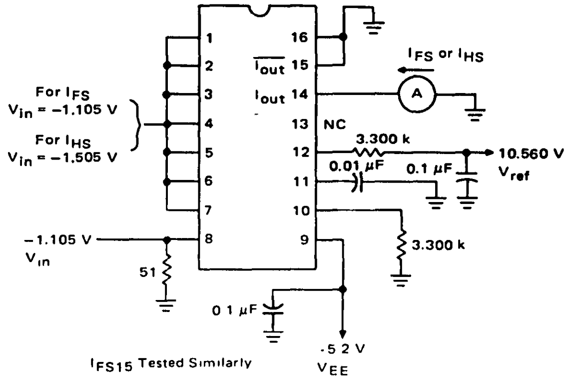
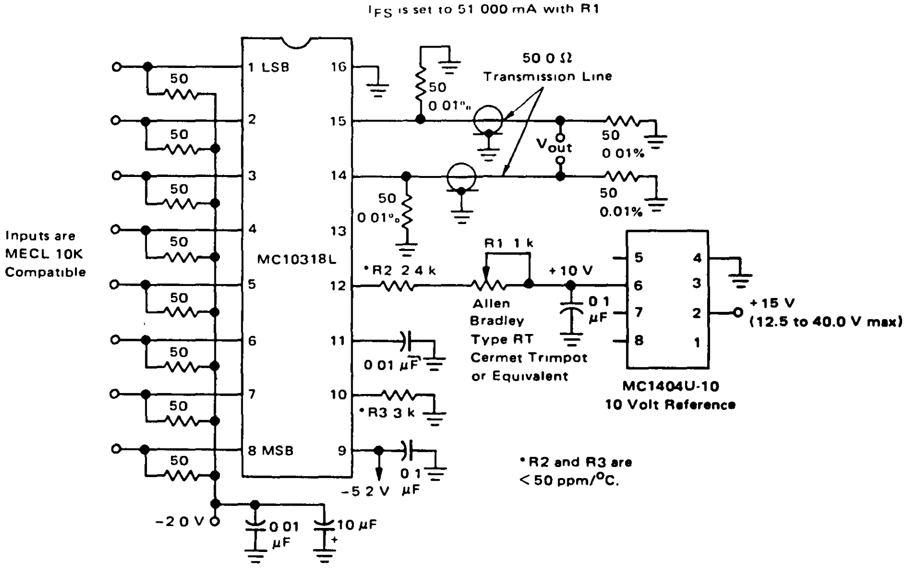
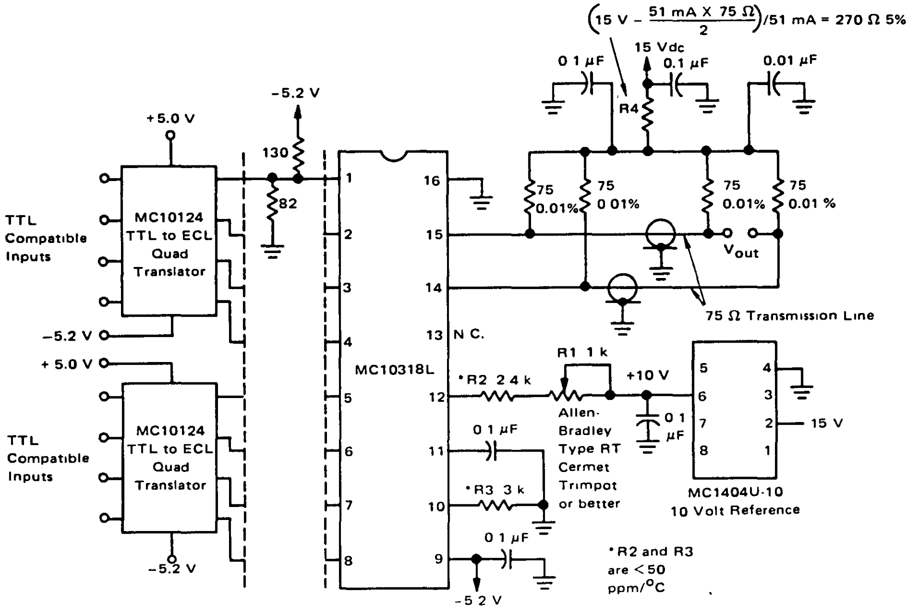


FIGURE 2 – TYPICAL CONNECTIONS FOR 50 Ω TRANSMISSION LINE



NOTE. Line impedances and termination impedance must be homogeneous 50 00 Ω. Any deviation will cause reflections which will seriously affect settling time Optimum performance cannot be realized with sockets. Good 1.0 GHz microstripline techniques must be used

FIGURE 3 – TYPICAL CONNECTIONS FOR 75 Ω TRANSMISSION LINE AND TTL-COMPATIBLE INPUTS



NOTE. See caution on line and termination impedance in Figure 2 and text

APPLICATION INFORMATION

Functional Test Circuit Construction

Test circuits used to evaluate this device or circuit designs used in actual practical situations must employ good 1.0 GHz RF microstripline practices if optimum performance is to be achieved from this device. Both line and termination impedances must be matched to within ±0.19% to minimize reflections which will appear as increased settling time. The use of sockets for initial evaluation is not recommended if specified settling time is to be obtained.

Applications information can be obtained by contacting:

Application Engineering
(602) 244-3021

If desired, test circuit artwork and board specifications will be supplied by contacting:

Linear Interface Marketing
(602) 962-2294

Successive Approximation A/D Converter

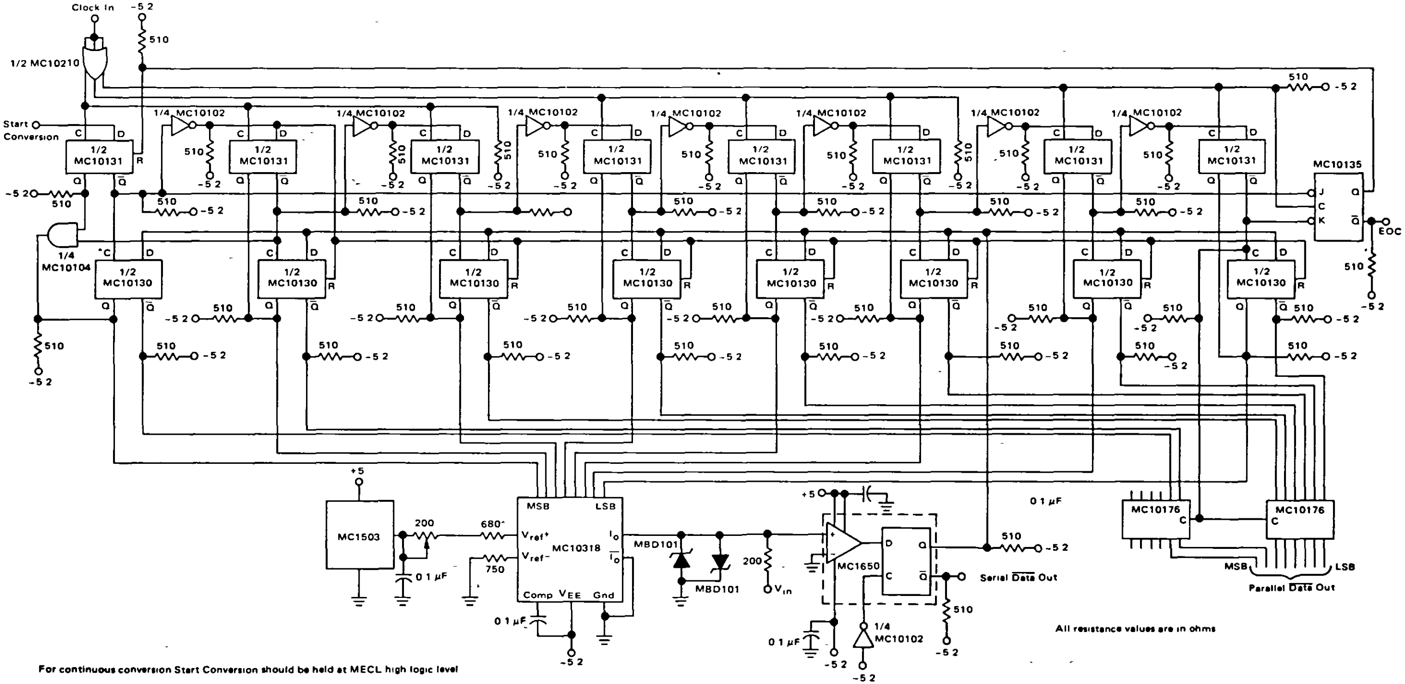
The circuit shown in Figure 4 uses the MC10318 in a successive approximation analog-to-digital converter. The circuit as shown will operate at a clock frequency above 30 MHz if proper attention is given to layout.

The full-scale voltage (V_{FS}) for the circuit as shown is 10.20 V. This full-scale voltage may be changed by changing the 200 Ω resistor to a value given by:

$$R = \frac{V_{FS}}{I_{FS}} = \frac{V_{FS}}{51\ \text{mA}}$$

However, at low values of V_{FS} the resolution of the comparator must be considered to maintain a ±1/2 LSB accuracy.

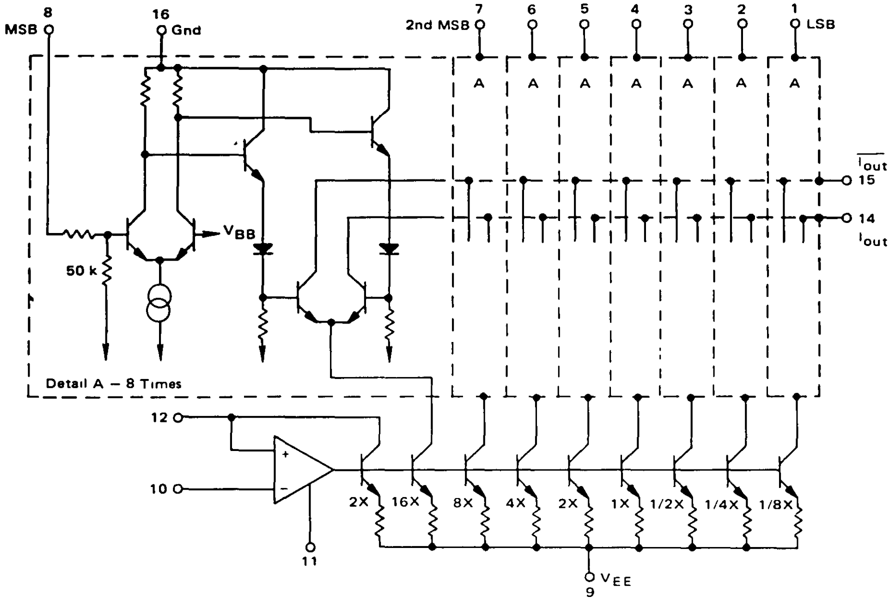
FIGURE 4 – SUCCESSIVE APPROXIMATION A/D CONVERTER USING MC10318

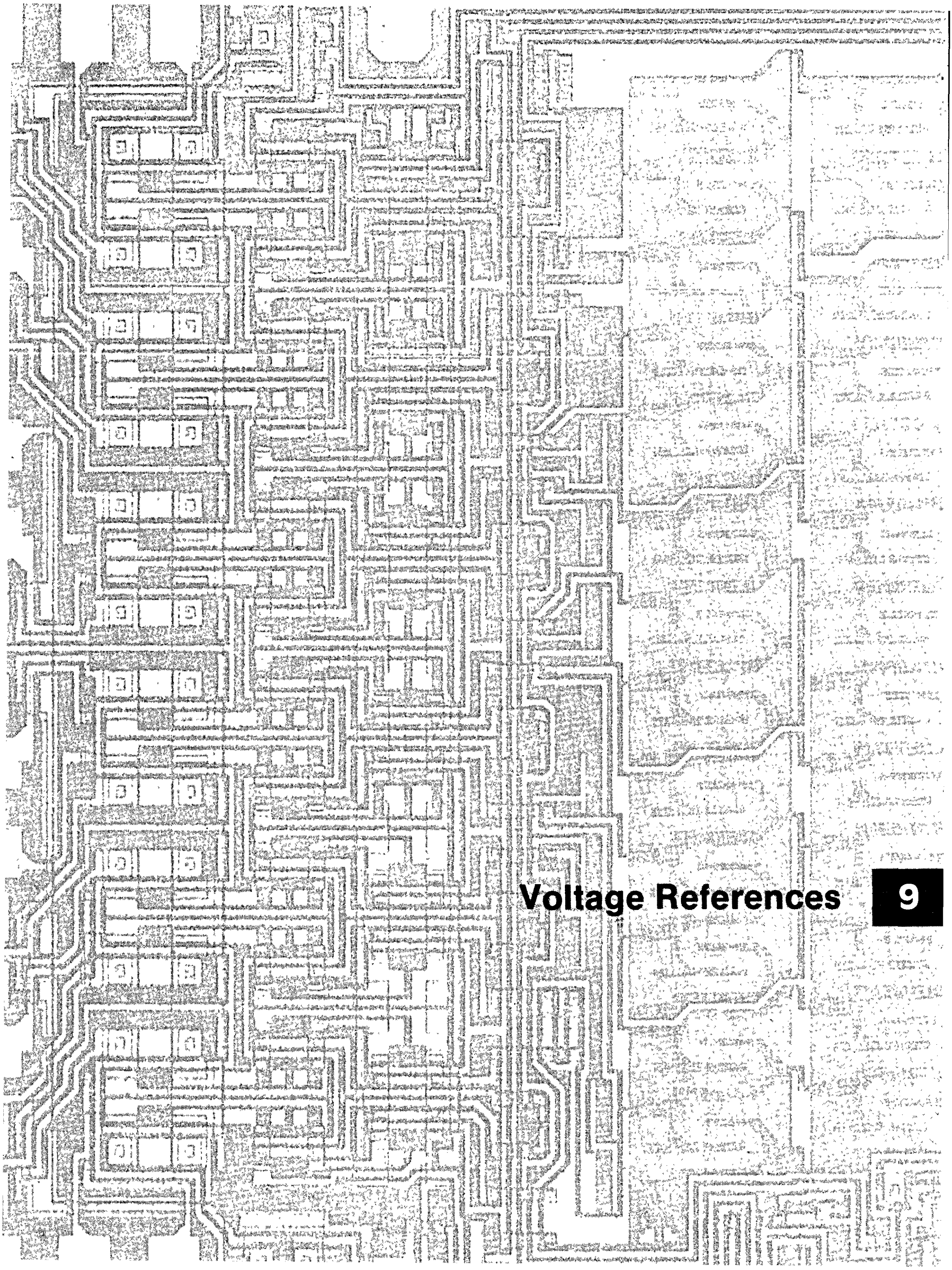


For continuous conversion Start Conversion should be held at MECL high logic level

All resistance values are in ohms

FIGURE 5 — MC10318 EQUIVALENT CIRCUIT





Voltage References

9

VOLTAGE REFERENCES

MOTOROLA

MC1400 MC1400A
MC1500 MC1500A

Product Preview

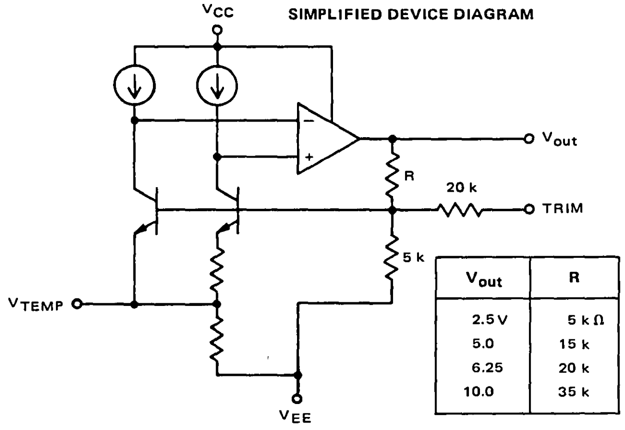
TIGHT-TOLERANCE, LOW-DRIFT VOLTAGE REFERENCE FAMILY

The MC1400 series of ICs is a family of temperature-compensated voltage references for precision data conversion and instrumentation applications. Advances in thin-film resistors, laser-trimming techniques, ion-implanted devices, and monolithic fabrication techniques make this reference both temperature and time stable in applications demanding accuracy to the 16-bit level.

These devices offer simple, no-external-component operation as three-terminal, positive-voltage references, and also simple, one-external-resistor operation as either positive or negative references. Unique circuitry permits these devices to either source or sink greater than 10 mA of load current with excellent regulation. This feature means that the buffer amplifiers and current sources normally required for precision zener references can be eliminated.

- Four Different Output Voltages: 2.5, 5.0, 6.25, 10 V
- Tight Absolute Accuracy: ±0.2% Maximum Initial Tolerance
- Single-Component Output Trimming Without Degrading Temperature Coefficient
- Wide Input Voltage Range: V_{REF} +1.0 V to +40 V
- Three-Terminal Operation:
  - Positive References That Can Source and Sink Current
- Two-Terminal Operation:
  - Positive or Negative References
  - Floating References
- Low Current Consumption: 0.75 mA Typical
- Very Low Temperature Coefficient: 5 ppm / °C Typical
- Low Output Noise Voltage
- Excellent Ripple Rejection: 100 dB Typical at 120 Hz
- Excellent Long Term Stability: 25 ppm / 1000 Hrs Typical

SIMPLIFIED DEVICE DIAGRAM



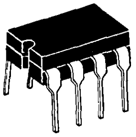
V_{out}	R
2.5 V	5 kΩ
5.0	15 k
6.25	20 k
10.0	35 k

This is advance information and specifications are subject to change without notice.

PRECISION VOLTAGE REFERENCES

2.5, 5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER-TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



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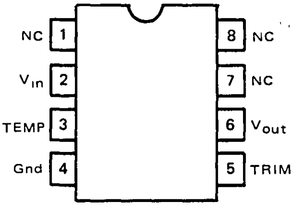


ORDERING INFORMATION

PACKAGE (ALL TYPES)
Ceramic DIP

Device	Temperature Range
2.5 Volts	
MC1500U2	−55°C to +125°C
MC1500AU2	−55°C to +125°C
MC1400U2	0°C to +70°C
MC1400AU2	0°C to +70°C
5.0 Volts	
MC1500U5	−55°C to +125°C
MC1500AU5	−55°C to +125°C
MC1400U5	0°C to +70°C
MC1400AU5	0°C to +70°C
6.25 Volts	
MC1500U6	−55°C to +125°C
MC1500AU6	−55°C to +125°C
MC1400U6	0°C to +70°C
MC1400AU6	0°C to +70°C
10 Volts	
MC1500U10	−55°C to +125°C
MC1500AU10	−55°C to +125°C
MC1400U10	0°C to +70°C
MC1400AU10	0°C to +70°C

MOTOROLA

MC1403,A
MC1503,A

PRECISION LOW-VOLTAGE REFERENCE

LASER TRIMMED
SILICON MONOLITHIC
INTEGRATED CIRCUIT

LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

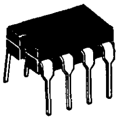
- Output Voltage = 2.5 V ±25 mV
- Input Voltage Range = 4.5 V to 40 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP Package

Typical Applications

- Voltage Reference for 8-12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temepraturе Range	T_A		
MC1503,A		-55 to +125	°C
MC1403,A		0 to +70	°C



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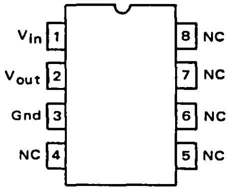
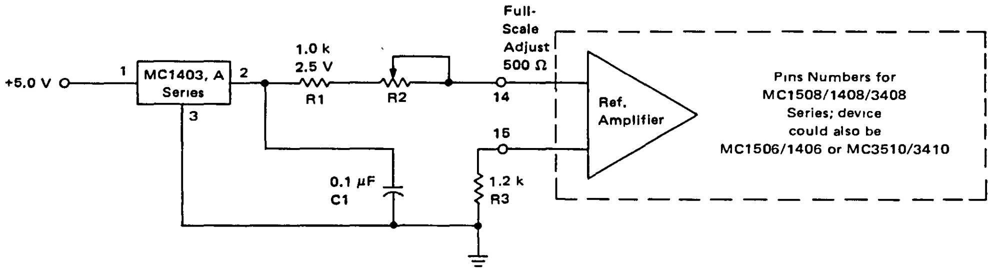


FIGURE 1 – A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1406/1506, MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_I = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503 } -55°C to +125°C		–	–	25	
MC1503A } -55°C to +125°C		–	–	11	
MC1403 } 0°C to +70°C		–	–	7.0	
MC1403A } 0°C to +70°C		–	–	4.4	
Line Regulation	Reg_{in}				mV
($15 V < V_I < 40 V$)		–	1.2	4.5	
($4.5 V < V_I < 15 V$)		–	0.6	3.0	
Load Regulation ($0 mA < I_O < 10 mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	mA

FIGURE 2 – MC1403/1503 SCHEMATIC

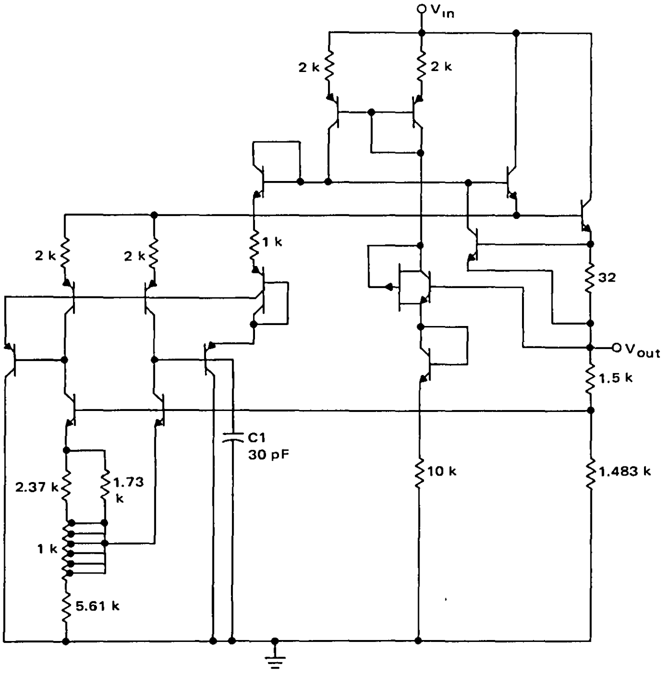


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in} (NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

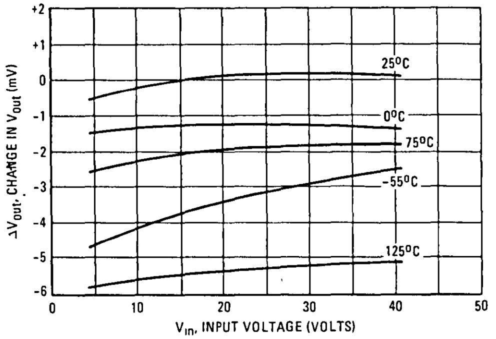


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE versus LOAD CURRENT (NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

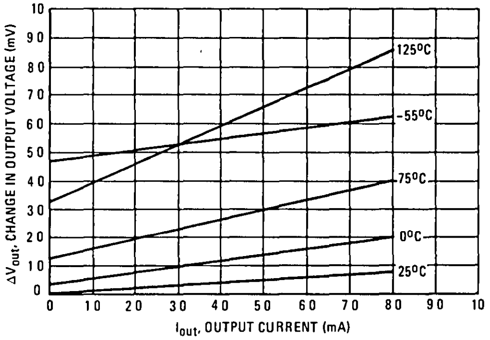


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE (V_{in} = 15 V, I_{out} = 0 mA)

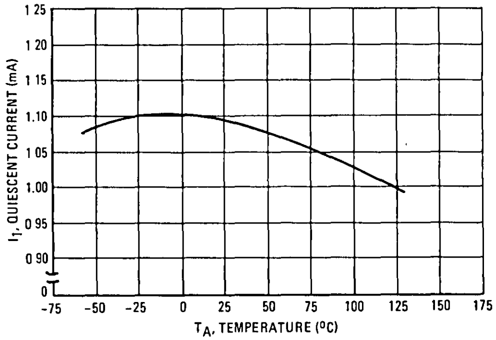


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO V_{out} @ V_{in} = 15 V)

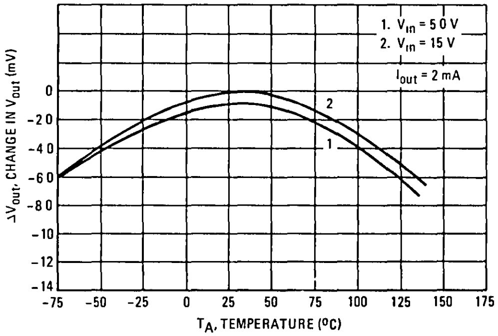
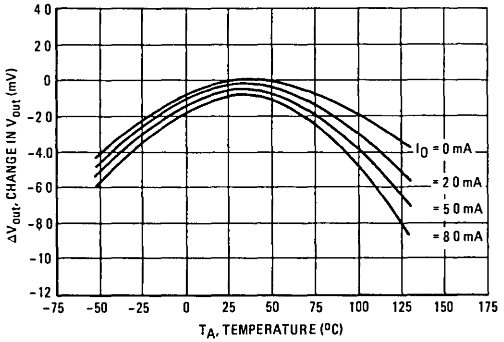


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO T_A = I_Q, V_{in} = 15 V, I_{out} = 0 mA)



3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

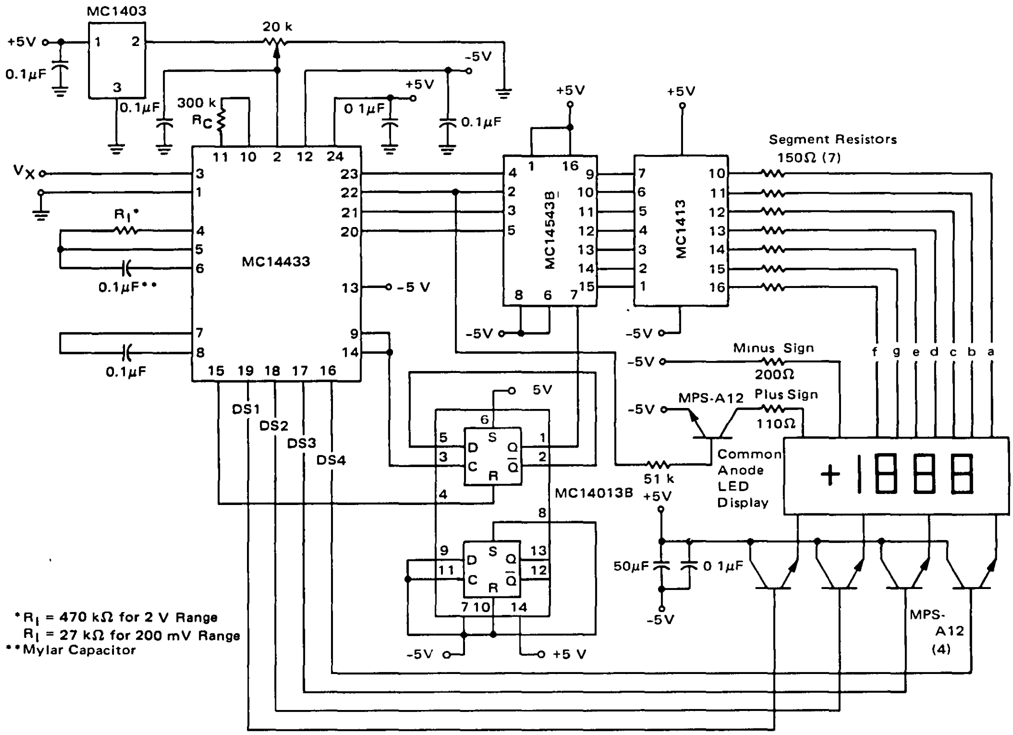
An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 – 3-1/2-DIGIT VOLTMETER



*R_I = 470 kΩ for 2 V Range
R_I = 27 kΩ for 200 mV Range
**Mylar Capacitor

MOTOROLA

MC1404 MC1404A MC1504 MC1504A

VOLTAGE REFERENCE FAMILY

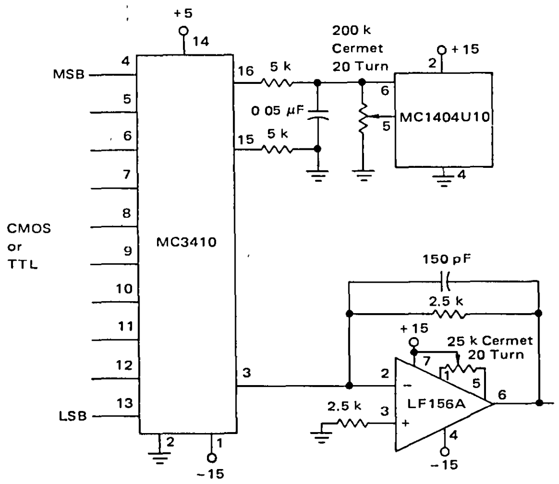
The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ± 6%
- Wide Input Voltage Range: V_{REF} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

TYPICAL APPLICATIONS

- Voltage Reference for 8 - 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

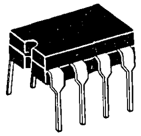
FIGURE 1 – VOLTAGE OUTPUT 10-BIT DAC USING MC1404U10



PRECISION LOW-DRIFT VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



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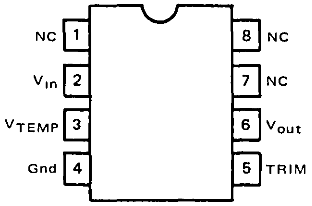


ORDERING INFORMATION

PACKAGE (ALL TYPES)
Ceramic DIP

Device	Temperature Range
5.0 Volts	
MC1504U5	-55°C to +125°C
MC1504AU5	-55°C to +125°C
MC1404U5	0°C to +70°C
MC1404AU5	0°C to +70°C
6.25 Volts	
MC1504U6	-55°C to +125°C
MC1504AU6	-55°C to +125°C
MC1404U6	0°C to +70°C
MC1404AU6	0°C to +70°C
10 Volts	
MC1504U10	-55°C to +125°C
MC1504AU10	-55°C to +125°C
MC1404U10	0°C to +70°C
MC1404AU10	0°C to +70°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range MC1504,A MC1404,A	T_A	 -55 to +125 0 to +70	 °C °C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504,A			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (I_O = 0 mA)	V_O							Volt
U5, AU5		4.95	5.00	5.05	4.95	5.00	5.05	
U6, AU6		6.19	6.25	6.31	6.19	6.25	6.31	
U10, AU10		9.90	10	10.10	9.90	10	10.10	
Output Voltage Tolerance	–	–	±0.1	±1.0	–	±0.1	±1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)	ΔV_{TRIM}	±6.0	–	–	±6.0	–	–	%
Output Voltage Temperature Coefficient, Over Full Temperature Range	$\Delta V_O/\Delta T$							ppm/°C
MC1404, MC1504		–	10	40	–	–	55	
MC1404A, MC1504A		–	10	25	–	–	25	
Maximum Output Voltage Change Over Temperature Range	ΔV_O							mV
MC1404U5, MC1504U5		–	–	14	–	–	50	
MC1404AU5, MC1504AU5		–	–	9.0	–	–	23	
MC1404U6, MC1504U6		–	–	17.5	–	–	62	
MC1404AU6, MC1504AU6		–	–	11	–	–	28	
MC1404U10, MC1504U10		–	–	28	–	–	99	
MC1404AU10, MC1504AU10		–	–	18	–	–	45	
Line Regulation (1) (V_{in} = V_{out} + 2.5 V to 40 V, I_{out} = 0 mA)	Reg_{LINE}	–	2.0	6.0	–	2.0	6.0	mV
Load Regulation (1) ($0 \leq I_O \leq 10$ mA)	Reg_{LOAD}	–	–	10	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	–	1.2	1.5	mA
Short Circuit Current	I_{sc}	15	20	30	–	–	30	mA
Long Term Stability	–	–	25	–	–	25	–	ppm/1000 hrs

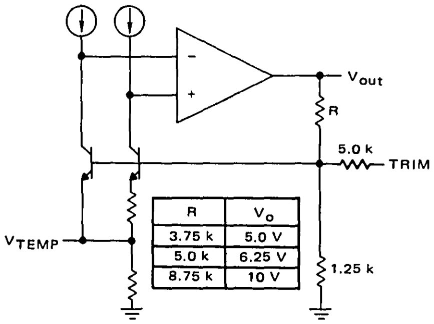
Note 1. Includes thermal effects.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504,A			Unit
		Min	Typ	Max	Min	Typ	Max	
Turn-On Settling Time (to ±0.01%)	t_S	–	50	–	–	50	–	µs
Output Noise Voltage – P to P (Bandwidth 0.1 to 10 Hz)	e_n	–	12	–	–	12	–	µV
Small-Signal Output Impedance	r_o							Ω
120 Hz		–	0.15	–	–	0.15	–	
500 Hz		–	0.2	–	–	0.2	–	
Power Supply Rejection Ratio	PSRR	70	80	–	70	80	–	dB

TYPICAL CHARACTERISTICS

FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM



R	V_o
3.75 k	5.0 V
5.0 k	6.25 V
8.75 k	10 V

FIGURE 3 – LINE REGULATION versus TEMPERATURE

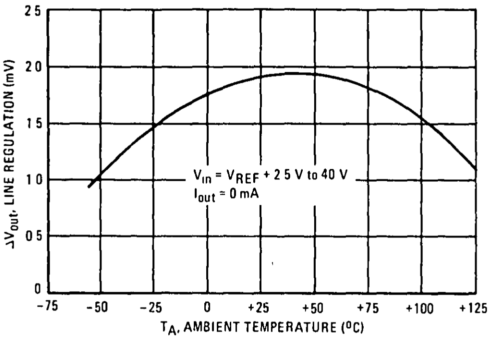


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE MC1404U10

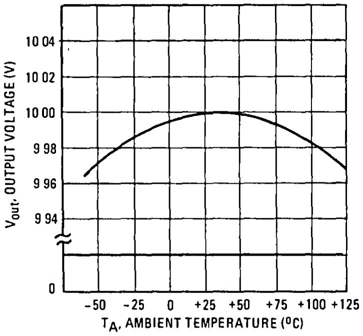


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

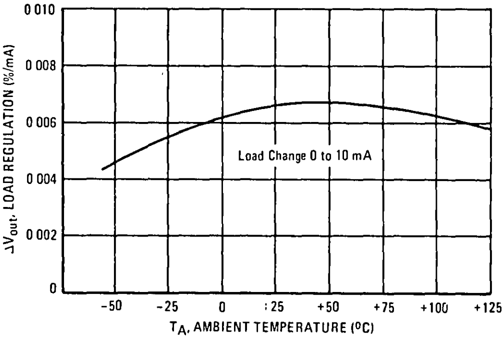


FIGURE 6 – POWER SUPPLY REJECTION RATIO versus FREQUENCY

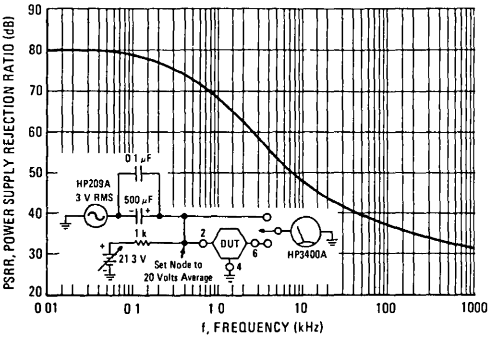


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE

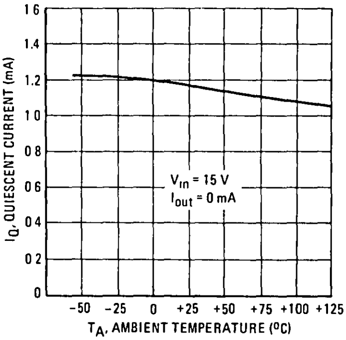


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

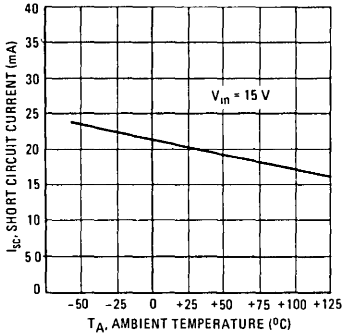


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE

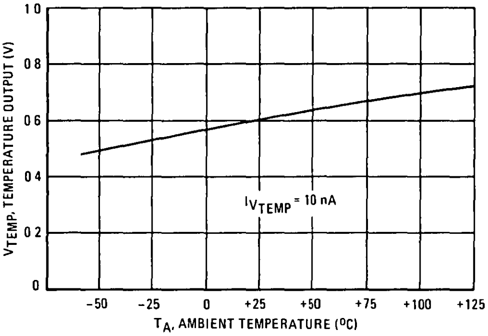
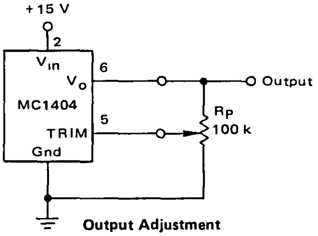


FIGURE 10 – OUTPUT TRIM CONFIGURATION

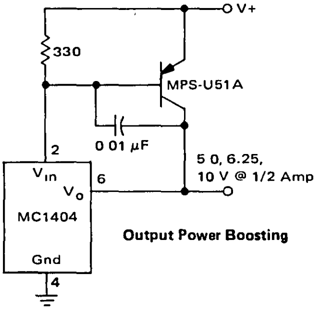


Output Adjustment

The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range For example, the output can be set to 10.000 V or to 10.240 V for binary applications For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ±6.0%.

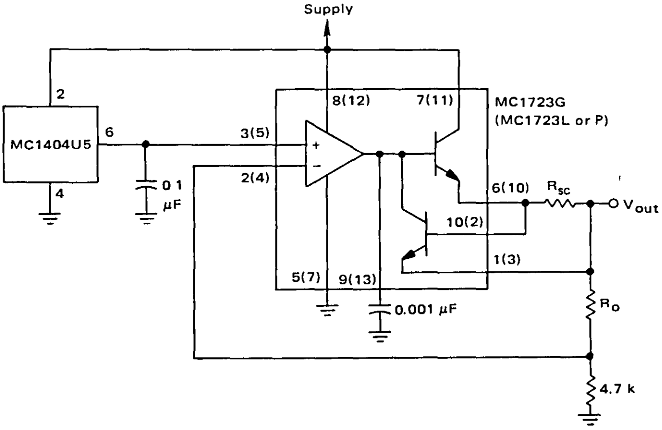
FIGURE 11 – PRECISION SUPPLY USING MC1404



Output Power Boosting

The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation If the power transistor current gain exceeds 75, a one ampere supply can be realized

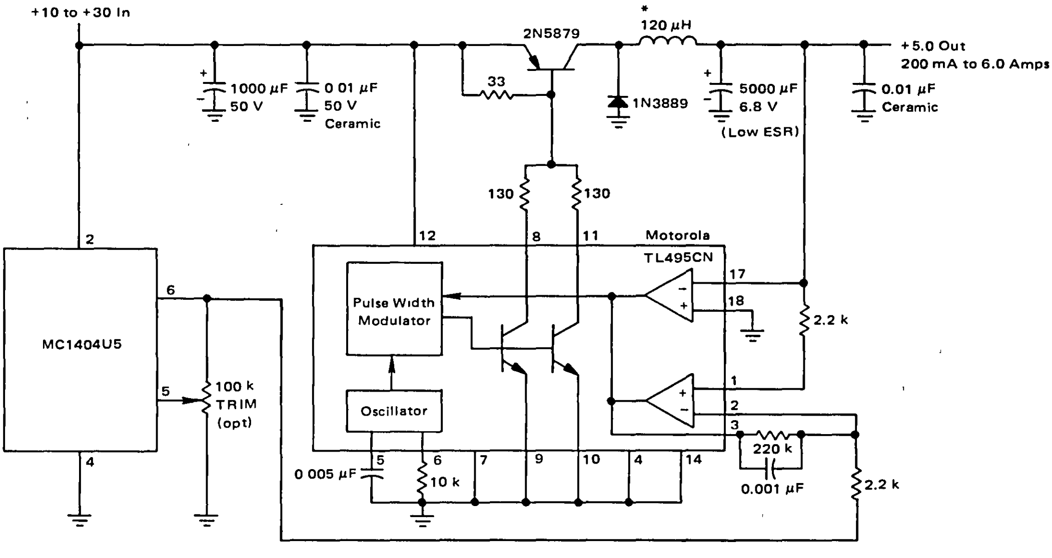
FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR



$$V_{out} = 5\ 0\ V \left(\frac{R_o + 4.7\ k}{4.7\ k}\right)$$

$$I_{omax} \approx \frac{0\ 6\ V}{R_{sc}}$$

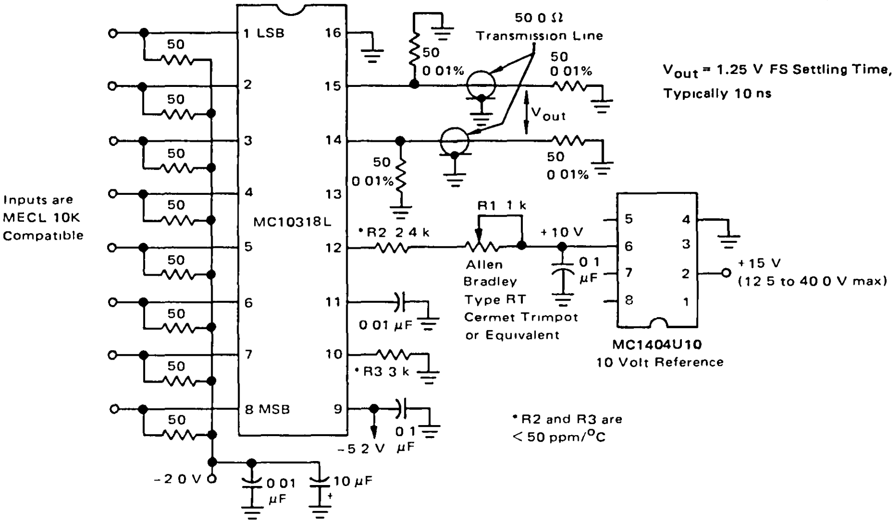
FIGURE 13 — 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE

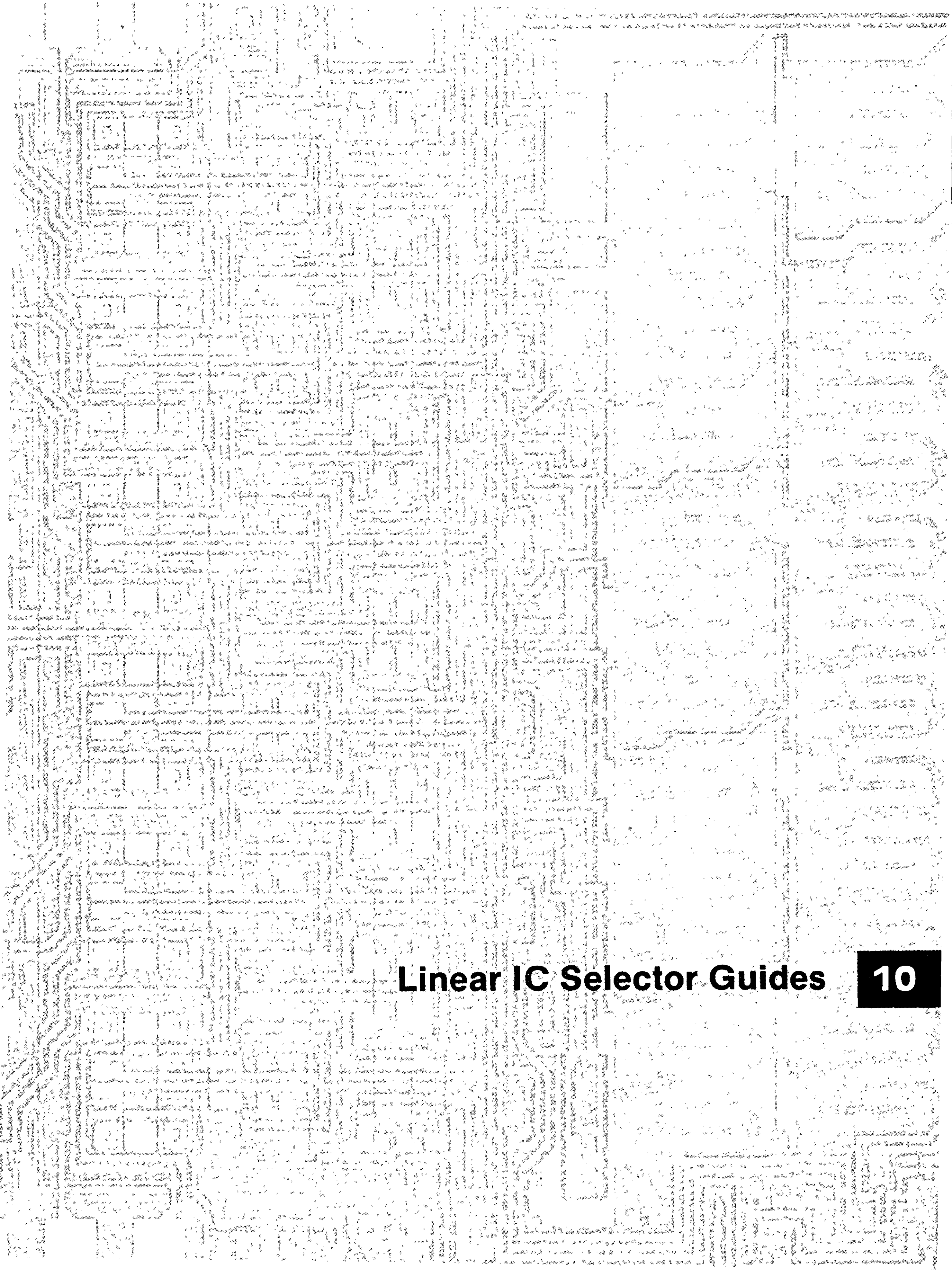


*40 Turns #16 Wire, Arnold A-894075-2 Ferrite Core

FIGURE 14 — HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10

I_{FS} is set to 51 000 mA with R1





Linear IC Selector Guides

10

OPERATIONAL AMPLIFIERS

Motorola offers a broad line of operational amplifiers to meet a wide range of usages. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of package styles as well as standard chips.

Single Operational Amplifiers

NONCOMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LM101A	0.075	2.0	10	10	50K	1.0	0.5	±3.0	±22	General Purpose	601, 693
LM108	0.002	2.0	3.0	0.2	50K	1.0	0.3	±3.0	±20	Precision	601, 606, 693
LM108A	0.002	0.5	1.0	0.2	80K	1.0	0.3	±3.0	±20	Precision	601, 606, 693
MC1520	2.0	10	15	100	1K	10	5.0	±4.0	±8.0	Differential Output	603, 606
MC1530	10	5.0	15	2.0µA	4.5K	3.0	1.0	±4.0	±9.0	General Purpose	603B, 606, 632
MC1531	15	10	15	25	2.5K	2.0	1.0	±4.0	±9.0	General Purpose (Darlington Input)	603B, 606, 632
MC1533	1.0	5.0	15	150	40K	0.8	2.0	±4.0	±20	General Purpose	603B, 606, 632
MC1539	0.5	3.0	15	60	50K	2.0	4.2	±4.0	±18	High Slew Rate	601, 632
MC1709	0.5	5.0	15	200	25K	1.0	0.3	±3.0	±18	General Purpose	601, 606, 632, 693
MC1709A	0.6	3.0	5.0	100	25K	1.0	0.5	±3.0	±18	High Performance MC1709	601, 606, 632
MC1712	5.0	2.0	15	500	2.5K	7.0	1.5	+6.0 -3.0	+14 -7.0	Wideband DC Amplifier	601, 606, 632
MC1748	0.5	5.0	15	200	50K	1.0	0.5	±3.0	±22	General Purpose	601, 693
Industrial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25K	1.0	0.5	±3.0	±18	General Purpose	601, 626, 693
LM308	7.0	7.5	15	1.0	25K	1.0	0.3	±3.0	±18	Precision	601, 606, 626, 693
LM308A	7.0	0.5	5.0	1.0	80K	1.0	0.3	±3.0	±18	Precision	601, 606, 626, 693
MC1420	4.0	15	15	200	750	10	5.0	±4.0	±8.0	Differential Output	603, 606
MC1430	15	10	15	4.0µA	3K	3.0	1.0	±4.0	±8.0	General Purpose	603B, 606, 632, 646
MC1431	0.3	15	15	100	1.5K	2.0	1.0	±4.0	±8.0	General Purpose (Darlington Input)	603B, 606, 632, 646
MC1433	2.0	7.5	15	50	30K	0.8	2.0	±4.0	±18	General Purpose	603B, 606, 632, 646
MC1439	1.0	7.5	15	100	15K	2.0	4.2	±6.0	±18	High Slew Rate	601, 626, 632, 646
MC1709C	1.5	7.5	15	500	15K	1.0	0.3	±3.0	±18	General Purpose	601, 606, 626, 632, 646, 693
MC1712C	7.5	5.0	15	2.0µA	2K	7.0	1.5	+6.0 -3.0	+14 -7.0	Wideband DC Amplifier	601, 606, 632
MC1748C	0.5	6.0	15	200	20K	1.0	0.5	±3.0	±18	General Purpose	601, 626, 693

Single Operational Amplifiers

INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LF155	100pA	5.0	5.0	20pA	50K	1.0	5.0	±5.0	±22	FET Input	601
LF155A	50pA	2.0	3.0	10pA	50K	1.0	5.0	±5.0	±22	FET Input	601
LF156	100pA	5.0	5.0	20pA	50K	2.0	15	±5.0	±22	FET Input	601
LF156A	50pA	2.0	3.0	10pA	50K	2.0	15	±5.0	±22	FET Input	601
LF157	100pA	5.0	5.0	20pA	50K	3.0	75	±5.0	±22	Wideband FET Input	601
LF157A	50pA	2.0	3.0	10pA	50K	3.0	75	±5.0	±22	Wideband FET Input	601
LM107	0.075	2.0	10	10	50K	1.0	0.5	±3.0	±22	General Purpose	601, 693
MC1536	0.02	5.0	10	3.0	100K	1.0	2.0	±15	±40	High Voltage	601
MC1556	0.015	4.0	10	2.0	100K	1.0	2.5	±3.0	±22	High Performance	601, 632
MC1733	0.20	–	–	3.0µA	90	90	–	±4.0	±8.0	Differential Wideband Video Amp	603, 632
MC1741	0.5	5.0	15	200	50K	1.0	0.5	±3.0	±22	General Purpose	601, 606, 632, 693
MC1741N	0.5	5.0	15	200	50K	1.0	0.5	±3.0	±22	Low Noise	601, 606, 632, 693
MC1741S	0.5	5.0	15	200	50K	1.0	10	±3.0	±22	High Slew Rate	601, 632, 693
MC1776	0.0075	5.0	15	3.0	200K	1.0	0.2	±1.5	±18	µPower Programmable	601, 632
MC35001	100pA	10	10	100pA	25K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
MC35001A	75pA	2.0	10	25pA	50K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
MC35001B	100pA	5.0	10	50pA	50K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
Industrial Temperature Range (0°C to +70°C)											
LF355	200pA	10	5.0	50pA	50K	1.0	5.0	±5.0	±18	FET Input	601
LF355A	50pA	2.0	1.0	10pA	50K	1.0	5.0	±5.0	±18	FET Input	601
LF356	200pA	10	5.0	50pA	50K	2.0	15	±5.0	±18	FET Input	601
LF356A	50pA	2.0	1.0	10pA	50K	2.0	15	±5.0	±18	FET Input	601
LF357	200pA	10	5.0	50pA	50K	3.0	75	±5.0	±18	Wideband FET Input	601
LF357A	50pA	2.0	1.0	10pA	50K	3.0	75	±5.0	±18	Wideband FET Input	601
LM307	0.25	7.5	10	50	25K	1.0	0.5	±3.0	±18	General Purpose	601, 626, 693
MC1436	0.04	10	12	10	70K	1.0	2.0	±15	±34	High Voltage	601
MC1456	0.03	10	12	10	70K	1.0	2.5	±3.0	±18	High Performance	601, 632
MC1733C	30	–	–	5.0µA	80	90	–	±4.0	±8.0	Differential Wideband Video Amp	601, 632, 646
MC1741C	0.5	6.0	15	200	20K	1.0	0.5	±3.0	±18	General Purpose	601, 632, 626, 646, 693
MC1741NC	0.5	6.0	15	200	20K	1.0	0.5	±3.0	±18	Low Noise	601, 632, 626, 646, 693
MC1741SC	0.5	6.0	15	200	20K	1.0	10	±3.0	±18	High Slew Rate	601, 632, 626, 646, 693
MC1776C	0.003	6.0	15	3.0	100K	1.0	0.2	±1.5	±18	µPower, Programmable	601
MC3476	0.05	6.0	15	25	50K	1.0	0.2	±1.5	±18	Low Cost µPower, Programmable	601, 626
MC34001	200pA	10	10	100pA	25K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34001A	100pA	2.0	10	50pA	50K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34001B	200pA	5.0	10	100pA	50K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693

Dual Operational Amplifiers

INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	Supply Voltage V max	Description	Packages
Military Temperature Range (-55°C to +125°)											
LM158	0.15	5.0	10	30	50K	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	601, 632, 693
MC1558	0.5	5.0	10	200	50K	1.1	0.8	±3.0	±22	Dual MC1741	601, 632, 693
MC1558N	0.5	5.0	10	200	50K	1.1	0.8	±3.0	±22	Low Noise	601, 632, 693
MC1558S	0.5	5.0	10	200	50K	1.0	10	±3.0	±22	High Slew Rate	601, 632, 693
MC1747	0.5	5.0	10	200	50K	1.0	0.5	±3.0	±22	Dual MC1741	601, 632
MC3558	0.5	5.0	10	50	50K	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	601, 632, 693
MC4558	0.5	5.0	10	200	50K	4.0	1.5	±3.0	±22	High Frequency	601, 632, 693
MC35002	100pA	10	10	100pA	25K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
MC35002A	75pA	2.0	10	25pA	50K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
MC35002B	100pA	5.0	10	50pA	50K	4.0	13	±5.0	±22	TRIMFET Input	601, 693
MC35022	150pA	2.0	5.0	70pA	25K	4.0	13	±5.0	±22	Precision TRIMFET Input	601, 693
MC35022A	60pA	0.5	5.0	25pA	50K	4.0	13	±5.0	±22	Precision TRIMFET Input	601, 693
MC35022B	75pA	1.0	5.0	50pA	50K	4.0	13	±5.0	±22	Precision TRIMFET Input	601, 693
Industrial Temperature Range (0°C to +70°C)											
LM358	0.25	6.0	7.0	50	25K	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	601, 626, 693
MC1458	0.5	6.0	10	200	20K	1.1	0.8	±3.0	±18	Dual MC1741	601, 626, 632, 646, 693
MC1458N	0.5	6.0	10	200	20K	1.1	0.8	±3.0	±18	Low Noise	601, 626, 632, 646, 693
MC1458S	0.5	6.0	10	200	20K	1.0	10	±3.0	±18	High Slew Rate	601, 626, 632 646, 693
MC1747C	0.5	6.0	10	200	25K	1.0	0.5	±3.0	±18	Dual MC1741	603, 632, 646
MC3458	0.5	10	7.0	50	20K	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Crossover Distortion)	601, 626, 693
MC4558C	0.5	6.0	10	200	20K	3.0	1.5	±3.0	±18	High Frequency	601, 626, 693
MC34002	100pA	10	10	100pA	25K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34002A	75pA	2.0	10	50pA	50K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34002B	100pA	5.0	10	70pA	25K	4.0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34022	150pA	2.0	5.0	70pA	25K	4.0	13	±5.0	±18	Precision TRIMFET Input	601, 626, 693
MC34022A	75pA	0.5	5.0	30pA	50K	4.0	13	±5.0	±18	Precision TRIMFET Input	601, 626, 693
MC34022B	150pA	1.0	5.0	70pA	50K	4.0	13	±5.0	±18	Precision TRIMFET Input	601, 626, 693
Automotive Temperature Range (-40°C to +85°C)											
MC3358	5.0	8.0	10	75	20K	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	626

NONCOMPENSATED

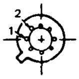
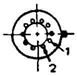
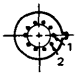
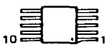
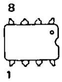
Military Temperature Range (-55°C to +125°C)											
MC1535	3.0	3.0	10	300	4K	1.0	0.01	±2.0	±10	General Purpose	603B, 606, 632
MC1537	0.5	5.0	10	200	25K	1.0	0.25	±3.0	±18	Dual MC1709	632
Industrial Temperature Range (0°C to +70°C)											
MC1435	5.0	5.0	10	500	3.5K	1.0	0.01	±2.0	±9.0	General Purpose	603B, 607, 632
MC1437	1.5	7.5	10	500	15K	1.0	0.25	±3.0	±18	Dual MC1709	632, 646

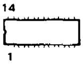
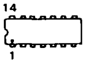
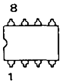
Quad Operational Amplifiers

INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	Supply Voltage V max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50K	1.0	0.6	±1.5	±16	Low Power	632, 646
								+3.0	+32	Consumption	
MC3503	0.5	5.0	7.0	50	50K	1.0	0.6	±1.5	±18	General Purpose	632, 646
								+3.0	+36	Low Power	
MC4741	0.5	5.0	15	200	50K	1.0	0.5	±3.0	±22	Quad MC1741	632, 646
MC35004	100pA	10	10	100pA	25K	4.0	13	±5.0	±22	Trimmed FET Input	632
MC35004A	75pA	2.0	10	25pA	50K	4.0	13	±5.0	±22	Trimmed FET Input	632
MC35004B	100pA	5.0	10	50pA	50K	4.0	13	±5.0	±22	Trimmed FET Input	632
Industrial Temperature Range (0°C to 70°C)											
LM324	0.25	6.0	7.0	50	25K	1.0	0.6	±1.5	±16	Low Power	632, 646
								+3.0	+32	Consumption	
MC3401	0.3	–	–	–	1K	5.0	0.6	±1.5	±18	Norton Input	632, 646
								+3.0	+36		
MC3403	0.5	10	7.0	50	20K	1.0	0.6	±1.5	±18	No Crossover	632, 646
								+3.0	+36	Distortion	
MC4741C	0.5	6.0	15	200	20K	1.0	0.5	±3.0	±18	Quad MC1741	632, 646
MC34004	200pA	10	10	100pA	25K	4.0	13	±5.0	±18	Trimmed FET Input	632, 646
MC34004A	100pA	2.0	10	50pA	50K	4.0	13	±5.0	±18	Trimmed FET Input	632, 646
MC3400B	200pA	5.0	10	100pA	50K	4.0	13	±5.0	±18	Trimmed FET Input	632, 646
Automotive Temperature Range (-40°C to +85°C)											
LM2902	0.5	10	–	50	–	1.0	0.6	±1.5	±13	Differential	646
								+3.0	+26	Low Power	
MC3301	0.3	–	–	–	1K	4.0	0.6	±2.0	±15	Norton Input	646
								+4.0	+28		
MC3303	0.5	8.0	10	75	20K	1.0	0.6	±1.5	±18	Differential	646
								+3.0	+36	General Purpose	

Package Styles

LEAD CONFIGURATION					
CASE	601	603	603B	606	626
MATERIAL	Metal	Metal	Metal	Ceramic	Plastic
SUFFIX after type number	G, H	G, H	G, H	F	P, P1, N

			
CASE	632	646	693
MATERIAL	Ceramic	Plastic	Ceramic
SUFFIX after type number	J, L	P, P2	J, U

VOLTAGE REGULATORS

Fixed Output Voltage Regulators

- **Low-cost monolithic circuits for positive and/or negative regulation at currents from 100 mA to 1.5A**
- **Ideal for on-card regulation of subsystems**
- **Internal current limiting thermal shutdown and safe-area compensation**

FIXED-VOLTAGE, 3-TERMINAL REGULATORS FOR POSITIVE OR NEGATIVE POLARITY POWER SUPPLIES.

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
2	±0.1	1500	–	MC7902C	5.5/35	40	120	1 0	1, 221A
3	±0 15	100	–	MC79L03AC	4 7/30	60	72	–	29, 79
	±0 3			MC79L03C		80			
5	±0 5	100	MC78L05C	MC79L05C	6 7/30	200	60	–	29, 79
	±0 25		MC78L05AC	MC79L05AC		150			
		500	MC78M05C	–	7/35	100	100	1 0	79, 221A
	±0 4	1500	LM109	–	.			1 1	1, 79
			LM209	–				1 0	
	±0 25		LM309	–		50			
	±0 35		**MC7805*	–	8 0/35			0 6	1
	±0 25		MC7805C	MC7905C	7/35	100		1 0	1, 221A
	±0 2		**MC7805A*	–	7 5/35	10	50	0 6	1
			**MC7805AC	–			100		1, 221A
	±0 25		**LM140 5*	–	7/35	50	50		1
			**LM340-5	–					
5 2	±0 26	1500	–	MC7905 2C	7 2/35	105	105	1 0	1, 221A
6	±0 3	500	MC78M06C	–	8/35	100	120	1 0	79, 221A
	±0 35	1500	**MC7806*	–	9/35	60	100	0 7	1
	±0 3		MC7806C	MC7906C	8/35	120	120		1, 221A
	±0 24		**MC7806A*	–	8 6/35	11	50		1
			**MC7806AC	–			100		1, 221A
	±0.3		**LM140 6*	–	8/35	60	60		1
			**LM340 6	–					
8	±0 8	100	MC78L08C	–	9 7/30	200	80	–	29, 79
			MC78L08AC	–		175			
	±0 4	500	MC78M08C	–	10/35	100	160	1 0	79, 221A
		1500	**MC7808*	–	11 5/35	80	100		1
			MC7808C	MC7908C	10/35	160	160		1, 221A
	±0 3		**MC7808A*	–	10 6/35	13	50		1
			**MC7808AC	–			100		1, 221A
	±0 4		**LM140-8*	–	10 5/35	80	80		1
			**LM340 8	–					
12	±1.2	100	MC78L12C	MC79L12C	13 7/35	250	100	–	29, 79
	±0 6		MC78L12AC	MC79L12AC					
		500	MC78M12C	–	14/35	100	240	1 0	79, 221A
		1500	**MC7812*	–	15 5/35	120	120	1.5	1
			MC7812C	MC7912C	14 5/35	240	240		1, 221A
	±0 5		**MC7812A*	–	14.8/35	18	50		1
			**MC7812AC	–			100		1, 221A
	±0 6		**LM140-12*	–	14.5/35	120	120	1 5	1
			**LM340-12	–					

**1979 New Product Introductions

*T_J = -55 to +150°C

†Output Voltage Tolerance for Worst Case

(continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	–	29, 79
	±0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	–	17/35	100	300	1.0	79, 221A
		1500	**MC7815*	–	18.5/35	150	150	1.8	1
			MC7815C	MC7915C	17.5/35	300	300		1, 221A
	±0.6		**MC7815A*	–	17.9/35	22	50		1
			**MC7815AC	–			100		1, 221A
	±0.75		**LM140-15*	–	17.5/35	150	150		1
			**LM340-15	–					
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	–	29, 79
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	–	20/35	100	360	1.0	79, 221A
		1500	**MC7818*	–	22/35	180	180	2.3	1
			MC7818C	MC7918C	21/35	360	360		1, 221A
	±0.7		**MC7818A*	–		31	50		1
			**MC7818AC	–			100		1, 221A
	±0.9		**LM140-18*	–		180	180		1
			**LM340-18	–					
20	±1.0	500	MC78M20C	–	22/40	10	400	1.1	79, 221A
24	±2 4	100	MC78L24C	MC79L24C	25.7/40	350	200	–	29, 79
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	–	26/40	100	480	1.2	79, 221A
		1500	**MC7824*	–	28/40	240	240	3 0	1
			MC7824C	MC7924C	27/40	480	480		1, 221A
	±1.0		**MC7824A*	–	27.3/40	36	50		1
			**MC7824AC	–	27/40		100		1, 221A
	±1.2		**LM140-24*	–		240	240		1
			**LM340-24	–					

**1979 New Product Introductions

*T_J = –55 to +150°C

†Output Voltage Tolerance for Worst Case

Variable Output Voltage Regulators

POSITIVE OUTPUT REGULATORS

I_O mA Max	Device Type	SUFFIX	V_{out} Volts		V_{in} Volts		$V_{in}-V_{out}$ Differential Volts Min	P_D Watts Max		Regulation % V_{out} @ T_A = 25°C Typ		TC V_{out} Typ %/°C	T_J = °C Max	Case
			Min	Max	Min	Max		T_C = 25°C	T_C = 25°C	Line	Load			
20	LM305	H	4.5	40	8 5	50	3.0	0 4	1 3	0 06	0.1	0.007	85	601
	LM205							0 68	1 6				100	
	LM105			30					2.7				150	
100	**LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0 04	0 5	0 006	125	29,79
	**LM217L									0 02	0.3	0.004	150	
	**LM117L*											0 003		
150	MC1723	CP	2.0	37	9.5	40	3 0	0 65	–	0.1	0 3	0.003	150	646
		CG						0 8	2.1	0 1		0.003		603C
		G								0.2		0.002		
		CL						1.0	–	0.1		0.003	175	632
		L							–	0.2		0 002		
250	MC1469	G	2.5	32	9	35	3 0	0.68	1.8	0 03	0.13	0 002	150	603
	MC1569			37	8 5	40	2 7			0 015				
600	MC1469	R	2.5	32	9 0	35	3 0	3.0	14 0	0 03	0.05	0 002	150	614
	MC1569			37	8 5	40	2 7			0 015				
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.07	1.5	0 006	125	221A
	LM317	H, K												79, 1
	LM217											0.004		
	LM117*									0 05	1.0	0 003	150	

*T_J = –55 to +150°C

**1979 New Product Introductions

Variable Output Voltage Regulators (continued)

NEGATIVE OUTPUT REGULATORS

I_O mA Max	Device Type	SUFFIX	V_{out} Volts		V_{in} Volts		$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max		Regulation % V_{out} @ $T_A = 25°C$ Typ		TC V_{out} Typ %/°C	T_J = °C Max	Case
			Min	Max	Min	Max		T_C = 25°C	T_C = 25°C	Line	Load			
20	LM304	H	0 035	30	8.0	40	2.0	0 4	1.3	0 1	0 05	0.007	80	603
	LM204		0 015	40		50		0 68	1.6				100	
	LM104								2.7				150	
250	MC1463	G	3.8	32	9 0	35	3 0	0 68	1.8	0 03	0.05	0 002	150	603
	MC1563		3.6	33	8 5	40	2.7			0.015	0 13			
600	MC1463	R	3.8	34	9 0	35	3.0	2 4	9 0	0.03	0 05	0.002	175	614
	MC1563		3.6	37	8.5	40	2.7			0 015				

Switching Regulators

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O ±mA Max	V_{CC} Volts		f_o kHz		Device Number	Suffix	T_A °C	Case
	Min	Max	Min	Max				
40	10	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	-55 to +125	620

Special Regulators

FLOATING VOLTAGE AND CURRENT REGULATORS

Designed for laboratory type power supplies. Voltage is limited only by the breakdown voltage of associated, external, series-pass transistors.

V_{out} Volts		I_O mA Max	Device Type	SUFFIX	V_{aux} Volts		P_D Watts Max	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/I_L$ % Max	TC V_{out} %/°C Typ	Case
Min	Max				Min	Max		Line	Load			
0	•	•	MC1466	L	21	30	0.75	0 015	0 015	0.2	0 01	632
			MC1566	L	20	35		0 004	0 004	0 1	0 006	

•Dependent on characteristics of external series-pass elements

DUAL ±15 V TRACKING REGULATORS.

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts		I_O mA Max	V_{in} Volts		Device Type	SUFFIX	P_D Watts Max	Reg_{line} mV	Reg_{load} mV	TC %/°C (T_{low} to T_{high}) Typ	T_A °C	Case
Min	Max		Min	Max								
14.8	15.2	±100	17	30	MC1468	G	0 8	10	10	3.0	0 to +75	603C
						L	1.0					632
						R	2.4					614
					MC1568	G	0 8				-55 to +125	603C
						L	1 0					632
						R	2.4					614

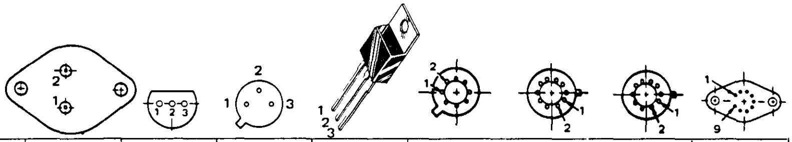
Special Regulators (continued)

LOW TEMPERATURE DRIFT, LOW VOLTAGE REFERENCE

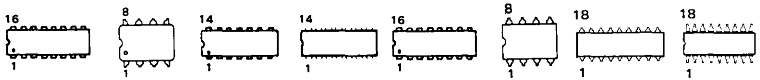
V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device Type	Suffix	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
2 5 ± 25 mV	10	40	MC1403	U	3/4 5 (Note 1)	10 (Note 3)	0 to +70	693
		25	MC1403A					
		55	MC1503				-55 to +125	
		25	MC1503A					
5 0 ± 50 mV		40	MC1404U5		6 0 (Note 2)		0 to +70	
		25	MC1404AU5					
		55	MC1504U5				-55 to +125	
		25	MC1504AU5					
6.25 ± 60 mV		40	MC1404U6				0 to +70	
		25	MC1404AU6					
		55	MC1504U6				-55 to +125	
		25	MC1504AU6					
10 ± 100 mV		40	MC1404U10				0 to +70	
		25	MC1404AU10					
		55	MC1504U10				-55 to +125	
		25	MC1504AU10					

Notes 1 $4\ 5 \leqslant V_I \leqslant 15\ V/15\ V \leqslant V_I \leqslant 40\ V$
2. $V_{in} = V_{out} + 2\ 5\ V$ to 40 V
3. $OmA < I_O < 10\ mA$

Package Styles



CASE	1 (TO-3)	29 (TO-92)	79 (TO-39)	221A (TO-220)	601	603 (TO-5 Type)	603C	614 (TO-66)
MATERIAL	Metal	Plastic	Metal	Plastic	Metal	Metal	Metal	Metal
SUFFIX	SK, K, KC	P, Z	G, H	T	G, H	G, H	G	R



CASE	620	626	632 (TO-116)	646	648	693	701	726
MATERIAL	Ceramic	Plastic	Ceramic	Plastic	Plastic	Ceramic	Ceramic	Plastic
SUFFIX	J, L	P or P1	L	P or P2	N, P	U	J	N

CIRCUITS FOR CONSUMER APPLICATIONS

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for Television, Audio, Radio, Citizens Band, Automotive and Organ applications.

Television Circuits

SOUND

Function	Features	Case	Type
Sound IF, Detector, Limiter, Audio Preamplifier	80 μV, 3 dB Limiting Sensitivity, 3.5 V (RMS) Output, Sufficient for Single Transistor Output Stage	646	MC1351
Sound IF Detector	Interchangeable with ULN2111A	646	MC1357
Sound IF Detector, dc Volume Control, Preamplifier	Excellent AMR, Interchangeable with CA3065	646	MC1358
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC} = 24$ V; $R_L = 16\ \Omega$	722A	TDA1190Z
	750 mW Output	648	TDA1190P

VIDEO

1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz = 60 dB typ, AGC Range = 70 dB min	626	MC1349
	IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min	626	MC1350
1st and 2nd Video IF, AGC Keyer and Amplifier	IF Gain @ 45 MHz = 53 dB typ, AGC Range = 75 dB min, "Forward AGC" Provided for Tuner	646	MC1352
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low-Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V	626	MC1330A1
	Same as MC1330A1 except zero signal dc output voltage of 7.8 to 9.0 V	626	MC1330A2
Automatic Fine Tuning	High Gain AFT System, Interchangeable with CA3064	646	MC1364
Automatic Fine Tuning with Intercarrier Mixer/Amplifier	AFT Circuit that Provides an AFT Voltage and an Amplified 4.5 MHz Intercarrier Sound Signal	646	CA3139

CHROMA

Chroma IF Amplifier and Subcarrier System	Includes Complete Chroma IF, AGC, dc Gain and Tint Controls Injection Locked Oscillator, Low Peripheral Parts Count	646	MC1398
Chroma IF Amplifier and Subcarrier System (PLL)	Includes Complete Chroma IF, AGC, dc Chroma and Hue Controls, Phase-Locked Loop (PLL) Oscillator, Color Killer Threshold Adjustment	648	MC1399
Dual Chroma Demodulators	Dual Doubly-Balanced Demodulator with RGB Matrix and Chroma Driver Stages	646	MC1324
	Dual Doubly-Balanced Demodulator with RGB Matrix and PAL Switch	646	MC1327
Triple Chroma Demodulator	Triple Doubly-Balanced Demodulator with Adjustable Output Matrix, Contains Three Independent Demodulators	648	MC1323

DEFLECTION

Horizontal Processor	Includes Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain	626	MC1391
	Same as MC1391 except designed to accept negative sawtooth sync pulse	626	MC1394
Vertical Processor	Includes Oscillator and Complementary Driver, Low Thermal Drift, Retrace Pulse for Effective Blanking	648	MC1393A

TV GAMES/DISPLAY

Color TV Video Modulator	Includes Chroma Oscillator and Clock Driver, Lead and Lag Network, Chroma Modulator, RF Oscillator, and Modulator.	646	MC1372
	Includes RF Oscillator and Modulator	626	MC1373

Audio Circuits

POWER AMPLIFIERS

Features	P_O Watts	V_{CC} Vdc Max	V_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Case	Type
Audio Power Amplifiers	0.5	15	3.0	4.0	8 0	626	MC1306
	0.25	12	3.0	3.0	16	626	MC3360
	8.0	28	50	55	2.0	314A, 314B	TDA2002

Radio Circuits

IF AMPLIFIERS

Function	Gain @ 10.7 MHz dB Typ	3 dB Limiting @ 10.7 MHz mV (RMS) typ	AMR dB Typ	Recovered Audio Output f = ±75 kHz mV (RMS)	Power Supply Volts Max	Case	Type
IF Amplifier	58	0.175	60	690	18	626	MC1350
Limiting FM-IF Amplifier	—	0.600	45	480	18	646	MC1355
Limiting IF Ampl/Quad Detector	53	0.4	45	480	16	646	MC1357
IF Amplifier	42	60	50	500	18	626	MC3310
Low-Power FM-IF for Dual Conversion Scanning Receivers	—	0.005	50	350 (f = ±3.0 kHz)	8.0	648	MC3357

DECODERS

Function	Channel Separation dB Typ	THD % Typ	Stereo—Indicator Lamp Driver mA Max	Features	Case	Type
FM Multiplex Stereo Decoder	47	0.06	50	Coilless Operation; 4.5 V Operation	646	MC1309
	40	0.3	75	Coilless Operation	646	MC1310
	45	0.2	100	Variable Separation	648	TCA4500A

AM RECEIVER

Features	Function	Case	Type
AM Radio Subsystem	RF Amplifier, AGC, Mixer, Oscillator, 1st IF Amplifier, 2nd IF Amplifier and Detector	648	HA1199

Organ Circuits

FREQUENCY DIVIDER

Function	V_{CC} Range Vdc	f_{Tog} MHz Typ	V_{OH} Vdc Min	Case	Type
7-Stage Divider	6-16	1.0	12.0/15.0	646	MC1302

ATTENUATOR

Function	V_{CC} Range Vdc	THD % Typ	A_V dB Typ	Attenuation Range dB Typ	Case	Type
Electronic Attenuator	9.0-18	0.6	13	90	626	MC3340

Automotive Circuits

OPERATIONAL AMPLIFIER

Function	V_{CC} Range Vdc	A_{VOl} V/V Min	I_{IB} μA Max	Unity Gain Bandwidth MHz Typ	Case	Type
Quad Operational Amplifier	4.0-28	1000	0.3	4.0	646	MC3301
	3.0-26	—	0.25	1.0	646	LM2902
Dual Operational Amplifier	3.0-26	—	0.25	1.0	626	LM2904

COMPARATORS

Function	V_{CC} Range Vdc	V_{IO} mV Max	I_{IO} nA Max	I_{IB} nA Max	Sink Current mA Typ	Case	Type
Quad Comparators	2.0-28	±20	—	500	6.0	646, 632	MC3302
	2.0-36	±7.0	±50	250	16.0	646	LM2901
		±5.0				646, 632	LM239
		±2.0				646, 632	LM239A

VOLTAGE REGULATOR

Function	Features	Case	Type
Automotive Voltage Regulator	Designed for use with NPN Darlington; Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field Alternator Charging System	646	MC3325
Flip-Chip Automotive Voltage Regulator	Same as MC3325	—	MCCF3326

ELECTRONIC IGNITION

Electronic Ignition Circuit	Designed for use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable	646	MC3333
Flip-Chip Electronic Ignition Circuit	Same as MC3333	—	MCCF3333

SPECIAL FUNCTION

Programmable Frequency Switch (Engine RPM Switch)	Wide Input Frequency Range (10 Hz to 100 kHz) Adjustable Hysteresis Wide Supply Operating Range (7 to 24 V)	646, 632	MC3344

Transistor Arrays

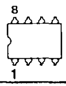
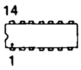
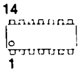
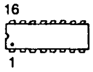
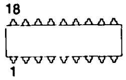
GENERAL-PURPOSE

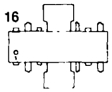
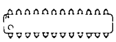
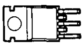
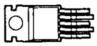
Function	I_C (max) mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Case	Type
One Differentially Connected pair and Three Isolated Transistors	50	15	20	5.0	646	MC3346 MC3386
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	646	CA3054

Special Functions

Function	Features	Case	Type
Emitter-Coupled Astable Multivibrator	Useful as DC-DC Converter, Power Regulator or Multivibrator. Toggle Freq = 100 kHz (typ)	626	MC3380
Phase-Locked Loop	Contains Voltage Controlled Oscillator and Double Balanced Phase Detector	646	NE565

Package Styles

Lead Configuration					
Case	626	632	646	648	701
Material	Plastic	Ceramic	Plastic	Plastic	Plastic
Suffix after Type Number	P or PL	L	P	P	P

Lead Configuration				
Case	722A	724	314A	314B
Material	Plastic	Plastic	Plastic	Plastic
Suffix after Type Number	P	P	H	V

SPECIAL PURPOSE CIRCUITS

The linear-integrated-circuits listed in this section were developed by Motorola for the system design engineer to fill special-purpose requirements. Temperature ranges and package availability are tailored to provide price/performance versatility.

Linear Four-Quadrant Multipliers

MC1594/1494

This device is designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/MC1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

MC1595/MC1495

Similar to the MC1594/1494, but without internal level shift and voltage regulator circuits.

Balanced Modulator-Demodulator

MC1596/MC1496

Designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection and chopper applications.

Timing Circuits

MC1555/MC1455/MC1422

These devices are highly stable timing circuits capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits. Timing from Microseconds through Hours. The MC1422 has variable threshold level, adjustable externally.

	Timing Error (typ)
MC1555	0.5%
MC1455	1.0%
MC1422	1.0%

MC3556/MC3456

Dual Version of the MC1555/MC1455

Low Frequency Power Amplifier

MC1554/MC1454

One-watt power amplifier for single or split supply operation. Typical voltage gain of 10, 18, or 36 V/V with 0.4% THD.

Power Control Circuits

MC3370

Electronic switch for triac triggering applications. Features zero-crossing detector to eliminate RFI, differential input with dual sensor inputs, input open and short protection, and built-in regulator permitting AC line operation.

CA3059/3079

Zero voltage switches designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz.

Monolithic Dual OP Amp and Dual Comparator

MC3505/MC3405

This device contains two differential input operational amplifiers and two comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block".

- Op Amp Equivalent in Performance to MC3403
- Comparator Similar in Performance to LM339
- Op Amps are Internally Frequency Compensated
- Supply Operation 3.0 Volts to 36.0 Volts
- Dual Supply Operation also Available

Package Styles

Operating Temperature Range		
-55 to +125°C	**0 to +70°C**	**Case**
MC1554	MC1454	603B
MC1555		601, 693
	MC1455	601, 626, 693
MC1594	MC1494	620
MC1595	MC1495	632
MC1596		603, 632
	MC1496	603, 632, 646
	MC1422	601, 626
MC3505		632
	MC3405	632, 646
MC3523		693
	MC3423	626, 693
MC3556		632
	MC3456	632, 646
	MC3370	626
	CA3059* CA3079*	646

*-40 to +85°C

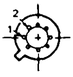
Overvoltage Protection Circuit

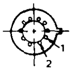
MC3523/MC3423

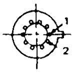
OVPs protect sensitive circuitry from transients or regulator failures when used with an external "crowbar" SCR. They sense the overvoltage and quickly "crowbar" or short circuit the supply, forcing it into current limiting or opening fuse or CB.

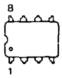
Voltage threshold is adjustable and OVPs can be programmed for minimum duration before tripping, supplying noise immunity.

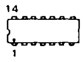
I_O ±mA	V_{CC} Volts		V_{Sense} Volts					
Max	Min	Max	Min	Max	Device Number	Suffix	T_A °C	Case
300	4.5	40	2.45	2.75	MC3423	P	0 to +70	626
						U	0 to +70	693
					MC3523	U	-55 to +125	693

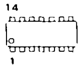


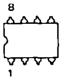












CASE	601	603	603B	626	632	646	693
MATERIAL	Metal	Metal	Metal	Plastic	Ceramic	Plastic	Ceramic
SUFFIX after type number	G	G	G	P or P1	L	P	U

HIGH FREQUENCY AMPLIFIERS

A variety of high-frequency circuits with features ranging from low-cost simplicity to multi-function versatility marks Motorola's line of integrated RF/IF amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see "Circuits for Consumer Applications".

NON-AGC Amplifiers

SE/NE592 – Differential Two Stage Video Amplifier

A monolithic, two state differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C – Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 v/v. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

MC1552/MC1553 – Low Distortion Amplifier

A high performance amplifier with internal series feedback for stable voltage gain and low distortion. Temperature compensation stabilizes operating point. Has selectable gain option and well characterized data that permits accurate response shaping. Useful for critical applications such as wideband linear amplifiers or fast-rise pulse amplifiers.

AGC Amplifiers

MC1550 – Low Cost Building Block

Single-stage cascade connected amplifier with delayed AGC characteristics, for operation at frequencies to 100 MHz. Has typical power gain of 25 dB @ 60 MHz.

MC1545/MC1445 – Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 75 MHz bandwidth makes it suitable for high-frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

MC1590 – Wide-Band General Purpose

Has differential inputs and outputs with unneutralized power gain as high as 35 dB typical at 100 MHz in tuned amplifier service. Effective AGC voltage range from 5 to 7 volts for a 30 dB gain reduction.

Electrical Specifications

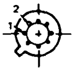
AGC AMPLIFIERS

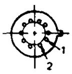
Operating Temperature Range					
-55 to +125°C	0 to +75°C	A_V dB	Band width MHz	V_{CC}/ V_{EE} Vdc	Case
MC1550	–	22 Min	22	+6/-	603B,606
MC1590	–	44 Typ @ 4 Typ @	10 100	+12/-	601
MC1545	MC1445	19 Typ @	75	+5/-5	603,607 632

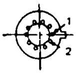
NON AGC AMPLIFIERS

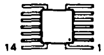
MC1733	MC1733C	52 @ 40 20	40 90 120	+6/-6	603,632
MC1553	–	46 @ 52	35 15	+6/-6	603B
MC1552	–	34 @ 40 @	40 35	+6/-6	603B
SE592	NE592	55 @ 45 @	40 90	+6/-6	603,632

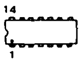
Package Styles



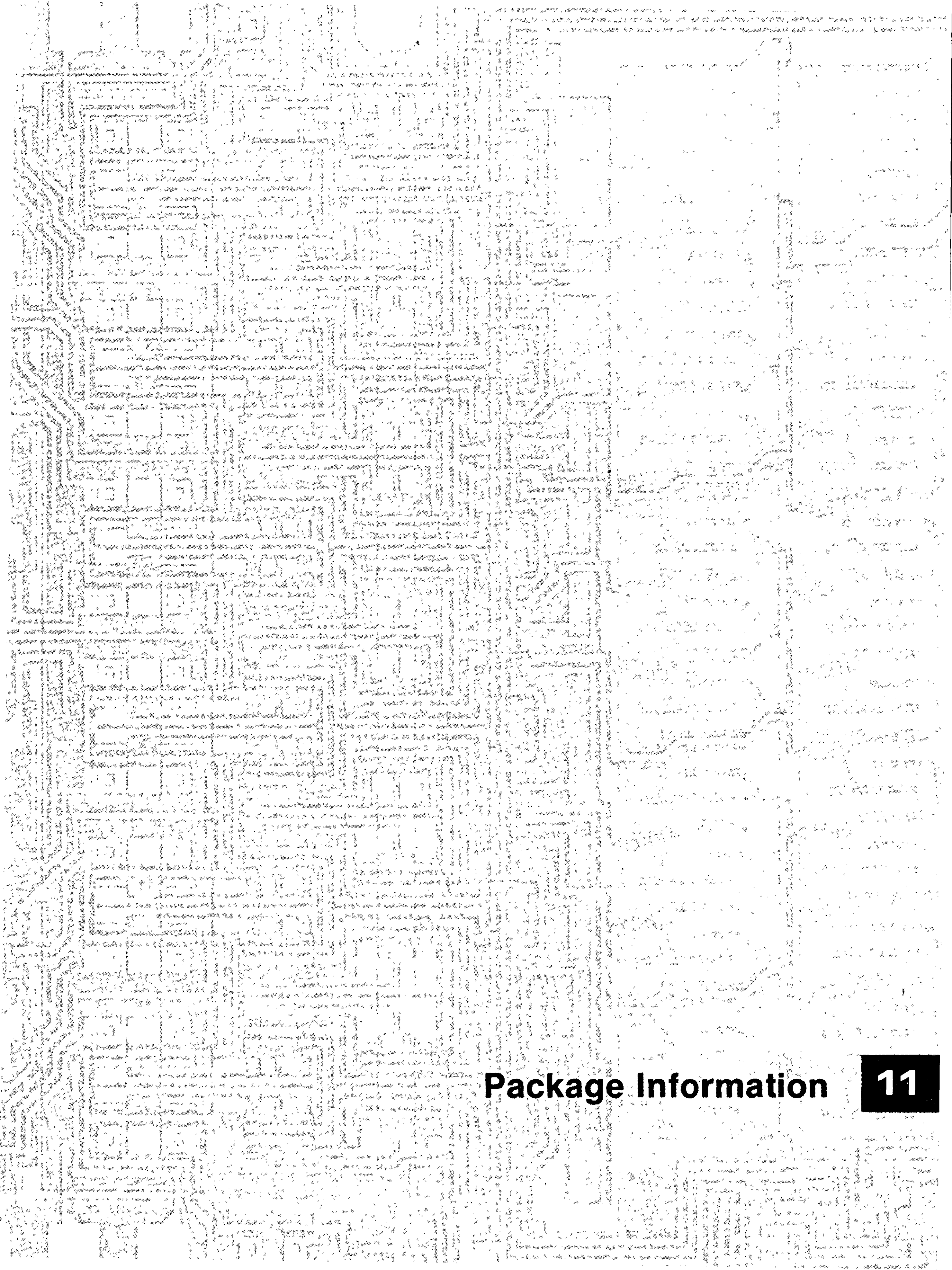








CASE	601	603	603B	606	607	632
MATERIAL	Metal	Metal	Metal	Ceramic	Ceramic	Ceramic
SUFFIX after type number	G	G	G	F	F	L



Package Information

11

CASE OUTLINE DIMENSIONS

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section. Outline dimensions for non-encapsulated standard linear device chips and flip-chip devices are found in the Chips Data Book.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

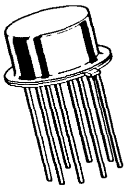
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

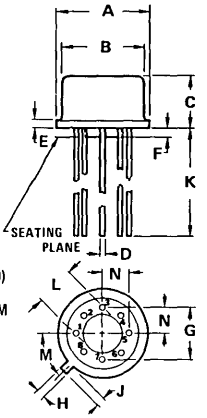
T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

CASE 601-04

Metal Package



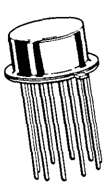


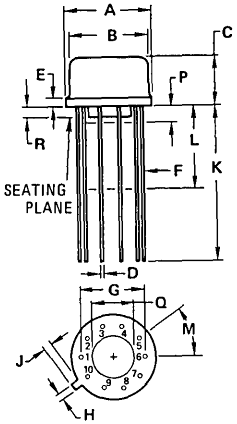
NOTE:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0 41	0.48	0.016	0 019
E	0.25	1.02	0.010	0.040
F	0 25	1.02	0 010	0.040
G	5 08 BSC		0.200 BSC	
H	0.71	0.86	0 028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0 500	–
L	3 05	4.06	0.120	0.160
M	45⁰ BSC		45⁰ BSC	
N	2.41	2.67	0.095	0 105

CASE 603-04

Metal Package





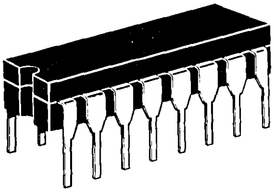
NOTE·
LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

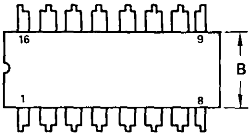
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8 51	9.39	0 335	0 370
B	7.75	8.51	0.305	0 335
C	4 19	4 70	0 165	0.185
D	0 407	0.533	0 016	0 021
E	–	1.02	–	0 040
F	0 406	0.483	0 016	0 019
G	5 84 BSC		0 230 BSC	
H	0 712	0.864	0.028	0 034
J	0.737	1.14	0.029	0 045
K	12.70	–	0.500	–
L	6 35	12 70	0.250	0.500
M	36⁰ BSC		36⁰ BSC	
P	–	1.27	–	0 050
Q	3.56	4.06	0.140	0 160
R	0.254	1.02	0 010	0.040

All JEDEC dimensions and notes apply

CASE 620-02

Ceramic Package

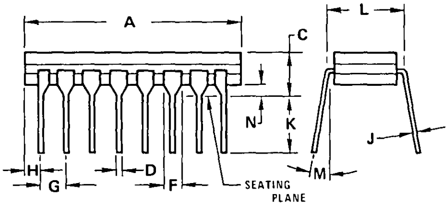




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19 05	19 81	0.750	0 780
B	6.22	6 98	0.245	0.275
C	4.06	5 08	0.160	0 200
D	0.38	0 51	0.015	0.020
F	1.40	1 65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0 51	1.14	0.020	0 045
J	0.20	0 30	0.008	0 012
K	3.18	4.06	0.125	0.160
L	7 37	7 87	0.290	0 310
M	–	15°	–	15°
N	0.51	1.02	0.020	0 040

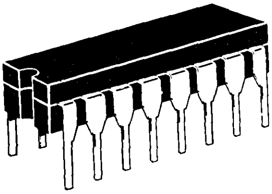
NOTES.

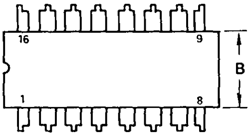
1. LEADS WITHIN 0.13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX. NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



CASE 620-06

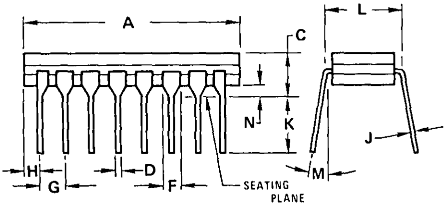
Ceramic Package





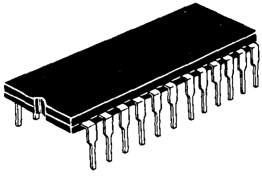
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6 10	7 49	0 240	0.295
C	–	5 08	–	0 200
D	0.38	0 53	0 015	0.021
F	1.40	1.78	0 055	0 070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0 045
J	0 20	0.30	0 008	0 012
K	3.18	5 08	0 125	0 200
L	7 62 BSC		0 300 BSC	
M	–	15°	–	15°
N	0 51	1 02	0 020	0 040

1. LEADS WITHIN 0.13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0 76 mm (0 030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

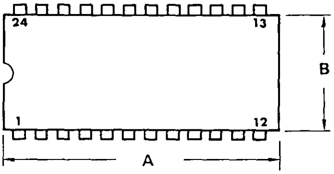


CASE 623-04

Ceramic Package

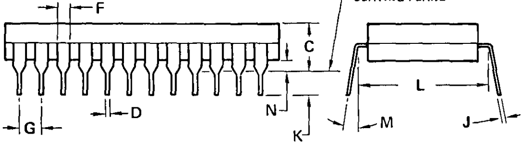


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31 24	32.77	1.230	1.290
B	12.70	15 49	0.500	0 610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050



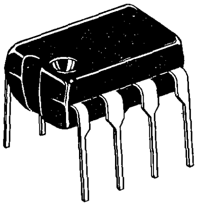
NOTES:

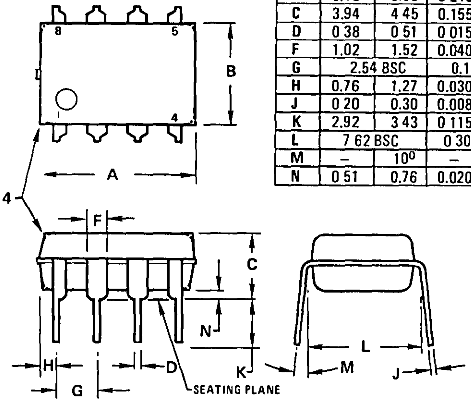
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL)



CASE 626-04

Plastic Package



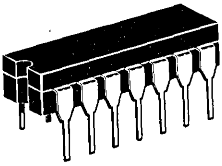


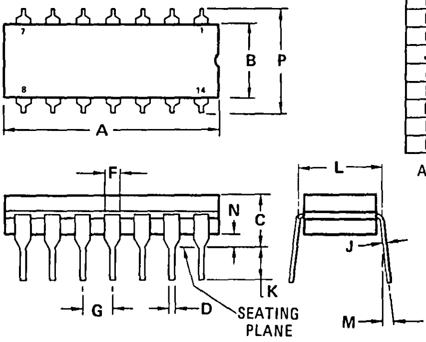
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9 40	10.16	0 370	0.400
B	6.10	6.60	0 240	0.260
C	3.94	4 45	0.155	0.175
D	0 38	0 51	0 015	0.020
F	1.02	1.52	0.040	0 060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0 050
J	0 20	0.30	0.008	0.012
K	2.92	3 43	0 115	0.135
L	7 62 BSC		0 300 BSC	
M	–	10^0	–	10^0
N	0 51	0.76	0.020	0.030

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

CASE 632-02

Ceramic Package





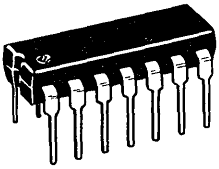
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5 08	–	0 200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0 030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0 51	0.76	0.020	0.030
P	–	8.25	–	0.325

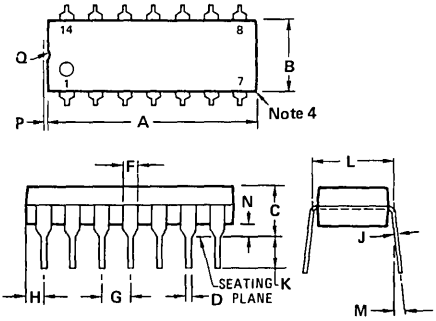
All JEDEC dimensions and notes apply.

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

CASE 646-05

Plastic Package



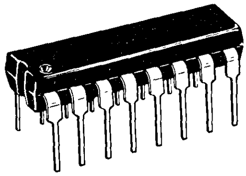


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6 60	0 240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2 41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0 115	0 135
L	7.62 BSC		0 300 BSC	
M	0^0	10^0	0^0	10^0
N	0 51	1.02	0.020	0 040

NOTES·
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH
4 ROUNDED CORNERS OPTIONAL

CASE 648-05

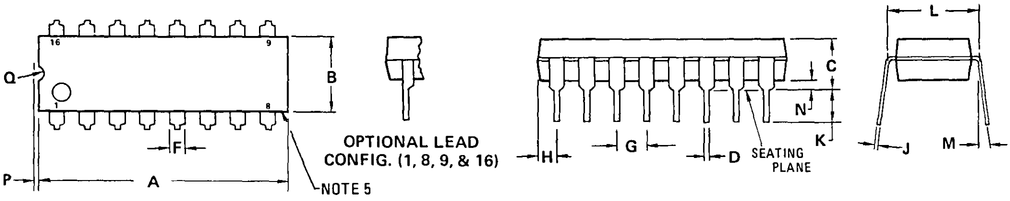
Plastic Package



NOTES:

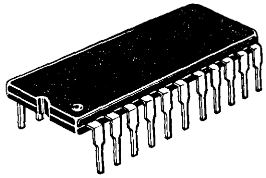
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0 070
G	2 54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0 38	0 008	0 015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040



CASE 649-03

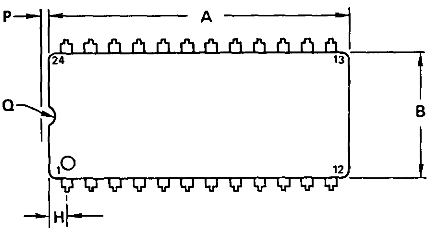
Plastic Package

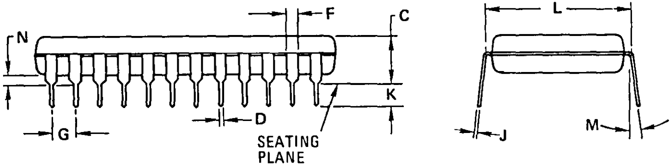


NOTES.

1. LEADS WITHIN 0.13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

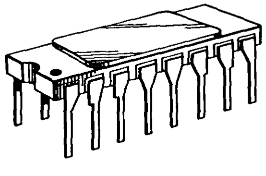
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31 50	32.13	1 240	1.265
B	13 21	13.72	0 520	0 540
C	4 70	5 21	0.185	0 205
D	0.38	0.51	0 015	0.020
F	1 02	1 52	0.040	0 060
G	2 54 BSC		0.100 BSC	
H	1.65	2 16	0.065	0 085
J	0.20	0 30	0.008	0.012
K	2 92	3.43	0 115	0 135
L	14.99	15 49	0.590	0.610
M	–	10°	–	10°
N	0 51	1 02	0 020	0.040
P	0 13	0.38	0.005	0.015
Q	0 51	0.76	0.020	0 030



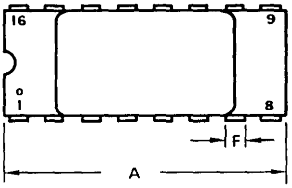


CASE 690-12

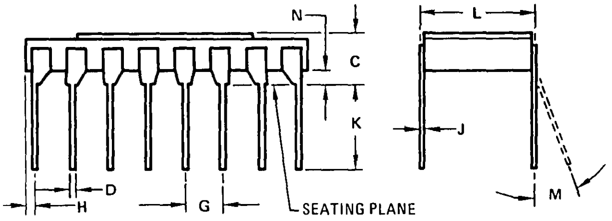
Ceramic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20 07	20 57	0 790	0 810
B	7.11	7 62	0 280	0 300
C	2 67	3 94	0 105	0 155
D	0.38	0.53	0 015	0.021
F	0.76	1 40	0 030	0.055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 30	0 008	0.012
K	3 18	5 08	0.125	0.200
L	7 62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0 38	1 40	0 015	0.055

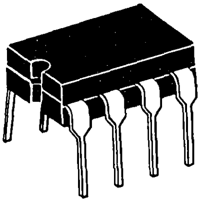


1. LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION, AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

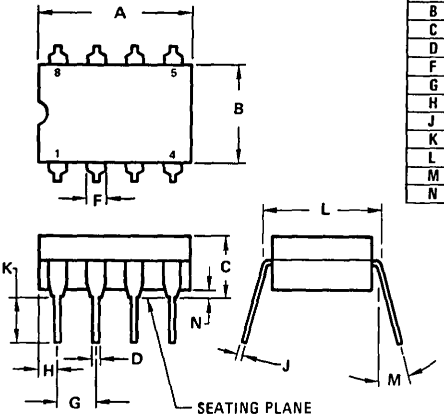


CASE 693-02

Ceramic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10 92	0.390	0 430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7 87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0 020	0 040

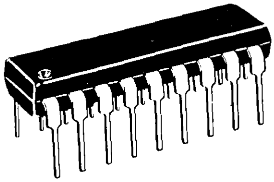


NOTES

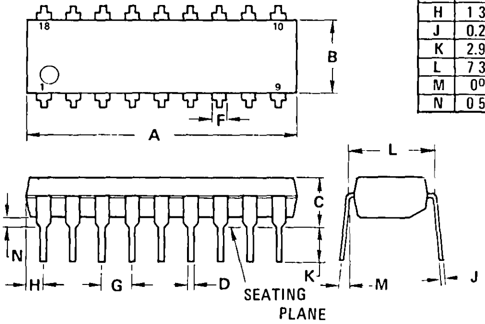
1. LEADS WITHIN 0.13 mm (0 005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 701-01

Plastic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23 11	23 88	0 910	0 940
B	6 10	6 60	0 240	0 260
C	4 06	4 57	0 160	0 180
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 32	1 83	0 052	0 072
J	0.20	0 30	0 008	0 012
K	2.92	3 43	0 115	0 135
L	7 37	7 87	0 290	0 310
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

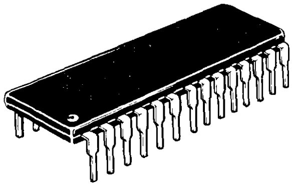


NOTES:

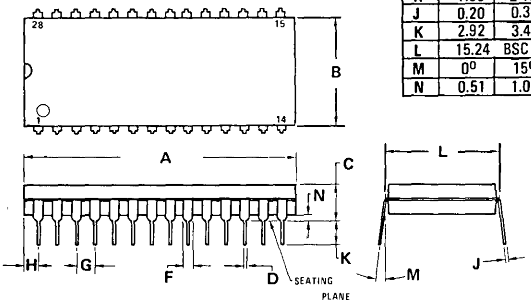
1. LEADS WITHIN 0.13 mm (0 005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 710-02

Plastic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13 72	14 22	0 540	0.560
C	3.94	5 08	0.155	0 200
D	0 36	0.56	0.014	0.022
F	1.02	1.52	0 040	0 060
G	2.54 BSC		0.100 BSC	
H	1.65	2 16	0 065	0 085
J	0.20	0.38	0 008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040



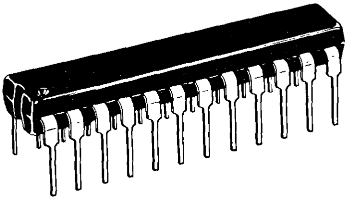
NOTES:

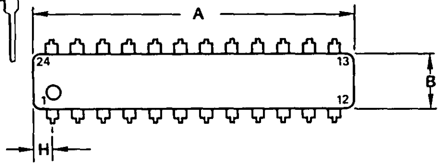
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 724-02

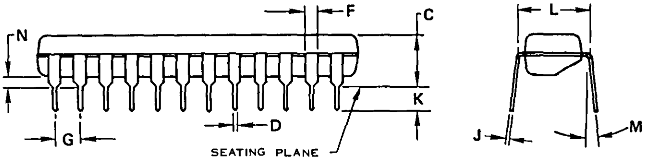
Plastic Package

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040





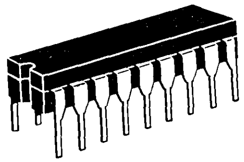
NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

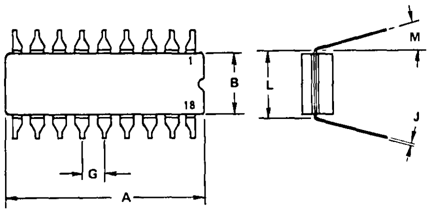


CASE 726-01

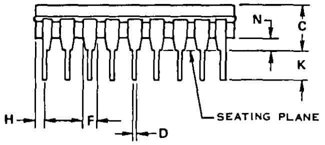
Ceramic Package

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0 910
B	6.63	7.24	0 261	0.285
C	–	5 08	–	0 200
D	0.41	0 51	0 016	0 020
F	1.40	1 65	0 055	0 065
G	2.54 BSC		0.100 BSC	
H	0 76	1 02	0.030	0 040
J	0 13	0.38	0.005	0 015
K	–	4 44	–	0.175
L	7.37	8.00	0 290	0 315
M	0°	15°	0°	15°
N	0 51	0.76	0.020	0 030





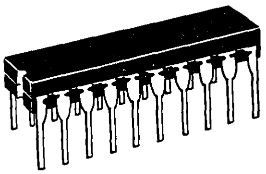
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

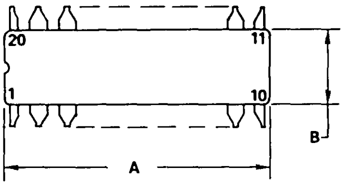


CASE 732-02

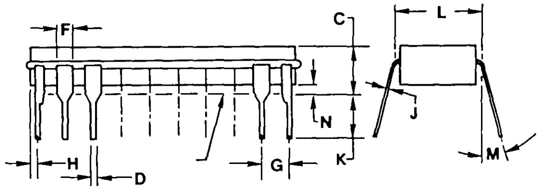
Ceramic Package

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6 86	7 49	0 270	0.295
C	4.32	5 08	0.170	0.200
D	0 38	0 56	0 015	0.022
F	1.40	1.65	0 055	0.065
G	2.54 BSC		0 100 BSC	
H	0.89	1.40	0 035	0.055
J	0.20	0.30	0 008	0 012
K	3 18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030



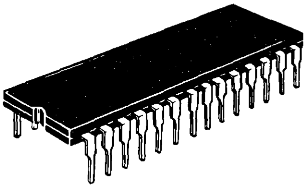


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.



CASE 733-02

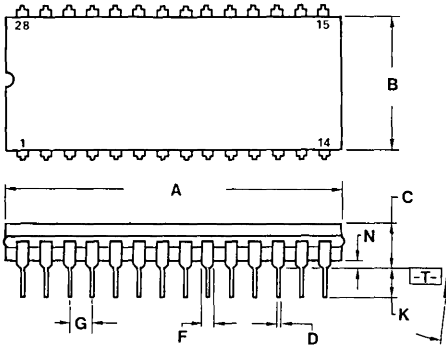
Ceramic Package

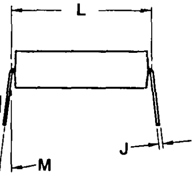


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36 45	37.85	1.435	1 490
B	12.70	15.37	0.500	0.605
C	4 06	5.84	0.160	0.230
D	0.38	0.56	0.015	0 022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0 30	0 008	0.012
K	2.54	4.06	0.100	0.160
L	15.24 BSC		0 600 BSC	
M	5°	15°	5°	15°
N	0.51	1 27	0 020	0 050

NOTES:

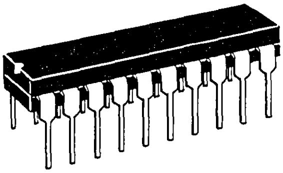
1. DIM -A- IS DATUM
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0 25 (0 010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14 5, 1973.



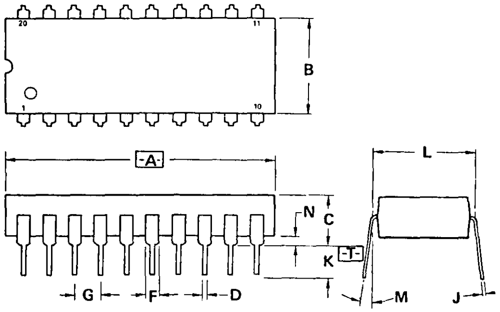


CASE 738-01

Plastic Package

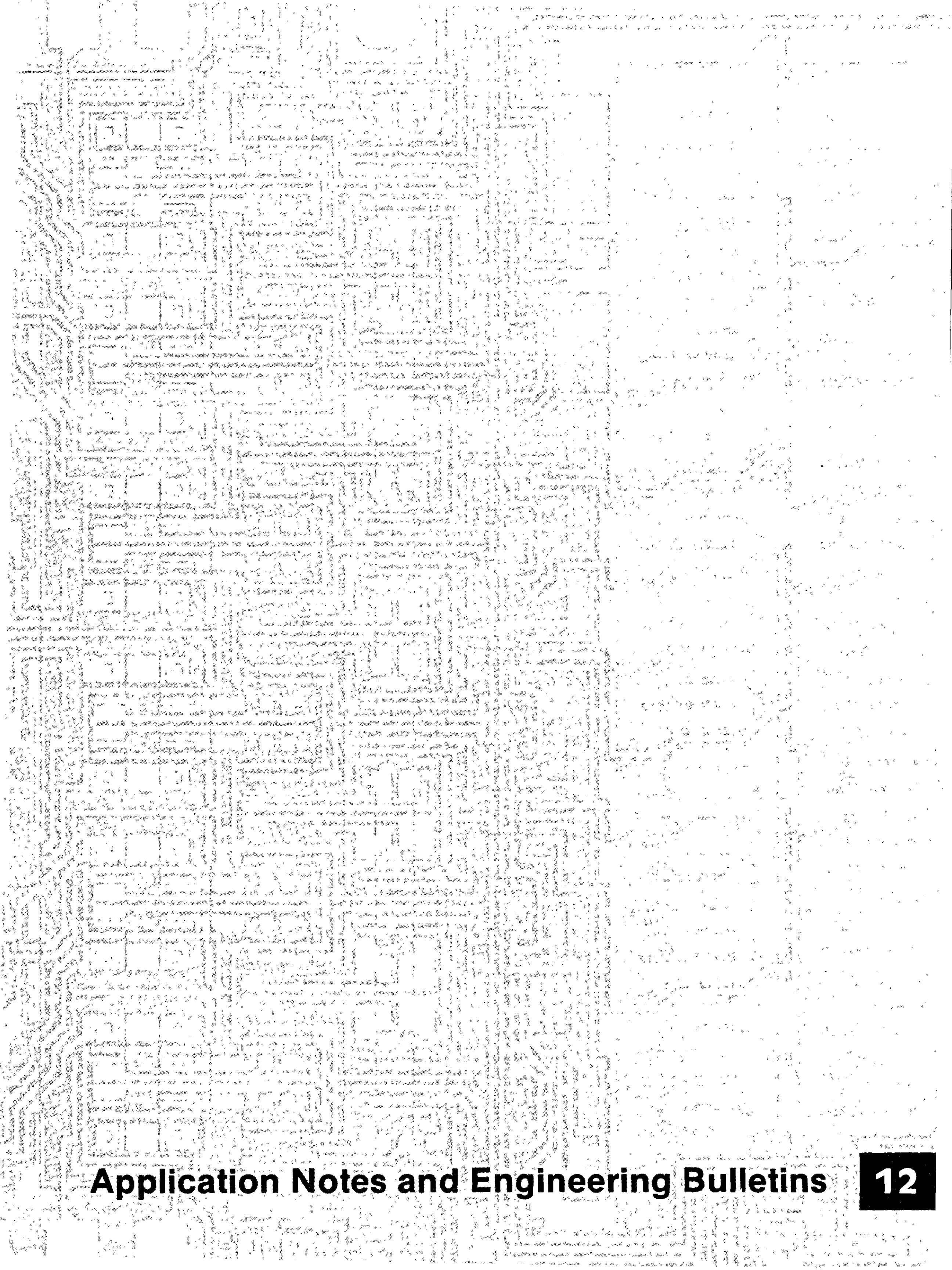


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25 65	27.18	1 010	1 070
B	6 10	6 60	0.240	0 260
C	3.94	4.19	0.155	0.165
D	0 38	0 56	0 015	0 022
F	1.27	1.78	0.050	0 070
G	2.54 BSC		0.100 BSC	
J	0.20	0 38	0.008	0 015
K	2.79	3.56	0.110	0.140
L	7 62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1 02	0 020	0 040



NOTES.

1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS,
   ⌖ | Ø 0.25 (0 010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



Application Notes and Engineering Bulletins

12

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-245A An Integrated Core Memory Sense Amplifier

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max), adjustable voltage gain, and fast cycle time (0.5 μs).

AN-273A More Value out of Integrated Operational Amplifier Data Sheets

The operational amplifier is rapidly becoming a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also, each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset circuits are also reviewed with respect to closed loop operation.

AN-290B Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices

Many Motorola power devices are now available in the Plastic Thermopad packages. Three package types are presently available. This application note provides information concerning the handling and mounting of these packages, as well as information on some thermal aspects.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including DC characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of AC and DC operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete AC and DC circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications Using The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This application note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductors for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543A Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multibvibrators, and peak level detectors are presented.

AN-553 A New Generation of Integrated Avionic Synthesizers

The need to generate signals of a multitude of different frequencies for avionic systems has resulted in complex solutions in the past. With the introduction of certain standard product integrated circuits, frequency synthesis using digital phase locked loop techniques presents a more practical solution. Several different types of servo phase locked loop systems are discussed and a practical design example is given. Results of design examples are presented along with possible applications.

AN-557 Analog-to-Digital Cyclic Converter

The A/D cyclic converter discussed in this note provides medium speed (1-5μs/ bit) and medium accuracy (7 or 8 bits) operation. A Cyclic converter uses the successive approximation technique in which an unknown analog input voltage is successively compared to a reference voltage to determine each bit of the digital output.

The cyclic converter offers continuous operation, automatic generation of the digital output in Gray-code form, and a building block structure. This structure uses a separate but identical circuit for each resolution bit. The cyclic converter finds use primarily in control and process applications.

AN-559 Simple Ramp A/D Converter

A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part—the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

AN-564 An ADF Frequency Synthesizer Utilizing Phase-Locked Loop Integrated Circuits

This application note describes an IC phase locked-loop frequency synthesizer suitable for the local oscillator function in aircraft Automatic Direction Finder (ADF) equipment.

AN-587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN-590 Servo Motor Drive Amplifiers

The design of transformerless, AC servo amplifiers using power darlington transistors and IC op amps are discussed. Two types of power amplifiers are illustrated, one using single +28 Volt power supply, the second using high voltage transistors in complementary configuration for operating directly off the line.

Four different op amp preamplifiers and 90° phase shifters are also described.

AN-599 Mounting Techniques for Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

AN-702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN-703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

AN-708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

AN-710 Communication System Transmission Losses

This report shows the derivation of the equations used to calculate the insertion loss associated with various component parts of a communications channel. The combinations of components form a system whose overall loss may not be equal to the sum of the losses of the various parts.

AN-711 The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems

The use of magnetic recording techniques has long been an important means of sorting digital information, as evidenced by the wide variety of equipment currently in use. Representative systems utilize drums, disks and tape as the recording medium.

All three techniques share the common problem of recovering the recorded digital information. The analog signal obtained by passing the recording medium by a magnetic sensor (Read Head) must be converted to a suitable digital format.

This application note reviews the general problem and discusses a number of specific circuit approaches.

AN-713 Binary D/A Converters can Provide BCD-Coded Conversion

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

AN-714 A Personalized Heart-Rate Monitor with Ditigal Readout

Using the micropower operational amplifier MC1776 and CMOS digital integrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-716 Successive Approximation A/D Conversion

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

AN-717 Battery Powered 5-MHz Frequency Counter

This application note describes a battery-powered 5-MHz frequency counter using the McMOS logic family for low-power operation. The basic counter is optimized, at a 12-volt supply for maximum performance with a linear input-signal conditioner. Several options are discussed which optimize the basic counter for minimum power dissipation. These options include a CMOS input signal-conditioner and multiplexed LED displays.

AN-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-720 Interfacing with MECL 10,000

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as; input impedance, output drive, gain and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling of non-compatible signals.

AN-732A A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs

NMOS semiconductor technology has made inroads into high density/high performance circuit design. The one-chip microprocessor, Random Access Memories, and Read Only Memories, are changing system implementation from random logic designs to software and firmware programmable microcomputing systems. Such systems frequently require relatively large amounts of memory.

This paper describes the design of an 8192-byte non-volatile Random Access Memory system using the MCM6605A 4Kx1 RAM. The syste is designed to work with the Motorola MC6800, an 8-bit microprocessor.

AN-737A Switched Mode Power Supplies—Highlighting A 5-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

AN-739 A Synthetic Spectrum Tuning System for TV

A tuning system is described which uses a complete spectrum of TV channel markers to achieve precise tuning to any channel.

AN-741 Interface Considerations for Numeric Display Systems

This application note describes several methods of multiplexing multi-digit, seven-segment displays. The logic devices illustrated are primarily CMOS with two examples describing TTL. The displays discussed are liquid crystal, LED, gas discharge, incandescent and fluorescent. How to interface between the logic and these displays, and what the interface considerations are, are described in detail.

AN-744 A Phase-Locked Loop Tuning System for Television

This note describes a frequency domain tuning system which utilizes direct digital countdown of the varactor tuner's local oscillator to obtain the proper local oscillator frequency for the channel number selected. The system features direct-channel access with equal ease of tuning and an exact channel readout for all VHF and UHF channels.

AN-746 A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System

This application note describes the design of a 3½-digit DVM (digital voltmeter) using the MC1405 and the MC14435 dual ramp A/D system. The performance criteria is that of a lab quality DVM with both 3½-digit resolution and accuracy while still retaining a low cost and low parts count instrument. Features of the DVM include circuitry for a high impedance input, autopolarity and overrange indication.

AN-751 A Disassociated Intercarrier Television Video IF Amplifier

This application note discusses a unique video IF system, incorporating the MC1331, low-level multiplier detector. Problem areas in IF design are discussed and the specific solutions are shown.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a ferroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-757 Analog-to-Digital Conversion Techniques with the MC6800 Microprocessor System

This application note describes several analog-to-digital conversion systems implemented with the M6800 microprocessor and external linear and digital IC's. Systems consisting of an 8- and 10-bit successive approximation approach, as well as dual ramp techniques of 3½-and 4½digit BCD and 12-bit binary, are shown with flow diagrams, source programs and hardware schematics. System tradeoffs of the various schemes and programs for binary-to-BCD and BCD-to-7 segment code are discussed.

AN-760 Application of The MC3416 Crosspoint Switch

The operation and application of the MC3416 4 x 4 balanced crosspoint switch is described in detail. Special emphasis is given to balanced switching systems like those in space division PABX. Discussion of the total system design using the MC3416 is also included.

AN-763 The MC1323—A Fully Programmable Demodulator

The MC1323 is a monolithic integrated circuit demodulator specifically designed for decoding the NTSC color television signal, even when non-standard receiver display tube phosphor primaries are used. The unique design allows independent adjustment of demodulator conversion gains and demodulation axes. This note describes the circuit operation of the MC1323 and several applications including low cost driving of unitized gun picture tubes and obtaining R-G-B demodulated outputs.

AN-765 An Approach To A Low-Noise TV IF System

This note describes a technique of measurement of the IF contribution and ways of minimization of the IF noise. An IF design, following these procedures, is described to meet the desired noise performance.

AN-767 A Line Operated, Regulated 5V/50A Switching Power Supply

This application note describes a regulated 220 V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

AN-775 M6800 Systems Utilizing the MC6875 Clock Generator/Driver

This application note describes the use of the MC6875 clock generator/driver in M6800 based systems. Design examples will demonstrate the capabilities of the driver in systems using slow and/or dynamic memories. Multiprocessing and DMA methods are also covered.

AN-781 Revised Data-Interface Standards

Revised data-interface standards permit faster data rates and longer cables. New chips, and RS232 adapters, simplify their use.

AN-787 An M6800 Clock System That Handles DMA and Memory Refresh Cycle Stealing

Dynamic memory and three-state cycle stealing for Direct Memory Access transfers require a clock generator and priority logic to maintain proper refresh times of the dynamic MPU and dynamic memory. The design presented here demonstrates use of the MC6875 clock generator with an MC6800 MPU.

ENGINEERING BULLETIN ABSTRACTS

EB-20 Multiplier/Op Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described by EB-20 to obtain the true rms of an input voltage ranging from 2 to 10 Vpk.

EB-21 DAC Key To Inexpensive 2⅔ Digit Voltmeter.

EB-21 presents an idea for the core of an economical 2⅔ digit voltmeter. Built around Motorola's MC1408 8-bit D/A converter, the meter can measure to 2.55 V in 10 mV steps.

EB-24A Input Buffer Circuits For The MC1505 Dual Ramp A-To-D Converter Subsystem

Several bipolar op amp buffers of medium-high impedance are described in this bulletin. It also discusses FET input op amp buffers providing high impedance and temperature drift under 1 mV over the 0°C to 50°C range.

EB-50 Build This Simple, Battery-Powered 3½ Digit DVM From Standard Parts

EB-50 describes a simple, battery-powered 3½ digit DVM capable of measuring up to 20 volts that can be built from readily obtained standard parts. Sufficient information is provided to construct the circuit including schematic, PC board layout, parts list and calibration instructions.

EB-51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB-51.

EB-52 Control Your Switching Regulator With The MC3380 Astable Multivibrator

Engineering Bulletin EB-52 describes the operation and characteristics of the MC3380 astable multivibrator and details the design of a 200 volt switching regulator circuit for gas discharge displays using this device as the control element.

EB-57 An Economical FM Transmitter Voice Processor from a Single IC

An MC3401 Quad OP-Amp is used as a Microphone/Modulation interface in an FM transmitter.

EB-58 Analog Data Acquisition Network for Digital Processing Using the MC1405-MC14435 A/D System

An MC1405-MC14435 combination is used to form a dual-slope A/D converter for analog data acquisition.

EB-66 A Symmetry Correcting Circuit for Use with the MC3420

EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

EB-78 NEW ICs In Switching Supplies

This bulletin describes a regulated 220 Vac to 5 Vdc converter design incorporating the MC3420 and MC3423 for the control and ancillary functions.

EB-85 Full-Bridge Switching Power Supplies

This bulletin provides selection information on devices for a full-bridge configuration supply in the 500-1000 watt power range.

EB-86 Half-Bridge Switching Power Supplies

This bulletin provides selection information on devices for a half-bridge configuration supply in the 100-500 watt power range.

EB-87 Flyback Switching Power Supplies

This bulletin provides selection information on devices for a flyback configuration supply in the 100-250 watt power range.

EB-88 Push-Pull Switching Power Supplies

This bulletin provides selection information on devices for a push-pull configuration supply in the 100-500 watt power range.

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