

ASSP

IF Band PLL Frequency Synthesizer MB15S02

■ DESCRIPTION

The Fujitsu MB15S02 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

RF synthesizer block of digital cellular phones can be realized easily as well as compactly with MB15S02 and MB15A16 (1.2 GHz; SSOP-16), which is Fujitsu's standard product developed for digital cellular phones.

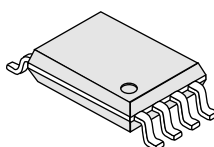
The MB15S02 is ideally suitable for GSM systems.

■ FEATURES

- Prescaler operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. ($V_{CC} = 3V$)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
 - $f_{osc} = 13.0MHz$, $f_{IF} = 284.0MHz$ (Div = "H")
 - $f_{osc} = 13.0MHz$, $f_{IF} = 116.0MHz$ (Div = "L")
- Rapid synchronization at powering up
Fujitsu's original charge pump "super charger circuit" is included, that enables rapid synchronization at powering up.
- Lock detector
- Low power supply voltage: $V_{CC} = 2.7$ to $3.6V$
- Wide operating temperature: $T_a = -40$ to $85^{\circ}C$
- Plastic 8-pin SSOP packages

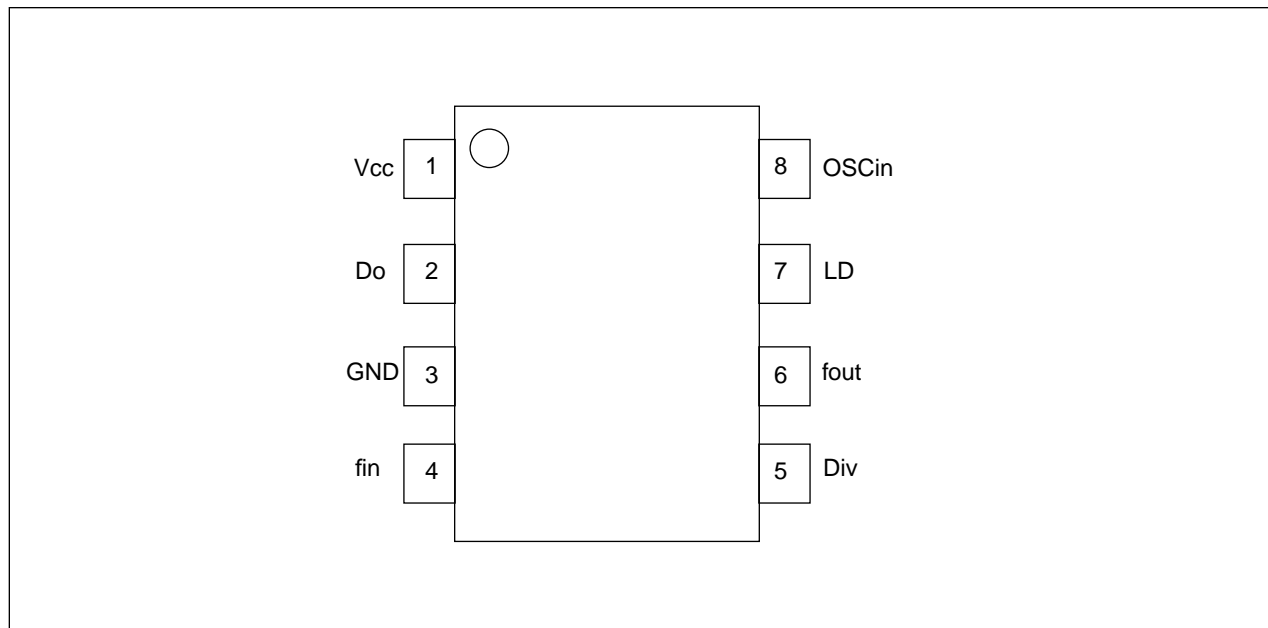
■ PACKAGE

8-pin, Plastic SSOP



(FPT-8P-M03)

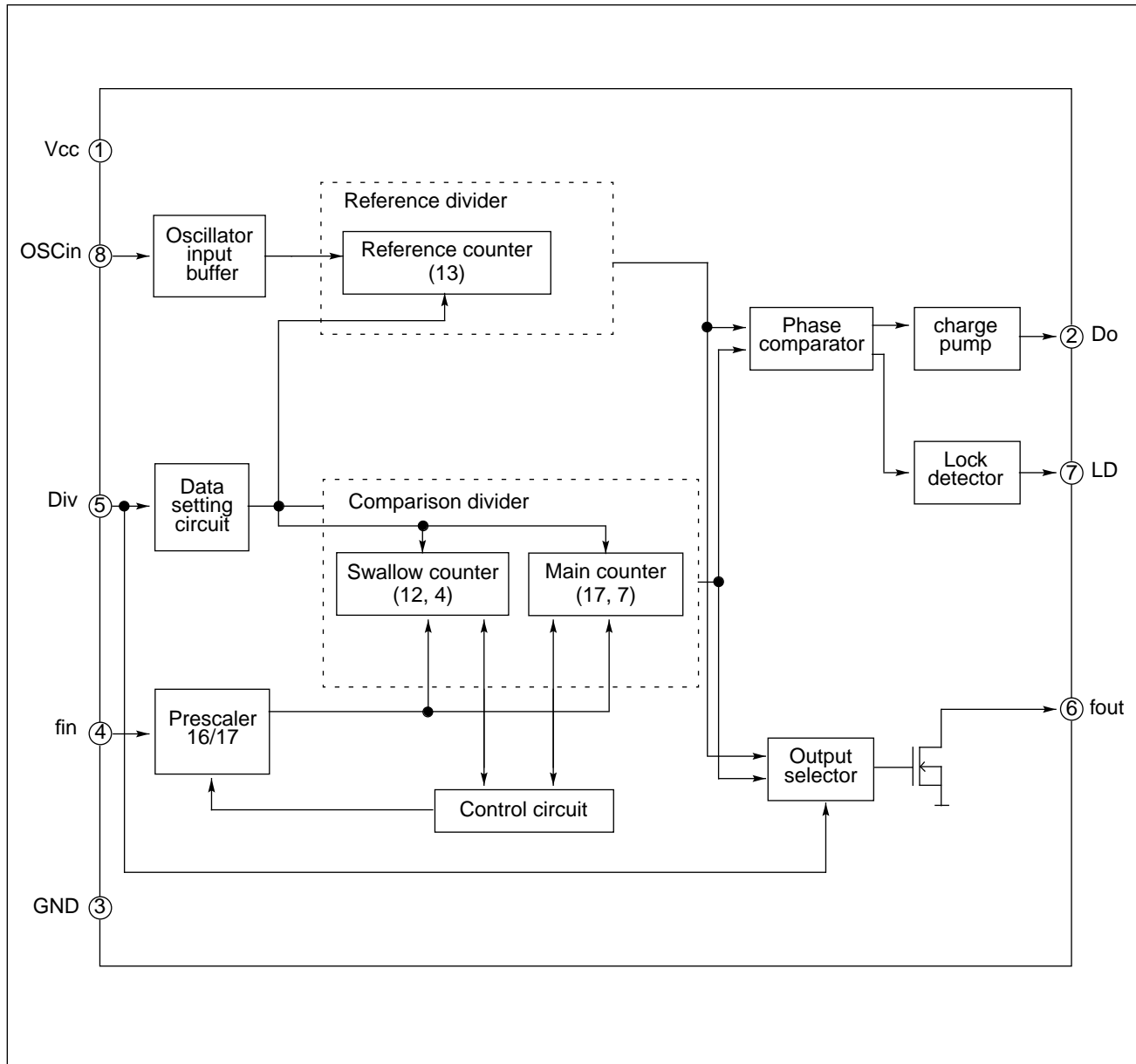
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	V _{CC}	Power supply voltage input (2.7V to 3.6V).
2	D _O	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to +5.0	V
Input voltage	V_I	−0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	−0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	0 to 5	mA
Storage temperature	T_{STG}	−55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	T_a	−40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC}	PLL is locked. $V_{CC} = 3.0V$, $T_a = 25^{\circ}C$	–	3.5	5.0	mA
Operating frequency	f_{in}	AC coupling by 1000pF capacitor	80	–	300	MHz
Oscillator input frequency	f_{osc}	AC coupling by 1000pF capacitor	–	13	23	MHz
Input sensitivity	V_{in}	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensitivity	OSCin	AC coupling by 1000pF capacitor	500	–	–	mVp p
Input voltage (Div)	V_{IH}		$V_{CC} \times 0.7$	–	–	V
	V_{IL}		–	–	$V_{CC} \times 0.3$	V
Input current (Div)	I_{IH}		–	–	1.0	μA
	I_{IL}		–1.0	–	–	μA
Input current (OSCin)	I_{OSC}		–100		100	μA
Output voltage	V_{OH}	$V_{CC} = 3.0V$	2.6	–	–	V
	V_{OL}	$V_{CC} = 3.0V$	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	$V_{DO} \leq 3.6V$	–	–	1.1	μA

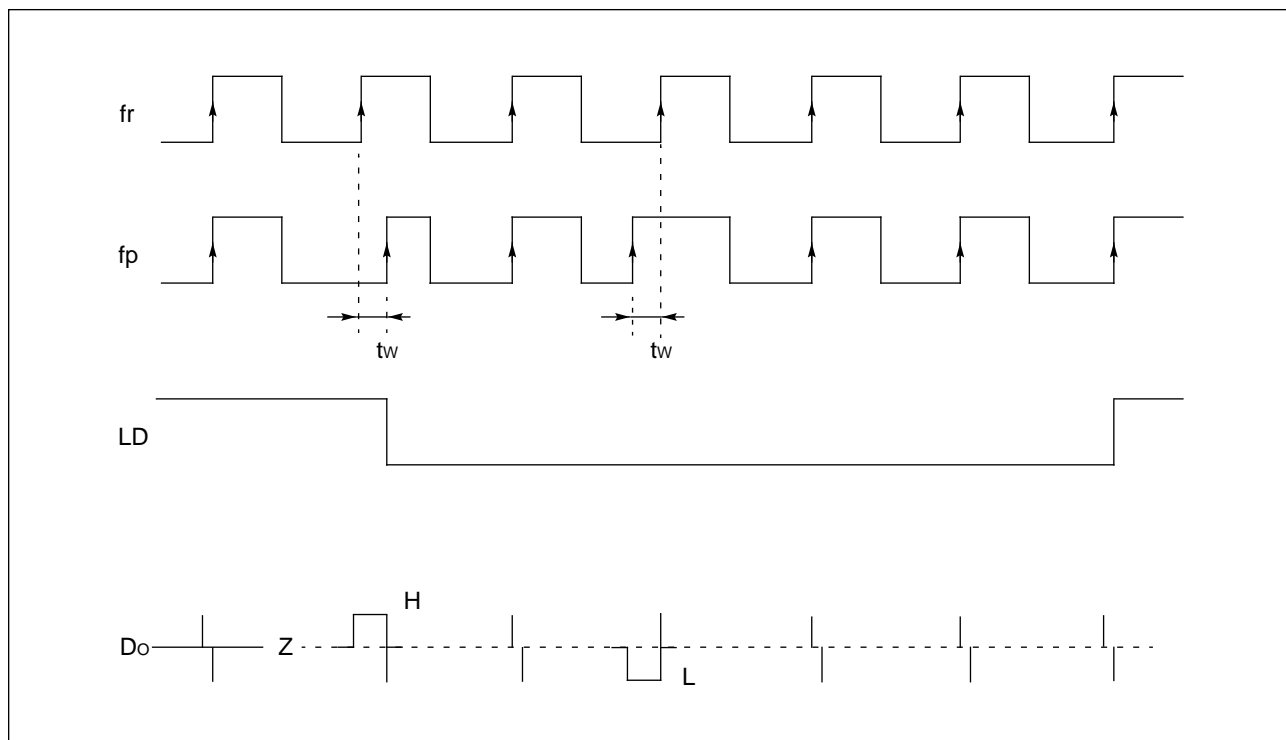
■ FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

$$f_{VCO} = \{(P \times N) + A\} \times f_{osc} \div R \quad (A < N)$$

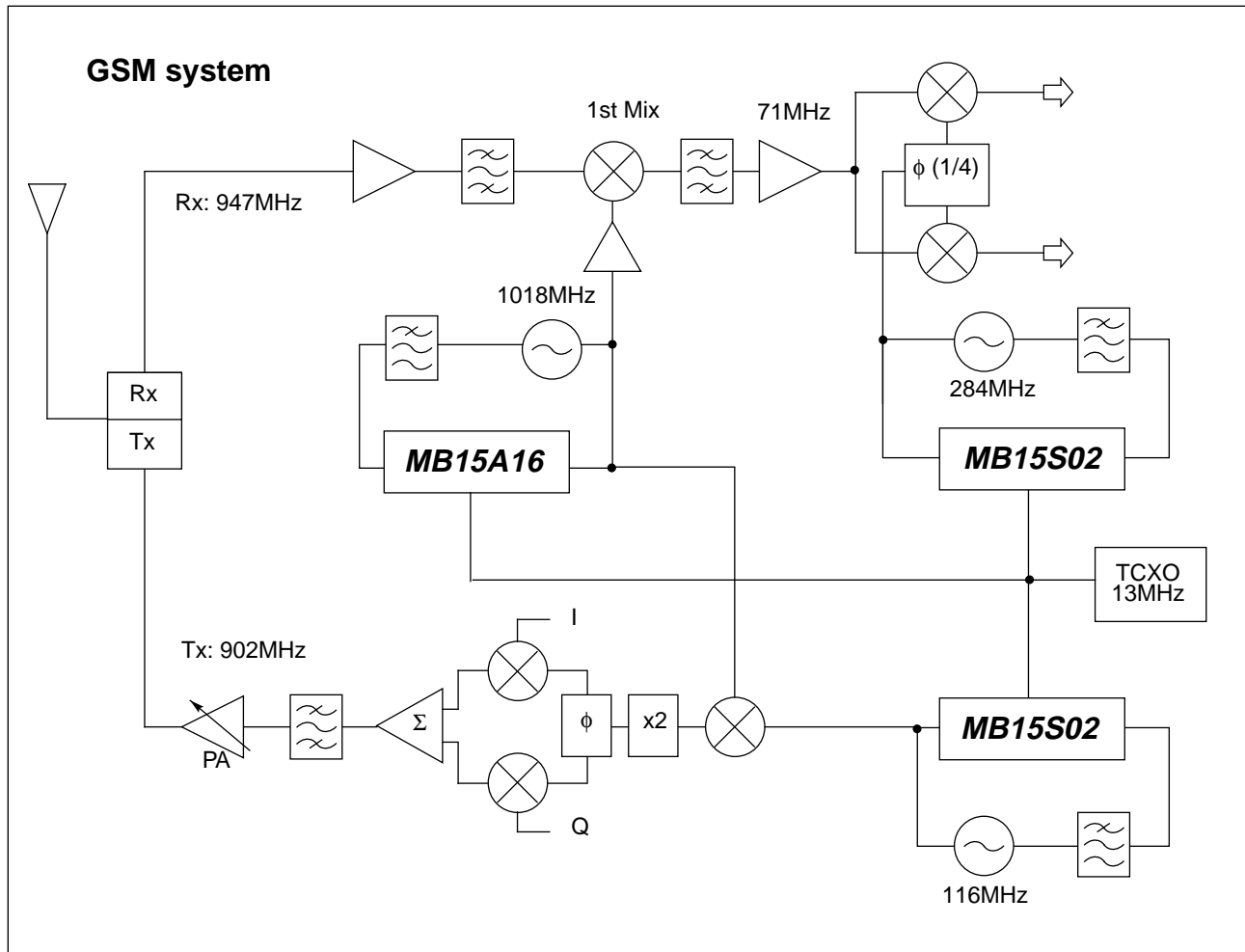
Symbol	Description	Div = "H"	Div = "L"
f _{vco}	Output frequency of external VCO	284.0 MHz	116.00 MHz
f _{osc}	Reference oscillation frequency	13.0 MHz	13.0 MHz
N	Divide ratio of the main counter	17	7
A	Divide ratio of the swallow counter	12	4
P	Preset divide ratio of dual modulus prescaler	16/17	16/17
R	Divide ratio of the reference counter	13 (fr = 1 MHz)	13 (fr = 1 MHz)

■ PHASE DETECTOR TIME CHART

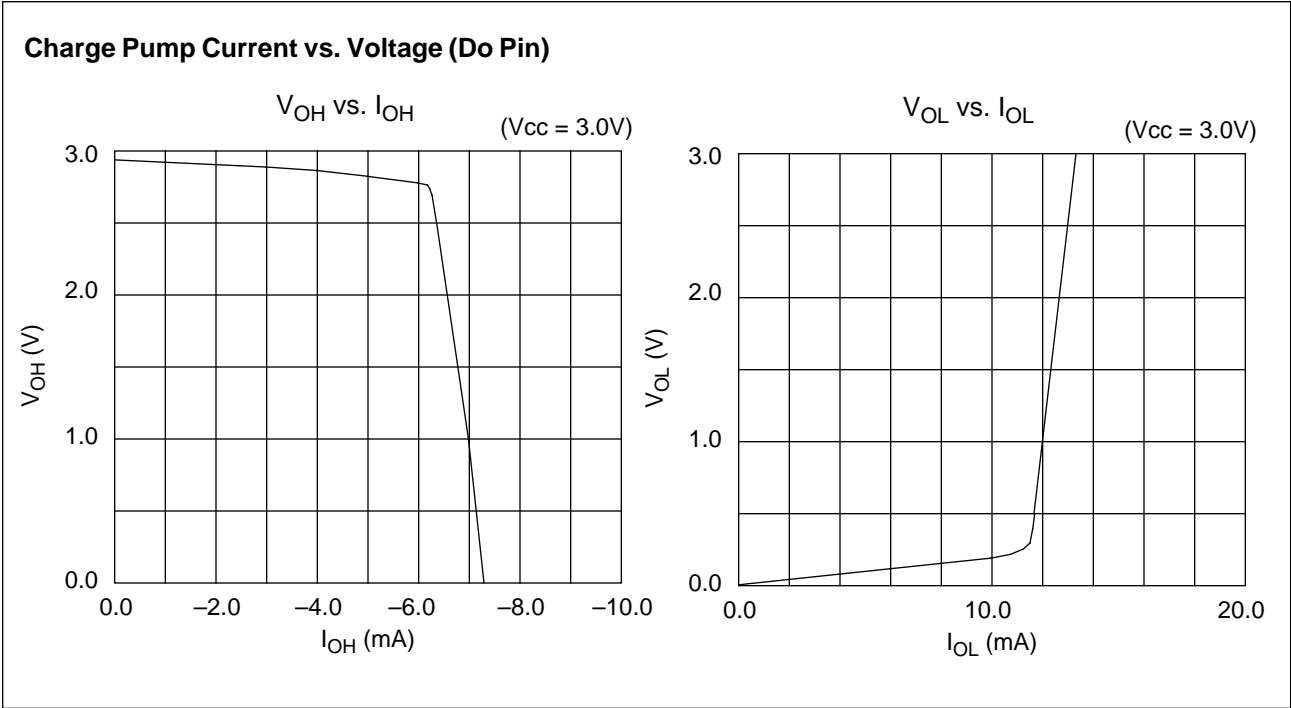


- Note:
- Phase difference detection range = -2π to $+2\pi$
 - Spikes on Do pulse during locking state are output to prevent dead zone.
 - LD output becomes low when phase difference is **tw** or more.
 - LD output becomes high when phase difference is **tw** or less and continues to be so for three cycles or more.
 - **tw** depends on OSCin input frequency.
(e.g. **tw**635ns to 1250ns when **fosc**in = 12.8 MHz)

■ APPLICATION EXAMPLE



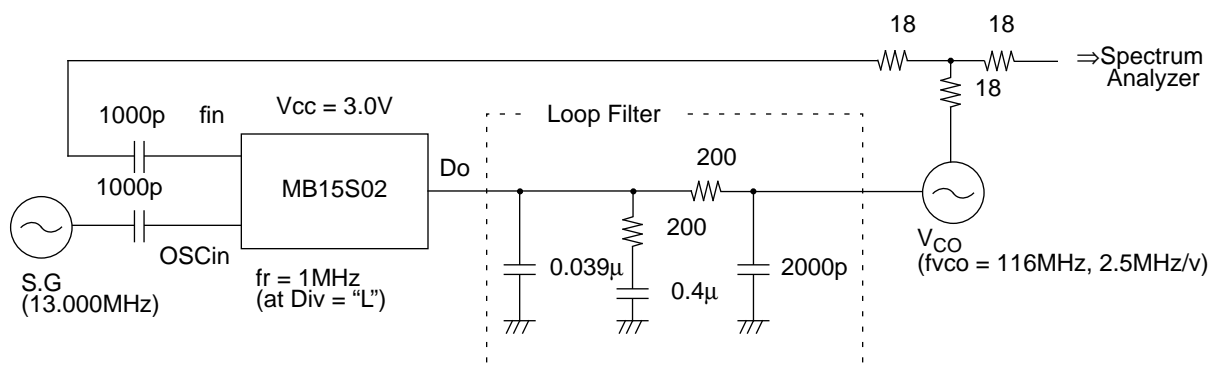
■ TYPICAL CHARACTERISTICS



■ APPLICATION INFORMATION

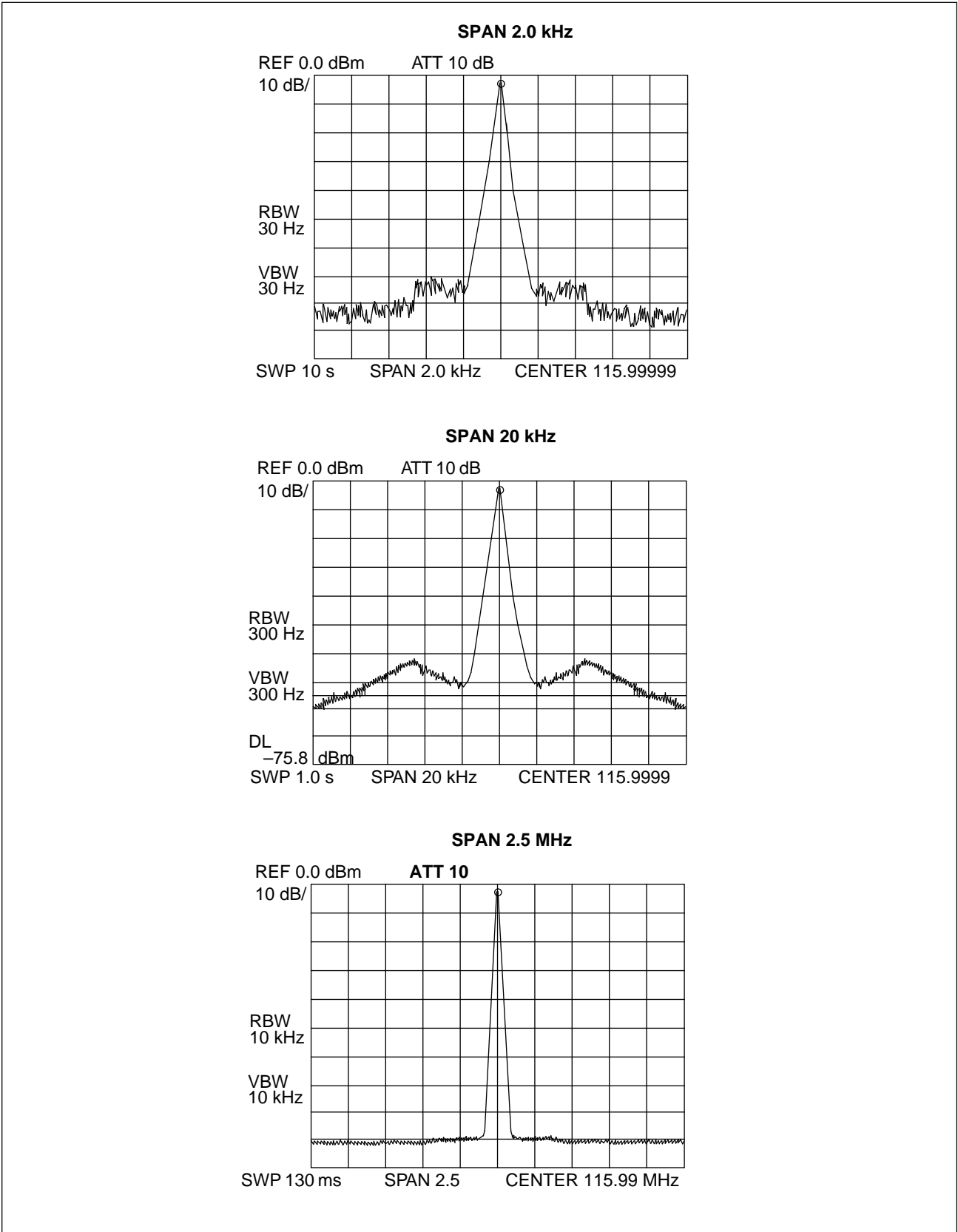
- Loop Characteristics (Div = "L")

(Measurement Circuit)



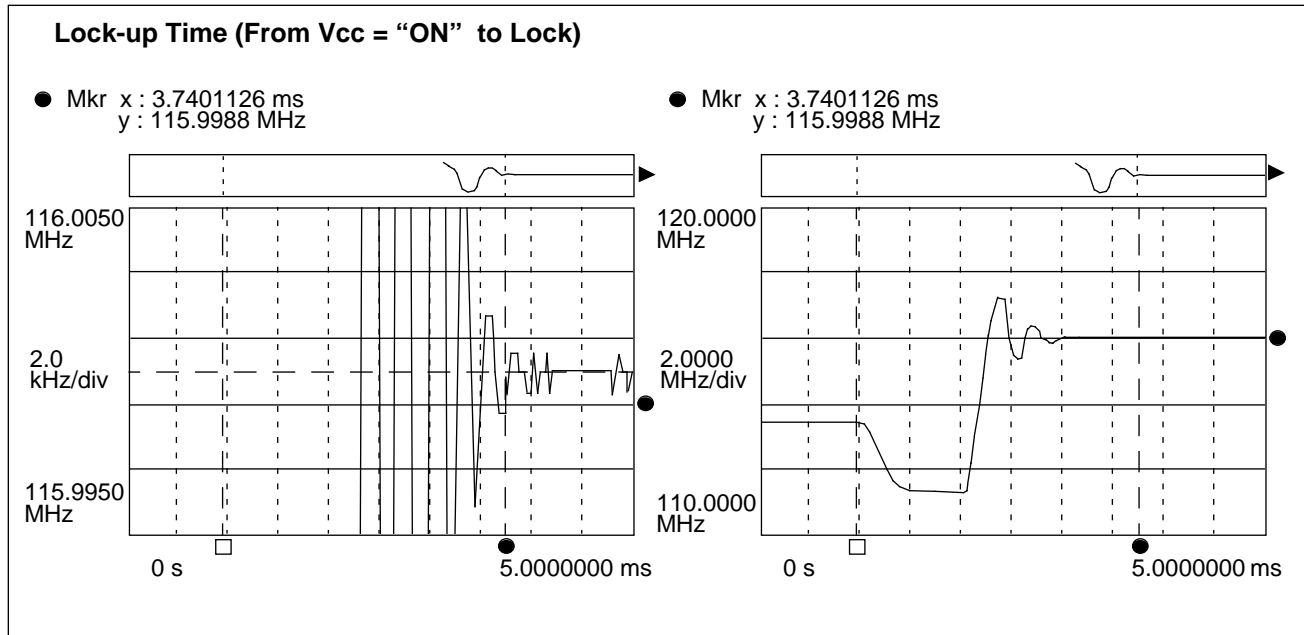
- (Measurement Results)

Parameter		Results	Unit	Note
PLL loop band width		8	kHz	f_{-3dB} at f_{vco}
PLL phase noise	$\Delta f = 1\text{kHz}$	96	dBc/Hz	
	$\Delta f = 10\text{kHz}$	102		
PLL reference spurious		86	dBc	$\Delta f = 1\text{MHz}$
PLL lock-up time (in $\pm 1\text{kHz}$)		3.7	ms	from Vcc OFF to Vcc ON



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■ ORDERING INFORMATION

Part number	Package	Remarks
MB15S02PFV	8 pin, Plastic SSOP (FPT-8P-M03)	

■ PACKAGE DIMENSION

